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Self-selective ferroelectric memory realized with semimetalic graphene channel

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A new concept of read-out method for ferroelectric random-access memory (FeRAM) using a graphene layer as the channel material of bottom-gated field effect transistor structure is demonstrated experimentally. The transconductance of the graphene channel is found to change its sign depending on the direction of spontaneous polarization (SP) in the underlying ferroelectric layer. This indicates that the memory state of FeRAM, specified by the SP direction of the ferroelectric layer, can be sensed unambiguously with transconductance measurements. With the proposed read-out method, it is possible to construct an array of ferroelectric memory cells in the form of a cross-point structure where the transconductance of a crossing cell can be measured selectively without any additional selector. This type of FeRAM can be a plausible solution for fabricating high speed, ultra-low power, long lifetime, and high density 3D stackable non-volatile memory.

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INTRODUCTION

There has been an enormous amount of interest in utilizing ferroelectric materials for fabricating non-volatile memory devices, so-called ferroelectric random-access memory (FeRAM), with low power consumption and high operation speed stemming from the voltage-driven fast switching of spontaneous polarization (SP) in a ferroelectric material[1–6]. However, the FeRAM structures that have been explored so far possess a couple of critical limitations including short cell lifetime due to the destructive read-out process or depolarization field[7–10].

As one way of overcoming such limitations, the FeRAM structure based on a field-effect transistor composed of graphene channel and ferroelectric gate insulator (ferroelectric GFET or FeGFET) has been studied by several research groups[11–16]. Most recently, there has been an experimental report demonstrating a quaternary-level memory device based on the four different polarization states observed in a semicircular top-gated ferroelectric nanowire FET[17]. In a FeGFET structure, the conductance of the graphene channel can vary depending on the direction of SP in the ferroelectric gate insulator due to the low density-of-states (DOS) of graphene associated with its unique energy-momentum relation near the Dirac point. Hence, the SP direction of the ferroelectric layer corresponding to the memory state of FeGFET can be sensed by measuring the conductance of the graphene channel. The main objective of all the previous works for FeGFET is basically for verifying this sensing mechanism. Although they could resolve the destructive read-out problem, the low on/off ratio of graphene channel conductance originating from the minimal conductance of graphene itself brings about the necessity of attaching a separate selector (transistor or diode) to each memory cell for realizing the random accessibility in read-out and write-in processes[15,16,18,19].

In this work, we demonstrate experimentally a new type of non-destructive read-out method for FeGFET structure which does not require any additional selector for random accessing. The proposed read-out method relies on measuring the transconductance of the graphene channel which is quantified to be the change of channel current divided by the change of gate voltage. Due to the ambipolar characteristics of graphene in its carrier transport, the sign of transconductance is found to be reversed as the SP direction of the ferroelectric layer switches. This sign reversal of transconductance can ensure the unambiguous read-out for the memory state of each cell specified by the SP direction of the ferroelectric layer. The physical mechanism for the sign reversal of transconductance will be discussed in detail.

RESULTS

Non-destructive read-out scheme enabling self-selective operation of FeGFET

The working principle of the non-destructive read-out method proposed in this work is as follows. For a typical back-gated FeGFET with its cross-sectional structure shown in Fig. 1a, the transconductance of graphene channel near-zero gate voltage (V_g) is expected to vary depending on the doping of graphene channel determined by the SP direction of ferroelectric layer thanks to the low DOS and the ambipolar carrier type of graphene[20,21]. Since the transconductance can be measured with a relatively small range of gate voltage around $V_g = 0$, the memory state specified by the SP direction of the ferroelectric layer can be read without being influenced by the gate voltage used for the transconductance measurement at all. In an ideal case, the transconductance of the graphene channel near $V_g = 0$ will be positive when the SP points upward since the graphene channel will be electron-doped due to the positive polarization charges induced on the top surface of the ferroelectric layer (Fig. 1b). On the other hand, if the SP points downward as shown in Fig. 1c, the negative polarization charges on the ferroelectric surface will make the graphene channel hole-doped so that the

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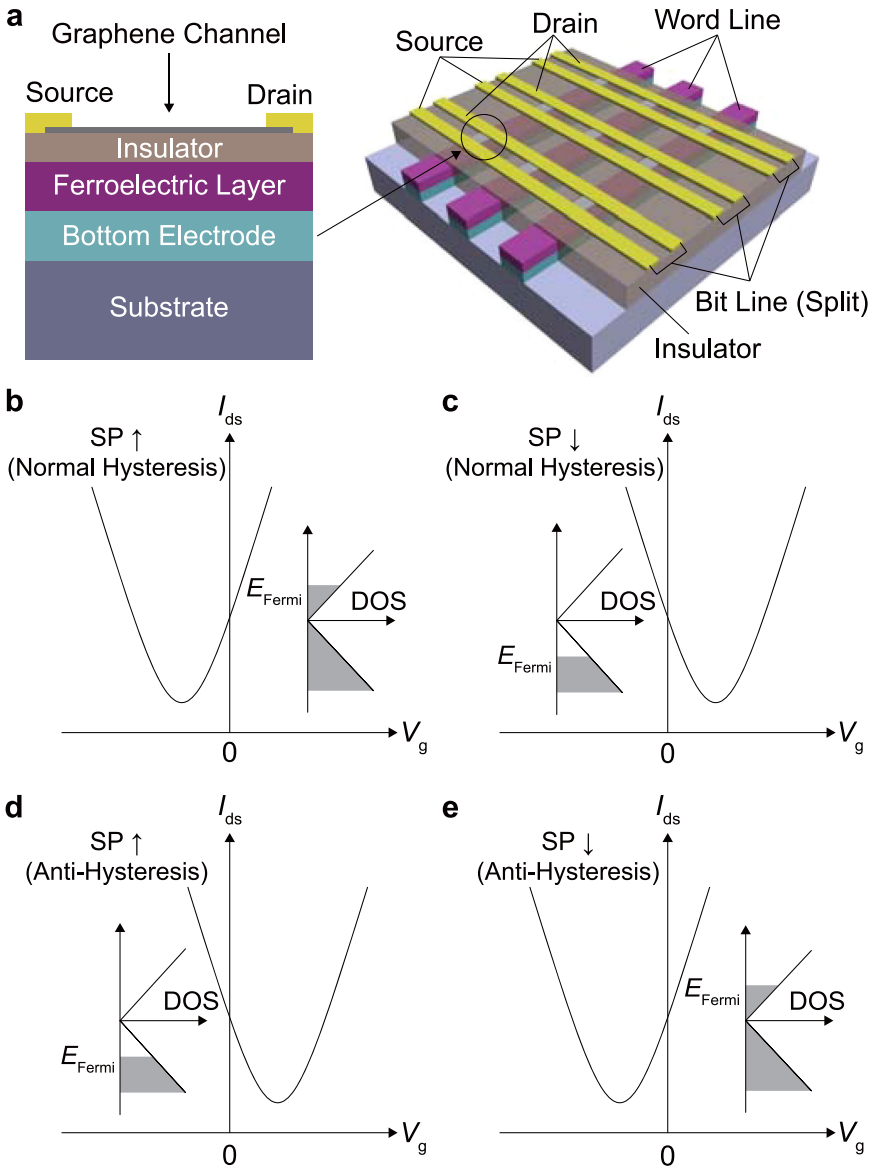

Fig. 1 Schematics of FeGFET and its I_{ds}–V_g curves. a Schematic illustration of FeGFET and its array structure. Drain-to-source current (I_{ds}) vs. gate voltage (V_g) curves for FeGFET showing the normal hysteretic (**b** upward and **c** downward SP), and anti-hysteretic (**d** upward and **e** downward SP) behaviors. The Fermi level matching with the doping of graphene channel is shown in the inset of each curve.

transconductance of the graphene channel will become negative. However, what has been observed experimentally so far is indeed opposite to the ideal expectation. It is found that the upward SP (positive surface polarization charges) makes the graphene channel hole-doped and the downward SP (negative surface polarization charges) electron-doped as shown in Fig. 1d, e, respectively[15,22–25]. This so-called anti-hysteretic behavior is considered to be due to the electron trapping and detrapping on the surface of the blocking insulator which is deposited on top of the ferroelectric layer. A more detailed discussion of the anti-hysteretic behavior will be given later. Here, it is noted that the proposed method is directly applicable for operating a cross-point type of FeGFET memory cell array, illustrated in Fig. 1a, with no selector device. The split bit-line structure of Fig. 1a makes all the memory cells in the same bit-line connected in parallel between shared source and drain electrodes. Accordingly, the gated channel properties of each FeGFET memory cell can be probed independently for the common source and drain voltages by ensuring that the ungated channel currents of the other FeGFET memory cells will just become an offset current as a sum. With this split bit-line structure, the operational characteristics of a single stand-alone FeGFET are naturally expected to manifest themselves even when being incorporated in an array form. Since the transconductance represents how the channel current is modulated as the gate voltage changes, the configuration of transconductance measurement will be established only for the crossing cell in the cross-point type array in Fig. 1a. This ensures that the memory state of the crossing cell, specified by its transconductance, can be sensed selectively without any additional selector device.

Fabrication of FeGFET memory cell

A prototype of FeGFET demonstrating the validity of the proposed read-out scheme was fabricated by following the procedures below. A 200 nm thick lead zirconate titanate (PZT, $Pb_{1.1}Zr_{0.35}Ti_{0.65}O_3$) layer grown with the sol–gel process on a Pt/Ti/SiO_2/Si substrate was chosen for the ferroelectric layer. The Pt/Ti (150 nm/10 nm) stacked layer acts as the back-gate electrode. The

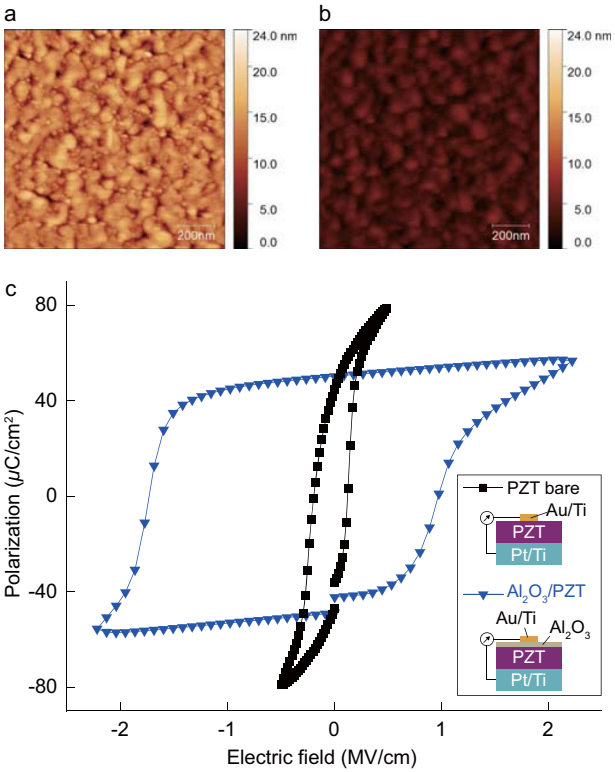

Fig. 2 Surface morphology and P–E hysteresis curves. AFM images were taken on the surface of **a** PZT layer and **b** Al_2O_3/PZT stack. **c** P–E hysteresis curves obtained for both PZT layer and Al_2O_3/PZT stack. The coercive field of the Al_2O_3/PZT stack appears to be much larger than that of the PZT layer while the remnant polarization almost does not change.

surface of the PZT layer is found to be somewhat rough as shown in the atomic force microscopy (AFM) image (Fig. 2a), typical for thin films grown with the sol–gel process. The average roughness is measured to be ~2.30 nm. This is noticeably large compared with the thickness of graphene (~0.34 nm) and the morphology of a graphene layer transferred on top of it can become quite undulated. Hence, a 15–30 nm thick Al_2O_3 film was deposited by using atomic layer deposition (ALD) on the PZT layer to reduce the surface roughness, down to ~1.07 nm as shown in Fig. 2b, and also block the leakage current through the PZT layer. In order to investigate the effect of the Al_2O_3 blocking layer on the apparent coercive field (E_c) and polarization, polarization vs. electric field (P–E) hysteresis loops were measured on both metal/PZT/metal and metal/Al_2O_3/PZT/metal capacitor structures as shown in Fig. 2c. In this case, the Al_2O_3 blocking layer is ~30 nm thick. The hysteresis loop measurements were performed with a triangular voltage sweep at 1 kHz frequency (Precision LC, Radiant Technologies). As shown in Fig. 2c, the existence of the Al_2O_3 layer is observed to increase the apparent coercive field noticeably to widen the curve while the saturation polarization (P_s) decreases moderately, and the remnant polarization (P_r) changes minimally as summarized in Table 1. In the sense of reducing the operation voltage of FeGFET, the Al_2O_3 layer is preferable to be as thin as possible. However, it should be thick enough to block the leakage current effectively. A non-ferroelectric insulating layer inserted in a metal/ferroelectric/metal stack can increase the depolarization field to cause the formation of reverse domains[26], reducing the polarization switching speed and limiting the device scaling. Therefore, it will be always beneficial to minimize the thickness of the Al_2O_3 layer by improving the insulating property of the ferroelectric layer. After the deposition of the Al_2O_3 layer, single-

Table 1. Material parameters extracted from P–E hysteresis measurements.

	Metal/PZT/metal	Metal/Al_2O_3/PZT/metal
P_s (μC/cm²)	79	57
P_r (μC/cm²)	45	50
E_c (kV/cm)	−190/127	−1730/975

Saturated polarization (P_s), remnant polarization (P_r), and coercive field (E_c) extracted from P–E hysteresis measurements for metal/PZT/metal and metal/Al_2O_3/PZT/metal capacitors.

layer graphene synthesized with chemical vapor deposition (CVD) on Cu foil was transferred on the Al_2O_3 surface by using the semi-dry transfer method demonstrated in ref. [27]. The transferred graphene layer was found to be mostly monolayer from Raman spectrum measurements. As shown in Supplementary Fig. 1, the ratio of 2D peak to G peak is close to two. Following the graphene transfer, the photolithography patterning and O_2 plasma etching processes were performed to form the graphene channel. Finally, the source and drain contacts were made with Au/Ti (50 nm/10 nm) stacked layers to complete the basic structure of FeGFET. For some of the fabricated FeGFETs, an additional AlO_x overlayer was formed on the graphene channel to modulate its doping type and density.

Operational characteristics of FeGFET without doping overlayer

Once the prototypic FeGFETs were fabricated, the drain-to-source current (I_{ds}) vs. back-gate voltage (V_g) curve with a small (0.1 V) drain-to-source voltage (V_{ds}) applied was measured first for the basic structure without the doping overlayer the schematic view of which is shown in Fig. 3a. The transfer curve (I_{ds}–V_g) measured at room temperature in air for the gate voltage sweeping between −8.0 V and 8.0 V is shown in Fig. 3b. The graphene channel is found to become hole-doped with positive back-gate voltages inducing upward SP and electron-doped with negative back-gate voltages inducing downward SP, which reveals the anti-hysteretic behaviors described earlier. Additionally, it is noted that the charge neutral point of the graphene channel appears larger in magnitude for p-type doping than n-type doping, implying that the graphene channel becomes p-type doped more easily than becoming n-type doped. This asymmetric doping tendency is considered to be another manifestation of the electron trapping and detrapping on the surface of the blocking insulator. A graphene film is known to be p-type doped typically when it is transferred on the surface of an oxide layer[27–29]. This is considered to be caused by the electron transfer from the graphene film into the trap states on the oxide surface as depicted in Fig. 3c. When the SP points downward, the repulsive force from the negative polarization charges induced on the ferroelectric surface will push some electrons trapped in the surface states back into the graphene channel. Then, the holes residing in the graphene channel will be annihilated by being recombined with the transferred electrons to reduce the p-type doping of the graphene channel. If the electron transfer from the trapped states to the graphene channel goes beyond the level of annihilating all the holes in the graphene channel, the doping type of graphene channel will change to n-type (anti-hysteretic). In the case of upward SP, the positive polarization charges induced on the ferroelectric surface will make some electrons transferred from the graphene channel into the surface trap states and the graphene channel will become p-type with the accompanying hole generation (anti-hysteretic). Since some amount of electrons in

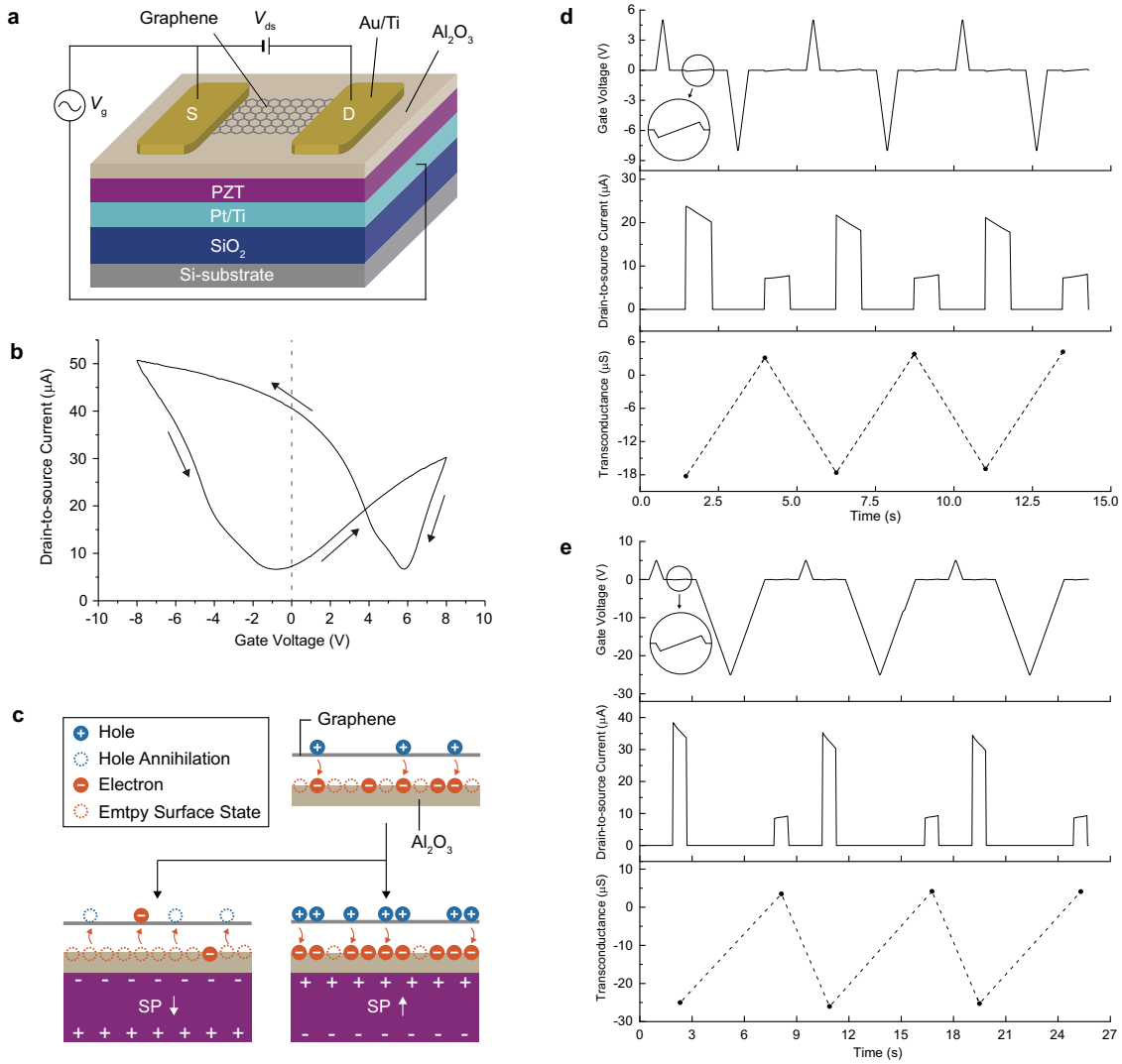

Fig. 3 FeGFET without doping overlayer. a Schematic view of the FeGFET without doping overlayer together with the configuration of electrical measurements. **b** Transfer curve (I_{ds}–V_g) obtained by sweeping the back-gate voltage as indicated by the arrows. **c** Schematic view of the electron transfer between graphene and Al_2O_3 layer causing the anti-hysteretic behavior in the drain-to-source current modulated by the ferroelectric SP. **d** Operational characteristics of the FeGFET showing the transfer curve in (**b**): (top) a series of triangular gate voltage pulses for write-in to switch SP direction of PZT layer alternatively (+5 V and −8 V) and saw-tooth gate voltage pulses for read-out (−0.1 V to +0.1 V), (middle) drain-to-source current obtained during read-out and (bottom) transconductance extracted from it showing the clear switching between upward and downward SP direction. **e** Operational characteristics of the FeGFET possessing relatively strong p-type doping tendency of graphene channel measured with the write-in voltages of +5 V and −25 V.

the graphene channel will be transferred already to the surface trap states even with no aid of SP, the additional electron transfer due to the upward SP will just enhance the p-type doping of the graphene channel.

In order to assess the operational characteristics of fabricated FeGFET as a memory device, the opposite-polarity voltage pulses were applied repeatedly on the back-gate electrode to switch the direction of SP in the ferroelectric layer and the transconductance of the graphene channel was measured between the voltage pulses. More concretely, as shown in the top graph of Fig. 3d, the high-voltage write-in triangular pulses were applied with their polarities being changed alternatively. Then, the low-voltage read-out saw-tooth pulses (from −0.1 V to 0.1 V) were applied between the write-in pulses. Just as a note, these switching characteristics measurements were performed at room temperature in the air. In our prototypic FeGFET, the PZT/Pt/Ti stack is global to cover the entire substrate. Hence, a substantial amount of capacitively-induced transient current decaying somewhat slowly can flow when a square pulse accompanied with abrupt voltage change is applied to the Pt/Ti back-gate electrode due to the large area of PZT/Pt/Ti stack. This transient current can disturb the subsequent transconductance measurement. The triangular pulse with its voltage increasing gradually was used to minimize the transient current. The middle and bottom graphs of Fig. 3d show the measured drain-to-source current and transconductance extracted from it, respectively. The write-in voltages used here were +5 V (upward SP) and −8 V (downward SP) which were chosen to ensure the clear switching of carrier type in the graphene channel within the range of back-gate voltage for the transfer curve shown in Fig. 3b. By considering the p-type doping tendency of graphene channel associated with the electron trap states on the blocking insulator surface, the write-in voltage for switching the graphene channel to n-type is preferable to be larger in magnitude than that for switching to p-type in order to make the measured transconductance more like symmetric between upward and downward SP. It

is apparent that the transconductance of the graphene channel changes its sign with the SP switching in the ferroelectric layer. One important notion here is that the sign of transconductance indicates the anti-hysteretic behavior of fabricated FeGFET, matching with the transfer curve in Fig. 3b. As described previously for the anti-hysteretic case, the graphene channel is found to be p-type (n-type) doped with the upward (downward) SP in the ferroelectric layer, leading to the negative (positive) transconductance. Since the electron trap density on the surface can change from batch to batch in growing the Al_2O_3 blocking insulator with ALD, the p-type doping tendency of the graphene channel can be various among the fabricated FeGFETs. Hence, the write-in voltage, especially for downward SP, also needs to be adjusted for switching the carrier type of graphene channel to n-type clearly. Figure 3e shows the operational characteristics of the FeGFET for which the p-type doping tendency was found to be stronger than other devices. In this case, the write-in voltage of −25 V was used for downward SP to achieve the associated transconductance comparable to the case of Fig. 3d. The endurance of fabricated FeGFET for multiple cyclic switching of memory state is also an important performance measure. Supplementary Fig. 3 shows the working cycle endurance of the FeGFET tested by performing the cyclic switching 1000 times in the air. The transconductance for downward SP is found to become saturated after decreasing shortly in the early stage of cycling while the transconductance for upward SP remains more steady throughout the entire cycling process. Most importantly, the sign of transconductance remains well-maintained for both directions of SP even after 1000 cycles.

Figure 4a shows the retention characteristics of the fabricated FeGFET obtained for both memory states (upward and downward SP) at room temperature and in vacuum (~10^{-3} Torr) for 24 h after a single write-in operation. As seen in the figure, the magnitude of measured transconductance decreases noticeably in the early stage of measurement. However, the decrease slows down and the transconductance gets saturated as time goes on. Most relevantly, the sign of transconductance is maintained for both upward and downward SP, indicating that the retention of memory state is pretty reliable. It is not quite conclusive what causes the decrease of transconductance after the write-in operation. One plausible explanation is the electrostatic screening for the surface polarization charges of the ferroelectric layer due to the hydronium (H_3O^+) and hydroxide (OH^-) ions residing between the graphene channel and the Al_2O_3 layer. It is known that the water molecules can be ionized into H_3O^+ and OH^- ions with the catalytic aid of oxide[30]. Hence, if there are water molecules sneaking into the gap between the graphene channel and the Al_2O_3 layer, some of them will be ionized, resulting in the coexistence of water molecules and H_3O^+ and OH^- ions. Although the graphene channel was formed by using the semi-dry transfer process with NO water involved[27], there will be always chances for ambient water molecules to go through some defective sites of graphene and stay between the graphene channel and the Al_2O_3 layer nearby those sites. The defective sites include the local tearing and loss occurring during the transfer process as well as the intrinsic grain boundaries and vacancies formed during the growth of the graphene layer. The FeGFET used for the retention test in the vacuum was also exposed to the air for a while before being put into the vacuum. Hence, a fair amount of water molecules is expected to go into the gap between the graphene channel and the Al_2O_3 layer. Once it was put into the vacuum, some of those water molecules might be released into the vacuum due to the pressure difference between inside and outside the gap, reducing the number of water molecules in the gap. When the polarization charges on the ferroelectric surface switch to the positive (upward SP), OH^- ions will be attracted toward the Al_2O_3 layer, and H_3O^+ ions will be repelled toward the graphene layer. Conversely, if the polarization charges switch to the negative (downward SP), H_3O^+ ions will be attracted toward the Al_2O_3 layer, and OH^- ions will be repelled toward the graphene layer. In either case, the two types of ion separated spatially will generate the electric field in the gap between graphene and Al_2O_3 layer along the direction opposite to that of the electric field originating from the polarization charges on the ferroelectric surface. Hence, some of the electrons transferred to either graphene channel or Al_2O_3 layer by the electric field from the ferroelectric polarization charges can be transferred backward (electron back-transfer) to reduce the doping concentration of the graphene channel (Fig. 4b, c). The motion of attracted ions is very likely to be slower than the electron transfer between the graphene channel and the surface trap states of the Al_2O_3 layer. Therefore, just after the SP of the ferroelectric layer switches upward or downward, the electron back-transfer will be pretty

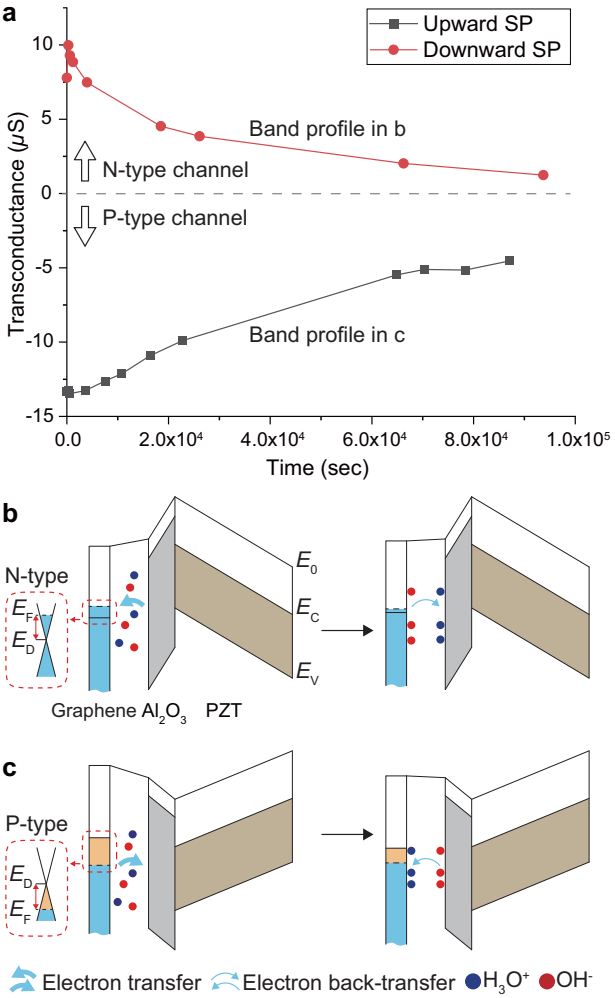

Fig. 4 Retention characteristics of FeGFET without doping overlayer. a The retention of memory state tested for both upward (black squares) and downward (red circles) SP at room temperature and in vacuum for 24 h after write-in process. The schematic time-evolving band profiles of graphene/Al_2O_3/PZT stack structure for **b** downward and **c** upward SP. After the write-in process, the H_3O^+ and OH^- ions separated spatially between graphene and Al_2O_3 layer weaken gradually the electric field effect from the surface polarization charges of ferroelectric layer, making some of the electrons transferred to either graphene channel or Al_2O_3 layer by the electric field from the surface polarization charges transferred backward (electron back-transfer). Here, E_F: Fermi level, E_D: Dirac point, E_0: Vacuum level, E_c: Conduction band edge, E_v: Valence band edge.

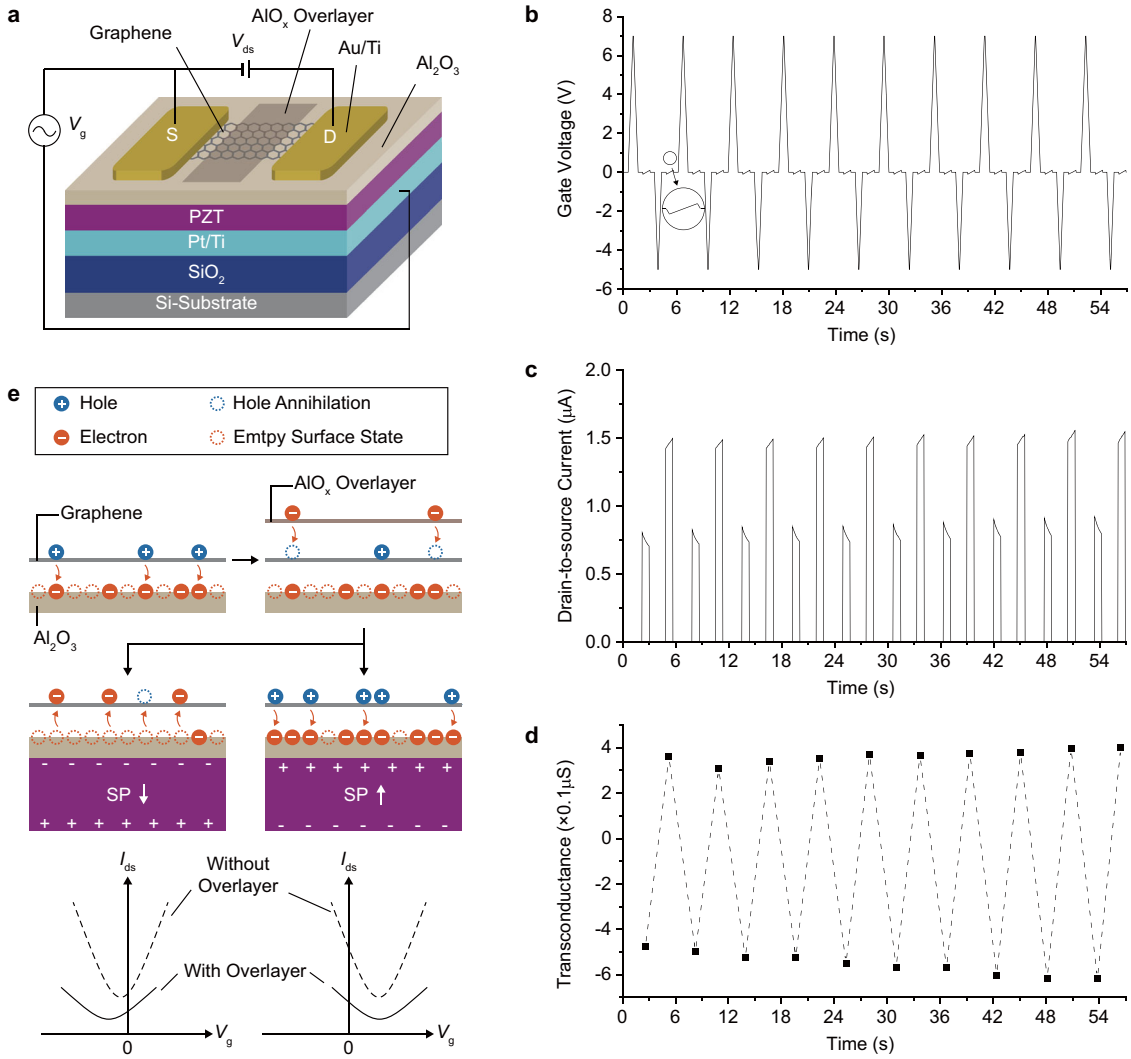

Fig. 5 FeGFET with AlO_x doping overlayer. a Schematic view of the FeGFET with AlO_x doping overlayer together with the configuration of electrical measurements. **b** A series of triangular gate voltage pulses for write-in to switch the SP direction of the PZT layer alternatively (+7 V and −5 V) and saw-tooth gate voltage pulses for read-out (−0.1 V to +0.1 V). **c** Drain-to-source current obtained during the read-out voltage sweep which is more symmetric with respect to zero gate voltage compared with that of FeGFET without doping overlayer and **d** transconductance extracted from (**c**). **e** Schematic view showing the electron transfer between graphene and Al_2O_3 doping layer and the influence of AlO_x overlayer on the drain-to-source current modulated by the ferroelectric SP.

weak and the graphene channel will be doped maximally for the given SP. Since then, the number of spatially-separated ion pairs, determining the degree of electron back-transfer, will increase somewhat rapidly in the beginning and becomes saturated slowly. Synchronously, the doping of the graphene channel will also decrease rapidly and get saturated slowly. In fact, this trend of graphene channel doping matches well with the measured transconductance of FeGFET shown in Fig. 4a.

In order to validate the electron back-transfer scenario, the retention measurements were performed also in the air and the measured data are shown in Supplementary Fig. 2. Since the water molecules residing between the graphene channel and the Al_2O_3 layer will hardly come out in the air, the transconductance change is expected to be more significant and rapid. The measured transconductance indeed shows the expected trend. Moreover, the transconductance is found to change its sign for downward SP, more concretely from positive (n-type) to negative (p-type), as time goes on. This behavior can be understood with the notion of the electric field effect from the negative polarization charges on the ferroelectric surface being suppressed strongly by the opposite-direction electric field between H_3O^+ and OH^- ions, making the situation become as if the ferroelectric layer does NOT exist (Fig. 3c).

Operational characteristics of FeGFET with AlO_x doping overlayer

In order to make the write-in voltage of FeGFET more symmetric, it is necessary to minimize the initial doping of the graphene channel so that the associated charge neutrality point becomes as close to 0 V as possible. Since it was quite challenging to passivate the surface trap states of the Al_2O_3 layer, the counter-doping of graphene channel achievable by forming a doping overlayer on top of it has been pursued. We first formed a ~2 nm thick Al film pattern covering the graphene channel by using e-beam evaporation and photolithography. Then, the Al film pattern was left in the air over a day to make it oxidized (Fig. 5a). Because of the relatively low work-function of Al, some amount of electrons are expected to be transferred from the Al film to the p-type

doped graphene channel so that the graphene channel becomes nearly intrinsic. Once this counter-doping of graphene channel is completed, the subsequent ambient oxidation process will convert the Al film to a non-stoichiometric AlO_x layer. The AlO_x overlayer formed this way will be sufficiently insulating to make the flow of charge carriers confined in the graphene channel.

Figure 5b shows triangular voltage pulses applied on the back-gate electrode where the write-in voltages are +7 V and −5 V for upward and downward SP, respectively. As before, the saw-tooth pulses sweeping from −0.1 V to 0.1 V were used for read-out. The anti-hysteretic behavior in the doping of graphene channel is observed again with the clear sign reversal of channel transconductance depending on the SP direction as noticed in Fig. 5c, d. As illustrated in Fig. 5e, the electrons transferred from the doping overlayer will be recombined with the holes in the graphene channel to reduce its p-type doping. If so, the write-in voltage for switching the SP downward to convert the graphene channel doping to n-type can decrease accordingly. This expectation indeed matches well with the measurements, confirming that −5 V is sufficient to turn the graphene channel into n-type. Another important notion is that the drain-to-source current and the channel transconductance were suppressed quite a lot, both over 10 times, compared with the case of no doping overlayer. This suppression is considered to be due to the Coulomb scattering from the charge impurities in the AlO_x overlayer which reduces the carrier mobility in the graphene channel. Since the channel conductance and transconductance are proportional to the carrier mobility, the reduction of carrier mobility will deteriorate them apparently. The I_{ds}–V_g curves sketched at the bottom of Fig. 5e represent this influence of carrier mobility reduction. Indeed, the carrier mobility reduction due to the AlO_x overlayer varies somewhat noticeably from sample to sample. This variation is considered to stem mainly from the inconsistent ambient condition, especially humidity, for oxidizing the overlayer in air and the thickness difference of the overlayer. The Al film for forming the AlO_x overlayer is very thin, targeted to be 2 nm. Hence, the deviation of its thickness from the target value, occurring during deposition, can be non-trivial. Differently from the FeGFET shown in Fig. 5, some FeGFETs show less reduction of transconductance. In addition to the counter-doping effect, the AlO_x overlayer was found to improve the memory retention of FeGFET. Supplementary Fig. 4 shows the retention characteristics of FeGFET with the AlO_x overlayer measured at room temperature and in vacuum (~10^{-3} Torr). Compared with the case of NO overlayer (Fig. 4a), the measured transconductance appears more stable. In the Al deposition process, the graphene channel stays in a high vacuum (~10^{-7} Torr) over an hour before starting the deposition. Accordingly, the water molecules residing in the gap between graphene and Al_2O_3 layer can be removed well, and the Al layer deposited subsequently can encapsulate the graphene channel to prevent water molecules from sneaking into the gap afterward. The improved retention of FeGFET with the AlO_x overlayer is considered to signify the reduced number of water molecules in the gap between graphene and Al_2O_3 layer. By the way, the encapsulation of the Al layer will NOT be perfect since the complete surface coverage is hardly expected for only ~2 nm thick thin film. Therefore, the retention characteristics of FeGFET with the AlO_x overlayer are also likely to deteriorate when the device sits in air. This tendency has actually been observed in our measurements.

DISCUSSION

Based on the experimental data presented so far, it can be claimed that the proposed read-out scheme measuring the transconductance of graphene channel in FeGFET can be an efficient and reliable way to realize the selector-free random-access non-volatile memory in the form of a cross-point array (Fig. 1a). The configuration of transconductance measurement is established only for the crossing cell where the top row of graphene channel (bit line) and the bottom gate electrode (word line) are crossed perpendicularly with each other, enabling the random-access to an arbitrary memory cell without any selection device. The random-access aspect will be valid also for write-in since the switching of SP in the ferroelectric layer is driven by the electric field stemming from the voltage difference between the top graphene channel and the bottom gate electrode. If the voltages applied on the graphene channel and the bottom gate electrode are smaller in magnitude than the coercive voltage of the ferroelectric layer but their difference is beyond the coercive voltage, only the ferroelectric layer of the crossing cell will have a sufficiently large electric field to switch the SP in it. Another advantage of measuring transconductance is that the direction of SP can be sensed in non-destructive manners. This implies that there is no need to switch the SP momentarily for figuring out its direction by inducing a displacement current (conventional destructive read-out). The non-destructive read-out is a crucial factor for resolving the fatigue problem of the ferroelectric layer which is a long-standing weakness of the conventional ferroelectric memory[31,32].

In conclusion, we proposed a new concept of read-out method for FeRAM with the bottom-gated FET structure composed of a graphene channel[33,34] and a ferroelectric gate insulator and demonstrated its validity and reliability experimentally. The transconductance of the graphene channel was measured to have opposite signs for two opposite directions of SP in the underlying ferroelectric layer, which is the essential working principle of the proposed read-out method. The unambiguous sensing of SP direction, corresponding to the memory state of FeRAM, with transconductance measurements, makes it possible to construct an array of ferroelectric memory cells in the form of cross-point structure where the memory state of a crossing cell can be read out selectively without any additional selector. Accompanied by the voltage-driven fast switching of ferroelectric SP, this FeRAM structure can be a plausible solution for fabricating high speed, ultra-low power, long lifetime, and high density 3D stackable non-volatile memory. As compared in Table 2, its operational performances even might be comparable to the Si-based Dynamic Random Access Memory (DRAM), the most representative high-speed memory, with an additional benefit of being non-volatile.

METHODS

Device fabrication (more detailed)

As described previously, a 200 nm thick PZT ($Pb_{1.1}Zr_{0.35}Ti_{0.65}O_3$) ferroelectric layer was grown with the sol–gel process on a Pt/Ti/SiO_2/Si substrate. The Pt/Ti (150 nm/10 nm) stacked layer was used as the back-gate electrode. After cleaning the surface of PZT film consecutively with acetone and methanol in

Table 2. Operational performances of commercial memories and FeGFET.

	Write time	Read time	Endurance	Retention
DRAM	<10 ns	<10 ns	10^{16}	V (<100 ms)
NAND Flash	200 μs/page	<50 ns	10^5	NV (>10 years)
FeGFET	<10 ns	<10 ns	10^{14}	NV (>10 years)

The operational performances of most representative commercial memories, DRAM and NOT-AND (NAND) Flash, are known generally. For FeGFET, the operational performances expected from its working principles or known for the conventional type of FeRAM are listed. Here, V: volatile and NV: non-volatile.

an ultrasonic bath for 5 min each, a 15–30 nm thick Al_2O_3 film was deposited by using ALD at 250 °C. The trimethylaluminum (TMA) and H_2O were used as the precursor and the oxidant, respectively. Then, a single layer of CVD graphene was transferred onto the Al_2O_3 surface by using the semi-dry transfer method where the graphene layer supported by a Polymethyl Methacrylate (PMMA) layer is transferred directly on the surface with the aid of an additional flexible supporter (Kapton tape) attached to the PMMA layer of PMMA/graphene stack. After the graphene transfer, the photoresist etch mask was patterned with the photolithography process which consists of spin-coating Hexamethyldisilazane (HMDS) and AZ5214E photoresist layers successively (HMDS: 1500 rpm for 30 s, AZ5214E: 4000 rpm for 30 s), exposing the coated layers to ultraviolet light with the power of 100 mJ/cm^2, and developing the exposed areas with AZ300MIF developer for 60 s. Then, the portion of graphene film uncovered with the photoresist mask was etched with O_2 plasma to form a strip-shaped graphene channel of ~10 μm width. Finally, the source and drain electrodes were formed on both ends of the graphene channel by depositing Au/Ti (50 nm/10 nm) film stacks on the patterned photoresist layer with electron beam (e-beam) evaporation and performing the lift-off process in acetone over a day. Excluding the area of the graphene channel covered with the source and drain electrodes, the actual channel length of the fabricated FeGFET is ~20 μm. For the AlO_x doping overlayer, a ~2 nm thick Al film pattern covering the entire width of graphene channel was formed by using photolithography, e-beam evaporation, and lift-off process in successive manners, and then it was oxidized in the atmosphere over a day.

DATA AVAILABILITY

The datasets generated and/or analyzed during the current study are available from the corresponding author on reasonable request.

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AUTHOR CONTRIBUTIONS

S.J., J.P., and K.P. conceived and designed the device structure and the experiments. S.J., J.P., J.K., and W.S. fabricated FeGFETs. S.J., J.P., J.J., H.P., and M.S. performed the electrical characterization for the fabricated devices. S.J., J.P., J.K., W.S., J.J., M.S., and K.P. analyzed the measured data. S.J., J.P., J.K., W.S., J.J., H.P., M.K., S.K., M.S., I.W.K., T.H. K., and K.P. discussed the results and wrote the paper.

COMPETING INTERESTS

The authors declare no competing interests.

ADDITIONAL INFORMATION

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