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Reduction of the Circulating Current among Parallel NPC Inverters

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Reduction of the Circulating Current among Parallel NPC Inverters

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***Abstract*—In medium/high power applications including smart transformers, active power filters and wind turbines, 3-level Neutral-Point-Clamped (NPC) inverters proved to be a reliable solution, providing high efficiency and low harmonic distortion. In practice, several NPCs are parallel connected and operated in interleaved to further increase the power handling and reduce the line filters size. However, if such configuration has a common dc-link, High-frequency Zero-Sequence Circulating Current (HF-ZSCC) arises among the inverters, increasing power losses of the switching devices and propagating the stress on the dc-capacitors. Moreover, the amplitude of the HF-ZSCC is inversely proportional to the filter inductance size, therefore in real applications it can reach hundreds of Amperes even with relatively low output currents. The research on the HF-ZSCC is mostly concentrated on 2-level inverters for low voltage grids and traction applications, where the inductance size is relatively big and the HF-ZSCC does not affect the system efficiency. Differently, NPCs provide higher switching degree of freedom and more sophisticated methods can be applied to reduce the HF-ZSCC. This paper investigates a Double-Reference Pulse-Width Modulation (DRPWM) as solution for diminishing the HF-ZSCC in paralleled NPCs. The performance of DRPWM method is confirmed by both simulation and experiments, performed on a 1.6MVA system.**

***Index Terms*—PWM inverters, common dc-link, modulation techniques, circulating current, parallel inverters, neutral-point-clamed inverters**

I. Introduction

THREE–LEVEL Neutral-Point-Clamped Voltage-Source Inverters (NPC VSI) have been widely used for decades. Compared to Two-Level VSIs (2L-VSI), the NPC VSI topology offers higher power handling, better current quality and reduced stress on switching devices and capacitors [1]. As a result, the NPC topology is mainly utilized in Medium Voltage (MV) and High Voltage (HV) applications, like smart transformers [2], Static Synchronous Compensators (STATCOM) [3], wind turbines [4], electric drives [5], Active Power Filters (APF) and Electric Vehicles (EV) [6], [7].

To further extend the aforementioned benefits, in particular the power-rating of the system, several VSIs are often connected in parallel [8]–[10]. Such configuration provides additional degree of freedom allowing to utilize interleaved Pulse-Width Modulation (PWM). In this case, the PWM cycles can be phase-shifted by proper angle, yielding less voltage and current ripples at the ac terminal, and therefore reduced size of the line filters. However, despite these advantages, paralleled VSIs with shared DC-link have Zero-Sequence Circulating Current (ZSCC) [10]. This current increases thermal stress of dc-link capacitors, overstresses semiconductors, causes higher power loss and saturate line inductors [1].

The ZSCC can be divided into 2 categories: (a) low-frequency ZSCC (LF-ZSCC) which is mostly influenced by the asymmetry of inverter parameters, like tolerance of filter inductors and difference in duty cycles or dead-time effects and (b) high-frequency ZSCC (HF-ZSCC), coming from the differential common-mode voltage (DCMV) due to the interleaving modulation, and depending on the filter inductance size.

There have been a lot of research about the reduction of the ZSCC in parallel 2L-VSIs. The simplest way to avoid the ZSCC is to add isolated transformers or use separate dc-sources as it was proposed in [11], [12]. Some studies suggest to reduce the ZSCC with the implementation of additional interphase inductors [8], however the aforementioned methods add complexity to the realization and significantly increases the system volume. Some studies propose deadbeat- [9] or PI- [13] control strategies to minimize the LF-ZSCC. The deadtime effects on the ZSCC were thoroughly studied in several research works, however it was proved that the deadtime affects only the low-frequency part [14], [15].

Nevertheless, in MV- and HV-, applications, it is common to operate at low switching frequencies and utilize smaller line filters to increase the power density, which is a very critical parameter, especially for high power range. Such configuration yields much greater contribution of the HF-ZSCC compared to that of the LF-ZSCC. In fact, in such systems the HF-ZSCC can reach hundreds of Amperes [16], [17] which can significantly increase the power losses on semiconductors or cease the inverter from running due to constant triggering of over-current protection system.

Thus the reduction of the HF-ZSCC is very important, as it deals more stress and power loss to the system than the LF-ZSCC, which can always be compensated by implementing

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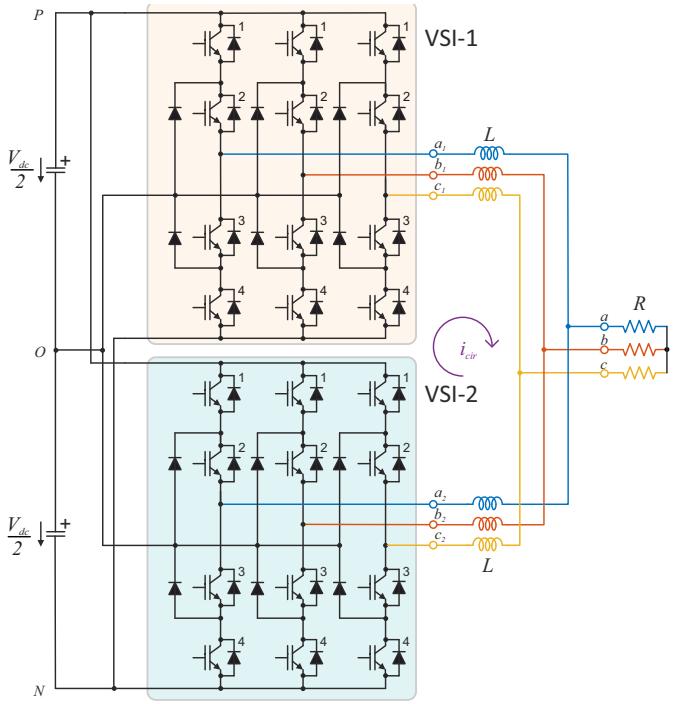

Fig. 1. Topology of the paralleled NPC VSI.

already mentioned methods into the system. The key to diminish the HF-ZSCC is to reduce the common-mode voltage (CMV) of each VSI. Expanded number of switching states and voltage levels of the NPC VSIs gives more possibilities for the modulation methods. In previous research [10], [18] it was proved that the Phase-Disposition (PD) PWM grants lower HF-ZSCC compared to that of the Alternative-Phase-Opposite-Disposition (APOD) PWM. Still, the HF-ZSCC can be further diminished by changing the reference signals of the NPC VSI. The simplest way is to use Space-Vector Pulse-Width Modulation (SVPWM) which is known for better dc-voltage utilization and lower CMV as compared to standard Sine Pulse-Width Modulation (SPWM). Furthermore, most HF-ZSCC reduction methods are based on SVPWM and require only small changes in software [19]. Yet, the research on the reduction of the HF-ZSCC in paralleled NPC VSIs is still a relevant topic seldom covered in research studies.

This paper proposes a carrier-based Double-Reference Pulse-Width Modulation (DRPWM) method to reduce the CMV and the HF-ZSCC of parallel-connected NPC VSIs. The method uses two different reference signals for upper and lower parts of each arm of the NPC VSI. These signals have overlapping regions near the zero-crossing point, which reduces the CMV and therefore the ZCSS. The performance of the proposed method is evaluated and analyzed in time- and frequency- domains and confirmed by simulations and experiments.

This paper is structured as follows: The concept of the CMV and the HF-ZSCC is described in Section II along with a discussion on considered modulation methods. The detailed analysis of the HF-ZSCC generation for SPWM, SVPWM and DRPWM are given in Section III. Simulation and experimental results to estimate the performance of the proposed method are shown in Section IV. Lastly, Section V provides the conclusions.

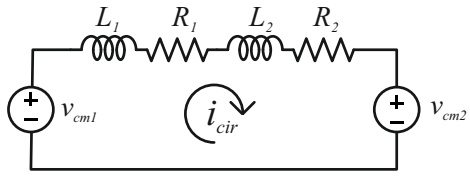

Fig. 2. Equivalent circuit of the DCMV and the HF-ZSCC.

II. Parallel NPC VSI

A. Circulating Current

This paper focuses on the high-frequency circulating current reduction in paralleled NPC VSIs with common dc-link and ac-load as shown in Fig. 1. As mentioned before, the parallel operation of the VSI increases the power level of the system due to the equal distribution of the output current. Furthermore, the interleaved operation of the VSIs can remarkably reduce the output current ripple. In this case, the PWM carriers of the VSIs are shifted by $360^o/n$, where n is the number of paralleled VSIs [20]. For a simple example with two parallel-connected VSIs, the shift angle is 180^o. The PWM carrier shift yields the change of the switching states, and therefore, DCMV is generated between the VSIs, leading to the generation of HF-ZSCC among the VSIs. The concept of the DCMV is depicted in Fig. 2 as an equivalent circuit, which demonstrates a possible path for the HF-ZSCC. The DCMV v_{dcm} is defined as

$$v_{dcm} = v_{\mathrm{cm1}} - v_{\mathrm{cm2}} = \frac{\sum v_{\mathrm{xo1}}}{3} - \frac{\sum v_{\mathrm{xo2}}}{3} \tag{1}$$

where v_{cm1} and v_{cm2} are the CMV of the VSI-1 and the VSI-2, respectively. v_{xo1} and v_{xo2} (x = a,b,c) are phase-to-neutral voltages of each VSI. Then, according to the Kirchhoff's law, the loop expression of the equivalent circuit is

$$v_{\mathrm{cm1}} - v_{\mathrm{cm2}} = L_1 \frac{di_{\mathrm{cir}}}{dt} + L_2 \frac{di_{\mathrm{cir}}}{dt} + R_1 i_{\mathrm{cir}} + R_2 i_{\mathrm{cir}} \tag{2}$$

where L_1, L_2, R_1 and R_2 are respectively the filter inductance and resistance of each VSI, while i_{cir} is the HF-ZSCC. Ideally in parallel configurations filters have the same inductance and summation of L_1 and L_2 results in $2L$.

As is evident from Fig. 2, if the CMVs of both VSIs are identical, (2) becomes zero, resulting in dissolution of the HF-ZSCC [21]. It is possible when both VSIs are operated simultaneously and the PWM is synchronized.

However, when paralleled VSIs are run in interleaved manner, the CMV of each inverter is different, thus, the HF-ZSCC between the inverters arises as

$$i_{\mathrm{cir}} = \frac{3}{n \cdot L} \int v_{\mathrm{dcm}}(t) dt \tag{3}$$

The HF-ZSCC proportionally depends on the CMV of each VSI. However, it is inversely-proportional to the inductance volume, meaning that for small inductances the amplitude of the HF-ZSCC is drastically increased.

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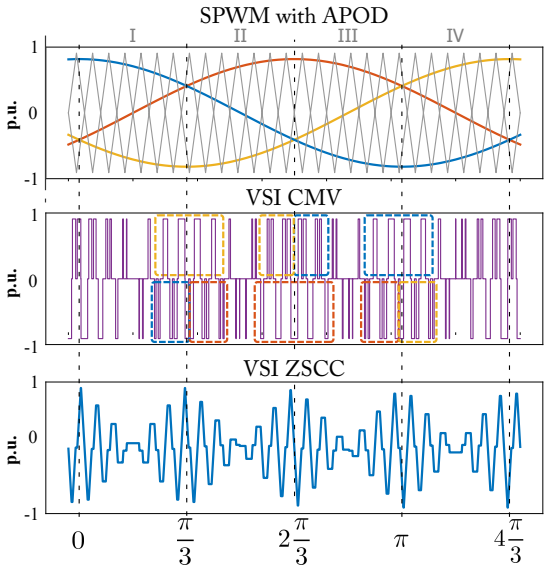

Fig. 3. Development of the circulating current as a function of CMV.

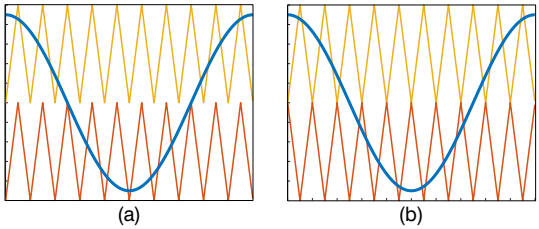

Fig. 4. Carrier Arrangement of the PWM: (a) PD and (b) APOD.

It is worth mentioning that filter inductance value of each VSI L_n decreases according to the number of interleaved VSIs connected in parallel, as each VSI contributes to the increase of the effective frequency

$$L_{\text{eff}} = L_n \cdot n \tag{4}$$

Fig. 3 shows the development of the HF-ZSCC with an example of single VSI with APOD PWM. Small carrier-fundamental frequency ratio is chosen for the sake of clarity. It can be seen, that the CMV of the VSI has different pulse width depending on the relation between the duty cycles. Moreover, it has periodic behavior and repeats itself 6 times per fundamental period. Like this, the pulses with the widest length occur at the point where one phase duty cycle is at its extremum, whereas the other phases have the same magnitude, which is a half of the extremum phase with negative sign. The phase with maximum duty cycle has the most prominent contribution to the pulse width of the CMV during the whole interval until the next extremum point. At this time the current integration has the longest effective area reaching the highest positive value at the positive pulse and the highest negative value at the negative pulse. In Fig. 3, these regions are highlighted with dotted lines with the line color representing the contributing phase. On the other hand, when one of the phases is close to zero point, the amplitudes of the other phases cancel out, leaving almost insignificant CMV pulse, which is not enough for the circulating current to integrate.

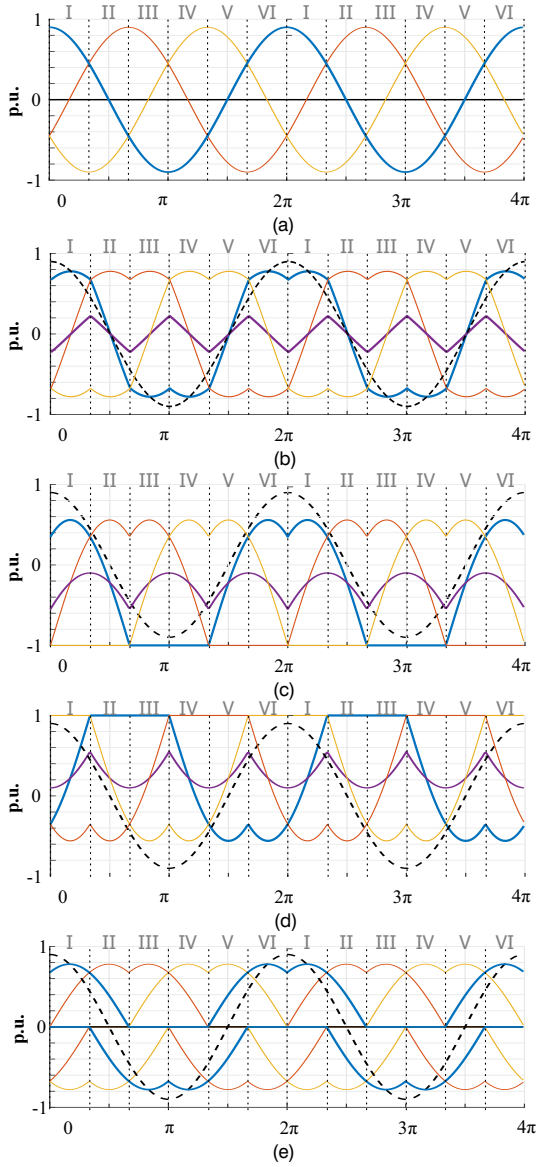

Fig. 5. Modulation methods of the NPC VSI. Red line, blue line and green line are duty cycles of phases A, B and C, respectively; dashed black line is sine-wave duty cycle, navy line is zero-sequence offset: (a) SPWM, (b) SVPWM, (c) DPWMMIN, (d) DPWMMAX and (e) DRPWM.

B. DRPWM

For three-level VSIs, there are two possible carrier arrangements of the PWM, depicted in Fig. 4, namely PD and APOD. The former uses two triangle carrier-waves with the same initial phase-shift, whereas the latter employs an initial phase-shift of 180^o between the upper carrier-wave and the lower carrier-wave. Real applications with single NPC-VSI usually employs the PD as it provides better waveform and spectrum quality performance [20], [22]. Alternatively, the APOD grants lower CMV and HF-ZSCC in paralleled-NPC VSIs without affecting the current quality [10], [18]. Hence, in this study only APOD is considered.

Figures 5(a)–(b) show most commonly used SPWM and SVPWM reference voltages of the NPC VSIs. The proposed DRPWM method is implemented using two reference signals

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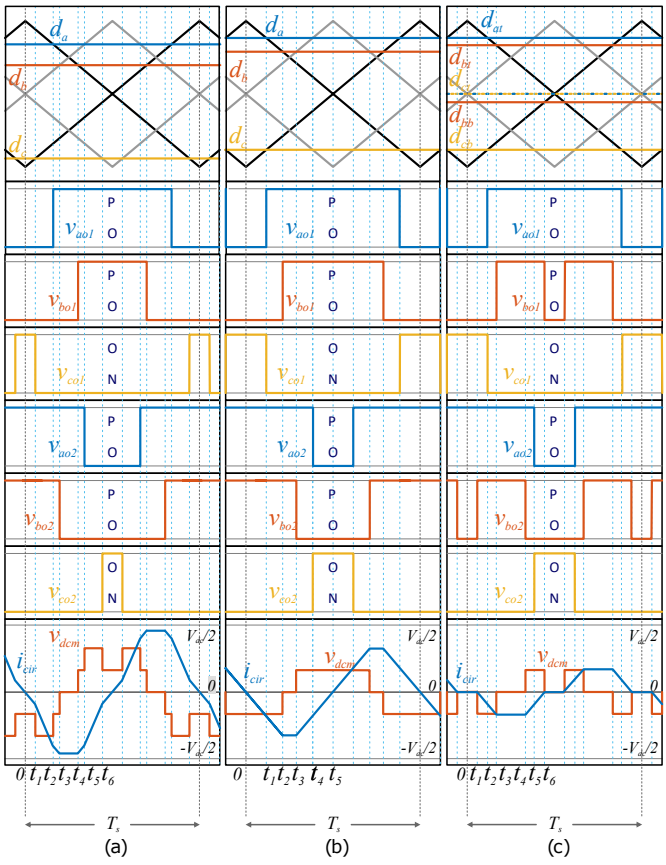

Fig. 6. Detailed switching sequence of parallel NPC VSIs in Sector I with MI = 0.9 : (a) SPWM, (b) SVPWM and (c) DRPWM.

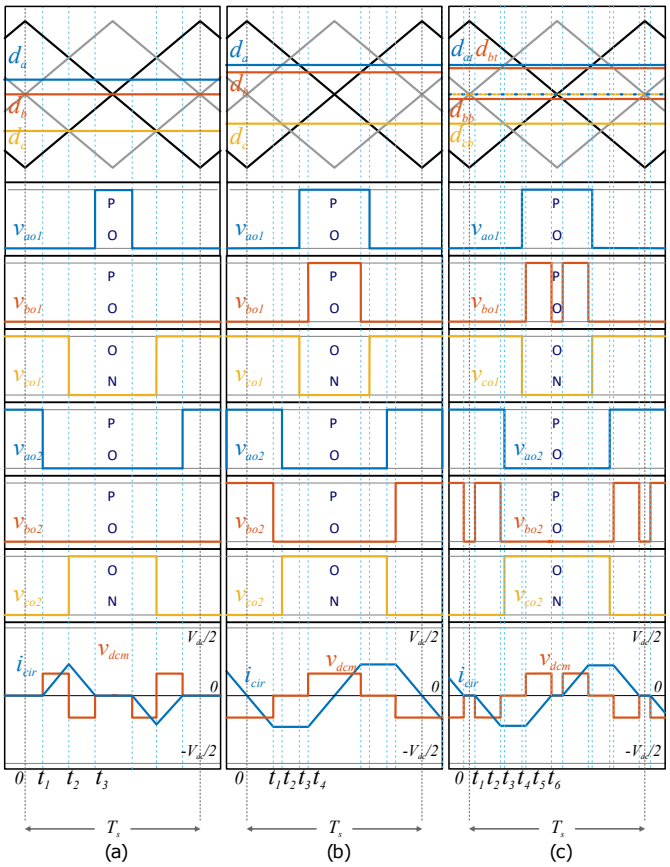

Fig. 7. Detailed switching sequence of parallel NPC VSIs in Sector I with MI = 0.5 : (a) SPWM, (b) SVPWM and (c) DRPWM.

derived independently for comparison with both the upper and the lower PWM carriers of the 3-level VSI. Two reference signals, shown in Fig. 5(d) are generated for top and bottom parts of each arm of the NPC with an overlap at the zero-crossing point. The reference signals are obtained with the maximum $(v_{\max})$ and minimum $(v_{\min})$ phase voltages. The DPWMMIN, shown in Fig. 5(b) is used as the bottom reference, whereas the top reference is calculated based on the DPWMMAX method, given in Fig. 5(c) [23]. Because the reference signals are applied only to the half of the NPC VSI, each signal should be divided by 2:

$$v_{xt}^{*} = \frac{1}{2} \cdot (v_x - v_{\min}) \tag{5}$$

$$v_{xb}^{*} = \frac{1}{2} \cdot (v_x - v_{\max}) \tag{6}$$

where xt - top reference and xb - bottom reference voltages.

The next section provides comparison between three modulation methods (SPWM, SVPWM and DRPWM) in terms of the CMV and the HF-ZSCC.

III. Analysis of the Considered PWM Methods

A. Time domain analysis of the DCMV and the HF-ZSCC

For the analysis, assume sector I of Fig. 5, where the duty cycles A and C are the maximum and the minimum, respectively. As the pattern is repeating itself throughout the sectors I-VI, the analytic results are identical for all sectors.

The detailed view of SPWM, SVPWM and DRPWM with the modulation index (MI) - 0.9 is shown in Fig. 6. The sampling interval considered in the analysis is the worst-case scenario, when one phase duty cycle is at its maximum point, while the other phases are close to each other. At this point the amplitude of the HF-ZSCC is at its extremum.

To simplify the analysis, the duty cycles are assumed to be constants during a single switching period. From Fig. 6(a) the DCMV of SPWM throughout a single sampling interval is

$$v_{\text{dcm}}^{\text{spwm}}(t) = \begin{cases} -\frac{V_{\text{dc}}}{6} & 0 < t < t_1 \\ -\frac{V_{\text{dc}}}{3} & t_1 < t < t_2 \\ -\frac{V_{\text{dc}}}{6} & t_2 < t < t_3 \\ 0 & t_3 < t < t_4 \\ \frac{V_{\text{dc}}}{6} & t_4 < t < t_5 \\ \frac{V_{\text{dc}}}{3} & t_5 < t < t_6 \end{cases} \tag{7}$$

where V_{dc} is the input DC voltage of the parallel VSI, t_1 to t_6 are time segments of the switching sequence.

The HF-ZSCC is estimated using (3). For SPWM the HF-ZSCC is

$$i_{\text{cir}}^{\text{spwm}}(t) = \begin{cases} -\frac{V_{\text{dc}}}{12L} \cdot (t) & 0 < t < t_1 \\ -\frac{V_{\text{dc}}}{12L} \cdot (2t - t_1) & t_1 < t < t_2 \\ -\frac{V_{\text{dc}}}{12L} \cdot (t + t_2 - t_1) & t_2 < t < t_3 \\ -\frac{V_{\text{dc}}}{12L} \cdot (t_3 + t_2 - t_1) & t_3 < t < t_4 \\ \frac{V_{\text{dc}}}{12L} \cdot (t - t_{12} - t_{34}) & t_4 < t < t_5 \\ \frac{V_{\text{dc}}}{12L} \cdot (2t - t_5 - t_{12} - t_{34}) & t_5 < t < t_6 \end{cases} \tag{8}$$

where t_{12} is $t_1 - t_2$ and $t_{34} = t_4 + t_3$. For SPWM, the amplitude of the DCMV $V_{\text{dc}}/3$ significantly increases the slope of the HF-ZSCC. Then, the DCMV is decreased with a step of $V_{\text{dc}}/6$ until it reaches 0 V. At this point the HF-ZSCC is at its maximum value.

According to Fig. 6, profile of the DCMV of SVPWM is lower than that of SPWM. The instant value of the DCMV is

$$v_{\text{dcm}}^{\text{svpwm}}(t) = \begin{cases} -\frac{V_{\text{dc}}}{6} & 0 < t < t_1 \\ -\frac{V_{\text{dc}}}{6} & t_1 < t < t_2 \\ 0 & t_2 < t < t_3 \\ \frac{V_{\text{dc}}}{6} & t_3 < t < t_4 \\ \frac{V_{\text{dc}}}{6} & t_4 < t < t_5 \end{cases} \tag{9}$$

The HF-ZSCC is evaluated in the same manner as that of SPWM:

$$i_{\text{cir}}^{\text{svpwm}}(t) = \begin{cases} -\frac{V_{\text{dc}}}{12L} \cdot (t - t_1) & t_0 < t < t_1 \\ -\frac{V_{\text{dc}}}{12L} \cdot (2t + t_2 - t_1) & t_1 < t < t_2 \\ -\frac{V_{\text{dc}}}{12L} \cdot (t - t_{13}) & t_2 < t < t_3 \\ -\frac{V_{\text{dc}}}{12L} \cdot (t_4 - t_{13}) & t_3 < t < t_4 \\ \frac{V_{\text{dc}}}{12L} \cdot (t - t_{45} + t_{13}) & t_4 < t < t_5 \end{cases} \tag{10}$$

where t_{13} and t_{45} are $3t_3 - t_2 + t_1$ and $\sum_{n=4}^{5} t_n$ respectively.

The DCMV of SVPWM is limited by $V_{\text{dc}}/6$ as the $V_{\text{dc}}/3$ peaks are diminished, resulting in decreased HF-ZSCC compared to that of SPWM. However, when DCMV is zero, the instant value of the HF-ZSCC is still at its maximum point.

Lastly, the DCMV of DRPWM is

$$v_{\text{dcm}}^{\text{drpwm}}(t) = \begin{cases} 0 & 0 < t < t_1 \\ -\frac{V_{\text{dc}}}{6} & t_1 < t < t_3 \\ 0 & t_3 < t < t_4 \\ \frac{V_{\text{dc}}}{6} & t_4 < t < t_6 \end{cases} \tag{11}$$

And for DRPWM the HF-ZSCC is evaluated as

$$i_{\text{cir}}^{\text{drpwm}}(t) = \begin{cases} 0 & t_1 < t < t_1 \\ -\frac{V_{\text{dc}}}{12L} \cdot (t - t_2) & t_2 < t < t_2 \\ -\frac{V_{\text{dc}}}{12L} \cdot (t - t_2) & t_3 < t < t_3 \\ -\frac{V_{\text{dc}}}{12L} \cdot (t_5 - t_2) & t_4 < t < t_4 \\ \frac{V_{\text{dc}}}{12L} \cdot (t - 2t_5 + t_2) & t_5 < t < t_6 \end{cases} \tag{12}$$

As is evident from Fig. 6 and (7)-(12) the DCMV of DRPWM is considerably lower compared to that of SPWM and SVPWM and limited by the maximum voltage $V_{\text{dc}}/6$. Moreover, for DRPWM, the zero-voltage regions of the DCMV are repeated 4 times per single sampling period, resulting in zero HF-ZSCC at each of these intervals, as shown in Fig. 6(c).

From the Fig. 6(c), the magnitudes of the maximum upper reference and the lower minimum reference are equal. The upper reference signal of the phase A in sector I is

$$v_{at}^{*} = \frac{1}{2} \cdot M \cdot [\sin(\omega t + \phi) - v_{\text{min}}] \tag{13}$$

$$v_{at}^{*} = \frac{1}{2} \cdot M \cdot \left[\sin(\omega t + \phi) - M \cdot \sin\left(\omega t + \frac{2}{3}\pi + \phi\right)\right] \tag{14}$$

where M is the MI, ω is the fundamental frequency, ϕ is the phase angle at the sector I which is $\frac{\pi}{6} < \phi < \frac{\pi}{2}$

Then the lower reference signal of the phase C is

$$v_{\text{cb}}^{*} = \frac{1}{2} \cdot M \cdot \left[\sin\left(\omega t + \frac{2}{3}\pi + \phi\right) - v_{\text{max}}\right] \tag{15}$$

$$v_{\text{cb}}^{*} = \frac{1}{2} \cdot M \cdot \left[\sin\left(\omega t + \frac{2}{3}\pi + \phi\right) - \sin\left(\omega t + \phi\right)\right] \tag{16}$$

Comparing (14) and (16) it is obvious that for the sector I phases A and C are related as

$$v_{at}^{*} = -v_{cb}^{*} \tag{17}$$

The PWM pulses related to the v_{max} and the v_{min} phases are always complementary, therefore, the resulting CMV is determined by the switching state of the third phase. For the P - state, $v_{\text{cm}} = v_{\text{dc}}/6$, for the N - state, $v_{\text{cm}} = -v_{\text{dc}}/6$, and for the O - state, $v_{\text{cm}} = 0$, which leads to reduced CMV over the whole switching period compared to that of SPWM.

Furthermore, phase B has two non-zero reference signals which are compared to the triangular carrier wave.

$$v_{bt}^{*} = \frac{1}{2} \cdot M \cdot \left[\sin\left(\omega t - \frac{2}{3}\pi + \phi\right) - \sin\left(\omega t + \frac{2}{3}\pi + \phi\right)\right] \tag{18}$$

$$v_{bb}^{*} = \frac{1}{2} \cdot M \cdot \left[\sin\left(\omega t - \frac{2}{3}\pi + \phi\right) - \sin\left(\omega t + \phi\right)\right] \tag{19}$$

Solving the equations via trigonometrical identities

$$v_{bt}^{*} = -\frac{\sqrt{3}}{2} \cdot M \cdot \cos(\omega t + \phi) \tag{20}$$

$$v_{bb}^{*} = -\frac{\sqrt{3}}{2} \cdot M \cdot \cos\left(\omega t - \frac{\pi}{3} + \phi\right) \tag{21}$$

Like this, an additional pulse is added to the phase B twice per sampling period at the times t_1 and t_6, forcing the O-state, which leads to $v_{\text{dcm}} = 0$.

On the other hand, as the MI decreases, the maximum pulse width becomes shorter, which affects the DCMV of the VSI and therefore influence the performance of the modulation. Fig. 7 shows the switching diagram of the three considered modulation methods with MI - 0.5. As can be seen from the Fig. 7, at low MI, the HF-ZSCC under SPWM tends to be lower than that of SVPWM and DRPWM. It happens due to the lower width of the positive and the negative instances of the DCMV. Furthermore, the amplitude of the DCMV for all three methods is $V_{\text{dc}}/6$. This way, the HF-ZSCC cannot be incremented fast enough to reach higher values. As for SVPWM and DRPWM, each instance of the DCMV is longer than that of SPWM. Thus, the HF-ZSCC keeps incrementing and reaches higher values compared to the HF-ZSCC in the case of SPWM. Moreover, when using DRPWM, the DCMV has a short interval, where the voltage becomes 0. It can be seen at the time points t_1-t_2 and t_6. At this moment, the HF-ZSCC stops increasing and holds its value. As a result, the performance of DRPWM is slightly better than that of the SVPWM at low values of the MI.

B. HF-ZSCC and Single-Phase RMS Current Analysis

To derive the HF-ZSCC Peak-to-peak (P2P) analytically, (7), (9) and (11) need to be solved with the consideration of

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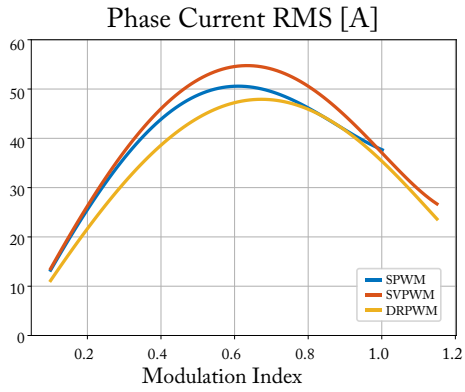

Fig. 8. Estimated RMS of single phase current of the interleaved NPC-VSI.

the MI and the sampling time T_s. Then, the time instances t_1–t_6 can be determined as per

$$M > 0.5 \begin{cases} t_1 = T_s(1-|d_{\text{max}}|)/2 \\ t_2 = T_s(|d_{\text{min}}|)/2 \\ t_3 = T_s(|d_{\text{mid}}|)/2 \\ t_4 = T_s(1-|d_{\text{min}}|)/2 \\ t_5 = T_s(1-|d_{\text{mid}}|)/2 \\ t_6 = T_s(|d_{\text{max}}|)/2 \end{cases} \tag{22}$$

$$M < 0.5 \begin{cases} t_1 = T_s(|d_{\text{mid}}|)/2 \\ t_2 = T_s(|d_{\text{min}}|)/2 \\ t_3 = T_s(|d_{\text{max}}|)/2 \\ t_4 = T_s(1-|d_{\text{max}}|)/2 \\ t_5 = T_s(1-|d_{\text{min}}|)/2 \\ t_6 = T_s(1-|d_{\text{mid}}|)/2 \end{cases} \tag{23}$$

where d_{max},d_{mid} and d_{min} are the maximum, middle and minimum modulation indexes of current sampling. Due to periodical behavior of three-phase systems, the pattern will be repeating every 6 times per fundamental period.

Substituting (22) and (23) into (7), (9) and (11) yields

$$M > 0.5 \begin{cases} i_{\text{p2p}}^{\text{spwm}} = \frac{V_{\text{dc}}T_s}{12L}(2|d_{\text{max}}|-1) \\ i_{\text{p2p}}^{\text{svpwm}} = \frac{V_{\text{dc}}T_s}{12L}(|d_{\text{min}}|) \\ i_{\text{p2p}}^{\text{drpwm}} = \frac{V_{\text{dc}}T_s}{12L}(|d_{\text{mid}}|) \end{cases} \tag{24}$$

for higher value of the MI and

$$M < 0.5 \begin{cases} i_{\text{p2p}}^{\text{spwm}} = \frac{V_{\text{dc}}T_s}{12L}(|d_{\text{mid}}|) \\ i_{\text{p2p}}^{\text{svpwm}} = \frac{V_{\text{dc}}T_s}{12L}(|d_{\text{min}}|-|d_{\text{mid}}|) \\ i_{\text{p2p}}^{\text{drpwm}} = \frac{V_{\text{dc}}T_s}{12L}(|d_{\text{min}}|-|d_{\text{mid}}|) \end{cases} \tag{25}$$

The rms value of a single phase per VSI can be expressed in terms of harmonic content of the DCMV [24]. The output voltage of a single VSI is

$$V_{\text{o}} = MV_{\text{dc}}\cos(\omega_o t) + \frac{V_{\text{dc}}}{\pi} \sum_m^\infty \sum_n^\infty \left[\frac{1}{m}J_n(m\pi M)\sin(n\tfrac{\pi}{2})\cos(m(\omega_c t+\phi_c)+n\omega_o t)\right] \tag{28}$$

where ω_o is fundamental frequency, ω_c is pwm frequency, M is the MI, J_n is a Bessel function of the first kind [24], ϕ_c is the pwm offset and m and n are the harmonic indies of the pwm and fundamental frequencies, respectively.

Applying (28) into (1) the DCMV of a single phase is derived. It is worth mentioning that the DC-offset and fundamental content is canceled out leaving only the side-band harmonics with different interleaved carrier components. After some manipulation with trigonometric identities the phase current harmonic components are expressed as

$$I^{\text{spwm}} = \frac{V_{\text{dc}}}{\pi} \cdot \sum_m^N \sum_n^N \frac{1}{m} J_n(m\pi M)\sin(n\frac{\pi}{2}) \tag{29}$$

Then the estimation of the RMS can be further simplified by fact that the side-bands harmonics of the first carrier component group $m = 1$ in (29) are the most prominent. Therefore, the RMS is

$$I_{\text{rms}}^{\text{spwm}} = \frac{V_{\text{dc}}}{\pi} \cdot \sqrt{\frac{\sum_n^N (J_n(\pi M)\sin(n\frac{\pi}{2}))^2}{N}} \tag{30}$$

From (30) it is clear that the rms for different values of the MI is determined by the Bessel function $J_n(m\pi M)$ only, which has periodically descending behavior with the peaks around $M = 0.5$.

The harmonic contents of the SVPWM and the DRPWM are derived using the same principle and after manipulations (26) and (27) are derived.

The equations (26) and (27) are more complex than (30) due to injection of harmonic triplets to the signal reference. However, based on the equations, the behavior of the rms under the considered modulations is similar due to the influence of the Bessel function characteristics. The estimated values of the RMS for $V_{dc} = 600V$ and $(-5 < n < 5)$ are shown in Fig. 8.

$$I_{\text{rms}}^{\text{svpwm}} = \frac{2V_{\text{dc}}}{\pi^2\sqrt{N}} \left[\sum_n^N \left[\begin{array}{c} \frac{\pi}{6}\sin([m+n]\frac{\pi}{2})[J_n(m\frac{3\pi}{4}M)+2\cos(n\frac{\pi}{6})J_n(m\frac{\sqrt{3}\pi}{4}M)] \\ +\frac{1}{n}\sin(m\frac{\pi}{2})\cos(n\frac{\pi}{2})\sin(n\frac{\pi}{6})\left(J_0(m\frac{3\pi}{4}M)-J_0(m\frac{\sqrt{3}\pi}{4}M)\right) \\ +\sum_k \frac{1}{n\pm k}\sin([m\pm k]\frac{\pi}{2})\cos([n\pm k])\frac{\pi}{2}\sin([n\pm k]\frac{\pi}{6}) \\ \left(J_k(m\frac{3\pi}{4}M)+2\cos([2n\pm 3k]\frac{\pi}{6})J_k(m\frac{\sqrt{3}\pi}{4}M)\right) \end{array}\right]^2\right]^{\frac{1}{2}} \tag{26}$$

$$I_{\text{rms}}^{\text{drpwm}} = \frac{2V_{\text{dc}}}{\pi^2\sqrt{N}} \left[\sum_n^N \left[\begin{array}{c} \frac{\pi}{3}\sin(n\frac{\pi}{2})\cos(n\frac{\pi}{6})J_n(m\frac{\sqrt{3}\pi}{2}M) \\ +\sum_k \frac{1}{n\pm k}\sin([n\pm k]\frac{\pi}{3})\cos([n\pm k]\frac{\pi}{6})\sin(k\frac{\pi}{2})J_k(m\frac{\sqrt{3}\pi}{2}M) \end{array}\right]^2\right]^{\frac{1}{2}} \tag{27}$$

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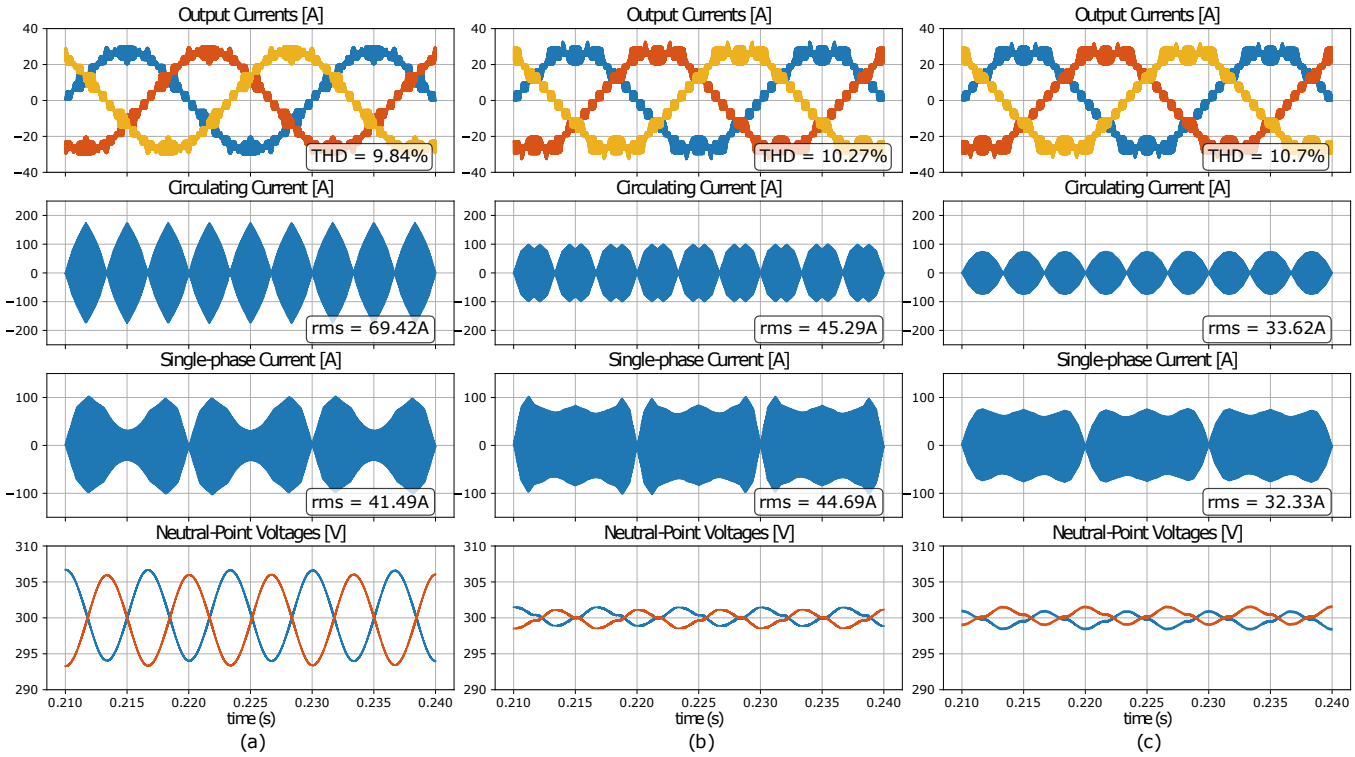

Fig. 9. Simulation results. Total load current, phase A current of a single inverter, HF-ZSCC and neutral-point voltage: (a) SPWM, (b) SVPWM and (c) DRPWM.

IV. Simulation and Experimental Results

The performance of the proposed method is validated through extensive simulation and experiments. The evaluation of the results is provided in this section. The parameters of the system are given in Table I.

A. Simulation Results

The simulation of 4-parallel-connected NPC VSIs with common dc-link source is implemented in Simulink MATLAB environment with PLECS toolbox. SPWM, SVPWM and DRPWM are all applied to the system under the interleaved operation.

The simulation results for MI 0.9 are given in Fig. 9. The total harmonic distortion (THD) is slightly affected when using SVPWM, however, the proposed method increases the THD from 9.84% to 10.7%. Fig. 10(a) provides the comparison of the THD for the three methods in a MI ranging from 0.1 to 1.15. The THD trend for the whole range of the MI is similar and common for most PWM techniques [25]–[30]. It is calculated from harmonic values of the current spectra as

$$\text{THD} = \sqrt{\sum_{n=2}^{N} \frac{(I_n/n)^2}{I_1}} \tag{31}$$

According to (3), when using a small filter inductance, the amplitude of the HF-ZSCC can reach significantly large values, even higher than the value of the output current. Hence, the P2P of the HF-ZSCC under SPWM has the highest value of 380 A compared to those of SVPWM (200 A)and DRPWM (160 A) methods. The amplitude of DRPWM HF-ZSCC is considerably lower among all the methods, and three times smaller than that of SPWM. Fig. 10(b) shows the P2P of the HF-ZSCC for different values of the MI. As can be seen from the figure, the P2P of DRPWM is considerably lower than that of SPWM and SVPWM in the MI range from 1.15 to 0.6. For low values of the MI the HF-ZSCC P2P of DRPWM is identical to that of SVPWM, but higher than the P2P of SPWM.

Although the quality of the load current is relatively high due to the interleaving, the phase currents of each inverter, given in Fig. 9 are still highly distorted. The amplitude and

TABLE I
System Parameters

Symbol	Description	Value
f_{sw}	Switching frequency	15 kHz
f_{o}	Fundamental frequency	50 Hz
V_{dc}	DC-link voltage	*600 V*
L	Filter inductance	25 µH
R	Load resistance	10 Ω
C_{dc}	DC-link capacitance	1 mF
M	MI	0.9

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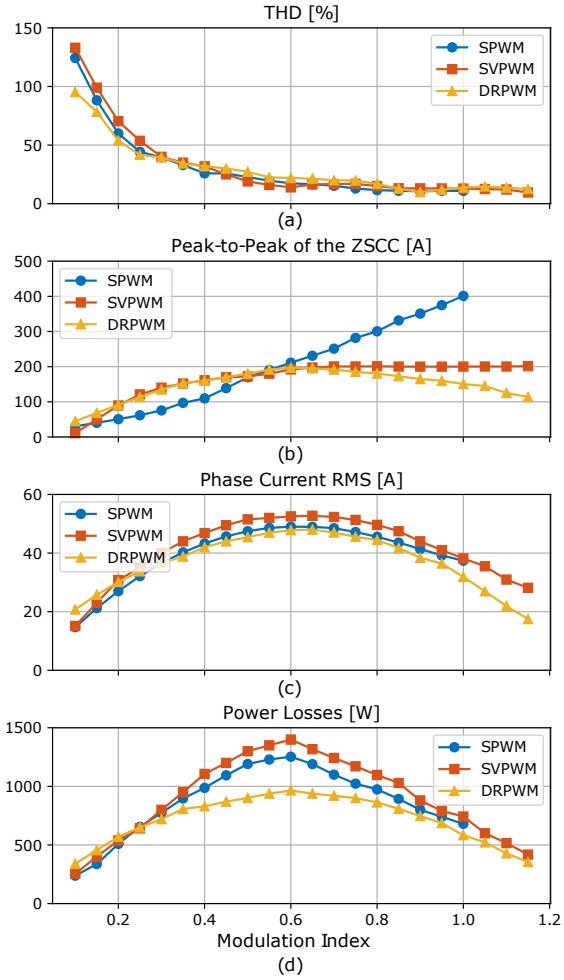

Fig. 10. Performance comparison of SPWM SVPWM, and DRPWM depending on the MI and Inductance: (a) THD of the output current (b) P2P value of the HF-ZSCC, (c) RMS value of the HF-ZSCC and (d) Power Losses of the inverter.

the profile of the current is decreased under DRPWM method compared to those of SPWM and SVPWM. The rms is the lowest under the proposed DRPWM method and equals 32.33A, whereas the rms of SPWM and SVPWM are 41.49A and 44.69A, respectively. Fig. 10(c) shows the rms of A-phase currents, influenced by the HF-ZSCC for different MIs. The simulated values are very similar to those, derived by equations (26), (27) and (30) and shown in Fig. 8. The rms of DRPWM is the lowest for the most of the MI range, followed by rms of SPWM. SVPWM has the highest value of the rms throughout the whole range.

B. Losses Analysis

To further investigate the epiphany of the proposed method, the power losses of a single inverter were evaluated throughout multiple simulations using parameters of an IGBT module FF600R12ME4 from Infineon [31]. Fig. 11 shows the comparison of the power losses between SPWM, SVPWM and DRPWM for $M = 0.9$.

The switching losses of the IGBT are evaluated using

$$P_{\text{sw}} = 2 \cdot (E_{\text{ton}} + E_{\text{toff}}) \cdot f_{\text{sw}} \tag{32}$$

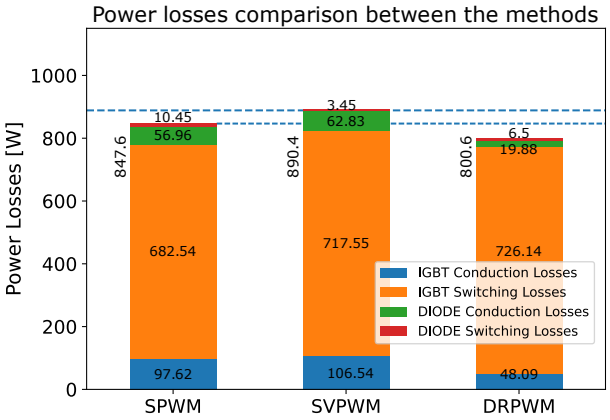

Fig. 11. Comparison of the Power Losses between SPWM, SVPWM and DRPWM for the MI = 0.9.

where E_{ton} and E_{toff} are respectively the turn-on and the turn-off energies per pulse:

$$\begin{aligned} E_{\text{ton}} &= (V_{\text{CE}} \cdot I_{\text{d}}/2) \cdot (t_{\text{on}} + t_{\text{don}}) \\ E_{\text{toff}} &= (V_{\text{CE}}/2 \cdot I_{\text{d}}) \cdot (t_{\text{off}} + t_{\text{dof}}) \end{aligned} \tag{33}$$

where V_{CE} is collector-emitter voltage applied to the IGBT, I_{d} is the load current and t_{on}, t_{don}, t_{off} and t_{dof} are on/off times with the corresponding on/off delays.

The conduction losses of the IGBT are calculated as

$$P_{cd} = R_{\text{on}} \cdot I_{\text{d}}^2. \tag{34}$$

In this equation R_{on} is On Resistance of the IGBT.

From (32)-(34), it can be noticed that the current I_{d} floating through the IGBT influences the power losses. From Figs. 9, 10, the phase current rms is the lowest in the case of the proposed method, whereas SVPWM has the highest value. Therefore the total power losses are significantly decreased under the proposed method. On the other hand, Figures 6-7 demonstrate that the proposed method adds more switching states to the sequence and therefore increases the switching losses. From Fig. 11, the switching losses of the DPRWM are higher compared to the switching losses of SPWM and SVPWM, however owing to significantly decreased current, the reduced conduction losses yield the total power losses reduction.

C. Experimental Results

The experimental results have been obtained from a Prototype of the MV grid impedance measurement system shown in Fig. 12(a). For the experiment 4 NPC-VSIs (Fig. 12(b)) have been connected in parallel to a resistor load with the parameters given in Table I. Fig. 13 provides the experimental waveforms of the considered methods. The time scale for all the waveforms is 2 ms/div.

The THD of the current is not changed significantly for SPWM and SVPWM methods, however, as shown in Fig. 13, DRPWM method affects the THD by approximately by 2.5%, which is acceptable in well-designed systems or can be improved by either connecting more inverters in parallel.

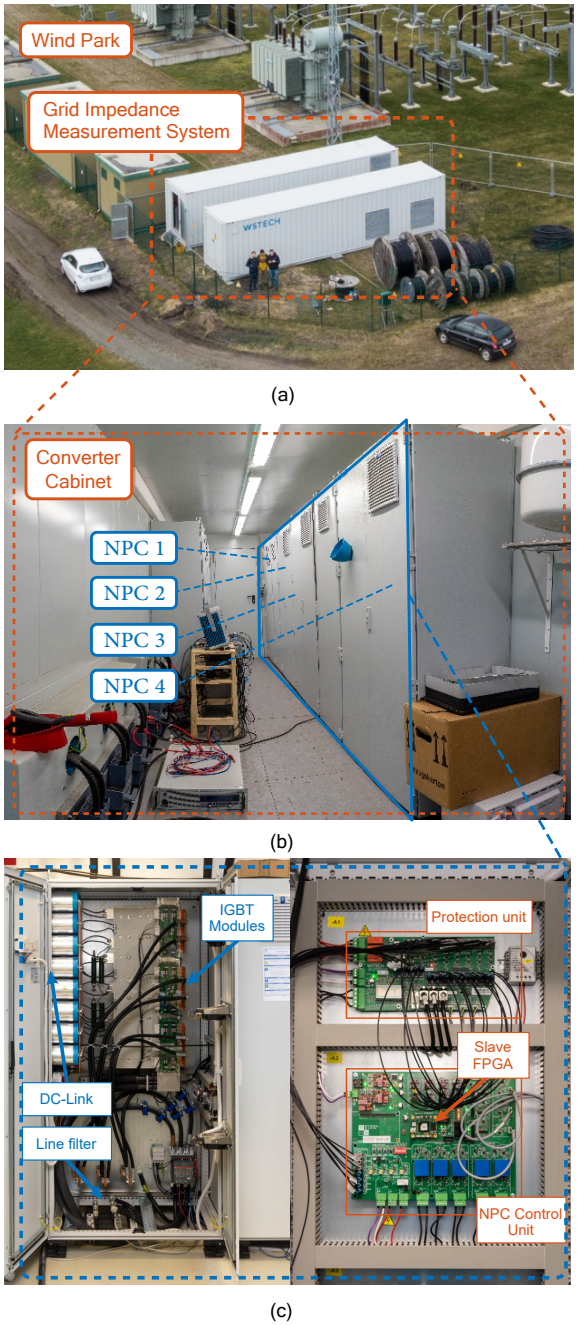

Fig. 12. Experimental setup: (a) MV grid impedance measurement system located in a wind-park, (b) Inside view of the system with 4 NPC VSI connected in parallel and (c) Power modules and control unit of a single NPC VSI.

It can be seen that the HF-ZSCC from the experimental results closely match the HF-ZSCC from the simulations. The HF-ZSCC P2P of SPWM is close to 400 A and is reduced to 200 A when SVPWM is implemented. However, the lowest value of the HF-ZSCC P2P is obtained under the operation with DRPWM and it is curtailed down to 100 A P2P.

The phase currents of a single VSI are shown in a scale of 100 A/div. As was stated before, they are influenced by the circulating current and result in increased power losses of each inverter. It can be noticed, that DRPWM gives the best results and the amplitude of the currents is significantly reduced.

The neutral-point voltages are compared for SPWM, SVPWM and DRPWM. As shown, the proposed method provides the same results for the balancing of the neutral-point voltages as those of the SVPWM. The performance can be further improved by applying known voltage balancing algorithms.

At last, the CMV of a single VSI for different modulation methods is shown in the last row of Fig. 13. The conventional SPWM has increased number of the CMV transitions switching between positive and negative DC-link voltages, whereas the profile of the SVPWM and proposed DRPWM is dependent on the direction of the AC current and the CMV transition switch between the positive (negative) DC-link voltage and neutral point.

V. Conclusion

This paper investigated the performance of the Double-Reference Pulse-Width Modulation (DRPWM) in interleaved operation of parallel-connected Neutral-Point Clamped Voltage Source Inverters (NPC VSI) in terms of the High-frequency Zero-Sequence Circulating Current (HF-ZSCC) reduction. DRPWM was compared to the most commonly used Sine Pulse-Width Modulation (SPWM) and Space-Vector Pulse-Width Modulation (SVPWM).

According to the analysis section, DRPWM significantly reduces the HF-ZSCC in the range of Modulation Indexes (MI) $0.6 - 1.15$. Furthermore, the power losses of the VSI can be significantly reduced compared to the losses in the case of SPWM and SVPWM methods. Moreover, the proposed method provides good initial balancing of the neutral-voltage balancing, however an additional balancing algorithm can be added for better performance.

The simulation and experimental results demonstrated that in systems using small filter inductance the HF-ZSCC reaches much higher values than the output current and therefore affects phase currents of each individual VSI, thereby sufficiently increasing the power losses of inverters. It has been confirmed that DRPWM remarkably reduces the HF-ZSCC for high values of the MI, however at a cost of deteriorated total harmonic distortion (THD) of the output current by approximately 2.5 % as compared to that of SPWM and SVPWM. Considering the reduction of HF-ZSCC and power losses minimization, the proposed method can be used as a trade-off. Furthermore, due to increased number of switching states, the proposed method is more effective in applications, which require interleaved operations of grid-tied VSIs utilizing small filter inductance, such as grid impedance analyzers, STATCOMs or FACTS.

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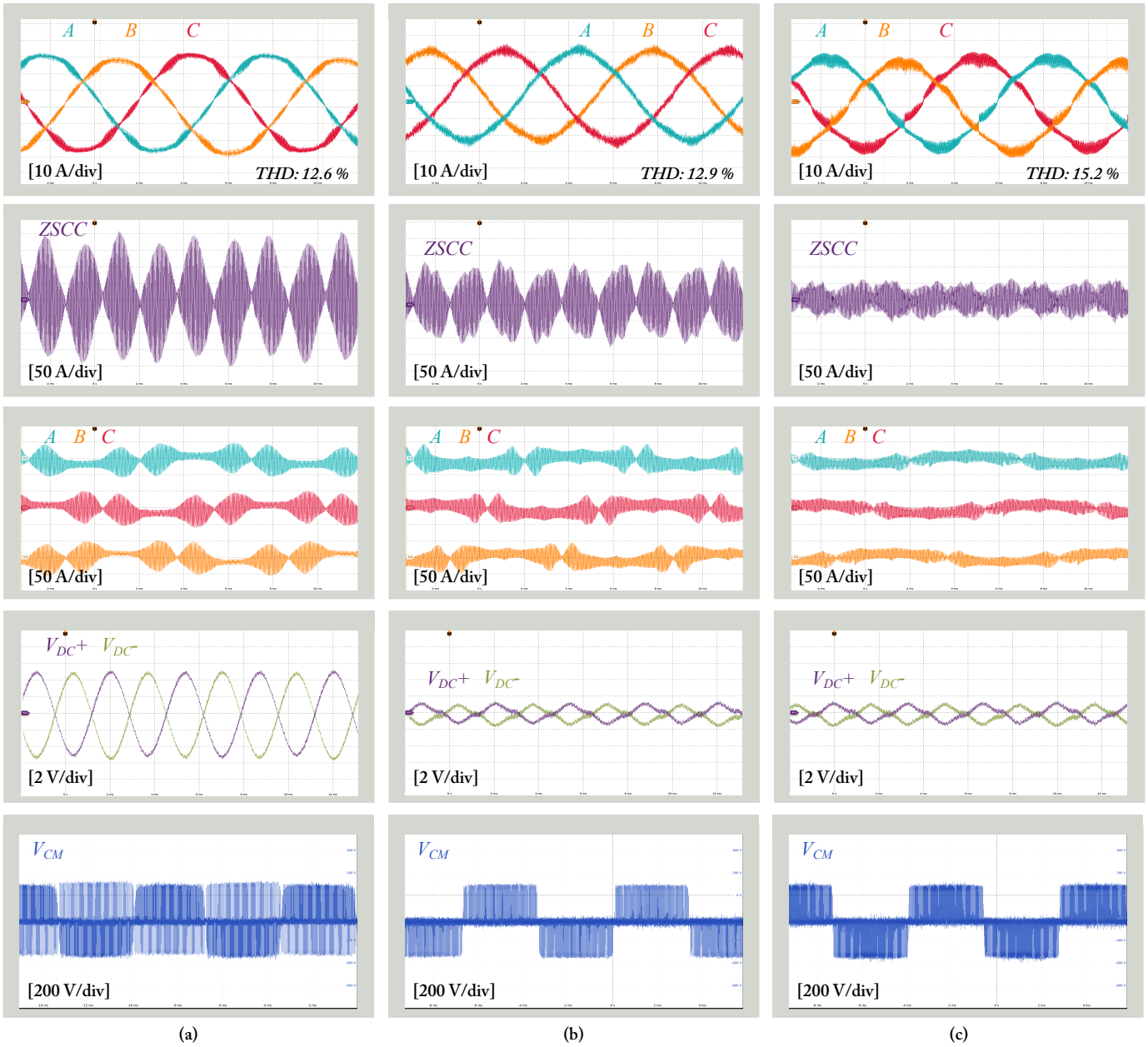

Fig. 13. Experimental results. Total load current, Phase currents A, B, and C of a single inverter, HF-ZSCC, neutral-point voltage and CMV: (a) SPWM, (b) SVPWM and (c) DRPWM.

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