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# Solid State Transformer with Integrated Input Stage

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***Abstract*—In this paper, a solid state transformer (SST) with integrated stages is addressed. The SST has been originally proposed for traction applications, after as an option to face the new requirements of the distributed generation but also suggested in many applications. There are different topologies, from one to three stages; certainly each one with their advantages and limitations. Some challenges for this type of systems are reducing the cost and increasing the efficiency.**

**The components reduction is discussed in this paper, by integrating two stages of the SST; the ac/dc converter and the DAB converter share one leg. The proposed scheme is described and numerically simulated.**

***Keywords— Distributed generation, Fewer semiconductors, Stage integration, Solid state transformer.***

## I. INTRODUCTION

Solid state transformer (SST) is suggested in different applications, such as the distributed generation [1]-[7], transportation applications [8]-[10], and renewable energy [11]-[12]. For the distributed generation, the SST has to compete with the traditional transformer in terms of cost and efficiency. But certainly, other characteristics are added, that the traditional one cannot offer.

There are different SST topologies reported in the literature [13]-[20]. Some schemes make a direct ac/ac transformation without any DC-link [13]-[14], the advantages of these schemes are the components count and the efficiency. However they are susceptible to voltage variations and are limited for providing reactive power compensation, but also the incorporation of other sources or storage elements is not simple. Then, these schemes are almost similar to the traditional transformer, but the size is reduced due to the high-frequency operation.

The more popular scheme for SST considers DC-links in the medium voltage (MV) side and low voltage (LV) side [15]-[18]. These schemes have the advantage that they are not susceptible to voltage variations due to the DC-links, and also may incorporate other power sources or storage elements like in [18], and other more advantages. However, the semiconductor count is not the best characteristic and also the efficiency is penalized due to the cascaded stages.

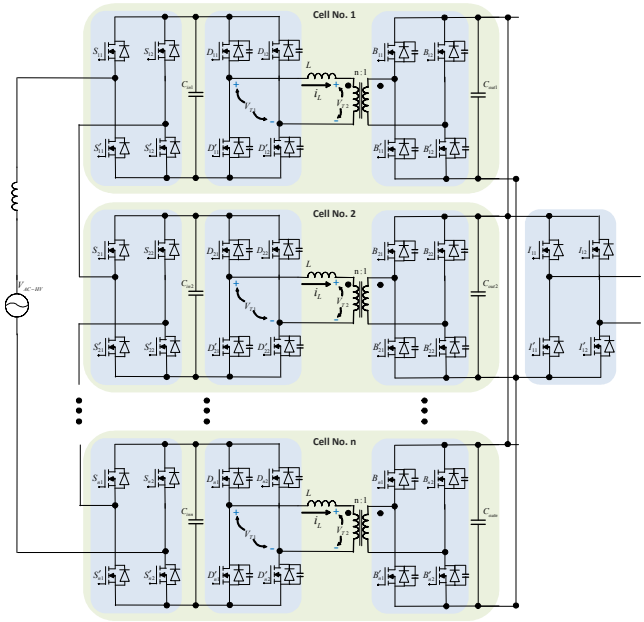


Fig. 1. Solid State Transformer: the typical scheme

In Fig. 1 is shown the typical configuration of the SST with the two DC links; it can be appreciated that n cells are employed. Each cell is composed of an ac/dc rectifier, a double active bridge (DAB) converter, and the dc/ac converter. There are two DC-links, the MV-link, and the LV-link. The DAB converter is mainly the core of the provided isolation.

Many works have been focused on the DAB converter efficiency [19]-[21], some of them are focused on getting the maximum efficiency in the whole range of operation. Other in the controller stage [22]-[24].

In [25] are studied different SST transformer topologies to evaluate the cost and other aspects. The difference between these analyzed topologies is the isolated stage, instead of a DAB converter is employed a multiple active bridge (MAB)

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converter. The isolated stage output is the main difference, the input stage remains intact. The components reduction is the main reason for that the SST with the MAB converter offers the best cost, according to [25].

In this paper is proposed a way to reduce components of the SST, the ac/dc converter and the input bridge of the DAB are integrated into a single stage. Then, a reduction of one power leg is obtained per cell. The operation of the ac/dc and the DAB converter is assured by design, then the same good characteristics of the traditional SST are obtained, but with fewer components. The proposed stage integration is described and numerically simulated to demonstrate the feasibility of the proposal.

The paper is organized as follows; in section II, the proposed SST is addressed, describing each stage. The numerical simulation results, demonstrating the performance, are presented in section III. And finally, some conclusions are given.

## II. Proposed Solid State Transformer

The proposed SST is shown in Fig. 2, as it can be observed it is composed of n cells, similar to the traditional one. The main difference is the cell, where the ac/dc converter and the first bridge of the DAB converter are integrated, they are sharing one power leg (Fig. 3).

The shared leg consists of the switches $S_{11}$ and $S'_{11}$, the other legs assure the operation in each power stage. The working zone of each integrated stage is assured by making some considerations, for that some bounding circuits may be considered to limit the duty cycle (phase shift) and the modulation index. The advantages of the schemes with the no integration are preserved with the proposal.

The ac/dc converter is operated with a sinusoidal pulse width modulation (SPWM), then an ac modulating signal is employed. A unipolar waveform is employed, then an input current with low harmonic distortion is expected, also for the multilevel operation.

The DAB converter is working in a bucking mode, but also a discontinuous conduction mode is considered for the inductor of this power stage; this is made for simplicity, but also because a soft-switching is assured during the whole power range, however other ways are possible.

The operation of the proposed integrated converter is described next, in the following sub-sections. This is addressed for each semi-cycle of the ac modulation signal.

### A. *Positive semi-cycle of ac modulation signal*

In Fig. 4(a) are shown the waveforms for the positive semi-cycle of the ac modulating signal. Only the signals for the upper switches are shown since the others are the opposite. The control signals of the output bridge are omitted since they are not involved in the integration. The ac voltage of the rectifier, the voltages of the inductor of the DAB, and also the primary current are shown.

To assure the operation $\delta_1$ is bounded to $\delta_{1max}$, this angle controls the power transfer of the DAB converter. Additionally, $\delta_s$ is bounded to $\delta_{smax}$, this angle is used for the sinusoidal modulation of the ac/dc stage, which is in direct

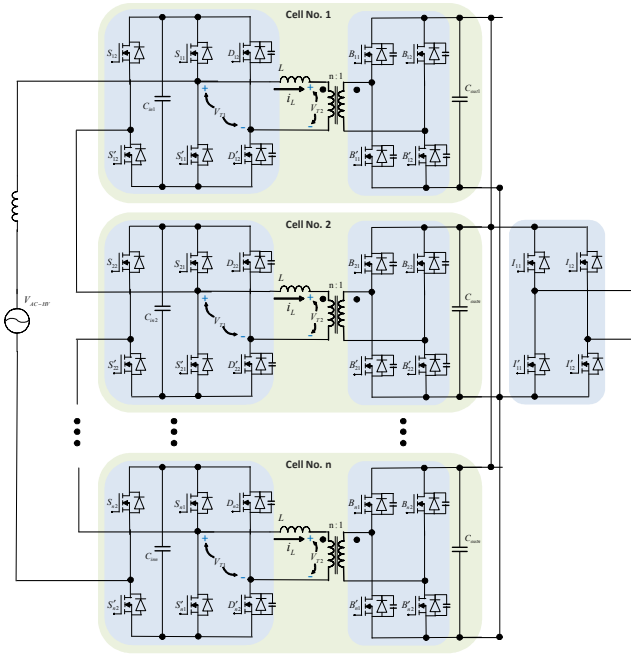


Fig. 2. Proposed integrated SST

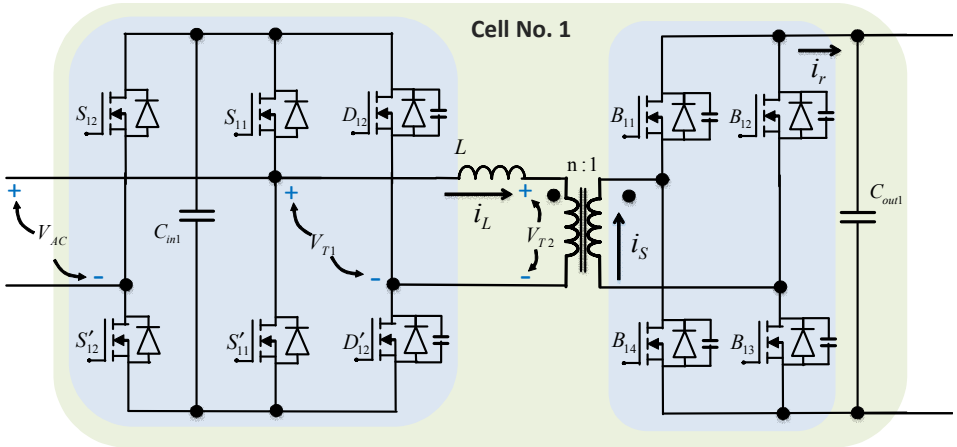


Fig. 3. Cell No. 1 of the proposed SST transformer

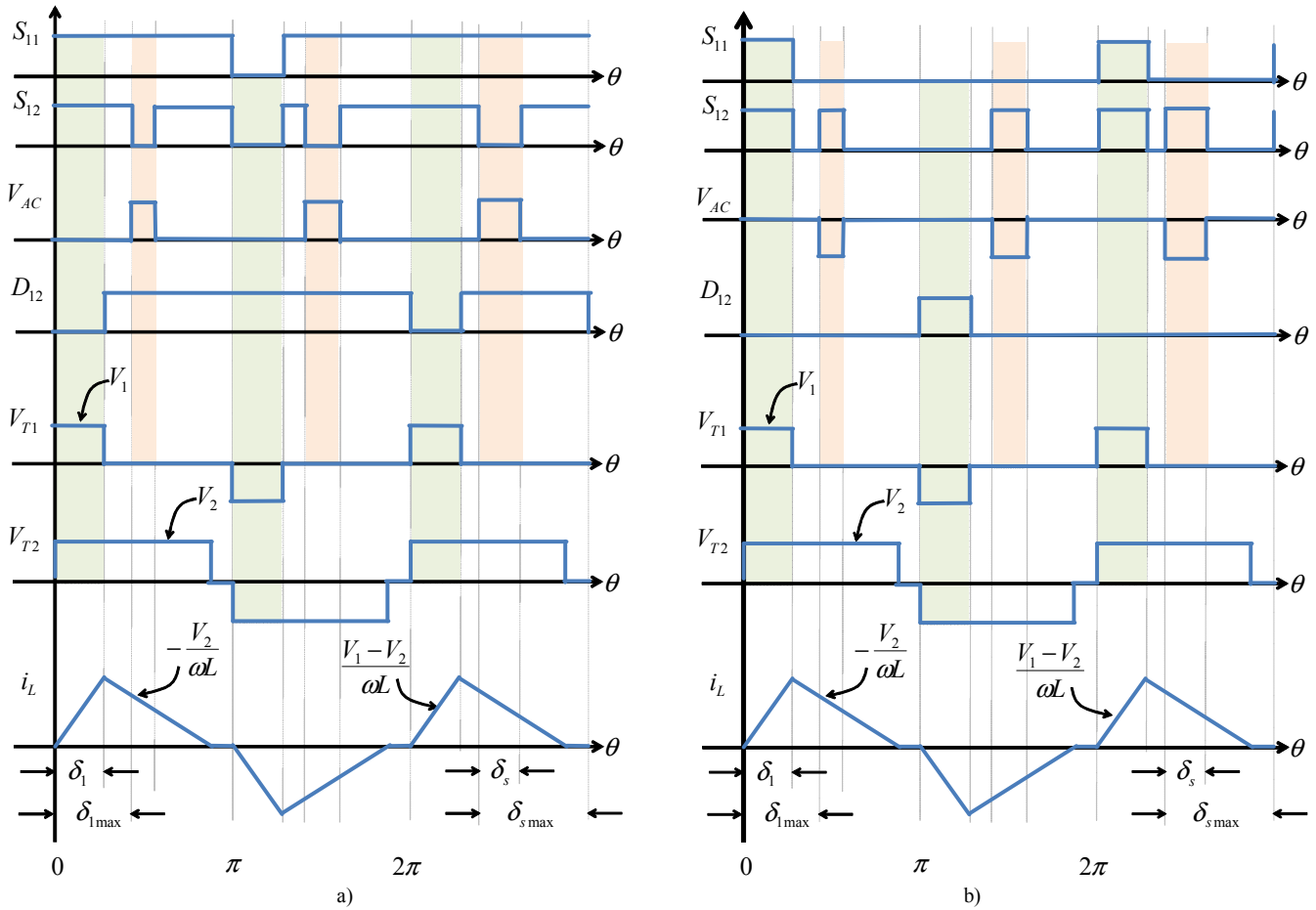


Fig. 4. Waveforms of the proposed converter. a) positive semi-cycle, b) negative semi-cycle.

relationship with the modulation index (Fig. 4). Then, there are no overlapping between the operations in both stages, this is made to assure the proper operation of each stage. The operation is as follows:

i) During $\delta_1$. The output $V_{T1}$ is positive, but also $V_{T2}$. During this time the inductor current will be increased from the zero value. For the $V_{AC}$ an output of zero is produced. Then, to obtain these voltages, the proper signals for the switches $S_{11}$, $S_{12}$, and $D_{12}$ are 1, 1, and 0 respectively.

ii) During $\delta_{1max} - \delta_1$. The output of $V_{T1}$ is now zero, and $V_{T2}$ remains positive. During this time the inductor current will be decreased. Notice that the diodes of the output bridge are conducting, then the switches may be in the off state during this time. For the $V_{AC}$ an output of zero is still produced. Then, to obtain these voltages, the proper signals for the switches $S_{11}$, $S_{12}$, and $D_{12}$ are 1, 1, and 1 respectively.

iii) During $\delta_s$. The output $V_{T1}$ remains in zero, but $V_{T2}$ is positive. During this time the inductor current will be decreased. For the $V_{AC}$, the positive output voltage is now produced. Then, to obtain these voltages, the proper signals for the switches $S_{11}$, $S_{12}$, and $D_{12}$ are 1, 0, and 1 respectively.

iv) During $\delta_{smax} - \delta_s$. The output of $V_{T1}$ is still in zero, and $V_{T2}$ remains positive (until the inductor has current). During this time the inductor current will be decreased until reach the zero current, and this occurs because the switches of the output bridge are turned off. For the $V_{AC}$ an output of zero is produced again. Then, to obtain these voltages, the proper signals for the switches $S_{11}$, $S_{12}$, and $D_{12}$ are 1, 1, and 1 respectively.

For the second semi-cycle of $V_{T1}$ similar operating waveforms are obtained, as it can be observed in Fig. 4(a). The main difference is that the negative semi-cycle of $V_{T1}$ and $V_{T2}$ occurs, and then the proper control signals are chosen.

It can be noticed in Fig. 4(a) how the pulse width of VAC is increased, and also how the high-frequency transformer operates at a constant frequency.

### *B. Negative semi-cycle of ac modulation signal*

In Fig. 4(b) are shown the waveforms for the negative semi-cycle of the ac modulating signal. Again only the signals for the upper switches are shown. The control signals of the output bridge are omitted again since they are not involved in the integration. The ac voltage of the rectifier, the voltages of the inductor of the DAB, and also the primary current are shown.

Again $\delta_1$ is bounded to $\delta_{1max}$ and $\delta_s$ is bounded to $\delta_{smax}$. The operation is as follows:

i) During $\delta_1$. The output $V_{T1}$ is positive, but also $V_{T2}$. During this time the inductor current will be increased from the zero value. For the $V_{AC}$ an output of zero is produced. Then, to obtain these voltages, the proper signals for the switches $S_{11}$, $S_{12}$, and $D_{12}$ are 1, 1, and 0 respectively. This is equal to the positive semi-cycle.

ii) During $\delta_{1max} - \delta_1$. The output of $V_{T1}$ is now zero, and $V_{T2}$ remains positive. During this time the inductor current will be decreased. For the $V_{AC}$ an output of zero is still produced. The output voltages are the same as the positive semi-cycle, however, now the control signals are selected differently to have a low switching frequency for some semiconductor legs. Then, to obtain these voltages, the proper signals for the switches $S_{11}$, $S_{12}$, and $D_{12}$ are 0, 0, and 0 respectively.

iii) During $\delta_s$. The output $V_{T1}$ remains in zero, but $V_{T2}$ is positive. During this time the inductor current will be decreased. For the $V_{AC}$, the negative output voltage is now produced. Then, to obtain these voltages, the proper signals for the switches $S_{11}$, $S_{12}$, and $D_{12}$ are 0, 1, and 0 respectively.

iv) During $\delta_{smax} - \delta_s$. The output of $V_{T1}$ is still in zero, and $V_{T2}$ remains positive (until the inductor has current). During this time the inductor current will be decreased until reach the zero current. For the $V_{AC}$ an output of zero is produced again. Then, to obtain these voltages, the proper signals for the switches $S_{11}$, $S_{12}$, and $D_{12}$ are 0, 0, and 0 respectively.

Again here, for the second semi-cycle of $V_{T1}$ similar operating waveforms are obtained, as it can be observed in Fig. 4(b).

## III. Simulation Results

The converter was designed and numerically simulated. The software employed is PSIM®. The parameters of each cell are summarized in Table I. In order to evaluate the performance of the system, different graphs are shown.

The simulated system consists of three cells (like in Fig. 2), but certainly, more cells can be employed. The control signals of each cell are displaced properly to get the multilevel operation at the input, but also to inject a reduced ripple current to the capacitor of the LV-link. That may permit to reduce its size.

### *A. Rectifier stage operation*

The results for the ac/dc stage at steady state are shown in Figs. 5 through 7. The tests show the results for a load of 160mΩ, then an output power of 1MW is obtained.

In Fig. 5, the waveforms of the MV-ac mains voltage and current are shown, but also one cell capacitor voltage is presented. As it can be observed a closed sinusoidal current is obtained, due to the SPWM, but also to the multilevel operation; the power factor is 0.99 and the THD for the current

TABLE I
System Parameters of Each SST Cell

| System parameter | Value |
|---|---|
| Transformer ratio | 5:1 |
| Inductance L | 1 mH |
| Main switching frequency | 1 kHz |
| Input grid voltage | 7.2 kV |
| MV-link voltage | 6 kV |
| LV-link voltage | 400 V |
| Output power | 1 MW |
| Load | 0.16 Ω |

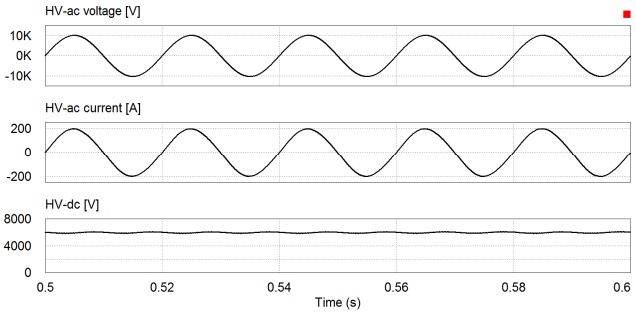


Fig. 5. Simulated results, ac/dc stage. From top to bottom: MV-ac mains voltage, MV-ac mains current, MV-dc cell capacitor voltage.

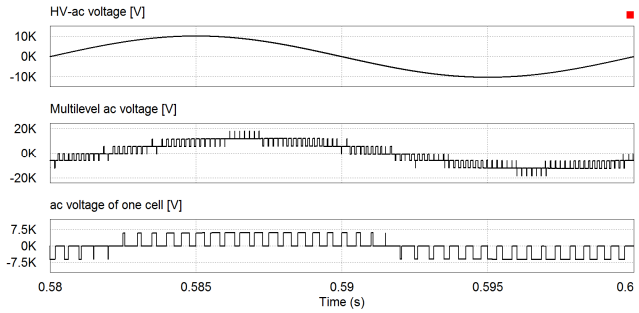


Fig. 6. Simulated results, multilevel ac voltage. From top to bottom: MV-ac mains voltage, multilevel ac voltage, ac voltage of one cell.

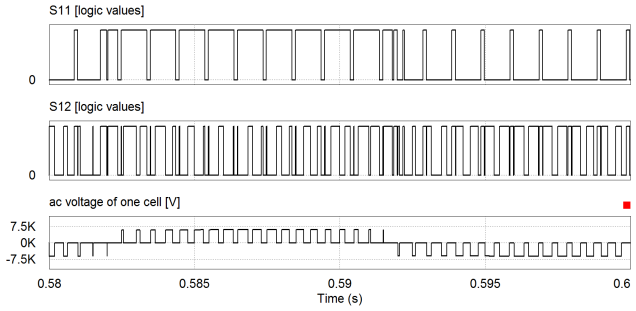


Fig. 7. Simulated results, control signals of ac/dc stage. From top to bottom: $S_{11}$, $S_{12}$ and ac voltage of one cell.

is 1.8%. The voltage of each capacitor cell is less than the peak of the AC mains voltage, as it can be observed, but a lower voltage may be considered if more cells are added.

In Fig. 6 is shown the ac voltage of one cell, but also the complete multilevel output voltage of the system is shown. As it can be observed the complete multilevel ac voltage has a higher frequency compared to a single cell, and this is because the phase displacement considered between the carriers in each rectifier of each cell. Also, the MV-ac mains voltage is shown for comparison purposes.

In Fig. 7 are shown the control signals of the switches for the ac/dc stage for one cell, but also the produced ac voltage is illustrated. The frequency of $S_{11}$ is 1 kHz, but for $S_{12}$ the frequency is the triple, this is the price to pay for the stage integration.

## B. *DAB operation*

The results for the DAB stage at steady state are shown in Figs. 8 and 10. The tests show the results for a load of 160mΩ, then an output power of 1MW is obtained.

In Fig. 8, the waveforms of $V_{T1}$ and $V_{T2}$ are shown, but also the current of the primary winding ($I_L$). As in can be observed the duty cycle of the first bridge is small, but for the other is bigger, the time in zero voltage for $V_{T2}$ is due to the zero current in the transformer. As it can be observed all the signal are in good agreement with the theory presented.

In Fig. 9 are shown the control signals of the switches for the first bridge of the DAB stage, just one cell; additionally, the current of the primary winding is shown. As it can be observed the frequency of all switches is 1 kHz, also the high-frequency transformer operates at a frequency of 1 kHz. It can be noticed that $S_{11}$ is the shared switch for the stage integration. Two graphs are shown in Fig. 9, because they operate differently depending on the semi-cycle of the ac modulating signal; however in each case, the output voltage of the first bridge is the same and also the primary winding current; the main difference is how the zero output voltage is produced.

The currents of the DAB converter, but regarding the output are shown in Fig. 10. In this case, one secondary winding current (Is) and its rectified current (Ir) are presented, but also the complete three cells current in the DC side is illustrated. As it can be observed, the LV capacitor will receive then a reduced ripple current; and this is because of the phase displacement between the different cells.

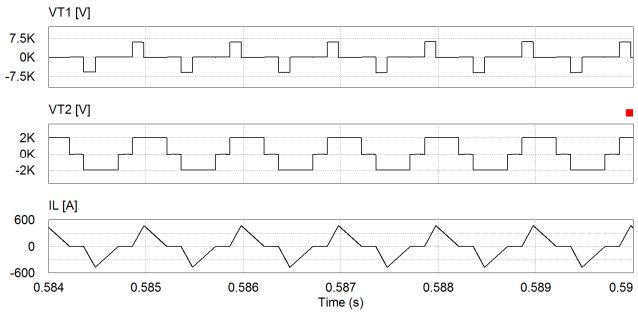


Fig. 8. Simulated results, DAB stage. From top to bottom: $V_{T1}$, $V_{T2}$, and primary winding current.

## C. *Voltage sag test*

The proposed system was tested under a voltage sag of 20%. This test is shown in Fig, 11, and as it can be observed the transition is completely absorbed by the SST. In the MV-link a voltage transition appears, however in the LV-link no voltage variation is registered. The proposal can operate

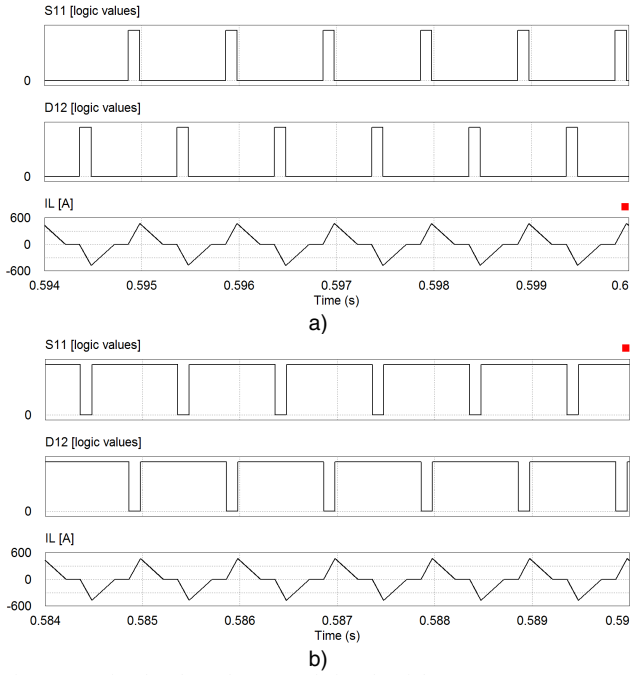


Fig. 9. Simulated results, control signals of the DAB stage. From top to bottom: $S_{11}$, $D_{12}$, and primary winding current. a) when negative semi-cycle of ac occurs, b) when positive semi-cycle of ac occurs.

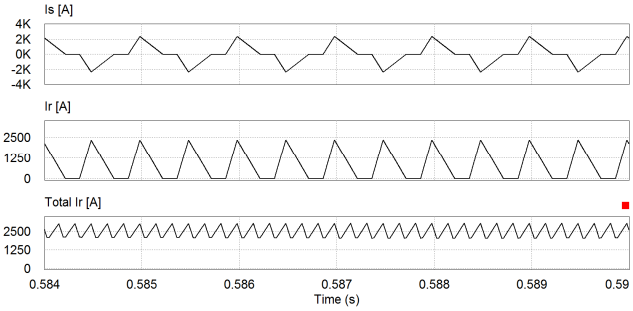


Fig. 10. Simulated results, the output currents of the DAB stage. From top to bottom: secondary winding current, rectified current (one cell), complete rectified current (three cells).

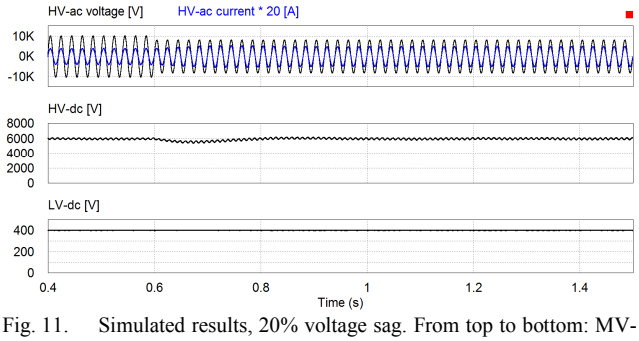


Fig. 11. Simulated results, 20% voltage sag. From top to bottom: MV-ac mains voltage, MV-ac mains current, MV-dc cell capacitor voltage, LV-dc link voltage.

properly even due to the reduction of one power leg per cell; therefore, the proposal is a good alternative to reduce components and maintain the advantages of the three-stage SST.

## IV. Conclusion

The SST is used in different applications, like distribution generation, transportation, and renewable energies, and so on. There are different schemes reported in the literature, and many works are focused on the DAB converter to increase its efficiency and also in the controller. Important challenges in this type of systems are the cost reduction and also the increase in efficiency.

In this paper is proposed the stage integration to reduce the size, volume, but also to reduce the cost. The proposal consists in integrating the ac/dc stage with the first bridge of the DAB. The resultant system has fewer components, one power leg is eliminated per cell; but also the same good input/output characteristics when it is compared to the traditional scheme without the integration. A close to unity PF and current THD of 1.8% are achieved, and due to the multilevel operation, an almost constant current may be provided to the LV-dc capacitor. Certainly more cells can be added, and then the MV-link capacitor may have less voltage, but also the LV-link capacitor will receive a more constant current.

The system was described and numerically simulated; different graphs were illustrated that show clear evidence that the proposal is suitable.

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