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Current-type Power Hardware in the Loop (PHIL) Evaluation for Smart Transformer Application

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***Abstract*—The development of power electronics and power systems due to the massive integration of renewable energy sources is challenging the distribution grids. Among several concepts, the Smart Transformer (ST), a solid-state transformer with advanced control and communication capabilities, has been investigated by several researchers. A great challenge of this kind of system is the possibility to test the effectiveness of the physical system under a broad spectrum of operating conditions. For this reason, the Power Hardware in the Loop (PHIL) concept can be adopted to emulate the behavior of a distribution grid connected to the ST. In this case, because the low-voltage stage of the ST is voltage controlled, the test setup must be current-controlled. In this paper, the current-controlled PHIL setup is analyzed. The theorethical analysis is carried out and preliminary results obtained with the PHIL facilities are presented, highlighting how the current-controlled PHIL can be an effective means to study the ST.**

I. Introduction

The integration of new loads (e.g., electric vehicles) challenges distribution grid management in several aspects, such as intermittent power, voltage violations, reverse power flow and harmonic instability.

The smart transformer (ST) is a power electronics-based transformer [1] that aims not only at adapting the voltage level from medium voltage (MV) to low voltage (LV), but at providing new services to the distribution grids: load identification and control [2], [3], reverse power flow controller [4], reactive power support in MV grid [5], power management in the DC grid [6], grid hosting capacity increase for photovoltaics (PV) and the integration of electric vehicle charging stations [7].

Fig. 1 shows the hardware and control structure of the ST. A three-stage solution is adopted, to guarantee the availability of the DC Links and to decouple the reactive power requirements of the two sides. The MV stage controls the MV current i_{MV}, and an outer voltage (V_{MV}^{*DC}) and reactive power (Q^*) loop gives the current references (i_d^* and i_q^*). The DC/DC stage regulates the power exchange between the two grids and controls the LV DC Link (V_{LV}^{DC}). The DC/AC inverter control target is the voltage (v_{LV}) regulation in the LV grid.

The Power-Hardware-In-Loop (PHIL) simulation by means of a Real Time Digital Simulator (RTDS) system offers new opportunities for hardware testing [8]–[11]. With respect to the classical CHIL evaluation, used for testing controllers and relays, the PHIL simulation allows to analyze the impact on the grid of the hardware under test using a scaled model connected to the RTDS by means of an interface converter. This feature increases the testing possibilities and allows to perform hardware tests without affecting the real grid (e.g., faults, overvoltages, high harmonic content, etc.).

Despite the many advantages that the PHIL has, its implementation is complex and the stability and accuracy of the loop must be studied in order to replicate accurately the behavior of the simulated grid in the hardware setup. The accuracy of the PHIL evaluation is related to the capacity of the interface converter controller (e.g., a linear power amplifier) to follow the reference signals sent by RTDS, keeping the system stable without any undesired behavior (e.g., instability caused by loop delays). The stability and accuracy of the loop depends on the chosen interface algorithm between software and hardware and on the interface converter [8], [9], [12]. The interface algorithm must be tailored to the application of the PHIL and incorrect tuning may lead to hardware behavior, which is not consistent with the RTDS simulation.

II. Loop modelling and Stability

The PHIL facility realized in lab is composed by 4 parts: the Hardware under Test (HuT) (the LV side of the ST), the RTDS, the linear power amplifier (3 phase, 4 quadrant Spitzenberger&Spies $PAS15000$), and the dSPACE control desk working station (Fig. 2).

The PHIL is realized by means of a current-type loop. The ST controls the voltage v_L on the filter capacitor. The measurement system measures the voltage and sends the measurement signals v_L to the RTDS software, RSCAD. Here the voltage is applied directly in the simulated grid by means of an ideal controlled voltage source. The current demanded by the grid i_g^* is sampled by the RTDS and sent to a current controller, that controls the current injection i_g of the linear power amplifier in order to reproduce accurately the grid current in RTDS i_g, closing the loop. Between the simulated grid and the ST hardware, a current scale factor can be chosen to represent in software systems bigger than the HuT size. In this case a scale factor of 50 has been introduced in the current to cope with the limited power capability of the hardware in lab. It means that $1\,\mathrm{A}$ current change in the hardware side corresponds to $50\,\mathrm{A}$ current change in RSCAD. Any change in the current absorption in RSCAD, due to a different load demand, influences the ST controller, and, vice-versa, any change in the ST voltage amplitude or frequency, impacts on the grid power consumption.

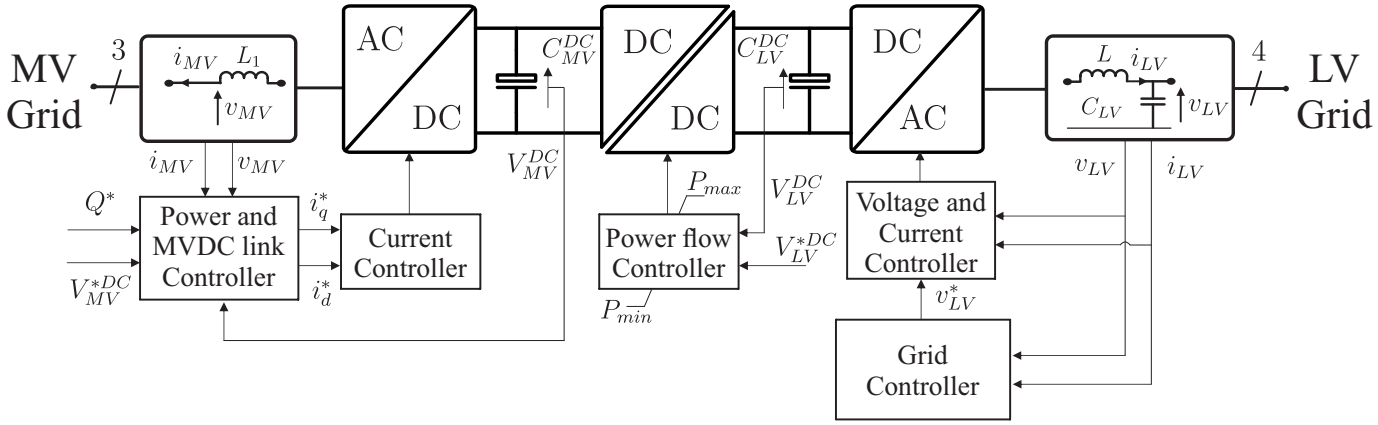

Fig. 1: Control structure of the ST.

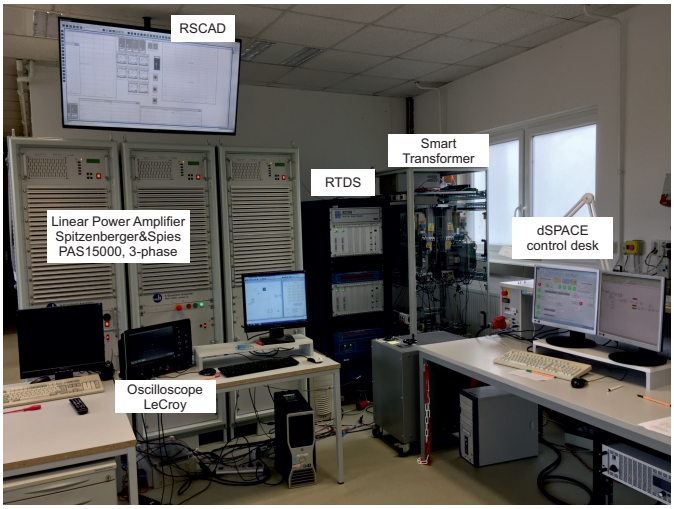

Fig. 2: Picture of the experimental setup with the main components highlighted.

III. Experimental Test Facility

The PHIL stability and accuracy are important for achieving realistic grid conditions in the laboratory. They are interlaced: the stability is a necessary condition for the PHIL evaluation, and it is needed for the evaluation accuracy and the equipment safety [9]. The accuracy of the PHIL can be defined as the capacity of the PHIL to reproduce in hardware a certain variable simulated in RSCAD with a certain dynamic. In the particular case of the current-type PHIL, it refers to the capacity of the power amplifier current controller to reproduce in hardware the current flowing in RSCAD.

However, the PHIL is composed of several interconnected elements, such as RTDS, power amplifier and HuT (i.e., the ST), working with their own controllers and dynamics. Hence, their interaction can affect the stability and accuracy of the loop in reproducing in the hardware side what simulated in RTDS. The purpose of this section is to analyze mathematically the stability and the accuracy of the loop in Fig. 3, and to perform a proper tuning of the power amplifier controller in order to get a tradeoff between accuracy and system stability.

The system shown in Fig. 3 can be represented mathematically as in Fig. 4. The ST and the RTDS are interfaced due to the voltage measurement v_L, that is reproduced in RSCAD as voltage source. Following, the RTDS provides the current reference i_L^* to the current controller implemented in RTDS, which controls the current on the inductor L_{PA}. This current i_g corresponds to the same output current of the ST filter on the grid side.

The transfer function written in the blocks in Fig. 4, are defined as follows:

$$
\begin{aligned}
F_{ST}(s) &= \frac{\frac{1}{sC_L} + R_{dL}}{\frac{1}{sC_L} + R_{dL} + L_L s + R_L} \\
RTDS(s) &= \frac{1}{L_{load}s + R_{load}} \cdot del_{RTDS} \\
CC_{ST}(s) &= K_{pi} \cdot del_{ST} \\
VC_{ST}(s) &= K_{pv} + K_{rv}\frac{s}{s^2 + w^2} \\
CC_{PA}(s) &= K_{pPA} + \frac{K_{iPA}}{s} + K_{rPA}\frac{s}{s^2 + w^2} \cdot del_{RTDS}^2 \\
del_{ST}(s) &= \frac{-T_c s + 1}{T_c s + 1} \\
del_{RTDS}(s) &= \frac{-T_c/2\, s + 1}{T_c/2\, s + 1}
\end{aligned}
\tag{1}
$$

where F_{ST} represents the ST LC filter transfer function, except for the contribution of the grid current $(L_L s + R_L)i_g$; $RTDS(s)$ is the equivalent grid implemented in RSCAD, composed of a passive LR load; CC_{ST} and VC_{ST} are respectively the ST current and voltage loop transfer function; CC_{PA} is the current controller of the power amplifier transfer function; and $del_{ST}(s)$ and $del_{RTDS}(s)$ are the delay transfer function of the ST and the RTDS, represented as Padé first order approximation of a time step T_c=100 μs. This

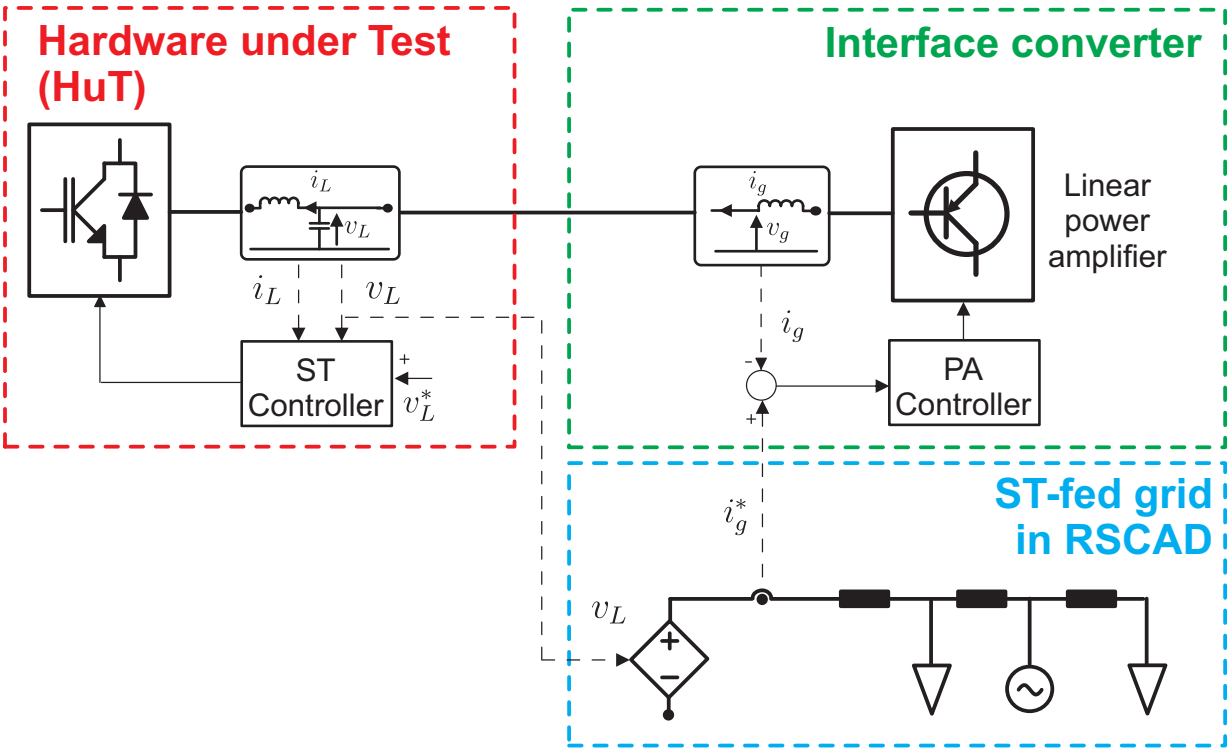

Fig. 3: PHIL: Hardware system (red frame), simulated system (green frame).

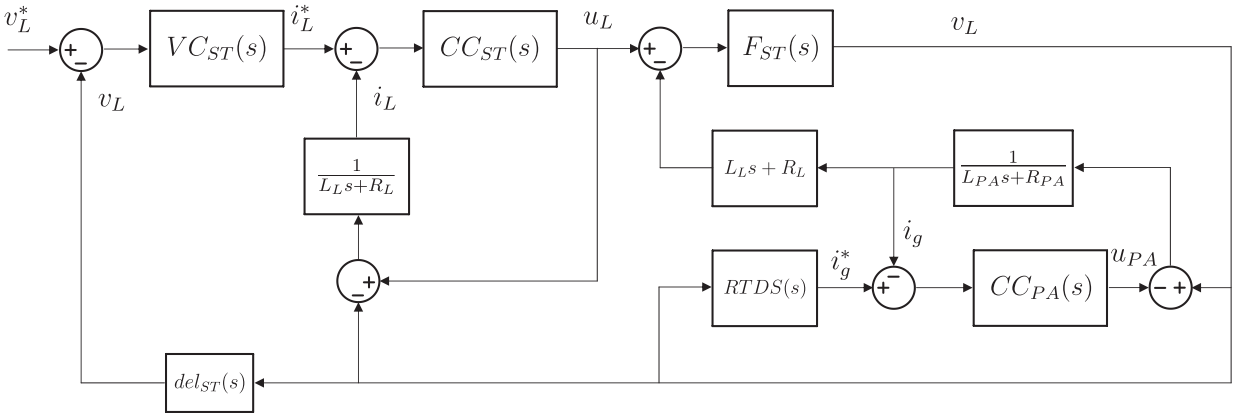

Fig. 4: Equivalent transfer function scheme of the PHIL setup depicted in Fig. 3

approximation is an acceptable tradeoff between accuracy and complexity in representing the delay. Moreover, the number of poles and zeros introduced in the transfer function are kept at the minimum. The Padé approximation equations of a single time step delay are described in (2), where the approximations up to the third order are listed. As can be noted in Fig. 5, where a delay of the single time step 50 μs is considered (i.e., $del_{RTDS}(s)$), increasing the order of the Padé approximation does not give substantial benefits in the dynamics to justify a higher complexity and more poles pairs in the transfer function.

$$
\begin{aligned}
Pade^1 &= \frac{2 - sT_c}{2 + sT_c} \\
Pade^2 &= \frac{12 - 6sT_c + (sT_c)^2}{12 + 6sT_c + (sT_c)^2} \\
Pade^3 &= \frac{120 - 60sT_c + 12(sT_c)^2 - (sT_c)^3}{120 + 60sT_c + 12(sT_c)^2 + (sT_c)^3}
\end{aligned}
\tag{2}
$$

The power amplifier parameters and ST-fed grid data simulated in RSCAD are listed in Table I. A current ratio i_{ratio} between the software and the hardware side is set to 50 initially

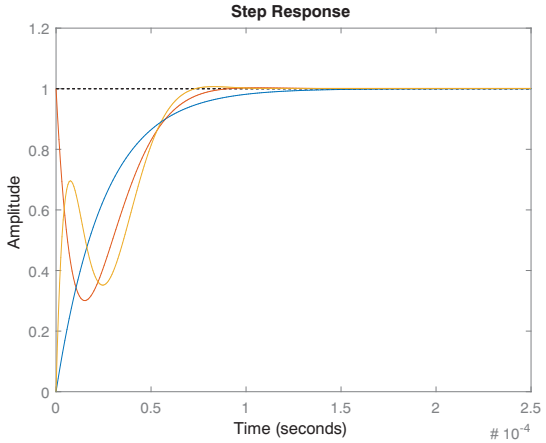

Fig. 5: Pade delay approximation of a delay $50\,\mu$s: first order (blue line), second order (red line), and third order (yellow line).

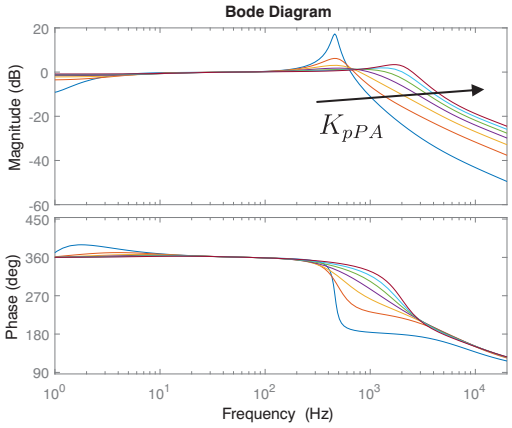

Fig. 6: Power amplifier current controller and plant close-loop bode plot.

in order to simulate large grids (hundreds of kW) with a small lab setup (4 kW).

TABLE I: PHIL power amplifier parameters

Parameter	Value	Parameter	Value
T_c	$50\,\mu$s	T_{ST}	$100\,\mu$s
L_{PA}	$2.4\,m$H	R_{PA}	$0.1\,\Omega$
R_{load}	$1\,\Omega$	L_{load}	1 mH
i_{ratio}	50 pu		

The power amplifier controller bandwidth can be increased, incrementing the value of the proportional controller K_{pPA}. In Fig. 6, the gain K_{pPA} has been varied from 1 to 19 with steps of 3, in order to show three effects created by the different controller bandwidth: the resonant peak present with low proportional gain (about 700 Hz) decreases, till disappearing with a gain higher than 7; a new resonance peak is present for higher gains at higher frequencies (1100 Hz), but of minor magnitude; and the power amplifier current controller bandwidth increases from 700 Hz in case of low gains, up to 3 kHz with gain K_{pPA}=19.

However, high power amplifier bandwidth may lead the system to instability. As shown in Fig. 7a, where the transfer function v_L/v_L^* is plotted, increasing K_{pPA} values, the stability of the system is affected. For a gain higher than 16, the system is not stable, and slightly lower gains (e.g. 13) may lead to high oscillatory behavior in the system. Another point to be noted, is the behavior over the frequency spectrum of the loop transfer function (Fig. 7b). Increasing the power amplifier controller gain, the response of the system tends to flatten over the frequency spectrum, and the resonance peak at high frequency (around 4 kHz) increases till the point it is not damped anymore (0 dB condition). As aforementioned, the tuning of the power amplifier controller must be done following a tradeoff between stability of the system and accuracy in reproducing the software phenomena in hardware side. For the ST testing, it is need a power amplifier current controller bandwidth high enough to represent the current dynamics up to several harmonics of the fundamental frequency (e.g. 13^{th} harmonic, that is 650 Hz). Thus the current controller tuning must have flat response in amplitude and limited phase shift in the desired range. For these reason, the tuning parameters listed in Table II have been chosen.

TABLE II: Power amplifier current controller parameters

Parameter	Kp_{PA}	Ki_{PA}	Kr_{PA}
Value	10	6	20000

IV. Conclusion

This paper has analyzed the current-type Power Hardware in the Loop control for a Smart Transformer applications. The theoretical analysis showed that a high bandwidth of the current controller of the interface is needed to correctly represents the emulated grid, however, stability problems arise.

V. Acknowledgement

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References

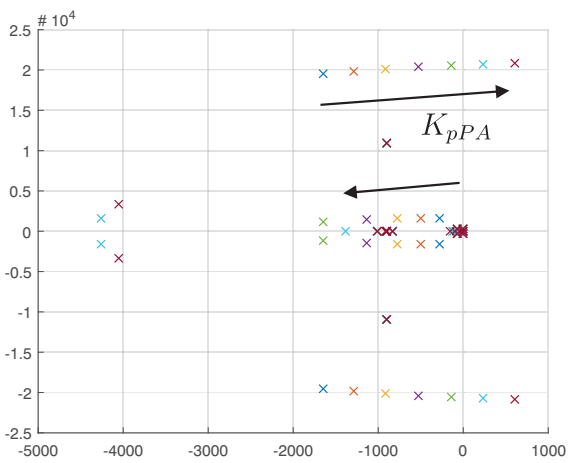
[1] M. Liserre, G. Buticchi, M. Andresen, G. De Carne, L. Costa, and Z. Zhiziang, "The smart transformer: Impact on the electric grid and technology challenges," *IEEE Industrial Electronics Magazine*, in press.

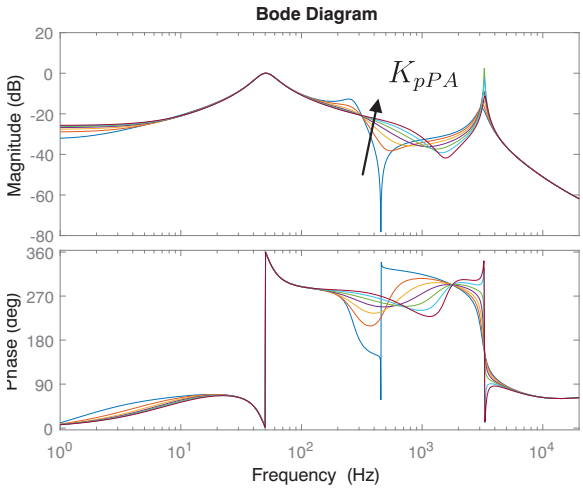
[2] G. D. Carne, M. Liserre, and C. Vournas, "On-line load sensitivity identification in lv distribution grids," *IEEE Transactions on Power Systems*, vol. PP, no. 99, pp. 1–1, 2016.

[3] G. De Carne, G. Buticchi, M. Liserre, and C. Vournas, "Load control using sensitivity identification by means of smart transformer," *IEEE Transactions on Smart Grid*, vol. PP, no. 99, pp. 1–1, 2016.

[4] G. Buticchi, G. D. Carne, D. Barater, Z. Zou, and M. Liserre, "Analysis of the frequency-based control of a master/slave microgrid," *IET Renewable Power Generation*, June 2016. [Online]. Available: http://digital-library.theiet.org/content/journals/10.1049/iet-rpg.2016.0167

[5] A. Q. Huang, "Medium-voltage solid-state transformer: Technology for a smarter and resilient grid," *IEEE Industrial Electronics Magazine*, vol. 10, no. 3, pp. 29–42, Sept 2016.





(a) (b)

Fig. 7: Loop stability analysis: (a) Root locus, and (b) close-loop bode plot of the transfer function v_L/v_L^*.

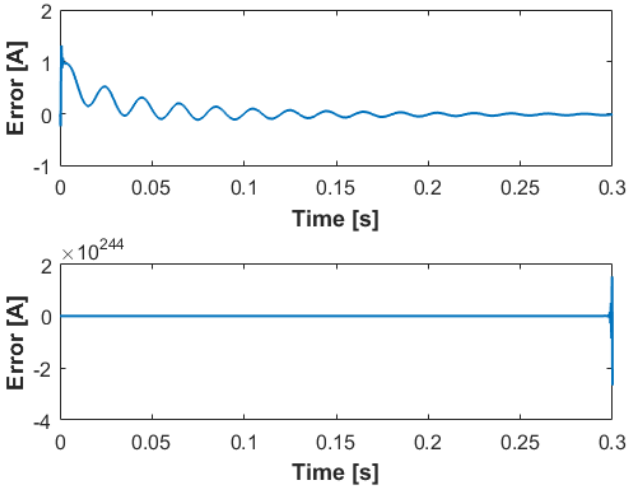


Fig. 8: Current error in case of: (a) Stable case (K_{pPA}=7), (b) Unstable case (K_{pPA}=16).

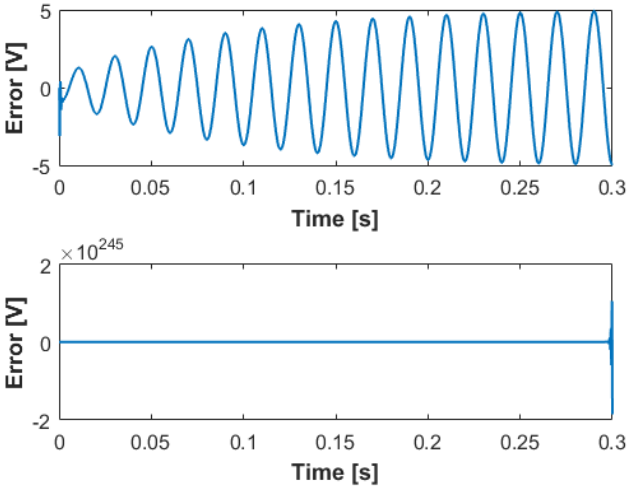


Fig. 9: Voltage error in case of: (a) Stable case (K_{pPA}=7), (b) Unstable case (K_{pPA}=16).

[6] X. Yu, X. She, X. Zhou, and A. Huang, "Power management for dc microgrid enabled by solid-state transformer," *IEEE Transactions on Smart Grid*, vol. 5, no. 2, pp. 954–965, March 2014.

[7] S. Huang, J. Pillai, M. Liserre, and B. Bak-Jensen, "Improving photovoltaic and electric vehicle penetration in distribution grids with smart transformer," in *4th Innovative Smart Grid Technologies Europe (ISGT EUROPE)*, Oct 2013, pp. 1–5.

[8] G. Lauss, M. Faruque, K. Schoder, C. Dufour, A. Viehweider, and J. Langston, "Characteristics and design of power hardware-in-the-loop simulations for electrical power systems," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 1, pp. 406–417, Jan 2016.

[9] C. Edrington, M. Steurer, J. Langston, T. El-Mezyani, and K. Schoder, "Role of power hardware in the loop in modeling and simulation for experimentation in power and energy systems," *Proceedings of the IEEE*, vol. 103, no. 12, pp. 2401–2409, Dec 2015.

[10] P. Kotsampopoulos, F. Lehfuss, G. Lauss, B. Bletterie, and N. Hatziargyriou, "The limitations of digital simulation and the advantages of phil testing in studying distributed generation provision of ancillary services," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 9, pp. 5502–5515, Sept 2015.

[11] F. Huerta, J. K. Gruber, M. Prodanovic, and P. Matatagui, "Power-hardware-in-the-loop test beds: evaluation tools for grid integration of distributed energy resources," *IEEE Industry Applications Magazine*, vol. 22, no. 2, pp. 18–26, March 2016.

[12] W. Ren, M. Steurer, and T. Baldwin, "Improve the stability and the accuracy of power hardware-in-the-loop simulation by selecting appropriate interface algorithms," *IEEE Transactions on Industry Applications*, vol. 44, no. 4, pp. 1286–1294, July 2008.