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Noise Efficient Integrated Amplifier Designs for Biomedical Applications

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Abstract: The recording of neural signals with small monolithically integrated amplifiers is of high interest in research as well as in commercial applications, where it is common to acquire 100 or more channels in parallel. This paper reviews the recent developments in low-noise biomedical amplifier design based on CMOS technology, including lateral bipolar devices. Seven major circuit topology categories are identified and analyzed on a per-channel basis in terms of their noise-efficiency factor (NEF), input-referred absolute noise, current consumption, and area. A historical trend towards lower NEF is observed whilst absolute noise power and current consumption exhibit a widespread over more than five orders of magnitude. The performance of lateral bipolar transistors as amplifier input devices is examined by transistor-level simulations and measurements from five different prototype designs fabricated in 180 nm and 350 nm CMOS technology. The lowest measured noise floor is 9.9 nV/$\sqrt{\text{Hz}}$ with a 10 µA bias current, which results in a NEF of 1.2.

Keywords: noise efficiency; NEF; lateral BJT; chopper stabilized; OTA; inverter based; current reuse; folded-cascode; multistage; low noise; low power; CMOS

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1. Introduction

Wearable and implantable devices for the recording of neural signals receive increasing interest in medicine and behavioral research. Applications range from recording action potentials from individual nerves with an implant to measuring the projection of compound signals on the tissue surface using wearable setups. All systems have in common that they are size and, consequentially, power limited. Thus, they require a high-quality amplifier input stage, which works within the tight power budget. Often, multiple channels are recorded in parallel. This limits the amount of power available for the individual amplifier even further. Examples for surface recorded biopotentials include the electromyogram (EMG) acquired with electrodes on the skin above muscles and the electrocardiogram (ECG) for heart activity monitoring. A system for a highly miniaturized wireless multichannel EMG of a flying dragonfly was presented in [1]. To enable more selective recording, tissue penetrating electrodes and associated interface electronics have been devised. In 1969, Wise et al. presented a microelectrode for extracellular recording with a minimum tip diameter of 2 µm and an integrated buffer amplifier for at least four channels [2]. Hoogerwerf and Wise then demonstrated a 3-dimensional 4 × 4 microelectrode array recording probe in 1994 based on a silicon platform [3].

Local field potentials (LFP) measured from the brain have been demonstrated to enable motion prediction [4]. In 2007, an integrated neural recording system with a microelectrode array suitable for recording action potentials (AP) from at least 100 probes was reported [5]. More recently, in 2016, the Neuropixel platform offers over 966 parallel recording channels [6]. Furthermore, integrated amplifiers allow the use of intracortical implanted systems, including brain–computer interfaces. Brain–computer interfaces are

used for the control of an exoskeleton [7], real-time brain-to-text translation of handwritten messages [8], or wireless on-screen selection tasks [9]. Acquiring the electroencephalogram (EEG) from the brain enables automatic drug deposition in closed-loop anesthesia. Novel closed-loop approaches target the treatment of epileptic seizures [10,11]. Algorithms for the interpretation of the EEG [12,13] and the combination with implantable drug-releasing units lead to novel therapeutic strategies for patients [14]. Brain activity mapping of mice with microprobes containing more than a thousand electrodes [15] is now a frequently used method in animal research [15–17]. Recently an even smaller system for mice in the first postnatal weeks was presented [18].

The acquired signals are typically in the range of a few tens of microvolts [19]. Although the required amplifier bandwidth varies for different biomedical applications, low-frequency operation not exceeding a few tens of kilohertz is a typical specification [20–22]. Generally, the preamplifier determines the signal-to-noise-ratio (SNR) of the signal processing chain [23]. Noise entering after the initial signal amplification becomes less detrimental. Consequently, the pre-amplifier has to be designed very carefully to yield low input-referred noise (IRN), and its voltage gain is high. The gain requirement results from the signal amplitude in the micro- to millivolt range that is amplified to the typical voltage range of integrated analog electronic circuits of about 1 V to 5 V, depending on technology. Thus, factors of 60 dB or more are common, and an IRN of less than 10 µV ensures that the signal may be well discriminated from the noise with an SNR much larger than 10 dB [24]. Reliable suppression of electrode offset voltages before amplification becomes essential to maintain appropriate dynamic range, and it presents a major design challenge. The review presented in [23] indicates that it is not uncommon to spend over 30% of the total power budget on pre-amplification to meet the tight noise requirements. The power budget is ultimately limited by the resulting heat generation, which must not cause any tissue damage. A safe power level of about 10 mW is suggested in [5] (equivalent to 100 µW per channel for the reported 100-channel system). It agrees well with the power available via wireless transfer [12]. Moreover, size is of concern, especially in the case of amplifier arrays. Considering a typical chip area of 1.5 mm × 1.5 mm, a 10-channel design must occupy below 0.23 mm^2 active area per channel (less if the area for pads and auxiliary circuits is factored in). Therefore, integrated circuit technology (mostly mature CMOS) is employed for highly miniaturized systems. Table 1 summarizes essential design parameters. The values are further supported by data from an extensive review of publications presented in Section 3.

Table 1. Typical parameters for biomedical amplifiers on a per-channel basis in systems with a large number of parallel channels.

Parameter	Value
Power	<100 µW
Gain	>60 dB
Bandwidth for	
• ECG	100 Hz
• Local Field Potentials (LFP)	500 Hz
• Single-fiber Action Potentials (AP)	10 kHz
Integrated IRN	<10 µV
Size	<0.23 mm^2
CMOS technology node	<0.5 µm

A CMOS input stage provides a good trade-off between high input impedance, high gain, low power consumption, and reasonable manufacturing costs [23]. However, the noise of a MOS field-effect transistor is dominated at low frequencies by its high intrinsic flicker noise. Vertical bipolar junction transistors (BJT) tend to yield lower input-referred flicker noise but have a lower input impedance and are expensive when additional process-

ing steps are required for production. Lateral BJT is sometimes employed as an alternative, as they are compatible with standard CMOS fabrication. However, lacking optimized material properties, these devices are less efficient and require higher bias current to yield comparable gain and noise as their optimized vertical equivalents. In addition to the technological properties of the input devices, the circuit topology of the preamplifier plays a major role in finding a sweet spot for the combination of parameters of Table 1.

In the past, a considerable number of pre-amplifiers have been reported with a variety of parameters and design approaches. A review and analysis of these circuits are provided in this paper, and it is structured as follows. In Section 2 we categorize the different amplifier topologies and analyze their suitability for low-noise amplification. Practical examples are then compared in Section 3 in terms of their measured noise/power and area trade-off. Special attention is given to the current-reuse topology as a dedicated structure for multiple channels. In Section 4, the performance of lateral BJT as an input transistor is investigated based on measured results from test structures fabricated in 180 nm and 350 nm CMOS technology. It is followed by a discussion in Section 5 and conclusions in Section 6.

2. Amplifier Topologies

There are conceptually different approaches to implement low-power and low-noise amplifiers for biomedical applications. Here, we sort them into seven major categories depending on their characteristic employment of either chopper techniques, current-reuse strategy, inverter configuration of the input stage, folded-cascode design, the use of multiple gain stages, conventional long-tail pair operational transconductance amplifier (OTA) configuration, or the use of BJT input devices. Simplified schematic diagrams of each of the approaches are shown in Figure 1a–f and are briefly described as follows.

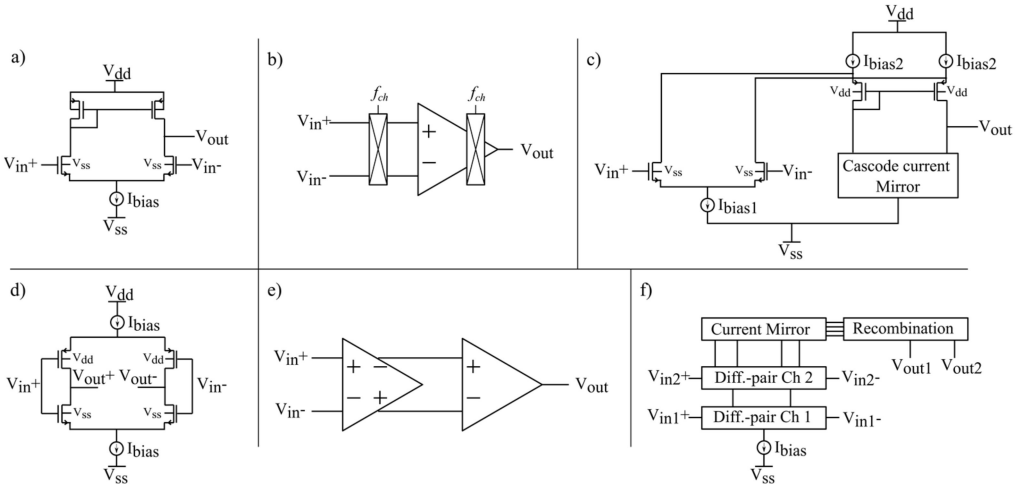

Figure 1. Exemplary configuration of the conceptually different approaches of low-power and low-noise amplification for biomedical applications: (**a**) conventional OTA with a differential input pair, a current mirror as load, and a bias current soure I_{bias}. (**b**) Chopper-stabilized amplifier with the chopping frequency f_{ch}. (**c**) Folded-cascode amplifier with a differential input pair in parallel to the cascoded current mirror, operating as high impedance load. (**d**) Inverter-based amplifier with complementary transistors on the left and right side, respectively, each pair forming an inverter. (**e**) Simple schematic of a multistage amplifier. (**f**) Current-reuse amplifier with an input pair for each channel (marked as Diff.-pair), a current mirror stage, and a recombination stage, which forms the output signal channels.

A. Conventional OTA

This category comprises circuits with a conventional differential pair input-stage followed by an impedance load. The load may be stacked with the input pair or placed in parallel after the input stage current was mirrored to the output stage [25].

B. Chopper input

The chopper amplifier modulates the input signal before amplification with a high-frequency carrier. The up-modulated signal is amplified and later mixed back to the base frequency and filtered. The amplification thus takes place at a higher intermediate frequency whereby low-frequency amplifier noise, especially flicker noise, is avoided. For example, in [26], a chopper-stabilized amplifier for EEG recording is demonstrated.

C. Folded-cascode

The use of folded-cascode amplifiers is a standard technique in CMOS amplifier design, as high linear range, wide common-mode range, and high bandwidth can be achieved with only a few transistors. The differential-pair transconductance input stage of a folded-cascode is operated in parallel with the actual gain stage (which presents the gain-generating high impedance load) [27].

D. Inverter-based input

The inverter-based amplifier is a less common technique. Due to its pseudo-differential input, the common-mode rejection is inherently low compared to a differential input [28]. Furthermore, the inverter-based amplifier is sensitive to process, voltage, and temperature variation [29]. Essentially, a structure resembling the conventional digital CMOS inverter operates around the inverter trigger point where the gain of the circuit is high. Built from few transistors and accordingly low parasitic capacitance, the inverter can achieve wide operating bandwidth with a small supply current. This makes the inverter-based amplifier efficient, and at the same time, the IRN tends to be high (this will become evident from a comparison in the following Sections with Figures 2 and 3). Generally, the noise can be reduced by allowing higher current consumption. In Figure 1d a pair of inverters yields a pseudo-differential configuration, and the use of current sources ensures an improvement of common-mode rejection. An example of a system employing low-power inverter-based amplifiers is given in [29].

E. Multistage amplifier

The multistage approach describes a cascade of gain stages where each stage may have a different topology. The first stage dominates the noise performance and, therefore, consumes most of the power. For example, a two-stage amplifier with a source follower as the second stage is presented in [30].

F. Current reuse

A more recent approach is the vertical stacking of gain elements, which allows to bias all of them with the same bias current. In doing so, channels need staggered common-mode bias voltages to ensure the input transistors are in saturation and to prevent the bias current source from being cut off. This presents a design overhead, which can be considered a major drawback of this approach.

Notably, there are two conceptually different methods of current reuse found in publications. A three-channel differential orthogonal current-reuse amplifier presented in [31] may serve as an example for the first method: In this design, all stacked units are treated as individual amplifiers, thus that the number of channels is increased without requiring additional current consumption in the input stage. Conversely, in the second method, stacked input pairs are used additively to boost the transconductance obtained for a single amplifier, allowing the bias current for each amplifier to be lowered. The latter approach is shown exemplarily in [28], where three stacked inverters generate a sixfold increase in transconductance for a single channel.

3. Noise vs. Power Trade-Off

To enable quantification and comparison of the trade-off between power consumption and noise of an amplifier, the noise efficiency factor (NEF) introduced in [32] has been widely employed as a figure-of-merit. The NEF compares the generated noise to the current

consumed by an amplifier, which is proportional to its power consumption under the assumption of a constant supply voltage. The NEF is especially significant for multichannel applications. Modifications of the NEF exist in the literature, which includes the supply voltage level as an additional factor (termed power-efficiency factor, PEF). However, the supply voltage is frequently set by the voltage requirements of other system components and is often ultimately determined by the battery voltage. Lowering the voltage with linear converters does not improve the power consumption of the system whilst the overhead of active converters in terms of size, design effort, and efficiency is often prohibitive. Therefore, we continue to use the NEF here in its original and most common form:

$$NEF = V_{rms,in}\sqrt{\frac{2 \cdot I_{tot}}{\pi \cdot U_{TH} \cdot 4kT \cdot f_c}} \quad (1)$$

where I_{tot} is the current used per amplifier channel, U_{TH} the thermal voltage (around 26 mV at room temperature), k the Boltzmann constant, T the temperature in Kelvin, f_c the 3-dB cut-off frequency and $V_{rms,in}$ is the IRN integrated over the entire frequency spectrum. The amplifier noise is put into relation with the shot noise generated by an ideal BJT biased with the same total current as the amplifier. Then, the factor $\sqrt{2/(\pi \cdot f_c)}$ results from the assumption of a first-order low-pass characteristic of the amplifier with the 3-dB cut-off frequency f_c. A lower NEF refers to better noise efficiency. Often, a loosely calculated NEF is presented. Either spot noise measurements are employed, or noise integration is not carried out to the cut-off frequency and thus excludes the roll-off tail from consideration. Consequently, a certain amount of variation can be expected from NEF reported in the publications, specific values, which are up to about 20% lower than expected from a rigorous application of Equation (1). For a single transistor design, the lowest possible NEF of unity is achieved by the theoretical ideal BJT. For the targeted biomedical applications, a differential input pair is typically used as it yields higher common-mode rejection. The theoretical NEF limit for a BJT differential input pair is 2 [23]. Only recently, these theoretical limits have been reached and surpassed in practical designs by the use of current-reuse strategies where current I_{tot} is routed to energize multiple stacked amplifiers.

Figure 2 shows measured NEF data reported for amplifier implementations in CMOS technology over the past 35 years. Naturally, the collection of data points is not comprehensive, but it is useful for observing several trends as outlined here. In the case of multichannel designs, the calculation is performed on a per-channel basis thus that any power consumption overhead is shared between channels.

Figure 2 shows the overall steadily improving NEF as indicated by the dashed blue line. The blue dashed line is a linear fit through all data points. Therefore, the linear fit distinguishes the better performing designs in terms of NEF located below the line from the other ones above. It should be pointed out that a higher NEF alone does not indicate a poor design. Often, other system parameters are of higher importance or absolute noise performance is paramount to the relative trade-off indicated by NEF.

Groups of data points can be formed as indicated by the circles. It is observed that the chopper-stabilized amplifiers exhibit a NEF between 2 and 15 with most designs residing in the upper half of the graph. Thus, applying the chopper technique does not seem to lead to improved noise efficiency. The groups of current-reuse, inverter-based, and folded-cascode designs appear in the lower half of the graph. The group of OTA designs spreads over a wide area above and below the line, suggesting that this design approach is suitable for efficient low-noise implementation, but it requires a careful trade-off of the different design specifications to achieve it. There are, for example, direct trade-offs with the device sizes and the input range. The current-reuse topologies are at the leading edge of efficiency.

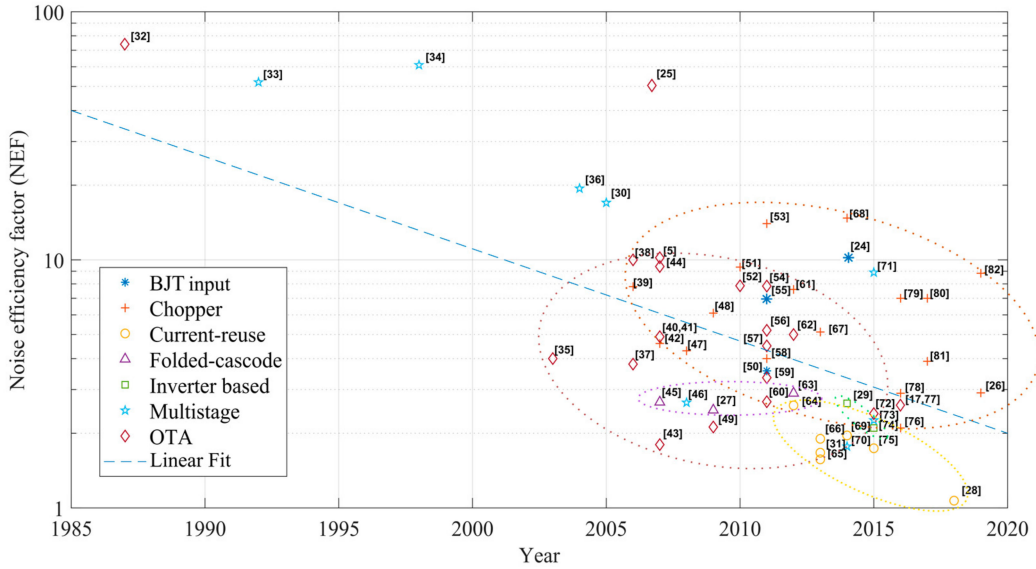

Figure 2. Noise efficiency of different CMOS-based amplifiers for biomedical applications, divided into seven categories. Each marker represents the calculated NEF of the noted reference [32–82] based on measured data ([17,77] are simulated noise data). Groups of data points of the same category are indicated by circles. The dashed line shows the best linear fit through all data points on the logarithmic scale. Designs marked as BJT input are realized with lateral BJT in CMOS technology.

Where there is a trend towards achieving lower NEF in recent years, no such development is seen in terms of absolute IRN. Figure 3 shows a plot of the noise level for the same designs as in Figure 2. As a basis for comparison, the mean spot noise voltage is calculated by integrating the squared noise voltage over the recording bandwidth and then dividing by this bandwidth. The absence of improvement in absolute noise may be explained by the noise target specification for an application in biomedical recording, where a minimum SNR is set for the expected signal amplitude in the microvolt- to millivolt range, as shown in Table 1. However, technological constraints also suggest a minimum noise level using standard dimensions for transistor sizes and currents. Example designs with lower noise are reported for other application areas [83,84] at the cost of additional technological effort, e.g., device cooling. There are only a few designs reported with BJT input transistors, but those that are yield highly competitive IRN. Notably, the choppered amplifiers yield high IRN and a relatively poor NEF. They can be beneficial in avoiding low-frequency noise in critical applications, e.g., the recording of LFP [45]. The inverter-based amplifiers tend to be noisy, which may be explained by the low bias currents in their input devices. Thus, they consume little power and are noise efficient, as seen in Figure 2.

The amplifiers compared here are mostly dedicated research prototypes for which less stringent requirements in terms of reliability, cost and usability apply compared to commercial production-line chips. To see if the option of individual chip tuning and optimization is reflected in the resulting noise performance, a comparison with published commercial devices is on order: Intan Technologies published an input-referred noise of 0.288 fV/Hz in the AP bandwidth for their RHD2216 interface chip [85]. Neuralink presented a chip with an input-referred noise of 3.48 fV/Hz [86]. The neuropixel platform by IMEC yields 2.5 fV/Hz in the AP bandwidth [15], including the noise generated by the electrode probe. These three examples confirm the overall picture drawn for the research devices of Figure 3, with an IRN located in the lower half of the chart and well within the cloud of research-grade designs.

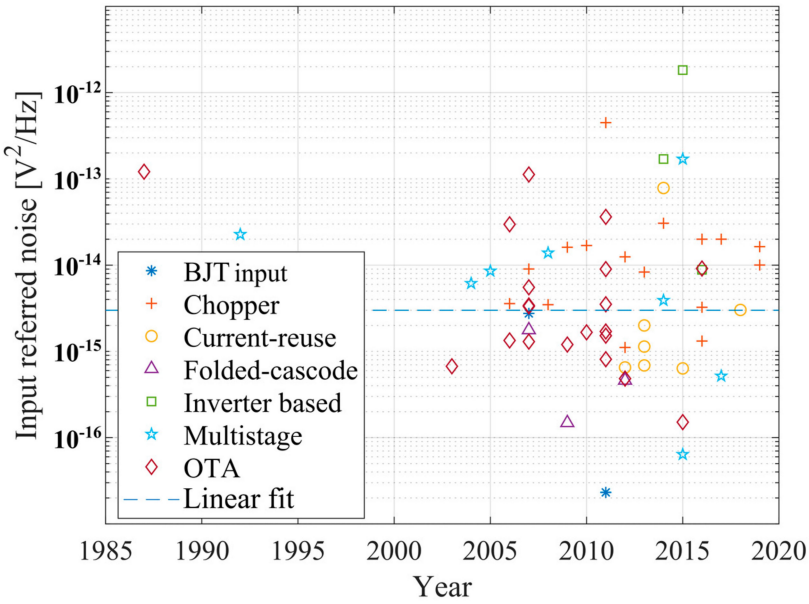

Figure 3. Average squared and integrated IRN of the amplifier topologies divided by their bandwidth. The dashed line is the best linear fit through all data points on the logarithmic scale.

For each of the seven topologies shown in Figure 2, major noise contributors can be identified. The input stage clearly dominates the noise in the OTA or inverter-based topology. In the chopper-stabilized amplifier, the switches of the input chopper induce charge injection, which leads to parasitic current flow in the input leads and generates additional current noise [87]. It is dependent on the chopping frequency and the amplitude of the chopper clock [87] and may be detrimental for high-impedance loads. For the folded-cascode topology the main noise contributors besides the input stage are the folding current mirrors and the (cascaded) output current mirrors [88]. In the current-reuse topology, the output recombination stage is a key factor. For a three-channel current reuse topology, eight current branches from the input stage are mirrored to the output stage. The multitude of mirrors requires careful design and takes a significant share of the overall current consumption as IRN of the mirrors must be reduced by a high transconductance [89].

A comparison of the mean current consumption for the different classes of design as well as the minimum and maximum total current values presented in Figure 4 completes the noise efficiency comparison. It is observed that the inverter-based technique uses the least current followed by the current-reuse technique. The current consumption of the chopper amplifiers is in the average region, exhibiting a considerable spread. Markedly, many publications remain vague about whether the power consumed for the generation of the chopper clock signals is included in their reported figures. Overall, a current consumption on the order of 1 µA per channel is seen to be a typical value, although with a widespread over more than one order of magnitude. For the commercial neuropixel a current consumption of 27.2 µA per channel (considering the power for the whole system) is reported [6].

The density of recording channels is affected by choice of implementation technology, and it may limit the maximum number of channels that can be implemented. Figure 5 shows the technologies employed for the designs of Figure 2 and their proportion of use. Overall, 70 percent of the technology nodes for biomedical applications are smaller than 500 nanometers. Nearly half of all circuits were designed in a 180 nanometer or smaller technology. With a share of 32 percent, the 180 nanometer technology is the most commonly used technology. Although the area per channel is only specified in few publications, 75 percent of these circuits are smaller than 0.23 mm^2 per channel. These empirical data support the values given in Table 1.

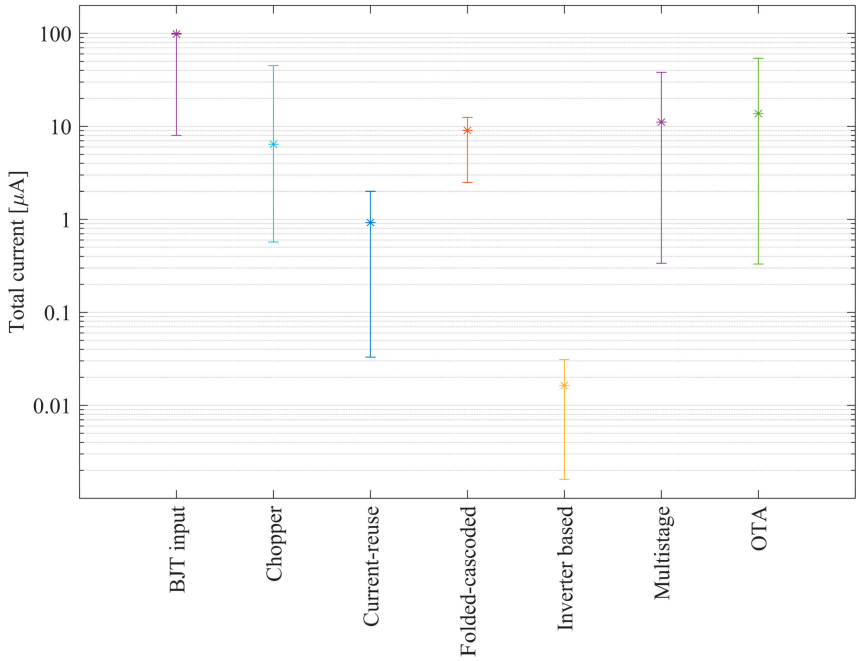

Figure 4. Average total current of the different amplifier categories and the published maximum and minimum values.

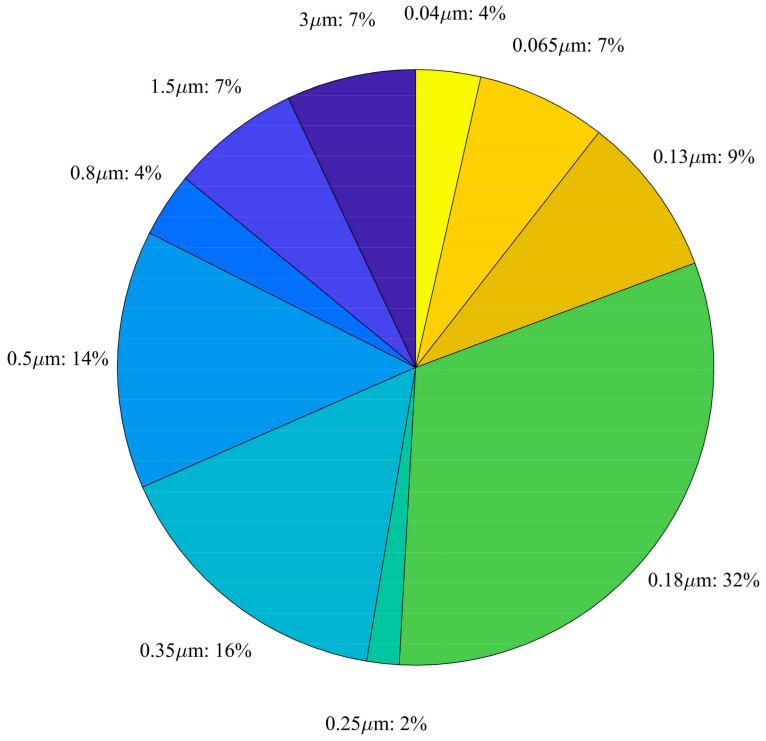

Figure 5. Break-down of CMOS Technology nodes used in the publications of Figure 2.

When MOS transistors are used as input devices, their size significantly affects the noise performance since the transconductance of the input stage scales with transistor width, and the gate area determines the flicker noise [90]. Although it is not the input stage alone that determines the overall system area and less than half of all publications shown in Figure 2 specify the area used per channel, it is informative to observe the noise performance in comparison to the circuit area. Figure 6 shows the NEF versus the area that

is used per channel. The area was normalized to account for the different technologies by dividing through the smallest producible area in the technology (i.e., the technology node size squared). For the larger designs, no direct correlation between the normalized area and the NEF can be observed. There is, however, a currently unpopulated area shaded in gray in Figure 6, which indicates a limit for the current size/noise trade-off. Moving towards smaller designs that would allow even higher channel density while maintaining a NEF well below 10 remains a current challenge.

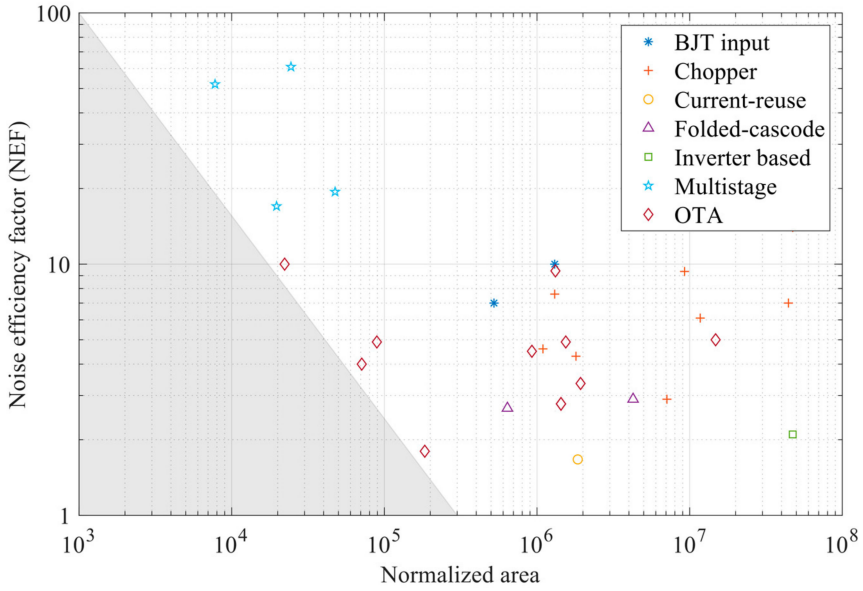

Figure 6. Comparison of the NEF and the normalized area per channel. The gray marked area shows a potential for improvement in biomedical amplifier design.

4. Lateral Bipolar Input Devices

Since biomedical applications often require amplification of very low-frequency signals, flicker noise power may become a dominant factor, as it is inversely proportional to frequency. Increasing the area of MOS devices can help reduce the input-referred flicker noise but may trade-off with limited amplifier bandwidth or stability due to higher parasitic capacitive load. The chopper technique can avoid the flicker noise bandwidth but comes with the aforementioned limitations in terms of current noise, power, and design overhead. By-and-large, the low-frequency noise is determined by technology constraints and offers limited optimization possibilities for the circuit designer. Accordingly, the noise corner-frequency has not seen any notable improvement over the years. For the designs investigated in Section 3, a minimum corner frequency of 0.5 Hz and a maximum corner frequency of 10 kHz is observed. Therefore, bipolar devices, which operate by bulk conduction and avoid the noise generating surface defect region, may exhibit lower flicker noise and are used as alternative input devices in selected applications.

The observation that only a few designs report the use of BJT can be partially attributed to the lower input impedance of the BJT compared to MOS transistors, making them less suitable for high-impedance electrode interfaces. The input resistance is somewhat technology-dependent, but commonly not exceeding the 100-kilo Ohm range [24]. Certain interface electrodes, including poly(3,4-ethylene-dioxythiophene) (PEDOT) or PEDOT-carbon-nanotube (CNT) coated microelectrode arrays as well as multi-electrode nerve cuffs for peripheral nerve recording, yield a low contact impedance of only a few kilo Ohms [50,91]. In these cases, the input impedance of a BJT input stage is higher than the electrode impedance, and shunt effects are negligible. A design challenge remains the compensation of residual input base currents, which can be addressed using compensating current sources at the base inputs [90].

The higher manufacturing cost and lower availability of dedicated BiCMOS manufacturing options make it necessary to implement BJT in standard CMOS technology as lateral devices. These, however, are not generally provided as standard device cells in all CMOS design kits and often remain poorly characterized. In the following, we examine different lateral BJT implementations for their key performance parameters based on measured prototype devices manufactured in 350 nm and 180 nm CMOS technologies. Figure 7a shows the cross-sectional structure of a typical lateral BJT where either a polysilicon layer or a metal layer above the base region serves to repel charge carriers away from the surface region deeper into the conducting bulk material.

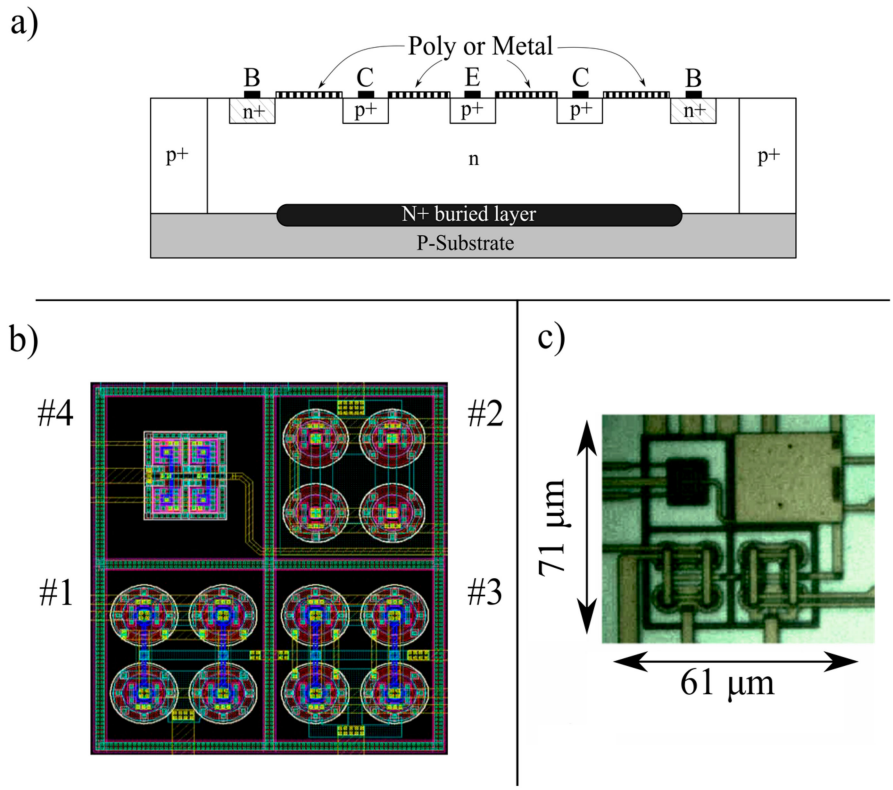

Figure 7. (**a**) Cross-section of a lateral BJT with a poly or a metal layer covering the BJT above the base region. (**b**) Layout of four prototype designs: BJT #1 is of circular shape with a poly layer above the base region. BJT #2 is a circular shape, but instead, metal covers the base region. BJT #3 is a Darlington pair transistor based on BJT #1. The BJT #4 has a poly-covered square shape. The BJT #4 design was also fabricated in 180 nm technology as BJT #5. (**c**) Microphotograph of the fabricated designs corresponding to the layout in (**b**).

Figure 7b shows the layout of four prototype designs, labeled BJT #1–#4. Each of the first three designs consists of four identical lateral BJT connected in parallel. The fourth design is a pair of parallel BJT connected in a Darlington configuration, which yields a higher forward current gain β. Firstly, all four designs are fabricated in 350 nm CMOS technology (photo of the active area shown in Figure 7c) and characterized. Secondly, the square transistor layout BJT #1 is also fabricated in 180 nm technology, here referred to as BJT #5.

It is known that β decreases with increasing emitter current bias [92]. This is especially expected for these devices realized without layers optimized for BJT operation, thus exhibiting pronounced high injection effects. The measured low-current β-factors of the lateral BJT prototypes from Figure 7b are shown in Table 2 together with other measured key parameters when the transistors are biased with moderate emitter current. The lateral BJT possesses a parasitic vertical transistor [93], causing part of the bias current to leak into

the substrate. This leads to a reduced measured current efficiency of 0.7 and less. Layout BJT #2, which uses a less effective metal layer instead of polysilicon to bias the active region, is found to be the least optimal design in terms of current gain, current efficiency, and input resistance. Designs #1 and #4 demonstrate the best performance. However, since not all design kits allow round shapes in the design rules, the square layout of BJT #4 is generally preferred. Moving this layout to 180 nm technology shows a decrease in the input resistance, current efficiency, and transconductance but an increase in current gain and Early voltage. To examine the noise performance, pairs of devices are connected in the differential setup shown in Figure 8. The bias tail current I_{bias} was chosen as 20 µA, and the load resistors were 100 kΩ.

Table 2. Measured results of the lateral BJT Prototypes shown in Figure 7b with 10 µA emitter bias current (I_{bias} = 20 µA).

	BJT #1	**BJT #2**	**BJT #3 (Darlington Pair)**	**BJT #4**	**BJT #5**
Current gain β	50	29	188	77	45
Current efficiency α	0.7	0.4	0.7	0.8	0.4
Early voltage	14 V	6 V	12 V	6 V	33 V
Input resistance r_π	199 kΩ	153 kΩ	1543 kΩ	272 kΩ	202 kΩ
Transconductance g_m	256 µA/V	190 µA/V	122 µA/V	285 µA/V	224 µA/V
IRN [nV/$\sqrt{}$Hz]	9.96	11.9	29	10.8	9.91
NEF	1.21	1.45	3.5	1.3	1.20

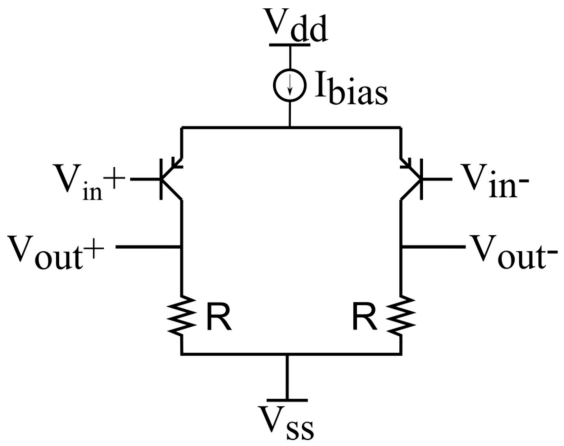

Figure 8. Symmetrical noise measurement setup with two lateral BJT (from two chips with designs as in Figure 5) with resistive loads of 100 kΩ and a bias current I_{bias} of 20 µA.

Assuming ideal BJT transistors yields for the input-referred spot noise density of each input transistor

$$V_{n\_in} = \sqrt{\frac{4q \cdot U_{TH}^2}{I_{bias}/2}} \tag{2}$$

where q is the electron charge and all other parameters as defined before. For the chosen bias tail current of 20 µA a V_{n_in} of 6.6 nV/$\sqrt{}$Hz was calculated. The measured voltage noise referred to a single transistor is presented in Table 2 for each design. It agrees well with the analytical expectation (with the exception of the Darlington pair not represented by Equation (2)). BJT #3 yields the highest noise. This is well explained by its low transconductance. The circular design #1 yields the best results. However, square design #4 is not far off and shows even lower noise in 180 nm technology (BJT #5). The flicker noise corner-frequency was measured for all devices below 100 Hz. The NEF is calculated between 1.2

and 3.5 for all presented prototypes and approaches the theoretical ideal BJT with an NEF of unity. The Darlington pair BJT #3 has the highest NEF due to its high IRN.

As an exemplary comparison between an amplifier using MOS input transistors compared to lateral BJT, we have simulated a pair of folded-cascode amplifiers in a standard 180 nm CMOS technology using Cadence design tools. In the first design, using lateral BJT, the differential-pair input stage is biased with a tail current of 10 µA, which is close to the mean value in Figure 4 for a folded-cascode amplifier. This results in a gain-bandwidth-product of 80 MHz and an IRN floor of 11 nV/$\sqrt{\text{Hz}}$. The comparable MOS-input amplifier is biased with the same tail current. The simulated input-referred noise floor is determined as 16 nV/$\sqrt{\text{Hz}}$, i.e., significantly higher with the same power consumption. As the theoretical input-referred shot noise of a MOS transistor is calculated by a factor of $2/3\ g_m$ versus $1/2\ g_m$ for a BJT transistor [23], the measurement is in good agreement with theoretical expectation. Integrating the IRN of the MOS folded-cascode between 50 Hz and 10 kHz, leads to 7.5 μV_{rms}. Hereby, a NEF of 9.1 is reached. Looking back at Figure 2, a NEF of 12.9 is significantly above the linear fit. For the folded-cascode with lateral BJT input stage, an integrated noise of 1.3 μV_{rms} is calculated, leading to a NEF of 2.2. Compared to Figure 2, the lateral BJT folded-cascode is right on the fitted line. The simulated input-referred noise is plotted in Figure 9, including the low-frequency flicker noise contribution. It is also put into comparison with the measured noise floor of the individual BJT designs. They are in good agreement with the results simulated for the complete amplifiers, as is expected for a design in which the input device dominates the overall IRN.

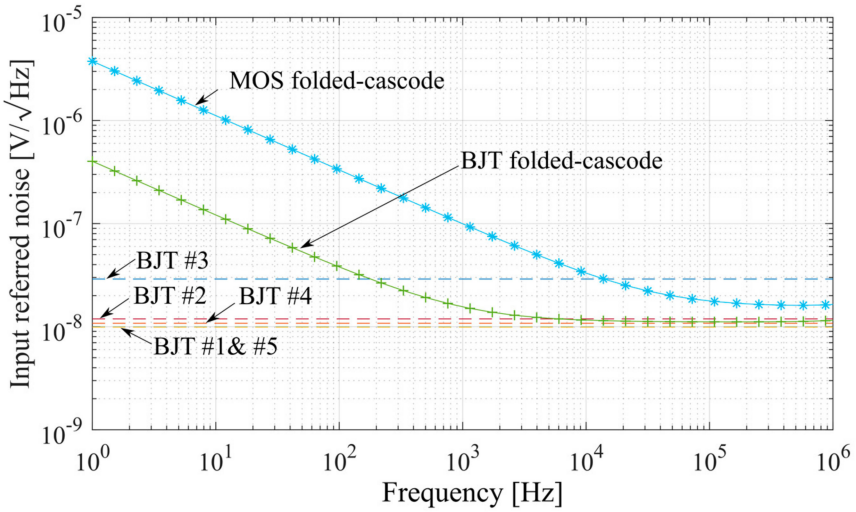

Figure 9. IRN comparison of simulated folded-cascode amplifiers with CMOS and BJT input devices. The total bias current is 20 µA. As a reference the measured noise floor of the lateral BJTs from Table 2 are marked as dashed lines.

5. Discussion

The current-reuse topology has been shown as achieving the overall best noise/efficiency trade-off with an NEF of 1.07. To reach this good result, the recombination stage also needs to be designed for low noise. In addition, the different common-mode bias voltages that are needed to bias each input transistor pair (the stacked stages labeled as differential pair in Figure 1f) at its intended operating point need to be realized. This is often achieved by capacitive AC-coupling of the input signal, thus precluding recording at very low frequencies [31]. The inverter-based amplifiers excel in terms of low current consumption. As a result, the IRN is higher than average. Therefore, it is especially interesting for applications uncritical to absolute noise but with high demands on power efficiency. The chopper-stabilized amplifiers are well suited for very low-frequency applications, but they suffer from current noise induced by charge injection and design overhead. Additionally, the good noise and power performance of folded-cascode amplifiers have been shown in Figures 3 and 4. The multistage amplifier

and the OTA are common amplifier designs for a wide range of uses. They are relatively uncomplicated to design and still yield good noise efficiency.

Concerning the choice of input transistors, the (lateral) BJT demonstrates the best absolute noise performance (5 nV/$\sqrt{\text{Hz}}$ was achieved for a complete amplifier). Highly optimized vertical devices in a dedicated manufacturing technology yield very high transconductance and subsequently low wideband noise for a given bias current when compared to CMOS counterparts [90]. Lateral devices manufactured cost-efficiently in standard CMOS technology are less efficient in this respect. Still, lateral BJT tends to generate less Flicker noise and, therefore, often presents an optimum choice for applications in the different biomedical bandwidths presented in Table 1. Clearly, their relatively low input impedance renders them less suitable for high impedance electrodes. But in combination with, for example, neural interfaces, including PEDOT coated electrodes and nerve cuff electrodes, they have the potential to perform well. To evaluate the effect of layout choices on the BJT performance in direct comparison, we have designed and measured four lateral BJT prototypes. Proper biasing of the base region is crucial for current efficiency, current gain, and input resistance, which leads to a preference of adding a polysilicon layer above the base region rather than using a less effective metal interconnect layer for this purpose. The best performance is obtained with a circular layout. However, not all design rules allow circular-shaped designs. The square layout with similarly good performance has been established as a practical compromise. Transferring and scaling the same square transistor layout to a smaller technology node shows further improved noise performance. The NEF obtained with all evaluated lateral devices (excluding the Darlington Pair) comes close to the ideal target of unity. A pair of folded-cascode amplifiers in 180 nm CMOS technology with MOS and with lateral BJT input transistors has been simulated as a practical example. The IRN is dominated by the input stage in these designs. A NEF of 2.2 has been reached for the folded-cascode amplifier with lateral BJT and a NEF of 12.9 for the MOS input stage, both with identical current consumption and gain-bandwidth-product.

6. Conclusions

Future applications require further miniaturized and parallelized amplifiers for the detection of biopotentials, including LFP, AP, and EEG. An improving trend in noise efficiency has been observed. The effects of design choices on noise and related trade-offs have been discussed by sorting the designs into seven topologies. A lower limit of the absolute IRN of published amplifiers for biomedical applications has been noticed. The need for steadily improving current consumption per channel has been observed from the historical data and explained by the continuing need for ever higher channel count and density in biomedical applications, especially neural interfaces. The current-reuse topology has been shown as offering the best noise/efficiency trade-off in this respect.

Although the lateral BJT input stages yield the best absolute noise performance and low flicker noise, it is noticed that only a few lateral BJT input stages are used. A total of five different lateral BJT prototypes were fabricated and presented here, all exhibiting competitive NEF. The lateral BJT amplifier is confirmed by simulation as a suitable design for highly efficient and low noise applications, although limited to low resistance electrode loads.

It is expected that the combination of noise-optimized input devices together with a current-reuse strategy employed in high-channel-count systems (in which also biasing overheads are effectively shared between channels) will be able to reduce the NEF on a per-channel basis well below unity in the near future while maintaining an absolute IRN in the order of 10 nV/$\sqrt{\text{Hz}}$. Achieving a NEF below 10 with a normalized area of less than 20,000 squares remains an open challenge.

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supervision, R.R. and A.B.; project administration, R.R.; funding acquisition, R.R. All authors have read and agreed to the published version of the manuscript.

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