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# Enhanced Current Capability for Modular Multilevel Converters by a Combined Sorting Algorithm for Capacitor Voltages and Semiconductor Losses

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***Abstract*—The modular multilevel converter (MMC) has become very attractive for high- and medium-voltage applications, generating excellent waveforms at very high efficiencies. One of the main challenges is the appropriate selection of inserted submodules (SMs), commonly done by capacitor voltage balancing algorithms. However, the semiconductor stress can only be balanced up to a certain degree by conventional algorithms, since the stress is not directly monitored. An uneven stress distribution between the SMs does not only result in different lifetime expectations, but also in increased maximum temperatures, for which each SM needs to be designed. With the goal of more effective utilization of chip area, a new balancing approach is introduced for monitoring and balancing not only the capacitor voltages but also the average power losses in each SM. In this way, the MMC current capability is significantly increased only by software without deteriorating the system performance and efficiency.**

## I. Introduction

The modular multilevel converter (MMC) has become a very popular topology for high-voltage and medium-voltage applications due to full controllability and easy scalability to different power levels [1]. Even fundamental switching frequency modulation methods, such as nearest level modulation (NLM), become suitable, whereas the individual submodules (SMs) will commonly be directly selected for balancing the capacitor voltages [2]. However, conventional balancing approaches do not automatically equalize the stress between the SMs, being particularly crucial for high number of SMs, low switching frequency and low power factors [3],[4]. These imbalances will be further increased due to parameter variations of components, caused by manufacturing and aging processes [5]. Consequently, even independent from the application there is a high attraction to utilize the redundancy of switching states not only to balance the capacitor voltages but also to equalize the semiconductor stress between the SMs. For proper SM selection, the stress of each semiconductor needs to be evaluated. This can be achieved by taking into account the junction temperatures as demonstrated in [3]-[5]. However, the online computation effort for accurate thermal modeling is quiet high and the utilization of additional temperature sensors should be avoided, especially for a high number of SMs.

As less expensive alternative, this paper introduces an approach to monitor and balance the average semiconductor power losses among all SMs, the effectiveness of stress balancing but also the associated enhanced MMC current carrying capability is exemplary demonstrated for a medium-voltage Static Synchronous Compensator (STATCOM) as a study case. The provided analysis is supported by thermal investigations of each SM.

This manuscript is organized as follows. Section II describes the basic principle of MMC. The proposed advanced balancing approach is introduced in Section III. In Section IV the effectiveness of the algorithm is proved by electrical and thermal results. Finally, the conclusion is given in Section V.

## II. Modular Multilevel Converter

In Fig. 1 the electrical circuit of the modular multilevel converter is depicted, whereas a STATCOM application is considered. Different from dc-connected applications the stored energy in the capacitors needs to be controlled from the ac grid. As modulation method, NLM has been selected with the goal of achieving maximum efficiency [6],[7]. Accordingly, the insertion number of each arm will be directly calculated to generate the closest possible voltage level according to (1), (2) [8].

$$n_{\mathrm{on,p}} = \mathrm{round}\left(\frac{N}{2} - \frac{v^*_{\mathrm{conv}}}{v^*_{\mathrm{c}}} - \frac{v^*_{\mathrm{diff}}}{2v^*_{\mathrm{c}}}\right) \tag{1}$$

$$n_{\mathrm{on,n}} = \mathrm{round}\left(\frac{N}{2} + \frac{v^*_{\mathrm{conv}}}{v^*_{\mathrm{c}}} - \frac{v^*_{\mathrm{diff}}}{2v^*_{\mathrm{c}}}\right) \tag{2}$$

The ac grid current will be controlled by the converter voltage, defined in (3) [9].

$$v_{\mathrm{conv}} = \frac{v_{\mathrm{n}} - v_{\mathrm{p}}}{2} \tag{3}$$

In contrast, the differential voltage describes the voltage across the arm inductors and can be used to control the circulating currents [10]. Both voltages can be set by the voltages across the SMs in each arm [11]. The mathematical

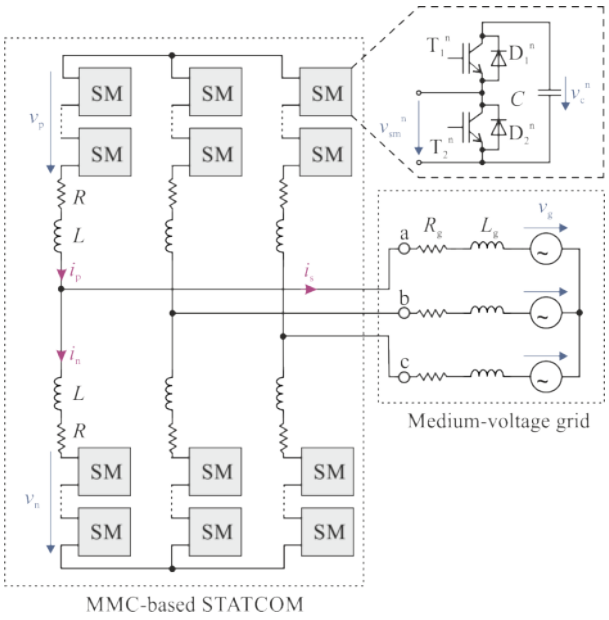



Figure 1: Modular multilevel converter in double-star half-bridge configuration.

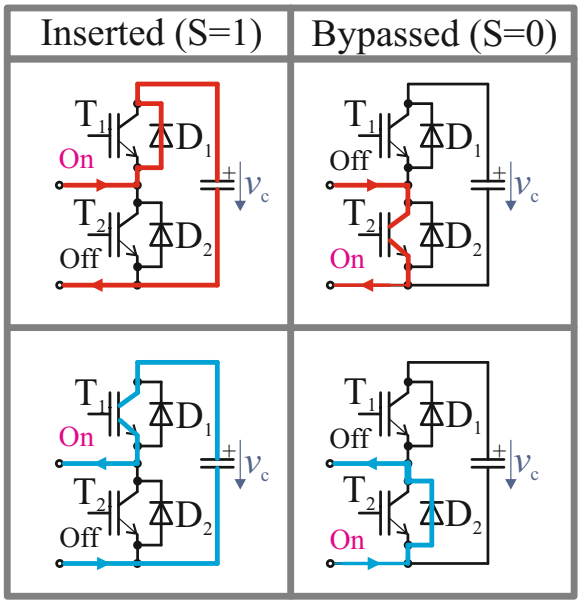



Figure 2: Current paths in one SM during normal operation.

definition of the arm voltages (p: upper arm, n: lower arm) is provided in (4) whereas the index n corresponds to the number of the SM.

$$v_{\mathrm{p|n}} = \sum_{n=1}^{N} v_{\mathrm{c}}^{n} \tag{4}$$

In Fig. 2 the possible current paths of one SM are depicted during normal operation. In order to balance the capacitor voltages in each arm, the SMs to be inserted or bypassed are commonly selected by the capacitor voltage, the switching state and the arm current direction [2].

## III. Advanced Submodule Balancing

Conventional capacitor voltage balancing approaches are able to balance the stress between the SMs up to a certain degree since the turn-on time of each SM will be limited due to its varying state of charge. However, especially at low switching frequencies, the switching patterns of the SMs can become very inhomogeneous, leading to a high spread in the semiconductor junction temperatures for the different SMs [3],[4]. This effect becomes even stronger at low power factors when the arm current is oscillating around zero, changing the polarity after each half period [3],[4]. Particularly during the negative half-period it is not adequate to only monitor the capacitor voltages because the state of charge remains approximately constant although conduction losses for IGBT $T_2$ and diode $D_2$ are created by the arm current. Consequently, the stress of the SMs needs to be directly controlled to achieve an effective balancing of the SM stress. This is not only crucial for the lifetime of the semiconductors [4] but also for an economic converter design as it will be shown in Section IV.

The goal of advanced SM balancing is to select the individual SM not only by its capacitor voltage but also by other criteria as the stress of the semiconductors. For this purpose, four cost functions are introduced in (5)-(8), where both the capacitor voltages and the averaged semiconductor power losses of each SM are taken into account.

$$c_1^{\mathrm{n}} = (v_{\mathrm{c}}^{\mathrm{n}} - v_{\mathrm{c,min}}) + \alpha_1(\overline{P}_{\mathrm{l,D1}}^{\mathrm{n}} - \overline{P}_{\mathrm{l,D1,min}}) \tag{5}$$

$$c_2^{\mathrm{n}} = (v_{\mathrm{c,max}} - v_{\mathrm{c}}^{\mathrm{n}}) + \alpha_2(\overline{P}_{\mathrm{l,T2}}^{\mathrm{n}} - \overline{P}_{\mathrm{l,T2,min}}) \tag{6}$$

$$c_3^{\mathrm{n}} = (v_{\mathrm{c,max}} - v_{\mathrm{c}}^{\mathrm{n}}) + \alpha_3(\overline{P}_{\mathrm{l,T1}}^{\mathrm{n}} - \overline{P}_{\mathrm{l,T1,min}}) \tag{7}$$

$$c_4^{\mathrm{n}} = (v_{\mathrm{c}}^{\mathrm{n}} - v_{\mathrm{c,min}}) + \alpha_4(\overline{P}_{\mathrm{l,D2}}^{\mathrm{n}} - \overline{P}_{\mathrm{l,D2,min}}) \tag{8}$$

The power losses of each semiconductor can be approximated by its datasheet characteristics and by the measured capacitor voltages and arm currents. According to Fig. 2 the semiconductors $T_2$ and $D_1$ are stressed during positive wave of the arm current. The occurring conduction losses can be calculated by (9), (10), where the forward voltages of IGBT and diode are defined as $v_{\mathrm{ce}}$ and $v_{\mathrm{f}}$, respectively.

$$\overline{P}_{\mathrm{l,T2,con}}^{n}(t) = \frac{1}{T_{\mathrm{av}}} \int_{t-T_{\mathrm{av}}}^{t} (1 - S^{n}(t')) \cdot v_{\mathrm{ce}}^{n}(t') \cdot i_{\mathrm{arm}}(t') dt' \tag{9}$$

$$\overline{P}_{\mathrm{l,D1,con}}^{n}(t) = \frac{1}{T_{\mathrm{av}}} \int_{t-T_{\mathrm{av}}}^{t} S^{n}(t') \cdot v_{\mathrm{f}}^{n}(t') \cdot i_{\mathrm{arm}}(t') dt' \tag{10}$$

On the other hand, the switching losses are described in (11), (12), whereas the switching energy $E_{\mathrm{sw}}$ depends on capacitor voltage, arm current and the direction of the switching transient. The value $cm^{n}$ is changing from 0 to 1 for each occurring commutation.

The turn-on losses of the diodes are usually negligible. All power losses are averaged over the time period $T_{\mathrm{av}}$ which should be selected as at least one grid period due to the

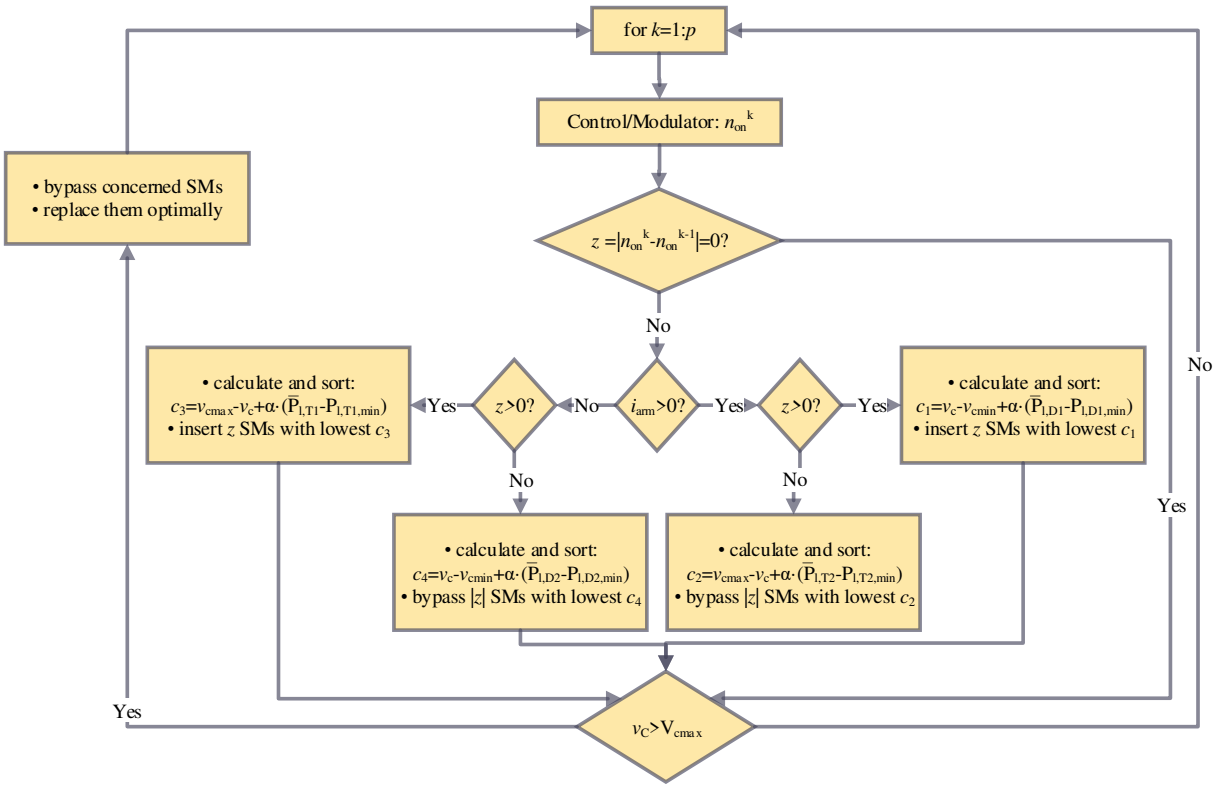



Figure 3: Flowchart for advanced SM balancing.

periodic behavior of the system. The weighting factor $\alpha$ needs to be adapted for a proper weighting of the semiconductor losses whereas a value of $\alpha = 0$ represents a conventional capacitor voltage balancing approach.

$$\overline{P}^{n}_{\mathrm{l,T2,sw}}(t) = \frac{1}{T_{\mathrm{av}}^2}\int_{t-T_{\mathrm{av}}}^{t} cm^{n}(t')\cdot E^{n}_{\mathrm{sw,T2}}(t')dt' \tag{11}$$

$$\overline{P}^{n}_{\mathrm{l,D1,sw}}(t) = \frac{1}{T_{\mathrm{av}}^2}\int_{t-T_{\mathrm{av}}}^{t} cm^{n}(t')\cdot E^{n}_{\mathrm{sw,D1}}(t')dt' \tag{12}$$

The semiconductors $T_1$ and $D_2$ are stressed during negative wave of the arm current. Accordingly, the averaged conduction losses and switching losses can be described by (13)-(16).

$$\overline{P}^{n}_{\mathrm{l,T1,con}}(t) = \frac{1}{T_{\mathrm{av}}}\int_{t-T_{\mathrm{av}}}^{t} S^{n}(t')\cdot v^{n}_{\mathrm{ce}}(t')\cdot|i_{\mathrm{arm}}(t')|dt' \tag{13}$$

$$\overline{P}^{n}_{\mathrm{l,D2,con}}(t) = \frac{1}{T_{\mathrm{av}}}\int_{t-T_{\mathrm{av}}}^{t} (1-S^{n}(t'))\cdot v^{n}_{\mathrm{f}}(t')\cdot|i_{\mathrm{arm}}(t')|dt' \tag{14}$$

$$\overline{P}^{n}_{\mathrm{l,T1,sw}}(t) = \frac{1}{T_{\mathrm{av}}^2}\int_{t-T_{\mathrm{av}}}^{t} cm^{n}(t')\cdot E^{n}_{\mathrm{sw,T1}}(t')dt' \tag{15}$$

$$\overline{P}^{n}_{\mathrm{l,sw,D2}}(t) = \frac{1}{T_{\mathrm{av}}^2}\int_{t-T_{\mathrm{av}}}^{t} cm^{n}(t')\cdot E^{n}_{\mathrm{sw,D2}}(t')dt' \tag{16}$$

The application of advanced SM balancing is further described in Table I. The SMs will be selected by minimizing one of the cost functions, in dependence of switching state, required switching action and arm current direction. In this way, the SMs will be not only selected by minimizing the spread in the capacitor voltages, but also by minimizing the average power losses of the subsequently loaded semiconductor.

Table I: Approach of advanced submodule balancing by minimization of cost functions.

| $i_{\mathrm{arm}}$ | Switching on (0→1) | Switching off (1→0) |
|---|---|---|
| positive | $\min\{c_1\}$ | $\min\{c_2\}$ |
| negative | $\min\{c_3\}$ | $\min\{c_4\}$ |

In general, the introduced approach is simply applicable for each control/modulation approach as long as the SM sorting is centralized. This becomes clear with the provided flowchart in Fig. 3 where k describes the number of sampling. After each sampling period, the control/modulator provides the number of inserted SMs $n_{\mathrm{on}}$ in each arm. If this number is changing, the SMs will be inserted/bypassed in analogue to Table I without directly affecting voltage shaping and switching frequency. Independent of the advanced balancing algorithm, an overvoltage protection is implemented to limit the maximum capacitor voltage to $V_{\mathrm{cmax}}$.

The consideration of average semiconductor losses is practically motivated, because the online computation effort can be strongly reduced by abandoning thermal modeling. An

Table II: MMC simulation parameters.

| Description | Parameter | Value | Unit |
|---|---|---|---|
| SMs per arm | $N$ | 40 | |
| SM's capacitance | $C$ | 30 | mF |
| Cap. voltage ref. | $v_c^*$ | 955 | V |
| Cap. voltage limit | $V_{c,max}$ | 1050 | V |
| Arm inductor | $L$ | 3 | mH |
| Arm resistance | $R$ | 17 | mΩ |
| Grid voltage (rms) | $V_g$ | 20 | kV |
| Grid inductance | $L_g$ | 1.13 | mH |

equalized distribution of power losses consequently also leads to an equal distribution of average temperatures if the cooling is assumed to be similar, whereas only the thermal cycles would be affected by the thermal time constants and the averaging interval.

## IV. Simulation Results

As a study cases, a 30 MVA medium-voltage STATCOM application is considered, whereas the applied parameters are summarized in Table II. Both ac-side and dc-side currents are properly controlled by standard balancing ($\alpha = 0$) as illustrated in Fig. 4 (study case I). The waveform generation is excellent without any need for additional filters.

As power modules, the 1700 V IGBT module FF600R17KE3 B2 from Infineon has been selected, rated for a dc-collector current of 600 A. Power losses of 29.8 kW are occurring in each arm as illustrated in Fig. 5, whereas the conduction losses are dominant. For minimization of the computation time, the online calculation of switching losses can be avoided for this application.

For the advanced balancing (study case II), a weighting factor $\alpha = 0.2\,\mathrm{V/W}$ and an averaging time of $T_{av} = 0.02\,\mathrm{s}$ (one grid period) have been selected, not affecting the converter efficiency according to Fig. 5. In Fig. 6 the junction temperatures of each semiconductor are depicted, with maximum temperatures in diode $D_1$ created by the low power factor. By activating the advanced balancing, the thermal spread between the SMs can be strongly reduced for all semiconductors. For the most stressed semiconductor $D_1$ the maximum occurring junction temperatures have been reduced from 100 °C to 95 °C, by keeping the semiconductor power losses and average temperatures constant.

For further analysis, the junction temperature distribution of all 40 SMs is depicted in Fig. 7 and 8 for diode $D_1$ and IGBT $T_1$, respectively. Taking into consideration the periodic behavior of the system, the temperatures are averaged over one grid period. Also for the averaged temperatures, the distribution has been significantly equalized. The temperature range of $D_1$ has been reduced from 11 K to 6 K and the temperature range of $T_1$ from 8 K to 4 K.

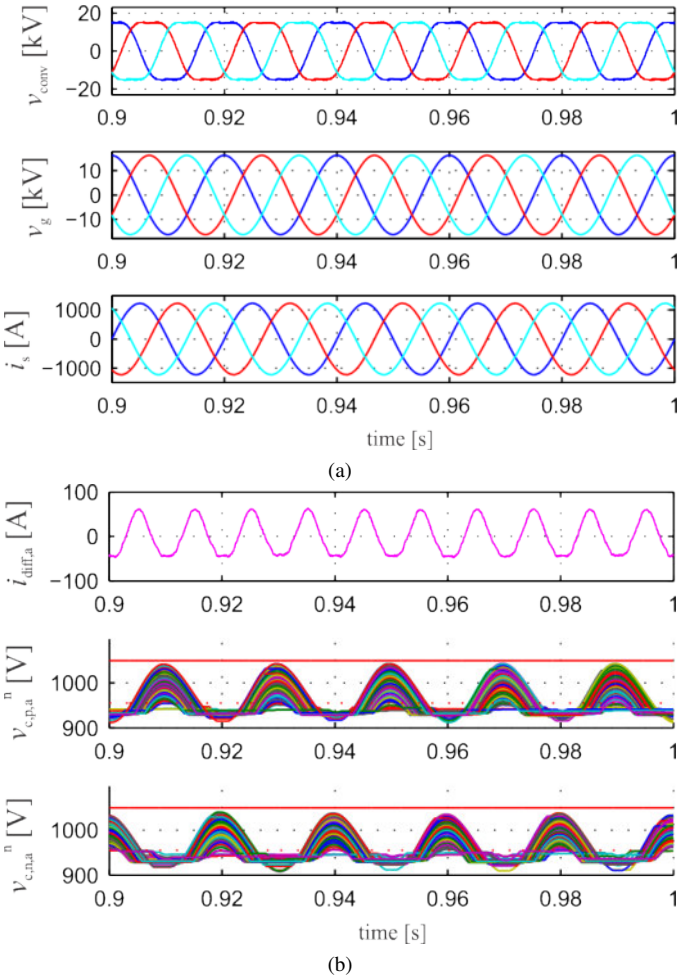



Figure 4: Standard balancing (study case I): a) Converter voltages, grid voltages and grid currents, b) Differential current and capacitor voltages (phase a).

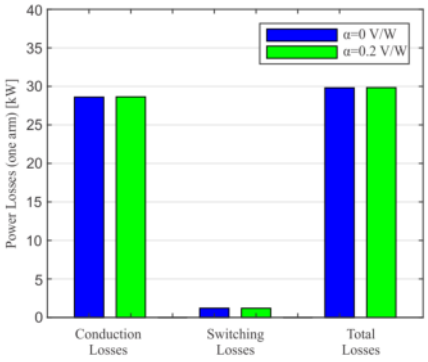
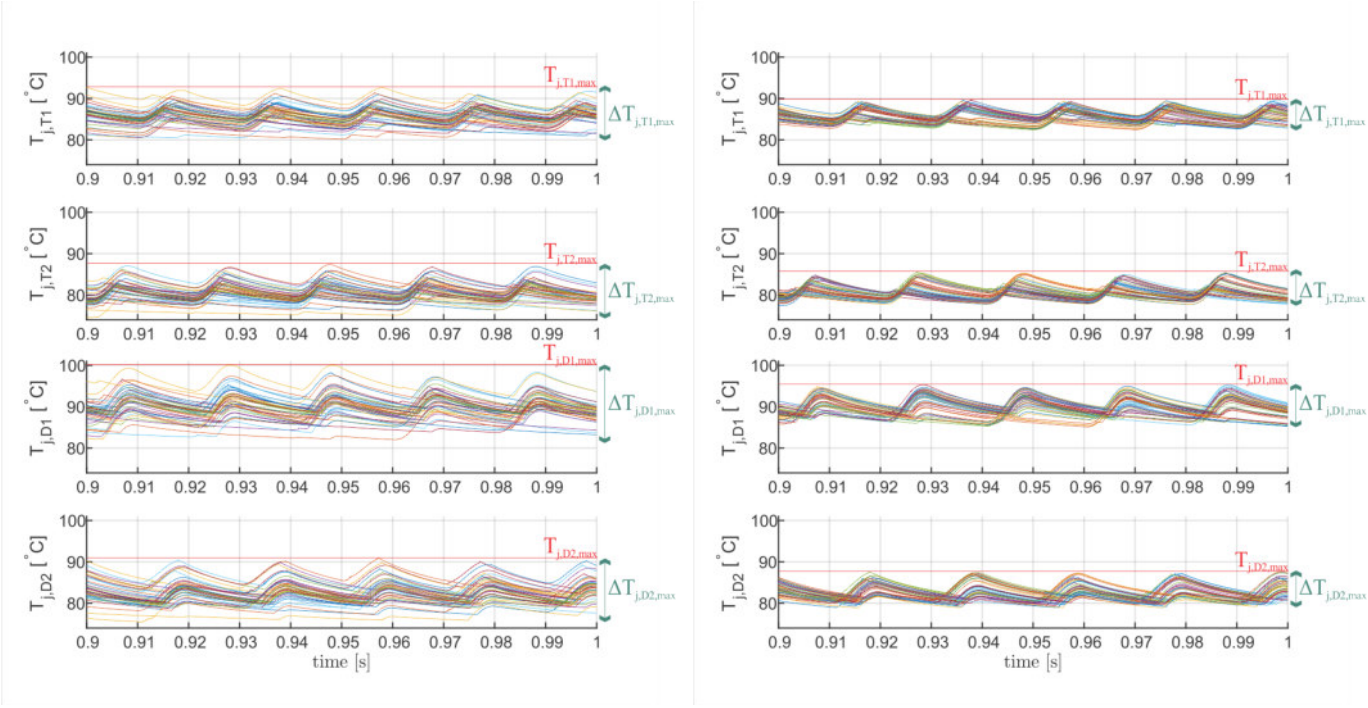
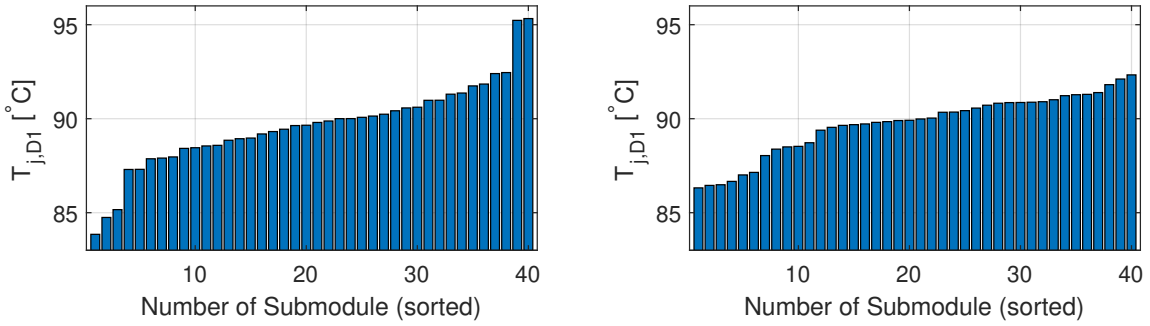



Figure 5: Semiconductor power losses (one arm) with standard balancing ($\alpha = 0$, study case I) and with advanced balancing ($\alpha = 0.2$, study case II).



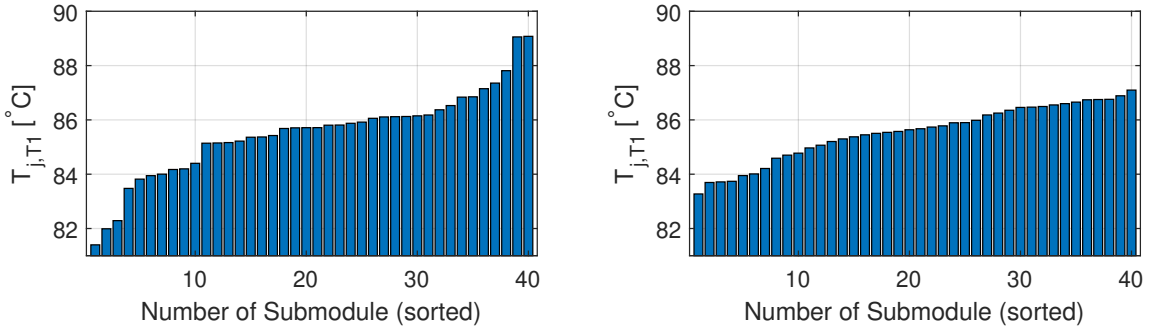

(a) (b)

Figure 6: Junction temp. (upper arm, phase a): a) Standard balancing (study case I), b) Advanced balancing (study case II).




(a) (b)

Figure 7: Distribution of time averaged (interval: 0.02 s) temperatures in $D_1$: a) Standard balancing (study case I), b) Advanced balancing (study case II).




(a) (b)

Figure 8: Distribution of time averaged (interval: 0.02 s) temperatures in $T_1$: a) Standard balancing (study case I), b) Advanced balancing (study case II).

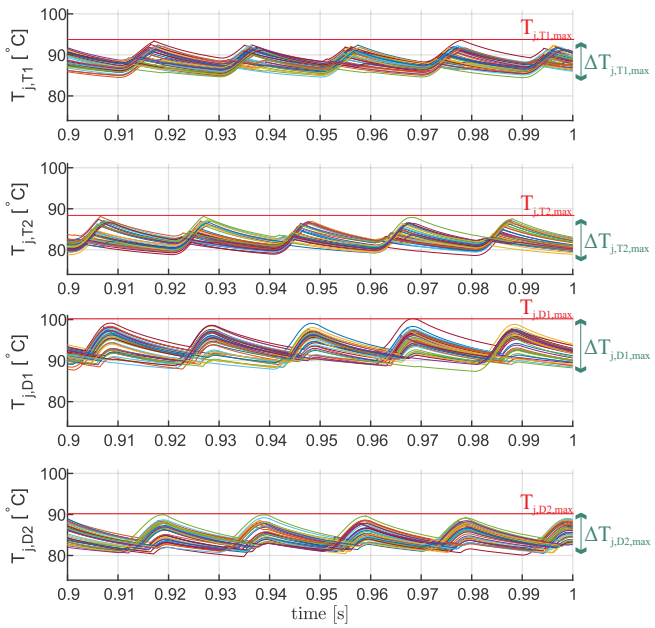



Figure 9: Advanced balancing with overrating (study case III): Thermal behavior (upper arm).

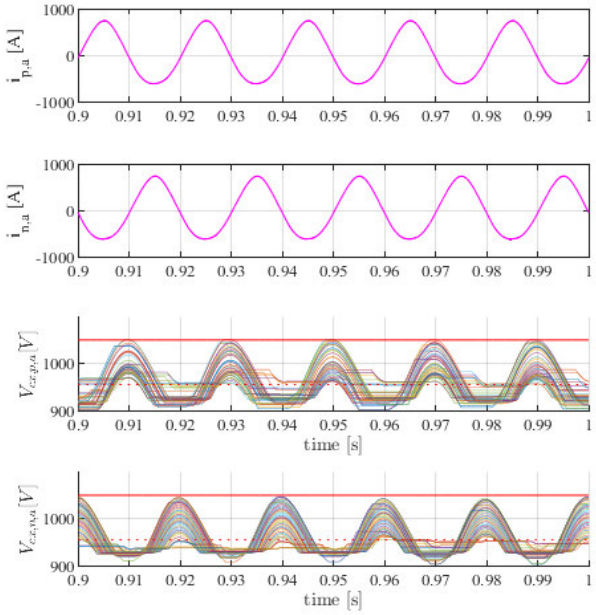



Figure 10: Advanced balancing with overrating (study case III): Electrical behavior (upper arm).

Since each SM needs to be designed for the worst case scenario, especially the significant reduction of maximum temperature is a huge benefit for a more efficient and economic converter design. Consequently, the reduced maximum junction temperatures by advanced balancing can be utilized for a higher current rating of the converter. This is further proven by study case III in Fig. 9 and 10, where the injected reactive current has been increased by 10 % without exceeding maximum temperatures of 100 °C. In order to reach the same capacitor voltage spread, the SM capacitance would need to be adapted to the selected power level, nevertheless additional costs for semiconductors have been completely eliminated by advanced balancing. Consequently, this means that the MMC rated for $S_g = 30\,\text{MVA}$ can be designed with significantly lower chip area or with a significantly smaller cooling system without affecting performance and efficiency of the converter.

The most important characteristic values of all three study cases are summarized in Table III. The spread of the junction temperatures with the advanced balancing (study case II) has been reduced by between unit[33]% and 44 % compared to standard balancing (study case I). The maximum junction temperatures are reduced up to 5 K, enabling a semiconductor current enhancement of at least 10 %, corresponding to additional 3 MVA (study case III) without exceeding the maximum temperatures. Despite of the 10 % increased power rating, the spread of the temperatures is still significantly reduced compared to the study case without the advance balancing (study case I).

Table III: Comparison of study cases: I) Standard design with standard balancing, II) Standard design with advanced balancing, III) Redesign with advanced balancing.

| **Study Case** | **I** | **II** | **III** |
|---|---|---|---|
| $S_g$ [MVA] | 30 | 30 | 33 |
| $\alpha$ [V/W] | 0 | 0.02 | 0.02 |
| $T_{j,T1,max}$[°C] | 92 | 90 | 94 |
| $T_{j,T2,max}$[°C] | 87 | 86 | 88 |
| $T_{j,D1,max}$[°C] | 100 | 95 | 100 |
| $T_{j,D2,max}$[°C] | 91 | 88 | 90 |
| $\Delta T_{j,T1}$[K] | 13 | 7 | 9 |
| $\Delta T_{j,T2}$[K] | 12 | 8 | 10 |
| $\Delta T_{j,D1}$[K] | 18 | 10 | 13 |
| $\Delta T_{j,D2}$[K] | 16 | 9 | 10 |

## V. Conclusion

An advanced SM balancing algorithm has been introduced for the MMC by taking into account not only the capacitor voltages but also the occurring semiconductor losses in each SM. It has been demonstrated that the stress distribution between the SMs can be strongly improved, leading to significantly reduced maximum junction temperatures. The more effective utilization of available chip area can be used either for a more economic semiconductor design or for a 10 % higher current capability, as demonstrated in this paper. The applied

advanced balancing does neither deteriorate the performance nor the efficiency of the converter. All these benefits have been achieved just by software implementation with limited computation effort, being easily applicable to other MMC applications.

## ACKNOWLEDGMENT

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