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***Abstract*—DC Solid-State Circuit Breakers (SSCB) play an important role in the protection of DC and hybrid AC/DC systems. As they operate mostly in on-state, the use of wide-bandgap devices, with low conduction losses, is an attractive solution. These devices need to be selected based on the rare occasion of fault breaking, with associated overcurrent and overvoltage intervals. In this work a novel clamping circuit, consisting in its simplified form of Metal-Oxide Varistors and capacitors, is proposed to be used in a DC SSCB. This circuit has the objective to reduce the breaker overvoltage during protection, enabling a lower number of required semiconductors in series and consequent overall reduced losses. An analysis of the idea and operation principle of the system is presented, alongside its stages of operation and defining equations. To evaluate its benefits, the system is compared with one typical passive solution. At the end a scaled prototype is tested, validating the benefits and theoretical analysis of the proposed approach.**

***Index Terms*—Solid-State Circuit Breaker, SSCB, Advanced Clamping Circuit**

I. Introduction

The penetration growth of DC grids due to its advantages relative to its AC counterpart, given by lower losses and costs, reduction of conversion stages and easier integration to renewables, has increased in applications that vary from very high power high voltage systems [1], medium voltage submarine and vessels [2], down to low voltage microgrids [3]. This type of technology demands more stringent control and faster protection solutions, since fault currents usually have faster rise time and can be more damaging, due to the lack of zero crossing and capacitive input and output connection of power electronic converters.

In traction and in the naval industry, for example, DC transmission and distribution is already a common and standardized topic [4], however as the distribution grid perceives an increasing penetration of power electronics, with support provided, for instance, to Battery Energy Storage Systems (BESS) [5], electric vehicles [6] and renewables in DC, the important figures of merit, such as protection response time and efficiency, are requiring improved and faster approaches to be utilized in the DC circuit breakers.

DC circuit breakers are mainly divided into three categories: Mechanical DC Circuit Breakers (MCB), Hybrid DC Circuit Breakers (HCB) and Solid-State DC Breakers (SSCB). An MCB consists basically of a common switch or a relay, where an electric arc between the contacts might occur while interrupting the current. Although common in low voltage applications, these breakers are unfeasible after a certain voltage level, as the energy absorbed by the arc would be too high. In an HCB a semiconductor switch parallels the mechanical switch/relay, providing either an auxiliary path for the current to break or a circuit that generates a resonance forcing the system to cross zero so that the mechanical part can be safely open. Both these solutions require a mechanical circuit to eliminate the fault. The SSCB utilizes semiconductors in the main path to break the current and can also be associated with a mechanical switch to ensure galvanic isolation between the parts. As is consists of a fully semiconductor based protection approach, it is orders of magnitude faster then its electromechanical counterparts [7].

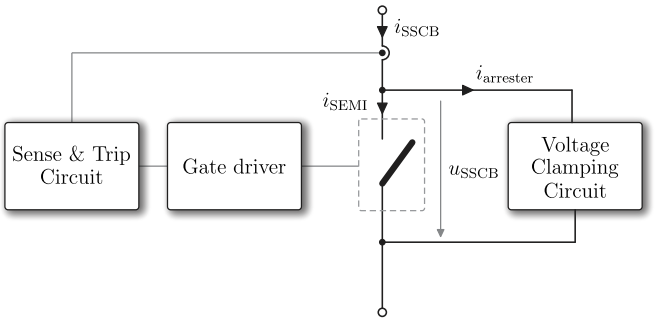

Fig. 1: General fault current clearing scheme of circuit breakers.

A generic Solid-State Circuit Breaker (SSCB) is presented in Fig. 1. On it, four main components are observed: sense and tripping circuit, gate driver, main current path and clamping circuit. The sense and tripping circuit is responsible for the detection and signaling of the fault. The driver circuit's main function is to control the states of the power semiconductor, but can also have additional features, such as fault sensing [8], current and voltage rise time control [9] and multiple device voltage blocking sharing capability [10]. The voltage clamping circuit, object of focus on this work, serves as both

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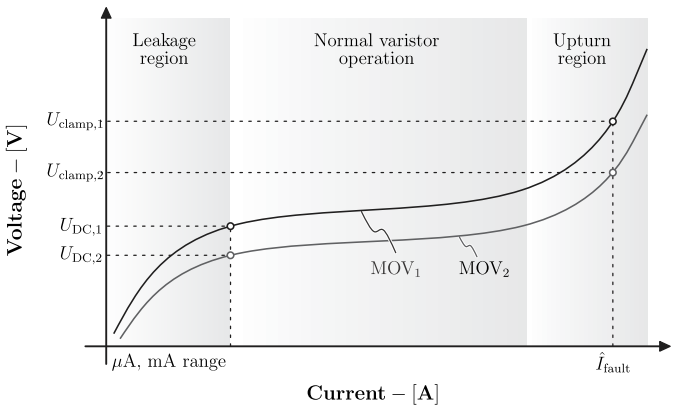


Fig. 2: MOV voltage x current curve.

an energy absorption and overvoltage protection mechanism. For this, the most basic approach is the use of a Metal-Oxide Varistor (MOV) to limit the overvoltage of the main path. The fundamental principle is based on the change of the resistance as a function of the applied voltage, as depicted in Fig. 2. When exposed to high voltage transient the varistor impedance changes from a near open circuit to a very low resistive path. The curve can be divided into three main sections, namely:

- **Leakage current region**: where the MOV acts as a large resistor and has a high resistance, appearing as an open circuit;
- **Normal varistor operation region**: acts as a conductor, conducting large amount of current for a small increase in voltage, approaching a short circuit;
- **Upturn region**: where the surge clamping function occurs, where the device operates similar to a short circuit.

This paper uses the characteristics of the MOV selection to propose a clamping circuit that allows for a lower overvoltage in the semiconductors of the main path, therefore the required number of devices in series, reducing system's losses and cost. In Section II the operating principle of the circuit is described, along with its main stages of operation and equations. Section III deals with the design intrinsic characteristics and trade-offs, providing a comparison between theoretically obtained and simulation results and Section IV shows the experimental validation in a reduced scale prototype.

II. Advanced Clamping Circuit - ACCT

One major factor affecting the cost, efficiency and sizing of the SSCB is the required number of semiconductors in the main path, which has to be clearly selected based on the transient characteristics of the breaking curve. The total number of semiconductors in series in a SSCB is given by

$$N_{\text{S}} = \left\lceil \frac{U_{\text{overvoltage}}}{U_{\text{DS/CE,max}} \cdot k_{\text{SOA}}} \right\rceil \tag{1}$$

where $\lceil x \rceil$ stands for the highest integer near x, $U_{\text{overvoltage}}$ the surge voltage, $U_{\text{DS/CE,max}}$ the rated peak allowable voltage in the device and k_{SOA} a safety switching margin.

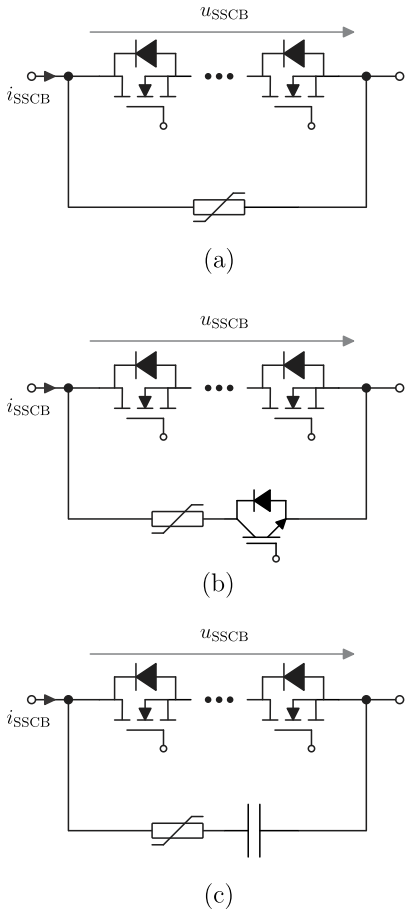


Fig. 3: Clamping methods using MOV: (a) Simple approach with MOV in parallel to main path, (b) AACC with the IGBT blocking partially the MOV DC voltage and (c) APCC with capacitor blocking partially the MOV DC voltage.

The most common MOV-based clamping approach relies on utilizing it directly in parallel with the main path (c.f. Fig. 3(a)). Once the semiconductors are opened the current follows a curve similar to one of the presented in Fig. 2, where the highest voltage that appears across the semiconductors U_{clamp} relates to the peak fault current $\hat{I}_{\text{fault}}$ when the MOV is in the upturn region. Here the selection of the varistor is a bit intricate, as it is important to choose one that will result in the lowest U_{clamp}, while still with a high DC blocking voltage, so that the fault is completely settled, i.e. the MOV DC voltage needs to be higher than the applied DC voltage of the system $U_{\text{DC,MOV}} > U_{\text{DC}}$.

A. Advanced Active Clamping Circuit - AACC

With the objective to use a lower DC rated MOV for higher voltage, with consequent lower overshoot, an auxiliary path circuit using the combination of the varistor and an active semiconductor was proposed in [13], here designated as Active Advanced Clamping Circuit (AACC). This is depicted in Fig. 3(b). In this case, the IGBT in the auxiliary path supports the voltage along with the MOV and as it only participates of

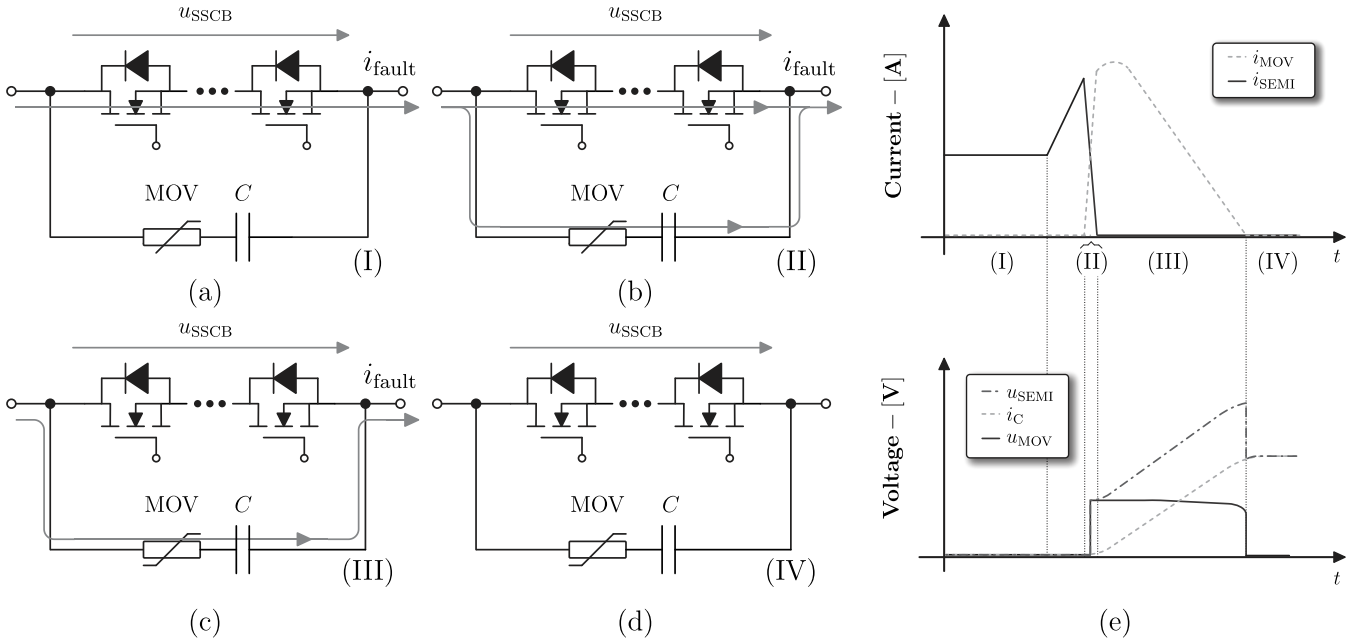


Fig. 4: General fault current clearing scheme of circuit breakers.

the conduction during the fault interruption, it does not affect the system efficiency.

B. Advanced Passive Clamping Circuit - APCC

To overcome some disadvantages observed in the AACC, the Advanced Passive Clamping Circuit (APCC) is proposed in this work (c.f. Fig. 3(c)). A capacitor bank is responsible for sharing the voltage with the MOV after the fault, replacing the role assumed by the IGBT in the case of Fig. 3(b). With this replacement, the auxiliary circuit becomes completely passive, reducing concerns related to driver circuits, fault detection for the auxiliary circuit and isolation requirements. On the other hand, this case demands a more thorough knowledge of the grid and fault worst case scenario, as there is no active stage.

C. APCC Principle of Operation

The stages of operation of the APCC can be divided in four, shown in Fig. 4 along with the expected voltage and current wave forms.

1) STAGE (I): : In the normal mode of operation the main path, represented by the combination of MOSFETs, is turned on and conducting the load current (c.f. Fig. 4(a)). Here the system obeys the equation for the voltage drop in the semiconductors combination

$$U_{\mathrm{SSCB}} = R_{\mathrm{DS,on,eq}} \cdot i_{\mathrm{Load}} \tag{2}$$

with $R_{\mathrm{DS,on,eq}}$ is the equivalent on-state resistance of the semiconductors assembly.

2) STAGE (II): : The main path conducts until a short circuit occurs. When the limit current is reached and the circuit is triggered the MOSFETs start to turn off and the load interchanges from the semiconductor to the path containing the MOV, as it is shown in Fig. 4(b).

3) STAGE (III): : When the main path is completely turned off the fault equation will obey the dynamics of the differential equation given by the system inductance, the MOV resistance, which is non-linear, and the capacitor. Once the fault clearing process starts:

$$U_{\mathrm{DC}} = u_{\mathrm{MOV}} + u_{\mathrm{C}} + u_{\mathrm{Rsc}} + u_{\mathrm{Lsc}}, \tag{3}$$

with R_{SC} and L_{SC} representing the short circuit resistance and inductance. Considering that during this interval the current is flowing through the clamping capacitor, then its voltage is calculated through:

$$U_{\mathrm{DC}} = K\left(C\,\frac{\mathrm{d}u_{\mathrm{C}}}{\mathrm{d}t}\right)^{\beta} + u_{\mathrm{C}} + R_{\mathrm{SC}}C\,\frac{\mathrm{d}u_{\mathrm{C}}}{\mathrm{d}t} + L_{\mathrm{SC}}C\,\frac{\mathrm{d}^2u_{\mathrm{C}}}{\mathrm{d}t^2} \tag{4}$$

where K and β are parameters that depend on the MOV selection [14]. The SSCB voltage during this interval is

$$u_{\mathrm{SSCB}} = u_{\mathrm{MOV}} + u_{\mathrm{C}} \tag{5}$$

Here it is important to mention one specific characteristic of the APCC: as the circuit obey (4), the peak current will no longer be given by the triggered opened current $\hat{I}_{\mathrm{fault}}$, but later, as depicted in Fig. 4(e).

4) STAGE (IV): : This interval begins once the fault current reaches zero. By then, the capacitor is charged to its final value and the MOV will have a DC voltage that is the difference of the supply and the capacitor, i.e.,

$$U_{\mathrm{DC,MOV}} = U_{\mathrm{DC}} - U_{\mathrm{C}} \tag{6}$$

III. Design Characteristics

A. Overvoltage x fault extinguishing trade-off

To validate the idea a SSCB was simulated with the parameters as shown in TABLE I. The main decision factor for the

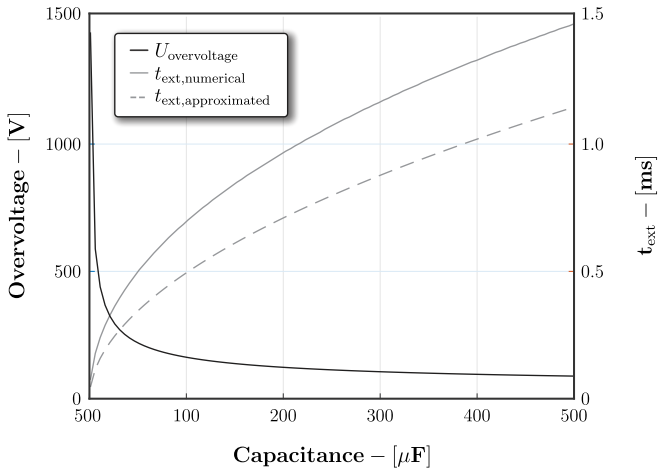


Fig. 5: Clamping methods using MOV: (a) Simple approach with MOV in parallel to main path, (b) AACC with the IGBT blocking partially the MOV DC voltage and (c) APCC with capacitor blocking partially the MOV DC voltage.

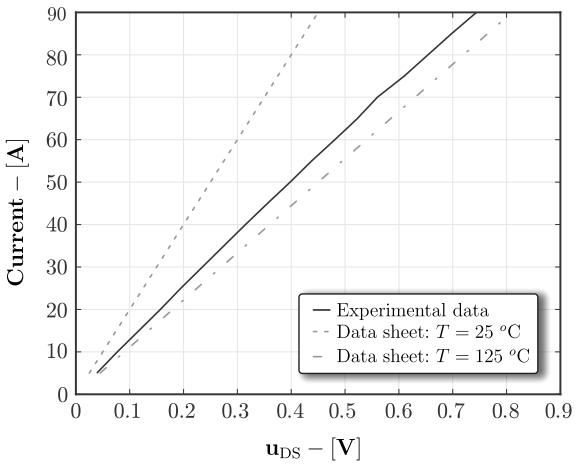


Fig. 6: Experimental characterization and data sheet curves of of the SiC power module DP200B1200N100749 in the tested setup.

design is the selection of the clamping capacitance, as it finally defines both the overvoltage and extinguishing time. Based on (3), (4) and (5) the relation can be numerically derived and the results are shown in Fig. 5. The fault extinguishing time is also compared with the simplified approximation as considered in [12] that disregards the non-linear behavior of the MOV and assumes the current falling to be linear, as in

$$t_{\text{ext,approx}} = \frac{L}{U_{\text{L}}} \cdot \hat{I}_{\text{fault}} = \frac{L_{\text{SC}}}{U_{\text{clamp}} - U_{\text{DC}}} \cdot \hat{I}_{\text{fault}} \quad (7)$$

that, as can be seen, will underestimate the value. In order to validate the numerical derivations, three simulations were realized containing both the common approach, with the MOV in parallel, and with the APCC. This second case was tested for lower and higher values of capacitance. These results are summarized in TABLE I. There, the numerically predicted extinguishing time $t_{\text{ext,pred.}}$ and overvoltage U_{pred} are compared with the ones obtained via simulation.

As Fig. 5 shows, there is a trade-off between fault extinguishing time and overvoltage seen in the semiconductors, therefore two different design approaches for the APCC were considered. In the first, the capacitance is selected in order to obtain approximately the same extinguishing time as in the typical case, to observe the increase in overvoltage. With $C = 60\,\text{nF}$, with t_{ext} increases $20\,\text{ns}$ over the typical solution. The overvoltage rises from $2.1\,\text{kV}$ up to $2.9\,\text{kV}$, a 38% increase.

In the second case, the capacitance is optimized to reduce the overvoltage in the semiconductors. For the study case, the SiC device DP200B1200N100749 from Danfoss Silicon Power is selected, with $U_{\text{DS,max}} = 1.3\,\text{kV}$ and an on-state resistance of $5\,\text{m}\Omega$. In this case the overvoltage is reduced down to $1.6\,\text{kV}$ with a consequent increase in t_{ext} to $694\,\text{ns}$.

TABLE I: Simulation parameters

Parameter	Symbol	Value
Applied DC Voltage	$U_{\text{DC,test}}$	1 kV
Nominal current	I_{nom}	200 A
Short circuit inductance	R_{SC}	10 mΩ
Short circuit inductance	L_{SC}	15 mH
Regular MOV	Varsi V480D100	
Reduced voltage MOV	Littelfuse TMOV34S141MP	

B. Loss reduction

The designed reduction in the overvoltage across the main semiconductor path causes a reduction in the required number of switches and consequent efficiency improvement in the system. For the considered case study, allowing for a safety operating margin of 70% ($k_{\text{SOA}} = 0.7$) the number of semiconductor devices before the APCC was

$$N_{\text{S}} = \left\lceil \frac{2.1\,\text{kV}}{1.3\,\text{kV} \cdot 0.7} \right\rceil = 3 \quad (8)$$

and in the case where the APCC is being applied

$$N'_{\text{S}} = \left\lceil \frac{1.6\,\text{kV}}{1.3\,\text{kV} \cdot 0.7} \right\rceil = 2 \quad (9)$$

To assess the percentage losses improvement the device DP200B1200N100749 was characterized experimentally, in

TABLE II: Simulation comparison for the cases of the MOV in parallel to the semiconductor path, using the APCC with 60 nF and with 840 nF.

Clamping type	$t_{\text{ext,pred.}}$	$t_{\text{ext,sim.}}$	$U_{\text{pred.}}$	$U_{\text{sim.}}$
MOV in parallel	140.8 ns	140.0 ns	2.1 kV	2.1 kV
APCC, $C = 60\,\text{nF}$	143.9 ns	157.1 ns	2.9 kV	3.0 kV
APCC, $C = 840\,\text{nF}$	694.5 ns	695.0 ns	1.6 kV	1.6 kV

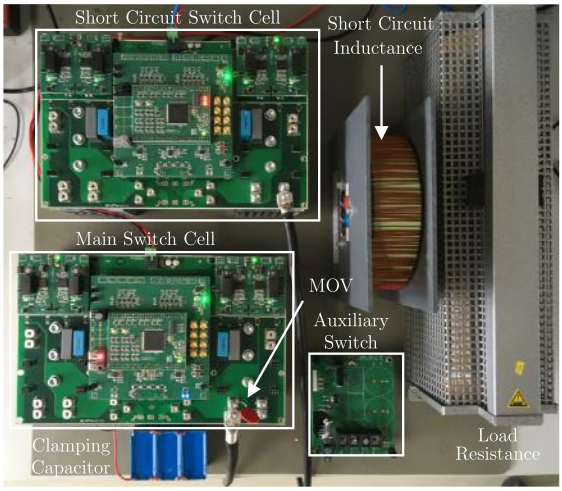


Fig. 7: Implemented experimental set up with main compo-nents highlighted.

the utilized prototype. As switching losses are negligible only the conduction was mapped, as depicted in Fig. 6. The generic loss equation for N_{S} series and N_{P} parallel connected SiC MOSFET devices under a constant load is

$$P_{\mathrm{loss}} = \frac{N_{\mathrm{S}}}{N_{\mathrm{P}}} \cdot R_{\mathrm{DS,on}} \cdot i_{\mathrm{Load}}^2 \tag{10}$$

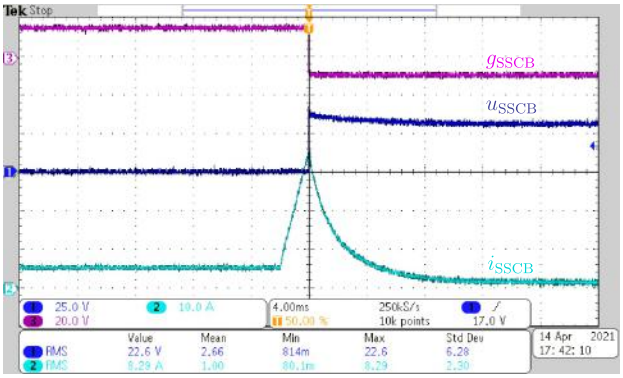
where $R_{\mathrm{DS,on}}$ is obtained from Fig. 6. In the analyzed case the overall losses are reduced from 600 W to 400 W, a 33% reduction. It is important to mention at this point that a scalable relation is not directly found, as the overvoltage reduction depends heavily on the non-linear behavior of the MOV and its selection. In case of higher voltage systems, however, it is not uncommon to see modular solutions where several identical modules are connected to meet the requirements in voltage and current [15]. The loss reduction has two direct consequences on the physical size of the system: the first is in respect of the semiconductor devices themselves and the second is of the reduction of the thermal system.

IV. Experimental Results

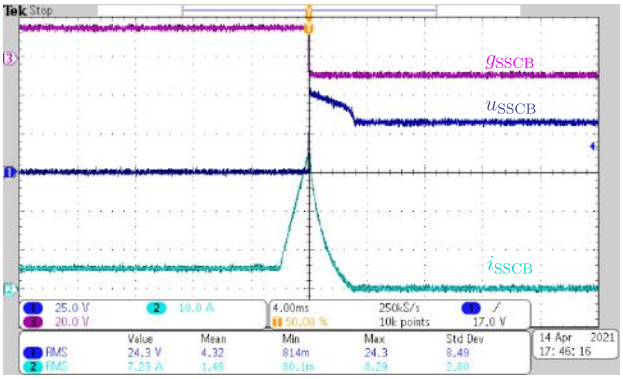
In order to evaluate the breaker performance experimentally and verify the design procedure, a scaled down setup was build and tested, as shown in Fig 7. The main specifications are shown in TABLE III.

TABLE III: Experimental parameters

Parameter	**Symbol**	**Value**
Applied DC Voltage	$U_{\mathrm{DC,test}}$	32.5 V
Nominal current	I_{nom}	5 A
Short circuit resistance	R_{SC}	19.1 mΩ
Short circuit inductance	L_{SC}	2.2 mH
Clamping capacitance	C	90 μF
Regular MOV	Littelfuse V33ZA70P	
Reduced voltage MOV	Littelfuse V20E14P	



(a)



(b)

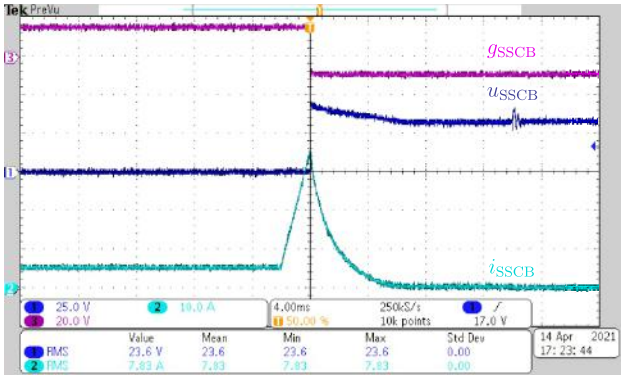
Fig. 8: Experimental test of the behavior of using a (a) lower DC rated MOV (V20E14P) and a (b) higher DC rated MOV (V33ZA70P).

To exemplify the problem with utilizing a lower DC rated MOV in parallel with the semiconductors, two tests were realized considering a test voltage of $U_{\mathrm{DC,test}} = 32.5\,\mathrm{V}$. The results are illustrated in Fig. 8. In the first case, Fig. 8(a), after the main path is opened the MOV remains conducting a current of 2.5 A. In the second, with higher rated voltage, the typical overvoltage curve generated by the MOV is visible across the terminals of the semiconductor. There, the varistor blocks the complete current after breaking the fault.

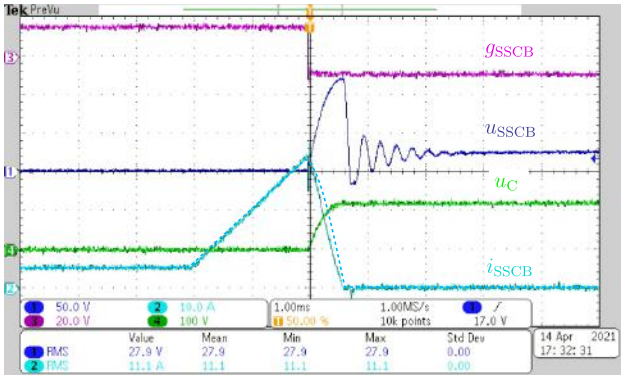
The active and passive clamping circuit operation are demonstrated in Fig. 9. In the first case the auxiliary semiconductor is opened 20 ms after the fault, as it can be seen with the small overvoltage in u_{SSCB}. For higher voltage cases, this value might reach an overshoot higher than the one handled in the fault breaking, damaging the system. In the passive case this is not seen as there is no active current breaking device, the current is extinguished naturally with the capacitor charging.

In the last case, due to the available devices, the focus was on reducing t_{ext} from around $1\,\mathrm{ms}$ to approximately $500\,\mu\mathrm{s}$, hence increasing the overvoltage in the SSCB. Here, it should be noted that even though the system presents a high overvoltage the feasibility of using a lower rated MOV is still seen, since the capacitor voltage is charged to its steady state

value. The blue dashed line shows the theoretically calculated behavior, therefore showing a near perfect estimation and design.



(c)



(d)

Fig. 9: Experimental test of the behavior of the (a) AACC and the (b) APCC. The dashed light blue line depicts the theoretical predicted behavior.

V. Conclusion

In this paper a new clamping circuit, denominated Advanced Passive Clamping Circuit (APCC) was proposed to reduce the clamped overvoltage appearing in a DC solid state circuit breaker during the fault handling process. The improved clamping characteristic allows for a reduction of the number of the series connected devices that are constantly on during regular operation. This reduction positively affects the system efficiency, size and thermal design.

In comparison to similar ideas the proposed solution is composed of only passive components, not requiring any extra driving circuit or additional concerns with isolation. In turn, since the system has no active controllability, it requires a deeper knowledge of the grid characteristics to which the system is connected to, as the fault breaking behavior relies solely on the design of the passive components involved.

Once the idea was presented and the important trade-offs described, a case study for a 1 kV/200 A system showed that the APCC can reduce the losses by 33%, which would consequently reduce overall costs with device and thermal circuitry. Finally, the experimental results showed the feasibility and validated the theoretical derivations of the proposed clamping approach.

Acknowledgment

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