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Polishing of Hard Machining Semiconductor Materials Made of Silicon Carbide

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In the paper the application of silicon carbide (SiC) in electronics especially for production of p–i–n diodes have been shown. Also the technology of honing process of samples made of silicon carbide using grinding, lapping and polishing method has been presented. Finally the process of machining and the stand for surface preparation, selected investigation results concerning assessment of geometrical microstructure and morphology of SiC samples surface layer after machining process have been depicted.

Keywords: Silicon carbide, grinding, lapping, polishing, microstructure, morphology, surface layer, semiconductor, SiC–pin diode

1. Introduction

Whereas polymers are highly visible engineering materials with a major impact on contemporary society, semiconductors are relatively invisible but have a comparable social impact. Technology has clearly revolutionized society, but solid–state electronics is revolutionizing technology itself. A relatively small group of elements and compounds has an important electrical property, semi–conduction , in which they are neither good electrical conductors nor good electrical insulators. Instead, their ability to conduct electricity is intermediate. These materials are called semiconductors [1]. Silicon carbide (SiC) is semicondustor material of a unique and very attractive phisical and electrical properties. They make possibility to manufacture devices which are characterized by so far unattainable parameters or difficult to obtain [2–6]. High critical breakdown field intensity allows to manufacture high voltage junctions of breakdown voltages exceeded 10 kV [7]. High energetic gap causes that from SiC it is possible to manufacture low-noice semiconductor devices, which working temperature can reach values exceeded 700°C [8], like also manufacture so–called. "blue optoelectronic" devices [9]. High drift velocity of electrons causes that on base of SiC it is possible to manufacturing high frequency devices of frequency reaching THz [10]. Good thermal conductivity is in turn important in point of view of reliability (thermal stresses) and problems with heat removal [11]. The main drawback in practical use of silicon carbide in electronics is extreme requirements concerning technological processes regarding to this material, comparing to silcon. It causes that technological processes and methods of characteristics, which are well known and mastered for silicon, are in this case inapplicable or inadequte for new requirements.

One of the critical technological processes of silicon carbide is the doping technology of this material. The thermal diffusion technology has been used on a large scale in silicon technology for winning of areas of a complex type and dope for many years. This is the simplest method ensuring complete electrical activation of introduced dope, what causes that it could be very attractive in applications basing on silicon carbide, ie. for production of the p–i–n diodes. Unfortunately it meets the serious problems. Main of them is the fact, that for effective process run of dope diffusion in silicon carbide it is necessary to lead it in temperatures exceeded 1800^{o}C. It can cause degradation of surface layer of SiC crystal. Because of this a number of trials of application of diffusion technology for needs of SiC has been marginal and obtained effects have been so far unsatisfactory. The lack of such a technology for SiC is one of main elements affecting on still small presence of devices made of SiC on the market of semiconductor devices.

The structure of of the p–i–n diode manufactured on SiC substrate with application of thermal technology of dope diffusion of P type has been presented in figure 1 and the view of diodes has been depicted in figure 2. A p–i–n diode is a fast low capacitance switching diode. A p–i–n diode is manufactured like a silicon switching diode with an intrinsic region added between the p–n junction layers. This yields a thicker depletion region, the insulating layer at the junction of a reverse biased diode. This results in lower capacitance than a reverse biased switching diode.

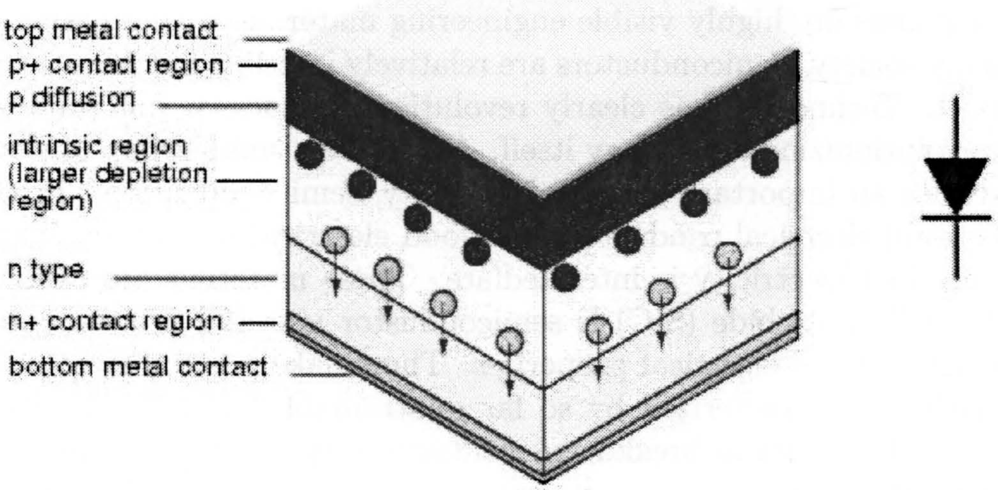

Figure 1 Exemplary construction of SiC p–i–n diodes with application of dope diffusion for obtaining p^+ area (cross section aligned with schematic symbol) [12]

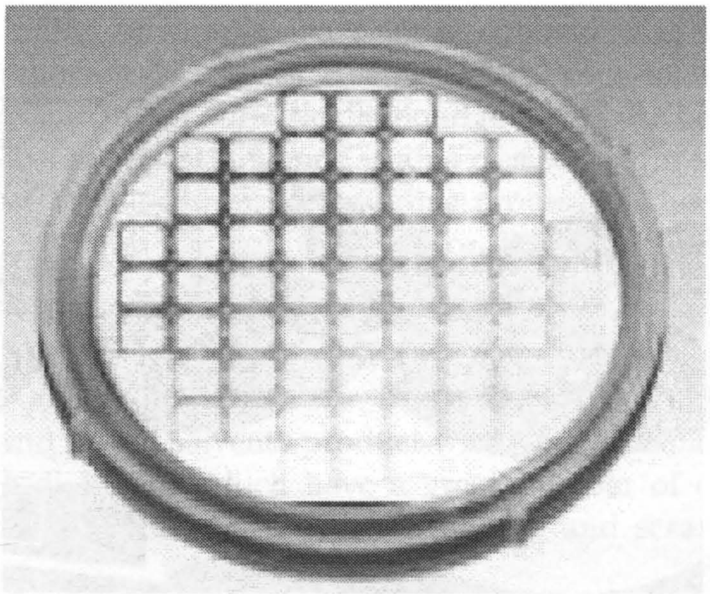

Figure 2 The view of SiC– p–i–n diodes; 4x4mm devices on a 2-inch wafer [13]

The restoration of low roughness of surface layer of SiC samples in order to performance of anode contact and to remove layer of a few microns from the underneath side of substrate, in order to performance of cathode contact after thermal diffusion processes, is one of substantial conditions of control of technology of manufacturing such a structure.

In regard of high hardness (over 9 in Mohs hardness scale) and high chemical resistance of silicon carbide these aims can be achieved by using machining technology. In this situation only one possibility is application of mechanical grinding and polishing technology using diamond suspensions of different grain sizes.

2. The stand for preparation of surface layer of structures made of silicon carbide

Preparation process of samples made of silicon carbide has been carried out using Phoenix Beta 2 (Buehler–Germany) dual platen grinder-polisher machine equiped with Vector power head (Fig. 3) and specimen holder for single force for 3-6 specimens up to max ø 25 mm, according to holder selected (Fig. 4a). Thus 3 to 6 specimens can be prepared under reproducible conditions. The Buehler grinder–polisher machine has stepless rotation speed (from 30 to 600 rpm) and the power head has settings of control time, preassure (up to 200 N), speed and direction and automatic start and stop system. Vector power head upgrades the Beta 2 grinder-polisher machine to from manual operation to semi–automatic operation, increasing productivity and specimen consistency. This stand is on equipment of Department of Production Engineering of Technical University of Lodz laboratory [14–16]. The SiC samples have been plastered to the steel discs of diameter ø 25 mm using resin (Fig. 4b).

Figure 3 The overall view of the Beta 2 dual platen grinder–polisher machine equipped with Vector power head and specimens holder

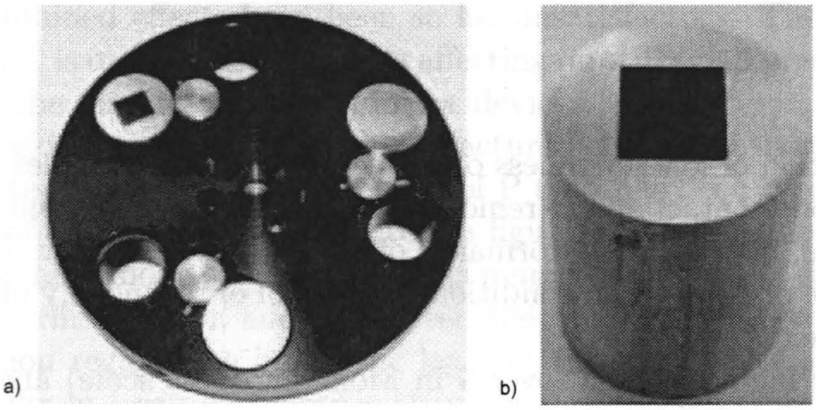

Figure 4 View of the specimens holder (a) and SiC sample plastered to the steel disc (b)

3. Technological process of grinding and polishing of samples made of silicon carbide

The samples made of silicon carbide of dimension 20 x 20 mm and thickness 0,5 mm have been used for investigations. The technological assumption was to remove SiC layer of a few microns from one of the sample surface and simultanously not to damage the other side. In thi purpose the Buehler Canadian Balsam resin has been used in order to glue the SiC sample to steel discs. This rasin is natural and inactive product. It hardens and is easily to removable after its heating to temperature 120^{o}C. The main technological requirement of technological process was to prepare samples of a low surface roughness and removal impurities from their surface layer. For this purpose the technological process of abrasive machining including following grinding and polishing operations has been elaborated [14]:

- two stage grinding of samples on grinder equiped with self adhesive metal bonded diamond abrasive discs Buehler UltraPrep; in sequential stages of grinding the granuality of abrasive diamond material has been diversified using accordingly: in first stage diamond grains of size 74 μm and in second stage diamond grains of size 40 μm; the grinding process has been carried out using polishing extender (no alcohol lubricant for diamond) Buehler MetaDiFluid
- two stage lapping of samples using self–adhesive lapping cloths Buehler Tri-Dent (medium hard to soft synthetic silk) and Buehler MetaDi Supreme diamond paste of diamond grain size 9 μm and 3 μm; MetaDi Supreme is a water-based and free of solvents product with high concentration of synthetic, polycrystaline diamonds which have a great number of cutting faces. This offers a particulary high material removal rate and scratch–free surfaces of samples.
- polishing of samples using self–adhesive polishing cloths Buehler Nylon (medium hard woven nylon cloth) and Buehler MiroMet Cerium Oxide (CeO) suspension of grain size 1 μm;
- washing of samples in ethyl alcohol of high purity (99,9 %) Chem Land using ultrasonic washer Polsonic – Sonic 1.

The technological conditions of realized operations of grinding and polishing of SiC samples have been shown in Tab. 1.

4. Experimental investigations

Experimental investigations have contained determination of technological conditions of realized grinding, lapping and polishing operations of silicon carbide surface samples, measurement of geometrical microstructure and estimation of morphology of SiC surface layer in 2D and 3D configuration.

4.1. *Determination of geometrical microstructure of SiC surface layer*

Presented investigation results concern comparison of geometrical microstructure parameters of SiC surface layer after each stage of its preparation. Geometrical microstructure of SiC surface has been estimated basing on roughness and waviness parameters of surface in 2D and 3D configuration. The profile measurements have been carried out in Department of Production Engineering of Technical University of Łódź–Poland laboratory, using profilometer type PGM–1C IOS. Measurements have been carried out under following conditions: measurement range 25 μm, $L = 0,8$ mm, $v = 0,2$ mm/s, $L_M = 1,25\mu$m. Exemplary profile measurements results of SiC samples in 2D configuration have been presented in Figs 5–7, however in 3D configuration in Figs 8–10. The values of roughness and waviness parameters of samples surfaces have been placed in suitable profilograms and have referred to their average value from five tests of profile measurement. Roughness parameters analysis of investigated samples in 2D configuration (Figs 5–7) has shown significant decrease of roughness of SiC samples surfaces after each stage of machining. After grinding process SiC surface roughness Ra has been equal to 0,10 and Rz equal to 0,72, while after polishing Ra has been equal to 0,02 and Rz equal to 0,20. Also decrease of waviness parameters in 2D configuration has been visible. After grinding process SiC surface waviness Wt has been equal to 0,30 and Wa equal to 0,07, while after polishing Wt has been equal to 0,09 and Wa equal to 0,02. The same situation has been observed in comparison of SiC surface roughness and waviness parameters in 3D configuration (Figs 8–10). After grinding process SiC surface roughness Ra has been equal to 0,09 and Wa equal to 0,08, while after polishing Ra has been equal to 0,03 and Wa equal to 0,03. Moreover it has been certified that after polishing process SiC surface layer has had no visible scratches and had glossy color.

Table 1 Conditions of technological process of SiC samples preparation

Process stages	Abrasive surface	Type of abrasive material	Lubricant type	Process time [min]	Feed force [N/cm^2]	Rotation speed of platen V [m/s]
Grinding of sample surface	Diamond abrasive disc UltraPrep	Diamond (grains of ø 125μm)	Monocrystalline diamond suspension Buehler MetaDi Fluid	5	10	6
	Diamond abrasive disc UltrPrep	Diamond (grains of ø 40μm)	Monocrystalline diamond suspension Buehler MetaDi Fluid	3	5	6
Lapping	Lapping cloth TriDent	Polycrystalline diamond (grains of ø 9μm)	Polycrystalline diamond suspension Buehler MetaDi Supreme	5	3	3
	Lapping cloth TriDent	Polycrystalline diamond (grains of ø 3μm)	Polycrystalline diamond suspension Buehler MetaDi Supreme	3	3	3
Polishing	Polishing cloth Nylon	Buehler MiroMet Cerium Oxide (CeO) suspension (1μm)	–	3	2	3

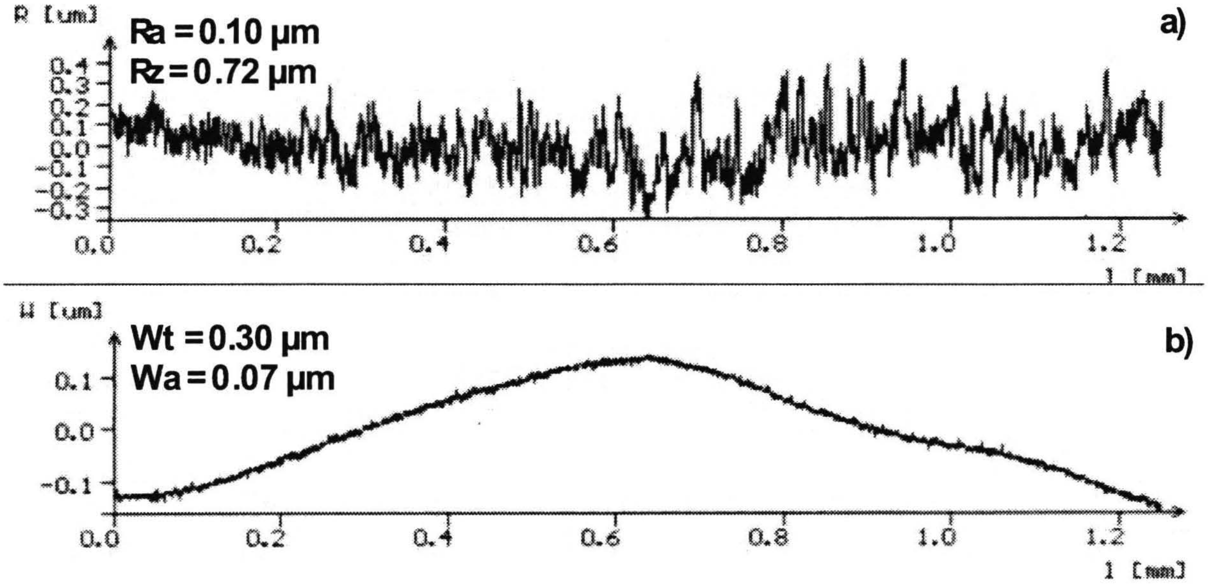

Figure 5 Profilograms of roughness (a) and waviness (b) in 2D configuration of SiC surface after grinding process (using diamond grains of ø 40 μm)

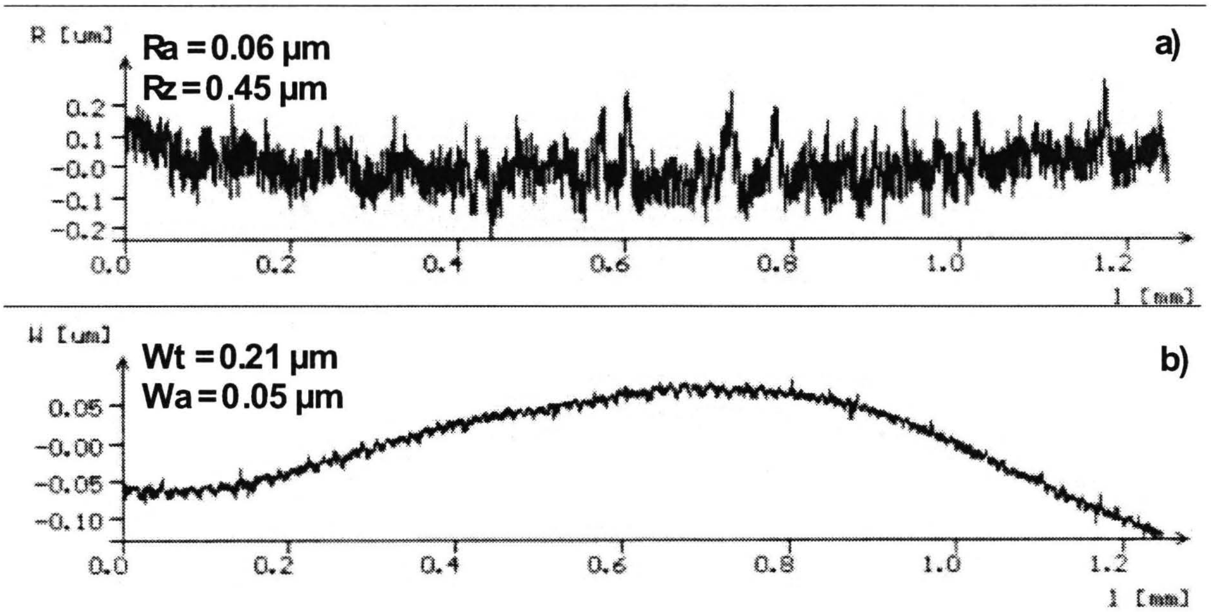

Figure 6 Profilograms of roughness (a) and waviness (b) in 2D configuration of SiC surface after lapping process (using polycrystalline diamond grains of ø 9 μm)

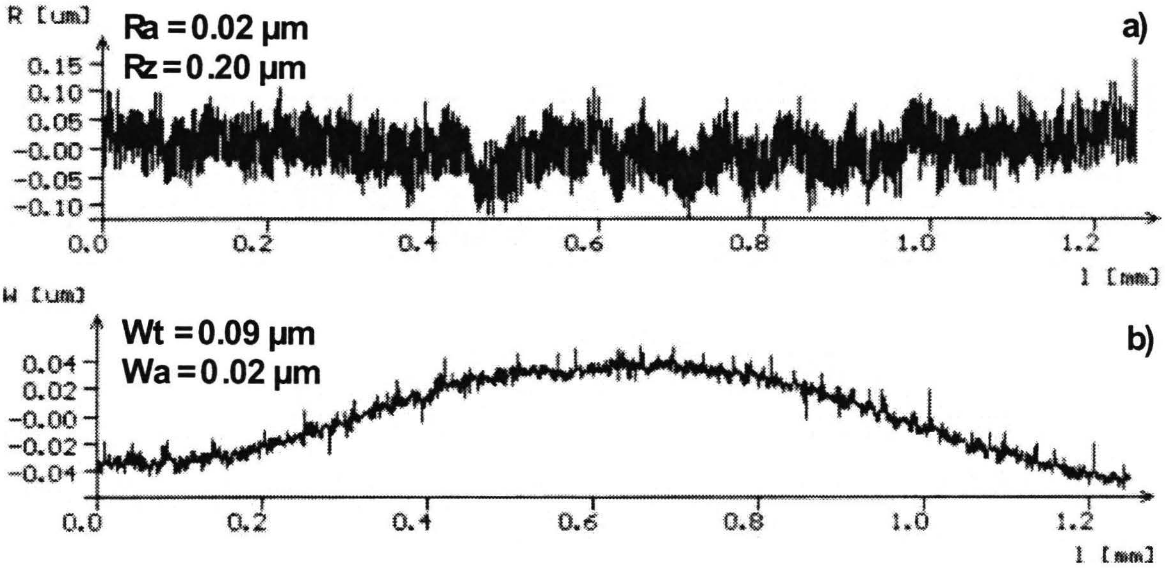

Figure 7 Profilograms of roughness (a) and waviness (b) in 2D configuration of SiC surface after polishing process (using cerium oxide grains of ø 1 μm)

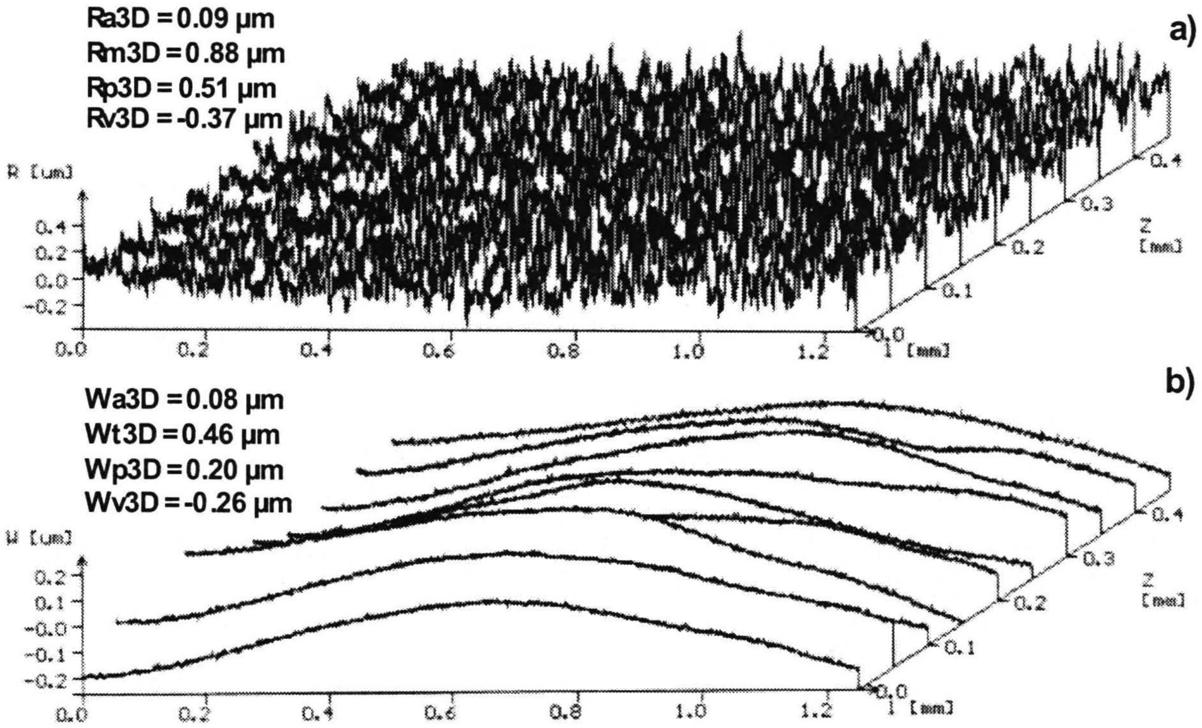

Figure 8 Profilograms of roughness (a) and waviness (b) in 3D configuration of SiC surface after grinding process (using diamond grains of ø 40 μm)

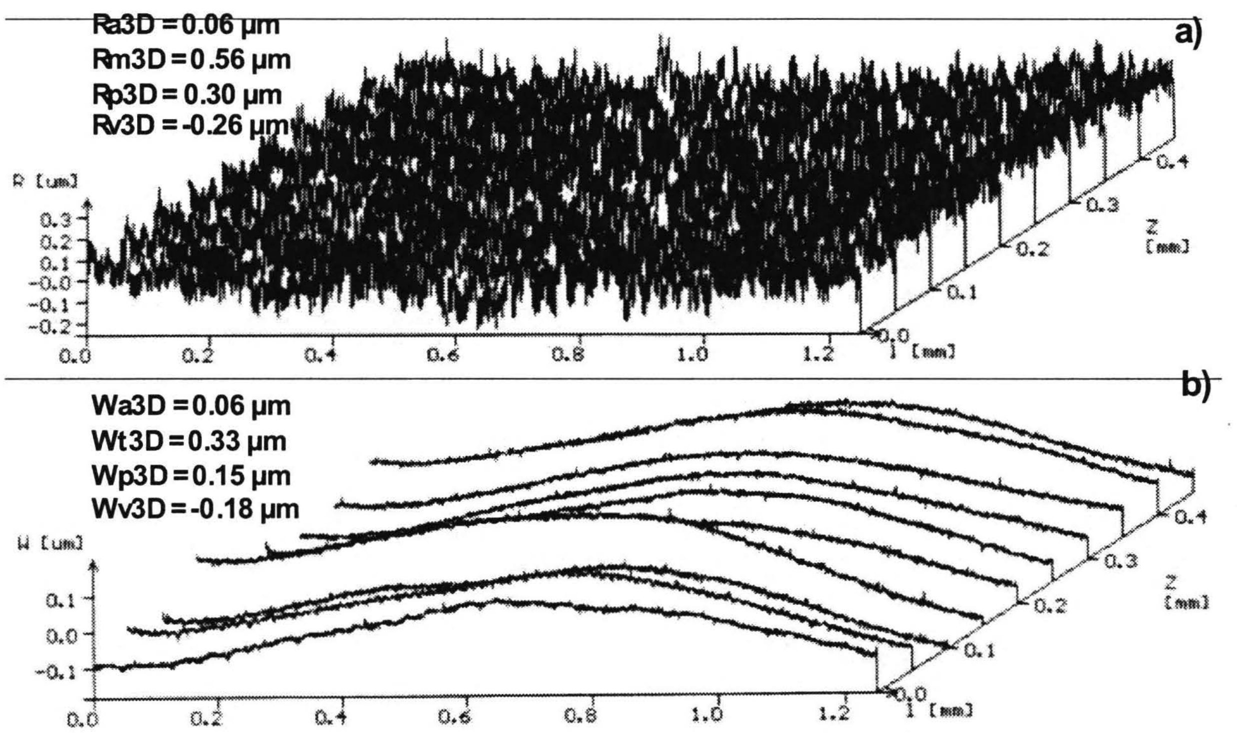

Figure 9 Profilograms of roughness (a) and waviness (b) in 2D configuration of SiC surface after lapping process (using polycrystalline diamond grains of ø 9 μm)

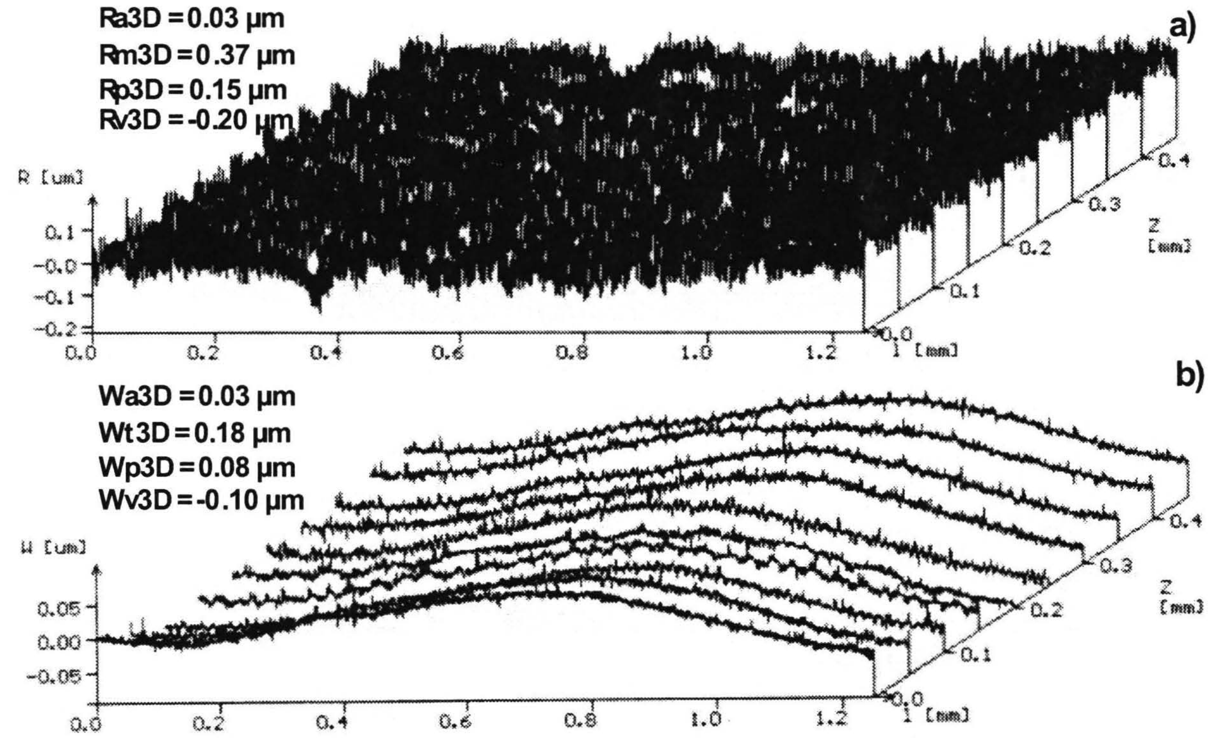

Figure 10 Profilograms of roughness (a) and waviness (b) in 3D configuration of SiC surface after polishing process (using cerium oxide grains of ø 1 μm)

4.2. *Determination of SiC surface layer morphology*

Morphology assessment of investigated samples surfaces has done using AFM technique. The basis of micro– and nanostructure estimation of SiC samples have been images of their surfaces in 2D and 3D configuration which have been obtained using atomic force microscope (AFM) of firm VEECO Multimode 5–USA. This stand is on equipment of Institute of Materials Science of Technical University of Lodz laboratory. The microscope has been equipped with scanning sonde of resonance frequency $f = 325$ kHz and elasticy constant $k = 40$ N/m. The images acquisition has been made using Nanoscope 7.3 computer program and MountainsMap 5 program has been used for the final pictures processing.

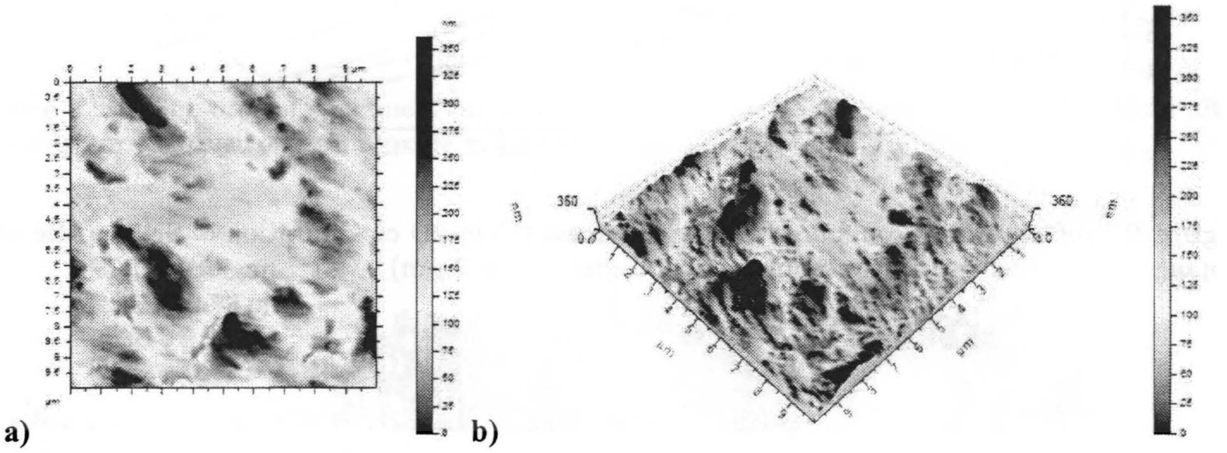

Figure 11 AFM images of SiC sample surface layer after first grinding process (diamond grains of ø 125 μm): a) image in 2D configuration, b) image in 3D configuration

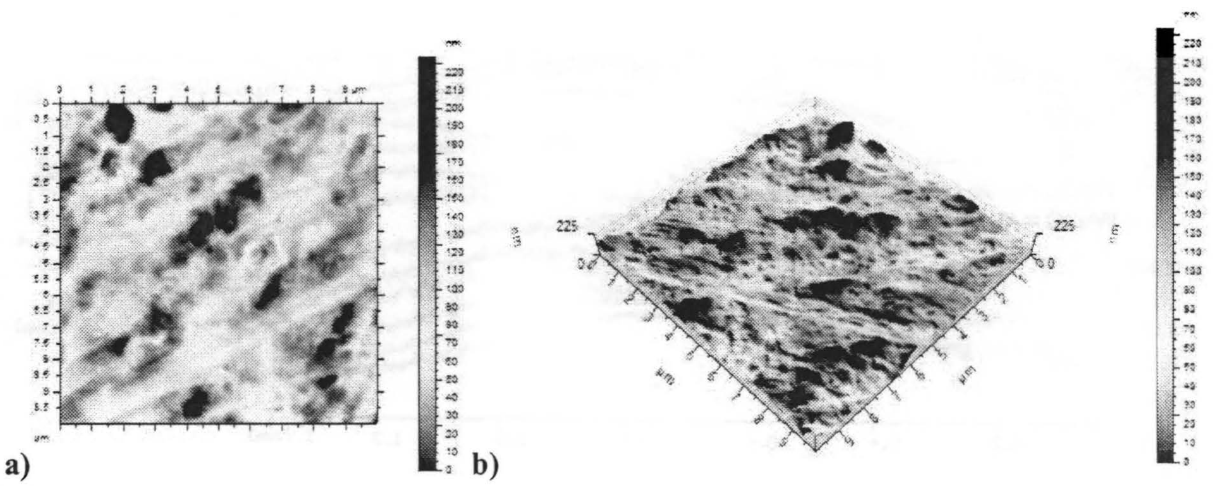

Figure 12 AFM images of SiC sample surface layer second grinding process (diamond grains of ø 40 μm): a) image in 2D configuration, b) image in 3D configuration

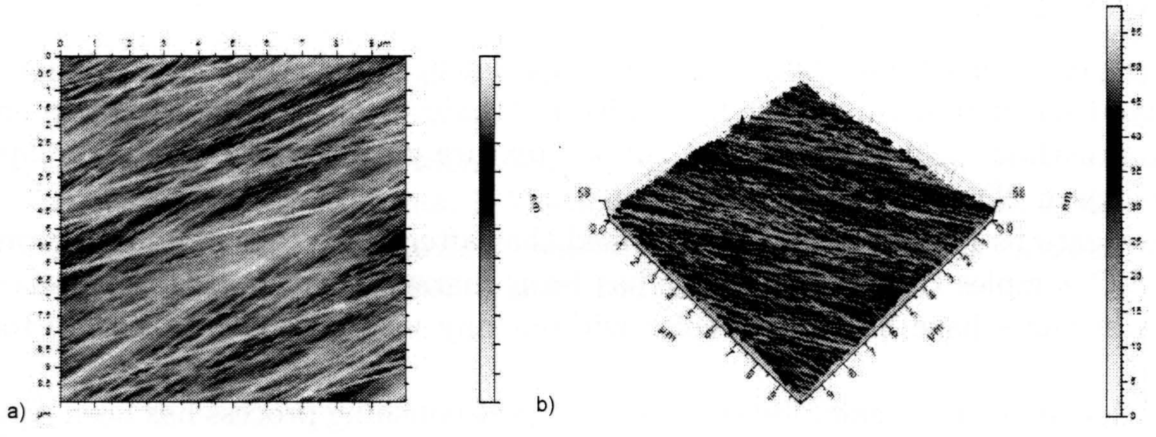

Figure 13 AFM images of SiC sample surface layer after lapping process (polycrystalline diamond grains of ⌀ 9 μm): a) image in 2D configuration, b) image in 3D configuration

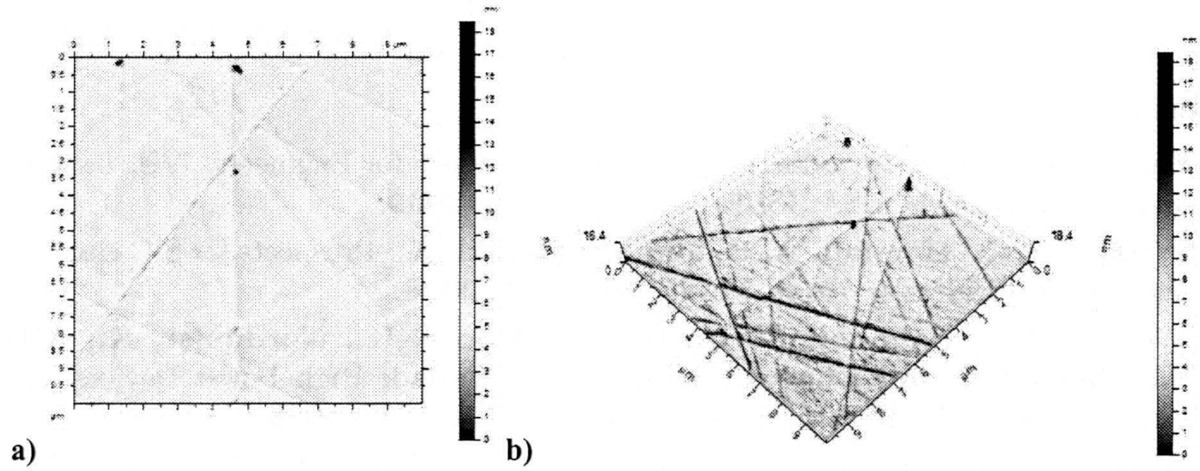

Figure 14 AFM images of SiC sample surface layer after polishing process (cerium oxide grains of ⌀ 1 μm): a) image in 2D configuration, b) image in 3D configuration

Every time the area of sample of dimension 10 x 10μm has been analyzed. Exemplary images of SiC samples surface layer morphology after sequential grinding, lapping and polishing stages have been depicted in Figs 11–14. These images have revealed significant changes in their surface layer morphology. Images of SiC samples surfaces obtained by AFM method after grinding process (Figs 11 and 12) have shown presence of many corrugations and distinct tool marks caused by machining, which have been visible in form of irregular scratches on surface. However after lapping process SiC surface layer has had smooth surface and several scratches visible in form of cracks (Fig. 13). After polishing process SiC sample surface has had only several visible lines of machining (Fig. 14).

5. Conclusions

In the paper it has been elaborated and experimentally checked out technology of preparation of structures based on silicon carbide using grinding, lapping and polishing method, compared selected surface texture parameters and surface layer morphology in 2D and 3D configuration.

Investigations carried out have confirmed that after final stage of polishing process of SiC samples their surface layer has been characterized by uniform texture. Samples surfaces have had glossy color without any visible to the naked eye tool marks.

The thickness of SiC samples after final stage of polishing process has been equal to circa 0,350 mm, thus required 150 μm of SiC substrate has been removed.

Elaborated technological process has ensured appropriate preparation of silicon carbide samples in range of required surface roughness and waviness and optical purity.

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