DESIGN, SIMULATION AND FABRICATION OF ALGAN/GAN NORMALLY-OFF HIGH ELECTRON MOBILITY TRANSISTORS WITH INVESTIGATION ON TEMPERATURE STABILITY

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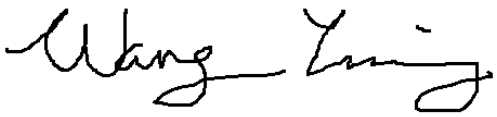
DECLARATION

I hereby declare that this thesis describes my PhD research work and I declare that it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously



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Abstract

AlGaN/GaN high electron mobility transistor (HEMT) has become a promising candidate to replace the conventional Silicon-based transistors in the field of power electronics due to the superiority in its channel mobility and its critical breakdown field. However, the device characteristics under high-temperature ambient are not fully understood for reliable implementations into the high power systems. In this thesis, the design, simulation, fabrication, and characterisation on the AlGaN/GaN HEMTs with investigations on high-temperature characteristics are carried out thoroughly.

Firstly, a Schottky-gated AlGaN/GaN HEMT was characterised and analytically modelled at temperatures up to 500K. The variation in some of the important physical parameters such as the Schottky barrier height, V_{TH}, sub-threshold swing, and specific contact resistances at high temperatures have been modelled with the verification of Sentaurus TCAD simulation. This work provides fundamental knowledge on the device performance and temperature dependence of the AlGaN/GaN HEMTs, which is useful for later studies.

Additionally, due to the intrinsic existence of the two-dimensional electron gas (2DEG) at the AlGaN/GaN interface caused by the polarisation field, the fabricated Schottky-gated HEMTs have negative V_{TH}, which is unsafe for high-power applications. Therefore, this thesis also focuses on the V_{TH} engineering through the partial AlGaN barrier recess combined with multiple fluorine plasma treatments (FPT) onto the Al_2O_3 gate dielectrics. The partial recess at the gate region is able to weaken the 2DEG density without degrading the channel conductivity. With subsequent triple Al_2O_3 deposition-FPT cycles,

significant amount of negative charge is incorporated into the gate dielectric to shift the V_{TH} to +6.5V. The negative charge concentration and distribution have been verified and modelled by the Sentaurus TCAD simulation and the V_{TH} analytical model. Such normally-off metal-insulator-semiconductor (MIS) HEMT is able to construct a monolithic logical inverter by integrating it with a normally-on MIS-HEMT. The fabricated inverter has high output swing of 96.6% and fast switching speed of less than 130ns, which is applicable for power integration circuits.

However, the V_{TH} is unstable for the MIS-HEMTs with multiple FPT on the Al_2O_3 layer at high temperature ambient. This thesis also proposed a method to characterise the distribution of FPT-induced electron trapped levels within the Al_2O_3 gate dielectrics through the V_{TH} swing and the gate stressing techniques. The V_{TH} thermal instability is caused by the shallower electron trap energy levels than the energy level within the Al_2O_3 bandgap from which electron emission will occur at high temperature named as the trap emission energy. It is also observed that at higher FPT power, the V_{TH} reduction is less at temperatures up to 200°C. Hence, higher FPT power is able to increase the amount of trapped electrons at deeper levels than the trap emission energy at high temperatures.

The relationship between the FPT power and the V_{TH} high-temperature stability of the fluorinated Al_2O_3/AlGaN/GaN MIS-HEMTs proposes a link between the Al-F bond incorporation and the trap energy level. To further enhance the V_{TH} high-temperature stability and process simplicity, a novel short Argon plasma treatment (APT) followed by single FPT on Al_2O_3 with inductively coupled plasma reactive ion etching (ICP-RIE) instrument is

reported in this thesis. High V_{TH} of 4.4V, satisfactory drain saturation current (I_{DMAX}) of 320mA/mm at ($V_G - V_{TH}$)=6V and 30% improvement in breakdown voltage than the device without APT were achieved. The measured V_{TH} of 2.5V at 200°C is the highest in hitherto reported FPT-AlGaN/GaN HEMTs. Based on the secondary ion mass spectroscopy (SIMS) and the X-ray photoelectron spectroscopy (XPS), the APT is able to effectively enhance the breaking of Al-O bonds and allow for the generation of excessive Al-F bonds in the following FPT process on the Al_2O_3 surface. According to the gate-stressing test which extracted the trap state distribution of the fabricated MIS-HEMTs together with the Gaussian 09 molecular simulations on the $Al_2O_{2.5}F$ and $Al_2O_2F_2$ cells with similar Al-F composition to the XPS characterisation results, the APT-then-FPT process can effectively shift most of the trap states to deeper energy levels than the trap emission level at 200°C. Therefore, better V_{TH} thermal stability was achieved at 200°C with the APT-then-FPT process.

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List of Abbreviations

Abbreviation	Description
2DEG	Two-dimensional electron gas
ALD	Atomic layer deposition
APT	Argon plasma treatment
CEP	Cathode electrode power for the ICP-RIE system
CMOS	Complementary metal-oxide-semiconductor
CP	Coil power for the ICP-RIE system
FPT	Fluorine plasma treatment
HEMT	High electron mobility transistor
ICP-RIE	Inductively coupled plasma reactive ion etching
I_D-V_D	Drain current versus drain voltage characteristics
I_D-V_G	Drain current versus gate voltage characteristics
I_G-V_G	Gate current versus gate voltage characteristics
MIS-HEMTs	Metal-insulator-semiconductor high electron mobility transistors
MOCVD	Metal-organic chemical vapour deposition
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistors
PECVD	Plasma-enhanced chemical vapour deposition
RIE	Reactive ion etching
SEM	Scanning Electron Spectroscopy
SIMS	Secondary ion mass spectroscopy
XPS	X-ray photoelectron spectroscopy

List of Symbols

Symbol	Description	Unit
E_G	Bandgap	eV
V_B	Base Voltage for pulsed current-voltage characteristics	V
k	Boltzmann constant	eVK^{-1}
ξ_{BR}	Breakdown electric field	MV/cm
V_{BR}	Breakdown voltage	V
C	Capacitance	F
σ	Capture cross section of the trap states	cm^2
G	Conductance	S
E_C	Conduction band edge	eV
ΔE_c	Conduction band offset	eV
N_C	Density of states	cm^{-3}
D_N	Density of trap states created by the single fluorine plasma treatments by ICP-RIE	cm^{-2}/eV
n_s	Density of two-dimensional electron gas	cm^{-2}
ε_{Al2O3}	Dielectric constant for Al_2O_3	
ε_{AlGaN}	Dielectric constant for AlGaN	
ε_{GaN}	Dielectric constant for GaN	
V_D	Drain Voltage	V
C_{13}, C_{33}	Elastic constants	GPa
μ_n	Electron mobility	$cm^2/V{\cdot}s$
q	Electronic charge	C
D_{eq}	Equivalent density of trap states created by the multiple fluorine plasma treatments transformed to the Al_2O_3/AlGaN interface	cm^{-2}/eV
τ_{fall}	Fall time of a square wave	ns
E_F	Fermi level	eV
I_G	Gate current	A/mm
L_G	Gate length	µm
L_{GD}	Gate-to-drain spacing	µm
L_{GS}	Gate-to-source spacing	µm
NM_H	High noise margin voltage	V
V_{IL}	Input-low voltage	V
V_{IH}	Input-high voltage	V
a	Lattice constant	Å
NM_L	Low noise margin voltage	V
I_{DMAX}	Maximum drain saturation current	A/mm
I_{off}	Off-state drain leakage current	A/mm
R_{on}	On-state resistance	$\Omega{\cdot}cm^2$
V_{OL}	Output-low voltage	V
V_{OH}	Output-high voltage	V
e_{31}, e_{33}	Piezoelectric constant	C/m^2
P_{PE}	Piezoelectric polarisation charge	C/m^2

σ_{pol}	Polarisation charge density	C/m^2
τ_{PHL}	Propagation delay from high-to-low	ns
τ_{PLH}	Propagation delay from low-to-high	ns
τ_{rise}	Rise time of a square wave	ns
ϕ_b	Schottky barrier height	V
R_{sh}	Sheet resistance	Ω/square
ρ_c	Specific contact resistivity	Ω·cm
P_{SP}	Spontaneous polarisation charge	C/m^2
SS	Sub-threshold swing	mV/decade
T	Temperature	K or °C
v_{th}	Thermal velocity	cm/s
d	Thickness of the AlGaN barrier layer	nm
V_{TH}	Threshold voltage	V
g_m	Transconductance	S
τ_e	Trap emission time	s
E_T	Trap energy level from the conduction band edge	eV
W_{ratio}	Width ratio of normally-off versus normally-off devices	

CHAPTER 1 Introduction

1.1 Background

The semiconductor industry has been dominated by silicon-based technology for decades with mature CMOS fabrication process. However, the need for higher power applications has made the silicon-based devices unsuitable because of its limitations on the channel mobility, saturation velocity, operating temperatures and the breakdown field [1]. Therefore, it is essential to use an alternative material to replace silicon in the field of modern power electronics applications.

Table 1.1 summarises the material parameters for Si, GaAs, SiC and GaN. These are the major materials used in the semiconductor industry. The first generation of devices based on III-V materials is the high electron mobility transistor (HEMT) with AlGaAs/GaAs heterojunction as the barrier and buffer layers of the device. With the appropriate amount of doping and applied gate bias, the two-dimensional electron gas (2DEG) carrier density can reach the magnitude of 10^{12} cm^{-2} for the AlGaAs/GaAs devices [2]. However, its small bandgap results in small breakdown field, which is not desirable for high power applications. Even though SiC is a good candidate for high power applications due to its wide bandgap (i.e. the fabricated device can potentially obtain high breakdown voltage), the carrier mobility is the lowest amongst these four materials. The low carrier mobility is undesirable for good on-state conductivity and fast switching speed.

Thus, amongst all of the materials listed in Table 1.1 [3], Gallium Nitride (GaN) is a promising material to fabricate HEMTs for high power applications due to its high breakdown field and good carrier mobility within the 2DEG. These physical properties allow GaN based devices to handle higher breakdown voltage, conduction current, and switching speed than conventional Si based power transistors.

Table 1.1 Comparison of GaN material properties with Si, GaAs, and SiC [3].

Properties	**Si**	**GaAs**	**SiC**	***GaN***
Energy Gap (eV)	1.11	1.43	3.2	*3.4*
Breakdown Electric Field (ξ_{BR}, in MV/cm)	0.6	0.5	3.0	*3.5*
Saturation Velocity (υ_{sat}, in 10^7 cm^2/s)	1.0	1.0	2.0	*2.5*
Thermal Conductivity (W/cm/K)	1.5	0.5	4.9	*1.5*
Mobility ($cm^2/V/s$)	1300	6000	600	*1500*

For GaN based devices used in power electronics, one of the challenges is the achievement of normally-off operations (i.e. the threshold voltage (V_{TH}) is greater than zero) in order to ensure the system security. Due to the intrinsic polarisation field within the material, 2DEG exists at the AlGaN/GaN interface without providing any external bias. Hence, the fabricated device is normally-on (i.e. $V_{TH}<0$) if no special gate design is implemented. Techniques such as AlGaN barrier layer recess which removed the local 2DEG channel under the gate [4-6], p-GaN cap layer at the gate which depleted the 2DEG at the AlGaN/GaN interface due to the junction depletion field [7, 8] and fluorine incorporation which introduced negatively charged ions to deplete the 2DEG at the gate [9] are implemented to achieve normally-off operations. Details of the abovementioned gate treatment techniques will be reviewed in Section 1.3.

Additionally, the performance of the power devices under high-temperature is important for power electronics applications as the power system is usually

implemented under high ambient temperature. For instance, the power electronic system within the electric or hybrid electric vehicles located near the engine has an ambient temperature of up to 200°C [10]. Therefore, proper modelling of the device performance at high temperature is important during the system design. In addition, the threshold voltage stability at high temperature is one of the most important properties for power devices as it is directly related to the on/off characteristics and the current rating of the device. A stable and high positive V_{TH} at high temperature ensure the safety, standby power consumption and performance of the system.

1.2 Overview of polarisation effect at AlGaN/GaN interface

The highly conductive two-dimensional electron gas (2DEG) formed at the AlGaN/GaN interface can act as the channel of a AlGaN/GaN HEMT. It is induced by the intrinsic polarisation effect without any external bias to the device nor any intentional doping to the material. Unlike the symmetrical materials such as tetrahedral-shaped silicon, the non-centrosymmetric materials have different faces at the opposing but uniaxial directions. For wurzite GaN structure, the (0001) faced GaN has gallium atoms at the surface (Ga-face), and the $(000\bar{1})$ faced GaN has nitrogen atoms at the surface (N-face), as illustrated in Fig. 1.1. Different methodologies for GaN epitaxial growth produce different faced layers. For example, plasma-induced molecular beam epitaxy (PIMBE) grown GaN films are N-faced, while for metal-organic chemical vapour deposition (MOCVD) grown GaN films produce Ga-faced surface [11].

The different faces of the material induce different polarity of the polarisation charge at the AlGaN/GaN interface, therefore result in different

electrical characteristics for the fabricated device. The polarisation consists of two different mechanisms: spontaneous and piezoelectric. The spontaneous polarisation (P_{SP}) is generated by the electron cloud displacement in the asymmetric GaN crystal [12], and the piezoelectric polarisation (P_{PE}) is induced by the mechanical force between the atoms at the AlGaN/GaN interface due to the lattice mismatch between AlGaN and GaN[13].

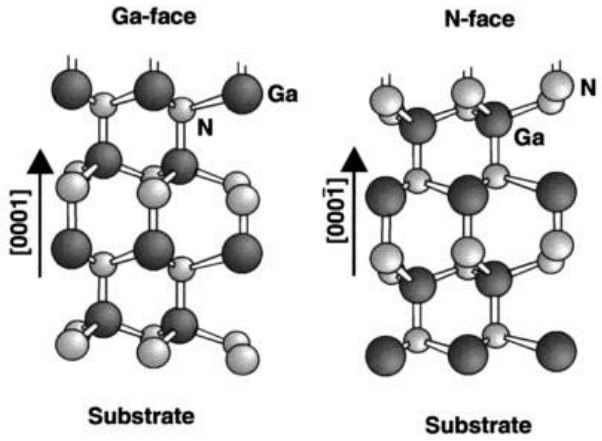


Fig. 1.1 Schematic diagram of the crystal structure of wurzite Ga-faced and N-faced GaN [11]

Fig. 1.2 summarises the polarity of spontaneous and piezoelectric polarisation at different faces and tensile forces. It is observed that for Ga-faced GaN, the electric field created by P_{SP} is pointing towards the substrate. For N-faced GaN, it is pointing towards the surface. Additionally, if interfacial mechanical forces exist at the AlGaN/GaN interface, P_{PE} will be induced. P_{SP} and P_{PE} will have the same polarity if the AlGaN barrier is experiencing tensile strain due to its smaller lattice constant than the GaN buffer. If GaN and AlGaN become the barrier and the buffer layers respectively, compressive strain will be exerted on the GaN barrier [6]. For AlGaN/GaN epitaxial layers grown by MOCVD, AlGaN layer is grown on Ga-face and experiences tensile strain. Therefore, both the P_{SP} and P_{PE} fields are pointing towards the substrate and a

net positive polarisation charge is induced at the AlGaN/GaN interface, as shown in Fig. 1.2(b). For AlGaN/GaN HEMT applications, MOCVD is normally used to obtain net positive polarisation charge.

The total amount of polarisation charge at Ga-faced AlGaN/GaN interface (σ_{pol}) can be expressed as Eq. (1.1) [13]. In Eq. (1.1), the amount of P_{SP} for wurzite GaN is -0.029 C/m^2 and the P_{SP} for AlGaN can be extracted by Eq. (1.2) [13], where x is the Al content within AlGaN. P_{PE} of AlGaN and GaN are defined in Eq. (1.3) [13], where a_0 is the lattice parameter at equilibrium, e_{31} and e_{33} are the piezo-electric coefficients and C_{13} together with C_{33} are the elastic coefficients. The detailed values of the above parameters are summarised in Table 1.2.

To compensate the positive polarisation charge at the Ga-faced AlGaN/GaN interface, free electrons accumulate at the AlGaN/GaN interface and form the two-dimensional electron gas (2DEG). 2DEG can be used as the conduction channel of a transistor. The 2DEG sheet carrier density for an ideal Schottky-gated AlGaN/GaN HEMT can be modelled by Eq. (1.4) [14], where q is the elementary charge for single carrier (1.6×10^{-19} C), t_{AlGaN} is the thickness of AlGaN, ε_0 is the permittivity in vacuum (8.85×10^{-14} F/cm), ε_{AlGaN} is the relative permittivity for AlGaN, ϕ_b is the Schottky barrier of the gate contact, E_F is the Fermi level from the GaN conduction band and ΔE_C is the conduction band offset between AlGaN and GaN. The ϕ_b, ε_{AlGaN}, E_F, and ΔE_C can be approximated by Eq. (1.5) to (1.8) [11], where $m^* \approx 0.22m_e$ is the effective electron mass of AlGaN, $\hbar$ is the plank's constant and E_g is the bandgap.

$$\begin{aligned}\sigma_{pol} &= P(AlGaN) - P(GaN) \\ &= \{P_{SP}(AlGaN) + P_{PE}(AlGaN)\} - P_{SP}(GaN) + P_{PE}(GaN)\}\end{aligned} \tag{1.1}$$

$$\mathrm{P_{SP}}(AlGaN) = -0.052x - 0.029, \text{ in } \mathrm{C/m^2} \tag{1.2}$$

$$\mathrm{P_{PE}} = 2\frac{a - a_0}{a_0}(e_{31} - e_{33}\frac{C_{13}}{C_{33}}) \tag{1.3}$$

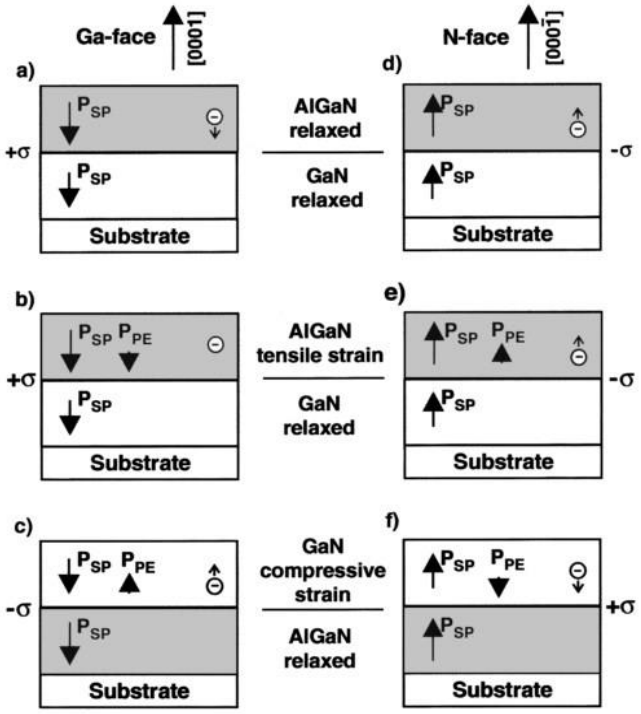


Fig. 1.2 Polarisation induced sheet charge density and directions of the spontaneous and piezoelectric polarisation in Ga- and N-face strained and relaxed AlGaN/GaN heterostructures [11].

Table 1.2 Summary of the parameters used for P_{SP} and P_{PE} calculations of AlGaN and GaN

	Al_xGaN	**GaN**
a_0 (nm)	0.3112x+0.3189(1−x)	0.3189
e_{31} (C/m^2)	−0.11x−0.49	−0.49
e_{33} (C/m^2)	0.73x+0.73	0.73
C_{13} (GPa)	5x+103	103
C_{33} (GPa)	−32x+405	405

$$n_s(x) = \frac{\sigma_{pol}}{q} - \frac{\varepsilon_0 \varepsilon_{AlGaN}}{q^2 t_{AlGaN}}[q\phi_b + E_F - \Delta E_C] \tag{1.4}$$

$$\varepsilon_{AlGaN} = -0.5x + 9.5 \tag{1.5}$$

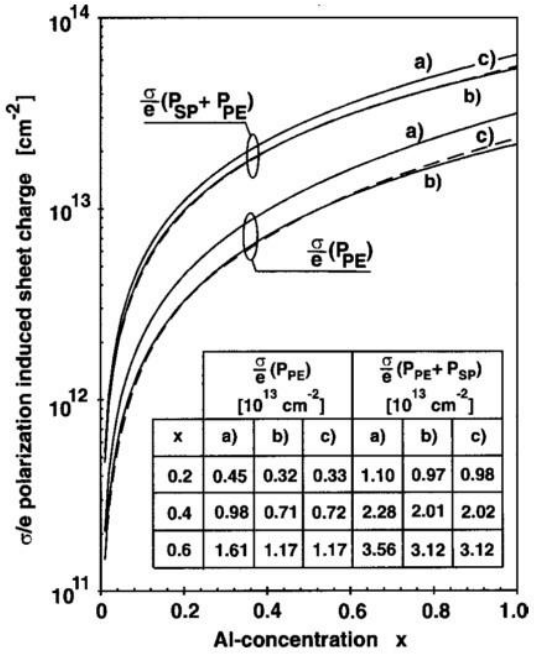
$$q\phi_b = 1.3x + 0.84, \text{ in eV} \tag{1.6}$$

$$E_F = \{\frac{9\pi\hbar q^2}{8\varepsilon_0\sqrt{8m^*}}\frac{n_s(x)}{\varepsilon_{AlGaN}}\}^{2/3} + \frac{\pi\hbar^2}{m^*}n_s(x) \tag{1.7}$$

$$\Delta E_C = 0.7[E_g(x) - E_g(0)] \tag{1.8}$$

Where
$$\begin{aligned} E_g(x) &= xE_g(AlN) + (1-x)E_g(GaN) - x(1-x)1.0 \\ &= x6.13 + (1-x)3.42 - x(1-x)1.0 \end{aligned}, \text{ in eV}$$

According to Eq. (1.1), (1.2) and (1.3), the Al content in AlGaN is an important factor to the magnitude of polarisation effect and the induced 2DEG density accordingly, since higher Al content enhances the AlGaN lattice mismatch with GaN. Fig. 1.3 demonstrates the effect of Al content to both P_{SP} and P_{PE}, and they both increase with higher Al content.



x	σ/e (P_PE) [10^13 cm^-2] a)	b)	c)	σ/e (P_PE + P_SP) [10^13 cm^-2] a)	b)	c)
0.2	0.45	0.32	0.33	1.10	0.97	0.98
0.4	0.98	0.71	0.72	2.28	2.01	2.02
0.6	1.61	1.17	1.17	3.56	3.12	3.12

Fig. 1.3 The relationship between polarisation-induced sheet charge and aluminium concentration [13].

The formation of 2DEG by the polarisation field can also be explained by the energy band diagram shown in Fig. 1.4. For an ideal surface where the defects are absent, the valence band of AlGaN surface is approaching the Fermi level as its thickness increases during epitaxial growth. Once the valence band of AlGaN surface reaches the Fermi level at the AlGaN critical thickness (d_{CR}), holes accumulate at the AlGaN surface and the same amount of negative sheet charge (i.e. the 2DEG) is formed at the interface to compensate the surface holes. The accumulated holes at the surface will hinder further potential increase due to the increase of AlGaN thickness. Hence, the 2DEG density is at equilibrium [15].

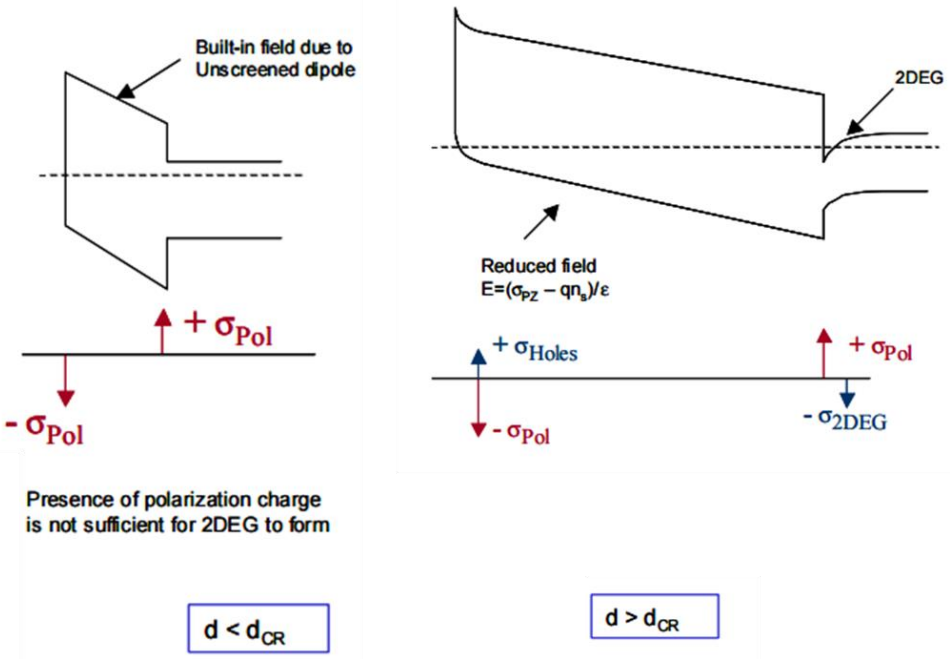


Fig. 1.4 The formation of 2DEG for ideal AlGaN surface [15]

If the AlGaN growth condition is not ideal, surface trap states will exist at the AlGaN surface, as shown in Fig. 1.5. When the thickness of AlGaN reaches the d_{CR}, electrons from the ambient partially fill the surface trap states and pin the Fermi level near the trap level. The electrons trapped at the surface, which

are defined as surface donors, have opposite polarity as the polarisation field. Therefore, the 2DEG density at the AlGaN/GaN interface is smaller than that with perfect AlGaN surface. Therefore, it is necessary to reduce the amount of surface trap states of the device by surface passivation during device fabrication.

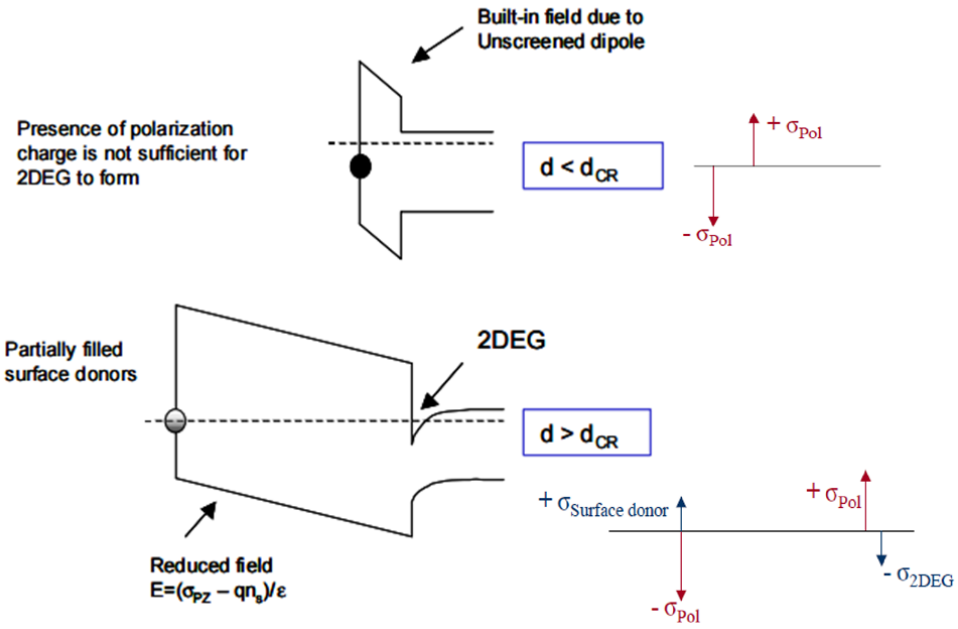


Fig. 1.5 The formation of 2DEG for non-ideal AlGaN surface [15].

1.3. Review of normally-off techniques for AlGaN/GaN HEMTs

Due to the nature of intrinsic polarisation effect for GaN, the fabricated devices will be at normally-on operations if no special treatment is applied at the gate region. It is not desirable for power applications due to system safety concerns. Design techniques such as AlGaN barrier layer recess [4-6], p-GaN cap layer [7, 8] and charged ion implantation through plasma treatment [9] have been implemented to realise normally-off (V_{TH}>0) operations and will be reviewed in this Section.

1.3.1 AlGaN barrier recess

According to the 2DEG formation mechanism illustrated in Section 1.2, 2DEG at the AlGaN/GaN interface will not be induced if the AlGaN barrier layer is below the critical thickness. Therefore, the channel between the source and drain contacts can be pinched off by selectively etching off the barrier layer at the gate region. The channel can be restored by the electron accumulation from a gate bias greater than the V_{TH}.

The relationship between the recessed gate and the performance of the device was reported in [6]. Fig. 1.6 is the cross-section schematic of the recessed-gate HEMT. In this figure, the $Al_{0.25}Ga_{0.75}N$ barrier layer is 25nm and the GaN channel layer is 2μm. The gate recess was realised by $Cl_2/BCl_3/Ar$ inductively coupled plasma reactive ion etching (ICP-RIE).

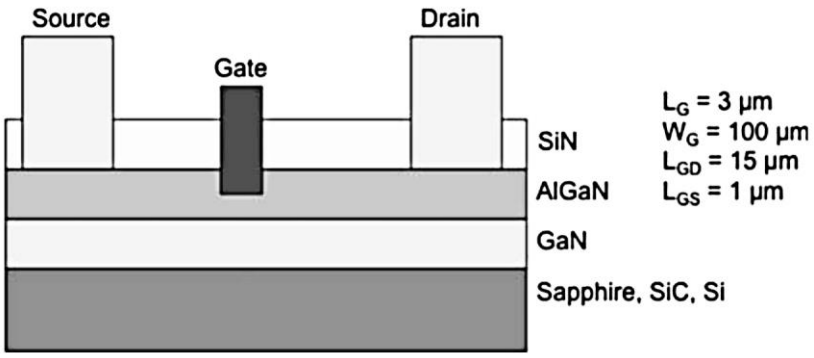


Fig. 1.6 Cross-sectional schematics of the recessed-gate HEMT reported in [6]

Fig. 1.7 and Fig. 1.8 demonstrate the I_D-V_G characteristics and the extracted V_{TH} of the devices with different recess depth and etch time. It is clearly shown that the V_{TH} is higher with the deeper recess depth. However, the maximum V_{TH} achieved by this method is only slightly above 0V. Additionally, the slope of the I_D-V_G is degrading with increasing recess depth. It implies the degradation of transconductance (the slope of the I_D-V_G curve) and the increase of on-state

resistance due to its damage to the AlGaN/GaN interface and the degradation in the carrier mobility.

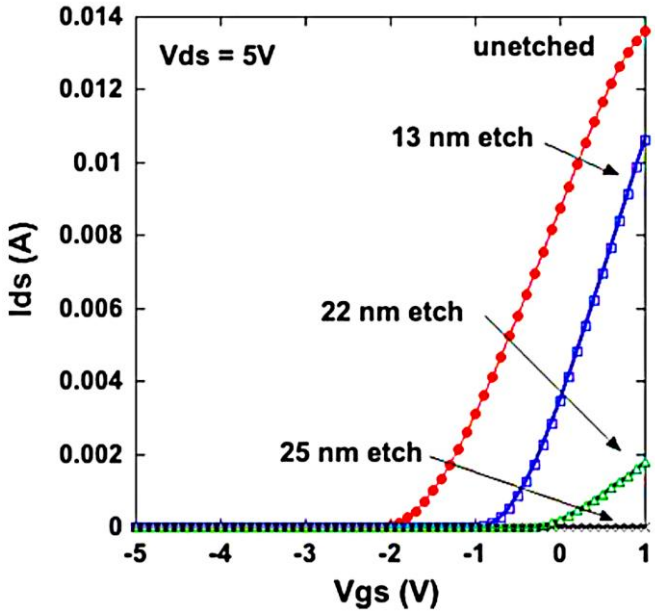


Fig. 1.7 I_D-V_G characteristics of the AlGaN/GaN HEMT with different AlGaN etching depth at the gate region. Measurement was carried out when V_{DS}=5V [6]

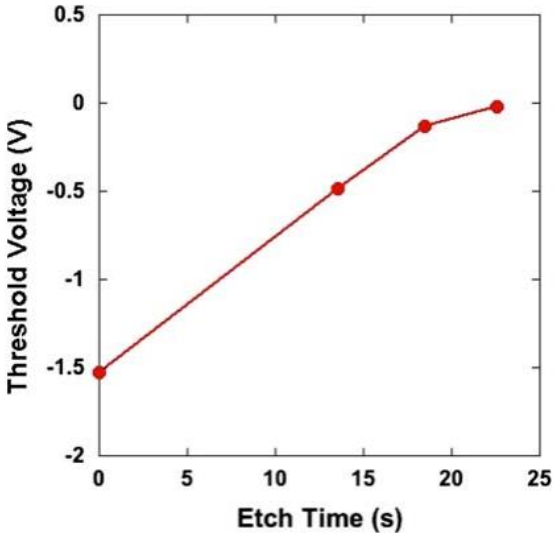


Fig. 1.8 Summary of extracted threshold voltage as a function of AlGaN etching time [6]

In Fig. 1.9, the 2DEG carrier mobility is obviously reduced with the increase of AlGaN recess depth. It is due to the exacerbation of carrier scattering by surface roughness. Therefore, for the state-of-the-art gate recessed devices

reported, surface recovery or protection have been applied to the gate to restore the degradation in mobility. The most common technique is to deposit a thin passivation layer before gate metal deposition to obtain metal-insulator-semiconductor (MIS) gate configurations [16, 17]. Another method reported is to insert an thin etch-stop layer in between AlGaN and GaN layers to ensure the etching process do not damage the GaN layer [18].

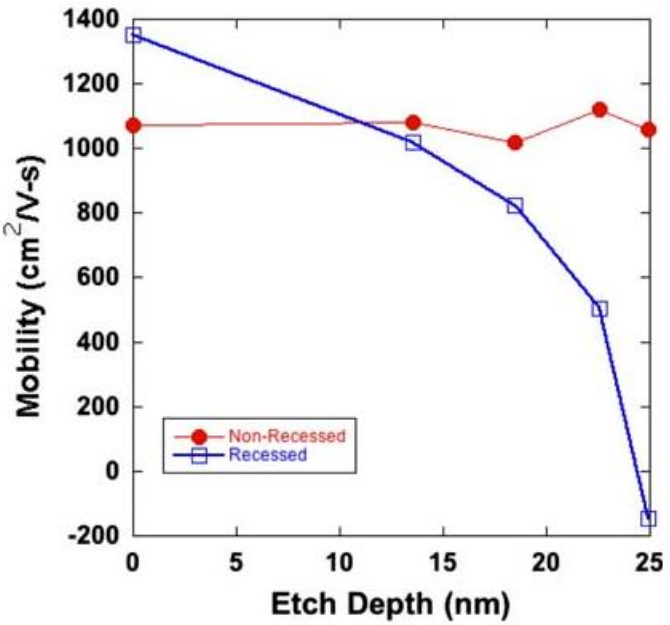


Fig. 1.9 Mobility as a function of etch depth [6]

The advantage of the barrier recess technique is the applicability in the cleanroom and the simplicity to implement into the fabrication process. It uses reactive ion etching (RIE) equipment with Cl_2-based gas, which are commonly used in the semiconductor industry or the laboratory. In addition, only one additional lithography process is required before the barrier etching. Table 1.3 summarises the V_{TH} and the maximum drain saturation current (I_{DMAX}) of the state-of-the-art normally-off GaN HEMT with different gate recess techniques. Due to different gate structures of the devices, I_{DMAX} reported in Table 1.3 are achieved with different gate overdrive voltages ($V_G - V_{TH}$). Even though the

novel etch-stop barrier layer has been implemented to control the gate recess, passivation layer deposition after gate recess is still a more widely-used technique that provides highest V_{TH} and I_{DMAX}.

Table 1.3 The threshold voltage (V_{TH}) and maximum drain current (I_{DMAX}) of the state-of-the-art GaN devices utilising gate recess techniques. The differences between the V_G and V_{TH} when I_{DMAX} are also shown in the table.

Reference	**Gate Processing Technique**	**V_{TH}**	**I_{DMAX}**
[16]	Wet Etch Recess+Al_2O_3 passivation	+1.7V	420mA/mm (@V_G−V_{TH}=4.3V)
[17]	Recess+SiN_X & HfO_2 dielectric stack	+1.65V	650mA/mm (@V_G−V_{TH}=4.35V)
[18]	Addition of AlN Etch-stop barrier layer	+0.3V	250mA/mm (@V_G−V_{TH}=2.7V)

The disadvantage for the barrier layer recess is the difficulty in the precise control of the etch thickness. If the AlGaN barrier is under-etched, the V_{TH} will be unable to reach normally-off condition. If the AlGaN barrier is over-etched, the surface damage introduced by the dry etching process will degrade the 2DEG carrier mobility and reduce the on-state conductivity and switching speed of the device. Additionally, the barrier recess technique is unable to obtain high enough V_{TH} due to the absence of additional depletion field or p-n junction.

1.3.2 P-GaN cap layer

Similar to the working principles of typical p-n homo-junction, the addition of p-GaN layer on top of the unintentionally doped AlGaN barrier can form a junction field which can deplete the 2DEG charge at the AlGaN/GaN interface. Fig. 1.10 compares the conduction band of the device with and without p-GaN layer. It is shown that the p-GaN layer at the gate is able to shift the conduction band at AlGaN/GaN interface above the Fermi level (0eV), implying the disappearance of the 2DEG and normally-off operations.

Fig. 1.11 demonstrates the schematic diagram of the p-GaN gate power HEMT on Si substrate reported by [19]. In Fig. 1.12, the threshold voltage reaches about +3V, which is much higher than the gate recess technique. The gate current becomes significant when V_G>6V at V_D=1V, implying the p-GaN/AlGaN junction forward voltage is about 6V. At V_D=10V, the gate current is suppressed even when V_G is greater than 6V. This can be explained by the hindering of the gate current flow as the p-GaN/AlGaN heterojunction is reversed biased between the drain and the gate terminals.

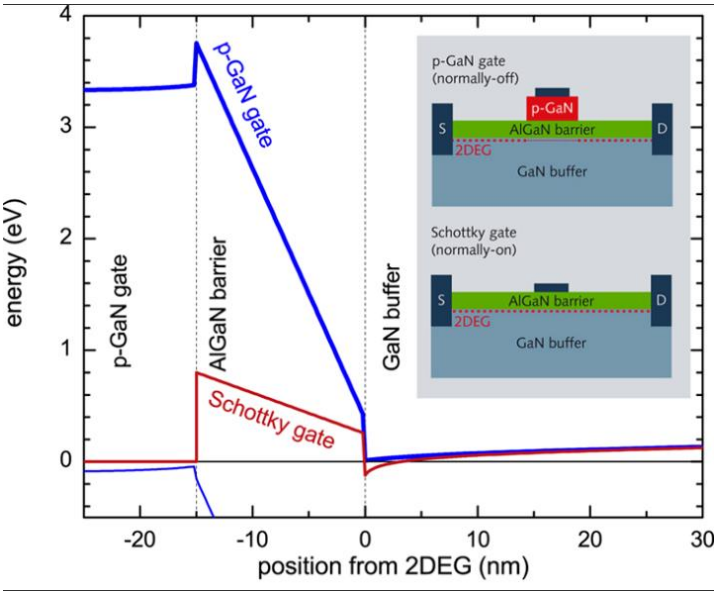


Fig. 1.10 The conduction band energy level underneath a normally-off p-GaN gate (blue line, cross-sectional schematic diagram is shown in the inset above) compared to a Schottky gate (red line, cross-sectional schematic diagram is shown in the inset below) [8]

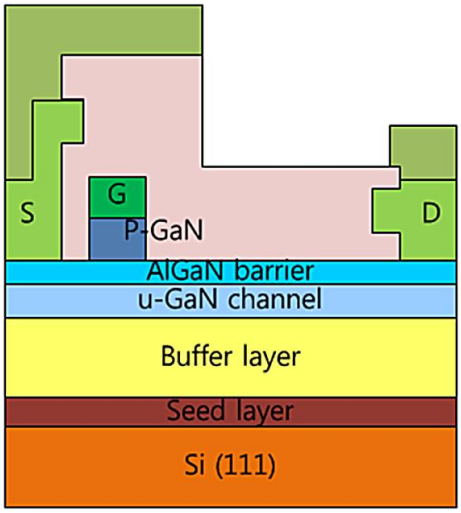


Fig. 1.11 Schematic diagram of the p-GaN gate power HEMT on Si substrate [19]

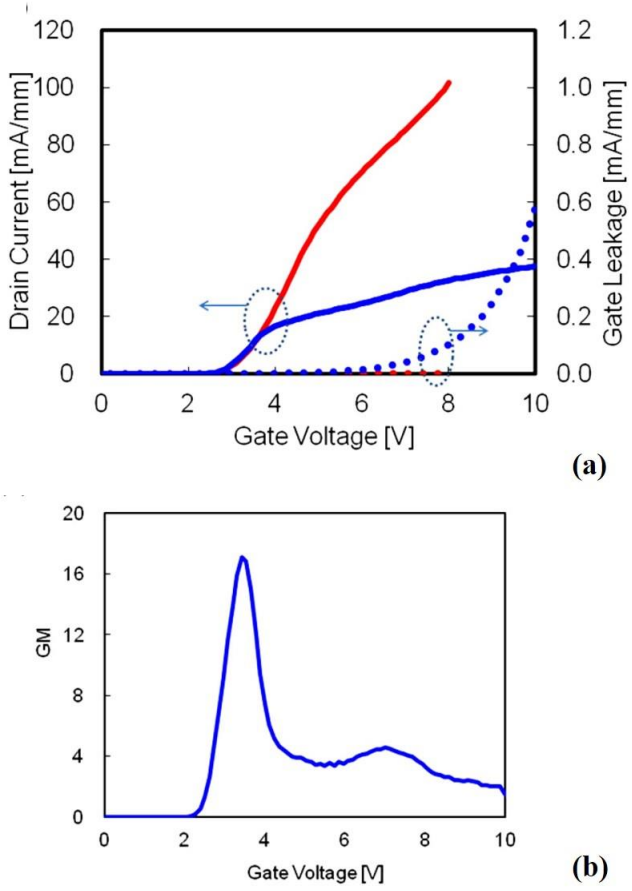


Fig. 1.12 The electrical characteristics of p-GaN HEMTs. **(a)** Drain and gate currents with respect to the gate bias at drain biases of 1 V (in blue) and 10 V (in red). **(b)** transconductance (g_m) characteristics.

Table 1.4 summarises the threshold voltage and the maximum drain saturation current (I_{DMAX}) of the state-of-the-art normally-off GaN HEMT with p-GaN cap layer. Generally, p-GaN cap layer is able to provide threshold voltage of more than 2V, yet the I_{DMAX} is not as high as the gate recess techniques due to the weaker control to the 2DEG from the gate contact through the thick p-GaN cap layer. In addition, the p-GaN/AlGaN junction will be forward biased before the gate drive voltage is large enough to induce high I_{DMAX}.

Table 1.4 The threshold voltage (V_{TH}) and maximum drain current (I_{DMAX}) for state-of-the-art GaN devices utilising p-GaN cap layer. The differences between the V_G and V_{TH} when I_{DMAX} are also shown in the table.

Reference	**Device Features**	**V_{TH}**	**I_{DMAX}**
[20]	Source-connected p-GaN gate	+2.44V	320mA/mm (@V_G−V_{TH}=4.56V)
[7]	p-GaN with Tungsten Schottky gate	+3.03V	220mA/mm (@V_G−V_{TH}=4.97V)
[8]	p-GaN with carbon doped buffer and AlGaN back-barrier	+1.1V	350mA/mm (@V_G−V_{TH}=3.9V)

The major issue for p-GaN gate is the difficulty of dopant activation. There are three reasons for low p-type dopant activation within GaN. Firstly, the activation energy of Mg dopant in GaN is very high (E_A =136~160 meV [21]). Secondly, Mg acceptors within GaN can be passivated through the formation of clusters with oppositely charged nitrogen vacancy (Mg-V_N) [22] Lastly, the Mg acceptors can also be passivated by the formation of electrically inactive Mg-H bonds with hydrogen atoms [23]. Hence, post-growth thermal annealing under N_2 or H_2 environment to compensate the nitrogen vacancy or hydrogen bonds and release Mg dopant is required for Mg to be effectively activated into free holes. The highest reported hole concentration was ~1×10^{18} cm^{-3} [24], regardless of the amount of Mg dosage.

1.3.3 Fluorine plasma treatment

As illustrated in Section 1.3.1, gate recess technology introduces surface damage that reduces the mobility and increases the gate leakage current. Therefore, [9, 25] have reported an alternative recess-free fluorine treatment technique by CF_4-based PECVD that implants fluorine ions into the AlGaN barrier at the gate region. When fluorine atoms are incorporated into AlGaN, they tend to absorb one free electron and behave as negative ions as fluorine has strongest electronegativity amongst all other elements. Due to the tight lattice structure in AlGaN/GaN heterostructures, most fluorine ions tend to stabilize at the interstitial sites by the repulsive force from neighbouring ions if the F is incorporated in AlGaN. Hence, the local potential within AlGaN is modulated and an extra barrier ϕ_F is introduced, as illustrated in the conduction band profile in Fig. 1.13 (b). Such modulation depletes the 2DEG at the AlGaN/GaN interface and achieves normally-off operation. The advantages of fluorine plasma treatment on achieving normally-off operation are the simplicity to control and the accessibility to the equipment. The fluorine plasma treatment normally uses RIE with F-based gas, which is widely available in the semiconductor industry and normally applied in SiO_2 etching process. It is also found that there is a direct relationship between the amount of incorporated negative charge and the 2DEG depletion field by the fluorine plasma treatment. Therefore, it is theoretically possible to obtain high V_{TH} by simply increasing the concentration of incorporated negative charge.

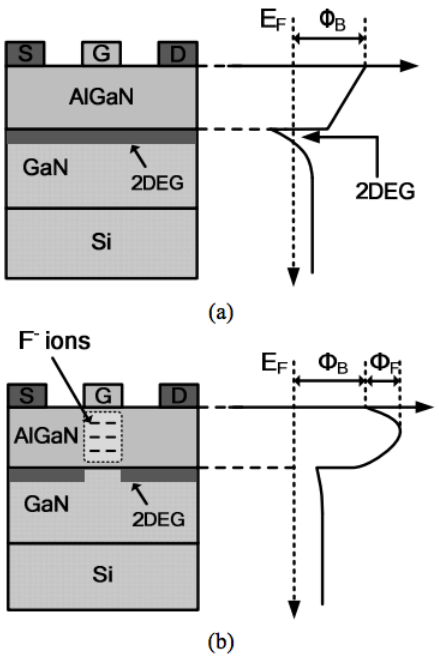


Fig. 1.13 Cross-sectional schematics and the conduction energy band of **(a)** standard normally-on and **(b)** fluorine-treated device [25]

Fig. 1.14 reports the relationship between the threshold voltage and RF plasma power and treatment time [9]. The V_{TH} increases with the rise of plasma power or the treatment time, and the maximum V_{TH} can be obtained is +0.9V.

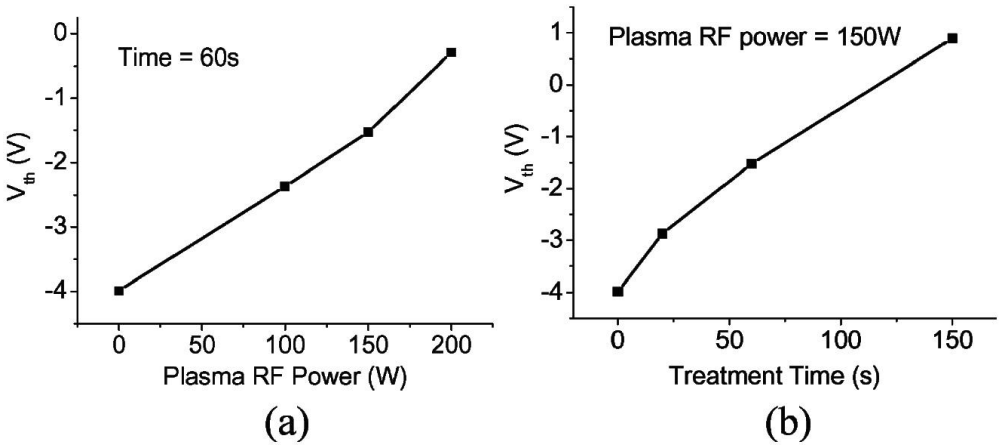


Fig. 1.14 The variations in the threshold voltage of the HEMT devices after the fluorine treatment with different **(a)** plasma power and **(b)** treatment time [9]

For the latest techniques utilising fluorine treatment, several approaches have been applied to enhance the V_{TH} and I_{DMAX}. For instance, a dielectric layer was applied after the fluorine treatment to reduce the surface damage and

preserve the material quality [26]. Table 1.5 demonstrates the V_{TH} and I_{DMAX} for the state-of-the-art GaN devices with fluorine treatment.

Table 1.5 The threshold voltage (V_{TH}) and maximum drain current (I_{DMAX}) for state-of-the-art GaN devices utilising fluorine treatments. The differences between the V_G and V_{TH} when I_{DMAX} are also shown in the table.

Reference	**Device Features**	**V_{TH}**	**I_{DMAX}**
[27]	$LaLuO_3$ for gate dielectric	+0.6V	400mA/mm (@V_G−V_{TH}=1.9V)
[28]	Si_3N_4 protected the gate during fluorine treatment and removed before gate metal deposition	+1.8V	380mA/mm (@V_G−V_{TH}=3.2V)
[29]	GaN device on SOI wafer	+0.9V	300mA/mm (@V_G−V_{TH}=1.6V)

The disadvantages of fluorine plasma treatment are mainly the concentration of incorporated fluorine and the thermal stability of negatively charged ions. As reported in Fig. 1.14, the V_{TH} (i.e. the concentration of incorporated negative charge) is increasing with higher RF power or longer treatment time. However, both parameters have to be constrained to ensure the 2DEG channel is protected from ion bombardment during the plasma treatment. Such trade-off prevents the device from achieving a high V_{TH} with good on-state conductivity. It is also reported that the V_{TH} of devices fabricated with fluorine treatment is unstable at higher ambient temperature. Detailed discussion will be made in Section 1.5.

Table 1.6 compares the advantages, disadvantages and device performance parameters for all of the gate design techniques reported in Section 1.3. Amongst all, the fluorine treatment has the potential to produce very high V_{TH} with a good I_{DMAX} if sufficient negative charge can be introduced in the gate region and confined above the AlGaN/GaN interface.

Table 1.6 Comparison of the advantages and disadvantages for the gate treatment techniques and their V_{TH} & I_{DMAX} reported in Section 1.3 to achieve normally-off operations

	Advantages	**Disadvantages**	**Latest Reported V_{TH}**	**Latest Reported I_{DMAX}**
Gate Recess	Easy to fabricate and control	Surface damage degrades 2DEG mobility and introduces traps	+1.7V [16] +1.65V [17]	500mA/mm [16] 650mA/mm [17]
	High I_{DMAX} after surface passivation	Low V_{TH}		
p-GaN cap	High V_{TH}	Difficult Mg dopant activation	+2.44V [20] +3.03V [7]	320mA/mm [20] 220mA/mm [7]
	Gate surface protected	Require extra epitaxial deposition process		
		Poor gate control due to thick p-GaN		
Fluorine plasma treatment	Easy to fabricate and control	May damage the lattice in channel region	+0.6V [27] +1.8V [28] +0.9V [30]	400mA/mm [27] 380mA/mm [28] 300mA/mm [30]
	Higher I_{DMAX} than p-GaN	Lower V_{TH} than p-GaN		
	Potentially can obtain high V_{TH}	Poor V_{TH} thermal stability		

1.4 Effect of charge trapping to the V_{TH} of AlGaN/GaN HEMTs

Even though GaN-based HEMT is a promising candidate for power electronics application due to its wide bandgap, high 2DEG carrier density and high mobility, the defects at the AlGaN surface, AlGaN/GaN interface, or the bulk of the gate dielectrics behaves as trap sites for free-moving charge and may affect the device performances.

The traps located between the gate contact and the 2DEG will alter the threshold voltage of the device [31]. An example is the fluorine-treated HEMTs reported in Section 1.3.3, which utilised trapped electrons by fluorine plasma treatment to deplete the 2DEG and achieve normally-off operations. However, even there is no plasma treatment applied to the gate, the unintentionally

introduced defects also affect the V_{TH}. According to the Fig. 1.15 extracted in [31], direct relationship is found between the V_{TH} hysteresis (ΔV_{TH}) and the maximum gate voltage during the I_D-V_G bi-directional sweep. Referring to Fig. 1.15 (b), a maximum V_{TH} hysteresis of 1V is found when maximum V_G is stressed to 9V.

The increase in the hysteresis at higher $V_{GS,max}$ is explainable by the variations in the energy band during the bi-directional sweep, extracted from [31] and shown in Fig. 1.16. In Fig. 1.16 (a), when V_G is increasing, the electrons from 2DEG are emitted and trapped at the Al_2O_3/GaN interface due to the field induced by positive V_G. These trapped charge behaves as a parasitic capacitor, $C_{trap\text{-}filling}$, connected in parallel with the 2DEG parasitic capacitance (C_{2DEG}). As shown in Fig. 1.16 (b), when V_G has reached its maximum and starts to decrease, the electrons trapped at the Al_2O_3/GaN interface are emitted after a period of time. Therefore, if the sweep time is faster than the trap emission time, the electrons at the interface will provide an extra field to deplete the 2DEG. Therefore, the V_{TH} is higher during the negative sweep.

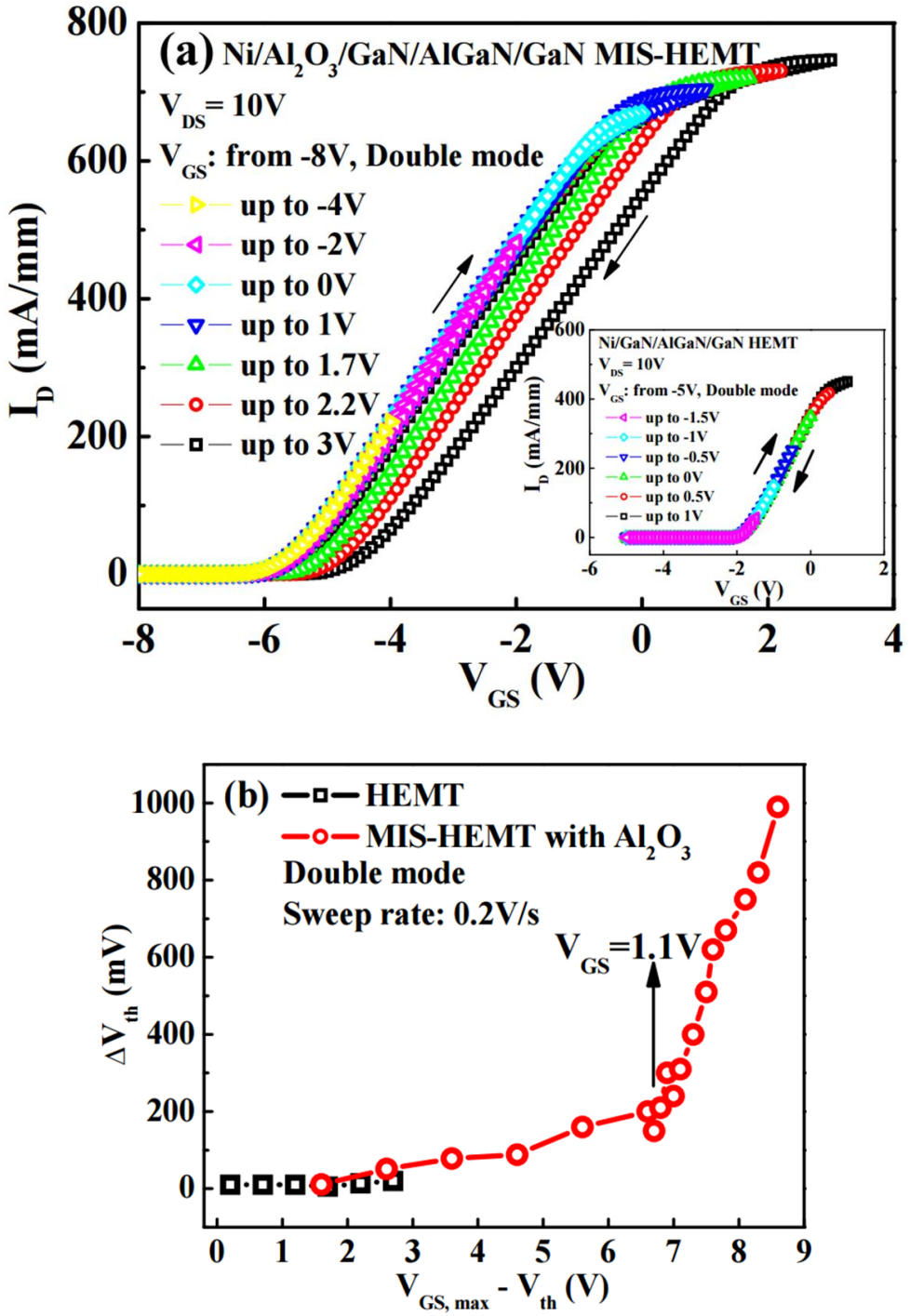


Fig. 1.15 (a) I_D-V_G transfer characteristics of Ni/Al_2O_3/GaN/AlGaN/GaN MIS-HEMTs and corresponding HEMTs with increasing $V_{G,max}$. **(b)** The relationship between ΔV_{TH} and $V_{G,max}$− V_{TH} for reported HEMT and MIS-HEMT [31]

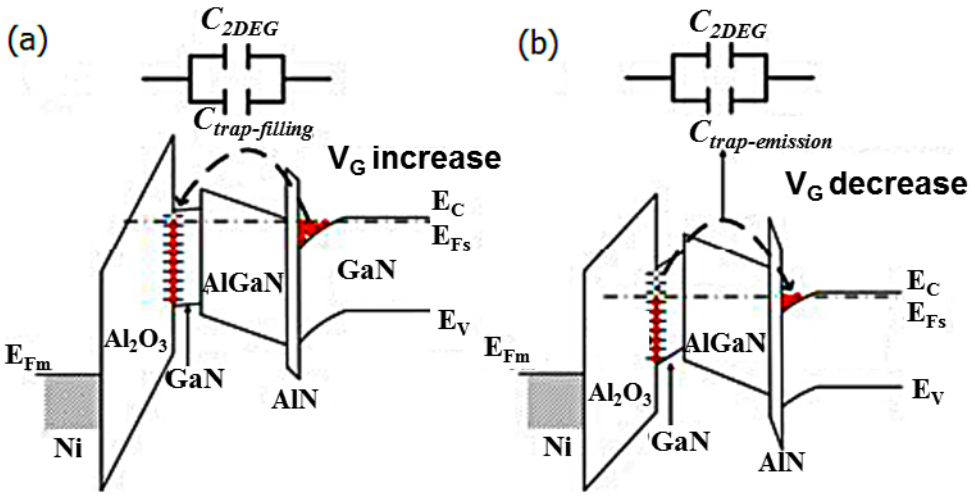


Fig. 1.16 Schematic band diagrams and equivalent circuits of MIS-diode when V_G is **(a)** increasing and **(b)** decreasing [31]

The model for the trap emission time from a certain trap state is expressed in Eq. (1.9), where σ_n is the capture cross section for holes, v_T is the electron thermal velocity, N_v is the effective density of states in the valence band, E_T is the energy depth of the trap states, and T is the ambient temperature. According to Eq. (1.9), the trap emission time at E_T is shorter at high temperature. In other words, the same trap emission time under higher ambient temperature will release the traps located at deeper levels than the ones at room temperature. Such effect affects the V_{TH} stability at high-temperatures, especially for the normally-off devices using fluorine plasma treatment as their gate processing technique. It will be further discussed in Section 1.5.

$$\tau_n(E) = \frac{1}{\sigma_n v_T N_v} \exp\left(\frac{E_T}{kT}\right) \tag{1.9}$$

1.5 V_{TH} thermal stability of fluorine plasma treated AlGaN/GaN HEMTs

The performance of the power device under high-temperature is important for power electronics applications as the system is usually implemented under

high ambient temperature. For instance, the power electronic system within the electric or hybrid electric vehicles located on the engine will have an ambient temperature of up to 200°C [10]. The V_{TH} thermal stability is one of the most important parameters for power devices as it directly influences the on/off characteristics and the current rating of the power system. A stable and high enough positive V_{TH} ensures the safety and performance of the system. In this section, the V_{TH} of AlGaN/GaN HEMTs with the fluorine treatment technique will be reviewed and compared.

An example of the V_{TH} thermal stability analysis is carried out on a normally-off HEMT fabricated with CF_4 plasma treatment on the gate at RF power of 150W for 150s [32]. According to the I_D-V_G characteristics of the device at 25°C and 375°C shown in Fig. 1.17, a 68% decrease of 0.76V to 0.24V is observed. It implies the stronger emission of trapped electrons from fluorine-induced trap states at higher temperatures.

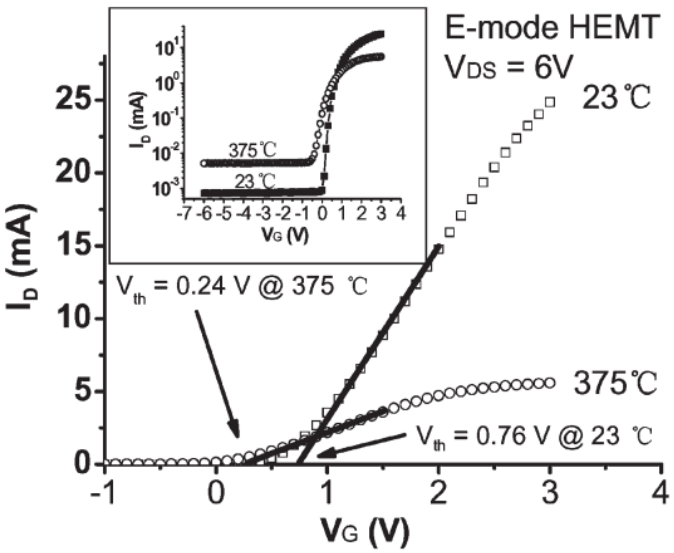


Fig. 1.17 I_D-V_G characteristics of normally-off (E-Mode) normally-off AlGaN/GaN HEMTs with a gate width of 100μm, operating at room temperature and 375°C [32]

It is also found that different techniques of fluorine incorporation lead to different V_{TH} thermal performances. The $Al_{0.28}GaN$ (22nm)/GaN (1.1μm) HEMT fabricated with CF_4 plasma or F ion implantation is reported in [33]. With CF_4 plasma treatment at RF power of 60W for 200s on the AlGaN barrier layer, the V_{TH} can be shifted from −3.1V to −0.9V at room temperature. If the AlGaN layer is processed with F ion implantation with a dose of 5×10^{12} cm^{-2} at 50 keV, the V_{TH}=−0.38V at room temperature. As shown in Fig. 1.19, the V_{TH} of CF_4-treated device will decrease from −0.9V to −1.6V at temperatures higher than 60°C. While for F ion implanted device, the V_{TH} can be maintained at −0.42V under 200°C. Due to the relationship between the trap level and the temperature indicated in Eq. (1.9), it is expected that most of the states with electrons occupied are relatively close to the conduction band (i.e. "shallow traps") if the F was introduced through plasma treatments. Therefore, the fluorine plasma treatment technique has to be replaced or optimised for improved V_{TH} thermal stability

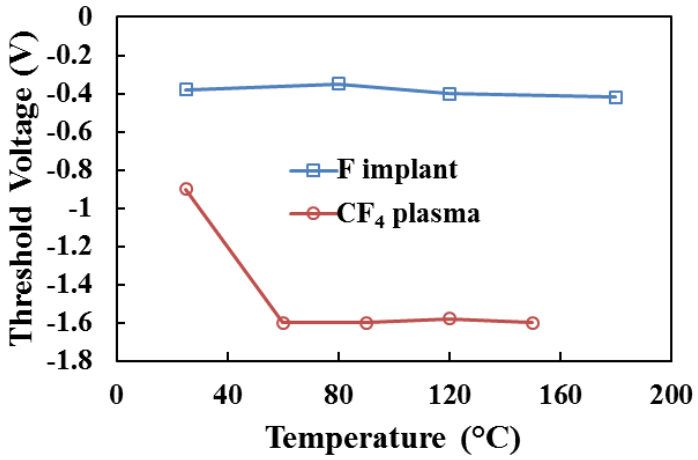


Fig. 1.18 Comparison of V_{TH} dependence on the ambient temperature for CF_4 plasma-treated and F-implanted AlGaN/GaN HEMTs [33]

1.6 Aims and objectives

The aim of this PhD thesis is the thorough study of the normally-off AlGaN/GaN HEMTs, including the design, simulation, fabrication and characterisation of the devices with special focus on the V_{TH} thermal stability. This PhD study offers deep understanding on the high-temperature device physics and possible solution to the future application of GaN-based HEMTs within a power electronic circuit under high ambient temperature.

In this thesis, the underlying physics on the influence of high temperature on the HEMTs was investigated with the optimisation of existed room-temperature analytical models. In order to fabricate a functional Al_2O_3/AlGaN/GaN power HEMTs with high V_{TH}, multiple fluorine plasma treatments combined with partial AlGaN recess were implemented with detailed analysis of the fluorine-induced trap distribution within the gate dielectrics. Finally, the understanding of the trap distribution and its relationship to V_{TH} thermal stability leaded to the successful design, fabrication and characterisation of an Al_2O_3/AlGaN/GaN-based normally-off MIS-HEMT with novel Argon pre-fluorination plasma treatment. The device maintained high V_{TH} of 2.5V at up to 200°C, which is the highest reported using the fluorine plasma treatment technology.

1.7 Thesis organisation

The thesis consists of 8 chapters, including the introduction as Chapter 1. The tools used for the simulation, fabrication and characterisation of the thesis are discussed in Chapter 2 with brief explanations of their operating principles. The major work of the thesis is documented in Chapters 3~7.

Firstly, in order to have a better understanding on the effect of high ambient temperature to the performance of AlGaN/GaN HEMTs, the steady state characterisation and modelling of AlGaN/GaN HEMT with temperatures up to 500K are carried out and is discussed in Chapter 3. By modifying the reported analytical model on AlGaN/GaN HEMTs to become temperature-dependent, the variations in the physical parameters at high temperatures such as the Schottky barrier height, 2DEG density, V_{TH}, specific contact resistance, subthreshold slope and the I_D-V_D characteristics are verified. This work is important for power device performance prediction and power circuit design because many applications in the power electronics systems are under high temperature environment.

In addition, the devices used for power electronics require high V_{TH} to ensure the system safety, standby power reduction and surge protection. In Chapter 4, the fabrication and characterisation of normally-off Al_2O_3/AlGaN/GaN power MIS-HEMTs with partial gate recess and multiple fluorine treatments to obtain high V_{TH} are realised. Based on the knowledge of the origin of 2DEG proposed in Chapter 3, the partial gate recess reduces the 2DEG density yet preserves the 2DEG carrier mobility. The multiple low-power fluorine plasma treatments on different ALD-Al_2O_3 gate dielectric layers enhance the fluorine-induced trapped negative charges within the gate dielectric significantly. Meanwhile, a monolithic logical inverter is also reported by integrating the abovementioned normally-off MIS-HEMT with a normally-on MIS-HEMT without any gate recess or fluorine plasma treatment. The inverter

has a large output swing and fast switching speed, making it possible for power integrated circuit application.

However, the high-temperature V_{TH} of the normally-off MIS-HEMT using the gate processing techniques reported in Chapter 4 decreases significantly due to the emission of the negative charges trapped at the Al_2O_3 gate dielectric. The depletion field to the 2DEG underneath the gate is weakened with the decrease in trapped negative charge concentration. In Chapter 5, the thermal emission of negative charges trapped at the Al_2O_3 gate dielectric is modelled and characterised. The distribution of the trap states along the Al_2O_3 energy band can be investigated by stressing the gate with various negative bias for a period of time. With such technique, the degradation of V_{TH} at high temperature can be related with the energy level that the trapped negative charge is located within the Al_2O_3 energy bandgap. Thus, the trap state distribution induced by fluorine treatments can be derived. It is also found that the higher fluorine plasma treatment power result in the accumulation of trapped negative charges at deeper energy level. Hence, more trapped charges remain in the trap sites at high temperatures.

As it is observed in Chapter 5, higher fluorine plasma power generates deeper trap states and thus obtain better V_{TH} thermal stability. It suggests that introducing a certain degree of damage to the Al_2O_3 surface creates traps within deeper energy levels. Therefore, in Chapter 6, a short Argon pre-fluorination treatment is implemented to break more Al-O bonds on the surface of Al_2O_3 prior to the fluorine treatments. The increased amount of surface dangling bonds enhances the Al-F bond formation during the subsequent fluorine plasma

treatment. Meanwhile, the multiple fluorine plasma treatments by conventional RIE is replaced with single treatment using ICP-RIE. The ICP-RIE is able to control the fluorine flux and the bombardment energy independently, thus obtain high concentration of incorporated fluorine without damaging the 2DEG channel quality. Using the gate-stressing technique reported in Chapter 5, the location of the peak of the trap states is shifted further away from the conduction band after the argon pre-fluorination treatment.

The physical mechanism of the argon pre-fluorination treatment is further discussed in Chapter 7. According to the SIMS measurement on the fluorine depth profile, the argon pre-fluorination treatment can effectively increase the peak of the F atoms and shift the peak location closer to the surface. The decline in the O atoms also showed the replacement of O atoms by the F atoms within Al_2O_3. With XPS characterisation, it is found that the argon pre-fluorination treatment has effectively increased the amount of Al-F bonds at the Al_2O_3 surface. The link between the increase in Al-F bonds and the amount of deeper level traps is verified by the Gaussian 09 molecular simulation tools. The simulated trap state distributions of the samples with and without argon pre-fluorination treatment agree with the ones obtained from the gate-stressing measurements. It is also found in the simulation that the formation of F-Al-F bond by argon pre-fluorination treatment also attributed to the generation of deeper traps.

Finally, the thesis is concluded in Chapter 8 with recommendations on the future research.

CHAPTER 2 Device Simulation, Fabrication and Characterisation Techniques

The work reported in this thesis involves simulation, fabrication, and characterisation of both the normally-on and normally-off AlGaN/GaN metal-insulator-semiconductor (MIS) HEMTs.

The device simulation carried out by Synopsys Sentaurus TCAD simulation [34-36] tools not only visualised the inherent physical properties of the devices, but also assisted in the design of novel devices. For instance, the investigation of the temperature dependence on the AlGaN/GaN HEMT performance reported in Chapter 3 used the Sentaurus device simulation to understand the variations in the Schottky barrier height, 2DEG density, and the threshold voltage (V_{TH}) at higher temperatures. They provide alternative and reliable indicators with the terminal measurement results to verify the accuracy of the analytical models proposed. In addition, in Chapter 4~6, the device simulation played an important role on determining the amount of negative charge trapped within the Al_2O_3 gate dielectric after the fluorine plasma treatments on the gate. These simulated values are essential for the design of the fluorine treatment recipes to obtain high V_{TH}. The simulation is also important for the extraction of the energy levels of traps where these negative charges are trapped within the gate dielectric. Detailed introduction on the Sentaurus device simulation tool is discussed in Section 2.1 and the sample run script for the normally-off Al_2O_3/AlGaN/GaN MIS-HEMTs with fluorine plasma treatments is demonstrated in Appendix I with brief explanations on the scripts.

The facilities used in the fabrication process include the photolithography mask aligner for pattern development, wet bench for sample cleaning and photoresist removal, electron-beam (e-beam) evaporator for metal deposition, rapid thermal annealing (RTA) for material recovery or ohmic contact formation, reactive ion etcher (RIE) for SiO_2 dry etching and fluorine plasma treatments reported in Chapter 4 and 5, inductively coupled plasma-RIE (ICP-RIE) for AlGaN & GaN dry etching together with F & Ar plasma treatment reported in Chapter 6 and 7, plasma-enhanced chemical vapour deposition (PECVD) for SiO_2 deposition and atomic layer deposition (ALD) for Al_2O_3 gate dielectric deposition. Detailed operating principles of these instruments are described in Section 2.2. Specific parameters used for the device fabrication are listed in Appendix II.

In order to understand the performance and the underlying physics of the fabricated devices, characterisations on the electrical performance, surface morphology, material composition and material bonding were carried out. These characterisations require the usage of power device analyser station, atomic force microscopy (AFM), scanning electron microscopy (SEM), secondary ion mass spectroscopy (SIMS), and X-ray photoelectron spectroscopy (XPS), respectively. Detailed operating principles of these instruments are described in Section 2.3.

2.1 Simulation of AlGaN/GaN MIS-HEMTs

The device simulation is a useful tool to understand the inherent physical properties and assist in the device design. The simulation of the AlGaN/GaN devices in this thesis was conducted by the Synopsis Sentaurus TCAD

simulation tools [34, 35], and the simulation process can be summarised as a flowchart shown in Fig. 2.1.

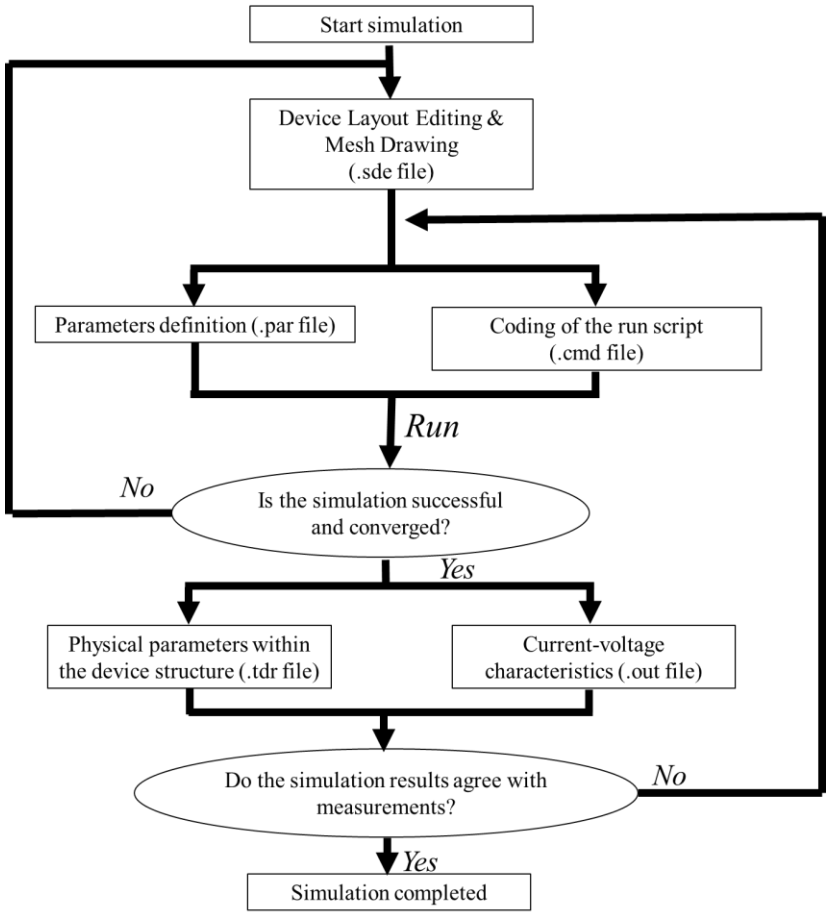


Fig. 2.1 The flowchart for AlGaN/GaN HEMT simulation procedures

The simulation begins with the drawing of the device structure with Sentaurus structural editor [35]. It can be either drawn through its graphical interface or coding. After the device structure drawing, the mesh is automatically drawn according to the assigned conditions in the structural editor. The physical models assigned in the Sentaurus Device simulation are calculated in every single mesh and these solutions are examined with the adjacent mesh to ensure they are converged [35]. Therefore, proper design on the mesh dimension is important to carry out converged and reliable results. Generally, the number of mesh used in the simulation is directly proportional to the

simulation time. However, convergence failure encounters if coarse mesh was placed at the region where abrupt change occurred. As a rule of thumb for the AlGaN/GaN HEMT simulations, very fine mesh is required at the metal contact edges and the device surface as the electric field is usually high at these regions. Additionally, fine mesh at the vertical direction is required at the material interfaces, especially at the AlGaN/GaN interface where 2DEG is present. To avoid long computation time, coarser mesh is acceptable at the other regions. An example for the layout of unbiased fluorinated Al_2O_3/AlGaN/GaN MIS-HEMT simulation with mesh is shown in Fig. 2.2. The distribution of the electron density (labelled as eDensity) is shown in colour, and successful 2DEG depletion (i.e. very low electron density at the AlGaN/GaN interface) underneath the fluorinated Al_2O_3 gate dielectric is observed.

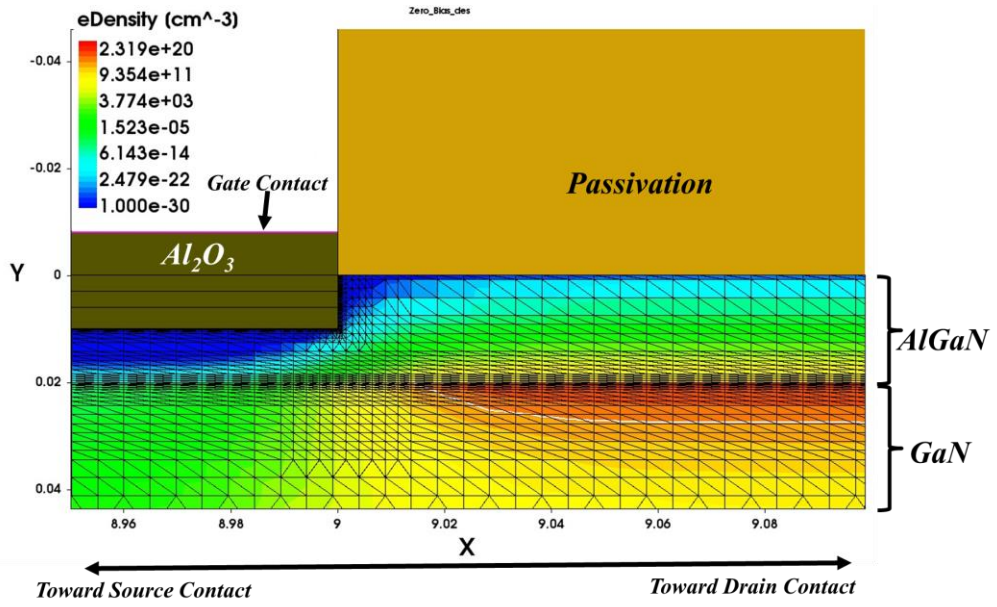


Fig. 2.2 The mesh and electron density distribution within the normally-off Al_2O_3/AlGaN/GaN MIS-HEMT device simulation at the edge of the gate towards the drain contact. V_G=V_D=0V.

With proper design of the device structure and the mesh, the Sentaurus Device run script (named with .cmd file extension) can be implemented to

simulate the device performance under a range of circumstances. The run script consists of the physical models included in the numerical solution of the device, the desired output parameters and the mathematical configurations for the simulation. Based on the Sentaurus template script of conventional normally-on AlGaN/GaN HEMTs simulation issued in [36], the Sentaurus Device run script used for normally-off Al_2O_3/AlGaN/GaN MIS-HEMTs with multiple fluorination plasma treatment used in Chapter 4 and 5 is attached in Appendix I. To obtain normally-off operation, the fluorine-induced negative charges are simulated as fixed interfacial charges at the designed locations, and the 2DEG concentration of the partially recessed AlGaN is obtainable from the weakened polarization field strength in the run script. These parameters are calibrated from the measured current-voltage characteristics to ensure the simulation is reliable before being used for the design. Detailed design process of the fluorine-treated normally-off device simulation is discussed in Chapter 4.

In order to link the script with reality and make the simulation outcome reliable, the parameters of the simulated materials used in the run script are defined in the parameter file with .par file extension. The physical parameters used in the simulations for Al_2O_3, AlGaN, GaN and AlN layers are the default values provided by the software [35].

If the script runs successfully without convergence failure, the output file with current-voltage characteristics from the contact terminals (labelled with .out file extension) and the mesh file with calculated physical characteristics (labelled with .tdr file extension) at any locations within the device will be generated. For example, the distribution of the electrons at the

$Al_{0.25}GaN$ (20nm)/GaN interface without any external bias shown in Fig. 2.3 can be extracted from the simulation. By integrating the electron density distribution near the AlGaN/GaN interface, the 2DEG density of the device can be calculated. It is about 8×10^{12} cm^{-2}, which is similar to the 2DEG density of the same wafer characterised from the Hall measurement [37].

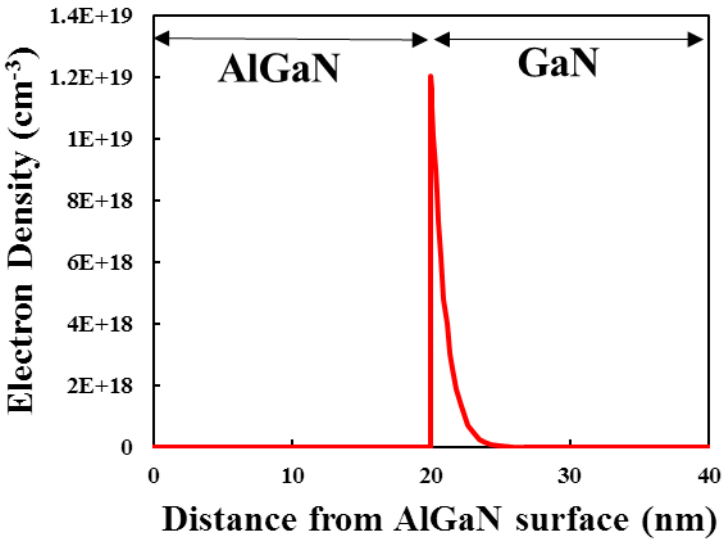


Fig. 2.3 The vertical electron density distribution near the $Al_{0.25}GaN$/GaN interface. The thickness of AlGaN is 20nm.

To verify the simulation configuration, a common device structure is simulated and compared with the experimental data. Such calibration step is essential before simulating the devices with novel structures. The calibration is achieved by reasonably adjusting the parameters. For example, in the device simulation used for Chapter 4~6, the simulation is calibrated with a partial recessed normally-on AlGaN/GaN MIS-HEMT reported in Section 4.3 and [37] before the design of the fluorine plasma treatments. By reducing the electron mobility of the 2DEG under the gate from 1450 $cm^2/V{\cdot}s$ to 1200 $cm^2/V{\cdot}s$, a good fit of the current-voltage characteristics between the simulated and measured devices is obtained and shown in Fig. 2.4. Such a good fit with the I_D-

V_D characteristics ensures the reliability of the parameters and models used for the simulation. Therefore, the negative charges placed within the Al_2O_3 are able to mimic the fluorine plasma treatments by fitting the simulated V_{TH} with the ones obtained in the measurement.

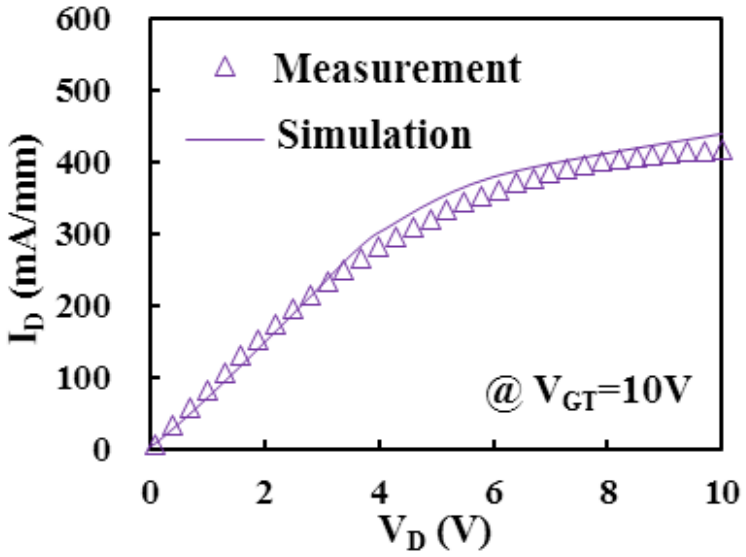


Fig. 2.4 The fitting between the measurement and simulation results for the I_D-V_D characteristics of Al_2O_3/AlGaN/GaN MIS-HEMT with 10nm AlGaN partial recess at the gate region. The measurement was conducted when $V_{GT}=V_G-V_{TH}=10V$.

2.2 Facilities used for AlGaN/GaN MIS-HEMT fabrication

The fabrication process of the normally-on and normally-off AlGaN/GaN MIS-HEMTs can be summarised as a flowchart shown in Fig. 2.5. The detailed run sheet and parameters used for the device fabrication in Chapter 3~7 are listed in Appendix II.

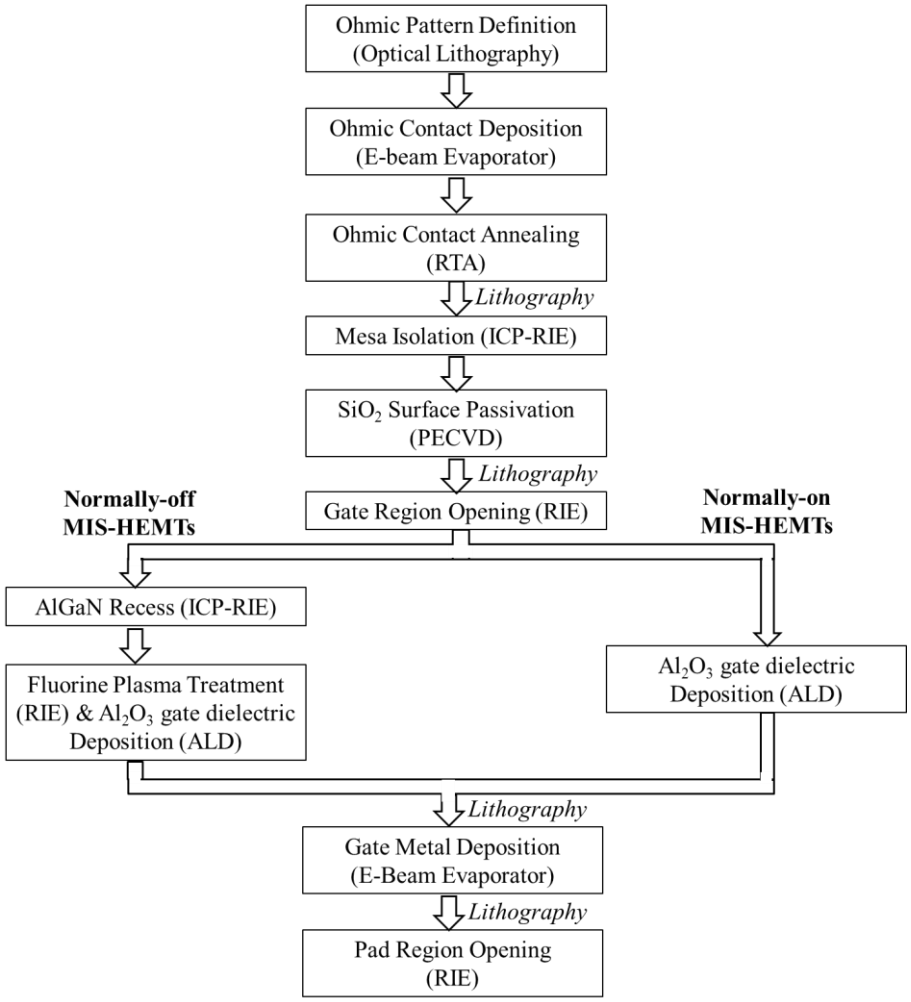


Fig. 2.5 The process flowchart for normally-on and normally-off Al_2O_3/AlGaN/GaN MIS-HEMTs fabrication.

The optical lithography is the most commonly used technique for pattern definition in the semiconductor industry [38]. It transfers the pattern defined on a photomask to the sample surface with the usage of organic light-sensitive photoresist. The photoresist exposed to UV radiation changes its solubility in a developer. It can either become more soluble (positive) or less soluble (negative) after light exposure. A positive photoresist AZ-5214E was used in this thesis, as it provides better resolution than most of the negative resists. Another feature for the AZ-5214E is its image reversal property, which forms undercuts on the developed sidewalls. The sidewall undercuts shown in Fig. 2.6 are ideal for

metal lift-off purposes [39]. The image reversal is obtained by a special insoluble crosslinking agent in the resist which is activated at 110°C baking after the first light exposure, while the unexposed area is behaved the same as the regular positive resist. After the flood exposure without any mask, the region where was exposed under the first illumination is remained on the sample with undercuts after development. Hence, the image on the mask should be designed as the reverse of the desired pattern. The principle of image reversal is demonstrated in Fig. 2.7 [40].

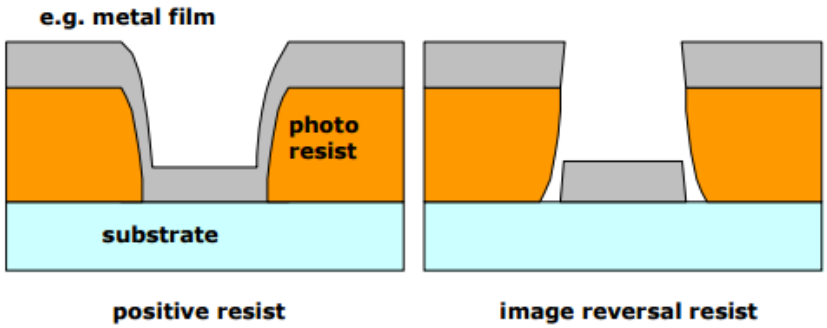


Fig. 2.6 The sidewall of the developed positive resist and the image reversal. The undercut of the sidewall made the metal lift-off more effective as the discontinuity of the metal film at the sidewall allows for complete resist strip-off [39]

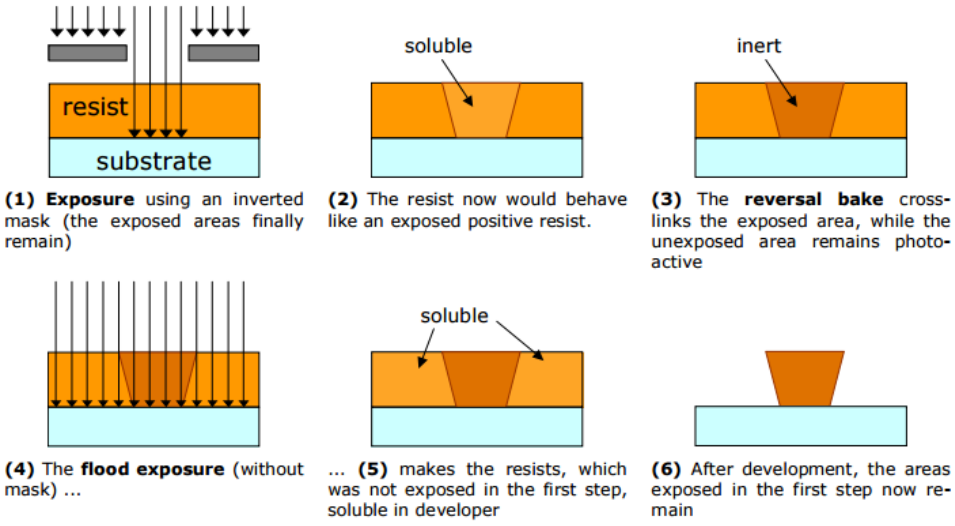


Fig. 2.7 The operating principles for the image reversal resist [40]

The reactive ion etching (RIE) is a commonly used dry etching technique that combines the chemical and physical etching on the surface to provide good selectivity and anisotropy. The RF power source in the RIE system is able to generate a strong electromagnetic field that dissociates the inlet gas molecules into electrons, ions, and chemically-active radicals. As ions do not have high enough mobility to keep up with the changing of the RF field, less ions than electrons are collected at the plates, which result in negative bias in both plates [41]. Therefore, the samples, which are placed on the plate, receive continuous bombardment from the ions during RIE.

For instance, the etching of SiO_2 with RIE involves in the usage of fluorine-based gas to dissociate the F radicals and react chemically with the SiO_2. Argon inert gas is also introduced to remove the surface residuals through Ar ion bombardment. In this thesis, CHF_3 gas is used due to laboratory conditions. In the RIE system with RF power supply, the CHF_3 will be dissociated into CH_xF_y, HF_x, and F radicals. Among these, F radicals are very reactive F atoms with incomplete outer electron shells. These F radicals tend to react with SiO_2 and form gaseous SiF_4 and O_2. The total reaction is shown in Eq. (2.1). The recipe used for SiO_2 etching in the thesis is the default recipe provided by the laboratory and is demonstrated in Table A-8 of Appendix II. SiO_2 etching speed of 43nm/min is obtained from this recipe referring to the Scanning Electron Microscopy (SEM) cross-sectional image.

$$\mathbf{4F+SiO_2 \rightarrow SiF_4+O_2} \quad (2.1)$$

Similarly, Cl-based gases (e.g. BCl_3 and Cl_2) are used as effective etchants for AlGaN and GaN based on the formation of volatile $GaCl_3$ after the reaction

[42, 43]. In this thesis, they have been used for mesa and partial AlGaN gate recess reported in chapters 4~7. The AlGaN gate recess recipe is based on the existing AlGaN etching recipe provided in the laboratory. Lower RF power is applied to ensure proper control of the shallow recess. The AlGaN gate recess speed is verified by the surface profile of Atomic Force Microscopy (AFM) summarised in Fig. 2.8. According to the AFM profile illustrated in Fig. 2.8(b), 30s of plasma etching induces 9.7nm of AlGaN recess. A smooth profile of surface roughness less than 1nm is observed from the AFM surface image.

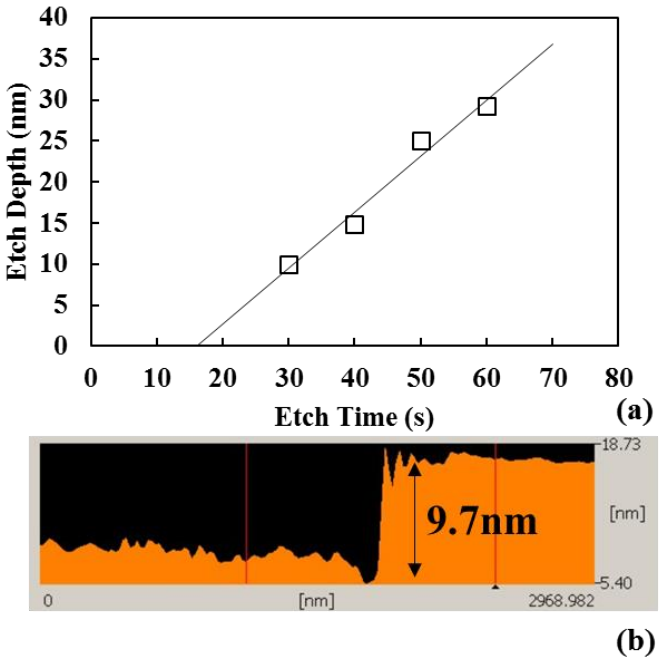


Fig. 2.8 (a) The summary of AlGaN etching depth using the AlGaN recess recipe reported in Table A-9 of Appendix II. **(b)** The AFM profile of the AlGaN surface underwent 30s of AlGaN recess. About 9.7nm AlGaN recess is obtained.

Due to the existence of fluorine radicals by using CHF_3-RIE, it is possible to use this technique for normally-off Al_2O_3/AlGaN/GaN MIS-HEMTs application. Since F does not form volatile products with Al-based materials, the F radicals can be trapped within the Al_2O_3 and form negative charges [37]. These negative charges are able to deplete the 2DEG underneath the

AlGaN/GaN interface and increase the V_{TH} of the MIS-HEMT. Detailed design of the plasma treatment recipes is explained in Chapter 4 and 6.

The RF power within a conventional RIE system not only controls the amount of F radicals induced in the plasma, but also affects the bias (i.e. the ion bombardment energy) on the plate. Therefore, even though using higher RF power to increase the concentration of F radicals is essential to improve the V_{TH} for the MIS-HEMT, the higher ion bombardment energy may degrade the 2DEG quality and device reliability. To overcome such trade-off, inductively coupled plasma (ICP) RIE was used for gate plasma treatments in Chapter 6 and 7. The schematics of a ICP-RIE system is shown in Fig. 2.9. The most significant difference between ICP-RIE and RIE systems is the independent RF control on the coil (which controls the concentration of radicals and ions) and the cathode (which controls the ion bombardment energy). Therefore, it is possible for the ICP system to obtain high F radical concentration and remain low ion bombardment energy to protect the 2DEG conductivity.

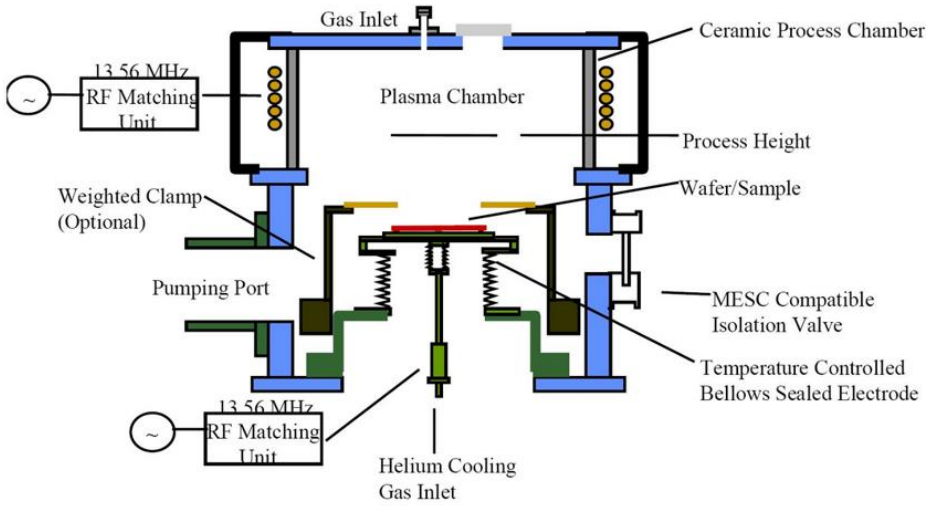


Fig. 2.9 Schematic diagram of the ICP-RIE system [44]

The chemical vapour deposition (CVD) is a film deposition process involves in chemical reactions [45]. It is usually used for the deposition of SiO_2 passivation with SiH_4 and N_2O as the reactant gas. The overall reaction is shown in Eq. (2.2), where H_2 and N_2 are the by-products of the reactions which can be easily desorbed from the surface.

$$SiH_4+2N_2O \rightarrow SiO_2+H_2+2N_2 \quad (2.2)$$

The rate of the film deposition depends on the CVD temperature, and the film growth rate is faster at higher temperature. Normally, for the growth of SiO_2 using SiH_4 and N_2O gas, the growth temperature has to be around 840-860°C [46]. However, such a high temperature may affect the ohmic contact quality on the sample as it is close to its annealing temperature. Alternatively, plasma-enhanced-CVD (PECVD) system was used in this thesis for SiO_2 deposition. The schematics of a typical PECVD system is shown in Fig. 2.10, in which the RF-powered electrodes induce a plasma in between to enhance the energy required to initiate the surface reaction. Consequently, the growth temperature can be significantly reduced without sacrificing the growth time. For example, the growth temperature of PECVD-grown SiO_2 is normally less than 400°C [47]. The SiO_2 deposition recipe used in the thesis is the default recipe provided in the laboratory, and is shown in Table A-7 of Appendix II. The SiO_2 deposition rate of the recipe is about 26nm/min, which was verified by the SEM cross-sectional image.

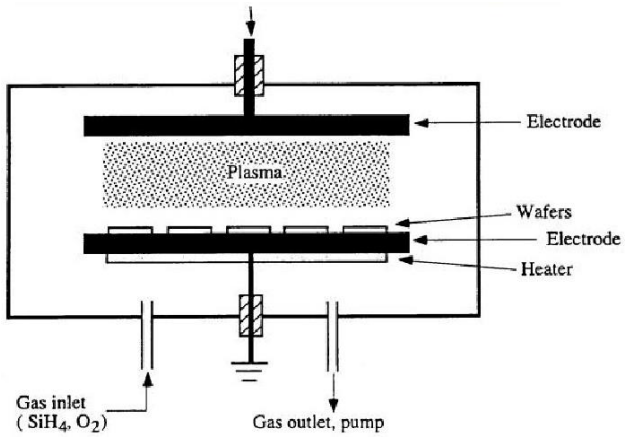


Fig. 2.10 Schematics of a typical PECVD system [45]

The atomic layer deposition (ALD) is a technique that enables very thin film depositions controlled in atomic level. In this thesis, ALD is used to deposit the Al_2O_3 gate dielectric due to its better quality and thickness control than PECVD. The deposition of Al_2O_3 in this thesis uses water and tri-methyl-aluminium (TMA) precursors to introduce pulses of water or TMA molecules as the source of Al and O atoms for Al_2O_3 formation. The overall reaction and process are shown in Eq. (2.3) [48] and Fig. 2.11 [49].

$$2Al(CH_3)_3+3H_2O \rightarrow Al_2O_3+6CH_4 \qquad (2.3)$$

In the schematic of ALD-Al_2O_3 growing process shown in Fig. 2.11, the silicon substrate is used as an example for demonstration, where hydroxide (OH) groups are formed at the surface due to air exposure. During the TMA precursor pulse, the TMA molecules react with the hydroxides and passivates the surface, where the CH_4 gas is formed as the by-product (Fig. 2.11 (b) and (c)). After purging nitrogen to evacuate the excessive TMA molecules in the chamber (Fig. 2.11 (d)), water precursor pulses are introduced to remove the CH_3 groups and create Al-O-Al bridges. CH_4 is formed again as the gaseous by-product (Fig. 2.10 (e) and (f)). Lastly, the unreacted H_2O and CH_4 are evacuated from the

chamber with nitrogen purge (Fig. 2.11 (g)). As in each cycle there is about one atomic layer deposited on the surface, the deposition rate of Al_2O_3 is about 0.1nm/cycle. The Al_2O_3 deposition recipe is reported in Table A-10 in Appendix II.

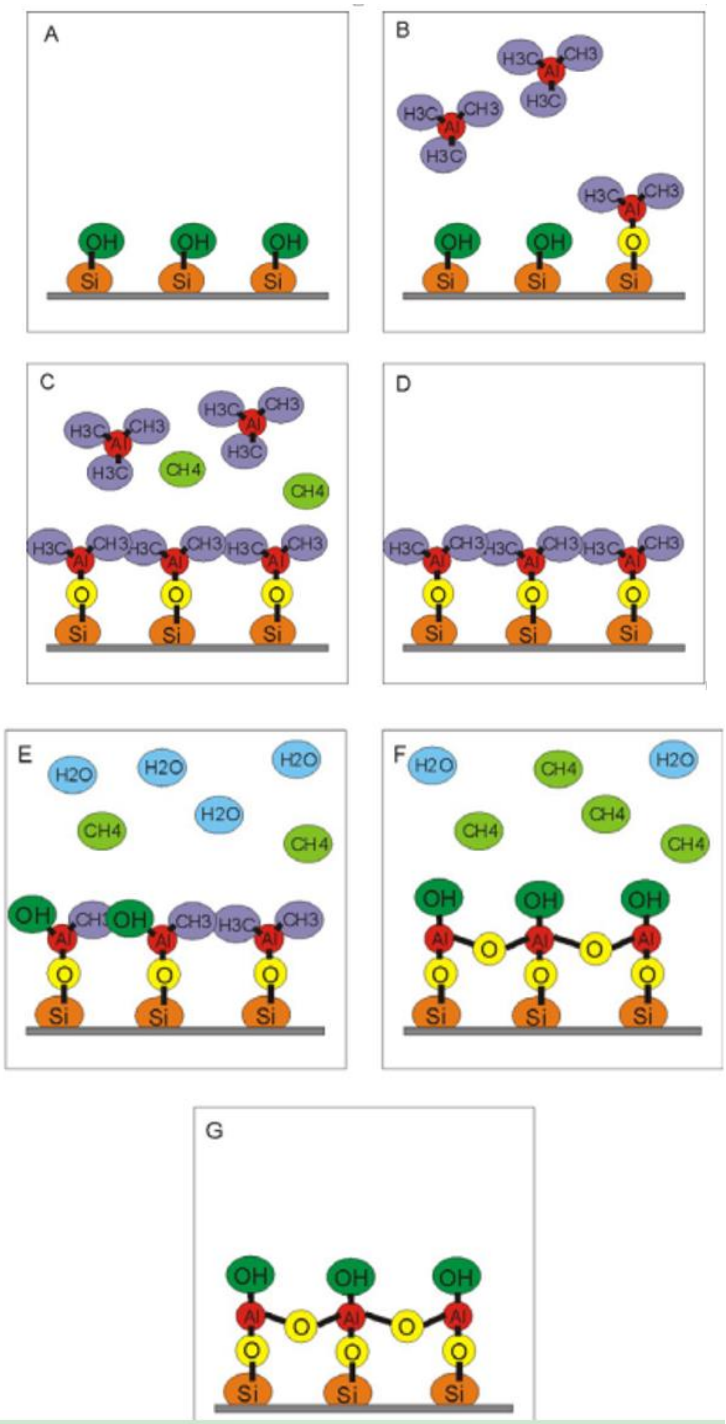


Fig. 2.11 Steps of depositing Al_2O_3 on Si substrate by Savannah 100 ALD system [49].

2.3 Facilities used for AlGaN/GaN MIS-HEMT characterisation

The characterisations of AlGaN/GaN MIS-HEMT include the electrical characterisation, the structure characterisation, and the material characterisation. The electrical characterisations in this thesis included all of the current-voltage analysis for threshold voltage, contact resistance, maximum drain current, and breakdown voltage. Those characterisations used the Agilent B1505A Power Device Analyser with a probing station and a hot plate. The structure characterisations in this thesis used the atomic force spectroscopy (AFM) for surface morphology analysis or shallow recess depth, and the scanning electron spectroscopy (SEM) for the cross-sectional view of the fabricated device. Lastly, the material characterisations involved in the application of secondary ion mass spectroscopy (SIMS) and the X-ray photoelectron spectroscopy (XPS) for the atomic depth profile and atomic bonding characterisations in the thesis respectively.

The AFM is a characterisation technique on surface profile and morphology. It uses a laser source to detect the deflection of a cantilever which attaches to a thin tip and sweeps the surface [50]. There are three scanning modes of the cantilever on the sample surface: contact, attractive, and tapping modes [51]. The contact mode, which the tip is always in contact with the sample and detecting the repulsive atomic force from the surface, provides the best resolution of the surface topology and the fastest scanning speed. However, it may damage the sample surface or the tip. The non-contact attractive mode utilised the attractive atomic force between the tip and the surface that made the tip resonant with the surface. It is a non-destructive method yet provides poor

resolution. The technique used for the AFM characterisation in the thesis is the tapping-mode, which the cantilever is vibrating at a certain frequency and amplitude to allow the tip to tap the surface during the sweep. A feedback control is also implemented to maintain the oscillation amplitude during measurement. Therefore, a good resolution of the surface topography with minimised surface damage can be achieved. The schematic layout of the tapping-mode AFM system is shown in Fig. 2.12.

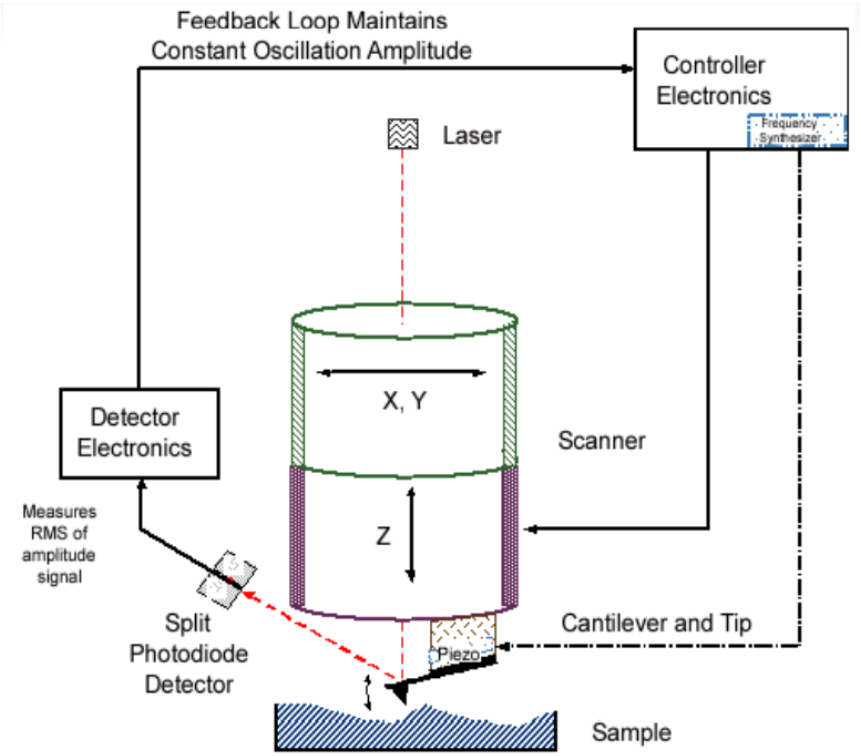


Fig. 2.12 Schematic diagram of the principles for the AFM tapping system [50]

The scanning electron microscope (SEM) is a commonly used system for nanoscale imaging. As shown in Fig. 2.13, the SEM has an electron gun as the source of the electron beam. After passing through the magnetic condenser lens and objective lens to adjust the electron beam concentration and diameter, the electrons reach the specimen and interact with the coulomb field of the nucleus

and electrons of the sample. The interaction can be categorised into inelastic and elastic interactions.

The inelastic interaction occurs when the electron beam interact with the electric field of the electrons in the sample [52]. The energy from the beam is transferred to the atoms on the sample and emit secondary electrons, which can be detected by the detector. Meanwhile, if the vacancies from the secondary electron are fulfilled by the electrons from higher orbitals, the excessive energy will either be emitted from the sample as X-ray or be transferred to other electrons in the atom and emit Auger electrons. The X-ray and Auger electrons can be collected by the detector and provide information about the surface material.

On the other hand, the elastic interaction occurs when there is no transfer in energy but only exchange in momentum between the electron beam and the atoms on the sample [52]. These electrons will scatter in the sample and may be deflected out to the specimen as the backscattered electrons. The backscattered electrons are collected by the detector and are used for surface topology imaging.

These interactions take place at different interaction volumes, which is shown in Fig. 2.14. The X-ray is able to escape to the surface from a deeper depth due to its long wavelength, while the escape depth for the secondary electrons is relatively shallow (5-50 nm). Therefore, the different signals in the SEM carry information from different depths.

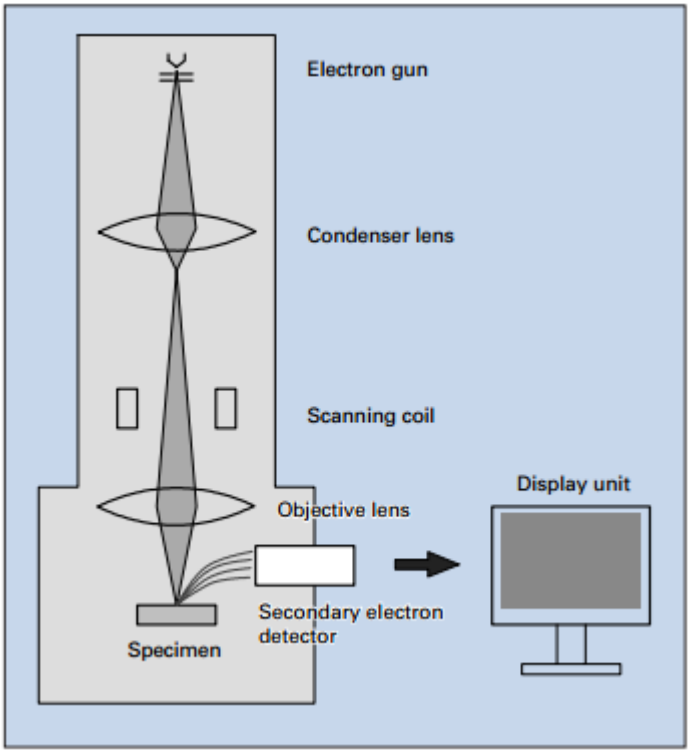


Fig. 2.13 Scanning Electron Microscopy (SEM) [53]

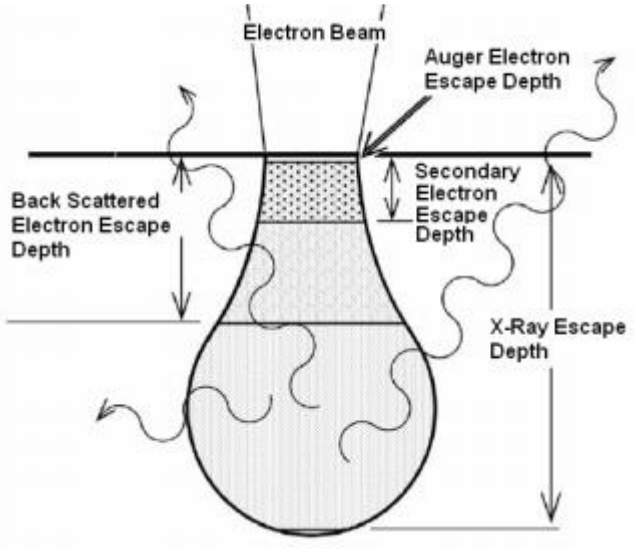


Fig. 2.14 The interaction volume of the particles reacted with the electron beam during the SEM measurement [52]

The secondary ion mass spectroscopy (SIMS) is a commonly used technique for surface spectroscopy, surface imaging, and depth profiling of the sample. In this thesis, SIMS is mainly used as the atomic depth profile within the Al_2O_3. It is a destructive method that uses the energetic ions as the primary

ion beam (usually O_2^+, O^-, Cs^+, Ar^+, or Ga^+) to bombard the surface and capture the secondary ions sputtered from the surface [54]. The sputtered secondary ions are collected by the detector with selected energy. It is achieved by the energy window set by the electrostatic energy analyser. Similarly, the ion mass can also be selected by the magnetic mass analyser. The components within a SIMS system are shown in Fig. 2.15.

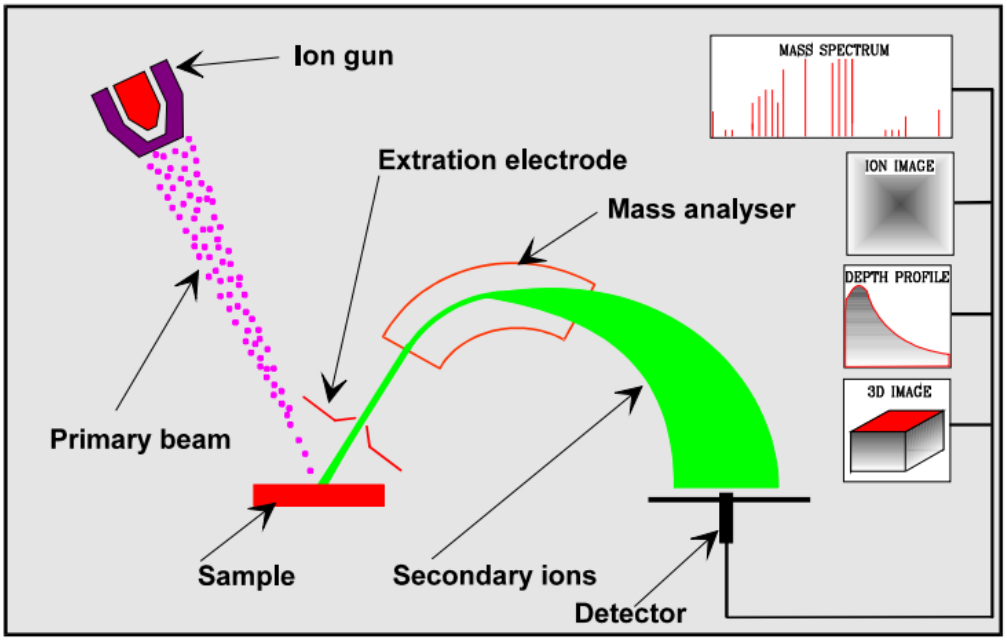


Fig. 2.15 Components within a SIMS system and the data can be retrieved from the SIMS system. [54]

The X-ray photoelectron spectroscopy (XPS) is a chemical analysis tool that utilised incident X-ray to induce photoelectron effect on the sample surface. As shown in the system schematics in Fig. 2.16 [55], the X-ray produced by the X-ray gun excites the electrons at the core levels to escape from the surface. After passing through the hemispherical sector analyser, electrons with selected energy can be collected by the detector. The electron energy spectra are produced by the XPS and they can be compared with the energy spectrum

database of materials to decide the chemical composition of the characterised sample.

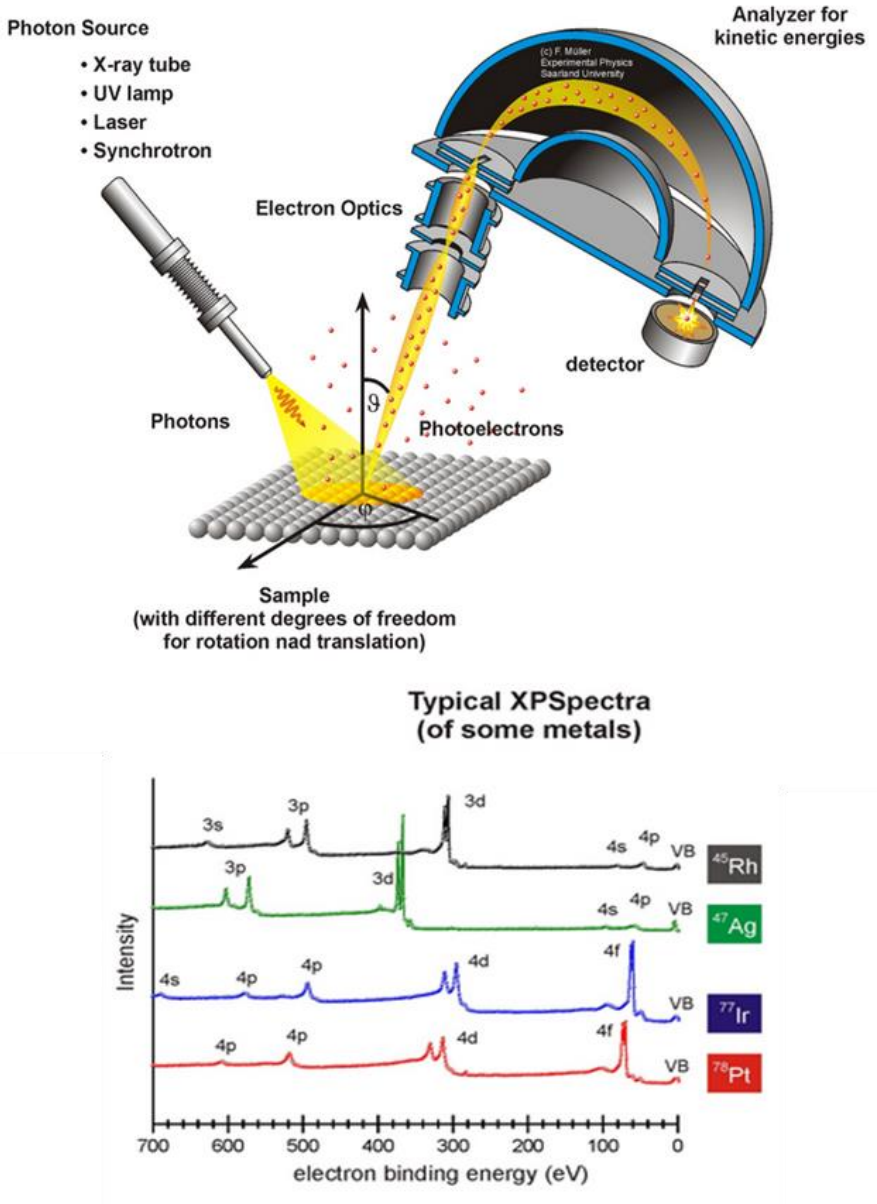


Fig. 2.16 The schematics of a XPS system together with a typical XPS spectra.

CHAPTER 3 High Temperature Characterisation and Analytical Modelling of AlGaN/GaN HEMTs under Steady State

3.1 Introduction

The properties of wide-bandgap (3.4eV) and high saturation velocity (1.5×10^7 cm/s) for GaN material enable it to be useful in the high-power applications operated under high temperature [56]. However, even though completed studies on the high-temperature effects on AlGaN/GaN HEMTs performance as regard to the Schottky gate barrier height, the two-dimensional electron gas (2DEG) sheet density [57, 58], threshold voltage (V_{TH}) [59], drain current-gate voltage (I_D-V_G) and the on-state drain current-voltage (I_D-V_D) characteristic variations [56, 60] already been observed, there is no study that verifies the analytical models of both the terminal characteristics and the intrinsic physical parameters under high temperature. This study improves the development of power circuit modelling at high temperatures as it prevents the solution of complicated numerical expressions that requires sophisticated computer coding. Additionally, the work reported in this chapter enables the device designer to predict the device performance under high temperature. The research of the GaN-based device performance in this chapter delivers the fundamental knowledge on the design of high threshold voltage Al_2O_3/AlGaN/GaN MIS-HEMTs reported in Chapter 4 and its studies on the high temperature performances reported in Chapter 5.

Starting with the characterisation of the I-V characteristics under high temperature, this work utilised the reported analytical models on characterising

the performances of AlGaN/GaN HEMT devices under room temperature and developed them to be adaptable to high temperature conditions. The accuracy of these models was then verified by the Sentaurus TCAD simulations and experimental characterisations.

3.2 The effect of high temperature on device characteristics

3.2.1 Structure and fabrication process of the characterised HEMTs

The cross-sectional schematic diagram and the microscopic image of the normally-on Schottky-gate AlGaN/GaN power HEMT used for modelling and characterisation in this chapter are shown in Fig. 3.1 (a) and (b). The device was fabricated on the AlGaN/GaN epitaxial wafer grown on Si substrate and a thick 4.2μm wide-bandgap AlN barrier layer which is responsible for high breakdown voltage. The thickness of the unintentionally-doped AlGaN and GaN epitaxial layers are 25nm and 1.6μm respectively. The AlGaN has an Al content of 20% to induce high 2DEG density with good carrier mobility. Therefore, the 2DEG can be used as the channel of a device with good conductivity and fast switching speed. A 1 nm GaN cap layer is deposited on top of the AlGaN barrier to prevent surface traps formation. The drain and source ohmic contacts are made of Ti/Al/Ni/Au with thickness of 25/125/45/55nm and rapid thermal annealing (RTA) processing at 850°C for 1 minute after deposition. The Ti/Al/Ni/Au metal stack configuration for ohmic contact is one of the most widely used technique for GaN-based HEMTs with small contact resistivity and good thermal stability. The gate electrode is made of un-annealed Ni/Au metal layers with thickness of 15/150nm and post-growth annealing at 400ºC for 20 minutes. The gate length

(L_G), gate-to-source length (L_{GS}) and gate-to-drain length (L_{GD}) are 2µm, 5µm and 7µm respectively. The width (W) of the normally-on HEMT is 130µm and it is assumed as the width of the ohmic pad. It is because of the similar width of mesa isolation as the pad width has minimised the outflow of current between the pads.

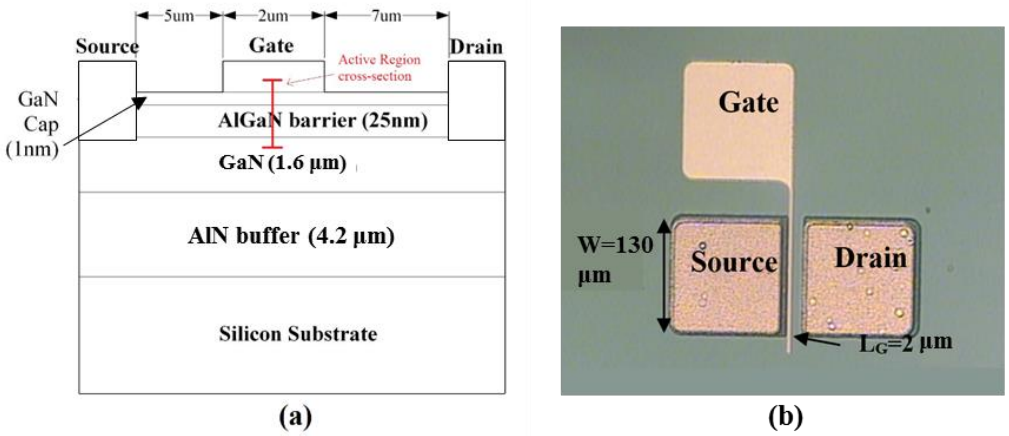


Fig. 3.1 (a) The cross-sectional schematic diagram the Schottky-gated normally-on AlGaN/GaN HEMT device; **(b)** the microscopic image of the fabricated normally-on AlGaN/GaN HEMT device.

3.2.2 Drain current-gate voltage (I_D-V_G) characteristics

The current-voltage characteristics demonstrated in this section were measured by the Agilent B1505A Power Device Analyser system. Fig. 3.2 (a) demonstrates the I_D-V_G measurements from 300K to 500K with 50K intervals in the sub-threshold region plotted in logarithmic scale. The drain voltage remained at V_D=6V during the characterisation. Table 3.1 reports the subthreshold swings and the threshold voltage (V_{TH}, obtained by extrapolating the linear region of the I_D-V_G characteristics plotted in linear scale shown in Fig. 3.2 (b) [61]) at different temperatures. From T=300K to 500K, the off-state leakage has increased by about three orders of magnitude. Meanwhile, the

subthreshold swing is also doubled. Little reduction of V_{TH} is found with the increase in temperature.

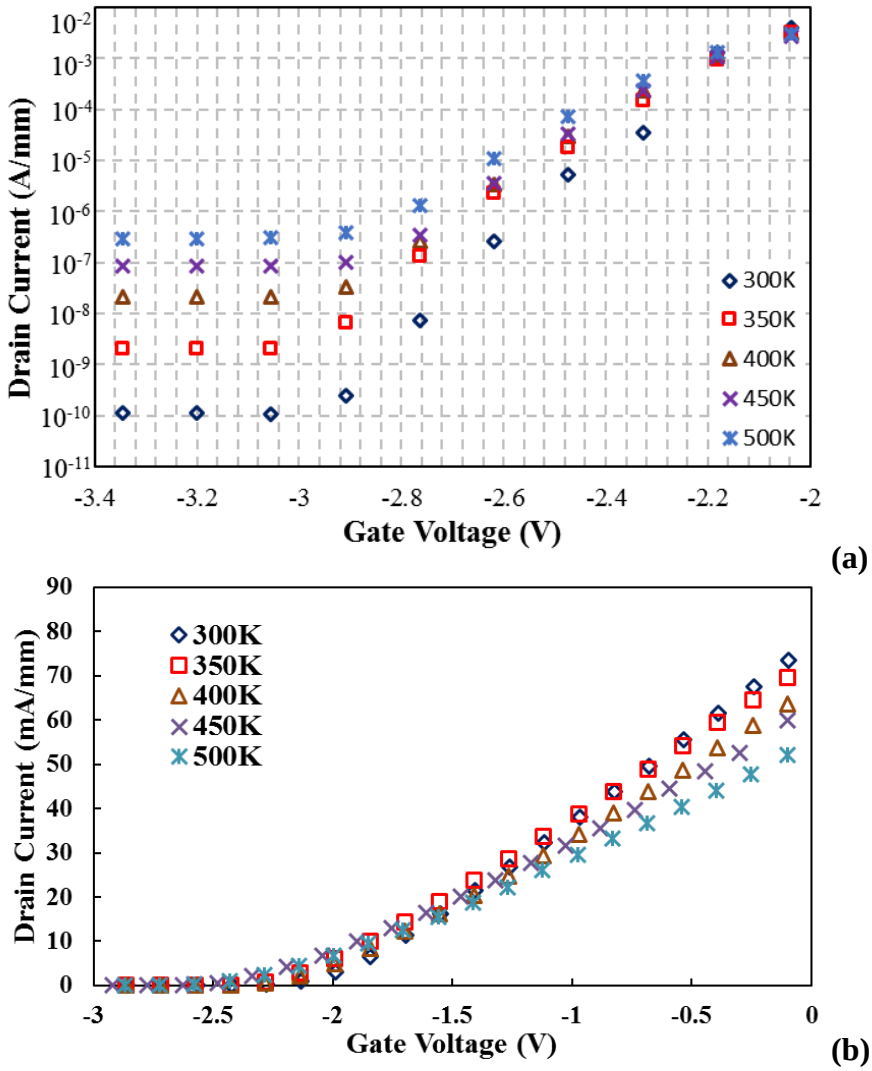


Fig. 3.2 (a) The logarithmic I_D-V_G characteristics in the sub-threshold region and **(b)** the linear I_D-V_G characteristics at temperatures from 300K to 500K. (V_D = 6V)

Table 3.1 The extracted V_{TH} and sub-threshold slope of the I_D-V_G curve at and different temperatures (V_D=6V)

Temperature (K)	Threshold Voltage (V)	Sub-threshold Slope (mV/dec)
300 K	-1.87	100
350 K	-2.05	120
400 K	-2.09	130
450 K	-2.12	160
500 K	-2.15	180

3.2.3 Drain current-drain voltage (I_D-V_D) characteristics

The I_D-V_D characteristics of different temperatures when V_G=0V (Fig. 3.3 (a)) and V_G=−1V (Fig. 3.3 (b)) are illustrated and summarised in Table 3.2. It is observed that the on-state resistance, which is the inverse of the slope of the I_D-V_D linear region, has increased at higher temperature. Approximately 100% increase of the on-state resistance is observed when temperature has raised from 300K to 500K. Meanwhile, about 40% reduction in the maximum drain saturation current (I_{DMAX}) is observed when the temperature rises from 300K to 500K. Similar trends are found when V_G used in the I_D-V_D characterisation is reduced to −1V, as shown in Fig. 3.3 (b) and Table 3.2.

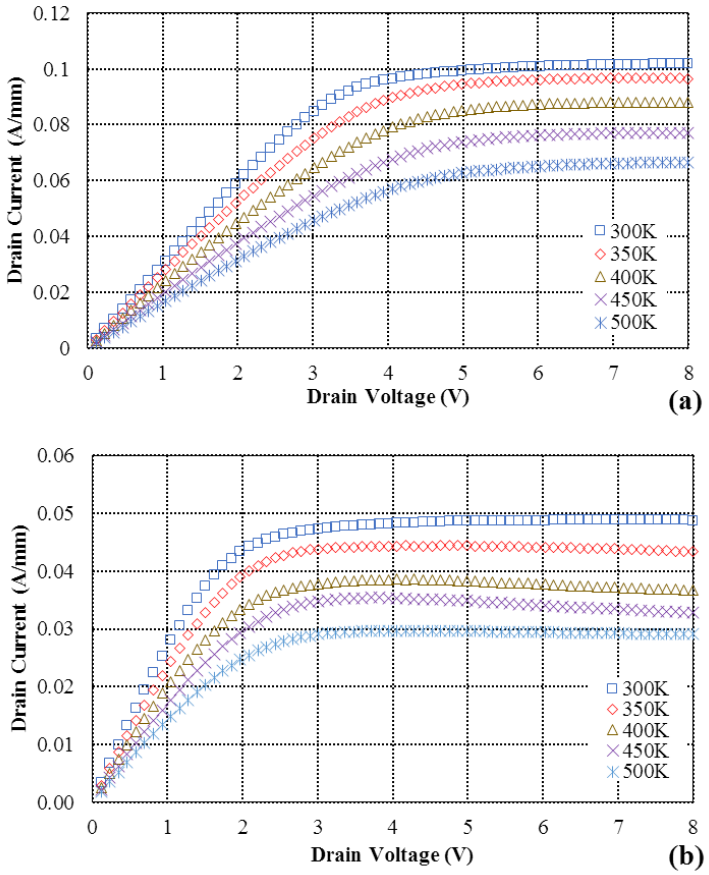


Fig. 3.3 The I_D-V_D characteristics of the device from T=300K to 500K. **(a)** V_G=1V and **(b)** V_G=−1V

Table 3.2 The on-state resistance and drain saturation current of the device from T=300K to 500K and V_G=0V and −1V.

	V_G=0V		V_G=−1V	
Temperature (K)	**On-state Resistance (Ω·mm)**	**Drain Saturation current (A/mm)**	**On-state Resistance (Ω·mm)**	**Drain Saturation current (A/mm)**
300 K	33	0.100	47	0.050
350 K	36	0.095	50	0.045
400 K	44	0.085	57	0.038
450 K	50	0.078	66	0.035
500 K	66	0.065	80	0.030

3.3 Verification of the AlGaN/GaN HEMT analytical model at high temperature

To understand the mechanism behind the performance variation at different temperatures, models for the physical parameters within the device have been verified and compared with device characterisation or Sentaurus TCAD simulation. Fig. 3.4 is the flowchart of the methodology adopted in the modelling approach. The method begins with the analytical modelling of the inherent properties of the devices, such as the flat-band Schottky barrier height. Then, combining it with the Fermi-Dirac function approximation, the 2DEG of the device can be modelled and be further used to model the V_{TH} and 2DEG carrier mobility. Lastly, they can be used to extract the terminal properties which can be directly measured, such as the I_D-V_D and I_D-V_G characteristics.

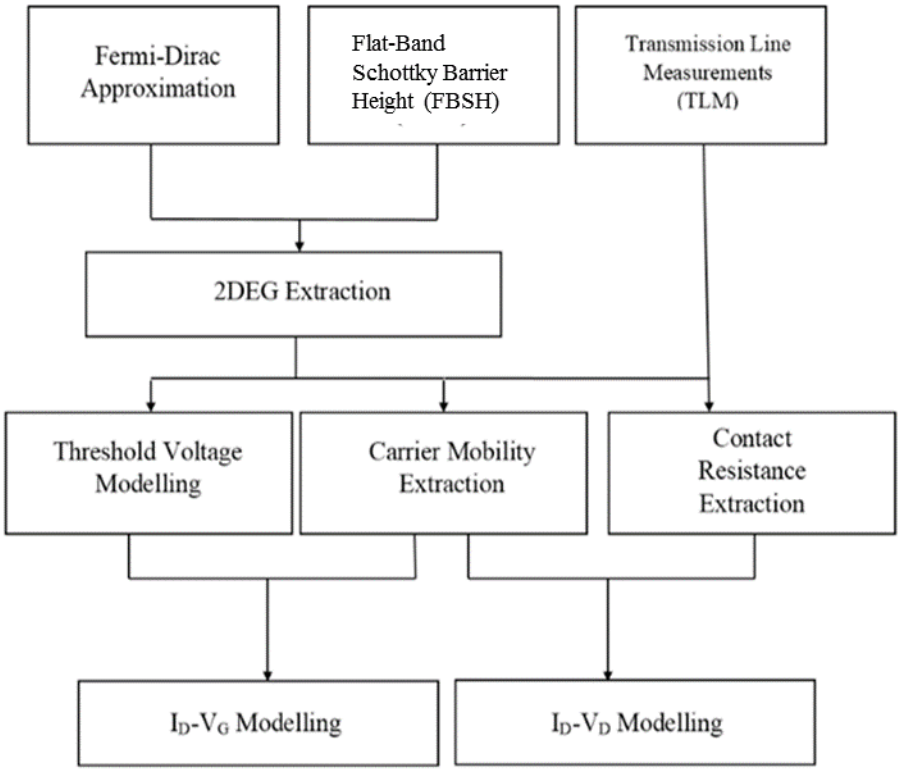


Fig. 3.4 The flowchart of the proposed analytical modelling process in characterising the AlGaN/GaN device performance at different high temperatures

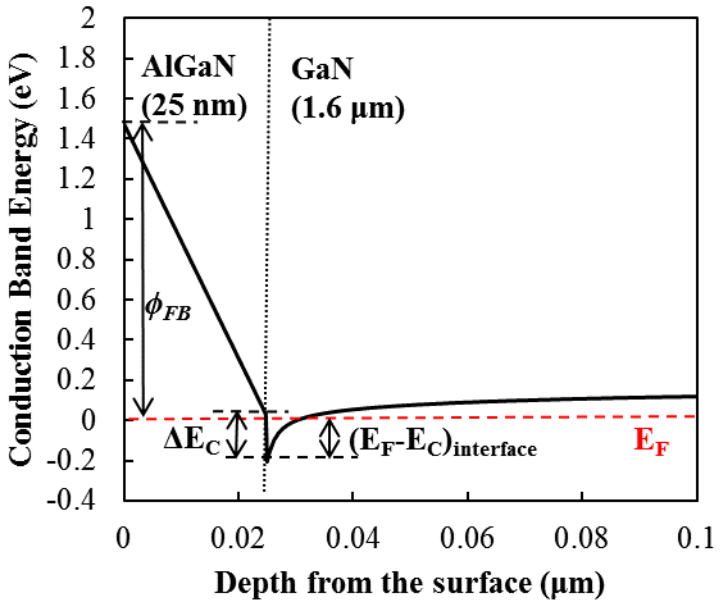


Fig. 3.5 The conduction energy band diagram of the active region (near AlGaN/GaN interface) of the HEMT without applying any external bias

The conduction band diagram of the active region (i.e. region near the 2DEG) underneath the gate metal is demonstrated in Fig. 3.5. The physical parameters involved will be explained and modelled in the following sections in this chapter.

3.3.1 Flat-band Schottky barrier height (FSBH) at the gate metal/AlGaN interface

Prior to the investigation of the effect of high temperatures to the performance of the fabricated AlGaN/GaN HEMTs, it is essential to observe the temperature dependence on the gate Schottky barrier height since it determines the 2DEG density and the V_{TH} within the device [11]. The study has applied the two-diode forward current model proposed in [62], which is usually used in FETs with heterojunction gate. However, the Schottky barrier height extracted from I_G-V_G measurements, which is also known as the effective Schottky barrier height (ESBH, ϕ_{EB}), is not the inherent physical parameter of the device as it is dependent on the applied gate electric field and current flow [63, 64]. Therefore, the flat-band Schottky barrier height (FSBH (ϕ_{FB})), which is the calibrated Schottky barrier height under zero electric field, was extracted and used for later stage calculations on the 2DEG together with the V_{TH} [9, 11, 64, 65]. In order to calculate the FBSH accurately, the temperature dependence on ϕ_{EB} and the ideality factor (n_G) shall be obtained first by measuring the I_G-V_G characteristics between the Schottky gate and the source terminals of the HEMT with Eq. (3.1) and (3.2) [62, 64, 66]. ϕ_{EB} and n_G in Eq. (3.1) are extracted by plotting the V_G versus $\ln(I_G/(aA^*T^2))$ through the gradients and the y-intercepts of the best fitted lines to the data points. The plot is demonstrated in Fig. 3.6 (a). In Eq. (3.1), a is the gate contact area and A^* is the effective Richardson constant (~28.4 $Acm^{-2}K^{-1}$ for $Al_{0.2}Ga_{0.8}N$ [64]). The effect of the

thin GaN cap layer to the Schottky barrier height is neglected as most of the current is tunnelled through this layer. To extract ΔE_C in Eq. (3.2) for FBSH, Eq. (3.3) is utilised [11]. Eq. (3.4) and (3.5) provide a method to calculate the temperature dependence on the band gap of AlN and GaN respectively [67].

$$\ln(\frac{I_G}{aA^*T^2}) = \frac{q}{n_G kT}(V_G - n_G\phi_{EB}) \tag{3.1}$$

$$\phi_{FB}=n_G\,\phi_{EB}-(n_G-1)[\Delta E_C(E_F-E_C)_{interface}] \tag{3.2}$$

$$\Delta E_c = 0.7[E_g(Al_xGa_{1-x}N) - E_g(GaN)]$$

$$= 0.7[xE_g(AlN) + (1-x)E_g(GaN) - x(1-x)\times 1.0eV - E_g(GaN)] \tag{3.3}$$

Where

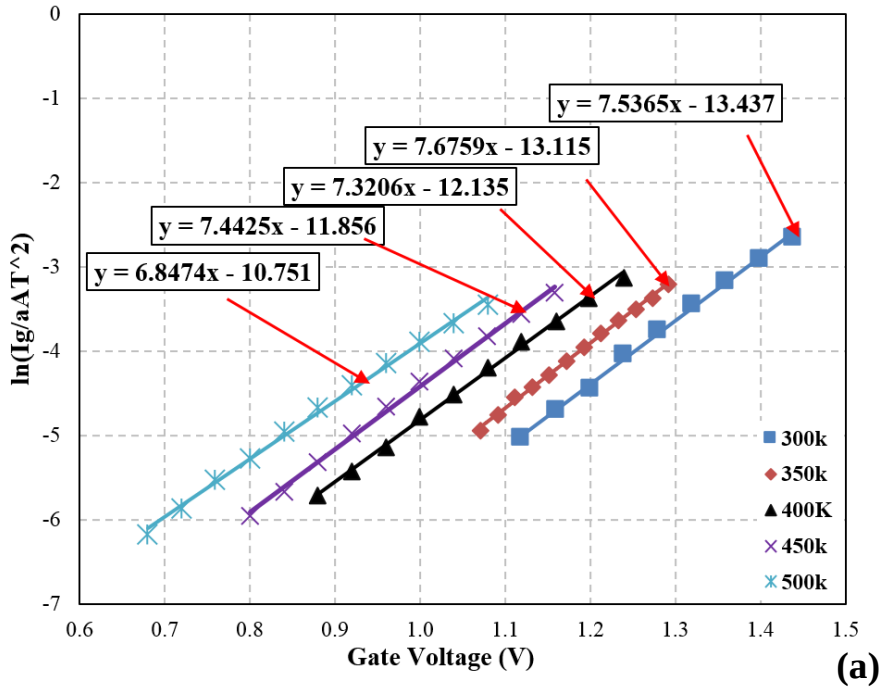
$$E_{g\_AlN}(T) = 6.312 - \frac{0.001799\,T^2}{T+1462} \tag{3.4}$$

$$E_{g\_GaN}(T) = 3.51 - \frac{0.000909\,T^2}{T+830} \tag{3.5}$$

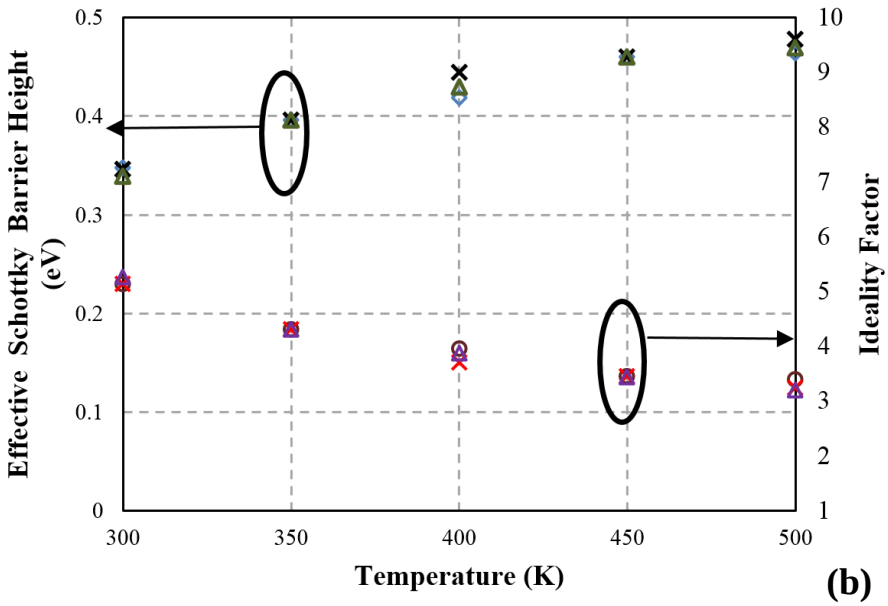
The values of the EBSH and the ideality factor under different temperatures are summarised in Fig. 3.6 (b). It is observed that the ESBH increases at higher temperatures, while the ideality factor has an opposite trend. It is also notable that the ideality factor for AlGaN/GaN HEMTs is much higher than one, implies the occurrence of strong band-to-impurity and band-to-band tunnelling [68].

The extraction of FSBH involves in the temperature dependence on the work function of the gate metal. In [69], the relationship of the FSBH and the Al content at 300K is provided. For $Al_{0.2}Ga_{0.8}N$, the FSBH is 1.5eV at room temperature. The variation in the FSBH with temperature can be related to the electron affinity of AlGaN (X_{AlGaN}) and the work function of the gate metal (ϕ_M). It is expressed as: $\phi_{FB}=\phi_M-X_{AlGaN}$ [70]. The nickel and gold work functions at

300K are 5.15eV and 5.1eV respectively, and their temperature coefficients are -5.6×10^{-4}eV/K and -6.8×10^{-4}eV/K respectively [71]. The work function and its temperature dependence of the Ni/Au alloy can be linearly interpolated. The X_{AlGaN} at room temperature is 3.6eV and its temperature dependence, which is originated from the change in AlGaN bandgap with temperature, is negligible compared to the more significant variations in the metal work functions [72]. The surface traps at the gate can also influence the accuracy of extracted FSBH. In this chapter, 9×10^{11}cm^{-2} of acceptor surface traps at the metal/semiconductor interface (N_{ST}) located at 1.0eV from the AlGaN valence band [73, 74] are adopted to calibrate the extracted ϕ_{FB} by adding the term $qN_{ST}d_{AlGaN}/\varepsilon_{AlGaN}$ into the derivation. Such calibration is applicable to the device characterised in this section as it uses the same Ni/Au gate metal stack configuration as the one reported in [74]. The temperature dependences on ϕ_{FB} obtained from modelling with and without the surface traps together with the characterised results are shown in Fig. 3.6 (c). They demonstrate that the FSBH decreases at higher temperature, and is further verified from the simulation results carried out by Sentaurus TCAD simulation tools. Therefore, the analytical FSBH model is able to accurately predict the Schottky barrier heights at temperatures ranging from 300K to 500K.


y = 7.5365x - 13.437
y = 7.6759x - 13.115
y = 7.3206x - 12.135
y = 7.4425x - 11.856
y = 6.8474x - 10.751
300k
350k
400K
450k
500k
ln(Ig/aAT^2)
Gate Voltage (V)
0
-1
-2
-3
-4
-5
-6
-7
0.6
0.7
0.8
0.9
1.0
1.1
1.2
1.3
1.4
1.5

(a)


Effective Schottky Barrier Height (eV)
Ideality Factor
Temperature (K)
0.5
0.4
0.3
0.2
0.1
0
10
9
8
7
6
5
4
3
2
1
300
350
400
450
500

(b)

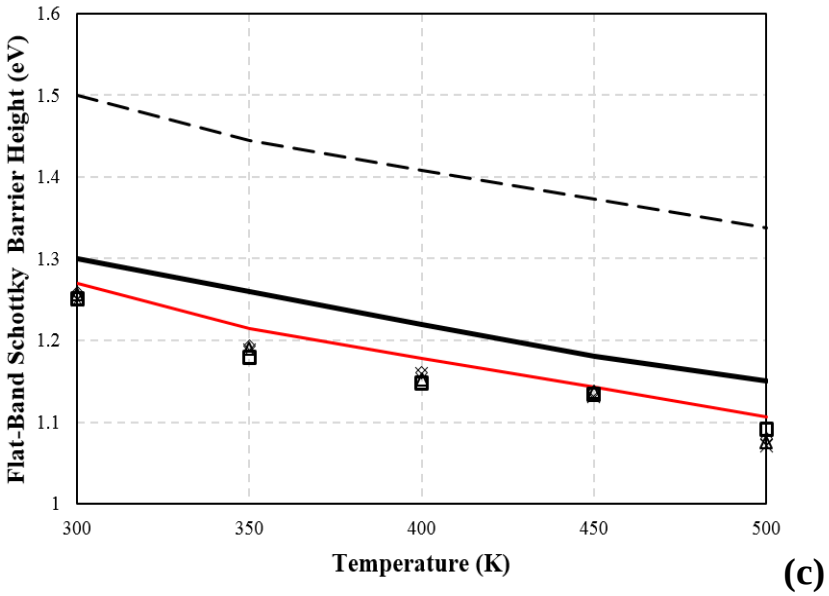


Fig. 3.6 (a) The experimental data of V_G versus $\ln(I_G/(AA\times T^2))$ from 300K to 500K; **(b)** The ESBH and the ideality factor (n_G) extracted from Eq. (3.1); **(c)** The experimental FSBH data based on five repetitive I_G-V_G characterisations, the analytically-modelled FSBH with (red solid line) and without (broken line) the $9\times 10^{11}cm^{-2}$ of acceptor surface trap from 300K to 500K. The TCAD Sentaurus simulation results (black bold line) are also included in the figure.

3.3.2 The conduction band location at the AlGaN/GaN interface and 2DEG density

To analytically extract the energy difference between the Fermi level and the conduction band at the GaN side of the AlGaN/GaN interface, labelled as $(E_F\text{-}E_C)_{interface}$, the Fermi-Dirac approximation is required. The most common way in band calculations for semiconductors is to use the Fermi-Dirac integral of order ½ ($F_{1/2}$) and gamma function of $\Gamma(3/2)=\sqrt{\pi}/2$. The complete expression of the Fermi-Dirac integral with half order is demonstrated in Eq. (3.6). However, it requires iterative numerical extractions. Since the conduction band of GaN at the AlGaN/GaN interface is lower than the Fermi level [13, 75], it can be perceived as degenerate and the approximations for degenerate semiconductors can be utilised, as shown in Eq. (3.7) [76]. In Eq. (3.7), E_F–E_C

is the difference between the Fermi level and the conduction band, *n* is the electron density at the position of interest, *k* is the Boltzmann constant, *T* is the ambient temperature, and N_{C_GaN} is the effective density of states at the conduction band of GaN.

$$\mathrm{F}_{1/2}(\eta_F) = \frac{\sqrt{\pi}}{2}\int_0^{\infty}\frac{\eta^{1/2}}{1+\exp(\eta-\eta_F)} \tag{3.6}$$

$$\eta_F(F_{1/2}) = \frac{\ln(F_{1/2})}{1-F_{1/2}} + (\frac{3\sqrt{\pi}F_{1/2}}{4})^{2/3} + \frac{8\sqrt{\pi}F_{1/2}}{3\times(4+\sqrt{\pi}F_{1/2})^2} = \frac{E_F - E_C}{kT}, \tag{3.7}$$

Where

$$F_{1/2} = \frac{n}{N_{C\_GaN}}$$

$$N_{C\_GaN} \sim= 4.3\times10^{14}T^{3/2}$$

Before solving the Fermi-Dirac approximations at the AlGaN/GaN interface, the electron density at the interface must be determined. It is normally extracted by solving the Poisson's equation, which is unable to be solved analytically. Therefore, a simplified analytic approach is proposed. For unintentionally doped AlGaN/GaN layers, the space charge at the AlGaN/GaN interface is determined by the polarisation charge induced by the spontaneous and piezoelectric polarisation fields [13]. Based on the electron distribution near the AlGaN/GaN interface extracted by the self-consistent Poisson-Schrodinger solver [11, 14, 77], the charge distribution near this interface can be empirically approximated as linearly distributed charge within 3nm to obtain similar peak electron concentration at the AlGaN/GaN interface. Therefore, as the temperature-independent polarisation charge concentration at the perfect $Al_{0.2}Ga_{0.8}N$/GaN interface is about 1.1×10^{13} cm^{-2}, its peak point charge density at the interface is around 7.33×10^{19} cm^{-3}. The electron density at the

AlGaN/GaN interface can then be approximated for conduction band location calculation in Eq. (3.7).

Once the conduction band level at the AlGaN/GaN interface is extracted, the 2DEG can be derived analytically from Eq. (3.8) proposed in [13]. In Eq. (3.8), $\varepsilon_{AlGaN(x)}$ is the dielectric constant of AlGaN, which can be obtained by linearly interpolating the dielectric constants of GaN (~8.9) and AlN (~8.5); σ_{pol} is the sheet polarisation charge concentration at the AlGaN/GaN interface, which is 1.1×10^{13} cm^{-2}; d_{AlGaN} is the thickness of the AlGaN layer; and $\Delta E_C(x)$ is the conduction band offset between AlGaN and GaN.

$$n_s(x)=\frac{\sigma_{pol}}{q}-\frac{\varepsilon_{AlGaN}(x)}{q^2 d_{AlGAN}}\left[q\phi_{FB}+(E_F-E_C)_{interface}-\Delta E_C(x)\right] \tag{3.8}$$

It has been previously reported that the polarisation charge concentration is independent from temperature [14]. The analytical approximation of the temperature dependence on E_F-E_C and the 2DEG density are verified by the Sentaurus TCAD simulations and the Hall measurement results provided by the wafer manufacturer shown in Fig. 3.7. For simplicity, the cap, the buffer, and the substrate layers were not involved in the simulations as they do not affect the on-state electrical properties. According to Fig. 3.7, it is seen that the quantum well at the AlGaN/GaN interface becomes shallower with the increase of temperature, while the 2DEG density increases at higher temperatures. It can be attributed to the decrease of the FBSH at higher temperature reversed the trend of 2DEG density and the depth of the quantum well. In summary, the analytical model predicts the temperature dependence on the quantum well and the 2DEG density very well. The mismatch between the model and the TCAD

simulation is within 2% at characterised temperatures. However, about 10% reduction of the 2DEG density is obtained by the Hall measurement compared with the values calculated and simulated. It can be attributed to the possible variations in manufacturing conditions, such as the uniformity and the quality of the epitaxial layers.

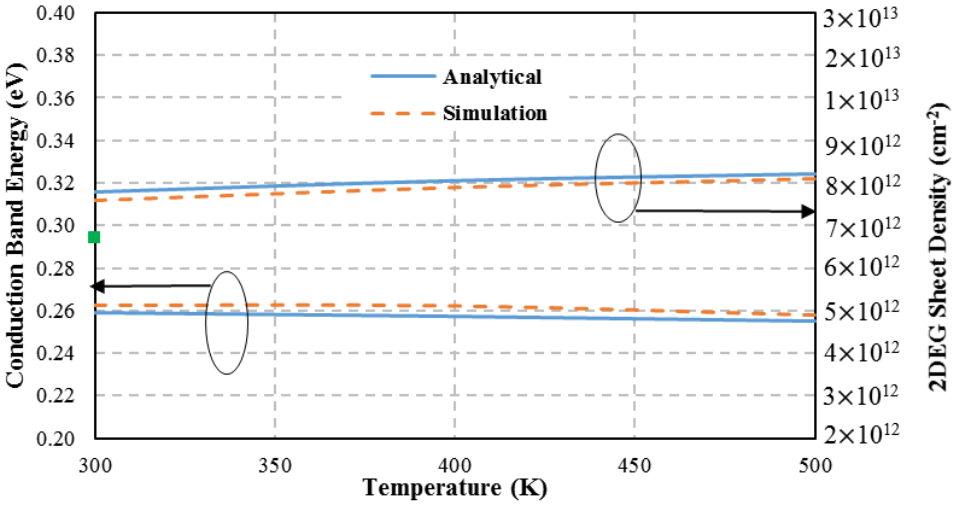


Fig. 3.7 The comparison between the model and TCAD simulation of the conduction band energy level with respect to the fermi level and the 2DEG sheet density from 300K to 500K. The green dot is the 2DEG sheet charge density provided by the wafer manufacturer by Hall measurement.

3.3.3 Analytical modelling of the threshold voltage (V_{TH})

The analytical model for the threshold voltage (V_{TH}) of the normally-on AlGaN/GaN HEMT is shown in Eq. (3.9) [62, 63]. The measured V_{TH} was obtained by linear extrapolating the I_D-V_G curves proposed in [61]. This method is one of the most widely used way to extract V_{TH}. The measurements are obtained when V_D= 1V. N_{ST} is the density of surface traps of the device mentioned in Section 3.3.1 ($9\times10^{11}cm^{-2}$). According to Fig. 3.8, the V_{TH} calculated by Eq. (3.9) has a good match with the experimental results, and the V_{TH} has declined only slightly at higher temperatures. This is caused by the

increase in the 2DEG sheet density at higher temperatures. Therefore, higher negative gate voltage is required to deplete the 2DEG and pinch off the channel.

$$V_{TH} = \phi_{FB} - \frac{d_{AlGaN}\sigma_{pol}}{\varepsilon_{AlGaN}} - \Delta E_C + (E_F - E_C)_{interface} - \frac{qd_{AlGaN}N_{st}}{\varepsilon_{AlGAN}} \quad (3.9)$$

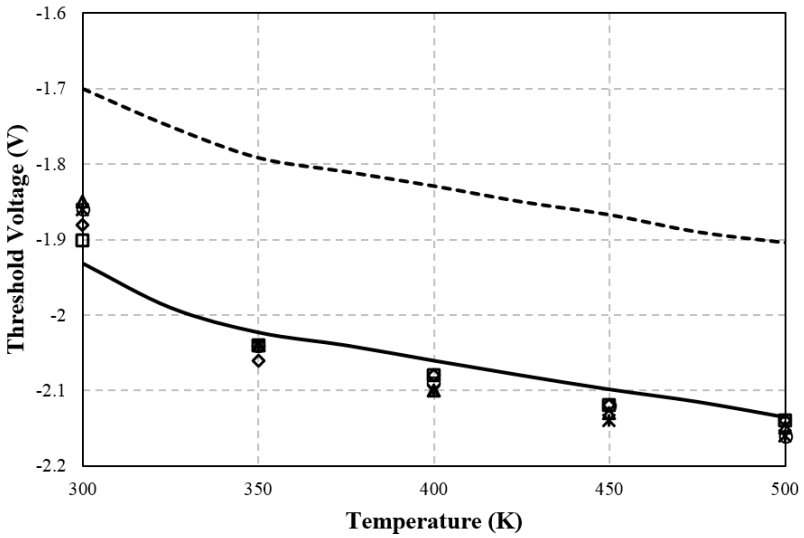


Fig. 3.8 The comparison between the V_{TH} obtained from the experiments (dots) and Eq. (3.9) with (solid line) and without (broken line) the incorporation of acceptor traps.

3.3.4 Modelling of specific contact resistance and 2DEG electron mobility

The extraction of specific contact resistance is also essential for the sub-threshold I_D-V_G and I_D-V_D modelling. It is an indicator of the quality of the ohmic contact fabricated on the AlGaN surface. It is desirable to obtain contacts with small specific contact resistance in order to reduce the conduction loss within the device. It can be obtained experimentally from the transmission line measurements (TLM) with small voltage sweep (from −1V to 1V) to avoid the self-heating effect. The self-heating effect may reduce the electron mobility during measurement and affect the accuracy of the extracted contact resistances. The distance between each of the contact pads are 15μm, 25μm, and 40μm. According to Fig. 3.9, the resistances versus the distances between the pads at

different temperatures are plotted. The slopes of the fitted lines in Fig. 3.9 are able to extract the sheet resistance (R_{sheet}) between the pads at different temperatures through $R_{sheet}=slope\times Z$, where Z is the width of the contact pad (130μm). Therefore, the electron mobility at 300K ($\mu_{(T=300K)}$) can be calculated from $\mu=1/(n_s q R_{sheet})$, where n_s equals to the 2DEG density extracted in Section 3.3.2. Once $\mu_{(T=300K)}$ is obtained, the 2DEG mobility at other temperatures can be extracted from the following relationship: $\mu(T)=\mu_{(T=300K)}\times(T/300)^{\gamma}$. In this expression, $\mu(T)$ is the mobility at the adjusted temperature, T is the temperature, and γ is the temperature-independent mobility exponent, which is assumed to be −1.5 [78]. The contact resistance of the ohmic contact is extracted based on the transmission line model reported in [79]. The calculated 2DEG mobility at different temperatures are summarised in Table 3.3.

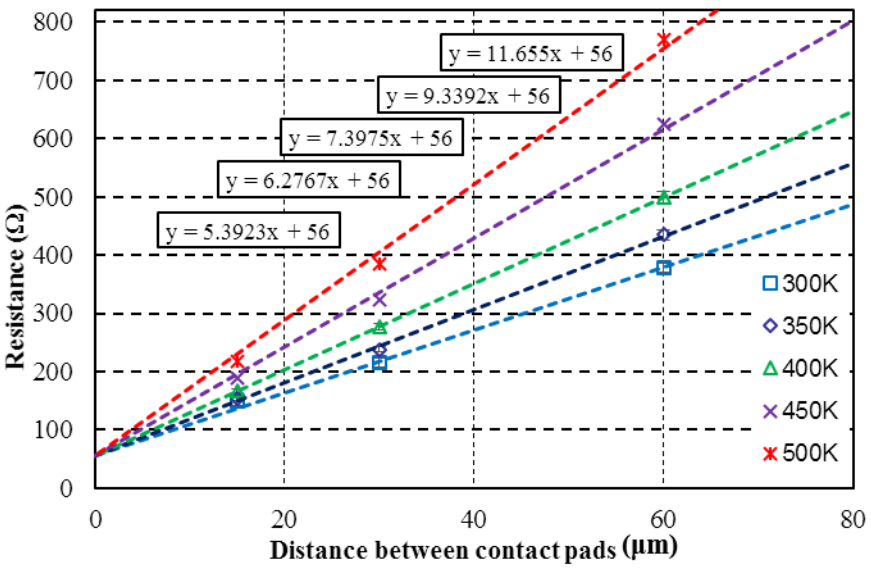


Fig. 3.9 The resistances versus the distance between each contact pads at different temperatures

Even though the carrier transport across the ohmic contact is dominated by the temperature-independent tunnelling process, both the contact resistance and specific contact resistivity are obviously reduced at higher temperatures. It can

be attributed to the involvement of thermionic mechanism during charge transportation at the metal/AlGaN interface within the ohmic contact. The thermionic transportation is enhanced at higher temperature [80]. Specifically, the specific contact resistance of the Ti/Al/Ni/Au ohmic contact can be modelled by the field emission effect illustrated in Eq. (3.10) [81]. ϕ_B is the barrier height at the metal/AlGaN interface and can be extracted by ϕ_M-X_{AlGaN}. For Ti/Al/Ni/Au ohmic contacts, a low-work-function TiN (ϕ_{TiN}=3.74eV) is formed and contacted the AlGaN surface after the rapid thermal annealing (RTA) process. However, the formation of TiN in reality is imperfect and a certain amount of Ti (ϕ_{TiN}=4.33eV) may remain at the interface. Therefore, the barrier height of the metal/AlGaN interface should be fitted within the range between 0.14 eV to 0.73 eV. With numerous iterations, ϕ_B=0.56 eV provides the best fit. N_D=5×10^{19}cm^{-3} [82] is the doping concentration of AlGaN at the interface. A_C is the area of the ohmic contact pad, which is 0.03 mm^2 for our sample. The value of E_F−E_C can be obtained from Eq. (3.7). The comparison between the model and the measurement results of the specific contact resistance is shown in Fig. 3.10. The barrier height at the ohmic contact and AlGaN interface can be different according to the types of metals used and the processing technologies applied.

$$\rho_c = \{\frac{A^* A_C T\pi q}{k\sin(\pi c_1 kT)}\exp(\frac{-\phi_B}{E_{00}}) - \frac{A^* A_C c_1 q}{(c_1 k)^2}\exp[\frac{-\phi_B}{E_{00}} - c_1(E_F - E_C)]\}^{-1} \quad (3.10)$$

Where $E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N_D}{m^*\varepsilon_{\mathrm{AlGaN}}}}$; $c_1 = \frac{1}{2E_{00}}\ln(\frac{4\phi_B}{E_F - E_C})$

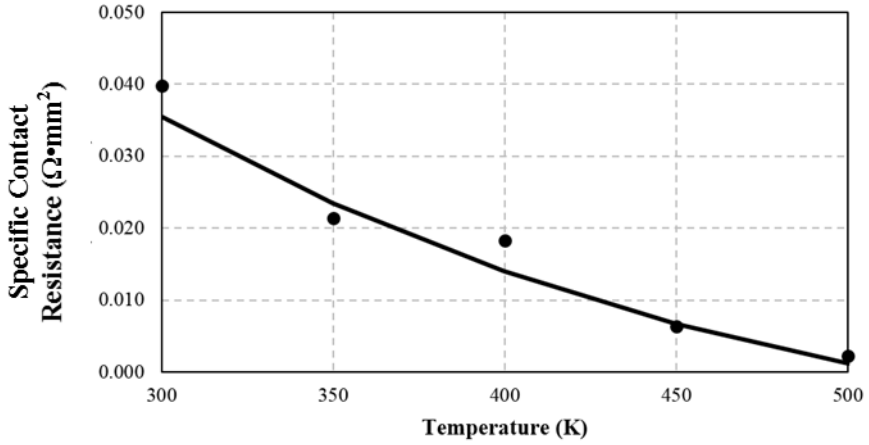


Fig. 3.10 The comparison between the specific contact resistance obtained from Eq. (3.10) (solid line) and TLM experimental results (dots)

Table 3.3 The parameters used for sub-threshold I_D-V_G and I_D-V_D modelling obtained from the TLM measurements.

Temperature (K)	**300K**	**350K**	**400K**	**450K**	**500K**
2DEG Density (10^{12} cm^{-2})	8.60	8.67	8.74	8.83	8.93
Mobility obtained from the TLM ($cm^2/V·s$)	895	719	599	452	380
Mobility obtained from the model ($cm^2/V·s$)	895	710	581	487	416
Mobility exponent	~=−1.5				
Sheet Resistivity (Ω/□)	896	1100	1300	1710	2160
Contact Resistance (Ω·mm)	4.43	3.61	3.61	2.43	1.63
Specific contact resistance ($Ω·mm^2$)	0.039	0.021	0.018	0.006	0.002

3.3.5 Modelling of I_D-V_G sub-threshold characteristics

The model used for I_D-V_G sub-threshold characteristics is described in Eq. (3.11) [83]. *L* and *W* are the length and width of the channel respectively, and μ is the 2DEG electron mobility which has been extracted from the TLM in Section 3.3.4 [84-86]. η is the capacitive coupling between the gate and the GaN surface, which is defined in Eq. (3.12). In Eq. (3.12), C_{AlGaN}, C_{QW}, $C_{depletion}$, $C_{surface}$ and C_{cap} are the capacitances of the AlGaN layer, quantum well at the AlGaN/GaN interface, depletion region at GaN, surface states and GaN cap layer, respectively. Fig. 3.11 demonstrates the location of these capacitances within the device [85]. For the device used in this study with a well passivated AlGaN surface with GaN cap layers and SiO_2 passivation layer, the amount of the surface states is so small that the $C_{surface}$ can be neglected [87]. C_{QW} can also be eliminated in the calculation due to the high conductivity of the 2DEG [88]. C_{cap} is also negligible since it is too thin that most of the carriers are tunnelled through rather than accumulating at both sides of the cap layer. $C_{depletion}$ and C_{AlGaN} can be obtained from $C=\varepsilon/d$. Therefore, η of the characterised HEMT can be approximated as 1.34 when the depletion depth of the unintentionally doped AlGaN/GaN HEMT is about 75 nm [11, 89].

$$I_{ds} = \frac{W\mu\varepsilon_{GaN}}{\sqrt{2}L}\left(\frac{kT}{q}\right)^2 \exp[q(V_{GS}-V_{th})/(\eta kT)]\times[1-\exp(\frac{-qV_{ds}}{kT})] \tag{3.11}$$

$$\eta = 1+\frac{C_{depletion}+2C_{QW}}{C_{AlGaN}+C_{cap}+C_{surface}} \cong 1.34 \tag{3.12}$$

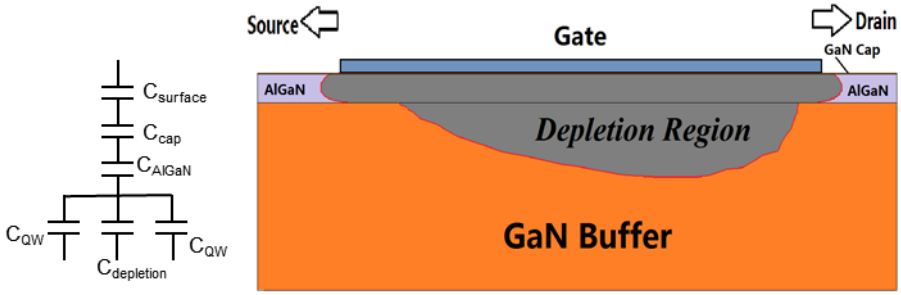


Fig. 3.11 The schematic of equivalent capacitance circuit diagram and the simulated depletion region of the AlGaN/GaN HEMT under the gate at sub-threshold condition.

By using Eq. (3.11) with the capacitive coupling constant, the I_D-V_G characteristics can be modelled, where the V_{TH} at different temperatures has already been obtained in Section 3.3.3. Compared to the experimental results, the analytical model has a good fit at all tested temperatures, as shown in Fig. 3.12.

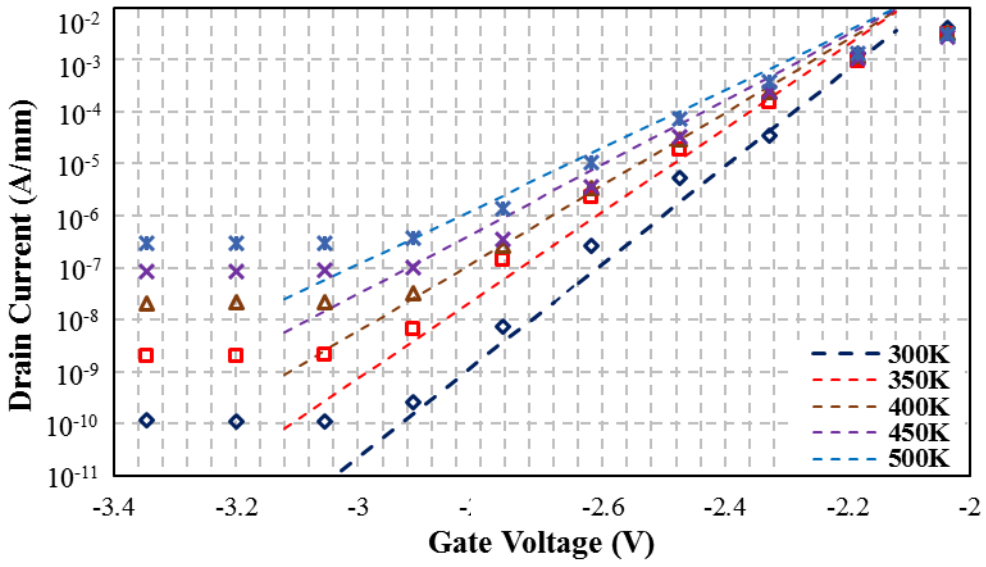


Fig. 3.12 The comparison between the experimental results (data points) and the analytical model (broken lines) of the I_D-V_G characteristics in the sub-threshold region from 300K to 500K. (V_D = 6V)

3.3.6 Modelling of I_D-V_D characteristics

The variations in I_D-V_D characteristics at various temperatures are mainly caused by the change of 2DEG channel mobility [78]. The enhancement of phonon scattering effect at higher temperature is the major mechanism responsible for the on-state current reduction.

The analytical I_D-V_D model is expressed differently under linear or saturation region. They are shown in Eq. (3.13) and (3.14) respectively [90]. R_d and R_s are the contact resistances of the drain and source terminals respectively, which are calculated and summarised in Table 3.3. In Eq. (3.15), the λ, saturation electric field (E_{sat}), and the saturation velocity (v_{sat}) can be extracted based on the 2DEG mobility values calculated in Section 3.3.4 and summarised in Table 3.3 [87, 89, 90]. Fig. 3.13 compares the experimental and analytical results of the I_D-V_D characteristics for V_G = 0V, –1V, between 300K and 500K.

$$I_{dlin} = \frac{A_{22} + \sqrt{A_{22}^2 - 4A_{11}A_{33}}}{2A_{11}} \tag{3.13}$$

$$A_{11} = (R_d - \frac{1}{\lambda E_{sat}})^2 - (R_s + \frac{1}{\lambda E_{sat}})^2$$

$$A_{22} = 2[V_{gd}(R_d - \frac{1}{\lambda E_{sat}}) + V_{gt}(R_s + \frac{1}{\lambda E_{sat}}) + \frac{1}{\lambda}L]$$

Where

$$A_{33} = V_{gd}^2 - V_{gt}^2$$

$$V_{gd} = V_{gt} - V_{ds}$$

$$V_{gt} = V_{gs} - V_{th}$$

$$I_{dsat} = \frac{A_2 + \sqrt{A_2^2 - 4A_1A_3}}{2A_1} \tag{3.14}$$

$$A_1 = -R_s^2 - \frac{2}{\lambda E_{sat}} R_s$$

$$A_2 = 2V_{gt}R_s + \frac{2}{\lambda E_{sat}} V_{gt} + \frac{2}{\lambda} L$$

$$A_3 = -V_{gt}^2$$

$$V_{dsat} = V_{gt} - (\frac{2}{\lambda E_{sat}} - R_d) I_{dsat}$$

Where

$$\lambda = \frac{W \varepsilon_{GaN} \mu}{d_{AlGaN}}, \quad E_{sat} = \frac{v_{sat}}{\mu}, v_{sat} = \frac{1.4 \times 10^7}{0.85 + 0.15 \frac{T}{300K}} \tag{3.15}$$

The on-state drain currents at both linear and saturation regions reduce at higher temperatures. It is mainly due to the mobility reduction caused by the enhanced phonon scattering of the lattice [13]. By examining the linear region of the I_D-V_D characteristics to extract the on-state resistance, it is observed that the on-state resistance is higher with increasing temperature. It proves the dominant effect of carrier phonon scattering on the on-state current even though the 2DEG density is slightly increasing at higher temperatures reported in Section 3.3.2.

The current reduction at lower V_G during the I_D-V_D sweep is caused by its depletion effect to the 2DEG channel at the gate region. When negative voltage is applied to the gate, the electrons at the 2DEG below the gate are depleted due to the electric field induced by V_G. Therefore, the free carrier density in 2DEG is reduced, resulting in current reduction and earlier current saturation [1].

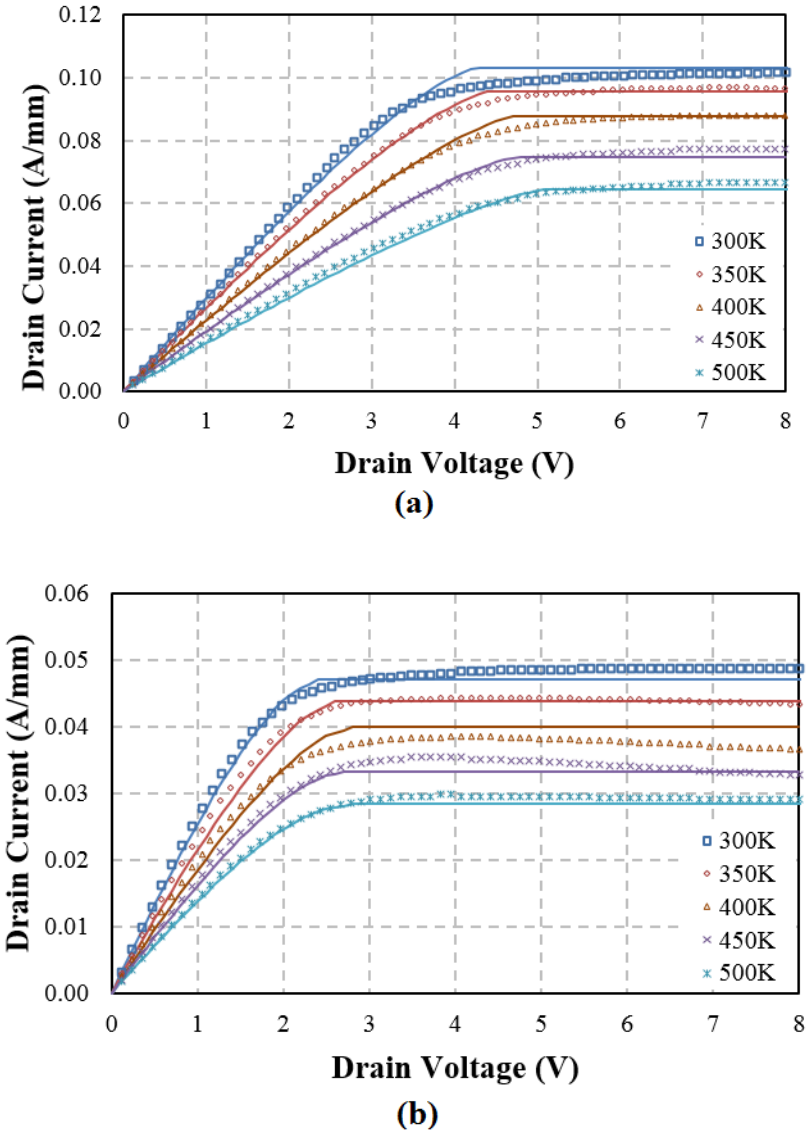


Fig. 3.13 The comparison between the experimental results (data point) and the analytical modelling results (solid lines) of the I_D-V_D characteristics from 300K to 500K when the gate voltage (V_G) is **(a)** 0V and **(b)** -1V

3.4. Conclusion

This chapter characterised the high-temperature performance of AlGaN/GaN HEMTs then integrates the existing room-temperature analytical models for high-temperature environment. Specifically, the temperature dependence on the FSBH, E_C-E_F at AlGaN/GaN interface, 2DEG sheet density,

threshold voltage, specific contact resistance, sub-threshold I_D-V_G and I_D-V_D characteristics have been illustrated. The models have been verified through characterising an $Al_{0.2}Ga_{0.8}N$/GaN HEMT by lab measurements and Sentaurus TCAD simulations. As a result, the analytical models are able to predict the device performance parameters fairly accurately at temperatures ranged from 300K to 500K. When temperature increases, the FBSH, E_C-E_F and drain saturation current decrease in different magnitudes, whereas the on-state resistance, 2DEG sheet density and the threshold voltage increase. The reduction in mobility due to enhanced phonon scattering is the dominant factor for the increase in the on-state resistance at higher temperatures. The increase in 2DEG is trivial to affect the on-state resistance. The proposed analytical models are useful for device designers on the prediction of the AlGaN/GaN HEMT device performance under high temperature. The fundamental knowledge on the device performance offered in this chapter will be applied in the V_{TH} engineering and V_{TH} thermal stability studies in chapters 4 and 5

CHAPTER 4 Multi-Fluorinated Al_2O_3/AlGaN/GaN MIS-HEMTs for High-V_{TH} and Monolithic Inverter Integration

4.1 Introduction

It is discussed in previous chapters that GaN-based power HEMTs are able to provide high breakdown voltage as well as good conductivity due to their superiority on breakdown field and 2DEG carrier density. However, achieving normally-off (i.e. threshold voltage higher than zero) operation for the GaN-based devices is strongly desired in order to simplify the gate drive circuit and improve the system reliability, particularly in power electronics applications. Special gate design approaches such as the AlGaN barrier recess [4-6], p-GaN cap layer [7, 8] and negative charge incorporation through fluorine plasma treatments (FPT) [9] have been explored in Section 1.3 to achieve normally-off operations. Among these, fluorine treatment is a promising technique as it is able to provide high threshold voltage (V_{TH}) without extra epitaxial growth or high temperature treatments which are costly and increasing the thermal budget on the device. However, the carriers in 2DEG channel suffer mobility degradation due to the impurity scattering from the implanted fluorine ions if they are in close proximity. Meanwhile, the reported V_{TH} of the devices fabricated with single FPT process are not very high (detailed review has been reported in Section 1.3.2). It implies that the 2DEG density in the gate region is

too high for FPT-introduced negative charges (F^-) to deplete the electrons in the 2DEG channel effectively. Table 4.1 summarises the reported gate fabrication methodology and the performance of the state-of-the-art devices with single FPT process applied on the gate. The maximum V_{TH} obtained from fluorine RIE plasma treatment is only 0.9V, which requires further improvements.

Table 4.1 Gate processing methodology of the state-of-the-art devices with fluorine treatment together with their threshold voltage (V_{TH}) and maximum drain current (I_{DMAX}) respectively

Ref	F Treatment recipe	Dielectric	Post-Gate Treatment	V_{TH}	I_{DMAX}
[27]	150W, CF_4 based RIE for 250s	16nm $LaLuO_3$	400ºC annealing in N_2 ambient for 10 minutes	+0.6V	400mA/mm
[28]	25keV F+ ions implantation. Dosage of 5×10^{12} cm^{-2}	80nm Si_3N_4 as protection layer before F treatment (gate stack details not mentioned)	50W, CF_4 based RIE to remove Si_3N_4	+1.8V	380mA/mm
[29]	150W, CF_4 based RIE for 250s	AlN/Al_2O_3 (2nm/10nm)	400ºC annealing in N_2 ambient for 10 minutes	+0.9V	300mA/mm

In this chapter, a normally-off AlGaN/GaN MIS-HEMT with partial AlGaN recess combining with multiple FPT on the Al_2O_3 gate dielectric is realised to significantly improve the V_{TH} of the device. The partial AlGaN recess weakens the polarisation field at the AlGaN/GaN interface and reduces the 2DEG density. Meanwhile, the multiple FPT can effectively improve the concentration of negative charges within the gate dielectric, thus provide a strong depletion field

to the 2DEG and raise the V_{TH}. With careful design of the multiple FPT recipe, the shortcoming in severe on-state current reduction due to the fluorine-induced damages to the 2DEG [91] can be effectively alleviated. With the assistance of the V_{TH} analytical model, the amount of the FPT-induced negative charge can be precisely guided. Lastly, a monolithic logic inverter is implemented with the combination of such normally-off HEMT as the power switch with a normally-on HEMT as the depletion-load. It mimics the standard pseudo-nMOS configuration.

4.2 Design and modelling of the high-V_{TH} MIS-HEMT

Referring to Section 1.3.2, it is clear that the AlGaN recess and FPT are both effective methodologies on increasing the V_{TH} from negative to positive. However, based on reported data in Table 4.1, single FPT applied on AlGaN does not provide sufficient negative charges in achieving high V_{TH}. Compared to FPT on AlGaN barrier layer, FPT on the gate dielectric enhances the amount of negative charge incorporation without significantly degrading the channel quality. The incorporated fluorine atoms are much further from 2DEG and ineffective to the 2DEG carrier mobility as compared with the FPT directly applied on AlGaN. Due to the precise control of the Al_2O_3 gate dielectric thickness by the atomic layer deposition (ALD) technique, it is possible to obtain good quality of Al_2O_3 with reasonable thickness after multiple fluorine treatments in between each ALD-Al_2O_3 deposition process. Therefore, much

more negative charges from FPT can be introduced into the gate dielectric than single FPT. To further increase the V_{TH} of the device, the AlGaN at the gate region is recessed partially to weaken the polarisation field and hence reduce the induced 2DEG density. The process flow for the gate formation is shown in Fig. 4.1 which illustrates in detail how multiple FPTs are done.

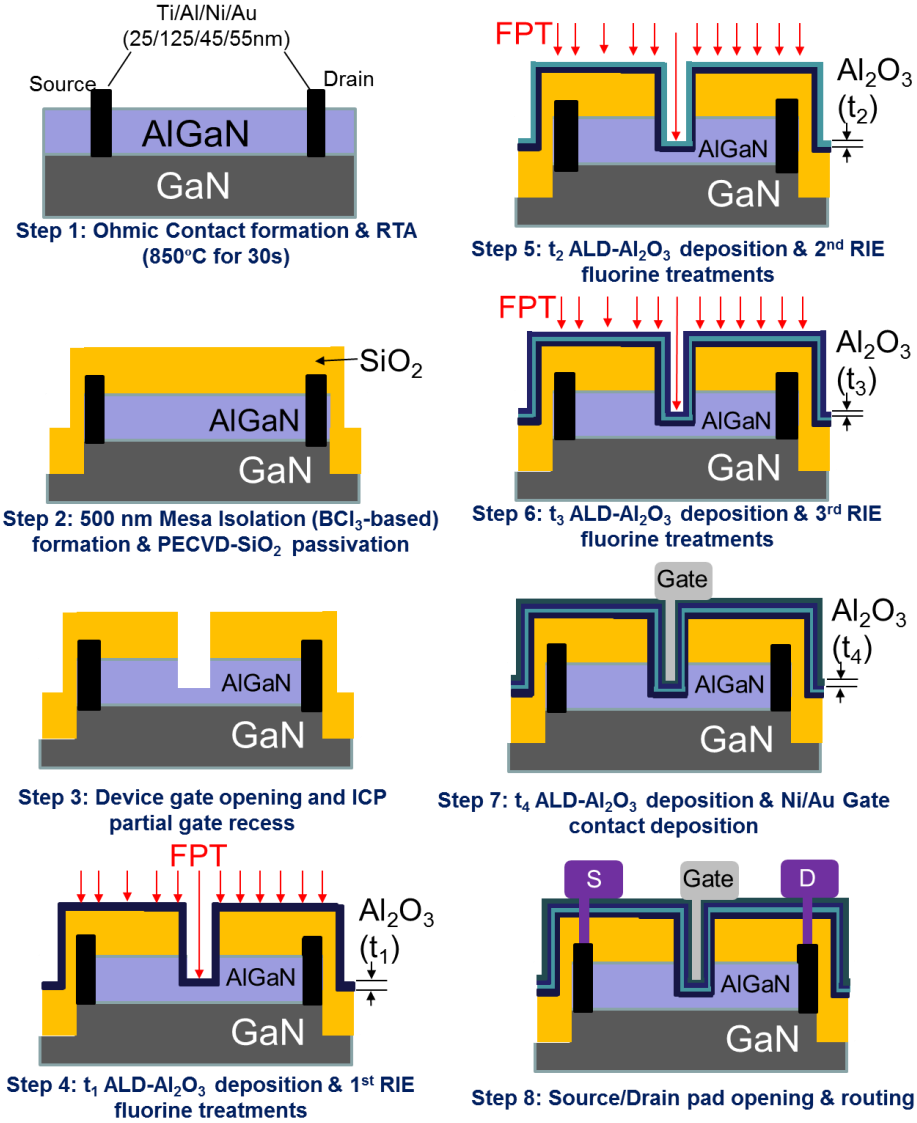


Fig. 4.1 Designed process of the multi-fluorinated Al_2O_3 gate dielectrics

To investigate the location and concentration of negative charges within the gate dielectric, three different sequences of the FPT process are designed and shown in Fig. 4.2. For dies C~E, four separate fluorine treatments are processed with RIE system at RF plasma power of 30W under CHF_3 gas ambient. Low RF plasma power of 30W is selected to minimise the bombardment damage introduced to the sample surface. The processing parameters were obtained from process short-loops under a wide range of conditions. For Die C, FPTs are conducted on both the AlGaN layer (one time) and Al_2O_3 dielectrics (3 times), where the dose is concentrated at the centre of the Al_2O_3 dielectric. For Dies D and E, both devices have eliminated the treatments at the AlGaN layer and the dosage is concentrated at the top surface of Al_2O_3. Die E has even more biased FPT distribution away from the 2DEG to minimise their influences on the channel quality and carrier mobility. A constant negative charge incorporation rate of about 4.65×10^{10} cm^2s^{-1} is extracted based on the FPT recipe used by fitting the V_{TH} of the fabricated devices with the Sentaurus simulation, which will be explained in detail later. Therefore, the incorporated negative charge concentration is in linear proportion to the plasma treatment time, as shown in Fig. 4.2.

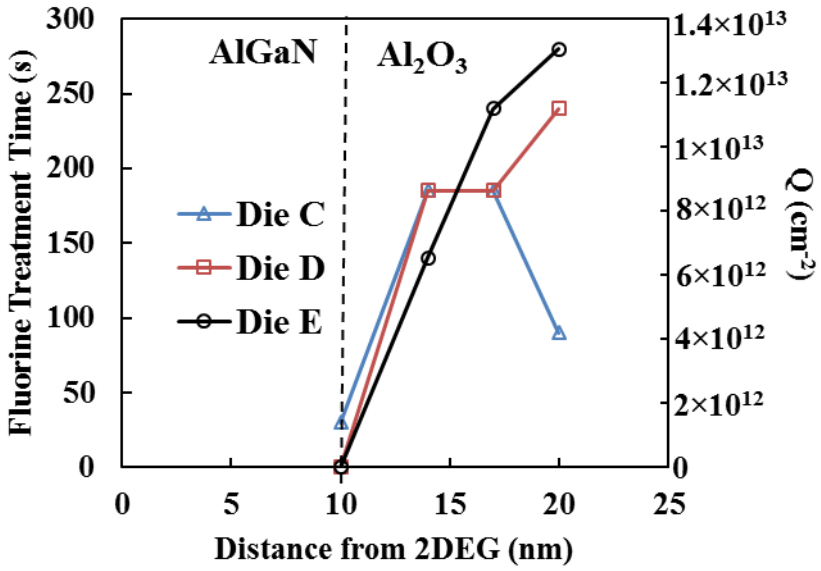


Fig. 4.2 The fluorine treatment time and the concentration of incorporated negative charges (Q) versus the distances of the treatments from the 2DEG applied on Dies C~E

$$V_{TH} = \frac{\phi_b - \Delta E_1 - \Delta E_2 - \Delta E_3}{q} - \frac{qQ_{2DEG}(t_{AlGaN} - t_{recess})}{\varepsilon_{AlGaN}} - \frac{q(Q_{2DEG} + Q_{EQ} + Q_T)}{\varepsilon_{Al_2O_3}} \sum_{n=1}^{4} t_n \tag{4.1}$$

$$Q_{EQ} = Q_1 + Q_2 \frac{t_2 + t_3 + t_4}{t_1 + t_2 + t_3 + t_4} + Q_3 \frac{t_3 + t_4}{t_1 + t_2 + t_3 + t_4} + Q_4 \frac{t_4}{t_1 + t_2 + t_3 + t_4} \tag{4.2}$$

To study the relationship between F ion incorporation through the FPT and the V_{TH} of the device, a V_{TH} model based on [92] has been extended for multi-layer fluorine treatments, which is presented in Eq.(4.1). The first term in Eq. (4.1) shows the band offsets between each layers. With the assistance of the conduction band diagram of Dies B~E shown in Fig. 4.3, the barrier between Ni and Al_2O_3 is ϕ_b=3.5eV [93], and ΔE_1 and ΔE_3 are the conduction band offsets between AlGaN/GaN and Al_2O_3/AlGaN respectively, which added to 2.1 eV [94]. ΔE_2 is the offset of the conduction band from the Fermi level before FPTs, which is −0.16 eV [14]. Permittivities of AlGaN and Al_2O_3 are ε_{AlGaN}=9.2ε_0 and

$\varepsilon_{Al2O3}=7\varepsilon_0$ respectively [14, 94]. The second and the third terms in Eq. (4.1) illustrate the electrostatic potentials across the AlGaN and Al_2O_3 layers respectively. $Q_{2DEG}=6\times10^{12}$ cm^{-2} is the 2DEG density at AlGaN/GaN interface when the thickness of AlGaN is 10nm [14]. $Q_T=-1.5\times10^{12}$ cm^{-2} is the fixed charge density at Al_2O_3/AlGaN interface [95]. Q_{EQ} is the equivalent amount of FPT-induced negative charge located at the Al_2O_3/AlGaN interface which achieves the identical electrostatic effect to the multiple fluorine charges Q_1~Q_4 within the Al_2O_3 gate dielectrics. The Q_{EQ} extracted from Eq. (4.2) is expressed as a sum of portions of Q_1~Q_4 related to their distances from the Al_2O_3/AlGaN interface. In other words, Q_4, which is the furthest to the Al_2O_3/AlGaN interface, has the weakest influence to the value of Q_{EQ}. The concept of Q_{EQ} helps to simplify the relationship between the Q_1~Q_4 and V_{TH}. It enables direct comparison of different combinations of Q_1~Q_4 to V_{TH}. The transformation between Q_1~Q_4 and Q_{EQ} is illustrated in Fig. 4.4 (a). As listed in Table 4.2, these four fluorine plasma treatments are applied on AlGaN surface (Q_1) and three layers of Al_2O_3 deposited by atomic layer deposition (ALD) at 250°C (labelled as Q_2~Q_4 on t_1~t_3). It is observed that the FPT will slightly etch the Al_2O_3 with a rate of 0.02nm/s observed by ellipsometer. Therefore, the deposition thickness of Al_2O_3 of Dies C~E are calibrated to ensure the total Al_2O_3 thickness after FPT are all about 18nm. According to Fig. 4.3, an additional potential barrier ϕ_F is induced after FPT will shift the conduction band at the AlGaN/GaN above the Fermi level, resulting in positive V_{TH}.

Fig. 4.4 (b) shows the relationship between V_{TH} and Q_{EQ} for data from model prediction (which is shown as dashed line in Fig. 4.4) by Eq.(4.1), Sentaurus simulations, measurement from previous work [91] and extracted V_{TH} on Dies B~E, which will be discussed in Section 4.4. The V_{TH} extracted from Sentaurus simulation used different combinations of Q_2, Q_3, and Q_4 at their respective locations to show the accuracy of V_{TH} extracted by the model using Q_{EQ}. The model prediction is realistic for all cases regardless of the amount and location of fluorine charge applied. In general, V_{TH} increases linearly with Q_{EQ}, indicating a higher potential barrier ϕ_F is induced by more FPT-induced negative charges incorporated within the Al_2O_3 gate dielectrics. Die E is expected to have the highest V_{TH} at around 6.5V due to its highset Q_{EQ}.

Table 4.2 Summary of the multiple FPT gate processing parameters for Dies C, D, and E.

Dies	**C**	**D**	**E**
1st F^- treatment time (s)	30	0	0
1st F^- treatment conc. [Q_1] (cm^{-2})	-1.40×10^{12}	0	0
2nd F^- treatment time (s)	185	185	140
2nd F^- treatment conc. [Q_2] (cm^{-2})	-8.60×10^{12}	-8.60×10^{12}	-6.51×10^{12}
3rd F^- treatment time (s)	185	185	240
3rd F^- treatment conc. [Q_3] (cm^{-2})	-8.60×10^{12}	-8.60×10^{12}	-1.21×10^{13}
4th F^- treatment time (s)	90	240	280
4th F^- treatment conc. [Q_4] (cm^{-2})	-4.19×10^{12}	-1.12×10^{13}	-1.30×10^{13}
Equivalent F^- conc. [Q_{EQ}] (cm^{-2})	$\mathbf{-1.52\times10^{13}}$	$\mathbf{-1.69\times10^{13}}$	$\mathbf{-1.82\times10^{13}}$
ALD-Al_2O_3 **t_1, t_2, t_3, t_4** (nm)	7.4, 6, 4.3, 8	7.4, 6, 7.6, 8	6.5, 7.3, 7.6, 8
Total thickness considering RIE etching by F^- treatments (nm)	**18.00**	**18.15**	**18.10**

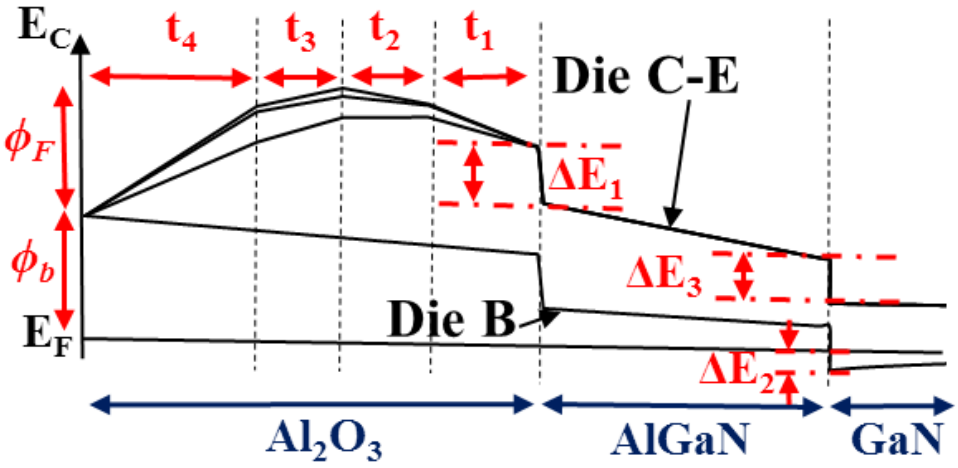


Fig. 4.3 Schematic conduction band energy (E_C) diagram along the gate region for Dies B~E.

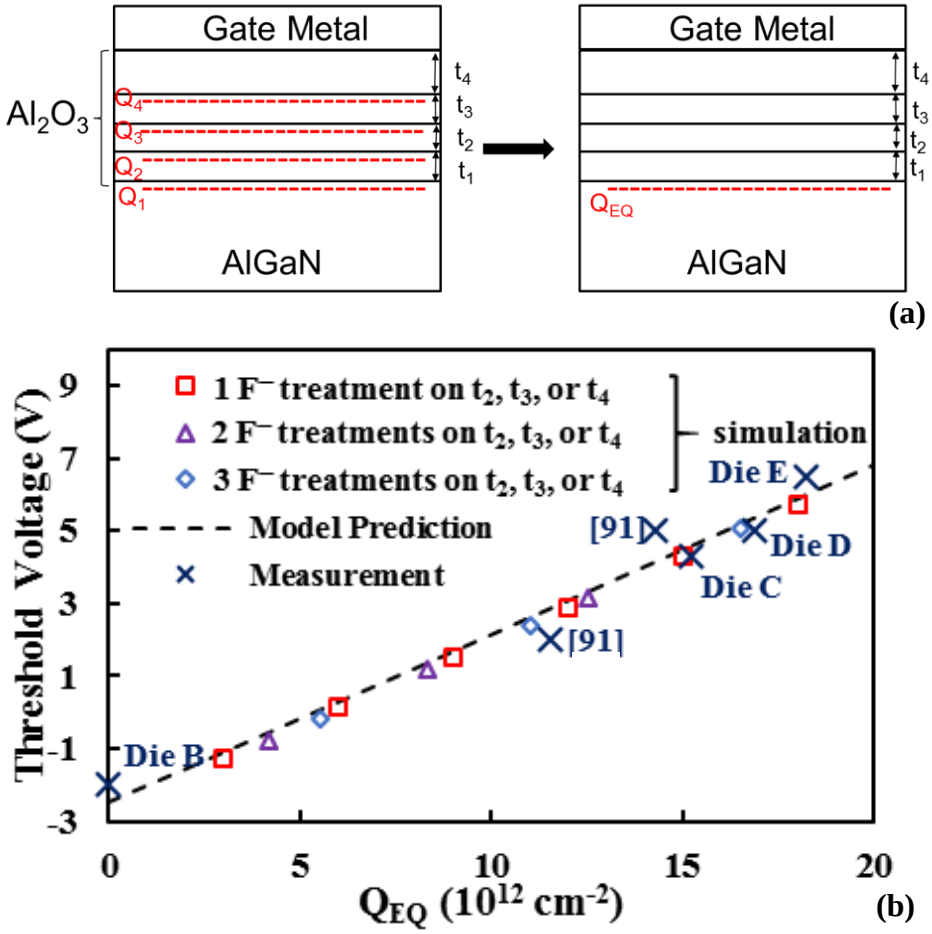


Fig. 4.4 (a) The schematic of Q_1~Q_4 and Q_{EQ} transformation **(b)** Relationship between V_{TH} and Q_{EQ} for data from model prediction (dash line), Sentaurus simulations, laboratory measurements from Dies B~E and previously reported work [91].

4.3 Fabrication process of the high-V_{TH} MIS-HEMT

The process parameters used for the gate stack formation are already demonstrated in Table 4.2 and verified by Sentaurus TCAD simulations [34]. The cross-sectional schematic diagram of the HEMT device in which the multi-layer fluorinated dielectric stack is shown in Fig. 4.5 (b). The epitaxial AlGaN/GaN on Si substrate has the 2DEG density and carrier mobility of 8.5×10^{12} cm^{-2} and 1450 $cm^2/V\cdot s$ respectively. The L_G, L_{GD} and L_{GS} are 3μm, 5μm and 5μm respectively. After mesa isolation by BCl_3-based ICP-RIE and SiO_2 dielectric deposition by PECVD, metal stacks made of Ti/Al/Ni/Au (25/125/45/55 nm) were deposited by the thermal evaporator and ohmic contacts were formed by post-deposition rapid thermal annealing (RTA) at 850°C for 30s. According to the transmission line measurements (TLM), the specific contact resistance of the ohmic contact is 2.4×10^{-6} Ωcm^2. About 10nm (which is about 50% of the total AlGaN thickness) of AlGaN barrier layer was recessed at the gate region by low power BCl_3-based ICP-RIE. The partial gate recess reduces the 2DEG concentration without severely damaging the AlGaN/GaN interface, thus the carrier mobility in the 2DEG channel can be preserved. To benchmark with the fluorinated Dies C~E, normally-on AlGaN/GaN MIS-HEMT dies without and with partial gate recess process were fabricated and labelled as Dies A and B.

For dies C~E, four separate fluorine treatments were processed with RIE system at RF plasma power of 30W under CHF_3 gas ambient. The processing parameters were obtained from process short-loops under a wide range of conditions. As listed in Table 4.2, these four fluorine plasma treatments were applied on AlGaN surface (Q_1) and on three layers of Al_2O_3 deposited by atomic layer deposition (ALD) at 250°C (labelled as Q_2~Q_4 on t_1~t_3). For Die E, the secondary ion mass spectroscopy (SIMS) measurement shown in Fig. 4.5 (a) was carried out to observe the F distribution within the gate dielectric. Three distinctive peaks of F concentration are found at t_1, t_2, and t_3, showing the effectiveness of FPT on F incorporation at the desired location. The integrated F concentrations of the three peaks at t_1, t_2, and t_3 are 1.76×10^{22} cm^{-2}, 3.2×10^{22} cm^{-2}, and, and 3.85×10^{22} cm^{-2} respectively. They give the similar ratio of $Q_2:Q_3:Q_4 = 1:1.82:2.15$ used in the Sentaurus simulation and Eq. (4.1). After the multiple fluorine plasma treatments, additional 8nm of Al_2O_3 (t_4) was deposited before the gate metal deposition. This helps to avoid the interactions between the negative charges incorporated by FPT with the traps at the metal/Al_2O_3 interface. Dies C~E have identical t_1, t_2, and t_3 thickness of 4nm, 3nm, and 3nm respectively after the FPTs due to the etching effect of the fluorine plasma. Finally, Ni/Au (15/150nm) layers were deposited by the thermal evaporator as gate metal. The cross-sectional schematics and SEM photo of gate region are shown in Fig. 4.5 (b).

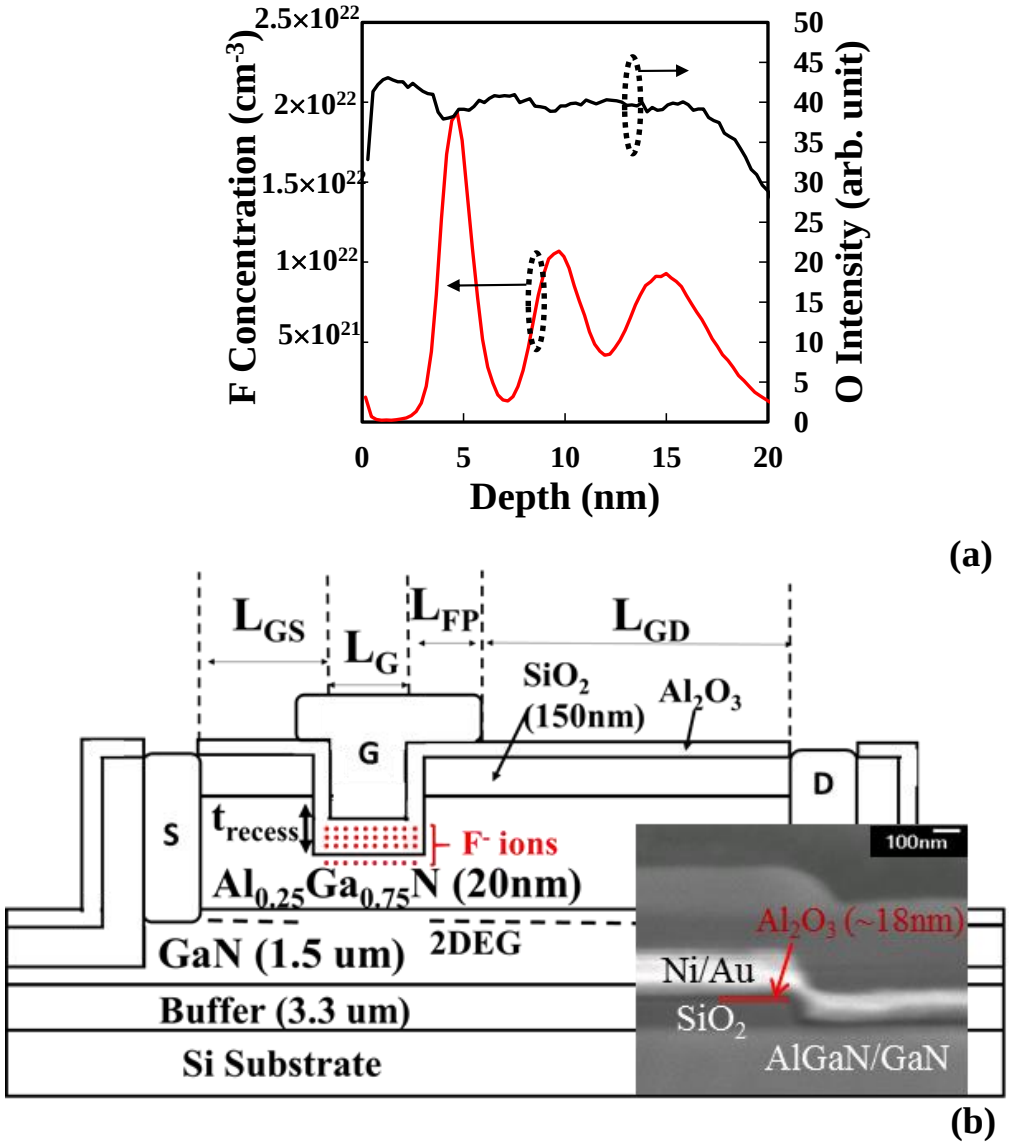


Fig. 4.5 (a) Fluorine profile within the Al_2O_3 of Die E characterised by SIMS; **(b)** Schematic of the normally-off HEMT device treated with partial AlGaN recess and fluorine plasma treated at the gate region. The SEM cross-sectional image of the gate region of the fabricated device is also demonstrated.

4.4 Characterisation of the high-V_{TH} MIS-HEMT

Fig. 4.6 shows the measured I_D-V_G, and the transconductance (g_m) of Dies A~E at V_D = 1V. The V_{TH} is extracted by extrapolating the tangent of the I_D-V_G characteristics at the voltage where g_m is at maximum. The recess-only Die B shifts the V_{TH} from −4.8V to −2.0V, showing the reduction of the polarisation

field and the 2DEG density after partial AlGaN recess. The Dies C~E that underwent fluorine plasma treatments have shifted the V_{TH} to normally-off operations, where Die E has the highest V_{TH} of +6.5V. The measured V_{TH} agrees with the design based on the V_{TH} analytical model as shown in Fig. 4.4. Consistent V_{TH} is obtained for all dies C~E from the I_D-V_G measurements when V_D=8V, as summarised in Table 4.3. It shows that the V_{TH} are stable when the devices are at the saturated region. Meanwhile, the maximum g_m=28mS/mm for Die E is similar to the untreated Die B. It indicates trivial degradation on the sub-threshold swing after the partial recess and multiple FPTs at the gate.

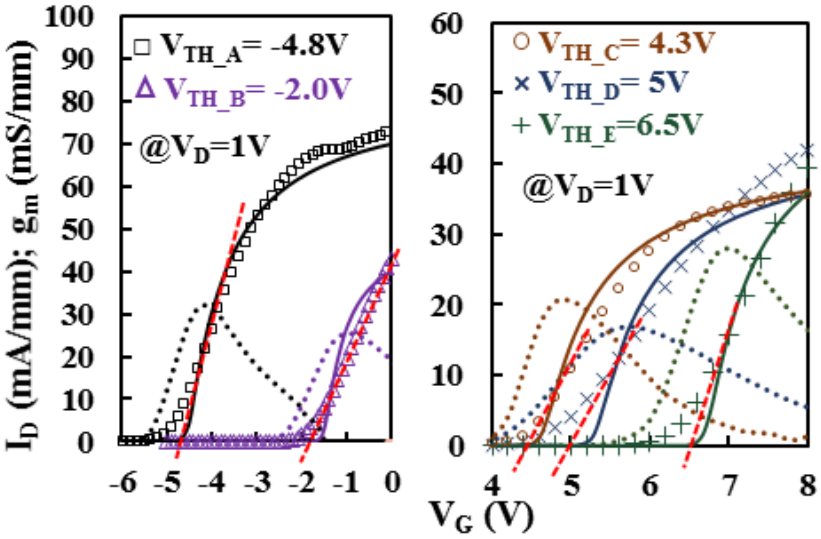


Fig. 4.6 Comparison of measured I_D-V_G (data points) on devices Dies A~E at V_D=1V. V_{TH} is obtained by linear extrapolating the I_D-V_G at the gate voltage where the maximum g_m (dotted lines) occurs.

Table 4.3 The V_{TH} of Dies C~E when V_D=1V and 8V

	Die C	**Die D**	**Die E**
V_{TH} at V_D=1V	4.3	5.0	6.5
V_{TH} at V_D=8V	4.2	4.8	6.4

Fig. 4.7 shows the I_D-V_G and I_G-V_G characteristics of Dies A~E in logarithmic scale. Low gate leakage current I_G of around 1nA/mm at V_G=12V is observed for Die E, indicating the preservation of dielectric quality after the multiple FPT process. However, FPT on the AlGaN barrier such as in the case of Die C provides a trap-assisted leakage path between the 2DEG and the gate metal contact. It results in high gate leakage and poor device reliability. Numerous characterisations on the V_{TH}, I_G and I_{DMAX} stability after terminal stresses have been conducted on Die E for reliability and stability verification. Less than 5% variation in V_{TH} is found after ten I_D-V_D sweeps. The I_D-V_D sweeps are done with V_D swept from 0V to 10V at V_{GT}= V_G−V_{TH} =10V with 1s holding of V_D at 10V after each sweep. Less than 6% reduction in I_{DMAX} is also observed if a 50ms-pulsed V_{GT} from −5V to 10V is applied before each I_D-V_D data point extraction. The values selected for gate and drain stress are to maximise the stressing conditions to ensure the device is reliable. In terms of the current collapse effect, the increase in the dynamic on-resistances (R_{on}) measured for Dies A, B, and E after off-state biasing V_D at 200V for 10s are 11.2%, 19.7%, and 61.3% respectively. Even though a significant increase in R_{on} is found for Die E, it is comparable to other fluorine-treated devices reported in [26]. The current collapse can be possibly mitigated by reduce the surface trap concentration or the peak electric field [3], which is achievable through surface passivation layer deposition and field plate implementation [96].

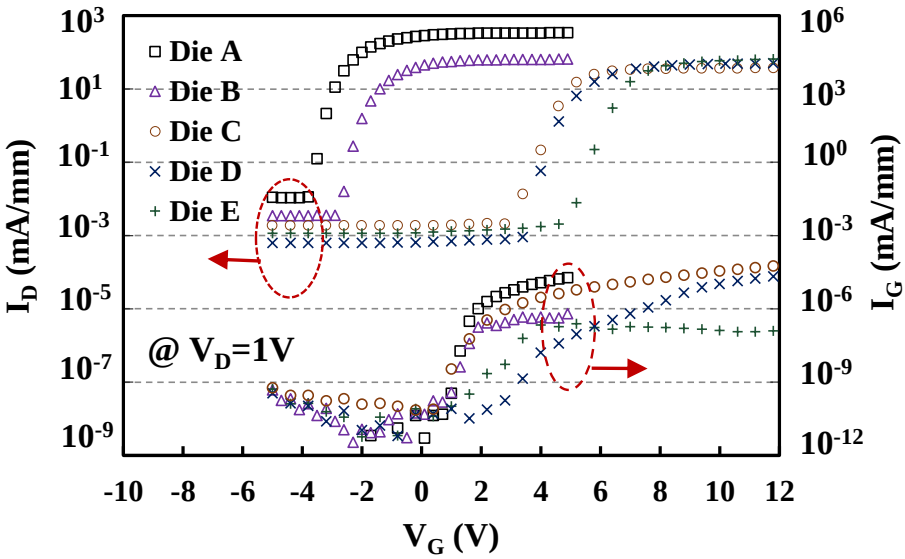


Fig. 4.7 I_D-V_G characteristics and I_G-V_G of Dies A-E at V_D=1V in log scale. Low off-state gate leakage current of 1 nA/mm is observed for Die E.

Fig. 4.8 (a) shows the on-state I_D-V_D characteristics of Dies A~E at gate overdrive voltage V_{GT} of 10V. The I_{DMAX} is defined as the maximum drain current in the saturation region when $V_{GT}=V_G-V_{TH}$=10V. After FPTs, a moderate 29% reduction in I_{DMAX}, which reduces from 490mA/mm to 350mA/mm, is observed for Dies D & E compared to normally-on Die A with neither gate recess nor FPTs on the gate. However, for Die C which also conducted FPT on AlGaN, about 60% reduction in I_{DMAX} is observed. It indicates that applying FPT directly on the AlGaN surface has deteriorated the AlGaN/GaN interface and reduced the carrier mobility of the 2DEG. The 2DEG carrier mobilities at the gate region shown in Table 3.3 are obtained from fitting the I_D-V_D characteristics in Fig. 4.8 (a) with Sentaurus simulations for Dies A~E. In agreement with the most I_{DMAX} degradation, the lowest 2DEG mobility is observed in Die C. In Fig. 4.8 (b), the off-state I_D-V_D characteristic of Die E with L_{GD}=15μm and L_{FP}=2.5μm at V_G =0V is shown. A maximum breakdown voltage of 1140V is obtained for Die E. It agrees with the designed rating

obtained from simulation [97] thus confirms the suitable gate formation without any premature breakdown. The comparison of V_{TH} and I_{DMAX} with other reported state-of-the-art AlGaN/GaN normally-off power HEMTs are shown in Fig. 4.9. Dies D and E reported in this chapter have the highest V_{TH} with competitive I_{DMAX} compared to the other reported devices.

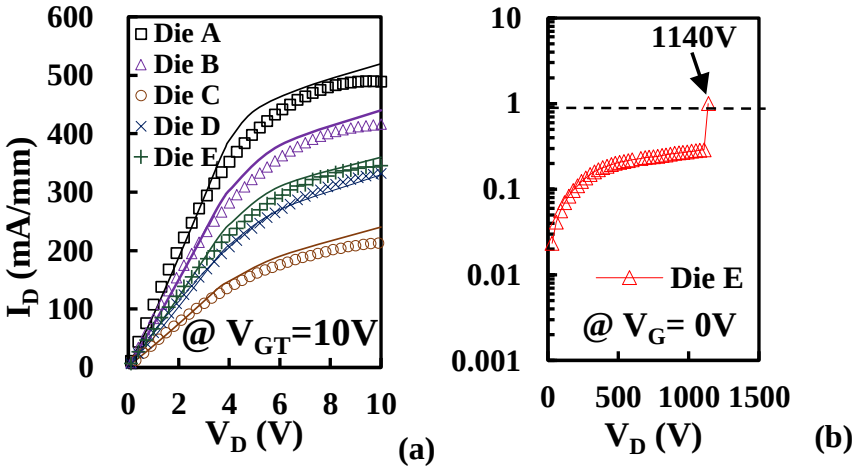


Fig. 4.8 (a) On-state I_D-V_D with measured data points and simulated solid lines of Dies A~E at V_{GT}=10V demonstrated. **(b)** Off-state I_D-V_D characteristic for Dies E at V_G=0V.

Table 4.4 The 2DEG carrier mobility for Dies A~E from simulations in Fig. 4.8 (a)

Dies	**A**	**B**	**C**	**D**	**E**
Mobility ($cm^2/V{\cdot}s$)	1450	1200	600	1000	1050

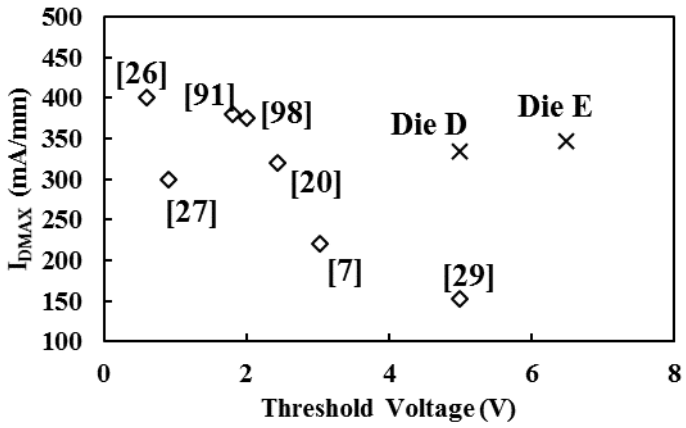


Fig. 4.9 Benchmark of V_{TH} and I_{DMAX} of Dies D & E with published state-of-the-art normally-off power AlGaN/GaN HEMTs [7, 20, 26, 27, 29, 91, 98]. Highest V_{TH} and a competitive I_{DMAX} are observed for Dies D and E.

4.5 Fabrication and characterisation of GaN-based monolithic inverter

In Sections 4.1 to 4.4, the enhancement-mode (V_{TH}>0V, E-mode) AlGaN/GaN MIS-HEMT with high V_{TH} and good conductivity was fabricated with multiple FPTs. Therefore, a monolithic logical inverter can be realised by integrating this normally-off MIS-HEMT with a depletion-mode (V_{TH}<0V, D-mode) AlGaN/GaN MIS-HEMT without any gate recess or FPTs at the gate region. A well-performed GaN-based inverter enables the full integration of control and current sensing unit for power integrated circuits with potentially low-cost GaN-on-Si wafers. In this section, a depletion-load NMOS inverter is fabricated with much enhanced noise margins and high output swing than conventional Si-based CMOS.

As indicated in the designed fabrication flow in Fig. 4.10, the inverter fabrication process begins with Ti/Al/Ni/Au (25/125/45/55 nm) ohmic contacts formed by RTA at 850°C for 30s. Then, 500nm-deep mesa isolation is formed by BCl_3-based ICP-RIE and 150nm SiO_2 dielectric deposition by PECVD for surface passivation. After opening the gate area at the normally-off region, about 10nm of AlGaN (50% of the original thickness) is recessed by low power BCl_3-based ICP-RIE to reduce the 2DEG concentration without damaging the AlGaN/GaN interface that degrades the electron mobility. Three cycles of ALD-Al_2O_3 depositions at 250°C and 30W of CHF_3-based RIE treatment were

applied to introduce sufficient F^- charges in the gate region for high V_{TH} for the normally-off devices [37]. Same as the fluorine treatment recipe utilised for Die E reported in Section 4.1 to 4.4, longer treatment time was applied on the top layer to minimise the penetration of fluorine atoms into the 2DEG channel that may create impurity scattering and mobility degradation. Then, the gate dielectric at the D-Mode gate region was etched away to remove the fluorine-treated Al_2O_3. 8nm of ALD-Al_2O_3 was deposited as the normally-on device gate dielectric and the last gate dielectric layer for the normally-off devices. This layer was applied to prevent high gate leakage by spacing the fluorinated normally-off gate stack away from the gate metal. Considering the CHF_3 plasma etching on Al_2O_3, the total Al_2O_3 thickness of 18.1nm for the normally-off device was obtained after the FPTs. Lastly, 15/150nm of Ni/Au was deposited as the gate metal. The gate length (L_G), gate-drain length (L_{GD}), gate-source length (L_{GS}), field-plate length (L_{FP}) for both normally-on and normally-off devices are 3μm, 10μm, 5μm and 1.5μm respectively. The cross-sectional schematic of the devices with metal routing to each other and the equivalent circuit diagram of the inverter are shown in Fig. 4.11. In this configuration, the normally-off HEMT is acted as the logic switch, while the normally-on HEMT is acted as the resistive load. Due to the absence of well-performed GaN-based PMOS transistor, such depletion-load NMOS configuration is a competitive substitution to CMOS configuration for GaN-based logic inverter applications. The specific steps and processing parameters used for gate fabrication are

summarised in Table 4.5. The equivalent F^- sheet concentrations of each layers are obtained by fitting the measured V_{TH} with Sentaurus TCAD simulations based on the same method used in [37] and Section 4.2.

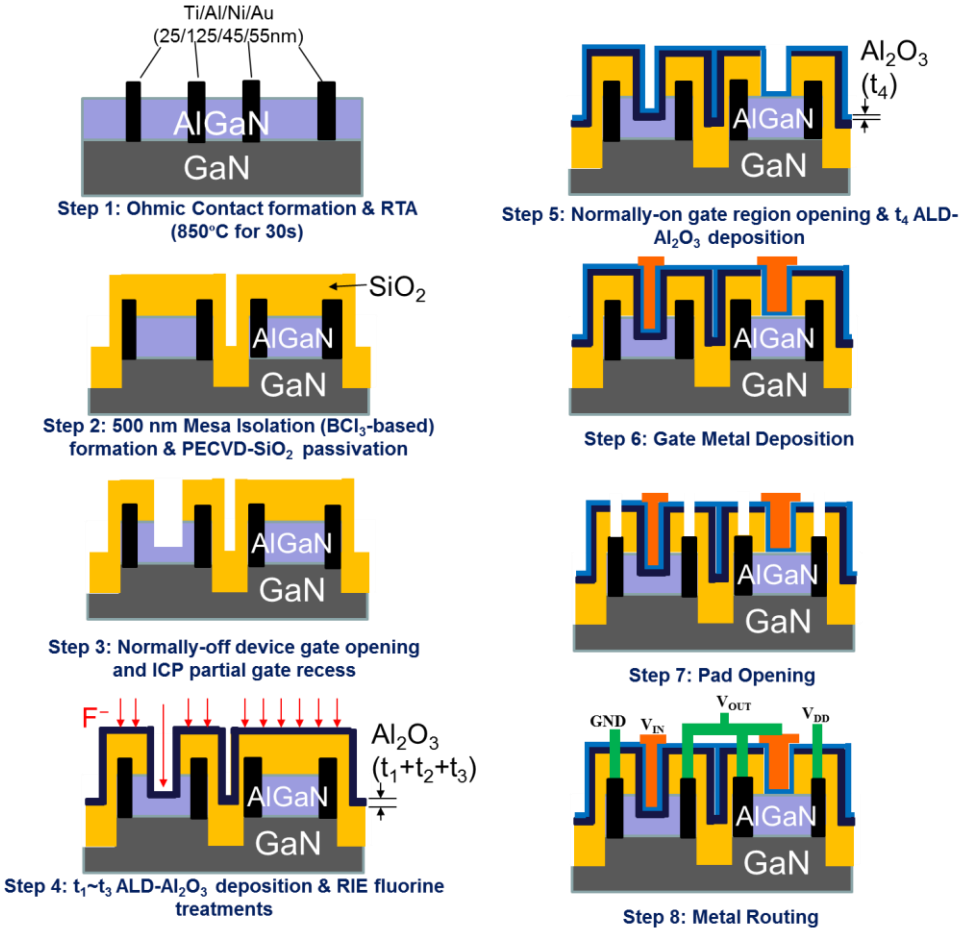


Fig. 4.10 The designed fabrication process flow of the monolithic inverter

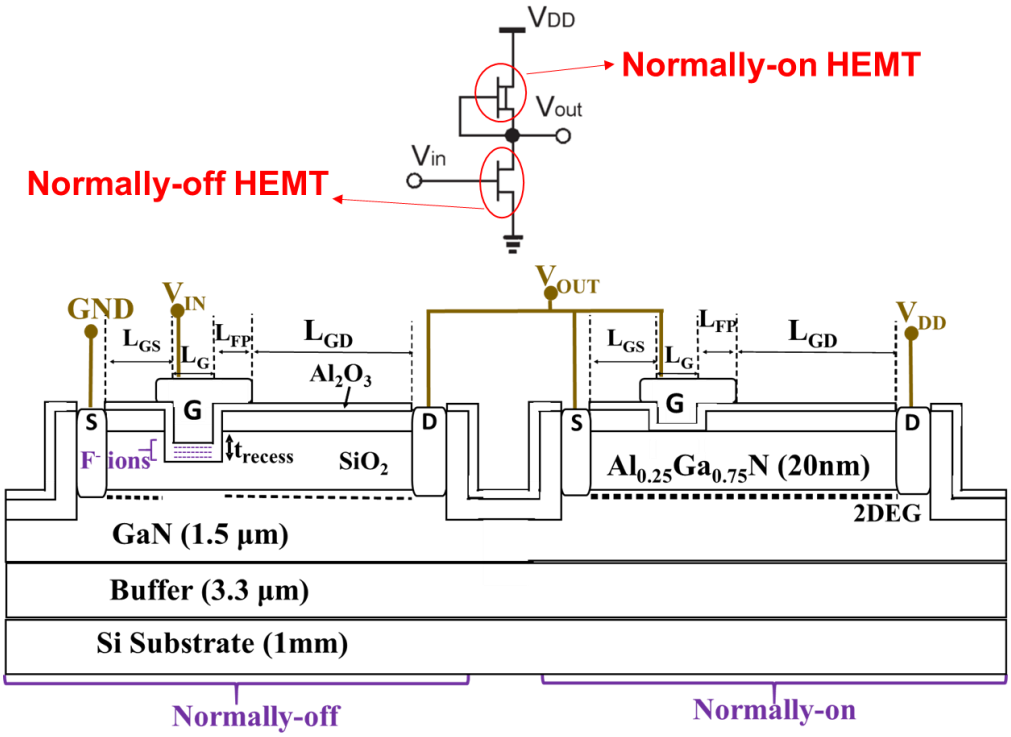


Fig. 4.11 Cross-sectional schematics of the monolithic logic inverter with normally-on and normally-off devices connected as depletion-load NMOS inverter configuration. The equivalent circuit diagram of the logic inverter is shown above.

The surface morphology of Al_2O_3 dielectrics before and after FPT is shown in Fig. 4.12 (a) and (b). The surface roughness RMS of the dielectric surface has increased from 0.648nm to 1.14nm after FPTs, showing the introduction of plasma-induced damage. However, such increase in surface roughness is not influential to the carriers in the 2DEG channel at the AlGaN/GaN interface. It does not result in any degradation in gate leakage.

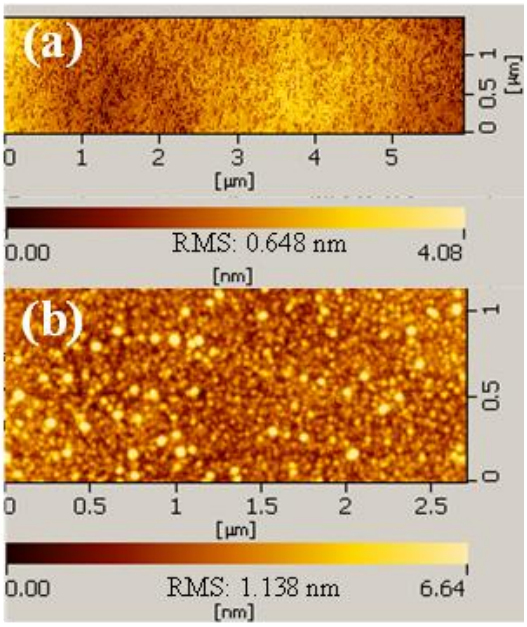


Fig. 4.12 The AFM image of the Al_2O_3 surface **(a)** without and **(b)** with FPT. The surface roughness RMS has trivially increased by about 0.5 nm after treatments.

Table 4.5 The fabrication process and the respective parameters used for the gate region

Step	Process	Parameters
1	AlGaN partial recess at normally-on region	Cl_2 ICP @ 30W for 30s
2	ALD-Al_2O_3	6.5 nm
3	F^- treatment	CHF_3 RIE @ 30W for 140s F^- Conc.~= -6.51×10^{12} cm^{-2}
4	ALD-Al_2O_3	7.3 nm
5	F^- treatment	CHF_3 RIE @ 30W for 260s F^- Conc.~= -1.21×10^{13} cm^{-2}
6	ALD-Al_2O_3	7.6 nm
7	F^- treatment	CHF_3 RIE @ 30W for 280s F^- Conc.~= -1.30×10^{13} cm^{-2}
8	Fluorinated Al_2O_3 removal at the normally-on region	BCl_3 ICP @ 200W for 180s
9	ALD-Al_2O_3	8 nm
10	Gate metal deposition	Ni/Au (15/150 nm)

The static voltage transfer characteristics (VTC) performance of the monolithic inverter with different width ratio between normally-off and normally-on HEMTs (W_{ratio}) of 20, 35, and 50 are shown in Fig. 4.13. The VTC

is a figure of merit for the static behaviour of the inverter. A sharp transition between the high and low conditions with large swing are desired. In the VTC characteristics, the definition of input-low (V_{IL}, lower voltage when slope=−1), output-low (V_{OL}, lowest output voltage), input-high (V_{IH}, higher voltage when slope=−1), output-high (V_{OH}, highest output voltage) are also shown. The above parameters extracted together with the ratio between the output voltage swing and maximum V_{IN} (S/V_{INMAX}), low noise-margin (N_{ML}), and high noise-margin (N_{MH}) voltages have been summarised in Table 4.5. It is observed that W_{ratio}=35 resulted in the highest S, N_{ML} and N_{MH}. Comparing with 82.8% of the GaN-based inverter reported in [99] and 80.3% of the Si CMOS inverter shown in [100], a much higher S/V_{INMAX} of 96.6% is achieved for the inverter fabricated with W_{ratio} of 35. It indicates good conductivity in both normally-on and normally-off HEMTs within the inverter. Therefore, there is much reduced voltage drop through the normally-off device when the input is high.

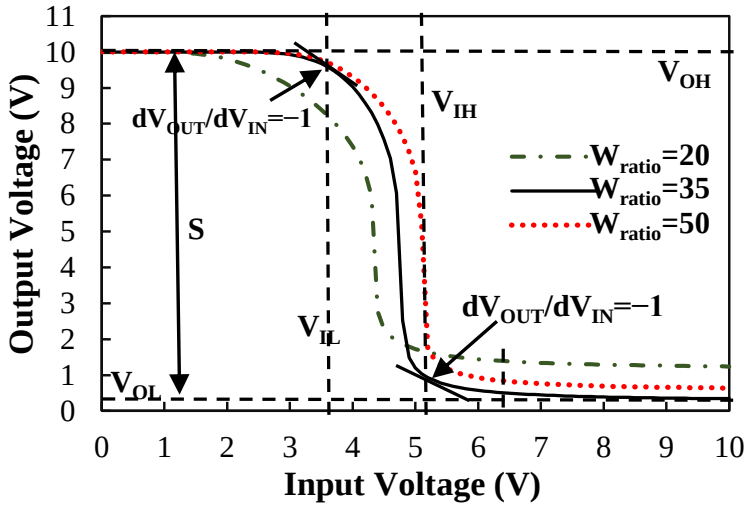


Fig. 4.13 Voltage-transfer characteristics (VTC) of the monolithic inverter with W_{ratio} of 20, 35, and 50. The definitions of V_{OL}, V_{IL}, V_{OH}, and V_{IH} are shown.

The dynamic performance of the inverter with W_{ratio}=35 at f=100 kHz has been demonstrated in Fig. 4.14. Successful and fast inverter switching from 0V to 10V is observed on input and output signals in Fig. 4.14(a). In Fig. 4.14(b), the rise of V_{OUT} waveform is shown along with the indicators of propagation delay from low to high (τ_{PLH}, the time difference between V_{IN} and V_{OUT} at 50% of V_{OH}) and rise time (τ_{rise}, the time different between 90% V_{OH} and 10% V_{OH}). All of the abovementioned parameters along with two additional characterisations on the propagation delay from high to low (labelled as τ_{PHL}) and the fall time (labelled as τ_{fall}) for W_{ratio}=20, 35 and 50 have been summarised in Table 4.5. It is found that there is a trade-off between the response times when the inverter is switching at different W_{ratio}. An optimal switching behaviour is observed when W_{ratio}=35. The propagation delay times of around 90ns for the fabricated inverter is comparable with the typical values of the inverters used in the high power and high frequency DC/DC converters [101].

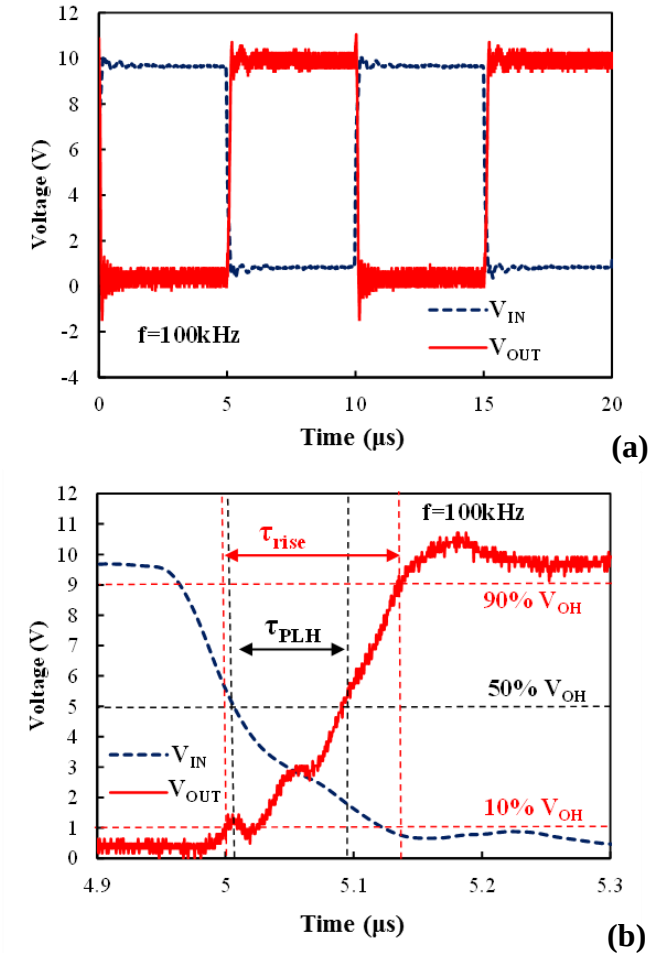


Fig.. 4.14 Dynamic performance of the monolithic inverter with W_{ratio}=35 at f=100 kHz with timespan of **(a)** 0~20 μs which shows complete switching periods and **(b)** 4.9~5.3 μs which presents the switch-on transient for V_{OUT} and the definition of τ_{PLH} and τ_{rise}.

Table 4.6 Summary of the performance of the monolithic inverter

W_{ratio}	**20**	**35**	**50**
V_{IL} (V)	2.9	3.6	3.8
V_{OL} (V)	1.24	0.34	0.64
V_{IH} (V)	4.6	5.1	5.4
V_{OH} (V)	10	10	10
S/V_{INMAX} (%)	87.6	96.6	94.6
$NM_L = V_{IL} - V_{OL}$ (V)	1.66	3.26	3.16
$NM_H = V_{OH} - V_{IH}$ (V)	5.40	4.90	4.60
τ_{PLH} (ns)	35	90	110
τ_{PHL} (ns)	90	80	73
τ_{rise} (ns)	100	135	140
τ_{fall} (ns)	90	40	35

4.6 Conclusion

In this chapter, a technique that combined partial AlGaN barrier layer recess with multiple fluorine treatments on dielectric stack was proposed to target for higher amount of negative charge incorporation within the gate dielectric stack while minimising the damage to 2DEG channel. Al_2O_3 deposited by atomic layer deposition (ALD) technology was applied in order to meet the requirement of high quality thin dielectric layers for the gate dielectrics. In addition, a monolithic inverter with large output swing and fast switching time was realised by combining the abovementioned normally-off device with a normally-on MIS-HEMT.

A normally-off AlGaN/GaN MIS-HEMT with high V_{TH} of +6.5V, competitive I_{DMAX} of 320mA/mm and good breakdown voltage of 1140V was achieved by partial AlGaN recess and multiple FPTs on the gate dielectric. The modelling on the relationship between multi-FPT-processed Al_2O_3 gate stacks

and V_{TH} has also been proposed to guide the gate region design. Good agreement on the simulated V_{TH} was verified by the I_D-V_G characterisations on the fabricated devices.

Lastly, a monolithic inverter based on GaN normally-off and normally-on MIS-HEMT configuration have been fabricated. The well-performed normally-off device as the driving transistor of the inverter enhances both the output voltage swing and the noise margins significantly. A better output swing and switching speed were realised as compared with conventional Si-based CMOS inverter.

CHAPTER 5 Fluorinated Trap Distribution within Al_2O_3 Gate Dielectric for Normally-off AlGaN/GaN MIS-HEMTs

5.1 Introduction

In previous chapters, it was observed that the normally-off AlGaN/GaN HEMT device with positive gate threshold voltage ($V_{TH} > 0$) is one of the most important properties required in power system switching applications for system controllability, safety, and standby power minimisation. To fabricate such device, AlGaN barrier recess [98] and fluorine plasma treatment [9, 26, 28, 99, 102] on the gate region are two of the approaches used to weaken the polarisation in the 2DEG conduction channel and induce an additional vertical electric field to deplete the carriers in the HEMT structure. For the devices underwent multiple fluorine plasma treatments (FPT) on ALD-Al_2O_3 gate dielectric combined with partial AlGaN recess, which was reported in Chapter 4 and [37], they allowed a significant amount of fluorine-induced negative charge (F^-) to be incorporated at the gate stack. As a result, high threshold voltage of +6.5V was obtained with satisfactory maximum drain current (I_{DMAX}) of 340mA/mm and off-state breakdown voltage of 1130V. However, a significant decrease in V_{TH} is found when devices operate at higher temperature. Therefore, it is necessary to study the distribution of trap states in the Al_2O_3 gate

dielectric bandgap after the FPTs to investigate the stability of the F^- within the gate dielectric at higher temperature.

This chapter studies the fluorine-induced negatively charged traps (F^-) within the Al_2O_3 gate dielectric by the gate stressing characterisation based on the V_{TH} model [37] and the Poole-Frenkel trap emission theory. Using such technique, the trap state concentrations at corresponding energy levels within the Al_2O_3 gate dielectrics can then be found. Hence, the V_{TH} stability for the fluorine-plasma treated AlGaN/GaN MIS-HEMTs under high temperatures can be understood.

5.2 Design and fabrication of HEMT devices with different RIE fluorine plasma power

The structure of the normally-off Al_2O_3/AlGaN/GaN MIS-HEMTs used in this chapter is based on the design for Die E in Chapter 4. According to Section 4.4, it is found that the Die E with most of the FPT processed closer to the Al_2O_3 surface is able to sustain the high-V_{TH} with least on-state current reduction compared to other FPT configurations reported. Therefore, in this chapter, the same FPT recipes applied on the same locations as the Die E in Chapter 4 are implemented with variations in the RF plasma power.

In Table 5.1, three different RIE recipes have been used for Dies A, B and C respectively with gate processing parameters listed. For Die A, 30W of RF power with 50 scum of CHF_3 gas is used in each of the treatments. This gate

processing recipe is identical to the Die E reported in Chapter 4. Higher RF power of 60W and 90W with the same flow of CHF_3 gas are used for Die B and C respectively to enhance the breaking of Al-O bonds, since the higher RF power has enhanced the ion bombardment and the fluorine radical concentration ionised from CHF_3.

The AlGaN/GaN HEMT device structure with multiple fluorine plasma treatments on the gate dielectric used for this work is shown in Fig. 5.1 (a). The fabrication began with the formation of Ti/Al/Ni/Au (25/125/45/55 nm) ohmic contacts with rapid thermal annealing (RTA) at 850°C for 30s. Then, 500nm-deep mesa isolation was obtained on the dies by BCl_3-based inductively coupled plasma reactive ion etching (ICP-RIE). 150nm of SiO_2 dielectric was deposited by PECVD for surface passivation. After the gate region opening, about 10nm of AlGaN, which is 50% of the total AlGaN layer thickness, was recessed by low power BCl_3-based ICP-RIE. Therefore, the 2DEG concentration under the gate is reduced yet the 2DEG mobility at the AlGaN/GaN interface is maintained. Followed by the first layer of Al_2O_3 deposition at 250°C by atomic layer deposition technique (ALD), three cycles of FPTs combining with ALD-Al_2O_3 gate dielectric depositions were used for gate stack formation. With this approach, sufficient F^- charges were introduced in the gate region for high V_{TH}. Longer FPT processing time was applied on the top layer of Al_2O_3 to minimise F^- penetration into the 2DEG channel region, which can possibly create degradation of 2DEG mobility. Considering the CHF_3 plasma etching on Al_2O_3,

the final Al_2O_3 thickness of 18.1nm is obtained. The thickness of each deposited layers was verified by the Scanning Electron Spectroscopy (SEM) image, which is shown in the inset of Fig. 5.1(a). The change in surface morphology after the FPT was assessed in the atomic force microscopy (AFM) image shown in Fig. 5.1 (b) and (c). The surface roughness RMS was increased from the un-fluorinated sample of 0.648nm to the fluorinated Die A of 1.138nm. It implies the increase in the surface dangling bonds and possible trapping sites after fluorination. For comparison, a benchmarking sample with 18nm of Al_2O_3 deposited after gate recess but without any fluorine plasma treatments was also fabricated and labelled as the "recess-only" device.

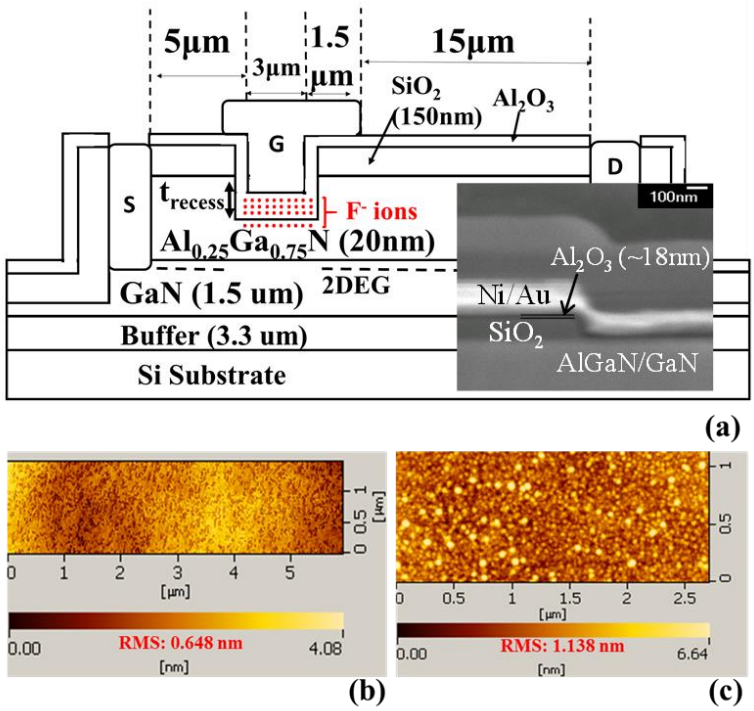


Fig. 5.1 (a) Cross-sectional schematic of the fabricated normally-off MIS-HEMT device, where the inset shows the cross-sectional SEM image of the fabricated device near the gate region. The approximate thickness of each of the layers is also shown; AFM image of the Al_2O_3 surface **(b)** without and **(c)** with fluorine plasma treatments (Die A);

The analytical model of the V_{TH} of fluorinated HEMT devices is shown in Eq. (5.1) [37]. The barrier ϕ_b between Ni and Al_2O_3 is 3.5eV. ΔE_1 and ΔE_3 are the conduction band offsets between Al_2O_3/AlGaN and AlGaN/GaN respectively, which added to 2.1eV. ΔE_2 is the conduction band offset from the Fermi level prior to the FPTs, which is –0.16eV. The permittivities of AlGaN and Al_2O_3 are $\varepsilon_{AlGaN}=9.2\varepsilon_0$ and $\varepsilon_{Al2O3}=7\varepsilon_0$. $Q_{2DEG}=6\times10^{12}\text{cm}^{-2}$ is the 2DEG density at AlGaN/GaN interface when AlGaN thickness is at 10nm. $Q_T=-1.5\times10^{12}\ \text{cm}^{-2}$ is the fixed charge density at Al_2O_3/AlGaN interface [95]. Q_{EQ} is the equivalent amount of charge at the Al_2O_3/AlGaN interface for the identical electrostatic effect by the multiple fluorine charges Q_1~Q_3 at different Al_2O_3 layers t_1~t_3. The extraction of Q_{EQ} was discussed in Section 4.2. Q_1~Q_3 values for the process conditions shown in Table 5.1 are extracted by fitting the measured V_{TH} from the I_D-V_G characterisations with the Sentaurus TCAD simulations [37].

$$V_{TH}=\frac{\phi_b-\Delta E_1-\Delta E_2-\Delta E_3}{q}-\frac{qQ_{2DEG}(t_{AlGaN}-t_{recess})}{\varepsilon_{AlGaN}}-\frac{q(Q_{2DEG}+Q_{EQ}+Q_T)}{\varepsilon_{Al_2O_3}}\sum_{n=1}^{4}t_n \tag{5.1}$$

where

$$Q_{EQ}=Q_1\frac{t_2+t_3+t_4}{t_1+t_2+t_3+t_4}+Q_2\frac{t_3+t_4}{t_1+t_2+t_3+t_4}+Q_3\frac{t_4}{t_1+t_2+t_3+t_4}$$

Table 5.1 Procedures of gate stack fabrication for multi-fluorinated normally-off MIS-HEMTs Die A, Die B, and Die C

Steps	Process	Die A	Die B	Die C
1	ALD-Al_2O_3 (t_1)	6.5 nm		9.3 nm
3	RIE F^- treatment (140s)	50 sccm CHF_3 @ 30W	50 sccm CHF_3 @ 60W	50 sccm CHF_3 @ 90W
4	ALD-Al_2O_3 (t_2)	7.3 nm	10.1 nm	12.8 nm
5	RIE F^- treatment (260s)	50 sccm CHF_3 @ 30W	50 sccm CHF_3 @ 60W	50 sccm CHF_3 @ 90W
6	ALD-Al_2O_3 (t_3)	7.6 nm	10.6 nm	13.5 nm
7	RIE F^- treatment (280s)	50 sccm CHF_3 @ 30W	50 sccm CHF_3 @ 60W	50 sccm CHF_3 @ 90W
8	ALD-Al_2O_3 (t_4)	8 nm		
Total Al_2O_3 thickness after F^- RIE treatment		**18.1 nm**		

5.3 Trapping and de-trapping of the negative charge within the gate region

Fig. 5.2 shows the bi-directional transfer gate swing characteristics (with sweeping time of 0.5V/s) of recess-only and fluorinated dies A, B, and C at V_D=1V. It is observed that the FPT is able to increase the V_{TH} from about −2.2V to 5.4V~7.4V at room temperature, indicating significant amount of negative charge trapping within the gate dielectric. The negative charges generate a depletion field to deplete the 2DEG. The increase in the RF power of the FPT creates greater amount of dissociated fluorine radicals provided to the sample surface and resulted in higher V_{TH}. Highest V_{TH} of 7.4V for Die C is found with RIE power at 90W. Additionally, positive shift in V_{TH} is investigated during the negative sweep of I_D-V_G comparing with the V_{TH} during the positive sweep. It

demonstrates the trapping and de-trapping behaviour of electrons to the trap states at Al_2O_3/AlGaN interface or Al_2O_3 bulk at high V_G during the positive sweep. The amount of de-trapped charge resulted in the change in V_{TH} during the bi-directional voltage swing is expressed as Q_{DETRAP} in Eq. (5.2) [103]. In Eq. (5.2), $\varepsilon_{Al2O3}=7\varepsilon_0$, where ε_0 is the permittivity in vacuum, q is the electronic charge and t_{Al2O3} is the thickness of Al_2O_3 as shown in Table 5.1. The parameters shown in Table 5.2 are the V_{TH}, ΔV_{TH} and Q_{DETRAP} values for Die A~C at 25°C based on Fig. 5.2 measurement data and Eq. (5.2). It is observed that the ΔV_{TH} is smaller with a higher fluorine treatment power, implying that more negative charges are located at deeper levels. Therefore, the charges are not trapped nor de-trapped by the V_G-induced variations in Fermi level during the gate swing at room temperature.

$$Q_{DETRAP} = \frac{\varepsilon_0 \varepsilon_{Al_2O_3} \Delta V_{TH}}{q t_{Al_2O_3}} \tag{5.2}$$

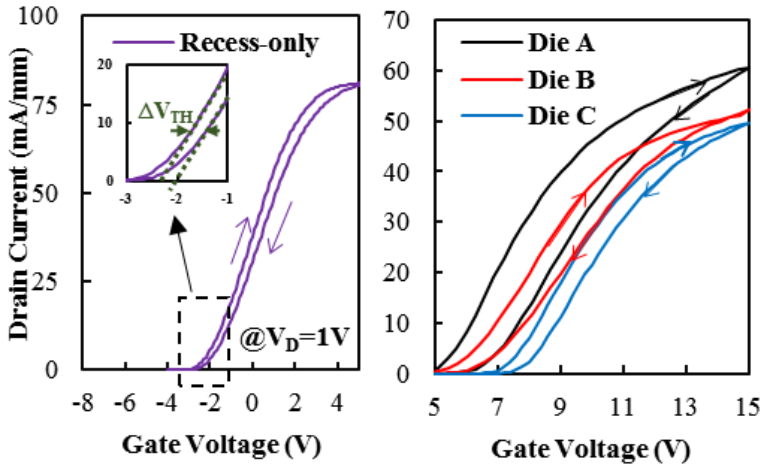


Fig. 5.2 Bi-directional linear I_D-V_G characterisic of recess-only and FPT-processed dies A~C at 25°C. The I_D-V_G sweep was done in 20s. ΔV_{TH} is demonstrated in the inset for the recess-only device.

Table 5.2 Extracted ΔV_{TH} and Q_{DETRAP} on devices of recess-only and FPT-processed dies A~C at 25 °C. V_{TH} is obtained by extrapolating the linear region of the positively-swept I_D-V_G curves.

Devices	Recess-only	Die A	Die B	Die C
V_{TH} in positive sweep (V)	−2.2	5.4	6.05	7.4
Q_{EQ} (10^{13} cm^{-2})	0	1.67	1.81	2.07
ΔV_{TH} (V)	0.4	1.5	1	0.8
Q_{DETRAP} (10^{12} cm^{-2})	1.07	4.01	2.67	2.13

Fig. 5.3 gives the schematic energy diagrams to illustrate the trapping and de-trapping mechanisms of charged carriers which resulted in ΔV_{TH} during the I_D-V_G bi-directional swing [104]. When V_G=0V (Fig. 5.3(a)), the fermi level (E_F) is pinned below the conduction band (E_C) of GaN due to the 2DEG depletion effect by the FPT-induced trapped negative charges. When $V_G=V_1>V_{TH}$ in positive sweep of I_D-V_G shown in Fig. 5.3(b), electrons from 2DEG at the AlGaN/GaN interface are attracted by the positive gate bias and move towards the gate metal. They will finally be trapped at empty states at the Al_2O_3/AlGaN interface or Al_2O_3 bulk through field emission (FE) or trap-assisted tunnelling (TAT) effects [105]. When V_G reaches maximum (shown in Fig. 5.3 (c)) and most of the empty states are being filled by electrons, those trapped electrons are slowly de-trapped back into 2DEG during negative sweep. The remained trapped electrons provide an additional depletion field to the 2DEG that causes positive V_{TH} shift comparing with the V_{TH} during the positive shift, as shown in Fig. 5.3 (d). Thus, higher amount of trapped charge results in larger V_{TH} and ΔV_{TH} is observed during the negative sweep.

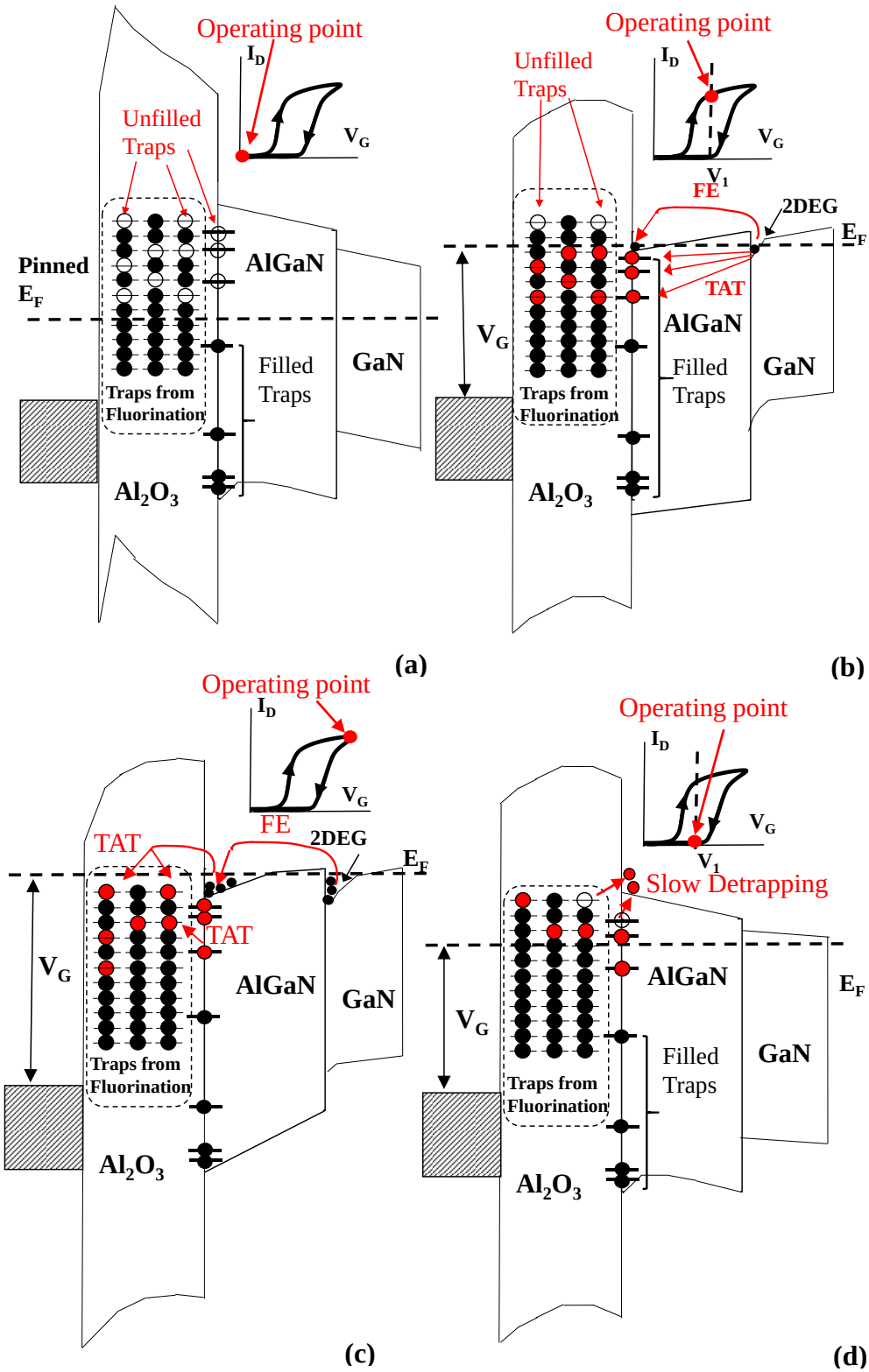


Fig. 5.3 Schematic energy band diagram of Al_2O_3/AlGaN/GaN interface at **(a)** V_G=0V in positive sweep **(b)** V_G=V_1 in positive sweep (the empty trap states start being filled due to field emission (FE) and trap-assisted tunneling (TAT) **(c)** V_G at maximum V_G and **(d)** V_G=V_1 in nagative sweep (more electrons remained in the gate dielectric and Al_2O_3/AlGaN interface since the trap emission is slower than the sweep time. Positive shift in V_{TH} is observed due to enhanced 2DEG depletion)

5.4 The effect and mechanism on V_{TH} thermal degradation of the fluorinated MIS-HEMTs

The amount of electrons trapped at FTP-induced trap states varies with temperature and thus changes the V_{TH} of the device. Fig. 5.4 summarises the variation in V_{TH} of the recess-only device and FPT-processed Dies A~C from 25°C to 200°C. Unlike the relatively stable V_{TH} for the recess-only device, a noticeable decrease in V_{TH} is found for all Dies A to C. It proves that the emission of electrons within the gate is mainly from the FPT-induced traps within Al_2O_3. Therefore, it can be expressed as solely the reduction in Q_{EQ} in Eq. (5.1). For both Dies A and B, the V_{TH} is reduced to about −1.9V at 200°C, which is closer to the V_{TH} of recess-only device. Therefore, most of the FPT-induced negative charges for Die A and B have been emitted from the trap sites and lost the control of V_{TH} under high temperatures. While for Die C at 200°C, V_{TH} remained at 2V, showing good retainment of Q_{EQ} at high temperature.

The deepest emission level of the FPT-induced negative charges corresponding to different temperatures can be modelled by Eq. (5.3) [106, 107]. In Eq. (5.3), E_{T_MAX} is the deepest energy level (referenced to the conduction band edge) of the trapped charges emitted from the trap sites, k_b is the Boltzmann's constant, T is the device temperature, $\gamma_n=(\nu_{th}/T^{0.5})(N_c/T^{1.5})=3.25\times10^{21}(m_n/m_0)$, where m_n/m_0 is the relative electron effective mass within Al_2O_3, which is 0.16 [108], ν_{th} is the thermal velocity of

Al_2O_3, obtainable from $v_{th}=(3k_bT/(m_nm_0))^{0.5}$ [109], N_C is the effective density of states in Al_2O_3, obtainable from $N_C=2(2\pi m_n m_0 k_b T/h^2)^{1.5}$ [109] and h is the Planck's constant. $\sigma_{Al2O3}=10^{-16}cm^2$ is the capture cross-section of the electrons in Al_2O_3 [110], and t=50s is the device heating time. The time is sufficient for stable device surface temperature and reaching quasi-steady state [111, 112]. The E_{T_MAX} is relatively insensitive to changes in the characterised time range. Therefore, the E_{T_MAX} at different temperatures are calculated and plotted in the schematic energy band diagram of Al_2O_3 in Fig. 5.5. It is reasonable to assume that all of the charges trapped shallower than E_{T_MAX} is emitted due to the exerted thermal energy. All trapped charges deeper than E_{T_MAX} at a certain temperature T is not emitted from the level.

$$E_{T\_MAX} = k_bT\ln(\gamma_n\sigma_{Al2O3}T^2t) \tag{5.3}$$

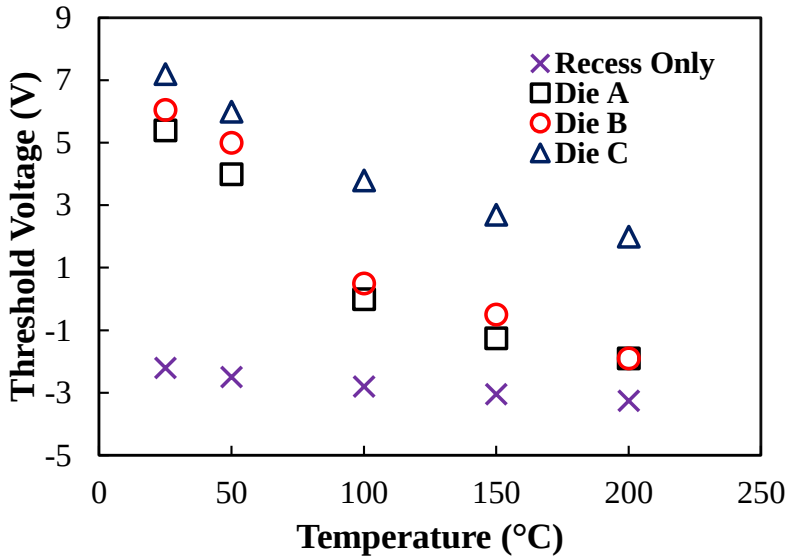


Fig. 5.4 The V_{TH} obtained from the I_D-V_G transfer characteristics for FPT-processed dies A~C and the unprocessed recess only device at temperatures from 25 °C to 200 °C.

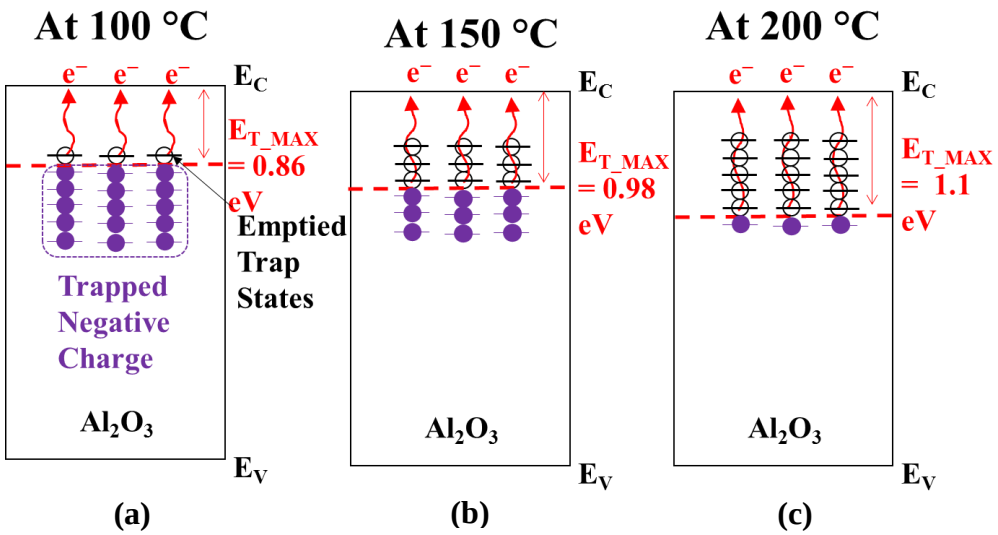


Fig. 5.5 The schematic energy band diagram and depicted trap emission mechanism of the FPT-processed Al_2O_3 with the maximum trap emission levels (E_{T_MAX}) demonstrated at **(a)** 100 °C **(b)** 150 °C and **(c)** 200 °C.

The variation in Q_{DETRAP} of the four devices with temperatures according to the bi-directional I_D-V_G measurements and Eq. (5.2) is summarised in Fig. 5.6. A significant increase in Q_{DETRAP} is found for the FPT-treated devices at higher temperatures, implying more negative charges are de-trapped faster than the I_D-V_G negative sweeping time (the sweep speed was 0.5s/V, thus the total negative sweep time was 7.5s). While for the recess-only device, the Q_{DETRAP} is much more stable at high temperature. It is also noteworthy that the amount of Q_{DETRAP} is less in Die C than in Die A and B at higher temperatures, implying less amount of the trapped charge is emitted from the sample with higher RIE plasma power. Therefore, it is possible to use the extracted Q_{DETRAP} to map the trap state distribution within the Al_2O_3 energy band with the assistance of Eq. (5.3). However, the bi-directional I_D-V_G characterisation is not capable of extracting the charges at deep-level FPT-induced trap states in Al_2O_3 accurately. These

deep-level traps are dominating the high temperature stability of the device as their emission time is much longer than the I_D-V_G sweep time. Furthermore, the excess carriers attracted from the 2DEG region during the positive V_G sweep may overestimate the actual amount of trapped charge within Al_2O_3. Therefore, in Section 5.5, the gate-stressing characterisations are carried out to provide a better estimation on the distribution of the traps within the Al_2O_3 energy band.

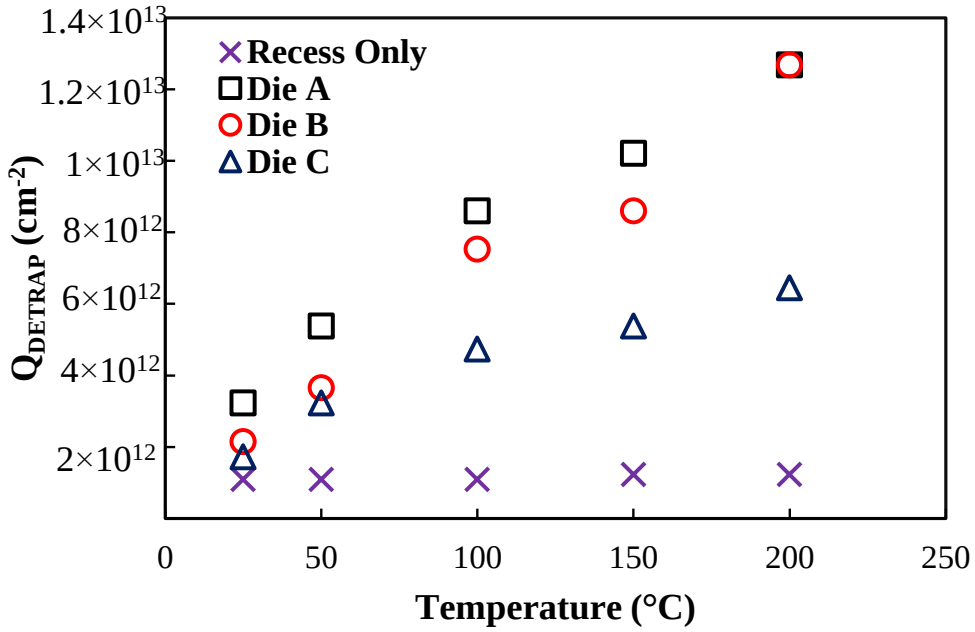


Fig. 5.6 The change in the Q_{DETRAP} obtained from bi-directional I_D-V_G characteristics for FPT-processed Die A~C comparing with unprocessed recess-only device at temperatures from 25°C to 200°C.

5.5 Deep trap state characterisation by the gate-stressing technique

In order to better estimate the deep trap states and densities (D_{EQ}) induced by FPT, the gate-stressing characterisation was carried out by stressing the gate at different levels of negative bias voltage. Based on the Poole-Frenkel trap

emission theory [113-116] leading to Eq. (5.4), the negative gate bias is able to provide an electric field (ξ) that enhances the emmission of FPT-induced negative charges trapped within Al_2O_3. A larger reduction of V_{TH} is observed with increasing gate base voltage (V_B) due to the stronger emission field. Specifically, pulsed I_D-V_G measurement with V_B from 0V to –40V held for 50s at 25°C was performed. In order to minimise the charge injection during positive V_G sweep which introduces error to the characterisation, the positive gate voltage is provided in terms of short pulses. After the initial 50s of V_B stressing to emit the trapped negative charges, the pulsed positive gate sweep initiates and returned to the same V_B between pulses. The time for V_B in between two pulses is 18ms and the time for pulsed positive V_G is 2ms to ensure the charge injection introduced by the positive V_G is emitted in each cycle. According to the change in V_{TH} for Die C at different pulse seapration times shown in Table 5.3, most of the carriers have already been emitted when pulse separation time is 18ms. Detailed time sequence of these V_G pulses is shown in the inset of Fig. 5.7(a). The sampled drain current (I_D) waveform from the characterisation is shown in Fig. 5.7(a). In Eq. (5.4), $Q_{EQ,0}$ and $Q_{EQ,VB}$ are the effective FPT-induced trapped negative charges before and after the gate stress V_B is applied. The $Q_{EQ,0}$ and $Q_{EQ,VB}$ can be derived by the change in characterised V_{TH} by Eq. (5.1).

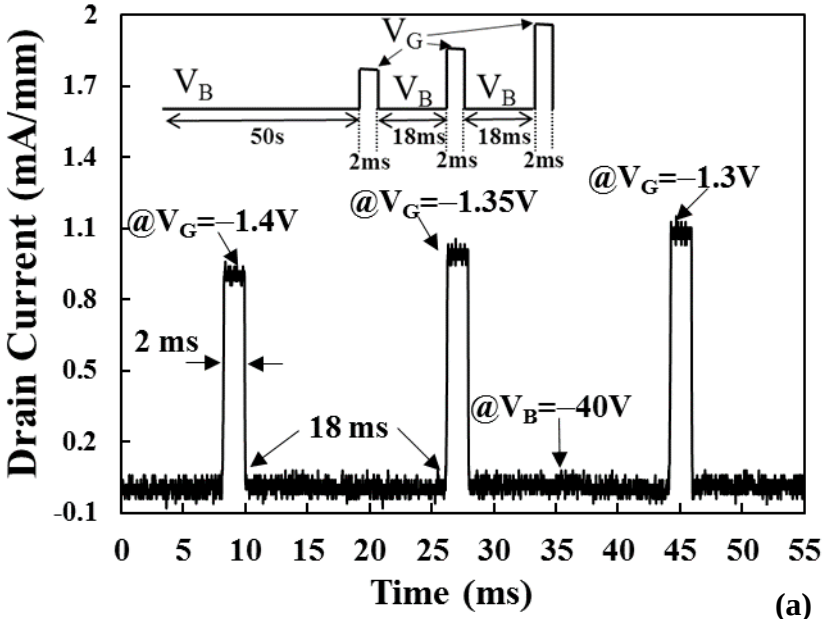
$$E_{T\_MAX} = \sqrt{\frac{q\xi}{\pi\varepsilon_{Al2O3}\varepsilon_0}} - \frac{kT}{q}\ln\left(1 - \frac{Q_{EQ,0}}{Q_{EQ,VB}}\right) \tag{5.4}$$

Where $$\xi = (\frac{V_G}{t_{Al2O3}} - \frac{\phi_b}{qt_{Al2O3}})$$

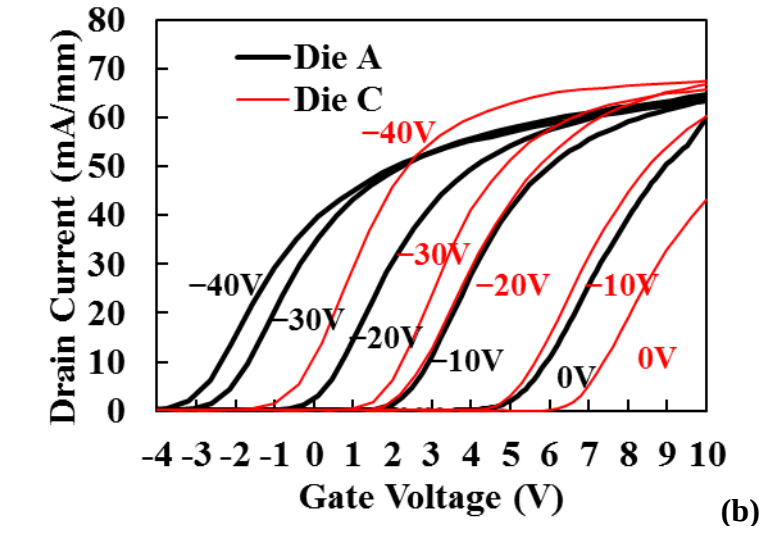
Table 5.3 The V_{TH} of Die C with different pulse separation time and V_B.

Pulse separation time	**V_{TH} when V_B=−20V**	**V_{TH} when V_B=−40V**
18ms	2.50V	−0.60V
48ms	2.50V	−0.65V
98ms	2.45V	−0.65V

The I_D-V_G characteristic of the Dies A and C are measured with gate stress voltage of V_B= 0V, –10, –20, –30 and –40V, as shown in Fig. 5.7(b). The V_{TH} decrease in Die C compared to Die A at V_B= –10V is less, implying Die C has less shallow trap states than that of Die A. Additionally, greater reduction in V_{TH} from when V_B= –40V to V_B= –30V of Die C than that of Die A indicates greater amount of deeper traps in Die C. The gate dielectric quality throughout the gate stress characterisation is verified by the off-state gate leakage current obtained before and after the gate stressing test, as shown in Fig. 5.7(c).



(a)



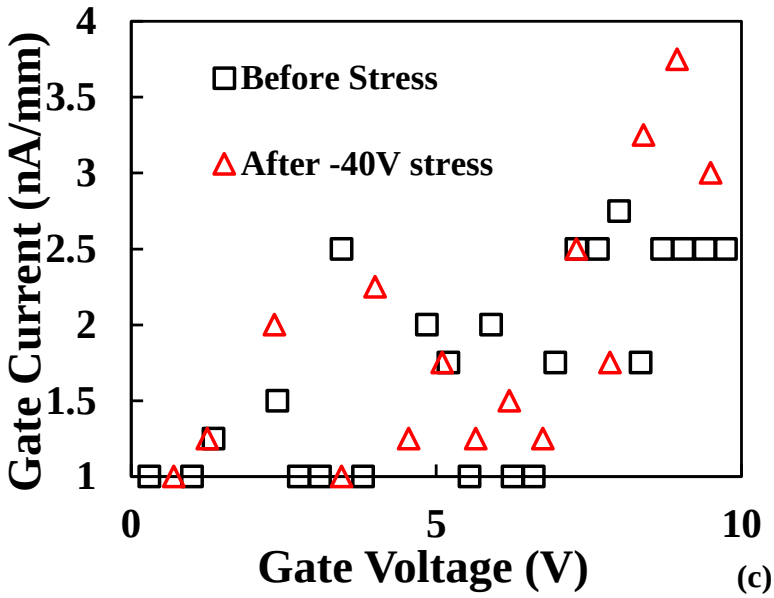


Fig. 5.7 (a) Drain current waveform during the I_D-V_G pulse when V_G is near the V_{TH} at V_B=−40V and V_D=1V. The inset shows the schematic V_G waveform, where the V_B is held initially for 50s followed by the pulsed signal with a period of 20ms (2ms pulse V_G and 18 ms bias V_B) during each sweep. **(b)** Pulsed I_D-V_G characterisation of Die A and C with V_B from 0V to −40V. **(c)** The I_G-V_G leakage currents before and after the gate stress measurement of −40V for 50s; Similar I_G leakage implies no damage to the gate dielectric after the stressing test.

Specifically, by using Eq. (5.3) and (5.4), the E_{T_MAX} from the conduction band (E_C) edge corresponding to the stressed V_B at 25°C and elevated device temperature without stressed gate bias are plotted in Fig. 5.8. It demonstrates

that V_B at 25°C is able to characterise the same E_{T_MAX} for high temperature effects with appropriate choice of V_B. For instance, both T=150°C and V_B=–15V correspond to E_{T_MAX}=0.98eV. In other words, all of the traps located shallower than 0.98eV from the E_C are emitted when the gate is unstressed at 150°C or stressed at –15V under room temperature.

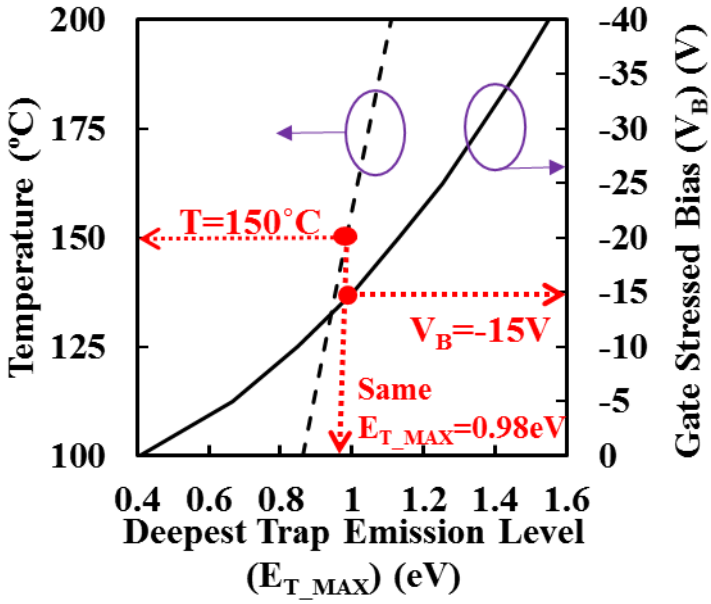


Fig. 5.8 The corresponding E_{T_MAX} from the conduction band edge within the Al_2O_3 gate dielectric stack at different stressed base voltage (V_B) and temperatures.

With proper selection on V_B, the FPT-induced trap state distribution can be quantified within the Al_2O_3 energy band. Therefore, the gate stress measurement is able to characterise the distribution of trap states over a wide range of trap energy levels. Accordingly, by using the V_{TH} model shown in Eq. (5.1), the amount of trapped charge emitted (ΔQ_{EQ}) from the energy levels shallower than E_{T_MAX} at high temperature can be extracted with the observed V_{TH} reduction and being referred to a certain value of V_B.

In Fig. 5.9, V_B ranging from −40V to 0V with 5V increments is applied to derive the trap state density (D_{EQ}) mapping for dies A, B, and C from 0.4eV to 1.5eV away from the conduction band energy (E_C) of Al_2O_3. The E_{T_MAX} at different temperatures is also indicated. Die A has the most D_{EQ} at shallow energy levels as it loses most of the D_{EQ} at high temperature. It implies the worse V_{TH} thermal stability if the gate was processed with low FPT power. While for Die C, higher D_{EQ} at deeper energy levels is observed. Especially, a lot of traps are located deeper than the trap emission energy of E_T=1.1eV (i.e. the E_{T_MAX} when T=200ºC). Therefore, more trapped charges in Die C remains in the dielectric at 200ºC. It clearly illustrates the capability of Die C maintaining its V_{TH} at 2V under high temperature. For further verification of the gate-stressing method, ΔQ_{EQ} can also be extracted by integrating the the best-fitted sixth-order polynomial function of the D_{EQ} measured points. The comparison of ΔQ_{EQ} obtained from the high-temperature ($\Delta Q_{EQ,\ HighT}$) and the D_{EQ} mapping in Fig. 5.9 ($\Delta Q_{EQ,Fig.5.9}$) for Dies A~C is summarised in Table 5.4. They agree with each other quite well with generally less than 15% mismatch, whereas such error can be due to the introduction of excess carriers into the Al_2O_3 trap states during the positive I_D-V_G swing. The mapping of FPT-induced trapped charge distribution within Al_2O_3 energy band provides valuable information and enables the prediction of the V_{TH} degradation at higher temperature.

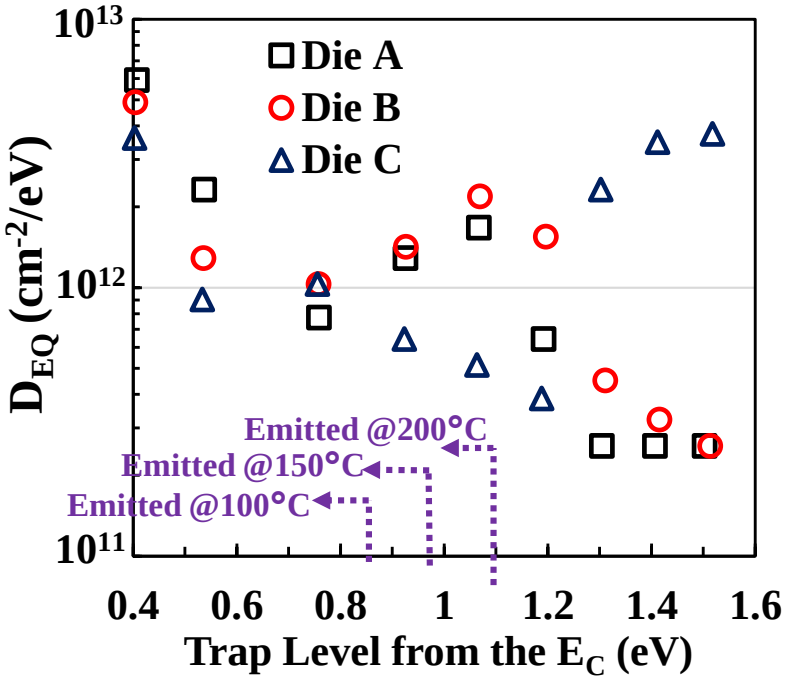


Fig. 5.9 The distribution of D_{EQ} within the Al_2O_3 energy band for Dies A, B, and C. It is quantified from the negative gate stress characterisation.

Table 5.4 The amount of V_{TH} reduction (V_{TH}−$V_{TH,25°C}$ in V) and Q_{EQ} reduction (ΔQ_{EQ}, in 10^{12} cm^{-2}) obtained from either the high temperature characterisation ($\Delta Q_{EQ,\ HighT}$, in 10^{12} cm^{-2})) or the integration of the D_{EQ} ($\Delta Q_{EQ,Fig.5.9}$, in 10^{12} cm^{-2}) for Dies A~C.

Temperature	100 ºC			150 ºC			200 ºC		
E_{T_MAX}	0.86 eV			0.98 eV			1.1 eV		
Dies	A	B	C	A	B	C	A	B	C
V_{TH}−$V_{TH,25°C}$	−5.2	−5.5	−3.7	−6.5	−6.5	−4.8	−7.2	−7.9	−5.5
$\Delta Q_{EQ,\ HighT}$	−9.6	−10	−6.8	−11.9	−11.9	−8.9	−13.1	−14.6	−10
$\Delta Q_{EQ,\ Fig.5.9}$	−9.9	−9.1	−7.8	−11.1	−10.8	−8.4	−12.9	−13.1	−9.0
% mismatch between $\Delta Q_{EQ,\ HighT}$ and $\Delta Q_{EQ,\ Fig.5.9}$	−3.1%	9%	−14.7%	6.7%	9.2%	5.6%	1.5%	10.3%	10%

5.6 Conclusion

In this chapter, the distributions of the FPT-induced traps for the multiple fluorinated Al_2O_3/AlGaN/GaN MIS-HEMTs were studied through the gate stressing technique combined with the analytical V_{TH} model and the Poole-Frenkel trap emission model. With this methodology, the distribution of the trapped negative charges within Al_2O_3 trap states can be found accurately. In addition, the capability of retaining the trapped charges at higher temperature can then be extracted. From the study carried out in Chapter 5.5, it revealed that at 200°C, greater amount of FPT-induced trap states located deeper than 1.1 eV allow more trapped negative charges to remain in the dielectric and maintain the V_{TH} at higher value under high temperature. For which, the Die C fabricated with a higher RF power on the gate dielectric during FPT can yield higher trap state density at levels deeper than 1.1eV. Therefore, higher V_{TH} of 2V at 200°C can be obtained.

CHAPTER 6 Characterisation of Al_2O_3/AlGaN/GaN MIS-HEMTs with Argon Pre-Fluorination Treatment for V_{TH} Thermal Stability Improvements

6.1 Introduction

Fluorine Plasma Treatment (FPT) is a promising gate processing method applied to GaN-based HEMTs to achieve normally-off operations with positive threshold voltage (V_{TH}). High V_{TH} is desired in power electronics applications to ensure the system safety and low standby power loss. However, the reported devices with FPT on AlGaN obtains low V_{TH} of around 0.6V at 25°C and 0.1V at 200°C [117]. Applying multiple traditional RIE-FPTs on Al_2O_3 gate dielectric along with partial gate recess utilised in Chapter 4, 5 and [37, 91] introduced a large concentration of trapped negative charges within the gate dielectric which achieved large V_{TH} of 6.5V. Meanwhile, a satisfactory I_{DMAX} of 350mA/mm [37] indicates the preservation of 2DEG channel quality after the multiple FPT on Al_2O_3. However, as observed in Chapter 5, the multiple low-power FPT process is complicated in fabrication process and is unable to generate sufficient deep-level trap states to retain the electrons at the trapped states under high temperature. In this chapter, the multiple RIE FPTs on Al_2O_3 were replaced by single ICP-RIE FPT to reduce the fabrication complexity for the first time. It is able to introduce significant flux of negative charges at low bombardment energy. Therefore, a high V_{TH} can be obtained while preserving the 2DEG

channel quality at the same time. In addition, a novel short Argon (Ar) plasma treatment (APT) was applied prior to FPT to effectively enhance the fluorine-plasma induced states to deeper energy levels within the Al_2O_3 dielectrics. Hence, the negative charges trapped at these deep trap states can be maintained within the dielectric at high temperatures. The study in this chapter proposed a simple and effective approach to achieve high-V_{TH} for AlGaN/GaN power HEMTs suitable for high temperature operation, which is useful in electric vehicle power systems.

6.2 Design and fabrication of normally-off HEMTs with argon pre-fluorination technology

The mechanism of Al_2O_3 gate dielectric fluorination on the V_{TH} shift can be explained by the conduction band energy diagram along the gate stack region without any external stress. It was simulated by the Sentaurus TCAD simulation tool [34, 35] and shown in Fig. 6.1. The barrier between Ni and Al_2O_3 is ϕ_b=3.5eV [93], and E_1 and E_3 are the conduction band offset between Al_2O_3/AlGaN and AlGaN/GaN respectively, which add to 2.1eV [94]. E_2 is the conduction band offset from the Fermi level before fluorine treatments, which is –0.16eV [14]. When there is no FPT applied to the Al_2O_3 gate dielectrics, the conduction band at the AlGaN/GaN interface is below the Fermi level (E_F) and the 2DEG is induced. Therefore, the V_{TH} of the fabricated device becomes negative due to the intrinsic existence of the 2DEG. If the Al_2O_3 gate dielectric

is fluorinated, significant amount of negative charge will be trapped in the Al_2O_3 and shift the conduction band at the AlGaN/GaN interface above the E_F. Hence, the electrons in 2DEG at the gate region are depleted by these negative charges and the device has its V_{TH} greater than zero. It is notable that if the negative charges are trapped at energy levels above the E_F, it will be emitted within a period of time. The emission time constant is related to the trap energy level of where the charge is trapped, which will be further discussed in Section 6.4.

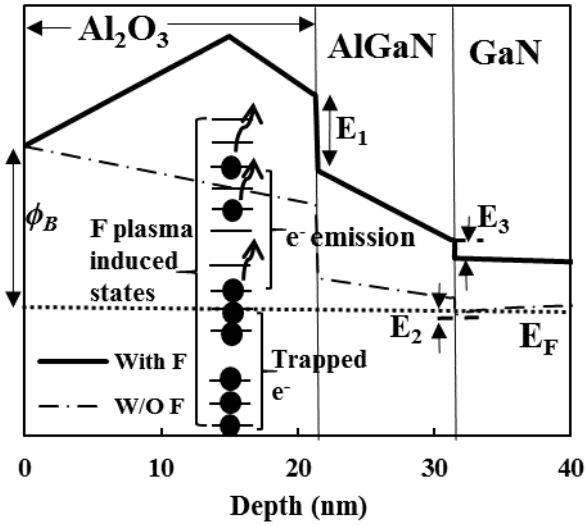


Fig. 6.1 The conduction band energy (E_C) schematic diagram along the gate stack region for the devices with (solid line) and without (dashed line) FPT at V_G=0V.

According to Chapter 5, better V_{TH} thermal stability was obtained when the RF power of the fluorine plasma treatment is higher. It was also reported in Section 2.2 that the RF plasma power controls the amount of fluorine radicals dissociated from CHF_3 as well as the surface bombardment energy of the dissociated ions. As summarised in Chapter 5, the significant improvement on the V_{TH} thermal stability of ΔV_{TH}=8V to 5.4V from 25°C to 200°C when the

RF power is increased from 30W to 90W implies the change in the energy level of the traps. In other words, more trap states will be formed at deeper energy levels within the gate dielectric bandgap when higher concentration of fluorine radicals is introduced. However, increasing the RF power in the RIE system will damage the surface or even the channel quality and will degrade the on-state device performances. As the fluorine radicals are neutral in the plasma and do not accelerate with RF power, the exacerbated surface damage with higher RF power may be attributed to the ions dissociated from the gas.

Based on these observations, the RIE was replaced with ICP-RIE to carry out FPTs in this chapter. Unlike conventional RIE system, the ICP-RIE is able to control the amount of dissociated fluorine radicals and the ion bombardment energy separately through independent adjustments on the coil and cathode power. In order to further enhance the fluorine incorporation during FPT, an innovative short APT is introduced to the gate dielectric surface right before the FPT. Therefore, shallow surface damage with broken Al-O bonds can be intentionally introduced to allow for increased amount of Al-F bonds. Detailed physical mechanism of the APT on V_{TH} thermal stability improvement will be demonstrated in Chapter 7.

The fabrication process flow and the cross-sectional schematic of the fluorinated device are shown in Fig. 6.2 and 6.3 respectively. Except for the gate region, the device uses the same wafer as the ones reported in Chapter 4 and 5.

The L_G, L_{GS}, L_{FP}, and L_{GD} are 3µm, 5µm, 1.5µm, and 5µm respectively. The AlGaN/GaN-on-Si wafer has the 2DEG carrier density and mobility of 8.5×10^{12} cm^{-2} and 1450 cm^2/Vs respectively. The fabrication of the device began with mesa isolation by BCl_3-based ICP-RIE and SiO_2 dielectric deposition by PECVD. Ti/Al/Ni/Au (25/125/45/55 nm) source/drain ohmic contacts were formed by RTA at 850°C for 30s. About 10nm (50%) of AlGaN was recessed at the gate region by low power BCl_3-based ICP-RIE to reduce the 2DEG concentration to $Q_{2DEG}=6\times10^{12}cm^{-2}$ without damaging the AlGaN/GaN interface, and to preserve carrier mobility in the 2DEG channel [37]. After 6.5nm of ALD-Al_2O_3 dielectric layer deposition at 250°C, Dies C~E underwent 20s ICP-Ar plasma treatment with a fixed coil power of 100W. The APT recipe implemented was based on the existing Al_2O_3 etching recipe using $BCl_3/Cl_2/Ar$ ICP-RIE (included in Appendix II). It uses the same coil power and Ar gas flow as the Al_2O_3 etching recipe to ensure the amount of dissociated Ar^+ is sufficient. Minor adjustment on the cathode power from the etching recipe was implemented to seek for optimised results. The design of the FPT recipe follows the principle of maximising the amount of fluorine radicals (i.e. high CP) while minimising the ion bombardment energy (i.e. low CEP). Therefore, ICP-CHF_3 plasma treatment was tested with fixed cathode power of 10W and varied CEP for 4 minutes, which will be discussed in Fig 6.5(a). After the tests, the CEP of FPT was determined to be 200W. The process parameters used for the gate formation and the resulting surface roughness RMS obtained from the Atomic

Force Microscopy (AFM) are listed in Table 6.1 and Fig. 6.4. The Al_2O_3 surface of Die A (without any plasma surface treatment) has a smooth surface with surface RMS of 0.38nm, as shown in Fig. 6.4 (a). According to the small 0.53nm surface roughness for Die B (FPT-only) shown in Fig. 6.4 (b), the designed FPT recipe does not have a significant impact on the surface roughness. It shows the effectiveness of damage control by minimising the CEP of the FPT recipe. If APT is introduced prior to FPT, the surface roughness RMS will be further increased. However, controlling the cathode power of the argon treatment below 75W (Die D shown in Fig. 6.4 (c)) is able to preserve the surface roughness RMS within 0.78nm. If the cathode power of the Ar treatment is increased to 100W (Die E), the surface roughness RMS will significantly increase from 0.78 nm to 2.29 nm, indicating damage to the Al_2O_3 surface. Finally, Ni/Au (15/150 nm) gate-metal deposition followed by annealing at 400°C for 5 minutes were applied.

Table 6.1 Processing parameters for the gate dielectric of Dies A~E

Steps	**Die A**	**Die B**	**Die C**	**Die D**	**Die E**
ALD-Al_2O_3 (t_1)	6.5 nm				
CEP for APT	N/A	N/A	50W	75W	100W
ICP FPT (CEP/CP)	N/A	10W/200W			
ALD-Al_2O_3 (t_2)	15 nm				
AFM surface RMS Roughness	0.38 nm	0.53 nm	0.61 nm	0.78 nm	2.29 nm

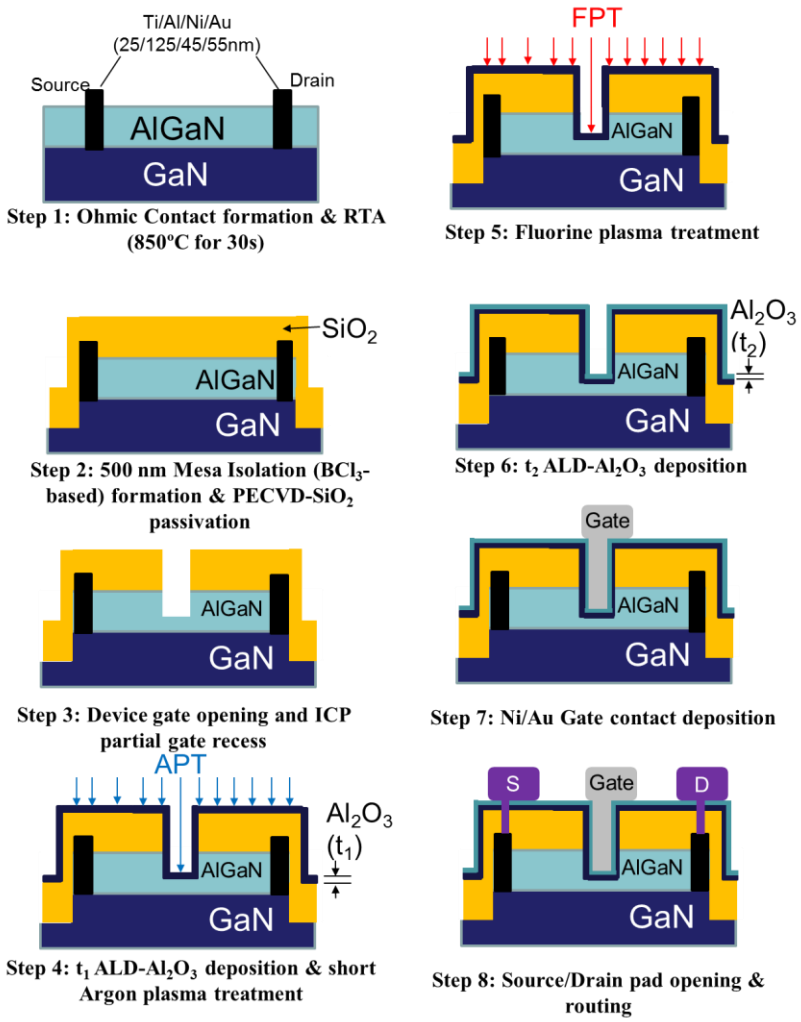


Fig. 6.2 The fabrication process flow of the normally-off Al_2O_3/AlGaN/GaN MIS-HEMT with APT-then-FPT gate process

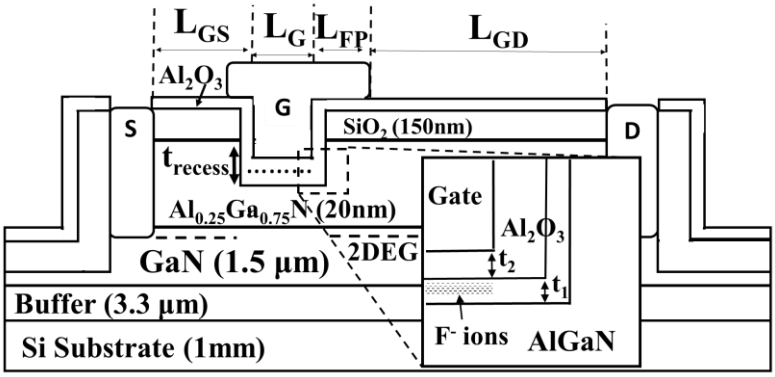


Fig. 6.3 The device cross-sectional schematics of the normally-off AlGaN/GaN MIS-HEMT with ICP-fluorinated Al_2O_3. The inset magnifies the gate region, where the fluorine-induced negatively charged ions (F^-) and the thickness of Al_2O_3 gate dielectric stack (t_1 and t_2) are shown.

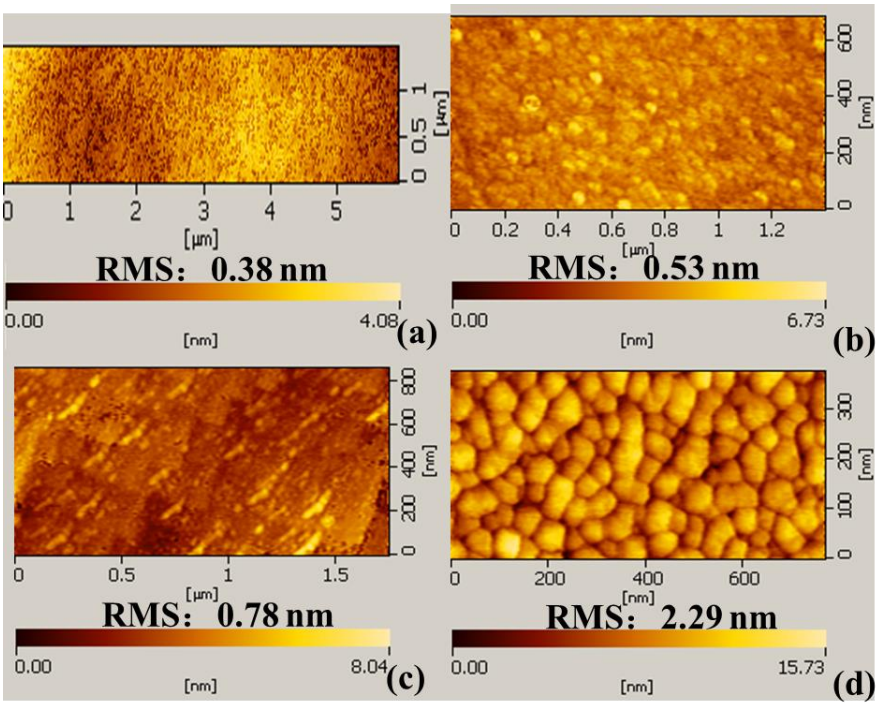


Fig. 6.4 The Atomic Force Microscopy (AFM) image of the Al_2O_3 surface right before t_2 deposition for **(a)** Die A **(b)** Die B **(c)** Die D and **(d)** Die E with the surface roughness RMS indicated.

6.3 Current-voltage characteristics at room temperature

In this section, the current-voltage characteristics of dies A~E designed in Section 6.2 are measured and compared. Fig. 6.5 (a) compares the I_D-V_G characteristics of the recess-only and FPT-only devices with varied coil power (CP, which controls the flux of particles within plasma) and fixed cathode electrode power (CEP, which controls the particle bombardment energy) of 10W on the CHF_3-based FPT. This test is applied to seek for optimum gas dissociation power to obtain maximum amount of negative charge incorporation into the sample and to minimise the damage to the surface at the same time. It is found that ICP-FPT is able to shift the V_{TH} from –0.95V to as much as 4.2V

(Die B with CP=200W). It is the highest reported V_{TH} with single FPT treatment. Replacing the conventional RIE with ICP-RIE process, the capability of introducing much more negative charges into Al_2O_3 gate dielectric yields higher V_{TH}. It is observed that 300W of CEP for FPT does not improve the V_{TH} but reduce the on-state conductivity, which implies the increase in the amount of positive ions dissociated from the CHF_3 gas (explained in Section 2.2) but unchanged concentration of the F radicals in the plasma when CEP is higher than 200W.

When applying argon plasma treatment (APT) prior to the FPT, which are noted as dies C, D, and E in Fig. 6.5 (b), slight variation in the V_{TH} was obtained with appropriate control of the CEP of the APT. 4.4V of V_{TH} is obtained for Die D with the Ar CEP at 75W, while increasing the Ar CEP to 100W (Die E) is able to further increase the V_{TH} to 5V due to greater amount of vacancies within Al_2O_3 for fluorine radicals to combine with after Ar bombardment. The preservation of gate leakage for Die C and D compared with Die B indicated in Fig. 6.5 (c) has ensured the Al_2O_3 gate dielectric quality after the APT with appropriate CEP. In Fig. 6.5 (d), a good I_{DMAX} of about 320mA/mm is found for Dies B~D, proving the preservation of 2DEG channel quality after Ar bombardment and FPT. Yet if the Ar cathode power is too high (Die E), it will roughen the treated surface, damage the channel, and worsen the I_{DMAX} or the gate leakage current. The obvious degradation in the mobility for Die E extracted from the simulation fitting with the I_D-V_D characteristics is observed

in Table 6.2. It is another evidence of the degradation in 2DEG with excessive CEP during APT.

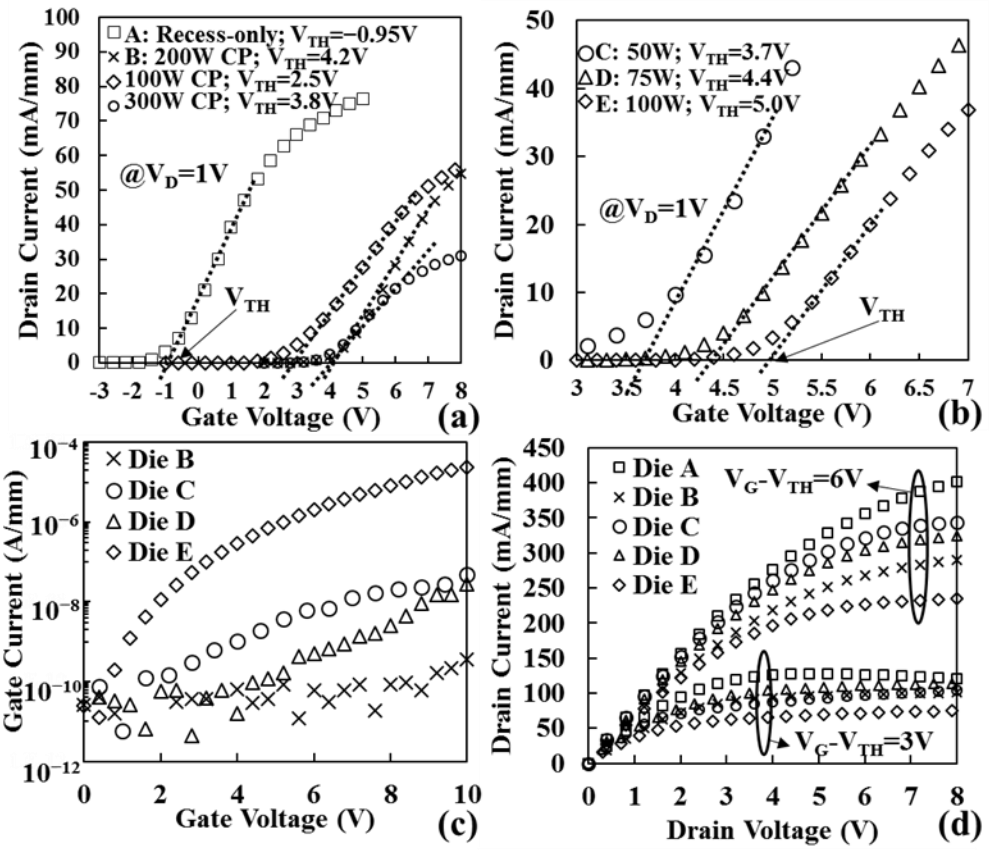


Fig. 6.5 I_D-V_G of **(a)** Dies A & B comparing with devices with different ICP-fluorination coil power (CP) of 100W and 300W and **(b)** Dies C~E with different Ar ICP pre-treatment cathode powers (CEP) at V_D of 1V. **(c)** I_G-V_G of Dies B~E at V_D=1V. **(d)** I_D-V_D performance of Dies A~E with V_G-V_{TH}=3V or 6V.

Table 6.2 The 2DEG carrier mobility for Dies A~E obtained by simulations in Fig. 6.5 (d)

Dies	**A**	**B**	**C**	**D**	**E**
Mobility obtained from simulation ($cm^2/V·s$)	1200	900	1050	1000	750
CEP for APT (W)	N/A	N/A	50W	75W	100W

According to Fig. 6.6 (a), proper APT also reduces the ratio between the dynamic on-state resistance and static on-state resistance ($R_{Dynamic}/R_{ON}$). R_{ON} was extracted from the linear region of the I_D-V_D characteristic with no stress applied before the measurement. $R_{Dynamic}$ was measured from the linear region of the I_D-V_D characteristic right after a drain bias was applied for 10 seconds at V_G=0V. In addition, the breakdown voltage, which was measured at V_G=–5V for un-treated Die A and V_G=0V for plasma-treated Dies B~E shown in Fig. 6.6 (b), is also improved with proper design of APT. These improvements imply effective passivation of the shallow trap states after the APT. For instance, Die D is able to have about 7% smaller $R_{Dynamic}/R_{on}$ (1.37 versus 1.27) and 40% higher breakdown voltage (940V versus 670V) than for FPT-only Die B without sacrificing the on-state conductivity. However, if the CEP for APT is too high (Die E), the off-state leakage will be significantly increased by about one order of magnitude and the breakdown voltage will be decreased to 800V. Therefore, reasonably optimised CEP for the APT process is necessary to ensure good performance of the device. Significant reduction in $R_{Dynamic}/R_{on}$ is observed when comparing with the $R_{Dynamic}/R_{on}$=1.61 for the multi-fluorinated Al_2O_3 stack based on conventional RIE technique reported in Section 4.2. It proves the significant reduction in the shallow trap concentrations with ICP-RIE treatment.

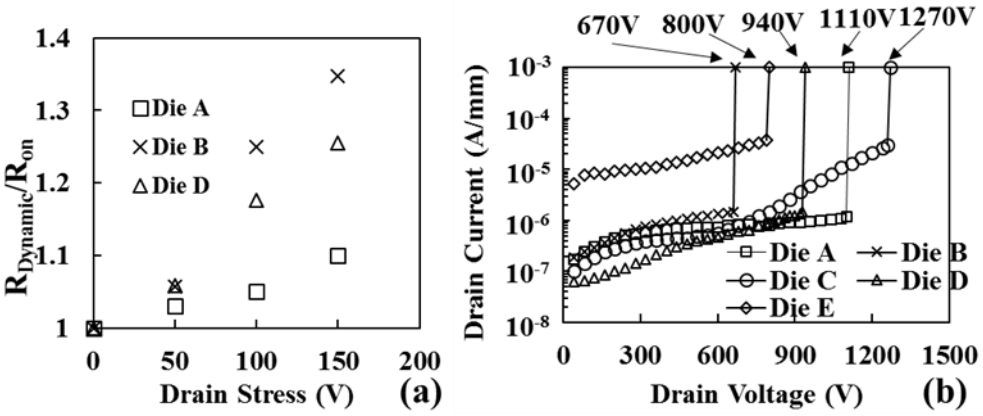


Fig. 6.6 (a) The ratio between the dynamic on-resistance ($R_{Dynamic}$) and the static on-resistance (R_{on}) of Dies A, B and D after drain bias applied for 10 seconds during off-state. **(b)** Off-state I_D-V_D performance of Dies B~E at V_G=0V and Die A at V_G=−5V.

6.4 V_{TH} thermal stability and deep trap characterisation

The effect of APT on the transfer characteristics of the device at high temperature can be illustrated in the logarithmic I_D-V_G curves of Die B (FPT-only) and Die D (APT+FPT) shown in Fig. 6.7. A significant improvement on the turn-on voltage is observed for Die D at 200°C. Detailed discussions on the change in V_{TH} at various temperatures will be conducted in Fig. 6.9. The drain leakage current of Die D is similar to the leakage of Die B at both 25°C (about 10nA/mm) and 200°C (about 1μA/mm), showing the preservation of the drain off-state leakage current after the APT process.

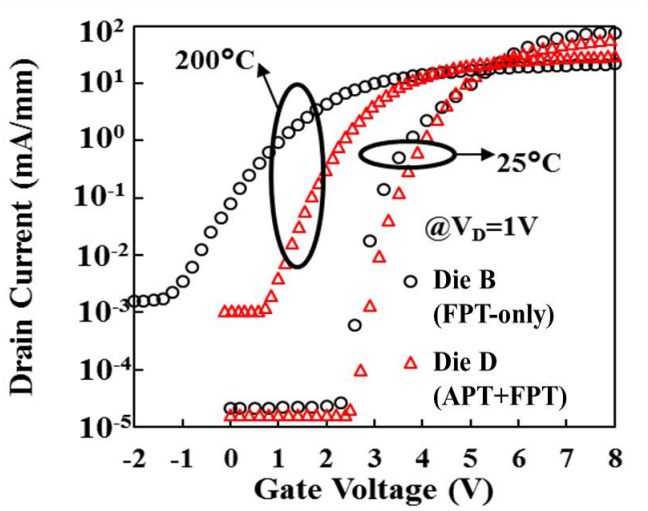


Fig. 6.7 The logarithmic I_D-V_G characteristic of Die B (gate processed with FPT-only) and Die D (gate processed with APT+FPT) at 25°C and 200°C.

The I_D-V_G hysteresis of Device B (FPT) and Device C (APT+FPT) with no delay time during the sweep at 25°C and 200°C are shown in Fig. 6.8 (a) and (b) respectively. Much smaller hysteresis of about 0.8V for Device C at 200°C is obtained than that of 2.2V for Device B, which is about 63.6% reduction in hysteresis. It indicates that less population of shallow traps within Al_2O_3, which are emitted at 200°C, is observed when the gate dielectric is treated with APT prior to FPT.

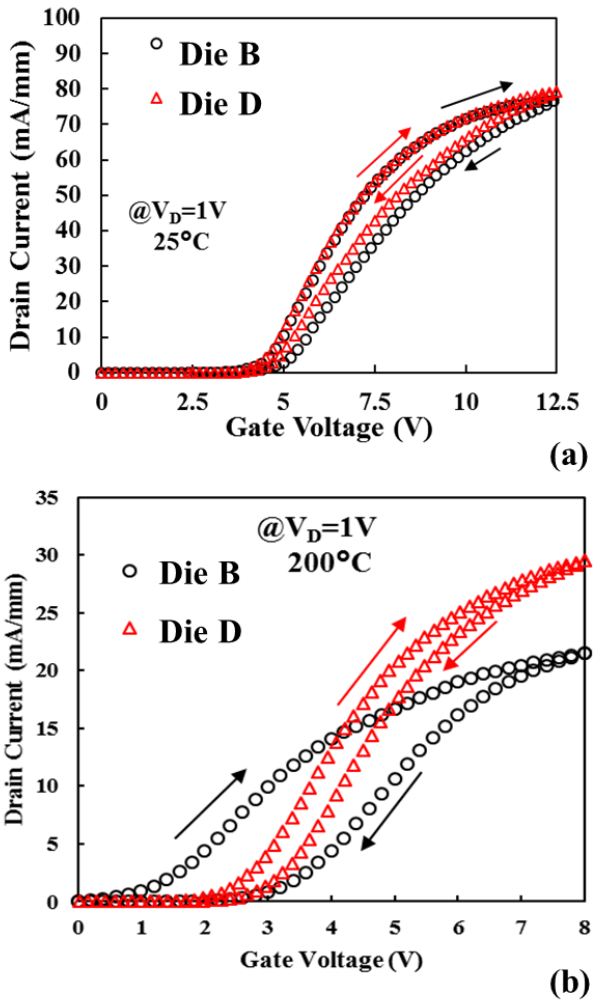


Fig. 6.8 The I_D-V_G hysteresis of Device B (FPT-only) and Device C (APT+FPT) at V_D=1V when the ambient temperature is **(a)** 25°C and **(b)** 200°C

To further elaborate the V_{TH} thermal stability and its relationship with trap distribution, the V_{TH} thermal stabilities of Dies A (no treatment), B (FPT only), and D (APT+FPT) at 25°C, 100°C, 150°C, and 200°C are reported in Fig. 6.9 (a) and (b). Generally, ICP-fluorination is able to maintain the device under enhancement-mode (V_{TH}>0V) with V_{TH}=0.6V at 200°C compared with the multiple RIE-fluorination technique [37] with V_{TH}=−2V at 200°C shown in Fig. 6.9 (b). More importantly, APT is able to improve the V_{TH} at 200°C significantly from 0.6V to 2.5V, which is the highest reported V_{TH} using the fluorination

technique to achieve normally-off operation. It implies the negative charges incorporated by FPT is mostly trapped at deeper level within the Al_2O_3 energy band if APT was applied prior to FPT. Specifically, the emission level of the electrons at different temperatures can be calculated by Eq. (6.1), where E_{T_MAX} is the deepest energy level of the trapped charges emitted from the trap sites, k_b is the Boltzmann's constant, T is the device temperature, $\gamma_n=(\nu_{th}/T^{0.5})(N_c/T^{1.5})=3.25\times10^{21}(m_n/m_0)$, where m_n/m_0=0.16 is the relative electron effective mass within Al_2O_3 [108], $\nu_{th}=(3k_bT/(m_nm_0))^{0.5}$ is the thermal velocity of Al_2O_3 [109], $N_C=2(2\pi m_n m_0 k_b T/h^2)^{1.5}$ is the effective density of states in Al_2O_3[109] and h is the Planck's constant. σ_{Al2O3} is the capture cross-section of the electrons in Al_2O_3, which is about 10^{-16} cm^2 [110], and t=50s is the device heating time to allow for sufficient device surface temperature stabilisation and to reach device quasi-steady state [111]. The E_{T_MAX} is insensitive to changes in the typical time range of tens of seconds required for reaching quasi steady state. It is reasonable to assume that all of the charges trapped in shallower levels than E_{T_MAX} can be emitted due to thermal energy, and the ones at a deeper level than E_{T_MAX} remained trapped. Once the E_{T_MAX} for a given temperature is found, as indicated in Fig. 6.9 (d), the amount of sheet negative trapped charge (Q_N) remained within the Al_2O_3 can be found from the change in V_{TH} referring to the V_{TH} at 25°C and the V_{TH} model depicted in Eq. (6.2). In Eq. (6.2), the barrier between Ni and Al_2O_3 is ϕ_b=3.5eV [93], and ΔE_1 together with ΔE_3 are the conduction band offset between AlGaN/GaN and Al_2O_3/AlGaN respectively,

which added to 2.1 eV [94]. ΔE_2 is the offset of the conduction band from the Fermi level before FPTs, which is −0.16 eV [14]. Permittivities of AlGaN and Al_2O_3 are $\varepsilon_{AlGaN}=9.2\varepsilon_0$ and $\varepsilon_{Al2O3}=7\varepsilon_0$ respectively [14, 94]. The second and the third terms in Eq. (4.1) illustrate the electrostatic potentials across the AlGaN and Al_2O_3 layers respectively. $Q_{2DEG}=6\times10^{12}\text{cm}^{-2}$ is the 2DEG density at AlGaN/GaN interface when the thickness of AlGaN is 10nm [14]. $Q_T=-1.5\times10^{12}\ \text{cm}^{-2}$ [95] is the fixed charge density at Al_2O_3/AlGaN interface.

To better estimate the densities of trap states created by plasma treatments in Al_2O_3 bandgap (D_N), the pulsed I_D-V_G measurement by stressing the gate at different levels of negative base voltage (V_B) was carried out. Based on the Poole-Frenkel trap emission theory reported in Section 5.5 which leads to the model shown in Eq. (6.3) [113], V_B is able to provide an external electric field (ξ) that enhances the emmission of negative charges trapped at deeper energy levels. Therefore, much larger reduction in V_{TH} is observed with increasing $|V_B|$. Specifically, pulsed I_D-V_G measurements with V_B from 0V to −40V held for 50s before the pulse under room temperature were performed and shown in Fig 6.9 (c). To minimise the charge injection into Al_2O_3 during the positive gate voltage sweep, 2ms-pulsed gate signals have longer 18ms-V_B between pulses. Detailed time sequence of these gate voltage pulses is shown in the inset of Fig. 6.9 (c). In Eq. (6.3), $Q_{N,0}$ and $Q_{N,VB}$, which are the trapped charges within Al_2O_3 before and after the gate stress is applied, can also be derived from the change in V_{TH} with Eq. (6.2). Hence, the comparison of E_{T_MAX} predicted by the high

temperautre and gate stressing techniques are shown in Fig. 6.9 (d). Clearly, much wider range of E_{T_MAX} is measured using the gate stressing technique.

$$E_{T\_MAX} = k_b T \ln(\gamma_n \sigma_{Al2O3} T^2 t) \tag{6.1}$$

$$V_{TH} = \frac{\phi_b - E_1 - E_2 - E_3}{q} - \frac{qQ_{2DEG}(t_{AlGaN} - t_{recess})}{\varepsilon_{AlGaN}\varepsilon_0} - \frac{q((Q_{2DEG} + Q_T)t_{Al2O3} - Q_N t_2)}{\varepsilon_{Al_2O_3}\varepsilon_0} \tag{6.2}$$

$$E_{T\_MAX} = \sqrt{q\xi/\pi\varepsilon_{Al2O3}\varepsilon_0} - (kT/q)\ln(1 - Q_{N,0}/Q_{N,VB}) \tag{6.3}$$

Where $$\xi = (V_G/t_{Al2O3} - \phi_b/qt_{Al2O3})$$

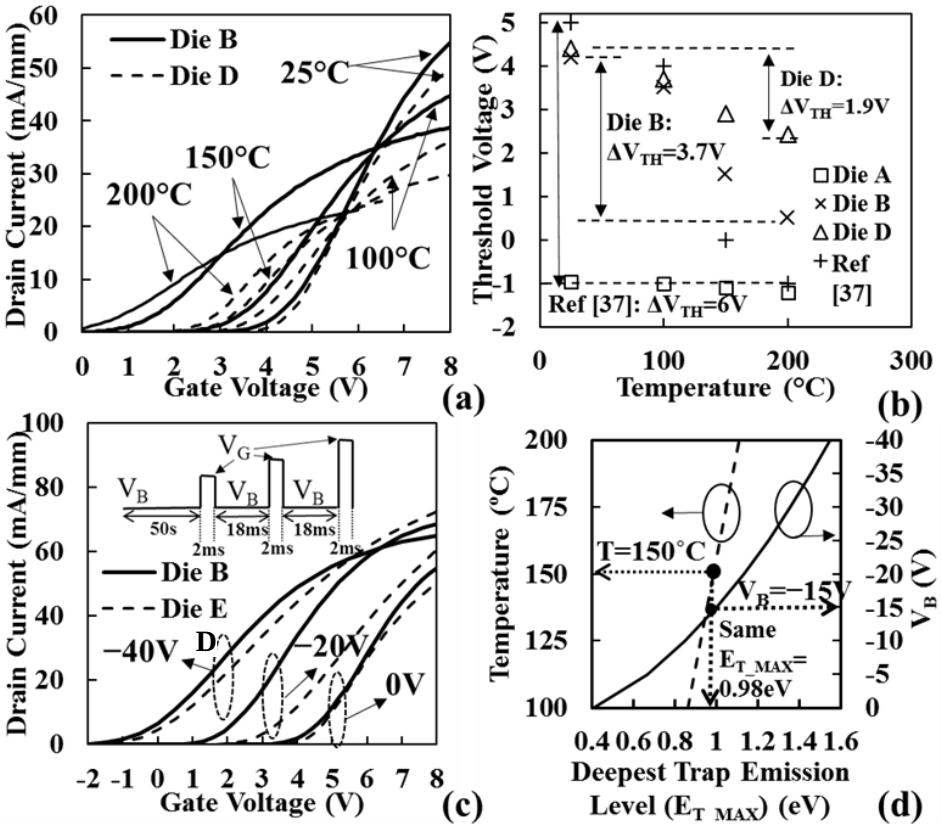


Fig. 6.9 I_D-V_G performance of Die B and D for V_D=1V) with **(a)** ambient temperatures of 25°C, 100°C, 150°C, and 200°C and **(c)** with stressed gate voltage (V_B) from 0V to −40V for 50s **(b)** The summary of ΔV_{TH} for Dies A~E at high temperatures. **(d)** The relationship between the stressed gate bias and the ambient temperature to the deepest trap emission level (E_{T_MAX})

The mechanism of trapping and emission of electrons from the fluorine plasma induced states within the Al_2O_3 energy band within a finite time is demonstrated in Fig. 6.10. When negative V_G is applied, the external field will pull the E_C up and resulted in more trapped negative charges located above the E_F which will be emitted within a period of time. In other words, the referred trap emission level at a fixed time can be varied by changing V_G. Therefore, with the application of a certain negative gate stress, the amount of trapped charge density located within a certain energy level away from E_C can be accessed without the need to increase the ambient temperature.

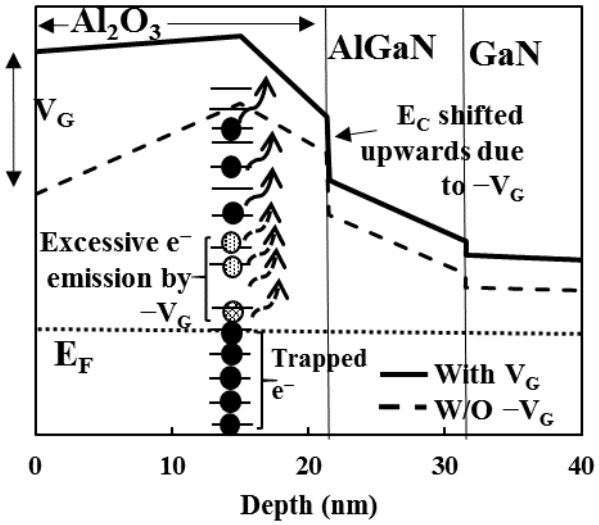


Fig. 6.10 The conduction band energy diagram along the gate stack region for fluorinated device with (solid line) and without (dashed line) negative gate stress.

The amount of intrinsic Q_N for Dies A to E at room temperature without any gate bias can be accurately calculated from the measured V_{TH} and Eq. (6.2) with verification from the good fitting to the V_{TH} obtained from Sentaurus TCAD simulation [34], as shown in Fig. 6.11 (a). In Fig. 6.11 (b), the D_N

mapping at corresponded energy level with and without APT (Die D & B respectively) are found by the gate stressing technique with V_B=0V to −40V with −5V intervals. The V_{TH} obtained for Die B and D with different negative gate stress are summarised in Table 6.3. The change in Q_N due to gate stressing test (ΔQ_{N2}) of different V_B can be extracted by integrating a sixth-order polynomial function that fitted with the D_N data-points with the RMS error less than 2%. ΔQ_{N2} can be directly compared with the change in Q_N caused by high-temperature (ΔQ_{N1}) with the same corresponded E_{T_MAX}, as shown in the Table 6.4. Generally, a good fit of less than 15% mismatch between ΔQ_{N1} and ΔQ_{N2} is observed. It indicates the effectiveness of the gate stressing technique on D_N extraction.

Table 6.3 The V_{TH} obtained for Die B and D after different gate base voltage (V_B)

V_B (V)	**−5**	**−10**	**−15**	**−20**	**−25**	**−30**	**−35**	**−40**
Die B	3.6	3.5	3.0	2.0	0.7	0	-0.3	-0.5
Die D	3.75	3.7	3.5	3.2	2.8	2.3	1.2	0

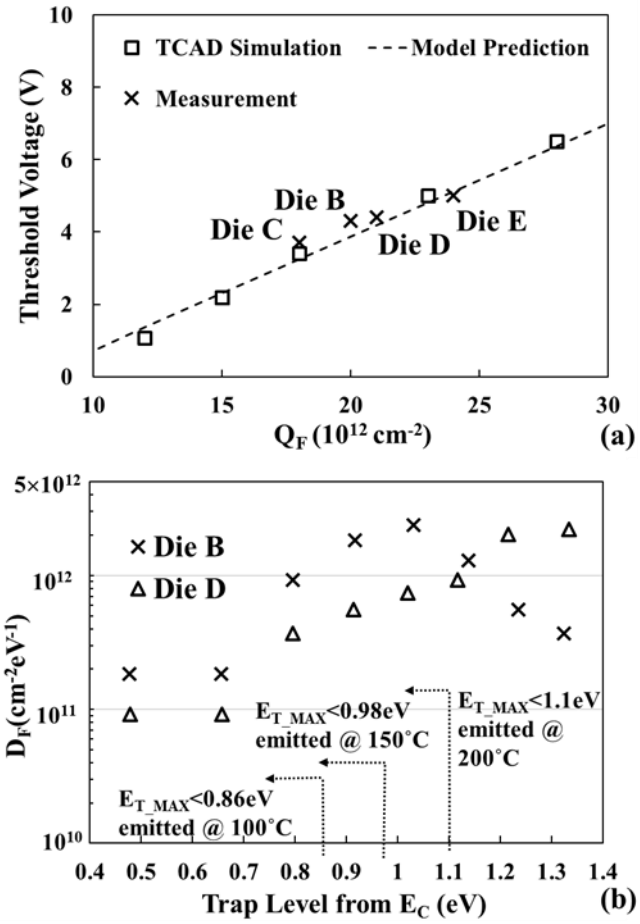


Fig. 6.11 (a) The relationship between the Q_N and the V_{TH} of Dies B~E with the usage of the model shown in Eq. (6.2) **(b)** The fluorine-induced trap state (D_N) distribution along the A_2O_3 energy level from the E_C.

Table 6.4 The amount of V_{TH} reduction from 25°C to 200ºC (ΔV_{TH}) and Q_N reduction obtained from the high temperature measurement (ΔQ_{N1}) and the integration of the 6th-order polynomical fitting of D_N (ΔQ_{N2}) for Dies B & D.

T	100 ºC		150 ºC		200 ºC	
E_{T_MAX}	0.86 eV		0.98 eV		1.1 eV	
Dies	B	D	B	D	B	D
ΔV_{TH} (V)	−0.9	−0.6	−2.7	−1.4	−3.7	−1.9
ΔQ_{N1} (10^{12} cm^{-2})	−2.3	−1.1	−5.4	−2.6	−7.1	−3.5
ΔQ_{N2} (10^{12} cm^{-2})	−2.0	−0.9	−4.5	−2.3	−6.8	−3.0
% mismatch between ΔQ_{N1} and ΔQ_{N2}	13%	18.1%	14.8%	11.5%	4.2%	14.2%

6.5 Conclusion

In this chapter, single ICP-based fluorine plasma treatment was applied on Al_2O_3 for the first time to realise normally-off operations of Al_2O_3/AlGaN/GaN MIS-HEMTs. It is able to obtain high V_{TH} of 4.2V with single plasma treatment due to the independent control on the coil and the cathode of the ICP-RIE system. Therefore, high F radical concentration and low ion bombardment energy can be obtained simultaneously with high coil power and low cathode power. In addition, by implementing a short argon plasma pre-fluorination treatment, the device can achieve a high V_{TH} of 4.4V, a satisfactory I_{DMAX} of 320mA/mm and 40% improvement on breakdown voltage than the device without Ar pre-fluorination treatment at room temperature due to the reduction in shallow trap states. Additionally, a highest-reported V_{TH} of 2.5V at 200°C compared to other FPT-processed AlGaN/GaN HEMTs was achieved from the device underwent APT prior to the FPT. With gate stressing characterisation, it was found that the negatively-charged traps tend to locate at deeper energy levels after the Ar treatment. Most of the trapped charges are located deeper than the trap emission level at 200°C (1.1eV from the conduction band edge). Therefore, more negative charges are remained in the gate dielectric to deplete the 2DEG and stabilize the V_{TH} at 200°C.

Chapter 7 The Physical Mechanism of the Argon Pre-Fluorination Treatment Leading to V_{TH} Thermal Stability Improvement

7.1 Introduction

According to Chapter 6, it was observed that the argon plasma treatment (APT) prior to the fluorine plasma treatment (FPT) treatment obtained the highest reported V_{TH} of +2.5V at 200°C among all FPT techniques. In this chapter, the underlying physical mechanisms of the APT-then-FPT process behind the improvement of V_{TH} thermal stability were investigated. Samples with the same APT and FPT recipes as the Die B and Die D reported in Chapter 6 were processed on the ALD-grown Al_2O_3 and analysed in this chapter. The detailed recipe is shown in Table 7.1. Sample C with APT-only was fabricated to verify the distribution and the role of Ar in the designed process. The depth profile of the F atoms was measured by the secondary ion mass spectroscopy (SIMS) to compare the F/Ar/O concentrations of these samples. Additionally, the X-ray photoelectron spectroscopy (XPS) analyses on the plasma-treated Al_2O_3 surfaces were performed to investigate the relative compositions of Al-O and Al-F bonds. However, it has to be ascertained that formation of different compositions of Al-F bonds can actually lead to trap formation with different distributions and energies. Hence the solution of the Schrödinger equation of $Al_2O_xF_y$ cells with defect potential modification using Gaussian 09 molecular

simulations was carried out to quantify how Al-F bond proportion affects the trap creation. Finally, the trap distribution extracted from the simulations was verified against the gate-stress experimental characterisation discussed in Section 6.4 to confirm the validity of the physical mechanism described.

Table 7.1 The parameters used for the gate plasma treatments for Samples A~D

	Sample A	**Sample B**	**Sample C**	**Sample D**
First Treatment	N/A	CHF_3-based CEP: 10W CP: 200W Time: 4 mins	Ar-based CEP: 75W CP: 100W Time: 20s	Ar-based CEP: 75W CP: 100W Time: 20s
Second Treatment	N/A	N/A	N/A	CHF_3-based CEP: 10W CP: 200W Time: 4 mins
Corresponding HEMT with the same gate structure reported in Chapter 6	Die A	Die B	N/A	Die D

7.2 Depth profile analysis for F and Ar atoms within Al_2O_3 dielectrics

To investigate the effect of APT to the F depth profile during the subsequent FPT process, the SIMS depth profile characterisation was carried out on Sample B and Sample D shown in Fig. 7.1. The APT and FPT processing recipes are identical to the ones used for Die B and Die C in Chapter 6. As material was removed during SIMS characterisation, these samples were fabricated separately from the devices discussed in Chapter 6 yet were from the same wafer

used in this thesis. 30nm of Al_2O_3 was deposited by ALD at 250°C before the plasma treatments and an additional 10nm of ALD-Al_2O_3 was deposited afterwards to seal the F atoms away from the surface to avoid the inaccuracy of SIMS characterisation at the surface. Even though the thickness of Al_2O_3 is different from the one used in Chapter 6, it does not have an effect on the F or Ar distribution. In the measured SIMS depth profile shown in Fig. 7.1 on samples B and D, an obvious increase in the peak of the F concentration is observed for the sample with APT-then-FPT process (Sample D). The peak F concentration has increased by about 85% with APT pre-fluorination process. It implies the assistance of APT in F incorporation into the Al_2O_3 as compared with Sample B due to prior creation of the additional dangling bonds after Ar bombardment. Additionally, the F depth profile is shifted towards the surface by about 2nm after APT, showing the depth of damage and dangling bonds created by APT is shallow. This also explains the slight increase in I_{DMAX} of Die D as compared with the I_{DMAX} of Die B shown in Fig. 6.5 (d). In terms of the O intensity, an obvious decrease in the relative O concentration was found at where F is present. This phenomenon indicates the replacement of O atoms by the F atoms within the Al_2O_3 dielectrics.

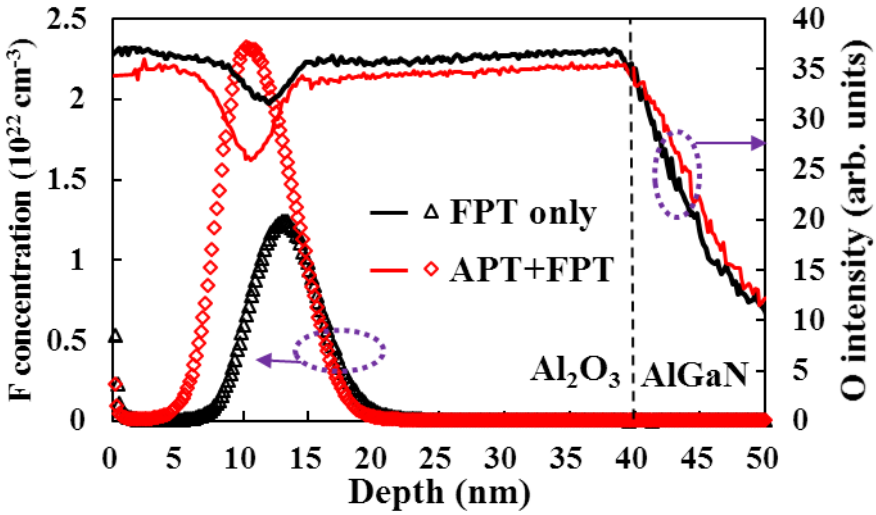


Fig. 7.1 The SIMS depth profiles for F and O atoms of the samples with (Sample D) and without APT (Sample B) prior to the FPT.

The effect of different fluorine depth profiles to the V_{TH} of the device can be investigated by transforming the profile into a sheet negative charge located at the peak of the SIMS profile, labelled as Q_N and shown in Fig. 7.2. Specifically, the depth profile of F is integrated from 0nm to 25nm from the surface and transformed into a sheet charge located at the peak of the SIMS profile. The distribution of trapped negative charges within the Al_2O_3 dielectric is assumed to be proportional to the F SIMS depth profile.

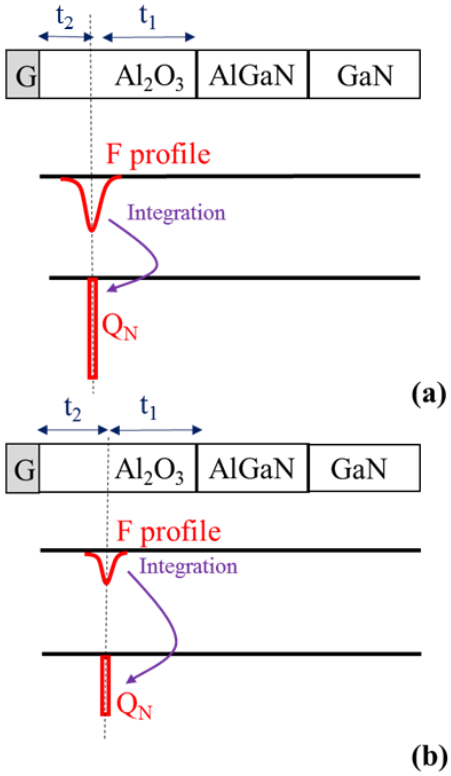


Fig. 7.2 The transformation of F depth profile into integrated sheet negative charge (Q_N) located at the peak of the profile (t_2 from the gate contact) for **(a)** sample went through APT & FPT (Sample D) and **(b)** sample went through FPT only (Sample B).

The effect of Q_N on V_{TH} can be calculated by the V_{TH} model used in Chapter 6 and shown in Eq. (7.1) [37], where the barrier ϕ_b between Ni and Al_2O_3 is 3.5eV. ΔE_1 and ΔE_3 are the conduction band offsets between Al_2O_3/AlGaN and AlGaN/GaN respectively, which added to 2.1eV. ΔE_2 is the conduction band offset from the Fermi level before fluorination treatments, which is –0.16eV. σ_{pol} is the polarisation charge between the recessed AlGaN barrier and GaN, which is 6×10^{12} cm^{-2}. Q_T=-1.5×10^{12} cm^{-2} is the fixed charge density at Al_2O_3/AlGaN interface. Q_N is the FPT-induced sheet negative charge equivalently located at the Al_2O_3/AlGaN interface. Permittivities are $\varepsilon_{AlGaN}=9.2\varepsilon_0$ and $\varepsilon_{Al2O3}=7\varepsilon_0$.

$$V_{TH} = \frac{\phi_b - E_1 - E_2 - E_3}{q} - \frac{q\sigma_{pol}(t_{AlGaN} - t_{recess})}{\varepsilon_{AlGaN}\varepsilon_0} - \frac{q((\sigma_{pol} + Q_T)t_{Al2O3} - Q_N t_2)}{\varepsilon_{Al_2O_3}\varepsilon_0} \quad (7.1)$$

Similar value of $Q_N \times t_2$ =1.37×10^{7}cm^{-1} is obtained for Sample B and D due to the shallower peak location (i.e. smaller t_2) for Sample D than Sample B even though its Q_N is greater. In other words, the effect of incorporated negative charges to the depletion of 2DEG carriers is the same for Sample B and D. As a result, since all of the other terms in Eq. (7.1) are the same between Sample B and D, the V_{TH} shall also be the same. This conclusion agrees with the similar V_{TH} of 4.2V and 4.4V obtained for Dies B and C shown in Fig. 6.4 (a) in Chapter 6. Therefore, introducing APT prior to FPT process does not influence the V_{TH} at room temperature.

It is assumed that there was no migration of F ions within our characterised range of temperatures due to the similar room-temperature V_{TH} of Sample B after several heating cycles to 200°C, which is shown in Fig 7.3. In this figure, cycle 1 is the room-temperature I_D-V_G characteristics after the device has been heated to 200°C once. The following process has been repeated again and labelled as cycle 2. The similar V_{TH} indicates the value of $Q_N \times t_2$ remained constant after these heating cycles. In other words, the temperatures used for characterisations in this study are not high enough to migrate the FTP-induced states within Al_2O_3.

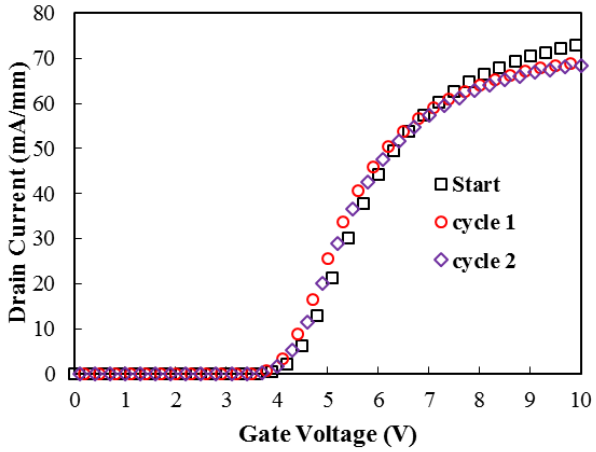


Fig. 7.3 The room-temperautre I_D-V_G characteristic of Sample B with two heating cycles to 200°C.

Additionally, the depth profiles of Ar atoms for Sample A (without Ar) and C (with Ar) were also inspected by the SIMS characterisation shown in Fig. 7.4 to evaluate the role played by Ar. It is observed that there is a decrease in the O profile for Sample C, showing the removal of the O atoms within the Al_2O_3 after the Ar treatment leading to formation of dangling bonds. It is also important to evaluate if any Ar was present in the Al_2O_3. However, the concentration of Ar atoms obtained by SIMS is not reliable due to the presence of Ca contamination on the surface introduced during the semiconductor fabrication process [118]. Hence, Ar profiles of Sample A (without APT) and Sample C (with APT-only) need to be compared to evaluate if any Ar was present. The Ar depth profile for Sample A and Sample C in Fig. 7.4 are similar, which proves the absence of Ar within Sample C since the effect of Ca contamination in these samples was identical. The Ar atoms tend to leave damages on the Al_2O_3 surface of the

sample and appear to be reflected back to the ambient. It explains why the effect of Ar is confined near the surface.

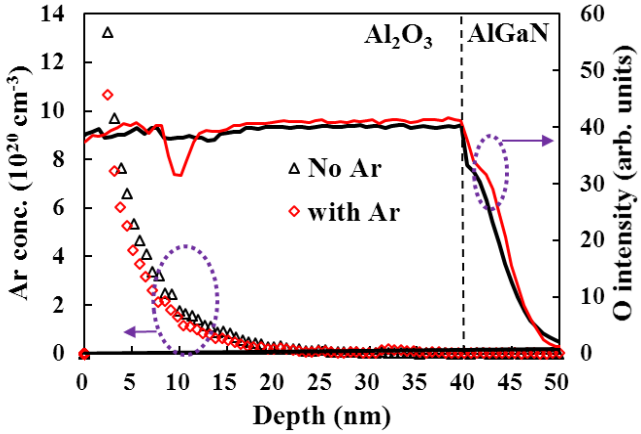


Fig. 7.4 The SIMS depth profiles for Ar and O atoms of the samples with (Sample C) and without (Sample A) APT.

7.3 Investigation of chemical compositions of plasma-treated Al_2O_3

To verify the underlying mechanism of the APT to the increase of deeper level of traps, the chemical composition study by XPS characterisations on Samples A~D was conducted. Unlike the samples used for SIMS characterisation, the plasma treated surfaces of the samples need to be exposed for XPS characterisation. The spectrum near the Al 2p and O 1s binding energies were analysed on samples A~D, and the F 1s spectrum were conducted on Sample B (FPT-only) and D (APT+FPT). According to the XPS scan near the Ar 2p binding energy for samples C and D which both underwent APT, there was no observable peak found in the spectrum. Therefore, it provides another evidence

along with the Ar depth profile from SIMS that no accountable Ar atoms remained in the sample after the APT.

In terms of the O 1s spectrum, both the APT and FPT decrease the height of the O 1s peaks as compared with the as-grown Al_2O_3 (Sample A) shown in Fig. 7.5 and Table 7.2. The detected photoelectron intensity at the O 1s peak explains the amount of electrons located at the inner 1s orbital of oxygen atoms on the sample surface. Therefore, the existence of O 1s peak is an indicator of the presence of O atoms. The reduced O 1s peaks after either APT or FPT imply the increase of oxygen vacancies (i.e. loss of oxygen atoms) at the sample surface. It is observed that Sample D with APT+FPT-processed surface has the lowest O 1s peak. Another method to characterise the O vacancies is by comparing the full widths at half maximum (FWHM) of the spectrum, which are shown in Table 7.2. Higher FWHM indicates higher amount of vacancies [119], and the highest value of the FWHM of Sample D (APT+FPT) also indicates the loss of O atoms at the surface of the Al_2O_3 samples.

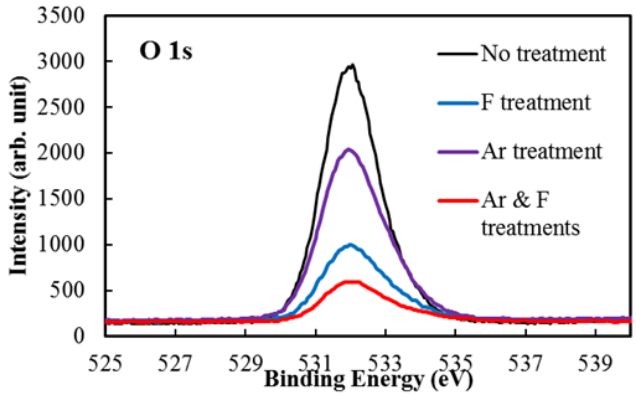


Fig. 7.5 The O 1s (binding energy=532 eV [120]) XPS spectrum of the ALD-Al_2O_3 samples with no plasma treatments (Sample A), FPT-only (Sample B), APT-only (Sample C) and APT-then-FPT (Sample D).

Table 7.2 Summary of the XPS characterisations on the O 1s spectrum for Sample A~D.

Samples	Peak Intensity (arb. unit)	FWHM (eV)
A	2949.0	1.900
B	995.7	2.217
C	2039.9	2.123
D	594.87	2.237

By fitting the measured Al 2p spectra to the reported Al-F and Al-O binding energies, the chemical composition of the Al bonds at the sample surface can be extracted. The fitting of the XPS spectrum of Sample B and Sample D to Al-F bonding (binding energy=77.17eV [121]) and Al-O bonding (binding energy=75.81 eV [122]) spectrum are shown in Fig. 7.6. The co-existence of the Al-F bonds and Al-O bonds for fluorine-treated samples is proven by the good fit between the measured XPS spectra and the spectra that combined the Al-F and Al-O spectrum. According to the Al 2p spectrum of Sample B and D and their fitting with the Al-O and Al-F spectrum shown in Fig. 7.6, the composition of Al-F bonds amongst all bonds has increased from 20.7% to 36.13% for Sample D than that for Sample B. Therefore, the APT prior to FPT can effectively increase the proportion of Al-F bonds within the material. The evidence of Al-F bonds formation also minimised the possibility of F combination with methyl groups and escape from the gate dielectric during the subsequent ALD process.

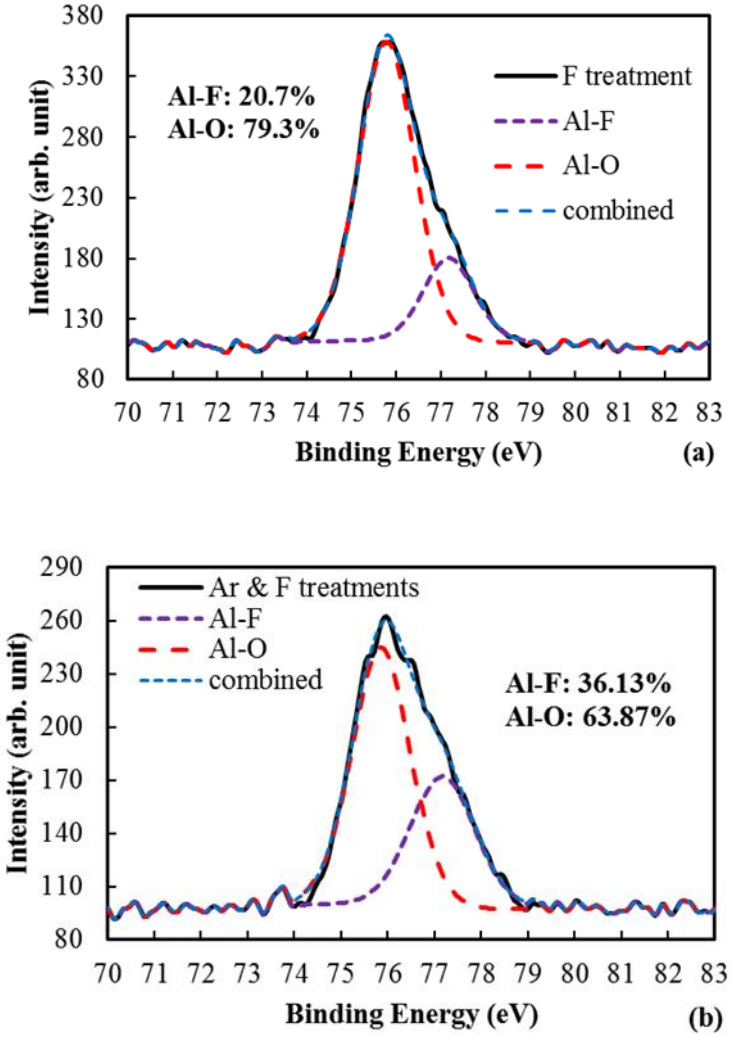


Fig. 7.6 The Al 2p XPS spectra of the ALD-Al_2O_3 sample with **(a)** F plasma treatment only (Sample B) and **(b)** Ar plasma treatment prior to the F plasma treatment (Sample D). The measured spectra is compared with the combined spectrum (blue) which consist of Al-O (red) and Al-F (purple) chemical bonding spectrum.

Finally, by directly compare the F 1s spectrum of Sample B (FPT-only) and Sample D (APT+FPT) shown in Fig. 7.7, an obvious increase in the XPS peak of Sample D is observed. Since the signal of F 1s inner shell indicates the existence of F atoms, it demonstrates the increase in the amount of F at the surface of Sample D. The peak intensity of F 1s spectra is increased by about

66% for Sample D, which presents a similar trend as the SIMS characterisations reported Fig. 7.1.

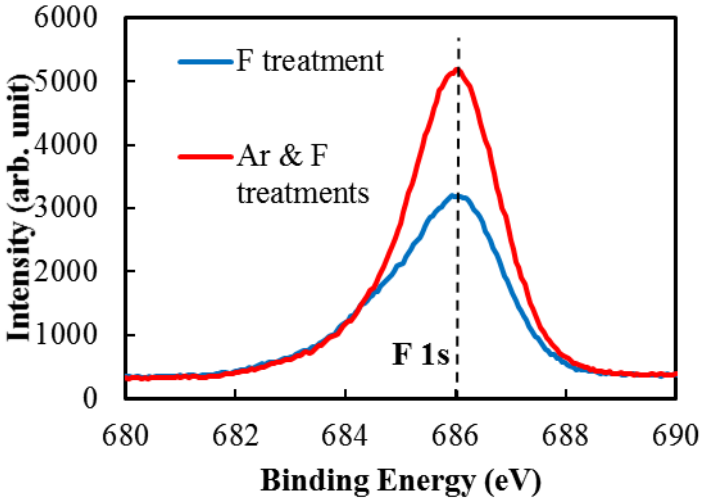


Fig. 7.7 The F 1s (binding energy=686 eV [123]) XPS spectra of the ALD-Al_2O_3 samples with F treatment only (Sample B), and Ar treatment prior to the F plasma treatment (Sample D).

7.4 Simulated trap states distribution within the Al_2O_3 energy band

To investigate the link between the Al-F bonds and the formation of trap states at deeper energy levels, the solution of the Schrödinger equation incorporating the defect potentials was used. A numerical solution was obtained for a primitive cell with 2 Al atoms bonded to a mixture of O and F when F is introduced by FPT. It yields the relative density of states (DOS) distribution within the energy bandgap (E_g) of 8.6eV. The bandgap is similar to the E_g=8.7eV of reported crystalline α-Al_2O_3 [124]. The bonding schematics of $Al_2O_xF_y$ primitive cells are shown in Fig. 7.8 (a), where each of the O atoms at the cell edge are counted as 0.5 O in the cell formula as they are shared with adjacent

primitive cells within the amorphous Al_2O_3 grown by ALD. The same bandgap (E_g) of 8.6 eV was obtained for Al_4O_6 and Al_6O_9 cluster simulations. Therefore, the same E_g is obtained regardless of the simulated cluster size. The Schrödinger equation for the traps[125, 126] is expressed as $(H_0+V)\Phi=E\Phi$, where H_0 is the Hamiltonian of the perfect crystal, V is the potential of the defects, Φ is the wave function, and E is its energy eigenvalue. When any impurities are introduced to the perfect lattice and substitute the host atoms, an additional potential V, which is related to the difference in the atomic electronegativity between them, arises near the impurities and performs as states with finite DOS forming the trap centres [125-127]. Deeper traps can be formed when more F atoms (electronegativity=3.98) [128] are substituting the O atoms (electronegativity=3.44) [128] to form more Al-F bonds locally by the APT-then-FPT treatments. To study the quantitative relationship between the composition of Al-F bonds and the trap state distribution within E_g, the atomistic first-principle simulations were numerically carried out by the Gaussian 09 software [129]. The software is able to model the electronic structures and orbital energies of desired molecular structures. The orbital energies of $Al_2O_xF_y$ lattice cell with different amount of Al-F bonds were calculated with the Hartree-Fock self-consistent method with the basis set of 6-31G for a good accuracy [130]. The proportion of Al-F bonds against the total amount of bonds used in the simulation was similar to the Al-F bond composition of 20% and 36% of the samples that underwent FPT with (Sample D) and without (Sample B)

APT shown in Fig. 7.8 (a). Once the Gaussian 09 software has solved the molecular orbital energies of the cell, the Multiwfn wavefunction analyser was then used to simulate the total DOS of the cells are plotted by the [131] in Fig. 7.8 (b). For $Al_2O_{2.5}F$ simulation (Al-F bond=17% with three O atoms shared with adjacent primitive cells), a symmetrical trap state distribution with peak DOS at about 0.96eV below E_C (i.e. the trap energy level, E_T, is 0.96eV) is found. For $Al_2O_2F_2$ simulation (Al-F bond=33%), the two F atoms can either be bonded with the same (denoted as $Al_2O_2F_2$ (I)) or different Al atoms (denoted as $Al_2O_2F_2$ (II)). Both of the calculated E_T levels are deeper than that of $Al_2O_{2.5}F$. Deepest E_T of 1.44eV is obtained for $Al_2O_2F_2$ (II) as the adjacency of the two F atoms provide the strongest local defect potential which hinders electron de-trapping.

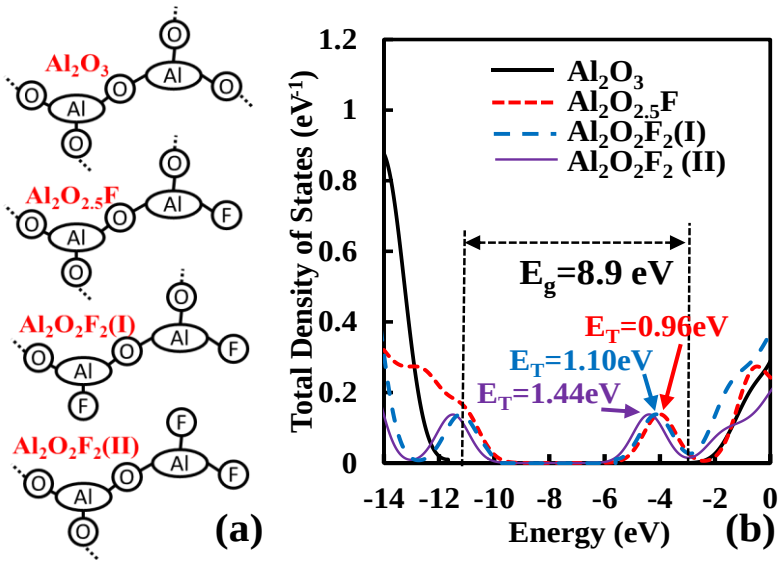


Fig. 7.8 (a) The bonding schematic of the Al_2O_3, $Al_2O_{2.5}F$, $Al_2O_2F_2$(I), and $Al_2O_2F_2$(II) primitive cells used in the Gaussian 09 simulation, where the dashed line represents the bonds connecting with adjacent primitive cells. **(b)** The simulated total DOS distrubutions of $Al_2O_xF_y$ along the energy band with the bandgap (E_g) of Al_2O_3 indicated.

To verify the simulated trap levels obtained in Fig. 7.8 (b) are realistic, the trap state densities (D_N) within the plasma-treated Al_2O_3 bandgap carried out by the gate stressing measurements on Dies B & D reported in Section 6.4 were compared. These comparisons were based on the similar Al-F composition between Die B & $Al_2O_{2.5}F$ and Die D & $Al_2O_2F_2$. Comparing the D_N of Die B (with FPT-only) shown in Fig. 6.11 (b) with the simulated DOS of $Al_2O_{2.5}F$ in Fig.7.8 (b), they have a similar energy peak level at around E_T=0.98eV. For D_N of the Die D (with APT+FPT) demonstrated in Fig. 6.11 (b) (similar Al-F composition as $Al_2O_2F_2$ clusters), it is found that the DOS of $Al_2O_2F_2$(II) provided a closer fit with the D_F of Die D than that of $Al_2O_2F_2$(I). The ratio of DOS of $Al_2O_2F_2$ (II) to $Al_2O_{2.5}F$ can be compared with the D_N of Die D to Die B along the range between 0.6eV and 1.2eV from the E_C to ensure the validity of the simulation. The comparison is listed in Table 7.3, and less than 14% mismatch between them is observed along the energy range. Therefore, $Al_2O_2F_2$ (II) is a more suitable model for the APT-then-FPT gate stack to explain its improvement in V_{TH} thermal stability. Its deeper trap level is attributed to the high local defect potential formed around the F-Al-F bonds.

Table 7.3 The simulated DOS ratio of the $Al_2O_2F_2$ (II): $Al_2O_{2.5}F$ extracted in Fig. 7.8 (b) and the characterised D_N ratio of the Die D (APT-then-FPT): Die B (FPT-only) extracted from Fig. 6.11(b). The mismatch between DOS simulation and D_N characterisation is also calculated.

E_T (eV)	**Ratio of DOS or D_N at certain E_T**		% mismatch between DOS ratio and D_N ratio
	DOS of $Al_2O_2F_2$ (II): $Al_2O_{2.5}F$ (Fig. 7.8 (b))	**D_N of Die D:Die B (Fig. 6.11 (b))**	
0.65	2.03	1.95	4.10%
0.8	2.64	2.51	5.17%
0.91	3.01	3.33	9.6%
1.02	2.82	3.24	12.96%
1.13	1.55	1.40	10.7%
1.23	0.66	0.76	13.15%

7.5 Conclusion

The mechanism of the V_{TH} high-temperature stability improvement with Ar treatment prior to the F plasma treatment was discussed in this chapter. By the SIMS characterisation, it was observed that the APT can effectively improve the peak concentration of the F depth profile and shift the location of the peak towards the surface. The decrease in the O concentration at where the F atoms were present showed the replacement of O atoms by the F atoms within the Al_2O_3. According to the XPS measurement of the plasma-treated Al_2O_3 surface, the proportion of the Al-F bonds was effectively increased from 20.1% to 36.1% for the sample with Ar bombardment.

The link between the increase in the Al-F bonds and the increase in the amount of deeper trap level states was verified by the Gaussian 09 molecular simulation. By simulating the $Al_2O_{2.5}F$ and $Al_2O_2F_2$ molecules which have the

similar Al-F bond compositions as Sample B (FPT-only) and D (APT+FPT), it was found that the increased Al-F composition can effectively shift the trap states away from the conduction band edge. In addition, the generation of F-Al-F bonding configuration after APT is one of the factors that shifts the trap states towards deeper level. The shifting of the trap level was attributed to the enhanced defect potential near the F-Al-F bonds.

Chapter 8 Conclusions and Suggested Future Work

8.1 Conclusions

Research attentions have been paid to Gallium Nitride for power device fabrication due to its superior material properties. Its high breakdown field makes the GaN-based device with high breakdown voltage possible. Meanwhile, the high mobility 2DEG induced from intrinsic polarisation field when AlGaN barrier layer is deposited on the GaN can be utilised as the highly-conductive channel of a device. However, challenges such as achieving normally-off operation with high threshold voltage at a wide range of temperatures and simultaneously maintaining an acceptable level of on-state conductivity and off-state breakdown voltage hinder the further promotion of GaN based devices. This PhD project focused on the design, simulation, fabrication and characterisation of GaN-based HEMTs with good V_{TH} thermal stability using fluorine plasma treatments on the Al_2O_3 gate dielectrics to realise normally-off operations. This study offered a possible solution to the GaN-based high-power systems which can minimise the system size and improve the system operating temperatures as compared with the conventional Si-based power electronics.

In Chapter 3, studies on the high temperature performance of GaN power HEMTs under steady state was carried out. It is important for power electronics applications as they are usually implemented at high temperature environment. The study adapted the existing analytical models for the Schottky barrier height,

2DEG carrier density, threshold voltage, and specific contact resistance under room temperature to be capable to model high temperature performances. This work provided fundamental knowledge of the physical parameters and device performance at high temperature, which is helpful in the future device design to improve the room temperature V_{TH} and obtain good V_{TH} thermal stability.

In Chapter 4, the fabrication and characterisation of normally-off Al_2O_3/AlGaN/GaN power MIS-HEMT with partial gate recess and multiple fluorine treatments to obtain high V_{TH} have been realised with successful modelling of V_{TH}. The characterised device has the highest reported threshold voltage of 6.5V for GaN-based HEMTs while preserving the maximum drain saturation current at 350mA/mm when V_G-V_{TH}=10V, the low drain/gate leakage and the breakdown voltage of up to 1130V. The device with such a high V_{TH} is desirable for power electronics applications as the noise signal has much less effect on the switching response. In addition, the standby power consumption is small for the device with high V_{TH} due to its small leakage current at V_G=0V. Meanwhile, a monolithic logical inverter with integration of the abovementioned normally-off MIS-HEMT with a normally-on MIS-HEMT the was also reported. The inverter has large output swing and fast switching speed, which offers a possible option for GaN-based power integrated circuit applications.

In Chapter 5, the thermal emission of negative charges trapped at the Al_2O_3 gate dielectric incorporated by fluorine plasma treatments was modelled and characterised. It was found that the different thermal V_{TH} stability is related to the energy level of trapped negative charge and better V_{TH} thermal stability was achieved if the trapped charges are accumulated at deeper level. The distribution of the trap states along the Al_2O_3 energy band was investigated by stressing the gate with various negative bias for a period of time. It was also found that the higher fluorine plasma treatment power resulted in the accumulation of trapped negative charges at deeper energy level from the Al_2O_3 conduction band. As a result, the V_{TH} was retained at 2V instead of –2V at 200°C if the fluorine plasma power had been increased from 30W to 90W. The study accomplished in this chapter provided a clear explanation on the relationship between the V_{TH} thermal stability and the fluorine treatment recipe with trap distribution mapping within the energy band. It provided important information for the design of fluorine plasma treatment recipe to achieve good V_{TH} thermal stability.

In Chapter 6, a novel short argon pre-fluorination treatment was implemented to create more O vacancies on the surface of Al_2O_3 prior to the fluorine treatments to allow for extra Al-F bond formation. Meanwhile, the multiple fluorine plasma treatments by conventional RIE was replaced with single ICP-RIE treatment for the first time to obtain high V_{TH} with a much simpler approach. With ICP-RIE technique, the fluorine flux and the bombardment energy can be controlled independently to obtain high

concentration of F radicals to improve the V_{TH} but small ion bombardment energy to minimise the 2DEG degradation. As a result, the V_{TH} of the fabricated device with APT-then-FPT process was able to reach 4.4V and 2.5V at 25°C and 200°C respectively. According to the gate-stressing technique reported in Chapter 5, the Ar pre-fluorination technique was able to shift the peak of the trapped charge levels from E_T=1eV towards deeper energy levels. The argon pre-fluorination treatment, which was firstly proposed in this thesis research, suggested an effective method to improve the V_{TH} thermal stability of normally-off AlGaN/GaN HEMTs utilising fluorine plasma treatment techniques on the gate.

The physical mechanism of the argon pre-fluorination treatment was further discussed in Chapter 7. With SIMS measurement on the fluorine depth profile, it was found that the argon pre-fluorination treatment can effectively increase the peak of the F atoms by about 85% and shift the peak location by about 2nm closer to the surface. With XPS characterisation, it was found that argon pre-fluorination treatment has effectively increased the composition of Al-F bonds at the Al_2O_3 surface from 20% to 36% of the total amount of bonds. The link between the increase in Al-F bonds and the amount of deeper level traps was verified by the Gaussian 09 molecular simulation tools. The simulation revealed the density of states distributions of $Al_2O_2F_2$(II) (where two F atoms bonded to one Al atom) and $Al_2O_{2.5}F$ cells have similar peak location to the fabricated devices with and without argon pre-fluorination treatment reported in Chapter

6 respectively. The thorough investigations of the physical mechanism on the argon pre-fluorination with various characterisation techniques provided clear evidence and explanation of the underlying physics on the V_{TH} thermal improvement of the devices reported in Chapter 6. In addition, the Gaussian 09 simulation has linked the trap state distribution and the chemical composition of fluorine plasma treated dielectrics, which is useful for the study of traps within a device.

8.2 Proposed Future Works

In summary, this thesis provided possible solutions to the future application of GaN-based HEMTs within a power electronic circuit under high-temperature ambient with successful fabrication of normally-off AlGaN/GaN HEMTs with high V_{TH} under either room temperature or high temperatures up to 200°C. However, several issues related to this work require further development before actual implementation.

Regarding the fabrication of the normally-off Al_2O_3/AlGaN/GaN MIS-HEMTs by using partial recess on AlGaN barrier and fluorine plasma treatments on the Al_2O_3, one of the difficulties is the control of the recess depth of the AlGaN barrier. Since the AlGaN recess technique is normally achieved by the ICP dry etching technique, the error in the etching speed is inevitable due to the difficult control of the chamber and plasma conditions. It is suggested to utilise

wet etching technique or the oxidation-then-wet-etching techniques [117] to enhance the integrity of the AlGaN barrier etching depth.

It is also suggested to carry out more research on the devices using argon pre-fluorination technique, especially on its switching behaviour. Even though the gate stress characterisation conducted in Chapter 7 did not observe any obvious difference in the shallow trap distribution between the devices with or without any argon treatments, the trap state distribution at levels near E_C is still unknown. The shallow state distribution is dominant in the switching characteristics of the device, thus requires further investigation before actual application in the power electronic circuits.

In addition, it is also possible to find other substances for pre-fluorination treatment. According to the research findings in this thesis, it does not matter which substance is used as the source of ion bombardment as long as it is heavy enough to create damages to the Al_2O_3 surface. It is possible to find another substance which is able to create more surface damage, or even being able to alter the defect potential within the material and further enhance the deep trap population.

In terms of the device application into circuits, the fluorine-treated device has the potential to be applied in the power integrated-circuit. For instance, a logical monolithic inverter with good output swing and fast switching speed has been reported in Section 4.5 in the thesis. However, the high temperature

performance of the inverter was not carried out in this thesis research. It is important to carry out a thorough research on the high temperature rating of the inverter before being implemented in actual applications.

Finally, the integration of the reported devices into a more complicated power IC can be studied in the future. For example, these devices are possible to be integrated as the power switches for a DC-DC buck/boost converter, or DC-AC inverters. By fabricating the integrated circuit on the GaN platform, the size of the circuit can be significantly reduced comparing with the conventional Si-based power IC. The size reduction of the system is attributed to the much higher power density for GaN-based devices and the reduction in the size of the cooling system as compared with Si-based system.

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Appendix I: Run Script of the Sentaurus Device Simulation for Normally-off Al_2O_3/AlGaN/GaN MIS-HEMTs

The run script is an example script used for the Sentaurus device simulation of Die E reported in Chapter 4.

Defining the electrodes:

```
Electrode {
    { Name="gate"     Voltage= 0 Schottky Workfunction= 5.1}
    { Name="source" Voltage= 0 Schottky Workfunction= 4.3}
    { Name="drain"    Voltage= 0 Schottky Workfunction= 4.3}
}
```

Calling the input files and naming the output file:

```
File {
    Grid= "sdemodel_msh.tdr"
    Parameter= "MIS.par"
    Current= "MIS_des.plt"
    Plot= "MIS_des.tdr"
    Output= "MIS_des.log"
}
```

Calling the physics models using for the solution of the entire device (based on the template for normally-on AlGaN/GaN HEMTs issued in [36]):

```
Physics {
    AreaFactor= 1000
    Mobility (
            DopingDependence
            Highfieldsaturation
            )
    EffectiveIntrinsicDensity (Nobandgapnarrowing)
    Fermi
    Piezoelectric_Polarisation (strain)
    Thermionic
    eBarrierTunneling "SourceNLM"
    eBarrierTunneling "DrainNLM"
}
```

Defining the polarisation field strength at AlGaN/GaN interface (strain activation rate of the partially-recessed AlGaN is defined based on the 2DEG concentration fitting with [14]):

```
Physics (MaterialInterface="AlGaN/GaN") {
    Piezoelectric_Polarisation (strain activation=0.7)
}
```

Defining the bulk traps within GaN (based on the template for normally-on AlGaN/GaN HEMTs issued in [36]):

```
Physics (Material="GaN") {
    Traps (
        (Acceptor Level Conc= 6.0e17 EnergyMid= 1.1 EnergySig= 0
        FromMidBandGap eXSection= 1e-15 hXSection= 1e-15)
    )
}
```

Defining the Al mole fraction and bulk traps within AlGaN (based on the template for normally-on AlGaN/GaN HEMTs issued in [36]):

```
Physics (Material="AlGaN") {
        MoleFraction( xFraction= 0.25 Grading= 0)
        Traps (
            (Acceptor Level Conc= 1e16 EnergyMid= 1.0 EnergySig= 0
            FromMidBandGap eXSection= 1e-15 hXSection= 1e-15)
        )
}
```

Defining the polarisation field at the AlGaN/passivation interface (strain activation is absent as the oxide is amorphous):

```
Physics (MaterialInterface="AlGaN/Oxide") {
        Piezoelectric_Polarisation (strain activation=0)
}
```

Defining the polarisation field at the AlGaN/Al_2O_3 interface (strain activation is absent as the oxide is amorphous):

```
Physics (MaterialInterface="AlGaN/Insulator1") {
        Piezoelectric_Polarisation (strain activation=0)
}
```

Defining the negative charge concentration at the first fluorine plasma treated surface located at the AlGaN/Al_2O_3 interface (fixed charge concentration is based on the fitting of simulated V_{TH} with the experimental V_{TH} by I_D-V_G characterisation):

```
Physics (RegionInterface="AlGaN/1AO") {
        Piezoelectric_Polarisation (strain activation=0)
```

```
        Traps(
                (FixedCharge Conc= -1.5e12)
            )
}
```

Defining the negative charge concentration at the second fluorine plasma treated surface located between t_1 and t_2 in Al_2O_3 reported in Chapter 4(fixed charge concentration is based on the fitting of simulated V_{TH} with the experimental V_{TH} by I_D-V_G characterisation):

```
Physics (RegionInterface="1AO/2AO") {
    Traps(
            (FixedCharge Conc= -7.42e12)
        )
}
```

Defining the negative charge concentration at the third fluorine plasma treated surface located between t_2 and t_3 in Al_2O_3 reported in Chapter 4 (fixed charge concentration is based on the fitting of simulated V_{TH} with the experimental V_{TH} by I_D-V_G characterisation):

```
Physics (RegionInterface="2AO/3AO") {
    Traps(
            (FixedCharge Conc=-1.2e13)
        )
}
```

Defining the negative charge concentration at the fourth fluorine plasma treated surface located between t_3 and t_4 in Al_2O_3 reported in Chapter 4 (fixed charge concentration is based on the fitting of simulated V_{TH} with the experimental V_{TH} by I_D-V_G characterisation):

```
Physics (RegionInterface="3AO/4AO") {
    Traps(
            (FixedCharge Conc= -1.29e12)
        )
}
```

Defining the non-local mesh at the ohmic contacts (required for carrier tunnelling model. Selection of parameters is based on the template for normally-on AlGaN/GaN HEMTs issued in [36]):

```
Math {
    NonLocal "SourceNLM" (
        Electrode="source"
        Digits= 4
        Length= 12e-7
        EnergyResolution= 1e-3
```

```
    )
    NonLocal "DrainNLM" (
        Electrode="drain"
        Digits= 4
        Length= 12e-7
        EnergyResolution= 1e-3
    )
}
```

Defining parameters required for output demonstration (selection of models is based on the template for normally-on AlGaN/GaN HEMTs issued in [36]):

```
Plot {
    NonLocal
    Electricfield/Vector
    eCurrent/Vector hCurrent/Vector TotalCurrent/Vector
    SRH Avalanche
    eMobility hMobility
    eQuasiFermi hQuasiFermi
    eGradQuasiFermi hGradQuasiFermi
    eEparallel hEparallel
    eVelocity hVelocity
    Doping DonorConcentration Acceptorconcentration
    SpaceCharge
    ConductionBand ValenceBand
    BandGap Affinity
    xMoleFraction
    PE_Polarisation/Vector
    PE_Charge
    eTrappedCharge eInterfaceTrappedCharge
    hTrappedCharge hInterfaceTrappedCharge
    eBarrierTunneling
}
```

Defining the mathematical models used for device solution (selection of models is based on the template for normally-on AlGaN/GaN HEMTs issued in [36]):

```
Math {
    Transient= BE
    ExitOnFailure
    Extrapolate
    Iterations= 20
    DirectCurrentComputation
    ErrRef(Electron)=1e5
    ErrRef(Hole)=1e5
```

```
    ExtendedPrecision
    Digits= 5
    RHSMin= 1e-15
    RHSMax= 1e30
    eDrForceRefDens= 1e8 hDrForceRefDens= 1e8
    CNormPrint
    NewtonPlot (
    Error MinError Residual)
}
```

Defining the sweeping method for the simulation (I_D-V_G sweep from V_G=0V to 15V with V_D=1V, coding is based on the template for normally-on AlGaN/GaN HEMTs issued in [36]:

```
Solve {
    Coupled (Iterations=10000 LinesearchDamping=1e-5) {Poisson}
    Coupled (Iterations=10000 LinesearchDamping=1e-5) {Poisson Hole}
    Coupled (Iterations=10000 LinesearchDamping=1e-5) {Poisson Electron Hole}

    Plot(FilePrefix="Zero_Bias")
    Quasistationary (
                InitialStep=1e-2 Minstep=1e-5 MaxStep=0.2
                Increment=1.6
                Goal{Name="drain" Voltage=1}
        ){
                Coupled {Poisson Electron}
          }
    Quasistationary (
                InitialStep=1e-2 Minstep=1e-5 MaxStep=0.25
                Increment=1.6
                Goal{Name="gate" Voltage=15}
        ){
                Coupled {Poisson Electron}
          }
}
```

Appendix II: Processing Parameters for Device Fabrication

Table A-1. Major fabrication process flow for fluorine-treated normally-off Al_2O_3/AlGaN/GaN MIS-HEMT

Steps	Process	Equipment Used	Process Outcome
1	Wafer Cleaning	Fume Cupboard	Cleaned wafer with dirt removed
2 (a)	Lithography (Double UV Exposure)	Karl Suss MA6 Mask Aligner	Ti/Al/Ni/Au with thickness of 25/125/45/55 nm
2 (b)	Drain/Source Metal Deposition	ULVAC EX-400 Electron-beam Film Evaporator	
2 (c)	Metal Lift-off	Fume Cupboard	
3	Rapid Thermal Annealing	BPS Nextral ADAX 60	Formation of ohmic contacts with Ti/Al/Ni/Au alloy
4 (a)	Lithography (Single Exposure)	Karl Suss MA6 Mask Aligner	~600 nm of AlGaN and GaN etched in the mesa region
4 (b)	Mesa Isolation	STS Multiplex ICP-RIE System	
5	Surface Passivation	Oxford Plasmalab 80 Plus PECVD System	~200nm of SiO_2 deposited
6 (a)	Lithography (Single UV Exposure)	Karl Suss MA6 Mask Aligner	~200nm SiO_2 etched at the gate
6 (b)	Gate Region Opening	STS Multiplex ICP-RIE System	
7	AlGaN Recess at the Gate Region	STS Multiplex ICP-RIE System	~10nm of AlGaN etched at the gate
8 (a)	Gate Dielectric Deposition	Savannah 100 ALD system	Plasma-treated Al_2O_3 gate dielectric
8 (b)	Plasma Treatments	STS Multiplex ICP-RIE System/Oxford PlasmaPro 80 RIE System	

9 (a)	Lithography (Double UV Exposure)	Karl Suss MA6 Mask Aligner	Ni/Au gate contact (15/150 nm)
9 (b)	Gate Metal Deposition	ULVAC EX-400 Electron-beam Film Evaporator	
9 (c)	Metal Lift-off	Fume Cupboard	
10 (a)	Lithography (Single UV Exposure)	STS Multiplex ICP-RIE System	Metal pads are exposed for device characterisations
10 (b)	Pad Opening	STS Multiplex ICP-RIE System	

Table A-2. Detailed processing procedure for wafer cleaning

(Refer to step 1 in Table A-1)

Steps	Process	Parameters
1	Organic Contamination Removal	Dip in H_2SO_4+H_2O_2 mix (ratio of 3:1) for 2 minutes; then rinse with DI water
2	Native Oxide Removal	Dip in buffered oxide etch (BOE) for 15s; then rinse with DI water

Table A-3. Detailed processing procedure for lithography (double UV exposure)

(This process is used for the lithography processes which require lifting-off (Steps 2(a) & 9(a) in Table A-1) as undercuts at the resist sidewall are obtained)

Steps	Process	Parameters
1	HMDS spin-coating for adhesion enhancement	3000 rpm for 20s
2	AZ-5214E Photoresist spin-coating	3000 rpm for 20s
3	Photoresist Pre-baking	120^{o} C for 60s
4	UV Light Exposure after aligned with the mask pattern	2s exposure at UV wavelength of 320nm
5	Photoresist Post-baking	120^{o} C for 90s
6	UV Light Exposure without mask	30s exposure at UV wavelength of 320nm
7	Pattern Development	Dip into FHD-5 positive photoresist developer for 50s
8	Lift-off after metal deposition	Dip into acetone and placed in ultrasonic cleaner for 20 min
9	Acetone Removal	Dip into IPA and placed in ultrasonic cleaner for 10 min
10	IPA Removal	Dip into DI water and placed in ultrasonic cleaner for 10 min; blow dry with N_2 gun

Table A-4. Detailed processing procedure for lithography (single UV exposure)

(This procedure is used for lithography processes which require no lifting-off (Steps 4(a), 6(a), and 10(a) in Table A-1))

Steps	Process	Parameters
1	HMDS spin-coating for adhesion enhancement	3000 rpm for 20s
2	AZ-5214E Photoresist spin-coating	3000 rpm for 20s
3	Photoresist Pre-baking	120^{o} C for 90s
4	UV Light Exposure after aligned with the mask pattern	30s exposure at UV wavelength of 320nm
5	Pattern Development	Dip into FHD-5 positive photoresist developer for 50s
6	Post-process photoresist removal	Dip into acetone and placed in ultrasonic cleaner for 10 min
7	Acetone Removal	Dip into IPA and placed in ultrasonic cleaner for 10 min
8	IPA Removal	Dip into DI water and placed in ultrasonic cleaner for 10 min; blow dry with N_2 gun

Table A-5. Detailed processing procedure for metal deposition by thermal evaporator

(Refer to steps 2(b) & 9(b) in Table A-1)

Steps	Process	Comments
1	Sample & Crucible Loading	Load the required metal crucibles with sufficient amount of metals within
2	Chamber Vacuuming	Wait until the chamber pressure is under 4×10^{-6} Pa (~2 hours)
3	E-beam location adjustment	Ensure the electron beam is bombarding the surface of the metal crucible
4	Metal Deposition	Carefully control the speed of metal deposition for good deposition uniformity and quality. Ensure the rate is around 0.1nm/s.
5	Crucible Cooling	Allow for about 3 min of cooling time after each deposition before changing the crucible
6	Change of Crucible	Change the crucible to the next required metal and repeat from step 3.
7	Chamber Vent & Sample Unloading	When metal deposition is completed, vent the chamber and unload the sample. Finally, vacuum the chamber after usage to avoid chamber contamination.

Table A-6. Parameters used for 500nm mesa isolation by ICP-RIE

(Refer to step 4(b) in Table A-1.)

Step 1: High Power Etch for fast etching speed (~2.3nm/s)		
Gas Flow	Ar	15 sccm
	BCl_3	2 sccm
	Cl_2	8 sccm
Pressure		120 mTorr
Coil Power		100 W
Cathode Power		175 W
Etch Time		190s
Step 2: Low Power Etch for improved etched surface quality (~0.3nm/s)		
Gas Flow	Ar	15 sccm
	BCl_3	2 sccm
	Cl_2	8 sccm
Pressure		120 mTorr
Coil Power		30 W
Cathode Power		30 W
Etch Time		200s

Table A-7. Parameters used for 200nm of SiO_2 Surface Passivation by PECVD

(Refer to step 5 in Table A-1)

Gas Flow	**N_2O**	706 sccm
	SiH_4/N_2	158 sccm
Pressure		906 mTorr
RF Power		18 W
Valve Position		26.3º
Temperature		300º C
SiO_2 deposition Time (rate is about 0.4nm/s)		450s

Table A-8. Parameters used for 200nm of gate region opening by ICP-RIE

(Refer to step 6(b) in Table A-1)

Gas Flow	**Ar**	5 sccm
	SF_6	20 sccm
Pressure		50 mTorr
Coil Power		5 W
Cathode Power		100 W
SiO_2 Etching Time (rate is about 0.6nm/s)		330s

Table A-9. Parameters used for AlGaN Recess by ICP-RIE

(Refer to step 7 in Table A-1)

Gas Flow	**Argon**	15 sccm
	BCl_3	2 sccm
	Cl_2	8 sccm
Pressure		120 mTorr
Coil Power		30 W
Cathode Power		30 W
Etch Time		30s

Table A-10. Parameters used for ALD-Al_2O_3 gate dielectric deposition

(Refer to step 8(a) in Table A-1)

Gas Flow	**Tri-methyl-aluminium (TMA)**	20 sccm
	H_2O	
Temperature		250^{o} C
Al_2O_3 Thickness per cycle		0.1nm

Table A-11. Parameters used for gate plasma treatment by RIE or ICP-RIE

(Refer to step 8(b) in Table A-1)

A: RIE Treatment	
CHF_3 gas flow	50 sccm
Pressure	37.5 mTorr
RF Power	Refer to Table 4.2, 5.1
Treatment Time	
B: ICP-RIE Treatment	
Step 1: Argon pre-treatment	
Ar gas flow	10 sccm
Pressure	15 mTorr
Cathode Power	Refer to Table 6.1
Coil Power	
Treatment Time (Varied)	20s
Step 2: Fluorine treatment	
CHF_3 gas flow	36 sccm
Pressure	37.5 mTorr
Cathode Power	10W
Coil Power	Refer to Table 6.1
Treatment Time	

Table A-12. Parameters used for pad opening by ICP-RIE

(Refer to step 10(b) in Table A-1)

Step 1: Al_2O_3 Etch		
Gas Flow	Ar	10 sccm
	BCl_3	25 sccm
Pressure		15 mTorr
Coil Power		100 W
Cathode Power		175 W
Etch Time		180s
Step 2: SiO_2 Etch		
Gas Flow	Ar	5 sccm
	SF_6	20 sccm
	Cl_2	8 sccm
Pressure		50 mTorr
Coil Power		5 W
Cathode Power		100 W
Etch Time		300s

Appendix III: List of Publications Related to this PhD Research

[1] **Y-H. Wang**, Y.C. Liang, G.S. Samudra, T-F. Chang, C-F. Huang, Y. Li and G-Q. Lo, "Analytical modelling of high temperature characteristics on the DC responses for Schottky-gate AlGaN/GaN HEMT devices" *5th International Energy Conversion Congress and Exhibition for Asia/Pacific region (ECCE Asia),* Melbourne, Australia, June 3-6, 2013.

[2] **Y-H. Wang**, Y.C. Liang, G.S. Samudra, T-F. Chang, C-F. Huang, Y. Li and G-Q. Lo, "Modelling temperature dependence on AlGaN/GaN power HEMT device characteristics" *Semiconductor Science and Technology,* vol. 28, pp. 125010, 2013.

[3] H. Huang, **Y-H. Wang**, Y.C. Liang, G.S. Samudra, C-F. Huang, W-H. Kuo, "5V high threshold voltage normally-off MIS-HEMTs with combined partially recessed and multiple fluorinated-dielectric layers gate structures" *46th Int. Conf. on Solid State Devices & Materials (SSDM),* Tsukuba, Japan, Sep. 8-11, 2014.

[4] **Y-H. Wang**, Y.C. Liang, G.S. Samudra, H. Huang, B-J. Huang, S-H. Huang, T-F. Chang, C-F. Huang, W-H. Kuo and G-Q. Lo, "6.5V High-V_{TH} AlGaN/GaN power MIS-HEMT and threshold voltage analytic modelling on multi-layer fluorinated gate stack", *IEEE Electron Device Letters,* vol. 36, pp. 381-383, 2015.

[5] **Y-H. Wang**, Y.C. Liang, G.S. Samudra, B-J. Huang, Y-C. Liao, C-F. Huang, W-H. Kuo and G-Q. Lo, "Effect of Gate Threshold Swings by ALD-Al_2O_3/AlGaN Interfacial Traps in GaN Power HEMT with Multiple Fluorinated Gate Dielectric Layers" *International Conference on Compound Semiconductor Manufacturing Technology (CS MANTECH)*, Scottsdale, USA, May. 18-21, 2015.

[6] **Y-H. Wang**, Y.C. Liang, G.S. Samudra, B-J. Huang, Y-C. Liao, C-F. Huang, W-H. Kuo and G-Q. Lo, "High Output Swing Monolithic Inverter with E-D Mode MIS-HEMTs for GaN Power Integrated Circuits" *The 11th IEEE International Conference on Power Electronics and Drive Systems (PEDS)*, Sydney, Australia, June. 9-12, 2015.

[7] T-F., Chang, T-C. Hsiao, S-H. Huang, C-F. Huang, **Y-H. Wang**, G.S. Samudra and Y.C. Liang "Threshold Voltage Instability in AlGaN/GaN HEMTs", *The 11th IEEE International Conference on Power Electronics and Drive Systems (PEDS)*, Sydney, Australia, June. 9-12, 2015.

[8] C-F. Huang, T-F. Chang, **Y-H. Wang** and Y.C. Liang, "(Invited) The Stability of High Voltage AlGaN/GaN HEMTs" *ECS Transactions*, vol. 66, pp. 127-137.

[9] **Y-H. Wang**, Y.C. Liang, G.S. Samudra, P-J Chu, Y-C. Liao, C-F. Huang, W-H. Kuo, and G-Q. Lo, "High-temperature studies of multiple fluorinated traps within an Al_2O_3 gate dielectric for E-Mode AlGaN/GaN power MIS-

HEMTs" *Semiconductor Science and Technology*, vol. 31, pp. 025004, 2015.

[10] **Y-H. Wang**, Y.C. Liang, G.S. Samudra, C-F. Huang, W-H. Kuo, and G-Q. Lo, "The Physical Mechanism on the Argon Pre-Fluorination Plasma Treatment Leading to High-Temperature Threshold Voltage Stability Improvement for Normally-off Al_2O_3/AlGaN/GaN MIS-HEMTs", *Applied Physics Letters* (Reviewing)