A TRANSCEIVER DESIGN FOR IMPLANTABLE MEDICAL DEVICES

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DECLARATION

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

LI CHONG
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Contents

Summary

In recent years, implantable devices and wearable devices are extensively applied in clinic to assist patients either to substitute the missing function of a damaged organ or to alleviate and remedy the disease progression of a malfunctioning part in the body. It has become one of the hottest topic in the intersection of electronic and medical. A number of products and applications such as brain pacemakers, retinal implants, wearable blood pressure monitors and blood glucose detectors have been released into healthcare markets. They are often used with operational software applets installed on smart phones/ tablets in order to monitor or assist the therapy of epilepsy, amblyopia, and even heart diseases. One of the key challenges of developing these devices is to reduce both the device size and power consumption while improving data rate and power efficiency. These two requirements are difficult to be simultaneously achieved because increasing data transfer rate normally increases the power consumption and enlarges the device size.

In this research, we propose a transceiver design for an implantable medical device that utilizes inductive coupling coils for data and power transmission. A Class E power amplifier was employed to amplify and transfer power from the transceiver side (external device) to the receiver side (internal implant). And then with a Load Shift Keying (LSK) demodulator --- a particular scheme of Amplitude Shift Keying (ASK) which has a higher data recovery efficiency compared to Frequency Shift Keying (FSK) structure for digital signal transmission --- the biological data captured by the implant were transmitted back to the transceiver. The LSK demodulation technique allowed power and data to be transferred simultaneously through one single inductive link. It could work under a variety

of modulation indexes and different coding/decoding protocols. Furthermore, it enables us to reduce both the power consumption and the device size of the transceiver. The circuits were fabricated in 180nm CMOS process technology and a prototype was designed to demonstrate the performance of the proposed demodulator. Measurement results indicated that the circuit could support the power carrier signal of different frequencies and data rates. The core area of the chip was 750μm x 800μm and the achievable minimum modulation index of the prototype was 5%, whereas the supported data rate was 1 Mbps. With a 1.65V power supply the total current consumption was 3.6 mA.

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List of Acronyms

AC	Alternating Current
ADC	Analog to Digital converter
ASK	Amplitude-Shift Keying
BMJ	British Medical Journal
CMOS	Complementary Metal-Oxide Semiconductor
CR SAR ADC	Charge Redistribution Successive Approximation Register ADC
DAC	Digital to Analog Converter
DC	Direct Current
DNL	Frequency Shift Keying
ECG	Electrocardiogram
EEG	Electroencephalogram
EMG	Electromyography
FCC	Federal Communication Committee
FDA	Food and Drug Administration
FPGA	Field-Programmable Gate Array
FSK	Frequency Shift Keying
GBW	Gain–bandwidth
INL	Integral Nonlinearity
IC	Integrated Circuits
IT	Information Technology
LSB	Lest Significant Bit
LSK	Load Shift Keying
Mbps	Megabits per second
MICS	Medical Implant Communication Services
MOS	Metal Oxide Semiconductor
MS	Mega Samples
MSB	Most Significant Bit
NASA	National Aeronautics and Space Administration
Op amp	Operational Amplifier
OTA	Operational Transconductance Amplifier
PCB	Printed Circuit Board
PSK	Phase-Shift Keying
RC	Resistor–Capacitor
RF	Radio Frequency
SAR	Successive Approximation Register
SAR ADC	Successive Approximation Register Analog to Digital Converter
SFDR	Spurious-Free Dynamic Range
SNDR	Signal-to-noise + Distortion Ratio
SNR	Signal-to-Noise Ratio
USA	United States of America
USD	US Dollar

Chapter 1 Introduction

1.1 Introduction

With the development of science and engineering, IT (information technology) is changing the modern lifestyle. In particular, wireless communication technology has revolutionized the way people communicate and acquire knowledge. It is ubiquitously employed in personal mobile products, and it is also gradually applied in healthcare appliances and services. Implementations of wireless technologies in wearable and portable healthcare devices have become some of the hottest topics in the intersection of electronic and medical. A vast array of products and applications such as wireless step monitors, wearable blood oxygen saturation monitors and heart rate detectors, etc., which often accompanied by some applets on smart phones/tablets have been employed to diagnose the epilepsy, muscle problems, heart diseases, etc. With these healthcare devices, both patients and hospitals may significantly reduce their expenses, for example, the United States saved around 1.9 trillion USD every year which might otherwise be spent on chronic diseases and their management in the past half-decade [1]. This huge potential of resource saving is attracting more and more researchers to work on this area. Among all the applications in this area, implantable medical device is one of the most promising outcome. Implantable medical device is normally implanted and operated within human body in order to diagnose diseases or process treatments, and it can be more focused on the trauma of a patient.

In the past half century, one of the most widely used implantable medical devices is microelectronic biosensor. It has a large amount of applications such as measurement

devices on heart-rate, ECG, EEG, temperature, oxygen saturation of blood and neuro-signal [2], etc.; also, some therapy devices, for example, with a bi-directional telemetry developed by NASA [3], Siemens-Pacesetter Inc., Sylmar, California implemented a Synchrony pacemaker and obtained approval from Food and Drug Administration (FDA) for general marketing in August 1989. Around a decade later, a deep-brain stimulator [4] was developed to send electrical impulses to specific brain nuclei for the treatment of movement and affective disorders. Now, with the advancements of science and technology, clinical markets require the implantable medical devices to have higher efficiencies and smaller form factors. Two things, therefore, become critical under such a demand: one is to achieve a high speed wireless data transmission channel between implants (in-body devices) and transceivers (off-body devices) with a high accuracy; the other one is to create a high efficiency wireless power recharging channel between implants and transceivers.

In this thesis, we propose a transceiver design of an implantable medical device utilizing inductive coupling coils for power and data transmission. A Class E power amplifier is employed to amplify and transfer power from the transceiver to the internal implanted device. And then by designing a Load Shift Keying (LSK) demodulator --- a special scheme of Amplitude Shift Keying (ASK) which has a higher data recovery efficiency compared to Frequency Shift Keying (FSK) structure for digital signal transmission --- the biology data captured by the implant are transmitted back to the off-body transceiver (external device). The LSK demodulation technique allows power and data transmission through one single inductive link simultaneously. It can work under a variety of modulation indexes and different coding/decoding protocols. Therefore, it can achieve a high data rate

and a high power transfer efficiency. Furthermore, it is also able to scale down the whole microelectronic system in terms of power consumption and volume.

1.2 Medical Implants

A medical implant is a man-made device implanted inside the human body. It is different from a transplant, which is an organ or tissue of natural origin [5]. A medical implant is implanted inside a human body to replace a missing biological structure or rectify a deforming structure of the body and eventually to re-implement the lost functionalities or to compensate for the abnormalities. Implants are not only passive biomedical materials such as silicone or apatite, they can also be active devices that contain electronic circuits so that to help people actively fulfil some particular functionalities. And these active devices are normally called implantable devices. One appealing technique for implantable devices is integrated solid-state circuit because of its higher integration density which enables its physical size to be smaller and its power consumption to be lower. Coupled with modern biomaterials, more and more implantable devices are developed with solid-state circuits integrated on them.

1.2.1 Wireless Medical Implantable Devices

In 1889, John Alexander MacWilliam reported his experiment about using electrical impulse to evoke a heart of asystole so that to achieve a rhythm of 60-70 beats per minute in the British Medical Journal (BMJ) [6]. Since then, a lot of researchers worked on pacemakers, which is a kind of device that uses electrical stimulation to drive heart beating. A pacemaker is primarily designed to aid a heart to maintain in an adequate beating rate

for a patient whose natural heart rate is not fast enough or there is disease in the heart's natural electrical conduction system [7]. In 1958, the first implantable artificial cardiac pacemaker was successfully implanted into Arne Larsson who is the world's first implantable pacemaker patient through thoracotomy at the Karolinska Institute in Solna, Sweden [8]. Recently，with wireless technique, modern pacemakers can inter-transfer data with the off-body device, and also be recharged or powered wirelessly.

Figure 1.1 and Figure 1.2 show us a couple of implant examples that have been clinically used. Both of them have been commercially launched in the healthcare market. The retinal implant as shown in Figure 1.1 was approved by the FDA in 2013, which was designed to enhance vision in patients who have been progressively blinded by the condition retinitis pigmentosa [9]. A miniature video camera is mounted on a patient's glasses to capture images, then the images are converted into electrical pulses and transmitted into the electrode array implanted on the retina of the patient through wireless channels. The electrode array will then stimulate the healthy cells on the retina and eventually create visual patterns in the brain [10]. Figure 1.2 shows a middle ear implantable device which has been approved by both European CE-mark in 1998 and FDA in 2000 [11] [12] [13]. Similar to the retinal implant, a microphone and an audio processor are worn by a patient on his or her ear to capture sounds, and then the sounds are converted into electrical signals and transmitted to a device implanted in the middle ear of the patient through wireless channels. The implanted device will transfer "the sounds" to the inner ear where auditory neurons will be activated to generate the sense of hearing [14]. Both of these two implantable devices are capable of being wirelessly recharged and transferring data.

Figure 1.1 Retinal implant with wireless interface [10]

Figure 1.2 Middle ear implantable device powered via inductive couple coils [15]

It is expected that more and more sophisticated implantable devices to be developed and launched in the healthcare market. These devices may need more power supply and wider bandwidth communication channel; meanwhile, to be integrated within a tiny package and should be easily implanted and maintained inside the human body. The requirements of wireless recharging and data transfer are therefore becoming more critical.

1.2.2 Wireless Telemetry

Telemetry generally means a device or the technique that fulfills automatic measurement and data transmission from remote locations or inaccessible sources through wire, radio or other methods, etc. [16]. The telemetry instrumentations that are employed in implantable medical devices are called biomedical telemetries or biotelemetries. With biomedical telemetries, the off-body devices of implantable medical devices can transmit data and power to the implanted internal devices. This transmission of data can be unidirectional or bidirectional. Unidirectional biotelemetries can be divided into two types: one is to transmit the biological data from the implanted device to the external body device where the data will be processed and monitored, such as electrocardiograph (ECG), neural signal or blood oxygen saturation; the other is to transmit commanding data or manipulating data from the external body devices to the implanted device so that to configure the internal device or control the internal device, for example, to stimulate the body tissue in a desired pattern [17] [18]. Normally, the biotelemetry which is used to transmit data is called data telemetry, whereas, the one which is used to transmit power is called power telemetry.

Telemetry has become a research topic for more than a century. How to wirelessly transmit power and data in a high efficiency is still challenging researchers. Especially, some applications (e.g. implants) even pose additional constraints on form factors and this increases the difficulty of research and development. At the same time, technology on biosensors are also becoming more advanced, which result in that higher and higher communication rate to be achieved between the external body device and the internal implanted device. All these requirements bring about higher difficulties in designing both

the power link and the data link. In the next section we will discuss some general requirements regarding the implantable medical devices.

1.2.3 Requirements of Wireless Implantable Medical Devices

Surgeries and some particular diseases require that the implantable medical devices to be as small as possible. For example, retinal implants and some cochlear implants are expected to be less than one centimeter in size. Some particular devices that are designed to process disease cells or to flow through the human circulatory system should be even smaller. If a medical device is similar to a blood cell in size (in couple of micro-meters), blood vessels can take the medical device to almost everywhere of a human body to cure diseases. Therefore, in modern micro-electronics research, it is expected to scale down the implantable device in physical size by a few orders of magnitudes.

A pivotal problem of designing such a tiny wireless implantable electronic device is to ensure enough power supply while the device is tiny. As we know, the power sources normally provide less power supply when its size is reduced. Another problem is that the micro-electronic devices are required to communicate wirelessly with external devices in order to transmit and receive biosignals and commands. Similar to the power source, antennas or inductive coils also perform worse when their physical sizes are diminished. Moreover, when a micro-electronic device is implanted inside a human body, the human tissue surrounding the device will reduce the inductance or radiation of the inductive coils or antennas. Hence, signal penetration through human tissue becomes the third problem in designing an implantable electronic device, which dictates that the device have to work in

a proper frequency and with enough power density. Therefore, there is a trade-off in designing implantable devices between size and power/data transmission.

1.2.4 Power Link of Implantable Devices

Since implantable micro-electronic devices are designed for specific diseases, the requirements on power also vary from application to application. Normally, devices with a higher data communication rate such as multi-channel neural recorders require relatively higher power density to support the wireless data link. Some other implantable devices, for instance, the retinal implants or the cochlear implants may consume a very large amounts of current in order to stimulate the target nerves, and therefore they consume even more power.

Table 1.1 lists the range of power consumptions of different implantable devices regarding the range of data rates in the former published research reports. The contents in this table are adapted from [19]. Even though different applications of implantable devices require different amounts of power, a trend can still be observed from the table. In Table 1.1, we can find that devices with higher data communication rates usually consume more power. It also can be seen in Table 1.1 that most of the devices or systems consume about 1 mW, and there are only three devices that consume less than 10^{-1} mW. Also most of the devices are in one centimeter size scale. And for a smaller device, its power consumption also tends to be lower.

Table 1.1 Power and data transmit status from recent research reports

	Data Rate (Mbps)			
Power (mW)	$10^{-3} – 10^{-2}$	$10^{-2} – 10^{0}$	$10^{0} – 10^{2}$	$10^{2} – 10^{3}$
10^{2} - 10^{3}			Emira 04 Khorram 05	Aytur 06
10^{1} - 10^{2}		Choi 03 Parramon 06 Cojocaru 06 Verma 05	Dong 05 Ryckaert 06	
10^{0} - 10^{1}	Philp 04 Peiris 05 Solzbacher 07	Najafi 98 Melly 01 Molnar 04 Jarvinen 05 Chen 06 Dawson 07	Daly06	
10^{-1} - 10^{0}	Otis 05	Cook 06 Dawson 09 Guermandi 07	Ghovanloo 04 Sawan 05	
$10^{-2} – 10^{-1}$		Pletercher 07 Pletercher 09 Bashirullah 09		

Nowadays, researchers are very interested in designing ultra-low power consumption circuits for implantable devices by optimizing analog circuits. The idea is to improve the analog circuit performance through different approaches such as high integration density, integrating fewer components and balancing different trade-offs, etc. as well as reducing the entire circuit power consumption. On the other hand, in digital circuit design, researchers are also attempting to miniaturize the whole circuit by lowering the data communication rate through better algorithms [20]. Recently, a lot of researchers have published studies on devices and systems with ultra-low power consumption [19]. They reported a large array of implantable devices that may consume from 10s to 100s of nW

through optimized circuit design and advance fabrication techniques. For example, in [21], the author reported a system with its amplifier, band-pass filter, and SAR-ADC integrated in a single chip and consumes just 450 nW. In fact, there are also some implantable devices which do not need to transmit data which may consume even less power.

To deliver enough energy to the implanted internal device from the external device as discussed above, many methods have been studied, for example, electro-magnetic wave, pure magnetic field, light or even sound. We will briefly analyze them below.

Radio frequency (RF) is a particular kind of electromagnetic wave with frequencies lies in a range of 3 kHz to 300 GHz [22]. It is widely used in wireless telemetries for industry applications, it can also be found in satellites, mobile phones, televisions and even radar systems. It is actually one of the most common and the most widely utilized technique to achieve wireless power and data transmission. However, because of its high frequency, RF may cause body tissue damage, e.g. ionizing tissue [23], it is rarely used in implantable device researches. In addition, radio frequency can be significantly attenuated when it passes through the human body tissue.

Another medium that is used to transmit signals is light, which is quite common in navigation applications. Sailors use a series of flash to communicate with each other from remote locations. In telemetry studies, researchers employ laser or diode to emit light from a source device, and then harvest and convert the optical signal into energy or data with a receiver device. One limitation of optical transmission is that the substance between the source device and the receiver device may block or attenuate the optical signal. To penetrate the tissues of human body, researchers also attempted to use light of different

wavelengths, e.g. infrared light to implement the optical link [24]. In [25], light was used to penetrate cornea and lens of a patient to transmit power and data for a retinal prosthesis implant. However, long time exposure under strong light may result in fatigue or even damage to human tissue.

One more technique which is used to transfer energy is acoustic wave. It is a commonly employed method in industry applications, especially in submarine applications. The reason behind is that other media source can be absorbed under water, yet sound wave can propagate faraway. However, with sound wave, the achievable data rate is very low. Hence, in implantable devices, researchers are attracted more by some media source such as inductive link which has no absorption issue and can also accomplish high data rate.

Inductive link is a kind of media source to implement telemetry, especially for biotelemetry. By placing two coupled coils in a proper distance, the coupling magnetic field generated in one coil will be transformed into electric current in the other coil. Then energy and data will be inter-transmitted between two coils simultaneously. Inductive link is one of the most widely used techniques to accomplish energy and data transmission in implantable devices. Compare with other media sources, inductive link can achieve a very high power transmission efficiency. Furthermore, data signal can also be transmitted through different modulation methods in an inductive link with power carrier signal. One critical limitation of the inductive link is its limited coil distance. Large distance may cause the transmission efficiency to greatly decrease, which means the external body inductive coil has to be placed in a proper distance (normally one to few centimeters) from the implanted inductive coil.

1.2.5 Data Link of Implantable Devices

For centuries, scientists were interested in transmitting data or signals into the bodies of living beings. A century ago, a series of experiments were conducted by Maurey to record the bird's muscle movements, in which a flying bird was studied by having wires attached on it and a hose lead to a smoked drum [26]. These experiments boosted most of the data transmission topics till even today for implantable device research. It is obvious that using wire is not a good choice for implantable devices. Not to mention that the wires will limited the movements of a human body; the wires penetrating skin surface can also easily cause skin infections. Furthermore, friction of the percutaneous wires may also lead to the muscle tissue damage. Hence, there are few researchers working on percutaneous wires that are used to connect implantable devices for clinical patients.

Advance of modern physical science enables engineering researchers to utilize various methods to implement data transmission without contact cables or wires. For implantable medical devices, similar to the power transmission, there are also several techniques including magnetic field, electro-magnetic wave and even light, etc. that have been employed or under research investigation for data links. Inductive link, which is a typical application of electro-magnetic induction has been widely used for implantable implementations, for example, the aforementioned mid-ear implantable device. The implanted device (receiver) and the external device (transceiver) communicate across the patient's skin in a distance of few centimeters' range. The transceiver and the receiver cannot be separated too far away because the further the distance between the transceiver coil and the receiver coil the more attenuation the electro-magnetic wave will experience.

On the contrary, shorter distance can help to enhance the strength of the inductive coupling. Recently, some of the implantable devices are designed to transmit power and data simultaneously through one coupling coil pair [27] [28]. However, for this type of designs or applications, the carrier frequencies cannot exceed tens of MHz because human tissue may absorb the high frequency signals and may also be damaged by them [29]. The most common frequency for these devices is 13.56 MHz. Meanwhile, the bandwidth of the transmitted signals may also be relatively small. For some particular implementations, which are not critical in data rate, this single coil pair solution is the best choice, because it can achieve high power efficiency and it takes less space than solutions of multi antennas/coil pairs.

There are also some researchers exploring the capability of radio frequency (RF) in transmitting a higher data rate because the carrier frequencies of RF signals can be hundreds of MHz or even higher as GHz. Another merit of RF technique is that the distance between transceiver and receiver can be meters away which is very competitive compared to inductive coupling coils. In [30], the author just employed RF as the data transmission method to fulfill the high data rate requirements of a neural recording. But also, as we have mentioned, because of the high carrier frequency, RF may be harmful to human body, and it is quite difficult to obtain approval from medical device regulation agency. For instance, the bandwidth is limited to 300 kHz for MICS (Medical Implant Communication Services) by FCC (Federal Communication Committee) standards in the USA. Hence, a lot of researchers are still concentrating on the inductive link systems. It can be found that quite many publications about the innovations on the inductive link were reported such as [31] - [34].

For modulation scheme of inductive links, considering the generic data transmission, frequency modulation is widely used for analog signal transmission because it is resilient to noise. Meanwhile, it can also be found that several different modulation schemes are used for inductive links, such as amplitude-shift keying (ASK) and phase-shift keying (PSK) are mostly employed for digital signal transmission. Also, considered the power transmission, there were some previous reports by means of multi-channels or multi coil pairs [35] [36] [37] to implement both the data and power transmission. However, including more physical components may result in a bigger implant device. Therefore, for implantable biomedical devices, because of the low power requirement and the limited physical size, the amplitude-shift keying (ASK) scheme is particularly appealing. In addition, an ASK scheme is normally a simple modulation circuit, which has low energy dissipation, adequate modulation index and reasonable signal-to-noise ratio (SNR) [38]. Furthermore, it enables the data transmission and power delivery to be achieved simultaneously.

1.2.6 Architecture of the Proposed Medical Device

Figure 1.3 shows the architecture of the proposed biomedical system which includes the external device and the implantable device. We propose to develop this as a neurosensory system to acquire sub-scalp EEG data so that to provide long-term, neurological health monitoring for epilepsy patients. As can be seen in Figure 1.3, the whole microsystem has two parts. The internal part on the right side in the figure is a microchip which is implanted under the skin of a patient and connected to a well-designed thin electrode array that is also implanted in the body but separated from the microchip. The electrons array is located in

the sub-galeal beneath the patient's scalp yet in the outside of the patient's skull. The other part on the left is the external body device which is a wearable device. It is the so called transceiver which can be a small piece of device integrated with power amplifier, data receiver and signal processor. In this design, the implant device on the right side of the figure is wirelessly powered through the coupling coils by the transceiver on the left. After detecting EEG data from the sub-scalp, the implant device can transmit the biological signal to the transceiver through the same coupling coils. In this thesis, we will concentrate on the transceiver part (the left part of Figure 1.3).

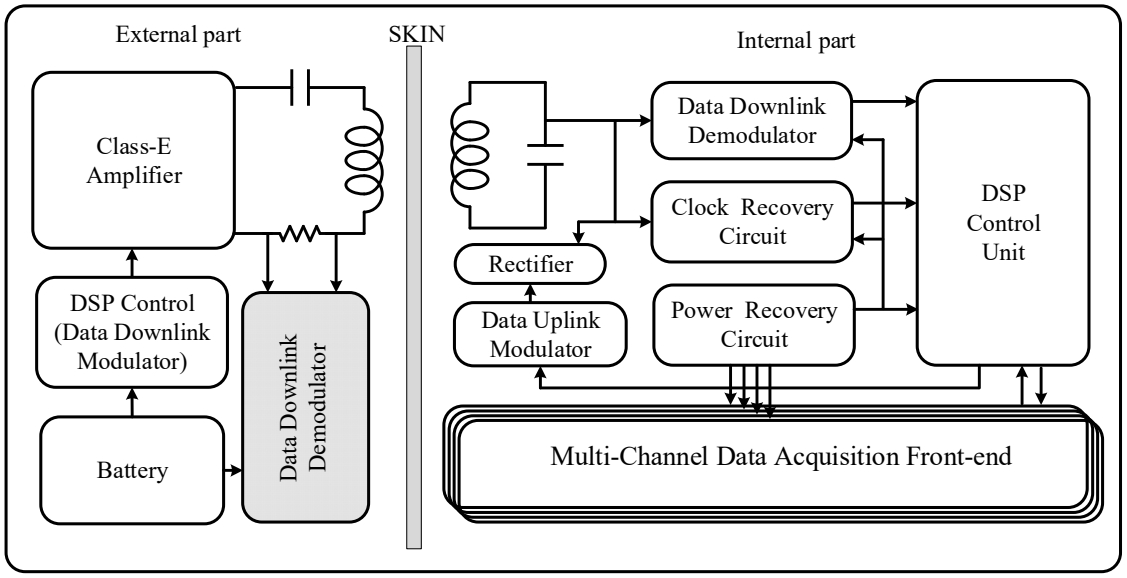

Figure 1.3 Architecture of the proposed implantable device and external device

Based on the discussions above, in the following contents, we will present a transceiver design of the implantable system by means of inductive coupling coils for power and data transmission. An E type power amplifier is employed to amplify and transfer power from the external transceiver to the internal implantable device. At the same time, by designing a load-shift keying (LSK) demodulator --- a special scheme of ASK --- the data signal from the implanted device is transmitted to the external transceiver. The LSK demodulation

technique allows power and data to be transmitted through one single inductive link simultaneously. It can work under a variety of modulation indexes and different coding/decoding protocol. Meanwhile, it enables us to reduce the power consumption and body size of the whole microelectronic system.

Chapter 2 Power Amplifier

This chapter conveys the analysis and design of power amplifiers for inductive data and power transceivers. First, we will discuss different topologies of power amplifiers. Then, state-of-the-art power amplifier designs are reviewed and analyzed. At last, we propose a novel Class-E amplifier for the proposed inductive transceiver device.

2.1 Power Amplifier

2.1.1 Introduction

Considering that the external transceiver part of a biomedical device is normally designed as a wearable/portable equipment so that it can be easily carried around by patients, and battery is normally the best option for its power supply. While, to extend the duration of a battery after a single recharge and also to prolong the lifetime of a battery, power amplifiers are widely employed to overcome the power issue in the external transceiver design. There are several topologies of power amplifiers. Based on the output stages for analog designs, they are categorized as A, B, AB and C, and based on the proportion of each input cycle for switching designs, they are categorized as D and E [39]. The D and E power amplifiers performance is significantly better than A to C [40] - [47]. Class E power amplifiers are generally one single-transistor solution, whereas two or more transistors are commonly required for Class D power amplifier. The transistors in power amplifiers are utilized as switches, which are expected to be non-power consumption components. Theoretically, a Class E power amplifier can achieve peak energy efficiency of 100%, whereas the values of Class A and Class B amplifier are 50% and 78% respectively. [48] reports a Class E

power amplifier design with power efficiency of 96%. Hence, a Class E amplifier is the more advantageous topology compared to the rest types of power amplifiers in terms of power efficiency. Furthermore, to drive a Class E amplifier is also simpler than the other power amplifiers [49]. Therefore, for power amplifications, Class E amplifier is particularly appealing among all the other amplifier architectures, especially for implantable device or short distance wireless communication applications.

2.1.2 Principle of Class E Power Amplifiers

Figure 2.1 shows a typical conventional basic architecture of Class E power amplifiers. As can be found in Figure 2.1, there is an RF choke, a MOS transistor M and a load network that includes two capacitors C_p and C_0 and an inductor L_p. The MOS transistor M is utilized as a switch. Controlled by the driver voltage at a specific work frequency, it will be switched between stages of "on" and "off" regularly. The inductance of RF choke should be large enough such that the DC current can dominate the AC components in the current. Therefore, the RF choke acts as a DC current source. In the load network, the capacitors C_0, C_p and the inductor L_p work together to generate sinusoidal waveforms, and eventually enable the MOS transistor M to be switched between on and off smoothly. And, the current that flows across M during the operations is quite a small value. In this circuit, the load of the circuit is Rp.

As mentioned above, to extend the battery life, we should try to reduce the energy dissipation in the circuit at the utmost. In another word, we need to endeavor to maximize the power efficiency while designing the whole circuit. The power efficiency is a parameter,

which is used to assess the proportion of power that is converted and delivered to the load. Regarding the definition, we can have the equation to calculate power efficiency:

$$\eta = \frac{\text{power that is converted and delivered to the load } R_p}{\text{DC power supply of } V_{cc}}$$

From the equation, it can be found that the ideal efficiency is 100%.

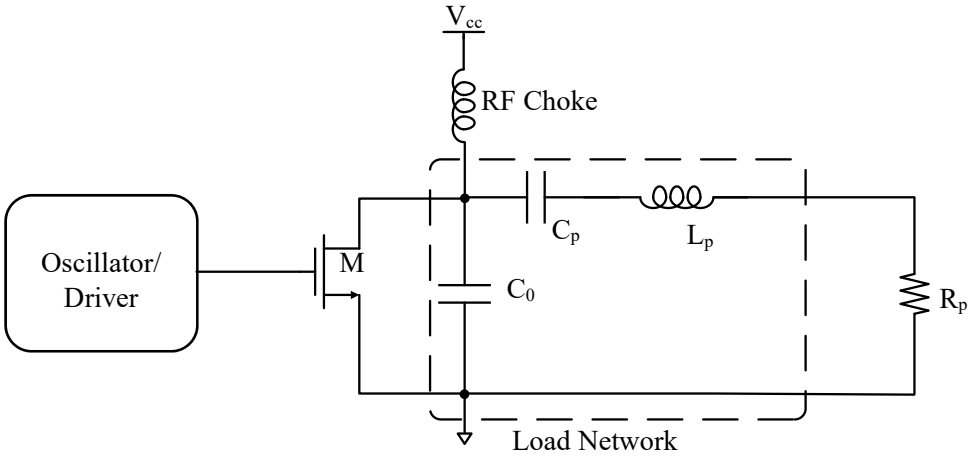

Figure 2.1 Structure of Class E power amplifier

2.1.3 Design Procedure

Since the concept of Class E power amplifier was introduced in 1964 by Ewing [50], there have been a lot of researches published on this type of power amplifier. Some introduces circuits that can support different quality factors, as well as the different duty ratios, and some introduces the analytical solutions for Class E power amplifier [51] [52].

From the previous designs, researchers were attempting to find out how the components affect each other, and what is the optimum setting value for each component, and eventually minimize the switching loss. Ideally, for conventional applications, by

neglecting the parasitic resistance of all the components, the total power that is delivered to the load resistor R_p can be 100%. But, this efficiency can never be achieved in practice. For wireless implantable devices, Class E power amplifiers are also widely employed to amplify and deliver power [53]. However, it can be found that the conventional applications are different from the wireless implantable devices. In the conventional applications, the output power of the circuit is the total power consumption of the load resistor R_p. While, for wireless implantable devices, the delivered power is expected to be the electromagnetic energy generated by the inductor L_p, and the power dissipated in the load resistor R_p should be as small as possible. But the design methods and procedures for the conventional applications are still applicable for the wireless implantable devices, because the optimizing aims are the same, which is to reduce the loss on the MOS transistor switch.

According to the optimizing design procedures introduced in [54], we will initially determine a starting parameter. What we need to consider in designing the circuit including: first, how much power we need to generate and deliver to the inductor L_p in the external device which is denoted as P_L. This is actually a requirement of the implanted device; second, the quality factor of the entire circuit, which is denoted as Q_p is determined by the requirement of the data transfer rate; last, the voltage source that is used to supply the power amplifier is denoted as V_{cc}. This voltage source value is normally the starting parameter. But it is adjustable in case that parameters of P_L and Q_p cannot meet the desired requirements. The power which is dissipated in the load resistor R_p and the power delivered in the inductor L_p can be calculated by

$$P_L = \frac{1}{2} L_p \omega_c |I_p|^2 \quad (2.1)$$

$$P_R = \frac{1}{2} R_p |I_p|^2 \quad (2.2)$$

Where I_P is the current that flow through R_P and L_P. With (2.1) and (2.2) and the quality factor equation of (2.3),

$$Q_P = \frac{P_L}{P_R} \quad (2.3)$$

we can have:

$$Q_p = \frac{L_p \omega_c}{R_p} \quad (2.4)$$

Then, P_R, which is the power consumed by R_P can be calculated by:

$$P_R = \frac{V_{cc}^2}{k R_p} \quad (2.5)$$

Where k is a constant parameter that is determined by Q_P and the duty ratio. Combining the equation above, we can derive the equation of L_P:

$$L_p = \frac{Q^2 V_{cc}^2}{k P_L \omega_C} \quad (2.6)$$

The equation of R_p is also achievable given Q_p,

$$R_p = \frac{L_p \omega_c}{Q_p} \quad (2.7)$$

After the calculation of the resistor R_p and the inductor L_p, we can then determine the remaining parameters of the whole circuit, for example, the values of the capacitors. However, considering the parasitic capacitance, we connected more capacitors and inductors in the circuit so that the values can be adjustable.

2.1.4 The Proposed Class E Amplifier

In this research, the power amplifier is required to deliver 1 mW to the secondary coil. And the power carrier frequency should be from 10 to 20 MHz. Based on these requirements, we designed the circuit as shown in Figure 2.2. The coil on the transceiver side is 19.8 mm and the size of the secondary side is 9.3 mm as shown in Figure 2.3 and the transceiver PCB prototype is shown in Figure 2.4. Measurement results will be discussed in chapter 7.

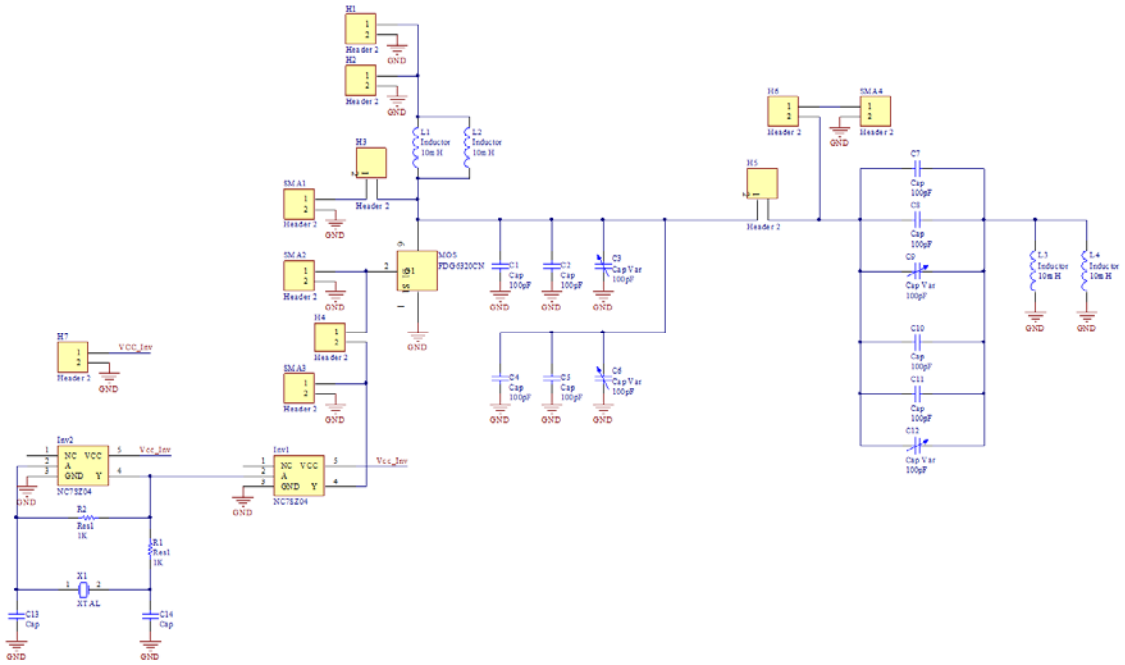

Figure 2.2 Class E amplifier circuit

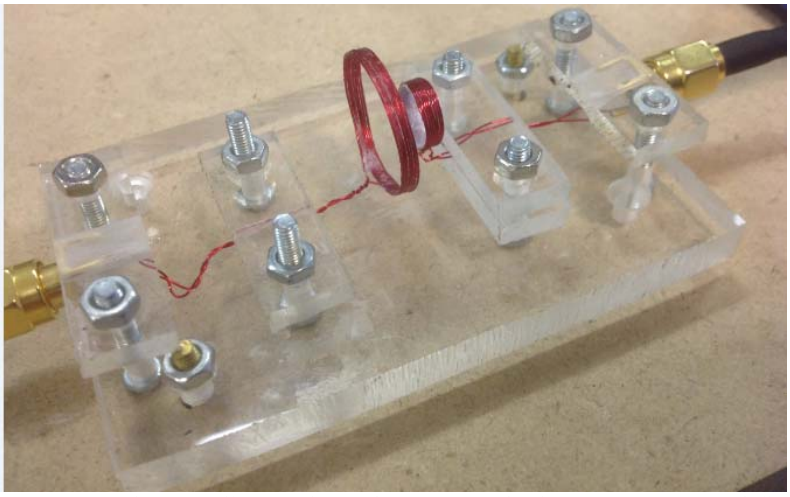

Figure 2.3 The coupling coils of the proposed Class E power amplifier

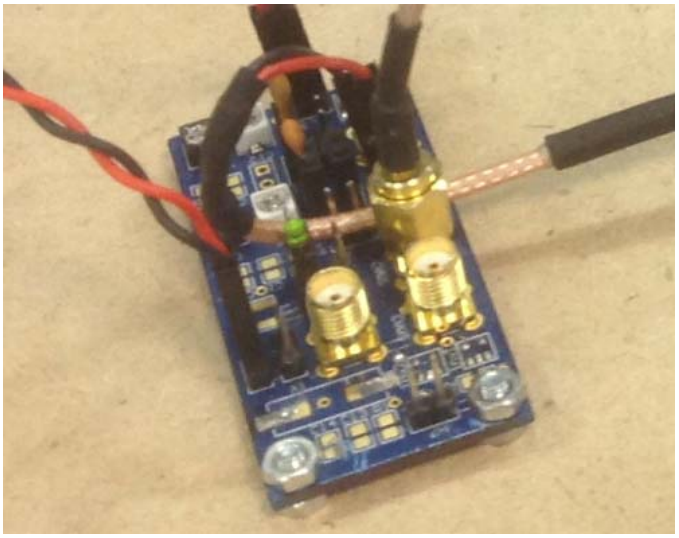

Figure 2.4 Proposed Class E amplifier prototype

Chapter 3 Load Shift Keying

3.1 Introduction

It is commonly seen that inductive coupling coils are employed to power implanted devices. However, most of the coupling coils suffer from transmitting enough power because of their limited physical sizes. Hence, to mitigate this limitation, Load Shift Keying (LSK) modulation scheme is adopted because it can support small modulation index signals which enhance the power transfer efficiency.

LSK, is also called "reflectance modulation" [55] [56], which is a particular implementation of passive impedance reflection, and also a primary method used in designing implantable medical devices for retrieving biological data. LSK is also considered as a special topology of amplitude-shift keying (ASK) in terms of the circuit design [56]. As we have discussed, the LSK is a bi-functional modulation technique, which allows transmissions of power and data to be accomplished simultaneously through one single inductive coupling link. A common inductive coupling link includes two basic inductive coil components. One property of an inductive coupling link is that when the loading impedance of one side is changed, the loading impedance in the coupled side reflects the change. This is actually the change of the reflected impedance. LSK modulation topology is just an application of this property. By detecting the reflected impedance changes occurred in the primary side, a LSK modulation device is able to analyze the loading impedance changes that happened in the secondary side, and eventually decode the signal. This signal is just the digital data transmitted by the secondary circuit. This working

scheme is different from a common topology of ASK scheme because in a common ASK modulation device the power efficiency may suffer more decrease when data is also transmitted in the same inductive link. For example, in the common ASK design of [57], the primary side was used to detect the amplitude changes of the input waveform, which was a reflection against the resonant capacitance changes or the inductance changes appeared on the secondary coil. However, while the primary side was working on the reflection, the changes from the secondary coil might conduct a resonant frequency change in the primary side, and this change could greatly affect the power transmission efficiency.

To realize the LSK modulation topology, a particular functional circuit is required to modulate the load impedance changes on the secondary side related to the transmitted digital data. This modulating procedure should affect as small as possible on the resonant capacitance or the inductance of the secondary side circuit; otherwise, the power transmission from the primary side to the secondary side will be affected. In this particular functional circuit design, the AC loading impedance on the secondary side is determined by both the inductive power recovery circuit and the DC loading impedance [58]. Therefore, through varying the power recovery circuit appropriately, which may adjust the DC load impedance of this circuit to a desire value, the AC loading impedance can be eventually modulated. In practice, a data-driven switch will be adopted to configure the circuit from one stage to another, and to change the DC loading impedance from one value to another. This configuration can eventually shift the AC loading impedance between two values according to the binary digital data. When the voltage potential crossing the primary coil reflects the AC loading impedance changes on its own amplitude, the changes will be recognized as data bits “0” and “1”. Through such a procedure, the data signal is thus

transmitted from the secondary side circuit to the primary side circuit. In this research, we focus on the development of the transceiver device, which is the primary side circuit. To test the entire working procedure, we utilized an FPGA to simulate the AC load impedance changes.

Even though the LSK is one of the most common ways to implement power and data transmission link, to design and realize a LSK with a high efficiency and high-speed transmission is still a challenging task.

The first challenge is to make sure that the waveform amplitude on the primary side circuit (the external body circuit) can reflect an immediate and distinct change when the AC load impedance on the secondary side circuit (the implanted device circuit) changes. To overcome this challenge, the AC load impedance change on the secondary coil have to be distinguishable as much as possible, which means the total amount of the load value should be changed as large as possible. Because the maximum achievable change on the load impedance is to reduce the amount from an initial value to zero, many reported designs chose either to shut down the load completely which means to keep the circuit open or to bypass the load which means to short the circuit. However, both of these two methods may disturb the secondary circuit on the resonance, and eventually reduce the total efficiency of power transmission from the primary circuit to the secondary circuit.

The second challenge is to achieve a high data rate. In the former discussed working procedure of LSK topology, to achieve a reliable recovery of the data signal on the primary circuit, the power carrier frequency ought to be separated away from the data bandwidth as much as possible. Meanwhile, the power carrier frequency cannot be too high as

discussed in chapter 1, because the high frequency signals can be absorbed by human tissue and may result in cell damage [59]. Hence, the carrier frequency have to be set to less than tens of MHz, for example, the most commonly used carrier frequency is 13.56MHz. This may ultimately affect the data rate of a LSK link by limiting it to a few Mbps. The achievable ratio of data rate to carrier frequency is normally very small.

The last challenge is to reduce the sensitivity of a LSK data link against the interferences of the surrounding environment. The media source that a LSK data link applied is electromagnetic wave. Hence, when the relative position or the orientation of the inductive coupling coils is changed, the density of the electromagnetic wave may also be modified, and this will lead to reduction on the efficiency of the wireless link. At the same time, other electronic devices around may also emit electromagnetic wave, and the unresolved electromagnetic wave may also affect a LSK inductive link by generating some unexpected amplitude variations on the power carrier waveform. All these changes or interferences may substantially reduce the demodulation accuracy of the LSK link. And it could be even more severe when the design is required to achieve a higher power transmission efficiency because this means the modulation index have to be small.

3.2 Principle of LSK [58]

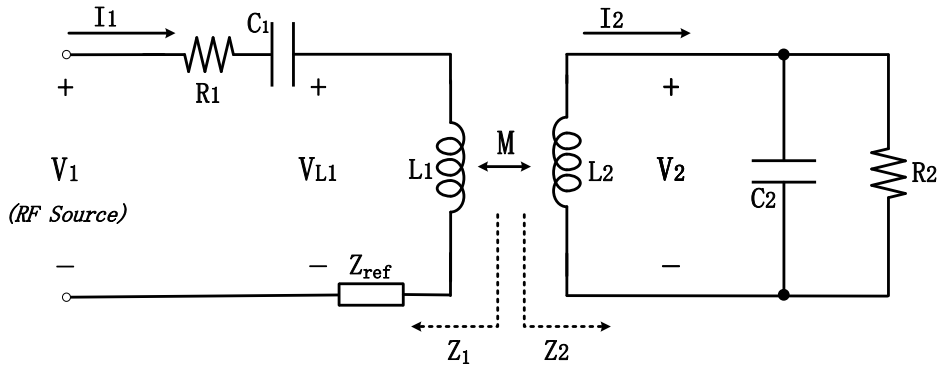

Figure 3.1 Circuit for analysis of LSK principle

Figure 3.1 shows the circuit, which is used to analyze the principle of LSK. It can be seen in the figure that M is the mutual inductance of the inductive coils; Z_2 is the secondary coil load impedance and reflected impedance in the primary side is Z_{ref}. If we define the RF power carrier's angular frequency as ω, according to [58] then we can have:

$$Z_{ref} = \frac{\omega^2 M^2}{Z_2} \tag{3.1}$$

And the primary coil load impedance is:

$$Z_1 = \frac{V_1}{I_1} = R_1 + Z_{ref} + j\left(\omega L_1 - \frac{1}{\omega C_1}\right) \tag{3.2}$$

If we take L_2 as a voltage source V_2, and the impedance in series with L_2 is $j\omega L_2$. Then we can calculate the secondary coil's impedance by the following equation:

$$\begin{aligned} Z_2 = \frac{V_2}{I_2} &= j\omega L_2 + \frac{1}{\left(j\omega C_2 + \frac{1}{R_2}\right)} \\ &= \frac{R_2}{1+\omega^2 R_2^2 C_2^2} + j\left(\omega L_2 - \frac{\omega C_2 R_2^2}{1+\omega^2 R_2^2 C_2^2}\right) \end{aligned} \tag{3.3}$$

As can be seen, both of the two circuits in the primary and the secondary sides work in frequency ω, which is a common resonant frequency. Therefore, if the imaginary parts of the impedance for both Z_1 and Z_2 are equal to zero, we can have:

$$\omega L_2 - \frac{\omega C_2 R_2^2}{1+\omega^2 R_2^2 C_2^2} = 0 \tag{3.4}$$

$$C_2^2(\omega^2 R_2^2 L_2) - C_2(R_2^2) + L_2 = 0 \tag{3.5}$$

With (3.5) and (3.3), we obtain:

$$Z_2 = \frac{R_2}{1+\omega^2 R_2^2 C_2^2} = \frac{L_2}{R_2 C_2} \tag{3.6}$$

According to [60], the mutual inductance can be calculate by the following equation:

$$M = k\sqrt{L_1 L_2} \tag{3.7}$$

Where k is the parameter of coupling-coefficient, which is determined by geometrical parameters. Then with the equations above, we can derive Z_1 as:

$$Z_1 = R_1 + \mathrm{k}^2\omega^2 L_1 C_2 R_2 \tag{3.8}$$

If we define V_{L1} as the potential difference between the two terminals of L_1, then,

$$V_{L1} = \frac{\omega Z_1 V_1}{Z_1} = \frac{V_1}{\omega C_1(R_1 + \mathrm{k}^2\omega^2 L_1 C_2 R_2)} \tag{3.9}$$

From the equation, if the resistance of the receiver circuit is changed from R_2 to R'_2, then the voltage V_{L1} will become:

$$V'_{L1} = \frac{V_1}{\omega C_1(R_1 + \mathrm{k}^2\omega^2 L_1 C_2 R'_2)} \tag{3.10}$$

The equation of (3.9) and (3.10) complied with our discussion in the former section. And based on this equation, the LSK modulation is designed in the following section.

3.3 The Proposed LSK Demodulator

Based on the discussion above, a LSK demodulator is designed and portrayed in Figure 3.2. This LSK demodulator is employed in the transceiver device to demodulate the received data from the reflected power carrier signal, process the demodulated signal and finally output a digitized waveform. It can be seen in Figure 3.2 that there are 6 modules in the whole circuit. The demodulator consists of a pre-amplifier (a), an envelope detector (b), a switched-capacitor band-pass filter (c) and an asynchronous 10-bit SAR ADC (d). Figure 3.2(e) and Figure 3.2(f) are two independent modules, which are an FPGA and a signal indicator.

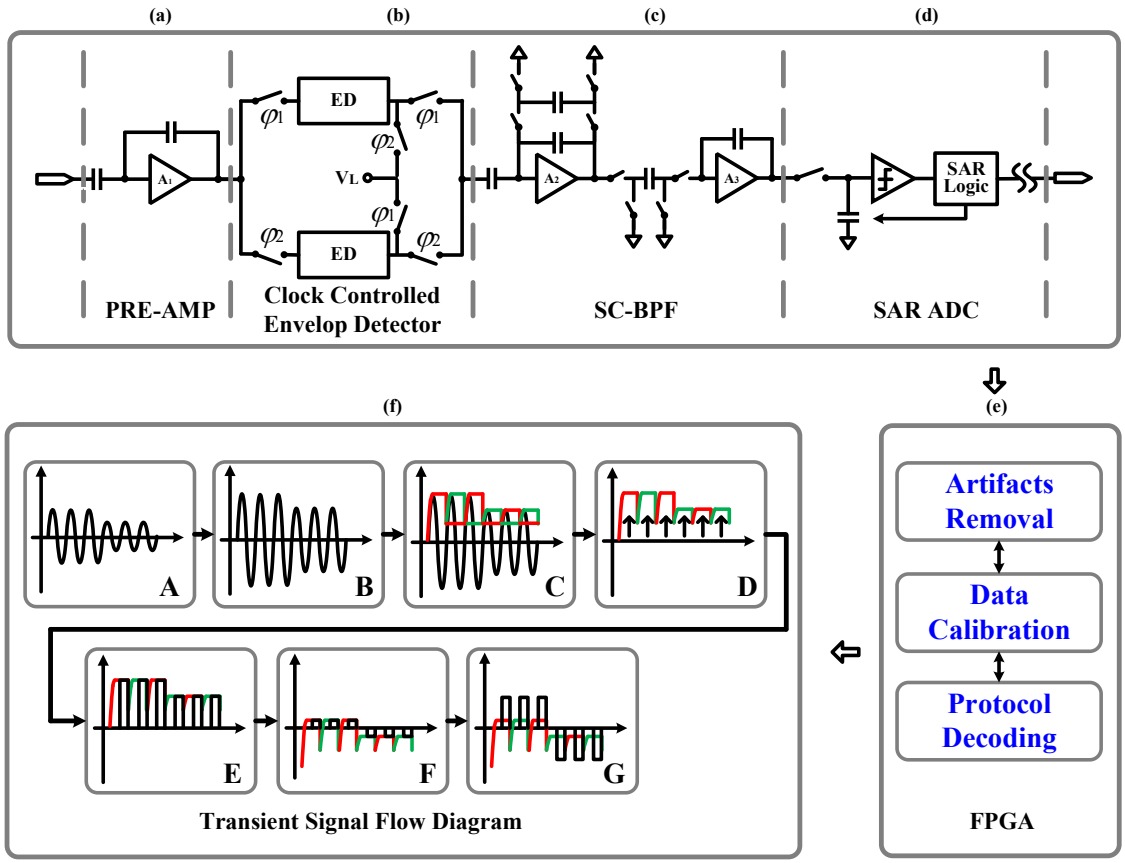

Figure 3.2 LSK demodulator circuit schematic

The pre-amplifier is a two stage Operational Transconductance Amplifier (OTA) that supports 600MHz GBW and serves as a buffer of the signal. Its output is directly fed to the next module, an envelope detector.

The envelope detector is designed to realize the spectral analysis following the pre-amplifier. A simple conventional envelope detector usually includes a diode and a capacitor, which has a diode voltage drop and a trade-off between slew rate and droop rate [61]. Some more practical designs may utilize an op-amp and either a diode or a CMOS transistor with a feedback path so that to reduce the diode voltage drop. However, the limited slew rate of op-amp increases the droop rate of the circuit [61]. And an increased droop rate means a faster speed of discharge. When the input voltage drops very fast, it is very hard for the detector to follow the input signal and accurately detect the peak value. In addition, most of the conventional designs discharge through a RC filter or a current source [61] - [64]. With these discharge branches, ripples may be introduced in the extracted envelope and they require a substantial bit-to-bit interval to avoid decoding errors. As a comparison, the envelope detector design in this thesis inherently suppresses the mentioned defects: as shown in Figure 3.2(b). More details about the design and the working flow will be discussed in chapter 4.

The switched-capacitor band-pass filter is cascaded following the envelope detector to get rid of the large DC component from the extracted envelope and amplify the envelope. This is because that the extracted envelope contains some unresolved interferences, which should be removed subsequently for a reliable data transmission. Detailed content will be discussed in chapter 5

In addition, the 10-bit asynchronous SAR ADC with 10 MHz sampling rate is designed to digitize the output signal of the filter. In this ADC design, both split-capacitor array and V_{CM}-based switching topology are employed to reduce power and area. More discussion can be found in chapter 6.

Compared to the previous research reports, the performance of this design is improved in the following two aspects: firstly, it achieves a higher sensitivity of modulation based on the simulation, which is less than 1% in modulation index without sacrificing the power transmission efficiency. Secondly the multi-phase envelope detector overcomes the trade-off between envelope ripples and the detector speed which increases the achievable data rate significantly [65] [66]. Thirdly, this design is an integrated circuit that included analog and digital components, which can reject some artifacts and interferences while processing and transmitting signals.

The schematic is implemented and simulated in Cadence 6.1. To test the simulation performance of the envelope detector, we generated an input signal in 20 MHz frequency and the modulation index was 1%, the signal was shown in Figure 3.3. This signal was generated by multiplying two signal sources, one was sinusoidal signal with a 20 MHz frequency and 1.0 V amplitude, and it was used to simulate the power carrier signal; the other signal was a square signal in a frequency of 2.5 MHz and amplitudes are 50 mV and 49.5 mV. Figure 3.4 shows the squire signal and it can be found that the modulation index is 1%. The demodulation result is shown in Figure 3.5. The result was captured before SAR ADC module. Measurement result of the prototype will be discussed in chapter 7.

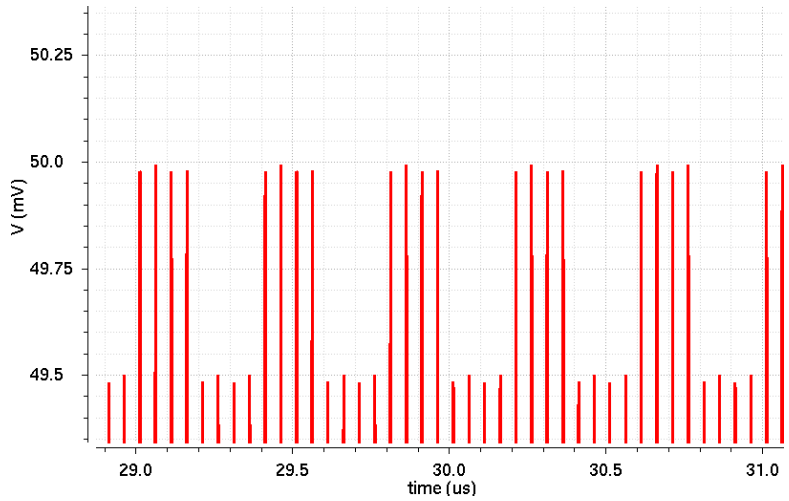

Figure 3.3 Mixed simulation input waveform with modulation index 1%

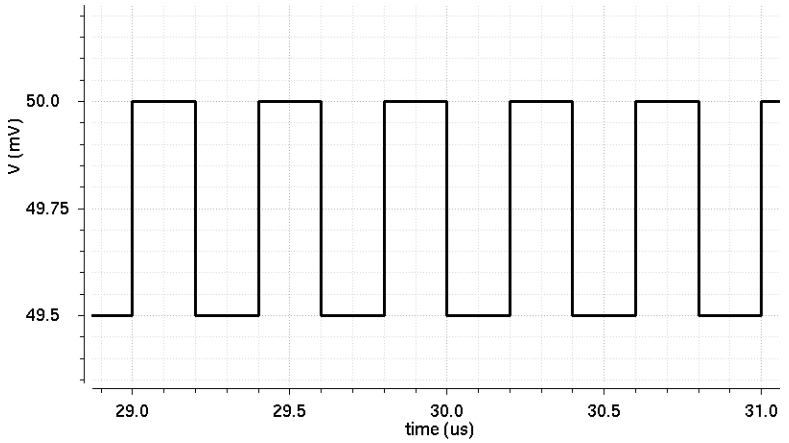

Figure 3.4 Square signal with 1% modulation index

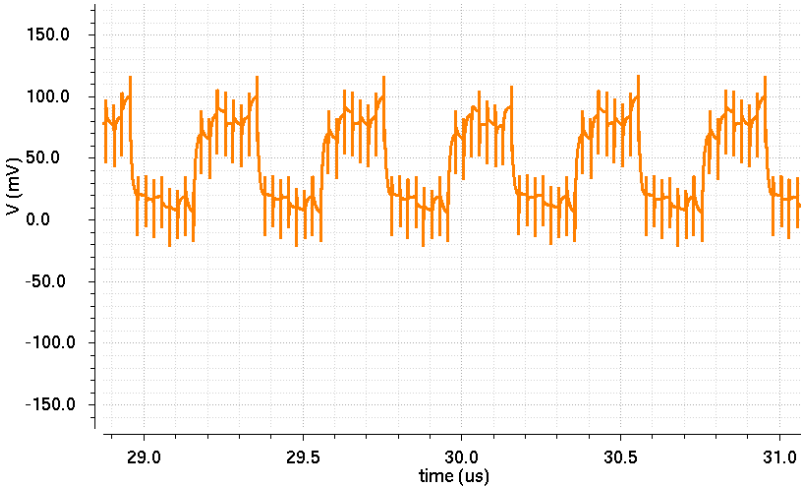

Figure 3.5 Demodulation simulation result of 2.5 MHz signal with 1% modulation index.

Chapter 4 Envelope Detector

4.1 Introduction

Envelope detector is also called peak detector, which is widely utilized as a core component by the transceiver side of a wireless communication link. It is usually employed to build up a closed-loop, which is also called automatic voltage gain circuit [67]. Normally, in analog circuit design, an envelope detector is used to detect either the positive peak value or the negative peak value of a signal, and also to track the values along with the change of time. Figure 4.1 shows the ideal output waveform of a positive envelope detector [68]. In this chapter, we will discuss a few envelope detector designs and the circuit we implemented for this thesis.

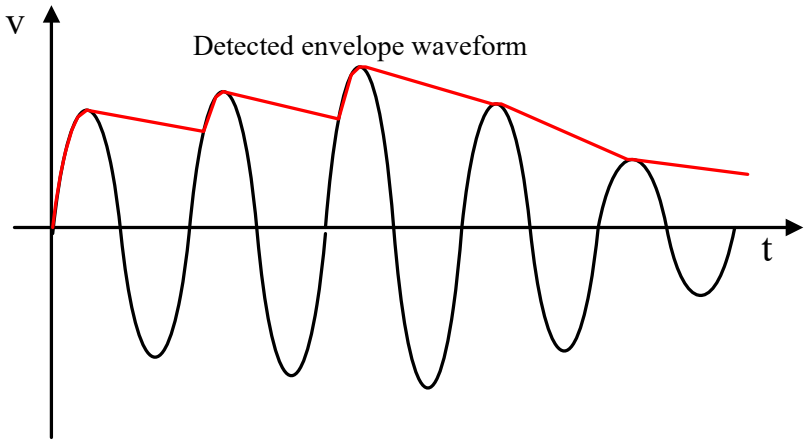

Figure 4.1 Ideal envelope detector output waveform

4.2 Principle of Envelope Detector

4.2.1 Diode Capacitor Envelope Detector

Figure 4.2 shows the principle schematics of a positive envelope detector [69]. From the schematic, this circuit contains two components only, which are a diode and a capacitor. We take this positive envelop detector as an example to illustrate the working principle of the envelop detector. As we can see in Figure 4.2, when the input voltage V_i is greater than the detected value V_p plus the voltage drop across the forward-biased diode D, then the diode D will be "turned on" and current will pass through the diode D and charge the capacitor C_h until the voltage of V_b is equal to or greater than V_a, then the diode will be "turned off" and the capacitor holds the V_b at the maximum value of the input signal, which means the output voltage follows input peak value. Even when V_i drop, the maximum value V_p will still be held at the maximum value of the input signal by capacitor C_h. Hence, if the capacitance of C_h is appropriate, the output signal will the waveform as shown in Figure 4.3.

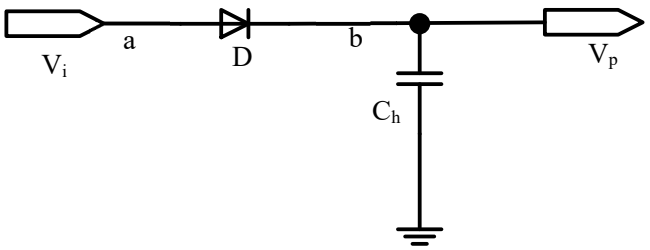

Figure 4.2 Diode capacitor envelope detector

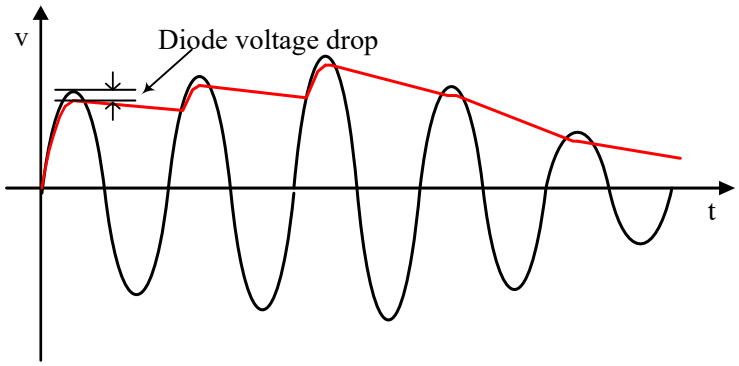

Figure 4.3 Output waveform of diode capacitor envelop detector

By analyzing the circuit shown in Figure 4.2 we can find that there are a few problems with this envelope detector circuit. First, the detected value V_p cannot be accurately equal to the maximum value of the input signal because there is a voltage drop across the diode D. Thus, if the input signal is similar to the diode voltage drop, the circuit may not able to detect the input. Second, the input impedance is almost zero which is too small because the diode is operated in forward-biased condition. Third, normally for a diode, the voltage drop is sensitive to the change of environmental temperature, as well as the current. This may be another severe effect on the accuracy of the envelope detector circuit. Fourth, there is no discharge path in the circuit. If there is a quick and distinct drop happens in the input signal, this envelope detector may not able to follow the drop, as shown in Figure 4.4. Fifth, there is also a tradeoff on how to set up the capacitor value. For a small capacitor, it is easy to discharge, however, hard to hold the peak value. On the contrary, for a big capacitor, it is easy to hold the peak value, however, need longer time to charge up and discharge [69].

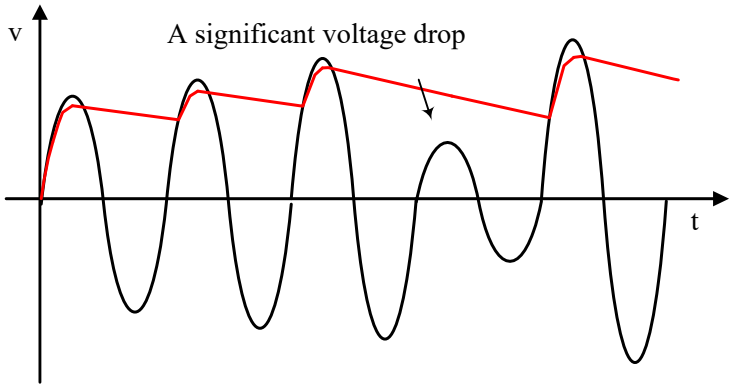

Figure 4.4 Envelope detector output failed to detect a quick and distinct input voltage drop

4.2.2 Detector Using Op-amp

Figure 4.5 shows a positive envelope detector with an op-amp in the loop. In this circuit, the voltage V_p is fed as a feedback to the negative input terminal of an op-amp A. With this configuration, V_p can closely follow the positive input V_i when V_i is larger than negative inputs of the op-amp A, which is V_p. Meanwhile, we can solve the first problem of the diode voltage drop discussed in section 4.2.1. While, when the input voltage V_i drops till less than V_p, which means the op-amp A operates in negative saturation condition, then the diode D is switched off, and the capacitor C_h will hold V_p at the previous maximum value.

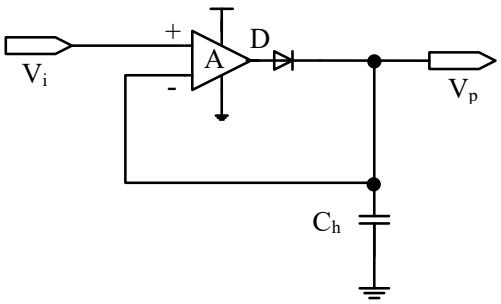

Figure 4.5 Envelope detector with op-amp

Compared with the diode capacitor envelope detector, an extra power supply is required to drive the op-amp A. At the same time, the slew rate of the op-amp will restrict the operation speed of the whole circuit.

4.2.3 Envelope Detector with MOS Transistor

Figure 4.6 demonstrates another envelope detector scheme, which is more practical. Its difference from the scheme shown in Figure 4.2 is that the diode is replaced by a source follower, and a buffer A_2 is cascaded. In this circuit, when the input V_i is greater than V_p, the MOS transistor M will be "turned on", which means the current can flow through M to charge up the capacitor C_h. In contrast, when V_i drops till less than V_p, which means that the negative input of op-amp A_1 is greater than the positive input, the MOS transistor will be "turned off" and the capacitor C_h will hold the output voltage at the former detected peak value. To improve the performance of following a falling input signal, the output is grounded through the resistor R_d to discharge C_h. With this discharge path, the circuit can achieve a higher droop rate. In some designs, the resistor R_d may also be replaced by a current source. Generally, to improve the loading capacity, a buffer A_2 may be implemented to isolate the detected voltage V_p from the following load circuit.

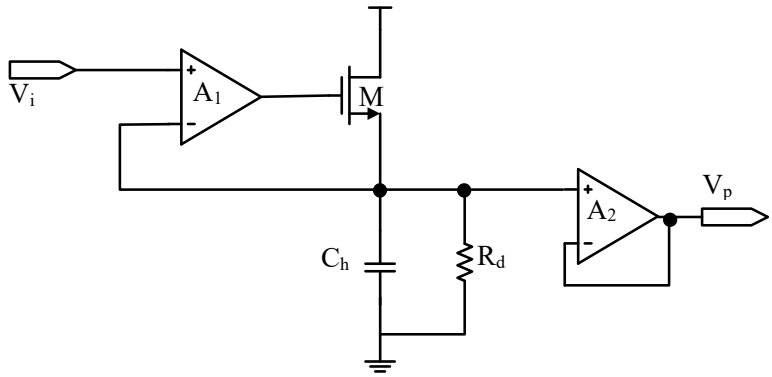

Figure 4.6 Positive envelope detector with MOS transistor and buffer

With this schematic, we can found that the first four problems mentioned in section 4.2.1 are somehow resolved. This circuit can have a more accurate trace in terms of a quick drop of the input signal because there is a special path to discharge the hold capacitor. However, we have to design the discharge path carefully. Because if the droop rate is too high or too low, the detector may not be able to detect the neighboring peak value if the input signal fluctuates too fast.

4.2.4 Positive Peak Detector Using Current Mirror

One more method to enhance the speed and accuracy of an envelope detector is to use a current mirror as the displacement of the diode in Figure 4.6. Figure 4.7 shows the schematic designed by this method. It can be seen that this positive envelope detector consists of a differential amplifier (CMOS transistor M_1 to M_4), a current mirror (CMOS transistor M_5/M_6) and a discharge path (R_d). In this circuit, the function of the differential amplifier is same as the op-amp in section 4.2.3. When V_i is greater than V_p, then transistor M_5 and M_6 will be “turned on”, the current can flow through. The current through transistor M_5 will be mirrored by transistor M6 and charge up the hold capacitor C_h.

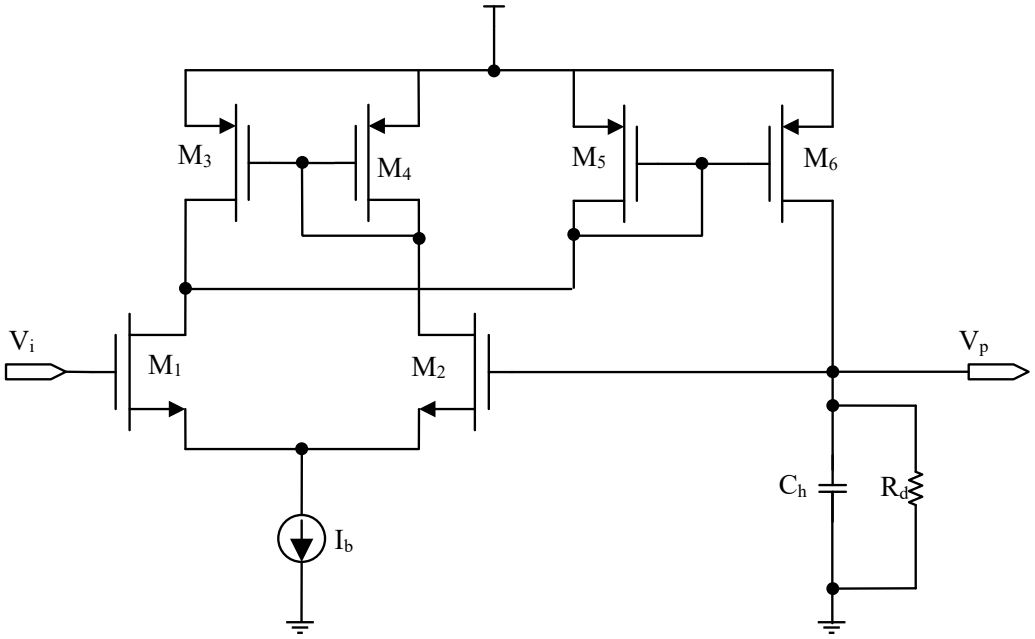

Figure 4.7 Positive envelope detector with current mirror

4.3 The Proposed Envelope Detector

In this work, the envelope detector is applied to accomplish spectral analysis following the pre-amplifier as shown in Figure 3.2. A simple conventional envelope detector as shown in Figure 4.2 is usually a diode-capacitor circuit, which has a diode voltage drop, and the droop rate conflict with the slew rate. Some more practical designs discussed above may utilize an op-amp and a diode or a MOS transistor with a feedback path so that to reduce the diode voltage drop or solve other problems discussed in section 4.2.1. However, the restricted slew rate of the operation amplifier may increase the droop rate. A higher droop rate means the discharge is faster. When the input peak value falls very fast, it may be very hard for the detector to accurately chase the input peak values. Furthermore, many of the conventional designs discharge through a RC filter or a current source [70] - [73] as

discussed in section 4.2.3 - 4.2.4. And this may contribute to the ripples in the output, which may need a substantial bit-to-bit interval to correct the decoding errors. As a comparison, the envelope detector design in this research inherently overcome the mentioned defects.

Firstly, as shown in Figure 4.8, to remove the diode voltage drop, a unidirectional current mirror (M_5 and M_6 or M_{11} and M_{12}) is constructed to replace the ideal diode of a conventional circuit. When the input voltages are greater than the maximum detected values, the OTA will produce a voltage amplitude on the drain and gate of M_5 or M_{11} which will "turn on" the current mirror, the excess current will flow through M_5 or M_{11}, and will be mirrored by M_6 or M_{12} and eventually to charge up the hold capacitor C_{h1}/ C_{h2} and force V_l/V_p to track the peak values of V_i. On the contrary, as V_l or V_p approaches V_i or while the input signal drop till less than the output peak value, the output of OTAs which are built-up by M_1 - M_4 and M_7 - M_{10} will drop to zero or even below, and the current mirrors will be cut off.

Secondly, to overcome the detecting issue due to low droop rate, we employ a configuration of non-overlapping clock and switched-capacitor to control two sets of envelope detectors to work in turns. With such a mechanism, through resetting each peak detector periodically, each envelope detector will be distributed more time to discharge itself. And after the reset, each one will work more precisely. The work procedure is stated here. When S_1 is switched on, then the upper envelope detector (M_7 to M_{12}) will work, and the lower detector (M_1 to M_6) will be reset. This is phase one. In reverse, when S_2 is switched on, then the lower envelope detector (M_1 to M_6) will work, and the upper detector (M_7 to M_{12}) will be reset. This is phase two. The holding capacitors C_{h1} and C_{h2} will work

in turns for these two envelope detectors to hold and output the detected peak values phase by phase. Through this mechanism, both of the two envelope detectors can have enough time to discharge itself, which eventually diminish the ripples and the distortions on the output waveform while the data rate is maintained the same.

We utilize a top clock to generate several non-overlapped clocks through digital standard cells. Also, the output signals of the proposed envelop detector are sampled by the subsequent filter or the ADC with a ¼-delayed sampling clock signal, which allows that the proposed system architecture has enough time for signal processing and settling.

This circuit can suppress the effect of switching glitches with three methods: first, the values of hold capacitors C_{h1} and C_{h2} are larger enough to suppress the switching glitches compared with conventional circuits; second, Switches S_1 and S_2 are controlled by non-overlapping clock signals, and dummy transistors are also used in the switches to remove glitches; third, the input signal has already been amplified before it is sent to the envelop detector, so the effect on amplitude introduced by glitches can be neglected here.

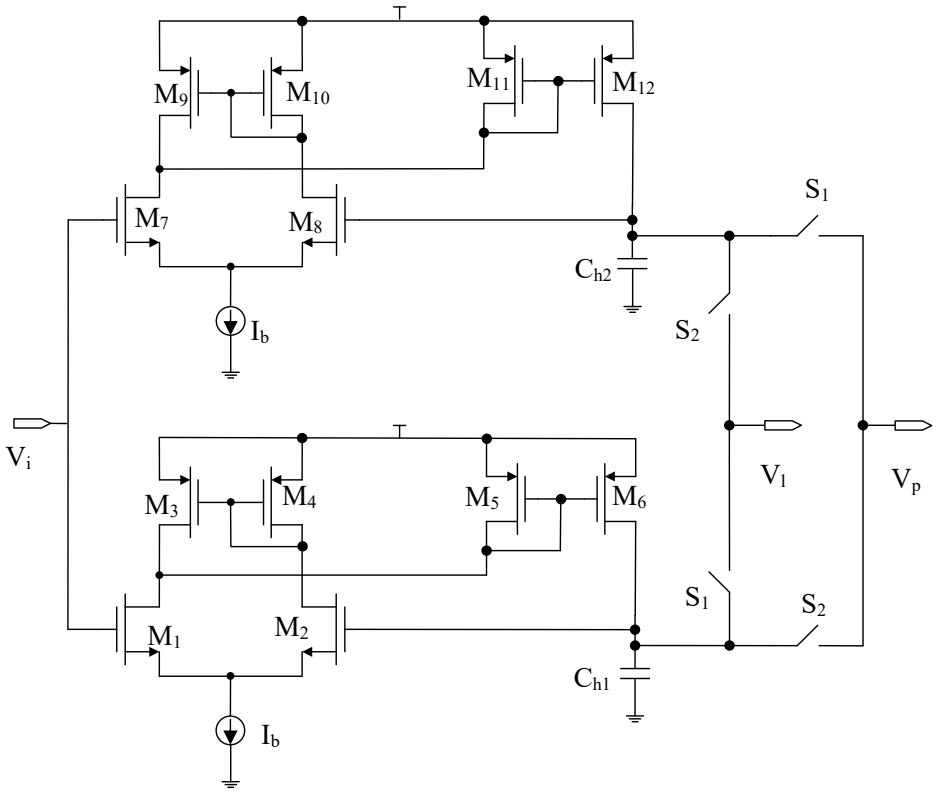

Figure 4.8 Multi-phase envelope detector with current mirror

The schematic is simulated in Cadence 6.1. To test the performance of the envelope detector, we generate an input signal in 20 MHz frequency and 50 mV amplitude as shown in Figure 4.9. This input is a multiplied signal by two sources, one is sinusoidal signal with a 20 MHz frequency and 1 V amplitude, and it is used to simulate the power carrier signal; the other one is a square signal in a frequency of 2.5 MHz and amplitudes of 50 mV and 35 mV. The simulation result is shown in Figure 4.10. Because the bit error rate is generally higher when the transmission signal is in a higher frequency compared with the signal in a lower frequency, so we provided the simulated results of the signal in a high frequency only and take them as reference.

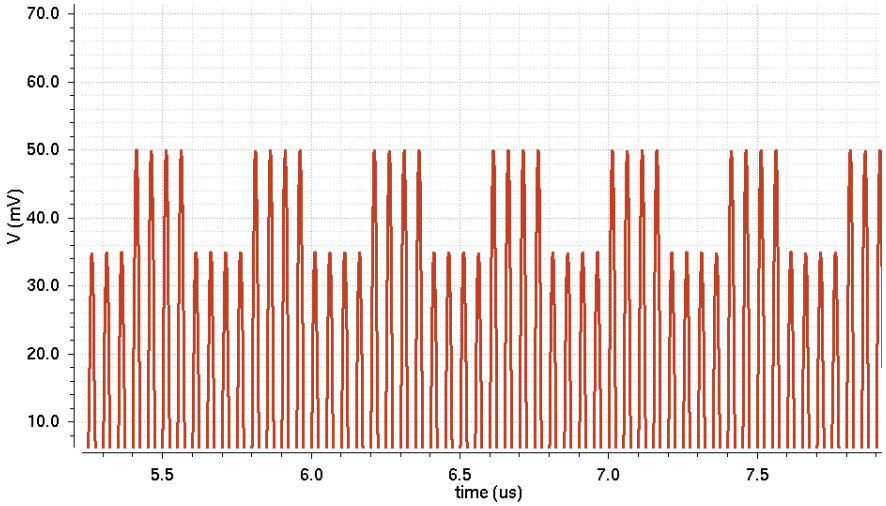

Figure 4.9 Modulated input signal for envelope detector simulation

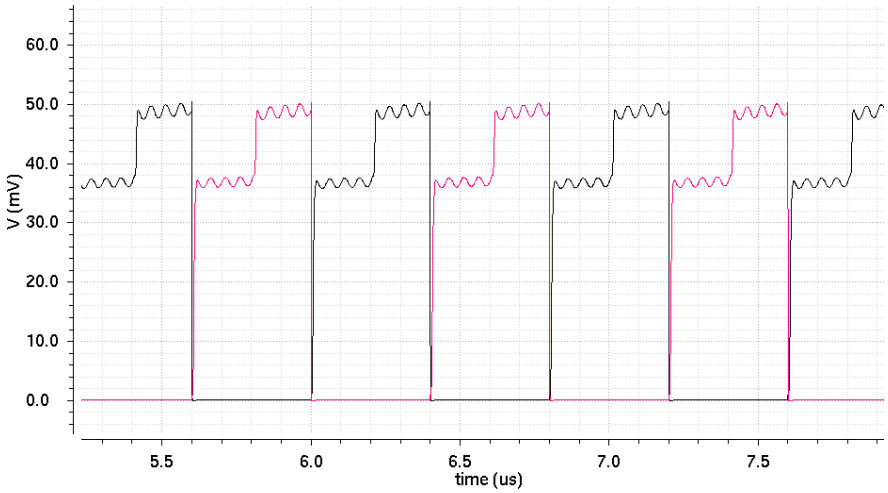

Figure 4.10 Simulate result regarding the input signal of Figure 4.9, two different color plots are the two phase of outputs, which are V_l and V_p in Figure 4.8

It can be seen in Figure 4.10 that there are still some ripples in the output waveform of envelope detector. This is because the designed envelope detector has a very quick discharge path which can help the envelope to follow the input signal closely. It is worthwhile to highlight that this output signal is actually a combination of the outputs from two phases, and they are the black color and the red color in the plots. The reason of having two phases of outputs is that in this research, to enhance the speed of the envelope detector

and also to give the envelope detector enough time to discharge, two sets of envelop detectors are employed to work in alternative phases, as shown in Figure 4.8. Based on such a switching machanism, the output of each set of envelop detector is then plotted in turns in Figure 4.10. Prototype mearsurement will be discussed in chapter 7.

Chapter 5 Filters

5.1 Introduction

Filter is a basic functional module in analog circuit design, which is used to process signals. Filters can be used to block some components of undesired frequencies from the original signals, or to amplify some particular frequency components of the original signal, or both [74]. A low-pass filter can block the components of high-frequencies from the pass-through signal and let low-frequencies components to flow through; a high-pass filter can block the components of low-frequencies from a signal and let the high-frequencies components to flow through. A band-pass filter is a hybrid circuit which is able to block both unwanted high and low frequencies components and let the signals within a certain range of frequencies to go through.

5.2 Principles of Filters

5.2.1 Passive Filters

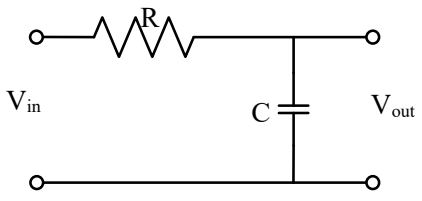

Figure 5.1 RC low-pass filter

Figure 5.1 demonstrates a conventional passive low-pass filter. If we assume that the input signal V_{in} is in high frequencies, then the capacitor C will act as a shorted branch. And the

output V_{out} will be equal to zero. On the contrary, if we assume that the input signal V_{in} is in low frequencies, the capacitor C will act like a huge impedance or even an open circuit. Then the output V_{out} will be approximately equal to V_{in}. From this analysis, we notice that the circuit in Figure 5.1 allows low frequencies signals to pass, and rejects signals of high frequencies. So, it is a low-pass filter. We take this filter as an example to discuss its mathematic module. Based on Figure 5.1, we can have the magnitude equation of the transfer function below:

$$\left|A(j\omega)\right| = \left|\frac{V_{out}}{V_{in}}\right| = \left|\frac{\frac{1}{j\omega C}}{R+\frac{1}{j\omega C}}\right| = \frac{1}{\sqrt{1+\omega^2R^2C^2}} \tag{5.1}$$

From the equation (5.1), it can be seen, when angular frequency ω increases, the magnitude of transfer function of the circuit which is the value of $\left|A(j\omega)\right|$ will drop quickly until zero. This is the reason why only low frequencies signals can pass. Normally, we define f_0 as the half-power frequency, where $f_0 = \omega_0/2\pi$. When the signal is in the half-power frequency, the low-pass magnitude is given by

$$\left|A(\omega_0)\right| = \frac{1}{\sqrt{2}}\left|A\right|_{\max} \tag{5.2}$$

Factor $1/\sqrt{2}$ is also calculated as 3dB. The Figure 5.2 shows the magnitude versus frequency of a low-pass filter.

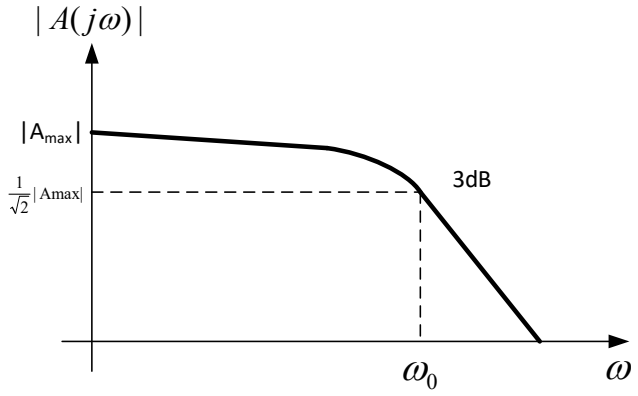

Figure 5.2 Magnitude versus frequency of RC low-pass filter

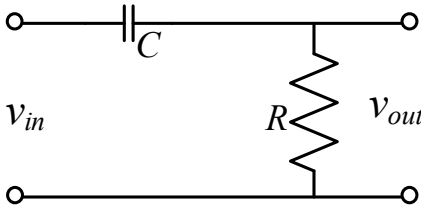

Figure 5.3 RC high-pass filter

Another filter circuit is shown in Figure 5.3. When the input signal V_{in} is in low frequencies, the capacitor C will act as a huge impedance or even an open circuit. Then the output V_{out} will approximately equal to zero. On the contrary, when the input signal V_{in} is in high frequencies, the capacitor C will act as a shorted path. Then the current will flow through capacitor C and the output V_{out} will approximately equal to V_{in}. From this analysis, we notice that the circuit in Figure 5.3 allows high frequencies signals to pass, and rejects signals of low frequencies. So, it is a high-pass filter. Similar to the low-pass filter, Figure 5.4 shows the magnitude versus frequency of a high-pass filter.

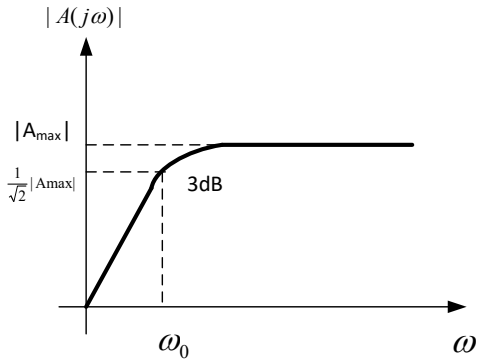

Figure 5.4 Magnitude versus frequency of RC high-pass filter

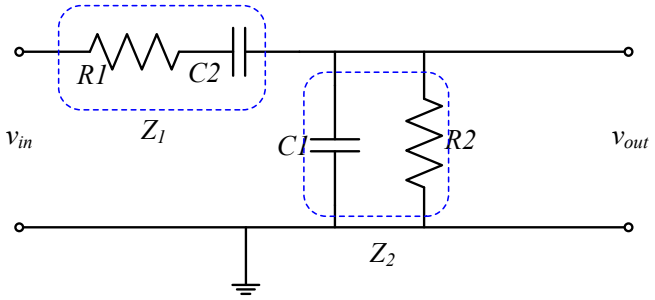

Figure 5.5 RC band-pass filter

Figure 5.5 demonstrates a band-pass filter. It is a hybrid circuit which was made up by a low-pass filter and a high-pass filter. It can be seen in the circuit, the R_1 and C_1 constitute a low-pass filter where only signals of low frequencies can flow through and R_2 and C_2 constitute a high-pass filter where only signals of high frequencies can flow through. This means that both the signals of low frequencies and signals of high frequencies are not able to flow through. Only the signals in a certain range of frequencies can pass. So, it is a band pass filter. As can be seen in Figure 5.5, the transfer function can be calculated by:

$$\frac{v_{out}}{v_{in}} = \frac{Z_1}{Z_1 + Z_2} \tag{5.3}$$

Where,

$$Z_1 = \frac{R_1 \dfrac{1}{j\omega C_2}}{R_1 + \dfrac{1}{j\omega C_2}} = \frac{R_1}{1 + j\omega R_1 C_2} \tag{5.4}$$

$$Z_2 = R_2 + \frac{1}{j\omega C_1} = \frac{1 + j\omega R_2 C_1}{j\omega C_1} \tag{5.5}$$

Thus,

$$A(j\omega) = \frac{Z_1}{Z_1 + Z_2} = \frac{\dfrac{R_1}{1 + j\omega R_1 C_2}}{\dfrac{R_1}{1 + j\omega R_1 C_2} + \dfrac{1 + j\omega R_2 C_1}{j\omega C_1}} \tag{5.6}$$

Assume $R_1 = R_2$ and $C_1 = C_2$, and $\omega_0 = 1/(RC)$, then,

$$A(j\omega) = \frac{\omega_0 \times j\omega}{(j\omega)^2 + 3\omega_0 \times j\omega + \omega_0^2} \tag{5.7}$$

The magnitude of the transfer function $|A(j\omega)|$ can be calculated by the equation below:

$$\left|A(j\omega)\right| = \frac{\omega_0 \omega}{\sqrt{(\omega_0{}^2 - \omega^2)^2 + 9\omega^2 \omega_0{}^2}} \tag{5.8}$$

From the equation (5.8), we can find that when ω is both too small or too big, the magnitude $|A(j\omega)|$ reduces. Figure 5.6 shows the magnitude response of a band-pass filter.

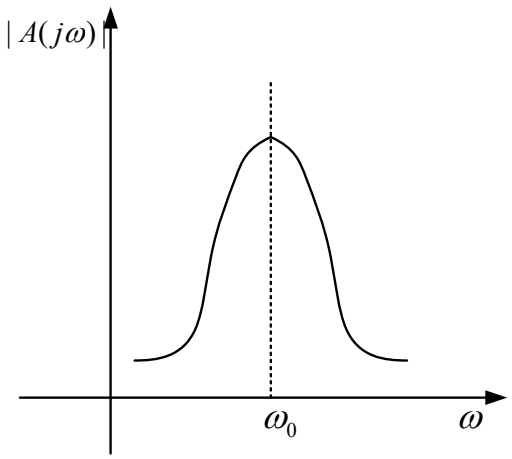

Figure 5.6 Magnitude versus frequency of RC band-pass filter

5.2.2 Active Filters

All the designs we have discussed above are filters built up with passive components. In practice, there are many designs that utilize active components to implement filter circuits. The reason is that if we design a filter with passive components only, attenuation will be introduced in the output of the circuit. However, active components can help to reduce or even overcome the attenuation. A typical low-pass filter circuit with an active component is shown in Figure 5.7. In this filter, there is an op-amp in the loop. The resistance and the capacitor make this circuit a low-pass filter, because signal components in high frequencies cannot pass through the circuit.

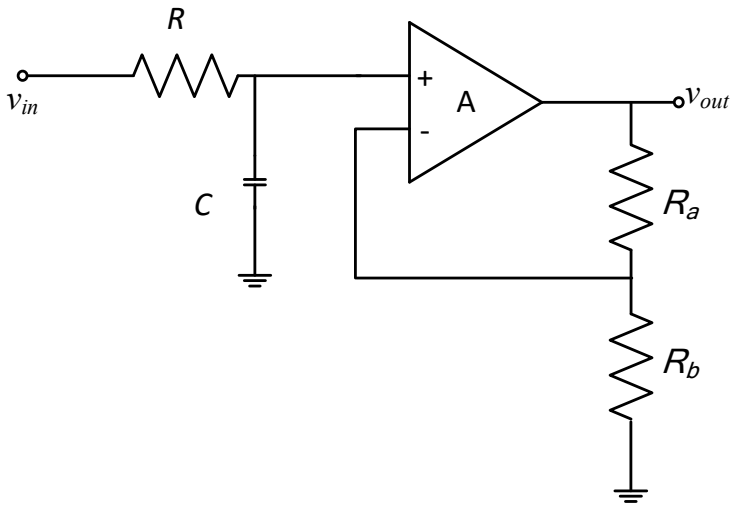

Figure 5.7 Low-pass filter with an operational amplifier

Figure 5.8 shows a high-pass filter. The principle is similar as the low-pass filter we discussed above.

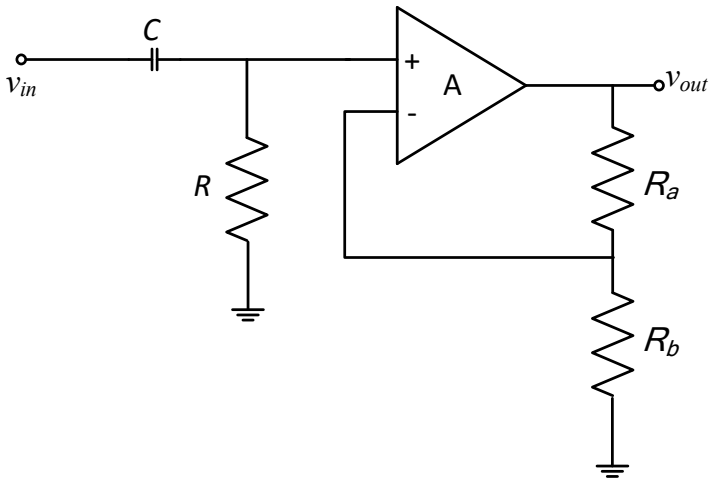

Figure 5.8 High-pass filter with an operational amplifier

5.3 The Proposed Band Pass Filter

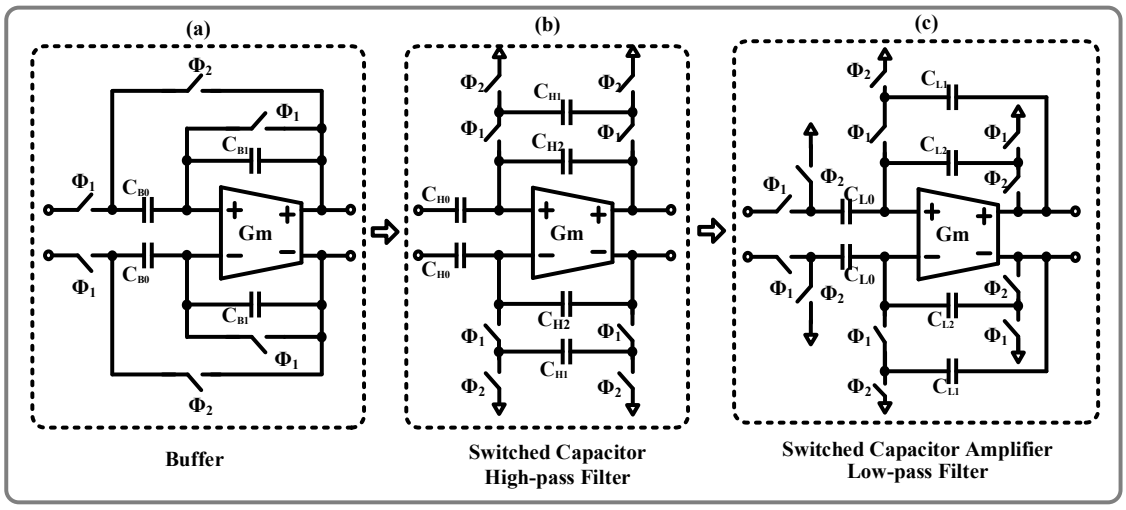

Figure 5.9 The proposed switched capacitor band-pass filter circuit

Figure 5.9 shows the differential switched capacitor band-pass filter circuit implemented in this research. The switched capacitor band-pass filter is cascaded following the envelope detector that we have discussed in Chapter 4. The function of this circuit is to remove the large DC components in the extracted envelope and amplify the envelope amplitude. From Figure 5.9, it can be seen that there are three parts in the circuit. The first part, Figure 5.9 (a) is a unity gain buffer, which is applied as a driver for the following circuits. Then, Figure 5.9 (b) is a switched capacitor based high-pass filter. In Figure 5.9 (b), switches controlled by ϕ_1 and ϕ_2 and capacitors C_{H1} constitute high resistors. And a high pass pole can be implemented with these high resistors and capacitors C_{H0}. Finally, Figure 5.9 (c) is a switched capacitor based low pass filter, which is a single stage active filter. In this part, the function of capacitor C_{L2} can remove the DC offset components caused by the amplifier. Switches controlled by ϕ_1 and ϕ_2 and capacitors C_{L0} and C_{L1} can provide a low pass pole. As a result, the complete circuit as shown in Figure 5.9 can realize a band-pass filer, and

this band-pass filter is employed to remove the unresolved interferences from the extracted envelop signals in order to eventually achieve a reliable data transmission.

Chapter 6 ADC

6.1 Introduction

Among all the functional modules in solid-state integrated circuit design, data converter should be one of the most widely used circuits that can be used as an interface between digital circuit and analog circuit. For example, when the physical signals are captured in the real world, they are all in analog format. To allow data post processing, we have to utilize converter to convert the signals from analog format to digital. Generally, there are two types of converters: one is DAC (digital to analog converter) which is used to convert digital signal to analog signal, the other one is ADC (analog to digital converter) which is used to convert analog signal to digital signal. ADC converters can also be divided into two categories: serial ADC and parallel ADC. A serial ADC outputs digital signal bit by bit; while a parallel ADC outputs digital signal by multi-bits simultaneously.

With the development of wearable electronic devices and portable devices, low power ADC or DAC converter circuits are extensively studied by many researchers. Among all the different types of low power ADC applications, Successive Approximation Register (SAR) Analog to Digital Converter (ADC) is one of the most common implementations of ADC because of its simpler circuit structure and lower power consumption [75] [76].

6.2 Principle of ADCs

6.2.1 Principle of SAR ADC

A successive approximation register ADC is a particular type of analog to digital converter that converts a continuous analog waveform into a discrete digital representation through binary search algorithm [76]. It needs a few cycles of comparison to achieve one signal sample's conversion. Normally the amount of the comparison cycles is the resolution of a SAR ADC. For example, if the resolution of a SAR ADC is 10 bit, then the output of a sample will be generated after 10 cycles of comparison. Higher resolution means more cycles of comparison, which commonly also means the SAR ADC needs more time to process a sampled signal. The SAR ADCs are widely used for low power and low speed applications. The speed is usually less than several MS (Mega Samples) per second. In recent years, along with the development of CMOS technology, the average device size of SAR ADCs is scaled down, the speed of them is however increased. Some designs can achieve resolution from 5 bit to 12 bit while the speed is around tens of MS per second, and some may be even faster [77]. Figure 6.1 shows the structure of a conventional successive approximation ADC.

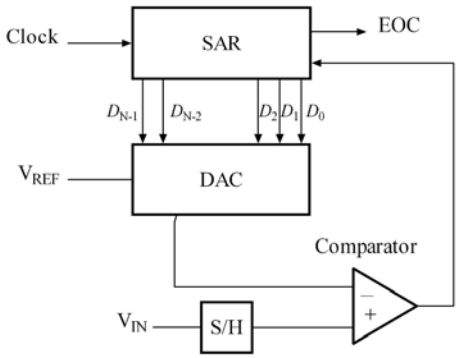

Figure 6.1 Structure of conventional SAR ADC [78]

Since a SAR ADC works in cycles. In every comparison cycle, the algorithm begins by comparing the voltage of the target with the middle element of the sorted array. If the target voltage is less than the voltage of the middle element, then the comparison goes ahead on the lower half of the array; if the voltage is greater than the voltage of the middle element, then the comparison goes ahead on the upper half of the array; if they are the same, then the position is returned and the comparison is finished and the conversion of a sample is done. The comparison operation flow of a SAR ADC is displayed in Figure 6.2.

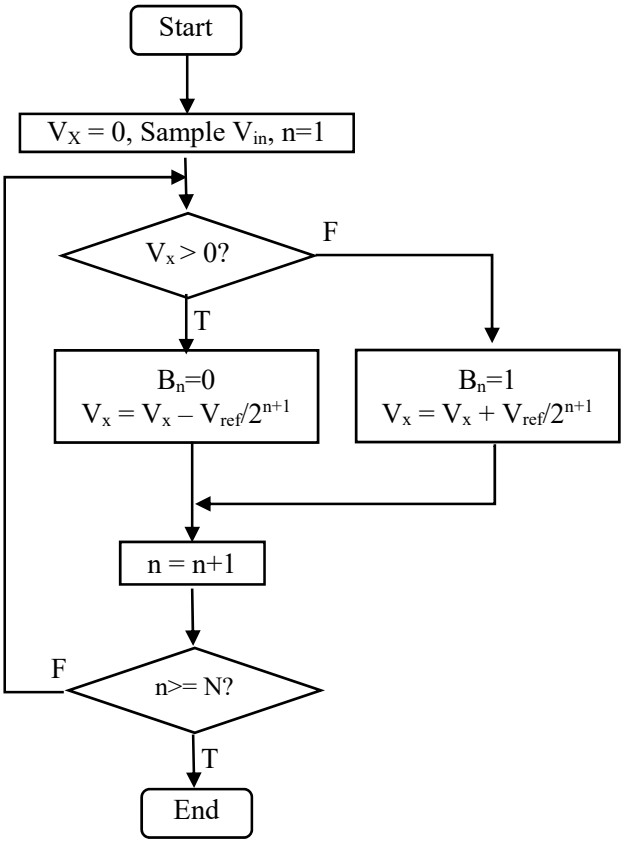

Figure 6.2 Operation flow of SAR ADC

6.2.2 Charge Redistribution SAR ADC

A Charge Redistribution Successive Approximation Register Analog to Digital Converter (Charge Redistribution SAR ADC, CR SAR ADC) is a particular architecture of the SAR ADC implementation [78]. It normally consists of a switch capacitor array, a sample and hold circuit, a DAC and a comparator. Figure 6.3 shows a typical schematic of the CR SAR ADC. The work flow of a CR SAR ADC considered consists of three steps, which represent three different working modes of it. They are sampling, holding and redistribution modes. Before an ADC working, the capacitor array will commonly be discharged. Then the ADC

shown in Figure 6.3 will first work in the sampling mode. By switching S_b and S_1 - S_n to the V_{in} side, all of the lower plates of the capacitors are switched to connect to the input signal. The comparator acts thence as an op-amp in this mode. If S_a is connected to the ground, which mean both V_x and V_y are zero. In such a connection, a total charge amount of $(-2^N C_0 * V_{in})$ will be stored on the upper plant of the capacitors. C_0 is the capacitor unit in the switch-capacitor array.

Next, ADC will work in the holding mode. S_b is switched to the V_{ref} side, and all the switches from S_1 to S_n on the lower plant side are switched to ground. At the meantime, S_a is switched off so that the charges in the upper plant of all the capacitors is applied as a voltage of $(-V_{in})$, which is input to the comparator as V_y.

Finally, in the third step ADC works in the redistribution mode, the charges in the upper plate of each capacitor is going to be applied independently or in group as a specific voltage supply to compare with the reference voltage V_{ref} to approximate the input sample signal and determine digital signal bits. It begins with generating the most significant bit (MSB) by switch S_n (the one controls the largest capacitor) to V_{ref}. This operation will change the voltage V_y to $(-V_{in} + V_{ref}/2)$ from $-V_{in}$, and eventually, this voltage will become the input of the comparator. It can be seen from Figure 6.3 that the two input terminals are connected to $V_y = (-V_{in} + V_{ref}/2)$ and ground, and it means V_{in} is compared with $V_{ref}/2$. After this operation, the ADC will get the first bit of the result. If V_y is larger than the potential of ground $(-V_{in} + V_{ref}/2 > 0)$, which mean V_{in} is less than $V_{ref}/2$, then the first bit of output, which is also the most significant bit B_1, will be "0"; on the contrary, if voltage V_y is less than the voltage of ground $(-V_{in} + V_{ref}/2 < 0)$, which means V_{in} is larger, then the first bit of

output B_1 will be “1”. Each bit of output signal from the comparator will also be used to control the next cycle of the comparison.

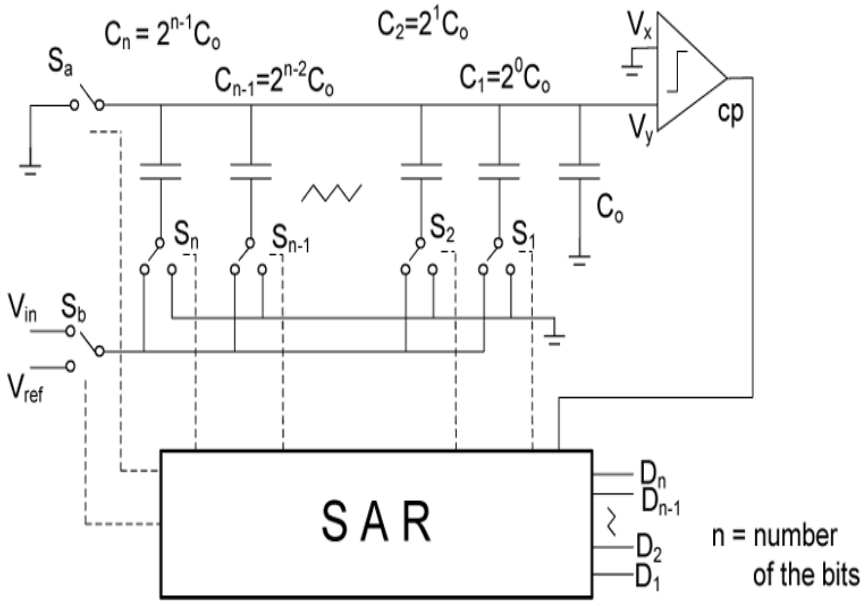

Figure 6.3 Switch-capacitor array scheme in CR SAR ADC [79]

If the first MSB output from comparator is a high potential output, then the most significant bit capacitor will remain connecting with V_{ref}; meanwhile, the neighbor capacitor, which is the second largest one in the switch-capacitor array will also be connected to the reference voltage V_{ref} through switch S_{n-1}. Since the capacitance of this capacitor is $2^{N-2}C_0$, the voltage V_y will be $(-V_{in} + V_{ref}/2 + V_{ref}/4)$. In contrast, if the first MSB output from comparator is a low potential output, then the most significant bit capacitor will be connected to ground but not remain connecting to V_{ref}. Meanwhile, the neighbor capacitor, which is the second largest one in the switch-capacitor array will be connected to V_{ref} through switch S_{n-1}. Since the capacitance of this capacitor is $2^{N-2}C_0$, the voltage V_y will be equal to $(-V_{in} + V_{ref}/4)$. The comparison procedure is same as the first MSB bit above.

After all the N cycles of comparison, the comparator will output the accurate digital value of the sampled input signal.

Figure 6.4 shows the equivalent switch capacitor array circuit of a charge redistribution SAR ADC which is in the redistribution mode. Regarding the principle of charge conservation, the changes of the voltage V_y is determined by the changes of the charges during each cycle of comparison in the redistribution mode. In another word, during the switching operation, the charges stored in the switch-capacitor array in the redistribution mode should equal to the sampling mode. From Figure 6.4, and V_y, we can have

$$C_{\text{ref}} * V_{\text{y}} - V_{ref} + C_{\text{gnd}} * V_{\text{y}} = (-2^{\text{N}}\text{C} * V_{\text{in}})$$

Solve the equation above, we can have

$$V_{\text{y}} = -V_{in} + (C_{\text{ref}}\, V_{ref})/\Sigma C$$

Where $C_{ref} = \sum_{n=1}^{N} C_n\, b_n,\ \sum C = 2^n C_0$.

C_{ref} is the capacitance summation of V_{ref}-connected-capacitors, and C_{gnd} is the capacitance summation of all the grounded capacitors. N is the ADC converter's resolution.

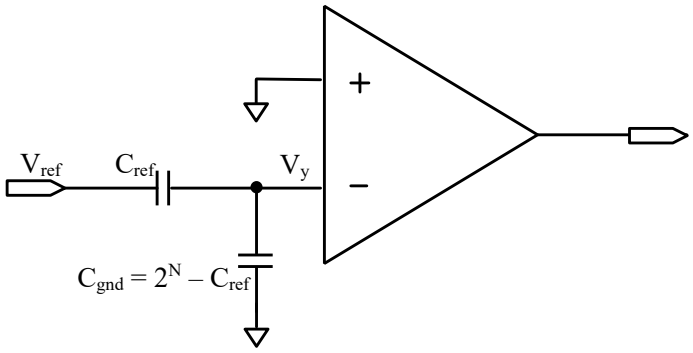

Figure 6.4 Analog equivalent of switch-capacitor array during charge redistribution

From the discussion in section 6.2, it is obvious that the performance of the entire charge redistribution SAR ADC device is determined by the performance of switch-capacitor array. The merit of this charge redistribution SAR ADC is that it is a low power consumption device, however, there are also some constraints with it. The most to be considered constraint of this circuit is that the big capacitance of switch-capacitor array limits the speed of the whole circuit. And, the parasitic capacitance is another limitation of the circuit. The parasitic capacitance in this charge redistribution SAR ADC circuit crucially determines the performance of the switch-capacitor array and the accuracy. Figure 6.5 shows that the parasitic capacitances, which associate with the capacitor C_i in both the upper plate and the lower plate. It can be seen in Figure 6.5, the capacitor C_i is a designed binary weighted capacitance. It consists of polysilicon layers and metal layers. And normally, when the substrate below the metal layers (the lower plate) is grounded in solid circuit, there may be parasitic capacitance exists, such as C_{pl} in Figure 6.5. And this parasitic capacitance may be 1/5 of the total capacitance of C_i. At the meantime, the parasitic capacitance on the upper plate may also exists because of the interconnect ware. It may also take 1% - 5% of the total capacitance of C_i.

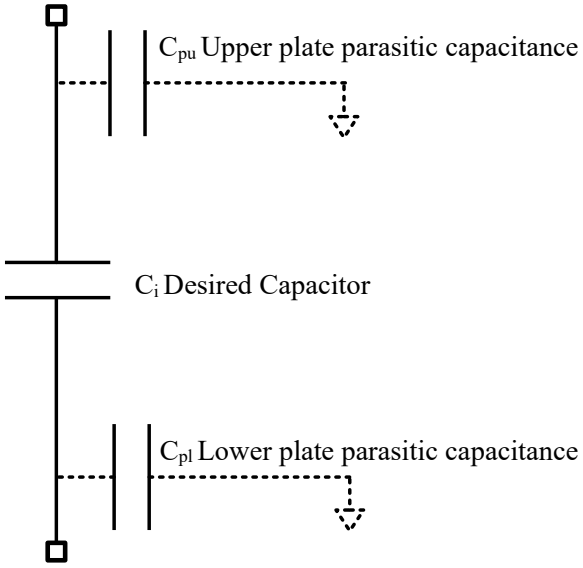

Figure 6.5 The parasitic capacitance of integrated capacitor

The switch array may contribute additional error in the circuit because the switches are implemented with CMOS transistors. Also, since the switches are connected to the upper plate and the lower plate, the performance will be affected by clock feedthrough and charge injections due to the channel capacitance. However, if all the capacitors' lower plant can be connected to V_{ref}, yet not the input of the comparator, the effect of parasitic capacitance can be reduced.

6.3 The Proposed SAR ADC

In this research, considering the power supply and the frequency of the power carrier signal. The ADC in the off-body transceiver side is expected to work with less than 20MHz signal bandwidth and the required resolution is 10 bit with a speed of 50MSps. And the power consumption should be less than 1 mW. Figure 6.6 shows the architecture of the SAR ADC in this research. It can be seen that this circuit is a fully differential architecture. The reason to choose a full differential architecture is that it can suppress the noises from the substrate

and the sample signal, and it can also reject the common mode noise. Hence, the accuracy can be significantly improved.

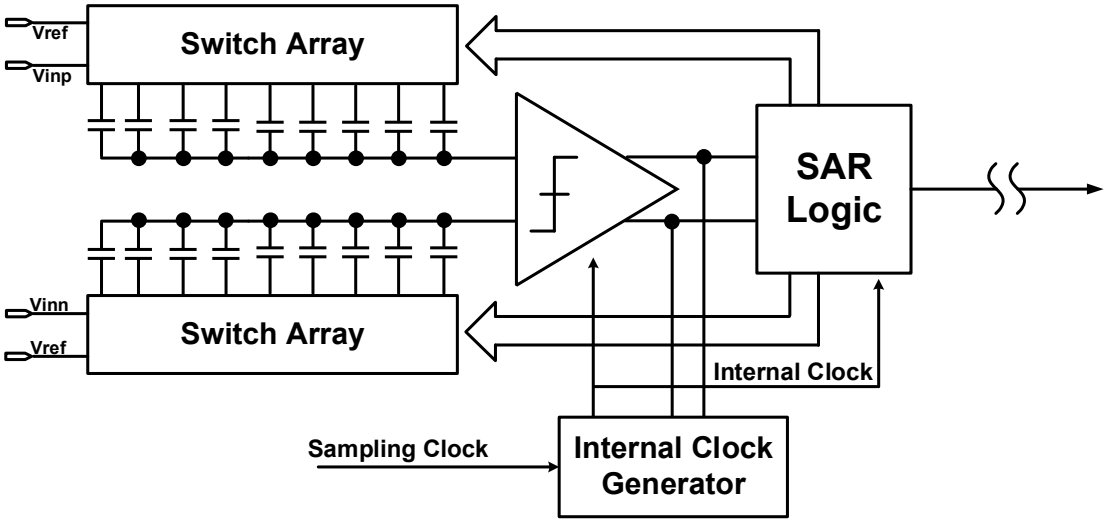

Figure 6.6 SAR ADC architecture in this research

Because the proposed SAR ADC is a fully differential architecture, the top switch array and the bottom switch array work in fully complementary operations. To simplify the description, we will only discuss the work mechanism of the top side. At the beginning, all the upper plants in the capacitor array should be connected to the input signal. At the meantime, the lower plant of the capacitors will be connected to V_{ref}. Then, the SAR ADC will disconnect the connection between the input and the upper plant of the capacitors. With this operation, the SAR ADC realizes the first cycle of comparison between V_{inp} and V_{inn}. It can be noticed that in this cycle, the SAR ADC outputs the first MSB bit without switching any single capacitor. Following this comparison, regarding the first MSB bit, the higher voltage potential side between the top and bottom sides of switch-capacitor arrays will be re-configured by connecting its largest capacitor to ground, and the side with lower voltage potential will be kept unchanged. With this operation, the SAR ADC realizes the

second cycle of comparison between (V_{inp}-V_{inn}) and (V_{ref}/2) or (-V_{ref}/2). Reiterating the operations, the SAR ADC will eventually get the least significant bit (LBT). For each cycle of comparison, there will be just one single capacitor re-configured by the switch array, and this mechanism significantly reduces the power dissipation of the whole ADC circuit. The schematic is simulated in Cadence 6.1.5. The simulation result is listed below:

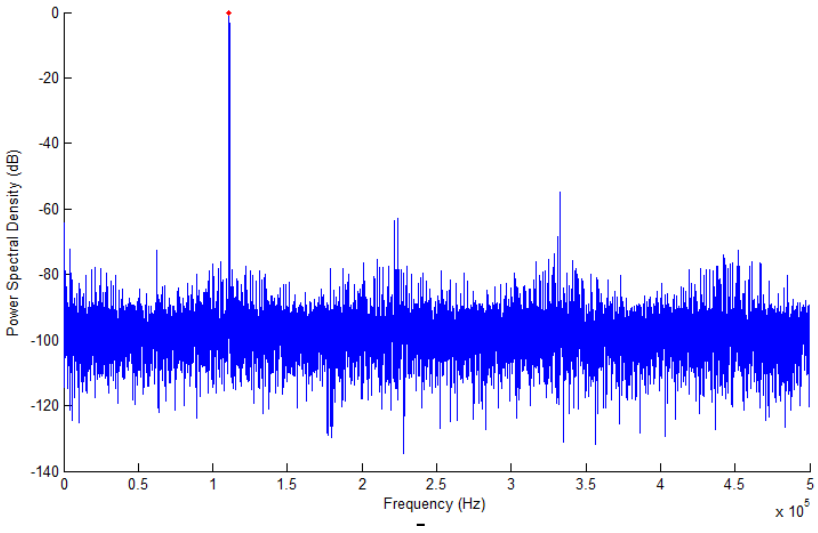

Figure 6.7 Measured 32,658 point FFT spectrum

The reason why we chose a 500kHz frequency signal is to verify high-order harmonic distortions for the designed circuits. Figure 6.7 demonstrates the power spectral and Table 6.1 displays the testing result in detail. Prototype measurement results will be discussed in chapter 7.

Table 6.1 Simulation result of the proposed SAR ADC

Specification	Result	
Supply Voltage (V)	1	1
DNL	-0.8 – 0.95	-0.92 - 1
INL	-0.9 - 1	-1.1 - 1.3
Power (mW)	<1	<1
SNDR (dB)	58.0	59
SFDR (dB)	47.8	52.9

Chapter 7 Measurement and Result

7.1 Introduction

Besides all the discussion earlier, in this chapter, we will demonstrate the prototype of this research and report the measurement result.

7.2 Class E amplifier measurement

As we have discussed in Chapter 2, considering the application requirements on the circuit, a prototype was created. Figure 7.1 shows the prototype of the proposed class E amplifier implementation. It can be found that there are three parts in Figure 7.1. The Class E amplifier in the figure is the implementation of the circuit of Figure 2.3, and it is connected to the coupling coil of the external transceiver by a piece of coaxial cable. The coaxial cable can help to reduce interferences. It can also be seen in the figure that there is a coil of implant. It is connected by another coaxial cable to an FPGA which is used to simulate the in body implanted device so that to generate loading impedance changes in this research.

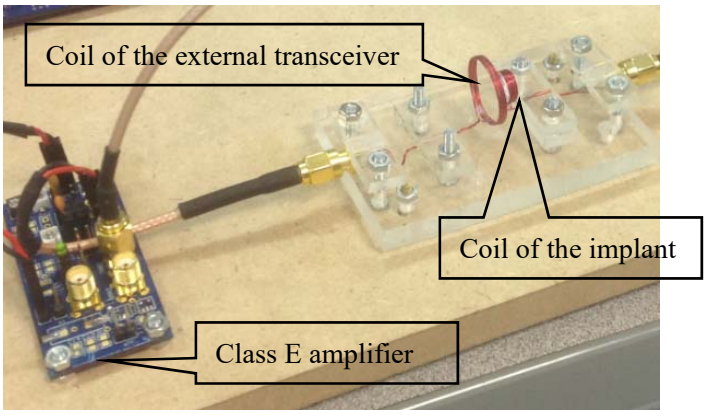

Figure 7.1 Prototype of the Class E power amplifier

The measurement is carried out with a power carrier of 10 MHz sinusoidal signal. The measure result is displayed in Figure 7.2 and Figure 7.3. Figure 7.2 displays how the coupling coefficient of the inductive link changes with respect to the different distances between the implanted coupling coil and the external transceiver coil, as shown in Figure 7.1. The range of distance is from 1 millimeter to 12 millimeters and the range of coupling coefficient is from 4% to 24%. The coupling coefficient will drop significantly with the increasing of coil distance. To achieve a coupling coefficient higher than 20%, we have to keep the coupling coil on the transceiver side close to coil on the implant side to within 3.5 millimeters; and to achieve a coupling coefficient of 10%, the coil distance should be less than 7.5 millimeters. The experiment was carried out in free space to verify the performance of the proposed system architecture. If the experiment is done with human tissue, the experiment performance will be degenerated. In the future, we will optimize the circuit design in order to achieve a better system performance, especially when there is human tissue between the transceiver and receiver.

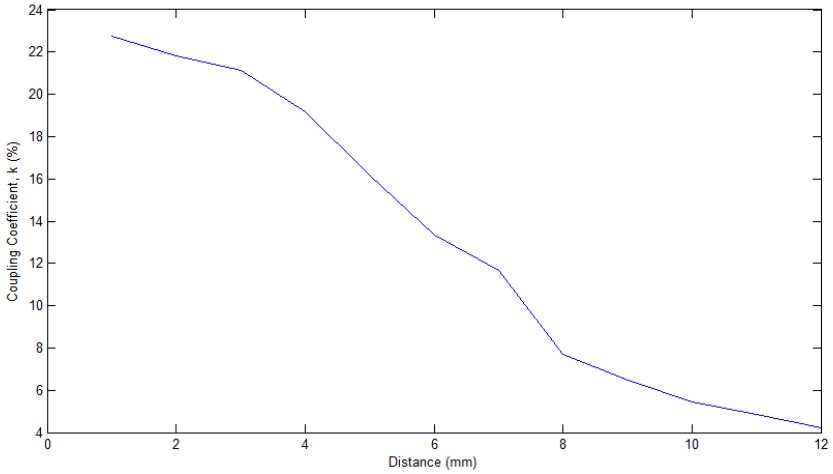

Figure 7.2 Coupling coefficient versus coils distance

Figure 7.3 displays how the inductive link efficiency changes with respect to different distances between the implanted coupling coil and the external transceiver coil as shown in Figure 7.1. It can be found that the range of distance is the same as Figure 7.2, which is from 1 millimeters to 12 millimeters, and the range of inductive link efficiency changes from 70% to 98%. The inductive link efficiency drops significantly with the increasing of coil distance. From 1 millimeter to 6 millimeters, the inductive link efficiency doesn't change too much (less than 5%), and after the coupling coils are separated by more than 7 millimeters, the inductive link efficiency will drop very quick.

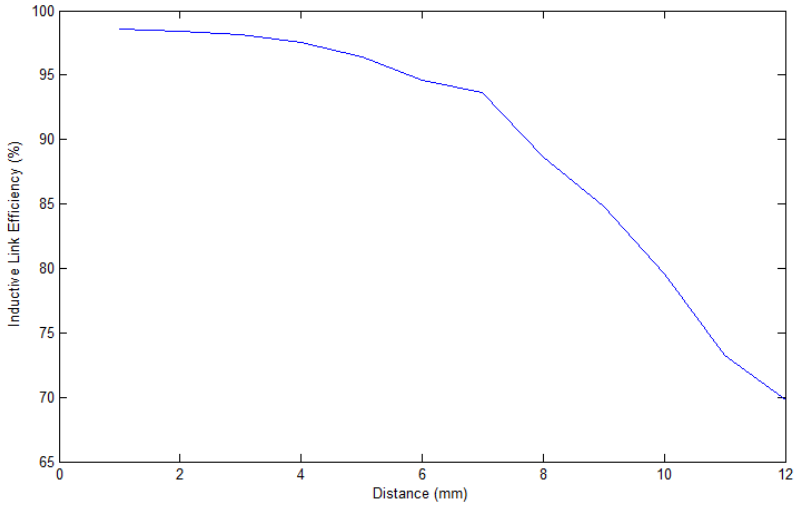

Figure 7.3 Inductive Link Efficiency versus coils distance

7.3 Envelope Detector and LSK Measurement

The designed LSK including the pre-amplifier, the envelope detector, the switched-capacitor band-pass filter and the SAR ADC were fabricated with 180nm CMOS technology as shown in Figure 7.4. A PCB testing circuit was created to test the chip as

shown in Figure 7.5. It can be seen that the chip has a core circuit area of 750 µm x 800 µm.

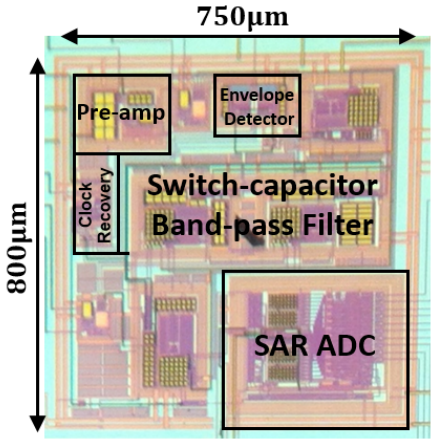

Figure 7.4 Prototype chip micrograph

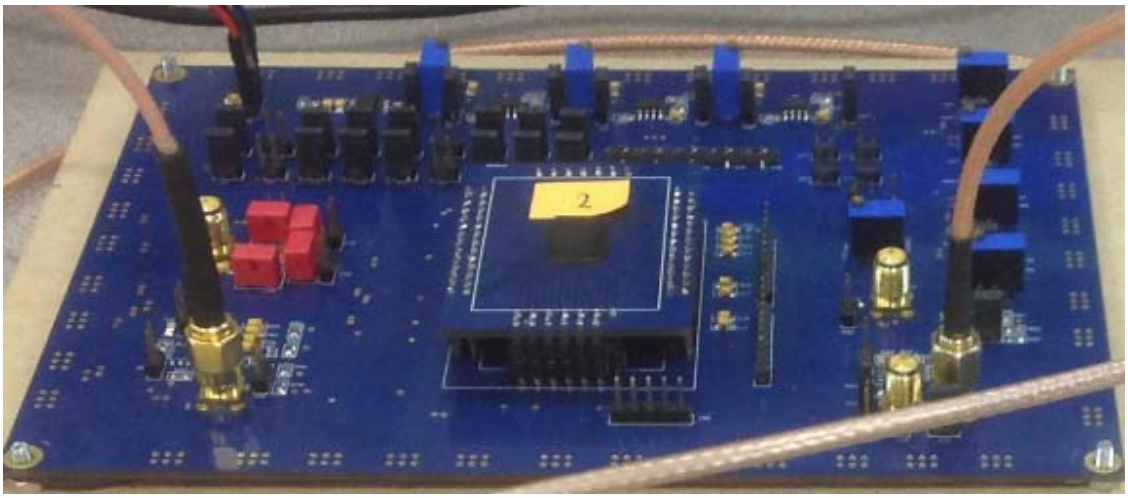

Figure 7.5 Prototype PCB board of the proposed transceiver

To test the envelope detector, a series of signals were generated by signal generator --- Agilent 33250A, and the signals were input to the envelope detector module in the prototype; then the outputs were captured by a mixed signal oscilloscope --- Agilent MSO614A. Results were processed and plotted in Matlab 2014. The envelope detector was independently tested by capturing the output signal before the output signal was sent to the SAR ADC. Figure 7.6 shows the extracted envelope of a square waveform which was

modulated by a 20k Hz signal with carrier frequency of 10 MHz in 50% modulation index. The amplitude difference could be clearly distinguished from the detected envelope because the modulation index of the input signal was relatively large, which was 50%.

Similarly, to test the LSK demodulator performance, a series of signal were generated by signal generator --- Agilent 33250A, and the signals were input to the prototype and the output signals were captured by a mixed signal oscilloscope --- Agilent MSO614A. A data signal of 1 MHz multiplied by a carrier signal in 10 MHz frequency and modulated in 6% modulation index was input to and demodulated by the prototype. The result was shown in Figure 7.7. A more distinct output was plotted in Figure 7.8 (a) and the SAR ADC output was plotted in Figure 7.8 (B).

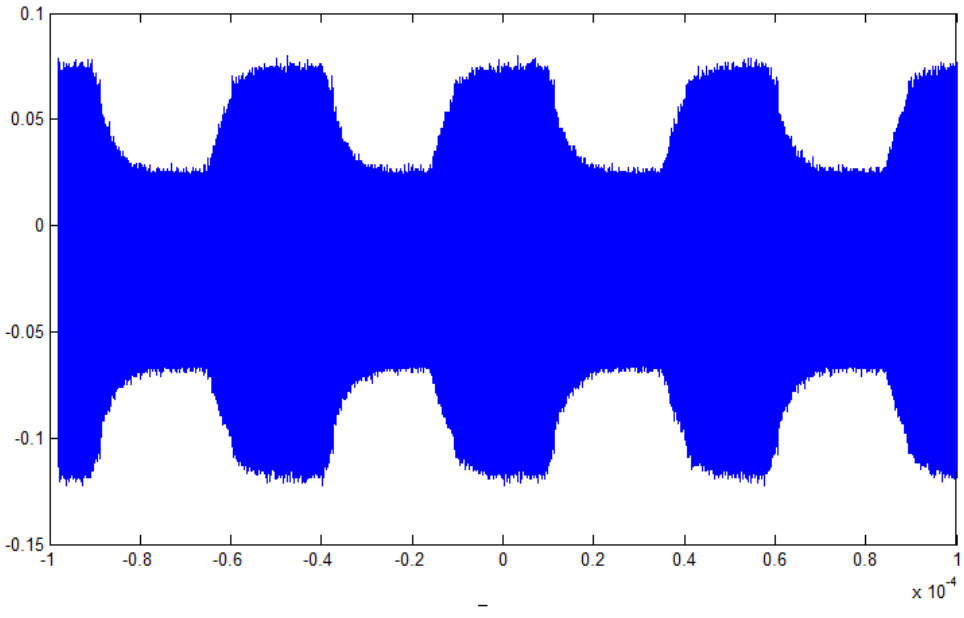

Figure 7.6 Extracted envelope of square wave modulated input signal (carrier frequency =10MHz, data rate =20 KHz, modulation index = 50%)

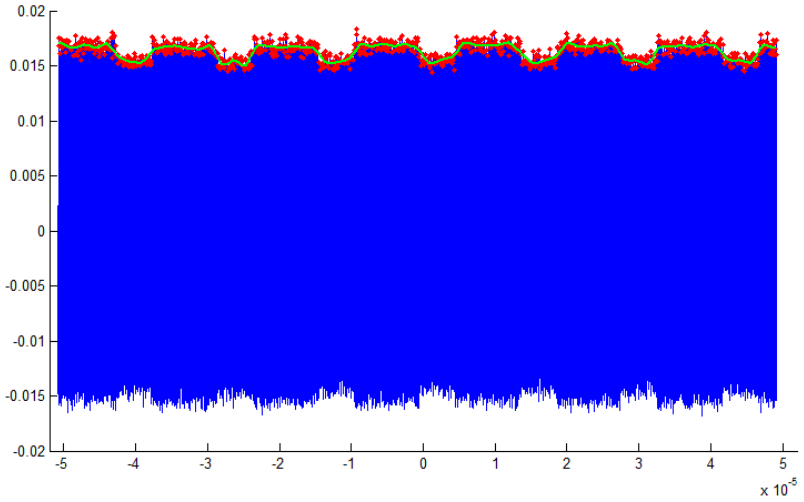

Figure 7.7 Demodulated output of a 1 MHz signal with carrier frequency of 10 MHz in 6% modulation index

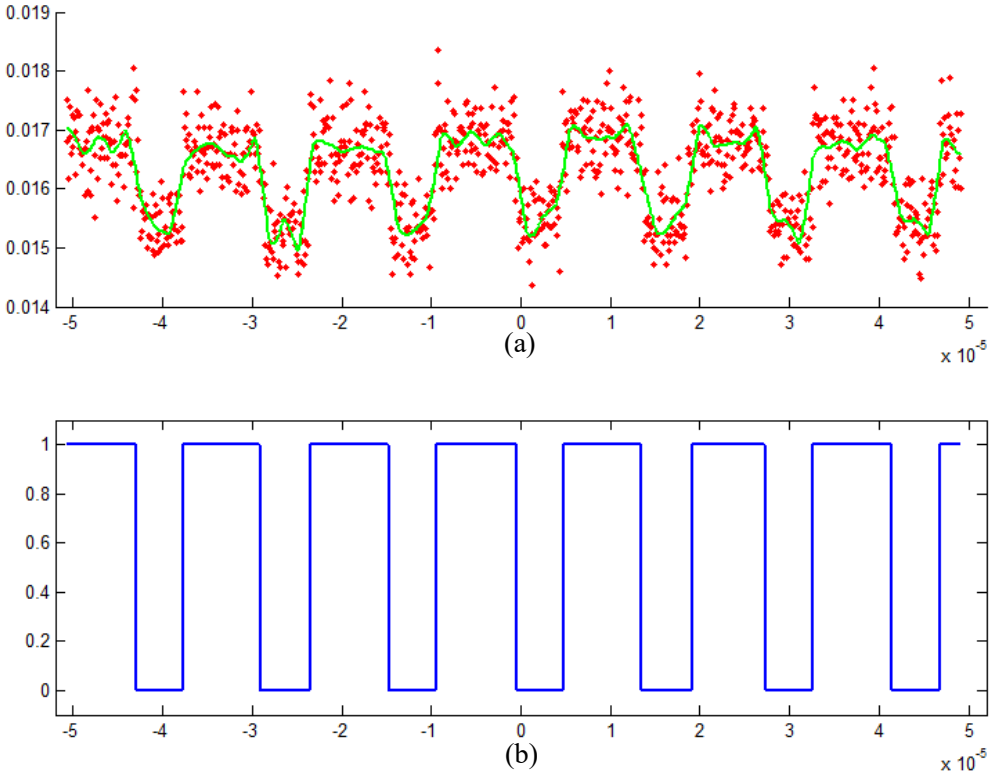

Figure 7.8 (a) Zoom-in of the output in Figure 7.7, (b) SAR ADC output

Figure 7.9 indicates how the minimum achievable modulation index changes related to the increasing inductive coils distance. It can be found that the coil distance is changed from 1 millimeter to 12 millimeters, and the corresponding minimum achievable modulation index

changes from 5% to 20%. For example, when the coils were separated in a 6 millimeters distance, to have a distinguish demodulation result, the input signal have to be modulated in a higher modulation index than 13%. In another word, this design can only detect a signal with modulation index of >13% when the coils distance is 6 millimeters. From the experiment result, it is shown that the best modulation index that we can achieve is 5%, which is a little different from the simulation because the performance of the designed circuits is degenerated after the chip was fabricated and there are several environment interferences on the prototype.

Figure 7.10 shows the power efficiency changes according to the inductive coils distance. From the figure we can find that in this design, 4 millimeters coil distance was the most optimal condition to achieve the highest efficiency which was 22%. This test was carried in the prototype with an FPGA to simulate an implanted device so that to generate the data signal. A more appropriate optimal distance can be a future work direction. Table 7.1 lists the details of the performance of the entire transceiver.

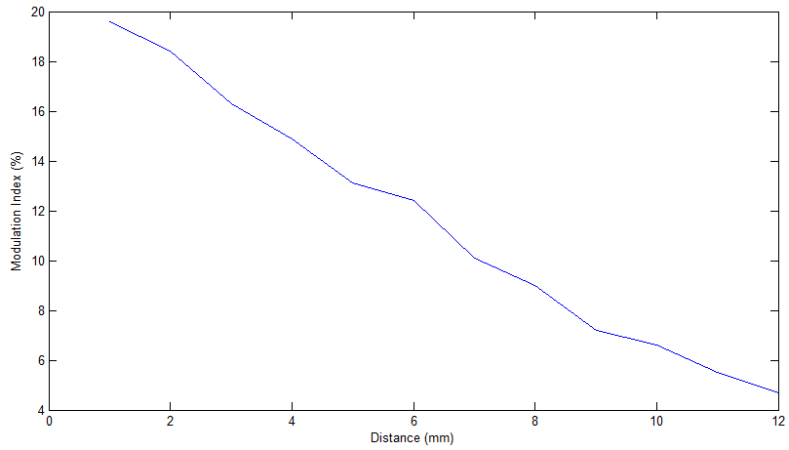

Figure 7.9 Minimum modulation index versus inductive link distance

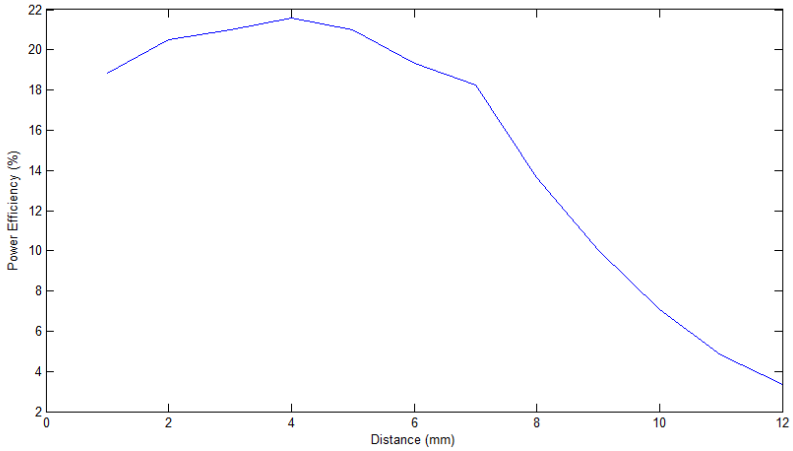

Figure 7.10 Power efficiency versus inductive link distance

Table 7.1 Designed transceiver performance

Wireless Power		Data Link (LSK demodulator)	
Operating Frequency	10 MHz	Fabricate Technology	0.18µm
Transmitter Coil	19.8mm, 1.62µH	Area	750µm x 800µm
Receiver Coil	9.3mm, 752nH	Current Consumption	3.6mA
Coupling Coefficient	11.7%	Data Rate	1Mbps
Inductive Link Efficiency	93.6%	Carrier/Data Ratio	10:1
		Modulation Index	5-20%

Chapter 8 Conclusion

Advance in science and technology changes the life style of modern human. For example, most of the people nowadays communicate and interact through electronic devices, which is very different from the conventional intercommunication method. When the technology is employed in medical research, new diagnosis and therapeutic methods were therefore created. There are a lot of new appliances, devices and software applications invented for health care. Implantable device and wearable devices are two typical types of devices in these inventions that have been extensively employed in clinic and health care markets because of the low cost, portability and easy operation. When researchers were exploring in this field, they found that smaller device size and lower power consumption made these devices being more widely used, especially when such devices could even perform better in wireless data communication and accuracy. Wireless biotelemetry, as the only contactless interface in both the transceiver and receiver of these devices is thus challenging to the researchers. Higher data rate and less energy dissipation are the two important objectives for such applications.

In this work, to achieve a higher data rate and to consume less power consumption, a novel transceiver for biotelemetry was designed. The circuit, which included a pre-amplifier, a multi-phase envelope detector, a switch-capacitor based bandpass filter and a 10 bit resolution SAR ADC was designed and the schematic was fabricated in 180nm CMOS process technology. A PCB prototype was also designed and produced to test the chip.

To reduce the power dissipation, a transistor based Class E power amplifier was designed for the transceiver to amplify input signals, and a pair of inductive coupling coils were

created for the Class E power amplifier while and FPGA based receiver were used to implement the transmission of energy and data. To reduce the power consumption and the body size, a single antenna/coil modulation solution --- LSK, which is a special scheme of ASK was opted for the transceiver demodulator. This is because the LSK modulation method has a higher data spectral efficiency than other modulation methods such as FSK or PSK. Meanwhile, the LSK demodulation technique allows power and data transmission simultaneously through one single inductive link. Through the LSK demodulator, the biological signals generated by the receiver were transmitted back to the transceiver.

The transceiver could work under a variety of modulation indexes and different coding/decoding protocols. At the same time, it was able to impose the whole microelectronic system in terms of power consumption and device size. The measurement results indicated that the circuit could support the power carrier signal in different frequencies and data rates. The area of the chip was 750μm x 800μm and the achievable minimum modulation index of the prototype was 5%, whereas the supported data rate was 1 Mbps. The total current consumption was 3.6mW with a 1.65 V power supply. There is still a gap between the prototype testing performance and the simulation result. However, consider the comprehensive performance, the proposed transceiver design was significantly improved in both power consumption and data rate among the same designs.

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