IMPROVING THE HAFNIA-BASED RESISTIVE RANDOM-ACCESS MEMORY THROUGH MATERAL ENGINEERING

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A THESIS SUBMITTED

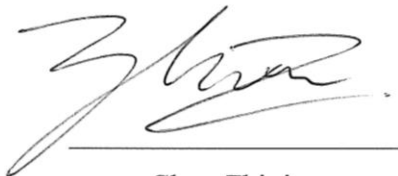
FOR THE DEGREE OF DOCTOR OF PHILOSOPHY
DEPARTMENT OF ELECTRICAL
AND COMPUTER ENGINEERING
NATIONAL UNIVERSITY OF SINGAPORE

2016

DECLARATION

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.



Chen Zhixian
8 January 2016

Acknowledgements

First and foremost, I would like to thank my supervisor, Prof. Wu Yihong, for the numerous ideas, suggestions and constructive discussions which helped bring this work to a higher level. I am truly grateful for the invaluable advice, guidance and support throughout my candidature. I am grateful to the ECE department (NUS) for the opportunity to further my knowledge and hone my skills. I would like to sincerely thank Wang Ying, Yang Yumeng and Zhang Chi for the help in the lab and the fruitful discussions we had.

I would also like to thank IME (A*STAR) for the development of my knowledge, skills and interests. Special thanks go to all the FAB staff for their assistance in wafer processing, along with the many other technical staff that helped in one way or another: Navab Singh, Li Xiang, Aashit Kamath, Fang Zheng, Wang Xinpeng, Tang Yanzhe, Zhang Zhiping, and Patrick Lo.

I would like to thank my parents for their guidance in my younger years, instilling in me the desire to pursue knowledge, and building up the strong foundation which defines who I am and who I want to be. To my sons, Jadan and Nathan, you never fail to put a smile on my face when times are tough. Thank you for all the silly antics and unconditional love. Aim high and chase your dreams!

To my wife, Michelle, this would not be possible without you. You ignited my passion for research 8 years ago, and now it ultimately culminates to this thesis. With your love and encouragement through the good times and bad, nothing is impossible with you.

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Summary

Resistive random-access memories (RRAMs), where changes in resistance determine the memory state, are extensively investigated as one of the promising next-generation non-volatile memory technologies. The RRAMs possess many superior characteristics over the currently dominant flash memories: higher speed, better endurance, more scalable design and simpler fabrication processes. Among the different types of RRAMs, the redox RRAM based on transition metal oxides, like hafnia or HfO_2, has the best CMOS compatibility. These redox RRAMs rely on the reduction of the HfO_2 under an electric field which generates and aligns oxygen vacancies into a filament. This conductive filament facilitates electron conduction, resulting in a low resistance state. The subsequent re-oxidation of the conductive filament, also under an electric field, results in a high resistance state. However, due to the stochastic nature of such resistive switching, a large variation in the resistance of each state is often observed from cycle to cycle, and sometimes even programming failure could occur. This effectively reduces the memory window between the high and low resistance states and could possibly result in bit errors.

This thesis aims to address the issue of large resistance variation and programming failure in HfO_2-based redox RRAMs by increasing the memory window and/or reducing the variation. Using CMOS available processes like silicidation and atomic layer deposition (ALD), systematic investigations on bottom electrodes and switching characteristics of HfO_2 were carried out to identify the best bottom electrode material which, when used together with

HfO_2, gives a large memory window and low variation in read-write characteristics. Programming or reliability failures were identified and relevant measures were taken to reduce the failure rate.

First, the role of vertical silicon nanowire (VSNW) field-effect transistor (FET) as a select device was investigated. The small footprint and CMOS compatibility of the VSNWFET makes it a good select device for stand-alone memories. The TiN/Ni/HfO_2/n^+-Si RRAM cell was able to switch under three different modes: bipolar, unipolar, and bipolar with low current switching. Most notable was the bipolar mode where a 100x memory window was observed without the need for a compliance current.

Next, through silicidation, a TiN/HfO_2/Ni-silicide RRAM cell with varying Ni concentrations in the Ni-silicide was studied. Parasitic SET was found to occur during RESET in devices with higher Ni concentrations, where a parasitic filament is formed while the actual filament is being annihilated. This was avoided by reducing the voltage used for RESET. At lower Ni concentrations, low current switching was found to be possible.

Finally, by using ALD, the HfO_2 in TiN/Ti/HfO_2/TiN RRAM cells was engineered with an aim to achieve large memory window. It was found that under certain filament forming conditions and with larger HfO_2 grain sizes, large memory window is possible. The addition of a TiO_2 current limiting layer further improves the endurance of the RRAM cell.

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Chapter 1 : Introduction

1.1. Resistive Random-Access Memory (RRAM)

Resistive random-access memory has gained much interest over the past decade due to its potential to replace flash memories, and possibly even SRAM or DRAM. These memories rely on non-volatile and reversible resistance change within the memory cell to determine the different memory states as opposed to capacitance changes in flash memories. Thus, these memories are termed resistive random-access memories, or RRAM. The resistance states are commonly termed high-resistance state (HRS) and low-resistance state (LRS), although there may be more states like in the case of multi-level cells.

In what follows, we will first give a brief introduction to the limitations of NAND flash technology and then discuss the characteristics and advantages of RRAM.

1.1.1. Limitations of NAND Flash Technology

As the scaling of NAND flash progresses, more and more reliability problems appear. The root cause of these problems lie in the fundamental operating principles of flash memory – charge trapping. Although charge trapping provides an excellent means to store data non-volatilely for large scale memory applications, the ability to hold those charges becomes questionable as the cells are becoming increasingly small.

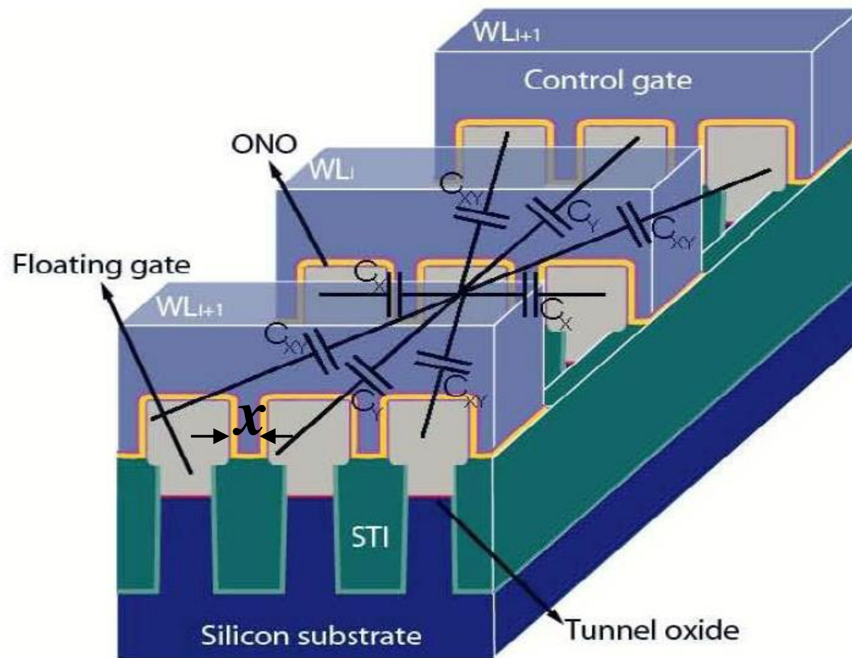
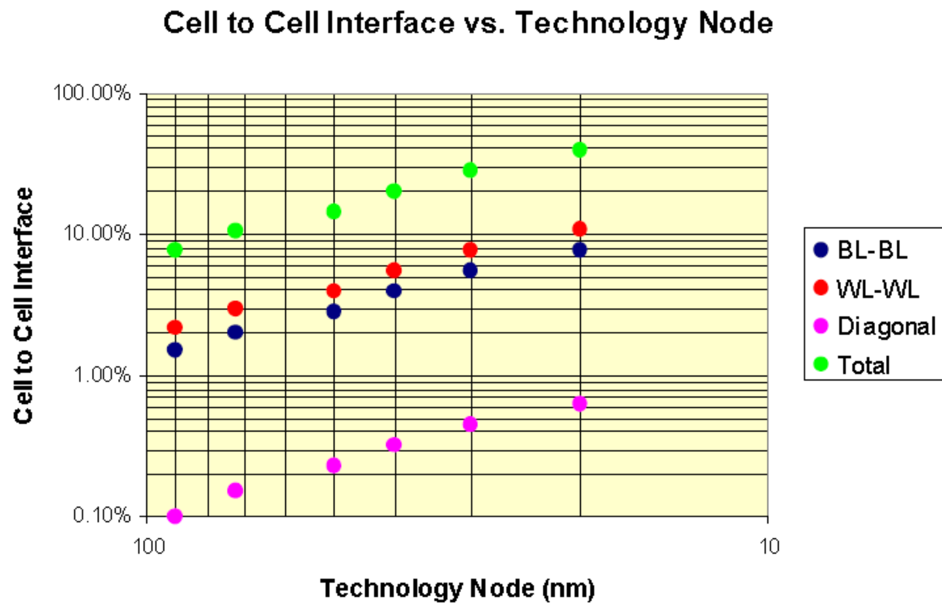


Figure 1.1. Three-dimensional view of the typical NAND flash memory array layout showing the various parasitic capacitances (© 2007 IEEE) [1].

Firstly, as the inter-cell spacing reduces with scaling, the space available for the control gate (CG), x, as shown in Figure 1.1, shrinks. The "wrapping" of CG around the floating gate (FG) is required to increase the CG to FG capacitance, which is needed for reliable erasing. Without sufficiently high CG to FG capacitance, the erase process, involving Fowler-Nordheim tunneling from FG to the channel, will not take place, since more electrons are injected into the FG from the CG than those tunneling out to the channel. So as x reduces, eventually the CG will not be able to fill the space and the CG to FG capacitance greatly reduces, rendering the devices unreliable.

Secondly, the space between word lines, along with x, also increases crosstalk or cell-to-cell interference, as shown in Figure 1.2. At close proximities, the program or erase of one cell may influence the neighboring

cells, about 40% in total at the 20 nm node, causing unwanted loss of data. The charge within a FG may also perturb the field of neighboring FG, leading to changes in charge distribution and could finally lead to read errors.



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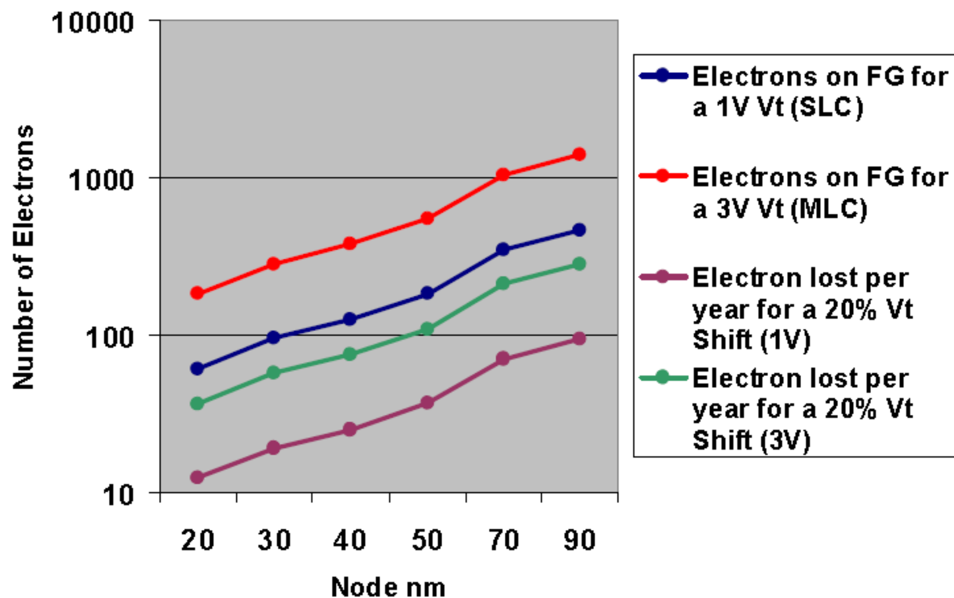

Figure 1.3. The predicted number of electrons present in the floating gate (FG) at various transistor threshold voltage, V_t (© 2007 IEEE) [1].

Thirdly, the tunnel oxide scaling also poses a problem of charge leakage, which would cause loss of data. The oxide gradually becomes damaged over program-erase cycles, forming traps within the oxide. These traps, if aligned in a column, would create a conduction path by trap-assisted tunneling, allowing charges within the FG to leak back into the channel. This creates a limitation for device endurance, which is the number of program-erase cycles before failure. The thinner the oxide is, the higher the chances of forming such a conduction path. Based on percolation theory [2], this limit of tunnel oxide may occur at about 7 nm thickness, below which the FG would be unable to hold charge.

Fourthly, the scaling of the size of the FG would also cause a scaling of the total charge present within the FG. At the 20 nm node, the trapped charges at 1 V threshold voltage (V_t) is predicted to be less than 100 electrons [1], as shown in Figure 1.3. A mere loss of about 10 electrons would cause more than 10% change in the V_t shift of the device. As such, the requirement for charge retention is increased at smaller sizes.

Lastly, in order to increase density-per-bit, multi-level cells (MLC) are used, whereby each memory cell is able to have multiple states, effectively allowing more bits within the same area. However, doing so would reduce the margin for errors as the memory window between each state tends to be much smaller, leading to much higher chances of errors.

Furthermore, endurance of flash memories is fairly low, about 10^4-10^5 cycles, which would not be suitable for embedded memory applications. Due to the charge trapping operation principle of flash memories, a high field and

longer time is needed to inject charge into the FG, resulting in high voltages and low write speeds.

All the above-mentioned are problems relating only to device operations and have not included process-related problems. Since the NAND flash half-pitch has advanced ahead of DRAM, it requires much more advanced processing, especially for lithography and etching. At smaller scales, it is also likely that process variations, like line edge roughness, random dopant fluctuations, noise from traps, have more impact on V_t variations,.

With all these problems ultimately limiting the size at which flash memories can be scaled, it is therefore crucial to search for alternative memories.

1.1.2. RRAM as a Solution

With a simple two-terminal metal-insulator-metal (MIM) structure and superior performance, RRAM can achieve higher density memory arrays with better performance and at lower power than flash memories. The two-terminal structure allows for a crossbar structure [3], dot/pillar structure [4], or even integrated into contact holes/vias [5], as shown in Figure 1.4. These structures are highly scalable, with cell sizes down to $4F^2$, where F is the technology node half pitch. They could also be stacked to increase the number of cells within the same $4F^2$ footprint. Furthermore, rather than a performance degradation, scaling the RRAM cell size was found to improve the memory window for certain types of RRAM [6]. This is due to the fact that the

conductive filament (CF) that is formed can be smaller than 10 nm diameter, as shown from current-sensing atomic force microscopy studies [7]. So reducing the cell area would not affect the CF formation, ie. no impact on the low-resistance state (LRS), but would reduce the leakage current, leading to an increased high-resistance state (HRS).

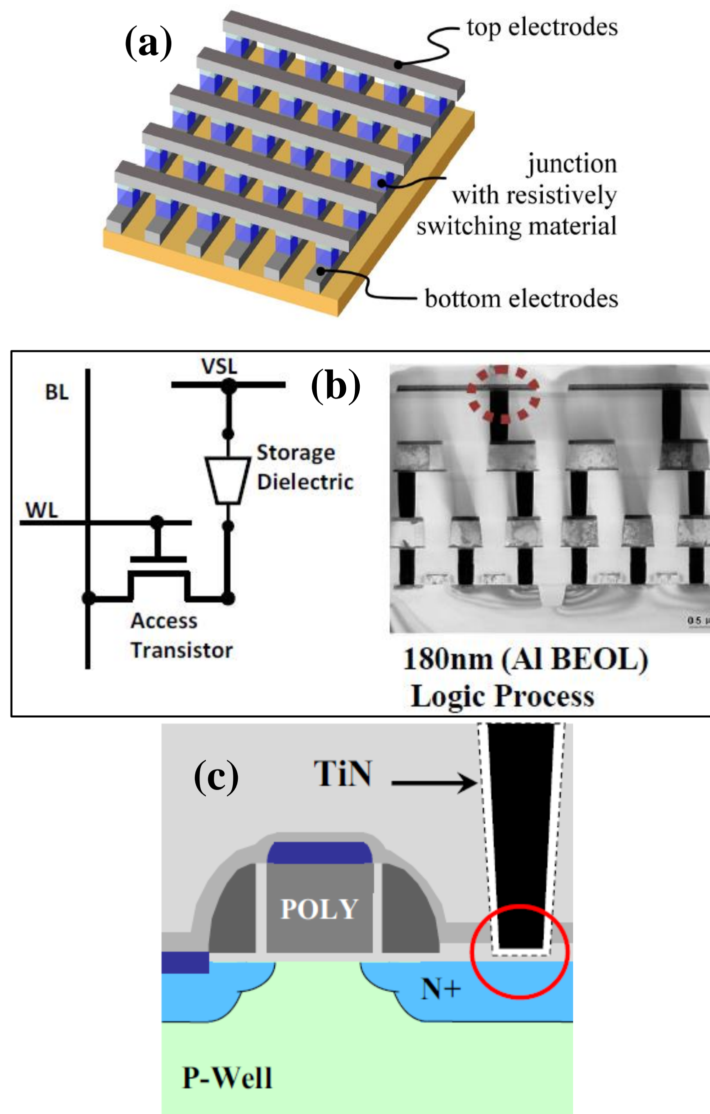

Figure 1.4. RRAM integrated into (a) crossbar structure (© 2008 IEEE) [3], (b) dot/pillar structure (© 2010 IEEE) [4], and (c) contact hole (© 2009 IEEE) [5].

In terms of performance, RRAMs are typically able to program much faster (< 100 ns pulse time) and at lower voltages (< 3 V) compared to flash memories (> 10 V with pulse time in μs). This results in a large reduction in power consumption or energy per bit. Additionally, the lower voltage requirement reduces any impact from line-to-line or cell-to-cell cross-talk. The endurance cycling of RRAMs (10^5 – 10^{12}) also far-exceed those of flash (10^4 – 10^5).

All these characteristics of RRAM make it a likely replacement for flash memory in the future. However, even though process complexity is much lower for two-terminal RRAM compared to flash memories, the choice of materials and interfaces in the MIM RRAM cell plays a vital role in determining the memory performance.

1.2. Types of RRAMs

Most RRAMs are two-terminal devices with a metal-insulator-metal (MIM) structure and are able to alter the insulator resistance to achieve different states. The resistance changes in RRAM resulting in the different memory states are induced through various methods and can be grouped according to mechanical, magnetic, thermochemical, electronic, and ionic-based RRAMs.

1.2.1. Mechanical Based

Mechanical effects take place in magneto-electro-mechanical systems (MEMS) relays, where a mechanical relay is switched between the ON and OFF states through electrostatic forces [8-9]. These memories have a massive difference between HRS and LRS since it is the difference between a short and open circuit. The cells are also able to withstand harsh environments, like high temperatures or high radiation. However, the switching speed is low, voltages and currents tend to be high, and there is also no room for multi-bit per cell. The mechanical nature of the cell also results in reliability problems, like striction, wear-and-tear, and these cells are typically too large to be considered for high density memory arrays.

1.2.2. Magnetic Based

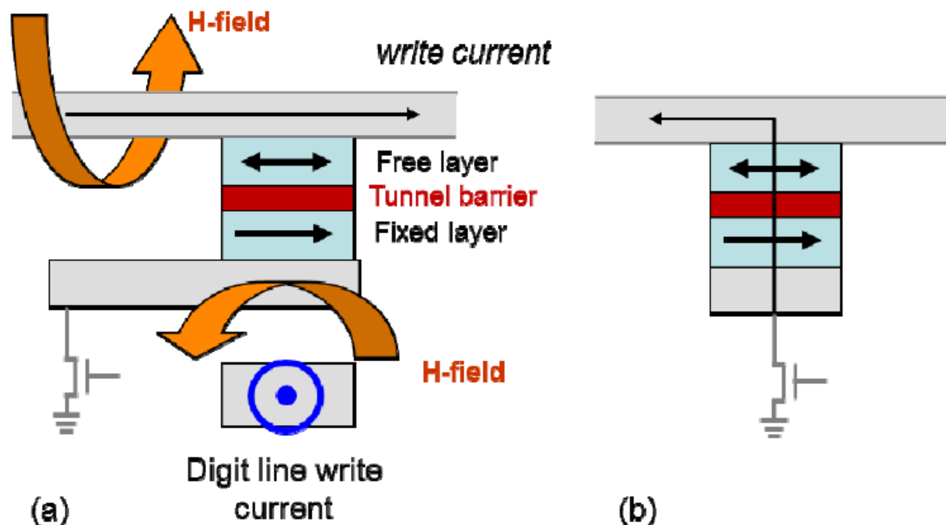

Figure 1.5. Cell diagrams of (a) toggle MRAM and (b) MTJ STT-MRAM (© 2012 IEEE) [10].

Memories employing magnetic effects, or magnetoresistive RAM (MRAM), rely on resistance change of a magnetic tunnel junction (MTJ) between two ferromagnetic electrodes [10], shown in Figure 1.5. If the electrodes are magnetized in the same direction (parallel polarization) the MTJ has a lower resistance as opposed to when they are in the opposite direction (anti-parallel polarization). Typically, one electrode has a fixed magnetization while the other is allowed to switch through the application of a magnetic field generated by passing current through nearby metal lines, as in Figure 1.5(a). In spin-torque transfer MRAM, shown in Figure 1.5(b), a polarized current is passed through the device and the magnetization is transferred through spin-torque transfer.

1.2.3. Thermochemical Based

Thermochemical effects may involve switching a material's crystal structure, between polycrystalline and amorphous, which would alter the resistance of the material. Typical material choices are chalcogenides, like GeSbTe (GST), with a typical device schematic shown in Figure 1.6. By flowing a large current density through a heater below the material, Joule heating greatly increases the temperature and destroys any crystal arrangement in the GST. Cooling the device quickly keeps the material in the amorphous phase and cooling slowly allows some crystallization to take place to form the polycrystalline phase. Such memories are thus called phase-change memories, or PCM, due to the switching between the two phases [11].

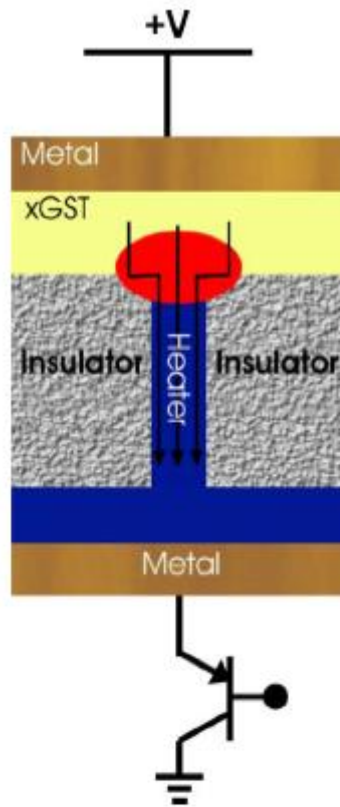

Figure 1.6. Device schematic of GeSbTe (GST) phase change memory (PCM) cell. Reproduced from [11], Copyright 2006, with permission from Elsevier.

Thermochemical effects have also been observed in transition metal oxide (TMO) switching materials, like NiO with Pt electrodes [12]. Applying a field induces a leakage current which, if current density is sufficiently high, increases the local temperature and causes a reduction of the NiO. This type of TMO reduction at high temperatures is a result of negative free energy of formation of such materials [13]. The free energy of formation is lower for TMO with lower valency, making it a more favourable phase to form when the material is at the semi-liquid state. The pure metal state may even form in some cases. This forms the basis for such memories to work. A continuous chain of localized lower valency or pure metallic TMO creates a conduction path, or conductive filament (CF). Applying a field again causes current to

flow mostly through the CF, inducing Joule heating once again which ruptures the CF due to dissolution.

1.2.4. Electronic Based

Electronic based memories involve an injection of electrons into the switching material to alter its conduction properties. The electrons may either be trapped at trapping sites within the material, like metal nanoclusters found in polymeric [14] or inorganic [15] insulators to increase the conductivity, or at a metal-semiconductor interface [16], lowering the Schottky barrier. Other materials like $SrTiO_3$ (STO) [17] would take electron injection as a form of doping, altering the conductivity as a result. These electronic based memories tend to create a conductive path throughout the entire switching material, ie. bulk effect, as opposed to memories based on CF formation, ie. local effect. Thus, there will be impact on both HRS and LRS from scaling of the memory cell area.

1.2.5. Ionic or Redox Based

Finally, ionic effects take place with movement or migration of either cations or anions with the assistance of an applied field. These memories are usually termed redox-based RRAM or redox-RRAM as the ions are formed through redox reactions.

Cation-based RRAMs [18], usually termed conductive-bridging RAM (CBRAM), electrochemical metallization (ECM) memories, or programmable metallization cell (PMC), involve an active electrode, using electrochemically active materials like Ag, Ni or Cu, an inert electrode, like Pt, W or Au, and a solid electrolyte in which the cations can conduct or migrate, which can be chalcogenide-based for high mobility, or even oxide-based. A field is applied during the filament forming process, causing dissolution of the active electrode into cations within the solid electrolyte. These cations are drifted by the field towards the inert electrode and are finally reduced by electrons from the inert electrode to form the elemental metal of the active electrode. This further progresses and gradually forms a chain of the elemental metal, resulting in a CF bridging the two electrodes, as seen in the transmission electron microscopy (TEM) image in Figure 1.7(a). During the RESET, the CF is annihilated by applying a field opposite to the forming field to dissolve the filament and drift the cations back towards the active electrode, as seen in the TEM image in Figure 1.7(b).

According to the study by Yang, *et al.* [18], the mobility of the cation in the electrolyte plays a big part in determining the direction of filament growth and

location of filament rupture. In electrolytes with high cation mobility, the cations reach the inert electrode quickly and are reduced there, resulting in a filament growing towards the active electrode. Filament rupture also occurs near the inert electrode. This is the case as seen in Figure 1.7. For low cation mobility electrolytes, the cations are too slow and get reduced near the active electrode instead and also rupture there, like in the case of α-Si electrolye cell shown in Figure 1.8.

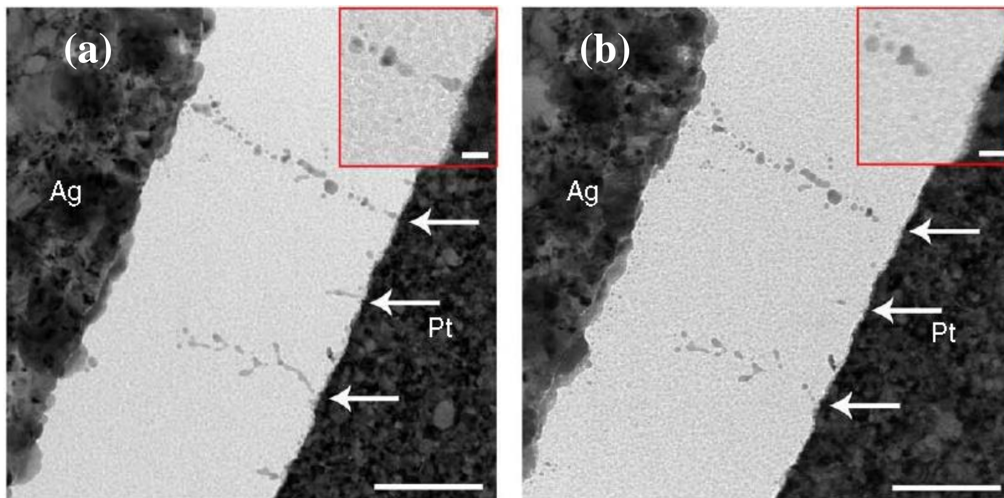

Figure 1.7. Transmission electron microscopy (TEM) images from an in-situ study of the filament formation in Pt/SiO_2/Ag RRAM cell showing the (a) formation of Ag filament after SET and (b) dissolution/annihilation of the Ag filament after RESET. Reproduced by permission from Macmillan Publishers Ltd: Nature Communications [18], copyright 2012.

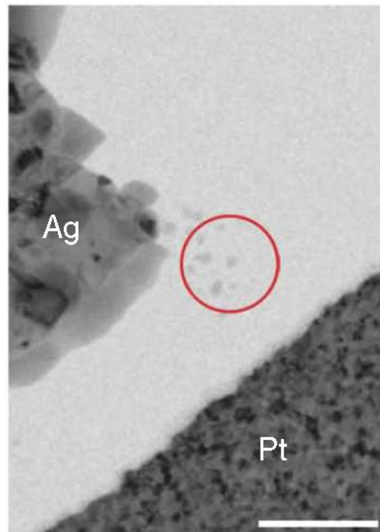

Figure 1.8. TEM image from the in-situ study of Pt/α-Si/Ag RRAM cell showing a partial Ag filament growing from Ag electrode. Reproduced by permission from Macmillan Publishers Ltd: Nature Communications [18], copyright 2012.

While cation-based RRAM rely on cation migration from the electrodes, anion-based RRAMs rely on anion migration from the switching material. Special TMOs, like HfO_2, TiO_2, Ta_2O_5, exhibit the ability to lose oxygen atoms, i.e., reduce, and create oxygen vacancies (V_o) [19]. The V_o are formed by applying a field which also drifts the oxygen ions towards the positive electrode and the V_o to the negative electrode, as shown in Figure 1.9. The V_o inside the material act as donors and facilitate electron conduction when a continuous chain of V_o forms a CF between the two electrodes. The excess oxygen atoms could be within interstitial sites of the TMO, trapped at the electrode-TMO interface or stored by the electrode. Reversing the field reduces the oxygen atoms and drifts them back to the V_o and oxidize the CF to form stoichiometric TMO again and annihilate the CF (Figure 1.10).

The ideal anode in such a case would be one with high oxygen affinity, but also be unreactive to oxygen, i.e., inert. One such electrode material commonly used is Pt. Such a material is able to accept large amounts of oxygen atoms, hold them without reacting, and then release them back into the TMO. However, the fact that inert electrodes are relatively unreactive makes the material difficult to etch and is not the ideal solution for CMOS processing, apart from the high material cost. TiN has thus been proposed and used [20-22] as an alternative for gettering and storing oxygen atom, like an oxygen reservoir. Adding a thin buffer layer of Ti below the TiN improves performance [6, 19, 23-24] due to the improved oxygen gettering properties of Ti.

The theory of oxygen vacancies forming and facilitating subsequent conduction has been shown using scanning transmission electron microscopy (STEM) on SiOCH/HfO_2/TiN RRAM cell along with high-angle annular dark-field detector (HAADF), shown in Figure 1.11(a), and electron energy loss spectroscopy (EELS) chemical mapping, shown in Figure 1.11(b), and spectra, shown in Figure 1.12 [25]. The oxygen-deficient HfO_{2-x} region is observed and identified to facilitate conduction in the LRS.

From the high-resolution TEM (HR-TEM) image of the same device (Figure 1.13), the grain boundaries of the poly-crystalline HfO_2 are also identified along with the oxygen-deficient HfO_{2-x} region and are theorized to play a role in the formation of the CF [25]. Electron conduction takes place along the grain boundaries during the forming process and provides local Joule heating to assist in reducing the HfO_2 into HfO_{2-x}, thus forming the CF.

The role of grain boundaries was also confirmed in the CS-AFM work on NiO-based RRAMs [7], where a Ni-rich phase was observed to exist at grain boundaries within the NiO film. So the CF made up of Ni precipitates is indeed formed at grain boundaries.

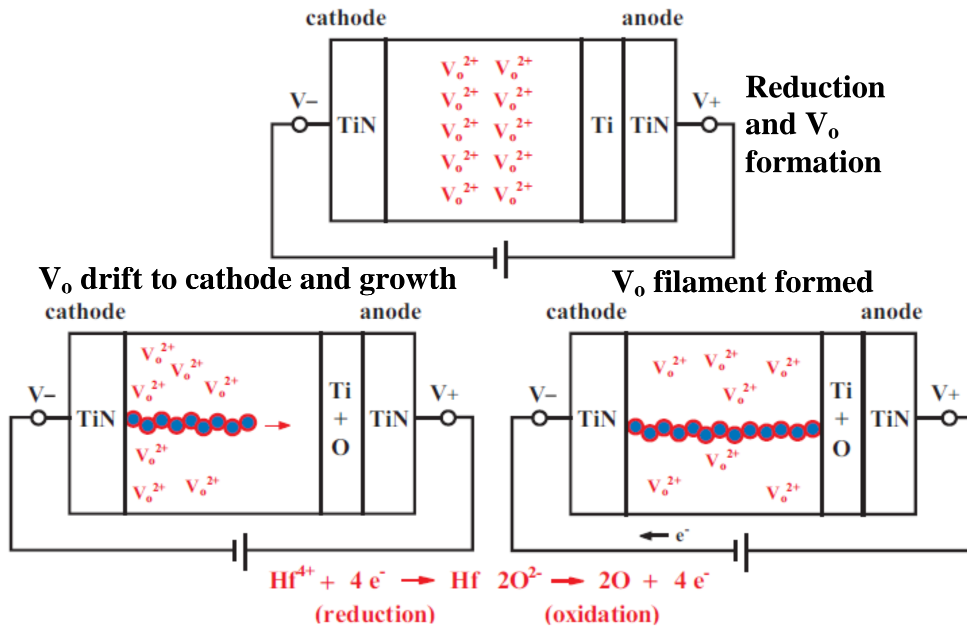

Figure 1.9. Illustration of the redox reactions occurring in TiN/HfO_2/Ti/TiN RRAM cells during the forming process (© 2011 IEEE) [19].

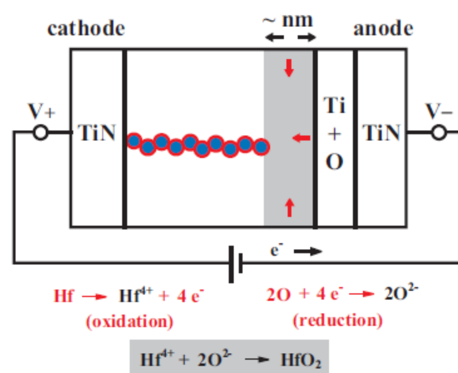

Figure 1.10. Illustration of the redox reactions occurring in TiN/HfO_2/Ti/TiN RRAM cells during the RESET process (© 2011 IEEE) [19].

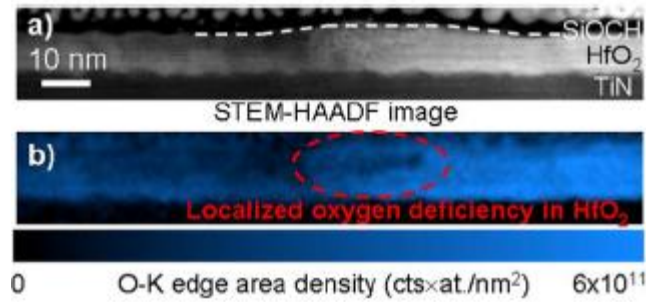

Figure 1.11. Scanning transmission electron microscopy (STEM) analyses on SiOCH/HfO_2/TiN RRAM cell using (a) high-angle annular dark-field detector (HAADF) and (b) electron energy loss spectroscopy (EELS) chemical mapping to identify the composition of the CF [25]. © IOP Publishing. Reproduced with permission. All rights reserved.

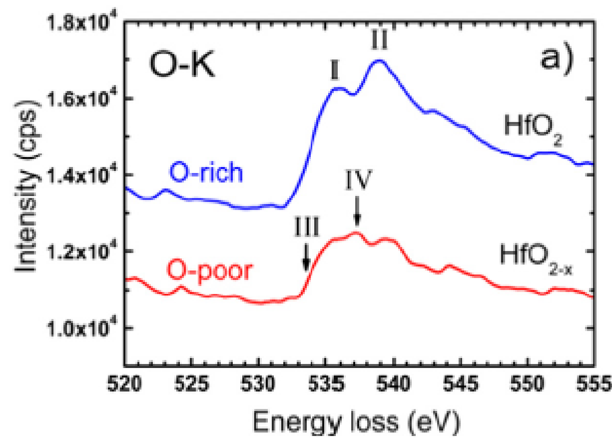

Figure 1.12. The EELS spectra of oxygen-rich HfO_2 and oxygen-deficient HfO_{2-x} regions within the SiOCH/HfO_2/TiN RRAM cell [25]. © IOP Publishing. Reproduced with permission. All rights reserved.

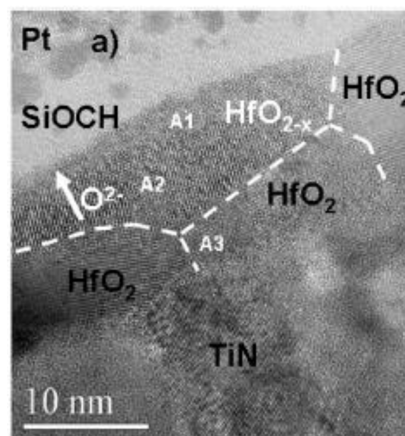

Figure 1.13. The high-resolution TEM (HR-TEM) image of the SiOCH/HfO_2/TiN RRAM cell, showing the oxygen-rich HfO_2 region, oxygen-deficient HfO_{2-x} region and the grain boundaries [25]. © IOP Publishing. Reproduced with permission. All rights reserved.

An alternate operating theory, although still based on V_o formation, involves a Ta_2O_5/TaO_2 bilayer [26], shown in Figure 1.14. A negative top electrode (TE) bias reduces the oxygen-rich Ta_2O_5 layer to form V_o, and the oxygen is stored in the TaO_2. The V_o then allows current to flow between the two electrodes through the TaO_2 with medium resistance.

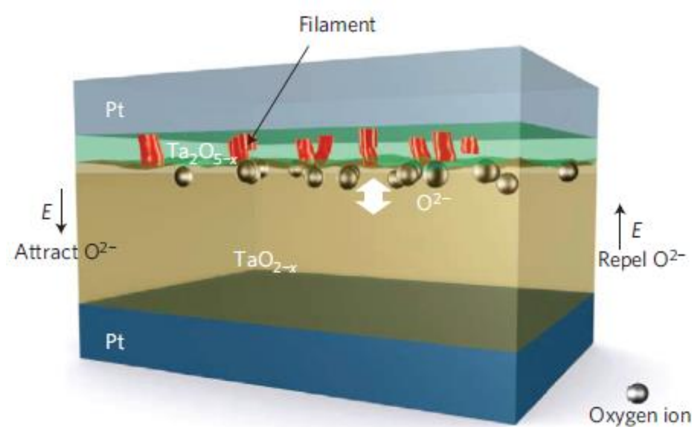

Figure 1.14. $Pt/TaO_2/Ta_2O_5/Pt$ cell schematic showing operating principle. Reproduced by permission from Macmillan Publishers Ltd: Nature Materials [26], copyright 2011.

1.3. Redox-Based RRAM Basic Operation

In redox-RRAMs, voltage bias is typically applied to the active electrode, referred to as the top electrode (TE), while grounding the inert electrode, referred to as the bottom electrode (BE). Most redox-RRAMs require a forming process, or initialization, of the memory cell, whereby a high positive voltage is applied to the TE of pristine devices to form the CF, shown in red in Figure 1.15. Such a forming process would result in an abrupt current increase

as the CF is rapidly formed and thus requires a current compliance to be in place to protect the device from permanent damage affecting the memory window and yield [27].

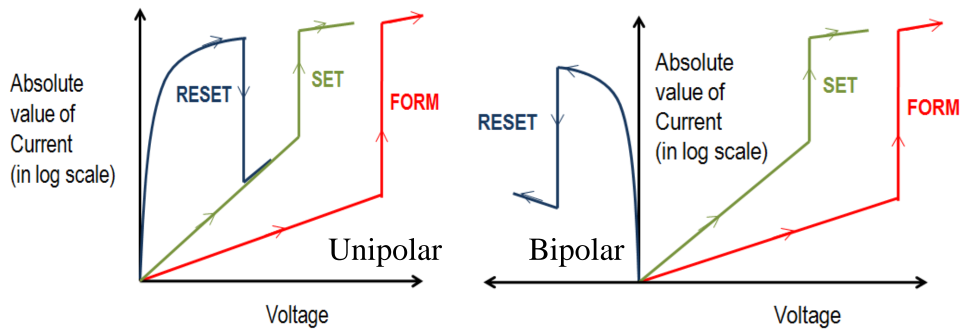

Figure 1.15. Typical I-V characteristics of unipolar and bipolar RRAMs.

After the forming process, the RRAM cell is read for switching. The SET process creates the CF, resulting in a high current jump and putting the RRAM into the LRS, while the RESET process annihilates the CF, with the RRAM seeing a current drop and goes into the HRS. Most TMO-based RRAMs have two different switching or operating regimes: unipolar and bipolar, as can be seen in Figure 1.15 where the typical I-V characteristics are illustrated. Unipolar, or sometimes known as non-polar, RRAMs have the same applied field direction regardless of SET or RESET, while bipolar have opposite field directions for SET and RESET.

As the field is always in the same direction for unipolar RRAMs, the operation relies more on thermochemical effects during the RESET cycle to heat the CF, diffuse the ions and annihilate the CF, since electronic and ionic effects need opposite field directions to drift electrons or ions back and forth

as with bipolar RRAM. The RESET cycle for the unipolar RRAM would usually involve a high current density inducing Joule heating and dissolution of the CF. So RESET current is usually higher than the compliance current of the SET cycle.

1.4. Comparison of RRAMs

Table 1.1 summarizes key features of three major contenders of emerging memories, PCM, MRAM and redox RRAM. The key features include the cell size, programming energy, read/write time, and endurance. These key features are compared with and benchmarked against those of NAND Flash and DRAMs.

Table 1.1. Comparison of some key features of NAND Flash, DRAM, PCM, MRAM and redox RRAM [28], with colors indicating good (green), fair (yellow) and poor (red) performance.

	Planar NAND Flash	DRAM	PCM	MRAM	Redox RRAM
Cell Size	$4F^2$	$6F^2$	$4F^2$	$6F^2$	$4F^2$
Programming Energy	Med	High	High	Med	Medium to Low
Read Time	~10 µs (page)	~10 ns	< 100ns	< 30 ns	< 50 ns
Write Time	~10 ms (page)	~10 ns	> 100 ns	< 10 ns	< 10 ns
Endurance	$< 10^5$	$> 10^{15}$	10^8	$> 10^{15}$	$> 10^8$

Although NAND Flash can be achieved in $4F^2$ cell size, the programming energy tends to be fairly high due to the large voltage required, typically 10-20 V. Most significantly, it requires read and write at the page level which affects the actual time for read/write even though each cell can be read/programmed at ~10 ns, and the endurance is typically limited to $\sim 10^5$ cycles. DRAM can read/write in ~10 ns with endurance over 10^{15} cycles, but has a larger cell size and requires refresh cycles which increases the programming energy. PCM has $4F^2$ cell size and short read time, with endurance able to do better than NAND Flash, although not as good as DRAM. However, the high programming current needed to change the material phase, which could be up to several milliamperes, causes high programming energy, and there could also be issues of thermal disturb between neighboring cells. MRAM is a strong candidate for DRAM and NAND Flash replacement, with short read/write times and endurance high enough to match DRAM. But the memory density is still unable to match that of NAND Flash, and furthermore, there is no option of multi-level cell with the MRAM. Although redox RRAM is unable to match the high endurance of DRAM, it can either match or surpass the key features of NAND Flash, with its small cell size, low programming energy, fast read/write and higher endurance. Thus, it is a good candidate for NAND Flash replacement. However, the challenges faced by redox RRAM are the large variations of the on/off currents and the need for a larger memory window if multi-level cells are to be achieved [28].

Table 1.2. Comparison of published material stacks of redox RRAM featuring TaO_x, HfO_x, TiO_x, and WO_x (© A. Prakash, *et al.*, Springer 2013) [29].

Device structure	Device size (μm^2)	Set/reset voltage (V)	Current compliance (μA)	Retention (s)	Resistance ratio	Endurance (cycles)
$W/TiO_x/TaO_x/TiN$	0.15 × 0.15	3.0/−3.0	80	>3 h, 85°C	100	10^4
Ir or $Pt/Ta_2O_{5-\delta}Ta_{2-\beta}/Pt$	0.5 × 0.5	−1/+0.8	80/150	$>10^7$	~10	10^9
$Pt/Ta_2O_{5-x}/TaO_{2-x}/Pt$	50 × 50-0.03 × 0.03	−2.0/+2.0	40-200	10 years, 85°C	~10	10^{12}
$Ru/Ta_2O_5/TiO_2/Ru$	4 × 4	+2.7/−1.0	~100	$>10^6$	~50	10^6
$TiN/Ti/HfO_x/TiN$	~0.4 × 0.4-0.03 × 0.03	1.0/−1.5	40, 200	$>10^4$, 200°C	~100	10^8
Hf, Ti, $Ta/HfO_2/TiN$	0.04 × 0.04	+1.8/−3	100	$>10^4$, 200°C	~10	10^{10}
$TiN/Hf/HfO_2/TiN$	0.01 × 0.01	±0.5	<80	10^5, 200°C	~100	5×10^7
$Pt/ZrO_x/HfO_x/TiN$	0.05 × 0.05	0.6/−1.5	50	10^5, 125°C	~100	10^6
$TiN/WO_x/TiN$	0.06 × 0.06	−1.4/+1.6	400	2×10^3 h, 150°C	~10	10^6

Among redox RRAMs, material stacks incorporating TaO_x, HfO_x, TiO_x, and WO_x have been intensively studied. These stacks all show good results, especially for TaO_x and HfO_x-based stacks (Table 1.2). But the TaO_x-based RRAMs often use Pt, Ru or Ir as the electrode, which are either expensive and/or not CMOS-friendly. Even when using CMOS available materials, certain performance may be impacted, like the $W/TiO_x/TaO_x/TiN$ stack which has retention and endurance issues. HfO_x-based stacks have the best CMOS compatibility, using CMOS-available materials and still showing mostly better performance. Most notably, the $TiN/Ti/HfO_2/TiN$ RRAM cell when integrated with transistors [6] show promising results, with resistance ratio ~100x and endurance > 10^6, shown in Figure 1.16. This RRAM cell was also shown to be able to switch with 5 ns pulse. However, from the LRS and HRS resistance distributions taken from the RRAMs within a 1 kbit array, shown in Figure 1.17, a large variation was observed [30].

So the HfO_2-based RRAMs show the most promise for a fully CMOS compatible RRAM cell with performance that could match or surpass that of NAND Flash. However, this material stack still suffers from large resistance

variation and more work needs to be done to reduce this variation or to increase the memory window to compensate for it.

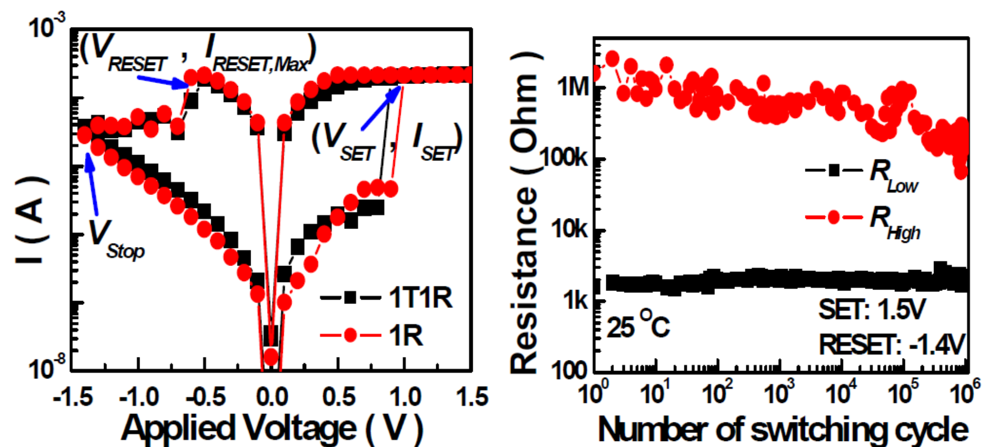

Figure 1.16. (Left) I-V sweep characteristics and (right) AC endurance cycling of $TiN/Ti/HfO_2/TiN$ RRAM cell (© 2008 IEEE) [6].

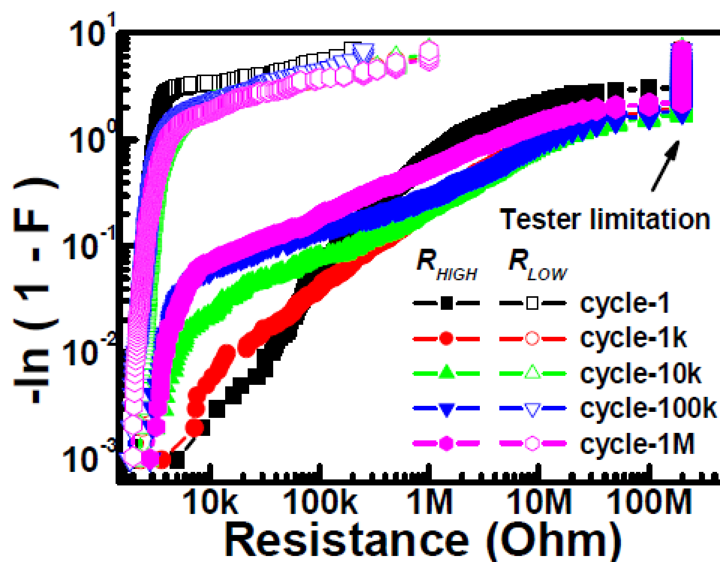

Figure 1.17. Resistance distribution of HRS (R_{HIGH}) and LRS (R_{LOW}) from a 1 kbit array of $TiN/Ti/HfO_2/TiN$ RRAM cells integrated with 0.18 µm CMOS transistors (© 2009 IEEE) [30].

1.5. The Need for a Select Device

Although RRAMs have a simple two-terminal MIM structure, it is this fact that such RRAMs would require a select device. Without such a device to select one particular cell, read errors would occur through a "sneak path" of the read current in large RRAM arrays. This is illustrated in Figure 1.18. When there are cells in LRS surrounding a cell in HRS, reading the cell in HRS would bring about a "sneak path", whereby the cell to be read is bypassed due to a current path passing through at least 3 LRS cells with lower resistance. The HRS would therefore be read as LRS, and hence the need for a device to allow selecting of only one RRAM cell.

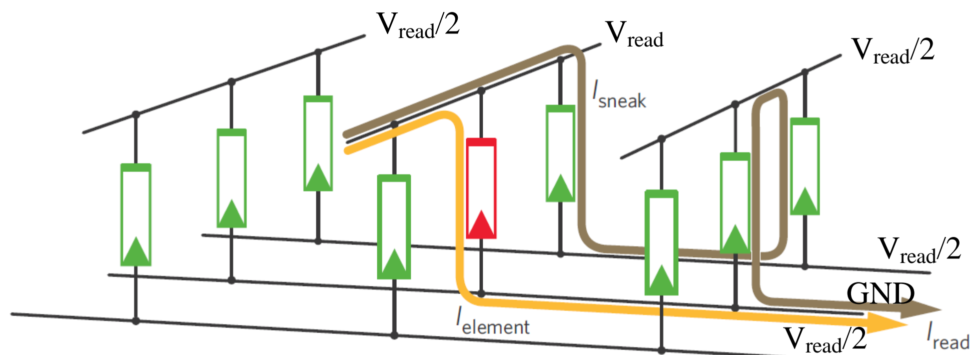

Figure 1.18. Illustration of the simplest case of a sneak path. The green diagrams indicate cells in LRS, and the red diagram indicates a cell in HRS. Reading the single HRS cell may cause current to "sneak" through at least 3 LRS cells, giving the read error that the cell to be read is in LRS. Reproduced by permission from Macmillan Publishers Ltd: Nature Materials [31], copyright 2010.

The select device typically comes in the form of a transistor or diode. Diodes can be done in a smaller footprint, but unless it is di-directional, like a varistor, it can only be used for unipolar RRAMs. Since diodes have a turn on

voltage (V_{on}), the selected cell should have a voltage drop more than V_{on} while the other cells should have voltage drop less than V_{on}. This can be done by using the biases shown in Figure 1.18. The selected cell top line would be read voltage (V_{read}) and bottom line would be at GND, while the other lines are at $V_{read}/2$. So as long as the diode V_{on} is between $V_{read}/2$ and V_{read}, the diode can be used as a select device in this case.

Transistors are by far the most versatile as select device, in the sense that the current is bi-directional and can be controlled by the gate bias to prevent unwanted current surge from damaging the RRAM cell. The 1-transistor-1-resistor (1T1R) cell also requires no special biasing of the unselected bit lines. But the disadvantage is the large transistor footprint compared to the RRAM cell which limits the scalability of the 1T1R cell. However, since the vertical silicon nanowire field-effect transistor (VSNWFET) is able to be defined in $4F^2$ area [32], as illustrated in Figure 1.19, using it as the transistor would not be limiting the RRAM cell scalability, and would result in a 1T1R cell with $4F^2$ footprint. Furthermore, the gate-all-around (GAA) structure enhances the gate control, which reduces short-channel effects, lowers the off-state current, and allows for a steeper subthreshold slope. Figure 1.20 shows an illustration of a 1T1R 4 x 4 array using VSNWFET as the select device. Each column would have a common top contact to the RRAM, forming the bit line (BL), and each row would have common gates, forming the word line (WL). Select line (SL) would be all the contacts to the bottom of the nanowires. Simply applying transistor turn-on voltage to one WL and RRAM read voltage to one BL, keeping all other lines including SL grounded, would select only one cell.

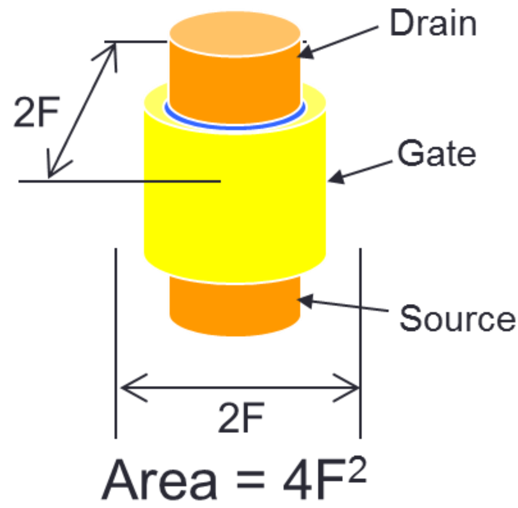

Figure 1.19. Illustration showing the smallest device area, or footprint, of the vertical silicon nanowire FET.

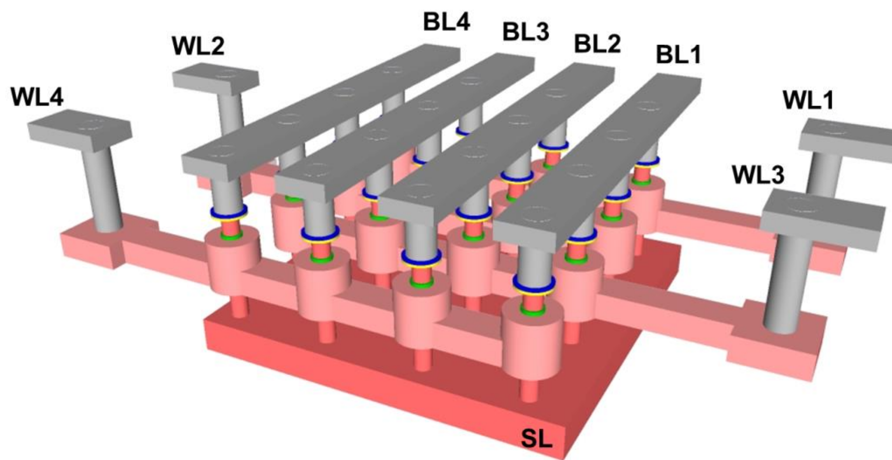

Figure 1.20. Three-dimensional schematic of a 1T1R 4 x 4 array, with each cell occupying $4F^2$ area. The gates of each row form the word lines (WL), the contacts to the RRAM on top of the nanowire in each column form the bit lines (BL), and the select line (SL) is common contact to the bottom of each nanowire.

1.6. Conduction Mechanisms

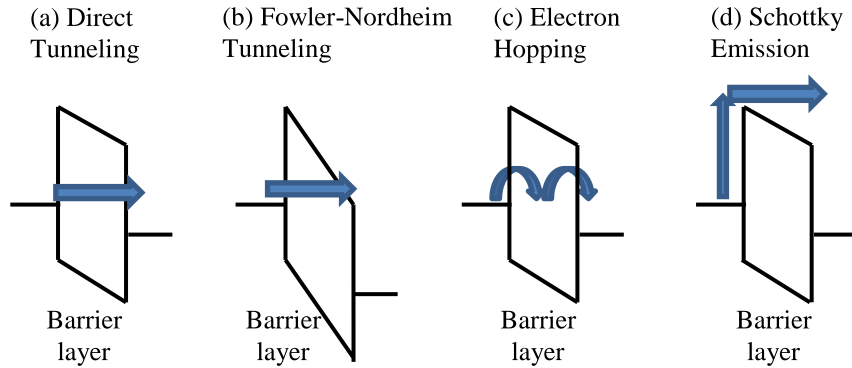

Figure 1.21. Band diagrams illustrating the conduction mechanism for (a) direct tunneling, (b) Fowler-Nordheim tunneling, (c) electron hopping, and (d) Schottky emission.

The conduction through a barrier layer can be described through various models or equations [33-35], as illustrated with band diagrams in Figure 1.21.

Under direct tunneling, the tunneling barrier is rectangular or trapezoidal and the electrons tunnel directly tunnel through the entire barrier [Figure 1.21(a)]. The current-voltage relation can be described by the following equation [33]:

$$\ln\left(\frac{I}{V^2}\right) \propto \ln\left(\frac{1}{V}\right) - \frac{2d\sqrt{2m_e\phi}}{\hbar}, \tag{1}$$

where d is the tunneling barrier width, m_e is the electron effective mass, and ϕ is the barrier height.

For Fowler-Nordheim (FN) tunneling, the electrons tunnel into the conduction band of the barrier layer instead [Figure 1.21(b)], which occurs under high electric fields, so the barrier is triangular and is described by the following equation [33]:

$$\ln\left(\frac{I}{V^2}\right) \propto -\frac{4d\sqrt{2m_e\phi^3}}{3\hbar q}\left(\frac{1}{V}\right), \tag{2}$$

where q is the electronic charge.

So a plot of $\ln(I/V^2)$–$1/V$ should reveal the conduction mechanism involved. A linear plot with negative slope would indicate FN tunneling, while a logarithmic curve would indicate direct tunneling.

Under Mott's Law, conductivity under low field can be described by [34]:

$$\sigma \approx \sigma_0 exp\left[-\left(\frac{T_0}{T}\right)^{-1/4}\right]. \tag{3}$$

So plotting $\ln(R)$-$T^{-1/4}$ should yield a linear curve if conduction is dominated by electron hopping.

Under Schottky emission, the current density, J, at temperature, T, and under voltage bias, V, is described by [35]:

$$J \approx A^{*}T^2 exp\left[\frac{-q\left(\phi_B-\sqrt{\frac{qV}{4\pi\varepsilon_r\varepsilon_0 d}}\right)}{k_B T}\right], \tag{4}$$

where A^* is the effective Richardson constant, q the electronic charge, ϕ_B the barrier height, ε_r the dielectric constant, ε_0 the permittivity of vacuum space, d the barrier width, and k_B the Boltzmann constant. Using:

$$J = \frac{I}{A}, \tag{5}$$

where A is the cell area, Equation (4) can be re-arranged to the following:

$$ln(I) = \sqrt{\frac{q}{4\pi\varepsilon_r\varepsilon_0 d}}\frac{q}{k_BT}\sqrt{V} + ln(AA^*T^2) - \frac{q\phi_B}{k_BT}, \tag{6}$$

$$ln\left(\frac{I}{T^2}\right) = \frac{q\left(\sqrt{\frac{qV}{4\pi\varepsilon_r\varepsilon_0 d}} - \phi_B\right)}{k_B}\frac{1}{T} + ln(AA^*). \tag{7}$$

Based on Equations (6)-(7) above, the ln(I)-$V^{1/2}$ and ln(I/T^2)-1/T plots should yield linear curves if the conduction is dominated by Schottky emission. From the intercept of the ln(I)-$V^{1/2}$ plot, the barrier height, ϕ_B, can be calculated from Equation (8) below, based on Equation (6):

$$\phi_B = \frac{k_BT}{q}[ln(AA^*T^2) - Intercept]. \tag{8}$$

From the slope of the ln(I)-$V^{1/2}$ plot, the barrier width, d, can also be estimated from Equation (6) and knowing the value of ε_r, according to:

$$d = \frac{q}{4\pi\varepsilon_r\varepsilon_0}\left(\frac{q}{k_BT.Slope}\right)^2. \tag{9}$$

1.7. Atomic Layer Deposition (ALD)

Atomic layer deposition (ALD) is a chemical vapor deposition (CVD) process that involves saturating gas-solid reactions of at least two chemicals, often termed precursors. The precursors are pulsed in a cyclic manner as illustrated in the example found in Figure 1.22 for ALD Al_2O_3. The first step involves the pulsing of precursor A which will react with the substrate surface and be chemisorbed onto the surface. Next, the unreacted precursor is purged, along with the gaseous by-products of the first reaction and any physisorbed precursor. In the third step, precursor B is pulsed, which will react with the previously chemisorbed layer. Finally, another purge is done to remove excess precursor, physisorbed precursor and reaction by-products [36-37].

By repeating the four ALD steps, an ALD film is deposited monolayer by monolayer, with each reaction being self-limited or self-terminating, resulting in a highly conformal, uniform film and controllable process [36-37]. The process temperatures can also be much lower than that of CVD. This makes ALD a good deposition method for RRAM layers as the resulting films are uniform, with control over the stoichiometry and also with possibility of doping or mixing of films, like alternating HfO_2 and Al_2O_3 monolayers to form HfAlO.

However, ALD often introduces impurities or contaminants from many possible sources: multiple reactions with precursors or by-products occurring, physisorbtion or chemisorbtion of by-products, decomposition of precursors, etc. As such, careful selection of precursors and also deposition conditions

need to be made to ensure high purity of the films. ALD usually requires thermally stable precursors with sufficient volatility to ensure fast transport to the substrate surface while avoiding condensation or decomposition. The reactions should also be self-limited, irreversible, complete, and the resulting by-products volatile and relatively unreactive [37].

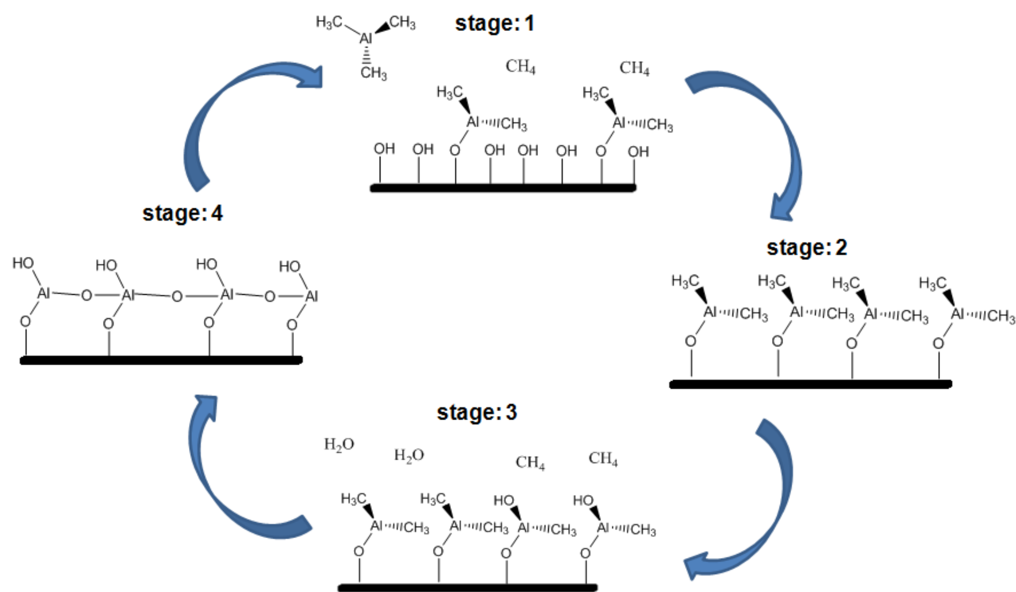

Figure 1.22. Example of the cycling steps in the atomic layer deposition (ALD) of Al_2O_3 layer using trimethylaluminum and H_2O (© H. Moshe, *et al.*, InTech 2013) [36].

Figure 1.23 shows a schematic of the ALD reactions in each half cycle of ALD HfO_2 using tetrakis(methylethylamido)hafnium (TEMAH) and H_2O as the precursors [38], which would be used in the work present in this thesis. The first reaction takes place after TEMAH is pulsed into the ALD reaction chamber and involves the chemisorbtion of TEMAH to the surface. Surface hydroxyls react with two of the alkylamine ligands in TEMAH and bonds the Hf to the O atoms, forming volatile ethylmethyl amine by-products, or

HNEtMe, in the process. The second reaction takes place after TEMAH is purged and H_2O pulsed into the chamber and involves H_2O reacting with the remaining two alkylamino ligands still bonded to Hf. This would bond hydroxyls to Hf and again forms dialkylamine by-products. Figure 1.24 shows a similar schematic for ALD HfO_2 using TEMAH precursor, but instead uses ozone, or O_3, as the oxidant [38]. In this case, after the initial chemisorbtion of TEMAH onto the surface, O_3 injection into the chamber would also cleave the Hf-N bonds connecting the alkylamino ligands to Hf, but instead producing radicials, *NEtMe. These radicals are unstable and would react with the highly reactive O_3 to form other by-products like CO_2, H_2O, CH_2O, NO, NO_2, etc. The resulting surface is –O–, where the O has an unpaired electron. This would then cleave the Hf-N bond during the next half cycle when TEMAH is again introduced into the reaction chamber, leaving a chemisorbed TEMAH ready for the next half cycle. Because O_3 is reactive, it tends to produce many carbon-containing by-products, like CO and CO_2, and these by-products may get introduced into the deposited HfO_2 films. So the resultant films from using O_3 oxidant tend to contain higher carbon content.

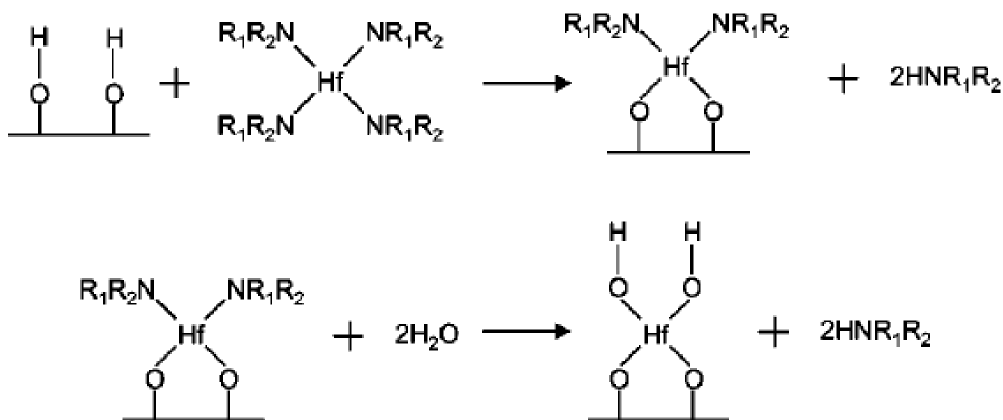

Figure 1.23. Schematic of the ALD reactions in each half cycle of ALD HfO_2 using tetrakis(ethylmethylamido)hafnium (where R_1 is a methyl ligand and R_2 an ethyl ligand) and H_2O as the precursors [38]. Reproduced by permission of The Electrochemical Society (© 2005).

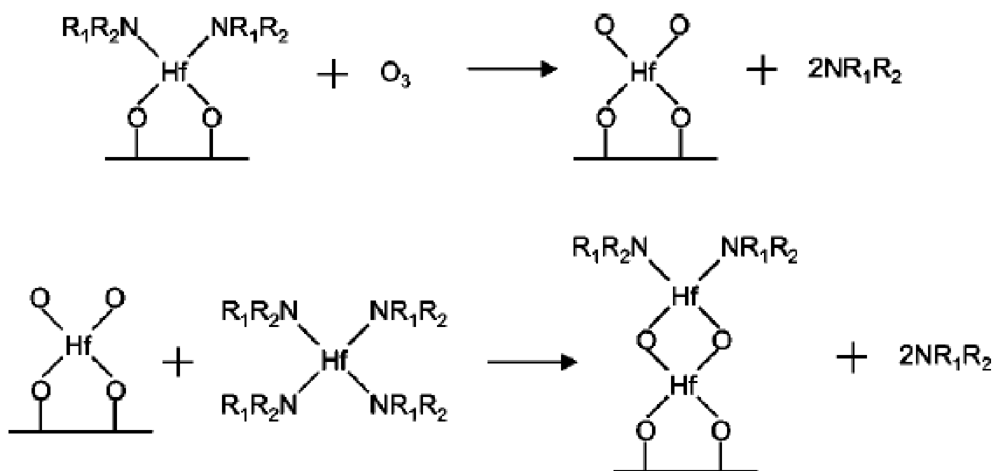

Figure 1.24. Schematic of the ALD reactions in each half cycle of ALD HfO_2 using tetrakis(ethylmethylamido)hafnium (where R_1 is a methyl ligand and R_2 an ethyl ligand) and O_3 as the precursors [38]. Reproduced by permission of The Electrochemical Society (© 2005).

1.8. Objectives of This Study

The objective of the work presented in this thesis is to further improve the HfO_2-based RRAM by increasing the memory window so as to make it more immune to resistance variations, or by reducing the variation itself. The approaches to achieving the objective involve (i) the use of transistor as a selector, (ii) exploration and optimization of a variety of electrode materials, and (iii) ALD engineering of HfO_2. To ensure future ease-of-integration, measures have been taken to ensure maximum compatibility with CMOS processes.

1.9. Overview of Dissertation

This thesis is organized into three main parts, dealing with respectively, (i) vertical silicon nanowire FET as the selector, (ii) electrode engineering with the focus on the bottom electrode materials, and (iii) material engineering of HfO_2 switching oxide through optimizing the ALD process.

Chapter 2 introduces the work on integrating the TiN/Ni/HfO_2/n^+-Si RRAM cell onto the vertical silicon nanowire FET to achieve a 1-transistor-1-resistor (1T1R) cell within a $4F^2$ footprint, where F is the half-pitch. The 1T1R cell was able to operate in three different modes: bipolar, unipolar, and bipolar with low current switching. Most notable is the bipolar mode, where a 100x memory window was observed.

Chapter 3 presents a study on using Ni-silicide as the bottom electrode of RRAM cells, with TiN as the top electrode and HfO_2 as the switching material. The performance dependence on Ni concentration in the Ni-silicide bottom electrode is discussed, along with the observation of low current switching in certain devices.

Chapter 4 compares various ALD processes used to deposit HfO_2 in TiN/Ti/HfO_2/TiN RRAM cells and describes a new ALD process involving the use of two precursors, or oxidants, and higher substrate temperature to improve the material quality and increase grain sizes.

Finally, Chapter 5 summarizes the work presented and provides recommendations for future work.

Chapter 2 : RRAM Integration with Vertical Si Nanowire FET

Integrating the RRAM cell with the VSNWFET not only allows such a 1T1R cell to have a small footprint of $4F^2$, the excellent electrical performance of the VSNWFET also provide low off state current and steep subthreshold slope. The VSNWFET also limits the current passing through the RRAM cell, effectively protecting the cell from current surges. Most notably, the small diameter of the VSNWFET should also help to scale the cell area when used as the BE. Scaling of the RRAM cell size was found to increase the memory window [19], due to the reduction of the RRAM off-state leakage current but with little impact to the on-state current.

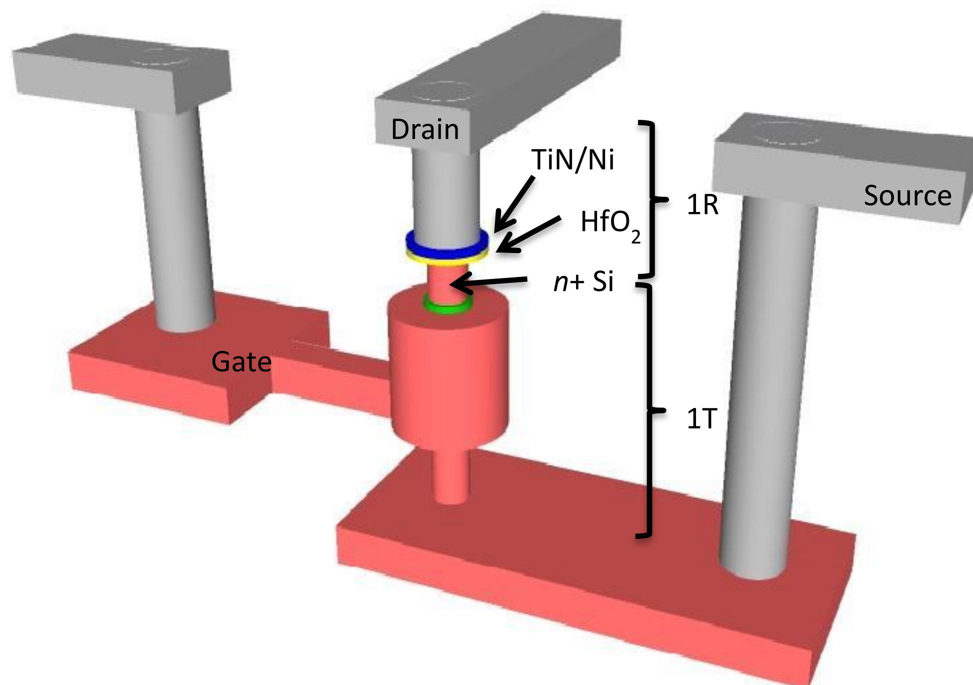

Figure 2.1. Three-dimensional schematic of a single 1T1R cell with TiN/Ni/HfO_2/n^+-Si RRAM stack.

This chapter describes the work on integrating a TiN/Ni/HfO_2/n^+-Si RRAM cell onto the VSNWFET and using the n^+ drain as the BE. The schematic of this 1T1R cell is shown in Figure 2.1. Such a cell was found to switch in three different modes: (I) unipolar, (II) bipolar, and (III) bipolar with low current switching, with Mode II showing the most stable switching with lower variations and larger memory window of 100x.

2.1. Device Fabrication

The 1T1R devices were fabricated on 8-inch *p*-type (~10^5 cm^{-3}) silicon wafers following the fabrication steps schematically shown in Figure 2.2 and with scanning electron microscope (SEM) images shown in Figure 2.3. First, a silicon nitride (SiN) hard mask was deposited and pillar dots were patterned using deep ultraviolet (DUV) lithography. After a photoresist trimming step was done in O_2 plasma to further reduce the diameter, the hard mask and ~400nm of silicon was etched using deep reactive ion etching (DRIE) in SF_6 chemistry to define vertical nanowires, with SEM image shown in Figure 2.3(a). The nanowires were then implanted with As, as in Figure 2.2(a), using the hard mask to prevent the top from being implanyed. SiO_2 was then deposited by plasma-enhanced CVD (PECVD) and partially etched in dilute HF (DHF) to remove SiO_2 from the sidewalls and only leave a layer on planar regions [Figure 2.2(b)]. Next, amorphous silicon was deposited by low pressure CVD (LPCVD), implanted with phosphorous and annealed to form poly-silicon *n*-type gate [Figure 2.2(c)]. This was followed by deposition of

SiO_2 and partial etch to expose the tip of the nanowire covered by poly-silicon [Figure 2.2(d)]. The exposed poly-silicon was then selectively removed in tetra-methyl ammonium hydroxide (TMAH) solution, leaving a structure shown in Figure 2.3(b), and the tip of the nanowire implanted with As at a tilted angle for junction self-alignment with the gate [Figure 2.2(e)]. A SiN spacer was then formed to encapsulate the nanowire tip and the SiO_2 removed in DHF. Patterning and etch was then performed to define the gate [Figure 2.2(f) and Figure 2.3(c)]. A thick layer of SiO_2 was then deposited and planarized with chemical-mechanical polishing (CMP) to expose the top of the nanowire, as shown in Figure 2.2(g) and Figure 2.3(d). The smallest nanowire tip size measured from SEM is 37 nm. The RRAM stack of 4 nm HfO_2, 5 nm Ni and 100 nm TiN were deposited by PVD sputtering and patterned using the pillar dot mask [Figure 2.2(h)]. The RRAM cell was then dry etched and covered with a layer of SiO_2 [Figure 2.2(i)]. Finally, contact holes were etched before standard metallization using TaN/Al/TaN [Figures 2.2(j), 2.3(e) and 2.3(f)].

The resultant 1T1R structure is shown in the transmission electron microscope (TEM) images of Figure 2.4. A sample with wider nanowire of ~80 nm was used to facilitate sample preparation and ensure clearer imaging of the entire structure. The n^+ drain of the VSNWFET is used as the BE of the TiN/Ni/HfO_2/n^+-Si RRAM cell.

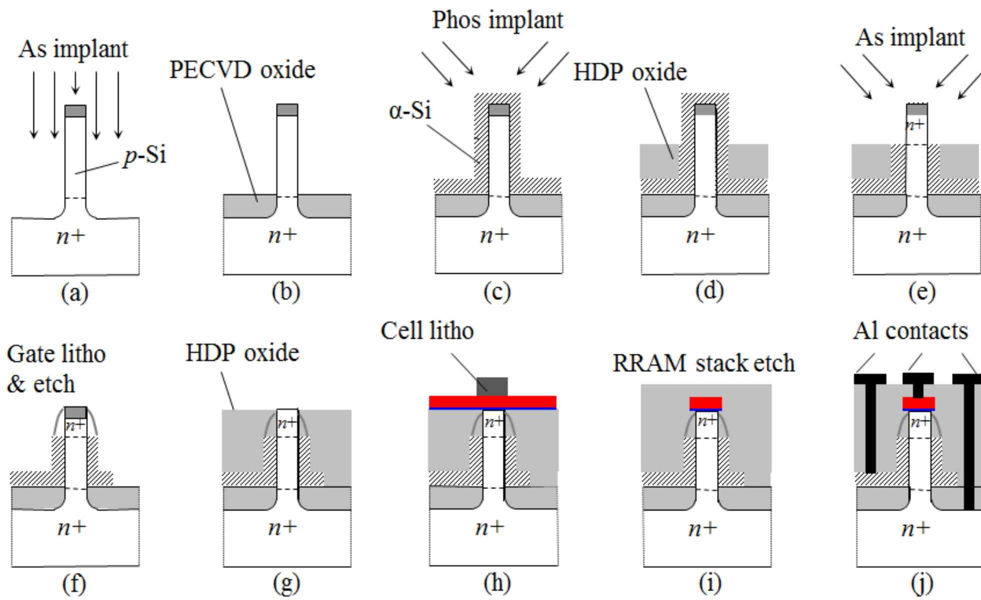

Figure 2.2. Fabrication schematic showing (a)-(f) standard VSNWFET process up to gate definition, (g) oxide deposition and CMP to expose nanowire tip, (h) RRAM cell deposition and patterning, (i) RRAM cell etch and oxide deposition, and (j) standard TaN/Al/TaN metallization.

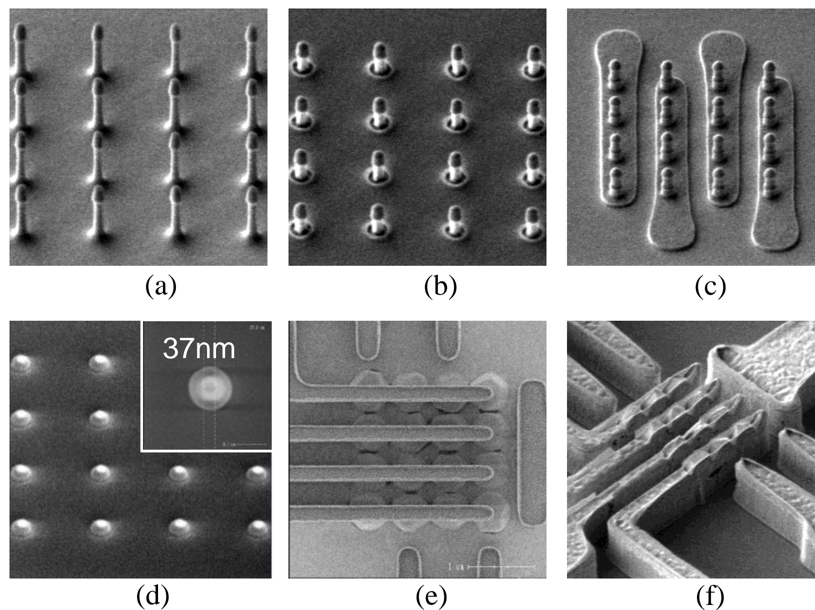

Figure 2.3. Scanning electron microscope (SEM) images taken after (a) vertical nanowire definition, (b) gate tip removal, (c), gate definition, (d) nanowire tip exposure with CMP, and (e)-(f) metallization.

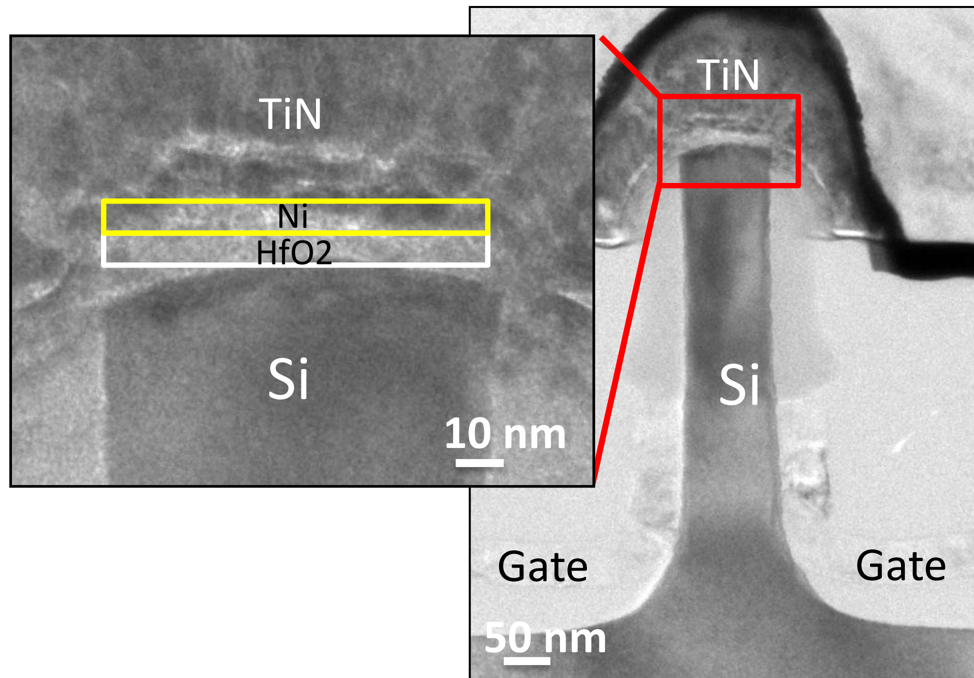

Figure 2.4. Transmission electron microscope (TEM) image showing a single VSNWFET 1T1R cell, with the inset showing the high-magnification image of the RRAM stack on top of the nanowire.

2.2. Results and Discussion

Figure 2.5 shows the transfer characteristics of the VSNWFET devices without RRAM cell that were fabricated together with the 1T1R cells. The performance of the VSNWFET shows on/off ratio of over 6 orders, subthreshold swing (SS) of 66 mV/decade and low drain-induced barrier lowering (DIBL) of 27 mV/V. The performance is either on par or better than those of state-of-the-art transistors either in production or near-production, like Samsung's 20 nm bulk planar [39], Intel's 22 nm bulk FinFET [40], and IBM/GlobaFoundries' 28 nm fully-depleted silicon-on-insulator (FDSOI) [41], even without the use of high-κ/metal-gate. However, to be fair, the gate length of the VSNWFET is longer than the above-mentioned transistors, and should therefore be more immune to short-channel effects (SCE). It should

still be noted that a longer gate for the VSNWFET does not increase transistor footprint, so it can have more immunity to SCE within the same footprint. Regardless, the transistor performance is sufficiently good to be used in the 1T1R cell. Comparing the transistor-only (1T) output characteristics with that of a 1T1R cell with RRAM cell deliberately broken, shown in Figure 2.6, there is little difference between the two. This shows that the RRAM cell has little impact on the transistor performance. It should be noted that the transistor threshold voltage is negative, making it a normally-on device. However, the threshold voltage can be tuned through gate doping or through metal gate.

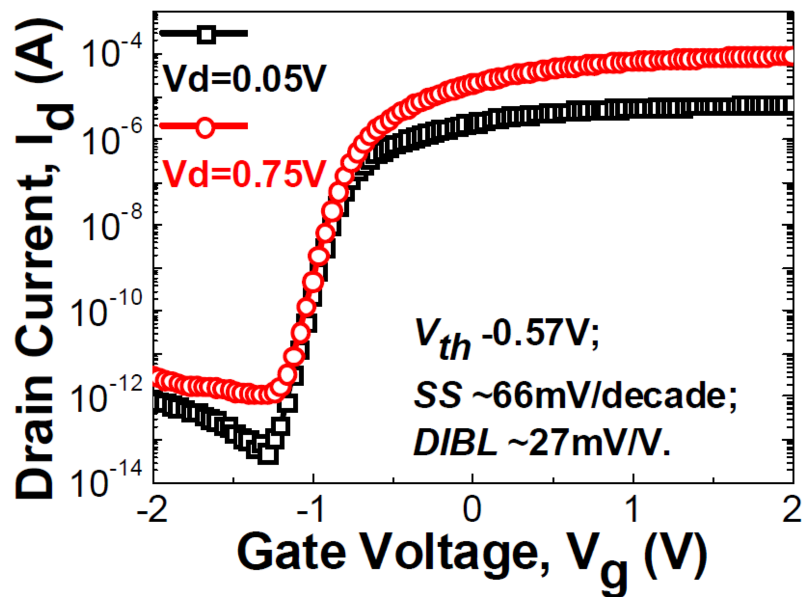

Figure 2.5. Transfer characteristics of a VSNWFET device without the RRAM cell.

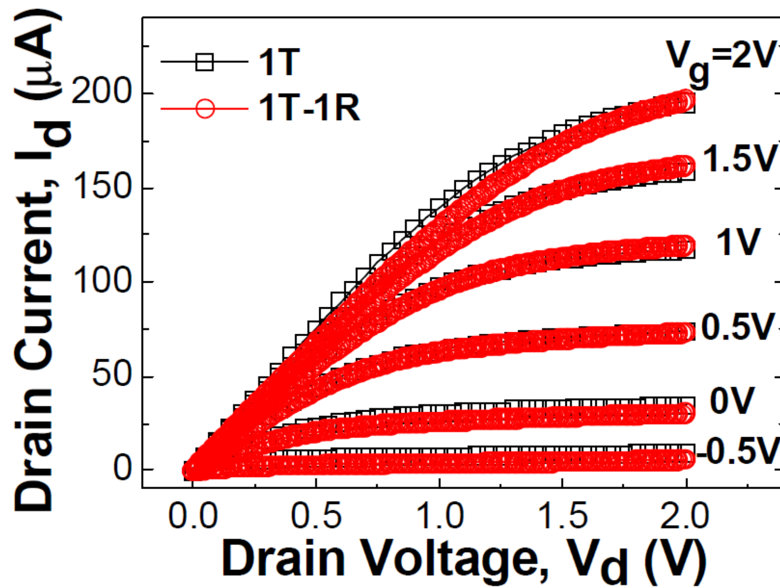

Figure 2.6. Output characteristics of a VSNWFET device without the RRAM cell (black) and a 1T1R cell with deliberately broken RRAM cell (red).

Using a gate voltage (V_g) of 1.5 V and 1 μA compliance current to form the RRAM cell, it was found that the cell could RESET under a positive bias, indicating it could operate in the unipolar regime (Mode I). The 100 cycle characteristics under Mode I is shown in Figure 2.7. It can be seen that the RESET with positive bias is large, resulting in a low off current and large memory window. This is evident from the endurance characteristics shown in Figure 2.8, where a 1000x window is present after 200 cycles. Even after considering the large variation in HRS, the memory window would still be more than 10x. This large memory window is also predicted to be retained for 10 years and at operating temperature of 85°C (Figure 2.9).

Such unipolar switching with Ni electrode has been attributed to Ni filaments being formed in the HfO_2 through injection from the Ni electrode under electric field [42]. Subsequent positive voltage sweep would annihilate

the Ni filament through oxidation and thermal dissolution. Although this resulted in a large memory window, there could be possible programming errors as evidenced from the distribution of SET voltage (V_{set}) and RESET voltage (V_{reset}) under Mode I, shown in Figure 2.10. The V_{set} and V_{reset} distributions are too close to each other, not allowing much margin for determining the optimal voltages to use, especially for RESET. If too high a voltage is used to RESET the RRAM cell, this could SET the device again after the RESET. Such is the challenge with unipolar RRAMs, when SET and RESET have the same polarity it could result in programming errors if the V_{set} and V_{reset} distributions are too close or even overlapping.

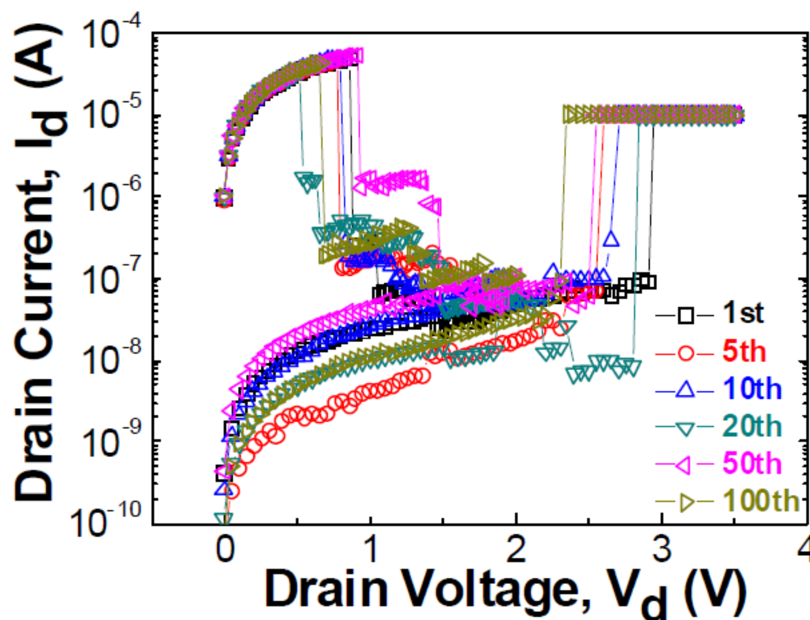

Figure 2.7. Switching characteristics of 100 cycles of the 1T1R cell under Mode I, unipolar switching.

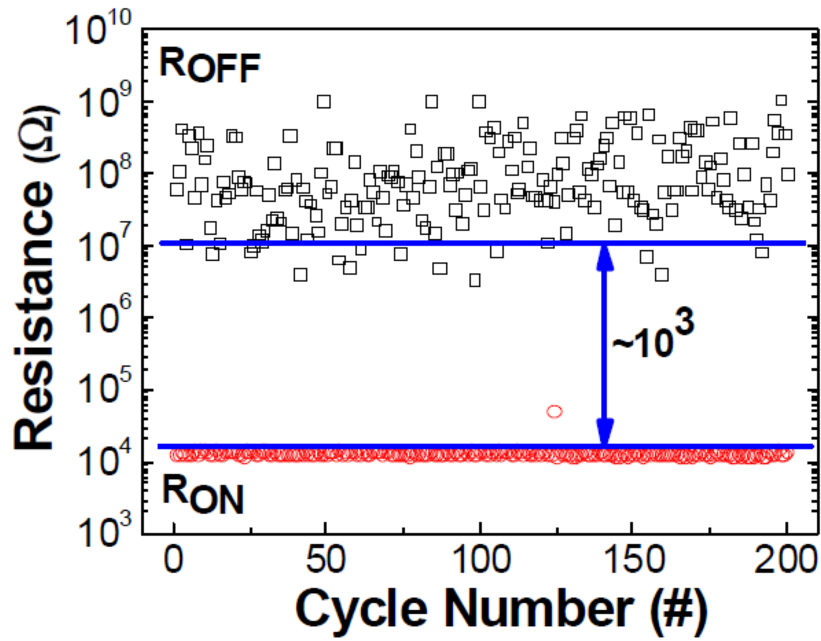

Figure 2.8. Endurance characteristics of the 1T1R cell under Mode I showing resistance distribution of HRS (black) and LRS (red) over 200 cycles.

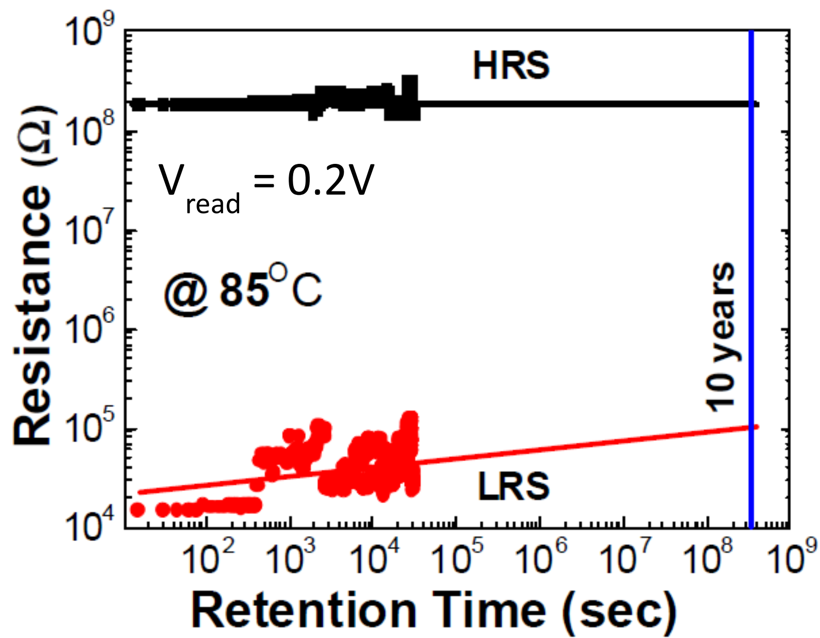

Figure 2.9. Retention characteristics of the 1T1R cell under Mode I.

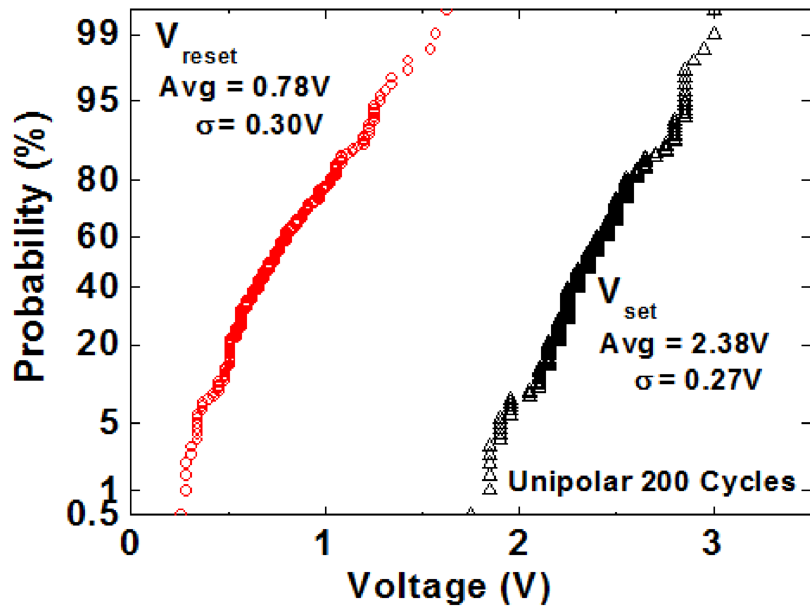

Figure 2.10. The distribution of SET voltage (V_{set}) and RESET voltage (V_{reset}) of the 1T1R cell in Mode I.

With the same forming conditions as Mode I but using a negative bias to RESET instead, the 1T1R cell is able to operate in bipolar mode (Mode II). The 100 cycle switching characteristics under Mode II is shown in Figure 2.11. A memory window of about 100x can be observed and also, no compliance current was required since the VSNWFET is able to control the current and prevent any unwanted surges. To investigate the resistance variations and effective memory window, 10 different devices across the same wafer were put through 100 cycles and their respective resistances are shown in Figure 2.12 as box plots. Even considering cell-to-cell and cycle-to-cycle resistance variations, the effective memory window is more than 10x, which is more than sufficient for reading the cell.

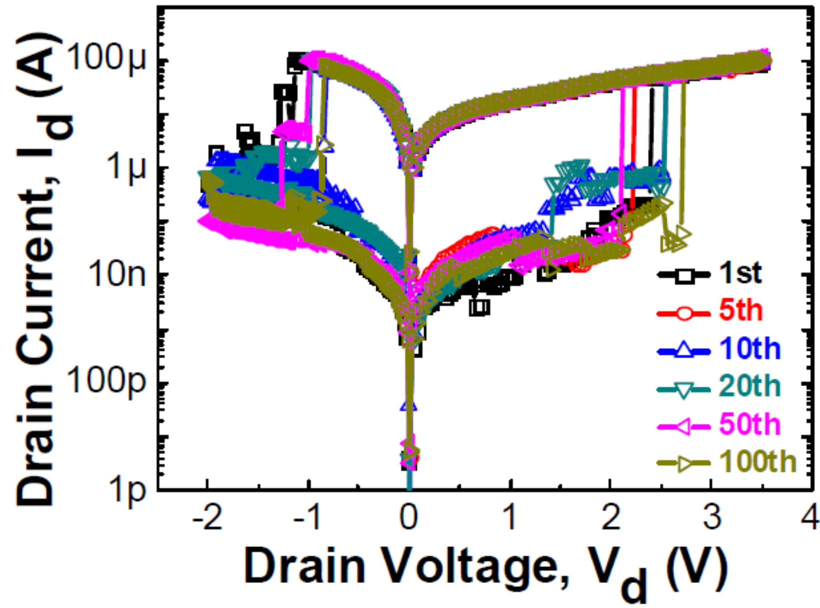

Figure 2.11. Switching characteristics of 100 cycles of the 1T1R cell under Mode II, bipolar switching.

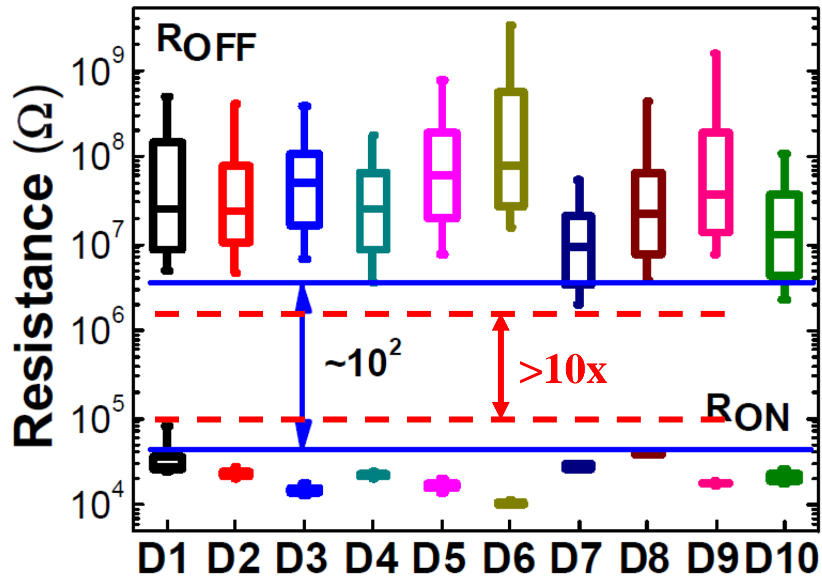

Figure 2.12. Box plot of the distribution of the memory states under Mode II over 100 cycles of 10 different RRAM cells, D1-D10.

Using a low compliance current of 20 nA, the1T1R cell was found to switch under low current conditions, as shown in the 100 cycle switching characteristics of Figure 2.13. RESET currents were mostly below 200 pA and the cell forming voltage is the same as V_{set}, so essentially, no forming process is required, ie. forming-free. A forming-free RRAM cell is very much desired from device operation point-of-view, as the cell is sensitive to forming conditions, and also from circuit operation point-of-view, as the forming or initialization process for a large array would typically take a long time. From the 100 cycle endurance characteristics in Figure 2.14, the cell is able to have more than 10x memory window using a read voltage (V_{read}) of 2 V. However, the cell-to-cell variation was found to be large. Figure 2.15 shows an example of another 1T1R cell operating under Mode III and with large current variations. There is almost no memory window for this particular cell, as evidenced from the resistance plot in Figure 2.16. So although the cell can switch at low currents, the variation is far too large for the cell to operate reliably.

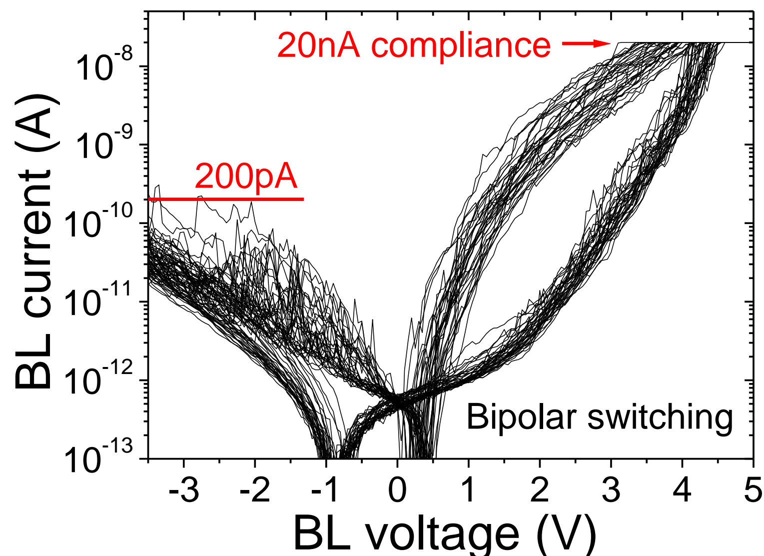

Figure 2.13. Switching characteristics of 100 cycles of the 1T1R cell under Mode III, bipolar switching with low current switching.

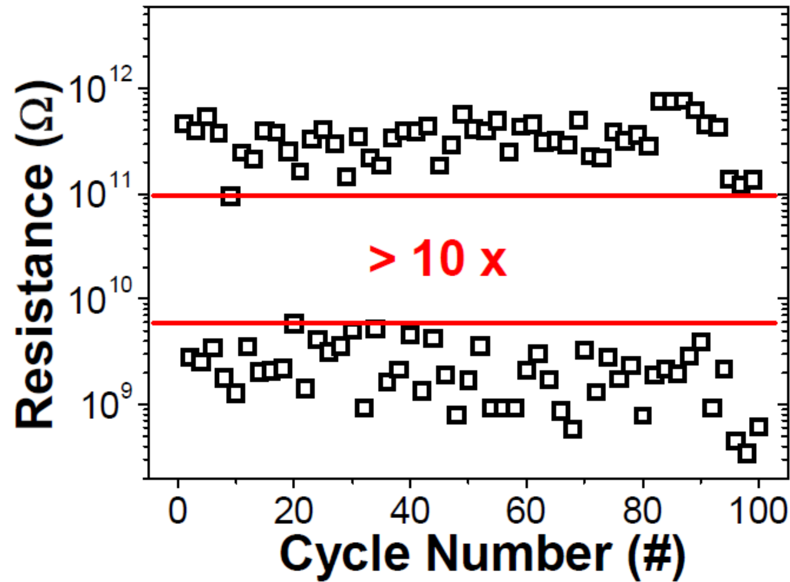

Figure 2.14. Endurance characteristics of the 1T1R cell under Mode III showing resistance distribution of the memory states over 100 cycles.

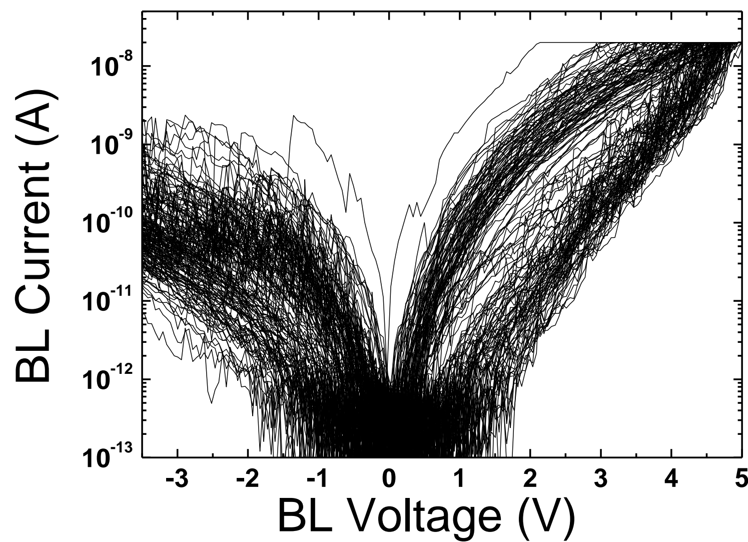

Figure 2.15. Switching characteristics of 80 cycles of a 1T1R cell under Mode III, showing large current variations.

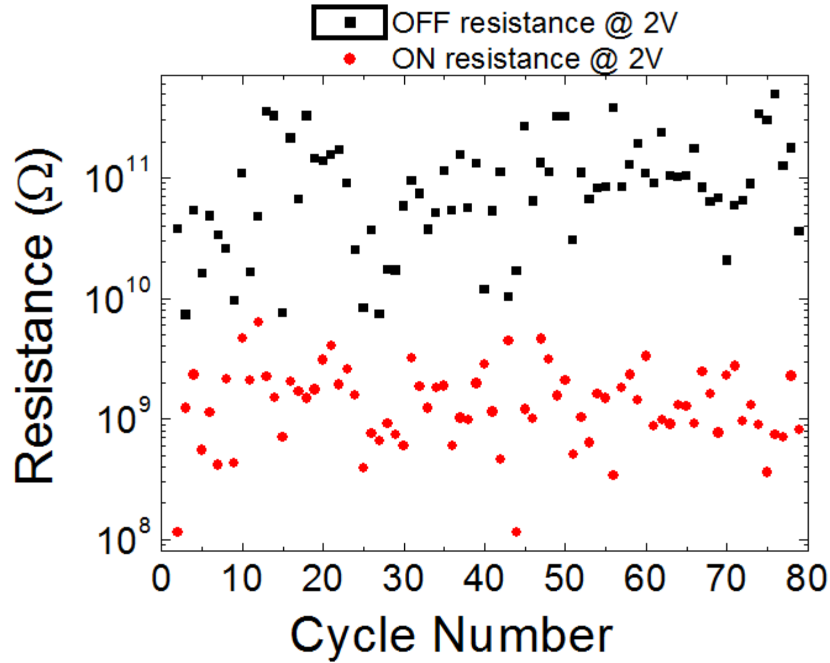

Figure 2.16. Endurance characteristics over 80 cycles of the above 1T1R cell under Mode III showing almost no memory window.

2.3. Summary

From the above results, the TiN/Ni/HfO_2/n^+-Si RRAM cell is able to operate under three different modes with various advantages and disadvantages. Under Mode I (unipolar), the memory window is large (~1000x) which provides more margin for resistance variations from cycle-to-cycle. However, the V_{set} and V_{reset} distributions were found to be too close, which could result in programming errors where a SET occurs during the RESET cycle when V_{set} is too low. Under Mode II (bipolar), although the memory window (~100x) is not as large as Mode I, the V_{set} and V_{reset} are of

opposite polarities, and so SET and RESET processes would not interfere with one another. Also, even after considering cell-to-cell and cycle-to-cycle resistance variations, Mode II is still able to maintain a memory window of more than 10x. Under Mode III (low current), the low current switching allows for low power operation, but the cell-to-cell variation was found to be large, effectively reducing the device yield.

So operating under Mode II gives the best performance, in terms of immunity to variations. On top of this, the VSNWFET as the select device not only allows simple and controllable selection of cells in large arrays, but also provides protection from unwanted current surges especially during SET cycles. So no compliance current is required. However, for CMOS compatibility, the etching of Ni electrode is non-ideal. After the dry etch of the TiN/Ni TE, a layer was found to partially coat the surface of the wafer. This is likely due to non-volatile by-products being created during the Ni etch which were subsequently deposited on the wafer. Typical use of Ni in CMOS process is for silicidation of the source/drain for reducing contact resistance. The silicidation process is self-aligned, since only exposed silicon will be silicided, and the subsequent wet etch removal of excess Ni is selective to the silicide and dielectrics. So no patterning and etching of the Ni is done.

Hence, the use of Ni-silicide as the electrode and the impact of the silicidation conditions on the RRAM performance would be a good study moving forward. This is the topic to be discussed in the next chapter.

Chapter 3 : Ni-Silicide as the Bottom Electrode

Using Ni-silicide as a bottom electrode (BE) in RRAMs allows it to be readily integrated with CMOS transistors. These transistors could have Ni-silicided source/drain regions, often done to reduce contact resistance, and could also be done for the vertical silicon nanowire FET. Since most silicidation processes are self-aligned to the source/drain regions, the BE would already be defined by these regions and so, no additional mask layers would be required to define BE.

There have been some work employing Ni-silicide as the BE [42-43], with some work even using it as the top electrode (TE) [44]. However, these works do not look into the effect that the conditions of silicidation would have on the RRAM performance. Such effects would need to be well characterized in order to design the integration with CMOS transistors.

The work presented in this chapter investigates the feasibility of Ni-silicide as the BE in TiN/HfO_2/Ni-silicide RRAM cells and also studies how the Ni concentration within the Ni-silicide impacts the performance of such a RRAM cell.

3.1. Device Preparation and Material Analyses

The TiN/HfO_2/Ni-silicide RRAM devices were fabricated on *p*-type (~10^{15} cm^{-3}) 8-inch silicon wafers. A cleaning step was first done to remove native oxide and any contaminants on the wafer surface. Ni is then deposited by sputtering, followed by a high temperature silicidation step to form Ni-silicide. Table 3.1 shows the various Ni thicknesses and silicidation conditions for the 4 devices fabricated, D1-D4. After the first silicidation step, a wet etch using H_2SO_4:H_2O_2:H_2O solution is done to selectively remove any unreacted Ni from the surface. Only D4 underwent a second silicidation step after the wet etch.

Following the Ni-silicide BE formation, a 5 nm HfO_2 switching oxide and 50 nm TiN TE were deposited through reactive sputtering, with HfO_2 deposited using Hf target in O_2 ambient and TiN deposited using Ti target in N_2 ambient. The TE was then patterned by dry lithography into dot patterns with 300 nm diameter and dry etched with Cl chemistry. A thick layer of SiO_2 was then deposited and patterned with contact holes to contact TE and BE. Then TaN/Al/TaN layers were sputtered and patterned into metal lines.

Atomic force microscopy (AFM) was used to measure root-mean-square (RMS) roughness and Auger electron spectroscopy (AES) used to determine the atomic composition at the surface of Ni-silicide. These analyses were done on samples with only Ni-silicide, following the conditions in Table 3.1. The AES spectrum was obtained from the pristine samples (before sputter) and also after in-situ Ar sputtering of the samples to remove approximately 8 nm

of material from the surface (after sputter). The atomic composition obtained before sputtering should also include some surface contaminants and any native grown oxide from the exposure to air, since AES is a surface sensitive method. After sputtering, the native oxide and any surface contaminants would have been removed, so the atomic composition obtained at this point should be the actual composition of the Ni-silicide bulk. The RMS roughness and atomic composition results are summarized in Table 3.1, along with the corresponding silicidation conditions.

Table 3.1. The various silicidation conditions used for each of the 4 TiN/HfO_2/Ni-silicide RRAM devices and their corresponding root-mean-square (RMS) roughness from atomic force microscopy (AFM) measurements and atomic composition from Auger electron spectroscopy (AES). AES was obtained from pristine samples (before sputter) and samples after Ar sputtering to remove ~8 nm of material from the surface (after sputter).

Device			D1	D2	D3	D4
Ni thickness			60nm	30nm	10nm	10nm
Silicidation 1st step			440°C, 2min			220°C, 2min
Silicidation 2nd step			None			440C, 2min
RMS roughness (nm)			5.01	4.64	0.46	0.90
AES	Before sputter	O	38.2%	38.2%	37.4%	45.4%
		Ni	23.4%	22.8%	22.3%	11.9%
		Si	38.4%	39.0%	40.3%	42.7%
	After sputter	Ni	50.7%	49.3%	47.9%	46.8%
		Si	49.3%	50.7%	52.1%	53.2%
Ni:Si before sputter			0.609	0.585	0.553	0.279
Ni:Si after sputter			1.028	0.972	0.919	0.880

From the atomic composition data after sputtering in Table 3.1, D1 was found to have the highest Ni concentration, followed by D2, D3 and D4, with D4 having the lowest Ni concentration. A high O concentration (> 37%) was observed at the surface (before sputtering), indicating the presence of a native oxide, and more so for D4 (~45%). Table 3.1 also includes the Ni:Si ratio calculated from the atomic composition before and after sputtering. It can be seen that the Ni:Si ratio is lower before sputtering than after, which means there is more Si than Ni at the surface. This is likely due to the native oxide grown being predominantly SiO_2.

Figure 3.1 (a)-(d) shows the TEM images of each of the 4 devices and Figure 3.1 (e)-(h) shows the corresponding electron dispersive x-ray spectroscopy (EDX) line scan plots, with the scan done from Ni-silicide BE to TiN TE. The native oxide between Ni-silicide and HfO_2 is not obvious in the TEM images of D1 and D2, but it becomes apparent in the TEM image of D3 and even more so for D4. The EDX line scans also show a higher Si atomic concentration at the Ni-silicide/HfO_2 interface, further confirming that the native oxide is mostly SiO_2. It can also be approximated from the EDX line scans that the thickness of this SiO_2 native oxide becomes thicker from D1 to D4.

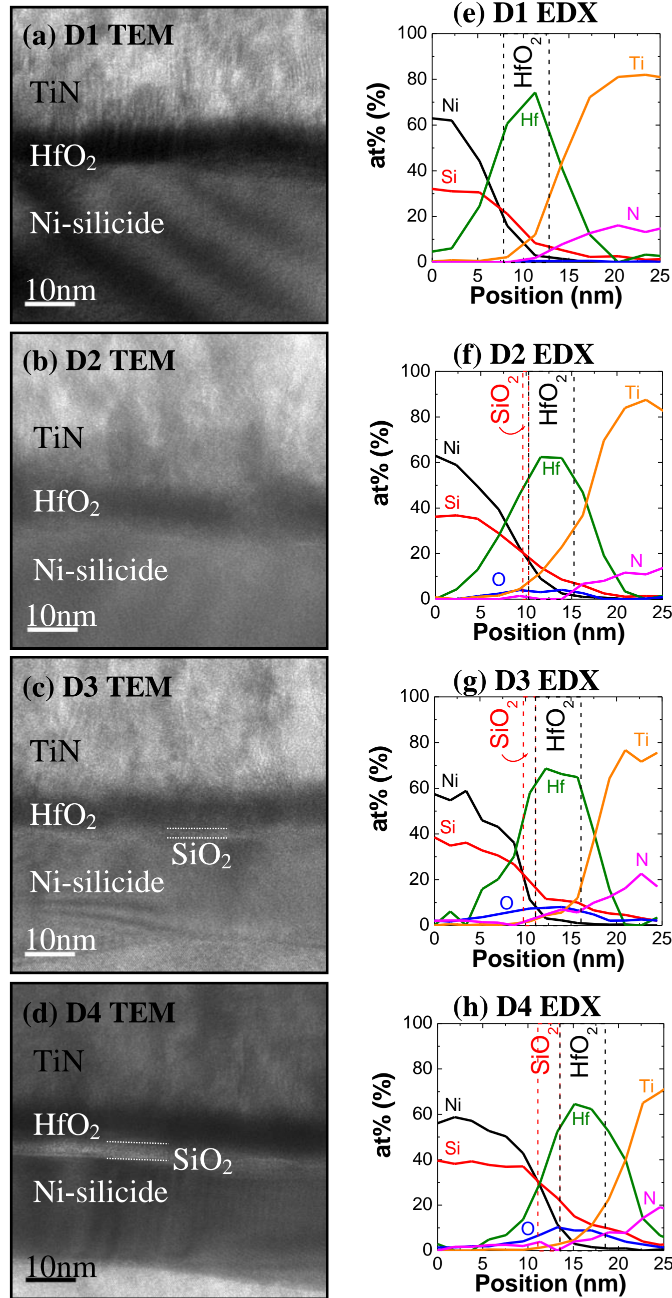

Figure 3.1. (a)-(d) TEM images and (e)-(h) electron dispersive x-ray spectroscopy (EDX) line scans from Ni-silicide to TiN of the various devices, D1-D4, respectively.

3.2. Results and Discussion

The devices were first formed with a positive voltage sweep followed by a RESET process with a negative voltage sweep, applying the voltage bias to TE while BE is grounded. This is followed by a cycling test of each device. Each cycle starts with a SET process where a positive voltage sweep is applied to a pre-determined maximum value, V_{set}, before sweeping back to zero. This is followed similarly by the RESET process but with a negative voltage sweep to the maximum value, $|V_{reset}|$.

Figures 3.2 and 3.3 show the bi-polar cycling performance of devices D1 and D2, respectively. A memory window of ~10x was observed and switching currents were high, with a 4 mA compliance current for SET. Most notably, a gradual reduction in the memory window was observed for both D1 and D2, and it is found that during some RESET cycles (negative voltage sweep), a parasitic SET occurred. Examples of this parasitic SET are shown in the inset of Figure 3.2, which occurred during the 12th RESET cycle of D1, and in the inset of Figure 3.3, which occurred during the 75th RESET cycle of D2. The parasitic SET is observed as an abrupt current jump, as with any SET process, but during the RESET cycle while the current is gradually decreasing. After each occurrence of parasitic SET, the subsequent RESET cycles are unable to lower the current back to the usual level before, effectively lowering the HRS and reducing the memory window. This means the parasitic SET is an unrecoverable process and has to be avoided.

The reason for such a parasitic SET was believed to be due to field-assisted Ni migration from the Ni-silicide BE, since during the RESET the field is towards the TiN TE. This is similar to the cation-based RRAM where the field would cause dissolution of the Ni-silicide electrode and drifts the resulting cations towards the TiN electrode. This would then form a Ni filament and lower the resistance for the HRS. If Ni-silicide indeed formed a Ni filament, the RRAM cell should be able to operate in the reverse as well, i.e., as a cation-based RRAM like in [42].

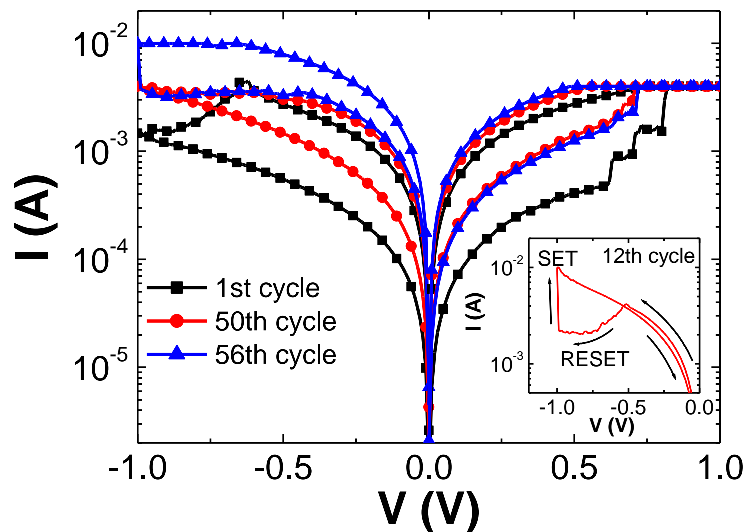

Figure 3.2. The cycling performance of D1, with the inset showing a parasitic SET during the RESET sweep of the 12th cycle.

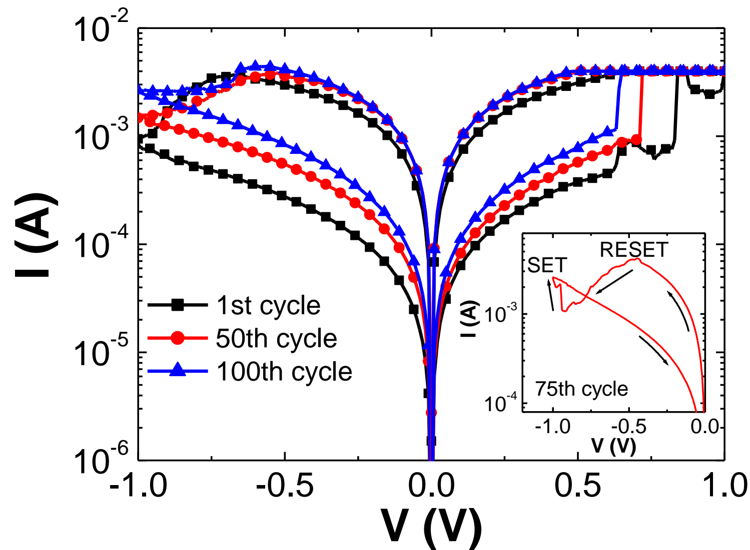

Figure 3.3. The cycling performance of D2, with the inset showing a parasitic SET during the RESET sweep of the 75th cycle.

To verify this hypothesis, the devices were first subjected to negative voltage forming, which should form a Ni filament. Figure 3.4 shows the obtained forming voltages, $|V_{form}|$, at which the devices experience the abrupt current jump associated with the forming process. The first observation was the lower $|V_{form}|$ from D4 to D1. This could be due to the higher roughness of the Ni-silicide BE of D1 and D2, shown in Table 3.1, either resulting in high fields or thinner sputtered HfO_2 at rough regions. However, the dependence of the $|V_{form}|$ on roughness is not as clear as compared to that of Ni concentration, as shown in Figure 3.5. The higher Ni concentration, through oxygen gettering, may have induced more partial filaments before electrical forming, thus lowering the $|V_{form}|$ required. The thinner native SiO_2 at higher Ni concentrations could also result in lower $|V_{form}|$. It was also observed that the higher the Ni concentration, ie. D1, the lower the negative $|V_{form}|$ compared to the positive V_{form}. There is virtually no difference between positive and

negative $|V_{forn}|$ for D4, which has the lowest Ni concentration. This gives some indication that Ni filaments are being formed as the higher the Ni concentration in the BE, the lower the negative $|V_{form}|$ relative to the positive.

The devices formed with a negative voltage were also found to work in unipolar mode, as shown in Figure 3.6, employing thermochemical effects to annihilate the filament by Joule heating. However, another possibility could be the higher Ni concentration increases the BE oxygen affinity, so the Ni-silicide draws in the oxygen from HfO_2 to form a V_o filament instead.

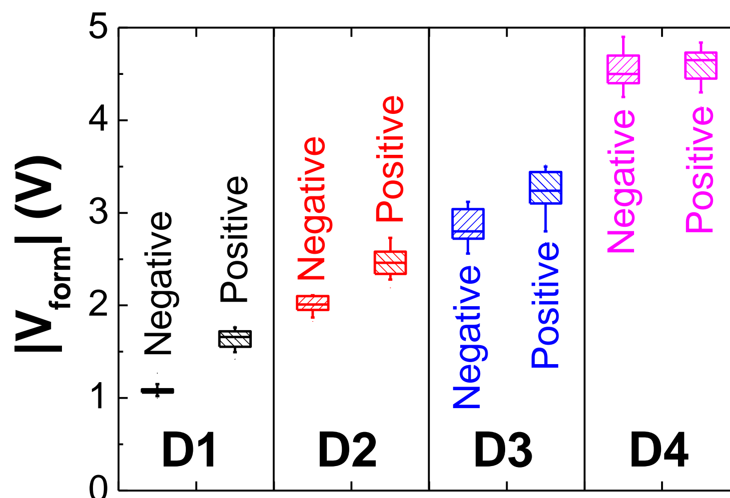

Figure 3.4. Box plot of positive and negative forming voltages, $|V_{form}|$, from over 10 devices each of D1-D4.

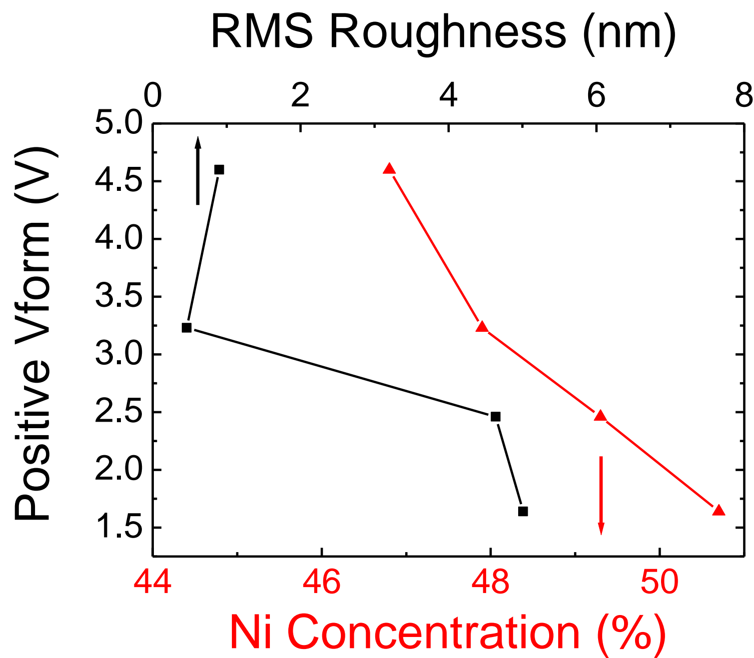

Figure 3.5. Dependence of the positive forming voltage (V_{form}) on Ni concentration and RMS roughness.

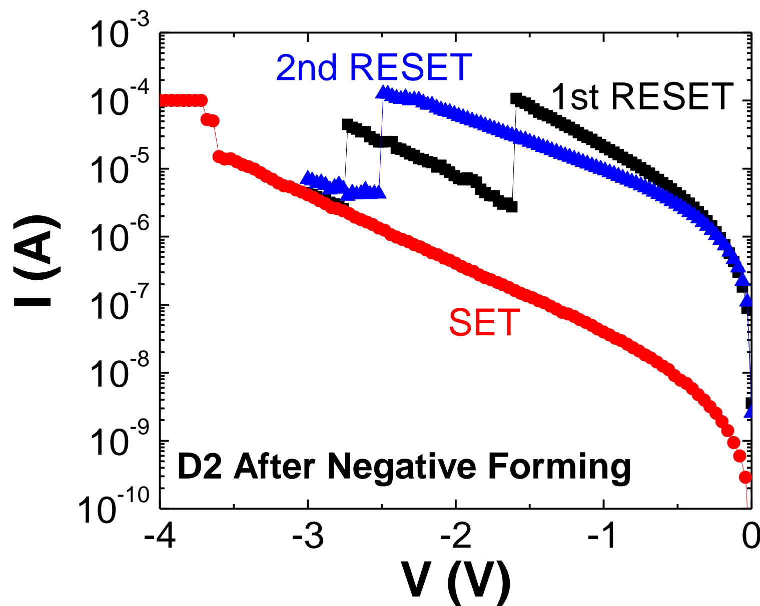

Figure 3.6. Unipolar characteristics of a D2 device after negative voltage forming.

To investigate further, an EDX line scan study was done on fabricated devices similar to D2 but with 10 nm HfO_2 instead. The EDX line scan is done parallel to and within the HfO_2, so a thicker HfO_2 would ensure the EDX scan remains within the HfO_2. Three different devices were scanned to observe any differences in their Ni concentrations within the HfO_2: one with positive forming, one with negative forming at 10 nA current compliance, one with negative forming at 50 nA current compliance. The Ni concentrations in atomic percentage of these three devices are shown in Figure 3.7. The devices that underwent negative voltage forming both had higher Ni concentrations than the one with positive voltage forming. This is further proof that Ni migration occurs at negative bias. Furthermore, the device formed at the higher compliance current of 50 nA had even higher Ni concentration than the one formed at lower compliance current. This indicates more Ni migration occurred at higher compliance current.

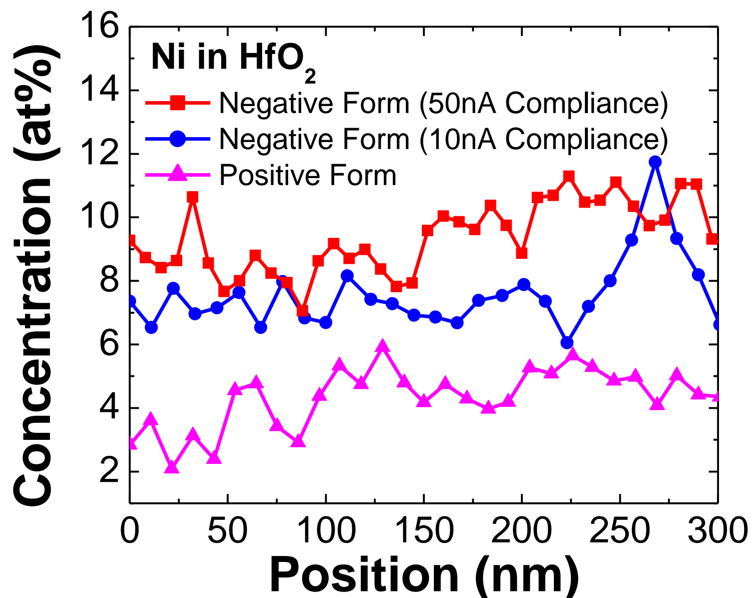

Figure 3.7. EDX line scan within 10 nm HfO_2 and under the TiN TE, showing Ni counts of D2 devices under various states.

From the various studies done above, the most likely cause of the parasitic SET is illustrated in Figure 3.8, showing the 4 states of the RESET process with the first occurrence of parasitic SET. Before the RESET occurs, state 1 has a V_o filament formed through positive forming. As the RESET takes place, the V_o filament withdraws from the Ni-silicide BE and the current reduces, as in state 2. At higher negative voltage, state 3 occurs, where a Ni filament is formed by Ni cation migration from the Ni-silicide BE and drifts along the electric field to contact the remaining V_o filament. State 4 may occur, where the V_o filament withdraws even more from the Ni filament and the current reduces again. Having two filaments working in the opposite direction of each other would also be working against each other, whereby one filament is SET while the other RESET, and vice versa. As such the memory window reduces over many cycles.

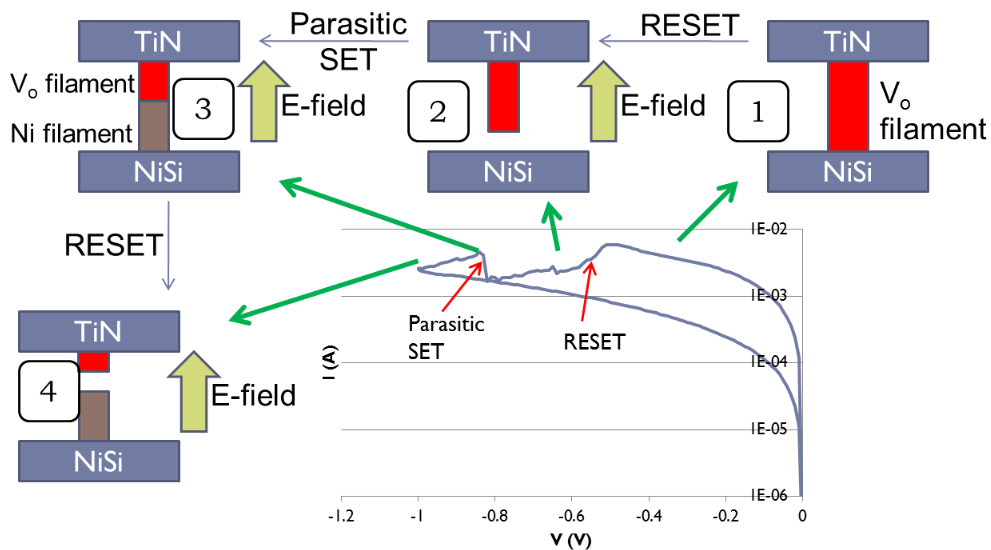

Figure 3.8. Illustration of the RESET, parasitic SET, and subsequent RESET processes.

An attempt to avoid the parasitic SET was done by reducing V_{reset} from -1 V to -0.8 V. The cycling performance is shown in Figure 3.9. There was no clear reduction of the memory window for 100 cycles, but some variation in the HRS was observed. This could be due to the V_{reset} of -0.8 V not being sufficient for a proper, complete RESET, so a partial RESET occurs for some cycles.

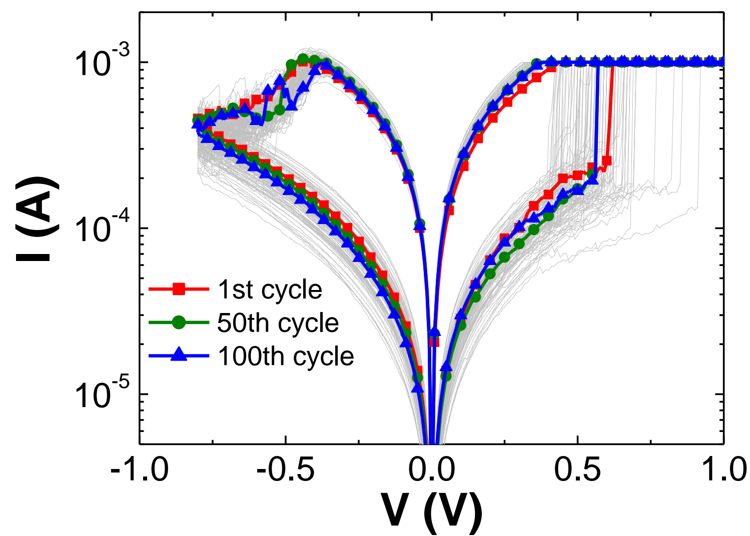

Figure 3.9. The D1 cycling performance, up to 100 cycles, with reduced RESET voltage of -0.8 V.

Using a compliance current of 400 nA, D3 and D4 were found to switch at low currents, shown in Figure 3.10 for D3 and Figure 3.11 for D4. RESET currents are < 100 pA for D3 and < 1 nA for D4. The devices are also forming-free, where the forming voltage is close to the SET voltage, or where the device is able to RESET to the same current level as the initial state. The I-V curves are noisy, indicating some instability and possibility of electron trapping/de-trapping causing the resistance change, ie. volatile switching. But the devices are able to retain HRS and LRS for 1000 s, even under 1 V stress and at 120°C, and maintain a memory window of 2x for D3 (Figure 3.12) and 10x for D4 (Figure 3.13). Since any trapped electrons would have been de-trapped by the elevated temperature and voltage stress, the fact that the HRS and LRS did not change indicates the switching is not from trapping/de-trapping of electrons. This kind of low current switching is very similar to that found in Chapter 2.

The low switching phenomena is believed to arise due to the presence of a thicker native SiO_2 for D3 and D4, as observed in the TEM images of Figure 3.1. With a typically lower breakdown field of HfO_2 [45], the HfO_2 experiences a soft breakdown first under low current compliance. The low compliance current prevents a breakdown of the SiO_2, which would break down irreversibly at higher compliance current, resulting in higher switching currents. So the SiO_2 seems to play a key role in the low current switching, acting as a tunneling barrier to the current.

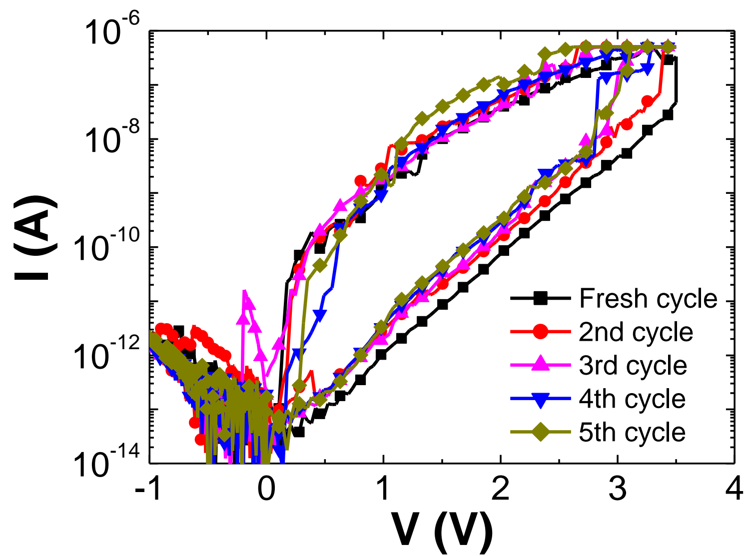

Figure 3.10. The 5-cycle I-V curves of D3, showing forming-free and low current switching characteristics.

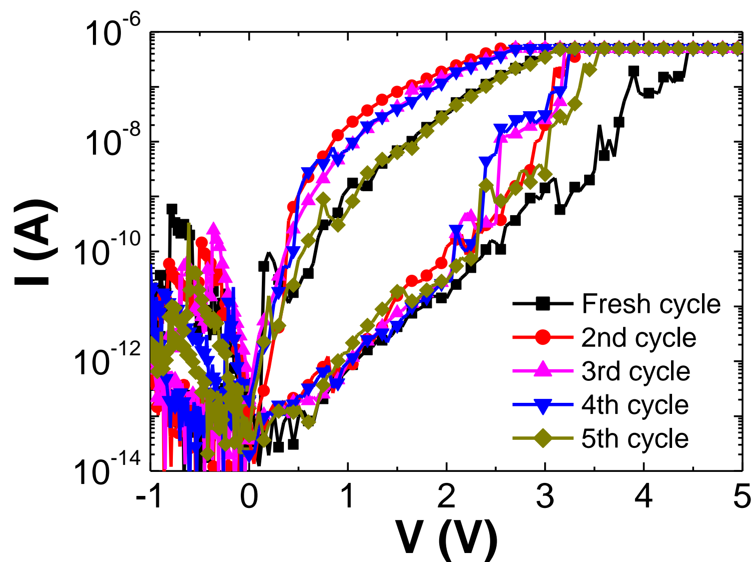

Figure 3.11. The 5-cycle I-V curves of D4, showing forming-free and low current switching characteristics.

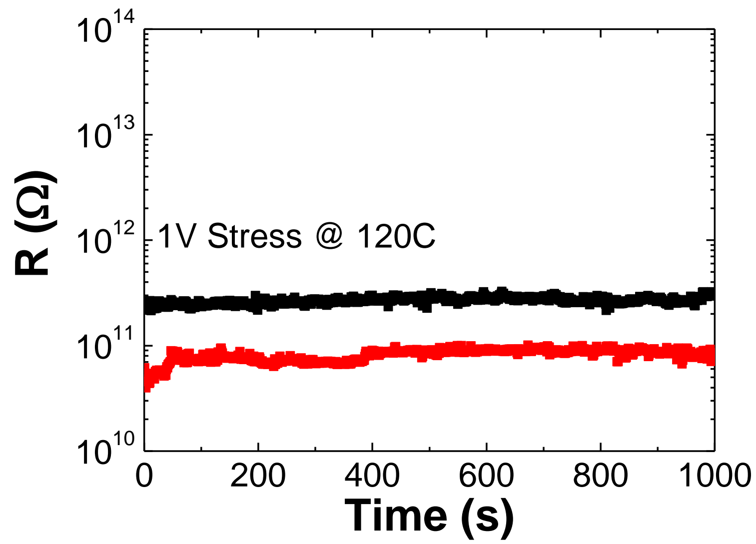

Figure 3.12. Retention characteristics for 1000 s at 120°C under 1V stress for D3, showing memory window of 2x.

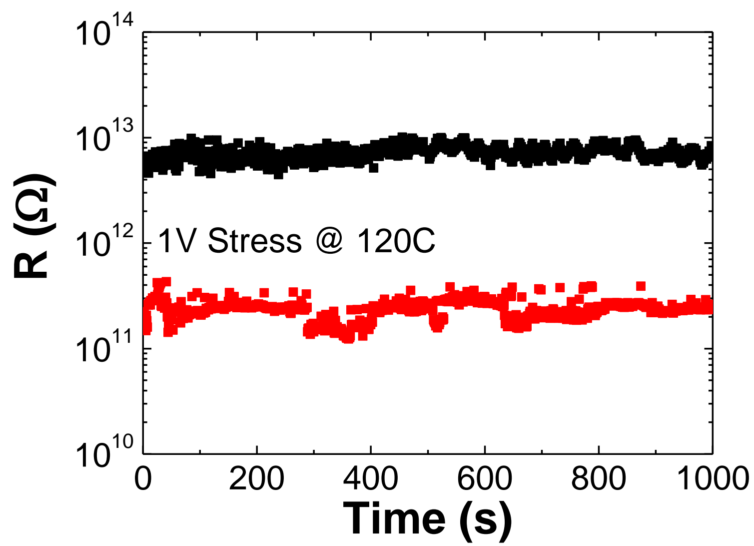

Figure 3.13. Retention characteristics for 1000 s at 120°C under 1V stress for D4, showing memory window of 10x.

As described in Chapter 1.6, plotting $\ln(I/V^2)$–$1/V$ of the low switching current RRAM cell should reveal either a linear plot with negative slope, indicating FN tunneling, or a logarithmic curve, indicating direct tunneling. Figure 3.14 shows the $\ln(I/V^2)$–$1/V$ plot for the HRS of D4. It can be seen that at lower voltages, or high 1/V, a logarithmic curve is present, while at higher voltages the curve is linear and with negative slope. This is a typical transition from direct tunneling to FN tunneling from low to high voltage [33].

The $\ln(I/V^2)$–$1/V$ plot for the LRS of D4 also shows a similar transition, as shown in Figure 3.15 for the 1st cycle. It can also be seen that the transition voltage, where the tunneling current transitions from direct to FN tunneling, is lower, i.e., higher 1/V. This is likely due to the oxygen vacancies generated in HfO_2 and accumulated at the SiO_2-HfO_2 interface causing the energy bands of SiO_2 to bend. As such, a lower voltage is required to result in FN tunneling. However, the evidence of direct tunneling is not present in the subsequent cycles, as shown in Figure 3.16, with the 1st cycle plotted for comparison. This could mean a further accumulation of oxygen vacancies occurred after the 1st cycle, resulting in the energy bands of SiO_2 bending to the point where FN tunneling dominates even at low voltages.

In comparison, the $\ln(I/V^2)$–$1/V$ plot for the LRS of D1 and D2 (Figure 3.17) shows only a logarithmic fit, which could indicate direct tunneling. Plotting $\ln(I/V^2)$–$\ln(1/V)$ instead, as in Figure 3.18, a linear fit with near-unity slope was observed. With the intercept from the $\ln(I/V^2)$–$\ln(1/V)$ plot and based on Equation (1), the thickness of the oxide barrier was estimated to be 0.3 nm for D1 and 0.35 nm for D2, assuming a barrier height, ϕ, of 3.7 eV,

corresponding to the interface of Ni-silicide to SiO_2. Compared with the barrier thickness of 2.1 nm similarly estimated for D4, the barrier for D1 and D2 is possibly an interfacial layer formed between Ni-silicide and HfO_2.

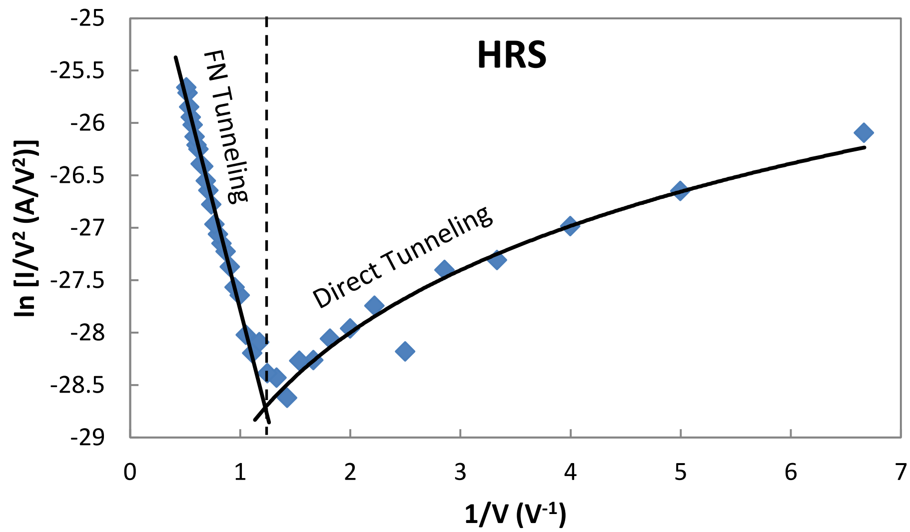

Figure 3.14. The $\ln(I/V^2) - 1/V$ plot of the HRS of D4, showing a transition from direct tunneling at low voltages to FN tunneling at higher voltages.

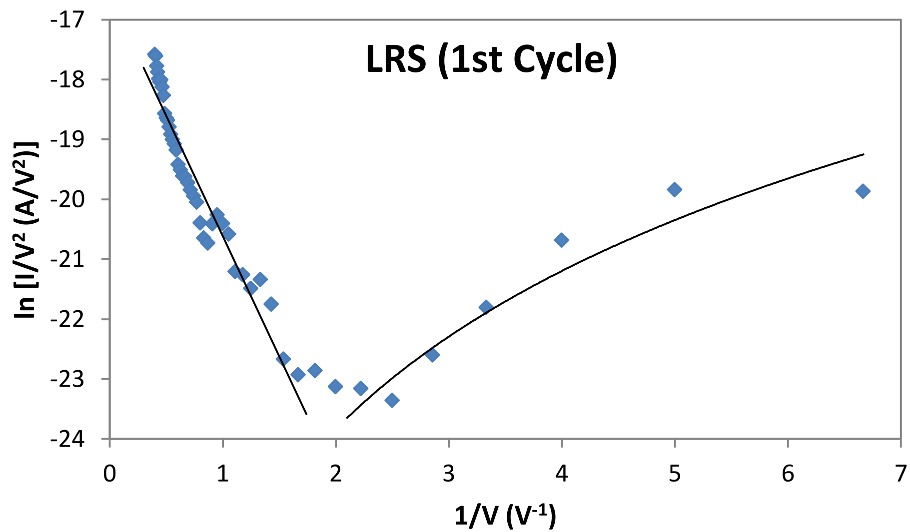

Figure 3.15. The $\ln(I/V^2) - 1/V$ plot of the LRS of the 1st cycle of D4, showing similar transition from direct tunneling to FN tunneling but at a lower voltage.

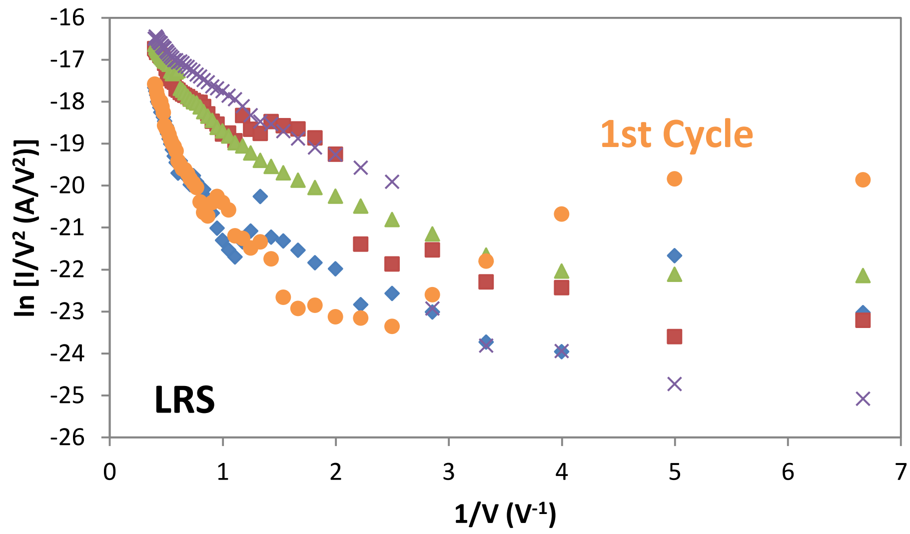

Figure 3.16. The ln(I/V^2) – 1/V plot of the LRS of the first 5 cycles of D4, with only the 1st cycle having indication of direct tunneling.

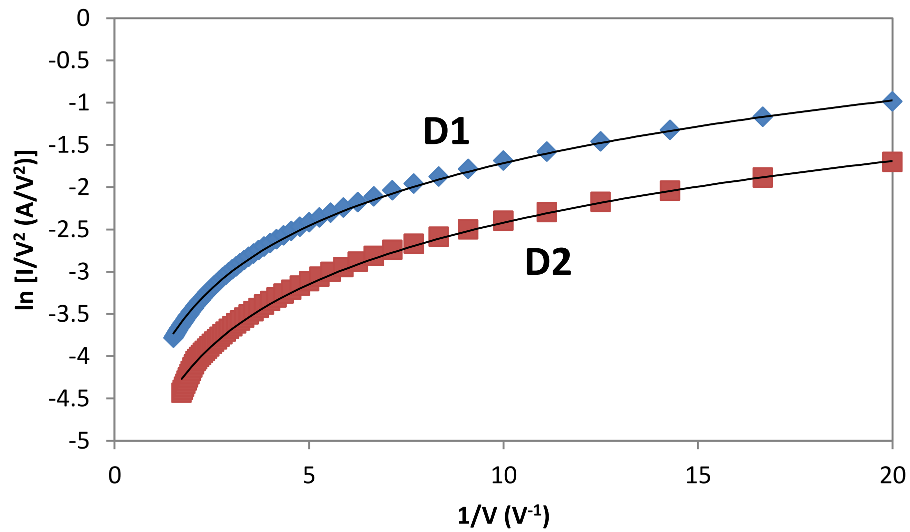

Figure 3.17. The ln(I/V^2) – 1/V plot of the LRS of D1 and D2, showing a logarithmic fits.

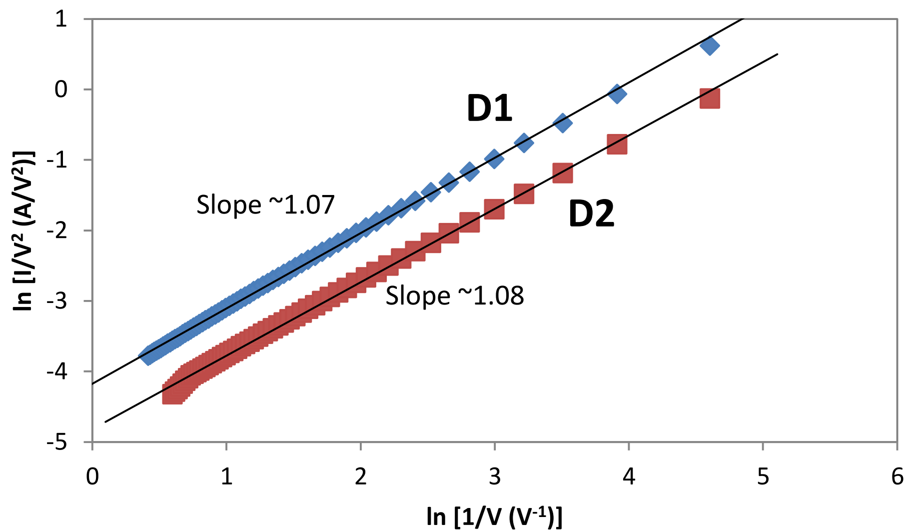

Figure 3.18. The $\ln(I/V^2) - \ln(1/V)$ plot of the LRS of D1 and D2, showing a near-unity slope.

3.3. Summary

In this chapter, a feasibility study of using Ni-silicide as the BE in TiN/HfO_2/Ni-silicide RRAM cells was presented. Four different Ni concentrations were used and a comparison of the different performance was made.

In RRAM cells with Ni-silicide of higher Ni concentration (> 49%), a parasitic SET process was found to occur during RESET. Upon a study under negative voltage, unipolar characteristics were found to be possible, indicating some cation-based switching occurs at negative voltage. Further investigation using EDX confirmed a higher concentration of Ni within the HfO_2 in RRAM cells formed using negative voltage. The likely cause for the parasitic SET

was therefore concluded to be due to the formation of a Ni filament under negative voltage. This parasitic SET could be avoided by lowering the V_{reset}, but this was observed to increase the HRS variation.

RRAM cells with lower Ni concentration (< 48%) showed the ability to switch with low currents (< 1 nA) and are forming-free. Even though the switching was noisy, the memory window was maintained for 1000 s, even under 1 V stress and at 120°C. The low current switching was attributed to a native SiO_2 layer between Ni-silicide and HfO_2. From conduction mechanism analyses, the dominant conduction was confirmed to be direct tunneling at low voltages, followed by FN tunneling at higher voltages, which is typical for tunneling barriers. However, after a few cycles, the evidence of direct tunneling gradually disappears, likely due to gradual accumulation of oxygen vacancies at the SiO_2-HfO_2 interface causing bending of the SiO_2 energy bands to a point where FN tunneling dominates even at low voltages.

From the above results, the use of Ni-silicide as the BE is not ideal, since at high Ni concentration, a parasitic SET either reduces the memory window or the method to avoid it causes HRS variation. Although RRAM cells with lower Ni concentrations are able to switch at ultra-low currents, the memory window is too small to be immune to the current variations as observed by the noisy I-V curves. In order to avoid the complications of involving both cation- and anion-based operation, a more unreactive but CMOS-compatible BE is needed, and TiN is one good candidate.

Chapter 4 : RRAM Material Engineering using ALD

As discussed in Section 1.7, ALD is an excellent process for material engineering in RRAM cells. This chapter presents work involving the use of various ALD oxidants and methods to deposit the HfO_2 switching layer in TiN/Ti/HfO_2/TiN RRAM cells.

First, the impact of substrate temperature, 250°C and 300°C, and use of oxidants, mainly H_2O and O_3, are studied. Most notable is the observation of low current switching and also a large RESET happening occasionally in some RRAM cells with HfO_2 deposited at 300°C using H_2O.

Next, the low current switching and large RESET phenomena are studied further through electrical measurements and a new ALD method to deposit HfO_2 is used in the process.

Finally, to improve the large RESET device yield, a buffer layer was introduced to attempt to limit the current overshooting problem which would greatly affect the endurance of the RRAM device.

4.1. Device Fabrication and Characterization

The work presented in this chapter involves the use of the TiN/Ti/HfO2/TiN RRAM material stack, unless otherwise stated. Devices were fabricated on 8-inch wafers using CMOS compatible processes. A 100 nm thick layer of SiO_2 was first deposited using plasma-enhanced chemical vapor deposition (PECVD), followed by the RRAM material stack deposition, with TiN BE by sputtering, HfO_2 by ALD, and TiN/Ti TE by sputtering. This is followed by patterning and etching of ~400 nm diameter dot patterns to define the TE. A layer of Si_3N_4 followed by SiO_2 were then deposited, contact holes patterned and then etched to provide contacts to both BE and TE. Metallization with Al metal lines then concludes the entire process.

Electrical characterization was performed at room temperature, with the bias applied to the TE and keeping BE grounded, unless otherwise specified. All electrical measurements were done using Agilent B1500A Device Parameter Analyzer and automated application tests programmed using Agilent EasyEXPERT software.

4.2. ALD HfO_2 Using H_2O or O_3

The effects of substrate temperature and oxidant used during the deposition of ALD HfO_2 were studied using TiN/Ti/HfO_2/TiN RRAM cells. Two different substrate temperatures of 250°C and 300°C along with different oxidants, H_2O and O_3, were used for ALD HfO_2. The RRAM devices were first formed using voltage sweep with a 100 nA current compliance before DC cycling was performed. Figures 4.1 and 4.2 show the typical I-V sweeps over 10 cycles of devices using H_2O oxidant at substrate temperatures 250°C and 300°C, respectively. Figures 4.3 and 4.4 show the same 10 cycles of I-V sweeps, but for devices using O_3 oxidant at substrate temperatures 250°C and 300°C, respectively. Overall, more than 10x memory window was observed for all devices and with high switching currents exceeding 1 mA.

Figure 4.5 summarizes some key parameters obtained from the 10 DC cycles of the four different conditions shown in Figures 4.1-4.4, namely the on and off current, I_{on} and I_{off}, respectively, and the I_{on}/I_{off} ratio. The I_{on} and I_{off} were both extracted from the I-V characteristics at 100 mV and the I_{on}/I_{off} ratio is calculated as the ratio of minimum I_{on} to maximum I_{off}, which is the effective memory window over 10 cycles. From Figure 4.5, the O_3 processes generally result in higher switching currents. This could likely be due to the higher carbon content from the O_3 process, as explained in Chapter 1.7. The carbon impurities create traps within the HfO_2 and increases the leakage current [46], possibly forming wider filaments through the larger number of leakage paths.

The condition of H_2O @ 300°C shows larger memory window of 36x, around 2x more than the other conditions. Thus, this particular process condition was chosen as the focus. Most notably, upon further measurement of devices for H_2O @ 300°C, large RESET was observed for some devices after forming, resulting in a large memory window of more than 1000x.

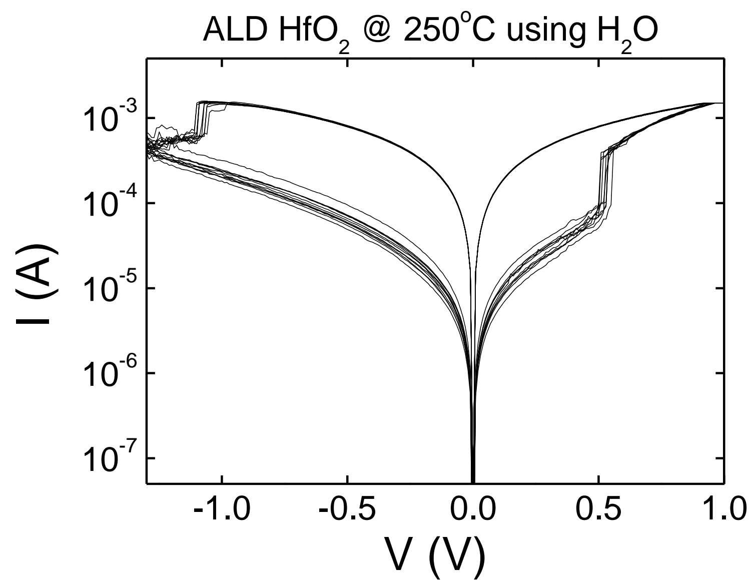

Figure 4.1. The typical 10-cycle I-V sweep of the TiN/Ti/HfO_2/TiN RRAM cell, with HfO_2 deposited by ALD at 250°C substrate temperature and using H_2O as oxidant.

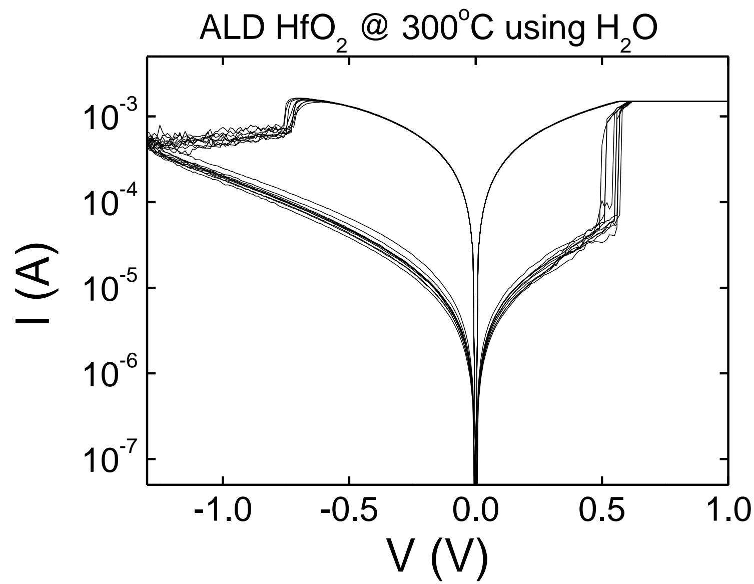

Figure 4.2. The typical 10-cycle I-V sweep of the TiN/Ti/HfO_2/TiN RRAM cell, with HfO_2 deposited by ALD at 300°C substrate temperature and using H_2O as oxidant.

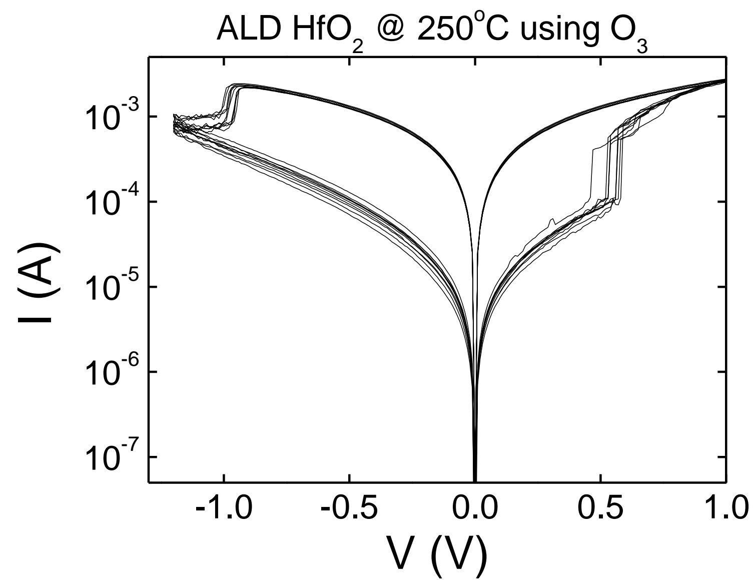

Figure 4.3. The typical 10-cycle I-V sweep of the TiN/Ti/HfO_2/TiN RRAM cell, with HfO_2 deposited by ALD at 250°C substrate temperature and using O_3 as oxidant.

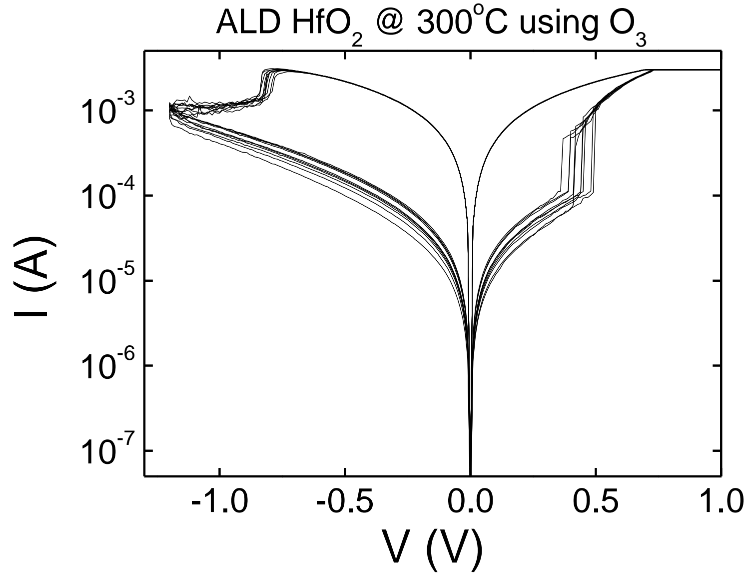

Figure 4.4. The typical 10-cycle I-V sweep of the TiN/Ti/HfO_2/TiN RRAM cell, with HfO_2 deposited by ALD at 300°C substrate temperature and using O_3 as oxidant.

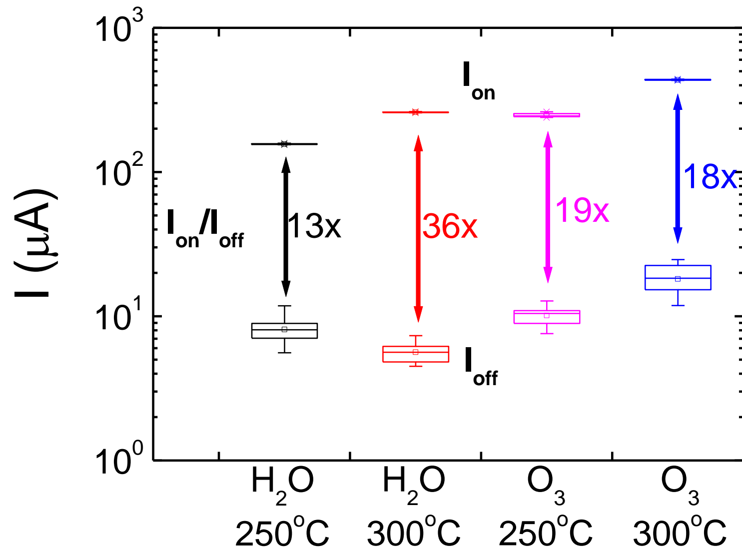

Figure 4.5. Box plot of the I_{on} and I_{off} of RRAMs with ALD HfO_2 deposited under various conditions, obtained at 100 mV from 10 DC cycles. The I_{on}/I_{off} ratio is also shown and is calculated as minimum I_{on} over maximum I_{off}.

4.2.1. Observation of Large RESET

Figure 4.6 show a typical cycle of a RRAM cell in the H_2O @ 300°C split having large RESET, defined as a current drop of > 100x during RESET cycle. Apart from the resulting large memory window of more than 1000x, the switching currents were also found to be lower (≤ 1 mA). Such characteristics were found in RRAM cells where the current was still low (partially formed cell), despite forming at 100 nA compliance current (CC). Upon another forming process of the same RRAM cell at higher CC of 1 μA, the cell was found to switch with large RESET. Figure 4.7 shows these two voltage sweeps, which then resulted in a large RESET (> 100x current drop) shown in the inset. Such a forming process is akin to a two-step voltage sweep with increasing CC which likely prevents current overshooting beyond the CC, resulting in "soft" forming. This would then result in the formation of a narrower conductive filament (CF).

As illustrated in Figure 4.8, the typical "hard" forming happens when a large current overshoots the CC due to the abrupt current jump being too fast for the compliance circuit to match. Also, allowing such a large current to flow through an insulating film may cause it to melt from Joule heating, ie. breakdown. This results in a large number of oxygen vacancies being generated and forming a wider CF, as observed in [27]. The following RESET process is then only able to annihilate a shorter length of the CF due to it being wider. The larger amount of Joule heating from current overshooting may also cause more thermal diffusion of the oxygen atoms farther away from the CF, making it harder to oxidize the oxygen vacancies and annihilate the CF .

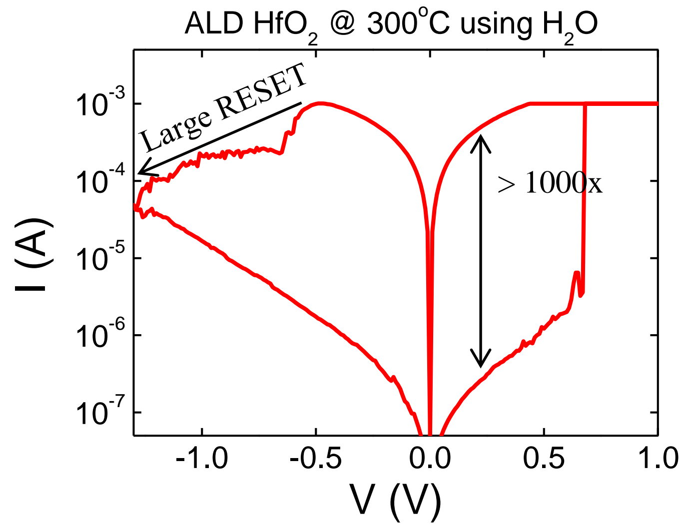

Figure 4.6. One cycle of a RRAM cell with ALD HfO_2 using H_2O at 300°C substrate temperature showing an example of large RESET (defined as a current drop of > 100x during RESET), resulting in a large memory window of more than 1000x.

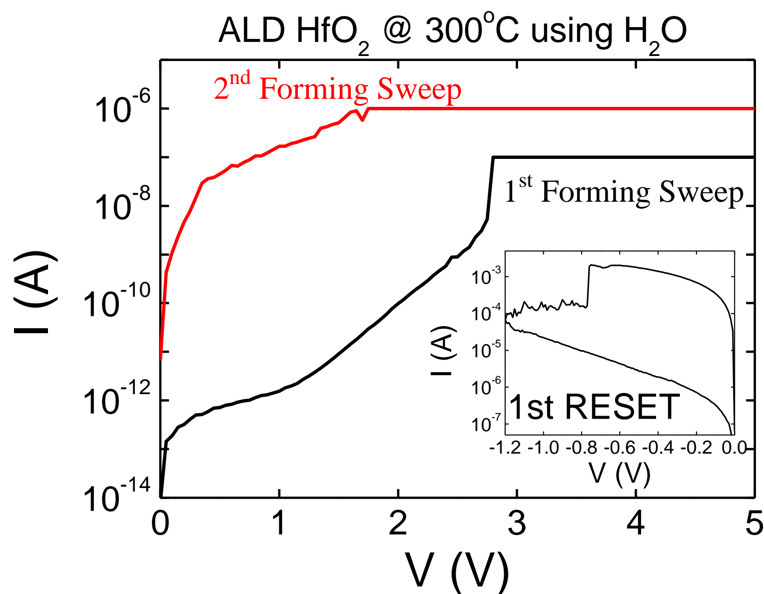

Figure 4.7. The forming I-V curves, using 2 sweeps with 100 nA and 1 μA compliance current, which result in large RESET, as evidenced in the first RESET after forming (inset).

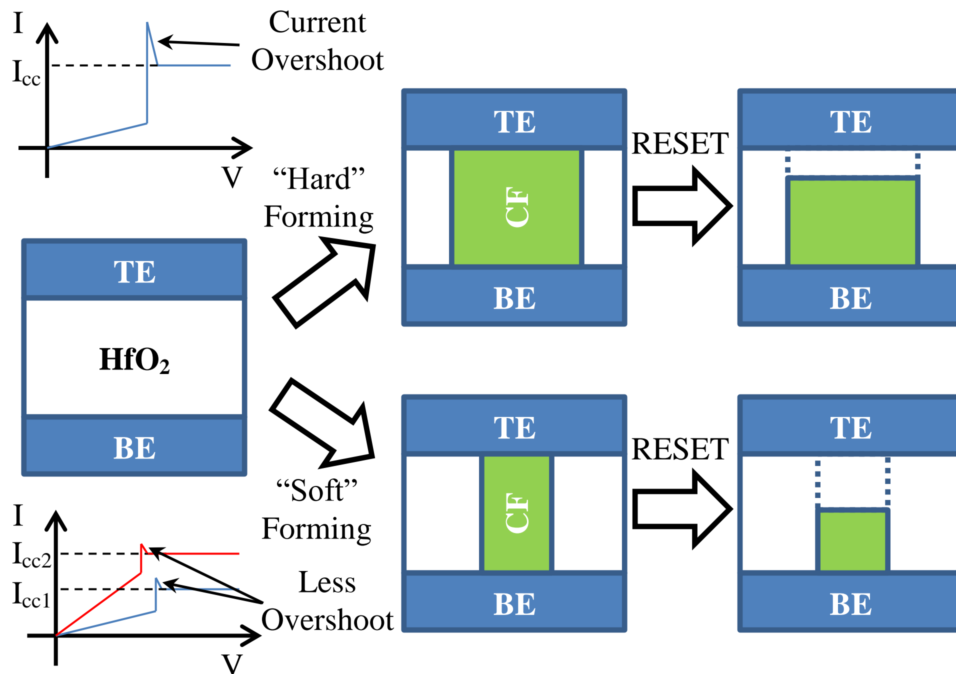

Figure 4.8. Illustration of the likely reason for large RESET after "soft" forming, where large current jumps are avoided.

Using a "soft" forming, shown in Figure 4.8, a large current overshoot is prevented by using a low CC, I_{cc1}, first to partially form the CF, followed by a higher CC, I_{cc2}, to completely form the CF. The resultant CF is narrower and thus easier to annihilate through the subsequent RESET process, allowing a large RESET to occur and increasing the HRS. Such a RRAM cell with a large memory window is very much desired, as it would give more margins for cycle-to-cycle resistance variations and also could allow multi-level cell operation.

However, the two-step forming sweep to two different CC only managed to form a handful of cells with large RESET. Most cells went into high current switching like in Figure 4.2. As such, rather than just a two-step forming process, a multi-step forming was attempted. Figure 4.9 shows the different

steps used for one particular RRAM cell, each with increasing CC. It can be seen that during such initial stages of CF formation, there are many oxygen vacancy generation and recombination occurring during the voltage sweep, causing current increments, for generation, and decrements, for recombination. The general trend of current increase shows the number of oxygen vacancies accumulating and gradually becoming aligned to form a CF. The success rate of forming large RESET cells increased with the use of this multi-step forming.

In order to further improve the forming yield, a new forming method was developed following the flow chart in Figure 4.10 and also illustrated in Figure 4.11. The method is similar to the multi-step voltage sweep example shown in Figure 4.9, involving an increasing CC with each step, but uses a constant voltage forming (CVF) rather than a voltage sweep. Initial, final and step size of the CC, in logarithmic scale, are user-defined I_{init}, I_{final}, I_{step}, respectively, together with the final forming voltage to use (V_{final}) and the time to apply forming voltage for each step (T_{form}). The program first does a voltage sweep with CC at I_{init} to determine the initial forming voltage to use (V_{init}), as shown in Figure 4.11(a). The voltage step size, V_{step}, is then calculated as a linear step from initial to final based on total number of steps. Each step would use CVF to form the RRAM cell at lower forming voltage (V_{form}), decreased by V_{step} [Figure 4.11(b)], at higher CC (I_{comp}), increased by I_{step} [Figure 4.11(c)], and for duration of T_{form}. If the cell fails to form within T_{step}, in the mth step for example, CVF is repeated but with V_{form} increased by V_{step} each time forming fails, i.e., I_{comp} not reached, or with V_{form} decreased by V_{step} in the event I_{comp} is reached within T_{form} [Figure 4.11(d)]. The I_{comp} is

always kept constant at $I_{comp,m}$ [Figure 4.11(e)]. The CVF proceeds with varying V_{form} based on whether $I_{comp,m}$ is reached until finally $I_{comp,m}$ can be reached using $V_{form,m}$. Then the program proceeds with the $(m+1)^{th}$ step using $V_{form,m+1}$ and $I_{comp,m+1}$. So CVF has to be successful for each step at lower V_{form} and higher I_{comp} than the previous step, before moving on to the next step. As such, each step may require multiple sub-steps to achieve successful CVF, making it a tedious process. However, though it may take time to successfully form the RRAM cell, the CVF method showed a remarkable improvement in forming yield, as shown in Figure 4.12. Forming yield was obtained from 20 RRAM cells and is defined as successfully forming RRAM cells with switching currents ≤ 1 mA and with memory window > 100x. This new CVF method was thus used to form subsequent RRAM cells for large RESET devices.

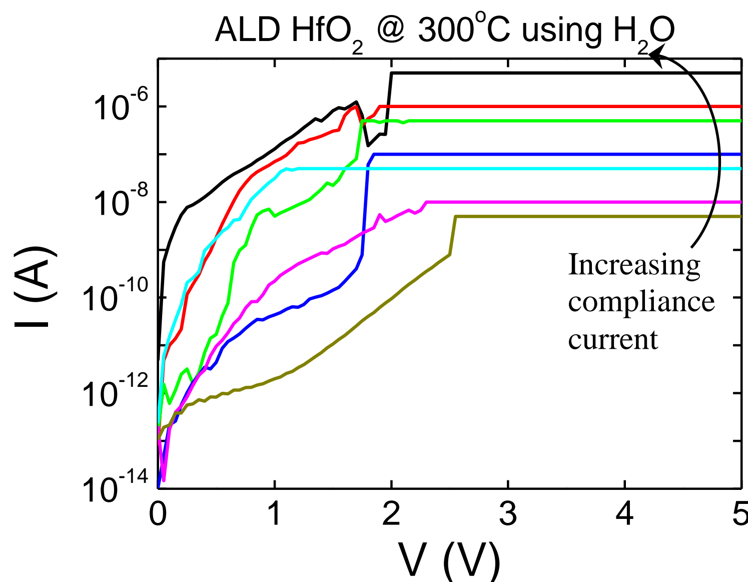

Figure 4.9. The multi-step voltage forming, with increasing current compliance, used in the gradual forming of RRAM devices for large RESET.

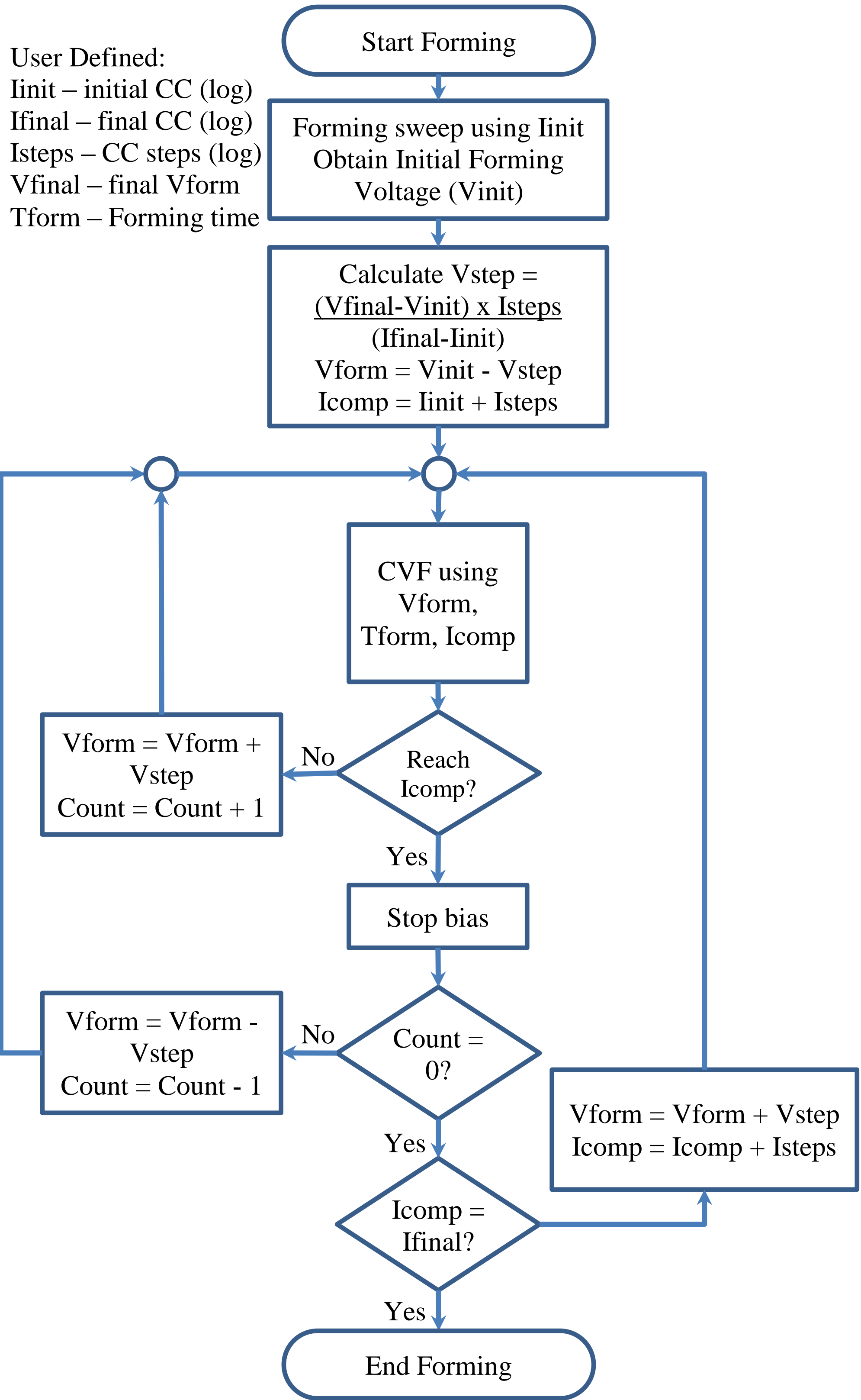

Figure 4.10. Flow chart showing the algorithm used for "soft" forming through constant voltage forming (CVF) and increasing compliance current.

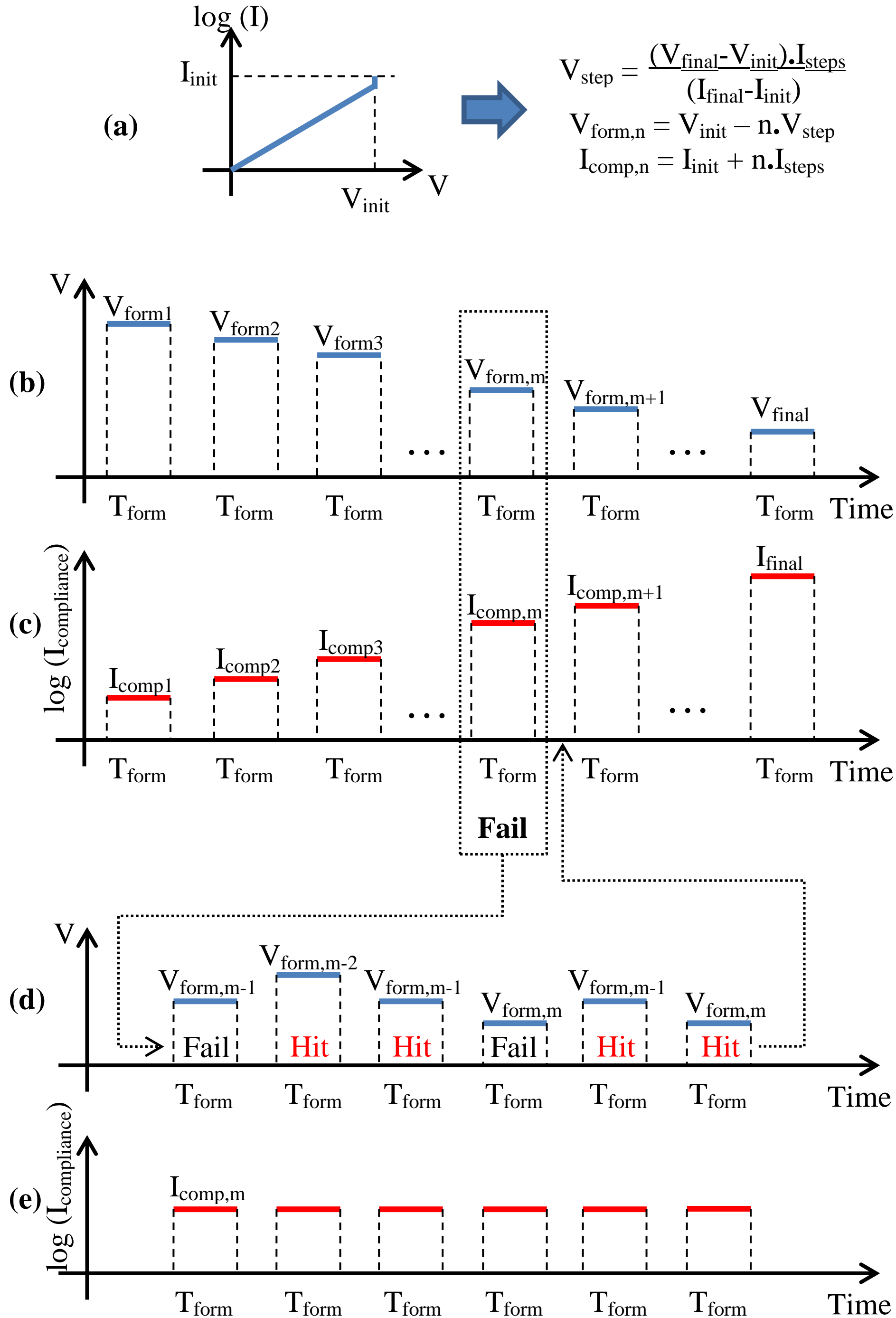

Figure 4.11. Waveforms illustrating the multi-step CVF method, starting with (a) initial voltage sweep to determine V_{init}, (b) CVF with decreasing V_{form} with each step of duration T_{form} and with (c) increasing I_{comp}. (d) Voltage and (e) current compliance waveforms in the event forming fails at the mth step.

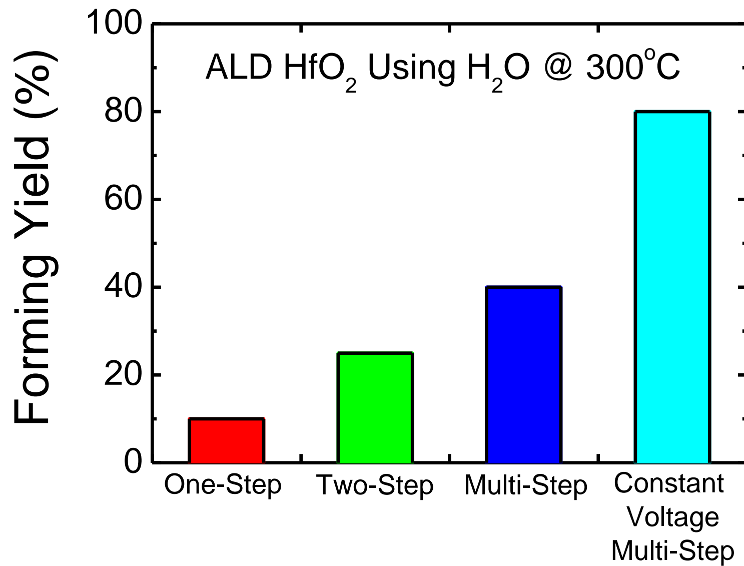

Figure 4.12. Forming yield dependence on the forming method, obtained from 20 different RRAM cells with ALD HfO_2 deposited at 300°C using H_2O.

Figure 4.13 shows the typical switching curves after CVF forming and using CC of 1 mA. It is clear from the 20-cycle switching characteristics that the memory window is reducing over cycles. This was believed to be due to the high CC as well as current overshoot beyond the CC causing a widening of the CF over cycles, as with "hard" forming. Thus, the CF gradually becomes harder to annihilate and RESET cannot achieve a lower current as before. A lower CC of 500 μA was then used on a different RRAM cell, and the switching characteristics shown in Figure 4.14. After 10 cycles, the RRAM cell showed little change in the memory window, showing that it is indeed the high CC that is causing the memory window to reduce. The importance of not only the forming process, but also SET process, can be seen from these experiments.

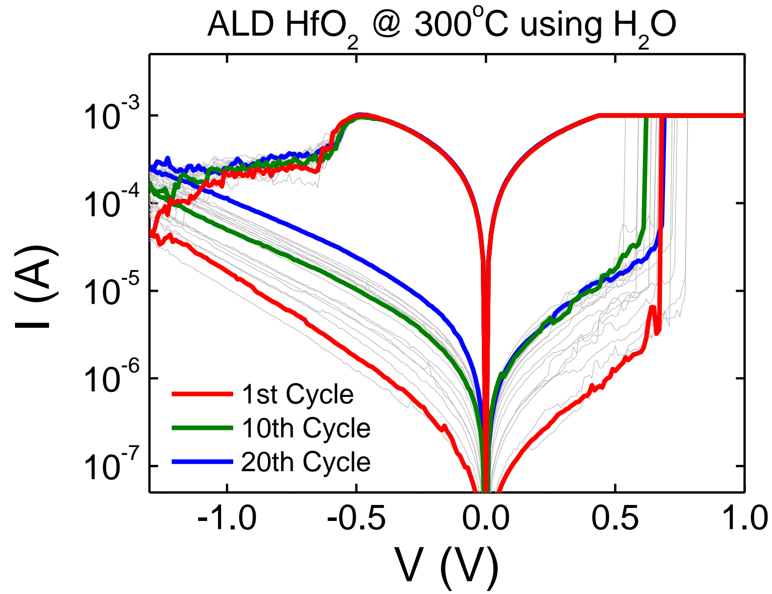

Figure 4.13. The 20-cycle I-V sweep of the TiN/Ti/HfO_2/TiN RRAM cell, with ALD HfO_2 at 300°C using H_2O, showing large RESET characteristics (1 mA current compliance) but with memory window reducing over cycles.

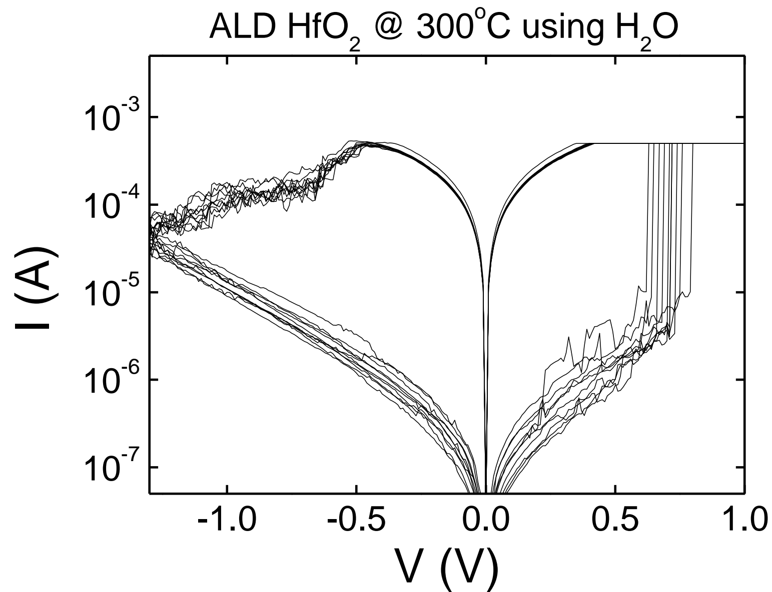

Figure 4.14. The 10-cycle I-V sweep of a large RESET RRAM device, but using lower current compliance of 500 μA, showing little or no reduction in memory window.

Figure 4.15 shows the 500-cycle endurance test on a large RESET RRAM cell. The cell is able to maintain a memory window of > 10x up till about 200 cycles, after which a serious degradation is observed and no memory window exists, ie. no switching. It can be seen that HRS had a gradual reduction until a large drop in resistance occurred around the 200th cycle. This is similar to the RRAM cell characteristics in Figure 4.13, indicating it is possibly due to gradual widening of the CF until it went into high current switching operation after the 200th cycle. Beyond this, the CC of 500 μA is insufficient to properly SET the cell and so it remained in the new HRS level of ~ $10^4\Omega$.

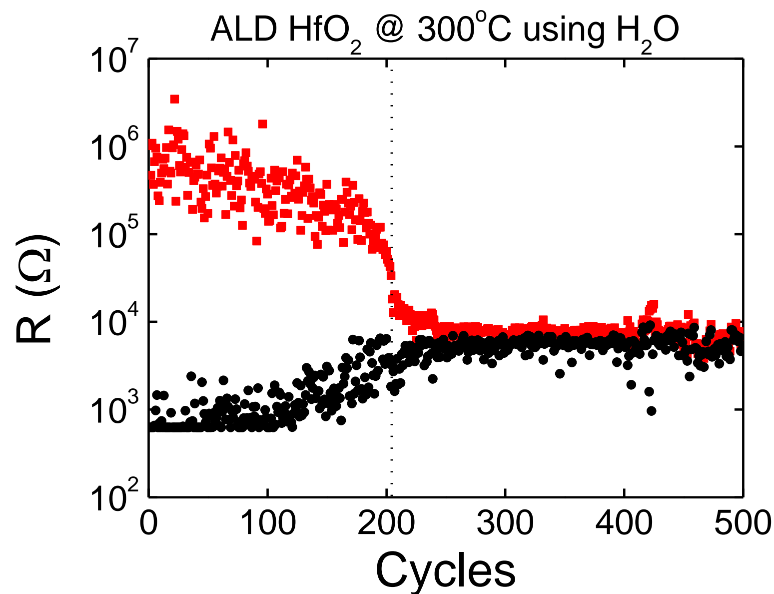

Figure 4.15. DC endurance cycling of TiN/Ti/HfO_2/TiN RRAM cell (ALD HfO_2 at 300°C using H_2O) up to 500 cycles showing serious degradation after 200 cycles.

4.2.2. Switching at Low Currents

By setting a lower final compliance current of $10^{-4.4}$ A (~40 μA) during the CVF forming, the RRAM device was found to switch at lower currents by using a subsequent compliance current of 50 μA for cycling. Figure 4.16 shows 10 typical cycles of such low current switching. All the currents were observed to be lower than 100 μA. It was also noticed that the curves were a little noisy and there were some current/resistance variations, especially for the HRS. Such noisy characteristics were also observed in the low current switching 1T1R cell presented in Chapter 2.2 and also the Ni-silicide BE cell presented in Chapter 3.2, although this RRAM is with higher current and less noise.

To investigate cycle-to-cycle variations, the device was cycled through 1000 DC cycles, with the resistances of each cycle plotted in Figure 4.17. This particular RRAM device had a fairly low variation in the HRS, resulting in an effective memory window of about 4x. However, a similar RRAM device that underwent the same forming and 1000 DC cycles did not fare so well. Figure 4.18 shows the resistances over the 1000 cycles of this particular cell. The HRS variation is clearly much larger, resulting in a smaller effective memory window of less than 2x.

This shows that the device-to-device variation is large when operating under low current switching. Since the major difference comes from the HRS, which shows larger variation as shown in Figure 4.18, this means the variation arises from the RESET process. From the I-V characteristics in Figure 4.16,

the HRS (low current region) also shows large variations in general. This could be due to the narrow CF formed, which should be narrower than the CF in devices showing large RESET. The narrower the CF, the more sensitive it is to generation, annihilation or movement of oxygen vacancies. For the RESET process, there could be generation or movement of oxygen vacancies, instead of only annihilation, to form or partially form the CF. This creates a noisy I-V during RESET, as can be observed in Figure 4.16, around -1V to -0.5V for the RESET process. Depending on when the RESET process is stopped, the current level in the HRS can vary, as determined by the noise.

It was further observed that the device with lower HRS variation (Figure 4.17) had a lower LRS, strongly indicating a wider CF, compared to the device with higher HRS variation (Figure 4.18). This further confirms the increase in HRS variation as a result of narrower CF and the cause of device-to-device variation to be from how well the CF size is controlled during forming. Such requirement on controlling CF size would further increase the dependence on the forming process. Therefore, operating under such low current switching may not be the best option for a reliable RRAM cell.

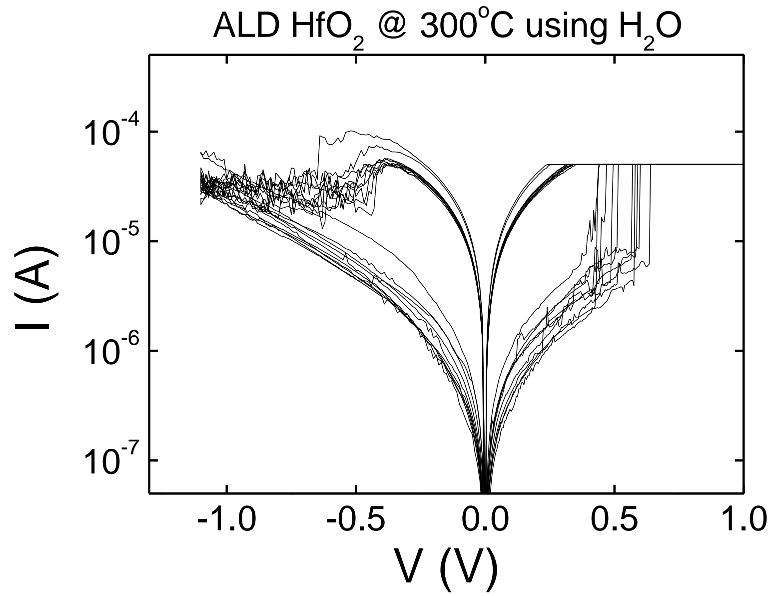

Figure 4.16. The 10-cycle I-V sweep of the TiN/Ti/HfO_2/TiN RRAM cell, with ALD HfO_2 at 300°C using H_2O, showing low current switching by using lower current compliance of 50 μA.

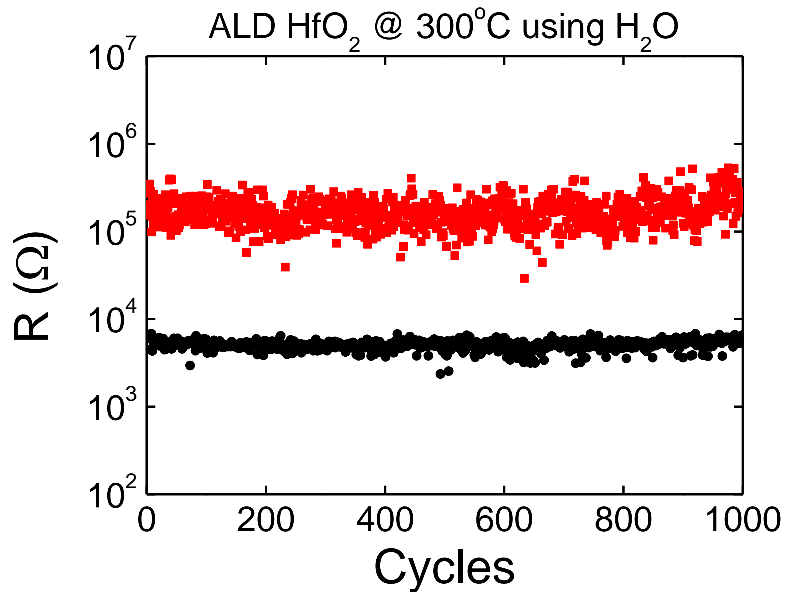

Figure 4.17. DC endurance cycling of TiN/Ti/HfO_2/TiN RRAM cell (ALD HfO_2 at 300°C using H_2O) up to 1000 cycles under low current switching.

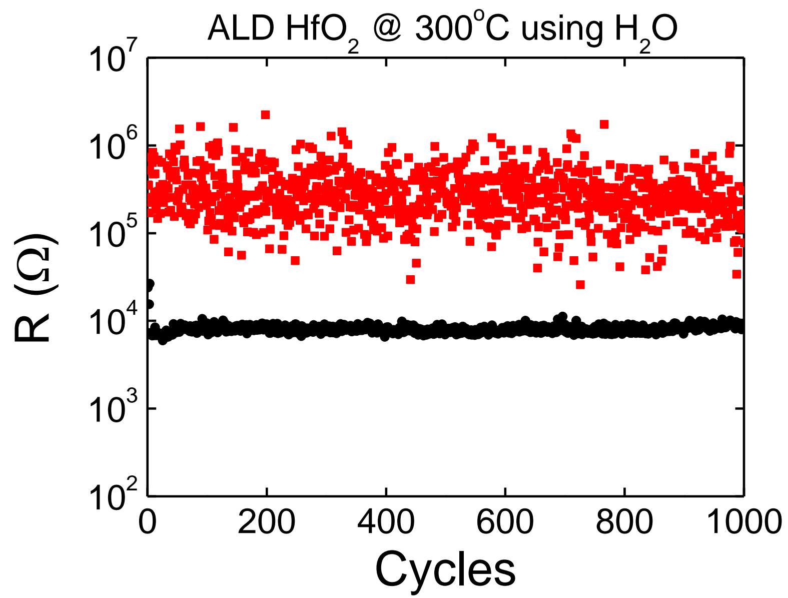

Figure 4.18. DC endurance cycling of TiN/Ti/HfO_2/TiN RRAM cell (ALD HfO_2 at 300°C using H_2O) up to 1000 cycles under low current switching but with large resistance variations.

4.3. ALD HfO_2 Using Dual Reactants

In order to further improve the performance of the HfO_2-based RRAM, a pure switching material free from impurities may be required. To achieve higher purity through ALD, a combination of H_2O and O_3 was used to deposit ALD Al_2O_3 and found to have lower hydrogen and carbon impurities [47]. Using only H_2O as the oxidant would tend to leave higher H content as the surface after each cycle is –OH terminated. Using only O_3 would leave –O– terminated surface, reducing the H content, but as explained in Section 1.7, the carbon-containing by-products incorporate a higher C content. By introducing O_3, but only after H_2O, would oxidize the H from the –OH surface along with any chemisorbed carbon compounds, leaving –O– surface and reducing H and C impurities in the resultant film. The lower impurity level may also result in improved crystallinity, as observed with TiN and V_2O_5 ALD films [48]. Impurities incorporated during deposition may disrupt the continuity of the crystal growth and prevent crystallization, especially if bonded with the Hf. This creates defects which may propagate to form grain boundaries as each monolayer is deposited. So a higher purity of the film would tend to improve crystallinity.

This method of using H_2O and O_3 together as oxidants (H_2O+O_3) was used to deposit ALD HfO_2 at substrate temperature of 300°C and the film analyzed with time-of-flight secondary ion mass spectroscopy (TOF-SIMS) and also x-ray diffraction (XRD). The analyses were also performed on ALD HfO_2 films using H_2O @ 250°C, H_2O @ 300°C, O_3 @ 250°C, and O_3 @ 300°C for comparison. Figures 4.19 and 4.20 show the intensity of H and C,

respectively, from TOF-SIMS analysis, normalized to the intensity of Si from the substrate. It can be seen that H_2O+O_3 @ 300°C has the lowest H and C concentration within the HfO_2 film. So using H_2O+O_3 should give HfO_2 films with lower H and C impurities. It can also be noted that although the O_3 @ 250°C process has similarly low H impurity as the H_2O+O_3 @ 300°C process, the C impurity is a lot higher. The O_3 @ 300°C does have lower C impurity than at 250°C, although still higher than the H_2O processes, but the H impurity is higher. The overall higher impurity levels of the O_3 processes compared with H_2O processes might have contributed to the higher switching currents as presented in Chapter 4.2.

Figure 4.21 shows the XRD spectra of the three different ALD HfO_2 films. It is clear that the H_2O @ 250°C had no obvious peaks, indicating either an amorphous film or polycrystalline film with grains too small to leave any diffraction peaks. The XRD spectra from the other two films show typical monoclinc HfO_2 diffraction peaks, with H_2O+O_3 @ 300°C having stronger peaks.

Figure 4.22 shows the diffraction peak for the (-111) plane, which is the largest peak. Using the Scherrer equation, the grain sizes were estimated from the full-width at half-maximum (FWHM) and Bragg angle of the (-111) XRD peak. The H_2O+O_3 @ 300°C was found to have larger grain size than H_2O @ 300°C, with H_2O @ 250°C having much smaller grain sizes less than 14 nm. Grain boundaries have been found to play an important role in facilitating the formation of the CF [25], with intersection points of three or more grain boundaries aiding spatial extension of the CF. Having smaller grain sizes

results in a higher chance of such intersection points occurring within a certain volume, and would thus tend to have a wider CF. HfO_2 with larger grains would be expected to have more direct grain boundary paths and narrower CF which should result in better forming yield and performance.

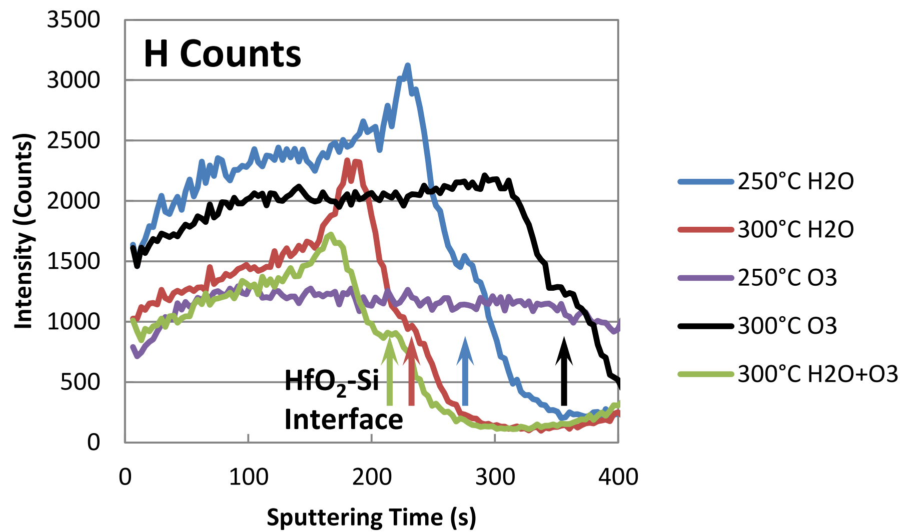

Figure 4.19. The H counts obtained from time-of-flight secondary ion mass spectroscopy (TOF-SIMS) measurements on ALD HfO_2 with different conditions.

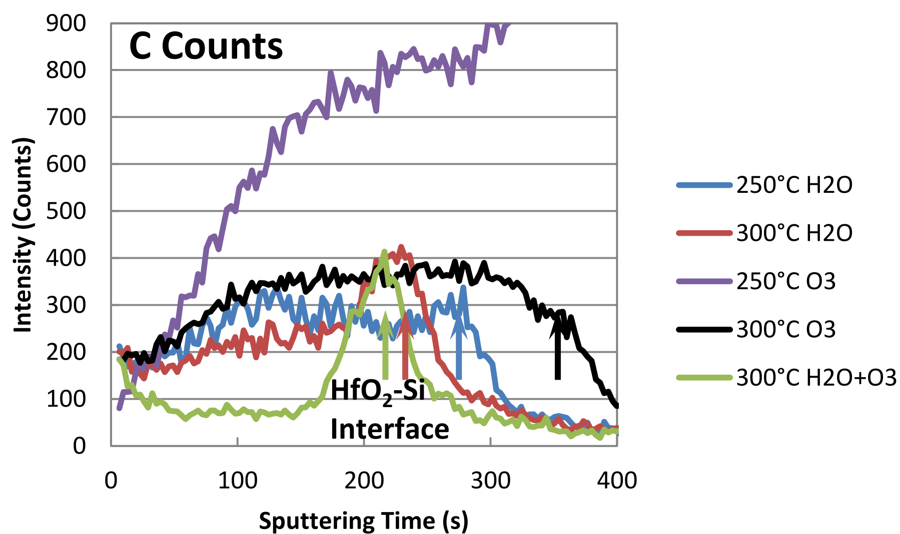

Figure 4.20. The C counts obtained from TOF-SIMS measurements on ALD HfO_2 with different conditions.

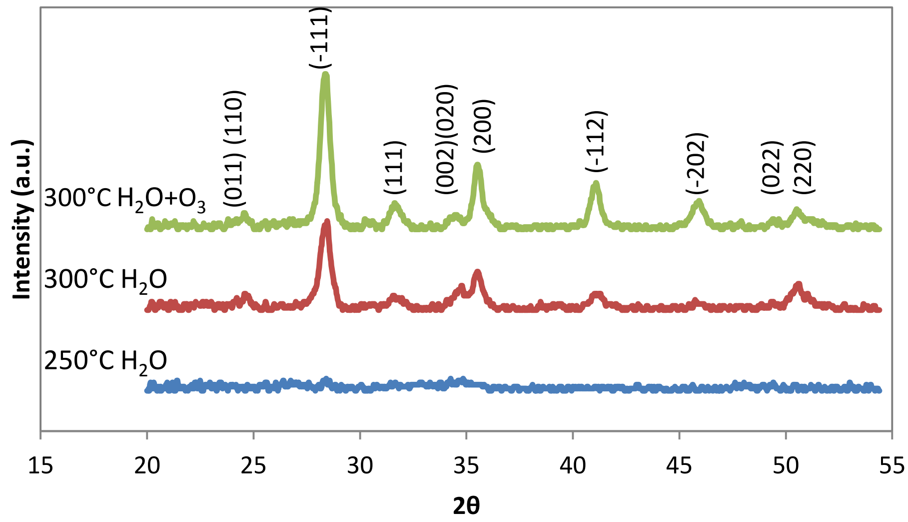

Figure 4.21. X-ray diffraction (XRD) spectra of ALD HfO_2 with various conditions, showing monoclinic HfO_2 structure for two conditions.

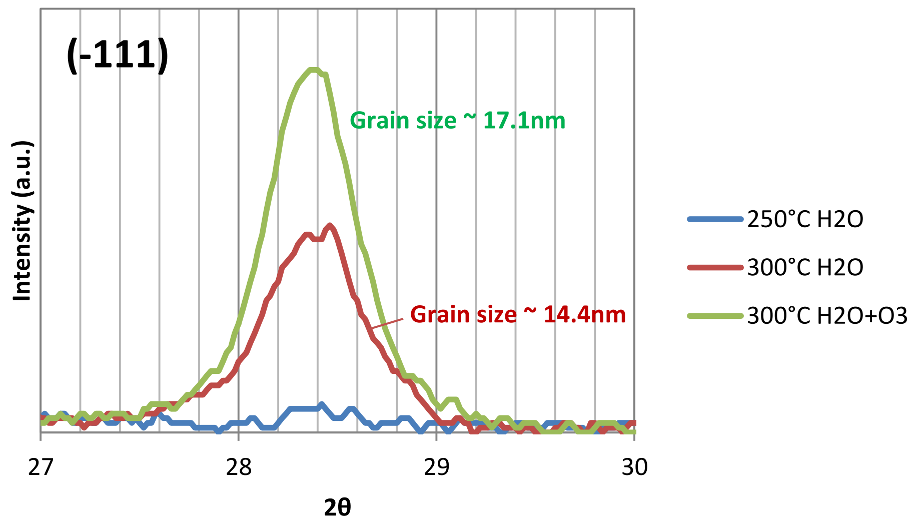

Figure 4.22. The XRD peak of (-111) plane of each ALD condition for HfO_2, together with average grain size estimated from applying the Scherrer equation.

The new ALD method of using both H_2O and O_3 was used to deposit HfO_2 in TiN/Ti/HfO_2/TiN RRAM cells and the performance compared with the other conditions. Figure 4.23 shows the forming yield of three different ALD conditions. It was found that ALD HfO_2 using H_2O @ 250°C was also able to achieve "soft" forming and allow large RESET, although at much lower chances. The ALD HfO_2 split using H_2O+O_3 @ 300°C had even higher forming yield than the ALD HfO_2 split only using H_2O. As expected, the trend is consistent with the grain size. Figure 4.24 shows the 500-cycle DC endurance performance of the RRAM cell using H_2O+O_3 ALD condition. There is a small improvement of 250 cycles to failure compared to the 200 cycles for H_2O condition in Figure 4.15. However, it should be noted that the HRS has a very large variation.

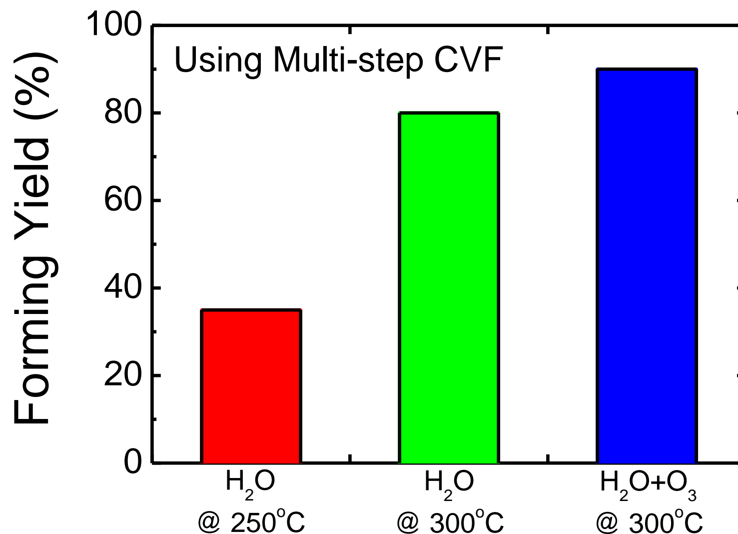

Figure 4.23. Forming yield dependence on the ALD HfO_2 conditions, obtained from 20 different RRAM cells and using multi-step CVF method.

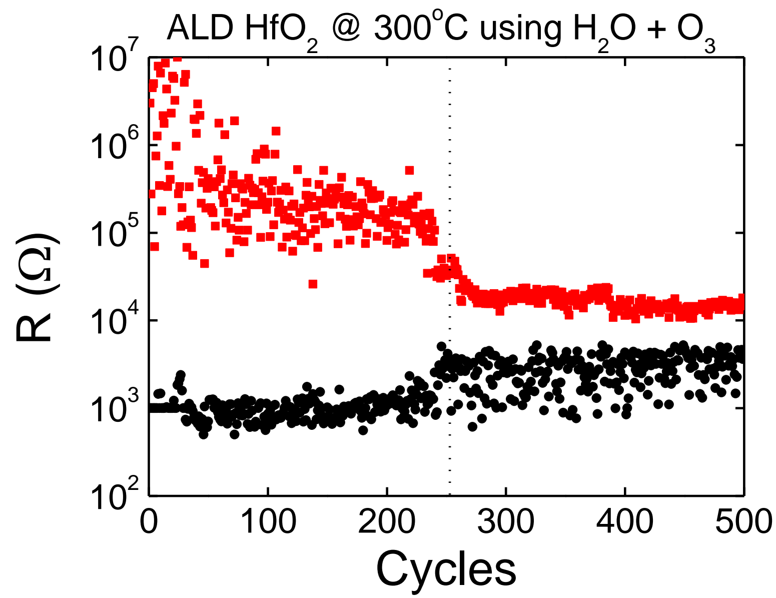

Figure 4.24. DC endurance cycling of TiN/Ti/HfO_2/TiN RRAM cell (ALD HfO_2 at 300°C using H_2O + O_3) up to 500 cycles showing some degradation after 250 cycles.

To understand the dominant conduction mechanism of the RRAM cell, the I-V characteristics of the LRS under large RESET operation were collected at various temperatures from 25°C to 65°C. By studying the relationship between resistance, R, current, I, and temperature, T, the conduction mechanism can be determined, as described in Chapter 1.6. Fitting the data into R-T plot for metallic conduction, ln(R)-$T^{-1/4}$ plot for Mott's Law describing electron hopping between traps, or ln(I/T^2)-1/T plot for Schottky emission, the best fit was found to be for Schottky emission (Figures 4.25 and 4.26).

The obtained ϕ_B from Figure 4.25 was 0.17 eV, which is close to the conduction band offset for TiO_2 with TiN. It is likely that a TiON layer was grown upon exposure to air between the PVD TiN BE process and ALD HfO_2 deposition, thus creating a Schottky barrier. The TiON could also arise from the oxygen gettering properties of TiN, thus forming TiON. Using an estimate of the ε_r of TiON, ~24.2 [49], and following Equation (9), d was estimated to be 3.1 nm. The ϕ_B was also extracted for RRAM cells operating under high current switching (0.12 eV), like in Figure 4.2, and also low current switching (0.24 eV). It appears that there could be some barrier lowering due to the oxygen vacancies generated during the forming and SET process, since high current switching, which should have more oxygen vacancies, had lower barrier, and low current switching, which should have less oxygen vacancies, had a higher barrier. Hence, it is likely that this TiON or TiO_2 interfacial layer plays a role in the switching.

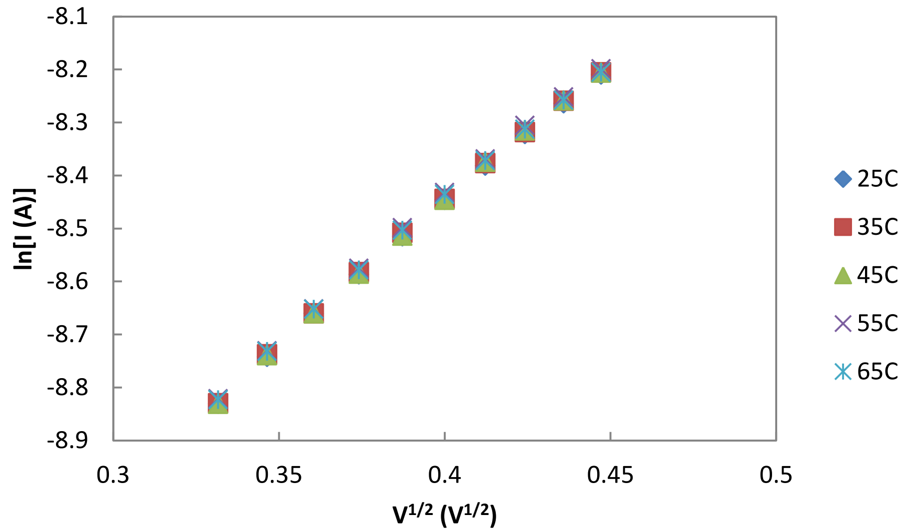

Figure 4.25. Plot of ln(I)-$V^{1/2}$ at various temperatures, showing a linear curve.

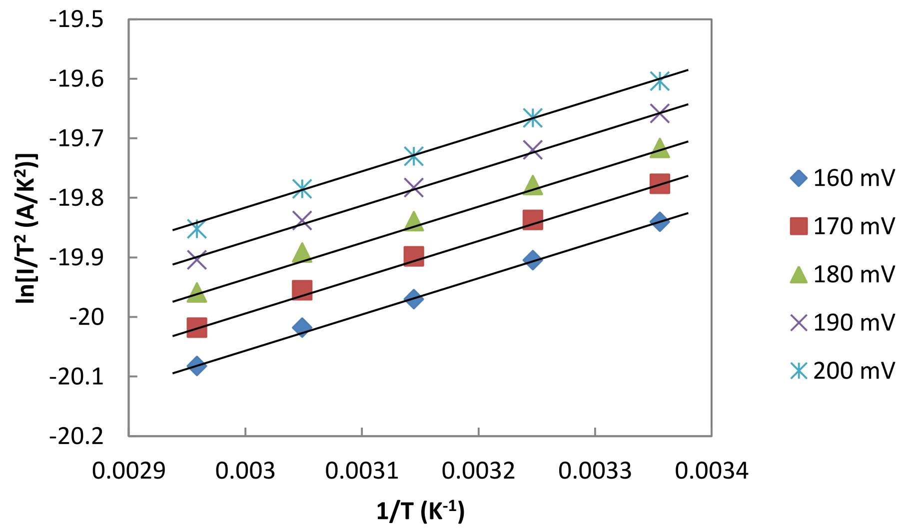

Figure 4.26. Plot of ln(I/T^2)-$V^{1/2}$ at various temperatures, showing a linear curve.

4.4. ALD HfO_2 with TiO_2 Buffer Layer

To investigate the improvement, if any, of deliberately increasing the interfacial TiO_2 layer, a 5 nm TiO_2 layer was added between TiN BE and HfO_2, deposited using ALD. Also, although using H_2O+O_3 to deposit ALD HfO_2 had improvement in forming yield, the endurance and HRS variation is still a problem. Since the RRAM cell is able to do large RESET, the off current is much lower. But this also causes a large SET, whereby the current jump during SET is much larger. This increases the chances and also the amount of current overshoot beyond the compliance current, causing endurance failure over cycles. In order to prevent overshoot, the TiO_2 would hopefully act as a buffer layer to protect the device.

Figure 4.27 shows 10 cycles of the RRAM cell with TiO_2 buffer layer and using H_2O+O_3 ALD HfO_2. The initial memory window was found to be mostly larger than the H_2O ALD HfO_2 counterpart (almost 10^4x). Since the TiN BE may also draw oxygen from HfO_2 to form oxygen vacancies and make the RRAM cell harder to RESET, by adding the TiO_2 layer, such an influence of the TiN BE is reduced and allow a larger RESET. Figure 4.28 shows the 500-cycle DC endurance test which was observed to be better than previous RRAM cells. Although the memory window reduces up to the 200th cycle, a 100x window is still maintained up till around the 350th cycle where the HRS starts to have more degradation. However, even after this degradation, there is still a window of ~10x. Most notably, there is much lesser variation in the HRS. The presence of the TiO_2 likely prevented some

current overshoot from occurring, thus allowing the RRAM cell to last more cycles before degrading.

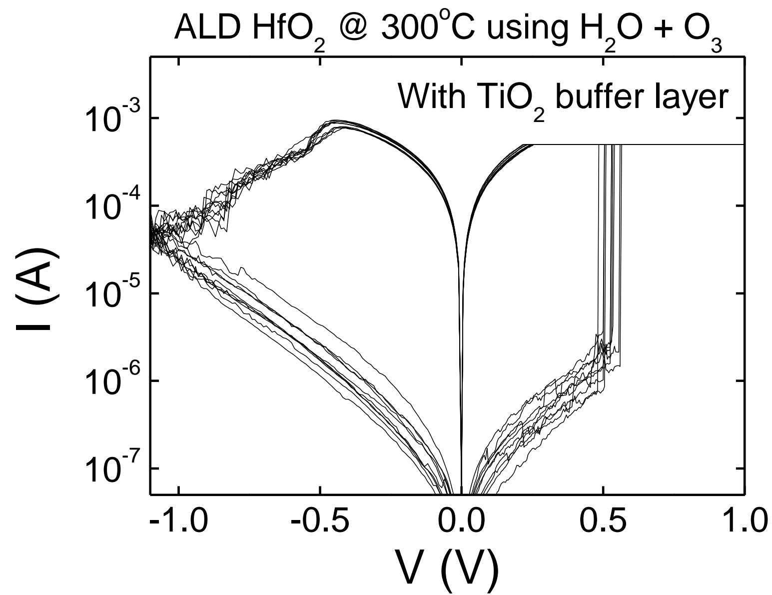

Figure 4.27. Ten DC cycles of $TiN/Ti/HfO_2/TiO_2/TiN$ RRAM cell (ALD HfO_2 at 300°C using $H_2O + O_3$) with large RESET.

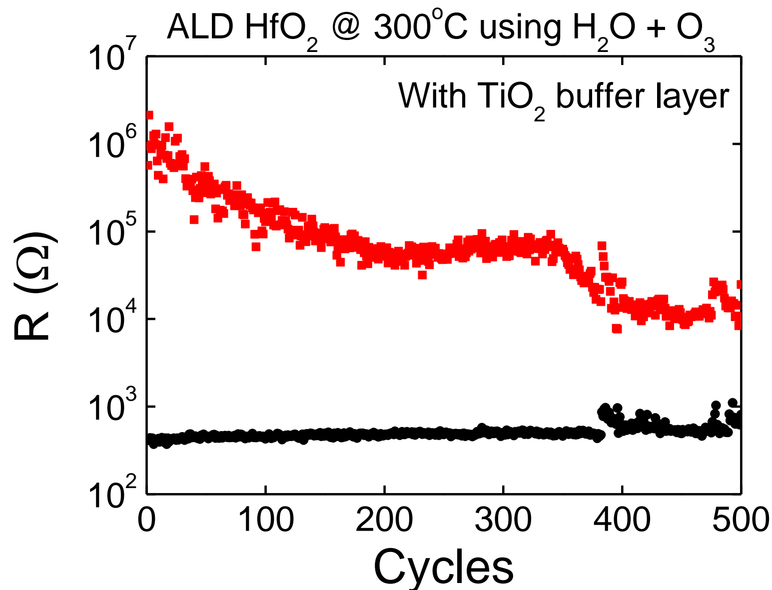

Figure 4.28. DC endurance cycling of $TiN/Ti/HfO_2/TiO_2/TiN$ RRAM cell (ALD HfO_2 at 300°C using $H_2O + O_3$) up to 500 cycles showing some degradation, but still maintaining a memory window > 10x.

4.5. Summary

In this chapter, material engineering was used to improve the characteristics of TiN/Ti/HfO_2/TiN RRAM cells. Through the use of ALD, various deposition methods and conditions were used and their impact on the RRAM performance were studied.

First, the study of ALD substrate temperature, 250°C and 300°C, and also oxidant, H_2O and O_3, showed RRAM cells deposited using O_3 tended to have higher switching currents, likely due to a higher carbon content incorporated during ALD. ALD HfO_2 RRAM cells using H_2O as the oxidants had lower switching currents and the condition using 300°C substrate temperature had the largest memory window.

Further testing of the H_2O @ 300°C condition revealed a large RESET phenomenon when the RRAM cell is formed through a two-step voltage sweep. This was attributed to a narrow CF being formed gradually through multi-step forming, allowing easier annihilation of the CF and resulting in lower currents after RESET. A refinement of the forming method was done to improve the forming yield. A constant voltage forming (CVF) multi-step forming process was thus created, which resulted in a significant improvement in forming yield. The CVF method basically involves applying a constant forming voltage at each step, with increasing compliance current and reducing forming voltage in subsequent steps, up to the final compliance current. The RRAM cell was able to endure about 200 DC cycles before the memory window reduced to zero.

Using the multi-step CVF method and setting a low final compliance current of ~40 µA, the RRAM device could switch at lower currents (<100 µA). This is likely due to an even narrower CF. However, it was found that the narrower CF resulted in larger resistance variation, especially for HRS. As such, operating under low current switching is not suitable for a reliable RRAM cell.

Next, a new ALD process using dual oxidants, H_2O followed by O_3, was introduced. HfO_2 films deposited through this H_2O+O_3 process were found to have lower carbon and hydrogen impurities, from SIMS analysis, compared with those deposited using H_2O at 250°C and 300°C. The higher purity of the HfO_2 films also resulted in a more crystalline film, as evidenced through XRD analysis of the grain sizes. The RRAM cells incorporating HfO_2 films deposited with H_2O+O_3 not only had higher forming yield using multi-step CVF method, the DC endurance was found to degrade only after 250 cycles, but still maintaining a memory window of >2x after 500 cycles. Through analysis of the temperature dependence of the conduction, a TiON or TiO_2 interfacial layer was believed to play a role in the switching.

Finally, to study the effect of TiO_2 on the RRAM cell, a 5 nm ALD TiO_2 was included into the RRAM cell, resulting in a TiN/Ti/HfO_2/TiO_2/TiN cell, with HfO_2 deposited using H_2O+O_3. This RRAM cell could achieve a much larger memory window of almost 10^4x, and could endure 500 DC cycles with >10x window. This shows that TiO_2 layer does improve the reliability of the RRAM cell over more cycles.

Chapter 5 : Summary and Recommendations for Future Work

5.1. Summary

This thesis has presented improvements to the HfO_2-based RRAM by increasing the memory window and reducing the resistance variations, effectively increasing the margin for programming or read errors.

The major findings and contributions are listed as follows:

1) Achieving a 1T1R cell within $4F^2$ footprint, featuring a TiN/Ni/HfO_2/n^+-Si RRAM cell integrated on the VSNWFET. The cell could operate in three different modes: unipolar, bipolar, and bipolar with low current switching. Of the three modes, the bipolar mode was found to have the least variation, with over 10x memory window even after considering cycle-to-cycle and cell-to-cell variations.

2) Observation of parasitic SET during RESET cycles for TiN/HfO_2/Ni-silicide RRAM cells with high Ni concentrations in Ni-silicide (> 49.3%), which is attributed to the injection of Ni into the HfO_2 material and forming a parasitic filament. Thus, care has to be taken to avoid high RESET voltages and cause parasitic SET.

3) Discovery of low current switching for TiN/HfO_2/Ni-silicide RRAM cells with low Ni concentrations in Ni-silicide (< 47.9%), which was determined to be due to the SiO_2 interfacial layer between HfO_2 and Ni-silicide creating a tunneling barrier and controlling the filament size.

4) Large memory window of 1000x was found to be possible in TiN/Ti/HfO_2/TiN RRAM cells with ALD HfO_2 deposited using H_2O oxidant at 300°C substrate temperature.

5) Established a new method of forming using multi-step constant voltage forming, allowing TiN/Ti/HfO_2/TiN RRAM cells to operate with large memory window and also improving the forming yield.

6) Developed a new ALD HfO_2 process involving both H_2O and O_3, which increased the film grain size and also improved the forming yield and endurance of TiN/Ti/HfO_2/TiN RRAM cells.

7) Inclusion of a TiO_2buffer layer between HfO_2 and TiN BE was found to further increase the memory window and reduce the resistance variations.

5.2. Recommendations for Future Work

Although the TiN/Ti/HfO_2/TiO_2/TiN RRAM cell showed almost 10,000x memory window, there is still further improvement needed for the endurance. Ideally, the buffer layer should act as a barrier layer for oxygen drift or diffusion into the BE and also as a current limiter, without any switching or breakdown occurring. It is likely that the thin TiO_2 was unable to withstand the high fields and currents, causing it to breakdown. Therefore, either a thicker TiO_2 or another material, like Al_2O_3 or Ta_2O_5, could be investigated for further improvement of the endurance.

Alternatively, a good current limiter would be a transistor, which can also alter its series resistance through the gate voltage. So the switching and buffer layers would not experience high currents that could damage either material. The performance of the one-transistor-one-resistor (1T1R) RRAM cell could be investigated by integrating the RRAM cell with the source/drain of the transistor. Endurance improvement is expected since the switching and buffer layers are both protected from irreversible damage.

To further increase the forming yield, a forming-free RRAM cell could be investigated. Reducing the thickness of the HfO_2 should reduce the forming voltage sufficiently until it coincides with the SET voltage, thus creating a forming-free cell. This would completely eliminate the need for a forming process, saving time and would result in higher yield.

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Journals

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