

**OPTIMAL PULSE WIDTH MODULATION OF
MULTILEVEL INVERTERS FOR MEDIUM
VOLTAGE DRIVES**

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NATIONAL UNIVERSITY OF SINGAPORE

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MULTILEVEL INVERTERS FOR MEDIUM
VOLTAGE DRIVES**

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DECLARATION

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

R. Amarendra

Amarendra Edpuganti

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Summary

Low device switching frequency modulation of multilevel inverters (MLIs) for medium voltage drives is essential to increase semiconductor device utilization, minimize cooling requirements and achieve higher overall system efficiency. However, there exists a trade-off between device switching frequency and harmonic distortion of machine stator currents. Therefore, classical modulation techniques such as sinusoidal pulsewidth modulation and space vector modulation techniques utilize higher device switching frequency (around 1 kHz) to generate good quality of machine stator currents. Based on the literature survey of several low device switching frequency modulation techniques, it has been identified that synchronous optimal pulsewidth modulation (SOP) is an effective and emerging modulation technique to achieve better quality of machine stator currents.

Till now, SOP has been demonstrated for classical three-level and five-level MLIs. On the other hand, the present trend in MV high power drives is to use MLIs with higher number of voltage levels to achieve better quality of output voltage waveforms. Also, several new topologies have been proposed as an alternative to classical MLI topologies and some of them found industrial relevance as well. Therefore, there is a need to analyze and propose modifications to the state-of-the-art SOP technique in order to modulate MLIs with any number of voltage levels and also emerging MLI topologies.

One of the main goal of the thesis is to develop systematic analysis to implement state-of-the-art SOP technique for MLIs with any number of voltage levels. The developed analysis has been utilized to modulate cascaded seven-level and nine-level MLIs with peak device switching frequency limited to rated fundamental frequency (50 Hz). However, it has been noticed that power semiconductor devices operate at unequal device switching frequency and peak device switching frequency is not limited to desired value. Subsequently, modified SOP technique has been proposed to overcome these issues. The proposed technique has been utilized to mod-

ulate seven or higher-level MLIs with peak device switching frequency set at rated fundamental frequency (50 Hz).

Also, the thesis has explored the feasibility of implementing SOP technique for one of the emerging topology known as modular multilevel converter (MMC). One of the main challenges for modulation of MMC is to achieve balanced floating capacitor voltages. Based on the study, a systematic algorithm has been developed to implement SOP for MMC topology. The proposed technique has been demonstrated for five-level MMC with peak device switching frequency set at 2000 Hz.

In addition, the thesis has investigated the issue of common-mode currents in machine stator windings for the dual inverter based MLI fed open-end stator winding induction motor drives. An enhanced SOP technique has been proposed to achieve high quality stator currents with elimination of common-mode currents, while operating power semiconductor devices at few hundred Hertz. Finally, dual n L-MMC topology has been proposed for open-end stator winding induction motor drives, which can be operated from a single dc source and generates any number of voltage levels. The proposed technique has been demonstrated experimentally with low power prototypes of dual two-level, dual three-level and dual three-level MMC topologies.

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List of Acronyms

AFE	Active-front end
ANPC	Active neutral-point-clamped
CCS	Continuous control set
CHB	Cascaded H-Bridge
CMV	Common-mode voltage
D2L	Dual two-level
D3L	Dual three-level
DTC	Direct torque control
EMI	Electromagnetic interference
FC	Flying capacitor
FCS	Finite control set
FMCC	Forced machine current control
GPC	Generalized predictive control
GTO	Gate turn-off thyristor
HNPC	H-Bridge with neutral-point-clamped phase leg
HV	High voltage
HVDC	High voltage direct current
IGBT	Insulated-gate bipolar transistor
IGCT	Integrated-gate commutated thyristor
LDSF	Low device switching frequency
LV	Low voltage
MLC	Multilevel converter
MLI	Multilevel inverter
MMC	Modular multilevel converter
MPC	Model predictive control
MPDCC	Model predictive direct current control
MPDTC	Model predictive direct torque control
MP ³ C	Model predictive pulse pattern control

MV	Medium voltage
NLC	Nearest level control
NPC	Neutral-point-clamped
NPP	Neutral-point-potential
NVC	Nearest vector control
OPP	Optimized Pulse Pattern
PMSG	Permanent magnet synchronous generator
PWM	Pulsewidth modulation
SPWM	Sinusoidal pulsewidth modulation
SHE	Selective harmonic elimination
SHM	Selective harmonic mitigation
SVC	Space vector control
SVM	Space vector modulation
SOP	Synchronous optimal pulsewidth modulation
TCC	Transistor clamped converter
TDD	Total demand distortion
THD	Total harmonic distortion
VNPC	Vienna neutral-point-clamped

List of Symbols

α_i	Switching angles or instants ($i=1,2,\dots,N$)
d	Distortion factor
f_1	Fundamental frequency
f_{1R}	Rated fundamental frequency
f_s	Device switching frequency
$f_{s,avg}$	Average device switching frequency
$f_{s,max}$	Maximum device switching frequency
i_h	Harmonic rms current
$i_{h,six-step}$	Harmonic rms current at six-step operation ($m = 1$)
k	k^{th} order harmonic component
i_k	Amplitude of k^{th} order harmonic component of converter output current
l_σ	Leakage inductance of induction motor
m	Modulation index
N	Pulse number
nL	n -level ($n=2,3,4,5,\dots$)
$s(i)$	Slope of switching transition at switching angle α_i ($i= 1,2,3, \dots, N$)
u_k	Amplitude of k^{th} order harmonic component of converter phase output voltage
$u_{k,six-step}$	Amplitude of k^{th} order harmonic component of converter phase output voltage at six-step operation ($m = 1$)
V_{peak}	Peak value of converter output voltage
w_1	Fundamental frequency of stator current

Chapter 1

Introduction

This Chapter presents the introduction of the thesis. The background behind motivation of this thesis is given in Section 1.1. The literature review of LDSF modulation techniques and emerging MLC topologies is presented in Section 1.2. Comparison of several LDSF modulation techniques is done in Section 1.3. The research problem and research objectives of the thesis are discussed in Section 1.4. The research contributions and outline of the thesis are given in Sections 1.5, and 1.6, respectively. This Chapter is concluded in Section 1.7.

1.1 Background

Development of novel converter topologies, new semiconductor devices, and innovative modulation techniques are essential to produce advanced power electronics technologies for modern applications. For high power applications, better efficiency can be obtained by increasing the voltage rating rather than current rating of power conversion system. There are two ways to handle increased voltage rating : (1) develop HV semiconductor devices, (2) develop new converter topologies with LV/MV semiconductor devices. Out of the two, development of new converter topologies known as MLCs have emerged as an attractive solution for MV/HV high power applications. The merits of MLCs over classical 2L converters are: higher operating volt-

age capability with matured LV/MV semiconductor devices, better output voltage waveform quality, lower harmonic distortion of input and output currents, reduced filters size, less $\frac{dv}{dt}$ stress, lower common-mode voltages, reduced electromagnetic interference, reduced torque ripple, and feasible fault-tolerant operation [2–10].

MLCs consist of an array of semiconductor devices and capacitive voltage sources, which can generate output voltage waveforms with multiple steps by appropriate switching. With increase in number of voltage levels or steps, the staircase output waveform approaches sinusoidal waveform. The classical multilevel topologies are NPC [11], FC [12] and CHB converters [13]. The topology of 3L-NPC has become popular due to its simple structure, but it has not been extended to higher level operation due to excessive losses of clamping diodes, uneven distribution of losses in inner and outer devices and unachievable dc-link capacitor voltage balance [14]. FC multilevel topologies are not suitable for high power applications due to requirement of higher device switching frequency to achieve capacitor voltage balance [15].

The CHB topology can achieve higher operating voltage by utilizing LV semiconductor devices. Due to modularity and scalability, the CHB topology has become industrial standard for high power and high quality demanding applications. However, the main disadvantage of CHB topology is the requirement of expensive and bulky phase-shifting multi-winding isolation transformer to provide large number of isolated dc sources [3].

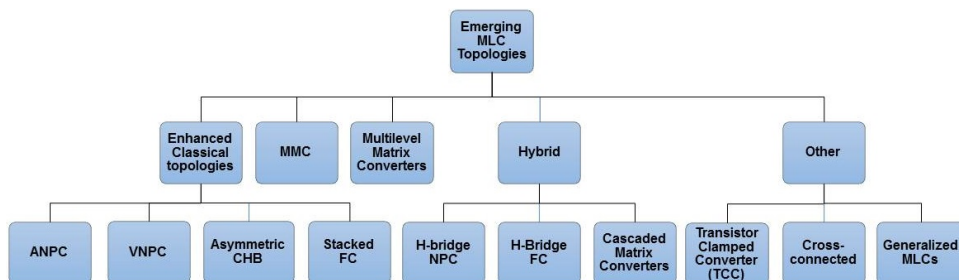


Fig. 1.1: Emerging MLC topologies

Therefore, applications such as traction, marine propulsion and wind power conversion, may not prefer CHB topology due to space and weight restrictions. Subsequently, several multilevel topologies have been proposed as classified in Fig. 1.1, with an aim to overcome the demerits of classical topologies, reduce the count of semiconductor devices for a given number of voltage levels, minimize the number of isolated dc sources, achieve easy scalability in terms of voltage and current, improve power density and so on [16–25].

In literature, numerous modulation techniques have been adapted or developed for MLCs. Although higher number of semiconductor devices leads to additional control complexity, MLCs provide extra degrees of freedom owing to higher number of switching states. SVM technique has been extended and generalized for n L-MLCs [26]. Classical SPWM has been extended for MLCs by using multiple carriers with either phase-shift (PS-PWM) or level-shift (LS-PWM) [27–29]. LS-PWM methods are better suited for NPC converters, whereas PS-PWM method is preferred for CHB and FC multilevel topologies [30]. The carrier based SPWM techniques require higher device switching frequency operation to obtain high quality waveforms. However, MLCs with higher number of voltage levels naturally improve the quality of waveforms and thus, it is possible to operate semiconductor devices with reduced switching frequency. For example, SPWM technique has been implemented with device switching frequency of 500 Hz for a 17L-HNPC inverter [31].

In MV high power drives, switching losses and conduction losses of power semiconductor devices are significant owing to high blocking voltages and commuted currents. However, thermal constraints of semiconductor devices and cooling system design impose limits on the total device losses. The conduction losses can be limited by proper selection of topology. The ideal topology is one, which has minimum number of series connected

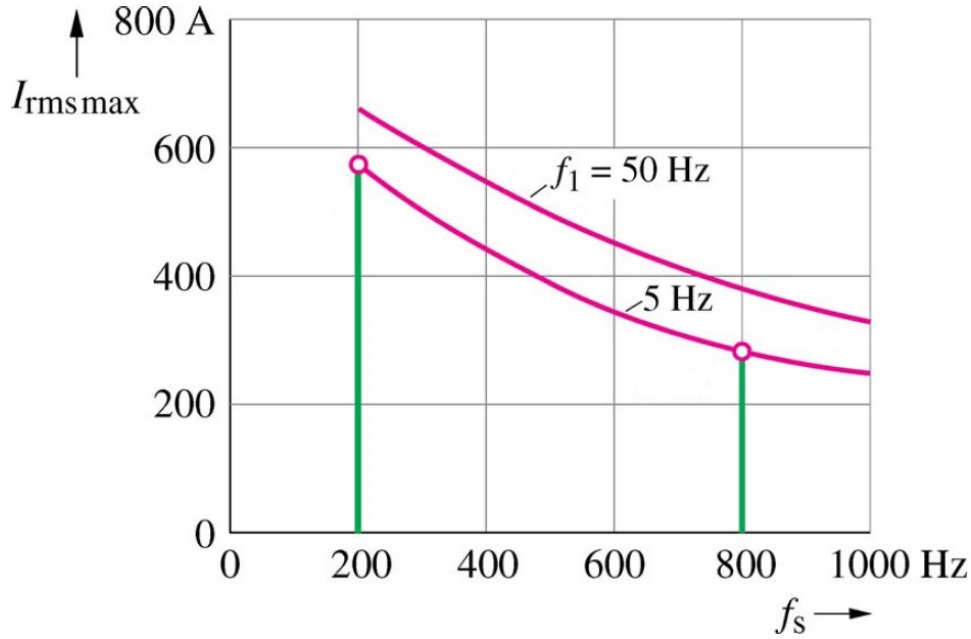


Fig. 1.2: Maximum device rms current versus f_s for EUPEC 6.5-kV 600-A IGBT module. (Courtesy of J. Holtz and X. Qi)

devices for different switching states. On the other hand, device switching losses can be limited by reducing device switching frequency. Due to thermal limits of power semiconductor devices, higher device switching frequency operation necessitates bringing down the device current to reduce the conduction losses and thus, it leads to significant derating of the converter. Therefore, LDSF modulation techniques are preferred in MV drives to achieve better device utilization. It should be observed from Fig. 1.2 that by limiting the device switching frequency to 200 Hz, the current-carrying capability of semiconductor device is almost doubled [1]. In addition, reduction of switching losses cut down cooling requirements that leads to further reduction in the manufacturing and operating cost as well as physical size of the equipment. Nonetheless, LDSF operation leads to penalty of higher harmonic distortion of converter output current waveforms and thus poses a research challenge.

1.2 Literature Survey

The Section presents literature survey of LDSF modulation techniques for high power applications, and emerging MLC topologies.

1.2.1 LDSF modulation techniques

The requirements of control and modulation schemes of MV drives are as follows : low device switching frequency due to thermal constraints of power semiconductor devices, lower harmonic current distortion to reduce the thermal losses in induction motor that lead to temperature rise and shortening of life span of machine, and fast dynamic response to handle sudden load changes, and speed transients. In practical applications, the device switching frequency is normally limited to around 200Hz for GTOs and 500Hz for IGBTs and IGCTs [32]. Major challenge is trade-off between device switching frequency and output power quality. However, the quality of output waveforms can be significantly improved by increasing the number of voltage levels. Thus, researchers are successful in bringing down the device switching frequency up to fundamental switching frequency owing to inherent benefits offered by multilevel topologies. The literature survey of LDSF modulation techniques is given next.

1.2.1.1 SVM

SVM techniques can effectively utilize the degrees of freedom offered by MLCs to achieve LDSF operation. A novel switching sequence design for the SVM of high-power MLCs optimized for minimizing device switching frequency and the improvement of harmonic spectrum has been proposed [33]. With this method, the device switching frequency has been maintained between 540 to 630 Hz for a 5L-HNPC topology without compromising on the power quality. A novel SVM technique based on improved

space vector structure has been proposed to reduce device switching frequency [34]. The space vector structure consists of two concentric 12-sided polygons, which is divided into smaller sized isosceles triangles. PWM switching on these smaller triangles reduces the device switching frequency without compromising on the power quality. This method has been demonstrated on dual 3L-NPC inverter fed open-end induction motor drive with $f_{s,avg}$ equal to $14f_{1R}$.

1.2.1.2 Predictive Control

Predictive control techniques were originally developed for process industries in 1970s [35]. It was introduced for control of 2L inverter based on predicting optimal switching vector in 1980s [36]. Predictive control technique uses system model to predict the future behavior of the system and then control actions are selected based on an optimization criteria. Key benefits are as follows: easy to understand and intuitive concept, simple handling of multi-variable case and multi-objective problems, easy to include system constraints and nonlinearities, and so on. Also, predictive controllers have fast transient response due to elimination of cascaded control structure, which is typical in a linear controller scheme. However, high amount of computational power required for predictive control collides with requirement of high sampling rates in power electronics applications.

In case of high power applications, predictive control schemes can ensure LDSF operation by including additional terms in cost function, while satisfying the system performance requirements. Some approaches include reduction in commutations by predicting number of switchings involved in using a new switching state or by predicting switching losses due to a new switching state or by selecting switching states such that predefined number of commutations are assured to realize constant switching frequency operation [37–40].

The classification of predictive control techniques is illustrated in Fig. 1.3. Two main categories of predictive control algorithms are developed in the literature. The first method extends traditional field-oriented control by using a predictive-based controller instead of inner current control loop, while keeping the modulator [41]. The second method employs predictive controller to directly manipulate the inverter switch positions without a modulator. The sub-categories of second method are hysteresis-based predictive control [36, 42–44] and trajectory-based predictive control [45]. The goal of hysteresis-based predictive control strategies also known as FMCC, is to keep the control system variables between the boundaries of a hysteresis area. The goal of FMCC with circular boundary (FMCC-C) scheme is to minimize stator current distortion [36], [42], whereas FMCC with rectangular boundary (FMCC-R) scheme aims at controlling the motor’s electromagnetic torque distortion [43]-[44]. In trajectory-based predictive control, the control variables are forced to follow predefined trajectories, for example, direct speed predictive control, where motor speed is directly controlled without any proportional-integral controllers [45].

The most popular approach in predictive control is MPC or receding horizon control technique. In this technique, future behavior of system variables are predicted in discrete-time steps. The number of predictive

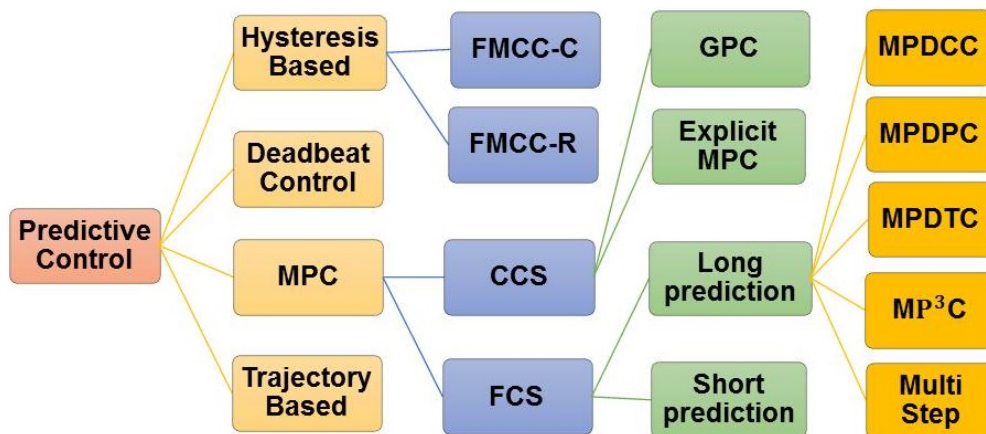


Fig. 1.3: Classification of predictive control techniques

discrete-steps is called prediction step N_p and is usually limited to a few sampling steps. An objective function is defined based on performance requirements and system constraints can be imposed on system variables or control inputs. The optimization problem is solved in real time at each sample step to determine optimal control sequence over prediction horizon. Out of this control sequence, only first input is utilized and entire procedure is repeated at the next sample step, while time horizon is shifted one step forward [46]. Due to receding horizon policy, there is an inherent closed-loop feedback.

Two main categories of MPC technique are: CCS-MPC and FCS-MPC or direct MPC [47]. The CCS-MPC technique requires modulator to generate switching states, whereas FCS-MPC technique can directly generate the switch positions. The main disadvantage of CCS-MPC technique is high computational burden and thus several methods have been proposed in the literature to offset this issue. One such scheme is known as GPC that solves the optimization problem analytically leading to a linear controller [48]. However, it is difficult to include nonlinearities and system constraints. Another scheme tries to move the huge part of calculations off-line by converting optimization problem into multi-parametric quadratic programming [41].

The FCS-MPC technique takes inherent advantage of discrete nature of power converters. The term FCS refers to a fact that power converters have finite number of switching states. Therefore, it is sufficient for MPC algorithm to evaluate optimal condition or cost function for these finite switching states. FCS-MPC technique is classified based on the prediction horizon: short prediction horizon ($N_p=1$) and long prediction horizon ($N_p \geq 2$) [49]. Due to less computational burden and ease of implementation, short prediction horizon MPC or one-step predictive control has been successfully applied in wide variety of power electronics applications. In case

of higher level MLCs, total number of switching sequences increase rapidly that leads to higher computational burden. Therefore, modifications are suggested to existing FCS-MPC technique to evaluate cost function only for a few closest vectors to last applied voltage vector to converter [50].

Long prediction horizon naturally improves the steady-state as well as dynamic performance and also avoids stability issues. However, computational burden increases exponentially with length of prediction horizon due to higher number of possible switching sequences [51]. Therefore, time required to solve underlying optimization problem is often longer than smaller sampling intervals used in power electronics applications, which makes the real time implementation a difficult task. Thus, there is a need to develop new algorithms to reduce the computational burden, while satisfying the performance requirements [52]. One of the proposed methods known as move blocking strategy, reduces the computational burden by dividing the prediction horizon into two parts. The first part of horizon consists of small sampling time, whereas second part consists of longer sampling time. The idea is that high-resolution sampling is required only at present time step to get accurate switching actions. By using coarse sampling at farther points, it is possible to achieve longer prediction horizons with lower computational burden [53].

The most popular approach to reduce the computational burden for longer prediction horizons is based on principle of extrapolation [54]. It realizes long prediction horizons by defining two horizons: switching horizon N_s and prediction horizon N_p . Usually hysteresis bounds on the controlled variables are required in the extrapolation strategies. In the predefined switching horizon period, the trajectories of controlled variables are created for all possible control sequences and the best possible trajectories are selected. Next, the best possible trajectories are extrapolated by maintaining switching states constant in the prediction horizon. The prediction

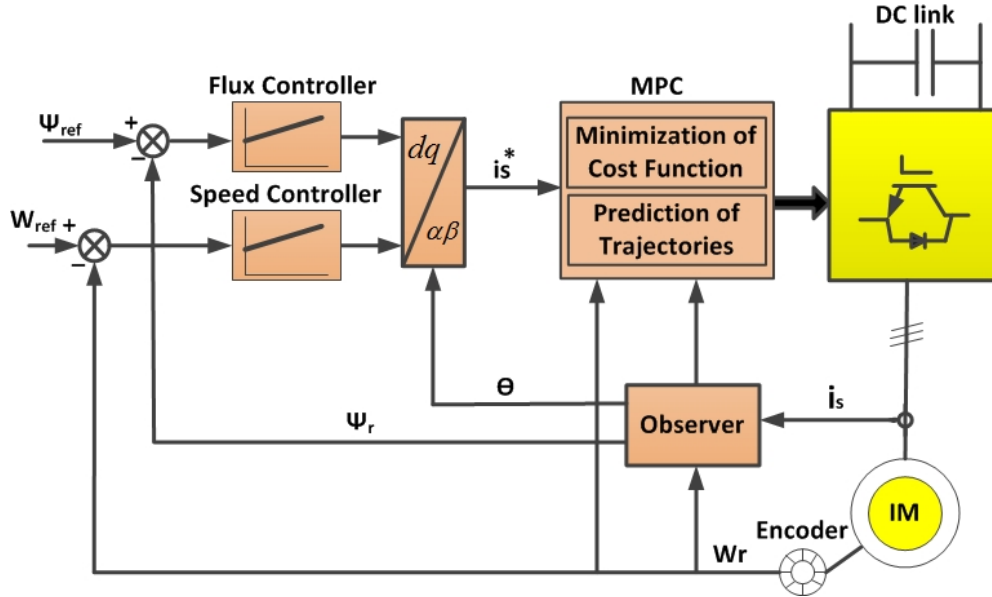


Fig. 1.4: MPDCC control scheme

horizon starts from the last step of switching horizon and is of variable length. The length of prediction horizon is the time step when first controlled variable hits the hysteresis bounds. It should be highlighted that even longer prediction horizons can be achieved by combining switching and extrapolation segments [52]. The techniques such as MPDTC, MPDCC, and MPDPC are developed based on these extrapolation strategies and are implemented with prediction horizons up to 100 steps. MPDTC is an extension of DTC method, obtained by replacing the lookup table of DTC with an online-optimization method for the control of machine torque and flux [55]. MPDCC is another variant of MPC algorithm in which machine stator currents are kept within hysteresis bound around their references [56]. The control diagram for MPDCC scheme is shown in Fig. 1.4. MPDPC is an extension of direct power control (DPC) where look-up operation is replaced by an on-line optimization algorithm [57]. All these techniques include penalty in cost function to minimize device switching frequency.

Another trend to reduce the computational burden of MPC techniques is development of new algorithms for efficient solving of underlying op-

timization problem [58]. Recently, ‘*branch and bound*’ method has been proposed to reduce the number of switching sequences to be explored and it has been shown that computational burden is reduced by an order of magnitude [59]. Also, computationally efficient multi-step FCS-MPC technique has been proposed by adapting sphere decoding principles to solve the optimization problem [60].

The most promising approach for reducing the computational burden is development of hybrid LDSF modulation techniques. One such control strategy is a combination of OPPs and MPC known as MP³C [61]. The basic idea is that optimal stator flux trajectory is derived from OPPs and then, MPC is made responsible to track this trajectory in real time. MPC algorithm utilizes optimal switching patterns as baseline and then does re-optimization to remove the flux error over the pre-defined horizon. This greatly alleviates the computational burden because deriving transient switching patterns from optimal switching patterns is less computationally demanding than computing an entirely new pulse pattern from scratch. A comparison between classical and MPC techniques is reported in [62]-[63].

1.2.1.3 SHE-PWM

The basic foundation for SHE-PWM was laid in early 1960s. It was proposed to eliminate two lower order harmonics by introducing additional switching angles in the square wave voltage waveform [64]. Switching angles were obtained by solving Fourier series expressions of harmonic components and the fundamental frequency component of load voltage was controlled by introducing phase-shift between inverter phase legs. Based on this idea, generalized methods were developed to eliminate a predefined number of lower order harmonic components and maintain desired value of fundamental component, for a given number of switching angles [65].

SHE-PWM technique has been successfully extended to MLC topologies [66–75]. The sequential steps in multilevel SHE-PWM are: selection of waveform symmetry, identification of all possible multilevel waveforms for a given number of switching angles, and calculate switching angles that satisfy the given requirements, and assigning switching angles to each semiconductor device that depends on the converter topology. For multilevel waveforms, quarter-wave and half-wave symmetries are usually introduced [66]–[67]. On the other hand, non-symmetrical waveform selection leads to increased complexity as well as computation burden and thus seldom used [68]. The next step is to identify all the possible multilevel waveforms for a given number of switching angles. It should be noted that there exists only single waveform (bipolar or unipolar) in case of classical 2L converters, whereas several waveforms exist for multilevel converters. The concept of low level envelope has been developed for multilevel converters to come up with single equation formulation to determine switching angles [69].

The switching angles are obtained by solving nonlinear transcendental equations to eliminate a particular number of lower order harmonics and obtain desired reference value for fundamental component. Some of the solving algorithms include numerical iterative techniques like Newton-Raphson [67], Walsh function approach [70], theory of resultants [71], optimization based techniques such as modern stochastic search, genetic algorithms, differential evolution, particle swarm optimization, and bee algorithm [72–75]. All the previous methods require off-line computation.

Several attempts have been made to obtain the switching angles in real time. The main issue with online implementation is increased complexity and higher computational burden to solve system of equations. One proposed method is to train artificial neural networks with complete and detailed knowledge of switching angle solutions and then utilize the same for obtaining switching angles in real time for a given modulation index [76].

In addition, MPC based SHE-PWM technique has been suggested to eliminate lower order harmonics in real time [77]. This proposed method utilizes sliding discrete Fourier transform to obtain amplitudes of harmonic components in real time and then uses predictive model to determine switching states that eliminate desired harmonics. This modulation method allows closed-loop operation with high dynamic performance. The main disadvantage is higher computational burden at higher number of voltage levels.

The final and important step in SHE-PWM technique is to assign switching angles to each semiconductor device that depends on the topology. For CHB multilevel topologies, switching angles are assigned based on device loss equalization and dc-link capacitor voltage balancing, which can be obtained easily based on level-shifted carriers or phase-shifted carriers [78]-[79]. For NPC and FC multilevel topologies, criteria for assigning switching angles is based on capacitor voltage balancing [80]-[81]. For MMCs, assignment of switching angles depends on the submodule capacitor voltage balancing [82].

The main advantage of SHE-PWM technique is that elimination of lower order harmonics is achieved with a few commutations in a fundamental cycle. Hence, switching losses as well as filters' size is significantly reduced in high power applications. Due to reduced switching losses, it possible to achieve better converter efficiency and enable air cooling. Consequently, SHE-PWM technique has become one of the popular LDSF modulation technique for high power applications and it has been commercialized by a group of industries [3]. This technique has been demonstrated for several applications such as motor drives, AFE rectifiers, grid connected converters such as STATCOM, solar power integration and so on [71, 83–86].

The main demerit of SHE-PWM technique is assumption of steady-state operating conditions during solving a set of equations. Therefore, lower order harmonics may not be completely eliminated during actual system

operation. In addition, closed-loop performance degrades when combined with closed-loop controller and so, most of the applications of SHE-PWM technique are limited to low performance drives such as pumps, fans, compressors, etc. Nevertheless, attempts are being made to improve the closed-loop performance by combining SHE-PWM with MPC technique [77]. In addition, it should be noted that energy present in the eliminated harmonics is distributed over the non-eliminated harmonics and hence their amplitudes tend to increase [5]. Therefore, elimination of lower order harmonics never leads to the best system performance. Thus, optimal PWM methods have been developed to minimize the overall effects of harmonics [87].

1.2.1.4 Staircase or Step Modulation

SHE-PWM technique for CHB multilevel topologies is also known as staircase or step modulation due to staircase shape of output voltage waveform. The main difference is that each angle is associated with a particular cell. The basic principle is to connect each cell of the multilevel inverter at predefined switching angles to generate the output waveform with a minimum possible commutations and then, SHE methods are used for off-line determination of switching angles to eliminate lower order harmonics [88]. Later, a simple method has been proposed to obtain the switching angles in real-time by making use of the voltage-second areas of the divided reference voltage corresponding to the MLC output voltage levels [89]. However, this technique neither leads to minimization of output voltage THD nor elimination of lower order harmonic components of output voltage. Subsequently, a real-time algorithm for staircase modulation was proposed to minimize THD of MLC output voltages with a fixed voltage source [90] as well as unequal or varying dc sources (batteries, photovoltaic arrays etc.) [91].

1.2.1.5 Optimal PWM

Optimal PWM techniques have been developed based on the observation that minimization of overall harmonics is better than complete elimination of certain lower order harmonics in order to achieve the best system performance [92]. Other benefits are easier convergence and increased continuity in the solution space. Optimization technique determines switching patterns based on minimizing a cost function or performance index. The classification of optimal PWM methods based on performance index is shown in Fig. 1.5. The goal of harmonic minimization technique is to obtain local minima of lower-order harmonic rather than their complete elimination, while maintaining the required fundamental frequency component [93]. The main advantage is feasibility of real time implementation due to faster convergence to local minima [94].

The most popular approach in optimal PWM is THD minimization [95–99]. In this regard, number of harmonics in the problem formulation are typically more than the number of available switching angles. In case of SHM technique, switching patterns are determined such that harmonic contents satisfy the grid code limits [100]. Another optimal PWM method has been reported considering duration of switching sub-cycles as variables, where sub-cycle is defined as time sequence of three consecutive switching state vectors [101]. This method demonstrates good dynamic response but solutions obtained are suboptimal due to restriction on sub-cycles. Other approaches are minimizing crest factor of output current waveform [102], minimizing motor harmonic losses [103], minimization of torque and speed

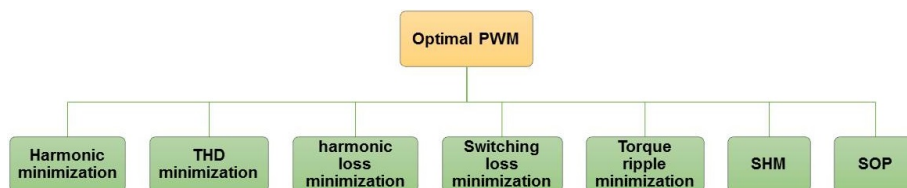


Fig. 1.5: Classification of optimal PWM techniques

ripples [104]-[105], minimizing switching loss [106] and elimination of particular resonant frequencies [107]. The main idea behind each performance criteria is to minimize the unwanted effects of harmonics catering to needs of particular application. In general, lower order harmonics need to be suppressed more than higher order harmonics, which is possible by using weighted THD function, i.e., divide magnitude of each harmonic by its harmonic order. The standard approaches to solve off-line optimization problem include gradient-based algorithms, artificial neural networks [108], genetic algorithms [109], and particle swarm optimization [110].

The most successful optimal PWM technique, which has been recently introduced in commercial MV drives is SOP [111]-[112]. This method is also referred to as SOPWM or optimized pulse patterns (OPP) in other literature. It is a combination of synchronous PWM and optimal PWM. Synchronous PWM is generally utilized in LDSF applications, where frequency of carrier signal f_c is always made an integer multiple of f_1 . This helps eliminate inter-harmonic components. Synchronous PWM results in a fewer number of switching instants in a fundamental period and thus minor variation in these switching angle values has significant influence on the harmonic distortion of output waveforms [113]. Therefore, optimization methods are suggested for off-line determination of switching angles with goal to minimize the harmonic distortion of output waveforms.

SOP technique has been demonstrated for classical 3L and 5L MLC topologies with $f_{s,max}$ set at 400 Hz and 200 Hz, respectively [114–116]. In addition, SOP along with NPP balancing algorithm has been demonstrated for 5L-HNPC inverter [117]. Also, SOP technique has been implemented for dual inverter based MLC topologies feeding open-end winding induction motor drives [118]. Recently, it has been demonstrated for 23-MW large salient pole synchronous motor drive while taking into account the anisotropic magnetic properties of the synchronous motor [119].

The optimal switching patterns are suitable only for low performance MV drives such as industrial fans, centrifugal pumps, blowers, etc., which operate in open-loop v/f control mode. For such drives, the stator voltage is adjusted in proportion to the fundamental frequency. High-performance drives require fast responses to change in speed and torque. During such transients, a different pulse pattern that has switching transitions at different time instances is instantaneously selected. However, the complex volt-second input to the machine does not satisfy the optimality conditions, which will lead to high transient currents in the drive [120].

To maintain optimal control during transient conditions, SOP technique should be combined with trajectory tracking control. Two types of trajectory tracking methods have been proposed in the literature. In the first method, optimal pulse patterns are used to compute optimal current trajectories and then trajectory controller forces the actual current vector

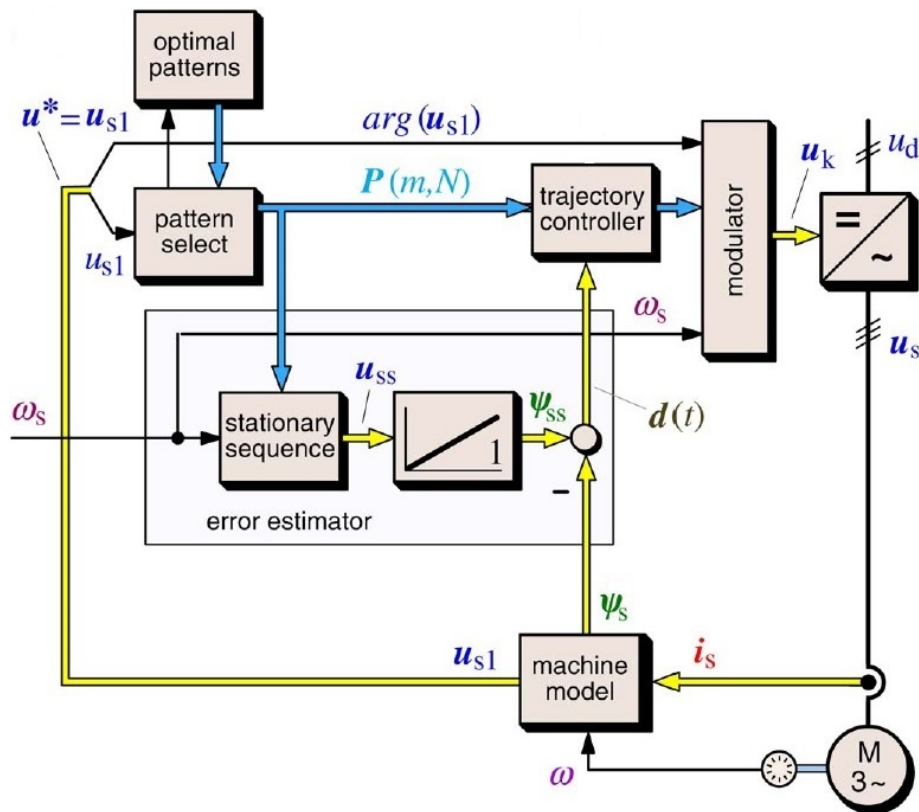


Fig. 1.6: Signal flow diagram of stator flux trajectory control system [1]

to follow the optimal current trajectory [121–123]. However, the stator trajectory current depends on leakage inductance of machine which is load dependent and thus fast online estimation of system parameters is required. In second method, optimal stator flux vector tracking has been proposed, which is independent of machine parameters or load conditions [124].

The signal flow graph of stator flux trajectory control is shown in Fig. 1.6. Based on the voltage reference u^* from the constant v/f characteristic, optimal pulse pattern $P(m,N)$ is selected and its steady-state voltage waveform u_{ss} is integrated to yield the optimal optimal steady-state flux trajectory ψ_{ss} . It serves as reference trajectory onto which estimated stator flux trajectory ψ_s is forced. Now, let us assume that transient condition occurs at time t . Then, a new optimal pulse pattern will be selected, which will have a different flux trajectory ψ_{ss1} . This leads to instantaneous difference in the flux vector known as dynamic modulation error $d(t) = \psi_{ss1}(t) - \psi_s(t)$. This error $d(t)$ is given as input to trajectory controller as shown in Fig. 1.6. The trajectory controller then modifies the actual optimal pulse

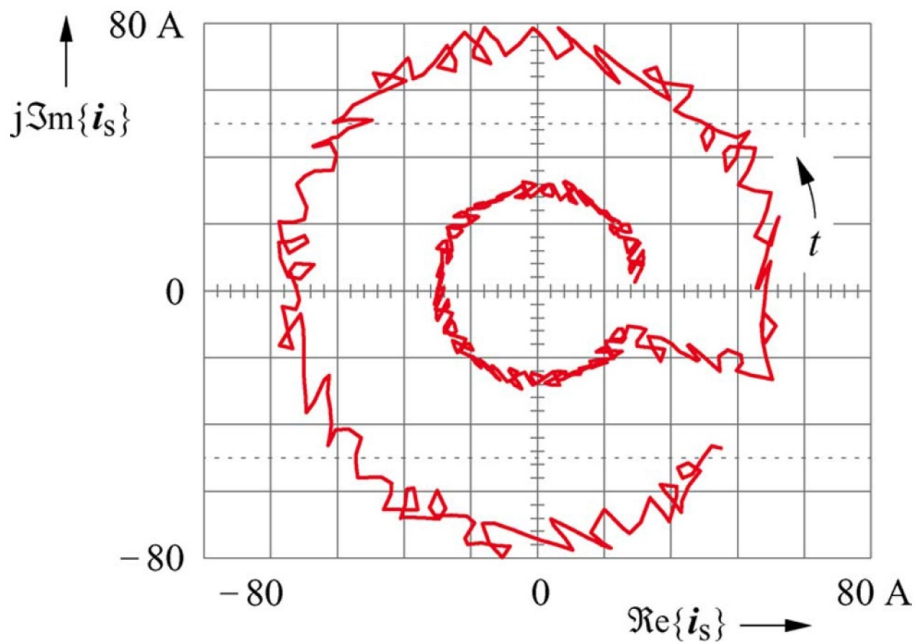


Fig. 1.7: Trajectory of the stator current vector with a step transition from no-load operation to nominal load [1]

pattern $P(m,N)$ by displacing the switching instants so as to minimize the error $d(t)$. More details about operation of trajectory controller can be seen in [124–127]. The performance of trajectory controller is shown in Fig. 1.7 for a step change from no-load operation to nominal load. It demonstrates the dead-beat behavior of trajectory controller. Recently, a new method MP³C has been proposed that replaces trajectory controller with MPC controller [61],[128].

1.2.1.6 Other Modulation Techniques

In literature, several other modulation techniques have been proposed to achieve LDSF operation without compromising on power quality. SVC or NVC technique has been proposed as alternative to SHE-PWM to avoid off-line computations and provide high dynamic performance [129]. The basic idea is to approximate reference vector to closest vector in the $\alpha - \beta$ plane without a modulator. Due to natural selection of the closest vector without any modulator, there will be higher reduction in the number of switching commutations. However, the best performance of SVC can be attained only for higher level MLCs due to higher and dense space vectors available. Otherwise, approximation errors will be large, which lead to variable magnitude error for the fundamental component as well as introduction of lower order harmonics. SVC has been demonstrated for a 11L CHB inverter with $f_{s,avg}$ limited to $1.4 * f_{1R}$ [129]. NLC is a time-domain counter part of SVC, where the nearest voltage level instead of a space vector is selected to obtain desired output voltage reference [130]. The major advantage is in terms of lesser implementation complexity, since it is easier to find the closest voltage level instead of the closest space vector.

Also, an adaptive duty-cycle modulation algorithm has been proposed by utilizing the slope of voltage reference to adapt the modulation period. This technique has been demonstrated for 9L asymmetric CHB inverter

with $f_{s,avg}$ ranging from 250 to 400 Hz [131]. A simple and novel SLOpe PWM technique with a trapezoidal modulator and a sinusoidal carrier signal has been proposed with device switching frequency equal to $11*f_1$ [132].

1.2.2 Emerging MLC topologies

One major focus while developing new multilevel topologies is to generate any number of levels in output voltage with single dc source. This obviously requires floating capacitors to generate intermediate voltage levels. The 5L and 9L ANPC topologies, which utilize single DC source are shown in Fig. 1.8. The floating capacitors need to be maintained at particular voltage level in order to generate required number of voltage levels as well as to reduce the harmonic distortion of output voltage. Due to availability of redundant switching states, it is always possible to keep the floating capacitor voltages within predefined limits by using higher device switching frequency operation [133]. On the other hand, LDSF operation leads to higher capacitor voltage ripple due to availability of a few switching commutations in a fundamental cycle. In this regard, MPC techniques are effective due to their flexibility in handling multi-objective problems [134].

Another emerging topology, which had gained lot of commercial interest is MMC. The MMC topology is shown in Fig. 1.9. MMC has been orig-

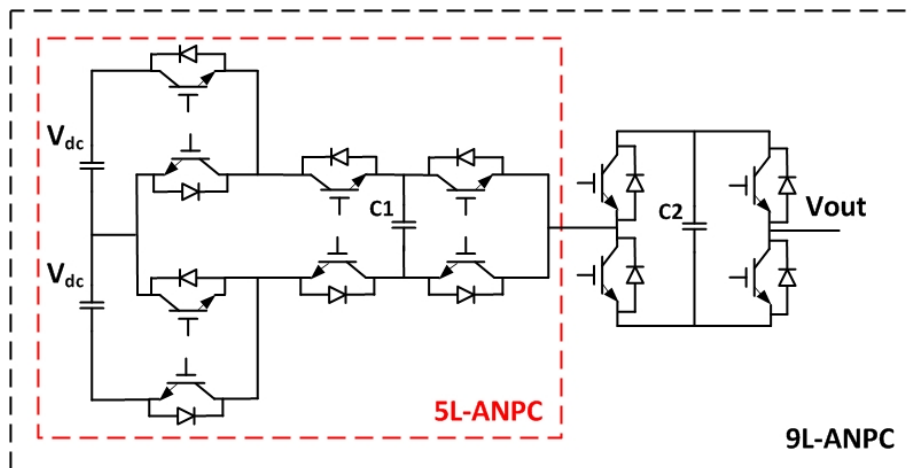


Fig. 1.8: ANPC topology for 5L and 9L operation

inally proposed for HVDC transmission systems [25, 135, 136]. Recently, MMC has been commercially introduced for MV drives both as an AFE rectifier and also as an inverter [137]. The main advantages are its modular design, easy scalability to reach any voltage and power levels, low expense for redundancy, and better output power quality due to the large number of voltage levels [138]. The first commercialized project of MMC used 200 sub-modules (SM) per phase reaching up to 400 MW [136]. At such a high number of voltage levels, it is easy to reduce the device switching frequency while maintaining the output power quality. On the other hand, MMCs in other applications such as MV drives consist only a few number of SMs per phase [139] and hence, there is a need for the development of LDSF modulation techniques suitable for MMC.

The objectives of MMC control are ac-side current tracking, minimization/elimination of circulating currents, submodule capacitor voltage balancing and LDSF operation. Among LDSF modulation techniques, SHE-PWM, NLC and predictive control techniques have been implemented for MMCs. A new modulation method allowing fundamental switching frequency utilizing the principles of SHE-PWM has been proposed [140]. It has been observed that reduced device switching frequency comes at the

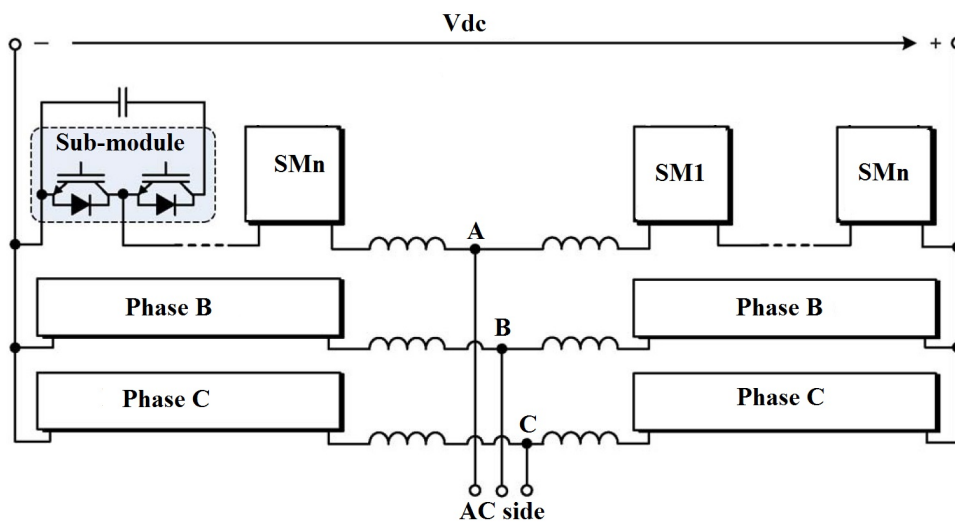


Fig. 1.9: MMC topology

cost of increased voltage ripple. This method does not have any control over circulating currents and thus, leads to increase in resistive losses and capacitor voltage ripple. Later, this method has been enhanced by introducing small deviations in the pulse patterns to eliminate dominating second order harmonic component in the circulating current [141]. On the other hand, NLC technique is more useful for MMC with higher number of voltage levels due to simpler implementation and low computational effort [142]. Also, OPP technique has been implemented for MMC topology at fundamental switching frequency [143].

The most promising LDSF modulation technique for MMC is MPC. The first implementation of FCS-MPC technique for MMC has been done with one-step prediction of ac-side currents, circulating currents and sub-module capacitor voltages [144]. However, minimization of switching losses has not been accounted in the cost function. Later, PWM-based MPC technique has been reported for MMC to achieve constant switching frequency and low device switching frequency [145]. Also, MPDCC technique with long prediction horizon has been implemented for MMC to track ac-side currents within hysteresis bounds, while minimizing circulating currents, SM capacitor voltage fluctuations and device switching frequency [146]. The main drawback of the above methods is that cost function is evaluated for all possible switching sequences and thus computational burden increases exponentially with increase in number of voltage levels. Therefore, real-time implementation of MPC technique becomes a challenging task. The same has been concluded from comparison study done between classical and MPC techniques in [147].

A novel MPC technique with three independent predictive controllers is proposed for the ac-side currents, circulating currents, and submodule capacitor voltage balancing [148]. Three different cost functions are defined to select the best switching states. The main advantage of this method is

reduction of computational burden. However, it does not provide flexibility to maintain trade-off among ac-side current tracking error, minimizing circulating current and capacitor voltage ripple. Later, indirect FCS-MPC method has been proposed with a cost function to select the best number of inserted submodules in each arm to minimize the ac-side current tracking error, circulating currents and sub-module capacitor voltage fluctuations [149]. By using modified switching strategy, device switching frequency has been reduced to 174 Hz for a 20L MMC and the total number of control actions are reduced to $(n+1)^2$ for an $n+1$ level MMC, which is quite significant reduction compared to C_n^{2n} in [144].

Another topology that had gained lot of interest from researchers is dual inverter based MLC topology, which is shown in Fig. 1.10. This topology has been introduced for open-end stator winding induction motor drives. The first proposed topology consists of dual 2L inverters feeding both ends of stator winding and generates 3L voltage waveforms across stator winding [150]. Later, MLC topology to generate 5L voltage waveforms across stator windings has been proposed by utilizing dual 3L-NPC inverter configuration [151]. It should be highlighted that both of the above topologies operates from a single dc source. Subsequently, several other MLC topologies to generate 5L to 9L voltage waveforms across stator winding have been proposed [152–157].

The major advantage of dual-inverter based MLC topologies over other

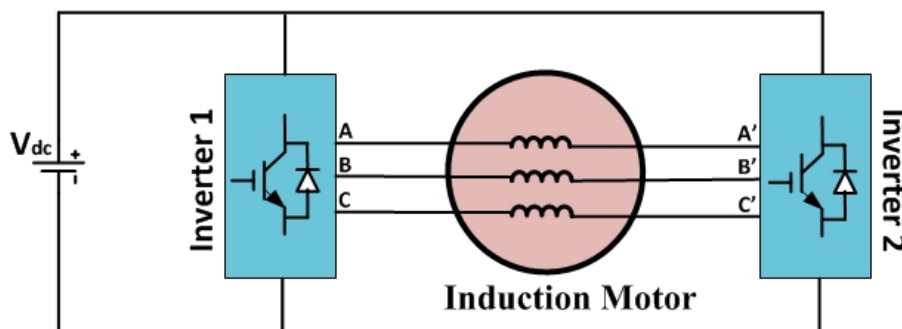


Fig. 1.10: Dual inverter based MLC topology for open-end stator winding induction motor drive

topologies is minimal requirement of dc sources, which becomes obvious when number of voltage levels becomes more than three. For example, a 5L dual inverter topology requires a single dc source, whereas NPC and CHB based 5L topologies requires three and six isolated dc sources, respectively. Similarly, a 9L dual-inverter topology requires two dc sources [157], whereas NPC and CHB based 9L topologies require six and twelve isolated dc sources, respectively. In general, isolated dc sources are obtained from phase-shifting multi-winding transformers, which are bulky and expensive, compared to standard transformers required for dual-inverter topologies. However, these benefits of dual-inverter based MLC topology come at the expense of additional cabling requirements for open-end stator winding induction motor drives.

Another important advantage of dual-inverter based MLC topologies is availability of higher redundant switching state combinations compared to single-inverter based MLCs with the same number of output voltage levels. For example, D2L inverter has 64 space vector combinations, whereas 3L-NPC inverter has 27 space vector combinations to generate 19 space vector locations [158]. By utilizing these redundant space vectors, it is possible to achieve floating capacitor voltages balance, elimination of common-mode voltages and so on. One more advantage of dual-inverter based MLC topologies is that the voltage amplitude required to produce air-gap flux in the machine is divided among the two inverters. Therefore, the device ratings as well as $\frac{dv}{dt}$ stress are reduced, which is very important for high-power applications.

The main disadvantage of dual-inverter topologies is requirement of common-mode inductor in series with machine stator windings to suppress the zero-sequence or common-mode current components. Initially, several SVM based control strategies have been reported to eliminate zero-sequence currents in the windings as well as to eliminate the common-mode voltages

which lead to bearing and leakage currents [155–160]. However, all these methods utilize high device switching frequency and hence will not be preferred for MV high-power applications. Recently, SOP technique has been implemented successfully [161] and it has been enhanced to minimize the zero sequence currents in machine windings for dual 3L inverter topology [162], while limiting the maximum device switching frequencies to 200 Hz. Using first SOP technique, the requirement of common-mode inductor still remains and thus there is a need to further enhance SOP technique.

1.3 Performance comparison of LDSF modulation techniques

The performance comparison between SPWM, SVM, SOP, and predictive control techniques is conducted in [62],[63] and the results are depicted in Fig. 1.11. It should be observed that SOP and MPC technique with long prediction horizons such as MPDCC $e(SE)^3$ or MPDTC $e(SE)^3$ have better steady-state performance at LDSF operation ($f_s < 300$ Hz). The main rea-

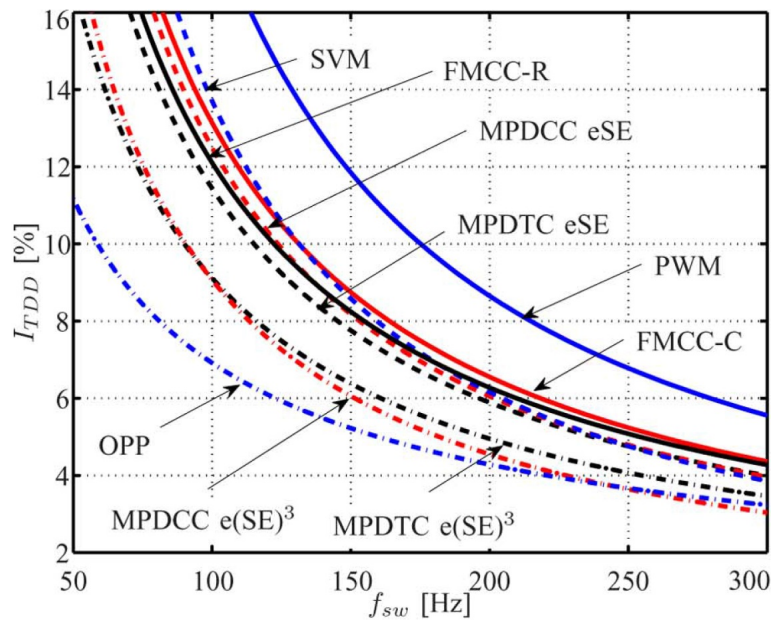


Fig. 1.11: Performance comparison between SPWM, SVM, MPC and SOP techniques : current TDD versus f_s (Note: SOP is referred as OPP in the figure). (Courtesy of J. Scoltock, T. Geyer, and U. Madawala)

son is that both SOP and MPC techniques generate switching states based on an optimization criteria. SOP depends on off-line computations and thus, it is always possible to obtain global best optimal switching states for the given performance requirements. On the other hand, MPC technique is based on online optimization that leads to higher computational burden. This is especially applicable in power electronics applications where sampling intervals are of the order of few microseconds. Researchers from academia and industry are working towards more sophisticated algorithms to overcome the computational issues of MPC technique [60]. It should be pointed out that optimal switching states obtained from MPC may not be the global best and thus it will not be able to deliver better performance than SOP technique.

Moreover, it should be observed that SOP outperforms all other modulation techniques if $f_{s,max}$ is set at 200 Hz. MPC technique with longer prediction horizons might improve the performance but at the cost of higher computational burden. Also, computational burden of MPC techniques rapidly increases at higher number of voltage levels. Therefore, it should be concluded that SOP technique is more appropriate for MLCs with higher number of voltage levels and also, it can reduce device switching frequency upto f_{1R} depending on the number of voltage levels.

Table 1.1: Specifications of commercialized higher level MLCs

Manufacturer	Voltage (kV)	Power	Levels
Siemens	2.3-13.8	120 MVA	9/13
TMEIC-GE	3.3/6.6	15 MVA	7/13
ArrowSpeed	2.3/4.16/6/11	5.6 MVA	11
RongXin	3/6/10	10 MVA	7/11/13/19
LS Ind. Sys.	3/4/6/10	11.1 MVA	13
Yaskawa	3.3/6.6	6 MVA	7/13
Beijing Leader and Harvest	3/3.3/4.16 6/6.6/10	6.25 MVA	9/11/15/17

1.4 Research Problem and Objectives

The control requirements of MV drives are : low device switching frequency operation, better quality of converter output currents, and fast dynamic performance. As explained in Section 1.3, SOP has superior performance over all other modulation techniques at LDSF operation. Until now, SOP has been demonstrated for classical 3L to 5L MLC topologies and closed-loop techniques in combination with stator flux trajectory control or MPC have been developed.

On the other hand, the present trend in MV high power drives is to use MLCs with higher number of voltage levels to achieve better quality output voltage waveforms. Table 1.1 shows some of the commercial products, which are using MLCs with seven levels and above [3]. It should be noted that manufacturers are preferring to go for higher-level topologies to achieve better quality waveforms, even though 3L-MLC topologies are sufficient to meet the power demand. Also, several new topologies have been proposed in the literature as an alternative to classical MLC topologies and some of them found industrial relevance as well. Therefore, there is a need to analyze and propose modifications to the state-of-the-art SOP technique in order to modulate MLCs with any number of voltage levels and also emerging MLC topologies.

Apart from this, state-of-the-art SOP technique needs to be enhanced to modulate dual inverter based MLC topologies such that common-mode currents are eliminated in the open-end stator windings of induction motor. Also, it has been identified that dual inverter based MLC topologies to generate seven or higher voltage levels in the stator winding voltages utilize more than one dc source. Therefore, there is a need to propose a new dual inverter based MLC topology that can be operated from a single dc source and generates any number of voltage levels. All these requirements are the main motivation behind the thesis.

The research objectives of the thesis are as follows:

1. Develop systematic analysis to implement state-of-the-art SOP technique for MLCs with any number of voltage levels.
2. Propose modified SOP technique for MMC topology.
3. Propose enhanced SOP technique for dual inverter based topologies to eliminate common-mode currents in machine stator windings.
4. Propose new dual inverter based topology that can be operated from a single dc source and generates any number of voltage levels.

1.5 Thesis Contributions

The major research contributions of the thesis are as follows:

1. SOP technique has been analyzed and categorized into three steps: estimation of pulse number N , optimization of switching angles, and allocation of optimal switching angles to each power semiconductor device. It has been identified that first and last steps in SOP technique are dependent on the converter topology, whereas second step in SOP technique is independent of converter topology. Based on the developed analysis, state-of-the-art generalized SOP technique along with angle swapping scheme has been employed to modulate cascaded 7L and 9L MLCs with $f_{s,avg}$ equal to f_{1R} .
2. Proposed modified SOP technique for modulating MLCs with five or higher levels to achieve the following objectives : identical device switching frequency, and limit the peak device switching frequency to desired $f_{s,max}$. The performance of the proposed technique is similar to that of state-of-the-art SOP technique but with further reduced device switching frequency. In addition, proposed technique maintains the same pulse number in the higher modulation index range

that avoids transients in machine currents. The proposed technique has been used to modulate cascaded 7L and 9L MLCs with $f_{s,max}$ set at f_{1R} .

3. Proposed enhanced SOP technique for MMC, which involves modifications in method to estimate pulse number N , and allocation of switching angles to each power semiconductor device. The identified criteria for allocating optimal switching angles are identical device switching frequency and balanced capacitor voltages. An angle swapping scheme has been proposed to balance capacitor voltages.
4. Proposed enhanced SOP technique for dual inverter based topologies to eliminate common-mode currents in machine stator windings. The basic idea for elimination of common-mode currents in stator windings is to utilize switching patterns that are 120° phase apart for the inverter phase legs feeding respective stator winding.
5. Proposed a new dual nL -MMC topology that can be operated from a single dc source and generates any number of voltage levels.

1.6 Thesis Outline

The contents of the thesis are organized as follows:

1. In Chapter 2, state-of-the-art SOP technique is systematically analyzed. The developed analysis is utilized to modulate cascaded 7L and 9L MLCs with $f_{s,avg}$ set at f_{1R} . The experimental results are demonstrated to validate the analysis.
2. In Chapter 3, modified SOP technique is presented for MLCs with five or higher levels to achieve following objectives : identical device switching frequency, limit the peak device switching frequency

to desired $f_{s,max}$. The proposed technique is demonstrated using low power prototypes of cascaded 7L and 9L MLCs.

3. In Chapter 4, details of modified SOP technique for MMC topology are presented. Experimental results from 5L-MMC topology are illustrated to validate the proposed technique.
4. In Chapter 5, enhanced SOP technique for dual inverter based topologies is presented to eliminate common-mode currents in machine stator windings. In addition, details of proposed dual nL -MMC topology that can be operated from a single dc source is discussed.
5. In Chapter 6, conclusions and summary of thesis are presented along with guidelines for future work.

1.7 Concluding Remarks

This Chapter has presented the requirements and challenges of modulation techniques for MV high power drives. Due to thermal constraints of power semiconductor devices, LDSF modulation techniques with high quality of converter output currents are preferred for MV drives. Based on the literature review of LDSF modulation techniques, it has been concluded that SOP technique has better steady-state and dynamic performance if device switching frequency is limited to 200 Hz. The study of emerging trends in MV drives and state-of-the-art SOP technique has led to following research objectives for this thesis : systematic analysis of SOP technique for modulating MLCs with any number of voltage levels, propose modified SOP technique for MMC topology, enhance state-of-the-art SOP technique to eliminate common-mode currents in the stator windings of induction motor, and propose new dual inverter based MLC topology that can be operated from a single dc source and generate any number of voltage levels.

Chapter 2

Generalized SOP Technique

2.1 Introduction

This Chapter gives the new analysis of generalized SOP technique and its implementation for 7L and 9L MLCs. SOP technique combines synchronous PWM with optimization technique. Synchronous PWM is used in low device switching frequency applications where carrier signal frequency f_c is always made an integer multiple of modulation signal frequency f_m , i.e., $\frac{f_s}{f_m}$ is an integer. This is done so as to eliminate sub-harmonic frequency components, which are undesirable in several applications. Synchronous PWM results in a fewer number of switching instants in one fundamental cycle and thus a little variation in the switching angle values will have considerable influence on the harmonic distortion of output voltage and current waveforms [113]. Therefore, optimization methods are suggested to predetermine the switching angles off-line for each steady-state operating point to achieve excellent quality of output waveforms [95]. These optimal switching angles are stored as look-up tables in controller memory and retrieved during real-time operation as demanded by outer-loop controller.

This Chapter is organized as follows: Basics of SOP are given in Section 2.2, method to estimate number of switching angles for each modulation index is discussed in Section 2.3, mathematical details about optimization

of switching angles are given in Section 2.4, procedure to allocate optimal switching angles to each power semiconductor device is discussed in Section 2.5, circuit topology and operation of 7L and 9L MLCs along with experimental results obtained with SOP technique are demonstrated in Sections 2.6 and 2.7, respectively. The Chapter is concluded in Section 2.8.

2.2 Basics of SOP

SOP technique has been implemented for v/f control of variable speed induction motor drives. In variable speed drives, the fundamental frequency f_1 varies from zero to f_{1R} . The typical value of f_{1R} is 50/60 Hz, however, it might go up to a few hundred Hertz in some high-speed applications. Therefore, the standard practice in SOP is to utilize normalized fundamental frequency $\frac{f_1}{f_{1R}}$, which is defined as modulation index m . The value of m varies from 0 to 1 and it is usually divided into small intervals to obtain the discrete values for m . SOP technique determines optimal switching angles for all possible discrete values of m .

A typical nL waveform is shown in Fig. 2.1, where V_{step} denotes the difference between two consecutive voltage levels and the value of V_{peak} should be equal to $0.5*(n-1)*V_{step}$. In general, half-wave and quarter-wave symmetries are introduced in the switching pattern in order to eliminate

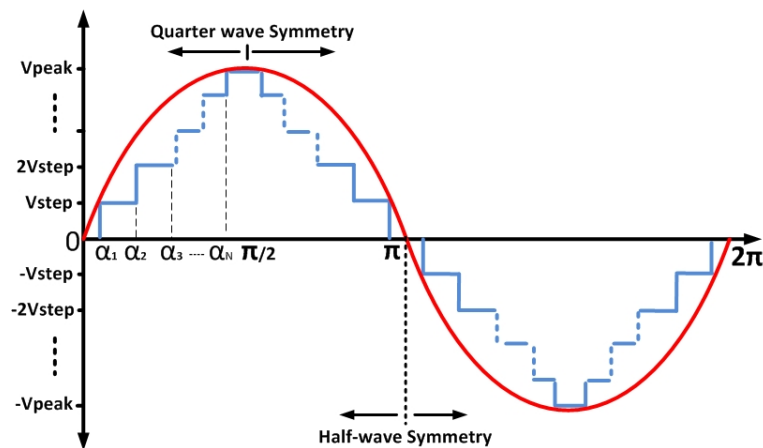


Fig. 2.1: A typical nL phase output voltage waveform

all odd order harmonics and then it is sufficient to determine the switching angles in a quarter fundamental period. The number of switching angles in a quarter period is denoted as pulse number, N . Implementation of SOP technique for each discrete value of m involves three steps :

1. Determine value of N such that $f_s \leq f_{s,max}$.
2. Optimization of switching angles to minimize harmonic distortion of converter output currents for each steady-state operating point (m,N) .
3. Allocation of switching angles to each power semiconductor device.

The first and last steps in SOP technique depends on converter topology, whereas the second step in SOP is independent of converter topology. Complete details about each step in SOP technique are given next.

2.3 Estimation of pulse number, N

The first step in SOP technique is to estimate value of N for each discrete value of m such that $f_s \leq f_{s,max}$, which depends on the converter topology. However, classical MLC topologies such as NPC, FC, CHB, and HNPC share a common feature that an nL -MLC consists of $0.5*(n-1)$ sub-converters such as H-Bridge or 3L-NPC in each phase. Therefore, it is possible to develop generic procedure for classical MLC topologies to estimate N for all possible discrete values of m [114]. On the other hand, some of the emerging MLC topologies such as MMCs require different procedure that will be dealt in Chapter 4.

For a 3L sub-converter operating at (m,N_{3L}) , f_s should be equal to $N_{3L}.m.f_{1R}$. Then, the value of N_{3L} such that $f_s \leq f_{s,max}$ for a particular

value of m is obtained as,

$$N_{3L} = \text{floor} \left(\frac{f_{s,max}}{m \cdot f_{1R}} \right) \quad (2.1)$$

where, $\text{floor}(x)$ denotes the largest integer smaller than x . The value of N for the classical nL -MLC that consists of $0.5 \cdot (n - 1) \cdot 3L$ sub-converters in each phase is obtained as,

$$\begin{aligned} N &= \text{floor} \left(\frac{(n - 1) \cdot N_{3L}}{2} \right) \\ &= \text{floor} \left(\frac{(n - 1) \cdot f_{s,max}}{2 \cdot m \cdot f_{1R}} \right). \end{aligned} \quad (2.2)$$

Due to usage of function $\text{floor}(x)$, each value of pulse number N will have its associated range of m . For example, a 9L inverter operating at $f_{s,max} = f_{1R}$ should have $N=4$ for values of m varying from 0.801 to 1. Also, it should be observed from (2.2) that N increases at lower values of m .

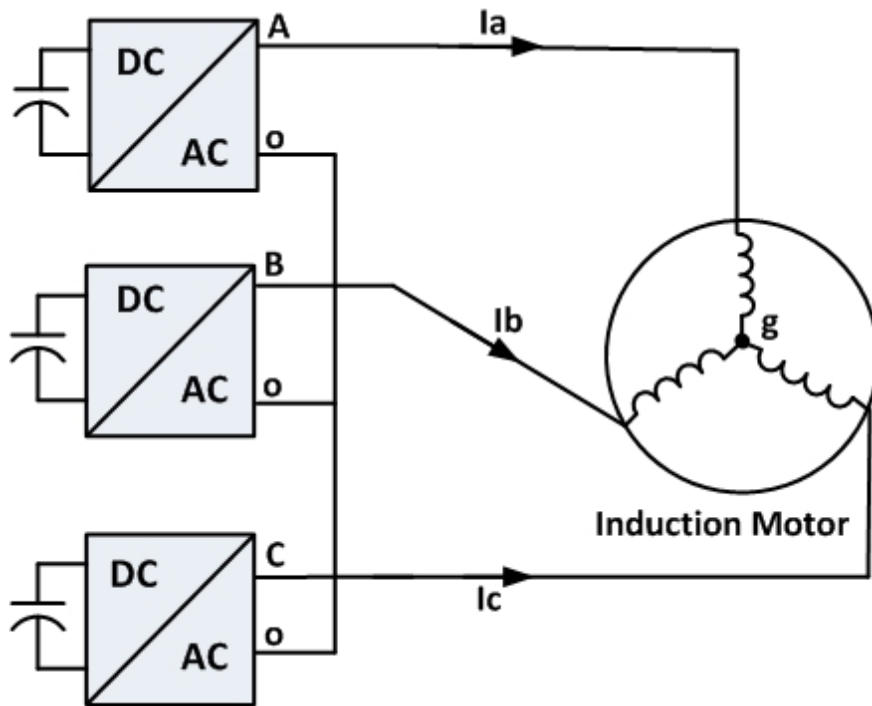


Fig. 2.2: MLC fed induction motor drive system

2.4 Optimization of switching angles

The next step in SOP is to perform optimization to determine switching angles for each steady-state operating point (m, N) . The goal of optimization is to minimize the harmonic distortion of machine stator currents. The preferred objective function is distortion factor d , which is independent of machine parameters. The expression for distortion factor is given by [113],

$$d = \frac{i_h}{i_{h, six-step}}. \quad (2.3)$$

A MLC fed induction motor drive is shown in Fig. 2.2. The phase output voltage of MLC and input phase voltage of induction motor are denoted as v_{jo} and v_{jg} ($j=A, B, C$), where o, g denote the neutral point of MLC and induction motor, respectively. Consider a typical nL phase output voltage waveform as shown in Fig. 2.1 with switching angles as $\alpha_1, \alpha_2, \alpha_3, \dots, \alpha_N$ in a quarter period. Using Fourier analysis, expressions of u_k and $u_{k, six-step}$ are obtained as,

$$u_k = \frac{8V_{peak}}{(n-1)k\pi} \sum_{i=1}^N s(i) \cos(k\alpha_i) \quad (2.4)$$

$$u_{k, six-step} = \frac{4V_{peak}}{k\pi} \quad (2.5)$$

where, term $s(i) = 1$ when the voltage level is switching to a higher potential and $s(i) = -1$ when switching to lower potential, and k corresponds to all odd order harmonics. The waveform v_{go} contains all the triple order harmonics of v_{jo} with amplitude equal to one third of amplitude of v_{jo} . So, phase voltage of induction motor $v_{jp} = v_{jo} - v_{po}$ has all the harmonics of v_{jo} except triple order harmonics [113]. Assuming that stator currents are determined

by leakage inductance, the expressions for i_k and i_h are obtained as,

$$i_k = \frac{u_k}{\omega_1 l_\sigma k} = \frac{8V_{peak}}{(n-1)\omega_1 k^2 l_\sigma \pi} \left(\sum_{i=1}^N s(i) \cos(k\alpha_i) \right) \quad (2.6)$$

$$i_h = \sqrt{\sum_k i_k^2} = \frac{1}{\omega_1 l_\sigma} \sqrt{\sum_k \left(\frac{u_k}{k} \right)^2} \quad (2.7)$$

where, k corresponds to all odd order harmonics except triple order harmonics ($k=5,7,11,13\dots$). The expression for $i_{h,six-step}$ is obtained as,

$$i_{h,six-step} = \sqrt{\sum_k i_{k,six-step}^2} = \frac{1}{\omega_1 l_\sigma} \sqrt{\sum_k \left(\frac{u_{k,six-step}}{k} \right)^2}. \quad (2.8)$$

After simplifying (2.7)-(2.8), the final expression for d is obtained as,

$$d = \frac{2\sqrt{\sum_k \left(\frac{1}{k^4} \right) \left(\sum_{i=1}^N s(i) \cos(k\alpha_i) \right)^2}}{(n-1)\sqrt{\sum_k \left(\frac{1}{k^4} \right)}}. \quad (2.9)$$

It should be observed from (2.9) that d depends on the two variables: $s(i)$ and α_i ($i=1,2\dots N$). To simplify optimization, all the possible set of $s(i)$ that lead to nL waveform known as structures should be determined in advance. Next, optimal switching angles for each structure are determined and then the structure that exhibits minimum d is selected. More details about multilevel structures are given next. In addition, constraint on the switching angles to maintain current modulation index value for constant v/f control of induction motor is obtained as,

$$\frac{f_1}{f_{1R}} = \frac{u_1}{u_{1,six-step}} = \frac{(n-1).m}{2} = \sum_{i=1}^N s(i) \cos(\alpha_i). \quad (2.10)$$

2.4.1 Multilevel Structures

The output waveform of the MLC can be represented as sequence of voltage levels known as structure. An nL waveform has n discrete voltage levels $-0.5 * (n - 1) * V_{step}, \dots, -V_{step}, 0, V_{step}, \dots, 0.5 * (n - 1) * V_{step}$, which can be represented by logic levels $-0.5 * (n - 1), \dots, -1, 0, 1, \dots, 0.5 * (n - 1)$, respectively. As there are more than two discrete voltage levels in case of MLCs, it is possible to have multiple sequence of voltage levels or structures that depends on the number of voltage levels. Different possible structures for 3L, 5L, 7L and 9L waveforms with $N=5$ are shown in Fig. 2.3. It should be observed that there exists only one possible structure for a 3L waveform, whereas higher number of structures exists for five or higher-level waveforms due to additional degree of freedom in choosing next voltage level. Similarly, the number of structures increases at higher values of N . The number of possible structures for 3L, 5L, 7L and 9L waveforms with N varying from 3 to 15 are shown in Table 2.1.

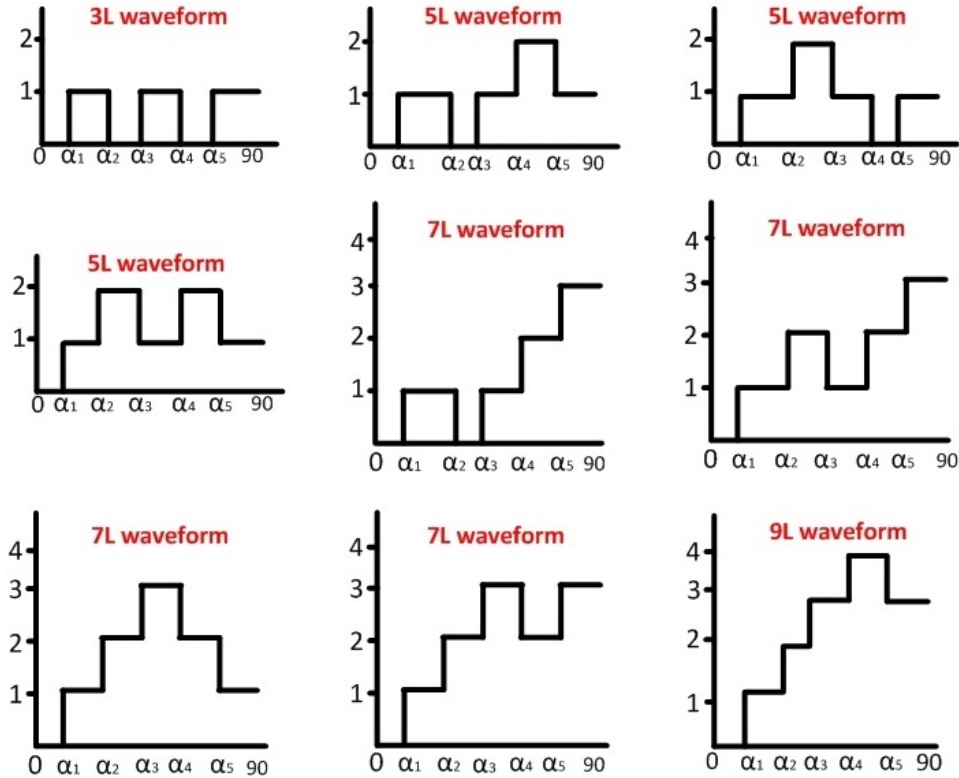


Fig. 2.3: Structures of 3L, 5L, 7L and 9L waveforms with $N = 5$

Table 2.1: Number of structures for 3L, 5L, 7L and 9L waveforms

Output	N												
	3	4	5	6	7	8	9	10	11	12	13	14	15
3L	1	1	1	1	1	1	1	1	1	1	1	1	1
5L	1	3	3	7	7	15	15	31	31	63	63	127	127
7L	1	1	4	5	13	18	39	57	112	169	313	482	859
9L	0	1	1	5	6	20	26	73	99	253	352	848	1200

Table 2.2: Structures of 3L, 5L, 7L and 9L waveforms with $N = 5$

Structure	Voltage levels	$s(i)$
3L	0, 1, 0, 1, 0, 1	1,-1,1,-1,1
5L	0, 1, 0, 1, 2, 1	1,-1,1,1,-1
	0, 1, 2, 1, 0, 1	1,1,-1,-1,1
	0, 1, 2, 1, 2, 1	1,1,-1,1,-1
7L	0, 1, 0, 1, 2, 3	1,-1,1,1,1
	0, 1, 2, 1, 2, 3	1,1,-1,1,1
	0, 1, 2, 3, 2, 1	1,1,1,-1,-1
	0, 1, 2, 3, 2, 3	1,1,1,-1,1
9L	0,1,2,3,4,3	1,1,1,1,-1

In SOP technique, a structure is usually represented as sequence of switching transitions $s(i)$ as demanded by expression for d in (2.9) with $s(i) = 1$ when switching to higher potential and $s(i) = -1$ when switching to lower potential. The representation of possible structures of 3L, 5L, 7L and 9L waveforms with $N=5$ illustrated in Fig. 2.3 is done in Table 2.2, in terms of sequence of logic voltage levels and $s(i)$. After determining all possible structures for a given N , the next step is to determine optimal switching patterns for each steady-state operating point (m, N) .

2.4.2 Optimization Algorithm

The optimization algorithm is implemented using MATLAB. Gradient search method ‘FMINCON’ with active-set algorithm searches for switching angles that minimize d . During optimization, the switching angles in a quarter period are determined for phase A and then complete switching pattern is

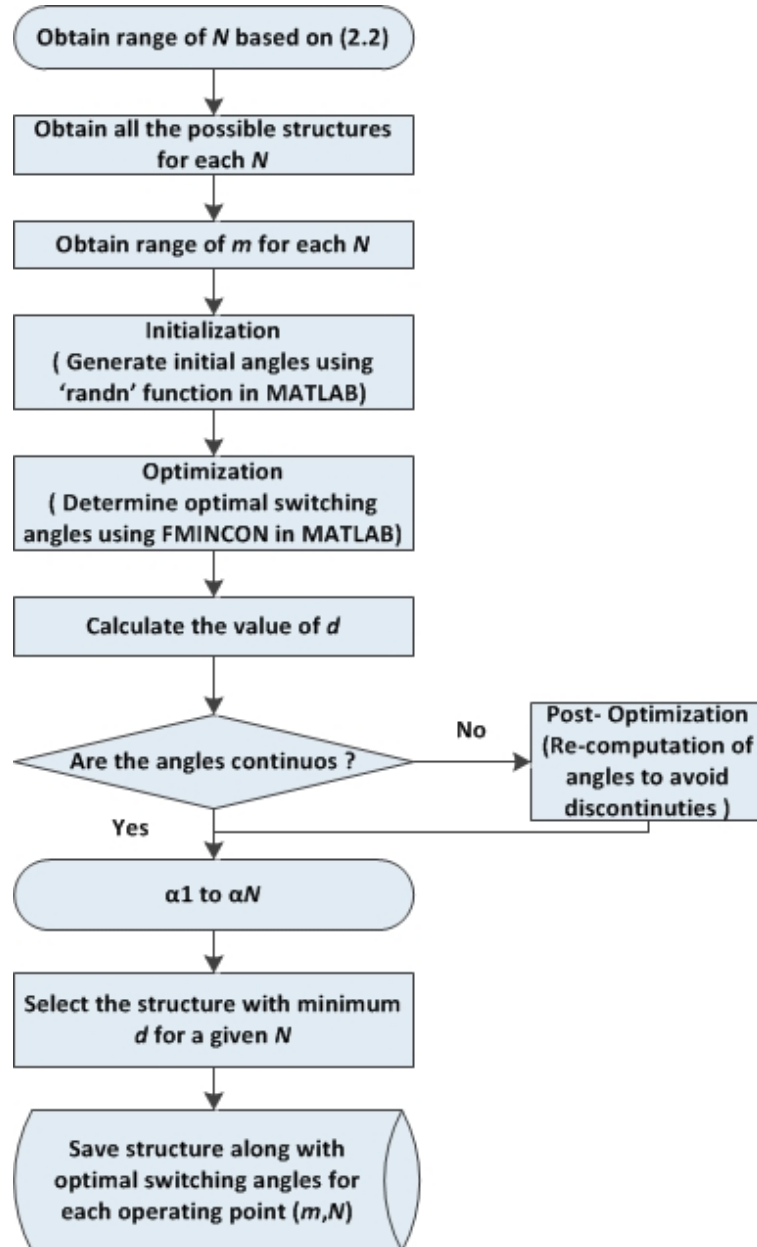


Fig. 2.4: Flowchart of optimization algorithm

obtained by utilizing half-wave and quarter-wave symmetries. Then, the switching patterns for the other two phases are obtained by shifting the phase A switching pattern by 120° and 240° , respectively. The flow chart of optimization algorithm is given in Fig. 2.4. More details of optimization algorithm are given next.

1. **Obtain the range of N :** The range of N for nL -MLC can be obtained by substituting minimum and maximum possible values of m in (2.2).

2. **Obtain all the possible structures of nL waveform for each N :**

An algorithm has been developed to obtain all the possible structures of nL waveform for a given N . All the structures are usually stored in the form of set of $s(i)$ as explained in Section 2.4.1.

3. **Initialization:** The next step is to obtain N switching angles that should correspond to the given value of m . The MATLAB function ‘*randn*’ is used to generate the switching angles α_2 to α_N with mean zero and standard deviation equal to one. Then, the value of α_1 is calculated based on (2.10). The gradient-based search algorithms might not give global best solutions, which depends on the initial switching angles. Therefore, several iterations were carried out in initialization step to obtain multiple set of initial switching angles. The set of switching angles with least value of d are selected and they define the initial values of switching angles for the optimization that follows in the next step.

4. **Optimization:** The MATLAB gradient method ‘*FMINCON*’ with active-set algorithm is used for solving the nonlinear constrained objective function. While calculating the value of d , the harmonic components of order up to 100 were considered. The optimization loop runs for all the possible structures for a given N over its associated modulation index range, starting from the set of initial switching angles obtained in previous step. The goal of optimization is to determine the switching angles that minimize d given by (2.9) with the following constraints:

- (a) Switching angles should be with in the range 0 to 90° .
- (b) Sufficient gap ($10\mu s$) between consecutive switching angles to allow for minimum ON/OFF times of the semiconductor devices.
- (c) Switching angles should satisfy non-linear constraint (2.10)

The iterations stop when the change in the value of objective function $\Delta d < 10^{-15}$. The structure, which exhibits minimum d for all operating points with same N is recorded. Optimal switching angles along with set of $s(i)$ of the structure that exhibits minimum d are stored as look-up tables for each steady state operating point (m, N) .

5. **Post-Optimization:** This loop starts when optimal switching angles were obtained for calculated range of m for a given N . The optimized switching angles for consecutive operating points with same N might have discontinuities. This might lead to transients in machine currents whenever the operating point passes a point of discontinuity. Therefore, post-optimization (PO) should be performed to establish the continuity of switching angles for values of m associated with N . In the beginning, the difference between switching angles of consecutive modulation index values for a given N were calculated. The PO starts if the maximum difference between consecutive switching angles $\Delta\alpha_i$ exceeds 5° . In the PO, the switching angles were re-optimized at the point of discontinuity, by using optimal switching angles corresponding to previous modulation index value as initial values. Due to PO, there might be a little compromise in distortion factor d but it helps avoid the transients in machine currents [114].

2.4.3 Optimization Results

The SOP technique has been used for generating optimal switching angles for 5L, 7L and 9L waveforms with $f_{s,max} = f_{1R}$. The performance of SOP technique in terms of d versus m for 5L, 7L and 9L waveforms before and after post-optimization is shown in Fig. 2.5 (a)-(b), respectively. Similarly, the results of optimization in terms of THD versus m for 5L, 7L and 9L waveforms before and after post-optimization are shown in Fig. 2.6 (a)-(b),

respectively. It should be observed that the performance of SOP technique is slightly compromised with post-optimization, which is necessary to avoid transients in machine currents. Also, harmonic distortion of output waveforms decreases as number of voltage levels increases. When value of m becomes closer to unity, operation of converter will be similar to six-step operation that leads towards higher harmonic distortion.

At lower values of m , the computation time to obtain optimal switching angles greatly increases due to large number of possible structures. Also, the performance of optimization is not much improved compared to classical modulation techniques at lower modulation index values [113]. Therefore, SVM is preferred when $m \leq 0.3$ [161]. However, MV high-power drives are usually operated in the higher modulation index range ($m > 0.5$) [131], where SOP offers superior performance. To conclude, best performance of SOP is expected in the modulation index range $0.3 < m < 0.93$, although SOP can be utilized over entire range of m .

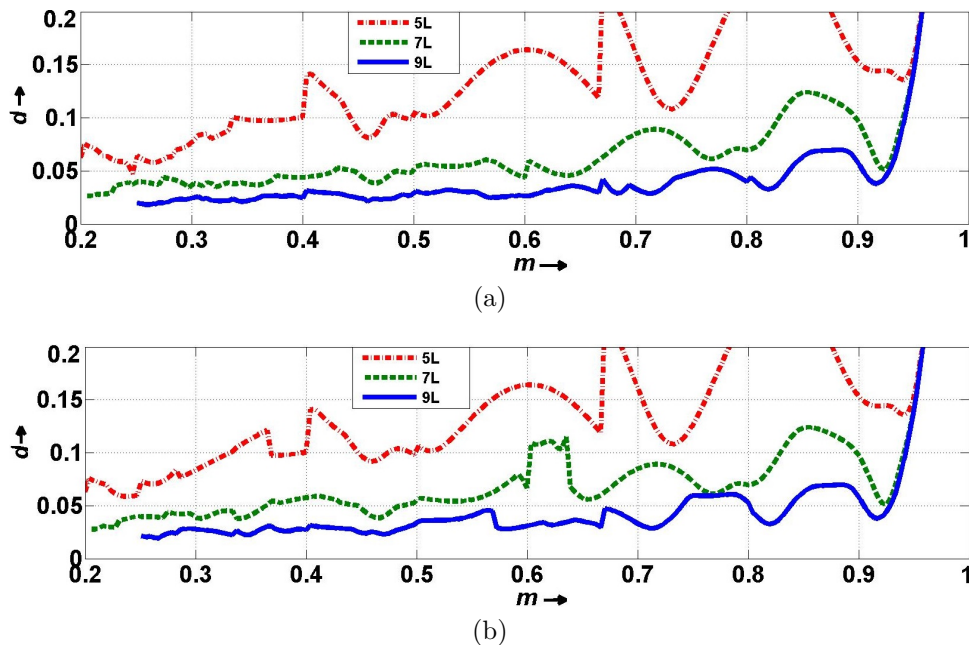


Fig. 2.5: Performance of SOP in terms of d for 5L, 7L and 9L waveforms with $f_{s,max}=f_{1R}$. (a) Before post-optimization (b) After post-optimization

2.5 Allocation of Optimal Switching Angles

The next step in SOP technique is to allocate optimal switching angles to each power semiconductor device. The signal flow graph in Fig. 2.7 explains the details of implementation SOP technique for the MLCs. The magnitude of the reference voltage vector u_{ref} is used for selecting the optimal switching pattern $P(m,N)$, which consists of optimal switching angles along with switching transitions $s(i)$ of best possible structure. The opti-

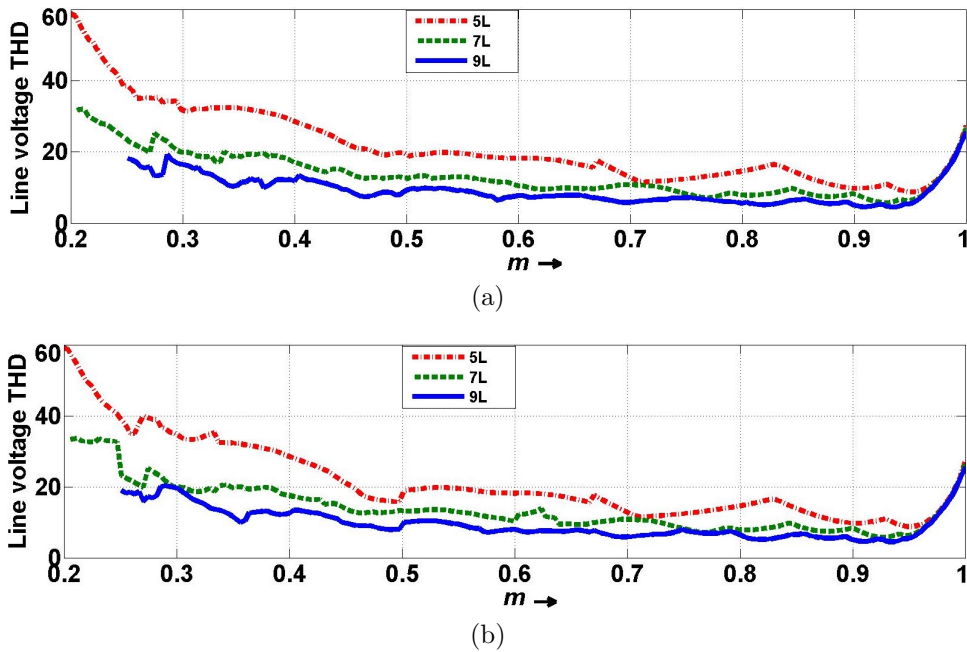


Fig. 2.6: Performance of SOP in terms of line voltage THD for 5L, 7L and 9L waveforms with $f_{s,max}=f_{1R}$. (a) Before post-optimization (b) After post-optimization

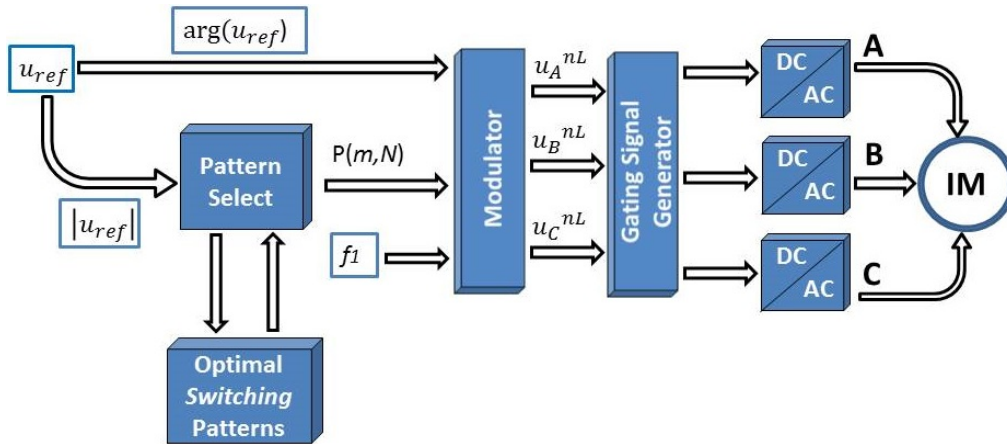


Fig. 2.7: Signal flow graph of SOP technique for an nL -MLC

mal switching pattern $P(m,N)$, phase angle of reference voltage vector and f_1 are given as input to modulator, which generates optimal nL switching state vector u_k^{nL} ($k=A, B, C$) of each phase. In the next stage, gating signal generator is responsible for assigning switching angles to each power semiconductor device based on the optimal switching patterns $P(m,N)$. It should be noted that optimal switching angles of nL waveform can be applied for any nL -MLC topology by modifying the mechanism of gating signal generator.

One of the most important criteria while assigning switching angles to each power semiconductor device is to achieve identical device switching frequency. In addition, there might be other requirements specific to each converter topology such as capacitor voltage balancing, minimizing capacitor voltage ripple, elimination/minimization of common-mode voltages or currents and so on. More details about allocation of switching angles will be treated separately for each MLC topology.

2.6 SOP of Cascaded 7L MLC

This section gives the implementation details of SOP technique for cascaded 7L MLC. In the beginning, circuit topology and operation of 7L MLC are described. Next, implementation details of SOP technique for 7L MLC are presented. At the end, experimental results are demonstrated to show the effectiveness of SOP technique.

2.6.1 Circuit Topology and Operation

The topology of 7L cascade inverter is shown in Fig. 2.8 [163]. Each phase consists of a connected set of 5L-HNPC inverter and the H-Bridge. The classical 7L CHB topology requires three separate dc sources in each phase, whereas this topology requires only two separate dc sources in each phase.

The synthesized output voltage levels of 7L cascade inverter are shown in Table 2.3. The mid-point potential of 3L-NPC1 and 3L-NPC2 phase legs with respect to neutral point 'P' is denoted as V_{3L1} and V_{3L2} , respectively and output voltage of H-Bridge is denoted as V_{HB} . The output potential of 5L-HNPC inverter is denoted as V_{5L} , which is equal to $V_{3L1} - V_{3L2}$. The voltages V_{3L1} and V_{3L2} consists of three discrete voltage levels $-V_{dc}$, 0, and V_{dc} , which are obtained by switching on top two switches, middle two switches, and bottom two switches, respectively. Thus, the output voltage V_{5L1} consists of five discrete voltage levels $-2V_{dc}$, $-V_{dc}$, 0, V_{dc} , and $2V_{dc}$. The voltage V_{HB} consists of three discrete voltage levels $-V_{dc}$, 0, and V_{dc} , which are obtained by switching on (S9,S12), (S9,S11) or (S10,S12), and (S10,S11), respectively. The phase output voltage of 7L cascade inverter is equal to $V_{5L} + V_{HB}$ and thus it consists of seven discrete voltage levels $-3V_{dc}$, $-2V_{dc}$, $-V_{dc}$, 0, V_{dc} , $2V_{dc}$, and $3V_{dc}$.

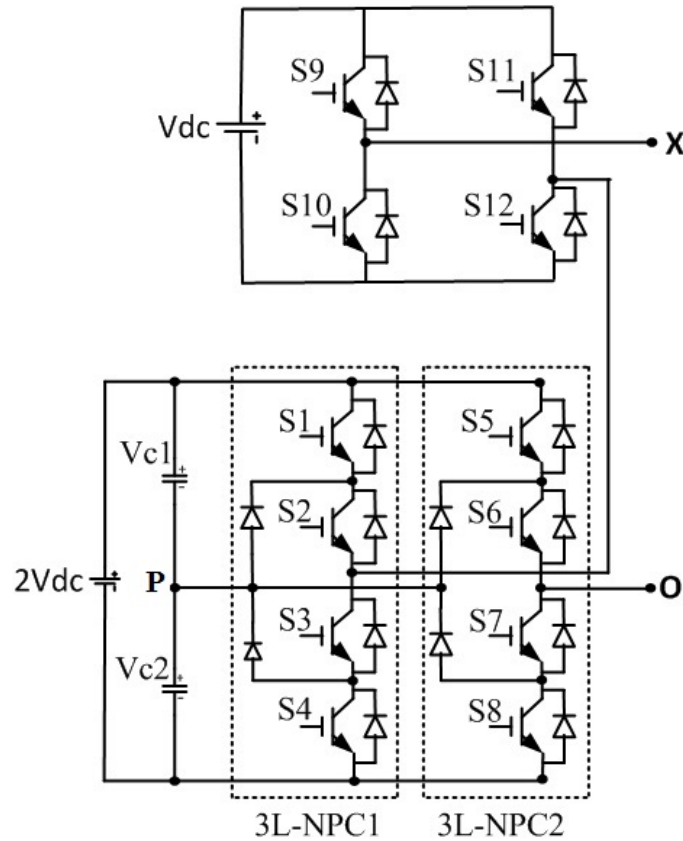


Fig. 2.8: Cascaded 7L inverter topology

Table 2.3: Switching states and synthesized output voltage levels of cascaded 7L MLC

V_{7L}	V_{5L}	V_{3L1}	V_{3L2}	V_{HB}	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
$-3V_{dc}$	$-2V_{dc}$	$-V_{dc}$	V_{dc}	$-V_{dc}$	0	0	1	1	1	1	0	0	0	1	1	0
$-2V_{dc}$	$-2V_{dc}$	$-V_{dc}$	V_{dc}	0	0	0	1	1	1	1	0	0	0	1	0	1
	$-V_{dc}$	$-V_{dc}$	0	$-V_{dc}$	0	0	1	1	0	1	1	0	0	1	1	0
	$-V_{dc}$	0	V_{dc}	$-V_{dc}$	0	1	1	0	1	1	0	0	0	1	1	0
$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	0	0	0	0	1	1	0	1	1	0	0	1	0	1
	$-V_{dc}$	0	V_{dc}	0	0	1	1	0	1	1	0	0	0	1	0	1
	0	0	0	$-V_{dc}$	0	1	1	0	0	1	1	0	0	1	1	0
0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	0	1
V_{dc}	0	0	0	V_{dc}	0	1	1	0	0	1	1	0	1	0	0	1
	V_{dc}	V_{dc}	0	0	1	1	0	0	0	1	1	0	0	1	0	1
	V_{dc}	0	$-V_{dc}$	0	0	1	1	0	0	0	1	1	0	1	0	1
$2V_{dc}$	V_{dc}	V_{dc}	0	V_{dc}	1	1	0	0	0	1	1	0	1	0	0	1
	V_{dc}	0	$-V_{dc}$	V_{dc}	0	1	1	0	0	0	1	1	1	0	0	1
	$2V_{dc}$	V_{dc}	$-V_{dc}$	0	1	1	0	0	0	0	1	1	0	1	0	1
$3V_{dc}$	$2V_{dc}$	V_{dc}	$-V_{dc}$	V_{dc}	1	1	0	0	0	0	1	1	1	0	0	1

2.6.2 Implementation of SOP technique

The SOP algorithm developed in MATLAB programming is used for generating optimal switching angles for 7L waveforms operating with $f_{s,max} = f_{1R}$. The MLC topology shown in Fig. 2.8 consists of two 3L-NPC phase legs and one H-Bridge in each phase and hence, the generalized SOP technique described in Sections 2.2 to 2.5 can be utilized. More details about implementation are given next.

Table 2.4: SOP of 7L-MLC at $f_{s,max}=f_{1R}$: Estimated values of N_{7L} and f_s for a given m

m	f_1	N_{7L}	f_s (Hz)
0.751 - 1	37.55 - 50.00	3	37.55 - 50
0.601 - 0.75	30.05 - 37.50	4	40.06 - 50
0.501 - 0.60	25.05 - 30.00	5	41.75 - 50
0.429 - .050	21.45 - 25.00	6	42.90 - 50
0.376 - 0.428	18.80 - 21.40	7	43.87 - 50
0.334 - 0.375	16.70 - 18.75	8	44.53 - 50
0.301 - 0.333	15.05 - 16.65	9	45.15 - 50

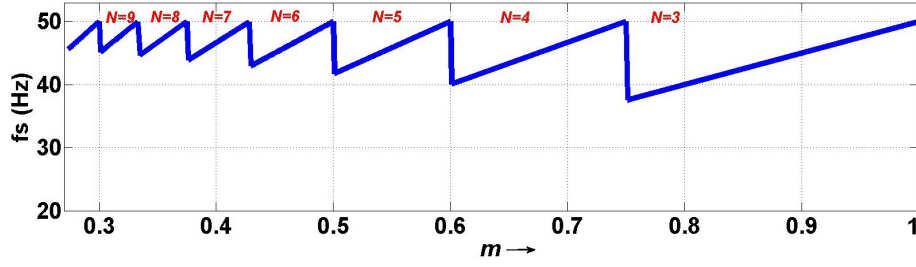


Fig. 2.9: SOP of 7L-MLC at $f_{s,max}=f_{1R}$: Estimated values of N and f_s for a given m

2.6.2.1 Estimation of pulse number, N

The objective of SOP technique is to operate 7L MLC at $f_{s,max} = f_{1R}$. Based on (2.2), the value of pulse number N_{7L} for each discrete value of m is obtained as,

$$N_{7L} = \text{floor} \left(\frac{3f_{s,max}}{m \cdot f_{1R}} \right) = \text{floor} \left(\frac{3}{m} \right). \quad (2.11)$$

Based on (2.11), the estimated value of N_{7L} and corresponding f_s for each discrete value of m is shown in Table 2.4 and Fig. 2.9. It should be observed that f_s is limited to f_{1R} for all operating points.

2.6.2.2 Optimization of switching angles

Based on (2.9) and (2.10), the expression for d and constraint on the switching angles to achieve given modulation index value for constant v/f control of induction motor drive are obtained as,

$$d = \frac{\sqrt{\sum_k \left(\frac{1}{k^4}\right) \left(\sum_{i=1}^N s(i) \cos(k\alpha_i)\right)^2}}{3\sqrt{\sum_k \left(\frac{1}{k^4}\right)}}, \quad (2.12)$$

$$m = \frac{1}{3} \sum_{i=1}^N s(i) \cos(\alpha_i). \quad (2.13)$$

The optimal switching angles for each steady-state operating points are determined based on the optimization algorithm given in Section 2.4.2. Next, details about allocation of optimal switching angles are presented.

Table 2.5: Distribution of switching transitions for cascaded 7L MLC

m	$f_1(Hz)$	N_{7L}	N_{HB}	N_{5L}	N_{3L1}	N_{3L2}	$f_{s,max}$ (Hz) (HB,3L1,3L2)	$f_{s,avg}$ (Hz)
0.751 - 1	37.55 - 50	3	1	2	1	1	50, 50, 50	37.55 - 50
0.601 - 0.75	30.05 - 37.5	4	1	3	1	2	37.5, 37.5, 75	40.06 - 50
			2	2	1	1	75, 37.5, 37.5	
0.501 - 0.600	25.05 - 30	5	1	4	2	2	30, 60, 60	41.75 - 50
			2	3	1	2	60, 30, 60	
0.429 - 0.5	21.45 - 25	6	2	4	2	2	50, 50, 50	42.9 - 50
0.376 - 0.428	18.8 - 21.4	7	2	5	2	3	42.85, 42.85, 64.28	43.87 - 50
			3	4	2	2	64.28, 42.85, 42.85	
0.334 - 0.375	16.7 - 18.75	8	2	6	3	3	37.5, 56.24, 56.24	44.53 - 50
			3	5	2	3	56.24, 37.5, 56.24	
			2	6	2	4	37.5, 37.5, 75	
			4	4	2	2	75, 37.5, 37.5	
0.301 - 0.333	15.05 - 16.65	9	3	6	3	3	50, 50, 50	45.15 - 50

2.6.2.3 Allocation of Optimal Switching Angles

The phase output of cascaded 7L MLC is obtained by combining outputs of 3L-NPC1, 3L-NPC2 and H-Bridge inverters. A systematic procedure is developed to assign switching angles for each semiconductor device from corresponding optimal 7L waveforms. The main challenge is to ensure identical distribution of switching commutations as well as minimal ripple in dc-link capacitor voltages of 5L-HNPC inverter.

A. Equal distribution of switching transitions: The switching transition in a 7L waveform leads to transition in one of the 3L sub-converters, i.e, 3L-NPC1, 3L-NPC2, and H-Bridge. Ideally, the total switching transitions in a 7L waveform, N_{7L} , should be equally divided among all 3L sub-converters to ensure equal distribution of switching losses. However, equal distribution of switching transitions is possible only when N_{7L} is a multiple of 3. Table 2.5 shows possible divisions of switching transitions N_{7L} among all 3L sub-converters. It should be observed that switching transitions are equally divided only when $N_{7L} = 3, 6$ or 9 . Otherwise, each 3L sub-converter will have different switching transitions. In addition, due to constraint of minimizing the dc-link voltage unbalance, equal division of switching transitions may not be possible even if N_{7L} is a multiple of 3. This leads to different device switching frequency for 3L sub-converters and hence, unequal switching losses. However, by using swapping of gating signals, it is possible to operate all power semiconductor devices at same switching frequency [161]. The last column of Table 2.5 shows that $f_{s,avg}$ is limited to f_{1R} for all operating points.

B. Minimizing ripple in dc-link capacitor voltages: The dc-link capacitor voltages of inverter are assumed constant while deriving (2.9). However, there might be ripple in dc-link capacitor voltages of 5L-HNPC inverter that depends on the load condition as well as switching patterns [164]. The difference between two dc-link capacitor voltages is termed as

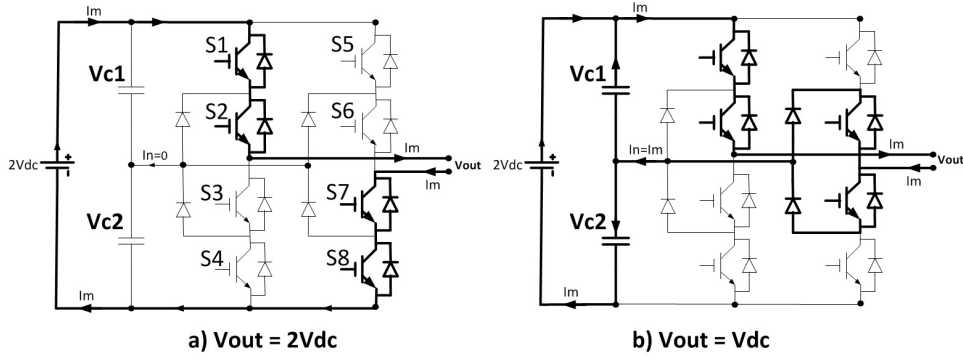


Fig. 2.10: Operation of 5L-HNPC inverter for different switching patterns

NPP error. In steady-state operating conditions, average value of NPP error tends to become zero and thus further distortion of machine currents is negligible [165]. On the other hand, NPP error might get accumulated during transient operation and thus NPP balancing algorithms have been proposed [117, 165, 166]. Moreover, the ripple in dc-link capacitor voltages should be minimized to reduce voltage stress on the power semiconductor devices and capacitors. The analysis of dc-link capacitor voltages of 5L-HNPC inverter for two different switching patterns are shown in Fig. 2.10. It should be observed that, charging and discharging of dc-link capacitor voltages happens when output is $\pm V_{dc}$, otherwise dc-link capacitor voltages remain constant.

2.6.2.4 Analysis for three different operating points

To demonstrate the performance of SOP technique, three operating points ($m=0.9225$, $N=3$), ($m=0.4667$, $N=6$) and ($m=0.3412$, $N=8$) have been selected. The allocation of optimal switching angles for three operating points are shown in Table 2.6 (a)-(c), which is done based on the analysis presented in Section 2.6.2.3. Table 2.7 shows two possible ways of assigning switching angles to power semiconductor devices corresponding to operating point ($m=0.4667$, $N=6$). In both cases the f_s is equal to $2f_1$. However, combination 1 is preferred over combination 2 as it leads to less NPP error in dc-link capacitor voltages of 5L-HNPC inverter. The

reason is that dc-link capacitors are charged/discharged for a shorter duration (30.66°) with combination 1 compared to combination 2 (66.17°) in a quarter period. Thus, combination 1 is selected because unbalance in dc-link capacitor voltages is less.

Table 2.6: Allocation of optimal switching angles for 7L MLC. (a)($m=0.9225$, $N=3$) (b)($m=0.4667$, $N=6$) (c) ($m=0.3412$, $N=8$)

Output	Switching Angles				N
	0°	5.4°	16.48°	34.71°	
V_{7L}	0	1	2	3	3
V_{5L}	0	1	2	2	2
V_{HB}	0	0	0	1	1
V_{3L1}	0	0	1	1	1
V_{3L2}	0	-1	-1	-1	1

(a)

Output	Switching Angles							N
	0°	2.98°	19.79°	27.36°	34.3°	60.57°	83.67°	
V_{7L}	0	1	2	3	2	1	0	6
V_{5L}	0	0	1	2	2	1	0	4
V_{HB}	0	1	1	1	0	0	0	2
V_{3L1}	0	0	0	1	1	0	0	2
V_{3L2}	0	0	-1	-1	-1	-1	0	2

(b)

Output	Switching Angles									
	0°	4.3°	12.15°	18.07°	20.99°	44.15°	46.0°	55.61°	66.9°	N
V_{7L}	0	1	2	1	2	3	2	1	0	8
V_{5L}	0	0	1	1	2	2	1	0	0	4
V_{HB}	0	1	1	0	0	1	1	1	0	4
V_{3L1}	0	0	0	0	1	1	0	0	0	2
V_{3L2}	0	0	-1	-1	-1	-1	-1	0	0	2

(c)

Table 2.7: Allocation of optimal switching angles of 7L MLC for ($m=0.4667$, $N=6$). (a) Combination 1 (b) Combination 2

Angle (deg)	V_{7L}	V_{5L}	V_{HB}	Duration (deg)
0	0	0	0	2.98
2.98	1	0	1	16.81
19.79	2	1	1	7.56
27.36	3	2	1	6.94
34.30	2	2	0	26.26
60.57	1	1	0	23.10
83.67	0	0	0	6.33
	$N=6$	$N=4$	$N=2$	

(a)

Angle (deg)	V_{7L}	V_{5L}	V_{HB}	Duration (deg)
0	0	0	0	2.98
2.98	1	1	0	16.81
19.79	2	2	0	7.56
27.36	3	2	1	6.94
34.30	2	1	1	26.26
60.57	1	1	0	23.10
83.67	0	0	0	6.33
	$N=6$	$N=4$	$N=2$	

(b)

2.6.3 Experimental results

A low power prototype of 7L cascade inverter has been developed for demonstrating the performance of SOP technique, as shown in Fig. 2.11. It has been implemented using 3L-NPC and six-pack modules from Infineon, and a six-pack IGBT driver SKHI 61R from Semikron. It should be noted that by using different pin configurations, it is possible to drive 3L-NPC module using SKHI 61R. The list of major components along with their rated parameters are shown in Table 2.8. The gating signals were pro-

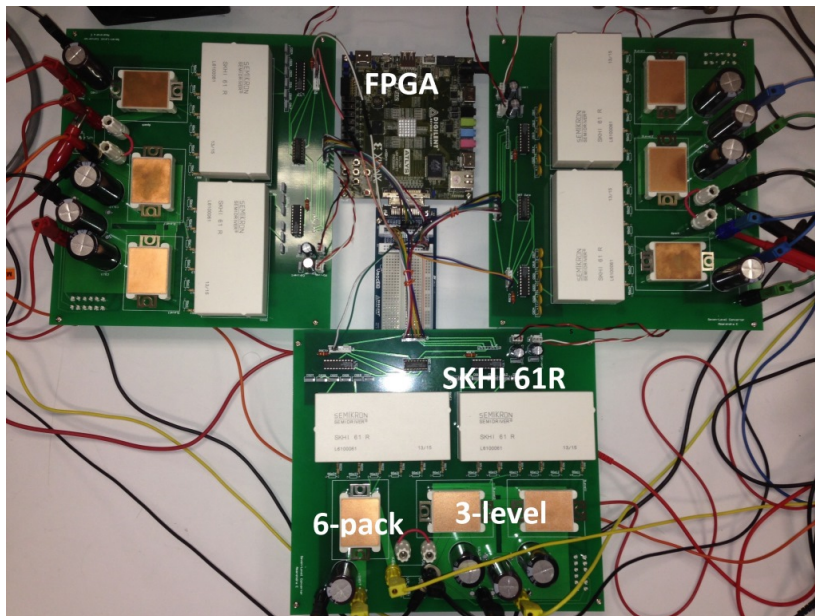


Fig. 2.11: Experimental setup of 7L MLC

Table 2.8: Parameters of major components in 7L MLC prototype

Components	Parameters
Induction Motor	1.5 kW, 400 V, 50 Hz
3L-NPC Module	F3L30R06W1E3_B11 $V_{CE} = 600$ V, $I_{Cnom} = 30$ A
Six-pack Module	FS30R06W1E3 $V_{CE} = 600$ V, $I_{Cnom} = 30$ A
Six-pack Driver	SKHI 61R $V_{CE} = 900$ V, $f_{max} = 50$ kHz
DC-link Capacitors	1000 μ F, 160 V electrolytic

grammed on a Xilinx Spartan-6 FPGA. Input dc voltage to H-Bridge and 5L-HNPC inverter are maintained at 40.75 V and 81.5 V, respectively, so that inverter feeds the 1.5-kW induction motor with phase voltage of 110 V at $f_1 = f_{1R}$. The inverter output is connected to induction motor without using any LC filter in order to get better understanding of dominant harmonics in converter output currents.

The assignment of optimal switching angles to each 3L sub-converter for the three operating points ($m=0.9225$, $N=3$), ($m=0.4667$, $N=6$) and ($m=0.3412$, $N=8$) are shown in Table 2.6 (a)-(c), respectively. The value of N and f_s for these operating points are summarized in Table 2.9 (a)-(c), respectively. For operating point ($m=0.4667$, $N=6$), f_s should be equal to $2f_1$ as $N=2$ for each 3L sub-converter, as shown in Table 2.9 (b). This can be confirmed from Fig. 2.12, which shows that each power semiconductor device has four commutations in one fundamental period, i.e., $f_s = 2f_1$.

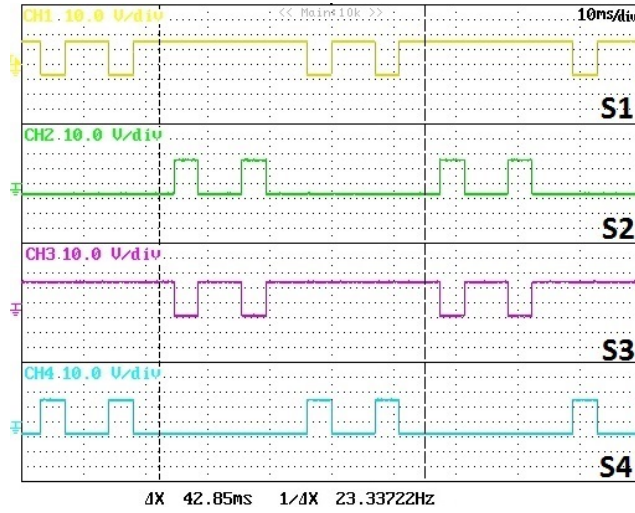
Table 2.9: Estimated values of N and f_s for 7L MLC: (a) ($m=0.9225$, $N=3$) (b) ($m=0.4667$, $N=6$) (c) ($m=0.3412$, $N=8$)

IGBT	N	f_s (Hz)	IGBT	N	f_s (Hz)	IGBT	N	f_s (Hz)
S1-S4	2	46.275	S1-S4	4	46.67	S1-S4	4	34.12
S5-S8	2	46.275	S5-S8	4	46.67	S5-S8	4	34.12
S9-S12	2	46.275	S9-S12	4	46.67	S9-S12	8	68.24

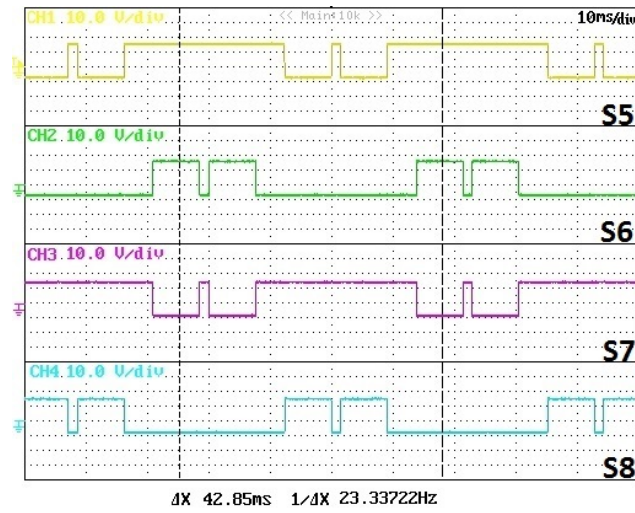
(a)

(b)

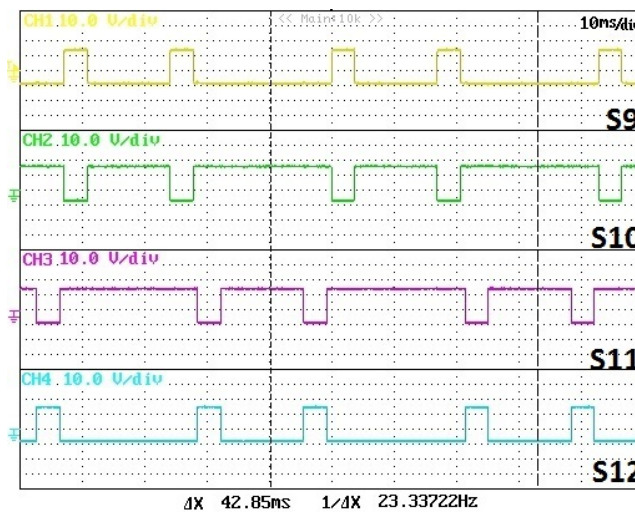
(c)



(a)

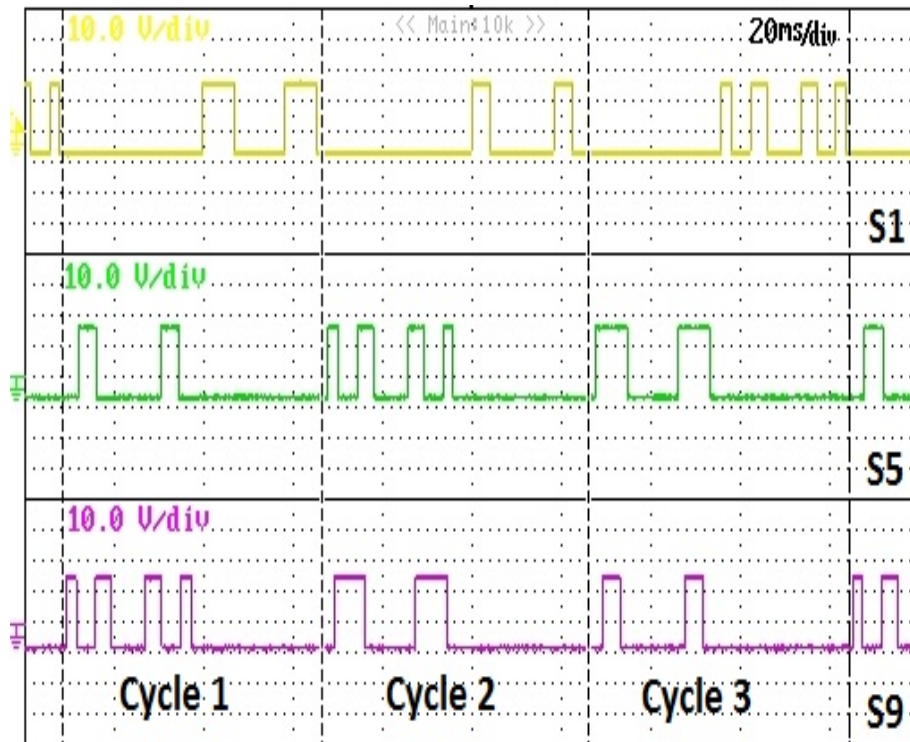


(b)

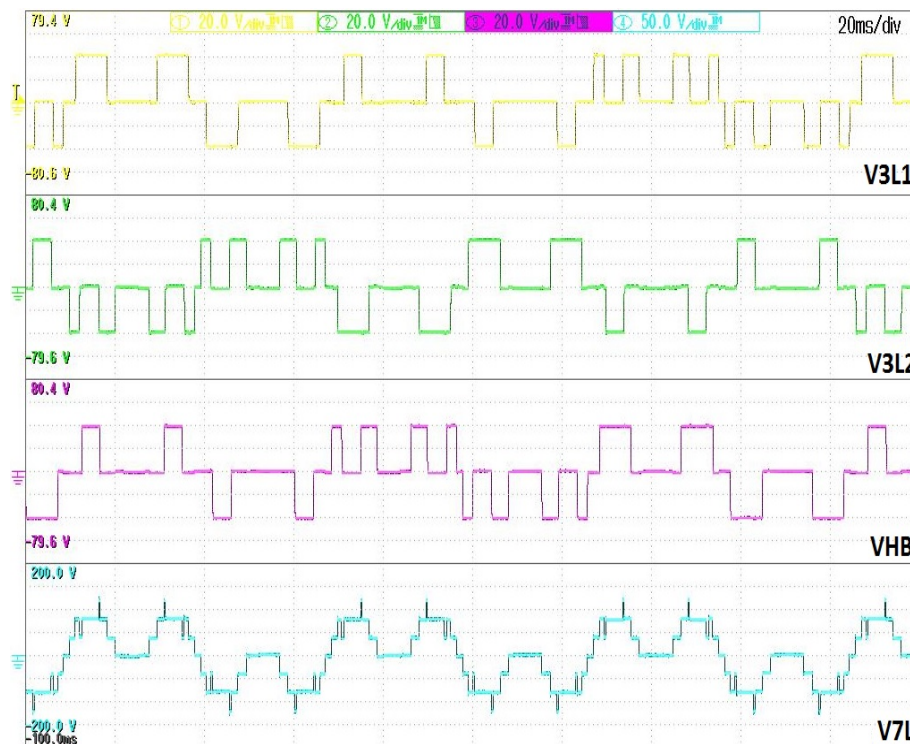


(c)

Fig. 2.12: Gating signals of power semiconductor devices for ($m=0.4667$, $N=6$). (a) 3L-NPC1 (b) 3L-NPC2 (c) H-Bridge



(a)



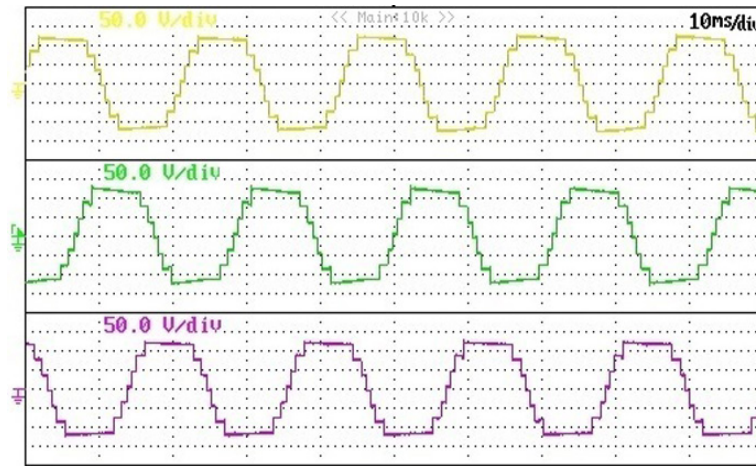
(b)

Fig. 2.13: Swapping technique for operating point ($m=0.3412$, $N=8$). (a) Gating signals of S1, S5 and S9 (b) Output voltage of 3L-NPC1, 3L-NPC2, H-Bridge and 7L-MLC

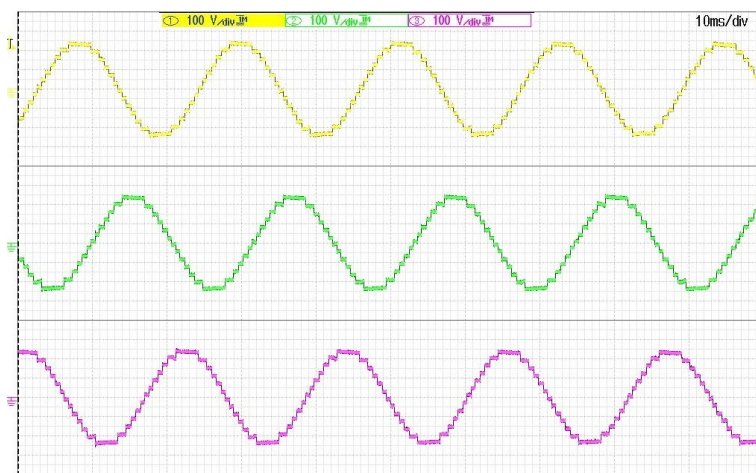
The distribution of switching commutations among 3L sub-converters for the operating point ($m=0.3412$, $N=8$) is shown in Table 2.6 (c) and summarized in Table 2.9 (c). It should be observed that value of N is different for sub-converters and thus power semiconductor devices will be operating at different switching frequency, i.e., $2f_1$, $2f_1$ and $4f_1$. By swapping the switching patterns among sub-converters after every fundamental cycle, it is possible to achieve identical device switching frequency. The swapping of gating signals can be observed in Fig. 2.13 (a) for three consecutive fundamental cycles. It should be observed from the waveforms that each semiconductor device has total switching transitions equal to 16 in three fundamental cycles and thus, device switching frequency will be equal to $\frac{8f_1}{3}$. The output voltages of 3L-NPC1, 3L-NPC2 and H-Bridge sub-converters with swapping of gating signals are shown in Fig. 2.13 (b). It should be noticed that the output phase voltage of 7L inverter remains the same with swapping of gating signals among 3L sub-converters.

For three operating points ($m=0.9225$, $N=3$), ($m=0.4667$, $N=6$), and ($m=0.3412$, $N=8$), phase voltage, line voltage and output currents of 7L inverter are shown in Figs. 2.14 (a)-(c) to Figs. 2.16 (a)-(c), respectively. It should be observed that the stator currents of induction motor are sinusoidal, although very low device switching frequencies equal to 46.275 Hz, 46.67 Hz and 45.49 Hz ($< f_{1R}$), respectively, have been utilized. It should be observed that the harmonic distortion of machine stator currents increases at lower values of m .

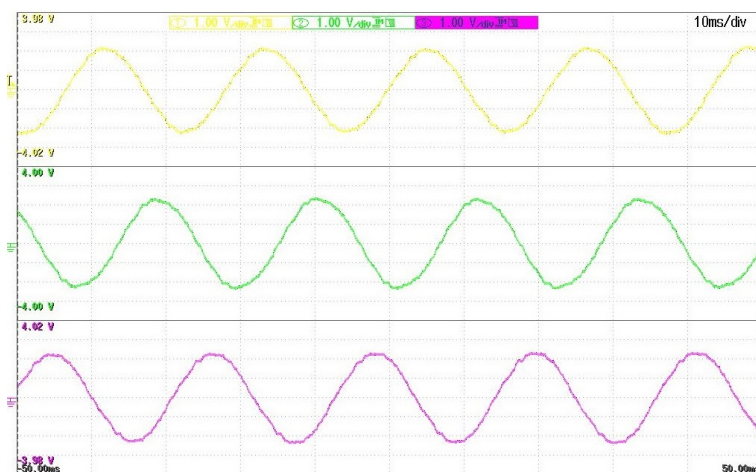
The dc-link capacitor voltages of 5L-HNPC inverter for the three operating points are shown in Fig. 2.17 (a)-(c), respectively. It should be observed that ripple in capacitor voltages is minimal. For operating point ($m=0.4667$, $N=6$), the dc-link capacitor voltages shown in Fig. 2.17 (b) have more NPP error due to higher duration for charging/discharging of dc-link capacitors (30.66°) compared to other operating points.



(a)

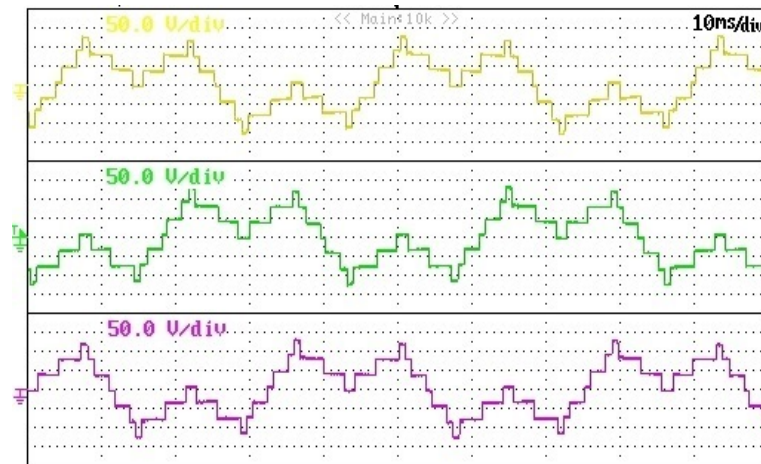


(b)

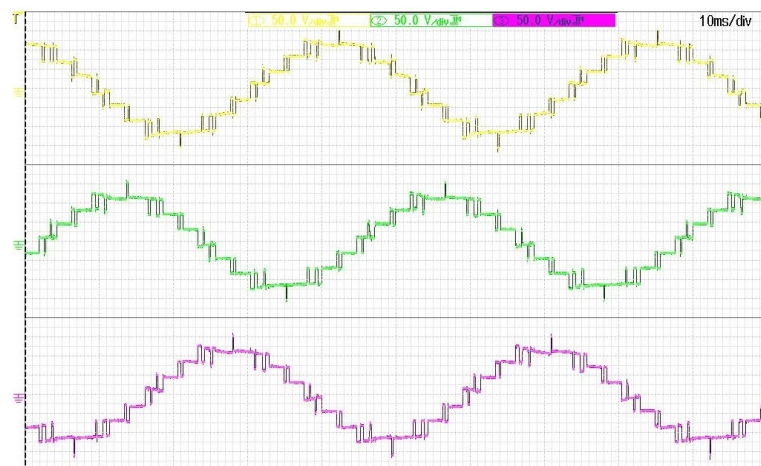


(c)

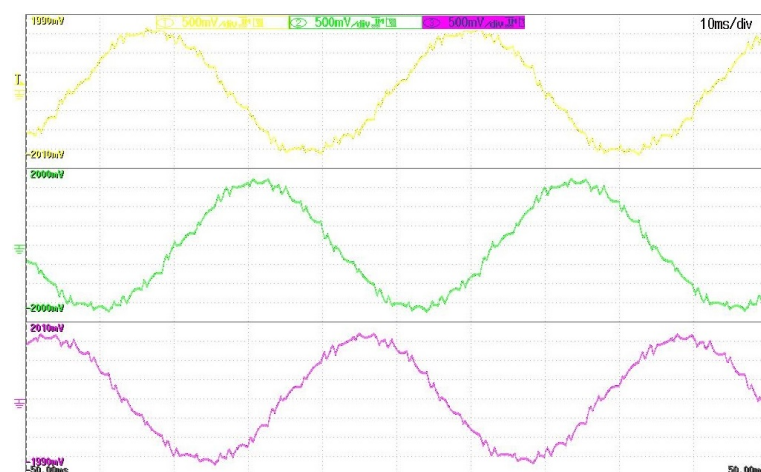
Fig. 2.14: Experimental results for ($m=0.9225$, $N=3$). X-axis:10 ms/div (a) Phase voltages of 7L inverter (Y-axis:50 V/div) (b) Input line voltages of induction motor (Y-axis:100 V/div) (c) Stator currents of induction motor (Y-axis:1 A/div)



(a)

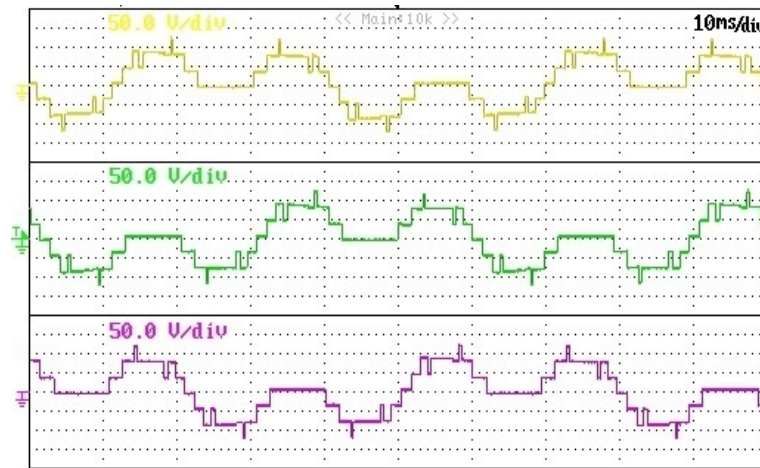


(b)

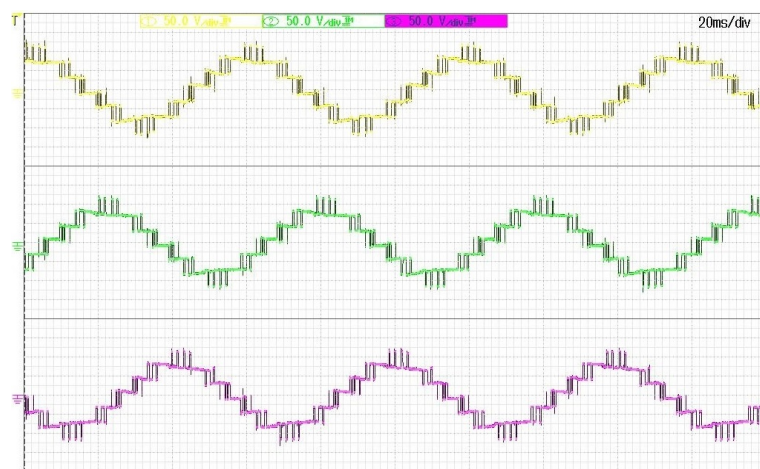


(c)

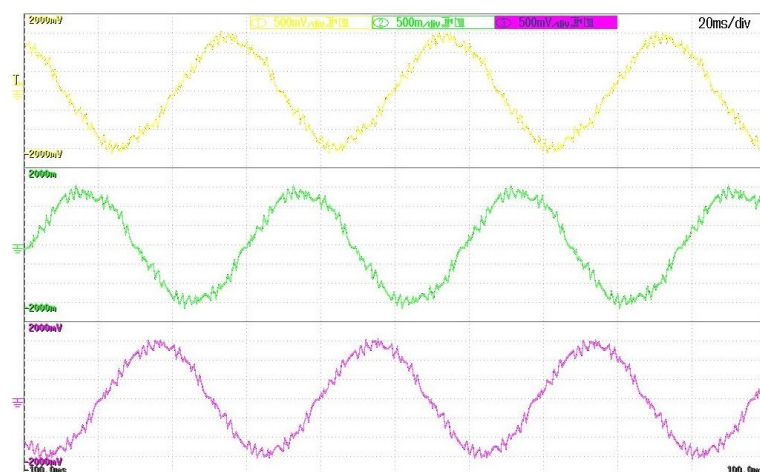
Fig. 2.15: Experimental results for ($m=0.4667$, $N=6$). X-axis:10 ms/div (a) Phase voltages of 7L inverter (Y-axis:50 V/div) (b) Input line voltages of induction motor (Y-axis:50 V/div) (c) Stator currents of induction motor (Y-axis:0.5 A/div)



(a)

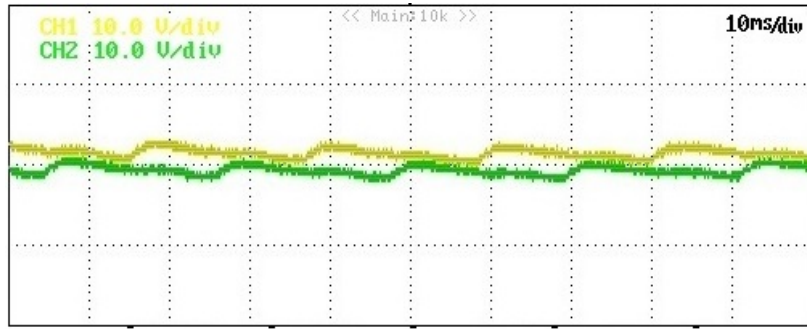


(b)

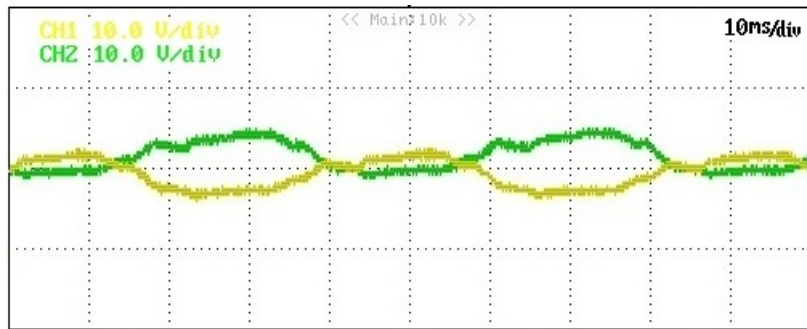


(c)

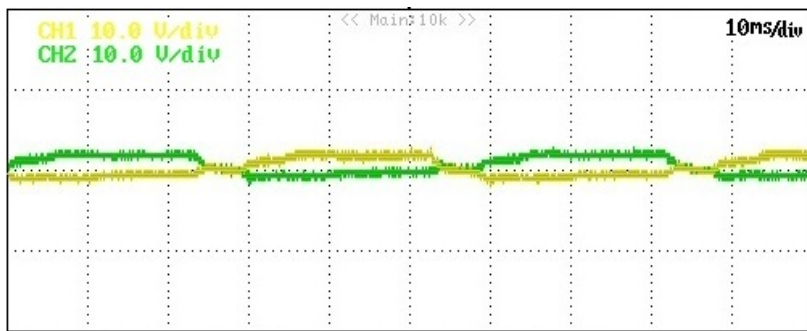
Fig. 2.16: Experimental results for ($m=0.3412$, $N=8$). (a) Phase voltages of 7L inverter (X-axis:10 ms/div, Y-axis:50 V/div) (b) Input line voltages of induction motor (X-axis:20 ms/div, Y-axis:50 V/div) (c) Stator currents of induction motor (X-axis:20 ms/div, Y-axis:0.5 A/div)



(a)

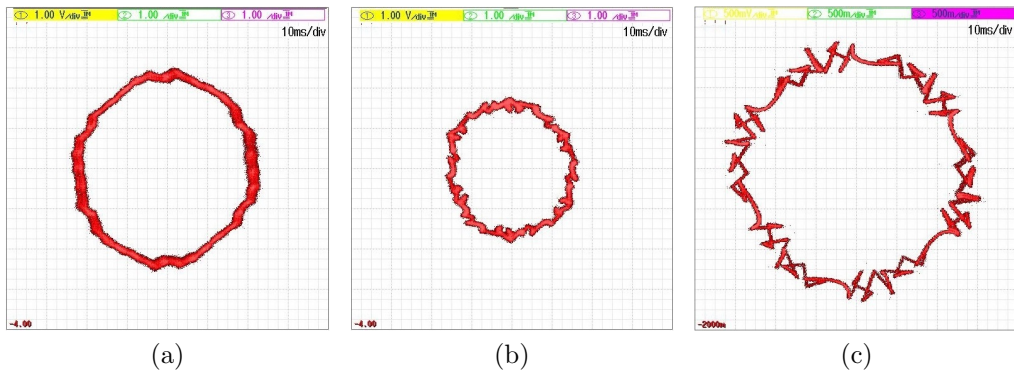


(b)



(c)

Fig. 2.17: Dc-link voltages of 5L-HNPC inverter. X-axis:10 ms/div, Y-axis:10 V/div. (a) ($m=0.9225, N=3$) (b) ($m=0.4667, N=6$) (c) ($m=0.3412, N=8$)



(a)

(b)

(c)

Fig. 2.18: Space vector trajectory of machine stator currents. X,Y-axes:1 A/div. (a) ($m=0.9225, N=3$) (b) ($m=0.4667, N=6$) (c) ($m=0.3412, N=8$)

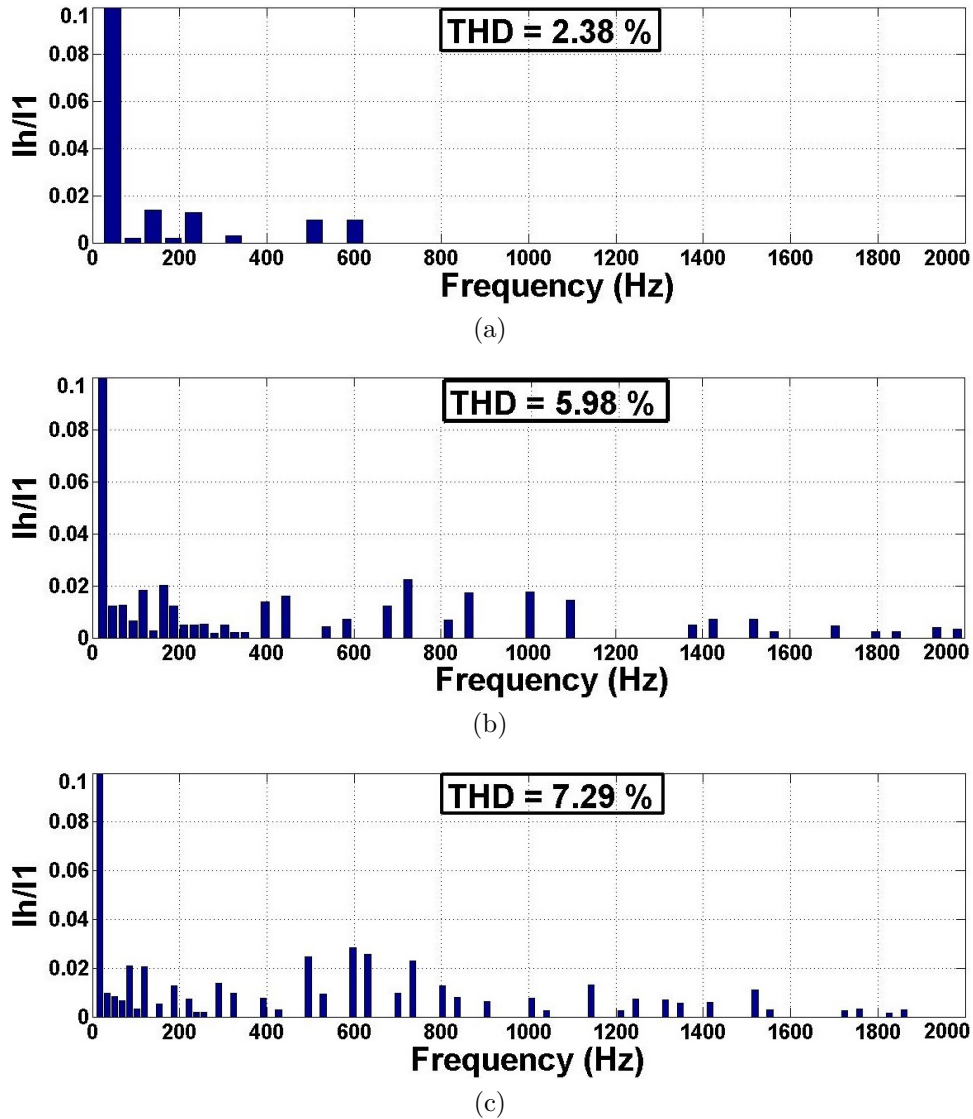


Fig. 2.19: Harmonic spectrum of stator currents. (a) ($m=0.9225$, $N=3$) (b) ($m=0.4667$, $N=6$) (c) ($m=0.3412$, $N=8$)

The space vector trajectory of induction motor stator currents for three operating points are shown in Fig. 2.18 (a)-(c), respectively. The nearly circular space vector trajectories indicates minimal harmonic distortion. It should be observed that harmonic distortion increases at lower m values. Also, data acquisition system has been used to record data of stator currents for demonstrating harmonic spectrum of stator currents. The harmonic spectrum of the stator currents for the three operating points are shown in Fig. 2.19 (a)-(c), respectively. The THD of stator currents for three operating points is equal to 2.38%, 5.98% and 7.29%, respectively and it

should be noted that all the dominant harmonic components are less than 3% of the fundamental component. Therefore, it should be concluded that SOP technique can reduce the average device switching frequency to f_{1R} without compromising on the quality of stator currents.

2.7 SOP of Cascaded 9L MLC

This Section gives the implementation details of SOP technique for cascaded 9L MLC. Initially, circuit topology and operation of 9L MLC are described and then implementation details for SOP of 9L MLC are presented. Finally, experimental results from 9L MLC fed 1.5-kW induction motor are demonstrated to show the effectiveness of SOP technique.

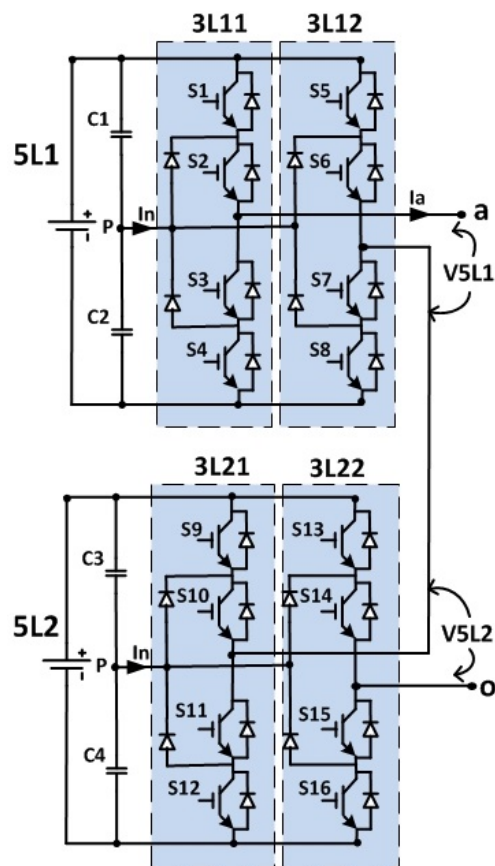


Fig. 2.20: Cascade 9L MLC topology

Table 2.10: Operation of cascade 9L MLC

$\mathbf{V_{9L}}$	$\mathbf{V_{5L1}}$	$\mathbf{V_{3L11}}$	$\mathbf{V_{3L12}}$	$\mathbf{V_{5L2}}$	$\mathbf{V_{3L21}}$	$\mathbf{V_{3L22}}$
$-4V_{dc}$	$-2V_{dc}$	$-V_{dc}$	V_{dc}	$-2V_{dc}$	$-V_{dc}$	V_{dc}
$-3V_{dc}$	$-2V_{dc}$	$-V_{dc}$	V_{dc}	$-V_{dc}$	$-V_{dc}$	0
	$-V_{dc}$	$-V_{dc}$	0	$-2V_{dc}$	$-V_{dc}$	V_{dc}
$-2V_{dc}$	$-2V_{dc}$	$-V_{dc}$	V_{dc}	0	0	0
	$-V_{dc}$	$-V_{dc}$	0	$-V_{dc}$	$-V_{dc}$	0
	0	0	0	$-2V_{dc}$	$-V_{dc}$	V_{dc}
$-V_{dc}$	$-2V_{dc}$	$-V_{dc}$	V_{dc}	V_{dc}	V_{dc}	0
	$-V_{dc}$	$-V_{dc}$	0	0	0	0
	0	0	0	$-V_{dc}$	$-V_{dc}$	0
	V_{dc}	V_{dc}	0	$-2V_{dc}$	$-V_{dc}$	V_{dc}
0	0	0	0	0	0	0
V_{dc}	$-V_{dc}$	$-V_{dc}$	0	$2V_{dc}$	V_{dc}	$-V_{dc}$
	0	0	0	V_{dc}	V_{dc}	0
	V_{dc}	V_{dc}	0	0	0	0
	$2V_{dc}$	V_{dc}	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	0
$2V_{dc}$	0	0	0	$2V_{dc}$	V_{dc}	$-V_{dc}$
	V_{dc}	V_{dc}	0	V_{dc}	V_{dc}	0
	$2V_{dc}$	V_{dc}	$-V_{dc}$	0	0	0
$3V_{dc}$	V_{dc}	V_{dc}	0	$2V_{dc}$	V_{dc}	$-V_{dc}$
	$2V_{dc}$	V_{dc}	$-V_{dc}$	V_{dc}	V_{dc}	0
$4V_{dc}$	$2V_{dc}$	V_{dc}	$-V_{dc}$	$2V_{dc}$	V_{dc}	$-V_{dc}$

2.7.1 Circuit topology and Operation

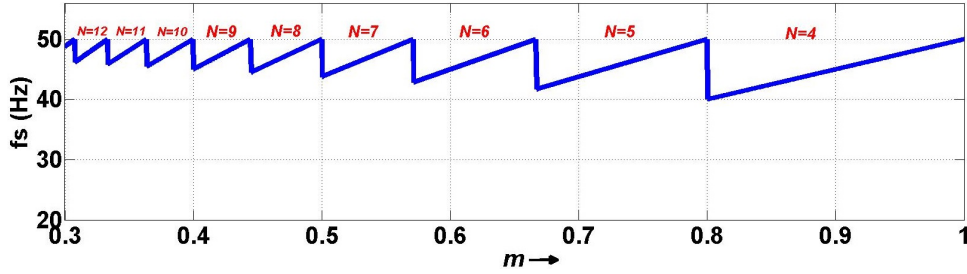
The topology of cascade 9L MLC is shown in Fig. 2.20. It consists of two 5L-HNPC converters connected in series. Each phase leg of 5L-HNPC converter generates three voltage levels ($-V_{dc}, 0, V_{dc}$) with respect to neutral point 'P'. The phase output voltage of each 5L-HNPC inverter consists of five voltage levels ($-2V_{dc}, -V_{dc}, 0, V_{dc}, 2V_{dc}$). As two 5L-HNPC inverters are connected in series, the inverter phase output voltage consists of nine voltage levels ($-4V_{dc}, -3V_{dc}, -2V_{dc}, -V_{dc}, 0, V_{dc}, 2V_{dc}, 3V_{dc}, 4V_{dc}$). The steady-state operation of cascade 9L MLC is shown in Table 2.10.

2.7.2 Implementation of SOP Technique

The SOP algorithm developed in MATLAB programming is used for generating optimal switching angles for 9L waveforms with $f_{s,max} = f_{1R}$. The 9L MLC topology shown in Fig. 2.20 consists of four 3L-NPC sub-converters in

Table 2.11: SOP of 9L MLC at $f_{s,max} = f_{1R}$: Estimated values of N_{9L} and f_s for a given m

m	f_1	N_{9L}	f_s (Hz)
0.801 - 1.000	40.05-50.00	4	40.05 - 50
0.668 - 0.800	33.40-40.00	5	41.75 - 50
0.572 - 0.667	28.60-33.35	6	42.90 - 50
0.501 - 0.571	25.05-28.55	7	43.84 - 50
0.445 - 0.500	22.25-25.00	8	44.50 - 50
0.401 - 0.444	20.05-22.20	9	45.11 - 50
0.365 - 0.400	18.25-20.00	10	45.62 - 50
0.334 - 0.364	16.70-18.20	11	45.92 - 50
0.309 - 0.333	15.45-16.65	12	46.35 - 50
0.287 - 0.308	14.35-15.40	13	46.64 - 50

Fig. 2.21: SOP of 9L MLC at $f_{s,max} = f_{1R}$: Estimated values of N_{9L} and f_s for a given m

each phase and thus, the generalized SOP technique described in Sections 2.2 to 2.5 can be utilized. Further details are given next.

2.7.2.1 Estimation of pulse number, N

Based on (2.2), the value of N_{9L} for each discrete value of m to operate 9L inverter with $f_{s,max} = f_{1R}$ is obtained as,

$$N_{9L} = \text{floor} \left(\frac{4f_{s,max}}{mf_{1R}} \right) = \text{floor} \left(\frac{4}{m} \right). \quad (2.14)$$

Based on (2.14), the estimated value of N_{9L} and corresponding f_s for a given m is shown in Table 2.11 and Fig. 2.21. It should be observed that $f_{s,max}$ is limited to f_{1R} for entire range of m .

Table 2.12: Distribution of switching commutations for cascaded 9L MLC

m	N_{9L}	N_{5L1}	N_{5L2}	N_{3L1}	N_{3L2}	N_{3L3}	N_{3L4}	$f_{s,max}(3L1-3L4)$ (Hz)	$f_{s,avg}$ (Hz)
0.801 - 1.000	4	2	2	1	1	1	1	50, 50, 50, 50	40.05 - 50
0.668 - 0.800	5	2	3	1	1	1	2	40, 40, 40, 80	41.75 - 50
0.572 - 0.667	6	3	3	1	2	1	2	33.33, 66.67, 33.33, 66.67	42.90 - 50
0.501 - 0.571	7	3	4	2	1	2	2	57.10, 28.55, 57.10, 57.10	43.84 - 50
0.445 - 0.500	8	4	4	2	2	2	2	50, 50, 50, 50	44.50 - 50
0.401 - 0.444	9	4	5	2	2	2	3	44.40, 44.40, 44.40, 66.60	45.11 - 50
0.365 - 0.400	10	5	5	2	3	3	2	40, 60, 60, 40	45.62 - 50
0.334 - 0.364	11	5	6	2	3	3	3	36.40, 54.60, 54.60, 36.40	45.92 - 50
	5	3	6	2	6	2	4	54.60, 36.40, 36.40, 72.80	
0.309 - 0.333	12	6	6	3	3	3	3	50, 50, 50, 50	46.35 - 50
0.287 - 0.308	13	6	7	3	3	3	4	46.20, 46.20, 46.20, 61.60	46.64 - 50

2.7.2.2 Optimization of switching angles

The expression of d for the 9L MLC can be obtained from (2.9) as follows,

$$d = \frac{\sqrt{\sum_k (\frac{1}{k^4}) (\sum_{i=1}^N s(i) \cos(k\alpha_i))^2}}{4\sqrt{\sum_k (\frac{1}{k^4})}}. \quad (2.15)$$

Based on (2.10), the constraint on the switching angles to maintain current modulation index value with constant v/f control of induction motor drive can be obtained as,

$$m = \frac{1}{4} \sum_{i=1}^N s(i) \cos(\alpha_i). \quad (2.16)$$

The optimal switching angles for all steady-state operating points are determined based on the optimization algorithm given in Section 2.4. Details of assigning switching angles to each semiconductor device are given next.

2.7.2.3 Allocation of Optimal Switching Angles

The next step after determining optimal switching angles is to allocate optimal switching angles to each power semiconductor device. The output of cascaded 9L inverter is obtained by combining the outputs of four 3L-NPC sub-converters. The main challenge is to choose those combinations that achieve identical device switching frequency as well as minimize the dc-link capacitor voltage ripple in each 5L-HNPC inverter.

A. Equal distribution of switching commutations: One of the most important criteria to be considered while assigning switching angles is to achieve identical device switching frequency. Each switching transition in a 9L waveform is due to switching transition in one of the four 3L-NPC inverters, which should be equally distributed to achieve same switching frequency for all power semiconductor devices. However, equal distribution of switching transitions among all four 3L-NPC inverters is possible only

when N_{9L} is a multiple of four. The distribution of switching transitions among four 3L-NPC inverters is shown in Table 2.12 for all steady-state operating points. It should be observed that for $N_{9L}=4, 8$ or 12 , switching transitions are equally divided among four 3L-NPC inverters, otherwise each 3L-NPC inverters will have different switching transitions. Additional measures like swapping of gating signals among four 3L-NPC inverters after every fundamental cycle is required to establish same number of switching transitions and thus achieve identical device switching frequency [161].

B. Minimizing dc-link capacitor voltage ripple: During optimization calculations, dc-link capacitor voltages are assumed constant. However, 3L-NPC topology contains floating dc-link capacitors which are not stabilized by external sources. Therefore, it is important to maintain dc-link capacitor voltage balance and also minimize the voltage ripple to avoid further distortion of machine stator currents and also to reduce the high voltage stress on power semiconductor devices as well as dc-link capacitors. It should be observed from Fig. 2.20 that potential of neutral point ‘P’ is floating and it changes in proportion to integral of neutral point current I_n . The neutral point current I_n depends on the load condition as well as switching patterns [164]. The difference between two dc-link capacitor voltages is termed as NPP error.

Table 2.13: Analysis of dc-link capacitor voltages of 5L-HNPC

5L	3L1	3L2	In	Vdc1	Vdc2
$2V_{dc}$	V_{dc}	$-V_{dc}$	0	Constant	Constant
V_{dc}	0	$-V_{dc}$	+ve	Charging	Discharging
V_{dc}	V_{dc}	0	-ve	Discharging	Charging
0	0	0	0	Constant	Constant
$-V_{dc}$	0	V_{dc}	-ve	Discharging	Charging
$-V_{dc}$	$-V_{dc}$	0	+ve	Charging	Discharging
$-2V_{dc}$	$-V_{dc}$	V_{dc}	0	Constant	Constant

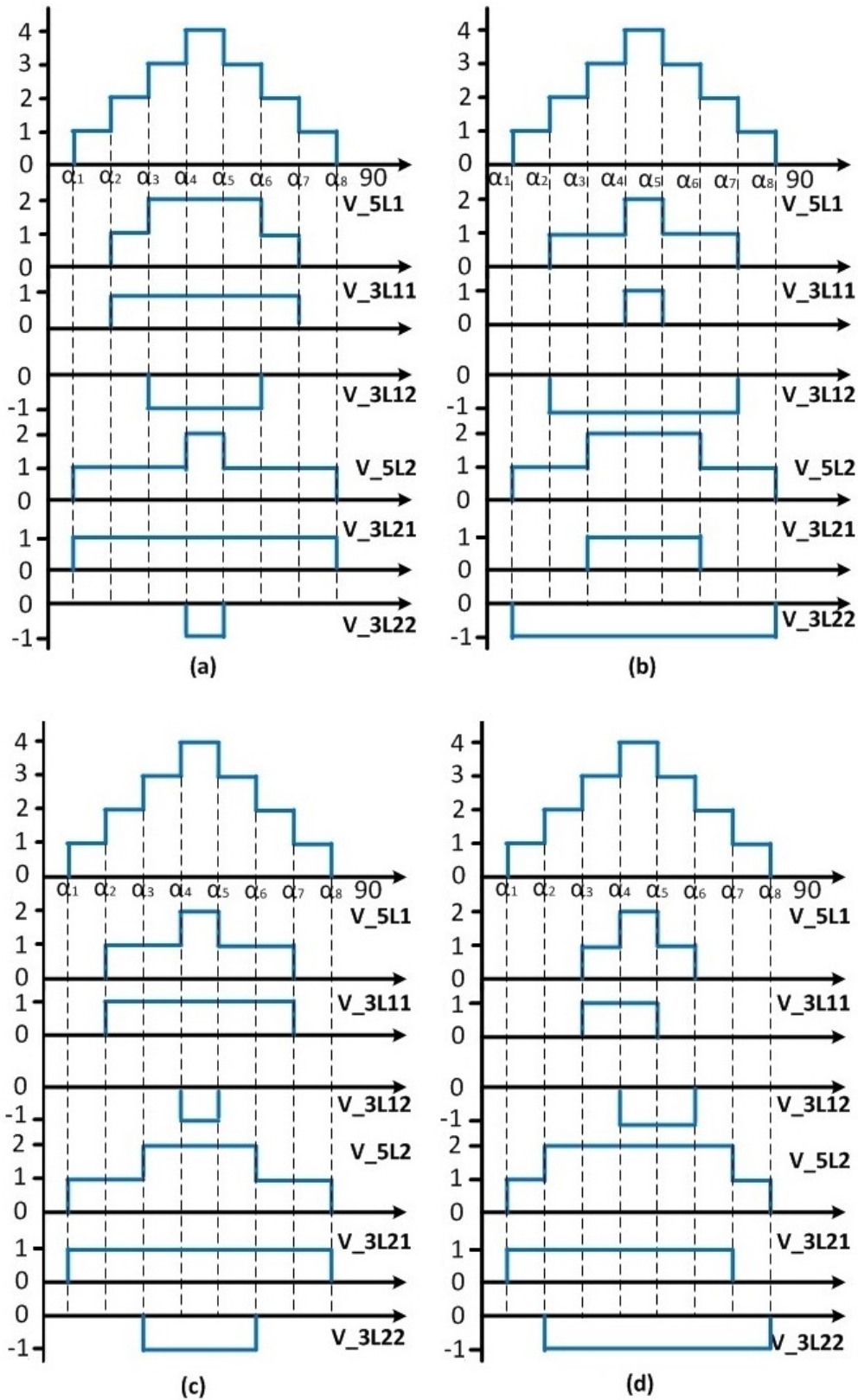


Fig. 2.22: Different possible realizations of 9L waveform

It should be observed from Table 2.13 that charging and discharging of dc-link capacitor voltages happens when the output potential of 5L-HNPC is $\pm V_{dc}$, whereas dc-link capacitor voltages remains constant if the output voltage of 5L-HNPC inverter is 0 or $\pm 2V_{dc}$. Due to natural balancing mechanism of NPC converters [165], the average value of NPP error tends to become zero in steady-state operating conditions and thus further distortion of machine currents is negligible. However, transient operating conditions might lead to accumulation of NPP error and thus several NPP balancing algorithms have been suggested in the literature [117, 165, 166].

Moreover, the ripple in dc-link capacitor voltages should be minimized otherwise it leads to high voltage stress on the power semiconductor devices and capacitors. This is possible by dividing the optimal 9L waveform such that output potential of V_{5L1}, V_{5L2} is $\pm V_{dc}$ for shorter duration. For example, four possible realizations of a optimal 9L waveform are shown in Fig. 2.22. With combination in Fig. 2.22 (d), output potential of V_{5L1}, V_{5L2} becomes $\pm V_{dc}$ for shorter time interval. Therefore, combination (d) is preferable to achieve minimal ripple in dc-link capacitor voltages. The exact value of unbalance depends on the load conditions.

Based on above analysis, distribution of commutations for three different operating points ($m=0.9216, N=4$), ($m=0.5804, N=6$), and ($m=0.4706, N=8$) are shown in Table 2.14 (a)-(c), respectively. It should be observed that equal distribution of switching commutations is possible only when N_{9L} is a multiple of four. Therefore, swapping of gating signals after every fundamental period should be performed to achieve identical device switching frequency. Also, it should be observed in the last row of Table 2.14 that optimal switching angles correspond to modulation index of given operating point.

Table 2.14: Allocation of optimal switching angles for 9L MLC.
 (a)($m=0.9216$, $N=4$) (b)($m=0.5804$, $N=6$) (c)($m=0.4706$, $N=8$)

Output	Switching Angles (Deg)					N
	0	4.11	11.97	23.13	37.72	
V_{9L}	0	1	2	3	4	4
V_{5L1}	0	0	0	1	2	2
V_{5L2}	0	1	2	2	2	2
V_{3L11}	0	0	0	0	1	1
V_{3L12}	0	0	0	-1	-1	1
V_{3L21}	0	0	1	1	1	1
V_{3L22}	0	-1	-1	-1	-1	1

$$\frac{1}{4} \sum_{i=1}^4 s(i) \cos(\alpha_i) = 0.9215 \approx m$$

(a)

Output	Switching Angles (Deg)							N
	0	28.72	32.33	35.97	46.95	59.29	73.32	
V_{9L}	0	1	0	1	2	3	4	6
V_{5L1}	0	0	0	0	0	1	2	2
V_{5L2}	0	1	0	1	2	2	2	4
V_{3L11}	0	0	0	0	0	0	1	1
V_{3L12}	0	0	0	0	0	-1	-1	1
V_{3L21}	0	0	0	0	1	1	1	1
V_{3L22}	0	-1	0	-1	-1	-1	-1	3

$$\frac{1}{4} \sum_{i=1}^6 s(i) \cos(\alpha_i) = 0.5800 \approx m$$

(b)

Output	Switching Angles (Deg)									N
	0	4.541	9.570	22.670	28.282	32.838	54.362	66.970	84.844	
V_{9L}	0	1	2	3	4	3	2	1	0	8
V_{5L1}	0	0	0	1	2	1	0	0	0	4
V_{5L2}	0	1	2	2	2	2	2	1	0	4
V_{3L11}	0	0	0	0	1	0	0	0	0	2
V_{3L12}	0	0	0	-1	-1	-1	0	0	0	2
V_{3L21}	0	0	1	1	1	1	1	0	0	2
V_{3L22}	0	-1	-1	-1	-1	-1	-1	-1	0	2

$$\frac{1}{4} \sum_{i=1}^8 s(i) \cos(\alpha_i) = 0.4709 \approx m$$

(c)

2.7.3 Experimental Results

The proposed SOP technique has been implemented for controlling cascade 9L inverter feeding a 1.5-kW induction motor. The low power prototype of cascaded 9L inverter for one of three phases is shown in Fig. 2.23. It has been implemented using 3L-NPC modules from Infineon and a six-pack IGBT driver SKHI 61R from Semikron. The gating signals are programmed on a Xilinx Spartan-6 FPGA. The induction motor was supplied with phase voltage of 110 V at 50 Hz operation and thus, the dc-link capacitor voltages should be maintained at 30.56 V based on (2.5). The list of major components along with their parameters are shown in Table 2.15. The output of 9L inverter is directly connected to the induction motor without using any LC filter to get better understanding of dominant harmonics.

The waveforms of output phase-voltage, line-voltage, and stator currents corresponding to operating points ($m=0.9216$, $N=4$), ($m=0.5804$, $N=6$), ($m=0.4706$, $N=8$), and ($m=0.3059$, $N=13$) are shown in Figs. 2.24 (a)-(c) to Figs. 2.27 (a)-(c), respectively. The output phase-voltage con-

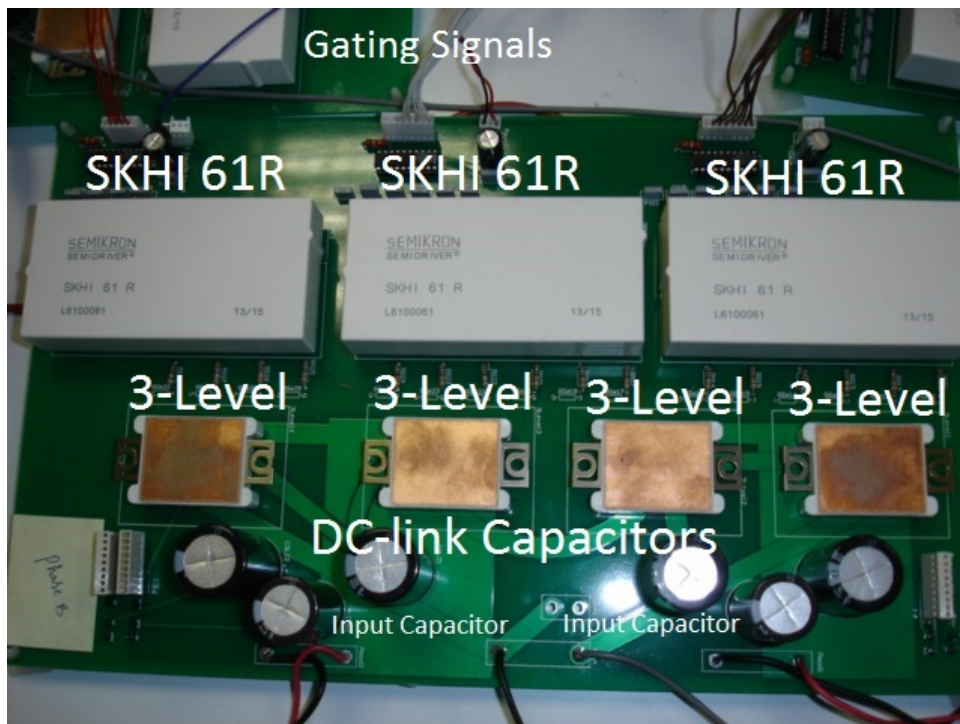


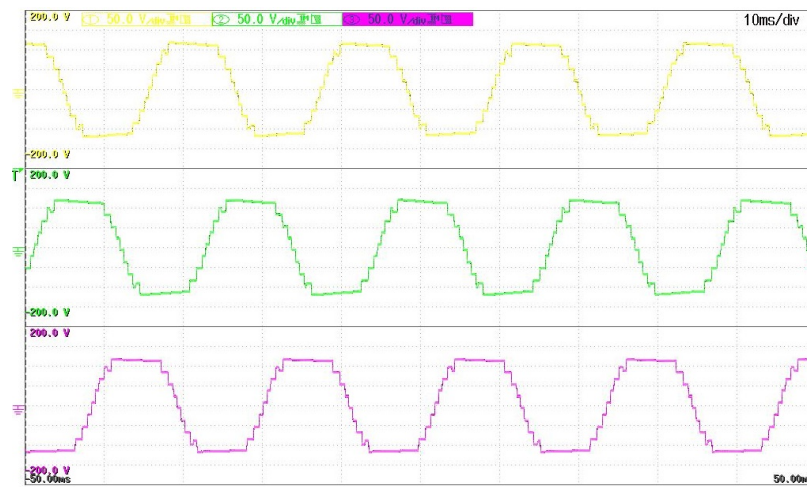
Fig. 2.23: PCB of cascade 9L MLC for one of the three phases

Table 2.15: List of components and their rated parameters for 9L MLC

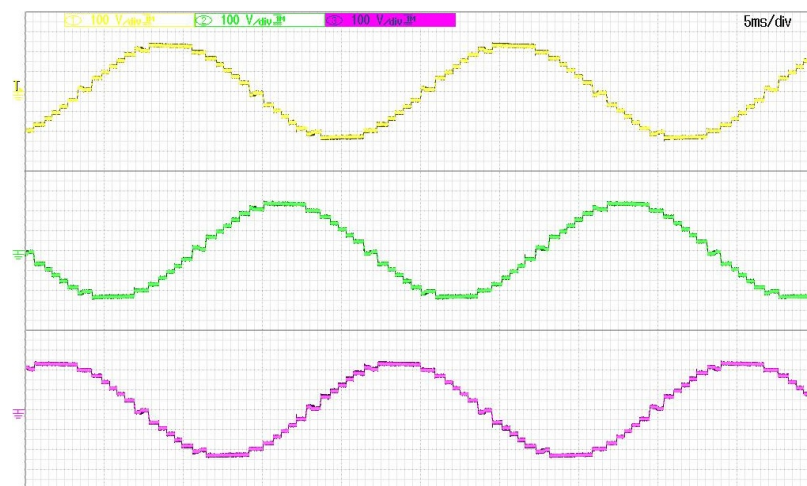
Components	Parameters
Induction Motor	1.5 kW, 400 V, 50 Hz
3L-NPC module	F3L30R06W1E3_B11 $V_{CE} = 600$ V, $I_{C_{nom}} = 30$ A
Sixpack Driver	SKHI 61R $V_{CE} = 900$ V, $f_{max} = 50$ kHz
Dc-link capacitors (C1-C4)	1 mF, 160 V electrolytic

sists of 9 voltage levels, whereas the output line-to-line voltage with 17 levels looks almost sinusoidal. The machine stator currents for four operating points are sinusoidal although device switching frequency is equal to 46.08 Hz, 43.53 Hz, 47.06 Hz, and 49.70 Hz, respectively, due to optimal switching patterns.

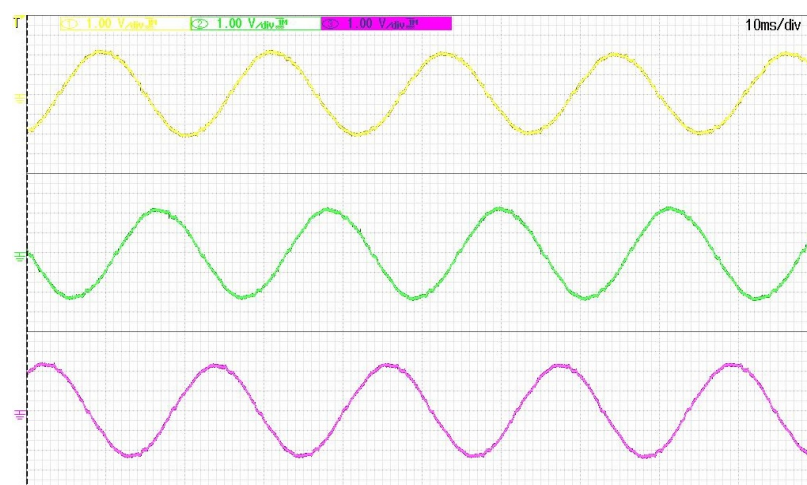
The waveforms of dc-link capacitor voltages and NPP error of two 5L-HNPC inverters for the four operating points are shown in Figs. 2.28 (a)-(d) to Figs. 2.31 (a)-(d), respectively. The ripple in dc-link capacitor voltages depends on the load and switching patterns, as explained in Section 2.7.2.3. Minimum peak-to-peak ripple of 2 volts has been observed in dc-link capacitors C1 to C4 corresponding to operating point ($m=0.9216$, $N=4$), whereas maximum peak-to-peak ripple of 6 volts is observed across dc-link capacitors C3 to C4 corresponding to operating point ($m=0.3059$, $N=13$). Also, it should be observed that average value of NPP error is almost zero, as shown in Figs. 2.28 (c)-(d) to Figs. 2.31 (c)-(d). There exists a small NPP error about 1.26 volts (4% of dc-link voltage) in bottom 5L-HNPC inverter as shown in Fig. 2.27 (d), however, it has not affected the harmonic distortion of output current significantly. However, by swapping switching patterns between two NPC legs of phase B the NPP error can be made approximately zero [117]. The efficiency of inverter is observed to be nearly 97% for the all the four different operating points due to low average device switching frequency ($\leq f_{1R}$).



(a)

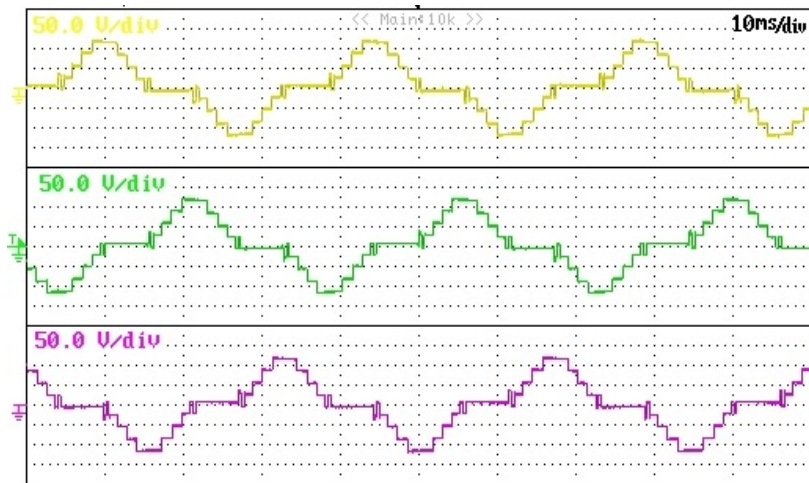


(b)

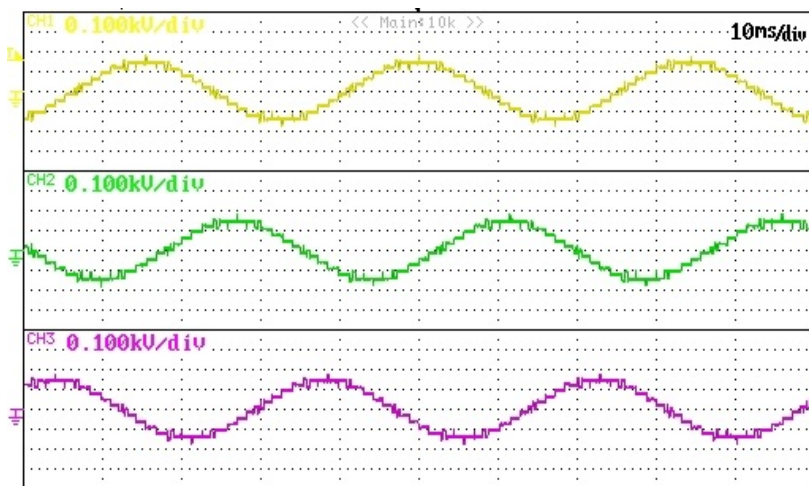


(c)

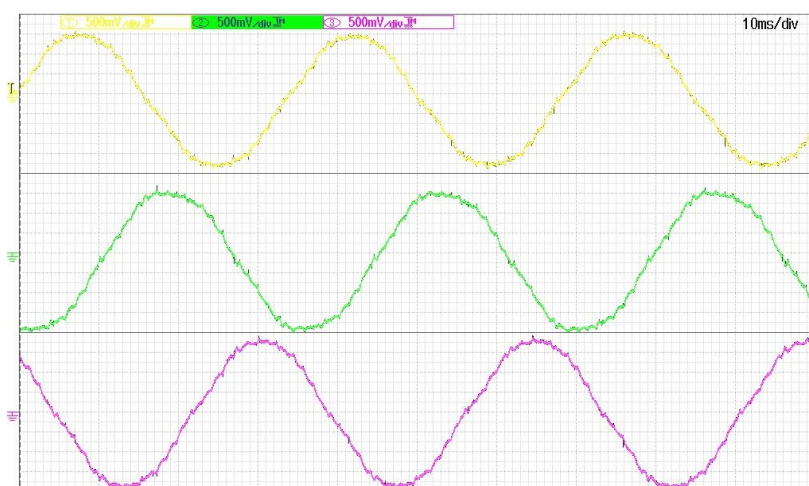
Fig. 2.24: Experimental results of 9L MLC for ($m=0.9216, N=4$). (a) Output phase-voltage (b) Output line-voltage (c) Machine stator currents



(a)

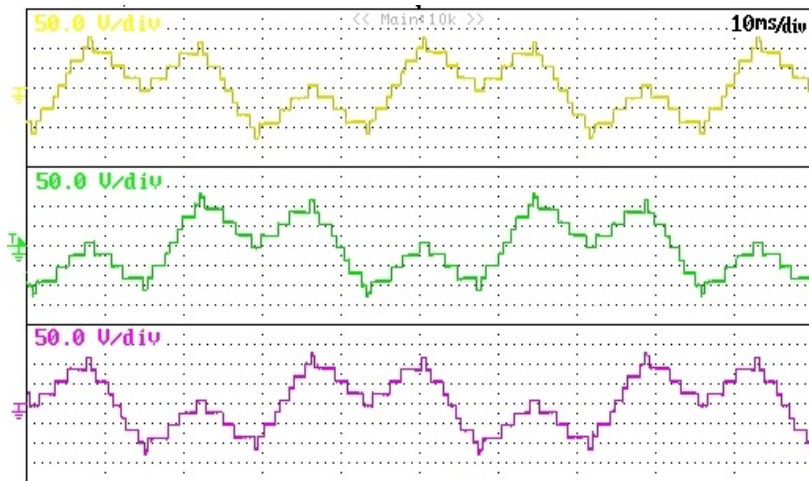


(b)

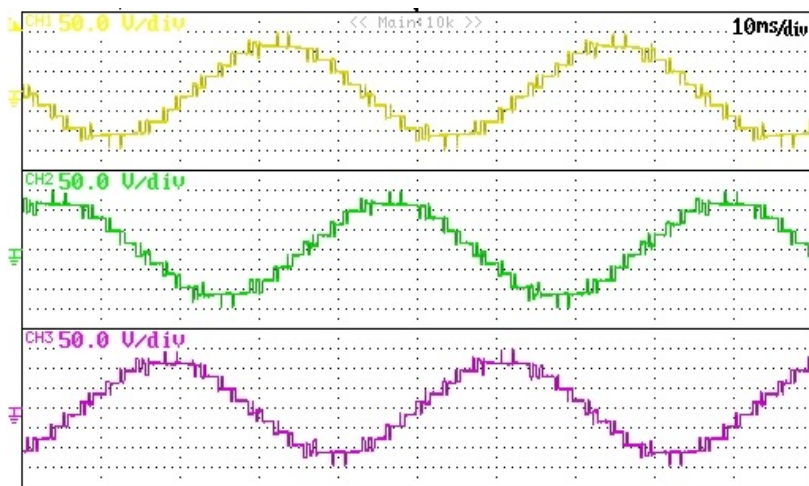


(c)

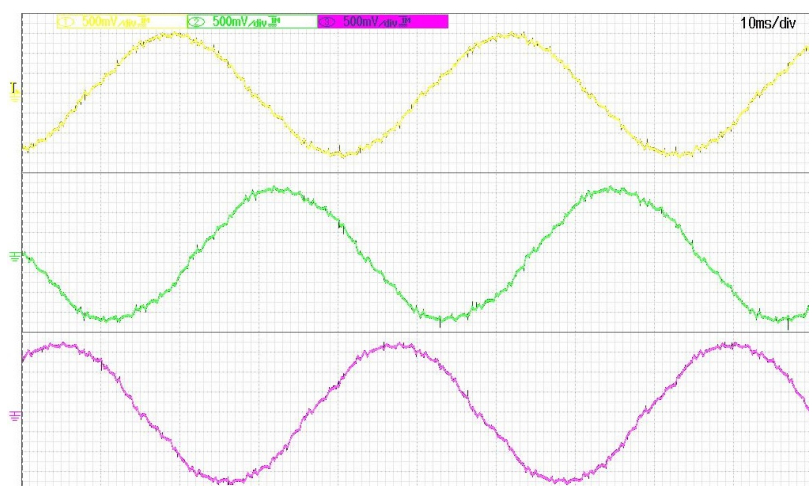
Fig. 2.25: Experimental results of 9L MLC for ($m=0.5804$, $N=6$). (a) Output phase-voltage (b) Output line-voltage (c) Machine stator currents



(a)

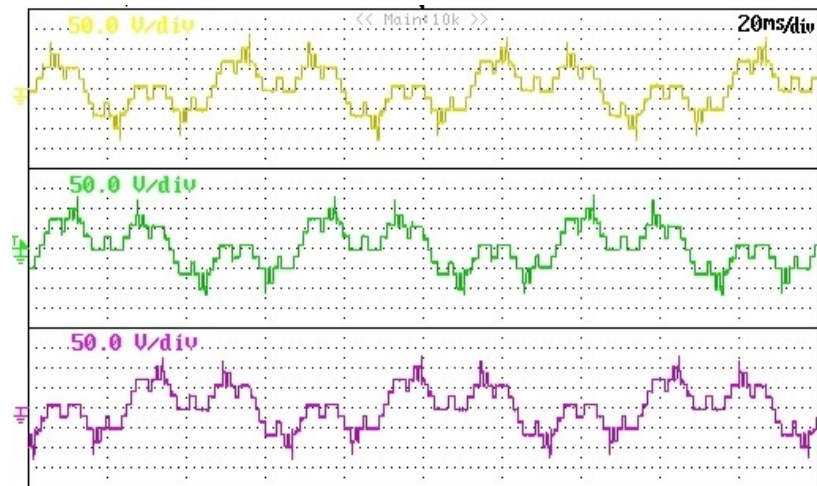


(b)

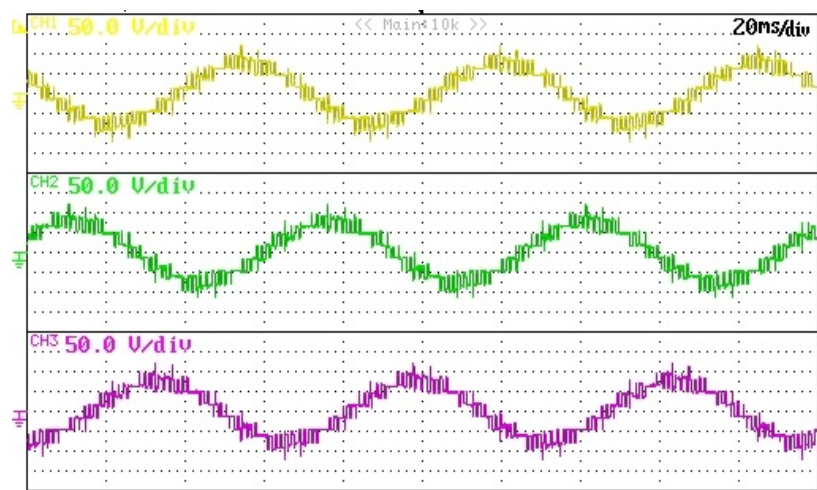


(c)

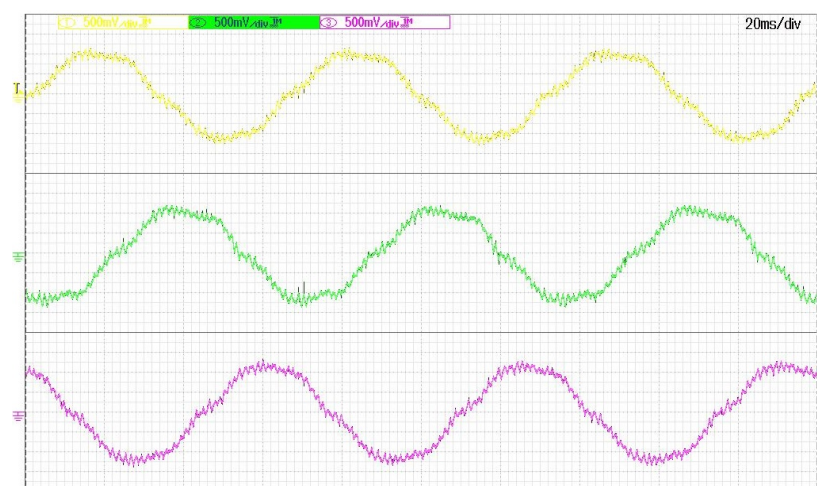
Fig. 2.26: Experimental results of 9L MLC for ($m=0.4706$, $N=8$). (a) Output phase-voltage (b) Output line-voltage (c) Machine stator currents



(a)

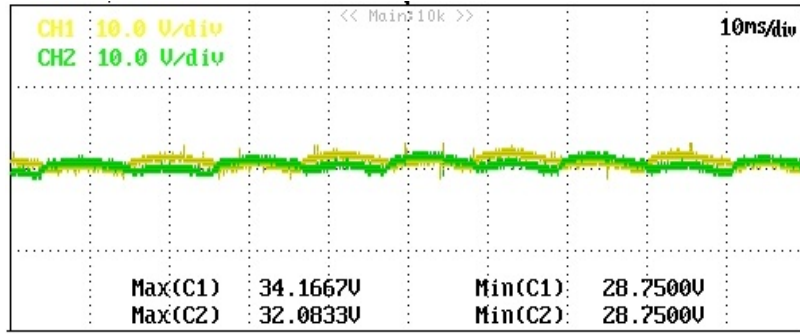


(b)

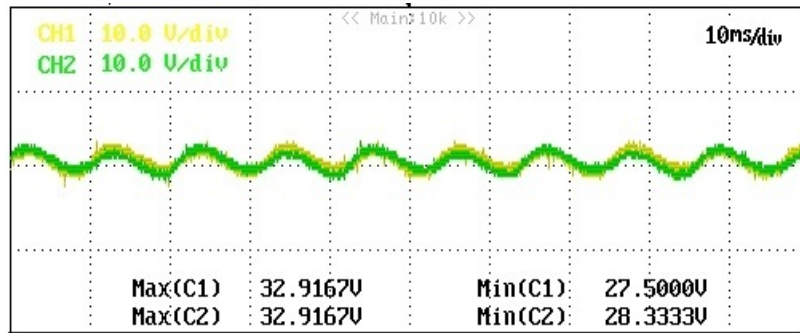


(c)

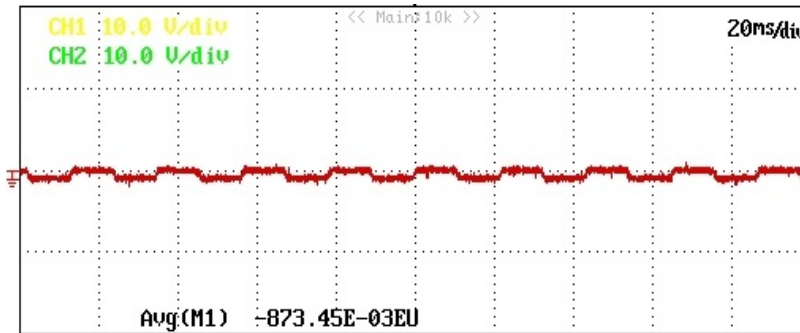
Fig. 2.27: Experimental results of 9L MLC for ($m=0.3059$, $N=13$). (a) Output phase-voltage (b) Output line-voltage (c) Machine stator currents



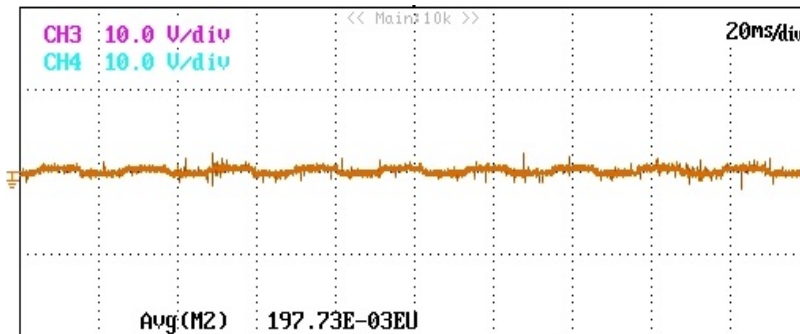
(a)



(b)

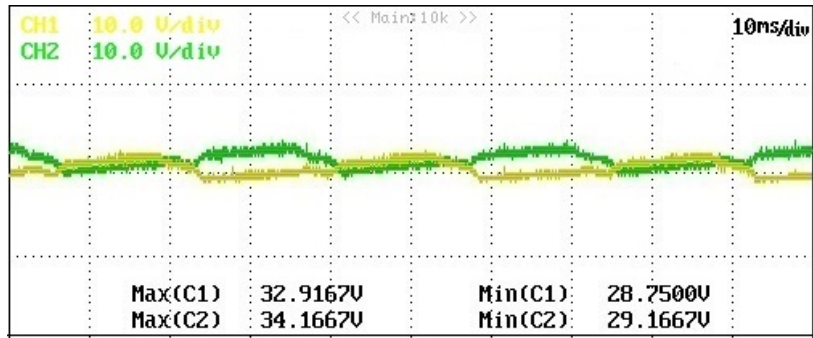


(c)

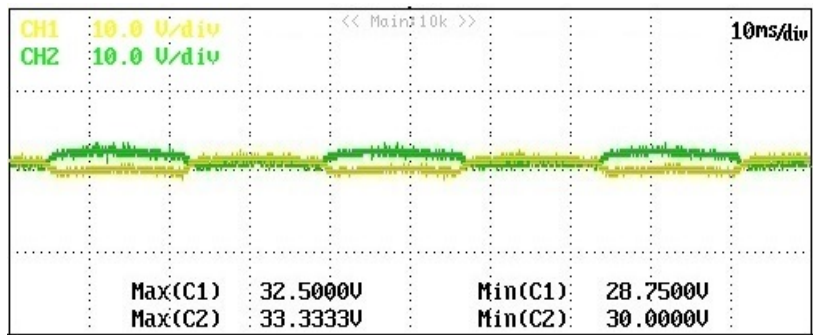


(d)

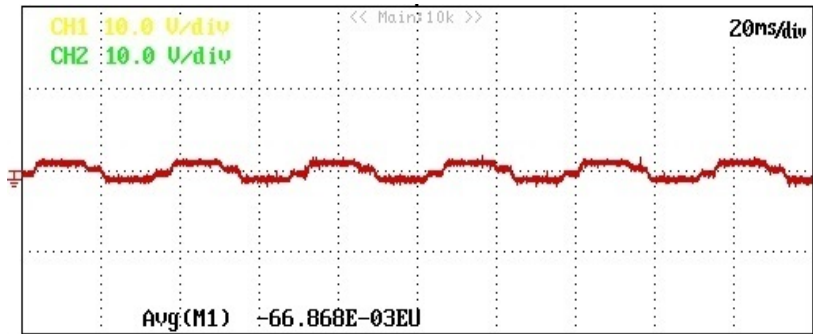
Fig. 2.28: Dc-link capacitor voltages and NPP error of 9L-MLC for ($m=0.9216, N=4$). (a) V_{C1} and V_{C2} (b) V_{C3} and V_{C4} (c) NPP error of top 5L-HNPC inverter (d) NPP error of bottom 5L-HNPC inverter



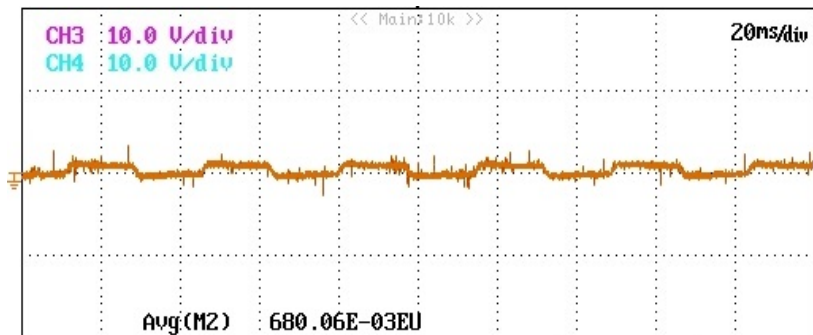
(a)



(b)

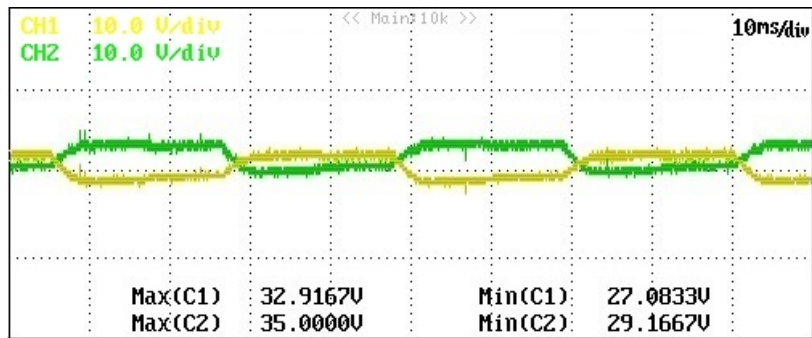


(c)

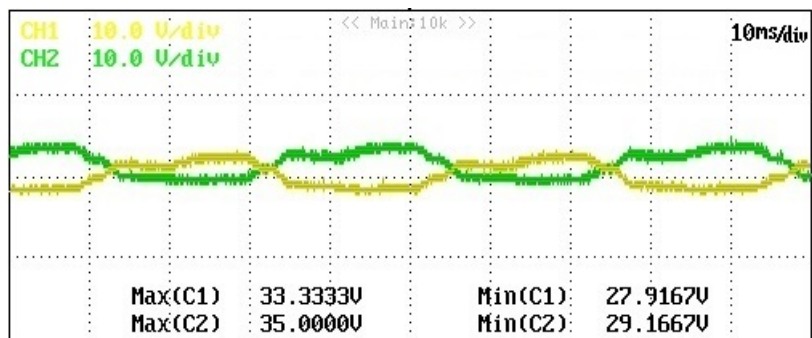


(d)

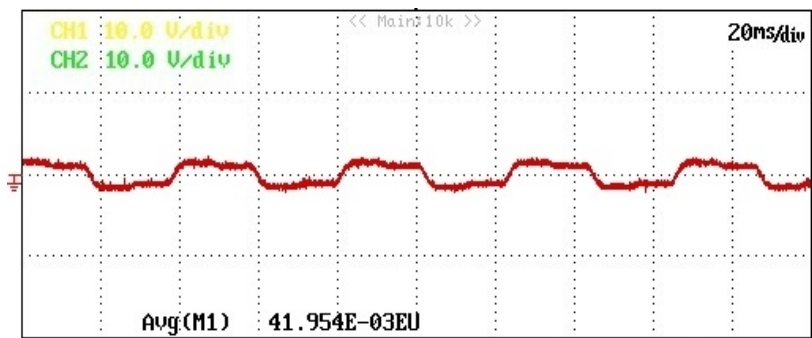
Fig. 2.29: Dc-link capacitor voltages and NPP error of 9L-MLC for ($m=0.5804$, $N=6$). (a) V_{C1} and V_{C2} (b) V_{C3} and V_{C4} (c) NPP error of top 5L-HNPC inverter (d) NPP error of bottom 5L-HNPC inverter



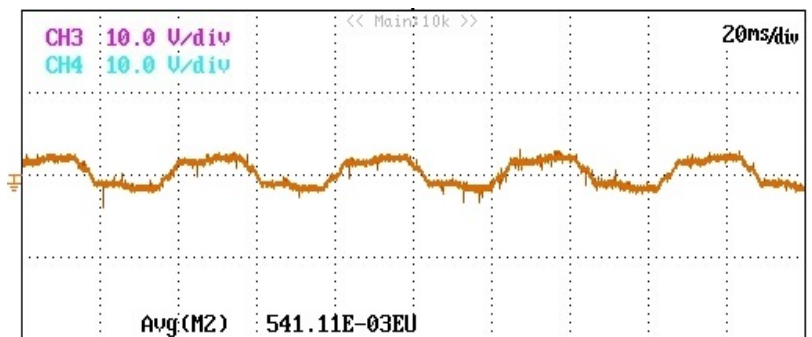
(a)



(b)

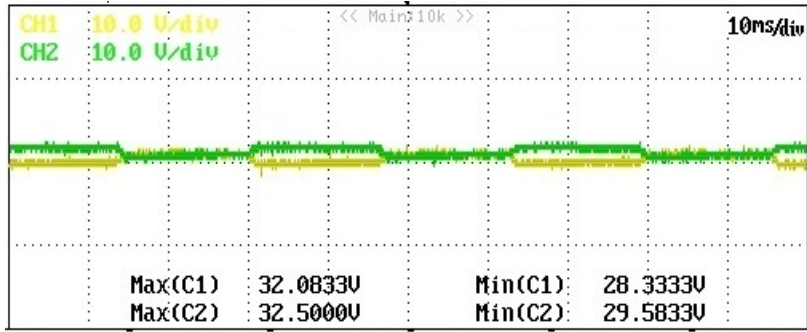


(c)

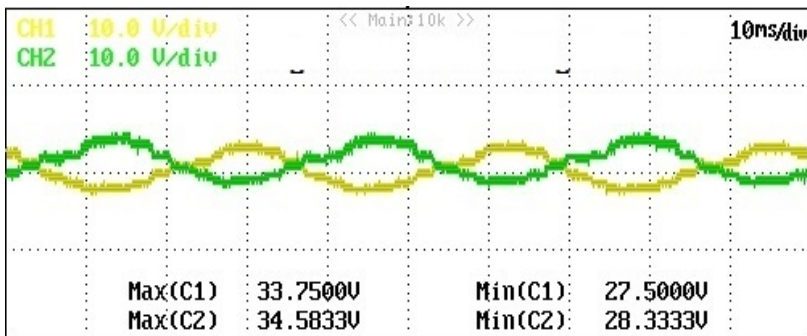


(d)

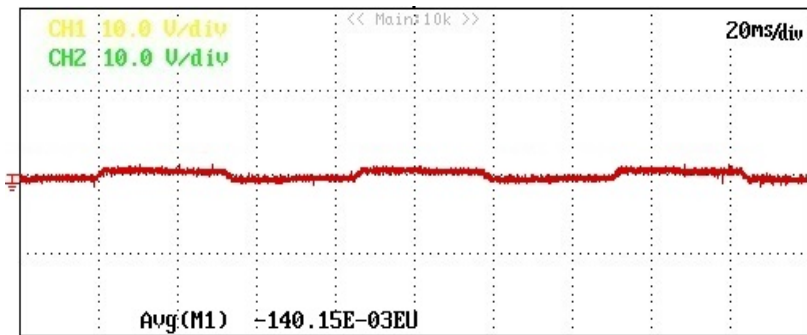
Fig. 2.30: Dc-link capacitor voltages and NPP error of 9L-MLC for ($m=0.4706$, $N=8$). (a) V_{C1} and V_{C2} (b) V_{C3} and V_{C4} (c) NPP error of top 5L-HNPC inverter (d) NPP error of bottom 5L-HNPC inverter



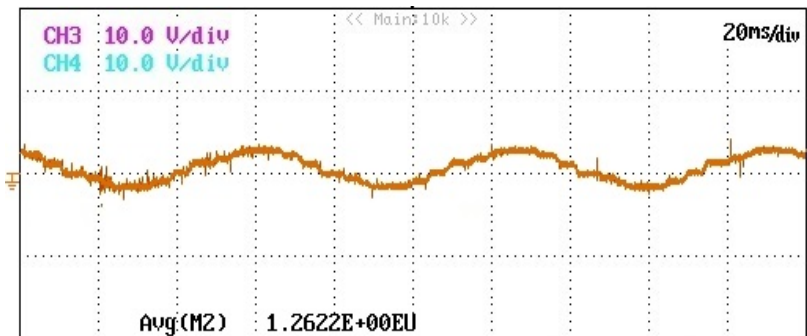
(a)



(b)



(c)



(d)

Fig. 2.31: Dc-link capacitor voltages and NPP error of 9L-MLC for ($m=0.3059, N=13$). (a) V_{C1} and V_{C2} (b) V_{C3} and V_{C4} (c) NPP error of top 5L-HNPC inverter (d) NPP error of bottom 5L-HNPC inverter

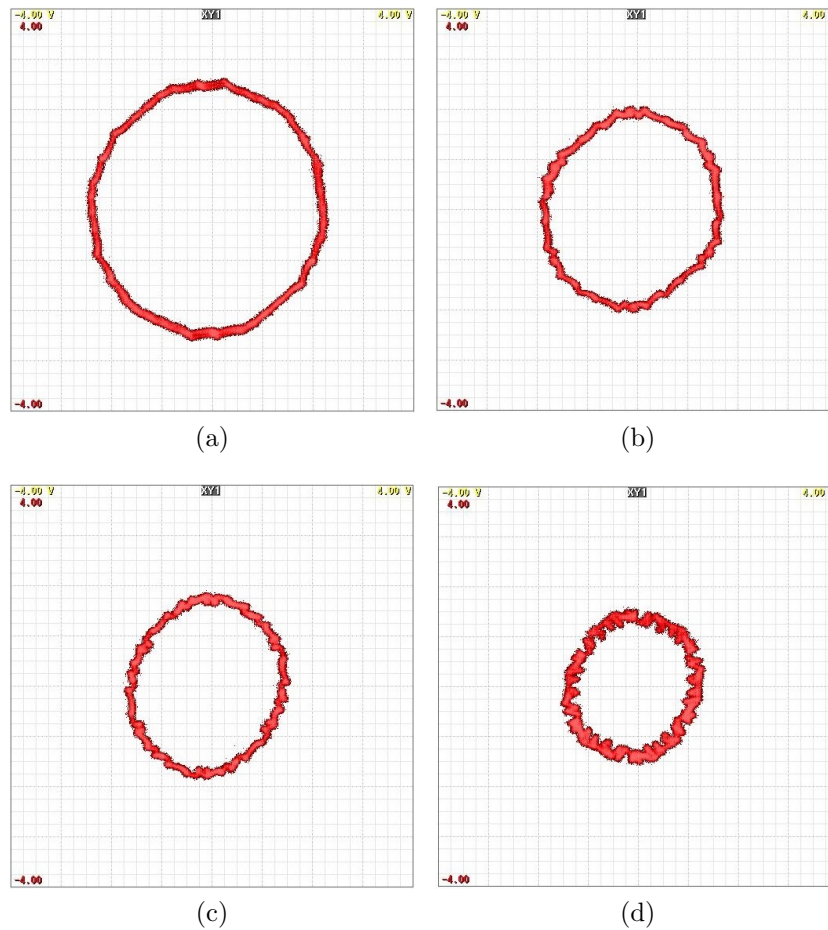
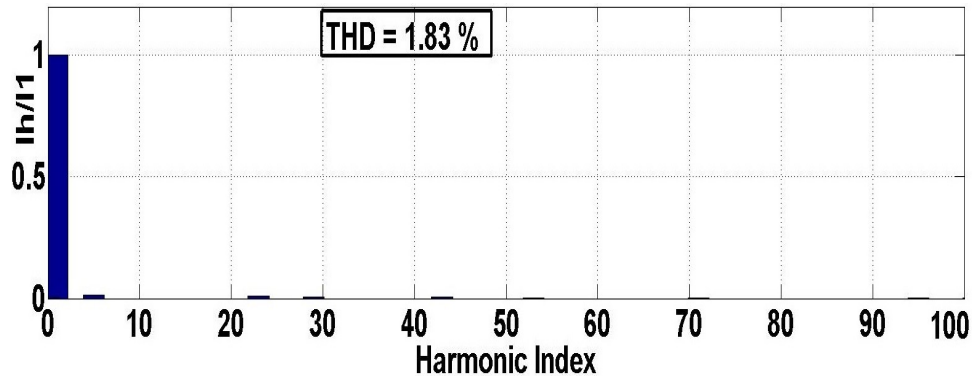


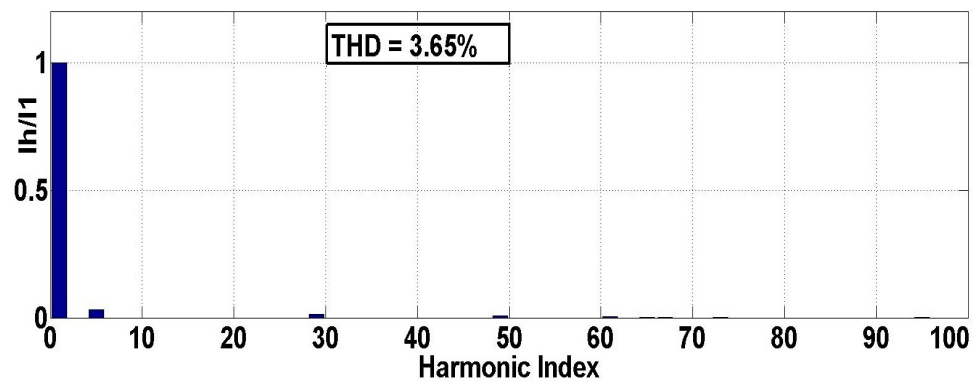
Fig. 2.32: Space vector trajectory of stator currents. (a) ($m=0.9216, N=4$) (b) ($m=0.5804, N=6$) (c) ($m=0.4706, N=8$) (d) ($m=0.3059, N=13$)

The space vector trajectories of machine stator currents for four operating points are shown in Fig. 2.32 (a)-(d), respectively. The circular space vector trajectories indicate very low harmonic distortion at $f_{s,avg} \leq f_{1R}$ due to optimal switching angles. In addition, harmonic analysis has been done on recorded stator currents. The values of THD between 2-5% for all operating points as shown in Fig. 2.32 (a)-(d) demonstrate the effectiveness of SOP technique.

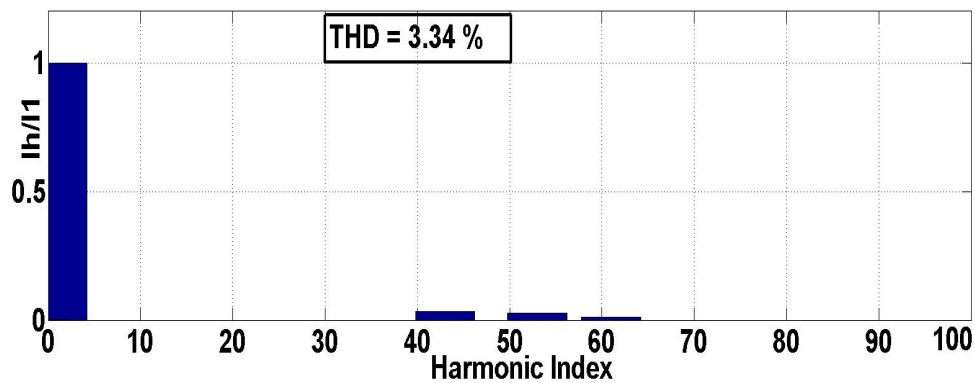
For operating point ($m=0.4706, N=8$), pulse number for all 3L-NPC inverters is obtained as 2 from Table 2.14 (b) and hence, switching frequency of all power semiconductor devices should be equal to $2f_1 (< f_{1R})$. This can be confirmed from the gating signals of semiconductor devices S1, S5, S9 and S13, as shown in Fig. 2.34.



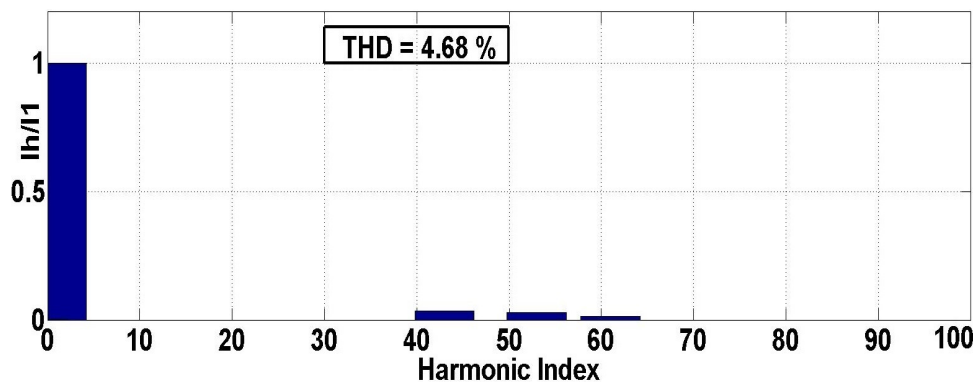
(a)



(b)



(c)



(d)

Fig. 2.33: FFT harmonic spectrum of machine stator current of phase A

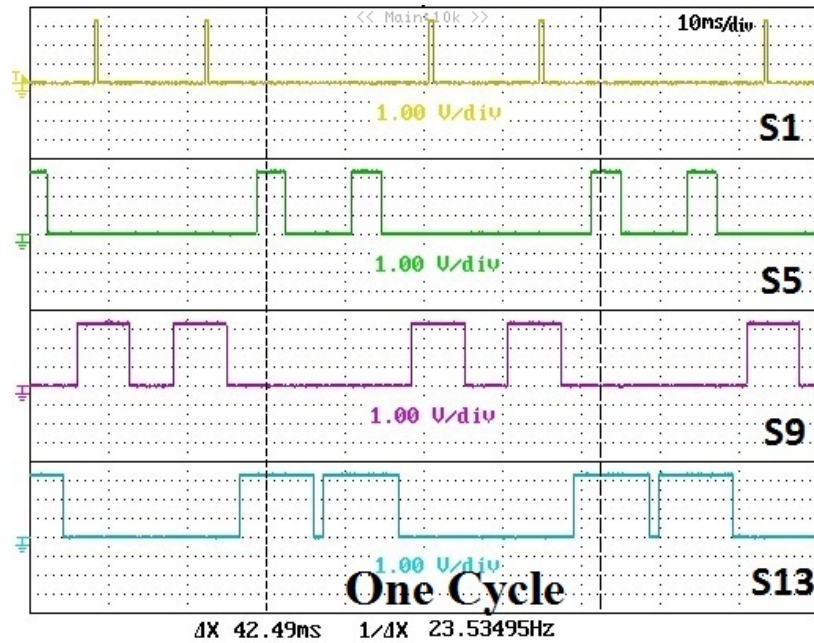


Fig. 2.34: Gating signals of semiconductor devices S1, S5, S9 and S13

2.7.4 Performance Comparison

The aim of this section is to compare the performance of the proposed SOP technique with level-shift SPWM for 9L MLC. The device switching frequency has been set at 500 Hz for level-shift SPWM in order to achieve the good quality of inverter output currents. The performance comparison in terms of various losses and efficiency is shown in Table 2.16. As expected, the switching losses with proposed SOP technique are much lower than level-shift SPWM that employs ten times higher device switching frequency. Therefore, reduced switching losses in SOP technique leads to lower cooling system requirements as well as higher device utilization. Also, the overall efficiency of drive system is slightly higher with proposed SOP technique. The difference in efficiency appears to be small but this will lead to saving of several kW of power in case of MV high power drives. Therefore, energy and cost savings will be huge in a long term perspective. To conclude, the proposed SOP technique achieves better system performance compared to standard level-shift SPWM technique.

Table 2.16: Performance comparison between proposed SOP and level-shift SPWM for 9L MLC

	SOP	level-shift SPWM
Dc input power	1.2584 MW	1.2584 MW
Switching losses	96.5 W	1247 W
Conduction losses	4052 W	3821 W
Total device losses	4148.5 W	5068 W
Drive output power	1.2357 MW	1.2319 MW
Overall efficiency	97.88 %	97.5 %

2.8 Summary and Conclusions

In this Chapter, SOP technique has been analyzed and divided into three steps : estimation of pulse number N , optimization of switching angles and allocation of optimal switching angles to each power semiconductor device. First and last steps in SOP technique are dependent on the converter topology, whereas second step in SOP technique is independent of converter topology. A systematic analysis has been presented for the last step of SOP technique to allocate optimal switching angles to each power semiconductor device. One of the main criteria to allocate optimal switching angles is to achieve identical device switching frequency. In addition, there might be other topology requirements such as capacitor voltage balancing, minimization of capacitor voltage ripple and so on. The developed analysis has been utilized to modulate 7L and 9L MLCs with $f_{s,avg} = f_{1R}$ and it has been demonstrated with low power prototypes of cascaded 7L and 9L MLCs.

Chapter 3

Modified Generalized SOP Technique

3.1 Introduction

This Chapter gives the details of proposed modified SOP technique for classical MLC topologies and its implementation details for 7L and 9L MLCs. As explained in the previous Chapter, classical MLC topologies such as NPC, FC, CHB, and HNPC topologies share a common feature that an nL -MLC consists of $0.5*(n-1)$ sub-converters such as H-Bridge or 3L-NPC in each phase. Generalized SOP technique determines optimal switching angles for nL -MLC for all steady-state operating points (m,N) . These optimal switching patterns should be assigned to each sub-converter in order to achieve identical switching frequency and also satisfy the topology requirements such as capacitor voltage balance, minimized capacitor voltage ripple, and so on. However, switching transitions in an nL waveform may not be equally distributed among sub-converters if pulse number N is not an integer multiple of $0.5*(n-1)$. Thus, it is not possible to achieve $f_s \leq f_{s,max}$. Also, power semiconductor devices operate at different device switching frequency, which lead to unequal device switching losses and thermal loading. Therefore, generalized SOP technique should be enhanced to limit the device switching frequency to desired $f_{s,max}$ and also to achieve identical device switching frequency.

One major application of MV drives is in low performance drives such as industrial fans, centrifugal pumps, and blowers. They are usually operated at higher modulation index range ($m > 0.5$) in open-loop v/f control mode [131]. For such drives, the stator voltage is adjusted in proportion to the fundamental frequency with gradient limited reference input [125]. Due to open-loop operation, it is important to reduce the transients in machine currents. Two scenarios which lead to large transients in machine currents are switching between operating points of different N and switching between operating points of same N but with large discontinuities in switching angles [124]. By utilizing post-optimization, it is possible to remove large discontinuities in switching angles for consecutive modulation index values as explained in Section 2.4.2. However, generalized SOP technique leads to operation of MLC with multiple pulse numbers at higher modulation index range ($m > 0.5$) as shown in Figs. 2.9 and 2.21 and hence, it leads to transients in machine currents [122]. Therefore, generalized SOP technique should be enhanced to eliminate transients in machine currents at higher modulation index values.

The objectives of the proposed modified SOP technique are as follows: (1) limit the device switching frequency to desired $f_{s,max}$, (2) achieve identical device switching frequency, (3) eliminate transients in machine currents at higher modulation index values, and (4) achieve low harmonic distortion in machine stator currents, while satisfying other topology requirements such as minimum voltage ripple in dc-link capacitors.

This Chapter is organized as follows: details of proposed modified SOP technique are given in Section 3.2, implementation details of proposed modified SOP technique for 7L and 9L MLCs are given in Section 3.3 and 3.4, respectively, and the conclusions of this chapter are given in Section 3.5.

3.2 Modified Generalized SOP

The complete details of generalized SOP technique are presented in Section 2.2. In principle, it involves three steps: (1) estimation of pulse number N in order to limit the device switching frequency to $f_{s,max}$, (2) optimization to pre-determine switching angles for each steady-state operating point (m,N) to minimize the harmonic distortion of converter output current, and (3) allocate optimal switching angles to each power semiconductor device. The proposed SOP technique modifies the first step of generalized SOP technique in order to achieve desired objectives as mentioned in Section 3.1. Complete details are given next.

3.2.1 New method for estimation of N

The goal is to operate MLC with identical device switching frequency that is limited to desired $f_{s,max}$. The generalized SOP technique utilizes top-down approach by estimating pulse number of nL waveform to achieve desired $f_{s,max}$ and then switching commutations are distributed among constituent 3L sub-converters. Some issues with this approach in case of five or higher-level MLCs are unequal device switching frequency, unable to limit device switching frequency to desired $f_{s,max}$, and varying pulse number at higher modulation index values. These issues can be solved by using bottom-up approach rather than top-down approach.

The basic idea is to select pulse number N_{3L} for each 3L sub-converter such that device switching frequency is limited to $f_{s,max}$ for all steady-state operating points (m,N) . Then, it naturally leads to identical device switching frequency that is limited to $f_{s,max}$. The device switching frequency of a 3L sub-converter operating at steady-state operating point (m,N_{3L}) should be equal to $N_{3L} * m * f_{1R}$. Then, the value of N_{3L} such that device switching

frequency is limited to $f_{s,max}$ is obtained as,

$$N_{3L} = \text{floor} \left(\frac{f_{s,max}}{f_1} \right) = \text{floor} \left(\frac{f_{s,max}}{m \cdot f_{1R}} \right) \quad (3.1)$$

It has already been established that generalized SOP technique can operate 7L and 9L MLCs at $f_{s,max} = f_{1R}$, while maintaining the quality of converter output currents. The same criteria will be adopted for proposed modified SOP technique. For each discrete value of m , the estimated value of N_{3L} such that $f_{s,max} = f_{1R}$ is shown in Table 3.1. It should be observed that device switching frequency is limited to f_{1R} for each value of m .

As explained previously, classical nL -MLC consists of $0.5 \cdot (n-1)$ sub-converters in each phase. For example, 7L MLC topology consists of two 3L-NPC converters plus an H-Bridge and 9L MLC topology consists of four 3L-NPC converters as shown in Figs. 2.8 and 2.20, respectively. A switching transition at the output voltage of a 7L inverter is owing to switching transition in one of three 3L sub-converters (3L-NPC or H-Bridge)

Table 3.1: N_{3L} and f_s for a given m to achieve $f_{s,max} = f_{1R}$

m	$f_1(\text{Hz})$	N_{3L}	$f_s(\text{Hz})$
0.501 - 1	25.05 - 50	1	25.05 - 50
0.334 - 0.5	16.7 to 25	2	33.40 - 50
0.251 - 0.333	12.55 to 16.66	3	37.65 - 50

Table 3.2: N_{7L} and f_s for a given m to achieve $f_{s,max} = f_{1R}$

m	N_{3L1}	N_{3L2}	N_{HB}	N_{7L}	$f_s(\text{Hz})$
0.501 - 1	1	1	1	3	25.05 - 50
0.334 - 0.5	2	2	2	6	33.40 - 50
0.251 - 0.333	3	3	3	9	37.65 - 50

Table 3.3: N_{9L} and f_s for a given m to achieve $f_{s,max} = f_{1R}$

m	$f_1(\text{Hz})$	$N_{3L(1-4)}$	N_{9L}	$f_s(\text{Hz})$
0.501 - 1	25.05 - 50	1	4	25.05 - 50
0.334 - 0.5	16.70 - 25	2	8	33.40 - 50
0.251 - 0.333	12.55 - 16.66	3	12	37.65 - 50

and hence, total switching transitions in a 7L waveform N_{7L} should be equal to sum of switching transitions in all three 3L sub-converters, i.e., $N_{3L1}+N_{3L2}+N_{HB}$. Similarly, value of N_{9L} for a 9L MLC topology shown in Fig. 2.20 should be equal to $4*N_{3L}$. For a given value of m , the estimated values of pulse number for 7L and 9L MLCs to achieve $f_{s,max} = f_{1R}$ are shown in Table 3.2 and 3.3, respectively.

The performance comparison between proposed and generalized SOP methods in terms of device switching frequency for 7L and 9L MLCs is shown in Fig. 3.1 (a)-(b), respectively. For 7L MLC, it should be observed in Fig. 3.1 (a) that both proposed and generalized SOP techniques achieve $f_{s,max}=f_{1R}$ but proposed method leads to lower f_s when N_{7L} is a not multiple of three. For 9L MLC, both proposed and generalized SOP techniques achieve $f_{s,max}=f_{1R}$ but the proposed method operates MLC at lower f_s when N_{9L} is not an integer multiple of four. Also, it should be observed at higher values of modulation index ($m > 0.5$) that proposed SOP technique maintains same pulse number, i.e., $N=3$ for 7L MLC and $N = 4$ for

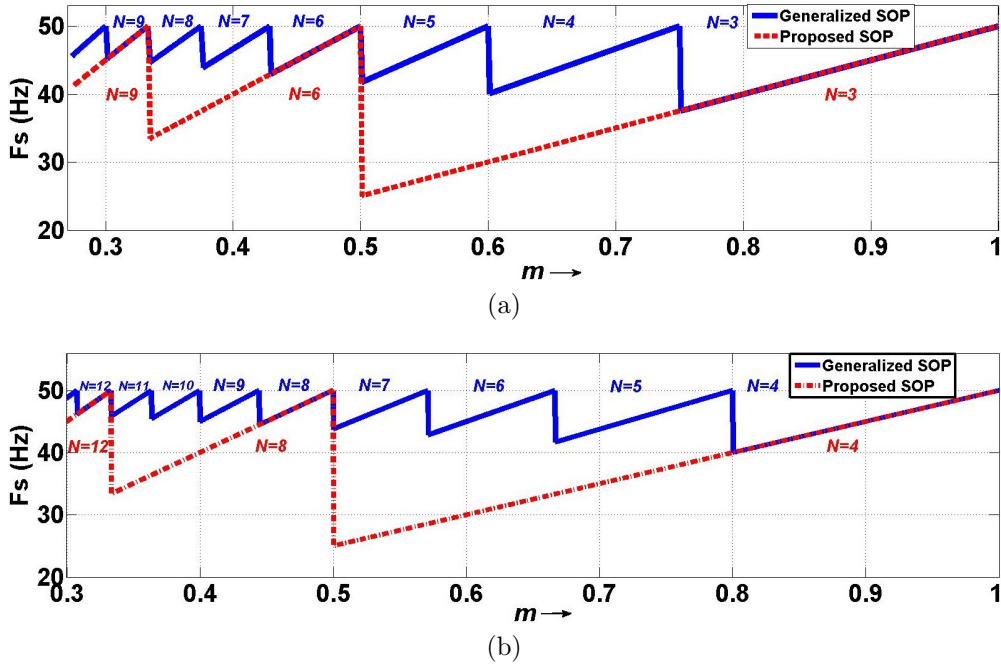


Fig. 3.1: Performance comparison between proposed and generalized SOP methods in terms of f_s with $f_{s,max}=f_{1R}$: (a) 7L MLC (b) 9L MLC

9L MLC, whereas generalized SOP technique leads to operation of MLC with multiple pulse numbers. Therefore, it is expected that transients in machine currents will be reduced at higher modulation index range with proposed SOP technique [122].

3.2.2 Optimization Results

The next step in SOP technique is to perform optimization to determine switching angles for each steady-state operating point (m, N) , which minimize harmonic distortion of machine stator currents. The procedure for optimization algorithm remains the same as presented in Section 2.4. The performance comparison between proposed SOP technique and generalized SOP technique in terms of d for 7L and 9L MLCs with $f_{s,max} = f_{1R}$ is shown in Fig. 3.2 (a)-(b), respectively. It should be noted that performance of proposed method is quite similar to generalized SOP method, although proposed method operates power semiconductor devices at lower device switching frequency.

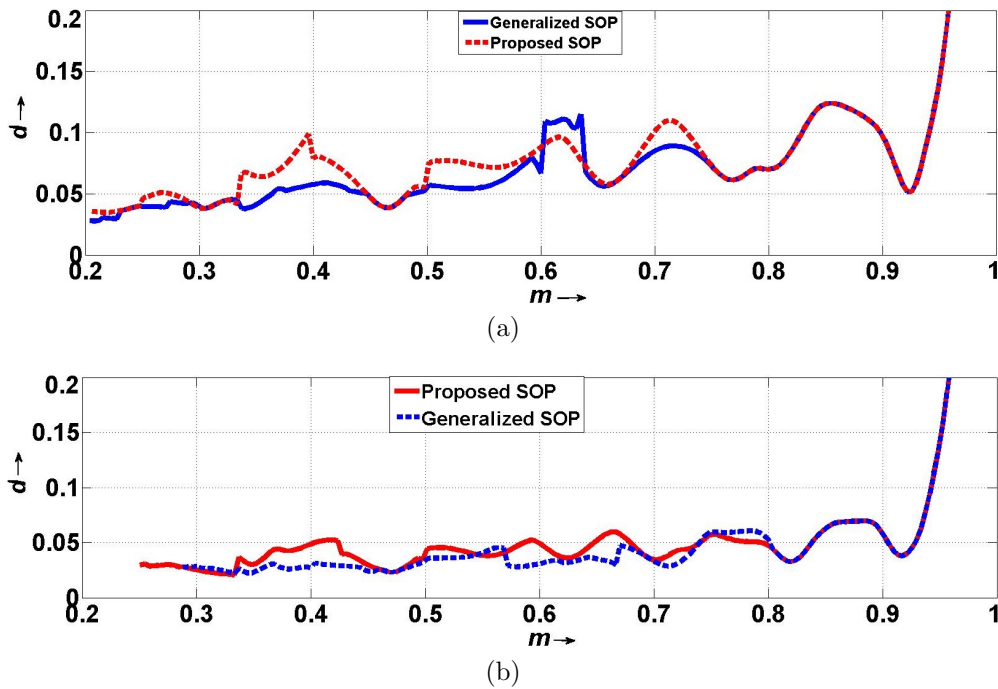
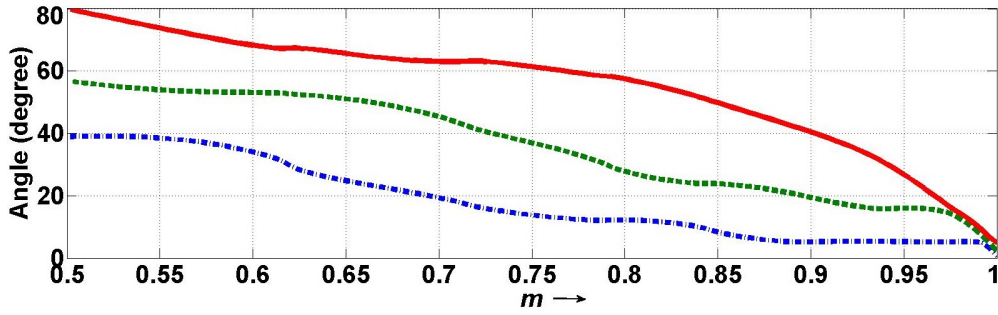
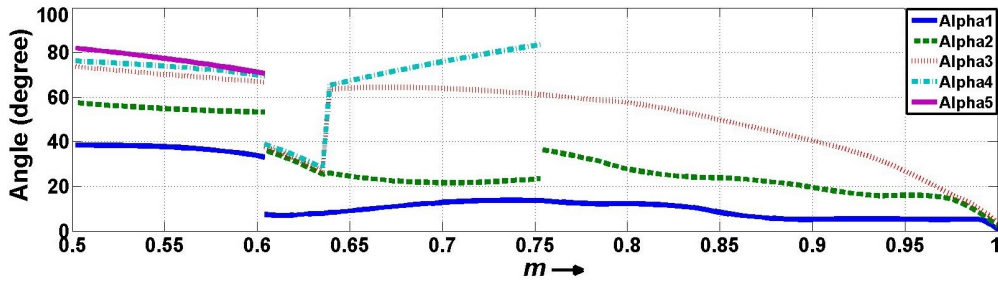


Fig. 3.2: Performance comparison between generalized and proposed SOP techniques in terms of d with $f_{s,max} = f_{1R}$: (a) 7L MLC (b) 9L MLC

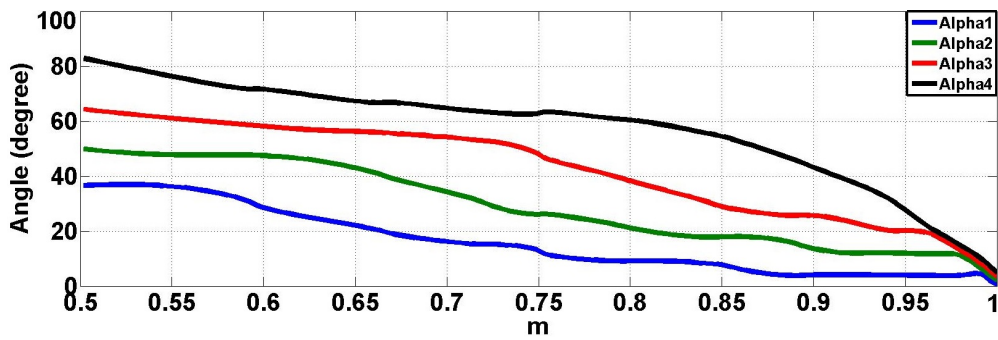


(a)

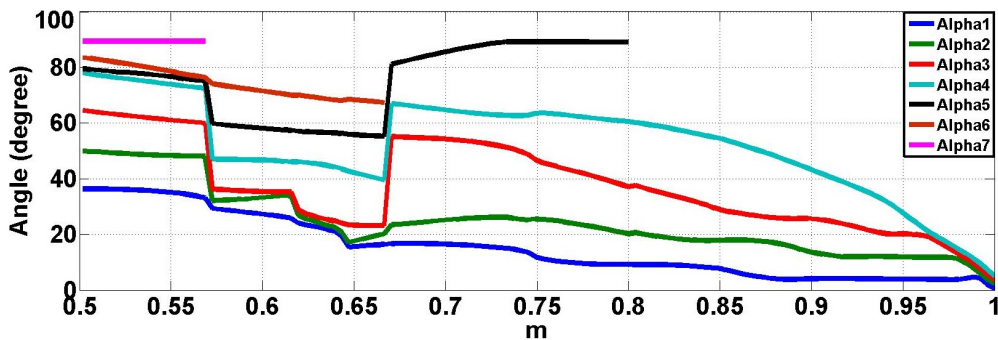


(b)

Fig. 3.3: Optimal switching angles of 7L MLC with $f_{s,max}=f_{1R}$. (a) proposed SOP method (b) generalized SOP method



(a)



(b)

Fig. 3.4: Optimal switching angles of 9L MLC with $f_{s,max}=f_{1R}$. (a) proposed SOP method (b) generalized SOP method

The optimal switching angles of 7L MLC and 9L MLC at $m > 0.5$ with proposed and generalized SOP techniques are shown in Figs. 3.3 (a)-(b) and Figs. 3.4 (a)-(b), respectively. The continuity of optimal switching angles can be seen for the given modulation index range with the proposed SOP technique. On the other hand, discontinuities in the optimal switching angles can be seen in case of generalized SOP technique. Therefore, it is expected that proposed SOP technique ensures smooth operation of drive by reducing the transients in machine currents.

3.3 Experimental Results for 7L MLC

The proposed modified SOP technique has been implemented for 7L MLC with $f_{s,max} = f_{1R}$. The experimental set-up is similar to one given in Section 2.6.3. The dc input voltages to H-Bridge and 5L-HNPC inverter were maintained at 40 V and 80 V, respectively. To demonstrate the performance of proposed modified SOP technique, four different operating points ($m=0.9294, N=3$), ($m=0.6824, N=3$), ($m=0.4824, N=6$), and ($m=0.3294, N=9$) have been selected. The switching angles determined using optimization algorithm have been stored in an FPGA controller. The optimal switching angles and their corresponding distribution of switching transitions among constituents 3L-NPC and H-Bridge converters for the four operating points are shown in Table 3.4 (a)-(d), respectively. It should be observed that constituent H-Bridge and 3L-NPC converters have identical device switching transitions.

Because the 7L topology consists of two 3L-NPC inverters, the dc-link capacitor voltage balancing and ripple is an important concern. It has been considered while assigning the switching angles to each semiconductor device. The procedure to allocate switching angles is same as that presented in Section 2.6.2.3. Owing to higher degrees of freedom, there exists several

Table 3.4: Optimal switching angles and distribution of N for 7L-MLC.
 (a) ($m=0.9294$, $N=3$) (b) ($m=0.6824$, $N=3$) (c) ($m=0.4824$, $N=6$) (d)
 ($m=0.3294$, $N=9$)

Optimal Angles (degree)					
Output	0	5.32	16.04	33.75	N
V_{7L}	0	1	2	3	3
V_{5L}	0	1	2	2	2
V_{HB}	0	0	0	1	1
V_{3L1}	0	0	1	1	1
V_{3L2}	0	-1	-1	-1	1

(a)

Optimal Angles (degree)					
Output	0	21.32	47.88	63.58	N
V_{7L}	0	1	2	3	3
V_{5L}	0	1	2	2	2
V_{HB}	0	0	0	1	1
V_{3L1}	0	0	1	1	1
V_{3L2}	0	-1	-1	-1	1

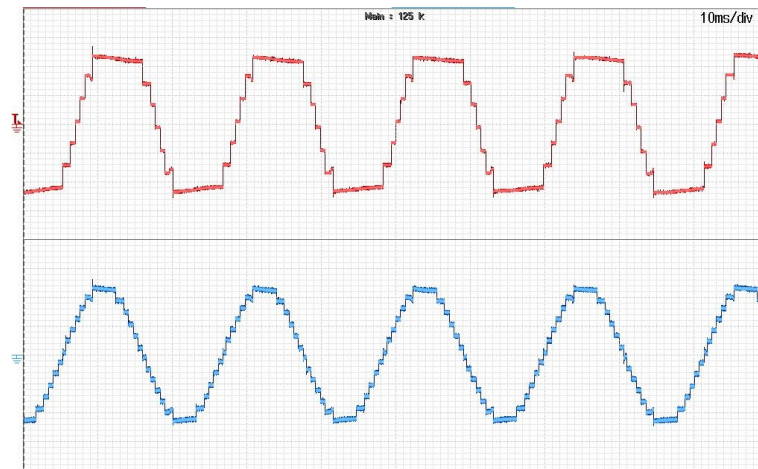
(b)

Optimal Angles (degree)								
Output	0	3.27	18.92	26.06	36.6	61.88	83.02	N
V_{7L}	0	1	2	3	2	1	0	6
V_{5L}	0	0	1	2	1	0	0	4
V_{HB}	0	1	1	1	1	1	0	2
V_{3L1}	0	0	1	1	0	0	0	2
V_{3L2}	0	-1	-1	-1	-1	-1	0	2

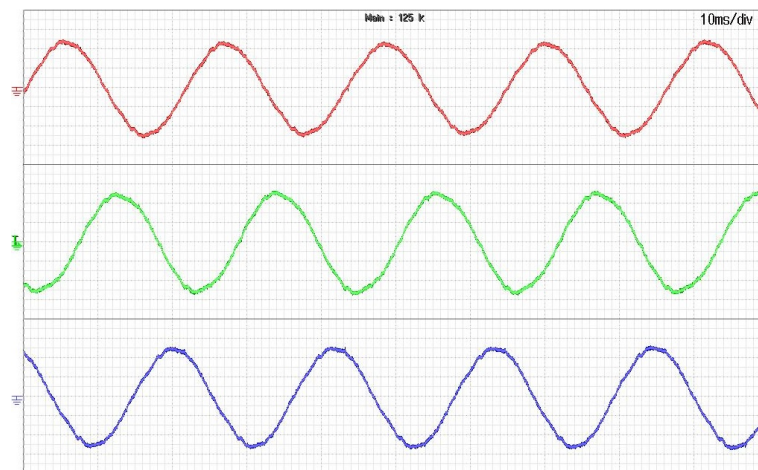
(c)

Optimal Angles (degree)											
Output	0	5.33	18.25	21.88	46.87	47.46	48.05	53.91	67.8	73.15	N
V_{7L}	0	1	0	1	2	3	2	1	0	1	9
V_{5L}	0	1	0	0	1	2	1	0	0	0	6
V_{HB}	0	0	0	1	1	1	1	1	0	1	3
V_{3L1}	0	1	0	0	1	1	1	1	1	1	3
V_{3L2}	0	0	0	0	0	-1	0	1	1	1	3

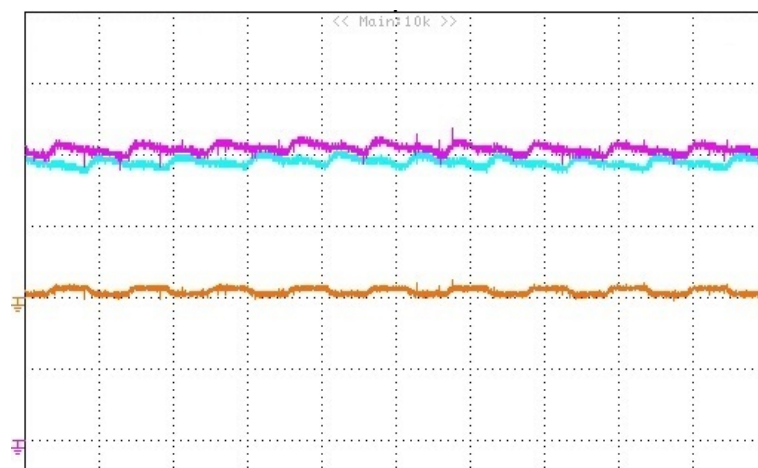
(d)



(a)

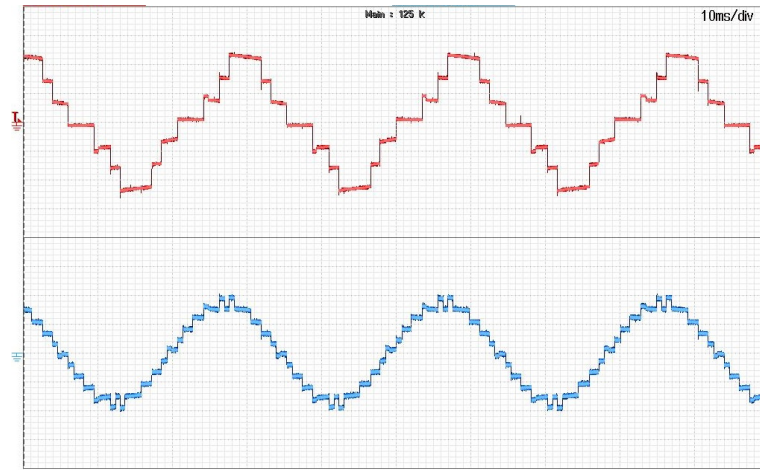


(b)

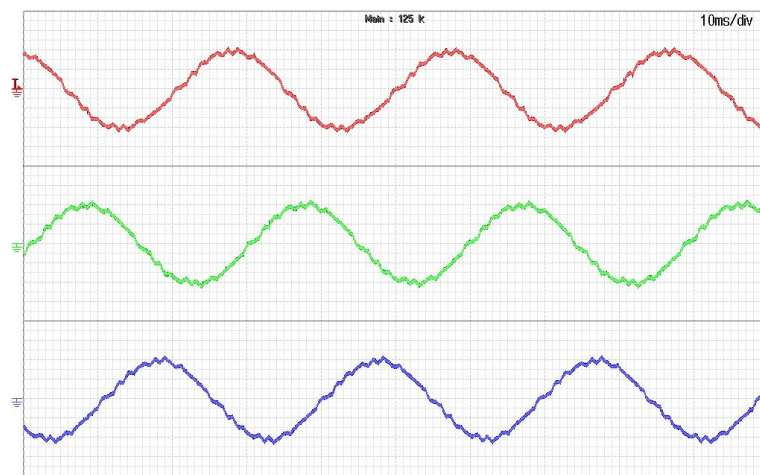


(c)

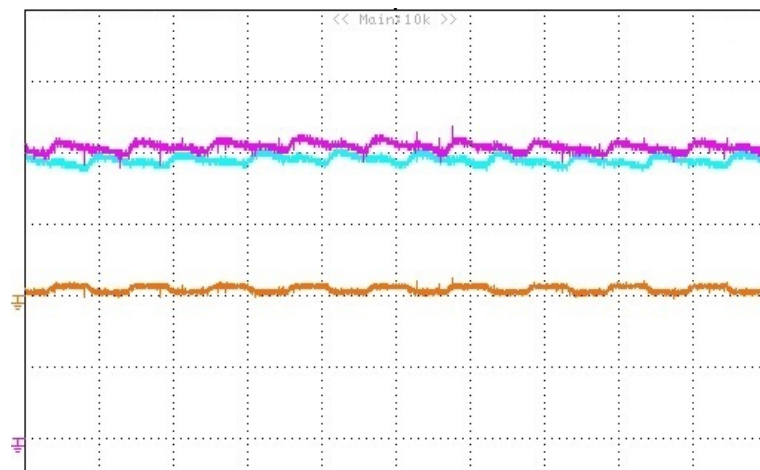
Fig. 3.5: Experimental results of 7L MLC for ($m=0.9294$, $N=3$). X-axis: 10 ms/div. (a) phase and line voltages (Y-axis: 50 V/div, 100 V/div) (b) machine stator currents (Y-axis: 1 A/div) (c) DC-link capacitor voltages and NPP error of 5L-HNPC inverter (X-axis:20 ms/div, Y-axis:10 V/div)



(a)

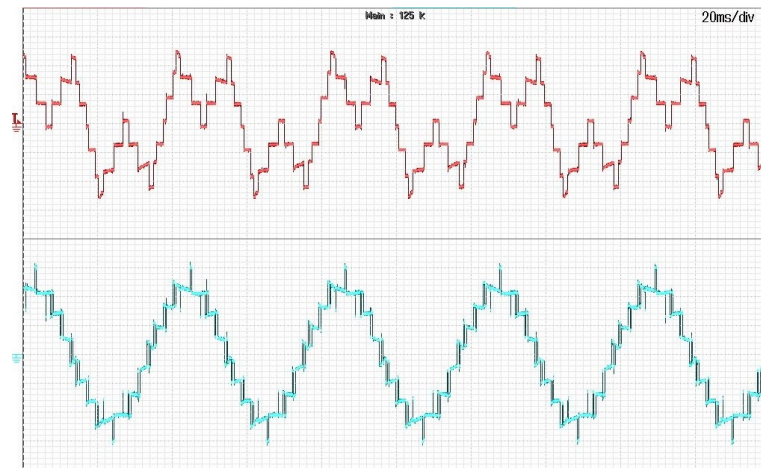


(b)

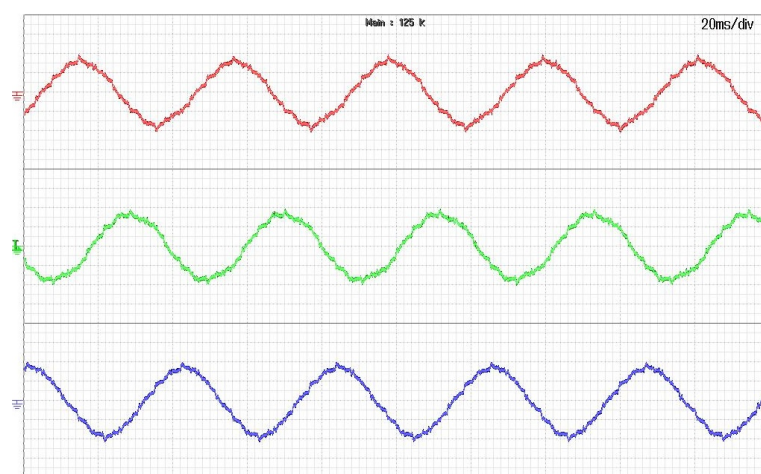


(c)

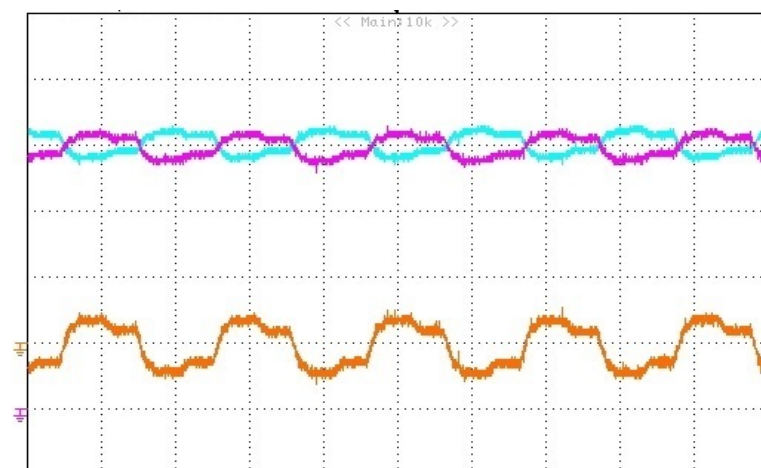
Fig. 3.6: Experimental results of 7L MLC for ($m=0.6824$, $N=3$). X-axis: 10 ms/div. (a) phase and line voltages (Y-axis: 50 V/div, 100 V/div) (b) machine stator currents (Y-axis: 1 A/div) (c) DC-link capacitor voltages and NPP error of 5L-HNPC inverter (X-axis:20 ms/div, Y-axis:10 V/div)



(a)

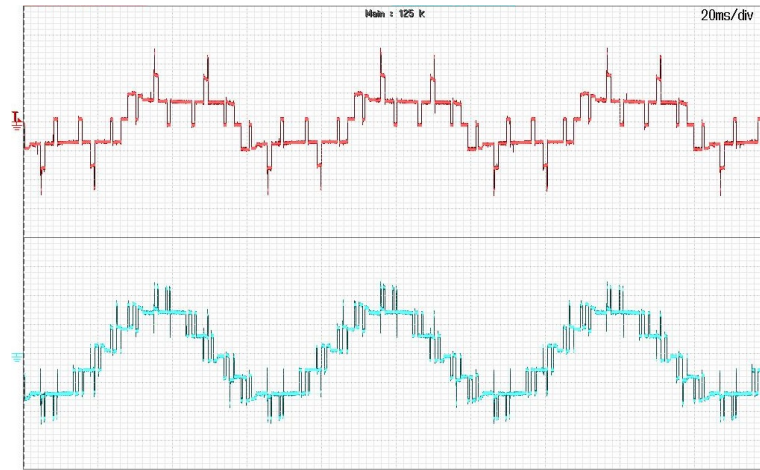


(b)

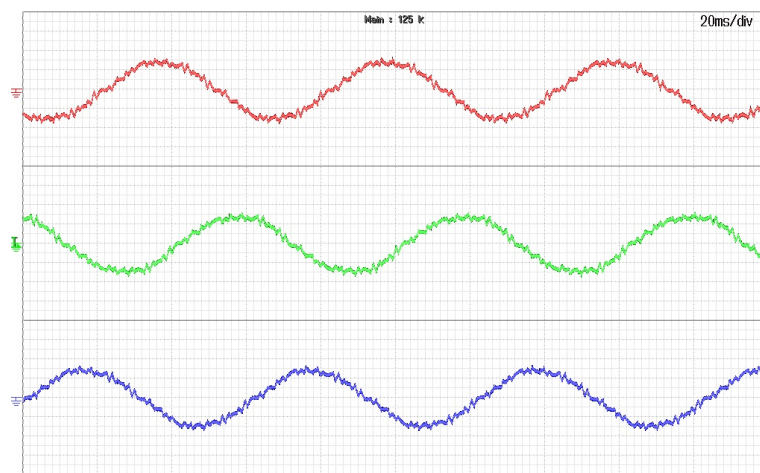


(c)

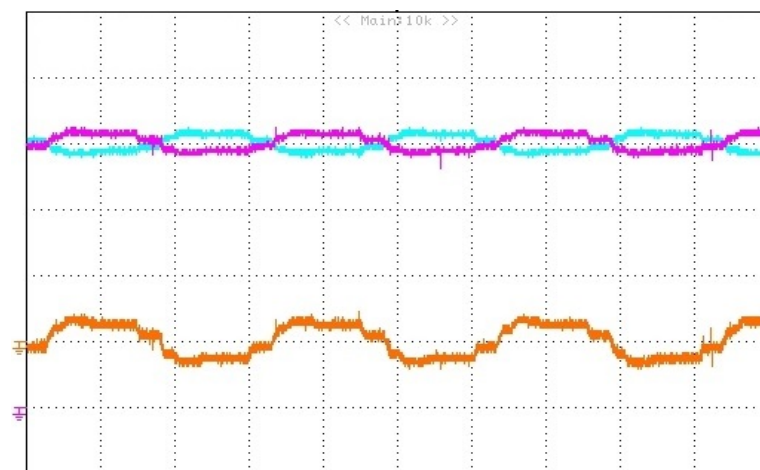
Fig. 3.7: Experimental results of 7L MLC for ($m=0.4824$, $N=6$). X-axis: 10 ms/div. (a) phase and line voltages (Y-axis: 50 V/div) (b) machine stator currents (Y-axis: 1 A/div) (c) DC-link capacitor voltages and NPP error of 5L-HNPC inverter (X-axis:20 ms/div, Y-axis:10 V/div)



(a)



(b)



(c)

Fig. 3.8: Experimental results of 7L MLC for ($m=0.3294$, $N=9$). X-axis: 10 ms/div. (a) phase and line voltages (Y-axis: 50 V/div) (b) machine stator currents (Y-axis: 1 A/div) (c) DC-link capacitor voltages and NPP error of 5L-HNPC inverter (X-axis:20 ms/div, Y-axis:10 V/div)

possible ways to realize optimal 7L waveforms, but the combinations, which lead to minimum voltage ripple across dc-link capacitors are preferred and selected. The dc-link voltage ripple significantly depends on the load as well as switching patterns [164]. In case of 5L-NPC inverter, the switching patterns, which lead to output voltage levels $\pm V_{dc}$ causes charging and discharging of dc-link capacitors. On the other hand, if the output voltage of 5L-NPC inverter is 0 or $\pm 2V_{dc}$, then dc-link capacitor voltages remain constant. This investigation is quite useful in selecting the pulse pattern that results into balanced dc-link capacitor voltages with small ripple.

The experimental results corresponding to operating points ($m=0.9294$, $N=3$), ($m=0.6824$, $N=3$), ($m=0.4824$, $N=6$), and ($m=0.3294$, $N=9$) are shown in Figs. 3.5 (a)-(c) to Figs. 3.8 (a)-(c), respectively. The inverter phase output voltage with seven-levels and line voltage waveforms with fifteen levels are shown in Figs. 3.5 (a) to Figs. 3.8 (a). The output currents are sinusoidal although device switching frequency is limited to f_{1R} , as shown in Figs. 3.5 (b) to Figs. 3.8 (b), respectively. It should be observed that the distortion of machine stator currents increases at lower values of m . The dc-link capacitor voltages and NPP error of 5L-HNPC inverter for the four operating points are shown in Fig. 3.5 (c) to Fig. 3.8 (c), respectively and it should be observed that ripple in dc-link capacitor voltages (V_{c1}, V_{c2}) of 5L-HNPC inverter is kept minimal.

The space vector trajectories of machine stator current corresponding to four operating points are shown in Fig. 3.9 (a)-(d), respectively. The nearly circular space vector trajectories show the high performance of SOP technique in reducing the harmonic distortion of machine currents, while limiting the maximum device switching frequency to f_{1R} . Also, inverter output currents are recorded into a PC through DEWESOFT data acquisition system. The FFT harmonic spectrum of machine currents for four operating points are shown in Fig. 3.10(a)-(d), respectively. The dis-

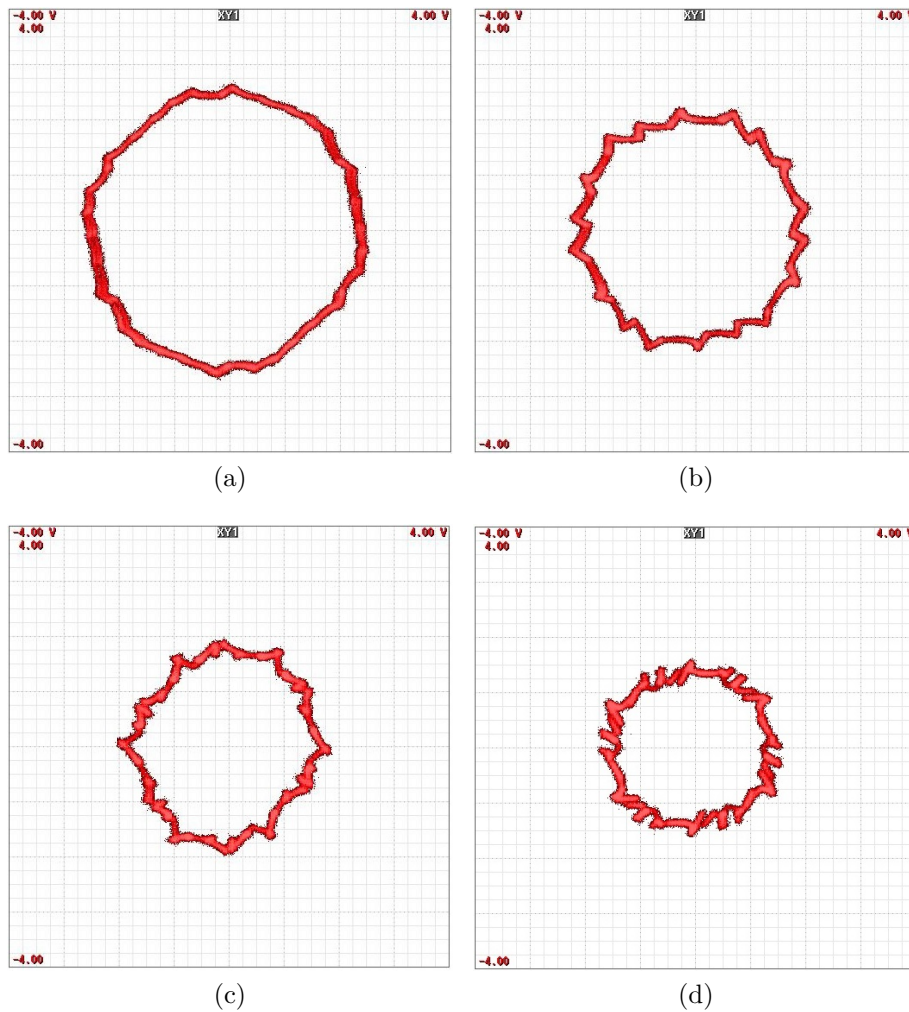


Fig. 3.9: Machine stator current space vector trajectories of 7L MLC (a) ($m=0.9294$, $N=3$) (b) ($m=0.6824$, $N=3$) (c) ($m=0.4824$, $N=6$) (d) ($m=0.3294$, $N=9$)

tortion factor of machine currents for the four operating points are equal to 0.052, 0.061, 0.051, and 0.048, respectively. The theoretical values of distortion factor for these four operating points are equal to 0.058, 0.077, 0.050, and 0.043, respectively. Thus, there is a close resemblance between theoretical and experimental results. Therefore, it can be concluded that proposed SOP technique limits the maximum device switching frequency to rated fundamental frequency f_{1R} , without compromising on the quality of machine currents.

The gating signals to one semiconductor device from 3L-NPC1, 3L-NPC2 and H-Bridge modules (S1, S5 and S9) have been captured to de-

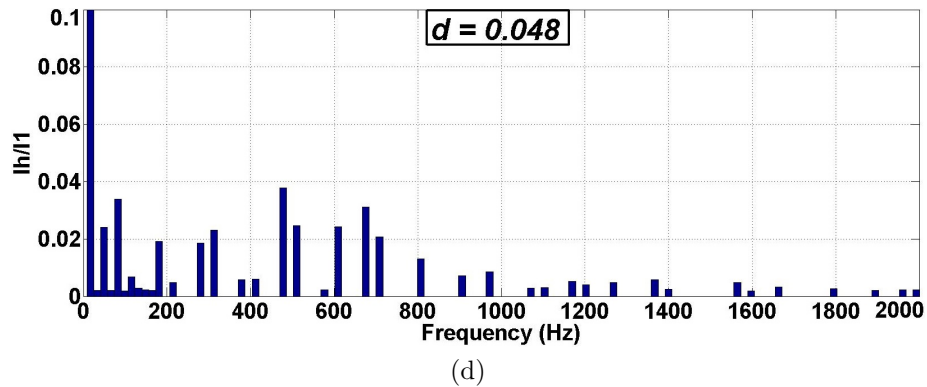
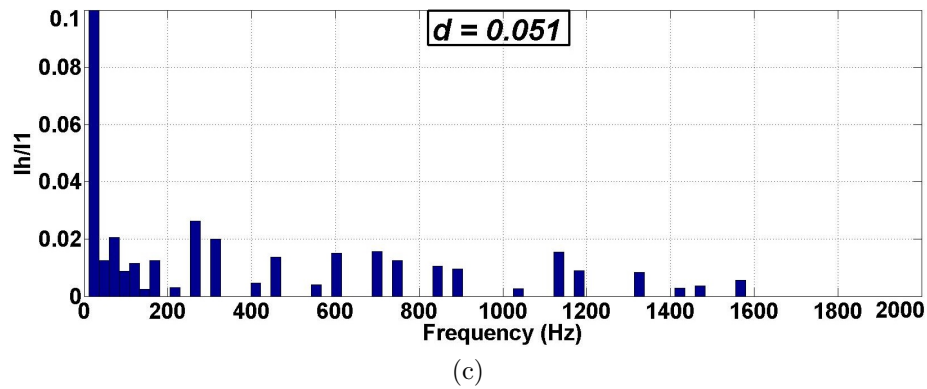
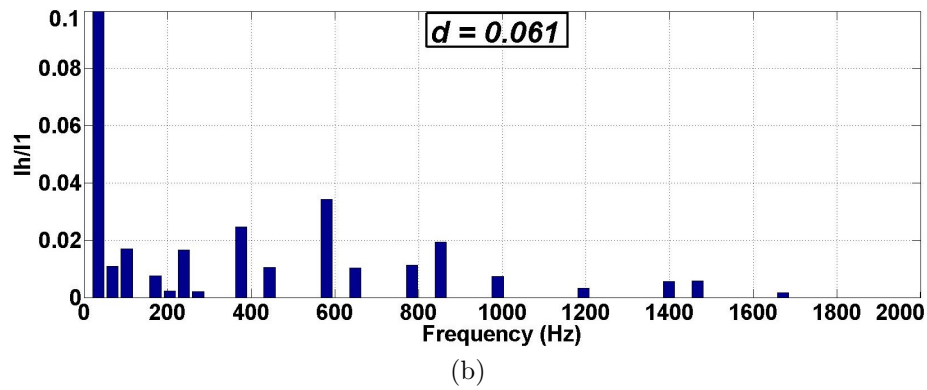
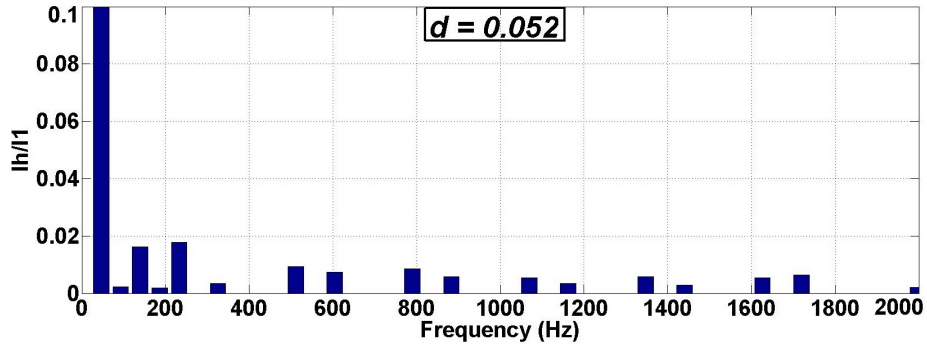
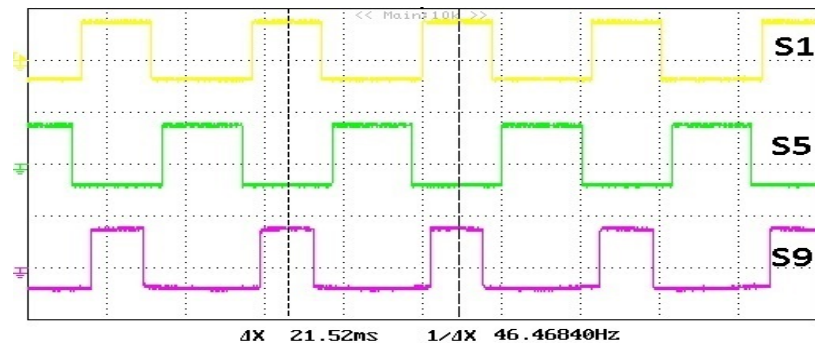
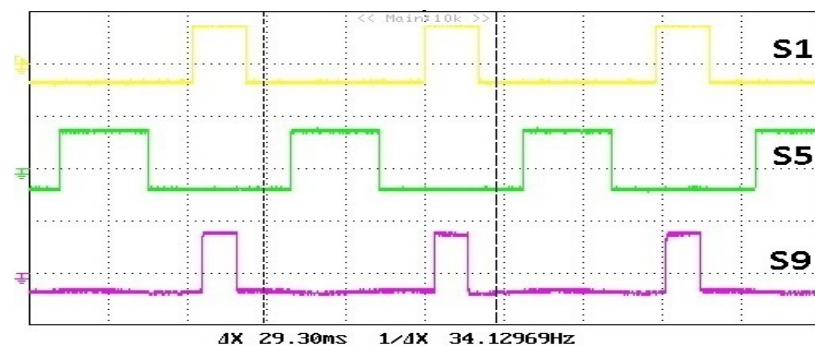


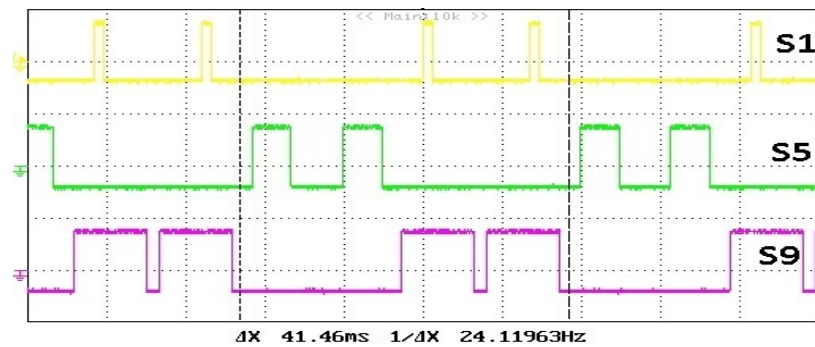
Fig. 3.10: FFT harmonic spectrum of machine stator currents of 7L MLC (enlarged view to show dominant harmonics). (a) ($m=0.9294$, $N=3$) (b) ($m=0.6824$, $N=3$) (c) ($m=0.4824$, $N=6$) (d) ($m=0.3294$, $N=9$)



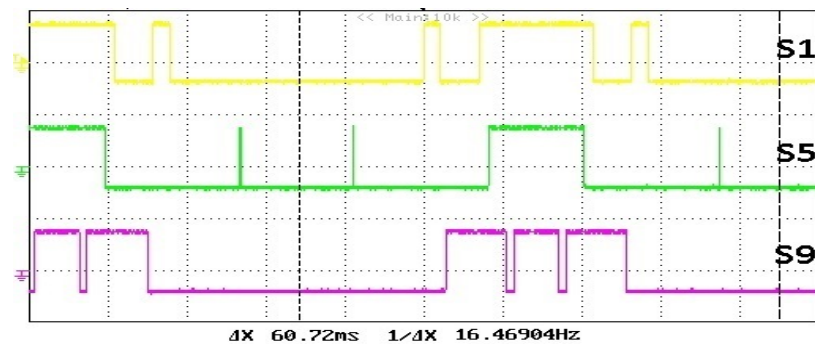
(a)



(b)



(c)



(d)

Fig. 3.11: Gating signals of semiconductor devices in 7L MLC. X-axis: 10 ms/div, Y-axis: 20 V/div (a)($m=0.9294$, $N=3$)(b)($m=0.6824$, $N=3$)(c)($m=0.4824$, $N=6$)(d)($m=0.3294$, $N=9$)

termine the device switching frequency. For operating point ($m=0.9294$, $N=3$, $f_1=46.47$ Hz), it can be calculated from Table 3.4 (a) that device switching frequency of all semiconductor devices should be equal to f_1 ($N=1$). This can be verified from the gating signals shown in Fig. 3.11 (a) that semiconductor device is turned on/off twice in one fundamental period i.e device switching frequency f_s is equal to $f_1=46.47$ Hz. Similarly, for operating point ($m=0.4824$, $N=6$, $f_1=24.12$ Hz), it can be observed from Table 3.4 (c) that device switching frequency of all semiconductor devices should be equal to $2f_1$ ($N=2$). This can be confirmed from gating signals shown in Fig. 3.11 (c). Similar observations can be made for the other two operating points from Fig. 3.11(b) and Fig. 3.11(d). It verifies that device switching frequency is limited to f_{1R} and all semiconductor devices operate at identical switching frequency.

3.4 Experimental Results for 9L MLC

The proposed modified SOP technique has been implemented for 9L MLC with $f_{s,max}=f_{1R}$. The experimental set-up for 9L MLC remains the same as that shown in Section 2.7.3. To demonstrate the effectiveness of proposed SOP technique, four operating points ($m=0.9176$, $N=4$), ($m=0.7020$, $N=4$), ($m=0.4980$, $N=8$), and ($m=0.3333$, $N=12$) have been selected. The optimal switching angles and their corresponding distribution of switching commutations for four operating points are shown in Table 3.5 (a)-(d), respectively. It should be observed that 3L-NPC inverters have the same value of N_{3L} and thus, identical device switching frequency operation is achieved. The device switching frequency for the four operating points should be equal to f_1 , f_1 , $2f_1$ and $3f_1$, respectively. Also, the optimal switching angles satisfy the optimization constraint as shown in the last row of each Table 3.5 (a)-(d).

Table 3.5: Optimal switching angles and division of N for 9L-MLC. (a) ($m=0.9176, N=4$) (b) ($m=0.7020, N=4$) (c) ($m=0.4980, N=8$) (d) ($m=0.3333, N=12$)

Optimal Angles (degree)							Optimal Angles (degree)						
Output	0	4.12	12.05	23.77	38.73	N	Output	0	16.05	33.9	54.05	64.54	N
V_{9L}	0	1	2	3	4	4	V_{9L}	0	1	2	3	4	4
V_{5L1}	0	0	0	1	2	2	V_{5L1}	0	0	0	1	2	2
V_{5L2}	0	1	2	2	2	2	V_{5L2}	0	1	2	2	2	2
V_{3L11}	0	0	0	0	1	1	V_{3L11}	0	0	0	0	1	1
V_{3L12}	0	0	0	-1	-1	1	V_{3L12}	0	0	0	-1	-1	1
V_{3L21}	0	0	1	1	1	1	V_{3L21}	0	0	1	1	1	1
V_{3L22}	0	-1	-1	-1	-1	1	V_{3L22}	0	-1	-1	-1	-1	1

$$\frac{1}{4} \sum_{i=1}^4 s(i) \cos(\alpha_i) = 0.9176 \approx m$$

$$\frac{1}{4} \sum_{i=1}^4 s(i) \cos(\alpha_i) = 0.7017 \approx m$$

(a)

(b)

Optimal Angles (degree)										
Output	0	2.83	8.07	12.51	23.45	49.16	57.34	65.81	73.33	N
V_{9L}	0	1	2	3	4	3	2	1	0	8
V_{5L1}	0	0	0	1	2	1	0	0	0	4
V_{5L2}	0	1	2	2	2	2	2	1	0	4
V_{3L11}	0	0	0	0	1	0	0	0	0	2
V_{3L12}	0	0	0	-1	-1	-1	0	0	0	2
V_{3L21}	0	0	1	1	1	1	1	0	0	2
V_{3L22}	0	-1	-1	-1	-1	-1	-1	-1	0	2

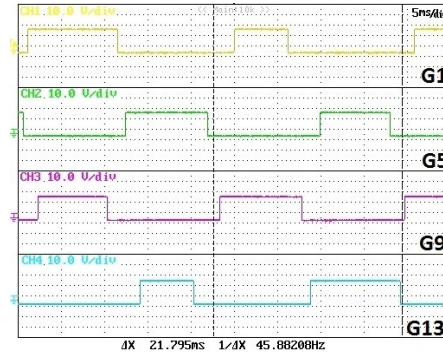
$$\frac{1}{4} \sum_{i=1}^8 s(i) \cos(\alpha_i) = 0.4984 \approx m$$

(c)

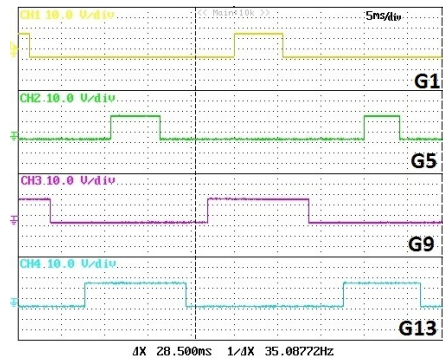
Optimal Angles (degree)														
Output	0	39.84	59.96	65.92	67.33	82.02	82.62	83.22	83.82	85.59	86.86	88.11	89.47	N
V_{9L}	0	1	2	1	2	3	4	3	2	3	2	3	2	12
V_{5L1}	0	1	2	1	2	2	2	2	2	2	1	2	2	6
V_{5L2}	0	0	0	0	0	1	2	1	0	1	1	1	0	6
V_{3L11}	0	0	1	0	1	1	1	1	1	1	1	1	1	3
V_{3L12}	0	-1	-1	-1	-1	-1	-1	-1	-1	-1	0	-1	-1	3
V_{3L21}	0	0	0	0	0	1	1	1	0	1	1	1	1	3
V_{3L22}	0	0	0	0	0	0	-1	0	0	0	0	0	1	3

$$\frac{1}{4} \sum_{i=1}^{12} s(i) \cos(\alpha_i) = 0.3332 \approx m$$

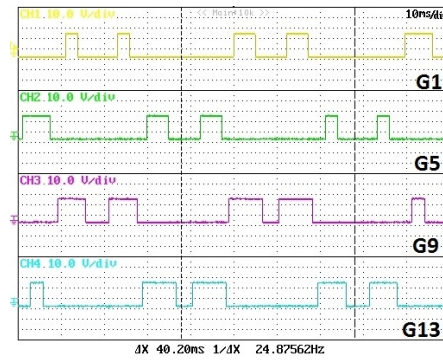
(d)



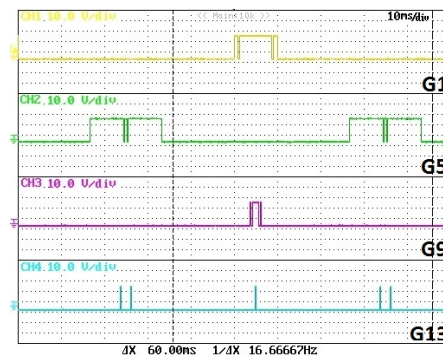
(a)



(b)

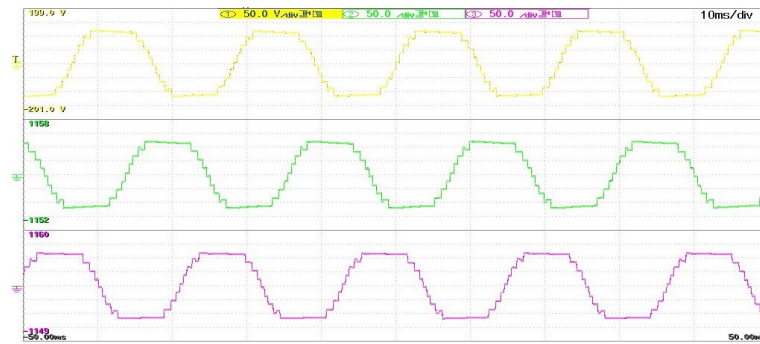


(c)

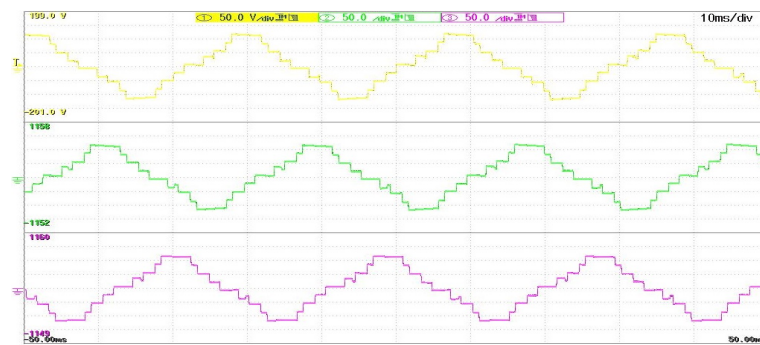


(d)

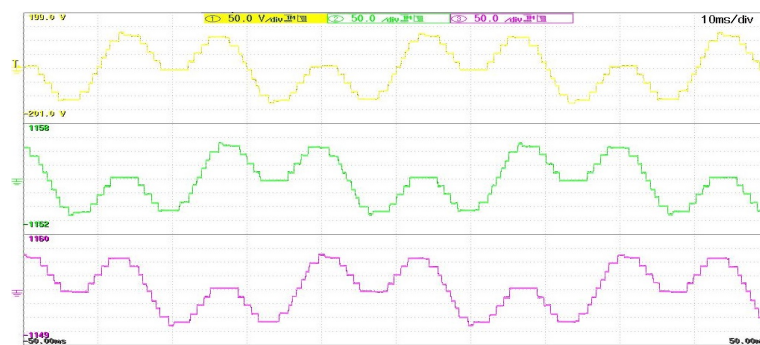
Fig. 3.12: Gating signals for IGBTs S1, S5, S9 and S13 in phase A of 9L MLC. (a) ($m=0.9176$, $N=4$) (b) ($m=0.7020$, $N=4$) (c) ($m=0.4980$, $N=8$) (d) ($m=0.3333$, $N=12$)



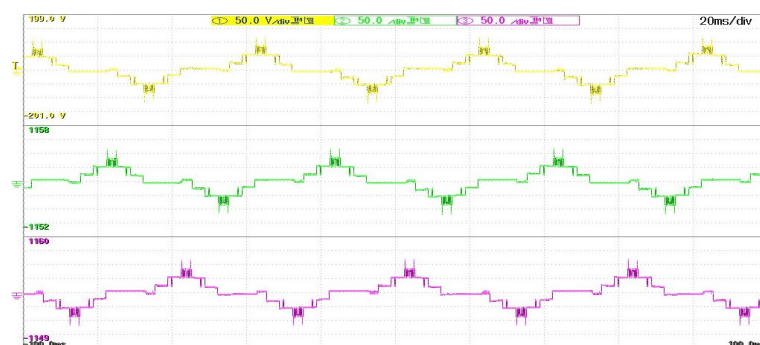
(a)



(b)

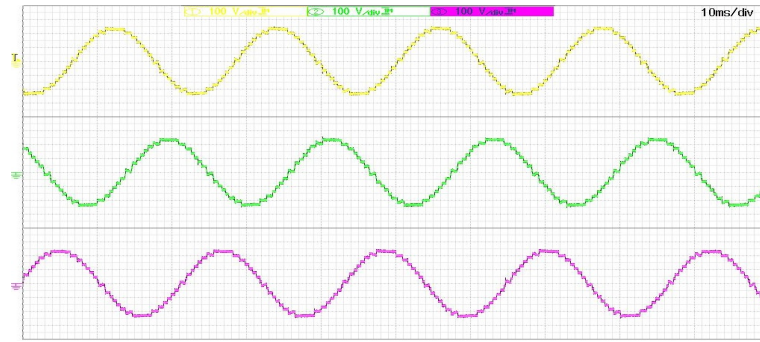


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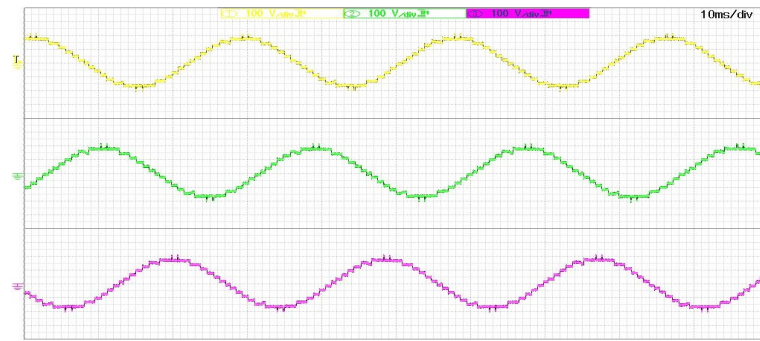


(d)

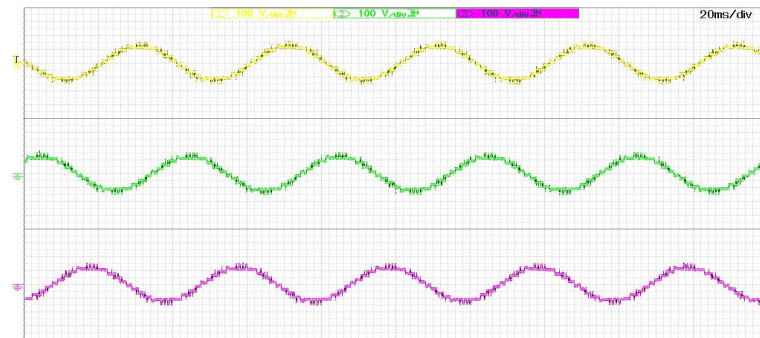
Fig. 3.13: Output phase-voltage of 9L MLC. X-axis:10 ms/div. Y-axis: 50 V/div. (a) ($m=0.9176$, $N=4$) (b) ($m=0.7020$, $N=4$) (c) ($m=0.4980$, $N=8$) (d) ($m=0.3333$, $N=12$)



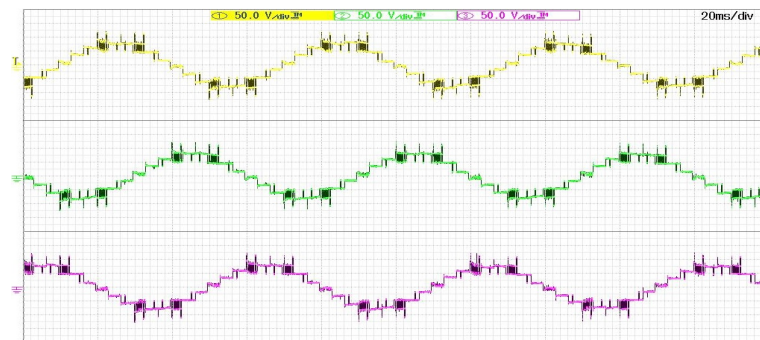
(a)



(b)



(c)

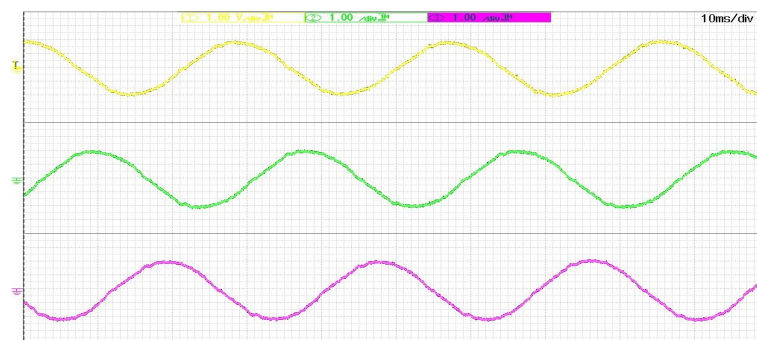


(d)

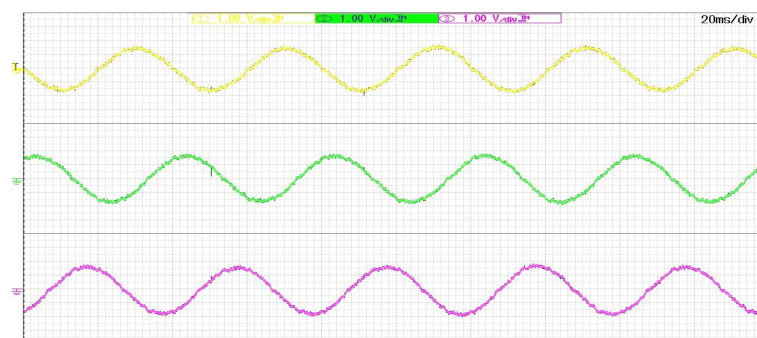
Fig. 3.14: Output line-voltage of 9L MLC. (a) ($m=0.9176$, $N=4$) (X-axis:10 ms/div, Y-axis: 100 V/div) (b) ($m=0.7020$, $N=4$) (X-axis:10 ms/div, Y-axis: 100 V/div)(c) ($m=0.4980$, $N=8$) (X-axis:20 ms/div, Y-axis: 100 V/div)(d) ($m=0.3333$, $N=12$) (X-axis:20 ms/div, Y-axis: 50 V/div)



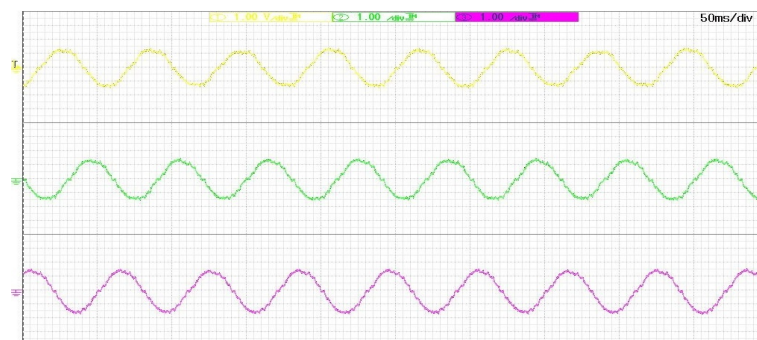
(a)



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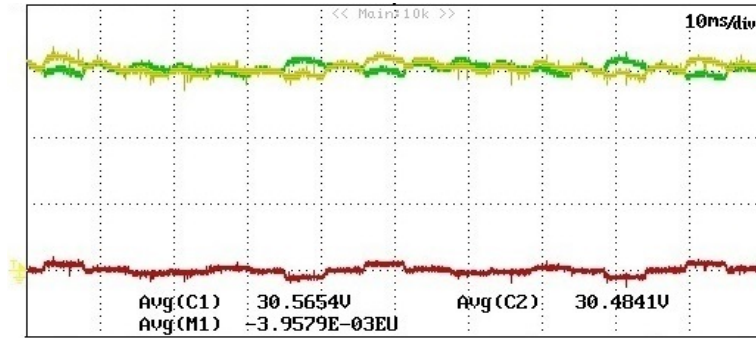


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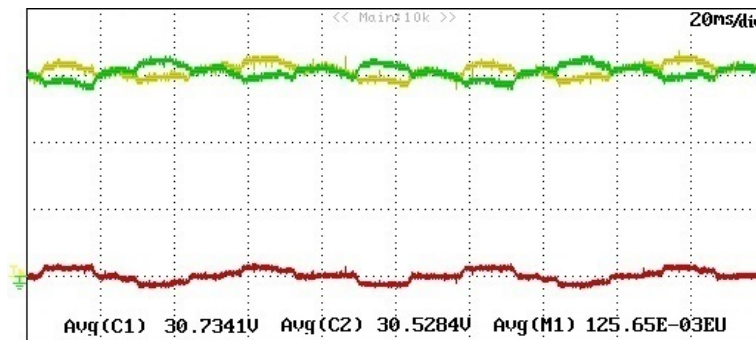


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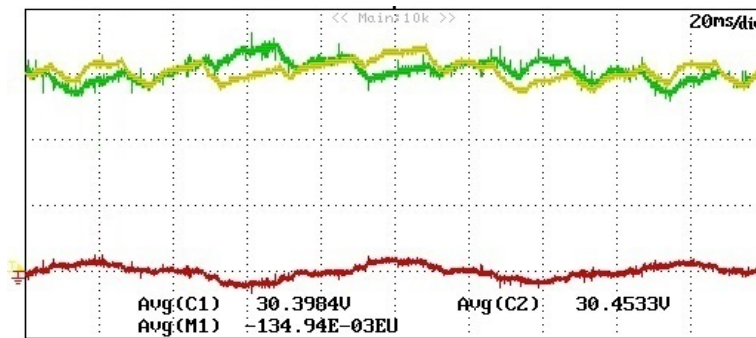
Fig. 3.15: Machine stator currents. Y-axis: 1 A/div. (a) ($m=0.9176$, $N=4$) (X-axis:10 ms/div) (b) ($m=0.7020$, $N=4$) (X-axis:10 ms/div)(c) ($m=0.4980$, $N=8$) (X-axis:20 ms/div)(d) ($m=0.3333$, $N=12$) (X-axis:50 ms/div)



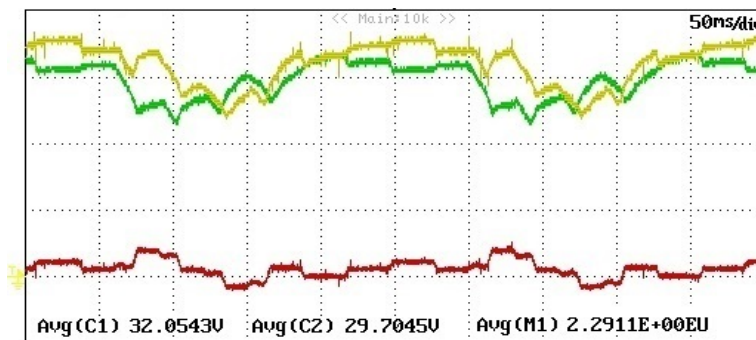
(a)



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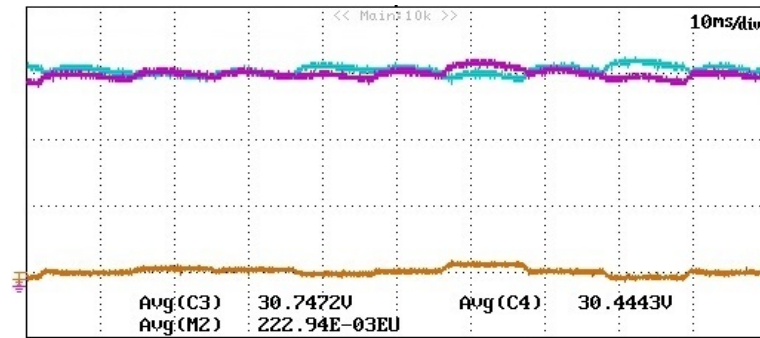


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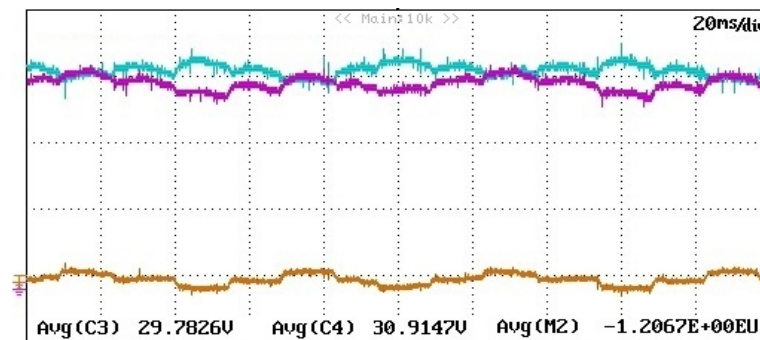


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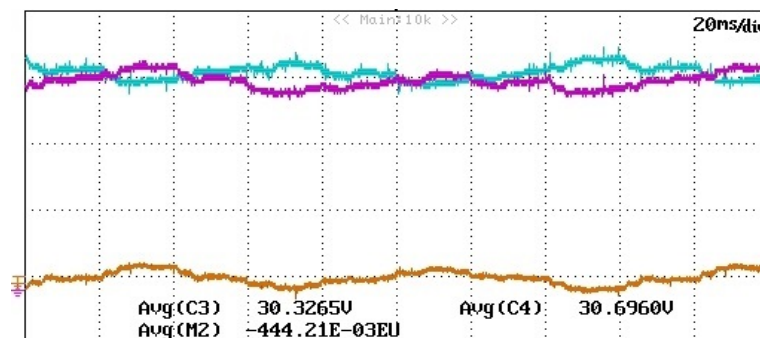
Fig. 3.16: Dc-link capacitor voltages and NPP error of 5L-HNPC1 inverter (V_{c1}, V_{c2}). Y-axis: 10 V/div (a) ($m=0.9176, N=4$) (b) ($m=0.7020, N=4$) (c) ($m=0.4980, N=8$) (d) ($m=0.3333, N=12$)



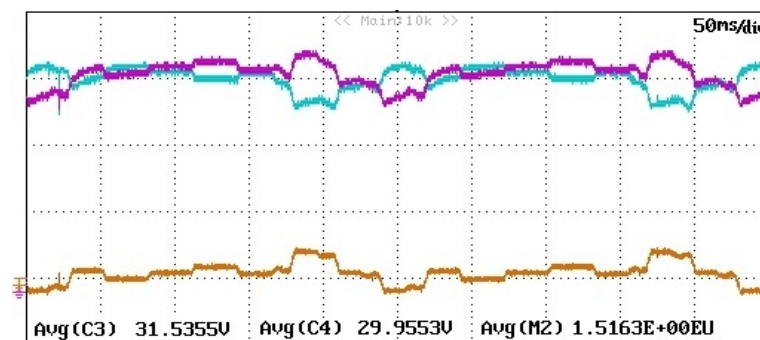
(a)



(b)



(c)



(d)

Fig. 3.17: Dc-link capacitor voltages and NPP error of 5L-HNPC2 inverter (V_{c3}, V_{c4}). Y-axis: 10 V/div. (a) ($m=0.9176, N=4$) (b) ($m=0.7020, N=4$) (c) ($m=0.4980, N=8$) (d) ($m=0.3333, N=12$)

Gating signals to the semiconductor devices S1, S5, S9 and S13 for the four operating points ($m=0.9176$, $N=4$, $f_1=45.88$ Hz), ($m=0.7020$, $N=4$, $f_1=35.10$ Hz), ($m=0.4980$, $N=8$, $f_1=24.90$ Hz) and ($m=0.3333$, $N=12$, $f_1=16.667$ Hz) are shown in Fig. 3.12 (a)-(d), respectively. It should be observed from Fig. 3.12 (a)-(d) that device switching frequency for the four operating points is equal to f_1 , f_1 , $2f_1$, and $3f_1$, respectively and the same can be verified from Table 3.5(a)-(d), respectively. Thus, it can be concluded that all semiconductor devices commute at same device switching frequency that is limited to f_{1R} .

The experimental results corresponding to four operating points are shown in Figs. 3.13 (a)-(d) to Figs. 3.19 (a)-(d), respectively. The inverter phase output voltages with nine voltage levels are shown in Fig. 3.13 (a)-(d). The line voltages of induction motor with 17 levels that are close to sinusoidal shape are shown in Fig. 3.14 (a)-(d). Due to optimal switching patterns, stator currents of induction motor are sinusoidal as shown in Fig. 3.15 (a)-(d), although device switching frequency is limited to 50 Hz. It should be observed that harmonic distortion of machine currents increases at lower values of modulation index.

The dc-link capacitor voltages and NPP error of 5L-HNPC1 and 5L-HNPC2 converters of phase A for the four operating points are shown in Figs. 3.16 (a)-(d) and Fig. 3.17 (a)-(d), respectively. NPP error is almost negligible for the operating points ($m=0.9176$, $N=4$), ($m=0.7020$, $N=4$) and ($m=0.4980$, $N=8$), whereas for the operating point ($m=0.3333$, $N=12$) it is slightly more (7.48%, 4.95%). However, THD of machine currents is within acceptable limits.

Space vector trajectory of stator currents for these four operating points are shown in Fig. 3.18 (a)-(d), respectively. Circular space vector trajectories indicate minimal harmonic distortion of machine currents. It should be observed that harmonic distortion of machine currents increases at lower

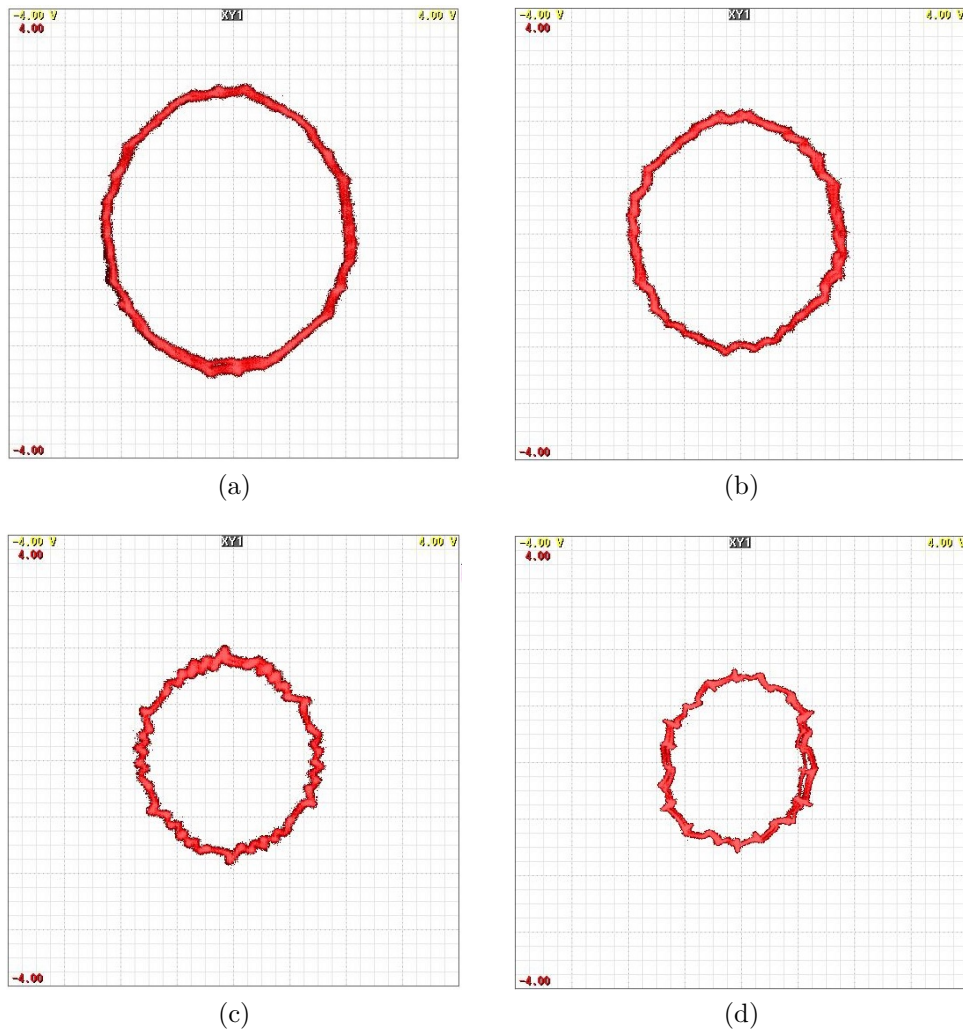


Fig. 3.18: Space vector trajectory of stator currents of 9L MLC. (a) ($m=0.9176$, $N=4$) (b) ($m=0.7020$, $N=4$) (c) ($m=0.4980$, $N=8$) (d) ($m=0.3333$, $N=12$)

values of m . In addition, recorded machine currents data has been processed to determine THD of machine current waveforms. Enlarged view of harmonic spectrum of machine current waveforms for these four operating points are shown in Fig. 3.19 (a)-(d), respectively. The THD of machine stator currents for the four operating points are equal to 2.30%, 3.10%, 4.82% and 7.12%, respectively. Current harmonic spectrum at these four operating points shows that dominant harmonics have magnitude less than 1%, 2%, 2%, and 3.5%, respectively. Therefore, it can be concluded that proposed SOP technique permits operation of 9L MLC with $f_s \leq f_{1R}$, while harmonic distortion of stator currents is kept minimal.

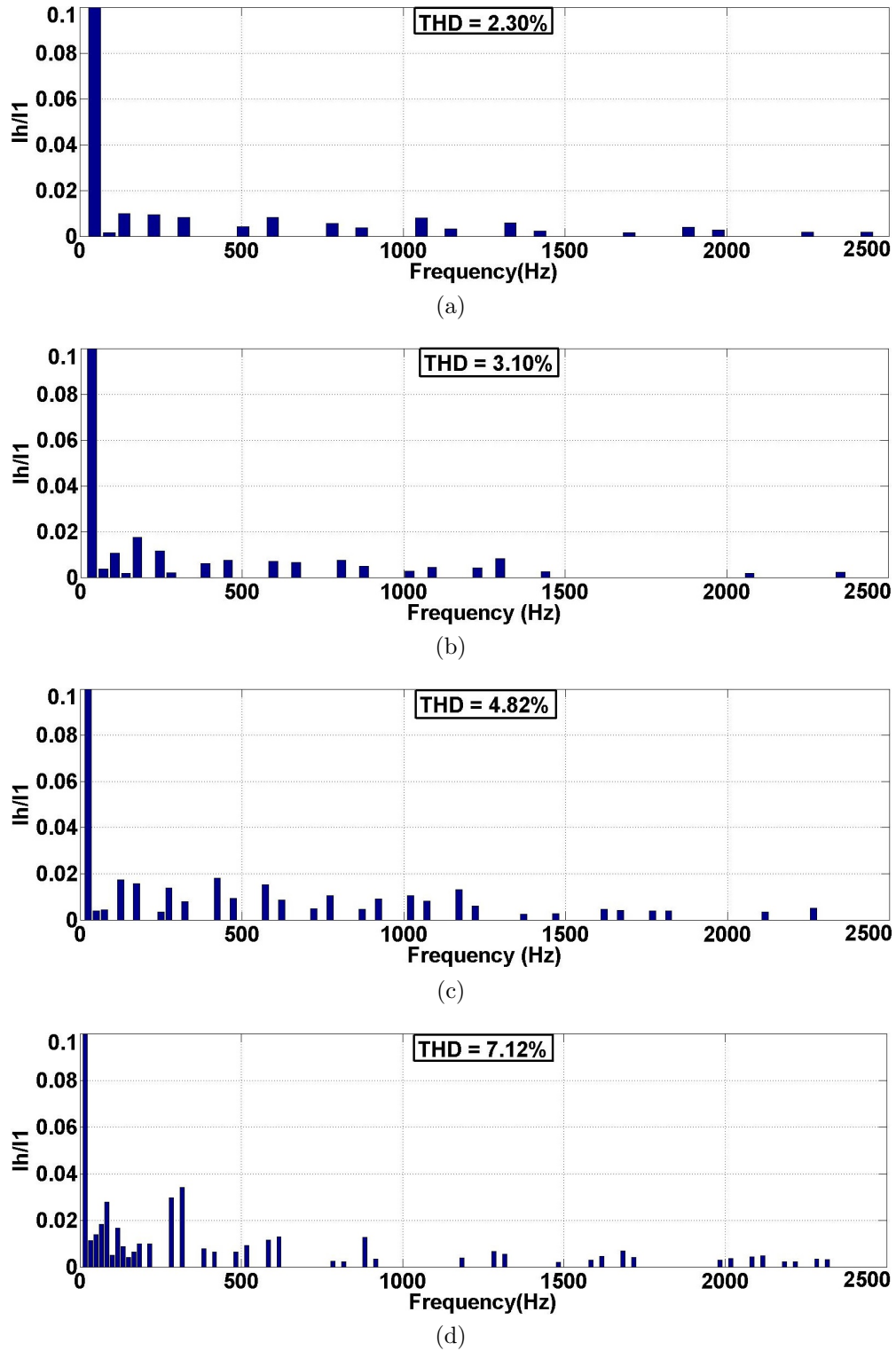


Fig. 3.19: Harmonic spectrum of machine stator currents for 9L MLC (enlarged view for showing dominant harmonics and their magnitude). (a) ($m=0.9176$, $N=4$) (b) ($m=0.7020$, $N=4$) (c) ($m=0.4980$, $N=8$) (d) ($m=0.3333$, $N=12$)

3.5 Summary and Conclusions

In this Chapter, complete details of proposed modified SOP technique have been presented. Three important steps in SOP technique are estimation of pulse number N , optimization of switching angles and allocation of optimal switching angles to each power semiconductor device. The proposed SOP technique modifies the first step in SOP technique such that power semiconductor devices operate at identical switching frequency and limit the peak device switching frequency to desired $f_{s,max}$. The performance of generalized and proposed SOP techniques are quite similar, although proposed SOP technique operates MLC at lower device switching frequency. In addition, proposed SOP technique maintains same pulse number in the higher modulation index range that avoids transients in machine currents. Low power prototypes of cascaded 7L and 9L MLCs have been developed to demonstrate the performance of SOP technique. From the experimental results, it can be concluded that SOP technique can operate seven or higher-level inverters with identical switching frequency and peak device switching frequency limited to rated fundamental frequency, while keeping harmonic distortion of machine currents below standard limits.

Chapter 4

Modified SOP Technique for MMC Topology

4.1 Introduction

MMC topology has been originally proposed for HVDC systems [25, 135, 136]. This topology overcomes the drawback of CHB topology by eliminating need of isolated dc sources by means of floating capacitors that act as voltage sources. Due to modularity and scalability, MMC is suitable for any voltage/current level requirements and also suitable for fault-tolerant operation. Recently, MMC has been commercially introduced for MV drives both as an active-front-end (AFE) rectifier and also as an inverter [137]. One of the main challenges for control of MMC is to achieve balanced submodule capacitor voltages. The unbalanced submodule capacitor voltages leads to further harmonic distortion of converter output currents and also, increases voltage stress on submodule capacitors and the power semiconductor devices. This Chapter gives the details of modified SOP technique for MMC topology. The objectives of the proposed technique are as follows: low device switching frequency operation, minimal harmonic distortion of converter output currents and balanced submodule capacitor voltages. The proposed technique has been utilized to modulate the 5L-MMC feeding an 1.5-kW induction motor drive with $f_{s,max}$ set at 200 Hz.

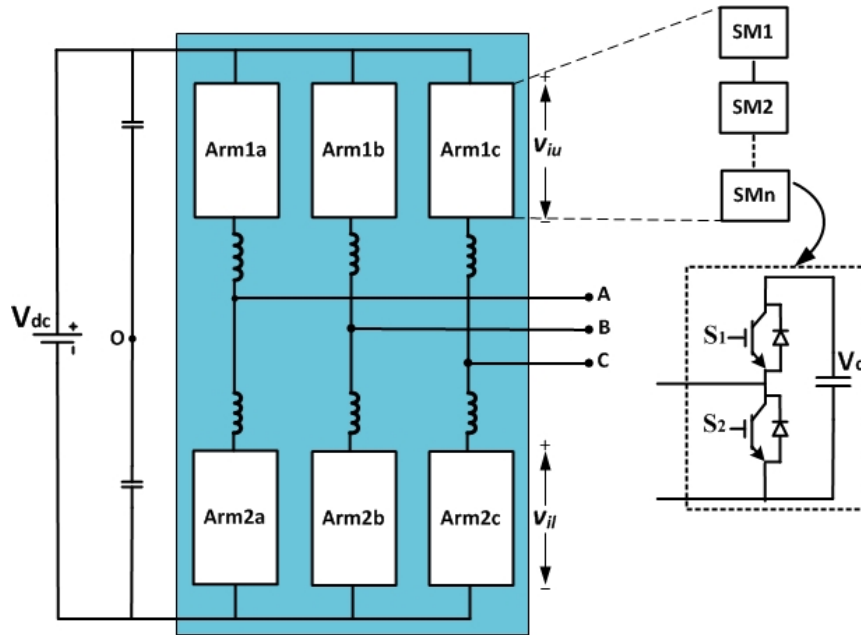


Fig. 4.1: MMC topology

This Chapter is organized as follows: circuit topology and operation of MMC is given in Section 4.2, details of proposed modified SOP technique are given in Section 4.3, experimental results for MMC topology are given in Section 4.4. This Chapter is concluded in Section 4.5.

4.2 Circuit Topology and Operation

The circuit configuration of MMC topology is shown in Fig. 4.1. Each phase leg of MMC consists of two arms connected in series via arm inductors. The arm connected to positive rail is called upper arm and the arm connected to negative rail is called lower arm. Each arm consists of several submodules connected in series. The submodule consists of a half-bridge cell with a dc capacitor. Each submodule can be either inserted or bypassed by turning on top switch S1 or bottom switch S2, respectively. When a submodule is inserted, its output voltage is equal to capacitor voltage that gets charged or discharged depending on the direction of arm current. When a submodule is bypassed, its output voltage will be zero and its capacitor voltage remains constant.

Table 4.1: Synthesis of output voltage levels of 5L-MMC

N_u	N_l	v_{iu}	v_{il}	v_{phO}
0	4	0	$4V_{nom}$	$2V_{nom}$
1	3	V_{nom}	$3V_{nom}$	V_{nom}
2	2	$2V_{nom}$	$2V_{nom}$	0
3	1	$3V_{nom}$	V_{nom}	$-V_{nom}$
4	0	$4V_{nom}$	0	$-2V_{nom}$

The ac-side output voltage is controlled by varying the number of submodules that are inserted in the upper and lower arms. Consider a single phase leg, let the instantaneous inserted voltages in upper arm and lower arm are denoted as v_{iu} and v_{il} , respectively. By neglecting the arm inductor voltage drop, it can be shown that ac-side output voltage is equal to $\frac{1}{2}(v_{il} - v_{iu})$ [167]. Let the number of submodules in each arm are denoted as N_{sm} . Then, nominal value of submodule capacitor voltage V_{nom} should be equal to V_{dc}/N_{sm} . In general, MMC is operated such that N_{sm} submodules are inserted in one phase leg, which lead to $N_{sm}+1$ voltage levels in output phase voltage. Thus, MMC with $(n-1)$ submodules in one arm is referred as n L-MMC in this paper. For example, MMC with four submodules in each arm is referred as 5L-MMC. The operation of 5L-MMC for one of three phase legs is shown in Table 4.1, where N_u , N_l denote the number of submodules inserted in upper arm and lower arm, respectively. It should be observed that phase output voltage v_{phO} ($ph \in A, B, C$) of MMC with four submodules consists of five voltage levels.

4.3 Modified SOP Technique

The implementation of SOP technique for any power electronic converter involves three steps :

1. Determine value of N such that $f_s \leq f_{s,max}$ for each m .

2. Perform optimization to pre-determine switching angles for each steady-state operating point (m, N) that minimize the total harmonic distortion of output current.
3. Assign switching angles to each power semiconductor device based on optimal switching patterns.

The first and last steps of SOP technique are dependent on converter topology and thus, modifications are required to modulate MMC topology. Some classical topologies such as NPC, FC, CHB or hybrid topologies such as 3L-NPC leg based CHB topology, share a common feature that an nL -MLC converter consists of $0.5*(n-1)$ sub-converters (H-Bridge or 3L-NPC) in each phase. Therefore, a generalized SOP technique has been developed to estimate pulse number N for an entire range of m , as explained in Chapters 2 and 3. The second step of SOP is independent of converter topology and thus, the implementation details remains same as in Section 2.4. In the last step of SOP, the switching angles to each power semiconductor device should be assigned in order to achieve identical device switching frequency. There might be additional requirements unique to each topology, for example, capacitor voltage balancing for MMC topology. More details about first and last steps of SOP technique for MMC topology are given next.

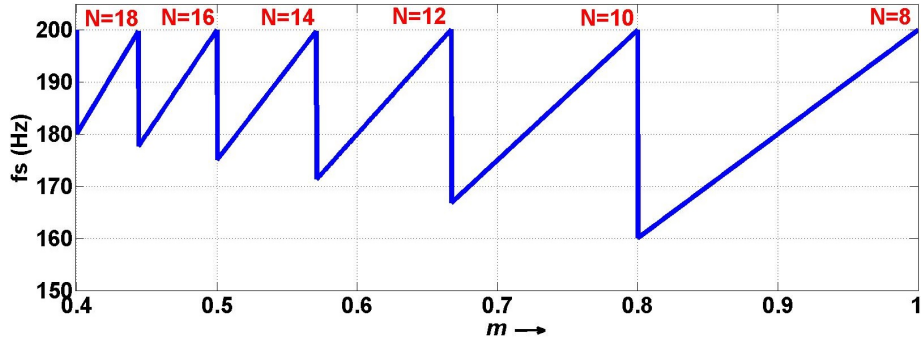
4.3.1 Calculation of N

Consider an nL -MMC that has to be operated with device switching frequency f_s limited to $f_{s,max}$. Let the ratio between f_s and f_1 be denoted as R_f . As the SOP technique demands that R_f should be an integer, the following relationship is obtained for each m ,

$$R_f = \text{floor} \left(\frac{f_{s,max}}{m f_{1R}} \right), \quad (4.1)$$

Table 4.2: SOP of 5L-MMC at $f_{s,max} = 200$ Hz: Computed N and f_s for a given m

m	f_1 (Hz)	N	f_s (Hz)
0.801 - 1.000	40.05 - 50.00	8	160.20 - 200
0.668 - 0.800	33.40 - 40.00	10	167.00 - 200
0.572 - 0.667	28.60 - 33.35	12	171.60 - 200
0.501 - 0.571	25.05 - 28.55	14	175.35 - 200
0.445 - 0.500	22.25 - 25.00	16	178.00 - 200
0.401 - 0.444	20.05 - 22.20	18	180.45 - 200
0.365 - 0.400	18.25 - 20.00	20	182.50 - 200
0.334 - 0.364	16.70 - 18.20	22	183.70 - 200
0.309 - 0.333	15.45 - 16.65	24	185.40 - 200
0.287 - 0.308	14.35 - 15.40	26	186.55 - 200

Fig. 4.2: SOP of 5L-MMC at $f_{s,max} = 200$ Hz: Computed N and f_s for a given m

where, the function ‘*floor*’ returns the largest previous integer. Then, the total number of commutations in one arm, which contains $(n-1)$ submodules should be equal to $(n-1)*2*R_f$. Finally, the value of N for the nL -MMC is obtained as,

$$\begin{aligned}
 N &= \frac{(n-1) * 2R_f}{4} \\
 &= \frac{(n-1)}{2} * \text{floor} \left(\frac{f_{s,max}}{m f_{1R}} \right). \quad (4.2)
 \end{aligned}$$

The goal of our study is to implement SOP for a 5L-MMC with $f_{s,max}$ set at 200 Hz. The selected value of $f_{s,max}$ is based on the experimental results from classical 5L-MLC topologies [114]. Based on (4.2), the estimated

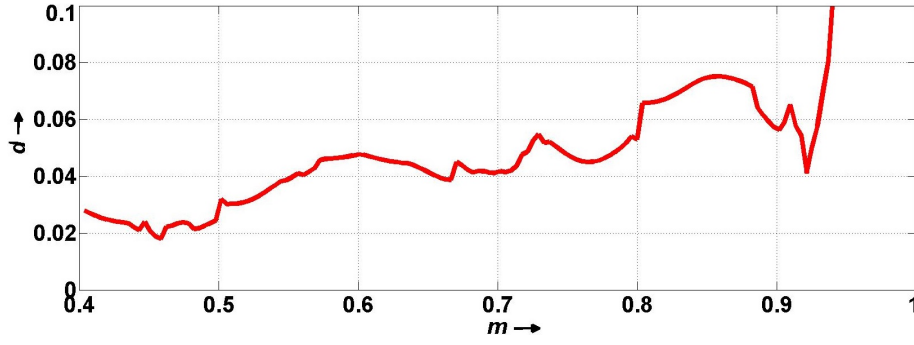


Fig. 4.3: Results of optimization for operating 5L-MMC at $f_{s,max} = 200$ Hz : d versus m

values of N and corresponding device switching frequency for different values of m are shown in Fig. 4.2 and Table 4.2. It should be observed that device switching frequency is limited to 200 Hz for each value of m . Next, optimization is performed to determine N switching angles for each steady-state operating point (m, N) that minimize the total harmonic distortion of converter output currents.

4.3.2 Optimization of switching angles

The procedure for optimization algorithm remains same as presented in Section 2.4. The optimization results of proposed technique for 5L-MMC with $f_{s,max} = 200$ Hz are shown in Fig. 4.3. It should be observed that harmonic distortion has been reduced significantly when $m < 0.93$. At higher modulation index values $m > 0.93$, harmonic distortion increases as MMC approaches six-step operation.

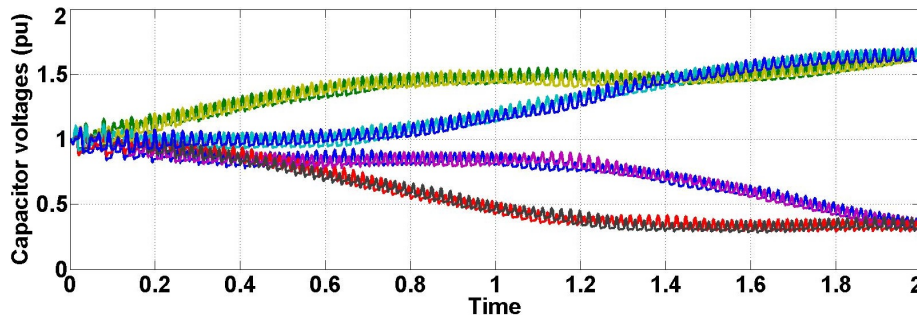


Fig. 4.4: Submodule capacitor voltages (p.u.) of one phase leg of 5L-MMC with pre-assigned switching angles for insertion/bypass of submodules

4.3.3 Allocation of Optimal Switching Angles

After determining the optimal switching angles, the next step is to allocate switching angles to each power semiconductor device. Two main factors to be considered while assigning switching angles are identical device switching frequency and balanced floating capacitor voltages. It is possible to write an algorithm to pre-determine switching angles to decide, which submodule to be inserted/bypassed based on the optimized switching angles in order to achieve identical device switching frequency. However, the submodule capacitor voltages gets diverged as shown in Fig. 4.4.

The main reason for divergence of submodule capacitor voltages is that charging and discharging of submodule capacitor voltages depends on magnitude and direction of arm current as well as duration for which submodule is inserted. Therefore, it is never possible to maintain capacitor voltages around their nominal value with pre-assigned switching instants to insert/bypass submodules. In this paper, angle swapping technique has been proposed to balance floating capacitor voltages.

Angle Swapping Technique: During one fundamental cycle, a certain energy transfer takes place between submodule capacitor and converter that depends on direction and magnitude of arm current and duration of submodule insertion. The capacitor voltages get charged if the net energy transfer is positive, whereas capacitor voltages get discharged if net energy transfer is negative in one fundamental cycle. Thus, the submodule capacitor voltages either continuously increase or decrease over a period of time due to pre-assigned switching angles, as shown in Fig. 4.4.

To achieve balanced capacitor voltages, MMC should be operated in such a way that net transfer of energy to a submodule capacitor is zero over a period of time. The idea is to swap the switching/gating angles among the submodules of one arm after every fundamental cycle. For example, pre-determined gating signals G1, G2, G3 and G4 for one arm of 5L-MMC

will drive the submodules as follows: 1st cycle: SM1, SM2, SM3 and SM4, 2nd cycle: SM2, SM3, SM4 and SM1, 3rd cycle: SM3, SM4, SM1, SM2, and 4th cycle: SM4, SM1, SM2, SM3. This way, it is possible to maintain submodule capacitor voltages around their nominal value.

Table 4.3: List of components and their parameters in 5L-MMC experimental setup

DC-link voltage V_{dc}	300 V
Number of submodules per arm N_{sm}	4
Nominal capacitor voltage V_{nom}	75 V
Arm inductance	1.35 mH
Submodule capacitance	1.33 mF
Induction motor	1.5 kW, 400 V, 50 Hz
Half-bridge modules	SK30GBB066T
	$V_{CE} = 600$ V, $I_{Cnom} = 30$ A
Six-pack driver	SKHI 61R

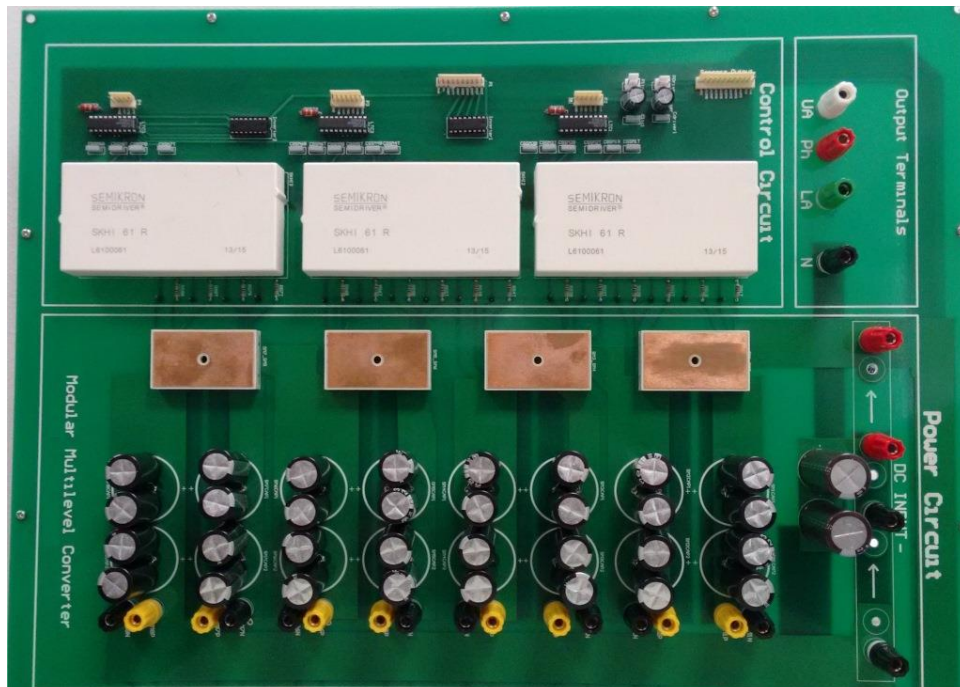


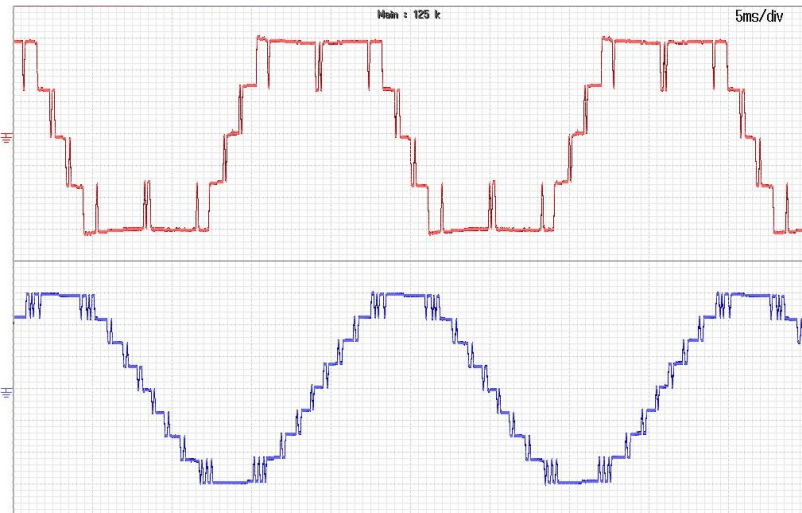
Fig. 4.5: Prototype of 5L-MMC phase leg

4.4 Experimental results

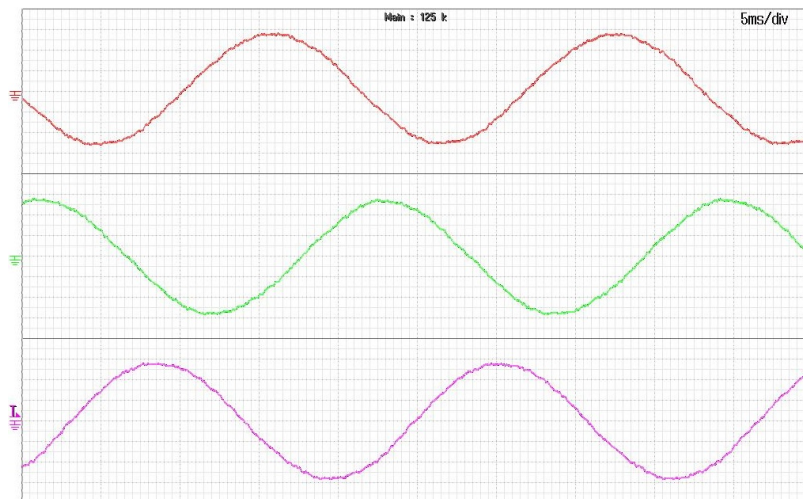
The proposed technique has been implemented for modulating 5L-MMC feeding an 1.5-kW induction motor with $f_{s,max}$ set at 200 Hz. A low power prototype of 5L-MMC phase leg has been developed with half-bridge modules from Semikron (SK30GGB066T) and six-pack IGBT driver SKHI 61R, as shown in Fig. 4.5. The list of components and their rated parameters of experimental set-up are shown in Table 4.3. The output of 5L-MMC is connected directly to induction motor without using any LC filter to get better understanding of significant harmonics in stator currents.

The optimal switching angles have been generated for three different operating points ($m=0.9216$, $N=8$), ($m=0.6667$, $N=12$), and ($m=0.4431$, $N=18$). For these three different operating points, the output phase voltage with five levels, line-to-line voltage, stator currents, and submodule capacitor voltages of upper arm of phase A are shown in Figs. 4.6 (a)-(c) to Figs. 4.8 (a)-(c), respectively. It should be observed that the machine stator currents are sinusoidal, although the device switching frequency has been limited to 200 Hz, as shown in Figs. 4.6 (b) to Figs. 4.8 (b). The SM capacitor voltages are well balanced with low voltage ripple owing to angle swapping scheme, as shown in Figs. 4.6 (c) to Figs. 4.8 (c). It should be noticed that voltage ripple increases as the value of m decreases.

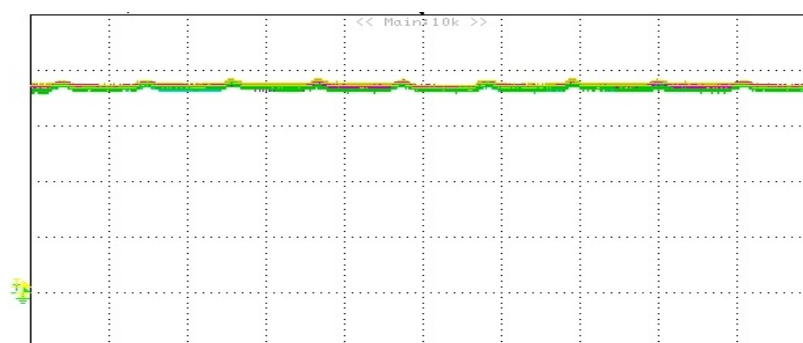
The space vector trajectories of stator currents for these three operating points are shown in Fig. 4.9 (a)-(c), respectively. The circular trajectories demonstrate low harmonic distortion of machine stator currents, although the device switching frequency has been limited to 200 Hz. In addition, FFT analysis has been performed on recorded stator currents to get better understanding of the harmonic spectrum with calculated optimal switching angles. The harmonic spectrum of stator currents for three operating points are shown in Fig. 4.10 (a)-(c), respectively. The THD of stator currents for three operating points are obtained as 2.09%, 3.09% and 3.81%,



(a)

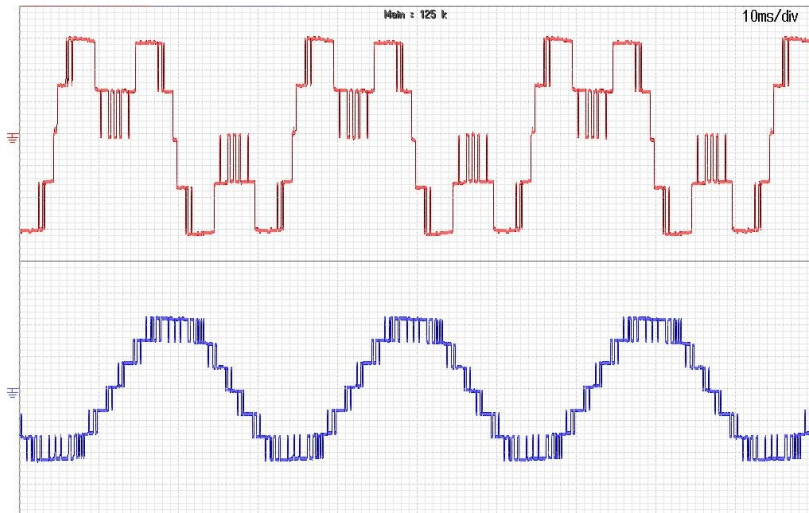


(b)

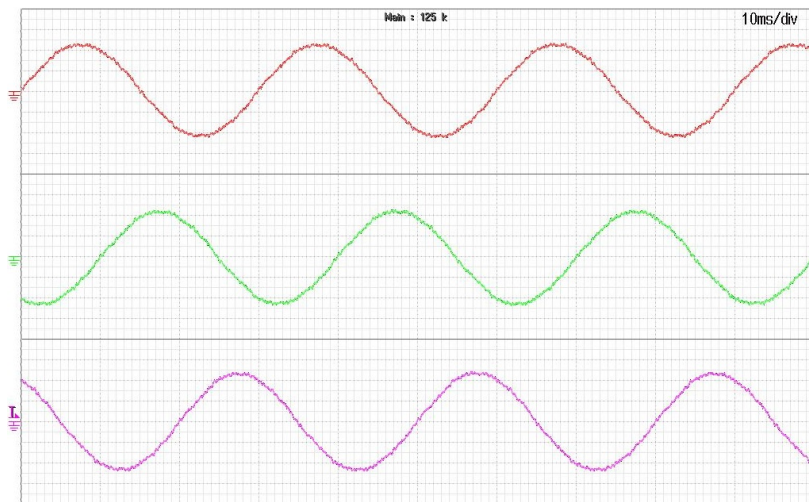


(c)

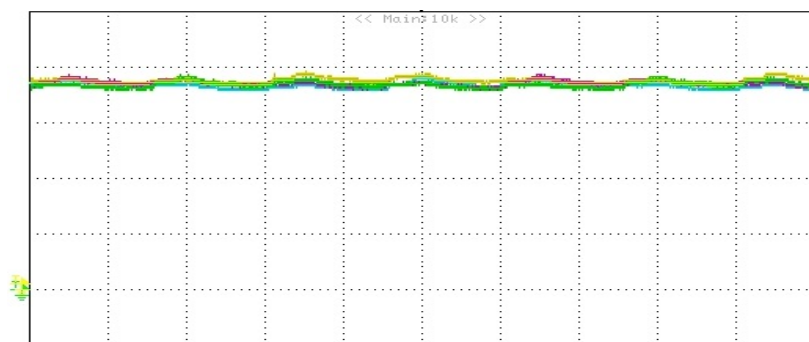
Fig. 4.6: Experimental results of 5L-MMC for ($m=0.9216$, $N=8$). X-axis: 5 ms/div. (a) Output phase and line-to-line voltage (Y-axis: 50 V/div, 100 V/div) (b) three-phase stator currents (Y-axis: 1 A/div). (c) submodule capacitor voltages of upper arm of phase A (X-Axis: 20 ms/div, Y-axis: 20 V/div)



(a)

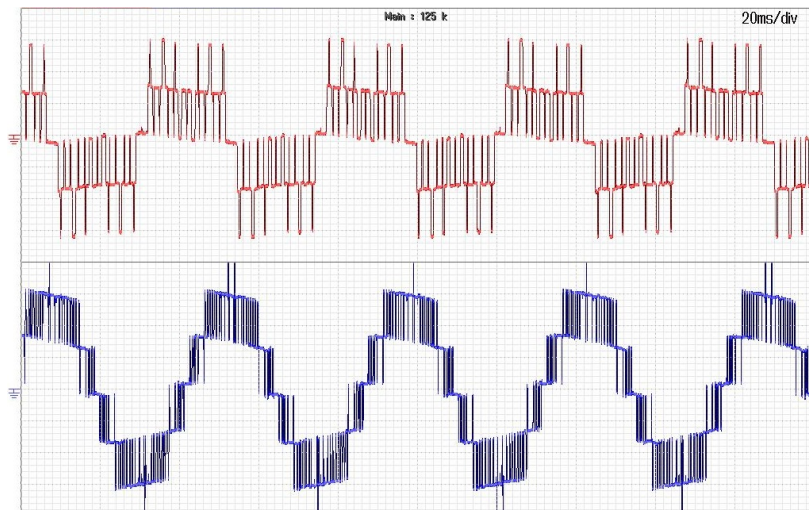


(b)

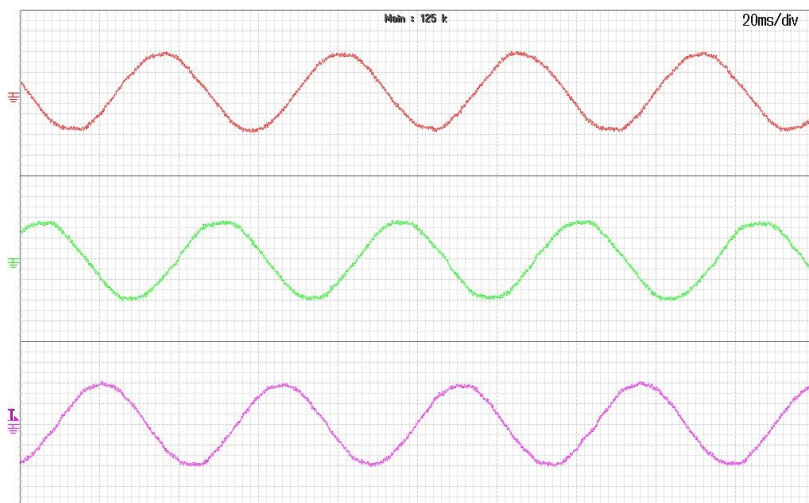


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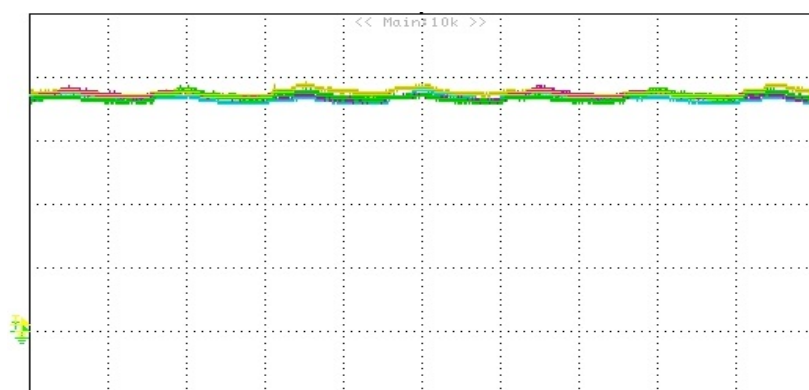
Fig. 4.7: Experimental results of 5L-MMC for ($m=0.6667$, $N=12$). X-axis: 10 ms/div. (a) Output phase and line-to-line voltage (Y-axis: 50 V/div, 100 V/div) (b) three-phase stator currents (Y-axis: 1 A/div) (c) submodule capacitor voltages of upper arm of phase A (X-Axis: 20 ms/div, Y-axis: 20 V/div)



(a)



(b)



(c)

Fig. 4.8: Experimental results of 5L-MMC for ($m=0.4431$, $N=18$). X-axis: 20 ms/div. (a) Output phase and line-to-line voltage (Y-axis: 50 V/div) (b) three-phase stator currents (Y-axis: 1 A/div)(c) submodule capacitor voltages of upper arm of phase A (X-Axis: 20 ms/div, Y-axis: 20 V/div)

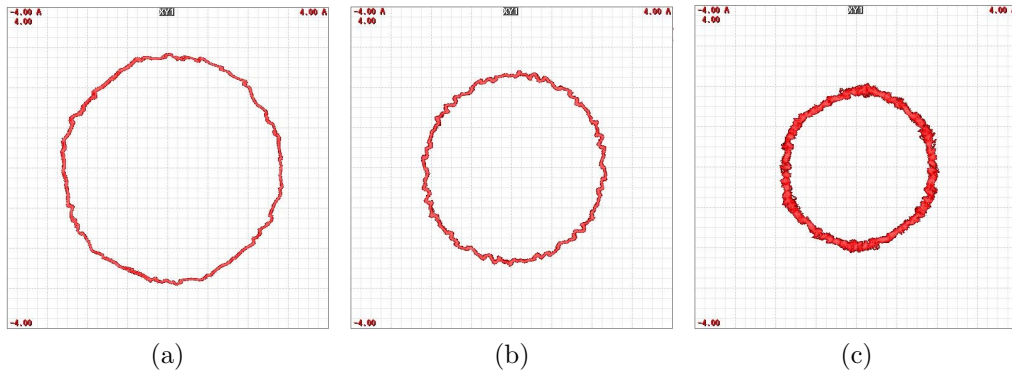
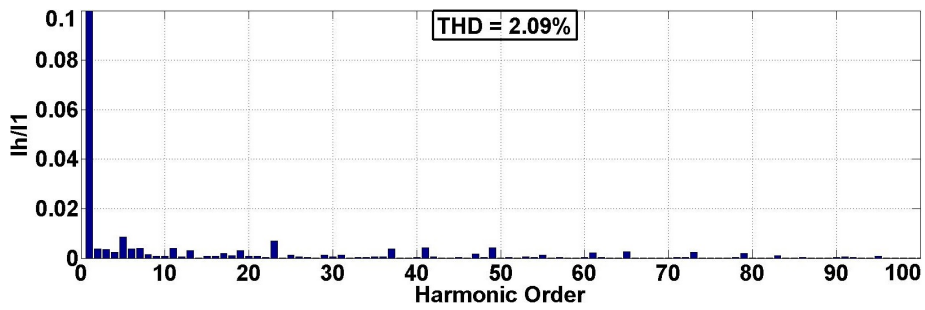
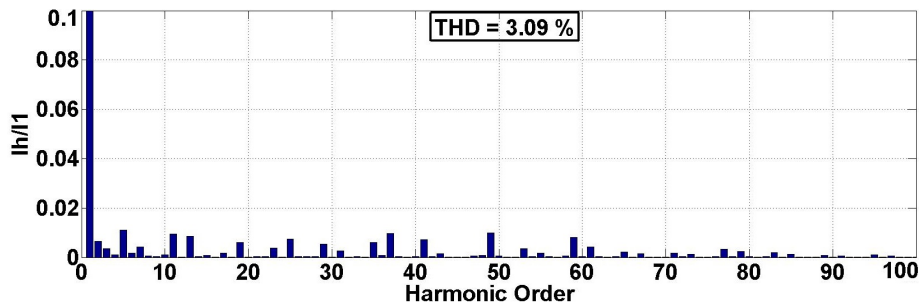


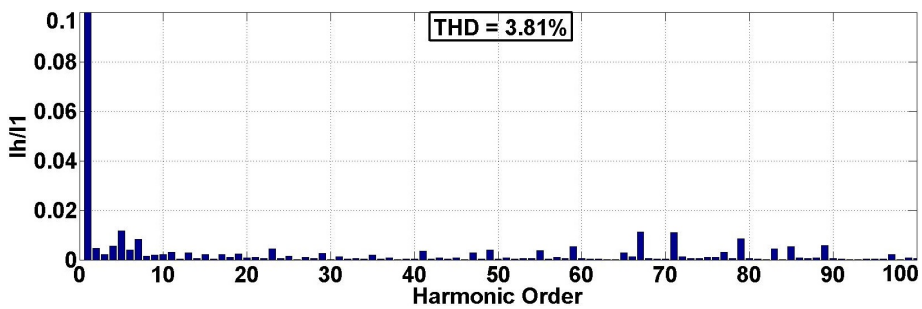
Fig. 4.9: Space vector trajectories of machine stator currents. X,Y-axis: 1 A/div (a) ($m=0.9216$, $N=8$). (b) ($m=0.6667$, $N=12$). (c) ($m=0.4431$, $N=18$)



(a)



(b)



(c)

Fig. 4.10: Harmonic spectrum of stator currents (enlarged view to show the dominant harmonic components). X-axis: Harmonic Order. Y-axis: $\frac{I_h}{I_1}$. (a) ($m=0.9216$, $N=8$). (b) ($m=0.6667$, $N=12$). (c) ($m=0.4431$, $N=18$)

respectively. Also, the enlarged view of harmonic spectrum shows that all dominant harmonic components are limited to 1% of fundamental component. From all the experimental results, it should be concluded that proposed technique modulates the 5L-MMC with $f_{s,max}$ set at 200 Hz, while minimizing the harmonic distortion of machine stator currents, and achieving balanced floating capacitor voltages.

4.5 Summary and Conclusions

Modular multilevel converters have recently found industrial relevance in medium voltage drives. The implementation of SOP for MMC topology requires the following modifications: method to estimate pulse number N at each modulation index value, and allocation of switching angles to each power semiconductor device. The optimal switching angles should be allocated to each power semiconductor device based on the following criteria: identical device switching frequency and balanced submodule capacitor voltages. An angle swapping scheme has been proposed to balance submodule capacitor voltages. The experimental results from 5L-MMC fed 1.5-kW induction motor drive validated the proposed method and demonstrated its performance.

Chapter 5

Enhanced SOP Technique for Dual Inverter Based MLC Topologies

5.1 Introduction

Dual inverter fed drives cut down the requirement of input dc sources. However, the main disadvantage of dual-inverter based MLC topologies is requirement of common-mode inductor in series with machine stator windings to suppress the zero-sequence or common-mode current components. This Chapter gives the details of proposed enhanced SOP technique for modulation of dual inverter based MLC topologies to achieve the following objectives : elimination of common-mode currents in the machine stator windings, lower harmonic distortion of machine stator currents and low device switching frequency operation. Also, an MMC based topology has been proposed for open-end stator winding induction motor drives to achieve single dc-link operation for any number of voltage levels. It should be noted that state-of-the-art dual inverter based topologies require more than one dc source for seven or higher level operation. The new topology is denoted as dual nL -MMC, where n denotes the number of voltage levels in output phase voltage of each MMC and it generates $2n$ voltage levels across stator winding voltages. This topology inherits all the advantages of MMC such as single dc source operation, scalability in terms of any voltage level

requirements, and fault-tolerant operation by using cell redundancy [168]. The proposed enhanced SOP technique has been utilized to modulate the D2L, D3L, and dual 3L-MMC topologies feeding an open-end stator winding induction motor drive.

This Chapter is organized as follows: circuit topology and operation of D2L, D3L and dual n L-MMC topologies are given in Section 5.2, details of proposed enhanced SOP technique are given in Section 5.3, experimental results for D2L, D3L and dual 3L-MMC topologies are given in Section 5.4, and the conclusions of this Chapter are given in Section 5.5.

5.2 Circuit topologies and Operation

The MLC topologies of D2L and D3L inverters feeding an open-end stator winding induction motor drive are shown in Fig. 5.1 (a)-(b), respectively. In case of D2L inverter, mid-point potential of each phase leg with respect

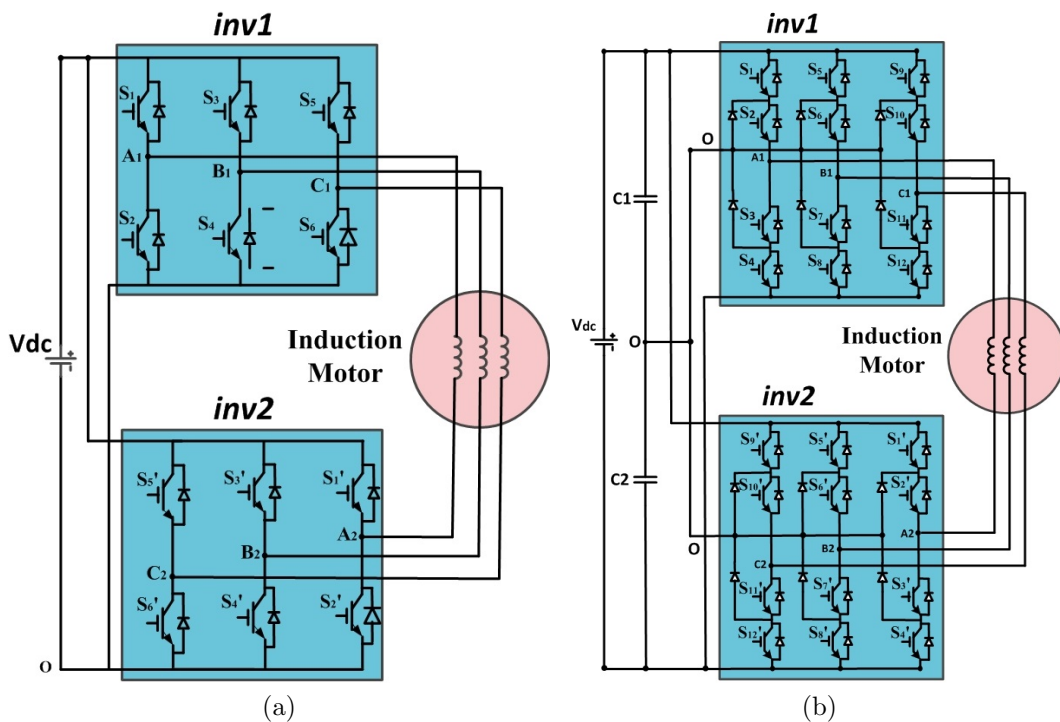


Fig. 5.1: Single dc-link dual inverter fed open-end stator winding induction motor drive. (a) D2L inverter (b) D3L inverter

to negative terminal of dc-link capacitor ‘O’ consists of two voltage levels $V_{dc}, 0$. Therefore, stator winding voltage consists of three voltage levels $-V_{dc}, 0, V_{dc}$. In case of D3L inverter, mid-point potential of each phase leg with respect to neutral-point of dc-link capacitors ‘O’ consists of three voltage levels $-V_{dc}, 0, V_{dc}$ and hence, stator winding voltages consists of five voltage levels $-2V_{dc}, -V_{dc}, 0, V_{dc}, 2V_{dc}$. More details about operation of D2L and D3L inverters can be seen in [158] and [151], respectively.

The circuit configuration of dual nL -MMC fed open-end stator winding induction motor drive is shown in Fig. 5.2. It consists of two MMCs feeding both ends of machine stator windings. The phase leg of MMC consists of two arms connected in series via arm inductors. The arm connected to positive rail is called upper arm and the arm connected to negative rail is called lower arm. Each arm consists of several submodules connected in series. The submodule consists of an half-bridge cell with a dc capacitor. Each submodule can be either inserted or bypassed by turning on top switch S1 or bottom switch S2, respectively. When a submodule is inserted, its output voltage is equal to capacitor voltage, otherwise it is equal to zero. When a submodule is inserted, its capacitor get charged or discharged depending on the direction of arm current. when a submodule is bypassed, its capacitor voltage remains constant.

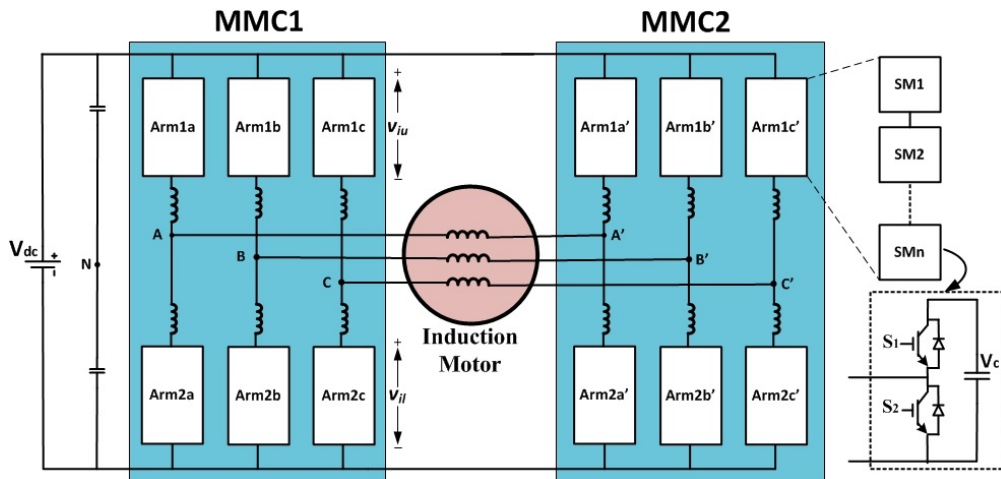


Fig. 5.2: Dual nL -MMC fed open-end stator winding IM drive

Table 5.1: Synthesis of output voltage levels in phase A of Dual 3L-MMC

N_u	N_l	N'_u	N'_l	V_{AN}	$V_{A'N}$	$V_{AA'}$
0	2	2	0	V_{nom}	$-V_{nom}$	$2V_{nom}$
0	2	1	1	V_{nom}	0	V_{nom}
1	1	2	0	0	$-V_{nom}$	V_{nom}
0	2	0	2	V_{nom}	V_{nom}	0
1	1	1	1	0	0	0
2	0	2	0	$-V_{nom}$	$-V_{nom}$	0
1	1	0	2	0	V_{nom}	$-V_{nom}$
2	0	1	1	$-V_{nom}$	0	$-V_{nom}$
2	0	0	2	$-V_{nom}$	V_{nom}	$-2V_{nom}$

The instantaneous ac-side output voltage of MMC depends on the number of SMs inserted in upper and lower arms. By varying the number of inserted SMs in a sinusoidal fashion, it is possible to generate sinusoidal output voltage. Let N_{sm} , N_u and N_l denote the total number of SMs in each arm, number of SMs inserted in upper arm, and lower arm, respectively. In general, each phase leg of MMC is controlled such that number of SMs inserted in each phase leg is equal to N_{sm} , i.e., $N_u + N_l = N_{sm}$ [168]. The nominal value of SM capacitor voltage V_{nom} should be equal to V_{dc}/N_{sm} , where V_{dc} denotes the dc input voltage. Consider a single phase leg, by neglecting the voltage drop across arm inductors, it can be shown that ac-side output voltage is equal to $\frac{1}{2}(v_{il} - v_{iu})$, where v_{iu} and v_{il} denotes the instantaneous voltages inserted in upper and lower arms, respectively [167]. The synthesis of output voltage levels for phase A of dual 3L-MMC is shown in Table 5.1. It should be observed that phase output voltage v_{AN} or $v_{A'N}$ consists of three voltage levels. The stator winding voltage is a summation of phase output voltages of two 3L-MMCs and thus, it consists of five voltage levels as shown in Table 5.1. The similar analysis can be done for any dual n L-MMC topology.

5.3 Enhanced SOP technique

The state-of-the-art SOP technique for open-end stator winding induction motor drives leads to common-mode currents in the machine stator windings. The common-mode currents are due to common-mode voltages generated in the machine stator windings [161]. A common-mode inductor is usually required in series with stator windings to suppress common-mode current components. The next question is how to modify the optimization algorithm so that optimal stator voltage waveforms does not have common-mode voltages. According to Fourier analysis, common-mode voltages consists only third order harmonic components. One possible method to eliminate all third order harmonic components is to include corresponding non-linear constraints in optimization algorithm. However, this might lead to poor performance of optimization algorithm. Therefore, it is better to utilize some symmetry conditions to achieve the objective of eliminating third order harmonic components. A well known fact from Fourier series analysis is that a waveform does not have third order harmonic components if it is obtained by subtracting two similar waveforms that are 120° phase apart. Therefore, it is possible to cancel the common-mode voltages generated across the stator winding by utilizing the same optimal switching angles for $inv1$ and $inv2$ but with 120° phase-shift. Basically, optimization algorithm should generate switching angles for $inv1$ and these switching angles should be phase-shifted by 120° to modulate $inv2$.

Another way of understanding common-mode voltage generation in stator winding is through voltage space vector concept. Let $cmv1$, $cmv2$ represents the common-mode voltages generated by voltage space vectors of $inv1$ and $inv2$, respectively, and $cmv = cmv1 - cmv2$ denotes the common-mode voltage generated across stator winding. If the voltage space vectors are selected such that $cmv1 = cmv2$, then common-mode voltage become zero in the stator winding and hence, common-mode current components

can be eliminated. For simplicity, let us consider voltage space vectors of classical 2L inverter, as shown in Fig. 5.3. It should be observed that, common-mode voltage generated by voltage space vectors 1, 3 and 5 that are 120° phase apart, are equal to $\frac{V_{dc}}{3}$. Similarly, the common-mode voltages generated by voltage space vectors 2, 4 and 6 that are 120° phase apart, are equal to $\frac{2V_{dc}}{3}$. Therefore, by choosing the voltage space vectors for *inv1* and *inv2* that are 120° phase apart, it is possible to cancel the common-mode voltages generated across the phase windings. Based on the Fourier analysis and voltage space vector concept, it should be concluded that common-mode voltages in stator winding can be eliminated by utilizing same switching pattern with 120° phase-shift for two inverters. This idea has been utilized to enhance state-of-the-art SOP technique for dual inverter based MLC topologies feeding open-end stator winding induction motor drives.

The three sequential steps of basic SOP technique for each discrete value of m are as follows: determine value of N such that f_s is limited to $f_{s,max}$, perform optimization to pre-determine switching angles for each steady-state operating point (m,N) that minimize d , and allocation of op-

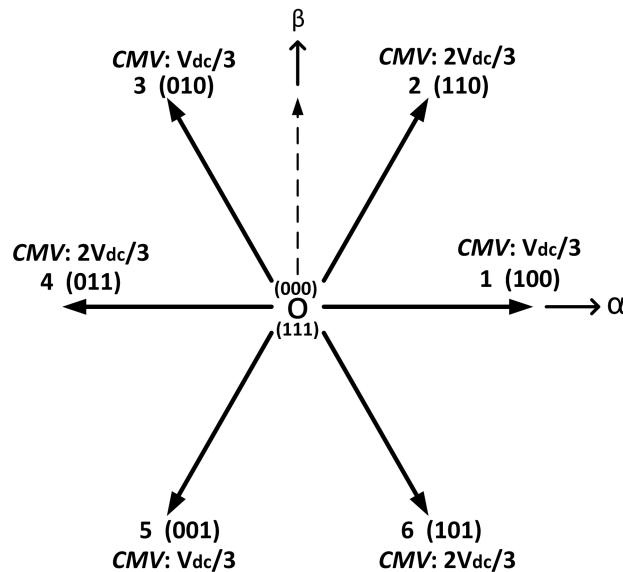


Fig. 5.3: Voltage space vectors for 2L inverter

timal switching angles to each power semiconductor device. In case of dual inverter based MLC topologies, state-of-the-art SOP technique generates optimal switching angles for stator winding voltages. On the contrary, proposed enhanced SOP technique generates optimal switching angles for output phase voltages of one of the two inverters and switching angles for other inverter will be obtained by adding 120° phase shift. Apart from this, all other details will remain the same as generalized SOP technique. More details about each step for D2L, D3L and dual nL -MMC are given next.

5.3.1 Computation of pulse number N

5.3.1.1 D2L inverter

The output potential waveform of classical 2L inverter is shown in Fig. 5.4. Let the pulse number for 2L inverter is denoted as N_{2L} and then, it can be shown that the total number of switching angles in one fundamental cycle will be equal to $4N_{2L} + 2$. For example, it should be observed from Fig. 5.4 that N_{2L} is equal to 3, i.e., α_1 to α_3 and the total number of switching angles are equal to 14, i.e., $0, \pi, \alpha_1$ to α_{12} . At each switching angle, both the semiconductor devices in a phase leg undergo commutation, for

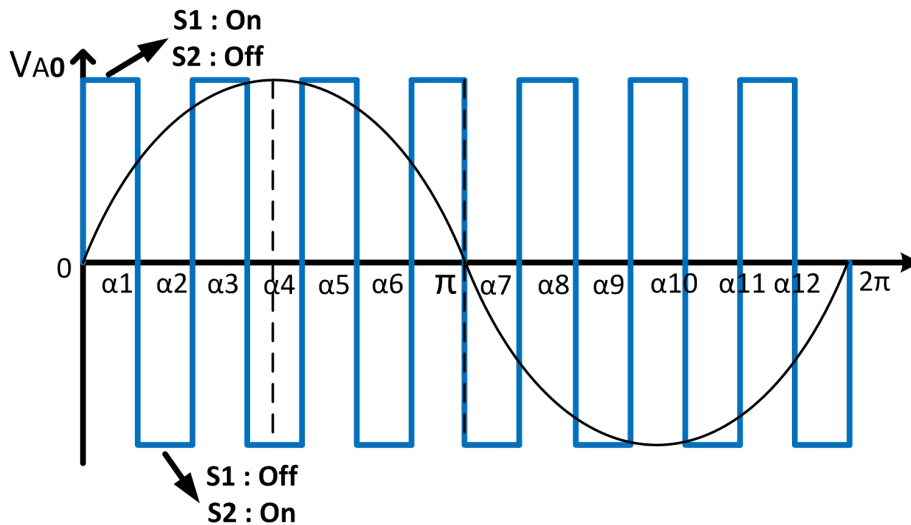
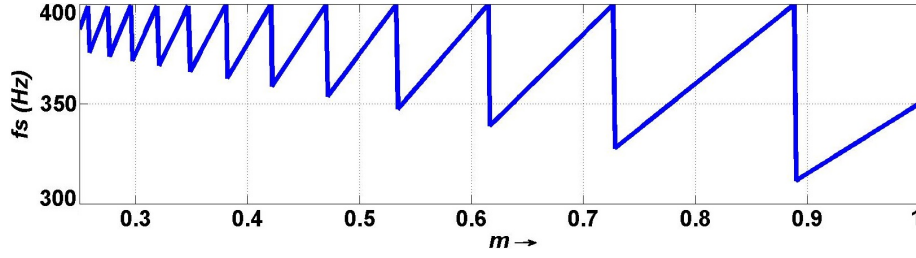


Fig. 5.4: Phase output voltage of 2L inverter

Table 5.2: SOP of D2L inverter at $f_{s,max} = 400$ Hz : Computed pulse number and corresponding f_s for a given value of m

m	$f_1(Hz)$	N_{2L1}	N_{2L2}	N_{D2L}	$f_s(Hz)$
0.889 - 1.000	44.49 - 50.00	3	3	6	311.46 - 350
0.728 - 0.888	36.41 - 44.44	4	4	8	327.73 - 400
0.616 - 0.727	30.82 - 40.00	5	5	10	339.01 - 400
0.534 - 0.615	26.72 - 30.77	6	6	12	347.32 - 400
0.471 - 0.533	23.58 - 26.67	7	7	14	353.69 - 400

Fig. 5.5: SOP of D2L inverter at $f_{s,max} = 400$ Hz : f_s versus m

example, S_1 is turned-off and S_2 is turned-on at α_1 , as shown in Fig. 5.4. Therefore, the total number of commutations of each semiconductor device are equal to $4N_{2L} + 2$ and hence, the device switching frequency f_s of the 2L inverter is equal to $(2N_{2L} + 1)f_1$. Then, the value of N_{2L} for a desired value of $f_{s,max}$ is obtained as,

$$N_{2L} = \text{floor} \left(\frac{f_{s,max} - f_1}{2f_1} \right) = \text{floor} \left(\frac{f_{s,max} - m \cdot f_{1R}}{2 \cdot m \cdot f_{1R}} \right) \quad (5.1)$$

The goal is to operate D2L inverter with $f_{s,max}$ set at 400 Hz. Let N_{2L1} , N_{2L2} , and N_{D2L} denote pulse number for phase output voltages of two 2L inverters and stator winding voltage, respectively. Based on (5.1), values of N_{2L1} , N_{2L2} , and N_{D2L} are estimated for each value of m , as shown in Table 5.2. Based on the computed values of pulse number, estimated value of f_s for different values of m is shown in Fig. 5.5. It should be observed that device switching frequency is limited to 400 Hz for each value of m .

5.3.1.2 D3L inverter

The output potential waveform of 3L-NPC inverter is shown in Fig. 5.6. Let the pulse number of phase output voltage of 3L-NPC inverter is denoted as N_{3L} and then, the total number of switching angles in one fundamental cycle should be equal to $4N_{3L}$. For example, it should be observed from Fig. 5.6 that N_{3L} is equal to 3, i.e., α_1 to α_3 and the total number of switching angles are equal to 12, i.e., α_1 to α_{12} . At each switching angle, only two switches in a phase leg undergo commutation. For example, S_1 is turned-off and S_3 is turned-on at α_2 , whereas S_2 is turned-on and S_4 is turned-off at α_8 , as shown in Fig. 5.6. Therefore, total number of commutations of each semiconductor device is equal to $2N_{3L}$ and hence, the device switching frequency f_s of the 3L-NPC inverter is equal to $N_{3L}f_1$. Then, the value of N_{3L} for a desired value of $f_{s,max}$ is obtained as,

$$N_{3L} = \text{floor} \left(\frac{f_{s,max}}{f_1} \right) = \text{floor} \left(\frac{f_{s,max}}{m \cdot f_{1R}} \right). \quad (5.2)$$

The goal is to operate D3L inverter with $f_{s,max}$ equal to 200 Hz. Let N_{3L1} , N_{3L2} , and N_{D3L} denote pulse number for phase output voltages of two 3L-NPC inverters and stator winding voltage, respectively. Their values

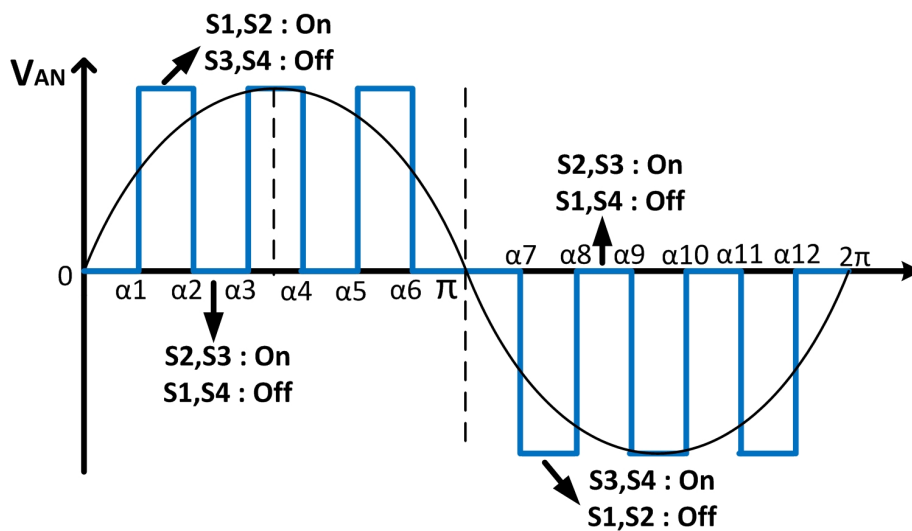
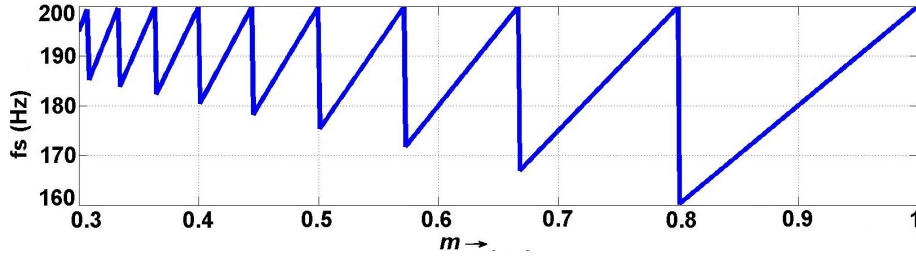


Fig. 5.6: Phase output voltage of 3L-NPC inverter

Table 5.3: SOP of D3L inverter at $f_{s,max} = 400$ Hz : Computed pulse number and corresponding f_s for a given m

m	$f_1(Hz)$	N_{3L1}	N_{3L2}	N_{D3L}	$f_s(Hz)$
0.801 - 1.000	40.05 - 50.00	4	4	8	160.20 - 200
0.667 - 0.800	33.38 - 40.00	5	5	10	166.90 - 200
0.572 - 0.667	28.62 - 33.33	6	6	12	171.73 - 200
0.501 - 0.571	25.05 - 28.57	7	7	14	175.35 - 200
0.445 - 0.500	22.27 - 25.00	8	8	16	178.17 - 200

Fig. 5.7: SOP of D3L inverter at $f_{s,max} = 200$ Hz : f_s versus m

can be calculated based on (5.2) for each value of m , as shown in Table 5.3. With the computed values of pulse number, the estimated value of f_s for different values of m is shown in Fig. 5.7. It should be observed that device switching frequency is limited to 200 Hz for each value of m .

5.3.1.3 Dual nL -MMC topology

Consider an nL -MMC that has to be operated with f_s limited to $f_{s,max}$. Let the ratio between $f_{s,max}$ and f_1 be denoted as R_f . As the SOP technique demands that R_f should be an integer, the following relationship should be satisfied,

$$R_f = \text{floor} \left(\frac{f_{s,max}}{f_1} \right) = \text{floor} \left(\frac{f_{s,max}}{m \cdot f_{1R}} \right), \quad (5.3)$$

where, the function ‘*floor*’ returns largest previous integer. Then, the total number of commutations in one arm, which contains $(n-1)$ submodules

should be equal to $(n-1)*2*R_f$. Finally, the value of N_{nLM} is obtained as,

$$\begin{aligned} N_{nLM} &= \frac{(n-1) * 2R_f}{4} \\ &= \frac{(n-1)}{2} * \text{floor} \left(\frac{f_{s,max}}{m \cdot f_{1R}} \right). \end{aligned} \quad (5.4)$$

The goal of our study is to modulate 3L-MMC with $f_{s,max}$ set at 400 Hz. Based on (5.4), the estimated value of N_{3LM} and corresponding f_s for different values of m are shown in Table 5.4 as well as Fig. 5.8. It should be observed that device switching frequency is limited to 400 Hz for each value of m .

Table 5.4: SOP of 3L-MMC with $f_{s,max} = 400$ Hz : Estimated value of N_{3LM} and corresponding f_s for a given m

m	$f_1(\text{Hz})$	N_{3LM}	$f_s(\text{Hz})$
0.890 - 1.000	44.50 - 50.00	8	356.00 - 400
0.801 - 0.889	40.05 - 44.45	9	360.45 - 400
0.728 - 0.800	36.40 - 40.00	10	364.00 - 400
0.668 - 0.727	33.40 - 36.35	11	367.40 - 400
0.616 - 0.667	30.80 - 33.35	12	369.60 - 400
0.572 - 0.615	28.60 - 30.75	13	371.80 - 400
0.534 - 0.571	26.70 - 28.55	14	373.80 - 400
0.501 - 0.533	25.05 - 26.65	15	375.75 - 400

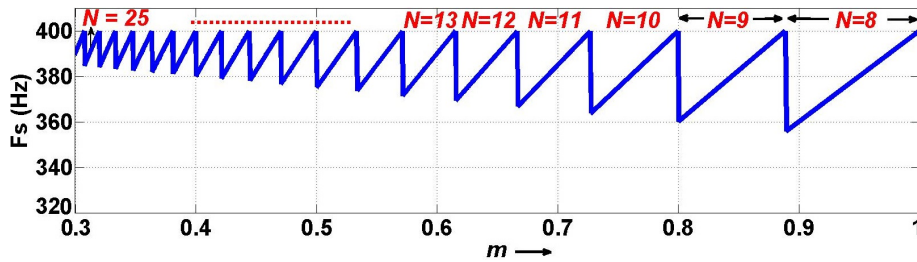


Fig. 5.8: SOP of 3L-MMC with $f_{s,max} = 400$ Hz : Estimated pulse number N and corresponding f_s for a given m

5.3.2 Optimization of Switching Angles

After determining the pulse number for each discrete value of m , the next step is to perform optimization of switching angles at each steady state operating point (m, N) in order to minimize the harmonic distortion of converter output current. As explained earlier, optimization is performed to compute switching angles of one of the two inverters, i.e., 2L or 3L-NPC or n L-MMC. The procedure for deriving expression of d remains the same as shown in Section 2.4. The final expressions of d_{2L} , d_{3L} , and d_{3LM} for 2L, 3L-NPC, and 3L-MMC are obtained as follows,

$$d_{2L} = \frac{\sqrt{\sum_k \left(\frac{1}{k^4}\right) \left(1 + \sum_{i=1}^{N_{2L}} s(i) \cos(k\alpha_i)\right)^2}}{\sqrt{\sum_k \left(\frac{1}{k^4}\right)}} \quad (5.5)$$

$$d_{3L} = \frac{\sqrt{\sum_k \left(\frac{1}{k^4}\right) \left(\sum_{i=1}^{N_{3L}} s(i) \cos(k\alpha_i)\right)^2}}{\sqrt{\sum_k \left(\frac{1}{k^4}\right)}} \quad (5.6)$$

$$d_{3LM} = \frac{\sqrt{\sum_k \left(\frac{1}{k^4}\right) \left(\sum_{i=1}^{N_{3LM}} s(i) \cos(k\alpha_i)\right)^2}}{\sqrt{\sum_k \left(\frac{1}{k^4}\right)}} \quad (5.7)$$

As the induction motor is operated at constant v/f control mode, the constraint on switching angles for 2L, 3L-NPC, and 3L-MMC are obtained as follows,

$$m_{2L} = 1 + \sum_{i=1}^{N_{2L}} s(i) \cos(\alpha_i) \quad (5.8)$$

$$m_{3L} = \sum_{i=1}^{N_{3L}} s(i) \cos(\alpha_i) \quad (5.9)$$

$$m_{3LM} = \sum_{i=1}^{N_{3LM}} s(i) \cos(\alpha_i) \quad (5.10)$$

The optimization algorithm is implemented using MATLAB. The details of optimization algorithm remains the same as reported in Section 2.4.2. Optimization results for D2L, D3L, and dual 3L-MMC topologies

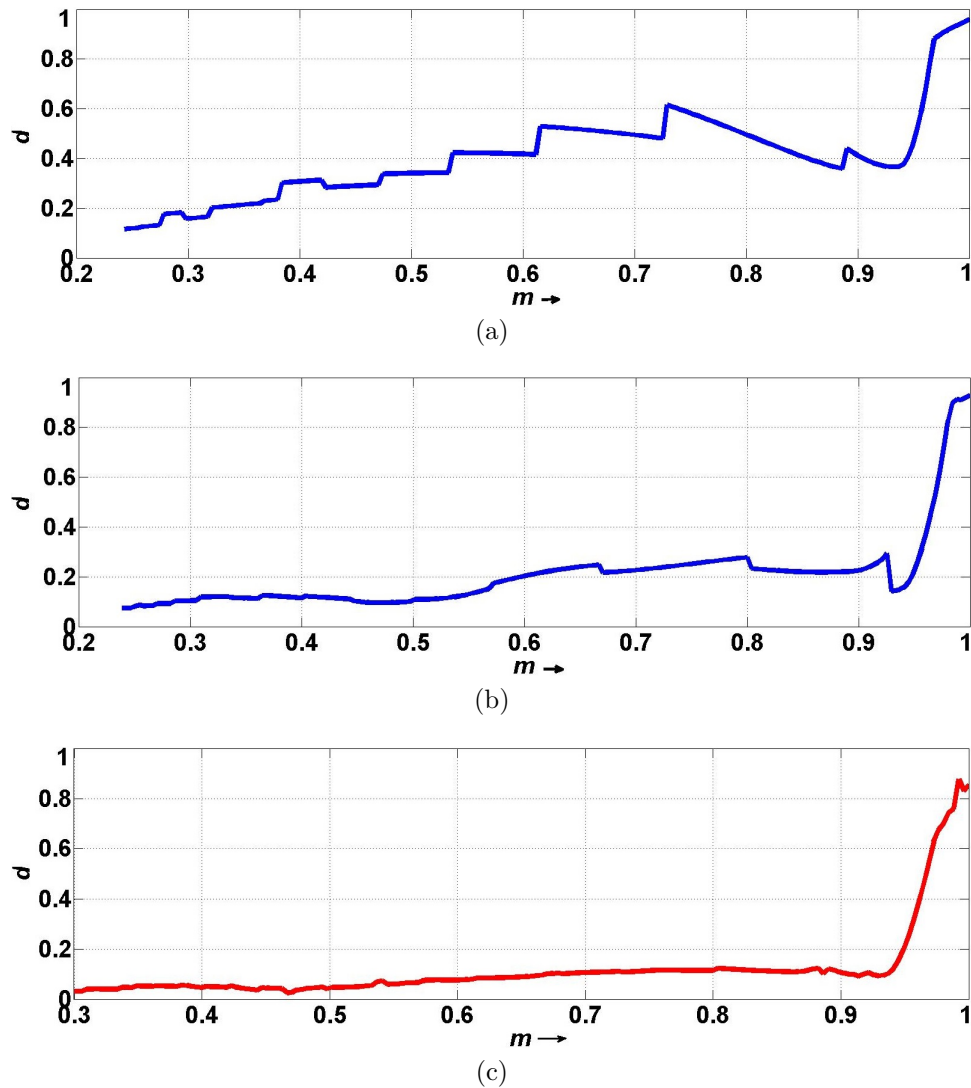


Fig. 5.9: Optimization results in terms of d versus m : (a) D2L inverter (b) D3L inverter (c) Dual 3L-MMC

are shown in Fig. 5.9 (a)-(c), respectively. It should be observed that performance of a D3L and dual 3L-MMC inverters are always better than a D2L inverter due to higher number of voltage levels. It should be observed that harmonic distortion has been reduced significantly except at higher modulation index values ($m > 0.93$), where inverter approaches six-step operation.

5.3.3 Allocation of Optimal Switching Angles

During optimization, the switching patterns of $inv1$ in phase A are determined for a quarter period. The complete switching pattern of phase A

is obtained by utilizing half-wave and quarter-wave symmetries. In order to eliminate the common-mode voltages and currents, the switching angles of $inv2$ in phase A are obtained by adding 120° phase-shift to switching angles of $inv1$ in phase A. The switching patterns for the other two phases are obtained by shifting the phase A switching pattern by 120° and 240° , respectively. Then, optimal switching angles should be assigned to each power semiconductor device while achieving identical switching frequency for all power semiconductor devices.

In case of dual nL -MMC, an algorithm has been developed to select submodules that needs to be inserted/bypassed based on the optimal switching angles, while achieving identical device switching frequency. However, the submodule capacitor voltages get diverged as shown in Fig. 5.10. The reason is that charging and discharging of submodule capacitor voltages depends on the magnitude and direction of arm current as well as the duration for which the submodule is inserted. Therefore, it is never possible to achieve balanced capacitor voltages with pre-assigned switching angles to insert/bypass submodules. Therefore, swapping technique has been utilized to maintain capacitor voltages around their nominal value.

Swapping technique: During one fundamental cycle, a certain energy transfer takes place between submodule capacitor and converter that depends on direction and magnitude of arm current and duration of submodule insertion. The capacitor voltages get charged if the net energy transfer is positive, whereas capacitor voltages get discharged if net energy

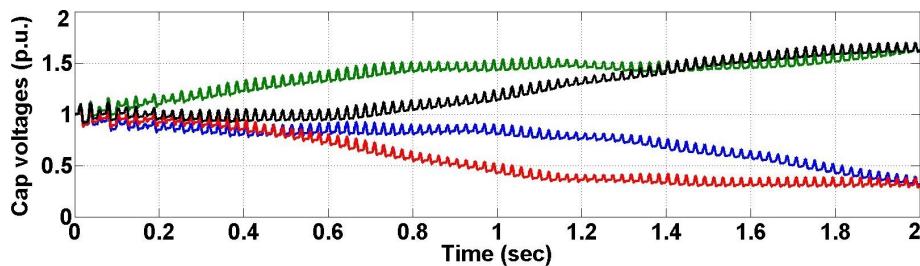


Fig. 5.10: Submodule capacitor voltages (p.u.) of 3L-MMC phase leg with pre-assigned switching angles

transfer is negative in one fundamental cycle. Thus, the submodule capacitor voltages either continuously increase or decrease over a period of time due to pre-assigned switching angles, as shown in Fig. 5.10. In order to maintain capacitor voltages around their nominal value, MMC should be operated in such a way that net transfer of energy to a submodule capacitor is zero over a period of time. The idea is to swap the switching angles among the submodules of one arm after every fundamental cycle. For example, pre-determined gating signals G1, G2 for 3L-MMC will drive the submodules as follows: 1st cycle: SM1, SM2, 2nd cycle: SM2, SM1. In this way, it is possible to maintain submodule capacitor voltages around their nominal value.

5.4 Experimental results

The proposed SOP technique has been implemented for modulating D2L, D3L and dual 3L-MMC topologies feeding an 1.5-kW open-end stator winding induction motor drive. The list of components and their parameters are shown in Table 5.4. Experimental laboratory prototype of D2L and D3L inverters for one of the three phases is shown in Fig. 5.11. The output terminals of this PCB should be connected to one of the stator windings of induction motor drive. The DC input voltages to D2L and D3L inverters are maintained at 70 V and 60 V, respectively. The output of D2L and D3L inverters is directly connected to induction motor without using any filter to get better understanding of significant harmonics in machine stator currents with optimal switching patterns. The induction motor is coupled to a separately excited DC generator and its output is connected to a fixed resistive load.

Table 5.5: List of components and their parameters in the experimental set-up of D2L and D3L inverters

Components	Parameters
Induction motor	1.5 kW, 400 V, 50 Hz
Six-pack driver	SKHI 61R
3L-NPC module	F3L30R06W1E3.B11 $V_{CE} = 600$ V, $I_{Cnom} = 30$ A
Six-pack Module	FS30R06W1E3 $V_{CE} = 600$ V, $I_{Cnom} = 30$ A
Half-bridge Modules	SK30GBB066T $V_{CE} = 600$ V, $I_{Cnom} = 30$ A

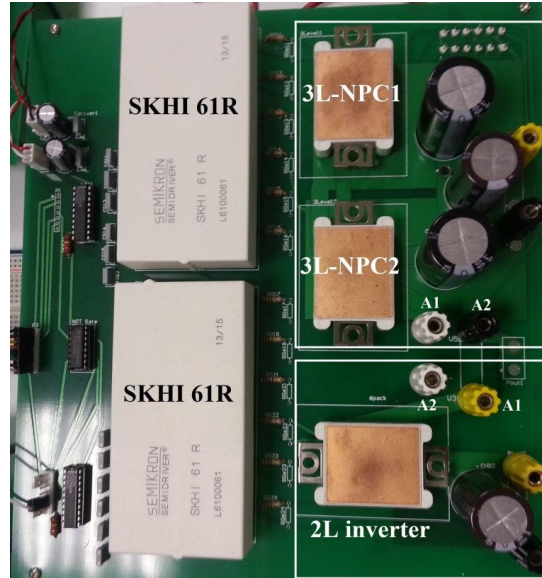
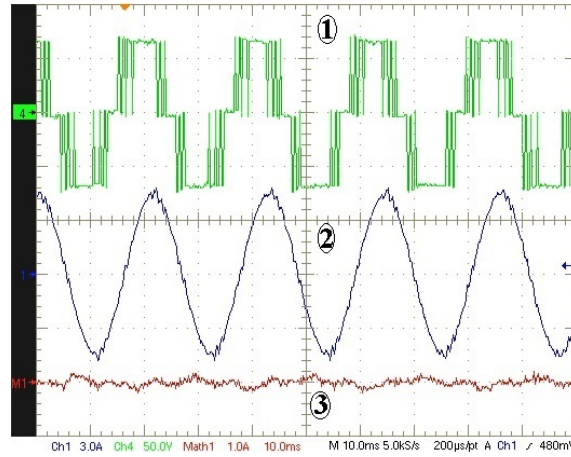


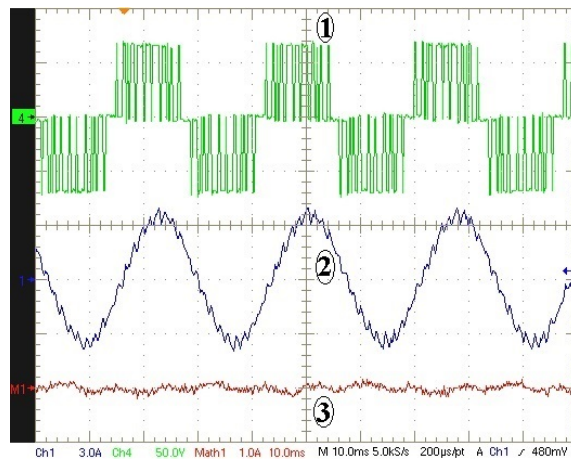
Fig. 5.11: Prototype of D2L and D3L inverters for one of the three-phases

5.4.1 D2L Inverter

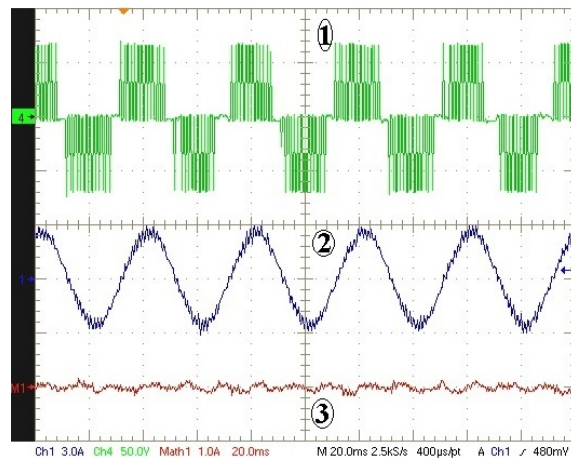
Optimal switching angles have been generated for three operating points ($m=0.9333$, $f_1=46.67$ Hz, $N=6$), ($m=0.7255$, $f_1=36.275$ Hz, $N=10$) and ($m=0.5020$, $f_1=25.1$ Hz, $N=14$) based on the proposed SOP technique. For each operating point, the machine stator winding voltage, stator current, and zero-sequence current are shown in Fig. 5.12 (a)-(c), respectively. The phase voltages consist of 3L waveforms and stator currents are sinusoidal. The zero-sequence current components are calculated by using relation $(i_a + i_b + i_c)/3$ and it should be observed that they are almost eliminated.



(a)



(b)



(c)

Fig. 5.12: Experimental results of D2L inverter : machine stator voltage ① (Y-axis:50 V/div), stator current ② (Y-axis:4 A/div), and zero-sequence current ③ (Y-axis:1 A/div). (a) ($m=0.9333$, $N=6$). X-axis:10 ms/div. (b) ($m=0.7255$, $N=10$). X-axis:10 ms/div. (c) ($m=0.5020$, $N=14$). X-axis:20 ms/div.

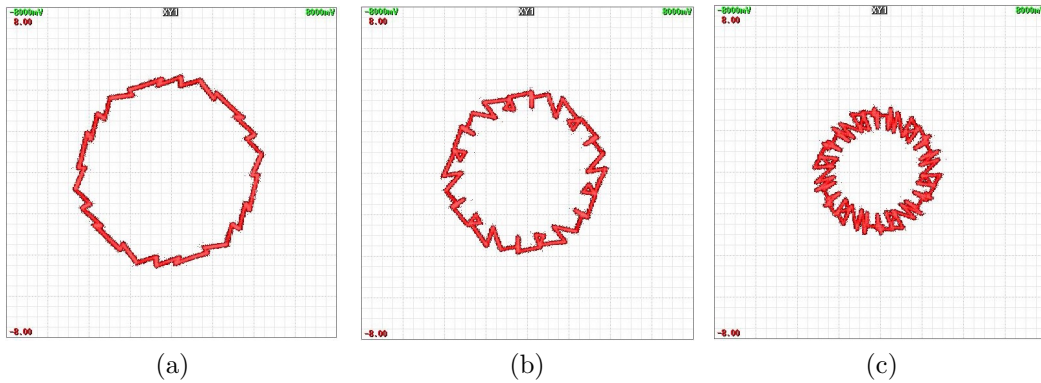
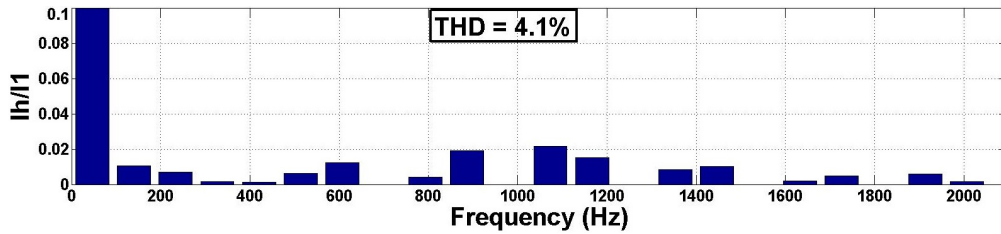
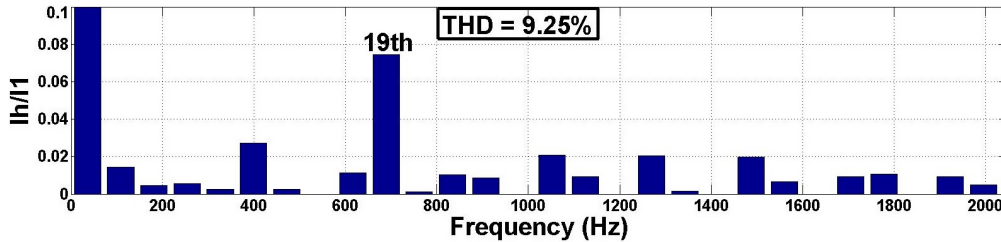


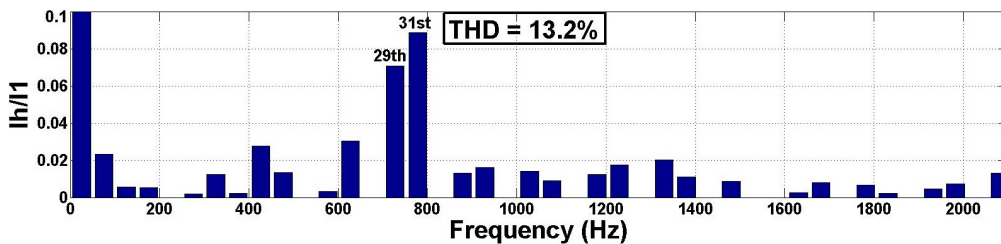
Fig. 5.13: Experimental results of D2L inverter : Stator current space vector trajectories. X-axis, Y-axis: 2 A/div (a) ($m=0.9333$, $N=6$) (b) ($m=0.7255$, $N=10$) (c) ($m=0.5020$, $N=14$)



(a)



(b)



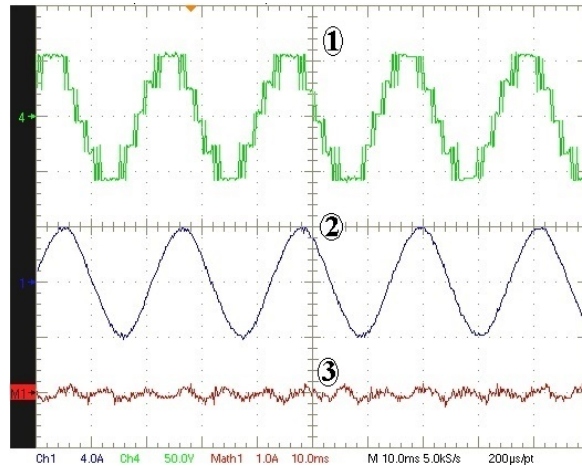
(c)

Fig. 5.14: Experimental results of D2L inverter : Harmonic spectrum of stator currents (enlarged view to show the dominant harmonic components). X-axis: Frequency (Hz). Y-axis: $\frac{I_h}{I_1}$. (a) ($m=0.9333$, $N=6$) (b) ($m=0.7255$, $N=10$) (c) ($m=0.502$, $N=14$)

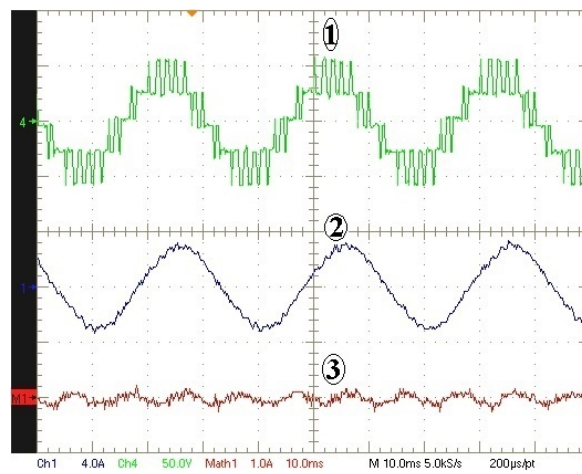
The space vector trajectories of stator currents corresponding to three operating points are shown in Fig. 5.13 (a)-(c), respectively. The nearly circular trajectories demonstrate low THD, while device switching frequency is limited to 400 Hz. It should be observed that harmonic distortion increases at lower values of modulation index. In addition, FFT analysis is performed on stator currents recorded into a PC by using data acquisition system. The current harmonic spectrum for operating point ($m=0.9333$, $N=6$) is displayed in Fig. 5.14 (a). It can be observed that THD of stator currents is equal to 4.1% with all the significant harmonics below 2% of fundamental. For operating point ($m=0.7255$, $N=10$), THD of stator currents is equal to 9.25% as shown in Fig. 5.14 (b) with one significant harmonic (19^{th}) of magnitude equal to 7.5% of fundamental. Similarly, for operating point ($m=0.502$, $N=14$), THD of stator currents is equal to 13.2% as shown in Fig. 5.14 (c) and there are two significant harmonics (29^{th} and 31^{st}) with magnitude equal to 7% and 8.9% of fundamental. The THD of stator currents seems significant for operating point ($m=0.5020$, $N=14$), but this is due to harmonics of higher order, which can be attenuated easily by using LC filter at the inverter output. Therefore, it should be concluded that proposed SOP technique eliminates common-mode currents while minimizing the harmonic distortion of machine stator currents.

5.4.2 D3L Inverter

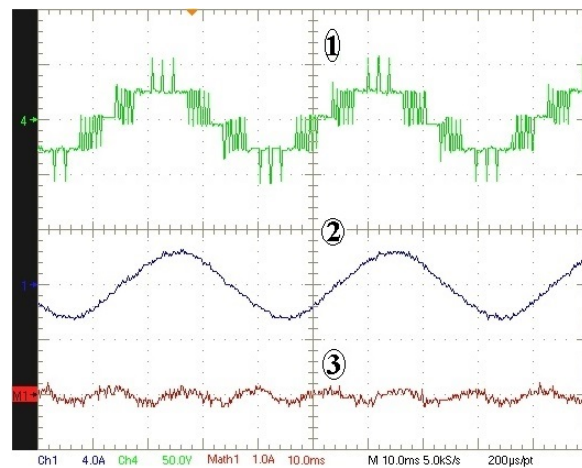
To demonstrate the performance of proposed SOP technique, three operating points ($m=0.9294$, $f_1=46.47$ Hz, $N=8$), ($m=0.6667$, $f_1=33.33$ Hz, $N=12$) and ($m=0.5098$, $f_1=25.49$ Hz, $N=14$) have been selected. For each operating point, the machine stator winding voltage, stator current, and zero-sequence current are shown in Fig. 5.15 (a)-(c), respectively. The stator voltage consists of 5L waveforms and stator currents are sinusoidal. The improvement in THD of stator currents compared to D2L inverter can



(a)



(b)



(c)

Fig. 5.15: Experimental results of D3L inverter : machine stator voltage ① (Y-axis:50 V/div), stator current ② (Y-axis:4 A/div), and zero-sequence current ③ (Y-axis:1 A/div). X-axis:10 ms/div. (a) ($m=0.9294$, $N=8$). (b) ($m=0.6667$, $N=12$). (c) ($m=0.5098$, $N=14$).

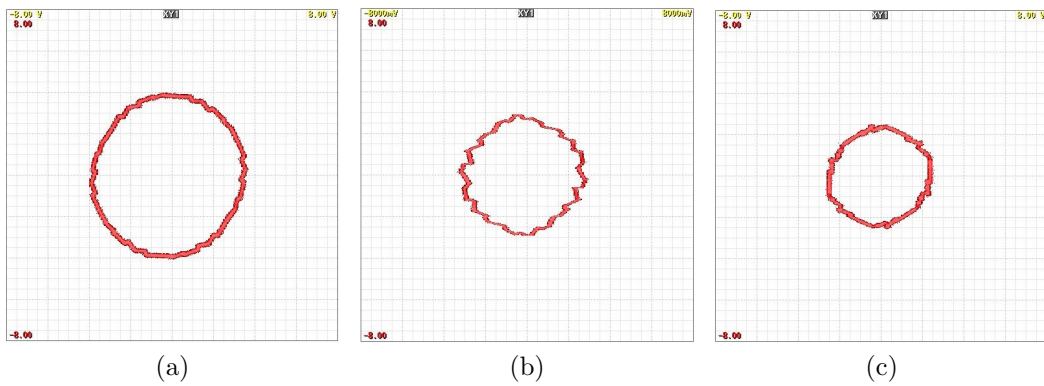
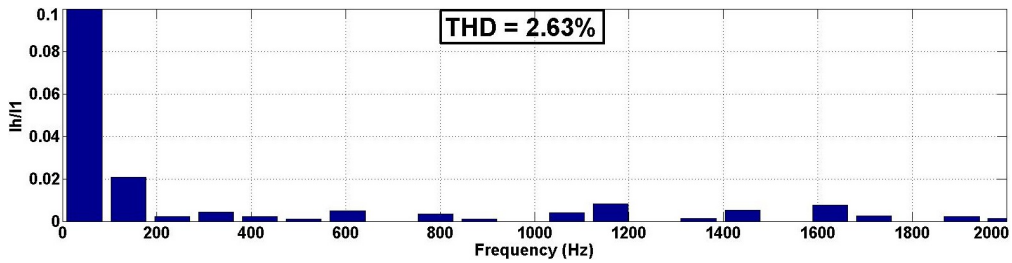
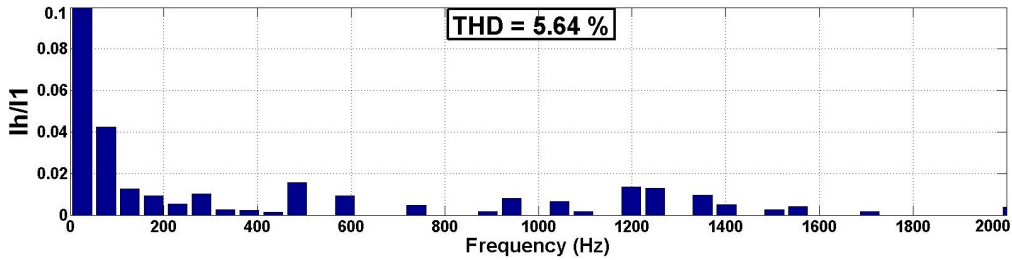


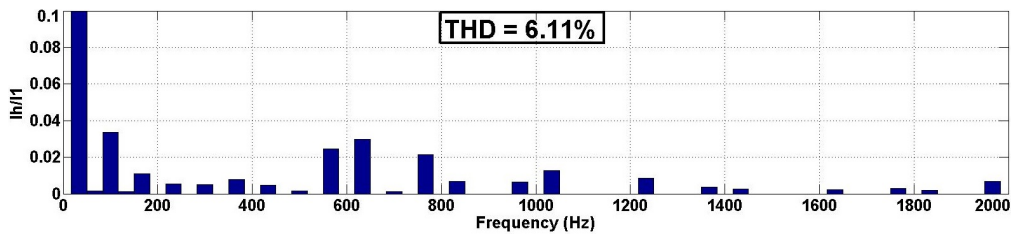
Fig. 5.16: Experimental results of D3L inverter : Stator current space vector trajectories. X-axis, Y-axis: 2 A/div (a) ($m=0.9294$, $N=8$) (b) ($m=0.667$, $N=12$) (c) ($m=0.5098$, $N=14$)



(a)



(b)



(c)

Fig. 5.17: Experimental results of D3L inverter : Harmonic spectrum of stator currents (enlarged view to show the dominant harmonic components). X-axis: Frequency (Hz). Y-axis: $\frac{I_h}{I_1}$. (a) ($m=0.9294$, $N=8$) (b) ($m=0.667$, $N=12$) (c) ($m=0.5098$, $N=14$)

be observed. The zero-sequence current components are almost eliminated. It should be noted that, the stator currents in each phase might differ in magnitude due to unequal winding resistances and inductance values and hence, there exist small zero-sequence current.

The space vector trajectories of stator currents corresponding to three operating points are shown in Fig. 5.16 (a)-(c), respectively. The nearly circular trajectories demonstrate low THD, while maximum device switching frequency is limited to 200 Hz. In addition, FFT analysis was performed on recorded stator currents. It can be observed from Fig. 5.17 (a)-(c) that the THD of stator currents for three operating points are equal to 2.63%, 5.64% and 6.11%, respectively. Due to 5L stator voltage waveforms in D3L inverter, better quality of stator current waveforms are achieved even with half of the device switching frequency compared to D2L inverter.

5.4.3 Dual 3L-MMC

The proposed SOP technique has been implemented for modulating dual 3L-MMC feeding an 1.5-kW open-end stator winding induction motor. Half-bridge modules from Semikron (SK30GBB066T) have been used for building low power prototype of dual 3L-MMC topology. Low power prototype of MMC for one of the three phases is shown in Fig. 5.18. The output terminals of this PCB should be connected to one phase open-end stator winding of induction motor drive. The system parameters of dual 3L-MMC prototype are shown in Table 5.6.

Table 5.6: Experimental parameters of dual 3L-MMC

DC-link voltage V_{dc}	150 V
Number of SMs per arm N_{sm}	2
Nominal capacitor voltage V_{nom}	75 V
Arm inductance	1.35 mH
Submodule capacitance	1.33 mF

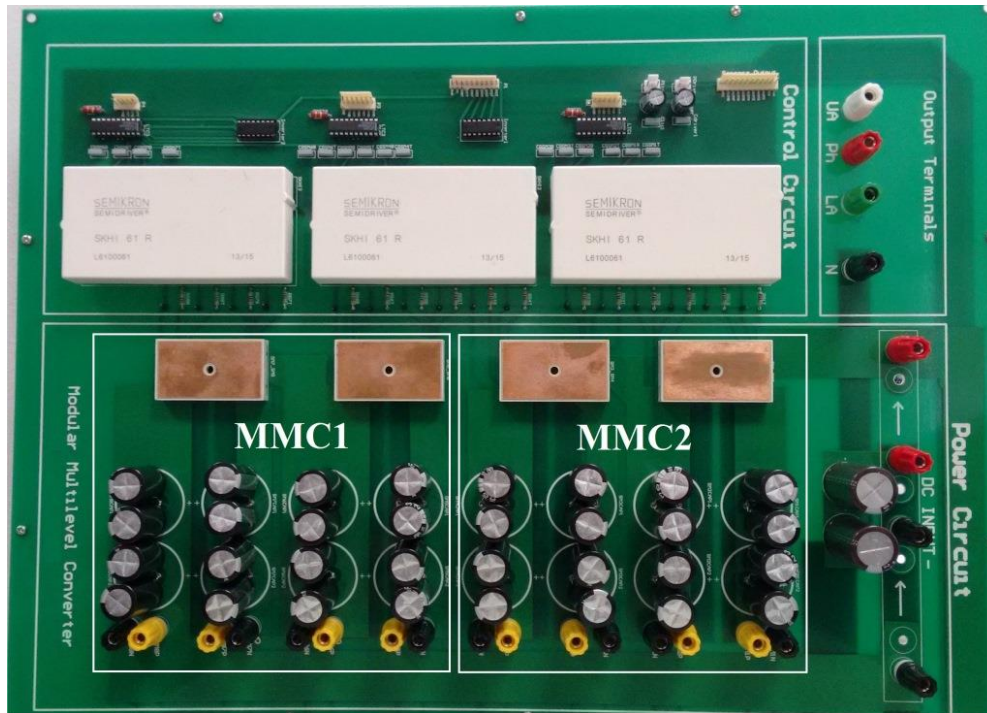
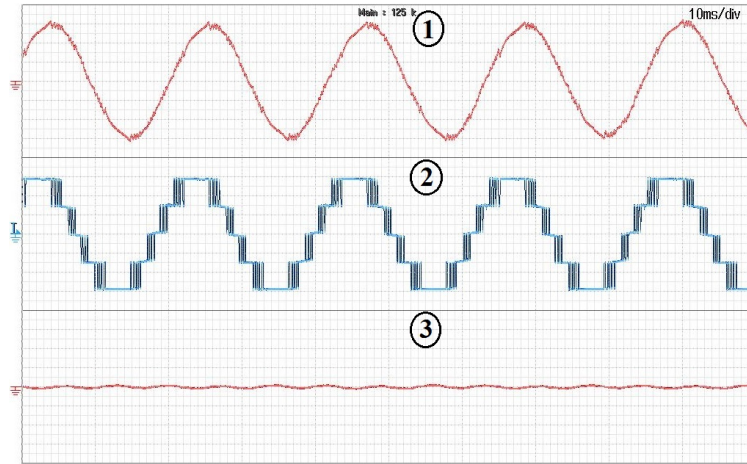


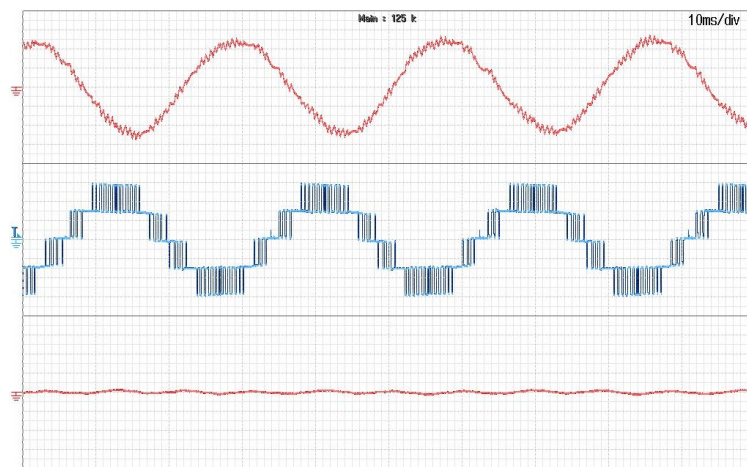
Fig. 5.18: Prototype of dual 3L-MMC for one of the three-phases

The optimal switching angles have been generated for three different operating points ($m=0.9294$, $N=8$), ($m=0.6667$, $N=11$), and ($m=0.5020$, $N=15$). Experimental results for three different operating points, i.e., stator current, stator voltage, and zero-sequence current for one of the three phases is shown in Fig. 5.19 (a)-(c), respectively. The stator voltage, which is obtained by combining outputs of two 3L-MMCs consists of five-level waveforms. It should be noted that pulse number of stator voltage waveforms should be equal to $2*N$. The machine stator currents are sinusoidal although the device switching frequency has been limited to 400 Hz. The zero-sequence current components are obtained by using relation $(i_a + i_b + i_c)/3$ and it should be observed that these are almost eliminated.

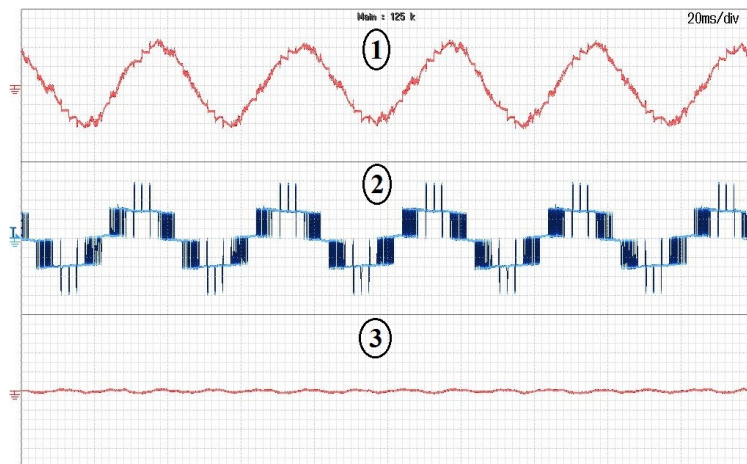
The space vector trajectories of stator currents for the three operating points ($m=0.9294$, $N=8$), ($m=0.6667$, $N=11$), and ($m=0.5020$, $N=15$) are shown in Fig. 5.20 (a)-(c), respectively. The nearly circular trajectories demonstrate low harmonic distortion of converter output current, although the device switching frequency has been limited to 400 Hz. In



(a)



(b)



(c)

Fig. 5.19: Experimental results of dual 3L-MMC inverter : machine stator current ① (Y-axis:50 V/div), stator voltage ② (Y-axis:1 A/div), and zero-sequence current ③ (Y-axis:1 A/div). (a) ($m=0.9294$, $N=8$). X-axis:10 ms/div. (b) ($m=0.7020$, $N=11$). X-axis:10 ms/div. (c) ($m=0.5020$, $N=15$). X-axis:20 ms/div.

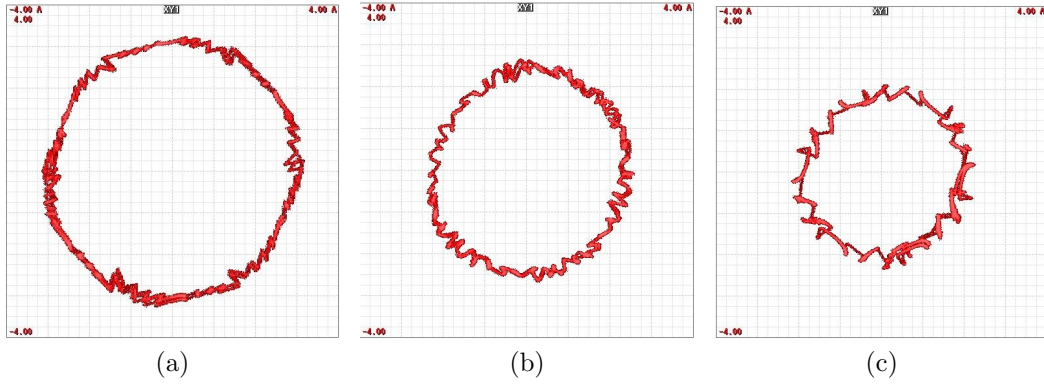


Fig. 5.20: Experimental results of dual 3L-MMC inverter : Stator current space vector trajectories. X,Y-axis:1 A/div (a) ($m=0.9294$, $N=8$) (b) ($m=0.7020$, $N=11$) (c) ($m=0.5020$, $N=15$)

addition, FFT analysis has been performed on recorded stator currents to get better understanding of the harmonic spectrum with calculated optimal switching angles. The harmonic spectrum of stator currents for three operating points are shown in Fig. 5.21 (a)-(c), respectively. The THD of stator currents for three operating points are obtained as 4.06%, 8.50% and 10.21%, respectively. Also, the enlarged view of harmonic spectrum shows that all dominant harmonic components are limited to 3% of fundamental component.

The submodule capacitor voltages of one phase leg of 3L-MMC for the three operating points ($m=0.9294$, $N=8$), ($m=0.6667$, $N=11$), and ($m=0.5020$, $N=15$) are shown in Fig. 5.22 (a)-(c), respectively. The submodule capacitor voltages are well balanced with low voltage ripple. It should be noticed that voltage ripple increases as the value of m decreases. From all the experimental results, it should be concluded that proposed enhanced SOP technique modulates the dual 3L-MMC fed open-end stator winding induction motor drives with elimination of common-mode currents at low device switching frequency, while maintaining lower harmonic distortion of machine stator currents, eliminating common-mode currents in stator windings, and balanced floating capacitor voltages.

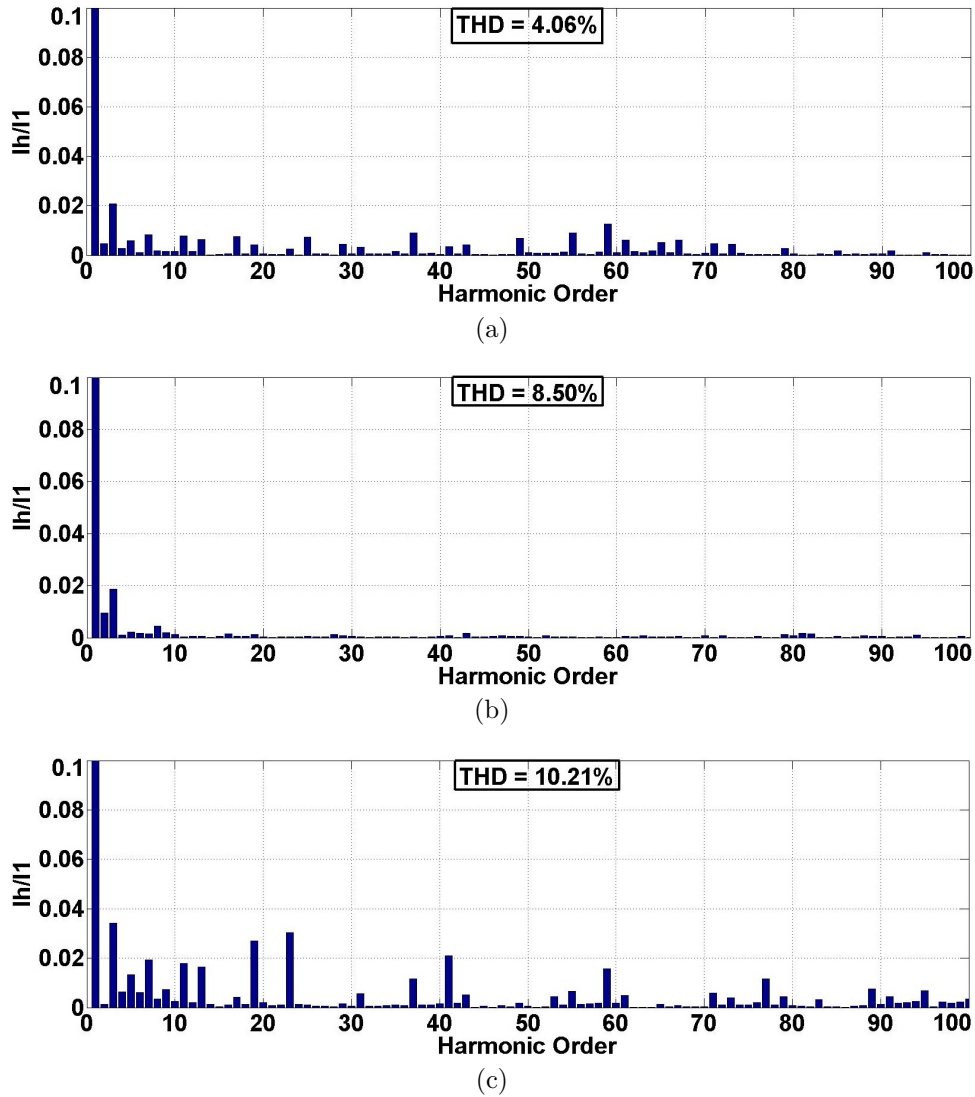


Fig. 5.21: Experimental results of dual 3L-MMC inverter : Harmonic spectrum of stator currents (enlarged view to show the dominant harmonic components). X-axis: Harmonic Order. Y-axis: $\frac{I_h}{I_1}$. a) ($m=0.9294$, $N=8$) (b) ($m=7020$, $N=11$) (c) ($m=0.5020$, $N=15$)

5.5 Summary and Conclusions

In this Chapter, complete details of enhanced SOP technique for dual inverter based MLC fed open-end stator-winding induction motor drives has been presented. Also, details of proposed dual n L-MMC that achieves single dc source operation for any number of voltage levels has been discussed. The control requirements of these topologies are as follows: low device switching frequency, minimal harmonic distortion of machine stator currents, elimination of common-mode currents in the stator windings. In

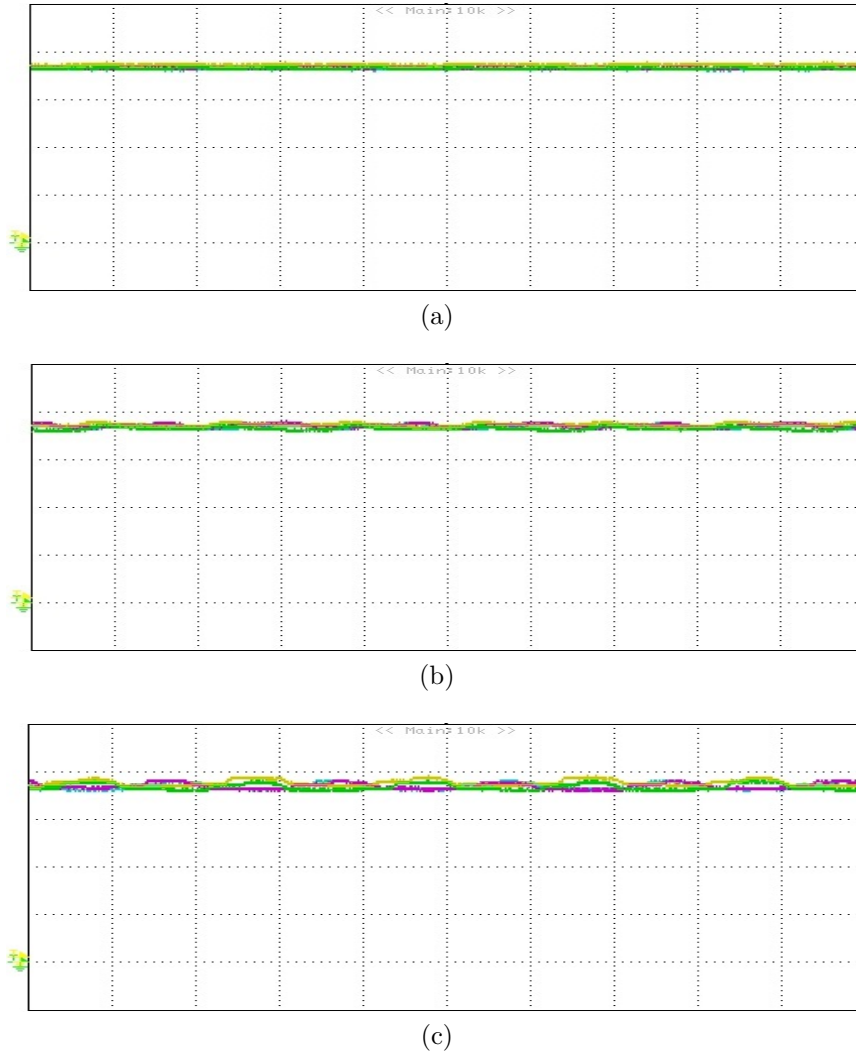


Fig. 5.22: Experimental results of dual 3L-MMC inverter : Submodule capacitor voltages of phase A. X-axis: 20 ms/div, Y-axis:20 V/div (a) ($m=0.9294$, $N=8$) (b) ($m=7020$, $N=11$) (c) ($m=0.5020$, $N=15$)

addition, dual nL -MMC topology requires balanced floating capacitor voltages. The basic idea for elimination of common-mode currents in stator windings is to achieve zero common-mode voltages in the stator windings. This is possible by utilizing switching patterns that are 120° phase apart for the inverter phase legs feeding respective stator winding. The proposed technique has been demonstrated on D2L, D3L, and dual 3L-MMC topologies feeding an 1.5-kW induction motor drive with maximum device switching frequency limited to 400 Hz, 200 Hz, and 400 Hz, respectively.

Chapter 6

Conclusions and Future Work

This chapter concludes the thesis. The summary and conclusions of each Chapter are given in Section 6.1, contributions of the thesis are summarized in Section 6.2, and guidelines for future research are given in Section 6.3.

6.1 Summary and Conclusions

Thermal constraints of power semiconductor devices restrict device switching frequency to a few hundred Hertz in MV drives. However, there exists a trade-off between device switching frequency and total harmonic distortion of machine stator currents. SOP is an effective and emerging low device switching frequency modulation technique, which does not compromise on the quality of machine stator currents. It has been successfully implemented for classical 3L and 5L MLC topologies. On the other hand, current trend in commercial MV drives is to utilize MLCs with higher number of voltage levels to achieve better quality output voltage waveforms. Also, several new topologies have been introduced as an alternative to classical MLC topologies. Therefore, there is a need to analyze and propose modifications to the state-of-the-art SOP technique in order to modulate MLCs with any number of voltage levels and also emerging MLC topologies. This is the main motivation for research carried out in this thesis.

In Chapter 2, SOP technique has been analyzed and implemented into three steps: estimation of pulse number N , optimization of switching angles and allocation of optimal switching angles to each power semiconductor device. It has been identified that first and last steps in SOP technique are dependent on the converter topology, whereas second step in SOP technique is independent of converter topology. The state-of-the-art generalized SOP technique has been developed based on the fact that classical MLC topologies share similar features. However, emerging topologies might require modifications. In the last step of SOP technique, one of the important requirement is to achieve identical device switching frequency and there might be additional requirements unique to each topology such as capacitor voltage balancing, elimination of common-mode currents, and so on. Based on the developed analysis, state-of-the-art generalized SOP technique has been utilized to modulate cascaded 7L and 9L MLCs with $f_{s,max}$ set at f_{1R} . However, it has been observed that converter operates with non identical device switching frequency and thus, device switching frequency is not limited to $f_{s,max}$. Therefore, angle swapping scheme has been utilized to limit average device switching frequency to f_{1R} . The experimental results from low power prototypes of 7L and 9 MLCs have demonstrated its performance.

In Chapter 3, enhanced SOP technique has been proposed to achieve identical switching frequency operation and limit the peak device switching frequency to desired $f_{s,max}$. It has been observed that proposed technique achieve similar performance as that of state-of-the-art SOP technique but with further reduced device switching frequency. In addition, proposed technique maintains the same pulse number for the higher modulation index range that avoids transients in machine currents. The proposed technique has been employed to modulate cascaded 7L and 9L MLCs with $f_{s,max}$ set at f_{1R} and it has been verified experimentally.

In Chapter 4, details of modified SOP technique for MMC topology has been presented. The implementation of SOP for MMC topology requires the following modifications: method to estimate pulse number N at each value of m , and allocation of switching angles to each power semiconductor device. The optimal switching angles should be allocated to each power semiconductor device based on following criteria: identical device switching frequency and balanced capacitor voltages. An angle swapping scheme has been proposed to achieve capacitor voltage balancing. The experimental results from 5L-MMC fed 1.5-kW induction motor drive validated the proposed method and demonstrated its performance. However, it has been noticed that capacitor voltage ripple is higher compared to classical modulation techniques, which utilize higher device switching frequency.

In Chapter 5, complete details of enhanced SOP technique for dual inverter based MLC fed open-end stator-winding induction motor drives have been presented. Also, dual n L-MMC topology has been proposed that achieves single dc source operation for any number of voltage levels. The control requirements of these topologies are as follows: low device switching frequency, minimal harmonic distortion of machine stator currents, elimination of common-mode currents in the stator windings. In addition, dual n L-MMC topology require balancing of floating capacitor voltages around their nominal value. The basic idea for elimination of common-mode currents in stator windings is to utilize switching patterns that are 120° phase apart for the inverter phase legs feeding respective stator winding. The proposed technique has been demonstrated on D2L, D3L, and dual 3L-MMC topologies feeding an 1.5-kW induction motor drive.

6.2 Summary of thesis contributions

The thesis contributions are explained in Section 1.5. They can be summarized as follows:

1. Development of a new systematic analysis of SOP technique. The proposed analysis has been utilized to modulate cascaded 7L and 9L MLCs with $f_{s,avg}$ equal to f_{1R} .
2. Analysis and implementation of modified SOP technique for modulating MLCs with five or higher levels to achieve identical device switching frequency, and limit the peak device switching frequency to desired $f_{s,max}$.
3. Analysis and implementation of modified SOP technique for MMC topology to achieve low device switching frequency operation, minimal harmonic distortion of output currents and balanced submodule capacitor voltages.
4. Analysis and implementation of enhanced SOP technique for dual inverter based topologies to eliminate common-mode currents in machine stator windings, while maintaining the quality of stator currents at low device switching frequency operation.
5. Development of a new dual nL -MMC topology that can be operated from a single dc source and generates any number of voltage levels.

6.3 Scope of Future Work

Based on the research done in this thesis, the recommendations for future research are as follows:

1. **Enhanced SOP for common-mode voltage reduction/elimination in open-end stator winding induction motor drives:**

In the thesis, SOP technique has been enhanced to eliminate common-mode currents in the stator winding. However, common-mode voltages that lead to bearing and leakage currents have been not considered. An enhanced SOP technique that can solve this issue will have great commercial importance.

2. Hybrid modulation technique for emerging MLC topologies with single dc-link source:

Emerging MLC topologies such as MMC or ANPC operate with single dc-link source by utilizing floating capacitor voltages. In the thesis, modified SOP technique has been presented to achieve balanced floating capacitor voltages. However, it has been observed that voltage ripple is higher compared to classical modulation techniques that utilize higher device switching frequency. This is due to omission of voltage ripple factor in the calculations. In addition, low device switching frequency limits effective utilization of redundant switching states to reduce capacitor voltage ripple. One obvious solution is to include voltage ripple in the optimization calculations. However, SOP will become dependent on the load parameters. Another simple solution is to increase the device switching frequency by utilizing redundant switching states to reduce the capacitor voltage ripple. However, this should not lead to unnecessary increase of device switching frequency. This leads to an important question : How to make the best utilization of redundant switching states to keep capacitor voltage ripple within limits at minimum possible device switching frequency. One possible solution could be developing hybrid modulation technique based on SOP and MPC techniques.

3. Grid integration of wind power:

The current trend in wind power turbines is to use PMSG with high power converters. At present, commercial PMSG based turbines are

available with ratings up to 6 MW and in future the ratings are expected to go beyond 10 MW. However, most of the research is carried out with high switching frequency modulation techniques (>1 kHz) such as SPWM and SVM. This is another potential area to do explore and enhance SOP technique, which has been limited to MV drives till now. Some challenges will be meeting stringent grid code requirements such as low voltage ride through capability, operation within given voltage and frequency fluctuations and so on.

4. **Enhanced SOP for AFE multilevel rectifiers:**

The high power applications with regenerative operation require front end converters with bidirectional power flow capability. As the grid codes become more restrictive, the use of multilevel topologies as AFE rectifier is becoming popular. At present, SOP technique has been implemented for AFE rectifiers but it requires bulky filter at the grid side terminals. Therefore, future research should focus on reducing the size of grid side filter, while maintaining the quality of grid currents within standard limits.

Bibliography

- [1] J. Holtz and X. Qi, “Optimal Control of Medium-Voltage Drives —An Overview,” *IEEE Trans. Ind. Electron.*, vol. 60, pp. 5472–5481, Dec 2013.
- [2] H. Abu-Rub, J. Holtz, J. Rodriguez, and G. Baoming, “Medium-Voltage Multilevel Converters -State of the Art, Challenges, and Requirements in Industrial Applications,” *IEEE Trans. Ind. Electron.*, vol. 57, pp. 2581 –2596, aug. 2010.
- [3] S. Kouro, M. Malinowski, K. Gopakumar, J. Pou, L. Franquelo, B. Wu, J. Rodriguez, M. Pérez, and J. Leon, “Recent Advances and Industrial Applications of Multilevel Converters,” *IEEE Trans. Ind. Electron.*, vol. 57, pp. 2553 –2580, aug. 2010.
- [4] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. Perez, “A Survey on Cascaded Multilevel Inverters,” *IEEE Trans. Ind. Electron.*, vol. 57, pp. 2197–2206, july 2010.
- [5] J. Rodriguez, L. Franquelo, S. Kouro, J. Leon, R. Portillo, M. Prats, and M. Perez, “Multilevel Converters: An Enabling Technology for High-Power Applications,” *Proc. IEEE*, vol. 97, pp. 1786 –1817, nov. 2009.
- [6] L. Franquelo, J. Rodriguez, J. Leon, S. Kouro, R. Portillo, and M. Prats, “The age of multilevel converters arrives,” *IEEE Ind. Electron. Mag.*, vol. 2, pp. 28 –39, june 2008.

- [7] S. Bernet, “Recent developments of high power converters for industry and traction applications,” *IEEE Trans. Power Electron.*, vol. 15, pp. 1102–1117, Nov 2000.
- [8] J. Rodriguez, J.-S. Lai, and F. Z. Peng, “Multilevel inverters: a survey of topologies, controls, and applications,” *IEEE Trans. Ind. Electron.*, vol. 49, pp. 724 – 738, aug 2002.
- [9] L. Tolbert, F. Z. Peng, and T. Habetler, “Multilevel converters for large electric drives,” *IEEE Trans. Ind. Appl.*, vol. 35, no. 1, pp. 36–44, 1999.
- [10] J.-S. Lai and F. Z. Peng, “Multilevel converters-a new breed of power converters,” *IEEE Trans. Ind. Appl.*, vol. 32, pp. 509 –517, may/jun 1996.
- [11] A. Nabae, I. Takahashi, and H. Akagi, “A New Neutral-Point-Clamped PWM Inverter,” *IEEE Trans. Ind. Appl.*, vol. IA-17, pp. 518 –523, sept. 1981.
- [12] T. A. Meynard and H. Foch, “Multi-level conversion: high voltage choppers and voltage-source inverters,” in *Proc. IEEE PESC*, pp. 397–403 vol.1, 1992.
- [13] P. Hammond, “A new approach to enhance power quality for medium voltage AC drives,” *IEEE Trans. Ind. Appl.*, vol. 33, pp. 202–208, jan 1997.
- [14] J. Rodriguez, S. Bernet, B. Wu, J. Pontt, and S. Kouro, “Multilevel Voltage-Source-Converter Topologies for Industrial Medium-Voltage Drives,” *IEEE Trans. Ind. Electron.*, vol. 54, pp. 2930 –2945, dec. 2007.

- [15] S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and Comparison of 4-kV Neutral-Point-Clamped, Flying-Capacitor, and Series-Connected H-Bridge Multilevel Converters," *IEEE Trans. Ind. Appl.*, vol. 43, pp. 1032–1040, july-aug. 2007.
- [16] T. Bruckner, S. Bernet, and H. Guldner, "The active NPC converter and its loss-balancing control," *IEEE Trans. Ind. Electron.*, vol. 52, pp. 855–868, June 2005.
- [17] T. Chaudhuri, A. Rufer, and P. Steimer, "The Common Cross-Connected Stage for the 5L ANPC Medium Voltage Multilevel Inverter," *IEEE Trans. Ind. Electron.*, vol. 57, pp. 2279–2286, July 2010.
- [18] M. Manjrekar, P. Steimer, and T. Lipo, "Hybrid multilevel power conversion system: a competitive solution for high-power applications," *IEEE Trans. Ind. Appl.*, vol. 36, no. 3, pp. 834–841, 2000.
- [19] W. Hill and C. Harbourt, "Performance of medium voltage multilevel inverters," in *Conf. Rec. IEEE IAS Annu. Meeting, Phoenix, AZ, October 37*, vol. 2, pp. 1186–1192 vol.2, October 1999.
- [20] S. Busquets-Monge and J. Nicolas-Apruzzese, "A Multilevel Active-Clamped Converter Topology —Operating Principle," *IEEE Trans. Ind. Electron.*, vol. 58, pp. 3868–3878, Sept 2011.
- [21] S. Chattopadhyay and C. Chakraborty, "A new multilevel inverter topology with self-balancing level doubling network," *IEEE Trans. Ind. Electron.*, vol. 61, pp. 4622–4631, Sept 2014.
- [22] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 611–618, 2001.

- [23] M. Kangarlu and E. Babaei, "A Generalized Cascaded Multilevel Inverter Using Series Connection of Submultilevel Inverters," *IEEE Trans. Power Electron.*, vol. 28, pp. 625–636, Feb 2013.
- [24] D. Floricau and F. Richardeau, "New Multilevel Converters Based on Stacked Commutation Cells With Shared Power Devices," *IEEE Trans. Ind. Electron.*, vol. 58, pp. 4675–4682, Oct 2011.
- [25] A. Lesnicar and R. Marquardt, "A new modular voltage source inverter topology," in *Sixth Eur. Conf. Power Electron. Appl.*, pp. 2–4, May 2003.
- [26] C. Patel, R. Ramchand, K. Sivakumar, A. Das, and K. Gopakumar, "A Rotor Flux Estimation During Zero and Active Vector Periods Using Current Error Space Vector From a Hysteresis Controller for a Sensorless Vector Control of IM Drive," *IEEE Trans. Ind. Electron.*, vol. 58, pp. 2334–2344, June 2011.
- [27] G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciuotto, "A new multilevel PWM method: a theoretical analysis," *IEEE Trans. Power Electron.*, vol. 7, pp. 497–505, Jul 1992.
- [28] L. Tolbert and T. Habetler, "Novel multilevel inverter carrier-based PWM method," *IEEE Trans. Ind. Appl.*, vol. 35, pp. 1098–1107, Sep 1999.
- [29] R. Gupta, A. Ghosh, and A. Joshi, "Switching Characterization of Cascaded Multilevel-Inverter-Controlled Systems," *IEEE Trans. Ind. Electron.*, vol. 55, pp. 1047–1058, March 2008.
- [30] B. McGrath and D. Holmes, "Multicarrier PWM strategies for multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, pp. 858–867, Aug 2002.

- [31] B. Ge, F. Z. Peng, A. de Almeida, and H. Abu-Rub, "An Effective Control Technique for Medium-Voltage High-Power Induction Motor Fed by Cascaded Neutral-Point-Clamped Inverter," *IEEE Trans. Ind. Electron.*, vol. 57, pp. 2659–2668, Aug 2010.
- [32] J. Rodriguez, B. Wu, S. Bernet, N. Zargari, J. Rebolledo, J. Pontt, and P. Steimer, "Design and Evaluation Criteria for High Power Drives," in *IEEE IAS Annu. Meeting*, pp. 1–9, Oct 2008.
- [33] Z. Cheng and B. Wu, "A Novel Switching Sequence Design for Five-Level NPC/H-Bridge Inverters With Improved Output Voltage Spectrum and Minimized Device Switching Frequency," *IEEE Trans. Power Electron.*, vol. 22, pp. 2138–2145, nov. 2007.
- [34] A. Das, K. Sivakumar, R. Ramchand, C. Patel, and K. Gopakumar, "A Pulsewidth Modulated Control of Induction Motor Drive Using Multilevel 12-Sided Polygonal Voltage Space Vectors," *IEEE Trans. Ind. Electron.*, vol. 56, pp. 2441–2449, July 2009.
- [35] D. Mayne, J. Rawlings, C. Rao, and P. Scokaert, "Constrained model predictive control: Stability and optimality," *Automatica*, vol. 36, no. 6, pp. 789–814, 2000.
- [36] J. Holtz and S. Stadtfeld, "A predictive controller for the stator current vector of AC machines fed from a switched voltage source," in *Proc. IPEC, Tokyo, Japan*, pp. 1665–1675, March 27–31 1983.
- [37] S. Kouro, P. Cortes, R. Vargas, U. Ammann, and J. Rodriguez, "Model Predictive Control —A Simple and Powerful Method to Control Power Converters," *IEEE Trans. Ind. Electron.*, vol. 56, pp. 1826–1838, June 2009.

- [38] R. Vargas, P. Cortes, U. Ammann, J. Rodriguez, and J. Pontt, "Predictive Control of a Three-Phase Neutral-Point-Clamped Inverter," *IEEE Trans. Ind. Electron.*, vol. 54, pp. 2697–2705, Oct 2007.
- [39] P. Cortes, J. Rodriguez, P. Antoniewicz, and M. Kazmierkowski, "Direct Power Control of an AFE Using Predictive Control," *IEEE Trans. Power Electron.*, vol. 23, pp. 2516–2523, Sept 2008.
- [40] C. Townsend, T. Summers, J. Vodden, A. Watson, R. Betz, and J. Clare, "Optimization of Switching Losses and Capacitor Voltage Ripple Using Model Predictive Control of a Cascaded H-Bridge Multilevel StatCom," *IEEE Trans. Power Electron.*, vol. 28, pp. 3077–3087, July 2013.
- [41] A. Linder and R. Kennel, "Model Predictive Control for Electrical Drives," in *Proc. IEEE Power Electron. Spec. Conf., Recife, Brazil*, pp. 1793–1799, June 2005.
- [42] J. Holtz and S. Stadtfeld, "A PWM inverter drive system with on-line optimized pulse patterns," in *Proc. Eur. Conf. Power Electron. Appl, Brussels, Belgium*, pp. 3.21–3.25, Oct 1985.
- [43] J. Holtz and S. Stadtfeld, "Field-oriented control by forced motor currents in a voltage fed inverter drive," in *Proc. IFAC Symp. Control Power Electron. Elect. Drives, Lausanne, Switzerland*, pp. 103–110, Sep 1983.
- [44] A. Khambadkone and J. Holtz, "Low switching frequency and high dynamic pulsewidth modulation based on field-orientation for high-power inverter drive," *IEEE Trans. Power Electron.*, vol. 7, pp. 627–632, Oct 1992.

- [45] P. Mutschler, “A new speed-control method for induction motors,” in *Proc. Conf. Rec. PCIM, Nuremberg, Germany*, pp. 131–136, May 1988.
- [46] M. Morari, C. Garcia, and D. M. Prett, “Model predictive control: Theory and practice A survey,” *Automatica*, vol. 25, no. 3, pp. 335–348, 1989.
- [47] P. Cortes, M. Kazmierkowski, R. Kennel, D. Quevedo, and J. Rodriguez, “Predictive Control in Power Electronics and Drives,” *IEEE Trans. Ind. Electron.*, vol. 55, pp. 4312–4324, Dec 2008.
- [48] R. Kennel, A. Linder, and M. Linke, “Generalized predictive control (GPC)-ready for use in drive applications?,” in *Power Electron. Spec. Conf.*, vol. 4, pp. 1839–1844 vol. 4, 2001.
- [49] J. Rodriguez, M. Kazmierkowski, J. Espinoza, P. Zanchetta, H. Abu-Rub, H. Young, and C. Rojas, “State of the Art of Finite Control Set Model Predictive Control in Power Electronics,” *IEEE Trans. Ind. Informat.*, vol. 9, pp. 1003–1016, May 2013.
- [50] P. Cortes, A. Wilson, S. Kouro, J. Rodriguez, and H. Abu-Rub, “Model Predictive Control of Multilevel Cascaded H-Bridge Inverters,” *IEEE Trans. Ind. Electron.*, vol. 57, pp. 2691–2699, August 2010.
- [51] S. Vazquez, J. Leon, L. Franquelo, J. Rodriguez, H. Young, A. Marquez, and P. Zanchetta, “Model Predictive Control: A Review of Its Applications in Power Electronics,” *IEEE Trans. Ind. Electron. Mag.*, vol. 8, pp. 16–31, March 2014.
- [52] P. Karamanakos, T. Geyer, N. Oikonomou, F. Kieferndorf, and S. Manias, “Direct Model Predictive Control: A Review of Strate-

- gies That Achieve Long Prediction Intervals for Power Electronics,” *IEEE Ind. Electron. Mag.*, vol. 8, pp. 32–43, March 2014.
- [53] T. Geyer, G. Papafotiou, and M. Morari, “Model Predictive Control in Power Electronics: A Hybrid Systems Approach,” in *IEEE Conf. Decision and Control*, pp. 5606–5611, Dec 2005.
- [54] T. Geyer, “Generalized Model Predictive Direct Torque Control: Long prediction horizons and minimization of switching losses,” in *Proc. 48th IEEE Conf. Decision and Control*, pp. 6799–6804, Dec 2009.
- [55] G. Papafotiou, J. Kley, K. Papadopoulos, P. Bohren, and M. Morari, “Model Predictive Direct Torque Control —Part II: Implementation and Experimental Evaluation,” *IEEE Trans. Ind. Electron.*, vol. 56, pp. 1906–1915, June 2009.
- [56] T. Geyer, “Model Predictive Direct Current Control: Formulation of the Stator Current Bounds and the Concept of the Switching Horizon,” *IEEE Ind. Appl. Mag.*, vol. 18, pp. 47–59, March 2012.
- [57] J. Scoltock, T. Geyer, and U. Madawala, “Model Predictive Direct Power Control for Grid-Connected NPC Converters,” *IEEE Trans. Ind. Electron.*, vol. 62, pp. 5319–5328, Sept 2015.
- [58] T. Geyer and D. Quevedo, “Multistep Finite Control Set Model Predictive Control for Power Electronics,” *IEEE Trans. Power Electron.*, vol. 29, pp. 6836–6846, Dec 2014.
- [59] T. Geyer, “Computationally Efficient Model Predictive Direct Torque Control,” *IEEE Trans. Power Electron.*, vol. 26, pp. 2804–2816, Oct 2011.

- [60] T. Geyer and D. Quevedo, "Performance of Multistep Finite Control Set Model Predictive Control for Power Electronics," *IEEE Trans. Power Electron.*, vol. 30, pp. 1633–1644, March 2015.
- [61] T. Geyer, N. Oikonomou, G. Papafotiou, and F. Kieferndorf, "Model Predictive Pulse Pattern Control," *IEEE Tran. Ind. Appl.*, vol. 48, pp. 663–676, March 2012.
- [62] J. Scoltock, T. Geyer, and U. Madawala, "A Comparison of Model Predictive Control Schemes for MV Induction Motor Drives," *IEEE Trans. Ind. Informat.*, vol. 9, pp. 909–919, May 2013.
- [63] T. Geyer, "A Comparison of Control and Modulation Schemes for Medium-Voltage Drives: Emerging Predictive Control Concepts Versus PWM-Based Schemes," *IEEE Tran. Ind. Appl.*, vol. 47, pp. 1380–1389, May 2011.
- [64] F. Turnbull, "Selected harmonic reduction in static D-C - A-C inverters," *IEEE Trans. Commun. Electron.*, vol. 83, no. 73, pp. 374–378, 1964.
- [65] H. S. Patel and R. Hoft, "Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I—Harmonic Elimination," *IEEE Trans. Ind. Appl.*, vol. IA-9, pp. 310–317, May 1973.
- [66] L. Li, D. Czarkowski, Y. Liu, and P. Pillay, "Multilevel selective harmonic elimination PWM technique in series-connected voltage inverters," *IEEE Trans. Ind. Appl.*, vol. 36, pp. 160–170, Jan 2000.
- [67] W. Fei, X. Du, and B. Wu, "A Generalized Half-Wave Symmetry SHE-PWM Formulation for Multilevel Voltage Inverters," *IEEE Trans. Ind. Electron.*, vol. 57, pp. 3030–3038, Sept 2010.

- [68] M. Dahidah, V. Agelidis, and M. Rao, "On Abolishing Symmetry Requirements in the Formulation of a Five-Level Selective Harmonic Elimination Pulse-Width Modulation Technique," *IEEE Trans. Power Electron.*, vol. 21, pp. 1833–1837, Nov 2006.
- [69] M. Dahidah, G. Konstantinou, and V. Agelidis, "A Review of Multilevel Selective Harmonic Elimination PWM: Formulations, Solving Algorithms, Implementation and Applications," *IEEE Trans. Power Electron.*, vol. 30, pp. 4091–4106, Aug 2015.
- [70] M. Ye, P. Song, and C. Zhang, "Study of harmonic elimination technology for multi-level inverters," in *Proc. IEEE ICIEA 2008*, pp. 242–245, June 2008.
- [71] Z. Du, L. Tolbert, and J. Chiasson, "Active harmonic elimination for multilevel converters," *IEEE Trans. Power Electron.*, vol. 21, pp. 459–469, March 2006.
- [72] S. Pulikanti and V. Agelidis, "Control of neutral point and flying capacitor voltages in five-level SHE-PWM controlled ANPC converter," in *Proc. IEEE ICIEA 2009*, pp. 172–177, May 2009.
- [73] M. Dahidah and V. Agelidis, "A Hybrid Genetic Algorithm for Selective Harmonic Elimination Control of a Multilevel Inverter with Non-Equal DC Sources," in *Proc. PEDS*, vol. 2, pp. 1205–1210, 2005.
- [74] H. Taghizadeh and M. Hagh, "Harmonic Elimination of Cascade Multilevel Inverters with Nonequal DC Sources Using Particle Swarm Optimization," *IEEE Trans. Ind. Electron.*, vol. 57, pp. 3678–3684, Nov 2010.
- [75] A. Kavousi, B. Vahidi, R. Salehi, M. Bakhshizadeh, N. Farokhnia, and S. Fathi, "Application of the Bee Algorithm for Selective Har-

- monic Elimination Strategy in Multilevel Inverters,” *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1689–1696, 2012.
- [76] F. Filho, L. Tolbert, Y. Cao, and B. Ozpineci, “Real-Time Selective Harmonic Minimization for Multilevel Inverters Connected to Solar Panels Using Artificial Neural Network Angle Generation,” *IEEE Trans. Ind. Appl.*, vol. 47, pp. 2117–2124, Sept 2011.
- [77] S. Kouro, B. La Rocca, P. Cortes, S. Alepuz, B. Wu, and J. Rodriguez, “Predictive control based selective harmonic elimination with low switching frequency for multilevel converters,” in *Proc. IEEE ECCE*, pp. 3130–3136, Sept 2009.
- [78] V. Agelidis, A. Balouktsis, and M. S. Dahidah, “A Five-Level Symmetrically Defined Selective Harmonic Elimination PWM Strategy: Analysis and Experimental Validation,” *IEEE Trans. Power Electron.*, vol. 23, pp. 19–26, Jan 2008.
- [79] M. S. A. Dahidah and V. Agelidis, “Selective Harmonic Elimination PWM Control for Cascaded Multilevel Voltage Source Converters: A Generalized Formula,” *IEEE Trans. Power Electron.*, vol. 23, pp. 1620–1630, July 2008.
- [80] S. Pulikanti, G. Konstantinou, and V. Agelidis, “DC-Link Voltage Ripple Compensation for Multilevel Active-Neutral-Point-Clamped Converters Operated With SHE-PWM,” *IEEE Trans. Power Del.*, vol. 27, pp. 2176–2184, Oct 2012.
- [81] S. Pulikanti and V. Agelidis, “Hybrid Flying-Capacitor-Based Active-Neutral-Point-Clamped Five-Level Converter Operated With SHE-PWM,” *IEEE Trans. Ind. Electron.*, vol. 58, pp. 4643–4653, Oct 2011.

- [82] G. Konstantinou, M. Ciobotaru, and V. Agelidis, "Selective harmonic elimination pulse-width modulation of modular multilevel converters," *IET Power Electron.*, vol. 6, pp. 96–107, Jan 2013.
- [83] W. Liu, Q. Song, X. Xie, Y. Chen, and G. Yan, "6 kV/1800 kVA medium voltage drive with three-level NPC inverter using IGCTs," in *Proc. IEEE APEC*, vol. 1, pp. 223–227 vol.1, Feb 2003.
- [84] A. Watson, P. Wheeler, and J. Clare, "A Complete Harmonic Elimination Approach to DC Link Voltage Balancing for a Cascaded Multilevel Rectifier," *IEEE Trans. Ind. Electron.*, vol. 54, pp. 2946–2953, Dec 2007.
- [85] B. Gultekin and M. Ermis, "Cascaded Multilevel Converter-Based Transmission STATCOM: System Design Methodology and Development of a 12 kV \pm 12 MVar Power Stage," *IEEE Trans. Power Electron.*, vol. 28, pp. 4930–4950, Nov 2013.
- [86] E. Ozdemir, S. Ozdemir, and L. Tolbert, "Fundamental-Frequency-Modulated Six-Level Diode-Clamped Multilevel Inverter for Three-Phase Stand-Alone Photovoltaic System," *IEEE Trans. Ind. Electron.*, vol. 56, pp. 4407–4415, Nov 2009.
- [87] G. S. Buja and G. B. Indri, "Optimal Pulsewidth Modulation for Feeding AC Motors," *IEEE Trans. Ind. Appl.*, vol. IA-13, pp. 38–44, Jan 1977.
- [88] B. Wu, *High-Power Converters and AC Drives*. Wiley, 2006.
- [89] D. W. Kang, H. C. Kim, T. J. Kim, and D. S. Hyun, "A simple method for acquiring the conducting angle in a multilevel cascaded inverter using step pulse waves," *IEE Proc. - Electr. Power Appl.*, vol. 152, pp. 103–111, Jan 2005.

- [90] Y. Liu, H. Hong, and A. Huang, "Real-Time Calculation of Switching Angles Minimizing THD for Multilevel Inverters With Step Modulation," *IEEE Trans. Ind. Electron.*, vol. 56, pp. 285–293, Feb 2009.
- [91] Y. Liu, H. Hong, and A. Huang, "Real-Time Algorithm for Minimizing THD in Multilevel Inverters With Unequal or Varying Voltage Steps Under Staircase Modulation," *IEEE Trans. Ind. Electron.*, vol. 56, pp. 2249–2258, June 2009.
- [92] F. C. Zach and H. Ertl, "Efficiency Optimal Control for AC Drives with PWM Inverters," *IEEE Trans. Ind. Appl.*, vol. IA-21, no. 4, pp. 987–1000, 1985.
- [93] M. El-Bakry, "Selective Harmonics Minimization for Multilevel Inverters," in *Int. Conf. Comp. Elect. Eng.*, vol. 2, pp. 341–346, Dec 2009.
- [94] F. Filho, H. Maia, T. Mateus, B. Ozpineci, L. Tolbert, and J. Pinto, "Adaptive Selective Harmonic Minimization Based on ANNs for Cascade Multilevel Inverters With Varying DC Sources," *IEEE Trans. Ind. Electron.*, vol. 60, pp. 1955–1962, May 2013.
- [95] G. S. Buja, "Optimum Output Waveforms in PWM Inverters," *IEEE Trans. Ind. Appl.*, vol. IA-16, pp. 830–836, nov. 1980.
- [96] P. M. Bhagwat and V. Stefanovic, "Generalized Structure of a Multilevel PWM Inverter," *IEEE Trans. Ind. Appl.*, vol. IA-19, pp. 1057–1069, Nov 1983.
- [97] I. Takahashi and H. Mochikawa, "A New Control of PWM Inverter Waveform for Minimum Loss Operation of an Induction Motor Drive," *IEEE Trans. Ind. Appl.*, vol. IA-21, pp. 580–587, May 1985.

- [98] R. Betz, R. Evans, and B. J. Cook, "Optimal Pulsewidth Modulation for Current Source Inverters," *IEEE Trans. Ind. Electron.*, vol. IE-33, no. 3, pp. 318–324, 1986.
- [99] S. Sirisukprasert, J.-S. Lai, and T.-H. Liu, "Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 49, pp. 875–881, Aug 2002.
- [100] L. Franquelo, J. Napoles, R. Guisado, J. Leon, and M. Aguirre, "A Flexible Selective Harmonic Mitigation Technique to Meet Grid Codes in Three-Level PWM Converters," *IEEE Trans. Ind. Electron.*, vol. 54, pp. 3022–3029, Dec 2007.
- [101] J. Holtz and B. Beyer, "Optimal pulsewidth modulation for AC servos and low-cost industrial drives," *IEEE Trans. Ind. Appl.*, vol. 30, pp. 1039–1047, Jul 1994.
- [102] R. M. Green and J. T. Boys, "PWM Sequence Selection and Optimization: A Novel Approach," *IEEE Trans. Ind. Appl.*, vol. IA-18, pp. 146–151, March 1982.
- [103] S. Hálasz, A. A. M. Hassan, and B. T. Huu, "Optimal control of three-level PWM inverters," *IEEE Trans. Ind. Electron.*, vol. 44, pp. 96–106, Feb 1997.
- [104] F. C. Zach, R. Martinez, S. Keplinger, and A. Seiser, "Dynamically Optimal Switching Patterns for PWM Inverter Drives (for Minimization of the Torque and Speed Ripples)," *IEEE Trans. Ind. Appl.*, vol. IA-21, no. 4, pp. 975–986, 1985.
- [105] K. Basu, J. Prasad, and G. Narayanan, "Minimization of Torque Ripple in PWM AC Drives," *IEEE Trans. Ind. Electron.*, vol. 56, pp. 553–558, Feb 2009.

- [106] X. Mao, R. Ayyanar, and H. Krishnamurthy, "Optimal Variable Switching Frequency Scheme for Reducing Switching Loss in Single-Phase Inverters Based on Time-Domain Ripple Analysis," *IEEE Tran. Power Electron.*, vol. 24, pp. 991–1001, April 2009.
- [107] J. Holtz and J.-O. Krah, "Adaptive optimal pulse-width modulation for the line-side converter of electric locomotives," *IEEE Trans. Power Electron.*, vol. 7, pp. 205–211, Jan 1992.
- [108] A. Trzynadlowski and S. Legowski, "Application of neural networks to the optimal control of three-phase voltage-controlled inverters," *IEEE Trans. Power Electron.*, vol. 9, pp. 397–404, Jul 1994.
- [109] B. Ozpineci, L. Tolbert, and J. Chiasson, "Harmonic optimization of multilevel converters using genetic algorithms," *IEEE Power Electron. Lett.*, vol. 3, pp. 92–95, Sept 2005.
- [110] M. Hagh, H. Taghizadeh, and K. Razi, "Harmonic Minimization in Multilevel Inverters Using Modified Species-Based Particle Swarm Optimization," *IEEE Trans. Power Electron.*, vol. 24, pp. 2259–2267, Oct 2009.
- [111] P. Torri, G. da Cunha, T. Boller, A. Rathore, J. Holtz, and N. Oikonomou, "Optimal pulse width modulation for multi-level inverter systems," April 20 2011. EP Patent App. EP20,090,171,698.
- [112] WEG. [Online]: <http://ecatalog.weg.net/files/wegnet/WEG-mvw01-medium-voltage-drive-usamvw0109-brochure-english.pdf>.
- [113] J. Holtz, "Pulsewidth modulation for electronic power conversion," *Proc. IEEE*, vol. 82, pp. 1194–1214, aug 1994.

- [114] A. Rathore, J. Holtz, and T. Boller, “Generalized Optimal Pulsewidth Modulation of Multilevel Inverters for Low-Switching-Frequency Control of Medium-Voltage High-Power Industrial AC Drives,” *IEEE Trans. Ind. Electron.*, vol. 60, pp. 4215–4224, Oct 2013.
- [115] A. Rathore, J. Holtz, and T. Boller, “Synchronous Optimal Pulsewidth Modulation for Low-Switching-Frequency Control of Medium-Voltage Multilevel Inverters,” *IEEE Trans. Ind. Electron.*, vol. 57, pp. 2374–2381, July 2010.
- [116] J. Holtz and B. Beyer, “Off-line optimized synchronous pulsewidth modulation with on-line control during transients,” *European Power Electron. J.*, vol. 01-3, pp. 183–190, 1991.
- [117] T. Boller, J. Holtz, and A. Rathore, “Neutral-Point Potential Balancing Using Synchronous Optimal Pulsewidth Modulation of Multilevel Inverters in Medium-Voltage High-Power AC Drives,” *IEEE Trans. Ind. Appl.*, vol. 50, pp. 549–557, Jan 2014.
- [118] T. Boller, J. Holtz, and A. Rathore, “Optimal pulsewidth modulation of a dual three-level inverter system operated from a single dc link,” in *Proc. IEEE ECCE*, pp. 3406–3410, Sept 2011.
- [119] J. Holtz, G. da Cunha, N. Petry, and P. Torri, “Control of Large Salient Pole Synchronous Machines using Synchronous Optimal Pulsewidth Modulation,” *IEEE Trans. Ind. Electron.*, vol. 62, pp. 3372–3379, June 2015.
- [120] J. Holtz and B. Beyer, “Optimal synchronous pulsewidth modulation with a trajectory tracking scheme for high dynamic performance [inverter control],” in *Proc. IEEE APEC*, pp. 147–154, 1992.

- [121] J. Holtz and B. Beyer, "Optimal synchronous pulsewidth modulation with a trajectory-tracking scheme for high-dynamic performance," *IEEE Trans. Ind. Appl.*, vol. 29, no. 6, pp. 1098–1105, 1993.
- [122] J. Holtz and B. Beyer, "Fast current trajectory tracking control based on synchronous optimal pulsewidth modulation," *IEEE Trans. Ind. Appl.*, vol. 31, pp. 1110–1120, sep/oct 1995.
- [123] J. Holtz and B. Beyer, "The trajectory tracking approach—a new method for minimum distortion PWM in dynamic high-power drives," *IEEE Trans. Ind. Appl.*, vol. 30, pp. 1048–1057, jul/aug 1994.
- [124] J. Holtz and N. Oikonomou, "Synchronous Optimal Pulsewidth Modulation and Stator Flux Trajectory Control for Medium-Voltage Drives," *IEEE Trans. Ind. Appl.*, vol. 43, pp. 600–608, march-april 2007.
- [125] N. Oikonomou and J. Holtz, "Closed-Loop Control of Medium-Voltage Drives Operated With Synchronous Optimal Pulsewidth Modulation," *IEEE Trans. Ind. Appl.*, vol. 44, pp. 115–123, jan.-feb. 2008.
- [126] J. Holtz and N. Oikonomou, "Fast Dynamic Control of Medium Voltage Drives Operating at Very Low Switching Frequency - an Overview," *IEEE Trans. Ind. Electron.*, vol. 55, pp. 1005–1013, march 2008.
- [127] J. Holtz and N. Oikonomou, "Estimation of the Fundamental Current in Low-Switching-Frequency High Dynamic Medium-Voltage Drives," *IEEE Trans. Ind. Appl.*, vol. 44, pp. 1597–1605, sept.-oct. 2008.

- [128] N. Oikonomou, C. Gutscher, P. Karamanakos, F. Kieferndorf, and T. Geyer, "Model Predictive Pulse Pattern Control for the Five-Level Active Neutral-Point-Clamped Inverter," *IEEE Tran. Ind. Appl.*, vol. 49, pp. 2583–2592, Nov 2013.
- [129] J. Rodriguez, L. Moran, P. Correa, and C. Silva, "A vector control technique for medium-voltage multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 49, pp. 882–888, Aug 2002.
- [130] S. Kouro, R. Bernal, H. Miranda, C. Silva, and J. Rodriguez, "High-Performance Torque and Flux Control for Multilevel Inverter Fed Induction Motors," *IEEE Trans. Power Electron.*, vol. 22, pp. 2116–2123, Nov 2007.
- [131] S. Kouro, J. Rebolledo, and J. Rodriguez, "Reduced Switching-Frequency-Modulation Algorithm for High-Power Multilevel Inverters," *IEEE Trans. Ind. Electron.*, vol. 54, pp. 2894–2901, oct. 2007.
- [132] F. Vargas-Merino, M. Meco-Gutierrez, J. Heredia-Larrubia, and A. Ruiz-Gonzalez, "Low Switching PWM Strategy Using a Carrier Wave Regulated by the Slope of a Trapezoidal Modulator Wave," *IEEE Trans. Ind. Electron.*, vol. 56, pp. 2270–2274, June 2009.
- [133] M. Saeedifard, P. Barbosa, and P. Steimer, "Operation and Control of a Hybrid Seven-Level Converter," *IEEE Trans. Power Electron.*, vol. 27, pp. 652–660, Feb 2012.
- [134] T. Geyer and S. Mastellone, "Model Predictive Direct Torque Control of a Five-Level ANPC Converter Drive System," *IEEE Tran. Ind. Appl.*, vol. 48, pp. 1565–1575, Sept 2012.
- [135] M. Glinka and R. Marquardt, "A new AC/AC multilevel converter family," *IEEE Trans. Ind. Electron.*, vol. 52, pp. 662–669, June 2005.

- [136] B. Gemmell, J. Dorn, D. Retzmann, and D. Soerangr, "Prospects of multilevel VSC technologies for power transmission," in *IEEE/PES Trans. Distrib. Conf. Expo.*, pp. 1–16, April 2008.
- [137] SIEMENS. Sinamics SM120. [Online] Available: <http://www.industry.siemens.com/drives/global/en/converter/mv-drives/sinamics-sm120-cm/Pages/sinamics-sm120-cm.aspx>.
- [138] S. Debnath, J. Qin, B. Bahrani, M. Saeedifard, and P. Barbosa, "Operation, Control, and Applications of the Modular Multilevel Converter: A Review," *IEEE Trans. Power Electron.*, vol. 30, pp. 37–53, Jan 2015.
- [139] M. Hagiwara, K. Nishimura, and H. Akagi, "A Medium-Voltage Motor Drive With a Modular Multilevel PWM Inverter," *IEEE Trans. Power Electron.*, vol. 25, pp. 1786–1799, July 2010.
- [140] K. Ilves, A. Antonopoulos, S. Norrga, and H.-P. Nee, "A New Modulation Method for the Modular Multilevel Converter Allowing Fundamental Switching Frequency," *IEEE Trans. Power Electron.*, vol. 27, pp. 3482–3494, Aug. 2012.
- [141] K. Ilves, A. Antonopoulos, L. Harnefors, S. Norrga, and H.-P. Nee, "Circulating current control in modular multilevel converters with fundamental switching frequency," in *Int. Power Electron. Motion Control Conf.*, vol. 1, pp. 249–256, June 2012.
- [142] P. Meshram and V. Borghate, "A Simplified Nearest Level Control (NLC) Voltage Balancing Method for Modular Multilevel Converter (MMC)," *IEEE Trans. Power Electron.*, vol. 30, pp. 450–462, Jan 2015.

- [143] J. Huber and A. Korn, "Optimized Pulse Pattern modulation for Modular Multilevel Converter high-speed drive," in *Proc. EPE/PEMC*, pp. LS1a-1.4-1-LS1a-1.4-7, Sept 2012.
- [144] J. Qin and M. Saeedifard, "Predictive Control of a Modular Multilevel Converter for a Back-to-Back HVDC System," *IEEE Trans. Power Deliv.*, vol. 27, pp. 1538-1547, July 2012.
- [145] G. Darivianakis, T. Geyer, and W. van der Merwe, "Model predictive current control of modular multilevel converters," in *Proc. IEEE ECCE*, pp. 5016-5023, Sept 2014.
- [146] B. Riar, T. Geyer, and U. Madawala, "Model Predictive Direct Current Control of Modular Multilevel Converters: Modelling, Analysis and Experimental Evaluation," *IEEE Trans. Power Electron.*, vol. 30, pp. 431-439, Jan 2015.
- [147] J. Bocker, B. Freudenberg, A. The, and S. Dieckerhoff, "Experimental Comparison of Model Predictive Control and Cascaded Control of the Modular Multilevel Converter," *IEEE Trans. Power Electron.*, vol. 30, pp. 422-430, Jan 2015.
- [148] J.-W. Moon, J.-S. Gwon, J.-W. Park, D.-W. Kang, and J.-M. Kim, "Model Predictive Control With a Reduced Number of Considered States in a Modular Multilevel Converter for HVDC System," *IEEE Trans. Power Del.*, vol. 30, pp. 608-617, April 2015.
- [149] M. Vatani, B. Bahrani, M. Saeedifard, and M. Hovd, "Indirect Finite Control Set Model Predictive Control of Modular Multilevel Converters," *IEEE Trans. Smart Grid*, vol. 6, pp. 1520-1529, May 2015.
- [150] H. Stemmler and P. Guggenbach, "Configurations of high-power voltage source inverter drives," in *Fifth European Conf. Power Electron. and Appl., 1993.*, pp. 7-14 vol.5, 1993.

- [151] K. Corzine, M. Wielebski, F. Peng, and J. Wang, "Control of cascaded multilevel inverters," *IEEE Trans. Power Electron.*, vol. 19, pp. 732–738, May 2004.
- [152] V. Somasekhar, K. Gopakumar, M. R. Baiju, K. Mohapatra, and L. Umanand, "A multilevel inverter system for an induction motor with open-end windings," *IEEE Trans. Ind. Electron.*, vol. 52, pp. 824–836, June 2005.
- [153] G. Mondal, K. Gopakumar, P. N. Tekwani, and E. Levi, "A Reduced-Switch-Count Five-Level Inverter With Common-Mode Voltage Elimination for an Open-End Winding Induction Motor Drive," *IEEE Trans. Ind. Electron.*, vol. 54, pp. 2344–2351, Aug 2007.
- [154] M. Rotella, G. Penailillo, J. Pereda, and J. Dixon, "PWM Method to Eliminate Power Sources in a Nonredundant 27-Level Inverter for Machine Drive Applications," *IEEE Trans. Ind. Electron.*, vol. 56, pp. 194–201, Jan 2009.
- [155] P. N. Tekwani, R. S. Kanchan, and K. Gopakumar, "A Dual Five-Level Inverter-Fed Induction Motor Drive With Common-Mode Voltage Elimination and DC-Link Capacitor Voltage Balancing Using Only the Switching-State Redundancy —Part I," *IEEE Trans. Ind. Electron.*, vol. 54, no. 5, pp. 2600–2608, 2007.
- [156] G. Mondal, K. Sivakumar, R. Ramchand, K. Gopakumar, and E. Levi, "A Dual Seven-Level Inverter Supply for an Open-End Winding Induction Motor Drive," *IEEE Trans. Ind. Electron.*, vol. 56, pp. 1665–1673, May 2009.
- [157] P. Rajeevan, K. Sivakumar, K. Gopakumar, C. Patel, and H. Abu-Rub, "A Nine-Level Inverter Topology for Medium-Voltage Induction

- Motor Drive With Open-End Stator Winding,” *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3627–3636, 2013.
- [158] V. T. Somasekhar, K. Gopakumar, E. Sivakumar, and S. Sinha, “A space vector modulation scheme for a dual two level inverter fed open-end winding induction motor drive for the elimination of zero sequence currents,” *EPE Journal*, vol. 12, no. 2, pp. 26–36, 2002.
- [159] M. R. Baiju, K. Mohapatra, R. S. Kanchan, and K. Gopakumar, “A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive,” *IEEE Trans. Power Electron.*, vol. 19, no. 3, pp. 794–805, 2004.
- [160] K. Corzine, S. Sudhoff, and C. Whitcomb, “Performance characteristics of a cascaded two-level converter,” *IEEE Trans. Energy Convers.*, vol. 14, pp. 433–439, Sep 1999.
- [161] J. Holtz and N. Oikonomou, “Optimal Control of a Dual Three-Level Inverter System for Medium-Voltage Drives,” *IEEE Trans. Ind. Appl.*, vol. 46, pp. 1034–1041, may-june 2010.
- [162] T. Boller, J. Holtz, and A. Rathore, “Optimal Pulsewidth Modulation of a Dual Three-Level Inverter System Operated From a Single DC Link,” *IEEE Trans. Ind. Appl.*, vol. 48, pp. 1610–1615, Sept 2012.
- [163] K. Corzine and Y. Familant, “A new cascaded multilevel H-bridge drive,” *IEEE Trans. Power Electron.*, vol. 17, pp. 125–131, jan 2002.
- [164] J. Holtz and N. Oikonomou, “Neutral Point Potential Balancing Algorithm at Low Modulation Index for Three-Level Inverter Medium-Voltage Drives,” *IEEE Trans. Ind. Appl.*, vol. 43, pp. 761–768, may-june 2007.

- [165] H. Du Toit Mouton, “Natural balancing of three-level neutral-point-clamped PWM inverters,” *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1017–1025, 2002.
- [166] Z. Shu, X. He, Z. Wang, D. Qiu, and Y. Jing, “Voltage Balancing Approaches for Diode-Clamped Multilevel Converters Using Auxiliary Capacitor-Based Circuits,” *IEEE Trans. Power Electron.*, vol. 28, no. 5, pp. 2111–2124, 2013.
- [167] L. Angquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiliadis, and H.-P. Nee, “Open-Loop Control of Modular Multilevel Converters Using Estimation of Stored Energy,” *IEEE Trans. Ind. Appl.*, vol. 47, pp. 2516–2524, Nov 2011.
- [168] M. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, “Circuit Topologies, Modeling, Control Schemes, and Applications of Modular Multilevel Converters,” *IEEE Trans. Power Electron.*, vol. 30, pp. 4–17, Jan 2015.

List of Publications

Journals

1. A. Edpuganti and A. Rathore, "Optimal Low Switching Frequency Pulsewidth Modulation of Nine-Level Cascade Inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 482–495, Jan 2015.
2. A. Edpuganti and A. Rathore, "Optimal Low-Switching Frequency Pulsewidth Modulation of Medium Voltage Seven-Level Cascade-5/3H Inverter," *IEEE Trans. Power Electron.*, vol. 30, no. 1, pp. 496–503, Jan 2015.
3. A. Edpuganti and A. Rathore, "Fundamental Switching Frequency Optimal Pulsewidth Modulation of Medium-Voltage Nine-Level Inverter," *IEEE Trans. Ind. Electron.*, vol. 62, no. 7, pp. 4096–4104, July 2015.
4. A. Edpuganti and A. Rathore, "Fundamental Switching Frequency Optimal PulseWidth Modulation of Medium Voltage Cascaded Seven-Level Inverter," *IEEE Trans. Ind. Appl.*, 2015, vol. 51, no. 4, pp. 3485–3492, July 2015.
5. A. Edpuganti and A. Rathore, "New Optimal Pulsewidth Modulation for Single DC-Link Dual-Inverter Fed Open-End Stator Winding Induction Motor Drive," *IEEE Trans. Power Electron.*, vol. 30, no. 8, pp. 4386–4393, Aug 2015.
6. A. Edpuganti and A. Rathore, "A Survey of Low Switching Frequency Modulation Techniques for Medium-Voltage Multilevel Converters," *IEEE Trans. Ind. Appl.*, vol. 51, no. 5, pp. 4212–4228, Sept 2015.
7. A. Edpuganti and A. Rathore, "Optimal Pulsewidth Modulation of Medium-Voltage Modular Multilevel Converter," *Accepted, IEEE Trans. Ind. Appl.*.
8. A. Edpuganti and A. Rathore, "Optimal Pulsewidth Modulation for Common-Mode Voltage Elimination of Medium-Voltage Modular Mul-

tilevel Converter fed Open-end Stator Winding Induction Motor Drives,”
Under Review, IEEE Trans. Ind. Electron.

Conferences

1. A. Edpuganti and A. Rathore, “Optimal low switching frequency pulsewidth modulation of medium voltage seven-level cascade-5/3H inverter,” *IEEE IECON*, Vienna, Austria, Nov 2013.

2. A. Edpuganti, A. Rathore, and J. Holtz, “New Optimal Pulsewidth Modulation for Single DC-Link Dual Inverter fed Open-end Stator Winding Induction Motor Drive,” *IEEE ECCE*, Pittsburgh, USA, Sept 2014.

3. A. Edpuganti and A. Rathore, “Fundamental switching frequency optimal pulsewidth modulation of medium voltage cascaded seven-level inverter,” *IEEE IAS Annu. Meeting*, Vancouver, Canada, Oct 2014.

4. A. Edpuganti and A. Rathore, “A survey of low-switching frequency modulation techniques for medium-voltage multilevel converters,” *IEEE IAS Annu. Meeting*, Vancouver, Canada, Oct 2014.

5. A. Edpuganti, A. Rathore, and A. Gupta, “Optimal fundamental switching frequency pulsewidth modulation of medium voltage cascade nine-level (9L) inverter,” *IEEE PEDES*, Mumbai, India, Dec 2014.

6. A. Edpuganti and A. Rathore, “Optimal Pulsewidth Modulation of Medium-Voltage Modular Multilevel Converter,” *IEEE IAS Annu. Meeting*, Dallas, Texas, USA, Oct 2015.

7. A. Edpuganti, A. Dwivedi, A. Rathore, and R. Srivastava, “Optimal Pulsewidth Modulation of Cascade Nine-Level (9L) Inverter for Medium Voltage High Power Industrial AC Drives ,” *IEEE IECON*, Yokohama, Japan, Nov 2015.

8. A. Edpuganti and A. Rathore, “Optimal Low-Switching Frequency Pulsewidth Modulation of Dual Modular Multilevel Converter for Medium-Voltage Open-end Winding Induction Motor Drive,” *Under Review, IEEE ECCE*, Milwaukee, USA, Sept 2016.