THEORETICAL STUDY OF ADVANCED FIELD-EFFECT TRANSISTORS BASED ON ALTERNATIVE CHANNEL MATERIALS FOR SUPPLY VOLTAGE REDUCTION

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DECLARATION

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information that have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Low Kain Lu

8 December 2015

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Abstract

Theoretical Study of Advanced Field-Effect Transistors based on Alternative Channel Materials for Supply Voltage Reduction

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Complementary-metal-oxide-semiconductor (CMOS) transistors have been commonly employed in the electronics for the past decades due to their excellent scalability, low cost, and high performance. Higher packing density per unit chip area and enhanced circuit performance can be achieved via the scaling of CMOS transistors. However, with the scaling of CMOS devices into the nanometer regime, the issues associated with the adverse short channel effects (SCEs) arise, leading to high leakage current which increases the static power of a transistor. Furthermore, exponential growth of the number of transistors per integrated circuit (IC) chip causes drastic increase of power density. All these contribute to high power consumption in an IC chip, which has become a serious problem as the technology advances.

In order to reduce the power consumption, power supply voltage (V_{DD}) needs to be lowered. Nevertheless, reduction of V_{DD} should not compromise the ON-current (I_{ON}) so that the switching speed of transistors can be sustained. In this context, metal-oxide-semiconductor field-effect transistors (MOSFETs) based on alternative channel materials with high product of carrier velocity and density of states (DOS) and

tunneling field-effect transistor (TFET) with steeper subthreshold slope (*S*) are promising candidates to enable the reduction of V_{DD}. In this thesis, MOSFETs with alternative potential channel materials and TFET are explored.

From the perspective of alternative channel materials, semiconductor alloys based on group IV materials, such as Ge and Sn, appear to be of great interest due to their tunable direct band gap and process or materials compatibility with the Si-based platform. We evaluate the electronic properties of $Ge_{1-x}Sn_x$ alloys using empirical pseudopotential method (EPM) for Sn composition varying from 0 to 20%. The effective masses of $Ge_{1-x}Sn_x$ alloys are subsequently extracted from the band edges along high symmetry lines. Based on the extracted effective mass of bulk GeSn, the transverse, longitudinal, and confinement effective masses are projected for the double-gate ultra-thin body (DG-UTB) n-MOSFET based on GeSn. The ballistic I_{ON} of GeSn-based DG-UTB n-MOSFET is investigated in order to assess its I_{ON} performance.

In addition to the conventional bulk and ultra-thin body channel materials from group IV and III-V, 2-dimensional (2D) monolayer materials, such as transition metal dichalcogenides (TMDs), with extremely thin body allow an excellent electrostatic control. This is desirable for the ultimately scaled CMOS to reduce the SCEs. We examine the electronic properties and the upper limit of the ballistic I_{ON} of MOSFETs based on hydrogenated silicene and germanene, so-called silicane and germanane, respectively. Their ON-current performances are compared with those of the TMDs based transistors. Silicane n-MOSFET outperforms the rest of n-channel transistors studied while silicane and germanane p-MOSFETs offer higher I_{ON} than 2D-TMDs p-MOSFETs.

In order to identify the potential channel materials with better voltage scalability for the reduction of the power consumption, the ultimate voltage scalability of a double-gate ultra-thin body MOSFET employing channel materials from group IV, III-V, and 2D materials is studied. The key performance metrics, including the voltage scalability and power delay product (PDP), are assessed based on the device specifications projected by the International Technology Roadmap for Semiconductors (ITRS) for high performance (HP) and low power (LP) applications. Channel materials from group IV, III-V, and black phosphorus (BP) are assessed based on the requirements for HP technology while 2D materials are evaluated according to LP technology requirements. It is found that Ge and GaSb transistors show good voltage scalability for HP application. For LP application, good voltage scalability and low PDP are attained in silicon, black phosphorus (BP), and silicane transistors.

For the transistor with steep subthreshold swing, we demonstrate a novel device structure for TFET with its source region extending into the channel region toward the drain. The proposed structure also exploits heterostructure with staggered (or type II) band alignment at the tunneling junction to enhance the I_{ON} of TFET. The horizontal heterostructure tunneling junction formed by the P^+ Ge source region underneath the P^- Si channel region enhances the I_{ON} by increasing the tunneling area which is scalable with the gate length. A more uniformly distributed electrostatic potential along the horizontal tunneling junction gives rise to steeper subthreshold characteristics.

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List of Symbols

a	Lattice parameters	nm
C_D	Gate-to-drain capacitance	F/cm^2
C_S	Gate-to-source capacitance	F/cm^2
C_G	Total gate capacitance	F/cm^2
C_{it}	Interface trap capacitance	F/cm^2
C_{OX}	Gate oxide capacitance	F/cm^2
C_Q	Quantum capacitance	F/cm^2
E_C	Conduction band energy	eV
E_g	Energy band gap	eV
E_g^Γ	Energy band gap at Γ valley	eV
E_g^L	Energy band gap at L valley	eV
$E_{f,d}$	Drain fermi energy	eV
$E_{f,s}$	Source fermi energy	eV
E_p	Kane energy	eV
E_V	Valence band energy	eV
f	Frequency	Hz
I_{DS}	Source to drain current	A/μm
$I_{D,sat}$	Saturation drain current	A/μm
$I_{LEAK,SD}$	Leakage current	A/μm
I_{OFF}	OFF-state current	A/μm
I_{ON}	ON-state current	A/μm
k	Boltzmann constant	eV/K
L_G	Gate length	m
m_0	Free electron effective mass	kg
$m_{e,l}^{*L}$	Longitudinal electron effective mass at L valley	kg
$m_{e,t}^{*L}$	Transverse electron effective mass at L valley	kg
$m_{e,l}^{*\Gamma}$	Longitudinal electron effective mass at Γ valley	kg

$m_{e,t}^{*\Gamma}$	Transverse electron effective mass at Γ valley	kg
$m_{e,l}^{*\Delta}$	Longitudinal electron effective mass at Δ valley	kg
$m_{e,t}^{*\Delta}$	Transverse electron effective mass at Δ valley	kg
$m_{lh}^{*\Gamma}$	Light hole effective mass	kg
$m_{hh}^{*\Gamma}$	Heavy hole effective mass	kg
m_x	Longitudinal effective mass	kg
m_y	Transverse effective mass	kg
m_z	Confinement effective mass	kg
Q_n	Electron density	cm^{-2}
Q_p	Hole density	cm^{-2}
P_{Active}	Active power consumption	W
$P_{Passive}$	Passive power consumption	W
q	Elementary charge	C
R_{SD}	Source-drain series resistance	Ω.μm
S	Subthreshold swing	mV/decade
T	Temperature	K
T_{body}	Body thickness	nm
τ_d	Time delay	s
V_{DS}	Drain voltage	V
V_{DD}	Power supply voltage	V
V_{GS}	Gate voltage	V
v_{inj}	Thermal injection velocity	ms^{-1}
V_{TH}	Threshold voltage	V
μ	Carrier mobility	$cm^2/V{\cdot}s$
W	Width of the transistor	m
$\gamma_1, \gamma_2, \gamma_3$	Luttinger parameters	

List of Abbreviation

2D	Two-dimensional
BP	Black phosphorus
BTBT	Band-to-band tunneling
CMOS	Complementary metal-oxide-semiconductor
CB	Conduction band
CBM	Conduction band minimum
CVD	Chemical vapor deposition
DFT-GGA	Density functional theory in general gradient approximation
VBM	Valence band maximum
E-k	Energy dispersion
EOT	Equivalent oxide thickness
EPM	Empirical pseudopotential method
DG	Double-gate
DOS	Density of states
FB-FET	Feedback field-effect transistor
GaSb	Gallium antimonide
Ge	Germanium
GeSn	Germanium-tin
HL	Heavy hole
HP	High performance
I-V	Current-voltage
IC	Integrated circuit
IMOS	Impact-ionization metal-oxide-semiconductor
ITRS	International Technology Roadmap for Semiconductors
InAs	Indium arsenide
$In_{0.3}Ga_{0.7}Sb$	Indium gallium antimonide
LH	Light hole

L_{OV}	Overlap length of the extended source
LP	Low power
MBE	Molecular beam epitaxy
MoS_2	Molybdenum disulfide
$MoSe_2$	Molybdenum diselenide
MOSFET	Metal-oxide-semiconductor field effect transistor
n-MOSFET	n-channel metal-oxide-semiconductor field-effect transistor
OPW	Orthogonalized plane wave
PAW	Projector-augmented plane wave
PBE	Perdew-Burke-Ernzerhof
p-MOSFET	p-channel metal-oxide-semiconductor field-effect transistor
SCEs	Short channel effects
S/D	Source / drain
Si	Silicon
SiO_2	Silicon dioxide
Sn	Tin
SO	Split-off
TCAD	Technology computer-aided design
TFET	Tunneling field-effect transistor
TMD	Transition metal dichalcogenides
T_{Si}	Silicon body thickness
UTB	Ultra-thin body
VASP	Vienna ab-initio simulation package
VB	Valance band
VCA	Virtual Crystal Approximation
WS_2	Tungsten disulfide
WSe_2	Tungsten diselenide
WKB	Wentzel-Kramers-Brillouin

Chapter 1

Introduction

1.1 Background

In complementary metal-oxide semiconductor (CMOS) technology, the logic functions in the integrated circuits (IC) are realized using n-channel and p-channel metal-oxide-semiconductor field effect transistors (n-MOSFETs and p-MOSFETs, respectively). Moore's law [1] predicts that the number of transistors in an IC approximately doubles every two years. The semiconductor industry follows the Moore's law for the past few decades. Continued scaling of CMOS devices enables the number of transistors on IC chips to increase at an exponential rate. Higher packing density allows more logic circuits to be fabricated on a given IC chip area which in turn reduces the cost per function.

The saturation drain current ($I_{D,sat}$) of an idealized long-channel MOSFET is inversely proportional to the gate length. Thus, the downscaling of gate length is beneficial for achieving higher $I_{D,sat}$, leading to enhancement in circuit speed performance. However, as transistor dimensions are aggressively scaled to the deep sub-micrometer regime and beyond, several serious challenges arise which make the downscaling of transistors extremely difficult. Among severe challenges include short-channel effects (SCEs) and reliability issue. Short channel effects, such as drain induced barrier lowering (DIBL), V_{TH} roll-off, and punch-through, significantly increase the OFF-state current (I_{OFF}) of highly scaled MOSFETs.

While higher packing density and improved circuit speed can be achieved via the scaling of CMOS devices, it also causes high power consumption issue. Basically,

power consumption of an IC can be categorized into two components: active power (P_{Active}) and passive power ($P_{Passive}$), as given by:

$$P_{Active} \propto C_L V_{DD}^2 f \,, \tag{1.1}$$

$$P_{Passive} \propto I_{OFF} V_{DD} \,, \tag{1.2}$$

where C_L is the load capacitance, V_{DD} is the power supply voltage, f is the switching frequency of the circuit, and I_{OFF} is the OFF-state current. Fig. 1.1 shows that both active and static power density increase with reduction of gate length. Power consumption has become a more serious issue for advanced technology nodes [2]-[4].

Equation 1.1 and 1.2 show that both P_{Active} and $P_{Passive}$ are strongly dependent on V_{DD}. Hence, V_{DD} reduction is one of the effective approaches to reduce the power consumption. Nonetheless, the downscaling of V_{DD} requires careful considerations. The switching speed of the circuit is inversely proportional to the time delay (τ_d), which is given by

$$\tau_d \propto \frac{V_{DD}}{I_{ON}} \,. \tag{1.3}$$

To ensure faster switching speed of circuits, the change in I_{ON} with V_{DD} downscaling needs to be smaller than the change in V_{DD}.

To address the power consumption issue in CMOS technology through V_{DD} reduction, two promising methods are focused in this thesis. The first approach is to explore MOSFETs with alternative channel materials which offer a higher product of carrier injection velocity and density of states (DOS) than Silicon. The second one is the use of novel transistors with steep switching characteristic. In the next two sections, the technological background and development of these two approaches are detailed.

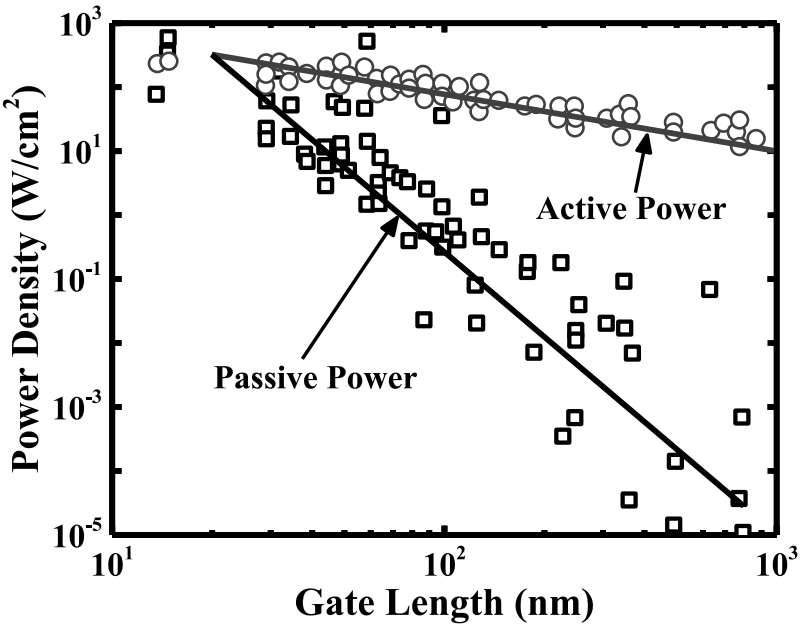

Fig. 1.1. Active power and static power versus gate length collected from literature. Both active and static power show increasing trend with the reduction of gate length. The contribution of static power to the overall power density increases and eventually becomes dominant at the highly scaled gate length. This figure is reproduced from Ref. [2].

1.2 Transistors with Alternative Channel Material

As transistor dimensions progress to the nanometer regime, quasi-ballistic transport dominates the drive current. The $I_{D,sat}$ equation of a MOSFET in quasi-ballistic regime is given by [5]:

$$I_{D,sat} = C_G W v_{inj} \left(\frac{1-r_c}{1+r_c} \right) (V_{GS} - V_{TH}), \tag{1.4}$$

where C_G is the gate capacitance, W is the channel width, v_{inj} is the thermal injection velocity, and r_c is the backscattering coefficient. From 1.4, one of the key parameters affecting the $I_{D,sat}$ of highly scaled transistors is the v_{inj}. It was found that v_{inj} is dependent on low-field mobility while r_c is inversely proportional to low-field mobility [6]-[7].

In addition, $I_{D,sat}$ is also a function of gate capacitance (C_G) whose value is determined by the series connection of the gate oxide capacitance (C_{OX}) and the quantum capacitance (C_Q). C_{OX} is determined by the thickness and the dielectric constant of gate oxide while C_Q depends on the DOS of the channel material. The downscaling of equivalent oxide thickness (EOT) with technology nodes and introduction of high mobility channel materials can result in the value of C_{OX} being comparable or even larger than that of C_Q. Under this condition, the charge in the channel is limited by the DOS which degrades the I_{ON}. Thus, it is crucial to utilize channel materials with reasonably high DOS in order to have a condition of $C_Q >> C_{OX}$ such that C_G is mainly determined by C_{OX} for achieving higher current.

For extremely scaled transistors, the channel length can be comparable or even smaller than the carrier mean free path. This leads to the operation in the ballistic regime where r_c is equal to zero. Fig. 1.2 shows the I_{DS}-V_{GS} characteristics of two transistors employing different channel materials with the same subthreshold swing. It is observed that material with higher product of injection velocity and DOS exhibits higher I_{ON} at the same gate overdrive. In other words, the same I_{ON} can be obtained at a lower V_{DD}, enabling the downscaling of V_{DD} without compromising I_{ON}. Therefore, it is desirable to employ materials with high v_{inj} and large DOS in the extremely scaled transistor to achieve higher I_{ON} at reduced V_{DD}-V_{TH}.

For the past few decades, silicon (Si) semiconductor material is primarily employed in CMOS technology. However, silicon being the mainstream semiconductor in the ICs is expected to eventually reach its scaling limit. Therefore, instead of depending on the conventional scaling approach, a variety of other techniques have been used to improve the performance of Si-based CMOS technology.

In semiconductor industry, strain techniques have been used to enhance the I_{ON} of Si-MOSFETs by boosting the mobility [9]-[20]. For instance, at the 90 nm technology node [9], SiGe liner stressor and SiN source/drain (S/D) stressors were employed by Intel Corporation to induce beneficial strains in the Si-based p-MOSFETs and n-MOSFET, respectively. The induced strain enhances the I_{ON} of Si-based MOSFETs via the modification of the electronic band structures.

However, the required improvement in current density and other device parameters, such as intrinsic delay, could no longer be satisfied by solely straining the conventional Si-based MOSFET. Due to the mobility limitation faced in Si MOSFETs, various alternative channel materials have been researched extensively in order to identify potential materials which exhibit superior performance than Si MOSFETs.

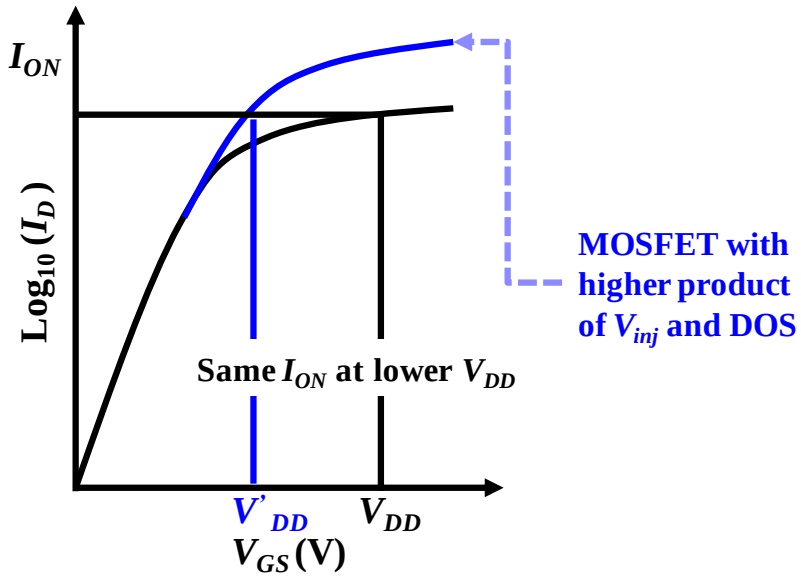

Fig. 1.2. $I_{DS} - V_{GS}$ of MOSFETs with different carrier injection velocity and density of states. Under the same I_{ON} and subthreshold swing, MOSFET with higher product of injection velocity and DOS (blue solid line) delivers the required I_{ON} at a lower V_{DD} as compared to the MOSFETs with lower injection velocity and DOS (black solid curve). In other words, MOSFETs with higher product of injection velocity and DOS can achieve higher I_{ON} at the same V_{DD}.

1.2.1 Group IV and III-V Semiconductors

The carrier injection velocities of channel materials can be indicated by their mobility since the carrier injection velocity is related to the low field mobility. Table 1.1 lists the bulk mobilities of some of the potential channel materials. Among promising alternative materials with high mobility for n-channel MOSFETs are III-V compound semiconductors due to their light electron effective mass. At a given I_{OFF}, III-V n-MOSFETs with higher carrier injection velocity owing to their smaller electron effective mass allow higher I_{ON} to be delivered. Hence, III-V n-MOSFETs are promising for achieving high speed at lower operating V_{DD} [21]-[31]. However, low electron DOS in III-V semiconductors may counteract the benefit of high injection velocity, limiting their I_{ON} in technology nodes with extremely scaled EOT.

For the group IV semiconductors, germanium (Ge) offers the highest hole mobility among the materials listed in Table 1.1. Apart from the elemental semiconductors of group IV, semiconductor alloys have been extensively used for altering material properties through tuning the alloy composition. The Si/Ge material system of group IV has been widely studied for applications in optoelectronics and electronics. However, the indirect nature of the band gap of the Si/Ge material system is a fundamental limitation for its application in optoelectronics.

Table 1.1. Bulk electron and hole mobility of various alternative channel materials [8].

	Si	**Ge**	**GaAs**	**InP**	**InAs**	**InSb**
Electron mobility ($cm^2/V{\cdot}s$)	1350	3900	8500	5400	40000	77000
Hole mobility ($cm^2/V{\cdot}s$)	480	1900	400	200	500	850

Recently, $Ge_{1-x}Sn_x$ alloy has attracted immense interest as a promising alternative alloy to achieve tunable direct band gaps in group IV diamond-cubic materials. With the incorporation of substitutional tin (Sn), $Ge_{1-x}Sn_x$ shows higher carrier mobility than Ge. By tuning the Sn composition, the band gap of $Ge_{1-x}Sn_x$ alloys exhibits a transition from indirect to direct. Very good progress has been made in realizing high-performance Ge P-MOSFETs [32]-[39]. Recently, GeSn channel P-MOSFETs were experimentally demonstrated to have higher hole mobility than Ge channel P-MOSFETs [40]-[42]. As compared to III-V semiconductors, $Ge_{1-x}Sn_x$ material systems make possible the fabrication of optical and electronic devices with group IV materials using a CMOS compatible process flow. As a result, the manufacturing cost can be reduced due to easier integration of $Ge_{1-x}Sn_x$ into current Si platform as compared to III-V materials.

1.2.2 Two-Dimensional Materials

Lower dimensional materials, such as 2D monolayer materials, are currently of much interest due to their superior electronic properties. One of the beneficial features of 2D monolayer materials is the extremely small body thickness which allows excellent electrostatic control of the channel potential by the gate electrode. The excellent electrostatic integrity inherent in the 2D material is desirable for the ultimately scaled CMOS to minimize the short channel effects arising from the downscaling of the transistors dimensions. Graphene, a 2D honeycomb network of carbon atoms, has attracted much attention because of its unique material properties [43]-[44]. The high mobility makes graphene highly attractive for nanoelectronic applications [45].

Despite the superior electronic properties of graphene, it has its own shortcomings, such as high leakage current originated from the zero band gap characteristic. This has sparked tremendous interest toward the exploration of other 2D materials. Among the possible 2D material systems are those from the family of transition metal dichalcogenides (TMD) (MoS_2, $MoSe_2$ WS_2, WSe_2 etc.) [46]-[48]. Unlike graphene, monolayer 2D-TMDs have intrinsic band gaps (1–2 eV) which make them possible as alternative channel materials for CMOS devices. The theoretical and experimental studies show that 2D-TMDs transistors are good for low power applications due to their large band gap and good electrostatic control [49]-[52].

1.3 Transistor with Steep Switching Behavior

The aggressive downscaling of CMOS transistors has to be accompanied with the reduction of V_{DD} so that constant electric fields in the transistors can be maintained. In order to sustain the same I_{ON} at reduced V_{DD}, the V_{TH} of the conventional MOSFETs needs to be reduced. However, decreasing V_{TH} without scaling the subthreshold swing (S) will result in a high I_{OFF} as depicted in Fig. 1.3. This leads to higher passive power consumption which is proportional to I_{OFF}. Thus, a steeper switching characteristic is required in order to retain the same I_{ON} and I_{OFF} when V_{DD} is reduced.

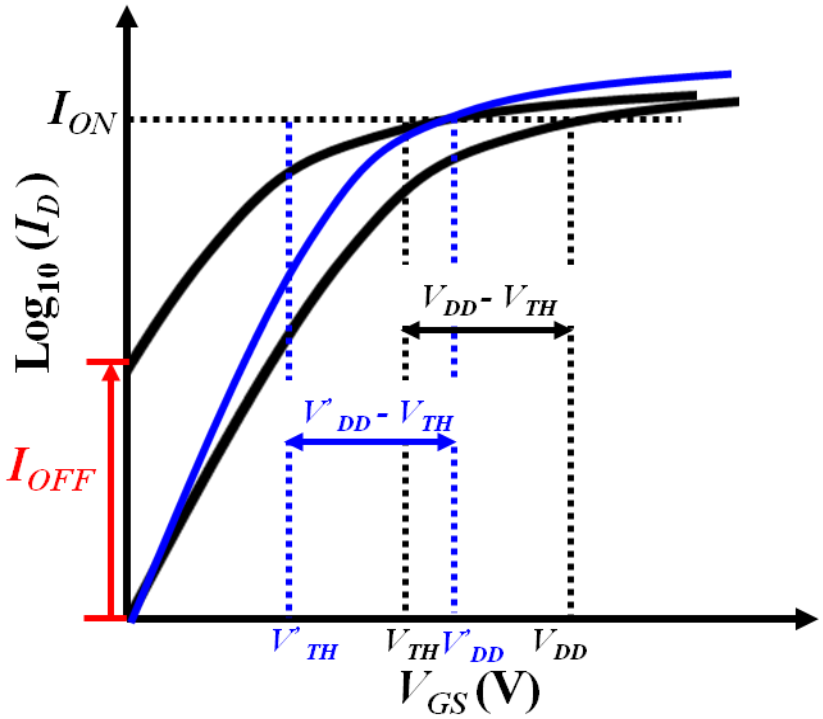

Fig. 1.3. $I_{DS} - V_{GS}$ of a conventional MOSFET (solid black curve) and steep-slope transistor (solid blue curve). When the power supply voltage is reduced from V_{DD} to V'_{DD}, the threshold voltage needs to be scaled down as well in order to maintain the same current drivability. However, an increase in the I_{OFF} is observed in the MOSFET with the V_{DD} reduction. Hence, transistor with steeper subthreshold characteristic is required in order to keep the same I_{OFF} at a reduced V_{DD}, as shown by the blue curve.

The operating mechanism of MOSFET is based on the injection of carrier from the source side over the potential barrier to the channel region with the potential barrier being modulated by the gate potential. As illustrated in Fig. 1.4, carriers at the source have a thermal energy distribution which follows the Fermi-Dirac distribution. Hence, there are always a finite number of high energy electrons that can surmount the potential barrier at the subthreshold operation region. These high energy electrons contribute to the subthreshold current which sets the lower limit of the MOSFETs subthreshold swing. The *S* of the MOSFETs can be mathematically described by

$$S = \ln 10 \frac{kT}{q}\left(1+\frac{C_D + C_{it}}{C_{OX}}\right) > \ln 10 \frac{kT}{q}, \qquad (1.5)$$

where k is the Boltzmann constant, T is the temperature, q is the electronic charge, C_D is the depletion capacitance, C_{OX} is the gate oxide capacitance, and C_{it} is the capacitance due to the interface traps. Based on equation 1.5, the lowest S that can be achieved by the conventional MOSFETs at room temperature is 60 mV/decade.

Due to this fundamental limit, I_{OFF} of MOSFETs will eventually reach an unacceptable level with the V_{DD} scaling (which requires reduction of V_{TH}). This calls for novel transistors that can achieve S smaller than 60 mV/decade at room temperature, so-called steep-slope transistors. Among the potential steep-slope transistors are impact-ionization metal-oxide-semiconductor (I-MOS) device [53]-[56], feedback field-effect transistor (FB-FET) [57]-[58], mechanical gate field-effect transistor [59]-[60], and tunneling field-effect transistor (TFET) [61]-[67].

The operating mechanism of IMOS is based on avalanche breakdown in the reverse biased p-i-n diode. In spite of having steeper S in I-MOS, a larger gate voltage is required to induce high electric field for the impact ionization to occur. This translates to higher power consumption due to larger bias required. In addition, I-MOS suffers from reliability issues due to the carrier trapping and the creation of interface states caused by the hot carriers. In FB-FET, the static power consumption is high as the p+-i-n+ diode works in the forward bias regime. For mechanical gate field-effect transistor, the high operating voltage and intrinsic delay limit its potential applications.

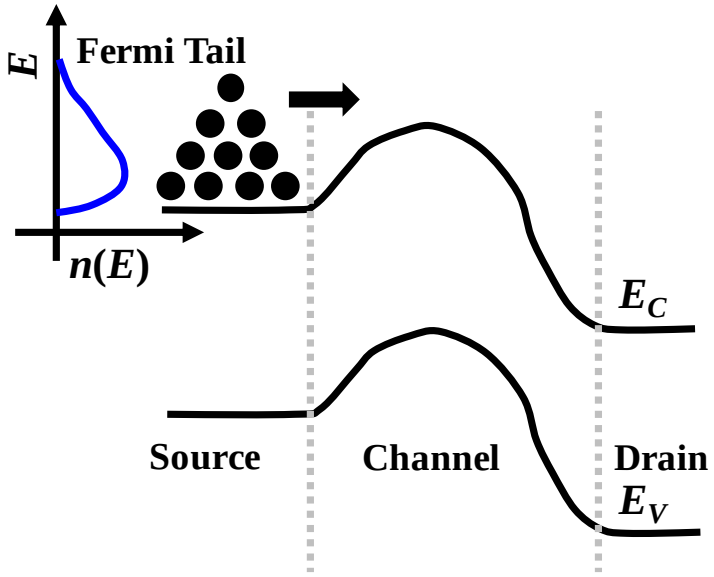

Fig. 1.4. Energy band diagram along source, channel, and drain region of a MOSFET. The energy distribution of carriers at the source region follows the Fermi Dirac distribution, resulting in finite amount of carriers available at high energy levels. Carriers in the tail of the Fermi distribution can surpass the potential barriers and contribute to the subthreshold current. This subthreshold current sets a lower limit for the switching characteristic of a conventional MOSFET.

1.3.1 Working Principles of TFET

Unlike the steep-slope transistors mentioned above, TFET utilizes the gate-controlled band-to-band tunneling (BTBT) mechanism to give rise to *S* less than 60 mV/decade at room temperature. The general structure of a TFET is shown in Fig. 1.5(a). It shares the same device structure as the typical MOSFET. However, the drain and source doping are complementary of each other. TFET is basically a gated P-I-N structure which makes use of the BTBT mechanism to give rise to the ON-state current. Fig. 1.5(b) shows the energy band along the source to drain in order to illustrate the operating mechanism of TFET. At the OFF-state, the tunneling barrier width (W_T) is substantially large which prevents the carriers in the source from tunneling to the channel. The leakage current of TFET is expected to be smaller than

that of MOSFETs since the high energy tail electrons are cut off by the band gap in the source. To switch on n-TFETs, a positive gate voltage is applied across the channel region which pulls the energy band down as shown by blue line in Fig. 1.5(b). The tunneling barrier is reduced exponentially which allows the carriers to tunnel from the source to the channel contributing to the ON-state current.

Recent theoretical research reports on TFETs reveal that TFET has the potential for the low power application with the V_{DD} operation below 0.5 V thanks to its steeper switching behavior and low OFF-state current. In this thesis, TFET is explored as a steep-slope transistor to address the power consumption issue.

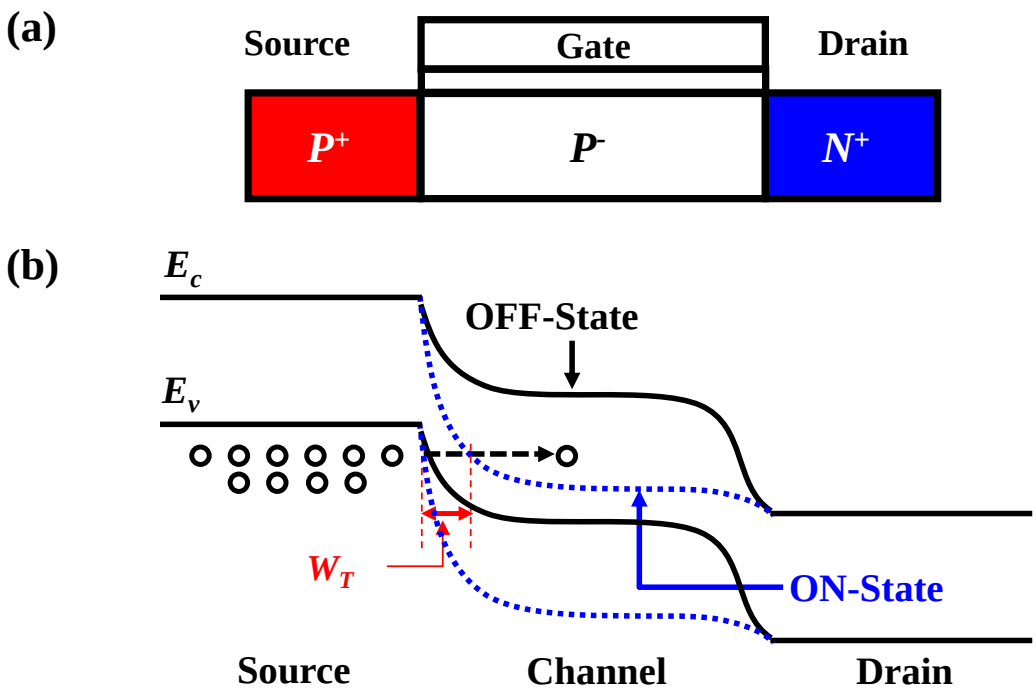

Fig. 1.5. (a) Schematic of P-I-N TFET, (b) Energy band along source to drain for OFF and ON-state. At the OFF-state, the tunneling barrier width (W_T) is large which prohibits the carriers from the source to tunnel to the channel region and the high energy carriers are filtered out by the band gap. Thus, the leakage current of TFET is expected to be lower. At the ON-state, W_T is reduced by the gate potential which permits band-to-band tunneling to occur, giving rise to an ON-state current.

1.3.2 Development and Designs of TFET Technology

In 1992, the first lateral surface tunnel transistors (STTs) based on III-V compound semiconductors [68]-[69] were proposed by Baba and Uemura after the discovery of the BTBT phenomenon by Leo Esaki in 1957 [70]. Since then, there have been extensive experimental research works conducted on improving the performance of TFETs based on Si [61]-[62], germanium (Ge) [71]-[73], and III-V [74]-[76]. In addition, various theoretical and simulation works with the aim of understanding the physical insights for device design of TFET have been carried out [64], [77]-[88].

Although a steeper switching characteristic can be achieved in TFETs, the I_{ON} of TFETs is still too low to satisfy the drive current requirement for low power application projected by the International Technology Roadmap for Semiconductors (ITRS) [89]. This calls for innovations and designs to enhance the I_{ON} of TFETs. Fig. 1.6 shows the main design considerations of TFET.

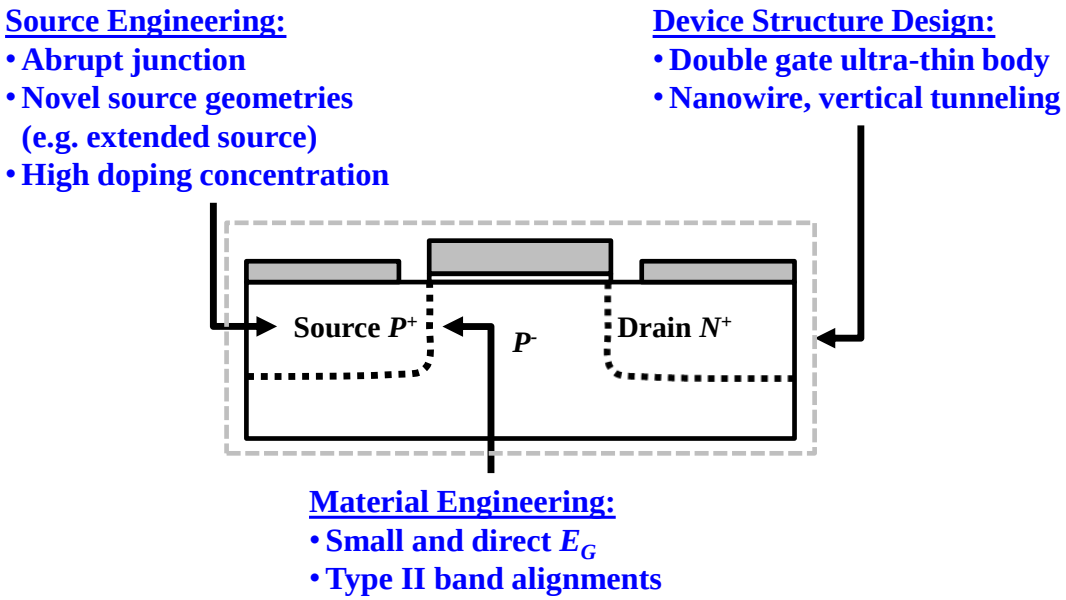

Fig. 1.6. Key points for the design considerations of TFET.

The BTBT rate of TFETs can be further improved by engineering the source junction. A highly doped and abrupt junction is desired for achieving high electric field and narrow depletion width at the tunneling junction. High electric field and narrow depletion region reduce the tunneling barrier width which in turn increases the BTBT rate exponentially. Specially-designed source structures, such as extended source structures, have been proposed to improve the *S* and drive currents of TFETs [61], [90].

Since the BTBT rate is inversely dependent on the band gap, materials with smaller and direct band gap are preferred. Ge and III-V semiconductors are potential materials due to their larger BTBT rate resulted from the smaller and direct band gaps. Another way of increasing the tunneling rate is the use of heterojunction with type II staggered band alignment [91]-[99]. The conduction band offset in the type II heterojunction reduces the effective band gap (energy difference between conduction band (CB) in the channel and valence band (VB) in the source). Thus, higher tunneling current can be obtained from the well-designed type II heterojunction.

Similar to the conventional MOSFETs, the current of TFETs is also modulated by the gate potential. Hence, it is important to enhance the gate control over the tunneling junction for the current improvement. This can be achieved by using the same device structures employed in the MOSFETs, such as multigate structure with ultra-thin body [100]-[101]. In addition, novel device structures have been proposed, including vertical TFETs and TFETs with source tunneling junction extending into the channel region.

1.4 Objectives of Thesis

The main objective of this thesis is to address the power consumption issue faced by the current CMOS technology via the reduction of power supply voltage. Two technology approaches are explored. The first option is to employ MOSFETs with alternative channel materials which offer higher product of carrier injection velocity and DOS. The second approach is to use TFET. For MOSFETs with high carrier injection velocity and DOS, various channel materials across group IV, III-V, and 2D atomically thin materials are explored to assess their potentials as alternative channel materials beyond silicon. For group IV semiconductors, $Ge_{1-x}Sn_x$ alloy is investigated by examining its electronic properties and ballistic I_{ON} at different tin (Sn) compositions. 2D materials can be an attractive alternative for low power applications due to their larger band gap and the excellent electrostatic integrity inherent in a two-dimensional system. In this context, 2D materials from group IV (hydrogenated silicene and germanene) are evaluated and compared to the 2D-transition metal dichalcogenides (2D-TMDs) in terms of their ballistic I_{ON}. Subsequently, the voltage scalability of ultra-thin body transistor employing channel materials from group IV, III-V, and 2D materials is assessed based on the ITRS-projected device specifications for high performance (HP) and low power (LP) technologies. For the V_{DD} reduction by employing TFET, a novel TFET device structure based on type II tunneling junction is proposed, aiming at improving the ON-current and the subthreshold swing. The findings from this thesis are part of the research efforts in scaling down the V_{DD} to mitigate the power consumption issues for highly scaled technology nodes.

1.5 Organization of Thesis

This thesis comprises 6 chapters. Chapter 1 covers the introduction of this research work, including the background information on the power consumption problems faced in the semiconductor industry and the possible solutions for the V_{DD} reduction to reduce the power consumption in IC chips.

In Chapter 2, the electronic properties of $Ge_{1-x}Sn_x$ alloy are studied by theoretically calculating its electronic band structures (*E*-*k*) at different Sn compositions. The *E*-*k* dispersion is obtained from the empirical pseudopotential method (EPM) where the fitting parameters are adjusted such that the band gaps from the calculated *E*-*k* dispersion match with those from the experimental results. The effective masses for both electron and hole are subsequently extracted along various high symmetry lines using a parabolic line fit. In addition, employing the effective-mass Hamiltonian for diamond semiconductor, the band edge dispersion at the Γ valley calculated by 8-band k.p. method is fitted to that obtained from the EPM approach. This is to derive the Luttinger-like parameters for $Ge_{1-x}Sn_x$ alloys. Using the extracted effective mass from the bulk GeSn material system, the equivalent effective masses of GeSn in the 2-dimensional system are projected. Subsequently, the ballistic I_{ON} of double-gate ultra-thin body n-MOSFET based on GeSn is calculated in order to assess their ultimate ON-current performance.

In Chapter 3, the ballistic I_{ON} of double-gate ultra-thin body (DG-UTB) transistors based 2D materials are investigated. The 2D materials studied consist of hydrogenated silicene and germanene, i.e., silicane and germanane, respectively. The electronic band structures of silicane and germanane are calculated using the first-principles density functional theory. Subsequently, the ballistic performance of MOSFETs is evaluated via the semi-classical ballistic transport model. The I_{ON} of

silicane and germanane are compared with those of 2D-transistion metal dichalcogenides (2D-TMDs) based on the ITRS projected requirements for HP and LOP technologies.

In Chapter 4, the ultimate voltage scalability of double-gate ultra-thin body (DG-UTB) MOSFETs employing materials from group IV, III-V, and 2D materials are examined based on the requirements for high performance (HP) and low power (LP) logic applications. The device specifications for HP and LP technologies are obtained from the 2013 edition of the International Technology Roadmap for Semiconductors (ITRS). The channel materials considered are composed of Ge, GaSb, InAs, $In_{0.3}Ga_{0.7}Sb$, and 2D materials [black phosphorus (BP), silicane, germanane, MoS_2, $MoSe_2$, WS_2, WSe_2]. The performance metrics (minimum scalable V_{DD}, power delay product (PDP)) are benchmarked based on the ones of Si MOSFET.

In Chapter 5, a novel TFET structure with an L-shaped Ge source is proposed. The device consists of a Ge source that extends underneath a Si-channel region and it is separated from the drain region by an insulator (SiO_2). By optimizing the overlap length of the extended source (L_{OV}) and the Si body thickness (T_{Si}), the current due to vertical band-to-band tunneling (BTBT) of the Ge–Si hetero-junction could be increased significantly and is scalable with L_{OV}. In addition, a steeper subthreshold swing can be achieved due to a more uniformly distributed electrostatic potential along the tunneling heterojunction.

Chapter 6 summarizes the key findings of this thesis and provides possible future directions based on the works carried out.

Chapter 2

GeSn Alloy as Channel Material for Metal-Oxide-Semiconductor Field-Effect Transistors

2.1 Introduction

As discussed in Chapter 1, GeSn alloys can be used in transistors and its material properties can be engineered by tuning the Sn composition. By tuning the Sn composition, the band gap of $Ge_{1-x}Sn_x$ alloys exhibits a transition from indirect to direct. The tunable direct band gap of $Ge_{1-x}Sn_x$ makes possible the fabrication of optical and electronic devices with group IV materials using a complementary-metal-oxide-semiconductor (CMOS) compatible process flow.

The GeSn material system can be grown epitaxially using various growth techniques such as molecular beam epitaxy (MBE) [102]-[114] and chemical vapor deposition (CVD) [115]-[120]. Pulsed UV laser annealing of amorphous Ge-Sn film has been used to synthesize the metastable crystalline $Ge_{1-x}Sn_x$ alloys [121]. Other techniques used to grow crystalline $Ge_{1-x}Sn_x$ are dc-diode sputtering [122] and RF sputtering [123]-[125]. An optical absorption measurement for diamond cubic $Ge_{1-x}Sn_x$ alloys performed by He *et al*. [108] has shown that the range of direct energy gap of $Ge_{1-x}Sn_x$ to be $0.35 < E_g < 0.80$ eV for $0.15 < x < 0$. Later, Guevara *et al*. [125] reported that the critical Sn composition (x_c) corresponding to the transition from indirect to direct band gap is experimentally observed to lie between $0.10 < x_c < 0.13$ determined from transmittance measurements using a fast-Fourier-transform infrared interferometer. D'.Costa *et al*. [120] and R. Chen *et al*. [113] reported the critical

concentration to be 0.11 and 0.071, respectively. First-principles and empirical methods have been used for the calculations of $Ge_{1-x}Sn_x$ alloys physical parameters. From first-principles calculations, the optical band gap bowing parameter (*b*) is reported to be 2.06 [126], 2.75 [127], 2.49 [128], and 1.90 [129] while calculations based on Virtual Crystal Approximation (VCA) generally give a smaller optical band gap bowing (0.94 [130], 0.25 [131], 0.4 [132], and 0.30 [133]).

The important parameters associated with the band structure of $Ge_{1-x}Sn_x$ have not been fully examined to date. One of the important fundamental parameters used in the design of electronic and optical devices is the effective mass. Most of the studies of $Ge_{1-x}Sn_x$ alloys have focused on band gaps and critical composition. However, the present lack of investigation on the effective mass parameters of $Ge_{1-x}Sn_x$ alloys has accentuated the need for theoretical calculation of $Ge_{1-x}Sn_x$ effective mass parameters.

In this Chapter, the empirical pseudopotential method (EPM) is adopted for calculating the band structures of $Ge_{1-x}Sn_x$ alloys along high symmetry lines in the Brillouin zone for Sn composition varying from 5% to 20%. The effective masses of electron and hole are extracted from the band edges using a parabolic line fit. Based on the band gap energies at L valley and Γ valley obtained from fitting the experimental data, the adjustable parameters of EPM are tuned in order to reproduce the band features that are in good agreement with experimental data.

This Chapter is organized as follows: A brief background of GeSn alloy research progress is discussed in section 2.1. Empirical pseudopotential method (EPM) and $Ge_{1-x}Sn_x$ band structure calculations approaches using EPM are described in Section 2.2.1 and 2.2.2, respectively. In Section 2.2.3, the results of $Ge_{1-x}Sn_x$ band structures calculations and effective masses are presented and discussed. In Section 2.3, we review the 8-band k.p model and the derivation of the Luttinger parameters

for $Ge_{1-x}Sn_x$ at different Sn composition. The ballistic I_{ON} of double-gate ultra-thin body n-channel metal-oxide-semiconductor field-effect transistor (n-MOSFET) based on GeSn alloy is discussed in Section 2.4. Section 2.5 summarizes the key points of this chapter.

2.2 Electronic Band Structure Analysis of GeSn Alloy

2.2.1 The empirical pseudopotential method

The EPM method [134] is employed for the calculation of the electronic band structure of $Ge_{1-x}Sn_x$ with the diamond cubic structure. The EPM is based on the orthogonalized plane wave (OPW) [135] method where the crystal wavefunction is constructed to be orthogonal to the core states. The pseudopotential Hamiltonian of semiconductors is given by:

$$H = -\frac{\hbar^2}{2m}\nabla^2 + V_p(\boldsymbol{r}), \tag{2.1}$$

where V_p is the pseudopotential of the crystal that can be expanded into a Fourier series over the reciprocal lattice *G* as:

$$V_p(\boldsymbol{r}) = \sum_{\boldsymbol{G}} \left(V^S(\boldsymbol{G}) S^S(\boldsymbol{G}) + iV^A(\boldsymbol{G}) S^A(\boldsymbol{G}) \right) e^{i\boldsymbol{G}.\boldsymbol{r}}. \tag{2.2}$$

In Eq. 2.2, $S^S(\boldsymbol{G})$ and $S^A(\boldsymbol{G})$ are the symmetric and asymmetric structural factors, respectively while $V^S(\boldsymbol{G})$ and $V^A(\boldsymbol{G})$ are the symmetric and asymmetric pseudopotential form factors, respectively. They are related to the cation atomic potential $V_1(\boldsymbol{G})$ and anion atomic potential $V_2(\boldsymbol{G})$ in the unit cell by:

$$V^S(\boldsymbol{G}) = \frac{1}{2}\left[V_1(\boldsymbol{G}) + V_2(\boldsymbol{G})\right], \tag{2.3}$$

$$V^A(\boldsymbol{G}) = \frac{1}{2}\left[V_1(\boldsymbol{G}) - V_2(\boldsymbol{G})\right]. \tag{2.4}$$

The adjustment of the form factors corresponds to the selection of a good, though not unique, pseudopotential which can describe the material characteristics reasonably well. Since Ge and Sn both crystallize in the diamond structure, their asymmetric form factors are essentially zero [$V^A(G) = 0$]. Hence, it remains only the symmetric form factors for $Ge_{1-x}Sn_x$ alloys. The basic set of plane waves used in our EPM calculation were chosen such that $|G+k|$ lies within a sphere bounded by a kinetic energy E_1 with a magnitude of 13.5 Ry. By utilizing a perturbation method by Lowdin [136], the second order contribution from all vectors G that satisfied the criterion of $E_1 < \frac{\hbar^2}{2m}|\boldsymbol{G}+\boldsymbol{k}|^2 < E_2$ with E_2 of 20.5 Ry was considered [137].

Spin-orbit interaction is included for the accurate calculation of the band structures with the addition of the following spin-orbit matrix element:

$$H_{SO} = (\boldsymbol{K_i} \times \boldsymbol{K_j}).\sigma_{S,S'}\left[-i\lambda^S.S^S(\boldsymbol{G}) + \lambda^A.S^A(\boldsymbol{G})\right], \tag{2.5}$$

where $\boldsymbol{K_i} = \boldsymbol{G_i} + \boldsymbol{k}$, $\boldsymbol{K_j} = \boldsymbol{G_j} + \boldsymbol{k}$ and $\sigma_{S,S'}$ is the usual Pauli spin index denoting either spin up or down. λ^S and λ^A are the symmetric and asymmetric spin-orbit contributions, respectively. They are related the cationic and anionic spin-orbit contribution, λ_c and λ_a, by

$$\lambda^S = \frac{1}{2}(\lambda_c + \lambda_a), \lambda^A = \frac{1}{2}(\lambda_c - \lambda_a), \tag{2.6}$$

where

$$\lambda_c = \mu B_{nl}^c(\boldsymbol{K}_i) B_{nl}^c(\boldsymbol{K}_j), \lambda_a = \alpha\mu B_{nl}^a(\boldsymbol{K}_i) B_{nl}^a(\boldsymbol{K}_j). \quad (2.7)$$

μ is an adjustable spin-orbit parameter and α is the ratio of the spin splitting of the free anion and cation atoms. $B_{nl}(\boldsymbol{K})$ is defined by

$$B_{nl}(\boldsymbol{K}) = \beta \int_0^\infty j_{nl}(\boldsymbol{Kr}) R_{nl}(\boldsymbol{r}) r^2 dr. \quad (2.8)$$

where β is a normalization constant. $j_{nl}(\boldsymbol{Kr})$ and $R_{nl}(\boldsymbol{r})$ are the spherical Bessel's function of l th angular momentum and the radial part of the core wavefunction, respectively.

2.2.2 $Ge_{1-x}Sn_x$ band structure calculations approach

The virtual crystal approximation (VCA) has been commonly used for the calculation of band structures of semiconductor alloys. In VCA, the semiconductor alloy consists of fictitious atoms each having an atomic potential being a compositionally weighted average of the atomic potentials of the constituent elemental atoms. Thus, VCA models alloys properties using atoms with mixed atomic potentials. However, VCA fails to describe correctly the characteristics of semiconductor alloys having band gap energies that vary strongly non-linearly with composition [138]. This inaccuracy arises from the nonlinear nature of composition dependence of atomic potential which is not well captured by VCA. Experimental works reported the direct band gap bowing parameter of $Ge_{1-x}Sn_x$ to be 1.94 [120], 2.1 [113], 2.3 [139]. These large bowing parameters illustrate the nonlinear nature in which properties of $Ge_{1-x}Sn_x$ alloy depend on its composition.

In this study, the band structures of $Ge_{1-x}Sn_x$ alloys with different Sn compositions [0.05, 0.08, 0.11, 0.14, 0.17, and 0.20] were calculated using the EPM approach. The $Ge_{1-x}Sn_x$ alloy studied here is a random alloy with face-centered cubic (FCC) lattice, i.e., Sn atoms substitute for Ge atoms randomly throughout the crystal. The lattice constant $Ge_{1-x}Sn_x$ alloy was obtained by linear interpolation between the lattice constants of Ge and Sn atoms according to Vegard's rule.

Instead of using VCA in which the weighted potentials of the constituent atoms (Ge and Sn) are added to obtain the pseudopotential form factors, a set of pseudopotential form factors was adjusted for each Sn composition for the $Ge_{1-x}Sn_x$ alloy. The bowing parameters of direct and indirect band gap obtained by Costa *et al*. [120] were adopted in this work for the calculation of band gap energies at L and Γ valley at various Sn compositions. The band gap energies of Ref. [120] were used as benchmarks. For each Sn composition, the form factors were iteratively updated and fed into EPM until the calculated band structure of $Ge_{1-x}Sn_x$ yields band gap energies which are in good agreement with the experimental values. The iterative method used in finding sets of form factors yielding band gap energies in good agreements with the experimental values is illustrated in Fig. 2.1.

In order to calculate the electronic properties of $Ge_{1-x}Sn_x$ alloy in a reliable manner, the models used in our EPM, such as the cutoff energies, structural factors, and form factors, were calibrated in order to reproduce the electronic properties of Ge reported in the literature. Based on the calibrated models, the calculated values of band gap and effective mass (electron and hole) of Ge at L and Γ valley are in good agreement with reported values, as shown in Table 2.1, Table 2.2, and Table 2.3.

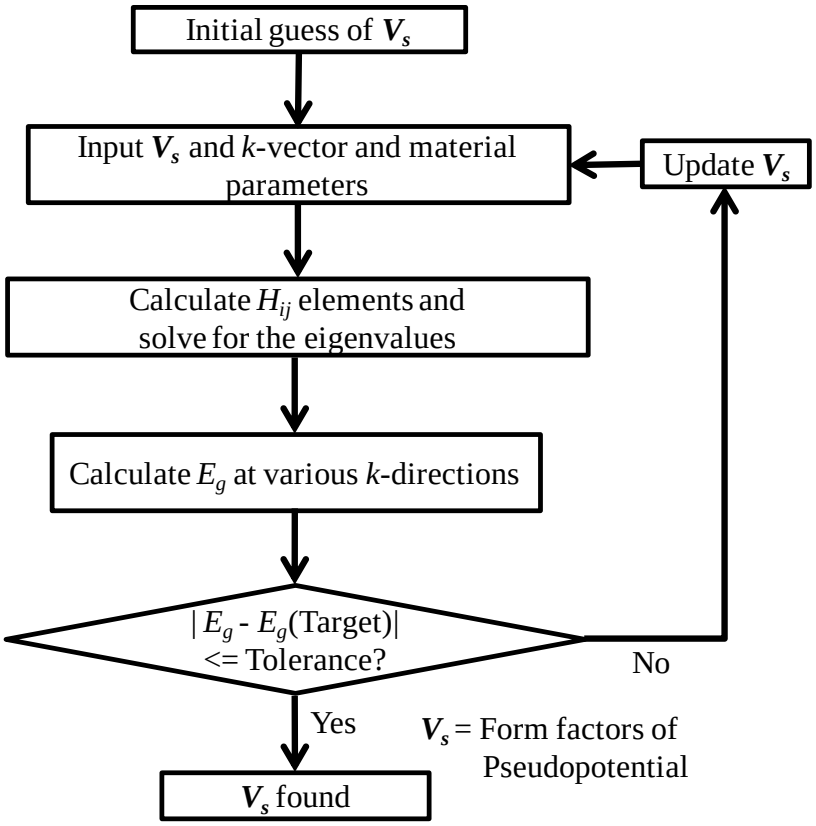

Fig. 2.1. Flow chart of the iterative process used in finding sets of pseudopotential form factors yielding band gap energies in good agreements with the experimental values.

2.2.3 Results and Discussions of $Ge_{1-x}Sn_x$ band structure

The final adjusted form factors of $Ge_{1-x}Sn_x$ are summarized in Table 2.1 for Sn composition ranging from 5% to 20%. E_g^{Γ} and E_g^{L} are the band gap energies at the Γ and L valley, respectively. Overall, the fitted E_g^{Γ} and E_g^{L} agree well with experimentally reported band gap energies [120]. Using the fitted form factors, the electronic band structures of $Ge_{1-x}Sn_x$ along high symmetry lines in the Brillouin zone were calculated and plotted in Fig. 2.2. Fig. 2.3 shows the indirect to direct band gap transition for $Ge_{1-x}Sn_x$. For x = 0.05, the conduction band minimal (CBM) is located at L valley which is 0.573 eV above the valence band maximal (VBM) [Fig. 2.3 (a)].

Fig. 2.3 (b) illustrates the critical composition of 11% where the band gap energies of L and Γ valley are equal. Fig. 2.3 (c) depicts the band structure of $Ge_{1-x}Sn_x$ with x = 0.20 which exhibits a direct gap characteristic with a band gap energy of 0.247 eV. The band gap energy of $Ge_{1-x}Sn_x$ at X (E_g^X), L (E_g^L), and Γ (E_g^Γ) valleys obtained from the band structures calculated by EPM is plotted against Sn compositions in Fig. 2.4. The E_g^Γ and E_g^L versus Sn composition curves from our calculations matched the corresponding curves of Ref. [120] which are plotted using dotted gray lines in Fig. 2.4.

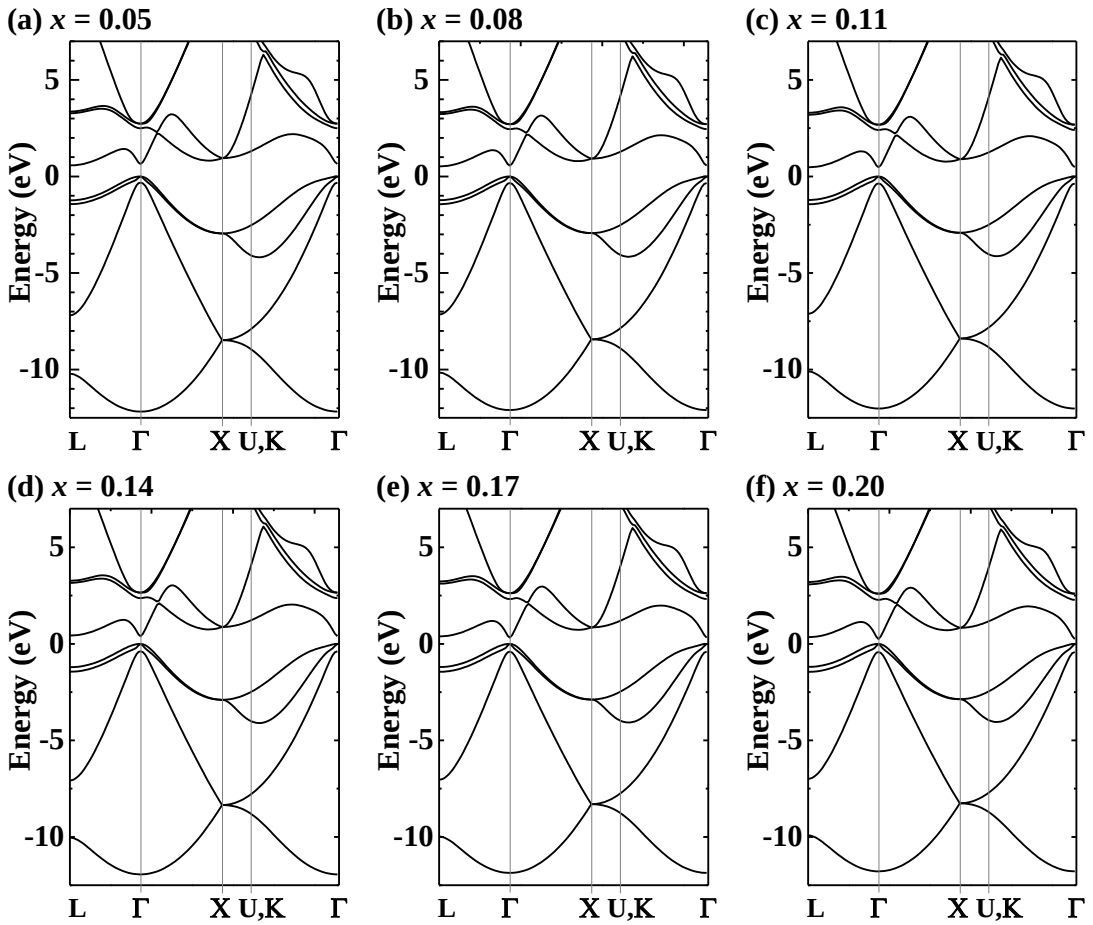

Fig. 2.2. Full band structure of $Ge_{1-x}Sn_x$ along high symmetry lines in the Brillouin zone for (a) x = 0.05, (b) x = 0.08, (c) x = 0.11, (d) x = 0.14, (e) x = 0.17, and (f) x = 0.20.

Table 2.1. The fitted form factors for $Ge_{1-x}Sn_x$ with various Sn compositions used in EPM. The calculated band gap energies are in good agreement with the reported data [120].

x	$V^S(3)$	$V^S(8)$	$V^S(11)$	E_g^Γ		E_g^L	
				Expt. [120]	This work	Expt. [120]	This work
0.00	-0.27200	0.05700	0.01700	0.8000	0.8019	0.660	0.6581
0.05	-0.26972	0.05575	0.01516	0.6470	0.6478	0.573	0.5727
0.08	-0.26825	0.05495	0.01418	0.5602	0.5605	0.524	0.5240
0.11	-0.26600	0.05345	0.01380	0.4766	0.4771	0.477	0.4769
0.14	-0.26410	0.05220	0.01330	0.3966	0.3966	0.432	0.4330
0.17	-0.26315	0.05190	0.01210	0.3201	0.3183	0.390	0.3900
0.20	-0.26130	0.05084	0.01160	0.2470	0.2475	0.350	0.3505

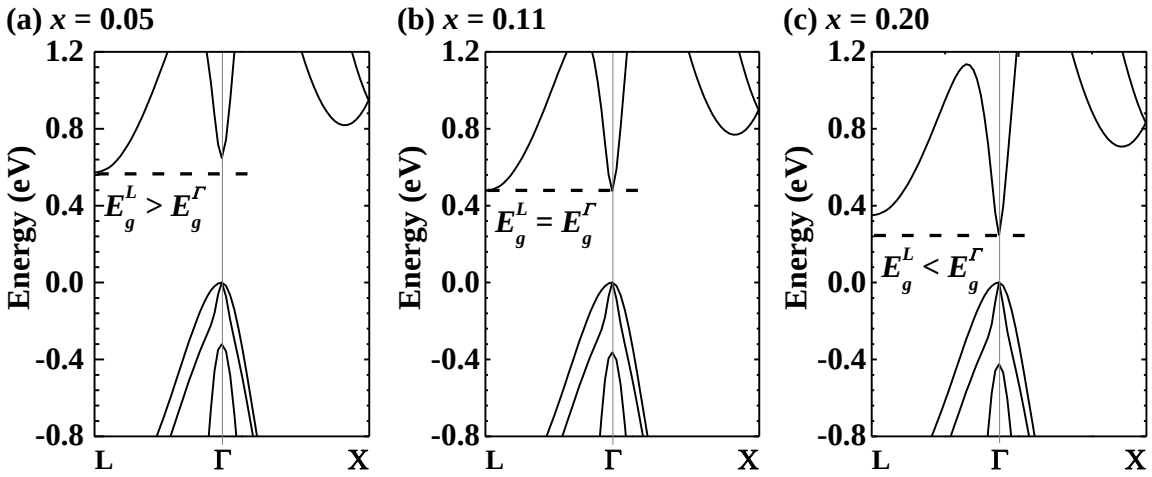

Fig. 2.3. Zoomed-in view of the electronic band structures of $Ge_{1-x}Sn_x$ along high symmetry lines for (a) x = 0.05, (b) x = 0.11, and (c) x = 0.20, showing the transition from indirect [Fig. 2.3(a)] to direct band gap [Fig. 2.3(c)] of $Ge_{1-x}Sn_x$. Fig. 2.3(b) illustrates the critical composition of 11% where the band gap energies of L and Γ valley are equal.

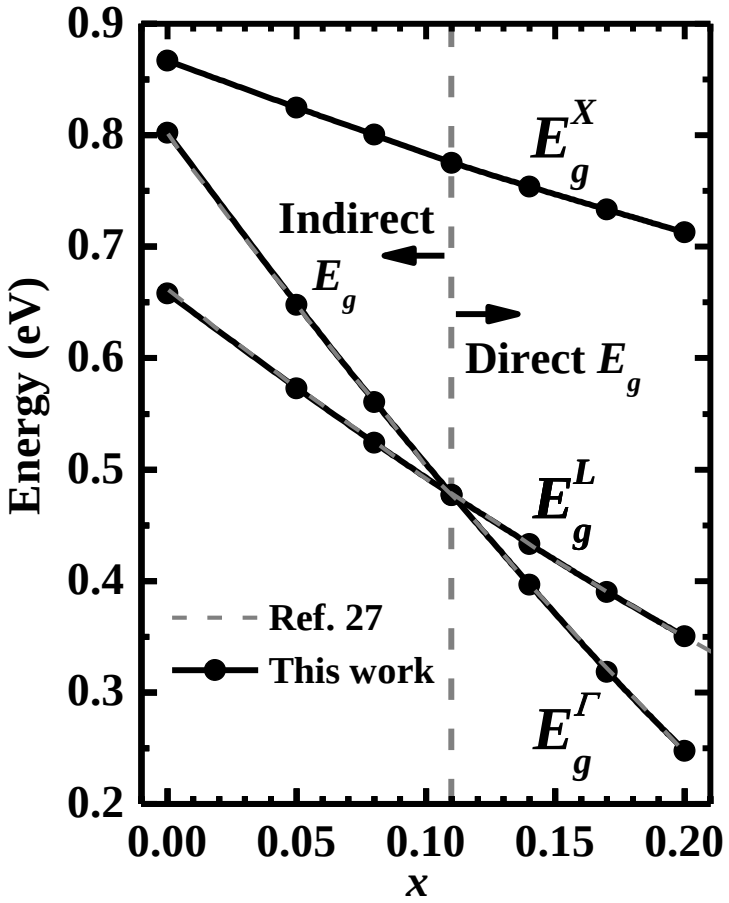

Fig. 2.4. The calculated band gap energies of X, L, and Γ valley at various Sn compositions. The band gap energies of L and Γ valley agree well with the experimentally reported values Ref. [120].

From the calculated band structure of $Ge_{1-x}Sn_x$ alloy, the electron and hole effective masses along [100], [110], and [111] direction of the Brillouin zone were extracted using a simple parabolic line fit. All the extracted effective masses are in the unit of free electron mass, m_0. The heavy-hole (HH), light-hole (LH), split-off (SO), and conduction band effective masses of Germanium (Ge) (corresponding to $Ge_{1-x}Sn_x$ with Sn composition x = 0.00) extracted from our EPM calculation were compared to reported data in the literature in Table 2.2 and Table 2.3. The calculated effective masses in the conduction band (Table 2.2) and in the valence band (Table 2.3) for Ge agree well with reported data.

Table 2.2. Effective masses of conduction band at symmetry valleys (L, Γ, and Δ) in the Brillouin zone.

	(m_0 unit)	$m_{e,l}^{*L}$	$m_{e,t}^{*L}$	$m_e^{*\Gamma}$	$m_{e,l}^{*\Delta}$	$m_{e,t}^{*\Delta}$
Ge	This work	1.595	0.092	0.0420	0.952	0.206
	Literature	1.578[a]	0.093[a]	0.0470[a]	0.889[a]	0.194[a]
		1.610[b]	0.081[b]	0.0380[b]	1.350[b]	0.290[b]
		1.568[c]	0.094[c]	0.0490[c]	1.851[c]	0.195[c]

[a]Ref.[140], [b]Ref.[141], [c]Ref.[142].

Table 2.3. Effective masses of heavy-hole, light-hole and split-off bands along symmetry lines [(100), (110), and (111)] in the Brillouin zone.

	(m_0 unit)	$m_{hh}^{*\Gamma}$			$m_{lh}^{*\Gamma}$			m_{so}
		(100)	(110)	(111)	(100)	(110)	(111)	
Ge	This work	0.226	0.439	0.597	0.0529	0.0476	0.0463	0.116
	Literature	0.251[a]	0.467[a]	0.623[a]	0.0600[a]	0.0530[a]	0.0520[a]	0.128[a]
		0.254[b]	0.477[b]	0.390[b]	0.0490[b]	0.0560[b]	0.0550[b]	0.097[c]

[a]Ref.[140], [b]Ref.[142], [c]Ref.[143].

The HH and LH effective masses of $Ge_{1-x}Sn_x$ against Sn compositions are depicted in Fig. 2.5(a) and 2.5(b), respectively. From Fig. 2.5(a), a small variation (less than 7% with respect to HH effective mass of Ge) of HH effective mass with the Sn composition was noticed along [100], [110], and [111] directions. For all Sn compositions, HH effective mass is the largest along [111] direction followed by [110] and [100] direction. Fig. 2.5(b) shows that LH effective mass decreases with progressively higher Sn composition along [100], [110], and [111] directions. LH along [111] has the smallest effective mass compared to that of [110] and [100] direction for the Sn compositions investigated. LH effective masses of different Sn composition were fitted with a quadratic polynomial. The fitted bowing equations for LH effective mass along [100], [110], and [111] directions are summarized in Table 2.4.

Table 2.4. The bowing equations for light-hole and electron effective masses fitted with a quadratic polynomial for $0 \leq x \leq 0.20$.

Effective Mass	Bowing equation (least squares fit)
m_{LH} [100]	$0.03669x^2 - 0.1781x + 0.05288$
m_{LH} [110]	$-0.01199x^2 - 0.1456x + 0.04759$
m_{LH} [111]	$-0.01992x^2 - 0.1384x + 0.04628$
m_e [111]	$0.009216x^2 - 0.1299x + 0.04202$

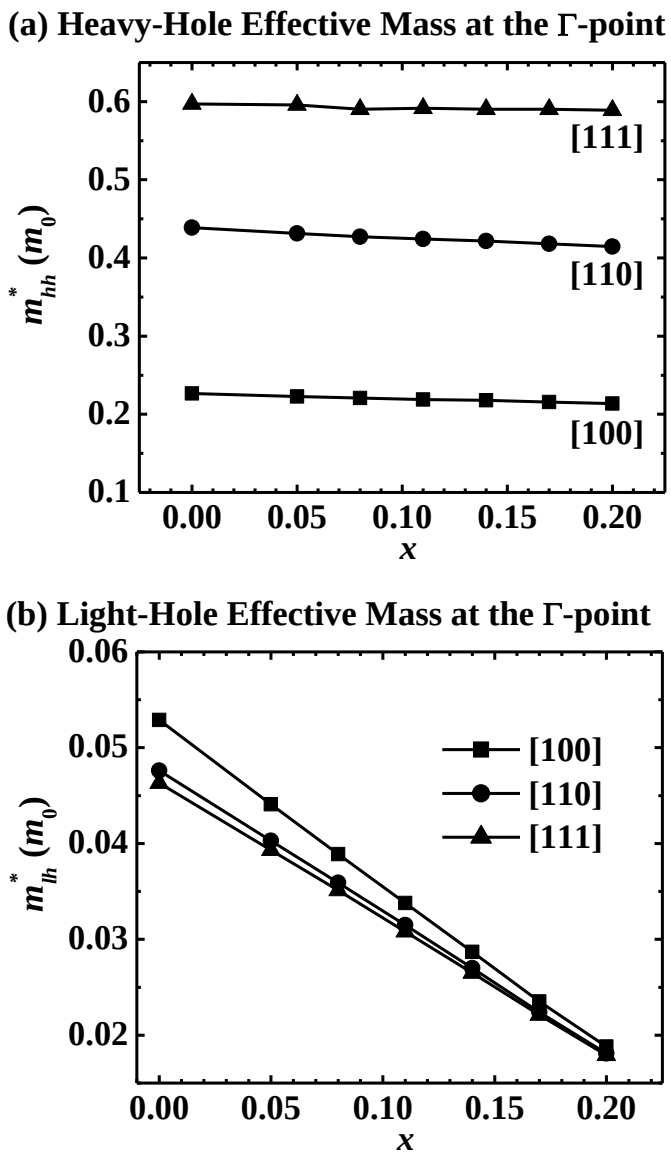

Fig. 2.5. (a) Heavy-hole (HH) and (b) light-hole (LH) effective masses of $Ge_{1-x}Sn_x$ along high symmetry lines in the Brillouin zone for x ranging from 0.0 to 0.20.

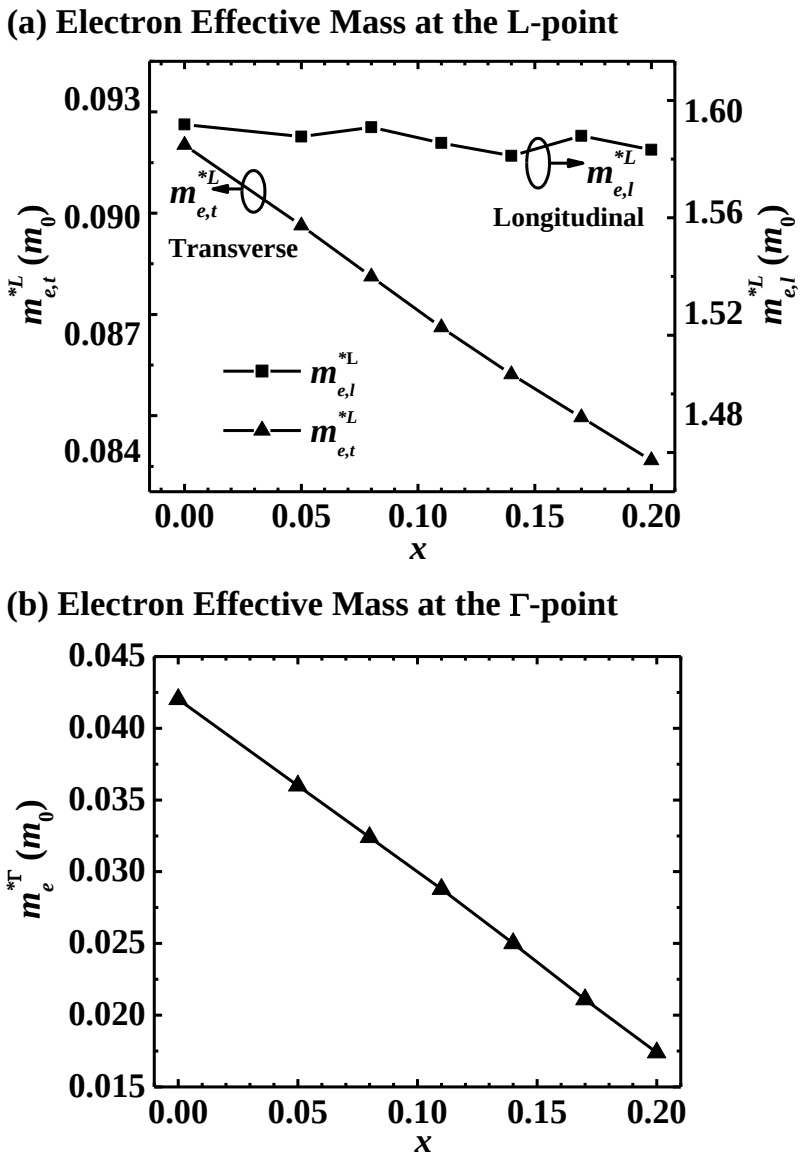

Fig. 2.6. Electron effective masses of $Ge_{1-x}Sn_x$ along high symmetry lines in the Brillouin zone for x ranging from 0.0 to 0.20: (a) Longitudinal and transverse electron effective mass at L valley, (b) Electron effective mass at Γ valley.

Fig. 2.6(a) shows the transverse $m^{*L}_{e,t}$ and longitudinal $m^{*L}_{e,l}$ electron effective masses at L valley. The effect of varying Sn composition in $Ge_{1-x}Sn_x$ is almost negligible for the longitudinal electron effective mass $m^{*L}_{e,l}$. The variation of $m^{*L}_{e,l}$ of $Ge_{1-x}Sn_x$ with respect to $m^{*L}_{e,l}$ of Ge is less than 1.5%. For transverse electron effective mass $m^{*L}_{e,t}$, it shows a nearly linear reduction trend with increasing Sn composition.

The electron effective mass at Γ valley $m_e^{*\Gamma}$ is shown in Fig. 2.6(b). By raising Sn composition in $Ge_{1-x}Sn_x$ from $x = 0$ to $x = 0.2$, $m_e^{*\Gamma}$ is reduced noticeably by about 60%. The bowing equation for the electron effective masses is deduced and summarized in Table 2.4.

The band structures for bulk $Ge_{1-x}Sn_x$ alloys were calculated in order to investigate the dependence of effective masses of bulk $Ge_{1-x}Sn_x$ alloys along different crystal directions on each crystal plane orientation. It should be noted that we are referring to band structures of bulk $Ge_{1-x}Sn_x$ and not of $Ge_{1-x}Sn_x$ crystal surfaces. Three common surface orientations of (100), (110), and (111) were studied. For each plane orientation, the effective masses along all in-plane directions were considered. Fig. 2.7-2.9 portray the effect of plane orientation and in-plane directions on electron and hole effective masses at Γ- valley. The inset of Fig. 2.7 shows the top views of wafers with (100), (110), and (111) planes. For each plane, various in-plane directions within the horizontal and vertical axes (from 0° to 90°) were considered. For (100) plane, 0° and 90° correspond to [001] and [010] directions, respectively. For (110) plane, 0° and 90° were taken along [001] and $[1\bar{1}0]$ directions. For (111) plane, the corresponding directions for 0° and 90° are $[\bar{1}10]$ and $[\bar{1}\bar{1}2]$, respectively.

From Fig. 2.7(a) and 2.7(b), the LH effective mass of (100) and (110) plane orientations shows slight anisotropy. For (100) plane orientation, the LH effective mass decreases with increasing channel direction from 0° to 50° while it starts to increase from 50° to 90° [Fig. 2.7(a)]. Fig. 2.7(b) shows the trend of decreased LH effective mass with increasing in-plane directions from 0° to 90° for (110) plane orientation. Fig. 2.7(c) illustrates that the LH effective mass of (111) plane is isotropic with all the in-plane directions having a similar effective mass.

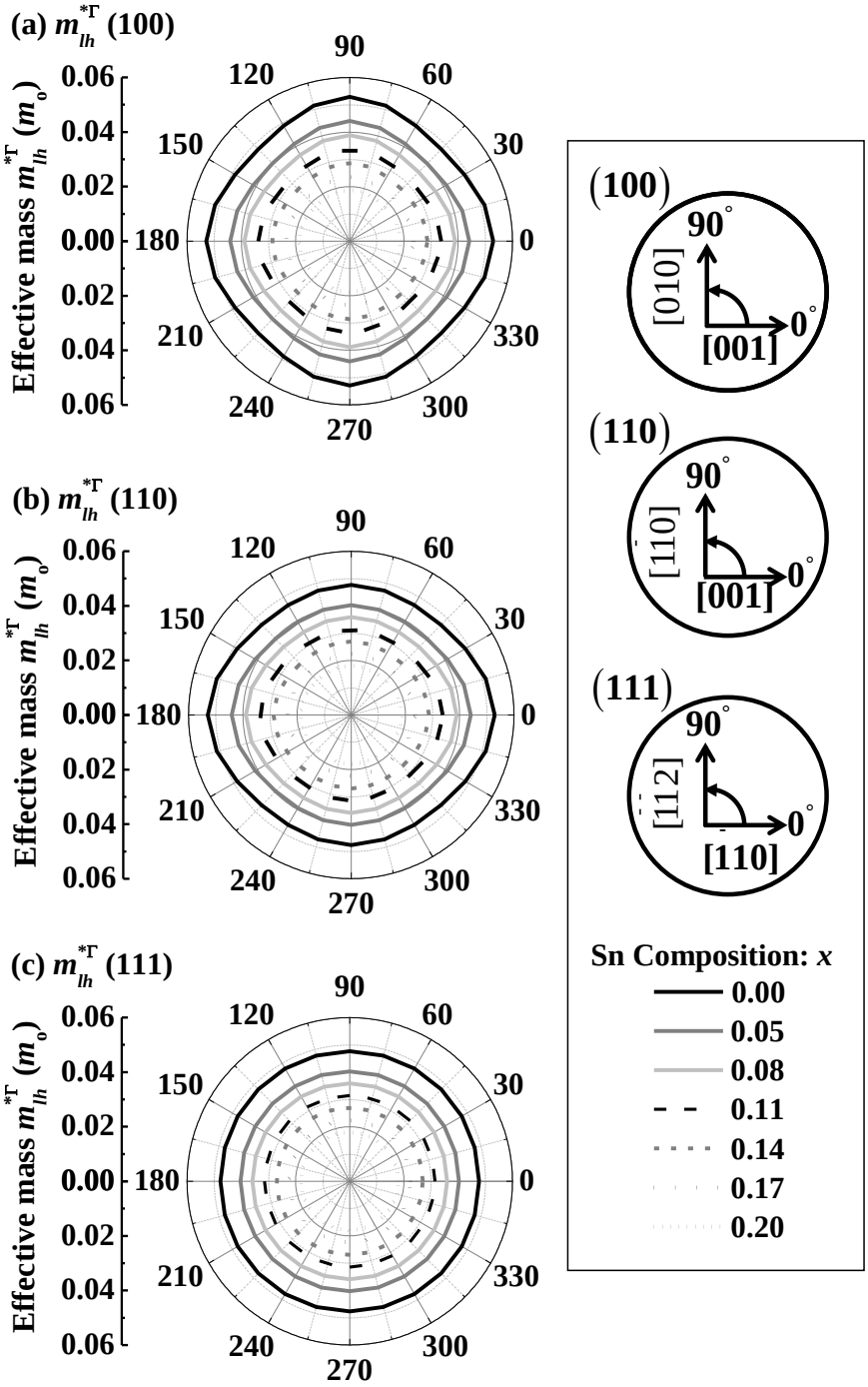

Fig. 2.7. The effective masses for light-hole, heavy-hole, and conduction band at Γ-valley of $Ge_{1-x}Sn_x$ for three common plane orientations [(100), (110), and (111)] and various in-plane directions. The LH effective masses along various in-plane directions for different plane orientations: (a) (100), (b) (110), and (c) (111). The LH effective mass of (100) and (110) shows slight anisotropy.

For the HH effective mass, an evident anisotropy was observed for (100) and (110) plane orientations. For (100) plane orientation, HH effective mass increases from 0° to 45° and decreases from 45° to 90° shown in Fig. 2.8(a). From Fig. 2.8(b), HH effective mass shows a similar trend as that of (100) plane orientation with increasing effective mass from 0° to 60° and decreasing from 60° to 90°. The HH of (111) plane orientation is rather isotropic for all channel directions shown in Fig. 2.8(c). The reduction of the HH effective mass with increasing Sn composition for three planes and all plane orientations is much less pronounced compared to the reduction seen in the LH effective mass.

For electron effective mass at Γ valley, it appears to be independent of the in-plane directions for all (100), (110), and (111) plane directions shown in Fig. 2.9(a)-2.9(c). Three plane orientations demonstrate a similar trend of electron effective mass along all in-plane directions.

Overall, the effective masses of LH, HH, and conduction band at Γ valley along all in-plane directions decrease with the increasing of Sn composition for all three plane orientations. This observation is consistent with the fact of reduced band gap energy of $Ge_{1-x}Sn_x$ alloy with increasing Sn composition which leads to smaller effective masses for $Ge_{1-x}Sn_x$ alloy with higher Sn composition.

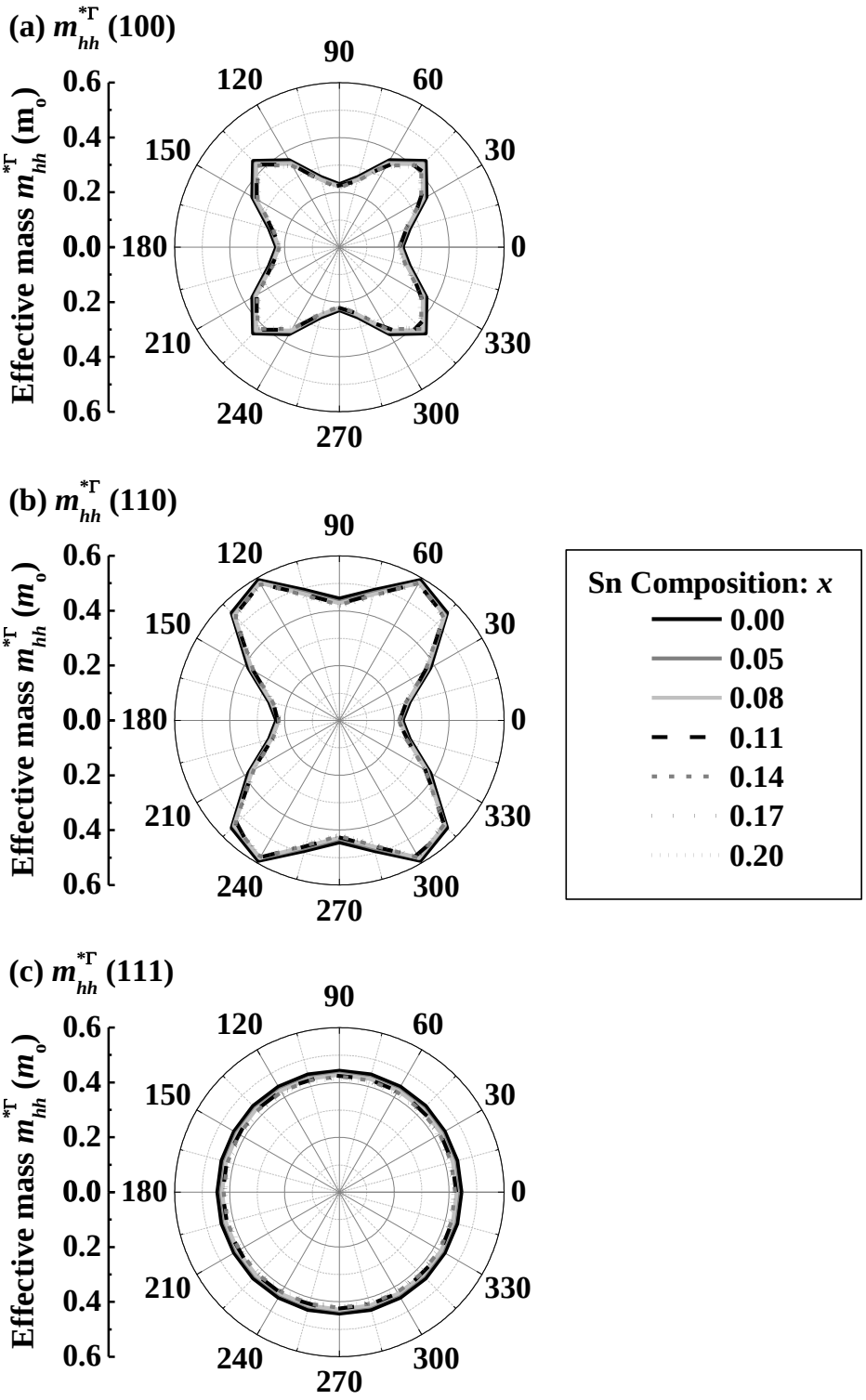

Fig. 2.8. The effective masses of HH for three plane orientations: (a) (100), (b) (110), and (c) (111). The effective masses for (100) and (110) plane orientations show evident anisotropy.

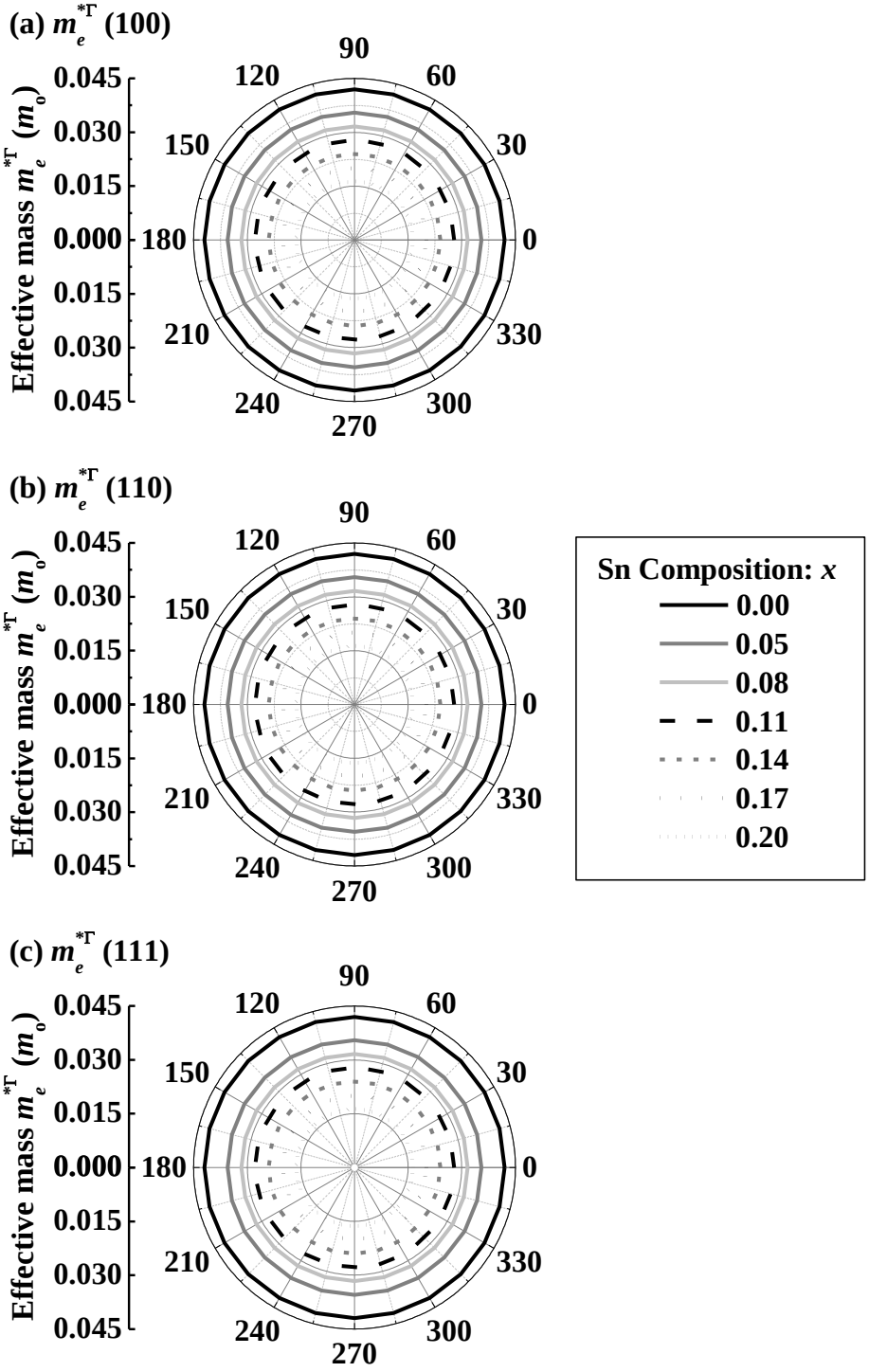

Fig. 2.9. The effective masses of electron for three plane orientations: (a) (100), (b) (110), and (c) (111). The effective masses for all plane orientations are isotropic for all the in-plane directions.

2.3 Derivation of Effective Mass Parameters

2.3.1 Effective Mass Approximation

k.p method has been commonly used for obtaining the electronic band structures of semiconductor materials for device designs, such as carrier mobility [144] and optical gain of quantum well laser [145]-[147]. It provides a computationally efficient means to calculate the band structures of different crystalline surfaces and orientations. The extraction of k.p effective mass parameters can be obtained by fitting the electronic band structures of k.p method to that of EPM [137], [146]-[147]. Using 8-band k.p Hamiltonian [148], the band edge dispersion at Γ valley obtained by k.p method was fitted to the EPM results by tuning the adjustable Luttinger-like parameters. The 8-band Hamiltonian for a diamond structure is given as:

$$H = \begin{bmatrix} C & 0 & \frac{1}{\sqrt{2}}P_-^* & -\sqrt{\frac{2}{3}}P_Z & -\frac{1}{\sqrt{6}}P_+^* & 0 & -\frac{1}{\sqrt{3}}P_Z & -\frac{1}{\sqrt{3}}P_+^* \\ 0 & C & 0 & \frac{1}{\sqrt{6}}P_-^* & -\sqrt{\frac{2}{3}}P_Z & -\frac{1}{\sqrt{2}}P_+^* & -\frac{1}{\sqrt{3}}P_-^* & \frac{1}{\sqrt{3}}P_Z \\ \frac{1}{\sqrt{2}}P_- & 0 & HH & S & -R & 0 & \frac{S}{\sqrt{2}} & -\sqrt{2}R \\ -\sqrt{\frac{2}{3}}P_Z & \frac{1}{\sqrt{6}}P_- & S^* & LH & 0 & -R & -D & -\sqrt{\frac{2}{3}}S \\ -\frac{1}{\sqrt{6}}P_+ & -\sqrt{\frac{2}{3}}P_Z & -R^* & 0 & LH & -S & -\sqrt{\frac{2}{3}}S^* & D \\ 0 & -\frac{1}{\sqrt{2}}P_+ & 0 & -R^* & -S^* & HH & \sqrt{2}R^* & \frac{S^*}{\sqrt{2}} \\ -\frac{1}{\sqrt{3}}P_Z & -\frac{1}{\sqrt{3}}P_- & \frac{S^*}{\sqrt{2}} & -D & -\sqrt{\frac{2}{3}}S & \sqrt{2}R & V & 0 \\ -\frac{1}{\sqrt{3}}P_+ & \frac{1}{\sqrt{3}}P_Z & -\sqrt{2}R^* & -\sqrt{\frac{2}{3}}S^* & D & \frac{S}{\sqrt{2}} & 0 & V \end{bmatrix}, \quad (2.9)$$

where

$$C = E_g^{\Gamma} + \frac{\hbar^2}{2\mathrm{m}_0}\left(\frac{1}{m_c} - \frac{E_p}{3}\left[\frac{2}{E_g^{\Gamma}} + \frac{1}{E_g^{\Gamma} + \Delta}\right]\right)\left(k_x^2 + k_y^2 + k_z^2\right), \quad (2.10a)$$

$$HH = -\frac{\hbar^2}{2\mathrm{m}_0}\left[\left(\gamma_1 + \gamma_2\right)\left(k_x^2 + k_y^2\right) + \left(\gamma_1 - 2\gamma_2\right)k_z^2\right], \quad (2.10b)$$

$$LH = -\frac{\hbar^2}{2\mathrm{m}_0}\left[\left(\gamma_1 - \gamma_2\right)\left(k_x^2 + k_y^2\right) + \left(\gamma_1 + 2\gamma_2\right)k_z^2\right], \quad (2.10c)$$

$$V = -\frac{\hbar^2}{2\mathrm{m}_0}\gamma_1\left(k_x^2 + k_y^2 + k_z^2\right) - \Delta, \quad (2.10d)$$

$$S = -\frac{\hbar^2}{2\mathrm{m}_0}2\sqrt{3}\gamma_3\left(-k_x + ik_y\right)k_z, \quad (2.10e)$$

$$R = -\frac{\hbar^2}{2\mathrm{m}_0}\sqrt{3}\left[\gamma_2\left(k_x^2 - k_y^2\right) - 2\gamma_3 ik_x k_y\right], \quad (2.10f)$$

$$D = -\frac{\hbar^2}{2\mathrm{m}_0}\sqrt{2}\gamma_2\left(k_x^2 + k_y^2 - 2k_z^2\right), \quad (2.10g)$$

$$P_{\pm} = P_o\left(k_x \pm ik_y\right), \quad (2.10h)$$

$$P_z = P_o k_z. \quad (2.10i)$$

m_c is the electron effective mass. Δ accounts for the spin-orbit interaction. γ_1, γ_2, and γ_3 are the modified effective mass parameters and related to the Luttinger parameters ($\gamma_1^L, \gamma_2^L, \gamma_3^L$) used in 6-band Hamiltonian by [149]:

$$\gamma_1 = \gamma_1^L - \frac{E_p}{3E_g}, \gamma_2 = \gamma_2^L - \frac{E_p}{6E_g}, \gamma_3 = \gamma_3^L - \frac{E_p}{6E_g}. \quad (2.11)$$

The mixing of the valence and conduction bands is governed by Kane energy (E_p) and it is related to P_o by:

$$E_p = \frac{2m_0}{\hbar^2}P_0^{\,2}. \quad (2.12)$$

In addition, the Luttinger parameters are approximately related to the heavy-hole and light-hole effective masses [150] by:

$$\gamma_1^L = \frac{1}{2}\left(\frac{1}{m_{lh}^{[001]}} + \frac{1}{m_{hh}^{[001]}}\right),$$
$$\gamma_2^L = \frac{1}{4}\left(\frac{1}{m_{lh}^{[001]}} - \frac{1}{m_{hh}^{[001]}}\right), \qquad (2.13)$$
$$\gamma_3^L = \frac{1}{4}\left(\frac{1}{m_{lh}^{[001]}} + \frac{1}{m_{hh}^{[001]}}\right) - \frac{1}{2m_{hh}^{[111]}}.$$

where $m_{hh(lh)}^{[001]}$ and $m_{hh(lh)}^{[111]}$ are heavy-hole (light-hole) effective mass in [001] and [111] directions respectively. Once the 8-band k.p Hamiltonian is established, the energy dispersion in the vicinity of the Γ valley can be obtained by diagonalizing the Hamiltonian matrix.

2.3.2 Discussions and Results of Numerical Fitting

Since the band gap of $Ge_{1-x}Sn_x$ alloy at Γ valley reduces with increasing Sn composition, the coupling of conduction band with valence band needs to be included for accurate calculations of band structures. Thus, 8-band k.p Hamiltonian was chosen over 6-band k.p Hamiltonian in order to account for the coupling between conduction and valence bands. The Luttinger-like parameters, γ_1, γ_2, and γ_3, are treated as adjustable parameters. Vegard's law was used to approximate other required parameters, such as Kane energy and lattice constant for each Sn composition of $Ge_{1-x}Sn_x$. Since the energy dispersion in the small vicinity of the Γ valley determines the transport behavior of semiconductors, accurate energy dispersion at the band edge is crucial. Hence, the fitting of band structure by k.p method to the ones by EPM is aimed at reproducing effective masses obtained from band structures by EPM.

For the fitting process, the initial guesses of the fitting parameters were calculated by eq. 2.13 based on the electron and hole effective masses at Γ valley obtained by EPM. For each fitting iteration, the effective masses of HH, LH, split-off (SO), and conduction bands (CB) were extracted from the band structures calculated by k.p method. These extracted effective masses were then compared with those of EPM. In the fitting process, the fitting parameters were iteratively adjusted in order to minimize the difference between effective masses obtained by k.p method and EPM.

The fitted Luttinger parameters of 8-band k.p method for each Sn composition of $Ge_{1-x}Sn_x$ are summarized in Table 2.5. The comparison of the effective masses of HH, LH, SO, and CB at different Sn composition obtained by k.p method and EPM is shown in Table 2.6 and Table 2.7. In Fig. 2.10, the band structures of $Ge_{1-x}Sn_x$ alloy by k.p method is compared to those of EPM for x = 0.05, 0.11, and 0.20. The band structures obtained by k.p method (dashed line) were fitted reasonably well to that by EPM which is plotted with open circles.

For Sn composition x from 0.05 to 0.20, the average difference between HH, LH, and CB effective masses obtained by k.p and by EPM is within 0.087%, indicating that a very good fitting was achieved. The average discrepancy for SO effective mass calculated by k.p method and by EPM is about 19%. Since the transport of semiconductors is essentially determined by HH, LH, and CB effective masses, the effect of SO effective mass is generally negligible. So, an average difference of 18% difference in SO effective mass will not affect the transport behavior of $Ge_{1-x}Sn_x$ alloys. Overall, from the results of Table 2.6, 2.7, and Fig. 2.10, the 8-band k.p method successfully reproduces the energy dispersions calculated by EPM at the vicinity of Γ valley.

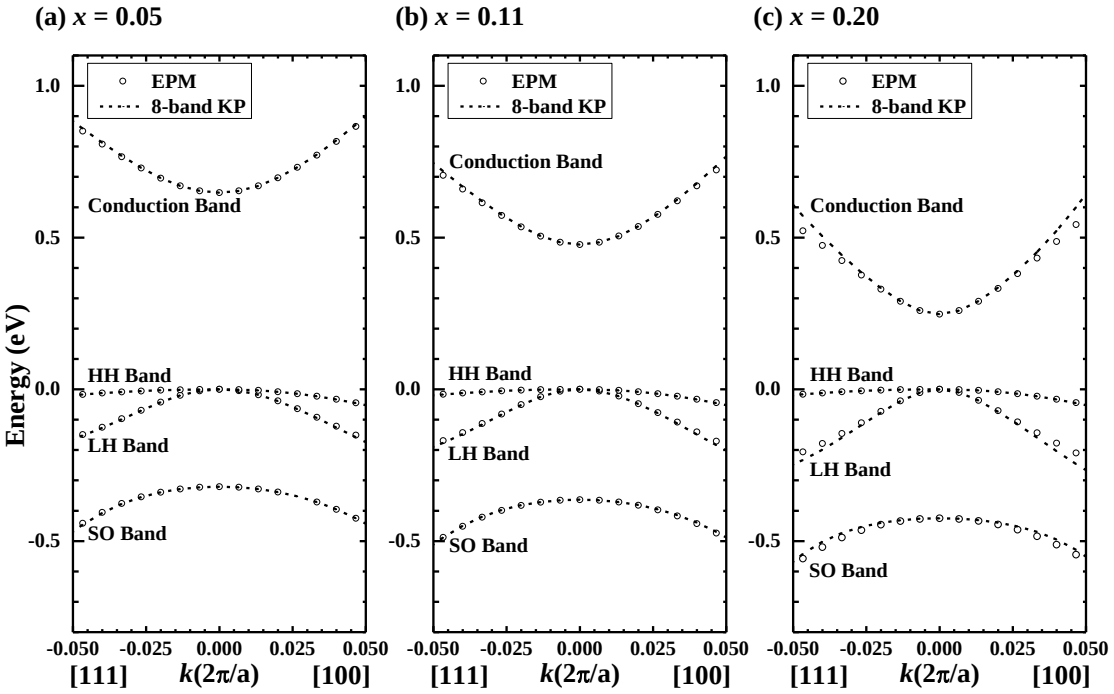

Fig. 2.10. The fitted band structures of $Ge_{1-x}Sn_x$ for (a) x = 0.05, (b) x = 0.11, and (c) x = 0.20 at Γ valley using 8-band k.p Hamiltonian with the spin-orbit interaction taken into account. The results of EPM calculation are plotted with open circles, and results from the k.p method are plotted using dashed lines.

Table 2.5. The fitted Luttinger-like parameters, including Kane energy (E_p), band gap energy at the Γ valley (E_g^Γ), and spin-orbit splitting Δ for $0.05 \le x \le 0.20$.

x	γ_1^L	γ_2^L	γ_3^L	E_p	E_g^Γ	Δ
0.05	13.6487	4.5823	5.9854	26.1850	0.6478	0.3209
0.08	15.2093	5.3417	6.7572	26.1160	0.5605	0.3423
0.11	17.2307	6.3319	7.7708	26.0470	0.4771	0.3635
0.14	19.9506	7.6821	9.1278	25.9780	0.3966	0.3845
0.17	23.8490	9.5988	11.0770	25.9090	0.3182	0.4048
0.20	29.5552	12.4408	13.9287	25.8400	0.2475	0.4249

Table 2.6. The effective masses of the LH and HH bands of $Ge_{1-x}Sn_x$ (in unit of m_0) obtained using a simple parabolic line fit using 8-band k.p method and EPM for $0.05 \leq x \leq 0.20$.

x	M_{LH} (k.p, EPM)		M_{HH} (k.p, EPM)	
	[100]	[111]	[100]	[111]
0.05	0.0441, 0.0441	0.0393, 0.0393	0.223, 0.223	0.596, 0.596
0.08	0.0389, 0.0389	0.0351, 0.0351	0.221, 0.221	0.590, 0.590
0.11	0.0338, 0.0338	0.0308, 0.0308	0.219, 0.219	0.592, 0.592
0.14	0.0287, 0.0287	0.0265, 0.0265	0.218, 0.218	0.590, 0.590
0.17	0.0235, 0.0235	0.0221, 0.0221	0.215, 0.215	0.590, 0.590
0.20	0.0188, 0.0188	0.0179, 0.0179	0.214, 0.214	0.589, 0.589

Table 2.7. The effective masses of the conduction and split-orbit bands of $Ge_{1-x}Sn_x$ (in unit of m_0) obtained using a simple parabolic line fit using 8-band k.p method and EPM for $0.05 \leq x \leq 0.20$.

x	M_e (k.p, EPM)		M_{SO} (k.p, EPM)	
	[100]	[111]	[100]	[111]
0.05	0.0355, 0.0355	0.0356, 0.0355	0.109, 0.109	0.108, 0.108
0.08	0.0316, 0.0316	0.0317, 0.0317	0.107, 0.104	0.107, 0.104
0.11	0.0278, 0.0278	0.0278, 0.0279	0.107, 0.100	0.106, 0.100
0.14	0.0240, 0.0240	0.0240, 0.0240	0.108, 0.096	0.108, 0.0958
0.17	0.0201, 0.0201	0.0202, 0.0201	0.114, 0.0915	0.114, 0.0913
0.20	0.0164, 0.0164	0.0165, 0.0164	0.132, 0.0875	0.131, 0.0874

2.4 Device Performance of GeSn based Transistor

2.4.1 Methodology and Device Model

The ON-current performance of double-gate ultra-thin body (DG-UTB) n-channel metal-oxide-semiconductor field-effect transistor (n-MOSFET) employing unstrained GeSn was assessed. GeSn n-MOSFET with the transport direction along [100] on (100) plane orientation was considered in this study. The longitudinal (m_x), transverse (m_y), and confinement (m_z) effective masses for the 2D GeSn material system were obtained from the projection of bulk effective mass of GeSn at L and Γ valley calculated from the previous section. The approach used is given by [151]. The values of m_x, m_y, and m_z for L and Γ valley are summarized in Table 2.8.

Using the effective masses listed in Table 2.8, the ballistic I_{ON} of GeSn DG-UTB n-MOSFET was calculated using the semi-classical ballistic transport based on top-of-the-barrier (TOB) model coupled with a capacitive model [152]-[154]. Fig. 2.11(a) shows that the carriers fill in the positive velocity states (+k) and the negative velocity states (-k) with their distributions determined by the source ($E_{f,s}$) and the drain ($E_{f,d}$) Fermi levels, respectively. Since the MOSFET is a 3-terminal device, the coupling of each terminal to the channel region is represented by a capacitive model, as shown in Fig. 2.11(b). The capacitive model consists of gate capacitance (C_G), drain capacitance (C_D), and source capacitance (C_S).

In order to assess the upper I_{ON} performance limit of MOSFETs, C_G is assumed to be much larger than C_S and C_D such that the electrostatic of the channel regime is almost perfectly controlled by the gate terminal. This assumption leads to a subthreshold swing close to the ideal 60 mV/decade at room temperature in our ballistic transport calculations. Subsequently, the calculated carrier density was coupled to the capacitive model to solve for the potential at the top of the barrier self-

consistently. Once self-consistency was achieved, the net ballistic current was evaluated from the difference between the positive and negative fluxes injected from the source and the drain. Note that the direct source-to-drain tunneling was not considered in the I_{ON} calculation which may become significant in highly scaled devices.

The values of the equivalent oxide thickness (EOT), power supply voltage (V_{DD}), and OFF-state current (I_{OFF}) used are 0.45 nm, 0.66 V, and 0.1 μA/μm, respectively, as projected by the 2013 edition of the ITRS [89] for the production year of 2026.

Table 2.8. The longitudinal (m_x), transverse (m_y), confinement (m_z) effective masses, subband degeneracy (g_v), and energy separation (ΔE) between L and Γ valley (ΔE) for 2D GeSn material system for $0 \leq x \leq 0.20$. The units for the effective mass and ΔE are m_0 (free electron mass) and eV, respectively.

(Sn %)	Valley	m_x	m_y	m_z	g_v	$\Delta E(E_g^L - E_g^\Gamma)$
(0%)	Γ	0.0420	0.0420	0.0420	1	0
Ge	L	0.1695	0.5929	0.1339	4	-0.1438
(5%)	Γ	0.0360	0.0360	0.0360	1	0
$Ge_{0.95}Sn_{0.05}$	L	0.1659	0.5900	0.1310	4	-0.0751
(8%)	Γ	0.0324	0.0324	0.0324	1	0
$Ge_{0.92}Sn_{0.08}$	L	0.1637	0.5903	0.1292	4	-0.0365
(11%)	Γ	0.0288	0.0288	0.0288	1	0
$Ge_{0.89}Sn_{0.11}$	L	0.1615	0.5874	0.1273	4	-0.0002
(14%)	Γ	0.0250	0.0250	0.0250	1	0
$Ge_{0.86}Sn_{0.14}$	L	0.1594	0.5849	0.1256	4	0.0364
(17%)	Γ	0.0211	0.0211	0.0211	1	0
$Ge_{0.83}Sn_{0.17}$	L	0.1575	0.5868	0.1240	4	0.0717
(20%)	Γ	0.0174	0.0174	0.0174	1	0
$Ge_{0.80}Sn_{0.20}$	L	0.1556	0.5842	0.1225	4	0.103

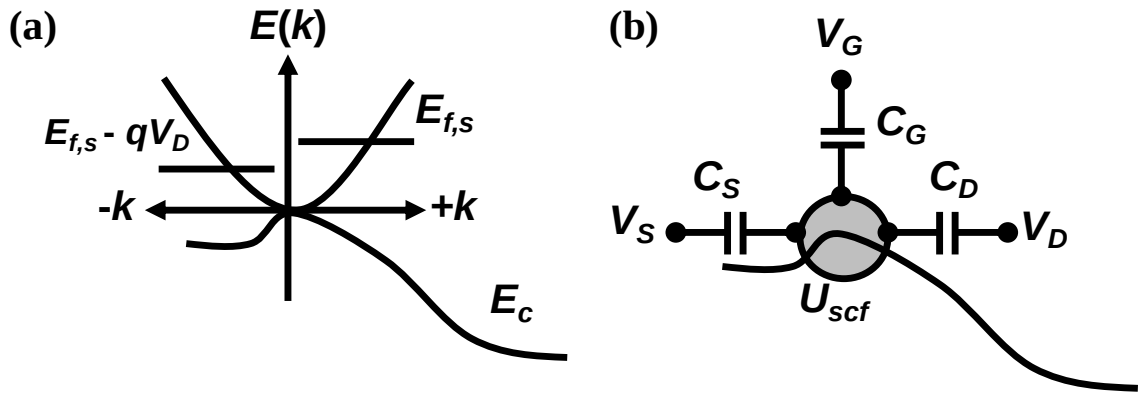

Fig. 2.11. (a) Illustration of TOB model. The summation of the respective carriers occupying *+k* and *–k* states from the source and the drain constitute the net charge at the top of the barrier. The ballistic current is the net flow of the positive and negative going fluxes injected from the source and the drain, respectively. (b) Capacitance model demonstrating the electrostatic coupling of the source (C_S), gate (C_G), and drain (C_D) terminals to the potential at top of the barrier (U_{scf}). A perfect gate control over the channel is assumed ($C_G >> C_S, C_D$).

2.4.2 Results and Discussions of I_{ON} Performance

The I_{ON} performance was examined for unstrained GeSn n-MOSFET with Sn compositions varying from 0 to 20%. This is to investigate how the Sn compositions affect the I_{ON} performance of GeSn n-MOSFET as GeSn becomes a direct bandgap semiconductor with a very small effective mass at the Γ valley. In this work, I_{ON} is defined to be the I_{DS} at $V_{DS} = V_{DD}$ and $V_{GS} = V_{DD} + V_{OFF}$. V_{OFF} is defined to be the V_{GS} at which $I_{DS} = I_{OFF}$ and $V_{DS} = V_{DD}$.

Fig. 2.12(a) shows the I_{ON} versus Sn composition of GeSn n-MOSFET with a body thickness (T_{body}) of 5 nm. The I_{ON} value increases with progressively higher Sn composition. The improvement in the I_{ON} with Sn composition is rather marginal with ~0.042% increase in the I_{ON} when Sn composition is increased from 0 to 20%. Fig. 2.12(b) shows the ratio of transport effective mass (m_x) to that of Ge for Γ and L valley at different Sn compositions. The rate of reduction in $m_x$with increasing Sn

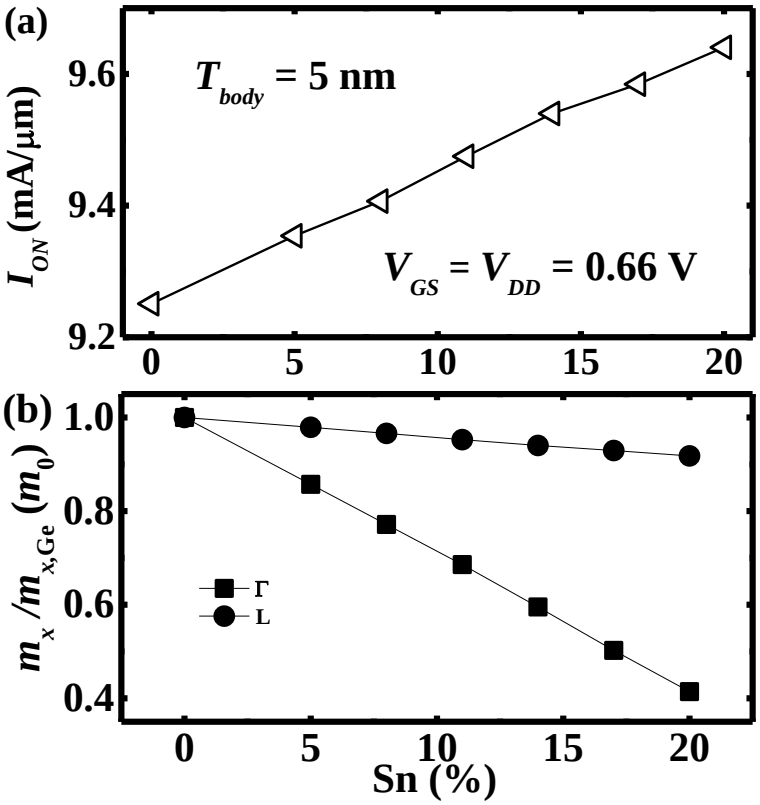

Fig. 2.12. (a) I_{ON} of GeSn n-MOSFET with Sn composition for T_{body} of 5 nm: I_{OFF} used for the I_{ON} extraction is 0.1 μA/μm. An increased trend over all Sn compositions examined is observed in the I_{ON} of GeSn n-MOSFETs with a T_{body} of 5 nm. (b) Ratio of transport effective mass (m_x) to that of Ge for Γ and L valley with Sn composition.

composition is higher for Γ valley than L valley. The m_x of Γ valley for Sn composition of 20% is reduced by ~60% relative to the m_x of Ge. The marginal increase in I_{ON} with Sn composition implies that the high carrier velocity at Γ valley resulting from the decrease of m_x with increasing Sn composition does not benefit the I_{ON} of GeSn n-MOSFET with 5 nm T_{body}.

To understand this I_{ON} trend with the Sn composition in Fig. 2.12(a), E_g^L, E_g^Γ and the energy separation ($\Delta E = E_g^L - E_g^\Gamma$) between L and Γ valley for 5 nm and 50 nm T_{body} are shown in Fig. 2.13. The subband energy of Γ and L valley at each composition was calculated based on the confinement effective mass (m_z) values.

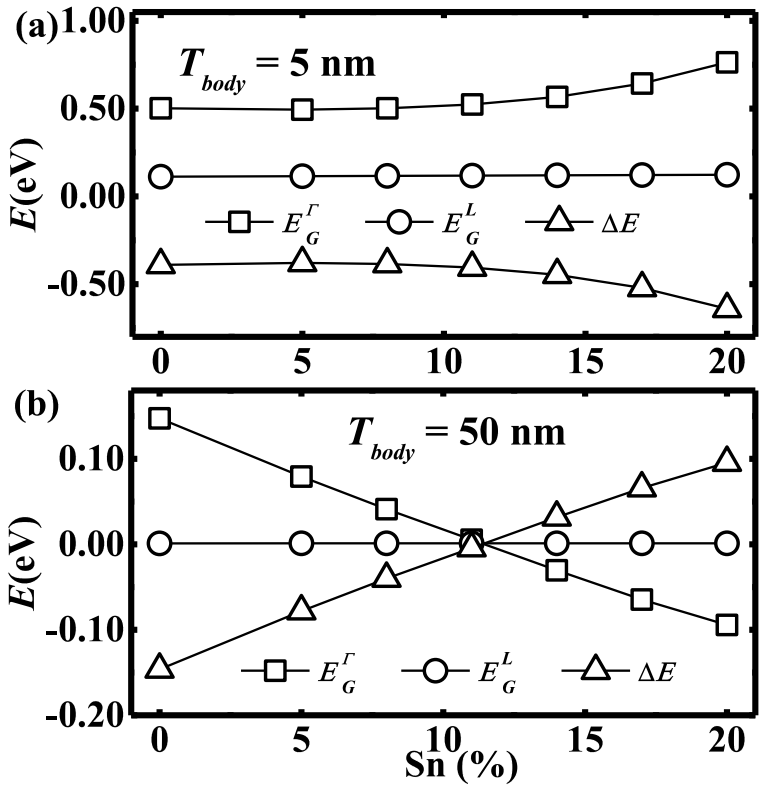

Fig. 2.13. E_g^Γ, E_g^L, and energy separation (ΔE) between L and Γ valley for (a) 5 nm and (b) 50 nm T_{body}. Due to the quantum confinement and relatively smaller m_z of Γ valley, the subband of Γ valley is higher than that of L valley for all Sn compositions for T_{body} of 5 nm. The ΔE of 50 nm T_{body} follows the trend of bulk GeSn.

From Fig. 2.13(a), ΔE of T_{body} = 5 nm is negative for all Sn compositions. The values of ΔE at different Sn compositions are smaller than -0.37 eV and drop to -0.64 eV at the Sn composition of 20%. At a T_{body} of 5 nm, the effect of quantum confinement is pronounced. From Table 2.8, the m_z of L valley is heavier than that of Γ valley for all Sn compositions studied. Due to light m_z at Γ valley, the subband of Γ valley is raised to the higher energy level as compared to the subband of L valley. This results in the subband of L valley being always lower than that of Γ valley for all Sn compositions studied.

Fig. 2.13(b) shows that the ΔE of T_{body} with 50 nm is very similar to that of bulk GeSn, both increasing with increasing Sn composition. The subband energy of Γ valley decreases with increasing Sn composition.

Next, the I_{ON} of GeSn n-MOSFET with 5 nm T_{body} is separated into individual I_{ON} component of Γ and L valley, as plotted in Fig. 2.14(a). In addition, the channel charge (Q_{ON}) and the average carrier velocity (V_{AVG}) of Γ and L valley at the ON-state are plotted in Fig. 2.14(b) and (c), respectively. For GeSn n-MOSFET of 5 nm T_{body}, the overall I_{ON} is entirely determined by the I_{ON} of the L valley, as illustrated in Fig. 2.14(a). As mentioned above, the subband of Γ valley is higher than the one of L valley due to the quantum confinement, leading to the negligible involvement of Γ valley in the transport. This is reflected in the magnitude of the I_{ON} and Q_{ON} of Γ valley being nearly zero. The transverse effective mass (m_y) of L valley is relatively similar for all Sn compositions investigated. This translates to almost similar magnitude of Q_{ON} for all Sn compositions studied, as observed in Fig. 2.14(b). The V_{AVG} of L valley shown in Fig. 2.14(c) increases with Sn compositions due to the reduction of m_x projected from L valley with Sn composition. Since Q_{ON} of L valley is independent of the Sn composition, the V_{AVG} of L valley dictates the I_{ON} trend of GeSn n-MOSFET with 5 nm, as shown in Fig. 2.12(a).

In order to investigate the effect of Γ valley on the ballistic I_{ON}, GeSn n-MOSFET with a larger T_{body} of 50 nm was simulated. As shown in Fig. 2.13(b), the ΔE of bulk GeSn and 50 nm T_{body} shows a similar trend, implying that the position of Γ and L valley of 50 nm T_{body} follows the trend of bulk GeSn. The assumption of constant potential across the whole body may not be practical for a T_{body} of 50 nm. Nonetheless, this assumption was used to understand device physical insights of GeSn n-MOSFET when both Γ and L valley are involved in the transport. Fig. 2.15(a)

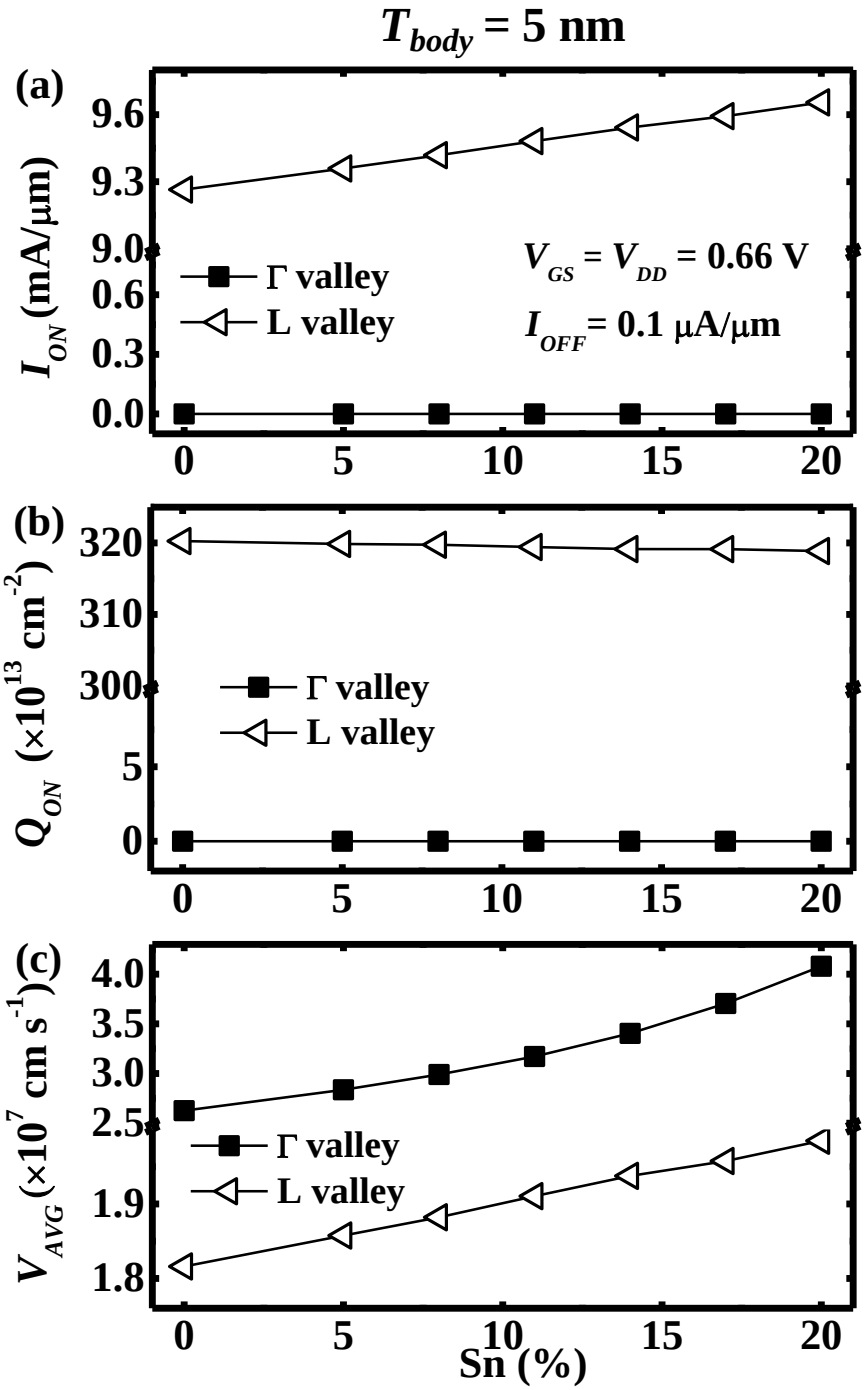

Fig. 2.14. GeSn n-MOSFET with 5 nm T_{body}: (a) The I_{ON}, (b) the total channel charge (Q_{ON}), and (c) the average carrier velocity (V_{AVG}) are separated into individual component of Γ and L valley. All values are extracted at the ON-state. The overall I_{ON} is entirely determined by the L valley. The contribution of Γ valley to the transport is negligible, as reflected in the magnitude of its I_{ON} and Q_{ON} being close to zero for all Sn compositions studied.

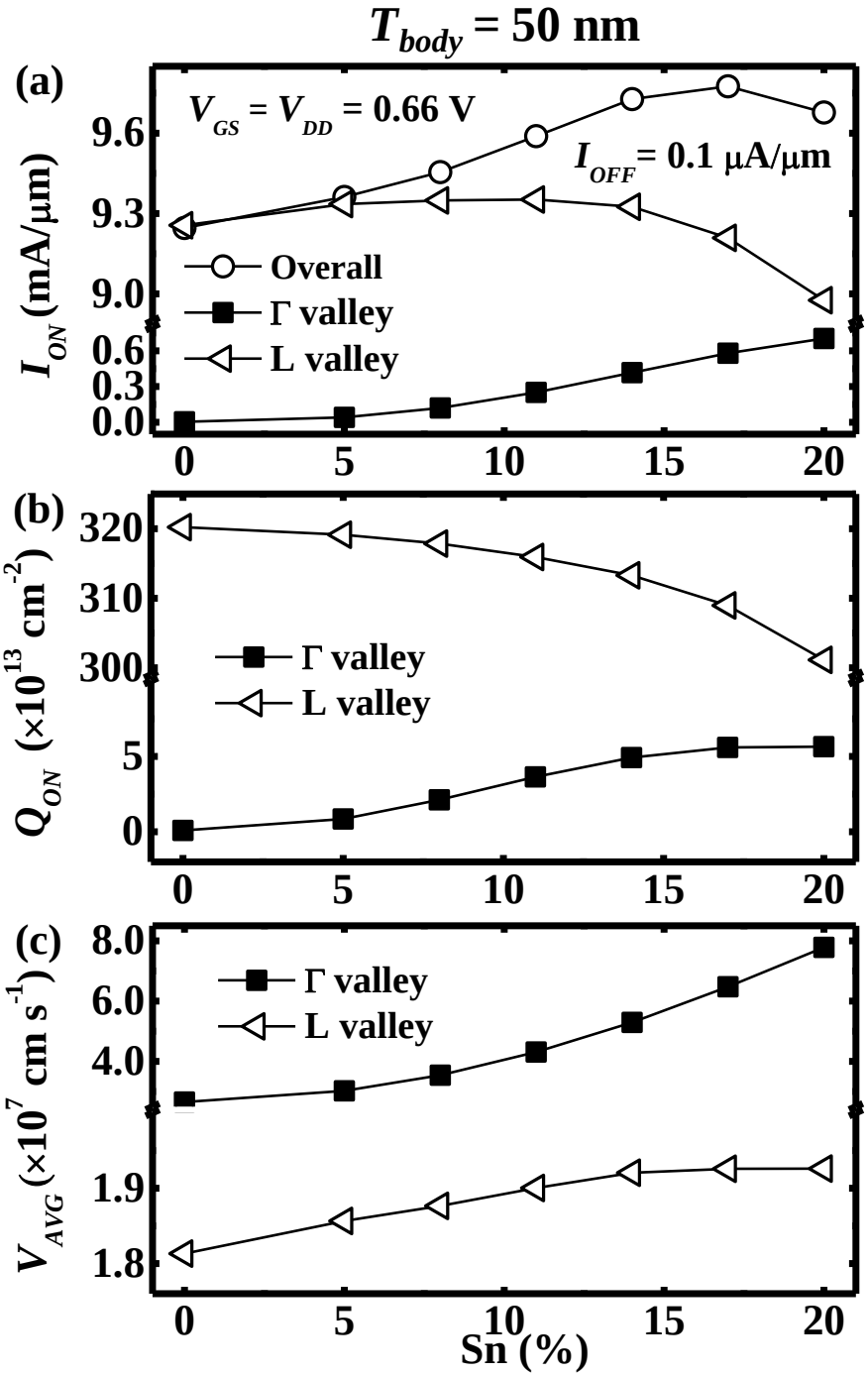

Fig. 2.15. GeSn n-MOSFET with 50 nm T_{body}: (a) The I_{ON}, (b) the total channel charge (Q_{ON}), and (c) the average carrier velocity (V_{AVG}) are separated into individual component of Γ and L valley. All values are extracted at the ON-state. Substantial fraction of the overall I_{ON} is contributed by the L valley. The I_{ON} of L valley drops more drastically for Sn greater than 11%. This is mainly due to the greater reduction in Q_{ON} with Sn composition when Sn is greater than 11% [Fig. 2.14(b)]. Due to smaller transport effective mass (m_x) of Γ valley, the V_{AVG} of Γ valley is higher than that of L valley.

shows that the degree of improvement in I_{ON} with increasing Sn composition is higher than that of GeSn n-MOSFET with 5 nm T_{body}. Unlike the case of 5 nm T_{body} where Γ valley has negligible contribution to the I_{ON}, the overall I_{ON} of GeSn n-MOSFET with 50 nm T_{body} is partially contributed by Γ valley, as shown in Fig. 2.15(a). Fig. 2.15(b) shows that the Q_{ON} of L valley decreases with Sn composition while the Q_{ON} of Γ valley increases with Sn composition. In terms of the average carrier velocity shown in Fig. 2.15(c), the V_{AVG} of the Γ valley is higher than that of L valley. This trend is expected since the transport effective mass (m_x) of Γ valley is smaller than that of L valley.

From the above analysis, it is found that the reduction of the effective mass at Γ valley with increasing Sn composition does not benefit the ballistic I_{ON} of GeSn n-MOSFET with highly scaled T_{body}. Due to small m_z at Γ valley, the subband energy of Γ valley is raised far above the one of L valley under strong quantum confinement.

2.5 Conclusions

The electronic band structures of $Ge_{1-x}Sn_x$ were calculated using the empirical pseudopotential method. By adjusting the form factors of the pseudopotential, the band gap energies obtained from the calculated band structures agree well with reported experimental data. With increasing Sn composition, the extracted $Ge_{1-x}Sn_x$ effective masses decrease for $0 < x < 0.20$ for light-hole valence band, conduction band at Γ valley and conduction band at L valley along transverse direction. The effective masses of heavy hole and conduction band at L valley along longitudinal direction are rather independent of Sn composition. The study of the dependence of effective masses at Γ valley on the plane orientations [(001), (110) and (111)] and in-plane directions reveals that the LH and HH effective masses show

anisotropy for plane orientations of (100) and (110). For electron effective mass, it shows isotropy and similar magnitude along all in-plane directions for all three plane orientations investigated. In addition, the Luttinger-like parameters of 8-band k.p model were derived by fitting the energy dispersion in the vicinity of the Γ valley to that by EPM. These effective masses and derived effective mass parameters of 8-band k.p method may be useful for the optical and electronic device designs employing $Ge_{1-x}Sn_x$ alloys.

From the device performance perspective, GeSn DG-UTB n-MOSFETs with thinner body [5 nm] show marginally improved ON-current with respect to the one of Ge n-MOSFET for all Sn compositions studied. Due to lighter m_z of Γ valley than that of L valley, the subband of Γ valley is raised to higher energy than that of L valley under strong quantum confinement. This leads to the transport performance being almost entirely determined by the L valley for GeSn n-MOSFET. Thus, GeSn n-MOSFET does not reap the benefit of reduction in effective mass of Γ valley with increasing Sn composition. In addition, the transport effective mass (m_x) of L valley decreases with Sn composition, leading to higher carrier velocity with increasing Sn composition. This results in an enhancement in I_{ON} with increasingly larger Sn composition for GeSn n-MOSFET with 5 nm body thickness. For GeSn n-MOSFET with thicker body [50 nm], the degree of enhancement in I_{ON} increases with Sn composition until 17% and drops at the Sn composition of 20%. For Sn composition smaller than 17%, the I_{ON} is enhanced due to the contribution of both L and Γ valley. The decrease in the I_{ON} enhancement at high Sn composition is due to the fact the subband of Γ valley becomes lower than that of L valley after Sn composition of 11%. This reduces the total charge in the channel when Sn is greater than 11% because the DOS of Γ valley is smaller than that of L valley.

Chapter 3

Drive Current of Silicane and Germanane Metal-Oxide-Semiconductor Field-Effect Transistors in the Ballistic Transport Regime: A Simulation Study

3.1 Introduction

Apart from the group IV semiconductors discussed in Chapter 2, lower dimensional materials, such as two-dimensional (2D) monolayer materials, are currently of great interest as alternative channel materials for complementary-metal-oxide-semiconductor (CMOS) devices due to their excellent electrostatic integrity inherent in a two-dimensional system. Among 2D material systems actively researched are the transition metal dichalcogenides (TMDs) [46]-[52].

Lately, the electronic properties of 2D hexagonal lattices of Si and Ge, so called silicene [155]-[166] and germanene [155]-[158], [167]-[168], have been intensively studied. The experimental studies reported the possible growth of silicene [169]-[175] and germanene [176] strips and nanoribbons. As compared to TMDs, 2D materials from group IV may have better integration and process or materials compatibility with the Si-based platform used in today's semiconductor industry. However, silicene and germanene are semi-metallic which requires band gap opening in order for the application in the nanoelectronic devices. Z. Ni *et al.* explored the use

of vertical electric field to open up the band gap in silicene and germanene for field-effect transistor (FET) applications [156].

Another feasible method in engineering the band gap of 2D materials is through the chemical functionalization, such as hydrogenation. Hydrogenated silicene and germanene [Fig. 3.1(a)], so called silicane and germanane, respectively, are semiconductors. Recently, Bianco *et al*. [177] successfully demonstrated hydrogenated germanene experimentally. Germanane has shown some superior properties, such as semiconducting characteristics and lighter effective mass than that of bulk germanium.

Up till now, numerous studies have been dedicated to the understanding of the material properties of silicane and germanane, such as electronic band structure of germanane [166], [178]-[183] and silicane [166], [178]-[186]. However, the device performance of germanane and silicane field-effect transistor has not been thoroughly studied or evaluated.

In this Chapter, we evaluate the upper limit of the drive current performance of germanane and silicane metal-oxide-semiconductor field-effect transistor (MOSFETs) in the ballistic transport regime. This study is crucial for assessing their suitability as CMOS devices. Theoretical studies [164], [178]-[179] show that chair-like configuration is energetically more stable than other configurations, such as boat-like configuration. Hence, silicane and germanane transistors in the chair-like configuration are considered in this study. The ballistic ON-state currents (I_{ON}) of germanane and silicane MOSFETs are compared with those of transistors having 2D-TMDs [Fig. 3.1(b)] as channel materials. Finally, the ballistic drive current of MOSFETs having channel materials made up of silicane, germanane, and 2D-TMDs is assessed based on the high performance (HP) and low operating power (LOP)

technology requirements specified in the International Technology Roadmap for Semiconductors (ITRS) [89] for production years from 2018 to 2026. The ITRS-projected parasitic resistance (R_{SD}) effects are also considered in calculating the ballistic I_{ON}. For all the 2D-material MOSFETs studied, their ballistic I_{ON} is assessed based on the requirements for HP logic application and their power supply voltage (V_{DD}) scalability is examined based on the requirements for LOP technology.

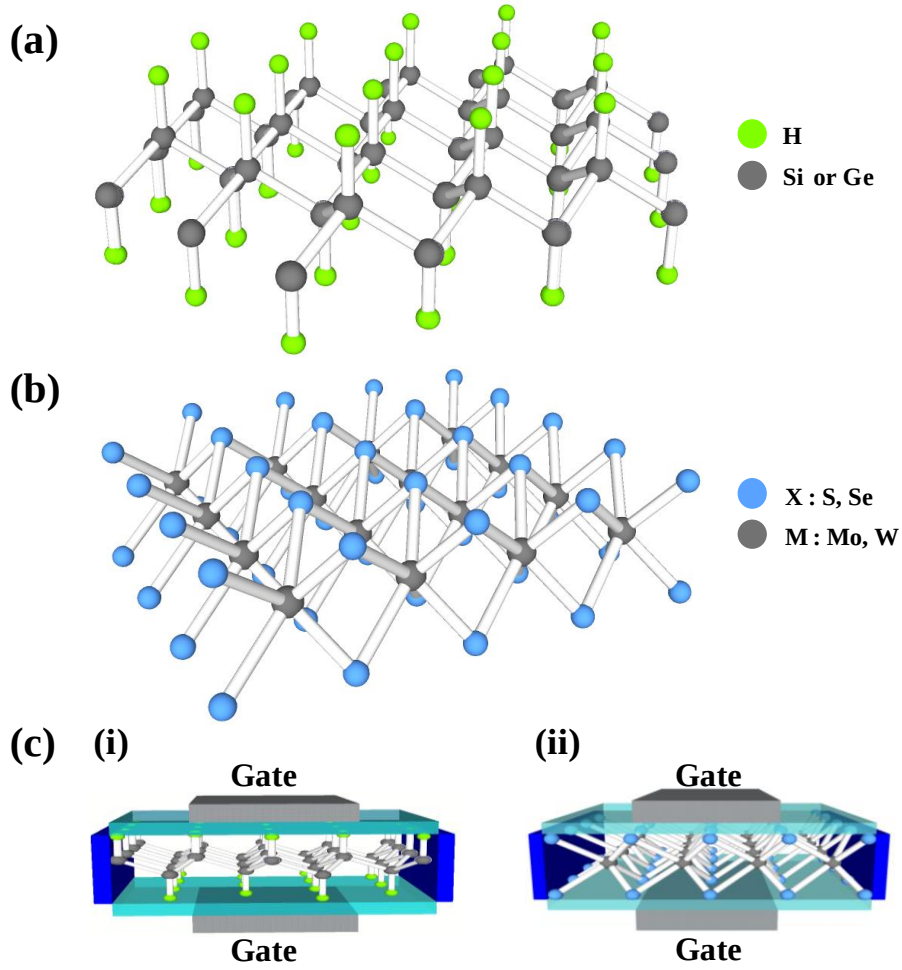

Fig. 3.1. Schematic illustrating the crystal structure of (a) hydrogenated silicene and germanene in the chair-like configuration. The black and green spheres represent silicon / germanium and hydrogen, respectively. (b) 2D-TMD in MX_2 form, where M = Mo, W; X = S, Se. (c) Double-gate MOSFET device structure with (i) silicane or germanane and (ii) 2D-TMD as channel material.

3.2 Approach

3.2.1 Electronic band structure calculations

As shown in Fig. 3.1(a), silicane (or germanane) has a hexagonal unit cell consisting of two Si (or Ge) atoms with hydrogen atom bonds with Si (or Ge) atom in an alternate up and down manner.

To minimize the interaction between the adjacent periodic layers, a vacuum spacing of at least 20 Å was added in the normal direction to the crystal plane. Within the density functional theory in the general gradient approximation (DFT-GGA) with the Perdew-Burke-Ernzerhof (PBE) exchange-correlation function [187], the electronic band structures (*E*-*k*) of silicane and germanane were calculated. The projector-augmented plane wave (PAW) potentials [188] were used. All the calculations were performed by using the Vienna *ab-initio* simulation package (VASP) [189], [190]. For the relaxation calculations, a plane-wave basis set with kinetic energy cutoff of 500 eV was employed. The convergence condition for the total energy and atomic force was set to be 10^{-4} eV and 0.01 eV/Å, respectively. 21×21×1 Monkhorst-Pack grid was used to sample the Brillouin zone [191]. A finer sampling of 51×51×1 *k*-point was used to obtain the *E*-*k* dispersion for the ballistic transport calculation.

3.2.2 Ballistic transport performance calculations

A double-gate MOSFET device structure, as depicted in Fig. 3.1(c) was used for the ballistic I_{ON} *evaluation*. The ballistic I_{ON} of silicane and germanane MOSFETs were evaluated by using a semi-classical ballistic transport model [152]-[154]. The charge at the top of the barrier was solved directly from the energy dispersions (*E*-*k*).

The net charge was obtained by summing up the carriers filling in the positive velocity states (+k) and the negative velocity states (-k) with their distributions determined by the source ($E_{f,s}$) and the drain ($E_{f,d}$) Fermi levels, respectively. For this study, the full electronic band structures within the first Brillouin zone obtained from *ab-initio* calculations were used to calculate the ballistic I_{ON}.

Since the MOSFET is a 3-terminal device, the coupling of each terminal to the channel region is represented by a capacitive model. The capacitive model consists of gate capacitance (C_G), drain capacitance (C_D), and source capacitance (C_S). In order to assess the upper I_{ON} performance limit of MOSFETs, C_G is assumed to be much larger than C_S and C_D such that the electrostatic of the channel regime is almost perfectly controlled by the gate terminal. This assumption leads to a subthreshold swing close to the ideal 60 mV/decade at room temperature in our ballistic transport calculations. Subsequently, the calculated carrier density was coupled to the capacitive model to solve for the potential at the top of the barrier self-consistently. Once self-consistency was achieved, the net ballistic current was evaluated from the difference between the positive and negative fluxes injected from the source and the drain.

Based on the total parasitic resistance specified in the ITRS for HP and LOP technology for years 2018 through 2026, the R_{SD} effects were included in the calculation of the ballistic I_{ON}.

3.3 Results and Discussions

3.3.1 Electronic band structure

The optimized structural parameters and electronic band gap of silicane and germanane presented in Table 3.1 agree well with the previously reported values

[178]-[179]. The *E-k* dispersion of 2D-TMDs (MoS_2, $MoSe_2$, WS_2, and WSe_2) from *ab-initio* calculations was performed previously and all the details were reported in [192].

As depicted in Fig. 3.2(a), silicane exhibits an indirect band gap (E_g) with its conduction band minimum (CBM) and valence band maximum (VBM) located at M and Γ valleys, respectively. The band gap of silicane is calculated to be 2.19 eV. The second lowest conduction point is at Γ valley which is 0.14 eV higher than that of the lowest conduction valley. Our calculation automatically accounted for the contributions of multiple valleys since the full electronic band structures were considered.

Germanane has a direct gap of 0.96 eV as shown in Fig. 3.2(b). The second lowest conduction point is located at M valley which is 0.97 eV higher than that of the lowest conduction point. This energy separation of 0.97 eV is consistent with the value reported in [177]. Although the DFT-GGA approach adopted in our *E-k* dispersion calculation may underestimate the band gap energies, the band gap underestimation issue will not affect the results of the ballistic performance of the MOSFET since the operating mechanism of MOSFET is based on the injection of carriers over the barrier and not the band-to-band tunneling.

Table 3.1. Optimized structural and electronic parameters of silicane and germanane. a, Δz, and d represent the lattice constant, buckling distance, and bond length, respectively. X = Silicon or Germanium and H = Hydrogen.

	Silicane	Germanane
a (Å)	3.889	4.089
Δz (Å)	0.7192	0.731
d (X-X) (Å)	2.358	2.471
d (X-H) (Å)	1.501	1.563

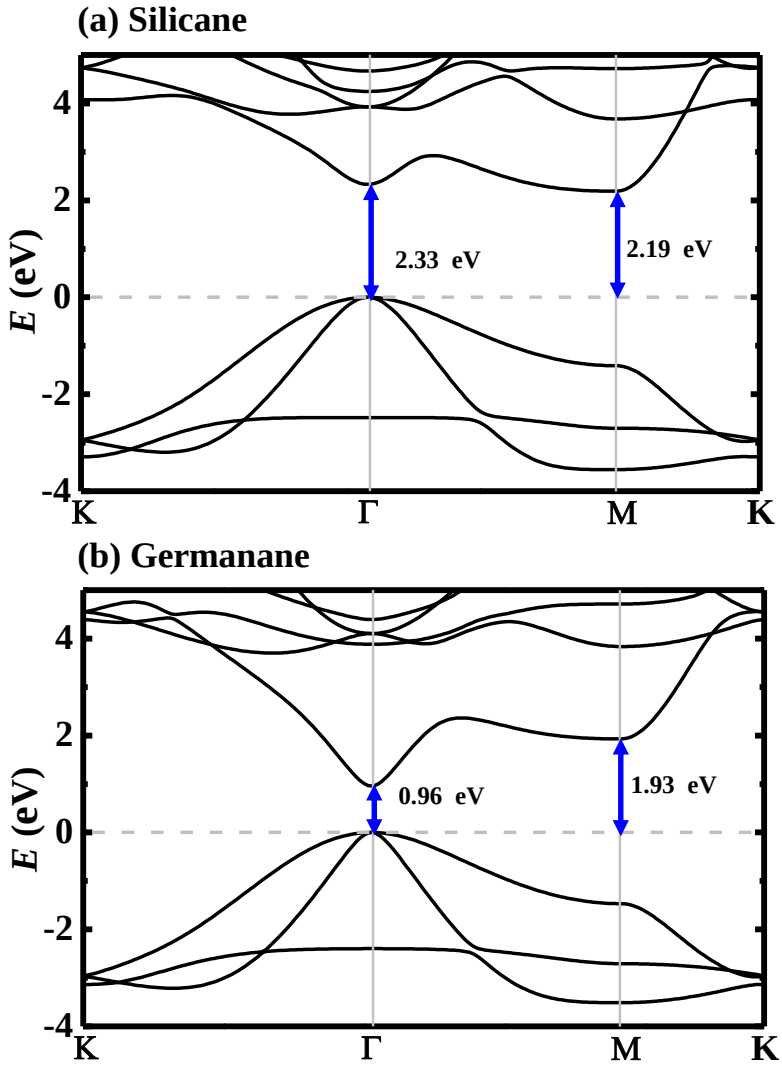

Fig. 3.2. Electronic band structures of (a) Silicane and (b) Germanane.

The effective masses at CBM and VBM along high symmetry directions were extracted using a parabolic line fit and their values are summarized in Table 3.2. The extracted electron and hole effective masses of germanane agree well with reported data from [177]. The CBM effective mass of germanane is smaller than that of silicane. The significantly smaller electron effective mass of germanane indicates a higher electron velocity in germanane than that in silicane.

The equi-energy contour of the lowest conduction band depicted in Fig. 3.3(a) shows that the conduction band of silicane has lower energy along the Γ→M line with its global minimum point at M valley, signifying higher carrier occupancy along that line. Another observation from Fig. 3.3(a) is that the variation of the energy along the M→Γ direction is more gradual than that along the M→K direction, implying higher electron effective mass along the M→Γ direction compared to that along the M→K direction. As shown in Fig. 3.3(b), the highest energy of the silicane valence band is at Γ valley. The energy variation from Γ valley to other directions is rather isotropic. This is reflected in the extracted hole effective mass along the Γ→M and the Γ→K directions having almost similar values.

Fig. 3.3(c) and 3.3(d) show that the lowest conduction band and the highest valence band of germanane are at the Γ valley. An isotropic trend is observed in the energy variation around Γ valley for the conduction band as shown in Fig. 3.3(c). It is noted that the valence band equi-energy contours of both silicane and germanane are highly similar in their topology as evident by their almost identical trend in the hole effective masses.

Table 3.2. The extracted effective masses of conduction band (m_n) and valence band (m_p). $m_{p,hh}$ and $m_{p,lh}$ represent the heavy and light hole effective mass, respectively. They are in the unit of free electron mass, m_0.

Silicane		Germanane	
m_n (Γ→K)	0.193	m_n (Γ→K)	0.0962
m_n (Γ→M)	0.182	m_n (Γ→M)	0.0873
m_n (M→K)	0.123	m_n (M→K)	0.116
m_n (M→ Γ)	3.23	m_n (M→ Γ)	3.34
$m_{p,hh}$ (Γ→K)	0.573	$m_{p,hh}$ (Γ→K)	0.516
$m_{p,hh}$ (Γ→M)	0.603	$m_{p,hh}$ (Γ→M)	0.54
$m_{p,lh}$ (Γ→K)	0.151	$m_{p,lh}$ (Γ→K)	0.097
$m_{p,lh}$ (Γ→M)	0.142	$m_{p,lh}$ (Γ→M)	0.0873

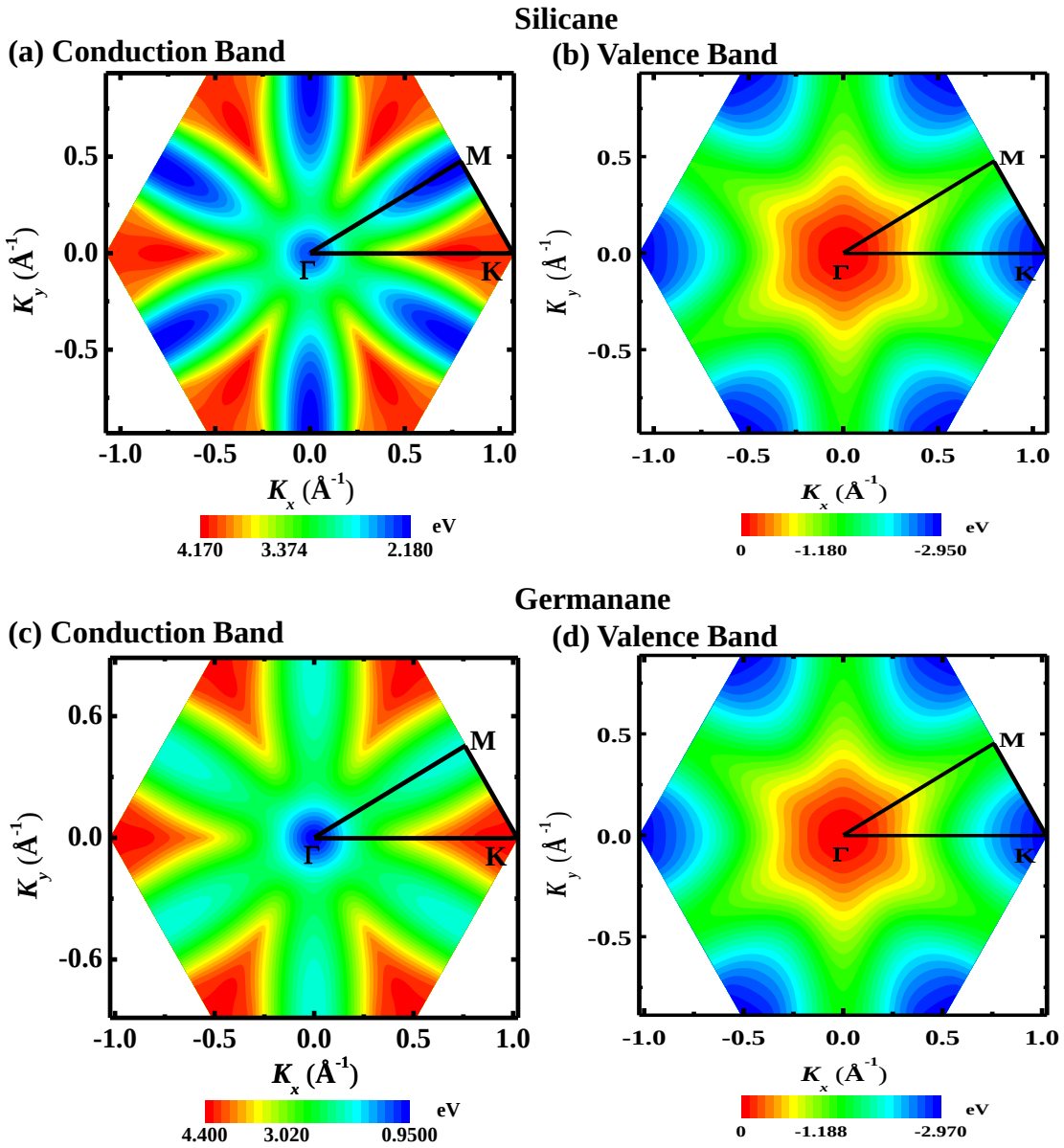

Fig. 3.3. Equi-energy contours (in momentum space): (a) CBM and (b) VBM of silicane and (c) CBM and (d) VBM of Germanane.

3.3.2 Electrical Performance

A V_{DD} of 0.6 V and an EOT of 0.47 nm were used throughout the ballistic transport calculations. In order to compare the I_{ON} of transistors made of different 2D materials, the OFF-state current (I_{OFF}) is fixed at 5 nA/μm, corresponding to the subthreshold source/drain leakage current ($I_{SD,leak}$) of LOP technology. The $E_{f,s}$ was

adjusted such that the current level is equal to the I_{OFF} value at gate voltage (V_{GS}) and drain voltage (V_{DS}) biased at 0 V and V_{DD}, respectively. Since the semi-classical ballistic transport model used in our calculations does not capture the subthreshold leakage due to band-to-band tunneling (BTBT), the focus of this work is to examine the effects of the band structures alone on the ballisticI_{ON}. It should be noted that the BTBT leakage currents may define the I_{OFF} limit. A more comprehensive simulation will be required to assess the performance of realistic devices. However, I_{OFF} caused by BTBT can be disregarded in our study due to the relatively large band gaps of 2D materials studied and reasonably small bias condition used. Hence, the model used here can provide physical insights of the upper I_{ON} limit and ultimate device performance limit of a transistor.

It has been reported that monolayer is a critical requirement for 2D-TMD MOSFETs to retain good electrostatic control of the channel potential by the gate electrode for achieving high I_{ON} [193]. I_{ON} and subthreshold swing (S) of TMDs MOSFET are degraded when the number of layers of TMDs increases due the loss of gate control from increased body thickness. Hence, the ballistic drive currents of monolayer 2D-TMDs MOSFETs were calculated for the comparative study of the transistor performance across different 2D channel materials. Since the ballistic I_{ON} calculated at different directions does not differ much from each other, only the results for the Γ→K direction were discussed.

3.3.2 (I): Ballistic Transport Performance of n-MOSFETs

Fig. 3.4(a) illustrates the transfer characteristics of n-channel MOSFETs (n-MOSFET). Among all the 2D materials studied, the silicane n-MOSFET delivers the highest I_{ON} of around 4700 μA/μm at V_{DS} = V_{GS} = 0.6 V. $MoSe_2$ n-MOSFET has the

lowest I_{ON}. The I_{ON} of the rest of the n-MOSFETs based on 2D materials is in the range from 3100 to 4100 μA/μm.

As depicted in Fig. 3.4(b), the average electron density of germanane n-MOSFET is the lowest. The silicane n-MOSFET has almost the same average electron density as the 2D-TMDs n-MOSFETs. Their average electron densities range from 1.7×10^{13} cm^{-2} to 2.0×10^{13} cm^{-2} at the ON-State. Since the first two lowest conduction valleys of silicane are located at M and Γ valleys, electrons can populate the region along the direction from M to Γ valley. This is confirmed from the electron distribution of silicane n-MOSFET in the first Brillouin zone shown in inset (i) of Fig 3.4(b) where the peak of electron density is observed at M and Γ valleys. It is also observed that the distribution of electron at M valley is anisotropic with the peak of the electron density extending more substantially toward Γ direction than that to K direction from M valley. The anisotropy of electron distribution at M valley is reflected in the electron effective mass extracted at M valley where the electron effective mass extracted from M→Γ (3.23 m_0) is noticeably larger than that of from M→K (0.123 m_0).

The inset (ii) of Fig. 3.4(b) shows that the electrons of mono-layer WS_2 are mostly found at the K valley which is the lowest conduction valley and at the second lowest conduction valley located at almost the midpoint along the K to Γ line. The electron distribution at the first two lowest conduction valleys of WS_2 is fairly isotropic. In contrast to silicane and WS_2, the lowest conduction point of germanane is at Γ valley and the energy separation of the first two lowest conduction points is rather large (0.97 eV). Thus, only the lowest conduction valley plays a major role in the carrier transport. This is evident in the electron distribution of germanane where

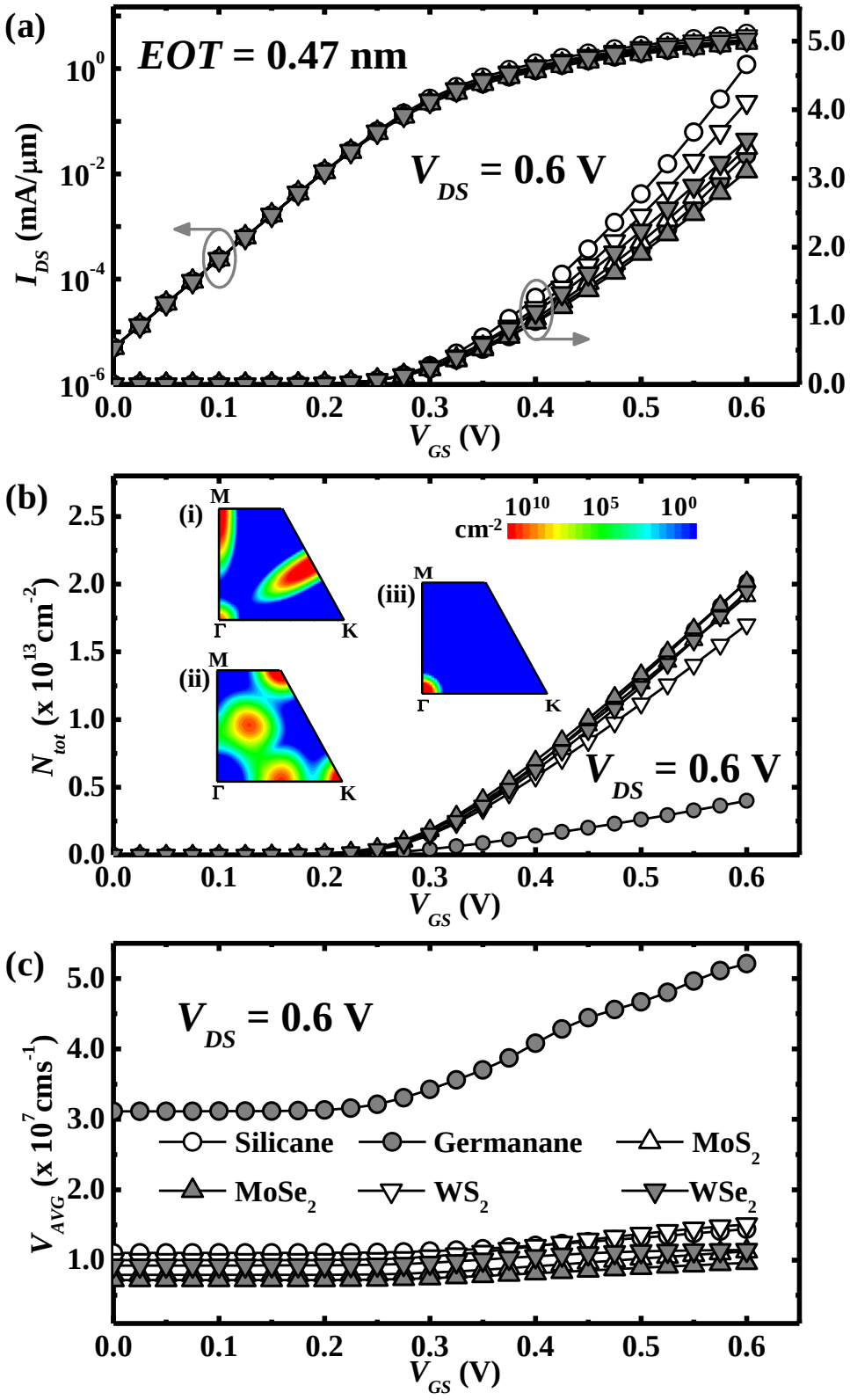

Fig. 3.4. n-MOSFET: (a) Ballistic $I_{DS} - V_{GS}$ for different 2D materials at V_{DD} = 0.6 V. (b) Average electron density. Insets showing the distribution of electron density in the positive quadrant of the first Brillouin zone ($k_x - k_y$ plane) at ON-state: (i) Silicane, (ii) WS_2, (iii) Germanane. (c) Average electron velocity.

the peak of the electron density is only concentrated at Γ valley region as elucidated in the inset (iii) of Fig. 3.4(b). Germanane suffers from the issue of lower electron DOS which is attributed to its smaller electron effective mass at the lowest conduction point.

The average electron velocity for different V_{GS} at V_{DS} of 0.6 V was obtained by dividing the drive current by the total charge density as shown in Fig. 3.4(c). At the ON-state, the average electron velocity of germanane is the highest due to its smallest effective mass among all materials studied. However, the higher average electron velocity of germanane does not sufficiently compensate the drawback in the charge density. $MoSe_2$ n-MOSFET has the lowest average velocity with its velocity magnitude nearly 82% smaller than that of germanane n-MOSFET. Even though $MoSe_2$ n-MOSFET has the highest electron density, the relatively small electron velocity causes the overall I_{ON} to be the smallest among the 2D-material n-MOSFETs studied. The average electron velocities of silicane, WS_2, WSe_2, and MoS_2 n-MOSFETs are almost similar which is within the range of (1.1-1.5) × 10^7 cm s^{-1}. On the other hand, silicane n-MOSFET with reasonable charge density and carrier velocity gives rise to the highest I_{ON}.

Table 3.3 summarizes the mean electron velocity, density, gate capacitance (C_G), and quantum capacitance (C_Q) of n-MOSFETs at the ON-state. C_G was obtained from the derivative of total charge (Q) in the channel with respect to the V_{GS} ($C_G = \partial Q/\partial V_{GS}$). C_Q was calculated from the analytical capacitance model ($1/C_G = 1/C_{OX} + 1/C_Q$), where C_{OX} is the oxide capacitance computed from the EOT used (oxide dielectric constant (ε_{OX}) = 3.9). At the ON-state, C_G values of all n-MOSFETs, except for germanane n-MOSFET, are greater than 9 μF/cm^2. Unlike germanane n-MOSFET whose C_G and C_Q values are comparable, C_Q values of other n-MOSFETs are at least

Table 3.3. n-MOSFET: The average electron velocity (V_{inj}), electron density (Q_n), gate capacitance (C_G), and quantum capacitance (C_Q). All values were extracted at the ON-state (V_{GS} = V_{DS} = 0.6 V, EOT = 0.47 nm).

2D materials	V_{inj}	Q_n	C_G	C_Q	C_G/C_{OX}
Silicane	1.441	2.020	0.114	0.505	0.776
Germanane	5.214	0.401	0.024	0.028	0.163
MoS_2	1.126	1.915	0.105	0.359	0.714
$MoSe_2$	0.960	2.022	0.112	0.465	0.762
WS_2	1.508	1.705	0.096	0.278	0.653
WSe_2	1.144	1.946	0.116	0.549	0.789

Unit: V_{inj}: $\times 10^7$ cm s^{-1}; Q_n: $\times 10^{13}$ cm^{-2}; C_G, C_Q: $\times 10^{-4}$ F/cm^2

2.9 times larger than those of their C_G. The ratio of C_G to C_{OX} in Table 3.3 shows that germanane n-MOSFET has the smallest ratio of 0.16. This implies that germanane n-MOSFET operates at quantum capacitance (C_Q) regime due to its smaller DOS.

3.3.2 (II): Ballistic Transport Performance of p-channel MOSFETs

As illustrated in Fig. 3.5(a), I_{ON} values of both germanane and silicane p-channel MOSFETs (p-MOSFETs) outperform those of 2D-TMDs p-MOSFETs. The I_{ON} of 2D-TMDs p-MOSFETs studied is in the range from 2100 µA/µm to 3500 µA/µm with MoS_2 p-MOSFET having the lowest I_{ON}. Germanane and silicane p-MOSFETs have about the same I_{ON} due to the high similarity of their valence band topology as illustrated in Fig. 3.3(b) and Fig. 3.3(d).

Fig. 3.5(b) illustrates that the variation of the average hole density of different 2D-material p-MOSFETs is comparatively small. When V_{GS} and V_{DS} are biased at -0.6

V, the hole density of MoS_2 is the highest (~2.3×10^{13} cm^{-2}). Germanane p-MOSFET has the lowest hole density which is about 31% smaller than that of MoS_2 p-MOSFET. As illustrated in inset (i) of Fig. 3.5(b), the hole density of germanane p-MOSFET is mainly found at Γ valley. For WSe_2 p-MOSFET, the hole density is peaked at K valley and part of the holes are distributed at Γ valley as shown in inset (ii) of Fig. 3.5(b). It is also noted that the hole distribution around Γ and K valley is rather isotropic.

The average hole velocity for different V_{GS} at V_{DS} of -0.6 V is plotted in Fig. 3.5(c). The average hole velocities of germanane and silicane p-MOSFETs are very close to each other [~$(1.5\text{-}1.6)\times10^7$ cm s^{-1}]. The higher average hole velocities in germanane and silicane p-MOSFETs make their I_{ON} higher than those of 2D-TMDs p-MOSFETs. The range of average hole velocity for 2D-TMDs p-MOSFETs is from 5.6×10^6 cm s^{-1} to 1.1×10^7 cm s^{-1} with MoS_2 p-MOSFET having the lowest average hole velocity.

Table 3.4 illustrates that the C_Q values of all p-MOSFETs are larger than those of C_G by at least 2.4 times. The ratios of C_G to C_{OX} of all p-MOSFETs are larger than 0.58, signifying that they operate at the classical regime. Their C_G values are mainly determined by C_{OX}.

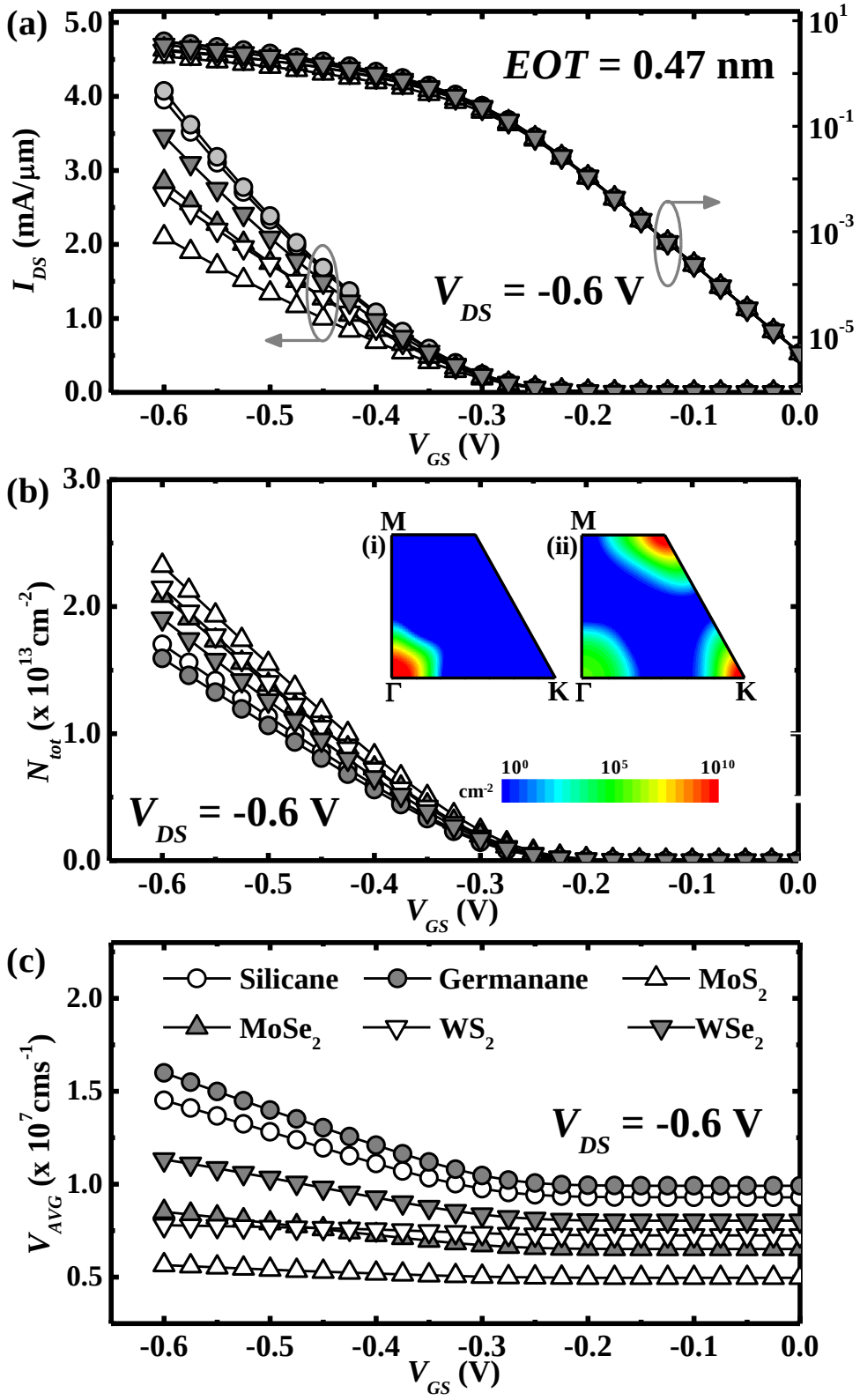

Fig. 3.5. p-MOSFET: (a) Ballistic $I_{DS} - V_{GS}$ for different 2D materials at V_{DD} = -0.6 V. (b) Average hole density. Insets showing the distribution of hole density in the positive quadrant of the first Brillouin zone (BZ) ($k_x - k_y$ plane) at ON-state (i) Germanane and (ii) WSe_2. (c) Average hole velocity.

Table 3.4. p-MOSFET: The average hole velocity (V_{inj}), hole density (Q_p), gate capacitance (C_G), and quantum capacitance (C_Q). All values were extracted at the ON-state (V_{GS} = V_{DS} = -0.6 V, EOT = 0.47 nm).

2D materials	V_{inj}	Q_p	C_G	C_Q	C_G/C_{OX}
Silicane	1.451	1.705	0.092	0.242	0.626
Germanane	1.599	1.594	0.085	0.203	0.578
MoS_2	0.564	2.322	0.125	0.836	0.850
$MoSe_2$	0.851	2.088	0.114	0.503	0.776
WS_2	0.779	2.150	0.121	0.686	0.823
WSe_2	1.134	1.908	0.105	0.362	0.714

Unit: V_{inj}: $\times 10^7$ cm s^{-1}; Q_p: $\times 10^{13}$ cm^{-2}; C_G, C_Q: $\times 10^{-4}$ F/cm^2

3.3.3: I_{ON} Assessment Based on ITRS Requirements for High Performance Technology

Four parameters, V_{DD}, EOT, R_{SD}, and I_{OFF}, were considered in assessing the I_{ON} of 2D-material MOSFETs based on the ITRS requirements for high performance logic applications for the production years from 2018 to 2026. The transistors in high performance integrated circuits have both the highest performance and the highest leakage current. The ITRS-projected values of V_{DD}, EOT, R_{SD}, and I_{OFF} for HP logic transistors at different production years were obtained from the 2012 edition of ITRS [89].

The I_{ON} of HP logic transistors was extracted at V_{DS} = V_{DD} and V_{GS} – V_{OFF} = V_{DD}. V_{OFF} is defined to be the V_{GS} at which I_{DS} = I_{OFF}. I_{OFF} of 100 nA/μm which corresponds to the $I_{SD,leak}$ of HP logic transistors was used in the I_{ON} extraction. From year 2018 to 2026, the ITRS-projected V_{DD} and EOT for HP logic transistors are downscaled from 0.73 V to 0.57 V and 0.68 nm to 0.45 nm, respectively while the

ITRS-projected R_{SD} decreases from 218 Ωμm to 104 Ωμm. The reduction of V_{DD} degrades the I_{ON} while the decrease of EOT leads to larger C_{OX} which improves the gate control for achieving higher current. The continual decrease in R_{SD} with production years ensures that the applied voltages are mainly dropped across the intrinsic MOSFET, leading to higher I_{ON}. The combination of the positive effect from reducing EOT and R_{SD} and the negative effect from downscaling the V_{DD} on I_{ON} determines the overall drive current for each production year.

3.3.3(I): I_{ON} Assessment of n-MOSFETs for HP Applications

As shown in Fig. 3.6(a), the I_{ON} of all 2D-material n-MOSFETs studied satisfies the I_{ON} requirements of HP logic transistors for year 2018 to 2024. For the production year of 2026, the I_{ON} of silicane, WS_2, WS_2, and MoS_2 n-MOSFETs is above the requirement while germanane and $MoSe_2$ n-MOSFETs barely meet the I_{ON} requirement.

In order to understand the trends observed in Fig. 3.6(a), the effect of R_{SD} was excluded from I_{ON} so that only the effects of V_{DD} and EOT on I_{ON} of each production year were examined. Fig. 3.6(b) shows the normalized ballistic I_{ON} at different production years calculated using the ITRS-projected V_{DD} and EOT without considering the effect of *RSD*. The ballistic I_{ON} in Fig. 3.6(b) was normalized to the I_{ON} of 2018. It can be seen from Fig. 3.6(b) that the variation in the ballistic I_{ON} of silicane, WS_2, WSe_2, MoS_2, and $MoSe_2$ n-MOSFETs for different production years is rather small. This small variation in I_{ON} indicates that the negative effect from decreasing V_{DD} is almost compensated by the positive effect from reducing EOT on the I_{ON}. In contrast, germanane n-MOSFET shows a larger decrease with ~35% reduction in I_{ON} from year 2018 to 2026. This implies that the negative effect from the

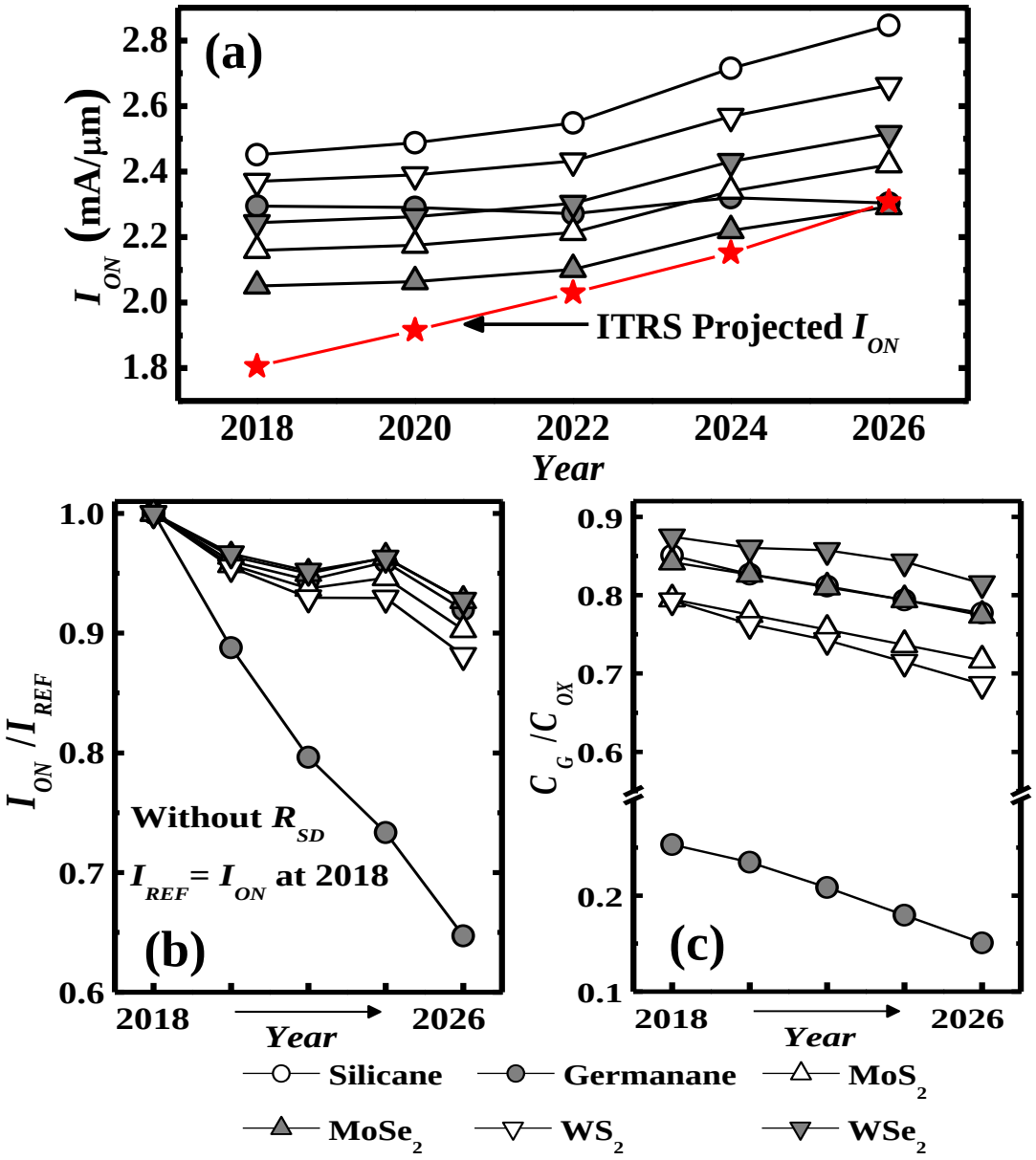

Fig. 3.6. I_{ON} of n-MOSFET for high performance logic application: (a) I_{ON}, (b) Ballistic I_{ON}/I_{REF} without considering R_{SD}, where I_{REF} is the I_{ON} of year 2018, and (c) C_G/C_{OX} at different years of production.

V_{DD} reduction dominates the positive effect from the decrease of EOT in germanane n-MOSFET, resulting in a larger reduction in I_{ON} with the production years.

Fig. 3.6(c) shows the ratio of C_G to C_{OX} for different production years. It is apparent from Fig. 3.6(c) that the C_G/C_{OX} of germanane n-MOSFET is the lowest

compared to those of other n-MOSFETs. This is due to C_Q effect in germanane n-MOSFET as shown in Table 3.3 where C_G is dominated by C_Q. Hence, germanane n-MOSFET does not benefit from the larger C_{OX} due to the reduction of EOT with production years. The negative effect from the decrease of V_{DD} with production years degrades the I_{ON} of germanane n-MOSFET. This explains the larger I_{ON} reduction with production years in germanane n-MOSFET shown in Fig. 3.6(b).

Subsequently, the effect of ITRS-projected R_{SD} was included in the calculation of I_{ON}. Since R_{SD} is the highest for year 2018 and gradually decreases with the years of production, the degree of I_{ON} degradation due to R_{SD} is the largest for 2018 and decreases with progressing production years. This explains the increased trend of I_{ON} over the production years in silicane, WS_2, WSe_2, MoS_2, and $MoSe_2$ n-MOSFETs shown in Fig. 3.6(a). For germanane n-MOSFET, the positive effect of decreasing R_{SD} compensates the negative effect of reducing V_{DD} with production years on I_{ON}, resulting in I_{ON} almost independent of the production years.

3.3.3(II): I_{ON} Assessment of p-MOSFETs for HP Applications

All 2D-material p-MOSFETs show increasing I_{ON} trend with production years as depicted in Fig. 3.7(a). The I_{ON} of germanane, silicane, and WSe_2 p-MOSFETs consistently meets the I_{ON} requirement for HP technology for all the production years studied. On the contrary, MoS_2 p-MOSFET fails to deliver the I_{ON} required for HP technology for all the production years examined. Similarly, Fig. 3.7(b) shows the normalized ballistic I_{ON} of p-MOSFET without considering the effect of RSD. A relatively small variation in I_{ON} with production years shown in Fig. 3.7(b) signifies that the opposite effects on I_{ON} from decreasing EOT and V_{DD} with production years nearly cancel out each other. The larger C_G/C_{OX} shown in Fig. 3.7(c) reveals that all

the p-MOSFETs studied operate in the classical regime where C_Q is larger than C_{OX} such that C_G is mainly determined by C_{OX}. As mentioned above, the effect of R_{SD} gets smaller with production years due to the decrease in the ITRS-projected R_{SD} from 218 Ωμm to 104 Ωμm, resulting in the rising trend in I_{ON} with progressing production years for all 2D-material p-MOSFETs studied as observed in Fig. 3.7(a).

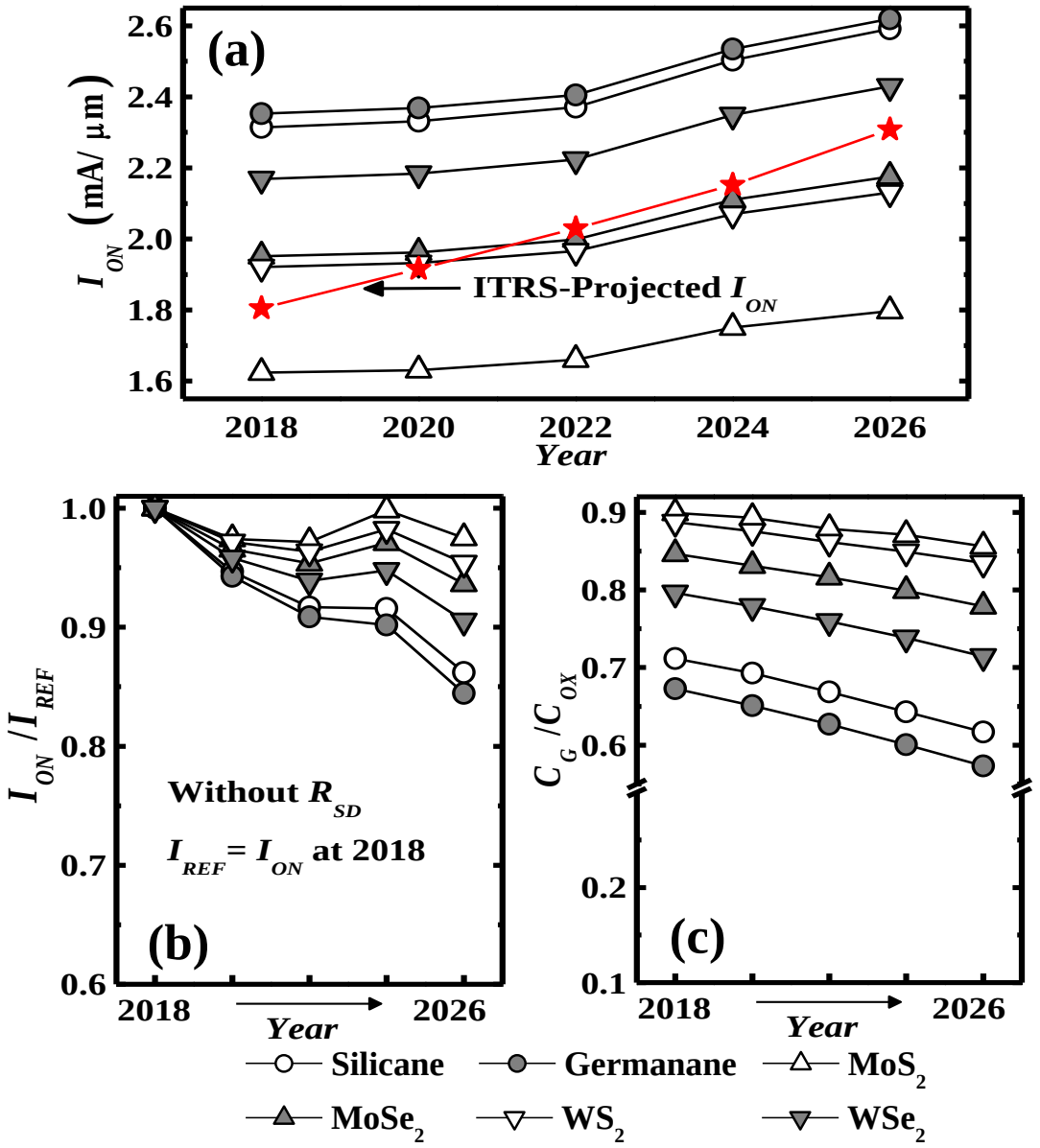

Fig. 3.7. I_{ON} of p-MOSFET for high performance logic application: (a) I_{ON}, (b) Ballistic I_{ON}/I_{REF} without considering R_{SD}, where I_{REF} is the I_{ON} of year 2018, (c) C_G/C_{OX} at different years of production.

3.3.4: V_{DD} Scalability Assessment Based on ITRS Requirements for Low Operating Power Technology

The V_{DD} scalability of 2D-material MOSFETs is examined based on the I_{ON} requirement for low operating power (LOP) technology from year 2018 to 2026. The transistors in LOP chips have lower performance and considerably lower leakage current. The V_{DD} scalability of a transistor was performed by scanning through a range of V_{DD} to identify the lowest V_{DD} [minimum scalable V_{DD} ($V_{DD,min}$)] which yields the required I_{ON} of LOP technology specified in ITRS $I_{SD,leak}$ of LOP technology (5 nA/μm) was used in the extraction of minimum scalable V_{DD}.

3.3.4 (I): V_{DD} Scalability Assessment of n-MOSFETs for LOP Applications

As shown in Fig. 3.8(a), all the 2D-material n-MOSFETs fulfill the I_{ON} requirement of LOP logic transistor for all the production years investigated with their minimum scalable V_{DD} below the ITRS-projected V_{DD}. Silicane n-MOSFET has the lowest scalable V_{DD} for the all the production years. Germanane n-MOSFET outperforms most of the 2D-material n-MOSFETs for the early production years studied in terms of the V_{DD} scalability. However, the decrease of the minimum scalable V_{DD} of Germanane n-MOSFET with production years is less drastic as compared to those of other n-MOSFETs.

Since leakage current is one of the major concerns for LOP logic application, lower V_{DD} and thicker EOT are projected for the LOP logic transistors compared to those of HP technology. The use of thicker EOTs in LOP logic transistors implies that the transistors operate in the carrier density limited regime caused by lower C_G. In the carrier density limited regime, the effect of the carrier velocity becomes dominant.

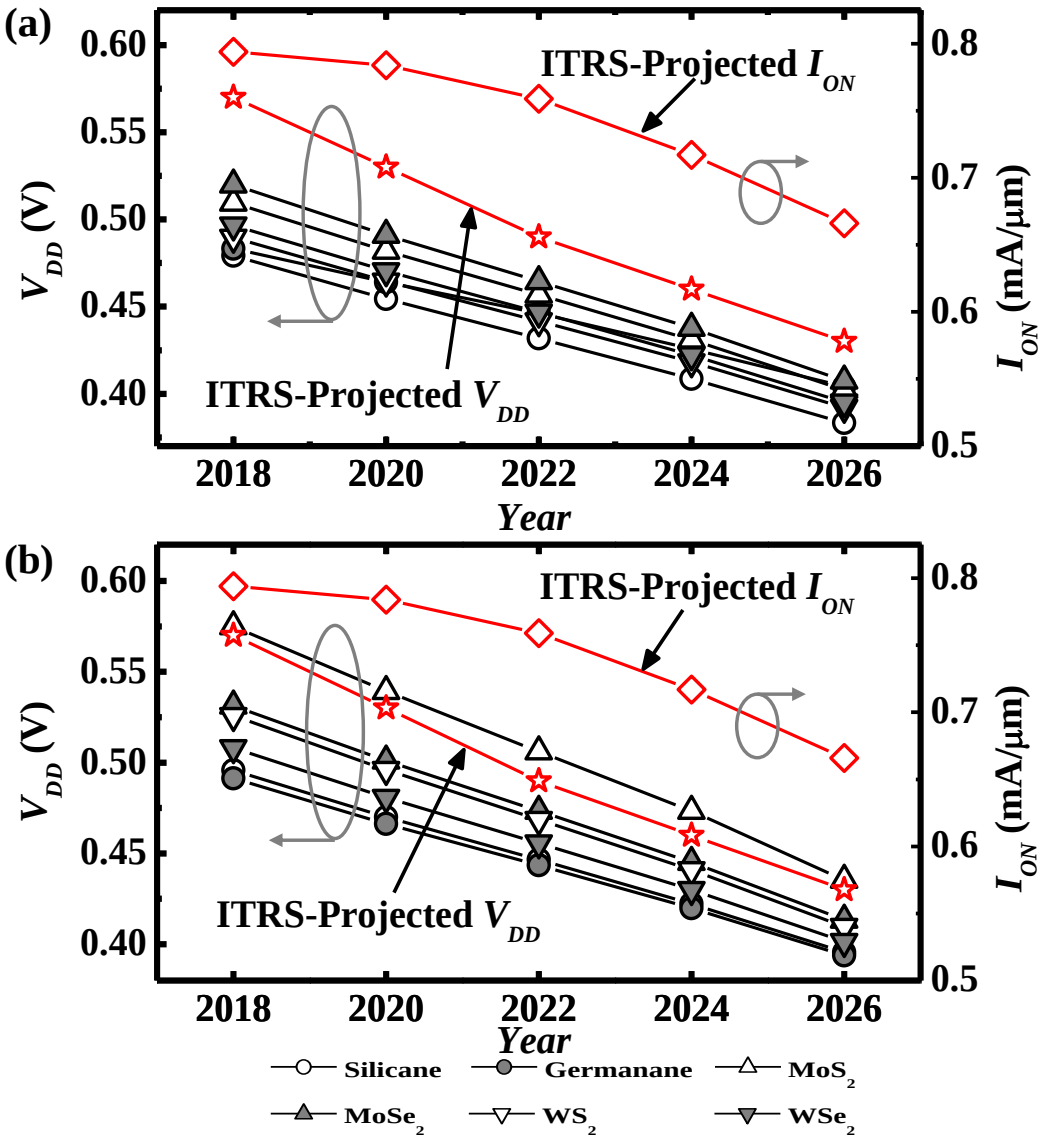

Fig. 3.8. Minimum scalable V_{DD} ($V_{DD,min}$) at different production years for low operating power logic applications: (a) n-MOSFET (b) p-MOSFET. $V_{DD,min}$ is defined to be the smallest V_{DD} required by the MOSFET to deliver the ITRS-projected I_{ON}.

The degradation of the average carrier density due to thicker EOT is less pronounced for germanane n-MOSFET since its operation is far away from the classical regime. At the condition of larger EOT, the higher electron velocity of germanane n-MOSFET leads to lower V_{DD} needed to achieve the required I_{ON}. This explains the minimum scalable V_{DD} of germanane n-MOSFET among the lowest for the year of 2018 due to

thicker ITRS-projected EOT (0.78 nm). When the production years advance from 2020 to 2026, the downscaling of EOT improves the C_G of all the n-MOSFETs except germanane n-MOSFET. The greater charge density induced by larger C_G enables further scaling of V_{DD} to much lower values. This is demonstrated in Fig. 3.8(a) where the minimum scalable V_{DD} of other n-MOSFETs is gradually lower than that of germanane n-MOSFET with production years.

3.3.4 (II): V_{DD} Scalability Assessment of p-MOSFETs for LOP Applications

The minimum scalable V_{DD} of all 2D-material p-MOSFETs except MoS_2 p-MOSFET is within the ITRS-projected V_{DD} as illustrated in Fig. 3.8(b). The rate of minimum scalable V_{DD} reduction with production years is almost identical for all the p-MOSFETs studied. Both germanane and silicane p-MOSFETs show better V_{DD} scalability than those of 2D-TMDs p-MOSFETs for all the production years examined. The minimum scalable V_{DD} of germanane p-MOSFET is the lowest followed by that of silicane p-MOSFET. MoS_2 p-MOSFET fails to deliver the required I_{ON} within the ITRS-projected V_{DD} for all the production years investigated. The poorer V_{DD} scalability of MoS_2 p-MOSFET is mainly due to its lower average hole velocity. Since the energy separation of the first two highest valence valleys of MoS_2 is significantly small, holes not only occupy the highest valence valley at K point but also at the second highest valence valley at Γ point which has a larger effective mass. The inferior average hole velocity in MoS_2 p-MOSFET results in higher minimum V_{DD} required to meet the I_{ON} requirement compared with those of other p-MOSFETs.

3.4 Conclusions

In this study, the upper I_{ON} performance limit of silicane and germanane is examined and compared with those of 2D-TMDs MOSFETs. Our results show that silicane n-channel transistor with reasonable electron density of states and velocity outperforms the n-channel transistors made of other 2D materials studied (Germanane, MoS_2, $MoSe_2$, WS_2, and WSe_2) in terms of I_{ON} for the same I_{OFF} of 5 nA/μm at V_{DD} = 0.6 V. However, the relatively lower electron affinity of silicane due to larger band gap may cause higher gate leakage attributed to lower tunneling barrier height. Germanane n-MOSFET has low density of states making its operating regime far away from the classical regime. Thus, the I_{ON} of germanane n-MOSFET is less sensitive to the EOT. This makes germanane n-MOSFET suitable for the low standby power applications where thicker EOT is desirable. Germanane p-MOSFET delivers the highest I_{ON} followed by silicane p-MOSFET and their ballistic I_{ON} performance is better than those of 2D-TMDs p-MOSFETs. The benchmarking of ballistic drive currents based on the ITRS I_{ON} requirement for HP and LOP technology reveals that silicane MOSFET meets the I_{ON} requirement of HP and LOP technology for years 2018 to 2026. Germanane MOSFET satisfies the I_{ON} requirement of HP and LOP logic transistors, except its n-MOSFET for the I_{ON} requirement of HP logic transistors for the production year of 2026.

Chapter 4

Voltage Scalability of Group IV, III-V, and 2D-Materials Ultra-Thin-Body Transistor based on ITRS metrics

4.1 Introduction

In this Chapter, we address the key issue pertaining to the choice of channel materials to effectively scale the V_{DD} of double-gate ultra-thin body (DG-UTB) transistors for future technology nodes. The channel materials considered comprise group IV (Ge), III-V [GaSb, InAs, and $In_{0.3}Ga_{0.7}Sb$], and 2-dimensional (2D) materials [black phosphorus (BP), 2D-transition metal dichalcogenides (TMDs), hydrogenated silicene (silicane), and hydrogenated germanene (germanane)]. The bias conditions and the parameters for DG-UTB MOSFET with various geometries are based on the projected values from the 2013 edition of the International Technology Roadmap for Semiconductors (ITRS) [89], as summarized in Table 4.1.

The ITRS-projected device specifications for high performance (HP) technology are used for Ge, III-V, and BP. This is because Ge [194]-[196] and III-V [9]-[22] materials were reported to have higher carrier mobilities. The device specifications for low power (LP) technology projected by the ITRS are used for 2D materials since they have larger effective masses and band gaps [46]-[52]. Hence, the leakage current due to direct source to drain tunneling and band-to-band tunneling of metal-oxide-semiconductor field-effect transistor (MOSFETs) based on 2D materials is expected to be lower.

DG-UTB MOSFET with silicon channel is included in the analysis for benchmarking purposes. The ON current performance was examined based on ITRS-projected device specifications for years 2018 and beyond. Subsequently, comprehensive assessment based on key performance metrics, such as minimum scalable voltage ($V_{DD,min}$) and power delay product (PDP), was carried out for technology node approaching the ultimate physical scaling limit. This corresponds to the production year of 2026 as projected by the ITRS.

4.2 Methodology

Fig. 4.1(a) shows the double-gate ultra-thin body MOSFET used in this study. The crystal structures of the channel materials considered in this work are shown in Fig. 4.1(b). Electrostatically, the channel potential is assumed to be fully controlled by the gate potential in order to exclude short-channel effects for evaluating the upper limit of the ballistic I_{ON} performance of DG-UTB MOSFET.

The electronic band structures (*E-k*) of group IV and III-V channel materials were obtained from the $sp^3d^5s^*$ [197] tight binding model and the *E-k* of 2D materials were from *ab-initio* calculations. Further details on the calculation of the *E-k* dispersion of 2D materials are given in [192], [198]. The ballistic I_{ON} was simulated using the semi-classical top-of-barrier model coupled with a capacitive model [152]-[154], considering the effect of the full *E-k* dispersion. The current due to the direct source to drain tunneling was captured using the Wentzel–Kramers–Brillouin (WKB) approximation. The WKB transmission probability (*T*) at a particular energy level (*E*) was calculated as:

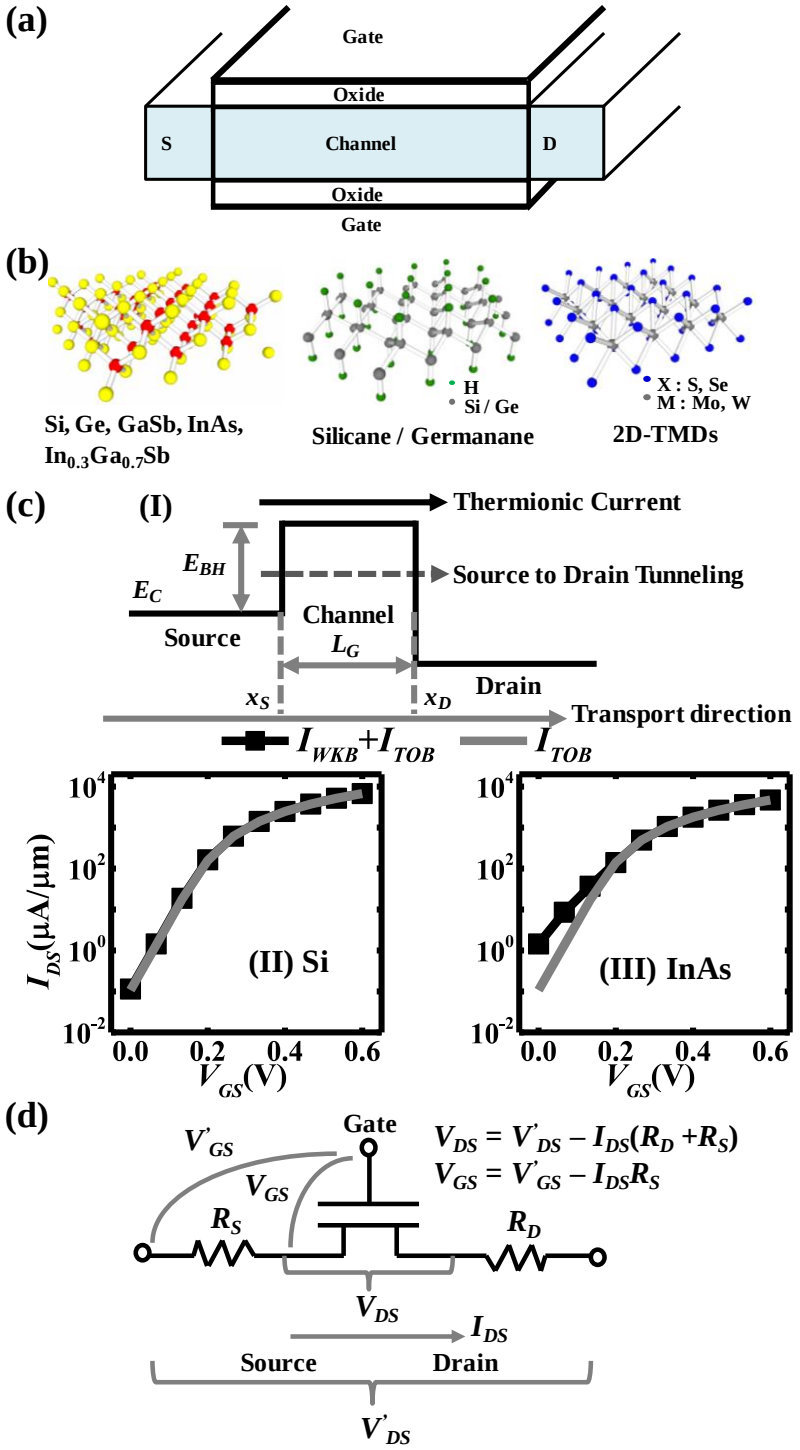

Fig. 4.1. (a) Double-Gate Ultra-Thin Body (DG-UTB) device structure. (b) Crystal structures of the channel materials considered in this work (c) (I) Conduction band profile across source, channel, and drain region. The barrier height is denoted as E_{BH}. Gate transfer characteristic of Si (II) and InAs (III) UTB n-MOSFETs based on ITRS specification for year 2026. Leakage current of InAs n-MOSFET increases after including the direct source-to-drain tunneling current (I_{WKB}) in addition to the thermionic current (I_{TOB}). (d) Circuit diagram of the simulated DG-UTB transistor with extrinsic source / drain resistance component (R_{SD}). A higher R_{SD} reduces the voltage drop across the intrinsic terminals of MOSFET.

$$T(E) = \exp\left(-2\int_{x_S}^{x_D} k(x)dx \right), \qquad 4.1(a)$$

$$k(x) = \frac{\sqrt{2m^*\left(E_{BH}(x) - E\right)}}{\hbar} \qquad 4.1(b)$$

where x_S and x_D are the positions at the source and drain region, respectively, whose conduction band (E_C) value equals E. $k(x)$ is the decay rate of carrier at the position x calculated based on the effective mass (m^*) model. E_{BH} and $\hbar$ are potential barrier height and reduced Planck constant, respectively. The values of m^* used in 4.1(b) were extracted from the conduction band minimum and valence band maximum of subbands of all channel materials considered at different surface orientations. The potential profile was assumed to be rectangular and the values of the channel length projected by the ITRS were used. The source/drain doping (N_D) of silicon was assumed to be 1×10^{20} cm^{-3} and a N_D of 1×10^{19} cm^{-3} was used for all of the other channel materials considered.

R_{SD} was included in the ballistic I_{ON} calculation using the model depicted in Fig. 4.1(d). This was done by post-processing the intrinsic simulation results. All the projected values for body thickness (T_{body}), equivalent oxide thickness (EOT), parasitic resistance (R_{SD}), V_{DD}, and gate length (L_G) from the 2013 edition of ITRS are summarized in Table 4.1. Since the ITRS projected values for gate length are in sub-10 nm regime, the scatterings are negligible. Hence, the transport becomes more ballistic which makes the ballistic transport assumption in our calculation acceptable.

For each channel material, the ballistic I_{ON} of DG-UTB MOSFET was exhaustively simulated along high symmetry transport directions on different surface orientations. This is to identify an optimum orientation and direction which gives the highest I_{ON} for each channel material considered. Three surface orientations [(100),

Table 4.1. T_{body}, EOT, R_{SD}, V_{DD}, and L_G for production years of 2018, 2022, and 2026, as projected by the 2013 ITRS.

Year		2018	2022	2026
T_{body} (nm)				
HP	Si/BP	4.1	2.8	2.0
	Ge	9.2	5.8	3.4
	III-V	8.5	5.3	3.0
LP	Si/2D Materials	4.7	3.2	2.2
EOT (nm)				
HP	Si/BP	0.64	0.54	0.45
	Ge	0.68	0.56	0.45
	III-V	0.68	0.56	0.45
LP	Si/2D Materials	0.64	0.54	0.45
R_{SD} (Ω.μm)				
HP	Si/BP	117	111	131
	Ge	149	105	72
	III-V	131	96	70
LP	Si/2D Materials	117	111	131
V_{DD} (V)				
HP	Si/BP	0.78	0.72	0.66
	Ge	0.63	0.58	0.54
	III-V	0.63	0.58	0.54
LP	Si/2D Materials	0.78	0.72	0.66
L_G (nm)				
HP	Si/BP	12.7	8.8	6.1
	Ge	14.0	9.3	5.8
	III-V	14.0	9.3	5.8
LP	Si/2D Materials	14.6	10.1	7.0

(110), and (111)] were examined for channel materials from group IV and III-V. For MOSFETs based on 2D materials, transport directions along k_x (Γ→K) and k_y (Γ→M) were considered.

For all analysis of the electrical performance, I_{ON} was extracted at $V_{DS} = V_{DD}$ and $V_{GS} = V_{DD} + V_{OFF}$. V_{OFF} is defined to be the V_{GS} at which $I_{DS} = I_{OFF}$ and $V_{DS} = V_{DD}$. I_{OFF} corresponds to the subthreshold source/drain leakage current ($I_{SD,leak}$) of HP and LP technology.

4.3 Results and Discussions

4.3.1 I_{ON} Performance of MOSFET for HP Technology Targeting Year 2018, 2022, and 2026

Fig. 4.2 shows the calculated ballistic I_{ON} for n-MOSFETs (filled) and p-MOSFETs (open) with channel materials from group IV, III-V, and BP targeting HP application for year 2018, 2022, and 2026. The I_{ON} values shown in Fig. 4.2 are the highest I_{ON} obtained from the exhaustive calculations performed on different surface orientations and transport directions for channel materials studied in this work. The ITRS-projected values for I_{ON} are plotted using solid red lines for all production years studied.

4.3.1 (I): *HP Technology: Comparison of ballistic I_{ON} of n-MOSFET*:

For the n-MOSFETs assessed for the HP technology, BP n-MOSFET exhibits the highest I_{ON}, followed by silicon n-MOSFET, for all production years. Amongst III-V channel materials considered, GaSb n-MOSFET outperforms the rest in terms of I_{ON}. The I_{ON} magnitudes of InAs and $In_{0.3}Ga_{0.7}Sb$ n-MOSFETs are relatively smaller [1.1 to 1.5 mA/μA for year 2026] with InAs n-MOSFET having the smallest I_{ON} for all production years examined.

It is worth noting that the ballistic I_{ON} of BP n-MOSFET along the k_x and k_y directions shows distinct characteristics. This is due to highly anisotropic nature in the electronic band structures of BP. Higher I_{ON} is observed along the k_x than the k_y transport direction. It can be attributed to higher carrier velocity resulting from the smaller longitudinal effective mass (m_l) and larger density of states (DOS) owing to the larger transverse effective mass (m_t). This observation is also consistent with ref. [199].

For n-MOSFETs based on III-V semiconductors, GaSb n-MOSFET consistently delivers the highest I_{ON} along $[\bar{1}10]$ direction on (110) surface orientation for all production years studied. On the other hand, the I_{ON} of InAs and $In_{0.3}Ga_{0.7}Sb$ n-MOSFETs appears to be less dependent on the orientations and transport directions. This is because the I_{ON} of both InAs and $In_{0.3}Ga_{0.7}Sb$ n-MOSFETs is mainly contributed by Γ valley. The isotropic energy dispersion at Γ valley results in little dependence on orientation and transport direction.

4.3.1 (II): *HP Technology: Comparison of ballistic I_{ON} of p-MOSFET*:

In terms of the I_{ON} performance for p-MOSFETs, the I_{ON} of BP and Si p-MOSFET outperforms the rest for all production years. Anisotropic trend in the I_{ON} is also observed in BP p-MOSFET with k_x direction exhibiting higher I_{ON}. Si p-MOSFET along $[\bar{1}10]$ direction on (110) surface orientation exhibits the highest I_{ON} for year 2018 and 2022 with their I_{ON} ranging from ~3.5 to ~3.8 mA/μm. For year 2026, the highest I_{ON} is found at [110]/(100) for Si p-MOSFET.

Ge, GaSb, InAs, and $In_{0.3}Ga_{0.7}Sb$ p-MOSFETs show the highest I_{ON} along $[\bar{1}10]$ transport direction on (011) surface. The I_{ON} of Ge p-MOSFET is relatively higher than those of III-V p-MOSFETs and its value is in the range of ~2.4 to ~3.3 mA/μm for year 2018 to 2026. The I_{ON} of InAs p-MOSFET is the lowest compared to those of other p-MOSFETs, ranging from 2.1 to 2.80 mA/μA for production years from 2018 to 2026.

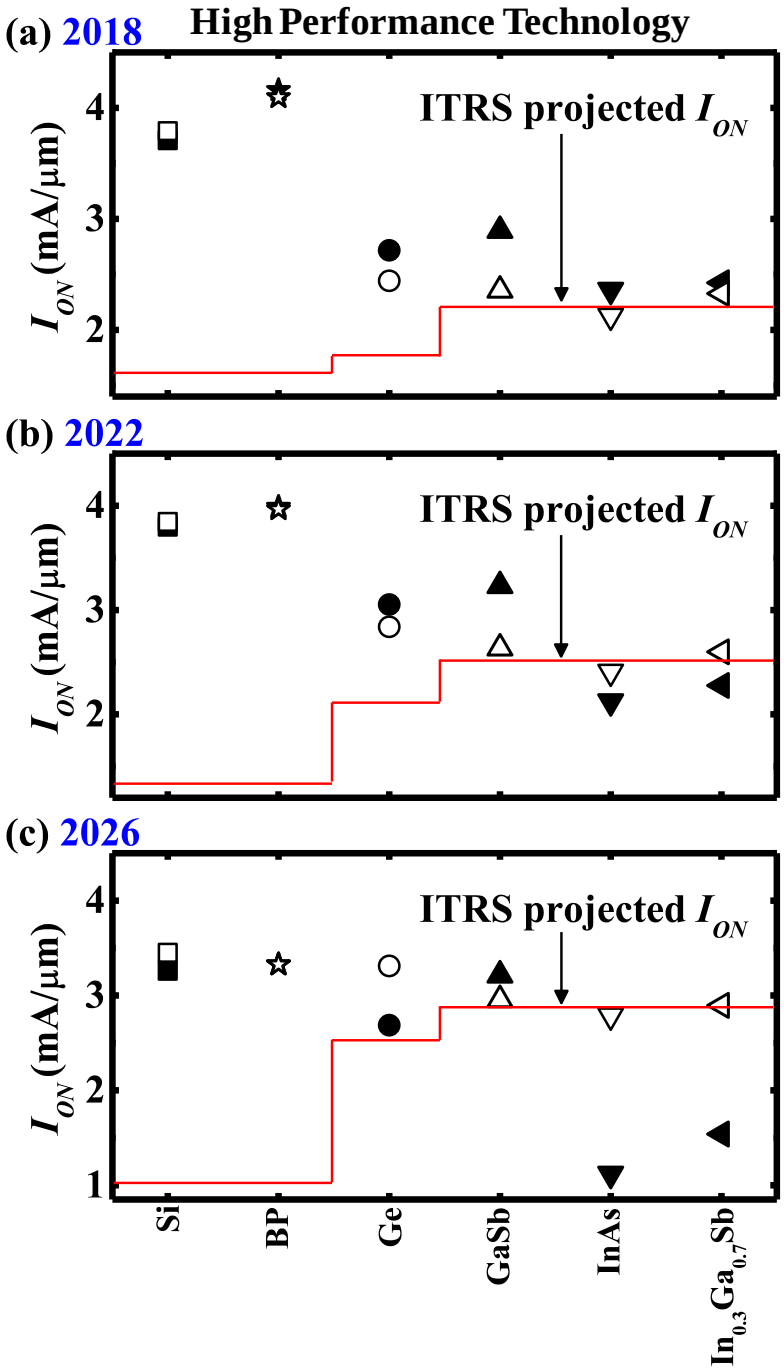

Fig. 4.2. HP technology: Comparison of ballistic I_{ON} of n-MOSFET (filled) and p-MOSFET (open) for HP technology for production year of (a) 2018; (b) 2022; and (c) 2026. BP and Si n-MOSFETs provide higher I_{ON} than the rest for all the production years. For all production years studied, the I_{ON} values of InAs and $In_{0.3}Ga_{0.7}Sb$ for both n-MOSFETs and p-MOSFETs are lower compared to those of other n-MOSFETs and p-MOSFETs. Higher I_{ON} observed in Si and BP n-MOSFET and p-MOSFET in the production years of 2018 and 2022 is mostly due to larger V_{DD} and smaller EOT projected by the 2013 ITRS.

4.3.2 I_{ON} Performance of MOSFET for LP Technology Targeting Year 2018, 2022, and 2026

For all 2D materials considered for the LP technology, their device specifications are based on the ones projected for the Si technology by the 2013 ITRS. Fig. 4.3 shows a comparison of I_{ON} of n-MOSFETs (filled) and p-MOSFETs (open), respectively, based on the ITRS-projected specifications for LP technology. The I_{ON} values of 2D materials n-MOSFETs, except for BP n-MOSFET, appear to be less dependent on the transport direction with I_{ON} along k_x direction being slightly larger than that of k_y direction.

4.3.2 (I): *LP Technology: Comparison of ballistic I_{ON} of n-MOSFET:*

Si n-MOSFET exhibits the highest I_{ON} for year 2018 and 2022, as featured in Fig. 4.3. It was found that Si n-MOSFET with transport direction along [110] on (100) surface orientation provides the best current drivability. n-MOSFETs based on BP, silicane, and WS_2 offer comparatively higher I_{ON} among the 2D material n-MOSFETs while $MoSe_2$ n-MOSFET delivers rather low I_{ON} for all production years studied. It is interesting to note that a larger degree of I_{ON} reduction is observed in germanane n-MOSFET from year 2018 to 2026. The explanation for this trend is provided in the Section III (C).

4.3.2 (II): *LP Technology: Comparison of ballistic I_{ON} of p-MOSFET:*

The I_{ON} comparison of p-MOSFETs in Fig. 4.3 reveals that Si and BP p-MOSFETs offer higher I_{ON} than the rest for all production years examined. Si p-MOSFET shows higher I_{ON} on (100) and (110) surface orientations. Germanane and silicane p-MOSFETs offer higher I_{ON} than 2D-TMDs p-MOSFETs and their I_{ON} magnitude is around ~1.5 to ~1.8 mA/μm at year 2026 and 2018. MoS_2 p-MOSFET

has the worst current drivability with its current magnitude below 1.25 mA/μm for all production years studied. The inferior I_{ON} performance of MoS_2 p-MOSFET is mainly due to its larger hole effective mass [198].

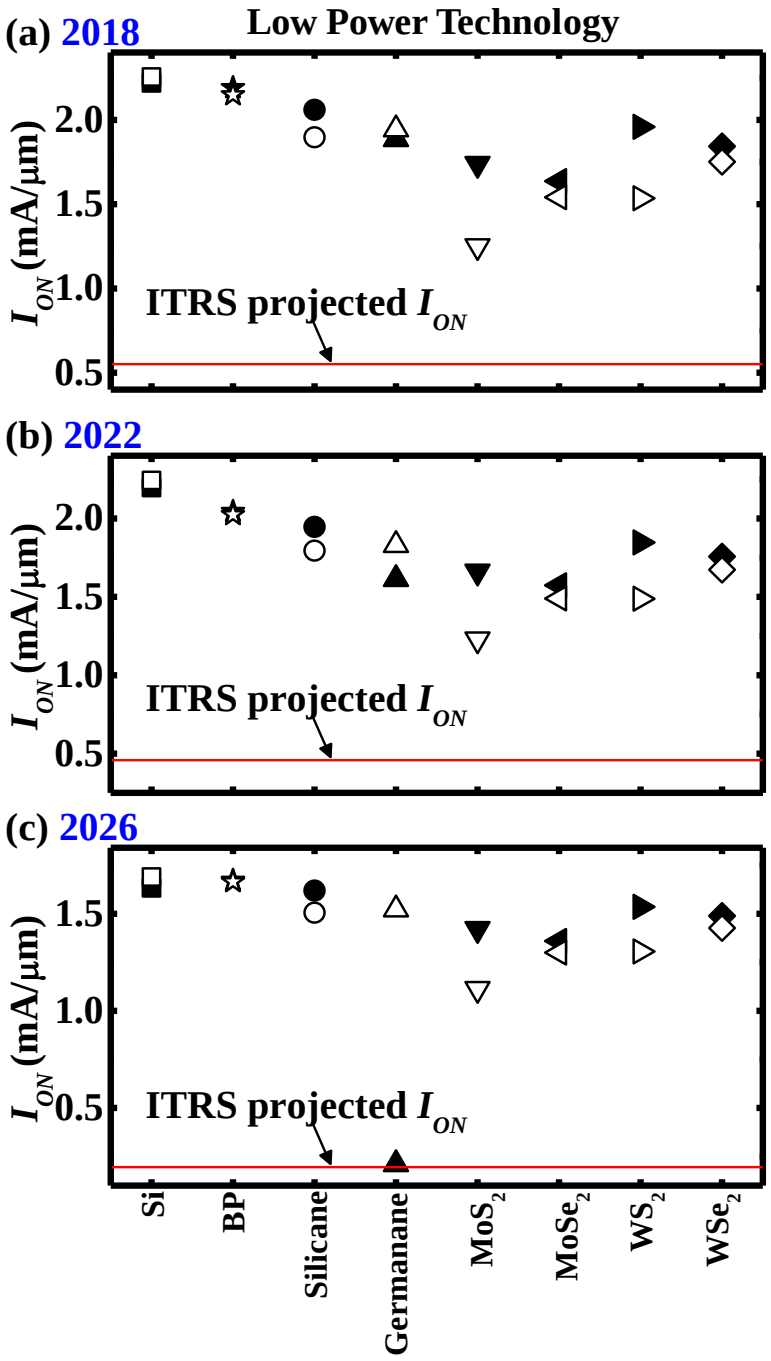

Fig. 4.3. LP technology: Comparison of ballistic I_{ON} of n-MOSFET (filled) and p-MOSFET (open) for LP technology for production year of (a) 2018; (b) 2022; and (c) 2026.

4.3.3 Detailed Performance Evaluation Based on 2026 ITRS Metrics

The V_{DD} scalability and power delay product (PDP) of DG-UTB MOSFETs were further assessed based on the ITRS-projected device specifications for HP and LP technology for the production year of 2026. For the assessment of V_{DD} scalability, the minimum V_{DD} ($V_{DD,min}$) required to deliver the benchmark I_{ON} was calculated for all channel materials studied. The benchmark I_{ON} is the I_{ON} of Si n-MOSFET and p-MOSFET calculated at the production year of 2026. The PDP was computed as $[Q_{ON} - Q_{OFF}]V_{DD,min}$, where Q_{ON} and Q_{OFF} are the total charge in the channel at the ON ($V_{GS} = V_{DS} = V_{DD}$) and OFF ($V_{GS} = 0$, $V_{DS} = V_{DD}$) states, respectively.

The ratios of $V_{DD,min}$ of n-MOSFET and p-MOSFET to that of Si n-MOSFET and p-MOSFET for HP and LP technology are shown in Fig. 4.4(a) and Fig. 4.6(a), respectively. The values of PDP of n-MOSFETs and p-MOSFETs for HP and LP technology are depicted in Fig. 4.4(b) and Fig. 4.6(b), respectively.

In order to understand the voltage scalability and PDP trends shown in Fig. 4.4 and Fig. 4.6, the total charge density in the channel (Q_{ON}) and the average carrier velocity (V_{AVG}) at the ON state of n-MOSFETs and p-MOSFETs for HP and LP technology were analyzed and plotted in Fig. 4.5 and Fig. 4.7, respectively.

4.3.3 (I): V_{DD} Scalability and PDP Assessment of MOSFETs for 2026 HP Technology:

4.3.3 I (a): *Voltage Scalability and PDP of n-MOSFET*:

Fig. 4.4(a) shows that GaSb n-MOSFET requires the smallest V_{DD} to deliver the benchmark I_{ON} with its $V_{DD,\,min}$ being ~18% lower than that of Si n-MOSFET. This is followed by Ge n-MOSFET. . The values of $V_{DD,min}$ of InAs and $In_{0.3}Ga_{0.7}Sb$ n-MOSFETs are larger than the one of Si n-MOSFET.

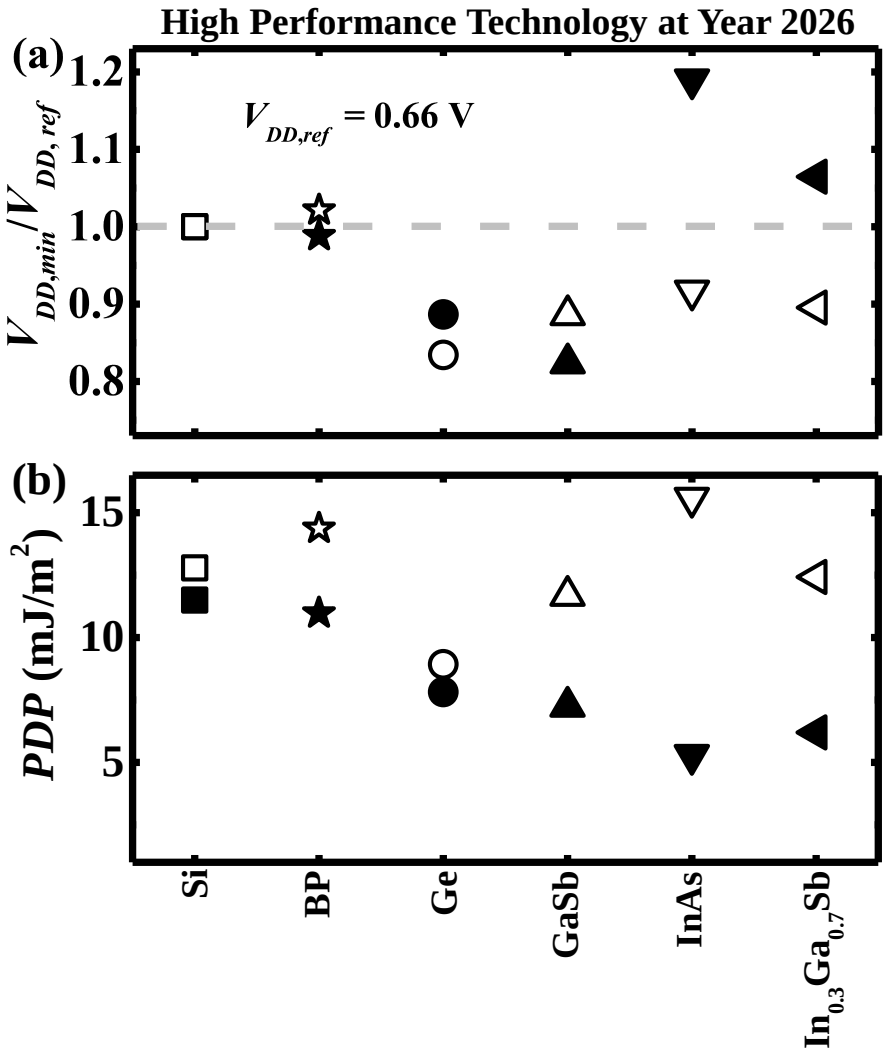

Fig. 4.4. HP technology at year 2026: (a) $V_{DD,min}/V_{DD,ref}$ of n-MOSFET (filled) and p-MOSFET (open), where V_{DD},ref is the $V_{DD,min}$ of Si MOSFET. $V_{DD,min}$ is defined to be the smallest value of V_{DD} required to deliver the I_{ON} of Si n-MOSFET and p-MOSFET, respectively at the production year of 2026. (b) Power delay product (PDP) across different channel materials.

As shown in Fig. 4.4(b), the PDP values of Si and BP n-MOSFETs are higher than the rest. InAs and $In_{0.3}Ga_{0.7}Sb$ n-MOSFETs offer comparatively lower PDP value despite their larger $V_{DD,min}$ among the n-MOSFETs studied.

Fig. 4.5(a) shows that Si and BP n-MOSFETs have relatively larger Q_{ON}, followed by GaSb and Ge n-MOSFETs while the Q_{ON} of InAs and $In_{0.3}Ga_{0.7}Sb$ n-MOSFETs are among the lowest.

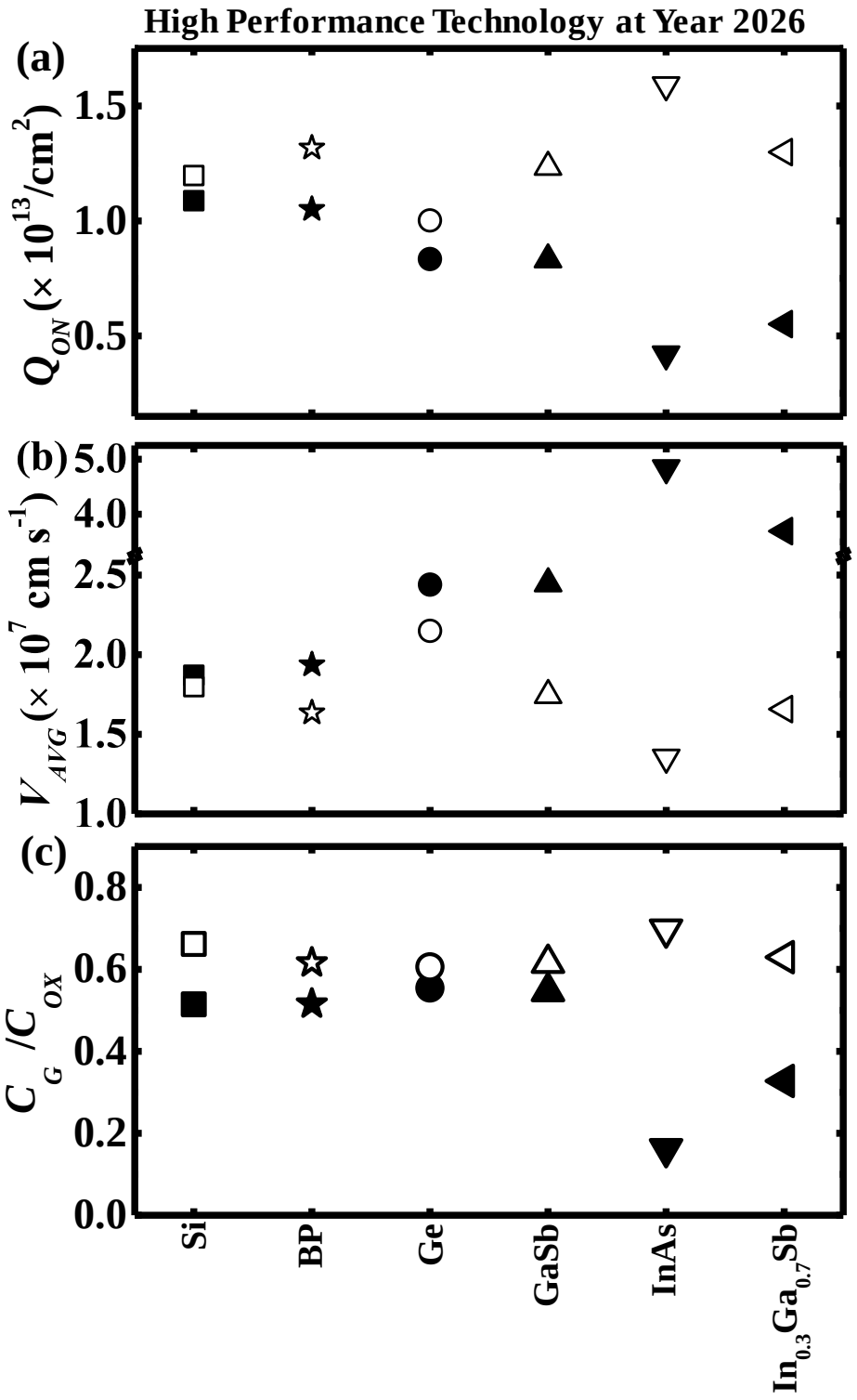

Fig. 4.5. HP technology at year 2026: (a) Carrier density in the channel of n-MOSFET (filled) and p-MOSFET (open) at the ON state. (b) Average carrier velocity of n-MOSFET and p-MOSFET at the ON state. (c) C_G/C_{OX} at the ON state. InAs and $In_{0.3}Ga_{0.7}Sb$ n-MOSFETs with smaller electron effective mass at Γ valley have the ratio of C_G to C_{OX} smaller than 0.4, indicating that they are operating in quantum capacitance regime.

Although higher Q_{ON} is observed in Si and BP n-MOSFETs, their V_{AVG} is lower than the rest at the ON state, as shown in Fig. 4.5(b). InAs n-MOSFET has the highest V_{AVG} [~5×10^7 cm s^{-1}]. This is due to its relatively smaller electron effective mass at the Γ valley. Nonetheless, the I_{ON} of InAs n-MOSFET is constrained by the density of states (DOS). This is reflected in Fig. 4.5(a) where the smallest Q_{ON} is observed in InAs n-MOSFET.

On the other hand, the V_{AVG} values of GaSb and Ge n-MOSFETs lie between the ones of $In_{0.3}Ga_{0.7}Sb$ and BP n-MOSFETs. GaSb and Ge n-MOSFETs with reasonable Q_{ON} and V_{AVG} give rise to lower $V_{DD,min}$ at the benchmark I_{ON} as shown in Fig. 4.4(a).

The smaller PDP value in InAs and $In_{0.3}Ga_{0.7}Sb$ n-MOSFETs can be attributed to their smaller electron effective mass. This results in higher carrier velocity and smaller amount of Q_{ON} required to switch from the OFF to ON state at the benchmark I_{ON}, as depicted in Fig. 4.5.

4.3.3 I (b): *Voltage Scalability and PDP of p-MOSFET*:

The $V_{DD,\,min}$ of all p-MOSFETs, except for BP p-MOSFET, is smaller than that of Si p-MOSFET. Ge p-MOSFET shows the best voltage scalability among all the p-MOSFETs studied. Its $V_{DD,min}$ is ~0.17 smaller than that of Si p-MOSFET, as shown in Fig. 4.4(a). Fig. 4.4(b) shows that the PDP value of all p-MOSFETs, except for BP and InAs p-MOSFETs, is smaller than that of Si p-MOSFET with Ge p-MOSFET having the lowest PDP.

The largest Q_{ON} amongst the p-MOSFETs studied is found in InAs p-MOSFET, followed by BP and $In_{0.3}Ga_{0.7}Sb$ p-MOSFETs. Ge p-MOSFET has the smallest Q_{ON}, as shown in Fig. 4.5(a). From the perspective of V_{AVG}, Ge p-MOSFET

outperforms the rest while InAs p-MOSFET exhibits the lowest V_{AVG}. The V_{AVG} values of Si and GaSb p-MOSFET are relatively similar [1.80×10^7 cm s^{-1}].

Even though Ge p-MOSFET has the lowest Q_{ON}, its highest V_{AVG} suffices to compensate the shortcoming in Q_{ON} to result in the smallest $V_{DD,min}$ (~0.83 of Si-p-MOSFET $V_{DD,min}$) and PDP. In contrast to Ge p-MOSFET, InAs p-MOSFET has the largest PDP caused by its great amount of Q_{ON}.

4.3.3 I (c): ***Gate Capacitance of n-MOSFET and p-MOSFET:***

Fig. 4.5(c) shows the ratio of gate capacitance (C_G) to oxide capacitance (C_{OX}) at the ON state ($V_{GS} = V_{DS} = V_{DD}$). C_G was obtained by taking the derivative of the total charge in the channel (Q) with respect to V_{GS} ($\partial Q/\partial V_{GS}$), where Q is a function of V_{GS} at $V_{DS} = V_{DD}$. C_{OX} was computed from the EOT used. The C_G/C_{OX} ratio of all the n-MOSFETs and p-MOSFETs, with the exception of InAs and $In_{0.3}Ga_{0.7}Sb$ n-MOSFETs, are greater than 0.5. InAs n-MOSFET has the lowest C_G/C_{OX} ratio of ~0.16.

A relatively small C_G/C_{OX} ratio in InAs and $In_{0.3}Ga_{0.7}Sb$ n-MOSFETs implies that both operate in the quantum capacitance (C_Q) regime. This quantum capacitance effect is regulated by the effective mass via density of states. Due to their smaller electron effective mass, the C_G of these materials is mainly determined by the C_Q. Since the ITRS-projected EOT decreases with production years, the C_Q effect becomes more evident. At highly scaled technology nodes, the I_{ON} of InAs and $In_{0.3}Ga_{0.7}Sb$ n-MOSFETs are expected to be limited by the DOS.

Unlike InAs and $In_{0.3}Ga_{0.7}Sb$ n-MOSFETs, the charges in the channel of other MOSFETs are primarily controlled by the C_{OX} which increases with production years due to reduction of EOT.

4.3.3 (II): V_{DD} Scalability and PDP Assessment of MOSFETs for 2026 LP Technology:

4.3.3 II (a): *Voltage Scalability and PDP of n-MOSFET*:

Fig. 4.6(a) shows that BP n-MOSFET offers the lowest $V_{DD,min}$. This is followed by silicane and WS_2 n-MOSFETs while Germanane n-MOSFET requires the highest $V_{DD,min}$ at the benchmark I_{ON}. Fig. 4.6(b) shows that Si, BP, silicane, and WS_2 offer relatively similar and lower PDP for n-MOSFET. The PDP of germanane n-MOSFET is the lowest despite its $V_{DD,min}$ being the largest.

In terms of the Q_{ON} shown in Fig. 4.7(a), n-MOSFETs based on 2D-TMDs display higher Q_{ON} than the rest with $MoSe_2$ n-MOSFET having the largest Q_{ON}. A nearly similar Q_{ON} is observed in BP and Si n-MOSFETs while germanane n-MOSFET has the lowest Q_{ON}.

Fig. 4.7(b) shows that germanane n-MOSFET has the highest average electron velocity, followed by BP and Si n-MOSFETs. 2D-TMDs n-MOSFETs have lower V_{AVG} with their magnitude being smaller than 1.5×10^7 cm s^{-1}.

The optimum Q_{ON} and V_{AVG} are attained in BP, Si, and silicane n-MOSFETs, resulting in lower $V_{DD,min}$ as depicted in Fig. 4.6(a). Highest carrier velocity in germanane n-MOSFET due to smaller effective mass at the Γ valley gives rise to a smallest PDP.

4.3.3 II (b): *Voltage Scalability and PDP of p-MOSFET*:

All p-MOSFETs studied show higher $V_{DD,min}$ than that of Si p-MOSFET, as illustrated in Fig. 4.6(a). BP p-MOSFET offers almost similar voltage scalability as Si p-MOSFET while MoS_2 p-MOSFET has the largest $V_{DD,min}$. Fig. 4.6(b) shows that Si p-MOSFET offers the lowest PDP, followed by BP, germanane, and silicane p-MOSFETs. The PDP of MoS_2 p-MOSFET is the highest which is ~24 mJ/m^2.

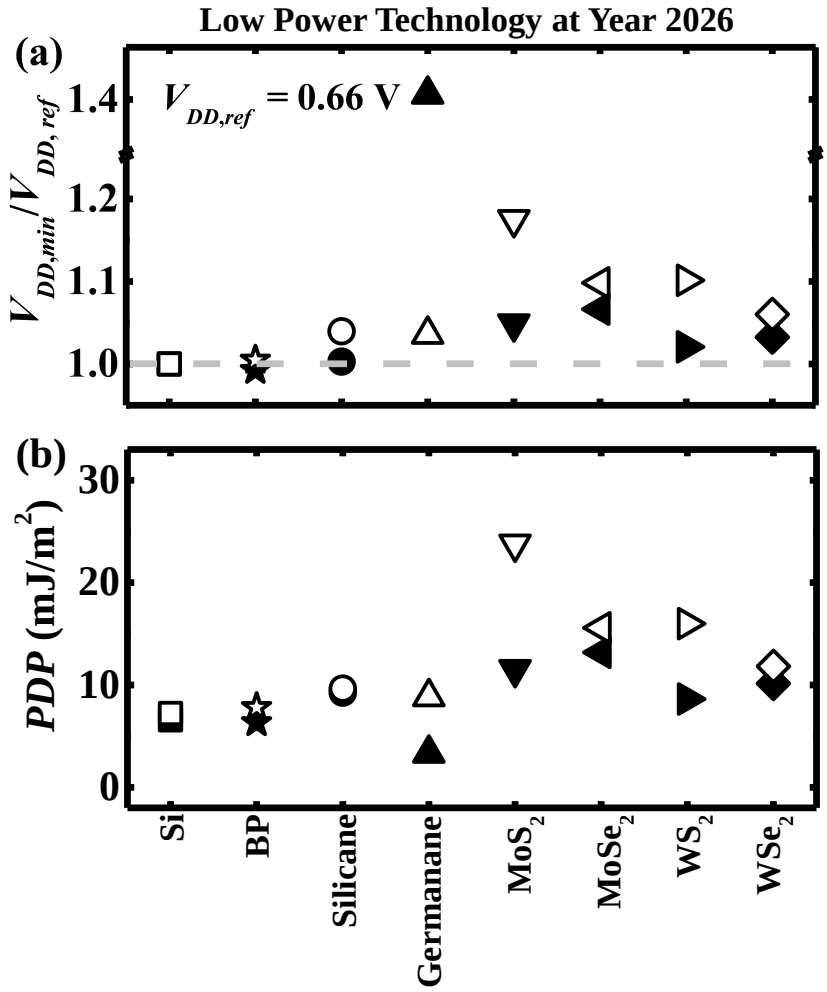

Fig. 4.6. LP technology at year 2026: (a) $V_{DD,min}/V_{DD,ref}$ of n-MOSFET (filled) and p-MOSFET (open). BP exhibits the smallest $V_{DD,min}$ for both n-MOSFET and p-MOSFET among the MOSFETs based on 2D materials. (b) Power delay product (PDP) across different channel materials.

For the Q_{ON} of p-MOSFETs, higher Q_{ON} is observed in the 2D-TMDs p-MOSFETs [Fig. 4.7(a)]. MoS_2 p-MOSFET has the largest Q_{ON} which translates to higher PDP as seen in Fig. 4.6(b). Larger amount of charge is involved during the transition from OFF to ON state for MoS_2 p-MOSFET. The hole V_{AVG} plotted in Fig. 4.7(b) shows that Si, BP, germanane, and silicane p-MOSFETs have higher hole V_{AVG} than the 2D-TMDs p-MOSFETs. The combinations of lower Q_{ON} and higher V_{AVG} in Si, BP, germanane, and silicane p-MOSFETs result in smaller PDP as compared to those of p-MOSFETs based on 2D-TMDs.

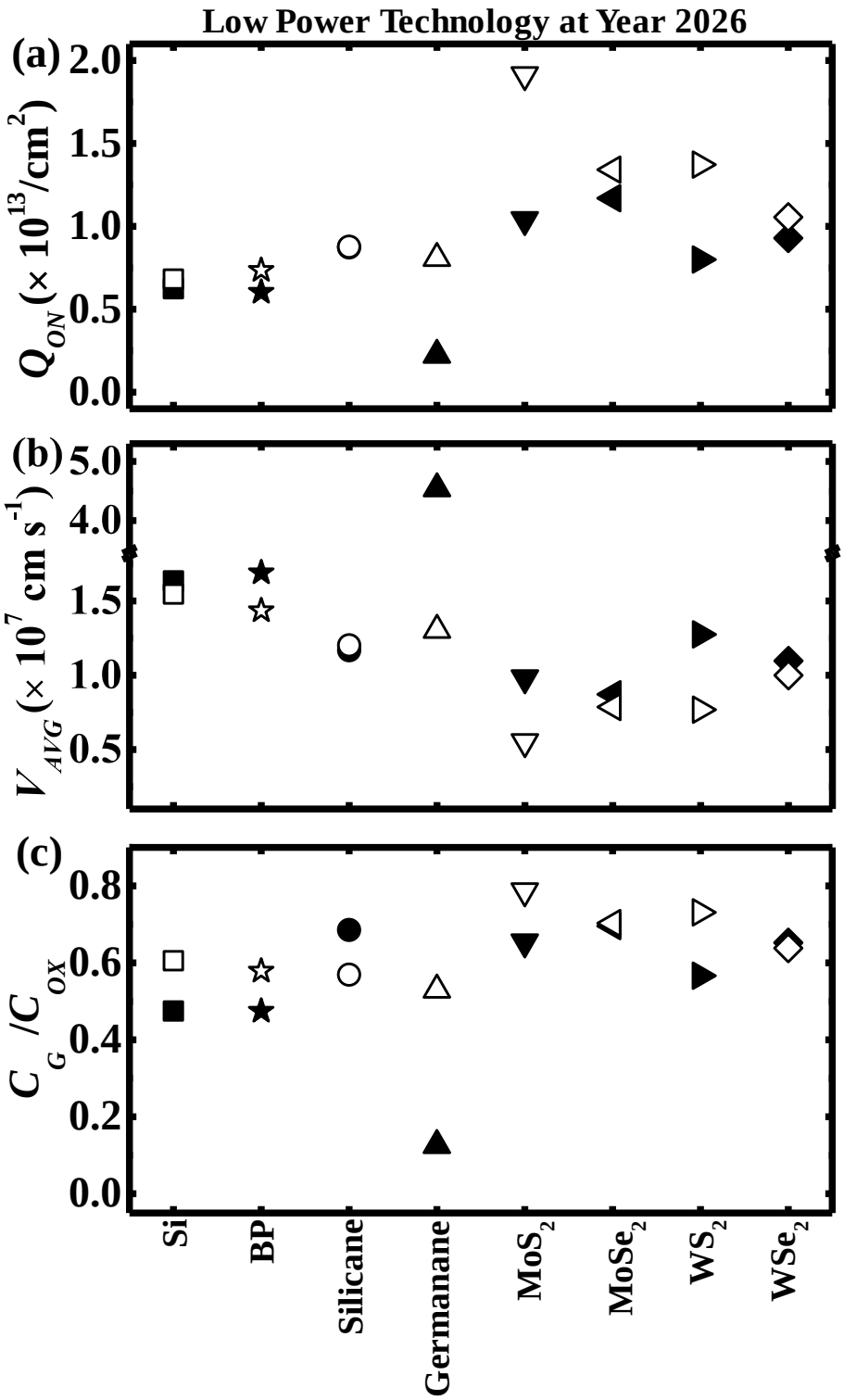

Fig. 4.7. LP technology at year 2026: (a) Carrier density in the channel of n-MOSFET (filled) and p-MOSFET (open) at the ON state. (b) Average carrier velocity of n-MOSFET and p-MOSFET at the ON state. (c) C_G/C_{OX} at the ON state. All n-MOSFETs and p-MOSFETs for LP technology operate at classical regime except for germanane n-MOSFET with its C_G/C_{OX} being smaller than 0.2.

4.3.3 II (c): *Gate Capacitance of n-MOSFET and p-MOSFET*:

Fig. 4.7(c) shows that the C_G/C_{OX} ratio of germanane n-MOSFET is the smallest with a magnitude of less than 0.2. On the other hand, the C_G/C_{OX} ratios of other n-MOSFETs and p-MOSFETs are larger than 0.45, implying that they operate in the classical regime.

Smaller quantum capacitance in germanane n-MOSFET and thinner EOT employed in the highly scaled technology node may cause C_{OX} to be comparable or larger than quantum capacitance. As a result, C_G of germanane n-MOSFET is dominated by the quantum capacitance, leading to the issue of low electron density which limits its I_{ON} in technology nodes with highly scaled EOT. Thus, a larger V_{DD} is required to achieve the benchmark I_{ON} for year 2026 when a smaller *EOT* of 0.45 nm was projected. This also explains the larger degree of I_{ON} reduction in germanane n-MOSFET with technology nodes due to reduction of EOT from year 2018 to 2026, as shown in Fig. 4.3.

4.3.3 (III): Summary of Voltage Scalability and PDP Assessment of MOSFETs for HP and LP Technology of Year 2026:

From the comparison of results for HP and LP device technologies based on the ITRS requirements for year 2026, GaSb and Ge n-MOSFETs offer better voltage scalability with their $V_{DD,min}$ being at least ~10% smaller than that of Si n-MOSFET for HP technology. Ge exhibits the lowest $V_{DD,min}$ and PDP for p-MOSFET. For n-MOSFETs, InAs and $In_{0.3}Ga_{0.7}Sb$ n-MOSFETs offer relatively lower PDP which translates to lower intrinsic power consumption. This is due to smaller amount of channel charge [smaller effective capacitance (C_{eff})] involved in switching the transistor. This leads to smaller intrinsic power consumption ($C_{eff}V^2_{DD}$) in n-

MOSFETs based on InAs and $In_{0.3}Ga_{0.7}Sb$.

For the assessment of LP technology, n-MOSFETs and p-MOSFETs based on Si, BP, and silicane offer relatively better voltage scalability than the rest. Germanane n-MOSFET and MoS_2 p-MOSFET require the largest $V_{DD,min}$ to achieve the benchmark I_{ON}. In terms of PDP, germanane and silicon deliver the lowest value for n-MOSFET and p-MOSFET, respectively.

4.4 Conclusions

Based on the ITRS-projected requirements for year 2018 and beyond, the electrical characteristics of DG-UTB MOSFETs with channel materials from group IV, III-V, and 2D materials along high symmetry transport directions on different surface orientations were exhaustively simulated. For HP technology, GaSb n-MOSFET has the best voltage scalability for n-MOSFET and Ge p-MOSFET offers the best performance for p-MOSFET at fixed I_{ON} and I_{OFF}. Even though n-MOSFETs based on InAs and $In_{0.3}Ga_{0.7}Sb$ require larger V_{DD} to achieve the benchmark I_{ON}, they offer lower PDP due to their lighter effective mass. For the voltage scalability assessment based on ITRS-projected requirements for LP technology, Si, BP, and silicane MOSFETs show better performance than the rest for both n-MOSFET and p-MOSFET. Germanane n-MOSFET has the lowest PDP despite its largest $V_{DD,min}$ due to its smaller electron effective mass at Γ valley. It should be noted that the electrical performance metrics presented in this work include the effect of R_{SD} whose values are different for Si, III-V, and Ge technologies.

Chapter 5

Tunneling Field-Effect Transistor: Device Physics and Design of a L-Shaped Germanium Source Tunneling Transistor

5.1 Introduction

When the complementary-metal-oxide-semiconductor (CMOS) devices are scaled down to the nanometer regime, the non-scalability of the subthreshold swing in the conventional metal-oxide-semiconductor field-effect transistors (MOSFETs) causes high leakage current at reduced power supply voltage (V_{DD}), increasing the static power in integrated circuits (ICs). To circumvent this problem, transistor with a steeper switching characteristic is required in order to maintain a high ON-state current (I_{ON}) at a reasonably low OFF-state current (I_{OFF}) with downscaling of V_{DD}.

In this Chapter, tunneling field-effect transistor (TFET) is explored as a steep-slope transistor to overcome the fundamental limit of subthreshold swing (60 mV/decade at room temperature) in a conventional MOSFET. A novel TFET structure with an L-shaped source for increased vertical tunneling region beneath the channel is proposed. An insulator (SiO_2) is positioned between the source and drain to eliminate leakage paths and to reduce I_{OFF}. Extensive simulations are carried out to study the effects of overlap length between the source and the gate stack (L_{OV}) and silicon thickness (T_{Si}) on the I_{ON} and subthreshold swing (S) of the TFET design investigated. In addition, the physics and device design of this novel structure are explored in detail.

This Chapter is organized as follows: In section 5.2, the device structure, methodology, and design of L-shaped Ge source TFET are discussed. Section 5.3 covers the results and discussions of L-shaped Ge source TFET. The design guidelines of L-shaped Ge source TEFT are recapped in Section 5.4. Section 5.5 summarizes the key points of this chapter.

5.2 Proposed Structure and Simulation Approach

5.2.1 Device structure and design

The hetero-junction structure has been widely used to further improve the ON-state current of TFETs [74], [91]-[97]. Instead of using a conventional lateral P^+ – Intrinsic – N^+ (PIN) structure comprising a single semiconductor material, a P^+ Ge – P^- Si – N^+ Si hetero-structure is investigated here. The Ge-Si hetero-junction is incorporated beneath the Si channel as well, as shown in Fig. 5.1. By extending the P^+ Ge source towards the drain and under the P^- Si channel [Figs. 5.1(a) and 5.1(b)], forming an L-shaped P^+ Ge source region, an additional horizontal hetero-junction is introduced so that carriers tunnel vertically from the valence band of the Ge Source towards the conduction band of Si near the interface between the Si channel and the gate dielectric. Therefore, the device structures of Figs. 5.1(a) and 5.1(b) are called L-shaped Ge source TFETs. An L-shaped Ge source TFET has both horizontal and vertical Ge-Si hetero-junctions. Thus, the ON-state current can be boosted owing to the additional tunneling current component (in the vertical direction) that arises from the existence of the horizontal hetero-junction or source-channel junction.

In Fig. 5.1(b), an insulating material SiO_2 is inserted between the L-shaped Ge source and the drain region to suppress leakage paths between the drain and the

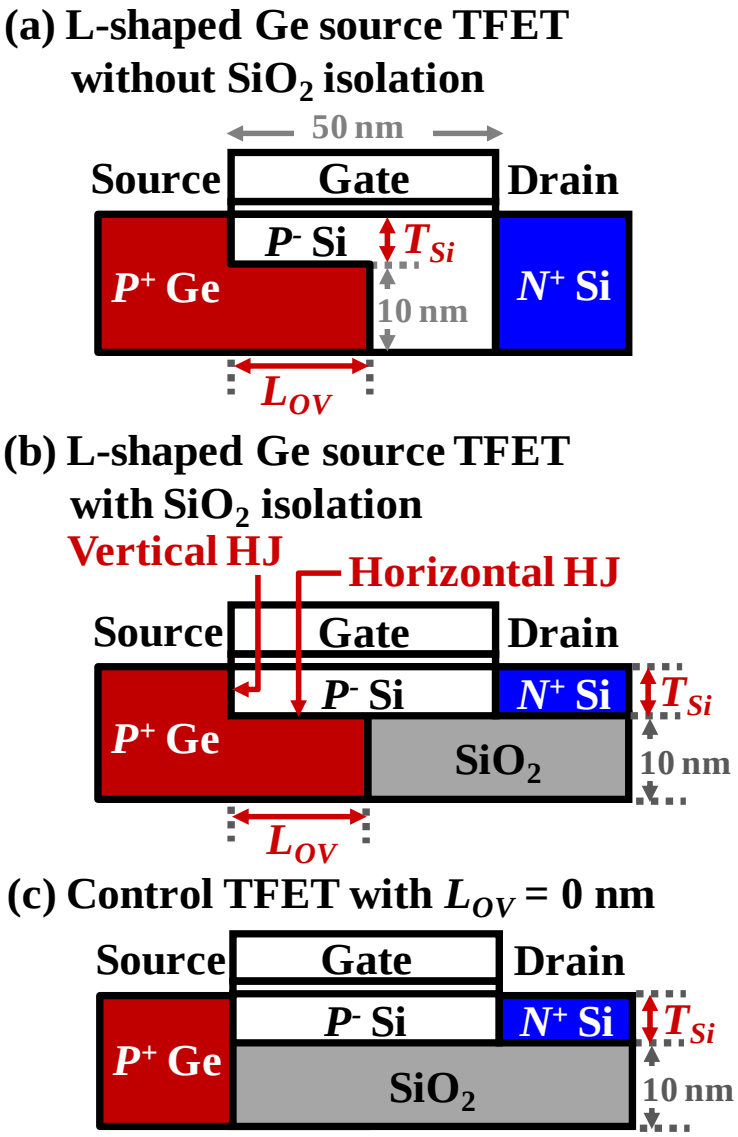

Fig. 5.1. Schematic of TFET with L-shaped P^+ Ge source and P^- Si channel (a) without SiO_2 isolation between source and drain, and (b) with SiO_2 isolation between source and drain. (c) a special case of the L-shaped Ge source TFET structure where L_{OV} = 0 nm. In all structures here, the gate stack comprises a gate electrode with L_G = 50 nm formed on a gate dielectric with an Equivalent Oxide Thickness (EOT) of 0.8 nm.

extended source. The SiO_2 material serves as a current block in the region where the source-to-drain distance is very small, thus suppressing the leakage tunneling current that would otherwise flow from the extended source to drain side. Any insulating material other than SiO_2 could also work as a current block. Fig. 5.2 compares the gate transfer characteristics of structures with [Fig. 5.1(b)] and without the SiO_2

isolation [Fig. 5.1(a)] between the source and drain. The L_{OV} for both structures is 30 nm. Without the SiO_2 isolation, the leakage current at V_{GS} = 0 V and V_{DS} = 0.4 V is ~10^{-8} mA/μm. Inserting the SiO_2 isolation brings the leakage current down by an appreciable 3.4 orders of magnitude, as compared to a device without SiO_2 isolation.

With the SiO_2 isolation structure, TFETs with a given gate length L_G can be designed with a larger L_{OV} to achieve a higher I_{ON} without raising the OFF-state leakage current substantially. Experimentally, the structure of Fig. 5.1(b) can be realized and fabricated on an ultra-thin Si-on-insulator (UT-SOI) wafer. The ultra-thin Si and buried oxide layers in the source regions can be etched away, with an undercut of the buried oxide, followed by an epitaxial growth of P^+ Ge underneath the Si layer and adjacent to the buried oxide. The buried oxide next to the Ge source separates it from the drain.

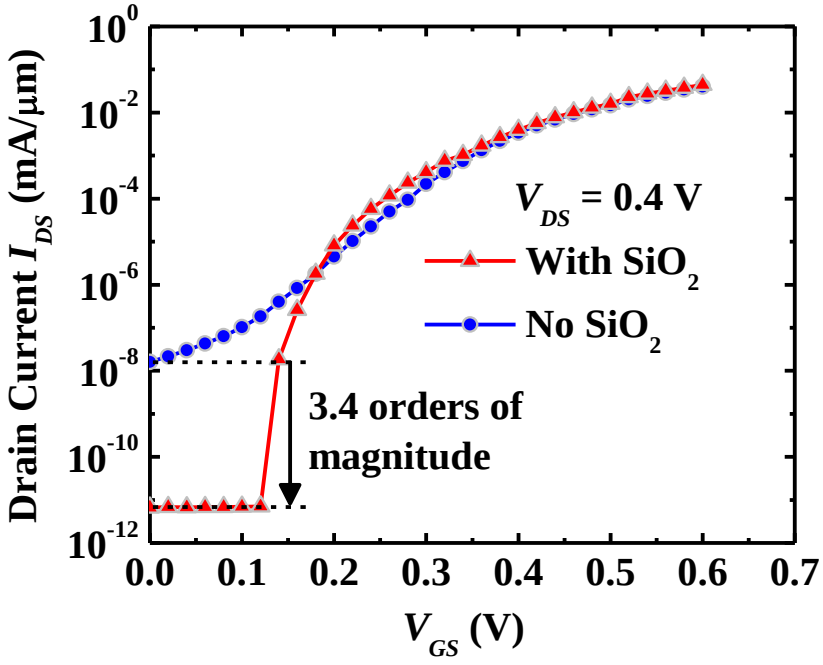

Fig. 5.2. Gate transfer characteristics obtained at V_{DS} = 0.4 V for the TFET designs in Figs. 5.1(a) and 5.1(b). In both device structures, the overlap of the P^+ Ge source under the gate L_{OV} and the Si body thickness T_{Si} are 30 and 5 nm, respectively. The TFET design of Fig. 5.1(a) has a high I_{OFF} of ~10^{-8} mA/μm due to source-to-drain leakage. The I_{OFF} is effectively suppressed with the insertion of an insulating material between the source and the drain which keeps the I_{OFF} below ~10^{-11} mA/μm.

5.2.2 Methodology and Device Parameters

A two-dimensional (2D) technology computer-aided design (TCAD) simulator with a physics based non-local BTBT algorithm was developed and used for this simulation [200]-[201]. The simulator employs a non-local algorithm for accurate calculation of the band-to-band tunneling current. The algorithm captures the essential physics of multi-dimensional tunneling in a 2D structure, and is designed to be robust and independent of mesh grids. The algorithm is able to intelligently search for all the possible tunneling paths. The first step is to search for the E_0 and E_{max} which defines the lower and upper limit of the energy range. For each bias point, E_0 is determined by the minimum energy of the conduction band E_c while E_{max} is the maximum energy of the valence band (E_v). The defined energy range is subsequently discretized. For each energy level E_m, the tunnelling paths between the nodes at 2-D surface of conduction band (E_c) and valence band (E_v) are identified and mapped into the tunnelling node-pairs [Fig. 5.3].

The corresponding BTBT generation rate (G_{BTBT}) of each node-pair is calculated and considered into the continuity equations. The tunnelling probability is calculated and considered into the continuity equations. The tunnelling probability is

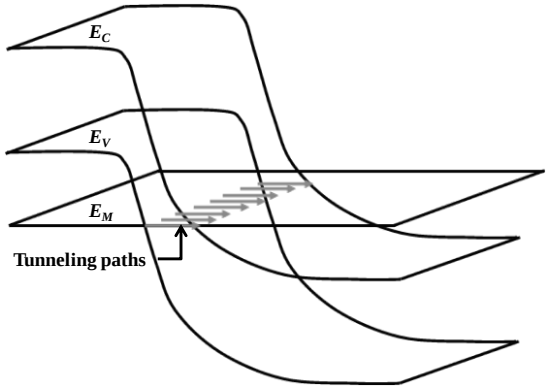

Fig. 5.3. 2-D energy surface of E_c and E_v. E_m is the m-th energy level. The tunnelling node-pairs are identified by searching for all the probable tunnelling paths from nodes at the surface of E_v to E_c.

calculated by the Wentzel-Kramers-Brillouin (WKB) method:

$$T(E) = \exp\left[-2\int_{E_c}^{E_v} \frac{\sqrt{2m_r^*\left(U(r)-E\right)}}{\hbar}.dr \right], \qquad (5.1)$$

where m_r^* is the tunneling reduced mass and $U(r)$-E is the barrier height at position r. m_r^* of Ge used is $0.02m_0$ which was fitted from experimental Ge tunneling diode [202]. BTBT generation rate (G_{BTBT}) is related to tunneling possibility and electron and hole concentrations at both starting node and ending node by:

$$G_{BTBT} = \int_{E_{\min}}^{E_{\max}} \frac{4\pi q m_{DOS}^* kT}{h^3} \frac{n_c p_v - n_i^2}{(n_c + n_i)(p_v + n_i)}.W.T(E).dE, \qquad (5.2)$$

where q is elementary charge, m_{DOS}^* is electron density-of-state effective mass, k is Boltzmann constant, T is temperature in Kelvin, n_c is the electron concentration at the ending node at E_c. p_v is the hole concentration at the starting node of tunneling at E_v, n_i is the intrinsic carrier concentration, and W is the width of a tunnel path.

The basic TFET structure studied in this work comprises a single-gated Si body TFET with an L-shaped Ge source, as shown schematically in Fig. 5.1(b). The key device design parameters are the overlap between the source and the gate stack L_{OV}, and the thickness of the Si body T_{Si}. The simulations were performed on 5 different T_{Si} values, ranging from 5 to 10 nm (5, 6, 7, 8, and 10 nm). For each T_{Si}, the effect of L_{OV} on the electrical characteristics was simulated by varying L_{OV} from 0 to 30 nm with a step size of 10 nm. The control TFET has a L_{OV} of 0 nm (Fig. 5.1(c)). In all devices simulated, a gate length of 50 nm and an Equivalent Oxide Thickness (EOT) of 0.8 nm were used. The P^+ source doping is 10^{20} cm^{-3} while the N^+ drain doping is 10^{19} cm^{-3}. The channel has a p-type concentration of 10^{16} cm^{-3}. All source, channel, and drain have a doping gradient of 0.5 nm/decade. All the model parameters

used in the simulations are corresponding to and calculated at room temperature.

I_{ON} is extracted at V_{DS} = 0.4 V and $V_{GS} - V_{OFF}$ = 0.4 V. V_{OFF} is defined to be the gate voltage at which $I_{DS} = 10^{-10}$ mA/μm. S is the average subthreshold swing obtained from the I_{DS}-V_{GS} curve for I_{DS} in the range of 10^{-9} to 10^{-4} mA/μm. The initial tunneling voltage V_{INT} is defined to be the gate voltage at which $I_{DS} = 10^{-9}$ mA/μm.

5.3 Results and Discussions

5.3.1 Impact of T_{Si} and L_{OV} on ON-state current:

The impact of L_{OV} on I_{ON} for various T_{Si} is illustrated in Fig. 5.4. It is observed that I_{ON} decreases with increasing T_{Si} for L_{OV} greater than 0 nm. This is due to a reduction of the vertical field and an increase in the vertical tunneling distance when T_{Si} is increased [203].

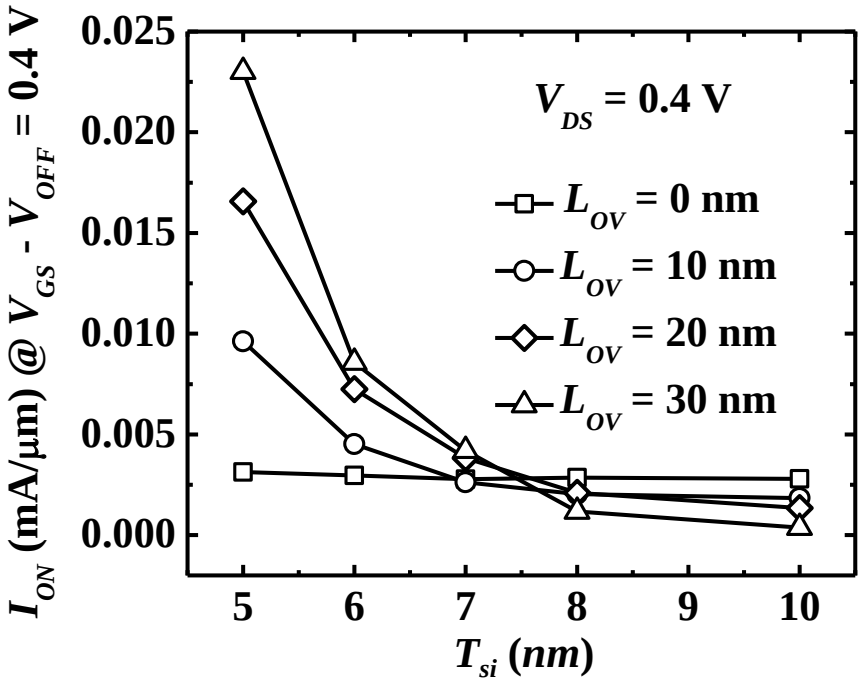

Fig. 5.4. I_{ON}-T_{Si} for L_{OV} = 10, 20, and 30 nm. I_{ON} is a strong function of L_{OV} at small T_{Si}.

Thus, the BTBT generation rate along the horizontal hetero-junction of the device with thicker T_{Si} of 10 nm is about 2 orders of magnitude lower than that in the device with thinner body (Fig. 5.5). The ON-state tunneling barrier width extracted along the vertical direction (A – A') at L_{OV} = 30 nm for T_{si} = 5 nm and T_{si} = 10 nm shows that the tunneling width is larger for a thicker T_{Si} (Fig. 5.6).

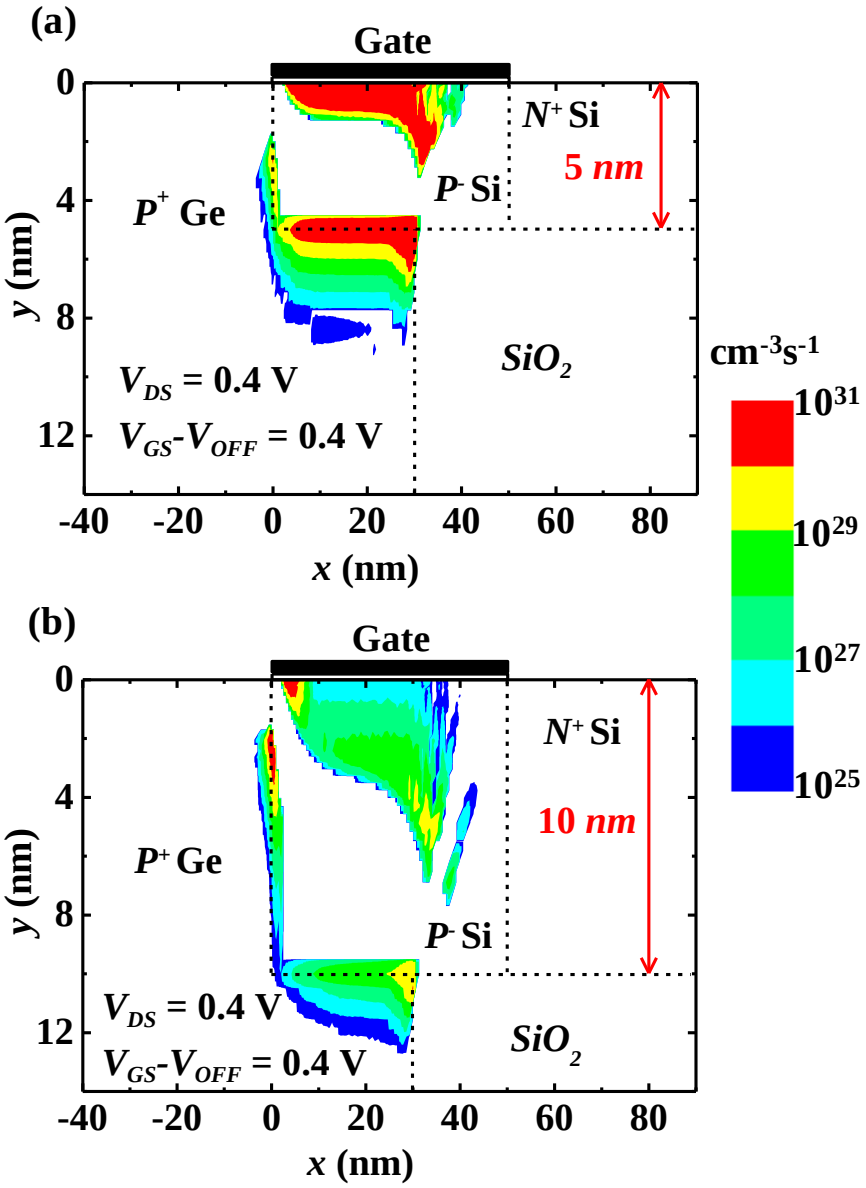

Fig. 5.5. BTBT Generation rate contour of device with L_{OV} = 30 nm for (a) T_{Si} = 5 nm, and (b) T_{Si} = 10 nm. Higher BTBT rate in 5 nm Si-body device is due to better gate electrostatic control over the vertical tunneling junction.

In addition, the vertical band bending for larger T_{Si} [Fig. 5.6(b)] is more moderate which can be translated as larger tunneling barrier width or lower electric field along the vertical direction. Since the tunneling rate is exponentially dependent on the electric field and the tunneling width [204], lower I_{ON} is observed for the case where T_{Si} = 10 nm as compared to T_{Si} = 5 nm.

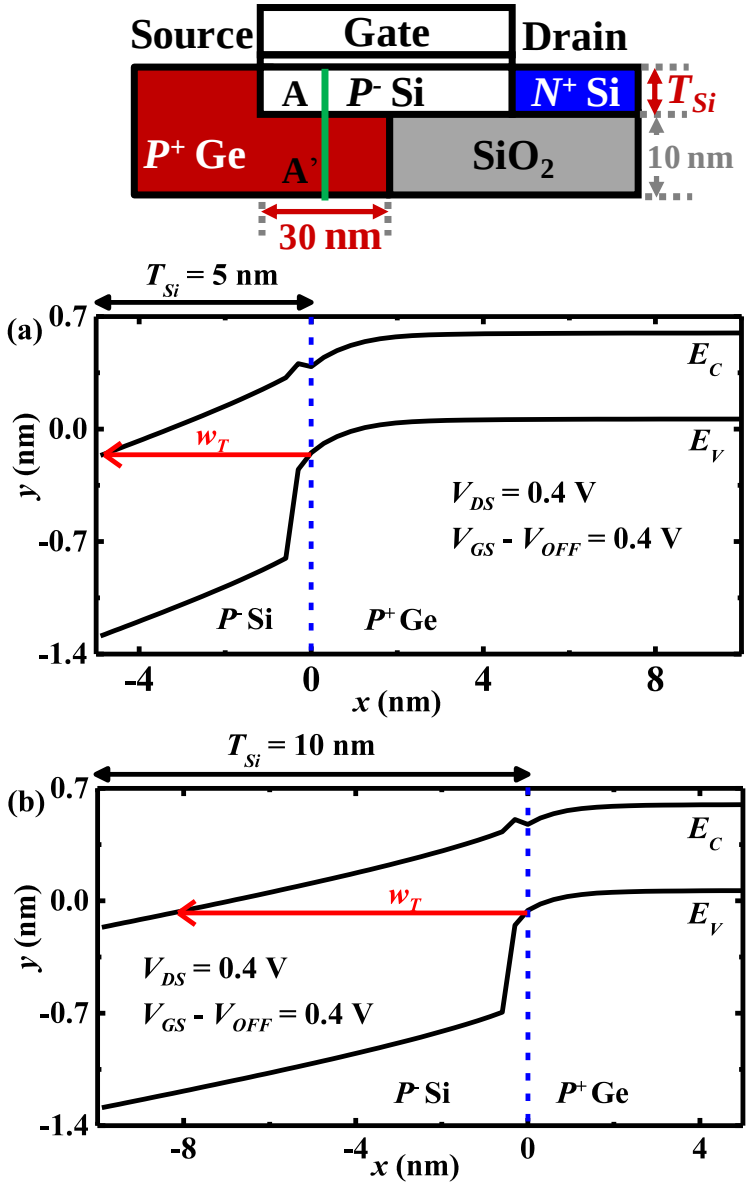

Fig. 5.6. The ON-state tunneling barrier width extracted along the vertical direction (A – A') at L_{OV} = 30 nm for (a) T_{Si} = 5 nm and (b) T_{Si} = 10 nm shows larger tunneling width for thicker T_{Si}.

For the control device with L_{OV} = 0 nm, I_{ON} appears to be almost independent of T_{Si} (Fig. 5.4). This is due to the fact that the drain current of the control device is dominated by lateral tunneling, and the tunneling current density peaks around the region adjacent to the Si channel surface. The tunneling current density decreases exponentially away from the Si channel surface. As I_{ON} of control device is mainly contributed by lateral tunneling near the Si channel interface, it is not substantially affected by the increasingly thicker T_{Si}. However, when T_{Si} is reduced to less than 5nm, additional quantum effects come into play, e.g. carrier quantization in the vertical direction. The dependence of I_{ON} on T_{Si} for the case when T_{Si} is less than 5 nm is not studied in this work.

Fig 5.7 (a) shows the simulated gate transfer characteristics for TFETs with T_{Si} of 5 nm and L_{OV} of 0, 10, and 30 nm. As illustrated in Fig. 5.7(b), at a fixed I_{OFF}, I_{ON} is ~7 times higher for the TFET with L_{OV} = 30 nm compared to that of a TFET with L_{OV} = 0 nm. The OFF-state current of TFETs with T_{Si} = 5 nm is below 1×10^{-11} mA/μm for different L_{OV}, and it is comparable to the OFF-state current of the control device. Another observation from Fig. 5.7(a) is that TFETs with L_{OV} larger than 0 nm have higher V_{INT} compared to the control device. This is due to the increase in the lateral tunneling width with the increasing L_{OV}, as illustrated by the 1-D band diagram extracted along the source-to-drain direction in Fig. 5.8.

Fig. 5.8 compares the band diagram along the source-to-drain direction, for the control TFET (L_{OV} = 0 nm) and TFET with L_{OV} = 30 nm in the OFF-state and under bias condition of V_{DS} = 0.4 V and V_{GS} = 0.18 V. The existence of the overlap region increases the tunneling barrier width in the lateral direction [Fig. 5.8(b)]. Hence, a higher gate voltage is needed to reduce the tunneling width in order to initiate the lateral tunneling. Fig. 5.9 shows the trend of increased lateral tunneling width with

increasing L_{OV}. By extending Ge source beneath the Si channel region, it modifies the potential distribution at the source and channel interface such that the lateral electric field near the vertical hetero-junction is lower, leading to a reduction in the lateral tunneling rate.

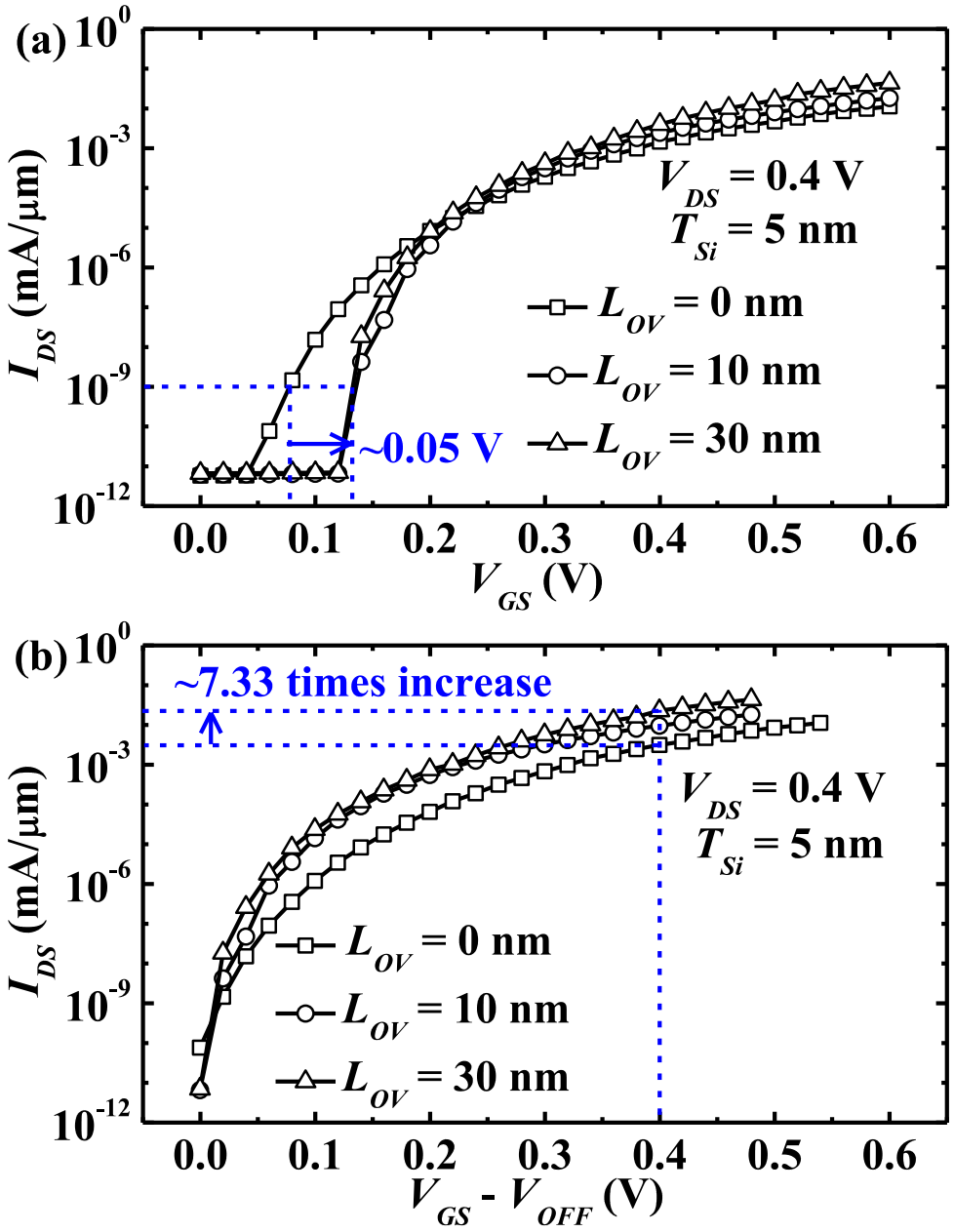

Fig. 5.7. (a) I_{DS}-V_{GS} and (b) I_{DS}-$(V_{GS}–V_{OFF})$ of TFET with various L_{OV} and T_{Si} = 5 nm. By increasing L_{OV} from 0 to 30 nm, S is improved by 13 mV/decade, I_{ON} is enhanced by 7.3 times, and V_{INT} is also higher by 50m V.

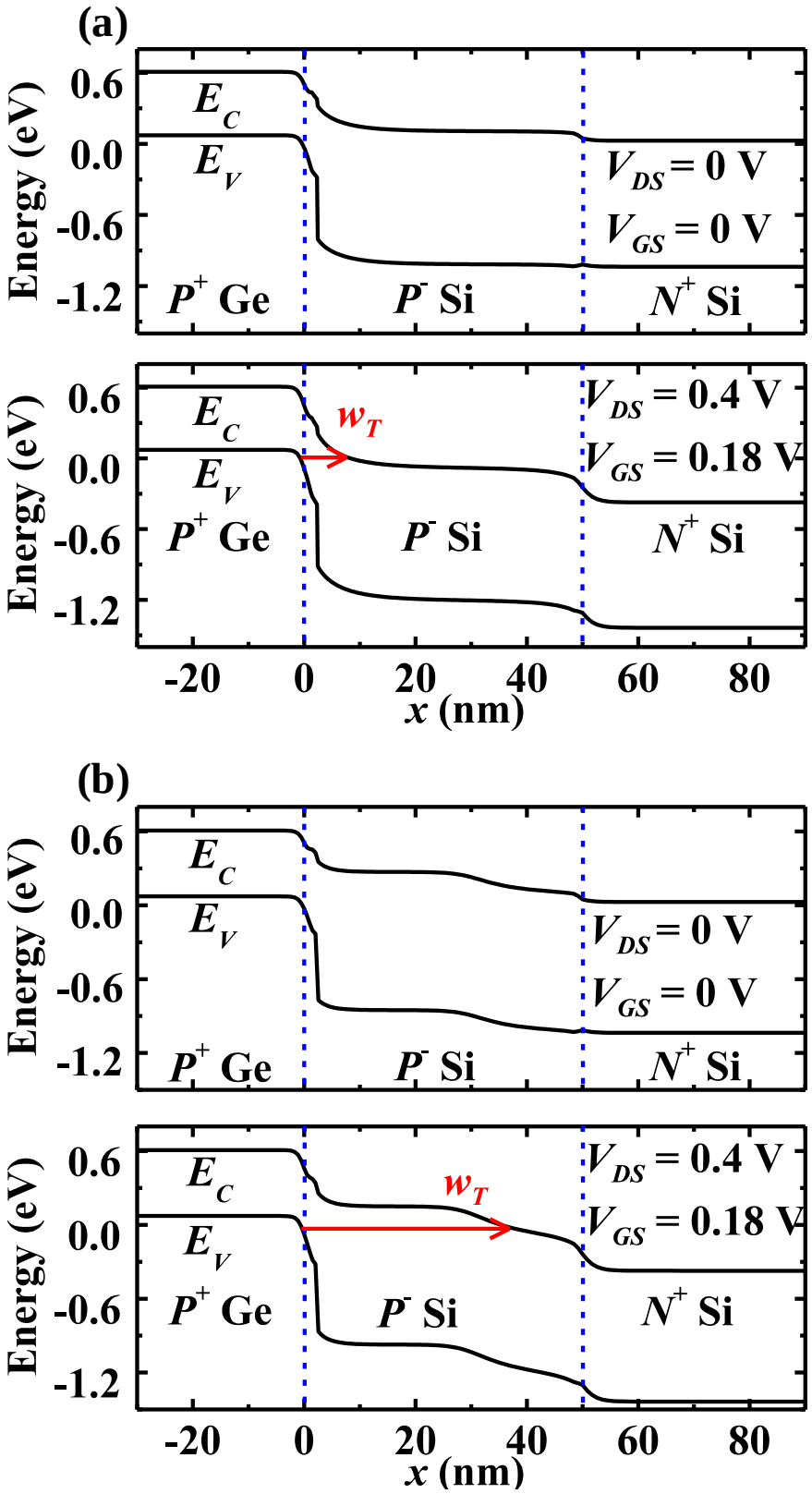

Fig. 5.8. Energy band diagram along source-to-drain of device with T_{Si} = 5 nm for (a) L_{OV} = 0 nm, and (b) L_{OV} = 30 nm in OFF-state and biased at V_{DS} = 0.4 v and V_{GS} = 0.18 V. The introduction of the overlap region in (b) increases the lateral tunneling barrier width encountered by the valence electrons in the source region.

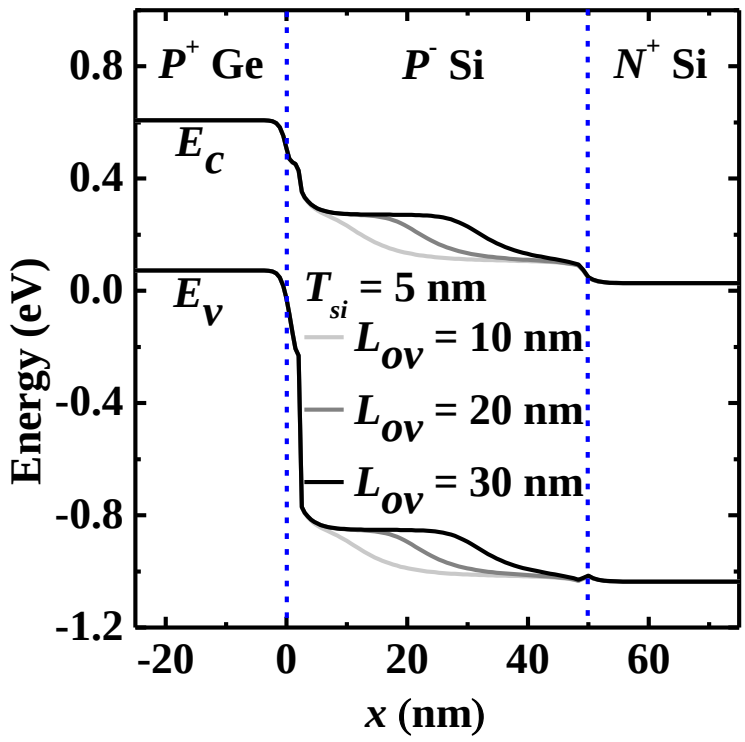

Fig. 5.9. Energy band diagram along source-to-drain of device with T_{Si} = 5 nm in OFF-state for L_{OV} = 10, 20, and 30 nm. The trend of increased lateral tunneling width, W_T, with increasing L_{OV} is observed.

The higher I_{ON} for larger L_{OV} in Fig. 5.7(b) can be explained by the larger tunneling area resulting from the larger hetero-tunneling junction with the increment of L_{OV}. This is further confirmed from the BTBT generation rate contours for devices with L_{OV} = 0 nm and L_{OV} = 30 nm (Fig. 5.10). Under the same gate drive condition, more areas with high generation rates are observed in a device with L_{OV} = 30 nm, as compared to that of a control device.

To verify that the dominant tunneling is in the vertical direction for thinner T_{Si} and larger L_{OV} structure, a 3-dimensional (3D) surface plot of energy bands (E_C and E_V) with superimposed tunneling paths at allowed energy levels is shown in Fig. 5.11. The direction of the tunneling paths validates that vertical tunneling is indeed the dominant current component for the device with T_{Si} = 5 nm and L_{OV} = 30 nm.

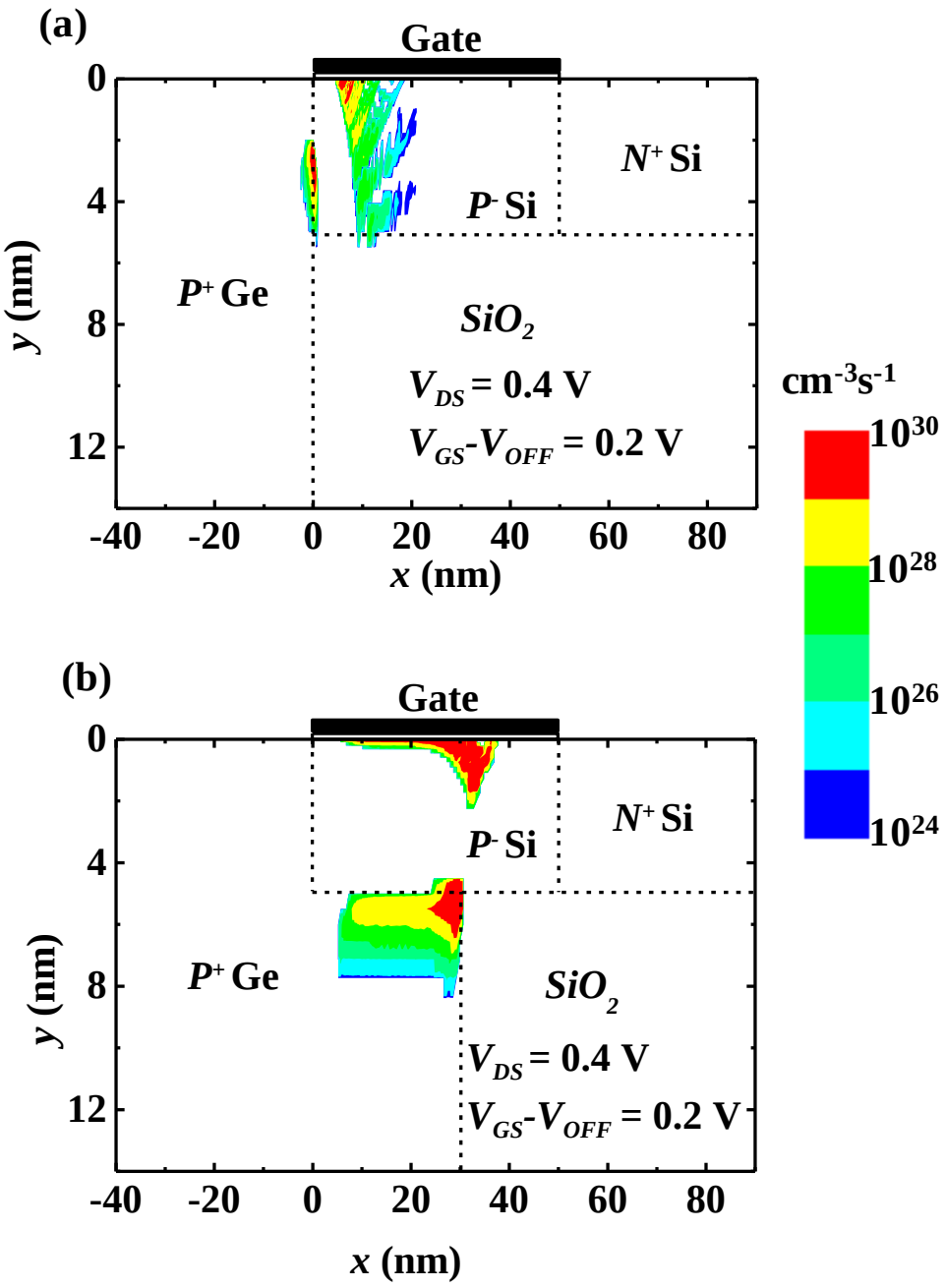

Fig. 5.10. BTBT Generation rate contour of device with T_{Si} = 5 nm for (a) L_{OV} = 0 nm, and (b) L_{OV} = 30 nm. The better uniformity of BTBT rate distribution over the overlap region shown in (b) results in a concerted electron tunneling in the vertical direction at a certain V_G, giving rise to steeper *S*.

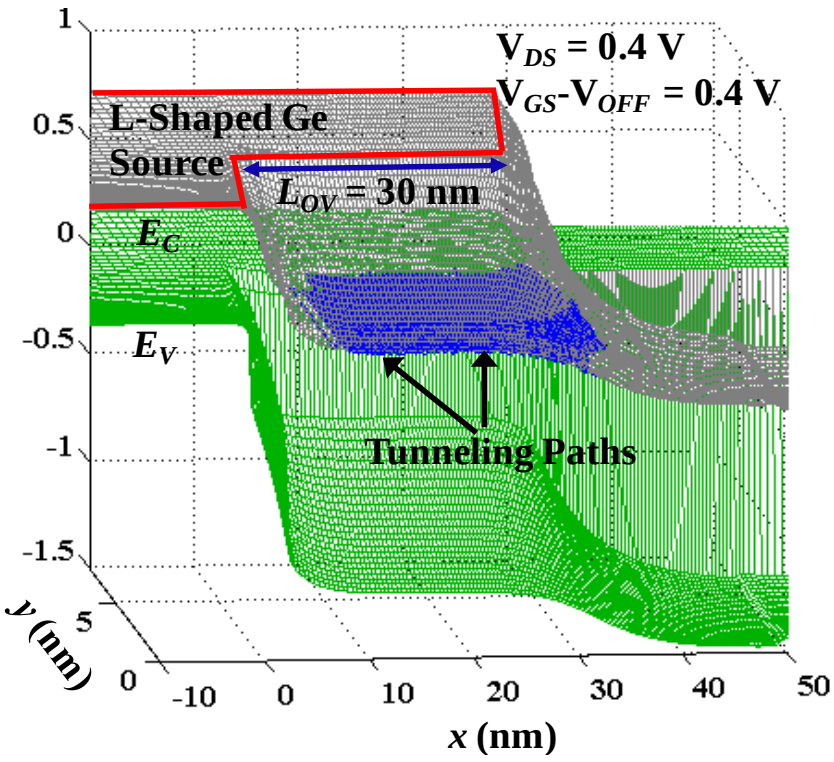

Fig. 5.11. 3D surface plot of energy band (E_C and E_V) with superimposed tunneling paths at allowed energy levels as extracted from simulation confirms that vertical tunneling indeed is the dominant current component for the device with T_{Si} = 5 nm and L_{OV} = 30 nm.

5.3.2 Impact of T_{Si} and L_{OV} on subthreshold swing S:

Fig. 5.12 illustrates the impact of L_{OV} on S for various T_{Si}. The subthreshold region of the I_{DS}-V_{GS} plot of TFETs with L_{OV} larger than 0 nm becomes steeper relative to the control device as T_{Si} is reduced below 8 nm. This is contributed by two factors. First, vertical tunneling is the dominant current component. Second, the vertical tunneling density along the horizontal hetero-junction is almost conformal or uniform. The electrostatic potential induced by the gate is more uniformly distributed along the horizontal hetero-junction located just beneath the Si channel region. As such, uniform tunneling with exponential increment in the vertical tunneling current density along the horizontal hetero-junction would give rise to steeper subthreshold

characteristics. This is in contrast with a vertical hetero-junction with non-uniform and decreasing tunneling current density with increasing depth from the channel surface. With lateral tunneling, the total current does not increase as abruptly with increase in V_G, as compared with vertical tunneling. Thus, for achieving a steeper *S*, a larger L_{OV} is preferred so that vertical tunneling dominates over lateral tunneling.

This is evident in Fig. 5.7 which shows improved *S* with progressively larger L_{OV} for T_{Si} = 5 nm. At T_{Si} of 5 nm, *S* improves from 40 to 27 mV/decade when L_{OV} increases from 0 to 30 nm. The improved *S* for larger L_{OV} in Fig. 5.7(b) is attributed to the dominant vertical tunneling mechanism. By increasing L_{OV} for the structure with T_{Si} = 5 nm, the onset voltage of the lateral tunneling is higher than that of vertical tunneling. Lower onset voltage of the vertical tunneling component makes it the dominant tunneling mechanism in the subthreshold regime. A more uniform BTBT rate distributed along the horizontal hetero-junction leads to initiation of tunneling from the Ge-Source to Si-body at a similar V_G in the tunneling region, resulting in a steeper *S*. This is verified by the better uniformity of BTBT rate contour for the device with L_{OV} = 30 nm compared to the control device at T_{Si} = 5 nm (Fig. 5.10).

5.4 Design guidelines for optimal L-shaped Ge source TFETs:

For device with L_G = 50 nm, higher I_{ON} and steeper *S* are achieved for devices with T_{Si} smaller than 8 nm and L_{OV} greater than 10 nm. When T_{Si} is greater than 8 nm, the effect of vertical tunneling is suppressed, due to weaker electrostatic control of the gate over the channel region (Fig. 5.5). Increasing the extended Ge Source L_{OV}

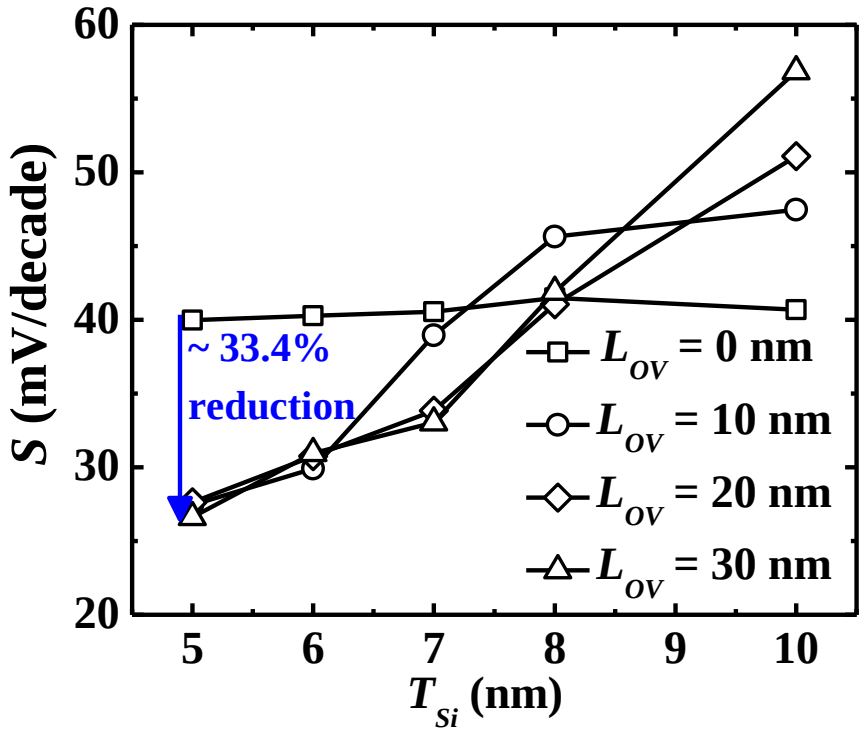

Fig. 5.12. *S*-T_{Si} for L_{OV} = 10, 20, and 30 nm. 33% reduction in *S* is obtained for T_{Si} = 5 nm when increasing L_{OV} from 0 to 30 nm.

underneath the Si channel makes the lateral tunneling less dominant and reduces the effect of lateral tunneling (Fig. 5.9).

For higher I_{ON} and steeper *S*, T_{Si} smaller than 8 nm and L_{OV} greater 10 nm should be adopted in L-shaped Ge source TFET. The separation of the extended L-shaped Ge source from the drain side by a layer of SiO_2 insulator allows L_{OV} to be extended more to the channel region to increase the area of vertical tunneling for I_{ON} improvement.

The EOT may affect the performance of the TFET via the modulation of the gate control over the channel region. The effect of EOT on TFET with the tunneling junction aligned with the gate electric field has been studied by Y. Lu *et al*. [205]. Y. Lu *et al*. reported that a smaller EOT provides stronger coupling between the gate and the channel, and thus higher ON-state current and steeper subthreshold swing can be

obtained. To further enhance the tunneling in-line with the gate field in the proposed structure, a smaller EOT should be employed in order to increase the gate control over the horizontal heterojunction, as shown in Fig. 5.1(b).

5.5 Conclusions

A novel TFET with L-shaped Ge source is investigated. The device physics and design are studied in detail through 2-D TCAD simulation. It is found that the source overlap region underneath the channel region improves I_{ON} and S of an L-shaped Ge source TFET with thinner T_{Si} and larger L_{OV}. Steeper S can be attributed to the more dominant and uniform vertical tunneling from the horizontal hetero-junction Ge source to the Si channel. In order to achieve this, the Si channel needs to be thin enough for more effective gate-to-channel coupling. Higher ON-state current is due to the increase in the tunneling area from the additional horizontal hetero-junction introduced by the extended Ge source underneath the Si region. The insertion of an insulator between the extended Ge source and drain allows a longer horizontal hetero-junction for achieving a higher I_{ON} without raising the leakage current. Thus, I_{ON} is scalable with L_{OV}. This alleviates the I_{ON} limitation and scalability issue faced by lateral TFET designs.

Chapter 6

Conclusion and Future Directions

6.1 Conclusion

Scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) according to the Moore's Law [1] has led to the continued improvement in both speed and density of devices in integrated circuits of complementary-metal-oxide-semiconductor (CMOS) technology. However, power density also increases with increased circuit density. Hence, power consumption has become a critical problem which ultimately hinders the progress of CMOS technology. One method to reduce the power consumption is to scale down the power supply voltage (V_{DD}) since power consumption is strongly dependent on the V_{DD}. Nevertheless, the reduction of V_{DD} should not compromise the ON-state current (I_{ON}) to ensure fast switching speed of CMOS circuits.

To address this issue, channel materials with high product of injection velocity and density of states (DOS) can be potentially used in MOSFETs in order to deliver higher I_{ON} at reduced V_{DD}. Another approach is to use transistors with steep switching characteristic such as tunneling field-effect transistors (TFETs). This thesis focuses on the exploration of MOSFETs based on alternative channel materials and tunneling field-effect transistor to achieve V_{DD} reduction for advanced technology nodes.

The first objective of this thesis is to explore various alternative channel materials with high product of injection velocity and density of states for MOSFETs operating at low V_{DD}. Amongst the potential channel materials considered in this work

comprise germanium-tin and 2-dimensional (2D) materials (silicane, germanane, MoS_2, $MoSe_2$, WS_2, and WSe_2). The second objective is on the investigation of novel structure for achieving high I_{ON} and steep switching behavior in TFETs. A novel device structure for TFET with heterojunction consisting of Ge and Si was proposed and analyzed theoretically.

The contributions of this thesis are listed in section 6.2. Finally, possible future directions and work for expanding on the research in this thesis are provided in Section 6.3.

6.2 Contribution of This Thesis

6.2.1 Theoretical Study of the Electronic Properties of GeSn Alloy as Channel Material for MOSFETs

The empirical pseudopotential method (EPM) was adopted for calculating the band structures of bulk $Ge_{1-x}Sn_x$ alloys for Sn composition varying from 5% to 20%. The electron and hole effective masses were extracted along various high symmetry directions on common crystal planes. With increasing Sn composition, the extracted $Ge_{1-x}Sn_x$ effective masses show a decreasing trend for light-hole valence band, conduction band at Γ valley and conduction band at L valley along transverse direction. The effective masses of heavy hole and conduction band at L valley along longitudinal direction are observed to be independent of Sn composition. The light hole (LH) and heavy hole (HH) effective masses show anisotropic trend for plane orientations of (100) and (110). For electron effective mass, an isotropic characteristic is observed for all three plane orientations investigated. In addition, the Luttinger-like parameters of 8-band k.p model were derived by fitting the energy dispersion in the

vicinity of the Γ valley to that by EPM. These effective masses and derived effective mass parameters of 8- band k.p method may be useful for the optical and electronic device designs employing $Ge_{1-x}Sn_x$ alloys. The assessment of ballistic I_{ON} of double-gate ultra-thin body (DG-UTB) n-channel metal-oxide-semiconductor field-effect transistor (n-MOSFET) based on GeSn alloy reveals that marginal enhancement in I_{ON} can be achieved in GeSn UTB n-MOSFET than that of Ge n-MOSFET. For GeSn n-MOSFET with thinner body, the involvement of Γ valley in the transport becomes insignificant. Under strong quantum confinement, light confinement effective mass of Γ valley causes the subband at Γ valley to be raised far above from the transport energy window. Therefore, GeSn n-MOSFET does not benefit from the reduction of effective mass at Γ valley with increasing Sn composition. The I_{ON} improvement in GeSn UTB n-MOSFET is more pronounced when a thicker body is employed since both Γ and L valley contribute to the transport.

6.2.2 Ballistic Transport Performance of Group IV 2D Materials: Silicane and Germanane MOSFETs

The electronic properties and the ballistic I_{ON} of hydrogenated silicene and germanene, i.e., silicane and germanane, respectively, were examined. Our results show that I_{ON} of silicane n-channel transistor with reasonable electron DOS and velocity is higher than those of the n-channel transistors made of other 2D materials studied (Germanane, MoS_2, $MoSe_2$, WS_2, and WSe_2) for the same I_{OFF} of 5 nA/μm. Germanane n-MOSFET with relatively lower electron effective mass operates at the quantum capacitance regime, especially at the highly scaled technology nodes. Thus, the I_{ON} of germanane n-MOSFET is less sensitive to the equivalent oxide thickness

(EOT) for advanced technology nodes. Both germanane and silicane p-channel metal-oxide-semiconductor field-effect transistors (p-MOSFETs) deliver higher I_{ON} than the 2-dimensional transition metal dichalcogenides (2D-TMDs) p-MOSFETs. Silicane MOSFET satisfies the I_{ON} requirement of high performance (HP) and low operating power (LOP) technology for years 2018–2026. Germanane MOSFET satisfies the I_{ON} requirement of HP and LOP logic transistors, except its n-MOSFET for the I_{ON} requirement of HP logic transistors for the production year of 2026.

6.2.3 Voltage Scalability of Ultra-Thin Body MOSFETs based on Group IV, III-V, and 2-Dimensional Materials

Based on the International Technology Roadmap for Semiconductors (ITRS) projected device specifications for high performance (HP) and low power (LP) technologies for year 2018 and beyond, the I_{ON} of DG-UTB MOSFETs with channel materials from group IV, III-V, and 2D materials were exhaustively simulated along high symmetry transport directions on different surface orientations. For the voltage scalability assessment based on the specifications of HP technology, GaSb n-MOSFET and Ge p-MOSFET offer the best voltage scalability for n-type and p-type MOSFET, respectively at the benchmarked I_{ON}. Although higher V_{DD} is required by n-MOSFETs based on InAs and $In_{0.3}Ga_{0.7}Sb$ to achieve the benchmark I_{ON}, they offer low power delay product (PDP) due to their light effective mass. For the voltage scalability assessment based on ITRS-projected requirements for LP Technology, Si, BP, and silicane MOSFETs have better voltage scalability and lower PDP than the MOSFETs based on 2D-TMDs and germanane for both n and p type MOSFETs.

6.2.4 Design and Physics of L-shaped Germanium Source Tunneling Transistor

A novel TFET with L-shaped Ge source was proposed and studied. The device physics and design were analyzed in detail via a means of 2D TCAD simulations. By extending the source overlap region underneath the channel region (L_{OV}) and employing a thinner silicon body, a significant improvement in I_{ON} and lower subthreshold swing (S) are achieved in the L-shaped Ge source TFET compared to the control device without the L_{OV}. Steeper S can be attributed to the more dominant and uniform vertical tunneling from the horizontal heterojunction Ge source to the Si channel. In order to ensure the efficiency of the vertical tunneling, a thinner Si channel is required to enhance the gate-to-channel coupling which in turn induces stronger electric field. Higher I_{ON} is achieved in the proposed structure due to the increased tunneling area from the additional horizontal hetero-junction introduced by the extended Ge source underneath the Si region. Low leakage current is ensured by having an insulator between the extended Ge source and drain to cut off the leakage conduction paths. Thus, I_{ON} is scalable with L_{OV} which alleviates the I_{ON} limitation and scalability issue faced by lateral TFET designs.

6.3 Future Directions

6.3.1 GeSn-based Transistors

Most of the device performances of GeSn transistor were assessed based on effective mass and the semi-classical approach which may not capture the performance accurately, especially when the device is scaled down to nanometer regime. The construction of the Hamiltonian of transistors based on effective mass

approximation (EMA) may lose its validity in highly scaled transistors. More advanced methods, such as the tight-binding formalism, which consider the atomistic nature of the material [206] need to be developed for accurate assessment of the device performance based on GeSn alloy. The leakage currents due to band-to-band tunneling and direct source to drain tunneling may define the I_{OFF} limit of transistor. These leakage currents are not captured by the semi-classical approach used in Chapter 2. This calls for evaluation of the electrical performance of GeSn-based transistor using quantum transport approach, such as non-equilibrium Green's function (NEGF), to capture the tunneling current component. The device performance assessment presented in Chapter 2 was carried out for GeSn n-MOSFET. However, there is still a lack of theoretical investigation of the device performance for GeSn p-MOSFET. So, the evaluation of I_{ON} performance for GeSn p-MOSFET is needed. The study of the effects of various scattering mechanisms, such as phonon scattering, on GeSn transistor is also necessary.

6.3.2 Transistors based on 2D Materials from Group IV

The ballistic I_{ON} of silicane and germanane transistor assessed in chapter 3 assumes the surface of silicene and germanene being fully covered by the hydrogen atoms. However, the hydrogen coverage may not be 100% in the real synthesis or fabrication of silicane and germanane. Thus, it is relevant to study how the hydrogen coverage affects the structural and electrical characteristic of the transistors. On the other hand, other chemical species, such as fluorine, can be used to passivate the surfaces of 2D materials. It would be useful to study the effects of chemical functionalizations due to other chemical species in terms of the electrical performance. This is to identify which chemical functionalization offers the best

electrical performance. Additionally, strain engineering is a commonly used approach to tune the electronic properties of semiconductors. It is worthwhile to study the effects of strain on the electronic transport of silicane and germanane transistors.

6.3.3 Tunneling Field-Effect Transistors

Recents simulation results, including the one reported in Chapter 5, and some experimental evidences show that the optimal electrical performance is achieved when the tunneling direction is aligned to the gate-induced electric field. To further study the device physics of the proposed structure in Chapter 5, more rigorous quantum simulation approaches, such as non-equilibrium Green's function (NEGF), are required in order to capture the quantum mechanical effects (e.g. tunneling and quantum confinement), geometry effects (e.g. EOT), and doping (e.g. source, channel, and drian doping) accurately. In addition, the interface traps at the tunneling junction can lead to the trap-assisted tunneling which degrades the subthreshold swing of TFET. Thus, the effects of interface traps on the electrical performance of TFET require further study using the quantum simulator. Another device structure based on vertical tunneling is the electron-hole bilayer tunneling field-effect transistor (EHB-TFET) [207]. Even though EHB-TFET holds promise for achieving higher I_{ON}, further investigation and optimization of this structure are needed. Possible works include making use of heterostructure at the tunneling junctions for the enhancement of I_{ON}. There are a few type II staggered band alignments available from the III-V semiconductors, such as GaSb-InAs heterojunction. Apart from that, the diagonal parasitic tunneling paths that exist between the channel and the drain are responsible for the degradation of the *S*. Hence, further works on the drain engineering to suppress the parasitic diagonal tunneling are necessary.

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Appendix

List of Publications

Journal Publications

1. **K. L. Low**, C. Zhan, G. Han, Y. Yang, K.-H. Goh, P. Guo, E.-H. Toh, and Y.-C. Yeo, "Device physics and design of a L-shaped Germanium source tunneling transistor," *Japanese Journal of Applied Physics*, vol. 51, no. 2S, pp. 02BC04, Feb. 2012.

2. **K. L. Low**, Y. Yang, G. Han, W. Fan, and Y.-C. Yeo, "Electronic band structure and effective mass parameters of $Ge_{1-x}Sn_x$ alloys," *Journal of Applied Physics*, vol. 112, no. 10, pp. 103715, Nov. 2012.

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4. **K. L. Low**, Y.-C. Yeo, and G. Liang, "Ultimate Performance Projection of Ultra-Thin-Body Transistor based on Group IV, III-V, and 2D-Materials," *IEEE Transactions on Electron Devices* (Accepted).

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1. **K. L. Low**, C. Zhan, G. Han, Y. Yang, K. H. Goh, P. Guo, E.-H. Toh, and Y.-C. Yeo, "Tunnel field-effect transistor with L-shaped germanium source: Device physics and design," *Extended Abstracts of the 2011 International Conference on Solid State Devices and Materials*, Nagoya, Japan, Sep. 28-30, 2011, pp. 849-850.

2. **K. L. Low**, Y. Yang, G. Han, W.-J. Fan, and Y.-C. Yeo, "Electronic band structure and effective masses of $Ge_{1-x}Sn_x$ alloys," *222nd Electrochemical Society Meeting*, Honolulu, HI USA, Oct. 7-12, 2012, pp. 519-526.

3. **K. L. Low**, Y.-C. Yeo, G. Liang, "Voltage scalability of double gate ultra-thin-body field-effect transistors with channel materials from group IV, III-V to 2D-materials based on ITRS metrics for year 2018 and beyond," *72nd Device Research Conference (DRC)*, Santa Barbara CA, USA, Jun. 22-25, 2014, pp. 203-204.

Other Co-authored Publications

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1. Y. Guo, X. Zhang, **K. L. Low**, K.-T. Lam, Y.-C. Yeo, and G. Liang, "Effect of Body Thickness on the Electrical Performance of Ballistic n-Channel GaSb Double gate Ultrathin-Body Transistor", *IEEE Transactions on Electron Devices*, vol. 62, no. 3, pp. 788 - 794, Mar. 2015.

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3. Y. Yang, **K. L. Low**, W. Wang, P. Guo, L. Wang, G. Han, and Y.-C. Yeo, "Germanium-tin n-channel tunneling field-effect transistor: Device physics and simulation study," *Journal of Applied Physics*, vol. 113, no. 19, pp. 194507, May 2013.

4. K.-H. Goh, Y. Cheng, **K. L. Low**, E. Y. J. Kong, C.-K. Chia, E.-H. Toh, and Y.-C. Yeo, "Physical model for gallium arsenide growth on germanium fins with different orientations formed on 10° offcut germanium-on-insulator substrate," *Journal of Applied Physics*, vol. 113, no. 4, pp. 044103, Jan. 2013.

5. Y. Tong, Q. Zhou, **K. L. Low**, L. X. Wang, L. H. Chua, T. Thanigaivelan, T. Henry, and Y.-C. Yeo, "Cold silicon pre-amorphization implant and pre-silicide sulfur implant for advanced nickel silicide contacts," *IEEE Transactions on Electron Devices*, vol. 61, no. 10, pp. 3499-3506, Aug. 2014.

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