STUDY OF CMOS COMPATIBLE RUTHENIUM OXIDE SCHOTTKY CONTACTS FOR ALGAN/GAN AND INALN/GAN DIODES AND HIGH MOBILITY TRANSISTORS GROWN ON SILICON (111) SUBSTRATES

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2015

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DECLARATION

I hereby declare that this thesis is my original work and it has been written by me in its entirety.

I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

LWIN MIN KYAW

30 July 2015

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Table of Contents

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

2DEG	2 Dimensional Electron Gas
AFM	Atomic Force Microscopy
Al	Aluminium
ALD	Atomic Layer Deposition
AlGaAs/InGaAs	Aluminum Gallium Arsenide/Indium Gallium Arsenide
AlGaN/GaN	Aluminum Gallium Nitride/Gallium Nitride
Au	Gold
BCl_3	Bromine trichloride
Cl_2	Chlorine
CMOS	Complementary Metal-Oxide-Semiconductor
CTLM	Circular Transmission Line Method
DC	Direct Current
DI	De-Ionized
EDS	Energy-Dispersive X-ray Spectroscopy
FE	Field Emission
FOM	Figure Of Merit
Ga	Gallium
GaAs	Gallium Arsenide
GaAs	Gallium Arsenide
HAADF	High-Angle Annular Dark Field
HEMT	High Electron Mobility Transistor
ICP	Inductively Coupled Plasma
InAlN/GaN	Indium Aluminum Nitride/Gallium Nitride

IPA	Iso-Propyl Alcohol
Ir	Iridium
LDMOSFET	Laterally Diffused Metal Oxide Semiconductor Field Effect Transistor
LTLM	Linear Transmission Line Method
MIS	Metal Insulator Semiconductor
MOCVD	Metal Organic Chemical Vapor Deposition
MOS	Metal Oxide Semiconductor
N	Nitrogen
Ni	Nickel
O	Oxygen
PA	Power Amplifier
Pd	Paladium
Pt	Platinum
RF	Radio Frequency
RIE	Reactive Ion Etch
RTA	Rapid Thermal Annealing
Ru	Ruthenium
RuO_2	Ruthenium Dioxide
RuO_x	Ruthenium Oxide
SBH	Schottky barrier height
Si	Silicon
SiC	Silicon Carbide
SIMS	Secondary Ion Mass Spectroscopy
STEM	Scanning Transmission Electron Microscopy
TEM	Transmission Electron Microscopy

Ti	Titanium
ToF-SIMS	Time of Flight Secondary Ion Mass Spectroscopy
UV	Ultra-Violet
W	Tungsten
W-CDMA	Wide Band Code Division Multiple Access
WN_x	Tungsten Nitride
XRD	X-ray Diffraction
μ-PL	Micro-Photo-Luminicence

LIST OF SYMBOLS

Symbol	Property	Unit
E_g	bandgap	eV
ε_r	relative permittivity	-
E_c	critical breakdown field	MV/cm
μ_n	electron mobility	$cm^2/V{\cdot}s$
σ_{th}	thermal conductivity	$W/cm{\cdot}K$
v_t	electron saturation velocity	cm/s
P_{SP}	spontaneous polarization	cm^{-2}
P_{PE}	piezoelectric polarization	cm^{-2}
f_T	unity current gain cut off frequency	Hz
f_{max}	unity power gain cut off frequency	Hz
R_c	contact resistance	Ω
R_{sh}	sheet resistance	Ω/□
ρ_c	contact resistivity	$\Omega{\cdot}cm^2$
φ_b	Schottky barrier height	eV
φ_m	metal work function	eV
χ_s	electron affinity of the semiconductor	eV
S	fermi level pinning factor	-
ΔX	the difference in electronegativity of constituent elements in semiconductor	eV
m^*	effective mass of carrier	kg
q	electron charge	C
h	planck constant	$m^2{\cdot}kg/s$
λ	de Broglie wavelength	m

k_B	Boltzmann’s constant	$m^2 \cdot kg \cdot s^{-2} \cdot K^{-}_{1}$
T	temperature	^{o}C or K
R_T	total resistance	Ω
L_T	transfer length	cm
J	current density	Acm^{-2}
A^*	Richardson's constant	$Acm^{-2}K^{-2}$
n	ideality factor	-
SBH	Schottky Barrier Height	eV
I	current	A/mm
F	Lorentz force	N
B_z	magnetic field in z direction	T
v_x	velocity in x direction	m/s
ε_y	electromotive force in y direction	V
J_x	current density in x direction	Acm^{-2}
n_s	carrier density	cm^{-3}
n_{sh}	sheet carrier density	cm^{-2}
μ_s	carrier mobility	$cm^2/V \cdot s$
V_H	Hall voltage	V
d_{hkl}	inter-planar spacing of any lattice planes with Miller indices {h k l}	-
θ	Bragg's angle	degree
V_{GS}	gate to source voltage	V
V_{DS}	drain to source voltage	V
V_{GD}	gate to drain voltage	V
V_{TH}	threshold voltage	V
$V_{overdrive}$	overdrive voltage	V
$I_{DSAT(max)}$	maximum drain current	A/mm

I_D	drain current	A/mm
I_{OFF}	OFF State current	A/mm
I_{ON}	ON State current	A/mm
I_{DSAT}	drain saturation current	A/mm
I_G	gate current	A/mm
I_{SUB}	substrate current	A/mm
SS	sub-threshold swing	mV/decade
C_G	gate capacitance	Fcm^{-2}
C_{GA}	maximum accumulation gate capacitance	Fcm^{-2}
R_{on}	static on state resistance	Ω·mm
L_{gd}	gate to drain distance	µm
L_{gs}	gate to source distance	µm
L_g	gate length	µm
W_g	gate width	µm
$E_{g0\text{-}2DEG}$	bandgap of the GaN near 2DEG	eV
T_0	Debye temperature	K
ω_0	phonon frequency at 0 K	cm^{-1}
c	speed of light	m/s
R_a	average roughness	nm
R_q	root mean square roughness	nm

LIST OF PUBLICATIONS

Journal Publications Directly Related to this Thesis

1. **L. M. Kyaw**, A. A. Saju, Y. Liu, M. K. Bera, S. P. Singh, S. Tripathy, and E. F. Chor, "Thermally Robust RuO_x Schottky Diodes and HEMTs on III-Nitrides", *Phys. Status Solidi C,* 11 (2014) 1–4.
2. **L. M. Kyaw**, S. B. Dolmanan, M. K. Bera, Y. Liu, H. R. Tan, T. N. Bhat, Y. Dikme, E. F. Chor and S. Tripathy, "Influence of RuO_x Gate Thermal Annealing on Electrical Characteristics of $Al_xGa_{1-x}N$/GaN HEMTs on 200-mm Silicon", *ECS Solid State Letters*, 3(2), (2014) Q5-Q8.
3. S. Tripathy, **L. M. Kyaw**, S. B. Dolmanan, Y. J. Ngoo, Y. Liu, M. K. Bera, S. P. Singh, H. R. Tan, T. N. Bhat, and E. F. Chor, "$In_xAl_{1-x}N$/AlN/GaN High Electron Mobility Transistor Structures on 200 mm Diameter Si(111) Substrates with Au-free Device Processing", *ECS Journal of Solid State Science and Technology,* 3(5), (2014) Q84-Q88.
4. **L. M. Kyaw**, L. K. Bera, Y. Liu, M. K. Bera, S. P. Singh, S. B. Dolmanan, H. R. Tan, T. N. Bhat, E. F. Chor, and S. Tripathy, "Probing channel temperature profiles in $Al_xGa_{1-x}N$/GaN high electron mobility transistors on 200 mm diameter Si(111) by optical spectroscopy", *Applied Physics Letters*, 105 (2014) 073504.
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6. **L. M. Kyaw**, Y. Liu, M. Y. Lai, T. N. Bhat, H. R. Tan, P. C. Lim, S. Tripathy, and E. F. Chor, "Annealing Pressure Dependent RuO_x Schottky Contacts on InAlN/AlN/GaN-on-Si(111) Heterostructure", *ECS Journal of Solid State Science and Technology*, 5 (2016) Q17.

Other Journal Publications

1. Y. Liu, S. P. Singh, Y. J. Ngoo, **L. M. Kyaw**, M. K. Bera, G. Q. Lo, and E. F. Chor, "Low thermal budget Hf/Al/Ta ohmic contacts for InAlN/GaN-on-Si HEMTs with enhanced breakdown voltage", *Journal of Vacuum Science &Technology B*, 32 (2014) 032201.
2. Y. Liu, S. P. Singh, **L. M. Kyaw**, M. K. Bera, Y. J. Ngoo, H. R. Tan, S. Tripathy, G. Q. Lo, and E. F. Chor, "Mechanisms of Ohmic Contact Formation and Carrier Transport of Low Temperature Annealed Hf/Al/Ta on $In_{0.18}Al_{0.82}N$/GaN-on-Si", *ECS Journal of Solid State Science and Technology*, 4(2), (2015) P30-P35.
3. M. K. Bera, Y. Liu, **L. M. Kyaw**, Y. J. Ngoo, S. P. Singh, and E. F. Chor, "Positive Threshold-Voltage Shift of Y_2O_3 Gate Dielectric InAlN/GaN-on-Si (111) MOSHEMTs with respect to HEMTs", *ECS Journal of Solid State Science and Technology*, 3(6), (2014) Q120-Q126.
4. S. P. Singh, Y. Liu, Y. J. Ngoo, **L. M. Kyaw**, M. K. Bera, S. B. Dolmanan, S. Tripathy and E. F. Chor, "Influence of PECVD deposited SiN_x passivation layer thickness on $In_{0.18}Al_{0.82}N$/GaN/Si HEMT", *Journal of Physics D: Applied Physics, (*in press).

Conference Publications and Presentations Directly Related to this Thesis

1. **L. M. Kyaw**, Y. Liu, M.K. Bera, Y. J. Ngoo, S. Tripathy, E. F. Chor, “Gold-free InAlN/GaN Schottky Gate HEMT on Si(111) Substrate with ZrO_2 Passivation”, *ECS Transactions*, 53(2), (2013) 75-83.
2. **L. M. Kyaw**, L. K. Bera, Y. Liu, M. K. Bera, S. P. Singh, S. B. Dolmanan, T. N. Bhat, E. F. Chor, and S. Tripathy, "Micro-Raman and Photoluminescence Thermography of AlGaN/GaN HEMTs Grown on 200 mm Si(111)", presented at the International Workshop on Nitride Semiconductors (IWN 2014), Wroclaw, Poland, August 24-29, 2014.
3. **L. M. Kyaw**, Y. Liu, M. K. Bera, S. P. Singh, S. Tripathy, and E. F. Chor, "Electrical Characteristics of Au-free $In_xAl_{1-x}N$/GaN HEMTs Fabricated Using A Single Contact Annealing Process", presented at the International Workshop on Nitride Semiconductors (IWN 2014), Wroclaw, Poland, August 24-29, 2014.
4. **L. M. Kyaw**, Y. Liu, M. Y. Lai, T. N. Bhat, H. R. Tan, P. C. Lim, S. Tripathy, and E. F. Chor, "Effect of Annealing Pressure and Ambient on Thermally Robust RuO_x Schottky Contacts on InAlN/AlN/GaN-on-Si(111) Heterostructure", *ECS Transactions*, 66(1), (2015) 249-257.

Other Conference Publications and Presentations

5. *Y. Liu*, M. K. Bera, **L. M. Kyaw**, G. Q. Lo, E. F. Chor, “Low resistivity Hf/Al/Ni/Au Ohmic Contact Scheme ton-Type GaN”, *World Academy of Science, Engineering and Technology* 69, (2012) 602
6. M. K. Bera, *Y. Liu*, **L. M. Kyaw**, Y. J. Ngoo, and E. F. Chor, “Thickness Dependent Electrical Characteristics of InAlN/GaN-on-Si MOSHEMTs

with Y_2O_3 Gate Dielectric and Au-free Ohmic Contact", *ECS Transactions*,53(2), (2013) 65-74

7. M. K. Bera, *Y. Liu*, **L. M. Kyaw**, Y. J. Ngoo, S. P. Singh, and E. F. Chor, "Fabrication and performance of InAlN/GaN-on-Si MOSHEMTs with $LaAlO_3$ gate dielectric using gate-first CMOS compatible process at low thermal budget", *ECS Transactions*, 61(4), (2014) 271.
8. *Y. Liu*, **L. M. Kyaw**, M.K. Bera, S. P. Singh, Y. J. Ngoo, G.Q. Lo, and E. F. Chor, "Low thermal budget Au-Free Hf-based ohmic contacts on InAlN/GaN heterostructure", *ECS Transactions*, 61(4), (2014) 319.
9. S. P. Singh, *Y. Liu*, **L. M. Kyaw**, Y. J. Ngoo, M. K. Bera, S. Tripathy, and E. F. Chor, "Silicon nitride thickness dependence electrical properties of InAlN/GaN heterostructures", *ECS Transactions*, 61(4), (2014) 215.

SUMMARY

In this thesis, the study focuses on the development of gold-free, CMOS compatible Schottky contact for low cost, low leakage current and high performance GaN based diodes and high mobility transistors (HEMTs). Our preliminary investigations show that although Ni/W Schottky contact is cheaper than conventional Ni/Au Schottky contact (as W is lower cost than Au), the leakage current and thermal stability are only comparable to that of Ni/Au. Our further studies have demonstrated that RuO_x Schottky contact yields lower leakage current and better thermal stability than Ni/Au Schottky contact on InAlN/GaN HEMTs. RuO_x Schottky contact is more thermally stable up to 800^{o}C compared to the latter at 600^{o}C. In addition, RuO_x Schottky contact exhitibts approxmiately 4 orders of magnitude lower leakage current than that of Ni/Au Schottky contact on InAlN/GaN HEMTs. Moreover, it has been found that the material and electrical characteristics of RuO_x Schottky contact depend on the annealing ambient and pressure (vacuum, N_2 and Ar; with N_2 and Ar at the same pressure). Annealing pressure has been shown to play a vital role, while ambient has minimal effect, in changing the material and electrical characteristics of RuO_x Schottky contact. With RuO_x thin film being semitransparent to optical excitation wavelengths, accurate thermal investigations underneath the gate of both AlGaN/GaN HEMTs and InAlN/GaN HEMTs have been made possible by means of micro-Raman and Photoluminescence (PL) techniques. This is not achievable with conventional Ni/Au gate. The maximum temperatures of both AlGaN/GaN HEMTs and InAlN/GaN HEMTs occur at the gate edge between gate and drain and their values are 435 K and 475 K respectively. Lastly, with thermally robust RuO_x

Schottky contact, we have demonstrated that the performance of InAlN/GaN HEMTs using a single contact annealing process is comparable to that of HEMTs using a conventional gate-last process. In conclusion, employing RuO_x Schottky contact in GaN based HEMTs could realize CMOS compatibility, high thermal budget and low leakage HEMTs for low cost, high temperature, high speed and high power applications.

Chapter 1: Introduction

1.1 Properties of Gallium Nitride

Gallium nitride (GaN) based devices have been attractive to researchers since the deomonstration of successful GaN synthesis demonstrated by Johnson *et al.* in 1932 [1] for more than eight decades. They are promising for high-temperature, high-speed and high-power electronic applications due to the superior material properties of GaN and also that of related III-nitrides over silicon (Si), gallium arsenide (GaAs) and silicon carbide (SiC). These material properties are listed in Table 1.1, which highlights the material parameter comparison among Si, GaAs, SiC, and GaN[2]. It can be observed in Table 1.1 that GaN has the widest bandgap (3.4 eV) among these materials. This indicates that GaN has high resistance to thermally generated leakage current; hence, it is suitable for high temperature applications. In addition, owing to its high critical breakdown field (around 4 MV/cm), GaN-based electronic devices such as diodes and transistors would be able to operate in high power applications. In addition, excellent electron transport characteristics of GaN including high electron mobility of 1300 $cm^2/V{\cdot}s$ and high electron saturation velocity of 3×10^7 $cm{\cdot}s^{-1}$ mean that it is also suitable for high speed and high frequency electron devices.

Table 1.1 Material parameters for Si, GaAs, SiC and GaN [2].

Material	**Si**	**GaAs**	**SiC**	**GaN**
Bandgap,E_g(eV)	1.12	1.42	3.25	**3.40**
Relative permittivity,ε_r	11.8	12.8	9.7	**9.0**
Breakdown field,E_c (MV/cm)	0.25	0.4	3	**4.0**
Electron saturation velocity,v_t (10^7 cm/s)	1.0	2.0	2.0	**3.0**
Electron mobility,μ_n (cm^2/V·s)	1300	6000	800	**1350**
Thermal conductivity,σ_{th}(W/cm·K)	1.5	0.5	4.9	**1.3**

Table 1.2 shows the figures of merit (FOMs) for Si, GaAs, SiC, and GaN[3], where Chow and Tyagi theoretically highlighted the advantages of GaN over Si, GaAs, and SiC for high frequency and high power applications by means of Johnson, Keyes and Baliga figures of merit. These figures are related to the material parameters such as the critical breakdown field (E_c), the dielectric permittivity (ε), the carrier mobility (μ), the thermal conductivity (σ_{th}), and the saturated electron velocity (v_t). These FOMs are used to evaluate the ability of power handling and thermal dissipation for electron devices. As observed in Table 1.2, FOMs of GaN are the best among these materials; hence, it is well suited for high speed, high-power and high-temperature applications.

Table 1.2 Figures of merit (FOMs) for various semiconductors at 300K for microwave power device applications. All FOMs are normalized with respect to those of silicon.

Figures of merit	**Johnson**	**Keyes**	**Baliga-low frequencies**	**Baliga-high frequencies**
Equation	$\propto (E_c v_t)^2$	$\propto \sigma_{th} \left(\frac{V_t}{\varepsilon}\right)^{1/2}$	$\propto \varepsilon \mu E_c^{\ 3}$	$\propto \mu E_c^{\ 3}$
Description	Power handling at high frequencies	Thermal dissipation	Power handling at low frequencies	Power handling at high frequencies
Si	1	1	1	1
GaAs	11	0.45	28	16
SiC	37	0.73	16	3.8
GaN	**790**	**1.8**	**910**	**100**

In addition, GaN based heterostructure technologies are available which allow quantum well and hetero-junction in GaN material system to span new operation areas for GaN based high mobility electron transistors (HEMTs). In GaN based HEMTs, two dimension electron gas (2DEG) results when a barrier layer (e.g., AlGaN or InAlN) is in contact with a buffer layer (e.g., GaN). This 2DEG has high electron density and high mobility without intentional doping in the barrier layer due to large spontaneous and piezoelectric polarizations[4, 5]. This reduces the coulombic scattering in GaN based heterostructure resulting in increased mobility [6]. For example, an

electron mobility in excess of 2000 $cm^2/V{\cdot}s$ at room temperature and 11000 $cm^2/V{\cdot}s$ at 4.2 K have been reported in the 2DEG channel in AlGaN/GaN HEMT grown on 6H-SiC substrate [7].

In addition to its excellent electrical properties mentioned above, GaN has a high hardness, thermal conductivity and excellent chemical inertness. This allows GaN-based devices to operate well in harsh environments [8]. Furthermore, with robustness against radiation, GaN could be used in military and space applications[9].

1.2 GaN based High Electron Mobility Transistors

1.2.1 GaN HEMT heterostructure growth

Due to the lack of native GaN substrates in large quantities, researchers had tried nearly most of the crystal-growth technologies on different substrates and orientations to grow high quality GaN materials. With the great progress achieved in the past several decades, GaN based heterostructures have been epitaxially grown in both metal organic chemical vapor deposition (MOCVD) [10] and molecular beam epitaxy (MBE) systems[11]. Compared to the latter, the former growth system is more popular for the epitaxial growth of GaN based heterostructures due to higher growth rate capability, multi-wafer growth capability leading to lower process cost and, similar quality of heterostructures and HEMTs [12].

Traditionally, GaN-based heterostructures have been grown on SiC and sapphire [15]. SiC substrate has a low lattice mismatch (3.5%) to GaN and a good thermal conductivity (4.9 W/cm.K), and good quality GaN HEMT epi-

layer structure on 4 inch SiC substrate have been demonstrated [16, 17, 18]. However, SiC substrate is expensive and large size 200 mm diameter SiC substrate is not available yet. On the other hand, sapphire substrate is less costly than SiC substrate. However, sapphire has a poor lattice mismatch (16.1%) to GaN and poor thermal conductivity (0.32 W/cm.K) [16]. More recently, researchers have become interested in growing GaN on Si substrate. Even though Si substrate has a large lattice mismatch (16%) to GaN, it is attractive due to the large wafer size availability (> 200 mm diameter), low wafer cost, and its relatively high thermal conductivity. Much research is being performed in order to overcome the challenges to obtain a good quality nitride based heterostructure on large Si wafers (specifically 200 mm diameter and above). With the capability of growing GaN based heterostructure on large size silicon substrate, it is one step closer to achieve economical GaN-on-silicon high power and high speed devices.

Table 1.3 summarizes the properties of various substrates for GaN epitaxial growth.

There are mainly two GaN based heterostructures used for the fabrication of HEMTs. One is the AlGaN/GaN heterostructure and another is the InAlN/GaN heterostructure. When a thin AlGaN epilayer is grown on a GaN buffer layer, a tensile strain is introduced in the top thin barrier layer resulting from lattice mismatch between the AlGaN barrier layer and GaN buffer layer. Both the piezoelectric polarization due to the presence of strain and the spontaneous polarization for nitride barriers are in the same direction. Furthermore, these 2 polarization fields are large enough to produce 2DEGs confined in the heterostructure without any dopant introduced in the barrier

layer. Normally, the sheet carrier concentration of 2DEG at the AlGaN/GaN heterostructure is in the range of ~10^{13} carriers per cm^2 and the mobility of carriers is as high as 1600 cm^2/Vs, owing to less scattering from ionized dopants and the interfaces resulted from having smoother surface at hetero interface compared to the surface of Si-SiO_2 interface in MOSFET. On the other hand, lattice matched $In_{0.17}Al_{0.83}N$/GaN heterostructure is strain free, thus resulting in reduced defects due to lattice mismatch and better reliability [8]. Moreover, the strong spontaneous polarization of the InAlN barrier layer induces a high sheet carrier density > 2 x 10^{13} cm^{-2} in 2DEG [9]. However, the carrier mobility in the InAlN/GaN 2DEG is not as high as that of AlGaN/GaN due to higher alloy disorder scattering compared to AlGaN/GaN [10]. Figure 1.1 shows the typical cross sectional view of AlGaN/GaN heterostructure and InAlN/GaN heterostructure grown on Si(111) substrate.

Table 1.3 Comparison of substrates available for GaN epitaxial growth[13, 14].

Substrate	**SiC**	**Sapphire**	**Si**
Thermal Conductivity (W/cm·K)	3	0.5	**1.5**
Resistivity (Ω·cm)	$>10^4$	$>10^8$	**$>10^4$**
Diameter used for Epitaxy (in)	2-3	2-4	**2-8**
Lattice mismatch to GaN (%)	3.5	16	**16.9**
Thermal expansion mismatch to GaN	18.9	-25.4	**116**
Cost	high	low	**low**

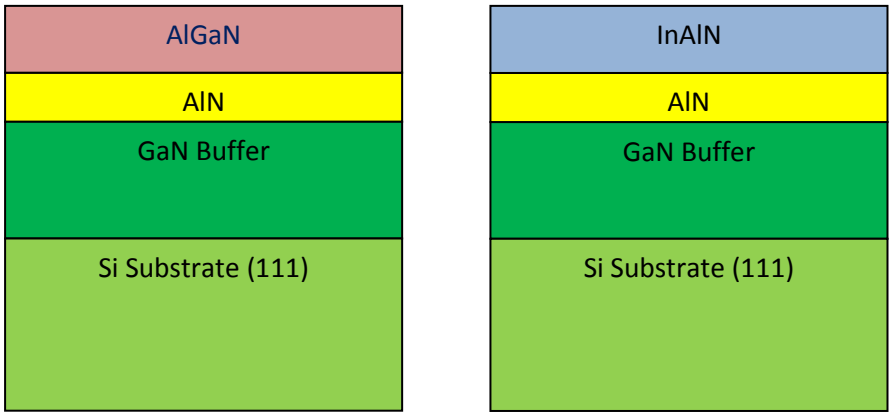

Figure 1.1 Schematic drawing of cross sectional view of AlGaN/GaN (left) and InAlN/GaN (right) heterostructure grown on Si(111) substrate.

1.2.2 Development of GaN based HEMTs

GaN based HEMTs can be divided into three groups depending on their gate stack structure namely Schottky (metal-semiconductor) gate HEMT, p-GaN gate HEMT and metal-insulator-semiconductor (MIS) gate HEMT. The cross sections of the HEMTs based on these three structures are shown in Figure 1.2. The p-GaN [11, 12] and MIS gate HEMTs are widely used for high power applications where the low leakage current and high breakdown voltage are desired. For high frequency applications, Schottky and MIS gate HEMTs are widely used. On the other hand, p-GaN gate is not a good candidate to be used in high frequency application due to its high Ohmic and access resistance which would increase the gate delay, hence, reducing the frequency performance compared to Schottky and MIS gate. Since our main focus is high frequency and high power HEMTs, we will focus on Schottky gate HEMT and MIS gate HEMT. The focus of my project is on Schottky gate HEMTs, while MIS gate HEMTs is carried out by another researcher in our research group.

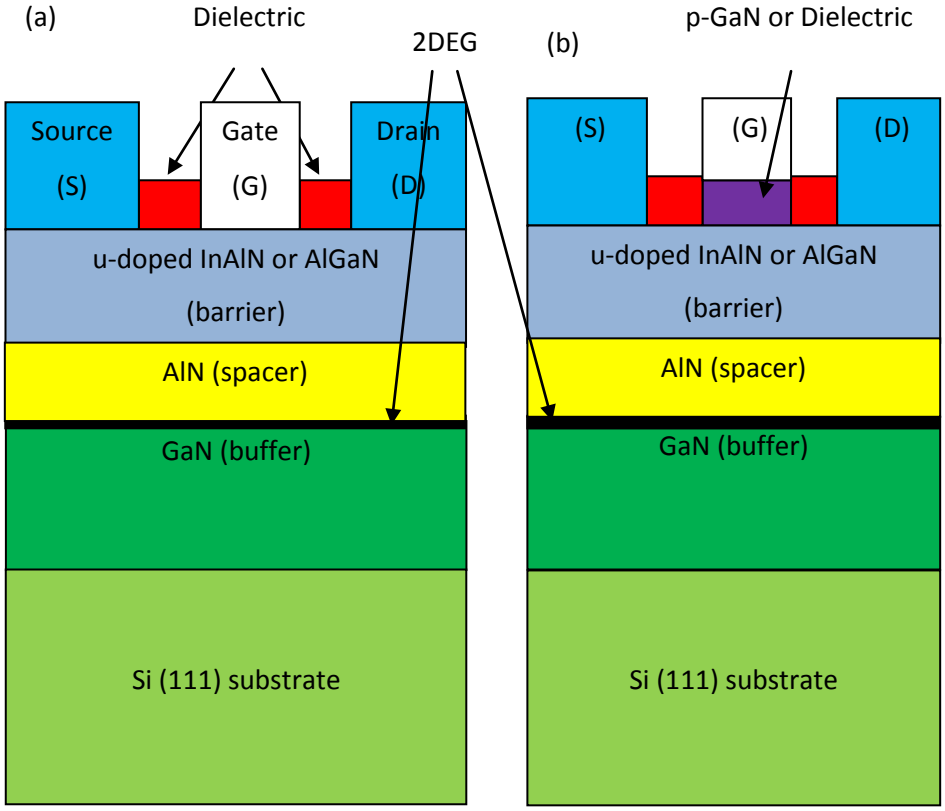

Figure 1.2 Schematic cross-sections of (a) Schottky gate HEMT (b) p-GaN gate HEMT or MIS gate HEMT.

The conventional fabrication of GaN HEMT uses a gate-last process, meaning the gate is made after the source/drain contact annealing, and this is shown in Figure 1.3. The gate-last process is commonly used because the traditional gold-based gate contact (e.g., Ni/Au) is not thermally robust to withstand the high temperature annealing (> 700^{o}C) required for the formation of low contact resistance of gold-based source/drain Ohmic contacts (e.g., Ti/Al/Ni/Au) to GaN based HEMTs. Annealing at such temperature could lead to high gate leakage due to Ni/Au thermal instability. More recently, a gate-first process has been proposed and this is shown in Figure 1.4. It should be noted that Si MOSFET process is typically a gate-first process.

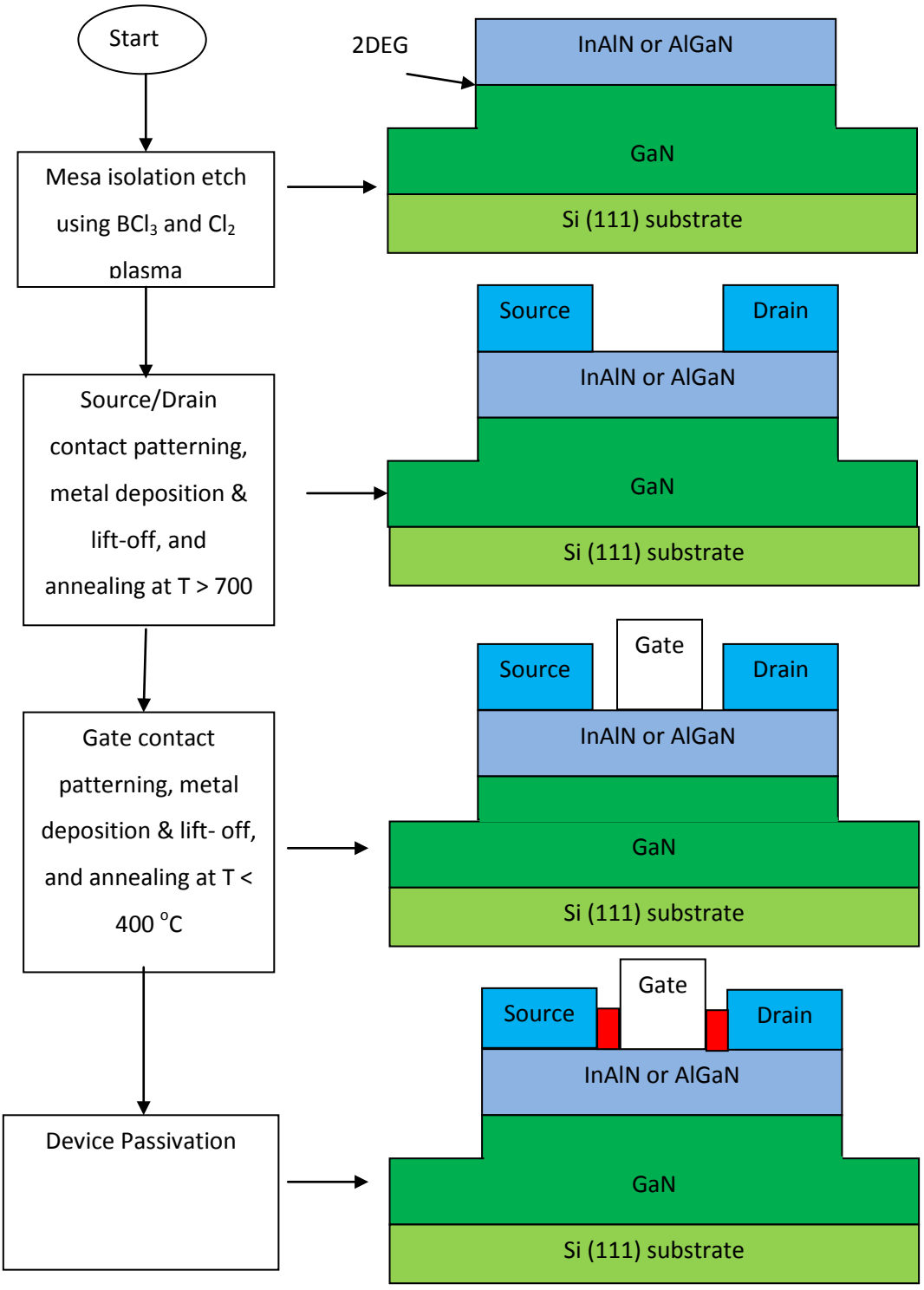

Figure 1.3 The conventional gate-last fabrication process of HEMT

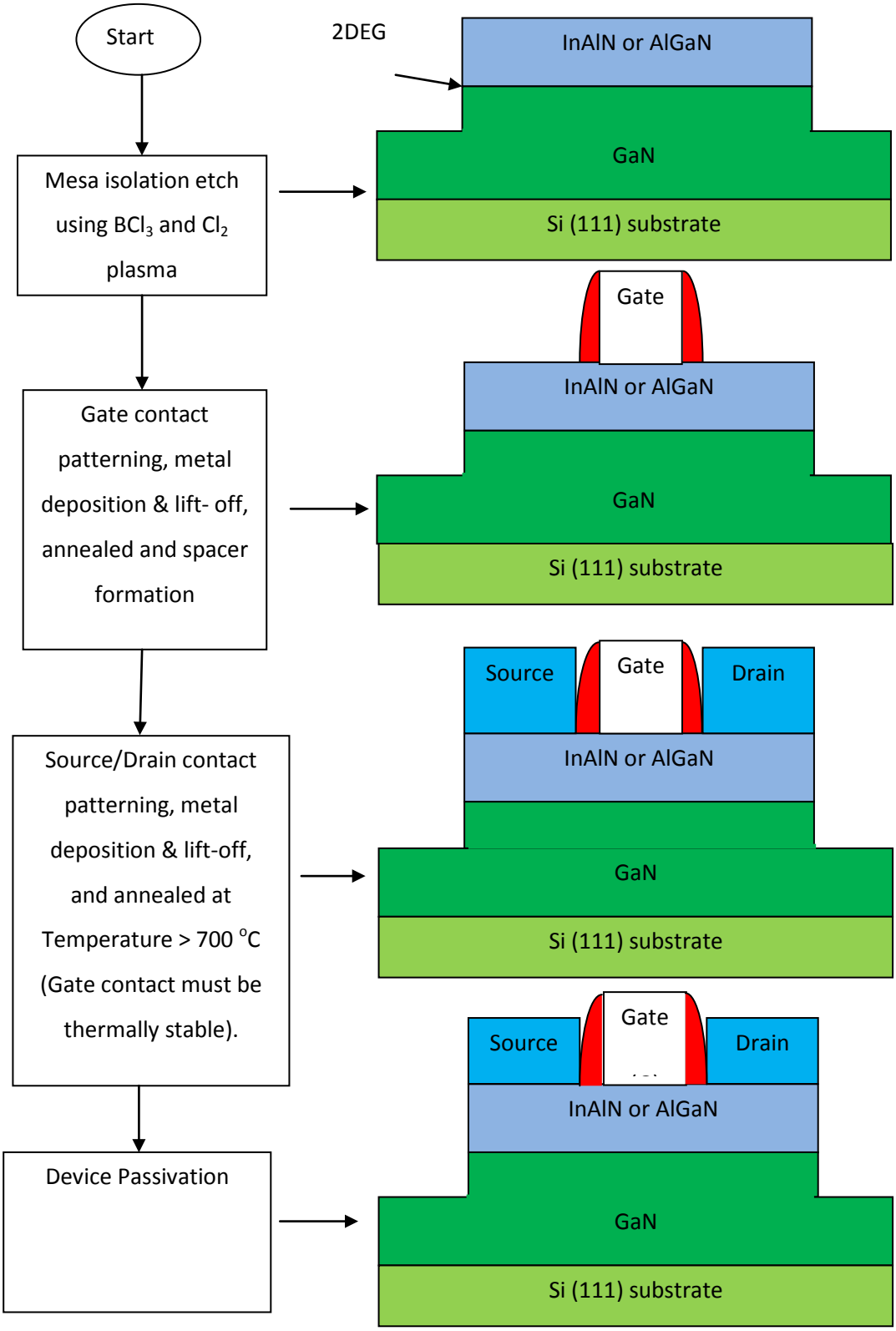

Figure 1.4 Gate-first fabrication process of HEMT

The gate-last process, as shown in Figure 1.3, starts with mesa isolation etch using inductively coupled plasma (ICP) with the gas mixture of BCl_3 and Cl_2, as shown in Figure 1.3. Following which, the source/drain contacts are patterned, and the metals are deposited using reactive sputtering or e-beam evaporation system. The contacts are defined after metal lift-off and are annealed at very high temperature (> 700^{o}C) to achieve Ohmic properties. The gate contact is subsequently patterned, and the gate metal is deposited using reactive sputtering or e-beam evaporation system. The gate contact is again defined after metal lift-off and is annealed at a moderate temperature (typically below 400^{o}C). The passivation dielectric layer is then deposited to complete the device fabrications.

1.2.3 AlGaN/GaN HEMTs technology

Owing to the excellent material properties of GaN and the benefits of heterojunctions, AlGaN/GaN HEMTs have been showing great prospective for high-power and high-frequency operations since the first demonstration in 1993 [15] in which Khan et al. reported that the AlGaN/GaN HEMTs with a 250 nm gate length exhibited maximum transconductance, $g_{m(max)}$, of 23 mS/mm, a maximum drain current, $I_{DSAT(max)}$, of 180 mA/mm, and an electron mobility of 563 cm^2/V·s at 300 K. Since the quality of AlGaN/GaN wafer and device processing technology is continuously enhanced from the first demonstration, the current AlGaN/GaN HEMTs exhibit great improvement in performance and could be comparable or better than other contending materials such as Si, GaAs, and SiC. Chung et al. [16] reported that $I_{DSAT(max)}$

of 1.2 A/mm and $g_{m(max)}$ of 410 mS/mm, an unity current gain cut off frequency, f_T of 70 GHz and a unity power gain cut off frequency, f_{max}, of 300 GHz were obtained in AlGaN/GaN-on-SiC HEMTs. For low cost and high performance GaN HEMTs on Si, Bouzid-Driad et al. [17] demonstrated that $I_{DSAT(max)}$ of 820 mA/mm, $g_{m(max)}$ of 440 mS/mm, and a f_T of 100 GHz and a high f_{max} of 206 GHz were achieved in AlGaN/GaN-on-Si HEMTs. Medjoub et al. [18] have demonstrated 100 nm gate GaN HEMT on 100 mm Si with a output power density of 2.5 W/mm at 40 GHz. Therefore, AlGaN/GaN HEMTs grown on Si are suitable for high frequency applications. In addition, Ikeda et al. [19] reported that 1.8 kV of three-terminal off-state breakdown voltage with ~15 µm gate to drain distance was achieved in AlGaN/GaN HEMTs on Si (111) substrate. Hence, this highlights that AlGaN/GaN HEMTs grown on Si are also suitable for high power applications.

1.2.4 InAlN/GaN HEMTs technology

Another GaN based heterostructure, InAlN/GaN, becomes popular for microwave power electronic technology [20]. In $In_{0.18}Al_{0.82}N$/GaN heterostructure, strain and piezoelectric polarization resulted from lattice mismatch do not exist. As shown in Table 1.4, InAlN/GaN heterostructure can provide higher 2DEG carrier concentration due to ~ 3 times higher spontaneous polarization than that of AlGaN/GaN, which means that a higher output current density can be achieved if the breakdown conditions can be maintained [21]. InAlN/GaN HEMTs have been shown experimentally to have

higher polarization charges without the drawback of high strain that resulted from lattice mismatch[22].

Table 1.4 Spontaneous polarization ($\mathbf{P}_{SP}$) and piezoelectric polarization ($\mathbf{P}_{EP}$) and theoretical calculation of the free electron density ($\mathbf{n}_s$) in InAlN/GaN and AlGaN/GaN HEMTs[23].

Structure	$\Delta\mathbf{P}_{SP}(cm^{-2})$	$\mathbf{P}_{EP}(cm^{-2})$	$\mathbf{n}_s$ (cm^{-2})
$Al_{0.3}Ga_{0.7}N/GaN$	-1.56×10^{-2}	-9.8×10^{-3}	1.58×10^{13}
$In_{0.17}Al_{0.83}/GaN$	-4.37×10^{-2}	0	2.73×10^{13}

The outstanding device performances have been reported[23-26] for InAlN/GaN HEMTs grown on SiC. Yue et al. [27] achieved $I_{DSAT(max)}$ of 1.9 A/mm, $g_{m(max)}$ of 653 m/mm and f_T of 400 GHz in InAlN/GaN-on-SiC HEMTs. Sun et al [28] reported that InAlN/GaN HEMTs grown on Si (111) has $I_{DSAT(max)}$ of 1.3 A/mm, $g_{m(max)}$ of 330 m/mm and f_T of 102 GHz which is the highest value achieved for InAlN/GaN HEMTs grown on Si(111). These results clearly demonstrate that InAlN/GaN HEMTs grown on Si(111) has not reached the potential yet. Further development of InAlN/GaN HEMTs depends on the improvement of material quality, the optimization of device structures and device processing technology.

1.2.5 Advantages of GaN HEMTs over Si LDMOSFETs

Owing to superior material properties, GaN based HEMT has many advantages over Si laterally diffused metal oxide semiconductor field effect

transistor, LDMOSFET. Lee et. al has studied the comparison of GaN based HEMT and Si LDMOS power amplifiers (PAs) for wide band code division multiple access (W-CDMA) applications [13]. In the study, they reported that GaN HEMT based class AB PA has 8.7 % higher efficiency compared to Si LDMOS counterpart. Furthermore, GaN HEMT PA is less sensitive to changes in temperature and can be controlled by the adaptive control of Pre distorter (a device used to improve the linearity of RF PA) to achieve fixed efficiency and gain. On the other hand, Si LDMOS is very sensitive to the changes in temperature and even with PD adaptive control, the gain and output efficiency of Si LDMOS varies by about 2.6 dB and 3 %, respectively. Hence, GaN HEMT is good candidate for use in high efficiency Radio Frequency (RF) PA.

Furthermore, owing to high breakdown voltage, GaN HEMTs can operate at high drain bias voltage [14]. For the same amount of the output power, the power, I^2R, wasted on parasitic resistance would be lowered in PA with higher drain bias voltage compared to PA with lower drain bias voltage. Hence, it increases efficiency and simplifies the cooling system which is an important advantage since the cost and weight of cooling system has very high impact on the cost of high power RF transmitter [14]. With high efficiency, GaN HEMT based PA would operate at lower temperature, hence, reducing power consumption, increasing reliability and life expectancy.

1.3 Challenges and motivations

Even though GaN based HEMTs have superior quality over Si based LDMOS, there are challenges that need to be addressed for HEMTs before they can replace MOSFET. The important challenges are related to cost, high gate leakage current and thermal stability, and device performance improvement.

1.3.1 Cost

Firstly, cost is the challenge for GaN based HEMTs to compete with other semiconductor devices (e.g., Si-based). However, with the availability of GaN based heterostructures grown on Si(111) wafer with excellent quality, low cost and high performance GaN based HEMTs become feasible. If the fabrication of GaN-on-Si HEMTs can be processed in existing Si fabrication foundries, the making of GaN-on-Si HEMTs can be made more cost competitive. Furthermore, with the availability of large Si substrate (> 100 mm diameter), Hahn et al. [29] have reported the enhancement mode 1.0 μm gate $Al_xGa_{1-x}N$/GaN HEMT on 150 mm diameter Si substrate with the extrinsic transconductance of 366 mS/mm using a recessed gate process. In addition, a few groups have recently reported on the realization of $Al_xGa_{1-x}N$/GaN heterostructures on Si(111) using Au-based contacts or Au-free contacts [30-36]. Therefore, with larger substrate (200 mm diameter), the fabrication cost per transistor could be further reduced. However, the conventional Au-based contacts is widely used in GaN based HEMT while gold acts as a deep level trap and fast diffuser in silicon which can degrade the Si based device performance; hence, it is strictly forbidden in Si CMOS foundries. In addition,

gold is an expensive material which would add cost to the fabrication of HEMT.

Therefore, we aim to develop non-gold based Schottky contacts for GaN-based HEMTs on Si (111) substrate to make them CMOS compatible to reduce the fabrication cost.

1.3.2 Gate Leakage and Thermal Stability

Another major factor that limits HEMT performance is the high Schottky gate leakage current (I_G) [37-39]. When a Schottky diode is forward biased, the current flowing through it depends exponentially on the forward biased voltage. Therefore, if a Schottky contact is used as the gate in HEMTs, the leakage current from the gate, I_G, will depend exponentially on the gate to source voltage, V_{GS}. This is depicted by a typical I_G-V_{GS} curve (at a fixed V_{DS}) of a Schottky gate HEMT shown in Figure 1.5. Hence, there is a maximum V_{GS} voltage (typically 2 to 3 V) above which the gate leakage will be too high and will increase the leakage loss and power consumption. Hence, the drain current, I_D, will be limited due to the constraint on V_{GS}.

A typical I_D-V_{GS} (at a fixed V_{DS}) curve is also shown in Figure 1.5. In the 'OFF" state of HEMT, the drain current, I_{OFF}, is mostly dominated by I_G, where I_G is the sum of gate to drain current, I_{GD} and gate to source current, I_{GS}. Since $|V_{GD}| > |V_{GS}|$ in the OFF state, I_G is dominated by I_{GD}. Hence, the gate reverse breakdown voltage is mainly determined by V_{GD}. Therefore, this limits the maximum drain bias voltage[40]. In addition to the limitation of drain and gate

voltages, the large Schottky gate leakage current can lead to a higher power consumption, smaller gate voltage swing and reduced device lifetime.

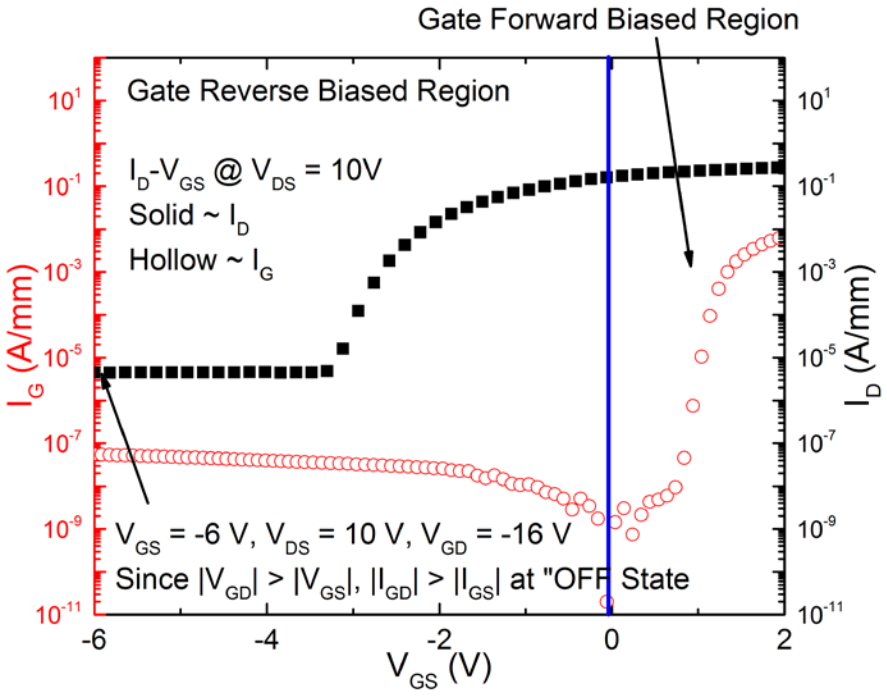

Figure 1.5 Typical I_D-V_{GS} and I_G-V_{GS} curves of Schottky gate HEMT.

Chen et al. [41] reported that the leakage current of the Schottky gate contact was due to the combination of several contributing components such as thermionic emission, generation recombination current, and tunneling current. At low bias voltage, the contribution of tunneling current dominates. This tunneling current resulted from the presence of dislocations in AlGaN/GaN and InAlN/GaN heterostructures [42, 43].

Many methods have been explored to reduce the gate leakage current of HEMTs. One of them is to use a high work function Schottky gate. To date, a number of high work function Schottky contacts to AlGaN/GaN heterostructure have been studied. Table 1.5 summarizes the properties of a

selection of commonly used Schottky contacts to AlGaN/GaN heterostructure. As shown in Table 1.5, high work function elemental metals such as Pt, Ni, Ir, and Pd can yield Schottky Barrier Height (SBH) higher than 0.85 eV after annealing at a temperature (typically less than 500^{o}C). However, their leakage current was reported to increase upon high temperature heat treatment (above 500^{o}C). Furthermore, the reverse leakage current of these contacts increased above 10^{-4} Acm^{-2} when annealed at above 500^{o}C which made them not suitable for use in high temperature applications. Most Schottky contacts listed in Table 1.5, except RuO_2, suffer from degradation of leakage current after annealing above 600^{o}C. Hence, RuO_2 may be a good Schottky gate candidate for high temperature applications.

One of the benefits of thermally robust gate is that HEMTs could be fabricated using the gate-first process (see Figure 1.4) where high temperature heat treatment (> 700^{o}C) is needed to form Ohmic contacts. HEMTs using conventional Ni/Au Schottky contact have to use either a dummy gate for gate-first process or gate-last process due to the increased reverse leakage current after the high temperature annealing to form Ohmic contacts. In contrast, a thermally robust gate allows the use of the gate-first self-aligned process, as shown in Figure 1.6, which is necessary to reduce transistor access resistances. Such a gate formation also requires fewer processing steps compared to the self-aligned gate-last process using dummy gate, as shown in Figure 1.7, thus reducing the fabrication cost [44, 45]. In addition, thermally robust HEMTs could be used in high temperature applications, for example, power converter for electric vehicle and geothermal plant.

Therefore, another motivation of our research is to develop thermally robust Schottky contacts with lower leakage current compared to traditional Ni/Au Schottky contacts on GaN based heterostructures. The thermally robust Schottky contacts should be CMOS compatible.

Table 1.5 Metal and alloy Schottky contacts to AlGaN/GaN Heterostructure

Metals/ Alloys	**Work Function** (eV)	**Schottky Barrier Height (SBH)** (eV)		**Annealing Temp above which the Reverse Leakage Current > 10^{-4} Acm^{-2} at -2 V**(^{o}C)	Ref
		No Anneal	Maximum (Annealing Temp)		
Pt	5.7	0.88	0.85 (300 ^{o}C)	-	[46]
Ir	5.27	0.68	0.85 (500 ^{o}C)	500	[46]
Ni	5.2	0.97	1.09 (300 ^{o}C)	500	[47]
Pd	5.1	0.95	1.23 (300 ^{o}C)	450	[47]
W	4.6	0.89	-	-	[48]
Pt/Ti/Au	5.65/4.33/5.1	0.65	1.05 (360 ^{o}C)	-	[49]
Ni/Au	5.15/5.1	0.59	0.65 (500 ^{o}C)	500	[50]
Ni/Pt/Au	5.15/5.65/5.1	0.57	0.74 (500 ^{o}C)	500	[51]
WN_x	-	-	1.21	600	[48]
RuO_2	5.1	0.56	1.1 (500 ^{o}C)	700	[52]

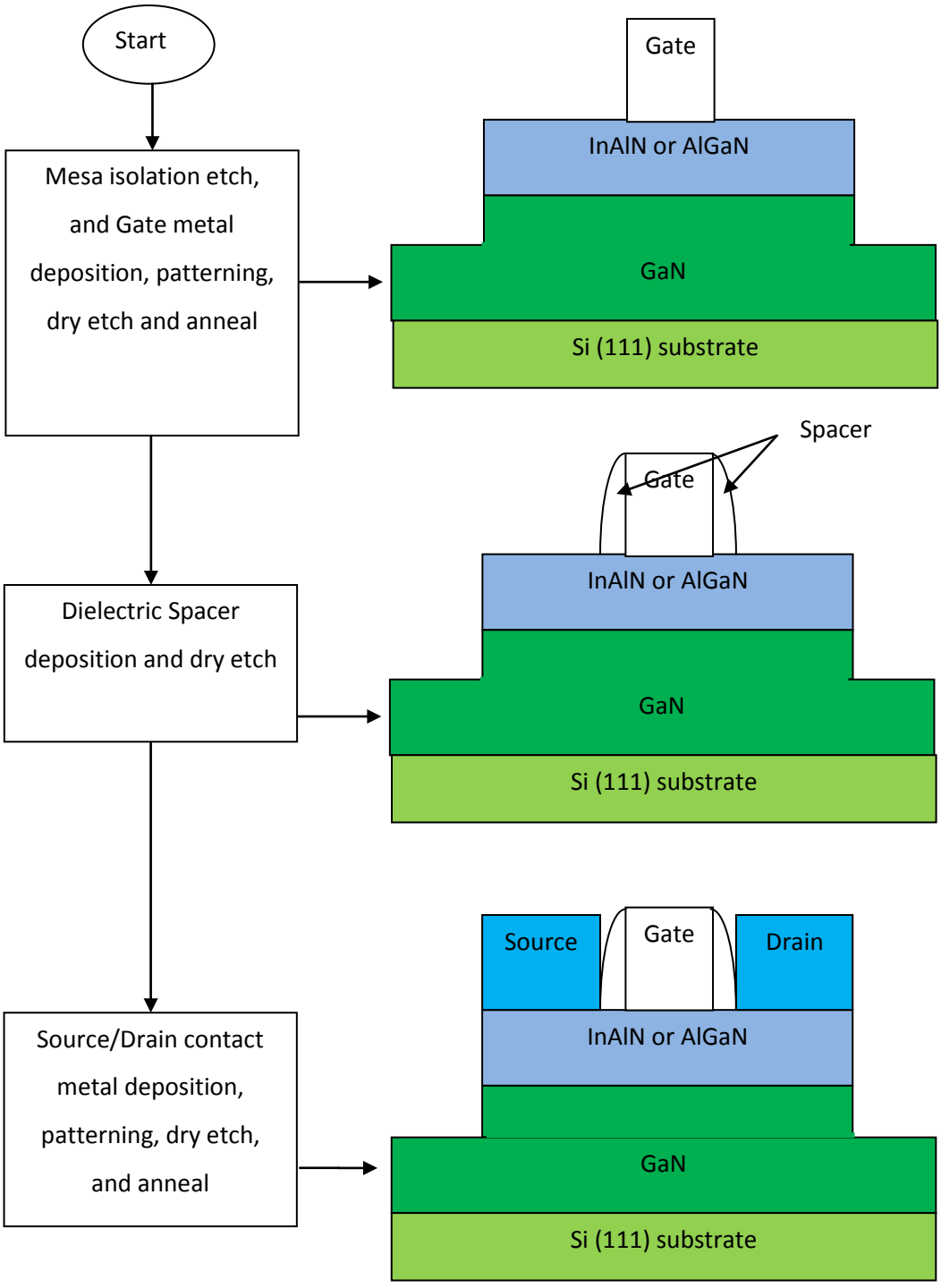

Figure 1.6 Schematics of self-aligned gate first process flow

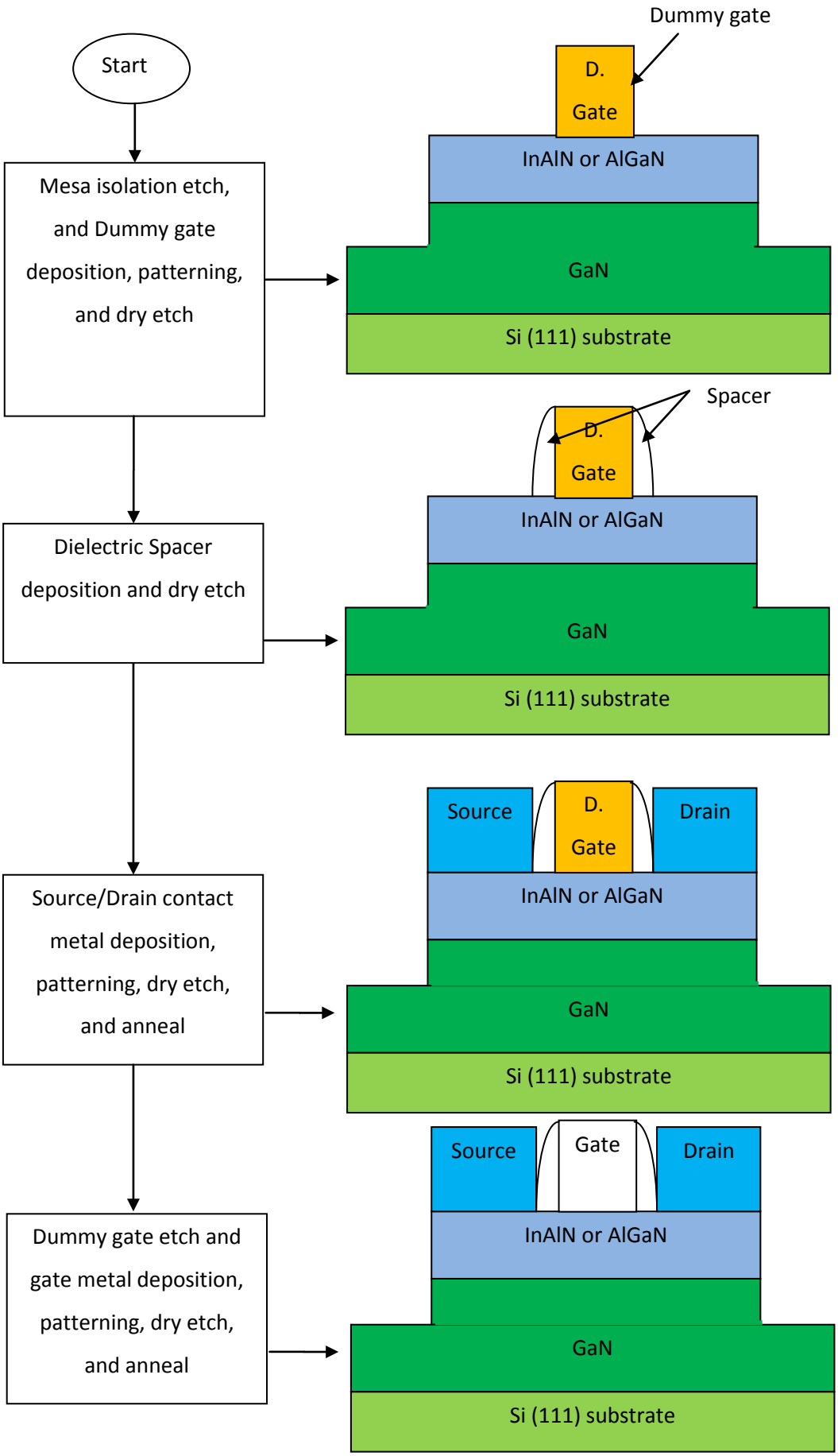

Figure 1.7 Schematics of self-aligned gate-last process using dummy gate

1.3.3 Self heating and thermal conductivities of GaN based HEMTs

The reliability of GaN based HEMTs is directly dependent on self heating effect like any others semiconductor. Hence, it is vital to determine the channel operating temperature profile under the specific bias condition. In addition it is equally important to understand the thermal resistance of GaN based HEMTs grown on Si(111). Proper thermal management is significant for GaN-based HEMT devices since self-heating effects under high power and high-frequency operation significantly impact device performance and reliability. Since most of the heat is generated around the region at the edge of the gate contact between the gate and drain [53], high spatial resolution is necessary for temperature profiling of the active region of HEMTs. Several experimental probes are commonly used to measure temperature profiles of biased HEMT devices, such as IR thermal imaging [54], as well as micro-Raman [55] and micro-Photoluminescence (μ-PL)[56] spectroscopy. Among them, micro-Raman and micro-Photoluminescence (μ-PL) provide high spatial resolution and ability to probe at the nucleation and Si interface in addition to channel temperature [57-60]. However, even with the availability of these optical spectroscopies for probing GaN based HEMT temperature, the conventional gate, Ni/Au, would not allow probing of channel temperature underneath the gate due to its opaque nature to the visible light and ultraviolet. In order to probe the channel temperature underneath the gate, transparent or semitransparent gate is necessary. As discussed in previous sub-section, RuO_2 has a potential to be used as a gate due to its low leakage current and high temperature stability. In addition, the thin RuO_2 layer is semitransparent to the

visible light and ultraviolet light since its has a band gap of 2.2 to 2.4 eV [61, 62].

Therefore, the last motivation of our research is to study the self heating effect and temperature profile of AlGaN/GaN and InAlN/GaN HEMTs on Si(111) under the bias condition with semi-transparent gate.

In summary, our motivation is to develop and investigate the performance of thermally robust CMOS compatible Schottky contacts for AlGaN/GaN and InAlN/GaN diodes and HEMTs grown on Si(111). We also aim to study the thermal performances and profiles of those HEMTs under biased to study the self heating effect.

1.4 Synopsis of the thesis

With the objectives and overview of the project described above, this thesis is organized as follows.

Chapter 2 gives a brief introduction to the physics and the operation principles of GaN based HEMTs. The fabrication and characterization techniques used in this work are also described. This chapter provides the theoretical background and experimental fundamentals in this project.

In Chapter 3, the preliminary investigations of Ni/W Schottky contacts on InAlN/GaN are first presented. To achieve Au-free contact with good surface roughness, W based contacts are used and optimized using Schottky diode structure. The DC characteristics of Ni/W based InAlN/GaN HEMTs on Si(111) was demonstrated.

In Chapter 4, we discuss the studies of thermally robust RuO_x Schottky contact to n-doped GaN and InAlN/GaN heterostructure grown on Si(111) substrate. A comparison, in terms of electrical performance and thermal stability, between RuO_x and Ni/Au Schottky contacts is also included. Furthermore, the electrical characteristic of RuO_x Schottky gate HEMT on InAlN/GaN will be discussed.

In Chapter 5, we study the effect of annealing temperature on the electrical characteristic of the thermally robust RuO_x Schottky gate AlGaN/GaN HEMTs grown on 200 mm diameter Si(111) substrate.

Chapter 6 provides the one dimension thermography of semi transparent RuO_x Schottky gate AlGaN/GaN and InAlN/GaN HEMTs using optical spectroscopy. The channel temperature are experimentally extracted from source to drain including the region underneath the transparent RuO_x gate where the maximum temperature occurs. In addition, we highlight the temperature of GaN buffer and nucleation layer AlN/Si interface.

In Chapter 7, we report the studies of annealing ambient and pressure effects on electrical and material characteristics of the thermally robust RuO_x Schottky contact on InAlN/GaN heterostructure grown on Si(111).

In Chapter 8, we demonstrate of the performance of RuO_x Schottky contact on InAlN/GaN HEMTs using a single annealed process in comparison with InAlN/GaN HEMTs using a conventional gate last process.

Lastly, in Chapter 9, a summary of this work is provided, followed by suggestions of the potential research to further develop this work.

Chapter 2: Physics in GaN-based devices, fabrication and characterization techniques

This chapter provides the theoretical background of the current study and also describes processes and apparatus that are employed for device fabrication and testing throughout this thesis including transmission line method (TLM), Hall Effect measurement, micro-photoluminescence spectroscopy, micro-Raman spectroscopy, X-ray diffraction measurement (XRD), secondary ion mass spectrometry (SIMS), transmission electron microscopy (TEM), and atomic force microscopy (AFM).

2.1 Physics in GaN-based devices

2.1.1 Schottky contacts

Schottky contact is a rectifying metal semiconductor contact which allows current flow in forward biased condition while it prevents current flow in reverse biased condition. A Schottky contact is used as a gate in GaN based HEMTs to control the electron carrier concentration in the channel. A good Schottky contact is desired for realization of HEMTs with excellent performance and reliability. Schottky contact is characterized by Schottky Barrier Height (SBH). According to Schottky and Mott [63], this Schottky barrier Height (SBH) is related to the difference between the work function of the metal and the electron affinity of the semiconductor and is defined by Eq. (2.1), where $\Phi_b, \Phi_{\mathrm{m}}$ and χ_s, are the SBH, the metal work function, electron affinity of the semiconductor, respectively.

$$\Phi_b = \Phi_m - \chi_s \tag{2.1}$$

On the other hand, Bardeen[64] has reported that the fermi level pinning phenomenon could arise if there were a large number of surface or interface charged states (>10^{12} states cm^{-2}) resulting in a weak dependence of SBH on the work function of the metal.

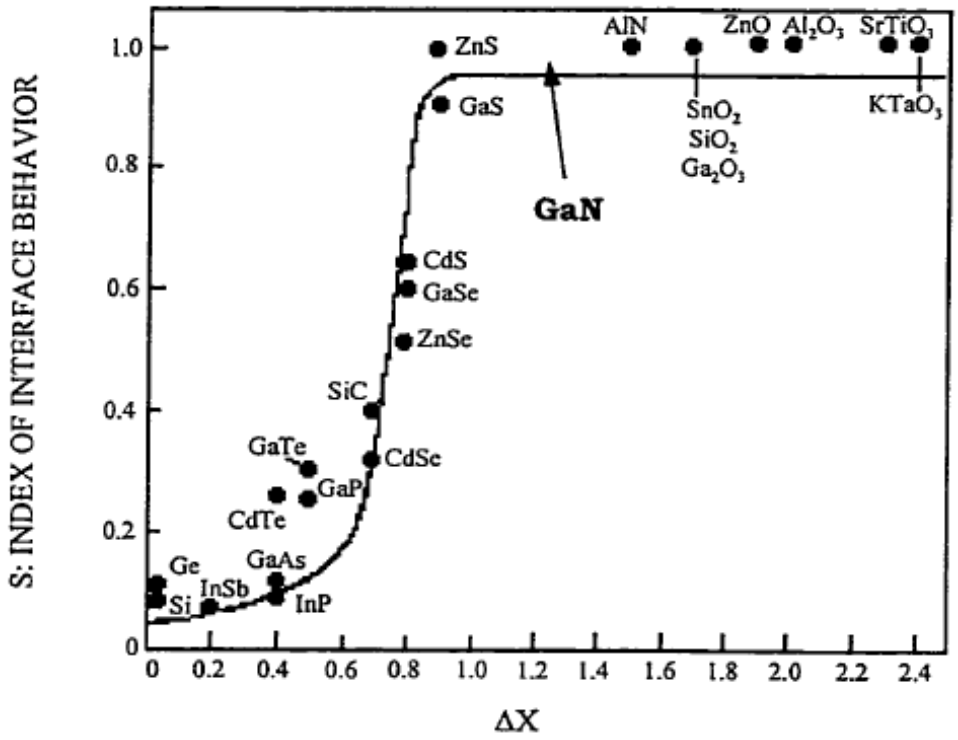

Figure 2.1 Index of interface behavior of various semiconductors versus the difference in electronegativity of their constituent elements [65].

However, resulting from the large amount of ionic bonds in GaN based semiconductor, the metal contacts to GaN based semiconductor have a strong correlation of SBH with the work function of the metal contacts. As shown in Figure 2.1, Kurtin et al [65] reported that the index of interface behavior (S), which is related to Fermi level pinning factor, increases when the difference in electronegativity of constituent elements in compound semiconductors reaches

more than 0.9. GaN and AlN has more than 0.9 Pauling electronegativity difference[66], as shown in Figure 2.1, which means that there is an insignificant fermi level pinning effect and barrier height is mainly attributed by the workfunction difference between metal and GaN.

2.1.2 Operation principle of GaN HEMTs

The most important feature of GaN HEMTs is the high sheet concentration and high mobility of carriers confined at the interface of the heterostructure, which is known to be resulted from strong spontaneous and piezoelectric polarization field in GaN based materials[67]. Figure 2.2 depicts the conduction band diagram of the InAlN/GaN heterostructure with an AlN spacer and the formation of 2DEG. If two semiconductors (e.g., InAlN and GaN) with different bandgaps are joined together to form heterojunction, discontinuity occurs in the conduction band edge resulting in a triangle quantum potential well at the heterostructure interface, as shown in Figure 2.2. The polarization induced electrons will accumulate in this potential well forming the sheet charge, analogous to the inversion layer formation at/near Si/SiO_2 interface. The thickness of this channel is typically only several nanometers, which is much smaller than the de Broglie wavelength of the electrons in GaN given by $\lambda = h/\sqrt{2k_B T m_n^*}$, where m_n^* is the effective electron mass of GaN, h is the Plank constant, k_B is the Boltzmann's constant and T is the temperature. Hence, the electrons are quantized in a two-dimensional system at the interface, and the channel is in the form of a 2DEG.

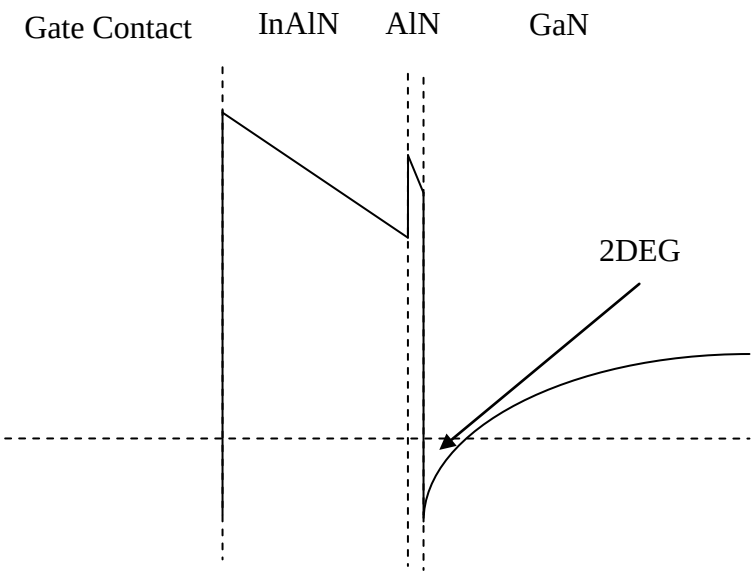

Figure 2.2 Conduction band diagram of InAlN/GaN heterostructure with an AlN spacer.

Figure 2.3 illustrates a schematic showing the cross-section of a typical AlGaN/GaN and InAlN//GaN HEMT structure. In AlGaN/GaN HEMTs, the source and drain Ohmic contacts are typically recessed to reduce contact resistance while in InAlN/GaN HEMTs, the source and drain Ohmic contacts are not recessed. This is owing to the thinner thickness of InAlN in the latter HEMTs than that of AlGaN in the former HEMTs. In both cases, the source is typically grounded while a positive bias is applied to the drain; hence, electrons in the 2DEG channel flow from source to drain. The voltage between the drain and source is named V_{DS}, while that between gate and source is named V_{GS}. The gate electrode can be a metal-semiconductor rectifying contact (i.e., Schottky contact) or metal oxide stack (i.e., MOS structure) or p-GaN. The gate voltage is used to control the charges in the 2DEG channel. The gate voltage required to turn off the channel is called the threshold voltage (V_{TH}). There are two types of mode in HEMTs namely depletion mode (D-mode) and enhancement mode (E-mode). The former has a negative threshold

voltage while the latter has the positive threshold voltage. In our study, we focus on the D-mode GaN HEMTs, which means the channel is normally on and the gate is negatively biased to turn off the channel.

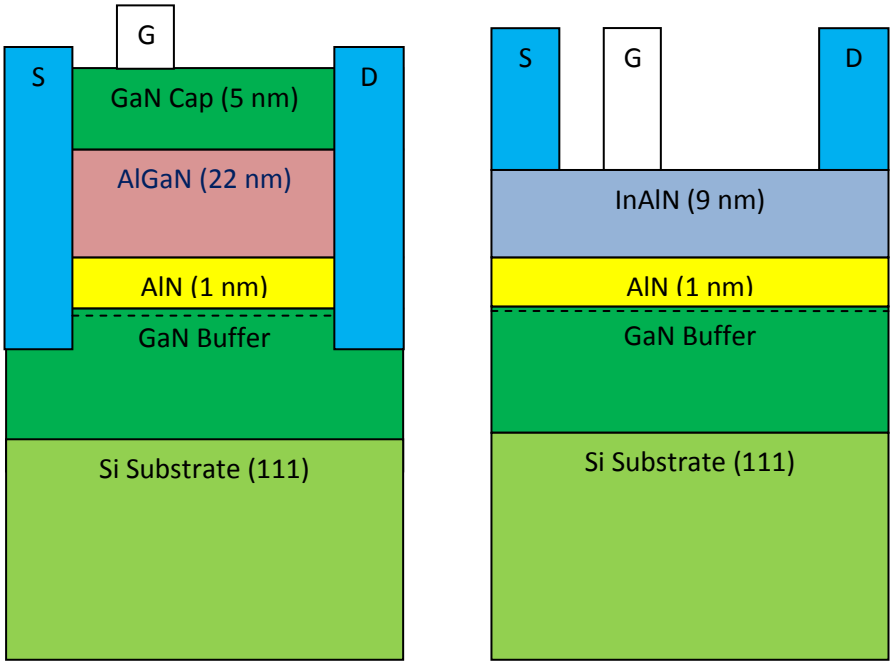

Figure 2.3 Cross-section of the typical AlGaN/GaN (left) and InAlN/GaN (right) HEMTs. S, D and G means source, drain and gate contact respectively. Recessed source and drain contacts are used in AlGaN/GaN HEMTs.

2.2 Device fabrication techniques

2.2.1 Sample preparation and cleaning process

Sample preparation began with dicing the n-GaN, InAlN/GaN and AlGaN/GaN wafers into small pieces by scribing the backside of the wafers with a diamond blade. The diced samples were then cleaned in acetone, followed by isopropyl alcohol (IPA) in an ultrasonic bath for 5 min to remove organic contaminations on the surface. The samples were then rinsed in deionized (DI) water and blown dry by nitrogen gun. Prior to the metal

deposition, the samples were dipped in HCl: H_2O (1:10) solution for 30 s to remove the native oxide on the surface.

2.2.2 Device isolation process

Device isolation could be performed using either mesa isolation process [68-70] or implantation isolation process using ions such as O^+, N+, H^+ and Ar^+[71-74] in the fabrication of GaN based HEMTs. Although the latter process provides higher breakdown voltage and better isolation, the former process is more widely used in GaN based HEMT fabrication due to its simplicity[75, 76]. Mesa isolation process can be done using either dry etch process (Cl_2 based) or wet etch process. Due to GaN's chemical stability[77], the wet etch process for mesa isolation is not widely used. In our study, the mesa isolation process (dry etch) was employed. The mesa height needs to be carefully chosen to prevent leakage current between adjacent devices or testing structures. Mesa heights were chosen carefully for device isolation as the current barrier effectively, and to prevent any possible discontinuity between the gate finger and gate pad across the mesa step [78]. Due to the resistance of GaN-based material to chemical acids, dry etching by inductively coupled plasma-reactive ion etching (ICP-RIE) was used for isolation of mesa. In this study, the equipment used for ICP-RIE is Plasmalab System 100 Cobra III-V Etcher from Oxford. In mesa isolation dry etch process, it was reported that the gas mixture of BCl_3:Cl_2 provides the lowest isolation leakage current [79]. Our etching conditions were as follows: the etchant chemistry mixture ~ BCl_3:Cl_2 (20:10 sccm), the chiller temperature ~ 6 ^oC, the processing chamber pressure ~ 10 mTorr, RIE power ~ 50 W and ICP power ~ 100 W. The average etching rate is~22 nm per min for GaN based HEMTs.

2.2.3 Photolithography process

In this study, the photolithography was chosen to define the geometry of device and test structures. The photoresist used in the photolithography process was AZ5214E which can be used to form the positive pattern or negative pattern of the mask dependent on the post-baking process. The method of using AZ5214E to form the latter pattern is called the image reversal process. The most important parameter of the image reversal process is reversal-bake temperature. Once optimized, it must be kept constant within ± 1°C to maintain a consistent process. This temperature also has to be optimized individually. The optimized temperature typically falls within the range from 110 to 125°C. If the image reversal bake temperature is too high (> 130^{o}C), the photoresist will also thermally crosslink in unexposed areas, hence, giving no pattern formation. Normally, the image reversal process includes: 1) normal exposure with mask, 2) post baking on hotplate, and 3) flood exposure without any masking procedure. In the study, we used AZ5214E photoresist to form the positive pattern for mesa isolation etch, while negative pattern of the mask (image reversal process) for metal lift-off process. It is worth mentioning that using this image reversal process, undercut structure can be formed, thus facilitating the lift-off process. As we know, due to the UV absorption of the photoactive compound, the UV light is attenuated when penetrating through photoresist layer during the UV exposure to positive photoresist. This causes a higher dissolution rate at the top and a lower rate at the bottom of the photoresist resulting in a positive slope as shown in Figure 2.4. With the image reversal process, this condition is reversed as higher exposed areas will

be crosslinked to a higher degree than those with lower dose, thus forming an undercut structure ideally suited for lift-off.

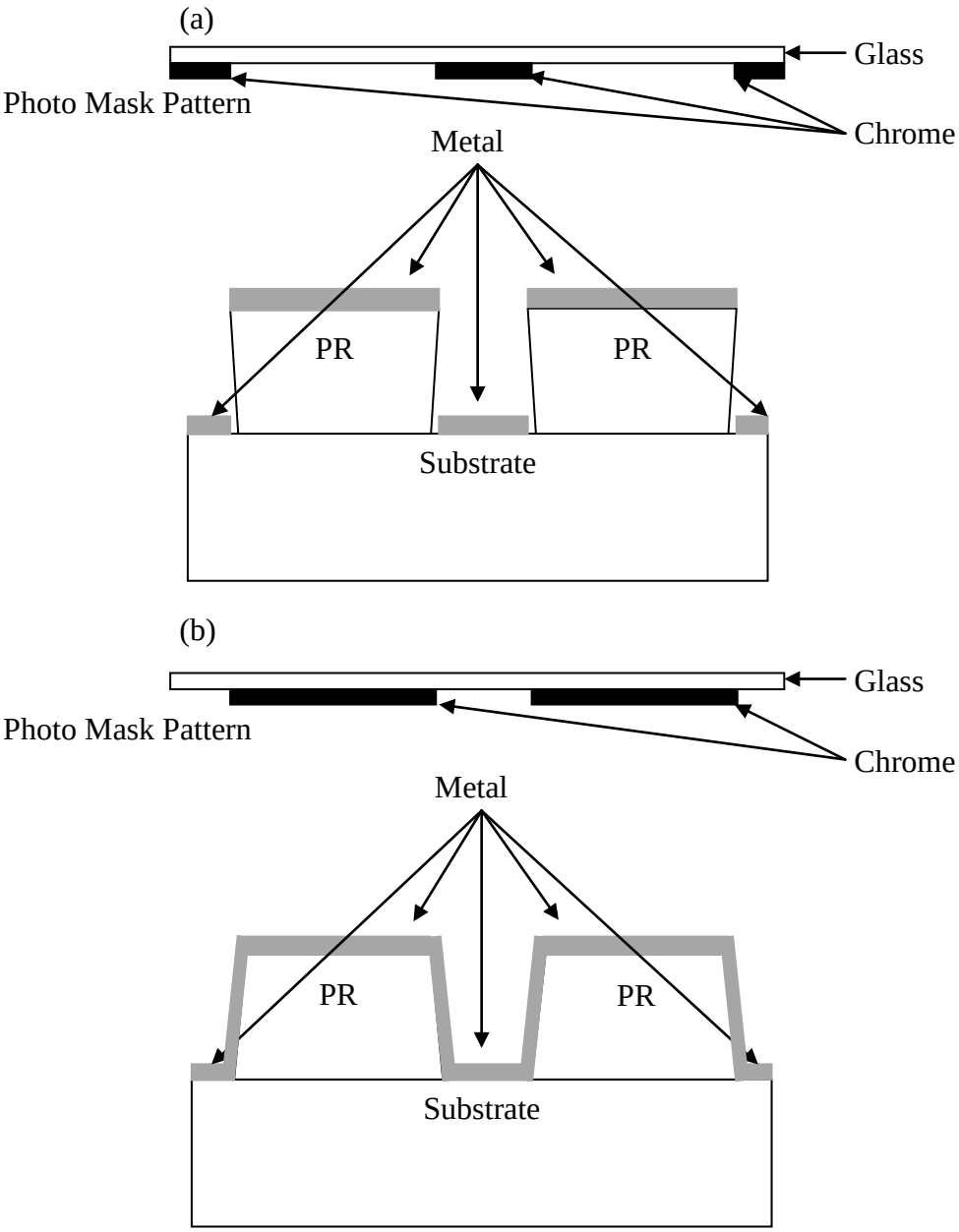

Figure 2.4 Schematic drawing showing the comparison of metal lift off process between (a) negative pattern (image reversal process) and (b) positive pattern. It is to be noted that in order to obtain the same pattern on the substrate, the mask patterns of these two processes are in reverse.

The procedures for our photolithography process are summarized as follows. After the sample cleaning as stated in Section 2.2.1, the photoresist is spin-

coated onto the wafer surface with a ramp up acceleration of 1000 rpm per 1 sec for 5 sec, a constant spinning speed at 5000 rpm for 30 s and the ramp down deceleration of 1000 rpm per 1 sec for 5 sec duration. This results in a photoresist thickness of ~1.3 μm. After the spin coating step, the sample is soft-baked at 105 ^{o}C for 5 min on a hotplate to remove the solvent from the photoresist and to increase its adhesion to the wafer. Then, the sample is aligned with respect to the mask in a Karl Suss MA6/MA8 aligner machine using the hard contact mode. The photoresist is exposed to the UV light (~4 W/cm^2) for 10 s. After the first exposure, the sample is post-baked at 110^{o}C for 1 min on a hotplate, followed by a flood exposure for 40 s. Lastly, the sample is developed in diluted AZ developer with DI water (1:1) for 50 s, then rinsed in DI water and dried by nitrogen gun.

2.2.4 Ohmic and Schottky metallization process

Metallization schemes for the ohmic and gate contacts were deposited by two techniques: electron beam (e-beam) evaporation and DC magnetron sputtering, respectively. A BOC Edwards multi-hearth e-beam evaporator was used for many of the depositions. The equipment is capable of 3 kW, has a rotating sample stage and a four-stage hearth with each crucible being 4 cc in capacity. High purity metals are added to graphite crucibles as metal sources.

For sputtered deposition, a Denton vacuum system, with DC magnetron heads, each able to hold a circular 3 inch diameter target with 0.125 inch thickness was used. The transition metals that require sputter deposition were Hf, Ti, Al, Ni, W, Ta and Ru. The sample was secured to a sample holder on a rotating stage during the deposition. The Ohmic metal deposition such as Ti, Al, Ni, Hf,

Ta and W was conducted at a power of ~200 W, in the ambient of Ar with the flow rate of 10 sccm Ar. For the Schottky metal deposition (RuO_x), Ru was sputtered at a power of ~50 W, in the ambient of Ar and O_2 with the flow rate of 20:10 sccm. Both metal depositions were conducted at the ambient pressure in the order of 10^{-3} Torr and at room temperature.

2.2.5 Lift-off process

In the study, the lift-off process was used for patterning deposited metal films, which refers to creating pattern of a target material on the surface of a substrate by means of using a sacrificial material (photoresist). In this thesis, the substrate is GaN based wafers and the sacrificial material is AZ5214E photoresist. Lift-off process was conducted after the metal deposition by e-beam evaporator or sputtering. During the lift-off process, the remaining photoresist would dissolve in acetone in an ultrasonic bath, effectively lifting-off the metal layer on top of it, thus forming the desired metal pattern. As mentioned in Section 2.2.3, the image reversal process causes the undercut structure which is ideal for lift off process.

2.2.6 Thermal annealing process

Thermal annealing is used to realize Ohmic contacts and Schottky contacts to improve their electrical properties. The annealing ambient can be vacuum, nitrogen (N_2) or Ar. If vacuum is used, the pressure is pumped down to ~6.67×10^{-3} Pa. If N_2 or Ar is used, the pressure is ~101.3 kPa. The equipment used in this study is ULVAC MILA-3000 Mini-lamp annealing system. The temperature ramping up and down rate is normally set to about 15^{o}C/s.

2.3 Characterization methods

2.3.1 Transmission line method (TLM)

Transmission line method (TLM) is a universal technique to study contact electrical properties and extract sheet resistance of substrate, contact resistance and specific contact resistivity. There are two types of structures namely, Circular TLM (CTLM) and Linear TLM (LTLM). The former is easier to fabricate since no additional isolation is needed while the latter is more accurate.

Circular Transmission Line Method (CTLM) test structure [80] is used in our experiments to measure the specific contact resistivity of ohmic contacts to GaN based HEMTs. A typical circular test structures consists of a circular inner region of radius *L*, a gap of width *d*, and a conducting outer region, as shown in Figure 2.5. The gap typically varies form a few microns to tens of microns. For equal sheet resistances under the metal and in the gap, and for the geometry of the circular contact resistance structure in Figure 2.5, the total resistance (R_T) between the internal and the external contacts[80]is

$$R_T = \frac{R_{sh}}{2\pi}\left[\frac{L_T}{L}\frac{I_0(L/L_T)}{I_1(L/L_T)} + \frac{L_T}{L+d}\frac{K_0(L/L_T)}{K_1(L/L_T)} + \ln\left(1+\frac{d}{L}\right)\right] \quad (2.2)$$

whereR_{sh} is the sheet resistance of the substrate, $L_T$is the transfer length, and the remaining parameters, I_0, I_1, K_0 and K_1, denote the modified Bessel functions of the first order. For $L >> 4L_T$, the Bessel function ratios I_0/I_1 and K_0/K_1 can be approximated by 1 and $R_T$then becomes

$$R_T = \frac{R_{sh}}{2\pi}\left[\frac{L_T}{L} + \frac{L_T}{L+d} + \ln\left(1+\frac{d}{L}\right)\right] \quad (2.3)$$

In the circular transmission line test structure in Figure 2.5, for *L*>>*d*, Eq. (2.3) simplifies to

$$R_T = \frac{R_{sh}}{2\pi L}(d + 2L_T) \tag{2.4}$$

From Eq. (2.4), a linear relationship is seen between R_T and *d*. By plotting R_T with respect to *d*, a straight line is expected with an intercept with the R_T −axis at c $= \frac{R_{sh}L_T}{\pi L}$, and a gradient of $g = \frac{R_{sh}}{2\pi L}$. From the gradient, the sheet resistance of the semiconductor (R_{sh}) can be determined, which then allows the transfer length (L_T) to be calculated from the R_T −axis intercept.

With R_{sh} and L_T, the specific contact resistivity (ρ_c) can be determined as given by

$$\rho_c = R_{sh}L_T^2 = (\pi L\, c^2)/(2g) \tag{2.5}$$

In our experiment, the CTLM structure consists of ring patterns with *L* of 90 μm and *d* of 5, 10, 15, 25, 35 and 45 μm, as shown in Figure 2.5.

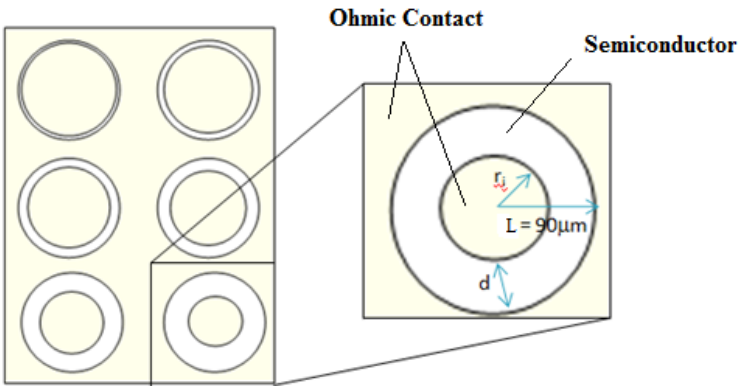

Figure 2.5 Circular transmission line method (CTLM) test structure.

Linear transmission line method (LTLM)[81] test structure consists of several contacts with different spacings between adjacent contacts, as shown in Figure 2.6. For contacts with $L \geq 1.5\ L_T$, the total resistance [81] between any two contacts is given by

$$R_T = \frac{R_{sh}\, d}{Z} + 2R_c \approx \frac{R_{sh}}{Z}(d + 2L_T) \tag{2.6}$$

where R_c is the contact resistance. The total resistance (R_T) is measured between adjacent contacts with various contact spacing. Similar to the CTLM, by plotting R_T versus d, a straight line will intercept R_T-axis at $\mathrm{c} = 2R_c = \frac{2R_{sh}L_T}{Z}$, with a gradient of $g = \frac{R_{sh}}{Z}$ and $L_T = \sqrt{\rho_c / R_{sh}}$. The specific contact resistance for LTLM test structure can be determined as follows,

$$\rho_c = R_{sh} L_T^2 = Z\, R_c^2 / g \tag{2.7}$$

Thus, sheet resistance, contact resistance and specific contact resistivity can be extracted from the R_T-d plot. In our experiment, the LTLM structure consists of d varies from 5, 10, 15, 25, 35, 45, 60, 75, to 90 μm, as shown in Figure 2.6.

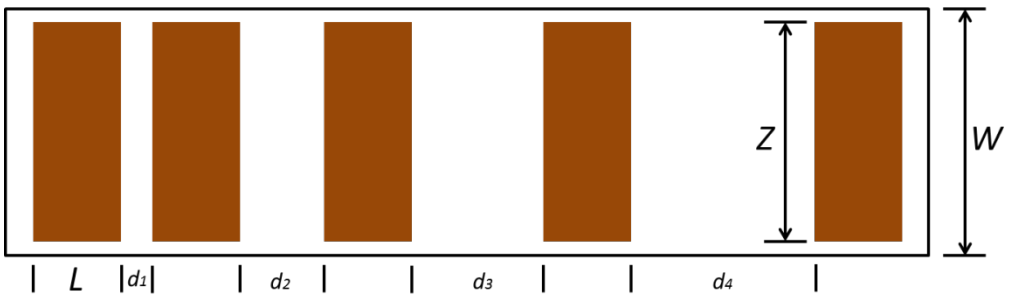

Figure 2.6 Linear transmission line method test structure with various spacing d. Z is the width of the contact pad and W is the width of the mesa isolation.

2.3.2 Schottky Barrier Height (SBH) extraction using Thermionic Emission Model

The thermionic current-voltage (*I-V*) relationship of a Schottky diode [47], neglecting series and shunt resistance, is given by

$$J = A^{*}T^{2}e^{\left(\frac{-q\Phi_B}{k_BT}\right)}e^{\left(\frac{qV}{nk_BT}\right)}\left(1 - e^{-\frac{qV}{k_BT}}\right) \tag{2.8}$$

where J is the current density, A^* is the effective Richardson constant, which has a theoretical value of 26.4 $Acm^{-2}K^{-2}$, 35.8 $Acm^{-2}K^{-2}$and 55.86 $Acm^{-2}K^{-2}$ for n-GaN[82], undoped AlGaN [83] and undoped InAlN [23] respectively. T is the absolute temperature, V is the applied voltage, k_B is the Boltzmann constant, n is the ideality factor and Φ_B is the SBH. By plotting $\ln(\frac{J}{1-e^{\frac{-qV}{k_BT}}})$ with respect to V, a linear relationship is obtained with a slope, $m = \frac{q}{nk_BT}$ and a y-intercept, $c = \ln(A^{*}T^{2}) - \frac{q\Phi_B}{k_BT}$. Therefore, the ideality factor and SBH can be determined from the slope and y-intercept, respectively.

2.3.3 Van der Pauw and Hall Effect measurement

Hall effect measurement[84] can be used to determine the sheet carrier density and type of the carrier (electrons or holes) of the semiconductor, while Van der Pauw measurement can be used to determine the sheet resistance of the semiconductor. Using these 2 techniques, the mobility of the carriers can be estimated. Although Hall effect measurement is a simple and low cost set up to measure the carrier density, there are theoretically seven prerequisites to ensure accurate measurment[85-87].

1. The sample must have a flat shape of uniform thickness.

2. The sample must not have any isolated holes.

3. The sample must be homogeneous and isotropic.

4. All four contacts must be located at the edges of the sample.

5. The area of contact of any individual contact should be at least an order of magnitude smaller than the area of the entire sample.

6. The metal semiconductor contact must be Ohmic.

7. The thickness of the sample must be much smaller than the length and width of the sample.

Figure 2.7 shows the sample shapes that are preferred, acceptable, and not recommended for Hall effect measurement.

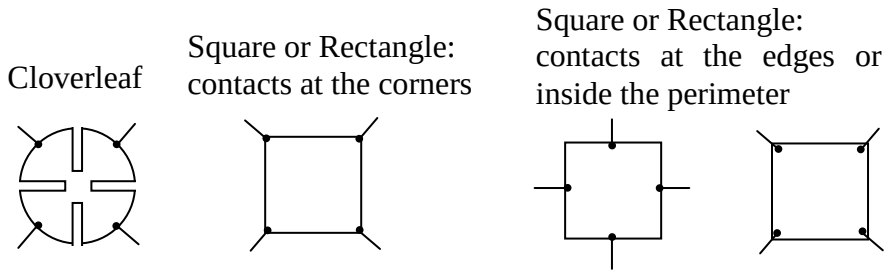

Figure 2.7 The sample shapes for Hall effect measurement.

Figure 2.8 shows the Hall voltage across a p- and n-semiconductor in the presence of current flow and a perpendicular magnetic field. As shown, the current is flowing in the positive-x direction and the magnetic field is applied in the negative-z direction. Since the force acting on the carriers due to the

magnetic field is $\vec{F} = q\,\vec{v} \times \vec{B}$, where v is the drift velocity, q is the carrier charge, and B is the magnetic field. The majority carriers in semiconductor will move to the positive-y direction. This results in an electric field in the negative-y direction for p-type semiconductor, and in the positive-y direction for n-type semiconductor. At equilibrium, Lorentz's force acting on the free carriers,

$$\vec{F} = q\,\vec{\varepsilon} + q\vec{v} \times \vec{B} = 0. \tag{2.9}$$

This gives rise to the Hall electric field -

$$\varepsilon_y = v_x B_z, \tag{2.10}$$

where B_z is the magnitude of the magnetic field. Since $v_x = \frac{J_x}{q n_s}$, where n_s is the bulk carrier density, Eq. (2.11) can be re-written as

$$n_s = \frac{J_x B_z}{q \varepsilon_y}. \tag{2.11}$$

Current Density (J_x) is given by $J_x = \frac{I_x}{W \times t}$ and Hall electric field is related to Hall voltage (V_H) by $\varepsilon_y = \frac{V_H}{W}$, where W and t are the width and thickness of the semiconductor sample respectively (see Figure 2.8). Therefore, Eq. (2.11) can be re-written as

$$n_{sh} = n_s \times t = \frac{I_x B_z}{q V_H}, \tag{2.12}$$

where n_{sh} is the sheet carrier density. Thus, with the knowledge of current (I_x), the Hall voltage (V_H) and the magnetic field (B_z), the sheet carrier density (n_{sh}) can be determined.

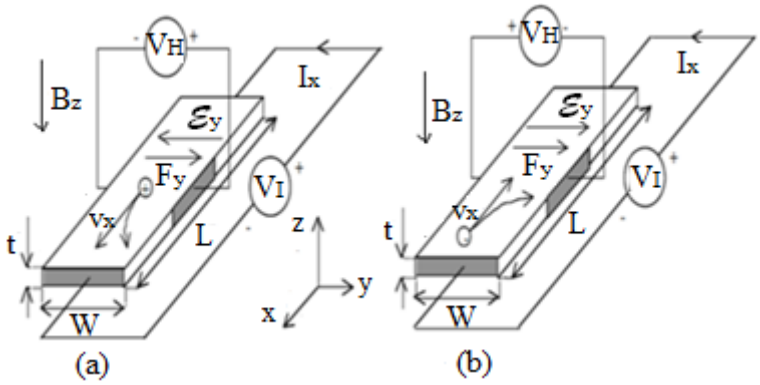

Figure 2.8 Hall voltage (V_H) owing the presence of current flow and a perpendicular magnetic field across (a) p-type semiconductor, and (b) n-type semiconductor.

The sheet resistivity (R_{sh}) of the semiconductor sample is determined using the Van der Pauw measurement given by

$$e^{\frac{R_A}{R_{sh}}} + e^{\frac{R_B}{R_{sh}}} = 1\,, \tag{2.13}$$

where R_A and R_B are the resistances measured in two orthogonal directions across the semiconductor sample, shown in Figure 2.9. The above expression can be solved numerically to give R_{sh}. With R_{sh} and n_{sh} from Hall effect measurement the carrier mobility (μ_s) can be determined by

$$\mu_s = \frac{1}{q n_{sh} R_{sh}}. \tag{2.14}$$

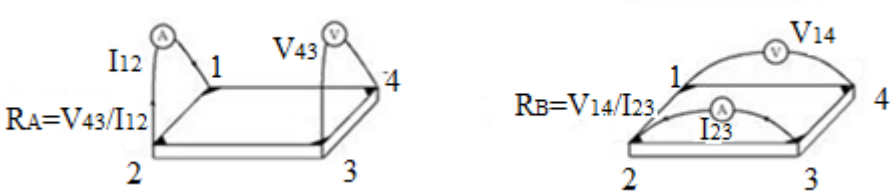

Figure 2.9 Van der Pauw resistance measurement[85]

2.3.4 Micro Photoluminescence Spectroscopy (μ- PL)

Micro-photoluminescence spectroscopy is a versatile, non-destructive, and widely used technique for material characterization. Photoluminescence is defined as the spontaneous emission of light from a material under optical excitation and can therefore be used to provide the detailed information on the wide variety of crystal defects, stress and temperature by applying an external photon with energy higher than the band gap energy and analyzing the re-radiated photons. Photoluminescence process typically includes three main phases[88], as shown in Figure 2.10:

(a) Excitation: Electrons absorb photon energy from external light source and excite to higher energy levels thus generating the electron hole pairs.

(b) Thermalization: Excited pairs relax towards quasi-thermal equilibrium distributions.

(c) Recombination: the thermalized electron hole pairs recombine radiatively to produce photons with an energy close to the bandgap energy of the materials.

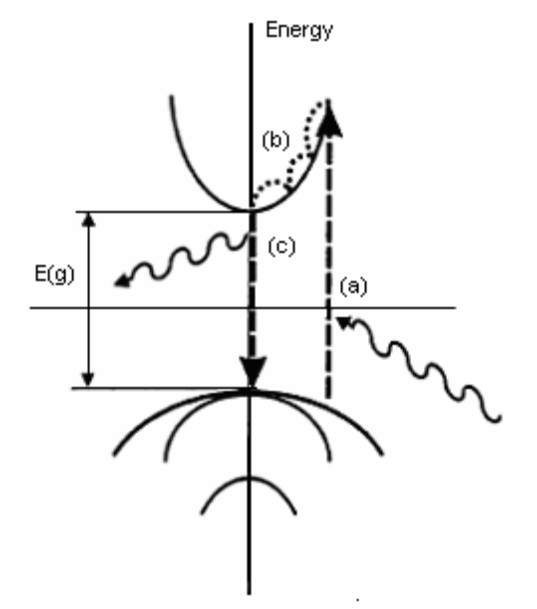

Figure 2.10 Photoluminescence process schematic. (a) Excitation. (b) Thermalization. (c) Radiative Recombination[89].

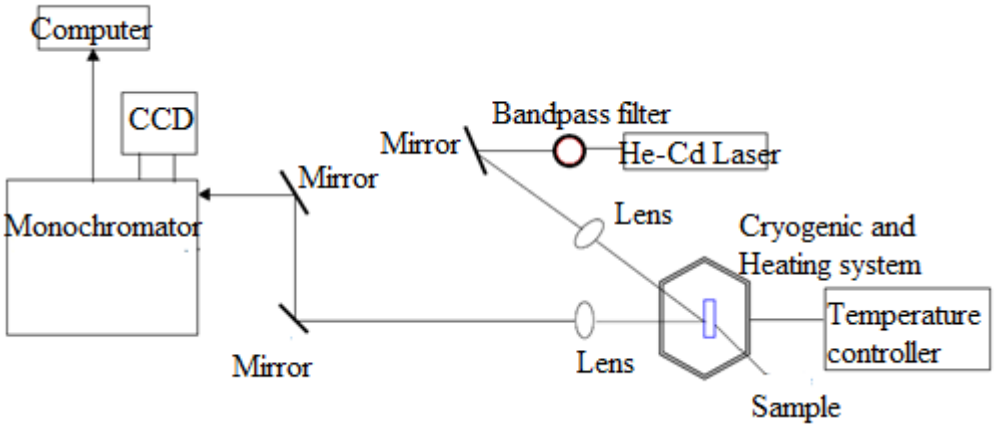

Figure 2.11 The schematic representation of simplified micro-Photoluminescence set-up[90]

Figure 2.11 illustrates the simplified photoluminescence setup. The setup consists of the light source, cryogenic and heating system, sample stage, lens, mirrors, monochromator, charge-coupling devices (CCD), and computer. The sample is excited with the light source(He-Cd laser)with emission lines in the UV spectrum (~325 nm). The cyrogenic and heating system was used to cool down or heat up the samples. The sample stage can be moved in resolution of

0.1 µm. The monochromator spectrally resolves the signal radiatively from the sample. The output signal was recorded in a computer. In our study, we used µ-PL to probe the channel temperature of the HEMTs under biased conditions.

2.3.5 Micro Raman Spectroscopy (µ-Raman)

Micro Raman Spectroscopy is a versatile, non-destructive, and widely used technique for characterization of the stress, defects and temperature of the sample [91]. As shown in Figure 2.12, µ-Raman relies on Raman scattering (Stokes or anti-Stokes scattering) of the incident photons from the laser source. These photons interact with phonons in the materials resulting in the re-radiated photon energy higher than or lower than that of the incident photons. This change in re-radiated photon energy gives information about the vibrational modes in the system. µ-Raman spectroscopy is similar to that of µ-PL as shown in Figure 2.11 except the light source which is Ar ions laser with the emission wavelength of 488 nm.

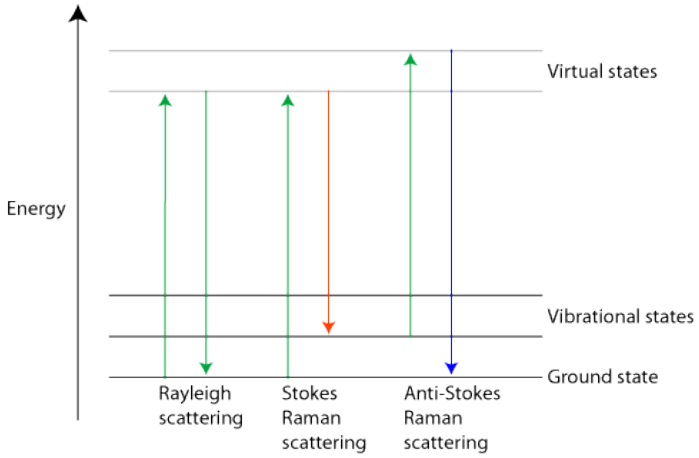

Figure 2.12 Scattering mechanisms in materials

2.3.6 X-ray Diffraction (XRD)

X-ray diffraction (XRD) is a well-developed, versatile non-destructive technique for material characterization used to provide the information on material, crystalline quality, lattice constant, alloy phase and composition of the sample.

The principle of XRD operation is the Bragg's law which is as follows.

$$2d_{hkl} \sin\theta = n\lambda \tag{2.15}$$

where d_{hkl} is the spacing of any lattice planes with Miller indices [92], θ is the corresponding Bragg's angle, n is an integer, and λ is the wavelength of the X-ray radiation. The relationship between lattice constants {h, k, l} and the plane spacing d_{hkl} can be precisely calculated with the following equation for wurtzite III-nitrides, where a and c are the lattice constants of the wurtzite III-nitrides.[92].

$$d_{hkl} = \frac{\sqrt{3}}{2}\left(\frac{h^2+k^2+hk}{a^2} + \frac{3l^2}{4c^2}\right)^{-\frac{1}{2}} \tag{2.16}$$

Thus, we can calculate the plane spacing, and thus the lattice constant by the Bragg angle θ and the X-ray wavelength. Accordingly, we can identify a particular phase by means of fitting both peak position and relative intensities which are corresponding to specific lattice plane and Miller indices of [92].

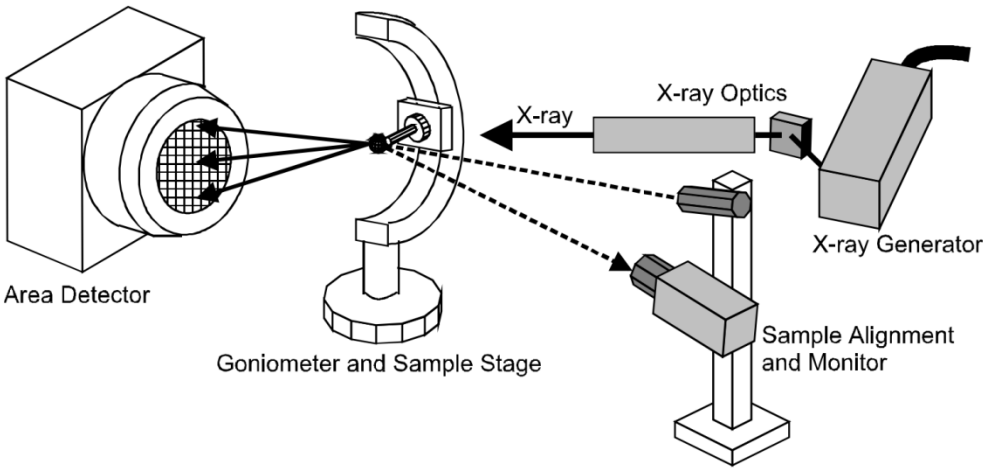

Figure 2.13Bruker D8 Discover with GADDS X-ray diffraction system.

A simplified schematic of a X-ray diffraction system (Bruker D8 Discover with GADDS XRD system) is shown in Figure 2.13. This system is used to characterize phase identification, phase quantification, texture, stress, high throughput screening faster with the use of 2 dimension detector. As seen, a X-ray diffractometer has an X-ray generator, X-ray optics, a goniometer and sample stage, a sample alignment and an X-ray area detector. X-ray generated from X-ray generator (Cu X-ray sealed tube) reflects from the flat graphite monochromator to obtain single K wavelength of 1.5418 A. This X-ray then passes through the double pin-hole collimator which is used to control the beam size and divergence before incident to the sample. When the X-ray diffractometer is working, the X-ray beam is focused on the sample mounted on the stage at certain angle of θ, while 2D X-ray detector placed on the opposite side 2θ away from the incident path of. When the measurement is continued, the incident angle is increased over time while the detector angel always keeps 2θ above the source path to receive the signals. We used this

XRD system to identify the phase formation of the contact metals and understand the reaction between contact metals and semiconductor substrate.

2.3.7 Transmission Electron Microscopy (TEM)

The transmission electron microscopy (TEM) is a powerful technique capable of imaging the materials in atomic resolution. Analogous to the optical microscopy, the TEM comprises lens to magnify the image of the sample. Nevertheless, the transmission electron microscope has higher resolution close to 0.08 nm owing to the smaller numerical aperture and shorter wavelength compared to the optical microscope. Figure 2.14 shows the schematic illustration of a typical transmission electron microscope. As shown in Figure 2.14, electrons generated from an source are accelerated by high voltage (typically 100 to 400 kV) and focused on the sample through a few sets of condenser lenses. The sample is prepared to be very thin in the order of several tens to several hundreds of nm to allow the electron beam to penetrate transparently and reduce the chance of spreading and is placed on a small copper grid with a few millimeters diameter,. The transmitted and forward scattered electrons produce a magnified image in the image plane and a diffraction pattern indicates the structural information in the back focal plane. The transmission electron microscope is able to operate in two modes, bright-field, and dark-field imaging. The former images are formed with only the transmitted electrons while the latter images are formed with a specific diffracted beam. Image contrast does not significantly depend on the absorption of electrons but rather on scattering and diffraction of electrons in the sample. Hence, dark-field imaging can provide a better image contrast. In our project, we used TEM techniques to study the contacts before and after

thermal annealing to evaluate the interface between contact and semi conductor.

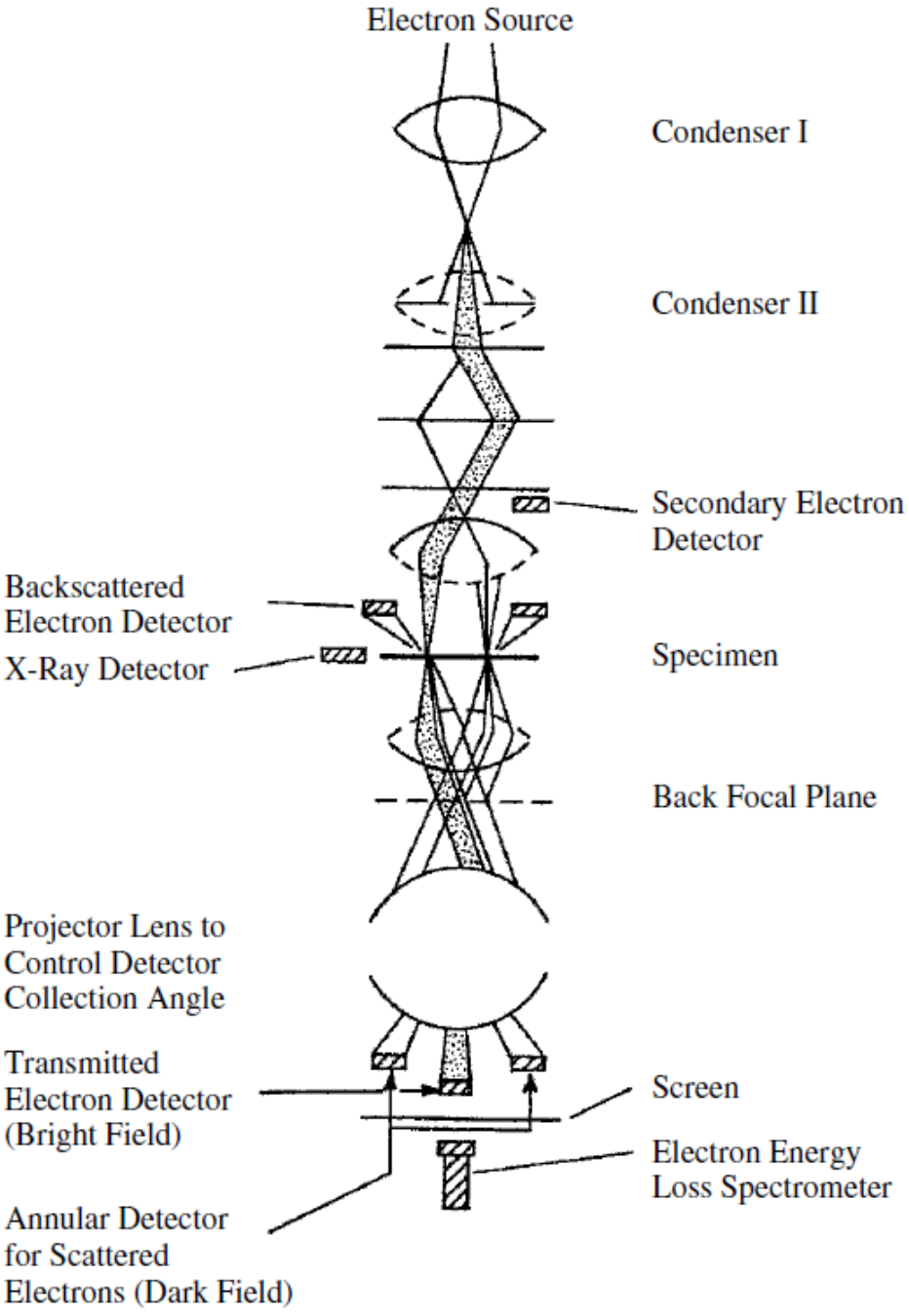

Figure 2.14 The principle of transmission electron microscopy (TEM) [81].

2.3.8 Secondary Ion Mass Spectrometry (SIMS)

Secondary Ion Mass Spectrometry (SIMS) is a well-known technique for surface spectroscopy and depth profiling. The schematic of SIMS is shown in Figure 2.15.In the SIMS experiment, a focused primary ion beam is used to bombard the sample surface. The transfer of primary ion energy resulted from atomic collision the target atoms will result in the ejection of target atoms and atom clusters. Most of these ejected atom and atom clusters are neutral; hence, they are not detectable by SIMS. However, some of these ejected atom and atom clusters (secondary ions) are ionized either positively or negatively. These secondary ions are then collected, analyzed and identified by a mass spectrometer. In Time of flight SIMS (TOF-SIMS), the mass of the ions are determined by measuring the time required to take the path from the sample trough the flight tube to the detector since the heavier ions will arrive at the detection system only after the lighter ions. In our experiment, ToF-SIMS was used for studying the depth profiling of our contact system with or without heat treatment.

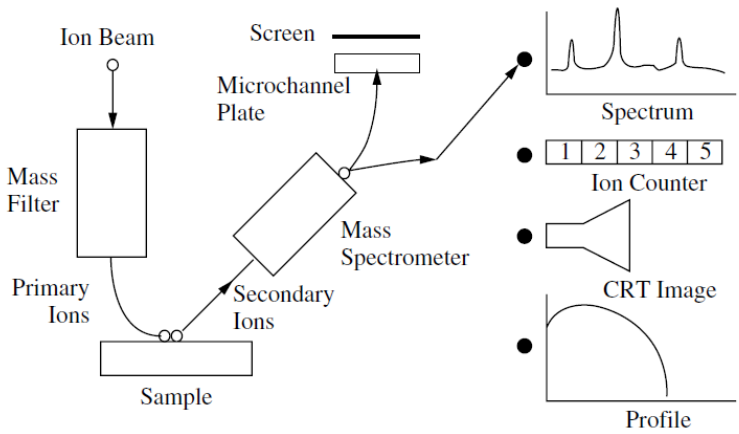

Figure 2.15 Schematic of a typical Secondary Ion Mass Spectrometry (SIMS)[81].

2.3.9 Atomic Force Microscope (AFM)

The Atomic Force Microscope (AFM) was used to study the surface morphology of both conducting and insulating samples. Its microscopy works by measuring the force between a probe and the sample, where the force depends on the property of the sample, the distance between the probe and sample, the probe geometry, and sample surface condition. As shown in Figure 2.16, AFM system consists of probe tip, cantilever, piezoelectric scanner, position sensitive photodetector and laser diode. The sharp probe tip usually made from silicon, silicon oxide or silicon nitride and attached to the cantilever end is used to sense the surface properties. To measure topography, the tip will contact with the sample which will cause the cantilever to deflect according to the force the tip received. A common technique used to detect the deflection of the cantilever and the cantilever's twist is to measure the laser diode light reflected from the cantilever into a four-segment position sensitive photodiode. The vertical motion is detected by z = (A+B)-(C+D) while the horizontal motion by x = (A+C)-(B+D). If the tip is scanned over the sample surface then the deflection of the cantilever can be recorded as an image which represents the three dimensional shape of the sample surface. AFM can operate in three modes, contact mode, non-contact mode and tapping mode. Contact mode could damage the sample surface and the cantilever tip although it gives the highest resolution. On the other hand, non-contact mode gives the lowest resolution although it does not damage the sample surface and the cantilever tip. Tapping mode provides the resolution between that of contact mode and non-contact mode with minimum sample and cantilever tip damage.

In our project, we used tapping mode AFM to examine the morphologies of our contacts before and after thermal annealing.

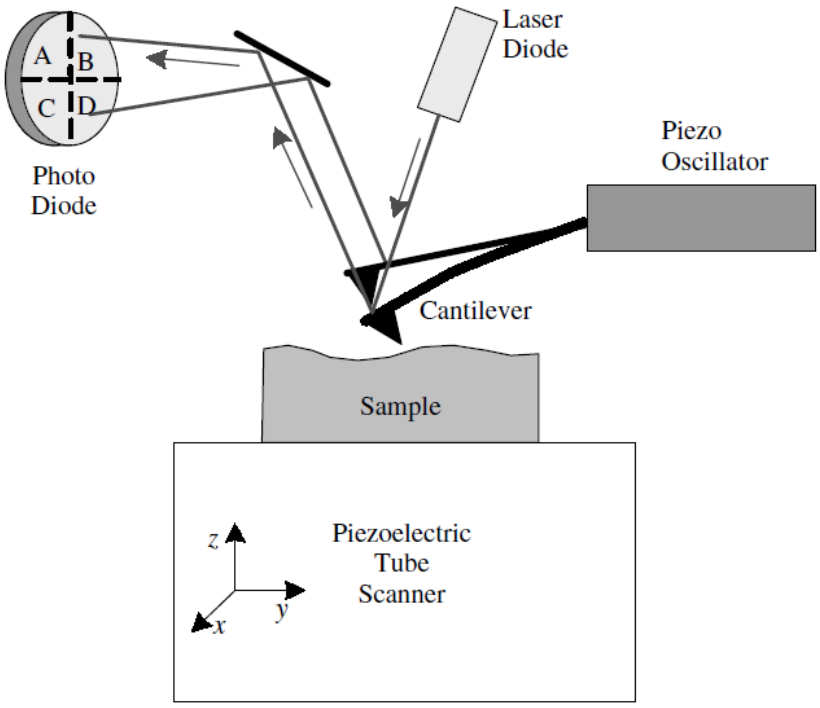

Figure 2.16 Schematic of an atomic force microscope[81].

Chapter 3: Preliminary explorations of cost effective CMOS compatible, gold-free Schottky contacts on InAlN/GaN grown on Si (111)

3.1 Introduction

As mentioned in Chapter 1, cost is one of the challenges for InAlN/GaN HEMT to compete with other semiconductor devices (e.g., Si-based). By growing InAlN/GaN HEMT structure on large Si substrate for economy of scale and developing Si compatible fabrication processes to allow the making of InAlN/GaN HEMTs in current Si fabrication foundries, it would make InAlN/GaN HEMTs more cost competitive. Traditional contacts of InAlN/GaN HEMTs are gold based, e.g., Ti/Al/Ni/Au for Ohmic contact and Ni/Au for Schottky contact. These are not welcome in Si fabrication foundries as gold is a deep level trap for Si and is very diffusive in Si, which can degrade the Si device performance and cause reliability issues. Therefore, we aim to develop non-gold based contacts for InAlN/GaN HEMTs to reduce the cost and in this chapter, we report our preliminary investigations on gold-free InAlN/GaN Schottky gate HEMT on Si (111) substrate. Among metals, W, Ti, TiN, Al and Co are currently used in Si foundries. However, W has higher melting point (3422^{o}C) compared to Al and lower resistivity (~52.8 nΩm) compared to Co, Ti and TiN. Lastly, W is cheaper and more abundant than Au; hence, W is used as a simple replacement of Au in our first attempt on Au-free contacts. The source/drain Ohmic contacts and Schottky gate contacts are Ti/Al/Ni/W and Ni/W, respectively. The effects of a thin high-k ZrO_2 surface passivation are also examined.

3.2 Experimental Procedures

The commercially available 4 inch InAlN/GaN epi-wafer used was grown on high resistive Si (111) substrate by means of Metal Organic Chemical Vapor Deposition (MOCVD) and its epi-layer structure is shown schematically in Figure 3.1. The wafer was characterized using Hall measurement at room temperature and exhibits a sheet resistance of 629 Ω/□, electron mobility of 570 cm^2/Vs and sheet concentration of 1.739×10^{13} carriers/cm^2. Gold-free Ti/Al/Ni/W Ohmic contact was first analyzed by means of the Circular Transmission Line Method (CTLM). In particular, different Ti/Al thickness ratios, and different annealing temperatures were investigated to optimize the Ohmic contact properties.

On the other hand, gold-free Schottky contact (Ni/W) with four different thickness ratios and four different annealing temperatures were examined using Schottky diode (shown schematically in Figure 3.1. Schottky diode was optimized to achieve the highest Schottky barrier height (SBH). Finally, the InAlN/GaN-on-Si Schottky gate HEMTs were fabricated and characterized.

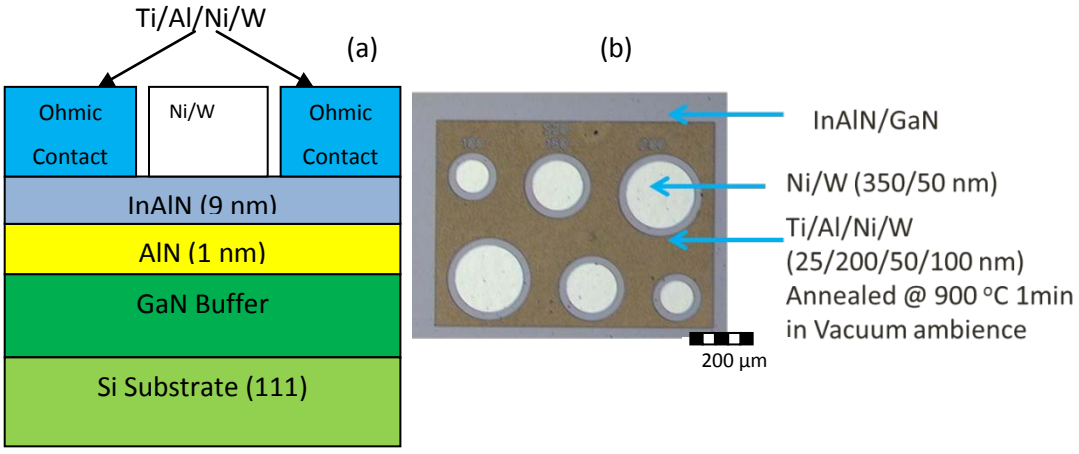

Figure 3.1 (a) Schematic cross-section and (b) morphology of InAlN/GaN-on-Si(111) Schottky diodes.

Figure 3.2 shows the schematic cross-section of Schottky gate InAlN/GaN-on-Si(111) HEMTs. The gate length and the source/drain distance of HEMT are 2 and 5 μm, respectively. The gate width is 2×50 μm (i.e., 2 gates with width of 50 μm each). The gate-last fabrication process for HEMT was used and it started with cleaning the wafer using Acetone, IPA and DI water, in that sequence, and followed by $HCl:H_2O$ (1:3). This cleaning process was performed before every lithography step. For mesa isolation, inductive coupled plasma (ICP) using gas mixtures of BCl_3 and Cl_2 was used to etch InAlN/GaN. After mesa isolation, non-gold based source/drain Ohmic contacts (Ti/Al/Ni/W) were deposited by means of sputtering and the contacts were annealed at 900^{o}C for 1 minute in vacuum ambient.

Prior to the gate metal deposition, the effect of O_2 plasma surface treatment was investigated and it was found that the resultant oxidation at the metal semiconductor interface helped reduce the reverse gate leakage current [93]. Therefore, O_2 plasma surface treatment was performed in an ICP chamber with a RIE power of 50 W and duration of 33 s prior to gate metal deposition. The Schottky gate contact (Ni/W) was then sputtered and annealed at 400^{o}C in vacuum for 1 minute.

It has been reported that the surface passivation of the semiconductor between drain, gate and source contacts (for example by Al_2O_3 and Si_3N_4) helps to decrease the transistor on-resistance, R_{on}, and increase the drain saturation current, I_{DSAT}, in addition to suppressing the current collapse effect [49]. Hence, a 7 nm thin ZrO_2 was deposited using Atomic Layer Deposition (ALD) for device passivation. For the contact openings, hydrofluoric acid (HF) was used to etch the ZrO_2.

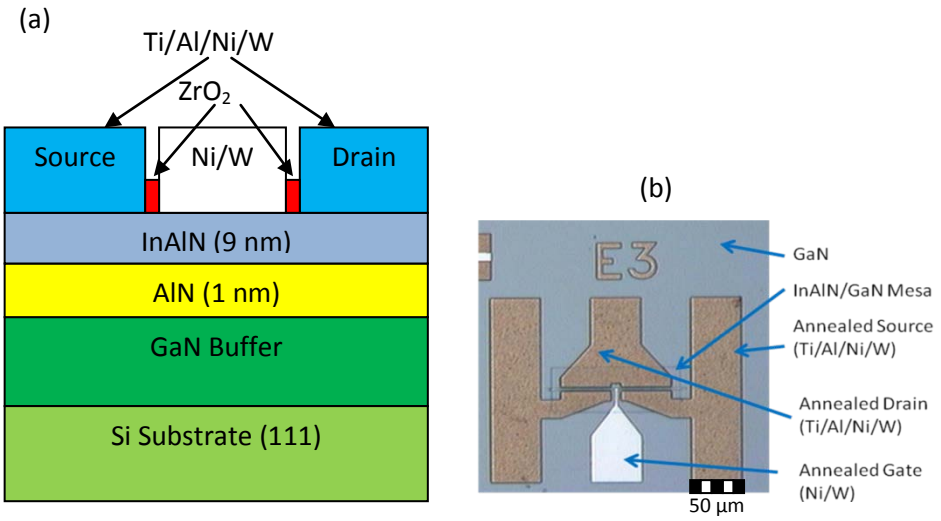

Figure 3.2 (a) Schematic cross-section and (b) surface morphology of the Schottky gate InAlN/GaN-on-Si(111) HEMTs.

3.3 Results and Discussion

The contacts and HEMTs were characterized using Agilent Semiconductor Analyzer B1500A at room temperature. For Ti/Al/Ni/W Ohmic contacts on InAlN/GaN, four different Al thicknesses were used, while the thickness of the Ti, Ni and W layers were kept constant: Ti/Al/Ni/W (25/50/40/100 nm, 25/100/40/100 nm, 25/150/40/100 nm and 25/200/40/100 nm). As shown in Table 3.1, Ti/Al/Ni/W (25/200/40/100 nm) has a minimum contact resistivity (ρ_c) of 1.06×10^{-6} Ωcm^2 after annealing at a temperature of 900°C in vacuum for 1 minute.

The effects of annealing temperature on ρ_c and R_c are also studied using Linear Transmission Line Method (LTLM), as shown in Figure 3.3. A great improvement in ρ_c is observed when contacts are annealed at 900°C in vacuum for 60 sec having an average ρ_c value around 1.45×10^{-6} $\Omega.cm^2$ (see Figure 3.3a). In addition, low R_c with an average value around 0.56 Ω.mm has been

obtained with this optimized Ti/Al/Ni/W (25/200/40/100 nm) ohmic scheme. For the same wafer, the traditional gold based contacts, Ti/Al/Ni/Au (25/200/40/100 nm), achieved minimum ρ_c of 6.79 × 10^{-7} Ωcm^2, after annealing at 850^{o}C in vacuum ambient for 30 s. Hence, the non gold based contacts are comparable to gold based contacts in terms of ρ_c.

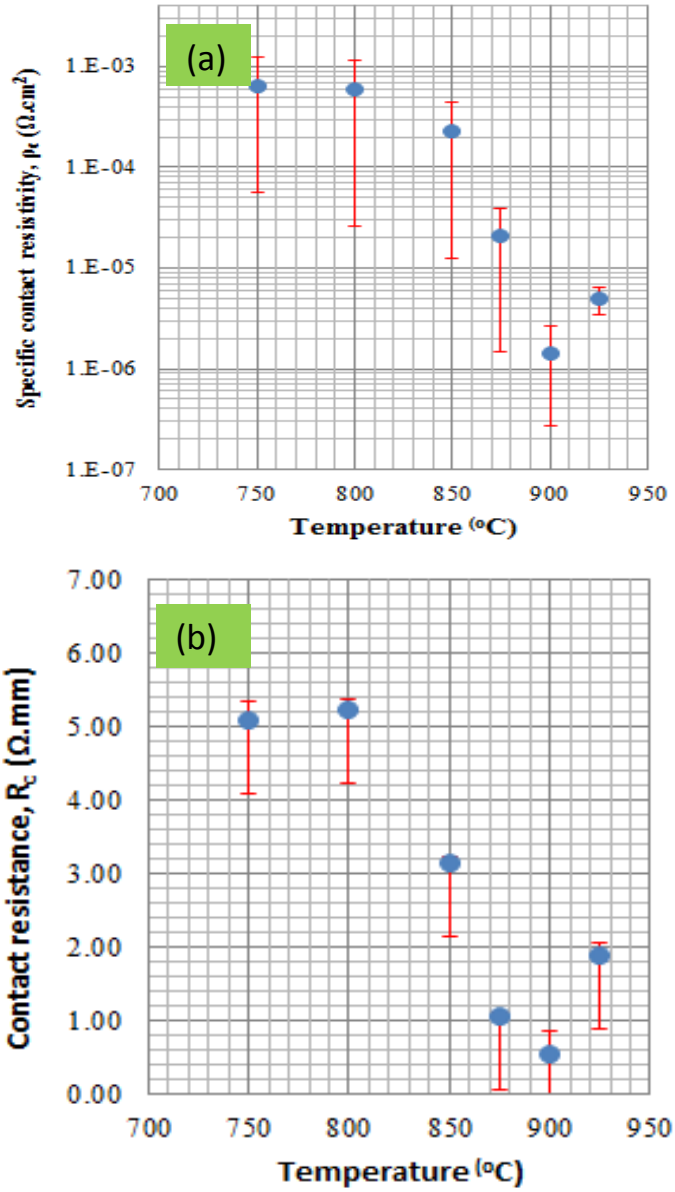

Figure 3.3 Annealing temperature variation of (a) specific contact resistivity and (b) contact resistance with an optimized Ti/Al/Ni/W (25/200/40/50 nm) layer combination on InAlN/GaN-on-Si(111).

Table 3.1Contact resistivity (ρ_c) as a function of Ti/Al thickness ratio of Ti/Al/Ni/W Ohmic contacts to InAlN/GaN-on-Si. Contacts were annealed at 900^{o}C in vacuum for 1 minute.

Ti/Al/Ni/W Thickness	ρ_c (Ωcm^2)
25/50/40/100 nm	1.26×10^{-4}
25/100/40/100 nm	2.41×10^{-4}
25/150/40/100 nm	6.28×10^{-6}
25/200/40/100 nm	1.06×10^{-6}

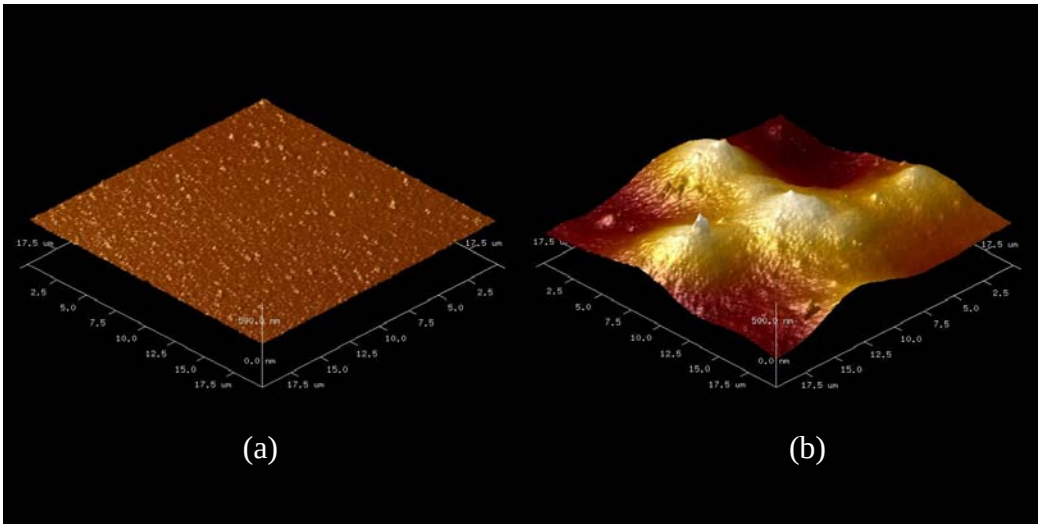

Figure 3.4 AFM images of (a) Ti/Al/Ni/W (25/200/40/100 nm) contact annealed at 900^{o}C 1 min in vacuum, and (b) Ti/Al/Ni/Au (25/200/40/100 nm) contact annealed at 850^{o}C 30 sec in vacuum.

Figure 3.4 shows the AFM images of gold based Ohmic contact (Ti/Al/Ni/Au) and non-gold based Ohmic contact (Ti/Al/Ni/W). It can be seen clearly that the morphology of the non-gold based Ti/Al/Ni/W Ohmic contact is less rough than that of the traditional gold based Ti/Al/Ni/Au contact, despite annealing at a higher temperature and for a longer duration for the former. The average roughness of the non-gold based Ohmic contact is 14.7 nm while that of gold

based Ohmic contact is 60.9 nm (~ 4 times higher). Hence, in terms of surface morphology Ti/Al/Ni/W is better compared to Ti/Al/Ni/Au.

For the Schottky diode, the SBH is determined using the *I-V* method. Since this contact system would be used as a gate in HEMT, the effective SBH given by the *I-V* method would provide the gate current transport mechanisms, while the *C-V* or photocurrent methods do not. The SBH is calculated using the thermionic emission equation:

$$J = A^{*}T^{2}e^{\left(\frac{-q\Phi_B}{k_BT}\right)}e^{\left(\frac{qV}{nk_BT}\right)}\left(1 - e^{-\frac{qV}{k_BT}}\right) \qquad (3.1)$$

where A^{*} is the Richardson's constant and is 55.86 $Acm^{-2}K^{-2}$ for undoped InAlN [42], J is the current density, T is the absolute temperature, q is the electron charge, Φ_B is Schottky Barrier Height (SBH), n is the ideality factor, k is the Boltzmann's constant and V is the applied voltage.

Figure 3.5 shows the *I-V* characteristics of Ni/W Schottky diodes for four different Ni/W thickness ratios, while Figure 3.6 depicts the *I-V* characteristics of Ni/W (350/50 nm) Schottky diodes as a function of annealing temperature. The SBH for Ni/W (50/50 nm), (150/50 nm), (250/50 nm) and (350/50 nm) are 0.547 ± 0.041, 0.549 ± 0.039, 0.631 ± 0.059, and 0.678 ± 0.055 respectively. The SBH of Ni/W contact on InAlN/GaN increases with increasing Ni/W thickness ratio, as shown in Figure 3.7. It is observed from the Ni-W phase diagram that Ni forms alloys with W at room temperature [94] and alloys such as NiW and Ni_4W are expected to have workfunction lower than that of Ni and higher than that of W. The SBH is related to the difference between the metal and semiconductor workfunctions, a lower workfunction of

metal would result in a lower SBH. With a higher Ni/W thickness ratio, it can be expected that the Ni-W alloys formed have a higher Ni content, meaning a higher workfunction for the gate metal, thus leading to a higher SBH with increasing Ni/W thickness ratio, as shown in Figure 3.7. Furthermore, the reverse leakage current of Ni/W (350/50 nm) is the lowest, as shown in Figure 3.5. This couples with the highest SBH, depicted in Figure 3.7, means that the optimized thickness for Ni/W is 350/50 nm.

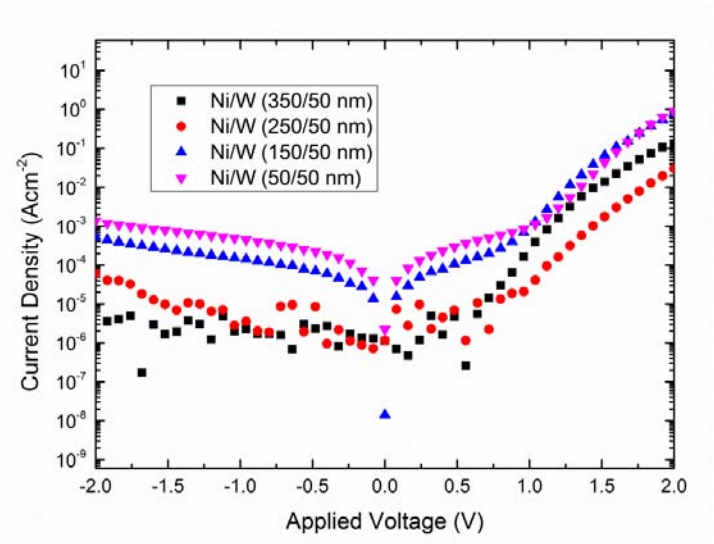

Figure 3.5 *I-V* characteristics of Ni/W Schottky diodes as a function of Ni/W thickness ratios. The contacts are under as-deposited condition (i.e., without annealing).

As shown in Figure 3.6, both the reverse leakage current and forward bias current of the Ni/W (350/50 nm) Schottky contact increase with increasing annealing temperature. It is noted that the increase at 600^{o}C is more significant. At the same time, the SBH improves with annealing temperature up to 400^{o}C and decreases beyond that, as depicted in Figure 3.7. The optimum annealing temperature for the Ni/W Schottky contact on InAlN/GaN was therefore found to be 400^{o}C with a maximum SBH of 0.72 ± 0.05 eV achieved. The resistivity

of Ni/W is extracted using four point probe resistivity measurement. The extracted resistivity of Ni/W (350/50 nm) annealed at 400°C is ~7.86 ± 0.26 nΩm.

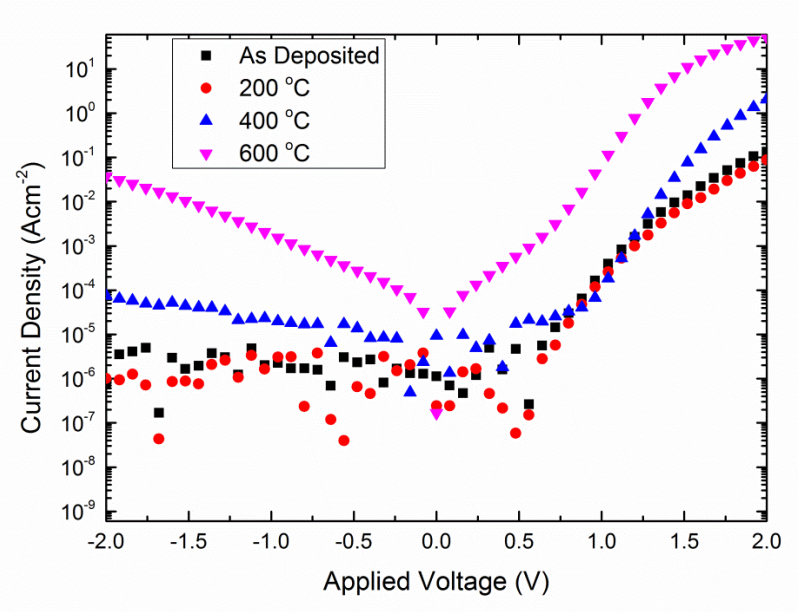

Figure 3.6 *I-V* characteristics of Ni/W (350/50 nm) Schottky diodes as a function of annealing temperature. The contact was annealed for 1 minute in vacuum ambient.

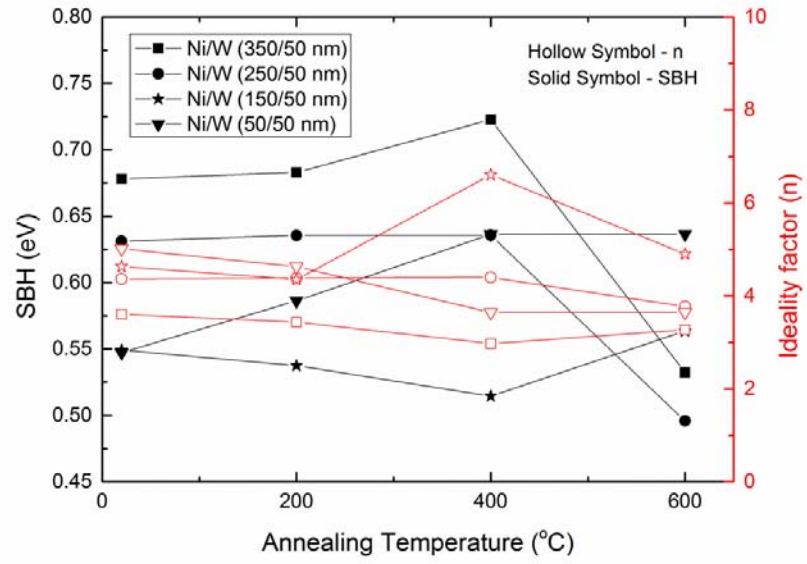

Figure 3.7 Effects of Ni/W thickness ratio and annealing temperature on SBH and ideality factor. The annealing was conducted in vacuum for 1 minute.

The variation of the *I-V* characteristic ideality factor (*n*) of the Ni/W contact on InAlN/GaN with the Ni/W thickness ratio and annealing temperature is also shown in Figure 3.7. The value of *n* is observed to be much higher than 1. Relatively high ideality factor could be resulted from the tunneling current instead of thermionic emission at low temperature. To examine this effect, the dependency of SBH on temperature was investigated. Figure 3.8 shows the *I-V* characteristic of the Ni/W (350/50 nm) Schottky contact on InAlN/GaN as a function of operating temperature. The contact has been annealed at 400^{o}C in vacuum for 1 minute. As shown in Figure 3.8, both the reverse leakage current and forward current increase with increasing operating temperature since more electrons have enough thermal energy for the thermionic emission at higher temperature. On the other hand, the ideality factor decreases, while the SBH increases with increasing operating temperature, as shown in Table 3.2. The minimum ideality factor and the maximum SBH achieved are 2.39 ± 0.13 and 0.92 ± 0.07 eV at 200^{o}C, respectively. This improvement in SBH and ideality factor could be resulted from the increased contribution of thermionic emission current at high operating temperature. On the other hand, the dislocations assisted tunneling dominated current transport mechanisms at the low operating temperature, which resulted in the high ideality factor and low effective SBH, as discussed in Donoval [42].

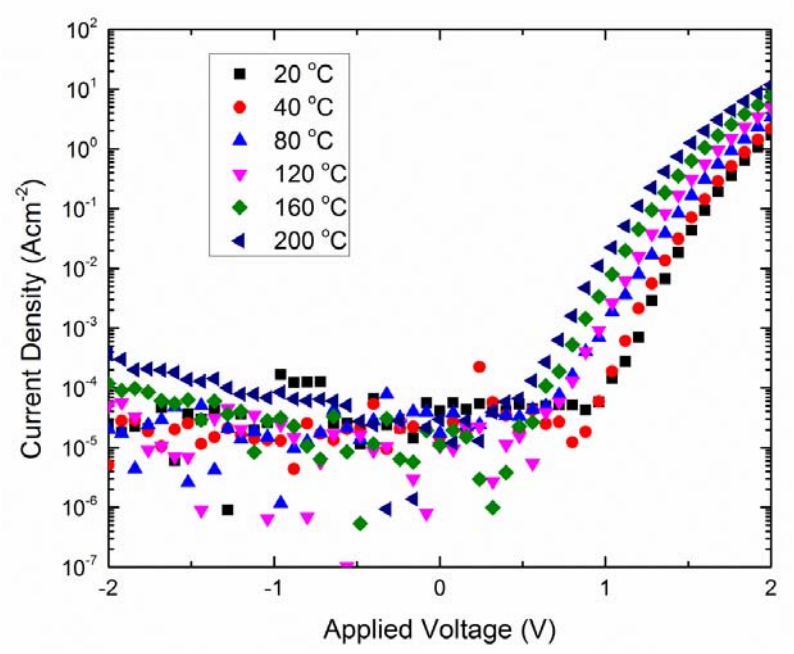

Figure 3.8 Operating temperature dependency of the Ni/W (350/50 nm) Schottky contact on InAlN/GaN. The contact has been annealed at 400°C in vacuum for 1 minute.

TABLE 3.2 SBH and ideality factor as a function of operating temperature of the Ni/W (350/50 nm) Schottky contact on InAlN/GaN. The contact has been annealed at 400°C in vacuum for 1 minute.

Operating Temperature (°C)	SBH (eV)	Ideality Factor
20	0.71	2.98
40	0.79	2.84
60	0.73	3.09
80	0.73	3.06
100	0.82	2.83
120	0.85	2.60
140	0.89	2.83
160	0.89	2.44
180	0.91	2.40
200	0.92	2.39

Clear advantage is observed using a thin 7 nm ZrO_2 layer to passivate the InAlN/GaN-on-Si HEMTs, as shown in Figure 3.9 and Figure 3.10. Devices with ZrO_2 passivation attain a higher maximum g_m of 160 mS/mm (an increase of ~33.3%) and a lower R_{on} of 10 Ω/mm (a reduction of ~16.7 %), compared to HEMTs without ZrO_2 passivation. It is worth noting that ZrO_2 passivation has helped produce a higher I_{DSAT} despite a lower gate overdrive ($V_{GS} - V_{th}$ of 2.7 versus 3 V), as depicted in Figure 3.9.

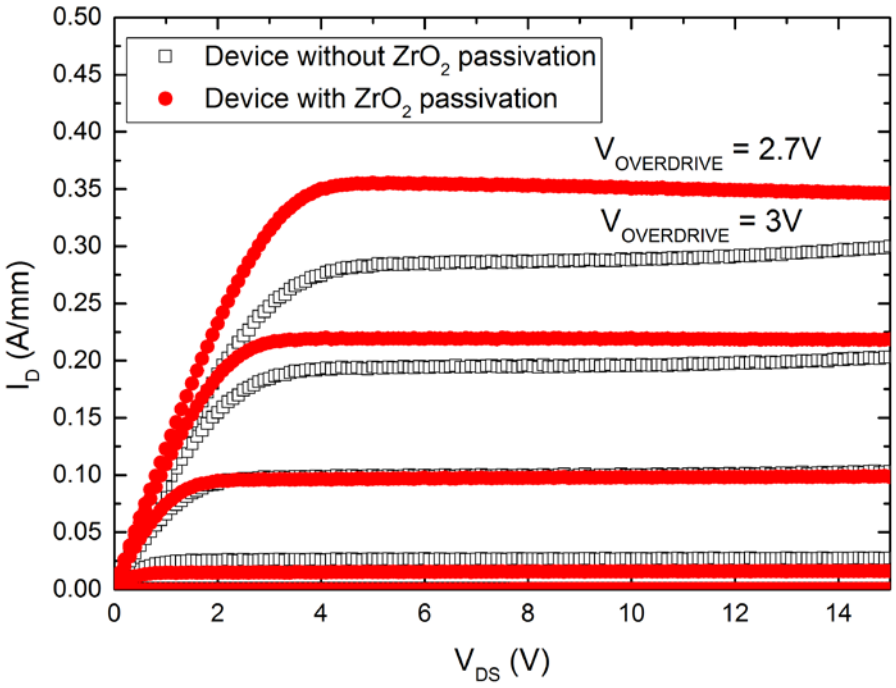

Figure 3.9 I_D-V_{DS} characteristics of InAlN/GaN-on-Si HEMT with and without ZrO_2 passivation. The threshold voltage, V_{th}, with and without passivation ZrO_2 is about -1.7 V and -1 V, respectively. The gate overdrive, $V_{OVERDRIVE}$ (= V_{GS} - V_{th}),was increased in steps of 1 V.

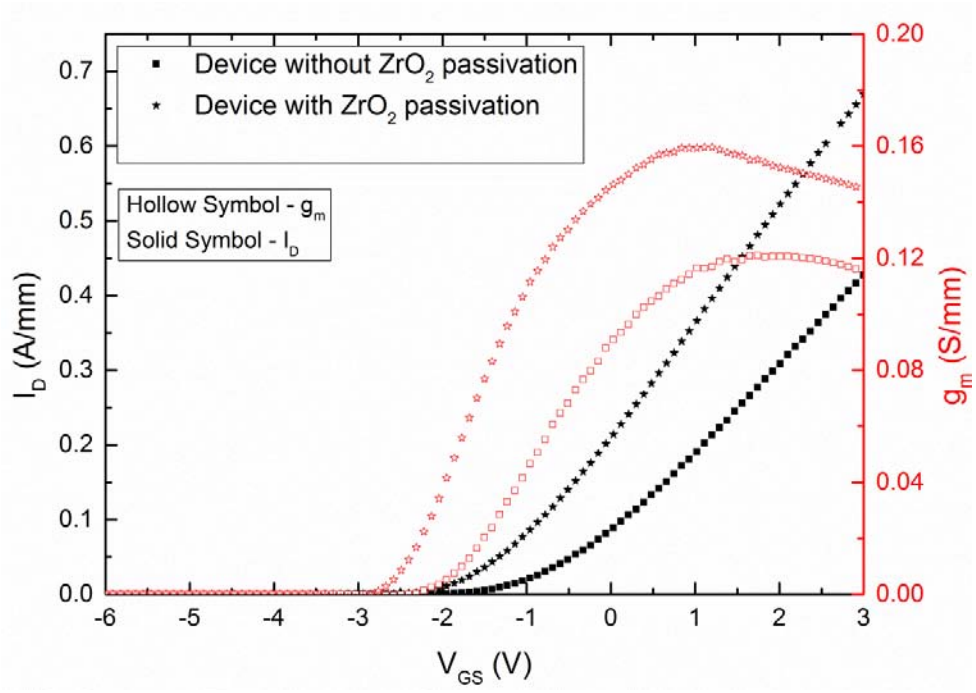

Figure 3.10 I_D-V_{GS} characteristics of InAlN/GaN-on-Si HEMT with and without ZrO_2 passivation at V_{DS} = 10 V

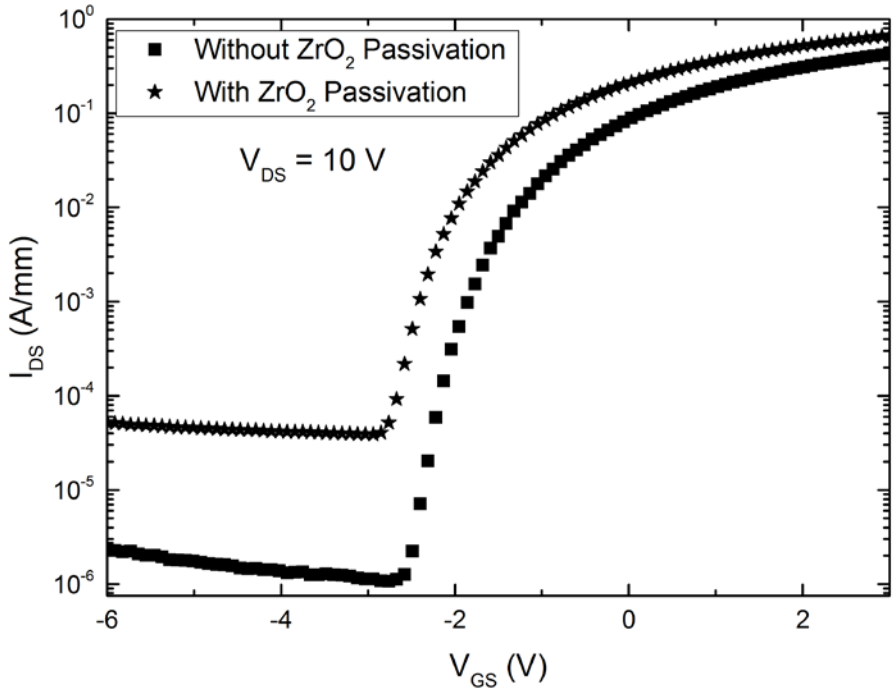

Figure 3.11 The transfer characteristics of InAlN/GaN-on-Si(111) HEMTs with and without ZrO_2 passivation at V_{DS} = 10 V.

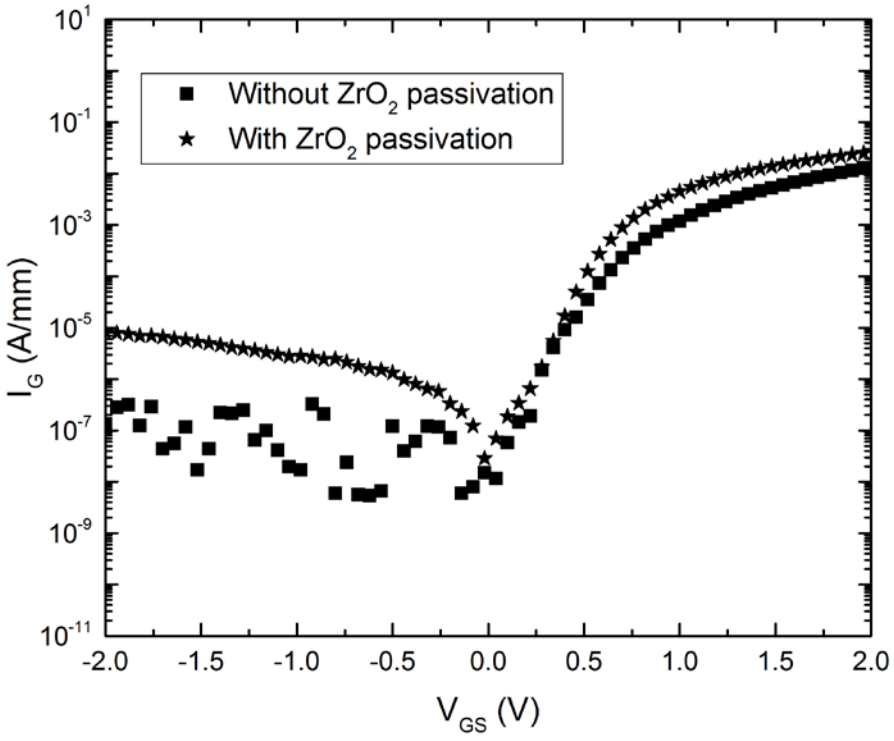

Figure 3.12 I_G-V_{GS} characteristics of InAlN/GaN-on-Si(111) HEMTs with and without ZrO_2 passivation.

The transfer characteristics and I_G-V_{GS} characteristics of InAlN/GaN-on-Si(111) HEMTs with and without ZrO_2 passivation are shown in Figure 3.11 and Figure 3.12 respectively. It can be observed that ZrO_2 passivation increases I_{ON} by 33% while it increases I_{OFF} by more than one order of magnitude thus reducing the ON-OFF current ratio by an order of magnitude as shown in Figure 3.11. This increase in I_{OFF} is mainly attributed by the increase in gate leakage current, which is also increased by more than one order of magnitude with ZrO_2 passivation as shown in Figure 3.12. The observation of increased I_{OFF} was also seen in InAlN/GaN HEMT and AlGaN/GaN with SiN passivation [95, 96]. This effect could be resulted from the surface leakage (the leakage currents through the bulk passivation layer

and the interfacial layer between the passivation layer and InAlN barrier layer) or the leakage current from the gate contact directly to the 2DEG underneath the gate. From the results of Li *et al.*, it is possible to conclude that the surface leakage current is not the major component of the increase in total gate leakage current in passivation [96]. Hence, it is likely that the increase in gate leakage current is resulted from the leakage current from the gate directly to the 2DEG underneath the gate.

The above changes in electrical characteristic due to ZrO_2 passviation is likely resulted from the enhancement of 2DEG, as shown in Figure 3.13. In the figure, the effects of ZrO_2 thickness on the sheet resistance (R_{sh}), carrier mobility (μ_s) and 2DEG concentration (n_{sh}) of the InAlN/GaN-on-Si(111) substrate, as characterized by means of Hall measurements are shown. It can be observed that with increasing ZrO_2 thickness, the sheet resistance decreases from 675 to 530Ω/□. The decrease in sheet resistance (by ~ 20%) is mainly caused by the increase in the 2DEG carrier concentration (by ~ 25%), as there is no significant change in the carrier mobility, as shown in Figure 3.13(b). This enhancement of 2DEG concentration was also observed in HEMTs with other dielectric passivation such as Al_2O_3 [97]. The shift in V_{th} seen in Fig. 3.9 is also probably caused by the enhancement of 2DEG concentration by ZrO_2. The increase in 2DEG due to ZrO_2 passivation could be resulted from the stress induced polarization charges and not from the dielectric charges since it is observed that there is an insignificant thickness dependency of 2DEG concentration above 7 nm ZrO_2 passivation similar to Al_2O_3 [97] and SiN passivation [98]. The thickness of 7 nm is optimum for ZrO_2 as a passivation

layer since there is no significant decrease in sheet resistance with ZrO_2 thickness above 7 nm.

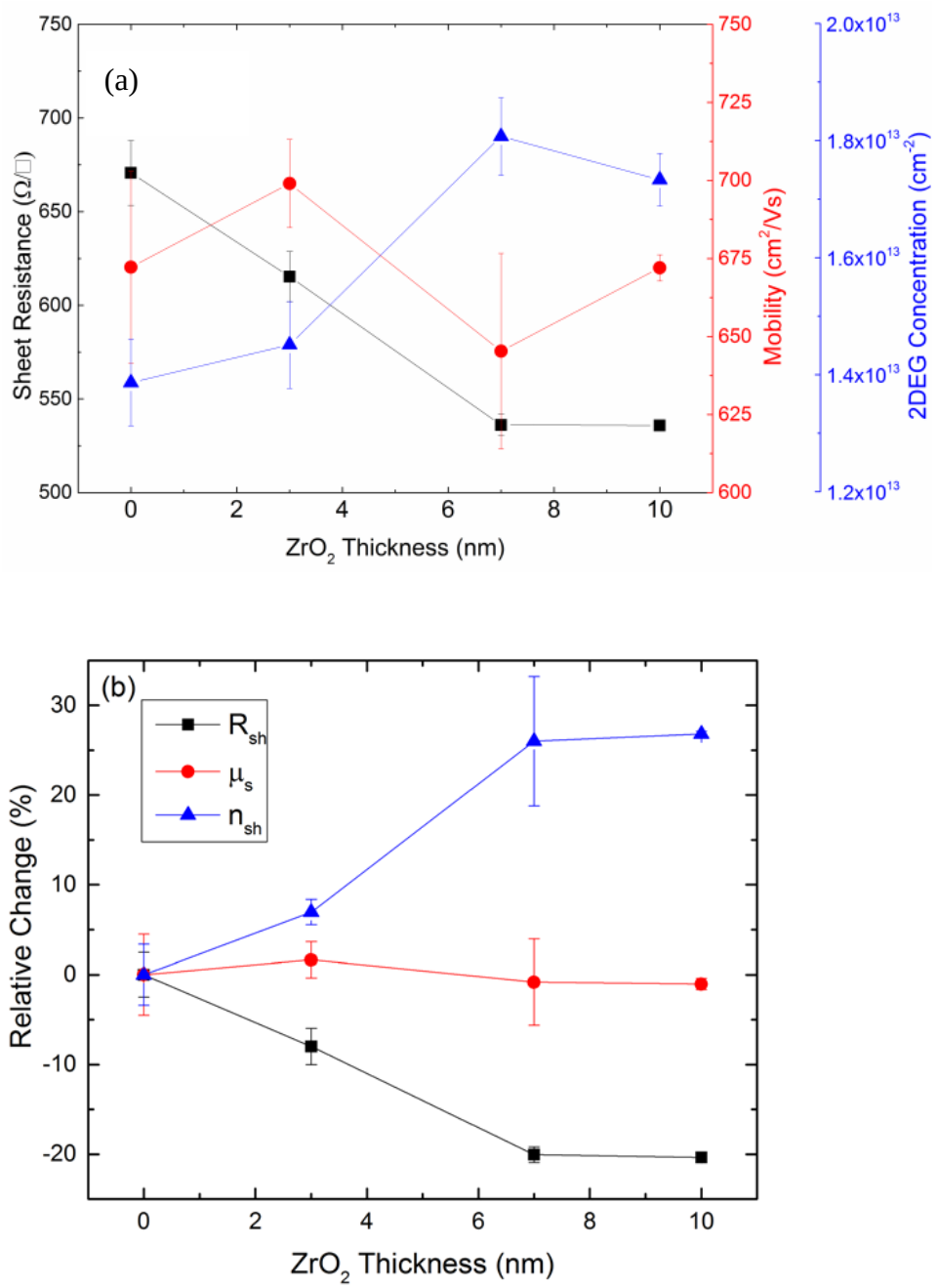

Figure 3.13 Effects of ZrO_2 thickness on (a) absolute value and (b) relative change of sheet resistance (R_{sh}, square), carrier mobility (μ_s, circle) and carrier concentration (n_{sh}, triangle).

3.4 Conclusion

In conclusion, we have studied the electrical properties of CMOS compatible gold-free Ti/Al/Ni/W Ohmic contact and Ni/W Schottky contact to InAlN/GaN HEMT grown on high resistive Si(111) substrate. The specific contact resistivity of Ti/Al/Ni/W contacts has been investigated as a function of annealing temperature and different Al thicknesses, and has achieved the lowest value of 1.06×10^{-6} Ω·cm^2 after annealing at 900^{o}C in vacuum. We have also investigated the Ni/W Schottky contacts as a function of annealing temperature and different Ni thicknesses and found that the maximum Schottky barrier height of the Ni/W (350/50 nm) contact achieved is 0.72 eV at room temperature. Hence, the electrical characteristics of InAlN/GaN-on-Si Schottky gate HEMTs with non-gold based contacts (Ti/Al/Ni/W Ohmic and Ni/W Schottky) are comparable to those of devices with gold-based contacts. We have also shown that a thin ZrO_2 passivation layer helps improve the DC characteristics of InAlN/GaN HEMTs, yielding a higher g_m (by ~33.3%) and a lower R_{on} (by ~16.7%) compared to HEMTs without passivation. However, both the OFF current and gate leakage current are increased by more than one order of magnitude which reduces the ON-OFF current ratio with ZrO_2 passivation.

Chapter 4: Thermally robust RuO_x Schottky diodes and HEMTs on n-GaN and InAlN/GaN heterostructure grown on 100 mm Si(111)

4.1 Introduction

As reported in Chapter 3, $In_xAl_{1-x}N$/GaN based Schottky diodes and high electron mobility transistors (HEMTs) using traditional Ni/Au and Ni/W Schottky contacts show a high reverse leakage current when annealed above 600^{o}C [50, 99, 100]. This limits the flexibility of HEMT fabrication processing, allowing only the use of gate-last process, where the gate contact is formed after the high temperature (> 700^{o}C) annealing for the formation of Ohmic contacts. In contrast, a thermally robust gate allows the use of gate-first self-aligned process, which is necessary to reduce transistor access resistances. Such a gate formation also requires fewer processing steps compared to the gate-last self-aligned process using dummy gate, thus reducing the fabrication cost [44, 45]. In addition, with thermally robust gate, $In_xAl_{1-x}N$/GaN HEMT could be used in high temperature applications. Furthermore, gold-free contacts are necessary to process GaN-on-Si based devices in existing Si foundries to lower the cost. Therefore, it is desirable to develop a thermally robust gold-free Schottky contact.

Ru (Ruthenium) is one of the platinum group metals; hence, it is chemically inert. Additionally, RuO_x (Ruthenium oxide) has a similar workfunction compared to Au (5.1 eV). Although Ru is one of the platinum group metals, it is cheaper compared to Au (1800 USD/kg versus 39760 USD/kg), this information is quoted on 25 March 2015). RuO_2 has been used as the Schottky

contact for n-type GaN and $Al_xGa_{1-x}N$/GaN heterostructures and demonstrated an increase in Schottky barrier height (SBH) and a reduction in reverse leakage currents when annealed at 500^oC in N_2 for 30 minutes [101, 102]. To the best of our knowledge, usage of RuO_2 as the Schottky gate contact on $In_{0.17}Al_{0.83}N$/GaN heterostructures is rather limited. Last but not least, it is CMOS compatible.

In this Chapter, we report the investigations of RuO_x Schottky diodes on n-GaN and $In_{0.17}Al_{0.83}N$/GaN, both grown on Si(111) substrates. The effects of post deposition thermal annealing temperature and ambient on the leakage current and SBH of RuO_x and Ni/Au Schottky diodes are presented. We also report the electrical characteristics of RuO_x Schottky gate $In_{0.17}Al_{0.83}N$/GaN-on-Si HEMTs.

4.2 Experimental Procedures

RuO_x based Schottky diodes were first fabricated on n-type GaN (with a carrier concentration of 5.57×10^{17} cm^{-3}) grown on Si(111) substrate. The fabrication process for the Schottky diodes started with the patterning and metallization of Ohmic contacts (Ti/Al/Ni/Au) deposited by electron beam evaporation. The contacts were subsequently defined by means of metal lift-off and were annealed at 900^oC in vacuum for 1 minute. After the Schottky contact patterning, about 100 nm thick RuO_x was sputtered in Ar (20 sccm) and O_2 (10 sccm) plasma ambient and defined also by means of metal lift-off. The Schottky contacts on n-GaN were then annealed at 4 different temperatures (400, 500, 600 and 700^oC) in vacuum and at 5 different temperatures (400, 500, 600, 700 and 800^oC) in N_2. The Schottky contacts

were characterized using thermionic emission model and the *I-V* characteristics were measured using an Agilent B1500A Semiconductor Parameter Analyzer at room temperature. In addition, the material properties of RuO_x annealed in vacuum and N_2 were characterized using x-ray diffraction (XRD).

RuO_x based Schottky diodes were also fabricated on 100 mm diameter $In_{0.17}Al_{0.83}N$/GaN-on-Si(111) heterostructure with a sheet resistance of 513 Ω/sq. The fabrication process of these Schottky diodes was the same as that of Schottky diodes on n-GaN, except for the Ohmic contacts (Ti/Al/Ni/W), which were non-gold based and sputter-deposited. Moreover, Ni/Au (30/80 nm) Schottky diodes on the same $In_{0.17}Al_{0.83}N$/GaN-on-Si(111) HEMT structure with Ti/Al/Ni/W Ohmic contacts were fabricated as reference samples for comparison of SBH, leakage currents, and thermal stability. Both the Ni/Au and RuO_x Schottky diodes on $In_{0.17}Al_{0.83}N$/GaN-on-Si(111) heterostructures are annealed at 5 different temperatures(400, 500, 600, 700, and 800^oC) in N_2 ambient for 1 minute.

Furthermore, RuO_x Schottky gate $In_xAl_{1-x}N$/GaN-on-Si(111) HEMTs were fabricated by means of the gate-last process. It started with mesa isolation etch using inductively coupled plasma (ICP) with the BCl_3/Cl_2 chemistry. After the Ohmic contact patterning, Ti/Al/Ni/W (25/200/40/50 nm) layers were deposited using a reactive sputtering system and followed by the metal lift-off process. The contacts were then annealed at 900^oC in vacuum for 1 minute. Subsequently, the gate was patterned and followed by sputter-deposition of 100 nm thick RuO_x. The RuO_x Schottky contacts were defined by a metal lift-off process. The device fabrication was completed with gate annealing at

700°C in N_2 for 1 minute. Since investigation of the Schottky contact is the main objective in this thesis, the fabricated HEMTs are unpassivated in our study. The DC pulsed *I-V* characterization of such HEMTs was conducted to showcase the electrical performances.

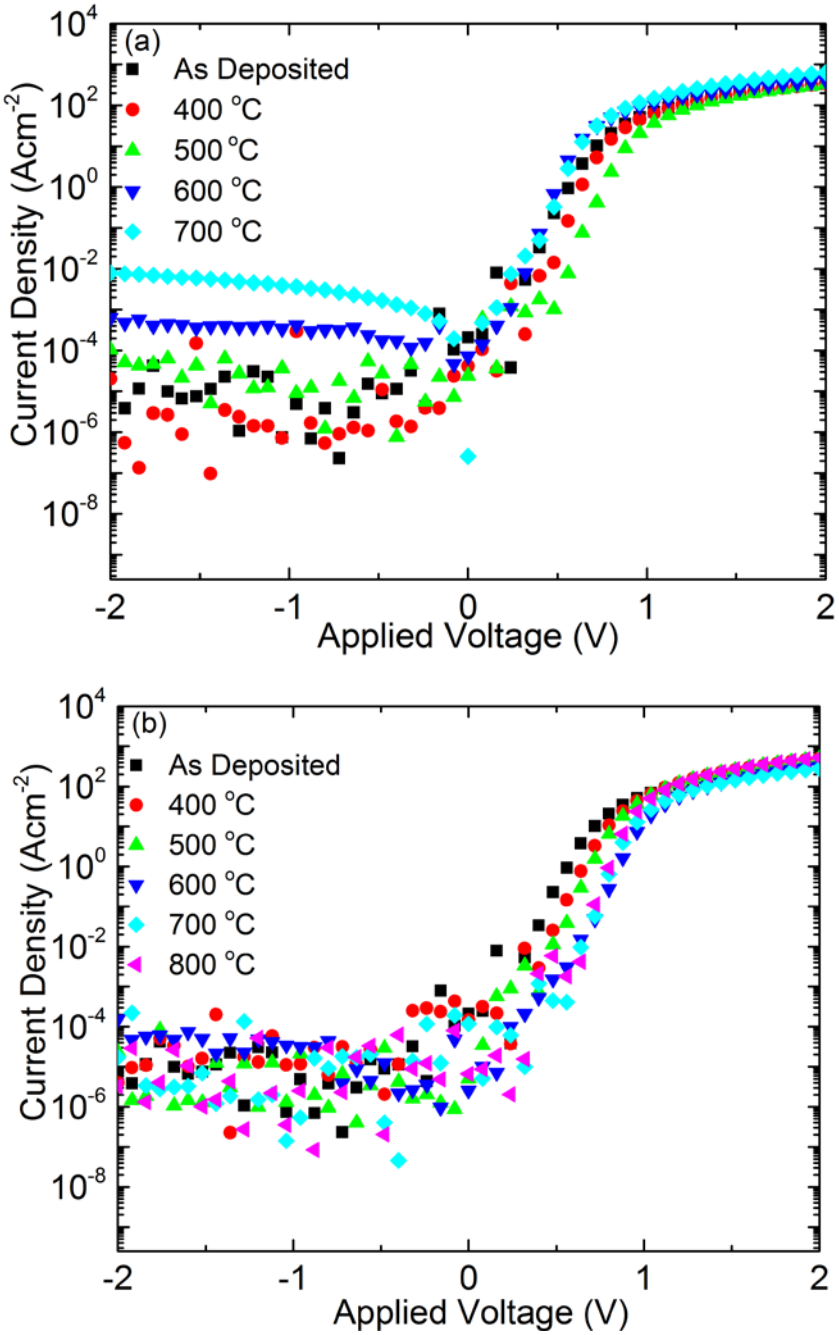

Figure 4.1 *I-V* characteristics of RuO_x Schottky diodes on n-GaN-on-Si(111) substrate, annealed at various temperatures in (a) vacuum and (b) N_2 for 1 minute.

4.3 Results and Discussions

Figure 4.1 shows the *I-V* characteristics comparison between RuO_x Schottky diodes on n-GaN annealed in N_2 and vacuum, while Figure 4.2 shows the effects of annealing ambient and temperature on the extracted SBH. As shown in Figure 4.1, the reverse biased leakage current of RuO_x Schottky diodes increases from 10^{-5} to 10^{-2} Acm^{-2} (three orders of magnitude) after annealing at a higher temperature of 700°C in vacuum. The corresponding SBH drops to 0.65 eV, from a maximum of 0.72 eV achieved at 400°C annealing in vacuum ambient (see Figure 4.2). On the other hand, the SBH of RuO_x Schottky diodes annealed in N_2 increases with increasing annealing temperature, from 0.62 eV (at no heat treatment condition) to 0.9 eV (after annealing at 700°C), a significant increase of 45 %. In particular, the reverse bias leakage current is still lower than 10^{-5} Acm^{-2}, even after annealing at 800°C in N_2 for 1 minute.

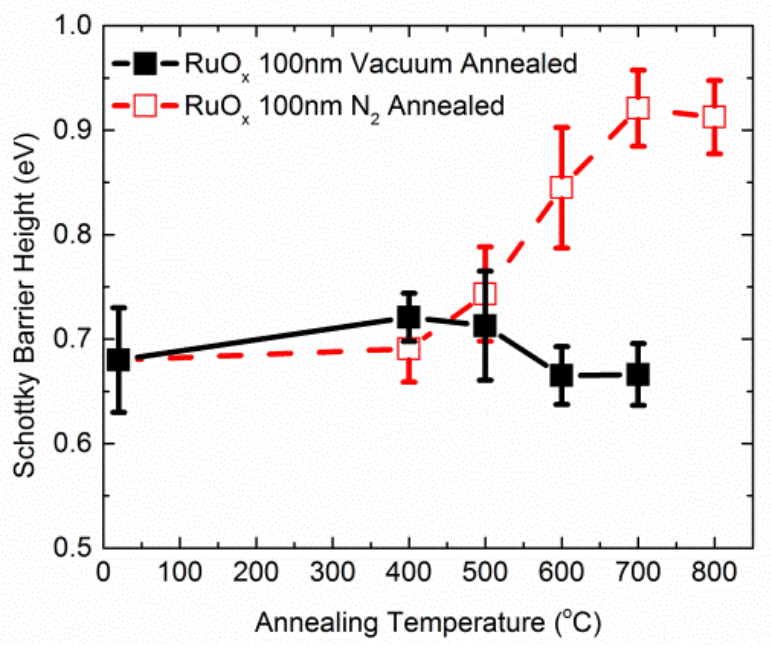

Figure 4.2 The effects of annealing temperatures on Schottky Barrier Height (SBH) of RuO_x Schottky diodes on n-GaN-on-Si(111) substrate, annealed in N_2 and vacuum for 1 minute.

The XRD spectra of RuO_x annealed in vacuum and N_2 are shown in Figure 4.3(a) and Figure 4.3(b), respectively. No XRD peaks are seen in RuO_x prior to annealing due to the amorphous nature of the as-deposited RuO_x. With annealing in vacuum, as shown in Figure 4.3(a), only Ru peaks (no RuO_2 peaks) are observed and the intensity of Ru peaks increases with increasing annealing temperature, thus resulting in Ru rich RuO_x Schottky contacts. On the other hand, with annealing in N_2, only RuO_2 peaks are observed, as shown in Figure 4.3(b), and the peak intensity enhances with increasing annealing temperature, which is expected to result in an increasingly RuO_2 rich RuO_x Schottky contacts. As Ru has a lower work function compared to RuO_2 (4.7 eV versus 5.1 eV), Ru rich RuO_x is likely to have a lower SBH. Hence, the decrease in SBH of RuO_x Schottky diodes annealed in vacuum (from 0.72 to 0.65 eV) with increasing annealing temperature (as shown in Figure 4.2) could be due to the increased content of Ru in RuO_x. Similarly, the increased presence of RuO_2 in the RuO_x contact annealed in N_2 is probably responsible for the increase in the SBH from 0.62 to 0.9 eV as shown in Figure 4.2, and has helped to reduce the leakage current. However, there is also a possibility of the formation of a thin insulator/oxide layer at the interface between RuO_x and substrate (resulting in MIS diode) with increasing annealing temperature in N_2, which may further increase the SBH and decrease the leakage current as discussed by Jeon et al [102]. We have also investigated on the possible formation of an interfacial oxide layer between RuO_x and InAlN by means of SIMS, and TEM and these will be reported in Chapter 7.

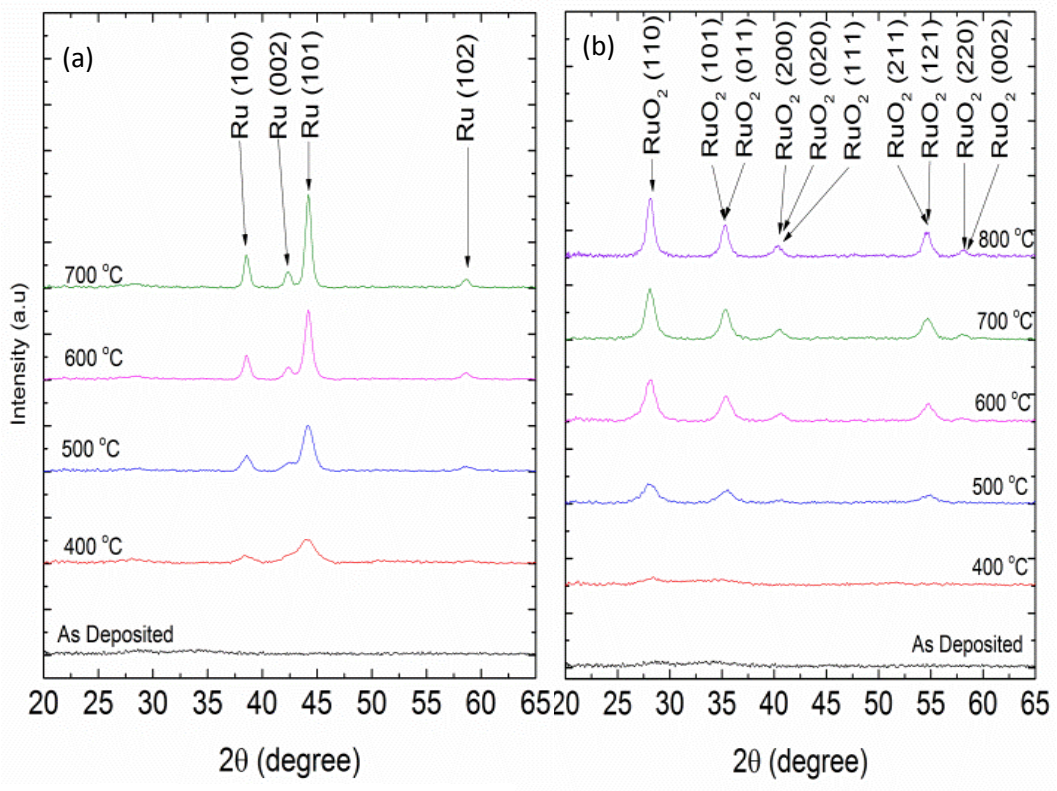

Figure 4.3 XRD spectra of RuO_x annealed in (a) vacuum and (b) N_2 at 400, 500, 600 and 700°C for 1 minute.

The *I-V* characteristics of RuO_x and Ni/Au Schottky diodes on $In_xAl_{1-x}N$/GaN -on-Si(111) annealed at 5 different temperatures (400, 500, 600, 700 and 800°C) in N_2 for 1 minute, are shown in Figure 4.4(a) and Figure 4.4(b). The leakage current of RuO_x Schottky diodes at –40 V decreases from 5×10^{-4} to 1×10^{-5} Acm^{-2} when the annealing temperature is increased to 800°C in N_2. In contrast, the leakage current of Ni/Au Schottky diodes increases from 3×10^{-2} to 2×10^{-1} Acm^{-2} at – 40 V. In addition, the extracted SBHs of RuO_x and Ni/Au Schottky diodes are shown in Figure 4.5. The SBH of Ni/Au Schottky diodes on $In_xAl_{1-x}N$/GaN-on-Si(111) substrates fluctuates between 0.85 and 0.9 eV when annealed in N_2 at different temperatures up to 800°C. On the other hand, the SBH of RuO_x Schottky diodes on $In_xAl_{1-x}N$/GaN-on-Si(111) increases from 0.9 to 1.24 eV with increasing annealing temperature up to 800°C. These

observations clearly indicate that RuO_x is more thermally stable compared to the conventional Ni/Au and Ni/W Schottky gate contacts reported in Chapter 3); hence, RuO_x is possibly a better gate contact for nitride based HEMTs.

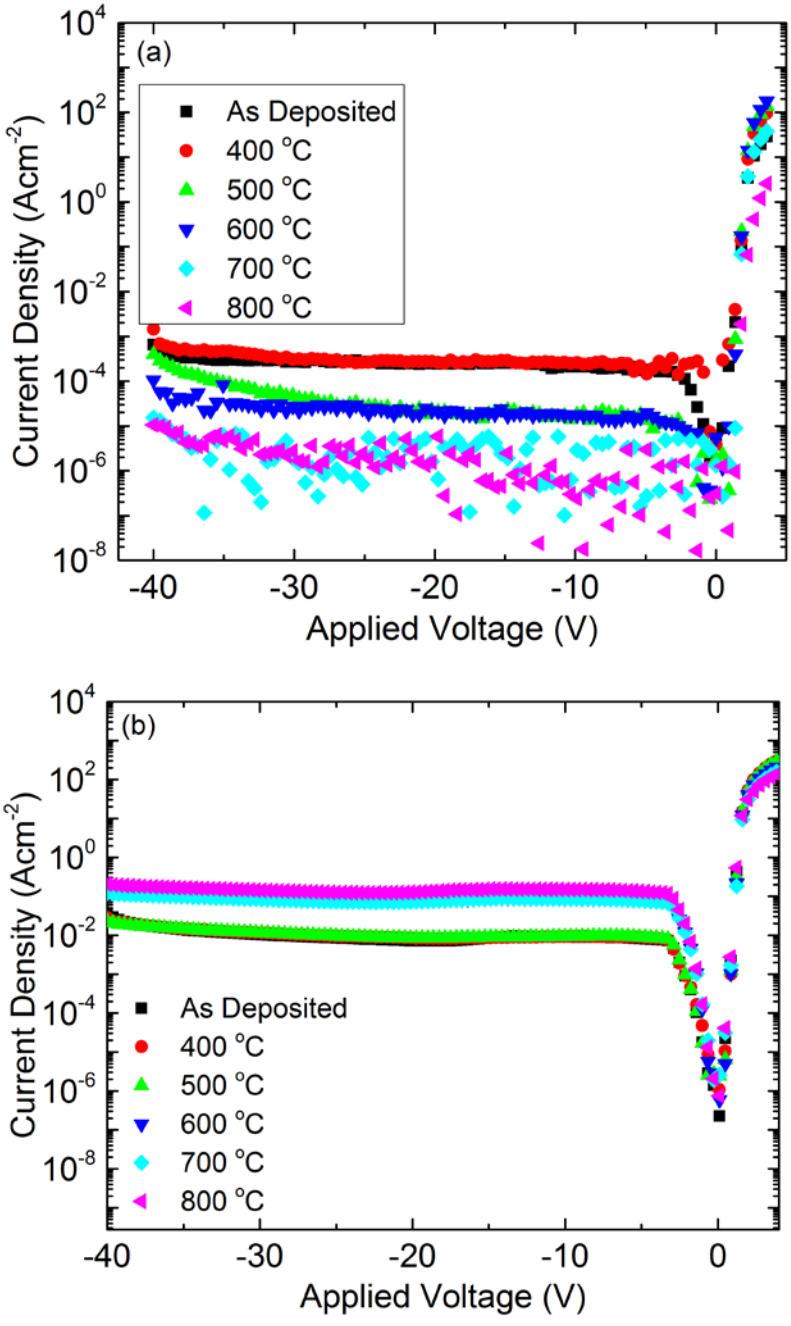

Figure 4.4 *I-V* characteristics of (a) RuO_x and (b) Ni/Au Schottky diodes on $In_{0.17}Al_{0.83}N$/GaN-on-Si(111) HEMTs, for various annealing temperatures in N_2. The annealing duration is 1 minute and the Ohmic contacts are Ti/Al/Ni/W (25/200/40/50 nm).

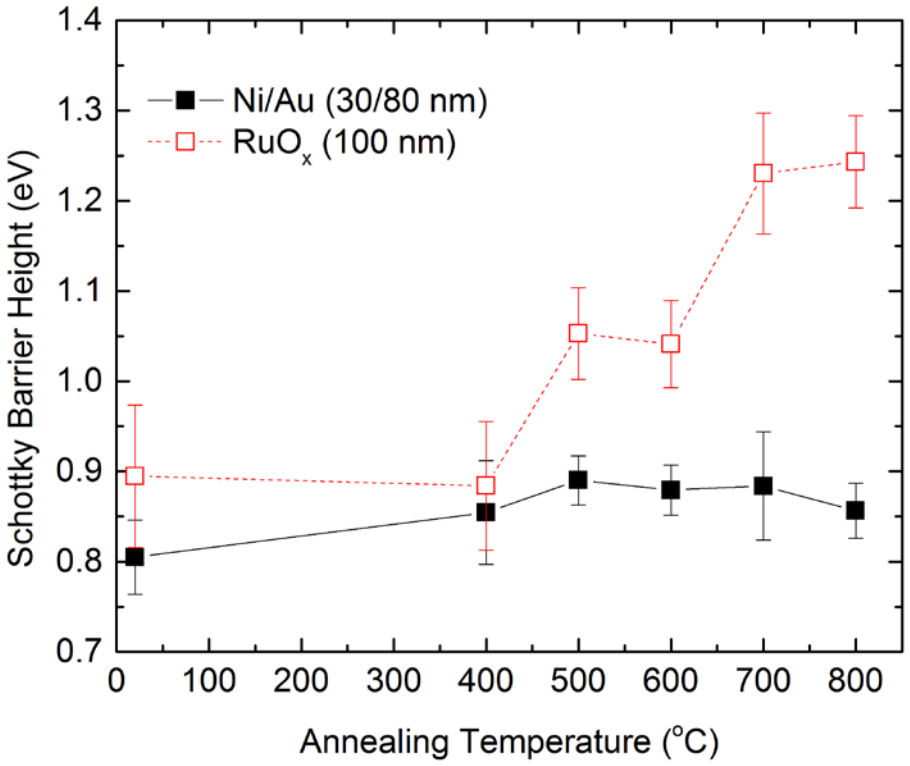

Figure 4.5 The effect of annealing temperature on Schottky Barrier Height (SBH) of RuO_x and Ni/Au on $In_xAl_{1-x}N$/GaN /Si (111) Schottky diodes annealed in N_2 for 1 minute.

An increase in Ohmic contact resistance by ~64% to 1.03 ± 0.1 Ωmm is observed for RuO_x Schottky diodes on $In_{0.17}Al_{0.83}N$/GaN-on-Si(111) annealed at 800°C compared to Ohmic contact before gate annealing. This change in Ohmic contact resistance would greatly affect HEMT electrical performance. Therefore, a lower annealing temperature of 700°C would provide the best post gate annealing conditions for the fabrication of RuO_x-based $In_{0.17}Al_{0.83}N$/GaN-on-Si(111) HEMTs.

$In_{0.17}Al_{0.83}N$/GaN-on-Si(111) HEMTs were fabricated using RuO_x as the Schottky gate contact and Ti/Al/Ni/W (25/200/40/50 nm) as the source/drain Ohmic contacts. The gate length is 1.5 µm with a gate width of 2×50 µm, and the drain to source spacing is 5 µm. The gate is placed mid-way between the

source and drain. Figure 4.6 shows the I_G-V_{GS} characteristics of the RuO_x Schottky gate $In_xAl_{1-x}N$/GaN HEMTs annealed at 700°C in N_2 for 1 minute. It can be clearly seen that RuO_x Schottky gate contact exhibits a low gate leakage current of 6×10^{-8} A/mm at –8V after annealing at 700°C. The extracted resistivity of RuO_x film annealed at 700°C is ~806 ± 17.4 nΩm which is ~10 times higher than the resistivity of Ni/W (350/50 nm).

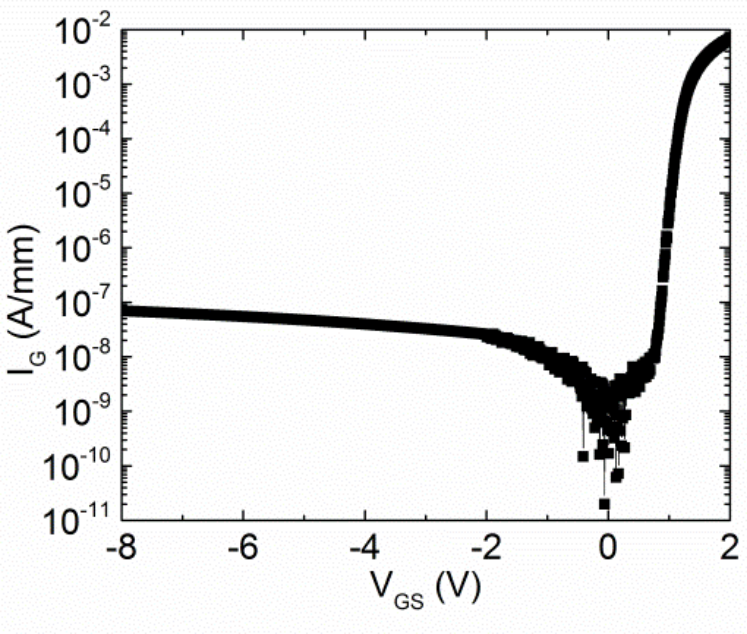

Figure 4.6 I_G-V_{GS} characteristics (with floating drain) of RuO_x Schottky gate $In_xAl_{1-x}N$/GaN-on-Si (111) HEMT, with the gate annealing at 700°C in N_2.

Figure 4.7 shows the plots of saturation drain current (I_D) and transconductance (g_m) versus V_{GS} of Schottky gate $In_xA_{1-x}N$/GaN-on-Si(111) HEMTs with gate annealing at 700°C. Figure 4.8 depicts the I_D-V_{DS} characteristics of these HEMTs. The characteristics were studied using the pulsed DC measurement system. The threshold voltage of HEMT, V_{TH}, is observed to be about – 2V. With the low gate leakage current (see Figure 4.6), the off-current of HEMTs is ~5×10^{-6} A/mm, hence resulting in an ON-OFF

current ratio of ~10^5. As shown in Figure 4.7, g_m of about 0.18 S/mm is achieved by our HEMTs. With this transconductance, the I_{DSAT} is about 0.41 A/mm at V_{GS} = 1 V, as seen in Figure 4.8.

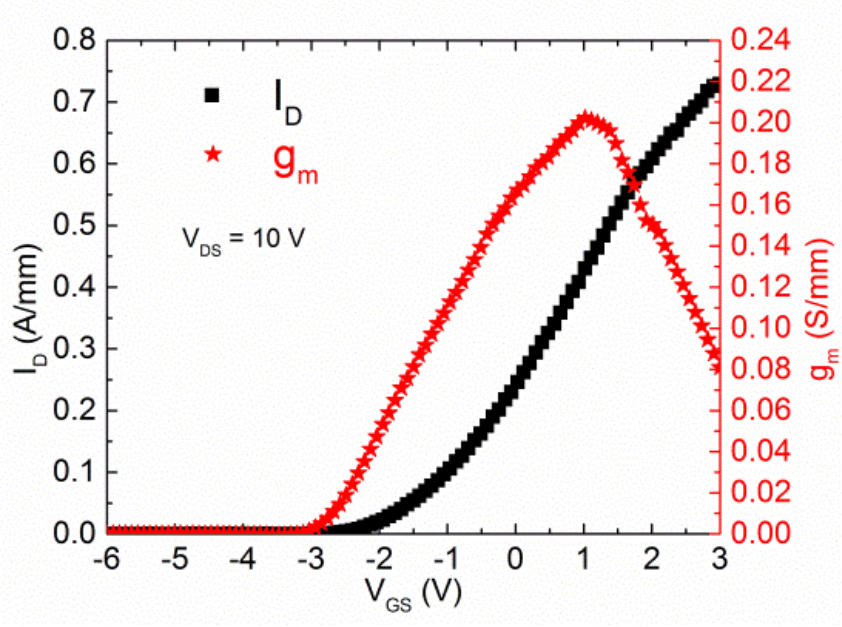

Figure 4.7 The I_D and g_m versus V_{GS} characteristics of RuO_x Schottky gate $In_xAl_{1-x}N$/GaN-on-Si (111) HEMT, with gate annealing at 700°C in N_2.

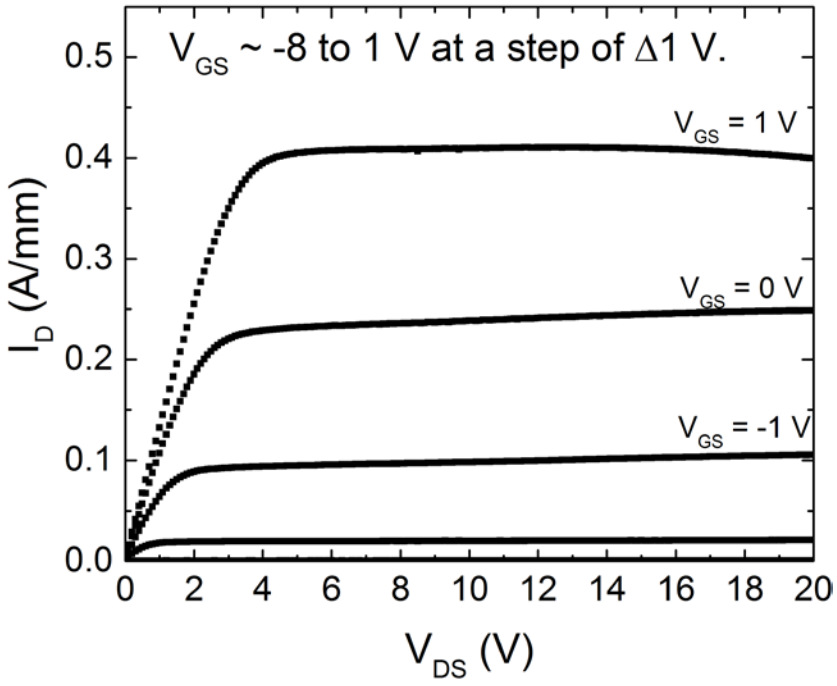

Figure 4.8 I_D-$V_{DS(pulsed)}$ characteristics of RuO_x Schottky gate $In_xAl_{1-x}N$/GaN-on-Si(111) HEMTs, annealed at 700°C.

The contact resistance (R_c) of Ti/Al/Ni/W (25/200/40/50 nm) source/drain Ohmic contacts before gate deposition and after post gate annealing at 700°C are 0.63 ± 0.05 and 0.72 ± 0.06 Ωmm, respectively; which do not have much effect on the change in R_{on}. The R_{sh} measured from TLM is about 2.57 ± 0.09 Ωmm. Since the measured ON-resistance, R_{on}, is ~8.33Ωmm and $R_{on} = R_{channel} + R_c + R_{sh}$, it is believed to be contributed and influenced more by the channel resistance ($R_{channel}$) and sheet resistance (R_{sh}) and less dependent on the contact resistance (R_c).

4.4 Conclusion

In summary, we have investigated the influence of post sputtering annealing ambient and temperature on the characteristics of RuO_x Schottky diodes on n-GaN grown on Si(111) substrate. RuO_x Schottky contacts on n-GaN on Si(111) substrate exhibit a SBH of 0.9 eV and a leakage current of 10^{-5} Acm^{-2} at – 2 V after annealing in N_2 at 700°C. Furthermore, RuO_x has been found to be more thermally stable than Ni/Au because RuO_x Schottky diodes have a lower leakage current and a higher SBH (~0.4 eV) than Ni/Au Schottky diodes when both are annealed at 800°C. By using RuO_x, instead of Ni/Au, as the Schottky gate contact in $In_xAl_{1-x}N$/GaN-on-Si(111) HEMTs, the ON-OFF current ratio is boosted to ~10^5, after gate annealing at 700°C in N_2. Furthermore, the maximum transconductance of ~0.18 S/mm and ON-resistance of ~8.33 Ωmm are achieved for a gate length of 1.5 μm. Therefore, gold-free HEMTs with RuO_x as a thermally robust gate contact, leading to a reduced leakage and OFF current, are suitable for high temperature applications.

Chapter 5: Thermally robust RuO_x based $Al_xGa_{1-x}N$/GaN Schottky HEMTs on 200 mm diameter Si(111) substrates

5.1 Introduction

In Chapter 4, we have shown the superior electrical characteristics of RuO_x Schottky contact over the traditional Schottky contact (Ni/Au) using InAlN/GaN heterostructure grown on 100 mm diameter Si(111) substrate. In addition, we have highlighted the low leakage InAlN/GaN HEMTs on 100 mm Si(111) using RuO_x Schottky contact as a gate. Since AlGaN/GaN HEMTs have higher 2DEG mobility while lower 2DEG concentration than InAlN/GaN HEMTs, they have similar potential as InAlN/GaN HEMTs for high speed, high power and high temperature applications. Currently, $Al_xGa_{1-x}N$/GaN heterostructures are usually grown on silicon (Si) and silicon carbide (SiC) substrates for power electronic applications. Although the quality of GaN grown on Si is not yet as good as that on SiC, epitaxy scale up on 200 mm diameter Si would eventually reduce the cost of GaN HEMT processing. With CMOS compatible gold-free contacts, these substrates can be processed in existing 200 mm Si foundries thus reducing the fabrication cost further. Therefore, our aim is to also investigate the annealing temperature dependent electrical characteristics of RuO_x Schottky gate contact on $Al_xGa_{1-x}N$/GaN HEMTs. In this chapter, we report on the electrical characteristics of $Al_xGa_{1-x}N$/GaN HEMT structures grown on 200 mm diameter Si(111) substrates. We will also present an in-depth study on the effect of different gate annealing temperatures (600, 700, 800, and 900^oC) on the electrical characteristics of $Al_xGa_{1-x}N$/GaN HEMTs on such 200 mm Si. The device characteristics in this

study highlight the application potentials of $Al_xGa_{1-x}N$/GaN HEMTs realized by 200 mm diameter GaN on Si epitaxy.

5.2 Experimental Procedures

The $Al_xGa_{1-x}N$/GaN HEMT structure used was grown on a 1.0 mm thick, 200 mm diameter Si(111) substrate by means of a refurbished AIXTRON CCS MOCVD system at Institute of Material Research and Engineering (IMRE). Figure 5.1(a) shows the scanning transmission electron microscopy (STEM) image of the full HEMT structure in high angle annular dark-field (HAADF) imaging mode. The total thickness of the nitrides stack is about 4.3 µm. The layer structure includes a 400 nm thick AlN nucleation layer, three step-graded $Al_xGa_{1-x}N$ intermediate layers (AlGaN I, AlGaN II, and AlGaN III) with a composition tuning range of Al from 60 to 20%, followed by an uninterrupted growth of GaN with a thickness >2.3 µm without any interlayer. The HEMT structure consists of a thin AlN spacer (~1.0 nm), an $Al_{0.24}Ga_{0.76}N$ barrier layer (21 – 22 nm) and a top undoped GaN (4.0 – 5.0 nm) cap layer. The z-contrast HAADF-STEM image of the top GaN/$Al_xGa_{1-x}N$/AlN/GaN interfaces is also shown in Figure 5.1(b). The cross-sectional TEM measurements show sharp interfaces of the nucleation and buffer layers. The growth of a thick uninterrupted GaN layer (>2.3 µm) was carried out to reduce the dislocation density at the top GaN channel.

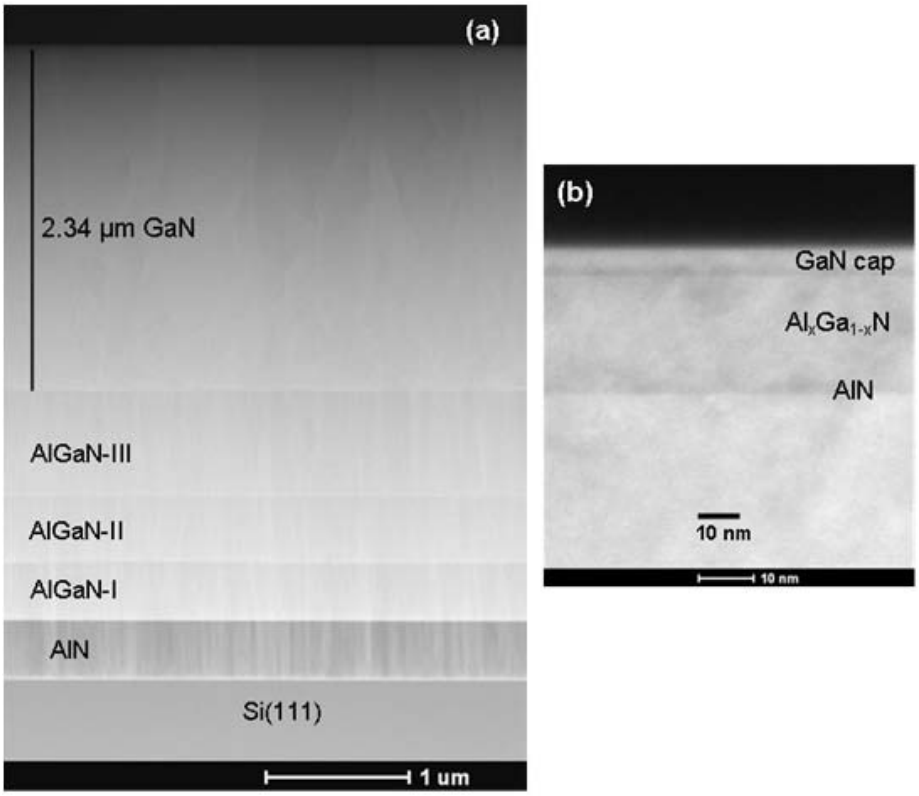

Figure 5.1 (a) The HAADF-STEM image of the full HEMT structure highlighting the thick AlN nucleation layer, multiple AlGaN layers and GaN buffer. (b) STEM image of the top HEMT interfaces.

The HEMT fabrication process began with a mesa isolation using the BCl_3/Cl_2 gas mixture in an inductively coupled plasma (ICP) etching system. After the source/drain area was patterned using photolithography process, a recess etch (~ 50 nm depth) was performed and the processing steps were followed by the formation of Au-free Ohmic contact, Ti/Al/Ni/W (25/200/40/50 nm) by means of sputtered deposition and metal lift-off process. The source/drain metal stack was then annealed at 900^oC in vacuum for 1 minute for the formation of Ohmic contacts. After patterning of the gate area, Au-free Schottky gate contact, RuO_x (~ 100 nm), was deposited by sputtering Ru in Ar/O_2 (20/10 sccm) ambient. The RuO_x contacts were then formed by metal lift-off as well

and followed by annealing at 4 different temperatures (600, 700, 800 and 900^{o}C) in N_2 for 1 minute to study the effects of rapid thermal annealing temperature on the device performance of unpassivated HEMTs. The dimensions of the HEMTs are as follows: the gate to drain distance, L_{gd} ~ 10 µm; the gate to source distance, L_{gs} ~ 2 µm; the gate length, L_g ~ 1.5 µm; and the gate width, W_g = 2 × 50 µm.

5.3 Results and Discussions

The Hall effect measurements were carried out in sample pieces diced from the 200 mm epiwafers. Sheet resistance, R_{sh}, in the range of 326 – 390 Ω/sq; a variation of electron mobility from 1540 to 1380 to cm^2/Vs; and a sheet carrier concentration variation of 1.08 × 10^{13} to 1.35 × 10^{13} cm^{-2} are observed. The uniformity and repeatable performance of the devices fabricated from such 200 mm epiwafers are complemented by studying the direct-current (dc) characteristics of the HEMTs. The effect of annealing temperature on the gate performance is shown in Figure 5.2(a). The gate leakage current, I_G, of HEMTs annealed at 600^{o}C is < 10^{-7} A/mm at – 40 V. There is an insignificant change in gate leakage current at – 40 V when HEMT annealing temperature was increased to 800^{o}C. This leakage current is comparable to that of Ni/Pt/Au annealed at 600^{o}C [103], while it is better than those of the conventional Ni/Au annealed at lower temperature (400^{o}C) [104, 105]. When annealed at 900^{o}C, the gate leakage current is still less than 10^{-7} A/mm up to – 20 V. However, above – 20 V, the gate leakage current increases and at – 40 V, it reaches ~3 × 10^{-6} A/mm (about an order of magnitude increase compared to HEMTs with annealing temperature up to 800^{o}C). The effective Schottky Barrier Heights (SBHs) of RuO_x on AlGaN/GaN heterostructures change

insignificantly with annealing temperature and the values are 0.85 ± 0.02, 0.81 ± 0.02, 0.82 ± 0.02, and 0.81 ± 0.06 eV at 600, 700, 800 and 900^{o}C respectively. The ideality factor is about 2.0 ± 0.2 at all annealing temperatures which indicates that the defect-assisted field emission current dominates in gate leakage current [42].

Figure 5.2(b) shows the typical static I_D (in log scale) as a function of V_{GS} at V_{DS} = 10 V when the gate is annealed at 4 different temperatures (600, 700, 800 and 900^{o}C). OFF current (I_{OFF}) of HEMTs with annealing temperature of up to 900^{o}C is about 10^{-8} A/mm. I_{OFF} is similar across the range of annealing temperatures because at V_{GD} = -16 V, as shown in Figure 5.2(a), the gate leakage current of HEMTs is < 10^{-7} A/mm. With this low I_{OFF}, the ON-OFF current ratio of > 10^{7} is achieved for all HEMTs with different gate annealing temperatures. The sub-threshold swing (*SS*) of HEMT is extracted in the I_D range from 10^{-7} to 10^{-4} A/mm and is found to be about 90 mV/decade and is insignificantly affected by annealing temperature up to 800^{o}C. Therefore, the control of gate contact over the channel is still good even when HEMT is annealed at 800^{o}C. The threshold voltage, V_{TH}, of HEMTs annealed at different temperatures up to 800^{o}C is ~ -2.3 ± 0.2 V. However, there is a positive shift in V_{TH} and increase in *SS* for HEMTs annealed at 900^{o}C. The values of V_{TH} and *SS* of HEMTs annealed at 900^{o}C are -2 V and 180 mV/dec, respectively. The increase in *SS* is due to the increased acceptor like traps at the interface which results in flat band voltage shift and the decrease in gate capacitance as shown in Figure 5.3(a), which shows the gate capacitance, C_G, as a function of gate to source voltage, V_{GS}, and annealing temperature. The maximum gate accumulation capacitances (C_{GA}) of HEMTs annealed at 600,

700, and 900°C are ~3.6×10^{-7}, ~3.75×10^{-7} and ~3.3×10^{-7} Fcm^{-2}, respectively. The decrease in C_{GA} will result in the decrease in channel *2DEG* density at gate annealing temperature 900°C, hence, decreasing the transconductance (g_m) and drain saturation current (I_{DSAT}), while increasing the value of ON-state resistance (R_{on}).

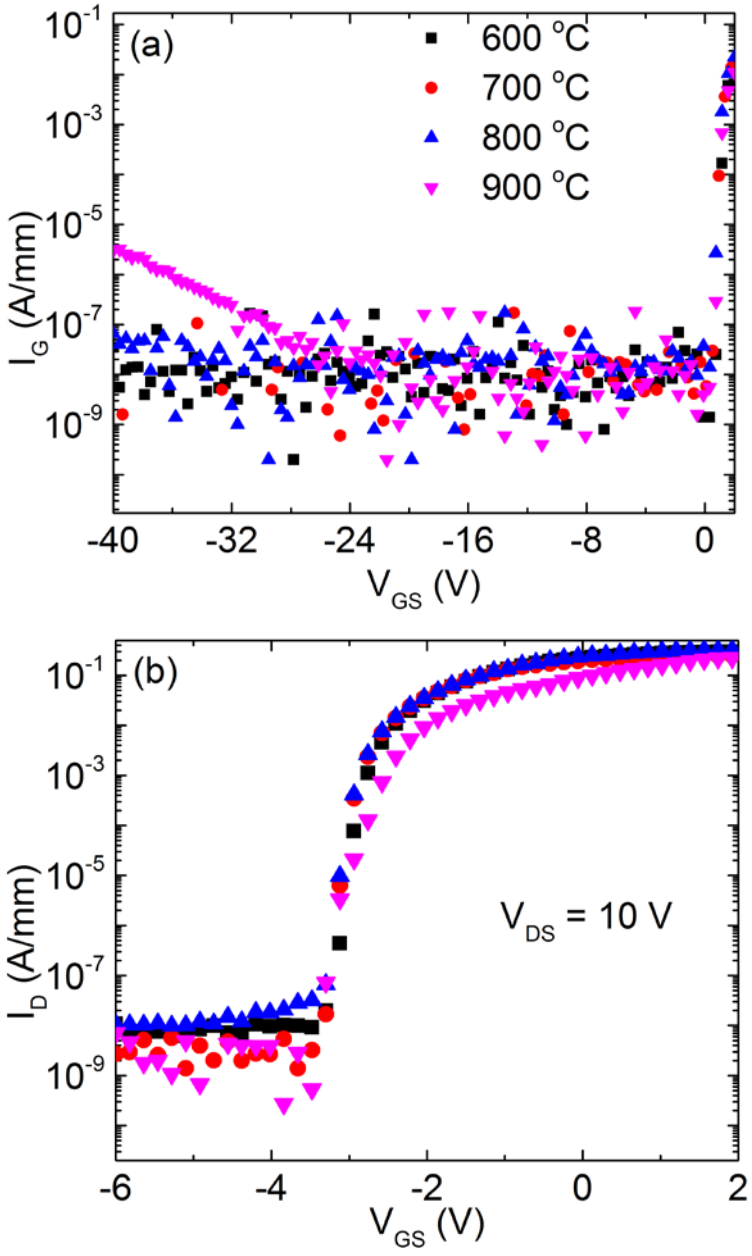

Figure 5.2 The effect of gate annealing temperature on (a) gate leakage currents at V_{DS} = 0 V (b) drain currents (log scale) at V_{DS} = 10 V as a function of V_{GS} in HEMTs fabricated with 1.5 µm RuO_x gate.

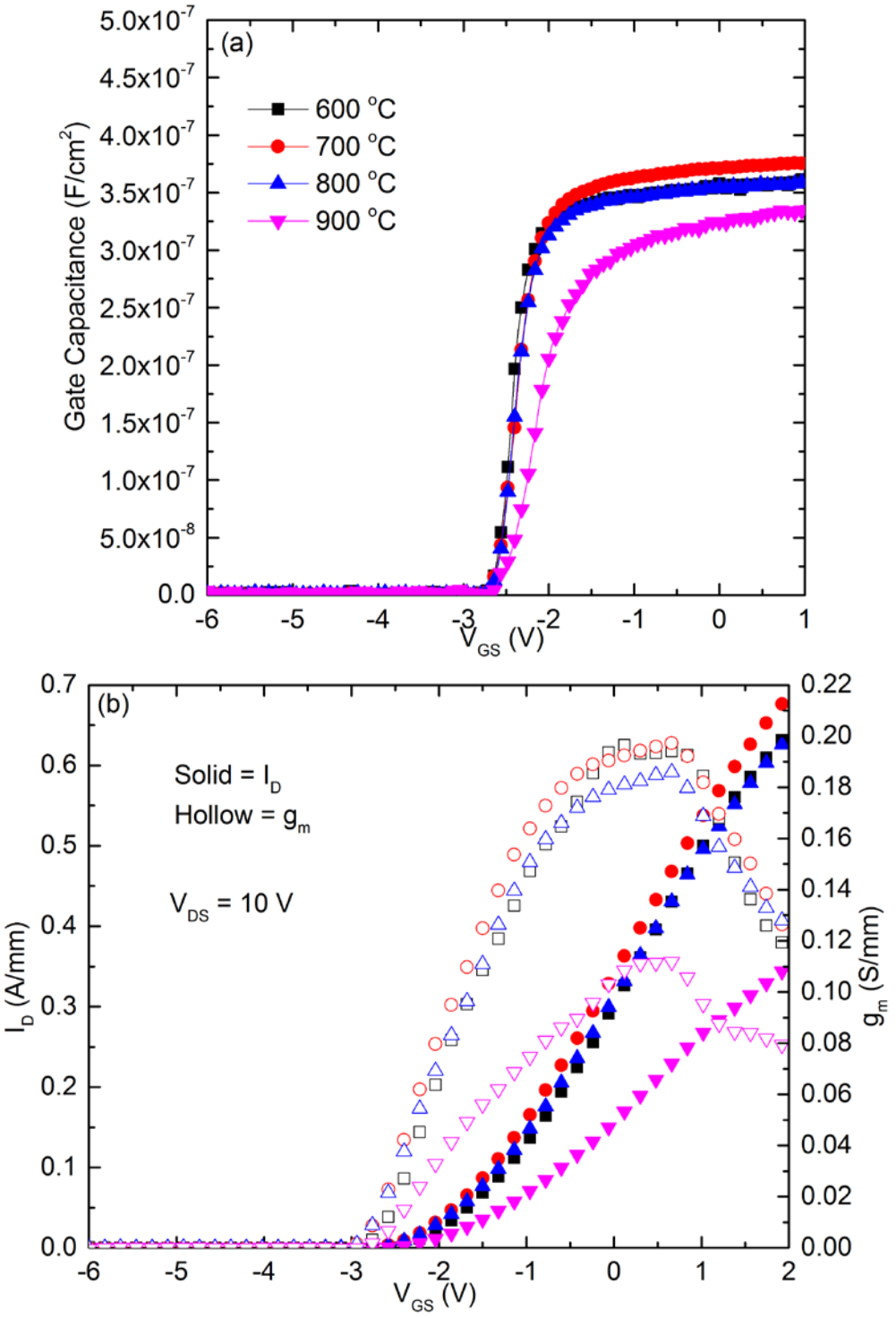

Figure 5.3 The characteristics of 1.5 μm RuO_x HEMT's (a) gate capacitance and (b) I_D and g_m with respect to annealing temperature and V_{GS}.

Figure 5.3(b) shows the effect of annealing temperature on g_m and the drain current, I_D, (in linear scale) as a function of V_{GS} at V_{DS} = 10 V. HEMTs

annealed at 700°C achieve the highest g_m at different V_{GS} due to the highest C_{GA}. The maximum g_m achieved is about 0.197 S/mm for HEMTs annealed at 600 and 700°C. However, it decreases to 0.186 S/mm and 0.115 S/mm after annealing at 800 and 900°C, respectively. The maximum drain currents, $I_{DSAT(max)}$, of HEMTs annealed at 600, 700, 800 and 900°C are 0.5 ± 0.01, 0.55 ± 0.03, 0.5 ± 0.03 and 0.3 ± 0.04 A/mm, respectively, at a gate overdrive voltage of ~ 3.3 V. Figure 5.4 shows the I_D-$V_{DS(pulsed)}$ characteristics of HEMTs at different annealing temperatures. Pulsed measurement is used to lower the effect of self-heating on the device performance. $I_{DSAT(max)}$, is the highest for an annealing temperature of 700°C, and it decreases with increasing annealing temperature beyond that (i.e, at 800 and 900°C), as shown in Figure 5.4. Current collapse resulted from our unpassivated HEMT surface is observed.

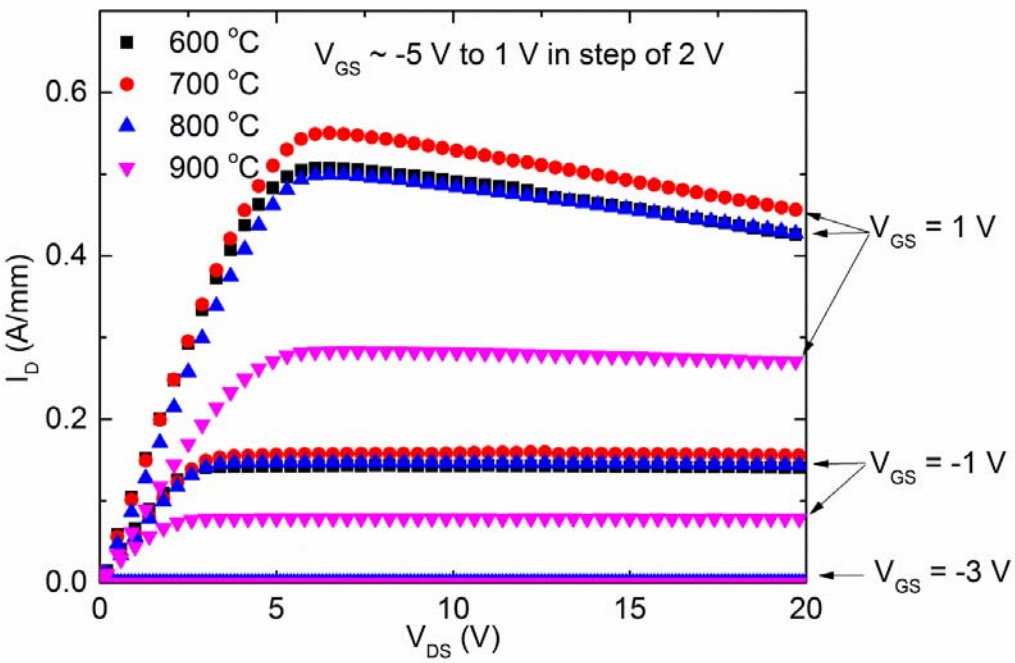

Figure 5.4 The effect of annealing temperature on I_D as a function of V_{DS} *and* V_{GS}.

Table 5.1 summarizes the ON-resistance (R_{on}), contact resistance (R_c), and sheet resistance (R_{sh}) as a function of annealing temperature. It can be observed that R_c of the Ohmic contact, Ti/Al/Ni/W (25/200/40/50 nm), is stable up to 700^{o}C, above which it degrades and becomes pseudo Ohmic at 900^{o}C. The increase in R_c with increasing annealing temperature results in higher R_{on}. HEMTs annealed at 600^{o}C have R_{on} ~ 9.02 ± 0.35Ω.mm, and it increases with increasing annealing temperature above 800^{o}C. At 900^{o}C, it becomes 16.1 ± 2.2 Ω.mm. On the other hand, there is no significant change in sheet resistance, R_{sh}. Therefore, the decrease in $g_{m(max)}$, and I_{DSAT} of HEMTs annealed at 900^{o}C are resulted mainly from the decrease in C_{GA}. On the other hand, the increase in R_{on} is contributed by not only the decrease in C_{GA} but also the increase in R_c when annealed at 900^{o}C.

Table 5.1 The values of On-resistance, R_{on}; contact resistance, R_c; and sheet resistance, R_{sh} as a function of annealing temperature of the $Al_xGa_{1-x}N$/GaN HEMT structure on a 200 mm diameter Si(111).

Annealing Temp T(^{o}C)	On Resistance R_{on}(Ω.mm)	Contact Resistance R_c (Ω.mm)	Sheet Resistance R_{sh} (Ω/□)
600	9.02 ± 0.35	1.4 ± 0.2	482 ± 20
700	8.83 ± 0.22	1.4 ± 0.3	497 ± 19
800	9.47 ± 0.57	1.5 ± 0.2	464 ± 24
900	16.1 ± 2.2	2.88 ± 1.0	511 ± 40

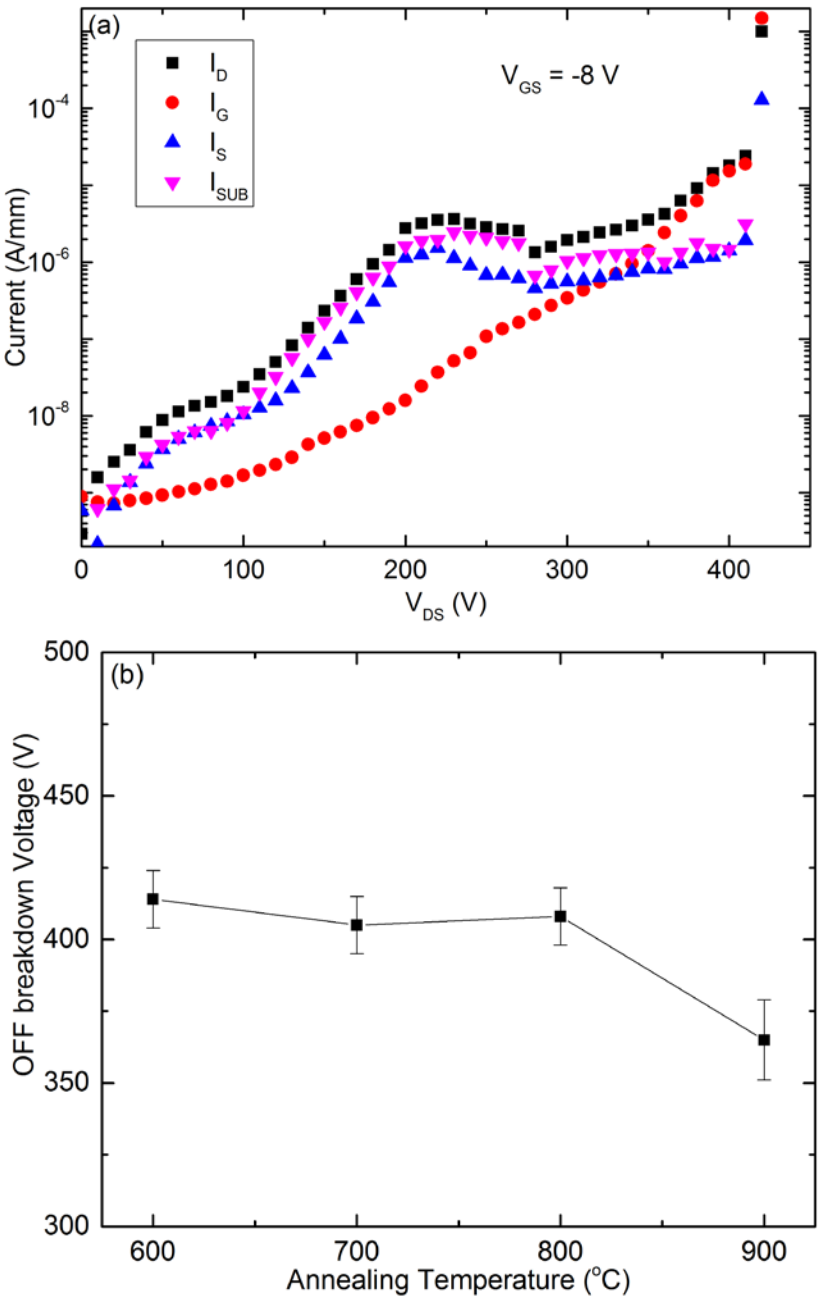

Figure 5.5 (a) Leakage currents of HEMT annealed at 600°C as a function of drain to source voltage. (b) OFF-state breakdown voltage as a function of RuO_x annealing temperature.

Figure 5.5(a) shows the leakage currents of HEMTs annealed at 600°C as a function of drain voltage. The drain, gate and source currents (I_D, I_G and I_S) are measured while the substrate current (I_{SUB}) is extracted using Kirchhoff's current law. It can be observed that the OFF-state breakdown is due to the gate

leakage. This is also true at other annealing temperatures. The OFF breakdown voltages of HEMTs annealed at 600, 700, 800 and 900^{o}C are 414 ± 10, 404 ± 10, 405 ± 10 and 360 ± 15 V, respectively as shown in Figure 5.5(b). It is observed in Figure 5.5(a) that I_D and I_S decreases when V_{DS} is between 240 and 280 V. This reduction could be resulted from the trapping of the charge carriers in the electric field dependent traps between gate and drain region which were activated between V_{DS} of 240 and 280 V. The demonstrated Au-free HEMTs are stable up to 800^{o}C with insignificant changes in R_{on}, g_m, I_{DSAT}, I_G, ON-OFF current ratio, and breakdown voltage. This stability is resulted from the structural quality $Al_xGa_{1-x}N$/GaN heterostructures and the electrical contacts.

The changes in C_{GA}, V_{TH}, and gate leakage current at 900^{o}C could be due to the following reason. The interfacial oxide (Ga based oxide) could be formed at the interface between RuO_x contact and GaN cap layer during the deposition of sputtered RuO_x. Due to the use of a sputtering process in Ar and O_2 ambient for the deposition of RuO_x layering on top of thin GaN cap, there is a possibility of GaO formation at RuO_x/GaN/$Al_xGa_{1-x}N$ upon annealing. This phenomenon is expected to be similar to the formation of the interfacial oxide (Al based oxide) at the interface between $In_{0.17}Al_{0.83}N$ and RuO_x during RuO_x deposition which will be reported in Chapter 7. This interfacial oxide is possibly in the range of a few nm such that there is an insignificant effect on gate capacitance. As the annealing temperature increases, the interfacial oxide thickness may increase thus reducing the effective AlGaN barrier layer contribution. At 900^{o}C, the oxide capacitance could contribute significantly that result in a decrease of the gate capacitance. V_{TH} shifts toward positive side

as seen in Figure 5.3(a) at 900^{o}C may arise due to the above reasons. Furthermore, observation of an increase in leakage current at 900^{o}C could be resulted from such gallium-based oxide degradation above annealing temperature of 850^{o}C [106].

The fabricated HEMTs show an improved ON/OFF current ratio and a lower SS value, where such parameters are influenced by the structural quality of $Al_xGa_{1-x}N$/GaN 2DEG heterostructures, the GaN buffer, and the nature of gate contacts at top interfaces. An ON/OFF current ratio of 10^5 in HEMTs was previously reported[107], using a buffer structure where GaN layer was embedded with low-temperature thin AlN interlayers. The presence of line defects and electrical non-uniformity at these multiple interlayers often creates high leakage paths. Therefore, to reduce defect density in the GaN buffer/channel regions and substrate leakage, we have employed a combination of relatively thicker AlN nucleation and AlGaN intermediate layers, and an improved thick uninterrupted GaN growth >2.2 µm. Such combinations with good electrical contacts results in an improvement in electrical properties of HEMTs on 200 mm diameter Si.

5.4 Conclusion

In summary, we have demonstrated Au-free HEMTs using the $Al_xGa_{1-x}N$/GaN heterostructures grown on 200 mm diameter Si(111) for high temperature applications. The source/drain Ohmic contact (Ti/Al/Ni/W) is insignificantly affected by the RuO_x gate with annealing temperature up to 800^{o}C resulting in little changes in R_c and R_{on}. Furthermore, the Schottky contact (RuO_x) is thermally stable up to 800^{o}C without much degradation in g_m and I_{DSAT}.

However, at 900^{o}C, the Ohmic and Schottky contacts degrade and lead to a reduction in g_m and I_{DSAT}, and an increase in R_{on}. The maximum g_m, I_{DSAT} and minimum R_{on} achieved are 0.197 S/mm, 0.55 A/mm and 8.83 Ωmm, respectively, for a 1.5 μm gate HEMT when the gate is annealed at 700^{o}C. We have also achieved the ON-OFF current ratio >10^7 and sub-threshold swing of 90 mV/decade for HEMT annealed up to 800^{o}C. Owing to an improved crystalline quality of $Al_xGa_{1-x}N$/GaN heterostructures and contacts, we have demonstrated AlGaN/GaN HEMTs with electrical characteristics stable up to gate annealing at 800^{o}C; hence, showcasing its potential for high power and high temperature applications.

Chapter 6: Probing channel temperature profiles of semitransparent RuO_x based Schottky contacts on InAlN/GaN HEMTs and AlGaN/GaN HEMTs on 200 mm diameter Si(111) by optical spectroscopy

6.1 Introduction

In our previous chapters, we have demonstrated low leakage thermally robust RuO_x based gate contact on $In_xAl_{1-x}N$/GaN HEMTs and $Al_xGa_{1-x}N$/GaN HEMTs. For applications in high voltage electronics, it is desirable to realize stable and repeatable growth and device processing technologies for such $In_xAl_{1-x}N$/GaN and $Al_xGa_{1-x}N$/GaN heterostructures. These high power devices are prone to severe degradation resulted from the defects and dislocations in the structures at large electrical biases. These defects and dislocations could trap the heat leading to higher channel temperatures in devices under operation at large electrical biases. If no proper heat dissipation occurs in such device architectures, the high channel temperature enhances phonon scattering and thus, degradation of channel carrier mobility and saturation velocity occurs. As a result, the direct-current (DC) output characteristics degrade significantly, which is known as the *self-heating effect*. In GaN-based HEMTs increased channel temperature decreases the drain currents (I_{DS}) at higher drain voltages (V_{DS}). This *self-heating effect* limits the device performances thus affecting long-term reliability of GaN-based electronics. By observing the temperature profiles of HEMTs, design of HEMTs could be improved for better electrical characteristic. Since RuO_x has a band gap of 2.2 to 2.4 eV[61, 62], it is semitransparent to optical excitation wavelengths. This makes it possible for us to observe the temperature

distribution of HEMTs even underneath the gate. This temperature distribution would provide information on how high the operating temperature of HEMTs is and where the highest temperature region is. In this chapter, we report the channel temperature profiles in $In_xAl_{1-x}N$/GaN HEMTs and $Al_xGa_{1-x}N$/GaN HEMTs that were grown on 200 mm diameter Si(111) substrates using the ultra violet Photoluminescence (UV PL) spectroscopy (325 nm excitation) and visible Raman spectroscopy (488 nm excitation). The temperature calibration with respect to optical phonon and band-edge PL peak shifts has been carried out on the same device surface, which takes into account any line shape changes in optical spectra due to processing of such transistors on Si substrates. The results obtained from HEMTs show that it is possible to measure the channel temperature accurately including regions underneath the gate areas where most of the device *self-heating* takes place using RuO_x based gate contact.

6.2 Experimental Procedures

A refurbished AIXTRON CCS MOCVD system was used to grow both $Al_xGa_{1-x}N$/GaN and $In_xAl_{1-x}N$/GaN heterostructures on 1.0 mm thick 200 mm diameter Si(111) substrates. The total thickness of the nitrides stack of $Al_xGa_{1-x}N$/GaN heterostructure is ~4.3 – 4.4 µm while that of $In_xAl_{1-x}N$/GaN heterostructure is ~3.2 – 3.3 µm. Figure 6.1(a) and Figure 6.1(c) show the scanning transmission electron microscopy (STEM) of the full nitride stack of $Al_xGa_{1-x}N$/GaN and $In_xAl_{1-x}N$/GaN heterostructures, respectively, in high angle annular dark-field (HAADF) imaging mode. The $Al_xGa_{1-x}N$/GaN heterostructure includes a ~400 nm thick AlN nucleation layer, three step-graded $Al_xGa_{1-x}N$ intermediate layers (AlGaN I, AlGaN II, and AlGaN III)

with Al composition range from 60 to 20%, followed by an uninterrupted growth of GaN with a thickness 2.3 – 2.4 µm. The top heterostructure interfaces consist of a thin AlN spacer (~1.0 nm), an $Al_{0.24}Ga_{0.76}N$ barrier layer (21 – 22 nm) and undoped GaN (4.0 – 5.0 nm) cap layer. The z-contrast HAADF-STEM imaging carried out at the top GaN/Al_xGa_{1-x}N/AlN/GaN interfaces is shown in the inset(Figure 6.1(b)).

On the other hand, the typical layer structure of $In_xAl_{1-x}N$/GaN heterostructure consists of a ~300 nm GaN channel beneath the $In_xAl_{1-x}N$ barrier layer, about ~1.0 µm unintentionally carbon-doped GaN buffer, step-graded $Al_xGa_{1-x}N$ intermediate layers, and a ~325 nm AlN nucleation layer on Si(111). STEM imaging clearly probes the top ~ 9.65 nm $In_xAl_{1-x}N$ barrier layer and the underlying ~1 nm AlN spacer layer, as shown in the inset (Figure 6.1(d)). The post growth high-resolution reciprocal space mapping by x-ray diffraction confirms an In composition of ~17% in the ~9 nm thick HEMT barrier. The Hall data of $Al_xGa_{1-x}N$/GaN heterostructure shows an average sheet resistance, R_{sh}, of 358 Ω/sq; an electron mobility of 1460 cm^2/Vs with an average sheet carrier density of 1.19×10^{13} cm^{-2}. On the other hand, the Hall data of $In_xAl_{1-x}N$/GaN heterostructure shows an average R_{sh} of ~250 ohm/sq, electron mobility of 900 cm^2/Vs, with an average sheet carrier density ~2.7×10^{13} cm^{-2}.

For the processing of HEMTs, RuO_x (100 nm) was used as the Au-free gate contact while Ti/Al/Ni/W (25/200/40/50 nm) layers annealed at 900^oC were used as Au-free source and drain contacts. The devices were not passivated with any dielectric layers. For the temperature mapping study, we used specific dimensions of HEMTs where the gate to drain distance, L_{gd} ~ 9.5 µm; the gate to source distance, L_{gs} ~ 2 µm; the gate length, L_g ~ 2.5 µm; and the

gate width, W_g = 2 × 50 µm. The only difference between the fabrication process of $Al_xGa_{1-x}N$/GaN HEMTs and $In_xAl_{1-x}N$/GaN HEMTs was that a 50 nm deep recess etch process was performed before $Al_xGa_{1-x}N$/GaN HEMT Ohmic contact formation while no recess etch was performed before $In_xAl_{1-x}N$/GaN HEMT Ohmic contact formation. Therefore, Ohmic contacts of $Al_xGa_{1-x}N$/GaN HEMTs are physically in contact with 2DEG while those of $In_xAl_{1-x}N$/GaN HEMTs are not as shown in Figure 6.2. However, R_c of Ohmic contact on InAlN/GaN HEMT is much lower (0.62 ± 0.08 versus 1.4 ± 0.2Ω.mm) than that of Ohmic contact on $Al_xGa_{1-x}N$/GaN HEMT.

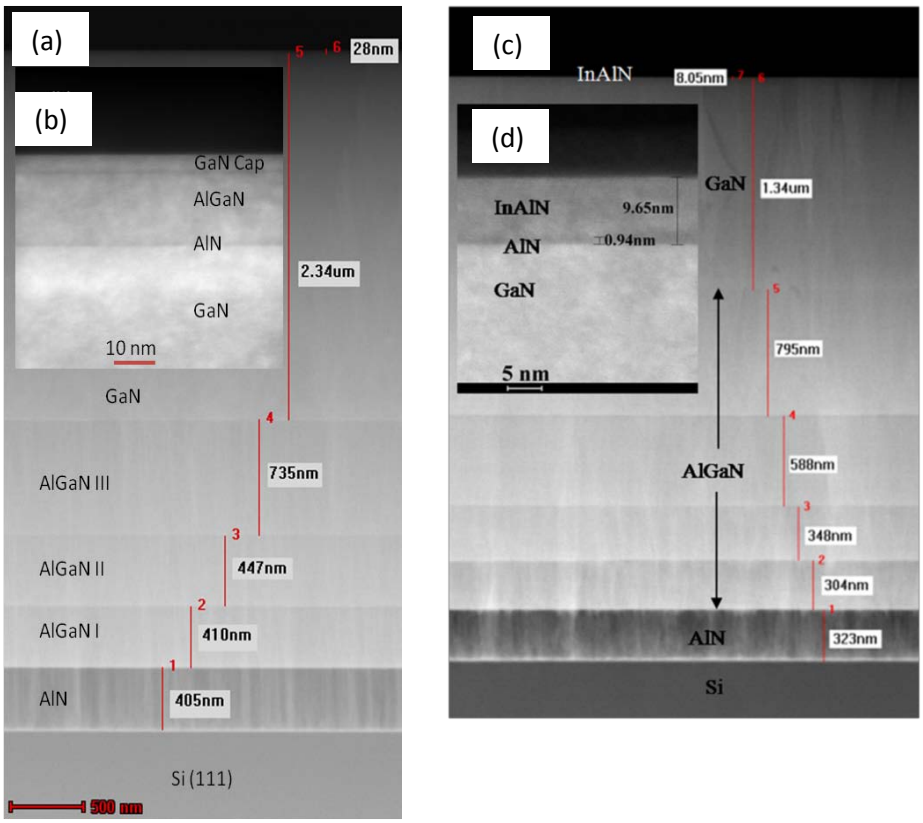

Figure 6.1 (a) The STEM image of the full $Al_xGa_{1-x}N$ HEMT structure showing the detailed configurations of epilayers used in this study. The inset (b) shows the STEM image of the top interfaces with $Al_xGa_{1-x}N$ barrier and thin GaN cap. (c) The STEM image of the full $In_xAl_{1-x}N$ HEMT structure showing the detailed configurations of epilayers used in this study. The inset (d) shows the STEM image of the top interfaces with $In_xAl_{1-x}N$ barrier.

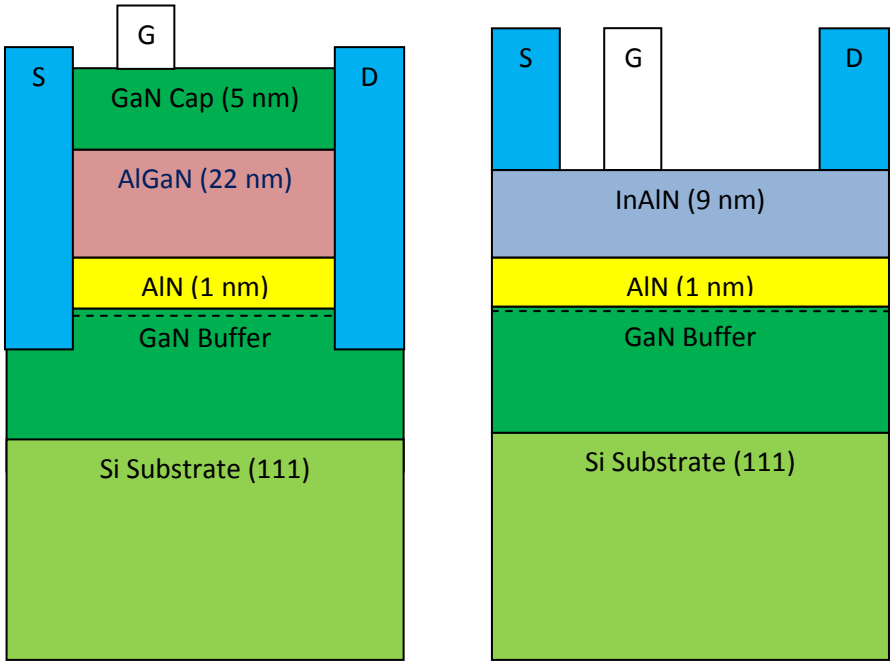

Figure 6.2 Schematics showing the cross section of AlGaN/GaN HEMTs (left) and InAlN/GaN HEMTs (right). The Source and Drain contacts (S & D symbols) of both HEMTs are Ti/Al/Ni/W with the same thickness (25/200/40/50 nm). AlGaN/GaN has ~ 50 nm recess etched Ohmic contact while InAlN/GaN has non recess etched Ohmic contact. The gate contact (G symbol) of both HEMTs is 100 nm thick RuO_x.

The micro-PL and micro-Raman measurements were carried out in a JY LABRAM-HR system equipped with a CCD detector based acquisition. The line scan mapping was done using a scanning stage capable of 0.1 µm step movement. The scattered light was collected in a back-scattering geometry through the long-working distance high numerical objective lens. The 488 nm line excitation in visible Raman mode allows well-resolved spectra recorded at 200 nm spacing where the substrate heating effect by the laser beam is negligible, as the excitation power during Raman sub-band gap excitation is kept very low. The line scan started from the source end to the gate and stopped at the drain end as no detectable Raman signal from GaN appeared in

source-drain contacts. The optical probe clearly detects Raman spectra of GaN under the gate contact. Similar line scans were performed on the regions of the device with a 325 nm excitation for the recording of PL spectra from GaN. The excitation power during the UV PL was kept very low (<1.0 μW) on the sample surface using neutral density filter settings in the spectrometer. The surface temperature rise was minimized with low power UV laser excitation when devices were not biased, and confirmed from the temperature calibration of peak shifts with high spectral resolution PL measurements. However, when HEMTs were electrically biased, they behaved like UV photodetectors under the 325 nm excitation wavelength, thus leading to a significant increase in photocurrents. Hence, the DC characteristics of transistors would change during PL probing when the surface was exposed to the laser beam and output power characteristics must be addressed in such experiments. For an accurate channel temperature profiling, we had carried out the temperature calibration on the HEMT device surface without any DC bias state by placing the diced samples inside a microscope-coupled heating-cooling OXFORD LN_2 cryostat. Both UV PL and Raman spectra were also recorded from the same regions of fabricated transistors at different temperatures. This type of calibration for spectral peak shifts takes care of any contact processing-induced hydrostatic uniaxial or biaxial stress variation at the GaN channel. After a proper calibration of peak shifts with respect to temperature, we analyzed the temperature in the devices under operation at different electrical bias voltages.

6.3 Results and Discussions

The temperature evolutions of the PL spectra from $Al_xGa_{1-x}N$/GaN and $In_xAl_{1-x}N$/GaN HEMT surfaces are addressed for a proper temperature calibration.

Figure 6.3(a) and Figure 6.3(b) show the PL spectra recorded from the $Al_xGa_{1-x}N$/GaN and $In_xAl_{1-x}N$/GaN HEMT structures without biasing state at source, drain and gate. The broader and intense band-edge free exciton emission of GaN peak is the dominant peak apart from the interference peaks observed at the lower energy side due to microscopic measurement on the GaN surface. The band-edge emission peak intensity decreases with increasing temperature while the spectral peak position is red-shifted from 3.44 eV at 150 K to 3.33 eV at 500 K. This red-shifted band-edge emission is due to the decrease of the band gap from the 2DEG GaN lattice with increasing sample temperature while a significant thermal broadening of the PL also appears at higher sample temperature. The increase in sample temperature enhances the electron-phonon interaction as a consequence the PL peak intensity reduces drastically due to the presence of defect sites at the top AlGaN/AlN/GaN 2DEG interfaces when compared to typical PL evolution from a strain-free GaN. In such a case of AlGaN/GaN heterostructure, it has been reported that the PL peak originates due to the recombination of electrons at the 2DEG and photo-excited holes at hetero-interfaces and the peak position is usually red-shifted compared to free excitonic emission of strain-free GaN[108, 109].The inset in Figure 6.3(a) shows the variation of experimentally observed PL peak as a function of sample temperature. The as-grown HEMT stack on 200 mm diameter Si(111) shows a concave wafer bowing <50 µm leading to a small component of starting residual in-plane tensile stress. The induced tensile stress thus modifies the electronic band gap structure at the 2DEG GaN as a result a significantly red-shifted PL band is recorded from the HEMT surface.

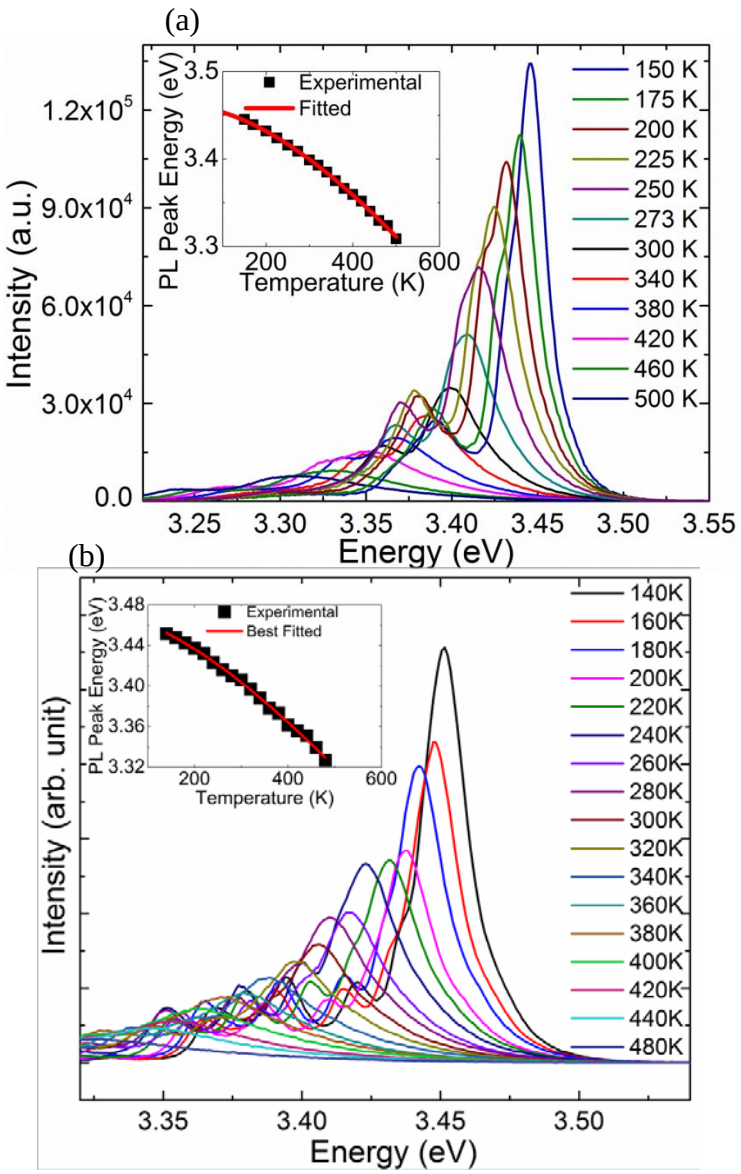

Figure 6.3 Micro-PL spectra of (a) AlGaN/GaN HEMT on Si substrate and (b)InAlN/GaN HEMT on Si substrate recorded at different temperatures from the device area used for optical temperature probing with 325 nm He-Cd laser line excitation. The inset shows the change in band edge PL peak energy as a function of sample temperature where the black square symbols represent the experimental results while the red line represents the best-fitted data using the Varshni's relationship shown in Equation (6.1).

Among various temperature-dependent band gap relationships of semiconductors, Varshni's equation is being extensively used to describe nonlinear temperature dependence of the band gap[110], and is given by the relation,

$$E(T) = E_{g0\text{-}2DEG} - \frac{\alpha T^2}{T + T_o} \quad (6.1)$$

where $E_{g0\text{-}2DEG}$ is the band gap of semiconductor at T=0 K; α is an empirical constant; and T_0 is associated with the Debye temperature. Above the Debye temperature range, the band-gap changes almost linearly with temperature rise due to linear changes of lattice constants and parameters related to electron-phonon interaction. The best fitting is obtained as shown as a solid line in the inset of Figure 6.3 and for the particular AlGaN/GaN HEMT interface configuration that takes into account a modified electronic structure of 2DEG GaN, the extracted values of $E_{g0\text{-}2DEG}$, α, and T_0 are 3.461 eV, 9.57×10^{-4} eV/K, and 1091 K, respectively. For InAlN/GaN HEMT interface configuration, the extracted values of $E_{g0\text{-}2DEG}$, α, and T_0 are 3.47 eV, 0.638 meV/K, and 566.2 K, respectively. The fitted $E_{g0\text{-}2DEG}$ values are thus sample specific which take into account the PL peak red shift related to the tensile strained interface and such a calibration does not overestimate channel temperatures at higher drain bias voltages. Using this type of sample specific calibration, the Varshni's relationship in Eq.(6.1) has been used to extract the channel temperature profiles using UV PL mapping technique for devices biased under high drain voltage ON-state operation. This type of sample specific measurements and calibration provide more accuracy when UV optical spectroscopy techniques are employed.

In order to compare the channel temperature profiles from UV PL calibration and the temperature from the entire epitaxial stack with information from Si substrate, micro-Raman experiments were performed on the same device area of these $Al_xGa_{1-x}N$/GaN HEMTs. The Raman spectra recorded from the

HEMT surface at different temperatures are shown in Figure 6.4. The spectra show four dominant peaks, such as optical phonon peak of Si substrate, E_2-highphonon from GaN, E_2-highphonon from thick AlN nucleation layer and A_1(LO) phonon from the GaN buffer. The insets of Figure 6.4 show the Raman peak shifts versus temperature plots for optical phonons of Si and E_2-high of GaN buffer. With an increase in sample temperature, all the peaks show phonon softening as expected in the visible Raman excitation. Apart from thermal expansion of lattice, there are several theories of temperature dependent phonon frequencies in semiconductors [111, 112] in first-order scattering related to phonon–phonon interactions up to the fourth order.

The experimental temperature-dependent E_2-high optical phonon peaks from HEMT stack are fitted using the relationship [113],

$$\omega(T) = \omega_0 - \frac{A}{e^{\frac{Bhc}{k_B T}} - 1} \tag{6.2}$$

where ω_0 is the phonon frequency at 0 K; T is the absolute temperature in K and A, B, are the fitting parameters, while h, c, and k_B are the Planck's constant, the speed of light in vacuum, and the Boltzmann's constant, respectively. The parameters, ω_0, A and B, for the case of Si substrate in AlGaN/GaN HEMT are 524 cm^{-1}, 8.58 $cm^{-1}$and 0.537, respectively while ω_0, A and B for the case of GaN buffer with in-plane tensile stress are 568 cm^{-1}, 4.74 cm^{-1}, and 0.538, respectively. The parameters, ω_0, A and B, for the case of Si substrate in InAlN/GaN HEMT are 523 cm^{-1}, 13.8 cm^{-1} and 0.761, respectively while ω_0, A and B for the case of GaN buffer in InAlN/GaN with in-plane tensile stress are 567 cm^{-1}, 18.1 cm^{-1}, and 1.33 respectively. The solid lines in the temperature zone of interests show the temperature calibration

fitting. The fitting parameters are then used to the extract temperature when the devices are in operation at a high drain bias ON-states.

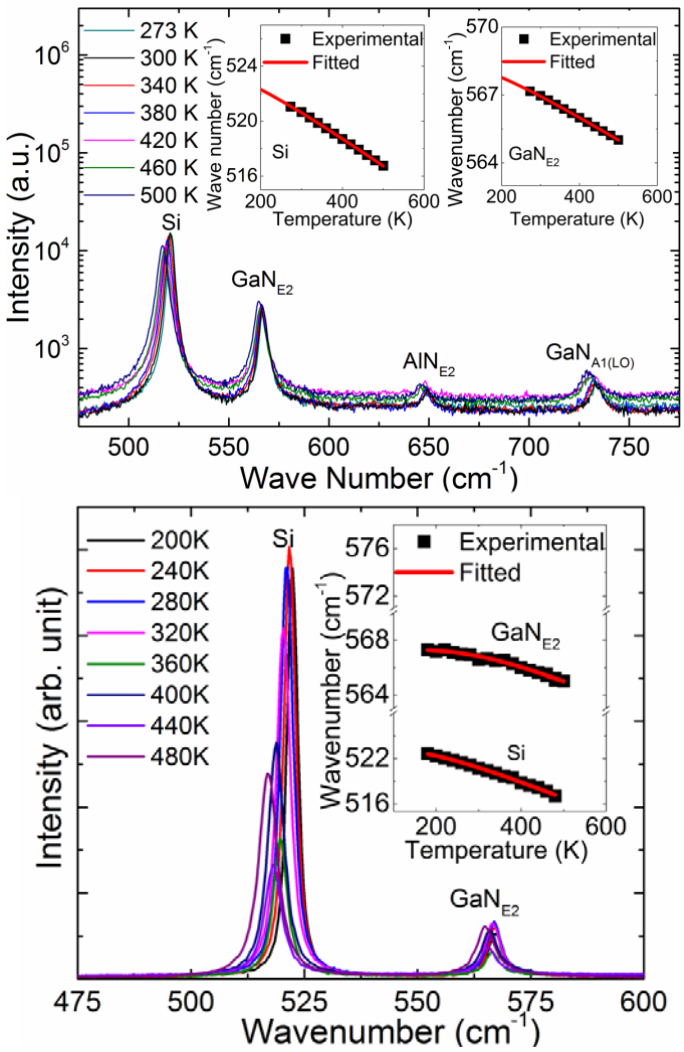

Figure 6.4 Micro-Raman spectra of (a) AlGaN/GaN HEMT and (b) InAlN/GaN HEMT on Si substrate at different temperatures with 488 nm Ar-ion laser line excitation. The insets show phonon peak shifts at different sample temperature for optical phonon of Si, and E_2-high of GaN. The black square symbols are the experimental results while the red lines are the fitted data using the phonon peak shifts and temperature relationship in Equation (6.2).

Figure 6.5(a) shows the I_D-V_{DS} characteristic of AlGaN/GaN HEMTs under visible light illumination and UV illumination. For AlGaN/GaN HEMTs under visible light illumination, $R_{on(VIS)}$ and $I_{D(SAT)(VIS)}$ at V_{GS}= 1.5 V are ~ 11.82

Ω.mm and 368.8 mA/mm, respectively. However, with UV PL illumination, there is 16% decrease in R_{on} and 35% increase in $I_{D(SAT)}$ due to the possible contribution from the photocarrier generation effect thus reducing the resistance of the 2DEG channel. Huang *et al*.[114]have reported that photocarrier generation occurs at the AlGaN surface, interface regions between AlGaN/GaN and deeper GaN buffer upon UV excitation. Thus, such 2DEG HEMT here also offers a possible candidate for UV photodetector. In PL mode device operation, the photocarrier generation is mainly observed at 2DEG GaN region and this effect results in a higher drain current and transconductance compared to our observations under visible light illumination.

Figure 6.5(b) shows the I_D-V_{DS} characteristics of InAlN/GaN HEMTs under visible light illumination and UV illumination. For InAlN/GaN HEMTs under visible light illumination, On resistance, $R_{on(VIS)}$, and drain saturation current $I_{D(SAT)(VIS)}$ at V_{DS} = 10 V and V_{GS} = 1.5 V are about 7.30Ω.mm and 0.575 A/mm, respectively. These result from a lower R_c (0.62 ± 0.08 versus 1.4 ± 0.2Ω.mm) and a higher gate to source capacitance due to a thinner barrier layer (~9 nm for InAlN versus 23 nm for AlGaN). Similar to AlGaN/GaN HEMTs, InAlN/GaN HEMTs under UV illumination also show a reduction in $R_{on(UV)}$(by ~12.7%) and an increase in $I_{D(SAT)(UV)}$ by (15.3%) at V_{GS} = 1.5 V and V_{DS} = 10 V. However, unlike AlGaN/GaN HEMTs, InAlN/GaN HEMTs under UV illumination could not pinch off easily due to the increase in I_D associated with both source and gate currents under UV illumination. The increase in source current is likely due to the photocarrier generation around 2DEG GaN channel while the increase in gate current could be resulted from the carrier

generations (electron-hole pairs) at the defect sites such as dislocation centers and sub-grain boundaries in the $In_xAl_{1-x}N$ barrier layer. This is not the band-to-band photocarrier generation since the $In_{0.17}Al_{0.83}N$ bandgap energy (~4.85 eV) is much higher than the excitation photon energy (3.82 eV). These photo-generated electrons at the channel then drifted along the electric field from gate to drain while the holes moved in opposite directions resulting in higher drain current under UV illumination.

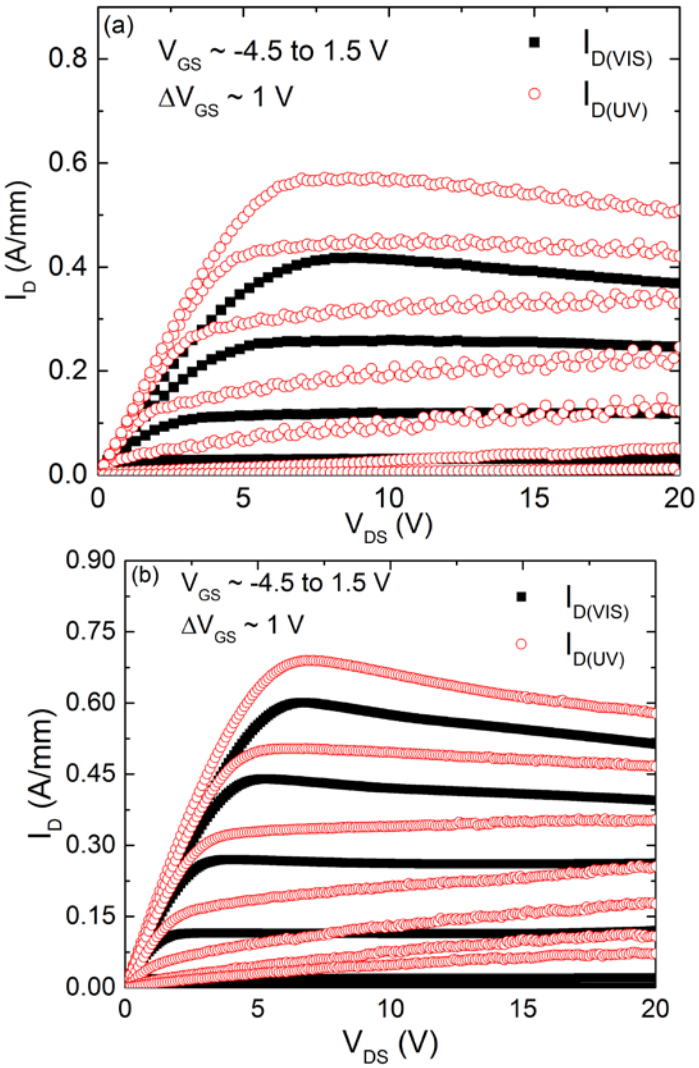

Figure 6.5 I_D-V_{DS} characteristics of (a) AlGaN/GaN HEMT and (b) InAlN/GaN HEMT under visible light illumination (solid symbols) and 325 nm UV PL illumination condition (hollow symbols).The dimensions of both HEMTs are as follows: L_{gd} ~ 9.5 µm; L_{gs} ~ 2 µm; L_g ~ 2.5 µm; and W_g = 2 × 50 µm.

On the other hand, Although dislocations defects are also observed in GaN/AlGaN barrier layer, in Fig. 6.1, it could be observed that GaN channel layer in AlGaN/GaN heterostructure has fewer dislocations than InAlN/GaN heterostructure. In addition, AlGaN/GaN has smoother surface than InAlN dislocation defects as shown in below Figure. As seen in below figures, the pits (black color) or dislocation defects are higher and bigger than AlGaN/GaN. Hence, the gate in AlGaN could still be in control of the channel in contrast to the gate in InAlN.

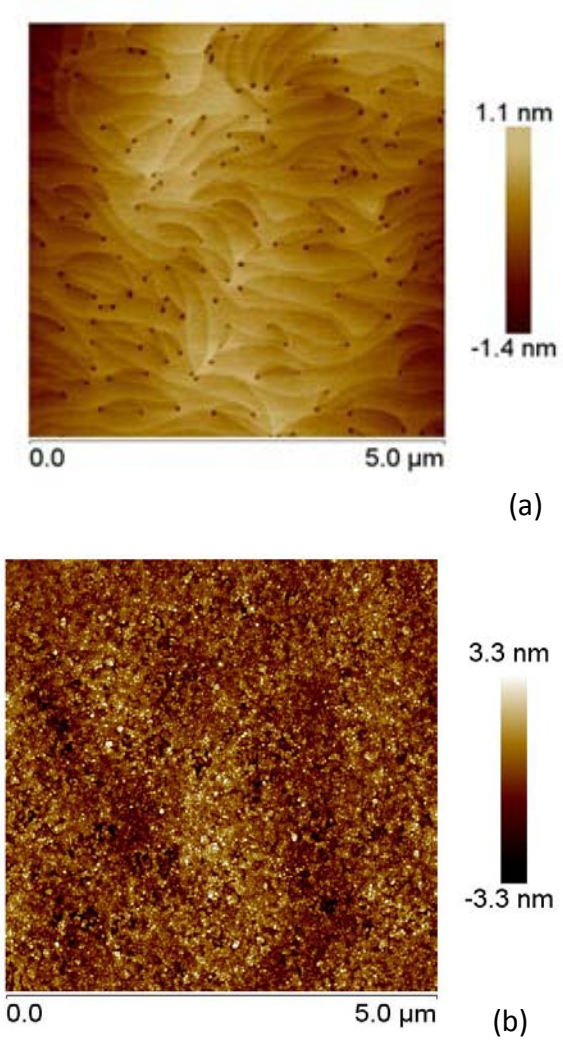

Figure 6.6 AFM images of (a) AlGaN/GaN and (b) InAlN/GaN heterostructure grown on 200 mm Si(111) substrates.

Figure 6.7 shows the 2DEG channel temperature profiles of AlGaN/GaN HEMTs and InAlN/GaN HEMTs grown on 200 mm diameter Si (111) under UV illumination and different biased conditions. Two sets of profiles for each HEMTs are shown here from the same device by probing nitride surface from source to drain contacts under different biasing conditions at V_{GS}= 1.5 V and V_{DS}= 15 and 20V. The channel temperature at 2DEG region is extracted using the Varshni's equation used for fitting band-edge PL peak at different temperatures as shown in Figure 6.3 for the calibration of UV PL data. For AlGaN/GaN HEMTs, the maximum temperature up to 435 K around the gate edge between gate and drain has been probed from such PL calibration. Due to the combined DC bias of V_{GS} and V_{DS}, the resultant electric field is highest at this gate edge which causes higher current crowding effect and as a consequence the temperature is maximum at this region for both V_{DS} =20 and 15 V while at fixed V_{GS} of 1.5V. The measured temperature gradually reduces along source/drain direction from the gate which indicates that the heat is well distributed radially outward from gate to source and drain regions. At lower V_{DS}, the temperature profile is lower due to a lower power handling of 8.1 W/mm in HEMT characteristics compared to power handling of ~10.2 W/mm at V_{DS}= 20 V. The maximum temperature obtain at gate edge region is about 395 – 400 K for V_{DS}= 15 V, which also indicates a substantial rise in channel temperature. For InAlN/GaN HEMTs, the maximum temperature is 475 K which is much higher than AlGaN/GaN HEMTs resulted from the higher power dissipation (11.58 W/mm Vs 10.2 W/mm). This maximum temperature also occurs around the gate edge, similar to AlGaN/GaN HEMTs.

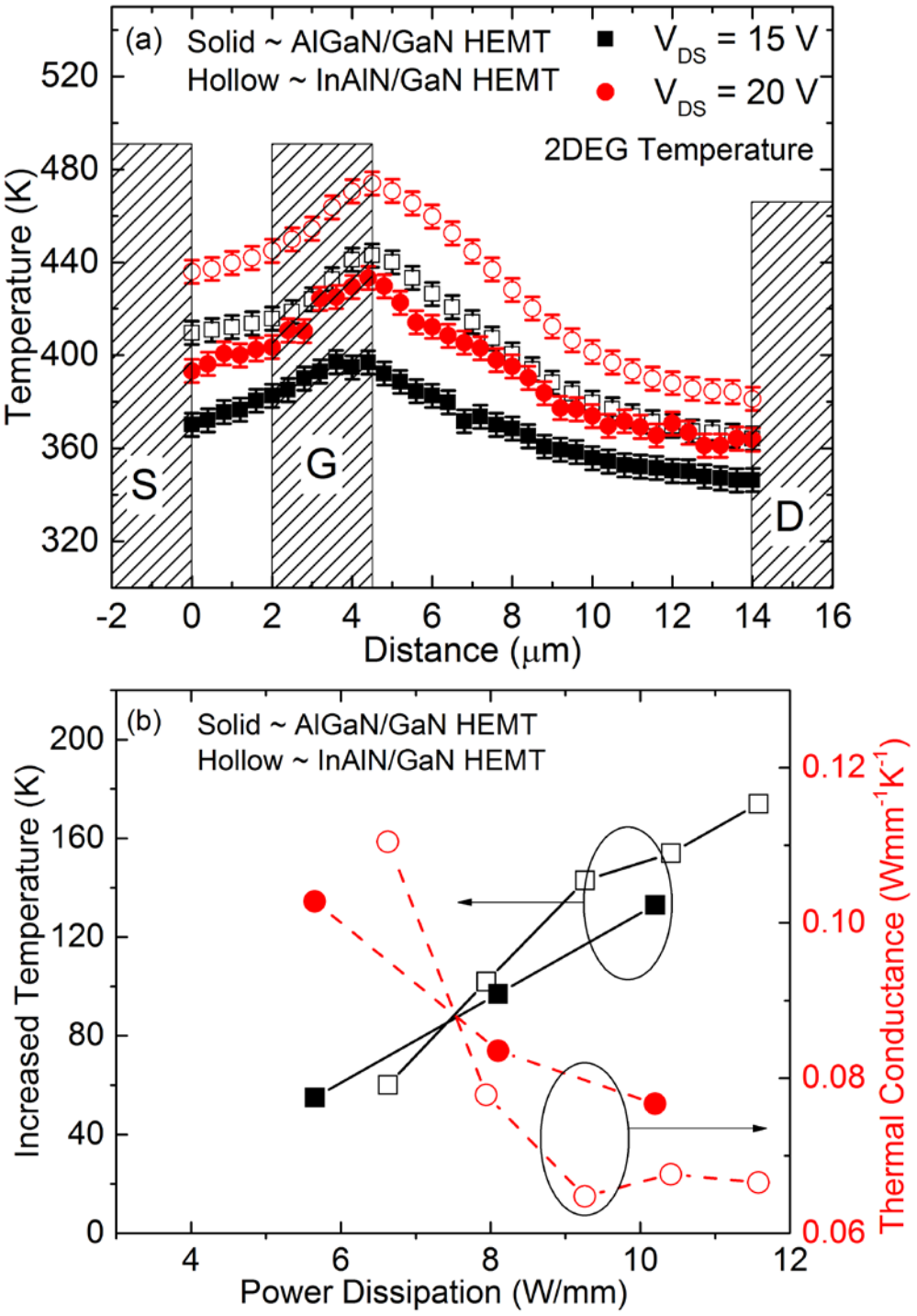

Figure 6.7 (a) The temperature profiles of 2DEG GaN channel region from 325 nm PL probing across source to drain regions of AlGaN/GaN HEMT and InAlN/GaN HEMT stack on 200 mm Si (111) at V_{DS} = 15 and 20 V. (b) Temperature rise (square symbols) at the gate edge region between gate and drain and thermal conductance (circle symbols) of AlGaN/GaN HEMT and InAlN/GaN HEMT as a function of DC power dissipation.

Minimum thermal conductance and maximum increased temperature of AlGaN/GaN HEMTs and InAlN/GaN HEMTs as a function of power dissipations are shown in Figure 6.7(b). The thermal conductivity of InAlN/GaN HEMTs tends to decrease sharply with increasing power dissipation and it is at its minimum (65.8 $Wm^{-1}K^{-1}$) when power dissipation > 9.26 W/mm. On the other hand, AlGaN/GaN HEMTs thermal conductivity also decreases with increasing power dissipation and its observed minimum value is 76.68 $Wm^{-1}K^{-1}$. At high power dissipation (~10.2 W/mm), AlGaN/GaN HEMT is thermally more conductive than InAlN/GaN HEMT (76.7 versus 67.6 $Wm^{-1}K^{-1}$). This could possibly be resulted from better growth quality (less dislocation and defects) in AlGaN/GaN HEMT compared to InAlN/GaN HEMT since there is a high possibility of heat trapping at the defect sites as observed in Figure 6.1 and Figure 6.6. The thermal conductance of our InAlN/GaN HEMT-on-Si(111) is much higher than the case of InAlN/GaN HEMT grown on sapphire [60](~28.0 $Wm^{-1}K^{-1}$) at similar power dissipation levels. This indicates that the Si substrate offers better heat dissipation compared to sapphire substrate. Therefore, simple back-end Si-substrate based thermal management solutions for such HEMTs may be cost effective.

The simultaneously measured temperature profiles in the whole AlGaN/GaN HEMT stack are then addressed by optical phonon peak shifts under 488 nm Raman excitations. Figure 6.8(a) also shows the visible Raman probe of temperature profiles from the HEMT stack and related temperature rise at the AlN/Si substrate. The power dissipation of HEMT is reduced at the same bias of V_{DS} = 15 V and 20 V compared to UV PL probing when measuring the

average GaN bulk temperature extracted from visible Raman scattering. With increasing V_{DS} from 15 to 20 V, the power dissipations of HEMTs increase from 5.85 W/mm to 7.38 W/mm and the highest temperature is probed at the area underneath the RuO_x gate contact and the drain region has the lowest temperature. The heat generated at the 2DEG interfaces dissipated vertically through the GaN buffer layer to the three-step graded AlGaN layers and thick AlN nucleation layer, and finally to the Si substrate. The Raman analysis shows temperature rise up to 350 – 370 K at the gate edges at different bias voltages. Due to the presence of a high density of dislocations and point defect complexes in these epitaxial AlGaN step-graded layers and AlN nucleation layers, there is high possibility of heat trapping at the defect sites. The scattering effects at the point defect complexes could be significant at AlN sites[115] when large diameter Si substrate is used in our case and therefore, despite a higher thermal conductivity offered by AlN-based layers, the crystalline quality of the nitride layers influences the channel temperature when devices are under operation at high power.

Figure 6.8(a) also shows the temperature profiles probed by visible Raman excitation at the AlN/Si interface where a comparatively lower temperature from Si is measured. This confirms the existence of *self-heating* in nitride stack at different power dissipation levels when HEMT device are under electrical stimulation. The relative temperature calibration from optical phonon shifts of Si substrate is thus useful to understand the contribution of different types of buffer layers to effective dissipation of heat generated at channel regions. Due to usage of a semi-transparent RuO_x gate, the temperature of the Si substrate beneath gate area is accurately measured using

visible laser Raman excitation. The temperature at the Si substrate thus changes insignificantly (~340 K) across the distance from the source to drain region of AlGaN/GaN HEMTs. We have also seen here that the temperature probed at AlN/Si interface from Si substrate is slightly higher (~340 K) compared to temperature of GaN buffer(~310 K) near the drain region. Since in this HEMT architecture, the distance from GaN channel to Si substrate is nearer than that from RuO_x gate area to drain contact area (4.3 μm vs 9.5 μm), the vertical heat dissipation is higher than lateral heat dissipation in the GaN buffer layer in this case when no passivation layers are used for the etched mesa structures. Another possible reason of lower temperature at GaN buffer near drain region in AlGaN/GaN HEMTs is that the recessed source and drain Ohmic contacts touch the 2DEG. This recess etch helps heat dissipate from the channel through the drain Ohmic metals in AlGaN/GaN HEMTs resulting in lowering the temperature around the drain region. This affect is not seen in InAlN/GaN HEMTs temperature profile shown in Figure 6.8(b).

Figure 6.8(b) shows the temperature profile of GaN buffer and AlN/Si interface in InAlN/GaN HEMTs. Unlike AlGaN/GaN HEMTs, the temperatures at GaN buffer from source to drain region changes insignificantly (~360 K). Hence, this supports the possible cause of recess etch which lowered the temperature at GaN buffer near the drain region in AlGaN/GaN HEMT. Similar to AlGaN/GaN HEMTs, AlN/Si interface has temperature of ~340 K from source to drain region. From these observations, it is clear that the *self-heating* in such GaN devices is also dependent on types of buffers, substrates and HEMT design.

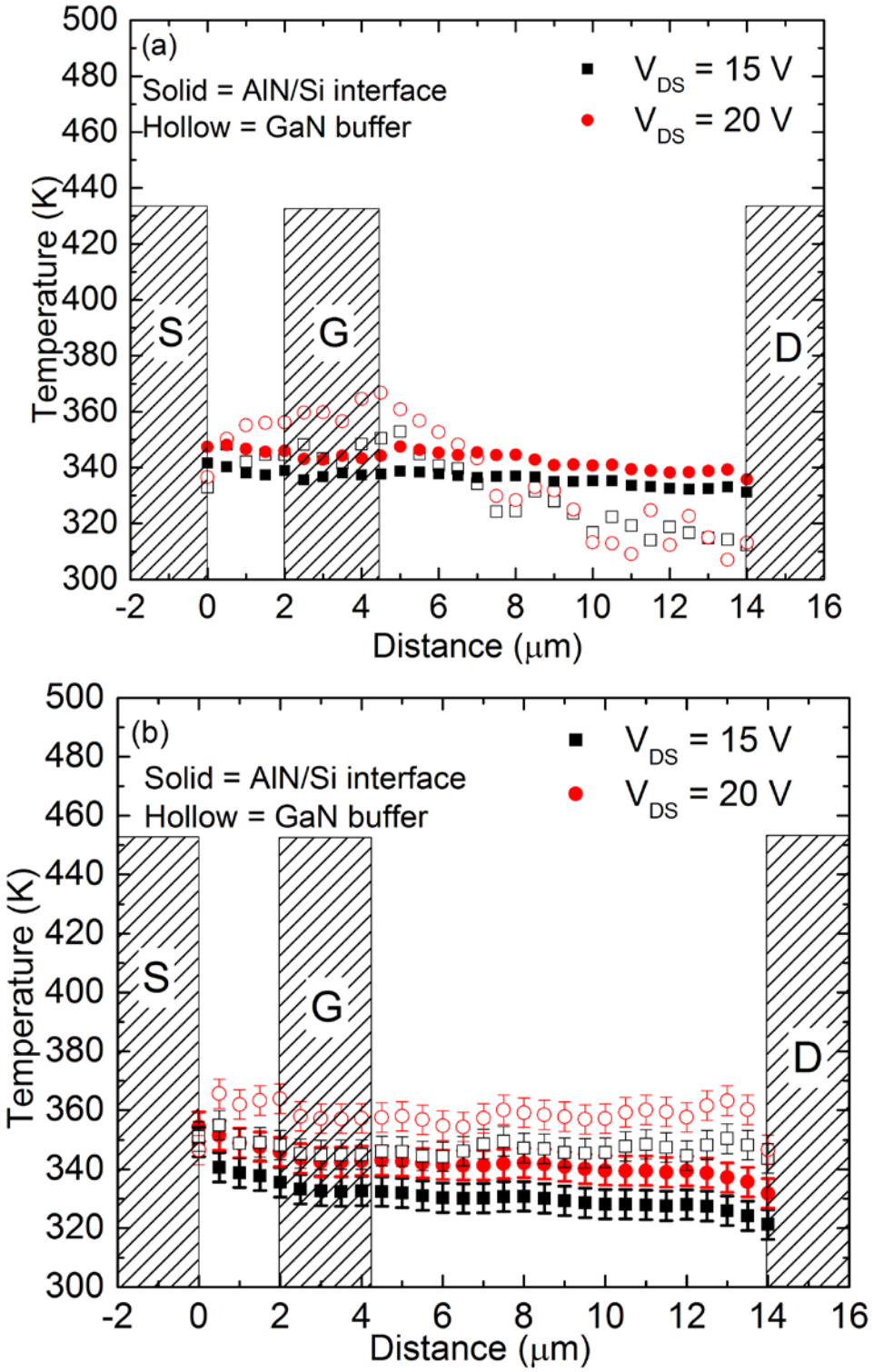

Figure 6.8 The average temperature profiles of GaN buffer layer and AlN/Si(111) interface measured between source and drain on the same (a) AlGaN/GaN HEMT and (b) InAlN/GaN HEMT device on Si by using optical phonon shift of Si and E_2-high phonon peak shift of GaN from 488 nm Raman excitation

6.4 Conclusion

Using RuO_x based Schottky contact as a gate electrode and non-destructive optical spectroscopic techniques, we have investigated the channel temperature profiles from source to drain region including the region underneath the gate in AlGaN/GaN HEMT and InAlN/GaN HEMT grown on a 200mm diameter Si substrate. Due to UV excitation, the photogenerated carriers are formed resulting in higher drain current in both InAlN/GaN HEMT and AlGaN/GaN HEMTs. InAlN/GaN HEMTs have higher drain current and higher power dissipation at the same bias voltage compared to AlGaN/GaN HEMTs under both UV illumination and visible illumination. Hence, InAlN/GaN HEMTs has higher maximum temperature (475 K Vs 433 K) compared to AlGaN/GaN HEMTs. Both maximum temperatures occurred around the gate edge between gate and drain region. With better growth quality heterostructure and recessed Ohmic contacts in AlGaN/GaN HEMTs, they have higher thermal conductivity (76.6 versus 67.6 $Wm^{-1}K^{-1}$) compared to InAlN/GaN HEMTs at the same power dissipation (~10.2 W/mm). In addition, we have demonstrated that HEMTs grown on Si(111) has higher thermal conductivity than HEMTs grown on sapphire.

Chapter 7: Effects of annealing pressure and ambient on thermally robust RuO_x Schottky Contacts on InAlN/AlN/GaN-on-Si(111) Heterostructure

7.1 Introduction

In our previous chapters, we have shown that RuO_x Schottky contacts have good potential as the anode and gate electrode in III-nitride high power diodes and HEMTs, respectively, owing to their low leakage current and good thermal stability[116]. We have also found that the electrical characteristics of RuO_x Schottky contacts depend on the annealing ambient and/or pressure, namely RuO_x Schottky diodes annealed in N_2 exhibit better thermal stability and lower leakage current compared to those annealed in vacuum. This is believed to be related to the oxidation of RuO_x to RuO_2 in N_2 annealing and the reduction of RuO_x to Ru in vacuum annealing as reported earlier in Chapter 4. Between N_2 and vacuum annealing, there are differences of pressure and ambient. Hence, it is not clear if the formation of RuO_2 or the reduction to Ru from RuO_x is related to the annealing pressure or ambient, or both. This motivates us to investigate the effects of annealing pressure and ambient on the electrical and material characteristics of RuO_x Schottky diodes by conducting annealing in vacuum, N_2 and Ar, with annealing in N_2 and Ar performed at the same pressure. Annealing in Ar would have an ambient similar to vacuum as Ar is an inert or noble gas.

In this Chapter, we investigate the effects of annealing pressure and ambient not only on the electrical characteristics of RuO_x based Schottky diodes, but also the material characteristic changes.

7.2 Experimental Procedures

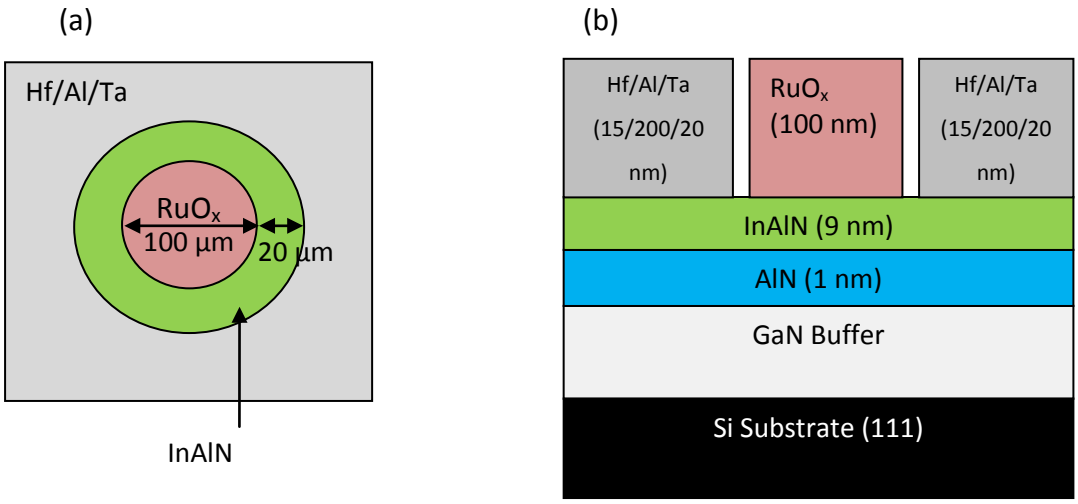

Figure 7.1 Schematic (a) top view and (b) cross sectional view of Schottky diodes with RuO_x (100 nm) as the anode and Hf/Al/Ta(15/200/20 nm) as the cathode.

Circular RuO_x Schottky diodes, as shown in Figure 7.1, were fabricated on $In_{0.17}Al_{0.83}N$/AlN/GaN on Si (111) substrate with a sheet resistance of 490 Ω/□. Device fabrication process began with cathode contact patterning on InAlN/AlN/GaN heterostructure. The cathode contacts, Hf/Al/Ta (15/200/20 nm), were then sputter-deposited in Ar plasma. The contacts were formed by the lift-off process and followed by annealing at 600 ^{o}C in vacuum for 1 minute to decrease the contact resistance. After anode contact patterning, RuO_x (100 nm) was sputter-deposited in Ar with 20 sccm flow rate and O_2 with 10 sccm flow rate. The substrates were not heated during RuO_x deposition. The anode contacts were also formed by means of the lift-off process, and were annealed under different pressures and ambients (in vacuum at a pressure of 6.67×10^{-3} Pa, in N_2 and Ar at the same pressure of 101.3 kPa)

at the temperature of 800 ^{o}C for 1 minute to study their effects on the electrical and material characteristics of RuO_x Schottky contacts.

7.3 Results and Discussions

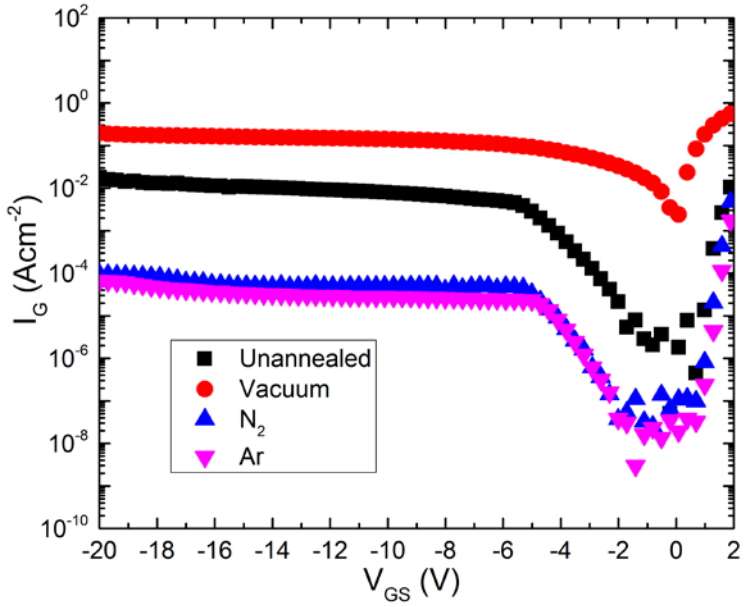

Figure 7.2 Typical *I-V* characteristics of RuO_x Schottky diodes under different annealing conditions.

The log scaled *I-V* characteristics of RuO_x Schottky diodes with different annealing conditions are shown in Figure 7.2. RuO_x Schottky diodes without annealing have a reverse leakage current of ~18.0 ± 2.1 mAcm^{-2} at the bias voltage of -20 V. With vacuum annealing at the pressure of 6.67 × 10^{-3} Pa, the reverse leakage current increases by one order of magnitude. In contrast, the reverse leakage current of RuO_x Schottky diodes annealed in either N_2 or Ar at the same pressure (~101.3 kPa) decreases by 2 orders of magnitude compared to that of RuO_x Schottky diodes without annealing. Therefore, from the *I-V*

characteristics of Schottky diodes, the lowest leakage current would be achieved with annealing in either N_2 or Ar, rather than in vacuum.

The Schottky Barrier Height (SBH) of RuO_x Schottky diode is extracted using its *I-V* characteristic. Since this contact system would be used as the gate in HEMTs, the effective SBH given by the *I-V* method would be more appropriate than that measured by means of the *C-V* or photocurrent method. The SBH is calculated using the thermionic emission equation:

$$I_D = AA^*T^2 e^{\left(\frac{-q\Phi_B}{kT}\right)} e^{\left(\frac{qV_D}{nkT}\right)} (1-e^{-\frac{qV_D}{kT}}) \quad [1]$$

where A is the area of the Schottky contact, A^* is the Richardson's constant and is 55.86 $Acm^{-2}K^{-2}$ for undoped InAlN [42], I_D is the current flowing through the diode, T is the absolute temperature, q is the electron charge, Φ_B is SBH, n is the ideality factor, k is the Boltzmann's constant and V_D is the applied voltage across the Schottky diode.

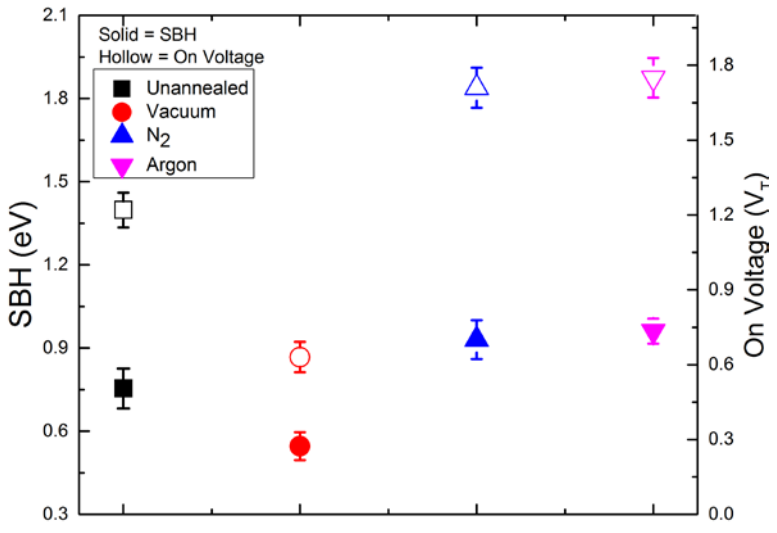

Figure 7.3 The extracted SBHs (Solid Symbol) and On Voltages (Hollow Symbol) of RuO_x Schottky diodes under different annealing conditions. The annealing temperature and duration are 800°C and 1 minute, respectively.

The extracted SBHs and On Voltages of RuO_x Schottky diodes under different annealing conditions are shown in Figure 7.3. The On Voltage is the minimum diode forward biased voltage for substantial current flow and is extracted from the linear extrapolation of the *I-V* characteristic in the linear region of the diode to the voltage axis. The effects of annealing ambient and pressure on SBH and leakage current at V_{DS} = - 20 V of RuO_x Schottky diodes are summarised inTable 7.1. The RuO_x Schottky diodes without annealing exhibit SBH of 0.754 ± 0.072 eV and On Voltage of 1.22 ± 0.07 V. The SBH and On Voltage reduce to 0.546 ± 0.050 eV and 0.631 ± 0.061 V, respectively with vacuum annealing at the pressure of 6.67×10^{-3} Pa. These reductions in SBH and On Voltage correlate well with the increase in reverse leakage current of these diodes, as shown in Figure 7.2 and Table 7.1. On the other hand, RuO_x Schottky diodes annealed in N_2 with the pressure of 101.3 kPa have SBH of 0.931 ± 0.070 eV and On Voltage of 1.71 ± 0.08 V. Similar SBH and On Voltage are observed for RuO_x Schottky diodes annealed in Ar with the same pressure of 101.3 kPa as N_2 annealing. Again, the increase in SBH and On Voltage of RuO_x Schottky diodes annealed in either Ar or N_2 corroborate well with the decrease in reverse leakage current of these diodes (see Figure 7.2 and Table 7.1).

As shown in Figure 7.2 and Figure 7.3, annealing in vacuum with the pressure of 6.67×10^{-3} Pa decreases the SBH and increases the leakage current, while annealing in Ar with the pressure of 101.3 kPa increases the SBH and decreases the leakage current. Since Ar is a noble gas, these changes in electrical characteristic of Schottky diodes are likely to be resulted from the change in pressure rather than ambient. In addition, annealing in N_2 yields

similar electrical characteristics as annealing in Ar, and this highlights that N_2 does not react with RuO_x at 800^oC and the annealing pressure plays a more critical role for the changes in RuO_x Schottky diodes electrical characteristics rather than ambient. To substantiate this, we conduct X-ray Diffraction (XRD) and Secondary Ion Mass Spectrometry (SIMS) characterisations of our samples.

Table 7.1 Leakage current @ -20 V and SBH of RuO_x Schottky diodes under different conditions. The annealing duration is 1 minute.

Annealing Ambient	Annealing Temp (^oC)	Annealing Pressure (Pa)	Leakage Current @ -20V (Acm^{-2})	SBH (eV)
Unannealed	-	-	~1.79×10^{-2}	0.754±0.072
Vacuum	800	~6.67×10^{-3}	~1.98×10^{-1}	0.546±0.050
N_2	800	~1.013×10^{5}	~9.37×10^{-5}	0.931±0.070
Ar	800	~1.013×10^{5}	~6.68×10^{-5}	0.961±0.045

XRD spectra of RuO_x Schottky diodes under different annealing conditions are shown in Figure 7.4. Unannealed RuO_x Schottky contacts are amorphous nature. With annealing in vacuum at the pressure of 6.67×10^{-3} Pa and at the temperature of 800^oC, 4 XRD peaks at 2θ of 38.6^o, 42.3^o, 44.2^o, and 58.7^o are observed, as shown in Figure 7.4. These peaks correspond to Ru crystal planes of Ru(100), Ru(002), Ru(101) and Ru(102), respectively. Hence, it can be deduced that polycrystalline Ru metal is formed with vacuum annealing, owing possibly to the dissociation of Ru and O bond in RuO_x. This agrees well with the relationship between the dissociation pressure and temperature of

RuO_2 bond proposed by Brunetti *et al.*[117]. Since the dissociation pressure of RuO_2 bond at 800°C is ~0.255 Pa, which is much higher (~40 times) than the pressure of our vacuum annealing, RuO_x reduces to Ru.

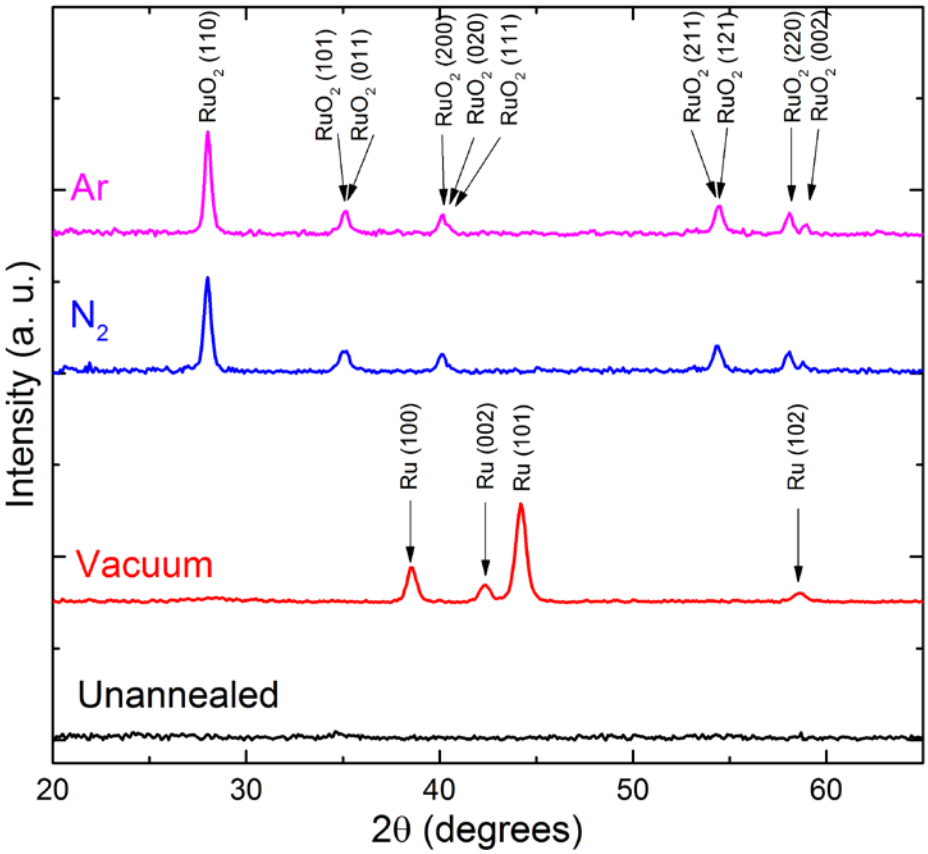

Figure 7.4 XRD spectra of RuO_x Schottky diodes under different annealing conditions. (unannealed ~ Black, annealed in vacuum ~ Red, in N_2 ~ Blue, and in Ar ~ Purple) at 800°C for 1 minute.

On the other hand, for RuO_x Schottky contacts annealed in N_2 at the pressure of 101.3 kPa, different RuO_2 crystal planes such as RuO_2 (110), RuO_2 (101), RuO_2 (011), and RuO_2 (200) are formed (see Figure 7.4). Similar XRD spectra are observed for RuO_x Schottky contacts annealed in Ar at the same pressure as in N_2. Therefore, it can be deduced that polycrystalline RuO_2 is formed when annealed in Ar and N_2. With Ar and N_2 annealing at the pressure of

101.3 kPa, which is more than 5 orders of magnitude higher than the dissociation pressure of RuO_2 bond, only polycrystalline RuO_2 are formed and no crystalline planes of Ru are observed.

Since RuO_2 has a higher workfunction than Ru (5.1 eV versus 4.7 eV), the formation of polycrystalline RuO_2 in RuO_x annealed in N_2 and Ar could be one of the reasons that leads to the increase in SBH and On Voltage, and decrease in leakage current. On the other hand, the formation of polycrystalline Ru metal in RuO_x annealed in vacuum could be one of the reasons for the decrease in SBH and On Voltage, and increase in leakage current.

In the SIMS profiles of unannealed RuO_x Schottky diodes, as shown in Figure 7.5(a), AlO is observed. This AlO could have resulted from interfacial oxides such as Al_2O_3 and/or InAlO, formed possibly during the Ru sputtering in Ar and O_2 plasma. AlO is also found in RuO_x annealed in vacuum, N_2 and Ar, as shown in Figure 7.5(b), (c) and (d), respectively. Therefore, the changes in leakage current, SBH and On Voltage observed in RuO_x Schottky diodes with annealing are not likely due to the formation of the interfacial oxide layer, instead more likely resulted from the formation of RuO_2 or the reduction to Ru from RuO_x, as discussed earlier. In addition, since the outdiffusions of Al, Ga, and In atoms are observed in all annealed samples (Ar, N_2 and vacuum), it maybe concluded that the outdiffusion is also not a factor that changes the leakage current, SBH and On Voltage of RuO_x Schottky diodes.

It is to be noted that the SIMS profiles of RuO_x annealed in Ar and N_2 are similar. The ratios of O to Ru counts in these two samples increase by ~24%

compared to unannealed RuO_x. This highlights that the oxygen content is increasing in RuO_x, hence resulting in the formation of polycrystalline RuO_2, as shown by the XRD spectra in Figure 7.4. On the other hand, the ratio of O to Ru counts decreases by 31% (0.127 Vs 0.185) in RuO_x annealed in vacuum compared to unannealed RuO_x. This indicates that oxygen might have diffused out from RuO_x during annealing in vacuum ambient. This also concurs with XRD spectra of RuO_x annealed in vacuum.

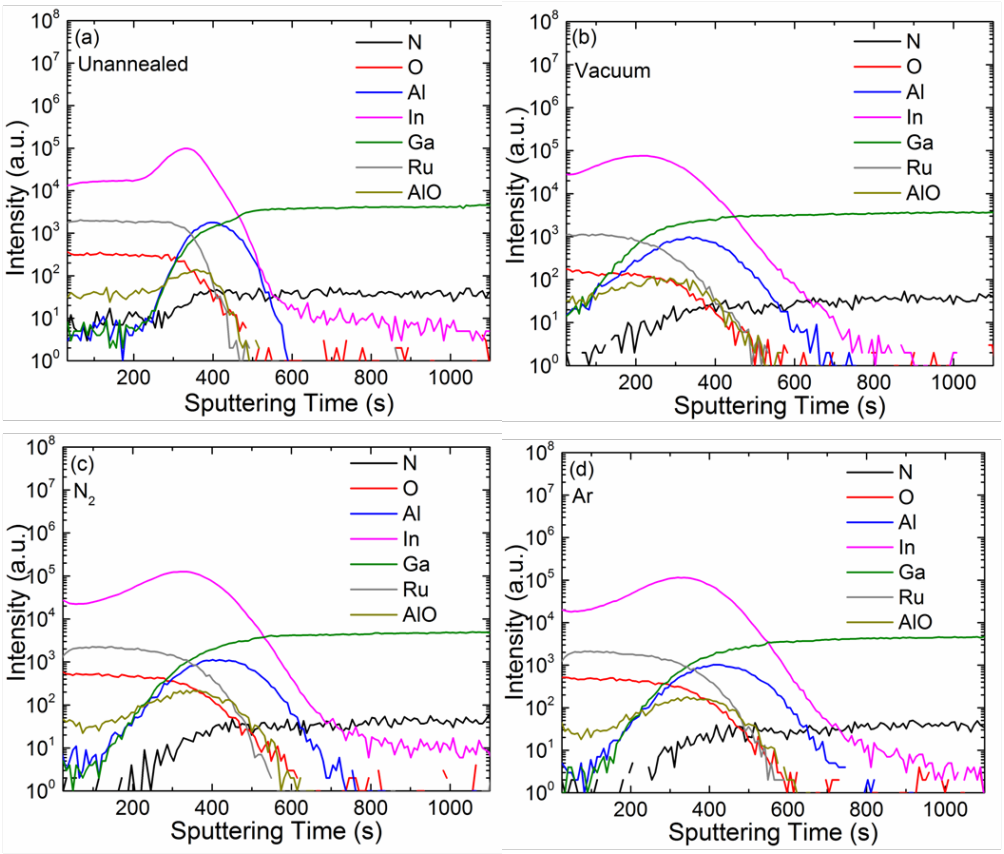

Figure 7.5 SIMS Profiles of RuO_x Schottky diodes under different annealing conditions: (a) Unannealed, (b) annealed in vacuum, (c) annealed in N_2, and (d) annealed in Ar. The annealing temperature and duration are 800^{o}C and 1 minute, respectively.

Figure 7.6 shows the HADDF-STEM images of RuO_x Schottky diodes under different annealing conditions: (a) unannealed, (b) annealed in vacuum, (c) annealed in N_2 and (d) annealed in Ar. First of all, we have observed the sharp InAlN and RuO_x interface and InAlN, AlN and GaN interface which mean there is no significant change to the interfaces due to heat treatment. It can also be observed in Figure 7.6(a) that unannealed RuO_x is amorphous in nature whereas annealed samples in Figure 7.6(b), (c) and (d)are polycrystalline. These support XRD data shown in Figure 7.4. There are dark areas near the interface in RuO_x Schottky contacts annealed in vacuum, N_2 and Ar possibly due to the polycrystalline formation from the amorphous after annealing. These dark areas are most likely the voids as EDS scans of these areas, as shown in Figure 7.6(e) for the vacuum annealed sample, have much less signal intensity than other areas. EDX scans of other samples (Ar, N_2 and unannealed) show similar features to those in Figure 7.6(e). We have also observed those voids in unannealed RuO_x but these voids are not near the interface between RuO_x and InAlN. Voids could decrease the contact surface of RuO_x to InAlN which could reduce the leakage current density. However, since voids are formed near the interface between RuO_x and InAlN in all 3 RuO_x Schottky diodes annealed in Ar, N_2 (101.3 kPa) and vacuum (6.67×10^{-3} Pa), the different annealing pressures and ambients do not significantly affect them; hence, these voids could not possibly have significant effect on the leakage current and SBH in RuO_x Schottky diodes.

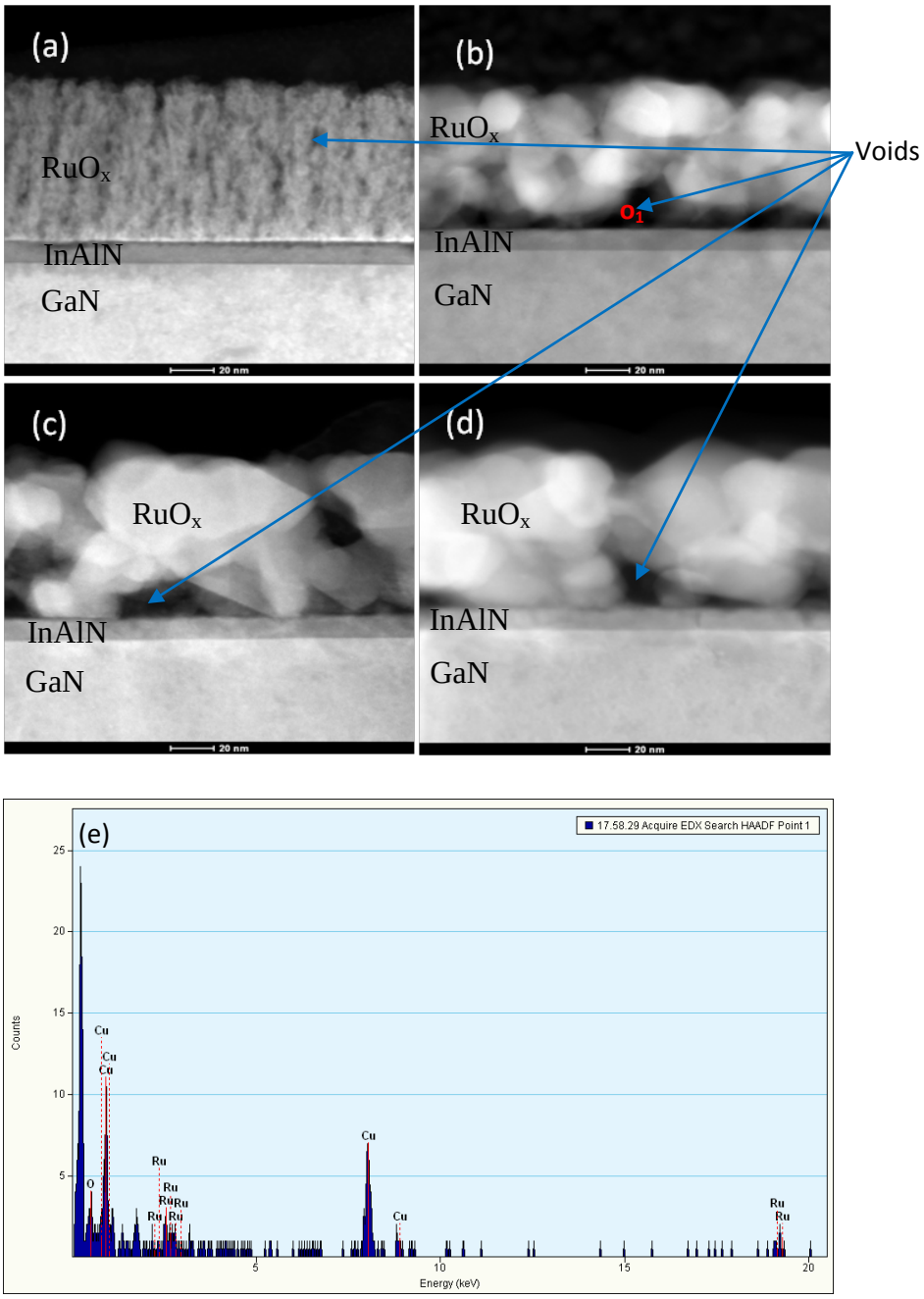

Figure 7.6 The HADDF-STEM images of RuO_x Schottky diodes under different annealing conditions: (a) unannealed, (b) annealed in vacuum, (c) annealed in N_2 and (d) annealed in Ar. The annealing temperature and duration are 800^{o}C and 1 minute, respectively. The magnification is 710k. (e) The spot EDX spectrum at O_1 (void) indicated in (b). Cu and C are observed due to contamination during TEM sample preparation. Similar EDX spectra of voids are observed in unannealed, N_2 annealed and Ar annealed samples.

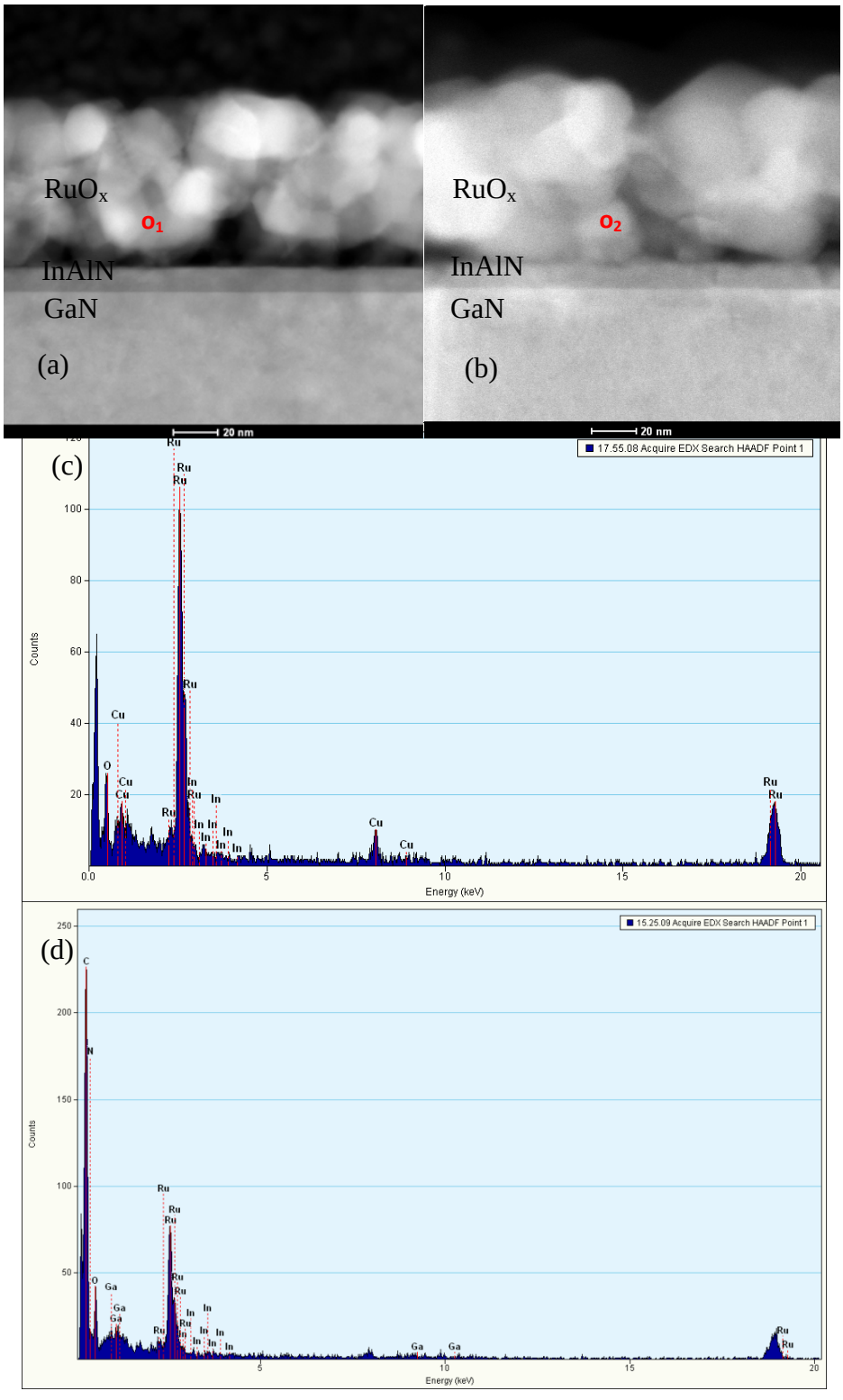

Figure 7.7 The HADDF-STEM images of RuO_x Schottky diodes (a) annealed in vacuum and (b) annealed in Ar. (c) The spot EDX spectrum at O_1 indicated in (a) and (d) The spot EDX spectrum at O_2 indicated in (b). Cu and C are observed due to contamination during TEM sample preparation.

Figure 7.7(c) and (d) show the point scan of EDX spectra of RuO_x annealed in vacuum and Ar respectively. RuO_x annealed in N_2 has similar data to that of RuO_x annealed in Ar. From these EDX spectra, it is seen that the ratio of Ru to O intensity is higher in RuO_x Schottky contact annealed in vacuum than in Ar. This could possibly indicate that RuO_x is converted to RuO_2 in Schottky contact annealed in Ar or N_2 while RuO_x is converted to Ru in Schottky contact annealed in vacuum. These results correlate with other material characterisation techniques such as XRD and SIMS. Therefore, the change in electrical characteristic of RuO_x Schottky contacts could likely be resulted from the change of oxygen content in RuO_x crystalline formation when they are annealed under different pressures (101.3 kPa Vs 6.67×10^{-3} Pa). We have also observed Ga peaks in both Ar and vacuum annealed samples as shown inFigure 7.7(c) and (d) although it is unlikely that Ga outdiffusion significantly affects the SBH and leakage current.

We have also studied the changes in surface morphology with different annealing ambients and pressures. Unannealed RuO_x has the smoothest surface with the average roughness (R_a) of 1.51 nm and the Root Mean Square roughness (R_q) of 2.05 nm, as shown in Figure 7.8. When annealed in vacuum at the pressure of 6.67×10^{-3} Pa, R_a and R_q increase to 2.38 nm and 2.94 nm, respectively. For annealing in either N_2 or Ar at the pressure of 101.3 kPa, the surface becomes rougher compared to unannealed RuO_x and those annealed in vacuum. The values of R_a and R_q for Ar annealed RuO_x are ~3.4 nm and ~4.46 nm respectively while those for N_2 annealed RuO_x are ~3.38 nm and 4.56 nm respectively; hence, N_2 and annealed RuO_x have similar surface. Therefore, it is possible to deduce that polycrystalline RuO_2 has a rougher surface

compared to polycrystalline Ru metal, which is consistent with the study done by Huang *et al*.[118]. In addition, we do not think that surface roughness is likely to be responsible for the changes in leakage current and SBH, since all annealed samples have rougher surface, to different extents, than unannealed samples.

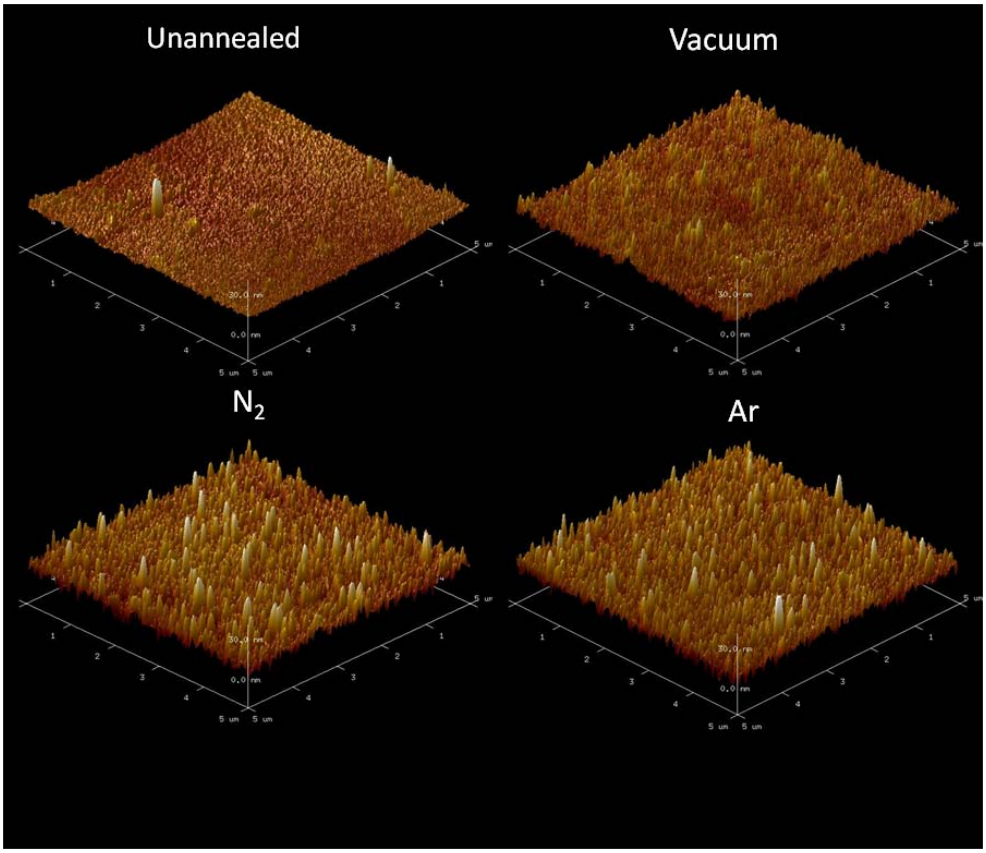

Figure 7.8 AFM images of RuO_x Schottky diodes under different annealing conditions. The sample surface area (x × y) is 5 μm × 5 μm. The minimum and maximum color scale for the z axis is -30 nm and 30 nm respectively.

7.4 Conclusion

In summary, we have investigated the effects of annealing ambient and pressure on the electrical and material characteristics of RuO_x on $In_{0.17}Al_{0.83}N$/AlN/GaN-on-Si(111)Schottky diodes. When RuO_x Schottky diodes are annealed in vacuum at the pressure of 6.67×10^{-3} Pa, SBH

decreases by 0.208 eV and the reverse leakage current increases by one order of magnitude with respect to unannealed diodes. These could possibly be caused by the dissociation of Ru and O bonds leading to the formation of Ru from RuO_x when annealed in vacuum at 800^oC owing to high vacuum (6.67×10^{-3} Pa). On the other hand, annealing in Ar at the pressure of 101.3 kPa, increases the SBH by 0.207 eV and decreases the reverse leakage current by about two orders of magnitude. These could possibly be resulted from the formation of RuO_2 in RuO_x Schottky diodes when annealed in Ar due to high temperature (800^oC) and high pressure (101.3 kPa) heat treatment. In addition, since the interfacial oxide is found in all samples including unannealed RuO_x, the changes in electrical and material characteristics are less likely due to the presence of interfacial oxide. The electrical and material characteristics of RuO_x Schottky diodes annealed in N_2 are similar to diodes annealed in Ar. Since Ar is an inert gas, it may be concluded that N_2 does not react with RuO_x or InAlN and that the annealing pressure is the reason for the changes in RuO_x Schottky diodes electrical and material characteristics.

Chapter 8: Single Contact Annealing Process for Both Gate-First and Gate-Last RuO_x Gate $In_xAl_{1-x}N$/GaN HEMTs

8.1 Introduction

Using thermally robust RuO_x as the gate contact (reported in earlier chapters), we propose a Single Contact Annealing Process (SCAP), where only one thermal annealing is performed for both the Schottky and Ohmic contacts after their deposition, for the fabrication of Schottky gate HEMTs. The Ohmic contact used is Hf/Al/Ta. In SCAP, the sequence of Ohmic and Schottky contact depositions can be interchanged (more details in the Experimental Procedures), thus making it possible for both the gate-first and gate-last processes. Therefore, it also provides flexibility in device processing. In this chapter, we report the fabrication and electrical characterizations of $In_{0.18}Al_{0.82}N$/GaN-on-Si HEMTs with RuO_x Schottky gate and Hf/Al/Ta Ohmic source/drain contacts fabricated by means of SCAP. In addition, comparable HEMTs with the same Schottky and Ohmic contacts were fabricated using the conventional gate-last process (CGLP) to serve as reference for comparison of device performance.

8.2 Experimental Procedures

RuO_x Schottky gate HEMTs were fabricated on diced samples from commercially available 100 mm diameter $In_{0.18}Al_{0.82}N$/GaN-on-Si(111) epi-wafer. The HEMT structure comprises an undoped 9 nm $In_{0.18}Al_{0.82}N$ barrier layer, 1 nm AlN spacer, and 1.3 μm GaN buffer on AlN/Si(111). The epi-wafer showed a sheet resistance of 354 Ω/ and an electron mobility of 943

$cm^2/V \cdot s$, as determined by Hall-measurements at room temperature. Two types of devices: Device A and Device B were fabricated using the process flows shown in Figure 8.1. Device A was made by means of the proposed SCAP, while Device B by the CGLP, where the gate contact is typically not given any annealing. The fabrication process for both Device A and Device B started with the isolation of active mesa region etched by the BCl_3-Cl_2 gas mixture in an Inductively Coupled Plasma (ICP) etcher. After the mesa isolation, the source and drain regions were patterned and Ohmic contact metals, Hf/Al/Ta (15/200/20 nm) were sputter-deposited. The contacts were subsequently defined by means of the lift-off process. Device B was then annealed at 600^oC in vacuum for 60 s (the optimized annealing conditions for Hf/Al/T [119]) to form good Ohmic contacts, whereas Device A was not given heat treatment at this stage. After the gate region patterning process, 100 nm RuO_x was sputter-deposited in a gas mixture of Ar and O_2. Lastly, Device A was annealed at 800^oC in N_2 ambient for 60 s. Unlike Device B, we could not use vacuum annealing condition for both Schottky and Ohmic contacts since we have reported in Chapter 7 that RuO_x Schottky contacts annealed in vacuum has the increased gate leakage current due to the Ru phase formation. On the other hand, RuO_x Schottky contacts annealed in N_2 is thermally stable up to 800^oC as reported in earlier chapters. In addition, we have also found that Hf/Al/Ta Ohmic contact annealed at 800^oC in N_2 has lower contact resistance (0.63 versus 1.3 Ωmm) than Hf/Al/Ta Ohmic contact annealed at 600^oC in N_2. Therefore, annealing at 800^oC in N_2 is a good compromised annealing condition for both Schottky and Ohmic contacts.

As seen in Figure 8.1, the patterning and deposition of source/drain and gate

contacts can be interchanged in the Device A process whereas Device B process does not offer such flexibility. The *I-V* and *C-V* characteristics of unpassivated HEMTs (both Device A and Device B) were measured using an Agilent B1500A Semiconductor Parameter Analyzer at room temperature. Both Device A and Device B have the following dimensions: gate length, L_G ~ 2.3 μm; source to drain distance, L_{SD} ~ 10 μm; gate to source distance, L_{GS} = 2 μm and gate width, W_G = 2 × 50 μm.

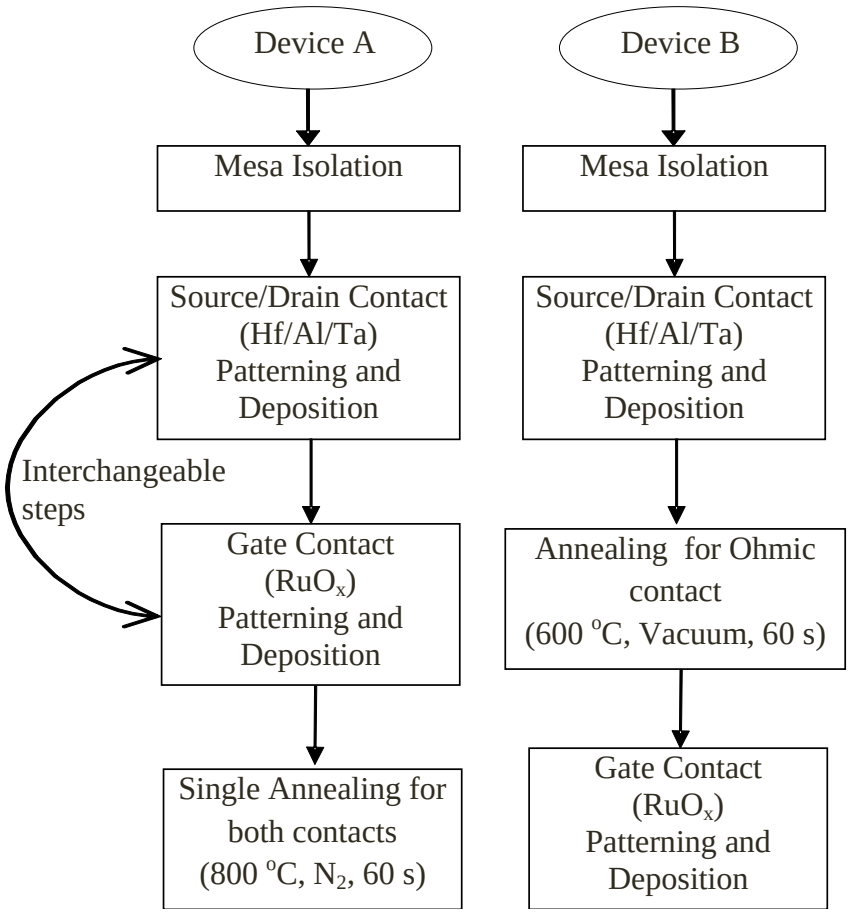

Figure 8.1 The Fabrication Process flows of Device A and Device B. Device A is made using the Single Contact Annealing Process (SCAP), while Device B using the conventional gate-last process.

8.3 Results and Discussions

Figure 8.2(a) shows the typical forward and reverse biased I_G-V_{GS} characteristics of Device A and Device B. The Schottky Barrier Height (*SBH*) and ideality factor of the gate contact were extracted using the thermionic emission current-voltage relationship. The extracted *SBH* of Device A and Device B are 1.14 and 0.97 eV, respectively. Despite having a higher *SBH*, Device A has approximately one order of magnitude higher gate leakage current compared to Device B. The lower leakage current in Device B could be resulted from the formation of a thicker oxide layer between the Schottky gate metal and $In_{0.18}Al_{0.82}N$ during Ohmic contact annealing. In addition, the extracted ideality factor *(n)* of Device A and Device B are 1.26 and 2.2, respectively. The higher value of *n* indicates that the electron transport mechanism between the gate contact metal and semiconductor in Device B is not dominated by the thermionic emission process, but contributed mainly by the thermionic field emission process. On the other hand, the current transport mechanism through the gate in Device A is predominated by the thermionic emission process since $n \sim 1.26$, close to 1. The discrepancy in transport mechanism points to modification of the metal-$In_{0.18}Al_{0.82}N$ interface in Device B, in comparison to Device A.

Furthermore, as shown in Figure 8.2(b), the gate capacitance (C_{GS})-V_{GS} characteristic of Device B shows that the accumulation capacitance ($C_{GS(ACC)}$) of Device B is ~0.621±0.057 μF/cm^2, which is ~ 12 % lower than that of Device A (~0.707±0.52 μF/cm^2). There is also a negative flat band voltage shift for Device B, with respect to Device A. One of the reasons for this is the 0.17 eV lower *SBH* in Device B. Moreover, the negative flat band voltage shift

for Device B indicates that the separation distance between the Schottky gate metal and the 2DEG channel is larger than in Device A. Since Device A also has a thin interfacial oxide layer (aluminium oxide) as shown in Figure 7.5 of Chapter 7, the lower $C_{GS(ACC)}$ and negative flat band voltage shift in Device B indicates the possibility of thicker oxide layer formation between RuO_x and $In_{0.18}Al_{0.82}N$.

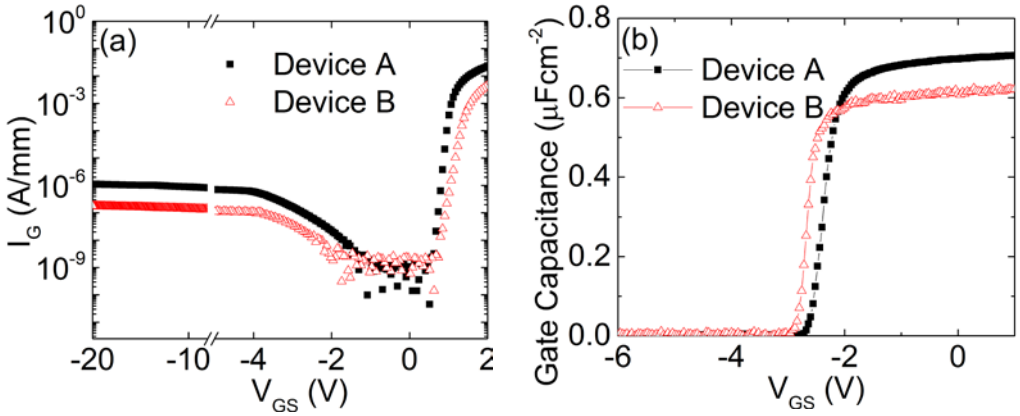

Figure 8.2 (a) I_G and (b) C_{GS} as a function of V_{GS} of Device A (black square) and Device B (red triangle).

Figure 8.3(a) depicts the $I_{D(LOG)}$ and transconductance (g_m) as a function of V_{GS} plots at V_{DS} = 10 V. With a lower gate leakage current in Device B of ~1.82×10^{-7} A/mm (see Figure 8.2(a)), the OFF current of Device B of ~2.02×10^{-7} A/mm is, as expected, smaller than that of Device A (~8.64×10^{-7} A/mm), There is a negative 0.4 V shift in the threshold voltage (V_{TH}) in Device B compared to Device A (-2.8 V versus -2.4 V). We also observe that the ON current (V_{GS} = 2 V and V_{DS} = 10 V) of Device A (~0.676 A/mm) is slightly smaller than that of Device B (~0.705 A/mm). This small difference is due to the discrepancy in the overdrive voltage ($V_{OVERDRIVE}$ = V_{GS} - V_{TH}).

Therefore, the ON-OFF current ratio of Device A is approximately one order of magnitude lower than that of Device B, and this is mainly due to the contribution of a higher gate leakage current in Device A. On the other hand, since Device A has higher $C_{GS(ACC)}$ compared to Device B, its maximum tranconductance, g_m is ~ 9.5% (0.195 versus 0.181 S/mm) more than that of Device B.

Figure 8.3(b) shows the I_D-V_{DS} characteristics of Device A and Device B at different $V_{OVERDRIVE}$. It can be seen that Device A has a higher drain saturation current ($I_{DS(SAT)}$) and lower ON resistance, R_{on}, compared to Device B. The values of $I_{DS(SAT)}$ of Device A and Device B are ~0.501 and ~0.458 A/mm, respectively at the same V_{DS} = 12 V and $V_{OVERDRIVE}$ = 3.4 V. The R_{on} of Device A and Device B are ~7.14±0.52 and ~7.66±0.47Ω.mm, respectively. The Ohmic contact resistance (R_c) and sheet resistance (R_{SH}), extracted from the Linear Transmission Line Model (LTLM) measurements, of Device A are ~0.63±0.33 Ω.mm and ~418±29 Ω/□, respectively, and those of Device B are ~0.61±0.19 Ω.mm and ~382±41 Ω/□, respectively. The higher values of Device A are the results of different contact annealing temperature used (800 and 600^{o}C, respectively for Device A and Device B). The estimated channel resistance, $R_{CHANNEL}$, (i.e., the resistance underneath the gate contact) of Device A and Device B are 2.66 and 3.50 Ωmm , respectively. Since our devices have relatively large L_G = 2.3 µm and L_{SD} = 10 µm, it is not surprising that the influence of $R_{CHANNEL}$ and R_{SH} dominates in R_{on}, $I_{DS(SAT)}$ and g_m. With down scaling and self-aligned process, L_G and L_{SD} will be greatly reduced, thus leading to lower R_{on}, higher $I_{DS(SAT)}$ and g_m.

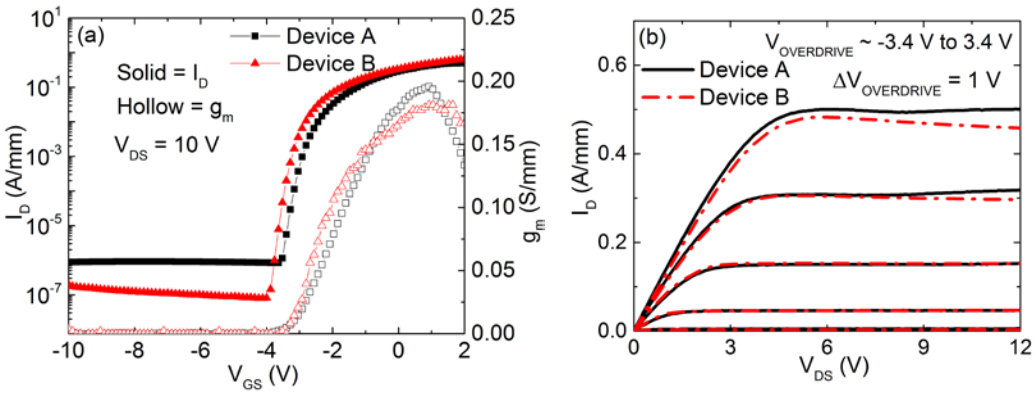

Figure 8.3 (a) $I_{D(LOG)}$ and transconductance (g_m) as a function of V_{GS} at V_{DS} = 10 V and (b) I_D-V_{DS} *at different* $V_{OVERDRIVE}$ of Device A (black square, solid line) and Device B (red triangle, dash-dot line).

8.4 Conclusion

In summary, we have demonstrated the fabrication of $In_{0.18}Al_{0.82}N$/GaN HEMTs on Si substrate with RuO_x Schottky gate and Hf/Al/Ta source/drain contacts using a Single Contact Annealing Process (SCAP) and this is made possible by the thermally robust RuO_x Schottky gate. The electrical characteristics of SCAP fabricated HEMTs are similar to those of comparable devices made by the conventional gate-last process (CGLP), within 10 % difference for most device parameters except for higher gate leakage current (~1.12×10^{-6} versus ~1.82×10^{-7} A/mm) and higher OFF current (~8.64×10^{-7} versus ~2.02×10^{-7} A/mm) in the former. The SCAP offers flexibility in process integration as it can be used to implement both gate-last and gate-first processes, without significant degradation in gate leakage current and OFF current

Chapter 9: Summary and suggested future work

9.1 Summary

In the past few years, significant improvements have been made in AlGaN/GaN HEMTs and InAlN/GaN HEMTs. However, Au-free Schottky contacts on these GaN based HEMTs with high thermal stability and low leakage current are desired for their CMOS compatibility to lower fabrication cost and for their reliability. Hence, the current work was motivated by the realization of thermally robust CMOS compatible Schottky contact for AlGaN/GaN and InAlN/GaN diodes and HEMTs grown on Si(111) substrates and investigation of thermal performance and profiles of these GaN based HEMTs under voltage stress to study the self heating effect.

9.1.1 Pre-RuO_x investigations of CMOS compatible, gold-free Schottky contacts on InAlN/GaN grown on Si (111)

The study of our first Au-free Schottky contact (Ni/W) was reported on InAlN/GaN HEMTs grown on Si (111) substrate. We have optimized the electrical properties of non gold based Ohmic (Ti/Al/Ni/W) and Schottky (Ni/W) contacts for application in InAlN/GaN-on-Si HEMTs. The minimum Ohmic contact resistivity achieved is 1.04×10^{-6} Ωcm^{-2} and the maximum SBH attained is 0.72 eV at room temperature. InAlN/GaN-on-Si Schottky gate HEMTs with non-gold based contacts (Ti/Al/Ni/W Ohmic and Ni/W Schottky) demonstrate performance comparable to devices with gold-based contacts. We have also shown that a thin ZrO_2 passivation layer helps improve the DC characteristics of InAlN/GaN HEMTs, yielding a higher g_m (by

~33.3%) and a lower R_{on} (by ~16.7%). However, with ZrO_2 passivation layer, I_{OFF} increases by more than one order of magnitude and ON-OFF current ratio decreases by ~ one order of magnitude.

9.1.2 Thermally robust RuO_x Schottky diodes and HEMTs on n-GaN and InAlN/GaN heterostructure grown on 100 mm Si(111)

Thermally robust RuO_x Schottky contacts on n-GaN grown on Si(111) substrate exhibit a SBH of 0.9 eV and a leakage current of 10^{-5} Acm^{-2} at – 2 V after annealing in N_2 at 700^{o}C. Furthermore, RuO_x has been found to be more thermally stable than Ni/Au because RuO_x Schottky diodes have a lower leakage current and a higher SBH (~0.4 eV) than Ni/Au Schottky diodes when both are annealed at 800^{o}C. By using RuO_x, instead of Ni/Au, as the Schottky gate contact in $In_xAl_{1-x}N$/GaN-on-Si(111) HEMTs, the ON-OFF current ratio is boosted to ~10^5, after gate annealing at 700^{o}C in N_2. Furthermore, the maximum transconductance of ~0.18 S/mm and ON-resistance of ~8.33 Ωmm are achieved for a gate length of 1.5 µm. Therefore, gold-free HEMTs with RuO_x as a thermally robust gate contact, leading to a reduced leakage and OFF current, are suitable for high temperature applications.

9.1.3 Thermally robust RuO_x based $Al_xGa_{1-x}N$/GaN Schottky HEMTs on 200 mm diameter Si(111) substrates

We have demonstrated Au-free HEMTs using the $Al_xGa_{1-x}N$/GaN heterostructures grown on 200 mm diameter Si(111) for high temperature applications. The source/drain Ohmic contact (Ti/Al/Ni/W) is insignificantly affected by the RuO_x gate with annealing temperature up to 800^{o}C resulting in

little changes in R_c and R_{on}. Furthermore, the Schottky contact (RuO_x) is thermally stable up to 800^{o}C without much degradation in g_m and I_{DSAT}. However, at 900^{o}C, the Ohmic and Schottky contacts degrade and lead to a reduction in g_m and I_{DSAT}, and an increase in R_{on}. The maximum g_m, I_{DSAT} and minimum R_{on} achieved are 0.197 S/mm, 0.55 A/mm and 8.83 Ωmm, respectively, for a 1.5 μm gate HEMT when the gate is annealed at 700^{o}C. We have also achieved the ON-OFF current ratio >10^7 and sub-threshold swing of 90 mV/decade for HEMT annealed up to 800^{o}C. Owing to an improved crystalline quality of $Al_xGa_{1-x}N$/GaN heterostructures and contacts, we have demonstrated HEMTs with electrical characteristics stable up to gate annealing at 800^{o}C.

9.1.4 Probing channel temperature profiles of semitransparent RuO_x based Schottky contacts on InAlN/GaN HEMTs and AlGaN/GaN HEMTs on 200 mm diameter Si(111) by optical spectroscopy

Using semitransparent RuO_x based Schottky contact as a gate electrode and non-destructive optical spectroscopic techniques, we have investigated the channel temperature profiles from source to drain region including the region underneath the gate in AlGaN/GaN HEMT and InAlN/GaN HEMT grown on a 200mm diameter Si substrate. Due to UV excitation, the photo generated carriers are generated and resulting in higher drain current in both InAlN/GaN HEMT and AlGaN/GaN HEMTs. InAlN/GaN HEMTs has higher drain current and higher power dissipation at the same bias voltage compared to AlGaN/GaN HEMTs under both UV illumination and visible illumination. Hence, InAlN/GaN HEMTs has higher maximum temperature (475 K Vs 433

K) compared to AlGaN/GaN HEMTs. Both maximum temperatures are occurred around the gate edge between gate and drain region. With better growth quality heterostructure and recessed Ohmic contacts in AlGaN/GaN HEMTs, it has higher thermal conductivity (76.6 Vs 64.7 $Wm^{-1}K^{-1}$) compared to InAlN/GaN HEMTs at the same power dissipation (~10.2 W/mm). In addition, we have demonstrated that HEMTs grown on Si(111) has higher thermal conductivity than HEMTs grown on sapphire.

9.1.5 Effects of annealing pressure and ambient on thermally robust RuO_x Schottky contacts on InAlN/AlN/GaN-on-Si(111) heterostructure

We have investigated the effects of annealing ambient and pressure on the electrical and material characteristics of RuO_x on $In_{0.17}Al_{0.83}N$/AlN/GaN-on-Si(111)Schottky diodes. When RuO_x Schottky diodes are annealed in vacuum at the pressure of 6.67×10^{-3} Pa, SBH decreases by 0.208 eV and the reverse leakage current increases by one order of magnitude with respect to unannealed diodes. These could possibly be caused by the dissociation of Ru and O bonds leading to the formation of Ru from RuO_x when annealed in vacuum at 800^{o}C owing to high vacuum (6.67×10^{-3} Pa). On the other hand, annealing in Ar at the pressure of 101.3 kPa, increases the SBH by 0.207 eV and decreases the reverse leakage current by about two orders of magnitude. These could possibly be resulted from the formation of RuO_2 in RuO_x Schottky diodes when annealed in Ar due to high temperature (800^{o}C) and high pressure (101.3 kPa) heat treatment. In addition, since the interfacial oxide is found in all samples including unannealed RuO_x, the changes in electrical and material characteristics are less likely due to the presence of

interfacial oxide. The electrical and material characteristics of RuO_x Schottky diodes annealed in N_2 are similar to diodes annealed in Ar. Since Ar is an inert gas, it may be concluded that N_2 does not react with RuO_x or InAlN and that the annealing pressure is the reason for the changes in RuO_x Schottky diodes electrical and material characteristics.

9.1.6 Single Contact Annealing Process for Both Gate-First and Gate-Last RuO_x Gate $In_xAl_{1-x}N$/GaN HEMTs

We have demonstrated the fabrication of $In_{0.18}Al_{0.82}N$/GaN HEMTs on Si substrate with RuO_x Schottky gate and Hf/Al/Ta source/drain contacts using a Single Contact Annealing Process (SCAP) and this is made possible by the thermally robust RuO_x Schottky gate. The electrical characteristics of SCAP fabricated HEMTs are similar to those of comparable devices made by the conventional gate-last process (CGLP), within 10 % difference for most device parameters except for higher gate leakage current (~1.12×10^{-6} versus ~1.82×10^{-7} A/mm) and higher OFF current (~8.64×10^{-7} versus ~2.02×10^{-7} A/mm) in the former. The SCAP offers flexibility in process integration as it can be used to implement both gate-last and gate-first processes, without significant degradation in gate leakage current and OFF current

9.2 Suggested future work

In this work, although the leakage current and thermal stability of AlGaN/GaN HEMTs and InAlN/GaN HEMTs have been effectively improved via employing a high quality RuO_x based Schottky gate electrode, there remain

issues that need to be investigated to further boost the device characteristics. In the following part, some future works are suggested.

9.2.1 Further developments of SCAP

In Chapter 8, we have reported the performance of RuO_x Schottky contact on InAlN/GaN HEMTs fabricated using single contact annealing process (SCAP) in comparison with HEMTs fabricated using conventional gate last process (CGLP). However, large dimension devices (gate length, $L_G \sim 2.3$ μm; source to drain distance, $L_{SD} \sim 10$ μm; and gate to source distance, $L_{GS} = 2$ μm) were used to compare these two types of HEMTs. This limits the electrical performance of these HEMTs. By scaling down the L_G and the use of self-aligned process, the electrical characteristics of HEMTs using SCAP can be improved. With thermally robust RuO_x and SCAP, self-aligned gate-first process could be realized as shown in Figure 1.6. This would minimize L_{GD} and L_{GS}, resulting in the reduction of access resistances from the regions between source/drain and gate. Therefore, with this approach, the device could be improved in terms of high-power and high-frequency performance. In addition, by comparing these HEMTs with CGLP HEMTs with self-aligned gate-last process using dummy gate shown in Figure 1.7, would highlight the benefits of SCAP in term of the reduction in the number of processes, and fabrication cost. Furthermore, as reported in Chapter 8, the annealing conditions used for Ohmic contacts of HEMTs fabricated using SCAP (800^oC in N_2) were different from that used for Ohmic contacts of HEMTs fabricated using CGLP (600^oC in vacuum). This causes the change in electrical performances between these two types of HEMTs. Therefore, it is desirable to

conduct a more direct comparative study between RuO_x Schottky contact InAlN/GaN HEMTs fabricated using SCAP and CGLP using the same Ohmic and/or Schottky annealing conditions (800^oC in N_2).

9.2.2 Reduction of RuO_x gate resistance for RF performance

Although RuO_x Schottky contact has low leakage current and high thermal stability, one of its disadvantages is its high resistivity of 45-60 μΩcm which is ~8 times higher than Ru metal[120]. Even though the effect of high gate resistivity is not seen in HEMT DC performance, it would degrade HEMT's RF performance. Therefore, we would like to propose a 2 layer structure, RuO_x as a base layer and Ru as a capping layer, By using a Ru/RuO_x bilayer structure, the Schottky contact resistance could be reduced. However, the base RuO_x layer thickness has to be optimized in order to achieve low leakage current and high thermal stability. Using RuO_x/Ru Schottky contact as a gate could enhance the performance of AlGaN/GaN HEMTs or InAlN/GaN HEMTs enabling them to be used in RF high power applications.

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