# LOW-POWER IMPULSE-RADIO ULTRA-WIDEBAND TECHNIQUES FOR BIOMEDICAL APPLICATIONS

ZHANG ZHE

(B.Sc, Peking University, China, 2008) (M.Sc, The University of Texas at Dallas, USA, 2009)

#### A THESIS SUBMITTED FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE 2015

# Declaration

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis. This thesis has also not been submitted for any degree in any university previously.

ZHANG ZHE 1ST AUGUST 2015

# Acknowledgements

I would like to express my sincere and great appreciation to my supervisors, Professor LIAN Yong and Associate Professor Koen MOUTHAAN for their valuable guidance, continuous encouragement and essential financial support. I would like to thank Singapore Economic Development Board (EDB) on sponsoring me with the IC Design Postgraduate Scholarship (ICPS) for financial assistance in my Ph.D. study. I would like to thank Prof. HENG Chun Huat, Prof. YANG Zhi, Prof. GUO Yong Xin and Prof. XU Yong Ping for their patient teaching and critical help on class and research work. I would like to thank Mr. TEO Seow Miang and Ms. ZHENG Huan Qun for their assistance in administrative management and CAD support. I wish to thank all my colleagues in Bioelectronics Lab and Signal Processing & VLSI Lab, National University of Singapore for their unselfish help and devoted collaboration. The list below may not be complete and the order does not indicate any importance: Dr LI Yongfu, Dr ZHANG Xiaoyang, Dr WANG Lei, Mr. David WONG, Ms. CHUA Dingjuan, Dr. YANG Zhenglin, Mr. XU Xiaoyuan, Dr. Chacko John DEEPU, Dr. LIEW Wen-sin. Dr. TAN Jun, Dr ZOU Xiaodan, Dr. ZHANG Jinghua, Mr. MAO Wei, Mr. ZHANG Daren, Mr. WANG Baitong, Mr. WU Tong. Finally, this work is also for JIANG Xi, NIU Tianfang, ENG Wei Jie and LI Xuchuan. Your names shall be in the database together with this work.

I also want to appreciate my family for their love and concern throughout my life. My grandmother, Wang Hechun, who had taken care of me since I came to this world and passed away one day before my Ph.D. oral defense, shall always be in my memory. My father, Zhang Jianhua, and my mother, Ma Chunming, deserve my apologies for my causing so much trouble while ignoring your deepest love. My grandfather, Zhang Haoming, constantly inspired and encouraged me when I met with difficulties. I know that my grandparents from mother's side, Ma Zhengyi and Chi Sufang were always with me when I sat at Sentosa amid depression. Finally, I wish to thank Ting Zhang for her remote encouragement and love throughout my study. Wish you best luck in your journey for Ph.D. and your beautiful life.

# Contents

Acknowledgements	ii
Contents in	v
Abstract vi	ii
List of Figures	x
List of Tables x	v
Abbreviations xv	/i
1 Introduction	1
1.1 Motivation $\ldots$	3
1.2 UWB Standard and Technology	5
1.3 IR-UWB for Low-power Wireless Solutions	8
1.4 Organization of the Thesis	9
1.5 List of Publications	1
2 Review of UWB Technologies 13	3
2.1 MB-OFDM-UWB	3
2.2 FM-UWB	4
2.3 IR-UWB	5
2.3.1 Review of State-of-the-art IR-UWB Transmitter	
Architecture and Circuit	7
2.3.2 Review of State-of-the-art IR-UWB Receiver	
Architecture and Circuit	0

#### CONTENTS

	2.3.3 IR-UWB Pulse Design	24
3	Mostly Digital Low Power Inductorless IR-UWB	
	Transceiver in 65 nm CMOS process	32
	3.1 Design Considerations and Goals	32
	3.2 System architecture	36
	3.3 Link budget	36
	3.4 Transmitter Design	39
	3.5 Receiver Design	42
	3.5.1 Active-inductor-based Self-biased Wideband LNA	43
	3.5.2 Pulse Detector $\ldots$	46
	3.5.3 Demodulation and Synchronization	48
	3.6 Measurement Result	50
	3.6.1 Transmitter	51
	3.6.2 Active-inductor-based Wideband LNA $\ .$	53
	3.6.3 Short-range Communication Mode	53
	3.6.4 Radar mode - Respiratory rate measurement	55
	3.7 Tranceiver Front-end Performance Comparison	58
4	A Low-power Low-leakage IR-UWB Transmitter and an	
	IR-UWB Receiver with a Coarse-fine TDC in 130-nm	
	CMOS process	62
	4.1 Design Considerations and Goals	63
	4.1.1 Energy-efficient IR-UWB Transmitter with Low	
	Stand-by Leakage	63
	4.1.2 IR-UWB Receiver with TDC $\ldots$	64
	4.2 Energy-efficient IR-UWB Transmitter with Low Stand-by	
	Leakage	66
	4.2.1 Transmitter Architecture	66
	4.2.2 Circuit Design	68
	4.2.3 Measurement Results and Comparison	70
	4.3 IR-UWB Receiver with a Coarse-fine TDC	76

#### CONTENTS

	4.3.1 Introduction and System Architecture	76
	4.3.2 Circuit Designs and Simulation Results	78
<b>5</b>	A Fully Integrated UWB Event-Driven ECG SoC	87
	5.1 Background and Introduction	87
	5.2 System Architecture $\ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots$	89
	5.3 Circuit Design Considerations	90
	5.3.1 DC-Input Front-End and Level-crossing ADC $\ . \ . \ .$ .	90
	5.3.2 UWB Transmitter and Antenna	92
	5.4 Simulation and Measurement Results	93
	5.5 Summary	96
6	Conclusions and Recommendations for Future Works	97
	6.1 Conclusions	97
	6.2 Recommendations of the Future Work	99
Bi	bliography	101

## Abstract

As the aging population is worldwide growing, health care issues related to aging have attracted much attention from not only policy makers The novel engineering solutions in but also engineering communities. health care could bring tangible benefits for elderly people who suffer Among many engineering solutions related to from chronic diseases. health care, wireless systems are essential. Wireless data communication is the most common application. Data must be transmitted and received in a secure channel under low power consumption. Other applications include contact-less vital-sign detection such as radar for remote sensing of heartbeat and respiration. In recent years, there has been increasing interest in implementing low-complexity, low-power, multi-functional wireless transceivers for biomedical applications. Among all the wireless techniques for biomedical applications, Impulse-radio Ultra-wideband (IR-UWB) is of special interest. In this research, we focus on system architecture and circuit design of low-complexity, low-power, multi-functional IR-UWB transceivers.

The first part of the thesis introduces an inductor-less IR-UWB transceiver for wireless short-range communication and vital-sign sensing. The all-digital transmitter generates IR-UWB pulses using an edge combining technique and consumes 21.6 pJ/pulse at 10 Mbps. A

novel active-inductor-based technique is used to achieve ultra-wideband input impedance matching in the receiver. The non-coherent receiver includes a simple demodulation and synchronization circuit which achieves self-synchronization without any on-chip or external oscillator. The receiver consumes 6.4 mW and achieves a sensitivity of -64 dBm at 10 Mbps. The transceiver is implemented in a 65 nm digital CMOS process and tested in a QFN40 package. The transmitter and receiver occupy only 0.03 mm<sup>2</sup> and 0.01 mm<sup>2</sup> respectively. Measurement results show that the transceiver/radar is capable of sensing the humans respiratory rate when the time interval is measured by a fast sampling digital oscilloscope.

The second part of the thesis presents the design and measurement results of a low-power energy-efficient IR-UWB transmitter for short-range communication and vital-sign sensing, as well as the design of an IR-UWB receiver with a coarse-fine Time-to-digital Converter (TDC) for radar application. In the IR-UWB transmitter, a digitally-controlled oscillator (DCO) generates the carrier frequency and a True Single-Phase Clocking (TSPC) mask generator works as pulse shaper. The cascode transistors in the output driver stage reduce the leakage power while combining the oscillator output and the masks. The transmitter achieves a total pulse energy of 37.9 pJ/pulse with a transmission efficiency of 8.6 %. The maximum output voltage amplitude is 0.94 V. The leakage power is only 0.73  $\mu$ W, which makes it a promising candidate for low-data-rate biomedical IR-UWB transceiver. The power scaling plot shows that the power consumption of the transmitter scales linearly with the data rate down to about 20 kbps. The transmitter is implemented in a 130 nm digital CMOS process and tested in a QFN package. The transmitter occupies 0.146 mm<sup>2</sup>. In the IR-UWB receiver, a multiple-phase Digitally-controlled Oscillator (DCO) is used as the coarse TDC while the fine TDC is realized by a Sigma-delta Time-to-digital Converter (SDTDC). The TDC is designed to achieve a fine resolution with a large dynamic range.

The third part of the thesis shows a case study in which the IR-UWB transceiver is integrated with biomedical sensors in a System-on-a-chip (SoC). The SoC includes an Electrocardiography (ECG) sensor front-end, a Level-crossing (LC) based asynchronous ADC, a low-power IR-UWB transmitter and an on-chip antenna. Implemented in 130 nm digital CMOS process, the system consumes 2.89  $\mu$ W with a 1.2 V supply while transmitting the raw ECG data.

# List of Figures

Figure 1.1	Wireless techniques in biomedical applications. (a)
	Wireless body area network and wireless sensor
	network. (b) Contact-less sensing of vital signs 4
Figure 1.2	UWB standard mask. (a) FCC (US). (b) ECC
	(Europe). (c) Japan. (d) Korea 6
Figure 2.1	MB-OFDM UWB band group allocation 14
Figure 2.2	FM-UWB transceiver block diagram. (a) FM-UWB
	transmitter. (b) FM-UWB receiver. [1] $\ldots \ldots 14$
Figure 2.3	Topology of IR-UWB Transmitters. (a)
	Upconversion. (b) Baseband pulse + Pulse shaper.
	(c) DAC direct synthesis. (d) Digital synthesis 18 $$
Figure 2.4	Topology of IR-UWB Receiver. (a) Coherent
	receivers. (b) Non-coherent receivers. (c) Direct
	sampling receivers. (d) Super-regenerative receivers $21$
Figure 2.5	IR-UWB pulse in time domain and frequency domain
	for $T_W = 140$ ps, $N = 2$ , $A_N = [-0.5, 0.5]$
Figure 2.6	IR-UWB pulse in time domain and frequency domain
	for $T_W = 80$ ps, $N = 2$ , $A_N = [-0.5, 0.5]$
Figure 2.7	IR-UWB pulse in time domain and frequency domain
	for $T_W = 80$ ps, $N = 4$ , $A_N = [0.5, -0.5, 0.5, -0.5]$
Figure 2.8	IR-UWB pulse in time domain and frequency domain
	for $T_W = 80$ ps, $N = 4$ , $A_N = [0.2, -0.5, 0.5, -0.2]$

Figure 2.9	IR-UWB pulse in time domain and
	frequency domain for $T_W = 80$ ps, $N = 20$ ,
	$A_N = [0.01, -0.12, 0.23, -0.34, 0.45, -0.56, 0.67, -0.78, 0.89, -1,$
	1,-0.89,0.78,-0.67,0.56,-0.45,0.34,-0.23,0.12,-0.01]
Figure 2.10	IR-UWB pulse in time domain and
	frequency domain for $T_W = 160$ ps, $N = 2$ ,
	$A_N = [0.01, -0.12, 0.23, -0.34, 0.45, -0.56, 0.67, -0.78, 0.89, -1,$
	1,-0.89,0.78,-0.67,0.56,-0.45,0.34,-0.23,0.12,-0.01]
Figure 3.1	System architecture of IR-UWB system (a)
	short-range communication (b) radar sensor 38
Figure 3.2	Schematic of the IR-UWB transmitter
Figure 3.3	Simulation results of transmitter in (a) time domain
	(b) frequency domain. $\dots \dots \dots$
Figure 3.4	Schematic of the active-inductor-based wideband LNA. 43
Figure 3.5	Simulation results of the LNA. (a) Simulated $ S_{11} $ .
	(b) Simulated voltage gain and noise figure 45
Figure 3.6	Simulation results of the LNA with and without
	active-inductor-based input matching 40
Figure 3.7	Pulse detector. (a) Schematic of the PD. (b)
	Mechanism of pulse detection $\ldots \ldots \ldots \ldots \ldots 4$
Figure 3.8	Receiver input power level vs frequency (BER $\geq 10^{-1}$ ) 48
Figure 3.9	(a) Schematic of the demodulator. (b) Timing
	diagram of demodulation and synchronization $49$
Figure 3.10	Micrograph of the chip. $\ldots \ldots \ldots$
Figure 3.11	Transmitter output in (a) time domain (b) frequency
	domain. $\ldots \ldots 52$
Figure 3.12	Simulated and measured $ S_{11} $
Figure 3.13	Measurement setup for communication mode. (a)
	Block diagram of the test setup. (b) LOS free space
	test environment. $\ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots 54$

Figure 3.14	(a)Transmitted and received NRZ data, (b)BER	
	versus input power	55
Figure 3.15	Measurement setup for radar sensor mode. (a) Block	
	diagram of the test setup (b) Test environment for	
	measuring human respiration. $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$	56
Figure 3.16	Respiration measurement (a) normal respiration in	
	the time domain (b) normal respiration in the	
	frequency domain. $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$	57
Figure 3.17	Respiration measurement (a) fast respiration in the	
	time domain (b) fast respiration in the frequency	
	domain. $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$	57
Figure 3.18	Human respiration changes from normal respiration	
	to held respiration to resumed respiration	58
Figure 4.1	Architecutre of the IB-UWB radar with	
i iguio ili	time-to-digital converter	65
Figure 4.2	Architecture of the IR-UWB Transmitter.	66
Figure 4.3	Schematic of the one-shot circuit.	67
Figure 4.4	Schematic of digitally-controlled oscillator.	68
Figure 4.5	Die micrograph of the IR-UWB transmitter	70
Figure 4.6	Transmitter output in time domain	71
Figure 4.7	Transmitter output in the frequency domain and its	
0	compliance with the FCC mask	72
Figure 4.8	Transmitter output in the frequency domain for	
0	various supply voltages.	72
Figure 4.9	(a)Power consumption of the transmitter versus the	
Ū.	PRF, (b) Energy per pulse of the transmitter versus	
	the PRF	73
Figure 4.10	Center frequency of the transmitter output versus	
-	different tuning codes	73

Figure 4.11	System architecture of the proposed time-to-digital	
	converter	76
Figure 4.12	Circuit of the receiver front-end, LNA and Power	
	Detector	79
Figure 4.13	Circuit of multi-phase recirculating oscillator. $\ . \ . \ .$	80
Figure 4.14	Timing diagram of multi-phase recirculating oscillator.	80
Figure 4.15	Circuit of the differential delay cell	81
Figure 4.16	Digital delay control of the delay element. $\ldots$ .	82
Figure 4.17	Circuit of the sigma-delta time-to-digital converter	82
Figure 4.18	Circuit of combined phase selector and charge pump.	83
Figure 4.19	SDTDC output in (a) time domain (b) frequency	
	domain. $\ldots$	84
Figure 4.20	Chip layout of the receiver with time-to-digital	
	converter	85
Figure 4.21	Time-domain measurement of the UWB receiver	
	front-end. $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$	86
Figure 4.22	Measured digital delay control of the delay element	86
Figure 5.1	Topology of IR-UWB	89
Figure 5.2	Circuit of ECG AFE	90
Figure 5.3	Circuit of level-crossing ADC $\ldots \ldots \ldots \ldots \ldots$	91
Figure 5.4	Topology of IR-UWB transmitter with on-chip antenna $% \mathcal{A}$	92
Figure 5.5	Die micrograph of the SOC $\ldots \ldots \ldots \ldots \ldots \ldots$	93
Figure 5.6	(a) Input-referred noise of the analog front-end, (b)	
	Output spectrum of the front-end and ADC	94
Figure 5.7	UWB TX output in (a) time domain and (b)	
	frequency domain. $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$ $\ldots$	95
Figure 5.8	On-chip antenna characteristics (a) Simulated and	
	measured input matching (b) Radiation pattern	
	when $\Phi = 0^{\circ}$ and $\Phi = 90^{\circ}$ at 4 GHz	95

Figure 5.9 (a) UWB TX power consumption vs data rate, (b) ECG signal reconstructed from wireless transmission. 96

# List of Tables

Table 3.1	Link Budget Calculation	39
Table 3.2	Transmitter Performance Comparison (I)	60
Table 3.3	Receiver Performance Comparison (I)	61
Table 4.1	Transmitter Performance Comparison (II)	75

# Abbreviations

#### **IR-UWB** Impulse-radio Ultra-wideband

- **FCC** Federal Communication Commission
- **PSD** Power Spectrum Density
- **MB-OFDM-UWB** Multiband Orthogonal Frequency-division Multiplexing Ultra-wideband
- FM-UWB Frequency-modulated Ultra-wideband
- **UWB** Ultra-wideband
- **WSN** Wireless Sensor Network
- **WBAN** Wireless Body Area Network
- **CMOS** Complementary Metal-Oxide-Semiconductor
- **ECG** Electrocardiography
- **ADC** Analog-to-digital Converter
- **DAC** Digital-to-analog Converter
- **LO** Local Oscillator
- PLL Phase-locked Loop

- **FOM** Figure of merit
- **CS** Common-source
- **CG** Common-gate
- **LNA** Low-noise Amplifier
- **SNR** Signal-to-Noise Ratio
- **TSPC** True Single-Phase Clocking
- **EM** Electromagnetic
- **SoC** System-on-a-chip
- **RF** Radio-frequency
- **WLAN** Wireless Local Area Network
- **IoT** Internet of Things
- **QoS** Quality of Service
- **MAC** Medium Access Control
- **PHY** Physical
- **LTE** Long Term Evolution
- **DLL** Delay-locked Loop
- **DSP** Digital Signal Processing
- **NRZ** Non-return-to-zero
- **S-OOK** Synchronized-OOK
- **CCU** Central Control Unit
- **DCO** Digitally-controlled Oscillator

- **ED** Energy Detector
- **CS** Common-source
- **CG** Common-gate
- **ESD** Electrostatic Discharge
- **PSC** Pulse Stretching Circuits
- **DFF** D Flip-Flop
- **BER** Bit Error Rate
- **ToF** Time of Flight
- FOMs Figures of Merit
- **PRF** Pulse Repetition Frequency
- $\textbf{MSBs} \hspace{0.1in} \operatorname{Most} \hspace{0.1in} \operatorname{Significant} \hspace{0.1in} \operatorname{Bits} \hspace{0.1in}$
- **LSBs** Least Significant Bits
- **TDC** Time-to-digital Converter
- **DPLL** Digital Phase-locked Loop
- **SDTDC** Sigma-delta Time-to-digital Converter
- **SDADC** Sigma-delta Analog-to-digital Converter
- **NB** Narrow-band
- **CVD** Cardiovascular Disease
- **AIC** Analog-to-information Converter
- **LC** Level-crossing
- **RO** Ring Oscillator

- **DPAs** Digital Power Amplifiers
- **AFE** Analog Front-end
- **IAs** Instrumental Amplifiers
- **PGA** Programmable-gain Amplifier
- **PD** Pulse Detector

# Chapter 1

# Introduction

Integrated circuit technologies have changed our life by providing us products with faster computing speed, more storage capacity and increasing mobility for decades. In recent years, the rapid scaling of Complementary Metal-Oxide-Semiconductor (CMOS) technology leads to the reduction of the feature sizes of the transistors. This increases the speed of the transistors and enables more transistors to be fabricated per unit chip area which facilitates integration of more functionalities. Though advanced CMOS technology continuously improves the performance of the digital circuits, it poses challenges for the analog circuit designers with reduced transistor intrinsic gain, increased reliability issues, inferior Signal-to-Noise Ratio (SNR) and incomplete or inaccurate device models. Integrating analog and/or Radio-frequency (RF) circuits with digital circuits in SoC, which of great interests for most people from academia and industry, is still a challenging task. Promising approaches for improving the performance of analog/RF circuits exploit the increasing speed and area efficiency of the digital counterparts [2]. Digitally assisted analog circuits are widely used in modern circuits and the performance of the analog/RF circuits are

increased continuously when the CMOS technology node approaches 10 nm. Some researchers even push more boldly in investigation of replacing the traditional analog/RF circuits with all-digital circuits [3].

Wireless technology is everywhere around us. Modern wireless technology evolves into countless products and occupies a trillion-dollar market from the original Maxwell's equations and quantum physics theories. Most of the people can be connected wirelessly by 3G/Long Term Evolution (LTE) mobile networks worldwide and Wireless Local Area Network (WLAN) is indispensable for many people at office or at home. The future of the wireless technology will be into several directions. 5G mobile network, which is possible to be implemented within this decade, aims at providing subscribers with super-high-speed wireless connections [4]. Internet of Things (IoT) comes to age when the internet networks expand to places such as manufacturing plants, power grids, healthcare facilities and transportation. IoT connects uniquely identifiable embedded computing devices within the existing internet infrastructure. In the future, it is very likely that every electronics device could be connected wirelessly. Requirements for next-generation wireless networks include increasing data rate, high Quality of Service (QoS) and better network security. There will be huge demands for wireless devices with low power, low cost and high reliability in the next few decades.

There is an increasing interest in low-power wireless technologies for biomedical applications. The global medical semiconductor market revenue will be doubled from \$ 3.2 billion in 2009 to \$ 6.8 billion in 2017 and wireless devices is one of the main forces that boost the growth [5]. With the migration from the expensive hospital-centric therapies to the low-cost patient-centric disease management and health monitoring in the daily life, more wirelessly connected biomedical devices are desired. Recent achievements in integrating low-energy biosensor, low-power signal processing and storage units with wireless communication techniques has made a non-invasive, low-cost, continuously-monitoring wearable healthcare system possible [6]. Continuous monitoring of human's health condition with reliability and agility demands the following requirements First, continuous operation covering 24 for the wireless techniques. hours for several days requires that the whole system runs under quite Provided with the constraint of the size of battery and low power. charging intervals, the wireless transmission is required to operate in low power consumption and high energy efficiency. Second, the wireless transmission must always be reliable. Sparkle events that endanger people's lives must be recorded and transmitted swiftly anytime in the whole continuous monitoring period. Any intermittent system or device fault is intolerable. Third, the wireless transmission must follow certain worldwide approved standards to facilitate successful wireless access and connection in different environments. Apart from the wireless communication which is very important in biomedical applications, there are other roles wireless techniques are able to play. Contact-less vital-sign monitoring could be a valuable tool in sleep monitoring and home health care systems, in which perturbation by the contact or invasive sensor system is undesirable [7]. For some implantable biomedical devices, power is delivered wirelessly and contact-less, high-efficiency power transfer has been a research focus [8].

### 1.1 Motivation

Wireless biomedical circuits can be grouped into several categories based on the applications. Wireless data communication is the most common application including Wireless Body Area Network (WBAN)







(b)

Figure 1.1: Wireless techniques in biomedical applications. (a) Wireless body area network and wireless sensor network. (b) Contact-less sensing of vital signs.

and Wireless Sensor Network (WSN), as shown in Fig. 1.1(a). The wireless sensor nodes in the WBAN or WSN should meet the following requirements: minimum form factor, minimum weight and cost, low-power operation, compatibility with standard-based protocol, and user-specific configurability and customization. Another application is contact-less vital-sign detection such as radar for remote sensing of heartbeat and respiration as shown in Fig. 1.1(b). Examples of this application include patient motion monitoring, sleep apnea alert and continuous vital-sign recording.

For all these applications mentioned above, low emission level, low power, and low cost are essential requirements. Low emissions ensure the Electromagnetic (EM) radiation does not cause hazardous effects to the human body. Low power consumption is required to ensure long battery life, which is crucial for prolonged continuous operation, especially in portable and implantable systems. Low cost is important for affordable treatment and health monitoring, as well as enabling minimal-cost disposable solutions. Configurable wireless circuits which are able to accomplish different tasks are favorable because of cost reduction and easy SoC integration. A configurable multi-functional chip that serves both wireless data communication and remote sensing is highly desirable in wireless biomedical systems.

### 1.2 UWB Standard and Technology

In 2002, the Federal Communication Commission (FCC) released a new unlicensed Ultra-wideband (UWB) frequency domain of 3.1-10.6 GHz to the market [9]. The emission level allowed by FCC for UWB signal



Figure 1.2: UWB standard mask. (a) FCC (US). (b) ECC (Europe). (c) Japan. (d) Korea.

(-41.3 dBm/MHz) [9] is very low and the potential harmful physiological effect from the EM radiation is weak. Fig. 1.2 shows the frequency masks regulated by different countries. The very low Power Spectrum Density (PSD) avoids interference with existing Narrow-band (NB) communication systems. The ultra-low PSD is compensated by the ultra-wide bandwidth to support wireless transmission. Due to the very low transmitted power allowed by the regulation, UWB technology may not be able to support reliable wireless signal transmission over a long distance; e.g. tens of meters. However, it provides exciting opportunities for some specialized medium or short-distance applications. One application using UWB technology targets at wireless data transmission at rates of hundreds of Mbps or a few Gbps for consumer electronics such as wireless USB [10] and inter-chip communications [11], [12].Apart from the high-speed systems which take advantage of the narrow pulse width of the UWB signals, another category of systems exploits the heavy duty-cycling of the UWB signal

transmission which leads to significant power reduction for low-data-rate wireless communication. This is a huge advantage for applications such as WSN, WBAN or implantable systems in which power conservation is one of the top requirements [13–15].

The large bandwidth of the UWB signal translates to very narrow pulses in the time domain. The pulse-like nature of the UWB signal not only enables heavy duty-cycling of the circuit which reduces the power consumption significantly, but also allows high-resolution positioning, localization and sensing [16, 17].

In 2012, Part 15.6 of the IEEE 802 standard was finalized with focus on Wireless Body Area Networks [18]. The standard defines the Medium Access Control (MAC) layers supporting several Physical (PHY) layers. In the IEEE 802.15.6 standard, UWB PHY layer is chosen as an option for implementing low power, medium or low-data-rate wireless communication. Transceiver chips in compliance with the IEEE 802.15.6 standard has been reported [19], though there has been no reported work integrating both the NB and UWB PHY layer implementations so far.

For UWB technology, several approaches for PHY implementation Multiband Orthogonal Frequency-division Multiplexing are possible: Ultra-wideband (MB-OFDM-UWB), Frequency-modulated (FM-UWB), Ultra-wideband and Impulse-radio Ultra-wideband (IR-UWB). MB-OFDM-UWB divides the ultra-wide full band into several narrower sub-bands and use traditional coherent transceivers to perform the modulation and demodulation. MB-OFDM-UWB is designed to provide high-rate data transmission and is power hungry with complex circuitry. FM-UWB is an analog implementation of a spread-spectrum system that targets short-range (1-10 m) applications with bit rate up to 100 kbps. Local Oscillator (LO) or carrier synchronization at the FM-UWB receiver is not required which results in a simple transceiver architecture.

## 1.3 IR-UWB for Low-power Wireless Solutions

IR-UWB is widely investigated for use in low-power biomedical or sensor applications. IR-UWB takes the advantage of the wideband nature by sending and receiving very short pulsed signals. As stated previously, the pulse-like nature of the IR-UWB signal not only enables heavy duty-cycling of the circuit, which reduces the power consumption significantly, but also allows high-resolution localization and sensing. Mostly-digital or all-digital circuitry could be used because of the wideband signal characteristics. The IR-UWB system is able to achieve lower circuit complexity and low power consumption. Because of the pulse nature, IR-UWB wireless transceiver can be designed to support a wide-range of data rates, and the power consumption is highly scalable with the data rate. State-of-the-art CMOS IR-UWB transceivers support data rates from several hundred kbps to several Gbps. The power consumption ranges from several tens of microwatts to several hundred milliwatts.

This thesis focuses on IR-UWB. Our objective to design mostly-digital, low-power, CMOS IR-UWB transceivers for biomedical applications. By reviewing the reported state-of-the-art designs, our works are designed to achieve the following goals in several directions. First, the total power consumption should be further reduced while the power efficiency should be increased compared with the reported works. The design of the IR-UWB transceiver should accommodate the application requirements and the link budget while achieving good performance. Not only the active power, but also the static power should be minimized to achieve better power efficiency and make power consumption scaling to lower data rates possible. Second, the cost of the IR-UWB transceiver should be minimized. The number of off-chip components should be reduced. To facilitate a SOC solution, the on-chip area should also be minimized, which indicates less use or absence of on-chip passive inductors. We will also explore the opportunity of using on-chip antennas to further reduce the off-chip components, thus making efforts in realizing a disposable biosensor solution. Last but not the least, we would like to design IR-UWB transceivers which can be used not only for short-range communication, but also for micropower vital-sign radar sensor. Multifunctional transceivers are investigated in different application scenarios.

### **1.4** Organization of the Thesis

The thesis is organized as follows: Chapter 2 reviews different UWB techniques and PHY implementations, with focus on literature reviews of the state-of-the-art IR-UWB transceivers and pulse shape design. Chapter 3 covers the design of an inductorless IR-UWB transceiver for wireless short-range communication and vital-sign sensing. Link budget calculations and system architecture will be discussed first. The design procedures and measurement results follow. Chapter 4 introduces the design and measurement results of a low-power energy-efficient IR-UWB transmitter with LO and mask combining technique. It also includes the design of an IR-UWB receiver with a coarse-fine TDC. Chapter 5 shows a case study in which the IR-UWB transceiver is integrated with biomedical

sensors in an SoC. Finally, chapter 6 discusses possible future work with the conclusions drawn.

### **1.5** List of Publications

- Zhe Zhang, Yongfu Li, Koen Mouthaan and Yong Lian, "A Miniature Inductorless IR-UWB Transceiver for Wireless Short-range Communication and Vital-sign Radar Sensor'," *IEEE ISSCC Student Research Preview*, Feb 2014.
- Zhe Zhang, Yongfu Li, Koen Mouthaan and Yong Lian, "A Miniature Reconfigurable Inductorless IR-UWB Transceiver and Radar for Wireless Short-range Communication and Vital-sign Sensing", revised for *IEEE Transactions on Biomedical Circuits and* Systems.
- Zhe Zhang, Yongfu Li, Xiaoyang Zhang and Yong Lian, "A 726-nW, 940-mVpp, 1-kpulses/s all-digital 3-to-5-GHz IR-UWB Transmitter for Short-range Communication and Radar Sensing in 130-nm CMOS", submitted to *IEEE Transactions on Circuits and Systems – II: Express Briefs.*
- Xiaoyang Zhang, Zhe Zhang, Yongfu Li, Changrong Liu, Yongxin Guo and Yong Lian, "A 2.89-μW Fully Integrated UWB Event-Driven ECG Sensor for Dry Electrode Use," Design Contest Award for International Symposium on Low Power Electronics and Design (ISLPED), 2015.
- Xiaoyang Zhang, Zhe Zhang, Yongfu Li, Changrong Liu, Yongxin Guo and Yong Lian, "A 2.89-μW Fully Integrated UWB Event-Driven ECG Sensor for Dry Electrode Use," accepted for Solid-State Circuits (A-SSCC), IEEE Asian Conference on, 2015.
- Yongfu Li, Zhe Zhang and Yong Lian, "Energy-efficient charge-recovery switching scheme for dual-capacitive-arrays SAR ADC," *Electronics Letters*, vol. 49, no. 5, pp. 330-332, 2013.

- Yongfu Li, Zhe Zhang, Dingjuan Chua and Yong Lian, "Placement for binary-weighted capacitive-array in SAR ADC using multiple weighting methods", *IEEE Transactions on Computer-Aided Design* of Integrated Circuits and Systems, vol. 33, no. 9, pp. 1277-1287, 2014.
- Yongfu Li, Wei Mao, Zhe Zhang and Yong Lian, "An ultra-low voltage comparator with faster comparison time and reduced offset voltage," *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2014.
- Yongfu Li, Zhe Zhang and Yong Lian, "A Dual-Channel 0.6-V 250-kS/s 4-to-10-bit Resolution-Reconfigurable SAR ADC for Sensor Applications," submitted to *IEEE Transactions on Circuits and Systems I: Regular Papers.*
- Yongfu Li, Zhe Zhang, Xiaoyang Zhang and Yong Lian, "A 0.4-to-1.2-V fully-digital low-dropout voltage regulator with fast-transient algorithm", submitted to *IEEE Transactions on Power Electronics*.

## Chapter 2

## **Review of UWB Technologies**

### 2.1 MB-OFDM-UWB

MB-OFDM-UWB is a frequency domain solution and targets high-data-rate communication while consuming considerable power. MB-OFDM-UWB works in similar ways as narrow-band communication systems by dividing the ultra-wide full band into several sub-bands [10,20–23]. It was adopted by the WiMedia Alliance supporting data rates from 53.3 to 480 Mbps [24]. The wireless link supports data transmission of high data rates which is comparable to wired applications such as USB2.0. The full ultra-wide 3.1-10.6 GHz band is divided into 14 sub-bands each with a bandwidth of 528 MHz (Fig. 2.1). Each band is further divided into 128 subchannels. The MB-OFDM-UWB is able to transmit and receive very high-rate data. However, the power consumption is also high. Most of the reported MB-OFDM-UWB transceivers consumes power of tens or hundreds of milliwatts [10, 20–23]. The high power consumption makes it



Figure 2.1: MB-OFDM UWB band group allocation



Figure 2.2: FM-UWB transceiver block diagram. (a) FM-UWB transmitter. (b) FM-UWB receiver. [1]

unsuitable for low power biomedical applications. Integration with other biomedical circuits such as analog front-end, Digital Signal Processing (DSP) circuits is also difficult because the complex circuit architecture requires a large chip area.

### 2.2 FM-UWB

FM-UWB is an analog implementation of a spread-spectrum system that targets short or medium-range (1-10m) applications with bit rates up to 100 kbps. It is included in IEEE 802.15.6 WBAN standard [18]. The advantages of FM-UWB include the low-complexity circuit architecture without requiring carrier synchronization and the immunity to interference because of its high frequency band (7.5-8.5 GHz) (Fig. 2.2). The data rate of FM-UWB transceiver, however, is mostly lower than 100 kbps [1, 25]. This restricts its use in some of the medium data-rate applications.

### 2.3 IR-UWB

IR-UWB does not use modulated carriers but ultra-short and modulated pulses to transmit and receive data. The carrierless and pulse-like nature leads to a large idle-to-active duty cycle ratio when the data rate is low. When there is no pulse transmitted and received, the transceiver circuits can be switched off to conserve energy. Digital circuitry could be intensively used in IR-UWB for two reasons. First, we could exploit the novel mostly-digital or all-digital circuits to generate the IR-UWB pulses. The continuing scaling of the digital CMOS process provides us with digital gates with smaller delay and decreasing transition power, which could be utilized to produce ultra-fast pulses with very large bandwidth. Second, digital circuits do not consume static power when there is no active transitions. If the IR-UWB system is implemented in an almost-digital or all-digital manner, the power consumption is the combination of the active power which is present for only the pulse durations, and the leakage power which is dominant in the intervals between the pulses.

The special characteristics of IR-UWB has led to great interest in the development of low-power and cost-effective IR-UWB transceivers, though

challenges still exist. Though the heavy duty-cycling is able to significantly reduce the active power, the leakage power could not be neglected when the data rate is very low. In the biomedical systems such as portable ECG devices [26], the power consumption of the sensor front-end, ADC and DSP is so low that the RF transceiver consumes the most amount of power [27]. If the power consumption of the biosensor SoC is constrained tightly, the leakage power of the transceiver must be carefully examined. Due to the required driving capability on the antenna impedance in the transmitter and noise and gain requirements in the receiver, some of the transistors in the IR-UWB transceivers can be very large and the leakage power could not be neglected.

The other challenge lies in the receiver synchronization and demodulation. The coherent receiver architecture requires a frequency synthesizer or a template generator which increases the circuit complexity and power consumption [14, 28]. The non-coherent IR-UWB transceiver architecture thus has been widely used in low-power and low-cost applications [13, 15, 29–31]. In the non-coherent receiver, the UWB pulse is detected by self-mixing or energy detection and an oscillator is not required in the radio front-end. In the wireless communication application, however, this simplicity is penalized due to the complex baseband demodulation and synchronization. The conventional implementation requires a Phase-locked Loop (PLL) or a Delay-locked Loop (DLL) for clock and data recovery [32]. Some of the reported works did not use PLL or DLL in the baseband [33]. However, the circuit is still complex and power hungry. Many of the reported IR-UWB works focus only on the analog/RF front-end design. The outputs of the transceivers are in the form of pulse trains. This is difficult for DSP to perform synchronization and demodulation. Energy efficient synchronization and demodulation is still one of the challenges in IR-UWB design.
As mentioned in previous sections, the pulse-like nature of the IR-UWB not only enables heavy duty-cycling of the transceiver circuits which reduces the power consumption significantly, but also allows for high-resolution, real-time localization and remote sensing. Many references reported discrete or integrated solutions for IR-UWB ranging and localization [13, 14, 16]. Ultra-short UWB pulses in the time domain help IR-UWB achieve ranging resolution of several millimeters. Real-time CMOS IR-UWB radars for human vital sign monitoring and illness diagnosis have been reported in [17, 34, 35].

In this research work, IR-UWB is chosen for transceiver implementation. In Chapter 3, the transceiver utilizes the advantages of IR-UWB in both low-power wireless data transmission and high-resolution remote sensing. The analog/RF part is reused in communication and radar modes and digital baseband is reconfigured for different operation modes. Improved synchronization and demodulation circuits are introduced. In Chapter 4, the leakage reduction in IR-UWB transmitter and transmission efficiency enhancement will be discussed.

The following two subsections give reviews on state-of-the-art IR-UWB transceiver architectures and circuits. Pulse design and pulse shaping will also be discussed.

# 2.3.1 Review of State-of-the-art IR-UWB Transmitter Architecture and Circuit

IR-UWB pulses can be generated by four different methods: Upconversion, Baseband pulse + Pulse shaper, Digital-to-analog Converter (DAC) direct synthesis and Digital synthesis. (Fig. 2.3)



Figure 2.3: Topology of IR-UWB Transmitters. (a) Upconversion. (b) Baseband pulse + Pulse shaper. (c) DAC direct synthesis. (d) Digital synthesis.

The first one is an extension of the traditional narrow-band approach (Fig. 2.3(a)). The baseband signal is up-converted by an LO oscillating at the carrier frequency [36]. The LO generator and the frequency upconverter use quite an amount of power. A derivation of this approach is the pulsed oscillator in which the oscillator is started and stopped by the baseband pulse [29,31,37–44]. When the pulses are not generated, the oscillator can be shut down to save power. The response time of the oscillator limits the bandwidth of the transmitter output. The center frequency and the bandwidth of the UWB pulses are determined by the LO frequency and the width of the baseband pulse.

The second method is to use a pulse shaper to shape a narrow baseband pulse to fit the pulse into the regulation mask (Fig. 2.3(b)) [45, 46]. The output pulse shaping stage is usually composed of multiple on-chip or off-chip inductors and capacitors. The advantages of this topology include that the spectrum could be well fit into the regulation mask provided that good and accurate designs of the passive devices is achieved. The output voltage swing could be as large as above the supply voltage since the LC filter can make the best use of the regulation mask and the inductors have shunt-peaking effect. The disadvantages of the LC filter are that it is hardly reconfigurable and the large number of on-chip or off-chip passive components are costly.

The third method is to directly synthesize the IR-UWB pulse using an ultra-fast DAC (Fig. 2.3(c)) [13,47]. With the fast speed of the advanced CMOS process, it is possible to directly synthesize the IR-UWB signal using DAC. DAC with Nyquist sampling rate at above 10 GS/s is very power consuming, and it is very difficult to achieve good resolution. In order to make the waveform spectrum in compliance with the FCC mask, an off-chip filter is often required.

The fourth method is to synthesize the UWB pulse by all digital gates (Fig. 2.3(d)) [11, 48–52]. First, impulse generators produce positive or negative impulses which are delayed relative to each other by digital delay stages. Then the short pulses are directly or indirectly combined. The advantages of this technique are its simplicity and all-digital implementation, relatively small area, and low power. In our work, this method is used to generate the IR-UWB signal in the transmitter in a low-power, energy-efficient way.

# 2.3.2 Review of State-of-the-art IR-UWB Receiver Architecture and Circuit

The IR-UWB receivers can be divided into four categories: Coherent receivers, non-coherent receivers, super-regenerative receivers and direct sampling receivers (Fig. 2.4).

The coherent receivers are similar to the narrow-band receivers (Fig. 2.4(a)) [14,28,53–59]. A LO or a pulse template is correlated or multiplied with the received signal. The high frequency signal is mixed down to a lower frequency for further processing. The coherent receivers can achieve good sensitivity and can adopt many demodulation schemes. However, for applications that require low power consumptions, coherent receivers are not suitable. To generate LO signal or pulse template requires complex circuits and threatens the power budget which many low-power applications can accept. In some references, the power of generating the LO signal or pulse template are not included [55, 58]. This lacks the considerations on the system level.



Figure 2.4: Topology of IR-UWB Receiver. (a) Coherent receivers. (b) Non-coherent receivers. (c) Direct sampling receivers. (d) Superregenerative receivers.

Direct sampling is also proposed in some references (Fig. 2.4(c)) [17,60], mostly for radar applications. Multiple-bit ADC or even single-bit ADC is used to sample the UWB signal at Nyquist rate. Considering the high frequency and wideband nature of the UWB signal, the sampling rate of ADC should be very high. The sampling rate needs to be 10 GS/s for the UWB low band (3-5 GHz) and 20 GS/s for the UWB higher band (6-10)GHz). Sampling the signal with high resolution is advantageous in the sense of recovering the exact profile of the IR-UWB signal. This is meaningful in radar applications, but is not necessary in communication, where one or multiple pulses represent one symbol of '1' or '0'. In [17], the IR-UWB signal is directly sampled in a time-interleaved manner. In [60], equivalent sampling technique was used. In the equivalent sampling architecture, the absolute sampling rate is slightly different from the pulse rate. The absolute sampling rate is not high but the difference between the sampling rate with the pulse rate should be precisely controlled to realize high time resolution. Direct sampling is seldom used in low-power communication **IR-UWB** transceivers.

The super-regenerative receiver is another topology for IR-UWB receiver (Fig. 2.4(d)) [61]. The technique is based on turning on and off an oscillator briefly when the IR-UWB pulse arrives. If an input pulse is present when the oscillator is on, the oscillation will start quickly and the amplitude of oscillation can reach a threshold to detect the pulse. The super-regenerative receiver takes the advantage that the whole front-end, including the power-consuming front-end amplifier, could be turned off when the oscillator is not oscillating. Challenges are in realizing the synchronization between the on window of the oscillator and the short pulse.

Non-coherent receivers, on the other hand, require no LO or pulse generator (Fig. 2.4(b)) [15, 29–31, 62–64]. The amplified input signal is

down-converted to baseband by a self-mixer or Energy Detector (ED). A threshold detector or comparator after the self-mixer or ED will retrieve the data of 1 or 0. This approach saves a lot of power by eliminating the LO or pulse generator, so it has been investigated intensively in the applications of WSN, WBAN and low power biomedical devices. One limitation of the non-coherent receivers comes from the mixing nature of the self-mixer or ED. While collecting the energy of the weak UWB signal, the self-mixer or ED also collects the energy of the noise over a wide band. Employing wideband RF amplification before the self-mixer or ED adds more noise across the wide band. To increase the sensitivity of the receiver, some works used integration after the self-mixer or ED to collect the energy from more than one pulse [62]. However, the improved sensitivity is achieved at the sacrifice of data rate, since multiple pulses (or chips) are used to represent one symbol. This method is advantageous for lower data rate applications. In order to align the integration window with the data pulses, usually one packet of data is transmitted at a time. A header is sent first to synchronize the integration window and data bits are sent later. For non-coherent receivers, synchronization and demodulation are great challenges due to the large idle-to-active duty cycle ratio. The data could not be sampled by the oversampling method and Non-return-to-zero (NRZ) data recovery is difficult. A Synchronized-OOK (S-OOK) non-coherent receiver was proposed in [29] to use a synchronizing pulse to latch the data pulse. In [29], an external clock is used to trigger the demodulator and synchronizer. In our design, as shown later, the demodulator and synchronization circuit is greatly simplified and no clock is needed in the demodulator. It is more resilient to the timing jitter and easier to scale with the data rate.

#### 2.3.3 IR-UWB Pulse Design

Though the approved FCC UWB band of 3.1-10.6 GHz is very wide, it still requires careful pulse shape design to fit the IR-UWB output spectrum into the FCC spectral mask. The challenge in meeting the FCC mask is mainly due to the spectrum notch from 960 MHz to 1.6 GHz, which is regulated to minimize the UWB interference to the GPS band. The sidelobes of the UWB signal spectrum should be controlled to avoid the spectrum violation. The Matlab simulations from Fig. 2.5 to 2.10 show different IR-UWB waveforms in the time domain and frequency domain. The Pulse Repetition Frequency (PRF) is 10 MHz and the output voltage amplitude is normalized to 1 V. One variable in the waveform design is the pulse width  $T_W$ , which determines the center frequency. The pulse bandwidth and the pulse shape are controlled by  $T_W$ , the number of impulses, N, and the amplitude of each impulse,  $A_N$ .

A zero-order Gaussian monopulse can be described by the Equation 2.1,

$$p(t) = Aexp(-\frac{t^2}{2T_W^2})$$
(2.1)

The equation in time domain in Equation 2.1 has a frequency domain representation of,

$$P(f) = AT_W \sqrt{2\pi} exp(-\frac{(2\pi f T_W)^2}{2})$$
(2.2)

The equation in the frequency domain shows that the bandwidth of the gaussian pulse is controlled by the width of the pulse in the time domain,  $T_W$ .

A first-order Gaussian monopulse can be described by the equation in Equation 2.3,

$$p(t) = Aexp(-\frac{(t-T_D)^2}{2T_W^2}) - Aexp(-\frac{(t+T_D)^2}{2T_W^2})$$
(2.3)

The frequency domain expression of the Equation 2.3 is in Equation 2.4

$$P(f) = AT_W \sqrt{2\pi} exp(-\frac{(2\pi fT_W)^2}{2})(exp(-i2\pi fT_D) + exp(-i2\pi f(-T_D)))$$
  
=  $2AT_W \sqrt{2\pi} exp(-\frac{(2\pi fT_W)^2}{2})cos(2\pi fT_D)$   
(2.4)

The Equation 2.4 shows that the center frequency of the first-order Gaussian pulse is mainly determined by the parameter  $T_D$ , which is half the distance between the positive impulse and negative impulse. As it will be shown in the analysis later in this subsection, first-order Gaussian pulse occupies large bandwidth at lower frequency and it is very difficult for the first-order Gaussian pulse to meet the FCC mask. In order to obtain more control over the band shape of the UWB signal, one of the solutions is to add more impulses. The Equation 2.5 shows the expression when the UWB pulse is composed of multiple (2N) impulses.

$$p(t) = \sum_{i=1}^{N} A_i [(2mod(i,2) - 1) \\ [exp(-\frac{(t - (2i - 1)T_D)^2}{2T_W^2}) - Aexp(-\frac{(t + (2i - 1)T_D)^2}{2T_W^2})]]$$
(2.5)

The Equation 2.6 shows the frequency domain expression of the UWB pulse from Equation 2.5 in the time domain.

$$P(f) = \sum_{i=1}^{N} A_i [(2mod(i,2)-1)T_W]$$
  

$$\sqrt{2\pi}exp(-\frac{(2\pi fT_W)^2}{2})(exp(-i2\pi fT_D) + exp(-i2\pi f(-T_D)))$$
  

$$= \sum_{i=1}^{N} 2A_i [(2mod(i,2)-1)T_W\sqrt{2\pi}exp(-\frac{(2\pi fT_W)^2}{2})(cos(2\pi f(2i-1)T_D)))$$
  
(2.6)

The center frequency, the bandwidth and the amplitude of the sidelobes can be controlled by changing the impulse width  $T_W$ , the distance between the pulses  $T_D$ , the number of impulses, N, and the amplitude of each impulse,  $A_N$ . The following discussion shows the steps taken to derive the pulses which meet the FCC requirements. We start from the first-order Gaussian pulse and increase the number of impulses with the amplitude constant for each impulse. Then we change the amplitude of each impulse to decrease the amplitude of the sidelobes. By adding more impulses, we



Figure 2.5: IR-UWB pulse in time domain and frequency domain for  $T_W = 140$  ps, N = 2,  $A_N = [-0.5, 0.5]$ .

achieve pulses with narrower bandwidth. By changing the distance between the impulses and the width of the impulses, we change the center frequency of the UWB pulse. The results give first-hand calculation results for circuit designs in the following chapters.

The pulse design is started with the simple first-order Gaussian monopulse. To make the analysis simple and decrease the number of tunable parameters, we assume that  $T_W = T_D$ . Fig. 2.5 shows the time domain and frequency domain representations of the IR-UWB pulse with  $T_W = 140$  ps, N = 2,  $A_N = [-0.5, 0.5]$ . It is shown that the pulse frequency spectrum violates the FCC mask. Two observations should be noted. First, if the output voltage amplitude is very small or the PRF is very low, it is possible that the IR-UWB pulse with two impulses meets the FCC mask because the PSD could be even lower than the spectrum notch between the 960 MHz and 1.6 GHz. In chapter 5, the IR-UWB pulse with only two impulses is used because the on-chip antenna has a very low gain (< -30 dB) and the data rate is very low (< 2 kbps). Second, monopulse UWB has a large DC spectrum component and it is mostly for UWB design below 960 MHz. Due to the differentiation function of the antenna, the monopulse will become a pulse with two impulses when it is transmitted into the air.



Figure 2.6: IR-UWB pulse in time domain and frequency domain for  $T_W = 80 \text{ ps}, N = 2, A_N = [-0.5, 0.5].$ 



Figure 2.7: IR-UWB pulse in time domain and frequency domain for  $T_W = 80$  ps, N=4,  $A_N = [0.5, -0.5, 0.5, -0.5]$ .

As a result one IR-UWB pulse is at least composed of two impulses.

Fig. 2.6 shows the time domain and frequency domain representations of the IR-UWB pulse with  $T_W = 80$  ps, N = 2,  $A_N = [-0.5, 0.5]$ . It is shown that the bandwidth of the IR-UWB is larger and the center frequency is higher compared with those in Fig. 2.5. The frequency spectrum still violates the FCC mask between the 960 MHz and 1.6 GHz. In order to fit the IR-UWB pulse into the FCC mask, one method is to include more impulses with tunable impulse amplitude. Another method is to reduce



Figure 2.8: IR-UWB pulse in time domain and frequency domain for  $T_W = 80$  ps, N=4,  $A_N = [0.2, -0.5, 0.5, -0.2]$ .

the PRF and decrease the voltage amplitude.

In order to make the UWB pulse spectrum compliant with the FCC mask, first we add two impulses to reduce the bandwidth and the sidelobes appear. Fig. 2.7 shows the the time domain and frequency domain representations of the IR-UWB pulse with  $T_W = 80$  ps, N=4,  $A_N = [0.5, -0.5, 0.5, -0.5]$ . The four impulses are of the same amplitude. It is noted that the sidelobes have too much power that the spectrum still violates the FCC mask. The pulse is equivalent to a sinusoidal wave multiplied by a square mask in the time domain. In the frequency domain, the PSD is in the forms of a sinc function, which has very large sidelobes. In order to reduce the amplitude of the sidelobes, the mask should be changed, which indicates the amplitude of the 1<sup>st</sup> and 4<sup>th</sup> impulses should be different from those of the 2<sup>nd</sup> and 3<sup>rd</sup> impulses.

Next we tune the amplitudes of the 1<sup>st</sup> and 4<sup>th</sup> impulses to be smaller than those of the 2<sup>nd</sup> and the 3<sup>rd</sup> impulses. Fig. 2.8 shows the the time domain and frequency domain representations of the IR-UWB pulse with  $T_W = 80$  ps, N=4,  $A_N = [0.2, -0.5, 0.5, -0.2]$ . It is shown that the spectrum



Figure 2.9: IR-UWB pulse in time domain and frequency domain for  $T_W = 80$  ps, N = 20,  $A_N = [0.01, -0.12, 0.23, -0.34, 0.45, -0.56, 0.67, -0.78, 0.89, -1, 1, -0.89, 0.78, -0.67, 0.56, -0.45, 0.34, -0.23, 0.12, -0.01].$ 



Figure 2.10: IR-UWB pulse in time domain and frequency domain for  $T_W = 160$  ps, N=2,  $A_N = [0.01, -0.12, 0.23, -0.34, 0.45, -0.56, 0.67, -0.78, 0.89, -1, 1, -0.89, 0.78, -0.67, 0.56, -0.45, 0.34, -0.23, 0.12, -0.01].$ 

of the IR-UWB pulse complies with the FCC regulation. The -10 dB bandwidth is about 6 GHz (3 GHz to 9 GHz) and the center frequency is about 5.8 GHz.

The full UWB band (3.1-10.6 GHz) is usually divided into low band (3.1-5 GHz) and high band (6-10 GHz). In order to make the UWB pulse fit into either one of the low band or high band, more impulses are required. Fig. 2.9 shows the the time domain and frequency domain representations of the IR-UWB pulse with  $T_W$ = 160 ps, N=20,  $A_N$ =[ 0.01, -0.12, 0.23, -0.34, 0.45, -0.56, 0.67, -0.78, 0.89, -1,1, -0.89, 0.78, -0.67, 0.56, -0.45, 0.34, -0.23, 0.12, -0.01]. The UWB signal is in the low band and the center frequency is about 4 GHz. Fig. 2.10 shows the the time domain and frequency domain representations of the IR-UWB pulse with  $T_W$ = 80 ps, N=20,  $A_N$ =[0.01, -0.12, 0.23, -0.34, 0.45, -0.56, 0.67, -0.78, 0.89, -1,1, -0.89, 0.78, -0.67, 0.56, -0.45, 0.34, -0.23, 0.12, -0.01]. The UWB signal is in the high band and the center frequency is about 7 GHz.

# Chapter 3

# Mostly Digital Low Power Inductorless IR-UWB Transceiver in 65 nm CMOS process

#### **3.1** Design Considerations and Goals

Low power consumption is the foremost objective in IR-UWB transceiver design for portable and implantable biomedical applications. The power consumption is usually constrained by battery size and battery replacement intervals. The energy efficiency of the IR-UWB transmitter has been greatly improved by techniques such as aggressive duty-cycling with mostly or all-digital designs [41, 42, 52]. The challenges lie more in the receiver. As introduced in previous chapters, compared with

the coherent receiver [14, 28], the non-coherent IR-UWB receiver reduces the circuit complexity and power consumption of the radio front-end [13, 15, 29–31]. However, the simplicity of the radio front-end is penalized by the complex demodulation and synchronization in digital baseband [32]. Synchronized-OOK (S-OOK) modulation was proposed in [29] to achieve low-power timing synchronization and data reception. In [29], an on-chip ring oscillator generates the receiver clock, whose frequency is fixed and prone to process variations. In this work, we eliminate the use of the on-chip or off-chip clock generator and the data is recovered by self-synchronization. The simple demodulator and synchronizer are composed of only digital gates, which helps achieve low power consumption, high energy efficiency and small chip area.

Cost reduction by minimizing the chip area is important when system integration of the radio transceiver with sensor front-end and DSP is considered. Use of off-chip components should also be avoided for system cost reduction. Most of the reported CMOS IR-UWB receivers extensively use monolithic inductors or off-chip inductors and/or capacitors to improve the input matching and enhance the gain bandwidth [13, 30]. These works mostly target stand-alone UWB transceiver systems. Cost reduction and integrating the transceiver with other circuit blocks are not of their interests. On-chip passive components occupy a large chip area and make **SOC!** (**SOC!**) implementations costly. To reduce the cost, completely inductorless designs are implemented for both the transmitter and the receiver in this work and the circuit area is minimized. Off-chip inductor and capacitors are not used for input matching or output filtering so the number of PCB components is reduced.

The non-coherent IR-UWB CMOS transceiver has been intensively used in short-range data communication. Its use in radar sensors for contact-less vital sign monitoring also attracts attention. CMOS IR-UWB radars were reported in [17, 60, 65, 66]. In correlation-based receivers [65], the distortion of the received pulses affects matching between received pulse and template. The ultra-high sampling frequency and interleaving architecture in [17] require a large chip area and high power consumption. Equivalent time sampling technique reduces the absolute sampling frequency [60]. Challenges for equivalent time sampling exist in precisely controlling the small time shift which is the inverse of the equivalent sampling frequency. Threshold sampler based radar utilizes continuous-time signal processing in [66]. The radio front-end in [66] is not optimized for power and input impedance matching. In this work, we verify the feasibility of applying the non-coherent IR-UWB transceiver for short-range vital-sign detection. The radio front-end is optimized for performance and cost. Real-time sensing of human respiration is achieved.

The following sections will detail the system architecture and circuit implementation of the proposed IR-UWB transceiver. The use of power-consuming RF or analog parts should be minimized or avoided. The reliable wireless transmission distance is designed to be about one meter. Biomedical applications such as ECG with a smaller number of channels usually require medium or low-data-rate rate communication; e.g. several hundred bps to several hundred kbps. The Analog-to-digital Converter (ADC) after the sensor front-end usually generates outputs of multiple bits for each channel. For example, in an ECG sensor, a 10-bit ADC is running at 30ksample/s [26]. An EEG sensor contains a 10-bit ADC running at 10ksample/s [67]. We also consider turning on and off the transceiver by duty cycling to reduce power. 1-10 Mbps is a reasonable choice considering the memory requirement in duty cycled transmitter and circuit complexity. As a result, a data rate of 1-10 Mbps is chosen in our design. Under the low-data-rate condition, the power and cost of the transceiver should be minimized, and the reconfigurability requirement should be addressed.



(a)



(b)

Figure 3.1: System architecture of IR-UWB system (a) short-range communication (b) radar sensor.

#### **3.2** System architecture

The proposed IR-UWB system is configurable for both short-range communication and radar sensing. The system architecture is shown in 3.1, where Fig. 3.1(a) represents the communication mode and Fig. Fig. 3.1(b) represents the radar sensing mode. All-digital implementation is adopted for transmitter design to improve the energy efficiency. An active-inductor-based Low-noise Amplifier (LNA) is proposed in the receiver for better wideband matching and reduced area. Non-coherent pulse detector downconverts the IR-UWB pulses to baseband. The difference between the communication mode and radar mode is in the In the communication mode, S-OOK modulator and demodulator. modulation and demodulation are performed. In the radar mode, there is no modulation and a train of IR-UWB pulses with a fixed repetition rate is transmitted and received. This is realized simply by setting all the input symbols as '0's in the S-OOK modulator. The time interval between the transmitted and received pulses is measured to determine the distance between the radar sensor and the detected object.

#### 3.3 Link budget

The link budget calculation for the short-range IR-UWB signal transmission is summarized in Table 3.1. The IR-UWB signal is pulse-based and the link budget can be calculated in terms of transmitted and received pulse energy [31]. IR-UWB signal covers a bandwidth of several hundreds of MHz or several GHz. It is difficult to calculate the pulse energy by integrating the PSD across the ultra-wide signal

bandwidth since the PSD at each specific frequency could not be accurately modelled or calculated. The transmitted pulse energy is thus estimated by circuit simulation. Based on the time-domain simulation waveform of the transmitter output, the transmitted pulse energy is estimated as:

$$E_{pTX} = 2 \ pJ \tag{3.1}$$

In the communication mode, the transceiver is to support the link between the wireless sensors and the Central Control Unit (CCU) as shown in Fig. 1.1(a). The transmission distance is 1 m or less. The path loss is calculated as 50 dB according to the channel model in [68].

$$PL = 50 \ dB \tag{3.2}$$

To achieve a total error rate of  $10^{-3}$  in the S-OOK modulation, it is shown that the required  $E_b/N_0$  is 18 dB [69]. The calculation is based on math model and it is validated by CMOS prototype measurements.

$$\frac{E_b}{N_0} = 18 \ dB \tag{3.3}$$

The noise figure of the non-coherent receiver is as high as 20 dB due to the receiver's nonlinear nature [31]. The nonlinearity of the non-coherent receiver generates at least 6-dB degradation on signal-to-noise ratio even the circuit is noiseless. Noise further increases by adding the amplifier noise and detector noise.

$$NF = 20 \ dB \tag{3.4}$$

The minimum required receiver input pulse energy can be calculated from the  $E_b/N_0$  and noise figure. The thermal noise floor is  $N_{th} = -174 dBm/Hz$ .

$$E_{pRX} = N_{th} \cdot NF \cdot \frac{E_b}{N_0} = 20 \ aJ \tag{3.5}$$

Assuming antenna gain as 3 dB and implementation loss as 3 dB. The link margin can be calculated as

$$M = 10\log_{10}(E_{pTX}/E_{pRX}) - PL - IL + 2G_a = 3 \ dB \tag{3.6}$$

The link budget calculation for communication mode is shown in Table 3.1. In the radar sensor mode, the transceiver is placed not far from the human body as shown in Fig. 1.1(b). Large-size antennas

	Symbol	Value	Unit
Transmit Pulse Energy	$E_{pTX}$	2	pJ
Antenna Gain	$G_a$	3	dB
Path Loss	PL	50	dB
Implementation Loss	IL	3	dB
Noise Figure	NF	20	dB
$E_b/N_{RX}$	$E_{pRX}/N_0$	18	dB
Min Received Pulse Energy	$E_{pRX}$	20	aJ
Link Margin <sup>1</sup>	M	3	dB

Table 3.1: Link Budget Calculation

<sup>1</sup>  $M = 10 log_{10}(E_{pTX}/E_{pRX}) - PL - IL + 2G_a (dB)$ 

with directional gain of 10 dB are used, and the signal propagation is line-of-sight (LOS). In this configuration, the signal can be received at a longer distance than in communication mode. The calculation predicts that the non-coherent receiver with a relatively simple system architecture is capable of supporting short-range IR-UWB signal transmission and detection.

#### 3.4 Transmitter Design

Both analog and digital approaches have been applied in generating the IR-UWB pulses. The analog approaches use up-conversion [48] or DAC direct synthesis [47]. However, the large power consumption is not suitable for low-power biomedical applications. Compared with the analog counterparts, all-digital IR-UWB transmitter is built from digital gates which consumes low power and provides good energy efficiency. One digital method avoids up-conversion by passively filtering a narrow pulse using an on-chip bandpass filter [46]. The shortcomings of using integrated



<del>4</del>

2

DATA

A<0:15>

F<0:9>

<sup>رة</sup> ب

Modulator

CLOCK DATA ĵ0

40

C

Figure 3.2: Schematic of the IR-UWB transmitter.

bandpass filters include a large chip area and a hardly tunable circuit. The IR-UWB transmitter in this work exploits direct edge combining technique to synthesize the output waveform [48,52]. There is no on-chip inductor so the area is minimized.

The circuit of the transmitter is shown in Fig. 3.2. The S-OOK waveform is produced by the modulator. One pilot pulse and one data pulse are generated by the modulator if the input non-return-to-zero (NRZ) data is '1'. Only the pilot pulse but no data pulse is present if the data is '0'. The modulator is composed of all-digital gates and the data pulse lags the pilot pulse by 5 ns. The modulated pulses then propagate into the variable delay line which produces rising and falling edges with small delays between them. The delay line is composed of current-starved asymmetric inverters whose delays are controlled by a 10-bit digital word. The asymmetric inverter architecture suppresses the undesirable glitches and improves the rise/fall time [70]. The edges are then combined by logic AND and OR gates to generate the negative and positive impulses. 16-bit amplitude tuning (4 bit for each impulse) controls the number of active AND and OR gates. The impulses drive the Digital Power Amplifiers (DPAs) and the dual capacitively-coupled structure with precharge transistors helps to reduce the low frequency components [41, 52]. The precharge transistors are self-controlled by the first and last propagating edges  $V_{0m}$ ,  $V_{6m}$ ,  $V_{0p}$ ,  $V_{6p}$  using simple combination logic gates.

The power consumption is divided into active power and leakage power. When the data rate is low, leakage power consumed by the digital gates significantly degrades the power efficiency when the transmitter is in idle state. Optimal sizing of the transistors starts from the output drivers. The transistors of the output drivers are sized to be just large enough to provide 0.8 V output swing to the antenna. Then the AND and OR gates



Figure 3.3: Simulation results of transmitter in (a) time domain (b) frequency domain.

are sized followed by the interstage buffers and the delay cells. Transistors at each stage are sized just large enough to drive the later stages with acceptable delay and rise/fall time.

On-chip decoupling capacitors are added to reduce the supply voltage ripple. The parasitics of bondpads, Electrostatic Discharge (ESD) devices and bondwires are modelled and included in the simulation. In this design, the transmitter generates a IR-UWB signal that covers 3.1-8 GHz. The simulated pulse peak-to-peak amplitude is about 0.8 V, as shown in Fig. 3.3.

### 3.5 Receiver Design

The IR-UWB receiver includes an active-inductor-based wideband LNA, a pulse detector and a demodulator and synchronizer.



Figure 3.4: Schematic of the active-inductor-based wideband LNA.

## 3.5.1 Active-inductor-based Self-biased Wideband LNA

Various techniques have been proposed to achieve wideband input matching and gain in LNAs. A bandpass-filter-based, inductively degenerated Common-source (CS) LNA was introduced in [71]. The large number of on-chip inductors and capacitors require a large chip area. The Common-gate (CG) LNA was widely used due to its superior broadband input matching and better linearity performance [72]. In the CG LNAs, the input capacitance degrades the input matching significantly when the operating frequency increases to several GHz. The total input capacitance includes the gate-source capacitance of the input transistor and other parasitic capacitance including those from the package and ESD devices. An inductor is usually introduced to form a resonant network and neutralize the input capacitance. In this work, a novel active-inductor-based input matching technique for CG LNA is intoduced. The on-chip passive inductor is replaced by an active inductor which is composed of  $M_1$  and  $R_F$ . The output of the first stage of the LNA is connected to the gate of  $M_1$  through a resistor  $R_F$ , as shown in Fig. 3.4. Simple circuit analysis shows that the input admittance can be expressed as:

$$G_{in} = g_{m1}g_{m2}R_{L1}\frac{1/(j\omega C_{gs1})}{1/(j\omega C_{gs1}) + R_F} + j\omega C_t + g_{m2}$$

$$= \frac{g_{m1}g_{m2}R_{L1}}{1 + \omega^2 C_{gs1}R_F} + g_{m2} - j\omega \frac{C_{gs1}R_F}{1 + \omega^2 C_{gs1}R_F} + j\omega C_t$$
(3.7)

It is obvious in (3.7) that the active inductor introduces a negative susceptance which cancels the positive susceptance of the total input capacitance  $C_t$ . The second stage of the LNA is a cascode CS stage for gain boosting. The third stage is a CS stage with an active-inductor load for bandwidth extension [73, 74]. The multi-stage LNA topology provides sufficient gain and good input matching over very wide bandwidth. The LNA is designed to work with a 1 V power supply and is self-biased without the need of biasing circuit.

The noise factor of the active-inductor-based LNA is estimated as the equation below.

$$F = 1 + \frac{\gamma_2}{g_{m2}R_S} + \gamma_1 g_{m1}R_S + \frac{(R_L + R_F)}{R_S(1 + g_{m2}R_{L1})^2}$$
(3.8)

 $R_S$  is the 50  $\Omega$  source impedance. The  $\gamma_1$  and  $\gamma_2$  are channel noise coefficients. Note that a larger  $R_F$  results in larger negative suspectance



Figure 3.5: Simulation results of the LNA. (a) Simulated  $|S_{11}|$ . (b) Simulated voltage gain and noise figure.

but increased noise factor. The value of the  $R_F$  is chosen by trade-off between input matching bandwidth and noise factor. The second term is introduced by the active-inductor transistor,  $M_1$ . Iterative simulations make sure this additional noise does not increase the total noise factor significantly. Simulation results of the designed LNA are shown in Fig. 3.5. The simulation includes the parasitic effects from ESD protection devices, bondpads and package. It is shown that good wideband input matching is achieved from 3.1 GHz to 8 GHz. The simulated voltage gain is from 23 dB to 25 dB and the simulated NF is from 5 to 7 dB within the band of interest. Simulation shows that 20 dB gain is required to amplify the input voltage to about 50 mV which can trigger the pulse detector properly. Comparison of simulation results with and without active-inductor input matching is shown in Fig 3.6. The input reflection coefficient comparison shows that the input matching with active inductor is improved significantly at higher frequency. The gain of the active-inductor LNA is also higher at above 5 GHz. Due to the feedback resistor, the noise figure degrades for active-inductor-based LNA. The degradation is less than 2 dB.



Figure 3.6: Simulation results of the LNA with and without activeinductor-based input matching

#### 3.5.2 Pulse Detector

In traditional non-coherent IR-UWB receivers, a self-mixer or squarer is used to downconvert the IR-UWB signal [29,31]. The baseband signal is then amplified by a baseband gain amplifier or integrated by an integrator. An ADC or a comparator finally generates the digital output. These approaches are relatively high-power and complex in circuitry. In [75,76], CS amplifier, utilizing the non-linear relationship between the drain current and the gate voltage, was used as a Pulse Detector (PD). Designed for millimeter wave systems, these PDs used resistor or inductor as load for wider bandwidth application. In this work, a PD used is shown in Fig. 3.8. In this design, the resistor load is replaced with a separately biased PMOS



Figure 3.7: Pulse detector. (a) Schematic of the PD. (b) Mechanism of pulse detection

transistor to achieve a high conversion gain. As shown in Fig. 3.8(b), when biased near the subthreshold region, the nonlinear I-V relationship of the NMOS transistor generates the baseband signal. The positive impulses are amplified more than the negative impulses. The input NMOS transistor is biased in the subthreshold region and consumes little power when no pulse is received. The input NMOS is sized as  $30\mu m/60nm$  to maximize the gain. The PMOS load is not sized with minimum length  $(4\mu m/600 nm)$ to increase the output impedance. The gate bias of the PMOS load is tuned to achieve better gain and set the output level. Three stages of asymmetrically-sized inverters amplify the baseband signal to full scale. The sizes of the inverter chain transistors are shown in Fig. 3.8 (a). The sizes are chosen based on simulation results. If the PMOS is much larger than NMOS, the inverter pulls up the rectified pulse. If the NMOS is much larger than the PMOS, the inverter pulls down the rectified pulse. The sizes of the inverters are chosen as  $4\mu m/600$  nm,  $4\mu m/600$  nm and  $4\mu m/600$  nm, based on the simulation. The buffer then further rectifies the baseband signal and produces the digital output pulses. The PD consumes only 80  $\mu W$  when the data rate is 10 Mbps.

Fig. ?? shows the simulation performance of the combined LNA and PD. The y axis shows the input power level of LNA when the output of PD shows errors. Time-domain simulation of thousands of symbols is difficult and we report the input power level when there is one or more



Figure 3.8: Receiver input power level vs frequency (BER  $\geq 10^{-1}$ )

errors shown every ten symbols. This estimation is acceptable because both theoretical analysis [] and measurement results in the following sections show a sharp drop of BER with decrease input power level. Possible reasons of transmission quality degradation may include more parasitic effects and less effective input matching.

#### 3.5.3 Demodulation and Synchronization

Synchronization of the IR-UWB received pulses are challenging. In [32], DLL is using to align the sampling clock with the pulses. The area is large and the power consumption is high. It requires a 32 MHz external reference. In [33], complex baseband circuit is composed of many analog circuits and the power is high. In [29], S-OOK synchronization is applied and ring oscillator is used for generating time reference for the synchronization circuit block.



Figure 3.9: (a) Schematic of the demodulator. (b) Timing diagram of demodulation and synchronization.

In S-OOK, one symbol is composed of two pulses, namely the pilot pulse and the data pulse. The pilot pulse indicates the start of one symbol and the data pulse carries the data. In this work, the stretched pilot pulse, as the reference clock, latches the stretched data pulse to produce the NRZ data output. The circuit of demodulator and synchronizer is shown in Fig. 3.9 (a) and the timing diagram of the demodulation and self-synchronization is shown in Fig. 3.9 (b).

The baseband pulse generated by the pulse detector is expanded by two Pulse Stretching Circuits (PSC). PSC A expands both the pilot pulse and the data pulse (if there is one data pulse) to the width of  $T_1$ . PSC B only expands the pilot pulse since the stretched pulse width  $T_2$  is larger than the delay between the pilot pulse and data pulse. The output of the PSC B is used as the reference clock. The output of PSC A is latched by this reference clock using a D Flip-Flop (DFF).  $T_2$  is tuned by four binary bits ( $B_0$ - $B_3$ ) so that the falling edge of the reference clock can latch the stretched data pulse if the symbol is '1'. When the symbol is '0', there is no data pulse and the output of the DFF is low.

The output data is in NRZ format. Only 13 logic elements (3 DFFs and 10 combinational gates) are used in the demodulator and synchronizer. This is much simpler than [69] which includes 61 logic elements (16 flip-flops and 45 combinational gates). No on-chip or off-chip clock source is required for the receiver.

#### **3.6** Measurement Result

The test chip is fabricated in a 65 nm digital CMOS 1P6M process. The chip is packaged in a standard QFN40 package and mounted on Rogers



Figure 3.10: Micrograph of the chip.

4003 PCB for testing. The die micrograph is shown in Fig. 3.10. The measurements were taken with a Tektronix DPO71254 Digital Oscilloscope, an Agilent E4407b spectrum analyzer and an 8753ES S-Parameter Network Analyzer.

#### 3.6.1 Transmitter

The measured time-domain transmitter output is shown in Fig. 3.11(a). The output peak-to-peak voltage amplitude is 0.75 V. The power consumption is 216  $\mu$ W at 10 Mbps and the Figure of merit (FOM) of energy per bit is 21.6 pJ/bit. The spectrum of the transmitted pulse is shown in Fig. 3.11(b) and is compliant with FCC regulations. The transmitter can support up to 80 Mbps data transmission.





Figure 3.11: Transmitter output in (a) time domain (b) frequency domain.


Figure 3.12: Simulated and measured  $|S_{11}|$ .

#### 3.6.2 Active-inductor-based Wideband LNA

The simulated and measured input  $|S_{11}|$  are shown in Fig. 3.12. The measured  $|S_{11}|$  is below -9.5 dB from 3.1-7.8 GHz. The  $|S_{11}|$  is measured on the packaged chip which is mounted on PCB. Good input matching is achieved across a very wide band despite the parasitic effects from bondpads, package, routing trace and connector. This shows the effectiveness of the proposed active-inductor-based matching technique. The DC current of the LNA is 6.3 mA from a 1 V power supply.

#### 3.6.3 Short-range Communication Mode

Fig. 3.13(a) shows the block diagram of the measurement setup for the communication mode. A variable attenuator is used for the Bit Error



(a)



Figure 3.13: Measurement setup for communication mode. (a) Block diagram of the test setup. (b) LOS free space test environment.



Figure 3.14: (a)Transmitted and received NRZ data, (b)BER versus input power.

Rate (BER) test. The free space LOS test is shown in Fig. 3.13(b). The transmitted and received data are captured by an oscilloscope and shown in Fig. 3.14 (a). Note that the output data is in NRZ format which can be directly processed by a baseband processor. The plot of BER versus the receiver input power is shown in Fig. 3.14 (b). The input sensitivity is -64 dBm for a BER of  $10^{-3}$  when the data rate is 10 Mbps.

#### 3.6.4 Radar mode - Respiratory rate measurement

The setup for measuring the human respiration using the radar mode is shown in Fig. 3.15. Directional antennas with 10 dB gain are used to increase the transmission gain. The input of the modulator is '0' so that an IR-UWB pulse train composed of only pilot pulses is sent to the human body. The digital output of the receiver is sampled and recorded by a Tektronix DPO 71254 oscilloscope. The frame sample rate is 3 Hz and the time resolution is 4 ps. The Time of Flight (ToF) between the transmitted and received pulse changes with the chest movement. The ToF is calculated and converted to the displacement by a computer program. The displacement of the chest versus time during normal and







Figure 3.15: Measurement setup for radar sensor mode. (a) Block diagram of the test setup (b) Test environment for measuring human respiration.



Figure 3.16: Respiration measurement (a) normal respiration in the time domain (b) normal respiration in the frequency domain.



Figure 3.17: Respiration measurement (a) fast respiration in the time domain (b) fast respiration in the frequency domain.

fast respiration is shown in Fig. 3.16(a) and Fig. 3.16(b). Fourier transformation reveals the respiratory rate as shown in Fig. 3.16(c) and Fig. 3.16(d). The respiration frequency is 0.25 Hz for normal respiration and 0.65 Hz for fast respiration. Fig. 3.18 shows one case of real-time human respiration monitoring. For the first 45 seconds, normal respiration is detected. The breath is then halted at the 45th second and is resumed after 20 seconds. Since the breath was held for 20 seconds, the respiratory rate is faster than normal when resumed.



Figure 3.18: Human respiration changes from normal respiration to held respiration to resumed respiration.

## 3.7 Tranceiver Front-end Performance Comparison

Table 3.2 shows the performance of the presented transmitter and several previous publications. Three Figures of Merit (FOMs) are compared. The first FOM is the widely-used DC energy per pulse  $E_{dTX}$ , which is the total DC power consumption divided by the pulse rate. The second FOM is the transmission efficiency, which is defined as the ratio of transmitted pulse energy  $E_{pTX}$  to  $E_{dTX}$  [31]. The efficiency is important since the transmitted pulse energy is closely related to the communication range in the non-coherent IR-UWB transceiver. However, the  $E_{pTX}$  is difficult to measure and is usually estimated from the time domain waveform or the power spectrum of the pulse. The transmission efficiency of the IR-UWB transmitter is usually below 10% [31, 52]. The third FOM is the energy per pulse normalized to output voltage amplitude  $E_{dTX}/V_{pp}$ , which was introduced in [46]. The energy per pulse  $E_{dTX}$  of this work is 21.6 pJ/pulse, which is better than or comparable to state-of-the-art works. The presented transmitter features an efficiency of 7.5%, which is the same as [52] and higher than the others. The pulse energy normalized to the output voltage amplitude is 27 pJ/V. The transmitter in this work only occupies an area of 0.03 mm<sup>2</sup>, as shown from the die photo in Fig. 3.10.

In [46], multiple on-chip inductors are used and the output voltage is boosted to be large. The design lacks the tunability and the area is very large. In [31], on-chip transformer is used as the load of the oscillator and different output increase the output swing to be 2.2 V. The power efficiency is partially limited by the power consumed to generator the ramping mask signal. [29], the pulse shaping is achieved by increase the pulse duration and the energy per pulse is large. All the three design above use one or multiple on-chip inductors and the area is large.

Table 3.3 compares the designed IR-UWB receiver with other designs. Because of the simple demodulation and synchronization circuit, our receiver achieves an energy per bit of 0.64 nJ/bit, which is lower than other references. The sensitivity of the receiver is measured as -64 dBm at 10 Mbps, which allows a reliable wireless data link for short distance. The total area of the designed receiver is only 0.01 mm<sup>2</sup>, which includes both the radio front-end and the demodulator (Fig. 3.10).

In [30], the power consumption is not reported and the die area is large. In [15], the power consumption is large because of the complex synchronization circuits. In [15,29,31], the the area is large due to the use of on-chip inductors.

This work		65	3.1-8	0.75	10	21.6	1.6		7.5	97	3	0.03
JSSC'12	[52]	130	3.1-5	0.6	10	20	1.5		7.5	33		0.13
JSSC'11	[29]	00	2.9 - 3.8	0.61	10	83	1.9		2.4	136	100	0.6
JSSC'11	[31]	130	7.25-8.5	2.2	5	186	13.2		7	03	0	0.23
TMTT'10	[46]	130	3.1-10	1.42	100	38.4	1.9		5	27		0.54
		Technology (nm)	Frequency Band (GHz)	Output Amplitude $V_{pp}$ (V)	Data Rate (Mbps)	Energy per pulse $E_{dTX}$ (pJ)	Transmitted Pulse Energy	$E_{pTX}$ (pJ)	Efficiency $E_{pTX}/E_{dTX}$ (%)	Normalized energy per pulse <sup>1</sup>	$E_{dTX}/V_{pp}~({ m pJ/V})$	Die Area $(mm^2)$

 Table 3.2: Transmitter Performance Comparison (I)

 $^1\mathrm{The}$  energy per pulse normalized to output voltage amplitude

This month	This work		3-8	10	6.4	0.64	-64	-84	0.01
JSSC'11	[29]	06	3.6 - 4.3		2.18	2.18	-66	-76	0.36
JSSC'11	[31]	130	7.25-8.5	ũ	4.2	0.84	-70	-87	0.45
JSSC'10	[15]	00	3.1-5	16	22.5	1.4	-76	-98	4.5
ISSCC'10	[30]	180	3.1-5	1	I	5.3	-82	-92	2
		Technology (nm)	Frequency Band (GHz)	Data Rate (Mbps)	Power Consumption (mW)	Energy per bit (nJ/bit)	Sensitivity for $10^{-3}$ BER (dBm)	Sensitivity for $10^{-3}$ BER scaled to $100 \text{ kb/s}$ (dBm)	Die Area $(mm^2)$

Table 3.3: Receiver Performance Comparison (I)

### Chapter 4

# A Low-power Low-leakage IR-UWB Transmitter and an IR-UWB Receiver with a Coarse-fine TDC in 130-nm CMOS process

In this chapter, design of a low-power energy-efficient IR-UWB transmitter and an IR-UWB Receiver with coarse-fine Time-to-digital Converter (TDC) are introduced. In the IR-UWB transmitter, a Digitally-controlled Oscillator (DCO) generates the carrier frequency and a True Single-Phase Clocking (TSPC) mask generator generates the pulse mask. The oscillator output and pulse mask are then combined using a cascode output driver stage with an on-chip inductor load. The main goal of the design is to reduce the static leakage power consumption while

maximizing the output swing and transmit efficiency. In the IR-UWB receiver, the input IR-UWB is first detected and digitized. The distance between the radar and the object is measured by digitizing the travel time between the transmitted pulse and received pulse using a coarse-fine TDC.

In section 4.1, the design considerations and goals will be discussed. Section 4.2 will introduce the proposed IR-UWB transmitter architecture, circuit and measurement results. Section 4.3 demonstrates the design of the IR-UWB receiver with a coarse-fine TDC.

### 4.1 Design Considerations and Goals

### 4.1.1 Energy-efficient IR-UWB Transmitter with Low Stand-by Leakage

The most important metric in comparing different IR-UWB transmitters is the DC energy consumed for transmitting one pulse, i.e., the energy per pulse. As introduced in Chapter 3, the transmitted pulse energy and transmitter output voltage amplitude are also important for successful establishment of a communication link. Maximizing transmitted pulse energy and transmitter output voltage amplitude under certain DC energy per transmitted pulse are important design considerations. Another important design goal is to minimize the leakage power consumption of the IR-UWB transmitter in idle state. In some biomedical applications such as ECG sensor, the raw data of the sensor frontend and ADC is quite low. In case of a low-power ECG front-end with a Level-crossing (LC) asynchronous ADC [77], the output data pulse rate from the ADC is below

2 kbps. Under the condition of this low data rate input, the active power of the IR-UWB is comparable with, or even less than, the leakage power. Note that the output driver transistors of the transmitter are designed to be quite large to be able to drive the normally 50  $\Omega$  antenna impedance and the leakage power is significant and almost constant. For example, a pair of PMOS( $300\mu$ m/130nm) and NMOS ( $150\mu$ m/130nm) in 130nm CMOS process burns a leakage current of 600 nA when the gates are off. For a pair of PMOS( $60\mu$ m/60nm) and NMOS ( $30\mu$ m/60nm) in 60nm CMOS process, the leakage current when the gates are off is about 1.2uA. We wish to minimize the leakage current in applications such as portable or implantable biomedical sensors since charging the battery could be difficult or impossible. In this design of the IR-UWB transmitter, the design goals are minimizing the leakage power, reducing the DC energy consumption per pulse and increasing the transmitted pulse efficiency.

The area limitation is not of importance and the process changed to Global Foundry 130 nm process, which to the author's understanding is not optimized for analog and RF applications. This 130 nm process features a worse high-frequency performance. The active-inductor approach is difficult to achieve wideband input matching and gain.

#### 4.1.2 IR-UWB Receiver with TDC

In Chapter 3, we demonstrated the feasibility of applying a non-coherent IR-UWB transceiver in sensing human's respiration. The time interval measurement was performed by an ultra-high-sampling-rate oscilloscope. The complete integrated radar SOC should include an on-chip time interval measurement circuit. Recent progressive technology scaling



Figure 4.1: Architecutre of the IR-UWB radar with time-to-digital converter.

provides CMOS gates with smaller timing delays and TDC with very high time resolutions have been reported.

The continuing work from this thesis is integrating a high-resolution, high-dynamic-range TDC with the IR-UWB transceiver. The system architecture is proposed as shown in Fig. 4.1. The difference between Fig. 4.1 and Fig. 3.1(b) is that the time interval measurement unit (oscilloscope) is replaced by the TDC.

The measurement results in Chapter 3 only show the respiration rate. This is limited by the frame sampling rate provided by the oscilloscope, which is 3 samples per second. If TDC is integrated, the timing resolution should be about 6.7 ps (1 mm) if the heartbeat rate could be sensed. The dynamic range, however, is required to be large. Assuming that the distance between the radar and the object is as far as at least half a meter,



Figure 4.2: Architecture of the IR-UWB Transmitter.

the TDC full range is 6.7 ns (1 m). This requires a TDC with a dynamic range of 10 or more bits. Some of the reported TDCs are designed to replace the phase detector in Digital Phase-locked Loop (DPLL) for multi-GHz applications [78, 79]. In these TDCs, the time resolution can be high but the total range cannot meet radar requirements.

# 4.2 Energy-efficient IR-UWB Transmitter with Low Stand-by Leakage

#### 4.2.1 Transmitter Architecture

The system architecture of the transmitter is shown as in Figure. 4.2. The one-shot circuit generates a narrow pulse which is slightly wider than



Figure 4.3: Schematic of the one-shot circuit.

the IR-UWB pulse. This narrow pulse opens the mask generator and the DCO. When the output of the one-shot circuit is low, the DCO and the mask generator are shut down. The DCO is controlled by 12 digital bits. 4 thermometer bits serve as frequency coarse tuning which controls the load capacitor of each stage of the DCO. 8 binary bits control the biasing circuit of the DCO stage which serve as the fine frequency tuning. The mask generator uses a TSPC circuit to generate the mask which controls the shape of the IR-UWB pulse. The mask generator is controlled by eight digital bits. The final stage is a cascode amplifier with an inductor load. The cascode transistors are driven by the outputs of the DCO and the mask generator. The on-chip inductor, which resonates with the output capacitance, boosts the output voltage. The output pad and the bondwire parasitics (not shown in the schematic) are included in the simulation.



Figure 4.4: Schematic of digitally-controlled oscillator.

#### 4.2.2 Circuit Design

#### 4.2.2.1 One-shot Circuit

The one-shot circuit is shown in Fig. 4.3. The one-shot signal is generated by the combining the input signal with its delay version by a NAND gate. The delay is simulated to be 3 ns with some margin. The bandwidth of the IR-UWB signal is designed to be 400 MHz, which corresponds to a pulse width of 2.5 ns.

#### 4.2.2.2 Digital-controlled Oscillator

The DCO is shown in Fig. 4.4. The DCO are composed of two inverters and one NAND gate. The biasing current and load capacitance can be controlled by digital codes. The enable signal (EN) is controlled by the output of the one-shot circuit. Frequency tuning of the DCO is a function of the 4-bit thermometer-coded digital coarse words C<1:4>and 8-bit binary-coded digital fine words F<1:8>. 4-bit thermometer-coded digital coarse words control the load capacitance of each stage. 8-bit binary-coded digital fine words control the biasing current of the inverters and NAND gate.

#### 4.2.2.3 Mask Generator

The circuit of the TSPC mask generator is shown in Fig. ??. The timing diagram of the mask generator is shown in Fig. ??. Same as in the DCO, the EN signal is the output of the one-shot circuit. When the EN changes from low to high, the transition edge will propagate through the TSPC stages. A<1>, A<3>, A<5>, A<7>, A<13>, A<15>, A<17> and A<19> are then synthesized by digital gates to generate the mask. The four masks, Mask<1:4>, could be chosen from the multiplexer by M<1:4> to generate different mask combinations. The output of the mask generator drives the output driver stage.

ff

#### 4.2.2.4 Output Driver Stage

The output driver stage is composed of a cascode amplifier with an inductor load (Fig. 4.2). The driver is driven by the outputs of the DCO and the mask generator. The inductor is in resonance with the output capacitance to generate a large output voltage swing. The advantage of the stack of transistors is the reduced leakage current when outputs of both DCO and mask generator are low. The output driver stage needs to drive



Figure 4.5: Die micrograph of the IR-UWB transmitter

the antenna impedance which is 50  $\Omega$  and is usually very large. The circuits preceding the output driver stage, such as DCO and mask generator, are smaller and the leakage of the output driver stage is the most significant. Compared with the design in Chapter 3, an on-chip inductor is used. Half of the circuit area is occupied by the load inductor, but the output voltage swing is larger than in Chapter 3.

#### 4.2.3 Measurement Results and Comparison

The transmitter was fabricated using the GlobalFoundries 130-nm CMOS process and was directly wire-bonded to a FR4 PCB to minimize parasitic and reduce packaging cost. The die micrograph is shown in Fig. 4.5 and the core occupies an active area of 470  $\mu$ m × 310  $\mu$ m with a total area is 0.146 mm<sup>2</sup>. The measurements were taken with the Tektronix DPO71254 Digital Oscilloscope and the Rohde Schwarz ZVL13 Vector Network Analyzer.



Figure 4.6: Transmitter output in time domain.

#### 4.2.3.1 IR-UWB Pulse Measurement

The measurement of the transmitter reveals that it is capable of generating pulses up to a PRF of 140 Mpulses/s. The turn-on time is 2 ns due to the propagation delays from the I/O pad driver and the level shifter.

Fig. 4.6 shows a time-domain view of the IR-UWB pulse and the nominal measured pulse width is approximately 2.5 ns. The maximum output voltage swing is 940 mV, as shown in Fig. 4.6. With a PRF of 10 Mpulses/s, the resulting spectrum of the output pulse achieves both indoor and outdoor FCC compliance with more than 24 dB of sidelobe suppression without requiring the use of an off-chip filter, as shown in Fig. 4.7. The PSD -10 dB bandwidth is about 480 MHz and the PSD is below -42.15



Figure 4.7: Transmitter output in the frequency domain and its compliance with the FCC mask.



Figure 4.8: Transmitter output in the frequency domain for various supply voltages.

dBm/MHz. The measured spectrum also achieve FCC compliance within the supply voltage range from 1.1 to 1.3 V, as shown in Fig. 4.8.



Figure 4.9: (a)Power consumption of the transmitter versus the PRF, (b) Energy per pulse of the transmitter versus the PRF.



Figure 4.10: Center frequency of the transmitter output versus different tuning codes

#### 4.2.3.2 Power Measurement

The power consumption of the transmitter was analyzed for various PRFs from 100 pulses/s to 140 Mpulses/s, as shown in Fig. 4.9 (a). The

average leakage power,  $P_L = 725.9$  nW. The PRF dependent part is  $36.9 \pm 4.4 \ \mu\text{W}/\text{PRF}(\text{Mpulse/s})$ . As can be seen in Fig. 4.9 (b), the overall energy (active and leakage) per pulse,  $E_{dTX}$  ranges from 7.6 nJ/pulse at a PRF of 100 pulse/s to  $37.9 \pm 4 \text{pJ/pulse}$  with PRF beyond 200 kpulse/s. The average deviation of  $\pm 4 \text{ pJ/pulse}$  arises from different masking modes. The transmitted pulse energy is  $E_{pTX} = 3.6 \text{ pJ/pulse}$ , based on calculation from the time-domain output waveform. Thus, the transmitter achieves a maximum efficiency  $\eta = 8.6\%$ .

#### 4.2.3.3 Frequency Tuning Measurement

The measured center frequencies of the transmitter output versus different coarse and fine tuning codes are shown in 4.10. The coarse tuning codes of C<1:4>= "0000" meet the UWB frequency spectrum requirement. One of the measurement observations is that the fine tuning is nonlinear and only a few Most Significant Bits (MSBs) of F<1:8> are effective. Since in UWB applications, there is no requirement for linear fine tuning of the center frequency

#### 4.2.3.4 Measurement Result Comparison

The reference works which are chosen to be compared with our work are those with leakage power reported. The comparison results are shown in Table. 4.1. The FOM of energy per pulse of our work is larger than those from [41] and [52], but the output swing of our work is also larger than theirs. Due to the large output voltage swing, which indicates large transmitted energy per pulse, the transmitted efficiency of our work is the

	JSSC'09	TMTT'10	JSSC'11	JSSC'12	This work	
	[41]	[46]	[29]	[52]	THIS WOLK	
Technology (nm)	90	130	90	130	130	
Frequency Band (GHz)	3.1 - 5	3.1-10	2.9 - 3.8	3.1-5	3.1-4	
Output Amplitude $V_{pp}$ (V)	0.5	1.42	0.61	0.6	0.94	
Data Rate (Mbps)	$249.6^{1}$	100	10	10	10	
Energy per pulse $E_{dTX}$ (pJ)	17.5	38.4	83	20	37.9	
Transmitted Pulse Energy	0.9	19	1 9	15	3.6	
$E_{pTX}$ (pJ)	0.5	1.5	1.5	1.0	5.0	
Efficiency $E_{pTX}/E_{dTX}$ (%)	5.1	5	2.4	7.5	8.6	
Normalized energy per pulse <sup>2</sup>	35	97	136	22	40.3	
$E_{dTX}/V_{pp} \ (pJ/V)$	- 55	21	150	- 55		
Die Area $(mm^2)$	0.07	0.54	0.6	0.13	0.146	
Leakage Power $(\mu W)$	123	3200	184	7.2	0.73	

Table 4.1: Transmitter Performance Comparison (II)

<sup>1</sup>Every symbol contains 16 pulses

highest among all the works in the table. The most significant contribution of our work is the reduction of the leakage power. The leakage power of  $0.73 \ \mu\text{W}$  is the lowest. In [41], the oscillator is not gated and is always on so the static power is high. The reason that [46] consumes such large static power is unclear. It might come from the delay cell which has a current source bias. The IR-UWB transmitter in [52] is implemented in a mostly-digital way. Its leakage power is much smaller than the other two references, yet it is larger than this work. It should be noted that not all the designs referred in the comparison table had the goals of minimizing the leakage power. Many of them have more focus on the system and the transmitter is not optimized specifically.



Figure 4.11: System architecture of the proposed time-to-digital converter.

## 4.3 IR-UWB Receiver with a Coarse-fine TDC

#### 4.3.1 Introduction and System Architecture

TDC can be categorized in similar ways as ADC. There are pipelined TDC [80], SAR TDC [81, 82] and cyclic TDC [79]. To realize a large dynamic range, the multilevel or coarse-fine structure is often used in TDC design [78, 83]. The coarse stage sets the approximate position by delay interpolation or oscillator-based counter. The fine stage generates the high-resolution time Least Significant Bits (LSBs). As in Sigma-delta Analog-to-digital Converter (SDADC) which exploits noise shaping to achieve high voltage resolution, noise shaping could also be used in TDC. It is interesting to see that gated ring oscillator inherently possesses the character of noise shaping [84, 85]. A SDTDC was also proposed in [86]. The system architecture of the proposed TDC which could be used in SOC IR-UWB radar is shown in Fig. 4.11. The phase interpolator is used as the coarse stage of the TDC. Based on the position of the detect arrived pulse, the closest phases relative to the arrived pulse are selected by the phase selector and the fine stage of TDC generates the fine LSBs.

The requirements of the dynamic range and resolution of the TDC can be estimated based on the below calculations. Assume the reference oscillator frequency is  $f_{ref}$ =50 MHz, the maximum time delay of the transmitted and the received pulses is 20 ns. This implies a maximum detection range of 3 meters. The phase interpolator then generates 8 phases. With an additional 3-bit counter and a recirculating oscillator, the delay per stage for the phase interpolator is  $\Delta$ =20ns/8/8 = 312.5 ps. This is a suitable delay range in a 130 nm CMOS process. Note that the human respiration rate and heart-beat rate are below  $f_0$ =5 Hz, and  $f_s=f_{ref}$ =50 MHz. This results in a effective oversampling ratio of at least 5000000.

$$OSR = \frac{f_s}{2f_0} = 5 \times 10^7$$
 (4.1)

The oversampling results in shaped noise spectrum. The oversampled noise power is shown as below.

$$P_n = \left(\frac{\Delta^2}{12}\right) \left(\frac{\pi^2}{3}\right) \left(\frac{2f_0}{f_s}\right)^3 = \left(\frac{\Delta^2}{12}\right) \left(\frac{\pi^2}{3}\right) \left(\frac{1}{OSR}\right)^3 \tag{4.2}$$

The theoretical shaped noise in terms of distance is thus

$$\Delta_n = \left(\frac{\pi}{\sqrt{36}}\right) \left(\frac{1}{OSR}\right)^{3/2} (\Delta) \tag{4.3}$$

Substitute the parameters above results in a distance resolution of about  $1.5 \times 10^{-8} ps$ . Note that 1mm distance corresponds to a time of 6.7ps. The ideal resolution which can be achieved by SDTDC fully meets the requirements for sensing the human vital signs.

#### 4.3.2 Circuit Designs and Simulation Results

#### 4.3.2.1 Receiver Front-end

The circuit of the non-coherent IR-UWB receiver front-end, the LNA and the Pulse Detector (PD), is shown in Fig. 4.12. Compared with the design in Chapter 3, the LNA includes several on-chip inductors. The process we used is 130 nm CMOS process compared with the 65 nm CMOS process used in Chapter 3. Inductorless design is not able to provide enough wideband input matching and gain bandwidth in this design. The first stage of the LNA is a current-reuse complimentary CG stage. The second stage is a cascode CS stage with a inductive load. The circuit of the PD is similar with that in Chapter 3. The input bias of the first stage is adjusted so that it reaches the threshold level of the inverter. The second stage is a self-biased amplifier and is followed by four stages of inverters which digitize the detected pulse.



Figure 4.12: Circuit of the receiver front-end, LNA and Power Detector.

#### 4.3.2.2 Time-to-digital Converter

The multilevel coarse-fine structure is used for implementing the TDC with high dynamic range and high resolution. An recirculating Ring Oscillator (RO) is used as the coarse phase interpolator. The circuit schematic of the recirculating RO is shown in Fig. 4.13. For every 8 cycles, the divider and the select logic change the control signals of the first multiplexer and the reference clock is injected into the oscillator [87]. The recirculating RO reduces the number of delay stages significantly. This design generates  $8 \times 8 = 64$  phases using only 4 differential delay stages. With an additional phase comparator and a digital controller, the recirculating RO could evolve into a multiplying DLL [87]. The timing diagram of the recirculating RO is shown in Fig. 4.14.

The circuit of the delay element is shown in Fig. 4.15. By using a



Figure 4.13: Circuit of multi-phase recirculating oscillator.



Figure 4.14: Timing diagram of multi-phase recirculating oscillator.

differential delay cell, four delay stages generate 8 phases and the immunity to power supply variation is increased. The delay of the delay element is



Figure 4.15: Circuit of the differential delay cell.

controlled in a fully digital manner. In order to achieve a linear tuning control, segmented digital tuning is used [52]. The simulated delay of one delay element versus the control word is plotted in Fig. 4.16. The delay tuning is linear and all the results from different process corner simulations cover the delay that we desire. The reference frequency can be changed to make sure the next reference input arrives after the oscillator stops, as long as the required detection range is met.

The digital phase selector selects the closest two phases related to the input pulse, and the two phases are used as the reference timing edges. The fine TDC is implemented by a SDTDC. The circuit of the first-order SDTDC is shown in Fig. 4.17. The delta function is realized by a phase detector while the sigma function is realized by integrating the current in the capacitors. The comparator compares the voltage on the capacitor and chooses the reference timing edge which opens the charge pumps. Based on the output of the comparator, one of the references (E(i - 1), E(i))



Figure 4.16: Digital delay control of the delay element.



Figure 4.17: Circuit of the sigma-delta time-to-digital converter.

is selected. The reference edge is then combined with the input edge to generate the UP or DOWN controls for the charge pump. For detailed circuit implementations, a fully differential topology is used and the phase selector and charge pump are combined as shown in Fig. 4.18. The SDTDC is first-order and is inherently stable because the phase selector ensures that the input edge is between the reference edges.

The simulated time-domain and frequency-domain analysis results are



Figure 4.18: Circuit of combined phase selector and charge pump.

shown in Fig. 4.19. The DC idle tone is used as an input. The first-order noise shaping is observed and multiple reference spurs are shown in the simulation.

The simulated power consumption of different circuit blocks as follows: LNA (5.3 mW), PD (0.2 mW), Recirculating RO (1.5 mW), Digital Phase Selector (0.1 mW), SDTDC (0.3 mW). The power supply is 1.2 V.

#### 4.3.2.3 Chip Implementation and Measurement Results

The chip was implemented in 130 nm digital CMOS technology and the layout is shown in Fig. 4.20. The chip has been sent for fabrication in December 2014. The chip will be received in approximately three months. Measurement will be carried out once the chip is received and bonded on test board.

Part of the measurement results are shown below. In Fig. 4.21, the receiver detects a signal of -66 dBm at 10 Mbps. The delay tuning

CHAPTER 4. A Low-power Low-leakage IR-UWB Transmitter and an IR-UWB Receiver with a Coarse-fine TDC in 130-nm CMOS process





Figure 4.19: SDTDC output in (a) time domain (b) frequency domain.

measurement of the ring oscillator is shown in ig. 4.22. Delay of the ring oscillator is closed to simulation in SS corner.



CHAPTER 4. A Low-power Low-leakage IR-UWB Transmitter and an IR-UWB Receiver with a Coarse-fine TDC in 130-nm CMOS process

Figure 4.20: Chip layout of the receiver with time-to-digital converter.

X XX XX XX 🐼 XX XX

XX CC XX CC XX

From the measurement, the fine TDC has some problems which we are still trying to find the reasons. The problems are the both of the outputs of the SDTDC are either at power or ground for different chips. One of the most possible reasons might be the malfunction of the common-mode feedback circuit.





Figure 4.21: Time-domain measurement of the UWB receiver front-end.



Figure 4.22: Measured digital delay control of the delay element.

### Chapter 5

# A Fully Integrated UWB Event-Driven ECG SoC

### 5.1 Background and Introduction

Cardiovascular Disease (CVD) is the leading cause of death around the world. In 2008, about 17.3 million people died from CVDs [88]. The deferred detection of CVD symptoms and the lack of timely medical treatment often lower the patients survival rate. Because most heart disorders occur in infrequent and unpredictable manners, accurate diagnosis and risk assessment are possible only if the heart condition is monitored and recorded continuously for long periods of time. To reduce the heart attack risk and prevent severe heart damage, the patient should have continuous ambulatory heart condition monitoring solutions. An effective way of managing CVD is to use low-cost disposable wireless ECG patch for continuous monitoring. The wearable ECG sensor could track the electrical activities of the heart through capturing the ECG signals in a noninvasive manner. The ECG signal is then transferred to the base station or internet. The cardiologists can receive real-time data for interpretation and diagnosis. The patient can benefit from preventional health care and early diagnosis on heart conditions, without requiring frequent hospital visits or in-hospital stays for ECG monitoring. In case of heart attack, emergency service will be alerted immediately through wireless communication and internet, and the chance of survival or near-complete recovery is significantly higher. The main design targets for wearable ECG devices include high quality ECG capturing, compact size, long battery life, comfortable and easy to use, and also low cost.

In this chapter, we introduce a new wireless ECG sensor SOC. It combines event-driven Level-crossing (LC) Analog-to-information Converter (AIC) [89], IR-UWB transmitter and on-chip antenna with high impedance ECG Analog Front-end (AFE) amplifier. The DC-coupled AFE significantly improves the input impedance and signal quality, without any active impedance boosting feedback loops [90]. The event-driven AIC system includes a LC ADC with built-in QRS detection for heart rate monitoring. The delta-modulated output is fed to a 3-5 GHz IR-UWB transmitter with an on-chip antenna. Implemented in 0.13  $\mu$ m CMOS technology, the total power consumption for raw ECG signal transmission is 2.89  $\mu$ W, which is over 6 times better compared to state-of-the-art designs [27, 91]. Also the sensor system does not require any external components, e.g. clock, filters and off-chip antenna, making it a perfect candidate for a low-cost disposable wireless ECG sensor.


Figure 5.1: Topology of IR-UWB

## 5.2 System Architecture

The architecture of the proposed ECG sensor system is shown in Fig. 5.1. The sensor first captures the single-channel ECG signal from the skin surface through the low-noise AFE. The signal is then digitized through an LC ADC with 32 quantization levels, and sent through the IR-UWB transmitter. The communication at the transmitter side uses an on-chip antenna to minimize the number of off-chip components. The receiver tunnels the ECG data to the gateway such as the personal smartphone. The data is then uploaded to the cloud database and sent to the professionals. Our design mainly focuses on the sensor and the IR-UWB transmitter, which is the most critical part in the system and also often limited by the available power budget. The IR-UWB receiver and the decoder are not attached to the human body, which allows less stringent requirements on power and size. The receiver that we use is from Chapter 3.



Figure 5.2: Circuit of ECG AFE

## 5.3 Circuit Design Considerations

#### 5.3.1 DC-Input Front-End and Level-crossing ADC

The ECG AFE consists of two Instrumental Amplifiers (IAs) as impedance boosting buffers, and a Programmable-gain Amplifier (PGA) for gain control (Fig. 5.2). For dry electrode application, a high input impedance is critical for good signal quality. In this design, the ECG differential inputs are directly connected to the high input impedance gate terminals of the IAs. To avoid saturation caused by electrode offsets, a



Figure 5.3: Circuit of level-crossing ADC

pseudo resistor, which connects the input and the common mode VCM, is used to stabilize the input baseline. The input dynamic range is further enhanced by maintaining an AC gain of 50 which is set by the  $C_1$  capacitor ratio, while suppressing the DC gain to one. The DC offset at the IA output is then fully blocked by the following AC-coupled PGA. At the PGA feedback branch, a pseudo resistor implemented using high-threshold PMOS provides the high-pass cut-off of less than 0.05 Hz. An offset detector which monitors the OTA inputs  $V_{1+}$  and  $V_{1-}$  is proposed. Whenever  $V_{1+}$  or  $V_{1-}$  is higher than  $V_{CM}$ , the capacitor  $C_{off1}$  or  $C_{off2}$  will be charged, and trigger the reset to pull  $V_{1+}$  and  $V_{1-}$  back to  $V_{CM}$ . The input-sensing reset mechanism helps to minimize the baseline settling time without violating the high-pass requirement.

The LC ADC with uniform level quantization consists of two continuous-time comparators to track the input, and samples the signal whenever it changes more than one quantization level (Fig. 5.3). The delta-modulated outputs, DIR and REQ representing the signal voltage change direction and every level-crossing event, are encoded into a bit-stream packet using Manchester coding for the IR-UWB Transmitter. To further reduce the ECG data rate when required, a QRS detector circuit is implemented. The QRS detection is based on counting the amplitude of



Figure 5.4: Topology of IR-UWB transmitter with on-chip antenna

monotonic rising or falling LC events and comparing it with the pre-defined QRS threshold. It identifies a rising edge with large amplitude as a QR wave, and marks the following turning point as an R peak. By sending the QRS peaks only, the transmission rate is reduced to only 1 bps.

#### 5.3.2 UWB Transmitter and Antenna

The IR-UWB transmitter and the 2 mm × 2.5 mm on-chip coplanar waveguide-fed monopole antenna are implemented to transmit the encoded data. The schematic is shown in Fig. 5.4. One IR-UWB pulse is generated by each rising edge of the encoded data. Monopulse minimizes the hardware cost while it does not violate the FCC spectrum mask since the data rate is very low and the on-chip antenna has very low gain. The digital edge-combining technique is used to generate the mono-cycle pulse while the cascade amplifier with optimized on-chip inductor is used to drive the on-chip antenna. The pulse width is controlled digitally  $(D_0 - D_3)$  by varying the load capacitance of the inverter. The transmitter is activated only if encoded data pulses are received from the



Figure 5.5: Die micrograph of the SOC

ADC. The heavy duty-cycling of the transmitter significantly reduces the power consumption. This topology simplifies existing architectures while achieving low leakage and high output voltage swing. The on-chip antenna is implemented using the thick top metal layer. Its gain and input matching is optimized for 3-5 GHz band with consideration of not occupying too much area.

## 5.4 Simulation and Measurement Results

The chip was fabricated in a standard 130 nm CMOS technology. The entire sensor operates under 1.2 V supply voltage, while the amplifier and the ADC can work under 0.8 V supply. The die micrograph is shown in Fig. 5.5, with most area occupied by the on-chip antenna.



Figure 5.6: (a) Input-referred noise of the analog front-end, (b) Output spectrum of the front-end and ADC.

The total power consumption is 2.89  $\mu$ W for full-rate raw ECG transmission, which is over one magnitude lower than the current state-of-the-art designs.

The noise performance of the analog front-end amplifier is shown in Fig. 5.6 (a). The front-end input-referred noise is 3.06  $\mu V_{rms}$ , integrated from 0.5 Hz to 150 Hz. The input impedance is over 3.6 G $\Omega$ . Using a 10-Hz sinusoid testing signal input, we measured the signal reconstructed from ADC output DIR and REQ. The spectrum is shown in Fig. 5.6 (b). The front-end and the ADC achieve 42.2 dB SNR.

The measured transmitter's output voltage swing is 600 mV when terminated with a 50  $\Omega$  load (Fig. 5.7a) and achieves FCC compliance at the data rate of 100 kbps (Fig. 5.7b). No violation on the FCC mask is possible since the raw ECG data is below 100 kbps. The total power consumption of the UWB transmitter is 1.46  $\mu$ W at 100 kbps, in which most of the power consumption is due to leakage. The power consumption of the IR-UWB transmitter versus the data rate is plotted in Fig. 5.9 (a). Below the data rate of 100 kbps, the leakage power is dominant and the power consumption is unchanged with data rate. When the data rate is



Figure 5.7: UWB TX output in (a) time domain and (b) frequency domain.



Figure 5.8: On-chip antenna characteristics (a) Simulated and measured input matching (b) Radiation pattern when  $\Phi=0^{\circ}$  and  $\Phi=90^{\circ}$  at 4 GHz.

higher than 1000 kbps, the power consumed by the pulse generation is much larger than the leakage power, and the power increases linearly with data rate. The de-embedded measurement of the on-chip antenna shows that it achieves -10 dB return loss from 2 to 7 GHz (Fig. 5.8a). The simulated radiation pattern indicates an omnidirectional pattern with a peak realized gain of -37.3 dBi at 4 GHz (Fig. 5.8b). A custom-designed UWB receiver with a PCB antenna is used to receive and demodulate the UWB signal transmitted from this ECG sensor. The recovered ECG signal is shown in Fig. 5.9 (b).



Figure 5.9: (a) UWB TX power consumption vs data rate, (b) ECG signal reconstructed from wireless transmission.

## 5.5 Summary

In this chapter, we presents a fully-integrated wireless ECG sensor. A high-impedance front-end amplifier improves the ECG signal quality using dry electrode. The event-driven ADC and QRS detector minimize the data rate for the IR-UWB transmitter. Also as the antenna is integrated and no crystal oscillators are needed, with very little extra off-chip components are required. The total power consumption under raw ECG transmission mode is only 2.89  $\mu$ W.

## Chapter 6

# Conclusions and Recommendations for Future Works

## 6.1 Conclusions

Designing low-power, energy-efficient wireless transceivers is one of the key focuses in emerging applications such as IoT, biomedical systems and wireless sensors. It is one of the hottest topics in academia and industry. In this thesis, we explored one of the promising techniques which could bring a low-power, low-complexity and cost-effective solution to future wireless systems, the IR-UWB. We focused on applying IR-UWB technology in low or medium-data-rate, short-range biomedical applications. The system analysis was done and several prototype circuits were built in standard CMOS processes, measured and compared with state-of-the-art references. We managed to meet the design goals despite of the challenges and difficulties.

In the first part of the thesis, we gave an overview of the state-of-the-art UWB techniques and illustrated the reason IR-UWB was chosen to implement the following works. Based on the requirements of power consumption, data rate, transmission range, circuit complexity and cost, we determined that IR-UWB is used for the transceiver design.

In the second part of the thesis, the design procedures and measurement results of an inductorless, miniature and multi-functional CMOS IR-UWB was demonstrated. The reviews of the state-of-the-art IR-UWB transmitters and receivers were performed first. The system architecture and circuit implementations are determined by the system requirements and the link budget analysis. The all-digital transmitter generates IR-UWB pulses using edge combining technique and consumes 21.6 pJ/pulse at 10 Mbps. The data rate can be scaled up to 150 Mbps. A novel active-inductor-based technique is proposed for the LNA that achieves ultra-wideband input impedance matching in the receiver. The non-coherent receiver employs a simple demodulation and synchronization circuit to achieve self-synchronization without any on-chip or external oscillator. Consuming 6.4 mW, the receiver attains -64 dBm sensitivity at 10 Mbps. The chip is implemented in a 65 nm digital CMOS process and occupies only 0.04 mm<sup>2</sup>. Measurement shows that the transceiver/radar is capable of sensing the human's respiratory rate. The low power consumption, less circuit complexity and low cost make it suitable for biomedical applications. The transceiver/radar was implemented in standard 65 nm digital CMOS process.

In the third part of the thesis, the design procedures and measurement results of a low-power and energy-efficient CMOS IR-UWB transmitter was introduced. A DCO generates the carrier frequency and a TSPC mask generator generates the pulse mask. The oscillator output and pulse mask are then combined using a cascode output driver stage with an on-chip inductor load. The leakage power is 725.9 nW, which is better than the other state-of-the-art works. The DC energy per pulse is  $E_{dTX} = 36.9$ pJ/pulse and the transmitted pulse energy is  $E_{pTX} = 3.6$  pJ/pulse. Thus, the transmitter achieves a maximum efficiency  $\eta = 8.6\%$ , which is among the best of the reported works. An IR-UWB receiver with a coarse-fine TDC is also included, a multiple-phase DCO is used as the coarse TDC while the fine TDC is realized by an SDTDC. The TDC is designed to achieve a fine resolution with a large dynamic range.

Finally, we show a case study in which the IR-UWB transceiver is integrated with biomedical sensors in an **SOC!** system. The SOC includes an ECG sensor front-end, a level-crossing based asynchronous ADC, a low-power IR-UWB transmitter and an on-chip antenna. Implemented in 130 nm digital CMOS process, the system consumes 2.89  $\mu$ W under 1.2 V supply while transmitting the raw ECG data.

### 6.2 Recommendations of the Future Work

The power consumption of the IR-UWB receiver could be further reduced by duty-cycling the analog/RF front-end. In [92], the self-synchronization which shuts the RF front-end was achieved. The off-chip oscillator is required and timing recovery circuit is complex. There are still opportunities to further reduce the power and circuit complexity of the IR-UWB receiver. Another possible future work is to integrate transceiver and NB transceiver together. UWB transceiver is used for low-power short-range communication, while NB transceiver is used for low-range communication consuming more power. It is desirable that the transceiver is in compliance with the IEEE 802.15.6 standard.

The decouple of the large dynamic range and the high resolution is an another interesting topic associated with the TDC. Though the large detection range (tens of centimeters) is required, the range in which high timing resolution should be achieved is very small. From calculation we could find that when the movement of the chest is detected by the IR-UWB radar with a TDC, only a few LSBs change. This implies novel TDC architecture and circuits can be further investigated for this kind of sparse-event sensing to reduce the circuit complexity and power consumption. The discussions could also be extended to another applications in which range finding is achieved, such as the ultrasound transceiver and the imaging sensor. One enlightening direction is compressive sensing, which is a newly invented signal processing technique which addresses the detection and recovery of the sparse signals [91].

In the recirculating DLL, the phase mismatch calibration was not included in the thesis work. The phase mismatches of the phase generator will cause nonlinearity in the TDC. On-chip nonlinearity calibration should be included in the future designs. Multiple phase generators are not only useful in TDC, but also very important in time-interleaved ADC and wireline transceivers, where precise multi-phase clocks or timing references are required.

# Bibliography

- N. Saputra and J. Long, "A fully-integrated, short-range, low data rate fm-uwb transmitter in 90 nm cmos," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1627–1635, July 2011.
- [2] B. Murmann, "Digitally Assisted Analog Circuits," *Micro, IEEE*, vol. 26, no. 2, pp. 38–47, March 2006.
- [3] R. Staszewski, K. Muhammad, D. Leipold, C.-M. Hung, Y.-C. Ho, J. Wallberg, C. Fernando, K. Maggio, R. Staszewski, T. Jung, J. Koh, S. John, I. Y. Deng, V. Sarda, O. Moreira-Tamayo, V. Mayega, R. Katz, O. Friedman, O. Eliezer, E. de Obaldia, and P. Balsara, "All-digital TX frequency synthesizer and discrete-time receiver for Bluetooth radio in 130-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2278–2291, Dec 2004.
- [4] J. Andrews, S. Buzzi, W. Choi, S. Hanly, A. Lozano, A. Soong, and J. Zhang, "What will 5g be?" Selected Areas in Communications, IEEE Journal on, vol. 32, no. 6, pp. 1065–1082, June 2014.
- [5] (2013, December) Wireless Devices, Developing Countries Boost Medical Electronics Growth. http://www.icinsights.com/data/ articles/documents/628.pdf.
- [6] C. Deepu, X. Zhang, W.-S. Liew, D. Wong, and Y. Lian, "An ecg-on-chip with 535 nw/channel integrated lossless data compressor for wireless sensors," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2435–2448, Nov 2014.
- [7] A. Droitcour, O. Boric-Lubecke, V. Lubecke, J. Lin, and G. Kovacs, "Range correlation and i/q performance benefits in single-chip silicon doppler radars for noncontact cardiopulmonary monitoring," *IEEE Trans. Microw. Theory Techn.*, vol. 52, no. 3, pp. 838–848, March 2004.

- [8] M. Zargham and P. Gulak, "Maximum achievable efficiency in near-field coupled power-transfer systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 3, pp. 228–245, June 2012.
- [9] (2002, Apr.) First Report and Order, Revision of Part 15 of the Commissions Rules Regarding Ultra-Wideband Transmission Systems. ET Docket 98-153.
- [10] D. Leenaerts, R. van de Beek, J. Bergervoet, H. Kundur, G. van der Weide, A. Kapoor, T. Y. Pu, Y. Fang, Y. J. Wang, B. Mukkada, H. S. Lim, V. Kiran, C. S. Lim, S. Badiu, and A. Chang, "A 65 nm CMOS Inductorless Triple Band Group WiMedia UWB PHY," *IEEE* J. Solid-State Circuits, vol. 44, no. 12, pp. 3499–3510, Dec 2009.
- [11] T. Kikkawa, P. Saha, N. Sasaki, and K. Kimoto, "Gaussian Monocycle Pulse Transmitter Using 0.18 mum CMOS Technology With On-Chip Integrated Antennas for Inter-Chip UWB Communication," *IEEE J. Solid-State Circuits*, vol. 43, no. 5, pp. 1303–1312, May 2008.
- [12] V. Kulkarni, M. Muqsith, K. Niitsu, H. Ishikuro, and T. Kuroda, "A 750 Mb/s, 12 pJ/b, 6-to-10 GHz CMOS IR-UWB Transmitter With Embedded On-Chip Antenna," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 394–403, Feb 2009.
- [13] D. Lachartre, B. Denis, D. Morche, L. Ouvry, M. Pezzin, B. Piaget, J. Prouvee, and P. Vincent, "A 1.1nJ/b 802.15.4a-compliant fully integrated UWB transceiver in 0.13 um CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 312 –313,313a.
- [14] S. Joo, W.-H. Chen, T.-Y. Choi, M.-K. Oh, J.-H. Park, J.-Y. Kim, and B. Jung, "A fully integrated 802.15.4a IR-UWB Transceiver in 0.13 um CMOS with digital RRC synthesis," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 228–229.
- [15] D. Daly, P. Mercier, M. Bhardwaj, A. Stone, Z. Aldworth, T. Daniel, J. Voldman, J. Hildebrand, and A. Chandrakasan, "A pulsed uwb receiver soc for insect motion control," *IEEE J. Solid-State Circuits*, vol. 45, no. 1, pp. 153–166, Jan. 2010.
- [16] C. Zhang, M. Kuhn, B. Merkl, A. Fathy, and M. Mahfouz, "Real-Time Noncoherent UWB Positioning Radar With Millimeter Range Accuracy: Theory and Experiment," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 1, pp. 9–20, 2010.
- [17] T.-S. Chu, J. Roderick, S. Chang, T. Mercer, C. Du, and H. Hashemi, "A short-range UWB impulse-radio CMOS sensor for human feature"

detection," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2011, pp. 294–296.

- [18] (2012) 802.15.6-2012 IEEE Standard for Local and metropolitan area networks - Part 15.6: Wireless Body Area Networks. http://standards. ieee.org/findstds/standard/802.15.6-2012.html.
- [19] X. Wang, K. Philips, C. Zhou, B. Busze, H. Pflug, A. Young, J. Romme, P. Harpe, S. Bagga, S. D'Amico, M. De Matteis, A. Baschirotto, and H. de Groot, "A high-band ir-uwb chipset for real-time duty-cycled communication and localization systems," in *IEEE Proc. Asian Solid-State Circuits Conf.*, Nov 2011, pp. 381–384.
- [20] O. Werther, M. Cavin, A. Schneider, R. Renninger, B. Liang, L. Bu, Y. Jin, J. Rogers, and J. Marcincavage, "A Fully Integrated 14 Band, 3.1 to 10.6 GHz 0.13 mum SiGe BiCMOS UWB RF Transceiver," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2829–2843, Dec 2008.
- [21] B. Razavi, T. Aytur, C. Lam, F.-R. Yang, K.-Y. Li, R.-H. Yan, H.-C. Kang, C.-C. Hsu, and C.-C. Lee, "A UWB CMOS transceiver," *IEEE J. Solid-State Circuits*, vol. 40, no. 12, pp. 2555–2562, Dec. 2005.
- [22] T. Aytur, H.-C. Kang, R. Mahadevappa, M. Altintas, S. Brink, T. Diep, C.-C. Hsu, F. Shi, F.-R. Yang, C.-C. Lee, R.-H. Yan, and B. Razavi, "A Fully Integrated UWB PHY in 0.13μm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb 2006, pp. 418–427.
- [23] H. Zheng, S. Lou, D. Lu, C. Shen, T. Chan, and H. Luong, "A 3.1 GHz - 8.0 GHz Single-Chip Transceiver for MB-OFDM UWB in 0.18μm CMOS Process," *IEEE J. Solid-State Circuits*, vol. 44, no. 2, pp. 414–426, Feb 2009.
- [24] (2005) ECMA-368 Standard. http://www.ecma-international.org/ publications/standards/Ecma-368.htm.
- [25] Y. Zhao, Y. Dong, J. F. M. Gerrits, G. van Veenendaal, J. Long, and J. Farserotu, "A Short Range, Low Data Rate, 7.2 GHz-7.7 GHz FM-UWB Receiver Front-End," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1872–1882, July 2009.
- [26] X. Zou, X. Xu, L. Yao, and Y. Lian, "A 1-v 450-nw fully integrated programmable biomedical sensor interface chip," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1067–1077, April 2009.
- [27] M. Khayatzadeh, X. Zhang, J. Tan, W.-S. Liew, and Y. Lian, "A 0.7-v 17.4-/spl mu/w 3-lead wireless ecg soc," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 5, pp. 583–592, Oct 2013.

- [28] F. Zhang, A. Jha, R. Gharpurey, and P. Kinget, "An agile, ultra-wideband pulse radio transceiver with discrete-time wideband-if," *IEEE J. Solid-State Circuits*, vol. 44, no. 5, pp. 1336–1351, May 2009.
- [29] M. Crepaldi, C. Li, J. Fernandes, and P. Kinget, "An Ultra-Wideband Impulse-Radio Transceiver Chipset Using Synchronized-OOK Modulation," *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2284 –2299, Oct. 2011.
- [30] Y. Zheng, S.-X. Diao, C.-W. Ang, Y. Gao, F.-C. Choong, Z. Chen, X. Liu, Y.-S. Wang, X.-J. Yuan, and C. Heng, "A 0.92/5.3nJ/b UWB impulse radio SoC for communication and localization," in *IEEE ISS-CC Dig. Tech. Papers*, Feb. 2010, pp. 230 –231.
- [31] S. Solda, M. Caruso, A. Bevilacqua, A. Gerosa, D. Vogrig, and A. Neviani, "A 5 Mb/s UWB-IR Transceiver Front-End for Wireless Sensor Networks in 0.13- μm CMOS," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1636 –1647, July 2011.
- [32] P. Mercier, M. Bhardwaj, D. Daly, and A. Chandrakasan, "A Low-Voltage Energy-Sampling IR-UWB Digital Baseband Employing Quadratic Correlation," *IEEE J. Solid-State Circuits*, vol. 45, no. 6, pp. 1209–1219, June 2010.
- [33] D. Barras, R. Meyer-Piening, G. von Bueren, W. Hirt, and H. Jaeckel, "A low-power baseband asic for an energy-collection ir-uwb receiver," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1721–1733, June 2009.
- [34] M. Caruso, M. Bassi, A. Bevilacqua, and A. Neviani, "A 2-to-16ghz 204mw 3mm-resolution stepped-frequency radar for breast-cancer diagnostic imaging in 65nm cmos," in *IEEE ISSCC Dig. Tech. Papers*, Feb 2013, pp. 240–241.
- [35] D. Zito, D. Pepe, M. Mincica, and F. Zito, "A 90nm cmos soc uwb pulse radar for respiratory rate monitoring," in *IEEE ISSCC Dig. Tech. Papers*, Feb 2011, pp. 40–41.
- [36] M. Demirkan and R. Spencer, "A pulse-based ultra-wideband transmitter in 90-nm cmos for wpans," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2820–2828, Dec 2008.
- [37] J. Ryckaert, C. Desset, A. Fort, M. Badaroglu, V. De Heyn, P. Wambacq, G. Van der Plas, S. Donnay, B. Van Poucke, and B. Gyselinckx, "Ultra-wide-band transmitter for low-power wireless body area networks: design and evaluation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2515–2525, Dec 2005.

- [38] J. Ryckaert, G. Van der Plas, V. De Heyn, C. Desset, B. Van Poucke, and J. Craninckx, "A 0.65-to-1.4 nJ/Burst 3-to-10 GHz UWB All-Digital TX in 90 nm CMOS for IEEE 802.15.4a," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2860 –2869, Dec. 2007.
- [39] K.-Y. Lin and M. El-Gamal, "Design of low power cmos ultra-wideband 3.1-10.6 ghz pulse-based transmitters," in *IEEE Proc. Custom Integrated Circuits Conf.*, Sept 2008, pp. 583–586.
- [40] A. T. Phan, J. Lee, V. Krizhanovskii, Q. Le, S.-K. Han, and S.-G. Lee, "Energy-efficient low-complexity cmos pulse generator for multiband uwb impulse radio," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 55, no. 11, pp. 3552–3563, Dec 2008.
- [41] P. Mercier, D. Daly, and A. Chandrakasan, "An Energy-Efficient All-Digital UWB Transmitter Employing Dual Capacitively-Coupled Pulse-Shaping Drivers," *IEEE J. Solid-State Circuits*, vol. 44, no. 6, pp. 1679–1688, June 2009.
- [42] S. Diao, Y. Zheng, and C.-H. Heng, "A CMOS Ultra Low-Power and Highly Efficient UWB-IR Transmitter for WPAN Applications," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 3, pp. 200–204, Mar. 2009.
- [43] Y. Park and D. Wentzloff, "An all-digital 12 pj/pulse ir-uwb transmitter synthesized from a standard cell library," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1147–1157, May 2011.
- [44] M. Pelissier, J. Jantunen, B. Gomez, J. Arponen, G. Masson, S. Dia, J. Varteva, and M. Gary, "A 112 mb/s full duplex remotely-powered impulse-uwb rfid transceiver for wireless nv-memory applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 916–927, April 2011.
- [45] L. Smaini, C. Tinella, D. Helal, C. Stoecklin, L. Chabert, C. Devaucelle, R. Cattenoz, N. Rinaldi, and D. Belot, "Single-chip cmos pulse generator for uwb systems," *IEEE J. Solid-State Circuits*, vol. 41, no. 7, pp. 1551–1561, July 2006.
- [46] S. Bourdel, Y. Bachelet, J. Gaubert, R. Vauche, O. Fourquin, N. Dehaese, and H. Barthelemy, "A 9-pJ/Pulse 1.42-Vpp OOK CMOS UWB Pulse Generator for the 3.1-10.6-GHz FCC Band," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 1, pp. 65 –73, Jan. 2010.
- [47] D. Baranauskas and D. Zelenin, "A 0.36w 6b up to 20gs/s dac for uwb wave formation," in *IEEE ISSCC Dig. Tech. Papers*, Feb 2006, pp. 2380–2389.

- [48] D. Wentzloff and A. Chandrakasan, "A 47pJ/pulse 3.1-to-5GHz All-Digital UWB Transmitter in 90nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 118–591.
- [49] T. Norimatsu, R. Fujiwara, M. Kokubo, M. Miyazaki, A. Maeki, Y. Ogata, S. Kobayashi, N. Koshizuka, and K. Sakamura, "A uwb-ir transmitter with digitally controlled pulse generator," *IEEE J. Solid-State Circuits*, vol. 42, no. 6, pp. 1300–1309, June 2007.
- [50] Y. Zhu, J. Zuegel, J. Marciante, and H. Wu, "Distributed waveform generator: A new circuit technique for ultra-wideband pulse generation, shaping and modulation," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 808–823, March 2009.
- [51] H. Miranda and T. Meng, "A programmable pulse uwb transmitter with 34% energy efficiency for multichannel neuro-recording systems," in *IEEE Proc. Custom Integrated Circuits Conf.*, Sept 2010, pp. 1–4.
- [52] L. Wang, Y. Lian, and C.-H. Heng, "3-5 GHz 4-Channel UWB Beamforming Transmitter With 1° Scanning Resolution Through Calibrated Vernier Delay Line in 0.13- μm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 12, pp. 3145 –3159, Dec. 2012.
- [53] J. Ryckaert, M. Verhelst, M. Badaroglu, S. D'Amico, V. De Heyn, C. Desset, P. Nuzzo, B. Van Poucke, P. Wambacq, A. Baschirotto, W. Dehaene, and G. Van der Plas, "A cmos ultra-wideband receiver for low data-rate communication," *IEEE J. Solid-State Circuits*, vol. 42, no. 11, pp. 2515–2527, Nov 2007.
- [54] Y. Zheng, M. Arasu, K.-W. Wong, Y. J. The, A. Suan, D. D. Tran, W. G. Yeoh, and D.-L. Kwong, "A 0.18 μm cmos 802.15.4a uwb transceiver for communication and localization," in *IEEE ISSCC Dig. Tech. Papers*, Feb 2008, pp. 118–600.
- [55] L. Zhou, Z. Chen, C.-C. Wang, F. Tzeng, V. Jain, and P. Heydari, "A 2-gb/s 130-nm cmos rf-correlation-based ir-uwb transceiver front-end," *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 4, pp. 1117–1130, April 2011.
- [56] N. Van Helleputte and G. Gielen, "A 70 pj/pulse analog front-end in 130 nm cmos for uwb impulse radio receivers," *IEEE J. Solid-State Circuits*, vol. 44, no. 7, pp. 1862–1871, July 2009.
- [57] Y. Zheng, Y. Tong, C. W. Ang, Y.-P. Xu, W. G. Yeoh, F. Lin, and R. Singh, "A cmos carrier-less uwb transceiver for wpan applications," in *IEEE ISSCC Dig. Tech. Papers*, Feb 2006, pp. 378–387.

- [58] A. Medi and W. Namgoong, "A high data-rate energy-efficient interference-tolerant fully integrated cmos frequency channelized uwb transceiver for impulse radio," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 974–980, April 2008.
- [59] L. Liu, T. Sakurai, and M. Takamiya, "A charge-domain auto- and cross-correlation based data synchronization scheme with power- and area-efficient pll for impulse radio uwb receiver," *Solid-State Circuits*, *IEEE Journal of*, vol. 46, no. 6, pp. 1349–1359, June 2011.
- [60] P. Park, S. Kim, S. Woo, and C. Kim, "A centimeter resolution, 10 m range cmos impulse radio radar for human motion monitoring," *IEEE J. Solid-State Circuits*, vol. 49, no. 5, pp. 1125–1134, May 2014.
- [61] P. Thoppay, C. Dehollaini, M. Green, and M. Declercq, "A 0.24-nj/bit super-regenerative pulsed uwb receiver in 0.18-μm cmos," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2623–2634, Nov 2011.
- [62] Z. Zou, D. Mendoza, P. Wang, Q. Zhou, J. Mao, F. Jonsson, H. Tenhunen, and L.-R. Zheng, "A low-power and flexible energy detection ir-uwb receiver for rfid and wireless sensor networks," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 7, pp. 1470–1482, July 2011.
- [63] F. Lee and A. Chandrakasan, "A 2.5 nJ/bit 0.65 V Pulsed UWB Receiver in 90 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2851–2859, Dec. 2007.
- [64] R. Dokania, X. Wang, S. Tallur, and A. Apsel, "A low power impulse radio design for body-area-networks," *IEEE Trans. Circuits Syst.*, vol. 58, no. 7, pp. 1458–1469, July 2011.
- [65] D. Zito, D. Pepe, M. Mincica, F. Zito, A. Tognetti, A. Lanata, and D. De Rossi, "SoC CMOS UWB Pulse Radar Sensor for Contactless Respiratory Rate Monitoring," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 6, pp. 503 –510, Dec. 2011.
- [66] H. Hjortland, D. Wisland, T. Lande, C. Limbodal, and K. Meisal, "Thresholded samplers for uwb impulse radar," in *IEEE Proc. Int.* Symp. Circuits and Systems., May 2007, pp. 1210–1213.
- [67] X. Zou, W.-S. Liew, L. Yao, and Y. Lian, "A 1v 22 uw 32-channel implantable eeg recording ic," in *IEEE ISSCC Dig. Tech. Papers*, Feb 2010, pp. 126–127.

- [68] Channel Model for Body Area Network IEEE IEEE 802.15 Working Group Document. [Online]. Available: https://mentor.ieee.org/802. 15/dcn/08/15-08-0780-09-0006-tg6-channel-model.pdf
- [69] M. Crepaldi and P. Kinget, "Error ratio model for synchronised-OOK IR-UWB receivers in AWGN channels," *IET Electron. Lett.*, vol. 49, no. 1, pp. 25–27, Jan. 2013.
- [70] C. Hu and P. Chiang, "All-digital 3-50 GHz ultra-wideband pulse generator for short-range wireless interconnect in 40nm CMOS," in *IEEE Proc. Custom Integrated Circuits Conf.*, 2011, pp. 1–4.
- [71] A. Bevilacqua and A. Niknejad, "An ultrawideband CMOS low-noise amplifier for 3.1-10.6-GHz wireless receivers," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2259 – 2268, Dec. 2004.
- [72] H. Zhang, X. Fan, and E. Sinencio, "A Low-Power, Linearized, Ultra-Wideband LNA Design Technique," vol. 44, no. 2, pp. 320 –330, Feb. 2009.
- [73] B. Razavi, Design of Integrated Circuits for Optical Communications. McGraw-Hill, 2002.
- [74] S. Hampel, O. Schmitz, M. Tiebout, and I. Rolfes, "Inductorless 1-10.5 GHz wideband LNA for multistandard applications," in *IEEE Proc. Asian Solid-State Circuits Conf.*, 2009, pp. 269–272.
- [75] J. Brown, K.-K. Huang, E. Ansari, R. Rogel, Y. Lee, and D. Wentzloff, "An ultra-low-power 9.8GHz crystal-less UWB transceiver with digital baseband integrated in 0.18 um BiCMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2013, pp. 442–443.
- [76] A. Oncu and M. Fujishima, "19.2mW 2Gbps CMOS pulse receiver for 60GHz band wireless communication," in VLSI Circuits, 2008 IEEE Symposium on, June 2008, pp. 158 –159.
- [77] X. Zhang, Z. Zhang, Y. Li, C. Liu, G. Y., and Y. Lian, "A 2.89-muw fully integrated uwb event-driven ecg sensor for dry electrode use," in prep.
- [78] M. Lee and A. Abidi, "A 9 b, 1.25 ps resolution coarse-fine time-to-digital converter in 90 nm cmos that amplifies a time residue," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 769–777, April 2008.
- [79] Y.-H. Seo, J.-S. Kim, H.-J. Park, and J.-Y. Sim, "A 1.25 ps resolution 8b cyclic tdc in 0.13 μm cmos," *IEEE J. Solid-State Circuits*, vol. 47, no. 3, pp. 736–743, March 2012.

- [80] K. Kim, W. Yu, and S. Cho, "A 9 bit, 1.12 ps resolution 2.5 b/stage pipelined time-to-digital converter in 65 nm cmos using time-register," *IEEE J. Solid-State Circuits*, vol. 49, no. 4, pp. 1007–1016, April 2014.
- [81] H. Chung, H. Ishikuro, and T. Kuroda, "A 10-bit 80-ms/s decision-select successive approximation tdc in 65-nm cmos," *IEEE J. Solid-State Circuits*, vol. 47, no. 5, pp. 1232–1241, May 2012.
- [82] A. Mantyniemi, T. Rahkonen, and J. Kostamovaara, "A cmos time-to-digital converter (tdc) based on a cyclic time domain successive approximation interpolation method," *IEEE J. Solid-State Circuits*, vol. 44, no. 11, pp. 3067–3078, Nov 2009.
- [83] J.-P. Jansson, A. Mantyniemi, and J. Kostamovaara, "A cmos time-to-digital converter with better than 10 ps single-shot precision," *IEEE J. Solid-State Circuits*, vol. 41, no. 6, pp. 1286–1296, June 2006.
- [84] A. Elshazly, S. Rao, B. Young, and P. Hanumolu, "A noise-shaping time-to-digital converter using switched-ring oscillators: Analysis, design, and measurement techniques," *IEEE J. Solid-State Circuit*s, vol. 49, no. 5, pp. 1184–1197, May 2014.
- [85] M. Straayer and M. Perrott, "A multi-path gated ring oscillator tdc with first-order noise shaping," *IEEE J. Solid-State Circuits*, vol. 44, no. 4, pp. 1089–1098, April 2009.
- [86] D.-W. Jee, Y.-H. Seo, H.-J. Park, and J.-Y. Sim, "A 2 ghz fractional-n digital pll with 1b noise shaping  $\delta \sigma$  tdc," *IEEE J. Solid-State Circuits*, vol. 47, no. 4, pp. 875–883, April 2012.
- [87] R. Farjad-Rad, W. Dally, H.-T. Ng, R. Senthinathan, M.-J. Lee, R. Rathi, and J. Poulton, "A low-power multiplying dll for low-jitter multigigahertz clock generation in highly integrated digital chips," *IEEE J. Solid-State Circuits*, vol. 37, no. 12, pp. 1804–1812, Dec 2002.
- [88] (2013) Cardiovascular diseases (CVDs). http://www.who.int/ cardiovascular\_diseases/en/.
- [89] Y. Tsividis, "Event-driven data acquisition and digital signal processing : A tutorial," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 57, no. 8, pp. 577–581, Aug 2010.
- [90] J. Xu, R. Yazicioglu, P. Harpe, K. Makinwa, and C. Van Hoof, "A 160 uw 8-channel active electrode system for eeg monitoring," in *IEEE ISSCC Dig. Tech. Papers*, Feb 2011, pp. 300–302.

- [91] F. Zhang, Y. Zhang, J. Silver, Y. Shakhsheer, M. Nagaraju, A. Klinefelter, J. Pandey, J. Boley, E. Carlson, A. Shrivastava, B. Otis, and B. Calhoun, "A batteryless 19 uw mics/ism-band energy harvesting body area sensor node soc," in *IEEE ISSCC Dig. Tech. Papers*, Feb 2012, pp. 298–300.
- [92] B. Vigraham and P. Kinget, "A self-duty-cycled and synchronized uwb pulse-radio receiver soc with automatic threshold-recovery based demodulation," *IEEE J. Solid-State Circuits*, vol. 49, no. 3, pp. 581–594, March 2014.