STUDY ON THE REDUCTION OF ACCESS RESISTANCE OF INALN/GAN HIGH ELECTRON MOBILITY TRANSISTORS

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STUDY ON THE REDUCTION OF ACCESS RESISTANCE OF INALN/GAN HIGH ELECTRON MOBILITY TRANSISTORS

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DECLARATION

I hereby declare that this thesis is my original work and it has been written by me in its entirety.

I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

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Liu Yi

20th Jan, 2015

体会这狂野

体会孤独

这是我

完美生活

——许巍

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SUMMARY

Device performance of InAlN/GaN high electron mobility transistors (HEMTs) can be limited by the access resistance, including contact resistance and semiconductor resistance at access region. With the advancing of technology, the demonstration of lattice matched InAlN/GaN grown on 8-inch silicon wafer presents an opportunity for the fabrication of InAlN/GaN HEMTs in modern silicon foundries. To realize that, it is necessary to develop CMOS process compatible ohmic contacts scheme to avoid the widely used gold based contacts in traditional GaN HEMTs. Furthermore, high temperature treatment is normally involved for those contacts, causing rough surface morphology and edges and hence reliability issues. In this research, we focus on the study on the reduction of access resistance in InAlN/GaN HEMTs in a perspective of CMOS compatibility and low thermal budget.

In this work, first we examined the Ti/Al with two-step annealing and Hf/Al/Ni/Au ohmic contacts on n-GaN as the preliminary evaluation works for InAlN/GaN HEMTs. The results showed that Hf-based ohmic contacts are promising to obtain contacts with low thermal budget and low contact resistance. A systematic study has been conducted for Hf-based contact on $In_{0.18}Al_{0.12}N$/GaN. The Hf/Al/Ta contacts yielded the lowest ohmic transition temperature of 550 ^{o}C, compared to other transition counterparts (Ti, Ta, Zr, Nb, and V). The optimized Hf/Al/Ta (15/200/20 nm) contacts after annealing at 600 ^{o}C exhibited the minimum contact resistance (R_c) of 0.59 Ω.mm that was comparable to traditional Ti/Al/Ni/Au contacts. The RMS roughness of the Hf/Al/Ta contact surface was as

low as 7.6 nm for Hf/Al/Ta contacts compared to 159 nm for Ti/Al/Ni/Au contacts. The interface between HF/Al/Ta contact and $In_{0.18}Al_{0.12}N$/GaN was also found to be smooth, in contrast to that for Ti/Al/Ni/Au contacts, which is rough with contact inclusions formation. The aging test showed that Hf/Al/Ta contacts were stable at 350 ^{o}C in air for more than 200 hours. Thermionic field emission (TFE) was found to be the dominant carrier transport mechanism in the optimized Hf/Al/Ta (15/200/20 nm) contacts for carrier transport. An effective energy barrier height and carrier density of 2DEG was found to be 0.48 eV and 1.72×10^{19} cm^{-3}, respectively, leading to an efficient electron tunneling through the InAlN barrier. DC output and transfer characteristics for InAlN/GaN HEMTs with the Hf/Al/Ta contacts are comparable to the counterparts with Ti/Al/Ni/Au contacts. Furthermore, the three-terminal off-state breakdown voltage of the devices with Hf/Al/Ta contacts is improved significantly by ~100 V (~ 53.5 %) higher than those with Ti/Al/Ni/Au contacts.

To further reduce the access resistance, $LaAlO_3$ (LAO) passivation has been examined in InAlN/GaN HEMTs with Hf/Al/Ta source/drain ohmic contacts. The sheet resistance of InAlN/GaN can be reduced by 12% due to 25 nm LAO passivation. After an off-state voltage stress, the results show that current collapse can be sigificantly suppressed by LAO passivation. In terms of device DC performance, an increase of 21% in I_{Dmax} an 20% of $g_{m,max}$ have been achieved in the LAO-passivated InAlN/GaN HEMTs compared to the unpassivated ones.

In conclusion, employing the Hf/Al/Ta ohmic contact scheme in InAlN/GaN HEMTs could realize CMOS compatibility and low thermal budget and also

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LIST OF ABBREVIATIONS

AFM	atomic force microscopy
ALD	atomic layer deposition
AlGaAs/InGaAs	aluminum gallium arsenide/indium gallium arsenide
AlGaN/GaN	aluminum gallium nitride/gallium nitride
CTE	coefficients of thermal expansion
CTLM	circular transmission line method
CMOS	complementary metal-oxide-semiconductor
DC	direct current
DI	de-ionized
EDX	energy-dispersive X-ray spectroscopy
FE	field emission
FOM	figure of merit
HAADF	high-angle annular-dark-field
HEMT	high electron mobility transistor
ICP	inductively couple plasma
InAlN/GaN	indium aluminum nitride/gallium nitride
IPA	isopropyl alcohol
LAO	lanthanum aluminum oxide
LD	laser diode
LED	light emitting diode
LTLM	linear transmission line method
MBE	molecular beam epitaxy

MOCVD	metal organic chemical vapor deposition
MOS	metal oxide semiconductor
MOVPE	metal organic vapor phase epitaxy
PECVD	plasma-enhanced chemical vapor deposition
PLD	plused laser deposition
RF	radio frequency
RIE	reactive ion etching
RMS	root mean square
RT	room temperature
RTA	rapid thermal annealing
SBH	Schottky barrier height
SSL	solid-state lighting
SIMS	secondary ion mass spectroscopy
STEM	scanning transmission electron microscopy
TE	thermionic emission
TEM	transmission electron microscopy
TFE	thermionic-field emission
TM	transition metal
ToF-SIMS	time of fight secondary ion mass spectroscopy
UV	ultra-violet
XRD	X-ray diffraction
2DEG	two-dimensional electron gas

LIST OF SYMBOLS

E_g	bandgap (eV)
ε	dielectric constant
E_c	critical breakdown field (MV/cm)
μ_n	electron mobility ($cm^2/V \cdot s$)
λ_{th}	thermal conductivity (W/cm·K)
v_t	electron saturation velocity (cm/s)
+σ	positive sheet charge
-σ	negative sheet charge
P_{SP}	spontaneous polarization
P_{PE}	piezoelectric polarization
α_L	thermal expansion coefficient ($/^oC$ or /K)
f_T	unity gain cut off frequency (Hz)
f_{max}	unity power gain frequency (Hz)
n_s	sheet carrier density (cm^{-2})
R_c	contact resistance (Ω)
R_{ext}	semiconductor resistance between gate and source/drain contacts (Ω)
R_{ch}	device channel resistance under the gate electrode (Ω)
R_{sh}	sheet resistance (Ω/□)
ρ_c	contact resistivity ($\Omega \cdot cm^2$)
Φ_b	Schottky barrier height (eV)
Φ_m	metal work function (eV)

χ_s electron affinity of the semiconductor (eV)

S fermi level pinning factor

ΔX the difference in electronegativity of constituent elements in semiconductor (eV)

E_{00} characteristic energy (eV)

N carrier concentration (cm^{-3})

m^* effective mass of carrier (kg)

q elementary electric charge (C)

h planck constant (J·s)

λ wavelength (nm)

k Boltzmann's constant (J/K)

T temperature (^oC or K)

R_T total resistance (Ω)

L_T transfer length (cm)

I current (A)

B magnetic field (T)

F_L Lorentz force (N)

v velocity (m/s)

V_H Hall voltage (V)

R_H Hall coefficient (m^3/C)

d_{hkl} inter-planar spacing of any lattice planes with Miller indices {h k l}

t_{Al}/t_{Hf} Al/Hf thickness ratio

t_{Al}/t_{Ti} Al/Ti thickness ratio

A_{Ri} Richardson constant (A·cm^{-2}·K^{-2})

E_n energy difference between the conduction-band edge and the Fermi level of the semiconductor (eV)

R_{on} on-state resistance (Ω)

R_a surface roughness (nm)

L_g gate length (μm)

L_{gs} gate-to-source distance (μm)

L_{gd} gate-to-drain distance (μm)

W_G gate width (μm)

V_{GS} voltage between gate and source (V)

V_{DS} voltage between drain and source (V)

V_{BK} breakdown voltage (V)

V_{th} threshold voltage (V)

$I_{D,max}$ maximum drain current (A)

$g_{m,max}$ maximum transconductance (mS)

LIST OF PUBLICATIONS

Journal Publications Directly Related to this Thesis

1. ***Y. Liu***, S. P. Singh, Y. J. Ngoo, L. M. Kyaw, M. K. Bera, G. Q. Lo, and E. F. Chor, "Low thermal budget Hf/Al/Ta ohmic contacts for InAlN/GaN-on-Si HEMTs with enhanced breakdown voltage", *Journal of Vacuum Science & Technology B,* 32 (2014) 032201.
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Other Journal Publications

3. M. K. Bera, ***Y. Liu***, L. M. Kyaw, Y. J. Ngoo, S. P. Singh, and E. F. Chor, "Positive Threshold-Voltage Shift of Y_2O_3 Gate Dielectric InAlN/GaN-on-Si (111) MOSHEMTs with respect to HEMTs", *Journal of Solid State Science and Technology*, 3(6), (2014) Q120-Q126.
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5. L. M. Kyaw, L. K. Bera, ***Y. Liu***, M. K. Bera, S. P. Singh, S. B. Dolmanan, H. R. Tan, T. N. Bhat, E. F. Chor, and S. Tripathy, "Probing channel temperature profiles in $Al_xGa_{1-x}N$/GaN high electron mobility transistors on 200 mm

diameter Si(111) by optical spectroscopy", *Applied Physics Letters*, 105 (2014) 073504.

6. L. M. Kyaw, S. B. Dolmanan, M. K. Bera, ***Y. Liu***, H. R. Tan, T. N. Bhat, Y. Dikme, E. F. Chor and S. Tripathy, "Influence of RuO_x Gate Thermal Annealing on Electrical Characteristics of $Al_xGa_{1-x}N$/GaN HEMTs on 200-mm Silicon", *ECS Solid State Letters*, 3(2), (2014) Q5-Q8.
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Conference Publications Directly Related to this Thesis

1. ***Y. Liu***, M. K. Bera, L. M. Kyaw, G. Q. Lo, E. F. Chor, "Low resistivity Hf/Al/Ni/Au Ohmic Contact Scheme to n-Type GaN", *World Academy of Science, Engineering and Technology* 69, (2012) 602
2. ***Y. Liu***, L. M. Kyaw, M.K. Bera, S. P. Singh, Y. J. Ngoo, G.Q. Lo, and E. F. Chor, "Low thermal budget Au- Free Hf-based ohmic contacts on InAlN/GaN heterostructure", *ECS Transactions*, 61(4), (2014) 319.

Other Conference Publications

3. M. K. Bera, ***Y. Liu***, L. M. Kyaw, Y. J. Ngoo, and E. F. Chor, "Thickness Dependent Electrical Characteristics of InAlN/GaN-on-Si MOSHEMTs with

Y_2O_3 Gate Dielectric and Au-free Ohmic Contact", *ECS Transactions*, 53(2), (2013) 65-74

4. L. M. Kyaw, ***Y. Liu***, M.K. Bera, Y. J. Ngoo, S. Tripathy, E. F. Chor, "Gold-free InAlN/GaN Schottky Gate HEMT on Si(111) Substrate with ZrO_2 Passivation", *ECS Transactions*, 53(2), (2013) 75-83
5. S. P. Singh, ***Y. Liu***, L. M. Kyaw, Y. J. Ngoo, M. K. Bera, S. Tripathy, and E. F. Chor, "Silicon nitride thickness dependence electrical properties of InAlN/GaN heterostructures", *ECS Transactions*, 61(4), (2014) 215.
6. M. K. Bera, ***Y. Liu***, L. M. Kyaw, Y. J. Ngoo, S. P. Singh, and E. F. Chor, "Fabrication and performance of InAlN/GaN-on-Si MOSHEMTs with $LaAlO_3$ gate dielectric using gate-first CMOS compatible process at low thermal budget", *ECS Transactions*, 61(4), (2014) 271.
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8. L. M. Kyaw, L. K. Bera, ***Y. Liu***, M. K. Bera, S. P. Singh, S. B. Dolmanan, T. N. Bhat, E. F. Chor, and S. Tripathy, "Micro-Raman and Photoluminescence Thermography of AlGaN/GaN HEMTs Grown on 200 mm Si(111)", presented at the International Workshop on Nitride Semiconductors (IWN 2014), Wroclaw, Poland, August 24-29, 2014.
9. L. M. Kyaw, ***Y. Liu***, M. K. Bera, S. P. Singh, S. Tripathy, and E. F. Chor, "Electrical Characteristics of Au-free $In_xAl_{1-x}N$/GaN HEMTs Fabricated

Using A Single Contact Annealing Process", presented at the International Workshop on Nitride Semiconductors (IWN 2014), Wroclaw, Poland, August 24-29, 2014.

Chapter 1

Introduction

An overview on gallium nitride (GaN) and its related heterostructures will be presented in this chapter. Section 1.1 will focus on the material properties of GaN, its related heterostructures and their possible applications. In Section 1.2, a brief introduction on the development of GaN based HEMTs will be given. After that, research work on access resistance on InAlN/GaN will be reviewed in Section 1.3. Finally, the motivation of this project and the scope of the thesis are described.

1.1 Properties of Gallium Nitride

GaN is considered one of the most important semiconductors after silicon. Since the successful synthesis of GaN demonstrated by Johnson *et al.* in 1932 [1] by means of heating purified gallium source in an ammonia ambient, it has been attractive to researchers in the fields of optoelectronics and microelectronics for more than eight decades. There are three types of GaN crystalline structures, namely zinc blende, rock salt and wurtzite. Under ambient conditions, the thermodynamically stable structure is wurtzite for GaN. In some cases, due to the compatibility with the topology of the substrate, the zinc blende GaN can be epitaxial grown on {011} crystal planes of cubic substrates like silicon [2], silicon carbide [3] etc. The rock salt structure for GaN is only realizable under high pressure and the structural phase change to rock salt form has been observed under the pressure of 52.2 GPa in experiment [4]. Therefore, the form of rock salt

GaN exists only in research laboratories, which also makes it impossible to be produced by any epitaxial growth techniques of low pressure. Among these three phases of GaN, the main interest is in wurtzite structure, which has a hexagonal unite cell and thus two lattice constants, **c** and **a**. Specifically, the wurtzite GaN includes alternating biatomic close-packed (0001) planes of N and Ga pairs. A stick-and-ball illustration of wurtzite GaN structure is portrayed in Figure 1.1. Since there is lack of an inversion plane vertical to the **c**-axis, GaN has two different polarities, namely, the surface of GaN terminated either by Ga atoms (Ga-polarity) with a label of (0001) plane or N atoms (N-polarity) with a label of $(000\bar{1})$ plane as shown in Figure 1.1. The discrepancy between these two directions of (0001) and $(000\bar{1})$ is critical in wurtzite GaN because Ga polarity or N polarity implies the different polarities of the polarization charges respectively. The (0001) plane, also called basal plane, is the most commonly used surface for growth, which indicates that the GaN substrate with Ga polarity are often obtained more easily compared to that with N polarity. Accordingly, many studies associated to GaN growth and GaN-based devices have been carried out on the wurtzite structure GaN.

Despite the fact that GaN is strategically important and has been extensively studied for a long time, further research is still required to approach the level of knowledge and application scope of other important semiconductors like silicon and gallium arsenide. Historically, the growth of GaN often encountered the challenges from large background n-type carrier concentrations owing to native defects and impurities. And the difficulty in realizing p-type doping in GaN

caused the limited applications and the slow progress of research in the early stage. However, much research on GaN growth has been conducted in the past tens of years, most of those challenges above have been well studied and understood, and some of them have been overcome or weakened. Therefore, the greatly improved GaN wafer quality due to the overcoming of those fundamental issues made it possible to fabricate GaN based devices in research level and also paved the way for their various applications.

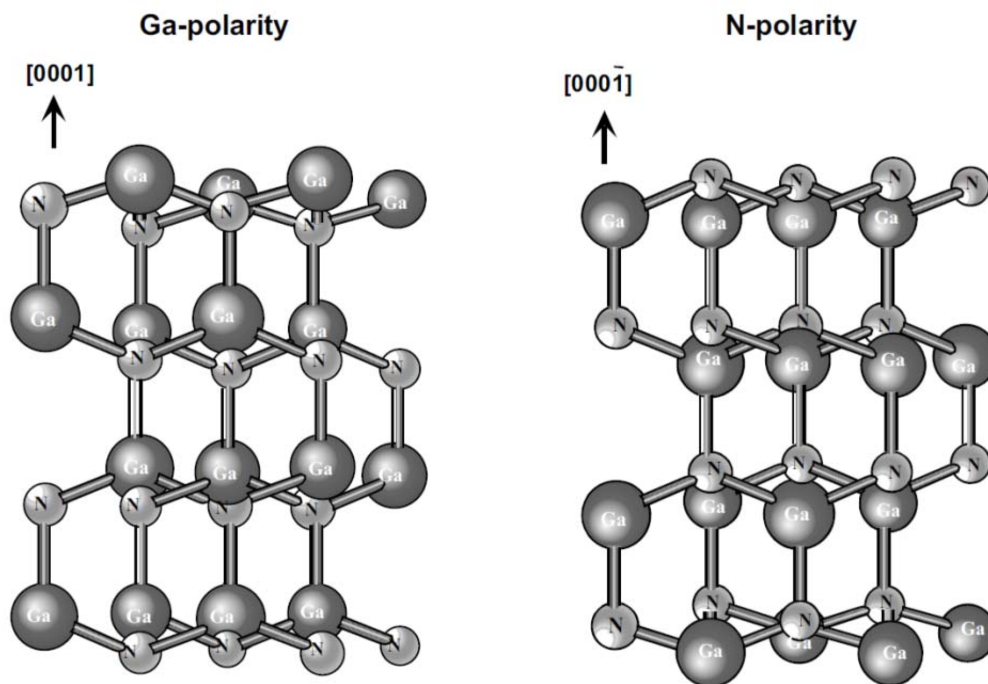


Figure 1.1 A stick-and-ball illustration of hexagonal structure for GaN [5].

First, one important area for GaN is the application of short-wavelength optoelectronics for the last few decades. Since the band gaps are not large enough (1.1 eV for Si and 1.4 for GaAs as shown in Table 1.1), silicon and traditional III-V semiconductor materials like GaAs cannot meet the requirements for the

optoelectronic devices in the blue and violet spectrum. Furthermore, silicon also has an indirect bandgap that indicating a low recombination efficiency of electron-hole pairs. However, GaN and its related alloys are principally appropriate in these fields. As shown in Figure 1.2, the wurtzite III-nitrides can form continuous alloys (InGaN, InAlN and AlGaN etc.) [6, 7], whose direct bandgaps range from 1.9 eV for InN, to 3.42 for GaN, and to 6.2 eV for AlN. Here, it is noted that the bandgap for wurtzite InN has been calibrated and accepted to be 0.7 eV [8]. The wide range of bandgap, corresponding to the photon wavelength from 200 nm to 1.77 μm, spans from the infrared, including the entire visible spectrum, and extends into the ultraviolet region. Therefore, this makes GaN and its related nitride alloys as promising candidates for optoelectronic device applications, such as light emitting diodes (LEDs) [9], laser diodes (LDs) [10], and detectors operating in the green, blue or UV wavelength [11]. Particularly, the GaN-based blue and green LEDs combined with GaAs-based red LEDs are essential to develop full-color displays and white light source for solid-state lighting (SSL) [12].

Furthermore, the unique physical and electrical properties of GaN have made it also promising for high-speed and high-power device applications, and these are summarized in Table 1.1, which shows a comparison of these material parameters for silicon (Si), Gallium arsenide (GaAs), silicon carbide (SiC), and GaN [12]. As seen, GaN possesses a wide bandgap of 3.4 eV, which indicates good resistance to the transition of intrinsic material characteristic and the increase of thermally generated leakage current at high-temperature. In addition, the high critical

breakdown field (around 4 MV/cm) allows GaN-based electronic devices/circuits (e.g., diodes, switches, amplifiers) to operate at high power. Furthermore, the good electron transport characteristics of GaN (high electron mobility of 1300 $cm^2/V{\cdot}s$ and high electron saturation velocity of 3×10^7 $cm{\cdot}s^{-1}$) are essential for electron devices working at high speed.

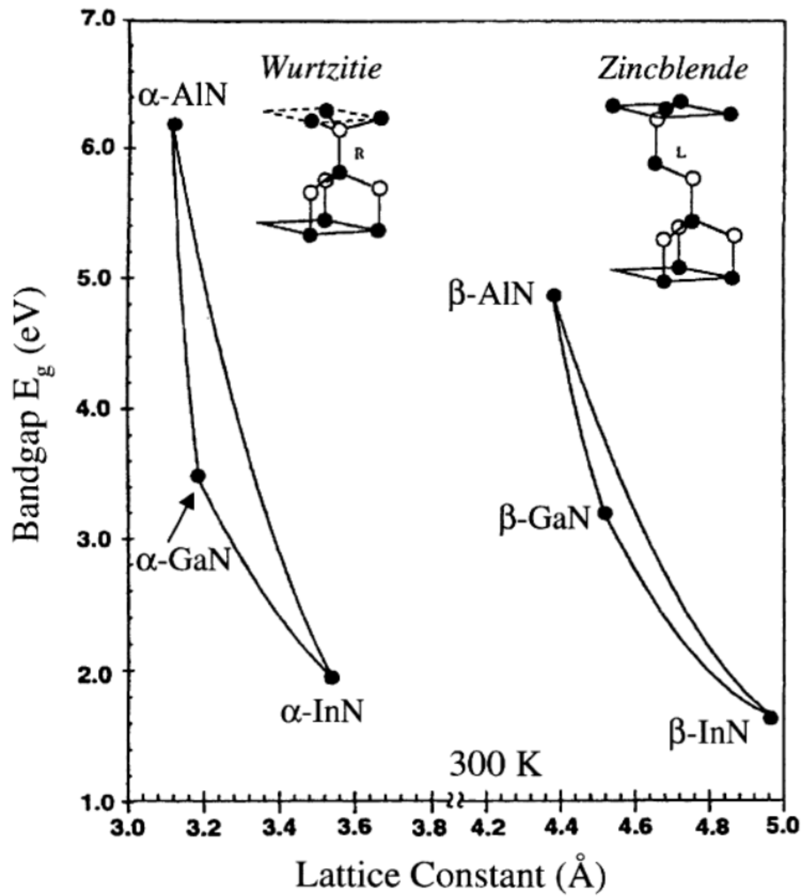


Figure 1.2 Bandgap versus lattice parameters for wurtzite (α-phase) and zinc blende (β-phase) binaries of AlN, GaN and InN [12].

Table 1.1 Material parameters for Si, GaAs, SiC and GaN [12].

Material	Si	GaAs	4H-SiC	**GaN**
Bandgap E_g (eV)	1.12	1.42	3.25	**3.4**
Dielectric constant ε	11.8	12.8	9.7	**9.0**
Critical breakdown field E_c (MV/cm)	0.25	0.4	3	**4.0**
Electron mobility μ_n (cm^2/V·s)	1350	6000	800	**1300**
Thermal conductivity λ_{th} (W/cm·K)	1.5	0.5	4.9	**1.3**
Electron saturation velocity v_t (10^7 cm/s)	1	2.0	2.0	**3.0**

Table 1.2 shows the power electronics figures of merit for for Si, GaAs, SiC, and GaN [13], where Chow and Tyagi proved theoretically the advantages of GaN over Si, GaAs, and SiC for high frequency and high power applications by means of Johnson, Keyes and Baliga figures of merit. These figures are related to critical breakdown field (E_c), Dielectric constant (ε), carrier mobility (μ), thermal conductivity (λ_{th}), and saturated electron velocity (v_t), and are used to evaluate the ability of power handling and thermal dissipation for electron devices. Si based devices for RF and power applications are limited by material properties such as inversion layer mobility, saturation velocity and small bandgap, and silicon technology currently is approaching the theoretical limits of performance.

Although, GaAs-based materials have been widely used in high frequency field, the high power application is limited by the small breakdown voltage and low thermal conductivity compared to either GaN or SiC. GaN and SiC, having a large bandgap, can be used in high-power and high-temperature applications due to the lower intrinsic carrier generation, high electron saturation velocity and high breakdown voltage.

However, the strongest advantage of GaN over SiC is that heterostructure technologies are available for GaN related alloys, which allows quantum well and hetero-junction realized in GaN material system to span new operation areas for GaN based high mobility electron transistors (HEMTs). To some extent, GaN based nitride electronics can be regarded as the wide bandgap counterpart of the AlGaAs/InGaAs system. Two dimension electron gases (2DEGs) with high electron density and high mobility can be achieved in GaN based heterostructures.

This implies that coulomb scattering in a Si-doped GaN based heterostructure can be reduced because of the spatial separation of the electron carriers from the ionized dopants. For instance, in AlGaN/GaN heterostructure, the widely used structure in GaN electronic devices, a measured Hall electron mobility of 2019 $cm^2/V\cdot s$ at room temperature and 10250 $cm^2/V\cdot s$ below 10 K has been reported in the 2DEG channel on 6H-SiC substrate [14]. Furthermore, owing to the strong polarization effects in GaN based heterostructure, device design options for HEMTs without introducing intentional dopants become possible. The total polarization charges in GaN based heterostructure arise mainly from two sources:

Table 1.2 Power electronics figures of merit (FOM) for various semiconductors at 300 K for microwave power device applications. All FOMs are normalized with respect to those of silicon.

Figures of merit	Johnson	Keyes	Baliga-low frequencies	Baliga-high frequencies
Equation	$\propto (E_C V_t)^2$	$\propto \lambda \left(\frac{V_t}{\varepsilon}\right)^{1/2}$	$\propto \varepsilon \mu {E_c}^3$	$\propto \mu {E_c}^3$
Description	Power handling at high frequencies	Thermal dissipation	Power handling at low frequencies	Power handling at high frequencies
Si	1	1	1	1
GaAs	11	0.45	28	16
4H-SiC	37	0.73	16	3.8
GaN	**790**	**1.8**	**910**	**100**

piezoelectric and spontaneous polarizations. The piezoelectric polarization results from the lack of center of inversion symmetry when III-nitride is strained along **c** axis in the wurtzite structure. The piezoelectric effect has two components: one is due to lattice mismatch strain while the other is due to the thermal strain caused by the thermal expansion coefficient difference between GaN and epitaxial layers grown in GaN (e.g., AlGaN). The spontaneous polarization effect happens owing to the non-centro symmetry wurtzite structure and the large ionicity of the

covalent III-nitrogen bond. For example, as shown in Figure 1.3, with different AlGaN compositions in AlGaN/GaN heterostructures, the piezoelectric polarization is negative for tensile and positive for compressive strained AlGaN barriers, respectively. The total macroscopic polarization of AlGaN layer is the sum of spontaneous polarization and strain-induced or piezoelectric polarization. Furthermore, at an abrupt interface (AlGaN/GaN), the difference in polarization of AlGaN and GaN will induce the positive sheet charge ($+\sigma$) for Ga-face and negative sheet charge ($-\sigma$) for N-face, an opposite sign of free charges (electron or holes) will tend to compensate the polarization induced charges at the interface. If the band offset at the abrupt interface of the heterostructure is high and the interface roughness is low, these accumulated free electrons or holes can be confined to form sheet charges in a potential well at the interface. Since polarization effects are large enough to produce 2DEGs confined in the AlGaN/GaN heterostructure as shown in Figure 1.3(c), a high sheet carrier concentration in the range of $\sim 10^{13}$ cm^{-2} can be achieved, which is ten times higher than that in the doped GaAs material system, even without intentionally introduced dopants in the AlGaN barrier layer.

In addition to its excellent optical and electrical properties mentioned above, GaN has a high hardness, heat capacity, thermal conductivity and superb chemical inertness, which allows GaN-based devices to operate well in harsh environments [15]. Furthermore, military and space applications could also benefit as GaN-based devices have revealed robustness in radiation environments [16].

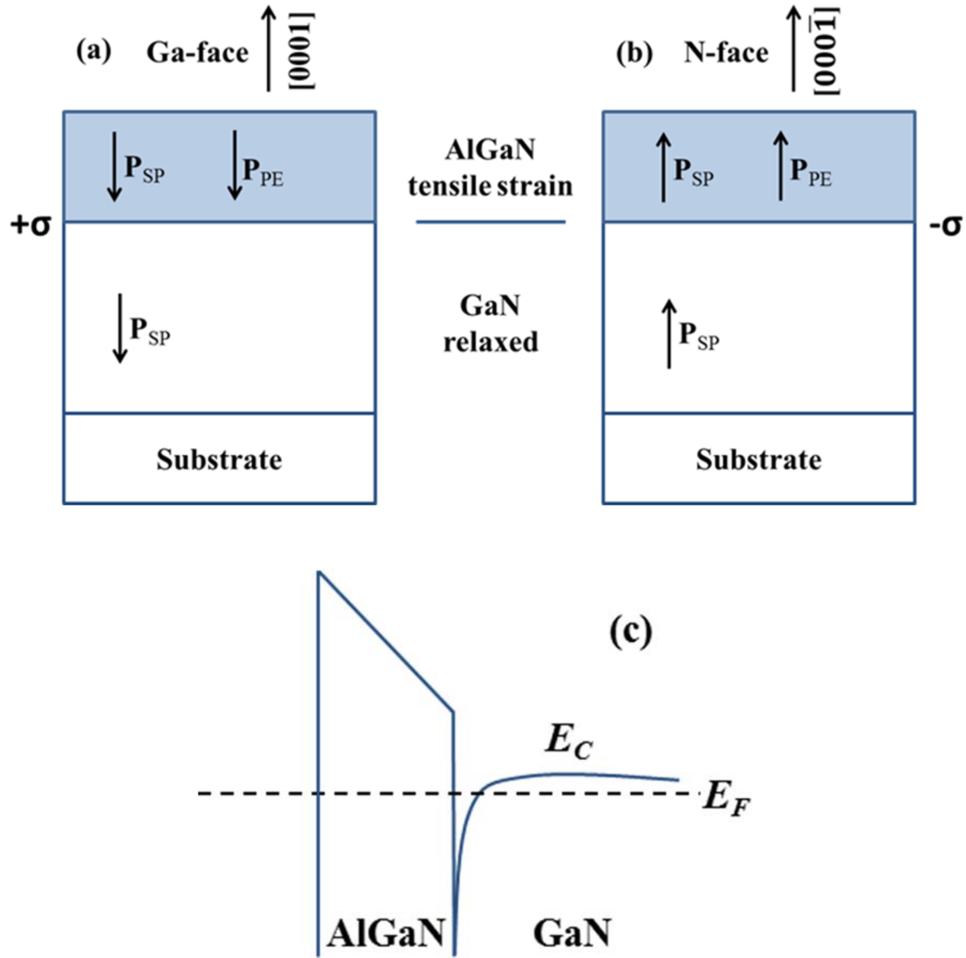


Figure 1.3 Polarization induced sheet charge density and directions of the spontaneous (SP) and piezoelectric (PE) polarizations in (a) Ga-face and (b) N-face AlGaN/GaN heterostructures [17]. (c) The energy band diagram for the AlGaN/GaN heterostructure with Ga-face AlGaN barrier layer.

1.2 GaN based High Electron Mobility Transistors

1.2.1 GaN HEMT heterostructure growth

Due to the lack of native GaN substrates in large quantities, researchers had tried nearly most of the crystal-growth technologies on different substrates and orientations to grow high quality GaN materials. With the great progresses

achieved in the past several decades, the epitaxial growth of GaN HEMT structures has been realized for both metal organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) systems. Compared to MBE, MOCVD is the more popular method, accepted widely for GaN and its related alloys epitaxial growth due to the higher growth rate, multi-wafer capability easily achievable, higher temperature growth (growth process is thermodynamically favorable), equivalently good quality of layers and the lower cost structure (both process and ownership).

The heterogeneous GaN epitaxy for HEMTs usually comprises three key elements shown in Figure 1.4: nucleation layer of the film, buffer layer structure, and device layer structure. The nucleation layer thin film is very essential for GaN hetero-epitaxial growth. At the early stage, the growth of GaN on foreign substrates had a rough surface mainly caused by the 3D-growth mode. Thus, a low-temperature AlN layer [18], prior to the high temperature growth of GaN, is first grown to serve as a template for the nucleation of growth, to accommodate lattice mismatch and promote lateral growth of the GaN film due to the decreased interfacial free energy between GaN and the substrate. Secondly, the buffer layer structure, typically a sequence of layers, is grown between the nucleation layer and the device layer structures. The principle functions of this structure are: coefficients of thermal expansion (CTEs) stress mitigation, threading dislocation density reduction, and electrical isolation. Mitigating the effects of the CTE mismatch is important to ensure crack-free epitaxy on a wafer that has wafer bow sufficiently low to allow for device fabrication on standard processing equipment.

The threading dislocation density benefits from the free energy reduction which drives the system toward the tendency to annihilate threading dislocations in the buffer layer structure. A highly semi-insulating buffer layer is also imperative to minimize device leakage by controlling the level of point defects such as impurity elements substituting for the Ga or N sites and lattice vacancies predominately determined the conductivity of the buffer material. Thirdly, the layers grown for the realization and optimization of the high electron mobility region consist of the device layer structure. Certain heterojunctions in the GaN material system produce a 2DEG with high mobility and unusually high charge due to band alignment that results in a dramatically downwards bending of the conduction band below the Fermi level as shown in Figure 1.3(c). The heterojunction to form 2DEG was first demonstrated by AlGaN/GaN and then afterwards InAlN/GaN. Furthermore, a thin AlN interlayer is normally inserted between the barrier layer (AlGaN or InAlN) and GaN to enhance the conduction band discontinuity, which can significantly improve the 2DEG carrier density and mobility.

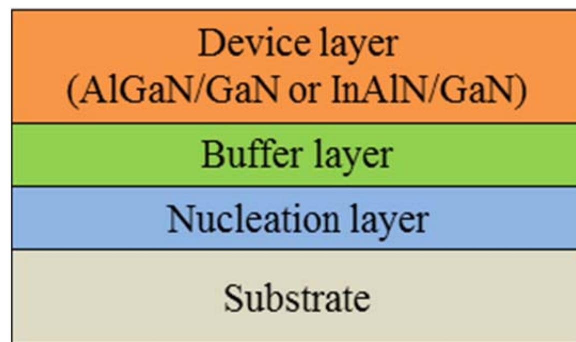


Figure1.4 The schematic of a typical GaN epitaxial heterostructure for HEMT application

Table 1.3 summarizes the properties of various substrates for GaN epitaxial growth. Initially, GaN HEMT structures were grown on sapphire due to the fact that it is cheap with a good quality and available for 2 to 4 inch substrates. The main disadvantage of sapphire is the poor thermal conductivity, resulting in excessive heating of HEMT device, which in turn impedes performance. The other shortcomings for sapphire substrate include a large mismatch (~16%), leading to a high amount of dislocations and higher thermal expansion coefficient introducing stress to cause cracks in epitaxial layer and substrate, and the lack of large size substrate at present. SiC was the next substrate to be used and is still the best choice for high performance requirement due to its lower lattice mismatch (~3.5%) and good thermal conductivity. The drawbacks of SiC are high cost and also limited large diameter of the substrates. Si substrate is becoming more attractive at present due to its relatively high thermal conductivity, low production price, and also available in large wafer size with vast quantity. Epitaxial growth of GaN on Si is challenging due to its large lattice constant and thermal expansion coefficient mismatch to GaN buffer, but techniques to overcome this have been developed over the past decade, resulting in increased performance and reliability. The growth of GaN HEMT heterostructures on silicon (111) was demonstrated in 1999 [19]. Recent developments in AlGaN/GaN and InAlN/GaN heterostructure epitaxy have also resulted in growth on 8-inch silicon substrates, compared to the maximum of 3 inches for SiC and 4 inches for sapphire [20-22]. This capability of growing GaN based heterostructure on large size silicon substrate could make huge step towards lower-cost GaN-on-silicon power devices.

Table 1.3 Comparison of substrates available for GaN epitaxial growth [23, 24].

Substrate	GaN	SiC	Sapphire	Si
Thermal Conductivity (W/cm·K)	1.3	3	0.5	1.5
Resistivity (Ω·cm)	$>10^4$	$>10^4$	$>10^8$	$>10^4$
Diameter used for Epitaxy (in)	2	2-3	2-4	2-8
Lattice mismatch to GaN (%)	0	3.5	16	16.9
Thermal expansion mismatch to GaN ($\alpha_{L(GaN)}$ - $\alpha_{L(sub)}$/$\alpha_{L(sub)}$)	0	18.9	-25.4	116
Cost	high	high	low	low

1.2.2 Development of GaN based HEMTs

1.2.2.1 Conventional AlGaN/GaN HEMTs technology

Benefiting from the excellent material properties of GaN and the advantages of heterojunctions, AlGaN/GaN HEMTs have been showing great potential for high-power and high-frequency operations since the first demonstration in 1993 [25]. However, the reported values in terms of device performance (maximum drain current, maximum extrinsic transconductance, maximum current- and power-gain cutoff frequency, and maximum power density) are diverse due to many key factors. The performance of GaN HEMTs is mainly affected by GaN heterostructure quality (carrier concentration and mobility), the properties of

ohmic contact and gate stack, devise dimension, advance device structure design (e.g., field plate and sub-micro T-gate), advance processing (e.g., regrowth ohmic and recessed gate) and surface passivation. The major developments and milestones achieved for AlGaN/GaN HEMTs are summarized below.

1. First demonstration of AlGaN/GaN HEMTs: Khan et al. [25] reported that the AlGaN/GaN HEMTs, with a 250 nm gate length, exhibited a maximum current density of 180 mA/mm, a peak extrinsic transconductance of 23 mS/mm and an electron mobility of 563 $cm^2/V \cdot s$ at 300 K.

2. Advanced ohmic technology: Qiao el al. [26, 27] employed solid phase reaction between ohmic metals and AlGaN layer during rapid thermal annealing and Buttari et al. [28] adopted dry etch method to reduce the thickness of AlGaN layer to enhance tunneling through the high bandgap AlGaN barrier layer. Regrown ohmic structure was also used by N. Chen et al. [29] to reduce the ohmic contact resistance by providing a small barrier between the regrown n+-GaN and AlGaN epilayer.

3. Metal-oxide-semiconductor HEMTs (MOS-HEMTs): Khan et al. [30] first reported the MOS-HEMT design which combines the advantages of the MOS structure that suppresses the gate leakage, and an AlGaN/GaN heterostructure that provides high-density high-mobility 2DEG channel.

4. Current collapse and passivation: Kohn et al. [31] first revealed current collapse on AlGaN/GaN HEMTs in 1999. The surface passivation technique by silicon nitride was proposed to prevent the positive charges at the surface from being

compensated [32]. Vetury et al. [33] proposed that current collapse during a microwave power measurement made on an AlGaN/GaN HEMT is the consequence of the creation of second virtual gate located between the gate and drain. This virtual gate is caused by the presence of states on the surface of AlGaN/GaN substrate.

5. Field plates: Chini et al. [34] first demonstrated the use of an additional separate field plate to increase the device performance from 8 W/mm to 18.8 W/mm. The improvement in the performance was due to the reduction of the peak field at the edge of the gate at drain side. This supported both a higher operating voltage of the HEMT and a reduced dispersion which led to higher power added efficiencies. By optimization of the field plate, Wu et al. [35] achieved a device power density of 32 W/mm at 4 GHz.

6. Reliability related to the reverse piezoelectric effect: Joh and Alamo first proposed [36, 37] and experimentally observed [38] the failure mechanism for AlGaN/GaN HEMTs that is based on crystallographic defect formation through the inverse piezoelectric effect due to high vertical electric field at the drain edge of the gate. When a high electric field is applied, the mechanical strain of the AlGaN barrier by this electric field can be produced due to the inverse piezoelectric effect. If the total strain exceeds a critical value, strain can relax through defect formation, such as dislocations.

As the quality of AlGaN/GaN wafer and device processing technology continuously evolved, the current AlGaN/GaN HEMTs exhibit great

improvement, which could be comparable or better than other competing materials (e.g., Si, GaAs, and InP). Chung et al. [39] reported that a maximum drain current density of 1.2 A/mm and peak extrinsic transconductance of 410 mS/mm, an f_T of 70 GHz and a high f_{max} of 300 GHz were obtained in AlGaN/GaN-on-SiC HEMTs with recessed ohmic contacts. Bouzid-Driad et al. [40] demonstrated that a maximum drain current density was 820 mA/mm, peak extrinsic transconductance of 440 mS/mm, and a f_T of 100 GHz and a high f_{max} of 206 GHz were achieved in AlGaN/GaN-on-Si HEMTs. Selvaraj et al. [41] obtained that 1.4 kV of three-terminal off-state breakdown voltage for gate-drain distance exceeding 15 μm with a specific on-resistance of 9.6 $m\Omega \cdot cm^2$ in AlGaN/GaN HEMTs on p-Si (111) substrate.

1.2.2.2 Emerging InAlN/GaN HEMTs technology

Although AlGaN/GaN HEMTs, the most popular GaN based electron devices, have demonstrated outstanding performance in the field of RF and power electronics in the last decade [42, 43], the reliability of AlGaN/GaN HEMT technology are still remaining, which has been explained by lattice defects introduced by the stress resulting from the mismatch and modulated by the inverse piezoelectric effect [36]. Based on this, InAlN/GaN heterostructures are emerging for RF and power electronic technology [44]. Simply, an $In_{0.18}Al_{0.82}N$ epitaxial layer grown lattice matched to GaN was chosen by substituting the AlGaN barrier to attempt to solve this problem. With the InAlN barrier lattice matched to GaN, stress and piezoelectric polarization do not exist, possibly improving the stability of the GaN heterostructure. As shown in Table 1.4, even

without piezoelectric polarization, InAlN/GaN heterostructure with a thinner layer of InAlN can provide higher 2DEG carrier density due to the three times higher spontaneous polarization than that in the conventional AlGaN/GaN, which implies a higher output current density and even higher power density if the breakdown conditions can be maintained [45]. Experimentally, InAlN/GaN HEMTs have been proposed to provide higher polarization charges without the drawback of high strain [46]. Several groups have demonstrated devices based on InAlN/GaN [47-50] with maximum current capabilities surpassing those of AlGaN/GaN structures.

Table 1.4 Spontaneous polarization ($\mathbf{P}_{SP}$) and piezoelectric polarization ($\mathbf{P}_{PE}$) and theoretical calculation of the free electron density ($\mathbf{n}_s$) in InAlN/GaN and AlGaN/GaN HEMTs [49].

Structure	$\Delta\mathbf{P}_{SP}$ (cm^{-2})	$\mathbf{P}_{PE}$ (cm^{-2})	$\mathbf{n}_s$ (cm^{-2})
$Al_{0.3}Ga_{0.7}N/GaN$	-1.56×10^{-2}	-9.8×10^{-3}	1.58×10^{13}
$In_{0.17}Al_{0.83}/GaN$	-4.37×10^{-2}	0	2.73×10^{13}

Since most of the technologies developed for AlGaN/GaN HEMTs can be transferred to InAlN/GaN, the progress for InAlN/GaN research is developing very fast. The outstanding device performances have been reported and are summarized as follows. Yue et al. [51] achieved a maximum drain current density of 1.9 A/mm, a peak extrinsic transconductance of 653 m/mm and f_T of 400 GHz in InAlN/GaN-on-SiC HEMTs. Schuette et al. [52] reported f_T / f_{max} of 359/347 GHz for enhancement mode and f_T / f_{max} of 302/301 GHz for depletion mode

InAlN/GaN-on-SiC HEMTs. Zhou et al. [53] demonstrated that a high three-terminal off-state breakdown voltage of 650 V in InAlN/GaN-on-sapphire HEMTs with Schottky source/drain contacts. Lee et al. [54] reported a three-terminal off-state breakdown voltage of 3 kV and a low specific on-resistance of 4.25 mΩ·cm^2 in InAlN/GaN HEMTs on SiC with an AlGaN back barrier. These results clearly demonstrate the potential of InAlN/GaN based devices for high frequency and high power applications. Further development of InAlN/GaN HEMTs depends on the improvement of material quality, the optimization of device structures and device processing technology.

1.3 Access resistance in InAlN/GaN HEMTs

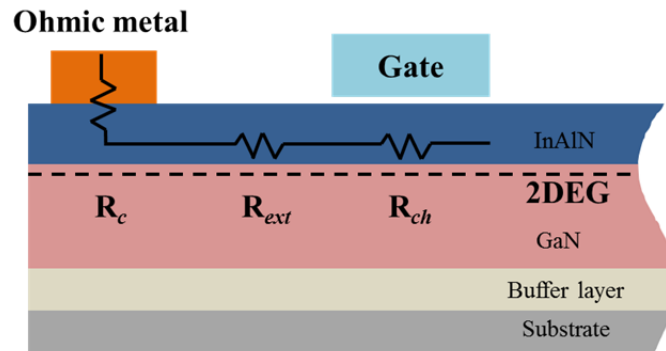


Figure1.5 Components of access resistance in InAlN/GaN HEMTs, where R_c is the resistance between metal contacts and InAlN barrier layer, R_{ext} is the semiconductor resistance between Gate and source/drain ohmic contacts, and R_{ch} is the device channel resistance under the gate electrode.

To fully utilize the advantages of emerging InAlN/GaN technology for HEMT application, one of the key factors is parasitic resistance. As show in Figure 1.5, the parasitic resistance consists of two major parts (R_c and R_{ext}) in the device

access region. R_c refers to the contact resistance of the ohmic contacts in InAlN/GaN HEMTs while R_{ext} is related to the semiconductor resistance between gate and source/drain contacts. Therefore, it is critical to enhance InAlN/GaN HEMTs performance by improving the properties of ohmic contacts and reducing the semiconductor resistance in the access region mentioned above.

Firstly, a good ohmic should exhibits low contact resistance and contact resistivity, smooth surface as well as good thermal stability. To achieve such a high quality ohmic contact, several techniques have been employed in InAlN/GaN heterostructure. Table 1.5 summarizes the ohmic contact resistance, specific contact resistivity, contact scheme and technologies used that have been reported and investigated in lattice matched InAlN/GaN heterostructure. First of all, Ti/Al based alloyed contacts are widely used in InAlN/GaN HEMTs [55-58], since there were also the most popular ohmic contacts in AlGaN/GaN HEMTs. The ohmic behavior formation of Ti/Al based alloyed contacts was found to correspond to the formation of TiN at the metal-semiconductor interface and the formation of its inclusions down to the level of the 2DEG after a high temperature contact annealing (~800 ^{o}C) [59]. Tirelli *et al.* [55] reported that Ti/Al/Mo/Au annealed at 860 ^{o}C achieved a contact resistance of 0.3 Ω·mm on InAlN/GaN. Lo et al. [57] demonstrated that the contact resistance of 0.65 Ω·mm and contact resistivity of 2×10^{-5} Ω·cm^2 for Ti/Al/Ni/Au contacts after 800 ^{o}C annealing. Recessed ohmic technology was also used to improve ohmic contact on InAlN/GaN [60-62]. K. Čičo et al. [61] utilized Ar-based sputtering process to recess the InAlN/GaN with a 15 nm barrier first and deposited traditional

Ti/Al/Ni/Au contacts. A low ohmic contact resistance of 0.39 Ω·mm was realized after annealing at 700 ^{o}C for 2 min. Pozzovivo et al. [62] used $SiCl_4$ chemistry to etch away about 3 nm of the 9 nm InAlN barrier layer in InAlN/GaN, and this had yielded contact resistance and specific contact resistivity of 0.7 Ω·mm and 1.1×10^{-7} Ω·cm^2, respectively, with 600 ^{o}C annealing for Ti/Al/Ni/Au ohmic contacts. Lee et al. [60] also used $SiCl_4$ to etch InAlN/GaN with a etch depth around 15 nm, indicating full removal of the 9.8 nm thick InAlN barrier layer in InAlN/GaN and using Mo/Al/Mo/Au contacts with annealing at 650 ^{o}C achieved a minimum contact resistance of 0.15 Ω·mm and contact resistivity of 7.8×10^{-7} Ω·cm^2. The researchers from University of Notre Dame developed a regrowth method to reduce contact resistance to InAlN/GaN [63-65]. First of all, a SiO_2 hard mask was deposited using plasma-enhanced chemical vapor deposition (PECVD) and the regrowth region was defined by stepper lithography and etched away to form a well with 40 nm deep. A layer of 80 nm n^+-GaN with a Si doping level of $\sim 1 \times 10^{20}$ cm^{-3} was then regrown by MBE on the SiO_2 mask patterned InAlN/GaN substrate. After the regrowth of n^+-GaN, the undesirable polycrystalline GaN on top of SiO_2 was lifted off by buffer HF. Lastly, nonalloyed ohmic contact of Ti/Au was formed by electron-beam evaporation. The Ti/Au-based regrowth ohmic contacts exhibited a total contact resistance of 0.16 Ω·mm. Overall, the development of good ohmic contact in InAlN/GaN HEMTs is still progressing since there are problems remaining which current method cannot to be solved. The recessed ohmic contacts always face the repeatability issues due to the lack of etching stop layer and difficulty of control etch rate in InAlN/GaN. The regrowth

technique is complicated and costly for mass production of InAlN/GaN HTMTs and also has the uniformity problem for large size wafer processing. Therefore, the traditional Ti/Al based alloyed contacts are most widely used in InAlN/GaN HEMTs, although they require high temperature annealing and thus cause a rough surface of ohmic contacts [59].

Table 1.5 Ohmic contacts to InAlN/GaN with their electrical results

Group	Wafer	R_{sh} (Ω/□)	Ohmic metal stack	R_c (Ω·mm)	ρ_c (10^{-7} Ω·cm^2)	Method	Temp. (°C)	Ref.
Uulm	InAlN /GaN	-	Ti/Al/ Ni/Cu/ Ta	0.46	-	-	900	[56]
UF	InAlN /GaN	231	Ti/Al/ Ni/Au	0.65	200	-	800	[57]
ETH	InAlN /GaN	193	Ti/Al/ Mo/Au	0.3	-	-	860	[55]
Xidian	InAlN /GaN/ InAlN	347	Ti/Al/ Ni/Au	0.33	-	-	830	[58]
UIUC	InAlN /GaN	241	Mo/Al/ Mo/Au	0.15	7.8	Recessed ($SiCl_4$)	650	[60]
SAS	InAlN /GaN	255	Ti/Al/ Ni/Au	0.39	-	Recessed (Ar)	700	[61]
TU Wien	InAlN /GaN	237	Ti/Al/ Ni/Au	0.7	1.1	Recessed ($SiCl_4$)	600	[62]
Notre Dame	InAlN /GaN	257	Ti/Al/ Ni/Au	0.4	-	Regrown n+-GaN	850	[64]
Notre Dame	InAlN /GaN	257	Mo/Au	0.25	0.11-0.15	Regrown n+-GaN	Non-alloyed	[65]
Notre Dame	InAlN /GaN	262	Ti/Au	0.16	-	Regrown n+-GaN	Non-alloyed	[63]

Secondly, to further improve the performance of GaN HEMTs, another approach is using device passivation techniques. Generally, passivation is very useful not

only in reduction of substrate sheet resistance but also suppression the current collapse in GaN HEMTs. Al_2O_3 and SiN are the most popular materials used for device passivation in InAlN/GaN HEMTs. J. Guo et al. [66] demonstrated that the sheet resistance of InAlN/GaN heterostructure was decreased from 425 to 382 Ω/□ after 140 nm SiN passivation layer by PECVD and the current collapse was effectively suppressed in InAlN/GaN HEMTs. H. Wang et al [67] reported that the use of a 25 nm Al_2O_3 passivation by atomic layer deposition (ALD) could improve the sheet resistance of InAlN/GaN substrate from 220 to 206 Ω/□ and suppressed the current collapse of devices. Therefore, a proper passivation layer can be applied to enhance InAlN/GaN HEMTs further.

1.4 Motivation and synopsis of the thesis

As mentioned earlier, with the availability of InAlN/GaN-on-Si wafer with excellent quality and a diameter of 8 inches, it is desirable to develop GaN-on-Si device fabrication technology to allow its processing in incumbent Si complementary metal–oxide–semiconductor (CMOS) foundries, so as to lower the costs of productions. However, as mentioned before the widely used Au-based contacts in InAlN/GaN devices, gold acts as a deep level and also a fast diffuser in silicon and is therefore strictly forbidden in Si fabs. Therefore, the development of CMOS-compatible metallization with a sufficiently low contact resistance in InAlN/GaN HEMTs is crucial to enable the processing of these devices in Si foundries. Gold is believed to prevent the oxidation of the metal surface during the rapid thermal annealing process and decrease the total contact resistance. Some experiments have, however, attributed the long-term degradation of ohmic

contacts to gold diffusion [68]. Therefore, a Au-free metallization scheme would also help to enhance the long-term contact reliability.

Traditionally, GaN based HEMTs and MOS-HEMTs are fabricated using a gate-last process, where the source/drain contacts are deposited and annealed before the gate contact or gate stack formation. This is different from the Si process, which is usually gate-first, where the gate stack is formed before the source/drain contacts. The gate-last process allows high thermal budget for the formation of good source/drain ohmic contacts, and at the same time, the preservation of the metal-semiconductor Schottky contact in HEMT (as high temperature anneal can degrade the properties of Schottky contact) or the use of various high-k dielectrics without the risk of recrystallizaion in MOS-HEMT (which can lead to higher gate leakage). In the gate-last process, Ti/Al based contacts with gold (e.g., Ti/Al/Ni/Au) are typically used, and after the necessary high temperature annealing (~ 800 ^{o}C) for good ohmic contact formation, they have rough surface morphology and edges [57] which could cause reliability issues. In addition, the gate-last process also limits the minimum source-to-gate distance (necessary distance or gaps are needed between gate and source/drain for gate alignment), which makes it difficult to achieve low source access resistance [53]. On the other hand, the gate-first process provides the possibility of self-alignment source/drain contacts to the gate stack, thus reducing drastically the source and drain access resistance. Although the gate-first process shows the advantage and capability for device scaling down, the high thermal budget of the widely accepted Ti-based contacts (e.g., Ti/Al/Ni/Au) can degrade the properties of the gate stack. In other

words, source/drain contacts with low thermal budget are desirable for the gate-first process.

In this thesis, one focus of the research is the evaluation and development of different ohmic contact schemes to achieve gold free and lower thermal budget for the compatibility of GaN based device fabrication in silicon foundries. More specifically, firstly for the preliminary studies, the gold-free Ti/Al contact on n-GaN, where a two-step annealing process, involving an initial annealing at low temperature followed by a second annealing at high temperature was studied. Afterwards, another preliminary study was to explore the transition metal hafnium (Hf) as ohmic metal for the replacement of Ti. The workfunction of Hf (3.9 eV) is less than that of Ti (4.33 eV). Hence, it may be advantages to replace Ti by Hf in the Ti-based contacts, e.g., Ti/Al/Ni/Au. On the other hand, a higher enthalpy for Hf nitride formation (-369.03 kJ/mol) than that of Ti (-347.2 kJ/mol), indicates Hf nitride is more thermodynamically favorable than TiN. Thus, Hf with a low workfunction and large negative value of nitride heat formation are probably a promising candidate to low thermal budget for GaN based devices. Secondly, after the preliminary study of the ohmic contacts on n-GaN, we will focus on Hf based and its other transition counterparts on InAlN/GaN and carry out a comprehensive study including material selection, optimization and physics of Au-free ohmic contacts with low thermal budget. Thirdly, a systemic comparison between the optimized Au-free contacts and traditional Ti/Al/Ni/Au contacts will be conducted in terms of morphology, microstructure, and device performance.

Another focus is to look into the lanthanum aluminate ($LaAlO_3$) as passivation for

InAlN/GaN HEMTs. Surface passivation by $LaAlO_3$ is studied as an alternative to Al_2O_3 and SiN passivation, since $LaAlO_3$ has high thermal stability (> 900 ^oC), and immune against moisture in the environment [69]. Therefore, the second focus for the current project was to preliminarily evaluate the feasibility of $LaAlO_3$ as a passivation layer in InAlN/GaN HEMTs.

Hence, with the objectives and overview of the project described above, this thesis is organized as follows.

Chapter 2 gives a brief introduction to the physics of ohmic contact, the operation principles and surface states of GaN based HEMTs. The fabrication and characterization techniques used in this work are also described. This chapter provides the theoretical background and experimental fundamentals to this project.

In Chapter 3, the preliminary investigations of ohmic contacts on n-GaN are first presented. To achieve Au-free contact with good surface roughness, the first evaluation of feasibility for Ti/Al ohmic contacts with a two-step annealing processing are described here. And later the characteristics of Hf-based ohmic contacts on n-GaN compared to Ti-based contact are also shown in this chapter.

In Chapter 4, a thorough study for Hf-based ohmic contacts on InAlN/GaN has been carried out here. For Hf-based contacts on InAlN/GaN, the comparison with other transition metals based contacts is conducted and the optimization of the Hf/Al thickness ratio is also performed. Furthermore, the contact formation and carrier transport mechanisms are investigated to reveal the physics of Hf/Al/Ta contacts.

In Chapter 5, the comparison between InAlN/GaN HEMTs with Hf- and Ti-based contacts is performed with respect to the ohmic contacts surface morphology, microstructure, DC performance and breakdown voltage.

Chapter 6 provides the preliminary study and evaluation for $LaAlO_3$ passivated InAlN/GaN HEMTs with Hf/Al/Ta contacts.

Lastly, in Chapter 7, a summary of this work is provided, followed by a suggestion of the potential research to further development of InAlN/GaN HEMTs.

Chapter 2

Physics in GaN-based devices, fabrication and characterization techniques

This chapter provides the theoretical background of the study and also describes processes and apparatus that are employed for device fabrication and testing throughout this thesis. Section 2.1 focuses on the theory of metal-semiconductor contact, operation principle of GaN HEMTs, and effects of surface states in GaN HEMTs. Section 2.2 describes the material structures and fabrication techniques used in this thesis. After that, several important characterization techniques used in this work are briefly described in Section 2.3, including transmission line method (TLM), Hall Effect measurement, secondary ion mass spectrometry (SIMS), transmission electron microscopy (TEM), X-ray diffraction measurement (XRD), and atomic force microscopy (AFM).

2.1 Physics in GaN-based devices

2.1.1 Metal-semiconductor contacts

The model for metal-semiconductor contact formation [70] demonstrated first by Schottky and Mott has the basic assumption that the barrier at the metal/semiconductor interface is a function of the difference between the work function of the metal and the electron affinity of the semiconductor. The Schottky barrier height (SBH) between the metal and n-type semiconductor is defined by

Eq. (2.1), where Φ_b, Φ_m and χ_s, are the SBH, the metal work function, electron affinity of the semiconductor, respectively.

$$\Phi_b = \Phi_m - \chi_s \tag{2.1}$$

When a weak dependence of the Schottky barrier on the work function of the metal was demonstrated, Bardeen established another model (the surface or interface state model) for the metal-semiconductor contact formation. In this model, due to a large number of surface or interface states (>10^{12} states cm^{-2}), the Fermi level could be pinned and the SBH is totally independent of the work function of the metal. The SBH is subsequently expressed as the Bardeen limit, as given by Eq. (2.2), where Φ_0 is the neutral level and E_g is the semiconductor bandgap.

$$\Phi_\mathrm{b} = \mathrm{E_g} - \Phi_0 \tag{2.2}$$

However, resulting from the large amount of ionic bonds, metal-GaN related semiconductor contacts show a relatively strong correlation of the barrier height with the contact metal work function instead of surface states. As shown in Figure 2.1, Kurtin et al [71] showed a plot of index of interface behavior versus the difference in electronegativity of constituent elements for different compound semiconductors to evaluate such kind of relationship. GaN and AlN has a Pauling electronegativity difference of above 1.0 [72], which means barrier height is mainly dependent on the difference between metal and GaN workfunction. In other words, the Fermi level pining effect does not affect much the properties of these ohmic contacts.

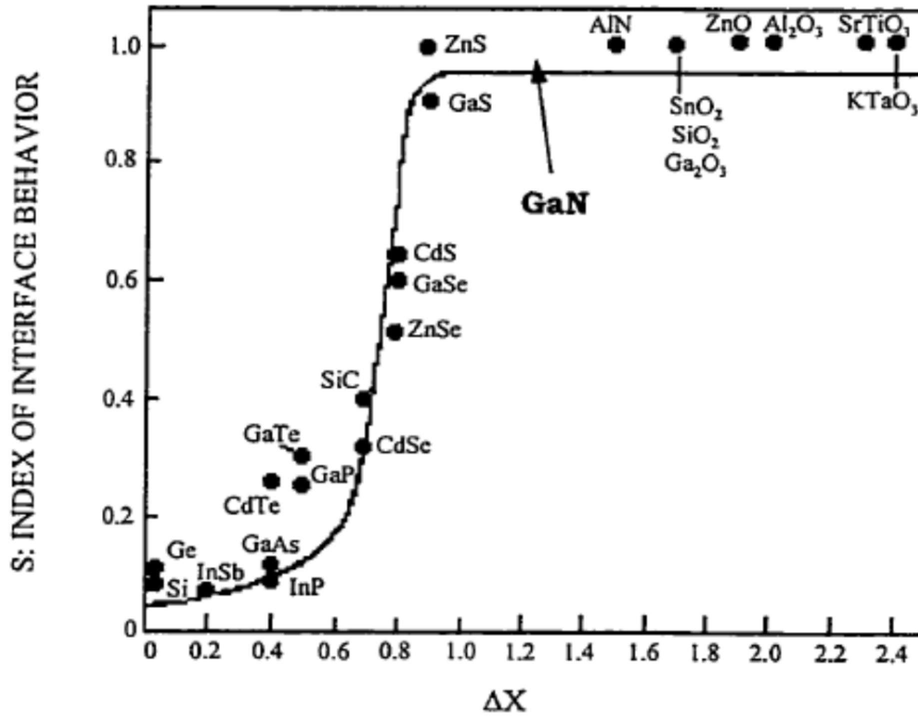


Figure 2.1 Index of interface behavior of various semiconductors (S) versus the difference in electronegativity of their constituent elements (ΔX) [71]. **S** is the pinning factor which is inversely proportional to the Fermi-level stabilization at the semiconductor-metal interface.

The carrier transport mechanisms for a metal–semiconductor (n-type) are depicted in Figure 2.2 [73]. For lightly-doped semiconductors, the current flows as a result of thermionic emission (TE), namely electrons thermally excited over the barrier shown Figure 2.2 (a). In the intermediate doping range, thermionic-field emission (TFE) dominates with carriers thermally exited to a certain energy level where the barrier is sufficiently narrow for tunneling to take place. For high doping concentration, the barrier is sufficiently narrow at or near the bottom of the conduction band for the electrons to tunnel directly, known as field emission (FE). The three regimes can be differentiated by calculating the characteristic energy E_{00} defined by

$$E_{00} = \frac{qh}{4\pi}\sqrt{\frac{N}{m^{*}\varepsilon}} \quad (2.3)$$

where N is the carrier concentration, m^* is the effective mass of carrier. Normally, a comparison of E_{00} with respect to the thermal energy kT shows thermionic emission to dominate for $kT >> E_{00}$, for thermionic-field emission $kT \approx E_{00}$ and for field emission $kT << E_{00}$. For simplicity, we can consider for TE, $E_{00} \leq 0.5\ kT$; for TFE, $0.5\ kT < E_{00} < 5\ kT$; and for FE, $E_{00} \geq 5\ kT$.

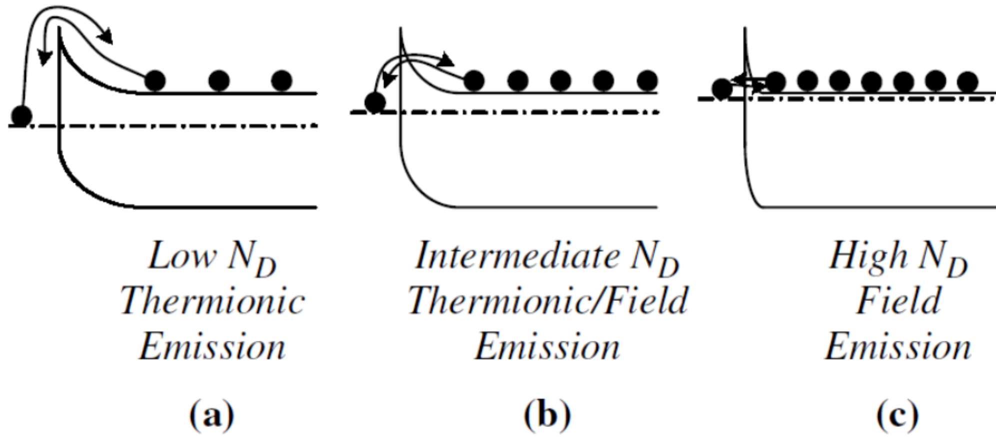


Figure 2.2 Ohmic contacts to n-type semiconductor with different doping concentrations [73].

2.1.2 Operation principle of GaN HEMTs

The most important feature of GaN HEMTs is the high sheet concentration and mobility of carriers confined at the interface of the heterostructure, which is induced by the strong spontaneous and piezoelectric polarization effect in GaN based materials. Figure 2.3 portrays the conduction band diagram of the

InAlN/GaN heterostructure with an AlN spacer and the formation of 2DEG. A heterojunction will be formed due to two semiconductors (e.g., InAlN/GaN) with different bandgaps joined together so that conduction band offset inevitably take place. Thus, this conduction band offset results in a triangle quantum potential well at the heterostructure interface, as shown in Figure 2.3. The electrons induced by the polarization effect will accumulate in this potential well and form a sheet charge, similar to the case of inversion channel in Si based MOFETs. The thickness of this channel is typically only several nanometers, which is much smaller than the de Broglie wavelength of the electrons in GaN given by $\lambda = h/\sqrt{2kTm_n^*}$, where m_n^* is the effective electron mass of GaN, h is the Plank constant, k is the Boltzmann's constant and T is the temperature. Hence, the electrons are quantized in a two-dimensional system at the interface, and the channel is in the form of a 2DEG.

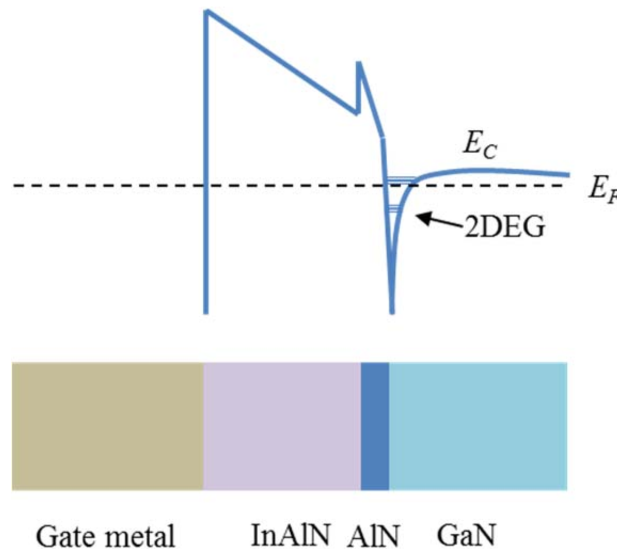
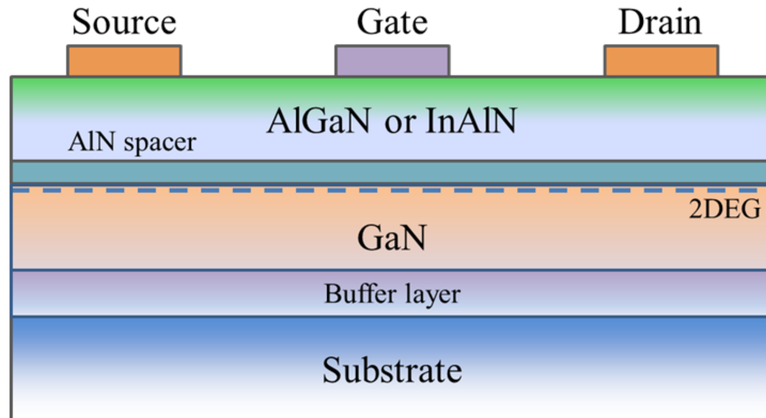
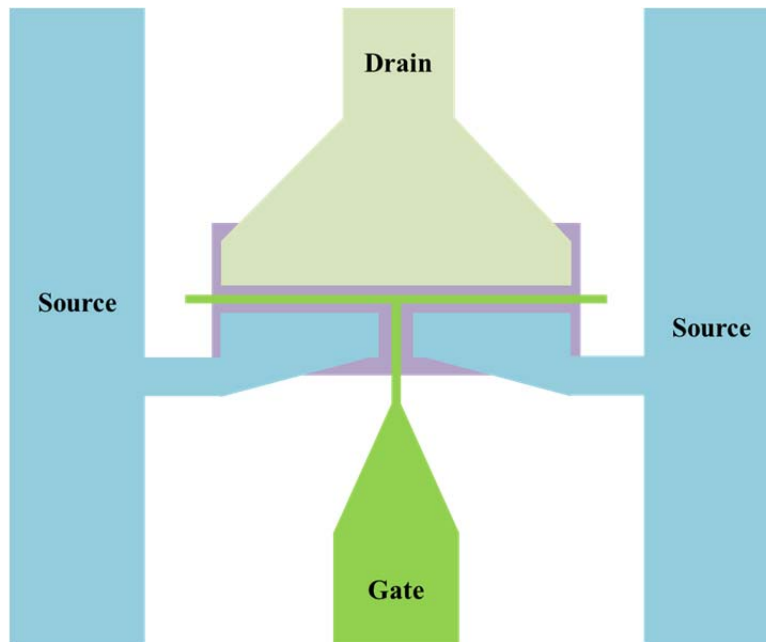


Figure 2.3 Conduction band diagram of InAlN/GaN heterostructure with an AlN spacer.

Figure 2.4 illustrates a schematic showing the cross section and top view of a typical GaN based HEMT structure in this study. Both the source and drain terminals are ohmic contacts, which provide the path of carrier flow in the



(a) Cross section



(b) Top view

Figure 2.4 Cross section and top view of the conventional AlGaN/GaN or InAlN/GaN HEMTs.

direction parallel to the InAlN/GaN heterojunction. The source is typically grounded while a positive bias is applied to the drain, thus driving the carriers in

2DEG channel to flow from source to drain. The applied voltage between the drain and source is named V_{DS}, while the gate-to-source voltage is named V_{GS}. The gate electrode can be either a metal-semiconductor rectifying contact (i.e., Schottky barrier contact) or metal oxide stack (i.e., MOS structure). The gate is used to modulate the conductivity of the 2DEG channel, since it can affect the field distribution of heterostructure below the gate and reduce or increase the carrier concentration through the application of a bias. By applying an appropriate gate bias, carriers in the channel can be fully depleted, and thereby no current canpass between the source and drain. The gate bias required to pinch-off the channel is termed the threshold voltage (VTH). If the threshold voltage is negative, the device is depletion-mode (D-mode); while the threshold voltage is positive, the device is enhancement-mode (E-mode). In this thesis, we focus on the traditional GaN HEMTs, namely the D-mode devices, which imply the channel is normally on and the gate is negatively biased.

2.1.3 Effects of surface states in GaN HEMTs

In InAlN/GaN or AlGaN/GaN heterostructures, polarization-induced charges constitute a dipole whose net contribution to the total space charge is exactly zero, which leads to the facts that the polarization-induced charges alone are not able to form the 2DEG channel. For a truly undoped barrier, it follows that any 2DEG electrons are due to donor-like surface states [74]. In other words, ionized donor-like surface states can give rise to positive charges, which forms the 2DEG

channel in the GaN based heterostructures based on the charge neutrality conditions. Therefore, the surface states have a very crucial impact on the performance of GaN based HEMTs.

Historically, the impact of surface states on device performance, known as current dispersion or current collapse [75], was first observed and studied in AlGaN/GaN HEMTs. If the positive charges are not enough or are neutralized, a depletion of 2DEG is resulted proportional to the charge imbalance on the surface. In the case of device operation, the 2DEG channel will be depleted and an extension of the gate depletion region could be created, as shown in Figure 2.5 [33].

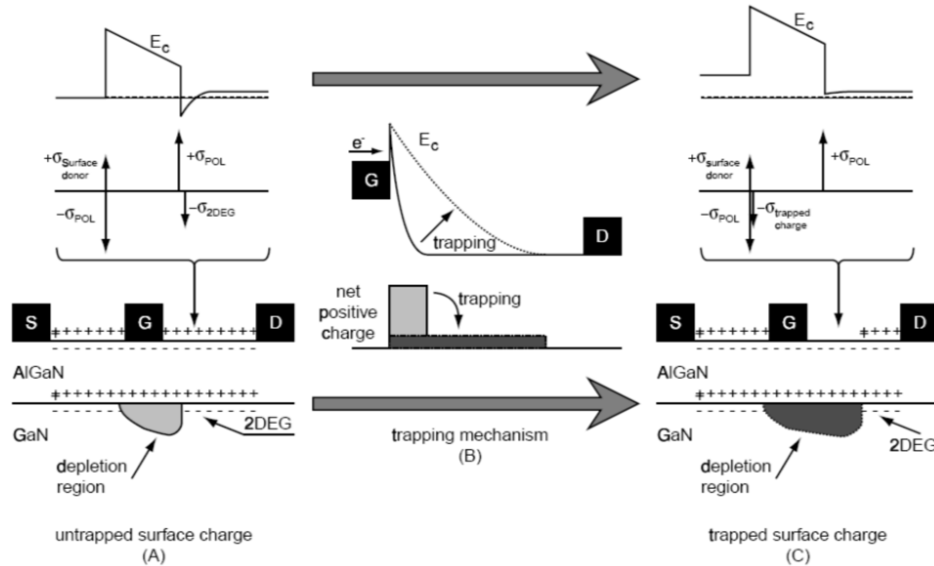


Figure 2.5: The mechanism of current dispersion in AlGaN/GaN HEMTs: (A) device at off-state condition without trapped surface charges; (B) trapping mechanism: electrons leaking from the gate get trapped on the surface deep donor, thus reducing the net positive surface charge. Gate-drain depletion region extend toward the drain, also lowering the peak electric field; (C) device at off-state condition with trapped surface charge: due to the charge compensation induced by the trapped electrons, 2DEG density is reduced. When the device is turned on, electrons trapped on the surface cannot respond immediately due to their long time constant for de-trapping process. Consequently, 2DEG density in the gate-drain access region is lower than its equilibrium value, inducing an increase in the parasitic drain access resistance.

Although this issue is still not fully understood, a model in terms of virtual gate was proposed by Vetury et al [33] , which has been widely accepted to explain the phenomena of current collapse in GaN HEMTs. In this model, an extension of the gate depletion region will be formed due to the trapped surface charges, as shown in Figure 2.5. Hence, the effect of surface negative charges is to act like a negatively biased metal gate, as shown in Figure 2.5. Namely, it seems that there exist two gates on the surface, between the source and drain, connected in series as shown in Figure 2.6.

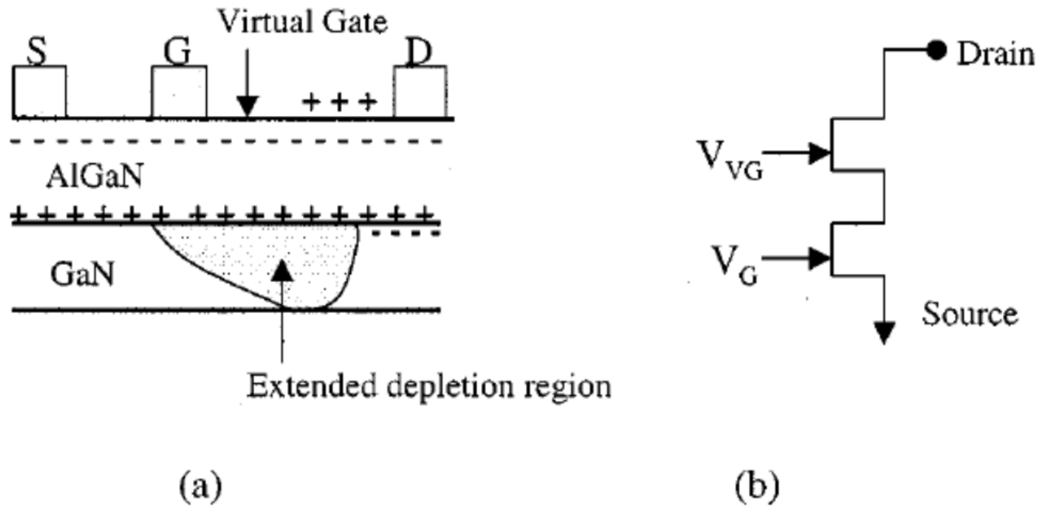


Figure 2.6 Model of the device showing (a) the location of the virtual gate, and (b) schematic representation of the device including the virtual gate. [33]

2.2 Device fabrication techniques

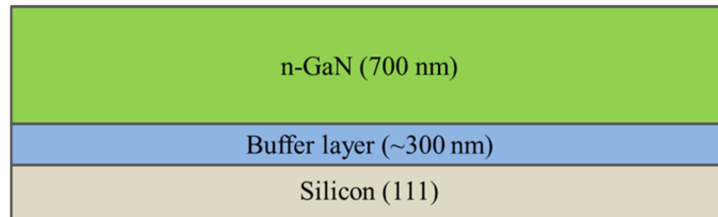
2.2.1 Material structure

Three types of epi-wafers (n-GaN and InAlN/GaN, as shown in Figure 2.7) were used in the current work and were purchased from NTT AT, Japan. They were grown using metal-organic chemical vapor deposition (MOCVD) on highly

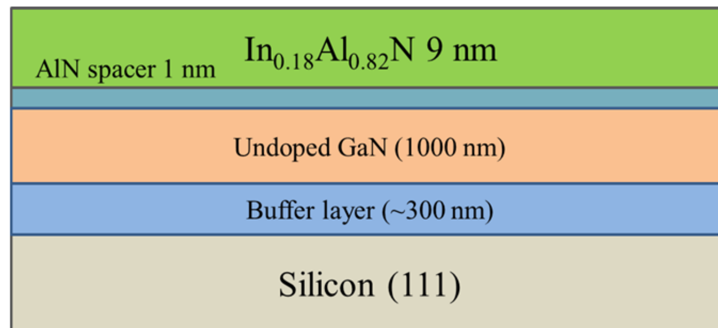
resistive silicon (111) substrate (> 6000 Ω·cm). The electrical properties of these wafers were characterized by Hall measurements at room temperature (RT). The carrier concentration (n_s) and mobility (μ) for both structures are summarized in Table 2.1.

For the n-GaN structure, as shown in Figure 2.7 (a), the epitaxial layers consist of (from bottom to top), a ~300 nm buffer layer and 700 nm n-GaN with Si doping concentration of 5×10^{18} cm^{-3}.

For the InAlN/GaN HEMT structure, as shown in Figure 2.7 (b), the epitaxial layers consist of (from bottom to top), a ~300 nm buffer layer, 1000 nm GaN channel layer, 1 nm AlN spacer, and 9 nm $In_{0.18}Al_{0.82}N$ barrier.



(a) n-GaN



(b) InAlN/GaN Heterostructure

Figure 2.7 Schematic cross sections for both the n-GaN and InAlN/GaN epitaxial wafer structure.

Table 2.1 Electrical Properties of n-GaN and InAlN/GaN wafer in this study.

Material	Wafer Structure	Carrier Concentration	Mobility ($cm^2/V \cdot s$)	Sheet Resistance (Ω/□)
n-GaN	(a)	3.5×10^{18} cm^{-3}	220	84.38
InAlN/GaN	(b)	1.2×10^{13} cm^{-2}	1112	458
InAlN/GaN	(b)	2.1×10^{13} cm^{-2}	833	360

2.2.2 Sample preparation

Sample preparation started with cutting the n-GaN and InAlN/GaN wafers into small pieces by scribing the backside of the wafers with a diamond blade. The resulting samples were cleaned in a standard surface degrease process with sequential cleaning by acetone, followed by isopropyl alcohol (IPA). All the organic solvent cleanings were conducted in an ultrasonic bath for 10 min to remove organic contaminations on the surface. The cleaning procedure was completed with a thorough rinsing of the sample in deionized (DI) water and then blown dry by nitrogen gun. Prior to the metal deposition, the sample was dip-etched by HCl: H_2O (1:10) solution for 15 s to remove the native oxide on the surface.

2.2.3 Device isolation

Conventional wet etching techniques used in traditional semiconductor processing have not been successful for GaN device fabrication owing to its chemical stability. For example, Maruska and Tietjen [76] reported that GaN is insoluble in H_2O, acids or bases at room temperature, but does dissolve in hot alkali solution

at very slow rates. For GaN-based devices, ion implantation and mesa structure are normally used to realize the isolation for different device and testing structures between one another to avoid wet etching processing. In our study, the mesa isolation method was employed since it is much simpler than the ion implantation isolation. The mesa height needs to be carefully chosen to prevent leakage current between adjacent devices or testing structures. Mesa heights should be chosen carefully for device isolation as the current barrier effectively, and to prevent any possible discontinuity between the gate finger and gate pad across the mesa step [77]. Due to the resistance of GaN-based material to chemical acids, dry etching by inductively coupled plasma-reactive ion etching (ICP-RIE) was used to form mesa isolation. In this study, Plasmalab System 100 Cobra III-V Etcher from Oxford instrument was used to etch the substrate, which has a 600 W, 13.56 MHz RF power source coupled to a solid state matching network. In the machine, the active electrode is equipped with a heater/chiller and is capable of operating at temperatures varying from 0 to 80 ^{o}C. For our study, the etching conditions are as follows: etchant chemistry: BCl_3/Cl_2 (20/10 sscm), processing chamber pressure: 10 mTorr, chiller temperature: 6 ^{o}C, ICP power: 100 W, and RIE power: 50 W. The average etching rate is ~22 nm/min for GaN.

2.2.4 Photolithography

In this study, the traditional photolithography was chosen to define the geometry of device and test structures. The photo resist AZ 5214E was used in the experimental procedure, which can be positive tone (comprising of novolak resin) or negative tone (comprising of naphthoquinone diazide as photoactive compound)

dependent on the post-baking process. The method of using AZ 5214E to form a negative pattern of a mask is called the image reversal process. The image reversal capability by AZ 5214E is realized by a special crosslinking agent working (above 110 ^{o}C) only in the exposed areas of AZ 5214E. The crosslinking agent together with exposed photoactive compound results in an insoluble material which becomes non-sensitive to light, while the rest of unexposed area still functions as a normal photoresist with positive tone. After an exposure without additional masking step required (known as flood exposure), these areas are dissolved in the AZ developer, however, the cross-linked areas after flood exposure remain to form the resultant pattern, which is the negative image of the mask pattern.

Normally, the image reversal process includes: 1) normal exposure with mask, 2) post baking in oven, and 3) flood exposure without any masking procedure. The most important parameter of the image reversal process is the reversal temperature. If the post-baking temperature is too low (< 110 ^{o}C), crosslinking agent would not work. On the other hand, if the reversal baking temperature is too high (> 130 ^{o}C), cross-linking would happen in the unexposed area as well under high temperature, thus giving no pattern formation. The optimization should be done carefully to keep the reversal baking temperature within ± 1 ^{o}C. In the study, we used AZ 5214E photoresist as both a positive resist and a negative resist.

The experimental procedures for our photolithography are listed as follows. After the sample cleaning, the photoresist is spin-coated to the wafer surface with a constant spinning speed at 500 rpm for 30 s. This results in a thickness of ~1.5 μm.

After the spin coating step, the sample is soft-baked at 105 ^{o}C for 1 min on the hotplate to remove the solvent from the resist and to increase resist adhesion to the wafer. Then, the sample is aligned with respect to the mask in a Karl Suss MA6 aligner machine using hard contact mode. The photoresist is exposed to the UV light (~4 W/cm^2) for 10 s. After the first exposure, the sample is post-baked at 110 ^{o}C for 5 min in an oven, followed by a flood exposure for 40 s (optional). Lastly, the sample is developed in diluted AZ developer with DI water (1:1) for 50 s, then rinsed in DI water for 10 cycles and dried by nitrogen gun.

2.2.5 Metallization

Metallization schemes for the ohmic and gate contacts were deposited by two techniques: electron beam (e-beam) evaporation and DC magnetron sputtering, respectively. A BOC Edwards multi-hearth e-beam evaporator was used for many of the depositions. The equipment is capable of 3 kW, has a rotating sample stage and a four-stage hearth with each crucible being 4 cc in capacity. High purity metals are added to graphite crucibles as metal sources.

A Denton vacuum system, with DC magnetron heads, each able to hold a circular 2 × 0.125 inch target was used for sputter deposition. The transition metals that require sputter deposition were Ti, Al, Hf, Ta, Zr, Nb and V. All the sputtering targets were purchased from Kurt J. Lesker Company, except the Hf target, which was from KAMiS Company. The sample was secured to a sample holder, which was placed on a rotating stage during the deposition. The metal deposition was

conducted at a power of ~200 W, pressure of 4.2×10^{-2} Torr and flow rate of 10 sccm using working gas Ar at room temperature.

Table 2.2 Different metal deposition rates for electron beam evaporation and sputtering in this study.

Electron Beam Evaporation		
Metal	Beam current (mA)	Deposition Rate (nm/s)
Ti	~75	~0.11
Al	~70	0.2-0.4
Ni	~125	~0.12
Au	~102	0.2-0.3
Sputtering		
Metal	Power (W)	Deposition Rate (nm/min)
Ti	200	~21
Hf	200	~32
Ta	200	~18.2
Zr	200	~30.9
Nb	200	~21.5
V	200	~12.7
Al	200	~23.8
W	200	~20.3

2.2.6 Lift-off technique

In the study, the lift-off process was used for patterning deposited metal films, which refers to the creating pattern of a target material on the surface of a substrate by means of using a sacrificial material. In this thesis, the substrate is n-

GaN or InAlN/GaN wafer and the sacrificial material is AZ 5214E photoresist. Lift-off process was conducted after the metal deposition by e-beam evaporator or sputtering. During the lift-off process, the remaining photoresist would dissolve in acetone in an ultrasonic bath, effectively lifting-off the metal layer on top of it, thus forming the desired metal pattern. The details about lift-off process are shown in the following Figure 2.8.

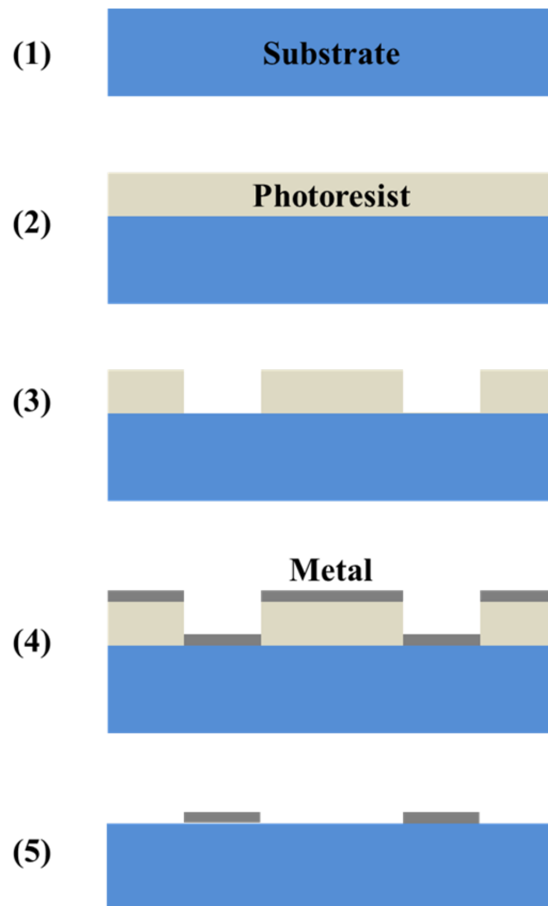


Figure 2.8 Lift-off technique: (1) before photoresist coating, (2) after photoresist coating, (3) after exposure and development, (4) after metal evaporation, (5) removal of photoresist and lift-off of metal, and (6) metal pattern formation after DI water clean.

2.2.7 Thermal annealing

Thermal annealing is used to realize ohmic contacts or to improve their electrical properties. The annealing ambient can be vacuum, nitrogen or air. If vacuum is used, the pressure is pumped down to 5×10^{-5} Torr. The equipment used in this study is ULVAC MILA-3000 Mini-lamp annealing system. The temperature ramping rate is normally set to about 10 ^{o}C/s.

2.2.8 Passivation

The device passivation for HEMT devices in this study was realized by pulsed laser deposition (PLD) technique. PLD is thin film deposition method that based on material ablation by a pulsed laser source. The target material is evaporated and deposited as thin film on the substrate by high-power laser pulses. Laser pulses are absorbed by the solid surface of target leading to rapid evaporation of the target materials. The ejected matters expand into surrounding vacuum consist of highly excited and ionized species in the form of plume. The plume expands away from the target with a strong forward-directed velocity distribution of different particles. The evaporated species finally condense on the substrate placed opposite to the target. Figure 2.9 shows the main components of a typical PLD system. As shown, there are several components of such a PLD system: 1) a target holder and a substrate holder in a vacuum chamber; 2) a high power laser source to produce laser beam focused by a set of optical components and guided through a quartz window into the chamber and onto the target surface; 3) a gas flow controller to provide the working gas during the process.

In this thesis, $LaAlO_3$ thin film was deposited using PLD as a passivation layer in InAlN/GaN HEMTs. Specifically, the samples were loaded into a PLD growth chamber with a base pressure of 1×10^{-8} Torr, where the LAO deposition was performed using a pulsed KrF excimer laser (λ = 248 nm, pulse duration = 30 ns) as the ablation source. Prior to the deposition, the sintered LAO target (purity = 99.9%, diameter = 1 inch) was cleaned by laser ablation under the deposition atmosphere with 500 laser pulses to remove possible surface contaminates and ensure a homogeneous surface morphology. The PLD parameters were fixed at: pulse energy of 180 mJ, repetition rate of 5 Hz, target-to-substrate distance of 6 cm, and a substrate temperature of 300 °C. The oxygen partial pressure of 2.7×10^{-4} Torr was chosen for the LAO deposition.

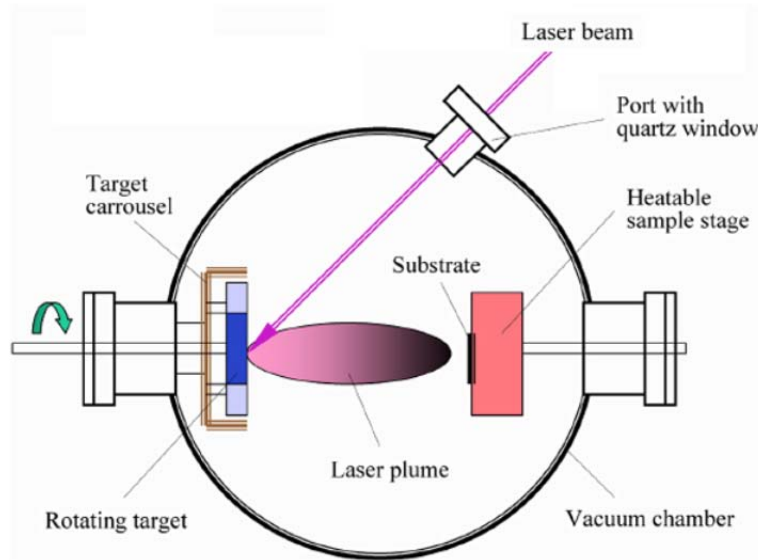


Figure 2.9 The basic setup of a typical pulsed laser deposition (PLD) machine [78]

2.3 Characterization methods

2.3.1 Transmission line method (TLM)

Transmission line method (TLM) is a universal technique to study contact electrical properties and extract sheet resistance of substrate, contact resistance and specific contact resistivity. In this study, we first used circular transmission line method (CTLM) to study the ohmic contact on n-GaN, since it requires no mesa isolation and makes the processing simple.. For the contact on InAlN/GaN heterostructure, we used linear transmission line method to extract both the contact resistance and contact resistivity, which provides more accurate results than CTLM. However, this requires mesa isolation, thus more involved processing.

Circular Transmission Line Method (CTLM) test structure [79] is used in our experiments to measure the specific contact resistivity of ohmic contacts to GaN. A typical circular test structures consists of a conducting circular inner region of radius *L*, a gap of width *d*, and a conducting outer region, as shown in Figure 2.10. The conducting regions are metallic and the gap typically varies form a few microns to tens of microns. For equal sheet resistances under the metal and in the gap, and for the geometry of the circular contact resistance structure in Figure 2.10, the total resistance (R_T) between the internal and the external contacts is

$$R_T = \frac{R_{sh}}{2\pi}\left[\frac{L_T}{L}\frac{I_0(L/L_T)}{I_1(L/L_T)} + \frac{L_T}{L+d}\frac{K_0(L/L_T)}{K_1(L/L_T)} + \ln\left(1+\frac{d}{L}\right)\right] \qquad (2.4)$$

where R_{sh} is the sheet resistance of the substrate, L_T is the transfer length, and *I* and *K* denote the modified Bessel functions of the first order. For $L >> 4L_T$, the Bessel function ratios I_0/I_1 and K_0/K_1 tend to unity and R_T becomes

$$R_T = \frac{R_{sh}}{2\pi}\left[\frac{L_T}{L} + \frac{L_T}{L+d} + \ln\left(1 + \frac{d}{L}\right)\right] \quad (2.5)$$

In the circular transmission line test structure in Figure 2.10, for $L >> d$, Eq. (2.5) simplifies to

$$R_T = \frac{R_{sh}}{2\pi L}(d + 2L_T)C \quad (2.6)$$

where C is the correction factor

$$\mathrm{C} = \frac{L}{d}\ln\left(1 + \frac{d}{L}\right) \quad (2.7)$$

For $d/L \ll 1$, Eq. (2.7) becomes

$$R_T = \frac{R_{sh}}{2\pi L}(d + 2L_T) \quad (2.8)$$

From Eq. (2.8), a linear relationship is seen between R_T and d. If we plot R_T versus d, a straight line will be obtained and it intercepts the R_T-axis at $R_0 = \frac{R_{sh}L_T}{\pi L}$ and has a gradient of $g = \frac{R_{sh}}{2\pi L}$. Since the transfer length is $L_T = \sqrt{\rho_c/R_{sh}}$, the specific contact resistance can be determined as follows,

$$\rho_c = R_{sh}L_T^2 = \pi L\, R_0^2/(2g) \quad (2.9)$$

Eq. (2.9) can be used for calculating the specific contact resistance (ρ_c), since R_0, and g can be measured directly.

Figure 2.10 Circular transmission line method test structure with various spacing d and same radius L. The brown areas indicated metallic regions.

Another test structure to measure the contact resistivity and contact resistance is shown in Figure 2.11. It is the linear transmission line method (LTLM) [73] test structure, which comprises several contacts with different spacing between adjacent contacts. For contacts with $L \geq 1.5\ L_T$, the total resistance between any two contacts is given by

$$R_T = \frac{R_{sh} \times d}{Z} + 2Rc \approx \frac{R_{sh}}{Z}(d + 2L_T) \tag{2.10}$$

where the approximation resulting from not considering the current flow around the contacts has a form similar to Eq. (2.8).

The total resistance (R_T) is measured between adjacent contacts with various contact spacing. Similar to the CTLM, when we plot R_T versus d, a straight line will intercept R_T -axis at $R_0 = \frac{2R_{sh}L_T}{Z}$, with a gradient of $g = \frac{R_{sh}}{Z}$ and $L_T = \sqrt{\rho_c / R_{sh}}$. The specific contact resistance for LTLM test structure can be determined as follows,

$$\rho_c = R_{sh} L_T^2 = Z\, R_0^2 / (4g) \tag{2.11}$$

Thus, sheet resistance, contact resistance and specific contact resistivity can be extracted from the R_T-d plot, but no correction factor needs to be introduced for this method.

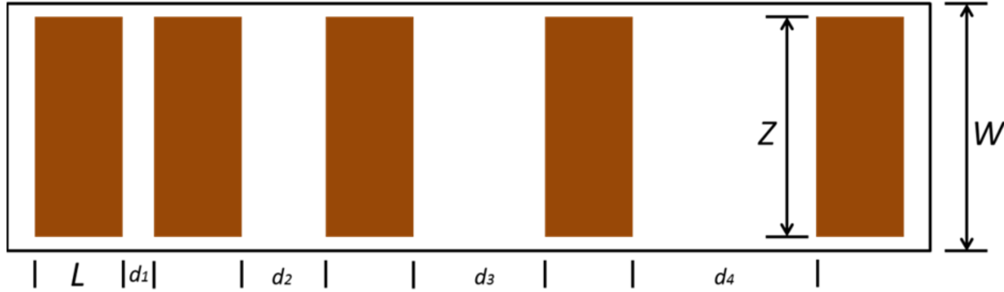


Figure 2.11 Linear transmission line method test structure with various spacing d and metal contact pad size L × Z.

In this study, the CTLM structure consists of ring patterns with an outer radius of 90 μm and different inner radii varying from 85, 80, 75, 65, 55, 45 μm. For the LTLM structure, it has several rectangular contact pads with a width of 200 μm and a length of 80 μm, and the spacing between contact pads varies from 5, 10, 15, 25, 35, 45, 60, 75, to 90 μm. In LTLM method, the unit of contact resistance is converted to Ω.mm, when it is normalized with respect to the width of contacts.

2.3.2 Hall Effect measurement

Since the Hall Effect was discovered, it has been widely used to determine the sheet resistance, mobility, carrier concentration and majority carrier type of a semiconductor material. Specifically, in a typical Hall measurement shown in Figure 2.12(a), when a constant current (I) is forced through the test sample within an orthogonal magnetic field (B), the free charge carriers (holes and

electrons) will experience a Lorentz force (F_L) = $q\ (v \times B)$, where v is the drift velocity of the carriers and q is the electronic charge. The carriers will flow in the opposite direction by the Lorentz force due to hole and electrons have opposite sign of charges. When either type of carrier is dominant, the accumulation of internal charge will induce a steady state Hall Voltage (V_H). To balance the magnetic and electrostatic forces on a single mobile charge, the following equation can be expressed

$$F_L = F_e = q\frac{V_H}{W} \tag{2.11}$$

The current can be calculated in terms of drift velocity,

$$\mathrm{I = n \times q \times v \times W \times t} \tag{2.12}$$

Where n is the density of charge carriers, $W\times t$ is the cross-section area through which the current passes through. The Hall coefficient R_H can be defined by the equations (2.11) and (2.12),

$$R_H = \frac{1}{n \cdot q} = \frac{V_H \cdot t}{I \cdot B} \tag{2.13}$$

Thus, the sheet Hall coefficient R_{HS} can be defined,

$$R_{HS} = \frac{R_H}{t} = \frac{V_H}{I \cdot B} \tag{2.14}$$

The sheet carrier concentration n_s can be calculated from the measured $R_{HS,}$

$$n_s = \frac{1}{q \cdot R_{HS}} \tag{2.15}$$

If the thickness t is known, the bulk carrier concentration can be given by $n = n_s/t$.

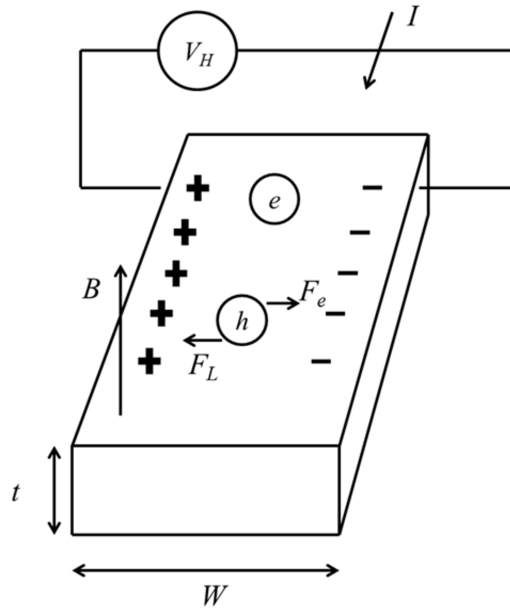
To measure Hall mobility (u_s), the sheet resistivity of under testing sample will be determined by van der Pauw's method, as shown in Figure 2.12(b). The current source is applied between contacts 1 and 2 and the voltage is measured between contacts 3 and 4, and we will obtain $R_{12,34}$. Similarly, the current source is applied between contacts 1 and 4, and the voltage is measured between contacts 2 and 3, and we will obtain $R_{14,23}$. The sheet resistivity ρ_s of under testing sample can be calculated,

$$\rho_s = 4.532 \times \frac{R_{12,34}+R_{14,23}}{2} \tag{2.16}$$

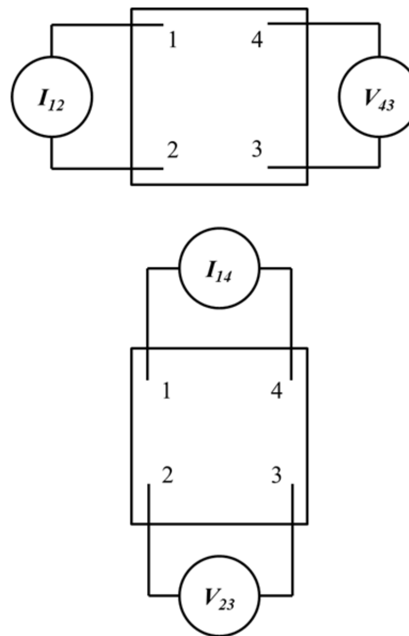
Thus, Hall mobility is calculated by

$$u_s = \frac{R_{HS}}{\rho_s} \tag{2.17}$$

In our experiment, a Bio-Rad HL5500PC Hall effect system was employed at room temperature to obtain the carrier concentration and mobility in n-GaN and InAlN/GaN heterostructure.



(a) Hall Effect schematic diagram



(b) van der Pauw contacts geometry

Figure 2.12 Schematic of the Hall Effect measurement: (a) Hall Effect schematic diagram and (b) van der Pauw contacts geometry

2.3.3 Secondary Ion Mass Spectrometry (SIMS)

Secondary Ion Mass Spectrometry (SIMS) is a well-known technique that can detect all elements, especially some elements in the 10^{14} to 10^{15} cm^{-3} range if there is very little background interference signal. The principle of SIMS shown in Figure 2.13 is based on the process of destructively remove materials from the sample by sputtering and the analysis of the ejected material by a mass analyzer. Most of the ejected matters are neutral so that those cannot be detected by normal SIMS, but some are positively or negatively charged. The mass/charge ratio of these ions is analyzed, resulted in a mass spectrum. The strength of SIMS is used to do quantitative depth profiling with one selected mass plotted as secondary ion yield versus sputtering time. In conventional SIMS, since electrostatic or magnetic spectrometer requires narrow slits for only those ions with the correct mass/charge ratio to be transmitted, the transmittance of the spectrometer significantly is reduced to values as low as 0.001%. However, the time-of-flight SIMS (ToF-SIMS), consisting of pulsed ions from a liquid Ga+ gun with beam diameters as small as 0.3 µm, does not have this limitation in conventional SIMS system where a continuous ion beam is used for sputtering. Therefore, ToF-SIMS can increase ion collection by 10-50%, indicating a lower incident beam current and sputtering rate compared to other SIMS techniques, to improve the sensitivity. In our project, ToF-SIMS was used for studying the reaction and inter-diffusion of different contact metals before and after annealing to understand the contact formation mechanism.

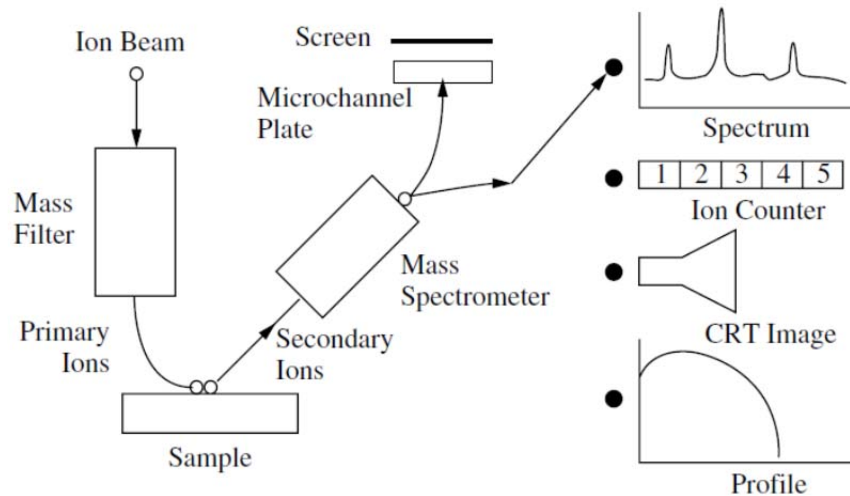


Figure 2.13 Schematic of a typical Secondary Ion Mass Spectrometry (SIMS) [73].

2.3.4 Transmission Electron Microscopy (TEM)

The transmission electron microscopy (TEM) is a powerful technique which is capable of imaging the materials in atomic scale resolution. Similar to the optical microscope, the TEM also consists of a series of lens to magnify the sample. However, the transmission electron microscope has higher resolution to approach 0.08 nm due to the smaller numerical aperture and shorter wavelength compared to the optical microscope. The schematic illustration of a typical transmission electron microscope is show in Figure 2.14. As shown, electrons generated from an electron source are accelerated by high voltage (normally 100 to 400 kV) and focused on the sample by a few sets of condenser lenses. The sample, placed on a small copper grid a few millimeters diameter, is intentionally prepared to be extremely thin (several tens to several hundred nm) to allow the electron beam to penetrate transparently and reduce the chance of spreading. The transmitted and

forward scattered electrons form a magnified image in the image plane and a diffraction pattern that indicating structural information in the back focal planet. The transmission electron microscope can operate in three modes, bright-field, dark-field and high-resolution mode (lattice imaging). Images formed with only the transmitted electrons are bright-filed images and images formed with a specific diffracted beam are dark-field images. Image contrast does not depend very much on absorption but rather on scattering and diffraction of electrons in the sample. Thus, dark-field images can provide a better image contrast. In scanning transmission electron microscopy (STEM), a fine electron beam (~0.1 nm in diameter) is rastered across the sample. The objective lens recombines the transmitted electrons from the region scanned by the probing electron beam to a fix area in the back focal plane. One of the main advantages of STEM over TEM is that it is capable of allowing using other signals that cannot be spatially correlated in TEM, since the primary electrons in an STEM system also produce secondary electrons, back scattered electrons, characteristic X-rays, electron energy loss and cathodoluminescence. In our project, we used TEM and STEM techniques to study the contacts before and after thermal annealing to evaluate the inter-diffusion and alloying among contact metals.

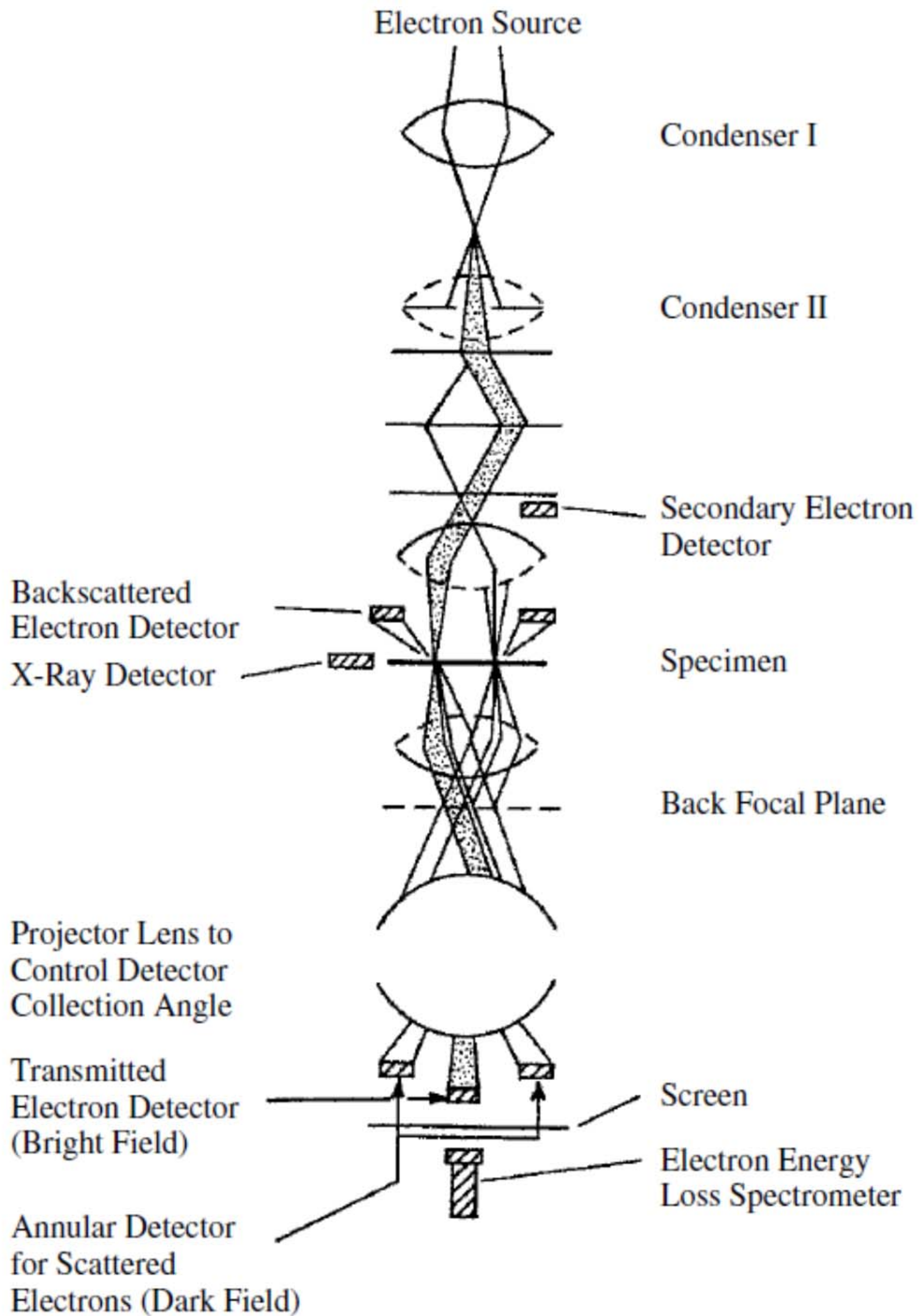


Figure 2.14 The principle of transmission electron microscopy (TEM) [73].

2.3.5 X-ray Diffraction (XRD)

X-ray diffraction (XRD) is a useful non-destructive technique for material characterization, which is able to identify material, crystalline quality, lattice constant, alloy phase and composition in the x-ray irradiated area.

The principle of XRD operation is based on the Bragg's law. We can express the relationship mathematically as follows.

$$2\sin\theta\, d_{hkl} = n\lambda$$

where d_{hkl} is the inter-planar spacing of any lattice planes with Miller indices {h k l}, θ is the relevant Bragg's angle estimated from the peak of the XRD spectrum, n is an integer, and λ is the wavelength of the X-ray radiation source. The relationship between lattice constants (a, b, c) and the plane spacing d_{hkl} can be precisely calculated based on {h k l} for different crystal structures (cubic, tetragonal, orthorhombic and hexagonal etc.). Thus, we can calculate the plane spacing, and thus the lattice constant by the Bragg angle θ and the X-ray wavelength. Accordingly, we can identify a particular phase by means of fitting both peak position and relative intensities which are corresponding to specific lattice plane and Miller indices of {h k l}. For hexagonal III-nitride materials, indices {h k i l} are normally used, where h + k + i = 0.

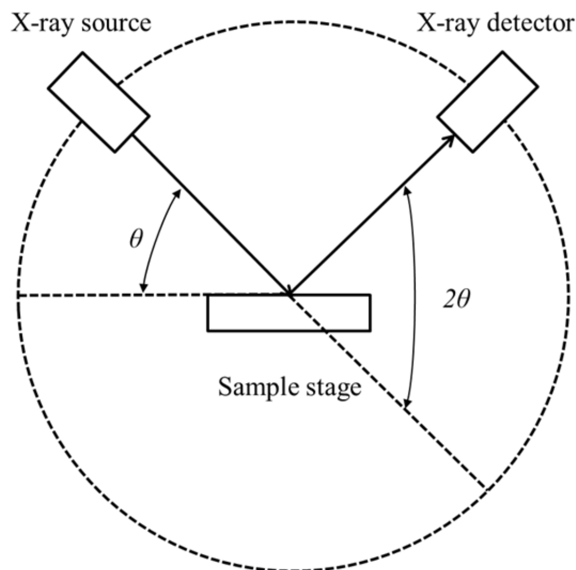


Figure 2.15 The principle of a typical X-ray diffraction system.

A typical schematic of an x-ray diffraction system is shown in Figure 2.15. As seen, the X-ray diffractometer has an X-ray source, a sample stage, an X-ray detector. The sample stage can rotate around the respective axe and also move along the x-y-z direction to position the sample. The x-ray source is usually generated from x-ray tubes, which consists of a metal target anode and a tungsten filament cathode with a high voltage between them. The filament is heated to emit thermal electrons, and the high electric field between the cathode and anode accelerates these thermal electrons towards the metal target. These high speed electrons will knock core electrons out of the metal target, and electrons in the outer orbitals relax to fill the vacancies, thus emitting x-rays. Afterwards, the x-ray exits the tube through monochromator. When the X-ray diffractometer is working, the X-ray beam is focused on the sample mounted on the stage at an incident angle θ, while an X-ray detector is placed on the opposite side 2θ away

from the incident path of. When the measurement is continued, the incident angle is increased over time while the detector angel always keeps 2θ above the source path to receive the signals. In our experiment, we used XRD to exam the phase formation and understand the reaction among contact metals and semiconductor substrate. The X-ray used in this study is Cu K-alpha with the wavelength of 0.15418 nm.

2.3.6 Atomic Force Microscope (AFM)

The Atomic Force Microscope (AFM) was used to study the surface morphology of our ohmic contacts, which is suitable for conducting as well as insulating sample. Its microscopy works by measuring the force between a probe and the sample, where the force depends on the property of the sample, the distance between the probe and sample, the probe geometry, and sample surface condition. As shown in Figure 2.16, a schematic of an AFM, a cantilever with a sharp tip mounted on its end is normally used, which could made from silicon, silicon oxide or silicon nitride. To measure topography, the tip will make contact with the sample continuously or by scanning across the sample surface. The piezoelectric scanner translates the signal which is correspondent to either the cantilever over the sample or the sample under the cantilever. A common technique used to sense the motion of the cantilever is to measure the light reflected from the cantilever in to a four-segment position sensitive photodiode. The cantilever motion causes the reflected light to impinge on different segment of the photodiode. Vertical motion is detected by $z = (A+C)-(B+D)$ and horizontal motion by $x = (A+B)-(C+D)$. Keeping the signal constant, equivalent to constant cantilever deflection, by

changing the sample height through a feedback arrangement, indicates the sample height variation. AFM can operate in three modes, contact mode, non-contact mode and tapping mode. In our project, we used AFM to exam the morphologies of contacts before and after thermal annealing.

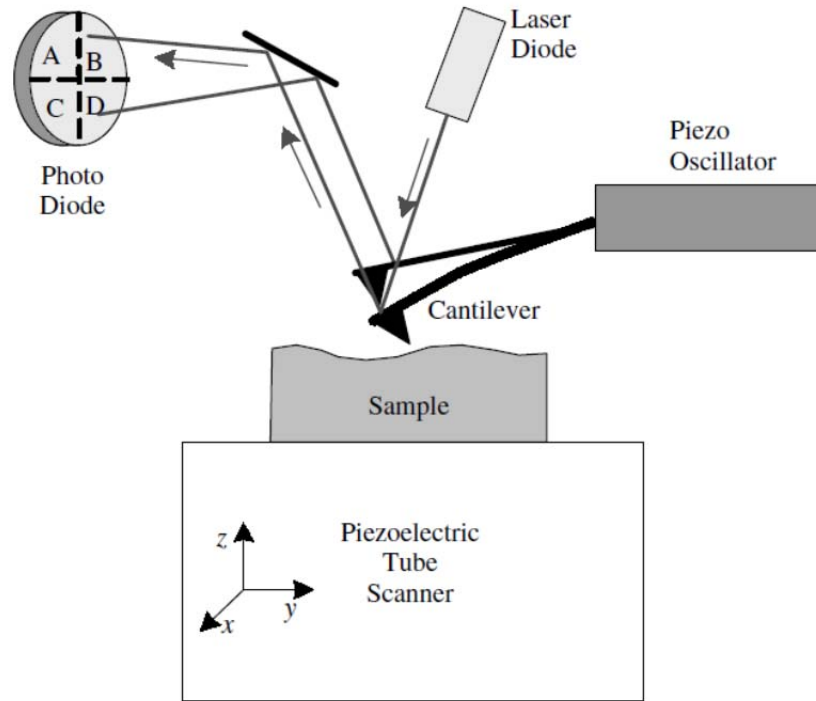


Figure 2.16 Schematic of an atomic force microscope [73].

Chapter 3

Preliminary Ohmic Contact Studies on n-GaN

As discussed in Chapter 1, a good ohmic scheme is playing a vital role in high performance GaN based HEMTs. One of the objectives of this thesis is to develop gold-free ohmic contact metallization with low thermal budget for the fabrication of GaN HEMTs in silicon foundries. In this chapter, the preliminary studies for ohmic contacts on n-GaN substrate will be presented and examined. First of all, in Section 3.1, our first attempt on Au-free contact is the Ti/Al bilayer without the Au capping layer. The Ti/Al bi-layer contact using a special two-step annealing process was evaluated. The special two-special annealing involves an initial annealing at low temperature (600 ^{o}C) followed by a second annealing at high temperature (700-900 ^{o}C) in vacuum. The electrical properties, surface roughness and contact formation mechanism for Ti/Al contacts with two-step annealing were also assessed. Afterwards, we report our first evaluation ohmic contact for low thermal budget purpose by introducing the Hf-based contacts. The preliminary comparison between Hf-based and the reference Ti/Al/Ni/Au contacts were also discussed.

3.1 Ti/Al ohmic contacts on n-GaN by two-step annealing processing

3.1.1 Introduction

Many experiments have been carried out to investigate the Ti/Al based ohmic contacts on GaN. Typically, Ti/Al covered by a diffusion barrier layer such as Ni [80], Ti [81] or Mo [82], and followed by a gold (Au) capping layer on the top (i.e., Ti/A/X/Au, where X is Ni, Ti, or Mo) is used in the GaN based devices for optoelectronic and power device applications. In order to obtain a low specific contact resistivity, the traditional ohmic contact scheme uses Au as a capping layer, which is helpful to prevent contact degradation resulting from oxidation. However, the surface morphology of the Au based ohmic contacts degrade after annealing due to the formation of Al–Au alloy phases caused by the melting of the alloy at low temperature (525 ^{o}C) [83]. This Al-Au alloy phase raises concerns about reproducibility or reliability issues, which may cause short circuit to electrical devices by the melting Al-Au alloys at elevated temperature. The other shortcoming of Au based contact is that it is highly diffusive in Si such that it is not compatible to the CMOS process in Si fabrication facilities. Hence, as an initiative of Au-free ohmic contacts, Ti/Al bilayer ohmic contacts on n-GaN are investigated. However, the contact resistivity of Ti/Al ohmic contact is not low enough compared to conventional Au-based ohmic contacts due to the fact that Ti/Al contact oxidizes easily. Its surface roughness degrades during high temperature annealing process since the melting point of Al is ~660 ^{o}C [84]. Recently, $TiAl_3$ has been reported as a reasonably good capping layer for the Ti/Al contacts [85]. Indeed, $TiAl_3$ is stable at high temperature and can be formed at around 500 ^{o}C [86]. In addition, $TiAl_3$ can be a good capping layer due to the formation of a very thin but continuous protective Al_2O_3 layer at the surface. In

this study, a two-step annealing process is utilized for the Ti/Al bilayer contact in order to obtain a top $TiAl_3$ layer first at a relatively low temperature (600 ^oC), lower than the melting point of Al, followed by a high temperature annealing to ensure low contact resistivity. Should the transformation to $TiAl_3$ layer be successful, the need for the deposition of a capping layer for the Ti/Al contact is eliminated. We will also examine if an improvement in surface roughness of the Ti/Al contact can be achieved using the two-step annealing process. The electrical properties, surface roughness and contact formation mechanism for Ti/Al contacts with two-step annealing has been evaluated and studied.

3.1.2 Experiment

In this section, the wafer structure of n-GaN wafers and cleaning process, native oxide removing, and photolithography has been discussed in Chapter 2. Metallization for Ti/Al was done by sputtering. Several Ti/Al ohmic schemes to n-GaN were considered by choosing different Ti/Al thicknesses/ratios, e.g., 30/60 nm, 30/90 nm, 30/120 nm, 30/150 nm and 30/180 nm, to fabricate the devices. For the two-step annealing, initial heat treatment was carried out in vacuum at 600 ^oC for 2 min followed by a second annealing at various temperatures in the range between 700-900 ^oC for 1 min in vacuum. We also fabricate Ti/Al contacts using one-step annealing without the first initial heat treatment for comparison. Current-voltage (I-V) characteristics were measured at room temperature using an Agilent B1500A semiconductor parameter analyzer. X-ray diffraction (XRD), time-of-flight secondary ion mass spectroscopy (ToF-SIMS) and atomic force microscope (AFM) were used in order to investigate the metallurgical reactions, roughness

and electrical properties for the Ti/Al contacts by one-step and two-step thermal treatments.

3.1.3 Electrical properties of Ti/Al contacts on n-GaN

Figure 3.1 shows a comparison in contact resistivity (ρ_C) between the two-step and one-step annealed samples with various Ti/Al thickness ratios (30/60, 30/90, 30/120, 30/150 and 30/180). First of all, for one-step annealed contacts, it is observed that ρ_C demonstrates a strong dependence on the Ti/Al thickness ratio. More specifically, ρ_C decreases with increasing Al content. Meanwhile, low Al content sample (e.g., Ti/Al ratio of 30/60) exhibits a small variation in ρ_C during annealing from 700 to 900 ^oC, while those samples with Ti/Al thickness of 30/90, 30/120 and 30/150 nm demonstrate a degradation trend at high temperature region. However, a ρ_C value as low as 2.66×10^{-6} $\Omega\cdot cm^2$ has been achieved for a Ti/Al thickness ratio of 30/180 nm, annealed at 850 ^oC.

On the other hand, two-step annealed samples demonstrate lower ρ_C values compared to those for one-step annealing for all Ti/Al thickness ratios. The samples with Ti/Al thickness ratios of 30/120 nm and 30/150 nm show a minimum ρ_C of 4.87×10^{-6} $\Omega\cdot cm^2$ and 4.9×10^{-6} $\Omega\cdot cm^2$, respectively while the minimum ρ_C value as low as 2.19×10^{-6} $\Omega\cdot cm^2$ is achieved for Ti/Al thickness ratio of 30/180 nm after the second-step annealing at 850 ^oC. Although the 30/180 nm Ti/Al contacts with one-step or two-step annealing exhibit lower ρ_C than either the 30/120 nm or 30/150 nm Ti/Al contact with two-step annealing, it is seen in Figure 3.2 that the surface morphology of the former is worse.

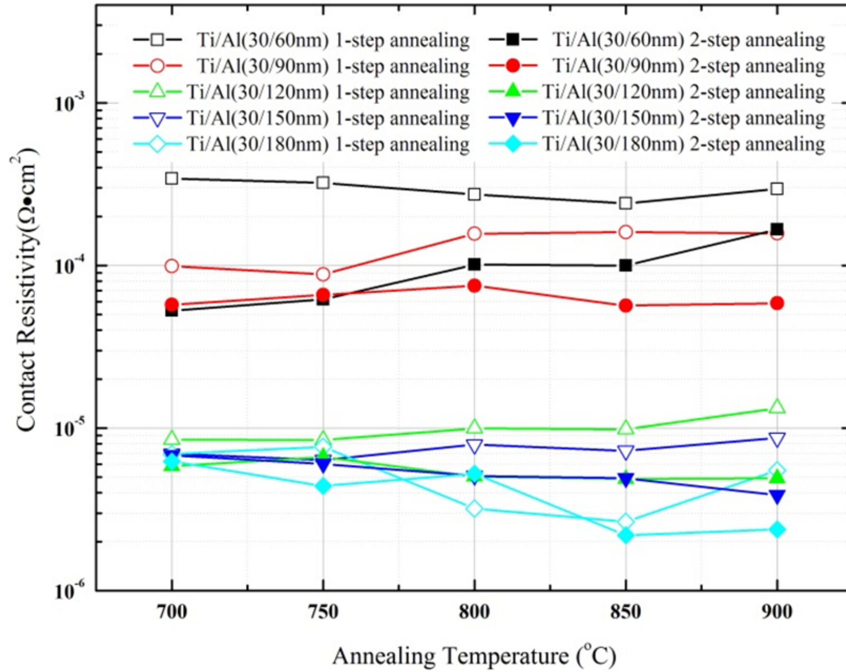


Figure 3.1 Contact resistivity of Ti/Al contacts on n-GaN with different thickness ratios by one-step or two-step annealing under different annealing temperatures.

3.1.4 Surface roughness of Ti/Al contact on n-GaN

Figure 3.2 shows the root mean square (RMS) roughness measured by means of AFM for different Ti/Al thickness ratios, both for the one-step and two-step annealed contacts. It can be noticed that high Al content contacts have higher surface roughness and that there is no significant difference in the RMS values between contacts with one-step and two-step annealing. However, the contacts with Ti/Al thickness of 30/60, 30/90, and 30/120 nm with two step annealing exhibit a much lower RMS roughness, having a value of 14, 15.6 and 10.9 nm, respectively, compared to contacts with one-step annealing. Based on the above experimental results shown in Figure 3.2 and the results shown in Figure 3.1, it can be concluded that the Ti/Al thickness of 30/120 nm will provide a good

tradeoff between surface roughness and specific contact resistivity, which is consistent with the previous work [87]. Further investigations will be carried out for the 30/120 nm Ti/Al contact.

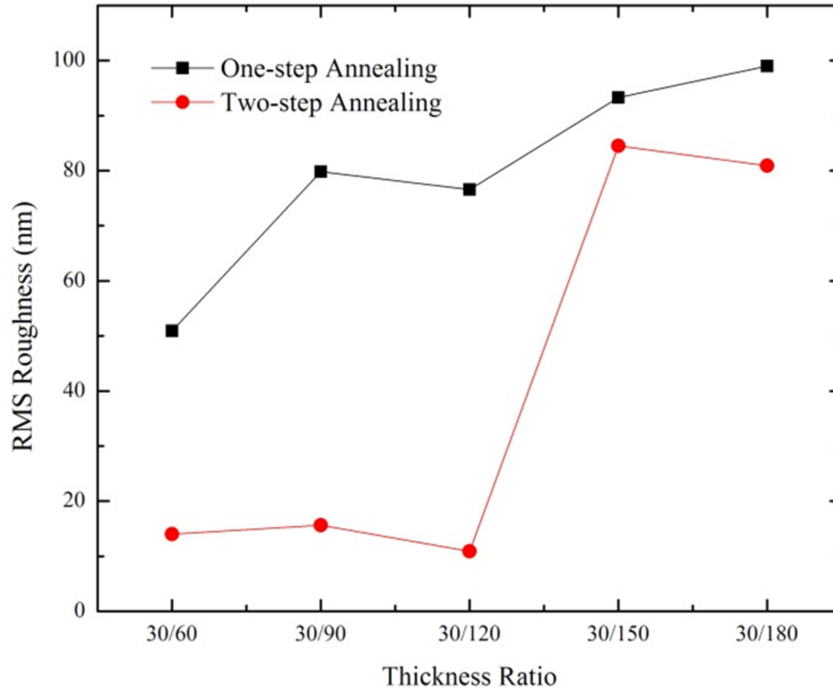


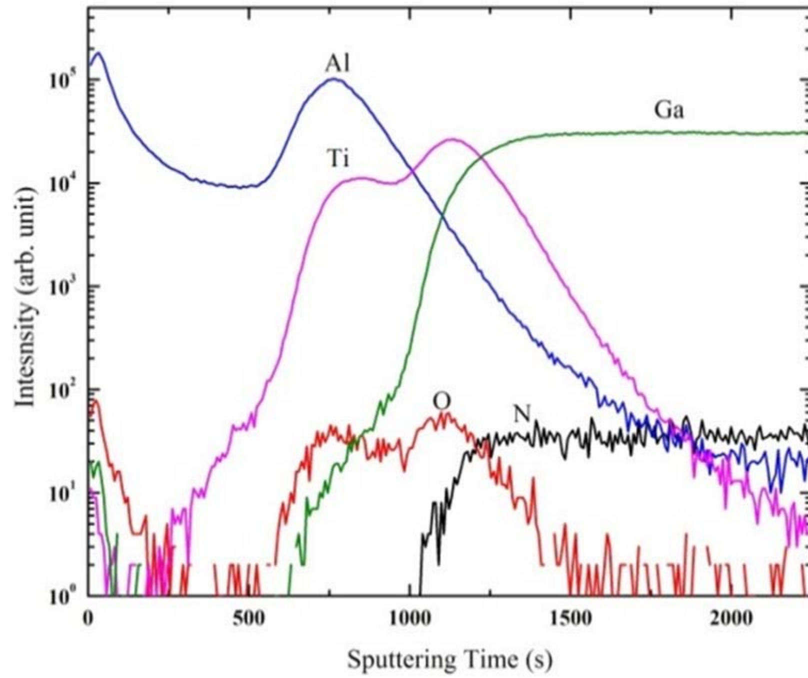
Figure 3.2 RMS roughness as a function of Ti/Al thickness ratio for contacts by one-step and two-step annealing at 850 ^{o}C in vacuum.

3.1.5 Contact formation for Ti/Al contacts on n-GaN

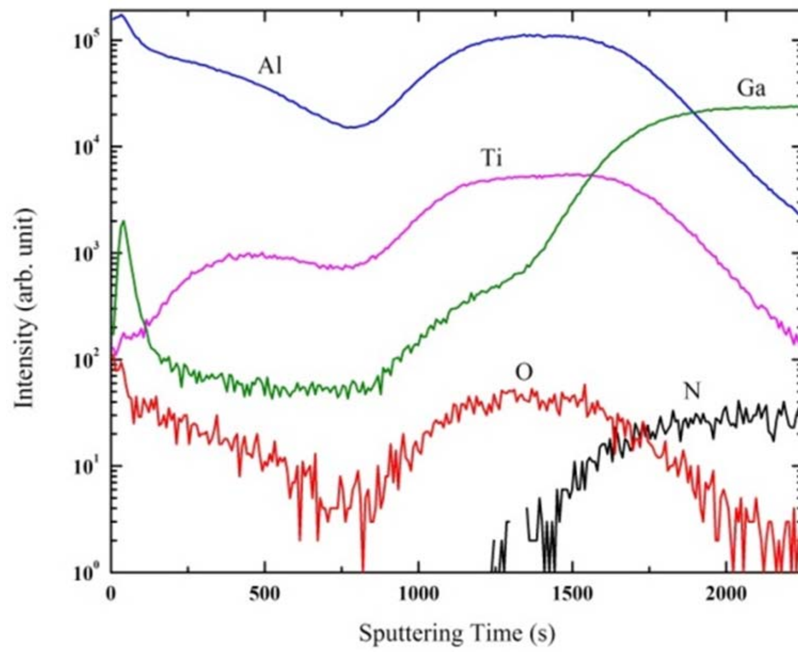
In order to investigate the solid phase reaction during thermal treatment, ToF-SIMS profiling was performed and XRD measurements are performed. Figure 3.3 shows the SIMS depth profile information of Ti/Al thickness ratio of 30/120 nm contacts under different conditions: (a) as-deposited, (b) after first-step annealing at 600 ^{o}C for 2 min and (c) after first-step annealing at 600 ^{o}C for 2 min, followed

by second-step annealing at 800 ^{o}C for 1 min. The corresponding XRD results are shown in Figure 3.4 and Figure 3.5.

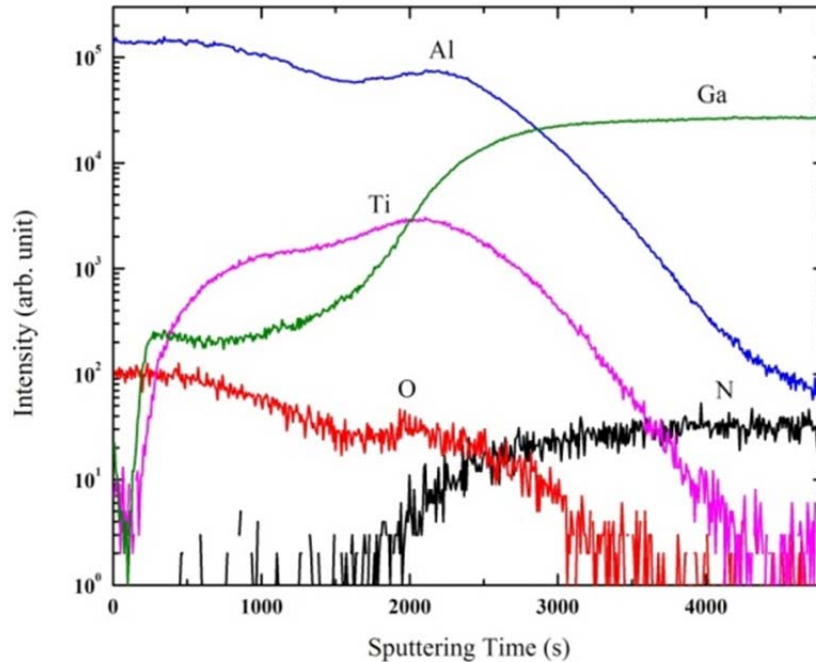
As shown in Figure 3.3, after the first-step annealing at 600 ^{o}C for 2 min in vacuum, and Ga out-diffusion was observed and Ti and Al inter-diffusion also happened, which means that it is possible for Ti and Al to form some kinds of alloys at this condition. This is confirmed by the XRD result shown in Figure 3.4, with the formation of $TiAl_3$ detected after the 600 ^{o}C annealing. Nitrogen out-diffusion is also observed during the second-step high temperature annealing at 800 ^{o}C, as shown in Figure 3.3(c), which leads to nitrogen vacancies being created at the interface between metal and GaN substrate, which is useful for the formation of ohmic contact. Although the nitride formation (Ti-Al-N alloy) was confirmed by XRD result in Figure 3.5, the contact resistivity does not change significantly, which may be due to the amount of Ti-Al-N alloy being inadequate to introduce a highly doped layer between GaN and metal contacts for the Ti/Al contacts with a thickness ratio of 30/120, as compared to the one with a ratio of 30/180, which shows a significant improvement for ρ_C at 850 ^{o}C. It is noteworthy that Ti does not diffuse to the surface of the contact after the second-step high temperature annealing at 800 ^{o}C, which could further indicate the formation of a thermally stable Ti-Al alloy. It will be seen in the following paragraph that the ToF-SIMS observation of formation of a stable Ti-Al alloy formation is consistent with the XRD results, where thermally stable $TiAl_3$ phase is actually identified.



(a) as-deposited



(b) First-step annealing at 600 ^{o}C for 2min



(c) After first-step annealing at 600 ^{o}C for 2 min followed by second-step annealing at 800 ^{o}C for 1 min.

Figure 3.3 ToF-SIMS depth profile for Ti/Al (30/120 nm) at different annealing conditions: (a) as deposited, (b) first-step annealing at 600°C for 2min, and (c) after first-step annealing at 600 ^{o}C for 2 min, followed by second-step annealing at 800 ^{o}C for 1 min.

As manifested by the $TiAl_3$ peaks in Figure 3.4, we have confirmation of our intention of carrying out the first-step annealing at a lower temperature, of which the main purpose is to allow reaction that leads to the formation of a stable $TiAl_3$ alloy between Ti and Al. As a result of $TiAl_3$ formation, the peaks corresponding to Ti have disappeared (which could signify full consumption of Ti), while the remaining Al is still detectable after the first-step annealing at 600 ^{o}C. Figure 3.5 shows the XRD profiles for the 30/120 nm Ti/Al contact under different second-step annealing conditions (the first-step annealing is 600 ^{o}C for 2 min in vacuum). It is noticed that after the second-step annealing at 700 ^{o}C, most of Al that

remained after the first-step annealing is 600 ^oC was consumed and converted to $TiAl_3$. After the second-step annealing at 800 ^oC, additional peaks corresponding to the phase of Ti_2AlN appear, this is consistent with the N_2 out-diffusion from GaN observed in the ToF-SIMS result after annealing at 800 ^oC (see Figure 3.3(c)). The out-diffused nitrogen reacts with Ti-Al alloy and leads to the Ti_2AlN formation, which can be detected by XRD shown in Figure 3.5. With the second-step annealing at a higher temperature of 850 ^oC, more peaks of Ti_2AlN are observed, which may indicate increasing amount of Ti_2AlN is formed (as a result of more N_2 out-diffusion from GaN). The formation of Ti_2AlN has also been reported elsewhere [86].

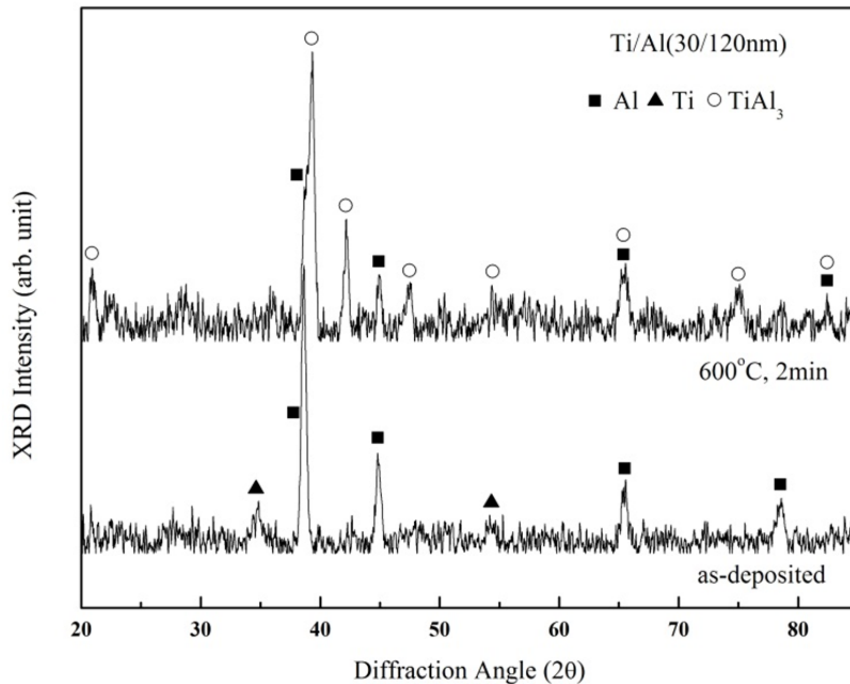


Figure 3.4 XRD scans of Ti/Al (30/120 nm) contacts: (a) as-deposited, (b) after the first-step annealing at 600 ^oC for 2 min in vacuum.

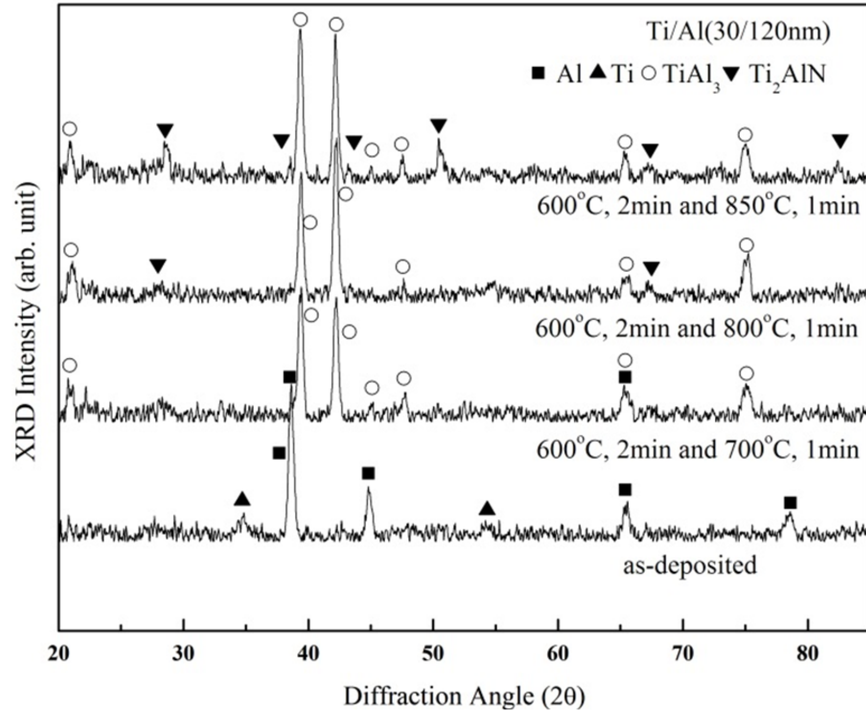


Figure 3.5 XRD scans of the Ti/Al (30/120 nm) contacts under various annealing conditions: (a)as-deposited, (b) first-step annealing at 600 ^{o}C for 2 min in vacuum, followed by second-step annealing at 700 ^{o}C for 1 min in vacuum, (c) first-step annealing at 600 ^{o}C for 2 min in vacuum, followed by second-step annealing at 800 ^{o}C for 1 min in vacuum, and (d)) first-step annealing at 600 ^{o}C for 2 min in vacuum, followed by second-step annealing at 850 ^{o}C for 1 min in vacuum.

As shown in Figure 3.4, most of Al reacted with Ti during the first-step annealing, meanwhile leading the high thermally stable phase of $TiAl_3$ formation. On the other hand, for Al rich samples (*e.g.,* Ti/Al thickness of 30/150 nm and 30/180 nm), a large amount of Al is expected to remain after the first-step annealing compared to the sample with Ti/Al thickness 30/120 nm which eventually will increase the surface roughness, hence leading to worse surface morphology after the second-step annealing, as shown in Figure 3.2. The similar mechanism for surface roughness has been explained in reference [86].

A discussion is provided as follows, in terms of the Ti-Al binary phase diagram shown in Figure 3.6 [86] on the observed XRD results (Figure 3.4 and Figure 3.5) and surface morphology (Figure 3.2) after the first and second step annealing conditions. The amount of remaining Al after the first-step annealing plays a crucial role in determining the surface roughness of Ti/Al contacts after the second-step annealing. According to the Ti-Al phase diagram in Figure 3.6, for Ti/Al thickness of 30/60, 30/90 and 30/120 nm, most of Al is consumed by Ti during the first-step annealing to form relative Ti-Al alloys (e.g., AlTi, Al_2Ti, Al_5Ti_2 and $TiAl_3$ etc.), which are thermally stable at high temperature.

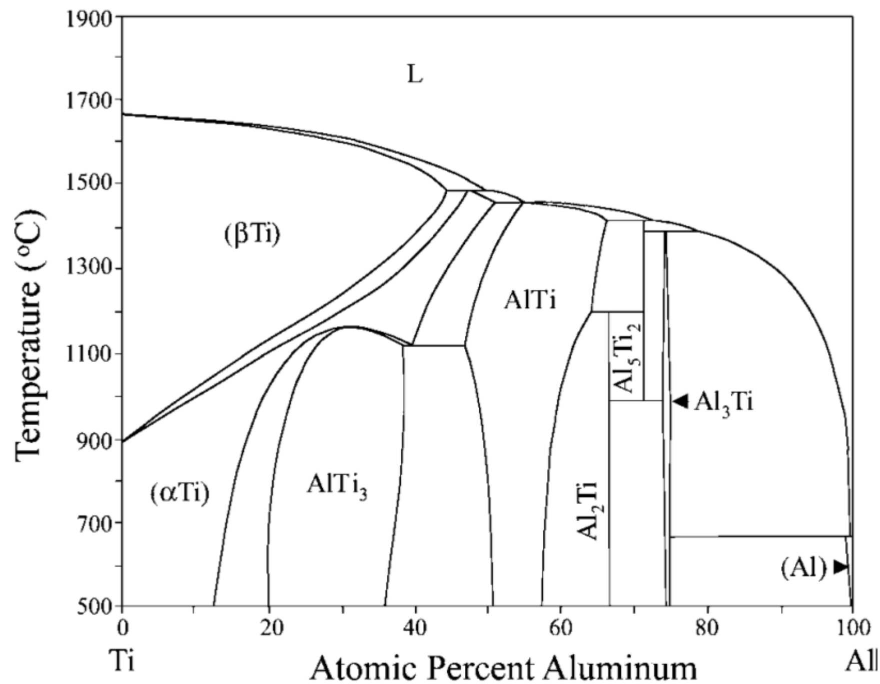


Figure 3.6 Phase diagram of the Ti-Al binary system [86].

The mechanism about ρ_C dependent on Al composition was discussed by Daele et al [88, 89]. They showed that the voids existed at the interface between Ti and GaN for Ti-rich contacts, after thermal annealing, could lead to the degradation of

Ti/Al ohmic contacts. The role of Al in the Ti/Al system was shown to decrease the aggressive Ti-GaN reaction [90], thus reducing the formation of voids at the metal-GaN interface. Moreover, $TiAl_3$, which can be formed for Al-rich (Al/Ti atomic ratio >3) contacts according to the Ti-Al binary phase diagram shown in Figure 3.6, could be used to reduce the oxidation of the bottom Ti layer [91]. Hence, in Figure 3.1 for Al-rich Ti/Al contacts (30/90, 30/ 120, 30/150 and 30/180), the two-step annealing shows better results than the one-step annealing. This may be attributed to $TiAl_3$, formed during the first-step low temperature annealing, which helps reduce contact metal oxidation in the subsequent second-step high temperature annealing. For Al rich samples annealed using a one-step process, there is less $TiAl_3$ existing before the high temperature annealing, so it could be easier for the Ti/Al contact to oxidize during the thermal treatment.

3.1.6 Summary

In this section, the two-step annealing has shown to be an effective method to obtaining good surface morphology for Ti/Al contacts, which require high annealing temperature (> 750 ^{o}C) to form low contact resistivity ohmic contact. Different thickness ratios between Ti and Al have been investigated. It has been confirmed that the first-step annealing at 600 ^{o}C has led to the formation of the stable $TiAl_3$. Our results show that the 30/120 nm Ti/Al contact presents a tradeoff between surface roughness and specific contact resistivity, with a minimum contact resistivity of 4.87×10^{-6} $\Omega\cdot cm^2$ and a RMS roughness less than 10 nm obtained. However, the thermal budget for those contacts is still high (>

750 ^{o}C). To try to lower the annealing temperature, we attempt to introduce other transition metal to replace Ti in the following section.

3.2 Hf-based ohmic contacts on n-GaN

3.2.1 Introduction

As discussed in Section 3.1, although Ti/Al contacts by two-step annealing processing shows a good tradeoff between surface roughness and contact resistivity, other ohmic metal could be introduced since the thermal budget required is still high (>750 ^{o}C). Generally, for ohmic contact formation at the metal-GaN interface, low work function of metal and formation of metal nitride, which leads to a heavily doped layer near the interface, are desired. Nitride formation is mainly driven by the change in enthalpy [92]. Hafnium (Hf) is attractive since it has a low work function of ~3.9 eV , close to the electron affinity of GaN and is lower than that of Ti (work function ~4.33 eV) [93]. Furthermore, Hf has more negative enthalpy (-88.2 kcal/mol) [94] for nitride formation than GaN (-26.3 kcal/mol), which means the transition metal nitride formation is thermodynamically favorable. Therefore, it is expected that Hf could form an ohmic contact to GaN at low temperature. In this section, a preliminary examination by using Hf based contacts with Au capping layer, i.e., Hf/Al/Ni/Au (essentially replacing Ti in the Ti/Al/Ni/Au contact by Hf), to examine the electrical and structural properties the Hf based contacts on n-GaN is conducted.

3.2.2 Experiment

In this section, the GaN wafer structure, cleaning process, native oxide removing, and photolithography are the same as those discussed in Section 3.1.2. Metal layers of Hf/Al/Ni/Au (20/100/25/50 nm) and Ti/Al/Ni/Au (20/100/25/50 nm) were deposited sequentially by e-beam evaporation. A rapid thermal annealing (RTA) process was carried out to do thermal annealing at various temperatures in the range between 600-900 ^{o}C for 1 min in vacuum for both Hf- and Ti-based contacts. Current-voltage (I-V) characteristics were obtained at room temperature using an Agilent B1500A semiconductor parameter analyzer. X-ray diffraction (XRD), time-of-flight secondary ion mass spectroscopy (ToF-SIMS) and cross-sectional transmission electron microscope (TEM) were used in order to investigate the metallurgical reactions and the mechanism behind the ohmic contact formation for Hf/Al/Ni/Au based scheme.

3.2.3 Electrical properties of Hf-based contacts on n-GaN

Figure 3.7 shows the results of *I-V* characteristics as a function of annealing temperature for Hf/Al/Ni/Au (20/100/25/50 nm) contacts on n-GaN with the CTLM structure having a gap spacing of 10 μm. A rectifying behavior is observed for the 600 ^{o}C annealed sample, however, the contacts become ohmic for ≥ 630 ^{o}C annealed conditions in which the steepest *I-V* slope is noted for the 650 ^{o}C annealed sample.

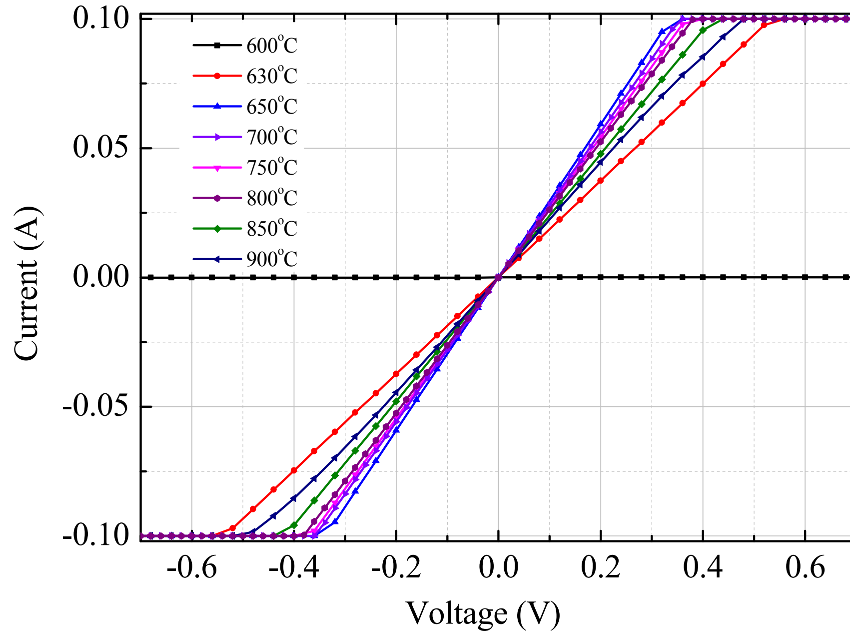


Figure 3.7 Typical I-V characteristics of Hf/Al/Ni/Au (20/100/25/50 nm) contacts on n-GaN as a function of annealing temperature performed in vacuum for 1 min.

The specific contact resistivity was calculated from the linear curve fitting of the relationship between measured resistances versus gap spacing, as described in Chapter 2. Figure 3.8 shows the variation of specific contact resistivity as a function of annealing temperature for the Hf and Ti based contacts on n-GaN. For Hf based contacts, it is observed that the specific contact resistivity initially decreases to 1.09×10^{-6} $\Omega\cdot cm^2$ upon annealing from 630 to 650 ^oC, and increases again to a value of 5.79×10^{-6} $\Omega\cdot cm^2$ after annealing at 900 ^oC. On the contrary, Ti based contact exhibits a significant drop in specific contact resistivity beyond 750 ^oC annealing temperature, in fact, demonstrates the lowest value of 8.65×10^{-7} $\Omega\cdot cm^2$ at 850 ^oC, and again shows an increasing trend at 900 ^oC, which is consistent with previous studies [95]. Therefore, from Figure 3.8, it is clear that Hf-based metal scheme can achieve a low specific contact resistivity at a

comparatively low annealing temperature of 650 °C, which is 200 °C lower than the 850 °C needed for the Ti/Al/Ni/Au contact.

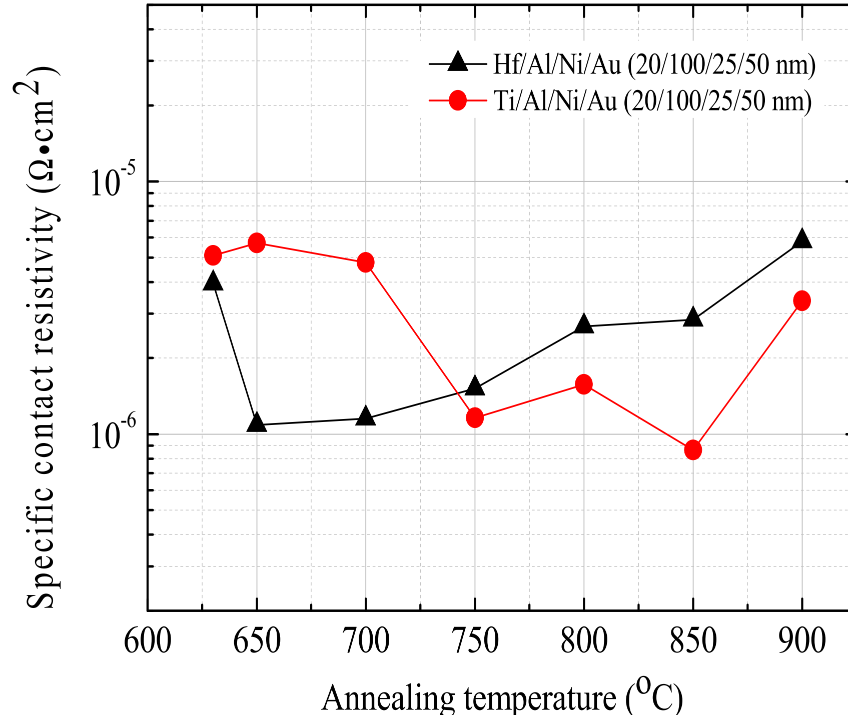


Figure 3.8 Variation of specific contact resistivity as a function of annealing temperature for Hf/Al/Ni/Au (20/100/25/50 nm) and Ti/Al/Nu/Au (20/100/25/50 nm) contacts on n-GaN.

3.2.4 Ohmic contact formation for Hf-based contacts on n-GaN

In order to investigate the mechanism behind the low temperature formation of ohmic contact for the Hf-based metal scheme, several physical-chemical characteristics have been measured. Figure 3.9 shows the SIMS depth profiles of several constituent metals for the Hf/Al/Ni/Au based contacts for the as-deposited and 650 °C annealed samples. It can be observed that after 650 °C annealing, most of the four constituent metals are mixed together, especially the Hf and Al layers,

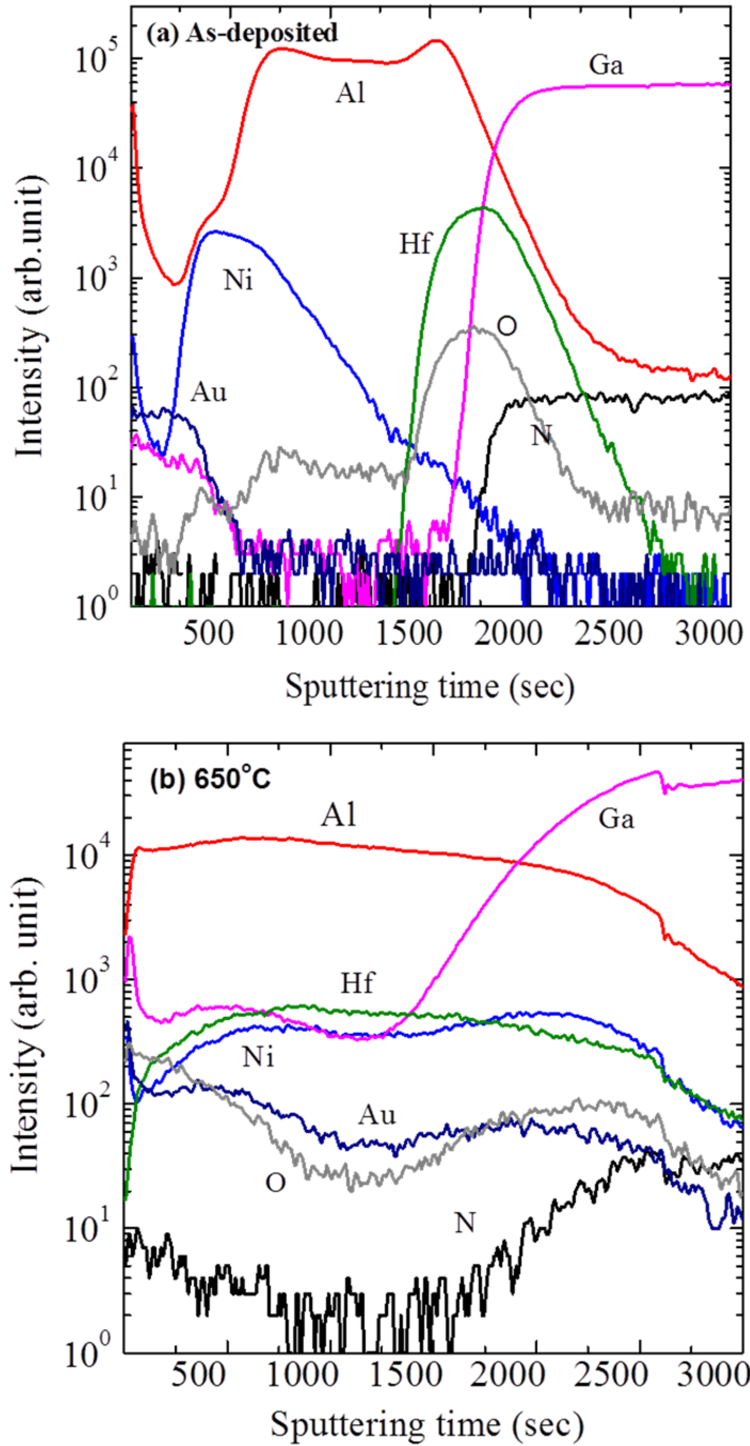


Figure 3.9 ToF-SIMS depth profiles of Hf/Al/Ni/Au on n-GaN (a) as-deposited, and (b) after annealing at 650 ^{o}C for 1min in vacuum.

which are completely mixed and have partly diffused into GaN while the out diffusion of nitrogen and gallium at the metal-semiconductor interface is also observed, as shown in Figure 3.9 (b). The out diffusion of nitrogen leads to vacancies that behave as donors, thus giving rise to a heavily n-doped layer near the surface of GaN, which is similar to the main reason for the formation of Ti based ohmic contacts to n-GaN [96, 97].

In order to identify the metal alloy phases formed, XRD analysis was performed. Figure 3.10 shows the XRD profiles of the Hf/Al/Ni/Au based contacts for the as-deposited and annealed samples, where annealing is done at 650 ^{o}C in vacuum for 1 min. It can be observed from the XRD scans in Figure 3.10 that the peaks corresponding to Au have disappeared after annealing at 650 ^{o}C, while new alloy phases corresponding to Au-Ni, Al-Au, Hf-Al and especially $Hf_{0.78}Al_{0.22}N$ and $Hf_{0.5}Al_{0.5}N$ alloy phases begin to appear. The observation of Hf-Al-N alloy phase has recently been reported [98]. Indeed, the formation of several Hf-Al intermetallic alloy phases at low temperature less than 400 ^{o}C has been reported earlier, as can be seen from the phase diagram and thermochemistry data of the binary Hf-Al system shown in Figure 3.11 [99]. It is anticipated that the existence of Hf-Al-N alloy similar to Ti-Al-N alloy for Ti based contacts [86] plays a crucial role to the formation of low temperature ohmic contact to n-GaN. Figure 3.12 presents the cross-sectional TEM images of the Hf/Al/Ni/Au (20/100/25/50 nm) based contact annealed at 650 ^{o}C. The interface between the metal and semiconductor can be seen clearly, which might be good to enhance the stability of Hf based contacts.

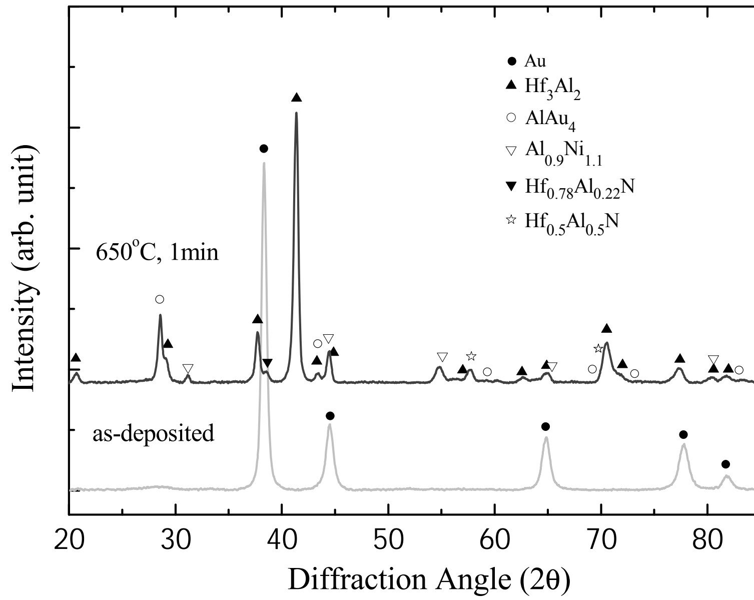


Figure 3.10 XRD scans of Hf/Al/Ni/Au (20/100/25/50 nm) contacts: (a) as-deposited, and (b) after annealing at 650 °C for 1 min in vacuum.

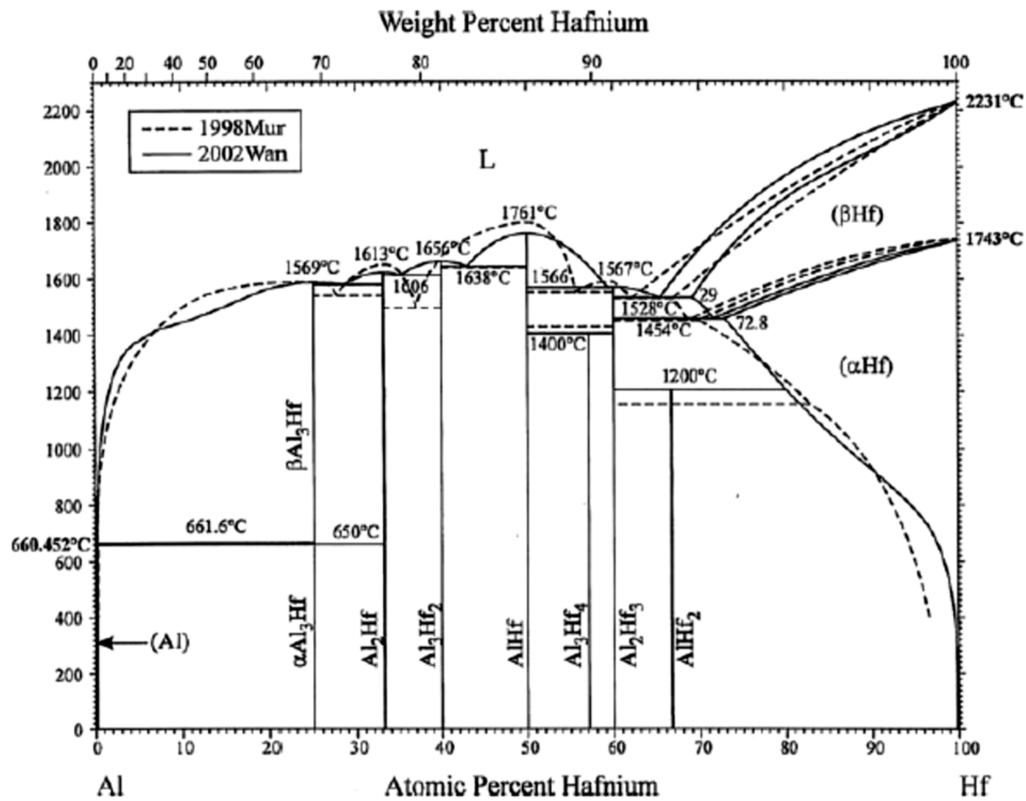


Figure 3.11 Phase diagram of the binary Hf-Al system.

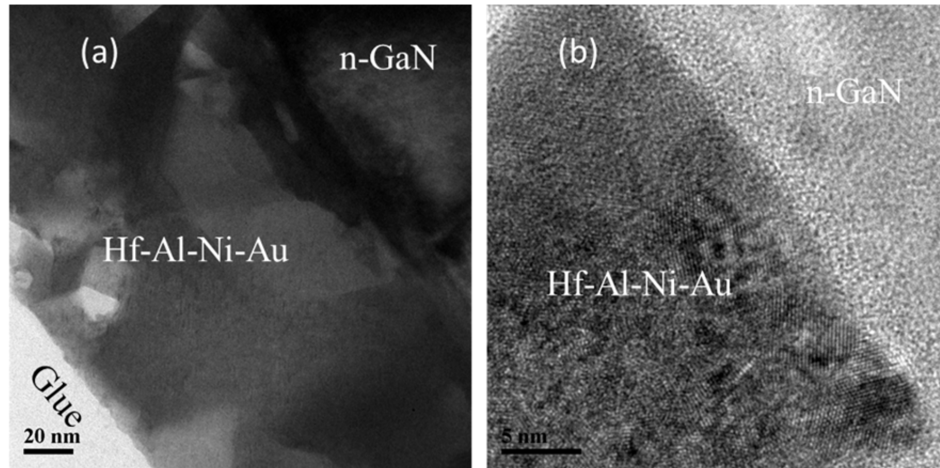


Figure 3.12 Cross-sectional TEM images of the Hf/Al/Ni/Au (20/100/25/50 nm) contact after annealing at 650 ^{o}C.

3.5 Summary

Hf/Al/Ni/Au based metal scheme was found to be able to form ohmic contact with low specific contact resistivity to n-GaN substrate at a relatively low annealing temperature of 650 ^{o}C (200 ^{o}C lower than the 850 ^{o}C required by the Ti/Al/Ni/Au contact). The SIMS and XRD results confirm the formation of Hf-Al and Hf-Al-N alloy phases which are likely to be responsible for the ohmic contact formation at low annealing temperature. The development of Hf-based metallization scheme to form low resistance ohmic contacts at an annealing temperature lower than the Al melting point could significantly reduce the risk of lateral overflow that often causes short-circuit between the gate and source/drain of the devices. Therefore, a low thermal budget contact could be achieved on InAlN/GaN heterostructure. The comprehensive investigations on Au-free Hf based contacts will be carried out later on InAlN/GaN-on-Si wafer in Chapter 4.

Chapter 4

Hf/Al/Ta ohmic contacts on InAlN/GaN

This chapter focuses on the realization of high performance ohmic contacts on InAlN/GaN heterostructures. From the work presented in Chapter 3, we have concluded that the Hf-based ohmic contact is a promising candidate and expected to serve well as the ohmic contacts on InAlN/GaN with lower thermal budget. Thus, this chapter first provides the comparison between Hf-based gold-free ohmic contacts and other transition metal based counterparts, which shows that Hf-based contacts are indeed the best. Following which, the optimization of Hf-based contacts on InAlN/GaN will be conducted. The mechanisms of ohmic contact formation and carrier transport of the optimized Hf-based ohmic contacts are also investigated.

4.1 Introduction

Since the InAlN/GaN HEMT technology was developed after AlGaN/GaN, the most popular ohmic contact schemes were transferred from AlGaN/GaN HEMTs. Historically, Ti/Al/X/Au ohmic metallization scheme under high temperature annealing was widely used in InAlN/GaN HEMTs, where X could be Ni, Mo, Ti, etc [55, 59, 100-103] and it acted as a diffusion barrier layer to the Au cap layer. Furthermore, up to date Ti/Al/Ni/Au and Mo/Al/Mo/Au contacts on InAlN/GaN with annealed at low temperature (600-650 ^{o}C) have been reported [60, 62]. However, these contacts necessitate pre-metal deposition surface treatment by plasma to render ohmic properties. In this chapter, transition metals such as Hf, Ti,

Ta, Zr, Nb, and V have been selected for ohmic contact formation owing to their low work function and large negative enthalpies for nitride formation [93, 94, 104-106]. And Ta, a refractory metal with high melting point (3017 ^{o}C), was used as the cap layer to prevent the surface oxidation of Al. We first examine a number of Au-free transition metal (TM) based ohmic contacts (TM/Al/Ta, where TM = Hf, Ti, Ta, Zr, Nb, and V) on InAlN/GaN, without the use of pre-metal deposition surface treatment by plasma, to identify the most promising candidate, i.e., one that requires the lowest annealing temperature to yield the lowest contact resistance. Subsequently, this transition metal based contact system is optimized with different thickness ratio. Lastly, the formation mechanism and carrier transport mechanism of the optimized ohmic contacts are studied.

4.2 Experiment

The InAlN/GaN heterostructures used in our experiments was shown in Figure 2.7(b). The sheet resistance of the epiwafer is 458 Ω/□, the 2DEG carrier mobility and concentration are 1112 cm^2/Vs and 1.2×10^{13} cm^{-2} respectively, as determined by room-temperature Hall measurement. The cleaning process, native oxide removing, photolithography and lift-off process are as those described in Chapter 2. Mesa isolations were realized using the BCl_3/Cl_2 gas chemistry in an ICP-RIE system. The ohmic contact metals were deposited in a sputtering system. To compare the transition metal based ohmic contacts, we studied the following metallization schemes, namely TM/Al/Ta (15/200/20 nm), where TM=Ti, Ta, Zr, Nb, V and Hf. All the transition metal based ohmic contacts were annealed at temperatures ranging from 550 to 700 ^{o}C for 60 s in vacuum. The most promising

transition metal based ohmic contact system identified (i.e., Hf/Al/Ta) was optimized subsequently. The current-voltage (I-V) characterizations of Hf/Al/Ta ohmic contacts were carried out at room-temperature using a semiconductor parameter analyzer (Agilent B1500A) by the four-point method. Based on the I-V results obtained, the contact resistance (R_c), contact resistivity (ρ_c) and substrate sheet resistance (R_{sh}) were extracted for the Hf based ohmic contacts annealed at different temperatures by linear transmission line method (LTLM). Time-of-flight secondary ion mass spectroscopy (ToF-SIMS) was performed to investigate the metal inter-diffusion before and after the thermal treatment. In addition, high-angle annular-dark-field (HAADF) scanning transmission electron microscopy (STEM) and energy-dispersive X-ray (EDX) spectroscopy were used to study the interface between the Hf-based ohmic contact and InAlN/GaN heterostructure. Besides, the I-V characteristics of the Hf/Al/Ta contact annealed at the optimum temperature were measured as a function of the sample temperature (from ~300 to 500 K) to analyze the contact carrier transportation mechanism. Finally, preliminary thermal aging tests were conducted at 350 ^{o}C in air for more than 200 hours to assess the Hf/Al/Ta contact thermal stability.

4.3 Au-free transition metal based contacts on InAlN/GaN

To evaluate the ohmic transition temperature of various transition metal (TM) based contacts on InAlN/GaN: TM/Al/Ta (15/200/20 nm), where TM = Hf, Ti, Ta, Zr, Nb, and V, annealing of these contacts was carried out in the temperature range from 550 to 700 ^{o}C. As shown in Figure 4.1, it has been found that Hf/Al/Ta contact demonstrated the lowest ohmic transition temperature and

became ohmic after annealing at 550 ^{o}C. On the other hand, the Ti, Ta, Zr, Nb based contacts become ohmic at a higher annealing temperature of 650 ^{o}C, while V based contacts attain ohmic properties at an even higher annealing temperature of 700 ^{o}C. It is also seen that the minimum R_c achieved is ~0.58 Ω·mm after annealing at 600 ^{o}C. The minimum R_c of Ti, Ta, Zr, Nb, and V based contacts, typically achieved at a temperature higher than their respective ohmic transition temperature, are found to be at least 115% higher than that of Hf/Al/Ta contacts.

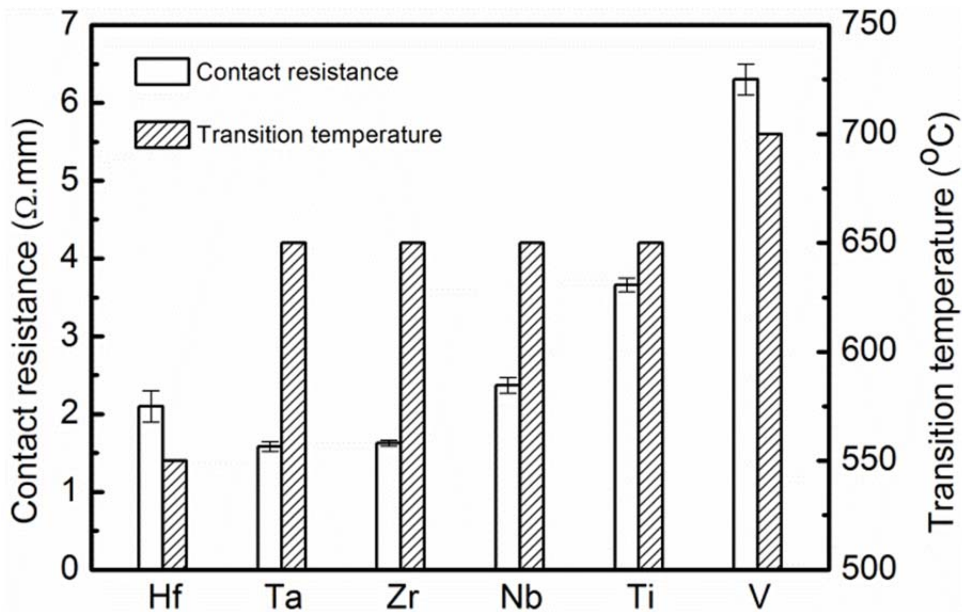


Figure 4.1 Contact resistance (R_c) and ohmic transition temperature for transition metal based ohmic contacts: TM/Al/Ta (15/200/20 nm), where TM= Hf, Ta, Zr, Nb, Ti and V. The contacts are annealed in vacuum for 60 s.

4.4 Optimization of Hf/Al/Ta contacts on InAlN/GaN

From the preceding discussion in Section 4.2, Hf/Al/Ta contact has been identified as the most promising candidate among the transition metal based contacts investigated. To optimize the ohmic contact properties, the effects of the

thickness of Hf and Al in the Hf/Al/Ta contacts on InAlN/GaN heterostructure are investigated by 1) varying the Hf layer thickness from 5 to 35 nm, while keeping the Al layer thickness constant at 200 nm; and 2) varying the Al layer thickness from 100 to 400 nm, while keeping the Hf layer thickness constant at 15 nm. The results (R_c) for the former as a function of annealing temperature are shown in Figure 4.2(a), and those for the latter are shown in Figure 4.2(b). In general, the R_c of Hf/Al/Ta contacts are sensitive to both the Hf and Al layer thicknesses, as seen in Figures 4.2(a) and 4.2(b). The R_c versus annealing temperature curves for Hf/Al/Ta contacts with different Hf and Al thicknesses exhibit similar trends, i.e., ohmic transition at 550 ^{o}C followed by a decrease of R_c up to 550 or 600 ^{o}C, and a slight increase of R_c beyond that. From Figures 4.2(a) and 4.2(b), the optimized Hf/Al/Ta contact is identified to have thickness of 15/200/20 nm.

Specifically, the I-V characteristics for optimized Hf/Al/Ta (15/200/20 nm) contacts with 5 μm spacing were measured and shown in Figure 4.3(a). It is observed that the I-V curve of the as-deposited contacts exhibit a very low current (~1.3 μA at 2 V). With increasing annealing temperature, Hf/Al/Ta contacts became ohmic at 550 ^{o}C and allow a much higher (by 4 orders of magnitude) current flow than that under as-deposited condition. The highest current is obtained for Hf/Al/Ta contacts under thermal annealing at 600 ^{o}C, which indicates an optimal annealing condition. The contact resistance (R_c) and contact resistivity (ρ_c) of Hf/Al/Ta (15/200/20 nm) contacts on InAlN/GaN are shown in Figure 4.3(b), as a function of annealing temperature. As seen, the R_c and ρ_c values of Hf/Al/Ta contacts decrease sharply with increasing annealing temperature from

550 to 600 ^{o}C, and beyond that, they increase slightly with increasing temperature. The best values are R_c of 0.59 ± 0.03 Ω.mm and ρ_c of 6.7 ± 0.58 × 10^{-6} Ω.cm^2 achieved after annealing at 600 ^{o}C.

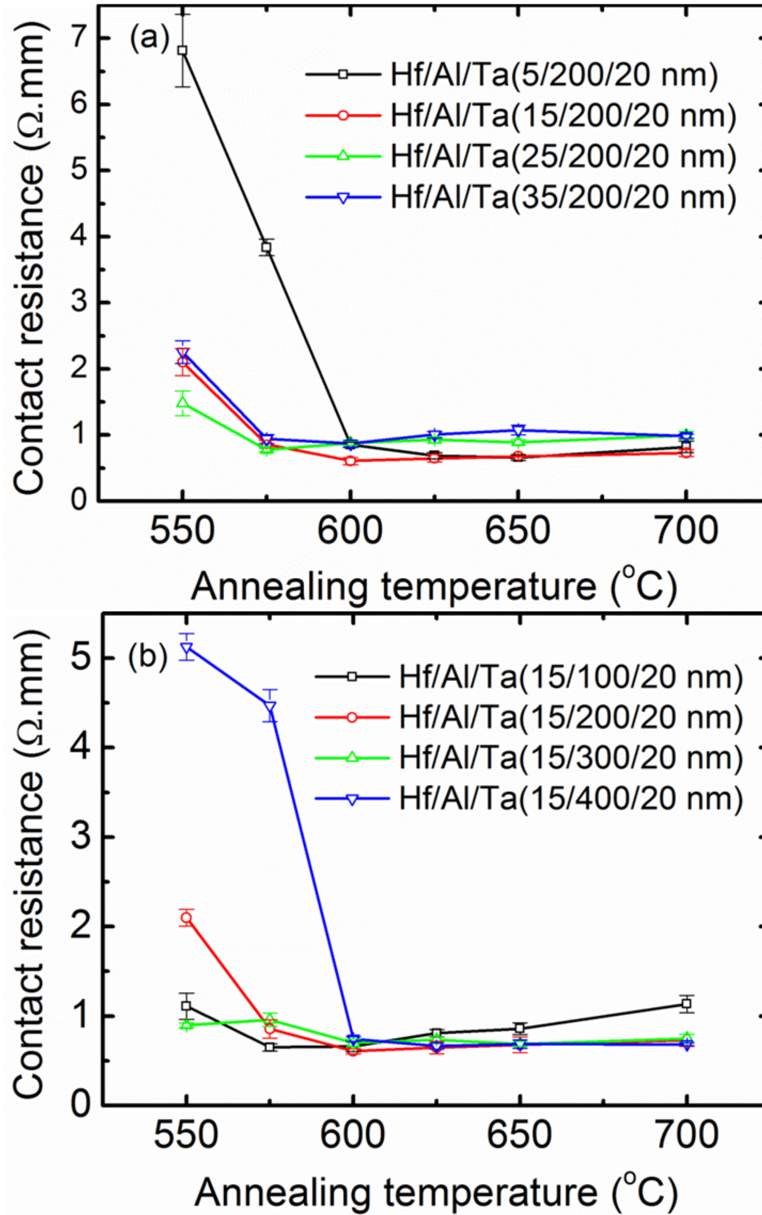


Figure 4.2 Effect of variation in (a) Hf and (b) Al thickness on the contact resistance (R_c) as a function of annealing temperature for the Hf/Al/Ta contacts annealed at 600 ^{o}C.

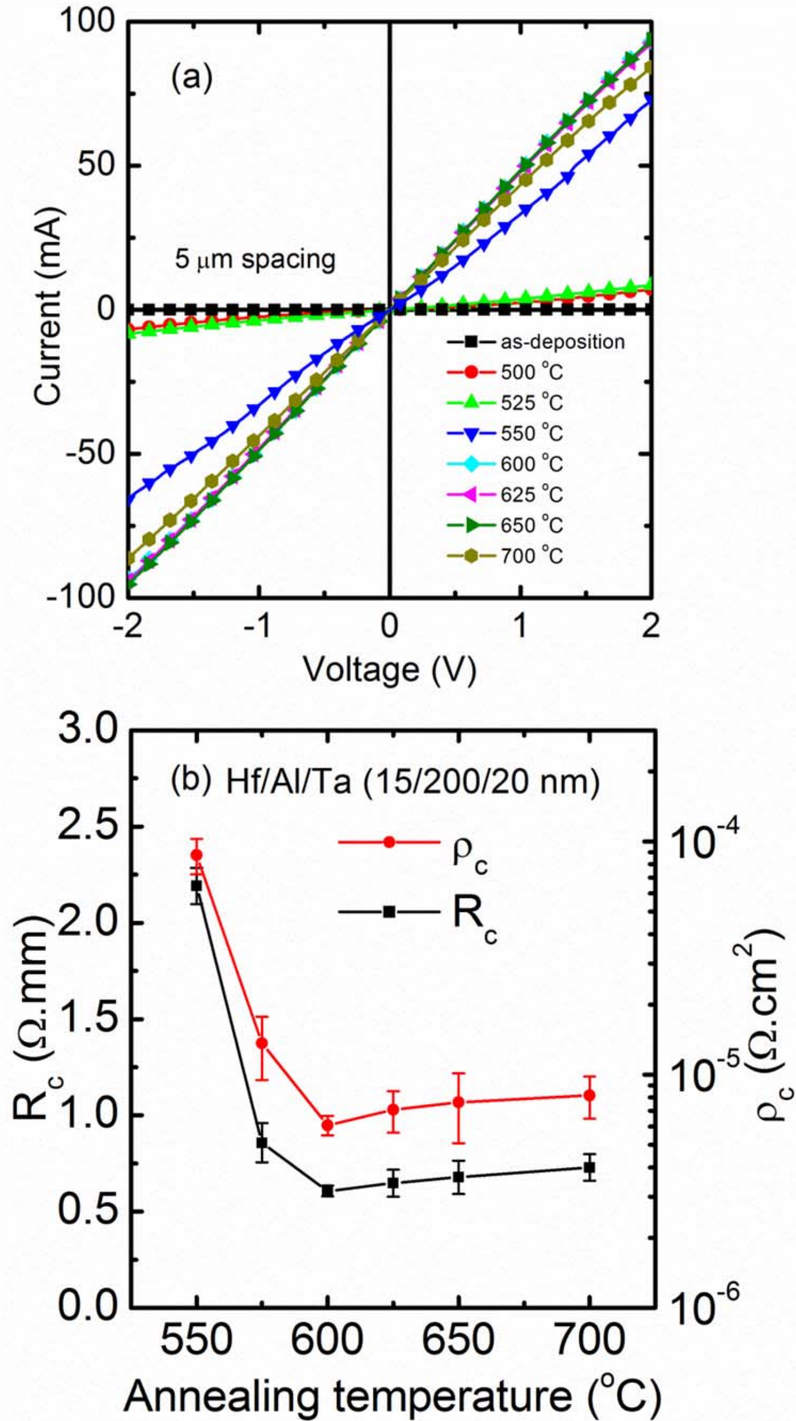


Figure 4.3 Electrical characterizations of Hf/Al/Ta (15/200/20 nm) contacts on InAlN/GaN heterostructure: (a) current-voltage (I-V) characteristics for a contact spacing of 5 μm, and (b) contact resistance (R_c) and contact resistivity (ρ_c) as a function of annealing temperature. The contacts were annealed in vacuum for 60 s.

The R_c for Hf/Al/Ta contacts annealed at the optimum temperature of 600 ^{o}C are also plotted as a function of Al/Hf thickness ratio (t_{Al}/t_{Hf}) in Figure 4.4, which shows that t_{Al}/t_{Hf} of 13.3 may be close to the optimum that yields the lowest R_c. This observation of dependence on t_{Al}/t_{Hf} is similar to that reported earlier for Ti/Al based ohmic contacts on (Al)GaN [86, 89, 107], where it was proposed that the aggressive reaction between Ti and (Al)GaN substrate could degrade the ohmic contact properties. To mitigate this, an Al layer was employed to reduce the aggressive Ti-(Al)GaN reaction. In the meantime, too much of Al was also not desirable as this would leave insufficient Ti to form Ti(Al)N at the (Al)GaN interface, which could lead to increased R_c. Thus, there was a need to optimize the Al/Ti thickness ratio (t_{Al}/t_{Ti}) in Ti/Al based ohmic contacts.

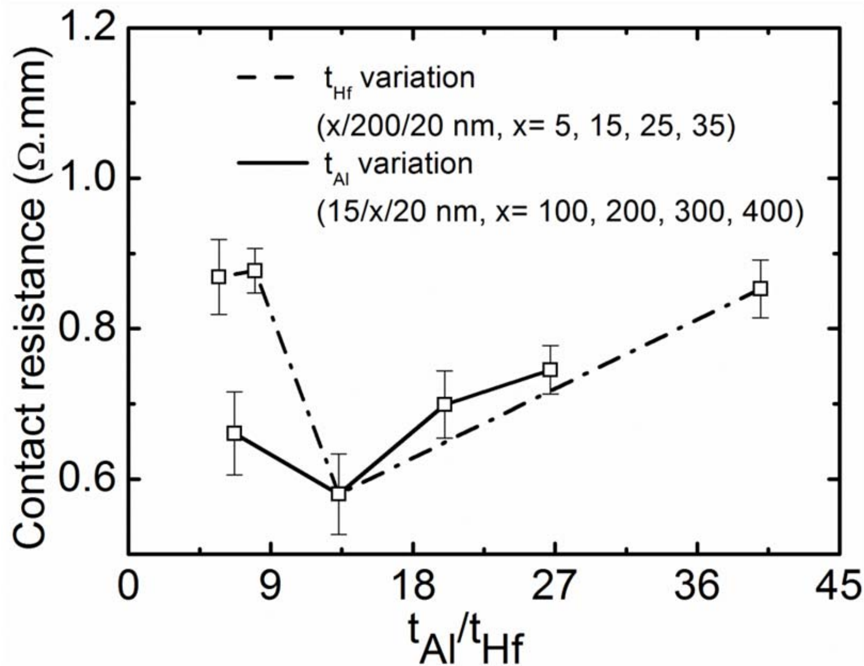


Figure 4. 4 Dependence of R_c on Al/Hf thickness ratio (t_{Al}/t_{Hf}) for the samples annealed at 600 ^{o}C.

We believe that similar to the case of Ti-Al based contacts on (Al)GaN, the Al layer in our Hf/Al/Ta contacts is needed to limit the reaction between Hf and InAlN/GaN (so as to limit HfN formation) to improve the ohmic contact properties, by forming Hf-Al alloy. As discussed above, the HfN phase is necessary for good ohmic contact but too much of it may not give better electrical properties owing possibly to the interface degradation induced, similar to that reported by Van Daele *et al.* for Ti-Al based contacts [89]. The Hf-Al alloy has been reported to form even at the low temperature of 350 ^{o}C [108], while HfN has been reported to form in the higher temperature range of 450-1200 ^{o}C by different methods [109-111]. Therefore, we believe the formation of HfN phase at 550 ^{o}C (the ohmic transition temperature for the Hf/Al/Ta contact) is limited by Hf-Al phase alloying. In our Hf/Al/Ta contacts, the optimum t_{Al}/t_{Hf} ratio was found to be 13.3. It is anticipated that for t_{Al}/t_{Hf} greater than 13.3, the amount of Hf remaining after Hf-Al alloy formation is not sufficient to form HfN phase, which is essential to induce a highly doped layer near the metal-semiconductor interface desired for good ohmic contact. However, for t_{Al}/t_{Hf} lower than 13.3, excessive HfN phase is formed, thus leading to increased R_c.

Figure 4.5 shows the XRD spectra for Hf/Al/Ta (x/200/20 nm, where x = 5, 15 35 nm) on InAlN/GaN after annealing at 600 ^{o}C. The spectrum for Hf/Al/Ta (15/200/20 nm) without annealing is also shown, where the peaks can be indexed corresponding to Hf, Al, and Ta element phases. The formation of Hf-Al alloy, i.e., $HfAl_3$, is evident after annealing at 600 ^{o}C. Moreover, with increasing Hf layer thickness, the amount of $HfAl_3$ phase also increases. This observation points

to the significant role of t_{Al}/t_{Hf} discussed above. In addition, it is noted that the formation of HfN (which is critical to good ohmic contact formation) is not evidenced in the XRD measurements. We believe this could be due to the incomplete reaction at the metal-semiconductor interface or suppressing of signal by upper metal layers.

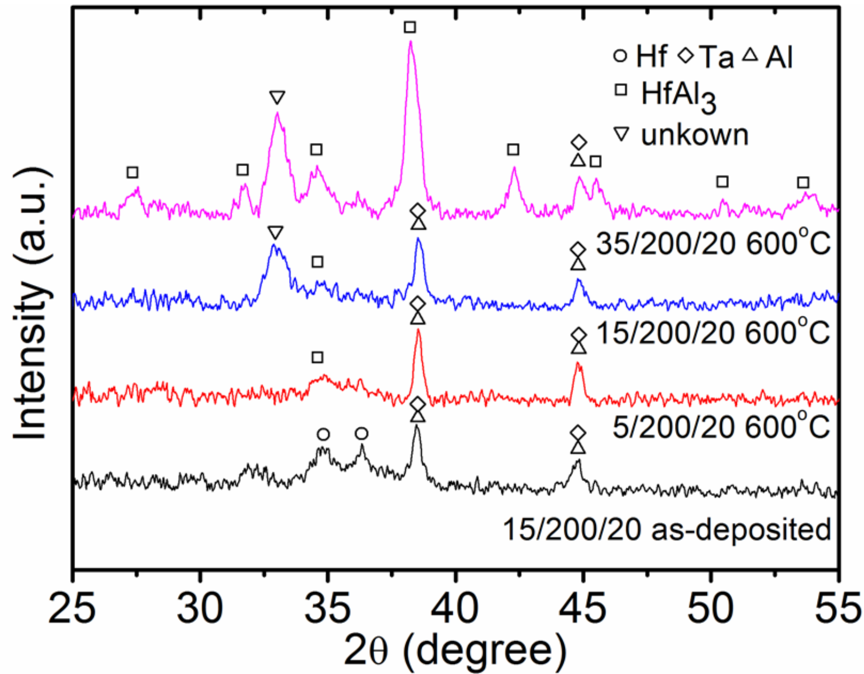


Figure 4.5 XRD spectra for Hf/Al/Ta contacts: as-deposited and annealed at 600 ^{o}C with different Hf layer thickness on InAlN/GaN.

4.5 Ohmic contact formation for Hf/Al/Ta contacts on InAlN/GaN

To examine the details of the reaction between contact metals and InAlN/GaN heterostructure, ToF-SIMS, STEM and EDX measurements were carried out. Figures 4.6(a) and 4.6(b) show the ToF-SIMS depth profiles of Hf/Al/Ta contacts on InAlN/GaN under the as-deposited and 600 ^{o}C annealing conditions. In general, as seen in Figure 4.6(b), changes in the profiles of Al, Hf, In, and N are clearly

noticeable after annealing at 600 ^{o}C compared to the as-deposited sample. The Hf and Al (from both the contact and InAlN/GaN heterostructure) inter-diffusion could signify the formation of Hf-Al alloy at 600 ^{o}C, which was confirmed by XRD (as shown in Figure 4.5). The Hf-Al alloy formation has also been reported to form at a low temperature of 350 ^{o}C. Furthermore, similar to the formation of Ti-Al alloy in the Ti/Al based ohmic contacts on GaN based heterostructures, the Hf-Al alloy formation could play a critical role (i.e., to limit HfN formation) to yield good ohmic contact properties. In our case, the possible formation of HfN can be linked with the observed out-diffusion of N, which can be understood as follows. The out diffusion of N at 600 ^{o}C as seen in Figure 4.6(b) is possibly due to the breaking of In-N bonds rather than Al-N bonds, since the bond strength of In-N bond (1.93 eV) is lower than that of Al-N bond (2.88 eV) [112]. At 600 ^{o}C annealing temperature, the In-N bonds could have been broken, owing to lower dissociation temperature of In-N bonds (~430 ^{o}C) [113] than Al-N bonds (~1800 ^{o}C) [114] in vacuum, thus allowing N to react with Hf to form HfN. Physically this process is triggered by the negative heat of formation of HfN (-88.2 kcal/mol) [94]. In addition, the out-diffusion of N could leave donor-like N-vacancies in InAlN/GaN, similar to the Ti-based ohmic contact on GaN and related materials [115-117], thus forming a thin heavily doped layer at the interface of Hf-based ohmic contact and InAlN/GaN substrate to reduce the barrier width, which is essential for efficient electron tunneling. Additionally, Ga out-diffusion is observed, which could be due to the breaking of Ga-N bonds, as the onset of

thermal dissociation of GaN around 600 °C annealing in vacuum has been experimentally evidenced [118].

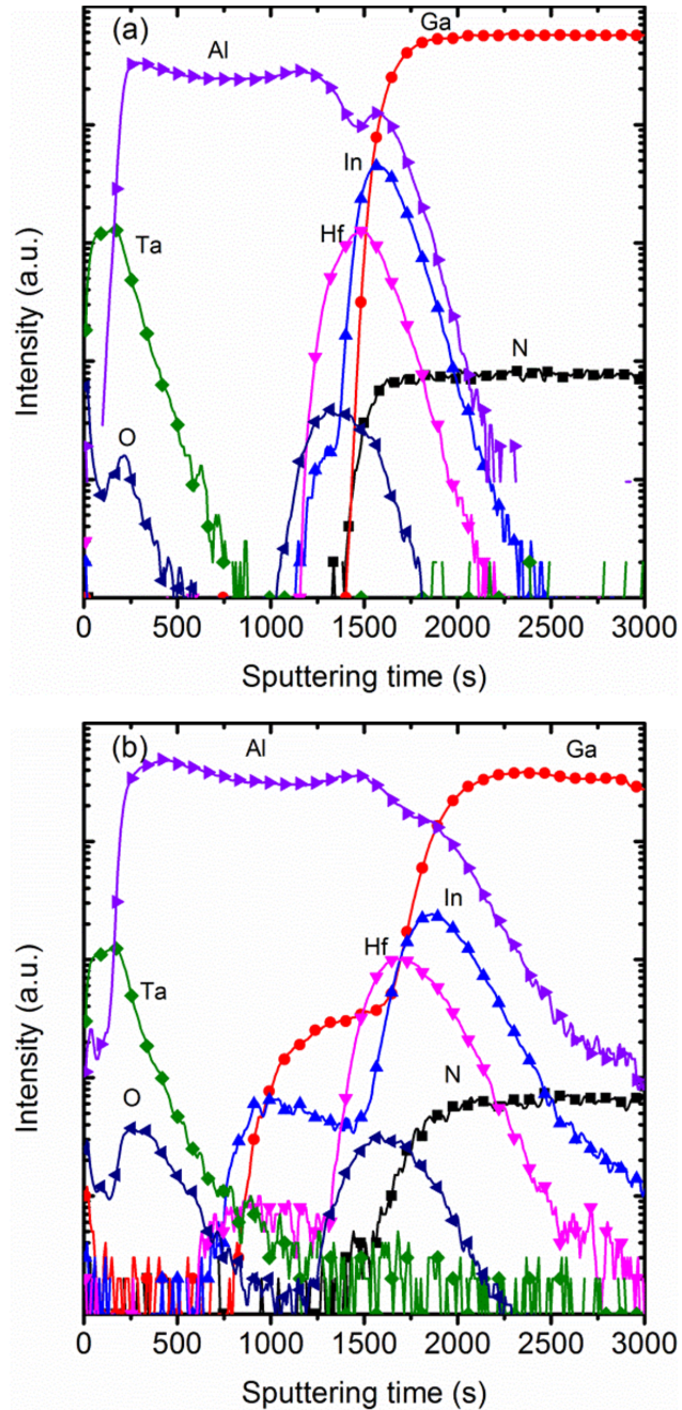


Figure 4.6 ToF-SIMS depth profiles of Hf/Al/Ta contact on InAlN/GaN (a) for the as-deposit condition, and (b) after annealing at 600 °C in vacuum for 60 s.

Figures 4.7(a) and 4.7(b) show the HAADF STEM images of Hf/Al/Ta contact on InAlN/GaN before and after 600 ^{o}C annealing, respectively. Although inter- and out-diffusion are observed in the ToF-SIMS profiles in Figure 4.6, the interface between Hf/Al/Ta contact and InAlN/GaN remains smooth after 600 ^{o}C annealing, as seen in figure 4.7(b). However, significant interface contrast changes are observed in Figure 4.7(b), suggesting that reaction between ohmic metal and semiconductor has occurred. It is also noted that the change in InAlN/AlN layer thickness is insignificant before and after 600 ^{o}C annealing, which implies minimal of InAlN/AlN has been consumed during annealing. This is also confirmed by the estimation of the InAlN/AlN layer thickness using the EDX line profiling across the interface between the Hf/Al/Ta contact and InAlN/GaN heterostructure, as shown in Figures 4.7(c) and 4.7(d). The InAlN/AlN layer thickness is estimated, by means of full width at half maximum (FWHM) of the Al peak, to be 10.5 and 10.0 nm before and after 600 ^{o}C annealing, respectively. Furthermore, Ta signal is not detected in Figure 4.7(d), which indicates Ta has not diffused to the interface between Ta/Al/Hf and InAlN/GaN after annealing at 600 ^{o}C, which means the ohmic contact formation is mainly dependent on the Hf/Al layers and Ta serves essentially as a cap layer to prevent the oxidation of contact layers, in particular, Al. This is consistent with the ToF-SIMS result for Hf/Al/Ta annealed at 600 ^{o}C, as shown in Figure 4.6(b), where no significant Ta signal is observed at the metal-semiconductor interface.

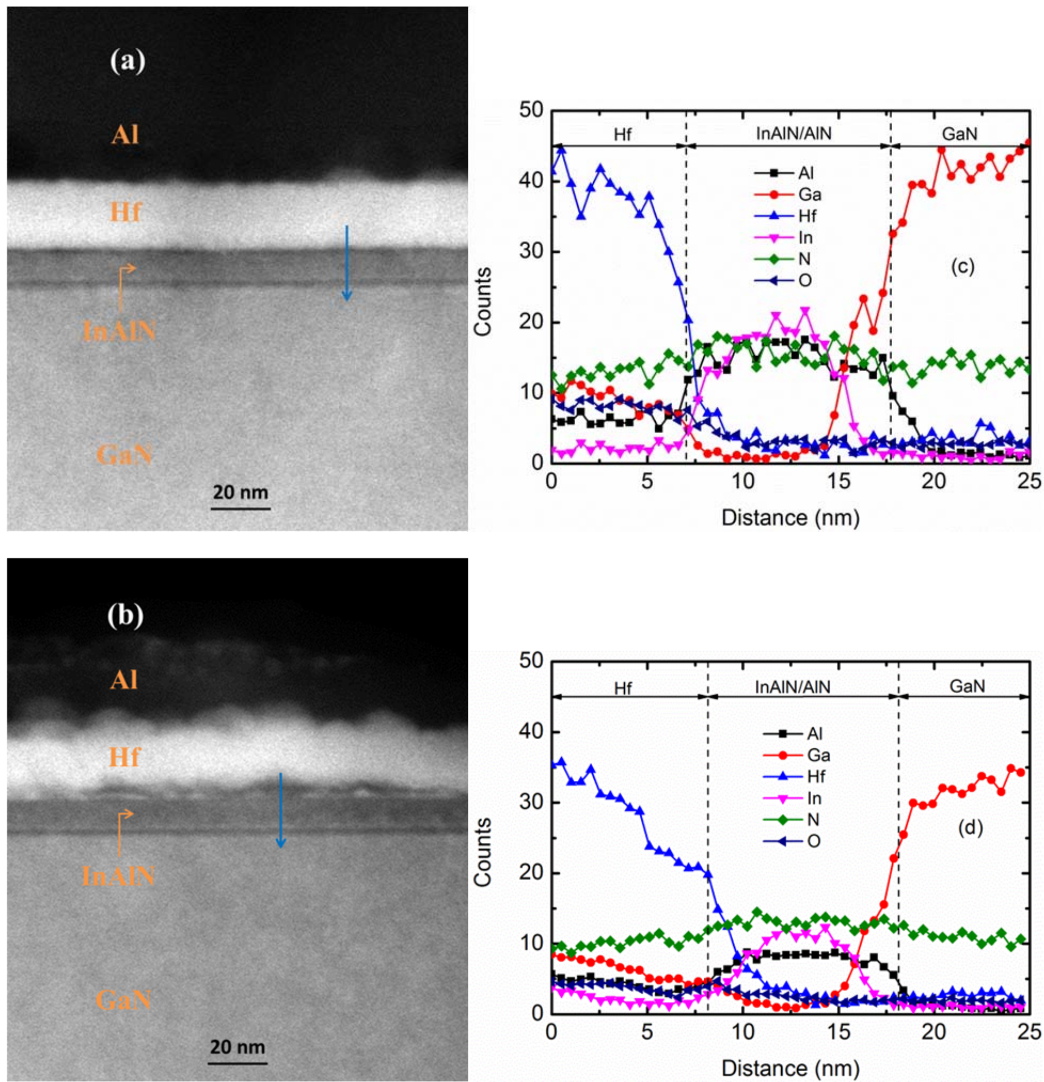
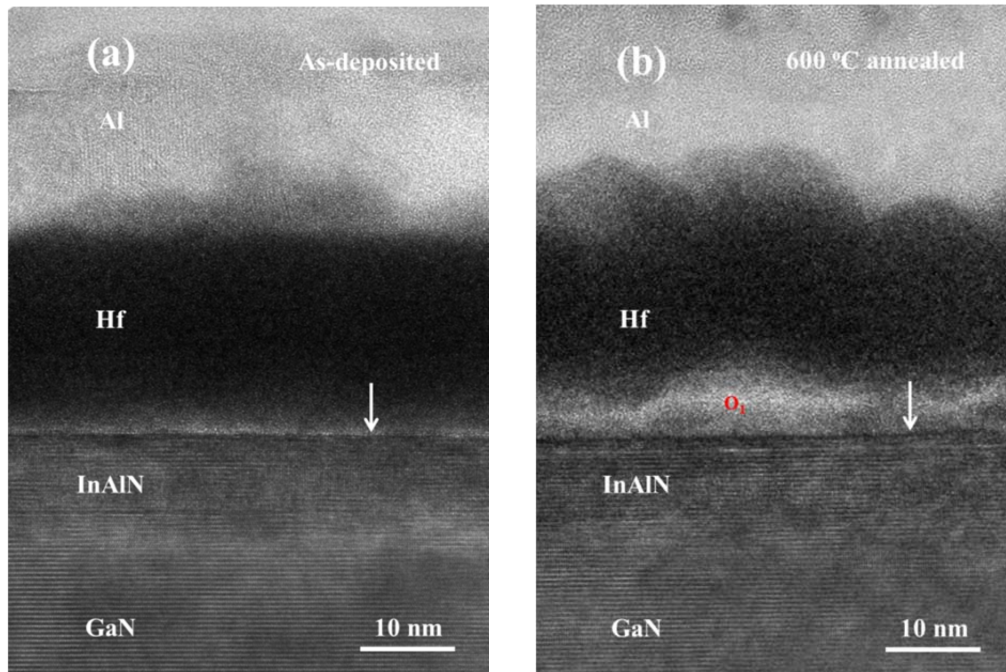


Figure 4.7 HAADF STEM images of Hf/Al/Ta contact on InAlN/GaN (a) for the as-deposited condition, and (b) after annealing at 600 ^{o}C in vacuum for 60 s. EDX line scans across the interface between Hf/Al/Ta contact and InAlN/GaN for the sample (c) before and (d) after 600 ^{o}C annealing, where the line scan position and direction are indicated in (a) and (b).

Figures 4.8(a) and 4.8(b) show the high resolution bight-field STEM images across the interface between Hf/Al/Ta contact and InAlN/GaN before and after 600 ^{o}C annealing. It is noted that the contrast at the interface, as shown by arrows in Figures 4.8(a) and 4.8(b), is different between the as-deposited and annealed

samples, which could point towards the formation of Hf(Al)N after thermal treatment. Moreover, broadening of the Hf layer and the region at the proximity of metal-semiconductor interface after annealing seen in Figure 4.8(b) indicates the inter-diffusion between Al and Hf. As the inter-diffusion of Al and Hf, and the formation of Hf-Al alloy have been clearly evident from ToF-SIMS in Figure 4.6 and our previous XRD results in Figure 4.5, we believe the bright region within the metal near the InAlN layer in Figure 4.8(b) corresponds to an intermediate density Hf-Al alloy. The formation of this alloy is confirmed by spot EDX spectrum (O: 45.6, Al: 16.4 and Hf: 38.1 in atomic percentage), as show in Figure 4.8(c). The high amount of oxygen observed here could be due to the oxidation during sample preparation. On the other hand, a dark region next to the bright region towards the metal-semiconductor interface, as shown by the arrow in Figure 4.8(b), could result from the reaction between metal and InAlN/GaN after annealing, which is most likely due to the formation of Hf-N, as a result of nitrogen out-diffusion observed in SIMS results.



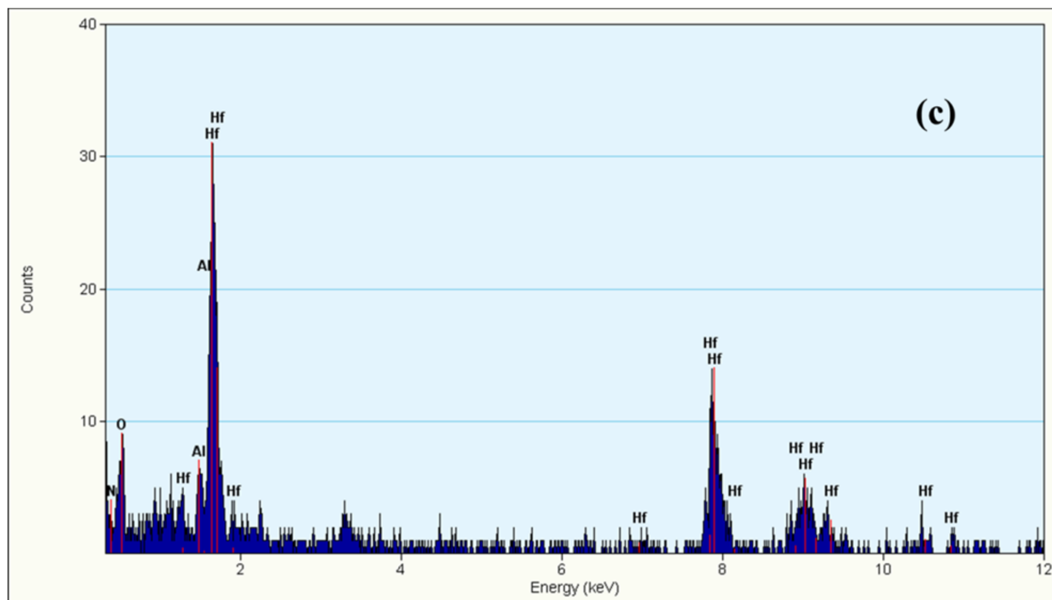


Figure 4.8 High resolution bright-field TEM images across the interface between Hf/Al/Ta contact and InAlN/GaN (e) before and (c) after 600 ^{o}C annealing. (c) The spot EDX spectrum at O_1 indicated in (b).

4.6 Carrier transport in Hf/Al/Ta contacts on InAlN/GaN

As shown the TEM results before, the metal-semiconductor interface for the sample after annealing at 600 ^{o}C shown in Figure 4.8(b) is found to be smooth. This is in contrast to traditional Ti-based contacts (e.g., Ti/Al/Ni/Au) annealed at higher temperature (> 800°C), where spike formation or ohmic metal penetration (i.e., contact inclusions) through the InAlN barrier layer was detected, thus leading to a rough metal-semiconductor interface and forming a direct carrier transport path [59, 119, 120] between the contact and semiconductor. Owing to the existence of contact inclusions, a parallel network of low resistive paths has been proposed to understand the transport mechanism for these spike-based contacts [121]. For Hf/Al/Ta ohmic contacts on InAlN/GaN with a smooth metal-semiconductor interface, the carrier transport mechanism could be different and this was investigated by means of the I-V-T measurements, as follows.

To investigate the carrier transport mechanism for the samples annealed at 600 ^{o}C, I-V measurement was carried out at various sample temperatures, ranging from ~300 to 500 K, as shown in Figure 4.9(a). The extracted values for R_c, ρ_c, and R_{sh} are plotted in Figure 4.9(b). As seen in Figure 4.9(a), the current decreases with increasing sample temperature, which means the total resistance between two contacts increases with increasing temperature. This is due to the increase in R_{sh}, as shown in Figure 4.9(b), as ρ_c decreases with increasing temperature. As a result, R_c has a marginal temperature dependence since $R_c = (R_{sh} \times \rho_c)^{1/2}$. The above phenomenon of R_{sh} increasing with increasing temperature was also widely reported for AlGaN/GaN heterostructures [122-124]. It is known that R_{sh} is

determined by the 2DEG density (n_s) and the mobility (μ), i.e., $R_{sh} \propto 1/(n_s\mu)$. Since n_s has a very weak temperature dependence [125, 126], the increase in R_{sh} is therefore believed to be mainly contributed by reduced μ, owing to lattice vibration at high measurement temperature, i.e., the optical phonon scattering [127, 128]. This conclusion could also be supported by the successful fitting, as shown in Figure 4.10, of R_{sh} to the following power-law relation with temperature [121, 122],

$$R_{sh} = R_{sh0} \left(\frac{T_0}{T}\right)^{\gamma}, \quad (4.1)$$

where R_{sh0} is the R_{sh} at T_0 = 300 K and γ is the power index. The R_{sh0} obtained was 525 Ω/□, and the γ was -1.55 from curve fitting. The discrepancy observed in the value of R_{sh0} obtained from curve fitting and that from Hall measurements (~458 Ω/□) is likely due to the increased sheet resistance of InAlN/GaN after annealing at 600 °C [57]. It is noted that the γ value obtained is very close to those previously reported in InAlN:Mg/GaN systems (-1.57) [121]. Furthermore, this amplitude of γ is lower than that of AlGaN/GaN heterostructures (~-2.18-3.42) [122-124, 129], which indicates a weaker temperature dependence of R_{sh} (and 2DEG mobility, μ, as well) in the InAlN/GaN substrate.

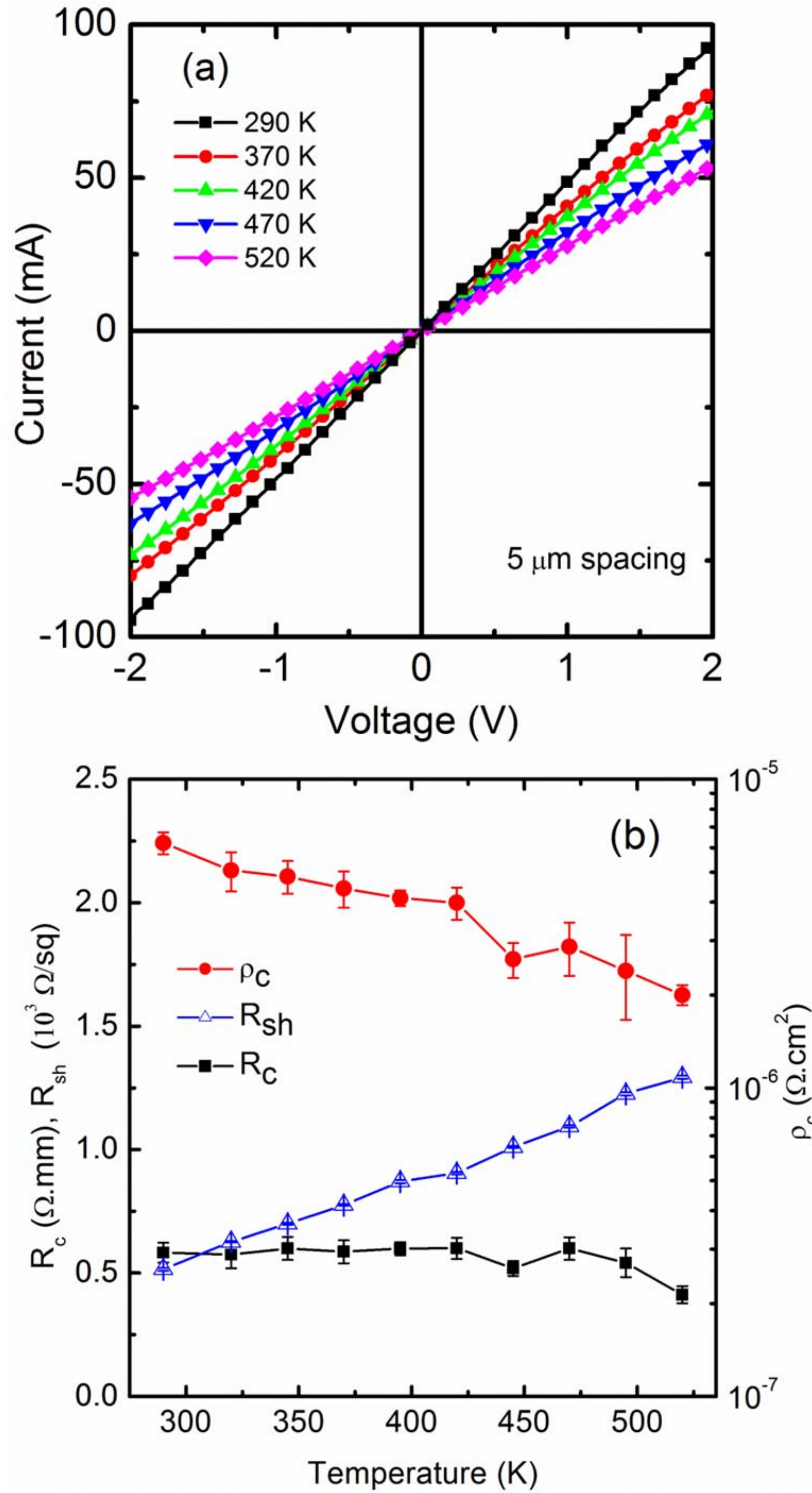


Figure 4.9 (a) Typical I-V curves for a contact spacing of 5 μm, and (b) R_{sh}, R_c and ρ_c of Hf/Al/Ta (15/200/20 nm) contacts on InAlN/GaN annealed at 600 °C as a function of measurement temperature.

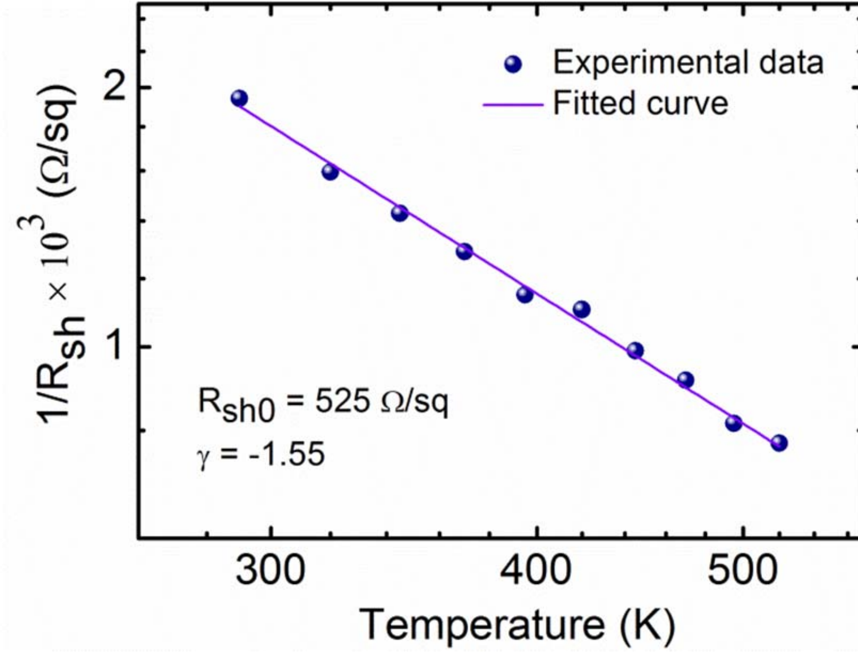


Figure 4.10 R_{sh}-T graph for the Hf/Al/Ta contacts on InAlN/GaN annealed at 600 ^{o}C.

The measured ρ_c as a function of temperature for the 600 ^{o}C annealed samples are shown in Figure 4.11. It is obvious that the ρ_c is temperature dependent and it decreases with increasing temperature. To understand the carrier transport for Hf/Al/Ta ohmic contacts on InAlN/GaN with a smooth metal-semiconductor interface, we fit our ρ_c data to three well known carrier transport models [130] for metal-semiconductor contacts, i.e., thermionic emission (TE), thermionic field emission (TFE), and field emission (FE). It is found that our data fit well the TFE model,

$$\rho_C = \frac{1}{qA_{Ri}} \frac{k^2}{\sqrt{\pi(\Phi_B+E_n)E_{00}}} cosh(\frac{E_{00}}{kT}) \sqrt{coth(\frac{E_{00}}{kT})} \exp(\frac{\Phi_B+E_n}{E_0} - \frac{E_n}{kT}), \quad (4.2)$$

as shown in Figure 4.11. In the above expression, $E_{00} = qh/4\pi\sqrt{N_D/m_n^*\varepsilon}$, $E_0 = E_{00}\coth(E_{00}/kT)$, and $A_{Ri} = 4\pi m_n^* q\, k_B^2/h^3$ is the Richardson constant. Here, h is the Planck constant, q is the electron charge, k is the Boltzmann constant, m_n^* and ε are the effective electron mass (0.22m_e) and dielectric constant of GaN (8.9ε_0), respectively, Φ_B is the barrier height to carrier transport, N_D is the electron carrier concentration, and E_n is the energy difference between the conduction-band edge and the Fermi level of the semiconductor. The Richardson constant was calculated to be 26.64 $Acm^{-2}K^{-2}$ for GaN. The other parameters including Φ_B, E_n and E_{00} are derived from best fitting to the experimental data. The fitted values of Φ_B of 0.48 eV, N_D of 1.72 × 10^{19} cm^{-3} and E_{00} of 0.055 eV and the theoretical curve are shown in Figure 4.11. N_D is 1.72 × 10^{19} cm^{-3} derived from $E_{00} = qh/4\pi\sqrt{N_D/m_n^*\varepsilon}$. The characteristic energy E_{00} is related to the tunneling probability for electrons in ohmic contacts [131]. It should be noted that TE dominates when $E_{00}/kT \leq 0.5$, TFE dominates when $0.5 < E_{00}/kT < 5$, and FE dominates when $E_{00}/kT \geq 5$. Here, for our case, E_{00}/kT is 2.13 at 300 K, which lies in the TFE regime, thus suggesting that our fitting results are reasonable. Additionally, a high carrier concentration N_D of 1.72 × 10^{19} cm^{-3}, which is related to the 2DEG, is obtained and this corroborates well with efficient tunneling process through the thin InAlN layer. This also agrees with the study of Kim et al., where a similar order of magnitude of N_D ~ 2.3 × 10^{19} cm^{-3} resulted in an significant tunneling process [121].

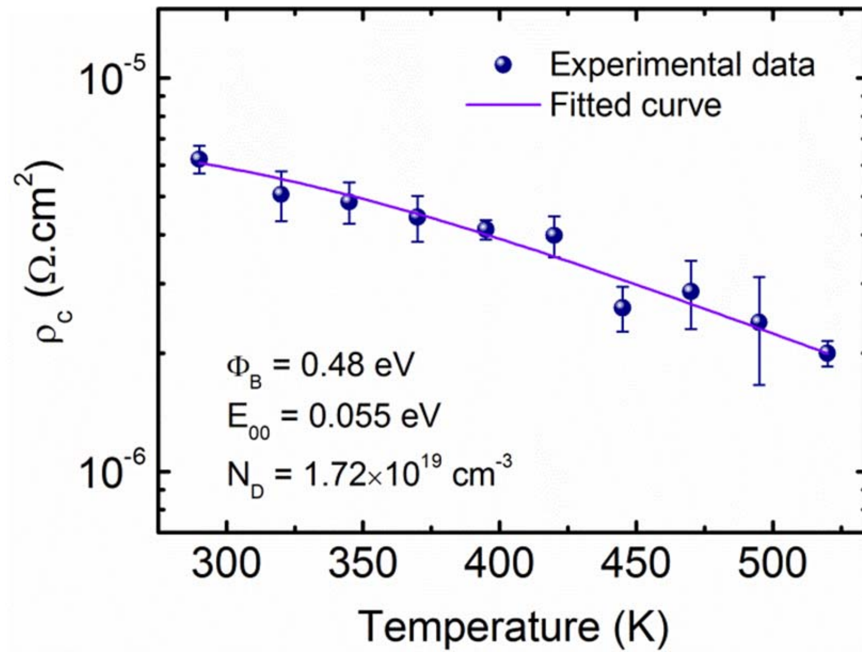


Figure 4.11 ρ_c –T graph for the Hf/Al/Ta contacts on InAlN/GaN annealed at 600 ^{o}C.

Furthermore, based on the observation in Figure 4.7, no spikes or contact inclusions were found through the InAlN barrier layer. This indicates that the tunneling of electrons from 2DEG has to overcome an effective barrier of Φ_B ~0.48 eV to transport through the InAlN barrier via the TFE process. This is different from the study of Kim et al.[121], where the contact inclusions (TiN) penetrate through the InAlN barrier layer, forming a parallel network of low resistive paths of TiN to allow direct carrier transport between the contact and the 2DEG channel in GaN. As seen in Figure 4.3(a), the current for the as-deposited sample shows a very small current passing through the contacts before annealing, whereas a significant current was obtained after 600 ^{o}C annealing. This dramatic change of electrical property for the Hf-based ohmic contacts after annealing can

be understood through the series two-barrier model [122]. Figure 4.12 shows a schematic based on this model for our Hf/Al/Ta contacts on InAlN/GaN. Before annealing, there is a relatively thick physical barrier of 10 nm InAlN/AlN between the metal and 2DEG (Φ_{B0}), thus resulting in limited chances for 2DEG to tunnel through it. However, as discussed earlier, a modified InAlN layer with a high density of donor-like N vacancies is formed in the proximity of the metal-semiconductor interface (region 5 shown in Figure 4.12) after annealing at 600 ^{o}C. This could lead to the formation of two energy barriers, as shown in Figure 4.12, with Φ_{B1} between metal and modified InAlN, and Φ_{B2} between unaltered InAlN and 2DEG. The modified energy barrier Φ_{B1} is likely to be very thin, thus allowing easy tunneling of electrons, leaving the carrier transport predominantly limited by the other barrier (Φ_{B2}) via TFE process. The barrier height obtained from TFE curve fitting of Φ_B ~0.48 eV is probably that of Φ_{B2}, or an effective value of the 2 energy barriers (Φ_{B1} and Φ_{B2}) in series.

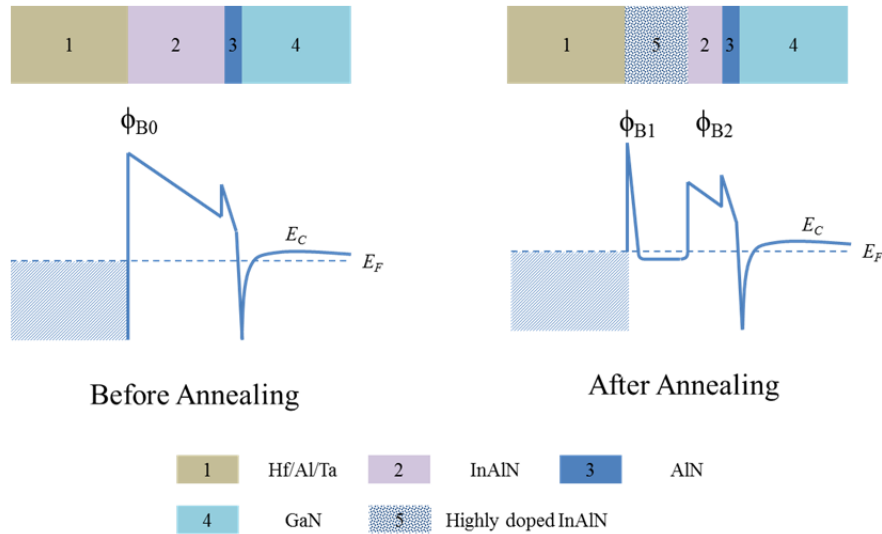


Figure 4.12 The energy band schematics of ohmic metal and InAlN/AlN/GaN for the samples before and after annealed at 600 ^{o}C.

4.7 Thermal stability of Hf/Al/Ta ohmic contact on InAlN/GaN

The thermal stability of ohmic contacts is also a concern for electron devices in a long-term operation. Hence, as an evaluation of enduring reliability, preliminary thermal aging test at 350 ^oC in air of the Hf/Al/Ta (15/200/20 nm) contacts on InAlN/GaN was also carried out. The result is shown in Figure 8 with no significant change in R_c observed after 200 hours at 350 ^oC in air, indicating a thermally stable property for the Hf/Al/Ta contacts.

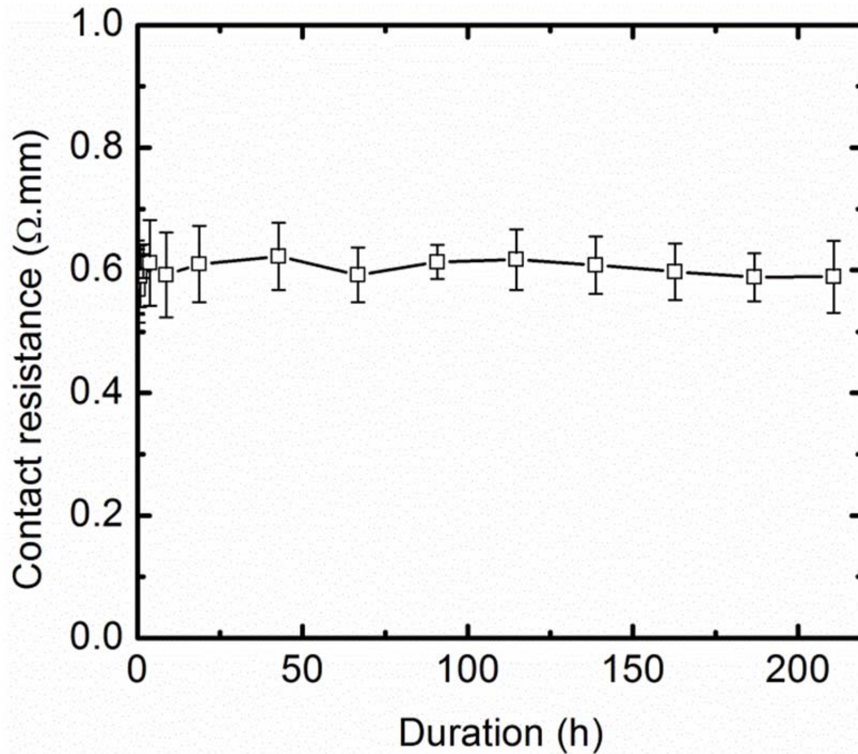


Figure 4.13 Preliminary thermal stability testing in air for Hf/Al/Ta (15/200/20 nm) contacts on InAlN/GaN at 350 ^oC.

4.8 Summary

In this chapter, Hf/Al/Ta contact on InAlN/GaN was found to exhibit the lowest ohmic transition temperature of 550 ^{o}C compared to other transition metals (Ti, Ta, Zr, Nb, and V). A minimum contact resistivity of $6.7 \pm 0.58 \times 10^{-6}$ $\Omega \cdot cm^2$ and contact resistance of 0.59 ± 0.03 $\Omega \cdot mm$ are achieved for the optimized Hf/Al/Ta (15/200/20 nm) ohmic contact with annealing at 600 ^{o}C in vacuum. STEM and ToF-SIMS results have revealed that the contacts have a smooth metal-semiconductor interface, and the formations of HfN and Hf-Al alloy near the interface, and these could be crucial to achieving good ohmic properties. The current-voltage-temperature (I-V-T) measurements have indicated a significant temperature dependence of the sheet resistance (R_{sh}) of InAlN/GaN and contact resistivity (ρ_c). The former follows a power-law (i.e., $R_{sh} \propto T^{1.55}$), owing possibly to optical phonon scattering, while analysis of the latter has shown that thermionic field emission (TFE) is the dominant carrier transport mechanism in the Hf/Al/Ta ohmic contacts on InAlN/GaN. The effective barrier height and carrier density of 2DEG are found to be 0.48 eV and 1.72×10^{19} cm^{-3}, respectively, leading to an efficient electron tunneling through the InAlN barrier. In addition, the carrier transport through the Hf/Al/Ta ohmic contacts on InAlN/GaN with a smooth metal-semiconductor interface can be understood using a series two-barrier model. Last but not least, the Hf/Al/Ta contacts on InAlN/GaN have been found to be stable at 350 ^{o}C in air for more than 200 hours.

Chapter 5

Performance comparison between InAlN/GaN HEMTs with Hf/Al/Ta and Ti/Al/Ni/Au ohmic contacts

From the experimental results presented in chapter 4, we can observe that Hf/Al/Ta ohmic contacts on InAlN/GaN exhibit good electrical properties with low thermal budget. In this chapter, we will investigate the effects of Hf/Al/Ta ohmic contacts with such low thermal budget on the device electrical characteristics with respect to comparable transistor with conventional Ti/Al/Ni/Au ohmic contacts.

5.1 Introduction

As we discuss in Chapter 4, the traditional Ti/Al/X/Au contacts usually need high annealing temperature (> 800 ^{o}C) to achieve a low contact resistance. At such high temperatures, the sheet resistance (R_{sh}) of the GaN based heterostructures can increase [57, 121], which may lead to higher on-state resistance (R_{on}) and limit the current delivery capability of transistors. In addition, the high annealing temperature can lead to spike formation across the interface between ohmic metal and semiconductor, thus leading to a lower device breakdown voltage [53, 132]. The high annealing temperature also causes the balling of molten Al due to its low melting point (660 °C), which leads to a rough contact surface. Furthermore, the formation of Al_4Au alloy, which has a low melting point of 525 ^{o}C, in the Ti/Al/X/Au contacts results in an even worse contact surface roughness [83, 133]. The rough surface may cause reproducibility and reliability issues, especially in

highly scaled devices. Lastly, it is noted that Au is not compatible with the Si CMOS process, owing to its high diffusivity in silicon. Therefore, in this section, we will conduct a systematic comparison between Hf/Al/Ta and Ti/Al/Ni/Au contacts in terms of contact properties and device performance.

5.2 Experiment

The InAlN/GaN-on-Si heterostructure and ohmic contact fabricated are the same as the procedures described in Chapter 4. Hf/Al/Ta (15/200/20 nm) contacts were prepared at 600 ^{o}C in vacuum for 60 s, namely, under the optimal condition. The conventional Ti/Al/Ni/Au (25/200/40/100 nm) contact system was also deposited, by means of electron beam evaporation, to serve as a reference for comparison. The Ti/Al/Ni/Au ohmic contacts were annealed at 800 ^{o}C for 60 s in vacuum. Finally, two types of InAlN/GaN-on-Si HEMTs with either Hf/Al/Ta or conventional Ti/Al/Ni/Au (25/200/40/100 nm) source/drain ohmic contacts were fabricated, with Ni/Au (30/80 nm) as the Schottky gate metal. All the devices in the present study were not passivated. The DC current–voltage (I–V) characterizations and breakdown measurements of the InAlN/GaN HEMTs were carried out using an Agilent B1505A semiconductor parameter analyzer. Optical microscope and atomic force microscope (AFM) were used to examine the edge acuity and surface morphology of the contacts. Cross-sectional transmission electron microscopy (TEM) was used to investigate the interface between substrate and ohmic metals.

5.3 Electrical properties comparison for LTLM structures

Figure 5.1(a) shows the I-V curves of Hf- and Ti-based contacts are linear, indicating their ohmic behavior and a higher current for Hf/Al/Ta contacts. Figure 5.1(b) shows the total resistance (R_T) between two contact pads, as a function of the contact pad spacing (d) of the LTLM structure, for the optimized Hf/Al/Ta (15/200/20 nm) and conventional Ti/Al/Ni/Au (25/200/40/100 nm) ohmic contacts on InAlN/GaN. The R_c, ρ_c and R_{sh} values extracted from the best linear regression fit of the R_T-d for Hf/Al/Ta and Ti/Al/Ni/Au contacts are summarized in Table 5.1. The Ti/Al/Ni/Au contacts exhibit a R_c of 0.51 Ω.mm and ρ_c of 4.75×10^{-6} Ω.cm^2 after annealing at 800 ^{o}C for 60 s in vacuum, while the Hf/Al/Ta (15/200/20 nm) contacts show a slightly higher R_c of 0.58 Ω.mm and higher ρ_c of 6.75×10^{-6} Ω.cm^2 after annealing at 600 ^{o}C for 60 s in vacuum. Although the Ti/Al/Ni/Au contacts show a lower R_c and ρ_c after annealing, the higher annealing temperature has led to an increased R_{sh} of 566 Ω/□ (by ~13.4 %), compared to 495 Ω/□ for the substrate with Hf/Al/Ta contacts annealed at a lower temperature of 600 ^{o}C. The high annealing temperature induced R_{sh} degradation was also observed by other researchers [57, 121]. Therefore, the Hf/Al/Ta contact with a lower thermal budget can suppress the R_{sh} degradation of the InAlN/GaN heterostructure and could lead to a lower parasitic access resistance for HEMTs when used to replace the Ti/Al/Ni/Au contact. This is desirable, especially for high power HEMTs, which usually have several tens of microns of source-to-drain spacing.

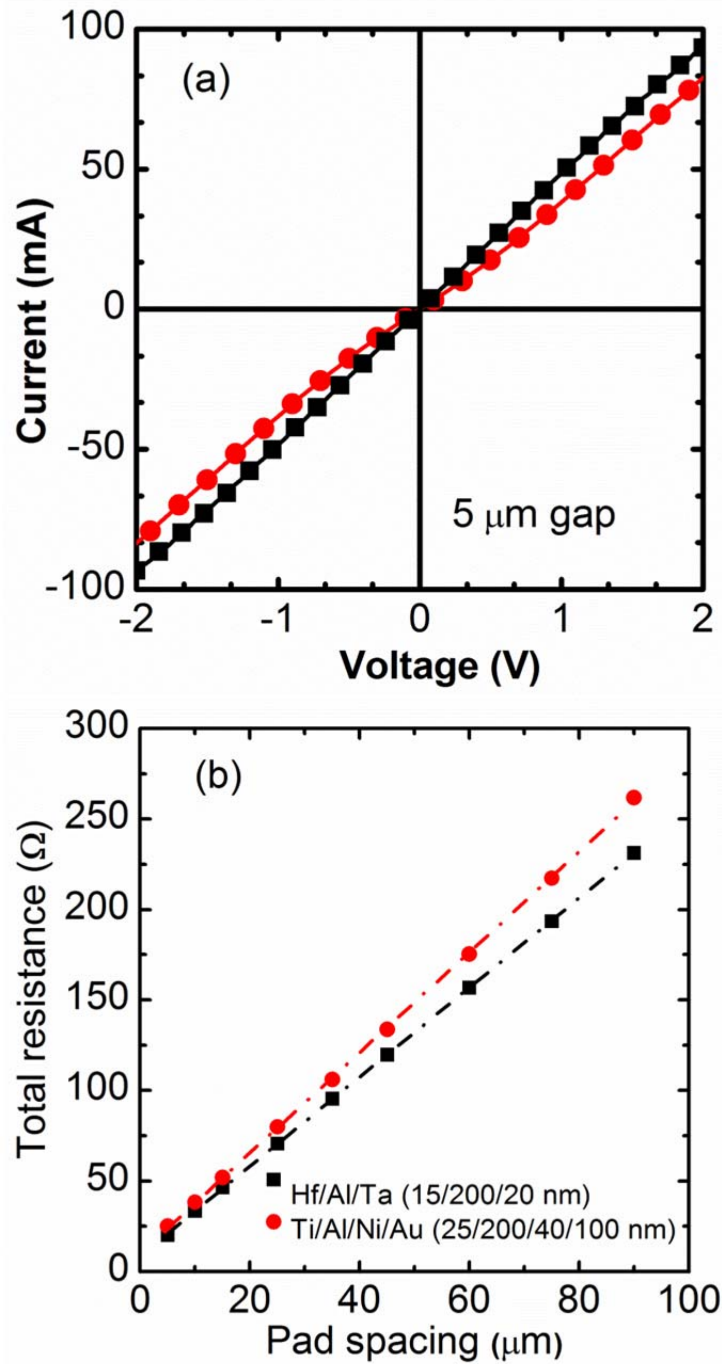


Figure 5.1 (a) I–V curves of the TLM patterns with a pad spacing of 5 μm for Hf/Al/Ta (15/200/20 nm) and Ti/Al/Ni/Au (25/200/40/100 nm) ohmic contacts. (b)Total resistance as a function of pad spacing of TLM patterns for Hf/Al/Ta (15/200/20 nm) and Ti/Al/Ni/Au (25/200/40/100 nm) ohmic contacts on InAlN/GaN

Table 5.1 The contact resistance, specific contact resistivity of Hf/Al/Ta (15/200/20 nm) and Ti/Al/Ni/Au (25/200/40/100 nm) contacts, and the sheet resistance of InAlN/GaN-on-Si substrate. The contact annealing temperatures are also shown.

	Annealing temperature (^{o}C)	Contact resistance (Ω.mm)	Specific contact resistivity (Ω.cm^2)	Sheet resistance (Ω/□)
Hf/Al/Ta	600	0.58	6.75×10^{-6}	495
Ti/Al/Ni/Au	800	0.51	4.75×10^{-6}	566

5.4 Contact surface morphology comparison

Figures 5.2(a)-5.2(d) show the optical and AFM images of the surface for the Ti/Al/Ni/Au (25/200/40/100 nm) and Hf/Al/Ta (15/200/20 nm) contacts after annealing. Compared with Ti/Al/Ni/Au, Hf/Al/Ta possesses a much smoother surface. The root-mean-square (RMS) surface roughness (R_a) decreases drastically from 159 nm for Ti/Al/Ni/Au to 7.6 nm for Hf/Al/Ta. The much improved surface morphology for the Hf/Al/Ta contact is likely owing to its low annealing temperature (600 ^{o}C), which prevents the Al balling effect, and the absence of Al_4Au formation. The high thermal budget of the Ti/Al/Ni/Au contacts (800 ^{o}C) has led to a rough surface morphology, which may cause problems of reproducibility and reliability when scaling down the devices as the ohmic contacts could not sustain good edge acuity at such a high temperature treatment.

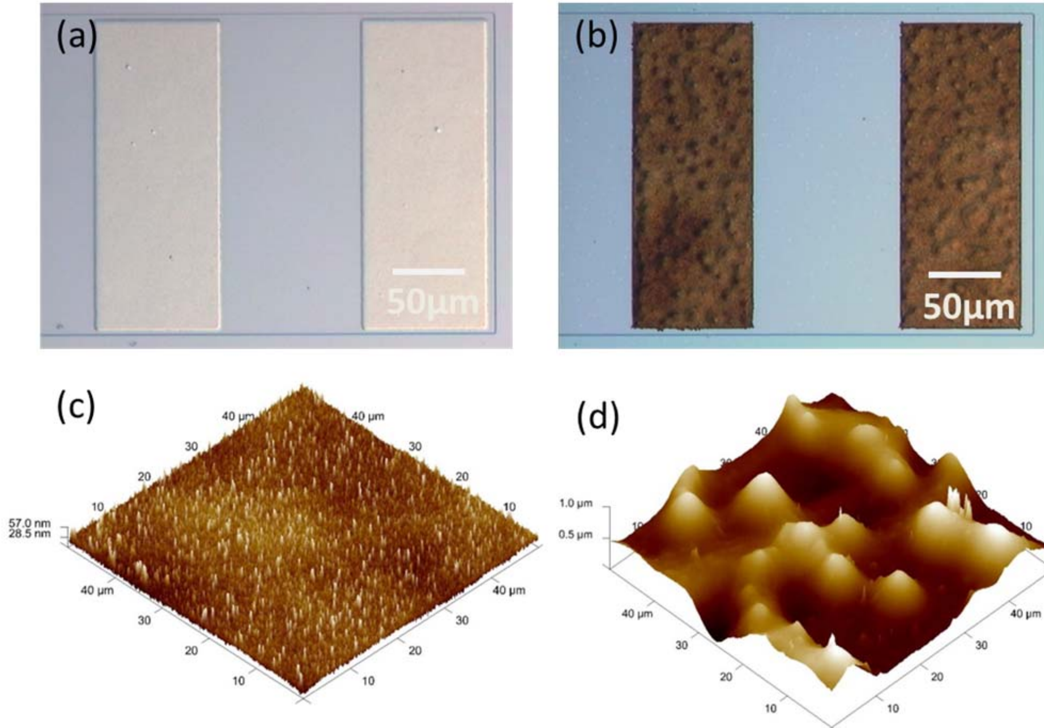


Figure 5.2 Optical microscope and AFM images of the ohmic contact surface for InAlN/GaN HEMTs: (a) optical and (c) AFM images of Hf/Al/Ta (15/200/20 nm) after annealing at 600°C in vacuum for 60 s; (b) optical and (d) AFM images of Ti/Al/Ni/Au (25/200/40/100 nm) after annealing at 800 ^{o}C in vacuum for 60 s.

5.5 Metal-semiconductor interface comparison

Figures 5.3(a) and 5.3(b) show the cross sectional TEM images of Ti/Al/Ni/Au (25/200/40/100 nm) and Hf/Al/Ta (15/200/20 nm) on InAlN/GaN heterostructure after thermal annealing. In the Ti/Al/Ni/Au contact, as shown in Figure 5.3(a), significant metal inter diffusion has happened among the various metal layers after 800 ^{o}C annealing. It is seen that Al and Ni has reacted and out diffused to yield Ni-Al alloy on the top, while most of Au has in diffused and reacted with Al to form Au-Al alloy, which shows that Ni is not an effective Au diffusion barrier.

Ti and/or Ti-Al alloy has reacted with the substrate, leading to contact inclusions or spikes formation. Furthermore, it is seen that the contact inclusions penetrate through the InAlN barrier layer and are in direct contact with the GaN channel layer. This indicates that two electron transport mechanisms are probably responsible for the Ti/Al/Ni/Au ohmic contact formation[59, 119]: 1) a tunneling mechanism as a result of Ti reacting with the InAlN layer, thus forming Ti(Al)N and leading to a large number of donor-like nitrogen vacancies being formed in the proximity of the metal-semiconductor interface that helps reduce the width of the Schottky barrier; and 2) a direct electron transport path via the localized contact inclusions that penetrate the InAlN barrier layer. The two mechanisms are usually observed in the Ti/Al/Ni/Au contact after high temperature annealing. The contact inclusion transport mechanism should dominate over the tunneling mechanism, since it allows electrons to flow freely between the contacts and 2DEG channel. This has been confirmed by the study for mechanism of carrier transport in Chapter 4. In the case of Hf/Al/Ta contact, as shown in Figure 5.3(b), all the metal layers (Hf, Al and Ta) do not mix well together due to the low annealing temperature, and no contact inclusion formation and penetration through the InAlN barrier layer is observed. As demonstrated in Chapter 4, the main electron transport mechanism in the Hf/Al/Ta ohmic contact is thermionic field emission.

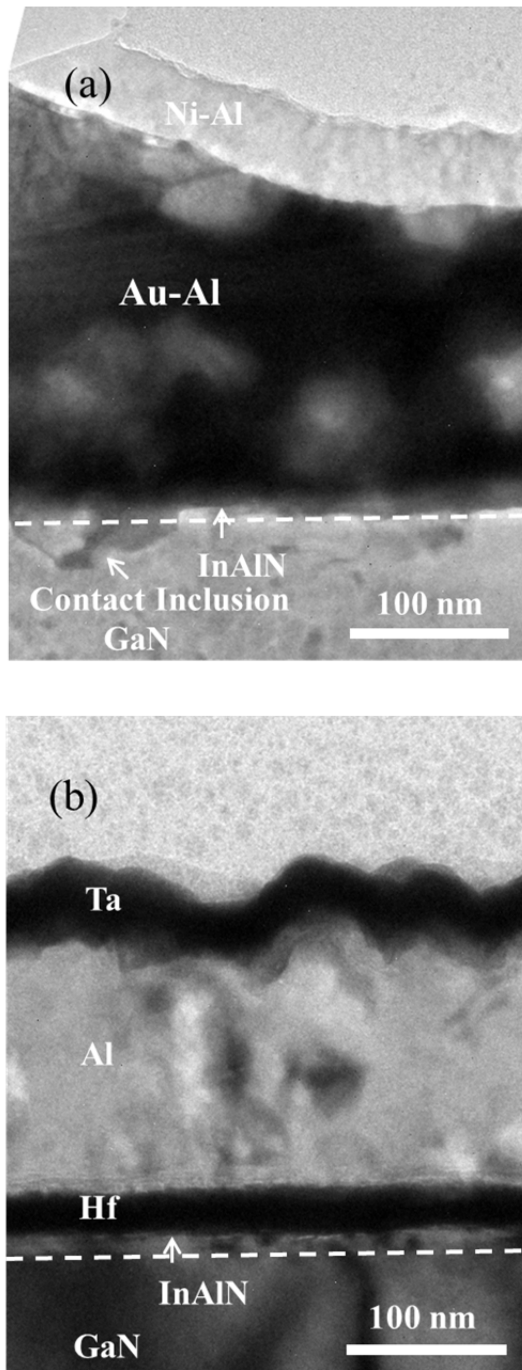


Figure 5.3 Cross-sectional TEM images of metal contacts on InAlN/GaN: (a) Ti/Al/Ni/Au (25/200/40/100 nm) after annealing at 800 ^{o}C, and (b) Hf/Al/Ta (15/200/20 nm) after annealing at 600 ^{o}C.

5.6 Device performance comparison

5.6.1 DC characteristics

To examine the impact of Hf/Al/Ta ohmic contacts, compared to conventional Ti/Al/Ni/Au ohmic contacts, on device performance, two types of InAlN/GaN-on-Si HEMTs with either Hf/Al/Ta (15/200/20 nm) or Ti/Al/Ni/Au (25/200/40/100 nm) source/drain ohmic contacts were fabricated. The Schottky gate metal used was Ni/Au (30/80 nm). The Hf/Al/Ta (15/200/20 nm) contacts were annealed at 600 ^{o}C in vacuum for 60 s and the Ti/Al/Ni/Au (25/200/40/100 nm) contacts were annealed at 800 ^{o}C in vacuum for 60 s, while the Ni/Au Schottky contacts were not given any annealing. Figure 5.4 shows the typical DC output and transfer characteristics of the two types of HEMTs. The measured HEMTs have a gate length, L_G = 1 μm; gate-to-source distance, L_{GS} = 2 μm; and gate-to-drain distance, L_{GD} = 4 μm. The gate width is W_G = 2 × 50 μm. As shown in Figures 5.4(a) and 8(b), a similar threshold voltage (V_{th}) of approximately -3 V is observed, which is expected since the Schottky contact metal is identical in the two types of HEMTs; a similar maximum drain current ($I_{D,max}$) of 740 mA/mm at V_{GS} = 1.5 V and a comparable maximum transconductance ($g_{m,max}$) of 175 mS/mm at V_{DS} = 10 V are obtained for the two types of HEMTs. On the other hand, the on-state resistance for Hf/Al/Ta HEMTs is 7.1 Ω.mm, which is slightly better than that of Ti/Al/Ni/Au HEMTs at 7.8 Ω.mm. This probably results from the increased R_{sh} of the substrate with Ti/Al/Ni/Au contacts, as shown in Table 5.1. Therefore, there is insignificant difference between InAlN/GaN HEMTs with Hf/Al/Ta (15/200/20 nm) and Ti/Al/Ni/Au (25/200/40/100 nm) ohmic contacts, which means the Au-

free Hf/Al/Ta ohmic contact is a good candidate to replace the traditional Ti/Al/Ni/Au contacts, thus allowing the fabrication of InAlN/GaN-on-Si HEMTs (using a Au free Schottky gate metal) in a CMOS process line.

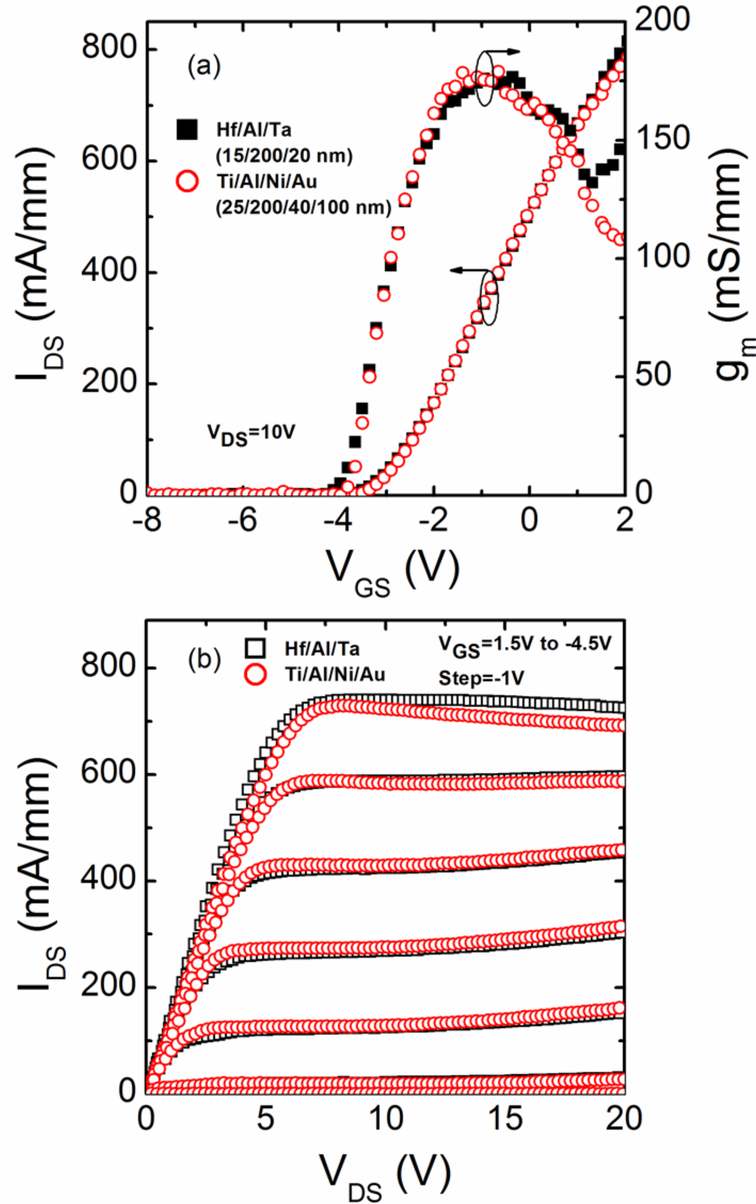


Figure 5.4 Measured DC I-V characteristics of InAlN/GaN HEMTs with Hf/Al/Ta and Ti/Al/Al/Au source/drain ohmic contacts: (a) I_G-V_{GS} characteristics measured at V_{DS} = 10 V, and (b) I_D-V_{DS} curves. The device dimensions of the InAlN/GaN HEMTs are $L_g/L_{gs}/L_{gd}/W_g = 1/2/4/2\times50$ μm.

5.6.2 Breakdown voltage

Figure 5.5(a) shows the two-terminal and three-terminal off-state breakdown measurements for Hf/Al/Ta (15/200/20 nm) and Ti/Al/Ni/Au (25/200/40/100 nm) ohmic contacts based InAlN/GaN HEMTs. Here, we define the breakdown voltage, V_{BK}, as the V_{DS} when the off-state drain current exceeds 1 mA/mm. For both the Hf and Ti based metallization schemes, a higher breakdown voltage is observed in the two-terminal measurements, as shown in Figure 5.5(a), where the breakdown is induced by the gate leakage. The results indicate that the three-terminal off-state breakdown is not induced by the gate injection as the Ni/Au Schottky gate allows only a low leakage through it for both the Hf/Al/Ta and Ti/Al/Ni/Au ohmic contact based HEMTs. To study the mechanisms of the three-terminal off-state breakdown in the Hf/Al/Ta and Ti/Al/Ni/Au based InAlN/GaN HEMTs, the leakage current through the gate, source and drain contacts were measured during the breakdown measurements and these are presented in Figure 5.5(b). For both types of HEMTs, the drain breakdown is mainly contributed by a much higher source current compared to a small gate leakage current, which means the three-terminal off-state breakdown could be attributed to the source-carrier-injection induced breakdown mechanism [132, 134, 135]. In GaN HEMTs, the GaN buffer layer is slightly n-doped due to the background doping from intrinsic nitrogen vacancies or oxygen impurities during the buffer growth by MOCVD. Therefore, at a high enough drain bias, the electrons could be injected from the source into the GaN buffer layer, which subsequently drift to the peak electrical-field region at the drain-side gate edge to trigger impact ionization in

the channel, and eventually, lead to the source-carrier-injection induced breakdown. As shown in Figure 5.5(b), the InAlN/GaN HEMTs with Ti/Au/Ni/Au contacts exhibit a higher source leakage than HEMTs with Hf/Al/Ta contacts. As a result, the latter achieve a higher breakdown voltage of 280 ± 20 V, a significant improvement of ~ 53.3% over that of the former, 187 ± 36 V.

The preceding discussion indicates that Hf/Al/Ta contacts could suppress the carrier injection from the source much better than Ti/Au/Ni/Au contacts. In InAlN/GaN HEMTs with Ti/Al/Ni/Au contacts, formation of contact inclusions or spikes has been observed due to metal diffusion under high temperature annealing, as shown in Figure 5.3(a). It is reasonable that the electric-field lines concentrate at the spikes and lead to a high electric-field region in the GaN buffer layer such that a local carrier injection into the GaN buffer layer is possible. In the case of InAlN/GaN HEMT with Hf/Al/Ta contacts, the interface between the source/drain ohmic contact and substrate is smooth, as seen in Figure 5.3(b), thus yielding a more uniform electric field distribution and suppressing the source carrier injection into the GaN buffer, therefore leading to an enhanced breakdown voltage. Replacing the Ni/Au gate by a gold-free gate, e.g., Ni/W, fully gold-free InAlN/GaN-on-Si HEMTs with improved three terminal off-state breakdown voltage can be realized using the Hf/Al/Ta source/drain ohmic contacts.

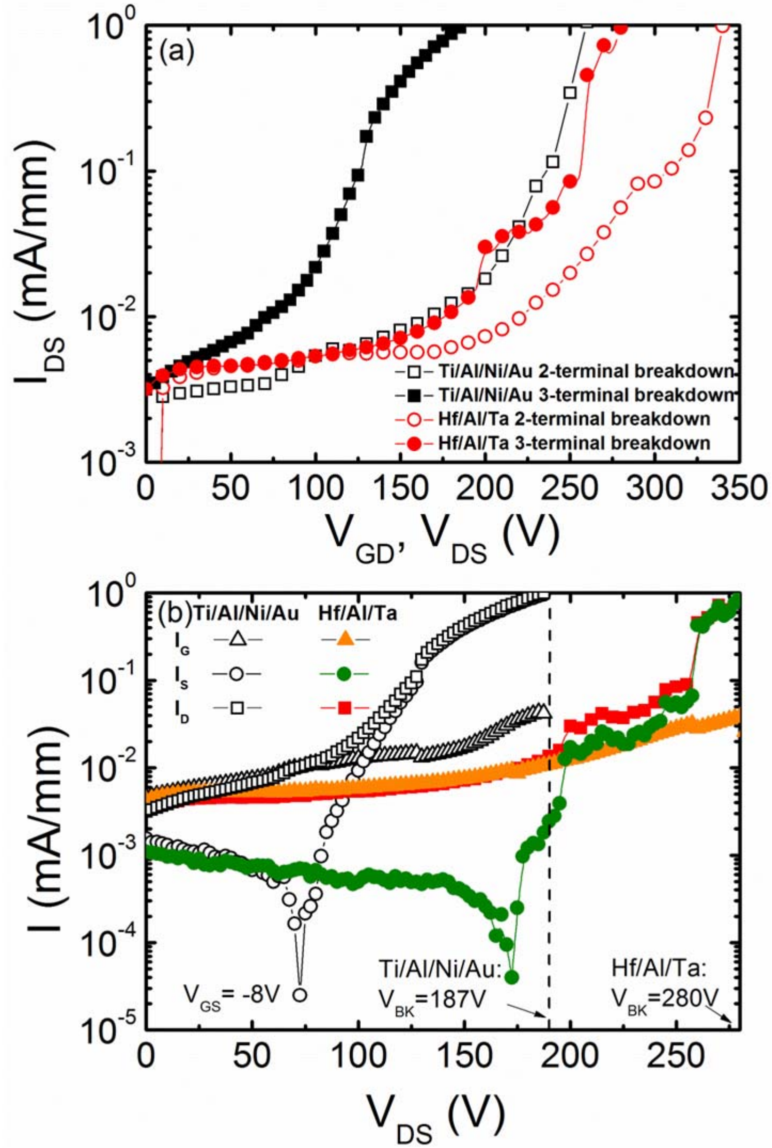


Figure 5.5 (a) Two-terminal and three-terminal off-state breakdown measurements, and (b) gate, drain, and source leakage currents (I_G, I_D, and I_S) versus drain bias (V_{DS}) in the off-state breakdown voltage measurement (V_{GS} = −8 V) of InAlN/GaN HEMTs with Hf/Al/Ta (15/200/20 nm) and Ti/Al/Ni/Au (25/200/40/100 nm) contacts. The device dimensions of the InAlN/GaN HEMTs are $L_g/L_{gs}/L_{gd}/W_g$ = 1/2/4/2×50 μm.

5.7 Summary

In this chapter, a comprehensive comparison between InAlN/GaN-on-Si HEMTs with Hf/Al/Ta ohmic contacts and conventional Ti/Al/Ni/Au ohmic contacts have been studies in terms of TLM I-V results, contact surface morphology, metal-semiconductor interface, and device performance. The RMS roughness of the contact surface is found to be as low as 7.6 nm for Hf/Al/Ta based contacts compared to 159 nm for conventional Ti/Al/Ni/Au contacts. TEM images show a smooth interface between the Hf/Al/Ta contact (with 600 ^{o}C annealing) and InAln/AlN/GaN heterostructure, in contrast to spikes formation for the 800 ^{o}C annealed Ti/Al/Ni/Au contacts. Moreover, insignificant changes are observed in terms of the DC output and transfer characteristics for InAlN/GaN-on-Si HEMTs with either the Hf/Al/Ta or Ti/Al/Ni/Au source-drain ohmic contacts. Whereas, the three-terminal off-state breakdown voltage of the former is improved significantly by ~100 V (~ 53.5 %) compared to the latter. This enhancement is possibly due to the absence of contact inclusions or spikes formation in the Hf/Al/Ta contacts, thus reducing source-carrier-injection induced breakdown mechanism. Based on our studies, the low thermal budget Hf/Al/Ta contact is a promising candidate to replace the Ti/Al/Ni/Au ohmic contact in InAlN/GaN-on-Si HEMTs.

Chapter 6

DC performance of InAlN/GaN HEMTs using $LaAlO_3$ for surface passivation

From the device results presented in the Chapter 5, the unpassivated InAlN/GaN HEMTs with Hf/Al/Ta contacts shows good performance. In this Chapter, the research work focuses on the evaluation of LaAlO3 as a surface passivation layer in InAlN/GaN HEMTs with the optimized Hf/Al/Ta contacts.

6.1 Introduction

As discussed in Chapter 1, InAlN/GaN HEMTs are promising for their excellent properties. However, applications of InAlN/GaN HEMTs are mostly restricted by surface trapping effects through drain current collapse. RF power is also much lower than that expected from the device DC characteristics due to the electron trapping states at the active surface region, which leads to dramatic degradation in the output power and the power-add efficiency (PAE) [136, 137]. Therefore, a passivation layer is necessary to reduce the density of surface states so as to mitigate the current collapse issue. The LaO_3 [138] and Al_2O_3 [67] have been reported to be effective for suppressing current collapse by surface states passivation on InAlN/GaN HEMTs. However, there is no report available for the surface passivation studies on InAlN/GaN with $LaAlO_3$. Furthermore, the $LaAlO_3$ has high thermal stability (>900 ^{o}C), and good immunity against moisture in the environment [69]. Hence, we will preliminarily examine the surface passivation

by $LaAlO_3$ and the feasibility as an alternative to popular Al_2O_3 [67] and SiN [66] passivation in this work.

6.2 Experiment

The InAlN/GaN-on-Si devices fabricated used the same procedures described in Chapter 5. The DC current–voltage (I–V) characterizations of the InAlN/GaN HEMTs were carried out using an Agilent B1500A semiconductor parameter analyzer. Hf/Al/Ta (15/200/20 nm) contacts by sputtering were annealed at 600 ^{o}C in vacuum for 60 s. The measured contact resistance is around 0.6 Ω.mm by using linear transmission-line method structure (LTLM) at room temperature. Schottky gate metallization was realized by sputtering, consisting of Ni/W (50/50 nm) layers. The surface of HEMTs was then passivated by 25 nm $LaAlO_3$ (LAO) deposited by PLD. DC characteristics measurements were measured and compared.

6.3 Device performance

6.3.1 Hall measurements

Hall measurements were carried out on both LAO-passivated and unpassivated InAlN/GaN-on-Si HEMTs at room temperature and the results are summarized in Table 6.1. It was found that the unpassivated HEMTs yielded a sheet carrier density (n_s) of 2.1×10^{13} cm^{-2}, carrier mobility (μ) of 833 $cm^2/V\cdot s$ and sheet resistance (R_{sh}) of 360 Ω/□. As for the LAO-passivated HEMTs, the electron carrier mobility decreased to 810 $cm^2/V\cdot s$, by around 3% after the 25 nm LAO

deposited. This decease of carrier mobility in the 2DEG channel after LAO passivation is probably due to an enhanced electron-electron coulomb scattering with a higher electron sheet density n_s in InAlN/GaN heterostructure, which was increased to 2.43×10^{13} cm^{-2}, almost by 16% compared to the unpassivated sample. This could be due to positive charges induced by LAO passivation layer at dielectric/InAlN interface, which is similar to other dielectric passivation in GaN HEMTs [139-141]. However, the real cause is still unclear in this preliminary work at this moment. Consequently, a 12% improvement of sheet resistance ($\propto 1/(n_s \times \mu)$) in InAlN/GaN was obtained in InAlN/GaN HEMTs with 25 nm LAO passivation compared to the unpassivated HEMTs. This indicates a lower resistance in the access region between the gate and source/drain, and hence better device performance for LAO-passivated devices is expected.

Table 6.1 Properties of InAlN/GaN-on-Si wafer before and after 25 nm PLD $LaAlO_3$ passivation.

Passivation	Carrier Concentration	Mobility (cm^2/V·s)	Sheet Resistance (Ω/□)
Before	2.1×10^{13} cm^{-2}	833	360
After	2.43×10^{13} cm^{-2}	810	317

6.3.2 DC characteristics

Two-terminal gate leakage current (I_{GS}) of the unpassivated and 25 nm LAO passivated InAlN/GaN HEMTs was measured are shown in Figure 6.1. As seen, LAO-passivated HEMTs exhibit a gate leakage of ~2.22×10^{-2} mA/mm at V_{GS} = -10 V, which is similar to that of the unpassivated devices ~2.16×10^{-2} mA/mm at

the same bias. This shows that 25 nm LAO passivation does not degrade the Schottky gate performance.

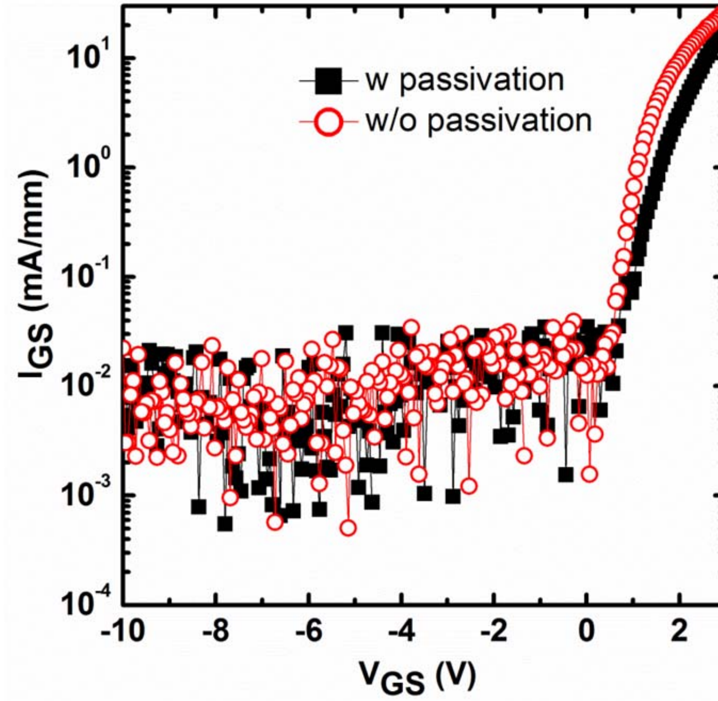


Figure 6.1 Two-terminal gate leakage current (I_{GS}) measured on Schottky diodes before and after 25 nm LAO passivation.

Figures 6.2(a) and 6.2(b) show the typical DC output and transfer characteristics of LAO-passivated and unpassivated InAlN/GaN-on-Si HEMTs, respectively. The measured devices have a gate length of 2 µm; gate-to-source distance of 2 µm and gate-to-drain distance of 10 µm. The gate width is 2 × 50 µm. As shown in Figure 6.2(a), where I_{DS}-V_{DS} characteristics with the gate biased from 1.5 V to -6.5 V in steps of 1 V are shown, both types of HEMTs exhibit good I_{DS}-V_{DS} pinch-off and saturation characteristics. The maximum drain current density (I_{Dmax})

of the LAO-passivated HEMTs is about 21% higher relative to the unpassivated HEMTs, increasing from 570 to 690 mA/mm. This improvement of device performance corresponds well to the decease of sheet resistance of the substrate in the access region of the LAO passivated HEMT. Similarly, as seen from Figure 6.2(b), the peak extrinsic transconductance ($g_{m,max}$) also increases by 20% from 120 mS/mm for unpassivated device to 144 mS/mm for the HEMTs with LAO passivation. This demonstrates that a better gate control has been resulted from passivation of the surface states and the virtual gate effect could be mitigated by the LAO passivation. In addition, we observed a negative shift in the threshold voltage (V_{th}) of the LAO passivated HEMTs compared to the unpassivated devices from -3.3 to -3.7 V. This corresponds to the higher carrier concentration in the 2DEG channel originated from surface passivation, as shown from Hall data in Table 6.1.

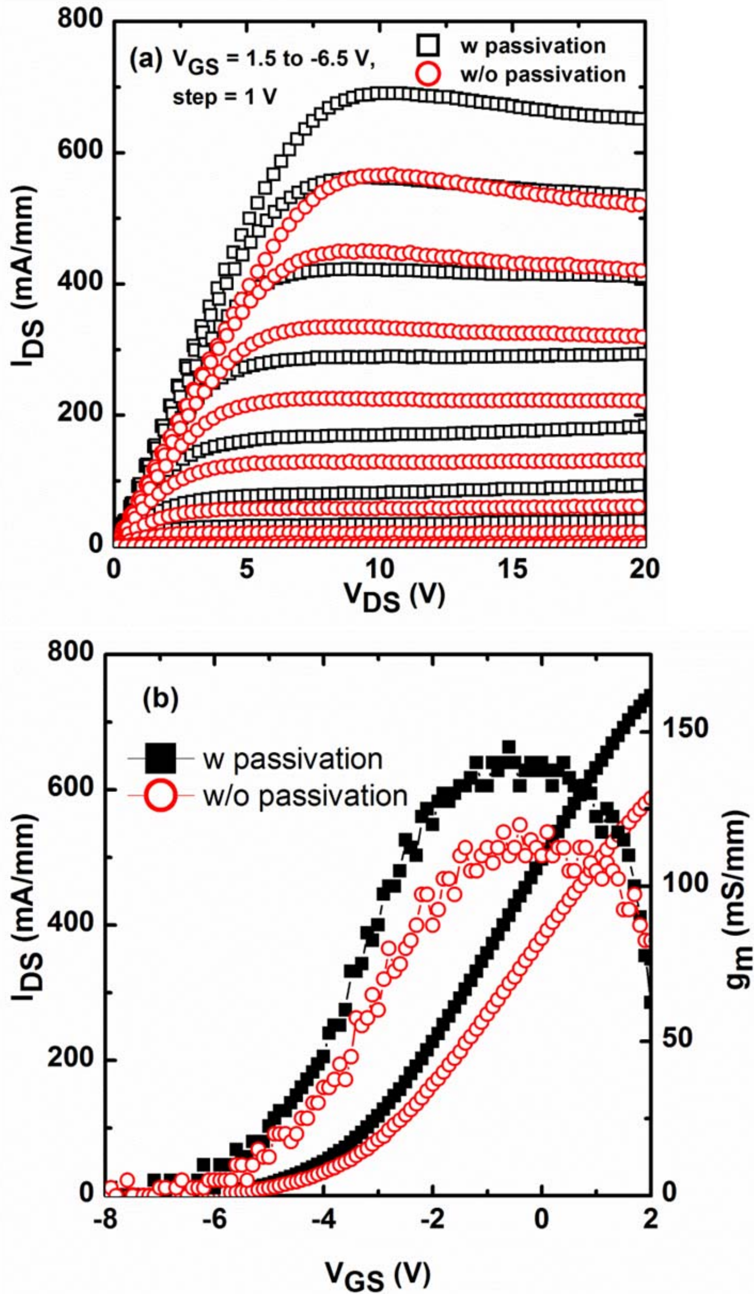


Figure 6.2 Measured DC I-V characteristics of InAlN/GaN HEMTs without passivation and with 25 nm passivation layer: (a) I_{DS}-V_{DS} curves and (b) I_{DS}-V_{GS} characteristics measured at V_{DS} = 10V. The device dimensions are $L_g/L_{gs}/L_{gd}/W_g$ = 2/2/10/2 × 50 μm.

To exame the current collapse under large drain bias, the devices were first biased at the off-state by applying a gate bias, V_{GS} = -15 V, at V_{DS} = 50 V for 100 s. Immediately after that, the devices were switched to the on-state by applying V_{GS} = 0 V and V_{DS} = -1 V to measure the I_{DS}-V_{DS} curves. Figure 6.3 shows the I_{DS}-V_{DS} results for both the passivated and unpassivated devices. For the unpassivated devices, current collapse is clearly seen after the voltage stress, as indicated by the decrease in the saturation current and the increase in the on-resitance, as shown in Figure 6.3(a). This could be caused by the trapping of electrons, from the reverse gate leakage under stress condition, by surface states in the proximity of gate region to form a virtul gate. This resultant virtual gate effect could cause the depletion of carriers in the 2DEG channel and thereby increase the parastic resistance. On the other hand, for the LAO passivated devices shown in Figure 6.3(b), the current collapse is suppressed significantly since no obvious changes are observed for the saturation current and on-resistance before and after voltage stress. This indicates that the virtual gate effect is greatly mitigated and the surface states can be effectively passivated by LAO. For instance, the change in the on-resistance (ΔR_{on}) for passivated devices is reduced to 0.5%, much lower than that for unpassivated devices of 28.5% at V_{GS} = 0 V, which means LAO could be a good passivation layer to improve the performance of InAlN/GaN HEMTs.

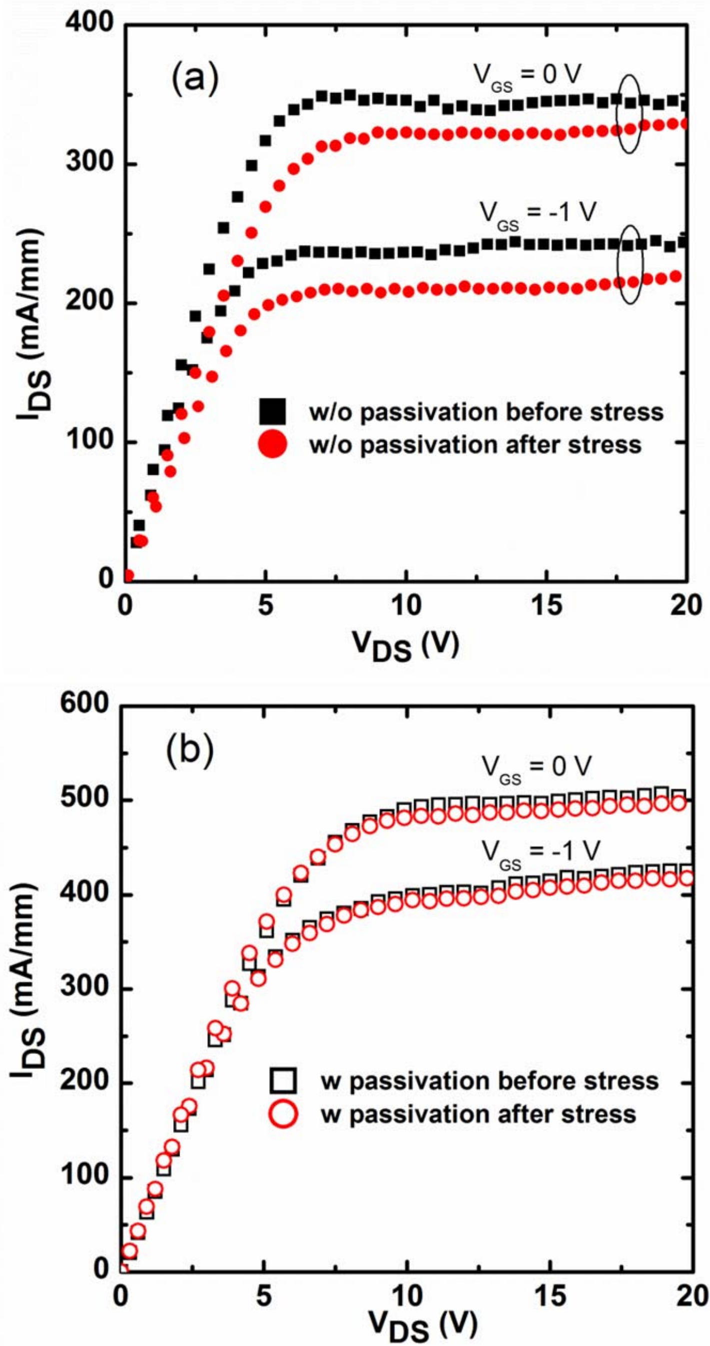


Figure 6.3 Measured I_{DS}-V_{DS} curves for (a) unpassivated and (b) passivated InAlN/GaN HEMTs before and after under voltage stress. The stress condictions are V_{GS} = -15 V and V_{DS} = 50 V for 100 s. The device dimensions are $L_g/L_{gs}/L_{gd}/W_g = 2/2/10/2 \times 50$ μm.

6.4 Summary

In this chapter, the effects of surface passivation on DC performance of InAlN/GaN HEMTs have been investigated using PLD LAO layer. Hall measurements have shown a 12 % improvement of sheet resistance of InAlN/GaN substrate with LAO passivation relative to the unpassivated InAlN/GaN. As for the gate leakage, no obvious difference was observed between unpassivated and passivated device, indicating LAO passivation did not weaken gate performance in InAlN/GaN HEMTs. Furthermore, an increase in I_{Dmax} (21%) an $g_{m,max}$ (20%) has been observed in the LAO-passivated InAlN/GaN HEMTs compared to the unpassivated, which implies the effective passivation for surface states from LAO passivation. Lastly, the suppressing of virtual gate effect in InAlN/GaN HEMTs has been demonstrated by LAO passivation after voltage stress.

Chapter 7

Summary and suggested future works

7.1 Summary

In the last decade, significant progress in InAlN/GaN HEMTs has been achieved. However, Au-free with low thermal budget ohmic contact schemes are still highly demanded to enable InAlN/GaN HEMTs device fabrication in silicon fab and hence lower the cost. The current work was thus motivated by the realization of the CMOS compatibility and improvement of device performance by reducing the access resistance for InAlN/GaN HEMTs. We looked into the investigation of gold-free low-thermal budget ohmic contacts and also passivation techniques.

7.1.1 Ti/Al and Hf-based ohmic contacts on n-GaN

We first studied the Ti/Al contacts with 2-step annealing and Hf/Al/Ni/Au contacts on n-GaN, which are the preliminary evaluation works for the fabrication of high performance GaN-based HEMTs. First, the feasibility of Ti/Al contacts on n-GaN processed by a two-step annealing was examined. The two-step annealing method was effective to achieve a good surface morphology but requires high annealing temperature (> 750 ^{o}C) to form low contact resistivity. It has been evident that the first-step annealing at 600 ^{o}C leads to the formation of stable $TiAl_3$ phases. The 30/120 nm Ti/Al contact on n-GaN shows the tradeoff between surface roughness and specific contact resistivity, with a minimum

contact resistivity of 4.87×10^{-6} $\Omega \cdot cm^2$ and a RMS roughness less than 10 nm obtained.

However, although the two-step annealing method shows a good tradeoff between surface roughness and contact resistivity, the thermal budget (~750 ^oC) is still not low enough to benefit device applications. Considering the lower workfunction of Hf (3.9 eV) than that of Ti (4.33 eV), and a higher enthalpy for Hf nitride formation (-369.03 kJ/mol) than that of TiN (-347.2 kJ/mol), Hf nitride is expected to be more thermodynamically favorable than TiN. Thus, Hf-based ohmic contact on n-GaN has been introduced and the comparison to traditional Ti/Al/Ni/Au contact was also carried out. It has been confirmed that Hf/Al/Ni/Au metallization can form ohmic on n-GaN with a low specific contact resistivity at 650 ^oC.

7.1.2 Hf/Al/Ta ohmic contact on InAlN/GaN heterostructures

Hf/Al/Ta contacts on InAlN/GaN were found to exhibit the lowest ohmic transition temperature of 550 ^oC compared to other transition metals (Ti, Ta, Zr, Nb, and V). A minimum contact resistivity of ~6.7×10^{-6} $\Omega \cdot cm^2$ and contact resistance of ~0.59 $\Omega \cdot mm$ are achieved for the optimized Hf/Al/Ta (15/200/20 nm) ohmic contact with annealing at 600 ^oC in vacuum. The mechanisms of ohmic contact formation and carrier transport of low temperature (600 ^oC) annealed Hf/Al/Ta on InAlN/GaN heterostructure have been investigated. The Hf/Al/Ta ohmic contacts have a smooth interface with InAlN/GaN, and the formations of HfN and Hf-Al alloy near the metal-semiconductor interface are critical to

achieving good ohmic contact. Thermionic field emission (TFE) is found to be the dominant carrier transport mechanism in the Hf/Al/Ta ohmic contacts on InAlN/GaN and analysis of the TFE model has revealed a high carrier density of 1.72×10^{19} cm^{-3} and an effective barrier height of 0.48 eV. The sheet resistance of the InAlN/GaN substrate is shown to increase with temperature by the power-law ($\propto T^{1.55}$). A series two-barrier model has been used to explain the carrier transport through the Hf/Al/Ta ohmic contacts on InAlN/GaN with a smooth metal-semiconductor interface. Furthermore, it has been shown that the Hf/Al/Ta contacts on InAlN/GaN are stable at 350 ^{o}C in air for more than 200 hours, indicating a good thermal stability for potential device applications.

7.1.3 Performance comparison between InAlN/GaN HEMTs with Hf/Al/Ta contacts and Ti/Al/Ni/Au contacts

A comparative study was conducted between InAN/GaN HEMTs with Hf/Al/Ta source/drain contacts and those with traditional Ti/Al/Ni/Au contacts in terms of TLM I-V results, contact surface morphology, metal-semiconductor interface, and device performance. The RMS roughness of the contact surface is found to be much smoother for Hf/Al/Ta based contacts compared to that for conventional Ti/Al/Ni/Au contacts. TEM images show a smooth metal-semiconductor interface for Hf/Al/Ta contacts, which is different from spikes formation for the 800 ^{o}C annealed Ti/Al/Ni/Au contacts. The InAlN/GaN HEMs with Hf/Al/Ta contacs shows a comparable DC performance to those InAlN/GaN HEMTs with Ti/Al/Ni/Au contacts. More importantly, the three-terminal off-state breakdown voltage of the device with Hf-based contacts is improved significantly by ~100 V

(~ 53.5 %) compared to those with Ti-Au based contacts. This enhancement is possibly due to the smooth meta-semiconductor interface in Hf/Al/Ta contacts, thus suppressing source-carrier-injection induced breakdown mechanism.

7.1.4 InAlN/GaN HEMTs with $LaAlO_3$ passivation

A preliminary study of $LaAlO_3$ (LAO) passivation has been examined in InAlN/GaN HEMTs with Hf/Al/Ta contacts. The sheet resistance of InAlN/GaN heterostructure can be reduced by 12% due to 25 nm LAO passivation. For the device performance, no obvious difference between unpassivated and passivated device implies that LAO layer did not degrade gate performance in InAlN/GaN HEMTs after passivation. Moreover, it indicates the effective passivation for surface states from LAO layer due to the fact that an increase of 21% in I_{Dmax} and 20% of $g_{m,max}$ have been obtained in the LAO-passivated InAlN/GaN HEMTs compared to the unpassivated.

7.2 Suggested Future works

7.2.1 Gate-first InAlN/GaN HEMTs with self-aligned source/drain

With the Au-free low-thermal budget Hf/Al/Ta contacts on InAlN/GaN developed in this thesis, it is natural to apply this contact scheme into the gate-first InAlN/GaN HEMTs with self-aligned source/drain. Due to the low thermal budget needed for Hf/Al/Ta contacts on InAlN/GaN, the Schottky gate or gate stack could be survive after the ohmic contacts annealing, which make it possible to realize the gate-first process. The gate-first process combined with the self-aligned source/drain contacts will further decrease the access resistance coming

from the semiconductor resistance in the access region between gate and source/drain. Therefore, with this approach aforementioned, the device performance could be improved dramatically in terms of high-power and high-frequency application for InAlN/GaN HEMTs.

7.2.2 Optimization of LAO passivation in InAlN/GaN HEMTs

As shown in Chapter 6, the LAO passivation is promising in terms of the preliminary results of InAlN/GaN HEMTs. Thus, a few futures works below could be carried out based the preliminary studies in Chapter 6.

(1) In the future, the optimization of LAO passivation technique is necessary, which could be carried out by varying a series of parameters including the layer thickness, post-deposition annealing and so on. Based on the optimized LAO passivation, gate-lag and drain-out lag output characteristics of InAlN/GaN HEMTs could be studied. Furthermore, the dynamic on-resistance (R_{on}) transients also could be investigated by time-dependent measurement [142]. Using this time-dependent measurement for R_{on} at different temperatures, the mechanism of LAO passivation could be studied quantitatively in terms of time constants and energy levels for the surface traps on InAlN/GaN.

(2) The effects of LAO passivation on the InAlN/GaN HEMTs frequency performance could be investigated also since the surface states have a significant influence on InAlN/GaN HEMTs especially for the high-frequency capability. For instance, small signal measurements could be performed before and after passivation to study the passivation effect on f_T and f_{MAX}. The passivation effect

on microwave noise performance could also be explored. Large signal measurements could be employed to study the effects of LAO passivation on output power and power-added efficiency.

(3) Recently, a simulation study by H. Hanawa proposed a way to improve the breakdown voltage by introducing a high-k passivation layer, which could smooth the electric field profiles between gate and drain in GaN HEMTs [143]. Therefore, it could be interesting to investigate the breakdown behavior of InAlN/GaN HEMT devices under high-*k* LAO passivation.

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