

**DEVELOPMENT OF
NANO/MICROELECTROMECHANICAL SYSTEM
(N/MEMS) SWITCHES**

QIAN YOU
(M.Sc., NUS)

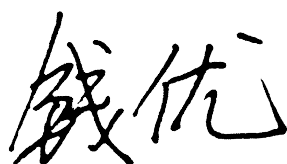
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DECLARATION

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.



Qian You

15 Jan 2015

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Summary

Power management is a daunting challenge for continuous MOSFET scaling-down due to leakage current issue. To avoid this power crisis, alternative switching devices have been proposed. Nano/Micro Electromechanical System (N/MEMS) switches have been attracting attention for their excellent switching properties such as zero-leakage current, abrupt switch behavior and potential to operate at high temperature. These unique properties make the N/MEMS switches a strong candidate for ultra-low power electronics and harsh environment integrated circuits. This thesis begins with a general overview of the existing N/MEMS switches prototypes and several proposed applications. It then presents the design considerations of N/MEMS switches in various aspects.

This work concentrates on further miniaturizing the size of the devices and clarifying the main issues on the successful implementation of N/MEMS switch technology. The state-of-the-art research shows two major constraints: very high actuation voltage and very limited process successful rate. Notable improvement works need to be done to address these issues including investigation of new device structures, development of advanced fabrication process and implementation of new materials. It is remarkably challenging when the mechanical switches have been reducing their dimensions from MEMS to NEMS (MEMS with sub-micrometer features).

To address the high actuation voltage issue of N/MEMS switches, U-shaped Si nanowire based NEMS switch has been developed. With the help of

Summary

U-shaped structure and ultra-small Si nanowire, the actuation voltage of the NEMS switch has been reduced from conventionally more than 5V to only 1V.

Prior demonstrations of NEMS switches normally demonstrate the operation of a single switching element which was mostly fabricated by a process with very low success rate. Therefore, extensive studies of NEMS switches design and properties associated with fabrication issues are difficult to be carried out. To address this problem, an all-metal-based NEMS switch has been developed in a systematical approach to fulfill a few technical requirements at the same time, mainly targeting on reliable fabrication process with high yield throughput. Molybdenum, as a new material for NEMS switches, has been used as the structural layer. The devices are fabricated with low temperature CMOS compatible process with a single mask layer. The electrical measurement shows sound high temperature operation characteristics with good reliability, e.g., survived after 28 hours continuous cycling testing at 300 °C environments. The devices also show low contact resistance of 2.5 k Ω and an on/off ratio as high as 10^8 . The basic design rules to obtain high process output are determined. With optimized dimensions, the achieved process yield is as high as 100 %.

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List of Acronyms

Al	Aluminum
Al ₂ O ₃	Aluminum Oxide
ALD	Atomic Layer Deposition
AlN	Aluminum Nitride
Ar	Argon
BEOL	Back-End-Of-Line
BOX	Buried-Oxide
CMOS	Complementary Metal–Oxide–Semiconductor
CMP	Chemical Mechanical Polishing
CNT	Carbon Nanotube
CPD	Critical Point Dryer
DHF	Dilute Hydrochloric Acid
DI water	Deionized Water
DRIE	Deep Reactive Ion Etching
EBL	Electron-Beam Lithography

FEM	Finite Element Method
FPGA	Field-Programmable Gate Array
HDP CVD	High-Density Plasma Chemical Vapor Deposition
HF	Hydrofluoric Acid
IC	Integrated Circuit
LPCVD	Low-Pressure Chemical Vapor Deposition
Mo	Molybdenum
MOCVD	Metal-Organic Chemical Vapour Deposition
MOSFET	Metal–Oxide–Semiconductor Field-Effect Transistor
N/MEMS	Nano / Micro -Electro-Mechanical System
NEMS	Nano -Electro-Mechanical System
NVM	Non-Volatized Memory
PECVD	Plasma-Enhanced Chemical Vapor Deposition
poly-Si _{0.4} Ge _{0.6}	Polycrystalline Silicon-Germanium
Pt	Platinum
PVD	Physical Vapor Deposition
PZT	Lead Zirconate Titanate

List of Acronyms

RTA	Rapid Thermal Annealing
Ru	Ruthenium
SEM	Scanning Electron Microscope
Si	Silicon
Si ₃ N ₄	Silicon Nitride
SiC	Silicon Carbide
SiNW	Silicon Nanowire
SiO ₂	Silicon Dioxide
SOI	Silicon-On-Insulator
SRAM	Static Random-Access Memory
TaN	Tantalum nitride
TiN	Titanium Nitride
TiO ₂	Titanium Dioxide
UV	Ultraviolet
VHF	Vapor Phase Hydrofluoric Acid
W	Tungsten
ZnO	Zinc Oxide

List of Symbols

A	Actuation area
a_c	Coefficient for pull-in voltage of cantilever
a_{ff}	Coefficient for pull-in voltage of fixed-fixed beam
C	Capacitance
E	Young's modulus
f	Natural frequency of the beam
g	Initial gap
g_{DB}	Gap between beam to drain terminal
g_{GB}	Gap between beam to gate terminal
I_{ds}	Drain to source current
I_{off}	Off-state leakage current
k	Spring constant
k_B	Boltzmann's constant
k_{eff}	Effective spring constant of the beam

List of Symbols

L_B	Beam length.
L_D	Drain terminal width
L_{DG}	Distant between drain terminal and gate terminal
L_G	Gate terminal width
m	Mass of the beam
q	The magnitude of the electrical charge on the electron
S	Subthreshold slope
T	Temperature
t	Width of the beam
U	Dimensional scaling factor
V	Voltage
V_{dd}	Supply voltage
V_{GS}	Gate to source voltage
V_{pi}	Pull-in voltage
V_t	Threshold voltage
w	Out-of plane thickness of the beam
z	The movable structure with displacement

z_{pi}	Maximum stable displacement
ε_0	Permittivity of the vacuum

Chapter 1 Introduction of N/MEMS Switches

1.1 Power-Efficiency Limitation of CMOS

Since the invention of complementary metal–oxide–semiconductor (CMOS), the integrated circuit (IC) based on CMOS technology virtually dominates every aspect of computation and communication. Two key advantages that have driven the ICs to the success from day one are low-cost and high-performance. As all the components of the ICs are projected on silicon (Si) wafers by photolithography rather than being assembled discretely, the cost of the ICs is essentially reduced with a smaller footprint. The aggressive dimension scale-down allows ICs, consisting of billions of transistors, to be produced cost-effectively.

The better performance of IC is attributed to the faster switch, less power consumption and more functionality of the transistors. As a result, the major motivation for the semiconductor industry is to keep scaling down the dimension and climbing the performance. Traditionally, dimensional scaling has been sufficient to deliver these aforementioned performance merits, but it reaches its bottleneck over the past few years. For metal–oxide–semiconductor field-effect transistor (MOSFET), the drain to source current (I_{ds}) will never be zero, instead it decreases exponentially at a rate of subthreshold slope S . In the best case, I_{ds} will decrease by a factor of 10 for every 60mV below the threshold voltage (V_t). The subthreshold slope is restricted by the fundamental

limit of thermal voltage, $k_B T/q$, where k_B is Boltzmann's constant, T is the temperature, q is the magnitude of the electrical charge on the electron. As the supply voltage (V_{dd}) and threshold voltage keep scaling down with the dimensions, there is less headroom below the threshold voltage. Consequently, the subthreshold leakage current increases exponentially with decreasing threshold voltage. The off-state leakage current (I_{off}) between the drain and the source increases dramatically, which can be estimated as[1].:

$$I_{off} \propto 10^{-V_t/S}$$

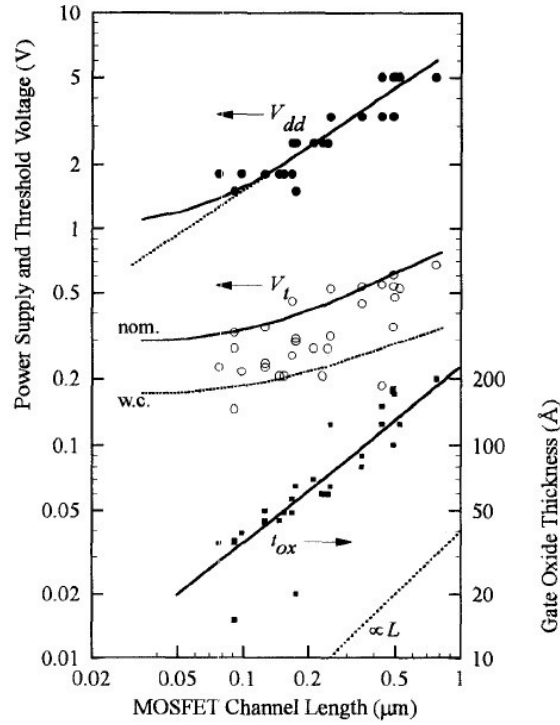


Figure 1-1 Trends of power supply voltage V_{dd} , threshold voltage V_t , and gate oxide thickness t_{ox} versus channel length for CMOS logic technologies. Adapted from [2]

The threshold voltage scaling-down has significantly slowed down below 0.3V to maintain a low off-state leakage current [3]. Meanwhile, the scaling-down of supply voltage (V_{dd}) has also slowed down, as the value of gate to source voltage V_{GS} should be maintained to achieve certain overdrive voltage

$|V_{GS} - V_T|$ (for high performance) as shown in Figure 1-1. Therefore, the active power consumption ($\propto V_{dd}^2$) and static power consumption ($\propto I_{off} \times V_{dd}$) become difficult to be controlled simultaneously. Furthermore, the gate to channel leakage current caused by direct tunneling through the gate oxide also worsens the problem [4].

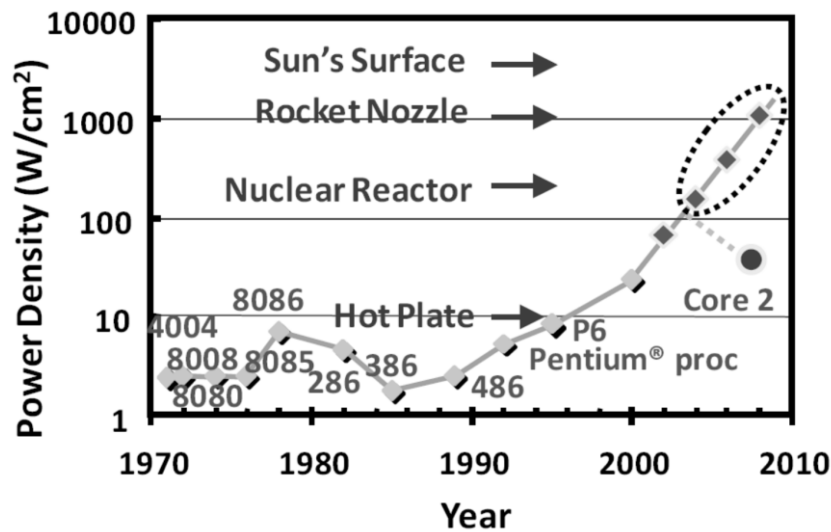


Figure 1-2 Power density versus minimum feature size as reported in [5].

From Figure 1-2, the power density of the microprocessors reached the dangerous territory of $10\text{W}/\text{cm}^2$ even before the release of Intel P6, higher than that of a hot plate. It was predicted to get worse for smaller critical dimensions. The traditional approach of simply scaling down the dimensions must be altered. To avoid the unreasonably high power density, the industry went from high speed single-core processors to slower multi-core processors working in parallel. However, parallelism is still only a temporary fix, the power consumption cannot be reduced indefinitely. To continually constrain the power density within a reasonable value, subthreshold leakage current needs to be eliminated.

1.2 The Call of New Applications

Continuous dimensional scaling-down explores a brand new field for diverse applications of computational devices. Portable and autonomous electronics have created an unexpected market in the recent years. Many researches are focusing on increased functionality of mobile devices, to make them the ultimate customer interface to the world [6].

Computational devices with limited power consumption and power resources can be embedded in almost every field. Such systems can be used to collect information with various sensor nodes, ranging from environmental monitoring [7, 8], building management [9], industrial application [10] to personal health care system[11-13] and home automation[14]. In these applications, the devices typically rely on a finite energy source like a battery or very limited power supply, such as energy harvester [15]. With limited progress in battery technology, the development of these technologies is greatly constrained. On the other hand, unlike pure computational devices, these sensor nodes or mobile devices will stay in a hibernating state for most of the time. Thus, technology which can eliminate the off-state power consumption will be favorable.

1.3 Mechanical Switches

Despite of some potential optimization that can extend the life of CMOS technology, the fundamental obstacle of subthreshold slope still underlies. Alternatives have been demonstrated with subthreshold slopes below 60 mV/dec, such as: ferroelectric FETs [16], tunneling FETs [17], and impact

ionization FET[18]. In this thesis, we will focus on electromechanical devices which show most unique electrical properties.

Micro/Nano-Electro-Mechanical system (N/MEMS) switches are devices which employ mechanical force to actuate a movable structure (in most cases, beam) to make a conductive path between two electrodes as shown in Figure 1-3(a). By removing the controlling mechanical force, the mechanical spring forces will pull back the conductive path, leaving the beam suspended. Due to the nature of their operational principle, N/MEMS switches define the off state by a physical air gap. The on state of the N/MEMS switches is established only when the contact is physically closed. Thus, the N/MEMS switches feature two fundamental properties which are unavailable in MOSFETs: zero off-state current and abrupt switching. A typical I-V curve can be found in Figure 1-3 (b). Moreover, zero off-state current means zero standby power dissipation and abrupt switching behavior suggest the potential of freely reduce the turn-on voltage.

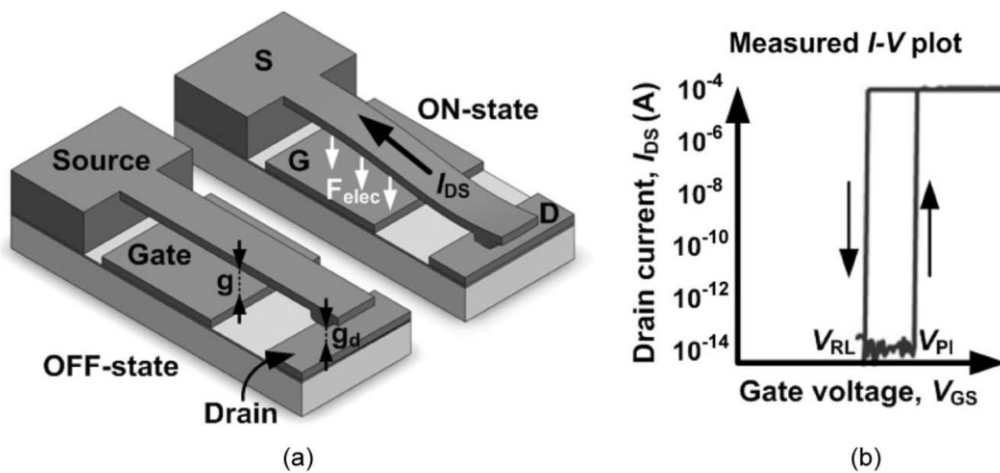


Figure 1-3 (a) Basic electrostatically actuated mechanical switch. (b) Measured current versus gate voltage characteristics for a mechanical switch. Adapted from [19].

Introduction of N/MEMS switches

Since N/MEMS switches can be fabricated at relatively low process temperature, and these switches do not have to be built with single crystalline semiconductor materials such as silicon (Si), they can be placed on top of CMOS routing layers using a back-end-of-line (BEOL) compatible process, which will reduce the chip footprint. Furthermore, alternative substrates such as glass or plastic can be used, which would significantly reduce the cost.

As N/MEMS switches can be fabricated directly above the CMOS wafer, possible applications for hybrid N/MEMS-CMOS technology include power gating [20-26], static random-access memory (SRAM) [27-29], field-programmable gate array (FPGA) [30-32]. The hysteresis property of the switches also makes them suitable for non-volatile memory (NVM) application [1.17]. Another advantage switches have over CMOS is robustness against temperature variations and radiation hardness, which is attractive, especially for industrial, military and space applications [33, 34].

Many issues still remain to be solved in order to apply N/MEMS switches in logic applications, among which the most critical one is contact reliability, since logic circuits would require the switches to operate over 10^{16} hot switching cycles. Since mechanical touches need to be established for every turn-on cycle, high velocity impact of the movable beam and the fixed electrode as well as the resultant “tip bouncing” can quickly degrade the contact [35, 36].

Another significant issue for N/MEMS switches is the presence of surface adhesion force (Van der Waals force) [37, 38]. The prototypes developed so far are generally large for realistic applications. With the devices scaling down,

permanent stiction might happen if the elastic restoring force is not sufficiently high. In order to minimize stiction and maintain clean contact spots, hermetically encapsulation [39, 40] process for N/MEMS switches should be developed.

1.4 Actuation Mechanism

In this section, various actuation mechanisms used in N/MEMS switches are classified into four major groups: electrostatic, piezoelectric, electrothermal, and electromagnetic actuation. These actuation mechanisms are commonly used in other MEMS devices with their own unique strength and weakness. In the following section, we will analyze these mechanisms by focusing on their power consumption and integration feasibility.

1.4.1 Electrostatic Actuation

In electrostatic actuation, a typical configuration consists of a movable electrode connected to suspending mechanical springs, while a fixed electrode is anchored onto the substrate. When a voltage difference is applied between the electrodes, the electrostatic attractive force accelerates the movable electrode to the stationary electrode. Meanwhile, the spring suspending the movable electrode is deformed.

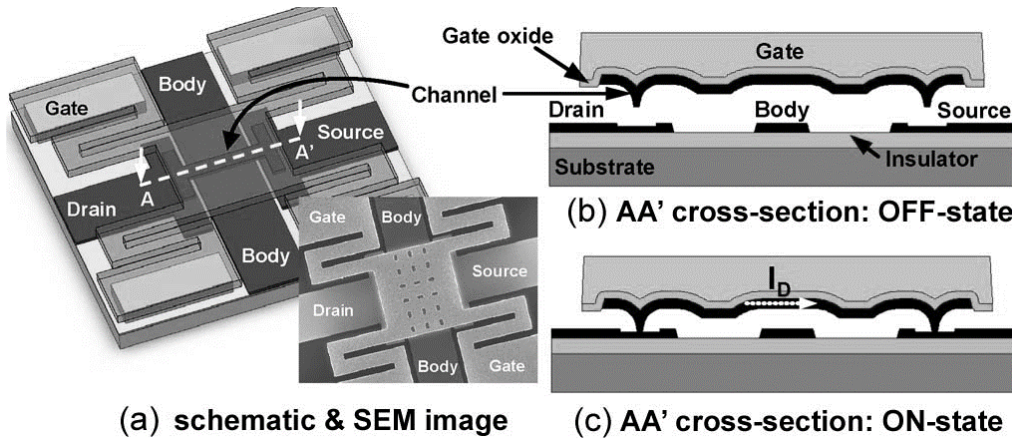


Figure 1-4 Schematic illustrations of an electrostatic actuated switch. (a) Isometric view. (b) Cross sectional view along the channel (AA') in the off-state. (c) Cross-sectional view in the on-state. In the off state, an air gap separates the channel from the metallic source and drain electrodes so that no current can flow. In the on state, electrostatic force between the gate and the body electrode causes the gate to be deflected downward sufficiently to bring the channel into contact with the source and drain electrodes, to form a conductive path for current to flow. Adapted from [41]

The electrostatic actuation gains most of the focus in the community. In principle, utilization of electrostatic actuation tolerates a wide variety of materials because it only requires conductors to be separated by a non-conductive gap. It is relatively easy to manufacture by using conventional process and material. Unlike electrothermal or electromagnetic actuation, it does not consume much active power as charging a capacitor is the only operation needed to turn on the devices [42, 43]. No continuous current path exists on the actuation side. The switching speed is relatively higher with only 10 to 100 ns delay [44, 45], while the electromagnetic and electrothermal switches usually have more 1 ms delay. One major constraint for electrostatic actuation is its high actuation voltage, and early demonstrations typically require around 50V supply voltage [46-48]. Fortunately, the actuation voltage scales down quickly with the dimension. Although most of the recent study

still requires a supply voltage of more than 5 V [49-55], a few approaches have been proposed to match the supply voltage with CMOS [41, 56, 57].

1.4.2 Piezoelectric Actuation

Piezoelectric effect is understood as the linear electromechanical interaction between mechanical and electrical state in crystalline materials. An applied voltage across the electrodes of a piezoelectric material will result in a net strain that is proportional to the magnitude of the electric field. Typical piezoelectric materials for MEMS application include lead zirconate titanate (PZT), aluminum nitride (AlN) and zinc oxide (ZnO).

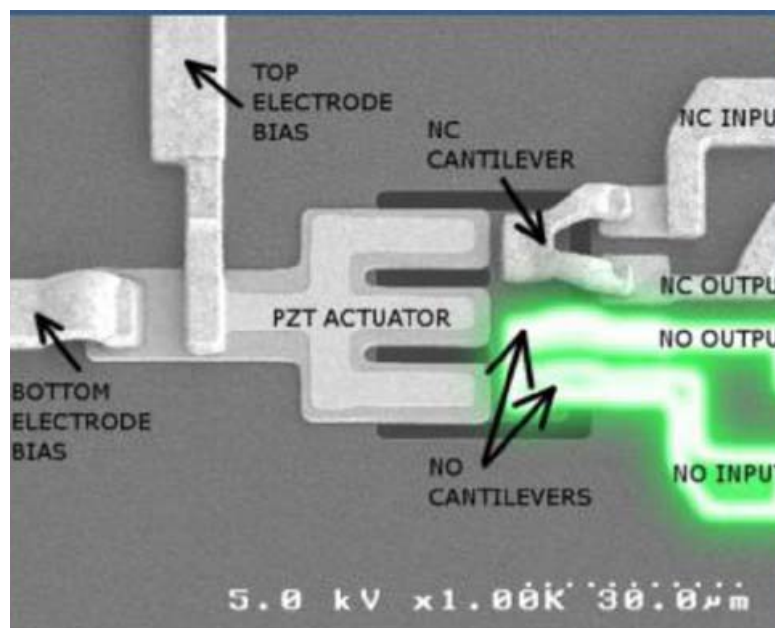


Figure 1-5 A PZT based MEMS switch. The switch utilizes the converse piezoelectric effect to generate movement. Two electrodes on the left (Top and bottom) provide the necessary electric field to bending down the contact. Output current flow is highlighted in green where the physical contact is formed. Adapted from [58, 59]

Piezoelectric switches provide strong actuation force and large deflection [60, 61]. The actuation voltage can be controlled within 1 V [62-70]. The major hurdle for piezoelectric actuation is the material development. PZT is

considered as the traditional piezoelectric material for MEMS, but the fabrication process is not CMOS compatible. Recent progress on AlN actuator makes the piezoelectric actuation mechanism an attractive alternation, but process development of a scaled device remains to be explored.

1.4.3 Electrothermal Actuation

Electrothermal actuators use stacked layer of materials with different thermal expansion coefficients, or a single material with specific geometry (Figure 1-6) [42]. Two actuators have been fabricated the switch will buckle when heated and go back to original state when power is turned off.

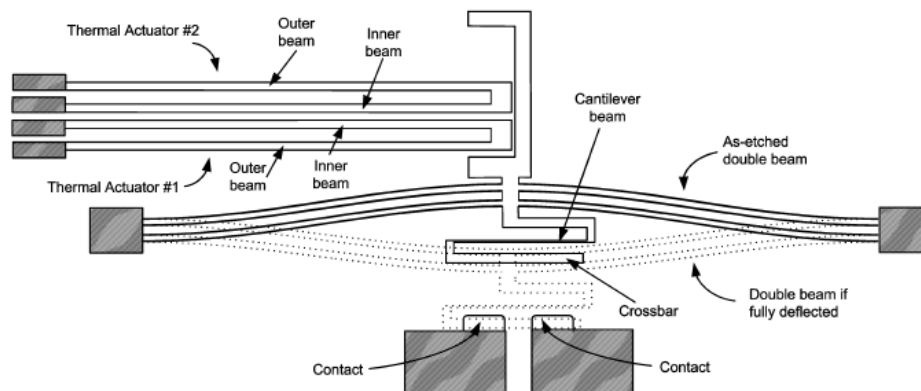


Figure 1-6 SEM image of a fully fabricated single-pole single-throw electromagnetic MEMS switch. When current applied to the coils, the magnetic force generated by the stationary permalloy overcomes the return spring force and closes the switch. Adapted from [71]

A few advantages are shown by using electrothermal actuation, including large displacement, high contact force (which provides low contact resistance), and relatively simple fabrication process. However, unlike electrostatic or piezoelectric actuators, electrothermal actuators consume a larger amount of active power as a constant temperature needs to be maintained for deformation.

In this sense, the electrothermal actuation has a fundamental contradiction with N/MEMS switch technology.

1.4.4 Electromagnetic Actuation

Reported electromagnetic switches are normally based on the deflection of NiFe permalloy cantilever which is actuated by coils [72-80]. Figure 1-7 shows an electromagnetic switch, where the permalloy serves as a movable structure and is connected to the gold contact.

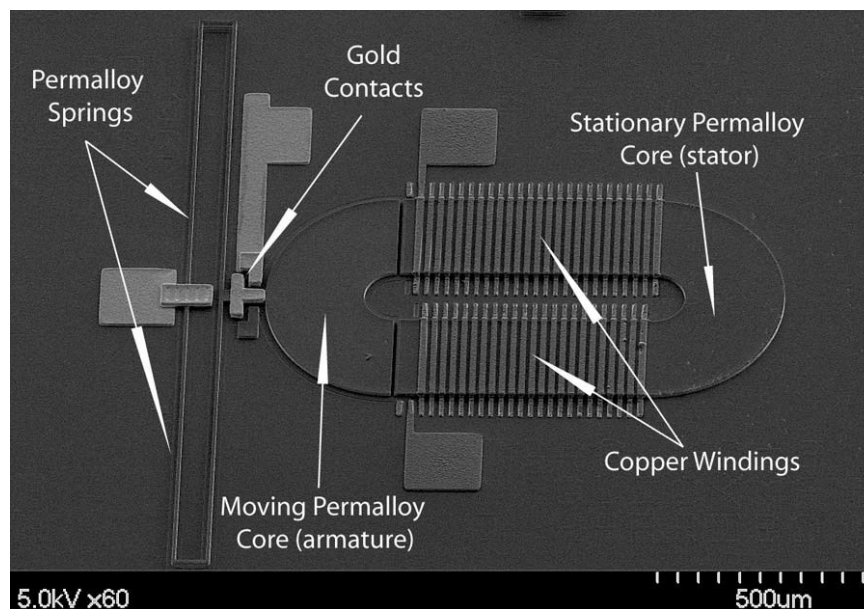


Figure 1-7 SEM image of a fully fabricated single-pole single-throw electromagnetic MEMS switch. When current applied to the coils, the magnetic force overcomes the return spring force and closes the switch. Adapted from [79]

The electromagnetic switches have some excellent performance including low operating voltage, low contact resistance and good endurance. But these devices are too large and slow to be used in ICs. Furthermore, the performance does not appear to be energy-efficient, and processing of ferroelectric materials is not compatible with CMOS technology.

1.4.5 Comparison of Different Actuation Mechanisms

Table 1-1 summarized the above mentioned four different actuation mechanisms. Electrostatic actuation would be the most suitable solution for N/MEMS switches. Considering the difficulty in process development and the cost of fabrication, any device targeting to replace MOSFET should be developed based on current CMOS process. Unlike piezoelectric and electromagnetic actuation, electrostatic actuation does not have specific requirement for material and can be easily fitted in the CMOS compatible process.

Table 1-1 Comparison of four actuation mechanisms

	Electrostatic	Piezoelectric	Electrothermal	Electromagnetic
Power Consumption	Low	Low	Very High (>1 mW)	High(> 1 mW)
Fabrication	Easy	Medium	Easy	Difficult
Speed	Fast (~10 ns)	Fast (~10 ns)	Slow (> 1ms)	Slow (> 1ms)
Scalable	Good	Medium	Medium	Poor

Moreover, the simple fabrication process and structure design ensure the dimension can be scaled down easily. In the meantime, the major drawback, i.e., high actuation voltage, can be reduced by using smaller device dimension. The power consumption of the electrostatic N/MEMS switches only comes from charging the capacitor, which can be considered as very limited.

On the other hand, electrothermal actuation and electromagnetic actuation have their fundamental limitation in mechanical switch application. Electrothermal actuation requires a continued power supply, which contradicts

the merits of mechanical switches. Electromagnetic actuation needs CMOS incompatible materials as well as tedious process for the coil.

As a result, most of the studies focus on electrostatic actuation. In the next section, recent studies on electrostatic actuated N/MEMS switch prototypes will be reviewed.

1.5 Recent Prototypes of N/MEMS Switches

In this section, various prototypes of N/MEMS switches are summarized, mainly focused on the process integration, electrical performance and reliability.

1.5.1 Folded- Flexure Beams Switches

Figure 1-8 shows the schematic view of the folded-flexure beams MEMS switches. The work is done by a joint research effort from UC Berkeley, MIT and UCLA [21, 81-110]. The switch is comprised of a movable plate (source) with four folded supporting beams at each corner. The folded-flexure beams are further extended to the anchor on the substrate. The gate and drain terminals are buried beneath the moveable plate with an air gap in between. When the gate-to-source voltage is sufficient to pull down the plate, physical contact will be established between source and drain, and then electrical signal will pass from the left side drain terminal across the movable source to the right side drain terminal.

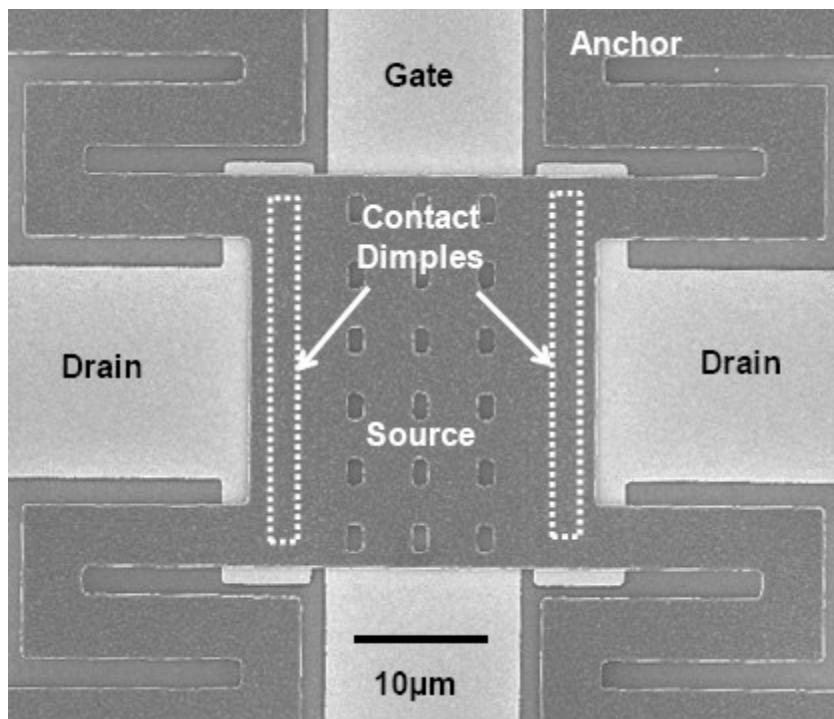


Figure 1-8 Top view a Folded-beam Switch, adapted from [99]

A four mask process is developed for the electrostatically actuated switches as shown in Figure 1-9. The process starts with atomic layer deposition (ALD) of 80nm aluminum oxide (Al_2O_3) at 300°C as bottom insulation. 50 nm tungsten (W) deposited by magnetron sputtering is used as bottom electrodes (gate and drain). Then silicon dioxide (SiO_2) deposited by low-pressure chemical vapor deposition (LPCVD) at 400°C works as the sacrificial material. Two layers of W and Al_2O_3 are then deposited and patterned as top electrode (source). *In-situ* boron-doped polycrystalline silicon-germanium (poly- $\text{Si}_{0.4}\text{Ge}_{0.6}$) deposited at 410°C by LPCVD is used as structural material. The low temperature LPCVD process is developed for post-CMOS integration. The thick poly- $\text{Si}_{0.4}\text{Ge}_{0.6}$ mainly serves as supporting layer for the W and Al_2O_3 . Lastly, an ultra-thin (3Å thick) coating of titanium dioxide (TiO_2) is deposited at 300°C by ALD after the device is released by vapor phase

hydrofluoric acid (VHF). The process temperature is controlled under 410 °C, all the materials used are CMOS compatible.

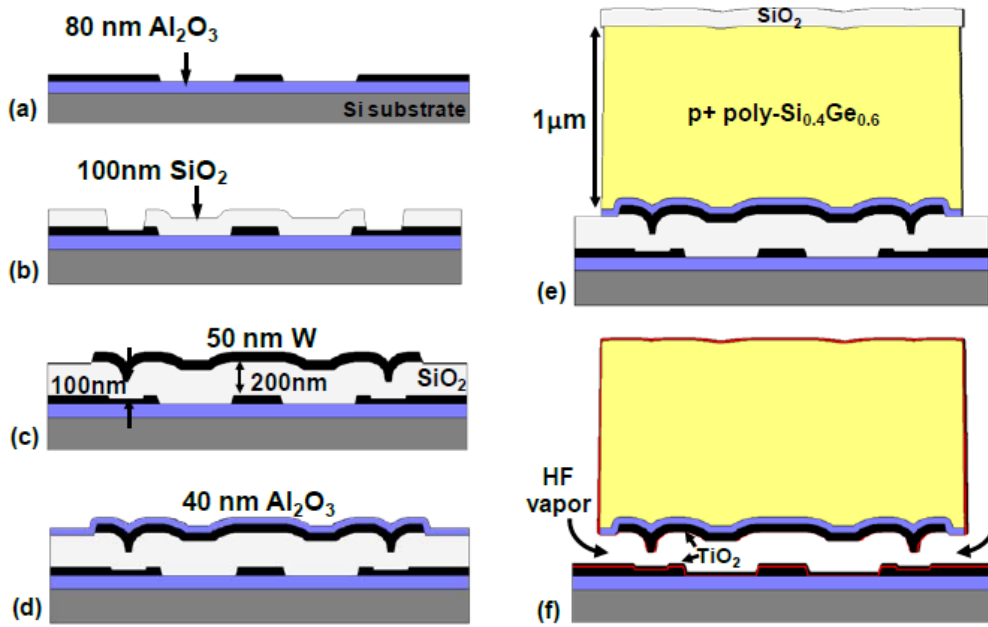


Figure 1-9 Process flow of the folded-flexure switch, adapted from [99]

Although the device occupies quite a large area, it shows very good electrical performance. Figure 1-10 shows the switch has an $S < 0.1 \text{ mV/dec}$ abrupt turn on behavior at 6.12V. The contact resistance is stabilized at 1~10 k Ω . Longer endurance measurement of 1.25 billion on/off cycles in N₂ ambient without stiction or failure is also demonstrated.

Device functionality is verified under a temperature range of 30° C -200°C. Radiation hardness of the devices is also achieved with alpha particles of various doses (200K rad, 2M rad, 20M rad). It is found that only switches exposed to 20M rad shows 10% jump in turn on voltage. Lower doses cause a negligible shift [99]. The typical amount of radiation encountered in space due to cosmic radiation is 50-100 rad/year. In the maximum intensity zone of inner

Van Allen belt, radiation can reach as high as 500k rad/year [111], under which it would still take 40 years to reach a level of 20M rad. Therefore, radiation is not expected to be a concern.

The 1 μm poly-Si_{0.4}Ge_{0.6} deposition is vital to the success of the whole process. A thick, low stress structure material eliminates the deformation of the switches induced by the thin, high stress material below. TiO₂ coating is also very important as it greatly raises the endurance of the switches from a few cycles to hundreds of billions of cycles [102].

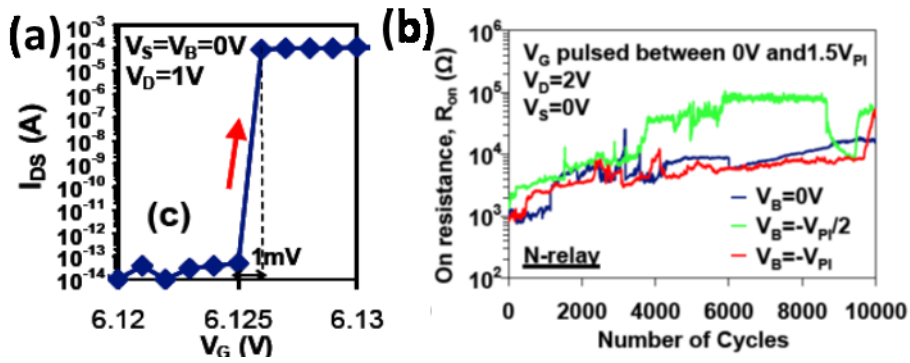


Figure 1-10 (a) I-V curve of switch turn on. (b) On-state resistance with cycling for different applied body bias, adapted from [41]

1.5.2 Platinum Coated Polysilicon Switches

Laterally actuated switch is an attractive solution because it allows the fixed electrodes to be patterned with the movable structure at the same time. Unlike the above mentioned vertically actuated switches, the contact surface for laterally actuated switches is on the sidewall. Thus, unless the whole structural material is metal, the movable beam needs proper coating for the contact.

A team from Stanford University developed laterally actuated, platinum-coated polysilicon switches [54, 112-115]. A 2 μm SiO_2 is first deposited by LPCVD at 400 $^\circ\text{C}$, which serves as both the sacrificial and the insulation layer. A 1.2- μm -thick *In-situ* doped polysilicon layer is then deposited by LPCVD at 580 $^\circ\text{C}$ and subsequently annealed at 1075 $^\circ\text{C}$ for 30s. A 300-nm oxide hard mask is used to pattern the polysilicon. The minimum gap is 600 nm. To coat the polysilicon sidewall with platinum (Pt), a 50 nm-thick Pt layer is sputtered followed by anisotropic etching to remove the Pt film from the bottom and top surfaces as shown in Figure 1-11 (a). The polysilicon structure is released by 49% hydrofluoric acid (HF) and critical point dryer (CPD) as shown in Figure 1-11(b).

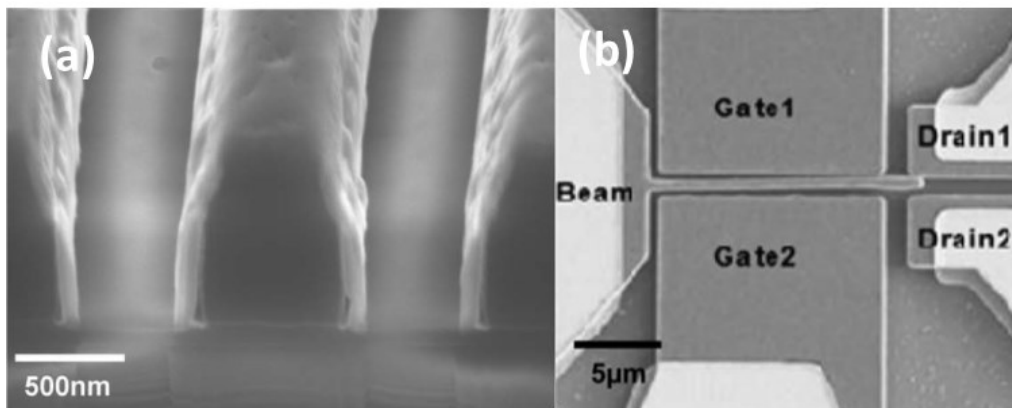


Figure 1-11 (a) SEM cross section of non-released platinum-coated beams. (b) SEM images showing actuation of a five terminal polysilicon switch coated with platinum. Adapted from [112]

The device shows abrupt turn-on and turn-off behavior at 8 V and 5 V, respectively. However, the study only includes single device demonstration, the yield of the switches is not mentioned. The fabrication process needs high temperature deposition as well as very high temperature annealing, which makes it unsuitable for post-CMOS integration.

1.5.3 Laterally Actuated Ruthenium Switches

Pure metal structural layers usually suffer from high strain and stress, but the deposition can be done at low temperature, which enables post-CMOS switch integration. Czaplewski et al [116, 117] demonstrated a laterally actuated switch using ruthenium (Ru) as both the contacting and structural layer.

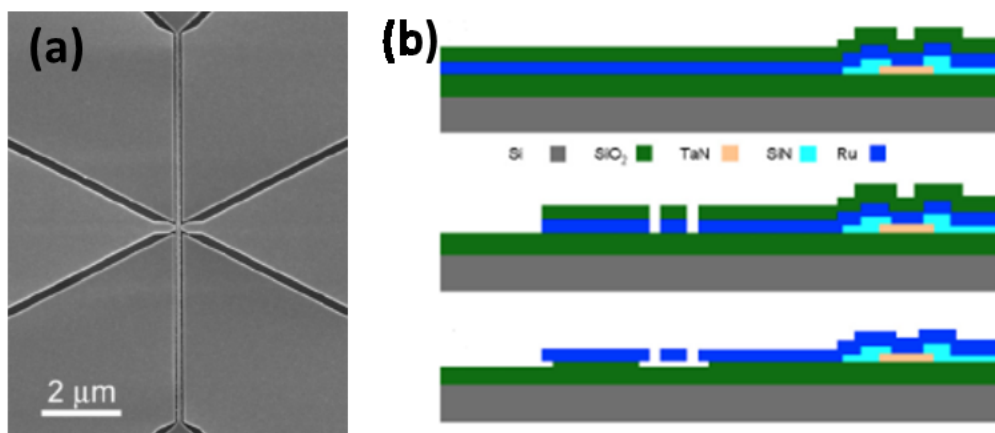


Figure 1-12 Laterally actuated ruthenium switches (a) SEM photo (b) process flow. Adapted from [116]

The switches are fabricated as follows (Figure 1-12 (a)). A 500 nm thick SiO₂ is thermally grown on silicon wafers as isolation dielectric and sacrificial layer. Tantalum nitride (TaN) interconnect is then sputtered and patterned as on-chip resistor. 100 nm Silicon nitride (Si₃N₄) is subsequently deposited for isolation, where via is also patterned and etched. Next, a 200 nm thick Ru and a 100 nm thick SiO₂ hard mask are deposited. The Ru-layer is subsequently patterned and etched with the SiO₂ hard mask. The smallest features of the switch, the actuation gaps (20-70 nm) and beam width (50-100 nm), are patterned using electron-beam lithography (EBL). Finally, the switches are

released by wet etching (1:3 HF: deionized (DI) water) for 1 minute, followed by rinsing in DI water and blown dry with N_2 .

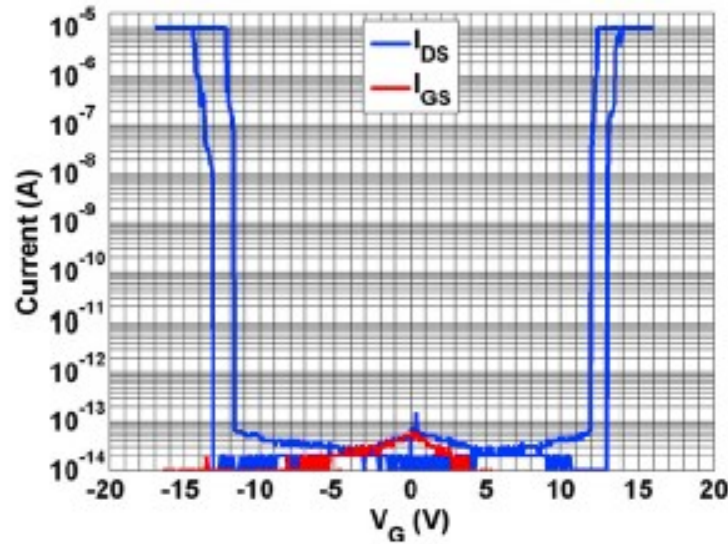


Figure 1-13 I-V curve of laterally actuated Ru switches, adapted from [116]

One of the fabricated switches with a beam length of 5 μm , beam thickness of 100 nm and gap width of 50 nm is measured for electrical properties as shown in Figure 1-13. The turn-on voltage is 13 V. However, the process yield is low, as only 12 switches are tested to be functional among 800 fabricated devices.

1.5.4 TiN Based Vertically Actuated Switches

Another example of pure metallic switches using titanium nitride (TiN) as structural and contact material is reported in [118-120]. The cantilever-type NEMS switches with 40-nm-thick suspension air gap and 50-nm-thick TiN are designed and fabricated. The bottom electrodes are fabricated with physical vapor deposition (PVD) of TiN on a Si_3N_4 insulation layer. The sacrificial SiO_2 layer is deposited by plasma-enhanced chemical vapor deposition

(PECVD) with a 40 nm actuation-gap from the gate and a 20 nm dimple gap from the drain. The movable top electrode is formed with 10 nm thick PVD TiN and an additional 40 nm thick metal-organic chemical vapor deposition (MOCVD) TiN layer. The length and width of the beams range from 700 nm to 900 nm and 200 nm to 400 nm, respectively. The devices are finally released by a wet process, followed by a CPD step as shown in Figure 1-14.

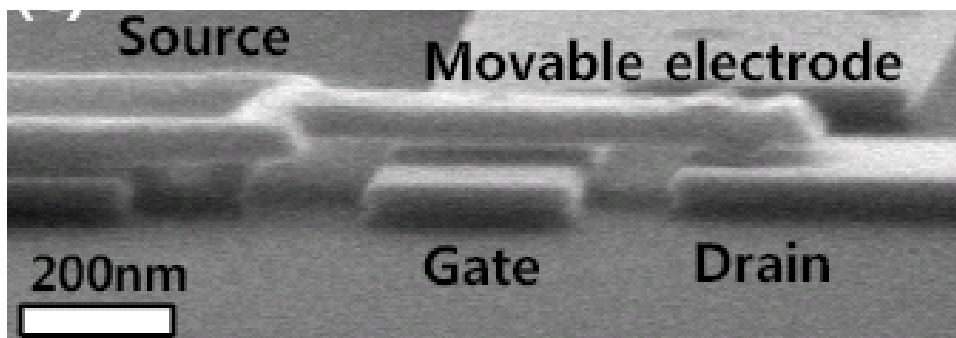


Figure 1-14 An SEM image of TiN Switch, adapted from [118]

Figure 1-15 shows the drain current versus gate voltage characteristics for a switch with cantilever length of 700 nm. The devices show only few dozen on/off cycles and contact resistance close to 1 G Ω , and thus further investigation needs to be done to improve the metal-to-metal contact.

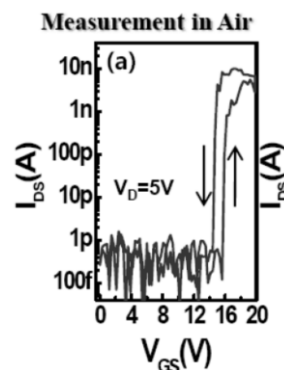


Figure 1-15 Measured I-V curve for TiN devices, adapted from [118]

1.5.5 Comparison of the Four Prototypes

Among the above mentioned four prototypes, the folded-flexure beams switches are proven to be the most reliable ones, with well controlled process temperature, lower turn-on voltage, good endurance and very high process yield. With the device dimension scaling down, the following three prototypes face their own problem. The platinum coated polysilicon switches require process temperature as high as 1075 °C. The laterally actuated ruthenium switches show very limited process yield. The TiN based switches have very high contact resistance which should not be observed with metallic contact surface. The turn-on voltage of the later three devices is also larger. Thus, more work should be done to achieve low temperature process integration, low pull-in voltage, low contact resistance and high process yield with scaled N/MEMS switches.

Table 1-2 Summary of devices described above

	Folded- flexure beams switches	Platinum coated polysilicon switches	Laterally actuated ruthenium switches	TiN based vertically actuated switch
Pattern method	Photolithography	Photolithography	EBL	Photolithography
Typical movable structure dimension	60 $\mu\text{m} \times 60 \mu\text{m}$	16 $\mu\text{m} \times 0.8 \mu\text{m}$	5 $\mu\text{m} \times 0.5 \mu\text{m}$	0.7 $\mu\text{m} \times 0.2 \mu\text{m}$
Highest Process temperature	410 °C	1075 °C	1200 °C (250 °C after the first oxide deposition)	Not mentioned
Turn-on voltage	6 V	8 V	13 V	16 V
Working temperature	Up to 200 °C	Room temperature	Room temperature	Room temperature
Yield	>95% [99]	Not mentioned	1.5%	Not mentioned

1.6 N/MEMS Switches Applications

N/MEMS switches provide some unique properties which are unavailable in CMOS technology as well as most of the proposed CMOS-replacement electronics. Table 1-3 summarizes some of these features and their targeted applications. In this section, selected applications are reviewed to show the merits of introducing N/MEMS switch technology as a key component of electronics.

Table 1-3 Switch property versus application

Property	Application
Zero leakage	Low-power circuit, power gating, FPGA
Hysteresis, Stiction	Non-volatile memories
High temperature and radiation	Industrial, Military

1.6.1 Pure N/MEMS Switches Circuit

Although the slower switching speed induced by mechanical delay suggests that N/MEMS switches cannot match with CMOS in operational frequency, the zero leakage current properties makes N/MEMS switches a compelling technology in ultra-low power circuits. Moreover, its nature to resist high temperature and radiation opens another regime of harsh-environment electronics.

The most complex pure N/MEMS switches integrated circuit reported so far consists of 98 MEMS switches, where the single device operation has been described in section 1.5.1. [87, 106, 107, 121, 122]. It demonstrates the micro-architecture and circuit techniques for building multipliers with

switches. A 16-bit mechanical switch multiplier is shown in Figure 1-16. Experimental results indicate that pure switch technology consumes 10 times lower energy per operation when compared to an equivalent CMOS multiplier of 90 nm technology node.

The enhanced performance of the multiplier confirms that the advantage of energy-efficiency can be extended to larger arithmetic blocks, suggesting that large scale logic circuit such as microprocessors can be expected to demonstrate similar energy/performance improvements by using N/MEMS switches as the basic circuit functional elements.

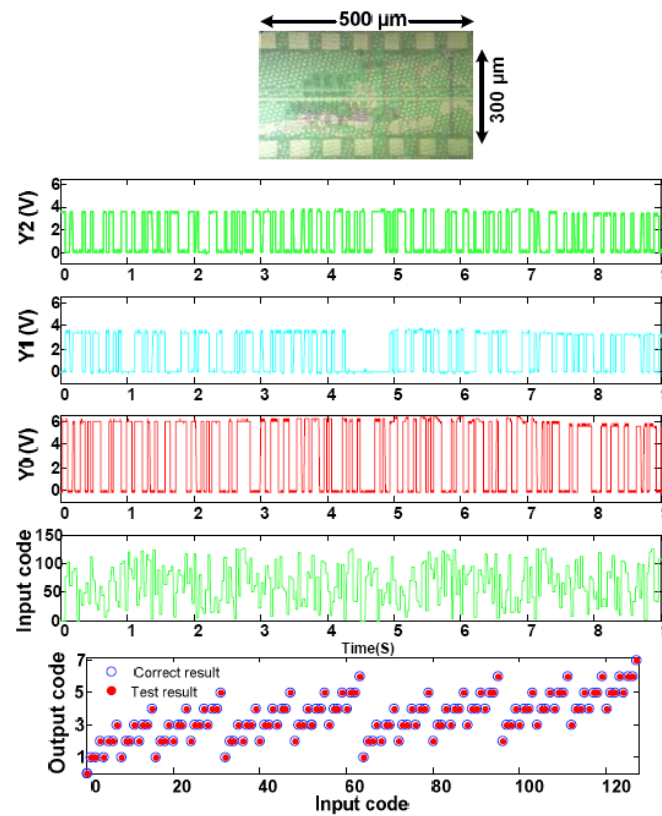


Figure 1-16 Experimental results of the MEMS switch circuit, adapted from [87]

1.6.2 NVM

After switches are turned on, adhesion force appears between the movable structure and the fixed electrode. If the adhesion force is large enough to overcome the spring restoring force, then even without the help of the electrostatic force, the on state of the switch can be preserved without power supply. With proper design of writing and erasing function, N/MEMS switches can be applied in non-volatile memory.

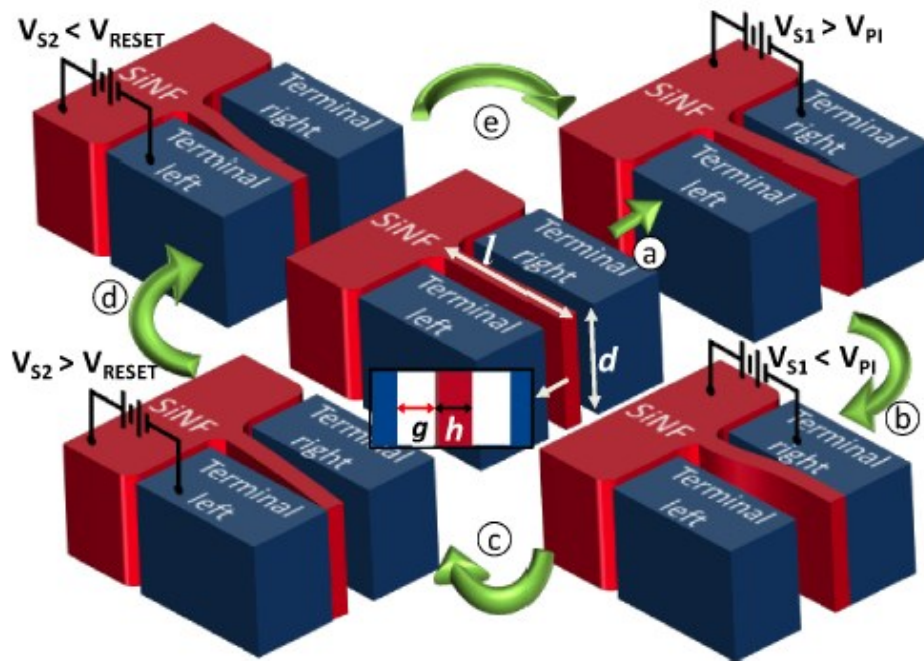


Figure 1-17 Schematic of NVM operation. Adapted from [123]

As shown in Figure 1-17, the silicon cantilever is actuated electrostatically to contact one of the two terminals when operation voltage is applied between the cantilever and either terminal [123-126]. After the cantilever is switched to one terminal, the bias voltage is turned off and the cantilever maintains its contact with this terminal due to adhesion between the surfaces of the silicon cantilever and electrode terminal. When the electrostatic potential is gradually

increased at the opposite terminal, the cantilever flips and switches towards the opposite lateral terminal. A silicon cantilever with dimension of 80 nm wide and 2 μm long is demonstrated to maintain its geometrical position even after the bias voltage is turned off. Bi-stable hysteresis behavior by writing and erasing voltage as low as 8.4 and 10.1 V is measured.

In Figure 1-18, repeatable write and erase operation is demonstrated by electrical measurement. Unfortunately, the devices are proven to stop working after 12 cycles, possibly due to the melting of silicon cantilever on one of the fixed electrodes caused by the large amount of joule heating.

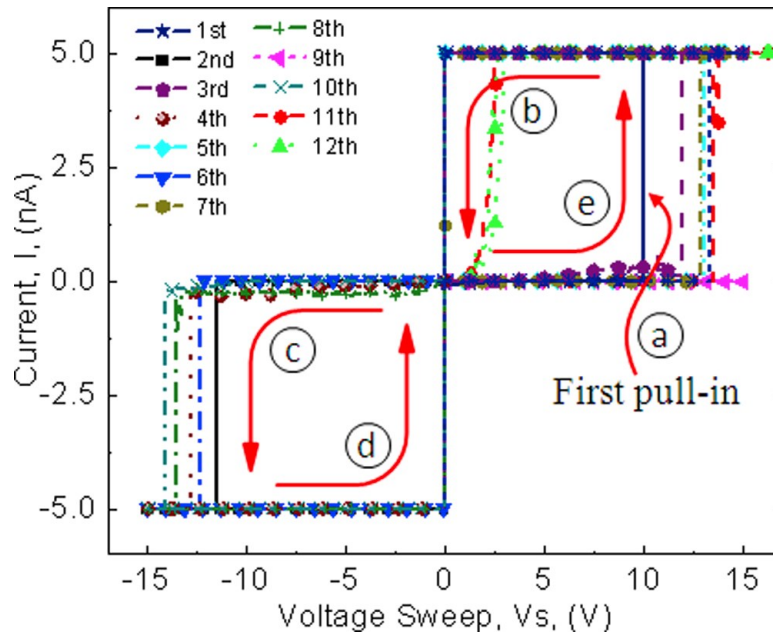


Figure 1-18 NVM I-V curve, adapted from [123].

1.6.3 Hybrid N/MEMS-CMOS Circuit

To fully utilize the zero leakage current properties of the N/MEMS switches and reduce the influence of their high mechanical delay, several

hybrid N/MEMS-CMOS circuits have been studied, such as power gating, FPGA and SRAM.

Switching off inactive CMOS logic circuit blocks by power gate is widely adopted to reduce power consumption. However, the leakage current of MOSFET power gates leads to the insufficient cutoff of the power supply. In contrast, N/MEMS switch based power gates are able to eliminate off-state leakage. Simple analysis and experimental demonstration have been made to predict the performance of MEMS switches over MOSFETs for power gates [20-23, 25, 127]. As shown in Figure 1-19, consider the off-period of CMOS logic circuit block is longer than 1 μs , N/MEMS based power gate shows significant advantages (up to 100 times less power consumption) over MOSFET power gating especially when the turn-on of the CMOS block is short.

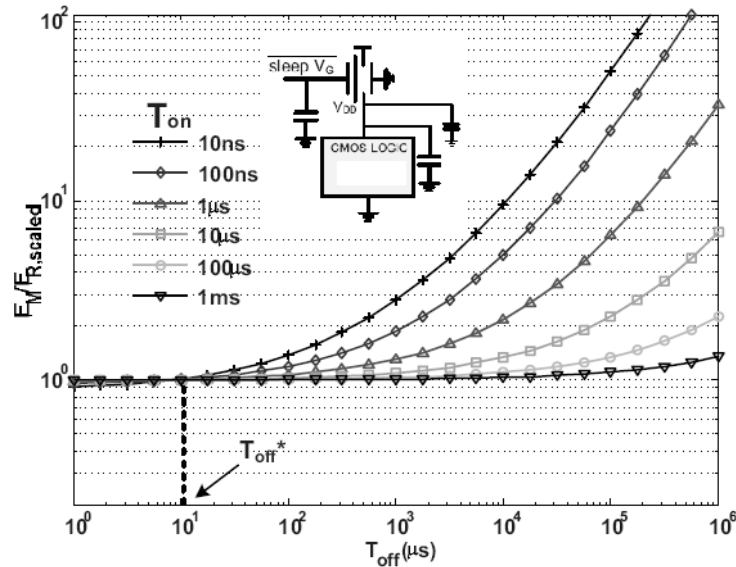


Figure 1-19 Energy ratio (MOSFETs to N/MEMS switches) vs. off-period for various on-period, for designs power gated with 90 nm MOSFETs and N/MEMS switches. Adapter from [21].

Similar principles can be applied to FPGA technology by replacing the routing switches in FPGA with N/MEMS switches as shown in Figure 1-20. Since FPGA programmable routing switches remain the same state after configuration, large mechanical delays of switches do not affect FPGA application performance. Moreover, N/MEMS switches with low on-state resistance value also contribute to improving the critical path delays in FPGA applications.

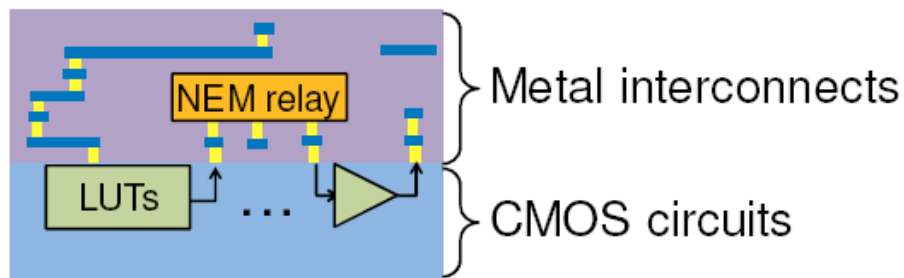


Figure 1-20 CMOS-NEMS FPGA using NEMS switches as routing Switches, adapted from [128].

Simulation results indicate that N/MEMS implemented FPGA can simultaneously achieve 10-fold leakage power reduction, 2-fold dynamic power reduction and 2-fold area reduction, without incurring any application speed penalty compared to a CMOS-only FPGA at the 22nm technology node as shown in Figure 1-21.

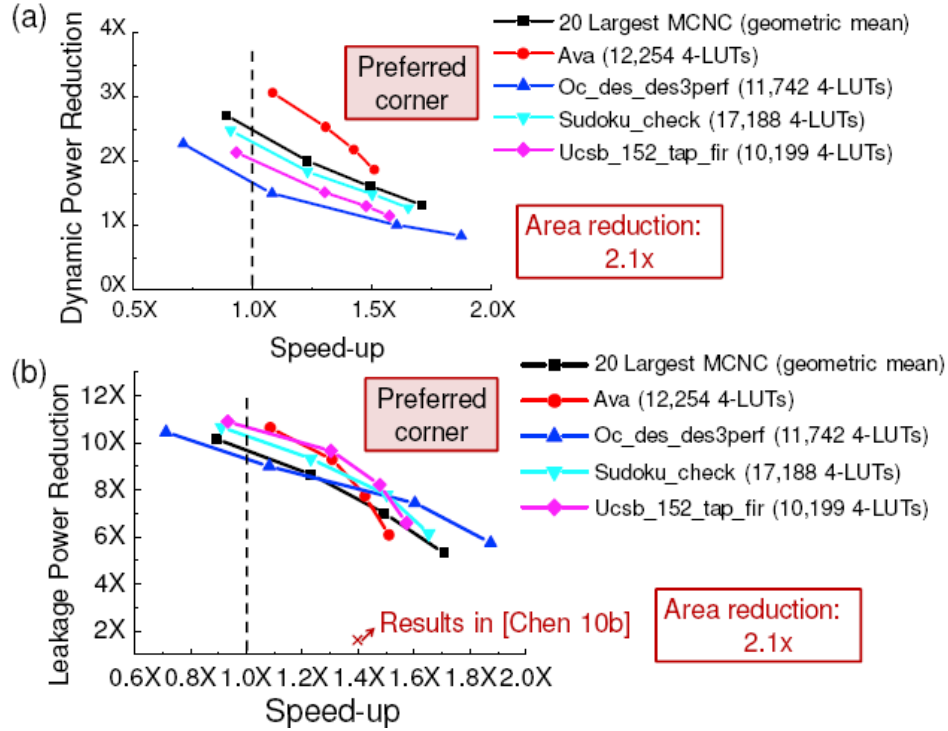


Figure 1-21 Power-speed trade-offs comparing CMOS-NEM FPGAs to a CMOS-only FPGA. (a) Dynamic power reduction vs. speed-up; (b) Leakage power reduction vs. speed-up, adapted from [128].

To achieve an increase in stability and decrease in leakage power dissipation, the pull-down MOSFETs in a conventional CMOS SRAM are replaced with N/MEMS switches (Figure 1-22). The zero leakage characteristic of NEMS switches results in a dramatic reduction in static power dissipation. The structure is designed so that the relatively long mechanical delay of the NEMS switches does not result in speed degradation. The read static noise margin is improved by 250%. In addition, by replacing the two transistors leaked most the current, MPD1 and MPD2, the static power dissipation decreases by 85%. The write delay decreases by 60%, and reading delay decreases by 10%.

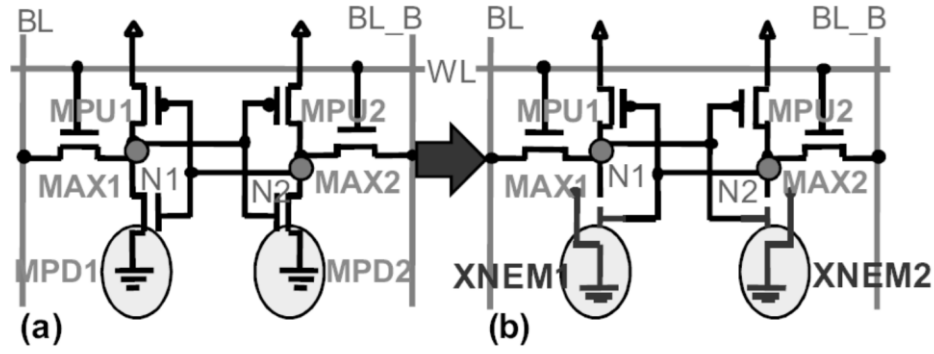


Figure 1-22 Schematic of (a) a conventional CMOS SRAM cell and (b) a NEMS/CMOS hybrid SRAM cell with NEMS Switches replacing the pull-down MOSFETs, adapted from [29].

1.7 Thesis organization

This thesis summarizes the various works on N/MEMS switches that were undertaken during the course of my candidature. The contents of each chapter in the thesis are as follows:

Chapter 2 will discuss the design consideration of electrostatically actuated N/MEMS switches, including the pull-in effect, pull-in voltage and the concerns of selecting contact material. From the device structure aspect, different actuation direction and beam type are discussed. The scalability of the switch technology is explained by analyzing the key parameters with the dimension scaling-down.

Chapter 3 will present a dual-silicon-nanowires based U-shaped NEMS switch with low pull-in voltage. The device is fabricated using standard CMOS compatible processes. The switch consists of a capacitive paddle with dimension of $2\ \mu\text{m}$ by $4\ \mu\text{m}$ mechanically supported by two silicon nanowires, suspended on top of the substrate with a gap of $145\ \text{nm}$. The nanowires are $5\ \mu\text{m}$ long with cross-section of $90\ \text{nm}$ by $90\ \text{nm}$. The average pull-in voltage is

about 1.12 V and the ratio of the on/off current is measured to be over 10000. According to the measurement results, this U-shape structure demonstrates great potential in lowering down the pull-in voltage.

Chapter 4 will provide an all metal based electrostatic NEMS switch fabricated using a one mask process. To enhance the reliability of NEMS switch and address a few issues with Si nanowire based devices, in chapter 4 and chapter 5, the main focus is to design a NEMS switch with CMOS compatible process, metal-to-metal contact, low contact resistance, good process yield and capability of harsh environment operation. The Damascene-like process is designed to ensure a clean, high aspect ratio, metal-to-metal mechanical contact. Molybdenum is used as the structural material. The devices show an abrupt switching behavior of 10^8 on/off ratio. High temperature cycling behavior is demonstrated in a vacuum chamber at 300 °C for more than 28 hours.

Chapter 5 will discuss the further optimization of all metal based NEMS switches. With reliable Damascene-like process, 800 devices with different dimensions have been measured with respect to the pull-in voltage and process yield. Dimensions with 100 % yield have been identified. General design rules of high yield dimension have also been proposed.

Finally, the main contributions of this thesis and suggestions for future works will be summarized in Chapter 6.

Chapter 2 Design Consideration of

N/MEMS Switches

Chapter 1 presented the basic structure of the operation of N/MEMS switches. By comparison of different actuation mechanisms, electrostatic actuation has been identified as the primary operation method for its extremely low active power consumption, simple fabrication process and scalability. Several prototype devices have been reviewed to show the zero off-state leakage current and abrupt on-to-off transition. Their process integration is also briefly discussed. As observed from these prototype devices, the barrier of dimensional miniaturization in the switch technology is developing a CMOS compatible process with low pull-in voltage, high yield and low contact resistance.

Moreover, applications of N/MEMS switches as well as hybrid N/MEMS-CMOS circuits are analyzed with the performance gain in power consumption. More than tenfold of energy saving can be achieved with these proposed circuit schemes.

To extend the discussion, this chapter also includes a detailed analysis of various parameters and design considerations of electrostatic actuated N/MEMS switches.

2.1 Pull-In Voltage

In conventional MOSFET, the current path between source and drain is established by the voltage applied to the gate electrode. Across the gate dielectric, the carrier concentration in the current path can be easily tuned by the gate voltage. However, in electrostatic N/MEMS switches, the gate is a conductive metal plane. When proper bias voltage is applied between the gate and the movable beam, the electrostatic force will attract the movable beam to physically form a current path.

The mechanical model of an electrostatic actuator used in the M / NEMS switches can be simplified as a parallel-plate capacitor as shown in Figure 2-1. The capacitor consists of a fixed electrode and a movable electrode with a spring constant of k . Voltage V applied across these two electrodes will generate electrostatic force to draw the movable electrode towards the fixed one.

Based on the charges stored in the parallel-plate capacitor between the movable plate and fixed ground plane, the electrostatic force acted on the movable structure with displacement z is:

$$F_e = \frac{d}{dz} \left(\frac{1}{2} CV^2 \right) = \frac{d}{dz} \left(\frac{\epsilon_0 AV^2}{2(g-z)} \right) = \frac{\epsilon_0 AV^2}{2(g-z)^2} \quad (2-1)$$

where C is the capacitance, A is the actuation area, g is the initial gap between two electrodes and ϵ_0 is the permittivity of the vacuum.

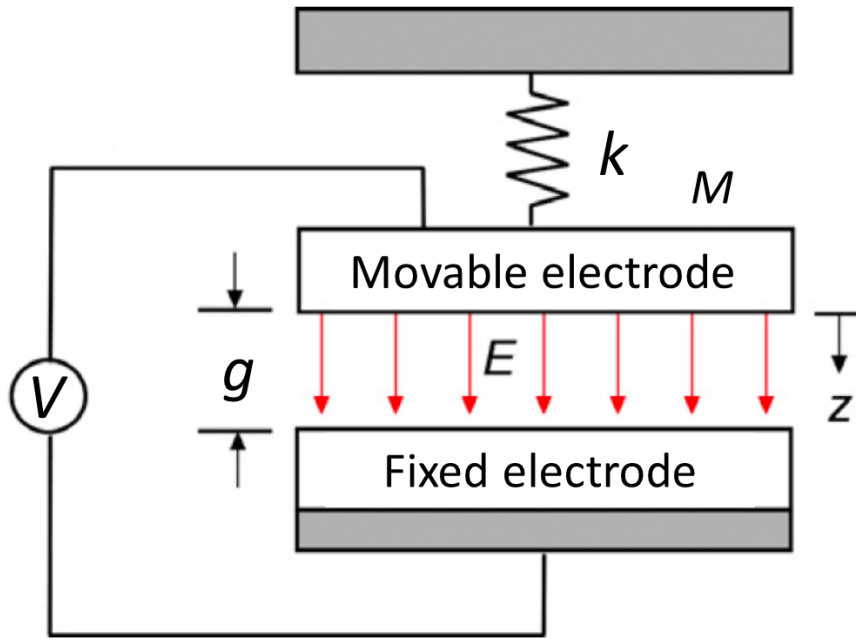


Figure 2-1 Schematic diagram of a N/MEMS switch

In equilibrium, the spring resorting force and the electrostatic force should be balanced:

$$kz = \frac{\epsilon_0 AV^2}{2(g - z)^2} \quad (2-2)$$

With a small value of V , the spring resorting force can balance the electrostatic force. When the displacement z increases, the electrostatic force will continue to grow while the mechanical restoring force, increasing only linearly, is unable to catch up with it. The two plates will be pulled against each other rapidly until made a contact. The phenomenon is well known as pull-in effect [129-143]. Thus, in electrostatic actuation, the gap closes abruptly when V is larger than the pull-in voltage V_{pi} . The maximum stable displacement can be achieved is $z_{pi}=g/3$ [137], therefore:

$$V_{pi} = \sqrt{\frac{8kg^3}{27\epsilon_0 A}} \quad (2-3)$$

It is important to note the electrostatic force is ambipolar, so a switch can be pulled-in by either a positive gate voltage or a negative gate voltage, to resemble both n-channel MOSFET and p-channel MOSFET at the same time. Therefore, complementary logic circuit design can be easily migrated to pure N/MEMS switch circuit design.

2.2 Contact Material

The functionality of N/MEMS switches relies on the repeatable on and off operation of the contact. As most of the actuators based MEMS devices developed by far are vibration based, no conclusive studies have been made for the N/MEMS switch contact reliability. Studies have been done by using poly Si [144-146], single-crystal Si[147], gold (Au) [148-150], Platinum (Pt) [67, 112, 113, 151, 152] , TiN, W, and Ru as the N/MEMS switches contact material. We can conclude some qualifications that the contact material should have.

First, the contact material should have a high hardness to withstand many contact cycles without damaging. For example, gold can provide extremely low on-resistance, but it is too soft and can be deformed easily. Furthermore, the material on both sides of the contact is preferred to be the same, as a material with higher hardness can easily damage the other side of contact with the lower hardness material.

Second, the contact material must be resistant to corrosion. Even a very thin layer of oxide on the contact surface will lead to a great increase of the contact resistance, except for contact material whose correspondent oxide is also conductive. For example, Ru and RuO₂ are both good conductors [153-155].

Next, the contact material should have a high melting point. The localized Joule heating effect could temporarily raise the temperature of the contact to a very high level.

Table 2-1 Properties of contact material at room temperature [156]

	Density ($\rho/\text{kg.m}^{-3}$)	Young's modulus (E/GPa)	Poisson's ratio (ν)	Melting point ($^{\circ}\text{C}$)	Thermal conductivity ($k/\text{W.m}^{-1}\text{.K}^{-1}$)	Coefficient linear thermal expansion ($\alpha/10^{-6}\text{K}^{-1}$)	Electrical resistivity ($\mu\Omega.\text{cm}$)	Mohs hardness	Resist to VHF
Silicon	2329	169 <110>	0.42	1409.9	83.7	2.56	100000	6-7	Yes
Aluminum	2699	70.2	0.35	660.3	237	23.03	2.65	2.5-3	Yes
Carbon (diamond)	3513	980	N.A.	3.820	990– 2320	1.2	1011	10	Yes
Copper	8960	129.8	0.34	1084.6	401	16.5	1.72	2.5-3	No
Gold	19320	78.5	0.42	1064.2	317	14.2	2.35	2.5	Yes
Molybdenum	10220	324.8	0.29	2621.9	142	5.4	5.2	5.5	Yes
Nickle	8902	199.5	0.31	1452.9	90.7	13.3	6.844	4	Yes
Platinum	21450	172.4	0.40	1771.9	71.6	9.1	9.81	4-4.5	Yes
Ruthenium	12370	432	0.25	2336.9	117	9.6	7.6	6-7	Yes
Titanium	4540	120.2	0.36	1668	21.9	8.35	42	6	Yes
Tungsten	19300	411	0.28	3413.9	174	4.59	5.65	7.5-8	Yes
TiN	5220	251	N.A.	2930	19.2	9.35	11.07	9	No

Last, the contact material should be resistant to the chemicals used for releasing the device. SiO₂ is used by most of the studies as sacrificial layer, because the VHF releasing process provides a very clean contact surface. Therefore, material cannot resist VHF would be unsuitable. Table 2-1 **Error! Reference source not found.** lists potential contact materials with their basic mechanical properties.

2.3 Laterally and Vertically Actuated

There are two types of N/MEMS switches: vertically and laterally actuated as shown in Figure 2-2. For a vertically actuated switch, the beam is suspended above the gate and drain terminal, which moves vertically towards the other two terminals after actuation. Laterally actuated switch has all the terminals in the same plane, thus, the beam moves laterally towards the other two terminals. The previous chapter discussed about the prototypes of other groups that have demonstrated the functionality of both types of switches. The advantages and constraints of these two types will be discussed below.

For a vertically actuated switch, the fabrication consists of multiple layers of material deposition and patterning. From substrate to top layer, the bottom electrode, sacrificial layer and movable structure are constructed in sequence. Based on this process, the thickness of each layer can be well controlled. It is a great advantage as the sacrificial material is targeted to be very thin to achieve low pull-in voltage. Moreover, the movable structure can consist of a number of different materials as shown in section 1.5.1, a thin metal layer is used as current path and a thick low stress layer is used to ensure the movable beam without significant deformation. As a number of deposition and etching

processes are involved, vertically actuated switches require a more complicated process, where 4~8 layers of mask are usually used in recent studies [157-161].

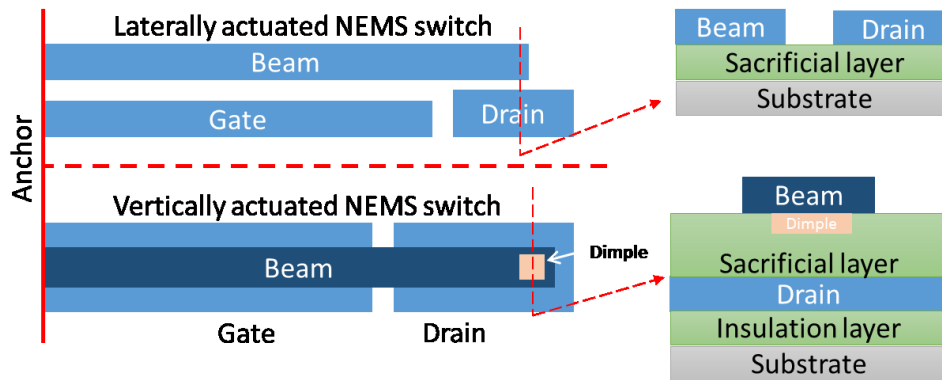


Figure 2-2 Schematic of laterally and vertically actuated switches. The drain terminal is closer to the beam to ensure no gate to beam pull-in. The cross-section views of each type are shown on the right.

Laterally actuated switches have all the terminals on the same layer of material and all the structures patterned at the same time, which reduces a lot of fabrication steps compared to vertically actuated switches. Accordingly, the movable beam itself and its surrounded terminals are defined by a single lithography step, which avoids misalignment between lithography steps. Thus, the actuation gap width and beam width are defined by mask design, which means different application requirements can be met at the same time. This flexibility is useful when multiple demands such as different actuation voltage and switching speed are needed for different parts of the system.

Encapsulation process is necessary to ensure functionality and reliability of these switches for practical use, and it is more feasible and easier to start with a laterally actuated switch as it has an almost flat surface after fabrication. It

only needs in-plane motion, therefore only an encapsulation shell of relatively low height is needed.

2.4 Fixed-Fixed Beam and Cantilever

As described in section 1.5, N/MEMS switches have two kinds of beam, fixed on both ends (fixed-fixed beam) or fixed on one end (cantilever). These two types of beam have a significant difference in the pull-in voltage and responds to residual stress.

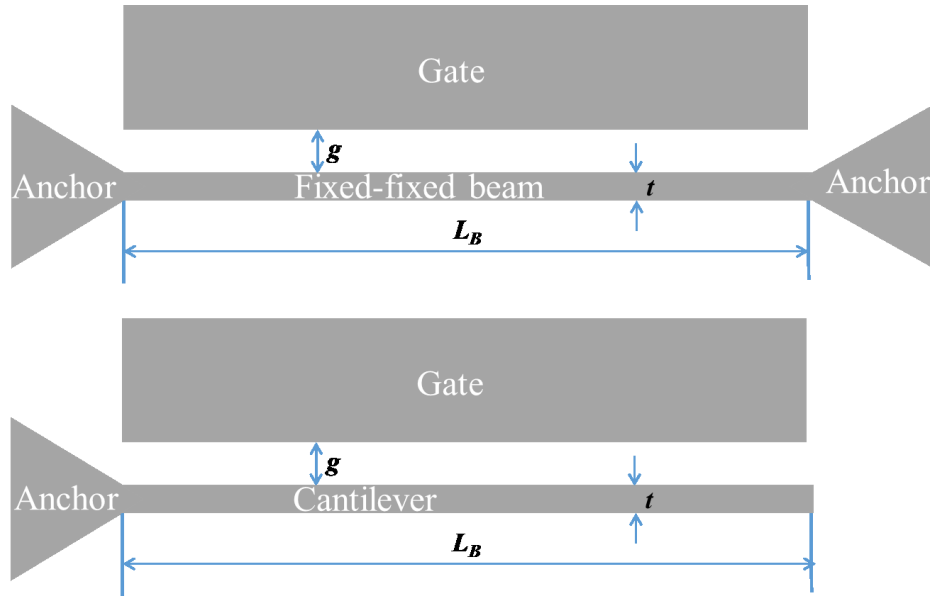


Figure 2-3 Fixed-fixed beam and cantilever

From equation (2-1) we learn that the spring constant k is closely related to the pull-in voltage. For the fixed-fixed beam case, k is given by [131, 134, 135]

$$k = \frac{32Ewt^3}{L_B^3} \quad (2-4)$$

where E is the Young's modulus of the material, w is the out-of plane thickness of the beam, t is the width of the beam and L_B is the beam length.

For cantilever case, k is given by:

$$k = \frac{2Ewt^3}{3L_B^3} \quad (2-5)$$

Substituting equation (2-4) and (2-5) into equation (2-3), we get the pull-in voltage for the fixed - fixed beam:

$$V_{pi} = \sqrt{\frac{256Et^3g^3}{27\varepsilon_0L_B^4}} \quad (2-6)$$

For cantilever:

$$V_{pi} = \sqrt{\frac{16Et^3g^3}{81\varepsilon_0L_B^4}} \quad (2-7)$$

Therefore, for devices with same dimensions, fixed-fixed beam needs 6.9 times higher pull-in voltage than cantilever devices.

One the other hand, the switching frequency of N/MEMS switches is very close to the natural frequency of the beam:

$$f = \frac{1}{2\pi} \sqrt{\frac{k}{m}} \quad (2-8)$$

where m is the mass of the beam. Similarly, the switching speed of the fixed - fixed beam is 6.9 times faster than cantilever with same dimension.

Despite of the mechanical property difference, another consideration should be taken into account to select from fixed-fixed beam and cantilever. In the

fabrication process, material deposition often happens at an elevated temperature. As a result, a mismatch of thermal expansion usually exists between the substrate and the deposited thin film, which will result in a residual stress.

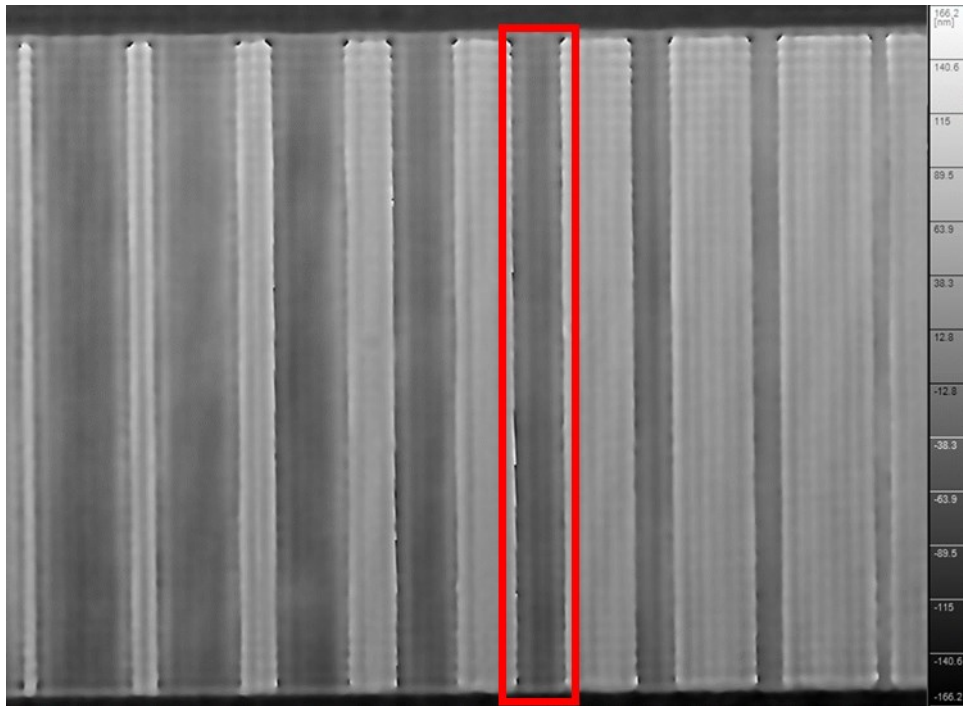


Figure 2-4 Phase pattern of a fixed-fixed beam in holography microscope, phase change for one period (white to black) represents deformation of 332.4 nm. The red rectangle enclosed one of the beams. No severe color change represents a flat topography of the beam. the beam length: 80 μm .

For fixed-fixed beam case, the compressive residual stress leads to beam buckling, but usually the phenomenon is not very severe (Figure 2-4). However, in cantilever case, a uniformly disturbed stress will not deform the beam at all. The deformation of the cantilever is mainly caused by the vertical stress gradient that results from the non-uniform stress acting over the film thickness. Both residual stress and vertical stress gradient are difficult to be optimized to a very small, uniformly value across the wafer.

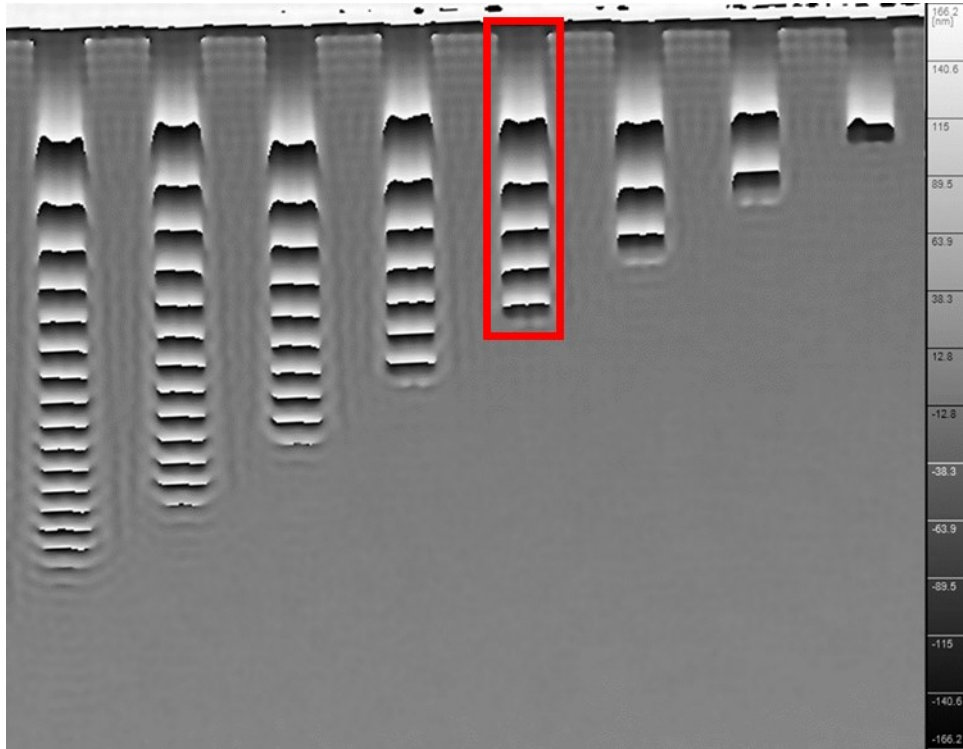


Figure 2-5 Phase pattern of cantilever beam in holography microscope, phase change for one period (white to black) represents deformation of 332.4 nm. The red rectangle enclosed one of the beams. More than 5 times of phase change can be found on the beam represents more than 1.5 μm bending. beam width: 4 μm

Figure 2-4 and Figure 2-5 show the phase pattern under holographic microscope. The fixed-fixed beam and cantilever are fabricated with 500 nm thick Al. The two patterns are very close on the same wafer. It can be clearly observed that the fixed-fixed beam does not show much deformation but the cantilever one has a very high bending (one period of phase refers to deformation of 332 nm).

2.5 Scalability of N/MEMS Switches

Similar to the CMOS technology, dimensional scaling-down can be applied to the N/MEMS switches to improve the device density, switching speed, power consumption and pull-in voltage. By introducing dimensional scaling

factor U , we can quickly estimate the scalability of the N/MEMS switches technology by using the equation derived above. With every dimension reduced by U , the spring constant of beam ($k \propto \frac{wt^3}{L_B^3}$) will decrease by the factor of U . Therefore, the pull-in voltage, which is proportional to $\sqrt{\frac{kg^3}{A}}$, will also scale down by the factor of U . With the mass of the beam shrined by the factor of U^3 , the device frequency $\propto \sqrt{\frac{k}{m}}$ can be escalated by the factor of U .

Table 2-2 The scaling properties of N/MEMS technology.

Switch parameter	Scaling Factor
Spring Constant, k	$1/U$
Mass, m	$1/U^3$
Pull-In Voltage, V_{pi}	$1/U$
Speed	U
Device Density	U^2
Switching Energy	$1/U^3$
Contact resistance	U^2
Stray capacitance	$1/U^2$
Leakage current	1
Mechanical shock resistance	U^2

The power consumed by the N/MEMS switches should include the energy used to close the gap and charge the loading capacitance. Thereby, the switching energy per operation E which is proportional to CV^2 , will be decreased by U^3 , with capacitance and pull-in voltage all reduced by U . Consider the increase of operation frequency by U , increase of device density by U^2 for a given area and decrease of switching energy per operation by U , the power density of the N/MEMS switch chip will remain constant.

We can conclude here that the N/MEMS technology is sustainable. With smaller critical dimensions, the supply voltage is decreased, but at the same time the device performance is improved without trade-off of the power density. Table 2-2 summarizes the switches scaling-down parameters versus various parameters.

Chapter 3 U-Shaped NEMS Switches with Low Actuation Voltage

As discussed, electrostatic actuated N/MEMS switches are favored for their low power consumption and fast switching speed. One of the major problems with electrostatic N/MEMS switches is the high actuation voltage. The typical pull-in voltage is 5–30 V from the recent reports. The high actuation voltage makes the N/MEMS switches difficult to be integrated with CMOS as well as other electronics and also increases the overall power consumption. In this chapter, the major effort would be on the method to lower down the pull-in voltage.

We can quickly estimate the pull-in voltage using the equations introduced in the last chapter. During the fabrication, a mask with 1 μm minimal feature size is used. A single-crystal silicon beam in $\langle 110 \rangle$ direction with 1 μm by 1 μm cross-section and 50 μm in length is used, and both fixed-fixed beam and cantilever devices pull-in voltage are calculated in Table 3-1.

Table 3-1 Pull-in voltage of N/MEMS switches

Lithography resolution	1 μm		0.1 μm	
Beam Type	Fixed-fixed beam	Cantilever	Fixed-fixed beam	Cantilever
Cross-section	1 μm by 1 μm		0.1 μm by 0.1 μm	
Beam Length	50 μm		5 μm	
Actuation gap	1 μm		0.1 μm	
Pull-in voltage	170 V	24.6 V	17 V	2.46 V

The pull-in voltage is as high as 24.6 V for cantilever. Even with 100 nm lithography technology, the pull-in voltage is still 2.46 V, which is far beyond the supply voltage used by CMOS. This supply voltage gap makes NEMS-CMOS hybrid circuit integration difficult.

There are various approaches to deal with the high pull-in voltage issue and the most effective way is still to scale down the dimension. Carbon based materials have demonstrated its enormous potential to realize extremely small devices [162-169]. Such excellent switching characteristics can be exemplified by carbon nanotube (CNT) NEMS switches [33, 51, 133, 170-187]. CNT based switches can be operated at 4.5 V[188]. However, the fabrication processes for CNT is not CMOS compatible and the variability on the CNT alignment and dimension hinder CNT NEMS switches from developing into a mass market product. In addition, CNT also grows into metallic or semiconductor material randomly by nature, which makes the performance undetermined.

3.1 Silicon Nanowire

Silicon is a very suitable material to prototype small dimension devices. As we are targeting on a low pull-in voltage devices, vertically actuated switches are most applicable as smaller actuation gap and beam thickness are easier to achieve. Commercially available silicon-on-insulator (SOI) wafer provides various thickness combinations of device layer and buried-oxide (BOX) layer, which is satisfactory for structure layer and sacrificial layer. Moreover, the single crystal silicon device layer is stress free so that the initial beam bending can be ruled out. Thus, we decide to use a top-down approach to fabricate

silicon nanowire (SiNW) with SOI wafer to demonstrate NEMS switches of very small dimension features.

The scaling down of the dimension not only makes the nanowire easy to be actuated but also reduces the electrostatic force it receives. In this chapter, a dual-silicon-nanowires based U-shaped NEMS switch is designed and characterized to demonstrate its low actuation voltage. The fabricated NEMS switch shows a remarkably low pull-in voltage and nearly zero off current, high on/off current ratio and repeatable switching behavior in ambient air.

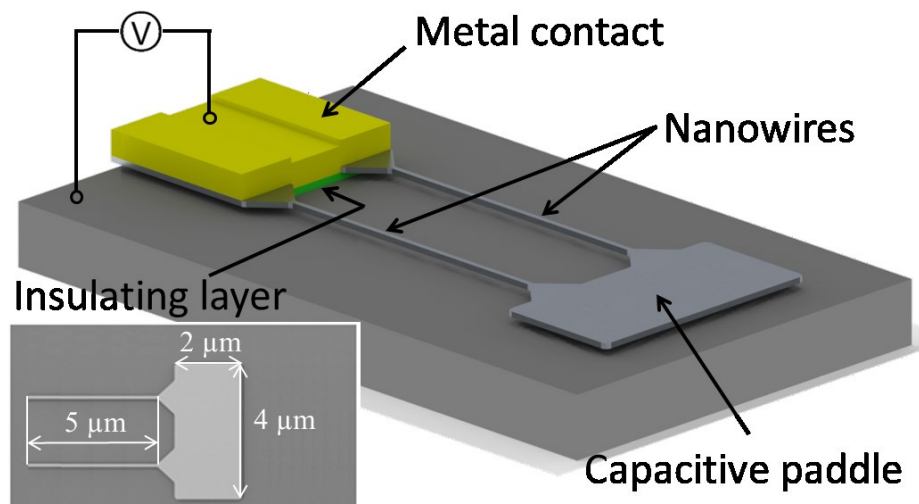


Figure 3-1 A schematic illustration of the U-shaped NEMS switch.

The schematic diagram of the NEMS switch is shown in Figure 3-1. Single crystal silicon is chosen as structural material because it is stress-free and very suitable to prototype these movable devices with very small dimensions. Two SiNWs are fixed at one end on top of the insulating layer and electrically connected by a metal contact. The other ends of the SiNWs are connected by a movable capacitive paddle to increase the electrostatic force. Therefore, the U-shaped structure consists of one capacitive paddle supported by two SiNWs

and suspended above the Si substrate. Both SiNWs have equal lengths of $5\text{ }\mu\text{m}$ and are separated by $2\text{ }\mu\text{m}$. The cross-section of the SiNW is nearly squarish, with side length of 90 nm . Once voltage is applied between the capacitive paddle and the substrate, the electrostatic force would bend the SiNWs down and the capacitive paddle would physical contact with the substrate. The combination of large capacitive paddle and flexible SiNWs makes the U-shaped structure bend more effectively under electrostatic actuation.

The purpose of using two SiNWs is to provide a balanced spring restoring force for the capacitive paddle, to avoid torsion behavior. The large capacitive paddle also provides a larger contact area, so that the joule heating effect could be attenuated to avoid heat concentration on a very small cross-section of a SiNW.

3.2 Simulation

Figure 3-2 shows the COMSOL[189] Finite element method (FEM) modeling performed to estimate the effect on the length variation of SiNW. During the modeling, a voltage difference is applied between the paddle and the substrate. The voltage is increased from 0 V to calculate the deformation of the switch at each voltage, until a voltage where no converged solution can be found. At this voltage, the paddle collapsed on the substrate, and we call it pull-in voltage. The size of the capacitive paddle and the gap are fixed in the simulation. When the length of SiNW equals to zero, which means the movable structure is only the capacitive paddle which is fixed at one end as a simple fix-free cantilever. The pull-in voltage of such cantilever type of switch increases to as high as 26.5 V . When very short SiNWs with a length of 0.2

μm are included in the simulation, the pull-in voltage dramatically decreases to 6.97 V.

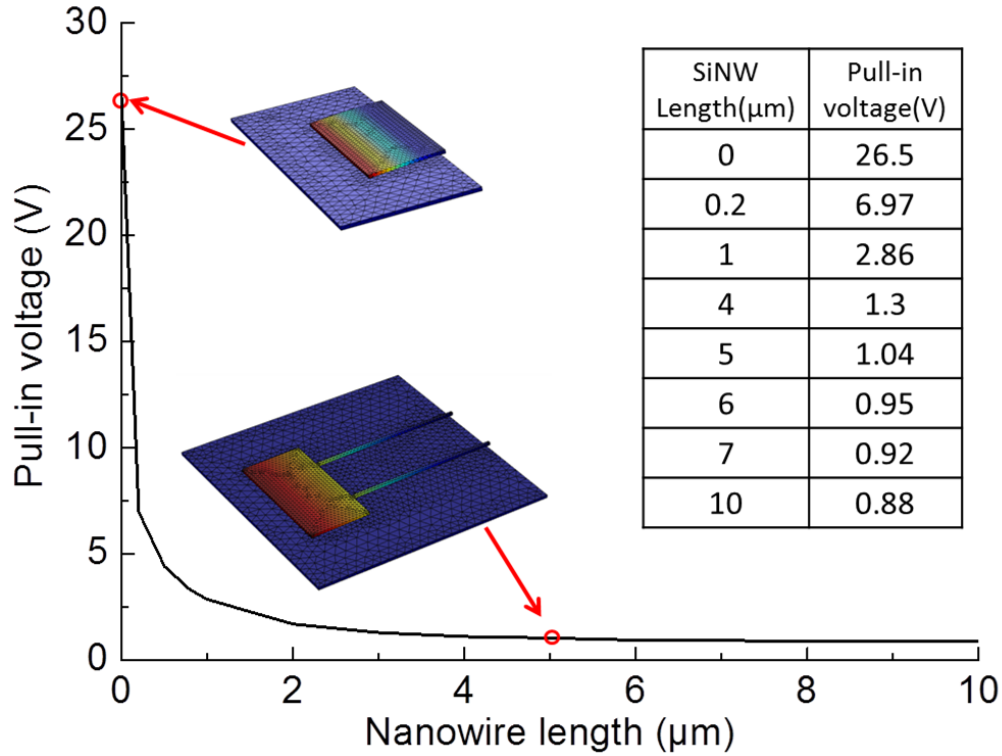


Figure 3-2 Simulated result for the influence on nanowire length versus pull-in voltage, as the length of SiNW varies from 0 μm to 10 μm .

In addition, simulation result has shown that the design has great effectiveness in reducing the pull-in voltage when SiNW length increases to 5 μm . Once the length of SiNW exceeds 5 μm , the pull-in voltage becomes saturated, without significant improvement in the performance in terms of pull-in voltage, and the paddle with a softer support structure suggests it would be easier to collapse. A better approach to further reduce the pull-in voltage is to enlarge the capacitive paddle. However, in this work, we choose 5 μm SiNWs and 2 μm paddle, as the pull-in voltage is projected to 1.04 V, very close to the modern CMOS supply voltage.

3.3 Fabrication Process

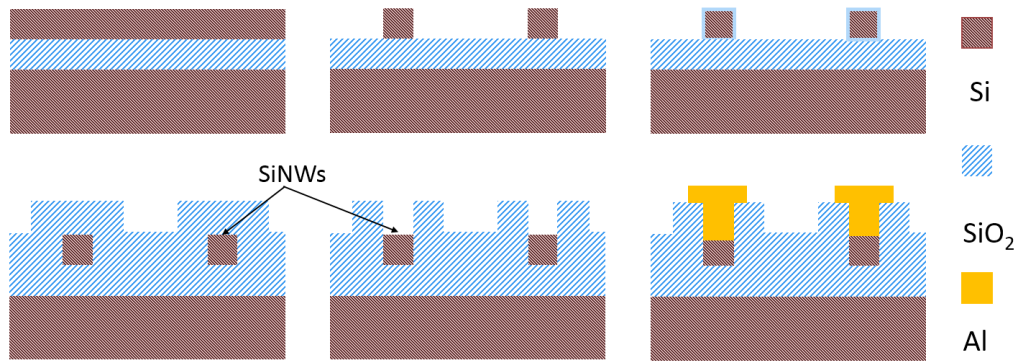


Figure 3-2 Process Flow for SiNW based NEMS switch

The fabrication process of the U-shaped NEMS switch starts with an SOI <100> wafer, with a device layer of 117 nm and buried oxide (BOX) layer of 145 nm as shown in Figure 3-2. The device layer is initially N-doped with an estimated doping level of $1.5 \times 10^{15} \text{ cm}^{-3}$ (the nominal resistivity is in the range from 8.5 $\Omega \cdot \text{cm}$ to 11.5 $\Omega \cdot \text{cm}$). In order to decrease the resistivity of the SiNWs, P-type implantation using BF^{2+} is performed with a dosage of $1 \times 10^{14} \text{ ion/cm}^2$ (twist 22° , tilt 7° , implantation energy: 50 KeV). After implantation, the carrier is activated by the rapid thermal annealing (RTA at 1050°C for 30 Sec). The SiNWs and the capacitive paddle are then patterned by photolithography. The mask used for SiNW features has a minimal dimension of 160 nm to define the width of the SiNW. The photoresist is then trimmed for 60 Sec after developed by the plasma induced feeding gas ($\text{He/O}_2 + \text{N}_2$) and the critical dimension is approximately decreased to 110 nm. After deep reactive ion etching (DRIE), the SiNW pattern is formed along <110> crystalline orientation. The plasma photoresist ashing ($\text{O}_2 + \text{N}_2$ at 250°C) is performed for 2 minutes. Piranha cleaning and dilute hydrochloric acid (DHF/1:100) are

carried out to remove the etching residue and the organic residue respectively. To further shrink down the dimension of SiNW, Sequentially, thermal dry oxidation (875°C for 120 minutes) is carried out. As a result, the SiNWs with average cross section of $90\text{ nm} \times 90\text{ nm}$ and length $5\text{ }\mu\text{m}$ are fabricated. Measurement result shows that the SiNW has a resistivity of $0.021\text{ }\Omega\cdot\text{cm}$, and the resistance per SiNW is $130\text{ k}\Omega$.

Figure 3-3 provides the SEM image of the SiNWs NEMS switches after release. The trapezoidal shaped cross-section with an average area of $90 \times 90\text{ nm}^2$ is confirmed by the transmission electron microscopy (TEM) image as shown in the inset of Figure 3-3. A 400 nm PECVD SiO_2 is then coated as the passivation layer to protect the SiNW from later metallization. After via opening on the passivation, 15s argon (Ar) ion bombardment is performed prior to sputtering of 750 nm aluminum (Al). A metallization is completed by dry etching process.

The device is released by VHF, which etching away the BOX layer between U-shaped NEMS switch and the silicon substrate. VHF is generated by 49% HF at room temperature. Aqueous solution of HF can be used for selective etching of sacrificial silicon dioxide. However, it requires special caution in handling because freestanding structures are very easy to stick to the substrate due to the surface tension force of the rinsing liquid when it evaporates. Moreover, the Al metal wire will not survive in the HF solution, but it is safe in VHF.

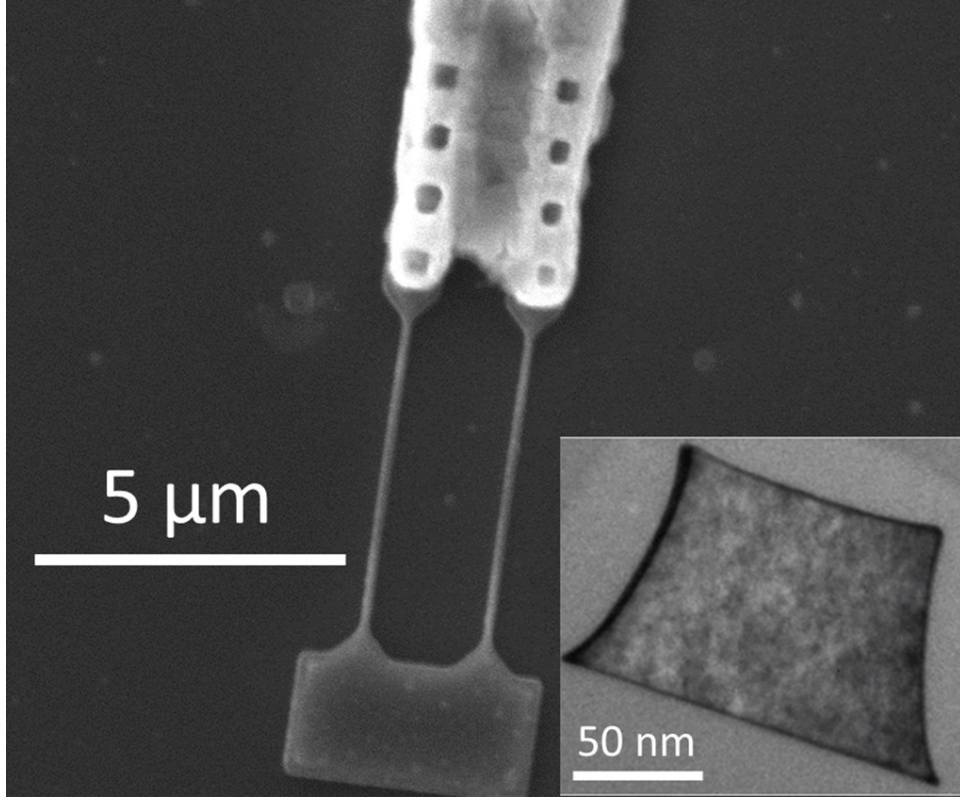
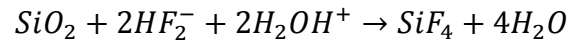
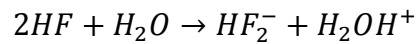


Figure 3-3 SEM photo of a U-shaped NEMS switch after HF vapor releasing, Inset: TEM image of a SiNW cross-section.

The VHF is designed to avoid liquid involve in the process. Unfortunately, considering the chemical reaction of SiO_2 etching by VHF, it still has water as a byproduct, the reaction can be described by [190]:



We can learn from the above equation that when reactions occur on the SiO_2 surface, the water adsorbed on the surface is believed to catalyze the reaction. Therefore, as a byproduct of the reaction, water cannot be avoided. To eliminate the stiction caused by liquid in the experiment, the chip would be pre-heated to 140 °C by a hotplate and put into the VHF at room temperature. During the release process, the chip is repeatedly heated on hotplate for every

20 Sec. A sum of 1 minute under VHF environment will fully release the SiO_2 beneath the capacitive paddle.

After the release process, the NEMS switches are checked under the scanning electron microscope (SEM). The SEM photo in Figure 3-3 shows a clean release process and the residues could be considered as acceptable. The surface of the substrate has not been attacked, and the two Si contact surfaces remain smooth and unaffected by the fabrication processes. The metal wire and contact with SiNW are well survived. No stiction or deflection could be found for SiNWs, and the paddle, which is formed by single crystal Si, remains free standing above the substrate.

3.4 Electrical Measurement

The device is then measured in air ambient with Agilent B1500A semiconductor device analyzer. Figure 3-4 shows the I-V plots of the fabricated U-shaped NEMS switch. Since it operates as a two-terminal switch, the voltage is applied between the U-shaped structure and the substrate. The voltage is swept from 0–3 V, with no compliance set for the current. The measured off current is around 10 pA, which is equivalent to the noise level of the measurement setup.

The first pull-in occurs at 1.81 V, causing the current to rapidly increase to 0.1 μA . Based on the applied voltage step of 10 mV, this abrupt switching slope is smaller than 4 mV/decade. This represents an ideal on/off current characteristic, where the sub-threshold slope is substantially lower than the theoretical limit of CMOS devices (60 mV/decade), and it also provides a

voltage range in which the off current is always limited to the noise level. The current continues to increase rapidly to $3 \mu\text{A}$, which is quite common in Si-Si contact. The on state current also indicates the resistance of the current loop mainly comes from the contact, which should be in the range of few hundreds of $\text{k}\Omega$.

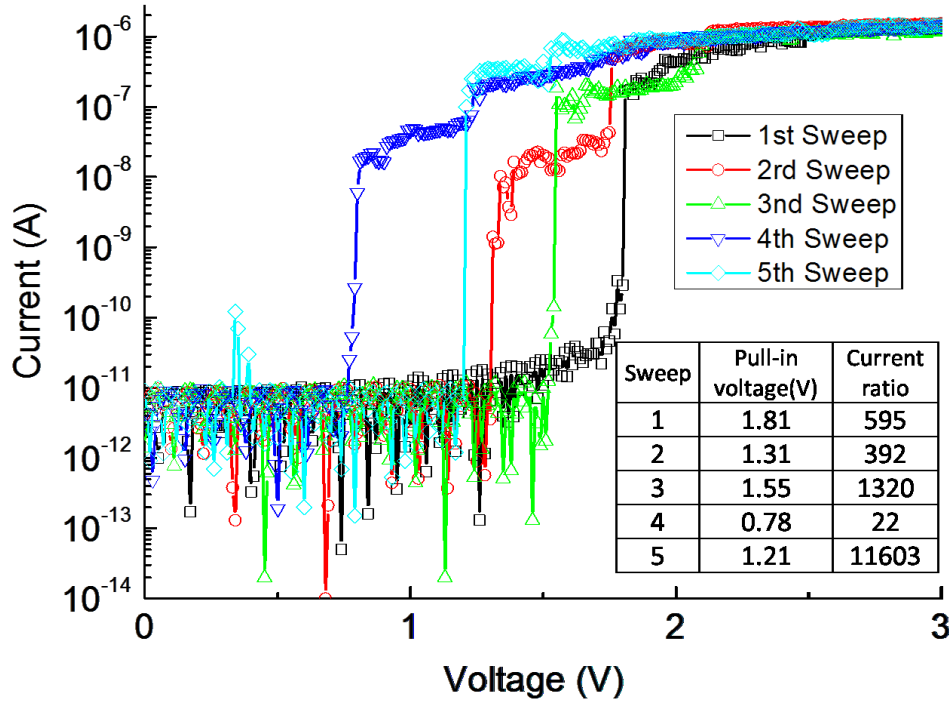


Figure 3-4 I-V characteristic of the device shown in Figure 3-3 for the first five switching cycles. The current ratio indicates the change in current that occurs within 10 mV of the pull-in voltage.

Hence, taking into consideration of our initial measurement results, our proposed U-shaped NEMS switch can be considered to be very attractive for low power applications due to its nearly zero leakage current and abrupt switching characteristics. It has a well-defined off-state range and the low pull-in voltage indicating its good compatibility with modern CMOS devices.

The following switching cycles also show a good turn-on switching behavior. The on/off state current maintains at the same level for every cycle.

The average pull-in voltage is 1.12 V. The pull-in voltage varies in a wide range of about 1 V. A possible reason for such pull-in voltage variation is the charging effect on the native oxide that has grown on the contact surface. During the electrical measurement, charges can be stored on these surfaces and an additional electrostatic force is formed to decrease the initial gap even the bias is removed. It also explains the reason why the first pull-in voltage is much larger than all the following sweeps after it.

Such kind of phenomenon cannot be avoided after VHF releasing for Si-Si contact working in ambient air condition. Joule heating caused by the current passing through the contact and SiNWs will make the condition even worse. Quickly encapsulating the devices into vacuum may help to reduce the effect but a thin layer of SiO₂ is still possible to grow on the surface during the wafer transfer. However, adding process to cover the contact with metal before release would largely improve the performance of the U-shaped NEMS switch, as it could avoid the charging issue and provide a much lower contact resistance.

However, we also observed that the nearly zero off current characteristics of the U-shaped NEMS switch start to deteriorate after five switching cycles (Figure 3-5). As the current going through the SiNW increase to 3 μ A, the nanowire suffers from an accumulative Joule heating effect after taking into consideration of its extremely small cross-section area. The oxide insulating layer beneath the SiNW would be physically damaged and eventually become welded in ambient air.

The device manages to operate for 12 cycles before no switching behavior is observed. Several techniques may help to improve endurance. Current limitation can be applied to the devices by introducing a series resistor. Replacing insulation layer with high melting point and strong hardness material is also promising to enhance the reliability of the device.

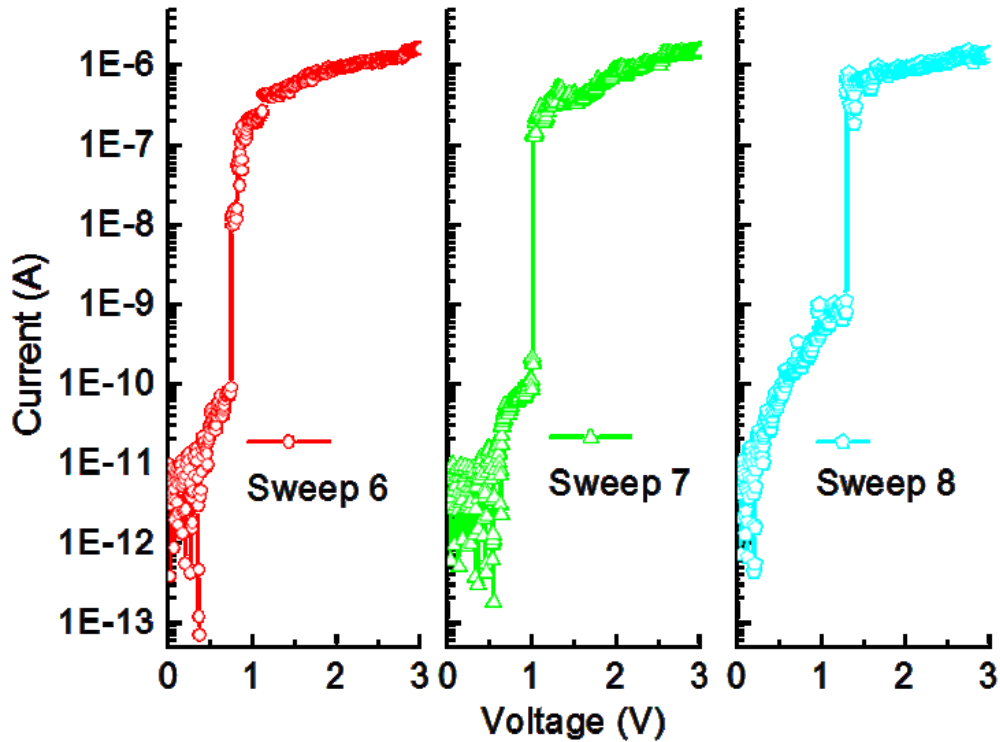


Figure 3-5 I-V characteristic of the device, with deterioration in off-state current during the 6 to 8 switching cycles.

After measurement, the failed devices are checked again in the SEM. In Figure 3-6, we can clearly see that the SiNW is welded and touched the substrate, but the paddle together with the contact area still reminds suspended above the substrate. We suspect the current through the SiNWs after physical contact may soften the SiNW, causing the device collapsed and further melting on the substrate.

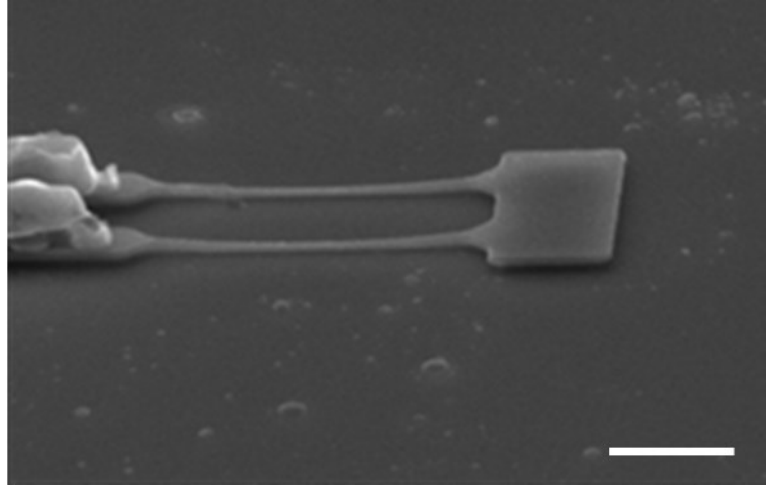


Figure 3-6 SiNWs NEMS switch welded on substrate, scale bar: 2 μm

For summary, the dual SiNWs based U-shaped NEMS switch shows excellent results in terms of lowering down the actuation voltage. We take advantage of the high electrostatic force generated from the large capacitive paddle and high flexibility from the single crystal SiNWs. The device shows great potential on the voltage compatibility with modern CMOS circuit. Further amendment with better insulting layer and contact material is possible so as to achieve a higher reliability and performance. Furthermore, both CMOS compatibility and ultra-low power consumption provide better integration with different kinds of devices.

3.5 Suggestion for Performance Improvement

During the design, simulation and measurement of U-shaped NEMS switch, we found that it is an effective structure to achieve a mechanical switch with 1V actuation voltage. The major drawback of this preliminary study lays into its reliability. The SiNWs based devices lack good endurance and stable pull-in voltage.

U-Shaped NEMS Switches with Low Actuation Voltage

The possible performance improvement aims for a highly reliable device. The actuator design should remain similar to achieve its low pull-in voltage. Single crystal silicon is still used as the structural material. Reliability of the devices should be enhanced with the following two ways, to avoid current directly passing through the SiNW and use metal as contact material. Therefore, instead of using two-terminal devices, the proposed new device would separate the actuation terminals and signal terminals as shown in Figure 3-7.

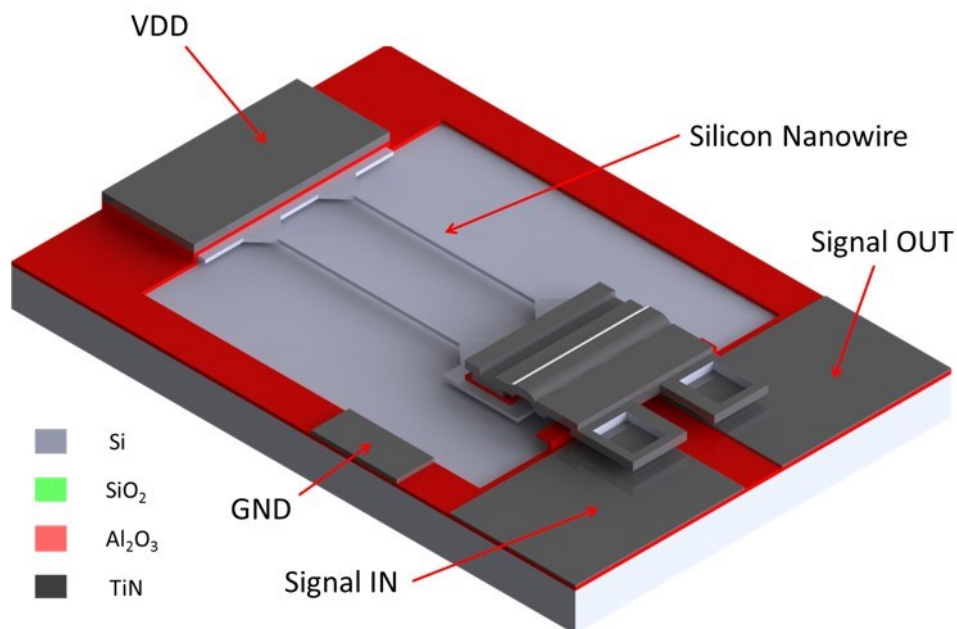


Figure 3-7 A schematic illustration of the U-shaped NEMS switch with metal contact.

A piece of metal structure for contact is attached to the head of the paddle and insulated with the actuation terminal by dielectric material. When bias voltage is applied between top actuation electrode and substrate actuation electrode, the nanowire will bend down by the electrostatic force. The contact electrodes will touch first, with a smaller gap than two actuation electrodes.

The signal would pass through the source terminal, the top contact electrode, and the drain terminal when actuation voltage is higher than the pull-in voltage.

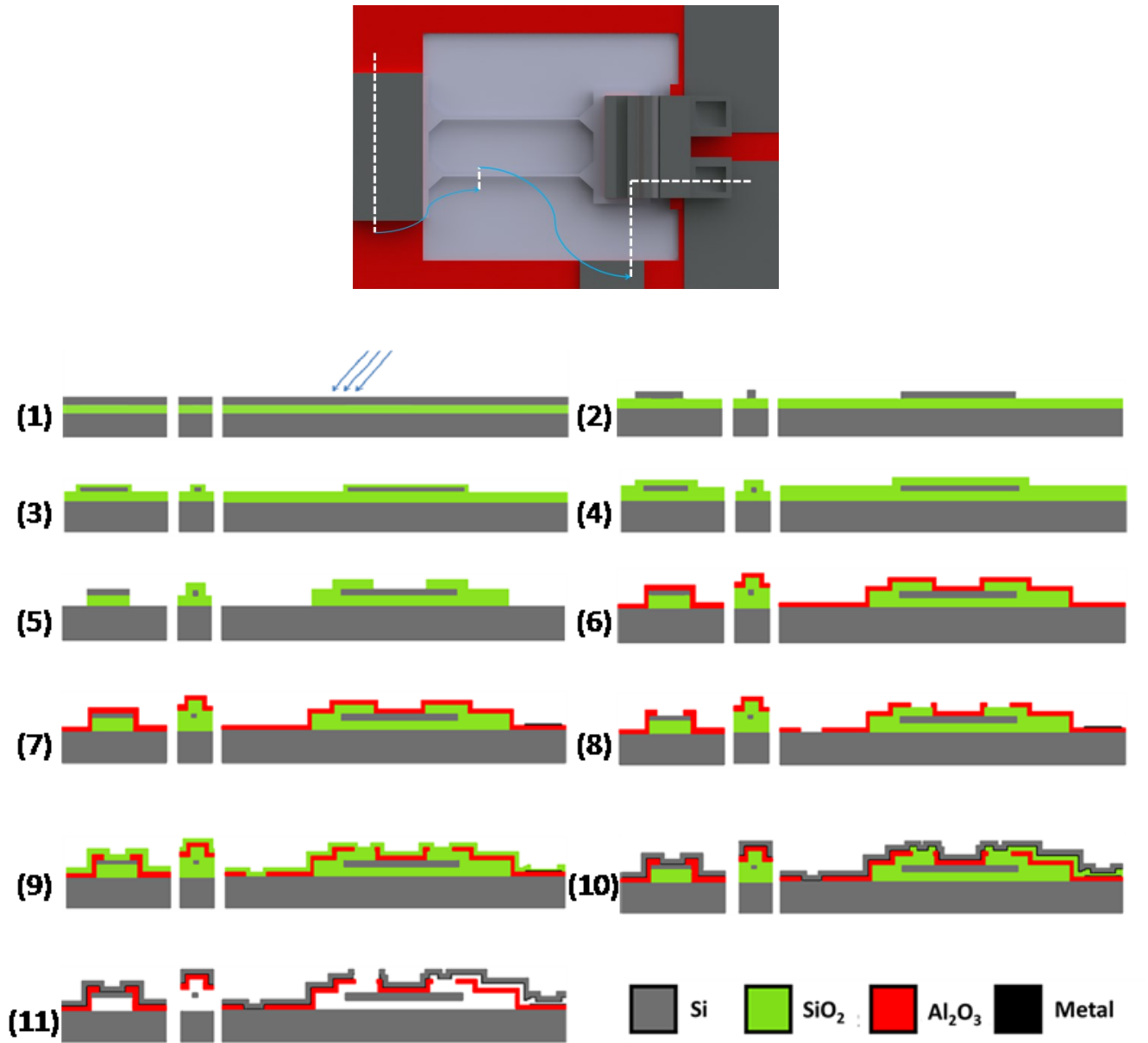


Figure 3-8 Process flow of Metal based SiNWs Switches, the cross-section is made along the white dash line above.

The proposed process flow is shown in Figure 3-9 using metal contact. The process begins with formation of silicon U-shaped structure includes implantation, silicon etching and thermal oxidation. Then a 100 nm LPCVD SiO₂ will be deposited for silicon nanowire protection. Two steps of SiO₂

U-Shaped NEMS Switches with Low Actuation Voltage

etching are performed at various places for material lands on silicon layer. The ALD Al_2O_3 layer will be deposited to act as the globe insulation and paddle insulation. Al_2O_3 is an insulation material with high melting point (2,072 °C) and is also resisting to VHF. Metal would be patterned as source and drain terminals above the Al_2O_3 layer. After the Al_2O_3 layer etching, the sacrificial oxide layer will be formed with dimple on contact, and the dimple is used to ensure physical contact only happen in the dimple area. The top metal electrode is then patterned, followed by VHF release.

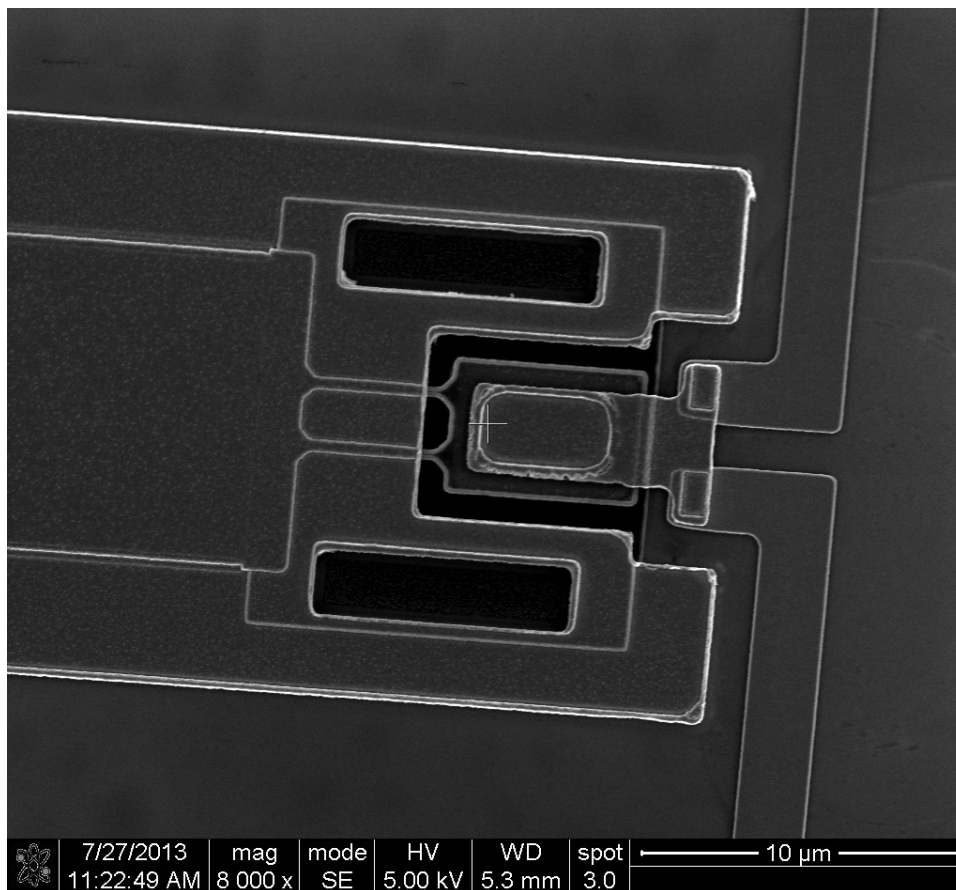


Figure 3-9 A released U-Shaped SiNW NEMS switch with metal contact

The above-mentioned process flow is an 8-mask process to leverage both stress-free Si structure layer and metal contact. A test run of this process has been conducted, the SEM of a released device can be found in Figure 3-9.

However, the electrical measurement shows the devices have a small leakage current between different terminals because of poor quality of the thin dielectric layer. The insulation is achieved by having a thin layer of dielectric material for a vertically actuated switch, any defect or fabrication errors will lead to a considerable amount of leakage current. Furthermore, residual stress on wafer usual result a curved wafer. Once the wafer under process is slightly curved, either the possibility of misalignment error increases or the further lithography process will be rejected by the stepper machine. Moreover, since the structural material is still Si, the pull-in voltage instability may still exist as the formation of the native oxide layer cannot be avoided. The above issues become hurdles which prevent us to come up with sound data. Hence we changed our design and optimization goal from making a low-driven voltage NEMS switches to NEMS switches with excellent reliability, while we still emphasize on CMOS compatible and simple fabrication process design. The further research effort and outcome will be described in the next chapter.

Chapter 4 All Metal Based NEMS Switches

Electrostatically actuated N/MEMS switches have been attracting attention for their excellent switching properties including zero-leakage current, abrupt switch behavior and potential to operate at high temperature [34, 191-197]. These unique properties make NEMS switch a strong candidate for ultra-low power electronics and harsh environment IC. As discussed in Chapter 1, research efforts so far face major challenges while scaling down the device dimensions, including high pull-in voltage, high contact resistance, limited reliability, poor process yield, and high process temperature. All these issues have a profound impact on implementing the NEMS switch technology.

The low process yield problem is especially important: without a stable fabrication process, research works are limited to demonstrating only a few key features of a single device. It is problematic to accumulate more knowledge to solve other issues with NEMS switches without a well-established process. As a result, there is no systematical study of NEMS switches so far.

Chapter 3 presents a SiNW based vertically actuated NEMS switch, the innovative device structure helps the NEMS switch to reach pull-in voltage of ~ 1 V for the first time. In the meantime, the yield and reliability of the pure Si based NEMS switch is not ideal. We learned that Si is not a suitable contact material, and thus to improve contact reliability and reduce contact resistance, metal-to-metal contact seems to be an inevitable choice. Recall the discussion

in section 2.2, contact materials are preferred to be high hardness and high melting temperature. Conventional conductive materials used in MEMS and CMOS fabrication like Al and Cu are not suitable. Thus, new material development needs to be addressed. The overall objective of this chapter is to develop a NEMS switches which covers the low temperature CMOS compatible process, metal-to-metal contact, low contact resistance, good process yield and capability of harsh environment operation. In chapter 4 and chapter 5, the development of all metal based NEMS switch would take consideration of these notable requirements and merits at the same time.

Two applications of NEMS switches are the primary motivations of the work in this chapter. The first one is the NEMS-CMOS integration. To build NEMS switch above the CMOS transistor, low temperature process must be used. Thus, current semiconductor based NEMS switches are not suitable since high temperature process is involved. Secondly, for high temperature application, using all metal based NEMS switches other than semiconductor based NEMS switches could largely reduce the resistance of the whole circuit. More detailed discussion is provided in section 4.1 and section 4.2 separately.

The major effort of this chapter lays on applying new material as well as developing new processes. We present a single mask, CMOS compatible process for all-metal-based NEMS switch, targeting to be used in NEMS-CMOS integration applications as well as NEMS-only logic circuits. Various electrical measurements under room temperature will demonstrate the superb performance of the fabricated devices. In the meantime, high temperature operation is also included to demonstrate the reliability of the NEMS switch.

Systematic study with a large number of devices characterized will be delivered in chapter 5, focusing on devices dimension optimization and failure analysis.

4.1 All-Metal-Based Laterally Actuated Switches for NEMS-CMOS integration

It would be difficult for NEMS switches to totally replace CMOS transistors in high performance ICs, since NEMS switches have a lower operating frequency due to their large mechanical delay. To avoid the low speed NEMS switches slowing down the circuit and fully utilize their zero leakage properties, several applications proposed for NEMS-CMOS integration has been reviewed in Section 1.6. By using NEMS switches to replace speed insensitive elements in FPGA [128, 198-201], power gating [21-23] and SRAM [27, 28, 202], it would largely reduce the power consumption of the whole NEMS-CMOS IC.

Therefore, directly fabricating NEMS switches on top of the CMOS layer (Figure 4-1) would be a realistic and cost-effective technique to realize hybrid NEMS-CMOS circuit [203, 204]. The semiconductor industry has developed air gap back end process [205] which is most suitable for the NEMS-CMOS hybrid circuit.

The following requirements should be fulfilled to enforce NEMS-CMOS integration: i) The NEMS switches should be realized by a low temperature CMOS-compatible process for the ease of implementing the process in a modern CMOS foundry; ii) A simple process is desired; especially when it can

leverage the existing metallization process; iii) The topography of the device should be small, to ensure the easy realization of devices with multiple layers stacking and wafer level encapsulation.

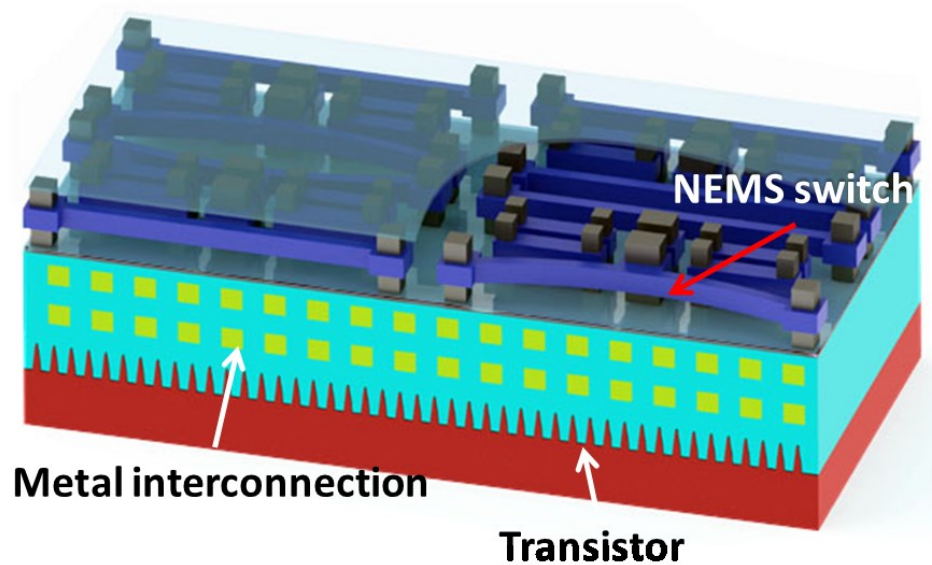


Figure 4-1 Schematic of building laterally actuated NEMS switches above CMOS. The NEMS switches are fabricated after transistor and interconnection process for NEMS-CMOS integration.

By far, most of the NEMS switches are not suitable for the NEMS-CMOS integration. Many reports lack demonstration of repeatable on/off switch behavior [187, 206, 207]. All-metal based NEMS switches seem to be a reasonable choice to align with post-CMOS process. The deposition method for metal is low temperature and it provides very low resistivity compared to semiconductor material.

In this study, laterally actuated switches are chosen because they can be fabricated with a single mask process, with all terminals formed in a single etching step. As shown in Figure 4-2, Gate, drain and source terminals are all in the same plane, with sufficient voltage applied between gate and source

terminal, the beam will bend in plane and make a physical contact to the drain terminal. In comparison, vertically actuated mechanical switches need 4~8 masks, multiple deposition and etching steps to assemble all terminals layer by layer. For three-dimensional integration, laterally actuated NEMS switches appear to have a much smaller topography, so that another layer of devices can be conveniently stacked on the existing device layer with a sacrificial layer and vias in between [25, 199, 208-211].

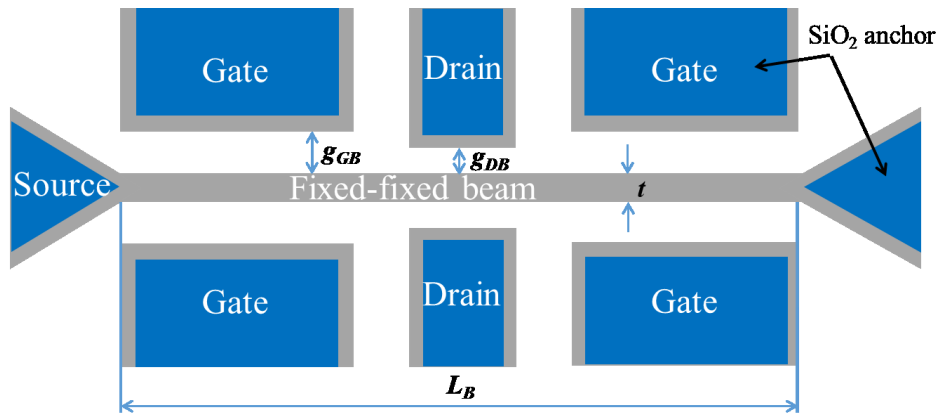


Figure 4-2 The schematic drawing of a laterally actuated all metal NEMS switch.

On the other hand, laterally actuated switches have one drawback compared to the vertically actuated switches. Recall equation (2-6), the pull-in voltage V_{pi} are highly sensitive to the beam width t , and gap g . To achieve a small V_{pi} , both beam width and gap should be small. In vertically actuated switches, these two values are decided by the film thickness, which can be easily scaled down to sub-100 nm. In laterally actuated switches, both parameters are controlled by the lithography, which means that it is much more difficult to scale them down. Thus, in this chapter, we put more focus on developing an all metal based NEMS switch with high reliability, which is fabricated by a CMOS compatible process with high process yield. The pull-in voltage is

limited by the lithography tool and we believe low pull-in voltage can be achieved with advanced lithography.

Since only one deposition step is involved in the laterally actuated switch fabrication, metallic material is most favorable for its low process temperature and low resistivity. As most of the device failures happen in the contact area, including welding, material transfer, delamination, and destruction [36], metals of high hardness and high melting point are commonly used, such as ruthenium [154, 155, 212, 213], tungsten [40, 109, 214]. As a result, molybdenum (Mo), with high melting temperature of 2623°C and relatively high hardness, is selected as the structural material in this study. Among the high melting temperature metals, Mo has a low thermal expansion coefficient, and thus the mechanical deformation of the released structure would be less significant over a wide range of operation temperature. The processes for Mo deposition and dry etching are CMOS compatible.

The most critical step in the laterally actuated switches fabrication is the formation of actuation gap. A sub 100nm width is needed to obtain a suitable pull-in voltage. Further scaling down the device dimension requires an even smaller gap. Meanwhile, the etched sidewall has to be vertical and smooth in order to achieve larger contact surface area. Extremely clean surface is wanted, because contamination between contact surfaces could cause high contact resistance and localized heat flux fusing the contact. The existing metal etching process normally has a low aspect ratio and lacks a thorough cleaning method. Last but not the least, the metal thin film should be thick enough to limit the deformation within a reasonable level. To address these concerns, the

fabrication process described in the section 4.3 using the single Damascene process concept is able to provide the NEMS switches with a clean, smooth, high aspect ratio metallic contact surface.

4.2 The Desire of High Temperature NEMS Switches

Besides using the all metal based NEMS switch for NEMS-CMOS integration, we are also targeting the devices can be operated under high temperature. The operating temperature of IC made by conventional bulk CMOS technology is not more than 150°C due to its intrinsic limitation. Logic devices capable of working beyond 300 °C are extremely desired for several rugged electronics applications such as automotive and aerospace equipment, oil and gas drilling [215]. Wide band gap material including silicon carbide (SiC) could be a possible solution, [216] however existing SiC based transistor is still constrained by large-size, high-threshold voltage and temperature dependent leakage current, which makes SiC difficult to be developed in large-scale IC [196]. On the other hand, N/MEMS contact switches are attractive alternatives for low-power logic operation at high temperature.[217-223]

In an electrostatically actuated three terminals NEMS switch, the movable structure experiences electrostatic forces controlled by gate terminal. Other than the conducting path established by pull-in, all the terminals are separated by dielectric material or air gap. Although vacuum tunneling currents and Brownian motion displacement currents still exist, the thickness of the dielectric material or air gap in NEMS switch is significantly larger than the leakage path in modern CMOS transistors, so that the leakage current is

negligible even at high temperature. As long as the structural and contact materials maintain its electrical and mechanical properties, the devices will be functional as designed even in high temperature environment. However, challenges still remain for recently reported N/MEMS switches[224, 225]. Most of the mechanical switches with good reliability are still in MEMS domain and high temperature operation is rarely demonstrated.

Intuitively, material with high melting point is used for high temperature NEMS switches. The silicon carbide (SiC) based NEMS switch has been proven for its functionality at 500 °C[192, 194], however the method of fabricating of such devices is rather complicated and not cost effective. Compared to SiC, all metal-based NEMS switch would be much easier to be implemented into the conventional CMOS process. Several materials with high melting point, which could be suitable for high temperature NEMS switches application, have been used extensively in modern CMOS and MEMS manufacture, including tungsten[81], tantalum, ruthenium[116] and Mo. The existing back-end process developed for CMOS process can be refined and evolved into process for making all metal NEMS switches. Furthermore, the contact resistance of all metal NEMS switch would be significantly lower than semiconductor based NEMS switches, i.e., the Si or SiC based NEMS switches [226-228]. One more advantage with all metal-based switches is the same material can be used for active devices and electrical interconnection, so that the integration effort is significantly reduced.

4.3 Fabrication Process

In this work, we report laterally actuated Mo NEMS switch fabricated by a single deep ultraviolet (UV) photolithography mask so that this new approach can overcome the common drawback of the laterally actuated NEMS switch.

A schematic drawing of three-terminal NEMS switch can be found in Figure 4-2, where a movable beam is fixed at its both ends, acting as the source terminal, and two fixed drain terminals are anchored besides the middle of the beam on both sides. Four gate terminals surround the rest of the beam. When sufficient voltage is applied across two gate terminals (same side) and the beam, balanced electrostatic force from two gate electrodes accelerates the movable beam toward the fixed drain terminal on one side and the switch is turned on by forming a physical contact between source beam and drain terminal. Reducing certain dimensions of the device, especially reducing the beam width and actuation gap, leads to lower actuation voltage. Beam width and actuation gap need to be defined as sub-100 nm features for ~10V actuation voltage. Expensive lithography tools capable of defining sub-100nm features are available in the industry, but typically not in university research labs.

In the process described below, a 200 nm mask is used to successfully define a 100nm metal-to-metal gap. Unlike conventional process designed for laterally actuated NEMS switches, the active parts of the switches are defined by filling metal into a silicon dioxide mold. Two main targets are achieved using this method: a clean contact surface and a reduced actuation gap.

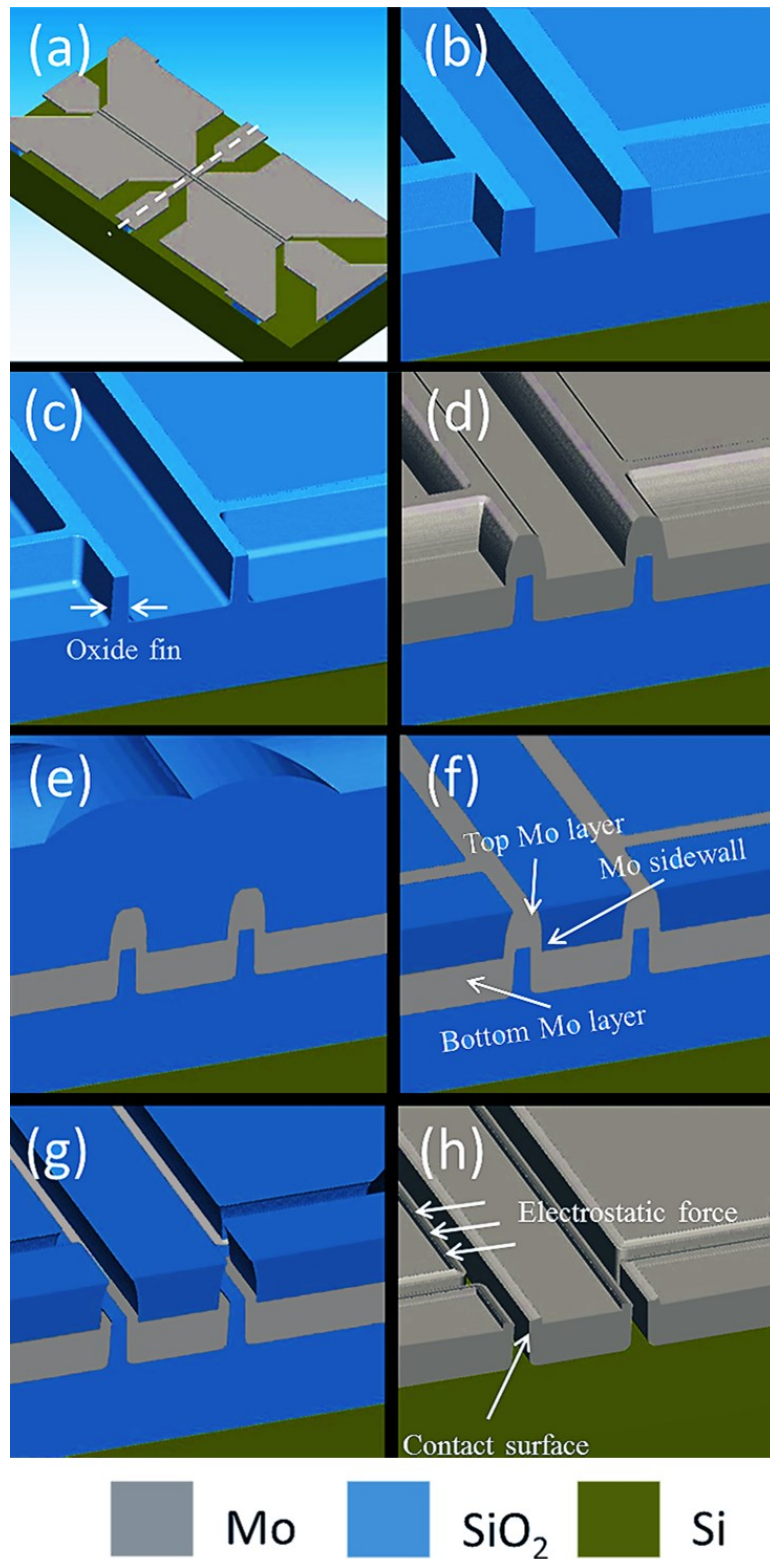


Figure 4-3 (a) The white dash line indicates the cross-section used in the following figures (b) SiO₂ RIE forming the trench (c) Wet etch reducing the oxide fin thickness (d) 300nm Mo PVD (e) 500nm HDP CVD SiO₂ (f) SiO₂ CMP (g) Mo RIE (h) VHF release

The process starts from a Si wafer with 1 μm silicon dioxide layer. Deep UV photolithography using 200 nm critical dimension mask defines the oxide features. The cross-section depicted for the whole process is cut across the middle of a fixed-fixed beam as shown in Figure 4-3 (a). The oxide layer is etched for 400 nm with reactive-ion etching (RIE) (Figure 4-3 (b)). The etching depth of oxide is controlled by time, which defines the depth of the mold and also determines the thickness of the beam in further steps. As a result, 600 nm oxide is left on the bottom of the oxide trench for insulation purpose. At this step, an oxide fin is formed, which will serve as a mold for metal structures as well as the sacrificial layer. After photoresist strip, the surface is cleaned with Piranha solution, and then the oxide fin is measured under SEM to have an 87° sidewall angle. Then wet etching is performed in 1:25 DHF to reduce the oxide fin thickness to 50nm from each side at 1nm/Sec etching rate. (Figure 4-3 (c)). A clean surface is prepared for the metal deposition afterward. Then a 300nm Mo layer has been deposited on oxide by PVD with 20% sidewall coverage, which leaves 60nm Mo layer on the sidewall (Figure 4-3 (d)), followed by 500 nm high-density plasma chemical vapor deposition (HDP CVD) SiO_2 to fill all the trenches (Figure 4-3 (e)). A SiO_2 chemical mechanical polishing (CMP) process is performed to expose the top MO layer. The whole wafer has been examined under SEM to check the outcome of CMP, even the smallest top Mo feature has been uncovered.

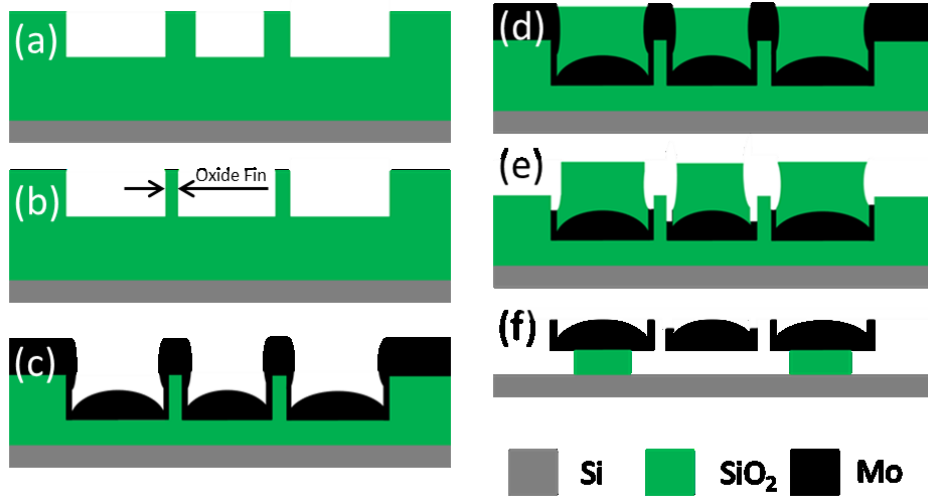


Figure 4-4 the cross-section view of process for all-metal-based NEMS Switch.

The remained oxide is used to protect the structural layer beneath (Figure 4-3 (f)). As we can observe, the oxide mold feature has been reversely transferred to the top oxide protecting layer, where it will serve as the hard mask for metal etch. Afterward, 300 nm Mo etching is done by RIE, to ensure the exposed top Mo layer is removed and only bottom Mo structural layer is left (Figure 4-3 (g)). Thus, the actuation gap and insulation between terminals are formed at the same time. The devices are finally released by VHF system (Figure 4-3 (h)). All processes are under 400 °C. A cross-section view of the whole process is provided in Figure 4-4. At the DHF etching step, when the minimum lithography dimension is used for both gap and beam width, decreased oxide fin thickness helps to reduce the pull-in voltage. Meanwhile, adding extra layer of SiO₂ on the sidewall achieves similar effect. However, reducing the oxide fin thickness seems to be a better choice, as the metal beam width is increased at the same time. Wider beam provides better thermal conductivity to quickly conduct the heat generated in the contact area. It has a

higher resonant frequency and switching speed. It is also more resistant to the beam to gate pull-in failure.

The differences between the proposed process above and conventional process (as described in section 1.5.3) are shown in Table 4-1. SiO₂ insulation layer and Mo structural layer are used in both cases. Although a few more steps are added, the proposed process shifts the formation of contact surface from Mo etching to deposition. The contact surface is not exposed until VHF release, which ensures etching residual do not contaminate the surface. The back end process in CMOS foundry could adapt this process easily with conventional dual-Damascene process.

Table 4-1 Process Differences between this work and conventional work

Item	This work	Conventional process
	SiO ₂ CVD → SiO ₂ Etching	
<i>Process</i>	→ Mo PVD → SiO ₂ CVD	SiO ₂ CVD → Mo PVD
<i>Sequence</i>	→ SiO ₂ CMP → Mo Etching	→ Mo Etching → VHF
	→ VHF	

SEM photos are taken during critical fabrication steps. Figure 4-5 shows the oxide fin after wet etching with 100 nm thickness and straight sidewall profile. As mentioned, the sidewall of the oxide fin before the wet etching is measured as 87°, which can be converted to 1:20 aspect ratio. Considering the height of the oxide fin of 400 nm, the minimum oxide thickness after wet etching is 40 nm.

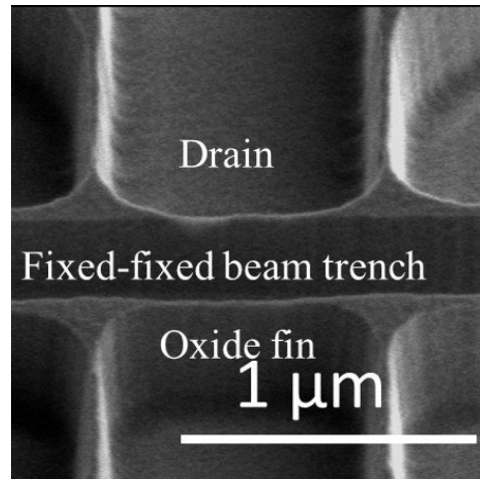


Figure 4-5 SEM photo of devices near the contact region after wet etch,

However, the oxide pattern is close to the limits of the photolithography machine in the first place, and the edge of the oxide fin is not 100% consistent and smooth. After a few attempts with different etching duration, we conclude that 100 nm oxide fin is the minimum thickness we can achieve with a uniform output of fin thickness.

Figure 4-6 shows the fully-covered oxide layer and large grains on the surface after Mo PVD. Metal deposition usually results in a rough surface like this. In vertically actuated N/MEMS switches, this surface will be used as one of the contact surface. Due to the surface roughness, only a small fraction of the apparent contact area is in physical touch when two surfaces are brought into contact. Therefore, the contact resistance of the N/MEMS switches is largely limited by the asperities on this surface. Fortunately, in the process, this rough surface with large grain is not used as contact surface.

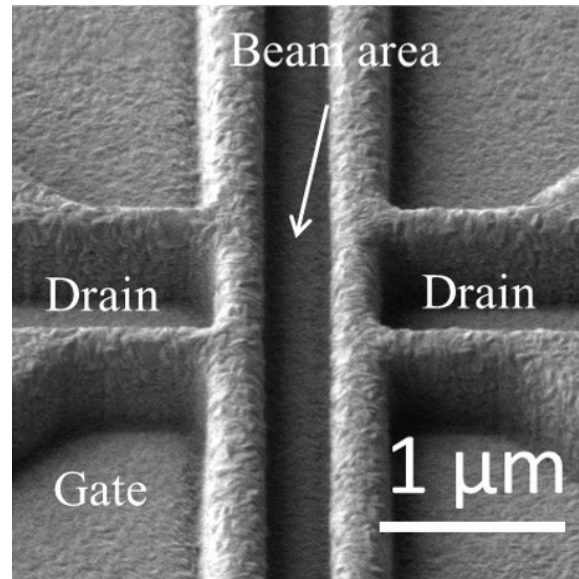


Figure 4-6 SEM photo of devices near the contact region after Mo deposition

Figure 4-7 shows Mo on top of the oxide fin can be successfully exposed after the oxide CMP step across the whole wafer. The CMP duration is designed to be over polished to make sure even the smallest features are consistently resolved. The extra CMP time do not have the impact of the final outcome of the devices as the two materials uncovered on the surface so far will be both removed in the future steps.

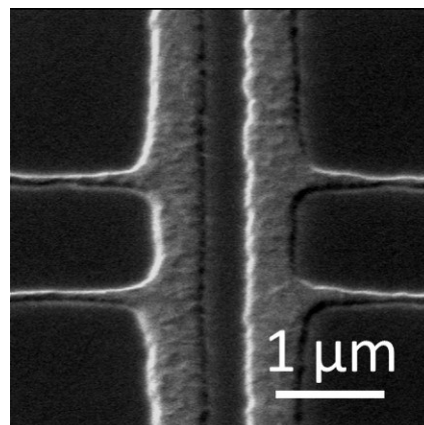


Figure 4-7 SEM photo of devices near the contact region after oxide CMP

Figure 4-8 shows after the top Mo layer etching, the upper edge of the oxide fin is exposed. We can see the very thin Mo sidewall through the gap between oxide fin and top oxide hard mask. The oxide hard mask is still remained to protect the 300 nm wide beam in the middle of the SEM.

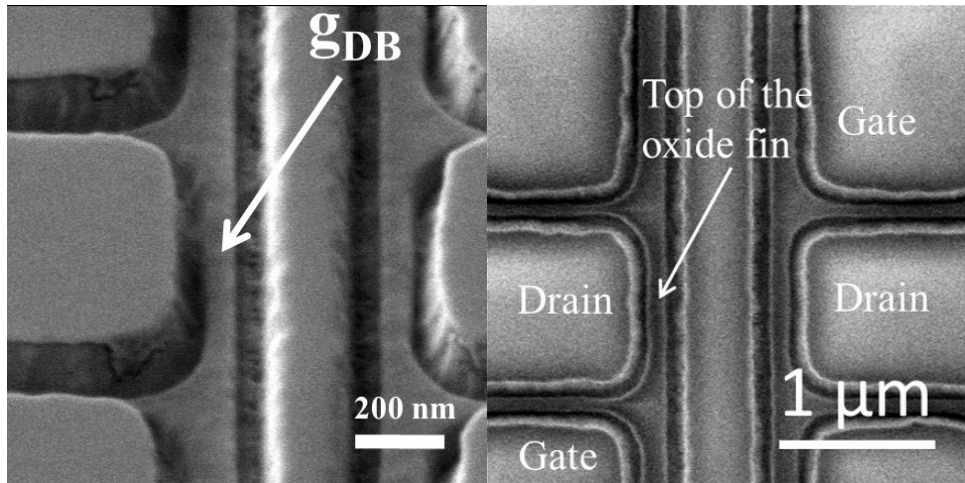


Figure 4-8 SEM photos of devices near the contact region after Mo RIE

Figure 4-9 shows a released fixed-fixed beam device. As large features are still being anchored on the substrate by the insulation SiO₂ beneath, no visible bending can be observed in this SEM. The VHF process results in a very uniform release and no attack on Mo by VHF can be found.

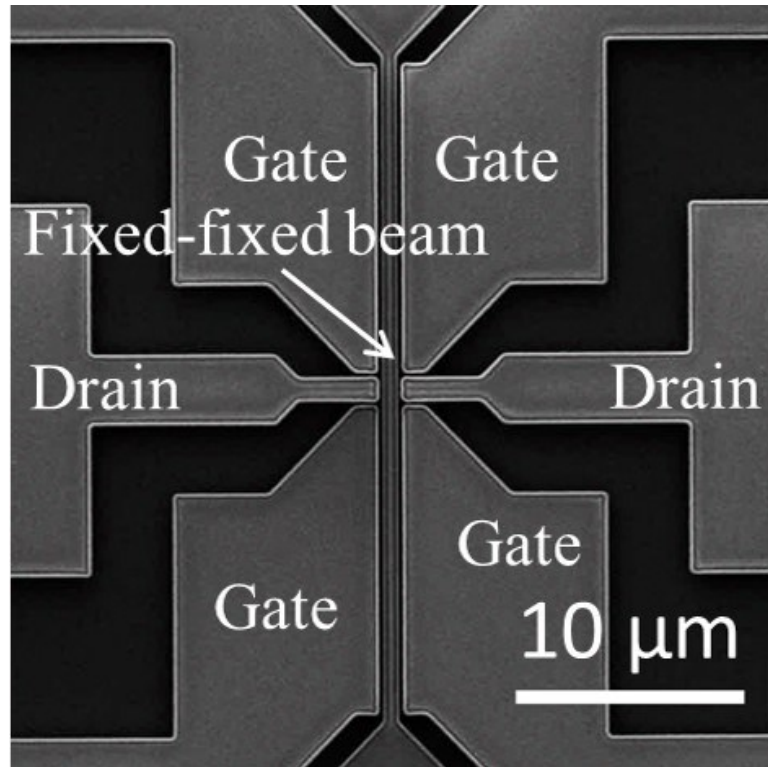


Figure 4-9 SEM photo of whole device after release.

Figure 4-10 shows the zoomed-in view of the contact area. When a released NEMS switch is focused under the SEM, charges from the electron gun accumulate on the metal. As the charges are not evenly distributed, a potential difference is presented between different terminals. With adequate electrostatic force generated by the charges, the beam is usually attracted to one of the drain terminal.

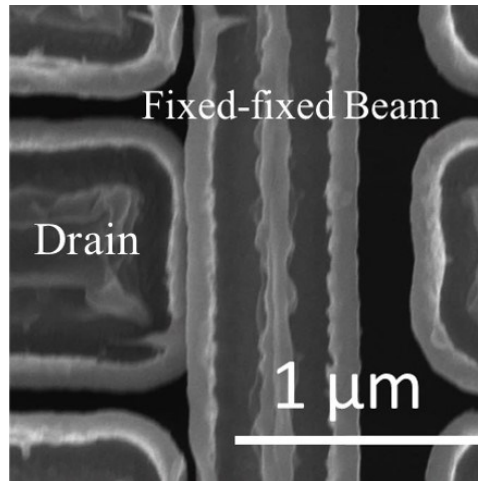


Figure 4-10 SEM photo of Fixed-fixed beam pull-in by electron charging.

The cantilever test structure (Figure 4-11) shows the Mo sidewall on the edges of the bottom Mo layer is almost etched away. This cantilever has a width of 300nm, which is the minimum width result from this process, although the wet etching process decreases the gap width, it also extends the beam width at the same time. The smooth Mo sidewall profile is shown in Figure 4-11, where no visible grain can be found compared to Figure 4-6.

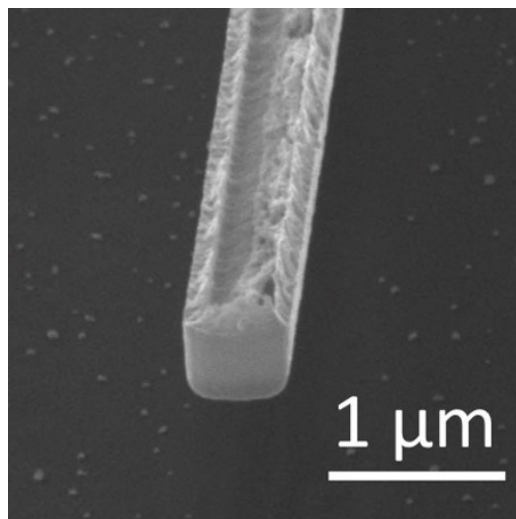


Figure 4-11 SEM photo of test structure of a single beam.

One alternative process to produce Mo beams via oxide mold is to directly CMP Mo layer after the Mo deposition process. In such way, a few depositing and etching steps can be saved. However, there is no existing Mo CMP process developed. Especially when Mo is directly on SiO_2 , where the adhesion between Mo and SiO_2 is poor. As shown in Figure 4-12, the Mo layer has been peeled off from the bottom oxide layer after a short CMP time. Adding an adhesive layer between Mo and oxide is also dangerous as the physical contact happens on that interface, so careful material selection is needed. As a result, we use SiO_2 CMP instead to form a hard mask layer above the Mo layer. Although the resultant top edge of the Mo structure layer is rough, it is not the critical contact surface and it should not have a large impact on the device performance.

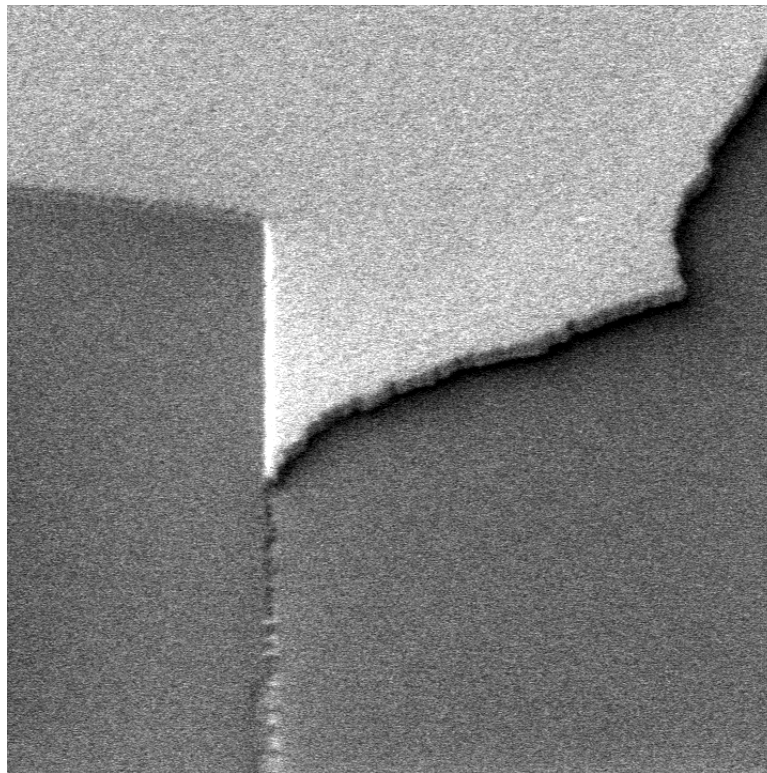


Figure 4-12 SEM photo of Mo peeled off from oxide

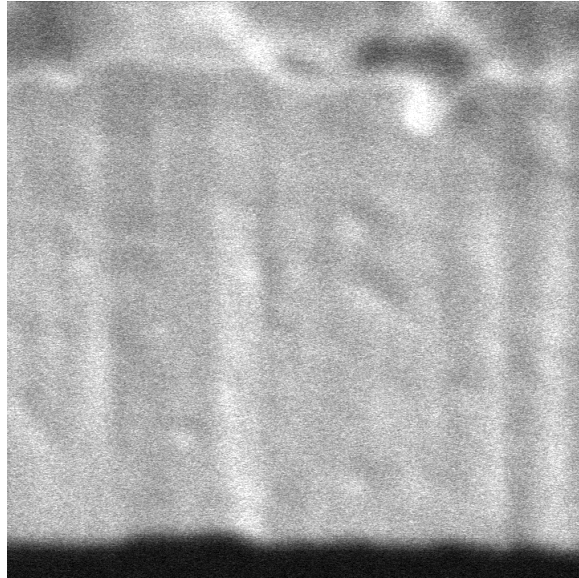


Figure 4-13 SEM photo of zoom-in view on the contact, field of view: 600nm by 600 nm

The roughness has great impact on the performance and reliability of the switch. A very rough surface means a large amount of current passing through a very limited number of contact points, which could cause welding and failure of the device. Figure 4-13 shows a zoom-in view of the contact surface. Compared to the coarse surface with metal gain shown in the Figure 4-6, it only shows a minimum roughness. The surface topology of the metal contact surface is transferred from the oxide mold, therefore, the effective contact points can be increased. Details on the contact resistance measurement will be presented in the later section.

On the other hand, a very smooth surface provides more contact area between the beam and drain. Extremely smooth surface is also undesirable, as it increases the surface interaction forces, which could cause the switch to stay in contact even after the gate voltage is removed.

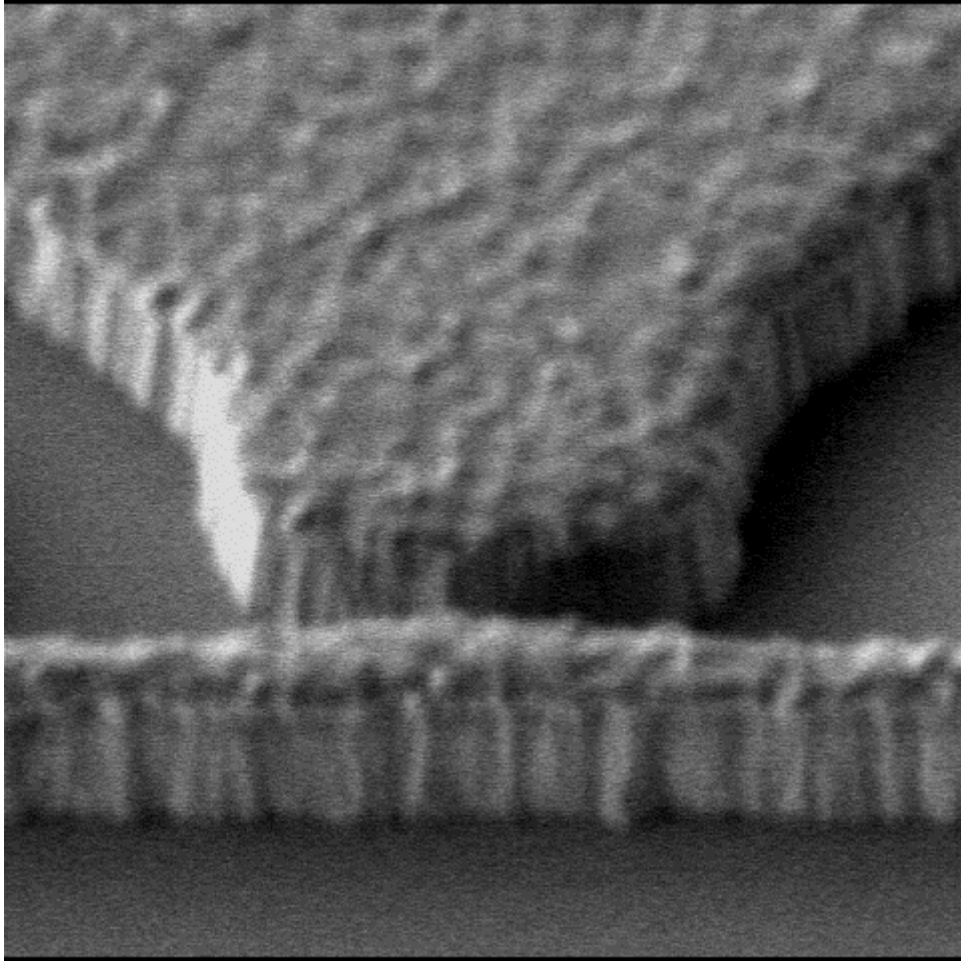


Figure 4-14 SEM photo of zoom-in view on the contact with direct Mo etch. field of view: 4 μm by 4 μm

In contrast, Figure 4-14 shows a test structure made by Mo direct etching. The beam width and gap width are the same as the process introduced above, the structure is fabricated by a simple Mo deposition and Mo etching. The etching surface shows a very high roughness as well as a much lower aspect ratio. Moreover, the etching residual is difficult to be removed as strong chemicals cannot be used with metal exposure.

4.4 Electrical Measurement with Limited Current

The pull-in voltage of NEMS switch can be roughly calculated by equation derived under the parallel plate assumption:

$$V_{pi} = \sqrt{\frac{256Et^3g_{GB}^3}{27\varepsilon_0L_B^4}} \quad (4-1)$$

where V_{pi} is the pull-in voltage, E is a Young's module of Mo (329 GPa), t the width of the beam, g_{GB} is the gap between the gate and fixed-fixed beam (as show in Figure 4-15), ε_0 is the permittivity of vacuum, and L_B is the length of the beam.

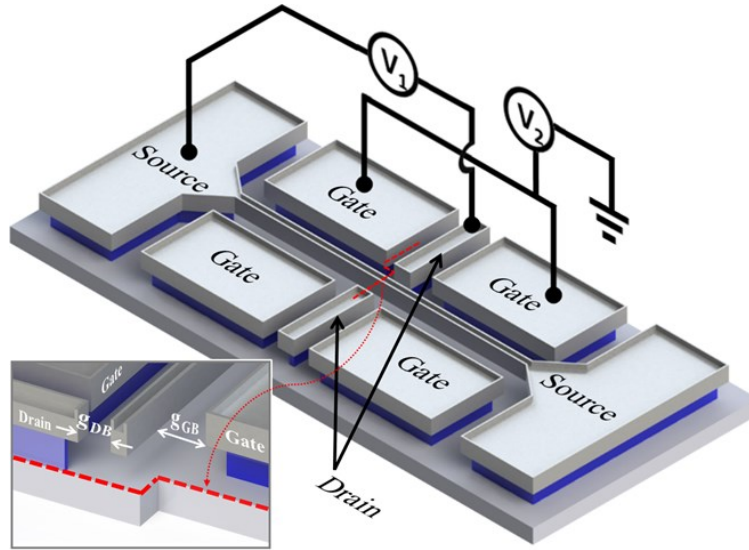


Figure 4-15 (a) The schematic drawing of an all metal NEMS contact switch. Inset: cross-section view of the device near contact region, the edge is defined by the red line in main figure. g_{DB} is the gap between beam to drain terminal, g_{GB} is the gap between beam to gate terminal

The wet etching process can reduce the gap but at the same time it will broaden the trench which will increase the width of the beam. As the process decreases the designed actuation gap g_{GB} from 250 nm to 150 nm, the beam

width extends with 100 nm as 50 nm etching has been done on both sides of the beam. The pull-in voltage versus g_{GB} , i.e., oxide fin thickness, is plotted on Figure 4-16 with different initial trench width cases.

The beginning point of the process is on the right side of the plot at 250 nm. For 200 nm trench beam width case, the pull-in voltage does not change a lot from 250 nm to 150 nm. When g_{GB} is 100 nm, the pull-in voltage is further reduced to 5V. Further reducing oxide fin to 30 nm could scale down the pull-in voltage to 1V. For a wider beam, this method appears to be more effective, for instance, the 400nm width trench case. The pull-in voltage is reduced from 24V to 16V after 100nm reduction on oxide fin thickness.

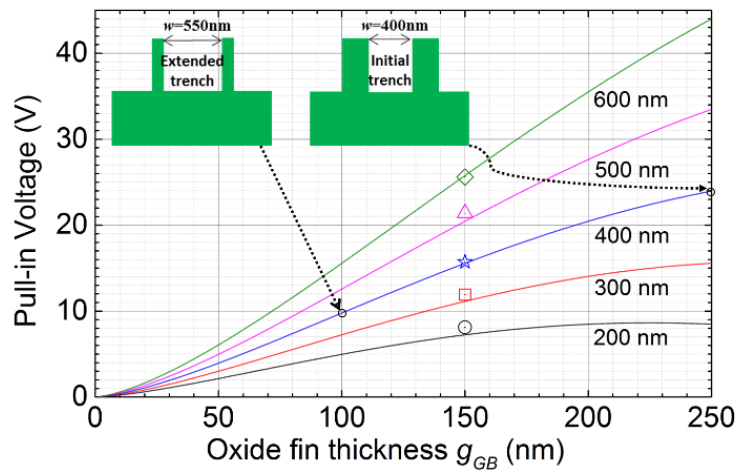


Figure 4-16 The Pull-in voltage of devices with 200nm, 300nm, 400nm, 500nm and 600nm initial oxide trench. The voltage varies with oxide fin thickness, which reduced by the wet etch process. The voltages projected to the 150nm oxide fin thickness for different initial trench width are 7.2V, 11.1V, 15.6V, 20.4V and 25.8V. Measured average pull-in voltage is plotted with the same color for varies trench width cases.

After the devices are released in VHF, they are loaded into a vacuum wafer probing system (Cascade Microtech, PMV200, as shown in Figure 4-17) at a high level of vacuum ($5.4\text{E-}6$ mbar). The devices were carefully characterized

and measured by a semiconductor parameter analyzer (Agilent Technology, B1500A).



Figure 4-17 The measurement setup with vacuum chamber

The setup has a noise level of 10pA (Figure 4-18) and an average open circuit current at 3.3 pA measured with test structure. All the devices tested are connected with the same configuration. The source terminal is connected to the ground state. Two gate terminals on the same side of a beam are connected together, when a voltage is applied to actuate the beam (Figure 4-15, V_2). A constant drain voltage of 1V is applied to detect the on/off state (Figure 4-15, V_1). The currents through all the terminals are monitored and have a limit of 10 nA to avoid excessive current melting its contact.

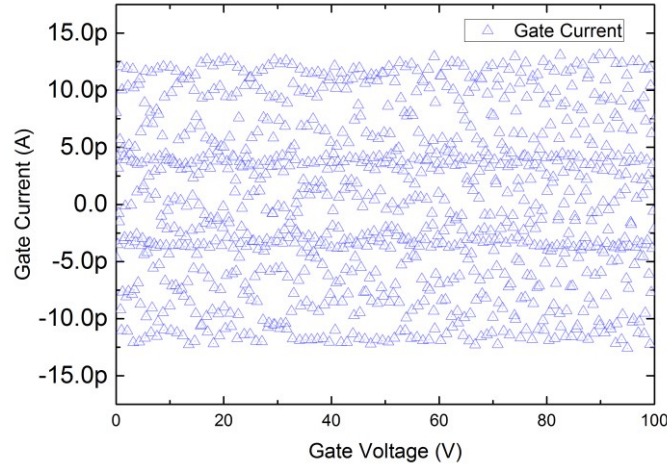


Figure 4-18 Noise level measurement

All tested devices in this chapter have the same beam length of $28\text{ }\mu\text{m}$, g_{GB} of 150nm and g_{DB} of 100nm . Two gate terminals on the same side of the beam have a width of $13.4\text{ }\mu\text{m}$. The width of drain terminal is $1\text{ }\mu\text{m}$ and the gap between gate and drain terminals is 100 nm . As described in the earlier section, 100 nm gap between different terminals is the smallest value we can achieve so far.

A few devices are tested at room temperature to obtain the pull in and pull out voltage by voltage sweep on gate terminals. The devices with 300nm , 400nm , 500nm , 600nm and 700nm beam width ($200\text{nm}\sim 600\text{nm}$ initial trench width) show average measured pull-in voltage of 8.1V , 11.9V , 15.7V , 21.4V and 25.6V (Figure 4-16). The measured pull-in voltage has good agreement to value derived by the analytical model except for the smallest width case.

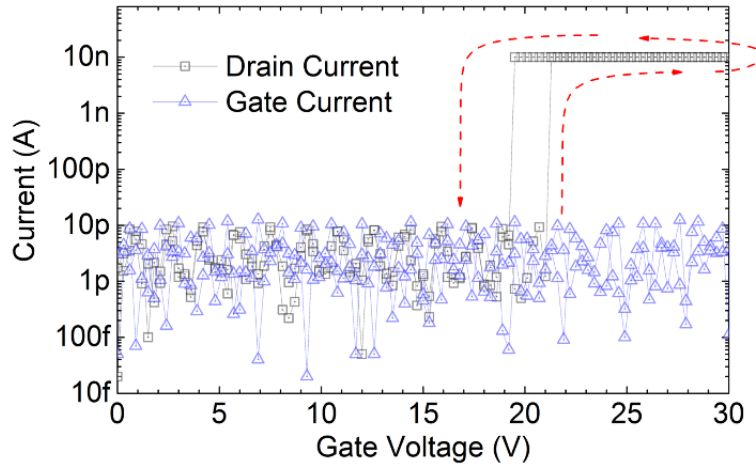


Figure 4-19 Double side I-V sweep for a NEMS switch with dimension: $g_{GB} = 150\text{nm}$, $g_{DB} = 100\text{nm}$, $w = 600\text{nm}$, $L_B = 28\text{ }\mu\text{m}$. Current displaced in the figures uses absolute value.

One typical I-V sweep is shown in Figure 4-19. The tested device has an initial trench of 500nm, after the wet etch process, the width of the beam is extended to 600nm. I-V sweep is performed from 0 to 30V and a reverse sweep of 30-0V is also performed to examine the hysteresis behavior. The device is suddenly turned on at 21.3V, and the drain current is changed straightly from the noise level to the current compliance. For reverse sweep from 30V to 0V, the device is pulled-out at 19.2V, and drain current jumps directly from current compliance to noise level. The gate current is below noise level all time. Similar abrupt switching behavior can also be observed from other devices tested.

4.5 Electrical Measurement with High Current

Device with $L_B = 28\text{ }\mu\text{m}$, $t = 700\text{ nm}$ and $g_{GB} = 150\text{ nm}$ is measured for high contact current as well as contact resistance. It is first tested for double side I-V sweep with 500 nA current compliance. General NEMS switch behaviors, including abrupt switching, zero off-state current and hysteresis behavior can

be found in Figure 4-20. The pull-in voltage of this device is recorded at 27.8V.

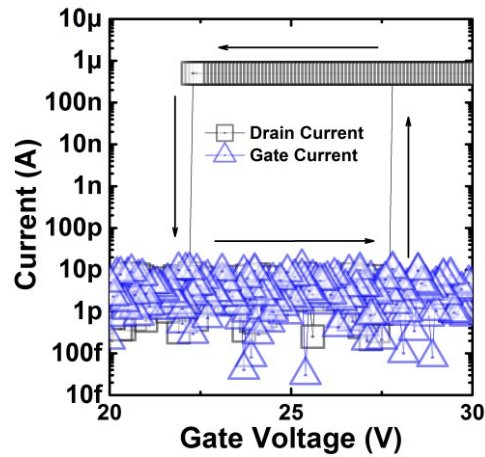


Figure 4-20 I-V sweep with 500nA current compliance.

The contact resistance of this device is also measured with 0.1V constant voltage at the drain terminal. The current compliance is removed and a cycling test is performed to monitor the contact resistance change over different cycles. Figure 4-21 shows in the initial cycle, the contact resistance is around 2.5 k Ω with 28.5 V gate bias, indicating a good metal to metal contact.

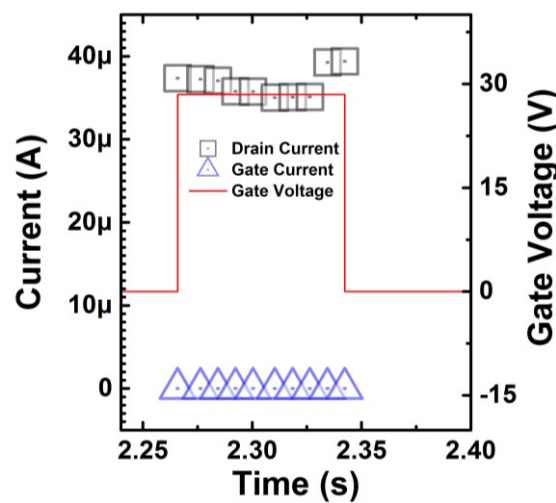


Figure 4-21 First cycle to obtain contact resistance.

Figure 4-22 reflects the contact resistance measured at every cycle. For the first 100 cycles, the gate voltage is set to be 28.5 V, the same as the measurement in Figure 4-21.

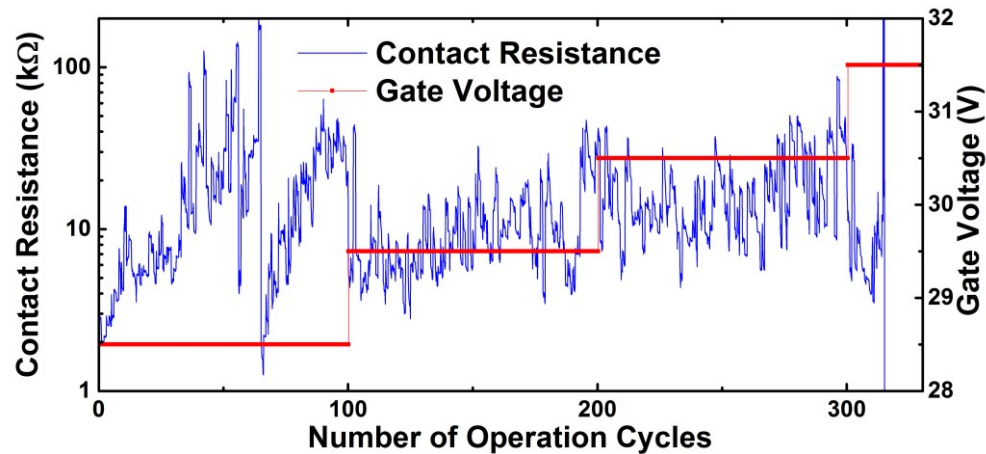


Figure 4-22 Contact resistance change over the cycling test.

The contact resistance gradually increases and suddenly drops in the 56th cycle, and again the resistance increases afterward. This large change over different cycles indicates the effective contact surface varies over the cycles.

Then the gate voltage is increased to 29.5V and 30.5V. A larger gate voltage seems to help to stabilize the contact resistance. It has an initial drop after voltage increases, and later it stays at 5~20kΩ.

After increasing the voltage to 31.5V, the beam collapse on the gate terminal, causing gate to beam shortage which cannot be recovered afterward. The measurement indicates that a higher gate voltage helps to stabilize the contact resistance, but further improvement should be done by proper surface coating.

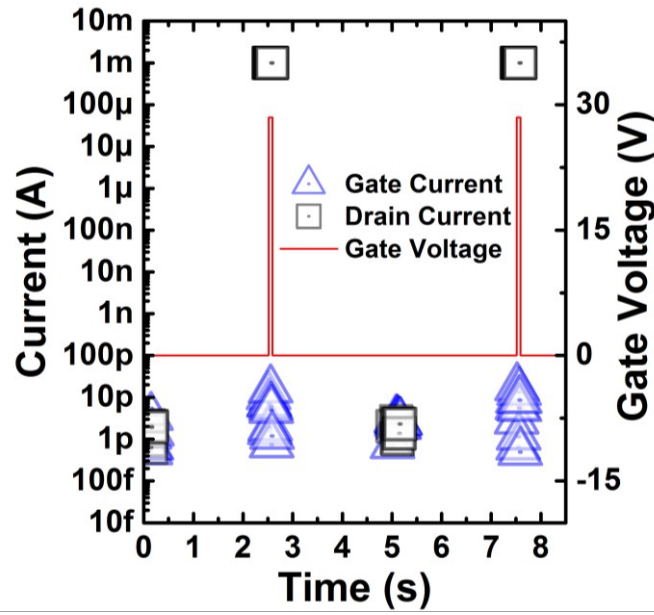


Figure 4-23 Electrical tests for a fixed-fixed beam device with dimension of $L_B=28\mu\text{m}$, $t=700\text{ nm}$ and $g_{GB}=150\text{ nm}$ Cycling test with 1mA current applied on drain terminal.

Afterward, higher current handling in the drain terminal is tested, and an exceptionally high current of 1 mA is applied with a 5s interval. The device shows a stable electrical performance in Figure 4-23 with an on/off ratio of 10^8 .

4.6 High Temperature Measurement

Then the devices are heated to 300 °C in vacuum chamber and kept for half an hour till the temperature is stabilized for high temperature test. The smallest device with 300nm beam width ($L_B=28\mu\text{m}$, $t=300\text{ nm}$ and $g_{GB}=150\text{ nm}$) is used to obtain the endurance data.

The cycling test is performed with the following method. The devices will be set to on-state and off-state repeatedly by pulling in and releasing the beam. With the pull-in voltage obtained at room temperature, the on-state gate

voltage is set to be 9V. For every 5.2s, the gate terminals are applied with a voltage at 9V to pull in the beam. The drain terminal is kept with a bias voltage of 1V.

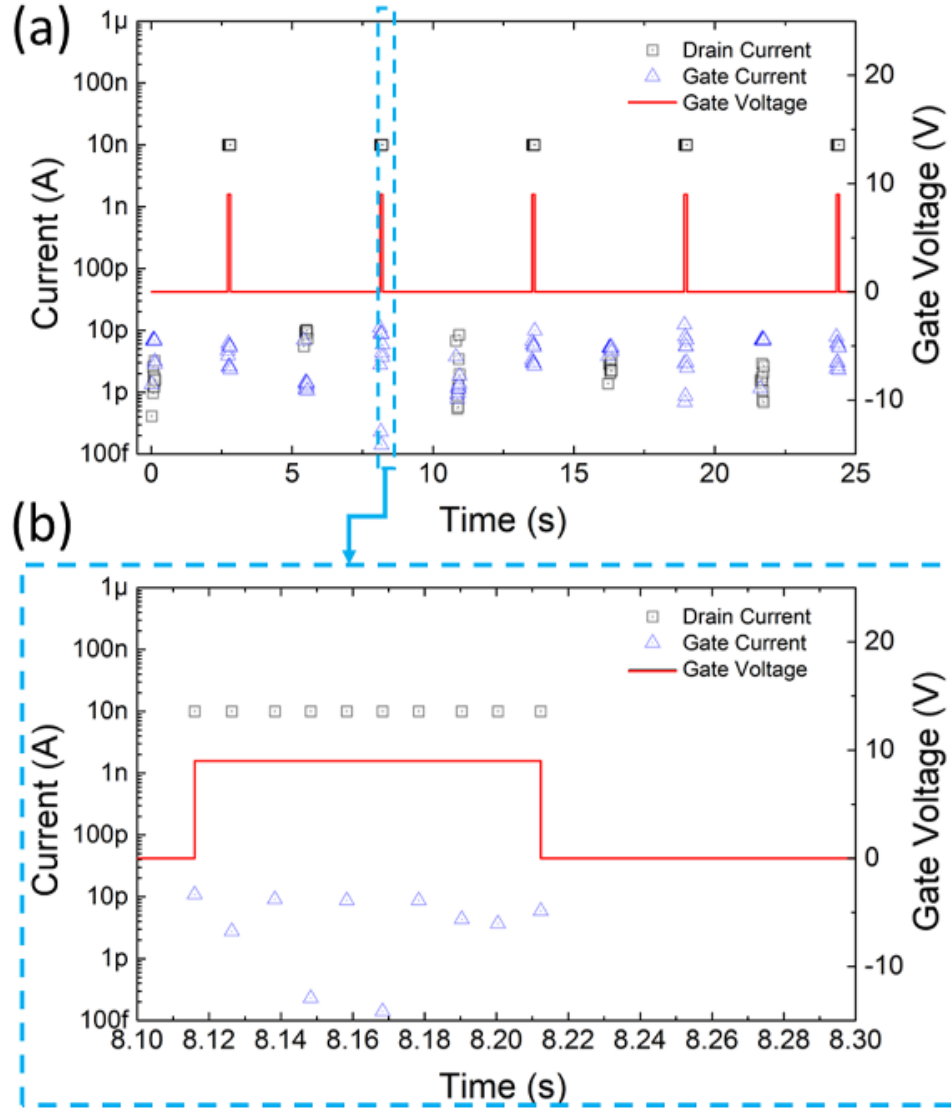


Figure 4-24 (a) First 25s of cycling test at 300 °C, (b) zoom-in view from 8.1s to 8.3s of the cycling test. Current displacement in the figures uses absolute value.

The gate voltage will be held for 120ms and totally 10 data points of measured current are recorded from every terminal. Then the gate voltage is set to 0V and the elastic restoring force pulls back the NEMS switch. Approximately 2.6s after the pull-in, another off-state measurement would be

performed; similarly 10 data points are monitored when the gate voltage is 0V. The drain voltage would remain at 1V in this case. The on-state drain current should hit the current compliance, indicating a good mechanical contact. All the other currents recorded should be below noise level, as they are off-state drain current or gate current. Figure 4-24 shows data recorded in the first few cycles.

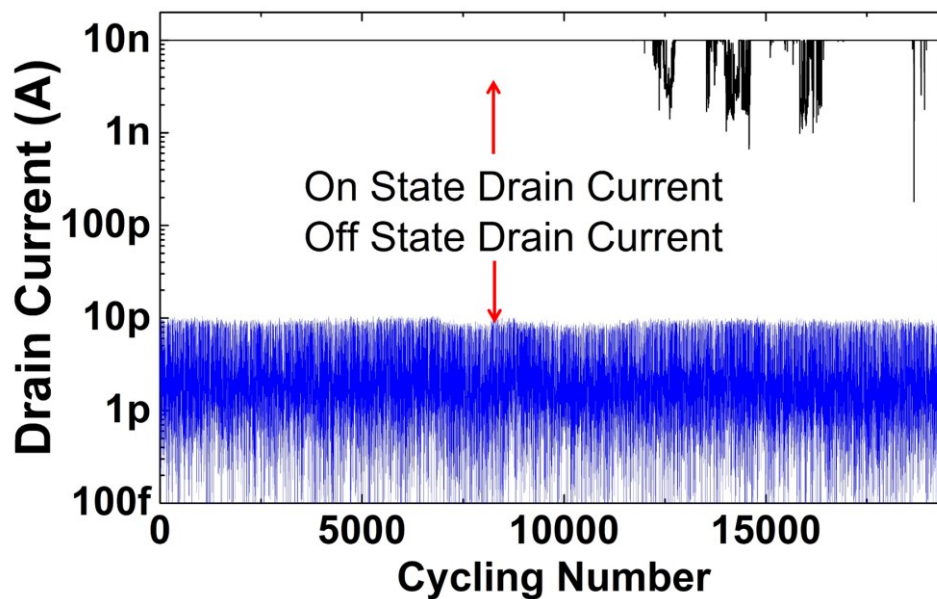


Figure 4-25 Cycling test data of drain current recorded at 300 °C.

Since testing is significantly slow at ~5 second per on/off cycle, only 20,000 cycles can be practically captured. The whole measurement lasts for more than 28 hours. Every point of data is carefully examined to check the on state and off state drain current. As shown in Figure 4-25, the off-state drain current is kept at a noise level below 10pA and with an average of 2.8 pA (absolute current value is used to calculate the average number).

In Figure 4-26 and Figure 4-27, either on-state or off-state, the gate current is kept at the noise level, while there is a subtle difference between on-state

gate current and off-state gate current. The average on-state gate current is 5.0 pA, and the off-state gate current is 2.7 pA.

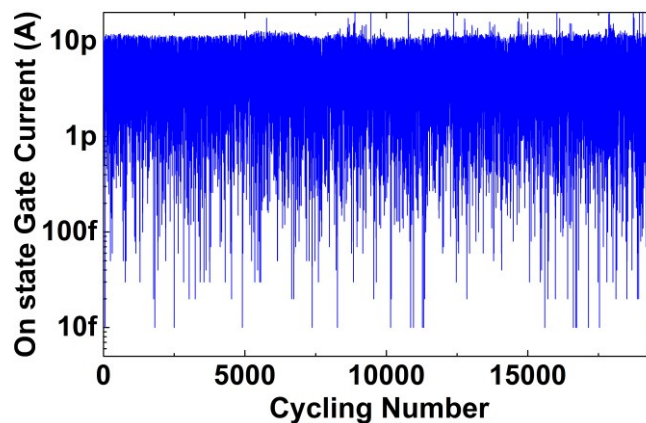


Figure 4-26 Cycling test data of on state gate current recorded at 300 °C.

It suggests a minor leakage current between gate terminal and source terminal may exist. Since all the data is very close to the noise level, we could not determine the accurate tunneling current.

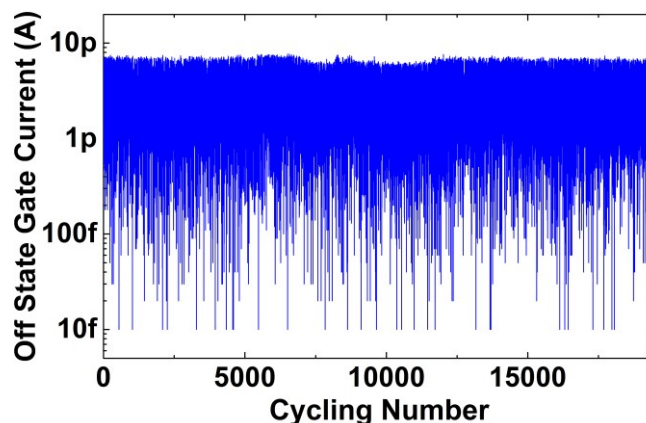


Figure 4-27 Cycling test data of off state gate current recorded at 300 °C.

The on-state current hits the 10nA compliance during the first 10,000 cycles. In the second half the cycling test, the drain current appears to have data points smaller than 10nA, which indicates the contact is degraded after 10,000 cycles. High contact resistance can be expected in these cycles.

This phenomenon does not happen in every cycle. 11.8% of the 10,000 cycles appears to have at least one data point cannot hit the current compliance. It suggests the contact surface experience material transfer or deformation throughout the cycling test. The gate voltage applied during the cycling test is not high enough to form a low resistance contact when the contact surface is not smooth. However, for each cycle, the on-state current is still several orders larger than off-state current.

After 20,000 cycles, an I-V sweep is performed for the device, the data can be found in Figure 4-28. The device still holds its noise-level off-state current, in drain terminal and gate terminals. The subthreshold swing is only 2.5mV/dec.

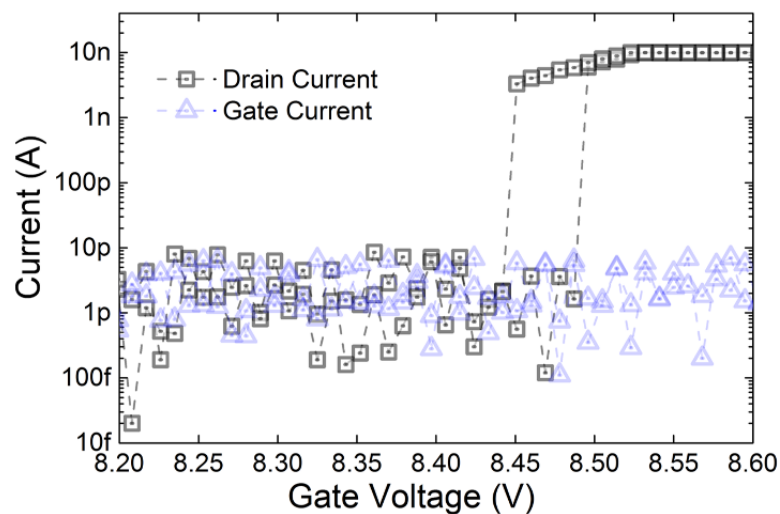


Figure 4-28 I-V sweep performed after cycling test at 300 °C. Current displacement in the figures uses absolute value. Drain terminal voltage is 1V during this measurement.

The I-V sweep also shows the device cannot reach the current compliance right after pull-in, so that a slightly higher voltage is needed for better contact. This behavior is also consistent with the low on-state drain current in the second half of the cycling test. However, the device still keeps the critical

properties for NEMS switch after 20,000 cycles of high temperature cycling testing. Two possible ways to obtain stable and low contact resistance devices are using harder material such as tungsten to prevent contact degradation or introducing compliant contact to increase effective contact surface area.

Similar cycling test has also been performed at room temperature for the devices with same dimensions and also from the same wafer. The purpose of the test is to compare the leakage current between room temperature and high temperature.

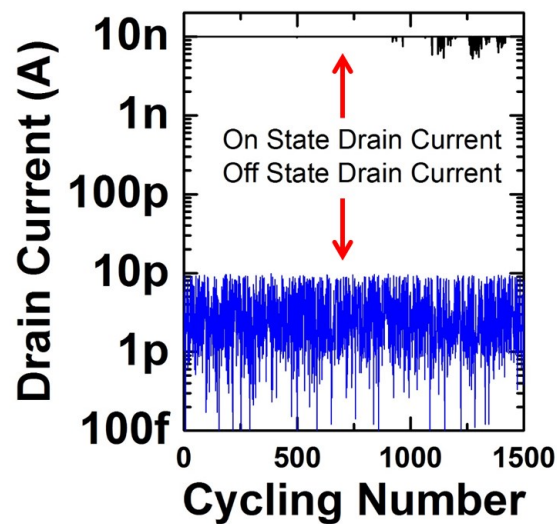


Figure 4-29 Cycling test data of drain current recorded at room temperature.

Thus 1500 cycles have been performed. The off-state drain current (*Figure 4-29*), on-state gate current (*Figure 4-30 (a)*), off-state gate current (*Figure 4-30 (b)*) are measured. The average off-state current is very close to 300 °C measurement of 3.4 pA, 8.1pA and 3.5pA, respectively.

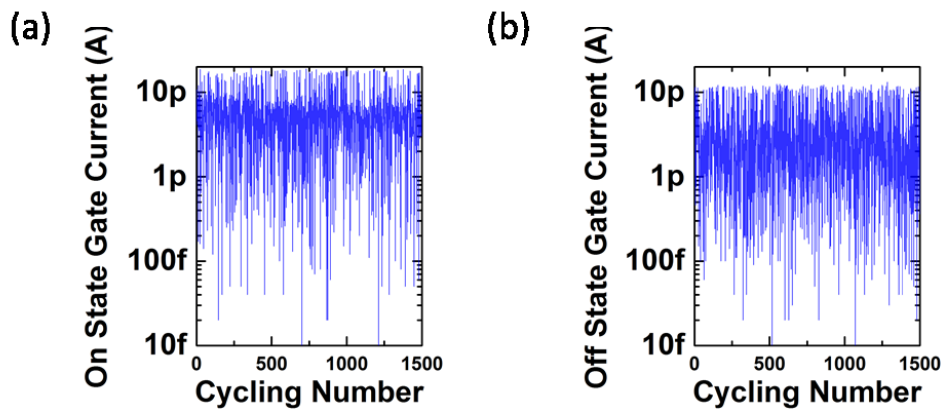


Figure 4-30 Cycling test data of (a) on state gate current, (b) off state gate current recorded for room temperature.

The leakage current data indicate off-state current will not be influenced by the temperature up to 300 °C. We also notice this device appears to have high contact resistance phenomenon at around 1000 cycles which indicates device reliability might be better at higher temperature.

This phenomenon possibly comes from the following two points: 300 °C is not high enough to obviously affect the mechanical properties of the NEMS switches, while the moisture and contaminations absorbed on the contact surface before measurement can be gradually removed during the high temperature testing process, under continuously baking at 300 °C. As a result, the NEMS switches with cleaner contact surface have shown better performance at 300 °C than at room temperature.

A few devices are also examined in the SEM after they cycled until a low on-state drain current level (<10 nA), but the contact surface in these devices remains smooth (Figure 4-31). We suspect the defect on contact surface is smaller than the resolution of SEM, and more refined tools like transmission

electron microscopy may help to reveal the reason of large contact resistance during cycling.

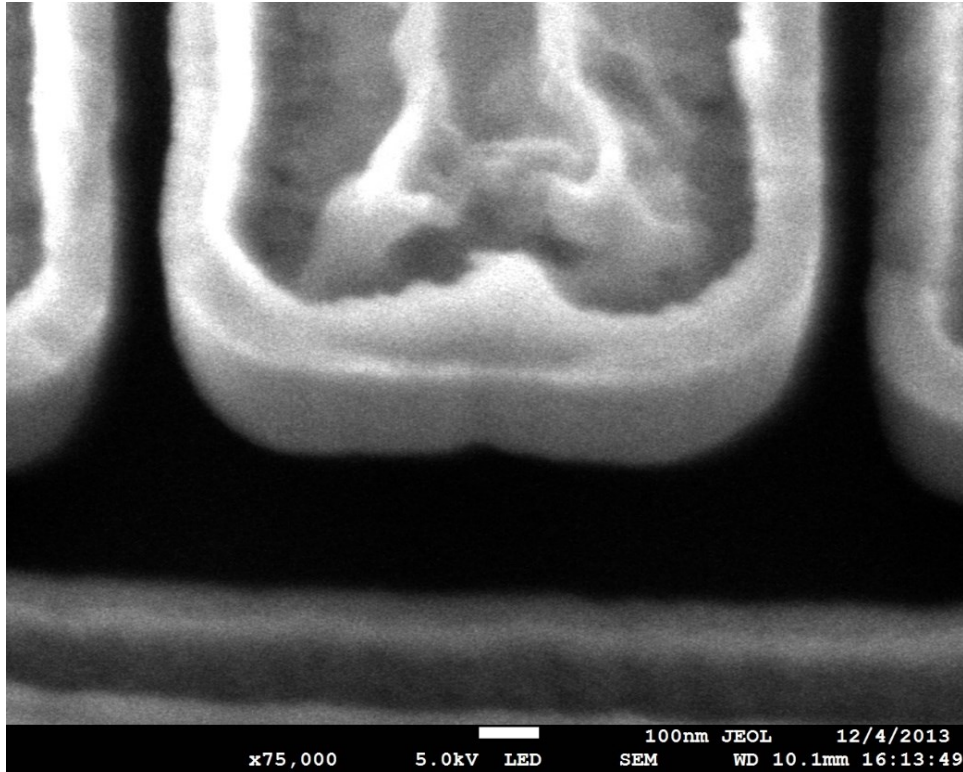


Figure 4-31 Drain contact area after cycling test, the beam is attracted by electron charging to another side

4.7 Conclusion

An all Mo based NEMS switch has been fabricated using a one mask process. The Damascene-like process is designed to ensure a clean, high aspect ratio, metal-to-metal mechanical contact. With no polymer or any other etching residual existing on the etching surface, the electrical performance is largely enhanced.

The I-V sweep has been done for devices with different width. The measured pull-in voltages fit with analytic prediction. The devices show an

abrupt switching behavior with 10^8 on/off ratio. The contact resistance is recorded at 2.5 k Ω . Very high current of 1 mA is able to pass through the very limited contact area. Cycling test at 300 °C and room temperature for the smallest width devices is performed to examine the endurance of the device. The devices work reliably for 28 hours, 20,000 cycles at 300 °C vacuum environment without failure and measurable leakage current.

Although metal based NEMS switch shows clear advantages of low contact resistance and low temperature process, due to the difficulties of fabrication, only limited reports have been published. Table 4-2 shows the comparison of recent reported metal based NEMS switch. Our Mo-based devices show not only great advantages in high reliability and low contact resistance, it is also the only reported case working under high temperature.

Table 4-2 Comparison of metal based NEMS switch

Reference	Contact material	Cycles	Contact Resistance	Operating temperature
[119]	TiN	500	No record	Room temperature
[206]	TiN-W	20	No record	Room temperature
[204]	Pt	8	10 M Ω	Room temperature
[229]	TiN	9	~100 M Ω	Room temperature
[230]	W	20	~ 100 M Ω	Room temperature
This work	Mo	>20,000	2.5 k Ω	300 °C

Chapter 5 Dimension Optimization of All Metal Based NEMS Switches

As discussed in the section 1.6, the implements of N/MEMS rely on multiple devices working at the same time. Therefore, the process yield is extremely important for N/MEMS switches. Unfortunately, yield of processes has not been addressed by recent studies [112, 228, 231]. Most of the studies only show the performance of a single device. The only data reported for the yield of NEMS switches in [213] is merely 1.5%. Lack of stable fabrication process becomes the major hurdle of accumulating more knowledge on NEMS switches.

In this chapter, the pull-in voltage and process yield of the prototype devices discussed in chapter 4 has been studied with various dimensions. Totally 800 switches have been characterized. With the help of Damascene-like process established in the last chapter, device optimization can be carried out. The pull-in voltages are measured and compared to the FEM modeling as well as analytical solution. The deviation between measured voltage and estimated value are identified. It also includes a basic method for NEMS switch designers to quickly identify the pull-in voltage. By examining the dimensions with close to 100% yield, optimizations are performed with a general rule of high process successful rate deducted. The failure mode of other dimensions is also concluded for future references. With this knowledge, future designs of NEMS switches can avoid the common failures.

5.1 Dimensions

Statistical measurements of pull-in voltage and process yield has been carried out by measuring 800 devices, which includes 500 fixed-fixed beam NEMS switches (50 different dimensions) and 300 cantilever beam switches (30 different dimension). The dimensions we focus on are mainly the length of beam L_B , the width of the beam t , and the gap the switches g_{GB} and g_{DB} as shown in Figure 5-1.

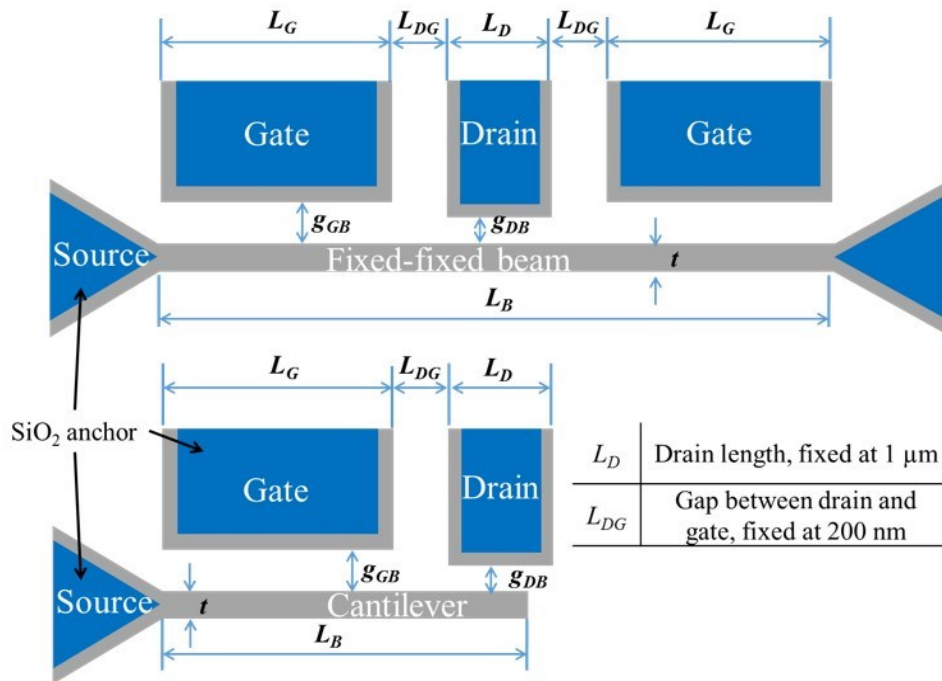


Figure 5-1 Schematic drawing of a fixed-fixed beam switch and a cantilever switch

These 800 devices are picked from 5 different chips across the same wafer. Every chip contains two devices with identical dimension. Only two most important factors, beam length and beam thickness vary, while other parameters are fixed.

Table 5-1 Design Parameter

	Quantity	Design Value
<i>Fixed-fixed beam</i>	Beam length, L_B	28 μm , 32 μm , 40 μm , 60 μm , 100 μm
	Beam width, t	300 nm, 400 nm, 500 nm, 600 nm, 700 nm
	Gap, (g_{GB} , g_{DB})	(150 nm, 100 nm), (200 nm, 150 nm)
<i>cantilever</i>	Beam length, L_B	12 μm , 14 μm , 16 μm , 20 μm , 30 μm , 50 μm
	Beam width, t	300 nm, 400 nm, 500 nm, 600 nm, 700 nm
	Gap, (g_{DB} , g_{GB})	(150 nm, 100 nm)

All parameter combinations shown in Table 5-1 are studied. Furthermore, for the fixed-fixed beam, two additional parameters, the actuation gap, g_{GB} , and the contact gap, g_{DB} , are also studied with two combinations. The selection of these dimensions is based on the following considerations. The beam length and beam thickness should cover a wide range. However, more dimensions of the shorter beam length are studied, as the very long beam is expected to have some stiction on the contact due to their low spring constants. The gap of the devices doesn't include a lot of combinations as usually it is decided by the critical dimension of the photolithography tool.

5.2 Pull-In Voltage

Before electrical measurement, analytical solution and finite element modeling are performed to estimate the pull-in voltage for each dimension. With simple parallel-plate model, pull-in voltage of NEMS switch in vacuum is:

$$V_{pi} = \sqrt{\frac{8k_{eff}g_{GB}^3}{27\varepsilon_0 L_B w}} \quad (5-1)$$

where w is the thickness of the beam. ε_0 is the permittivity of the vacuum. k_{eff} is the effective spring constant of the beam, which is related to beam type and the electrostatic force distribution along the beam. For a more accurate k_{eff} , we consider the drain voltage is normally much smaller than the gate voltage, with no electrostatics force from drain terminal contributed to the pull-in. For fixed-fixed beam cases, the electrostatic force is missing in the middle of the beam. Thereby, the effective spring constant of the fixed-fixed beam is given by:

$$k_{eff} = \frac{4Ewt^3}{L_G^2(L_B - L_G)} \quad (5-2)$$

where E is the Young's module of Mo.

The pull-in voltage of fixed-fixed beam is given by:

$$V_{pi} = \sqrt{\frac{32Et^3g_{GB}^3}{27\varepsilon_0L_G^2L_B(L_B - L_G)}} \quad (5-3)$$

Similarly, for cantilever case, we consider no electrostatic force at the tip of the beam:

$$k_{eff} = \frac{2Ewt^3}{L_G^2(4L_B - L_G)} \quad (5-4)$$

The pull-in voltage is given by:

$$V_{pi} = \sqrt{\frac{16Et^3g_{GB}^3}{27\varepsilon_0L_G^2L_B(4L_B - L_G)}} \quad (5-5)$$

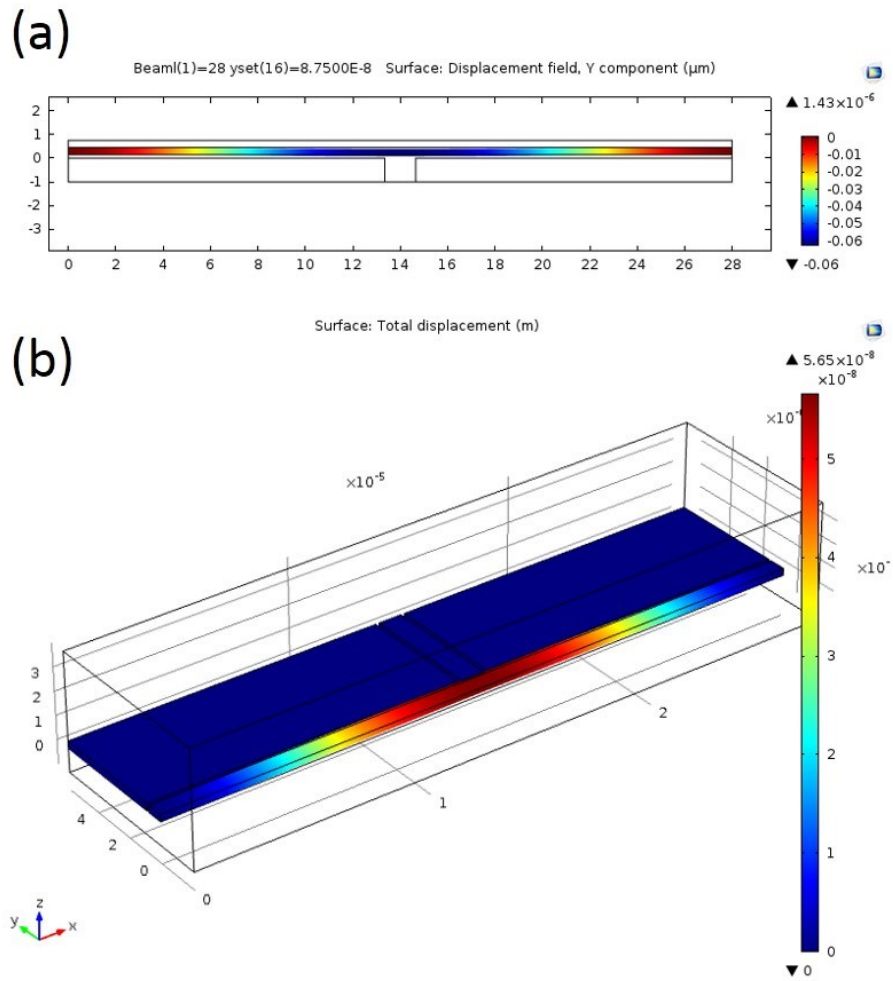


Figure 5-2 (a) 2D simulation of a fixed-fixed beam NEMS switch. (b) 3D simulation of a fixed-fixed beam NEMS switch.

Notice the structure layer thickness has been cancelled during the calculation, therefore it does not have an impact on the pull-in voltage in this model. There are a lot of assumptions for the parallel-plate model: considering the beam has a linear spring constant, a piston-like motion where the pull-in always occurs when deformation reaches one-third of the actuation gap; Furthermore, no fringing field is taken into account. 2D and 3D FEM modeling are performed for higher accuracy, using COMSOL Multiphysics tool [189] as shown in Figure 5-2. During the simulation, a voltage difference is applied between the two gate electrode and the beam. The voltage is

increased from 0V to calculate the deformation of the switch at each voltage, until a voltage where no converged solution can be found. At this voltage, the beam collapsed on the drain terminal, and we call it pull-in voltage.

The 2D model covers a very wide range of dimension, and we only did 3D simulations of the dimensions shown in Table II. The simulation sweeps the voltage from a smaller guessed value until convergence failure near the pull-in, and then this voltage is recorded as pull-in voltage. The simulation generally takes quite a lot of computational cost, as one 2D simulation takes a few minutes and 3D simulation needs few tens of minutes using a state-of-art workstation.

The simulation results have been plotted in Figure 5-3, Figure 5-4 and Figure 5-5. Figure 5-3 is fixed-fixed beam device with $g_{DB}=100$ nm, $g_{GB}=150$ nm. Figure 5-4 is also fixed-fixed beam device, but with $g_{DB}=150$ nm, $g_{GB}=200$ nm, Figure 5-5 is the cantilever device with $g_{DB}=100$ nm, $g_{GB}=150$ nm. The 3D simulation results are typically 10% lower than the 2D simulation, which is most likely caused by the fringing field out-of-plane. Although so many assumptions are applied to the analytical solution, it appears that by simply adding a constant coefficient to equation (5-3) and (5-5), the analytical solution would fit the 2D simulation very well.

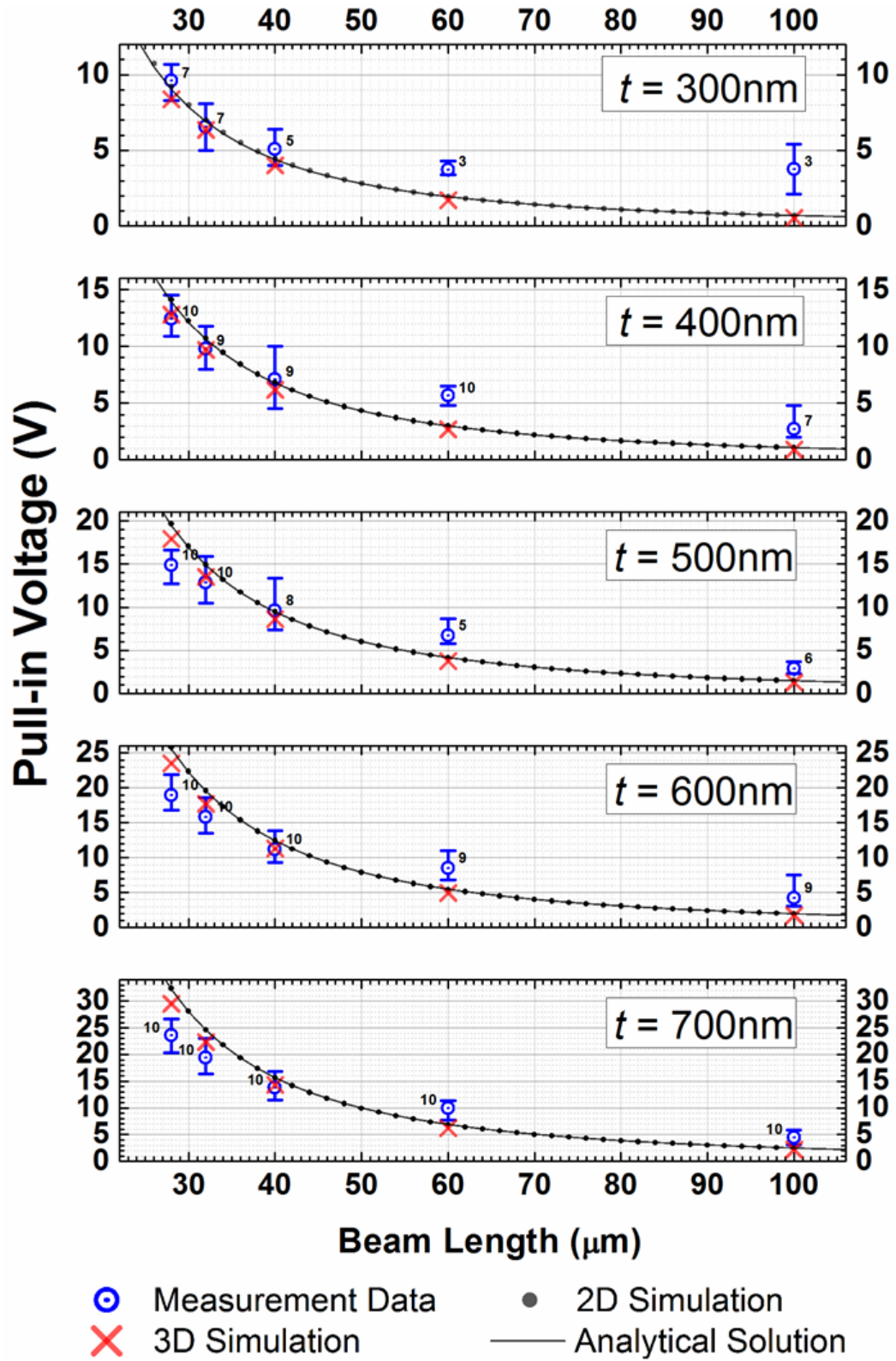


Figure 5-3 Pull-in voltage summary of fixed-fixed beam devices with $g_{GB} = 150$ nm, and $g_{DB} = 100$ nm, with beam length L_B , beam width t varies.

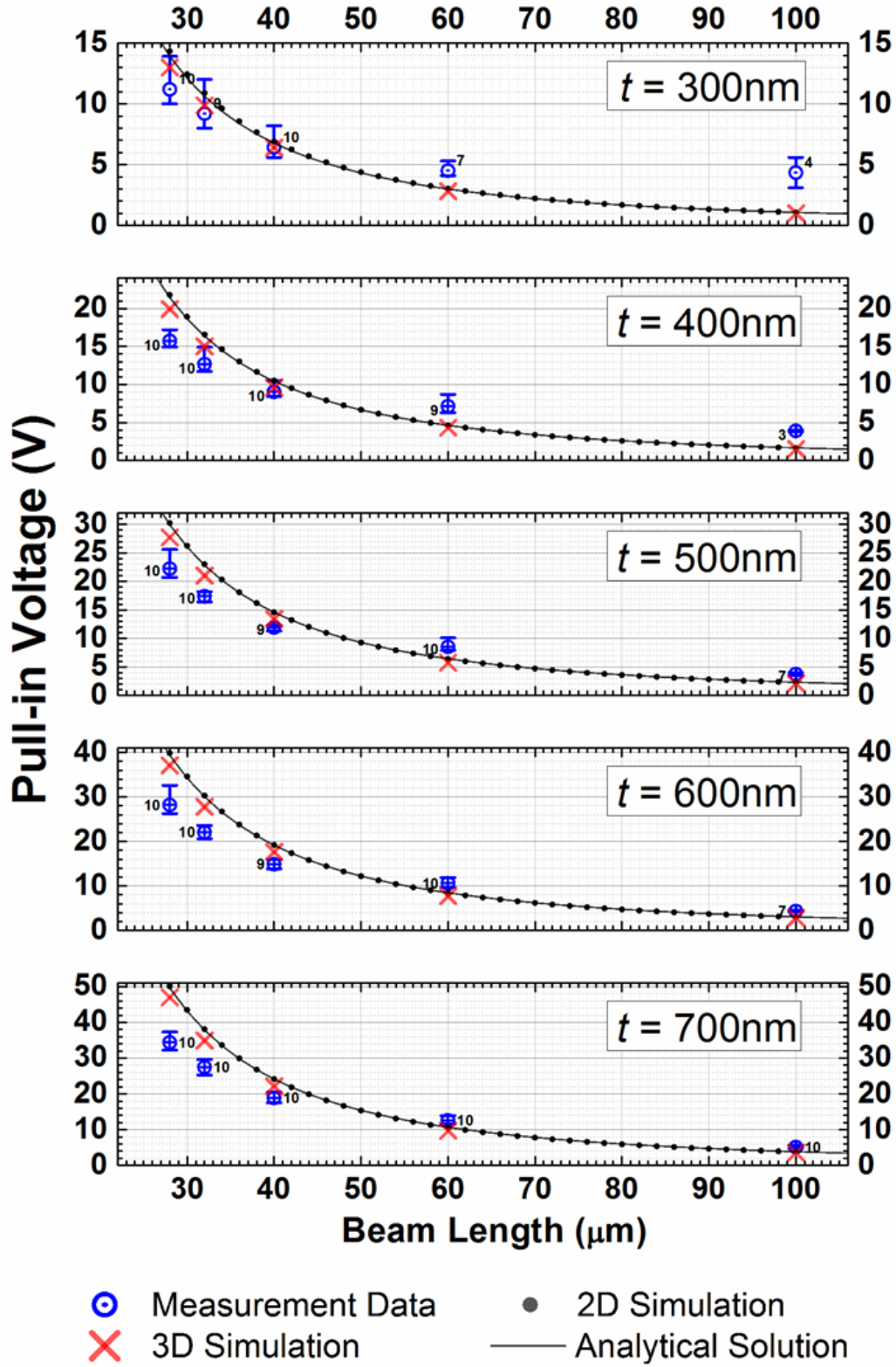


Figure 5-4 Pull-in voltage summary of fixed-fixed beam devices with $g_{GB} = 200$ nm, and $g_{DB} = 150$ nm, with beam length L_B , beam width t varies.

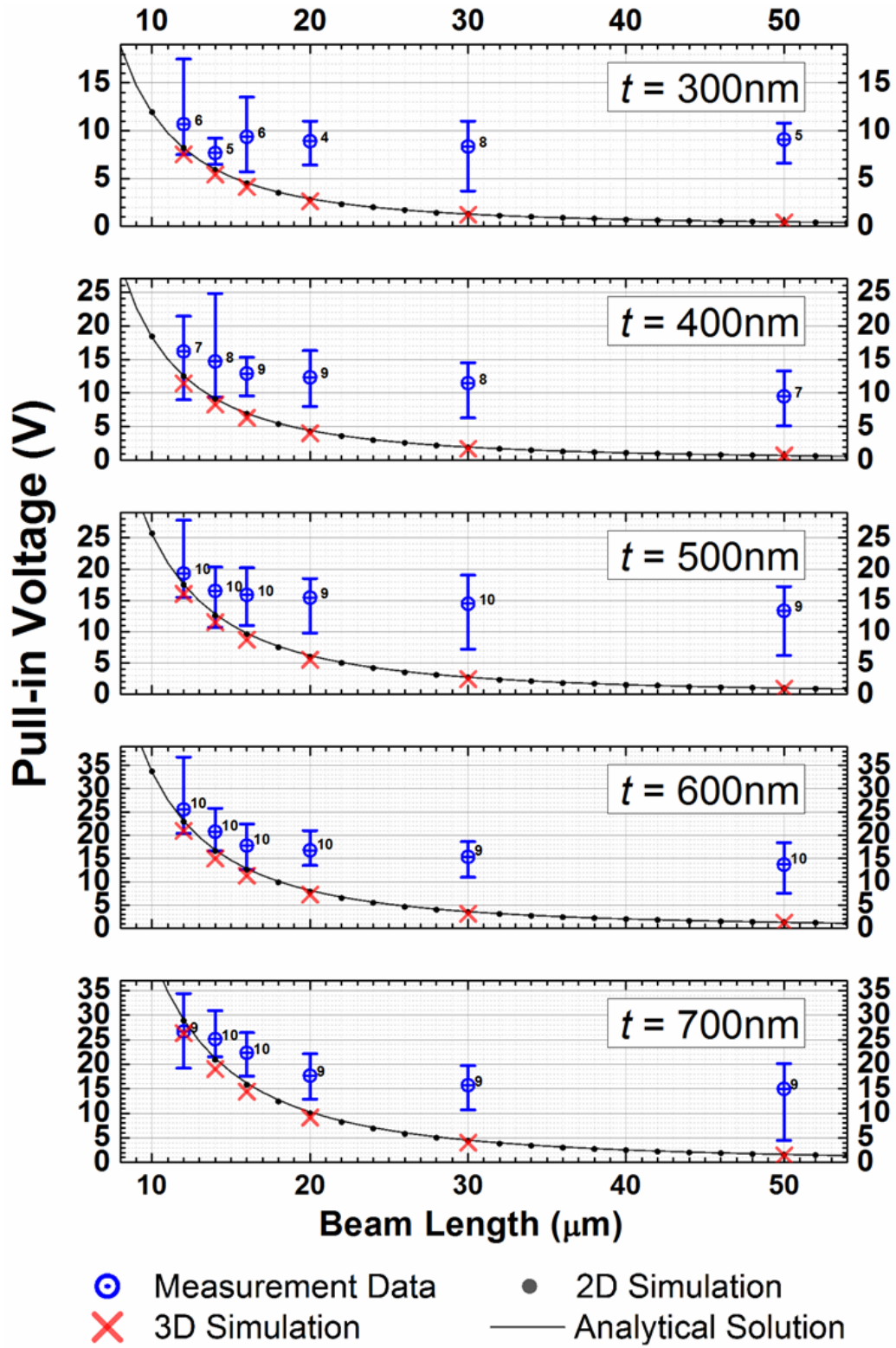


Figure 5-5 Pull-in voltage summary of cantilever beam devices with $g_{GB} = 150$ nm, and $g_{DB} = 100$ nm, with beam length L_B , beam width t varies.

For fixed-fixed beam:

$$V_{pi} = a_{ff} \sqrt{\frac{32Et^3 g_{GB}^3}{27\epsilon_0 L_G^2 L_B (L_B - L_G)}} \quad (5-6)$$

For cantilever beam:

$$V_{pi} = a_c \sqrt{\frac{16Et^3 g_{GB}^3}{27\epsilon_0 L_G^2 L_B (4L_B - L_G)}} \quad (5-7)$$

By assigning $a_{ff} = 1.26$ and $a_c = 1.4$, the deviation between analytical solution and 2D simulation is only $\pm 2\%$ for fixed-fixed beam and $\pm 4.5\%$ for cantilever across the whole simulation range. For 3D simulation cases, assigning $a_{ff} = 1.2$ and $a_c = 1.3$, the deviation is still up to 10% in some cases. The accuracy of the analytical model is higher when L_B/t is smaller than 70, with $\pm 4\%$ for fixed-fixed beam and $\pm 5\%$ for cantilevers. Although the equation is constrained to a limited range, it is still acceptable as very high beam length to width ratio is not desired in actual design, which will be discussed later.

With the prediction of the pull-in voltage, 800 devices are measured individually in vacuum. The procedures are as follows: an I-V sweep starts from 0V with a 0.1V step. 10 nA compliance is given to each terminal. Current from every terminal is monitored. Once pull-in phenomenon is observed, the I-V sweep would be terminated manually, and typically the device would be overdriven for 1V. Based on the measurement, we can classify the 800 measurements into 6 different categories below:

- i. Repeatable devices: after the I-V sweep, a repeatable device shows beam current and drain current in the opposite direction. The gate current keeps at noise level as shown in *Figure 5-6 (a)*. A quick cycling test for a few tens of cycles shown in *Figure 5-6 (b)* verifies the repeatability.
- ii. Gate to beam pull-in: in I-V sweep, the gate current raises at the same time with the beam current or drain current shown in *Figure 5-6 (c)*, and no cycling behavior can be observed in these devices.
- iii. Secondary pull-in: in the I-V sweep, the devices behave like the repeatable devices at first, but it quickly shows gate to beam pull-in right after the first pull-in as shown in *Figure 5-6 (d)*.
- iv. Stiction: in I-V sweep, the signal is identical to the repeatable devices shown in *Figure 5-6 (e)*. But in the following cycling measurement and I-V sweep as shown in *Figure 5-6 (f)*, the device has a constant current between drain and beam even with 0V gate voltage.
- v. Short circuit: in I-V sweep, the drain current and beam current appear from the beginning of the sweep.
- vi. No signal: even after very large voltage overdrive, there is no current observed in any of the terminals.

Detail causes of the failure will be discussed later. We focus on the pull-in voltage analysis first. In the above 6 cases, pull-in voltage can be obtained from case 1 to case 4. All pull-in voltage data have been plotted in *Figure 5-3*, *Figure 5-4* and *Figure 5-5*, the number besides the measurement data show the quantity of the data.

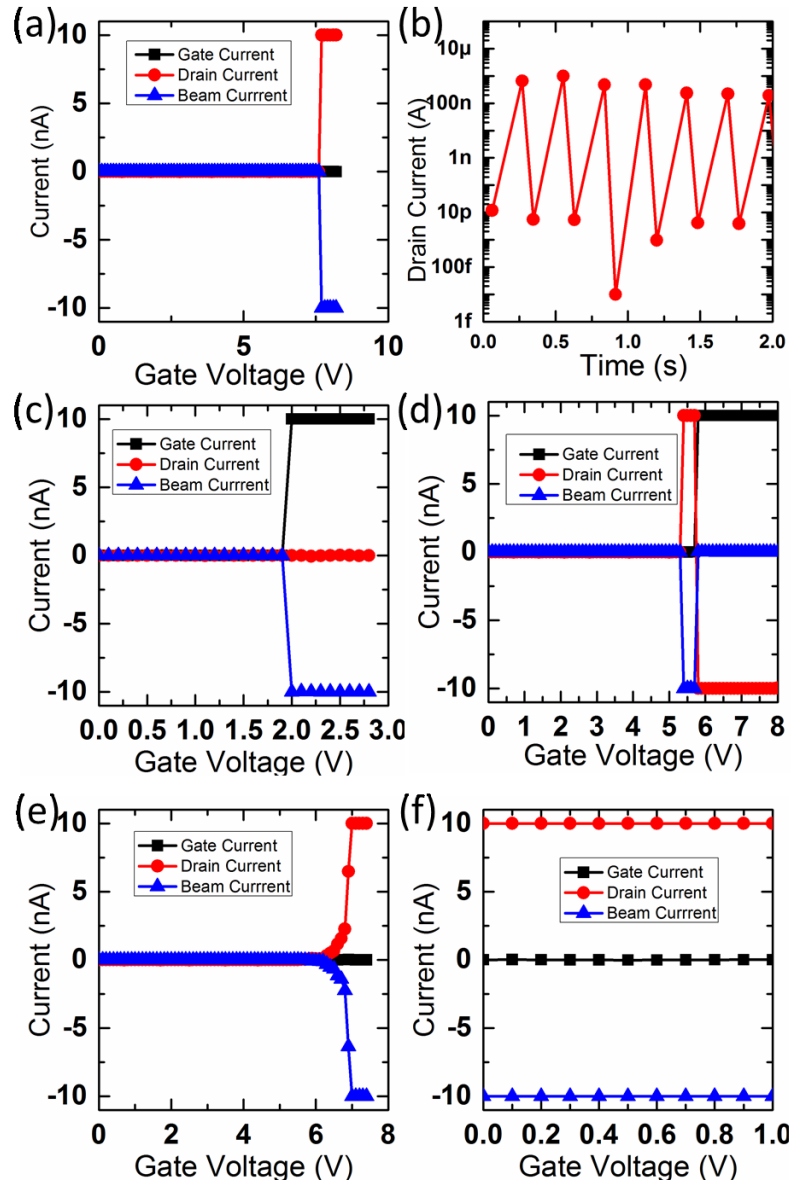


Figure 5-6 (a) I-V curve of a repeatable device (b) cycling measurement of a repeatable device. (c) I-V curve of a gate to beam pull-in device. (d) I-V curve of a device to secondary pull-in. (e) First round I-V curve of a device with stiction (f) Second round I-V curve of a device with stiction

Generally the measured pull-in voltages for fixed-fixed beam NEMS switches are smaller than simulation when beam length is smaller than $60\text{ }\mu\text{m}$. In Figure 4-11, an extra sidewall exists on every edge, which will induce an extra electrostatic force. On the other hand, when the beam length is larger than $60\text{ }\mu\text{m}$, the pull-in voltage is much higher than expected.

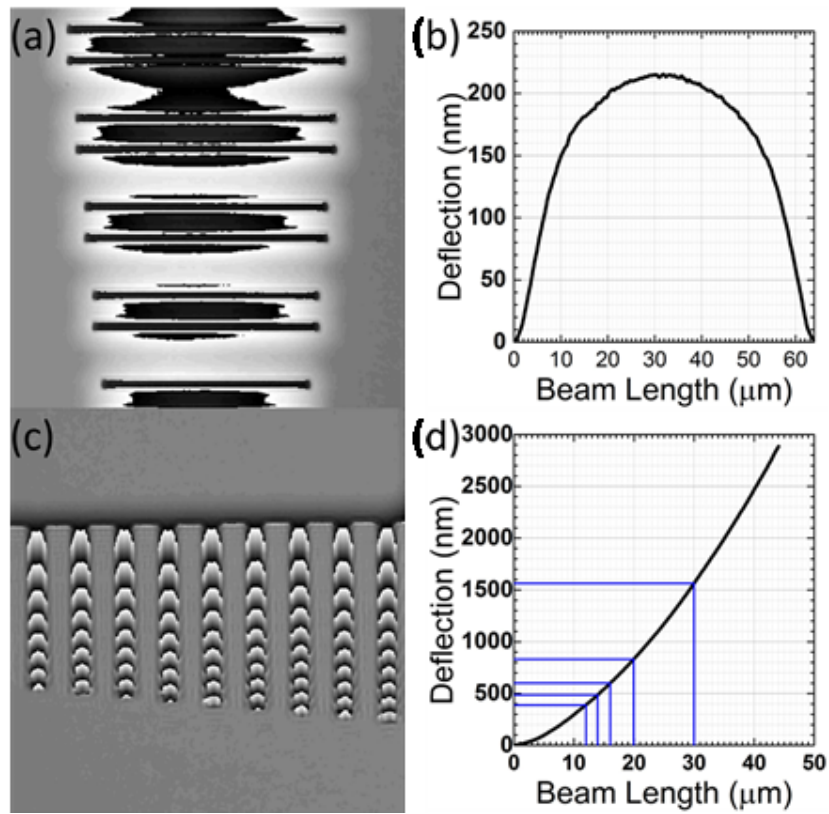


Figure 5-7 (a) The phase pattern of the fixed-fixed beams. (b) Beam deflection of a 60 μm fixed-fixed beam. (c) The phase pattern of cantilever beams (d) beam deflection of a 50 μm cantilever.

The test structure is examined under a holographic microscope (Lyncee Tec, DHM-R2200). The phase pattern can be found in *Figure 5-7(a)*. For a 60 μm fixed-fixed beam, the maximum deflection in the middle is about 220nm as shown in *Figure 5-7 (b)*, therefore, the effective capacitance between gate terminal and beam terminal is much smaller.

For cantilever case, the problem become severe (*Figure 5-7 (c)*): the test structure has a deflection of more than 300 nm at the point which is 12 μm from the anchor as shown in *Figure 5-7 (d)*. As a result, only the first 12 μm near the anchor is effectively used for electrostatic actuation, and thus the mean value of the pull-in voltage does not decrease when the beam length increases from 12 μm to 50 μm . The pull-in voltage cover quite a wide range

as the beam deflection varies across different positions of the wafer. We do observe that some devices have drain to beam contact even when the beam length is very long, which indicates that in some area the bending is much smaller.

The deflection is induced by the stress gradient of the film deposited. We found even after thermal annealing, excimer laser annealing and Ar plasma treating, no uniform control effect on the deflection is achieved. Nonetheless, if we can maintain the film thickness and keep scaling down all the other dimensions, the deformation can be confined to an acceptable level. Fixed-fixed beam with less than 40 μm beam length is preferable. For cantilever, the length should be smaller than 3 μm when targeting to achieve tip bending of less than 50 nm.

5.3 Failure Mode and Process Yield

Next, we will exam the failure mode and process yield for different dimensions. The devices have been grouped as Figure 5-3, Figure 5-4 and Figure 5-5. The statistic on failure mode is mainly based on electrical measurement. For the above mentioned failure mode, it is difficult to be confirmed in the SEM directly, as a beam to gate shortage normally leads to device melting.

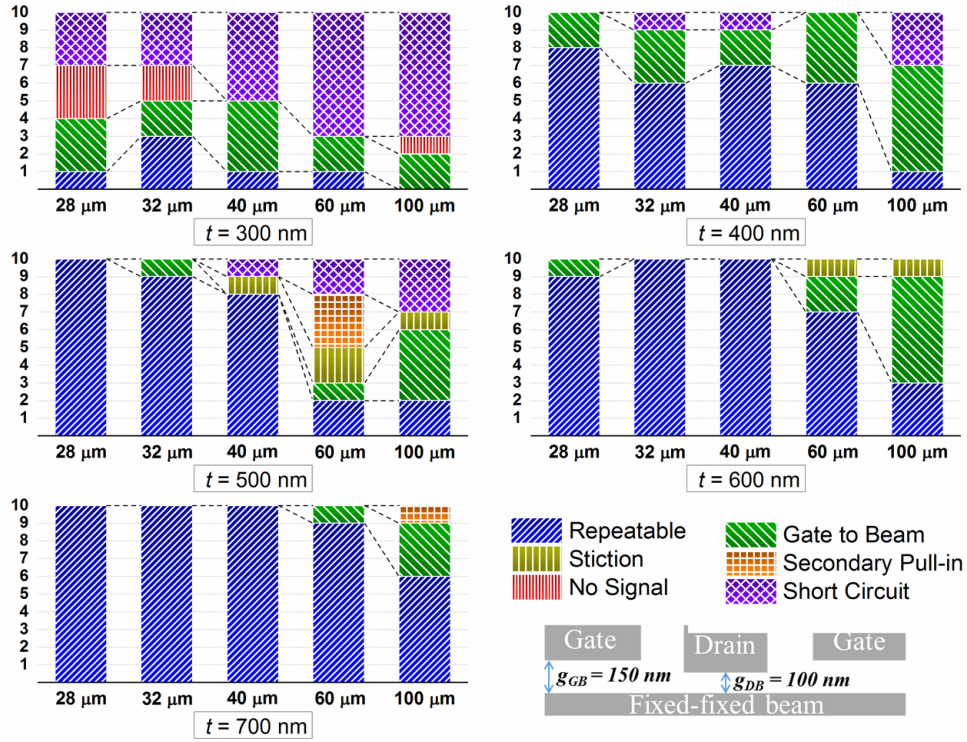


Figure 5-8 Failure analysis of fixed-fixed beam devices with $g_{GB} = 150 \text{ nm}$, and $g_{DB} = 100 \text{ nm}$, with beam length L_B (x-axis), beam width t varies. Number on y-axis indicate the count of different failure mode.

First, failure mode of fixed-fixed beam with $g_{GB} = 150 \text{ nm}$, and $g_{DB} = 100 \text{ nm}$ is plotted on Figure 5-8. The devices generally show very good repeatability with the beam width of $t > 500 \text{ nm}$ and beam length of $L_B < 40 \mu\text{m}$. Six groups of devices have a 100% process yield of repeatability with 60 devices measured.

Overall, the predominant failure mode is a gate to beam pull-in, in which the beam cannot withstand the excessive electrostatic force and collapse on the gate terminal, after the beam touches the drain. Two possible gate to beam pull-in methods are shown in Figure 5-9.

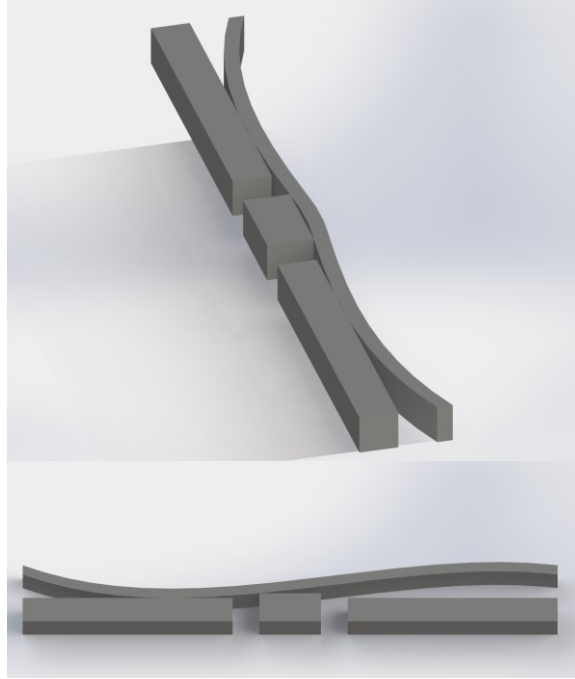


Figure 5-9 Gate to beam pull-in devices

Meanwhile, the secondary pull-in effect can be treated as a special case of gate to beam pull-in, as after a successful drain to beam touch, a small extra voltage makes the beam collapse on the gate.

A few stiction cases can also be observed when the beam is too long, in which the elastic force is not high enough to detach the beam from the drain terminal. The stiction mode is good for non-volatile memory application, but we fail to observe consistent stiction phenomena in all switches of certain dimensions, which means that the Van de Waal force on the contact surface varies from device to device. Thus, a wider drain terminal should be used for non-volatile memory devices.

Another major failure mode in this group is short circuit, it is understandable that very long and thin beams will touch the other terminal when the stress is high. However, the 300 nm wide beam group has a lot of

short circuit devices. The main reason is that the etching step between *Figure 4-3 (f)* and *Figure 4-3 (g)* cannot fully etch away unwanted Mo, because the lithography condition is a bit different in the case of 100nm wide gap and 300nm wide beam. This problem can be easily avoided by adding etching time in logic circuit application, where the devices have similar gap and beam width. The similar reason why some devices in that group have no signal when the gap opens on the actuation side, is that the beam is fixed on the other side caused by incomplete etching.

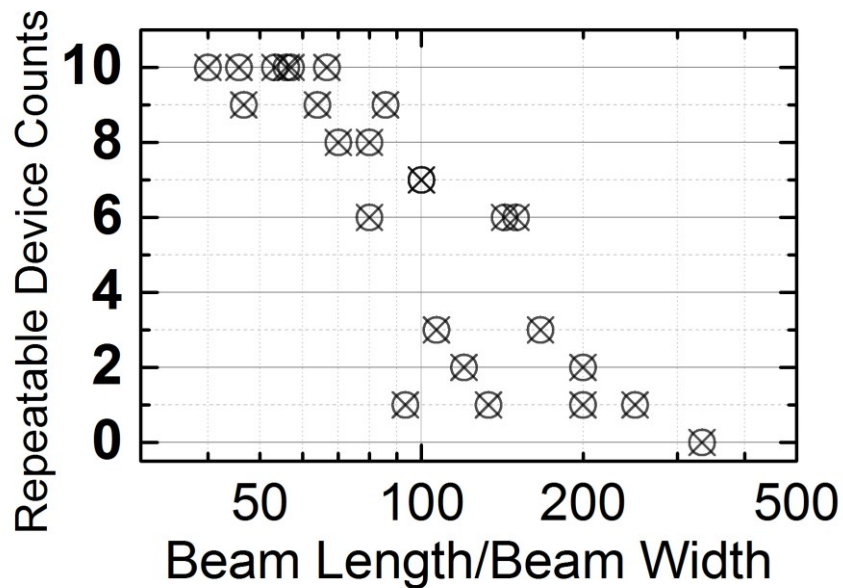


Figure 5-10 Counts of repeatable device versus beam length to width ratio

Most failures are closely related to the stiffness of the beam. The effective spring constant is antiproportional to $(L_B/t)^3$. The process yield drops quickly with $L_B/t > 70$ as shown in Figure 5-10. As mentioned, in the fabrication process after the oxide mold is prepared, decreasing or increasing the oxide fin thickness has the similar effects on reducing the pull-in voltage. Reducing the oxide fin thickness is more favorable, as it will also decrease the beam length to width ratio and improve the device yield as shown above.

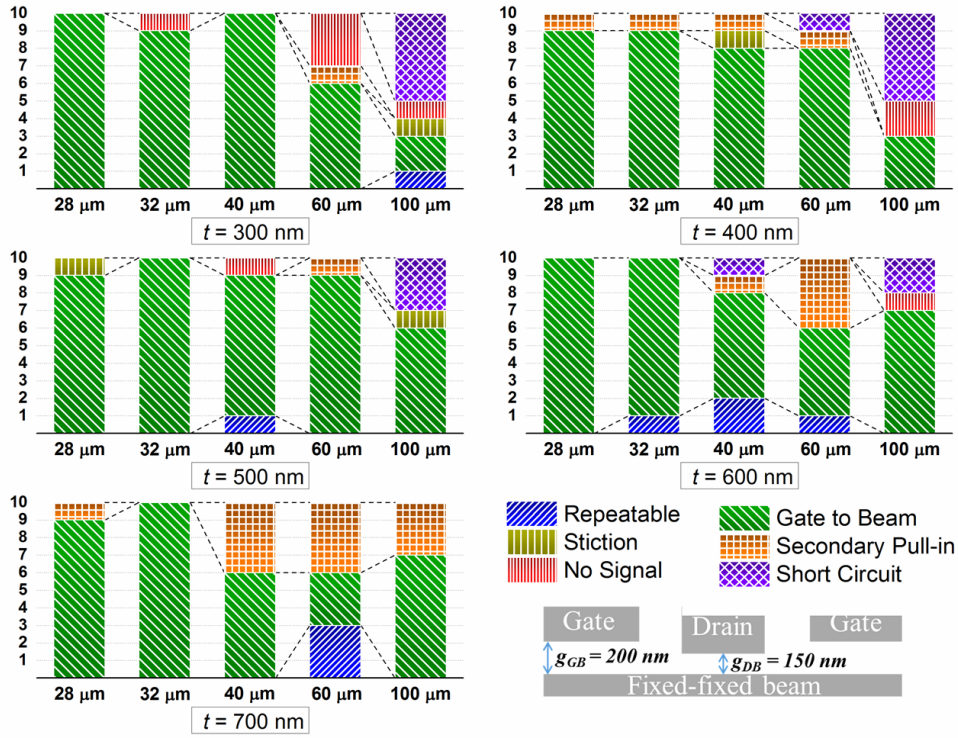


Figure 5-11 Failure analysis of fixed-fixed beam devices with $g_{GB} = 200 \text{ nm}$ and $g_{DB} = 150 \text{ nm}$, with beam length L_B (x-axis), beam width t varies. Number on y-axis indicate the count of different failure mode.

For fixed-fixed beam with $g_{GB} = 200 \text{ nm}$ and $g_{DB} = 150 \text{ nm}$ shown in Figure 5-11, the dominant failure mode is the gate to beam pull-in. Even the devices with high spring constant (small length/width ratio) face nearly 100% collapse on the gate terminal. Compared to the previous group, all the dimensions are the same except for the gap width. The g_{GB} to g_{DB} ratio is 1.33 compared to 1.5 in the previous case. Therefore, the difference between actuation gap and contact gap is a very sensitive factor for device yield, and maintaining a 1.5 ratio is a reasonable requirement.

Larger g_{GB} to g_{DB} ratio may further guarantee no gate-to-beam pull-in. As g_{DB} is usually defined by the smallest dimension available, the actuation gap will expand accordingly causing an unwanted pull-in voltage increase.

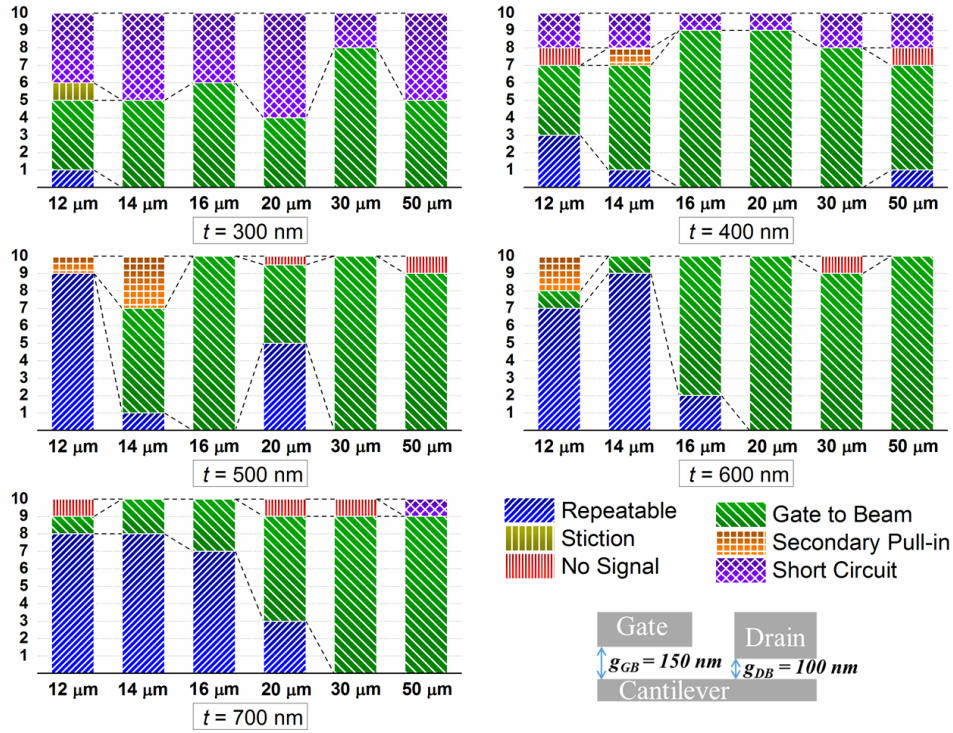


Figure 5-12 Failure analysis of cantilever beam devices with $g_{GB} = 150 \text{ nm}$, and $g_{DB} = 100 \text{ nm}$, with beam length L_B (x-axis), beam width t varies. Number on y-axis indicate the count of different failure mode.

Lastly, for the cantilever shown in Figure 5-12, compared with the pull-in voltage figure (Figure 5-5), suffers severe bending and the curvature varies from device to device. From the measurement, most devices experience a direct beam to gate touch. As shown in Figure 5-13, no overlap between drain terminal and beam exists, thus the gate-to-beam pull-in is inevitable when high stress gradient presents. As discussed in the last section, the cantilever devices will have better control of bending when a beam length is further scaled down and the metal thickness is remained unchanged at the same time.

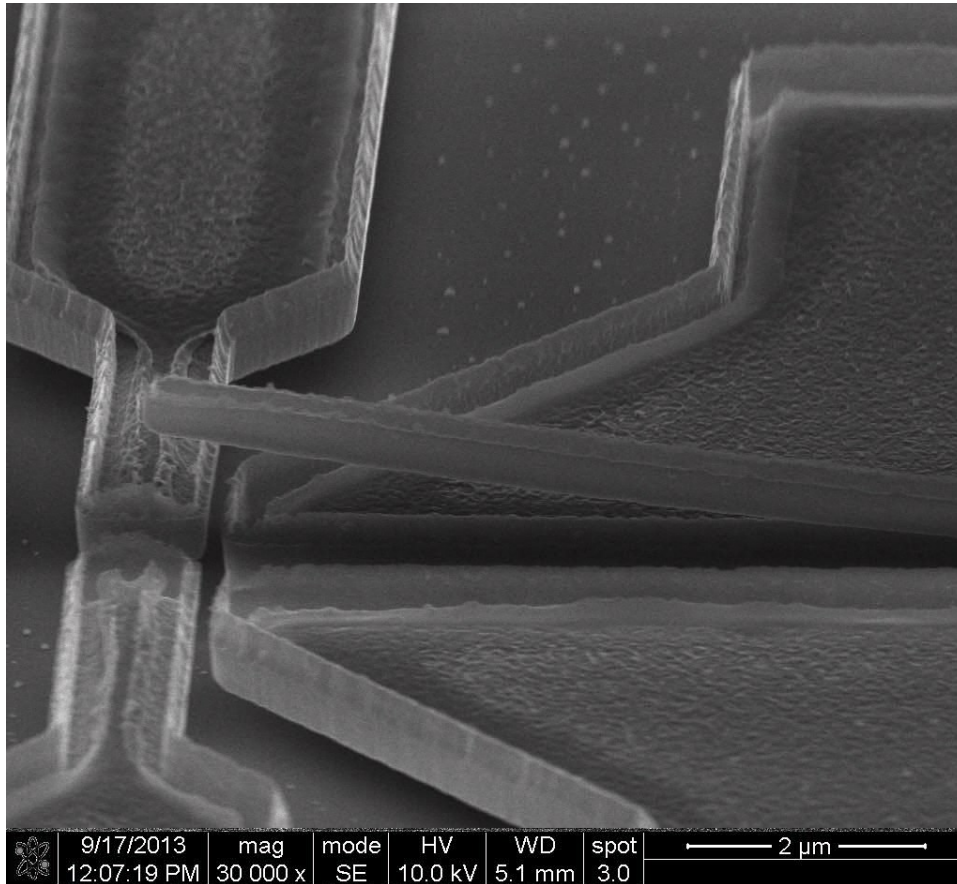


Figure 5-13 Cantilever in NEMS switch with severe bending.

5.4 Conclusion

This chapter provides a few references to identify the dimension of NEMS switches, and to ensure the devices have a desired pull-in voltage, less stress issue, and high process yield.

1. This chapter begins with an analytical solution developed to estimate the pull-in voltage, $\pm 2\%$ deviation compared with FEM is achieved.
2. The deformation of the metal film needs to be carefully considered. Lack of methods to eliminate the stress gradient, the only effective way is to maintain the metal film thickness and reduce the beam length

simultaneously. For 300 nm thick Mo film, maximum length of fixed-fixed beam and cantilever is 40 μm and 3 μm respectively.

3. For certain critical dimension and pull-in voltage, a low beam length to width ratio is required to obtain a high process yield, where L_B/t should be less than 70
4. The actuation gap to contact gap ratio is also critical and should be no smaller than 1.5.

Chapter 6 Conclusions

6.1 Contributions of This Works

This thesis aims to solve the challenges that CMOS technology are facing today – the increasing needs of computational ability versus the management of power consumption. The growing demands on logic devices working in a harsh environment and ultra-low power application also reveal the limitation of state-of-art ICs. To achieve that end, N/MEMS switch technology that has zero-state leakage current and abrupt switch behavior is investigated.

In this work, design consideration and prototype devices of N/MEMS switches are demonstrated. In particular, based on the existing works, two major hurdles of the NEMS switch technology towards their miniaturization are studied: high pull-in voltage and low process yield.

The key contributions of this work are summarized, as follows:

The dual SiNWs based U-shaped NEMS switch shows superior outcome in terms of low actuation voltage. We take advantage of the high electrostatic force generated by the large capacitive paddle and high flexibility from the single crystal SiNWs. For the first time, electrostatic actuated NEMS switches achieve a $\sim 1\text{V}$ pull-in voltage.

To further extend the range of application, an all Mo based NEMS switch has been fabricated. The goal of developing this kind of device is to achieve the following requirements simultaneously: low temperature CMOS

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compatible process, limited mask layer used, sound reliability, low contact resistance, ~100nm metal-to-metal gap, high temperature operation capability and high process yield. Studies so far can only accomplish one or two characteristics among them.

The objective is fully realized. Thanks to the all metal structural material, the process temperature is successfully controlled under 400 °C. The Damascene-like process provides a clean, high aspect ratio and metal-to-metal contact surface by using only one single mask.

I-V sweep tests done for devices with different width show good performance of abrupt switching behavior with 10^8 on/off ratio. Contact resistance of the device has been measured as 2.5 k Ω . 1 mA current can safely pass through the contact area. Cycling tests at 300 °C and room temperature for the smallest width devices are performed to examine the endurance of the device. The devices work reliably for 28 hours, 20,000 cycles at 300 °C vacuum environment without failure.

Statistical study of the all metal based NEMS switches is carried afterward, several dimensions with 100% process yield are identified. The basic design rules to obtain high process yield devices are determined. For certain critical dimension and pull-in voltage, a low beam length to width ratio is desirable to obtain a very high process yield, where $L_B/t < 70$ is preferred. The actuation gap to contact gap ratio is also critical and should be no smaller than 1.5.

6.2 Future Directions

6.2.1 Further scaling

As the statistical study shown in chapter 5, even the devices with very high beam length/beam width ratio need around 3V pull-in voltage, further scaling of the dimension is critical to implement the NEMS switch technology.

In chapter 4, we have discussed the detailed process flow for the all-metal NEMS switches. The critical dimension of the mask used for the current batch of devices is 200 nm, with wet etching to reduce the pull-in voltage, and the minimum actuation gap can be achieved is 100 nm. To further scale down the device dimension, the only way is to use the lithographic tool with better resolution.

Another aspect of device scaling-down is the thickness of the metal layer, as discussed in Chapter 4 and Chapter 5, to keep the metal layer with certain thickness will help to confine the deformation the beam. In that sense, the process of forming the oxide fin needs to be optimized. Considering the fin thickness is scaling down but the fin height needs to be maintained, the aspect ratio of oxide fin needs to be increased. Thus, higher aspect ratio oxide etching process needs to be developed.

The effect of scaling-down will also be changed if the metal layer thickness w keeps constant. A few properties shown in Table 2-2 need to be altered. However, the pull-in voltage is still scaling down with the same factor and the switching speed will also increase accordingly. Thus, these two most

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important aspects of NEMS switches can still be favored from the smaller device dimension. The detailed scaling properties can be found in Table 6-1.

The all-metal-based NEMS switch developed in chapter 4 and chapter 5 has drawback of high pull-in voltage compared to the U-shaped SiNW switch introduced in chapter 3. For laterally actuated NEMS switch, the pull-in voltage is largely limited by the minimal feature size of the process. While further scaling down the dimensions can not only achieve a NEMS switch with similar operating voltage as CMOS transistor, but can largely improve the performance of speed and energy consumption as well.

Table 6-1 The scaling properties of N/MEMS technology with constant w

Switch parameter	Scaling Factor
Spring Constant, k	1
Mass, m	$1/U^2$
Pull-In Voltage, V_{pi}	$1/U$
Speed	U
Device Density	U^2
Switching Energy	$1/U^2$

6.2.2 Devices with different functions

The operation of N/MEMS switches is based on the control of three different forces: the electrostatic force, the spring restoring force and the

adhesion force. For device targeting on logic function. The spring restoring forces are designed to be larger than the adhesion force. By changing the dimension of the contact surface, the adhesion forces will overcome the spring restoring force. Once the physical contact is formed, the on state will remain even after the electrostatic force is removed. Therefore, memory devices like NVM and one time programmable memory can be realized by simply modify the layout without fabrication process change.

With the robust NEMS switch process developed, there is quite a lot of space to demonstrate devices with different functions within the same chip.

Furthermore, the U-shaped SiNW NEMS switches are also capable of monolithically fabrication with SiNW transistors. The process of U-shaped SiNW NEMS switch starts with SOI wafer, followed by SiNW formation, doping, dielectric material formation and metallization. The similar sequence has been used for SiNW transistors fabrication[232]. Therefore, NEMS-CMOS integration can be achieved by fabricating SiNW NEMS switches and SiNW transistors at the same time.

6.2.3 Encapsulation

Any N/MEMS device needs proper packaging to protect the devices. For N/MEMS switches, it is important to provide a clean environment for the operation. Vacuum level encapsulation is more favored as it ensures the contact surface would not be oxidized over the time. Removing air also increases the speed of the switches as the air damping is eliminated from the surroundings.

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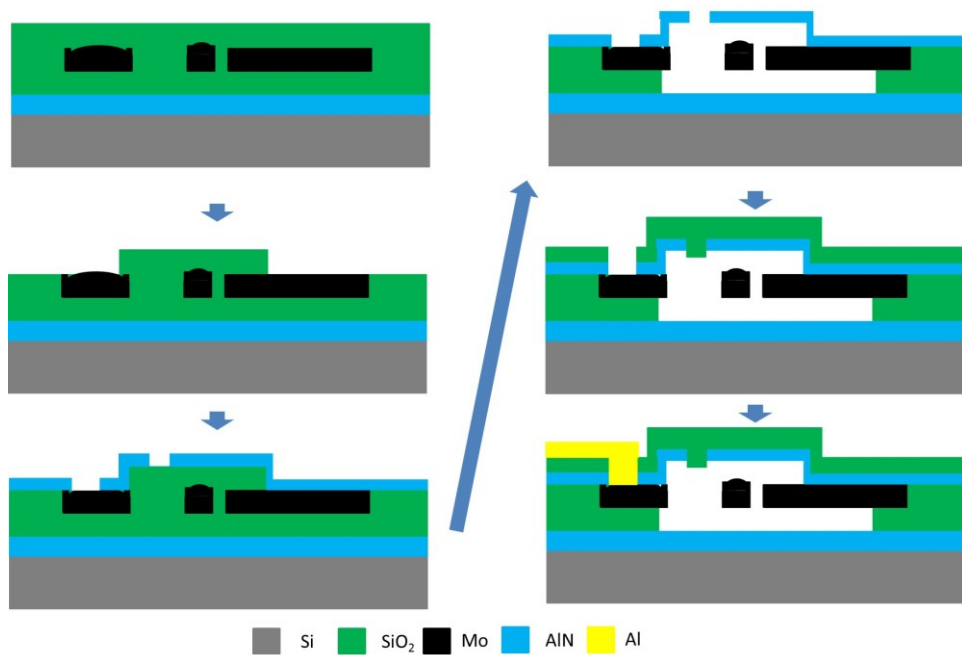


Figure 6-1 Proposed Process flow for wafer level encapsulated NEMS switch

A possible process flow for wafer level encapsulated NEMS switches is shown in Figure 6-1. An extra layer of AlN is added on NEMS switches for insulation. After fabrication of laterally actuated NEMS switches, the metal structure is buried with SiO₂ for the encapsulation. The top SiO₂ is planarized by CMP, following by RIE to define the active area. A 500 nm AlN layer is deposited by PVD and pattern for releasing hole. The devices are then released by VHF. The sealing is conducted by 1 μm SiO₂ deposition. Lastly, the metal pad is opened for Al interconnection.

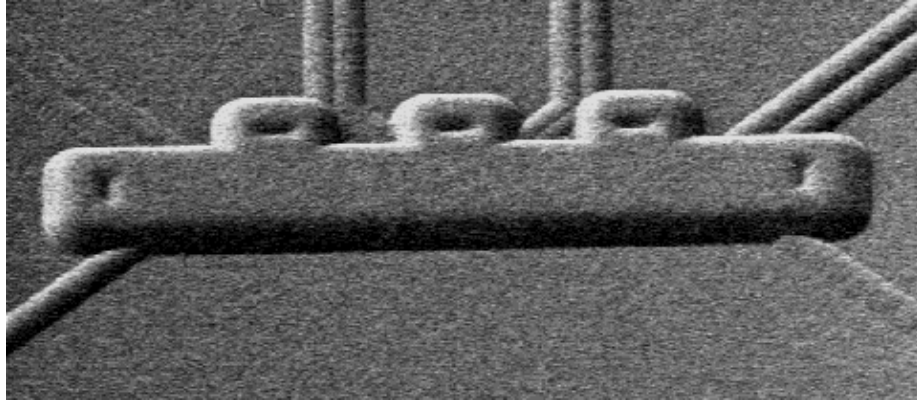


Figure 6-2 SEM image of an encapsulated NEMS switch

A test run of encapsulation process has been conducted. Figure 6-2 depicted a sealed fixed-fixed beam switch. No obvious deformation is found on the sealing roof. All release holes are successfully sealed. The cross-section of the cavity containing the movable beam is shown in Figure 6-3. Unfortunately, since the cavity is cut by FIB, a thick gallium layer is deposited inside the surface of the cavity, and buried the thin Mo layer inside. However, we still can clearly recognize the SiO_2/AlN roof supports adequate room of the NEMS switches operation.

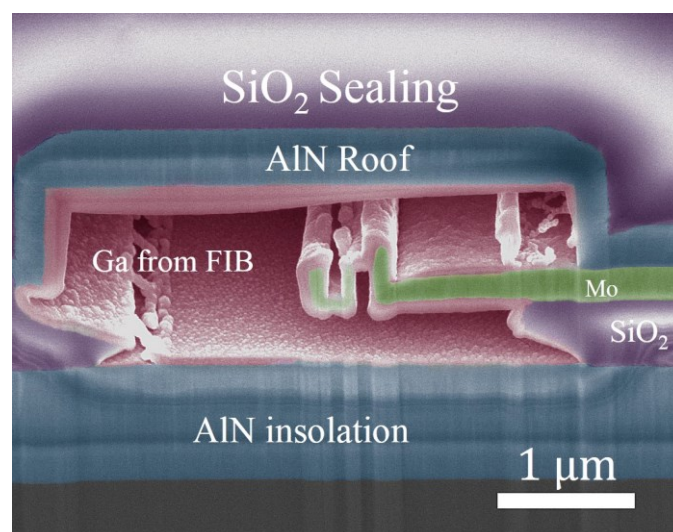


Figure 6-3 Cross-section of an encapsulated NEMS switch

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Bibliography

- [1] Y. Taur and T. H. Ning, *Fundamentals of modern VLSI devices* vol. 2: Cambridge University Press Cambridge, 1998.
- [2] T. Yuan and E. J. Nowak, "CMOS devices below 0.1 μm : how high will performance go?," in *International Electron Devices Meeting, 1997. IEDM '97. Technical Digest.*, pp. 215-218, 1997.
- [3] G. Shahidi, J. D. Warnock, J. Comfort, S. Fischer, P. A. McFarland, A. Acovic, T. I. Chappell, B. A. Chappell, T. H. Ning, and C. J. Anderson, "CMOS scaling in the 0.1- μm , 1. X-volt regime for high-performance applications," *IBM Journal of Research and Development*, vol. 39, pp. 229-244, 1995.
- [4] *International Technology Roadmap for Semiconductors (ITRS), 2013 Edition*. Available: <http://www.itrs.net/reports.html>
- [5] S. Borkar, "Design challenges of technology scaling," *IEEE Micro*, vol. 19, pp. 23-29, 1999.
- [6] I. F. Akyildiz, W. Su, Y. Sankarasubramaniam, and E. Cayirci, "Wireless sensor networks: a survey," *Computer Networks*, vol. 38, pp. 393-422, 2002.
- [7] A. Dada and F. Thiesse, "Sensor Applications in the Supply Chain: The Example of Quality-Based Issuing of Perishables," in *The Internet of Things*. vol. 4952, C. Floerkemeier, M. Langheinrich, E. Fleisch, F. Mattern, and S. Sarma, Eds., ed: Springer Berlin Heidelberg, pp. 140-154, 2008.
- [8] A. Ilic, T. Staake, and E. Fleisch, "Using Sensor Information to Reduce the Carbon Footprint of Perishable Goods," *Pervasive Computing, IEEE*, vol. 8, pp. 22-29, 2009.
- [9] J. Gubbi, R. Buyya, S. Marusic, and M. Palaniswami, "Internet of Things (IoT): A vision, architectural elements, and future directions," *Future Generation Computer Systems*, vol. 29, pp. 1645-1660, 2013.
- [10] P. Spiess, S. Karnouskos, D. Guinard, D. Savio, O. Baecker, L. Souza, and V. Trifa, "SOA-Based Integration of the Internet of Things in Enterprise Services," in *IEEE International Conference on Web Services (ICWS)*, pp. 968-975, 2009.
- [11] V. M. Rohokale, N. R. Prasad, and R. Prasad, "A cooperative Internet of Things (IoT) for rural healthcare monitoring and control," in *2nd International Conference on Wireless Communication, Vehicular Technology, Information Theory and Aerospace & Electronic Systems Technology (Wireless VITAE)*, pp. 1-6, 2011.

- [12] N. Bui and M. Zorzi, "Health care applications: a solution based on the internet of things," in *Proceedings of the 4th International Symposium on Applied Sciences in Biomedical and Communication Technologies*, Barcelona, Spain, pp. 1-5, 2011.
- [13] A. Ghose, C. Bhaumik, D. Das, and A. K. Agrawal, "Mobile healthcare infrastructure for home and small clinic," in *Proceedings of the 2nd ACM international workshop on Pervasive Wireless Healthcare*, Hilton Head, South Carolina, USA, pp. 15-20, 2012.
- [14] C. Buckl, S. Sommer, A. Scholz, A. Knoll, A. Kemper, J. Heuer, and A. Schmitt, "Services to the Field: An Approach for Resource Constrained Sensor/Actor Networks," in *International Conference on Advanced Information Networking and Applications Workshops (WAINA)*, pp. 476-481, 2009.
- [15] W. K. G. Seah, E. Zhi Ang, and H. Tan, "Wireless sensor networks powered by ambient energy harvesting (WSN-HEAP) - Survey and challenges," in *1st International Conference on Wireless Communication, Vehicular Technology, Information Theory and Aerospace & Electronic Systems Technology (Wireless VITAE)*, pp. 1-5, 2009.
- [16] S. Salahuddin and S. Datta, "Use of negative capacitance to provide voltage amplification for low power nanoscale devices," *Nano letters*, vol. 8, pp. 405-410, 2008.
- [17] R. Gandhi, Z. Chen, N. Singh, K. Banerjee, and S. Lee, "Vertical Si-Nanowire n-Type Tunneling FETs With Low Subthreshold Swing (<50mV/decade) at Room Temperature," *IEEE Electron Device Letters*, vol. 32, pp. 437-439, 2011.
- [18] K. Gopalakrishnan, P. B. Griffin, and J. D. Plummer, "I-MOS: A novel semiconductor device with a subthreshold slope lower than kT/q ," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 289-292, 2002.
- [19] V. Pott, H. Kam, R. Nathanael, J. Jeon, E. Alon, and T.-J. K. Liu, "Mechanical Computing Redux: Relays for Integrated Circuit Applications," *Proceedings of the IEEE*, 2010.
- [20] G. R. Voicu, M. Enachescu, and S. D. Cotofana, "Towards "zero-energy" using NEMFET-based power management for 3D hybrid stacked ICs," in *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, pp. 203-209, 2011.
- [21] T.-J. K. Liu, V. Pott, E. Alon, H. Fariborzi, M. Spencer, V. Karkare, J. Jeon, R. Nathanael, C. Wang, F. Chen, H. Kam, V. Stojanović, and D. Markovic, "Analysis and demonstration of MEM-relay power gating," in *IEEE Custom Integrated Circuits Conference (CICC)*, pp. 1-4, 2010.

- [22] X. Huang, C. Zhang, H. Yu, and W. Zhang, "A Nanoelectromechanical-Switch-Based Thermal Management for 3-D Integrated Many-Core Memory-Processor System," *IEEE Transactions on Nanotechnology*, 2012.
- [23] M. B. Henry and L. Nazhandali, "NEMS-Based Functional Unit Power-Gating: Design, Analysis, and Optimization," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, pp. 290-302, 2013.
- [24] M. B. Henry, R. Lyster, L. Nazh, L. Nazhandali, A. Fruehling, and D. Peroulis, "MEMS-Based Power Gating for Highly Scalable Periodic and Event-Driven Processing," in *24th International Conference on VLSI Design (VLSI Design)*, 2011.
- [25] M. Enachescu, G. R. Voicu, and S. D. Cotofana, "Leakage-enhanced 3D-Stacked NEMFET-based power management architecture for autonomous sensors systems," in *15th International Conference on System Theory, Control, and Computing (ICSTCC)*, pp. 1-6, 2011.
- [26] H. Alrudainy, A. Mokhov, and A. Yakovlev, "A scalable physical model for Nano-Electro-Mechanical relays," *24th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, pp. 1-7, 2014.
- [27] Y. Nakagome, M. Horiguchi, T. Kawahara, and K. Itoh, "Review and future prospects of low-voltage RAM circuits," *IBM Journal of Research and Development*, vol. 47, pp. 525-552, 2003.
- [28] R. W. Mann, W. W. Abadeer, M. J. Breitwisch, O. Bula, J. S. Brown, B. C. Colwill, P. E. Cottrell, W. T. Crocco, S. S. Furkay, M. J. Hauser, T. B. Hook, D. Hoyniak, J. M. Johnson, C. H. Lam, R. D. Mih, J. Rivard, A. Moriwaki, E. Phipps, C. S. Putnam, B. A. Rainey, J. J. Toomey, and M. I. Younus, "Ultralow-power SRAM technology," *IBM Journal of Research and Development*, vol. 47, pp. 553-566, 2003.
- [29] S. Chong, H.-S. P. Wong, K. Akarvardar, R. Parsa, J.-B. Yoon, R. T. Howe, and S. Mitra, "Nanoelectromechanical (NEM) relays integrated with CMOS SRAM for improved stability and low leakage," in *Proceedings of the 2009 International Conference on Computer-Aided Design (ICCAD)*, New York, New York, USA, p. 478, 2009.
- [30] Y. J. Kim and W. Y. Choi, "Nonvolatile Nanoelectromechanical Memory Switches for Low-Power and High-Speed Field-Programmable Gate Arrays," *IEEE Transactions on Electron Devices*, vol. PP, pp. 1-1, 2014.
- [31] S. Han, V. Sirigiri, D. G. Saab, F. K. Chowdhury, and M. Tabid-Azar, "Compact NEMS FPGA design for harsh environment and low power requirement," in *The 17th International Conference on Solid-State*

- Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII)*, pp. 2369-2372, 2013.
- [32] C. Chen, H.-S. P. Wong, K. Akarvardar, R. Parsa, N. Patil, S. Chong, J. Provine, D. Lewis, J. Watt, R. T. Howe, and S. Mitra, "Efficient FPGAs using nanoelectromechanical relays," in *Proceedings of the 18th annual ACM/SIGDA international symposium on Field programmable gate arrays* 2010.
 - [33] M. N. Lovellette, A. B. Campbell, H. L. Hughes, R. K. Lawrence, J. W. Ward, M. Meinhold, T. R. Bengtson, G. F. Carleton, B. M. Segal, and T. Rueckes, "Nanotube memories for space applications," in *IEEE Aerospace Conference*, pp. 2300-2305, 2004.
 - [34] V. Ranganathan, T. He, S. Rajgopal, M. Mehregany, X. L. Feng, and S. Bhunia, "Nanomechanical non-volatile memory for computing at extreme," in *IEEE/ACM International Symposium on Nanoscale Architectures (NANOARCH)*, pp. 44-45, 2013.
 - [35] A. Basu, R. P. Hennessy, G. Adams, and N. E. McGruer, "Hot switching damage mechanisms in MEMS contacts—evidence and understanding," *Journal of Micromechanics and Microengineering*, vol. 24, p. 105004, 2014.
 - [36] T. Ishida, K. Kakushima, and H. Fujita, "Degradation Mechanisms of Contact Point During Switching Operation of MEMS Switch," *Journal of Microelectromechanical Systems*, 2013.
 - [37] F. W. DelRio, M. P. Boer, J. A. Knapp, E. David Reedy, P. J. Clews, and M. L. Dunn, "The role of van der Waals forces in adhesion of micromachined surfaces," *Nature Materials*, vol. 4, pp. 629-634, 2005.
 - [38] T.-J. K. Liu, J. Yaung, L. Hutin, and J. Jeon, "Adhesive Force Characterization for MEM Logic Relays With Sub-Micron Contacting Regions," *Journal of Microelectromechanical Systems*, vol. 23, pp. 198-203, 2014.
 - [39] S. Obata, M. Inoue, T. Miyagi, I. Mori, Y. Sugizaki, Y. Shimooka, A. Kojima, M. Endo, and H. Shibata, "In-line wafer level hermetic packages for MEMS variable capacitor," in *58th Electronic Components and Technology Conference*, pp. 158-163, 2008.
 - [40] T.-J. K. Liu, Y. Chen, I.-R. Chen, L. Hutin, and V. Subramanian, "Micro-relay reliability improvement by inkjet-printed microshell encapsulation," in *The 17th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII)*, pp. 1974-1977, 2013.
 - [41] R. Nathanael, V. Pott, H. Kam, J. Jeon, and T. J. K. Liu, "4-Terminal Relay Technology for Complementary Logic," *IEEE International Electron Devices Meeting*, pp. 204-207, 2009.

- [42] J. Qiu, J. H. Lang, A. H. Slocum, and A. C. Weber, "A bulk-micromachined bistable relay with U-Shaped thermal actuators," *Journal of Microelectromechanical Systems*, vol. 14, pp. 1099-1109, 2005.
- [43] D. Lee, W. S. Lee, J. Provine, J. O. Lee, J. B. Yoon, R. T. Howe, S. Mitra, and H. S. P. Wong, "Titanium Nitride Sidewall Stringer Process for Lateral Nanoelectromechanical Relays," *23rd IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, pp. 456-459, 2010.
- [44] S. W. Lee, S. J. Park, E. E. B. Campbell, and Y. W. Park, "A fast and low-power microelectromechanical system-based non-volatile memory device," *Nature Communications*, vol. 2, 2011.
- [45] D. N. Guerra, M. Imboden, and P. Mohanty, "Electrostatically actuated silicon-based nanomechanical switch at room temperature," *Applied Physics Letters*, vol. 93, 2008.
- [46] K. E. Petersen, "Micromechanical Membrane Switches on Silicon," *IBM Journal of Research and Development*, vol. 23, pp. 376-385, 1979.
- [47] K. E. Petersen, "Micromechanical voltage controlled switches and circuits," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 100-103, 1978.
- [48] K. E. Petersen, "Silicon as a mechanical material," *Proceedings of the IEEE*, vol. 70, pp. 420-457, 1982.
- [49] W. W. Jang, J. O. Lee, J. B. Yoon, M. S. Kim, J. M. Lee, S. M. Kim, K. H. Cho, D. W. Kim, D. Park, and W. S. Lee, "Fabrication and characterization of a nanoelectromechanical switch with 15-nm-thick suspension air gap," *Applied Physics Letters*, vol. 92, 2008.
- [50] J. Rubin, R. Sundararaman, M. Kim, and S. Tiwari, "A Low-Voltage Torsion Nanorelay," *IEEE Electron Device Letters*, vol. 32, pp. 414-416, 2011.
- [51] Y. Hayamizu, T. Yamada, K. Mizuno, R. C. Davis, D. N. Futaba, M. Yumura, and K. Hata, "Integrated three-dimensional microelectromechanical devices from processable carbon nanotube wafers," *Nature Nanotechnology*, vol. 3, pp. 289-294, 2008.
- [52] J. E. Jang, S. N. Cha, Y. Choi, G. A. J. Amaratunga, D. J. Kang, D. G. Hasko, J. E. Jung, and J. M. Kim, "Nanoelectromechanical switches with vertically aligned carbon nanotubes," *Applied Physics Letters*, vol. 87, 2005.
- [53] M. Y. Liao, S. Hishita, E. Watanabe, S. Koizumi, and Y. Koide, "Suspended Single-Crystal Diamond Nanowires for High-Performance

- Nanoelectromechanical Switches," *Advanced Materials*, vol. 22, pp. 5393-+, 2010.
- [54] R. Parsa, M. Shavezipur, W. S. Lee, S. Chong, D. Lee, H. S. P. Wong, R. Maboudian, and R. T. Howe, "Nanoelectromechanical Relays with Decoupled Electrode and Suspension," *IEEE 24th International Conference on Micro Electro Mechanical Systems (MEMS)*, pp. 1361-1364, 2011.
 - [55] J. O. Lee, M. W. Kim, S. D. Ko, H. O. Kang, W. H. Bae, M. H. Kang, K. N. Kim, D. E. Yoo, and J. B. Yoon, "3-Terminal Nanoelectromechanical Switching Device in Insulating Liquid Media for Low Voltage Operation and Reliability Improvement," *IEEE International Electron Devices Meeting*, pp. 208-211, 2009.
 - [56] W. F. Xiang and C. Lee, "Nanoelectromechanical torsion switch of low operation voltage for nonvolatile memory application," *Applied Physics Letters*, vol. 96, p. 193113, 2010.
 - [57] S. Chong, B. Lee, S. Mitra, R. T. Howe, and H. S. P. Wong, "Integration of Nanoelectromechanical Relays With Silicon nMOS," *IEEE Transactions on Electron Devices*, vol. 59, pp. 255-258, 2012.
 - [58] R. M. Proie, R. G. Polcawich, J. S. Pulskamp, T. Ivanov, and M. E. Zaghoul, "Development of a PZT MEMS Switch Architecture for Low-Power Digital Applications," *Journal of Microelectromechanical Systems*, 2011.
 - [59] J. S. Pulskamp and R. M. Proie, "Nano-and micro-electromechanical switch dynamics," *Journal of Microelectromechanical Systems*, 2013.
 - [60] R. M. Proie, R. G. Polcawich, J. S. Pulskamp, T. Ivanov, and M. E. Zaghoul, "Development of a PZT MEMS Switch Architecture for Low-Power Digital Applications," *Journal of Microelectromechanical Systems*, vol. 20, pp. 1032-1042, 2011.
 - [61] N. Sinha, T. S. Jones, Z. J. Guo, and G. Piazza, "Body-Biased Complementary Logic Implemented Using AlN Piezoelectric MEMS Switches," *Journal of Microelectromechanical Systems*, vol. 21, pp. 484-496, 2012.
 - [62] N. Sinha, G. Zhijun, A. Tazzoli, A. DeHon, and G. Piazza, "1 Volt digital logic circuits realized by stress-resilient ALN parallel dual-beam MEMS relays," in *IEEE 25th International Conference on Micro Electro Mechanical Systems (MEMS)*, pp. 668-671, 2012.
 - [63] M. Kousuke, M. Moriyama, M. Esashi, and S. Tanaka, "Low-voltage PZT-actuated MEMS switch monolithically integrated with CMOS circuit," in *IEEE 25th International Conference on Micro Electro Mechanical Systems (MEMS)*, pp. 1153-1156, 2012.

- [64] U. Zaghoul and G. Piazza, "Highly Scalable NEMS Relays With Stress-Tuned Switching Voltage Using Piezoelectric Buckling Actuators," *IEEE Transactions on Electron Devices*, pp. 1-1, 2014.
- [65] U. Zaghoul and G. Piazza, "Synthesis and characterization of 10 nm thick piezoelectric AlN films with high c-axis orientation for miniaturized nanoelectromechanical devices," *Applied Physics Letters*, vol. 104, p. 253101, 2014.
- [66] U. Zaghoul and G. Piazza, "Sub-1-volt Piezoelectric Nanoelectromechanical Relays With Millivolt Switching Capability," *IEEE Electron Device Letters*, vol. 35, pp. 669-671, 2014.
- [67] U. Zaghoul and G. Piazza, "10–25 nm piezoelectric nano-actuators and NEMS switches for millivolt computational logic," in *IEEE 26th International Conference on Micro Electro Mechanical Systems (MEMS)*, pp. 233-236, 2013.
- [68] N. Sinha, G. E. Wabiszewski, R. Mahameed, V. V. Felmetzger, S. M. Tanner, R. Carpick, and G. Piazza, "Piezoelectric aluminum nitride nanoelectromechanical actuators," *Applied Physics Letters*, vol. 95, p. 053106, 2009.
- [69] N. Sinha, T. S. Jones, Z. Guo, and G. Piazza, "Body-Biased Complementary Logic Implemented Using AlN Piezoelectric MEMS Switches," *Journal of Microelectromechanical Systems*, vol. 21, pp. 484-496, 2012.
- [70] N. Sinha, Z. Guo, A. Tazzoli, A. DeHon, and G. Piazza, "1 Volt digital logic circuits realized by stress-resilient ALN parallel dual-beam MEMS relays," in *IEEE 25th International Conference on Micro Electro Mechanical Systems (MEMS)*, pp. 668-671, 2012.
- [71] J. Qiu, J. H. Lang, A. H. Slocum, and A. C. Weber, "A bulk-micromachined bistable relay with U-shaped thermal actuators," *Journal of Microelectromechanical Systems*, 2005.
- [72] M. Tang, E. Liao, C. K. Cheng, D. Lee, R. Kumar, Y. H. Lee, R. Shankar, O. Le Neel, G. Noviello, and F. Italia, "A Magnetostatic MEMS Switch Designed for Portable Applications," *Journal of Microelectromechanical Systems*, vol. 19, pp. 1131-1139, 2010.
- [73] M. Tang, Y. H. Lee, R. Kumar, R. Shankar, O. Le Neel, and G. Noviello, "A MEMS Microreed Switch With One Reed Embedded in the Silicon Substrate," *Journal of Microelectromechanical Systems*, vol. 20, pp. 1336-1344, 2011.
- [74] M. Glickman, P. Tseng, J. Harrison, T. Niblock, I. B. Goldberg, and J. W. Judy, "High-Performance Lateral-Actuating Magnetic MEMS Switch," *Journal of Microelectromechanical Systems*, vol. 20, pp. 842-851, 2011.

- [75] M. Tang, E. Liao, K. C. Cheng, D. Lee, R. Kumar, Y. H. Lee, R. Shankar, O. Le Néel, G. Noviello, and F. Italia, "A Magnetostatic MEMS Switch Designed for Portable Applications," *Journal of Microelectromechanical Systems*, 2010.
- [76] M. Tang, Y. H. Lee, R. Kumar, R. Shankar, O. Le Néel, and G. Noviello, "A MEMS Microreed Switch With One Reed Embedded in the Silicon Substrate," *Journal of Microelectromechanical Systems*, 2011.
- [77] Y. Zhang, G. Ding, X. Shun, X. Li, and B. Cai, "Design and analysis of the micromechanical structure for an electromagnetic bistable RF MEMS switch," in *Asia-Pacific Microwave Conference Proceedings (APMC)*, pp. 1-4, 2005.
- [78] M. Vincent, L. Chiesi, J. C. Fourier, A. Garnier, B. Grappe, C. Lapiere, C. Coutier, A. Samperio, S. Paineau, F. Houze, and S. Noel, "Electrical Contact Reliability in a Magnetic MEMS Switch," in *Proceedings of the 54th IEEE Holm Conference on Electrical Contacts*, pp. 145-150, 2008.
- [79] M. Glickman, P. Tseng, J. Harrison, T. Niblock, I. B. Goldberg, and J. W. Judy, "High-Performance Lateral-Actuating Magnetic MEMS Switch," *Journal of Microelectromechanical Systems*, 2011.
- [80] I.-J. Cho and E. Yoon, "Design and fabrication of a single membrane push-pull SPDT RF MEMS switch operated by electromagnetic actuation and electrostatic hold," *Journal of Micromechanics and Microengineering*, vol. 20, p. 035028, 2010.
- [81] Y. Chen, R. Nathanael, J. Jeon, J. Yaung, L. Hutin, and T.-j. K. Liu, "Characterization of Contact Resistance Stability in MEM Relays With Tungsten Electrodes," *Journal of Microelectromechanical Systems*, pp. 1-3, 2012.
- [82] R. Nathanael, T.-J. K. Liu, V. Pott, H. Kam, and J. Jeon, "4-terminal relay technology for complementary logic," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 1-4, 2009.
- [83] H. Kam and T.-J. K. Liu, "Pull-In and Release Voltage Design for Nanoelectromechanical Field-Effect Transistors," *IEEE Transactions on Electron Devices*, 2009.
- [84] R. Nathanael, V. Pott, H. Kam, J. Jeon, E. Alon, and T.-J. K. Liu, "Four-Terminal-Relay Body-Biasing Schemes for Complementary Logic Circuits," *IEEE Electron Device Letters*, 2010.
- [85] R. Nathanael, J. Jeon, I.-R. Chen, Y. Chen, F. Chen, H. Kam, and T.-J. K. Liu, "Multi-input/multi-output relay design for more compact and versatile implementation of digital logic with zero leakage,"

- International Symposium on VLSI Technology, Systems, and Applications (VLSI-TSA)*, pp. 1-2, 2012.
- [86] H. Kam, T.-J. K. Liu, and E. Alon, "Design Requirements for Steeply Switching Logic Devices," *IEEE Transactions on Electron Devices*, 2012.
 - [87] T.-J. K. Liu, H. Fariborzi, F. Chen, R. Nathanael, I.-R. Chen, L. Hutin, R. Lee, and V. Stojanović, "Relays do not leak - CMOS does," in *50th ACM / EDAC / IEEE Design Automation Conference (DAC)*, pp. 1-4, 2013.
 - [88] I.-R. Chen, Y. Chen, L. Hutin, V. Pott, R. Nathanael, and T.-J. K. Liu, "Stable ruthenium-contact relay technology for low-power logic," in *The 17th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII)*, pp. 896-899, 2013.
 - [89] G. K. Fedder, T.-J. K. Liu, R. T. Howe, and E. P. Quevy, "Technologies for Cofabricating MEMS and Electronics," *Proceedings of the IEEE*, vol. 96, pp. 306-322, 2008.
 - [90] T.-J. K. Liu, I.-R. Chen, L. Hutin, C. Park, R. Lee, R. Nathanael, J. Yaung, and J. Jeon, "Scaled Micro-Relay Structure with Low Strain Gradient for Reduced Operating Voltage," *ECS Transactions*, vol. 45, pp. 101-106, 2012.
 - [91] H. Kam, Y. Chen, and T.-J. K. Liu, "Reliable micro-electro-mechanical (MEM) switch design for ultra-low-power logic," *IEEE International Reliability Physics Symposium (IRPS)*, pp. 6-6A.1.5, 2013.
 - [92] Y. Chen, T.-J. K. Liu, R. Nathanael, J. Yaung, and L. Hutin, "Reliability of MEM relays for zero leakage logic," in *SPIE MOEMS-MEMS*, p. 861404, 2013.
 - [93] T.-J. K. Liu, E. Alon, L. Hutin, I.-R. Chen, R. Nathanael, Y. Chen, and M. Spencer, "Recent progress and challenges for relay logic switch technology," in *Symposium on VLSI Technology (VLSIT)*, pp. 43-44, 2012.
 - [94] V. Pott, E. Alon, T.-J. K. Liu, J. Jeon, R. Nathanael, and H. Kam, "Prospects for MEM logic switch technology," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 18-18.3.4, 2010.
 - [95] H. Kam, E. Alon, and T.-J. K. Liu, "A predictive contact reliability model for MEM logic switches," *IEEE International Electron Devices Meeting (IEDM)*, pp. 16-16.4.4, 2010.
 - [96] A. E. Franke, T.-J. K. Liu, J. M. Heck, and R. T. Howe, "Polycrystalline silicon-germanium films for integrated microsystems,"

- Journal of Microelectromechanical Systems*, vol. 12, pp. 160-171, 2003.
- [97] J. Jeon, V. Pott, H. Kam, R. Nathanael, E. Alon, and T.-J. K. Liu, "Perfectly Complementary Relay Design for Digital Logic Applications," *IEEE Electron Device Letters*, 2010.
 - [98] T.-J. K. Liu, "Nanomechanical Switches for Ultra - Low - Power Computation and Memory," in *Annual Device Research Conference Short Course*, pp. 1-49, 2014.
 - [99] R. Nathanael, "Nano-Electro-Mechanical (NEM) Relay Devices and Technology for Ultra-Low Energy Digital Integrated Circuits," Ph.D Thesis, University of California, Berkeley, 2012.
 - [100] D. Lee, S. Mitra, and R. T. Howe, "Multi-spacer technique for low-voltage, high-aspect-ratio lateral electrostatic actuators," in *International Solid-State Sensors, Actuators and Microsystems Conference, TRANSDUCERS*, 2011.
 - [101] J. Jeon, T.-J. K. Liu, E. Alon, L. Hutin, R. Jevtic, N. Liu, Y. Chen, R. Nathanael, W. Kwon, M. Spencer, and B. Nikolic, "Multiple-Input Relay Design for More Compact Implementation of Digital Logic Circuits," *IEEE Electron Device Letters*, 2012.
 - [102] V. Pott, H. Kam, J. Jeon, and T.-J. K. Liu, "Improvement in mechanical contact reliability with ALD TiO₂ coating," in *AVS 56th International Symposium & Exhibition*, pp. 8-13, 2009.
 - [103] J. Jeon, T.-J. K. Liu, and W. Kwon, "Embedded Memory Capability of Four-Terminal Relay Technology," *IEEE Transactions on Electron Devices*, 2011.
 - [104] H. Kam, T.-J. K. Liu, V. Stojanović, D. Markovic, and E. Alon, "Design, Optimization, and Scaling of MEM Relays for Ultra-Low-Power Digital Logic," *IEEE Transactions on Electron Devices*, 2011.
 - [105] V. Pott, H. Kam, R. Nathanael, and J. Jeon, "Design and reliability of a micro-relay technology for zero-standby-power digital logic applications," in *IEEE International Electron Devices Meeting (IEDM)*, 2009.
 - [106] H. Fariborzi, T.-J. K. Liu, F. Chen, V. Stojanović, R. Nathanael, and J. Jeon, "Design and demonstration of micro-electro-mechanical relay multipliers," in *IEEE Asian Solid State Circuits Conference (A-SSCC)*, pp. 117-120, 2011.
 - [107] E. Alon, T.-J. K. Liu, V. Pott, F. Chen, M. Spencer, R. Nathanael, C. Wang, H. Fariborzi, A. Gupta, H. Kam, J. Jeon, D. Markovic, and V. Stojanović, "Demonstration of integrated micro-electro-mechanical switch circuits for VLSI applications," in *IEEE International Solid-*

- State Circuits Conference Digest of Technical Papers (ISSCC)*, pp. 150-151, 2010.
- [108] T.-J. K. Liu, H. Kam, E. Alon, and M. Horowitz, "Circuit-level requirements for MOSFET-replacement devices," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 1-1, 2008.
 - [109] T.-J. K. Liu, Y. Chen, R. Nathanael, J. Jeon, J. Yaung, and L. Hutin, "Characterization of Contact Resistance Stability in MEM Relays With Tungsten Electrodes," *Journal of Microelectromechanical Systems*, 2012.
 - [110] D. Lee, V. Pott, H. Kam, R. Nathanael, and T.-J. K. Liu, "AFM characterization of adhesion force in micro-relays," in *IEEE 23rd International Conference on Micro Electro Mechanical Systems (MEMS)*, pp. 232-235, 2009.
 - [111] R. Mewaldt, A. Davis, W. Binns, G. de Nolfo, J. George, M. Israel, R. Leske, E. Stone, M. Wiedenbeck, and T. von Rosenvinge, "The Cosmic Ray Radiation Dose in Interplanetary Space Present Day and Worst-Case Evaluations," in *International Cosmic Ray Conference*, p. 433, 2005.
 - [112] R. Parsa, H.-S. P. Wong, W. S. Lee, M. Shavezipur, J. Provine, R. Maboudian, S. Mitra, and R. T. Howe, "Laterally Actuated Platinum-Coated Polysilicon NEM Relays," *Journal of Microelectromechanical Systems*, vol. 22, pp. 768-778, 2013.
 - [113] W. S. Lee, S. Chong, R. Parsa, J. Provine, D. Lee, S. Mitra, H.-S. P. Wong, and R. T. Howe, "Dual sidewall lateral nanoelectromechanical relays with beam isolation," in *International Solid-State Sensors, Actuators and Microsystems Conference, TRANSDUCERS*, pp. 2606-2609, 2011.
 - [114] M. Shavezipur, K. Harrison, W. S. Lee, S. Mitra, H.-S. P. Wong, and R. T. Howe, "Partitioning Electrostatic and Mechanical Domains in Nanoelectromechanical Relays," *Journal of Microelectromechanical Systems*, 2014.
 - [115] M. Shavezipur, W. S. Lee, K. L. Harrison, J. Provine, S. Mitra, H.-S. P. Wong, and R. T. Howe, "Laterally actuated nanoelectromechanical relays with compliant, low resistance contact," in *IEEE 26th International Conference on Micro Electro Mechanical Systems (MEMS)*, pp. 520-523, 2013.
 - [116] D. A. Czapslewski, G. A. Patrizi, G. M. Kraus, J. R. Wendt, C. D. Nordquist, S. L. Wolfley, M. S. Baker, and M. P. de Boer, "A nanomechanical switch for integration with CMOS logic," *Journal of Micromechanics and Microengineering*, vol. 19, p. 085003, 2009.

- [117] D. A. Czaplewski, G. M. Kraus, and C. D. Nordquist, "Nanomechanical switches for power saving in CMOS applications," *Electronics Letters*, vol. 45, p. 550, 2009.
- [118] J. O. Lee, M.-W. Kim, S.-D. Ko, H.-O. Kang, W.-H. Bae, M.-H. Kang, K.-N. Kim, D.-E. Yoo, and J.-B. Yoon, "3-terminal nanoelectromechanical switching device in insulating liquid media for low voltage operation and reliability improvement," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 1-4, 2009.
- [119] W. W. Jang, J. O. Lee, J.-B. Yoon, M.-S. Kim, J.-M. Lee, S.-M. Kim, K.-H. Cho, D.-W. Kim, D. Park, and W.-S. Lee, "Fabrication and characterization of a nanoelectromechanical switch with 15-nm-thick suspension air gap," *Applied Physics Letters*, vol. 92, p. 103110, 2008.
- [120] W. W. Jang, J.-B. Yoon, M.-S. Kim, J.-M. Lee, S.-M. Kim, E.-J. Yoon, K.-H. Cho, S.-Y. Lee, I.-H. Choi, D.-W. Kim, and D. Park, "NEMS switch with 30nm-thick beam and 20nm-thick air-gap for high density non-volatile memory applications," *Solid-State Electronics*, vol. 52, pp. 1578-1583, 2008.
- [121] M. Spencer, F. Chen, R. Nathanael, V. Pott, T.-J. K. Liu, E. Alon, C. Wang, H. Fariborzi, A. Gupta, H. Kam, J. Jeon, D. Markovic, and V. Stojanović, "Demonstration of Integrated Micro-Electro-Mechanical Relay Circuits for VLSI Applications," *IEEE Journal of Solid-State Circuits*, 2011.
- [122] H. Fariborzi, "Design and Demonstration of Integrated Micro-Electro-Mechanical Relay Circuits for VLSI Applications " Ph.D Thesis, University of California, Berkeley, 2013.
- [123] B. W. Soon, E. J. Ng, Y. Qian, N. Singh, M. Julius Tsai, and C. Lee, "A bi-stable nanoelectromechanical non-volatile memory based on van der Waals force," *Applied Physics Letters*, vol. 103, p. 053122, 2013.
- [124] B. W. Soon, N. Singh, J. M. Tsai, and C. Lee, "Fabrication and characterization of a silicon nanofin non-volatile memory," in *The 17th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII)*, pp. 892-895, 2013.
- [125] B. W. Soon, N. Singh, J. M. Tsai, and C. Lee, "A bi-stable silicon nanofin nanoelectromechanical switch based on van der Waals force for non-volatile memory applications," in *8th IEEE International Conference on Nano/Micro Engineered and Molecular Systems (NEMS)*, pp. 562-565, 2013.
- [126] B. W. Soon, E. J. Ng, N. Singh, J. M. Tsai, Y. Qian, and C. Lee, "A Bistable Electrostatic Silicon Nanofin Relay for Nonvolatile Memory Application," *Journal of Microelectromechanical Systems*, vol. 22, pp. 1004-1006, 2013.

- [127] S. K. Manohar, R. Venkatasubramanian, and P. T. Balsara, "Heterogeneous NEMS-CMOS DCM Buck Regulator for Improved Area and Enhanced Power Efficiency," *IEEE Transactions on Nanotechnology*, p. 1, 2014.
- [128] C. Chen, W. S. Lee, R. Parsa, S. Chong, J. Provine, J. Watt, R. T. Howe, H.-S. P. Wong, and S. Mitra, "Nano-Electro-Mechanical relays for FPGA routing: Experimental demonstration and a design technique," in *Design, Automation, Test in Europe Conference Exhibition (DATE)*, pp. 1361-1366, 2012.
- [129] J. Cheng, J. Zhe, and X. T. Wu, "Analytical and finite element model pull-in study of rigid and deformable electrostatic microactuators," *Journal of Micromechanics and Microengineering*, vol. 14, pp. 57-68, 2004.
- [130] COMSOL. (2013, Sep 10). Pull-in of an RF MEMS Switch. 1-18. Available: www.comsol.com/model/pull-in-of-an-rf-mems-switch-16379.
- [131] S. Pamidighantam, R. Puers, and K. Baert, "Pull-in voltage analysis of electrostatically actuated beam structures with fixed-fixed and fixed-free end conditions," *Journal of Micromechanics and Microengineering*, 2002.
- [132] L. C. Wei, A. B. Mohammad, and N. M. Kassim, "Analytical modeling for determination of pull-in voltage for an electrostatic actuated MEMS cantilever beam," in *Semiconductor Electronics, 2002. Proceedings. ICSE 2002. IEEE International Conference on*, pp. 233-238, 2002.
- [133] M. Dequesnes, S. V. Rotkin, and N. R. Aluru, "Calculation of pull-in voltages for carbon-nanotube-based nanoelectromechanical switches," *Nanotechnology*, 2002.
- [134] S. Chowdhury, M. Ahmadi, and W. C. Miller, "A closed-form model for the pull-in voltage of electrostatically actuated cantilever beams," *Journal of Micromechanics and Microengineering*, vol. 15, pp. 756-763, 2005.
- [135] S. Chowdhury and M. Ahmadi, "A comparison of pull-in voltage calculation methods for MEMS-based electrostatic actuator design," in *1st International Conference on Sensing Technology*, Palmerston North, New Zealand, 2005.
- [136] Z. Zhang, M. Kamon, and L. Daniel, "Continuation-Based Pull-In and Lift-Off Simulation Algorithms for Microelectromechanical Devices," *Journal of Microelectromechanical Systems*, vol. 23, pp. 1084-1093, 2014.

- [137] W. M. Zhang, H. Yan, Z. K. Peng, and G. Meng, "Electrostatic pull-in instability in MEMS/NEMS: A review," *Sensors and Actuators a-Physical*, vol. 214, pp. 187-218, 2014.
- [138] R. K. Gupta, "Electrostatic pull-in test structure design for in-situ mechanical property measurements of microelectromechanical systems (MEMS)," Massachusetts Institute of Technology, 1998.
- [139] S.-U. Hwang, J.-M. Choi, H.-H. Yang, C.-H. Kim, C. Jung, H. Gyu Park, Y.-K. Choi, and J.-B. Yoon, "Electrostatic switching biosensor - a novel label-free DNA detection using an electrode charging technique," in *IEEE 24th International Conference on Micro Electro Mechanical Systems (MEMS)*, pp. 857-860, 2011.
- [140] G. O'Brien, D. J. Monk, and L. Lin, "MEMS cantilever beam electrostatic pull-in model," in *Proc. SPIE 4593, Design, Characterization, and Packaging for MEMS and Microelectronics II*, 2001.
- [141] S. Gorthi, A. Mohanty, and A. Chatterjee, "MEMS Parallel Plate Actuators: Pull-in, Pull-out and Other Transitions," in *International Conference on MEMS and Semiconductor Nanotechnology*, IIT Kharagpur, India, 2005.
- [142] O. Degani, E. Socher, A. Lipson, T. Lejtner, D. J. Setter, S. Kaldor, and Y. Nemirovsky, "Pull-in study of an electrostatic torsion microactuator," *Journal of Microelectromechanical Systems*, vol. 7, pp. 373-379, 1998.
- [143] S. Chowdhury and M. Ahmadi, "Pull-in voltage calculations for MEMS sensors with cantilevered beams," *The 3rd International IEEE-NEWCAS Conference*, 2005.
- [144] W. W. Jang, J. O. Lee, and J.-B. Yoon, "A Dram-Like Mechanical Non-Volatile Memory," in *International Solid-State Sensors, Actuators and Microsystems Conference, TRANSDUCERS*, pp. 2187-2190, 2007.
- [145] W. W. Jang, O. D. Kwon, J. O. Lee, and J.-B. Yoon, "Microelectromechanical (MEM) switch and inverter for digital IC applications," in *IEEE Asian Solid-State Circuits Conference (ASSCC)*, pp. 256-259, 2007.
- [146] T. Akashi, H. Funabashi, and Y. Nonomura, "A mushroom-shaped convex poly-Si structure for preventing z-directional stiction of an SOI-MEMS device," in *IEEE 24th International Conference on Micro Electro Mechanical Systems (MEMS)*, pp. 201-204, 2011.
- [147] W. Xiang and C. Lee, "Nanoelectromechanical torsion switch of low operation voltage for nonvolatile memory application," *Applied Physics Letters*, vol. 96, p. 193113, 2010.

- [148] A. Fruehling, S. Xiao, M. Qi, K. Roy, and D. Peroulis, "Nano-switch for study of gold contact behavior," in *IEEE Sensors*, pp. 248-251, 2009.
- [149] K. M. Hurst, N. Ansari, C. B. Roberts, and W. R. Ashurst, "Self-Assembled Monolayer-Immobilized Gold Nanoparticles as Durable, Anti-Stiction Coatings for MEMS," *Journal of Microelectromechanical Systems*, 2011.
- [150] A. Broue, T. Fourcade, J. Dhennin, F. Courtade, P. L. Charvet, P. Pons, X. Lafontan, and R. Plana, "Validation of bending tests by nanoindentation for micro-contact analysis of MEMS switches," *Journal of Micromechanics and Microengineering*, vol. 20, p. 085025, 2010.
- [151] F. Streller, G. E. Wabiszewski, and R. Carpick, "Development and assessment of next-generation nanoelectromechanical switch contact materials," in *International Conference on Nanotechnology (IEEE-NANO)*, pp. 141-145, 2014.
- [152] R. Parsa, M. Shavezipur, W. S. Lee, S. Chong, D. Lee, H.-S. P. Wong, R. Maboudian, and R. T. Howe, "Nanoelectromechanical relays with decoupled electrode and suspension," in *IEEE 24th International Conference on Micro Electro Mechanical Systems (MEMS)*, pp. 1361-1364, 2011.
- [153] V. Brand, M. P. Boer, and M. S. Baker, "Contamination Thresholds of Pt- and -Coated Ohmic Switches," *Journal of Microelectromechanical Systems*, 2013.
- [154] M. P. de Boer, D. A. Czaplewski, M. S. Baker, S. L. Wolfley, and J. A. Ohlhausen, "Design, fabrication, performance and reliability of Pt- and RuO₂-coated microrelays tested in ultra-high purity gas environments," *Journal of Micromechanics and Microengineering*, vol. 22, p. 105027, 2012.
- [155] D. A. Czaplewski, C. D. Nordquist, G. A. Patrizi, G. M. Kraus, and W. D. Cowan, "RF MEMS Switches With RuO₂-Au Contacts Cycled to 10 Billion Cycles," *Journal of Microelectromechanical Systems*, 2013.
- [156] F. Cardarelli, *Materials handbook: a concise desktop reference*: Springer, 2008.
- [157] V. Pott, R. Vaddi, G. L. Chua, J. T. M. Lin, and T. T.-H. Kim, "Design Optimization of Pulsed-Mode Electromechanical Nonvolatile Memory," *IEEE Electron Device Letters*, 2012.
- [158] V. Pott, G. L. Chua, R. Vaddi, J. M. Tsai, and T. T.-H. Kim, "The Shuttle Nanoelectromechanical Nonvolatile Memory," *IEEE Transactions on Electron Devices*, 2012.

- [159] A. T. Do, J. K. Gopal, P. Singh, G. L. Chua, K. S. Yeo, and T. T.-H. Kim, "Design and array implementation a cantilever-based non-volatile memory utilizing vibrational reset," in *Proceedings of the European Solid-State Device Research Conference (ESSDERC)*, pp. 284-287, 2013.
- [160] P. Singh, G. L. Chua, Y. S. Liang, K. G. Jayaraman, A. T. Do, and T. T. H. Kim, "Anchor-free NEMS non-volatile memory cell for harsh environment data storage," *Journal of Micromechanics and Microengineering*, vol. 24, 2014.
- [161] M.-W. Kim, Y.-H. Song, S.-D. Ko, S.-J. Ahn, and J.-B. Yoon, "Ultra-low voltage MEMS switch using a folded hinge structure," *Micro and Nano Systems Letters*, vol. 2, 2014.
- [162] Y. Qian, K.-T. Lam, C. Lee, and G. Liang, "The effects of interlayer mismatch on electronic properties of bilayer armchair graphene nanoribbons," *Carbon*, vol. 50, pp. 1659-1666, 2012.
- [163] K.-T. Lam, M. Stephen Leo, C. Lee, and G. Liang, "Design evaluation of graphene nanoribbon nanoelectromechanical devices," *Journal of Applied Physics*, vol. 110, p. 024302, 2011.
- [164] K.-T. Lam, C. Lee, and G. Liang, "Bilayer graphene nanoribbon nanoelectromechanical system device: A computational study," *Applied Physics Letters*, vol. 95, pp. -, 2009.
- [165] S.-M. Kim, E. B. Song, S. Lee, S. Seo, D. H. Seo, Y. Hwang, R. Candler, and K. L. Wang, "Suspended few-layer graphene beam electromechanical switch with abrupt on-off characteristics and minimal leakage current," *Applied Physics Letters*, vol. 99, p. 023103, 2011.
- [166] Z. Shi, H. Lu, L. Zhang, R. Yang, Y. Wang, D. Liu, H. Guo, D. Shi, H. Gao, E. Wang, and G. Zhang, "Studies of graphene-based nanoelectromechanical switches," *Nano Research*, vol. 5, pp. 82-87, 2011.
- [167] K. I. Bolotin, C. Chen, S. Rosenblatt, P. Kim, I. Kymissis, H. L. Stormer, T. F. Heinz, and J. Hone, "NEMS applications of graphene," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 1-4, 2009.
- [168] P. Li, Z. You, and T. Cui, "Graphene cantilever beams for nano switches," *Applied Physics Letters*, vol. 101, p. 093111, 2012.
- [169] K. M. Milaninia, M. A. Baldo, A. Reina, and J. Kong, "All graphene electromechanical switch fabricated by chemical vapor deposition," *Applied Physics Letters*, vol. 95, p. 183105, 2009.

- [170] S. W. Lee, D. S. Lee, R. E. Morjan, S. H. Jhang, M. Sveningsson, O. A. Nerushev, Y. W. Park, and E. E. B. Campbell, "A Three-Terminal Carbon Nanorelay," *Nano Letters*, vol. 4, pp. 2027-2030, 2004.
- [171] A. R. Hall, S. Paulson, T. Cui, J. P. Lu, L.-C. Qin, and S. Washburn, "Torsional electromechanical systems based on carbon nanotubes," *Reports on Progress in Physics*, vol. 75, p. 116501, 2012.
- [172] J. W. Kang, J. Ha Lee, H. Joo Lee, and H. J. Hwang, "A study on carbon nanotube bridge as a electromechanical memory device," *Physica E: Low-dimensional Systems and Nanostructures*, vol. 27, pp. 332-340, 2005.
- [173] J. Cao, W. A. Vitale, and A. M. Ionescu, "Self-assembled nano-electro-mechanical tri-state carbon nanotube switches for reconfigurable integrated circuits," in *Micro Electro Mechanical Systems (MEMS), 2012 IEEE 25th International Conference on*, pp. 188-191, 2012.
- [174] H. F. Dadgour, A. M. Cassell, and K. Banerjee, "Scaling and variability analysis of CNT-based NEMS devices and circuits with implications for process design," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 1-4, 2008.
- [175] O. Y. Loh, X. Wei, C. Ke, J. Sullivan, and H. D. Espinosa, "Robust Carbon-Nanotube-Based Nano-electromechanical Devices: Understanding and Eliminating Prevalent Failure Modes Using Alternative Electrode Materials," *Small*, vol. 7, pp. 79-86, 2010.
- [176] M.-W. Jang, C.-L. Chen, W. E. Partlo, S. R. Patil, D. Lee, Z. Ye, D. Lilja, T. A. Taton, T. Cui, and S. A. Campbell, "A pure single-walled carbon nanotube thin film based three-terminal microelectromechanical switch," *Applied Physics Letters*, vol. 98, p. 073502, 2011.
- [177] J. E. Jang, S. N. Cha, Y. J. Choi, G. A. J. Amaratunga, D. J. Kang, D. G. Hasko, J. E. Jung, and J. M. Kim, "Nanoscale capacitors based on metal-insulator-carbon nanotube-metal structures," *Applied Physics Letters*, vol. 87, p. 263103, 2005.
- [178] J. E. Jang, S. N. Cha, Y. J. Choi, G. A. J. Amaratunga, D. J. Kang, D. G. Hasko, J. E. Jung, and J. M. Kim, "Nanoelectromechanical switches with vertically aligned carbon nanotubes," *Applied Physics Letters*, vol. 87, pp. 163114-163114, 2005.
- [179] J. Choi, J.-I. Lee, Y. Eun, M.-O. Kim, and J. Kim, "Microswitch with self-assembled carbon nanotube arrays for high current density and reliable contact," in *Micro Electro Mechanical Systems (MEMS), 2011 IEEE 24th International Conference on*, pp. 87-90, 2011.

- [180] T. Yamada, N. Makiomoto, A. Sekiguchi, Y. Yamamoto, K. Kobashi, Y. Hayamizu, Y. Yomogida, H. Tanaka, H. Shima, H. Akinaga, D. N. Futaba, and K. Hata, "Hierarchical Three-Dimensional Layer-by-Layer Assembly of Carbon Nanotube Wafers for Integrated Nanoelectronic Devices," *Nano Letters*, vol. 12, pp. 4540-4545, 2012.
- [181] S. N. Cha, J. E. Jang, Y. J. Choi, G. A. J. Amaratunga, D. J. Kang, D. G. Hasko, J. E. Jung, and J. M. Kim, "Fabrication of a nanoelectromechanical switch using a suspended carbon nanotube," *Applied Physics Letters*, vol. 86, p. 083105, 2005.
- [182] L. Maslov, "Concept of nonvolatile memory based on multiwall carbon nanotubes," *Nanotechnology*, vol. 17, pp. 2475-2482, 2006.
- [183] M. Y. A. Yousif, P. Lundgren, F. Ghavanini, P. Enoksson, and S. Bengtsson, "CMOS considerations in nanoelectromechanical carbon nanotube-based switches," *Nanotechnology*, vol. 19, p. 285204, 2008.
- [184] J. M. Kinaret, T. Nord, and S. Viefers, "A carbon-nanotube-based nanorelay," *Applied Physics Letters*, vol. 82, p. 1287, 2003.
- [185] J. Choi, J.-I. Lee, Y. Eun, M.-O. Kim, and J. Kim, "Aligned Carbon Nanotube Arrays for Degradation-Resistant, Intimate Contact in Micromechanical Devices," *Advanced Materials*, vol. 23, pp. 2231-2236, 2011.
- [186] S. W. Lee, S. J. Park, E. E. B. Campbell, and Y. W. Park, "A fast and low-power microelectromechanical system-based non-volatile memory device," *Nature Communications*, vol. 2, pp. 220-6, 2011.
- [187] O. Y. Loh and H. D. Espinosa, "Nanoelectromechanical contact switches," *Nature Nanotechnology*, vol. 7, pp. 283-295, 2012.
- [188] J. E. Jang, S. N. Cha, Y. J. Choi, T. P. Butler, D. J. Kang, D. G. Hasko, J. E. Jung, Y. W. Jin, J. M. Kim, and G. A. J. Amaratunga, "Nanoelectromechanical switch with low voltage drive," *Applied Physics Letters*, vol. 93, p. 113105, 2008.
- [189] Comsol, "COMSOL multiphysics user's guide," *Version: September*, 2005.
- [190] Y. Fukuta, H. Fujita, and H. Toshiyoshi, "Vapor Hydrofluoric Acid Sacrificial Release Technique for Micro Electro Mechanical Systems Using Labware," *Japanese Journal of Applied Physics*, vol. 42, pp. 3690-3694, 2003.
- [191] X. L. Feng, M. H. Matheny, C. A. Zorman, M. Mehregany, and M. L. Roukes, "Low Voltage Nanoelectromechanical Switches Based on Silicon Carbide Nanowires," *Nano Letters*, vol. 10, pp. 2891-2896, 2010.

- [192] T. He, R. Yang, S. Rajgopal, M. A. Tupta, S. Bhunia, M. Mehregany, and P. X.-L. Feng, "Robust silicon carbide (SiC) nanoelectromechanical switches with long cycles in ambient and high temperature conditions," in *IEEE 26th International Conference on Micro Electro Mechanical Systems (MEMS)*, ed: IEEE, pp. 516-519, 2013.
- [193] T.-H. Lee, S. Bhunia, and M. Mehregany, "Electromechanical Computing at 500 C with Silicon Carbide," *Science*, vol. 329, pp. 1316-1318, 2010.
- [194] T.-H. Lee, S. Bhunia, and M. Mehregany, "Electromechanical computing at 500 degrees C with silicon carbide.," *Science*, vol. 329, pp. 1316-8, 2010.
- [195] M. Mehregany, T. He, R. Yang, V. Ranganathan, S. Rajgopal, M. A. Tupta, S. Bhunia, and X. L. Feng, "Silicon carbide (SiC) nanoelectromechanical switches and logic gates with long cycles and robust performance in ambient air and at high temperature," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 4-4.6.4, 2013.
- [196] M. Mehregany and T. H. Lee, "Silicon Carbide NEMS Logic for High Temperature Applications," *Micro- and Nanotechnology Sensors, Systems, and Applications II*, vol. 7679, 2010.
- [197] X. Wang, S. Narasimhan, A. Krishna, F. G. Wolff, S. Rajgopal, T.-H. Lee, M. Mehregany, and S. Bhunia, "High-temperature (>500°C) reconfigurable computing using silicon carbide NEMS switches," in *Design, Automation & Test in Europe Conference & Exhibition (DATE), 2011*, pp. 1-6, 2011.
- [198] C. Chen, S. Lee, J. Provine, S. Chong, R. Parsa, D. Lee, R. T. Howe, H.-S. P. Wong, and S. Mitra, "Nano-Electro-Mechanical (NEM) relays and their application to FPGA routing," in *17th Asia and South Pacific Design Automation Conference (ASP-DAC)*, pp. 639-639, 2012.
- [199] C. Dong, C. Chen, S. Mitra, and D. Chen, "Architecture and performance evaluation of 3D CMOS-NEM FPGA," *13th International Workshop on System Level Interconnect Prediction (SLIP)*, pp. 1-8, 2011.
- [200] S. Han, V. Sirigiri, D. G. Saab, and M. Tabid-Azar, "Ultra-low power NEMS FPGA," in *IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, pp. 533-538, 2012.
- [201] K. V. Sirigiri, K. Alzoubi, D. G. Saab, F. Kocan, and M. Tabid-Azar, "Ultra-low-Power Ultra-fast Hybrid CNEMS-CMOS FPGA," in *International Conference on Field Programmable Logic and Applications (FPL)*, 2010.

- [202] H. F. Dadgour and K. Banerjee, "Hybrid NEMS-CMOS integrated circuits: A novel strategy for energy-efficient designs," *Computers Digital Techniques, IET*, vol. 3, pp. 593-608, 2009.
- [203] S. Chong, B. Lee, K. B. Parizi, J. Provine, S. Mitra, R. T. Howe, and H.-S. P. Wong, "Integration of nanoelectromechanical (NEM) relays with silicon CMOS with functional CMOS-NEM circuit," in *IEEE International Electron Devices Meeting (IEDM)*, pp. 30-30.5.4, 2011.
- [204] S. Chong, H.-S. P. Wong, B. Lee, S. Mitra, and R. T. Howe, "Integration of Nanoelectromechanical Relays With Silicon nMOS," *IEEE Transactions on Electron Devices*, 2012.
- [205] S. Nitta, D. Edelstein, S. Ponoht, L. Clevenger, X. Liu, and T. Standaert, "Performance and reliability of airgaps for advanced BEOL Interconnects," in *Interconnect Technology Conference, 2008. IITC 2008. International*, pp. 191-192, 2008.
- [206] J. O. Lee, Y.-H. Song, M.-W. Kim, M.-H. Kang, J.-S. Oh, H.-H. Yang, and J.-B. Yoon, "A sub-1-volt nanoelectromechanical switching device," *Nature Nanotechnology*, pp. 1-5, 2012.
- [207] A. Subramanian, L. X. Dong, B. J. Nelson, and A. Ferreira, "Supermolecular switches based on multiwalled carbon nanotubes," *Applied Physics Letters*, vol. 96, p. 073116, 2010.
- [208] V. Beiu, W. Ibrahim, M. Tache, and T. J. K. Liu, "On ultra-low power hybrid NEMS-CMOS," in *International Conference on Nanotechnology (IEEE-NANO)*, pp. 201-206, 2014.
- [209] H. F. Dadgour and K. Banerjee, "Design and Analysis of Hybrid NEMS-CMOS Circuits for Ultra Low-Power Applications," in *44th ACM/IEEE Design Automation Conference (DAC)*, New York, New York, USA, pp. 306-311, 2007.
- [210] S. K. Manohar, R. Venkatasubramanian, and P. T. Balsara, "Hybrid NEMS-CMOS DC-DC Converter for Improved Area and Power Efficiency," in *25th International Conference on VLSI Design (VLSID)*, pp. 221-226, 2012.
- [211] Q. Xia, W. Robinett, M. W. Cumbie, N. Banerjee, T. J. Cardinali, J. J. Yang, W. Wu, X. Li, W. M. Tong, D. B. Strukov, G. S. Snider, G. Medeiros-Ribeiro, and R. S. Williams, "Memristor-CMOS Hybrid Integrated Circuits for Reconfigurable Logic," *Nano Letters*, vol. 9, pp. 3640-3645, 2009.
- [212] D. A. Czaplewski, C. D. Nordquist, C. W. Dyck, G. A. Patrizi, G. M. Kraus, and W. D. Cowan, "Lifetime limitations of ohmic, contacting RF MEMS switches with Au, Pt and Ir contact materials due to accumulation of 'friction polymer' on the contacts," *Journal of Micromechanics and Microengineering*, vol. 22, p. 105005, 2012.

- [213] D. A. Czaplewski, M. P. Boer, G. A. Patrizi, G. M. Kraus, J. R. Wendt, C. D. Nordquist, S. L. Wolfley, and M. S. Baker, "A nanomechanical switch for integration with CMOS logic," *Journal of Micromechanics and Microengineering*, vol. 19, p. 085003, 2009.
- [214] T.-J. K. Liu, J. Jeon, V. Pott, H. Kam, R. Nathanael, and E. Alon, "Seesaw Relay Logic and Memory Circuits," *Journal of Microelectromechanical Systems*, vol. 19, pp. 1012-1014, 2010.
- [215] P. G. Neudeck, R. S. Okojie, and L. Y. Chen, "High-temperature electronics - A role for wide bandgap semiconductors?," *Proceedings of the IEEE*, vol. 90, pp. 1065-1076, 2002.
- [216] P. G. Neudeck, M. J. Krasowski, L. Y. Chen, and N. F. Prokop, "Characterization of 6H-SiC JFET Integrated Circuits Over A Broad Temperature Range from-150 degrees C to+500 degrees C," *Silicon Carbide and Related Materials 2009, Pts 1 and 2*, vol. 645-648, pp. 1135-1138, 2010.
- [217] M. Enachescu, M. Lefter, A. Bazigos, A. M. Ionescu, and S. Dan Cotofana, "Ultra low power NEMFET based logic," *IEEE International Symposium on Circuits and Systems (ISCAS2013)*, pp. 566-569, 2013.
- [218] D. Lee, W. S. Lee, C. Chen, F. Fallah, J. Provine, S. Chong, J. Watkins, R. T. Howe, H.-S. P. Wong, and S. Mitra, "Combinational Logic Design Using Six-Terminal NEM Relays," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 32, pp. 653-666, 2013.
- [219] R. Venkatasubramanian, S. K. Manohar, and P. T. Balsara, "NEM Relay-Based Sequential Logic Circuits for Low-Power Design," *IEEE Transactions on Nanotechnology*, vol. 12, pp. 386-398, 2013.
- [220] U. Zaghloul and G. Piazza, "10–25 NM piezoelectric nano-actuators and NEMS switches for millivolt computational logic," in *IEEE 26th International Conference on Micro Electro Mechanical Systems (MEMS)*, ed: IEEE, pp. 233-236, 2013.
- [221] O. Y. Loh and H. D. Espinosa, "Nanoelectromechanical contact switches," *Nature Nanotechnology*, vol. 7, pp. 283-295, 2012.
- [222] S. W. Lee, S. J. Park, E. E. B. Campbell, and Y. W. Park, "A fast and low-power microelectromechanical system-based non-volatile memory device.," *Nature communications*, vol. 2, p. 220, 2011.
- [223] X. L. Feng, M. H. Matheny, C. a. Zorman, M. Mehregany, and M. L. Roukes, "Low voltage nanoelectromechanical switches based on silicon carbide nanowires.," *Nano letters*, vol. 10, pp. 2891-6, 2010.
- [224] D. Grogg, U. Drechsler, A. Knoll, U. Duerig, Y. Pu, C. Hagleitner, and M. Despont, "Curved in-plane electromechanical relay for low power

- logic applications," *Journal of Micromechanics and Microengineering*, vol. 23, p. 025024, 2013.
- [225] T. J. W. Wagner and D. Vella, "Switch on, switch off: stiction in nanoelectromechanical switches.," *Nanotechnology*, vol. 24, p. 275501, 2013.
 - [226] T. He, J. Lee, Z. Wang, and X. L. Feng, "Interrogating contact-mode silicon carbide (SiC) nanoelectromechanical switching dynamics by ultrasensitive laser interferometry," in *Micro Electro Mechanical Systems (MEMS), 2014 IEEE 27th International Conference on*, 2014.
 - [227] T. He, V. Ranganathan, R. Yang, S. Rajgopal, S. Bhunia, M. Mehregany, and X. L. Feng, "Time-domain AC characterization of silicon carbide (SiC) nanoelectromechanical switches toward high-speed operations," in *The 17th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS & EUROSENSORS XXVII)*, pp. 669-672, 2013.
 - [228] T. He, R. Yang, S. Rajgopal, S. Bhunia, M. Mehregany, and X. L. Feng, "Dual-gate silicon carbide (SiC) lateral nanoelectromechanical switches," in *8th IEEE International Conference on Nano/Micro Engineered and Molecular Systems (NEMS)*, pp. 554-557, 2013.
 - [229] J. L. Muñoz-Gamarra, A. Uranga, and N. Barniol, "Nanomechanical switches based on metal-insulator-metal capacitors from a standard complementary-metal-oxide semiconductor technology," *Applied Physics Letters*, vol. 104, p. 243105, 2014.
 - [230] J. L. Muñoz-Gamarra, G. Vidal-Álvarez, F. Torres, A. Uranga, and N. Barniol, "CMOS-MEMS switches based on back-end metal layers," *Microelectronic Engineering*, 2014.
 - [231] D. Grogg, U. Drechsler, A. Knoll, U. Duerig, Y. Pu, C. Hagleitner, and M. Despont, "Curved in-plane electromechanical relay for low power logic applications," *Journal of Micromechanics and Microengineering*, vol. 23, p. 025024, 2013.
 - [232] T. Wang, L. Lou, and C. Lee, "A Junctionless Gate-All-Around Silicon Nanowire FET of High Linearity and Its Potential Applications," *Electron Device Letters, IEEE*, vol. 34, pp. 478-480, 2013.

Appendix I: Process Flow of U-Shaped NEMS Switches

1	Laser Mark
2	Cleaning: SC 1+ 1kW Megasonic + Quick Dump Rinser + DHF(1:200)-120s + Isopropyl Alcohol Dry
3	Implantation: BF ₂ , 1E14, 15keV, Tilt 7, Twist 22
4	Annealing: Implant activation (1050 °C ,30sec)
5	Lithography: 3200 Å with BARC; Dose = 54; Focus = 0.15
6	Critical dimension measurement
7	Etching Si: 80 sec
8	Photoresist strip (O ₂ + N ₂ at 250°C)
9	Cleaning: Piranha 10 minutes
10	Cleaning: DHF 1:100, 10s
11	Deposition: 400 nm PECVD SiO ₂
12	Lithography: 5500Å without BARC; Dose = 30; Focus = 0
13	Etching SiO ₂ : stop on Si

Appendix

14	Photoresist strip ($O_2 + N_2$ at $250^\circ C$)
15	Cleaning: Piranha 10 minutes
16	Deposition: Argon sputtering (15 secs) + 250\AA -TaN + $7.5k\text{\AA}$ - Al
17	Lithography: $2\text{ }\mu m$ with BARC; Dose = 36; Focus = -0.2
18	Etching metal: $7.5k\text{\AA}$ - Al+ 250\AA -TaN+ In-situ Photoresist strip
19	Photoresist strip ($O_2 + N_2$ at $250^\circ C$)
20	Metal sintering: $420^\circ C$, 30 minutes

Appendix II: Process Flow of All Metal Based NEMS Switches

1	Laser Mark
2	Cleaning: SC 1 + 1kW Megasonic + Quick Dump Rinser + DHF(1:200)-120s + Isopropyl Alcohol Dry
3	Deposition: 1 μm PECVD SiO_2
4	Lithography: 3200 Å with BARC; Dose = 52; Focus = 0
5	Etching SiO_2 : 48s
6	Photoresist strip (O_2 + N_2 at 250°C)
7	Cleaning: Piranha 5 minutes
8	Wet etching: DHF 1:7, 50s
9	Cleaning: Piranha 5 minutes
10	Deposition: PVD 300 nm Mo
11	Deposition: NH_3 treatment + HDP PECVD 500 nm SiO_2
12	CMP: CMP SiO_2 stop on MO
13	Etching Mo: 55s

Appendix III: Process Flow of Encapsulated All Metal Based NEMS Switches

1	Laser Mark
2	Cleaning: SC 1 + 1kW Megasonic + Quick Dump Rinser + DHF(1:200)-120s + Isopropyl Alcohol Dry
3	Deposition: 1 μm PVD AlN
4	Deposition: 1 μm PECVD SiO ₂
5	Lithography: 3200 Å with BARC; Dose = 52; Focus = 0
6	Etching SiO ₂ : 48s
7	Photoresist strip (O ₂ + N ₂ at 250°C)
8	Cleaning: Piranha 5 minutes
9	Wet etching: DHF 1:7, 50s
10	Cleaning: Piranha 5 minutes
11	Deposition: PVD 300 nm Mo
12	Deposition: NH ₃ treatment + HDP PECVD 500 nm SiO ₂
13	CMP: CMP SiO ₂ stop on MO

14	Etching Mo: 55s
15	Deposition: HDP PECVD 800 nm SiO ₂
16	CMP: CMP SiO ₂ 500 nm
17	Lithography: 1 μ m with BARC; Dose = 32; Focus = 0
18	Etching SiO ₂ : Stop on Mo
19	Photoresist strip (O ₂ + N ₂ at 250°C)
20	Cleaning: Post etching polymer removal
21	Deposition: PVD 500 nm AlN
22	Deposition: PECVD 50 nm SiO ₂
23	Lithography: 1 μ m with BARC; Dose = 32; Focus = 0
24	Etching SiO ₂ : Stop on AlN
25	Etching AlN: Stop on SiO ₂
26	Photoresist strip (O ₂ + N ₂ at 250°C)
27	Cleaning: Post etching polymer removal
28	Release: VHF for 15 minutes
29	Deposition: PECVD 1 μ m SiO ₂
30	Lithography: 1 μ m with BARC; Dose = 32; Focus = 0

Appendix

31	Etching SiO ₂ : Stop on AlN
32	Etching AlN: Stop on Mo
33	Photoresist strip (O ₂ + N ₂ at 250°C)
34	Cleaning: Post etching polymer removal
35	Deposition: PVD 500 nm Al
36	Lithography: 1 μm with BARC; Dose = 32; Focus = 0
37	Etching metal: 7500 nm Al + In-situ Photoresist strip
38	Photoresist strip (O ₂ + N ₂ at 250°C)
39	Cleaning: Post etching polymer removal

Appendix IV: List of Publication

Journal Papers

- [1] **You Qian**, Bo Woon Soon, and Chengkuo Lee, “Pull-In Voltage and Fabrication Yield Analysis of All-Metal-Based Nanoelectromechanical Switches”, *IEEE/ASME J. Microelectromech. Syst.*, (minor revision)
- [2] Bo Woon Soon, **You Qian**, Eldwin J. Ng, Vu A. Hong , Yushi Yang, Chae Hyuck Ahn, Thomas W. Kenny, and Chengkuo Lee, “Investigation of a Vacuum Encapsulated Si-to-Si Contact Microswitch Operated from -60 °C to 400 °C”, *IEEE/ASME J. Microelectromech. Syst.*, (minor revision)
- [3] Prakash Pitchappa, LokeshDhakar, Chong Pei Ho, **You Qian**, Navab Singh and Chengkuo Lee, Periodic array of subwavelength MEMS cantilevers for dynamic manipulation of terahertz waves, *IEEE/ASME J. Microelectromech. Syst.*, to be published
- [4] Bo Woon Soon, Eldwin J. Ng, Vu A. Hong , Yushi Yang, Chae Hyuck Ahn, **You Qian**, Thomas W. Kenny, and Chengkuo Lee, “Fabrication and Characterization of a Vacuum Encapsulated Curved Beam Switch for Harsh Environment Application”, *IEEE/ASME J. Microelectromech. Syst.*, vol.23, No.5, pp. 1021-1030, 2014
- [5] Huicong Liu, **You Qian**, Nan Wang and Chengkuo Lee, “An In-Plane Approximated Nonlinear MEMS Electromagnetic Energy Harvester”, *IEEE/ASME J. Microelectromech. Syst.*, vol. 23, no. 3, pp. 740-749, 2014.
- [6] **You Qian**, Bo Woon Soon, Pushpapraj Singh, Humberto Campanella and Chengkuo Lee, “All Metal Nanoelectromechanical Switch Working At 300 °C For Rugged Electronics Applications”, *Nanoscale* vol. 6, no. 11, pp. 5606-5611, 2014.
- [7] Huicong Liu, **You Qian** and Chengkuo Lee, “A Multi-Frequency Vibration-Based MEMS Electromagnetic Energy Harvesting Device”, *Sens. Actuators A: Phys.*, vol. 204, pp. 37-43, 2013.
- [8] Bo Woon Soon, Eldwin Jiaqiang Ng, Navab Singh, Julius Minglin Tsai, **You Qian**, and Chengkuo Lee, “A Bistable Electrostatic Silicon Nanofin Relay for Nonvolatile Memory Application”, *IEEE/ASME J. Microelectromech. Syst.*, vol. 22, no. 5, pp. 1004-1006, 2013.
- [9] Bo Woon Soon, Eldwin Jiaqiang Ng, **You Qian**, Navab Singh, Julius Minglin Tsai, and Chengkuo Lee, , “A Bi-Stable Nanoelectromechanical Non-Volatile Memory Based on Van Der Waals Force”, *Appl. Phys. Lett.*, vol. 103, no. 5, 053122, 2013.

- [10] Fusheng Ma, **You Qian**, Yu-Sheng Lin, Hongwei Liu, Xinhai Zhang, Zhen Liu, Julius Ming-Lin Tsai and Chengkuo Lee, “Polarization-Sensitive Microelectromechanical Systems Based Tunable Terahertz Metamaterials Using Three Dimensional Electric Split-Ring Resonator Arrays”, *Appl. Phys. Lett.*, vol. 102, no. 16, 161912, 2013.
- [11] Yu-Sheng Lin, **You Qian**, Fusheng Ma, Zhen Liu, Piotr Kropelnicki, and Chengkuo Lee, “Development of Stress-Induced Curved Actuators for A Tunable Thz Filter Based on Double Split Ring Resonators”, *Appl. Phys. Lett.*, vol. 102, no. 11, 111908, 2013.
- [12] Kah How Koh, **You Qian** and Chengkuo Lee, “Design and Characterization of A 3-D MEMS VOA Driven by Hybrid Electromagnetic and Electrothermal Actuation Mechanisms”, *J. Micromech. Microeng.*, vol. 22, no. 10, 105031, 2012.
- [13] **You Qian**, Kai Tak Lam, Chengkuo Lee and Gengchiao Liang, “The Effect of Interlayer Mismatch on Electronic Properties of Bilayer Armchair Graphene Nanoribbons”, *Carbon*, vol. 50, no. 4, pp. 1659-1666, 2012.
- [14] **You Qian**, Liang Lou, Julius Ming-Lin Tsai and Chengkuo Lee, “A Dual-Silicon-Nanowires Based U-Shaped Nanoelectromechanical Switch with Low Pull-In Voltage”, *Appl. Phys. Lett.*, vol. 100, no. 11, 113102, 2012.

Conference Papers

- [1] Bo Woon Soon, **You Qian**, Eldwin J. Ng, Thomas W. Kenny and Chengkuo Lee, “Silicon-To-Silicon Microswitch With Wide Operation Temperature Range”, *The 18th Intern. Conf. on Solid-State Sensors, Actuators and Microsystems (Transducers 2015)*, Anchorage, Alaska, June 21-25, 2015.
- [2] **You Qian**, Bowoon Soon, Zhuolin Xiang and Chengkuo Lee, “Pull-In Voltage and Fabrication Yield Analysis for Fixed-Fixed Beam Nanoelectromechanical Switches”, *The 18th Intern. Conf. on Solid-State Sensors, Actuators and Microsystems (Transducers 2015)*, Anchorage, Alaska, June 21-25, 2015.
- [3] Prakash Pitchappa, Chong Pei Ho, **You Qian**, Yu-Sheng Lin, Navab Singh and Chengkuo Lee, “Enhanced controllability in MEMS metamaterial”, *The 28th IEEE Intern. Conference on Micro Electro Mechanical Systems (IEEE MEMS 2015)*, pp. 1032-1035, Estoril, Portugal, Jan. 18-22, 2015.

- [4] **You Qian**, Bowoon Soon and Chengkuo Lee, “Preliminary Study of Nanoelectromechanical Switches for Low Power Implantable Biomedical Devices,” *Intern. Conf. on BioElectronics, BioSensor, BioMedical Devices, BioMEMS/NEMS and Applications 2014 (Bio4Apps 2014)*, Shanghai, China, Nov. 17-19, 2014.
- [5] Prakash Pitchappa, Chong Pei Ho, **You Qian**, Yu Sheng Lin, Navab Singh and Chengkuo Lee, “MEMS Switchable Infrared Metamaterial Absorber”, *Intern. Conf. on Experimental Mechanics in conjunction with the 13th Asian Conf. on Experimental Mechanics 2014 (icEM2014-ACEM13)*, Singapore, Nov. 15-17, 2014.
- [6] Bo Woon Soon, **You Qian** and Chengkuo Lee, “A Vacuum Encapsulated Curved Beam Microswitch for Harsh Environment Applications”, *The 6th International Symposium on Microchemistry and Microsystems (ISMM 2014)*, pp. 178-179, Singapore, Jul. 29 – Aug. 1, 2014.
- [7] (Best paper award) **You Qian**, Bo Woon Soon and Chengkuo Lee, “All Metal Nanoelectromechanical Switches Working at 300 °C”, *The 6th International Symposium on Microchemistry and Microsystems (ISMM 2014)*, pp. 155-156, Singapore, Jul. 29 – Aug. 1, 2014.
- [8] **You Qian**, Bo Woon Soon and Chengkuo Lee, “Molybdenum Based Nanoelectromechanical Switch Fabricated by Damascene-Like Process”, *The 7th Asia-Pacific Conf. on Transducers and Micro/Nano Technologies (APCOT 2014)*, EXCO, Daegu, Republic of Korea, June 29 – July 2, 2014.
- [9] Fusheng Ma, Yu-Sheng Lin, **You Qian**, Chong Pei Ho, Prakash Pitchappa and Chengkuo Lee, “Development of Tunable 3-D Esrr For Thz Applications”, *2013 IEEE International Conf. on Optical MEMS and Nanophotonics*, pp. 141-142, Kanazawa, Japan, Aug. 18-22, 2013.
- [10] Yu-Sheng Lin, Chong Pei Ho, Prakash Pitchappa, Fusheng Ma, **You Qian**, Piotr Kropelnicki and Chengkuo Lee, “Tunable Thz Filter Using 3-D Split-Ring Resonators”, *2013 IEEE International Conf. on Optical MEMS and Nanophotonics*, pp. 167-168, Kanazawa, Japan, Aug. 18-22, 2013.
- [11] Yu-Sheng Lin, Fusheng Ma, **You Qian**, Piotr Kropelnicki, Zhen Liu, and Chengkuo Lee, “A Three-Dimensional Thz Metamaterials Using Double Split-Ring Resonators”, *The 10th Conference on Lasers and Electro-Optics Pacific Rim (CLEO-PR) & the 18th OptoElectronics and Communications Conference/Photonics in Switching (OECC/PS)*, WC4-5, Kyoto, Japan, Jun.30-Jul. 04, 2013.
- [12] Fusheng Ma, **You Qian**, Yu-Sheng Lin, Hongwei Liu, Xinhai Zhang, and Chengkuo Lee, “Development of MEMS Electric Split-Ring Resonator Arrays As Tunable Thz Filters”, *The 10th Conference*

on Lasers and Electro-Optics Pacific Rim (CLEO-PR) & the 18th OptoElectronics and Communications Conference/Photonics in Switching (OECC/PS), WC4-6, Kyoto, Japan, Jun.30-Jul. 04, 2013.

- [13] Huicong Liu, **You Qian**, Nan Wang, and Chengkuo Lee, “Study Of The Wideband Behavior of An In-Plane Electromagnetic MEMS Energy Harvester”, *The 26th IEEE International Conference on Micro Electro Mechanical Systems (IEEE MEMS 2013)*, pp. 829-832, Taipei, Taiwan, Jan. 20-24, 2013.
- [14] **You Qian**, Liang Lou, Vincent Pott, Minglin Julius Tsai and Chengkuo Lee, “A Dual-Silicon-Nanowire Based Nanoelectromechanical Switch”, *The 5th IEEE International Nanoelectronics Conference (INEC 2013)*, pp. 350-352, Singapore, Jan. 2 - 4, 2013.