

**DEVELOPMENT OF NEMS RELAYS IN LOGIC  
COMPUTATION AND RUGGED ELECTRONICS**

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# **DECLARATION**

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.



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# CONTENTS

<b>DECLARATION.....</b>	<b>I</b>
<b>ACKNOWLEDGEMENTS .....</b>	<b>II</b>
<b>CONTENTS.....</b>	<b>IV</b>
<b>SUMMARY .....</b>	<b>X</b>
<b>LIST OF TABLES .....</b>	<b>XIII</b>
<b>LIST OF FIGURES .....</b>	<b>XIV</b>
<b>LIST OF SYMBOLS AND ABBREVIATIONS .....</b>	<b>XXXI</b>
<b>CHAPTER 1: INTRODUCTION.....</b>	<b>1</b>
1.1    General introduction.....	1
1.2    Background to the research .....	5
1.2.1    Semiconductor transistor limits in harsh environment.....	7
1.2.2    Existing high temperature electronics devices .....	9
1.2.2.1    Silicon on insulator.....	10
1.2.2.2    III-V material compound transistor and SiC technology.....	10
1.3    State of the art N/MEMS switch.....	13
1.3.1    Electrostatic N/MEMS switch.....	15
1.3.2    N/MEMS switches: Memory and logic devices.....	20
1.3.3    N/MEMS switch: Material selection.....	22

1.3.3.1	Silicon Carbide .....	22
1.3.3.2	Metal and metal oxides.....	23
1.3.3.3	Other materials .....	25
1.4	Silicon as N/MEMS switch .....	27
1.4.1	Nano-size dimension of Si based N/MEMS switch .....	27
1.4.2	Si based N/MEMS non-volatile memory .....	30
1.4.3	Reliability in high temperature.....	32
1.4.4	Operation reliability in high acceleration.....	33
1.4.5	Secondary pull-in phenomenon.....	34
1.5	Motivation and objective.....	37
1.6	Organization of thesis.....	39

**CHAPTER 2: DESIGN AND FABRICATION OF A SILICON NANOFIN NON-VOLATILE MEMORY BASED ON VAN DER WAALS FORCE .....43**

2.1	Introduction .....	43
2.2	Operational NEMS switch with bi-stable states .....	44
2.3	Critical length and van der Waals force .....	46
2.3.1	Governing equations for beam's critical length .....	46
2.3.2	Finite element simulations and boundary conditions .....	52
2.3.3	Design of experiment (DOE) parameter .....	55
2.4	Design approach .....	55

2.4.1	Layout view.....	55
2.5	Fabrication process.....	57
2.5.1	Detailed fabrication and critical steps .....	58
2.5.1.1	Ultra high aspect ratio silicon nanofin definition .....	60
2.5.1.2	Gap definition.....	65
2.5.1.3	Side terminal definition .....	66
2.5.1.4	Isolation and metallization .....	68
2.5.1.5	Device release.....	69
2.6	Fabrication outcome .....	70
2.7	Conclusion.....	71

**CHAPTER 3: CHARACTERIZATION OF TWO TERMINAL SILICON NANOFIN NON-VOLATILE MEMORY.....72**

3.1	Testing setup and procedure .....	72
3.2	Electrical characterization .....	73
3.3	Result and discussion .....	74
3.3.1	I-V characteristics of a two-terminal electrostatic SiNF non-volatile memory .....	74
3.3.2	Non-volatile hysteresis operation.....	80
3.3.3	Memory and logic domain .....	87
3.3.4	Switching speed .....	90
3.3.5	Pull-in variation with respect to temperature .....	92

3.3.6	Reliability in high temperature and failure analysis.....	93
3.4	Non-volatile memory application.....	95
3.5	Conclusions .....	97
<b>CHAPTER 4: DESIGN AND FABRICATION OF A VACUUM</b>		
<b>ENCAPSULATED SILICON TO SILICON CURVED BEAM LOGIC</b>		
<b>SWITCH .....98</b>		
4.1	Introduction .....	98
4.2	Wafer level vacuum encapsulation.....	100
4.3	Robustness of a curved beam structure against secondary pull-in failure	102
4.4	Curved beam stiffness and breakdown voltage tolerance.....	103
4.4.1	Governing equations for curved beam's stiffness .....	104
4.4.2	Finite element simulations and boundary conditions .....	106
4.4.3	Stopper design.....	110
4.4.4	Design of Experiment (DOE) parameter.....	112
4.5	Design approach.....	113
4.5.1	Layout view.....	113
4.6	Fabrication Process.....	114
4.6.1	Detailed Fabrication and critical steps .....	116
4.7	Fabrication outcome .....	118
4.8	Conclusion.....	122



**CHAPTER 5: CHARACTERIZATION OF A VACUUM  
ENCAPSULATED SILICON TO SILICON CURVED BEAM LOGIC  
SWITCH IN HARSH ENVIRONMENT .....123**

5.1 Testing set-up and procedure..... 123

5.2 Electrical and mechanical characterization ..... 129

5.3 Result and discussion ..... 132

5.3.1 I-V characteristics of a three-terminal electrostatic switch ..... 132

5.3.2 Contact resistance..... 138

5.3.3 Curved beam structure robustness against secondary pull-in ..... 140

5.3.4 Switching speed ..... 143

5.3.5 Operation range from – 60 °C to 400 °C..... 145

5.3.5.1 Pull-in voltage drift..... 145

5.3.5.2 Contact resistance drift ..... 148

5.3.6 Reliability of switch versus temperature..... 151

5.3.6.1 At room temperature..... 152

5.3.6.2 At higher temperature up to 400 °C ..... 155

5.3.7 Reliability of curved beam switch under high acceleration ..... 160

5.4 Conclusion..... 167

**CHAPTER 6: FAILURE MECHANISM AND ANALYSIS.....169**

6.1 Joule heating phenomenon at contact interface..... 169

6.1.1 Failure in N/MEMS Si-to-Si switch..... 169

6.1.2	Contact temperature .....	173
6.1.3	Failure mechanism .....	178
6.2	Conclusion.....	181
<b>CHAPTER 7: CONCLUSIONS AND FUTURE WORK.....</b>		<b>183</b>
7.1	Conclusions on current work.....	183
7.2	Recommendations for future work .....	186
7.3	Refractory metal as possible higher reliable material.....	186
7.3.1	Material selection .....	186
7.3.2	A vacuum encapsulated Mo curved beam switch .....	190
7.3.3	Fabrication process flow .....	190
7.3.4	Fabrication results .....	192
7.3.5	Towards high density all mechanical logic computation .....	192
<b>BIBLIOGRAPHY .....</b>		<b>194</b>
<b>LIST OF PUBLICATIONS .....</b>		<b>212</b>
<b>APPENDICES .....</b>		<b>215</b>
A1.	ANSYS CODE – Simulation of bi-stable hysteresis curve .....	215
A2.	ANSYS CODE – Temperature simulation of contact resistor.....	221

## SUMMARY

The physical limitation in silicon bandgap hinders the development of rugged electronics. In the case of harsh environment operation such as down-hole operation where ambient temperature can rise beyond 300 °C, the electronic peripherals are disrupted due to substantial surge in the off-state current. Meanwhile, technology such as silicon-on-insulator (SOI) device, silicon carbide (SiC) and III-V semiconductors are explored by others. But these platforms are usually temperature range limited and difficult to be fabricated. Therefore an all mechanical complementary-metal-oxide-semiconductor (CMOS) compatible architecture is attractive to be implemented in high temperature logic computation and rugged electronics.

This thesis aims to explore and develop high temperature logic computation and rugged electronic leveraging on nano/microelectromechanical (N/MEMS) switches. First, a non-volatile memory (NVM) is demonstrated using an ultra-high aspect ratio two-terminal silicon nanofin (SiNF) switch. The SiNF switch is fabricated on a silicon-on-insulator (SOI) wafer with aspect ratio of 1:35 and minute size of 80 nm width ( $w$ )  $\times$  3.5  $\mu\text{m}$  height ( $h$ )  $\times$  2  $\mu\text{m}$  length ( $l$ ). This nano-scale dimension is favourable for high density application. The two-terminal switch is designed to demonstrate non-volatile memory's hysteresis behaviour based on the novel idea of van der Waals

(VDW) force latching mechanism. This bi-stable mechanism leveraging on surface adhesion demonstrated is the first of its kind in nano-scale switches. Set and reset operation can be configured by electrostatically actuating the SiNF between one of two terminals, with pull-in voltage ranging from 10 to 20 V. The off-state leakage current in hundreds of pA range while the on/off is in the order of  $10^2$ . Low voltage drift of -24mV/K is demonstrated from 50 °C to 150 °C with switching speed of approximately ~70ns.

Next, a logic switch that demonstrates logic computation function is designed and encapsulated in vacuum to enhance the lifetime in high temperature. This three-terminal micro switch relies on a curved beam (source) that actuates toward the contact terminal (drain) by charging the control terminal (gate). The curved beam design also increases the spring stiffness thus providing better reliability. Meanwhile, three independent terminals are designed to provide uninterrupted gate control and drain-source signals. The micro switch demonstrated high sub-threshold slope of 120  $\mu$ V/decade and pull-in voltage ranges from 15 to 25 V. In extreme temperature environment, operation range of the micro switch from -60 °C to 400 °C is verified and demonstrated, which yields a resistance drift of approximately -200  $\Omega$ /K. Meanwhile, lifetime of more than  $10^7$  cycles at room temperature and  $10^6$  cycles in high temperature of 400 °C are successfully verified. Subsequently, investigation using a shaker

test from 1 g to 10 g is performed to show that the switch's operation is unaffected by high acceleration. Such study is important for application in high acceleration environment such as satellite deployment or rocket launch. Failure analysis of both devices are performed and further studied. The study of such Si-to-Si contact-based micro switches provides a crucial guideline and paves the path to the future of mechanical computing and failure mechanisms in harsh environment applications.

## LIST OF TABLES

Table 1.1 Technologies available for HTE market [6, 79] .....	7
Table 1.2 Summary of technology in high temperature electronics [27, 92, 134].....	15
Table 1.3 Comparison of N/MEMS actuation mechanisms [135-153], [154-157].....	17
Table 1.4 Comparison of lifetime and temperature study of different N/MEMS switches.....	26
Table 2.1 SiNF parameters in design of experiment (DOE).....	55
Table 3.1 Comparison of Switching speed between different NEMS switch.....	92
Table 4.1 Curve beam parameters in design of experiment (DOE).....	112
Table 5.1 Parameter Settings for On-Off Cycle.....	151
Table 6.1 Comparison of specification of different N/MEMS switches for high temperature environment .....	182
Table 7.1 Material Property of different candidate for switch [210] .....	187

## LIST OF FIGURES

Figure 1.1: Example of rugged electronics application: Tunnel boring machine's (TBM) sensor network showing the position of different electrical modules [1, 2]. ....	2
Figure 1.2: High temperature electronics requirement in different industry sector [6]. .....	6
Figure 1.3: Semiconductor carrier's density change with respect to temperature. At high temperature, intrinsic carriers dominate and device's behaviour becomes unstable [79-81]. .....	8
Figure 1.4: Comparison of silicon, 6H-SiC, and 2H-GaN intrinsic carrier concentration ( $n_i$ ) versus temperature [79]. .....	11
Figure 1.5: (a) Switching characteristics of a NMOS with sub-threshold swing. (b) Steep sub-threshold rise and fall of a micro switch .....	13
Figure 1.6: Operation of electrostatic switches. (a) Operation of electrostatic switches in OFF and ON states. (b) Typical voltage sweeping curve of electrostatic switches. ....	18
Figure 1.7: Dimension parameter of a typical cantilever beam. ....	19
Figure 1.8: (a) Die photo of the hybrid N/MEMS-CMOS chip. (b) layout and cross-section of the N/MEMS switch. (c) Voltage transfer characteristic showing hyper abrupt transitions between logic states. (d) Timing diagrams for 2-V, 50-Hz operation [41, 160]. .....	20

Figure 1.9: (a) Schematic diagram of the MEMS-based non-volatile memory device. The CNT is used for the source/drain channel and a MEM cantilever is added to transfer charges to the floating gate. (b) Diagrams demonstrating the programming (upper three panels)/erasing (lower three panels) processes. Blue/red colours indicate the polarities  $\pm$  of the applied voltages. (c) Memory endurance operation under repeated programming/erasing cycles for the side-floating gate device. The test was performed over 500 cycles for 600 s with  $V_{ds} = 100$  mV. (d) Expanded section of (c) also showing the voltages applied to the cantilever (purple line) and activating electrode (green line) [41, 160].

Figure 1.10: (a) SEM of an inverter device. (b) zoom-in of the highlighted contact [39].

Figure 1.11: Localized Joule heating resulting in melting of SiC [39].

Figure 1.12: (a) SEM images showing actuation of a five terminal polysilicon switch coated with platinum on the sidewalls and selected top surfaces. (b) SEM cross section of unreleased platinum-coated beams [171].

Figure 1.13: (a) Optical micrograph showing the switch design. Four folded springs are attached to an anchor point on the wafer, and the opposite sides are connected to the edges of a rectangular plate. Four dimples connect to two signal lines on opposite sides of the switch. (b) SEM of the device with moving plate broken and shift aside to reveal gate and bottom contact area [28].

Figure 1.14: (a) A schematic illustration of the U-shape NEMS switch. (b) SEM



photo of a U-shape NEMS switch after HF vapor releasing, Inset: TEM image of a SiNW cross-section [133].	28
Figure 1.15: I-V characteristic of the device. For the first five switching cycles, the current ratio indicates the change in current that occurs within 10 mV of the pull-in voltage.	29
Figure 1.16: (a) SEM image of two 3T switch; (b) The typical switching current–voltage characteristics of the 3T switch. The inset shows the switch on/off diagram and the hysteresis of $I_{DS}$ – $V_{GS}$ as the gate voltage is swept from $V_{GS} = 0$ to 9.0 V and then back to 0 V at $V_{DS} = 2.0$ V [81].	30
Figure 1.17: A schematic illustration of the NEMS torsion switch device. (b) SEM photo of a NEMS torsion switch after HF vapour releasing. The dimension: CL, CW, TL, and TW of device are 9 $\mu\text{m}$ , 1.5 $\mu\text{m}$ , 2.4 $\mu\text{m}$ , and 530 nm respectively [18].	31
Figure 1.18: I-V characteristic of the device for multiple operations [18].	32
Figure 1.19: (a) SEM image of a five-terminal switch after electrostatic actuation. High current flow between the beam and the gate after shorting causes irreversible damage. (b) Plot of the displacement of the source at the gate and the maximum displacement of the source as a function of gate voltage for a N/MEMS switch. The source pulls in to the drain at approximately 7 V. As the voltage is increased, the source Shorts to the gate at approximately 11 V. The difference between these two voltages is the operating voltage [189].	35

Figure 1.20: Illustration of secondary pull-in for free-end cantilever beam, double-clamped beam. ....	36
Figure 1.21: SEM image of the curved beam switch showing three terminals: drain, gate and source. The contact area is depicted by dashed line [194]. ....	37
Figure 2.1: (a) Top view schematic of the NEMS memory with SiNF as the actuator that can switch between two terminals (b) Structure and operation of a bi-stable NEMS switch. (1) SiNF is pulled-in to the right terminal by $V_{SI}$ . (2) VDW force holds the SiNF in contact position even after the electrostatic force is removed (3) As bias is applied opposite, SiNF flips towards the other terminal. (4) VDW force holds the switch in left terminal. (5) The switch cycles between two terminals, resulting in bi-stable state device. ....	45
Figure 2.2: Side view of cantilever structure stick to bottom substrate with dimensional parameters. ....	47
Figure 2.3: (a) FEM simulation model of a SiNF in ANSYS with displacement (in $\mu\text{MKS}$ ) denoted. (b) The result of simulation for a successful non-volatile hysteresis curve due to van der Waals force. As the voltage sweep from starting from 0 V, tip displacement of the SiNF is simulated. Pull-in is detected after that and the stiction due to van der Waals force is consider as a load that holds the SiNF tip in closed contact position. The contact remains closed as voltage sweep return to zero. The same phenomenon repeats on the other side of the switch terminal, forming a non-volatile hysteresis curve. ....	54

Figure 2.4: (a) Reticle (25 × 35 mm) top layout. (b) Single device cell layout with top metallization pads. ....56

Figure 2.5: Zoom-in view of the SiNF with specific dimensions. ....57

Figure 2.6: A 3D schematic of the NEMS memory with SiNF as the actuator that switches between the terminals. The entire structure is made from Si except the metallization using Al. ....57

Figure 2.7: CMOS front end of the line (FEOL) process flow for SiNF switch. . a.) SOI wafer – 3.5 μm device layer, 1μm BOX. b.) 3.5 μm Si DRIE. c.) Dry oxidation. d.) 5 μm poly-Si deposition and planarization till flat. e.) Al metallization. f.) Device release in VHF. .... 60

Figure 2.8: (a) Wafer exposure map and measurement location of the available die area. (b) FEM result of SiNF exposure optimization. Bossung’s plot shows optimized window of target SiNF’s CD. .... 62

Figure 2.9: (a) Overall SiNF definition with DRIE. (b) Zoom-in of one SiNF with open end with very straight sidewall. (c) Sideview of SiNF shows etched surface profile. .... 63

Figure 2.10: (a) Local oxidation (wet) of SiNF to reduce surface roughness and overall SiNF width. (b) SiNF width of 80 nm after removing surface oxide. (c) Side view of SiNF shows extremely smooth sidewall. .... 64

Figure 2.11: AFM result of sidewall of SiNF ..... 65

Figure 2.12: (a) Photoresist opening of the SiNF area for gap definition. (b) SiO<sub>2</sub>

sacrificial reduction etches using HF acids around the SiNF actuation area to create 80nm gap.....	66
Figure 2.13: (a) Thick poly silicon deposition overfilling all trenches and forming side terminal of the SiNF. (b) After CMP, SiNF is exposed and the terminals are self-aligned to side. (c) Zoom-in of the SiNF. ....	67
Figure 2.14: (a) Isolation trench stop on buried oxide layer (BOX) to isolate the SiNF and the gate-electrodes. (b) SiNF is etched to become a cantilever, SiO <sub>2</sub> sidewall remains due to higher selectivity. ....	69
Figure 2.15 (a) Top view of the released SiNF. (b) Tilted view of the SiNF with 80 nm width. ....	69
Figure 2.16: SEM of a switch device of 8 μm length × 90nm thick SiNF. (Inset) Zoom in view of the SiNF in the centre of the device. ....	70
Figure 3.1: Testing set-up of the SiNF electrical characterization. Probe station with microchamber (Cascade RBL-6100) equipped with semiconductor analyser (Agilent B1500) and function generator (Tektronix AFG 3102).....	72
Figure 3.2: Measured hysteresis curve of a 2 μm long fin showing two pull-in voltage (-10 V and 12 V) of a SiNF device. (Inset) log scale curve. 0V point omitted for illustration purpose. The on/off ratio of the SiNF is approximately 2~3 orders of magnitude.....	75
Figure 3.3: Pull-in voltage, $V_{PI}$ versus different thickness of switch of 80 – 120 nm (measured). Constant error bar for twenty switching devices and median of each	

thickness are measured. Pull-in voltage,  $V_{PI}$  increases with the thickness of SiNF. ... 76

Figure 3.4: Pull-in voltage,  $V_{PI}$  versus different switching length of 2 $\mu\text{m}$ , 8 $\mu\text{m}$  and 12 $\mu\text{m}$ . Constant error bar for twenty switching devices and median of each length are measured. Pull-in voltage,  $V_{PI}$  reduces with the length of SiNF. .... 76

Figure 3.5: (a) Pull-in voltage line fitting with respect to SiNF length on a log-log scale. (b) ) Pull-in voltage line fitting with respect to SiNF width on a log-log scale. 77

Figure 3.6: Comparison of pull-in voltage for analytical model and experimental value. Mean value is taken from experimental value. Overall the experimental value is higher than then analytical value, where the analytical model is a standard parallel capacitor model. .... 79

Figure 3.7: Measured  $I_S - V_S$  curve of an 8  $\mu\text{m}$  length SiNF device. The current compliance of the measurement is limited up to 100  $\mu\text{A}$ . From 0V to 10V, measured  $V_{PI}$  is 5.95 V at 25m V/decade. The measured  $I_{ON}/I_{OFF}$  is  $10^5$ . From 10 V to 0 V, the pull out is not abrupt but shows charging relation. .... 80

Figure 3.8: SEM diagram showing a 2  $\mu\text{m}$  length  $\times$  80 nm width SiNF in operation. (a) SiNF remains at neutral position. (b) SiNF contact remains on hold to the left terminal, depicting state “0”. (c) SiNF flips to the right terminal and on hold to the right terminal, depicting state “1”. .... 80

Figure 3.9: Live video of the SiNF switching in real time, captured under SEM. The SiNF switch is activated and makes contact with the right terminal during operation. 83

Figure 3.10: Measured bi-stable I-V Characteristic of the NEMS memory. (a) 2  $\mu\text{m}$

SiNF device (b) 8  $\mu\text{m}$  SiNF device. The bi-stable operation is shown in a following sequence. (1) First the SiNF is pulled in to the left terminal. (2) Left terminal contact holding by the VDW. (3) SiNF flips to the right terminal. (4) Right terminal contact holding by the VDW. Note that the current is continuous when voltage sweep returns to 0V. .... 85

Figure 3.11: Constant error bar of  $V_{PI}$  and  $V_{RESET}$  versus 2, 8, and 12  $\mu\text{m}$  long SiNF of twenty devices.  $V_{PI}$  reduced while  $V_{RESET}$  increases sharply, while device with fin length of 12  $\mu\text{m}$  cannot be reset due to permanent adhesion. .... 86

Figure 3.12: SEM images of SiNF. (a) 2  $\mu\text{m}$  SiNF. Inset: Zoom-in of contact between SiNF and terminal. (b,c) 8,12  $\mu\text{m}$  SiNF device. Insets: Zoom in view of SiNF bending and in contact with either terminal. .... 88

Figure 3.13: Force of spring and van der Waals of silicon beam and contact surfaces of Si and  $\text{SiO}_2$  versus measured contact area of SiNF. Non-volatile memory region is defined as the van der Waals force is larger than the spring restoration force of the SiNF. The logic region is vice versa. .... 90

Figure 3.14: Switching speed of an 80 nm  $\times$  2  $\mu\text{m}$  SiNF. The time difference,  $\Delta t$  given by the delay is measured to be 26.3 ns. .... 91

Figure 3.15:  $V_{PI}$  at temperature of 50  $^\circ\text{C}$ , 100  $^\circ\text{C}$  and 150  $^\circ\text{C}$  of 2  $\mu\text{m}$  long switch of thickness 90 nm. Low voltage drift of 24mV/K is measured. .... 93

Figure 3.16: SEM diagram of an 8  $\mu\text{m}$  SiNF after failure. SiNF is melted and fused to the actuating terminal. .... 94

Figure: 3.17 Vacuum encapsulation of the SiNF switch can prevent oxidation of the contact interface. Meanwhile, Joule heating needs to be reduced to enhance the lifetime of the device. ....95

Figure 3.18: Proposed  $2^3$  bit memory array implemented by two-terminal SiNF switch. Each device consists of two states, namely Reset State ‘0’ and Programmed State ‘1’. Write and reset operation can be executed by turning on both read and write line. Meanwhile, read operation is performed by low current measurement where device are subjected to a read potential ( $V_{read} < V_{PI}$ ) .....96

Figure 4.1: Illustration of radial electrostatic force exerted on the curved beam when gate potential is changed from high to low. (Condition for pull-in:  $V_{GATE} \geq V_{PI}$ ).....99

Figure 4.2: Epi-seal process flow. Starting from the left: Device definition, sacrificial and spacer deposition, cap and release hole patterning, poly-silicon sealing and interconnect redistribution [184]..... 101

Figure 4.3: Illustration of secondary pull-in comparison between electrostatic switch for curve beam, free-end cantilever beam, double-clamped beam. The curved beam structure offers robust gate voltage overdrive and prevention from secondary pull-in due to the enhanced mechanical strength after pull-in happens..... 103

Figure 4.4: Cross-section layout of the semi-circular curved beam electrostatic switch design..... 107

Figure 4.5: Simulation result of pull-in voltage versus radius of curvature for curved beam with varying widths. Inset: 3D model of curved switch (Displacement: 0 -

0.86 $\mu\text{m}$ ).....	109
Figure 4.6: Simulated high breakdown voltage of 174 V with initial pull-in and contacted drain at approximately 11 V. Inset: Pull-in of drain to gate during breakdown. (Displacement: $0 - 3.1 \times 10^{-3} \mu\text{m}$ ) .....	110
Figure 4.7: Contact dimple stopper and contact distance requirement for curved beam switch. ....	112
Figure 4.8: Layout view of one $3 \times 3 \text{ mm}^2$ die. A single device cell is shown at the bottom. One device comprised of a curved beam, gate and drain. ....	113
Figure 4.9: Exploded view of the Si-to-Si MEMS switch with encapsulation layers consist of device layer, capping layer, sealing layer and metallization layer with different function. ....	115
Figure 4.10: Fabrication process flow of encapsulated curve switch. (a) Si deep trench etching. (b) $\text{SiO}_2$ overfills to seal trench. (c) Via definition with device release. (d) Si epitaxy sealing and electrode isolation. (e) Passivation opening. (f) Al metallization.....	117
Figure 4.11: (a) Top view of the finished chip with metalized aluminium pad. (b.) X-Ray image showing the encapsulated three-terminal switch comprised of a movable curve beam (Source), control terminal (Gate) and contact terminal (Drain).	119
Figure 4.12: SEM image of a $3 \mu\text{m} \times 85 \mu\text{m}$ radius curved switch before encapsulation is performed. The image is captured after the DRIE process. (Inset) Zoom-in of the contact region.....	120



Figure 4.13: SEM cross-section of a curved switch device showing the released curved beam with a poly-silicon encapsulation seal. (a.) Encapsulated curved beam.

(b.) Epi-Seal process with encapsulated beam..... 121

Figure 5.1: Testing set up of the vacuum encapsulated curved beam switch. The set up includes a probe station (Cascade RBL-6100) equipped with CCTV, a semiconductor analyser (Agilent B1500), the probe station stage modified with a hot plate (Thermo Scientific HP131225Q Cimarec). The Zoom-in image shows the DUT placed under hot plate with temperature setting 500 °C..... 125

Figure 5.2: Calibration of surface temperature of the curved beam switch. The measured temperature is regulated to its setting temperature for more accurate temperature setting purpose. .... 126

Figure 5.3: Vacuum probe station (Cascade Microtech vacuum probe station, PMV200) equipped with an 8” wafer vacuum test chamber, turbo pump and a compressor tower for cooling. Bottom image shows the detail of the temperature controller that can be set from -60 °C to 300 °C..... 127

Figure 5.4: Testing set up of operation high acceleration. The set up comprised of a shaker (Brüel & Kjær LDS V406) together with power amplifier and a semiconductor analyser (Agilent B1500). The same set up is illustrated by the schematics diagram with defined axis of acceleration..... 128

Figure 5.5: Scanning electron micrograph (SEM) of a curved beam Si-to-Si MEMS switch. The operation of the switch is shown where  $V_G$  is used to control the

actuation with gate terminal and  $V_S$  is used to detect signal from source to drain.

Parameter radius,  $r$  and width,  $w$  of beam is shown. .... 129

Figure 5.6: Three terminal testing of  $I_D$ ,  $I_S$ ,  $I_G - V_G$ . Pull-in and pull-out of the curved beam is shown by the near ideal abrupt on-off characteristics at 20 V and 3.8 V respectively. Low noise and power is demonstrate by the low gate current ( $I_G$ ) at pA range at all time during entire sweep. .... 130

Figure 5.7: Cycling test set-up for Si-to-Si reliability test. Test A based on voltage source ( $V_S$ ) and current measurement ( $I_S$ ) while Test B based on current source ( $I_S$ ) and voltage measurement ( $V_S$ ). .... 132

Figure 5.8: Three-terminal testing of  $I_D$ ,  $I_S$ ,  $I_G - V_G$ . (a) Switch turns on during forward  $V_G$  sweep and turns off during return  $V_G$  sweep. (b)  $I_G$  remains low with measured noise floor of the semiconductor analyzer. .... 134

Figure 5.9:  $I_D$ ,  $I_G - V_G$  of 5  $\mu\text{m}$  wide  $\times$  165  $\mu\text{m}$  radius curved beam. Permanent non-resettable contact is obtained as  $V_G$  sweeps returns to zero, indicating switch remains in contact. .... 136

Figure 5.10: Measurement of ten sweeping cycles.  $I_{DS} - V_G$  sweeping cycles within same device. Pull-out variation is highlighted. .... 137

Figure 5.11: Comparison between measured pull-in voltages ( $V_{PI}$ ) of 3, 5  $\mu\text{m}$  (width) curved beam with various radius versus analytical model. Absolute error 1 – 3 V measured from 15 devices of the same dimension. .... 138

Figure 5.12: Pull-in and pull-out characteristics of a 5  $\mu\text{m}$   $\times$  95  $\mu\text{m}$  curved beam

switch showing a contact resistance measurement without current compliance. ....	140
Figure 5.13: Pull-in and pull-out characteristics of a $5\ \mu\text{m} \times 95\ \mu\text{m}$ device with voltage over drive from 0 to 100V. Gate current ( $I_G$ ) remain low at pA level during the sweep.....	141
Figure 5.14: High voltage breakdown endurance. (a) $V_{PI}$ at 24.5 V of $5\ \mu\text{m} \times 95\ \mu\text{m}$ radius beam, $V_G$ until 50 V (b) $V_{PI}$ at 15.5 V of $5\ \mu\text{m} \times 115\ \mu\text{m}$ radius beam, $V_G$ until 100 V.....	142
Figure 5.15: Ultra high speed pulse I-V measurement for switching delay. (a) $5\ \mu\text{m} \times 75\ \mu\text{m}$ radius switch (b) $5\ \mu\text{m} \times 95\ \mu\text{m}$ radius switch.....	144
Figure 5.16: I-V measurement of a $5\ \mu\text{m} \times 150\ \mu\text{m}$ radius curved beam switch. (a) Pull-in and pull-out characteristics from room temperature to 400 °C. (b) Linear fit of the extracted pull-in voltage yields a $V_{PI}$ drift of 1.04mV/K. ....	147
Figure 5.17: I-V measurement of a $5\ \mu\text{m} \times 95\ \mu\text{m}$ radius curved beam switch. (a) Pull-in and pull-out characteristics from room temperature to 400 °C. (b) Linear fit of the extracted pull-in voltage yields a $V_{PI}$ drift of 1.36mV/K. ....	148
Figure 5.18: Contact resistance of a $5 \times 127\ \mu\text{m}$ curved beam from -60 °C to 300 °C. (a.) Multiple pull-in $I_{DS} - V_G$ at different temperatures. (b.) Extracted contact resistance drift (35 measurements) of -196Ω/K.....	150
Figure 5.19: Real time measurement set-up for on-off cycling test up to $10^5$ cycles under ambient condition of $5\ \mu\text{m} \times 95\ \mu\text{m}$ radius beam. (a) Real time measurement of multiple cycles. (b) zoom-in of one cycle. ....	153

Figure 5.20: I-V characteristics for  $10^6$  cycles under ambient condition. (a) On-off drain source current ( $I_{DS}$ ) with respect to every cycle. (b) On-off gate current ( $I_G$ ) with respect to every cycle..... 154

Figure 5.21: Contact resistance versus no. of cycles under 300 °C elevated temperature. (Inset) Zoom in on the contact resistance during on cycle..... 156

Figure 5.22: (a) One million cycles at 400 °C verified with  $I_{DS}$  current limited to 0.5  $\mu$ A in log scale. (b) Zoomed-in of device showing seven repeated on-off cycle with respect to gate voltage..... 157

Figure 5.23: Reliability statistics of twenty-five devices with maximum current flow (1A). By limiting the current to 0.5  $\mu$ A (highlighted), the reliability is enhanced – a lifetime of one million cycles is achieved at 300 °C and 400 °C..... 158

Figure 5.24: Operation under acceleration shock test with device placed flat on the shaker. The direction of acceleration is along the z-axis, as represented by the red dash arrow. The electrical connection for gate, drain and source is connected to the semiconductor analyser..... 161

Figure 5.25: I-V characteristics of a  $3 \mu\text{m} \times 80 \mu\text{m}$  radius curved beam device under z-axis acceleration. (a) Consistent pull-in voltage of approximately 22 V at incremental acceleration from 1 g to 10 g @ 2kHz. (b) Zoom-in of the pull-in voltage..... 162

Figure 5.26: Operation under acceleration shock test with device placed in upright position on the shaker. The direction of acceleration is along the y-axis, as

represented by the red dash arrow. The electrical connection for gate, drain and source is connected to the semiconductor analyzer. .... 163

Figure 5.27: I-V characteristics of a  $3\ \mu\text{m} \times 80\ \mu\text{m}$  radius curved beam device under  $y$ -axis acceleration (a) Pull-in voltage decreases with increases of acceleration from 1 g to 10 g @ 2 kHz. (b) Zoom-in of the pull-in voltage. .... 164

Figure 5.28: Operation under acceleration shock test with device placed in upright position on the shaker. The direction of acceleration is along the  $x$ -axis, as represented by the red dash arrow. The electrical connection for gate, drain and source is connected to the semiconductor analyzer. .... 165

Figure 5.29: I-V characteristics of a  $3\ \mu\text{m} \times 80\ \mu\text{m}$  radius curved beam device under  $x$ -axis acceleration (a) Pull-in voltage decreases with increases of acceleration from 1 g to 10 g. (b) Zoom-in of the pull-in voltage. .... 166

Figure 5.30: Pull-in voltage ( $V_{PI}$ ) stability with respect to acceleration at  $z$ -axis and  $y$ -axis.  $V_{PI}$  drift in  $y$ -axis acceleration of -40 mV/g is extracted from curve fitting using measurement result while no drift is observed in  $z$ -axis acceleration. .... 167

Figure 6.1: Contact resistance versus number of cycles at 300 °C with maximum current compliance (1 A) (a) Approximately 47 thousand cycles achieved for Si-to-Si switch encapsulated in vacuum. (b) Zoom-in to the last few cycles showing that device fail..... 170

Figure 6.2: Contact resistance versus number of cycles at 400 °C with maximum current compliance (1 A) (a) Merely 923 cycles achieved for Si-to-Si switch

encapsulated in vacuum. (b) Zoomed-in view of device that failed abruptly at 923 cycles. ....	171
Figure 6.3: Focus ion beam milling reveals cross-sectional view of a failed device after sudden failure at high temperature cycling.....	172
Figure 6.4: Dependency of the contact resistance on $V_{DS}$ bias from 0.5 V to 4.5 V (a) $I_{DS}$ - $V_G$ at different $V_{DS}$ where device failed at $V_{DS} = 4.5V$ . (b) Contact resistance (45 measurements) and calculated contact temperature versus drain source voltage, $R_C$ - $V_{DS}$ . ....	175
Figure 6.5: (a.) $I_{DS}$ - $V_G$ at different $V_{DS}$ with $I_{DS}$ limited to 0.5 $\mu A$ . The device fails to pull out at $V_{DS} = 8$ V. (b.) The hysteresis gap increases as drain-source voltage increases.....	177
Figure 6.6: Failure mechanisms of contact switches. Repeated push and pull by turning on and off electrostatic force can results in four major mechanics of contact degradation.....	179
Figure 6.7: Focus ion beam milling reveals cross-sectional view of a failed device after ~5 million cycling test. ....	180
Figure 7.1: Modeling of joule heating of contact resistor using ANSYS .....	188
Figure 7.2: Max temperature of contact tips versus sweeping voltage of Si based contact.....	189
Figure 7.3: Max temperature of contact tips versus sweeping voltage of Mo based contact.....	189

Figure 7.4: Process flow of a vacuum encapsulated Mo based switch. (a) Define SiO<sub>2</sub> molding. (b) Mo deposition. (c) Define SiO<sub>2</sub> masking. (d) CMP isolation. (e) Deposit sacrificial SiO<sub>2</sub> (f) AlN capping layer with release vent. (g) Deposit SiO<sub>2</sub> sealing after release. (h) Pad metallization. .... 190

Figure 7.5: Preliminary fabrication outcome of the proposed process flow. (a) Vacuum encapsulation performed on Mo switch. (b) Structure before encapsulation showing terminals and curved beam. .... 192

Figure 7.6: (a) Array of four Mo switches with encapsulation. (b) FIB cross-section of encapsulation showing four nano-size Mo beams. (c) Zoom in detail of one switch. .... 193

## LIST OF SYMBOLS AND ABBREVIATIONS

$E$	Young's modulus
$n_i$	Intrinsic carrier's density
$N_C$	Electron density of states
$N_V$	Holes density of states
$T$	Temperature
$k$	Boltzmann constant
$E_G$	Energy bandgap of semiconductor
$I_{DS}$	Drain-source current
$V_G$	Gate voltage
$I_{CL}$	Channel leakage current
$I_{SL}$	Drain-to-substrate leakage current
$I_{OFF}$	Off current
$g_d$	Drain to source gap
$g$	Gate to source gap
$t_f$	Thickness
$k_{eff}$	Effective spring constant
$K_C$	Spring constant of curved beam
$A$	Effective capacitive area
$A_C$	Area of cross-section
$\epsilon_0$	Permittivity of free space
$h$	Height
$w$	Width



$l$	Length
$d$	Height
$L_c$	Critical length
$t$	Thickness
$r$	Radius
$I$	Area moment of inertia
$G$	Shear modulus
$\nu$	Poisson's ratio
$\alpha'$	Thermal coefficient expansion
$\beta'$	Young's modulus temperature coefficient
$g_g$	Gate gap
$H_{Si}$	Hamaker's constant of Si
$R$	Radius of curvature
$H$	Hamaker's constant
$V_{th}$	Threshold voltage
$V_{dd}$	Drain voltage
$V_{GS}$	Gate voltage sweep
$V_{PI}$	Pull-in voltage
$V_{PO}$	Pull-out voltage
$V_{on}$	Turn on voltage
$V_{G1}$	Gate voltage 1
$V_{G2}$	Gate voltage 2
$V_{Sweep}$	Sweeping voltage

$V_{S1}$	First sweeping voltage
$V_{S2}$	Second sweeping voltage
$V_D$	Drain voltage
$V_S$	Source voltage
$V_{ds}$	Drain-source voltage
$V_G$	Gate voltage
$I_S$	Source current
$I_D$	Drain current
$I_{DS}$	Drain-source current
$I_G$	Gate current
$R_C$	Contact resistance
$F_{elec}$	Electrostatic force
$F_{VDW}$	Van der Waals force
$F_{spring}$	Spring restoration force
2T	Two-terminal
3T	Three-terminal
NEMS	Nanoelectromechanical system
HTE	High temperature electronics
CMOS	Complementary-metal-oxide-semiconductor
MPW	Multi project wafer
TBM	Tunnel Boring Machine
UTBSOI	Ultra-thin body silicon on insulator
MOSFET	Metal-oxide-field-effect-transistor
IC	Integrated circuit

SOI	Silicon-on-Insulator
CAD	Computer aided design
HEMT	High electron mobility transistor
N/MEMS	Nano/microelectromechanical systems
RF	Radio frequency
DOE	Design of experiment
NVM	Non-volatile memory
SiNF	Silicon nanofin
MPW	Multi project wafer
FEM	Finite element method
FEA	Finite element analysis
BOX	Buried oxide
VDW	Van der Waals
EPI-SEAL	Epitaxy silicon sealing
SiNF	Silicon nanofin
NVM	Non-volatile memory
Si	Silicon
SiC	Silicon carbide
GaN	Gallium nitride
Au	Gold
RuO <sub>2</sub>	Ruthenium Oxide
Poly Si Ge	Poly Silicon Germanium
W	Tungsten
TiN	Titanium Nitride

Pt	Platinum
Ru	Ruthenium
A-C	Amorphous Silicon
Al <sub>2</sub> O <sub>3</sub>	Aluminium oxide
SiO <sub>2</sub>	Silicon dioxide
Al	Aluminium
Mo	Molybdenum
C <sub>4</sub> F <sub>8</sub>	Octafluorocyclobutane
SF <sub>6</sub>	Sulfur Hexafluoride
MOCVD	Metal organic chemical vapour deposition
VPE	Vapour phase epitaxy
MBE	Molecular beam epitaxy
LPCVD	Low pressure chemical vapour deposition
DRIE	Deep reactive ion etching
PECVD	Plasma enhanced chemical vapour deposition
PVD	Physical vapour deposition
CMP	Chemical-mechanical polishing
SEM	Scanning electron micrograph
BARC	Bottom anti-reflective coating
FEM	Focus exposure matrix
CD	Critical dimension
LOCOS	Local oxidation
HF	Hydrofluoric acids
VHF	Hydrofluoric acid vapour

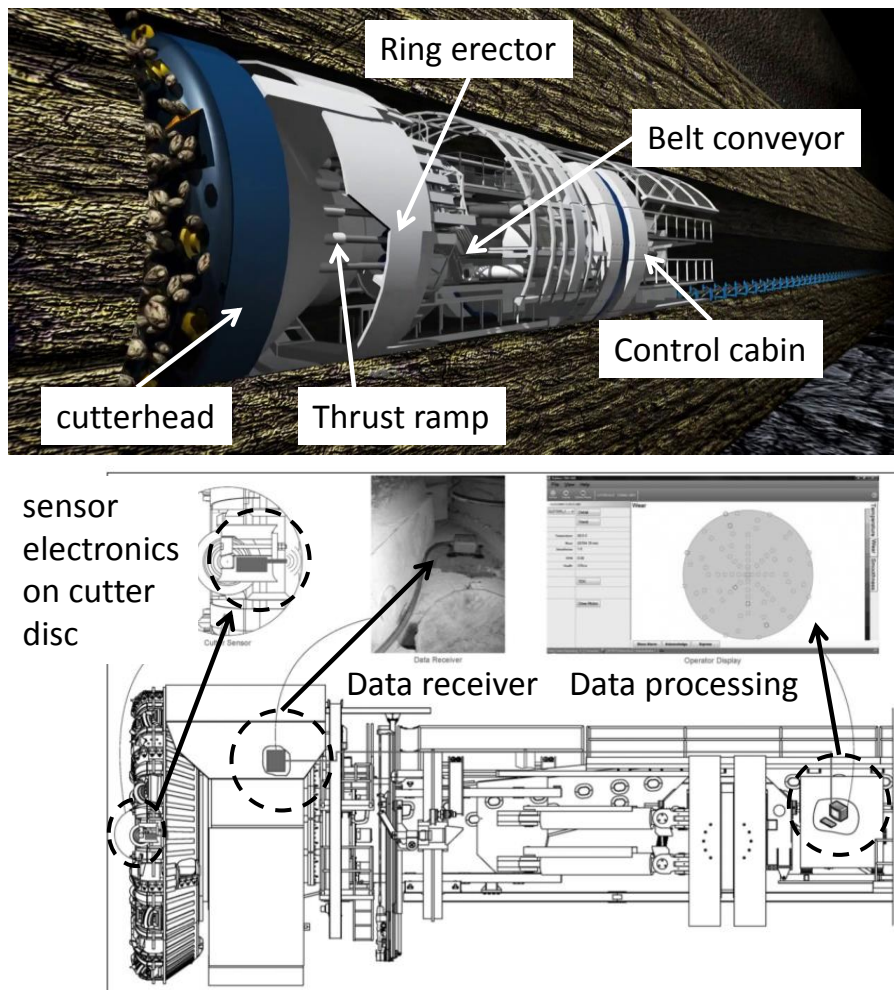
BARC	Bottom anti-reflective coating
SMU	Source monitoring unit
HRSMU	High resolution source monitoring unit
FIB	Focused ion beam

# CHAPTER 1: INTRODUCTION

## 1.1 General introduction

The mentioning of harsh environment is particularly associated with high temperature and acceleration. For example, the call for capability to withstand temperature  $> 300\text{ }^{\circ}\text{C}$  is normal for operation such as down-hole exploration in oil & gas industry, automotive and aerospace application. Acceleration is likely to have an impact on the packaging of the electronics placed near to the harsh environment. Despite low consumer demands, the drive to develop rugged electronics or high temperature electronics (HTE) is real. In a harsh environment sensor system, the embodiment of each component depends of the overall infrastructure. A typical control instrument and sensory network comprised of the sensors (input), microcontroller (process), and interfacing electronics (output). For example, in construction's tunnel boring shown in Figure 1.1, the pressure sensors and temperature sensors together with the read-out electronics are often integrated on the cutterhead of the tunnel-boring machine [1, 2]. The read-out electronics are critical in feeding back the power, speed and safety manoeuvres to the control cabin during the underground tunnel construction. Meanwhile, during a rocket launch or a satellite deployment, the acceleration experienced by the electronics could go up to 5 g [3-5]. To safeguard the electronics under high

acceleration, special packaging or mechanical fixture is designed to protect the electrical circuitry and sensors. Similarly, it is also important to study the acceleration impact in N/MEMs devices.



**Figure 1.1: Example of rugged electronics application: Tunnel boring machine's (TBM) sensor network showing the position of different electrical modules [1, 2].**

This leads to the demand of an electronics system that is reliable and able to withstand high temperature and resistant to acceleration. Since the market is largely dominated by silicon electronics, it is natural to study and explore the

possibility for a convenient implementation using existing complementary-oxide-semiconductor (CMOS) platform technology. In fact, Si bandgap devices in harsh environment had been extensively researched and reported [6, 7]. Nevertheless, bandgap devices exhibit intrinsic physical limitation. As the temperature elevated beyond 300°C, intrinsic carrier density surpasses the dopants, resulting in higher sub-threshold leakage, causing off-state current to increase [6, 8, 9]. Altogether, these circuit's technologies are not effectively reducing the leakage power in high temperature, making these devices not suitable for harsh electronics application beyond 300 °C. There have been research such as using thin film diamond or diamond based transistor [10-12], III-V GaN based transistor [13-15] and SiC based power transistor [12, 16, 17] to produce more reliable high temperature electronics. Although some commercialized products are qualified to operate up to 250 °C, operation beyond this temperature is still questionable, as the material deteriorates in high temperature environment. Meanwhile, some of the devices are not fabricated by standard CMOS foundry, which is why it is less lucrative to design a processing unit using the technology.







On the other hand, N/MEMS electrostatic switches have been demonstrated and have potential to offer several unique features, such as near-infinite sub-threshold slope, near zero leakage and the potential for operation in harsh environment [18-34]. These features are due to the nature of micromechanical switching, where the static power dissipation is ideally zero. The capacitive switches' characteristic is exceptionally power efficient in power gating or ruggedized electronics applications [26, 35-48]. The most important of all, N/MEMS switches have been either hypothesized or reported of being able to withstand harsh environments [27, 28, 31, 32, 34, 35, 39, 40, 49-59], and such properties may prove invaluable for logic computing or memory in the area of rugged electronics, where machines and devices operate in harsh environments. On the application side, MEMS switches have demonstrated the capability of CMOS logic operation and non-volatile memory. It is also proposed by many as a possible alternative to the limitations of scaling CMOS transistors, as it shows much lower power consumption [60-69]. To date, N/MEMS switches have shown promising capability in CMOS-MEMS hybrid memory circuits and also for standalone ruggedized logic operation in harsh environments [70-77]. For the application in harsh environment, more research and study in the reliability, encapsulation and structural designs are necessary in order to improve the overall performance of N/MEMS switches.

## 1.2 Background to the research

In practice, there is no technology base for temperature above 300 °C. The driving force is low since there are only few keen investors because most of the applications are limited to military, automotive, heavy industry and aerospace, as shown in Figure 1.2. Majority of the current HTE electronics are developed using either silicon or silicon-on-insulator technology. The usable range in Table 1.1 shows that these commercial products is yet to meet the industry's needs, as some of the requirements exceed the current applicable technology. In principle, the rule of thumb for the upper temperature limit of semiconductor is approximately 500 times of the bandgap energy as shown in equation (1.1) [78]. For example, maximum temperature of Si is approximately  $500 \times 1.12\text{eV} \approx 560\text{K}$ . As Si technology is limited by small bandgap, other possible areas such as N/MEMS switches, wide bandgap semiconductors and silicon carbide technology are being explored for possibility in rugged electronics application.

$$\textit{Temperature}_{max}(K) = 500 \times E(eV) \quad (1.1)$$

HT needs by industry sector		
	Industry sector	Temperature °C
	<b>Well-logging instrumentation</b>	
	Oil and gas wells	75-225
	Steam injection	200-300
	Geothermal wells	200-600
	<b>Aerospace</b>	
	Electronic braking systems	Up to 250
	Rack-mounted avionics	Up to 250
	Engine control/monitoring	Up to 300
	Smart skins	Up to 350
	<b>Industrial processing</b>	
	Various hot processes	Up to 600
	Fluid level monitoring	Up to 1,000
	Flame monitoring	Up to 600
	<b>Other industries</b>	
	Utilities	Up to 500
	Military	Up to 250
	Communications	Up to 250
	Heavy industrial equipment	Up to 300
	Space systems	Up to 600
	Air pollution control	Up to 550
	Nuclear reactor monitoring	Up to 550

**Figure 1.2: High temperature electronics requirement in different industry sector [6].**

In this chapter, the current available semiconductor technology and its challenges will be discussed. Meanwhile, literature survey on the current research status of N/MEMS switch in rugged electronics application are reviewed and presented.

**Table 1.1 Technologies available for HTE market [6, 79]**

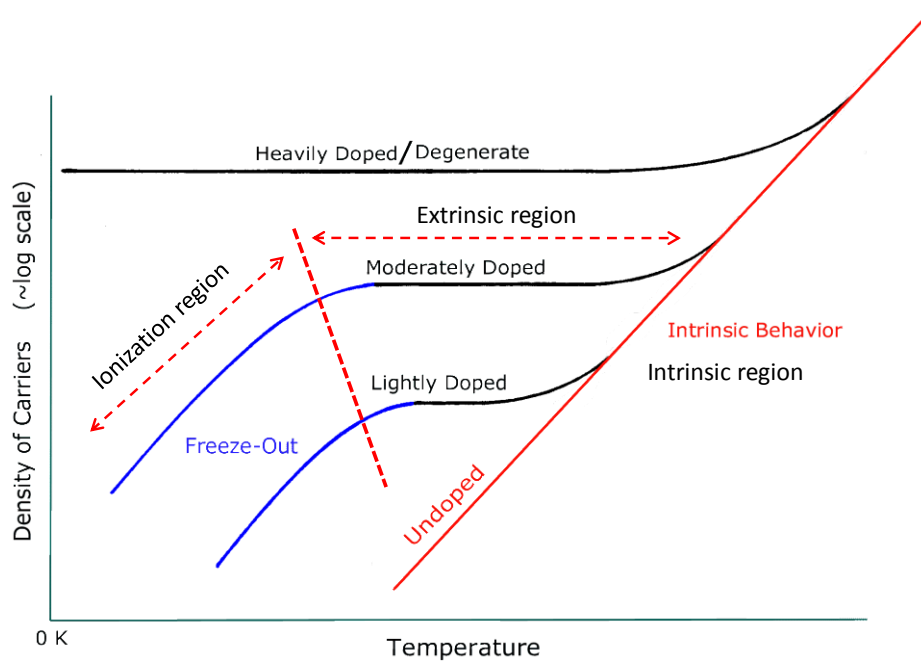
High Temperature Electronics Application	Peak Ambient	Chip Power	Current Technology
<b>Automotive</b>			
Engine Control Electronics	150 °C	< 1 kW	BS & SOI
On-cylinder & Exhaust Pipe	600 °C	< 1 kW	NA
Electric Suspension & Brakes	250 °C	> 10 kW	BS
Electric/Hybrid Vehicle PMAD	150 °C	> 10 kW	BS
<b>Turbine Engine</b>			
Sensors, Telemetry, Control	300 °C 600 °C	< 1 kW < 1 kW	BS & SOI NA
Electric Actuation	150 °C 600 °C	> 10 kW > 10 kW	BS & SOI NA
<b>Spacecraft</b>			
Power Management	150 °C 300 °C	> 1 kW > 10 kW	BS & SOI NA
Venus & Mercury Exploration	550 °C	~ 1 kW	NA
<b>Industrial</b>			
High Temperature Processing	300 °C 600 °C	< 1 kW < 1 kW	SOI NA
<b>Deep-Well Drilling Telemetry</b>			
Oil and Gas	300 °C	< 1 kW	SOI
Geothermal	600 °C	< 1 kW	NA

BS: bulk silicon, SOI: Silicon-on-insulator, NA: not presently available, WBG: wide bandgap.

### 1.2.1 Semiconductor transistor limits in harsh environment

The operating temperature limits of a conventional transistor depends on a number of factors including type of devices (bipolar transistor, field-effect transistor, device's design (geometry, technology node and dimensions), interconnects packaging (material and dimensions) and type of circuits (logic, memory or power electronics). In principal, electrical and thermal conductivity is a function of the density of states (conduction for electrons, valence for holes), the Fermi energy level and the temperature. As such, for different doping level, the intrinsic carrier density versus temperature is shown in Figure 1.3. At the cold extreme, depending on the doping concentration in the semiconductor, minimum thermal energy is required to

ionize the dopants in order to produce carrier in the semiconductor substrate. If the temperature is too low, inadequate ionizations can lead to insufficient carriers, resulting in a phenomenon called freeze-out. For Si, the minimum energy to overcome freeze-out is  $\sim 0.05$  eV, this is also referred as the ionization energy. In the extrinsic region, most semiconductors operate normally when impurity dopants are the source of carriers. However, at high temperature, the intrinsic carrier's density exceeds the dopant's concentration due to thermal excitation and causes the device to cease to operate normally [79-81].



**Figure 1.3: Semiconductor carrier's density change with respect to temperature. At high temperature, intrinsic carriers dominate and device's behaviour becomes unstable [79-81].**

In today's market, majority semiconductor transistors integrated circuits are metal-oxide-semiconductor-field-effect-transistor (MOSFET). In transistor

physics, the major current leakages are fundamentally tied to the intrinsic carrier concentration ( $n_i$ ). Since intrinsic carriers are understood to be exponentially proportional to temperature, hence the turn-off characteristics of the device are principally governed by the temperature dependent leakage current [82-84]. At higher temperature, the inversion channel is disrupted by the surge in leakage current contributed by the thermally excited intrinsic carriers. This phenomenon exists in Si bandgap transistors, which is a disadvantage in rugged electronics. The effect reinforced by the conventional temperature limits in most standard electronics datasheet that usually specifies -40 °C to 125°C. Overall, conventional silicon semiconductor had shown insufficient capability to operate in high temperature.

### **1.2.2 Existing high temperature electronics devices**

As silicon bandgap is insufficient for high temperature electronics, researchers turn their attention to SOI and wide bandgap semiconductors such as III-V compound and silicon carbide (SiC). The first effectively suppress the leakage current, and physically drives silicon transistor to maximum temperature up to 250 °C. There were some successes reported in the latter mostly at research level, where results are reported with fundamental theoretical simulations and basic practical synthesis. Furthermore, III-V compound and SiC fabrication remain challenging and material exotic until now. This means enormous

breakthrough in the development of integration and high quality substrates is still pending for the technology to advance to the next level.

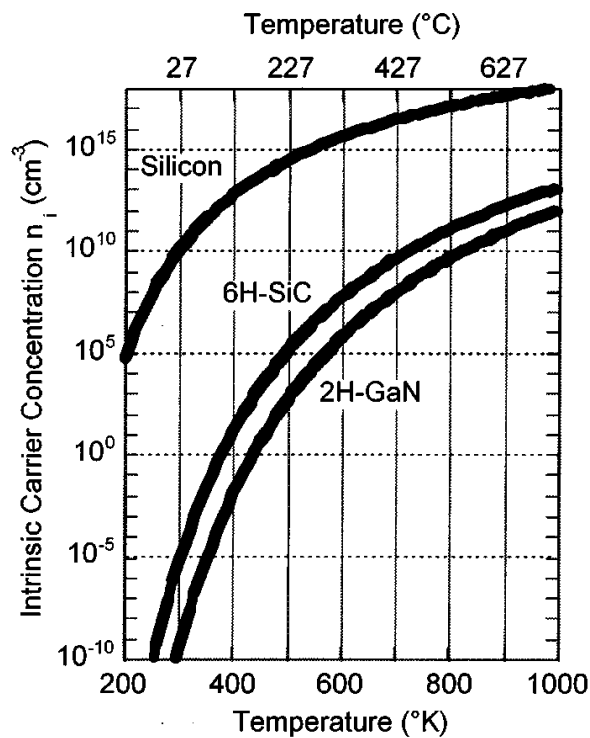
#### **1.2.2.1 Silicon on insulator**

The sub-threshold and substrate leakage ( $I_{CL}$ ,  $I_{SL}$ ) in Si transistor can be greatly suppressed using silicon-on-insulator technology, as the thin Si on SiO<sub>2</sub> dielectric stacking allows the N-MOSFET to be isolated better from the substrate. Hence the device can endure higher temperature before leakage current becomes large enough to cause device failure. The leakage current reported can be three orders lower than the transistor built on bulk silicon substrate [9, 85]. High temperature electronics based on this technology has been well developed and successfully commercialized by Honeywell Corp. [86, 87]. However, the usable range of the device is only from -55 °C to 250 °C. The overall SOI technology is sufficiently mature for high temperature electronics < 250 °C. For higher temperature, alternative technology has to be developed.

#### **1.2.2.2 III-V material compound transistor and SiC technology**

Despite limited processing technology of compound epitaxy, III-V compound and silicon carbide have taken a step forward in semiconductor electronics other than its success in opto-electronics [13, 15, 88-93]. Due to wider

bandgap, SiC (2.4 – 3.26 eV) and GaN (3.14 eV) have lower intrinsic carrier's density than Si as shown in Figure 1.4, which makes them favourable for high temperature electronics [26, 80, 94-96]. The development in high electron mobility transistor (HEMT) using GaN (3.14 eV) has shown high temperature operation > 300 °C. At research level, a reliable HEMT based digital inverter functioning at 375 °C has been demonstrated by Yong *et al* [97-99].



**Figure 1.4: Comparison of silicon, 6H-SiC, and 2H-GaN intrinsic carrier concentration ( $n_i$ ) versus temperature [79].**

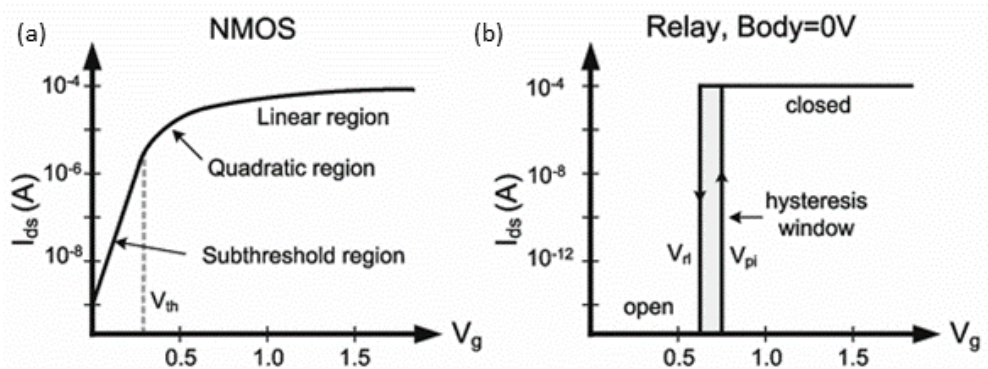
Meanwhile, small scale manufacturing of SiC MOSFET power transistors has been demonstrated by Cree Inc [17, 100, 101]. However, the current confirmed maximum operating temperature is only 200 °C and has not met the criteria of the rugged electronics application.



Challenges in developing III-V compound and SiC rugged electronics lies in the device integration. In both materials' integration, crystal dislocation and lattice matching is a major task, involving exotic processes and equipment. These processes usually include metal-organic chemical vapour deposition (MOCVD), vapour phase epitaxy (VPE) or molecular beam epitaxy (MBE). At the wafer level integration, substrates such as sapphire substrate or single crystal SiC substrate are needed [102-111]. The single polytype SiC substrate are made using a process called "Lely" where crystals are grown at temperatures above 2000 °C from a polycrystalline powder source [112-115]. The challenges above have limited wafer level integration to 2 – 4 inch wafer and have significantly affected economic of scales. Furthermore, III-V material such as indium and gallium belongs to rare earth material and can be of higher cost compared to abundant silicon. Meanwhile, as the material doesn't form native oxide itself, dielectric incorporation and adherence is still a difficult task. In general, more radical improvement in crystal growth, material quality and integration methods is necessary to realize the wide bandgap high temperature electronics, thus an alternative solution such as N/MEMS switches is being explored and researched.

### 1.3 State of the art N/MEMS switch

Problematic operation of semiconductor devices in high temperature is also manifested by device's self-heating. As the internal junction temperature heats up during operation. On the contrary, a junctionless device such as N/MEMS switch is favourable. Nano/microelectromechanical (N/MEMS) switch is a nano/micro-size device able to alter between two or more states and usually made of multiple movable and fixed electrodes. N/MEMS switches are able to offer several unique features, such as near-infinite sub-threshold slope, near zero leakage and the potential for operation in harsh environment [26, 116-122]. A good comparison of the switching characteristics between NMOS and N/MEMS switch is shown in Figure 1.5.



**Figure 1.5: (a) Switching characteristics of a NMOS with sub-threshold swing. (b) Steep sub-threshold rise and fall of a micro switch**

Unlike its bulk version, N/MEMS switch is not human hand operated and can be categorized into two major types: passive and active switch. Passive switch

is triggered through environmental energy transduction (e.g. magnetic reed switch [123, 124], latching shock switch [125, 126]) while active switch's state is configurable by deliberately applying known triggering signal (e.g. Radio frequency (RF) MEMS switch [127-129], logic switch [122, 130-133]). Despite proven functionality and application, reliability and structural integrity continues to haunt N/MEMS switch in high temperature environment, as surface degrades rapidly through continuous cycling and the structural reliability is still questionable. This technology's developments need to be optimized, designed and breakthrough before real product can be finally commercialized. Table 1.2 summarizes the features offered by different technology for high temperature and rugged electronics [27, 92, 134]. In this context, it is noted that, N/MEMS switch cannot replace all the functionality of conventional electron devices. For example, N/MEMS switches are not able to replace the analog/passive function in a circuit.

**Table 1.2 Summary of technology in high temperature electronics  
[27, 92, 134]**

Property	Technology				
	Silicon	Silicon-on-Insulator	III-V compound	Silicon Carbide	N/MEMS switch
Max Temp (°C)	<150	< 250	< 350	> 600	> 500
Status	Commercial	Commercial	Research	Research	Research
Functions	Analog, memory, controller,	Analog, memory, controller	RF, power devices	Power electronics	Memory, controller
Gate-length (nm)	14	14	32	65	Nano-size
CMOS	Yes	Yes	No	No	Yes

### 1.3.1 Electrostatic N/MEMS switch

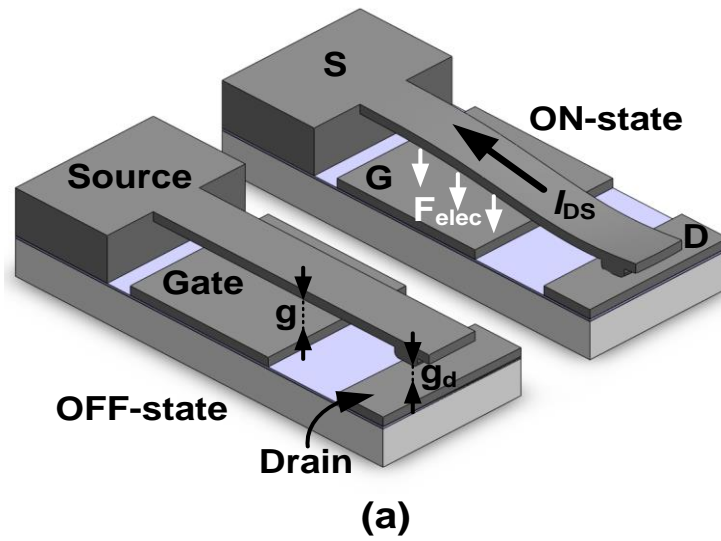
There are four major actuation mechanisms in N/MEMS switches being vastly researched. i.e.: Electrothermal, piezoelectric, electrostatic and electromagnetic. Table 1.3 shows a summary of advantages and disadvantages between different N/MEMS actuation mechanisms [135-153]. In this thesis, electrostatic actuation is chosen because of its outstanding features compared to other mechanism in N/MEMS switches for harsh environment application. First, it is shown that electrostatic actuation is unsusceptible to temperature change in contrast to piezoelectric or electromagnetic devices' Curie

temperature limit [154-157]. Meanwhile, the capacitive based principal allows ideally zero power consumption and fast actuation compared to electrothermal devices. Furthermore, the fabrication process of an electrostatic device is relatively straightforward despite challenges when low voltage operation is desired. Overall, electrostatics N/MEMS switch is the most suitable candidate to be implemented in high temperature electronics. The main design parameter to switch operation is the pull-in voltage  $V_{PI}$ , which is related to the dimension of the switch. Figure 1.6(a) shows the standard operation of three-terminal electrostatic switches. This switch consists of a cantilever beam (source terminal), a control (gate terminal) and a signal (drain terminal). The cantilever is a free moving structure anchored on the substrate. The drain and gate terminal are both fixed and not movable. An air-gap separates the source and drain terminals in the off-state, so that no current can flow between these electrodes, i.e.  $I_{OFF} = 0$ . During on state, a potential bias is applied between gate and source and this actuates the cantilever due to the electrostatic attraction. When this potential reaches the pull-in voltage, the beam become unstable and pulled-in towards the gate and simultaneously makes contact with the drain. In a normal configuration, a dielectric layer exists between gate and source that prevents signal loss between the two. Under such circumstances, the gap between the drain and source ( $g_d$ ) is naturally smaller than the gap between gate and source ( $g$ ).

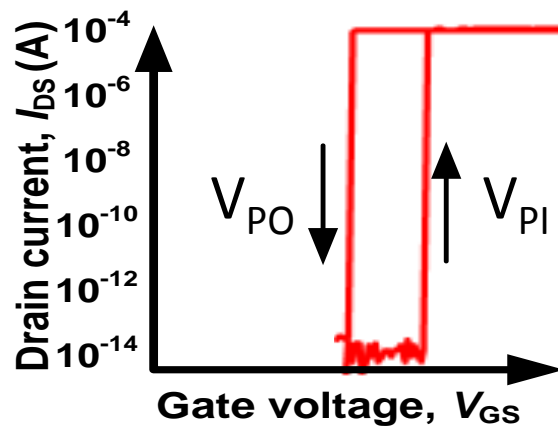
**Table 1.3 Comparison of N/MEMS actuation mechanisms  
[135-153], [154-157]**

Electrothermal	Piezoelectric	Electrostatic	Electromagnetic
<b>PROS</b>			
<ul style="list-style-type: none"> <li>▪ Easy to fabricate by conventional process and material</li> <li>▪ Low actuation voltage</li> <li>▪ High contact force, and low contact resistance</li> </ul>	<ul style="list-style-type: none"> <li>▪ Low actuation voltage</li> <li>▪ Bi-direction actuation</li> <li>▪ Low power consumption</li> </ul>	<ul style="list-style-type: none"> <li>▪ Demonstrated <math>10^7</math> cycles</li> <li>▪ High operation frequency</li> <li>▪ Low active power consumption</li> <li>▪ Easy to fabricate by conventional process and material</li> <li>▪ Insensitive to temperature</li> </ul>	<ul style="list-style-type: none"> <li>▪ Nonvolatile operation</li> <li>▪ Bi-direction actuation</li> </ul>
<b>CONS</b>			
<ul style="list-style-type: none"> <li>▪ High active power, current dependent</li> <li>▪ Large footprints</li> <li>▪ Large thermal drift</li> <li>▪ Uni-direction actuation</li> </ul>	<ul style="list-style-type: none"> <li>▪ Material dependent fabrication</li> <li>▪ Curie temperature dependent</li> </ul>	<ul style="list-style-type: none"> <li>▪ High actuation voltage</li> <li>▪ Uni-direction actuation</li> </ul>	<ul style="list-style-type: none"> <li>▪ Material dependent fabrication</li> <li>▪ High active power consumption</li> <li>▪ Large footprint</li> <li>▪ Curie temperature dependent</li> </ul>

Figure 1.6 (b) shows the typical measured curve for an N/MEMS switch. An abrupt increase in current during gate voltage sweep ( $V_{GS}$ ) depicts a pull-in phenomenon and this is associated with the pull-in voltage ( $V_{PI}$ ). As the voltage sweep returns to zero, the beam is restored to its initial position. The potential bias when this happens is referred as the pull-out voltage ( $V_{PO}$ ).



### Measured $I$ - $V$ plot



**Figure 1.6: Operation of electrostatic switches. (a) Operation of electrostatic switches in OFF and ON states. (b) Typical voltage sweeping curve of electrostatic switches.**

Analytical models for electrostatic pull-in are well established for such switch.

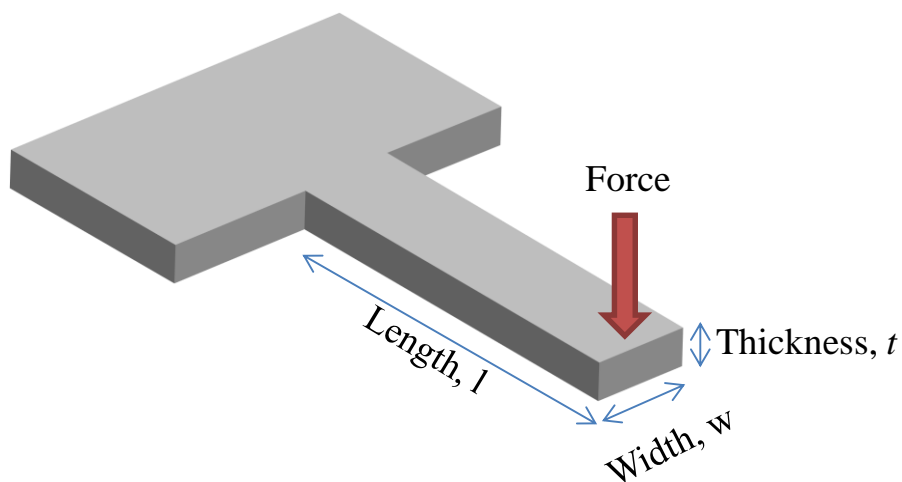
The pull-in voltage, given in equation (1.2), is well established from parallel plate capacitor theory by assuming no fringing field [20, 26, 158, 159].

$$V_{on} \approx \sqrt{\frac{8k_{eff}g^3}{27\varepsilon_0A}} \quad (1.2)$$

Where  $k_{eff}$  is the effective spring constant of the system,  $g$  is the gap between the movable and stationary electrode,  $\varepsilon_0$  is the permittivity of free space and  $A$  is the area of effective electrostatic force. The simple cantilever spring constant is derived by the Euler-Bernoulli model and takes the form of equation (1.3)

$$k_{eff} = Ew \frac{t^3}{4l^3} \quad (1.3)$$

Where  $E$  is the Young's Modulus of the material,  $h$  is the height,  $w$  is the width,  $l$  is length as shown in Figure 1.7.



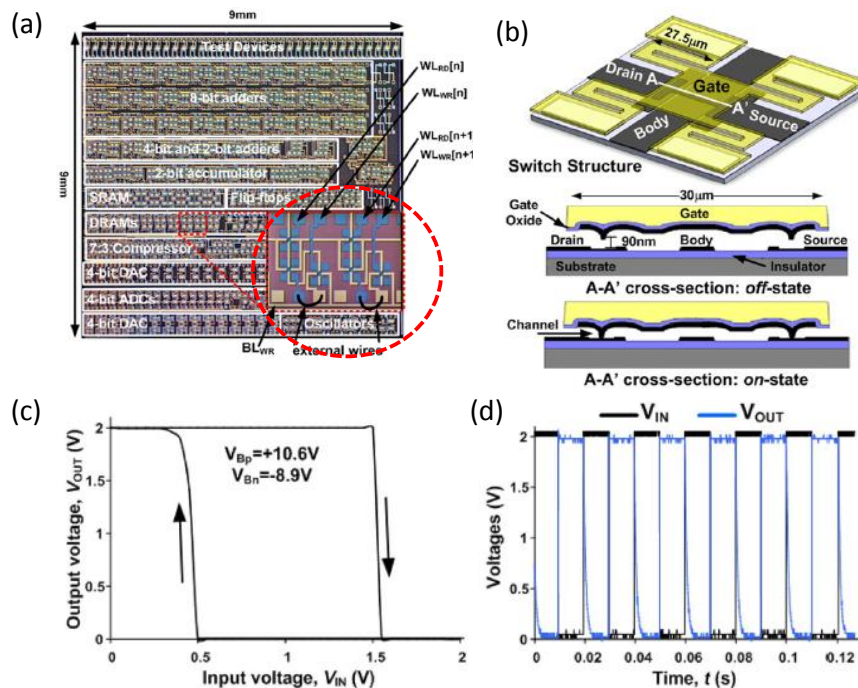
**Figure 1.7: Dimension parameter of a typical cantilever beam.**



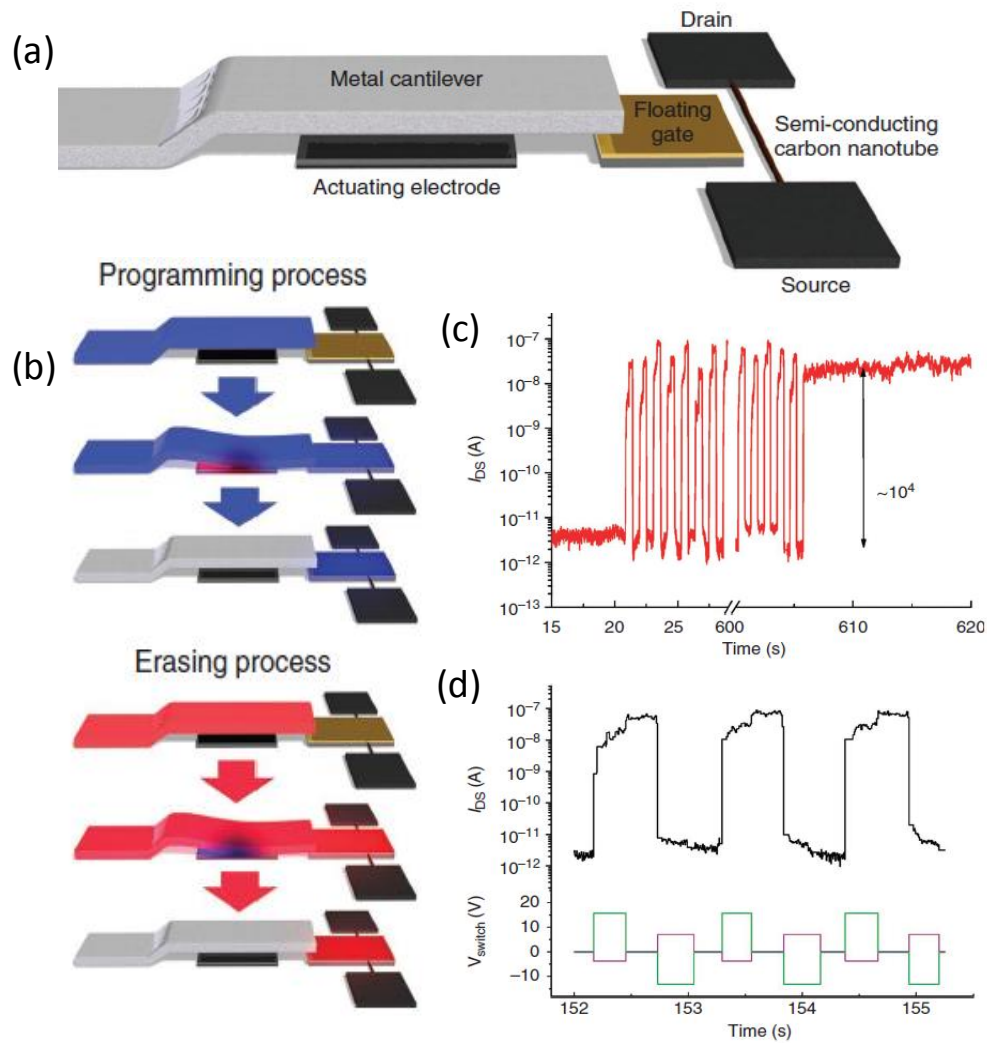
It is well noted that the pull-in voltage exponentially increases proportional to the effective gap of the actuation,  $g^{3/2}$ , hence to achieve low  $V_{PI}$ , the gap has to be as small as possible, which is typically  $< 1 \mu\text{m}$ .

### 1.3.2 N/MEMS switches: Memory and logic devices

There have been a few exciting development in functional integration of N/MEMS switch to date. Both Chen *et al* and Park *et al* demonstrated complementary N/MEMS to CMOS, also known as a hybrid N/MEMS – CMOS technology [41, 160].



**Figure 1.8:** (a) Die photo of the hybrid N/MEMS-CMOS chip. (b) layout and cross-section of the N/MEMS switch. (c) Voltage transfer characteristic showing hyper abrupt transitions between logic states. (d) Timing diagrams for 2-V, 50-Hz operation [41, 160].



**Figure 1.9:** (a) Schematic diagram of the MEMS-based non-volatile memory device. The CNT is used for the source/drain channel and a MEM cantilever is added to transfer charges to the floating gate. (b) Diagrams demonstrating the programming (upper three panels)/erasing (lower three panels) processes. Blue/red colours indicate the polarities  $\pm$  of the applied voltages. (c) Memory endurance operation under repeated programming/erasing cycles for the side-floating gate device. The test was performed over 500 cycles for 600 s with  $V_{ds} = 100$  mV. (d) Expanded section of (c) also showing the voltages applied to the cantilever (purple line) and activating electrode (green line) [41, 160].

The first hybrid MEMS switch inverter is monolithically integrated on CMOS die. The device has shown 10 times lower energy over conventional CMOS

circuits with 20 – 30  $\mu$ s mechanical delay. This device is shown in Figure 1.8. Meanwhile, complementary N/MEMS with erasing speed faster than the Flash memory is demonstrated by Park *et al.* At 145 ns, the data erasing operation is boosted at least 5 times faster than the current Flash technology. The device schematics and operation is shown in Figure 1.9.

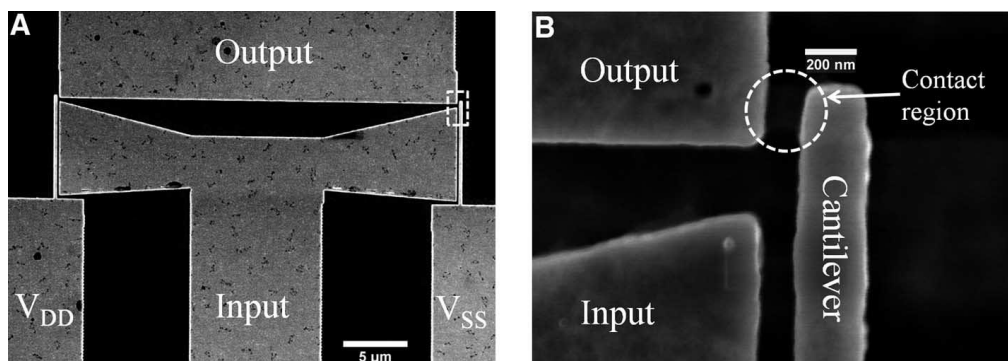
### **1.3.3 N/MEMS switch: Material selection**

Mechanical contact switches are known to suffer from a certain degree of degradation after every operation, especially at high temperature. Reports suggest that high current density, hot switching and high impact velocity may also causes switch micro-welding, fracture, contact surface degradation and oxidation that will eventually leads to failure [32, 161-166]. The severity in degradation is commonly associated with the contact material [56, 167-170]. Hence material property such as hardness, melting point and resistivity are crucial in surviving harsh environment application. Nonetheless, CMOS compatible materials are more favourable due to its cost effectiveness and established manufacturability.

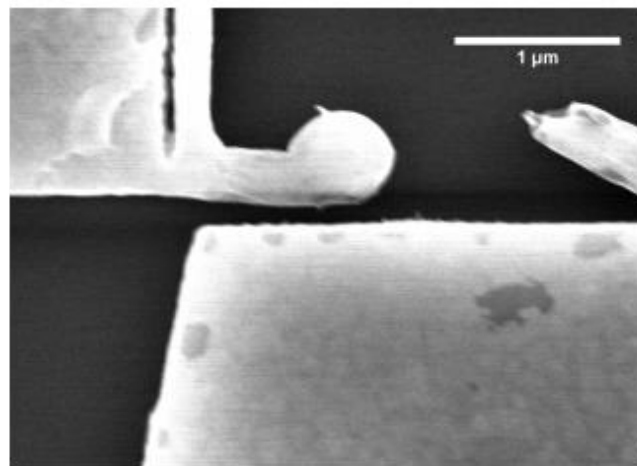
#### **1.3.3.1 Silicon Carbide**

In year 2010, a highly reliable NEMS switch based on SiC was reported by Lee *et al* [39]. The all mechanical single device successfully verified inverter

operation at 500 °C for at least 2 billion cycles. Figure 1.10 shows the SiC based inverter and the details of the contact. Despite the impressive finding, the device suffers from localized Joule heating and the failure is shown in Figure 1.11.



**Figure 1.10: (a) SEM of an inverter device. (b) zoom-in of the highlighted contact [39].**

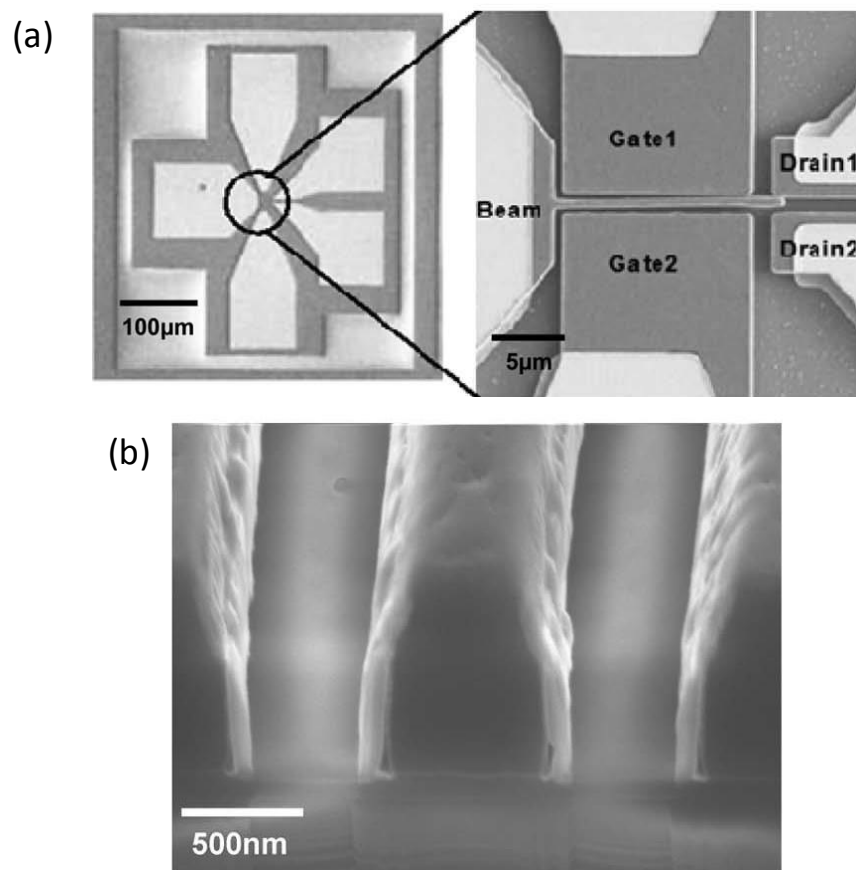


**Figure 1.11: Localized Joule heating resulting in melting of SiC [39].**

### 1.3.3.2 Metal and metal oxides

Alternatively, metallic contact N/MEMS switches are reported as well. The high conductivity of metal is indisputably the best advantage in lowering

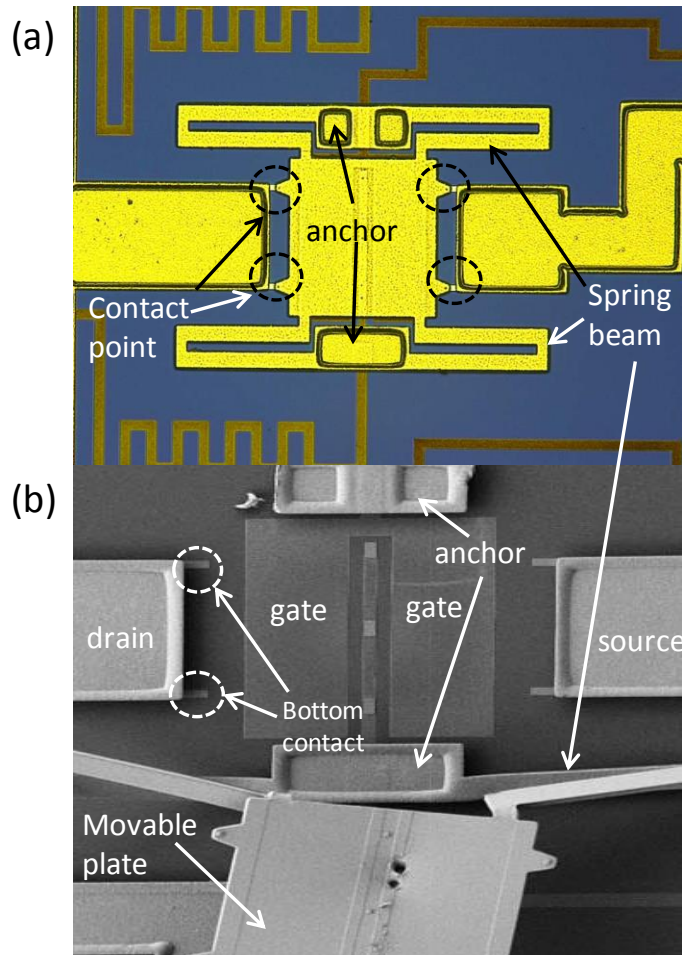
contact resistance. In year 2013, a platinum coated silicon beam N/MEMS switch with 3 k $\Omega$  contact resistance was reported by Parsa *et al* [171]. At least 10<sup>8</sup> cycles at room temperature were successfully verified and device have shown possible low power application. The SEM and the detail of the platinum coated device are shown in Figure 1.12.



**Figure 1.12: (a) SEM images showing actuation of a five terminal polysilicon switch coated with platinum on the sidewalls and selected top surfaces. (b) SEM cross section of unreleased platinum-coated beams [171].**

In the same year, there has been some success with metal to metal oxide interface such as Au to RuO<sub>2</sub> that shows more than 10<sup>10</sup> cycles operation

under normal temperature [28]. The device is shown in Figure 1.13.



**Figure 1.13: (a) Optical micrograph showing the switch design. Four folded springs are attached to an anchor point on the wafer, and the opposite sides are connected to the edges of a rectangular plate. Four dimples connect to two signal lines on opposite sides of the switch. (b) SEM of the device with moving plate broken and shift aside to reveal gate and bottom contact area [28].**

### 1.3.3.3 Other materials

There are also other unconventional material such as silicon-germanium, titanium dioxide, molybdenum, amorphous carbon coating and others. Table 1.4 shows the comparison of the recent development in N/MEMS switches

lifetime and operation in high temperature. Despite high temperature capability mentioned by most of the reports, note that the only experimental results for high temperature are demonstrated by Mehregany *et al* at 500 °C.

**Table 1.4 Comparison of lifetime and temperature study of different N/MEMS switches**

Institution	Beam material	Contact	Lifetime	Testing pressure	Temp (°C)	Ref.
Case western University	SiC	SiC-SiC	$2 \times 10^9$	Vacuum	RT-500	[31, 39]
Berkeley University	Poly-Si Ge	W-W	$10^9$	N2	RT	[47]
University of Berkeley	W	TiO <sub>2</sub> -TiO <sub>2</sub>	$10^9$	N2	RT	[172]
KAIST University	TiN	W-TiN	$< 10^3$	In air	RT	[173]
Sandia Lab	Au	RuO <sub>2</sub> – Au (beam)	$10^{10}$	N2 / O2	RT	[28]
Stanford University	Poly Si	Pt coat- Pt coat	$10^7$	In dry N <sub>2</sub>	RT	[171]
University of Berkeley	Ru	Ru-Ru	$2 \times 10^6$	vacuum	RT	[170]
IBM Lab	Si	A-C to A-C on Pt/Au	$10^8$	NR	RT	[174]

## **1.4 Silicon as N/MEMS switch**

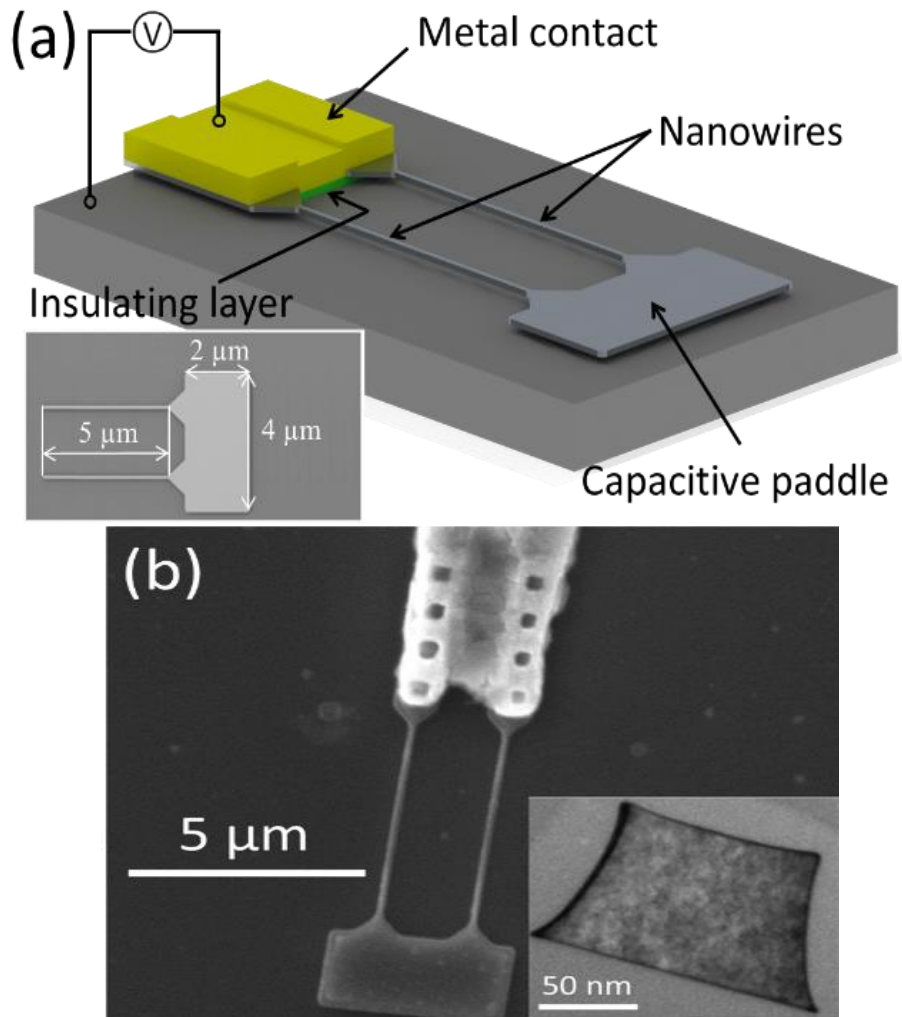
Silicon has high melting point of 1414°C, Mohs hardness scale of 7 and relatively high Young's Modulus of 130-188GPa, which makes it one of the most appropriate material in terms of reliability, adequately hard material and suitable in low operating voltage design [175]. Other than CMOS compatibility, Si is one of the most applicable platforms in micromachining fabrication, where most of the process technologies are developed surrounding Si material, making Si the most established material in N/MEMS micromachining. However, oxidation poses a huge challenge as contact interface experiences a great deal of oxidation when current flows through the uneven surface asperities. Hence an encapsulation package or vacuum level testing is required to enhance the reliability of Si based N/MEMS switches.

### **1.4.1 Nano-size dimension of Si based N/MEMS switch**

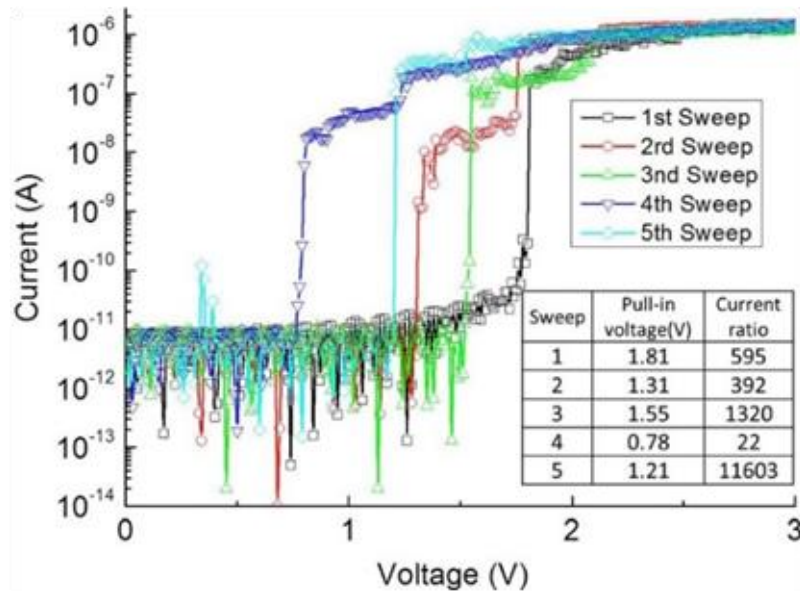
Si technology is regarded as the epitome in the history of semiconductor. The widely available database in device and process technology highly surpasses any other semiconductor material. As CMOS scaling quest travels, Si fabrication has taken huge leaps in process technology. Since then, extreme patterning capability is enabled. In 2012, Qian *et al* demonstrated a dual silicon nanowires switch with a paddle-like contact for low power computing and alternative to CMOS scaling [133]. The Si based nanowires has enable



low operating voltage and possible high density configuration. The device is shown in Figure 1.14. The low actuation voltage of average 1.12 V has shown  $10^4$  orders of on/off ratio as shown in Figure 1.15.

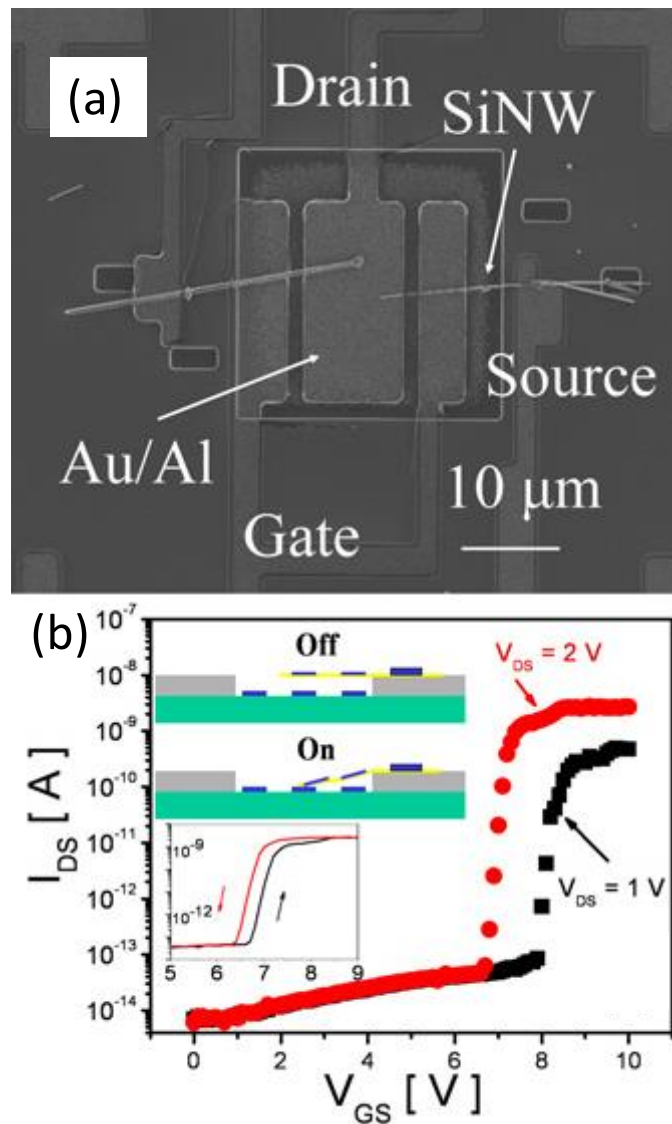


**Figure 1.14: (a) A schematic illustration of the U-shape NEMS switch. (b) SEM photo of a U-shape NEMS switch after HF vapor releasing, Inset: TEM image of a SiNW cross-section [133].**



**Figure 1.15: I-V characteristic of the device. For the first five switching cycles, the current ratio indicates the change in current that occurs within 10 mV of the pull-in voltage.**

Meanwhile, Li *et al* has demonstrated fabrication and characterization of Si based nanowire for logic application [81]. Two-terminal and three-terminal devices are demonstrated. The SEM images of three-terminal device are shown in Figure 1.16(a). The Si based nanowires are pulled in to contact the drain as gate voltage is applied at the gate terminal. The I-V characteristics are shown in Figure 1.16(b). The pull-in voltage of this switch is approximately 8 V. The devices have negligible power consumption in the off-state and very small switching energy. The nano-size (30-300 nm in diameter) of the Si based nanowire has shown promising features and possibility in low power, high density computing.

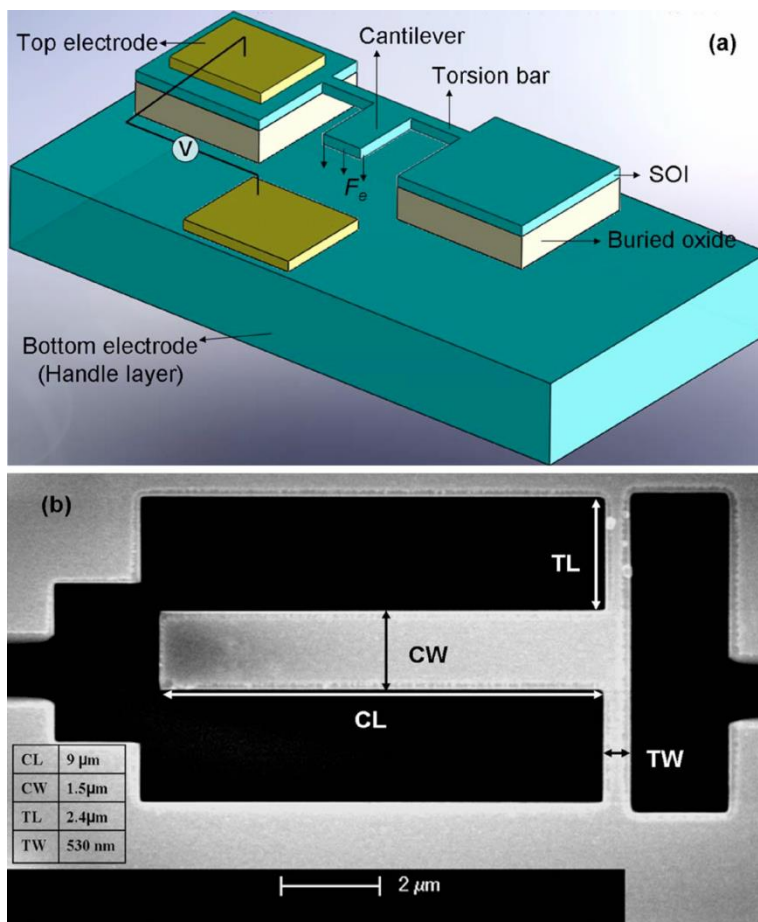


**Figure 1.16:** (a) SEM image of two 3T switch; (b) The typical switching current–voltage characteristics of the 3T switch. The inset shows the switch on/off diagram and the hysteresis of  $I_{DS}$ – $V_{GS}$  as the gate voltage is swept from  $V_{GS} = 0$  to 9.0 V and then back to 0 V at  $V_{DS} = 2.0$  V [81].

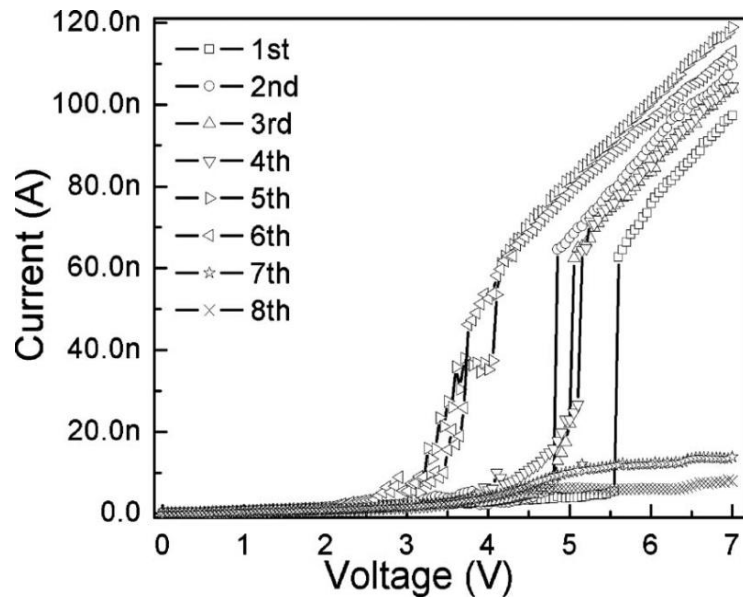
#### 1.4.2 Si based N/MEMS non-volatile memory

On top of low voltage power computing and high density computing, Si based non-volatile memory has been demonstrated by Xiang *et al* [18]. By leveraging on a 220 nm suspended Si cantilever supporting by torsional

spring, the device has demonstrated low power actuation. The SEM diagram of the device is shown in Figure 1.17. Low operating voltage of 5.5 V is reported and the device has shown possible high density in random access and non-volatile memory application. The measurement result is shown in Figure 1.18.



**Figure 1.17: A schematic illustration of the NEMS torsion switch device. (b) SEM photo of a NEMS torsion switch after HF vapour releasing. The dimension: CL, CW, TL, and TW of device are 9 μm, 1.5 μm, 2.4 μm, and 530 nm respectively [18].**



**Figure 1.18: I-V characteristic of the device for multiple operations [18].**

Despite exceptional features, the memory operation demonstrated by the device still relies on CMOS based charge layer storage to realize a non-volatile memory. In all mechanical computing for harsh environment, charge layer free or mechanically bi-stable operation is preferred.

### **1.4.3 Reliability in high temperature**

Regardless of above demonstration, little is known about the reliability and failure mechanisms of Si based N/MEMS switches, especially under high temperature. The only reliability investigated in high temperature is SiC switches as described in section 1.3.3.1. Nonetheless, Si technology has stronger fabrication database than SiC and the limit of Si based contact has not been reported so far. Thus it is worthwhile to investigate the reliability of Si

based contact in high temperature. Furthermore, most test configuration in Table 1.4 emphasize on testing in vacuum. This shows that N/MEMS switch requires vacuum or a clean environment in order to survive longer and thus increases lifetime. Therefore, encapsulation development is important in order to provide a pristine environment to N/MEMS switch. In that case, realistic characterization results can be obtained.

#### **1.4.4 Operation reliability in high acceleration**

In future, miniaturized satellite systems will replace the current bulky version as technology advances. N/MEMS switch capability to withstand high temperature is favorable to be implemented in the electronics in such machine. However, the operation during high acceleration or g-force during the launch or take-off experienced by the N/MEMS is still unknown. The typical acceleration during a rocket launch is 2 – 5 g [176, 177]. In contrast to conventional electronics circuits, the small movable parts in N/MEMS switches can be affected by the high acceleration g force. The beam acts as a proof mass in N/MEMS switch. Under high acceleration, the beam may displace and hence it is important to study the characteristics of the N/MEMS switches under high acceleration.

### 1.4.5 Secondary pull-in phenomenon

Another undesired property of N/MEMS switches is secondary pull-in [151, 171, 178] other than contact degradation. This phenomenon increases the risk in catastrophic N/MEMS failure. The failure happens when the moving terminal contacts the gate terminal, resulting in a short circuit or burning the device. Some of the catastrophic failures are shown in Figure 1.19. High current flow from source to gate may generate enormous amount of heat that can eventually burn the device. The condition become more severe as the contact area is proportional to the gate voltage, which depicts an operation voltage range of N/MEMS switch as shown in Figure 1.19(b). The phenomenon of secondary pull-in is illustrated in Figure 1.20. For cantilever beam designs, secondary pull-in can occur when the gate voltage is overdriven, and the excessive electrostatic force causes the beam to contact the gate, resulting in a short circuit and device failure. This may also happen during gate voltage spikes. Some reported MEMS switches implement a layer of dielectric insulation such as alumina ( $\text{Al}_2\text{O}_3$ ) or silicon dioxide ( $\text{SiO}_2$ ), between the gate and the actuation beam to prevent secondary pull-in and catastrophic short circuits [41, 47, 179]. However, the implementation of dielectric layers furthers impedes the operating voltage of the device. As it increases the effective gate between the gate and drain terminal.

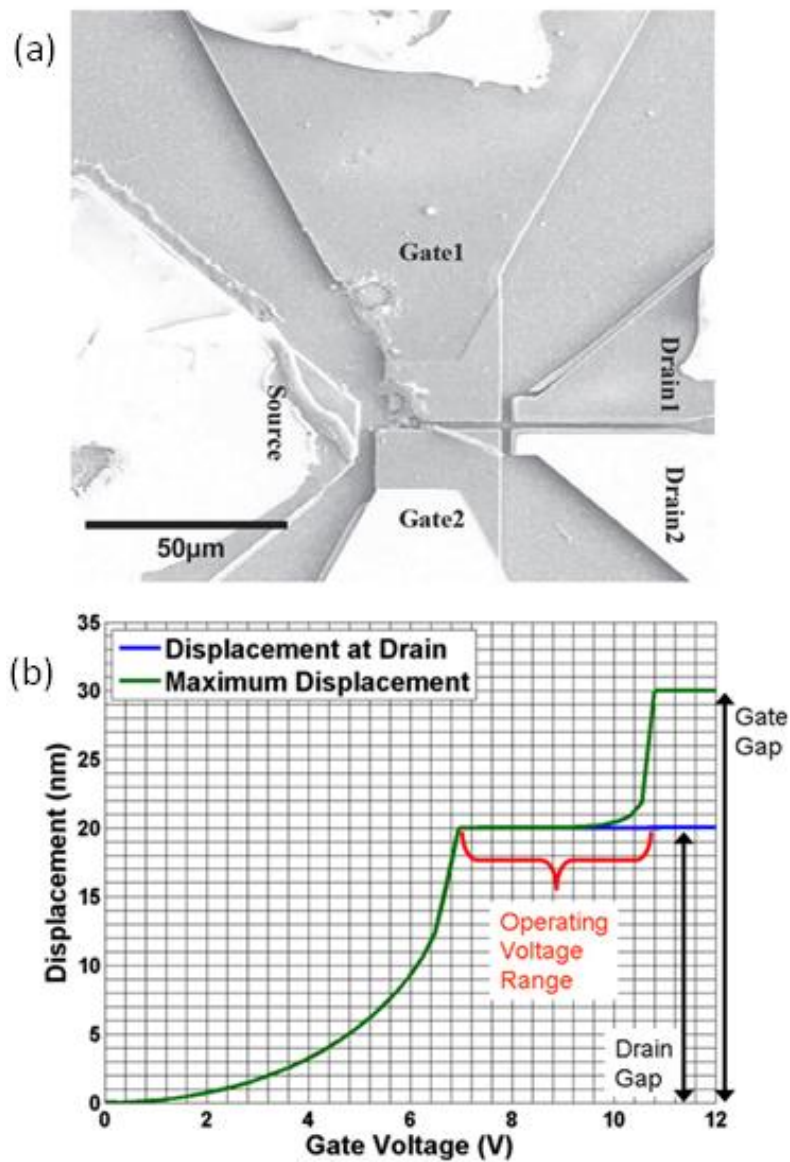
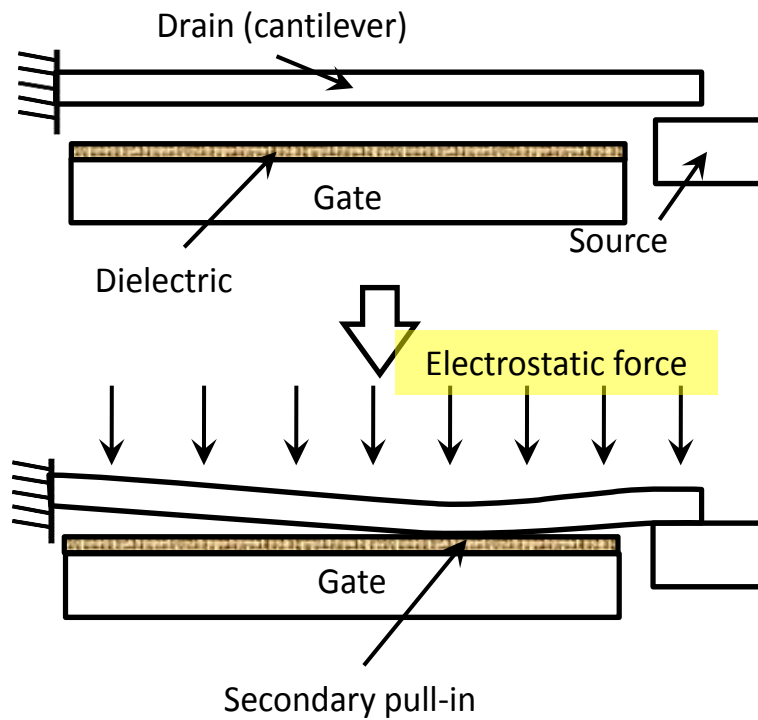


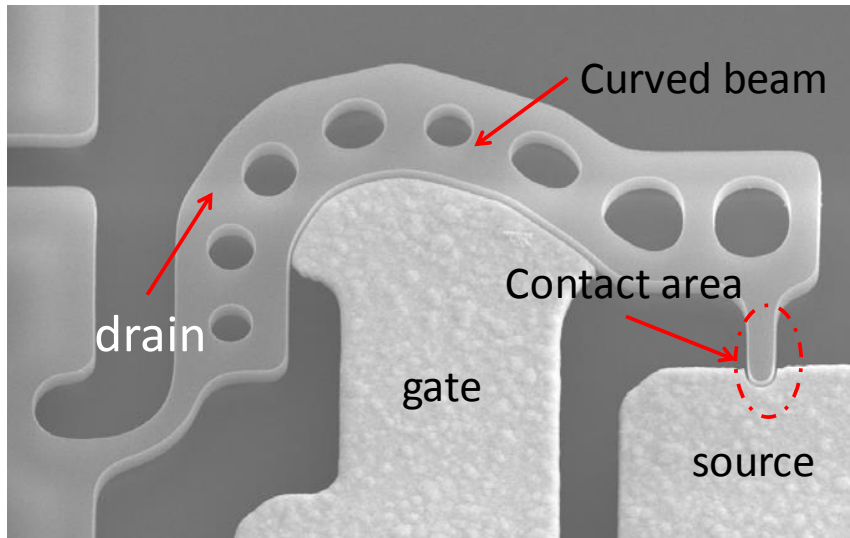
Figure 1.19: (a) SEM image of a five-terminal switch after electrostatic actuation. High current flow between the beam and the gate after shorting causes irreversible damage. (b) Plot of the displacement of the source at the gate and the maximum displacement of the source as a function of gate voltage for a N/MEMS switch. The source pulls in to the drain at approximately 7 V. As the voltage is increased, the source shorts to the gate at approximately 11 V. The difference between these two voltages is the operating voltage [189].





**Figure 1.20: Illustration of secondary pull-in for free-end cantilever beam, double-clamped beam.**

High breakdown voltages have also been reported with an inclined curved electrode with rotation around small hinges, as reported by Grogg *et al* [194]. The SEM image of the device is shown in Figure 1.21. However, such hinge placement imposes higher flexibility in horizontal  $x$ -direction and may cause breakdown earlier than a perfect circular beam. Another disadvantage of the switch is the large size of the switch is in hundreds of micro-meter, which is not favorable for high density application.



**Figure 1.21: SEM image of the curved beam switch showing three terminals: drain, gate and source. The contact area is depicted by dashed line [194].**

## **1.5 Motivation and objective**

The primary focus of this work is to able to achieve a silicon based N/MEMS technology that can be embedded into low level logical computational operation and memory, with enhanced device reliability in harsh environment application. Silicon contact is chosen due to its high melting point and well established database in current semiconductor industry. Nano-size structures can be well developed using Si and this is important to realize high density devices. In a non-volatile memory demonstration, a new mechanical latching concept is attempted based on van der Waals force surface adhesion. This idea allows charge storage layer free memory to be developed in order to create all-mechanical computing devices. Meanwhile, novel idea in modifying straight cantilever to curved cantilever is attempted to improve the spring

stiffness against secondary pull-in failure. To realize a logic computation in harsh environment with improved performance, the Si based three-terminal switch is encapsulated in vacuum with wafer level packaging technology. The vacuum level encapsulation is shown to slowdown the degradation of the switch under high temperature environment. Multiple testing is performed systematically to characterize the switches. In this context, standard I-V characterization, and more ruggedized testing in high temperature ( $> 300^{\circ}\text{C}$ ) is performed to investigate the reliability and lifetime of these Si based switch. After that, the operation of the switch is investigated under high acceleration ( $< 10\text{ g}$ ) using a shaker equipment. The purpose to test the switch operation under acceleration up to  $10\text{ g}$  is to determine the device can withstand the stress under such environment. For example, the typical acceleration during a rocket or satellite launch is  $2 - 5\text{ g}$  [176, 177]. In contrast to conventional electronics circuits, the small movable parts in N/MEMS switches can be affected by the high acceleration  $g$  force. Thus it is important to study the characteristics of the N/MEMS switches under such acceleration. With all this, hopefully this technology can be materialized and new exploration in related field such as material improvement and circuitry assembly is initiated, leading to an entirely new technology platform.

## **1.6 Organization of thesis**

In accordance with the motivation and objective of the current work as mentioned in section, this thesis is divided into seven chapters and these chapters are organized as of below:

Chapter 1 is a general introductory of the current problem statement. The limitation of existing technology as well as technology currently in research are reviewed and discussed. After that, N/MEMS switch technology are proposed and justified. A literature review on the current research and development status is covered to examine the underlying challenges and produces better and novel ideas, especially on the reliability and failure of N/MEMS switches in high temperature environment.

Chapter 2 proposed the concept of the mechanically bi-stable silicon nanofin (SiNF) that is electrostatically actuated and possess the features similar of a non-volatile memory (NVM). Analytical model of the SiNF's critical length is derived in order to define SiNF non-volatility effectively. The SiNF is simulated with proper boundary condition in ANSYS finite element simulation. Finally a design of experiment (DOE) comprised of different length and width is determined and translated into a reticle layout. The layout is then meticulously patterned on to semiconductor wafers and

multiple layers of critical process are performed in order to realize the feature designed. These steps include critical dimension lithography, deep reactive ion etching, nano-size gap formation, electrode definition and device release. Fabrication outcome is lastly presented in the form of scanning electron micrographs (SEM).

Chapter 3 contains all the characterization and analyses of the bi-stable SiNF non-volatile memory. First the testing set up is briefly introduced and the electrical characterization of the SiNF switch is explained. The most important measurement: Non-volatile I-V characteristics is measured and presented. Clear set and reset functions, represented by the pull-in voltages of the SiNF switch is measured and investigated. Overall the non-volatile hysteresis window agrees well with the model based on van der Waals force surface attraction. The contact area is further analysed to differentiate between a logic and memory due to the van der Waals force. The nanosecond speed in this device is measured and presented. Finally the device is tested under high temperature and it shows that the performance is poor and improvements are necessary in order to be applied as a rugged electronics component.

Chapter 4 proposed a new design of a logic switch using same Si material as contact body. The design relies on a curve structure that is almost impossible

to breakdown once turns on, hence mitigating secondary pull-in failure. More importantly, this switch is encapsulated in wafer level vacuum encapsulation, referred as the Epi-seal process. The stiffness of such structure is first determined by an analytical model in order to obtain the pull-in voltage approximation. After that the robustness of the curved beam structure is simulated with Coventorware finite element method (FEM). The stopper design of the curved beam switch is also explained with proper illustration. The logic switch is part of a tape-out of a multi project wafer (MPW) service initiated by Stanford University. The process flow as well as the critical steps of the Epi-seal process is presented. The fabrication results are finally presented.

Chapter 5 covers the testing and characterization of the vacuum encapsulated curved beam switch. Other than standard characterization, the switch's operation under acceleration is performed to verify the switch's mechanical resistance to shock. More rugged measurement is performed including testing from -60 °C to 400 °C is reported. I-V characteristics, contact resistance, curved beam structure robustness against secondary pull-in, switching speed are measured. With the vacuum encapsulation, high reliability of at least  $10^7$  and  $10^6$  on-off cycles are successfully demonstrated under room temperature and high temperature of 400 °C respectively. Lastly

the operation reliability of the curved beam switch under high acceleration is reported.

In Chapter 6, the failure analysis of a Si-to-Si contact is performed using the data from the curved beam switch. First the cross-sectional failure of the Si-to-Si switch is presented. From the failure, it is deduced that the temperature at contact interface is an important factor to the contact reliability. The temperature at contact is investigated thoroughly by understanding the Joule heating phenomenon during on-off operation. This is done by performing more testing with drain-source signal and creating heat at the contact interface. A model is presented to predict the temperature at contact. With all this, the lifetime of the curved beam switch in high temperature is improved.

Finally, conclusions on the current work and recommendations for future work are presented in Chapter 7.

# **CHAPTER 2: DESIGN AND FABRICATION OF A SILICON NANOFIN NON-VOLATILE MEMORY BASED ON VAN DER WAALS FORCE**

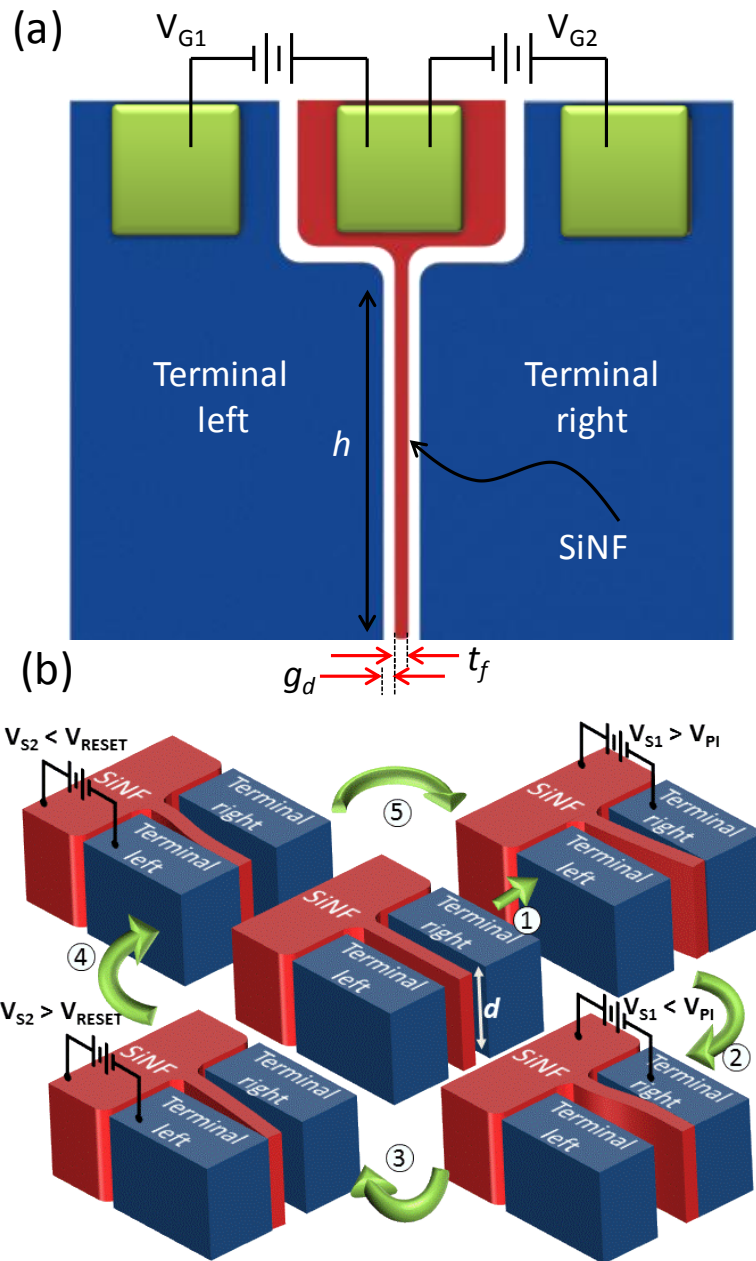
## **2.1 Introduction**

In harsh environment, conventional Flash memory degrades rapidly due to increased activity of hot carrier injection and standby leakage current. Reported maximum memory retention temperature of Flash is estimated to be approximately 250 °C [180]. In this chapter, a high aspect ratio silicon nanofin (SiNF) based nanoelectromechanical (NEMS) switch has been simulated and fabricated as a potential alternative to solid-state non-volatile memory (NVM) for application such as storage in harsh environments. To demonstrate bi-stability, deliberate stiction is designed into device by manipulating surface forces and spring restoration forces. This is done by implementing novel mechanical memory latching mechanism leveraging on van der Waals force. The result is a device that is able to demonstrate non-volatile memory (NVM) hysteresis behaviour [181]. Meanwhile, high density non-volatile memory is made possible with the nano-scale dimension of the SiNF. Meanwhile, silicon material is chosen to fabricate the device due to its high melting temperature and ability to survive harsh environment.



## 2.2 Operational NEMS switch with bi-stable states

A sketch of the bi-stable three-terminal switch is shown in Figure 2.1(a). This switch comprised of a cantilever beam with thickness  $t_f$  and length  $h$ , flanked by two gate terminals on either side, separated by gaps of  $g_d$  respectively. The cantilever beam is a high aspect ratio (1:35) silicon based nanofin (SiNF), fabricated using entirely CMOS process. The design of experiment (DOE) dimension of the SiNF consists of 2, 8 and 12  $\mu\text{m}$  length ( $h$ ) with 80 nm thick ( $t_f$ ) and 3.5  $\mu\text{m}$  height ( $d$ ). The gap ( $g_d$ ) between the SiNF to either terminal is approximately 80 nm. The SiNF is designed to switch between two side lateral terminals by electrostatic force, controlled by two different gate voltages,  $V_{G1}$  and  $V_{G2}$ . This reported switch is lateral based since the actuation is in-plane movement. The step-by-step operation is better illustrated by Figure 2.1(b). Initially, the SiNF is in a neutral state. To actuate the SiNF to the right terminal, a sweeping voltage ( $V_{S1}$ ) is applied between the two. Pull-in of the SiNF happens when the sweeping voltage reaches a certain threshold voltage, this voltage is referred as the pull-in voltage ( $V_{PI}$ ). Subsequently, when this voltage is removed, van der Waals force at the interface between SiNF and terminal will maintain the contact without on-hold bias, resulting in hysteresis behaviour. Meanwhile, the SiNF flips and switches towards the opposite lateral terminal when a second sweeping voltage ( $V_{S2}$ ) is applied across the left terminal.



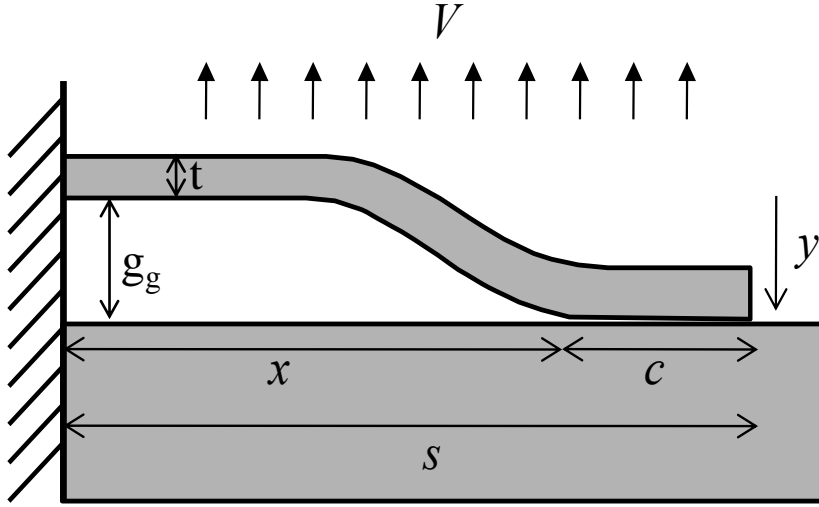
**Figure 2.1:** (a) Top view schematic of the NEMS memory with SiNF as the actuator that can switch between two terminals (b) Structure and operation of a bi-stable NEMS switch. (1) SiNF is pulled-in to the right terminal by  $V_{S1}$ . (2) VDW force holds the SiNF in contact position even after the electrostatic force is removed (3) As bias is applied opposite, SiNF flips towards the other terminal. (4) VDW force holds the switch in left terminal. (5) The switch cycles between two terminals, resulting in bi-stable state device.

The SiNF structure makes NEMS switch bi-directionally while exhibiting non-volatile hysteresis, thus it is able to provide two different states. Both stable states available attributed to van der Waals force that enables the NEMS switch to serve as storage-layer-free NVM.

## **2.3 Critical length and van der Waals force**

### **2.3.1 Governing equations for beam's critical length**

The van der Waals based stiction cannot be over designed or else the device won't be able to reset. In order to resolve the critical length ( $L_c$ ) at the quasi-stable state, the presented model follows a methodology presented by Mastrangelo and Hsu [182, 183]. The profile of an actuated cantilever beam is shown in Figure 2.2, with the beam sticking to the drain electrode at distance  $c$ , the contact length. The adhesion area is modelled as a region held flat against the drain electrode. The contact length is determined by the balance of beam elastic energy, van der Waals adhesion energy and electrostatic energy, with the total energy of the system being minimized at equilibrium. Unit width of the cantilever beam is assumed throughout the analysis. Assuming the electrostatic force is being applied from the opposite side via a voltage  $V$  across  $0 \leq x \leq s$ , the beam deflection  $y$  in this region is given by the Euler-Bernoulli beam equation (2.1).



**Figure 2.2: Side view of cantilever structure stick to bottom substrate with dimensional parameters.**

$$EI \frac{d^4 y}{dx^4} = -\frac{\epsilon_0 V^2}{2(y + g_g)^2} \quad (2.1)$$

Where the moment of inertia  $I$  per unit width is given by equation (2.2)

$$I = \frac{t^3}{12} \quad (2.2)$$

The boundary conditions are

$$y(0) = \left. \frac{dy}{dx} \right|_0 = 0, \quad y(s) = g_d, \quad \left. \frac{dy}{dx} \right|_s = \theta = \frac{mg_d}{s} \quad (2.3)$$

Where  $\theta$  is the shear angle of the tip, and  $m$  is a non-dimensional number. The last boundary condition is necessary to account for beam tip shear, which is

significant as  $c$  becomes small. An exact solution for  $y$  is not easily expressed analytically, thus a series solution is used. An expansion to the fourth order gives the equation (2.4)

$$y = \left( \frac{(3-m)g_d}{s^2} - \frac{s^2 \varepsilon_0 V^2}{48EIg_g^2} \right) x^2 + \left( \frac{(m-2)g_d}{s^3} + \frac{s \varepsilon_0 V^2}{24EIg_g^2} \right) x^3 - \frac{\varepsilon_0 V^2 x^4}{48EIg_g^2} \quad (2.4)$$

Given

$$\theta = \frac{M_o t}{Ec^3} \left( \frac{42}{5} + 3 \left( \frac{c}{t} \right)^2 \frac{E}{G} \right) \quad (2.5)$$

Where shear modulus  $G = E/2(1 + \nu)$ ,  $\nu$  is Poisson's ratio, and rearranging gives

$$M_o = -EI \left. \frac{d^2 y}{dx^2} \right|_s = \frac{2EIg_d}{s^2} (3 - 2m) + \frac{s^2 \varepsilon_0 V^2}{24g_g^2} \quad (2.6)$$

Solving  $m$ , gives

$$m = \frac{(5cE + 14t^2)(144EIg_d g_g^2 + s^4 \varepsilon_0 V^2)}{8Eg_d g_g^2 (60EIc^2 + 5Gc^3 st + 168GIt^2)} \quad (2.7)$$

Thus the elastic energy stored in the beam is given by

$$\begin{aligned}
 U_E &= \frac{EI}{2} \int_0^s \left( \frac{d^2y}{dx^2} \right)^2 dx \\
 &= \frac{2EIg_d^2}{s^3} (3 - 3m + m^2) + \frac{s^5 \epsilon_0^2 V^4}{5760EIg_g^4}
 \end{aligned} \tag{2.8}$$

While the van der Waals adhesion energy is given by equation (2.9).

$$U_{vdw} = \frac{Hc}{12\pi r^2} \tag{2.9}$$

Where  $Hc$  is the Hamaker's constant for the material used. Here,  $H_{Si} = 5 \times 10^{-20}$  J is used,  $r$  is the separation between the two surfaces.

Meanwhile, the electrostatic energy can be expressed as

$$U_{es} = -\frac{\epsilon_0 V^2}{2} \int_{\epsilon_1}^{\epsilon_2} \frac{1}{(y + g_g)} dx \tag{2.10}$$

A simple analytical solution to the integral is not easily found. As an approximation, the integrand is first expressed as a series expansion up to fourth order. This gives

$$\begin{aligned}
U_{es} = & -\frac{\varepsilon_0 V^2}{2} \int_{\epsilon_1}^{\epsilon_2} \left[ \frac{1}{g_g} + \left( \frac{(m-3)g}{s^2 g_g^2} + \frac{s^2 \varepsilon_0 V^2}{48EIg_g^4} \right) x^2 \right. \\
& + \left. \left( \frac{(2-m)g}{s^3 g_g^2} + \frac{s\varepsilon_0 V^2}{24EIg_g^4} \right) x^3 + \frac{x^4}{(48EIg_g^2)^2} \right. \\
& \left. \times \left( 48EI\varepsilon_0 V^2 + \frac{(48EIgdg_g^2(m-3) + s^4 \varepsilon_0 V^2)^2}{s^4 g_g^3} \right) \right] dx
\end{aligned} \tag{2.11}$$

Where the integral limits  $\epsilon_1$  and  $\epsilon_2$  represents each ends of the beam. By evaluating the integral, setting  $\epsilon_1 = 0$ ,

$$\begin{aligned}
U_{es} = & -\frac{\varepsilon_0 V^2}{2} \left[ \frac{\epsilon_2}{g_g} + \frac{\epsilon_2^3}{3} \left( \frac{(m-3)g}{s^2 g_g^2} + \frac{s^2 \varepsilon_0 V^2}{48EIg_g^4} \right) \right. \\
& + \frac{\epsilon_2^4}{4} \left( \frac{(2-m)g}{s^3 g_g^2} + \frac{s\varepsilon_0 V^2}{24EIg_g^4} \right) + \frac{\epsilon_2^5}{5(48EIg_g^2)^2} \\
& \left. \times \left( 48EI\varepsilon_0 V^2 + \frac{(48EIgdg_g^2(m-3) + s^4 \varepsilon_0 V^2)^2}{s^4 g_g^3} \right) \right]
\end{aligned} \tag{2.12}$$

The total energy  $U_T$  is

$$U_T = U_E + U_{es} - U_{vdw} \tag{2.13}$$

And the equilibrium is found by setting its derivative to zero. Pull-out occurs as  $c$  approaches 0, thus  $V_{PO}$  is found by solving

$$\left. \frac{dU_T}{dc} \right|_{c=0} = \left. \frac{dU_E}{dc} \right|_{c=0} + \left. \frac{dU_{es}}{dc} \right|_{c=0} - \left. \frac{dU_{vdw}}{dc} \right|_{c=0} = 0 \tag{2.14}$$

Lastly, solving the boundary condition and rearranging the equation yields the critical length,  $L_c$  equation (2.15) below.

$$L_c = \left( \frac{9\pi Et^3 g_d^2 r^2}{2H} \right)^{1/4} \quad (2.15)$$

An expression for the critical length of the cantilever beam as well as a closed-form solution for the pull-out voltage can be obtained through a series expansion of fourth order. This closed-form solution enables rapid analysis of wide ranges of design parameters, reducing the reliance on finite element simulations which can be time consuming. If cantilever length exceeds the critical length  $L_c$ , adhesive surface forces that is dominated by van der Waals interactions, can overcome the elastic restoring force and allow the cantilever to retain switch contact after pull-in even after the actuation voltage is removed, thus functioning as non-volatile memory (NVM). In contrast, if the cantilever length is shorter, the restoring force will dominate and the beam will break the contact and operates like a logic switch. In higher temperature, temperature affected parameter has to be taken into account. The parameter affected by the elevated temperature can be the stiffness of the beam, and the Hamaker's constant dependency on temperature. The beam stiffness dependency is affected by the Young's Modulus thermal coefficient of Si,  $\beta = -67 \times 10^{-6} \text{ K}^{-1}$  [197]. Since this value is negative, the adhesion force is expected to increase,



resulting in larger surface force between the contacts. The latter parameter, Hamaker's constant at elevated temperature can be estimated by the following equation.

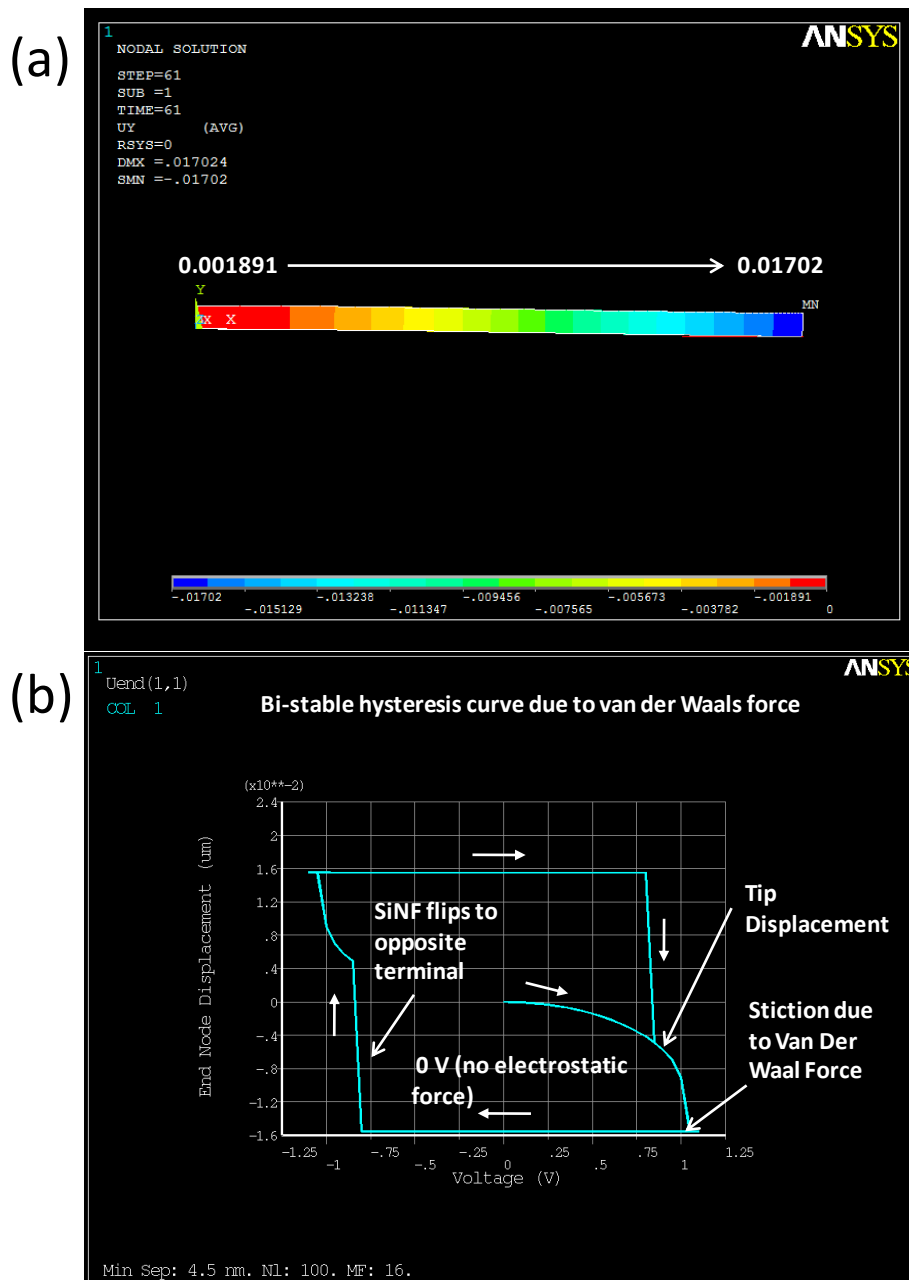
$$H_{\theta} = H_C \left( \frac{T_{\theta}}{T_0} \right) \quad (2.16)$$

Where  $H_C$  is the Hamaker's constant at room temperature,  $T_{\theta}$  is the intermediate temperature and  $T_0$  is the room temperature. By looking at the temperature dependency for both parameters, it can be conclude that the adhesion force is larger at higher temperature. The design is realized in the next part by fabrication of a non-volatile memory using silicon nanofin (SiNF). The device is fabricated and characterized to show bi-stable states non-volatility properties. Its critical length is estimated with equation derivation in the next section and it shows that surface forces can be leveraged to realize bi-stable non-volatile mechanical device.

### **2.3.2 Finite element simulations and boundary conditions**

Finite-element analysis (FEA) simulations are carried out using ANSYS. Figure 2.3(a) shows the simulation result and the schematics of the model used in the simulation. Structural element PLANE183, contact element TARGE169 and CONTA171 is used to simulate the dimension parameters to design a bi-stable state switch based on van der Waals force ( $F_{VDW}$ ). The

ANSYS code is detailed in Appendix 1. A parallel-plate capacitive model is used to simulate the electrostatic force between the SiNF and the terminals in accordance to their respective gaps. A voltage sweep (V) is applied at one side of the terminal. The electrostatic force ( $F_{ELEC}$ ) gradually rises as the sweeping voltage increases. At displacement of approximately 1/3 of the gap distance, the cantilever is pulled in to contact the gate. Then  $F_{VDW}$  is input as a load to hold the SiNF, while the voltage sweeps back to zero. If the spring restoration force is larger than the van der Waals adhesion,  $F_{SPRING} > F_{VDW}$ , the SiNF will bounce back to the original position, else the SiNF will remain in contact. The simulation result is shown in Figure 2.3(b).



**Figure 2.3: (a) FEM simulation model of a SiNF in ANSYS with displacement (in  $\mu\text{MKS}$ ) denoted. (b) The result of simulation for a successful non-volatile hysteresis curve due to van der Waals force. As the voltage sweep from starting from 0 V, tip displacement of the SiNF is simulated. Pull-in is detected after that and the stiction due to van der Waals force is considered as a load that holds the SiNF tip in closed contact position. The contact remains closed as voltage sweep returns to zero. The same phenomenon repeats on the other side of the switch terminal, forming a non-volatile hysteresis curve.**

### 2.3.3 Design of experiment (DOE) parameter

Table 2.1 shows the parameter decided for SiNF after both simulation and numerical solution are performed. The pull-in results are compared to the analytical model and it is found that the discrepancy is about 12% which is considered a good approximation; this is shown in the next chapter. A notable assumption is that the simulated  $V_{PI}$  is consistent, which is considered ideal compared to real measurement.

**Table 2.1 SiNF parameters in design of experiment (DOE)**

Parameters	Value (nm)	Pull-in voltage
Beam Length, $h$	2000, 8000, 12000	10, 0.4, 0.2 V
Beam thickness, $t_f$	80, 90, 100, 110	
Gap size, $g_d$	~ 80	

## 2.4 Design approach

### 2.4.1 Layout view

Nikon 203B KRF 6" reticle with  $25 \times 33$  mm design area is available for the SiNF non-volatile memory design of experiment. Figure 2.4(a) shows the top view of the entire layout. Detail of one device is shown in Figure 2.4(b) and the zoom-in of the SiNF layout is shown in Figure 2.5.

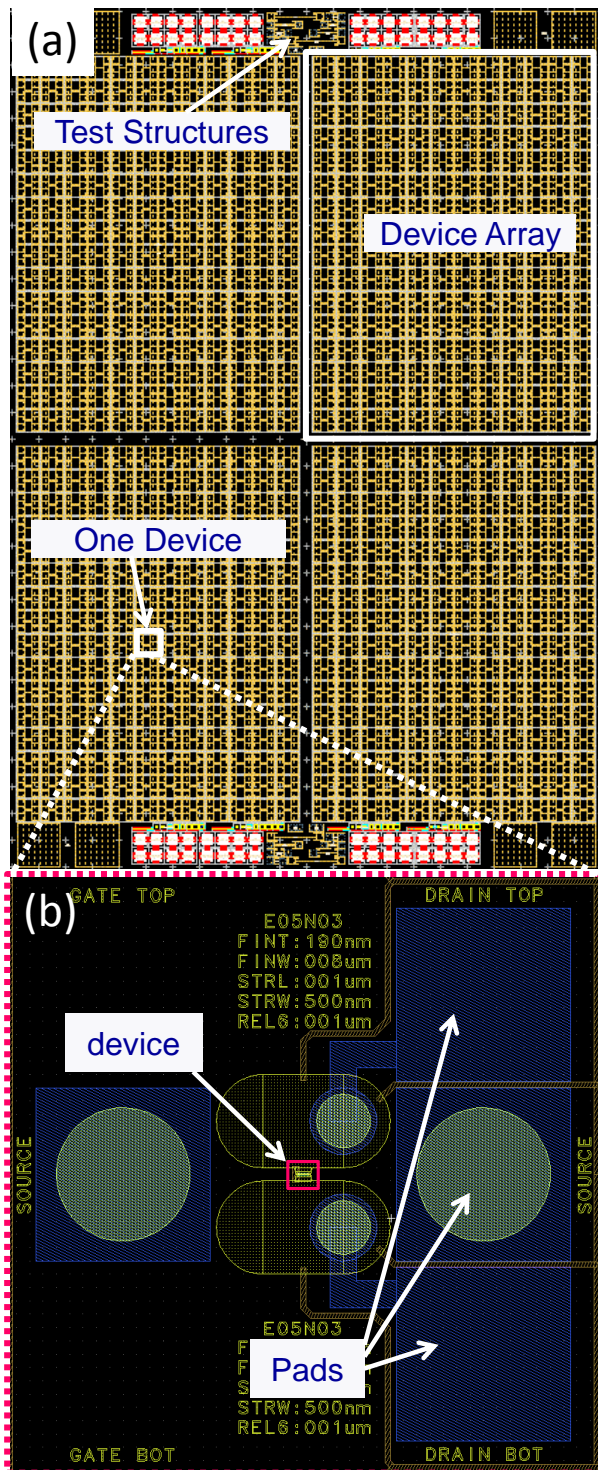


Figure 2.4: (a) Reticle (25 × 35 mm) top layout. (b) Single device cell layout with top metallization pads.

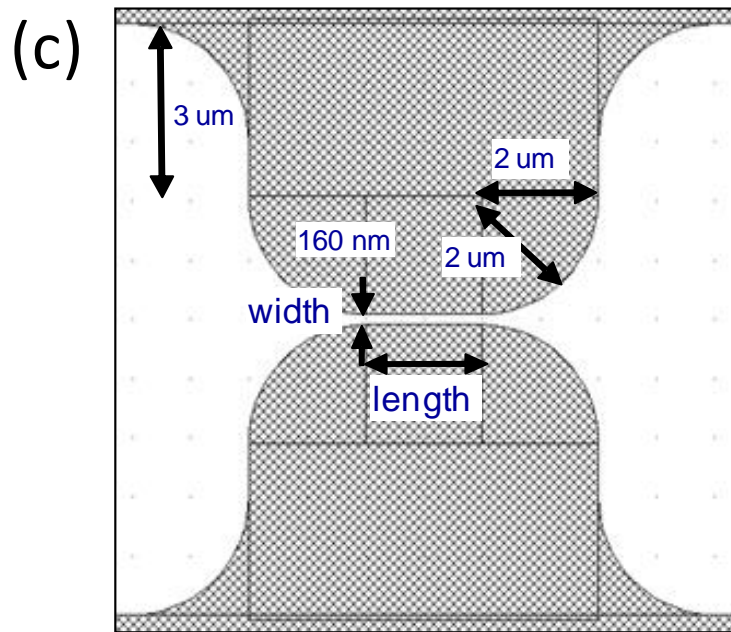


Figure 2.5: Zoom-in view of the SiNF with specific dimensions.

## 2.5 Fabrication process

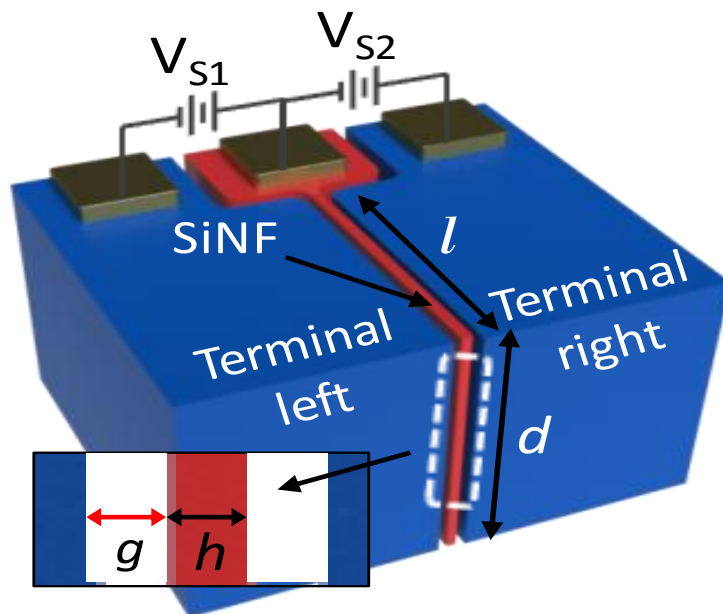


Figure 2.6: A 3D schematic of the NEMS memory with SiNF as the actuator that switches between the terminals. The entire structure is made from Si except the metallization using Al.

Defining nano-electromechanical system (NEMS) device remains a huge challenge in this device. Figure 2.6 shows the 3D schematics of the SiNF non-volatile memory. The nano-size SiNF aspect ratio is approximately 1:35 and the gap between the SiNF and the adjacent terminal is approximately 80~100 nm. From the schematics, it is also seen that metallization pads are fabricated on the Si. The SiNF beam is intact during the fabrication and released in the last step using a dry isotropic etching. The detailed fabrication and optimization will be discussed later in this section.

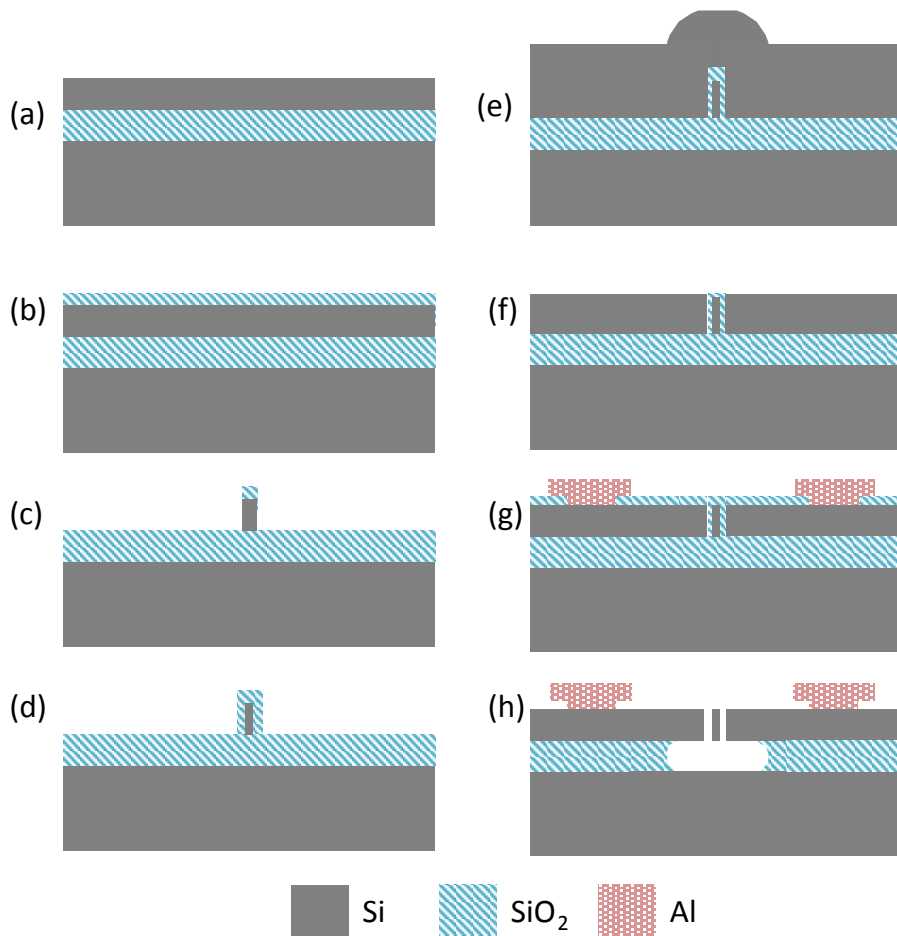
### **2.5.1 Detailed fabrication and critical steps**

In the Si-to-Si NEMS memory, process recipes are repeatedly optimized to provide a high aspect ratio and smooth surface to the main structure: The SiNF beam. Structurally Si has good reliability and implantation can be performed to reduce the resistivity of the material. Other than that, nano-size electromechanical device can be realized without much intrinsic stress when it is made out of single crystal Si, which is the standard case of for SOI wafer platform. However, the conductance of Si is still incomparable to metal no matter how much impurity density can be implemented. Figure 2.7 shows the fabrication process flow. a.) Starting from SOI wafer. b.) a layer of SiO<sub>2</sub> is thermally grown as a hard mask for the first layer etching. c.) hard mask is etched followed by silicon deep reactive ion etching (DRIE). d.) Further

oxidation is performed to reduce the overall fin dimension to nano-scale size < 100 nm. e.) Poly Si is overfilled as the gate electrode to the SiNF. f.) The wafer is planarized so that the fin is exposed. g.) An insulation layer of SiO<sub>2</sub> is deposited followed by opening to the gate and Al is deposited as contact. h.) Finally the device is release in dry hydrofluoric acid vapour to remove the SiO<sub>2</sub>, leaving the SiNF suspended. Heavy implantation and activation is performed at step a. and step e. in order to make the silicon as conductive as possible to reduce the resistance of the Si. More details on the fabrication process will be given below.

Fabrication of nano-scale device is challenging and the process is carried out at Institute of Microelectronics, Agency of Science and Technology Singapore (A\*STAR) where 248 nm deep UV lithography tool is available. Multiple steps of CMOS compatible processes are leveraged to create a Si-to-Si two-terminal NVM. First, eight inch SOI wafer with 3.5 μm N-type device layer and 1 μm BOX is used. A high dosage phosphorous implantation of  $5 \times 10^{16}$  ion/cm<sup>2</sup> at 80keV is performed to make the device layer more conductive. Next, 300nm of thin SiO<sub>2</sub> is thermally grown at 1050°C in O<sub>2</sub> ambient to create hard mask for the first etching step. The above completes the substrate preparation to start the first lithography.



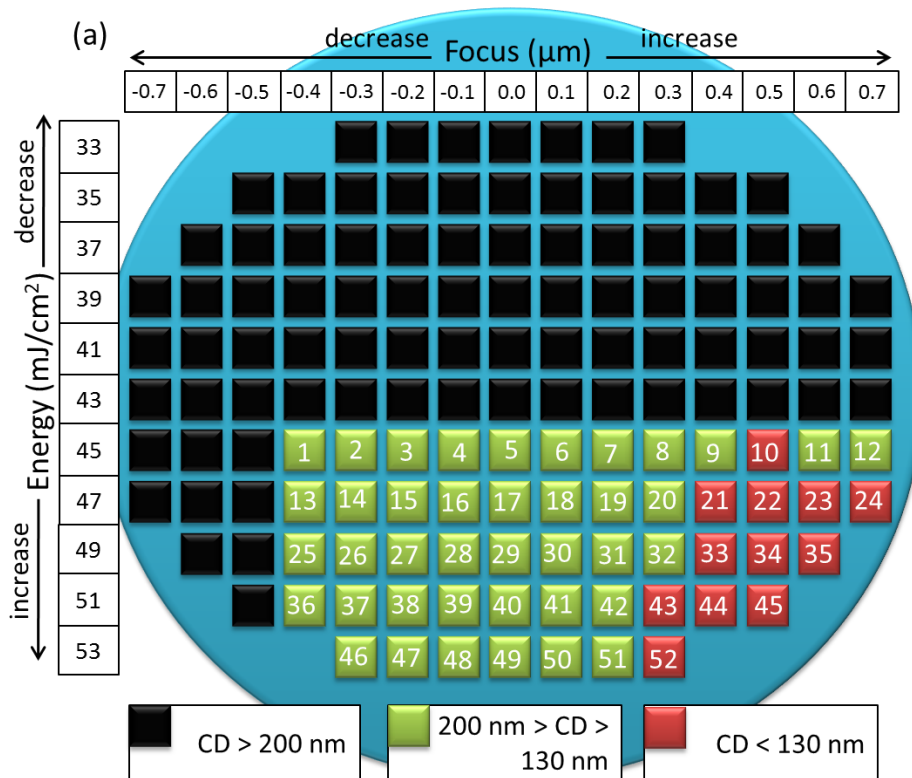


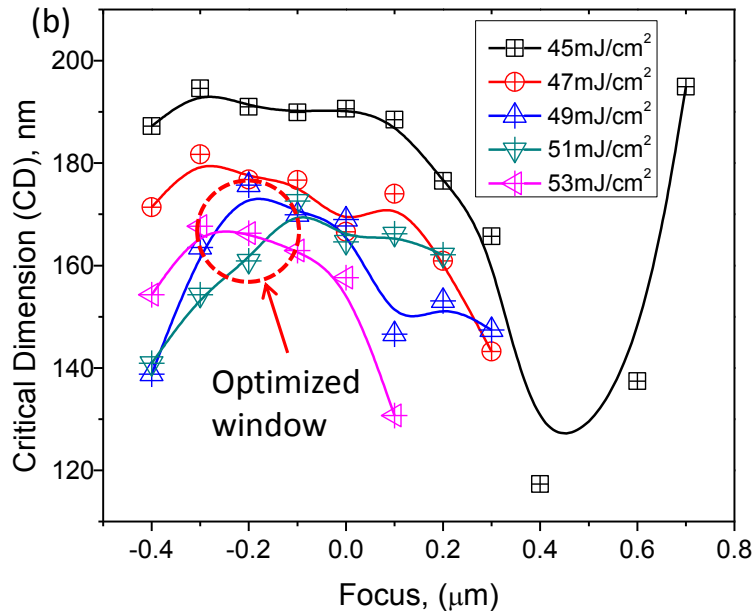
**Figure 2.7: CMOS front end of the line (FEOL) process flow for SiNF switch. . a.) SOI wafer – 3.5  $\mu\text{m}$  device layer, 1 $\mu\text{m}$  BOX. b.) 3.5  $\mu\text{m}$  Si DRIE. c.) Dry oxidation. d.) 5  $\mu\text{m}$  poly-Si deposition and planarization till flat. e.) Al metallization. f.) Device release in VHF.**

### 2.5.1.1 Ultra high aspect ratio silicon nanofin definition

In the first layer, patterning of SiNF is performed with Nikon KRF 248nm excimer laser scanner. The wafer is first coated with 60nm of bottom antireflective coating (BARC) and 320 nm of deep UV photoresist (Microchem UV210). A Bossung plot analysis is done to obtain the optimal exposure condition after performing focus exposure matrix (FEM). This is shown in Figure 2.8. Figure 2.8(a) represents wafer exposure map with both

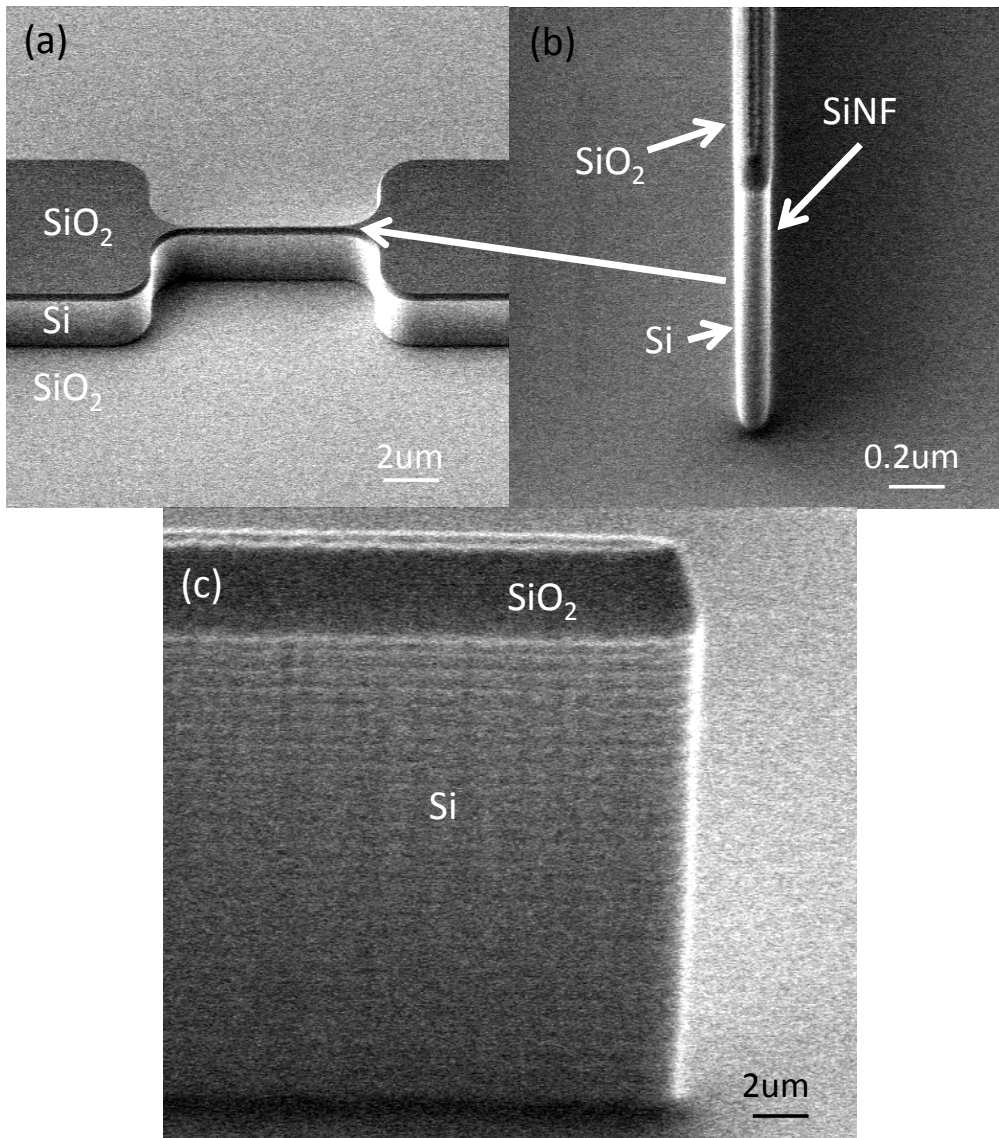
x-axis and y-axis representing exposure parameter (exposure energy in  $\text{mJ}/\text{cm}^2$ ) and lens focus correction (focusing distance calibration in  $\mu\text{m}$ ). The area of interest is defined by the critical dimension measurement. This area is defined by the critical dimension of the SiNF from  $200 \text{ nm} > \text{CD} > 130 \text{ nm}$ . The  $\text{CD} > 200 \text{ nm}$  and  $< 130 \text{ nm}$  is not accounted in this optimization. By plotting measured CD from device labelled from 1 to 52 versus focus and energy level, which is also known as a Bossung plot as shown in Figure 2.8(b), the optimized window can be determined. The energy range ( $49\text{-}53\text{mJ}/\text{cm}^2$ ) and focus  $-0.2 \mu\text{m}$  is the optimized parameter for the scanner exposure condition.





**Figure 2.8: (a) Wafer exposure map and measurement location of the available die area. (b) FEM result of SiNF exposure optimization. Bossung's plot shows optimized window of target SiNF's CD.**

A final exposure condition of energy = 52 mJ/cm<sup>2</sup>, focus = -0.2  $\mu\text{m}$  is chosen for the definition of the SiNF. This condition has shown the critical dimension (CD) nearest to target. After that, the hard mask is etched in optimized C<sub>4</sub>F<sub>8</sub> + Ar based recipe using high density plasma etcher. The PR is then stripped and the wafer proceed to deep reactive ion etching to produce a SiNF with minimum CD of 160 nm  $\times$  3.5  $\mu\text{m}$  height. This etch is done with BOSCH high aspect ratio deep reactive ion etching (DRIE), this recipe is optimized with extremely short 5 seconds passivation cycle of 25 sccm C<sub>4</sub>F<sub>8</sub>, alternating earlier with a longer 30 seconds etching cycle of 40 sccm SF<sub>6</sub> + 90 sccm C<sub>4</sub>F<sub>8</sub>, chamber pressure remain constant throughout the etch at 45 mTorr, the coil power of etching and passivation is 800 and 600W respectively.

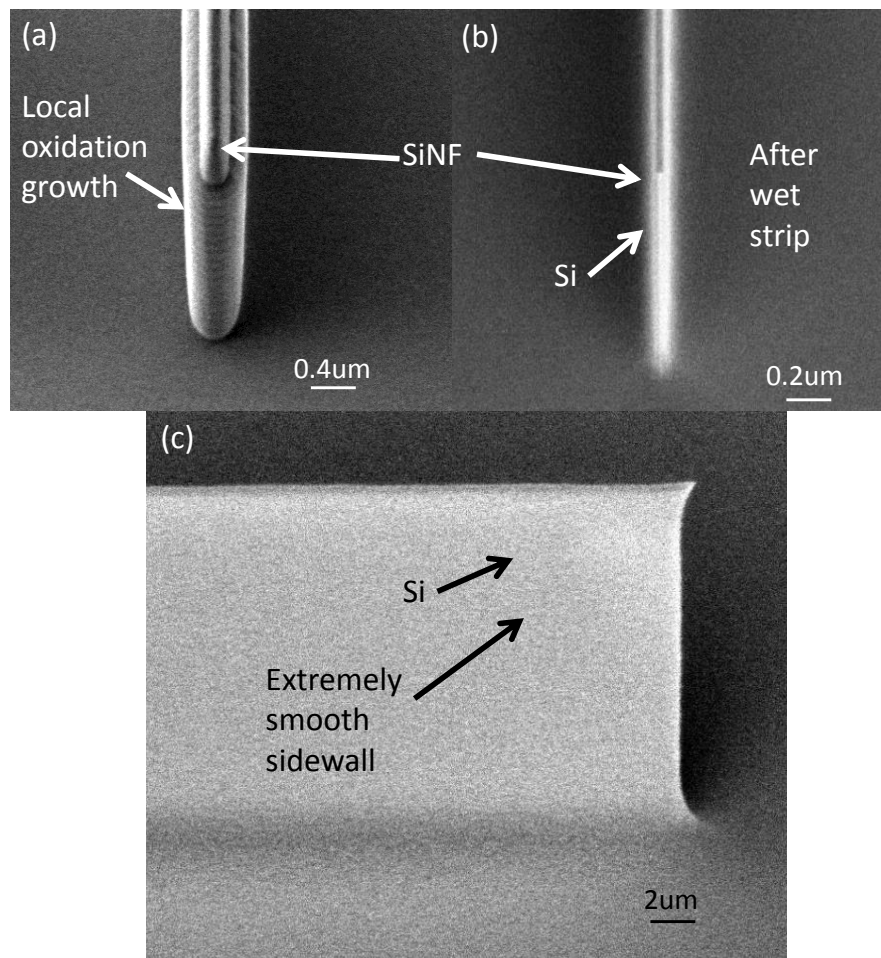


**Figure 2.9: (a) Overall SiNF definition with DRIE. (b) Zoom-in of one SiNF with open end with very straight sidewall. (c) Sideview of SiNF shows etched surface profile.**

The etching results in a slight scalloping sidewall and this is crucial because reducing sidewall roughness will enhance the van der Waals adhesion force.

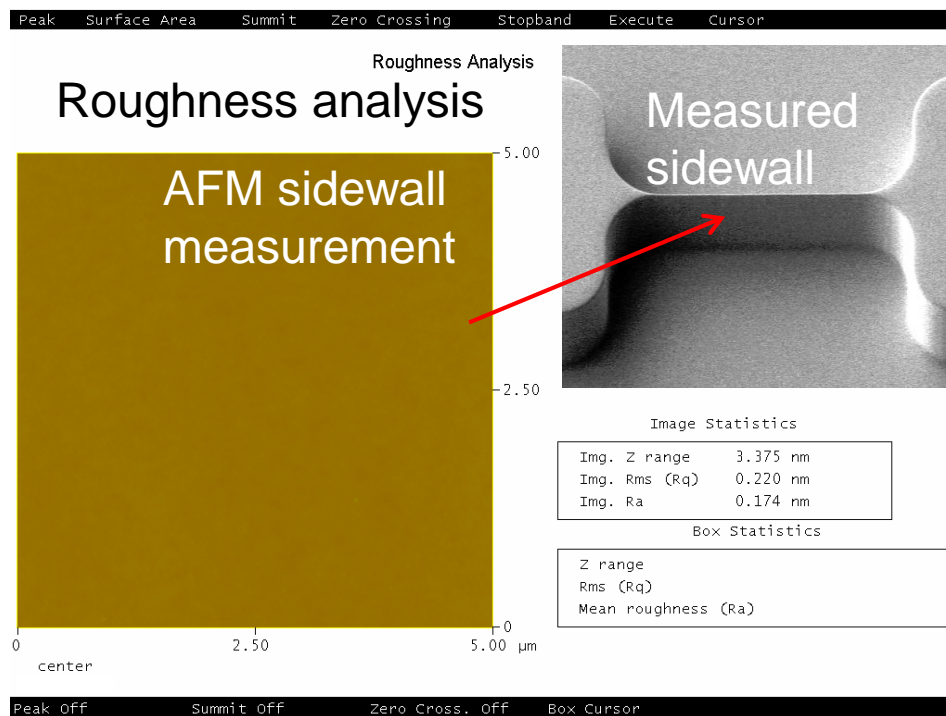
The final etching result is shown in Figure 2.9(a) – (c). The aspect ratio of the SiNF at this stage is approximately 1:15. Further process is performed to increase the aspect ratio and reduce the surface roughness after DRIE. To

reduce surface roughness of the sidewall, wet local oxidation (LOCOS) at 1050 °C is performed in SEMCO tube furnace. The pressure of the oxidation in the furnace is 1 atm. The process gas flow is 1 slm DI water vapour with a 0.5 slm of oxygen. In this process, fin width is further reduced as the Si is being consumed during oxidation. The final SiNF width reduces from minimum CD of 160 nm to 80 nm, achieving aspect ratio of approximately 1:35, the final dimensions of the SiNF width ranges from 80-110nm.



**Figure 2.10: (a) Local oxidation (wet) of SiNF to reduce surface roughness and overall SiNF width. (b) SiNF width of 80 nm after removing surface oxide. (c) Side view of SiNF shows extremely smooth sidewall.**

The smoothening effect and the SiNF thinning are shown in the SEM diagram in Figure 2.10(a) – (c). An AFM sidewall measurement reveals that the surface roughness is similar to the bulk silicon wafer surface. From the result shown in Figure 2.11, the overall thickness is reduced and at the same time the surface roughness is measured to be  $< 0.22 \text{ nm}_{\text{RMS}}$ . The thickness reduction can be measured accurately by ellipsometry measurement.

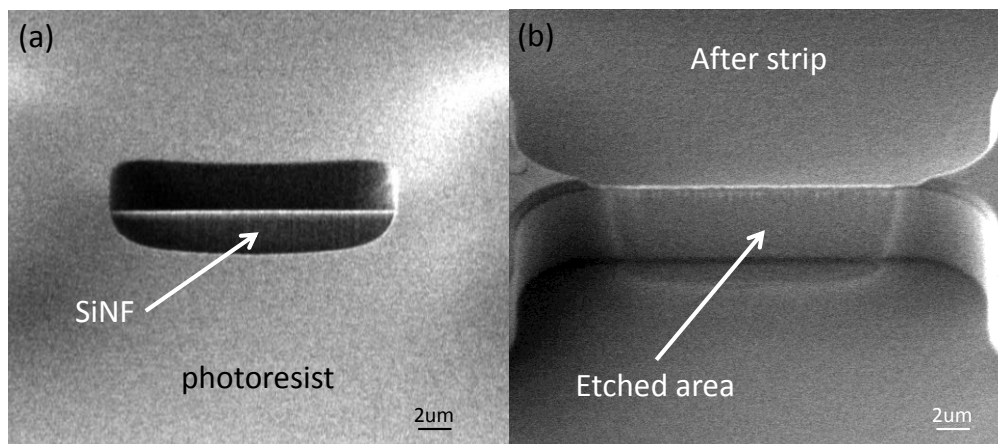


**Figure 2.11: AFM result of sidewall of SiNF**

### 2.5.1.2 Gap definition

The thermally grown  $\text{SiO}_2$  can be conveniently defined as the sacrificial layer and the insulation layer. The area near the actuation gap has to be etched partially by creating a smaller gap for the electrostatic actuation. In order to do

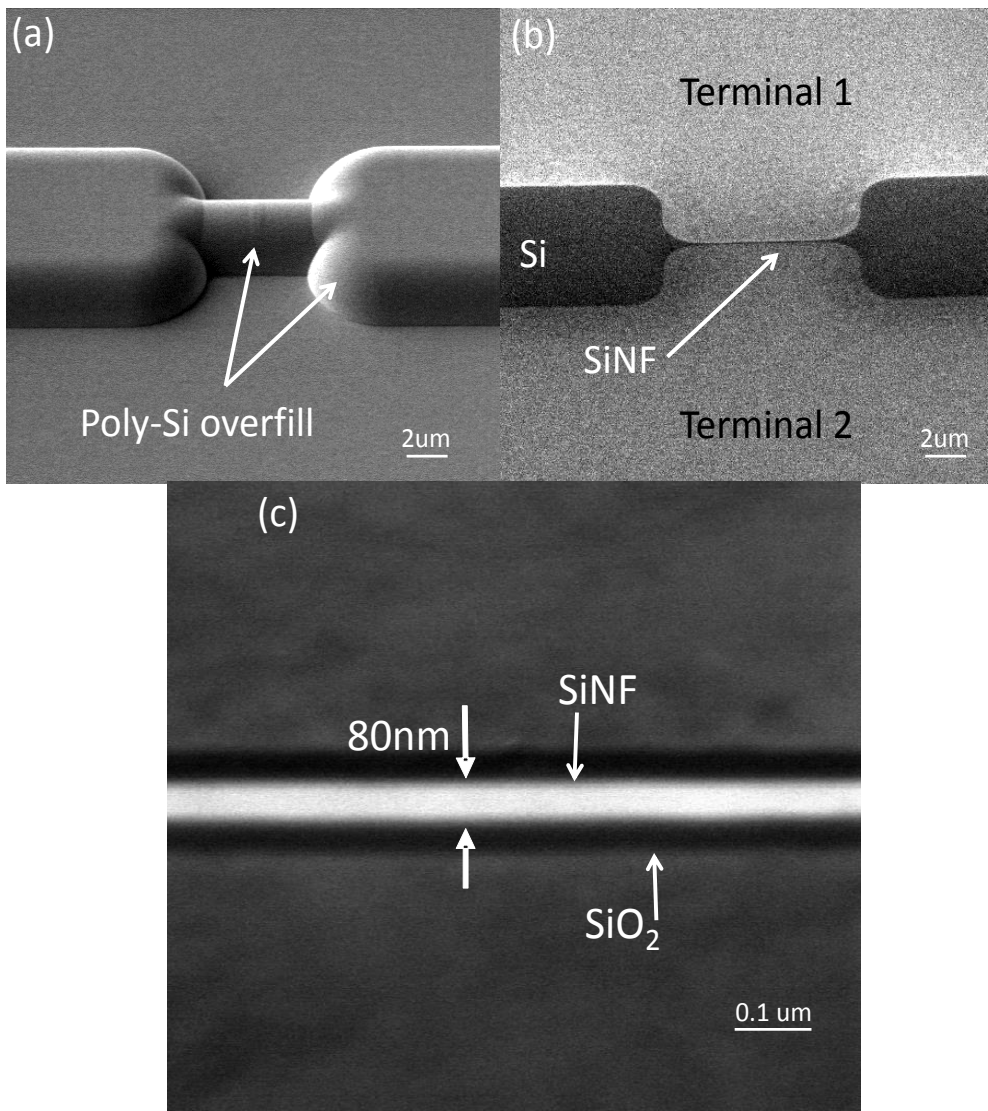
this, first the thickness of the SiO<sub>2</sub> is measured with ellipsometer, since the gap target is approximately 80 nm, any excess SiO<sub>2</sub> has to be etched away. This is done by time etch using diluted hydrofluoric (HF) acid of (1:25), which etch rate is about 35 nm/min, using photoresist as a mask. The photoresist coating has to be thicker to protect most of the area except the opening of the effective actuation area near the SiNF. This is shown in Figure 2.12(a). Careful timing and repeated rounds of etching and measurement are performed to ensure the gap achieve the target of 80 nm of SiO<sub>2</sub>. The result after etching and stripping the photoresist is shown in Figure 2.12(b).



**Figure 2.12: (a) Photoresist opening of the SiNF area for gap definition. (b) SiO<sub>2</sub> sacrificial reduction etches using HF acids around the SiNF actuation area to create 80nm gap.**

### 2.5.1.3 Side terminal definition

Now that the SiNF is completed, the side terminal next to it is defined. A 4  $\mu\text{m}$  low pressure chemical vapour deposition (LPCVD) thick poly-silicon is deposited on the overall wafer, this process naturally over fills the entire SiNF.



**Figure 2.13: (a) Thick poly silicon deposition overfilling all trenches and forming side terminal of the SiNF. (b) After CMP, SiNF is exposed and the terminals are self-aligned to side. (c) Zoom-in of the SiNF.**

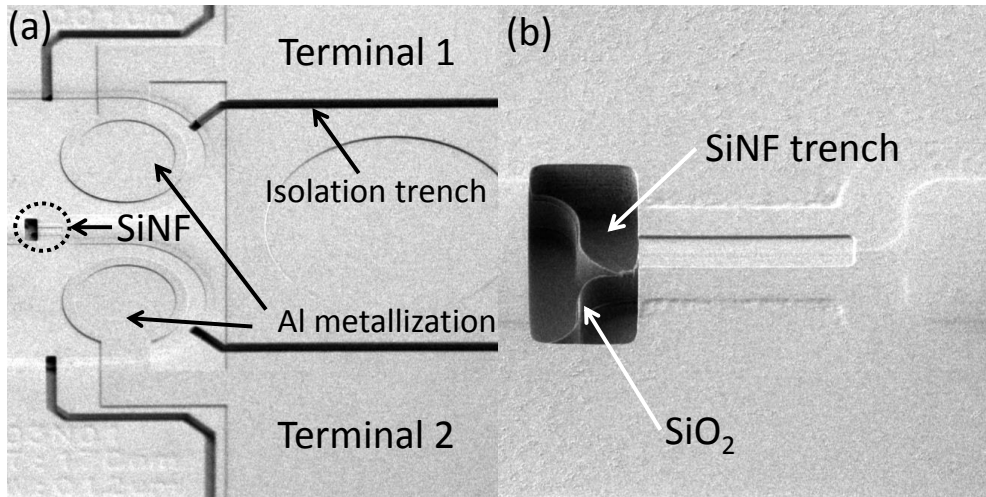
The side terminals are entirely self-aligned with the SiNF since the poly-silicon is uniformly deposited on the whole wafer. The deposition is shown in Figure 2.13(a). After that, poly-Si CMP is performed to planarize the entire wafer, until the SiNF emerges from overfilled poly-Si. This is shown in Figure 2.13(b). The zoom-in detail of the SiNF is shown in Figure 2.13(c).



The poly-Si back filled is heavily implanted twice with  $5 \times 10^{15}$  ions/cm<sup>2</sup> Arsenic dopant and activated with high temperature of 1050 °C for 12 hours. At this stage the SiNF can be released to inspect the partial completeness of the device.

#### **2.5.1.4 Isolation and metallization**

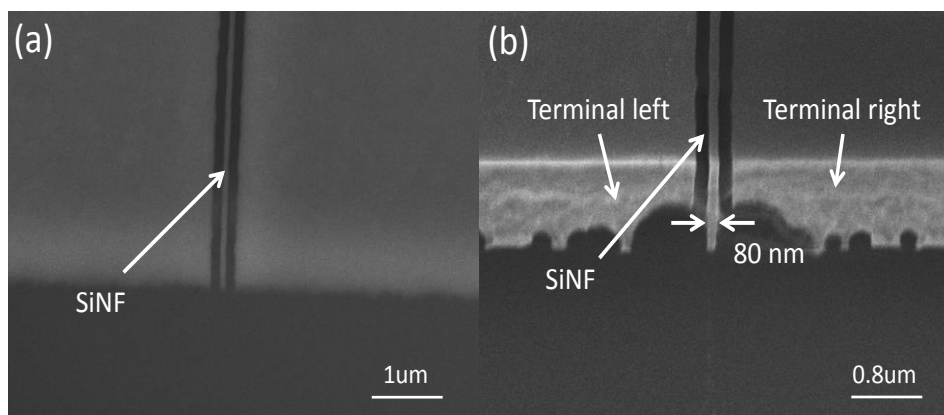
To re-distribute the electrodes, an insulating 300 nm LPCVD SiO<sub>2</sub> is deposited and etch back on release area, this layer also serves as the insulation to the metallization path. Vias are etched into this dielectric layer in order for the metallization to contact the silicon terminals. After that, 500 nm aluminium (Al) is sputtered and patterned to provide contact to the SiNF and poly-Si gate. The Al interconnects are designed in larger dimension so that it is able to survive the isotropic etching during the release. To further prevent the possibility of leakage current, isolation trench is patterned and etched stop on buffered oxide layer (BOX) to isolate the SiNF and the terminal electrodes. This is shown in Figure 2.14(a). At the same time, this etch defines the SiNF trench, where one edge of the SiNF is etched and the SiNF becomes a cantilever. This is shown in Figure 2.14 (b). Due to the selectivity, some SiO<sub>2</sub> sidewall remains but this will be etched during the last release process.



**Figure 2.14: (a) Isolation trench stop on buried oxide layer (BOX) to isolate the SiNF and the gate-electrodes. (b) SiNF is etched to become a cantilever, SiO<sub>2</sub> sidewall remains due to higher selectivity.**

### 2.5.1.5 Device release

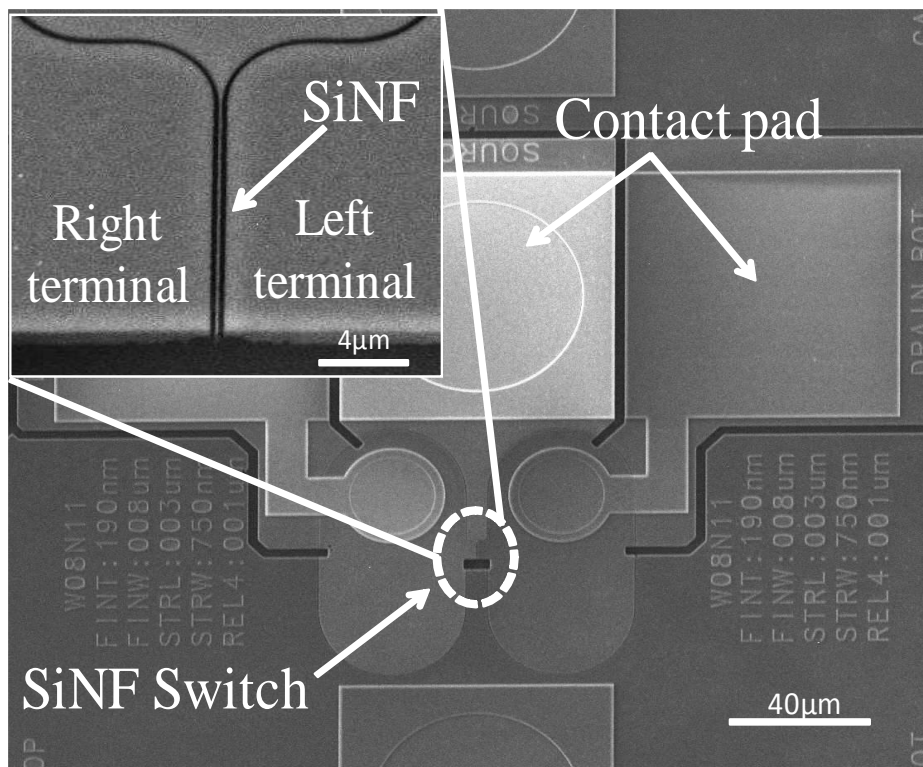
Lastly the device is released in hydrofluoric acid vapour (VHF). The top view of the release SiNF is shown in Figure 2.15(a) and the tilted view is shown in Figure 2.15(b). Since the SiNF is fabricated from the device layer, the SiNF is stress free. Furthermore, dry release is capable of providing a non-stiction suspended structure, resulting SiNF initially in neutral position before testing.



**Figure 2.15 (a) Top view of the released SiNF. (b) Tilted view of the SiNF with 80 nm width.**

## 2.6 Fabrication outcome

Figure 2.16 shows the SEM image of a 12  $\mu\text{m}$  SiNF device where contact pads are Al metalized. A zoom-in image of the SiNF shows that the SiNF is extremely straight and does not suffer from any bending due to stress and all SiNF are at neutral position. The SiNF is now movable and can be controlled by applying a potential between both terminal and the SiNF. The testing and characterization will be discussed in more detail in next chapter.



**Figure 2.16: SEM of a switch device of 8  $\mu\text{m}$  length  $\times$  90nm thick SiNF. (Inset) Zoom in view of the SiNF in the centre of the device.**

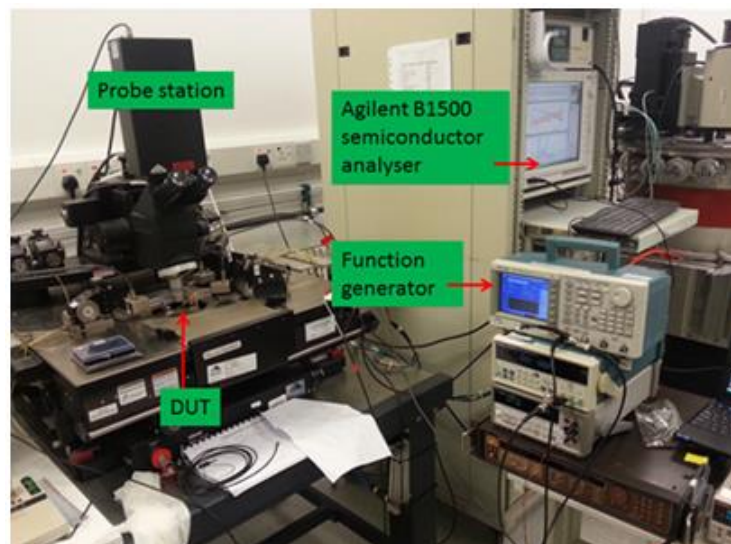
## 2.7 Conclusion

In conclusion, this chapter introduced a new bi-stable SiNF non-volatile memory concept leveraging on stiction dominated by van der Waals force. A critical length model is presented to determine whether a cantilever is a non-volatile memory or a logic switch. Meanwhile, FEM simulation using ANSYS is performed to validate the design. Both critical length model and FEM simulation converges into design of the silicon based nanofin (SiNF) switch that operates like a non-volatile memory. The parameters generated are converted into layout and the device is fabricated. The two main categories of MEMS processing techniques, i.e., bulk micromachining and surface micromachining, as well as the three main building blocks of MEMS processing, i.e., deposition, lithography, and etching, were also presented in this chapter. In-depth MEMS fabrication techniques used in the fabrication of the devices in the current work are introduced and explained. This includes the optimization of small CD lithography, high aspect ratio formation, interconnect isolation and release strategy. Lastly, the detailed microfabrication process outcome that realizes the structures and devices in the current work is presented. The device characterization will be presented in next chapter.

# CHAPTER 3: CHARACTERIZATION OF TWO TERMINAL SILICON NANOFIN NON-VOLATILE MEMORY

## 3.1 Testing setup and procedure

The fabricated device is tested and characterized in Cascade micro chamber (RBL-6100) with temperature controlled stage. Measurement is set up and performed using B1500 semiconductor analyser. The analyser is equipped with two source monitoring units (SMU) and one high resolution source monitoring unit (HRSMU). Meanwhile, Tektronix function generator (AFG 3102) and oscilloscopes (DPO7354C) are used to measure the switching speed. The overall set-up is shown in Figure 3.1.



**Figure 3.1: Testing set-up of the SiNF electrical characterization. Probe station with microchamber (Cascade RBL-6100) equipped with semiconductor analyser (Agilent B1500) and function generator (Tektronix AFG 3102)**

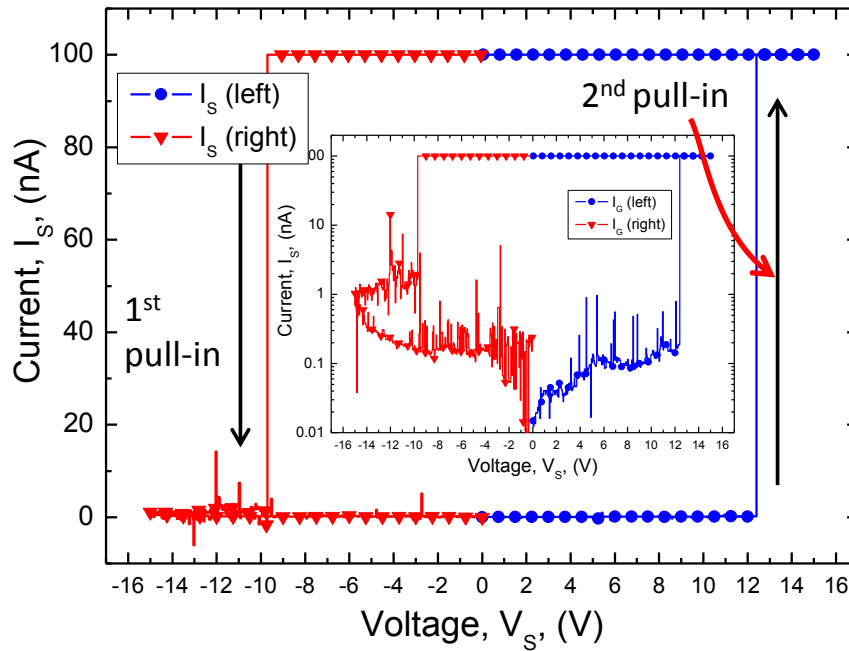
### 3.2 Electrical characterization

First, the pull-in voltage ( $V_{PI}$ ) is measured and statistical results are systematically analysed and compared with FEM results. In first test, a voltage sweep ( $V_s$ ) is applied across left terminal and right terminal from negative region (0 to -15V) to positive region (0 to 15V) to detect the pull-in voltage. Figure 2.6 in the previous section illustrates the measurement configuration. The test is performed inside a  $N_2$  purged micro chamber at elevated temperature of 50°C to remove any moisture. Hence capillary force is negligible. After that, to determine the van der Waals force operation, the non-volatile hysteresis of the SiNF is measured and verified together with SEM inspection. The result is further analysed to determine the working region of the SiNF more precisely: logic or memory. Then, the switching speed of the SiNF switch is measured and compared with a standard resonance frequency model. The SiNF switch is subjected to higher temperature and the drift from 50 °C to 150 °C is measured. Finally, the reliability and the failure mechanism of the switch are presented.

### 3.3 Result and discussion

#### 3.3.1 I-V characteristics of a two-terminal electrostatic SiNF non-volatile memory

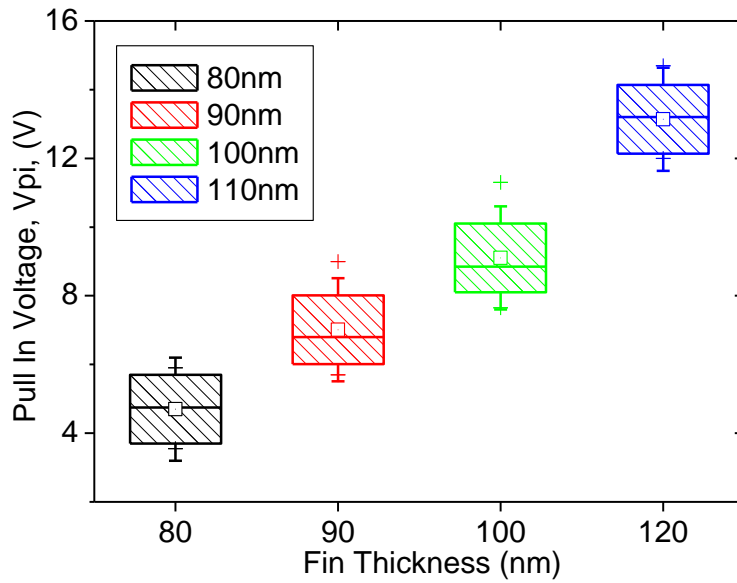
Using the testing setup described in section 3.1, first the I-V characteristics of the SiNF switch is measured. The result is shown in Figure 3.2. A sweeping voltage  $V_S$  is applied across the SiNF and the left terminal. An abrupt increase in current,  $I_S$ , of  $10^3$  order is observed showing that the SiNF is switched and in contact with the right terminal. This pull-in happens initially at  $V_S = -10$  V. This is also known as the pull in voltage,  $V_{PI}$ . When  $V_S$  gradually rise on the left terminal, the 2<sup>nd</sup> pull-in happens. Altogether this completes one loop of pull-in voltage measurement. When  $V_S$  is gradually decrease to zero, it is noted that the current does not fall back to zero, except at  $V_S = 0$  V, (omitted in Figure 3.2), depicting that the SiNF is still remain in contact with the terminal. It is important to emphasize that the abrupt switching is a mechanical effect. Thus the sub-threshold swing of the SiNF switch or any kind of switch is always ideally infinite. In actual experiment, the switching is always detected within two smallest voltage resolution set during the measurement. The measurement can be easily confused with some “charging like on-off” curves, which are just measurement of a shorted dielectric or capacitor.



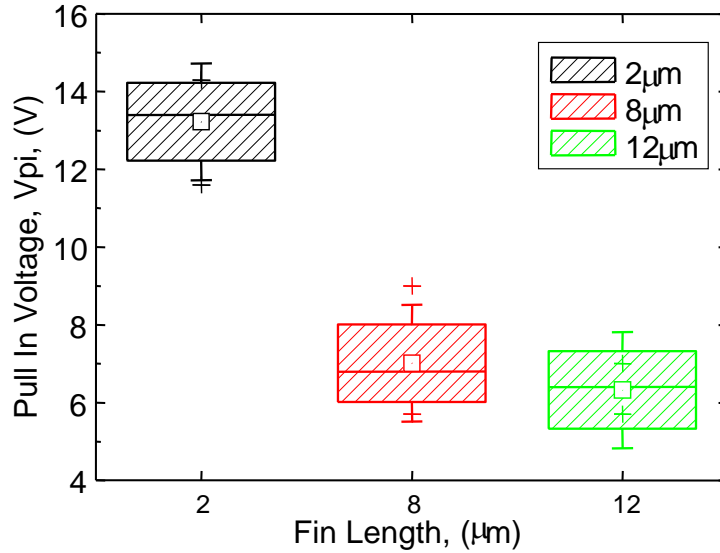
**Figure 3.2: Measured hysteresis curve of a 2  $\mu\text{m}$  long fin showing two pull-in voltage (-10 V and 12 V) of a SiNF device. (Inset) log scale curve. 0V point omitted for illustration purpose. The on/off ratio of the SiNF is approximately 2~3 orders of magnitude.**

Figure 3.3 and Figure 3.4 show the correlation between the pull-in voltage versus the length and thickness of the SiNF. The measurement is performed statistically for twenty devices and results show that longer length and smaller thickness reduces the pull-in voltage while keeping non-volatile hysteresis behaviour for 2  $\mu\text{m}$  and 8  $\mu\text{m}$  SiNF. The measurement results agree well with a standard pull-in model of an electrostatic based cantilever as shown in section 1.3.1. As the SiNF switch's pull-in voltage is proportional to  $w^{3/2}$  and inversely proportional to  $l^2$  of the beam's dimension.



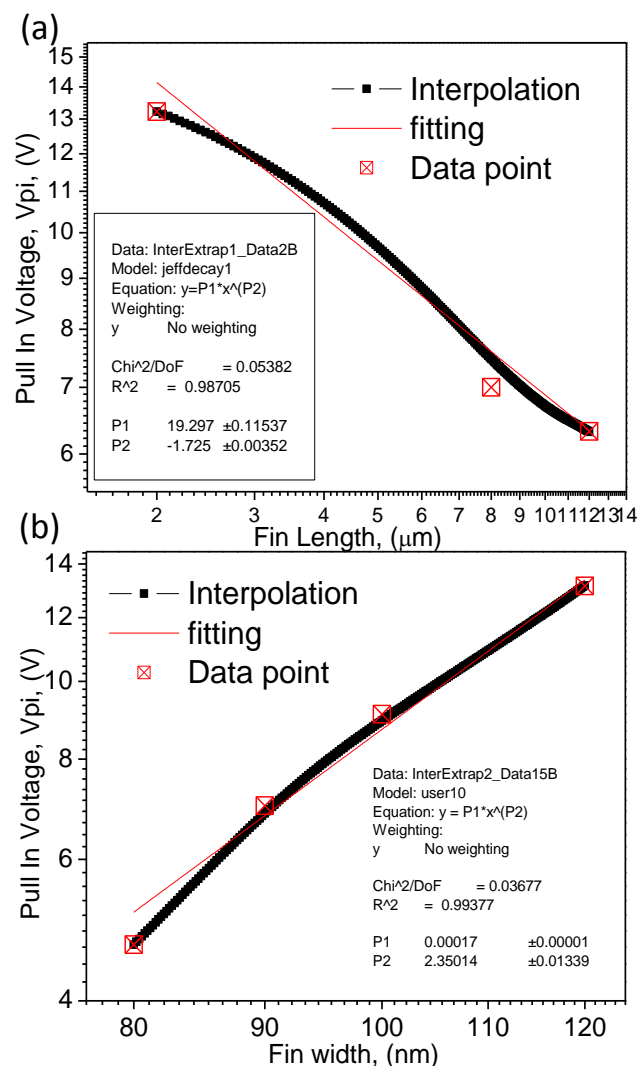


**Figure 3.3: Pull-in voltage,  $V_{PI}$  versus different thickness of switch of 80 – 120 nm (measured). Constant error bar for twenty switching devices and median of each thickness are measured. Pull-in voltage,  $V_{PI}$  increases with the thickness of SiNF.**



**Figure 3.4: Pull-in voltage,  $V_{PI}$  versus different switching length of 2 $\mu\text{m}$ , 8 $\mu\text{m}$  and 12 $\mu\text{m}$ . Constant error bar for twenty switching devices and median of each length are measured. Pull-in voltage,  $V_{PI}$  reduces with the length of SiNF.**

By plotting the experimental  $V_{PI}$  versus  $w$  and  $l$  on a log-log plot as shown in Figure 3.5(a) and (b), the fitting corresponds to  $l$  yield power exponents of -1.725 and the fitting corresponds to  $w$  yield 2.35 can be found. The fitted power coefficient is agreeable to the theoretical value. However, the power exponent corresponds to  $w$  seems to be higher. This may be due to fabrication or design error in the critical dimension of the SiNF.



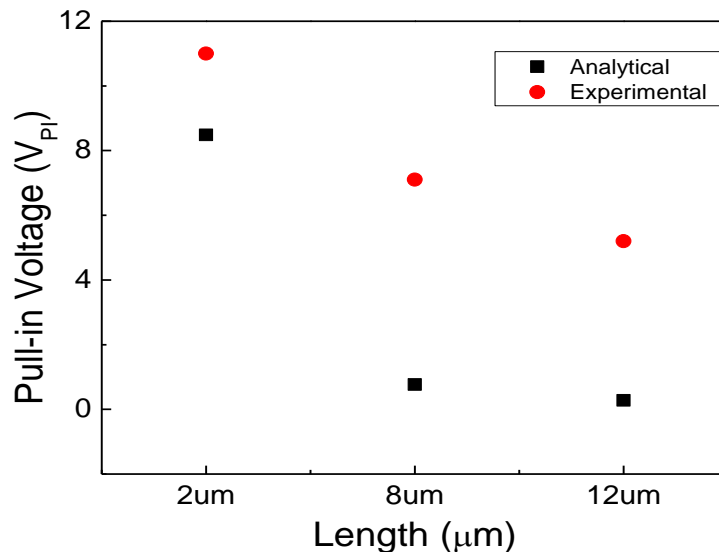
**Figure 3.5: (a) Pull-in voltage line fitting with respect to SiNF length on a log-log scale. (b) Pull-in voltage line fitting with respect to SiNF width on a log-log scale.**

A comparison is done between the analytical and experimental value of the pull-in voltage as shown in Figure 3.6. Overall the pull-in voltage reduces inversely proportional to the length of the SiNF, which shows a good trend in  $V_{PI}$ . However, the experimental value is generally higher than the expected value, possibly due to fabrication tolerance especially in the release process and non-uniform electrostatic force exerted in such tiny beam. The analytical model used in predicting the pull-in voltage of the beam is too ideal. For short beam, the effective modulus equals to the Young's Modulus,  $E$ . However, the SiNF is a long beam, where  $l > 5t$ . The effective modulus becomes the plate modulus as shown below.

$$E_{plate} = \frac{E}{1 - \nu^2} \quad (3.1)$$

where  $E$  is the Young's Modulus,  $\nu$  is the Poisson ratio of Si = 0.17.

The abrupt jump in sweeping current corresponds to on-off current ratio ( $I_{on}/I_{off}$ ) of  $10^3$  which is considered far from ideal due to the compliance current setting of 100 nA. If an excessive current flows through SiNF, this may cause significant localized heating and result in fusing and oxidation of the Si switch. Thus, the device suffers from poor yield and reliability. This may improve if the testing is done under vacuum encapsulation which is viable at packaging level and may prove valuable to such devices.



**Figure 3.6: Comparison of pull-in voltage for analytical model and experimental value. Mean value is taken from experimental value. Overall the experimental value is higher than then analytical value, where the analytical model is a standard parallel capacitor model.**

Other alternative solution like contact enhance coating like Au, Pt and  $\text{RuO}_2$  may solve this issue but the fabrication of such small device will be extremely challenging [28, 171]. The on-off current ratio of  $10^5$  is demonstrated with 100  $\mu\text{A}$  current compliance as shown in Figure 3.7 with the similar device, but the device works for only once. This is shown from when the sweeping current gradually reduce when sweeping voltage is decreasing, resembling current discharging curve, which may be caused by SiNF melted to the respective actuating terminal. The pull-in voltage is 5.95V at 25mV/decade, achieving five order of on-off ratio. From the experimental results, it is shown that the length is crucial in designing a resettable switch.

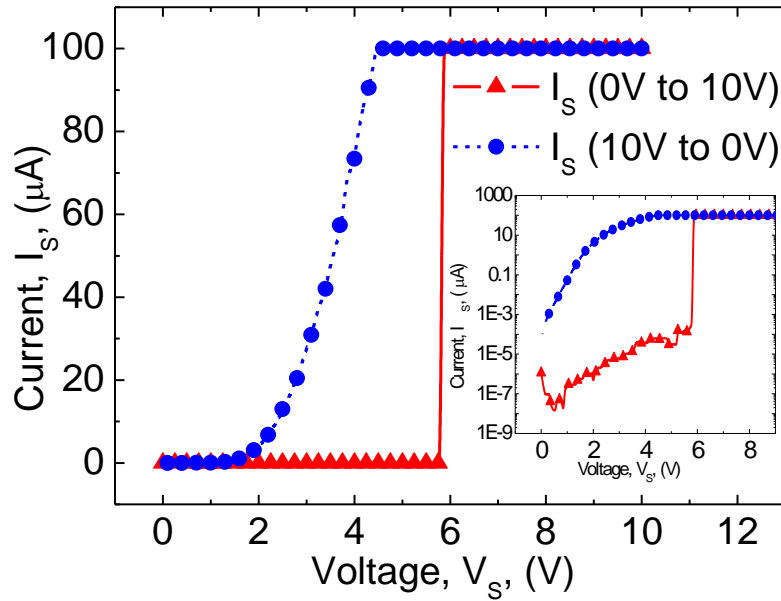


Figure 3.7: Measured  $I_S - V_S$  curve of an 8  $\mu\text{m}$  length SiNF device. The current compliance of the measurement is limited up to 100  $\mu\text{A}$ . From 0V to 10V, measured  $V_{PI}$  is 5.95 V at 25m V/decade. The measured  $I_{ON}/I_{OFF}$  is  $10^5$ . From 10 V to 0 V, the pull out is not abrupt but shows charging relation.

### 3.3.2 Non-volatile hysteresis operation

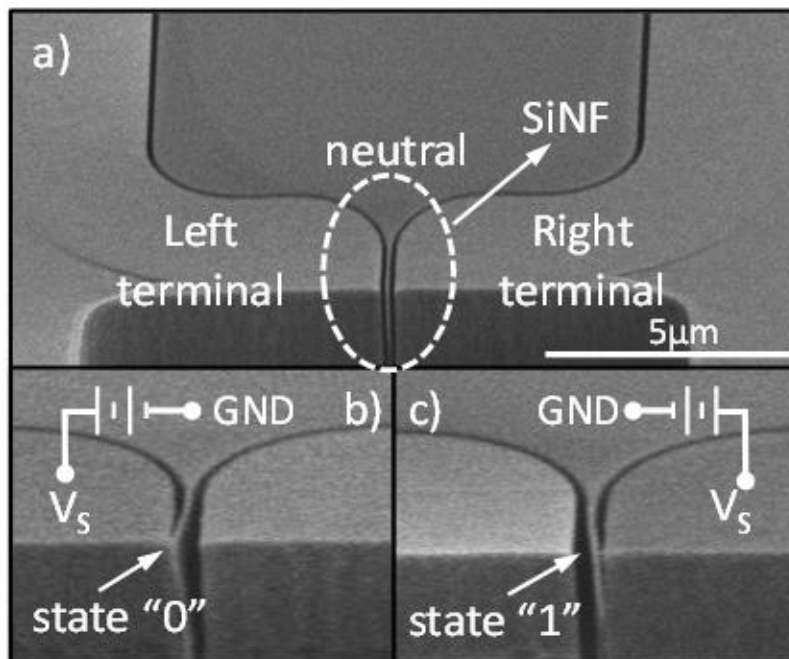
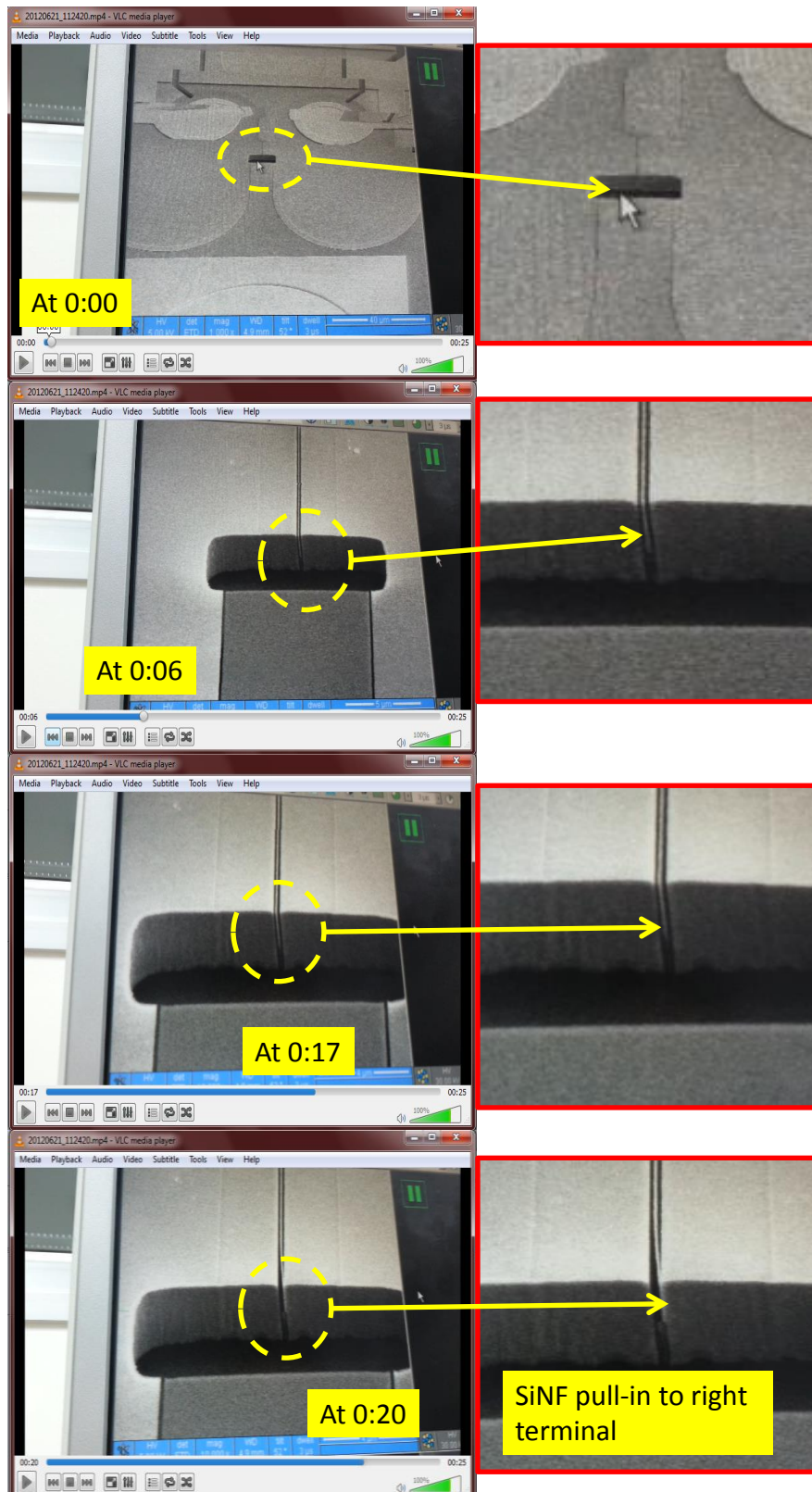


Figure 3.8: SEM diagram showing a 2  $\mu\text{m}$  length  $\times$  80 nm width SiNF in operation. (a) SiNF remains at neutral position. (b) SiNF contact remains on hold to the left terminal, depicting state "0". (c) SiNF flips to the right terminal and on hold to the right terminal, depicting state "1".

Figure 3.8(a) shows the SEM of a  $2\ \mu\text{m} \times 80\ \text{nm}$  NEMS switch in neutral state. As the total electrostatic attraction force is proportionate to  $V_S$ , electrostatic pull-in of the SiNF to the either terminal happens when this voltage approaches pull-in voltage ( $V_{PI}$ ), i.e.  $V_S = V_{PI}$ . To show this, with the SiNF grounded, a voltage sweep ( $V_S$ ) is applied across left terminal and right terminal from negative region (typically 0 to -15V) to positive region (0 to 15V). Figure 3.8 (b) shows the SEM of SiNF actuated by contacting the left terminal. A live video of the SiNF actuation is shown in Figure 3.9. After switching is performed in SEM, the device is removed from the SEM inspection tool and the bias is removed. After that, the switched memory state is tested with a small voltage  $V_S$  and the direction agree well result under SEM. This shows that the presence of connection still exist between the SiNF and the left terminal, even without holding bias. Van der Waals force between the SiNF and the left terminal in this case was able to overcome the spring restoration force and thus the SiNF was latched in the final switch position even though there is no on-hold bias voltage. After that,  $V_S$  is applied across SiNF and the opposite terminal. When the voltage gradually increases, the SiNF flips and switches towards the right terminal when the electrostatic force is larger than the spring restoration force and the van der Waals adhesion. This happens at  $V_S = -12\text{V}$ . Similarly, Figure 3.8 (c) shows the SEM of the same device with reversed  $V_S$  applied across source and right terminal. Electrostatic

force is negligible when the switch is turned off, thus the major remaining force that holds the contact is the van der Waals attraction. Despite actuation arises from the electrostatic force in the electron beam scanning in SEM microscope, the results are reliable due to multiple device tested are verified. During the SEM inspection of the 2  $\mu\text{m}$  SiNF, it is observed that the SiNF is barely bent and only the tip, which is approximately 5% of the SiNF body, is in contact with the terminal electrode, which means the gap between the body of the SiNF and the opposite terminal is relatively unchanged. This indicates that in 2  $\mu\text{m}$  SiNF, the initial pull-in voltage should be identical to the voltage that is used to flip the SiNF to the opposite terminal, also known as the second pull-in. This is shown in the next measurement in Figure 3.10(a).

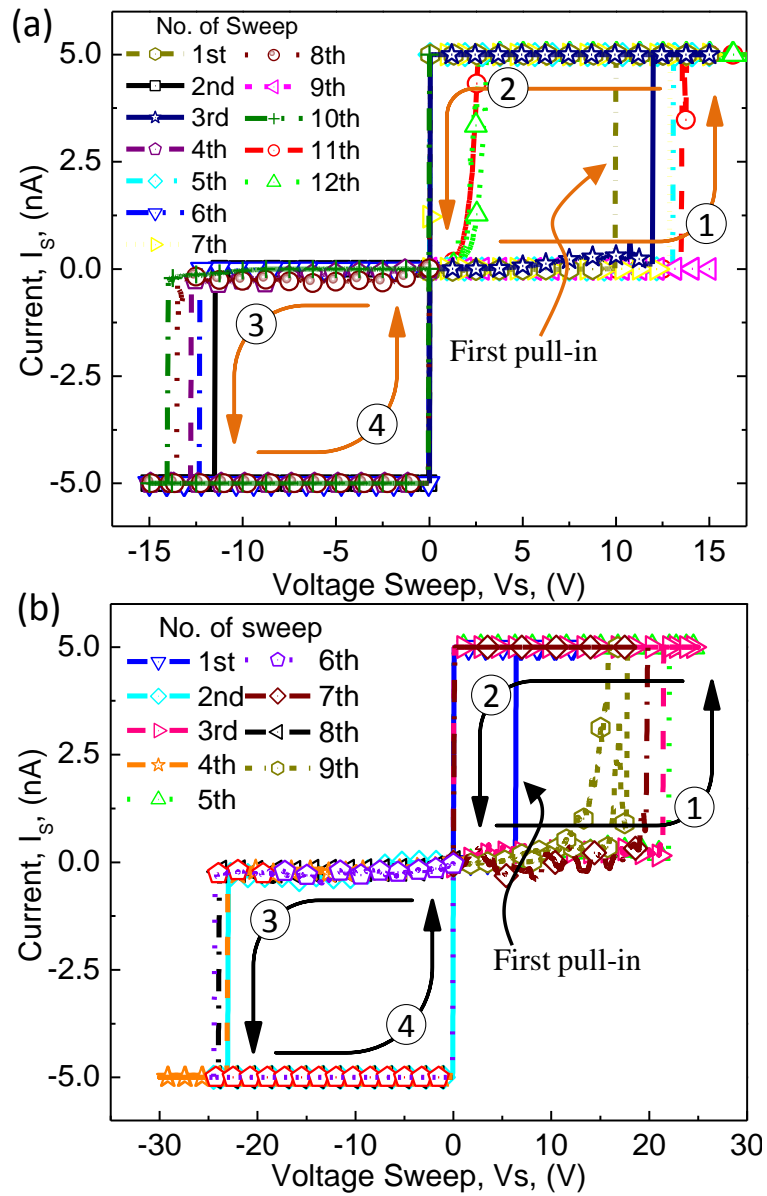
The second pull-in can also be referred as the resetting voltage ( $V_{RESET}$ ) since the function of this voltage is reversing the state of the SiNF. The detailed non-volatile memory operation cycles of 2  $\mu\text{m}$  and 8  $\mu\text{m}$  SiNF are shown in Figure 3.10(a) – (b). From both measurements, the initial pull-in voltage ( $V_{PI}$ ) of the device is lower compared to the rest of the resetting voltage ( $V_{RESET}$ ), this is due to the initial neutral position of the SiNF, where the gap is approximate 80 nm. After the first pull-in, the subsequent operation voltage will be  $V_{RESET}$  where the gap is possibly increased to 160 nm. Thus larger electrostatic force is required to pull-in the switch.



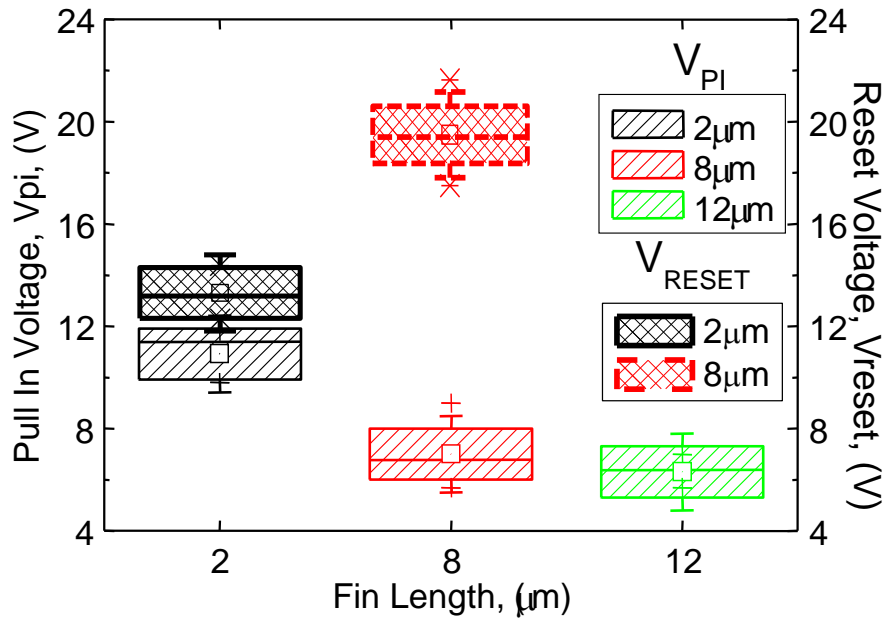
**Figure 3.9: Live video of the SiNF switching in real time, captured under SEM. The SiNF switch is activated and makes contact with the right terminal during operation.**



Referring to the operation sequence as shown in Figure 3.10, the sequence of the hysteresis comes about in a sequence from 1 to 4. In sequence 1, the SiNF is pull-in to the right terminal, when the voltage sweep returns to zero in sequence 2, no pull-out is detected depicting the SiNF is still in contact with the right terminal. As the voltage sweep across the opposite terminal in sequence 3, the SiNF flips as  $F_{ELEC} + F_{SPRING} > F_{VDW}$ . As the voltage sweep returns to zero in sequence 4, van der Waals force again holds the SiNF in contacts. Altogether the device demonstrated a bi-stable hysteresis curve, thus the device operates like a NVM. The 2  $\mu\text{m}$  SiNF operates for the 11<sup>th</sup> sweep before failing as currents returns to zero during voltage back sweep resembling a discharging curve at around 3 – 4 V, following 12<sup>th</sup> sweep trace the same charging curve as voltage sweep vice versa. The same phenomenon happens at the 9<sup>th</sup> sweep of the 8  $\mu\text{m}$  SiNF device. The devices are inspected under SEM and it is determined that the SiNF has burnt and melted to either terminal. It is known that joule heating can be detrimental to such devices. The failure will be further discussed in section 3.3.6.



**Figure 3.10: Measured bi-stable  $I$ - $V$  Characteristic of the NEMS memory. (a)  $2\ \mu\text{m}$  SiNF device (b)  $8\ \mu\text{m}$  SiNF device. The bi-stable operation is shown in a following sequence. (1) First the SiNF is pulled in to the left terminal. (2) Left terminal contact holding by the VDW. (3) SiNF flips to the right terminal. (4) Right terminal contact holding by the VDW. Note that the current is continuous when voltage sweep returns to  $0\text{V}$ .**

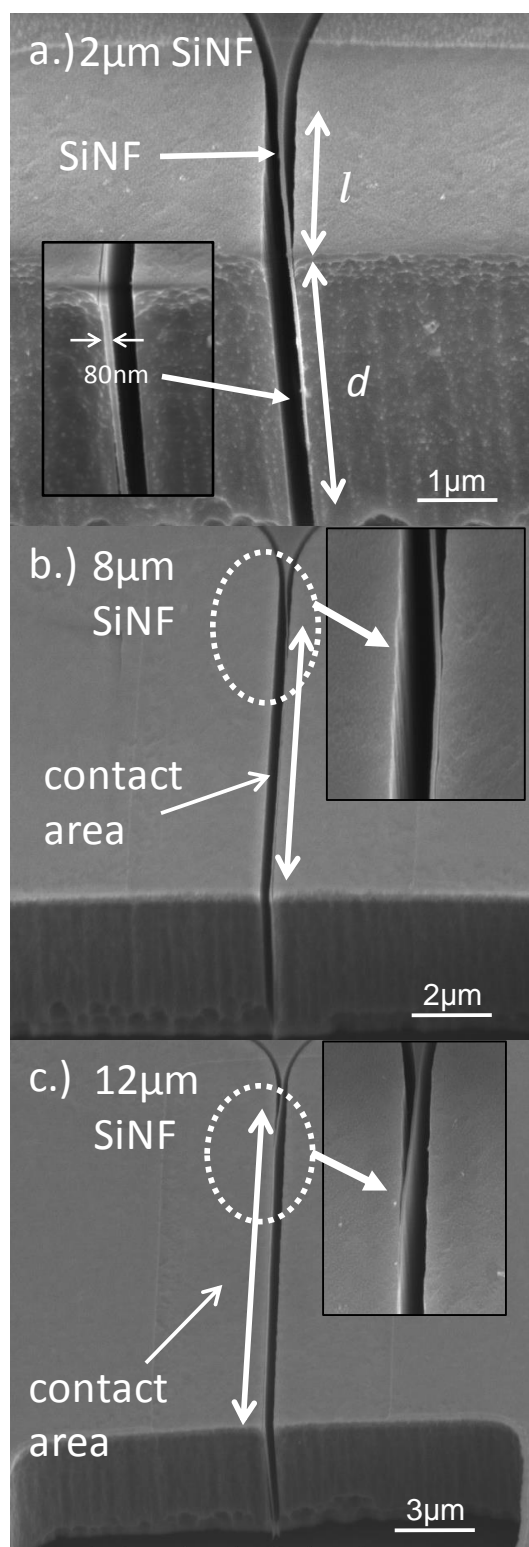


**Figure 3.11: Constant error bar of  $V_{PI}$  and  $V_{RESET}$  versus 2, 8, and 12  $\mu\text{m}$  long SiNF of twenty devices.  $V_{PI}$  reduced while  $V_{RESET}$  increases sharply, while device with fin length of 12  $\mu\text{m}$  cannot be reset due to permanent adhesion.**

From the experiment results, it is shown that the length is crucial in designing a resettable switch. Figure 3.11 shows the correlation between the  $V_{PI}$  and  $V_{RESET}$  versus the length of the SiNF. The measurement is performed statistically for twenty devices and results show  $V_{PI}$  is inversely proportional to SiNF's length. However, the non-volatile hysteresis behaviour is only obtainable in 2 $\mu\text{m}$  devices and 8 $\mu\text{m}$  devices. Overwhelming adhesion force causes drastic increase in  $V_{RESET}$  as the SiNF length increases, which leads to permanent adhesion in 12  $\mu\text{m}$  SiNF switch. The trade-off between the required pull-out energy and the van der Waals force has to be taken into design consideration.

### 3.3.3 Memory and logic domain

In contrast, all 12  $\mu\text{m}$  SiNF can only be activated once and no  $V_{RESET}$  can be detected anymore until the switching voltage reaches breakdown at approximately 120V. In a coincidence, it is found that the SiNF can be switched during SEM inspection. The actuation is highly depending on the electron beam scanning and it happens more often during higher magnification. Figure 3.12 shows the SEM images of all three SiNF devices, which is actuated under the SEM. These devices are measured to be consistent with the inspection. From these SEM diagrams, the contact area can be extracted. 12  $\mu\text{m}$  devices has the largest contact area, the first pull-in contact of such device is catastrophic and causes the device to fail due to permanent adhesion. From the result, van der Waals adhesion cannot be too strong compared to the spring restoring force to enable a re-writeable NVM. The spring restoring force and van der Waals force can be determined with equation (3.2) and (3.3) respectively.



**Figure 3.12: SEM images of SiNF. (a) 2  $\mu\text{m}$  SiNF. Inset: Zoom-in of contact between SiNF and terminal. (b,c) 8,12  $\mu\text{m}$  SiNF device. Insets: Zoom in view of SiNF bending and in contact with either terminal.**

$$F_{spring} = \frac{E}{(1 - \nu^2)} \cdot \frac{dh^3}{4l^3} \cdot g \quad (3.2)$$

Where  $E$  is the Young's modulus,  $\nu$  is the Poisson ratio,  $d$ ,  $h$ ,  $l$  is the depth, thickness and length of the SiNF respectively. Meanwhile the van der Waals force equation according to the Lennard Jones potential [8], is shown below.

$$F_{VDW}(\text{per unit area}) = \frac{H_C}{6\pi} \cdot \left[ \frac{1}{g_0} - \frac{r_0^6}{g_0^9} \right] \quad (3.3)$$

Where  $H_C$  is the Hamaker's constant,  $r_0$  is the interatomic equilibrium distance,  $g_0$  is the cut off distance when the SiNF is in contact. By plotting both forces with respect to contact area, the non-volatile memory region and the logic region can be deduced as shown in Figure 3.13. As the contact area increases, the surface force dominates and the SiNF act as a memory. Since the contact area is depending on aspect ratio, it also means that logic operation is possible.

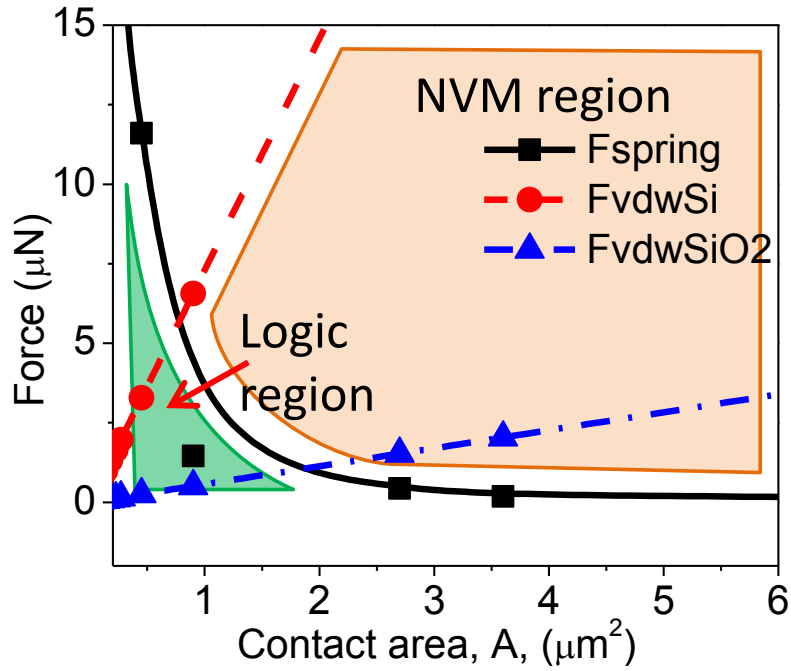


Figure 3.13: Force of spring and van der Waals of silicon beam and contact surfaces of Si and SiO<sub>2</sub> versus measured contact area of SiNF. Non-volatile memory region is defined as the van der Waals force is larger than the spring restoration force of the SiNF. The logic region is vice versa.

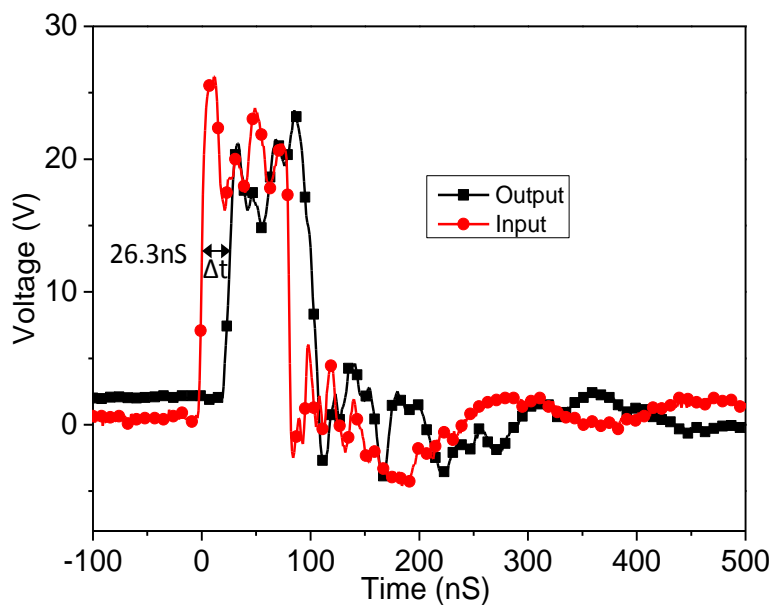
### 3.3.4 Switching speed

The switching speed can be assumed from the natural frequency of a cantilever beam, which is given by the harmonic oscillator formula as shown in (3.4) [27].

$$f_o = \frac{1}{2\pi} \sqrt{\frac{3EI}{mL^3}} \quad (3.4)$$

Where E is the Young's Modulus of Si, I is the moment area of inertia, m is the mass of silicon, L is the length of the SiNF. For an 80 nm × 2 μm SiNF, the switching time is approximately 73ns. The switching speed is also verified

with measurement result as shown in Figure 3.14. The switching speed experiment is performed using the similar testing set up in Section 5.3.4. This is a high speed pulse monitoring unit (PMU) installed in a Keithley SCS 4200 semiconductor analyzer. An 80 ns pulse is applied as input through the first channel of the switch, as the switch closes, the output is detected by a second channel using the PMU. By superimpose the output on the input on the same timestamp, the delay during the switch turns on can be obtained. Overall the switching speed is in nanosecond region.



**Figure 3.14: Switching speed of an  $80 \text{ nm} \times 2 \text{ }\mu\text{m}$  SiNF. The time difference,  $\Delta t$  given by the delay is measured to be 26.3 ns.**

Table 3.1 shows the comparison between different classes of NEMS/MEMS switches. The demonstrated silicon switch is one of the fastest among silicon based switch, the nearest competitor would be polysilicon based switch with 280ns.

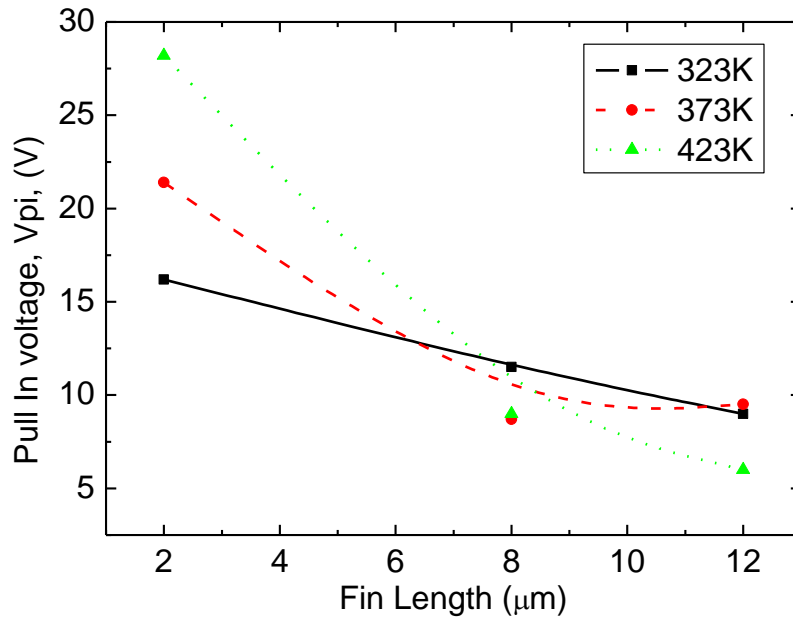


**Table 3.1 Comparison of Switching speed between different NEMS switch**

<b>Institution</b>	<b>material</b>	<b>Measured speed (ns)</b>	<b>Theoretical (ns)</b>	<b>Ref.</b>
Case western University	SiC	< 200	NA	[31, 39]
Sandia Lab	Ru	15-81	NA	[189]
California Institute of Technology	CNT	2.8	20	[211, 118]
Stanford University	Poly Si	NA	280	[171]
National University of Singapore	Si	26	NA	This work

### 3.3.5 Pull-in variation with respect to temperature

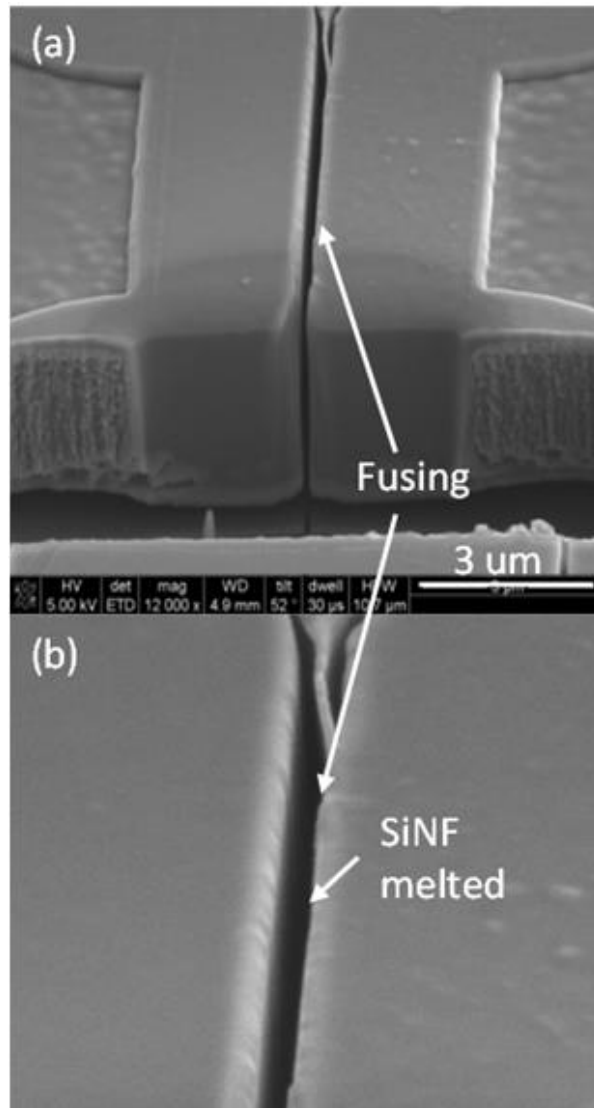
For the first time,  $V_{PI}$  drift versus temperature of such device as shown in Figure 3.15. The temperature of the probe station stage is heated to 100 °C and 150 °C respectively and the pull-in voltage of SiNF with different length is measured. The voltage drift is calculated from the 8  $\mu\text{m}$  SiNF device only, by estimation from the figure, where the voltage difference from 323 - 423K is around 2.4 V. The lowest voltage drift of 24mV/K is measured in this device. Pull-in voltage of three SiNF with 2, 8 and 12  $\mu\text{m}$  is experimentally tested at 50, 100 and 150 °C, which is maximum limit of the temperature controlled stage.



**Figure 3.15:**  $V_{PI}$  at temperature of 50 °C, 100 °C and 150 °C of 2 μm long switch of thickness 90 nm. Low voltage drift of 24mV/K is measured.

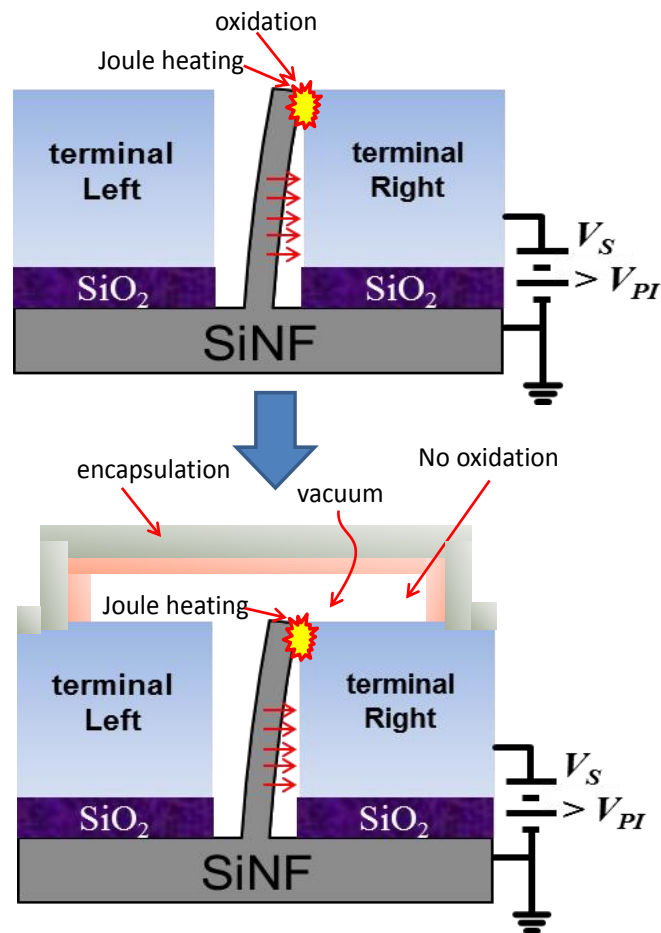
### 3.3.6 Reliability in high temperature and failure analysis

Despite the device's performance in non-volatile memory, the reliability of the SiNF in high temperature is poor. Under normal temperature, the SiNF switch can survive up to tens of cycles. Oxidation and Joule heating are among the reasons the SiNF is not reliable. At room temperature, oxidation happens rapidly especially when the switches are exposed to air. The deterioration is enhanced further by Joule heating. The failures are shown in Figure 3.16. It is observed under SEM inspection that the SiNF is fused to one side of the terminal, the entire beam has melted and joined seamlessly to the sidewall of the actuating terminal. This problem is consistent and happens to most of the devices after failure has occurred.



**Figure 3.16: SEM diagram of an 8  $\mu\text{m}$  SiNF after failure. SiNF is melted and fused to the actuating terminal.**

The possible solution to enhance or improve the reliability of the SiNF is encapsulating the SiNF in a vacuum encapsulation. The concept is shown in Figure: 3.17. With limited oxygen inside the cavity, the surface oxidation of the SiNF is limited. Meanwhile, Joule heating can be controlled via current compliance or build in resistor. The enhancement will be further discussed in the logic switches in the next two chapters.

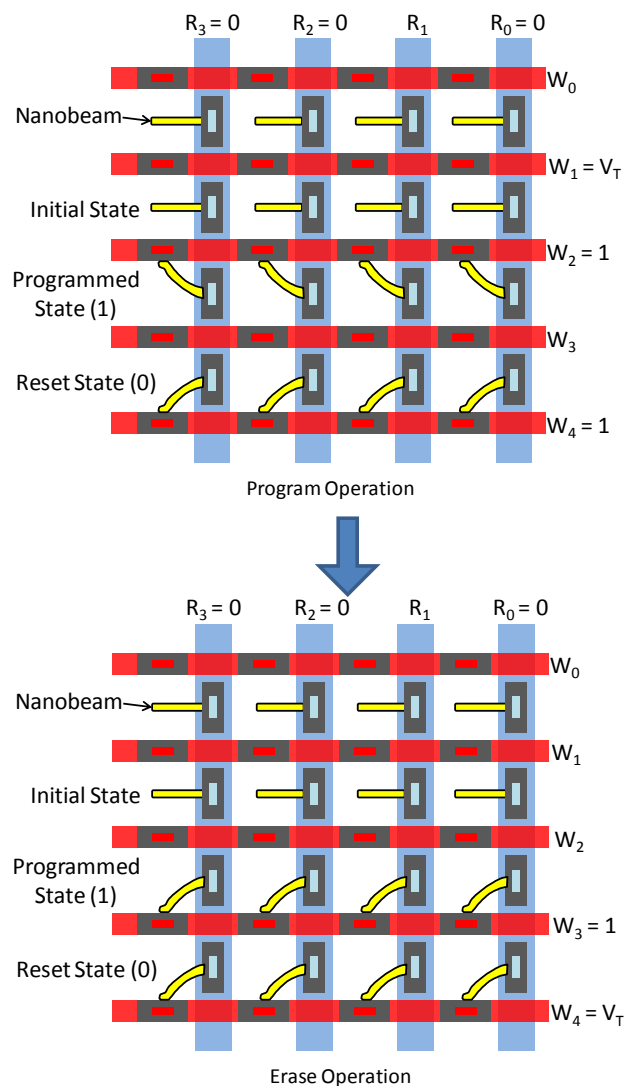


**Figure: 3.17** Vacuum encapsulation of the SiNF switch can prevent oxidation of the contact interface. Meanwhile, Joule heating needs to be reduced to enhance the lifetime of the device.

### 3.4 Non-volatile memory application

To realize an array of devices with a small footprint, an array structure is proposed such that each terminal electrode is shared between two SiNF, as shown in Figure 3.18. To program or erase the device in an array without affecting other cells, a threshold holding voltage ( $V_T$ ) needs to be defined such that it is sufficient to prevent the SiNF from switching when a program voltage is applied to the other electrode, yet insufficient to cause switching itself. For

instance, to erase the programmed state (1) in the same figure,  $V_{RESET}$  is applied to W3 while  $V_T$  needs to be applied to W4 to hold the already reset state (0) where  $0 < V_T < V_{RESET}$ . As such the proposed array structure has shown a possible array of non-volatile memory.



**Figure 3.18: Proposed 2<sup>3</sup> bit memory array implemented by two-terminal SiNF switch. Each device consists of two states, namely Reset State ‘0’ and Programmed State ‘1’. Write and reset operation can be executed by turning on both read and write line. Meanwhile, read operation is performed by low current measurement where device are subjected to a read potential ( $V_{read} < V_{PI}$ )**

### 3.5 Conclusions

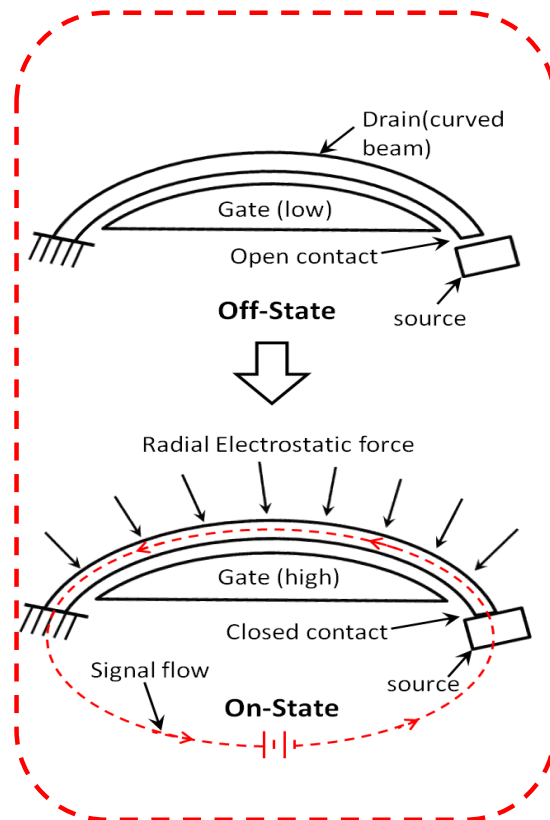
In conclusion, a SiNF non-volatile memory consists of a high aspect ratio (1:35) silicon nanofin (SiNF) with smallest dimension of  $80 \text{ nm } (w) \times 3.5 \text{ }\mu\text{m } (h) \times 2 \text{ }\mu\text{m } (l)$  is characterized in this chapter. The device nano-scale size is among the smallest in its class. The device demonstrates low power operation while exhibiting non-volatile hysteresis loop with two bi-stable states. It is also the first measured result of two way bi-stable hysteresis curve based on novel VDW force for application in NVM memory. Measurement results show bi-stable hysteresis behaviour with pull-in voltage ( $V_{PI}$ ) and reset voltage ( $V_{RESET}$ ) as low as 8.4V and 10.1V. The switching speed of the memory is measured to be 26.3 ns, one of the fastest demonstrated in nano-scale switches. The average voltage drift calculated from SiNF non-volatile memory is 24mV/°C from 50°C to 150°C. Meanwhile, the nano-size gap and width of the SiNF makes the device attractive for scalability with estimated compact density about 390kBits/mm<sup>2</sup>. However, the current fabrication process produce very low yield and the current device has very low reliability especially in high temperature, the failure observed is due to fusing/micro-welding, as a result of Joule heating and oxidation during switching operation. In next chapter, a three-terminal switch with ultra-clean vacuum encapsulation is shown to overcome the problem faced by the SiNF non-volatile memory.

# **CHAPTER 4: DESIGN AND FABRICATION OF A VACUUM ENCAPSULATED SILICON TO SILICON CURVED BEAM LOGIC SWITCH**

## **4.1 Introduction**

Following the poor reliability of the SiNF non-volatile memory in high temperature, an attempt to fabricate silicon based vacuum encapsulated curved switch is fabricated to investigate its operation capability in harsh environment. The logic switch comprised of three-terminals: These terminals consist of drain (movable curved beam), gate (fixed) and source (fixed) as shown in the top of Figure 4.1. The curved beam switch defined in single crystal silicon, which is almost stress-free and homogenous. The entire moving structure and Si-to-Si electrodes are encapsulated in a vacuum environment with electrical interconnects built through the encapsulation to the chip surface and metalized by aluminium. The on-off operation of the curved beam switch is shown in the same figure, where an arbitrary signal can flow through the contact from source to drain when the beam is pulled in electrostatically by the gate. Extremely clean vacuum encapsulation process is performed to seal the switch after release process, providing pristine operating surroundings for switching operation. Meanwhile, the curved beam design has enhanced the spring stiffness of the beam upon contact, resulting in robust

control voltage overdrive. The similar high breakdown voltages are also reported with an inclined curved electrode with rotation around small hinges demonstrated by Grogg *et al* [194].



**Figure 4.1: Illustration of radial electrostatic force exerted on the curved beam when gate potential is changed from high to low. (Condition for pull-in:  $V_{GATE} \geq V_{PI}$ )**

Meanwhile, preliminary reliability study of such switch is investigated and shown here. Failure analyses are performed to show that the reliability is temperature dependent.  $10^7$  on-off cycling test is performed and achieved under room ambient and at least  $10^6$  cycles at elevated temperature of  $400^\circ\text{C}$ , with measured consistent contact resistance of approximately  $30\text{k}\Omega$ . Micro-welding is presumably happening beyond  $400^\circ\text{C}$ ; however, enhanced

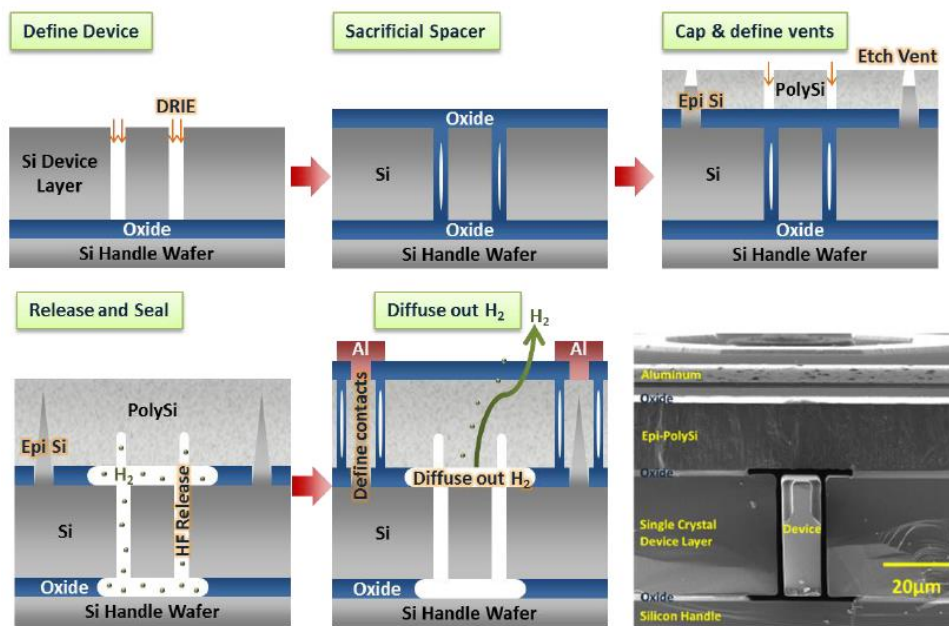


reliability is verified through manipulation of current compliance, which will be detailed in next chapter.

## **4.2 Wafer level vacuum encapsulation**

Based on discussion from the previous chapter, an advanced vacuum packaging is necessary to preserve the lifetime of N/MEMS switch. In this chapter, a vacuum level encapsulation leveraging on a poly-silicon sealing in epi-reactor is proposed. This process is also known as the Epi-Seal encapsulation. The Epi-seal encapsulation process was proposed by researchers at the Robert Bosch Research and Technology Center in Palo Alto and then demonstrated in a close collaboration with Stanford University. In this process, movable silicon microstructures are encapsulated with a layer of epitaxially deposited silicon, allowing for operation in an ultra-clean, hermetic, vacuum environment [184, 185]. High yields (>90%) are typically achieved and a similar process is used commercially by SiTime Corporation to fabricate silicon MEMS resonators [186, 187]. The vacuum level inside the encapsulation is reported and verified [188]. The standard Epi-seal process is as illustrated in Figure 4.2. First, the MEMS structure is defined by etching trenches in the device layer of a SOI wafer using deep reactive ion etching (DRIE). A sacrificial oxide layer is deposited to fill the trenches and to provide an oxide spacer layer above the device. Contacts are etched in the oxide and a silicon layer is deposited in an epitaxial reactor. This results in

crystalline silicon where there is a crystalline seed and epitaxial poly-silicon where there is oxide. Release holes are then etched into this cap and vapour HF is used to etch oxide to release the device. After a high temperature hydrogen bake in an epitaxial reactor to remove contaminants and native oxide, a second layer of epitaxial silicon is deposited, sealing the device in a clean cavity. Thereafter, electrical isolation and contacts are defined. The pressure in the cavity is further lowered by diffusing hydrogen in the cavity out, achieving a pressure of a couple of Pa.

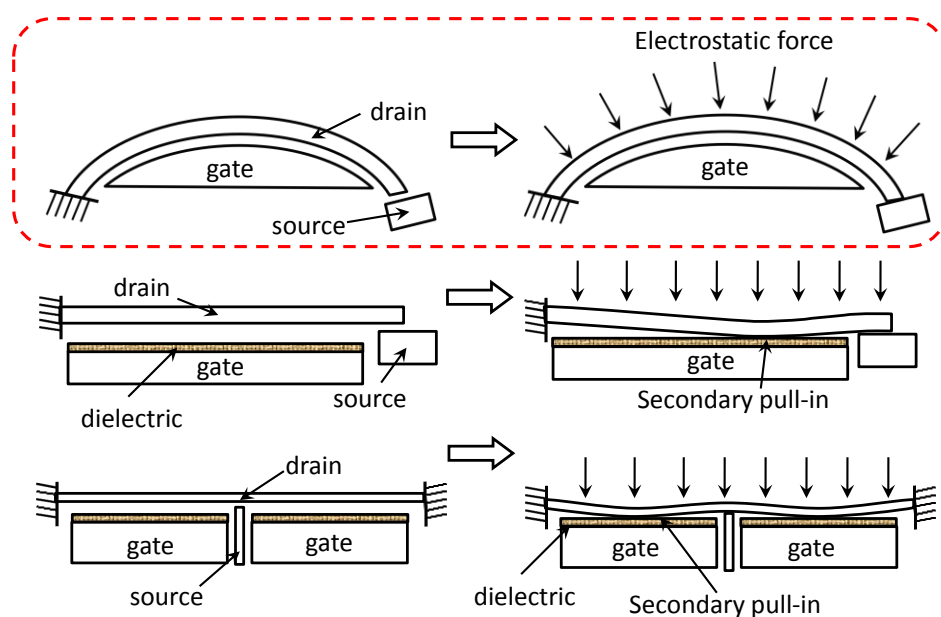


**Figure 4.2: Epi-seal process flow. Starting from the left: Device definition, sacrificial and spacer deposition, cap and release hole patterning, poly-silicon sealing and interconnect redistribution [184].**

### **4.3 Robustness of a curved beam structure against secondary pull-in failure**

Some undesired properties such as secondary pull-in prevent or degrade the performance of MEMS switches [151, 189]. The phenomenon of secondary pull-in is illustrated in Figure 4.3. For cantilever and doubled-clamped beam designs, secondary pull-in can occur when the gate voltage is overdriven, and the excessive electrostatic force causes the beam to contact the gate, resulting in a short circuit and device failure. This may also happen during gate voltage spikes. Some reported MEMS switches implement a layer of dielectric insulation such as alumina ( $\text{Al}_2\text{O}_3$ ) or silicon dioxide ( $\text{SiO}_2$ ), between the gate and the actuation beam to prevent secondary pull-in and catastrophic short circuits [41, 47, 179]. These dielectric layers can prevent device failure, but also seriously degrade device operation at critical dimensions as leakage happens. Hence, gate drain pull-in is undesired and rugged ohmic contacts are greatly preferred. To derive a robust architecture to the three-terminal logic switches, curved beam is designed as the movable contact. In addition to the benefits of ultra-clean vacuum encapsulation, the curved beam design provides a high tolerance to a gate voltage overdrive. When the drain is in contact with source, the source acts as a stopper for the curved beam, and the curved shape of the beam reduces further deformation due to the arch-like structure, resulting in a robust configuration that is able to sustain a high gate

voltage. This also increases the resilience to large overshoots during gate voltage pulses. These switches are highly suitable in rugged electronics applications such as downhole, aerospace and automotive applications. Regardless of the high contact resistance, logic devices and on-off circuits in harsh environments can be achieved.



**Figure 4.3: Illustration of secondary pull-in comparison between electrostatic switch for curve beam, free-end cantilever beam, double-clamped beam. The curved beam structure offers robust gate voltage overdrive and prevention from secondary pull-in due to the enhanced mechanical strength after pull-in happens.**

#### 4.4 Curved beam stiffness and breakdown voltage tolerance

Since the curved beam's width proposed is much smaller than the radius of curvature,  $R \gg h$ , the spring constant of the curved beam can be approximated by the curved beam deformation model, where neutral axis of the curved beam

is parallel but not equal to the centroid axis. Subsequently, the pull-in voltage can be approximated by the parallel plate capacitor model, assuming negligible fringing effects, since the width-to-gap ratio is approximately (26:1) with largest gap being 1.5  $\mu\text{m}$ , and the thickness of the device layer is 40  $\mu\text{m}$ .

#### 4.4.1 Governing equations for curved beam's stiffness

The curved beam reaction and deformation formulas are also defined similarly for circular arches as derived by Roark's formula for stress and strain [190]. The vertical deformation of a one end free, the other end clamped cantilever is given by equation (4.1) below.

$$\delta_V = -\frac{R^3}{EI} L_{FV} \quad (4.1)$$

Where  $R$  is the radius of curvature,  $E$  is the Young's modulus of silicon,  $I$  is the area moment of inertia. The loading term,  $L_{FV}$  is assume to be a partial uniformly distributed radial loading, given by equation (4.2)

$$L_{FV} = wR \left[ k_1 \sin\theta \left( \frac{\pi}{2} + \sin\theta \cos\theta \right) + 2k_2 \sin\theta \left( \frac{\pi}{2} - 2\sin\theta \cos\theta \right) \right] \quad (4.2)$$

Where  $w$  is the unit load,  $R$  is the radius of curvature,  $k_1 = 1-\alpha+\beta$ ,  $k_2 = 1-\alpha$ .

Where the hoop stress deformation factor,  $\alpha$  is given below,

$$\alpha = \frac{I}{A_C R^2} \quad (4.3)$$

Where  $I$  is the area moment of inertia,  $A$  is the cross-sectional area,  $R$  is the radius of the curvature. The radial shear deformation factor,  $\beta$  is given by below,

$$\beta = \frac{FEI}{GA_C R^2} \quad (4.4)$$

Where  $E$  is the Si Young's Modulus,  $I$  is the second area moment of inertia,  $R$  is the radius of curvature from centroid,  $A$  is the cross-sectional area of the beam and  $G$  is the shear modulus of elasticity. Since the radial force is a full span,  $\theta = \pi/2$ , simplifying both equation above gives

$$\delta_V = -\frac{\pi w R^4}{2EI} (k_1 + 2k_2) \quad (4.5)$$

Rearranging the equation, the spring constant of the curved beam is given by equation (4.6)

$$K_C = \frac{2EI}{3\pi R^3 (1 - \alpha + \frac{\beta}{3})} \quad (4.6)$$

In order for the switch to be turned on, the potential applied across gate and

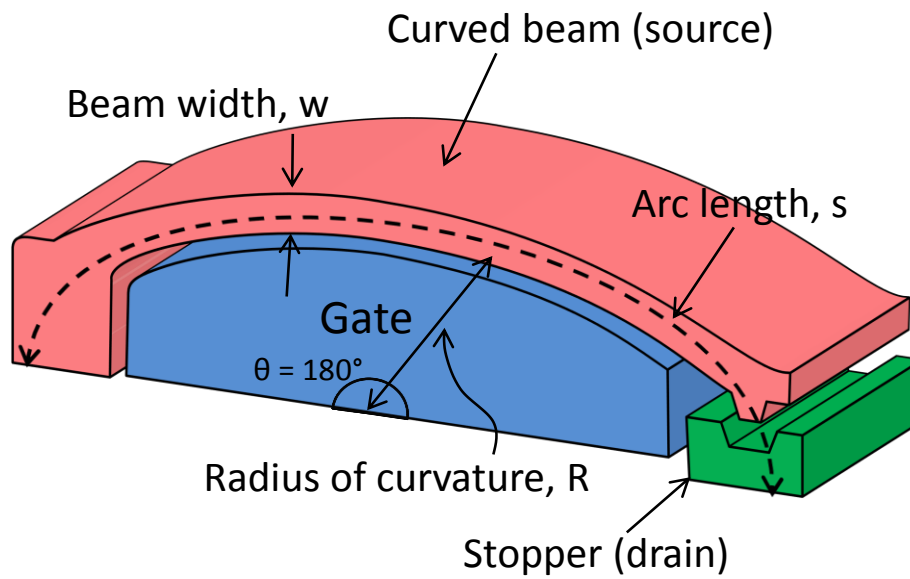
drain has to overcome the curved beam spring restoration force ( $V_G > V_{PI}$ ), where  $V_{PI}$  is the pull-in voltage. In most ideal case, pull-in voltage due to parallel capacitance can be approximated by the equation (4.7).

$$V_{PI} = \left( \frac{8 K_C d^3}{27 \epsilon A} \right)^{\frac{1}{2}} \quad (4.7)$$

Where  $K_C$  is the spring constant of the curved beam,  $d$  is the separation gap between the gate and the drain,  $\epsilon$  is the relative permittivity of vacuum,  $A$  is the effective capacitive area between gate and drain.

#### 4.4.2 Finite element simulations and boundary conditions

A 3D FEM simulation (Coventorware) model is used to simulate the pull-in voltage for different beam length, widths, and radii of curvature. In the simulation, a voltage is swept across the gate, and the upper and lower bounds of pull-in voltage were calculated. Figure 4.4 shows a cross-section layout of the semi-circular switch with  $\theta = 180^\circ$ . The curved beam strength after pull-in is also simulated to find out the robustness of the beam against secondary pull-in failure.

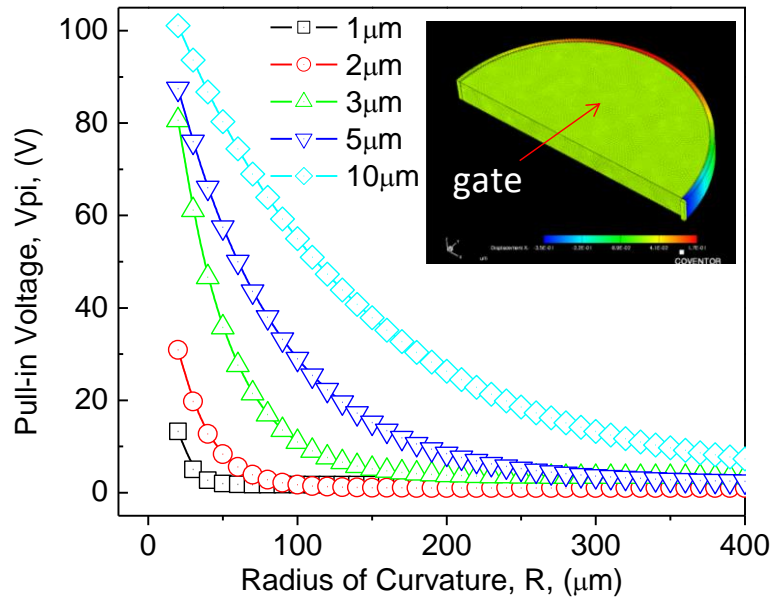


**Figure 4.4: Cross-section layout of the semi-circular curved beam electrostatic switch design.**

Pull-in voltage ( $V_{PI}$ ) can be obtained using Coventorware's CoSolve to solve both the mechanical and electrostatic physics domains. The electrostatic force is computed by applying a potential difference between gate and curved beam (source). This force is then substituted into the mechanical domain to calculate the deflection. Iterating between these two domains yields a static solution with low voltage differences. The FEM simulation is solved based on non-linear iteration computation, where deflection caused by electrostatic force is calculated based on every sweeping voltage step as parameter. The simulation will diverge at some point when sweeping voltage is beyond the pull-in voltage. Pull-in phenomenon is defined as the 1/3 distance of the actuation gap. As the gap closes, the simulation generates a divergence due to the non-linear force generated by electrostatic force. The program is



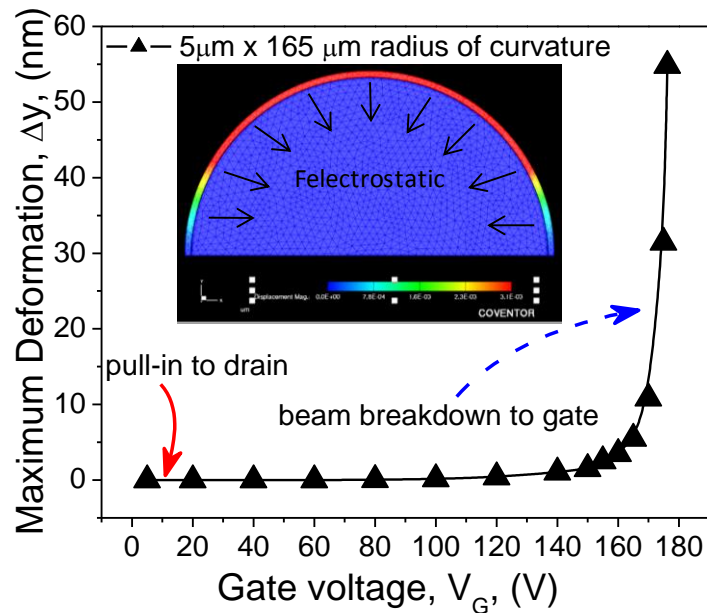
intelligent enough to stop by itself, and return to iterate a lower voltage input subsequently until it gets a convergence. Once the difference between the voltages fall below the user's setting resolution, the simulator stops and  $V_{PI}$  is determined. In this case, it is the accuracy of the pull-in voltage. The electrostatic force is also determined by the voltage sweep. It is determined that  $V_{PI}$  decreases for increasing radius of gate  $R$ , and the relationship generally follows a double exponential decay model as shown in Figure 4.5. This relationship was tested and verified for several widths of the beam ( $w$ ) and showed in next chapter. Since the target actuation voltage for the switch device is in the range of 10 – 30 V, for various  $w$ , the upper and lower bounds of  $R$  has to be determined. This was made possible through interpolation and/or extrapolation of the FEM results. According to FEM simulations, for the same  $w$  and  $s$ , a decreasing  $V_{PI}$  is observed with decreasing  $\theta$ . This is agreeable with the analytical model, since increasing  $\theta$  is equivalent to reduce the spring constant of the beam, Furthermore, using Coventorware, the net electrostatic force acting on the beam was calculated.



**Figure 4.5: Simulation result of pull-in voltage versus radius of curvature for curved beam with varying widths. Inset: 3D model of curved switch (Displacement: 0 - 0.86  $\mu\text{m}$ ).**

In the breakdown voltage (secondary pull-in of beam-to-gate) simulation, a voltage ramp trajectory is applied to the gate and the beam's mechanical response is computed with a double clamped arch-structure as shown in the inset in Figure 4.6. It is assumed that when curved beam contacts source, it becomes a double-clamped arch instead of a free-end curved cantilever. As the beam deforms until a critical voltage, the growth of electrostatic force becomes dominant over the linear mechanical restoring force. This response is again non-linear and numerous CoSolve iterations are performed to find a stable solution. A set of iterations are repeated between convergence and divergence of the solutions to determine the stable breakdown voltage of the arch structure. The breakdown voltage is thus determined in a similar manner

as the pull-in voltage described above, with the exception of the double-clamped boundary conditions. The spring constant of the curved beam is expected to be approximately 16 times of a straight cantilever beam, resulting in very high breakdown voltage endurance. Simulation results of a  $5\ \mu\text{m} \times 165\ \mu\text{m}$  radius beam which has pull-in voltage of 11 V capable of withstanding excessive overdrive gate voltage and only breakdown at 174 V as shown in Figure 4.6.



**Figure 4.6: Simulated high breakdown voltage of 174 V with initial pull-in and contacted drain at approximately 11 V. Inset: Pull-in of drain to gate during breakdown. (Displacement:  $0 - 3.1 \times 10^{-3} \mu\text{m}$ )**

#### 4.4.3 Stopper design

The contact dimple is designed to reduce stiction while maintaining low operating voltage. As the spring stiffness is non-linear to its length and

actuation gap, it is challenging to minimize the contact area to prevent stiction. Surface forces and micro-welding between contact's asperities may be the cause of stiction. In this chapter, all of the curved switches have only a single and identical dimple. Note that actuation of the curved switch is centripetal to the centre of radius (0,0) and the radial electrostatic force is always tangential to the beam curvature. Therefore, rotating motion is considered when the curved beam is being actuated, with one side being anchored. The details of the contact design are shown in Figure 4.7. The beam is attracted towards the gate by radial electrostatic force. After pull-in, the curved beam will assume a new position with a gap of  $g_o'$ . Hence,  $g_o$  has to be greater than the contact distance  $g_c$  to prevent short circuit between gate and drain. Thus, a multiplication factor  $x$  of 1.5 is used throughout the design. The initial designed gap,  $g_o$ , is given by equation (4.8).

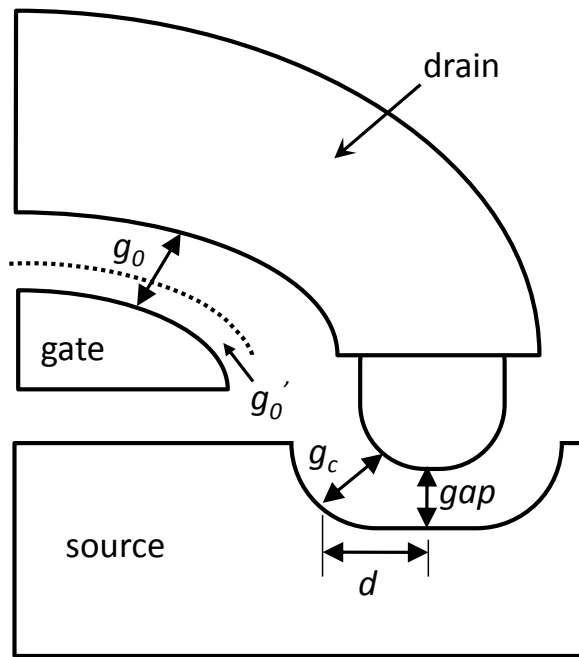
$$g_o \geq x\sqrt{gap^2 + d^2} \quad (4.8)$$

where

$$g_o' = g_o - g_c$$

$$g_c \approx \sqrt{gap^2 + d^2}$$

Where  $g_o$  is the initial gap,  $x$  is multiplication factor,  $g_h$  is the horizontal distance between contact points and  $g_v$  is the vertical distance between contact points.



**Figure 4.7: Contact dimple stopper and contact distance requirement for curved beam switch.**

#### 4.4.4 Design of Experiment (DOE) parameter

Table 4.1 shows the parameter decided for curved beam after both simulation and numerical solution are performed.

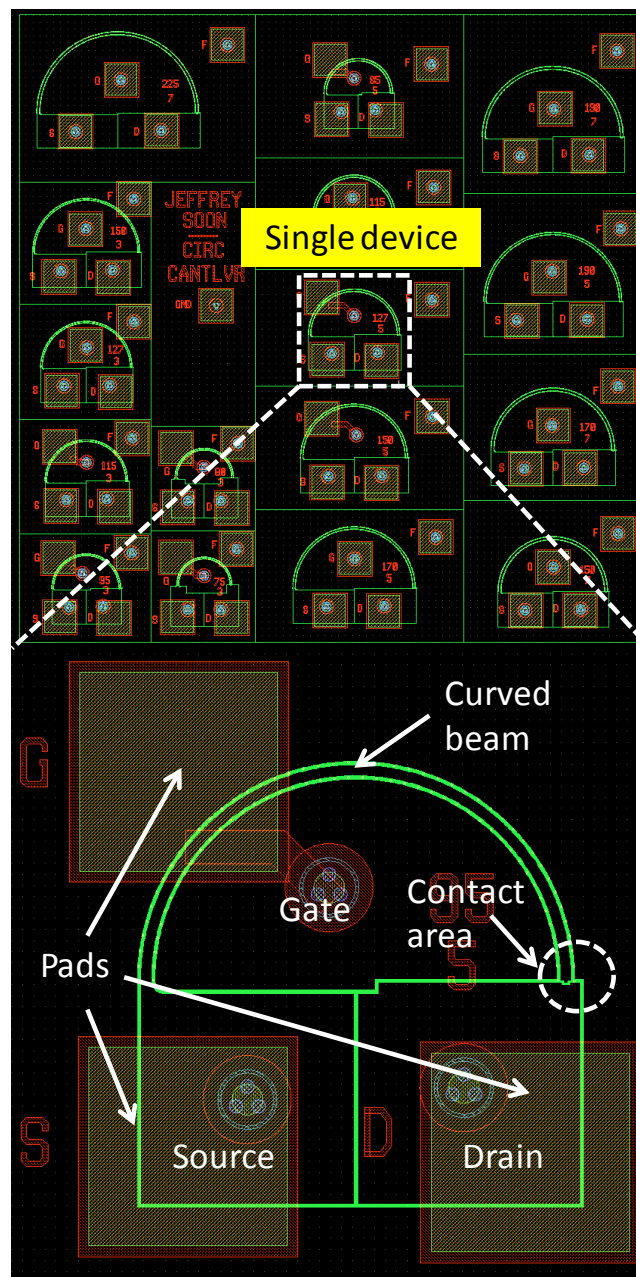
**Table 4.1 Curve beam parameters in design of experiment (DOE)**

Parameters	Value ( $\mu\text{m}$ )	Pull-in voltage
Beam width, $w$	3, 5	10 – 30 V
Radius of curvature, R	75, 80, 115, 127	

## 4.5 Design approach

### 4.5.1 Layout view

The layout design is part of a multi project wafer (MPW) initiated by Epi-seal process team and a single cell is shown in Figure 4.8.

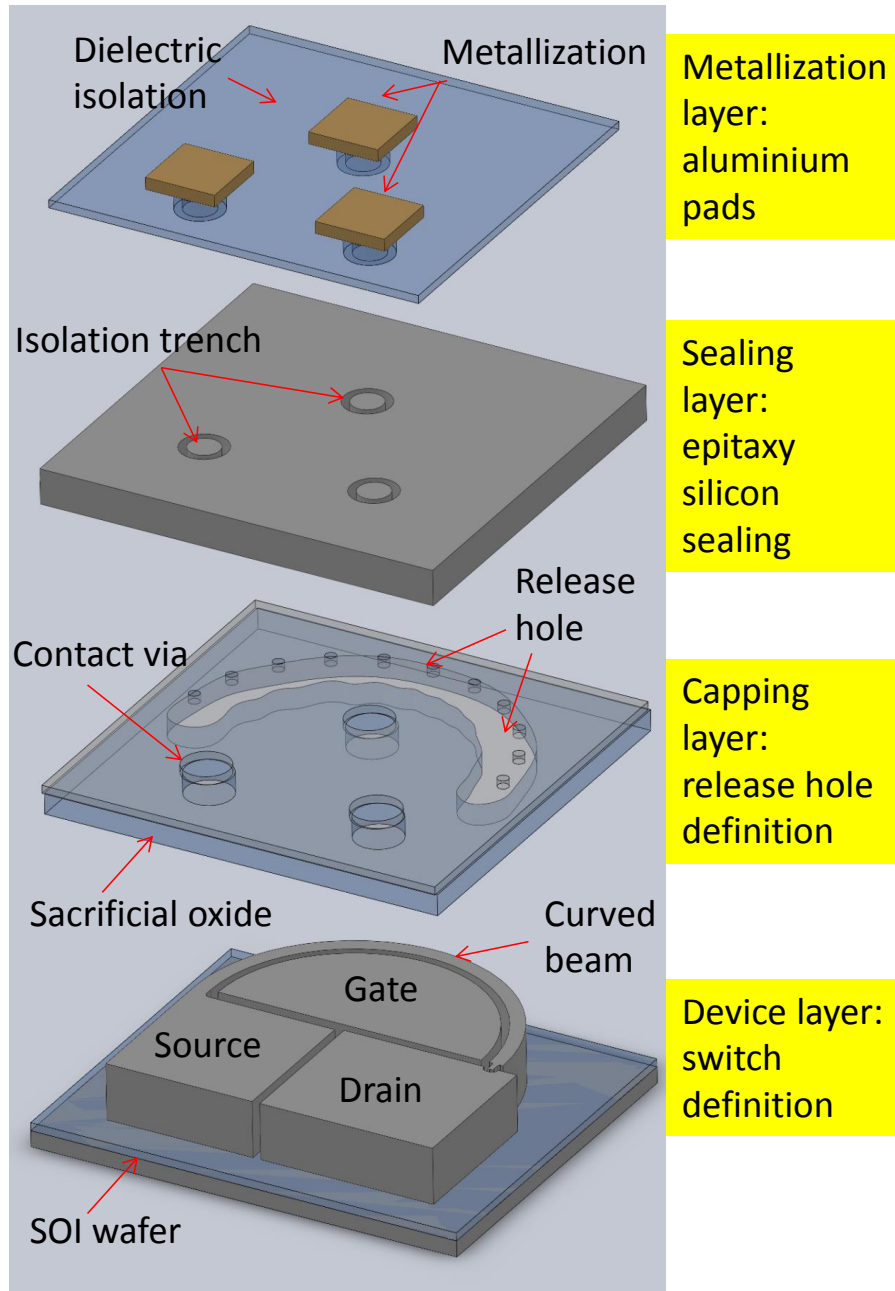


**Figure 4.8:** Layout view of one  $3 \times 3 \text{ mm}^2$  die. A single device cell is shown at the bottom. One device comprised of a curved beam, gate and drain.

The available space is limited to  $3 \times 3 \text{ mm}^2$  die. Thus the design rules for the epi-seal fabrication place a limit on device dimensions. The gap between drain and gate ranges from  $1.0 - 1.5 \text{ }\mu\text{m}$  and gap between drain and source is  $0.7 - 0.8 \text{ }\mu\text{m}$ . Gap distance is important in lowering pull-in voltage, which is proportional to  $\text{gap}^{3/2}$ . However, this gap has to be considered carefully as it is defined by etching unless some surface compensating process can be performed to fill the etching trench in order to make smaller gap.

#### **4.6 Fabrication Process**

Figure 4.9 shows the exploded view of the vacuum encapsulated switch. In the bottom layer, the MEMS switch consists of three terminals: source (movable curved beam, fixed at one end), gate (fixed) and drain (fixed) defined on SOI wafer. Further up layer is the capping layer with release holes and silicon sealing layer. In the sealing process, the ultra-clean environment is created for the active part of the device during the encapsulation as part of the Epi-seal process, when the wafer is sealed at temperature  $> 1100 \text{ }^\circ\text{C}$  with hydrogen, dichlorosilane and hydrogen chloride in an Epi-reactor. This process eliminates residual oxygen, hydrocarbons and water, leaving only sub-Pa pressure. Simultaneously, the sealing layer acts as a contact via to the device's terminals. An isolation trench etches followed by dielectric fill and contact metallization is performed to create the top metal pads and interconnects.

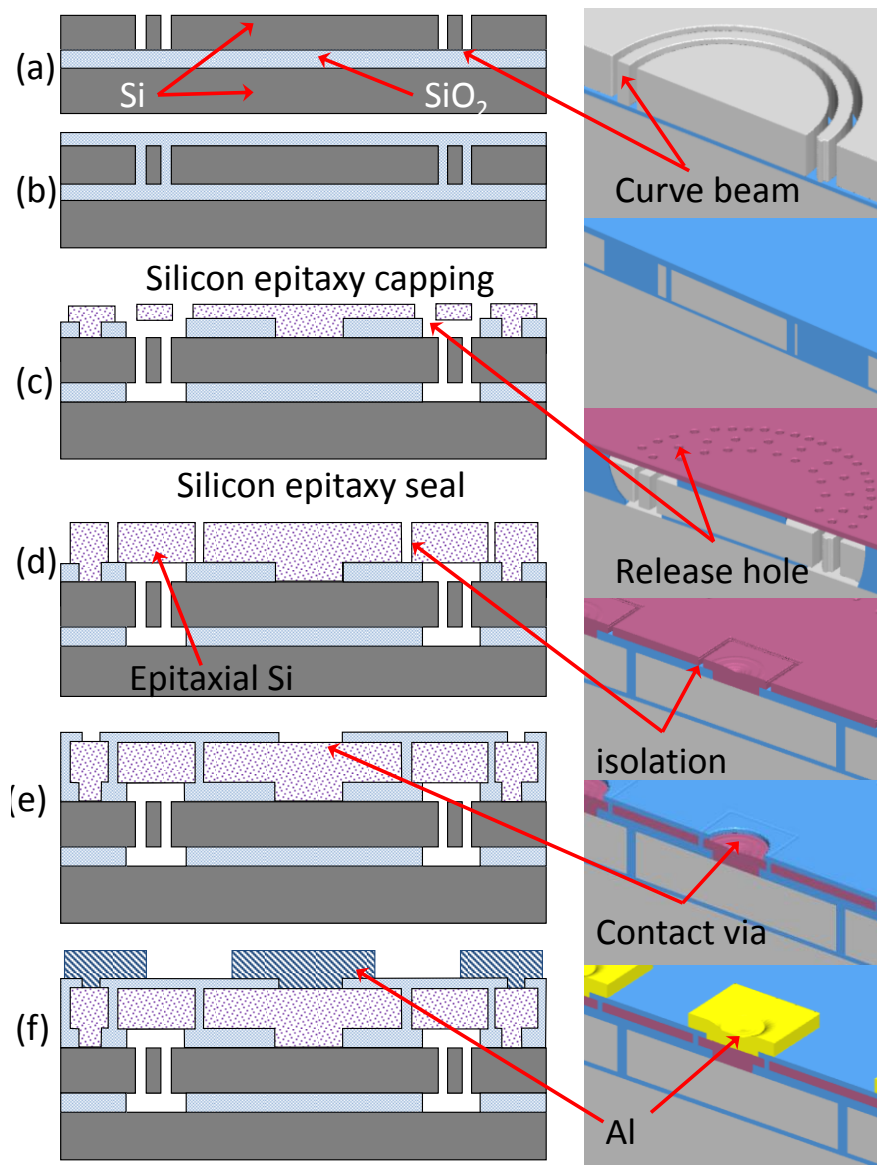


**Figure 4.9: Exploded view of the Si-to-Si MEMS switch with encapsulation layers consist of device layer, capping layer, sealing layer and metallization layer with different function.**



#### 4.6.1 Detailed Fabrication and critical steps

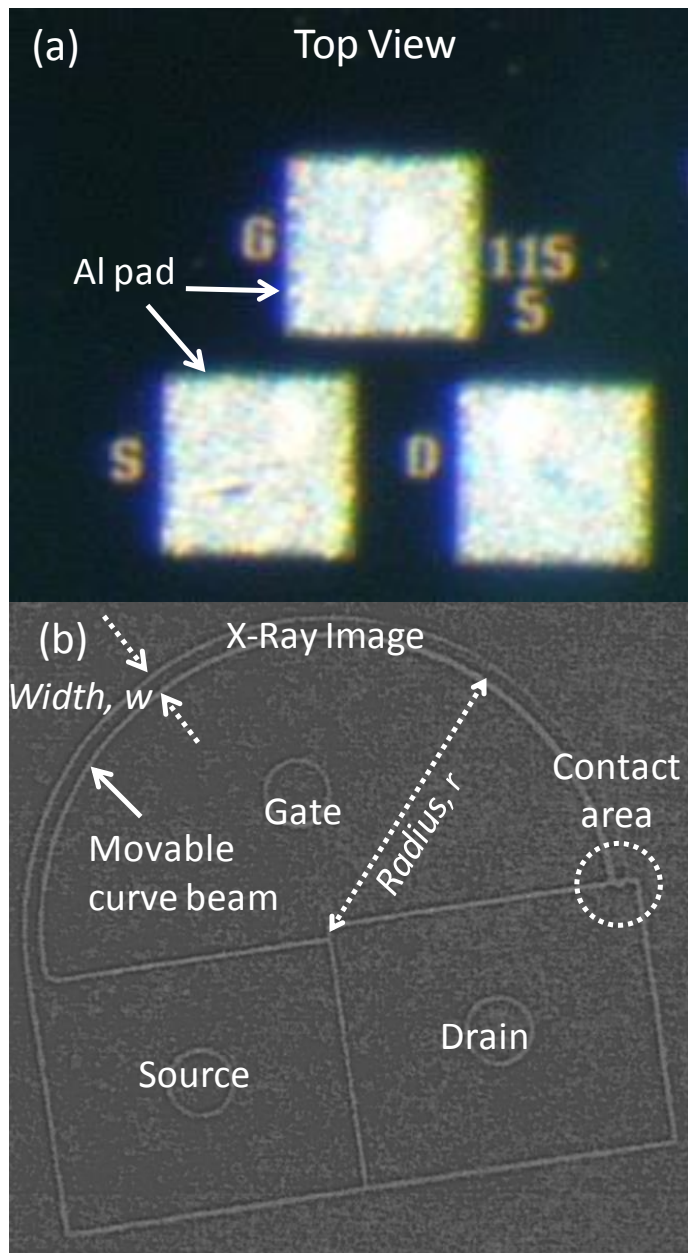
To realize or simulate the most ideal environment, pristine vacuum level encapsulation is a requirement to investigate the Si-to-Si contact. Such process flow is shown in Figure 4.10. Initial SOI wafer of 40  $\mu\text{m}$  thick device layer with 1  $\mu\text{m}$  buried oxide is used. First, deep reactive ion etching (DRIE) is processed to etch 40  $\mu\text{m}$  deep trenches into thick silicon device layer, stopping on  $\text{SiO}_2$  layer. After that, sacrificial  $\text{SiO}_2$  is low pressure chemical vapour deposited to overfill the trenches. In this context the etching gap of the initial DRIE has to be limited so overfill can completely seal the etched trench. Next, the  $\text{SiO}_2$  layer is etched to define where the electrode should be interfaced, at the same time the opening area serves as the anchor area for the following Si epitaxy capping. The release hole is patterned and etches in the Si capping layer to provide access to the  $\text{SiO}_2$  underneath. Then, isotropic vapour hydrofluoric acid is used to etch the oxide in order to release the beam. Subsequently the release hole is sealed by second layer of Si epitaxy. This process is also referred as the Epi-Seal where a few Pa of pressure level can be achieved. During the sealing, the wafer is exposed to high temperature with hydrogen gas content and this process removes most impurities and polymers as reported [188, 191]. Subsequently, top Si is isolated with  $\text{SiO}_2$  and finally the contact pads are open and metalized with aluminium.



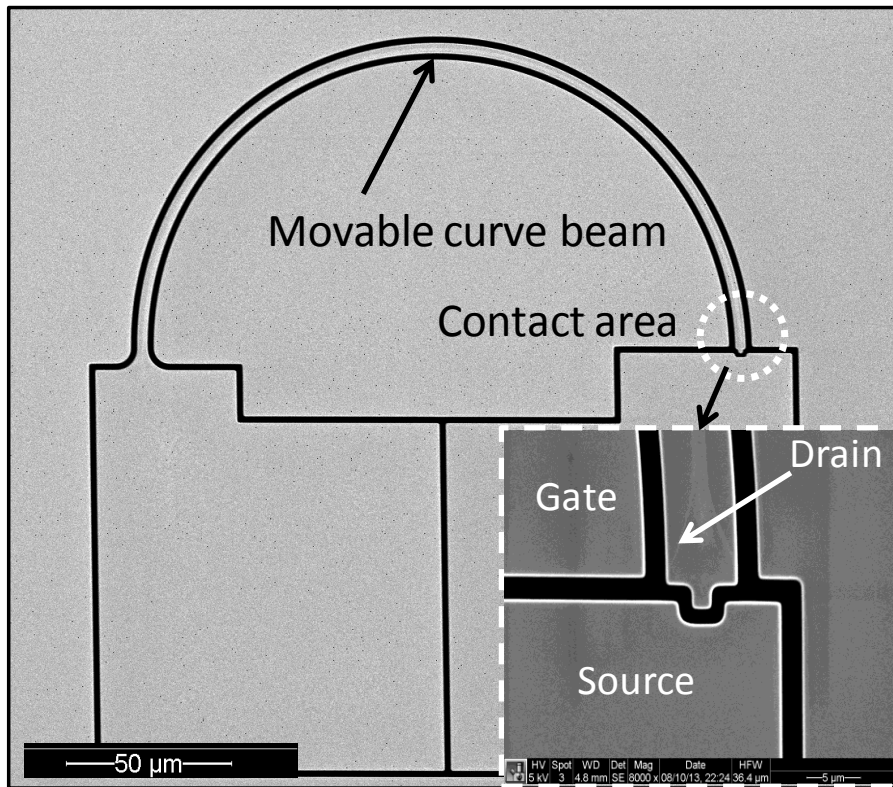
**Figure 4.10: Fabrication process flow of encapsulated curve switch. (a) Si deep trench etching. (b)  $\text{SiO}_2$  overfills to seal trench. (c) Via definition with device release. (d) Si epitaxy sealing and electrode isolation. (e) Passivation opening. (f) Al metallization.**

## 4.7 Fabrication outcome

A Si-to-Si MEMS switch, consist of all Si material, is defined on single crystal silicon. This device has homogenous material property and is stress free after fabrication. Mainly 3  $\mu\text{m}$  and 5  $\mu\text{m}$  width curved beam devices are fabricated and then characterized. The dimension is also restricted by the design rules of the MPW wafer. The entire moving structure is encapsulated in vacuum environment with only electrical terminal interconnects are fanned out on the chip surface and metalized by aluminium. These terminals consist of drain (movable curve beam), gate (fixed) and source (fixed) is shown in X-Ray diagram in Figure 4.11. The finish chip has flat topography and only the metal pads are visible under optical microscope. This is shown in Figure 4.11(a). The X-ray image of the encapsulated device is shown in Figure 4.11(b). The curved beam's dimension, radius and width, is represented by  $r$  and  $w$  in the same figure, where the beam is defined on the circle of the radius. This image is taken with an X-ray inspection system (DAGE XD 6500). The image reveals the encapsulated switch under the epitaxy seal.



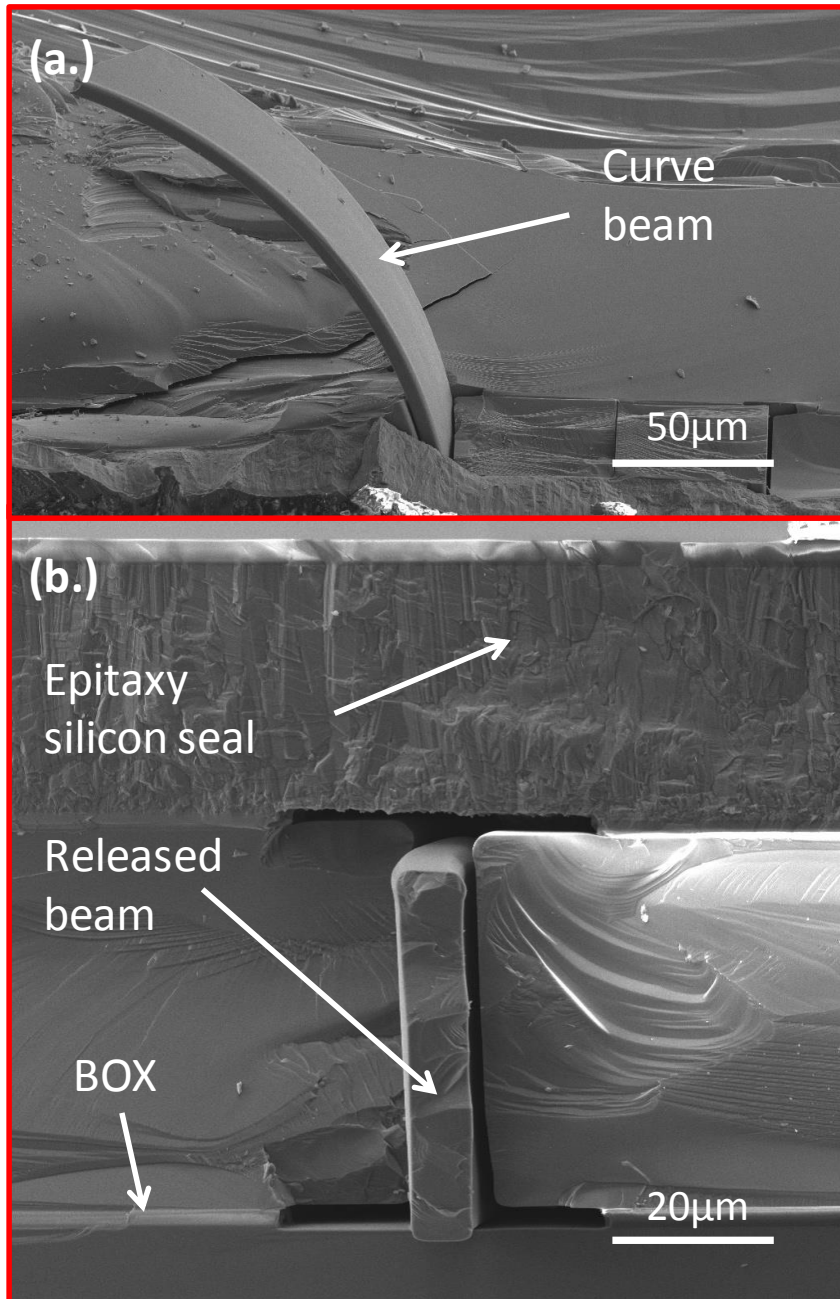
**Figure 4.11: (a) Top view of the finished chip with metalized aluminium pad. (b.) X-Ray image showing the encapsulated three-terminal switch comprised of a movable curve beam (Source), control terminal (Gate) and contact terminal (Drain).**



**Figure 4.12: SEM image of a  $3\ \mu\text{m} \times 85\ \mu\text{m}$  radius curved switch before encapsulation is performed. The image is captured after the DRIE process. (Inset) Zoom-in of the contact region.**

Since the chip is fully encapsulated, it is difficult to inspect the internal structure due to the Epi-seal process. Nonetheless, SEM image of a three-terminal curved beam switch before capping is shown in Figure 4.12. It is clearly seen that the DRIE is processed well and the contact region is well defined. Due to process limitation, the minimum gap distance can be defined as advised by the Epi-seal process is  $0.7\ \mu\text{m}$ . The cross-section of encapsulated curved beam is shown in Figure 4.13. A protruding silicon curved beam is shown in Figure 4.13(a). Note that during the epi-seal process, the DRIE etched surfaces are smoothen under silicon reflow process as

reported [192]. The released beam is encapsulated under a  $\sim 25\ \mu\text{m}$ -thick epitaxial polysilicon layer, as shown in Figure 4.13(b).



**Figure 4.13: SEM cross-section of a curved switch device showing the released curved beam with a poly-silicon encapsulation seal. (a.) Encapsulated curved beam. (b.) Epi-Seal process with encapsulated beam.**

## 4.8 Conclusion

In conclusion, this chapter introduced a vacuum encapsulated three-terminal logic switch that relies on a curved beam for better reliability enhancement. The Epi-seal vacuum packaging provides a pristine environment for the contact to operate in harsh environment. Due to the high temperature (1100 °C) sealing process, oxygen and polymers are removed from the release cavity, thus oxidation of switch is unlikely to happen during operation. Spring constant of the curved beam is derived in order to obtain the design values of the device dimension. The device is then simulated and designed using FEM analysis to obtain desired pull-in voltage. Meanwhile, overdrive voltage tolerance is simulated to be at least 10 times of the pull-in voltage, depicting stiffness improvement in the curved beam actuation mechanism. The overdrive voltage tolerance offers robust operating voltage and is more reliable against surge protection. Subsequently, the process flow is explained in details and the fabrication outcome is presented. The electrical characterization of this device will be detailed in next chapter.

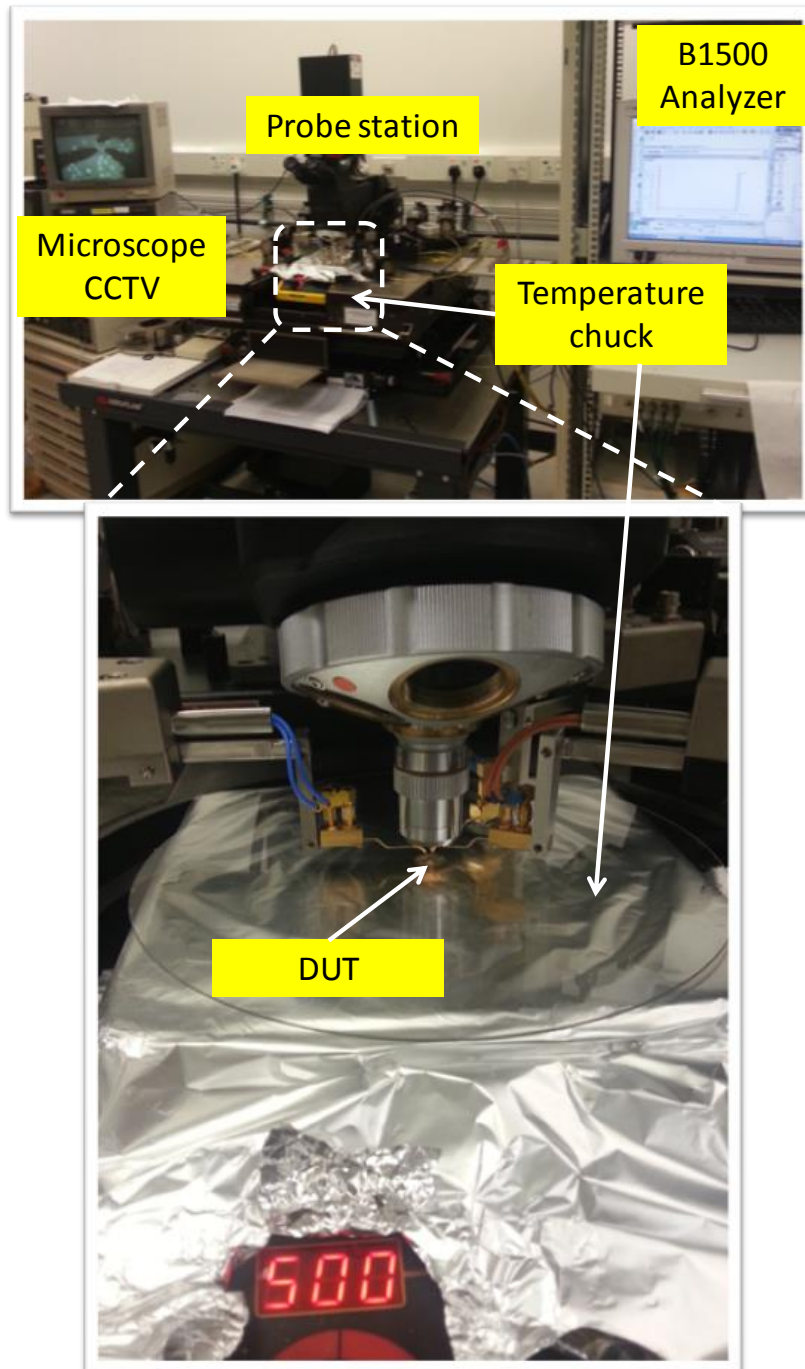
# **CHAPTER 5: CHARACTERIZATION OF A VACUUM ENCAPSULATED SILICON TO SILICON CURVED BEAM LOGIC SWITCH IN HARSH ENVIRONMENT**

## **5.1 Testing set-up and procedure**

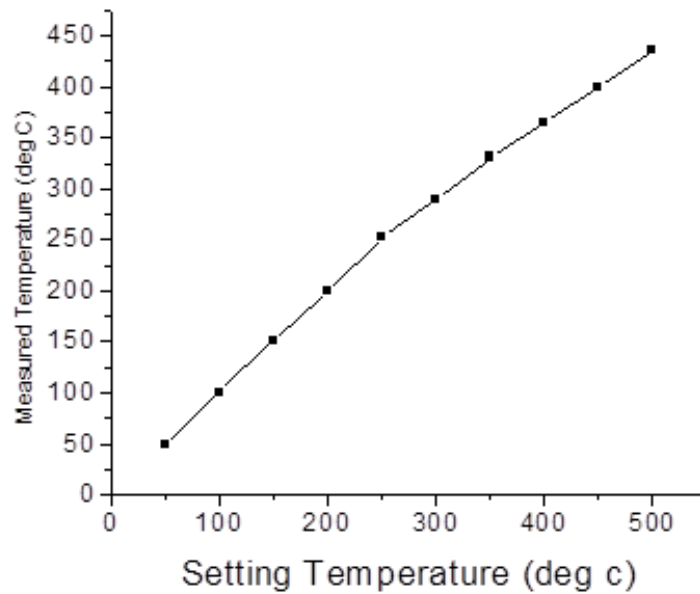
At room temperature, the chips are exposed to air and tested in a Cascade Microtech microchamber (RBL-6100) with semiconductor analyser (Agilent B1500) equipped with two standard source monitoring units (SMU) and one high resolution (HRES-SMU). The device under test (DUT) is placed on the hotplate while three Kelvin probes are used to characterize the electrical properties. Two different electrical test conditions are mainly set in the curved beam switch's electrical characterization. This will be further discussed in the next section. The semi-automatic probe station allows probing view from a closed-circuit television. This set up is similar to the one as described in section 3.1. In the high temperature testing, the probe station stage was modified with a Thermo Scientific hotplate (HP131225Q Cimarec). The temperature range provided by the hotplate ranged from room temperature to 540 °C. The coil or heating element of the hotplate generates significant noise in the device and over shadow some of the switch operation. This noise can be isolated by placing a conductive aluminium foil shield connected to the tester



ground. The overall experiment set up is shown in Figure 5.1. However, the hot plate temperature on the surface may suffer from convection loss. In order to calibrate the real surface temperature, a T-type thermocouple is used to measure the actual temperature of the surface of a dummy device placed on the temperature stage. The measured temperature is calibrated against the setting temperature and the result is shown in Figure 5.2. This curve provides convenient adjustment for actual temperature with reference to setting temperature. The calibration result also provides more accurate measurement in high temperature measurement. The testing of the curved beam device in open air probe station is generally consistent compared to testing in vacuum chamber. As during the encapsulation process, the device is sealed in a hydrogen environment (epi-reactor) and is subject largely to high temperature baking. Most oxygen molecules are removed due to this process. Thus oxidation of the contact interface can be entirely prevented during the measurement.



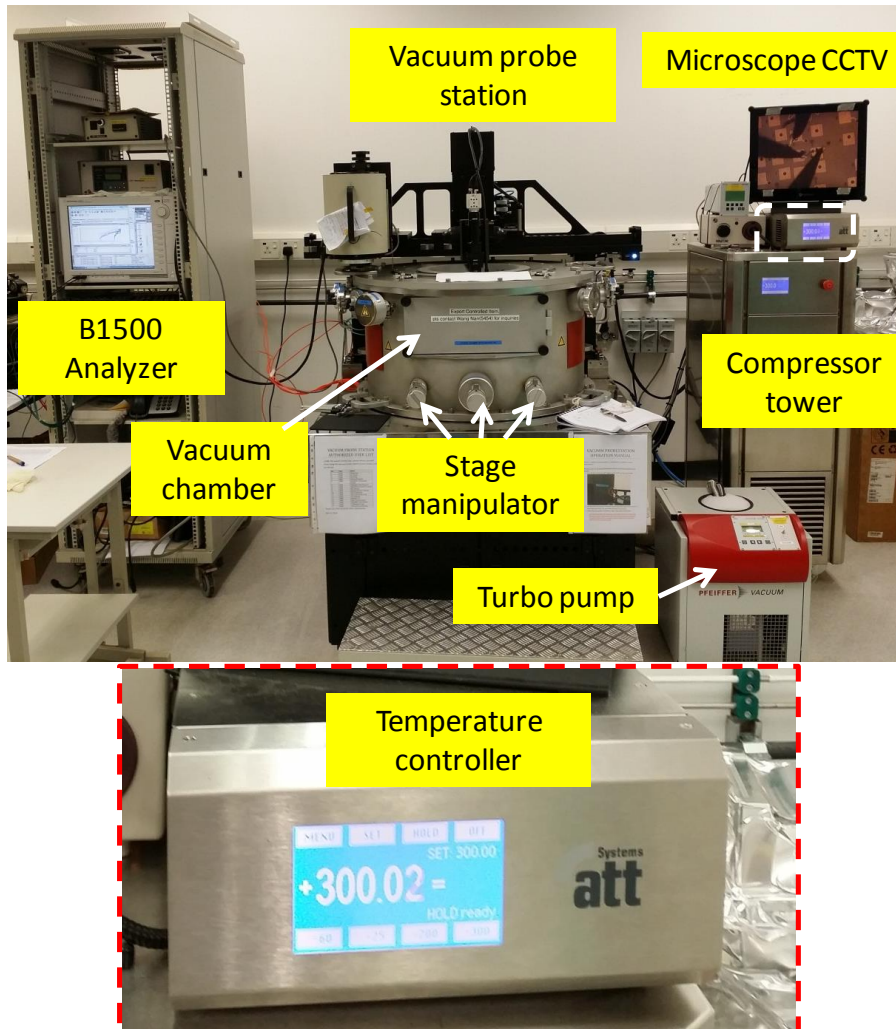
**Figure 5.1: Testing set up of the vacuum encapsulated curved beam switch. The set up includes a probe station (Cascade RBL-6100) equipped with CCTV, a semiconductor analyser (Agilent B1500), the probe station stage modified with a hot plate (Thermo Scientific HP131225Q Cimarec). The Zoom-in image shows the DUT placed under hot plate with temperature setting 500 °C.**



**Figure 5.2: Calibration of surface temperature of the curved beam switch. The measured temperature is regulated to its setting temperature for more accurate temperature setting purpose.**

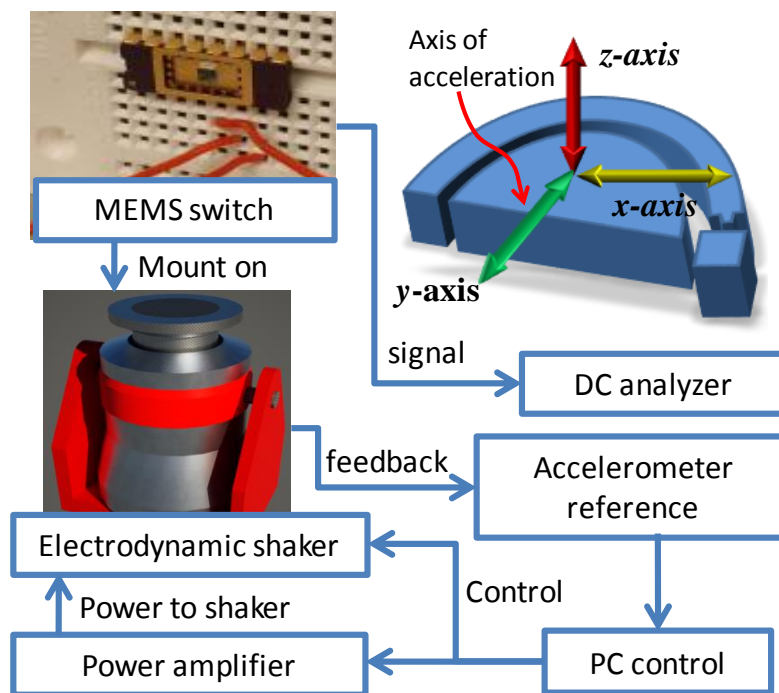
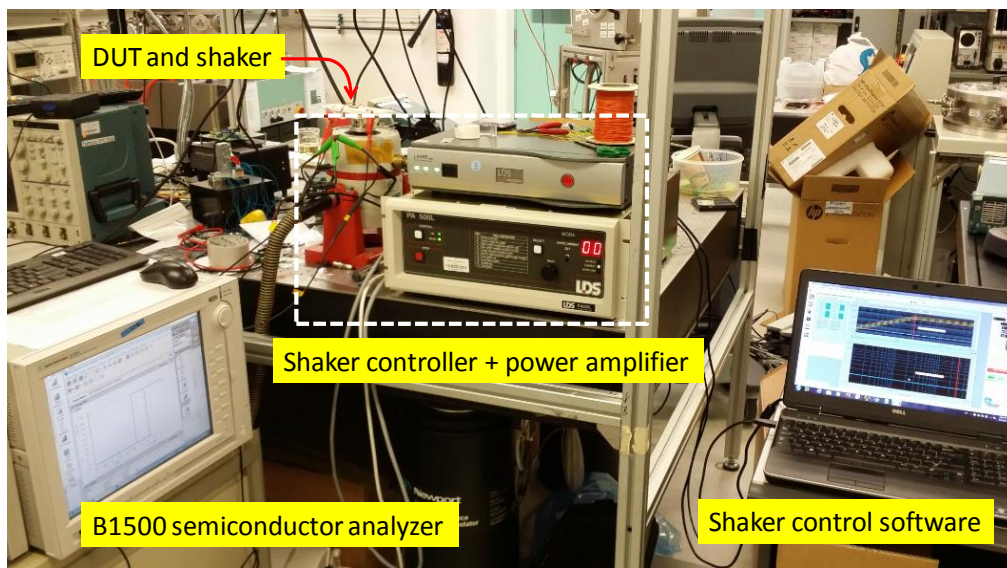
Meanwhile, harsh environment testing from cold to hot temperature can be done in another test chamber equipped with a temperature controller as well as a cooling compressor (Cascade Microtech vacuum probe station, PMV200). The usable temperature of this probe station ranges from -60 °C to 300 °C. During the measurement, the air in the test chamber can be purged and chamber pressure < 1m Torr can be achieved by using a turbo pump. If desired, the enclosed environment of the vacuum probe station also enables nitrogen purged condition, instead of vacuum. The vacuum and nitrogen environment are also meant to protect the interior and hardware of the probe station as the temperature is raised to 300 °C. As for the electrical set up, similar configuration with the unenclosed probe station is used. The overall set up of

the vacuum probe station during test is shown in Figure 5.3.



**Figure 5.3: Vacuum probe station (Cascade Microtech vacuum probe station, PMV200) equipped with an 8” wafer vacuum test chamber, turbo pump and a compressor tower for cooling. Bottom image shows the detail of the temperature controller that can be set from -60 °C to 300 °C.**

The switching delay of the device under 300 °C is measured using Keithley 4200-SCS equipped with one 4225-PMU high speed pulse IV module. The high speed pulse IV module is able to measure both current and voltage in high resolution

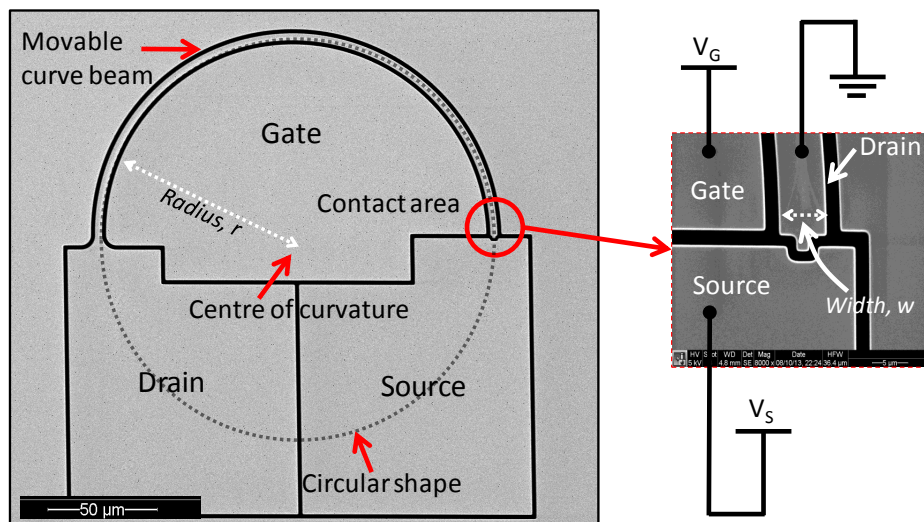


**Figure 5.4: Testing set up of operation high acceleration. The set up comprised of a shaker (Brüel & Kjær LDS V406) together with power amplifier and a semiconductor analyser (Agilent B1500). The same set up is illustrated by the schematics diagram with defined axis of acceleration.**

The Keithley analyzer provides high speed voltage pulsing with simultaneous current and voltage measurement, at acquisition rates of up to 200 megasamples/second (MS/s) with 14-bit analog-to-digital converters (A/Ds),

using two A/Ds per channel (four A/Ds per card). At 40V range, minimum measurement window is 100 ns with 10 ns resolution. Meanwhile, an accelerometer testing is set up to verify the operation of the curved beam switch under high acceleration. The set up comprised of a semiconductor analyzer (Agilent B1500), a shaker (Brüel & Kjær LDS V406) powered by a power amplifier. The curved beam electrical characteristics are measured at different acceleration at fixed frequency. This testing set up is shown in Figure 5.4.

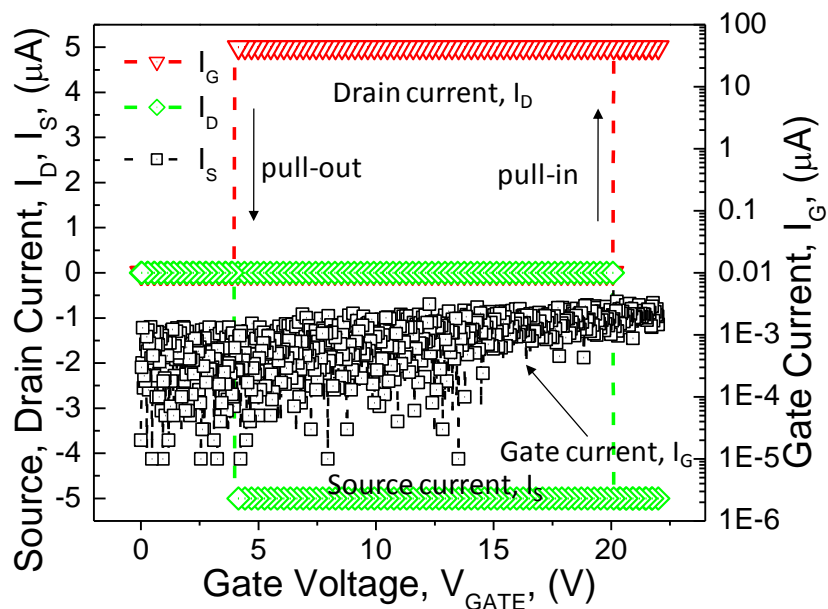
## 5.2 Electrical and mechanical characterization



**Figure 5.5: Scanning electron micrograph (SEM) of a curved beam Si-to-Si MEMS switch. The operation of the switch is shown where  $V_G$  is used to control the actuation with gate terminal and  $V_S$  is used to detect signal from source to drain. Parameter radius,  $r$  and width,  $w$  of beam is shown.**

Similar to the testing requirement presented CHAPTER 3: but more ruggedized switching characterization is performed on the vacuum

encapsulated Si-to-Si switch. Standard switch cycling with more details, the switch is also tested under higher operating voltage and elevated temperature. Figure 5.6 shows an example of a measured typical pull-in and pull-out of a curved beam switch. Gate voltage ( $V_G$ ) is swept from 0 V to 25 V. Pull-in phenomenon is represented by abrupt drain ( $I_D$ ) and source current ( $I_S$ ) rise as indicated during the voltage increment sweep, while pull-out voltage is represented by the abrupt drop in both current during voltage decrement sweep. As compared to two-terminal devices discussed in previous section, three-terminal switch distinctively separate gate control signal from drain and source terminal, resulting in advantages such as low and high power gating and power logic application.

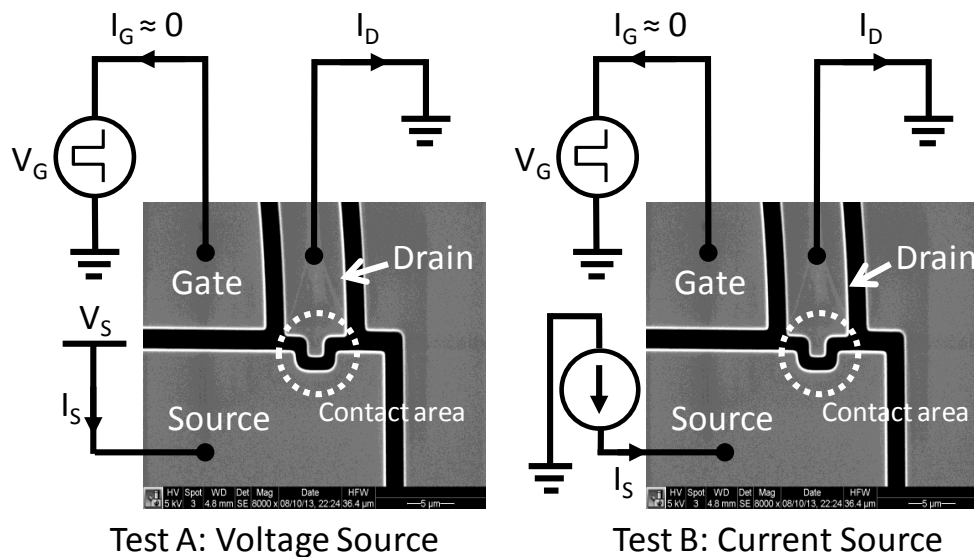


**Figure 5.6: Three terminal testing of  $I_D$ ,  $I_S$ ,  $I_G - V_G$ . Pull-in and pull-out of the curved beam is shown by the near ideal abrupt on-off characteristics at 20 V and 3.8 V respectively. Low noise and power is demonstrate by the low gate current ( $I_G$ ) at pA range at all time during entire sweep.**

Any mechanical or electronics switch has contact lifetime and this is no exception to MEMS switch. In the reliability testing, MEMS switches operating lifetime can be experimentally measured by alternating the switches on-off until it fails. Two different cycling experiment set-ups are carried out to measure the lifetime of the Si-to-Si vacuum encapsulated switch, i.e., voltage source or current source signal can be performed as shown in Figure 5.7. In Test A, a constant voltage source,  $V_S$  is applied between drain and source while gate is biased with an alternating signal,  $V_G$ . This signal continuously turns the device on and off, while drain and source current,  $I_D$  and  $I_S$  are measured in every on and off cycle and is used to determine the contact resistance. Similarly, in Test B, instead of voltage source, a current source,  $I_S$  is applied from drain to source while the potential drop between both terminals is measured. This potential drop between the terminals depicts the contact resistance as the constant current source is constricted by the contact area and surface asperities. The advantage by performing Test B over Test A is excessive heating can be mitigated by  $I_S$  compliance current setting. In order to further investigate the curved beam switch functionality, the switching range is tested at the limit of the achievable temperature from  $-60\text{ }^\circ\text{C}$  to  $400\text{ }^\circ\text{C}$ . Through the understanding of contact's Joule heating, some current compliance settings can be used to enhance the lifetime of the curved beam switch. Important characteristics of the switch are measured and presented in



the later part of the chapter. Lastly the curved beam's reliability under high acceleration is characterized by measuring the switch's operation in acceleration. This is done by placing the curved beam switch on a shaker while the operation is measured by a semiconductor analyzer. The axis of acceleration used in the experiment is in-plane acceleration (y-axis) and out-of plane acceleration (z-axis). Maximum shaker output of 10 g @ 2kHz is verified.



**Figure 5.7: Cycling test set-up for Si-to-Si reliability test. Test A based on voltage source ( $V_S$ ) and current measurement ( $I_S$ ) while Test B based on current source ( $I_S$ ) and voltage measurement ( $V_S$ ).**

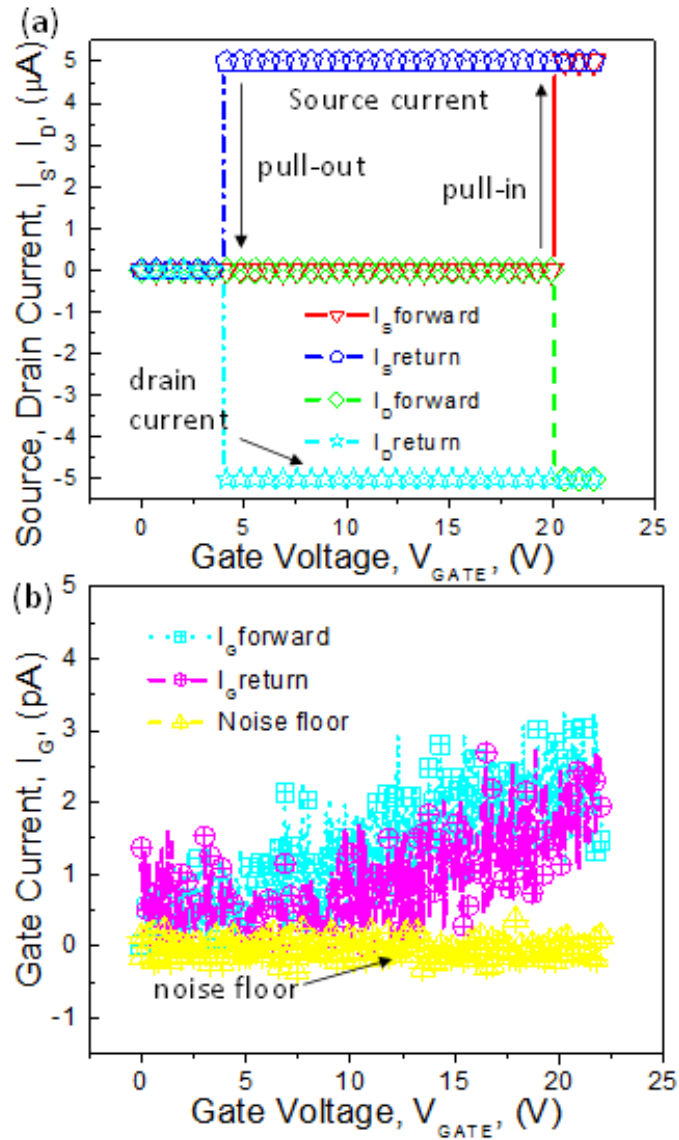
## 5.3 Result and discussion

### 5.3.1 I-V characteristics of a three-terminal electrostatic switch

In I-V characterization, a three-terminal device is demonstrated with low gate current ( $I_G$ ) throughout the measurement (pA range). After pull-in, positive

current will flow as the curved beam contacts source. In contrast, a negative current will flow through source. Pull-out can be measured by sweeping the gate voltage back from 25 V to 0 V. Figure 5.8 shows a measured pull-in and pull-out of a 5  $\mu\text{m}$  thick  $\times$  95  $\mu\text{m}$  radius curve beam switch. In this switch, the pull-in voltage ( $V_{PI}$ ) is 20V and pull-out voltage ( $V_{PO}$ ) is 4.77V. Typical current on-off ratio ( $I_{on}/I_{off}$ ) of approximately  $10^6$  and approximately 6.25mV/decade is demonstrated in this device. The abrupt drain ( $I_D$ ) and source current ( $I_S$ ) indicated by the rise and fall during the voltage forward and backward sweep is the pull-in and pull-out of the curved beam. This is shown in Figure 5.8(a). Such hyper abrupt rise and fall is the feature of a pure mechanical switching. Low gate current ( $I_G$ ) throughout the measurement is shown in Figure 5.8(b). This depicts no contact was made between the curved beam and the gate during the entire voltage sweep. The current flows in all three terminals: drain, source and gate current are measured concurrently, where gate is connected to sweeping voltage, DC bias of 2 - 2.5 V is applied to source and drain is subjected to ground. As compared to two-terminal devices discussed in previous section, three-terminals switch distinctively separate gate control signal from drain and source terminal, leaving uninterrupted signal conditioning between drain and source. Note that gate current measurement is important to measure a three-terminal device, as experimental error may not be detected when device is still able to produce abrupt rise in

current even sometimes when gate is shorted to drain.

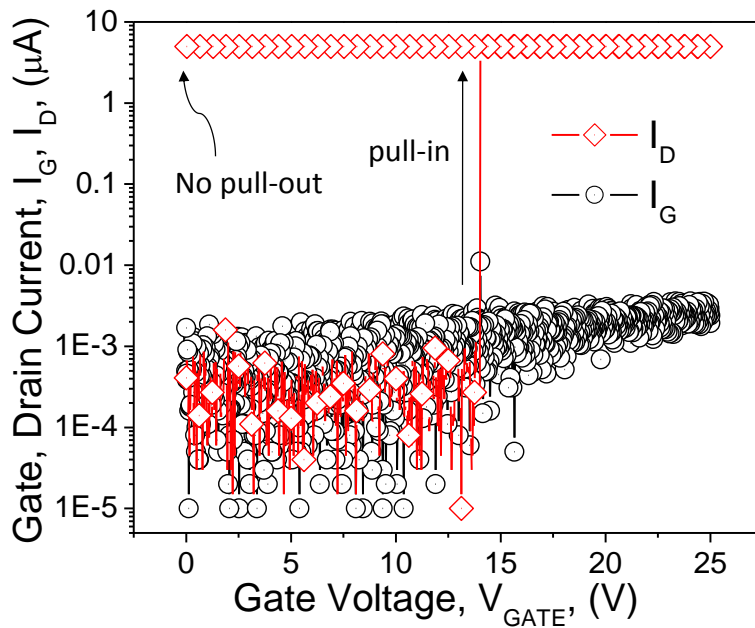


**Figure 5.8: Three-terminal testing of  $I_D, I_S, I_G - V_G$ . (a) Switch turns on during forward  $V_G$  sweep and turns off during return  $V_G$  sweep. (b)  $I_G$  remains low with measured noise floor of the semiconductor analyzer.**

Hysteresis window in pull-in and pull-out voltage is related to the surface adhesion and the imposed electrostatic force. In order to break-off from the contact, the spring restoration force has to overcome surface adhesion and

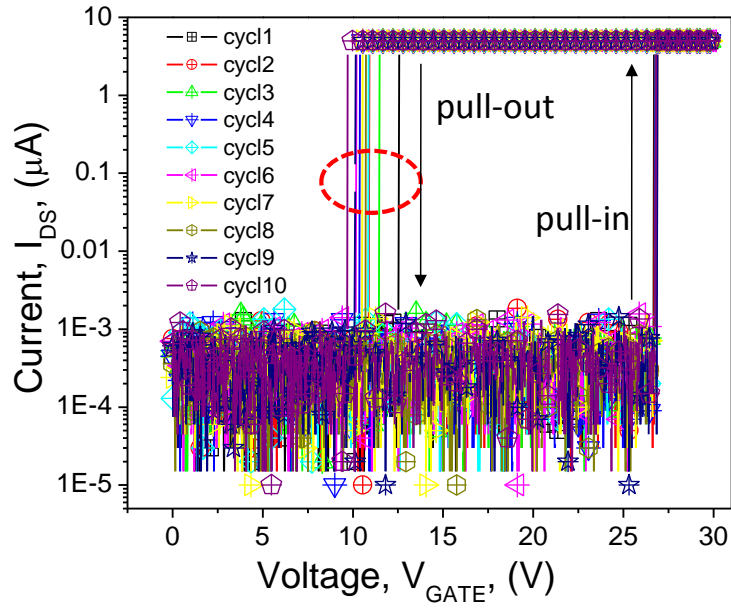
electrostatic force. Trade-off between  $V_{PI}$  and spring constant is inevitable to make the switch behave between a logic and a onetime programmable device. Gap between the pull-in and pull-out can be seen as a measure of the balance between spring constant and surface adhesion force. In other mean, curved beam design can be optimized further to operate at lower voltage however surface contact has to be considered carefully to compensate lower restoration force. Despite one time programmable application can be realized as reported [193], the reliability or memory retention characteristics of such contact based memory is unknown. A three-terminal switch can be designed into low power electronics and all-mechanical logic application for harsh environment applications.

It is noted in these experiments that most low voltage designs ( $< 15$  V) only work once and no pull-out can be detected. Such a result is shown for a  $5 \mu\text{m}$  wide  $\times$   $165 \mu\text{m}$  radius curved beam shown in Figure 5.9. After one pull-in, it is observed that the curved beam is permanently in contact. Although surface adhesion such as van der Waals force and surface charging, the permanent contact may have been caused by micro-welding due to joule heating at the asperity-to-asperity contact, as this effect is consistent with the increasing of the current limit in the source-drain terminal.



**Figure 5.9:  $I_D, I_G - V_G$  of  $5 \mu\text{m}$  wide  $\times$   $165 \mu\text{m}$  radius curved beam. Permanent non-resettable contact is obtained as  $V_G$  sweeps returns to zero, indicating switch remains in contact.**

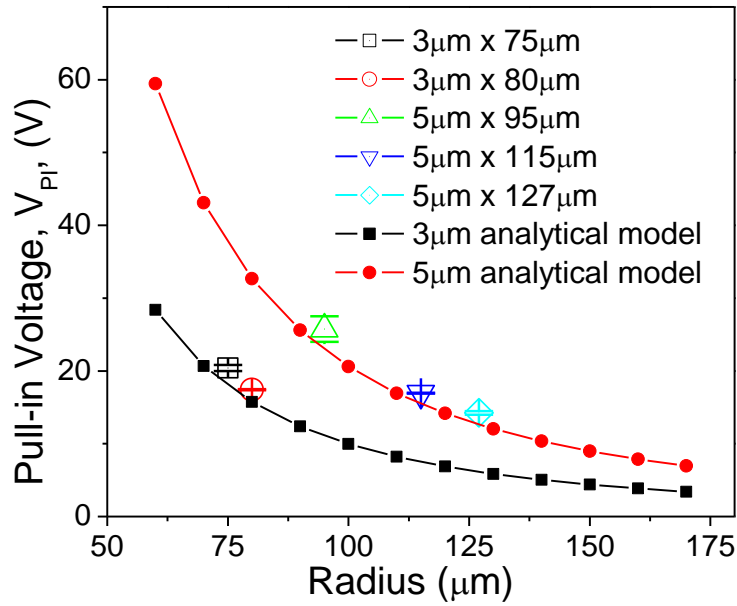
For most devices that actuate at higher voltages, the curved switches produce a consistent  $V_{PI}$  within same device. Ten cycles of repeated gate voltage sweeps are shown in Figure 5.10, indicating a consistent pull-in voltage at approximately 26V for a  $5 \mu\text{m}$  wide  $\times$   $95 \mu\text{m}$  radius curved beam, while the average pull-out voltage is 11.9 V. The gate current ( $I_G$ ) remains low throughout the measurement in pA range, showing consistency of no gate leakage to the curved beam. The observed variation in the pull-out voltage is related to the adhesion force between contact surface of drain and source, which can evolve somewhat due to wear of asperities.



**Figure 5.10: Measurement of ten sweeping cycles.  $I_{DS} - V_G$  sweeping cycles within same device. Pull-out variation is highlighted.**

The analytical model for pull-in voltage from earlier section 4.4.1 is compared with the experiment results. Overall, the pull-in voltage ( $V_{PI}$ ) is agreeable to the analytical model as shown in Figure 5.11, a total of experiment results of 15 devices were tested and compared to the analytical solution. Absolute error of 1V – 3 V is confirmed with the devices tested. In the same figure, it is shown that the pull-in voltage is highly proportional to curved beam length, which can be simply determined by the equation (5.1).

$$l = \pi r \quad (5.1)$$



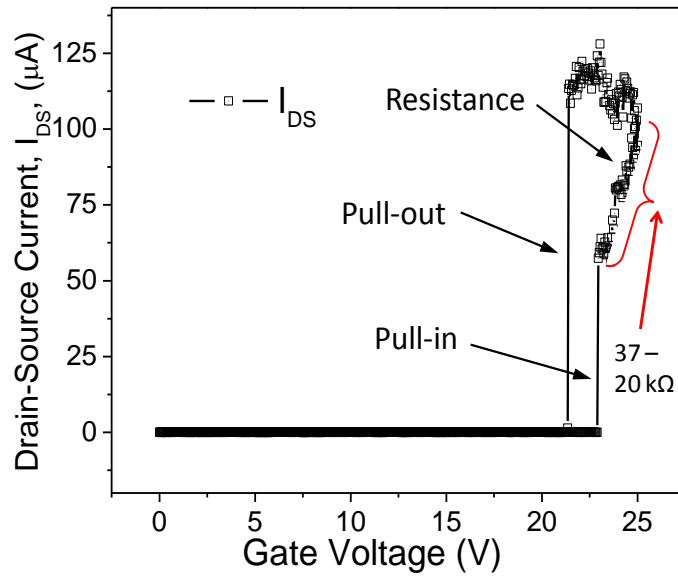
**Figure 5.11: Comparison between measured pull-in voltages ( $V_{PI}$ ) of 3, 5  $\mu\text{m}$  (width) curved beam with various radius versus analytical model. Absolute error 1 – 3 V measured from 15 devices of the same dimension.**

### 5.3.2 Contact resistance

As the curved beam pulled in by the gate to contact the source, drain-source current ( $I_{DS}$ ) flows due to a constant DC bias applied between the two. The amount of current flow depends on the contact resistance. In this testing set up, current compliance is set to the maximum so that the current flow is uncontrolled. Drain-source current ( $I_{DS}$ ) is measured and the measurement is shown in Figure 5.12. Upon contact,  $I_{DS}$  is restricted immediately and rises gradually. This current flow is represented by the slope right after the near infinite abrupt current rise, showing the resistance of the contact. The contact resistance is predominantly determined by the contact asperity and area of contact. Depending on surface condition, the real contact area to apparent

contact ratio can be unpredictable due to some uncertain factors such as operating condition, temperature effect and material property variation. In the curved beam Si to Si contact resistance measurement, the extracted resistance is approximately 10 - 100 k $\Omega$ , depending on the operating condition and environment temperature. Using Figure 5.12, after pull-in, drain source current will come to a region where the amount of current rises gradually with gate voltage. From this current rise, the contact resistance can be extracted. Since the drain source voltage is 2 V, the contact resistance upon contact can be estimated to be 37 k $\Omega$ . As gate voltage continues to sweep, higher electrostatic force imposes more contact area, leading to current rise, this in turn lowers the contact resistance. The extracted resistance before the gate sweeps back to 0 V is 20 k $\Omega$ . Meanwhile, it is important to show that the switch is still able to pull-out after making contact. As gate voltage sweeps back to zero, the electrostatic force decreases, thus the beam is restored to the initial position when the spring restoration force is larger than the electrostatic force. In some cases, pull-out cannot be obtained when the switch's contact is fused after pull-in. This is caused by micro-welding, as a result of Joule's heating when a large current flows through the contact.



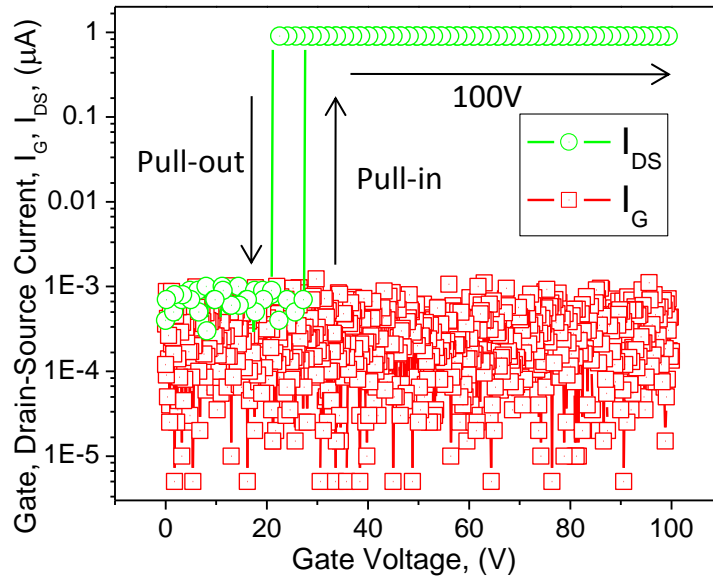


**Figure 5.12: Pull-in and pull-out characteristics of a  $5 \mu\text{m} \times 95 \mu\text{m}$  curved beam switch showing a contact resistance measurement without current compliance.**

### 5.3.3 Curved beam structure robustness against secondary pull-in

High overdriving voltage can impose large contact force to the switch's contacts. Such electrostatic pull-in generates an exponential force over small gate voltage increment and may result in mechanical degradation at the contact surface, causing early fatality in switching. However, the relatively tough hardness of Si material (Mohs hardness: 7) attributed to the mechanical durability in Si-to-Si MEMS switch. In the curved beam contact switch, there is no obvious adverse effect using large gate over drive voltage such as shown in Figure 5.13. As pull-out is still obtainable as the spring restoration force overcomes the electrostatic and adhesion force. Note that the beam does not collapse and contact with gate despite high gate voltage is applied, as gate

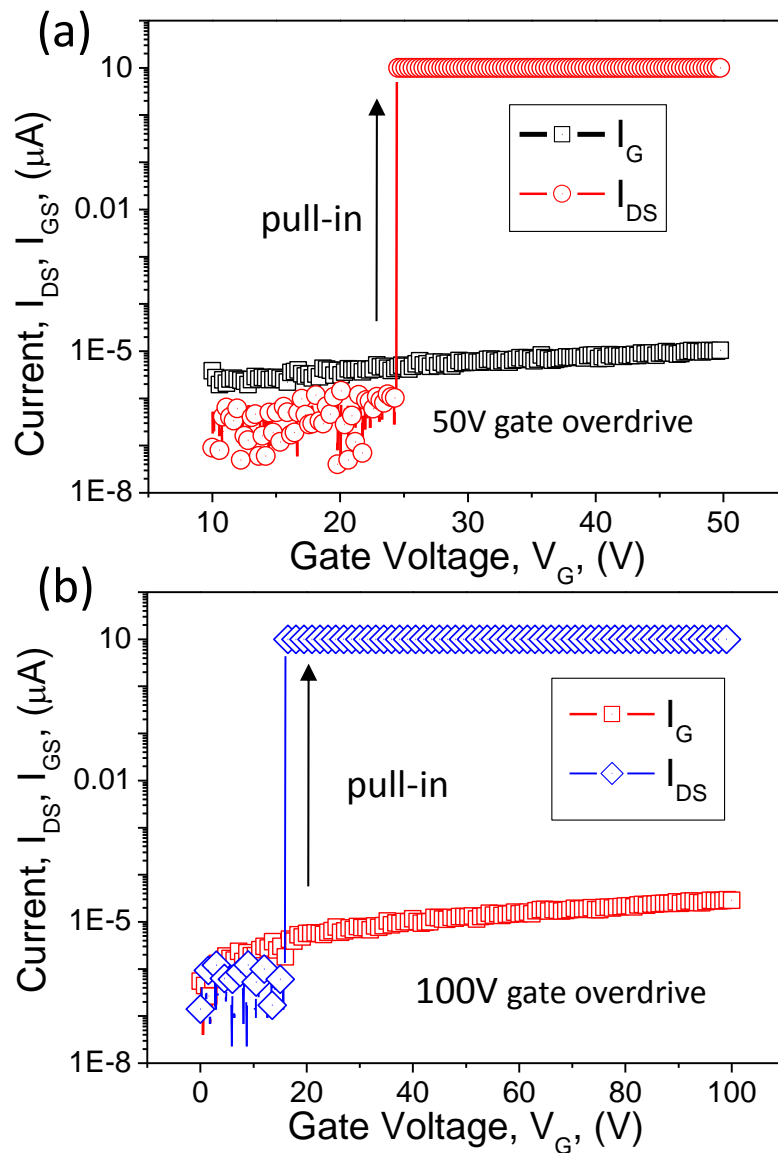
current,  $I_G$  remains low throughout the voltage sweep. This is due to the curved beam design which naturally turns into arch-like structure that is extremely resilient to secondary gate pull-in, thus allowing robust gate voltage control.



**Figure 5.13: Pull-in and pull-out characteristics of a  $5 \mu\text{m} \times 95 \mu\text{m}$  device with voltage over drive from 0 to 100V. Gate current ( $I_G$ ) remain low at pA level during the sweep.**

Figure 5.14 shows the stress testing of the curved beam by overdriving gate voltage ( $V_G$ ) well beyond the pull-in voltage ( $V_{PI}$ ) of two respective devices. While abrupt switching characteristics of drain-source current ( $I_{DS}$ ) equivalent to current on-off ratio ( $I_{on}/I_{off}$ ) of  $10^7$  is observed, the gate current ( $I_G$ ) remains low in pA range throughout the voltage sweep from 10 V to 50 V as shown in Figure 5.14(a) for  $5 \mu\text{m} \times 95 \mu\text{m}$  radius curved beam. The pull-in voltage of this device is 24.5 V. Even higher driving voltage is tested as shown in Figure 5.14(b). No breakdown is observed at gate voltage ( $V_G$ ) sweeps from

0 V – 100 V for a  $5 \mu\text{m} \times 115 \mu\text{m}$  radius curved beam with a lower pull-in voltage of 15.5 V. 100 V is the maximum voltage setting of the semiconductor analyzer.



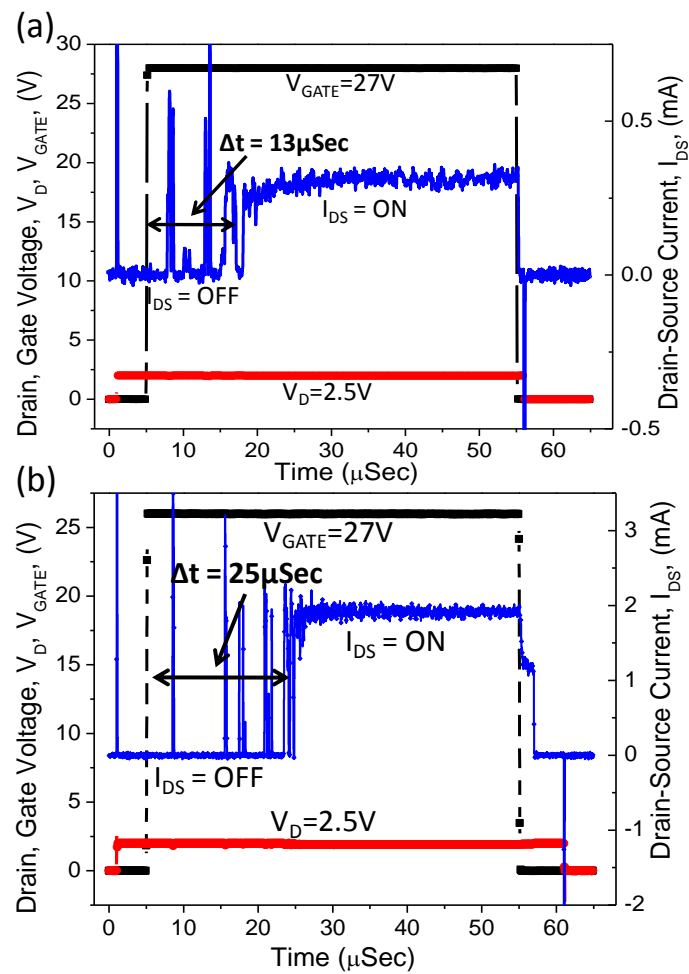
**Figure 5.14: High voltage breakdown endurance. (a)  $V_{PI}$  at 24.5 V of  $5 \mu\text{m} \times 95 \mu\text{m}$  radius beam,  $V_G$  until 50 V (b)  $V_{PI}$  at 15.5 V of  $5 \mu\text{m} \times 115 \mu\text{m}$  radius beam,  $V_G$  until 100 V.**

The robustness in voltage over drive is also reported using an inclined curved electrode with rotation around small hinges. Such hinge placement imposes higher flexibility in horizontal  $x$ -direction and may cause breakdown earlier than a perfect circular beam [194]. There is also a probability that the switch could become stuck with no pull-out detected after a very high gate voltage overdrive.

### 5.3.4 Switching speed

The switching speed of the curved beam switch is extracted through ultra-fast I-V pulse monitoring unit using Keithley SCS-4200 semiconductor analyzer. A fast pulse of 27 V, 100 ns rise/fall time with a 50  $\mu$ s pulse width is applied on the gate bias voltage ( $V_G$ ) to turn on switch while another pulse with lower voltage, 2.5 V, same rise/fall time with larger pulse width of 60  $\mu$ s is applied to the source ( $V_S$ ).  $V_S$  has larger pulse width so that the source voltage encompasses the entire gate voltage pulse, which enables the measurement of entire switch on and switch off in the curved beam. Both the source-drain current ( $I_{DS}$ ) and gate current ( $I_G$ ) are monitored during the pulses. Figure 5.15 shows the real time on-off switching delay of 5  $\mu$ m  $\times$  75  $\mu$ m radius and 5  $\mu$ m  $\times$  95  $\mu$ m radius curved switch respectively. Under vacuum encapsulation, squeeze film damping is considered insignificant in switching delay. The on-off delay of the beam is due to charging, inertia, switch bounce, and finally,

surface adhesion. The calculated spring constant  $K_C$  of the  $5\ \mu\text{m} \times 75\ \mu\text{m}$  radius and the  $5\ \mu\text{m} \times 95\ \mu\text{m}$  radius curved beams are  $58.7\ \text{N/m}$  and  $39.8\ \text{N/m}$  respectively. Between these two examples, a faster switching speed is detected in a shorter curved beam due to higher spring constant, which is consistent with a standard resonant model [195]. Note that there is a few  $\mu\text{s}$  delay switch off in the  $5\ \mu\text{m} \times 95\ \mu\text{m}$  beam. This is probably the delay when the beam breaks the contact, which is held by surface adhesion, surface charges and micro-welding.



**Figure 5.15: Ultra high speed pulse I-V measurement for switching delay. (a)  $5\ \mu\text{m} \times 75\ \mu\text{m}$  radius switch (b)  $5\ \mu\text{m} \times 95\ \mu\text{m}$  radius switch.**

### **5.3.5 Operation range from – 60 °C to 400 °C**

The device's operation range is investigated from -60 °C to 300 °C. This is the setting limit of temperature controller. However, the 400 °C operation is verified during pull-in voltage variation testing and lifetime reliability using the testing set up shown in section 5.1. This study is performed by testing the device in a vacuum probe station (Cascade Microtech PMV200) with a temperature controlled stage. Convective heat loss from the device is considered negligible under the vacuum condition of the test.

#### **5.3.5.1 Pull-in voltage drift**

The thermal effect on the pull-in voltage of the curved beam is related to the thermal expansion of the device material. The reason of the effect is no other than the temperature dependency of Young's modulus in Si material. The material property modifies the mechanical stiffness of the curved beam of the three-terminal switch, resulting changes to the pull-in voltage required to produce beam's instability for critical deflection. The spring constant of the curved beam ( $k_c$ ) is part of the key temperature dependent parameters following the equation (5.2)

$$k_c = k_c(1 + \alpha' + \beta') \times T \quad (5.2)$$

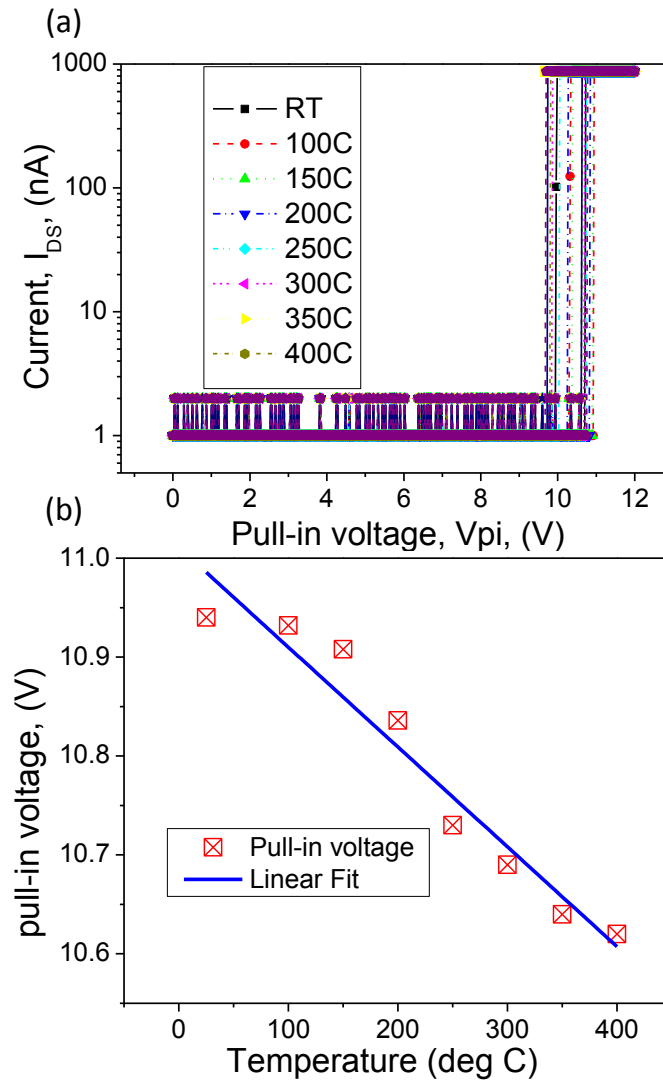
Where  $T$  is the setting temperature,  $\alpha'$  is the thermal coefficient expansion and

$\beta'$  is Young's modulus temperature coefficient of Si respectively. By simplifying equation (4.7) and (5.2), yields a temperature dependent pull-in voltage model as shown below (5.3)

$$V_{PI} = \sqrt{\frac{8}{27} \frac{k_c d^3}{\epsilon A}} \cdot \frac{(\alpha' \beta')}{2\sqrt{(1 + \alpha' + \beta') \cdot T}} \quad (5.3)$$

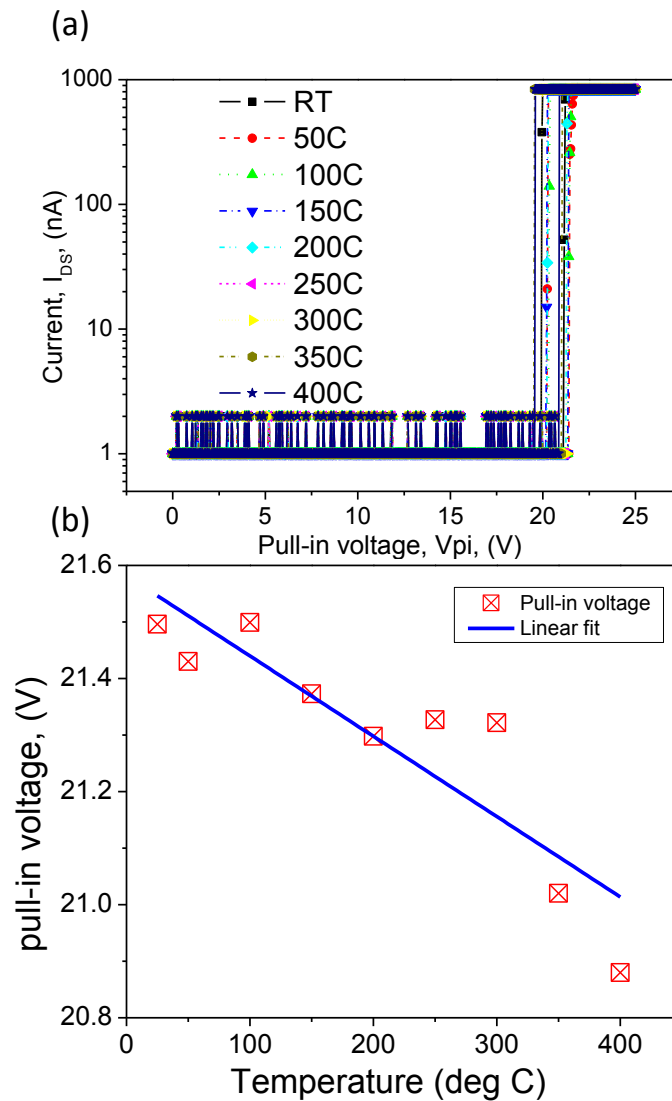
Where  $k_c$  is the spring constant of the curved beam,  $d$  is the separation gap between the gate and the drain,  $\epsilon$  is the relative permittivity of vacuum,  $A$  is the effective capacitive area between gate and drain,  $T$  is the setting temperature,  $\alpha'$  is the thermal coefficient expansion and  $\beta'$  is Young's modulus temperature coefficient of Si respectively. In this fabrication, the curved beam is pure single crystal Si, which is the device layer of the SOI wafer. Considering thermal coefficient expansion of Si ( $\alpha'$ ) =  $3 \times 10^{-6}/K$  and Young's modulus coefficient,  $\beta' = -60 \times 10^{-6}/K$  [196, 197]. The pull-in voltage has a tendency towards decrement due to negative thermal coefficient expansion of Young's modulus. However, the difference between measured and computed values could be attributed to the uncertainties in the exact values of the thermal expansion and Young's modulus thermal coefficients. The pull-in voltage of the curved beam device against different temperature step is measured to verify its temperature dependency. Figure 5.16 and Figure 5.17 shows the pull-in voltage variation with increase temperature step of a  $5 \mu\text{m} \times 150 \mu\text{m}$

and a  $5 \mu\text{m} \times 95 \mu\text{m}$  radius curved beam respectively. Overall the measured pull-in voltage is agreeable with the negative coefficient of Young's modulus of Si. The extracted  $V_{PI}$  drift are 1.36 mV/K and 1.04 mV/K.



**Figure 5.16: I-V measurement of a  $5 \mu\text{m} \times 150 \mu\text{m}$  radius curved beam switch. (a) Pull-in and pull-out characteristics from room temperature to 400 °C. (b) Linear fit of the extracted pull-in voltage yields a  $V_{PI}$  drift of 1.04mV/K.**





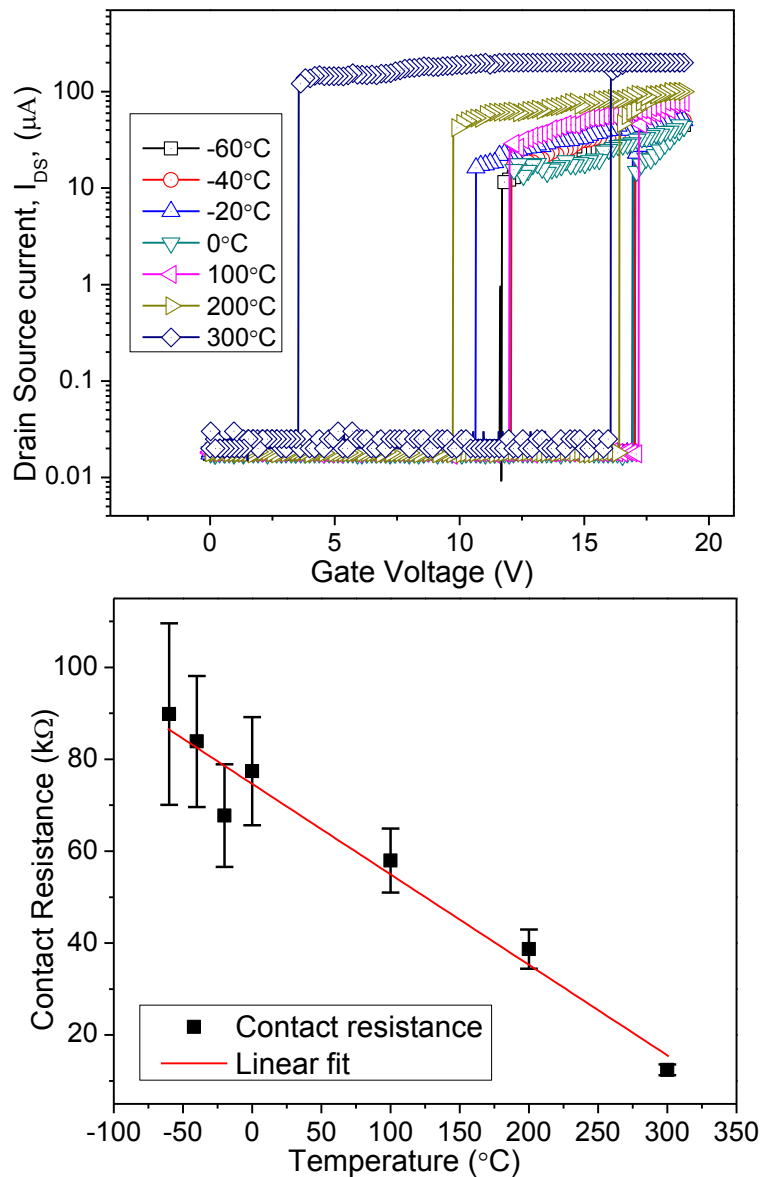
**Figure 5.17: I-V measurement of a  $5 \mu\text{m} \times 95 \mu\text{m}$  radius curved beam switch. (a) Pull-in and pull-out characteristics from room temperature to  $400 \text{ }^\circ\text{C}$ . (b) Linear fit of the extracted pull-in voltage yields a  $V_{PI}$  drift of  $1.36\text{mV/K}$ .**

### 5.3.5.2 Contact resistance drift

First, the curved beam switch's contact resistances are measured from  $-60 \text{ }^\circ\text{C}$  to  $300 \text{ }^\circ\text{C}$ . The gate voltage,  $V_G$  is swept from 0 to 20 V, while the drain-source voltage,  $V_{DS}$  is set to 2.5 V. As the curved beam (source) pulled in to the drain terminal, the drain-source current  $I_{DS}$  rise is detected and measured. The

measurement results at different temperature settings are shown in Figure 5.18(a). In contrast to the result from Figure 5.10, the pull-in voltage varies slightly with increasing temperature. This is due to thermal expansion and the dependency of the Young's Modulus of Si to temperature [196, 197]. In this experiment, the current limit is set to a maximum of 1A, so that the contact resistance can be determined by the linear current rise after the abrupt jump in drain-source current,  $I_{DS}$ . The contact resistance decreases linearly as the drain-source current,  $I_{DS}$  increases from -60 °C to 300 °C. As shown in Figure 5.18(b), the fitted mean variation in contact resistance from -60 °C to 300 °C is approximately -200 Ω/K. The decrease in contact resistance may arise from contact area increases with temperature, due to decreases in the modulus of silicon at elevated temperatures [198, 199]. As a result, larger drain-source current,  $I_{DS}$  can flow through the contact, therefore reducing the resistance. This combination of effects may also leads to faster surface degradation due to increased Joule heating and additional material softening. Under these circumstances, there could be an adverse effect of increased probability of micro-welding at the contact interface, especially at higher temperature. This hypothesis is consistent with the observation of increased hysteresis width between pull-in and pull-out voltages, as the pull-out voltage gradually decreases with each higher temperature step. While the electrical conductivity and beam stiffness are largely unaffected by temperature, changes in the

hysteresis width may indicate growth in contact area, and higher contact adhesion force. This hypothesis is also supported by the observation that the “on voltage” remains constant while the “off voltage” is reduced as the number of cycle increases.



**Figure 5.18: Contact resistance of a  $5 \times 127 \mu\text{m}$  curved beam from -60  $^{\circ}\text{C}$  to 300  $^{\circ}\text{C}$ . (a.) Multiple pull-in  $I_{DS} - V_G$  at different temperatures. (b.) Extracted contact resistance drift (35 measurements) of -196 $\Omega/\text{K}$ .**

### 5.3.6 Reliability of switch versus temperature

A real time measurement was performed using two different test states in the semiconductor analyzer. The first state turns on the device by setting gate voltage above the pull-in voltage by 1 V to ensure that the switch turns on. The second state resets the device by setting the gate voltage to zero bias, turning the switch off. Finally both states can be looped to a desired number of cycles. One cycle consists both on and off test states. Three parameters, the currents ( $I_{DS}$ ,  $I_G$ ) and the bias voltage ( $V_G$ ) were recorded. The source bias ( $V_S$ ) is set to a low voltage of 2.5 V, to provide current signal flow from source to drain. The current compliance of  $I_{DS}$  is set to 5 nA, in order to protect the contact from excessive joule heating due to high current. The on-off cycling conditions are illustrated in Table 5.1.

**Table 5.1 Parameter Settings for On-Off Cycle**

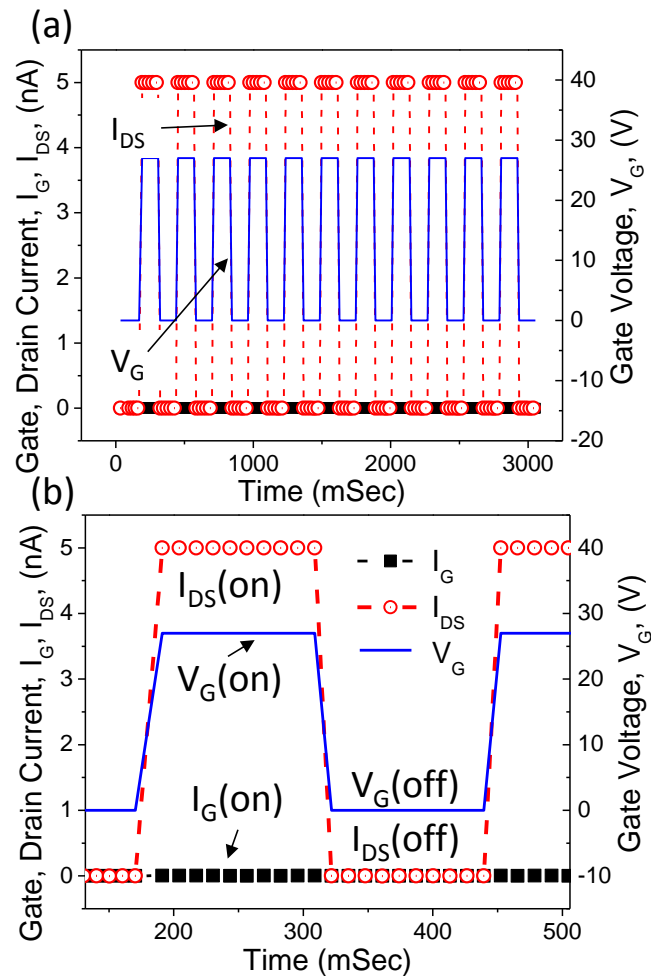
State	Parameters		
	Gate bias ( $V_G$ , V)	Source bias ( $V_S$ , V)	Current limit ( $I_{DS}$ , nA)
On-cycle	$\geq V_{PI} + 1$	2.5	compliance = 5
Off-cycle	0	2.5	compliance = 5

Despite the simple settings, the operational characteristics of the semiconductor analyzer induce delays of a few seconds between loops. Hence measurement of  $10^5$  cycles consumes approximately 100 hours to complete.

Every on-off cycle records 10 samples within sampling interval period of 400 mSec, which translates to 2.5 Hz, which is still far away from the simulated resonant frequency of 111 kHz. Assuming  $\sim 25 \mu\text{s}$  switching delay, the contact and hold time for each cycle is approximately 200mSec. This results in a total contact time of approximately 5.5 hours under ambient temperature condition for  $10^5$  cycles for these tests. Note that all switching cycles were performed under hot switching contact mode, where source signal is biased at 2.5 V (5 nA compliance) during the on-off cycles.

#### **5.3.6.1 At room temperature**

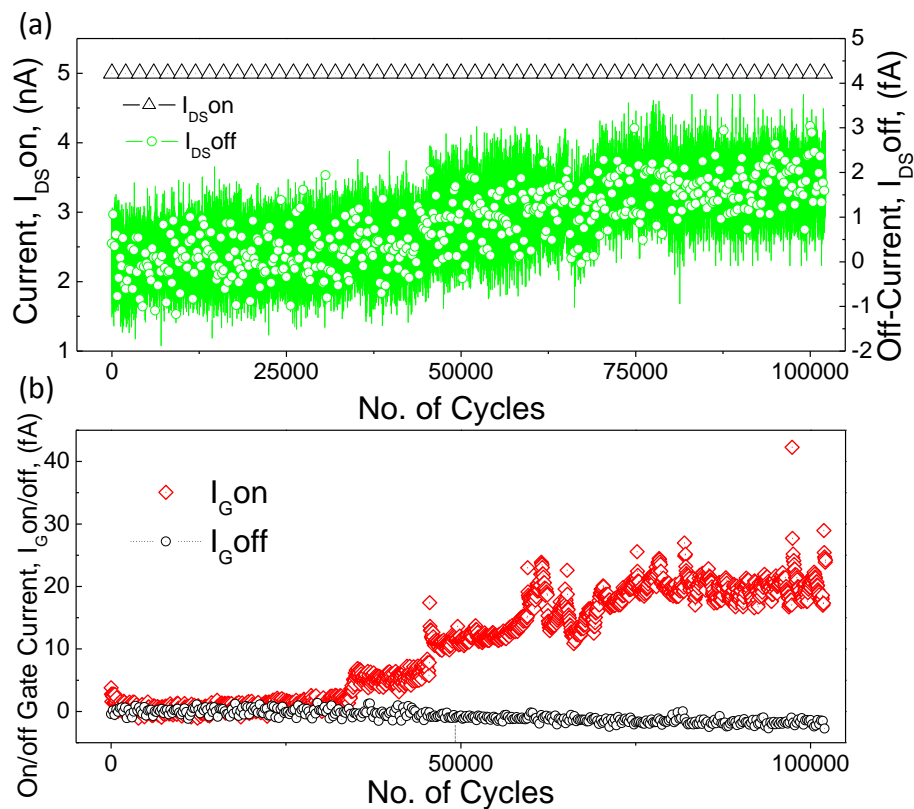
Figure 5.19(a) shows the real time measurement of multiple cycles of a  $5 \mu\text{m} \times 95 \mu\text{m}$  radius beam. During on-state, source-drain current ( $I_{DS}$ ) flow as the curved switch is turned on by gate voltage ( $V_G$ ), which is set 1 V higher than the pull-in voltage ( $V_{PI}$ ). More details are shown in Figure 5.19(b). During off-state,  $I_{DS}$  drops to near zero almost immediately when gate voltage is turned off. It is also important to verify that both on and off gate current remain low in pA range. Overall, the behavior is similar to an ideal three-terminal logic switch switching device.



**Figure 5.19: Real time measurement set-up for on-off cycling test up to  $10^5$  cycles under ambient condition of  $5 \mu\text{m} \times 95 \mu\text{m}$  radius beam. (a) Real time measurement of multiple cycles. (b) zoom-in of one cycle.**

The lifetime of MEMS switches depends on the operating environment. Poor reliability and failure can be caused by factors such as humidity, heat, pressure and stiction. In this work, reliability results of a MEMS switch operating in high temperature environment is demonstrated. One million or  $10^6$  room temperature cycles are performed with each cycle measured. The I-V characteristics of both drain-source current ( $I_{DS}$ ) and gate current ( $I_G$ ) during each on and off cycle can be obtained. Data extracted from the measured I-V

characteristics of every cycle is shown in Figure 5.20. In one cycle, the drain-source current, ( $I_{DS}$ ) reaches 5 nA current compliance limit in the on-state. In the off-state, the leakage current between the drain-source and the gate-source contacts is in the pA range. During experiments up to  $10^6$  cycles, there is some gradual increase in the leakage current between the open drain-source and gate-source contact. This source could include leakage between the electrodes on the surface of the chip, internal leakage due to wear at the contacts.

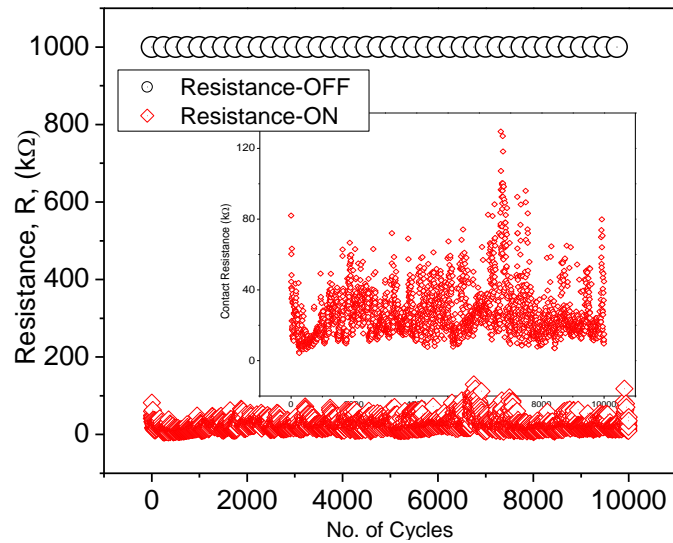


**Figure 5.20: I-V characteristics for  $10^6$  cycles under ambient condition. (a) On-off drain source current ( $I_{DS}$ ) with respect to every cycle. (b) On-off gate current ( $I_G$ ) with respect to every cycle.**

### 5.3.6.2 At higher temperature up to 400 °C

A  $5\ \mu\text{m} \times 95\ \mu\text{m}$  radius device is verified to work at least for  $10^4$  cycles at an elevated temperature of 300 °C. The measured result is comparable to the initial cycling condition of cycling results at room temperature. A  $5\ \mu\text{A}$  current with a large voltage bias is set across source and drain. As the switch turns on, this current flow through the source-drain terminal and the voltage will adjust itself to maintain maximum current of  $5\ \mu\text{A}$ . This voltage bias is measured by the source monitoring unit and the contact resistance can be directly extracted. The current compliance setting is important in this experiment as too high current may cause excessive joule heating and the switch may fail. Figure 5.21 shows the measured contact resistance during the cycling of this device. The contact resistance remains at an average value of  $\sim 28\ \text{k}\Omega$  throughout these tests. The large deviation in the contact resistance is a result of the contact asperity modification after every on-off cycle. Note that when device is turned off, the measured contact resistance of  $1\ \text{M}\Omega$  represents saturation in the measurement. The actual open circuit resistance is known to be in hundreds of gigaohms. This confirms that the switch remains functional up to 10,000 cycles, even when operated at 300 °C. Despite the high deviation in on-resistance, it is still possible to differentiate between on and off state of the device. However, high deviation in on-resistance may disrupt readout and lead to tight threshold control in such devices.

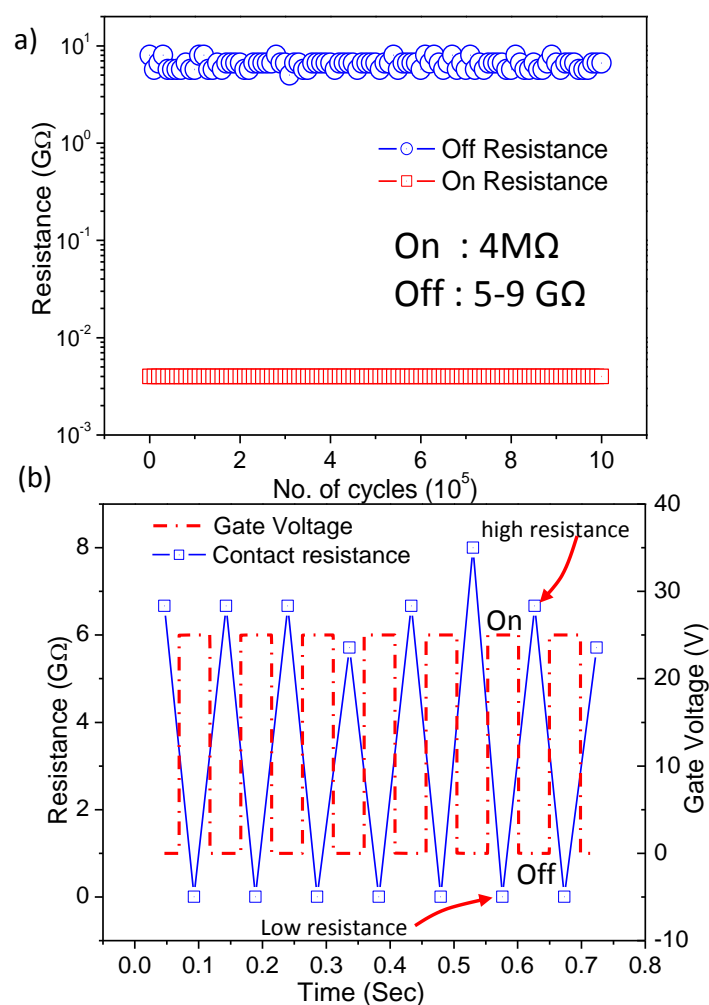




**Figure 5.21: Contact resistance versus no. of cycles under 300 °C elevated temperature. (Inset) Zoom in on the contact resistance during on cycle.**

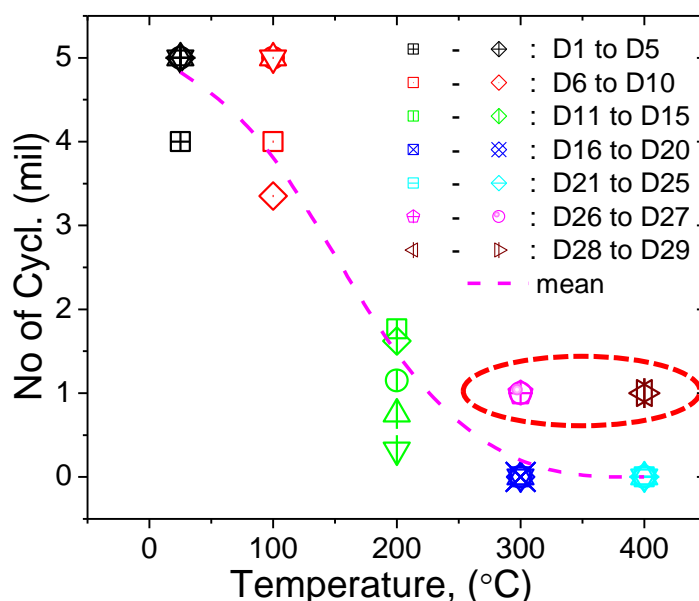
Further testing has to be systematically performed to better analyse the reliability of the vacuum encapsulated curved beam switch. With the testing temperature further elevated to 400 °C. The experiment is repeated with the drain-source current,  $I_{DS}$  current limited to 0.5  $\mu\text{A}$  in order to improve the device's lifetime in higher temperature, instead of a maximum current of 5  $\mu\text{A}$ . In this test, the opportunity for Joule heating is further reduced and the surface degradation at the contact should be slowed, hence achieving higher reliability. Using this current-limited configuration, it is observed that the lifetime of the contact switch can be extended to over  $10^6$  cycles at 400 °C. This result is shown in Figure 5.22(a). Due to the current compliance, now the contact resistance has been increased to 4 M $\Omega$  while the open resistance is depending on the noise level measurement of the analyzer, somewhere in between 5 to 9 G $\Omega$ . Figure 5.22(b) shows the zoom-in of seven on-off cycles

observed as a function of the gate voltage. An inverter function is demonstrated here: As gate turns on the curved beam switch, the resistance drops as current flows through the beam. The reverse happens when the gate turns off and the beam returns to its initial position. Although the current is limited to  $0.5 \mu\text{A}$ , three orders improvement in the stability of the on/off voltage ratio is still obtainable.



**Figure 5.22: (a) One million cycles at  $400 \text{ }^\circ\text{C}$  verified with  $I_{DS}$  current limited to  $0.5 \mu\text{A}$  in log scale. (b) Zoomed-in of device showing seven repeated on-off cycle with respect to gate voltage.**

Joule heating phenomenon is often associated with temperature increase near the contact interface. The phenomenon is further understood and will be presented in next chapter. With the understanding of Joule heating, effective drain-source current compliance is implemented to increase the lifetime of the curved beam switches operating at higher temperature.



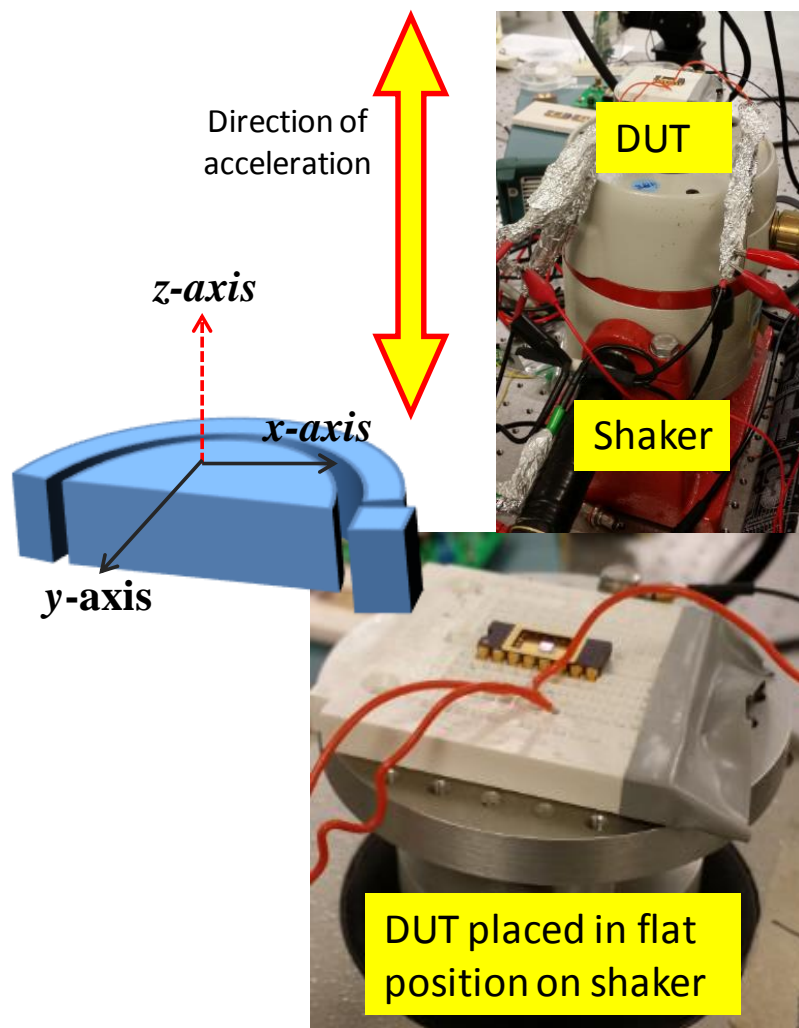
**Figure 5.23: Reliability statistics of twenty-five devices with maximum current flow (1A). By limiting the current to 0.5  $\mu$ A (highlighted), the reliability is enhanced – a lifetime of one million cycles is achieved at 300 °C and 400 °C.**

Lastly, multiple devices are tested and the statistical results are shown in Figure 5.23. A total of twenty five devices named D1 - D25 are tested at room temperature, 100 °C, 200 °C, 300 °C and 400 °C with five devices per temperature. These devices are tested at maximum drain-source current,  $I_{DS}$  (1A) except for the device (D27 - D29) highlighted with a dotted line which

are tested with 0.5  $\mu\text{A}$  current compliance setting. The lifetime of these Si-to-Si switches decreases with higher temperature as expected. The lifetime drops drastically above 200  $^{\circ}\text{C}$  and beyond that, the switch fails after just a few thousand cycles or less at 300  $^{\circ}\text{C}$  and 400  $^{\circ}\text{C}$  under maximum drain-source current flow. However, by limiting the current to 0.5  $\mu\text{A}$ , device D27 – D29 can be cycled for at least  $10^6$  cycles at high temperatures of 300  $^{\circ}\text{C}$  and 400  $^{\circ}\text{C}$  without failure, as shown by the highlighted measurement. With this result, it shows that the reliability of ultra-clean Si-to-Si switches can be enhanced by limiting the current flowing between the contacts. This result also indicates that, in some way, the probability of the defective occurrence may be reduced due to the limited drain-source current,  $I_{DS}$ . In general, the measurement shows that the switch lifetime is highly dependent on the surrounding temperature, drain-source voltage,  $V_{DS}$  and prolonged lifetime at high temperature can be achieved by limiting drain-source current,  $I_{DS}$ . With the above results, the vacuum encapsulated curved beam switch is considered a reliable mechanical switch for rugged electronics application.

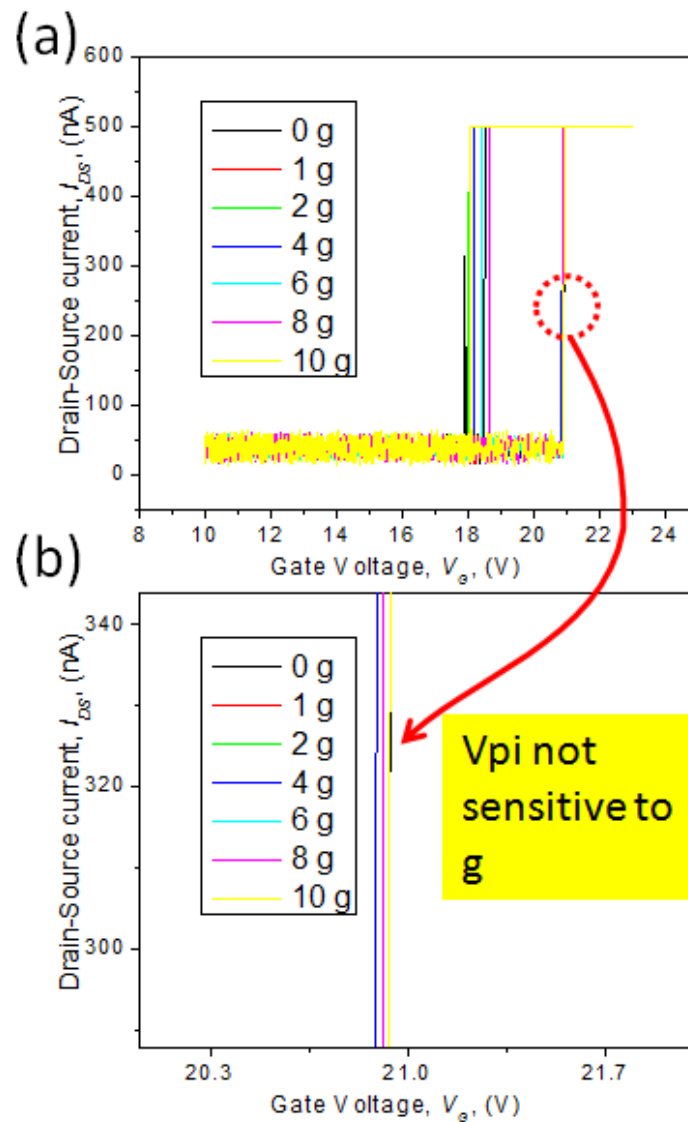
### 5.3.7 Reliability of curved beam switch under high acceleration

The vacuum encapsulated curved beam switch's operation is further investigated by subjecting the device under high acceleration. This is done by performing a standard MEMS accelerometer testing on the device. I-V characteristics of the curved beam switch is measured at different acceleration while the frequency of the acceleration is fixed. First the  $z$ -axis acceleration is applied to the curved beam switch, the position of the device is shown in Figure 5.24. The device is placed flat on the shaker, thus the acceleration is also considered out-of-plane of the device. The curved beam switch is wire bonded so that electrical connection can be conveniently connected using a bread board. The I-V characteristics of a  $3\ \mu\text{m} \times 80\ \mu\text{m}$  radius curved beam switch is measured and the result is shown in Figure 5.25. The pull-in voltage of this device is approximately 22 V. The pull-in characteristics of the switch is unaffected by the out-of-plane acceleration from 1 g to 10 g @ 2kHz in  $z$ -axis direction. As the beam is not flexible in this direction, stable  $V_{PI}$  is expected.



**Figure 5.24: Operation under acceleration shock test with device placed flat on the shaker. The direction of acceleration is along the  $z$ -axis, as represented by the red dash arrow. The electrical connection for gate, drain and source is connected to the semiconductor analyser.**

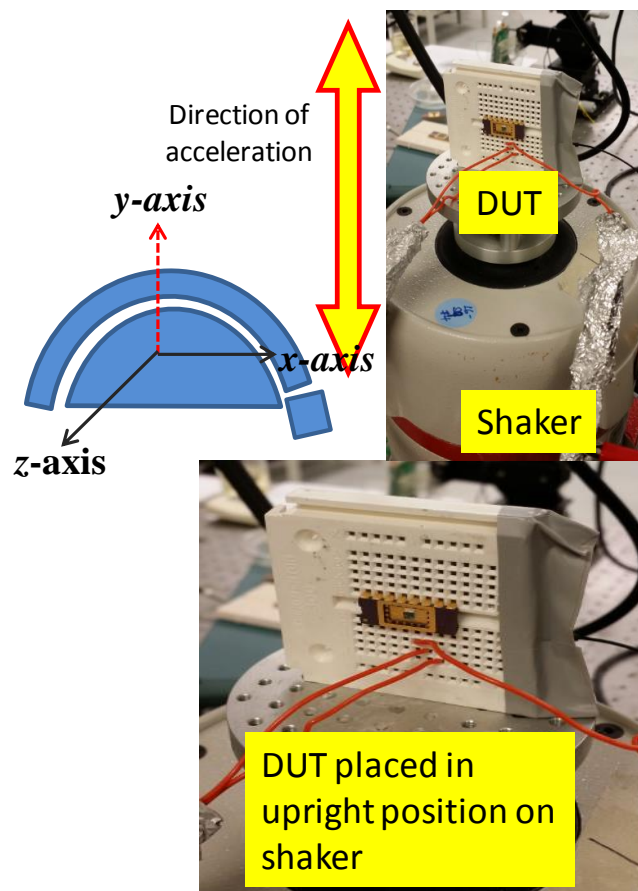
Next,  $y$ -axis acceleration is applied to the device by placing it upright on the shaker. This is shown in Figure 5.26. In principal,  $y$ -axis acceleration is the worst case acceleration to the curved beam switch as the movement of the beam is along the axis of acceleration. The measured I-V characteristic is shown in Figure 5.27.



**Figure 5.25: I-V characteristics of a  $3 \mu\text{m} \times 80 \mu\text{m}$  radius curved beam device under  $z$ -axis acceleration. (a) Consistent pull-in voltage of approximately 22 V at incremental acceleration from 1 g to 10 g @ 2kHz. (b) Zoom-in of the pull-in voltage.**

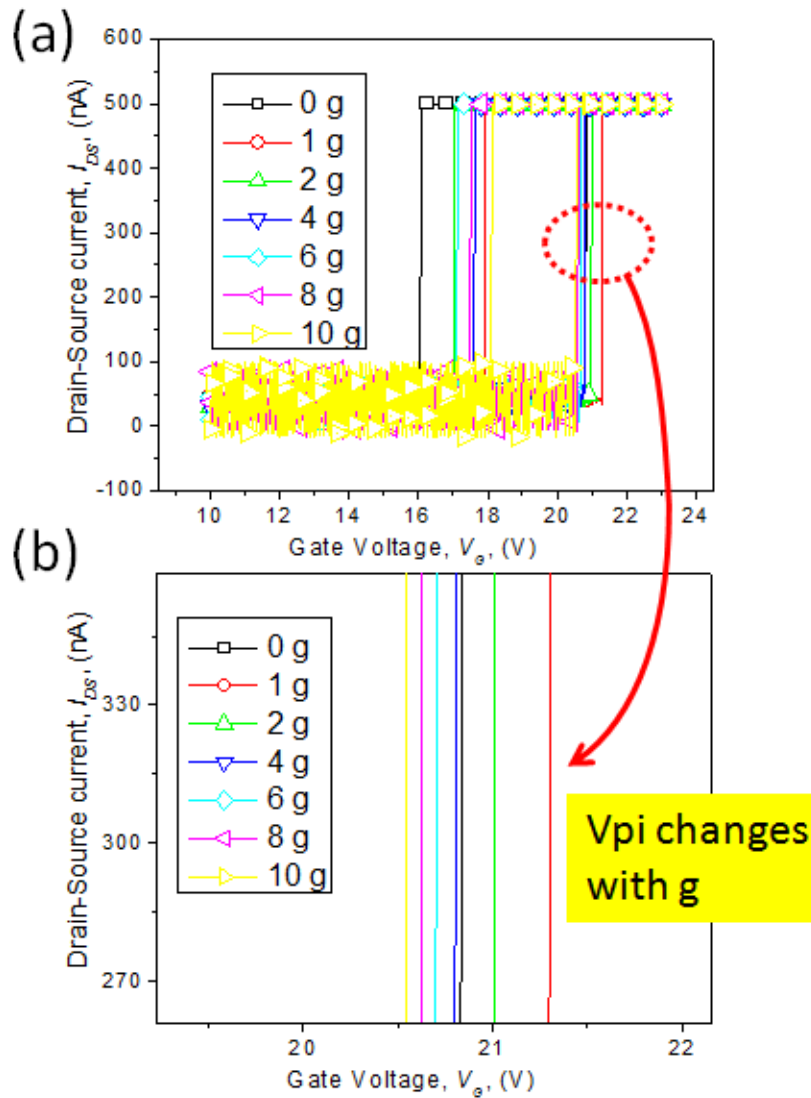
In contrast to the  $z$ -axis measurement, the pull-in voltage now drifts with acceleration. The zoom-in of the pull-in voltage drift is shown in Figure 5.27(a). This phenomenon had been explained by other group that reports on pull-in based MEMS inclinometers [200]. The frequency at resonance of the

curved beam changes while under the effect of an external force. In this case, the initial gap between the curved beam and gate varies according to the applied acceleration, thus affecting  $V_{PI}$ . The curved beam itself acted like a proof mass like a MEMS accelerometer, causing the voltage to drift with the applied acceleration.



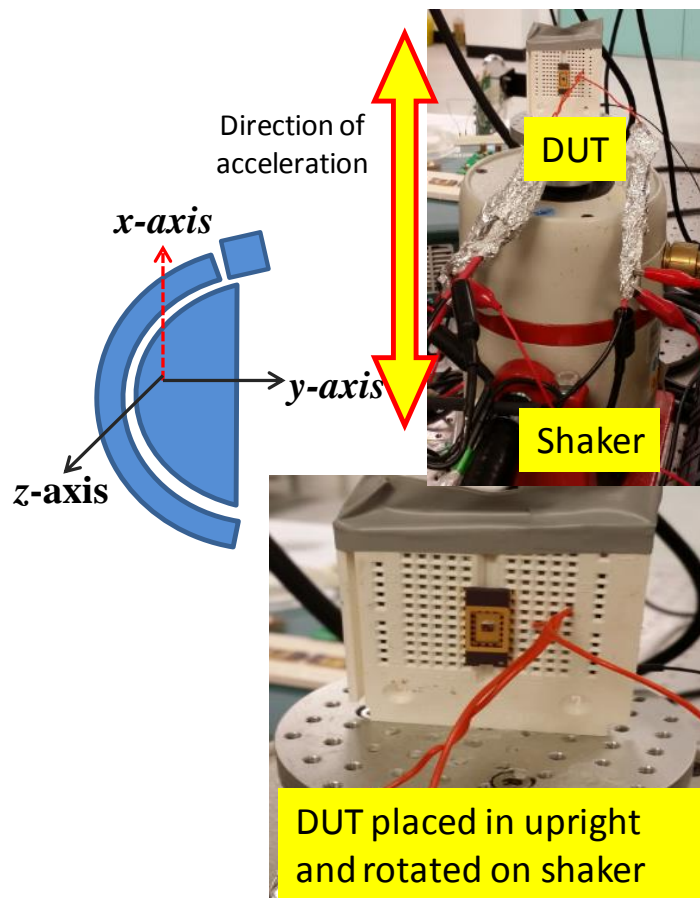
**Figure 5.26: Operation under acceleration shock test with device placed in upright position on the shaker. The direction of acceleration is along the y-axis, as represented by the red dash arrow. The electrical connection for gate, drain and source is connected to the semiconductor analyzer.**





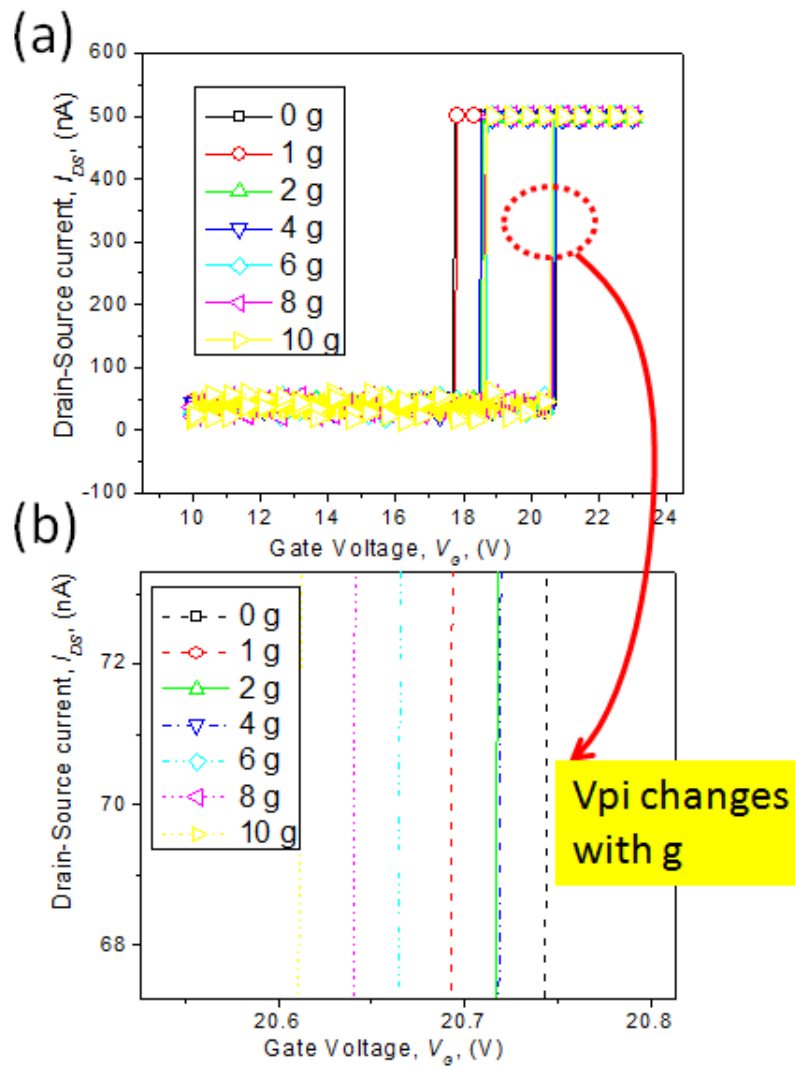
**Figure 5.27: I-V characteristics of a  $3 \mu\text{m} \times 80 \mu\text{m}$  radius curved beam device under  $y$ -axis acceleration (a) Pull-in voltage decreases with increases of acceleration from 1 g to 10 g @ 2 kHz. (b) Zoom-in of the pull-in voltage.**

Lastly, the device is tested under acceleration in  $x$ -axis. The test setup is shown in Figure 5.28. Similar to the  $y$ -axis result, the  $x$ -axis data is shown in Figure 5.29. The device data agrees with the data from  $y$ -data. Since the curved beam is a symmetrical beam with perfect  $180^\circ$  arch. The  $x$ -axis and  $y$ -axis data reflect similar behaviour.



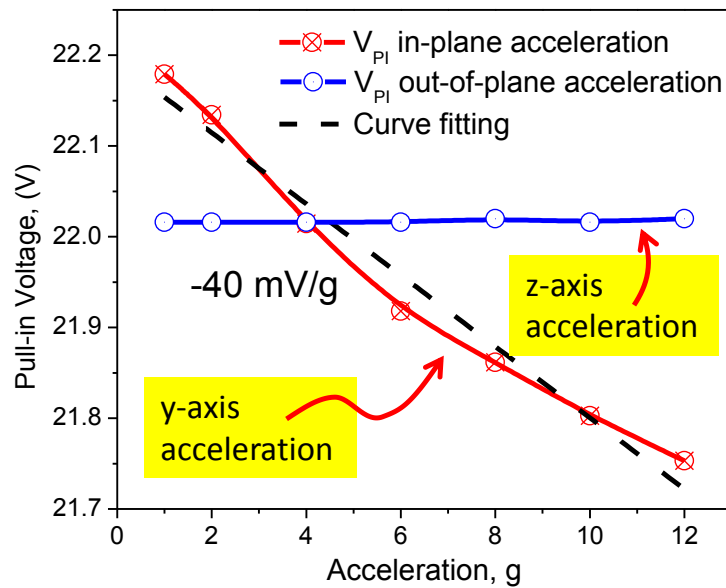
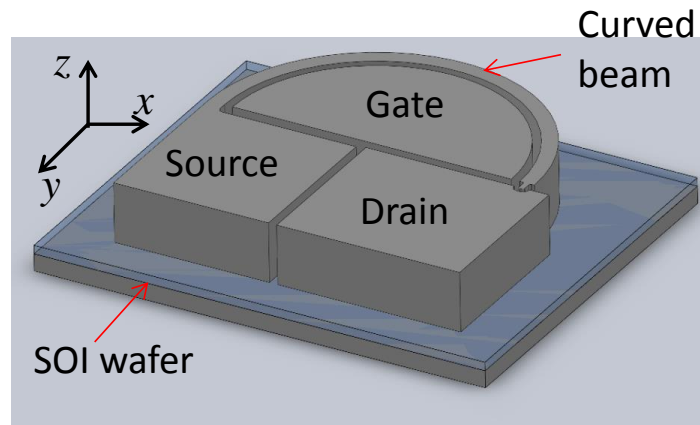
**Figure 5.28: Operation under acceleration shock test with device placed in upright position on the shaker. The direction of acceleration is along the  $x$ -axis, as represented by the red dash arrow. The electrical connection for gate, drain and source is connected to the semiconductor analyzer.**

The measurement result is summarized in Figure 5.30. The switch is unaffected in  $z$ -axis acceleration and  $-40$  mV/g drift in  $V_{PI}$  from 1-10 g is extracted for  $y$ -axis acceleration. This drift is similar to the result of  $x$ -axis measurement. The observed voltage drift is related to the displacement of the beam due to force exerted by the acceleration. Although the obtained result shows negative voltage coefficient to acceleration, there is a possibility of positive voltage coefficient as the displacement of the beam is bi-directional.



**Figure 5.29: I-V characteristics of a  $3 \mu\text{m} \times 80 \mu\text{m}$  radius curved beam device under  $x$ -axis acceleration (a) Pull-in voltage decreases with increases of acceleration from 1 g to 10 g. (b) Zoom-in of the pull-in voltage.**

As the beam acts as a mass, the beam tends to oscillates with the acceleration, resulting in variation of pull-in voltage. Despite voltage drift, the curved beam switch is verified to operate  $< 10$  g. The measurement of switch operation in high acceleration is important to application in aerospace engineering.



**Figure 5.30: Pull-in voltage ( $V_{PI}$ ) stability with respect to acceleration at z-axis and y-axis.  $V_{PI}$  drift in y-axis acceleration of  $-40$  mV/g is extracted from curve fitting using measurement result while no drift is observed in z-axis acceleration.**

## 5.4 Conclusion

In summary, an encapsulated curved beam silicon switching device is designed, fabricated and characterized. Experiment show that the curved beam has potential for mitigation of secondary pull-in, as no breakdown is observed at gate voltage ( $V_G$ ) sweeps from 0 – 100V, thus enabling a robust threshold voltage in switch operation. Micro-second switching delays are

measured, showing fast switching of 13  $\mu\text{s}$  from off to on, and immediate switch off. In reliability study and harsh environmental test, the temperature-dependent behavior of a curved beam Si to Si contact switch, sealed in an ultra-clean environment is thoroughly investigated. The switch is known to work under room temperature for at least  $10^7$  cycles. Measurement is done and analysis is shown to explain the temperature dependency of the contact resistance and the potential difference across the contact, drain-source voltage. In order to prevent excessive Joule heating, limiting the drain-source current,  $I_{DS}$  current is shown to prolong the lifetime of such switches at high temperature. With the understanding of Joule heating, at least  $10^6$  cycles of operation has been successfully verified at 300 °C and 400 °C. Meanwhile, the operation of the curved beam switch is confirmed uninterrupted under high acceleration shock test of 10g@2kHz, which depicts that the curved beam switch is reliable under high acceleration. Such experiment measurement is reported for the first time for N/MEMS switches. This measurement is important for device operating under high acceleration, i.e.: miniaturized satellite, rocket launch. The high reliability could be valuable for harsh environment electronics such as automotive, aerospace and down-hole applications.

## **CHAPTER 6: Failure Mechanism and Analysis**

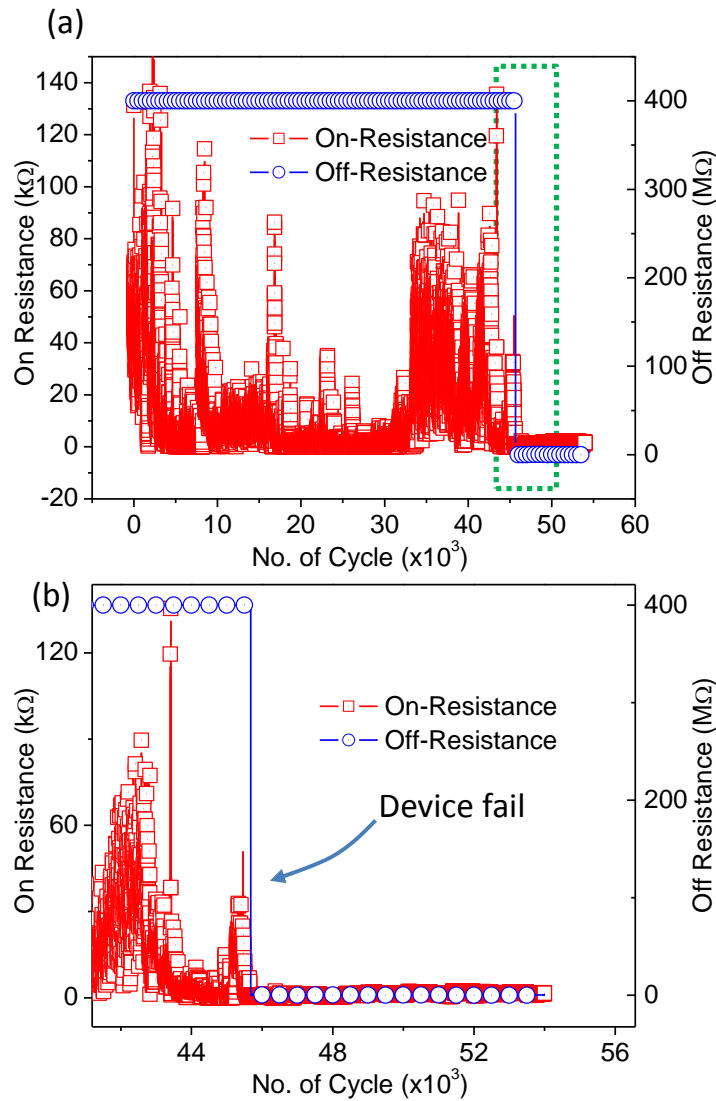
### **6.1 Joule heating phenomenon at contact interface**

To further understand the failure mechanisms of the Si-to-Si contact interface, post-test analyses as well as additional experiments are carried out. The aim of this investigation is to find out the physical degradation and contributing factors that cause failure in Si-to-Si contact switch. This work is also important to other similar works as N/MEMS switches relies on mechanical contact.

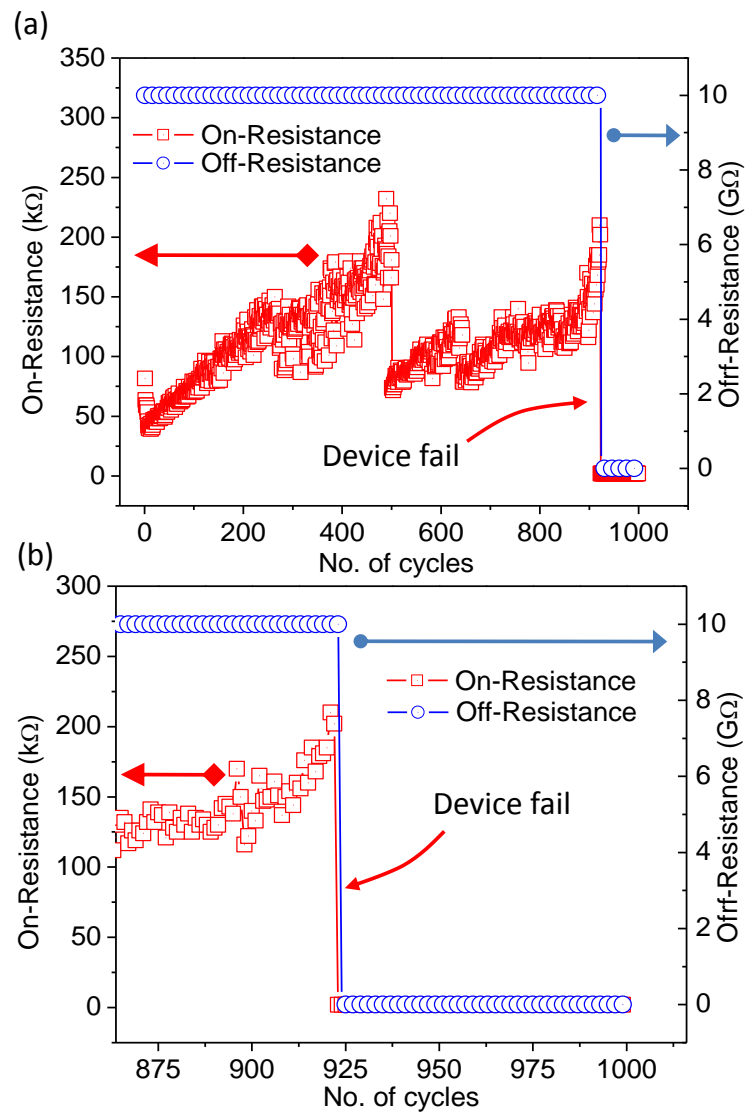
#### **6.1.1 Failure in N/MEMS Si-to-Si switch**

In the reliability test experiments, the drain-source voltage,  $V_{DS}$  is set to 2 V, the drain-source current,  $I_{DS}$  is limited to 1 A (maximum current compliance), and continuous on-off cycling of the switch is explored at a high temperature of 300 °C. In this experiment, the switch operated up to 47 thousands cycles before failure as shown in Figure 6.1(a). A zoom-in of the plot in Figure 6.1(b) shows that the switch failed to disconnect during the off cycle. The experiment is repeated with a similar device at 400 °C. This time, the lifetime of the switch is even lower, merely 923 cycles are achieved. The result is shown in Figure 6.2. This failure mode indicates that the beam is permanently in contact with drain. It is also note that, in these high-temperature Si-to-Si contact tests,

the contact resistance rises gradually with number of cycles and then, this resistance falls and gradually rise intermittently, which could arise from contact modification and roughening of the contact surface.



**Figure 6.1: Contact resistance versus number of cycles at 300 °C with maximum current compliance (1 A) (a) Approximately 47 thousand cycles achieved for Si-to-Si switch encapsulated in vacuum. (b) Zoom-in to the last few cycles showing that device fail.**

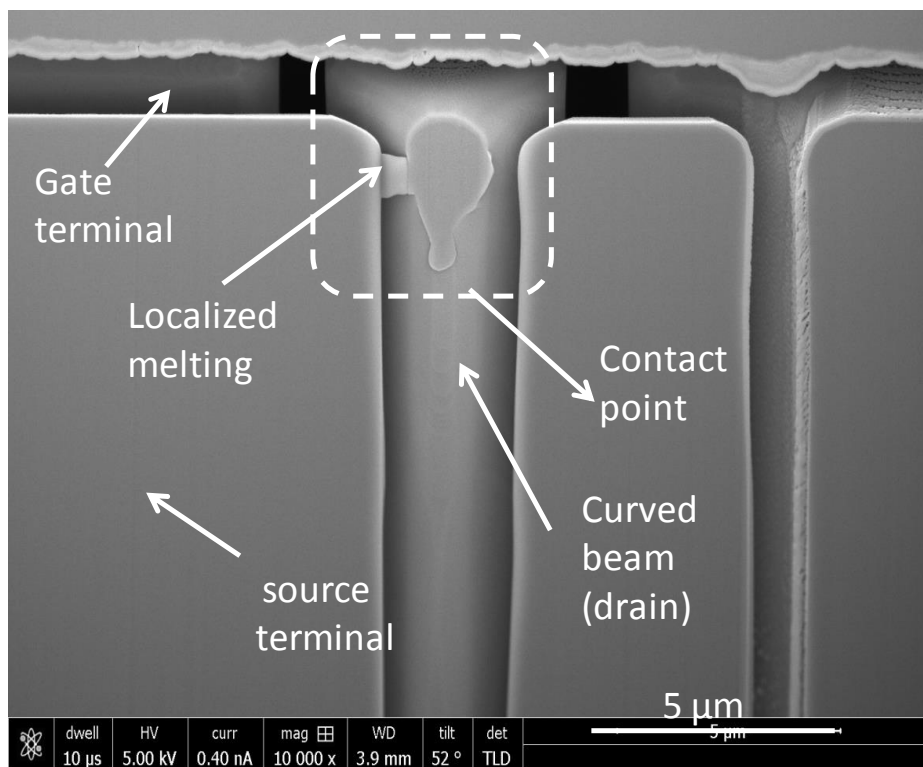


**Figure 6.2: Contact resistance versus number of cycles at 400 °C with maximum current compliance (1 A) (a) Merely 923 cycles achieved for Si-to-Si switch encapsulated in vacuum. (b) Zoomed-in view of device that failed abruptly at 923 cycles.**

In order to investigate the physical activity of the Si-to-Si contact switches sealed with the epitaxy poly-silicon encapsulation process, a focused ion beam is used to mill through the cap and device layer to a depth of nearly 100 μm, and cross-section scanning electron microscopy is used to inspect the interfaces in search for the failure mechanism. The SEM inspection is shown



in Figure 6.3. From the SEM, it is shown that the contact point is micro-welded to one of the terminal. It is known that excessive Joule heating in N/MEMS switches can cause catastrophic failure. Hence the temperature near the contact interface has to be lower than the melting temperature of the material to ensure longer operating lifetime.

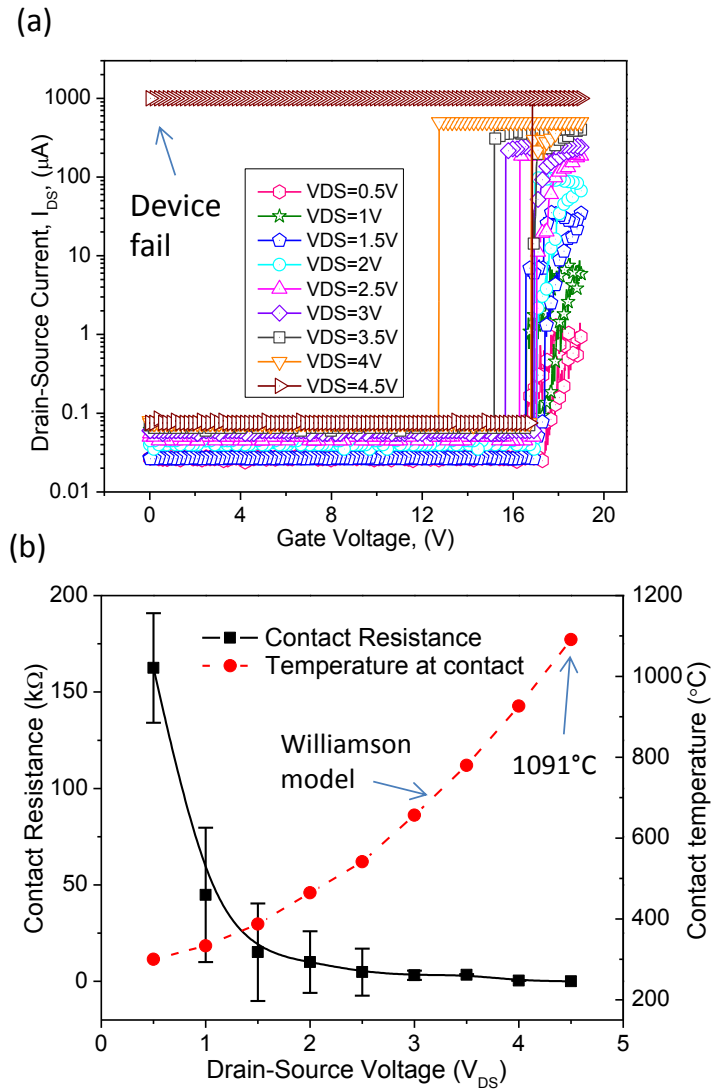


**Figure 6.3: Focus ion beam milling reveals cross-sectional view of a failed device after sudden failure at high temperature cycling**

### 6.1.2 Contact temperature

The role of temperature at the contact is further investigated since excessive Joule heating can cause catastrophic failure. To study the temperature at contact, the drain-source current ( $I_{DS}$ ) change, is measured with respect to different drain-source voltage ( $V_{DS}$ ). The increase in current flow due to higher drain-source voltage can be leveraged to find out the maximum current the device can withstand. To do this, the gate voltage sweep experiment is repeated with drain-source voltage,  $V_{DS}$  steps at 0.5 V until device failure is observed. This experiment is done in room temperature hence any temperature dependent parameter is due to the temperature change near the contact of the Si-to-Si switch. The drain-source current,  $I_{DS}$  measurements at different  $V_{DS}$  are shown in Figure 6.4(a). Increasing the drain-source voltage,  $V_{DS}$  leads to higher drain-source current,  $I_{DS}$  through the contact, resulting in increased heating and lower contact resistance. The amount of current flow is much higher compared to that caused by elevated temperature. At  $V_{DS}$  of 4.5 V, the drain and source are permanently fused in contact and no pull-out voltage is observed. The extracted contact resistance decreases exponentially with respect to the drain-source voltage, as shown in Figure 6.4(b). These results show a more severe effect compared to measurements of contact resistance change as a function of the operating temperature of the device. The decrease in contact resistance with increases in drain-source voltage ( $V_{DS}$ ) is also a

result of Si softening at higher temperature, which induces larger contact area and higher flow of current, which is similar to the effect of increasing temperature. However, in these tests, the effect may be more severe as the drain-source current flow,  $I_{DS}$  is constricted through A-spots. These “A-spots” are modeled as tiny contact areas on the surfaces between a pair of solid electrodes through which almost all of the electric current flows. The current density flowing through these A-spots can be a few orders higher than the average current density between contacts [201, 202]. Additional heating, softening and localized micro-welding may arise as a result of higher temperature near the contact [203]. The result shows that the drain-source voltage,  $V_{DS}$  is a greater factor than ambient temperature increment, probably because the local temperature increases are more important than the temperature of the external environment in these studies.



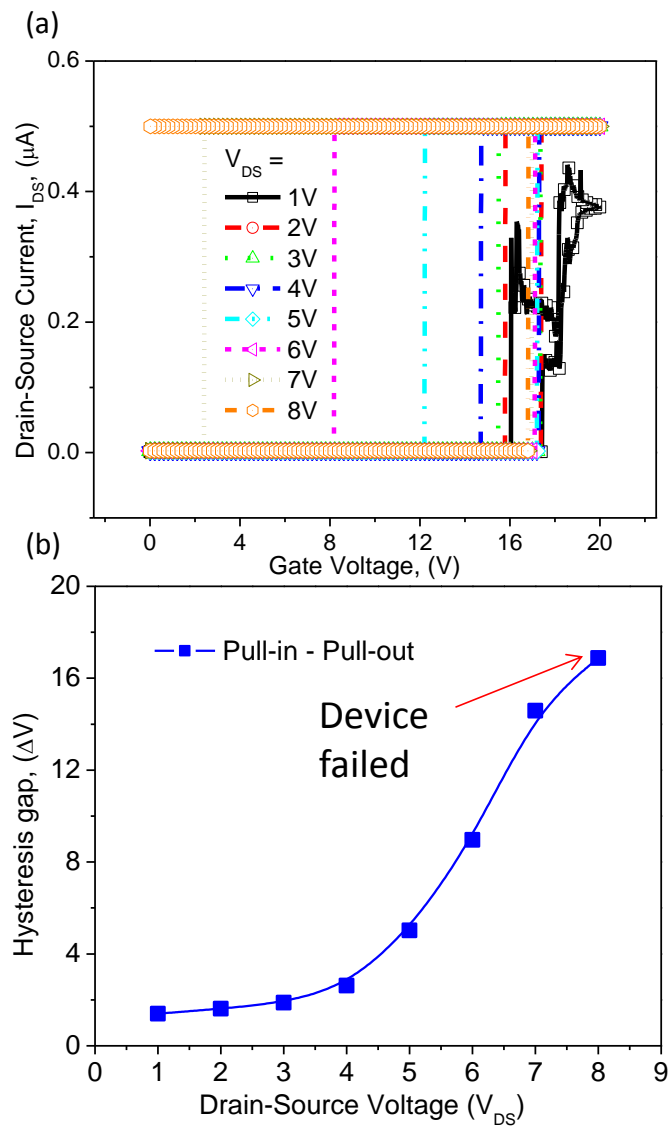
**Figure 6.4: Dependency of the contact resistance on  $V_{DS}$  bias from 0.5 V to 4.5 V (a)  $I_{DS}$  -  $V_G$  at different  $V_{DS}$  where device failed at  $V_{DS} = 4.5$  V. (b) Contact resistance (45 measurements) and calculated contact temperature versus drain source voltage,  $R_C$  -  $V_{DS}$ .**

The temperature near the contact due to Joule heating can be approximated using the Williamson-Bowden Model as shown in equation (6.1) [204].

$$U^2 = 8 \int_0^{T_{\theta}} \lambda \rho d\theta \quad (6.1)$$

Where  $U$  is the potential difference between the contact points,  $\lambda$  is the thermal conductivity of Si,  $\rho$  is the resistivity of the isotropic material and  $T_\theta$  is the maximum temperature due to Joule heating between contacts. The maximum Si-to-Si contact temperature versus potential difference is plotted in Figure 6.4(b). At drain-source voltage,  $V_{DS} = 4.5$  V, the maximum temperature predicted in this model is almost 1100 °C. Although this temperature is lower than the melting temperature of Si at 1414 °C, it is believed that the actual temperature at some portions of the contact region may not be accurately modeled because of the complexity of the contact. The actual temperature of the A-spots could be higher than predicted in this model, which would cause more severe micro-welding. This condition could be enhanced by the fact that the heavily doped Si has lower melting temperatures by 150 K [205]. Note that the Si here is in-situ doped with a high impurity concentration of  $6 \times 10^{19}$  Phosphorus ions/cm<sup>3</sup>. At least ten devices were tested and all devices show the same failure at drain-source voltage,  $V_{DS}$  between 4 to 5 V. By understanding the temperature near the contact interface, the reliability of the device can be improved by limiting the current that flows through the contact. In this way, the contact degradation is lowered by reducing undesired excessive Joule heating. Figure 6.5(a) shows sweeps of the gate voltage with drain-source current,  $I_{DS}$ , limited to 0.5  $\mu$ A. The drain-source voltage is increased in 1 V steps until the device fails. We show that a higher drain-source voltage,  $V_{DS}$ , of

up to 7 V can be attained before the device fails, which is 3 V more than the in our previous section. After drain-source current,  $I_{DS}$  reaches current limit, the drain-source voltage,  $V_{DS}$  remain constant through the sweep until pull-out happens ( $V_{DS} = I_{DS} \times \text{contact resistance}$ ).

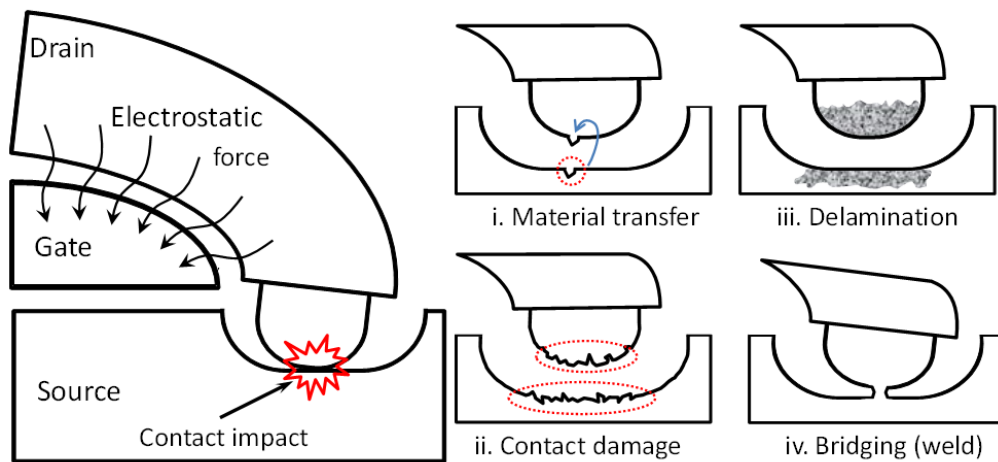


**Figure 6.5:** (a.)  $I_{DS} - V_G$  at different  $V_{DS}$  with  $I_{DS}$  limited to  $0.5\ \mu\text{A}$ . The device fails to pull out at  $V_{DS} = 8\text{ V}$ . (b.) The hysteresis gap increases as drain-source voltage increases.

In other mean, the actual drain-source voltage at the contact is lower than the setting drain-source voltage. The hysteresis width  $\Delta V$  is shown in Figure 6.5(b). As the drain-source voltage increases, the width between pull-in and pull-out voltage widens. The increase in the hysteresis width shows that a larger adhesion force is present. The switch fails when it does not pull out even when the gate voltage is zero. Here, the largest hysteresis gap of 14.1 V is achieved at 7 V before the device fails at 8 V. This result also indicates that contact defects caused by Joule heating such as micro-welding and material transfer can be reduced significantly by limiting the drain-source current.

### **6.1.3 Failure mechanism**

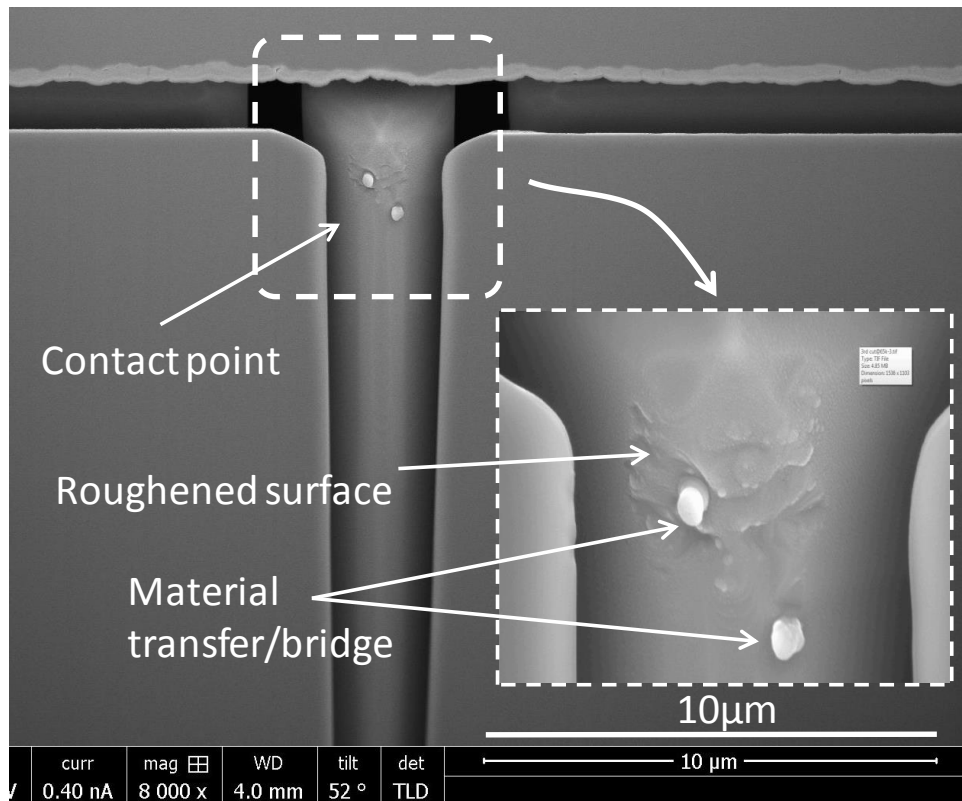
Contact degradation has been explained by other researchers as shown in Figure 6.6. In which contact material transfer and contact damage can lead to permanent bridging at the contact interface [162, 164]. In the Si-to-Si contact reliability experiment, the surface of the contact is modified through repetitive on and off cycling. During the contact and separation process, the damage incurred starts to accumulate and eventually leads to failure. Some of the failure mechanism includes material transfer, contact damage, delamination and bridge formation. Furthermore, this effect should be enhanced by elevated temperature.



**Figure 6.6: Failure mechanisms of contact switches. Repeated push and pull by turning on and off electrostatic force can result in four major mechanisms of contact degradation.**

From the reliability testing of 25 devices, it is shown that the lifetime shortens as the temperature increases. All the failed devices experience the same catastrophic phenomenon as shown in Fig. 6.1 and Fig. 6.2, where the device failed to disconnect and is permanently turned on. As the hardness of silicon decreases at elevated temperature, a higher contact area is expected [198, 199]. As a result, a larger drain-source current can flow through the contact, therefore reducing the resistance. This leads to hot switching surface degradation in conjunction with the potential applied between the contacts. At higher temperature, hot switching regularly leads to a large amount of material transfer and this is explained as a complex event that is not describable by any model [30].





**Figure 6.7: Focus ion beam milling reveals cross-sectional view of a failed device after ~5 million cycling test.**

Figure 6.7 shows one of the device's contact area failures after five million cycles. It is observed that contact roughening and bridging is formed on the contact surface. It is well understood that these defects may eventually lead to catastrophic failure in the device. Since the device is vacuum encapsulated, and all the native oxide is removed before the encapsulation, oxidation is deemed negligible. The permanent fuse between the source and the drain terminal shown in Figure 6.3 agrees with the measurement result in Fig. 6.1 and Fig. 6.2. The FIB/SEM is labelled with the terminals so it is clearer that the localized melting causes micro-welding between the two terminals.

## 6.2 Conclusion

In conclusion, the failure mechanisms of a Si-to-Si switch is analyzed and presented. The observed failure from the previous chapter is investigated and reveals that contact degradation in N/MEMS switch is an important consideration for reliability. Analysis of the contact degradation is reinforced by the physical inspection using SEM and FIB cross-section. From the inspection, some of the major failure at contacts involves various mechanical wear and surface degradation mechanisms. This includes contact damages, material transfers and bridge formation. The inspection results in coincides with the breakdown in switch reliability testing. Step-by-step experiment shows that the contact temperature is affected by both ambient temperature and the drain-source voltage. By effectively limiting the drain-source current, Joule heating at the temperature can be controlled and higher reliability can be obtained. Table 6.1 summarizes three groups that have conducted N/MEMS switch in high temperature environment.

**Table 6.1 Comparison of specification of different N/MEMS switches for high temperature environment**

<b>Institution</b>	<b>Pull-in voltage (V)</b>	<b>Contact resistance (kΩ)</b>	<b>material</b>	<b>Lifetime</b>	<b>package</b>	<b>Temperature (°C)</b>	<b>Ref.</b>
Case western University	14.1 – 17.9	> 10	SiC	$2 \times 10^9$	No	RT to 500	[31, 39]
National University of Singapore	8.5 – 21	2.7	Mo Based	$2 \times 10^4$	No	RT to 300	[34]
National University of Singapore	11 – 30	10 - 100	Si Based	$> 5 \times 10^6$ @RT $10^6$ @400°C	Vacuum encapsulated	-60 to 400	This work

## **CHAPTER 7: CONCLUSIONS AND FUTURE WORK**

### **7.1 Conclusions on current work**

In the first part of the thesis, a lateral high aspect ratio NEMS SiNF non-volatile memory is fabricated with CMOS processes. This device is systematically characterized and the device demonstrates bi-stability and therefore operates as a NVM. The SiNF is favorable due to its small dimension and may possibly enable high density application in future. The nano-size SiNF has an estimated scalable density of 390kBits/mm<sup>2</sup>. Hot switching of this device is performed and low voltage drift of 24 mV/K is possible in higher temperature environment. However, the device is not encapsulated and the reliability testing at high temperature is not satisfactory. Consequently, vacuum encapsulation packaging using Epi-seal process is performed to encapsulate a curved beam logic device in the latter part is presented. The encapsulated curved beam silicon switching device is designed, fabricated and characterized. Both simulation and experiment show that the curved beam has potential for mitigation of secondary pull-in, thus enabling a robust threshold voltage in switch operation. Micro-second switching delays

are measured, showing fast switching of 13  $\mu\text{s}$  from off to on, and immediate switch off. Meanwhile, reliability of such vacuum encapsulated switch is demonstrated with measurements that shows the device contact resistance dependence with temperature and the potential difference across the contact, drain-source voltage ( $V_{DS}$ ). In order to prevent excessive Joule heating, limiting the drain-source current,  $I_{DS}$  current is shown to prolong the lifetime of such switches at high temperature. At least  $10^6$  operation cycles fewer than 300 °C and 400 °C have been successfully demonstrated. Extra miles are achieved as the curved beam switch is verified to work under acceleration from 1 to 10 g @ 2 kHz. In the last part, the failure mechanisms and failure analysis is performed to further explain the temperature near contact. This temperature is also associated with the current that flows through the contact. The result is consistent with the physical inspection of the contact area. In summary, N/MEMS switch in this thesis has demonstrated exceptional operation in high temperature and resistant to acceleration. The high reliability could be valuable for harsh environment electronics such as automotive, aerospace and down-hole applications. Despite these features, more work need to be done in order to take the research to next level.

Through different devices' examples, Si-to-Si contacts seem to be a good candidate for MEMS switching device. This interface has demonstrated both

non-volatile memory and logic computation application. Repeatable operation in high temperature environment such as 300°C and 400 °C has been demonstrated in vacuum encapsulated Si-to-Si MEMS switch where such temperature is usually devastating to the current state-of-art CMOS devices. To lower the resistivity and amplify the range of usage, the production and design of such device requires development in the field of thin film coatings. Metallic layer such as titanium nitride (TiN), Ruthenium (Ru) and Molybdenum (Mo) is deemed to be a good add-on to the contact area to enhance the reliability of the device. Even after that, good vacuum encapsulation with non-oxidizing content is necessary to prolong the lifetime of MEMS switch, as well as providing a pristine environment for the switch to operate in harsh environment. From the previous experimental measurement and results, although a bi-stable switch is realized, the Si based NEMS switch is not suitable for rugged electronics as the reliability is poor. Due to the nano-scale dimension of the switch, report suggests that high current density, hot switching and high impact velocity may cause switch micro-welding, fracture, contact surface degradation and oxidation will eventually lead to failure [32, 162, 166, 168, 206, 207]. Under these circumstances, material selection is a crucial element to reduce contact resistance, increase heat conduction and be able to withstand contact degradation due to force. In terms

of design consideration, contact area of the switch should be optimized to prevent stiction and the device should operate in low voltage region such as < 5 V.

## **7.2 Recommendations for future work**

### **7.3 Refractory metal as possible higher reliable material**

Among all metal elements, refractory metal are known for their extraordinary resistant to heat and wear. So when metal contacts are considered, naturally possible refractory metals such as Mo, Ti, Ru, are considered.

#### **7.3.1 Material selection**

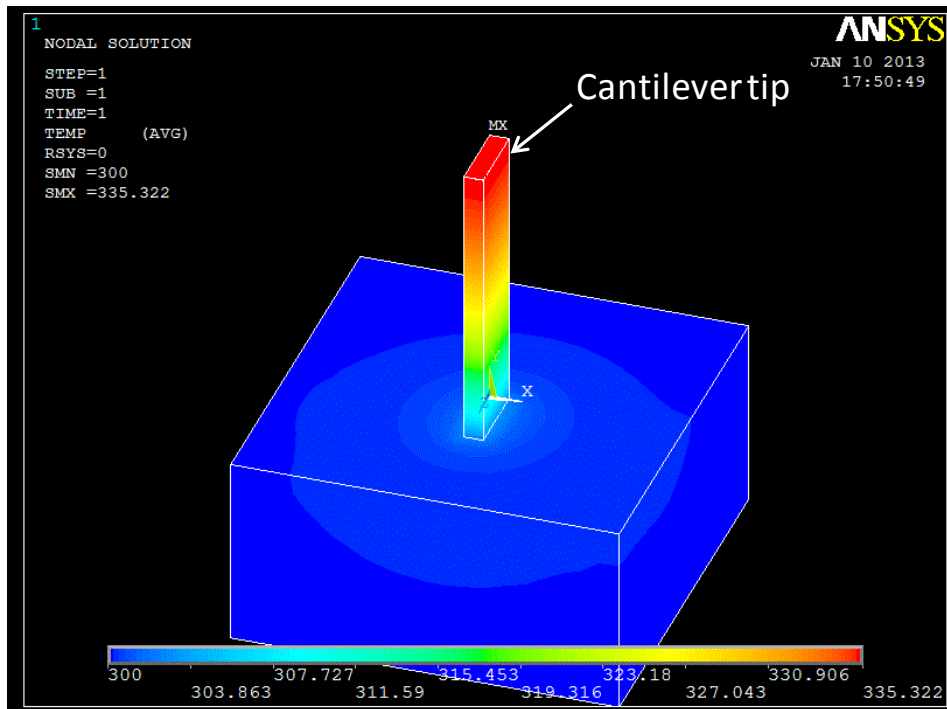
Instead of silicon, refractory metal – Molybdenum (Mo) is a good choice due to its exceptional property in conductance, hardness and melting temperature [208, 209]. Table 7.1 shows the material property of different material taken into consideration. Among the material, tungsten, W, has the highest melting point, but this material oxides easily under room condition and hence it is a challenge to be used. The next highest melting point for metal is Molybdenum, Mo, with melting temperature of 2623 °C [210], which is far superior to Si. Moreover, it has very low resistivity which suggests that the contact resistance is lower compared to Si.

**Table 7.1 Material Property of different candidate for switch [210]**

<b>Material</b>	<b>E(GPa)</b>	<b>MOHS hardness</b>	<b>Resistivity (<math>\mu \Omega</math>-cm)</b>	<b>Melting Temperature (<math>^{\circ}</math>C)</b>
Ag	83	2.5	1.6	961
Al	70	3	2.8	660
Au	78	2.5	2.2	1064
Cu	120	3	1.7	1084
Pt	184	3.5	10.5	1768
Rh	256	6	4.3	1964
Ru	292	6.5	7.1	2334
Ti	110	6	42	1668
W	405	7.5	5.3	3422
Mo	329	5.5	5.34	2623
Si	150	6.5	Doping dependent	1414
SiC	220	9	Doping dependent	2730

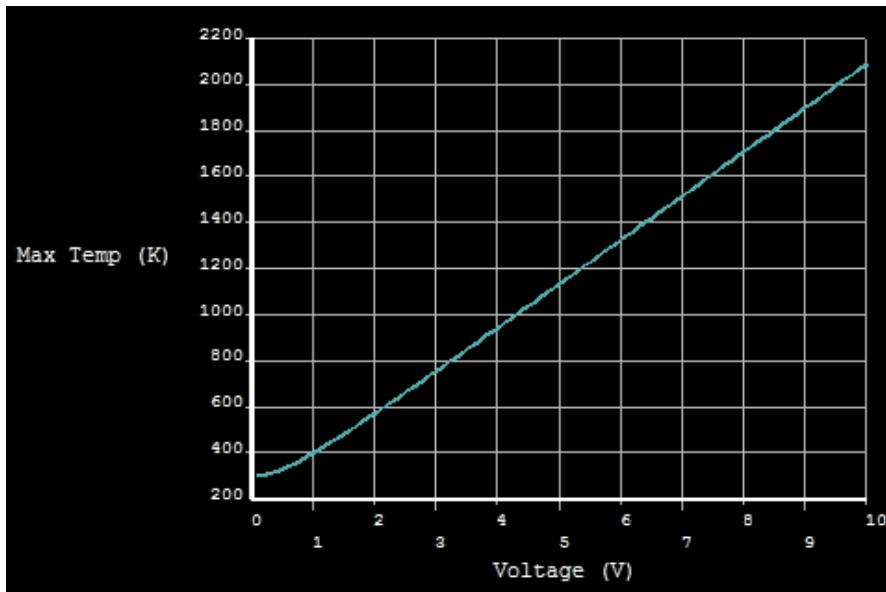
A preliminary simulation of thermal contact temperature is performed in ANSYS to verify the maximum temperature of the contact between Si and Mo. Figure 7.1 shows the 3D model simulation. A sweeping voltage is passed through a cantilever where the tip of the cantilever is referred as the contact and where the maximum temperature will occur. Bottom Mo layer is added to sink the heat source so that a reference can be defined.



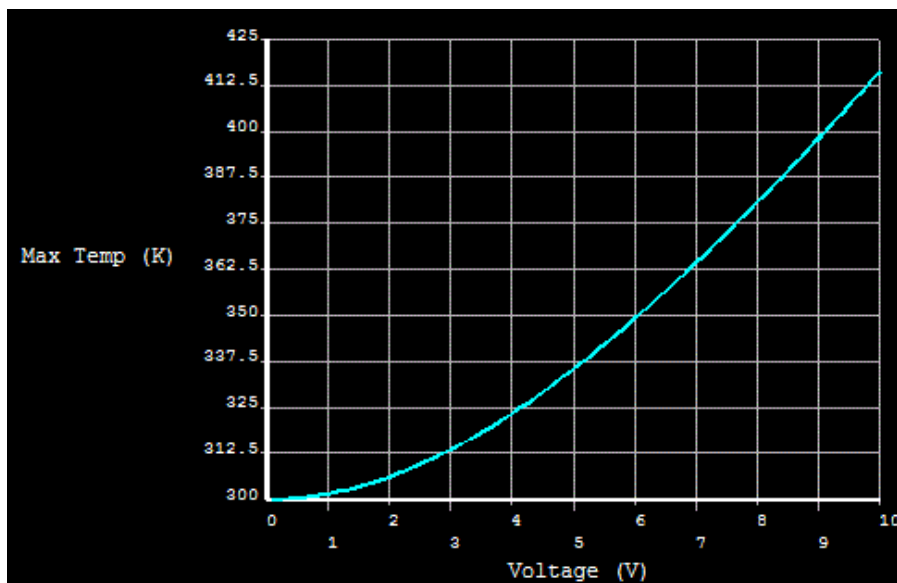


**Figure 7.1: Modeling of joule heating of contact resistor using ANSYS**

Figure 7.2 and Figure 7.3 shows the simulation results of Si based contact and Mo based contact respectively. From the results, it is obvious that Mo is far more superior contact element than Si. The maximum temperature of Si is more than 2000K while the maximum temperature of Mo is only approximately about 415K. Under this condition, Mo stands a better chance to withstand the Joule heating during switching while Si based switch is easily liable to fail due to micro-welding or fusing. The ANSYS code for this simulation is attached in Appendix A2.



**Figure 7.2: Max temperature of contact tips versus sweeping voltage of Si based contact.**

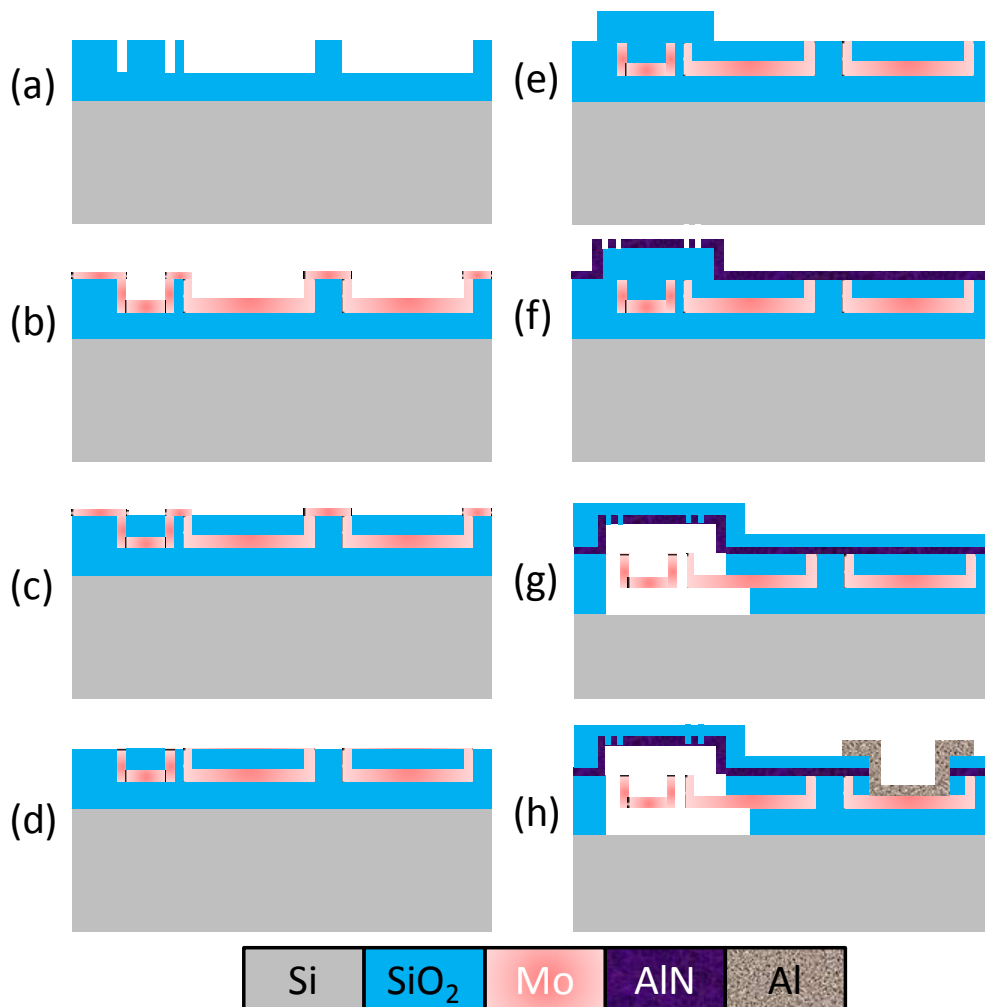


**Figure 7.3: Max temperature of contact tips versus sweeping voltage of Mo based contact.**

### 7.3.2 A vacuum encapsulated Mo curved beam switch

With the above discussion, Mo is a good candidate to be implemented in N/MEMS switch. However, the process flow is entirely different and new challenges expected before demonstrable devices can be fabricated.

### 7.3.3 Fabrication process flow

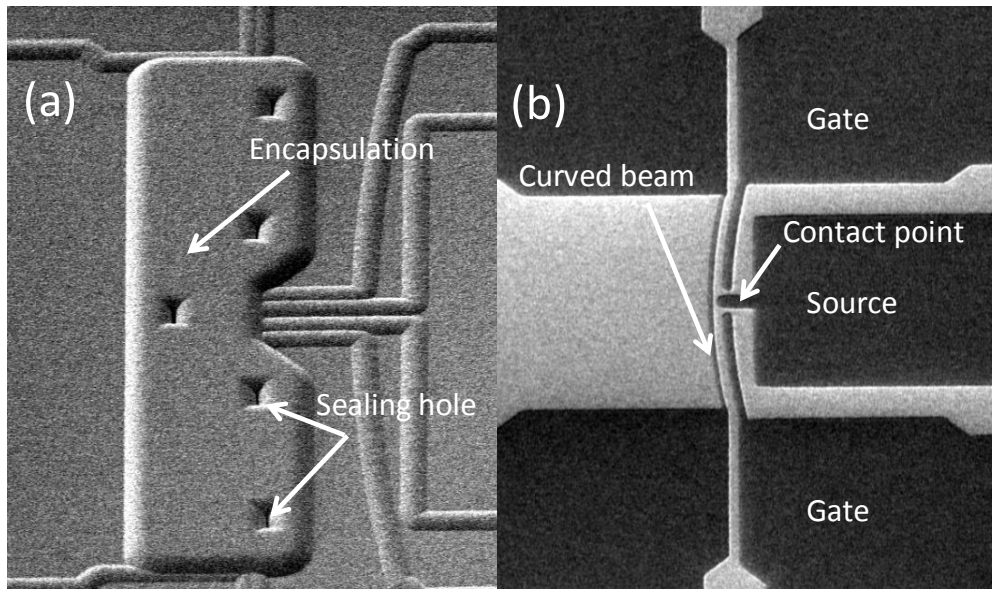


**Figure 7.4: Process flow of a vacuum encapsulated Mo based switch. (a) Define SiO<sub>2</sub> molding. (b) Mo deposition. (c) Define SiO<sub>2</sub> masking. (d) CMP isolation. (e) Deposit sacrificial SiO<sub>2</sub> (f) AlN capping layer with release vent. (g) Deposit SiO<sub>2</sub> sealing after release. (h) Pad metallization.**

Figure 7.4(a)-(h) shows the proposed process flow of the three-terminal Mo based N/MEMS switch. Starting from a thick oxide on bulk Si substrate, the Mo beam and terminal structures are partially etched into the oxide layer. This partial etched oxide layer serves as a mould for the beam and the terminals as the next Mo deposition will conform to the topography of the etched surface. Subsequently, Mo followed by a thick of SiO<sub>2</sub> is deposited. The SiO<sub>2</sub> layer will serve as a mask to isolate the Mo terminal. To do this, the Mo has to be exposed. So a CMP is performed to reveal the Mo and a RIE Mo etch is done to isolate the Mo layer into source, drain and gate. To encapsulate the device, sacrificial oxide housing is deposited and patterned right on top of the actuation area. This is followed by AlN housing with small release holes defined. The release holes are defined with CD < 1.5 μm to allow VHF to etch and release the Mo beam inside the housing. After that the release holes are sealed with another layer of thick oxide. Lastly, to contact the terminals, via opening through the thick oxide and Al metallization is done to provide metallised pads for testing.

### 7.3.4 Fabrication results

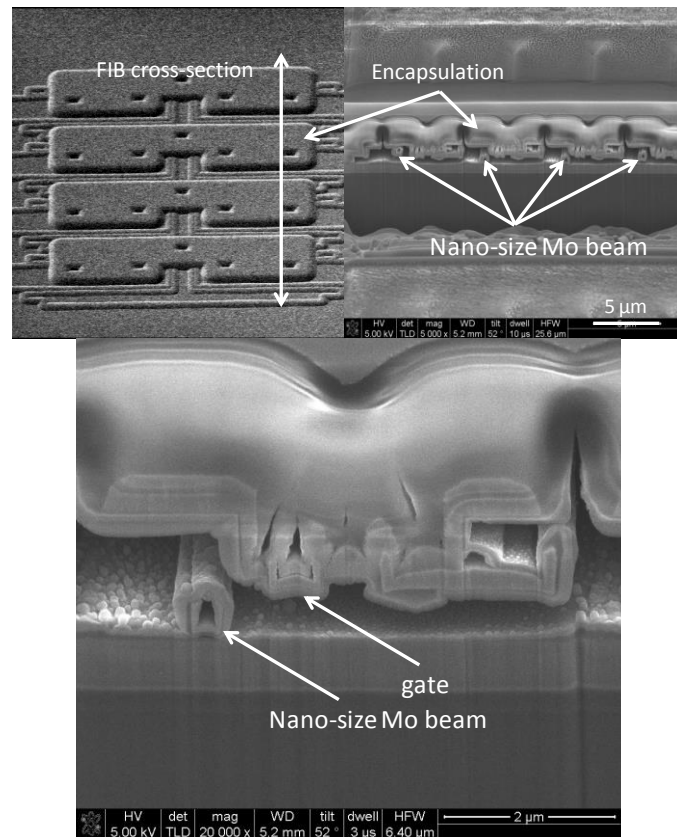
Preliminary fabrication results of the encapsulated Mo based N/MEMS switch is shown in Figure 7.5. Overall the encapsulation is a success but the device is not able to function well due to intrinsic leakage in the substrate. The source of leakage is believed to be a contamination problem due to pollution in deionised water.



**Figure 7.5: Preliminary fabrication outcome of the proposed process flow. (a) Vacuum encapsulation performed on Mo switch. (b) Structure before encapsulation showing terminals and curved beam.**

### 7.3.5 Towards high density all mechanical logic computation

In the attempt on creating high density logic array, four Mo based N/MEMS switches are distributed into an array and vacuum encapsulated. Figure 7.6(a) shows the preliminary fabrication result of a switch array comprised of four Mo beams and its terminals.



**Figure 7.6: (a) Array of four Mo switches with encapsulation. (b) FIB cross-section of encapsulation showing four nano-size Mo beams. (c) Zoom in detail of one switch.**

The switches are encapsulated in vacuum using thin film layers. An FIB cross-section shown in Figure 7.6(b) shows that the encapsulation is a success. The zoom-in details of one device is shown in Figure 7.6(c). The nano-size Mo beam adjacent to the gate terminal is shown to be fully released. This preliminary fabrication result shows possible high density implementation using N/MEMS switch. This result is encouraging and suggests that more complex N/MEMS switch systems for harsh environment electronics can be integrated.

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## APPENDICES

### A1. ANSYS CODE – Simulation of bi-stable hysteresis curve

```
! --- Beam Dimensions
bl      = 1           ! Beam length, um (X)
bt      = 0.03       ! Beam thickness, um (Y)
bw      = 0.2        ! Beam width, um (Z)
gap     = 0.02       ! gap, um
Rsep    = 3E-3       ! Min gap

H1      = 0.2        ! Distance between substrate and gate
Hgate   = 0.8        ! Gate height

! --- Beam Meshing Controls
Nl      = 40         ! # Elements in length direction
MF      = 16         ! Meshing length factor
Nt      = 1          ! # Elements in thickness dir

hAm     = 5E-14      ! Hamaker Constant for vdW forces in
pJ
Tol     = 2E-4       ! Tolerance between iterations in um
maxCLoop= 50

! --- Applied load
Vmin    = 0          ! Start Voltage
Vmax    = 3          ! End Voltage (Set this above pull-in -
not too high or will error)
Vstep   = 0.2        ! Step Voltage
Nswp    = 3

!-----
eps0 = 8.854E-12
PI = 3.141592654

/CONT, 1, 128
/UIS, MSGPOP, 3
```

```

! --- Preprocessor
/PREP7
BETAD, 1E-10

! ----- Element Types -----
ET,1,PLANE183, , ,          !    PLANE183,    Structural
(UX,UY), with thickness(width) input
ET,2,TARGE169
ET,3,CONTA172
KEYOPT,3,3,0
KEYOPT,3,4,0
KEYOPT,3,5,0
KEYOPT,3,7,0
KEYOPT,3,8,0
KEYOPT,3,9,0
KEYOPT,3,10,2
KEYOPT,3,11,0
KEYOPT,3,12,0
KEYOPT,3,2,0
KEYOPT,2,2,0
KEYOPT,2,3,0

! --- Titanium Silicide
!MP,EX,1,160E3
!MP,PRXY,1,0.22
!MP,DENS,1,2.330E-15

MP, EX, 1, 265E-3
MP, PRXY, 1, 0.21
MP, DENS, 1, 4E-15
MP, MU, 1, 0.2

! ----- Draw Structure -----
RECTNG, 0, bl, 0, bt

! ----- Mesh Structure -----
ESIZE, bl/Nl
LSEL, S, LOC, Y, 0
LESIZE, ALL, , ,Nl, 1/MF
LSEL, A, LOC, Y, bt

```

```
LESIZE, ALL, , ,Nl, MF
LSEL, S, LOC, Y, 0+1E-7, bt-1E-7
LESIZE, ALL, , ,Nt
AMESH, ALL
```

```
! ----- Bottom Target -----
```

```
R,2
REAL,2
R,2,,,1.0,0.1,0,
RMORE,,,1.0E20,0.0,1.0,
RMORE,0.0,0,1.0,,1.0,0.5
RMORE,0,1.0,1.0,0.0,,1.0
```

```
*GET,_KPmax,KP,0,NUM,MAX
K, _KPmax+1, 0, -gap+Rsep, 0
K, _KPmax+2, bl, -gap+Rsep, 0
L, _KPmax+2, _KPmax+1
LSEL, S, LOC, Y, -gap+Rsep
LATT, -1, 2, 2
LMESH, ALL
```

```
! ----- Bottom Contact -----
```

```
LSEL,S,LOC,Y,0
NSLL,S,1
ESLN,S,0
MAT, 1
TYPE,3
REAL, 2
ESURF
```

```
! ----- Top Target -----
```

```
R,3
REAL,3
R,3,,,1.0,0.1,0,
RMORE,,,1.0E20,0.0,1.0,
RMORE,0.0,0,1.0,,1.0,0.5
RMORE,0,1.0,1.0,0.0,,1.0
```

```
*GET,_KPmax,KP,0,NUM,MAX
K, _KPmax+1, 0, bt+gap-Rsep, 0
K, _KPmax+2, bl, bt+gap-Rsep, 0
```

```

L, _KPmax+1, _KPmax+2
LSEL, S, LOC, Y, bt+gap-Rsep
LATT, -1, 3, 2
LMESH, ALL

! ----- Top Contact -----
LSEL,S,LOC,Y,bt
NSLL,S,1
ESLN,S,0
MAT, 1
TYPE,3
REAL, 3
ESURF

! ----- Fix -----
LSEL, S, LOC, Y, -gap+Rsep
LSEL, A, LOC, X, 0
DL, ALL, , ALL

FINISH

/SOLU
ANTYPE, STATIC

! --- Define arrays
NSEL, S, LOC, Y, 0
NSEL, R, LOC, X, H1, bl
CM, enodes, NODES
*GET, Nnodes, NODE, 0, COUNT
*DIME, Profile, ARRAY, Nnodes, maxCLoop
*DIME, ConvTest, ARRAY, Nnodes, 1
*DIME, Nforce, ARRAY, Nnodes

*DIME, Uend, TABLE, Nswp*(Vmax-Vmin)/Vstep+1
*DIME, UendArr, ARRAY, Nswp*(Vmax-Vmin)/Vstep+1
Uendnode = NODE(bl, 0, 0)

ALLSEL, ALL

```

```

*DO, L, 1, Nswp*(Vmax-Vmin)/Vstep+1
  *IF, L, LE, (Vmax-Vmin)/Vstep+1, THEN
    Vmag1 = Vmin + (L-1)*Vstep
    Vmag2 = 0
  *ELSEIF, L, LE, 2*(Vmax-Vmin)/Vstep+1
    Vmag1 = 2*Vmax - Vmin - (L-1)*Vstep
    Vmag2 = 0
  *ELSE
    Vmag1 = 0
    Vmag2 = -(2*Vmax - Vmin - (L-1)*Vstep)
  *ENDIF

```

```

*DO, P, 1, maxCLoop
  /SOLU
    *IF, P, GT, 1, THEN
      PARSAV, ALL
      ANTYPE, STATIC, REST
      PARRES
    *ENDIF
    !DELTIM, del_t
    !TIME, P*t_f

    ! --- Apply Loads
    NSEL, S, NODE, , enodes
    *GET, Nnum, NODE, 0, NUM, MIN
    *DO, I, 1, Nnodes
      _aaa=arnode(Nnum)
      FN = 0
      *IF, P, GT, 1, THEN
        ! Add van der Waals
          FN = FN -
          _aaa*hAm/6/PI/((gap+Profile(I,P-1))**3)
          FN = FN +
          _aaa*hAm/6/PI/((gap-Profile(I,P-1))**3)
        ! Add Electrostatic Force
          FN = FN -
          eps0*_aaa/2*(Vmag1**2)/((gap+Profile(I,P-1))**2)
          FN = FN +
          eps0*_aaa/2*(Vmag2**2)/((gap-Profile(I,P-1))**2)
      *ENDIF
    *ENDIF

```



```

                F, Nnum, FY, FN
            *ENDIF
            Nnum = NDNEXT(Nnum)
        *ENDDO

        ALLSEL, ALL
        SOLVE
    FINISH

/POST1
    SET, LAST
    NSEL, S, NODE, , enodes
    *GET, Nnum, NODE, 0, NUM, MIN

    *DO, I, 1, Nnodes
        Profile(I, P) = UY(Nnum)
        Nnum = NDNEXT(Nnum)
    *ENDDO

! Check centerline Profile for convergence
*IF, P, GT, 1, THEN
    *VABS, 1
    *VOPER, ConvTest, Profile(1,P-1), SUB, Profile(1,P)
    ! Obtain the difference between the the current and previous step
    *VABS, 0
    *VSCFUN, ConvMax, MAX, ConvTest
    *IF, ConvMax, LE, Tol, THEN
        *EXIT
    *ENDIF
*ENDIF
    FINISH
*ENDDO

*IF, L, LE, 2*(Vmax-Vmin)/Vstep+1, THEN
    Uend(L,0) = Vmag1
*ELSE
    Uend(L,0) = -Vmag2
*ENDIF
    Uend(L,1) = UY(Uendnode)
    UendArr(L,1) = UY(Uendnode)

```

```

*IF, UY(Uendnode), GE, gap-Rsep, THEN
  *EXIT
*ENDIF

/SOLU
  PARSAV, ALL
  ANTYPE, STATIC, REST
  PARRES
  FINISH

*ENDDO

Ldup = L+L-(Vmax-Vmin)/Vstep
*DO, Lsym, L+1, Ldup
  Uend(Lsym,0) = -Vmax+Vstep*(Lsym-L-1)
  Li = Lsym - L + Vmax/Vstep
  Uend(Lsym, 1) = -UendArr(Li, 1)
*ENDDO
  Uend(Lsym+1, 1) = -UendArr(Li, 1)

  /AXLAB, X, Voltage (V)
  /AXLAB, Y, End Node Displacement (um)
  /TITLE, Min Sep: %Rsep*1000% nm. NI: %NI%. MF: %MF%.
  *VLEN, Ldup+1
  *VPLOT, Uend(1,0), Uend(1,1)

```

## **A2. ANSYS CODE – Temperature simulation of contact**

### **resistor**

```

! Thermal simulation of a block, with "contact resistor"
! Implement voltage sweep

```

```

/UIS, MSGPOP, 3
/PREP7

```

```

bh      =  1.5      ! Beam height
bt      =  0.1      ! Beam thickness

```

```
bw          = 0.4          ! Beam width
res_t       = 5E-2        ! Contact resistor thickness
```

```
Vstart     = 0.1
Vend       = 10
Vstep      = 0.1
Nsteps     = ((Vend - Vstart)/Vstep) + 1
CurrV      = Vstart
```

```
BLOCK, 0,bt,0,bh-res_t,0,bw
BLOCK, 0,bt,bh-res_t,bh,0,bw
ALLSEL,ALL
VGLUE,ALL
```

```
ET,1,SOLID226,110
```

```
! === Material Properties ===
```

```
MP, DENS, 1, 2.329E-15
MP, KXX, 1, 32E6
MP, RSVX, 1, -8E-11,6E-13
!MP, SBKX, 1, 0
```

```
MP, DENS, 2, 2.329E-15
MP, KXX, 2, 32E9
MP, RSVX, 2, -1.49333E-9,1.12E-11
!MP, SBKX, 2, 0
```

```
VSEL,S,LOC,Y,0,bh-res_t
VATT,1,,1
VSEL,S,LOC,Y,bh-res_t,bh
VATT,2,,1
```

```
ALLSEL,ALL
ESIZE,0.05
VMESH,ALL
ALLSEL,ALL
```

```
FINISH
/SOLU
```

```

ANTYPE,0
NEQIT, 100 ! Max iterations per step

*GET, Nnodes, NODE, 0, COUNT
*DIME, TipTemp, TABLE, Nsteps
*DIME, NodeTemps, ARRAY, Nnodes

*DO, L, 1, Nsteps
  NSEL,S,LOC,Y,0
  D,ALL,VOLT,0
  D,ALL,TEMP,300
  NSEL,S,LOC,Y,bh
  D,ALL,VOLT,CurrV
  ALLSEL,ALL
  TUNIF,300

  ALLSEL,ALL
  SOLVE
  FINISH

  /POST1
  SET, LAST

  ALLSEL,ALL
  *GET, Nmin, NODE, 0, NUM, MIN
  *VGET, NodeTemps, NODE, Nmin, TEMP
  *VSCFUN, MaxTemp, MAX, NodeTemps
  TipTemp(L,0) = CurrV
  TipTemp(L,1) = MaxTemp

  ! Determine next voltage value
  CurrV = CurrV + Vstep

  *IF, L, EQ, Nsteps, THEN
    *EXIT
  *ENDIF

  FINISH

  /SOLU

```

```

    PARSAV, ALL
    ANTYPE, STATIC, REST
    PARRES
*ENDDO

! === Output data ===
! Write to file
*CREATE, mymac, mac
/OUTPUT, 'tiptemp_reduced_resist','dat'
*VWRITE, 'Voltage', 'Max_Temp'
% 14C % 14C
*VWRITE, TipTemp(1,0), TipTemp(1,1)
% 14.5G % 14.5G
/OUTPUT, TERM
*END
/INPUT, mymac, mac

! Plot graph
/TITLE, Temperature Simulation, reduced resistivity of Si 100X
/AXLAB, X, Voltage (V)
/AXLAB, Y, Max Temp (K)
*VLEN, L
*VPLOT, TipTemp(1,0), TipTemp(1,1)
FINISH

```