ULTRA LOW POWER CIRCUITS FOR WEARABLE BIOMEDICAL SENSORS

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NATIONAL UNIVERSITY OF SINGAPORE

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DECLARATION

I hereby declare that this thesis is my original work and it has been written by me in its entirety.

I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

ZHANG XIAOYANG

MARCH 13, 2015

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Contents

SUMMARY

The main research topic is designing high-performance energy-efficient circuits for wearable sensors, which capture and process biomedical signals such as electrocardiogram (ECG) and respiratory rate for telemedicine and preventive healthcare service. New pseudo resistors are proposed to avoid attenuating sub-0.1 Hz signal with <0.4% distortions at 3 V output. A positive feedback loop for AC-coupled analog front-end (AFE) improves the input impedance and hence the signal quality. Also, a DC-coupled AFE featuring 4 GΩ input impedance is designed for dry-electrode ECG sensing. The energy efficiency of the sensor system is enhanced by integrating signal processing tasks into the analog-to-digital converter (ADC). Based on level-crossing sampling with delta modulation, a 220-nW event-driven ADC with QRS detection function is introduced. Integrated with ultra-wideband transmitter, the wireless ECG sensor consumes less than 3 μW under full-rate transmission. All the presented designs were fabricated and verified by the chip measurements.

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List of Abbreviations

+P	Positive Prediction.
A2I	Analog-to-Information.
ADC	Analog-to-Digital Converter.
AFE	Analog Front-End.
AMI	Acute Myocardial Infarction.
BE	Back-End.
BGR	Bandgap Reference.
BP	Blood Pressure.
bpm	Beat Per Minute.
BUF	Buffer.
CC	Capacitive-Coupled.
CHD	Coronary Heart Disease.
CHS	Chopper Stabilization.
CM	Common Mode.
CMFB	Common-Mode Feedback.
CMRR	Common-Mode Reject Ratio.
CT	Continuous-Time.
CVD	Cardiovascular Disease.

DAC	Digital-to-Analog Converter.
DRL	Rriven-Right-Leg.
DSP	Digital Signal Processing.
ECG	Electrocardiogram.
EDR	ECG-Derived Respiratory.
EMG	Electromyography.
FFT	Fast Fourier Transform.
GBW	Gain-Bandwidth Product.
HR	Heart Rate.
HRV	Heart Rate Variation.
IA	Instrumental Amplifier.
ICG	Impedance Cardiography.
IFC	Input-Feature Correlated.
IoT	Internet-of-Things.
IR	Impulse-Radio.
LA	Left Arm.
LC	Level-Crossing.
LCS	Level-Crossing Sampling.
LL	Left Leg.
LMS	Least Mean Square.
LSB	Least Significant Bit.
MCU	Microcontroller.
MICS	Medical Implant Communication Service.
MiM	Metal-insulator-Metal.

MLII	Modified Lead II.
MUX	Multiplexer.
NEF	Noise Efficiency Factor.
NFC	Near-Field Communication.
NSR	Normal Sinus Rhythm.
OPA	Operational Amplifier.
OTA	Operational Transconductance Amplifier.
PGA	Programmable-Gain Amplifier.
PSRR	Power-Supply Reject Ratio.
PUT	Pulse-Triggered.
PVC	Premature Ventricular Complex.
QFG	Quasi-Floating Gate.
RA	Right Arm.
RF	Radio Frequency.
RL	Right Leg.
RR	Respiratory Rate.
RSA	Respiratory Sinus Arrhythmia.
RTC	Real-Time Clock.
S/H	Sample-and-Hold.
SA	Sinoatrial.
SAR	Successive Approximation.
Se	Sensitivity.
SFDR	Spurious-Free Dynamic Range.
SNDR	Signal-to-Noise and Distortion Ratio.

SNR	Signal-to-Noise Ratio.
SoC	System-on-Chip.
SPI	Serial Peripheral Interface.
SRAM	Static Random-Access Memory.
THD	Total Harmonic Distortion.
t-PUT	Time-Assisted Pulse-Triggered.
TX	Transmitter.
UWB	Ultra-WideBand.
WSN	Wearable Sensor Network.
XTAL	Crystal Oscillator.

CHAPTER 1

Introduction

1.1 Background

Cardiovascular disease (CVD) is the leading cause of human death around the world [1]. CVD refers to diseases affecting the cardiovascular system including the heart, the blood vessels, or both [2]. The common CVDs include coronary heart disease (CHD), heart failure, and stroke. In 2008 around 17.3 million people died from CVDs globally. The projected number of death from CVDs will increase to 23.3 million by the year of 2030 [3].

Even in developed countries with well-established healthcare system such as the United States, CVD-related death and cost are a growing social burden. Fig. 1.1 and 1.2 show the death and costs statistics for CVDs from American Heart Association [4]. By 2030, more than $ 800 billion is to be invested in the health expenditures targeting CVDs, exceeding any other diagnostic groups.

Early action is the key for reducing heart disease risks. The late detection of CVD symptoms and the lack of prompt medical treatment often cost the patient's life. Some of the warning symptoms including chest pain and shortness of breath are often easy to identify. But to facilitate further diagnosis on the heart conditions,

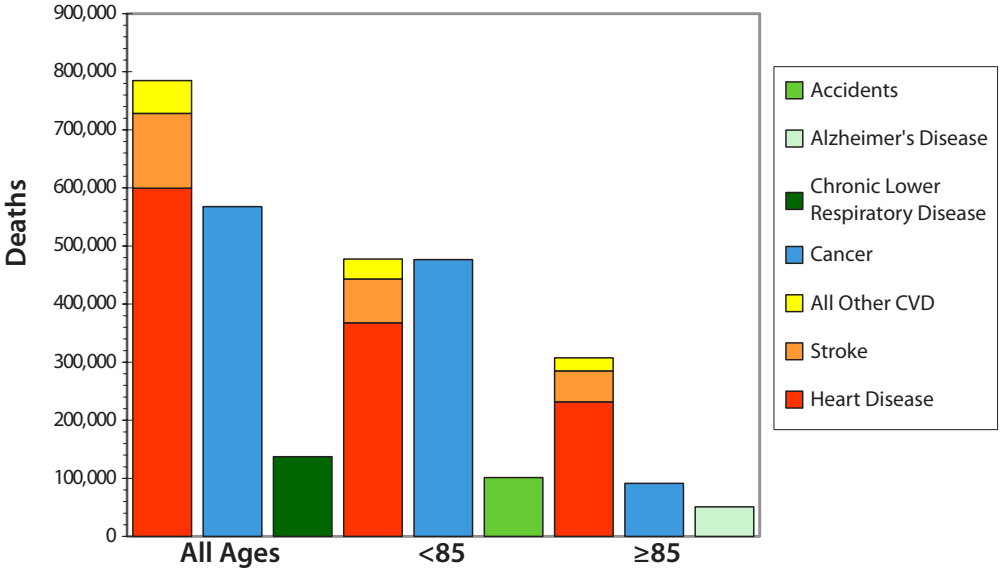

Figure 1.1: Cardiovascular disease and other major causes of death in the United States, 2009.

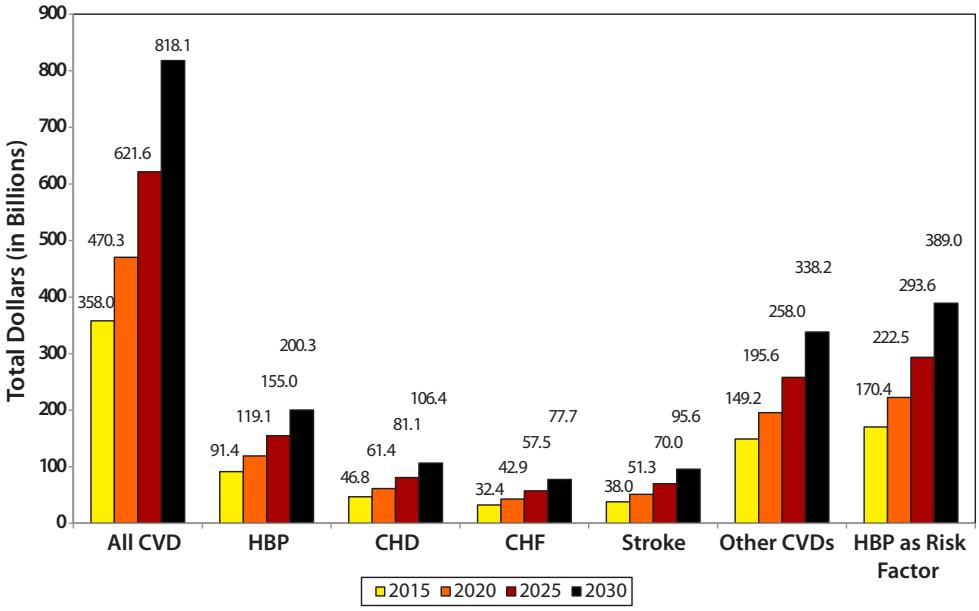

Figure 1.2: Projected total costs of cardiovascular disease in 2010 billion $ in the United States.

more thorough evidence is required to evaluate the heart activity. The human heart activities include the electrical stimulation and the mechanical muscle contraction in response to the electrical impulse. While blood pressure, pulses, and other perfusion approaches are selected to monitor the mechanical function [5], the best way to assess the electrical cardiac function is through examining the electrocardiogram (ECG) signal.

The ECG is a vital part of the health assessment, manifesting the electrical activity of the heart. Fig. 1.3 [6] provides a typical ECG signal as well as the corresponding electrical conduction system of the heart. By identifying any possible abnormal heart rhythm or arrhythmia from ECG traces, various detailed information on heart conditions is obtained [7].

Mostly the ECG is captured through several adhesive electrodes attached on the skin surface, and several different lead systems exists for various diagnostic purposes. The commonly adopted 3-lead system requires connecting 3 electrodes to the Left Arm (LA), Right Arm (RA), and Left Leg (LL) respectively. In this system, three lead vectors are available with

$$\text{Lead I} = \Phi_{LA} - \Phi_{RA} \tag{1.1}$$

$$\text{Lead II} = \Phi_{LL} - \Phi_{RA} \tag{1.2}$$

$$\text{Lead III} = \Phi_{LL} - \Phi_{LA} \tag{1.3}$$

where Φ_{LA}, Φ_{RA}, Φ_{LL} are the potentials of the 3 attached electrodes. In other word, to obtain the standard 3-lead ECG, is basically to measure the voltage differences between the LA, RA, and LL electrodes. A more thorough approach to assess the heart condition is the 12-lead ECG system, which introduces another 6 precordial leads V_1 to V_6. The 12-lead system is of significant clinical value [6], and the suggested placement is illustrated in Fig. 1.4 [8]. ECG diagnosis is often performed by cardiologists reading the ECG strip captured by ECG machines,

with an ECG strip example given in Fig. 1.5.

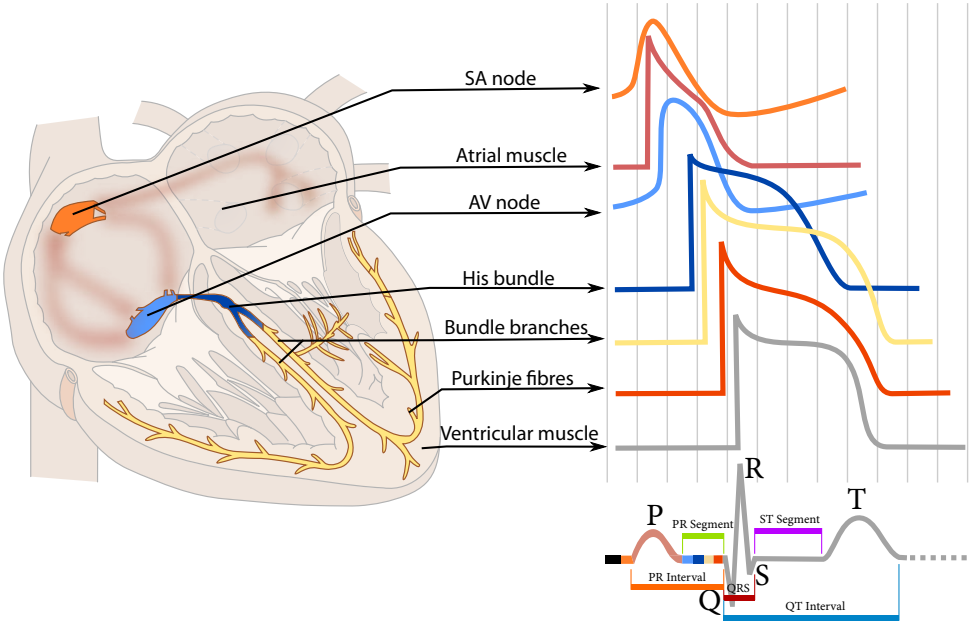

Figure 1.3: ECG and its conduction origins.

To reduce the heart attack risk and prevent severe heart damage, long-term continuous heart condition monitoring solutions are favored. This is because many arrhythmias, especially those at early stages, occur rather sporadically and infrequently. Currently a Holter—the most commonly used ECG monitoring device in hospitals—can only record the ECG for 1 or 2 days at maximum. Unless the warning symptoms are becoming regular, it is unlikely the Holter could help provide early diagnosis and preventive medications on CVDs. Moreover, the subject still needs to visit the hospital in order to perform the ECG screening test. This hospital-centered healthcare service in the end discourages people to make early and preventive actions on CVDs due to its inconvenience and inefficiency.

In response to the challenges mentioned above, a new healthcare framework based on telemedicine and preventive medicine is proposed. Shown in Fig. 1.6, the system includes wearable sensor network (WSN) at the patient side, and data storage and mining at the hospitals or other healthcare service providers. Under

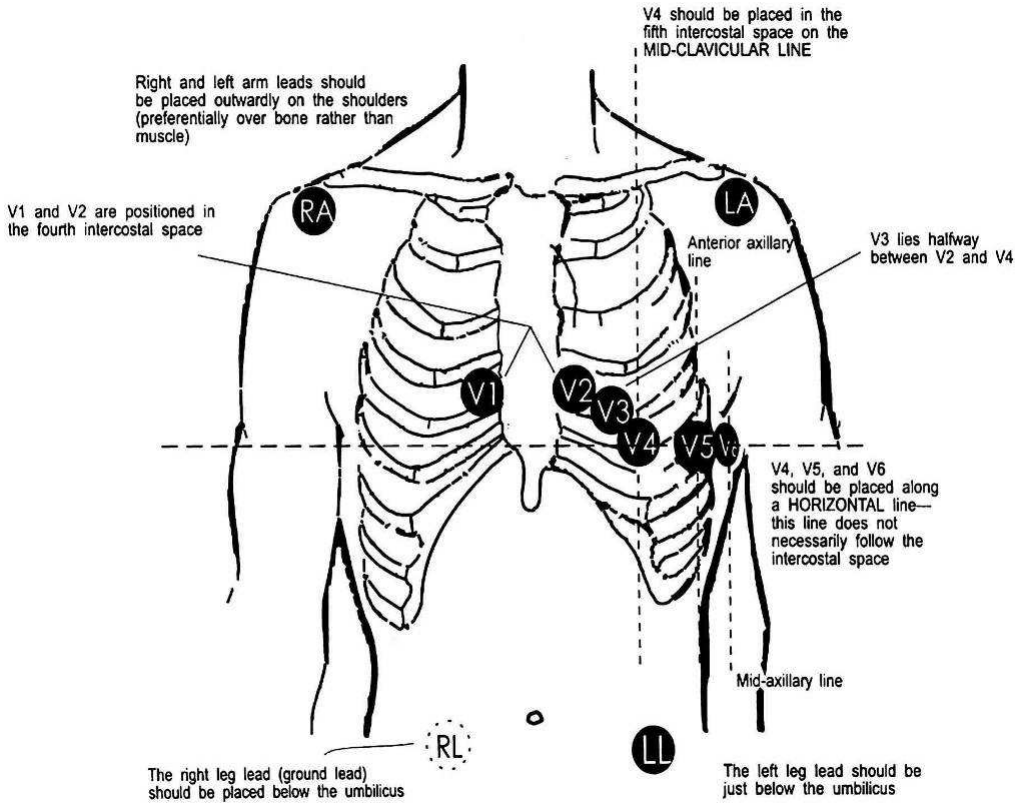

Figure 1.4: 12-lead ECG electrode placement.

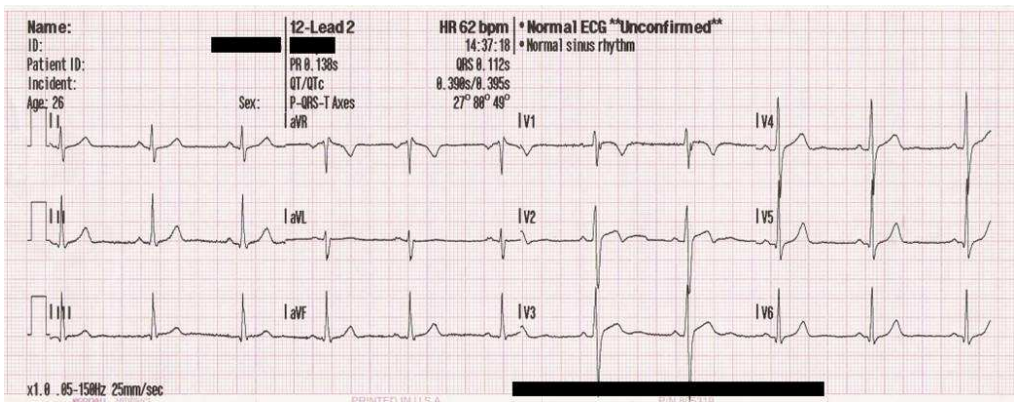

Figure 1.5: Example of a 12-lead ECG strip.

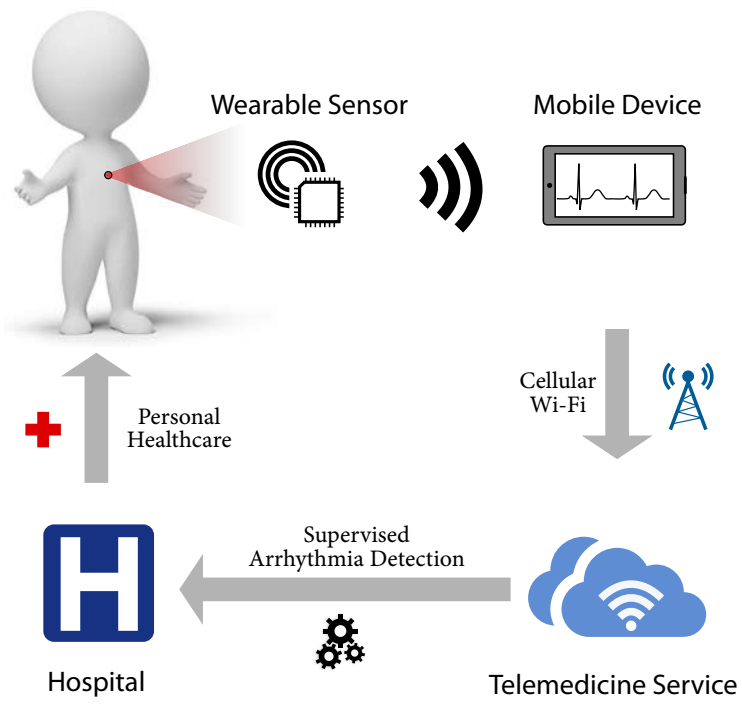

Figure 1.6: Telemedicine-based healthcare using wearable sensors.

the Internet-of-Things (IoT) context, a wearable biomedical sensor captures the ECG signal from the electrodes placed on the body skin, suppress the noise, and transmit the ECG data to a personal gateway like the smartphone. The wireless transmission from the sensor to the phone can be directly through near-field communication (NFC), Bluetooth LE, or proprietary radios. Next, the vital sign information is securely sent to the telemedicine cloud storage and analyzed by the professions in hospitals, providing diagnostic assessments based on the subject's health condition. The patient can take advantages of the preventive healthcare and early diagnosis on heart conditions without the trouble of frequent hospital visits. In case of heart attack, the patient will be provided with immediate action through the wireless communication within the golden hour, significantly increasing the chance of survival or near-complete recovery. This personalized healthcare service is more effectively and promptly than the traditional healthcare models.

1.2 Wearable Biomedical Sensor

One of the most critical parts in the telemedicine infrastructure is the wearable sensor. The ECG sensor captures the ECG signal and transmit the data eventually to the cloud through the mobile gateway. The main design targets for wearable ECG device include compact size, long battery life, high quality ECG capturing, comfort and etc, with more details rendered as follows.

1. **ECG Quality for Medical Use**

   Reliable diagnosis is only possible if the acquired ECG traces are clean and accurate. As shown in Fig. 1.3, each part of the ECG represents the electrical activity of a particular node or junction. Therefore all the PQRST waves should be clearly identifiable on the graph. Because the ECG peak-to-peak amplitude is only several millivolts, the sensor will rely on the low-noise high-gain amplifier to suppress noise. Such an amplifier could consume excessive power if designed improperly. Besides the noise, other parameters including common-mode rejection ratio (CMRR) and total harmonic distortion (THD) are also critical to the ECG tracing quality.

2. **Size & Power**

   The wearable device is often powered by a rechargeable battery, and its size is mainly restricted by the battery mounted. Therefore to reduce the size and increase the battery life, the power consumption for the circuit should be extremely low. Long battery life or self-powered sensor is mostly welcomed in such applications as it facilitates continuous recording of ECG signal without causing much inconvenience to the patient like replacing the battery and re-applying electrodes. For example, using a ultralight $2\times12\times12.5$ mm^3 10-mAh 3.7-V Lithium polymer cell, the entire circuit power must be less than 50 μW if aiming for one month use per charge. This

becomes even more challenging if the wireless transmitter is included. The wireless power is often the most power consuming part of the entire system, and is proportional to the data rate. Therefore, the duty cycle must be below 0.1 % in order to achieve this goal [9].

3. **Comfort & Long-Term Concerns**

   Most sensors require silver/silver choloride (Ag/AgCl) wet electrodes for ECG capturing, which lower the skin/electrode impedance and improves signal quality. However, the electrolyte often causes skin irritation after long-time wear, and the signal quality will deteriorate after the gel is dry. Hence wet electrodes are not the best solution for long-term monitoring. Using dry electrodes avoids those problems at the expense of much higher input impedance, and the ECG signals captured under dry electrodes using existing sensors are much worse and cannot be used for diagnosis purposes.

4. **Multiple Functions**

   It is desirable to incorporate in the same sensor other possible diagnostic functions, such as heart rate (HR) extraction and heart rate variation (HRV) detection. Meanwhile, a normal ECG trace cannot rule out the possibility of an impending heart attack like acute myocardial infarction (AMI) [10], and other vital signs like respiratory and blood perfusion could improve the fidelity for complete CVD risk assessment. In particular, respiratory rate could provide significant prognostic information [11] for AMI patients. Dyspnea (breathlessness) or tachypnea (rapid breathing), which often accompany heart attack, can be easily identified by checking the respiratory rate [12]. It is therefore desirable to capture various vital signs, especially for the patients who have a prior heart attack history.

Unfortunately, no existing sensors fulfill all the requirements listed. Most commercial low-noise amplifiers consume significant power that makes them unsuitable for long-term wearable sensors. It is therefore required to design an application-specified sensor circuit for this low-power wearable application. Meanwhile, many of the recent low-power ECG sensor designs have high noise floor and poor ECG signal qualities. There are even fewer designs that are able to work with dry electrodes or capture extensive vital signs. Designing a low-noise low-power multi-functional ECG sensor requires significant research efforts, which are therefore covered in the remaining part of this dissertation.

1.3 Organization of the Thesis and Main Contributions

The theis highlights the system- and circuit-level low-power design techniques for the biomedical ECG sensor, with main focus on the analog front-end circuit and the event-driven system. The first part including Chapter 2 through 4 discusses the low-power front-end amplifier designs for ECG and also body impedance measurements.

- Chapter 2 starts with a review of selected works on low-power biomedical sensors. General considerations for the sensor front-end are discussed, including the evaluations on various resistor implementations aiming at close-DC high-pass corner frequency and low harmonic distortion. Two designs with different process technologies are studied.

- Chapter 3 presents a design with improved performance as well as other functions such as respiratory for comprehensive heart monitoring. A low-bandwidth impedance monitoring method is proposed for applications such as respiratory monitoring. The design also incorporate various auxiliary blocks to improve the power efficiency.

- Chapter 4 further improves the design in Chapter 3 for impedance resolution with two ECG front-end design techniques. A positive current feedback loop improves the input impedance and ECG signal quality. Back-connected diodes are used at the amplifier inputs to lock the input common mode and accelerates ECG baseline settling time.

Following the discussions on front-end designs, the second part explores further opportunities to reduce the ECG sensor power beyond the amplifier's level.

- Chapter 5 moves to the data compression area to reduce the system power. After introducing the current research progress on level-crossing ADCs, a nanoWatt event-driven ADC with continuous-time QRS detections is proposed. The performance of the two QRS detectors are evaluated, demonstrating competitive detection accuracy at minimal hardware overhead.

- Chapter 6 proposes a novel DC-input front-end with high input impedance, which is especially suitable for dry electrodes use. The wireless sensor design extends the applications of the event-driven concepts in Chapter 5 to wireless transmission. Including a ultra-wideband transmitter and an on-chip antenna, the entire system consumes less than 3 μW when transmitting full-rate ECG data.

Chapter 7 summarizes and concludes the thesis with some ongoing and future work descriptions.

The main contributions of the presented work includes the following aspects, with each targeting the mentioned design challenges in Section 1.2.

1. **Low Noise and Low Distortion**

In the first part of the thesis, the main contribution is on the low-noise front-end amplifiers. Design considerations for thermal and flicker noise optimizations are introduced, especially at the first stage. To fulfill the bandwidth requirements of ECG analysis, different filtering topologies are evaluated. Also the output harmonics are much reduced by optimizing the filter feedback loop configurations at different stages.

2. **Low Data Rate**

   Instead of merely optimizing the amplifier's power consumption, a more effective approach is to minimize the output data rate, and hence reduce the wireless power. The second part of the thesis presents a power-efficient event-driven analog-to-digital converter (ADC) with intrinsic data compression. The ADC digitizes the ECG output in continuous-time (CT) domain, and samples the signal only when the input changes. A more aggressive data compression scheme is also included when only the heart rate instead of raw ECG data is required, and the proposed two nanoWatt ECG QRS detectors prove several benefits of low-power continuous-time signal processing at the sensor side.

3. **High Input Impedance**

   Two front-end designs with high input impedance are also included in the thesis, aiming for dry electrode applications. One design uses an extra current feedback loop to reduce the current drain from the electrodes. Another completely redesigned front-end adopts a DC-input structure, and minimizes the input offset through various approaches including electrode shielding and filtering. Moreover combined with event-driven ADC and UWB, the DC-input ECG sensor demonstrates the lowest power for full-rate wireless transmission, which is one magnitude lower than the state-of-the-

art designs.

4. **Biomedical Acquisition Beyond ECG**

   Other vital signs including the respiratory condition and the thoracic blood flow are monitored using a reconfigured front-end with low bandwidth requirements for the operational amplifier, making the designs great candidates for multi-parameter wearable sensors.

1.4 List of Publications

Listed below are the publications related to the work in Chapter 3 and 5. Papers on the remaining contents are in preparation.

[1] X. Zhang and Y. Lian, "A 300-mV 220-nW event-driven ADC with real-time QRS detection for wearable ECG sensors," in *IEEE Trans. Biomed. Circuits Syst.*, vol. 8, no. 6, pp. 834-843, 2014.

[2] M. Khayatzadeh, X. Zhang, J. Tan, W.-S. Liew, and Y. Lian, "A 0.7-V 17.4-μW 3-lead wireless ECG SoC," in *Biomedical Circuits and Systems Conference (BioCAS), 2012 IEEE*, Nov 2012, pp. 344-347.

[3] M. Khayatzadeh, X. Zhang, J. Tan, W.-S. Liew, and Y. Lian, "A 0.7-V 17.4-μW 3-lead wireless ECG SoC," in *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 5, pp. 583-592, 2013.

[4] C. J. Deepu, X. Zhang, W.-S. Liew, D. L. T. Wong, and Y. Lian, "An ECG-SoC with 535nW/channel lossless data compression for wearable sensors," in *Solid-State Circuits Conference (A-SSCC), 2013 IEEE Asian*, 2013, pp. 145-148.

[5] C. J. Deepu, X. Zhang, W.-S. Liew, D. L. T. Wong, and Y. Lian, "An ECG-on-Chip with 535-nW/Channel Integrated Lossless Data Compressor for Wearable Sensors,", *IEEE J. Solid-State Circuits*, Accepted, 2014

[6] X. Zhang, C. J. Deepu, W.-S. Liew, D. L. T. Wong, X. Xu, and Y. Lian, "A 13.4 μA ECG and Respiratory Rate Acquisition SoC for Wearable Sensor Applications", journal paper under preparation.

[7] X. Zhang, Z. Zhang, Y. Li, C. Liu, Y. Guo, and Y. Lian, "A 2.89-μW Fully Integrated UWB Event-Driven ECG Sensor for Dry Electrode Use", journal paper under preparation.

[8] X. Zhang, C. J. Deepu, W.-S. Liew, and Y. Lian, "A 10-μA Biomedical SoC for High-Impedance 3-Lead ECG and Thoracic Impedance Monitoring", journal paper under preparation.

[9] X. Zhang, Z. Zhang, Y. Li, C. Liu, Y. Guo, and Y. Lian, "A 2.89-μW Fully Integrated UWB Event-Driven ECG SoC", conference paper under preparation.

CHAPTER 2

Analog Front-End for ECG Signal Acquisition

This chapter introduces low-noise front-end amplifiers for ECG sensors. The front-end amplifier is one of the most critical parts in the ECG sensor system, and it often determines the system's noise and distortion, which deserves significant design efforts. Starting with a brief introduction to the ECG signal and the acquisition system, this chapter discusses the basic analog front-end architecture, with reviews of recently published low-noise biomedical amplifier designs. Next, several design considerations are shared, with highlights on a chain-like input configuration for multi-lead ECG, and evaluations of various on-chip resistor implementation approaches. Two ECG sensor front-end designs in 0.35-μm and 0.13-μm technology are introduced in the end.

2.1 ECG Basics

The design of a better ECG sensor starts with understanding the basic of ECG. Fig. 2.1 illustrates the basic ECG waveform. In each normal cardiac cycle, there

are five important waves or complexes, marked as P, Q, R, S, T respectively. A small deflection called U wave may also follow the T wave as shown. As given in Fig. 1.3, those complexes represent the cardiac muscle cells' depolarization and repolarization within each heart beat [5]. The P wave represents the begin of depolarization process for sinus or sinoatrial (SA) node. For health subjects, the SA node is also the pacemaker tissue of the heart, with an intrinsic frequency about 70 beats per minute. Following the P complex, the much larger and sharper QRS complex origins from the depolarization of the ventricles, or generally the heart contraction. Next to the QRS, the T wave stands for the repolarization of ventricles. The time intervals between complexes, such as PR interval or QRS interval, are reliable variables showing the conduction velocity between different nodes. In particular, the interval between two consecutive R peaks, or R-R interval, is the time duration of one heart beat, and hence is used to calculate the instant heart rate. In general, those intervals or segments contains critical evidences for reliable diagnosis.

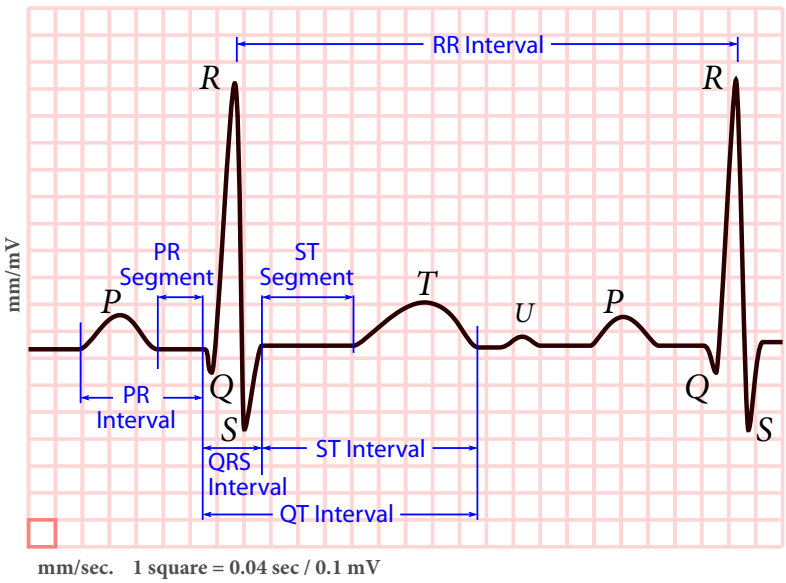

Figure 2.1: ECG basics for diagnosis.

The power spectrum of the ECG provides further information on ECG

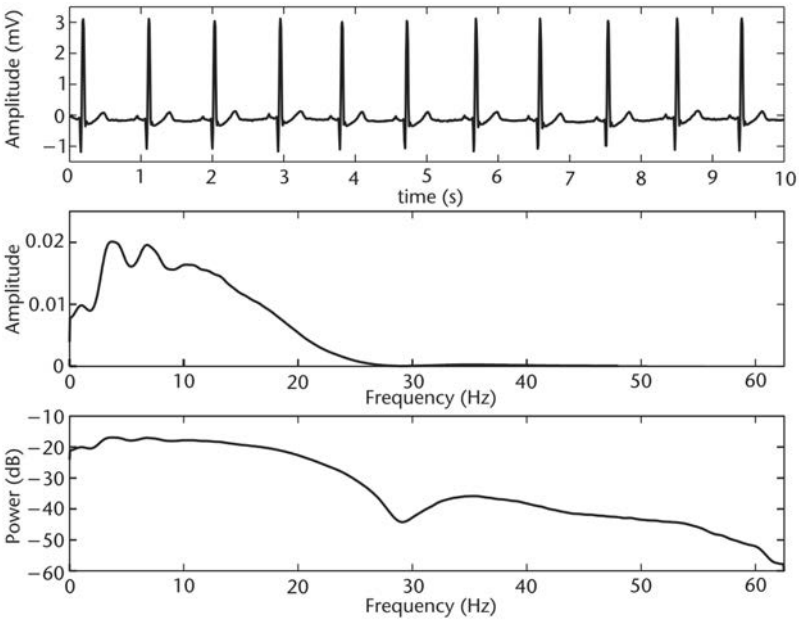

Figure 2.2: Lead II ECG and associated linear and log-linear periodograms.

characteristics. Fig. 2.2 shows a 10-second normal sinus rhythm (NSR) ECG and its amplitude and frequency estimation from [13]. The ECG amplitude is about several millivolts , with the highest peak often defined by the QRS wave height. The main power for ECG signals concentrate at sub-100-Hz low-frequency region. The peaks shown around 1, 4, 7, and 10 Hz correspond to energies from the heart rate of 65 beat per minute (bpm), T wave, P wave, and the QRS complex. Generally, monitoring ECG frequency is around 0.5 Hz to 75 Hz, while a more stringent requirement for diagnostic ECG may target for a wider bandwidth from 0.05 Hz to 150 Hz [13].

The ECG measurements through adhesive electrodes could be disturbed by several different types of noise and artifacts. The most significant interference is the power-line noise or mains noise coupled from power grids, due to the the alternating current of the AC power supply. The fundamental frequency is 50-Hz (Europe and most of Asia) or 60-Hz (Americas) depending on the countries. Another serious noise is the motion artifacts generated through relative

movements between the skin and the attached electrodes. The movements cause the electrode-skin interface capacitors charging and discharging, and therefore alter the signal baseline from time to time. Similar artifacts also occur due to the nearby muscle activities, or the electromyography (EMG) signals [14, 15]. Last but not least, the sensor circuit noise, especially the flicker noise at lower frequencies from CMOS transistors, is another notable contributor in the captured ECG.

2.2 ECG Sensor and AFE Overview

To obtain clear ECG signals, the ECG sensor is designed to amplify and digitize the ECG traces for further signal processing tasks, and meanwhile suppress various noise and artifacts. Shown in Fig. 2.3 is the system architecture of a typical wireless ECG sensor. The sensor often consists of the analog front-end (AFE) amplifiers, ADCs, digital back-end processors, and wireless transmitters. To sense the ionic current flow from ECG heart activity, one or more biopotential electrodes are used to convert the ion current into electric potentials [16]. After the signal is captured through electrodes, it is first amplified and filtered by one or more front-end amplifiers first, and then quantized by the ADC that follows. The digital processor performs some signal processing tasks such as digital filtering or signal compression, and sends the data out of the sensor node through the wireless transmitters. For multi-lead ECG, the system may include extra amplifiers, multiplexers (MUXs), or ADCs for simultaneous capture. The AFE usually includes more than one amplifiers to perform different signal conditioning tasks discussed as follows.

First, the analog front-end is mainly for signal amplification. Since the input amplitude is only a few millivolts, sufficient gain is required to improve the effective resolution by matching the signal amplitude to the ADC's dynamic

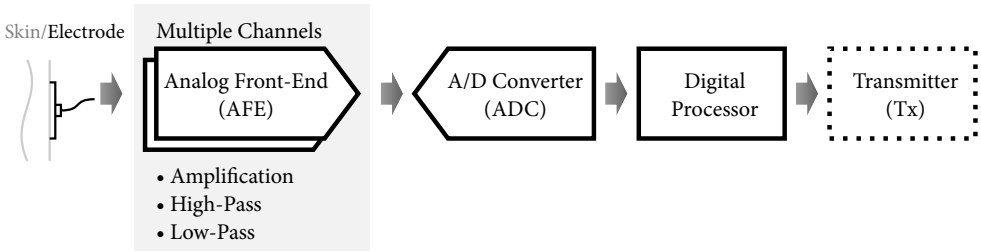

Figure 2.3: ECG sensor system overview.

range. Under 1-V power supply voltage for example, the gain is around 200 within the ECG frequency band. To fit different surface or electrode conditions, programmable gain tuning is highly recommended.

Second, the AFE needs the capability to remove the DC electrode offsets, similar to a high-pass filter. The electrode offset origins from concentration and polarization of ions at the electrode-skin interface. Known as the half-cell potential E_{hf} shown in the electrode model in Fig. 2.4 [17, 18, 19], the potential difference can be up to 200 mV for the widely-used Ag/AgCl disposable wet electrodes, almost two magnitudes higher than the ECG amplitude [20]. The exact value of this electrode offset depends on factors like electrode and electrolyte materials, contact size, resistance, temperature, and etc. An intuitive approach to mitigate the offset is to block the DC completely before amplification at the front-end, because the DC potential carries no information for ECG interpretation. Otherwise if the sensor amplifies the input signal without handling the offset, the amplifier output will quickly get saturated at DC, and lose all the ECG details. Note that although certain designs adopt a low-gain amplifier with high-resolution ADC to compensate the dynamic range loss due to the offset [21], they suffer from high ADC power consumption, and limit the use within specific electrodes with low half-cell potentials.

Last but not least, the front-end would include low-pass anti-aliasing function before the ADC. The ADC samples at around 512 Hz or even lower frequen-

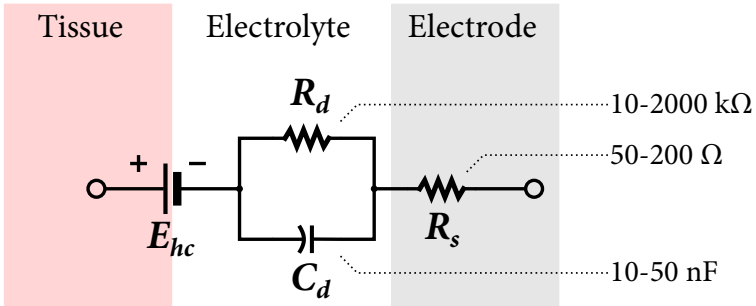

Figure 2.4: Equivalent circuit for a biopotential electrode.

cies, since the major ECG power is below 150 Hz. The noise beyond Nyquist frequency must be suppressed to avoid aliasing errors. For extra benefits, the AFE low-pass filter can attenuate the high-frequency noise and artifacts such as powerline harmonics and certain motion artifacts.

2.3 Instrumental Amplifier Designs Review

Designing a power-efficient high-performance AFE requires reviewing tradeoffs between noise, distortion, power, CMRR, power-supply reject ratio (PSRR), and so on. Of all the possible amplifier stages, the first stage, or the instrumental amplifier (IA) is the bottleneck and the most critical part, as it determines the AFE noise level and common-mode rejection performance. This section lists representative architectures of instrumental amplifiers for biomedical applications. Following discussions on the basic model, prior research efforts on the AFE designs are highlighted regarding each type.

2.3.1 AC Coupling

The AC-coupled or capacitively-coupled instrumental amplifier is widely used for biomedical applications due to its simplicity and power efficiency. Fig. 2.5 shows the simplified AC-coupled IA, which includes an operational amplifier (OPA), a

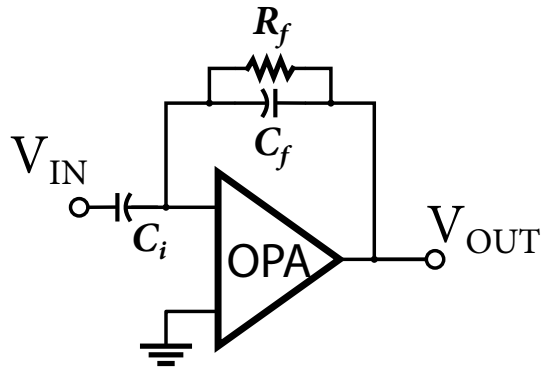

Figure 2.5: AC-coupled or capacitively-coupled instrumental amplifier.

resistor, and two capacitors for the single-ended design. Assuming an ideal OPA, the transfer function of the instrumental amplifier is given by

$$A_{IA} = \frac{V_{OUT}}{V_{IN}} = \frac{j\omega R_f C_i}{1 + j\omega R_f C_f} \tag{2.1}$$

which is basically a high-pass filter with passband gain of $G = C_i/C_f$ and 3-dB cut-off frequency at $f_H = 1/(2\pi R_f C_f)$. The OPA itself contains an intrinsic low-pass cut-off at the bandwidth frequency f_L. Therefore, designers can tune the G, f_H, f_L independently to achieve the design target.

One limit for fully integrated silicon implementation of the above design for ECG acquisition is the chip area. Given a high-pass corner frequency of 0.05 Hz as the target, the resistor R_f and the capacitor C_f at the IA feedback path are too large in area to be on chip. While there are no effective alternatives for capacitors, a feasible solution would be to generate up to $G\Omega$ resistance using transistors by limiting the current to sub-pA. More specifically, given the C_f is about 1 pF, the effective resistance R_f must be over 3 $T\Omega$.

Past years has seen notable research efforts on the issues for low-power AC-coupled IA for biomedical signal acquisition, including the mentioned $T\Omega$ on-chip resistor structures. Before 1990s there were already micro-power designs on biomedical amplifiers [22]. In particular, [23] introduced the noise efficiency

factor (NEF) to evaluate the noise given the same current and bandwidth for various architectures, compared to an ideal bipolar amplifier. The NEF is defined as

$$NEF = v_{ni,rms} \cdot \sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \tag{2.2}$$

where $v_{ni,rms}$ is the input-referred noise, I_{tot} is the total current and BW is the amplifier's bandwidth. Compared to the CMOS-based designs, the bipolar amplifiers do not suffer from the low-frequency flicker noise or 1/f noise, and those IA designs are occasionally used in modern CMOS technologies through the lateral structures [24].

[25] proposed the popular MOS-bipolar pseudo resistor to achieve up to $10^{12}\Omega$ resistance for small inputs. The pseudo resistor consists of two diode-connected PMOS transistors, with current conducting through the parasitic bipolar transistor [26]. By limiting the current, the IA in [25] achieved a high-pass corner of 0.025 Hz. This initial architecture of pseudo resistors and its variances were widely used in many AC-coupled designs [27, 28]. [29] adopted a slightly changed symmetrical pseudo resistor design. To control the resistance value more accurately, [30, 31, 32] proposed a balanced tunable pseudo resistor to achieve high dynamic range and low signal distortion, where the gate voltage is changed relative to the transistor bulk potential. Simplified tunable pseudo resistors through the gate voltage were used in several designs such as [33]. Recently [34] also gave an example of the T-connected pseudo resistor to optimize cut-off frequency. Other than the pseudo resistor implementations, [35, 36] used an active feedback with a Miller integrator to suppress the low-frequency inputs. Recently [37] also provided summaries for the pseudo resistors. A more detailed analysis on high-resistance implementations are included in Section 2.4.3.

Besides the efforts on DC suppression, many worked on improving the signal quality and reduce the noise, especially the powerline 50-/60-Hz noise and

motion artifacts. The interference and artifacts had caught early attentions back to 1970s [38, 39, 40]. [41, 42] included a dedicated 50-/60-Hz powerline interference cancellation feedback based on a fully-differential capacitively coupled amplifier. The feedback signal is also AC-coupled and subtracted from the input, from a sinc anti-aliasing filter to place notches precisely at the interference frequencies. The digital-assisted sensor interface mitigates the interference at the input stage and avoids amplifier saturation. On the other hand, since higher input impedance could partially mitigate motion artifacts [43, 44, 45], designs like [46, 47] worked in this direction and also for dry or non-contact electrodes ECG sensing. At the circuit levels, designers are also making efforts to improve the power efficiency of AC-coupled IAs. Current reuse is one of the most popular techniques beside subthreshold design. Examples include sharing current branches between adjacent channels [48], or sharing within the amplifiers output stages [49].

2.3.2 Chopper Stabilization

Chopper stabilization (CHS) is a common technique to reduce amplifier $1/f$ noise and input offsets [50, 51]. As illustrated in Fig. 2.6 redrawn from [50], the input signal is modulated to higher frequencies and chopped back in latter stages. Since the input is modulated twice under the same clock frequency while the noise and offset only once, at the output the power of $1/f$ noise and offset will concentrate around the clocking frequency and its harmonics, which can be easily cut by the following filters. The CHS technique is gaining its popular in recent years due to its almost-digital architecture and compatibility with technology scaling, with major application areas including precise DC instrumental amplifiers like temperature sensors [52].

One major problem using the CHS IA directly for biomedical signal acquisition is, again, the DC offset of the ECG signal. The differential DC input

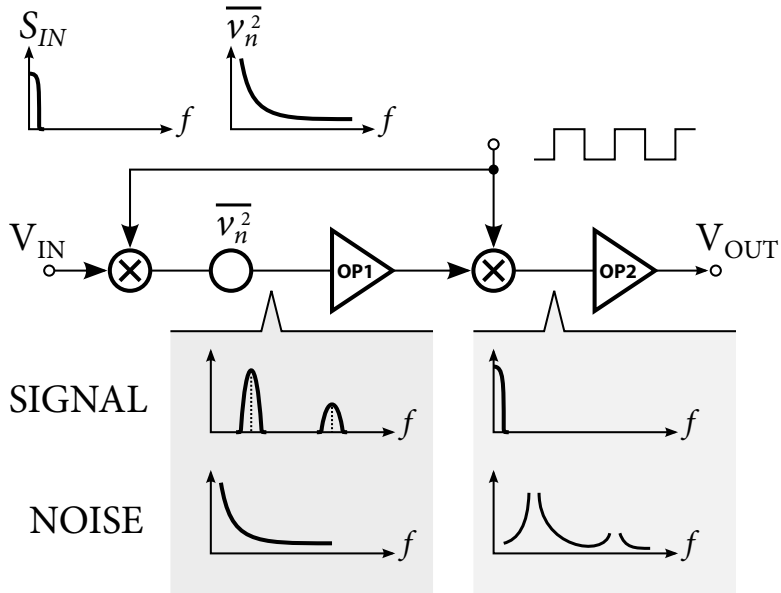

Figure 2.6: Chopper Stabilization concept.

between electrodes is much larger than the signal amplitude and will saturate the amplifier. There are several ways to suppress or eliminate the DC offsets. The first one is chopper-stabilized capacitive-coupled (CC) instrumentation amplifiers, combining the DC blocking benefit from pure AC-coupled IAs. For example, [53] used modulation feedback to cancel the residual error caused by limited amplifier gain bandwidth. Also the front-end gain is set by the capacitor ratio from another ac feedback for its noise and linearity advantages. For the feedback path, [54] used pseudo resistor to improve the high-pass corner, while [55] used switched-capacitor to achieve large resistors. A similar capacitively-coupled chopper instrumentation amplifier with impedance boosting feedback loop and ripple reduction loop is implemented in [56] under more advanced technology. To improve the input offset tolerance, an extra DC servo loop is added in the improved designs [57] to remove the input offsets, which is continuously improved in recent IAs like [58]. The second approach is to use current-feedback chopper-stabilized IAs [59, 60]. Further improved designs focused on large electrode offset

rejection [61] using fine and coarse filters at the feedback path. [62] adopted a multi-path chopper topology to eliminate the transfer function notch caused by the ripple reduction loop. Meanwhile, the power efficiency for multi-function biomedical system was improved through multiple output stage sharing and event-driven adaptive sampling [63, 64] In recent years, such feedback control loops for high-pass cut-off control and common-mode rejection calibrations were moved gradually into digital domains [65, 66, 67]. Active electrodes discussed in [68, 69, 70] also focused on the back-end common-mode rejection improvement through proper feedbacks and digital calibrations.

2.3.3 Others

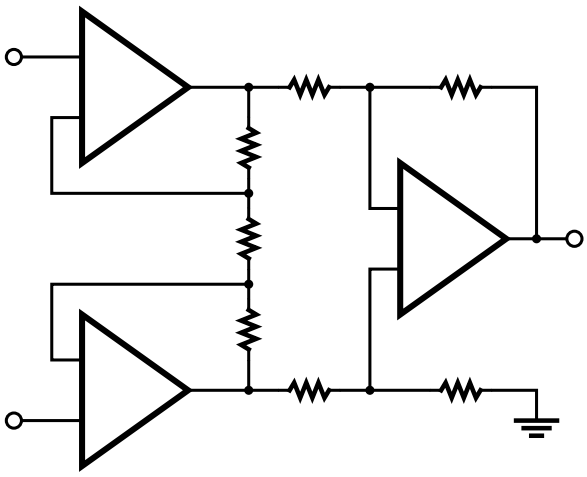

Figure 2.7: 3-OP instrumental amplifier.

Most discrete or commercial designs [21, 71] choose the 3-OP architecture printed in Fig. 2.7. It has high input impedance and common-mode rejection ratio, at the cost of higher power consumption and limited integration level. But recently instrumental amplifiers with DC direct inputs have gain popularity due to its high input impedance. For example, a DC-coupled design for neural signal acquisition proposed in [72] features offset cancellation through feedback similar

to [41], and calibrations for gain and input mismatch. Chapter 6 in this thesis will also introduce a feedback-free DC-coupled AFE design.

There are also notable work featuring architectures targeting for reasonable performance and power efficiency. Complementary-input instrumental amplifiers in [73, 74] improve the current efficiency at the input pair by introducing another input and increasing the transconductance. Open-loop designs could further save the current at the cost of imprecise gain and reduced power supply noise rejection. [75] uses 3-stage open-loop amplifiers and demonstrates good energy efficiency for miniaturized neural sensor. To meet a more stringent noise requirement, designs like [76] uses multiple stages combining the chopper stabilization techniques with capacitively-coupled transimpedance amplifier. As a current-mode amplifier, it achieves good noise and linearity performance at the cost of higher power.

Table 2.1 gives an performance overview of selected AC-coupled and chopper-stabilization instrumental amplifiers. This thesis will mainly focus on the AC-coupled designs, which are quite suitable for energy-constrained sensor applications.

2.4 Analog Front-End Design Considerations

This section discusses the system-level architecture for multi-lead input ECG sensors and the implementation of on-chip high-value resistor using pseudo resistors. The chain-like connection for multi-channel system is first introduced for its input sharing feature. Next, various pseudo resistors are evaluated for its resistance and linearity.

Table 2.1: Performance Summary of Recent IA Designs

AC-Coupled	[25]	[29]	[28]	[31]	[41]	[42]	[9]	[34]
Technology (μm)	1.5	0.35	0.5	0.35	0.18	0.18	0.13	0.18
Power Supply (V)	± 2.5	0.8-1.5	2.8	1.0	1.5	0.6	1.2	1.8
Current (μA)	16	2.3	0.74	0.34	0.86	1.92	4.0	29.8
Gain (dB)	39.5	40.2	40.9	45.6-60	37-82	34.5-69.4	40-78	41-61
Bandwidth (Hz)	0.025-7.2k	0.003-245	0.4-295	0.005-292	0.12-100	0.02-156	-320	0.1-7k
Input-Referred Noise (μV_{rms})	2.2	2.7	1.66	2.5	3.4	3.44	2.0	5.23
CMRR (dB)	83	64	66	71.2	60	70.4	70	–

Chopper Stabilization	[77]	[55]	[57]	[69]	[65]	[78]	[79]	[66]
Technology (μm)	0.5	0.18	0.065	0.18	0.18	0.18	0.18	0.18
Power Supply (V)	2.0	1.0	1.0	1.8	1.2	1.2	1.8	1.2
Current (μA)	5.3	3.5	1.8	11	5	14.2	1.08	13.3
Gain (dB)	49.5-62.5	60	40	40	40	37.5-49.5	26-53	–
Bandwidth (Hz)	-170	0.5-100	0.5-500	-1k	0.2-200	-250	1-100	–
Input-Referred Noise (μV_{rms})	1.1	1.3	0.67	0.8	1.3	1.0	2.2	0.61
CMRR (dB)	105	60	134	82	120	100	100	110

2.4.1 Chain-Like Input Configuration for Multi-Channel ECG

As discussed previous in Chapter 1.1, the single-lead ECG is often inadequate for comprehensive heart diagnosis due to its limited dimension. To simultaneously capture multiple ECG signals, more than one analog front-end channels are needed. One problem with multi-channel sensors is the number of inputs. Differential inputs for each channel is preferred for its common-mode suppression. Therefore in a N-channel system, at least $2N$ inputs are required, occupying many input pins and adding cumbersome for lead connections.

The following designs propose the chain-like input connection configuration. Each channel's inputs are shared with the two adjacent channels. Effectively, there are only one input for each amplifier channel. For 12-lead ECG especially, there are only 8 independent channels, i.e. 6 chest leads V_1 through V_6 and any two from limb or peripheral leads L1/L2/L3. Shown in Fig. 2.8 is the configuration for 12-lead ECG. All the 12 leads can be directly calculated from the 8-channel outputs, using as few as 9 input cables for connections. Similarly a 3-lead ECG sensor may only require 2 independent channels and 3 inputs.

To further improve the suppression of common-mode artifacts or mains interference, a special amplifier marked as driven-right-leg (DRL) is included. The DRL extracts the common mode from ECG inputs and drives the body potential through the negative feedback, normally via the Right Leg (RL) electrode. As only the common-mode signals are fed back, no ECG outputs are affected by the DRL loop. With a proper feedback loop gain, the sensor will suffer less from the common-mode noise and benefit from clearer ECG waveforms.

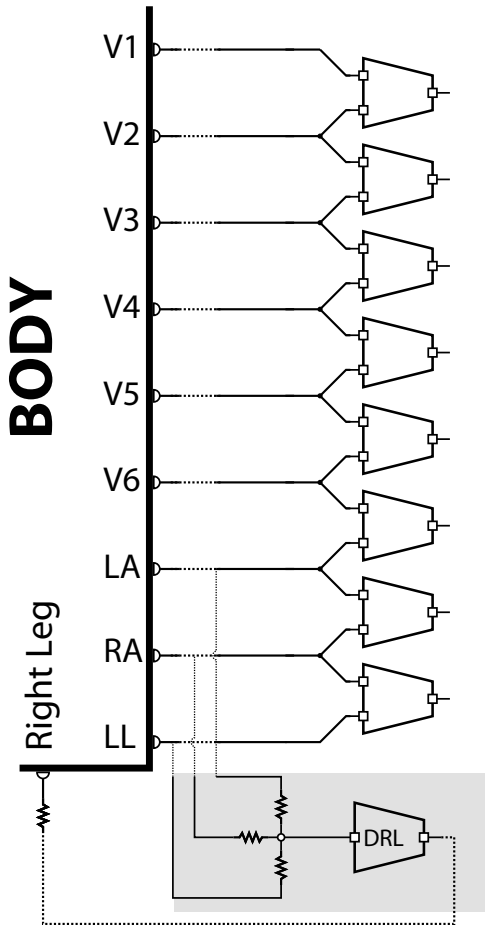

Figure 2.8: The chain-like connection for a 12-lead 8-channel ECG acquisition system.

2.4.2 Isolated Gain Control

Among the architecture introduced in Section 2.3, most designs proposed are capacitively-coupled front-ends. The capacitively-coupled AFEs are power efficient and effective in removing offsets and artifacts without additional feedbacks. Also the input impedance is naturally high for AC-coupled IAs.

To achieve the desired gain and bandwidth control, it is common to implement the AFE through multiple stages. Fig. 2.9 shows the entire analog front-end, including an instrumental amplifier, a programmable-gain amplifier (PGA), and an buffer (BUF). The IA has been discussed in previous part for its DC-blocking

and high-pass filtering. Tunable gain is achieved by the PGA changing the feedback capacitor value C_{f2} via digital controls. The output buffer would improve the signal settling time for the ADC sample-and-hold (S/H). Using a standalone gain stage helps improve the AFE's linearity and low-pass filter roll-off, compared to a single low-noise amplifier with over 60 dB close-loop gain. Also since the anti-aliasing filter is implemented through the operational amplifier's bandwidth roll-off, a higher-order low-pass filtering would much reduce the noise folding, which is made possible by multiple amplifiers in the signal path.

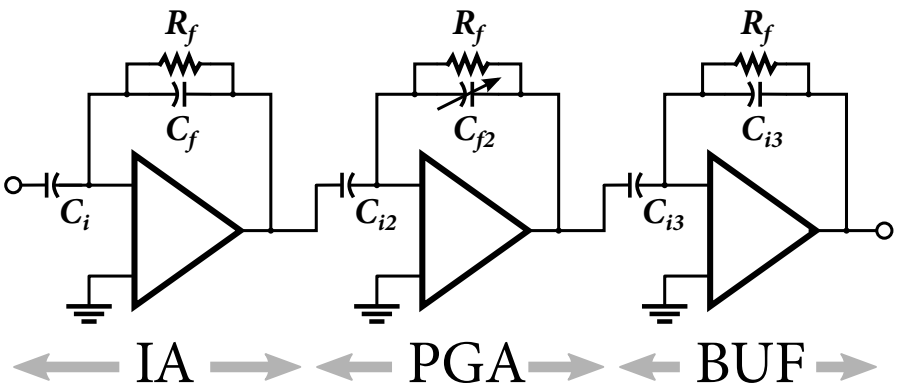

Figure 2.9: AC-coupled AFE, with IA, PGA and optional output buffer.

2.4.3 Pseudo Resistors

To remove the electrode offsets, the passive RC filter is favored due to its simplicity and limited noise affects. Because the ECG frequency around 0.5 Hz is useful for diagnosis, the high-pass cut-off frequency is targeted at 0.1 Hz or below. Given that normal on-chip metal-insulator-metal (MiM) capacitance C is around several picofarads, a resistor beyond GΩ is needed, which is challenging for on-chip integration. Instead of using traditional resistors provided by the design kits, pseudo resistors from MOS transistors are a common choice. This section explains the use of pseudo resistors in both the instrumental amplifier and

the programmable-gain amplifier. Through the discussion, designers are able to choose the suitable pseudo resistors for the biomedical sensor front-end systems.

Up to 32 pseudo resistor structures are benchmarked, using the same width and length in 0.35 um CMOS technology. While some of the designs like 1 and 10 are from previous work, most are new variations. Design 3, 4, 11, 14 are tunable pseudo resistors and the voltage sources are set at 0.1 V. The evaluation focuses on the resistance value as well as linearity, i.e. the variation of the resistance regarding the voltage applied. For simplicity, only symmetrical designs are involved.

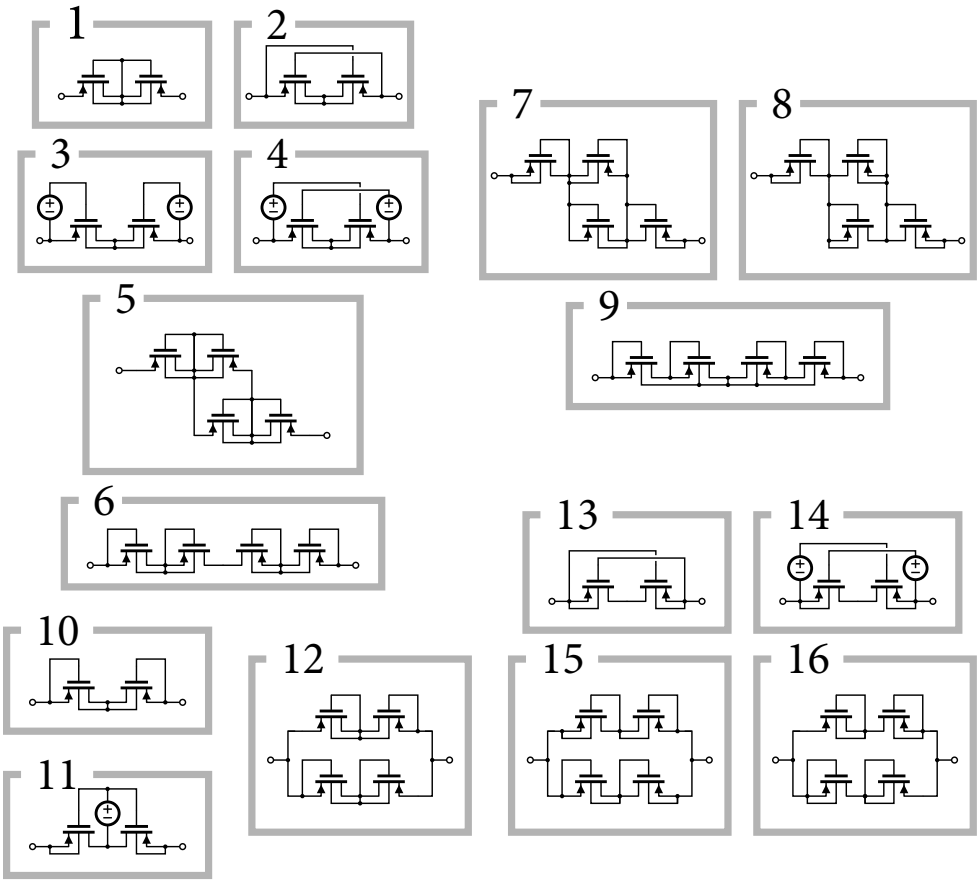

Figure 2.10: Pseudo resistors with symmetrical characteristics

The simulated results are summarized in Fig. 2.11. X-axis stands for the effective resistance for large amplitude input, when the voltage applied ΔV is 1.5 V, and then Y-axis is the resistance under $\Delta V = 0.15V$ for small input. Ideally for

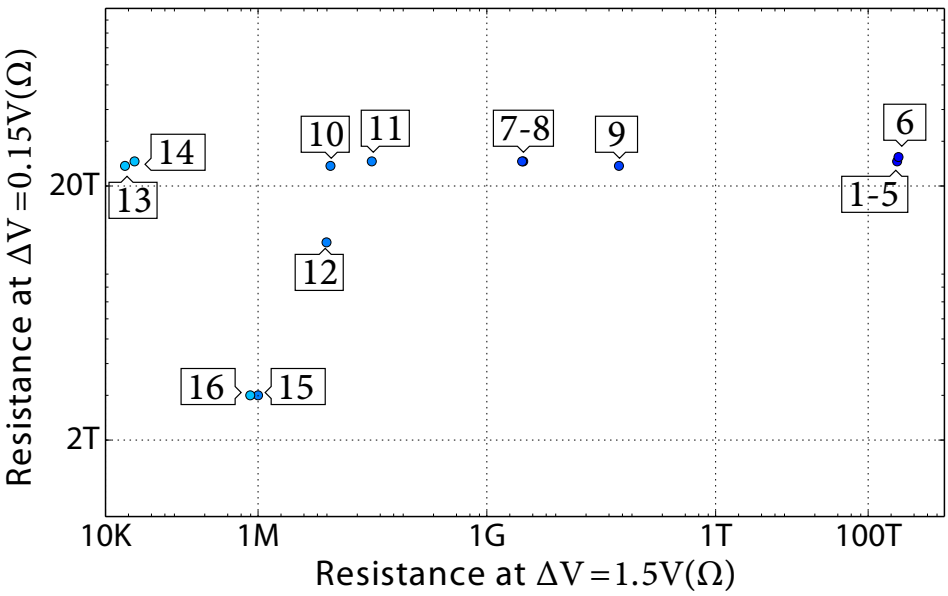

Figure 2.11: Pseudo resistors performance summary.

a passive resistor the x and y value are the same. But designs with large resistance only at small input scenarios is still a reasonable choice at the IA stage, when the signal amplitude is still limited. Below gives further analysis.

1. Design 1-6 have over 100 $T\Omega$ at large amplitude but around 20 $T\Omega$ for small input. The very high impedance makes them good candidates for all input stages, especially the PGA and output buffer where the output could be close to rail-to-rail. On the other hand, when the ECG baseline at the IA stage drifts way, it takes longer time to get the baseline settled to the center, as a result of the large time constant. This is in the end a disadvantage to deploy design 1-6 into the first stage.

2. Design 7-9 have the similar performance, with large-input resistance smaller than design 1-6. But as the current flowed through the pseudo resistors is still less than 1 nA at the 1.5 V voltage, these designs are unlikely causing loading for any stages. So the output linearity is not affected. Also given the current at large input amplitude is about 4 orders higher than the small-

input current, with design 7-9 at IA the baseline settles much faster after motion artifacts or electrode re-applying procedure.

3. Design 10-16 are generally unsuitable for PGA or buffer stages as they draw large current when the output amplitude is high. They can only be used for IA stages. The ECG baseline is settled much more quickly at the IA output.

Many of the pseudo resistor designs discussed can be used for AC-coupled biomedical front-end amplifiers. Certain designs suffer from large current drain when the output amplitude is large, which makes them not suitable in the PGA or BUF stages. On the other hand, they can still be used in the IA stage where the signal power is small without output loading.

2.5 Design Examples and Measurement Results

This section introduces two low-power front-end circuit examples in 0.35-μm and 0.13-μm technology respectively. The 0.35-μm design contains 8 standalone ECG front-end channel for the standard 12-lead ECG monitoring. Separate pseudo resistors are used in the IA and PGA stages to guarantee sub-0.1-Hz high-pass corner and low harmonic distortions. Meanwhile, the 0.13-μm sensor is a 3-lead ECG wireless sensor with the total power consumption limited within 0.5 μW for each channel. This design is aimed at self-powered wireless sensors where the power budget is extremely restricted.

2.5.1 ECG Analog Front-End in 0.35 μm

Similar to the one introduced in Section 2.4.2, the proposed architecture for a single capacitively-coupled ECG channel is given in Fig. 2.12. The IA stage gain is 50 and PGA gain tunable from 5 to 40. Therefore the overall amplification gain is

selected among 250/500/1000/2000 through a 2-bit control $G < 1 : 0 >$. Another digital control signal LPF changes the low-pass cut-off frequency for the PGA stage. To improve common-mode suppression, the IA chooses fully-differential structure. Two different types of pseudo resistors are used in the IA and PGA stage. As analyzed in Section 2.4.3, the pseudo resistor A has similar performance as design 7 in Fig. 2.10, and is suitable for the input stage with small signal amplitude. When the baseline voltage is far from the circuit common mode, the effective resistance for this pseudo resistor drops sharply and speeds up baseline recovering. The pseudo resistor B contains two copies of design 10 in serial with extended high resistance range. It does not drain excessive current at the output even at the power rail.

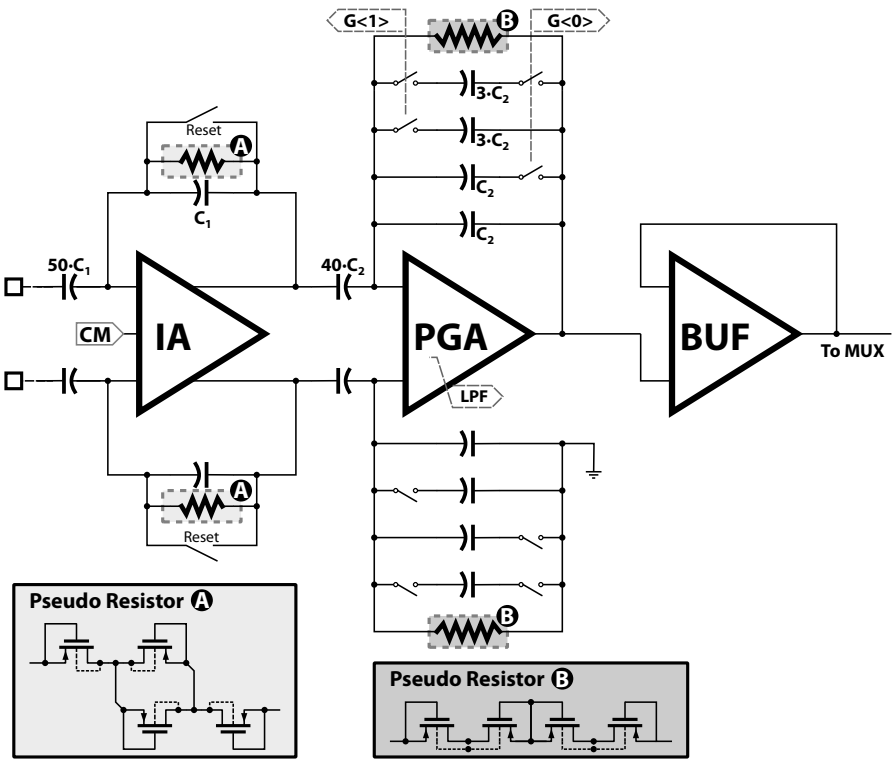

Figure 2.12: The ECG front-end amplifiers with dedicated pseudo resistors for IA and PGA.

The two-stage fully-differential amplifier used in the first stage is in Fig. 2.13.

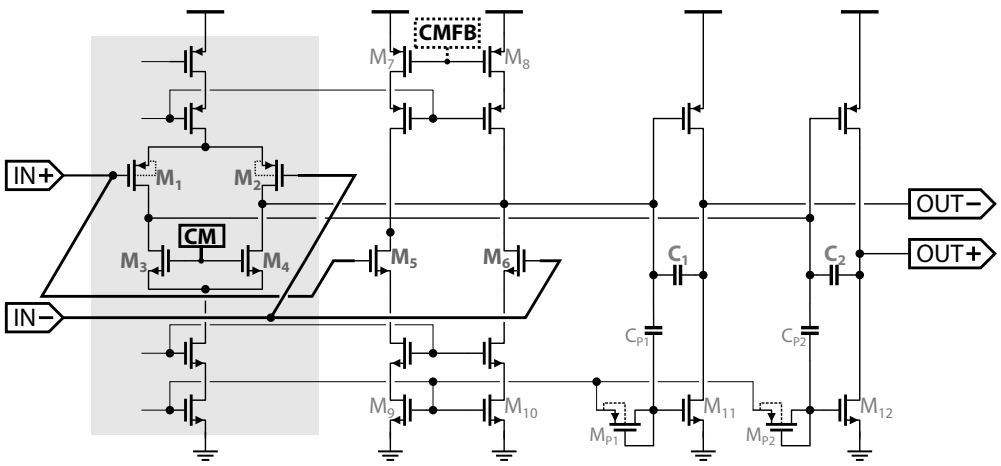

Figure 2.13: The 2-stage amplifier used for IA.

To improve the power efficiency, all the input pairs are in the subthreshold region. Both PMOS ($M_{1,2}$) and NMOS ($M_{5,6}$) are used for input pairs, which avoids locking of the amplifier when the input accidentally drives the input pair out of the normal working region. Also the effective transconductance is increased. A common-mode feedback (CMFB) circuitry controls the tail current mirror ($M_{7,8}$). The output stage uses quasi-floating gate (QFG) transistors ($M_{P1,11}$ and $M_{P2,12}$) [80, 81] to take advantage of the high output slew rate from class-AB operation.

Fig. 2.14 shows the PGA amplifier. The LPF signal is used to control the effective transconductance g_m. When LPF is on, the g_m will change to its 1/5 value using degeneration through $M_{3,4}$. Since the miller capacitor C_M does not change, the gain-bandwidth product (GBW) will drop accordingly, reducing the low-pass roll-off frequency of the PGA stage.

The entire system also includes a SAR-ADC, a digital back-end (BE) for SPI control and data processing, and accessory blocks like bandgap reference (BGR) and crystal oscillator (XTAL) driver. The total die area is 3.4 mm by 2.8 mm, with the die photo given in Fig. 2.15. Each ECG channel consumes about 4.25 μA current under 3 V supply. The total harmonic distortion for 10 harmonics is about 0.05 %. The ECG pass-band gain is tunable between 47.8 dB and 65.5 dB through

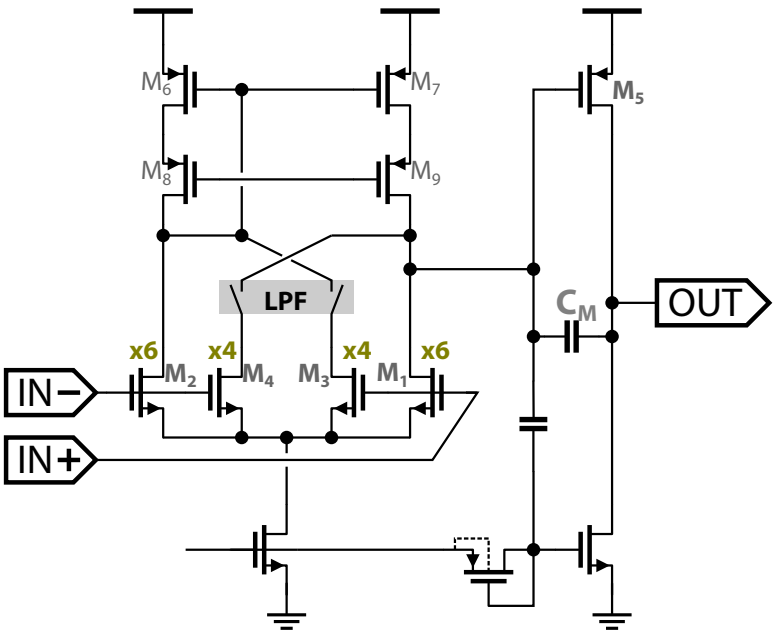

Figure 2.14: The amplifier in the PGA stage.

digital SPI controls. 3-dB high-pass cut-off frequency is less than 0.05 Hz, and the low-pass corner can be also adjusted from the lowest of 68 Hz to 345 Hz. The PSRR is 101.0 dB, and the CMRR is 106.5 dB.

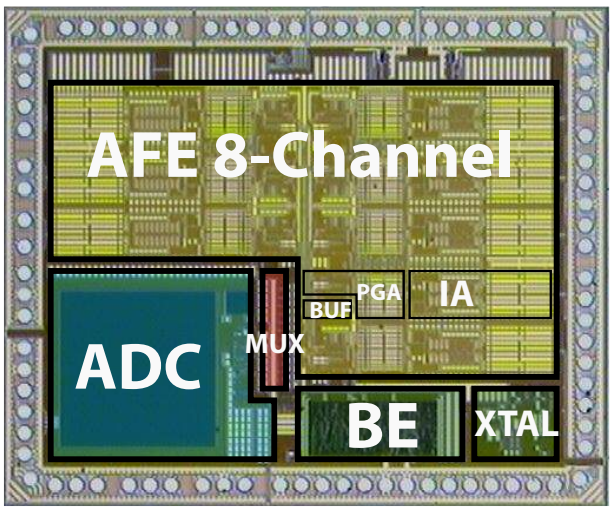

Figure 2.15: Die micro-photograph for the 0.35-µm 8-channel ECG sensor.

2.5.2 ECG Analog Front-End in 0.13 μm

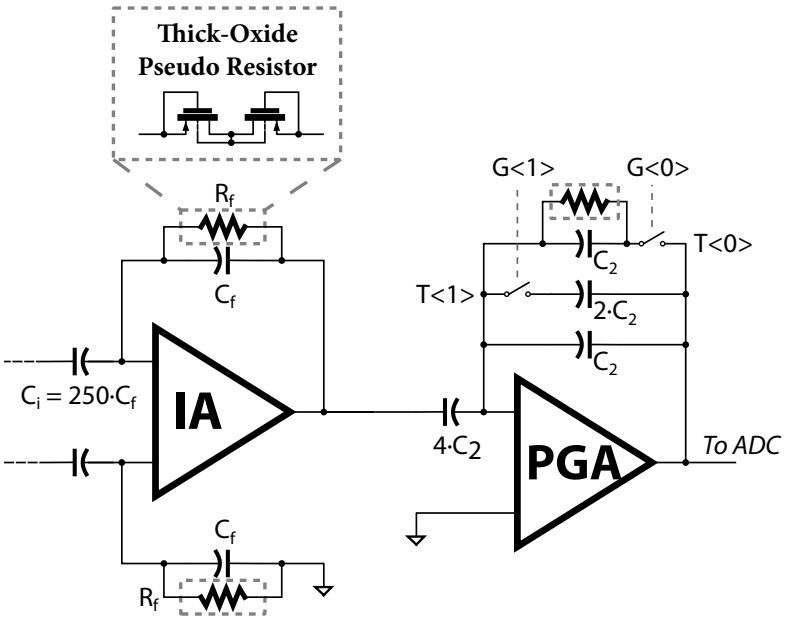

Figure 2.16: The 0.13 μm AFE design with IA and PGA.

The second design at 0.13 μm pushes the supply voltage and power consumption to its limit. Fig. 2.16 gives the front-end design with an instrumentation amplifier and a programmable-gain amplifier. To improve the power efficiency the output buffer is not included. The front-end was designed for a low-power programmable wireless 3-lead ECG sensor [82, 83], also including a successive approximation (SAR) ADC, a custom-designed microcontroller (MCU), two 16-kb static random-access memory (SRAM), and a Medical Implant Communication Service (MICS) band transceiver.

The IA uses capacitive-coupled structure for its low-power dissipation and simplicity. To mitigate low-frequency baseline fluctuations and ECG electrodes offsets under 0.67 Hz [84], high impedance pseudo-resistors are required. Unfortunately under 0.13-μm CMOS process, conventional nominal-threshold pseudo resistors given in Section 2.4.3 and Fig. 2.10 are insufficient due to the increasing

leakage current. Using those designs, over 100 pF capacitance is required for the AFE to achieve sub-0.67 Hz high-pass cut-off, which takes too much area. To solve this problem, this design uses two high-threshold thick-oxide PMOS transistors for the pseudo resistor. Post-layout simulation shows the resistance is boosted from 4.9 GΩ to 583.1 GΩ by changing the nominal-V_{TH} PMOS transistors to thick-oxide ones, illustrated in Fig. 2.17.

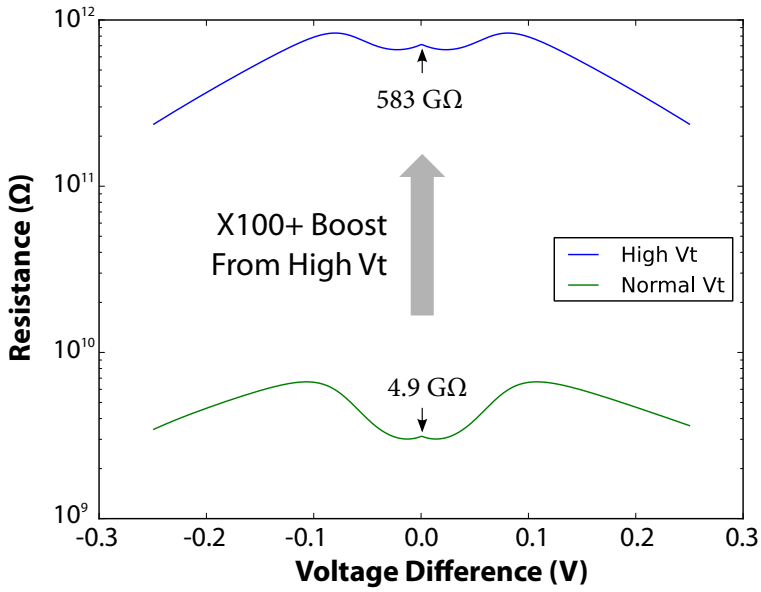

Figure 2.17: The high-V_{TH} pseudo resistor versus normal V_{TH} one.

Thick-oxide transistors are also used in the differential pair of the instrumental amplifier stage. The two P-MOSFETs M_{P1} and M_{P2} in Fig. 2.18 are all high-threshold transistors in the kit. Thick-oxide transistors generally have less flicker noise given the same size, and help reduce the sensor noise.

In Fig. 2.19 the schematic of the DRL circuit is provided. The main function of DRL is to suppress the mains interference from the power supply, through active feedback loop connected at the right-leg electrode. The DRL sums up the 3 lead inputs, extracts the common mode, and feed it back to drive the RL electrode.

For the best possible power efficiency the supply voltage is set as low as 0.5 V for the AFE. The power consumption under 0.5 V supply is only 0.32 μW for

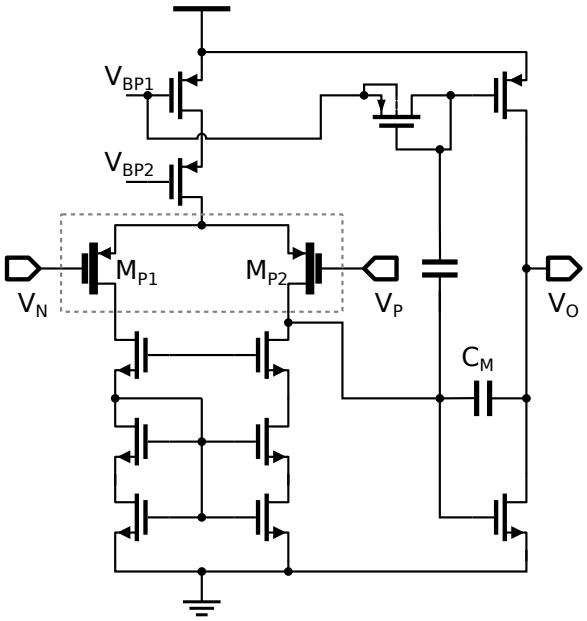

Figure 2.18: The OTA used in the IA.

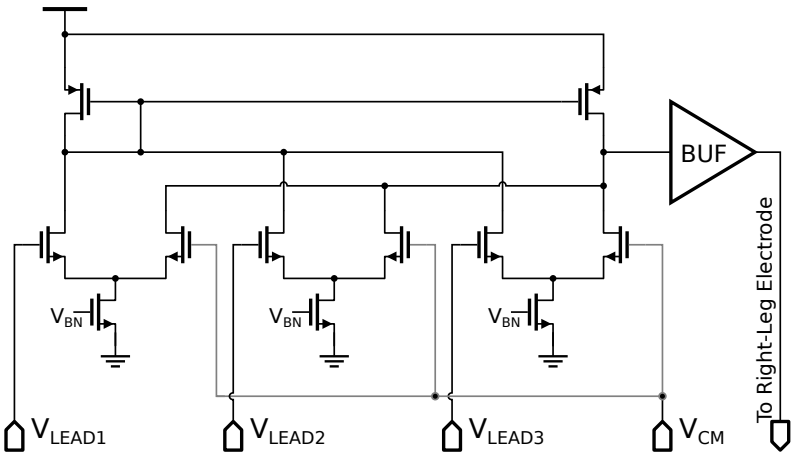

Figure 2.19: DRL circuit used in the designs.

each ECG channel. The AFE functions correctly under 0.45 V to 1.0 V power supply. Given in Fig. 2.20 is the die photo for this ECG SoC chip. The system gain is tunable from 36 dB to 44 dB with low-pass cut-off at about 64 Hz, with frequency responses provided in Fig. 2.21. Thanks to the thick-oxide pseudo-resistor configuration, the low-frequency high-pass corner is less than 0.1 Hz. The input-referred noise, integrated from 0.5 Hz to 250 Hz, is 6.9 μV_{rms}. The PSRR is about 70 dB, and the CMRR is 59 dB.

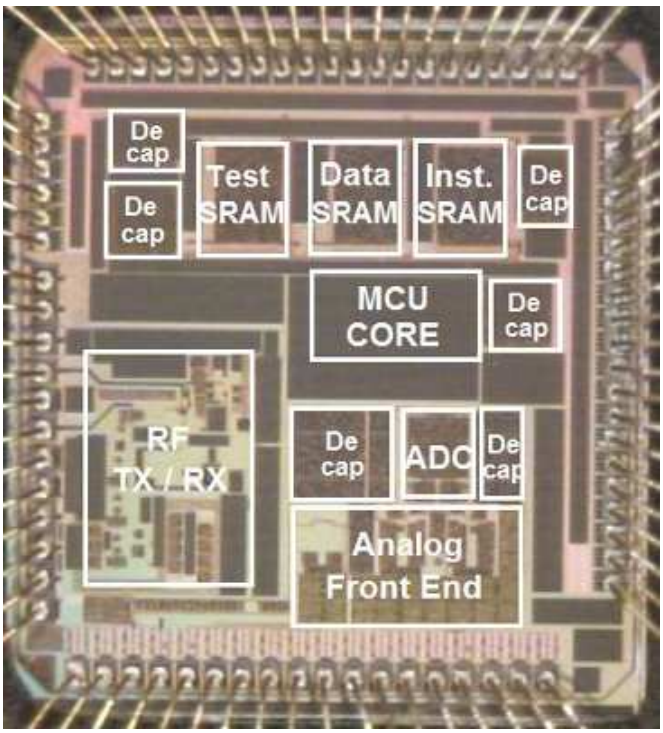

Figure 2.20: Die photo of the 0.13-μm ECG SoC.

2.6 Conclusions

This chapter reviews past designs of low-power analog front-end for biomedical signal acquisition. The chain-like input configuration for multi-channel sensor systems is highlighted for input port saving. A thorough investigation on the pseudo resistor choices is conducted, including discussions on the requirements

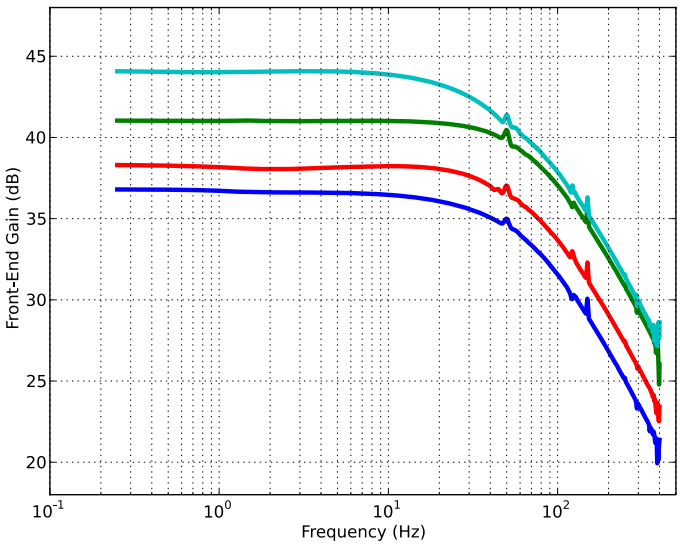

Figure 2.21: The tunable gain and frequency response of the AFE.

for the pseudo resistors at various input stages. Two capacitively-coupled design examples are then introduced. In the coming chapters more details are revealed on designing low-power biomedical front-end, with special efforts on extending the front-end functions and improving the signal quality.

CHAPTER 3

A 13.4 μA ECG and Respiration SoC

This chapter presents a low-power multi-functional biomedical System-on-Chip (SoC) for simultaneous 3-lead ECG and respiration acquisition. The capacitively-coupled analog front-end features low noise and tunable gain and bandwidth settings for different acquisition tasks. The cascaded pseudo resistor structure improves the analog output linearity. To monitor the respiratory conditions, the thoracic impedance is tracked continuously using the early demodulation technique, which reduces the amplifier's bandwidth requirement and save the power consumption. A lead-off detector and a lossless ECG signal compressor can further reduce the power consumption for wireless communication. Fabricated in 0.35 μm CMOS technology, the whole SoC consumes 13.4 μA under 3.0 V power supply. The input-referred noise is 1.46 μV_{rms}, with full-range total harmonic distortion of less than 0.4%. The low distortion and high power efficiency makes it a good candidate for long-term wearable biomedical sensors.

3.1 Introduction

The most common approach to assess the heart condition of the patients is to monitor the long-term ECG patterns. However, a normal ECG trace cannot rule out the possibility of an impending heart attack like AMI [10]. To improve the immediate diagnosis of AMI, other possible symptoms from the patient shall be considered. For example, dyspnea (breathlessness) or tachypnea (rapid breathing), which often accompany heart attack, could be easily identified by checking the respiratory rate (RR) [12]. Recent research also shows that respiratory rate could provide significant prognostic information [11] for AMI patients. It is therefore desirable to capture both the ECG and the RR data, especially for the patients who have a prior heart attack history.

By extending the functions of traditional ECG sensors, a multi-parameter biomedical sensor could be one of the best candidates to for vital signs acquisition. Nevertheless, designing a low-noise low-power wearable ECG+RR sensor remains challenging. The ECG signal, which is normally a few millivolts in amplitude, could be easily overwhelmed by noise or artifacts. To facilitate long-term continuous recording, the system power consumption should be significantly reduced. Otherwise the battery life would be compromised. The RR can be acquired by the non-invasive impedance pneumography [85]. Several low-power designs have been reported in recent years [31, 86, 77], but few are designed for respiration monitoring. A few recent designs like [77, 65, 78, 79] also include tissue impedance monitoring. The impedance data in those design are used for motion artifacts suppression, and high-frequency current injection requires much higher power due to the amplifier's bandwidth limits. Other designs like [87] use HRV to obtain the respiratory frequency, which are hardware efficient but the RR pattern is less accurate.

This chapter proposes a fully-integrated ECG+RR biosignal acquisition SoC, which is able to capture the standard 3-lead ECG and single-channel respiration simultaneously. The multi-channel ECG signals are acquired using capacitively-coupled front-ends. Different pseudo resistors are used to ensure low high-pass corner as well as high linearity. For the respiration measurement, the early demodulation of the injected signal before IA helps to relax the bandwidth constraint and save the power of the amplifiers. By removing the DC part, the measurement results could achieve the optimal dynamic range regardless of the patient's conditions. Also, a slope-based lossless ECG compressor is implemented to reduce the ECG data rate, which is highly proportional to the power consumption for wireless communication. The clinical trials show clear respiratory rhythm and 3-lead ECG traces with clear P and T waves for diagnostic uses. The total power consumption of the SoC is 40 μW.

The remaining is organized as follows. Section 3.2 introduces the architecture of the SoC, including various approaches to improve the signal quality and minimize the power consumption. The circuit details, especially for the AFE are revealed in Section 3.3. Chip measurement results are discussed in Section 3.4. The final section draws the conclusion remarks.

3.2 System Architecture

The architecture of the proposed ECG+RR system is shown in Fig. 3.1. The main system includes an AFE, a 12-bit SAR ADC, and a lossless ECG compressor. The ECG signal and respiratory data are acquired through the low-noise AC-coupling AFE. After proper signal conditioning, the ECG and respiratory analog outputs are multiplexed and digitized by the SAR ADC. A 32.768-kHz real-time clock (RTC) signal is generated from the on-chip crystal oscillator driver. The system

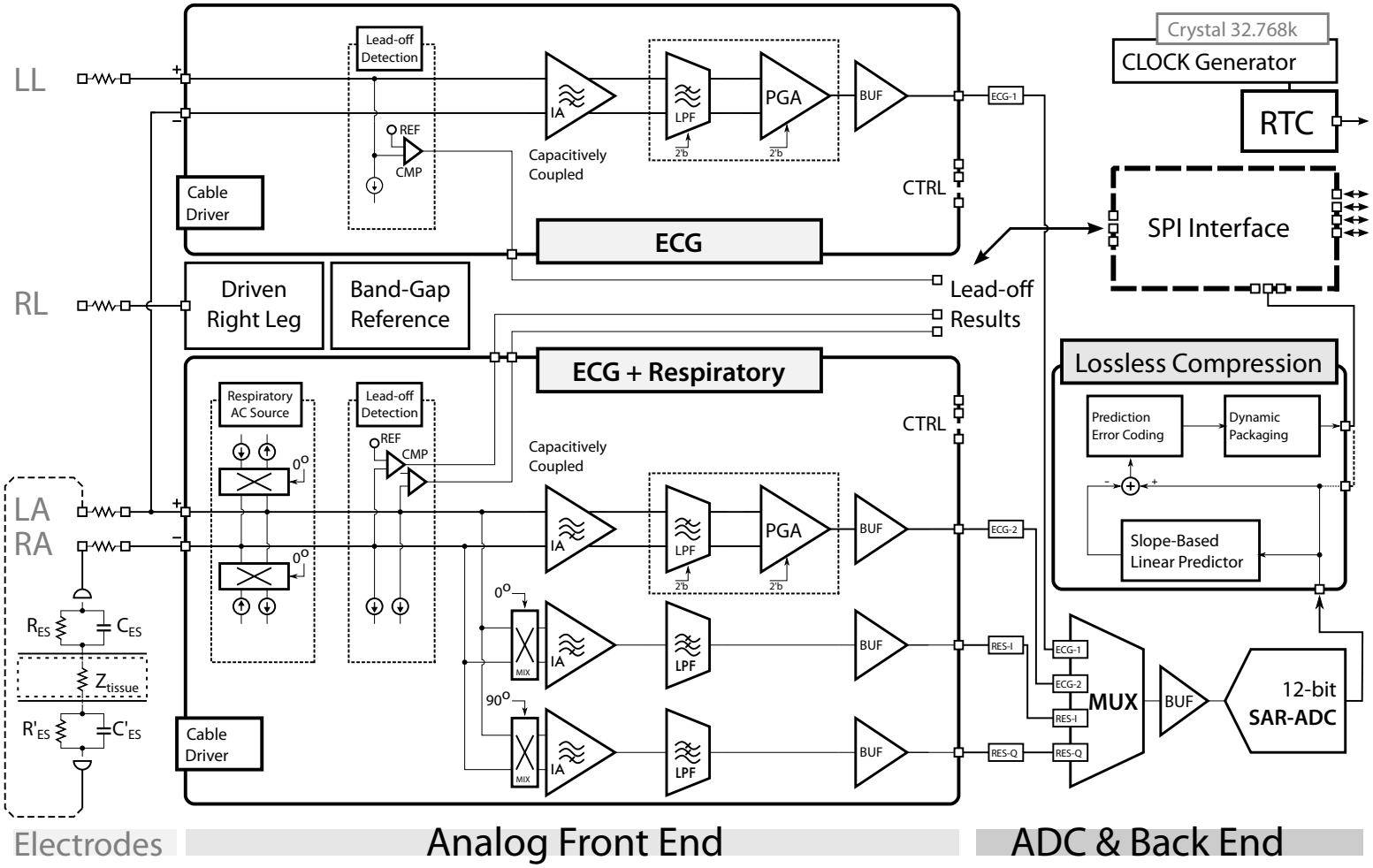

Figure 3.1: Diagram of the ECG+Respiratory system.

sampling rate is 512 Hz, and it can be reduced to 128 Hz when lower data rate is desired. An optional input-aware compression scheme can be applied to minimize the data rate without losing any bits. The data exchange is through a standard Serial Peripheral Interface (SPI).

The analog front-end includes two low-noise readout channels, one for simultaneous ECG and respiratory signals acquisition, and one for ECG only. The two ECG channels are fully-differential designs to enhance common-mode suppression for power-line 50-Hz or 60-Hz interference. As shown in Fig. 3.1, the positive input of the ECG channels are connected together. The three standalone inputs of the 2 ECG channels are fully utilized under the standard 3-lead ECG configuration. Using this chained connection, lead-I (potential between LA and RA electrodes) and lead-III (between LL and LA electrodes) are directly captured through the AFEs, while lead-II signal can be calculated by calculating the difference between lead-I and lead-II. Therefore, the entire AFE for lead-II is saved.

The ECG signals are first sensed through a low-noise IA, and then filtered and amplified through the PGA. The IA input is AC-coupled which eliminates electrode-skin DC offsets completely. To accommodate different ECG input amplitudes, the overall pass-band gain is tunable through 250 to 2000, controlled by a two-bit input. Another two-bit signal is used to control the low-pass corner, limiting the signal bandwidth below the Nyquist frequency. Rail-to-rail output buffers are inserted before and after the MUX on each signal paths. The buffers help reduce the settling time and minimize the tracking errors of the ADC sampling [31].

To monitor the respiration condition, the SoC measures the change of the electrical tissue impedance Z_{tissue}. An 8-kHz tunable AC current source injects 0.1~10 μA current into the body through the electrode, converting the impedance

signal into voltage. The voltage signal is then amplified with a gain of 450. Since the common mode is set at the current source, single-ended output configuration is used for the impedance amplifier for its simplicity and low power consumption.

Besides the tissue impedance Z_{tissue}, the respiratory measurement also takes the electrode-skin interface impedance R_{ES} and C_{ES} into consideration. So the respiration data will be affected by other artifacts like the electrode or body movements. On the bright side, the impedance data can be used for motion artifacts removal and so that the quality of ECG traces could be improved [65]. Motion artifacts are normally caused by skin-electrode stretch, which can be monitored through the change of the skin-electrode impedance [88]. Inspired from previous designs [77, 78, 45], both the in-phase (I) and quadrature (Q) channels for impedance monitoring are extracted in the respiratory measurement channel for this SoC. The motion artifacts are filtered using a standard 2nd-order Least-Mean-Square filter with the quadrature impedance signal as the input. The LMS filter is implemented off the chip.

This design also includes several accessory blocks to improve the signal quality and power efficiency. First, the DRL circuitry extracts the common mode variations from the 3-lead ECG input, and feeds it back to the body. With the ECG amplifiers, the DRL forms a feedback loop to reduce the common-mode interference effectively [38]. Second, the cables between the electrodes and the AFE channel inputs are actively shielded using the output of the ECG cable driver. The cable driver is a voltage buffer, with the AFE outputs as the buffer input. This active shielding helps mitigate the effects from various interferences. Third, a lead-off detector is installed on each input lead. When the connection between the electrode and the body is off or unreliable, the lead-off detector will notify the external MCU, and the system could enter the sleep mode with lower standby power, waiting until the user reconnects the electrodes.

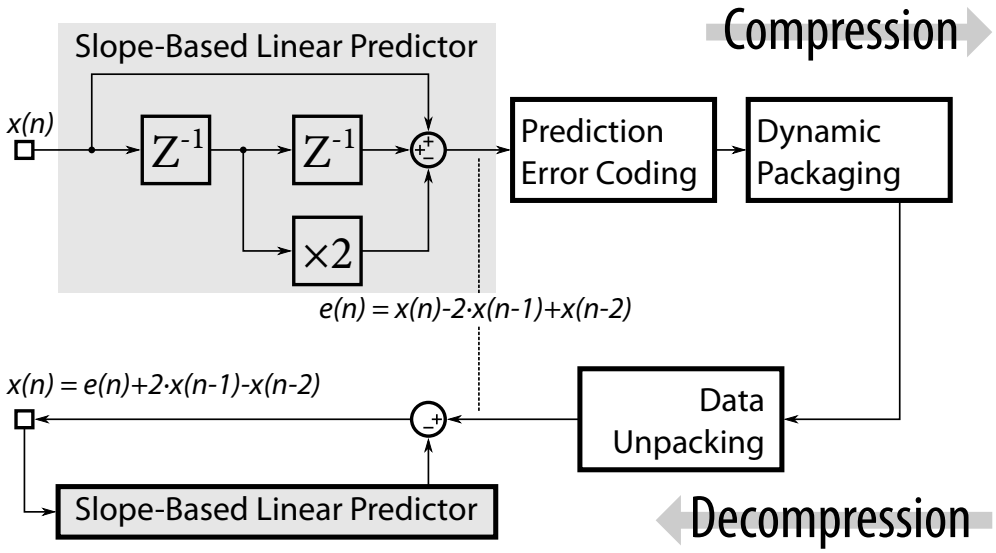

Figure 3.2: Lossless ECG compressor and decompresser.

More aggressive power reduction at the system-level is possible only if the data rate could be decreased. This is achieved by an on-chip low-power ECG compressor. The whole process is lossless so that no information is lost during the compression. Both the compression and decompression scheme are illustrated in Fig. 3.2. First, a slope-based linear predictor estimates the current value $x(n)$ based on the slope value derived from previous samples $x(n-1)$ and $x(n-2)$. $x(n)$ may differ from the predicted value of $x(n-1)+\Delta x(n-1) = 2\cdot x(n-1)-x(n-2)$, so the prediction error $e(n)$ is obtained and encoded separately. Mostly $e(n)$ is small in amplitude and could be coded efficiently by discarding most significant bits (MSBs) which are all zero. To package the errors into fixed-length 16-bit output, various headers are appended to accommodate different $e(n)$, so that several $e(n)$ values could be packaged in one word output. This helps to reduce hardware complexity of the compressor itself, compared with the variable-length Huffman coding scheme.

3.3 Circuit Designs

Among all the circuit parts, the analog front end is the most critical one, as it is often the bottleneck in the system regarding the noise and distortion performance. First, the input-referred noise needs to be low enough for accurate biosignal acquisition. Second, the signal distortion should be less than 1% even at the 3 V full-scale output. Last but not least, as the sampling rate of the ADC is no more than 512 Hz, higher-order low-pass filters with less than 200 Hz cut-off frequency are necessary to eliminate aliasing errors. Nevertheless, the limited power budget disallows adding extra anti-aliasing filters. So the signal bandwidth is reduced by designing low-bandwidth OTA for both the IA and the PGA. This section highlights all these circuit design considerations and trade-offs for the analog front end.

3.3.1 ECG Channel with the Pseudo Resistors

Fig. 3.3 shows the architecture of a single-channel capacitively-coupled ECG front end. The main purpose for the front end is to amplify the input ECG signal with tunable gain and bandwidth. While the amplitude of a typical ECG signal from Ag/Cl wet electrodes is around millivolts, the DC offset between the differential electrodes could be more than 200 mV. To avoid saturating the amplifiers and increase the input dynamic range, the input offset should be canceled properly.

A simple and power-efficient way to block the DC offset is to implement a high-pass filter. Since the low-frequency component of ECG traces around 0.5 Hz still contains important information for accurate arrhythmia diagnosis on ST elevation, the high-pass corner needs to be at 0.05 Hz or lower [13]. Large capacitors and resistors are hence required to achieve such a low cut-off frequency, at the cost of significant chip area. In our design, pseudo resistors [25] with

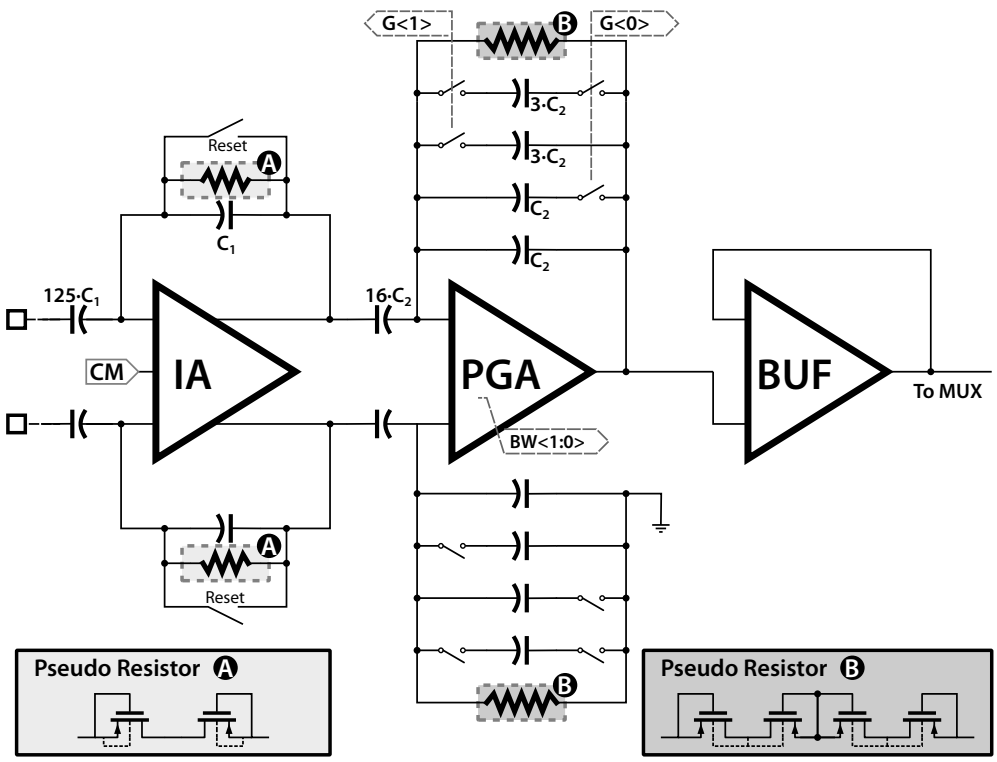

Figure 3.3: The ECG front-end amplifiers with two types of pseudo resistors.

GΩ resistance are used. The pseudo resistors are normally two or more diode-connected p-type MOSFETs in parallel. The bulk of each PMOS is often connected to the source or drain, so that the performance of the pseudo resistor is less affected by the absolute voltage applied on it.

Two types of pseudo resistors are used in the IA and the PGA stage respectively. The simulated resistance versus input voltage across the pseudo resistors is plotted in Fig. 3.4. As C_1 in the IA stage is around 0.5 pF, the equivalent resistance of the pseudo resistor in this stage should be at least $6.4 \times 10^6 M\Omega$. The input amplitude is small for the IA stage, so the pseudo resistor does not need to support large input, and the A design is adequate. For the PGA stage however, the input amplitude could be as high as 1.5 V. Because the resistance of the A design is around $1M\Omega$ at $\pm 1.5V$, the current flowing through the pseudo resistor would be about $1\mu A$, causing loading errors at the output. It is necessary to use other

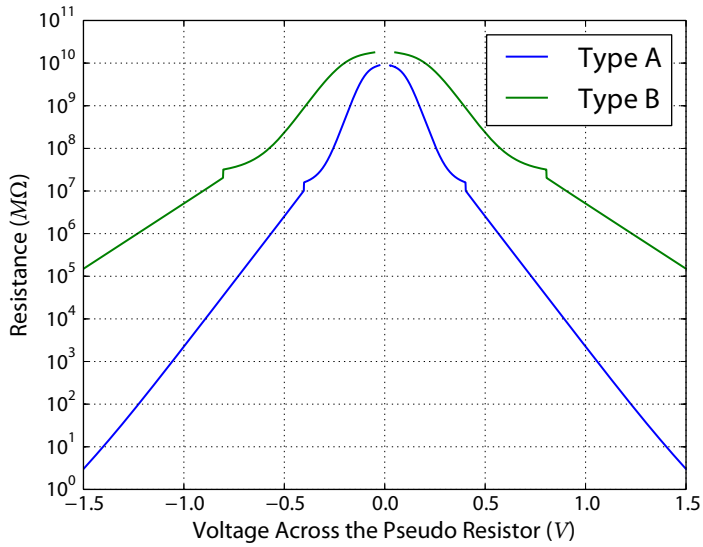

Figure 3.4: Simulated resistance for the two pseudo resistors.

pseudo resistor structures with even higher resistance for a wide input range. By cascading two A designs in parallel, the resistance of the B design is 10^5 higher at 1.5 V than the original A design. As shown in the testing result later in Section 3.4, the cascaded pseudo resistor helps to achieve less than 0.4% THD at 3 V output.

3.3.2 Instrumental Amplifier

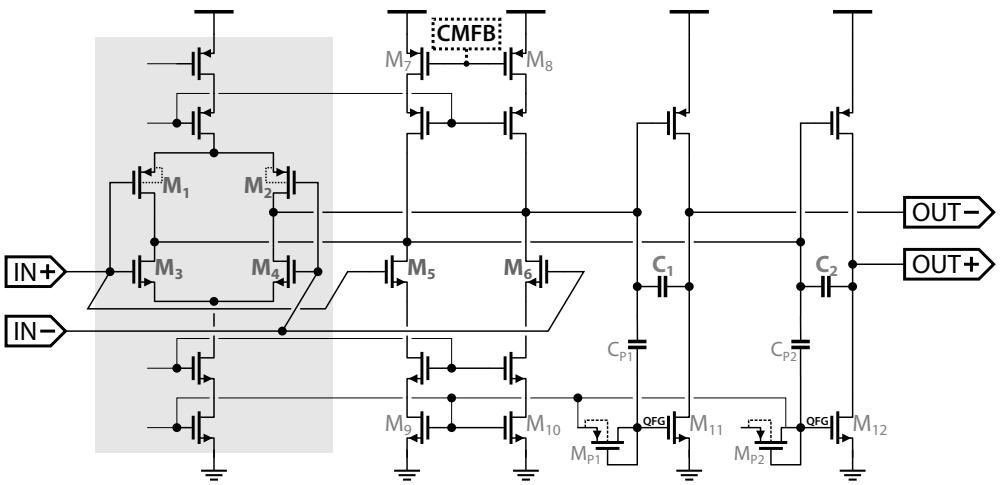

Figure 3.5: The amplifier used in the IA stage.

Fig. 3.5 shows the schematic of the low-noise operational transconductance amplifier (OTA) used in the instrumental amplifier for ECG capturing. The fully-differential configuration increases common-mode suppression, making the ECG signal less affected by common-mode artifacts and power-line interference. Two-stage architecture is used to improve output swing and open-loop gain. At the first stage, an extra g_m branch with $M_{1\text{-}4}$ as input transistors is added, which is marked in grey background in the figure. The branch consists of an inverter-based differential pair, which improves the current efficiency regarding the transconductance. By tuning the current between $M_{1\text{-}4}$ and another input pair $M_{5,6}$, the OTA transconductance g_{mi} could be changed, which is given by

$$g_{mi} = g_{m1,2} + g_{m3,4} + g_{m5,6} \tag{3.1}$$

To improve the noise/power efficiency, all the input transistors $M_{1\text{-}6}$ are biased in the subthreshold regime. The thermal noise current of a MOS transistor operated in the weak inversion [89] could be modeled as

$$\overline{i^2_{n,thermal}} = 2kTn \cdot g_m \tag{3.2}$$

and n is the subthreshold slope factor, which is around 1.3 as simulated in this technology. The noise contributions of the cascaded transistors and the tail current sources are negligible. Also the first stage dominates the noise for a typical two-stage OTA. Based on the simplification mentioned, the input-referred thermal noise of this OTA is approximately

$$\overline{v^2_{ni,thermal}} \approx \frac{4kTn}{g_{mi}} \left(1 + \frac{g_{m7,8}}{g_{mi}} + \frac{g_{m9,10}}{g_{mi}}\right) \Delta f \tag{3.3}$$

The NEF [23] is used to measure the noise/power trade-off, which is defined by

$$NEF = v_{ni,rms} \cdot \sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \tag{3.4}$$

where I_{tot} is the total current and BW is the amplifier's bandwidth. Suppose the drain current I_d of $M_{1,2,3,4}$ is $\alpha \cdot I_{tot}$, and the drain current of $M_{5,6}$ is $\beta \cdot I_{tot}$. Also under the EKV model [89, 90], the g_m of a subthreshold MOS transistor is approximately

$$g_m = \frac{I_d}{nU_T} \tag{3.5}$$

with the $U_T = kT/q \approx 26mV$. If we further ignore the flicker noise and the noise contribution from $M_{7\text{-}10}$ and the CMFB, the optimal NEF for this OTA architecture is

$$NEF_{opt} = \sqrt{\frac{n^2}{2\alpha + \beta}} \tag{3.6}$$

Note that for the current of the first stage cannot exceed the total current I_{tot}. To minimize the NEF, given that $2\alpha + 2\beta < 1$ is require, α should be maximized to take advantage of the current reuse between $M_{1,2}$ and $M_{3,4}$. If $\alpha = 0.5$ that all the current flows to the inverter-based amplifier branch, the minimum NEF of 1.3 could be achieved. Unfortunately, pursuing the highest NEF would impair other design targets like the bandwidth limits and the settling time, which are discussed as follows.

First, unlike other high-speed designs, it is advantageous to limit the bandwidth of the IA for ECG and RR capturing. The intrinsic low-pass characteristic of the OTA helps to suppress the high-frequency noise and artifacts without any extra active filters. This issue becomes even more critical as the sampling rate is 512 Hz or lower. Since the bandwidth of the IA is

$$BW = \frac{g_{mi}}{C_{1,2} \cdot G_{IA}} \tag{3.7}$$

both the IA pass-band gain G_{IA} and the Miller-compensation capacitance value $C_{1,2}$ shall be increased to obtain small bandwidth. As the gain is also determined by the C_1 capacitor ratio given in Fig. 3.4, either approach demands significant

capacitor area on chip. Alternatively, the g_{mi} can be reduced, with the side effect of increasing the noise floor.

Second, large output slew rate is required to mitigate the output distortion. Because the gain of the IA G_{IA} is 125, harmonic distortions could be introduced even at the IA stage. The most straightforward way to improve the linearity is to increase the static current at the output stage. Simulation also shows higher output stage current improves the recovery time after resetting the IA. But excessive current at the second stage would inevitably affect the power utilization and the transconductance g_{mi}. An output boosting technique named Quasi-floating gating [80] is also used to push the second stage of the OTA into class-AB operation. The gates of $M_{11,12}$ are partially controlled by the first stage's outputs through the small capacitors $C_{P1,P2}$, so that the transconductance of the second stage $g_{m11,12}$ is enhanced.

Last but not least, the common-mode feedback circuit should be carefully design to avoid stability issue. As the drain current of $M_{5,6}$ is controlled by the CMFB circuit, setting β too small would cause the CMFB failing to adjust the common-mode current. On the other hand, using large β is likely to introduce CMFB stability issues. Moreover, the CMFB circuit itself requires minimal current dissipation to ensure enough common-mode settling time and the loop stability.

With all the trade-offs mentioned above, we allocate half of the total current to the second stage to improve the output linearity and the IA recovery time after reset. α and β are both set at 0.1, considering the bandwidth upper limits. The optimal NEF now becomes 2.4. Note that this simple calculation does not include the flicker noise, which could be optimized by using large width and length for all the input transistors $M_{1\text{-}6}$.

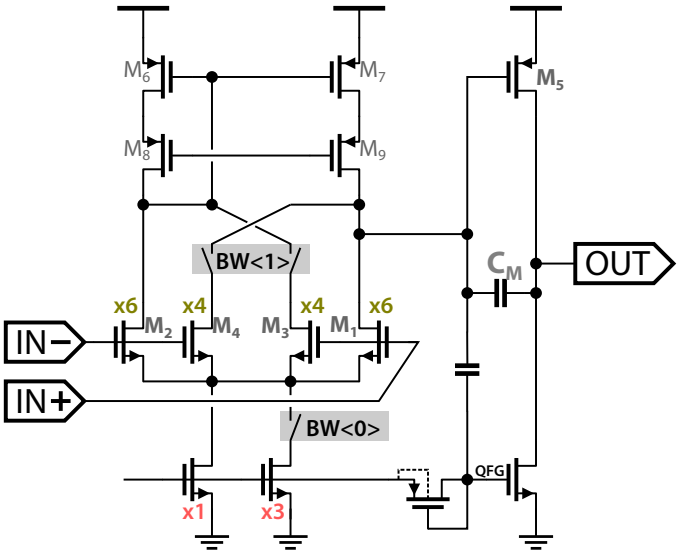

Figure 3.6: The amplifier in the PGA.

3.3.3 Programmable-Gain Amplifier

The programmable-gain amplifier changes the ECG pass-band gain as well as the low-pass cut-off frequency through the digital control bits G<1:0> and BW<1:0>. The gain is tuned by switching on and off the parallel capacitors C_2, shown in Fig. 3.3. The schematic for the OTA at the PGA stage is given in Fig. 3.6.

To reduce the aliasing errors under different sampling rate at the ADC, the signal bandwidth shall be tunable. The low-pass filtering function is realized through the OTA's close-loop bandwidth. The most common method to tune a two-stage amplifier's bandwidth is by changing the Miller capacitor. Also since the close-loop gain of the IA is higher than the PGA, it seems desirable to tune the C_{P1} and C_{P2} for bandwidth control. But because the g_m of the IA OTA is much higher to improve the noise performance, $C_{P1,2}$ each must be at least 8 pF in order to obtain the desired low-pass corner at around 200 Hz. It is even worse when the sampling rate is reduced to 128 Hz, that $C_{P1,2}$ in total need to be over 64 pF. An an alternative approach, the OTA design in [31] achieves the tunable bandwidth by

changing the input stage current. This may cause noise degradation at the lowest bandwidth setting, when the OTA current is small. Considering the noise and area constraints, the bandwidth tuning is at the PGA stage.

The OTA bandwidth is mainly tuned by adjusting the input g_m for the PGA. For the similar reason mentioned above, changing the Miller capacitor C_M alone cannot meet the bandwidth target. So part of the bandwidth tuning is done through changing the tail current of the first stage, by switching on or off an extra current mirror controlled by the BW<0> input. On the other hand, changing the biasing current too much would shift the operation condition, especially for M_5 in the second stage. To solve this issue, the higher bit BW<1> takes control of the NMOS degeneration ratio, rather than the biasing current directly. If BW<1> is turned on, about 2/5 of the total current will flow through M_3 and M_4, and reduce the effective current to 1/5 of the original value. The biasing condition of M_5 is unchanged as the current flows through the PMOS loads $M_{6\text{-}10}$ remains the same.

3.3.4 Early Demodulation Impedance Measurement

A common approach to measure the respiratory rate is to track the changes in the electrical impedance of the thorax during inhalation or exhalation [91]. A high-frequency AC current is injected through the electrodes to the body, and the voltage between the two electrodes is then extracted and amplified. Because the change of the impedance (about 1 Ω, depending on the frequency) is often much less than the baseline impedance (500 Ω), the DC part should be filtered for better input dynamic range, similar to ECG capturing.

Existing designs like [91, 77, 78] uses CHS technique when measuring the tissue impedance. The CHS could effectively remove the input offsets of the OTA as well as the flicker noise, and achieve high resolution for those low-frequency measurements. However, CHS-based amplifier alone may saturate if the DC offset

from the signal source is too large. Additional DC cancellation servo loops are required, which increases the AFE power and complexity. Another issue arises when the chopping frequency f_c is high and the power is constrained. As the signal is chopped to higher frequency, the IA's bandwidth need to be at least 8-10 times higher than f_c to avoid attenuations, which in turn requires higher power consumption.

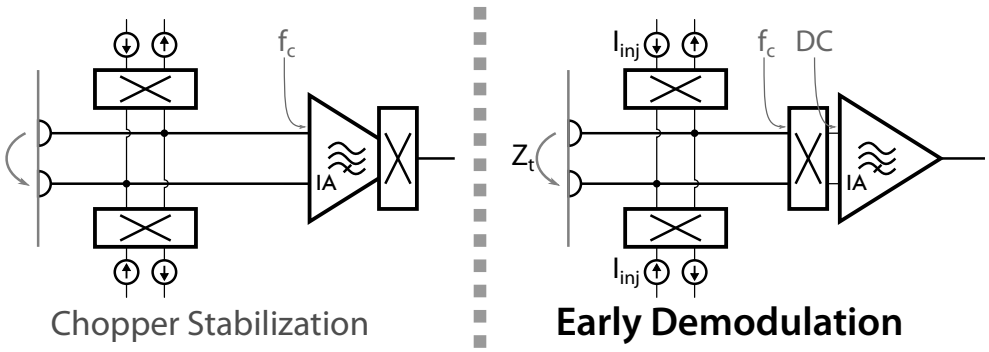

Figure 3.7: The early demodulation impedance monitoring compared to the chopper stabilization.

To improve the power efficiency for RR monitoring, the simplified early demodulation technique is proposed as illustrated in Fig. 3.7. The chopper at the output of the IA is now moved before the amplifier's input ports. So the high-frequency voltage signal due to the current injection is demodulated to DC band before the amplifiers. In other word, instead of amplifying the input signal at chopping frequency f_c, the IA now have a low-frequency input signal close to DC. The bandwidth requirement for the IA is therefore much lower compared to the traditional chopper architecture. For the disadvantage, this early demodulation loses the ability to filter the OTA's offset. But this offsets is less critical for RR tracking application, where only the variance of the impedance is concerned. The IA architecture for RR monitoring is similar to the IA for ECG channel. Therefore, the DC potential difference caused by baseline impedance is removed completely,

and the low-frequency impedance information remains unchanged, since the high-pass corner of the IA is much lower than 0.05 Hz as discussed earlier. This DC-blocking impedance measurement can tolerate different input situations where the skin and electrodes impedance may vary greatly among the patience. Another benefit from this early demodulation structure is that increasing the injection current frequency does not necessarily require higher circuit power consumption. It is then possible to for this single amplifier configuration to operate under different probing frequencies.

The OTA used for respiratory measurement is a single-ended variation from Fig. 3.5. The input common mode is set by the AC current source. Also the common-mode variation for impedance measurement path is not critical. So a single-ended architecture is adopted for the OTA to save the power consumption. Note that moderate distortion on the RR measurement is still acceptable. Therefore the PGA stage is entirely skipped after increasing the IA gain for RR to 450. The total current consumption is less than 2 μA for the entire impedance measurement channel, when using 0.4 μA probing current.

3.3.5 Lead-off Detector

For long-term ECG and respiratory monitoring, the device should work continuously for days with minimal user intervention. When one or more electrodes are off the skin, the device should be able to notify the user. Before the connection is restored, it would be wise to discard the segment automatically without wasting power on signal recording or transferring, since the captured data during lead-off are likely inaccurate and useless. Another issue is that the electrodes may dry out after certain time of usage. Similarly, dried electrodes would more likely introduce artifacts and reduce the signal quality. It is therefore necessary to include another sensor that monitors the electrode conditions to target at this application scenario.

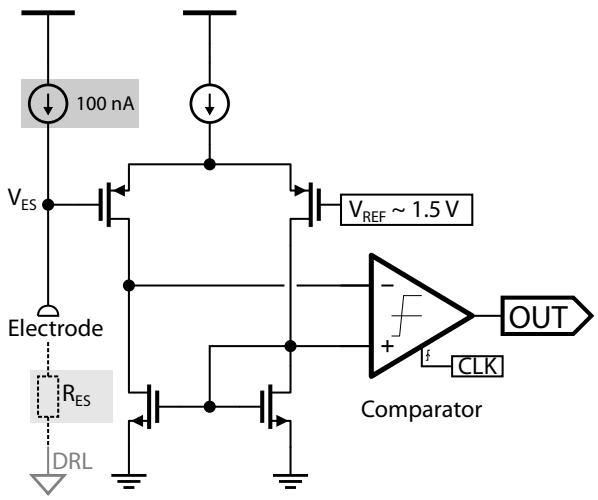

Figure 3.8: The electrode lead-off detector.

In this SoC, a low-power lead-off detector is built on-chip, which measures and compares the DC electrode-skin resistance R_{ES} with a reference value. The schematic is shown in Fig. 3.8. A fixed 100 nA current is injected to the body through the connected electrode, converting the resistance into voltage V_{ES}. Next, a single-stage differential amplifier compares V_{ES} with the reference voltage V_{REF}. V_{REF} is set at around 1.5 V. So the threshold resistance for lead-off decision is about 15 MΩ. Because the accuracy for the V_{REF} and the threshold is not critical, V_{REF} is generated simply from existing current mirrors and diode-connected transistors, and the total current for the amplifier is only 20 nA.

3.3.6 MUX & ADC

The analog MUX uses bootstrapped switches to reduce the tracking errors, shown in Fig. 3.9. The NMOS M_1 with reduced size has smaller on-resistance and parasitic capacitance. This reduces the MUX settling time and cross-channel interference from the parasitic capacitor coupling. Illustrated in the timing diagram in Fig. 3.10, the MUX's switching is misaligned with ADC sampling clock, which provides sufficient settling time for the analog signal before ADC sampling and

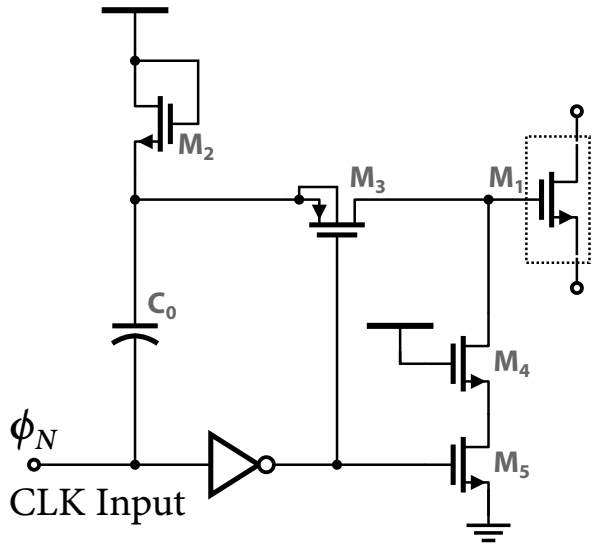

Figure 3.9: Bootstrapped switch used in the MUX.

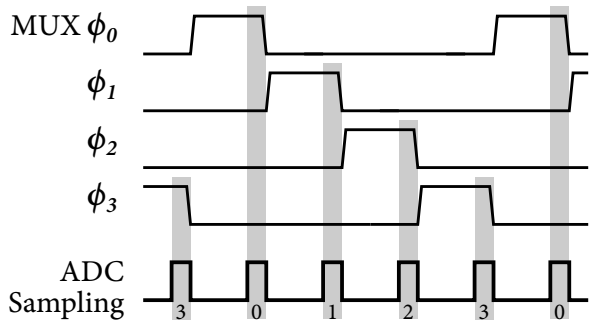

Figure 3.10: MUX and ADC sampling timing diagram.

therefore further minimize signal distortion.

The ADC uses dual-capacitive-array architecture [32] to reduce the dynamic power from capacitor switching. Showing in Fig. 3.11, an extra 6-bit S/H array is used to sample the input signal, besides the 12-bit DAC capacitor array. The smaller S/H array is used to digitize steps with larger changes in the input, generating the 6-bit MSBs, while the LSBs are from the DAC array with finer resolution. Switching power is reduced thanks to the smaller capacitance values and voltage steps.

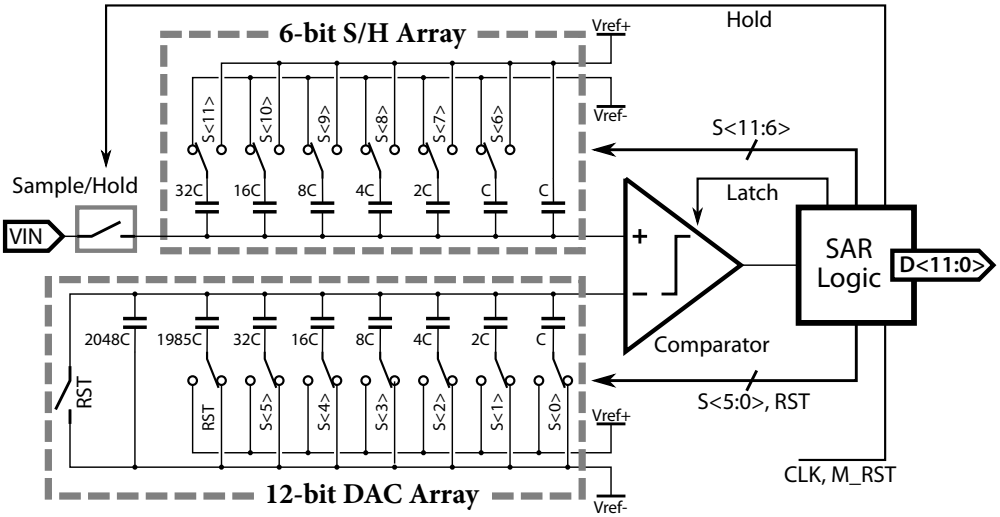

Figure 3.11: The dual-capacitive-array SAR ADC.

3.4 Measurement Results

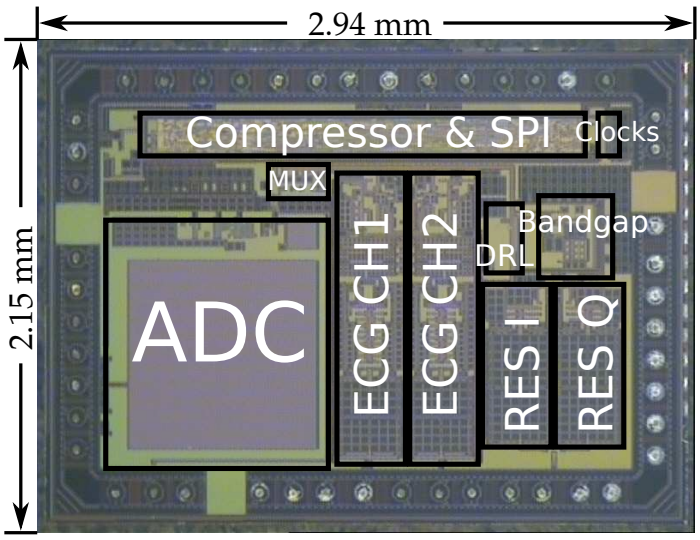

Figure 3.12: Micro-photograph of the fabricated chip.

This SoC chip is fabricated in a 0.35 μm standard CMOS process. The system operates under a single 3.0 V supply voltage, which helps to maximize the ECG output swing and eliminate any voltage level converters when integrated with the external MCU. The total chip area is 2.94 mm × 2.15 mm, with the micro-

photograph shown in Fig. 3.12. The measurement results for the front-end, the ADC, and the compressor are summarized in Table 3.1. The power consumption is measured with the injection current for respiratory monitoring set at 400 nA. For higher injected current, the total current rises accordingly. The power and area breakdown are shown in Fig. 3.13. The 2 ECG channels consume about 1/3 of the total power. At the moment very few sensor designs have the impedance or respiratory monitoring function. Therefore Table 3.2 compares the front-end amplifier design only. The ECG amplifier in this design is comparable to the state-of-the-art work Among the listed designs, [67] and the proposed work are the only two with impedance sensing.

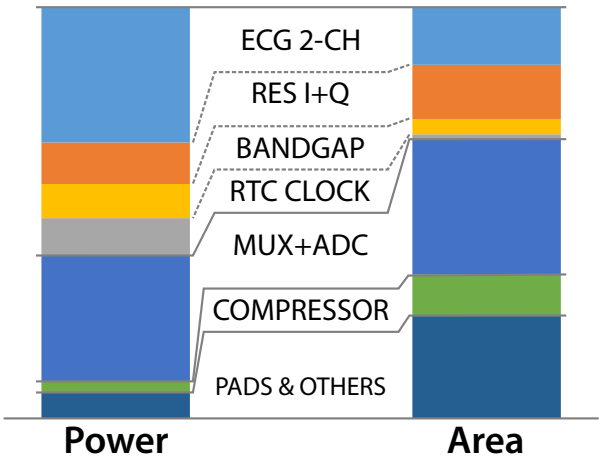

Figure 3.13: Power and area breakdown for the chip.

Fig. 3.14 shows the input noise spectrum of the ECG channel. The input-referred rms noise is 1.47 μV_{rms}, integrated from 0.5 Hz to 250 Hz. The thermal noise floor is at 55 nV/$\sqrt{Hz}$, with the 1/f noise corner at around 50 Hz. The NEF [23] is used to measure the noise / power trade-off, which is defined by

$$NEF = v_{ni,rms} \cdot \sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \tag{3.8}$$

where I_{tot} is the total current and BW is the amplifier's bandwidth. This design achieves a noise efficiency parameter NEF of 3.31. The gain and bandwidth are

Table 3.1: Performance of the ECG/Respiratory SoC

Parameter	Results
Single-Channel ECG AFE Current	2.1 μA
Gain Settings (G)	47/53/59/65 dB
High-Pass Corner	<7.5 mHz
Low-Pass Corner (BW)	15-200 Hz
Input-Referred Noise @ 0.5~250 Hz	1.46 μV_{rms}
Noise Efficiency Factor (NEF)	3.31
Total Harmonic Distortion @ Full Scale (THD)	<0.4 %
Common-Mode Rejection Ratio (CMRR)	65 dB
Power Supply Rejection Ratio (PSRR)	76 dB
Single-Channel RR I+Q AFE Current	1.1 μA
AC Current Injected	0.4-10 μA
AC Current Source Frequency	8 kHz
Impedance Resolution	0.7 Ω
ADC Total Current	4.1 μA
Sampling Rate per Channel	512 Hz
Differential Non-Linearity (DNL)	-0.88/+0.62
Integral Non-Linearity (INL)	-1.42/+1.31
Signal-to-Noise and Distortion Ratio (SNDR)	58.29 dB
Spurious-Free Dynamic Range (SFDR)	65.30 dB
Effective Number of Bits (ENOB)	9.39
Compressor Current	0.72 μA
Gate count per Channel	0.56 K
Compression Ratio	2.25
Power Supply (VDD)	3.0 V
System Total Current	13.4 μA

Table 3.2: Comparison of the Front-End Amplifiers

	This work	[29]	[92]	[32]	[67]
Technology	0.35 μm	0.35 μm	0.13 μm	0.35 μm	0.18 μm
Supply	3.0 V	1.0 V	1.0 V	1.0 V	1.2 V
Gain	47 - 65 dB	40.2 dB	38.3 dB	59 - 70.4 dB	28 - 36 dB
High-P Freq	7.5 mHz	3 mHz	25 mHz	0.5 Hz	0.5 Hz
Input Noise	1.46 μV	2.7 μV	1.95 μV	1.15 μV	0.61 μV
CMRR	65 dB	64 dB	63 dB	83 dB	110 dB
Current	2.1 μA	2.3 μA	12.5 μA	0.385 μA	13.3 μA

both tunable, with the frequency response provided in Fig. 3.15. The signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) performance of the SAR ADC is provided in Fig. 3.16. In this test, the input frequency is 117 Hz.

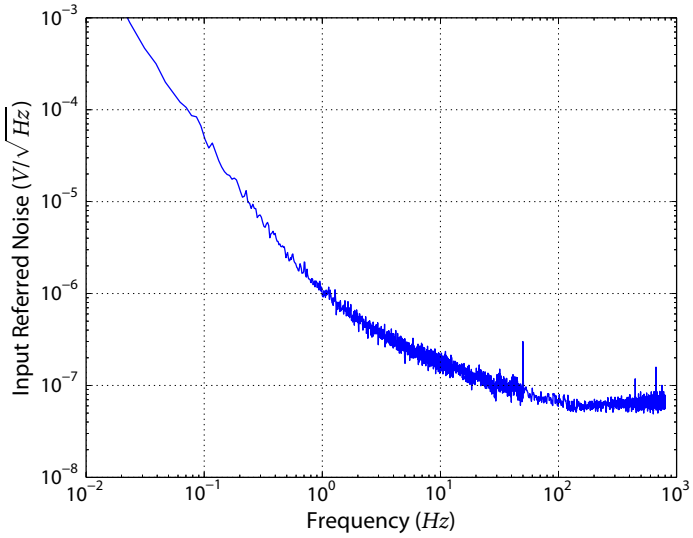

Figure 3.14: Input-referred noise of the AFE.

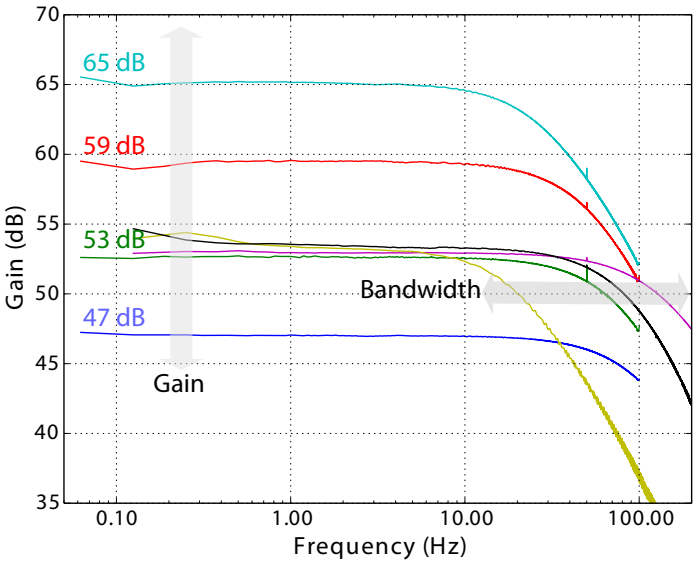

Figure 3.15: Frequency response of the front-end, with gain and bandwidth tunable in wide ranges.

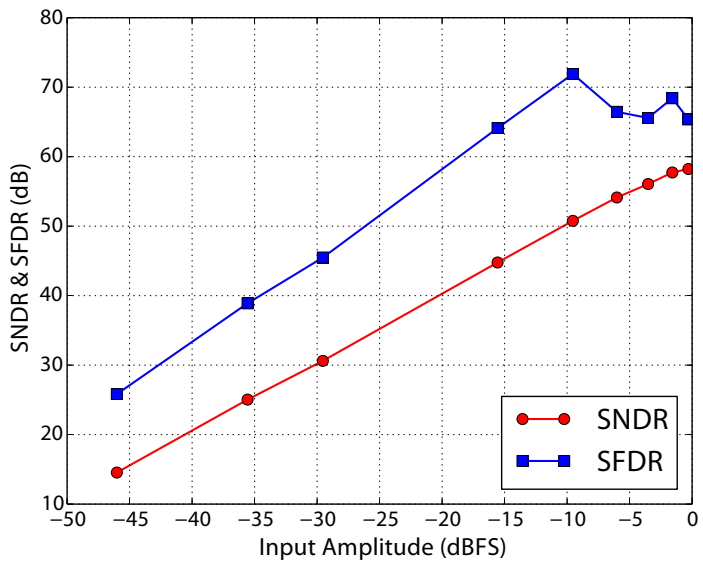

Figure 3.16: SNDR and SFDR performance of the ADC.

3.4.1 ECG Acquisition

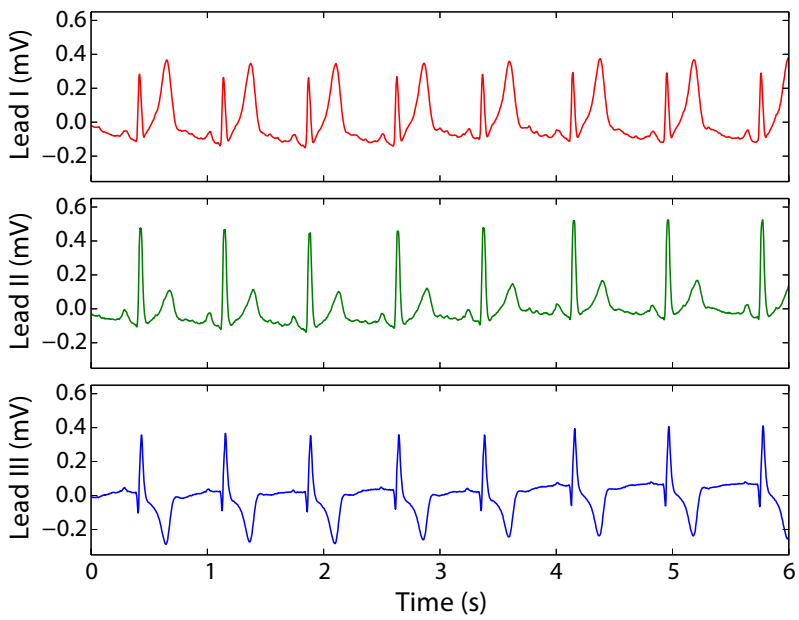

Figure 3.17: Captured 3-Lead ECG data.

The 3-Lead ECG signals captured by the SoC are shown in Fig. 3.17. The AFE uses 500 gain with the lowest bandwidth setting. The P and T morphologies

can be easily identified in the figure, especially for the lead-II plot. Power-line noise and other artifacts are effectively suppressed by the DRL circuit and cable drivers.

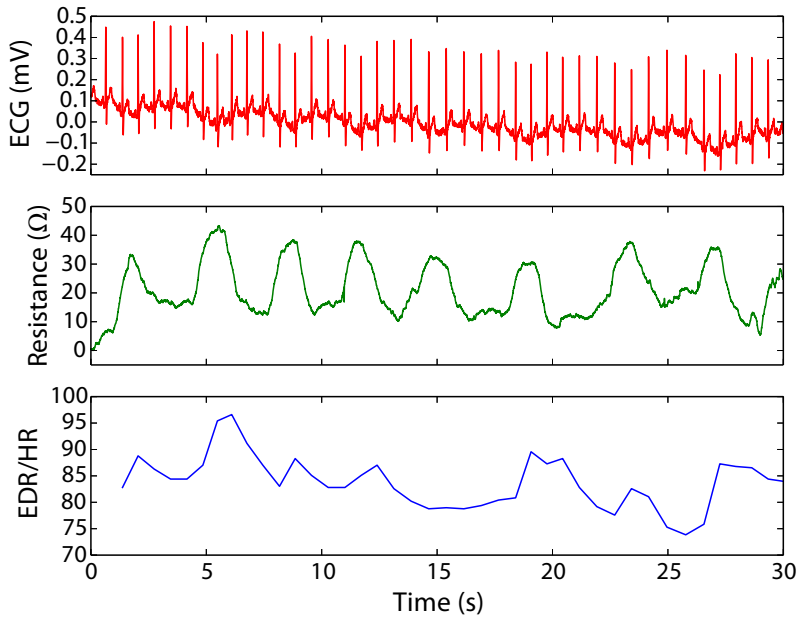

Figure 3.18: Respiratory rate compared to the ECG-derived respiration signal.

Fig. 3.18 provides the respiration data through resistance measurement. As analyzed before, the baseline impedance is filtered, and only the impedance change will be tracked. Besides the ECG and RR signal, the third subplot shows the ECG-derived respiratory (EDR), which is equivalent to instant HRV. A few publications [93, 94] reported high correlation between the RR and the EDR signal. It is also a respiration monitoring approach by checking the beat-to-beat variations in the RR intervals, origining from the respiratory sinus arrhythmia (RSA). This method is common for estimation respiration rate and apneas detection [95]. Here the correlation is demonstrated in the figure.

It is also possible to extend the system for impedance-based motion artifacts removal. The capacitive reactance, or the imaginary part of the impedance information, reflects the electrode-skin interface conditions[45, 96]. Fig. 3.19 shows

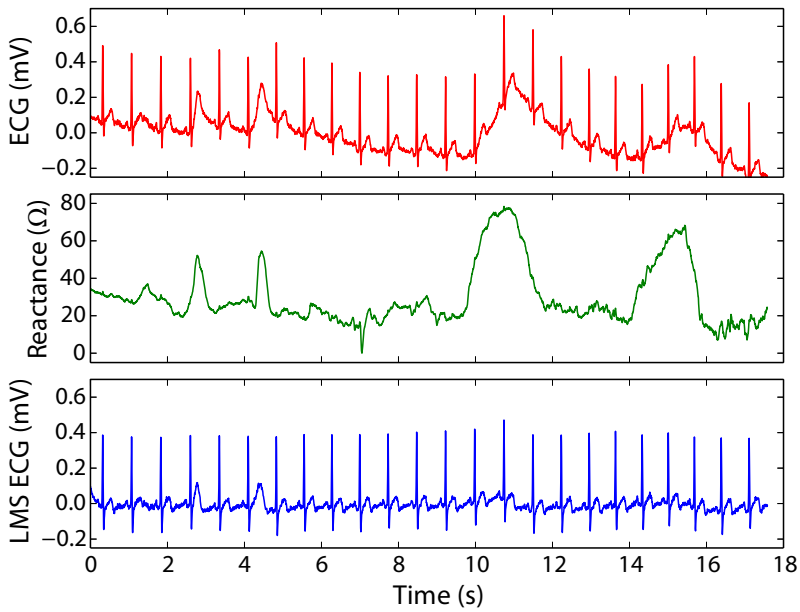

Figure 3.19: ECG baseline removal using quadrature impedance data.

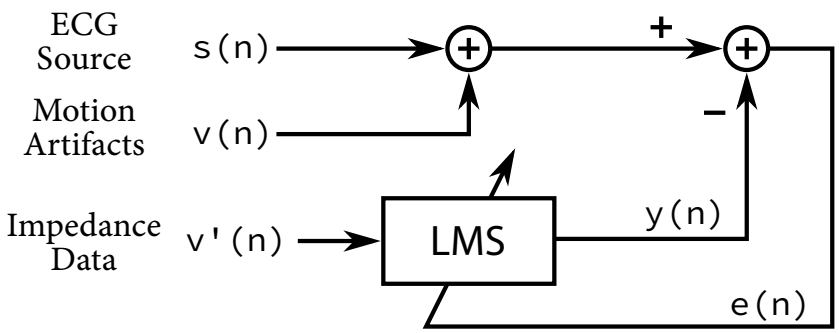

Figure 3.20: LMS filter used for motion artifacts removal.

the original ECG signal captured from human subjects, the imaginary (quadrature) part of the impedance data, and the output of the least mean square (LMS) filter with minimized baseline wandering. The artifacts are introduced by intentionally pulling or pushing the electrodes. Judging from the waveform, the high correlation between baseline and the reactance data is observed, which provides opportunities to use the reactance impedance as adaptive filter input $v'(n)$. The baseline drift are removed as shown in the plot, using a simple LMS filter given in

Fig. 3.20. Compared to the results in [97, 98] or other bandpass-based approaches, this simple and less aggressive motion artifacts removal method maintains most P and T waves unaltered.

3.5 Conclusions

Presented in this chapter is a multi-parameter biosignal SoC for long-term wearable sensor applications featuring low noise and high power efficiency. The cascaded pseudo resistor maintains high impedance over the entire 3 V range, and reduces the amplifier large output distortion. The early demodulation structure for the respiratory measurement relaxes the amplifier's bandwidth requirement. The lead-off detection and the impedance data improve the data reliability. And the lossless ECG compressor reduces the ECG data rate, which induces significant power saving at the system level. Implemented in 0.35 μm CMOS technology, the input referred noise between 0.5 Hz and 250 Hz is 1.46 μV_{rms}, and the complete SoC consumes 40 μW under 3.0 V supply voltage, which makes it a great candidate for wearable biomedical applications.

CHAPTER 4

A 10-μA Biomedical SoC for High-Impedance 3-Lead ECG and Thoracic Impedance Monitoring

This chapter continues the discussion on multi-function biomedical acquisition system. Following the respiratory monitoring mentioned in Chapter 3, the proposed design increases the impedance measurement resolution without much power overhead, making it suitable for continuous impedance cardiography (ICG) [99] application. A positive current feedback loop for ECG channels is designed with care to increase the input impedance and hence the signal quality. Also the input locking through diodes are proposed to improve ECG amplifier reliability and settling time.

4.1 Introduction

Thoracic impedance cardiography is an emerging non-invasive technique to obtain the blood flow properties in the thorax [100]. It is measured by injecting

a high-frequency current between the neck and the trunk [101] to convert the impedance signal into the voltage. [102] suggested the first derivative thoracic impedance is highly related to the cardiac cycle, and can be used to timing the important intervals. The impedance variation data can be used as an early warning for conditions like pulmonary edema or pulmonary congestion [103]. For cardiac output evaluation, the impedance cardiography also has the advantages on connection simplicity as the electrode positions are not required to be accurate [104]. Thoracic impedance is also a direct approach to measure the ventilatory conditions [105].

Combined with the ECG measurement, thoracic impedance offers additional information on the systemic vascular resistance, and therefore are used to monitor the blood pressure (BP) or for guiding therapy for hypertension [106, 107, 108, 109]. This instrument tracks the changes in blood fluid volume during electrical systole, and provides reproducible results for systemic hemodynamics [110, 111, 112, 113].

A major problem to integrating the thoracic impedance measurement with the ECG sensor is the high power consumption. Recent designs such as [114, 115] consumes 40 μW for a single front-end channel, which exceeds the power budgets. In this chapter, a more efficient design is proposed, adopting the early demodulation first introduced in Section 3.3.4 in the previous design. This reduces the power consumption for the impedance amplifiers significantly.

This chapter is organized as follows. Following this introduction, Section 4.2 gives the system architecture overview. The focus is on the analog front-end designs, so the next Section 4.3 introduces the front-end blocks. This section highlights two major design innovations, i.e., the impedance feedback loop and ECG baseline settling acceleration. The chip measurement results and signals captured from volunteers are discussed in Section 4.4. Section 4.5 concludes this chapter.

4.2 System Architecture

The entire ECG + impedance system is illustrated in Fig. 4.1. It includes AFE for 3-lead 2-channel ECG acquisition, an impedance-to-voltage 2-channel amplifier, a 12-bit SAR ADC, a lossless ECG compressor, and a ECG QRS detector.

The ECG signals are first amplified through an AC-coupled low-noise IA, and filtered and amplified through the PGA in the next stage. The gain is tunable to maximize the dynamic range. An output buffer is used to improve the analog output settling for the sample-and-hold in the MUX. Two standalone ECG channels are integrated, aiming for 3-lead ECG acquisition purposes.

The impedance channel is similar to the architecture proposed in the previous chapter 3.2, but with much higher gain and resolution to measure the blood perfusion. The impedance is converted into the measurable voltage signal through the AC current source. Again, 2 separate channels are designed to capture both in-phase (I) and quadrature (Q) impedance information, which are related to the resistance and reactance accordingly. Aiming for finer resolution, the gain and the injected current are both increased in this design.

After digitized by the ADC [116], the ECG signal is further processed by the backend processor that consists of a lossless ECG compressor and a QRS peak detector. The main motivation for the compressor is to reduce the data rate and the wireless transmission power as a result [117]. Through a slope-based linear predictor to estimate the future values and store the error, the well-conditioned ECG signals can be compressed over 2 times without losing any information. A QRS detector is implemented and used at the heart rate detection mode, where the data rate could be as low as 1-2 Hz for ultra-low-power operation.

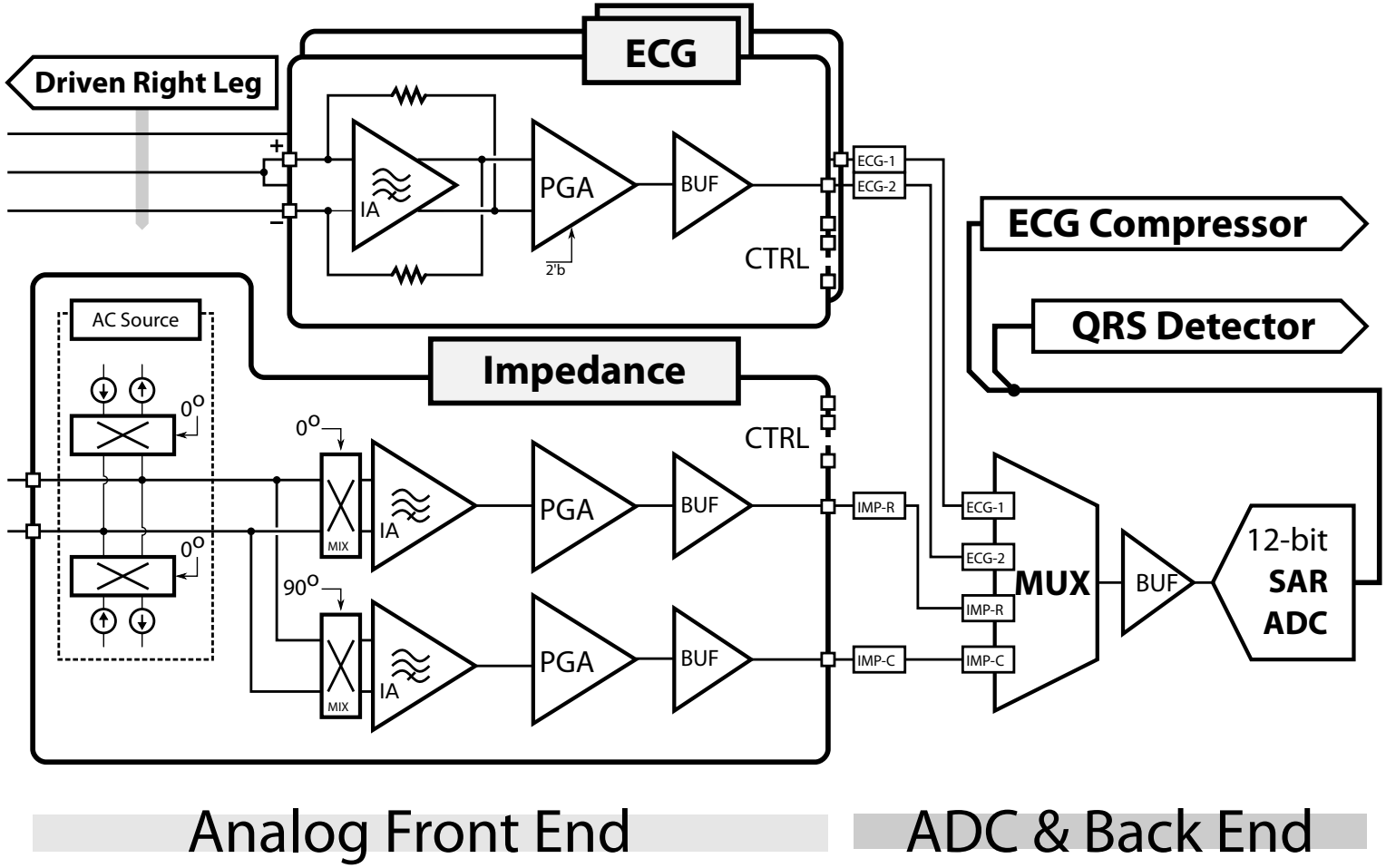

Figure 4.1: The ECG+Impedance system architecture.

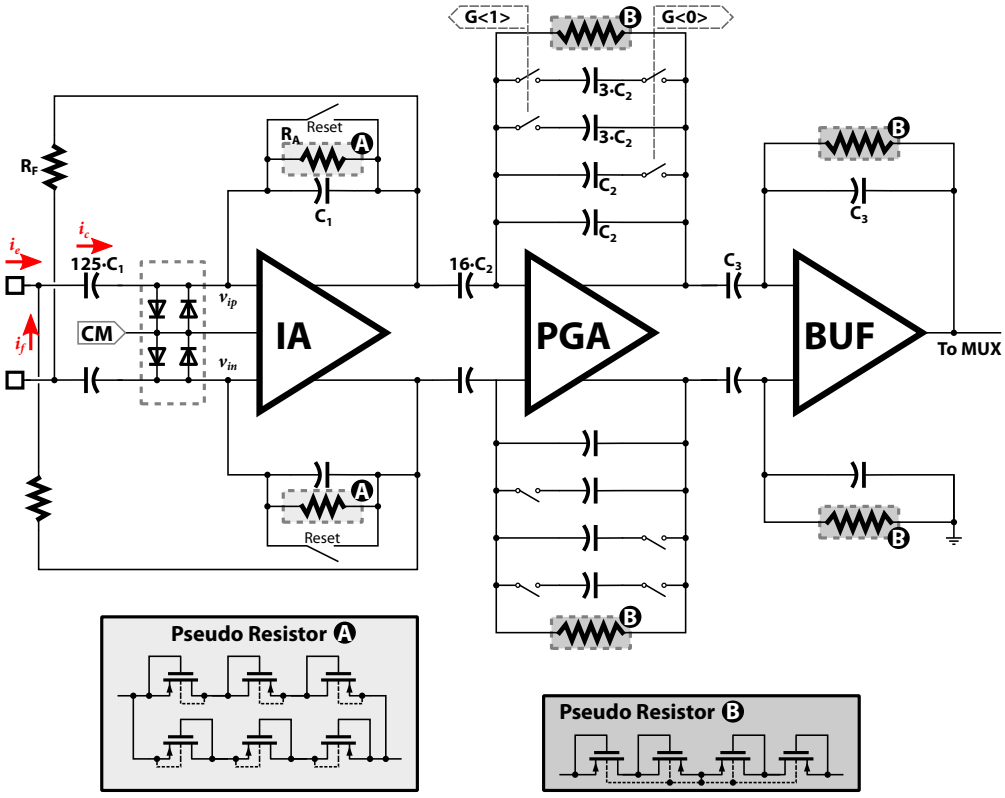

Figure 4.2: The AC-coupled analog front-end with impedance boosting and fast settling.

4.3 Analog Front-End Design Considerations

Fig. 4.2 shows the architecture of a single-channel ECG AFE. All the three stages—the instrumental amplifier, the programmable-gain amplifier, and the output buffer—are AC-coupled using capacitors to block the DC offsets. The high-pass cut-off frequency is determined by the first stage negative RC feedback through R_A and C_1. The gain of the IA is set at 125, and the PGA's gain is tuned from 2 to 16 through the digital control $G < 1 : 0 >$. The output buffer is also AC-coupled to support rail-to-rail output, without designing rail-to-rail input range at the cost of extra power.

Two unique pseudo resistors are used. The A-type design starts with three diode-connected PMOS transistors in series. To make it symmetrical a mirrored

copy is added in parallel. Fig. 4.3 shows the pseudo resistor I-V characteristic. The x axis is the voltage across the tested pseudo resistor, and the y axis is the current. When the voltage is limited within 0.5 V, the resistance is large enough to create a sub-0.1 Hz high-pass cut-off [13]. But if the voltage is much higher and close to 1.5 V, the current would be as high as 10 nA. Occasionally the high-frequency motion artifacts may drive the internal amplifier input voltage away from the designed common mode. In this situation higher feedback currents would improve the settling time and avoid the dead zone when the ECG is saturated. But a very-low high-pass corner frequency must be achieved using the same feedback loop at normal mode with small input. As analyzed above, the given A-type design does have much lower resistance at large voltage, and relatively high for small input. This A-type pseudo resistor is a perfect fit for the IA stage.

A different pseudo resistor (marked B in Fig. 4.2 and Fig. 4.3) is used for the PGA and the BUF. In order to utilize the full dynamic range of the ADC followed, the output ECG from the AFE would be close to full range. Under the circumstance, if the PGA and the BUF use the same A-type pseudo resistor for feedback, at high output amplitude a much larger current is flowed. This results in harmonic distortions for the output. To solve this problem, the B-type design with much larger resistance across the full range is adopted. Another advantage of using higher resistance is that the feedback capacitor C_2 and C_3 can be smaller than C_1 without limiting the high-pass corner.

The remaining part of this section will highlight another two design optimizations. The first one is to avoid amplifier locking for the IA stage and further reduce the settling time. The second one is to improve the input impedance and therefore obtain higher-quality ECG traces.

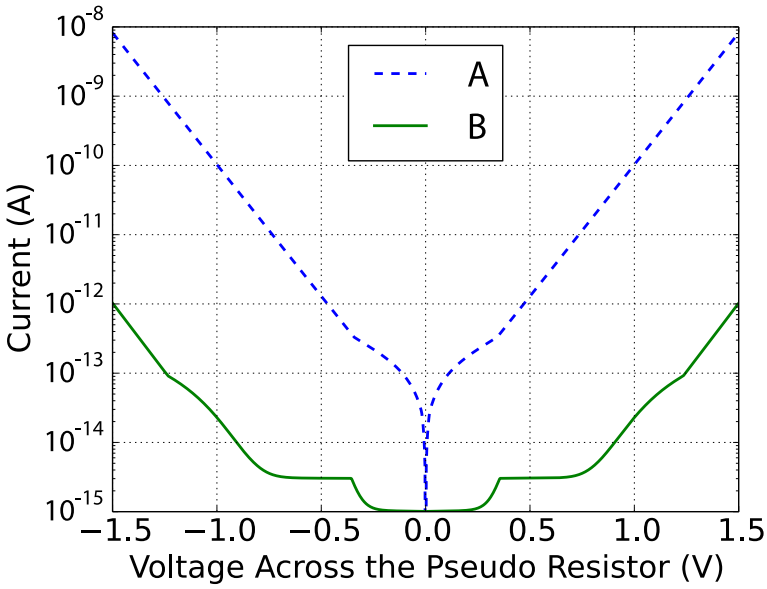

Figure 4.3: Comparing the two pseudo resistors.

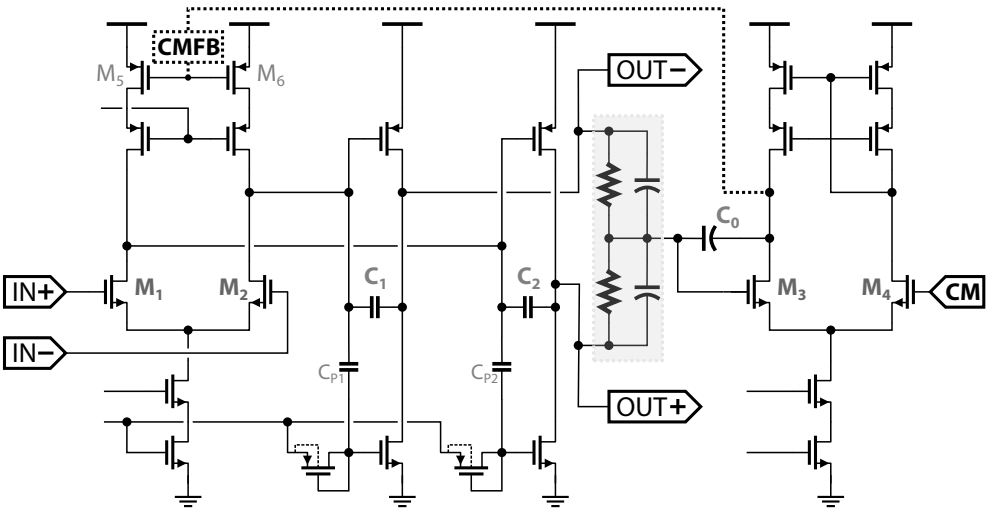

Figure 4.4: The fully-differential amplifier used in the IA stage, with common-mode feedback circuit.

4.3.1 Anti-Lock and Fast Baseline Settling

Fig. 4.4 gives the schematic for the internal amplifier use in the low-noise IA stage. It is a two-stage fully-differential amplifier, with a CMFB to fix the output common mode. From the main amplifier's outputs, two pseudo resistors marked in gray are used to extract the output common-mode signal, and compared with the system common mode (CM). Instead of using dedicated CMFBs for each stages, one CMFB is built to mitigate the output common mode drift for power saving. The CMFB output is directly connected to the current mirror in the first stage $M_{5,6}$. With the second stage and the CMFB input pair $M_{3,4}$, a three-stage feedback loop is created, and deserves much effort for phase compensation. The capacitor C_0, as well as the miller capacitors $C_{1,2}$ are all included to ensure stability for the common-mode feedback. Also, the gain of the CMFB is limited to avoid oscillations, which inevitably restricts the common mode tuning range.

Close-loop simulation for the IA stage shows that in certain situations when the inputs IN+ and IN- are accidentally driven to VDD or GND, the CMFB may be inadequate to pull the output voltage back, and the entire IA will be locked. Unless manually reset, the IA can no longer work as designed since the transistors are out of saturation region. This causes serious reliability issues for the entire front-end.

To solve the deadlock of the amplifier, two diodes in parallel and facing in the opposite direction are used to connect the amplifier inputs (v_{ip} and v_{in} in Fig. 4.2) and the common mode. Marked in dark background in Fig. 4.2, the diodes are open and acting as parasitics only during the normal operation. When the input voltage at v_{ip} and v_{in} are significantly away from the common mode, the diodes quickly pull the voltage back, and push the amplifier out of the deadlock region as described.

Moreover, the diodes help accelerate ECG baseline settling in a similar way as the A-type pseudo resistor mentioned before. When the input voltages are charged by the artifacts, the diodes pull them back close to V_{CM}. The diodes provide additional currents for input settling in case the given A-type design resistance is too large under process variation.

4.3.2 Impedance Boosting

High input impedance for the ECG front-end has several advantages, including higher signal amplitude and less affected by the motion artifacts and power-line interference [118, 20, 45]. AC-coupled amplifiers normally have high input impedance at the ECG band because of the capacitance. This subsection discusses the approach to further increase the impedance and improve the signal quality.

A basic idea to enhance the input impedance is by reducing the needed electrode current i_e when input voltage changes. A fixed current i_c must flow through the input capacitors with $125C_1$ under certain input voltage. To decrease the input current i_e, the current flowed through the capacitors i_c can be partially provided from other sources, rather than entirely from the electrodes. As shown in Fig. 4.2, a current feedback loop through R_F is added in each input port. When the input voltage changes, the current i_f through R_F will support part of the input current required by the capacitors, and therefore reduces the electrode current and increases the impedance.

To investigate the effects of positive feedback to the input impedance, the instrumental amplifier with the impedance boosting loop is redrawn in Fig. 4.5. The feedback resistor is modeled with resistance R_F and capacitance C_F. The IA's gain is G ignoring the feedback loop. C_p is the parasitic capacitor at the internal

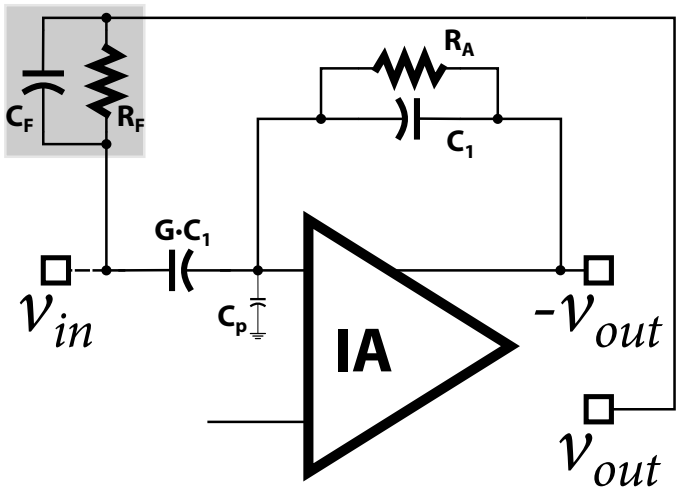

Figure 4.5: Analyzing the impedance boosting of the low-noise amplifier.

amplifier's input. The transfer function for the IA can be derived as follows.

$$A_{IA} = \frac{v_{out}}{v_{in}} = \frac{j\omega G R_A C_1}{1 + j\omega R_A C_1} \tag{4.1}$$

Therefore the transfer function for the voltage is indeed unaffected by the feedback loop, with unchanged gain G and 3-dB cut-off frequency $1/(2\pi R_A C_1)$ as analyzed in previous chapter 2.3.1. The main change bought from the positive feedback is that the input current required to drive GC_1 is reduced, and hence the input impedance increases, which is given by

$$I_{IA} = \frac{v_{in}}{i_{in}} \tag{4.2}$$

$$= \frac{1}{j\omega G C_1} \cdot \frac{1}{1 - \frac{(1+j\omega R_F C_F)\cdot[j\omega(G-1)R_A C_1 - 1]}{j\omega G R_F C_1 \cdot (1+j\omega R_A C_1)}} \tag{4.3}$$

$$= \frac{1}{j\omega G C_1} \cdot \frac{1}{1-F} \tag{4.4}$$

with

$$F = \frac{(1 + j\omega R_F C_F) \cdot [j\omega(G-1)R_A C_1 - 1]}{j\omega G R_F C_1 \cdot (1 + j\omega R_A C_1)} \tag{4.5}$$

where the F is the impedance boosting factor. The more F is close to one, the larger output impedance would be. At ECG frequency, the assumption $\omega R_A C_1 \gg 1$ is

valid, then

$$F = \frac{G-1}{G} \cdot \frac{1 + j\omega R_F C_F}{j\omega R_F C_1} \tag{4.6}$$

Given that $G = 125$ in the instrumental amplifier, and it is required to have $F < 1$ to avoid oscillation, C_F must be much smaller than C_1. Further assuming that $\omega R_F C_F \ll 1$, then we have

$$I_{IA} = \frac{1}{j\omega G C_1 - \frac{G-1}{R_F}} \tag{4.7}$$

Required by $I_{IA} > 0$ for all the ECG frequencies,

$$R_F > \frac{G-1}{2\pi f G C_1} \tag{4.8}$$

Now to compensate the impedance at the ECG signal frequencies, f is selected at about 1 Hz. Also C_1 is assigned with 10 pF. Then the feedback resistance must be larger than 0.32 TΩ. If the feedback capacitance C_F is fixed, lower R_F leads to higher input impedance and hence better signal quality.

It is impossible to use the passive resistors to implement such a large resistance on chip. Pseudo resistors are hence used for R_F. Due to the inevitable process variation for the pseudo resistors, it is very difficult to make sure the chip R_F is exact as required for maximum impedance boosting. Tunable pseudo resistors as proposed in [32] and etc. are therefore preferred, and the optimal impedance boosting could be achieved.

4.4 Measurements Results

4.4.1 Chip Performance

This entire system is fabricated in a 0.35-μm standard CMOS process. The total area is 3.04 mm × 2.2 mm shown in Fig. 4.6. The system can operate under a wide

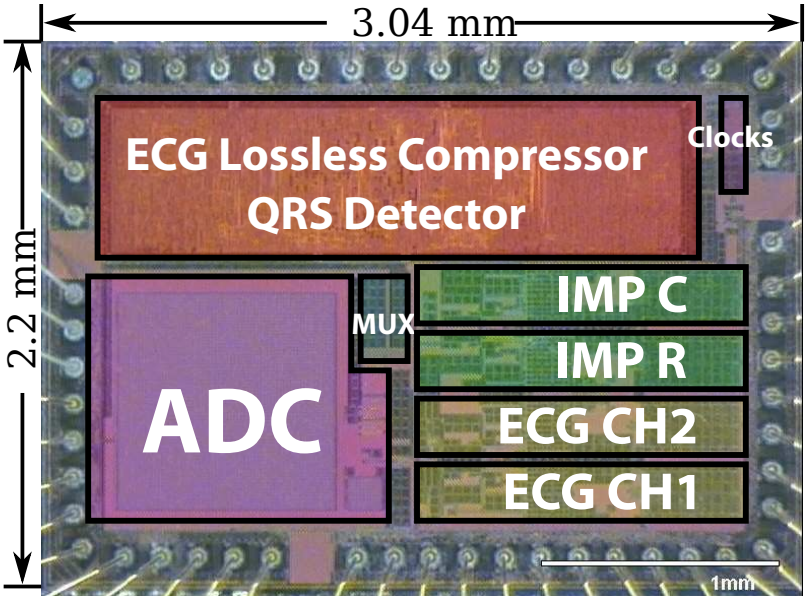

Figure 4.6: The 0.35 μm chip partition.

supply voltage from 1.8 V to 3.6 V. Table 4.1 summarizes the measurement results and Table 4.2 compares the impedance part with established designs in particular. The 0.1 Ω resolution is obtained by tuning an off-chip trimmer connected to the impedance channel input and monitoring the output response. Our design achives the lowest power under applicable resolution.

Fig. 4.7 gives the frequency response for the AFE, with passband gain tunable from 300 to 2400. The input-referred noise is plotted in Fig. 4.8, and the CMRR for the ECG channel is in Fig. 4.9. The effect of the impedance boosting is also evaluated. Shown in Fig. 4.10, the input impedance is about 10% higher when the positive feedback is turned on.

4.4.2 ECG and Impedance

The manufactured chip has been prototyped into an Arduino shield shown in Fig. 4.11. The SPI interface for the chip is directly connected to the Arduino board for bi-directional communications. The data is then send to the PC through USB

Table 4.1: Performance of the ECG+Impedance SoC

Parameter	Results
Single-Channel ECG AFE Current	1.25 µA
Gain Settings (G)	49.6/55.6/61.6/67.6 dB
High-Pass Corner	<0.07 Hz
Input-Referred Noise @ 0.5~250 Hz	1.95 μV_{rms}
Total Harmonic Distortion @ Full Scale (THD)	<0.71 %
Common-Mode Rejection Ratio (CMRR)	82 dB
Power Supply Rejection Ratio (PSRR)	70 dB
Impedance Channel Current	4.75 µA
AC Current Injected	0.1-160 µA
AC Current Source Frequency	8/16 kHz
Impedance Resolution	0.1 Ω
ADC Total Current	0.68 µA
Backend Total Current	1.05 µA
System Total Current	10.81 µA

Table 4.2: Comparison of the Impedance Readout Circuits

	This work	[67]	[79]	[21]
Injected Current	0.1 - 160 µA	27 - 117 µA	10 - 40 µA	30 µA
Source Type	square	pseudo-sine	pseudo-sine	square
Resolution	0.1 Ω	9.8 mΩ	10.5 mΩ	13.3 mΩ
Power	14.3 µW	58 µW	56.2 µW	335 µW

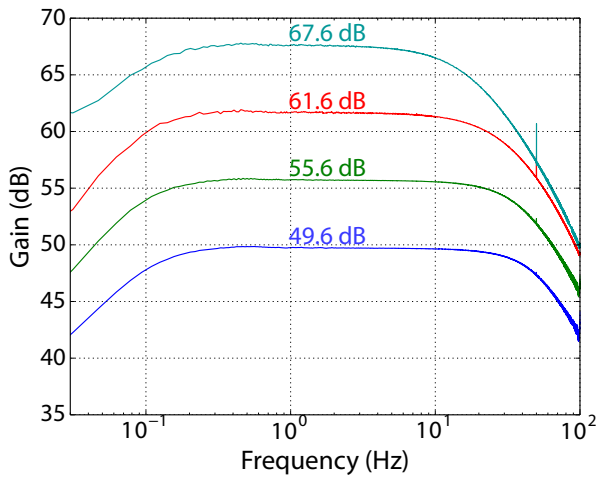

Figure 4.7: Frequency response with tunable gain configurations.

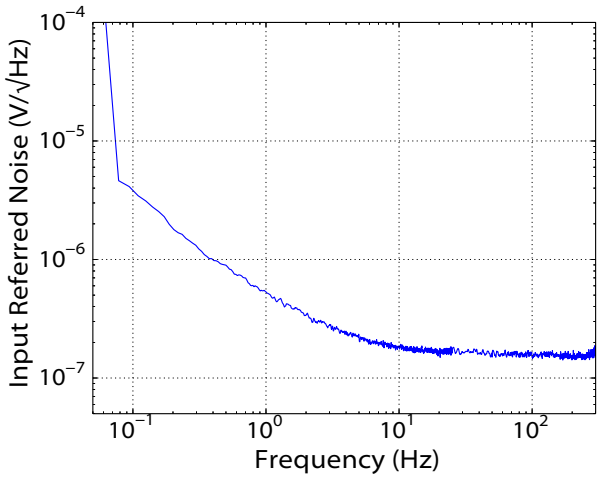

Figure 4.8: Input-referred noise.

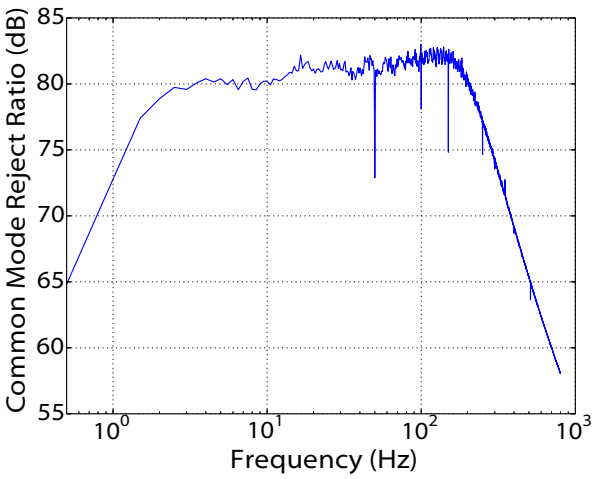

Figure 4.9: Common-mode suppression for a single ECG channel.

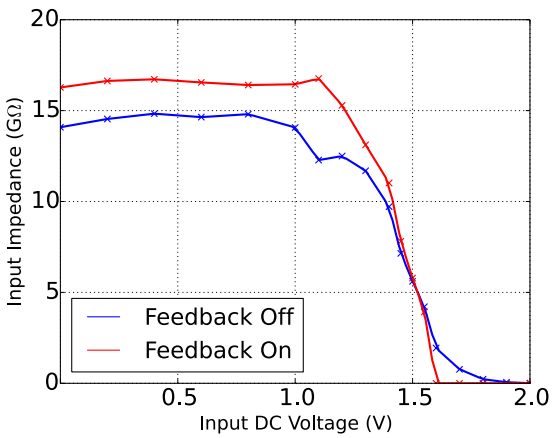

Figure 4.10: Measured input resistance.

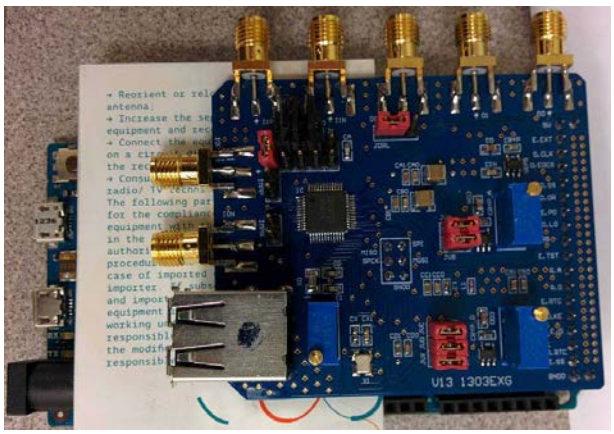

Figure 4.11: The ECG+impedance acquisition shield board for Arduino Due development board.

serial port. A graphic user interface in Python is written to visualize the output in real time, as shown in Fig. 4.12. The two plots on the left are the 2-channel ECG raw data using the 3-lead ECG connection. And the two on the right includes the resistance and reactance changes between the lead-II two electrodes LL and RA. Thanks to the high input impedance and DRL, the ECG traces are clean and not affected by the 50-/60-Hz mains noise.

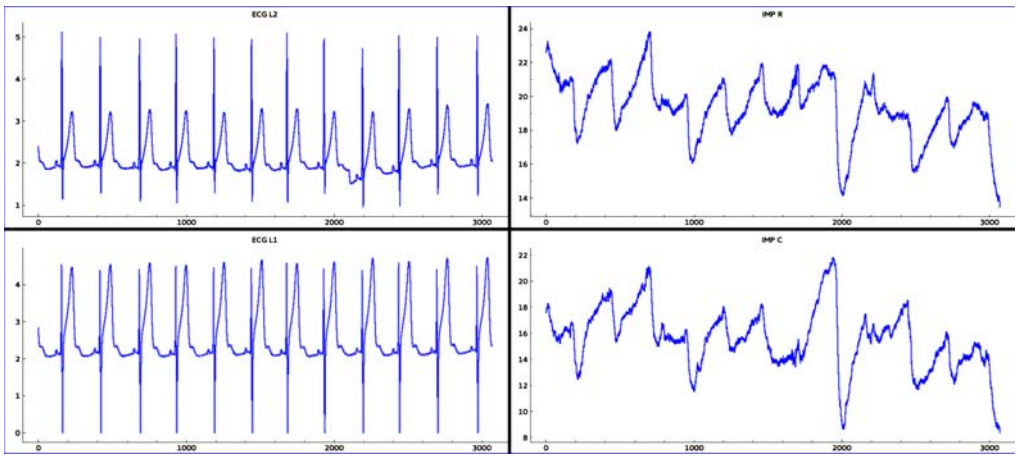

Figure 4.12: 2-channel ECG, resistance, and reactance real-time plot.

As an example of high-resolution impedance sensing, Fig. 4.13 gives the bioelectric impedance results using the RJL Systems Quantum Desktop Body Composition Analyzer and the designed low-power system. An inflatable cuff

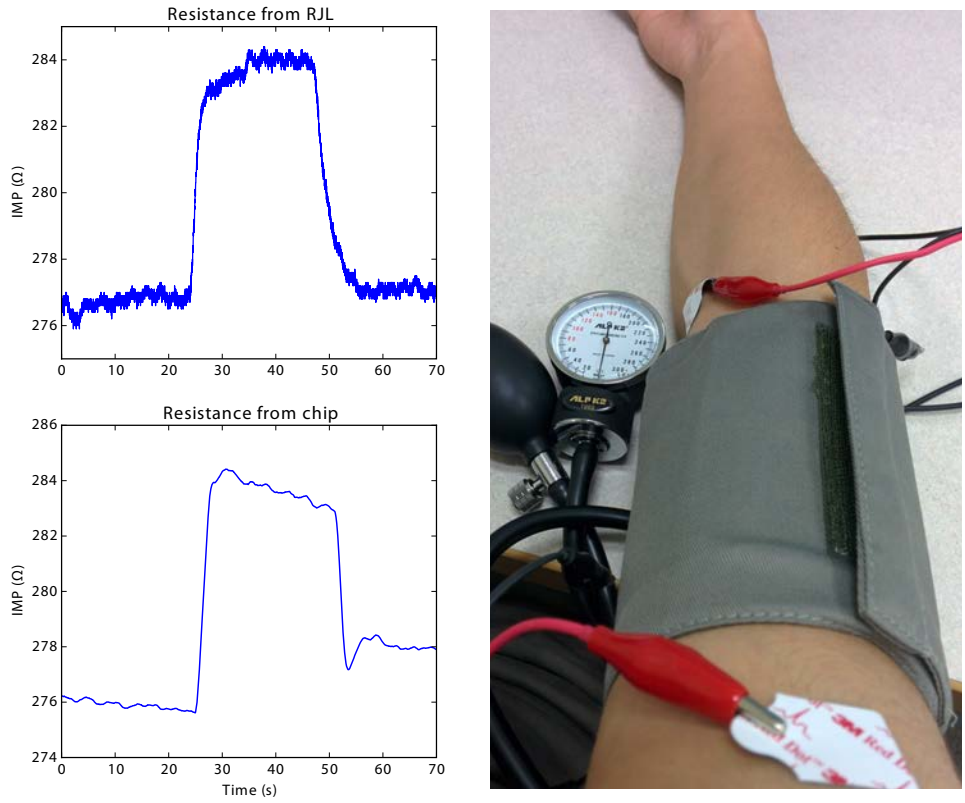

Figure 4.13: Impedance changes from blood flow control using the chip.

was placed around the upper arm to restrict blood flow, and the impedance at the two ends are measured. During 25-50 s the cuff was inflated to limit the blood flow, which should cause the impedance to rise at the beginning and fall back to normal afterwards. Due to the high-pass feature of the design, the plot using the chip in Fig. 4.13 is different from the RJL results. Nevertheless, the rise and fall trend is clearly visible, where the peak-to-peak changes are less than 8 Ω.

4.4.3 Towards Wearable Sensors

To integrate the final SoC in the final wearable device, the size of the device must be minimized to maintain its wearable feature. This means both the circuit board and the accessories like batteries and the surface electrodes should be as small as possible, which is only possible with low-power and high input impedance

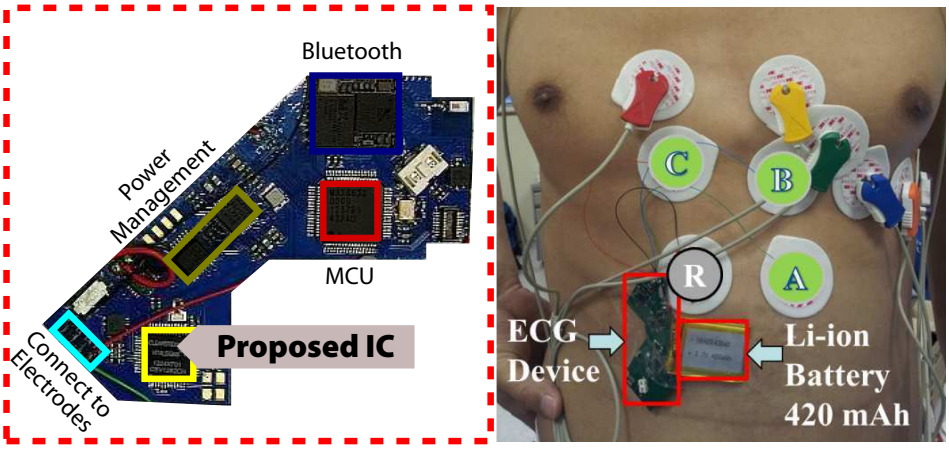

Figure 4.14: The wearable sensor prototype based on the proposed chip.

designs. On the left of Fig. 4.14 shows the circuit part of the integrated sensor. Besides the final chip, it mainly consists of the power management part for battery power, the Bluetooth module to transmit the ECG signal to personal gateway devices like smartphones or computers. The whole device can be powered using a 420 mAh Li-Ion battery for 1 - 2 weeks. Fig. 4.14 also gives the real-life setting when the device prototype is put on the chest.

4.5 Conclusions

This chapter presents a multi-functional biomedical ECG and impedance measurement system improved from the original design in Chapter 3. The main design efforts are on improving the ECG acquisition quality and reliability. By integrating low-power impedance measurement on the sensor, such a system can be further used for respiratory rate and dry weight monitoring towards a complete personal healthcare sensor.

CHAPTER 5

A 300-mV 220-nW Event-Driven ADC with Real-Time QRS Detection

This chapter presents an ultra-low-power event-driven ADC with real-time QRS detection for wearable ECG sensors. Two QRS detection algorithms, PUT and t-PUT, are proposed based on the level-crossing events generated from the ADC. The PUT detector achieves 97.63% sensitivity and 97.33% positive prediction in simulation on the MIT-BIH Arrhythmia Database. The t-PUT improves the sensitivity and positive prediction to 97.76% and 98.59% respectively. Fabricated in 0.13 μm CMOS technology, the ADC with QRS detector consumes only 220 nW measured under 300 mV power supply, making it the first nanoWatt compact analog-to-information (A2I) converter with embedded QRS detector.

5.1 Motivation & Literature Review

The first part of the thesis introduces several low-power AFE designs. For a complete wearable sensor with transmitter, most power is in fact consumed by the wireless transmitter. Therefore, the benefits from optimizing the AFE

power dissipation alone is rather limited. As mentioned in Section 3.2, significant power reduction in a wireless ECG system is only possible if the use of wireless transceiver is kept at minimum. This is achieved by either data compression or pre-filtering at the front-end and ADC side, as well as duty cycling the wireless transmitter. For example, when the heart rate information instead of full ECG signal is required, it is beneficial to perform signal processing tasks like QRS detection locally in the sensor part. In this circumstance, the data rate is as low as several bits per second, promising significant wireless power suppression. In other words, transmitting processed information is preferred over the raw data when the power is constrained.

This chapter presents a nanoWatt A2I system for QRS detection, which integrates signal processing tasks into an analog-to-digital converter without incurring much hardware overhead. Two algorithms, i.e. PUlse-Triggered (PUT) QRS detection and time-assisted PUT (t-PUT), are proposed. Both algorithms are verified in simulation using all 48 modified lead II (MLII) ECG client records from MIT-BIH Arrhythmia Database [119], with over 99% sensitivity and positive prediction for at least 2/3 of the total records. Compared to the Nyquist ADC based system, the event-driven nature of A2I system not only reduces the number of sample points, but also improves power efficiency [120]. The measurement results demonstrate the potential of the A2I system in terms of power efficiency and simplicity in hardware implementation.

The chapter is organized as follows. The remaining of this section briefly discusses the current research progress on event-driven ADC systems as well as QRS detectors. Section 5.2 introduces the system architecture of the ADC and QRS detector. Algorithms designed for QRS detection are presented and evaluated in Section 5.3. Circuit details are given in Section 5.4. Chip measurement results are discussed in Section 5.5. Conclusion remarks are drawn in the last section.

5.1.1 Level-Crossing ADC

Event-driven ADC can be implemented based on level-crossing scheme, i.e. the ADC generates a new output if and only if the amplitude of input changes by a given value, ΔV. The idea of asynchronous level-crossing sampling was initially proposed by H. Inose in 1966 [121]. Inose had also proposed the concept of delta-modulation as "generating coded pulses in accordance with a certain change in signal amplitude". In 1981 J. Mark mentioned that this level-crossing non-uniform sampling technique had potentials to compress data and therefore reduce the data rate [122]. In 1996 N. Sayiner discussed the effects of various non-idealities in both system level and circuit level [123]. This analysis was further enriched by E. Allier [124]. Recent years have also seen the development of adaptive level-crossing sampling system, aiming at further decrease data rate and related processing power [125] [126] [127] [128]. Also a few publications like [129] focus on the optimization of the ADC power, making it suitable for energy-constrained sensor applications.

In 2000s, researchers started to focus on the level-crossing sampled signal processing techniques. The sampled data is non-uniform and continuous in time domain, therefore it is incompatible with the mature digital signal processing (DSP) approach. Designs from M. Renaudin's group like [124] had adopted time quantization method on sampled data, and built full asynchronous design to perform filtering tasks [130] [131]. Other designs like [132] interpolated the output into uniform, equally-spaced data, or used time-mode signal processing [133]. Y. Tsividis's group, on the other hand, developed CT DSP systems without quantization time interval [134]. Specific delay element was designed for the CT DSP purpose [135]. By utilizing continuous delay element, the time accuracy was preserved and manipulated similar to digital filters.

The level-crossing-based ADC is much more efficient than that of Nyquist ADC for certain types of signal [120]. After the initial applications in speech processing [136] [124] and later ultrasound feature extraction [137], level-crossing ADCs demonstrated power advantages over Nyquist ADCs in biomedical sensing applications [127] [138]. The recent [128] introduces a time-varying comparison window and further reduces the output activity for sporadic input signals. The low-power sensor design in [63] showed significant data reduction using adaptive-rate ADC for ECG signal, which was mostly oversampled using Nyquist ADC as high frequency QRS complex only occurs in a short period of time. For higher frequency signals, Kurchuk also proposed the first level-crossing sampling system for GHz-range signals after reducing the internal delays of Tsividis's CT DSP architecture[139].

5.1.2 QRS Detection

QRS detection algorithms can be generally classified into two main categories: the frequency-domain analysis and the time-domain manipulation.

The frequency-analysis-based QRS detectors normally attain good accuracy and are robust against noise. [140] identified QRS by estimating the power spectral. First proposed in [141], wavelet transformation was also widely used. More recent works with circuit implementations like [142, 143, 144] also used various wavelets to improve the detection accuracy under various signal acquisition environments. Other methods include neural network [145, 146], genetic algorithms [147], adaptive filtering [148], and etc. Compared with the time-domain methods, their advantages on accuracy are often at the cost of hardware complexity.

In contrast, the time-domain approaches achieve reasonably good accuracy at low hardware complexity. Early work in [149] proposed using signal differentiation or slope to identify the QRS peaks. The famous Pan-Tompkins method in [150]

also relied on the slope, amplitude and width information, and it is still widely used in many computer-assisted QRS detection softwares. An improved version of Pan-Tompkins was published one year later in [151], discussing the threshold setting for different patients. Next, [152] proposed a Hilbert transform based approach to solve the threshold configuration for Pan-Tompkins algorithms and its variations. [153] has analyzed the performance of those QRS detectors using first derivative. A recent ECG processor design from [154] achieved remarkable power efficiency in 45 nm technology, thanks to the low computation load of the Pan-Tompkins detection algorithm.

A few other designs used cross-correlation for beat detection, such as [155, 156]. [157] analyzed the input morphology to extract the peaks and valleys. Circuit implementations in [158] based on multiscale mathematical morphology also demonstrated reasonable accuracy results. Depending on the information used and the order of derivatives, the time-domain approach can still be robust against various noise and artifacts [159].

The beauty of time-domain approaches is the possibility of combining signal processing with ADC as demonstrated in [160], in which the input-feature correlated (IFC) QRS detection algorithm is embedded into an A2I converter.

5.2 Event-Driven System Architecture

The architecture of the proposed event-driven QRS processor is shown in Fig. 5.1. The major block, an event-driven ADC [161], converts analog input into level-crossing (LC) events. The subsequent real-time QRS detection block extracts the QRS information from the ADC's output stream.

The event-driven ADC includes two asynchronous comparators, a digital-to-analog converter (DAC) and an asynchronous digital control unit consisting

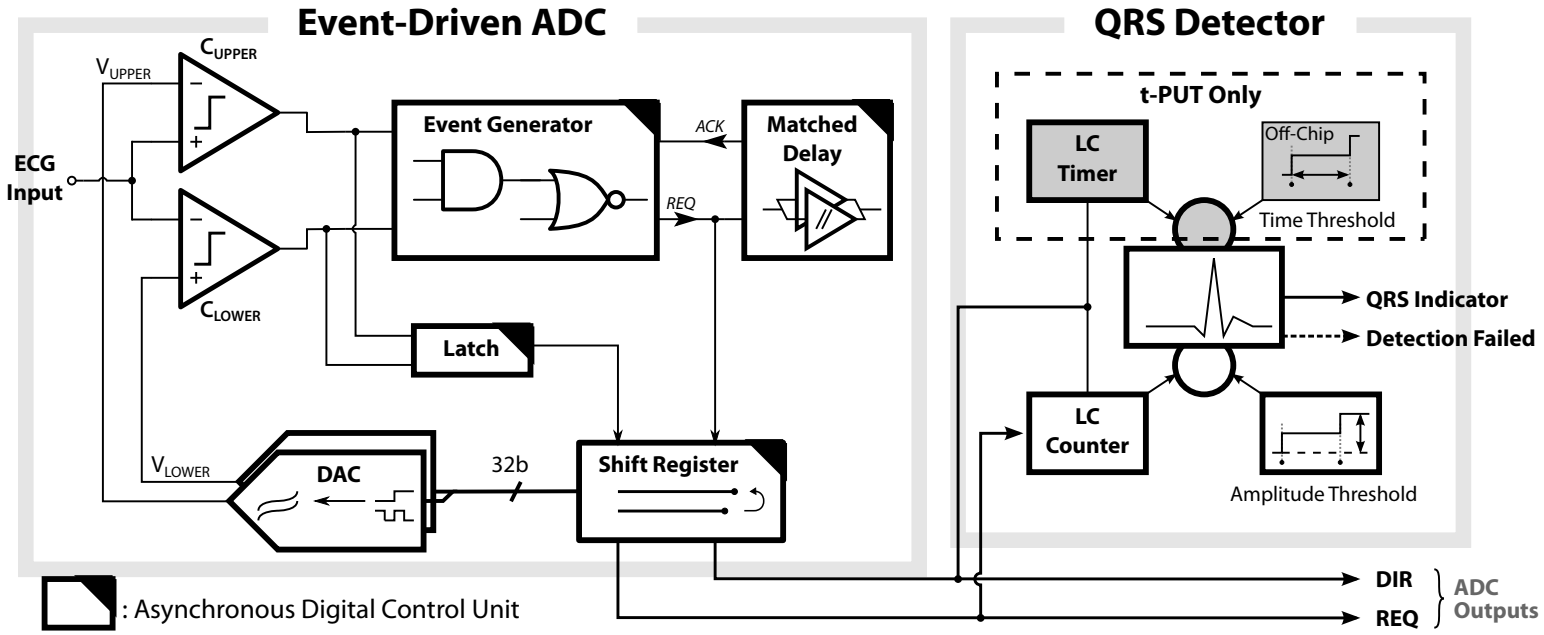

Figure 5.1: Diagram of proposed event-driven QRS processor.

of a latch, an event generator, a matched delay block and a shift register for event processing. The two comparators, C_{UPPER} and C_{LOWER}, continuously compare analog input with two voltage levels, V_{UPPER} and V_{LOWER}, generated by the DAC. The difference between V_{UPPER} and V_{LOWER} is one least significant bit (LSB) voltage ΔV. When the input voltage level rises above V_{UPPER} such that $V_{INPUT} > V_{UPPER} > V_{LOWER}$, the comparator C_{UPPER}'s output turns high while C_{LOWER}'s remains low. The latch's output is high, so the event generator increases the shift register's output by 1 bit, raising the DAC's outputs V_{UPPER} and V_{LOWER} each by ΔV. This process is defined as a RISE level-crossing event, or {RISE} for simplicity. If C_{UPPER}'s output remains high after V_{UPPER} and V_{LOWER} update, another {RISE} event follows and raises the DAC's output levels further. The matched delay block controls the minimal interval of two events, which is slightly longer than ADC loop delay. It ensures that the condition $V_{UPPER} > V_{INPUT} > V_{LOWER}$ is satisfied eventually after the comparators respond to the new values. Similarly, when $V_{INPUT} < V_{LOWER}$, the shift register's output is decreased by 1 bit, and the DAC lowers V_{UPPER} and V_{LOWER} each by a ΔV. This is referred as a FALL level-crossing event and noted as {FALL}.

The ADC's outputs are encoded as delta-modulated 2-bit stream [121], DIR and REQ, in our system as indicated in the lower right corner of Fig. 5.1. DIR represents the signal direction, i.e. the rise or fall of input voltage level. REQ indicates the occurrence of the {RISE} or {FALL} events. An example of the ADC outputs is illustrated in Fig. 5.2 for an ECG signal. Whenever there is a {RISE} (or {FALL}), event indicator REQ outputs a short pulse, and the level direction indicator DIR turns high to indicate a rise in voltage (or remains low for a voltage fall). Generated from {RISE} or {FALL} events by the digital control units, the REQ and DIR outputs represent the input activity, and are the input signals for the subsequent QRS detector.

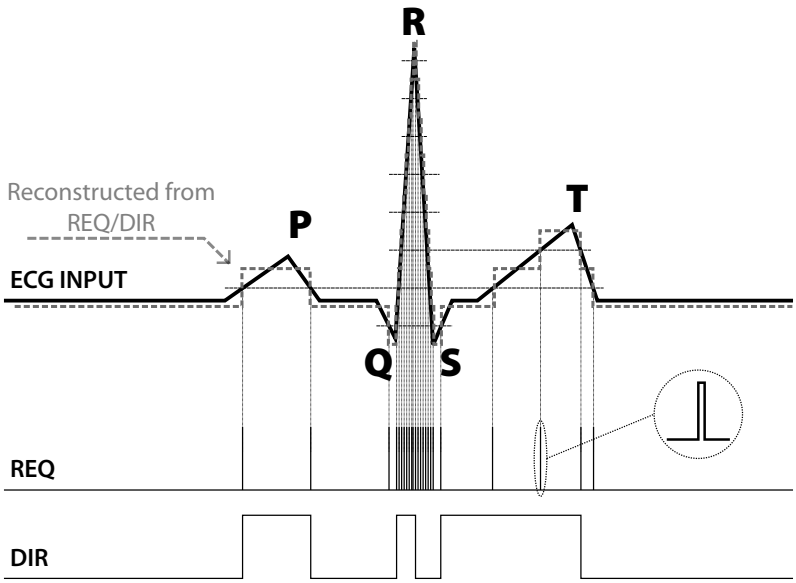

Figure 5.2: Delta-modulated event-driven ADC outputs for an ECG signal.

The QRS detector shown in the right part of Fig. 5.1 consists of a LC counter, an amplitude-threshold-setting block, and related logic controls. The t-PUT QRS requires additional timer and time-threshold-setting blocks. The blocks for t-PUT only are shaded in grey. They are switched off when only PUT is activated. Both the LC counter and the LC timer receive information from the ADC. The LC counter counts the number of monotonic {RISE} or {FALL} events. The LC timer measures the duration of every monotonic event sequence. Details about the QRS detection and circuit implementations are discussed in the following sections.

5.3 QRS Detection Algorithms and Performance Evaluations

5.3.1 QRS Detection Algorithms

The operational principle of PUT and t-PUT algorithms is illustrated in Fig. 5.3 and a flowchart is given in Fig. 5.4. As t-PUT is improved from PUT, the PUT

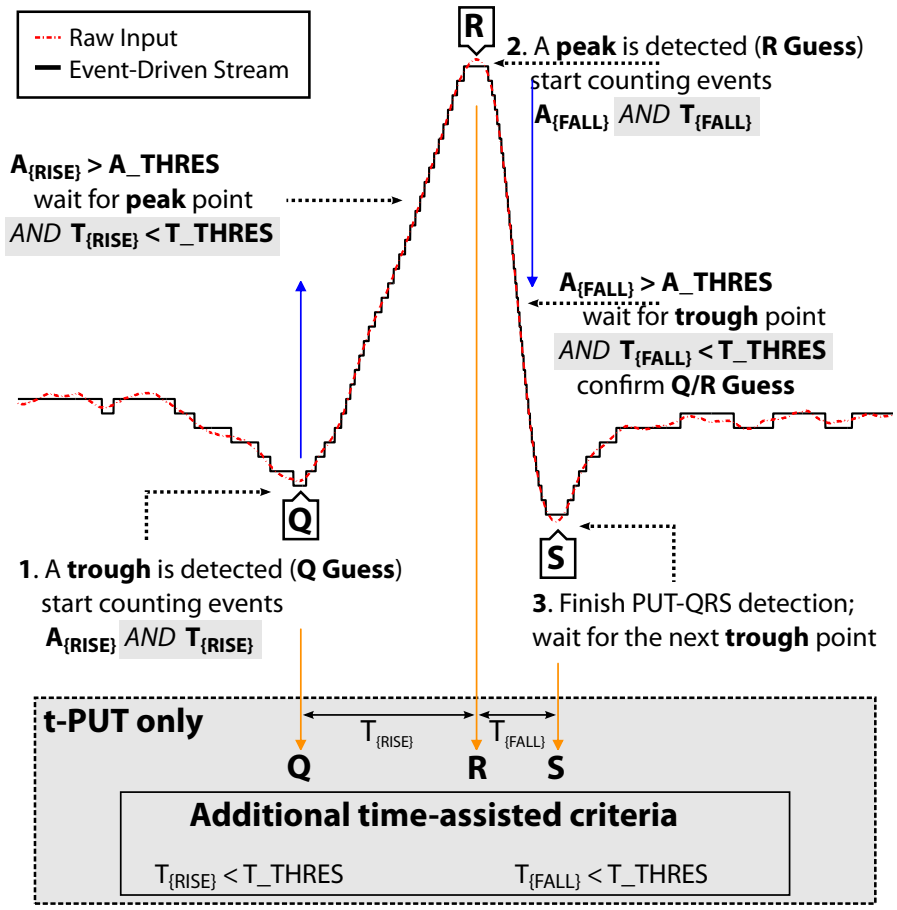

Figure 5.3: PUT and t-PUT QRS detection algorithms, with t-PUT related part in grey boxes.

algorithm is introduced first. The PUT involves three main steps.

1. The algorithm starts with identifying the Q wave. Every trough point in the input is a possible candidate of Q wave. It is identified by a {FALL} followed by a {RISE}, noted as a {FALL, RISE} sequence, in the ADC output. A valid Q wave should consist of a {FALL, RISE} followed by a number of uninterrupted {RISE} events. The LC counter in the QRS block tracks the number of uninterrupted {RISE} events. The counter starts counting when a {FALL, RISE} occurs. Each subsequent {RISE} event increases the counter by 1. The counter resets its value when one of the following two conditions is

met: (1) the pre-defined threshold value A_THRES is reached; (2) a {FALL} event occurs before the counter reaching A_THRES. A_THRES is defined as the minimal number of {RISE} events for a rising edge to be qualified as a Q-R interval. If the LC counter resets due to the first condition, the Q wave identification process completes and the algorithm moves to Step 2 for R peak detection. Otherwise, the algorithm goes back to beginning and waits for a new {FALL, RISE} sequence.

2. The R wave identification and confirmation start with peak detection. The identified peak is first marked as an unconfirmed R guess when a {FALL} is detected in the Q-R edge. This is referred as a {RISE, FALL} sequence. To confirm the detected peak is indeed an R peak, the LC counter starts to count the number of uninterrupted {FALL} events. The counter resets itself based on the two conditions similar to those in Step 1. The only difference is that the A_THRES represents the minimal number of {FALL} events for a falling edge to be qualified as an R-S interval. Note that it uses the same value of A_THRES for identifying Q-R and R-S intervals because of the similarity between these two intervals. If the counter resets due to the first condition, the R wave is successfully detected, i.e. the previous R peak guess is confirmed. The output "QRS Indicator" is asserted. The algorithm moves to next step to complete the detection process. Otherwise, the output "Detection Failed" is asserted. The algorithm goes to the beginning and waits for a new {FALL, RISE} sequence.

3. The S wave detection is straightforward, i.e. detecting the arrival of a {RISE} event on the R-S edge. Once the {RISE} is detected, the QRS detector resets the outputs and is ready for next QRS.

By choosing a proper A_THRES value, PUT-QRS is capable of distinguishing true QRS waves from P/T waves or small fluctuations, which are usually smaller in amplitude compared with QRS peaks. In our design, A_THRES is set to 7 for both Q-R and R-S edges, representing a 3-bit counter for the LC. A high-performance front end also improves the PUT-QRS performance by suppressing the noise and the power-line interference.

However, when a high T wave occurs or the amplitude of ECG signal changes abruptly, PUT-QRS may generate false QRS results under its fixed threshold setting. To solve this problem, a LC timer is added to improve the PUT-QRS, which is shown earlier in a grey box in Fig. 5.1. With the LC timer, the new time-assisted PUT makes use of both the amplitude (number of monotonic LC events) and the time (duration of monotonic LC events) information from the event-driven ADC's outputs.

The timing characteristics of QRS complex add another dimension to QRS detection [162] and form the basis for t-PUT QRS identification. A normal QRS duration is less than 0.1 second. Therefore a large pulse lasting longer than 0.1 second is unlikely to be a healthy QRS complex. This additional criterion helps to differentiate the true QRS complex from other large pulses.

The additional components in t-PUT are highlighted with grey shaded areas in Figs. 5.3 and 5.4. It can be seen that a LC timer and a time threshold T_THRES are introduced in t-PUT. The T_THRES is defined as the longest possible duration of a Q-R (or an R-S) wave. Although the LC counter and the LC timer count the amplitude and the duration of a rising (or falling) edge, the operations of these counters are different. The LC counter resets itself once its value reaches A_THRES or a {FALL} (or {RISE}) arrives before it accumulates to A_THRES. The LC timer, on the other hand, does not stop counting until a {FALL} (or {RISE}) occurs in a Q-R (or an R-S) edge. The Q-R or R-S edge is confirmed in t-PUT

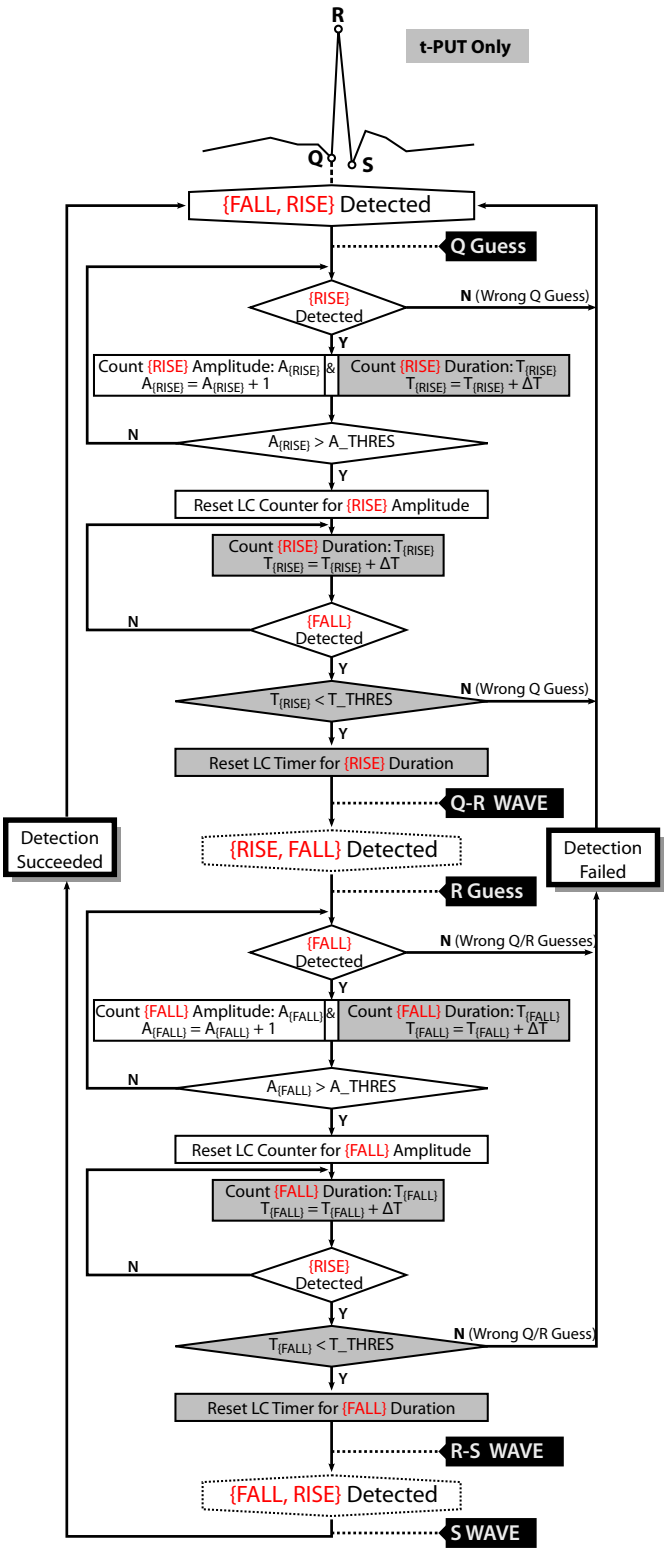

Figure 5.4: PUT and t-PUT QRS detection flowchart, where time-based steps for t-PUT in greyed boxes are turned off for PUT.

algorithm only if the timer value T is less than T_THRES and counter value A > A_THRES. Such additional criterion improves QRS detection accuracy over PUT, especially for ECG signals with large P or T waves. The benefits of t-PUT are covered in the performance evaluations.

5.3.2 QRS Detector Performance Evaluations

The proposed PUT and t-PUT algorithms are evaluated by all records in the MIT-BIT Arrhythmia Database. For PUT QRS detector, simulation shows the detection accuracy varies depending on the ECG signal quality and characteristics. Of the 48 records in total, 29 records have less than 1% errors, and 39 records have less than 5% errors. The detection errors are either missed peaks (false negative errors) or mistakenly identified peaks (false positive errors). PUT-QRS faces difficulties in identifying some QRS peaks correctly in the remaining 9 records. The main reasons are given below.

1. The T wave is high, i.e. the amplitude of T wave is comparable to the nearby QRS. In such cases, the PUT-QRS detector marks the T wave as R mistakenly, incurring a false positive error. Examples include ECG with multiform premature ventricular complexes (PVCs) like 106, 107, and 217. This issue can be partly solved by using the improved t-PUT QRS algorithm.

2. The local QRS height varies greatly within the 30-minute records. The changes in amplitude in these cases vary from 0.3 mV to 1.8 mV. A fixed A_THRES value can hardly handle such wide dynamics. Records 106, 108, 200, 203, and 233 belong to this category. All these records show multifocal or multiform PVCs. One way to address this issue is to make A_THRES programmable, such that A_THRES adapts to the input signal.

3. Power-line interference (Record 207) and noise (Record 210) during ECG capture make QRS detection difficult. Since the signals from MIT-BIH are pre-filtered, high-performance front ends with good CMRR, PSRR and signal conditioning is required to achieve the similar accuracy results under clinical trials.

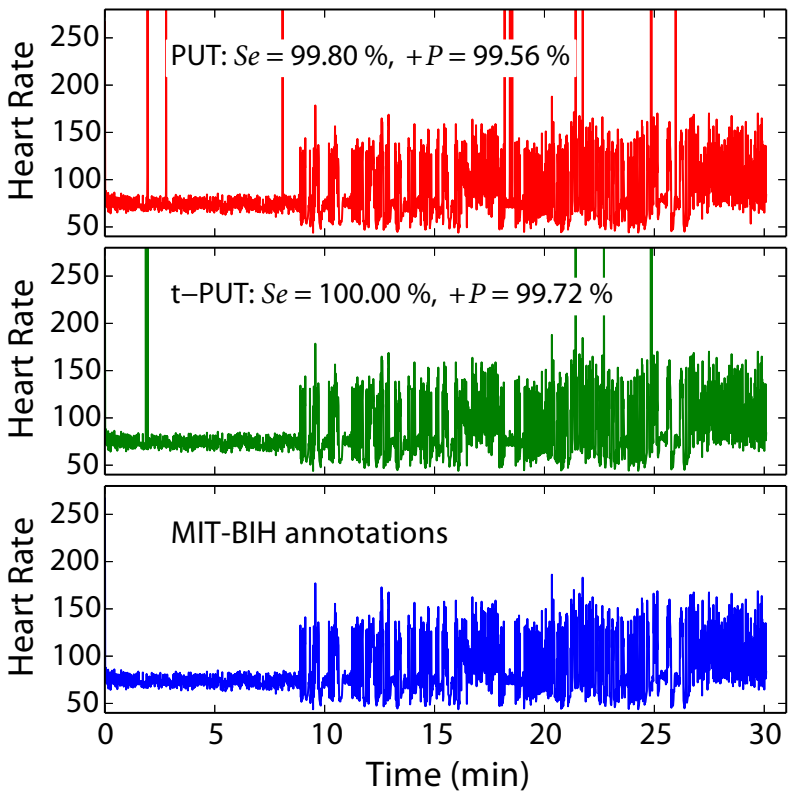

Figure 5.5: Heart rate calculated based on R-R interval.

The time-assisted PUT detector addresses the detection errors due to high T wave. The additional time information is used to filter out T waves which are high in amplitude but last much longer than that of a normal QRS complex. Fig. 5.5 shows the instant heart rates calculated from both detectors and annotated heart rates in the database. The input is a 30-minute ECG from Record 222. The upper graph is the result from PUT-QRS detector. There are 11 large positive spikes shown in the PUT heart rate, each representing a false positive detection error.

Also there are 5 missed beats in PUT-QRS. The plot in the middle shows the result from the t-PUT algorithm, and lower one is the annotated heart rates from the MIT-BIH database. All the false negative detects and some false positive detects are corrected in t-PUT QRS. The rest false positive errors are due to the changing QRS height, which cannot be handled error-free using a single threshold.

Table 5.1: Performance of Pulse-Triggered and Time-Assisted Pulse-Triggered QRS Detectors

Tape ID	**Total Peaks**	**PUT FN**	**PUT FP**	**PUT Se(%)**	**PUT +P(%)**	**t-PUT Se(%)**	**t-PUT +P(%)**
100	2273	0	0	100.00	100.00	100.00	100.00
101	1865	2	0	99.89	100.00	99.89	100.00
102	2187	2	1	99.91	99.95	99.91	99.95
103	2084	0	0	100.00	100.00	100.00	100.00
104	2229	29	44	98.72	98.06	99.02	98.67
105	2572	29	45	98.89	98.28	98.09	99.27
106	2027	190	64	91.43	96.94	94.28	96.02
107	2137	20	1295	99.07	62.27	97.62	99.81
108	1763	210	17	89.36	99.04	89.36	99.04
109	2532	51	7	98.03	99.72	98.03	99.72
111	2124	59	6	97.30	99.72	97.30	99.72
112	2539	0	0	100.00	100.00	100.00	100.00
113	1795	0	0	100.00	100.00	100.00	100.00
114	1879	11	7	99.42	99.63	99.47	99.68
115	1953	0	0	100.00	100.00	100.00	100.00
116	2412	21	2	99.14	99.92	99.14	99.92

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Table 5.1 – *Continued from previous page*

Tape ID	Total Peaks	PUT FN	PUT FP	PUT Se(%)	PUT +P(%)	t-PUT Se(%)	t-PUT +P(%)
117	1535	0	4	100.00	99.74	100.00	100.00
118	2278	24	70	98.96	97.02	99.35	97.56
119	1987	0	0	100.00	100.00	100.00	100.00
121	1863	3	0	99.84	100.00	99.84	100.00
122	2476	0	0	100.00	100.00	100.00	100.00
123	1518	0	0	100.00	100.00	100.00	100.00
124	1619	13	3	99.20	99.82	99.57	99.88
200	2601	480	316	84.42	89.17	84.42	89.17
201	1963	7	38	99.64	98.10	99.44	99.34
202	2136	10	5	99.53	99.77	99.86	99.72
203	2980	483	342	86.05	89.70	86.05	89.70
205	2656	33	23	98.77	99.14	99.07	98.99
207	2332	324	138	87.80	94.41	87.80	94.41
208	2955	32	23	98.93	99.23	98.93	99.23
209	3005	3	1	99.90	99.97	99.90	99.97
210	2650	143	65	94.88	97.61	97.25	96.12
212	2748	0	0	100.00	100.00	100.00	100.00
213	3251	23	8	99.30	99.75	99.30	99.75
214	2262	14	23	99.38	98.99	99.38	98.99
215	3363	31	11	99.09	99.67	99.09	99.67
217	2208	247	55	89.94	97.57	92.00	99.82
219	2154	16	5	99.26	99.77	99.26	99.77

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Table 5.1 – *Continued from previous page*

Tape ID	Total Peaks	PUT FN	PUT FP	PUT Se(%)	PUT +P(%)	t-PUT Se(%)	t-PUT +P(%)
220	2048	0	1	100.00	99.95	100.00	99.95
221	2427	18	8	99.26	99.67	99.26	99.67
222	2483	5	11	99.80	99.56	100.00	99.72
223	2605	23	107	99.12	96.05	97.90	98.90
228	2053	44	53	97.90	97.48	97.90	97.48
230	2256	1	1	99.96	99.96	99.96	99.96
231	1571	0	0	100.00	100.00	100.00	100.00
232	1780	7	3	99.61	99.83	99.61	99.83
233	3079	57	213	98.18	93.53	98.18	93.53
234	2753	0	0	100.00	100.00	100.00	100.00
Total	**109966**	**2665**	**3015**	**97.63**	**97.33**	**97.76**	**98.59**

The complete QRS detection results for PUT and t-PUT are listed in Table 5.1. Sensitivity (Se) and positive prediction (+P) are used to represent the detection accuracy.

$$Se(\%) = \frac{TP}{TP + FN} \tag{5.1}$$

$$+P(\%) = \frac{TP}{TP + FP} \tag{5.2}$$

where TP is the number of total QRS peaks from database annotations, FN is the number of false negative errors, and FP is the number of false negative errors.

One advantage of PUT-QRS algorithm is its very low hardware complexity and potential for low power implementation. More importantly, the simplicity of PUT-QRS does not drastically reduce the detection accuracy as shown in Table

5.1. Further improvements can be made to PUT algorithm by making A_THRES programmable, which can be tuned by either physicians or a calibration algorithm.

The performance of PUT and t-PUT QRS detectors is compared with some well-established methods based on traditional DSP techniques and an A2I based QRS detector as shown in Table 5.2.

Table 5.2: Performance Comparison with Published QRS Detection Methods

Method	Se(%)	+P(%)	Ref
Wavelet Transform	99.90	99.94	[141]
Input-Feature Correlated	79.33[a]	98.55[a]	[160]
Filter Bank	99.59	99.94	[163]
Genetic Algorithm	99.60	99.94	[147]
Mathematical Morphology	99.38	99.94	[157]
PUT	97.63	97.33	–
t-PUT	97.76	98.59	–

[a] Results using all records in MIT-BIH database based on our simulations without 5 Hz - 35 Hz bandpass filtering.

It can been seen that the DSP based methods achieve better sensitivity and positive prediction at the cost of high computational complexity. A similar A2I based QRS detector named IFC A2I converter was proposed in [160]. The IFC method is the first reported A2I system for QRS detection and is the closest match to the proposed algorithms. Both IFC and our proposed detectors are based on level-crossing event processing. But there are notable differences between them. The IFC QRS uses the voltage values of previously detected Q troughs and R peaks as references to determine the current trough and peak. The detection starts with finding a Q wave among possible troughs. If a trough's voltage is higher than 50% of the average value of previous troughs, this average value itself is updated. Further, if this trough is higher than 70% of the previous average, this trough is marked as Q point. After confirming the Q point, IFC detects the R

peak by checking the next peak's voltage in a way similar to Q point detection. In summary, the IFC QRS uses prior knowledge of trough and peak points to identify the current R peak, while the PUT and t-PUT algorithms use only local information to detect the R peak. PUT and t-PUT do not involve any arithmetic units while IFC performs moving average and multiplication in continuous-time domain. Both t-PUT and IFC use time information in the detection process. t-PUT relies on time information to differentiate between QRS complex and non-QRS peaks while IFC uses time data for slope measurements. IFC works well with adaptive asynchronously sampled data, while PUT requires all LC samples are equally spaced in amplitude.

Our extensive simulations also suggest that the proposed PUT and t-PUT algorithms are robust when handling abnormal ECG signals. The reasons are two-fold. First, the PUT treats each QRS independently, which promises fast start-up and consistent result for every QRS peak. Second, the PUT detector is less affected by low-frequency noise and baseline fluctuations. It can quickly recover from detection errors even when there are abnormal peaks or troughs. Fig. 5.6 illustrates a section from Record 105, which has two exceptional pulses, one high R peak and one low trough. The unexpected high R peak affects the detection accuracy if previous peaks are involved in the decision of current peak as IFC does. Similarly, a sudden low trough drastically changes the average value for Q troughs, and leads to detection errors in the subsequent Q waves. It is clear from Fig. 5.6 that the PUT handles such abnormal ECG well.

5.4 Circuit Design Considerations

ECG signals are within the frequency band of 0.05 Hz ~ 250 Hz. Such a low frequency allows the proposed event-driven system to work at a very low speed.

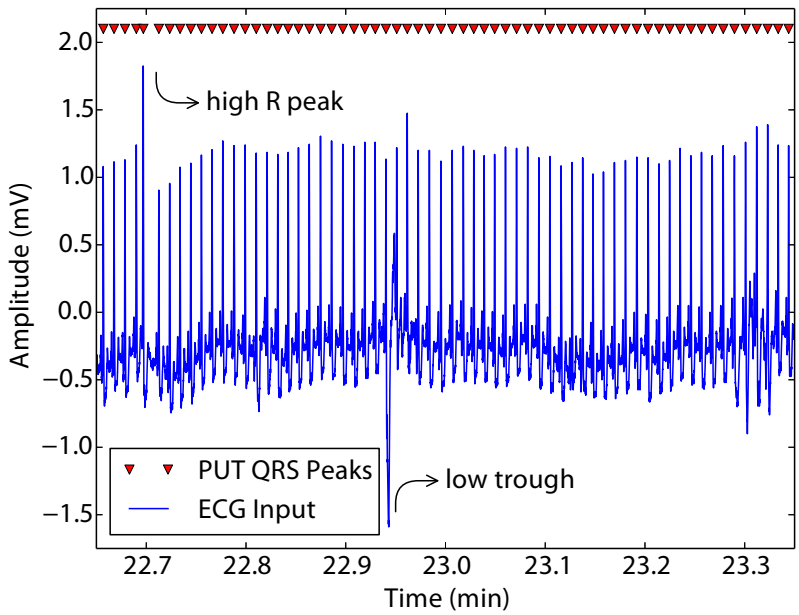

Figure 5.6: Simulated QRS detection results for abnormal ECG signals.

This feature provides us an opportunity to aggressively lower the supply voltage to 300 mV. As discussed in [123, 164, 165], the performance of event-driven ADCs is mainly determined by ADC's feedback loop delay, the comparator's resolution, and the DAC's resolution. Under 300 mV supply voltage, all transistors operate in the subthreshold or cutoff region. The static current for analog blocks such as comparators is substantially reduced, which restricts the circuit speed and input voltage range. The designer needs to find a proper balance between power consumption and system performance. This section highlights the design considerations under such a low supply voltage.

5.4.1 300 mV Process-Insensitive Comparator

The three-stage comparator used in our proposed design is shown in Fig. 5.7. Stage 1 is a differential amplifier with rail-to-rail input range [166]. Stage 2 provides gain for the comparator and Stage 3 is an inverter buffer generating full-scale output. Several factors should be considered when designing under 300mV.

First, the rail-to-rail input range is crucial for analog circuits when supply voltage is reduced. This requires both PMOS and NMOS differential amplifiers for the first stage. In Stage 1, M_{P3} and M_{P4} are the active loads for $M_{N1,2}$ NMOS input pair. With current tail M_{NB}, they form an NMOS differential amplifier. Similarly, M_{PB}, $M_{P1,2}$, and $M_{N3,4}$ build up a PMOS amplifier. Both amplifiers' outputs are connected through four transistors highlighted in grey in Fig. 5.7. These four transistors generate outputs V_{O1} and V_{O2} of Stage 1 by averaging the outputs of NMOS and PMOS amplifiers.

Second, high CMRR provides reliable open-loop gain under any input situations. Since V_{O1} is connected to the two diode-connected loads M_{P3} and M_{N3}, its voltage depends little on the input. By proper sizing, V_{O1} is set at 130 mV, which biased the input PMOS transistors of Stage 2 $M_{P5,6}$ in moderate inversion region with enough headroom. Through this common-mode shifting [167], Stage 2 is able to generate high differential gain regardless of the input voltage. Without Stage 1, the gain of Stage 2 and the output delay severely depend on the input common-mode as the V_{DS} of the tail PMOS M_{PB2} is small. Considering V_{O1}'s insensitivity to input voltages, all the current tails are biased using V_{O1}. This voltage biasing technique has a disadvantage that the total current of Stage 1 is exponential to the supply voltage. But it saves the extra biasing circuits and current, and the performance is guaranteed in wide supply voltage [166].

Last but not least, the comparator uses large transistors to suppress process variation, flicker noise, and input offset. In Stage 1, the length for $M_{P1,2}$ and $M_{N3,4}$ is 3 μm. The cross-coupled loads in Stage 2 increases the DC gain. To avoid negative loading, the cross-coupled NMOS transistors are half the size of the diode-connected ones in this stage. Post-layout simulations under all corners and temperature from -10 °C to 80 °C show the comparator has delay less than 3.6 μs and ENOB over 8.1 bits under 300 mV supply. The comparator also fully operates

under power supply from 0.2 V through 1.2 V, with all-situation worst-case delay of 34.6 µs and ENOB of 7.2 bits.

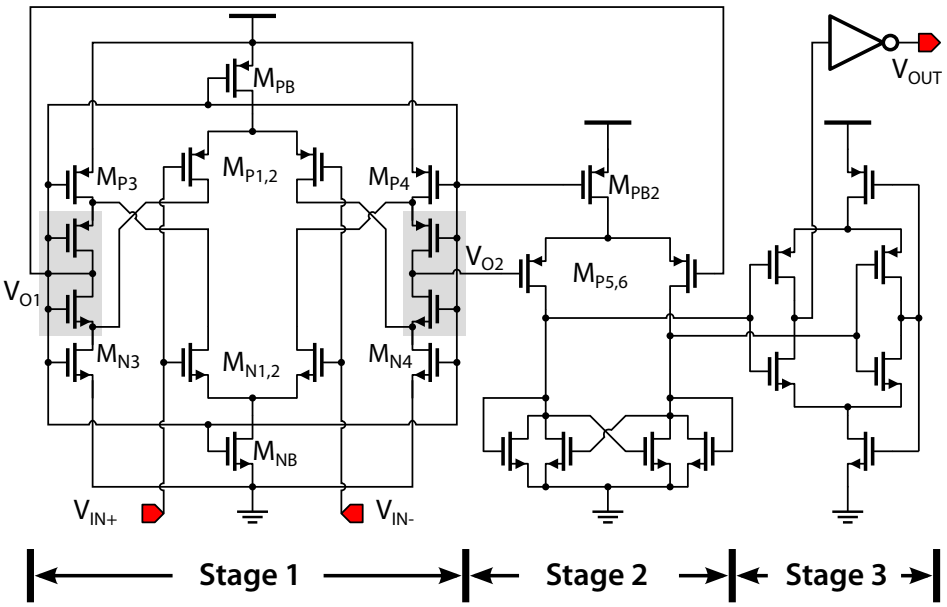

Figure 5.7: 3-stage comparator used in the event-driven ADC.

5.4.2 Low-Voltage DAC and System Hysteresis

Fig. 5.8 shows the 5-bit DAC architecture. It generates two voltage references V_{UPPER} and V_{LOWER} from one string resistor ladder network. The DAC connects V_{UPPER} and V_{LOWER} to specific voltage levels through bootstrapped switches [168], which are controlled by the 32-bit shift register block. Simulations show that 5-bit DAC resolution is sufficient for reliable PUT QRS detection. The increase of resolution improves the QRS detection accuracy, especially for ECGs with large variation in amplitude. However, higher resolutions require better resistor matching and less feedback delay, which lead to higher power consumption and larger chip area.

The DAC includes 10% hysteresis V_H for both V_{UPPER} and V_{LOWER} within each LSB ΔV to mitigate noise and fluctuations. Hysteresis removes erroneous

level-crossing events due to noise, interference, or other fluctuations. The exact hysteresis value is set by the resistor ratio. As shown in Fig. 5.8, a resistor of 2R is inserted between 6R (or 7R) resistors. The difference between V_{UPPER} and V_{LOWER} is slightly larger than 1 LSB ΔV. In most cases when one of the switches T<1:30> is on, we have

$$\begin{aligned} V_T &= V_{UPPER} - V_{LOWER} \\ &= \frac{2R + 6R + 2R}{2^5 \cdot (2R + 6R)} V_{DD} \\ &= 125\% \cdot \Delta V \end{aligned} \tag{5.3}$$

In this implementation, each R is about 13 kΩ. By using a different resistor ratio, the hysteresis value changes accordingly. Increasing hysteresis improves PUT and t-PUT detection accuracy by filtering out noise. However, higher hysteresis removes ECG details, resulting in poorer ADC performance. A 10% hysteresis seems to be a good balance between QRS detection accuracy and ADC performance according to our simulations.

The switch design is given in Fig. 5.9. All switches used in DAC are bootstrapped. As linearity is not an issue for small signals, an extra PMOS, circled in grey in Fig. 5.9, is added to boost the conductivity. It further improves the circuit speed and DAC accuracy under 0.3 V.

5.4.3 Asynchronous LC Timer and Delay Cell

The level-crossing timer used for time measurement in t-PUT is shown in Fig. 5.10. It contains 16 asynchronous unit delay cells and a counter, all connected in a loop. The LC timer measures the duration from a rising edge to the following falling edge (or from a falling edge to the following rising edge) of the DIR signal, which corresponds to the duration of uninterrupted {RISE} (or {FALL}) events. The rising and falling edges of DIR signal are first converted to a pair of START and

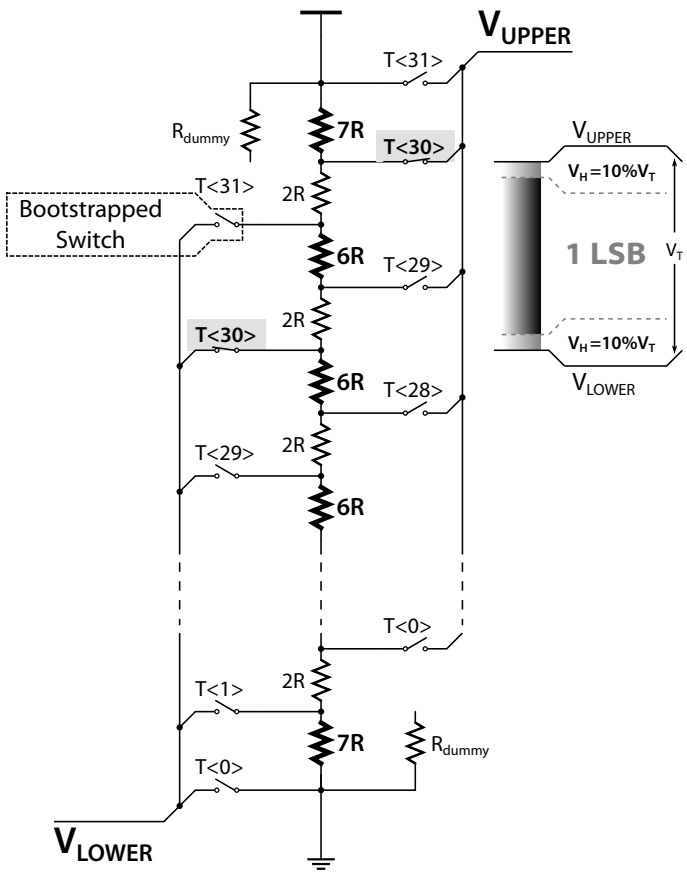

Figure 5.8: DAC design with hysteresis.

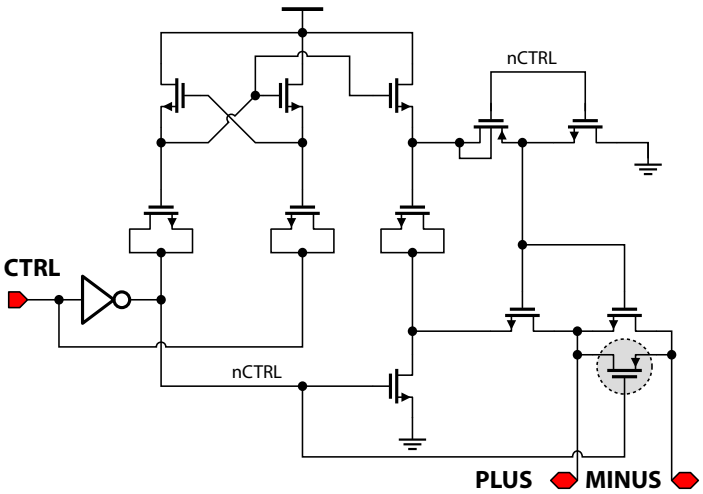

Figure 5.9: Bootstrapped switches used in low-voltage DAC.

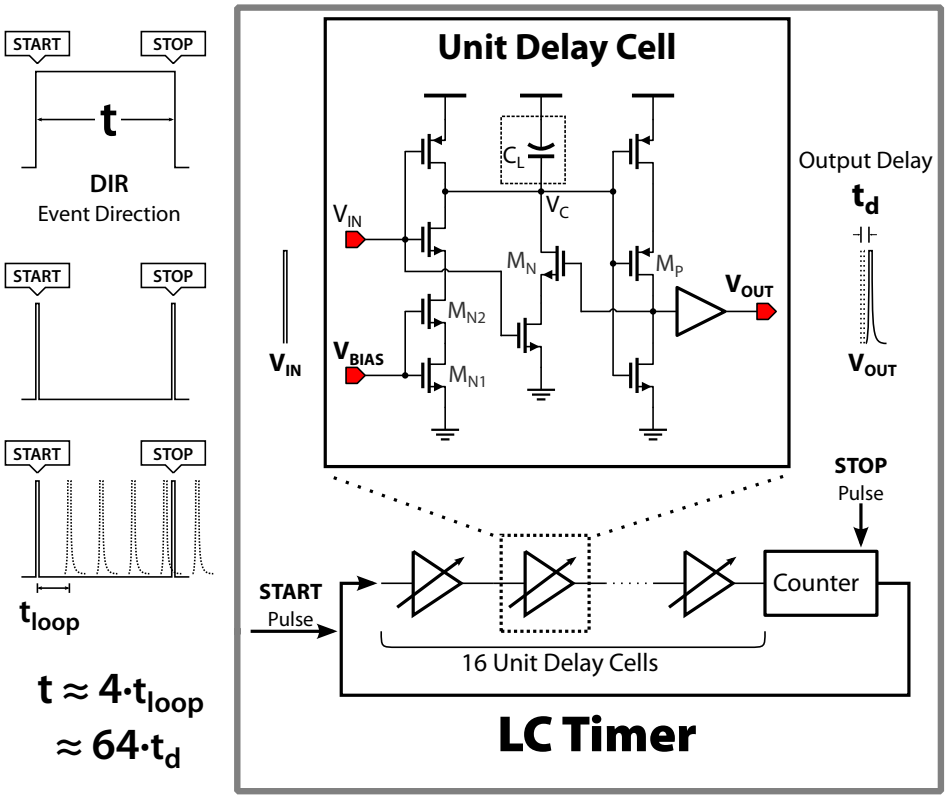

Figure 5.10: LC Timer and delay cell for timing control.

STOP pulses as shown at the left of Fig. 5.10. The START pulse then propagates through the chain of 16 delay cells to the counter. The delayed pulse increases the counter value by 1 and triggers the counter to generate a new pulse, which is looped back to the input of delay chain. This process continues, until the STOP pulse arrives and the counter stops counting. The LC timer outputs the counter value and resets the counter, waiting for next START pulse. As each delay cell provides a delay of t_d, the counter value N can be converted into the duration of DIR signal, i.e. $t = N \cdot 16t_d$.

The delay cell is based on a current-starved digital buffer [169, 170]. When V_{IN} is low, C_L is charged and V_{OUT} is turned low. When V_{IN} turns high, C_L gets discharged slowly through M_{N2} and M_{N1}, until the voltage at V_C falls to a threshold value V_{TH} and turns M_P moderately on. The positive feedback [171], formed by

M_N and M_P, accelerates the remaining discharging process. The acceleration helps to reduce short current. Two small transistors M_{N2} and M_{N1} are used to limit the discharging current, which increase the delay time to several milliseconds. This delay time is adjustable by changing the V_{BIAS} voltage.

The matched delay block in the ADC uses the same delay cell to avoid race conditions. When a new event is generated, the matched delay block locks this event for t_{lock} time, until the DAC updates V_{UPPER} and V_{LOWER}, and comparators are ready to respond to the new references. Together with the event generator, the matched delay block establishes a simple hazard-free 4-phase asynchronous handshaking protocol. In our design, a delay chain consisting of 8 delay cells are used to generate tunable delay t_{lock}.

5.4.4 Digital Control Unit and QRS Detector

The digital control unit for the ADC and the PUT detector are synthesized using customized 0.3 V digital cell library. An external counter is required to set the T_THRES value in the t-PUT QRS detector, as the existing device models for simulation are not accurately characterized under 0.3 V. Also LC timer should be calibrated using accurate external time reference. Everything else in Fig. 5.1 are fully implemented in the chip.

5.5 Measurement Results and Discussions

This ADC-QRS chip is fabricated in a 0.13 μm standard CMOS process. It includes the event-driven ADC, the complete PUT-QRS detector, and the LC timer for t-PUT detection. The total core area is 420×850 μm^2. The die photo is shown in Fig. 5.11.

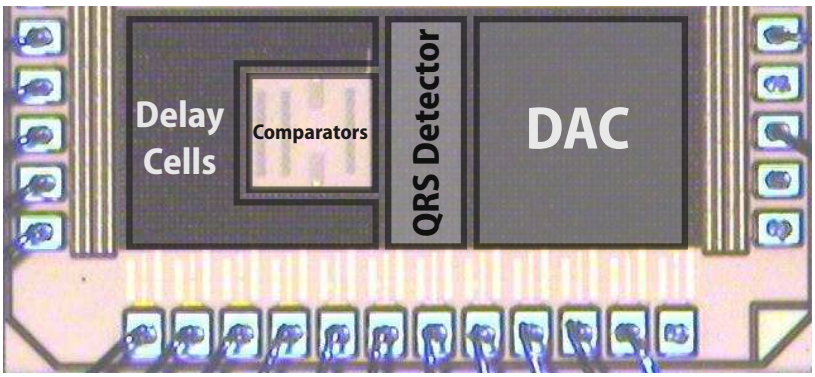

Figure 5.11: Micro-photograph of the fabricated event-driven system chip.

The event-driven ADC is first tested using 0.3 V full-swing 50-Hz sinusoidal input. The delta-modulated outputs REQ and DIR are first captured to reconstruct the input, and the recontructed input is resampled at a higher frequency of 25 kHz before power spectrum analysis through Fast Fourier Transform (FFT). Based on the FFT result, the SNDR is 28.3 dB. We also measured the maximum input frequency without slope overload [172] at 1.2 kHz. At higher frequencies the ADC loop delay is too large to track the level-crossing events.

The functions of the overall system are verified with the help of a Fluke ECG simulator. The Lead II output of the simulator is first amplified through an SR560 low-noise voltage preamplifier to around 0.3 V_{PP}, and then connected to the ADC's input. Fig. 5.12 shows the measured PUT-QRS detection results, delta-modulated outputs and the reconstructed signal. As designed, the QRS output is only activated during the R-S interval. Under 0.3 V supply, the total power consumption of the system is 220 nW using the ECG input. The system also fully functions under higher supply voltage up to 0.6 V.

To test the t-PUT QRS detector, the delay chain used in the LC timer needs to be characterized. By changing the bias voltage V_{BIAS} of the delay cells from 300 mV to 0 mV, the delay t_{loop} is tuned from 14.1 µs to 976 µs. In order to measure the QRS duration of about 0.1 s, an external 8-bit counter is required for the LC

timer, assuming using the maximum delay by setting V_{BIAS}=0.

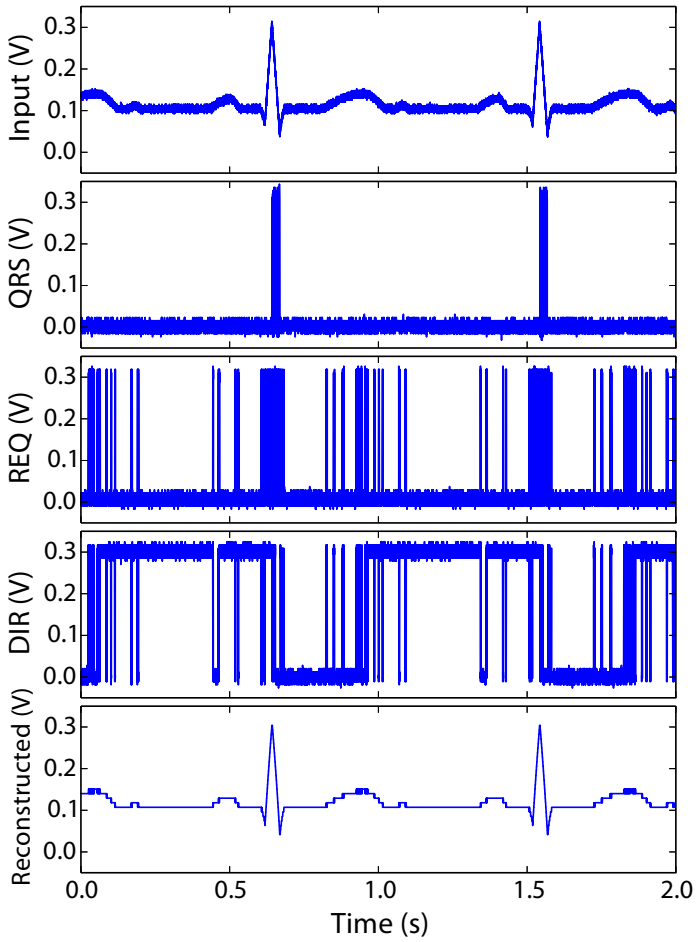

Figure 5.12: Chip testing results using ECG simulator input.

Fig. 5.13 gives the power consumption and area breakdowns through post-layout simulations. The analog blocks, including the two comparators and the DAC, consume over 84% of the total power, while the QRS detector consumes less than 9.5%. Therefore, the total power consumption changes little with the input frequency, which is also verified in our measurements. To our best knowledge, it has the lowest power consumption among all reported QRS detectors. In terms of area, the resistor array in the DAC takes up over half of the total chip area, followed by the delay cells.

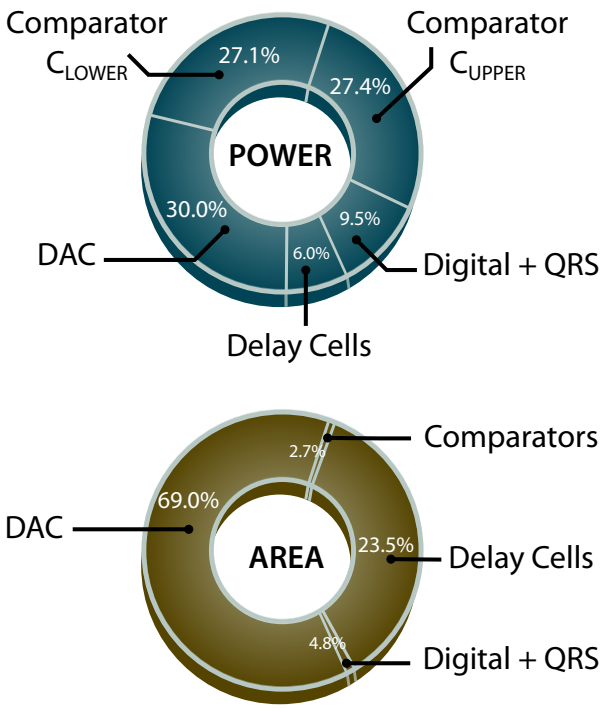

Figure 5.13: Power and area breakdowns for the whole system.

5.5.1 Performance Evaluation

Table 5.3: Comparison of Low-Power Event-Driven ADCs

	[169]	[127]	[173]	[174]	[129]	This Work
Process (μm)	0.09	0.18	0.13	0.5	0.18	0.13
Supply (V)	1	0.7	0.8	3.3	0.8	0.3
SNDR (dB)	47	43.2	47	31	49	28.3[b]
ENOB (bits)	7.5	6.9	7.5	4.8	7.9	4.4
Max Freq. (kHz)	20	4	20	5	5	1
Power (μW)	50	25[a]	3	8.25	0.313	0.22[b]
Area (mm^2)	0.06	0.96[a]	0.36	0.06	0.045	0.36[b]

[a] Analog part only.
[b] ADC and QRS; measured at 50 Hz input.

Table 5.3 and Table 5.4 compare this work with recently published event-driven ADCs and low-power QRS detectors. Our ADC has the lowest supply voltage and power. The proposed QRS detectors achieve similar performance for

most MIT-BIH database records compared to [143]. There are only 4 records, i.e. 200, 203, 217, and 233, where [143] demonstrates better sensitivity and positive prediction. Note that the comparison excluded Record 207 because [143] does not count episodes of ventricular flutter in the record. The overall better performance of [143] was achieved at the cost of larger area and an order of magnitude higher power.

Table 5.4: Comparison of Low-Power QRS Detectors

	[143]	[154]	[158]	[175]	t-PUT
Process	0.35 µm	45 nm	0.35 µm	0.18 µm	0.13 µm
Supply(V)	1.8	0.34	3.3	–	0.3
Se(%)	99.31[a]	~96[b]	99.81[c]	95.65	97.76[c]
+P(%)	99.70[a]	~95[b]	99.80[c]	99.36	98.59[c]
Power(µW)	0.83	0.33	2.7	2.21	0.034
Area(mm^2)	1.1	0.49	–	0.68	0.10

[a] Excludes counts for ventricular flutter in Record 207.
[b] Estimated from Fig. 5 in [154]
[c] Simulation results only.

5.5.2 Discussions

This chapter demonstrates a low-voltage low-power event-driven ECG processor chip for QRS detection. The measurement results verify the functionality of the chip and demonstrate the good energy efficiency of A2I based system. However, our measurement also reveals that event-driven based QRS detector is prone to noise, especially power-line noise and large changes in signal amplitude over time. The monotonic {RISE} events during QR waves may get interrupted, which induces false negative detection errors. The changing amplitude of ECG signal also reduces the QRS detection accuracy as the threshold A_THRES is fixed. Similar to [160], QRS detection accuracy is sensitive to the signal amplitude and threshold A_THRES settings. If the ECG peak-to-peak voltage is lower than

$V_{DD}/2$, distinguishing QRS peaks from other P/T peaks becomes challenging, given the fixed 5-bit quantization level. There are several ways to minimize the effect of the noise and improve the detection accuracy. A low-noise front-end amplifier with band-pass filtering could improve the ECG signal quality and suppress the power-line noise. Real-time impedance measurement combining with motion artifacts cancellation [176] could also be an option, especially for wearable applications. Another way is to use adaptive threshold as mentioned in Section 5.3. Search-back [150] could be another effective way to improve the accuracy at the cost of complexity.

5.6 Conclusion

Chapter 5 presents the design of a low-voltage low-power A2I QRS detection chip. The very low speed requirements of the event-driven circuit allow the use of a low supply voltage in order to reduce power. The low power and good accuracy are achieved through the proposed pulse-triggered and time-assisted pulse-triggered QRS algorithms that directly utilize the information embedded in level-crossing events to identify QRS complex. The algorithms are verified through simulations using signals from MIT-BIH ECG Arrhythmia Database. Implemented in 0.13 μm CMOS technology, the A2I-QRS chip consumes 220 nW under 300 mV supply voltage for typical ECG input, which demonstrates the potential of using A2I system in ultra-low-power designs for wearable biomedical applications.

CHAPTER 6

A 2.89-μW Event-Driven Wireless Dry-Electrode ECG Sensor

6.1 Introduction

The wearable ECG sensor tracks the electrical activities of the heart through capturing the ECG signals in a noninvasive manner. The ECG signal is then transferred to the cardiologists for interpretation. Combined with telemedicine infrastructure and the cloud service, the patient can benefit from preventional health care and early diagnosis on heart conditions, without frequent hospital visits for ECG monitoring. In case of heart attack, the patient will be provided with immediate action through the wireless communication within the golden hour, and the chance of survival or near-complete recovery is significantly higher.

The main design targets for wearable ECG devices include high signal quality, compact size, long battery life, comfortable and easy to use, and also low cost. Designing such an ECG sensor system however, remains challenging. First of all, the ECG signal, which is normally a few millivolts in amplitude, could be easily overwhelmed by noise or artifacts. So low noise amplifiers are critical for the

signal quality. Second, the wearable device is often powered by a rechargeable battery, and its size is mainly restricted by the battery mounted. In order to reduce the sensor size while increasing the battery life for long-term continuous recording, the power consumption for the entire system should be extremely low. Third, while wet Ag/Cl electrodes are used widely for the ECG sensing, it is never a comfortable choice for long-term monitoring. Wearing wet electrodes for long time will cause skin irritation, and the signal quality deteriorates after the gel is dried. Dry electrode candidates like metal or fabric electrodes could be a better solution. The ECG sensor should not cause skin irritation after long-time wear. Last but not least, the total cost for such a device should be reasonably low and affordable for massive use. As for the circuit, higher-level integration with minimal use of external components is advantageous.

Wearable ECG sensor design has attracted much research effort in the past years. For the front-end part, a few low-power designs like [31, 77] are promising for wet electrode applications, and have shown decent performance with low power consumption. But as the input impedance is low for AC-coupled or chopper stabilization amplifier, those designs are not compatible with dry electrodes. Approaches like [66] improve the input impedance as well as the noise performance, but the power consumption is higher. The design in [72] uses DC-coupled amplifier, but the feedback loop is implemented off the chip. None of those designs mentioned above includes wireless communication part. As shown in [98], the wireless communication could be the most power consuming part of the whole sensor system, which is the greatest obstacle for long-term low-power operation. On the other hand, [177, 83] demonstrate full wireless sensor nodes including radio frequency (RF) transmitters. When sending the heart beat data only, the power is less than 20 μW by heavy duty cycling. But the power consumption under the raw data transmission mode is still high considering the power budget

for long-term continuous operation.

A brand new type of wireless ECG sensor is proposed in this chapter. It combines event-driven LC analog-to-information converter [178], impulse-radio (IR) ultra-wideband (UWB) transmitter (TX) and on-chip antenna with high-impedance ECG AFE amplifier. The DC-coupled AFE significantly improves the input impedance and signal quality, without any active impedance boosting feedback loops [68]. The event-driven analog-to-information system includes a LC ADC with built-in QRS detection for heart rate monitoring. The delta-modulated output is fed to a 3-5 GHz IR-UWB TX with an on-chip antenna. Implemented in 0.13 μm CMOS technology, the total power consumption for raw ECG signal transmission is 2.89 μW, which is over 6 times better compared to the state-of-the-art designs [177, 83]. Also the sensor system does not require any external components, e.g. clock, filters and off-chip antenna, making it a perfect candidate for low-cost disposable wireless ECG sensor.

The paper is organized as follows. Section 6.2 starts with the architecture of the SoC, and briefly introduces the event-driven platform with QRS detection. The circuit implementation details for each block are revealed in Section 6.3. Chip measurement results are discussed in Section 6.4. ECG is captured from volunteers using different ECG electrodes, and the effects of various artifacts are then evaluated. The final section draws the conclusion remarks.

6.2 System Architecture

The architecture of the proposed ECG sensor system is shown in Fig. 6.1. The sensor first captures the single-channel ECG from skin surface through the low-noise AFE. The signal is then digitized through a level-crossing ADC with 32 quantization levels, and sent through the UWB transmitter. Alternatively if the

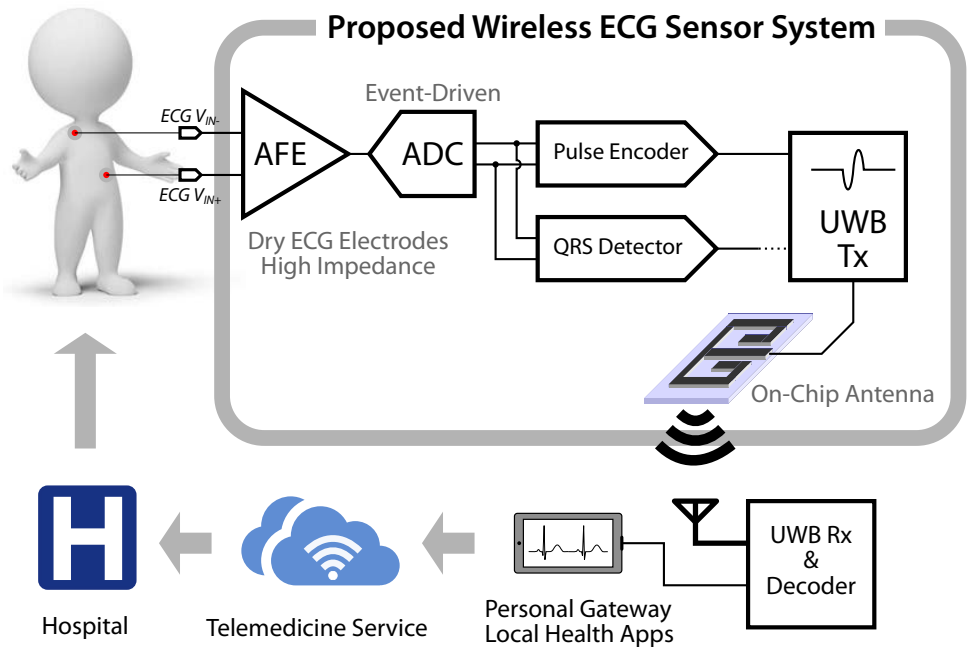

Figure 6.1: The wireless ECG sensor with telemedicine applications.

heart rate information is required, the event-driven QRS detector will generate pulses representing the heart beats, and the pulses are then transmitted to the receiver. The communication at the transmitter side uses an on-chip antenna to minimize the use of off-chip components. The receiver is a bridging device, which tunnels the ECG data to the gateway such as the personal smartphone. Next, the data is uploaded to the cloud database through Wi-Fi or cellular network. At the final stage, the ECG signal is analyzed by cardiologist for personalized diagnosis and health care services. Our design mainly focus on the sensor part before the UWB receiver, which is the most critical part in the system and also often limited by the available power budget. The UWB receiver and the decoder are not attached to human body, thus allows less stringent requirement on power and size.

Being directly connected to the body, the analog front-end's performance is crucial to the signal acquisition quality. First, the noise of the whole sensor

is often limited by the IA at the first stage. Sensors with higher noise may not be capable to capture the clinical ECG for accurate diagnosis, especially when the most critical P wave is lost in the noise floor. Second, the AFE should be able to reject the input offset effectively to avoid amplifier saturation. The typical input offset for Ag/Cl wet electrodes is around 200 mV, much larger than the amplitude of ECG signals. AC-coupled amplifiers [25] and the extra DC servo loop for chopper stabilized amplifiers [59] are the most common solutions for offset suppression. Third, high input impedance will increase the captured signal amplitude, especially when the connection between skin and the electrode is not firm [20]. Also a high input impedance front-end helps mitigate the motion artifacts [45] and powerline interference [118]. Unfortunately, few designs could achieve the impedance requirement without power overhead or compromising the other two factors mentioned. The DC-input AFE in [72] has very high input impedance, but it requires off-chip DAC feedback for offset cancellation. [46] showed TΩ input impedance using an input buffer, but the gain is unity and the power consumption is high. A power-efficient active electrode using one PMOS transistor is analyzed in [179], but it has limited input range and deteriorated common-mode reject ratio due to mismatch. This design introduces a new DC-input front-end architecture suitable for both wet and dry electrode use. The offset is canceled through the RC filter at the complementary feedback of the amplifier. Section 6.3.1 gives detailed analysis for the front-end.

The event-driven ADC digitizes the ECG signal using level-crossing sampling (LCS) scheme [123, 161]. The LCS is highly effective for ECG data compression, as a significant part of the ECG trace is of very small variations, and LC ADC will sample this part infrequently [180]. Shown in the left side of Fig. 6.2, it includes two asynchronous comparators, an event generator, an accumulator, and a DAC. The analog input is tracked by the two comparators C_H and C_L. Whenever the

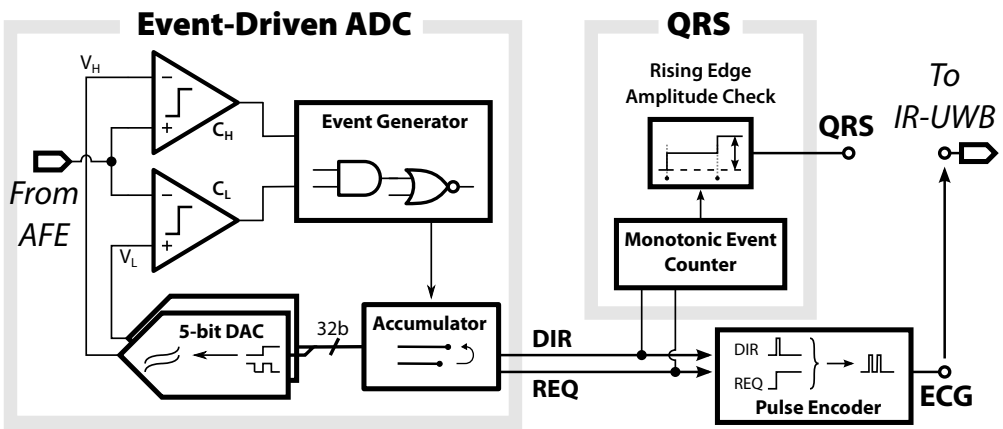

Figure 6.2: Event-driven ADC and the QRS detector.

input voltage level rises or falls by one least-significant-bit voltage defined by the DAC, one comparator's output voltage will be high, and the change is then captured and processed by the event generator. Next the accumulator updates the DAC outputs V_H and V_L, which serve as the threshold value for the two comparators.

The output of the event-driven ADC is delta-modulated into 2 bits, DIR and REQ [121]. An illustration of the ADC outputs is given in Fig. 6.3. DIR represents the signal change direction, and each pulse at REQ output stands for one level-crossing event [181]. The 2-bit outputs completely convey the input signal variation up to the designed resolution. In order to transmit the ECG signals, further modulation is required to avoid synchronization issue between DIR and REQ. A pulse encoder translates the 2-bit output into one pulse stream. As shown in Fig. 6.3, when DIR is at high voltage level, each signal pulse at REQ is encoded into 2 pulses, which are close to each other. When DIR is low, the signal pulse remains in the output. To avoid misinterpreted the 2 pulses generated when DIR is high as 2 separate 'low' pulses, the interval Δt_{enc} between the 2 pulses must be much less than the minimal possible REQ pulse intervals. In this design, the ADC quantization level N is 32. Suppose the maximum frequency f_{max} from the

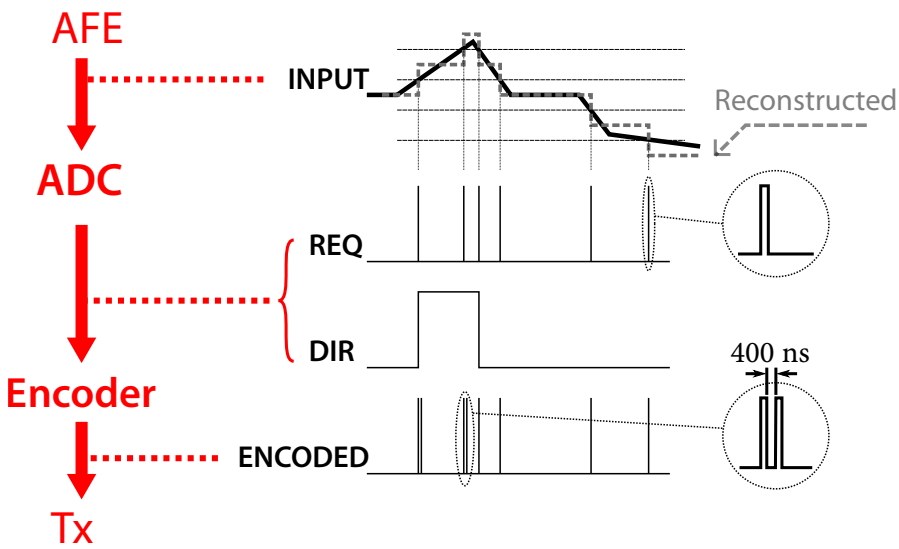

Figure 6.3: Delta modulation and pulse encoder outputs.

ECG front-end is 250 Hz, the worst-case pulse interval Δt_{REQ} for REQ is then given by

$$\Delta t_{REQ} = \frac{1}{2\pi f_{max} \cdot N} = 20\mu s \tag{6.1}$$

By controlling the Δt_{enc} at about 400 ns, much less than Δt_{REQ}, this misinterpretation at the receiver side is unlikely.

A QRS detector utilizing the event-driven level-crossing information is included in the sensor. It provides an operation mode with further minimized data rate, when only heart rate information rather than medical-grade diagnostic ECG data is needed. The detector counts the number of the monotonic rising level-crossing events. If it exceeds a threshold, which means the input voltage level rises high from the baseline, the next turning point is marked as the R peak [181].

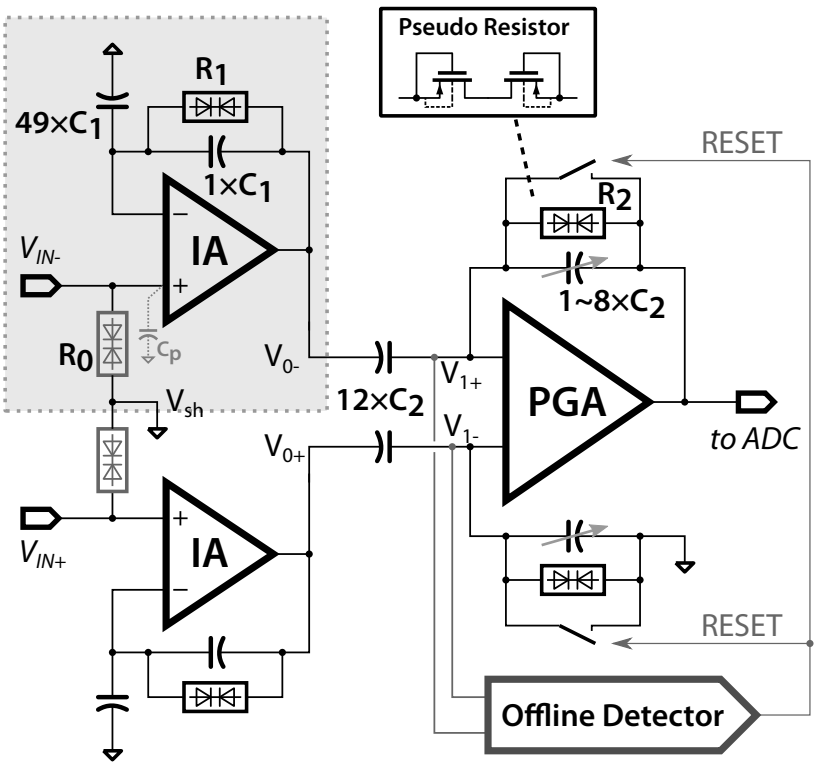

Figure 6.4: DC-coupled ECG front-end.

6.3 Circuit Designs

6.3.1 DC-Input Front-End

Fig. 6.4 shows the AFE circuit diagram for one ECG channel. It consists of two instrumentation amplifiers as impedance boosting buffers, one PGA, and an auxiliary off-line detector. For dry electrode application, high input impedance is critical for good signal quality. In this design, the ECG differential inputs are directly connected to the high input impedance gate terminals of the IAs. The DC-input topology greatly improves the input impedance as well as the ability to sense weak ECG signals from dry electrode, because there are no choppers or large capacitors at the signal input port.

One potential issue of the DC-input front-end is that the input offset is not

removed. To interface with various electrodes and skin conditions, the front-end amplifier is designed to minimize the effects from input DC offsets. Otherwise the amplifier could be easily saturated at early stages, making the accurate ECG capturing impossible. It is possible to design a dedicated feedback loop to cancel the input offset according to the amplifier output [72], but the feedback circuits would increase the system power and chip area, and affect the input noise performance. Moreover, any additional feedback path connected to the input port is likely to deteriorate the input impedance. The proposed design adopted three approaches to minimize the effects of input offsets, without significantly increasing the input impedance.

First, a resistor connects the input port to the circuit input common mode shielding voltage V_{sh}. The resistor, marked as R_0 in the figure, sets and stabilizes the input DC level. To avoid loading the input directly, the resistance of R_0 must be over GΩs. As it is impractical to integrate large resistors directly on chip, the symmetrical pseudo resistor shown in the upper part of Fig. 6.4 is used, modified from the original design in [25]. The pseudo resistor includes 2 diode-connected PMOS transistors, both biased in subthreshold region. A larger R_0 value increases the input resistance directly. However, setting the resistance too high would compromise the input DC settling time, which is determined by the RC time constant from R_0 and parasitic input capacitance C_p. The parasitic capacitance C_p is mainly from the large input-pair transistors of the amplifier, as well as the pseudo resistor R_0 itself. The resistance R_0 is approximately the same as the effective impedance of C_p at 10 Hz main ECG frequency, so that the input impedance is not limited by R_0 alone. Compared to other biasing approaches using resistive divider like in [72], only one diode-connected transistor shows up in the input path and contributes to the input parasitic C_p. Often the shielding voltage is close to system common mode V_{CM}. It is also possible to tune the input

shielding voltage V_{sh} to maximize the offset suppression according to the ECG signal level. For example, when the initial input potential is low, the V_{sh} can be increased until the amplifier's input reaches the designed value close to $V_{DD}/2$.

Second, the IA stage adopts high gain at the ECG frequency, while the gain at DC is significantly lower. Fig. 6.4 marks one of the IA stage in light gray background. Ignoring R_0, the transfer function from ECG input $V_{IN-/IN+}$ to the IA output $V_{0-/0+}$ is given by

$$\frac{V_0}{V_{IN}} = \frac{j\omega \cdot 50R_1C_1 + 1}{j\omega \cdot R_1C_1 + 1} \tag{6.2}$$

At DC, the amplifier gain equals to one by setting $\omega = 0$. For higher frequencies when $\omega R_1C_1 \gg 1$, the gain is close to 50. To reduce the input-referred noise for the IA buffer amplifier, a higher gain of 50 is set for the IA stage. Designing a low-gain low-noise amplifier requires more currents for the IA stage [46]. By attenuating the input signal at DC, the offset amplitude is reduced compared to the ECG signal. Note that the ωR_1C_1 shall be much larger than one even at 0.5 Hz, so that the S-T segment with low frequency is not attenuated causing false diagnosis [13]. Increasing C_1 has negative affects on the chip area. Therefore thick-oxide transistors for pseudo resistor implementation of R_1 is used, which provides over 100 times higher resistance compared to using normal threshold transistors [83].

Third, the remaining DC offset after the IA stage output is completely blocked by the PGA stage. The gain difference of 50, or 34 dB attenuation from IA alone, is inadequate to reject the input offsets while amplifying the ECG to its full scale. Therefore the following stage needs to further increase the dynamic range. The PGA stage uses capacitive-coupling architecture with 4 possible gain settings selected through external control bits. The gain is tuned by changing the C_2 capacitor ratio, varying from the highest 12:1 to the lowest 12:8. Like R_1, the

pseudo resistor at the PGA stage also adopts thick-oxide PMOS to reduce the high-pass cutoff frequency.

Similar to AC-coupled IAs, the common-mode rejection ability of the proposed design relies on the capacitor ratio matching between the positive and negative input branch. Putting the two IA parts close to each other in the layout would benefit the CMRR and improve the readout signal quality. The mismatch between pseudo resistors affects the low-frequency CMRR below the high-pass corner, which is less severe for the ECG application.

6.3.2 Offline Detector

In most cases the input offset is fully removed at the PGA output. For unexpected use cases such as lead off or electrode reattaching, the ECG baseline may temporarily drift away from the common mode to a larger extend, resulting in clipped ECG waveforms. In such a circumstance, a reset to the front-end amplifiers is necessary, by shorting the pseudo resistors R_2 and pulling the PGA output to common mode V_{CM} forcedly. The reset avoids long waiting time for the front-end, especially because the high-pass cutoff frequency is lower than 0.1 Hz.

This design includes an offline detector for the ECG signal. The schematic of the offline detector is in Fig. 6.5. The detector monitors whether the ECG output is clipped at the PGA output. The monitoring is implemented by tracking the gate voltage (V_{1+} and V_{1-}) of the PGA input pair. Under normal conditions, the amplifier inputs V_{1+} and V_{1-} are close to the common mode V_{CM} because of the close loop feedback. Whenever the PGA output is saturated, the amplifier inputs V_{1+} and V_{1-} are drifting away from V_{CM}. Based on this mechanism, the offline detector will automatically issue a reset command to the PGA once the V_{1+} and V_{1-} voltages are notably higher or lower than V_{CM}.

The offline detector includes two unbalanced comparators, in which the

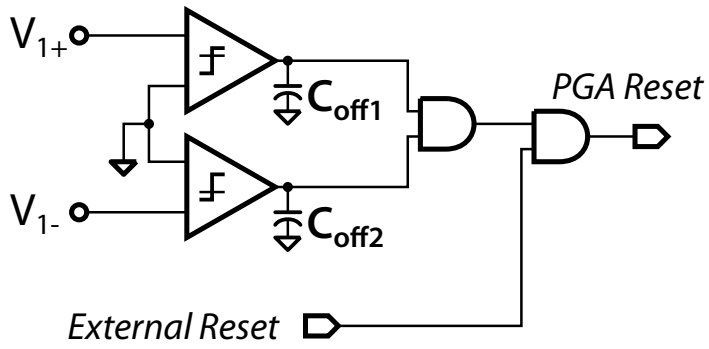

Figure 6.5: Offline detector for the PGA stage.

two transistors in the input pair are of different sizes. Therefore, only when the input is much higher than V_{CM}, the comparator output will turn high. This avoids generating an extra reference, which does not need to be accurate nevertheless. To avoid repetitive resetting, two large capacitors C_{off1} and C_{off2} are at the comparator outputs. The charging and discharging time is then increased, waiting for the amplifier to be settled after resetting.

6.3.3 Comparators in ADC

Fig. 6.6 shows the comparator used in the event-driven ADC. Since the ADC samples based on level-crossing events instead of periodical clock, asynchronous comparators are necessary for input level monitoring. The first stage of the ADC, marked in gray background, is a self-biased differential amplifier [166]. It accepts rail-to-rail input and improves the signal dynamic range. This differential input stage is also insensitive to the voltage supply variations [181]. The second stage uses an inverter to generate full-scale output and further improve the open-loop gain.

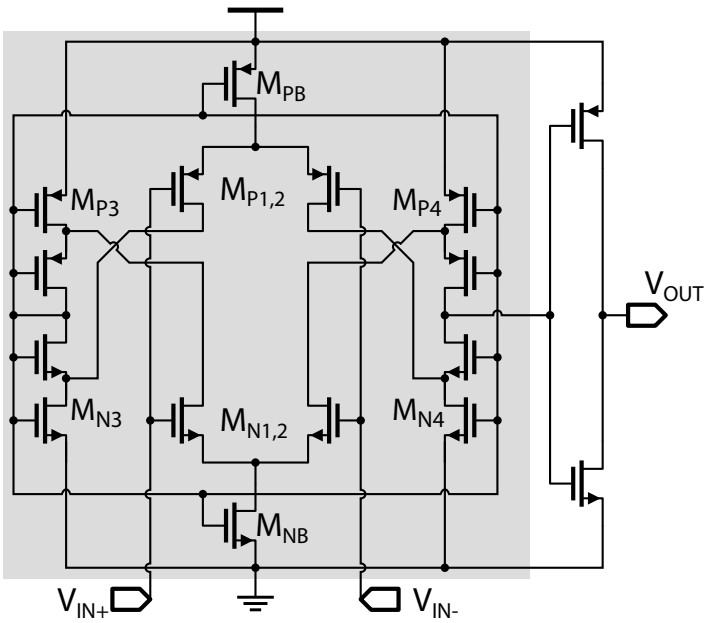

Figure 6.6: The asynchronous comparator in the ADC.

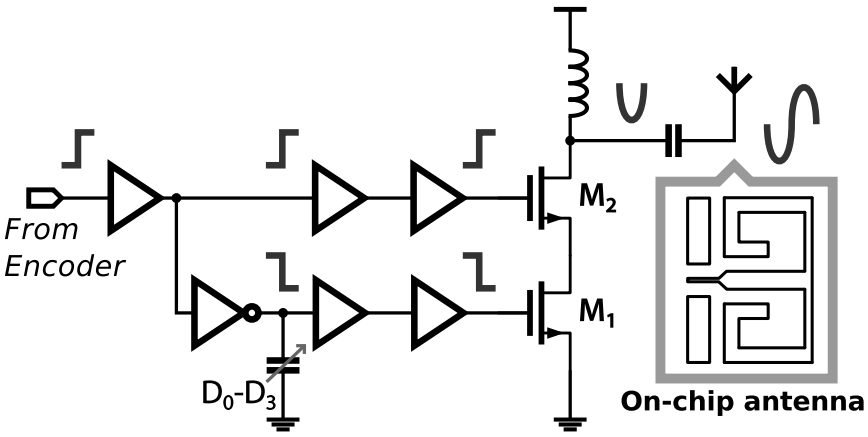

Figure 6.7: The schematic of the UWB transmitter.

6.3.4 UWB Transmitter and Antenna

The IR-UWB TX and the 2 mm × 2.5 mm on-chip coplanar waveguide-fed monopole antenna are implemented to transmit the encoded data. The schematic is shown in Fig. 6.7.

The digital edge-combining technique is used to generate the mono-cycle pulse while the cascade amplifier with optimized on-chip inductor is used to drive

Table 6.1: Performance Comparison of ECG Wireless SoC

	This work	[74]	[83]
Technology	130 nm	130 nm	130 nm
Supply	1.2 V	0.3-1.2 V	0.25-0.7 V
FE Current	1.19 μA	4 μA	1.4 μA
Input Impedance	3.6 GΩ	<10 MΩ	<10 MΩ
Input Noise	3.06 μV	2 μV	6.9 μV
FE Gain	38-55 dB	40-78 dB	36-44 dB
FE Bandwidth	0.5-180 Hz	0-320 Hz	0.05-150 Hz
CMRR	64.9 dB	>70 dB	59 dB
PSRR	61.5 dB	-	70 dB
FE SNR	42.2 dB	-	45.6 dB
TX Band	3-5 GHz UWB	MICS/ISM	MICS
TX Power	1.46 μW @100 kbps	160 μW @200 kbps	600 μW @150 kbps
Energy/bit	14.6 pJ/b	0.8 nJ/b	4 nJ/b
Total Power	2.89 μW (HR & raw)	19 μW (HR) 397 μW (raw)	17.4 μW (HR) 74.8 μW (raw)

the on-chip antenna. The pulse width is controlled digitally (D_0-D_3) by varying the load capacitance of the inverter. The transmitter is activated only if encoded data pulses are received from the ADC. The heavy duty-cycling of the transmitter significantly reduces the power consumption.

6.4 Measurement Results

6.4.1 Chip Performance

The chip was fabricated in a standard 0.13 μm CMOS technology. The entire sensor operates under 1.2 V supply voltage, while the amplifier and the ADC can work under 0.8 V supply. The die photomicrograph is shown in Fig. 6.8, with most area occupied by the on-chip antenna.

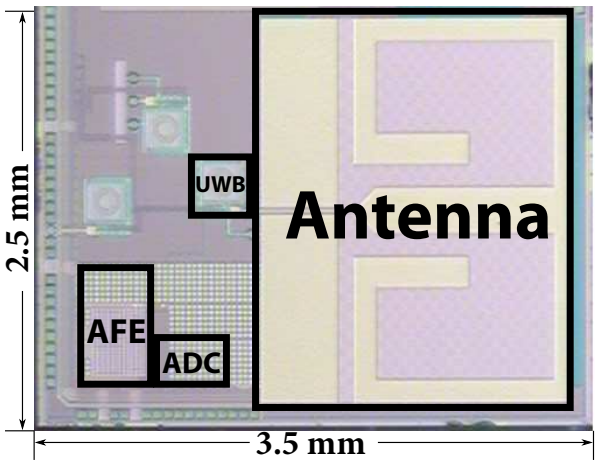

Figure 6.8: Micro-photograph of the fabricated chip.

The performance results are summarized in Table 6.1. The total power consumption is 2.89 μW for full-rate raw ECG transmission, which is over one magnitude lower than the current state-of-the-art designs.

The noise performance of the analog front-end amplifier is shown in Fig. 6.9. The front-end input-referred noise is 3.06 μV_{rms}, integrated from 0.5 Hz to 150 Hz. The input impedance is over 3.6 GΩ. With a 10-Hz sinusoid testing signal input, the spectrum of the signal reconstructed from ADC output DIR and REQ is shown in Fig. 6.10. The front-end and the ADC achieve 42.2 dB signal-to-noise ratio (SNR).

The measured transmitter's output voltage swing is 600 mV with a 50Ω load and achieves the FCC compliance at the data rate of 100 kbps (Fig. 5). The total power consumption of the UWB transmitter is 1.46 μW. The de-embedded measurement of the on-chip antenna shows that it achieves -10 dB return loss from 2 to 7 GHz (Fig. 6(a)). The simulated radiation pattern indicates an omnidirectional pattern with a peak realized gain of -37.3 dBi at 4 GHz (Fig. 6(b)). A custom-designed UWB receiver with a PCB antenna is used to receive and demodulate the UWB signal transmitted from this ECG sensor. The recovered ECG signal is shown in Fig. 6.11.

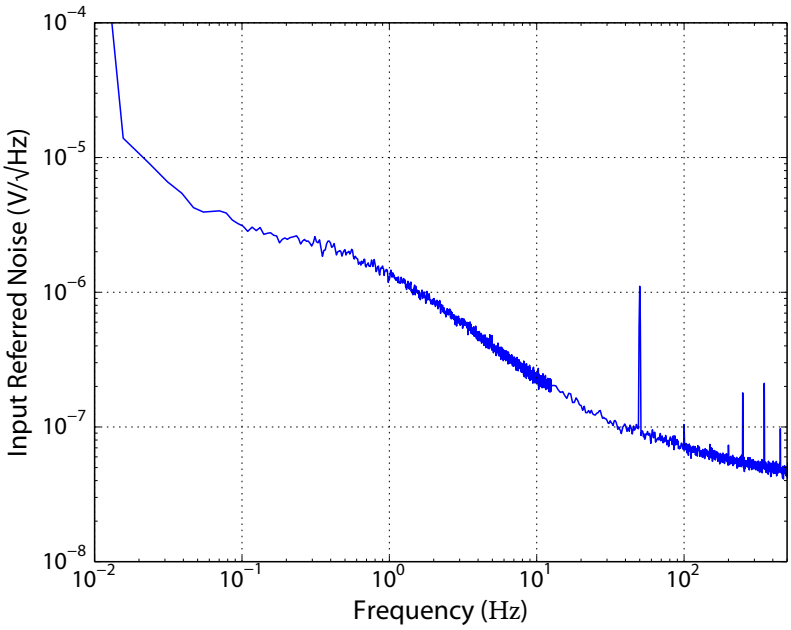

Figure 6.9: Input-referred noise of the analog front-end.

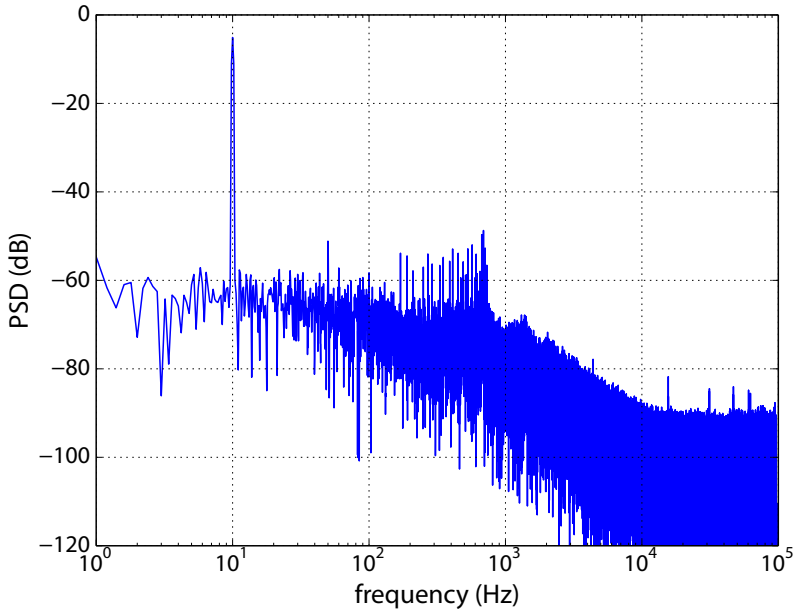

Figure 6.10: Output spectrum of the front-end and ADC.

6.4.2 ECG Measurement

Fig. 6.4.2 gives the dry electrodes used in the human test. The electrode is from the low-cost 2-layer PCB, with the bottom metal layer open for ECG sensing.

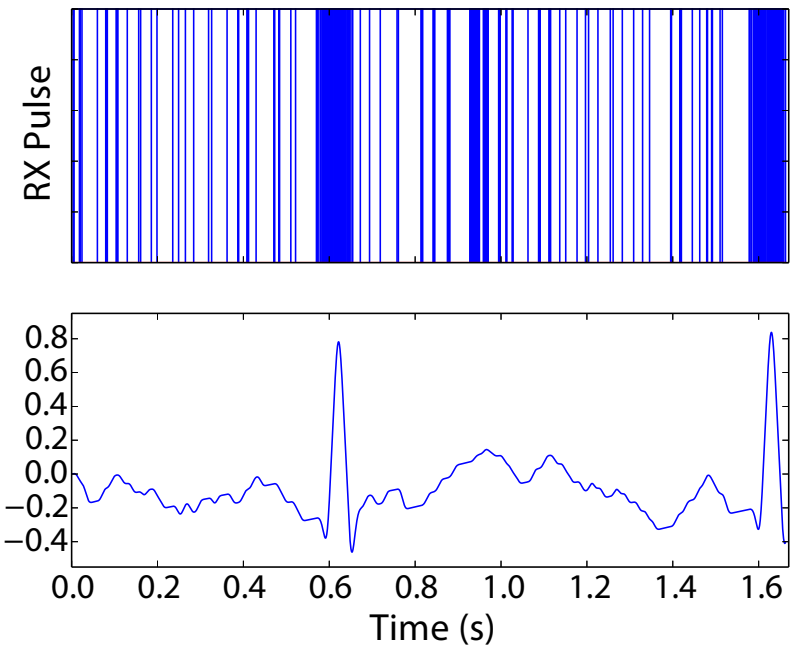

Figure 6.11: ECG signal reconstructed from wireless transmission.

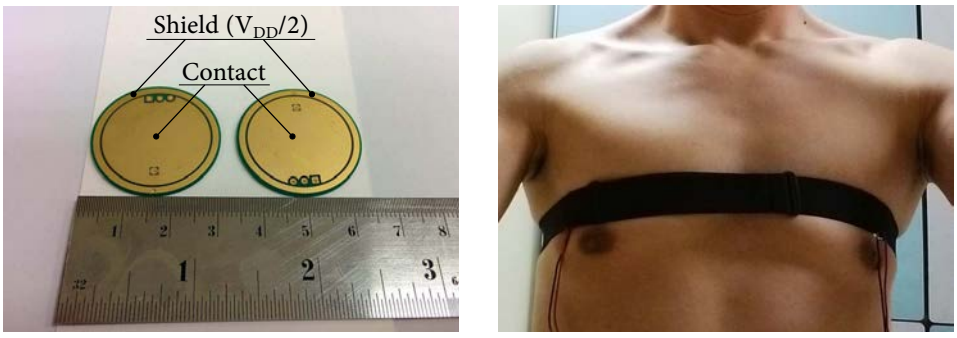

Figure 6.12: (a) Dry electrodes used; (b) chest lead position using dry electrodes.

Around the inner contact, an outside ring is used as the shield electrode. The outer periphery of the electrode sets the skin potential close to the circuit common-mode, which effectively reduces the skin-electrode offset and accelerate the ECG baseline settling. 2 such electrodes are put on the chest side, as shown in Fig. 6.4.2. The chest ECG is captured and reconstructed using the ADC's output first, shown in Fig. 6.4.2.

Fig. 6.14 shows the 20-s ECG captured using the high-impedance front-end during moderate body movement and activities. The test subject walks in normal

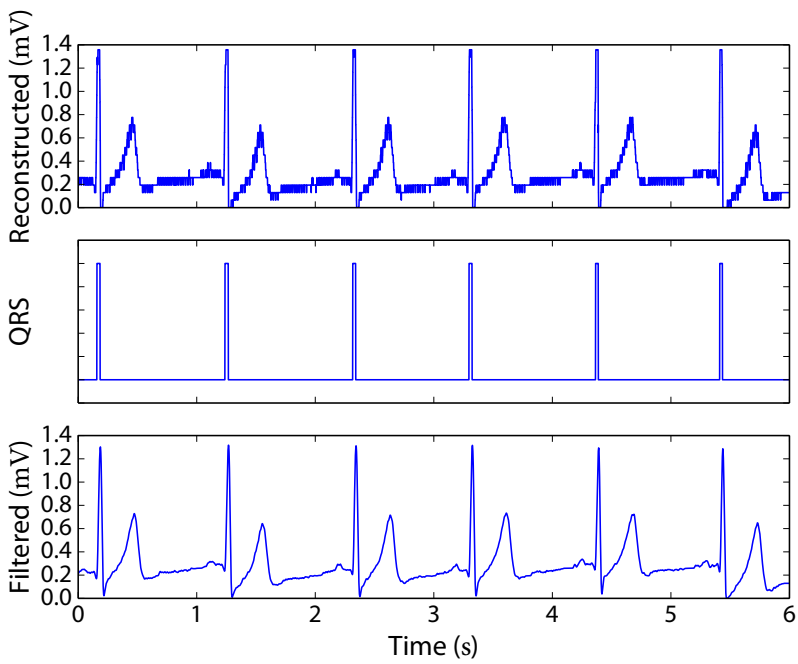

Figure 6.13: ECG input reconstruction and QRS detection result, using dry electrodes.

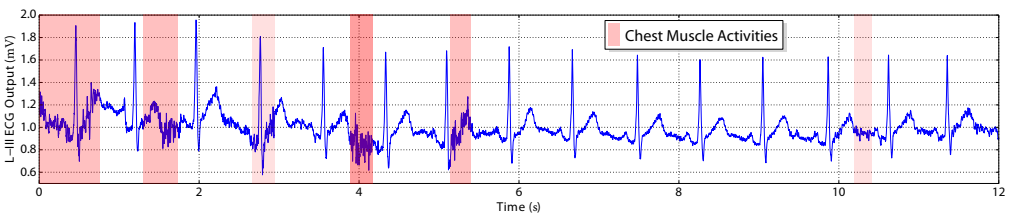

Figure 6.14: ECG captured during subject walking and stretching chest muscles.

pace and occasionally stretches the muscle. The results show that moderate body movement does not affect the ECG baseline at all. Further, the muscle response will only evoke the EMG signal, as marked in dark background in the plot. No significant ECG baseline drift is caused by the muscle activity, thanks to the high input impedance from DC-input AFE.

6.5 Conclusions

The chapter discusses the design of an event-driven ECG sensor chip with impulse-radio ultra-wideband transmitter and on-chip antenna. The DC-coupled front-end architecture improves the signal quality under dry electrode sensing, with the input impedance of up to 3.6 GΩ. The captured ECG trace is less affected by motion artifacts. A power-efficient QRS detector based on level-crossing output further reduces the data rate with minimal power and area overhead. A low-power ultra-wideband transmitter sends the modulated event-driven pulse through an on-chip antenna. Implemented in 0.13 μm CMOS technology, the system consumes 2.89 μW under 1.2 V supply while transmitting the raw ECG data, which is one magnitude lower than the current state-of-the-art design. The highly integrated ECG sensor system does not require any external clocks, wet electrodes, or large antennas, which makes it a good candidate for disposable wireless ECG sensor applications.

CHAPTER 7

Conclusions and Future Works

7.1 Design Reviews

The thesis covers design techniques for biomedical sensor systems including analog front-ends and event-driven ADC/signal processors. Among the total six designs introduced, four chips adopt the capacitive-coupling amplifier architecture. The capacitive-coupling front-end has several benefits, such as low bandwidth requirement and low power consumption, full-range electrode offsets cancellation, and relatively higher input impedance. Another design discussed in the last chapter chooses a new DC-input front-end without feedback offset control. This DC-input sensor has higher impedance and better artifacts suppression according to the measurements results. Also the chip areas is much reduced after avoiding the large input capacitors, which is especially welcomed under advanced technology nodes.

The first key charateristic for biomedical circuits is the low frequency of the input signal. While the ECG input DC offsets are normally blocked to maximize the dynamic range, for precise disgnosis the signal around 0.5 Hz cannot be attenuated. This calls for a high-pass filter cut at around 0.05 Hz and with very

large RC constant. Pseudo resistors, or any active designs with controlled current, are naturally the best candidates for on-chip large resistance implementation. But the resistance values and linearities vary remarkably for different implementations. After evaluating up to 32 pseudo resistor designs in the relevant chapter, the designers would have a basic understanding for the pseudo resistor characteristics, as well as the guidelines for choosing pseudo resistors in different amplifier stages.

The second effort is mainly on improving the signal quality. While using adhesive Ag/AgCl electrodes with capacitive-coupling front-end would generally guarantee a decent ECG trace captured, it is not the case if using metal electrodes or other dry electrodes, due to the higher impedance required. Aiming at this issue, a new DC-coupled front-end architecture is proposed. The DC-blocking task is deferred to later stages, while the input buffers use a smaller gain to avoid offset-induced saturation. Again, pseudo resistors are used to ensure the input potential eventually settled to the circuit common mode. As there are no large capacitors at the lead input, the input impedance could be much higher. Measurement results also prove the DC-coupled design is less vulnerable to the motion artifacts.

Meanwhile, a new impedance boosting method is also discussed for AC-coupled front-end. A weak positive current feedback path is added, which is able provide some of the current needed to drive the large input capacitors, and hence minimizes the input current from the electrodes.

A few other design techniques are also highlighted for the ECG and impedance measurement channels. The sub-0.1-Hz high-pass corner also causes slow baseline settling, and often a reset is required to make sure the ECG baseline return to the common mode instantaneously. To avoid the troublesome of manual resets, an offset detector is used to monitor the ECG signal DC, and sends reset command whenever necessary. Also the input voltages of the amplifiers are locked within the common mode range using diodes in order to minimize the chance of input DC

drifts. On the impedance measurement part, the early demodulation architecture for impedance measurement drastically reduces the bandwidth requirement for the amplifier from over 100 kHz to less than 10 Hz, and saves the amplifier power.

The second part of the thesis discusses the possibility to reduce system power more significantly. The main direction for optimization is on reducing the data rate, because lower data rate can shrink the wireless transmission power greatly. Note that several designs in the first part already includes on-chip lossless ECG signal digital compressors based on slope prediction, which normally can reduce the data rate to its 1/2 to 1/3. The two designs in the second part feature data compression directly at the sampling stage, and are more energy efficient.

The first idea is to perform signal processing tasks directly within the ADC block during sampling and quantization. A clean ECG signal is often of low activity and sporadic, and it can be applied in event-driven level-crossing sampling scheme, where the sampling occurs only when the signal voltage changes. Level-crossing sampling generates fewer samples without resolution degradation, and based on the level-crossing ADC, various time-based signal processing tasks can be performed, like ECG QRS peak detection. The event-driven QRS detector consumes nanoWatt power but still achieves high detection accuracy, which is a great candidate for self-power ECG sensor processors.

In the final design a complete low-power pulse-based asynchronous wireless ECG sensor is proposed, based on the level-crossing sampling and event-driven QRS detector. The signal processing tasks are performed directly at the level-crossing ADC side, and therefore no extra micro-controllers are used. The pulse-based UWB transceiver is well compatible with the event-driven system and delta modulation, which only sends the pulses at the time when the input ECG changes one least significant bit in voltage. At very low data rate, the total power

consumption for the UWB is minimized significantly. Combining with the DC-coupled front-end, the event-driven wireless sensor consumes very limited power even for raw ECG data transmission, and it is also the dry electrode ECG wireless sensor with the lowest raw data power consumption by far.

7.2 Ongoing and Future Works

The main research in the past five years has been focused on integrated circuit design for the analog front-end amplifiers and event-driven biomedical systems. And based on the progress and design experience, several new designs have been scheduled in the two areas. The main directions for further improvements of the sensor amplifiers include

- With the new high CMRR design with boosted input impedance introduced in Chapter 4, the driven-right-leg output is not required to connect to the RL electrode to suppress the 50-/60-Hz mains interference. The next step is to mitigate the effects more aggressively, either by using dynamic element matching for the input capacitors of the instrumental amplifier, or through dedicated 50-/60-Hz active feedback filters to cancel the interference. The benefits include reduced power consumption by removing the DRL, reduced electrodes, and better signal quality.

- Chapter 4 also briefly discussed the possibilities of using thoracic impedance to monitor the cardiac input and hence the blood pressure. To improve the accuracy, the impedance measurement channels ought to be less noisy and of higher resolution. Careful trade-offs between the power and performance should be investigated in the impedance measurement amplifier designs.

- The DC-input instrumental amplifier architecture proposed in Chapter 6

is promising due to its low power, small area, and superior signal quality for dry electrodes. Further research on the DC-input system would help extend the tolerable input voltage range, and evaluate the compatibilities with different dry electrode materials.

Meanwhile, extra efforts are made to improve the efficiency of the event-driven system, including

- The QRS detection algorithm based on level-crossing sampling in Chapter 5 could be further improved for its sensitivity and positive prediction. For example, using ECG derivative output helps distinguish the QRS peaks more accurately from noises or artifacts

- Non-uniform sampling in general is promising for reducing the data rate given the same resolution requirement. Given the prior knowledge for ECG signals, it is possible to design an adaptive sampling scheme which achieves the best possible sampling efficiency without much power overhead.

Designing an energy-efficient biomedical sensor system requires close collaborations across different areas. The dream for self-powered healthcare sensors with medical-grade performance may sound impossible in the past, but nowadays it is within the reach thanks to the continuous research efforts on low-power biomedical system design.

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