SOFT-SWITCHING CURRENT-FED POWER CONVERTERS FOR LOW VOLTAGE HIGH CURRENT APPLICATIONS

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DECLARATION

I hereby declare that this thesis is my original work and it has been written by me in its entirety.

I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Pan Xuewei

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24 June 2014

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Summary

This thesis presents novel current-fed soft-switching topologies and modulation techniques for low voltage high current applications such as solar photovoltaic (PV) and fuel cell based utility interactive inverters and fuel cell vehicles (FCVs). Low voltage energy storage system (ESS) in microgrid, electric vehicles (EVs), uninterruptible power supply (UPS), and DC microgrid are also within the scope of low voltage high current applications. The main objective of this thesis is to develop high-frequency soft-switching current-fed power converters for low voltage high current applications. Fuel cell is a typical low voltage high current source of energy. Fuel cell inverters provide continuous and secured output in all seasons. FCVs offer zero emission, satisfied driving range, and short refueling time, and therefore FCVs exhibit significant potential for transportation. In this thesis, the specifications are taken for FCV but the proposed topologies, modulation techniques, control design, and the demonstrated results are suitable for any general applications of low voltage high current such as PV/fuel cell based utility interactive inverters, UPS, microgrid, V2G, and energy storage. Similar merits and performance are expected.

This thesis first analyzes various propulsion system architectures and power conditioning systems (PCS) for FCVs. Among all aspects of PCS, the main focus of the thesis is on the front-end DC/DC converter interfacing the fuel cell stack and high voltage dc bus, and bidirectional DC/DC converter connecting the energy storage system (ESS) and high voltage dc bus. High voltage dc bus is connected to traction inverter.

The fuel cell stack voltage and generated power vary mainly with fuel flow rate. The front-end DC/DC converter is employed to mitigate such variations, to stabilize output voltage and to control power flow. To achieve high density power converters, high frequency modulation and soft-switching of semiconductor devices is desired. However, to maintain soft-switching over wide variation in source voltage and current while expecting high performance has been a challenge. A magnetizing inductance assisted extended soft-switching three-phase AC link current-fed DC/DC converter is proposed, analyzed, and designed. Simulation and experimental results of the converter are presented. The proposed converter maintained zero voltage soft-switching (ZVS) of all semiconductor devices over wide range of load (full load till 10% load) and source voltage (22V and 41V).

To improve the fuel economy and transient performance of FCVs, auxiliary energy storage devices such as battery or supercapacitor are usually utilized. A bidirectional DC/DC converter is needed to actively control power flow between the energy storage device and the dc bus. A novel naturally clamped zero current commutated soft-switching bidirectional current-fed dual active bridge (CFDAB) isolated DC/DC converter is proposed in this thesis. Proposed secondary modulation technique naturally clamps the voltage across the low voltage side current-fed devices with zero current commutation (ZCC) eliminating the necessity for so far traditionally adopted active-clamp circuit or passive snubbers. Soft-switching is achieved for both direction of power transfer. For the CFDAB converter, small signal model and relevant transfer functions are derived. Two-loop controller is designed and implemented on mixed signal processor Cypress PSoC 5. Simulation and experimental results

are provided to demonstrate the dynamic performance with fast response and small voltage undershoot/overshoot.

Modular multi-cell current-fed full-bridge voltage doubler (CF-FBVD) is proposed for high power application. Parallel Input Series Output (PISO) configuration is employed for interleaving two cells with phase-shifted modulation between them. The input and output ripples were much reduced due to interleaved cells.

The proposed secondary modulation technique is also modified and applied to the current-fed three-phase topology. A trade-off among power transferring capacity, device count, cost, and efficiency is obtained. The input and output filter requirements are much reduced with the interleaved and three-phase design.

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List of Acronyms

EIA	Energy Information Administration
EPA	Environmental Protection Agency
BEVs	Battery Electric Vehicles
HEVs	Hybrid Electric Vehicles
PHEVs	Plug-in Hybrid Electric Vehicles
FCVs	Fuel-Cell Vehicles
ICE	Internal Combustion Engine
ESS	Energy Storage System
DOE	Department of Energy
PEFC	Polymer Electrolyte Fuel Cell
PEMFC	Proton Exchange Membrane Fuel Cell
EMI	Low Electromagnetic Interference
ZVS	Zero-Voltage Switching
ZCS	Zero-Current Switching
AFC	Alkaline Fuel Cell
DMFC	Direct Methanol Fuel Cell
MCFC	Molten Carbonate Fuel Cell
PAFC	Phosphoric Acid Fuel Cell
SOFC	Solid Oxide Fuel Cell
ERCCs	Energy Recovery Clamp Circuits
RC	Resistor-Capacitor
RCD	Resistor-Capacitor-Diode
SRC	Series Resonant Converter
PRC	Parallel Resonant Converter

SPRC	Series Parallel Resonant Converter
QRCs	Quasi-Resonant Converters
MRCs	Multi-Resonant converters
CFDAB	Current-Fed Dual Active Bridge
ZCC	Zero Current Commutation
NVC	Natural Voltage Clamping
SSM	Small Signal Modeling
PM	Phase Margin
GM	Gain Margin
BW	Bandwidth
PSoC	Programmable System-on-Chip
SAR	Successive Approximate Register
PEBB	Power Electronics Building Block
CF-FBVD	Current-Fed Full-Bridge Voltage Doubler
VF-DAB	Voltage-Fed Dual Active Full-Bridge
CF-DAHB	Current-Fed Dual Active Half-Bridge
CF-DAFB	Current-Fed Dual Active Full-Bridge
TDR	Total Device Rating
CESS	Composite Energy Storage System
PIPO	Parallel Input Parallel Output
PISO	Parallel Input Series Output
MIPO	Multiple Input Parallel Output
MISO	Multiple Input Series Output
SISO	Series Input Series Output
SIPO	Series Input Parallel Output

Chapter 1

Background and Problem Definition

1.1 Background

Renewable energy has experienced impressive growth over the past decade owing to the dwindling fossil fuel reserves, concern on global climate change, energy security, and air pollution. Non-conventional energy sources such as solar, hydrogen, and correlated energy storage are low voltage high current sources. These sources produce variable and/or discontinuous output and therefore, power electronics is necessary to condition them into regulated and useful form. The main objective of this thesis is to develop modular high-frequency soft-switching current-fed power converters for low voltage high current applications. Since fuel cell is a typical low voltage high current energy source, in this thesis, the converter are developed under the scenario of fuel cell applications. However, the proposed novel soft-switching current-fed topologies and modulation techniques are suitable for any general low voltage high current applications such as solar/fuel cell based utility interactive inverters, UPS, microgrid, V2G, and energy storage. Similar merits and performance is expected owing to similar specifications and properties.

Global consumption of fossil fuels has been increasing in gigantic proportion with the rapid development of largely populated countries like China and India. U.S. Energy Information Administration (EIA) recently

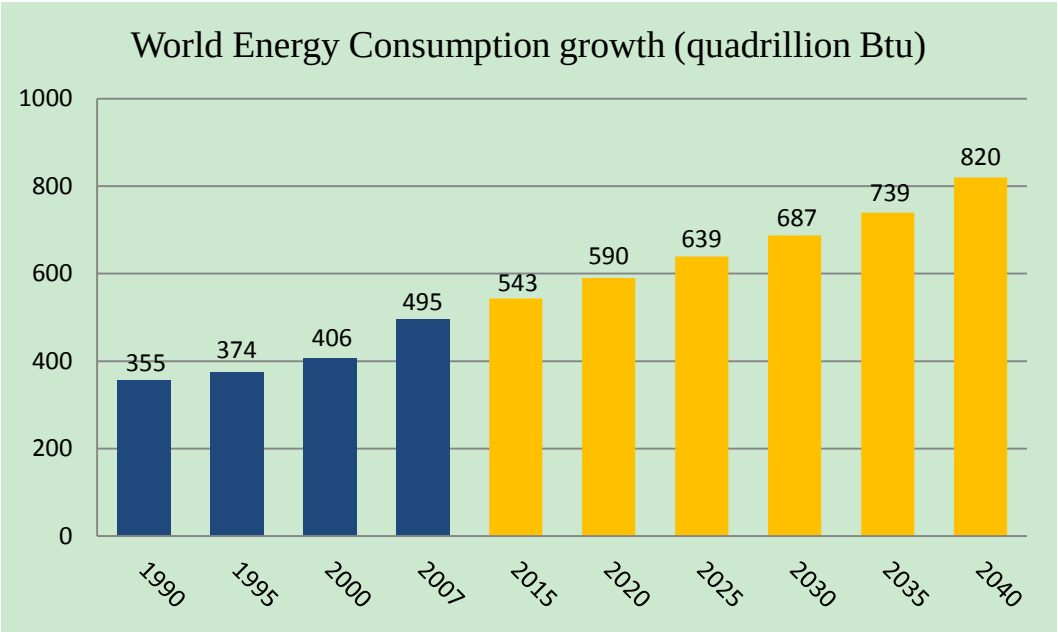


Fig. 1.1. World energy consumption growth [1].

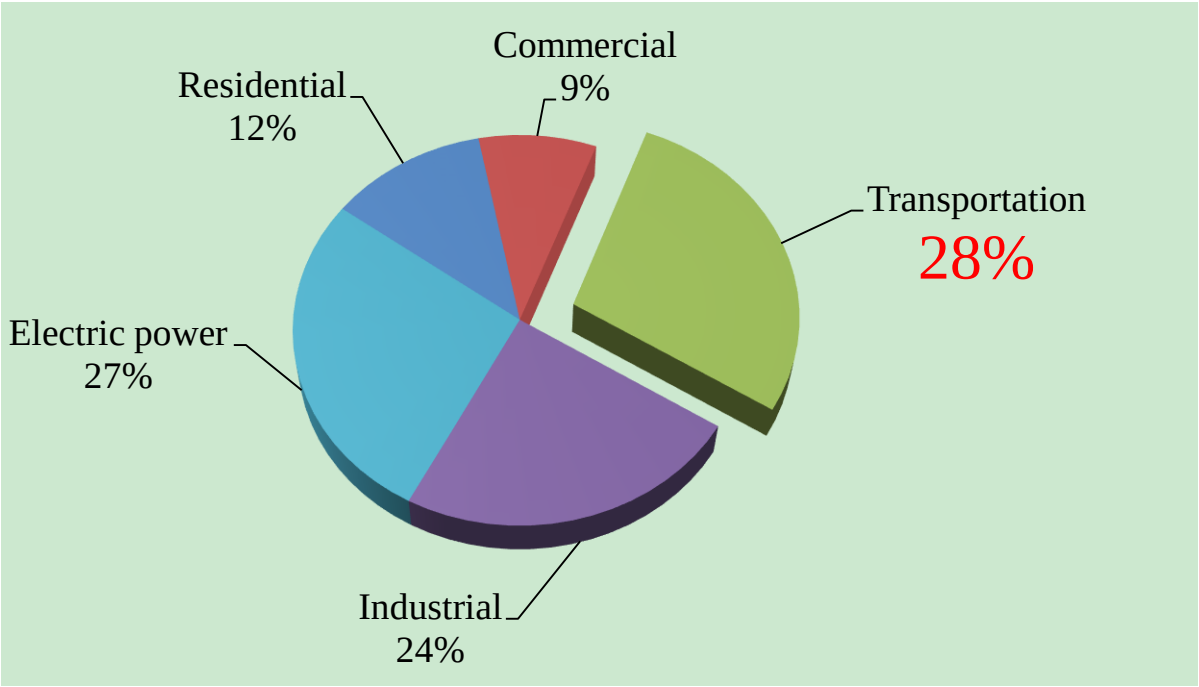


Fig. 1.2. US energy consumption by sector in 2009[2-3].

released International Energy Outlook 2013 (IEO2013) [1-2]. It projects that world's energy consumption will grow by 56% between 2010 and 2040, from 524 quadrillion British thermal units (Btu) to 820 quadrillion Btu as shown in Fig. 1.1 [1]. A major portion of the worldwide fossil fuel consumption occurs in the transportation sector. According to the EIA, the total energy

consumption of United States in 2009 was 27.7 trillion kilowatt hours (kWh), with 28% in transportation sector as illustrated in Fig. 1.2 [2-3]. For transportation sector, 94% of the supply source is from petroleum and only 3% is from renewable energy. Approximately 72% of petroleum is used for transportation sector. About 63% of crude oil consumption relied on import for United States in 2009 [2-3]. Meanwhile, the global number of vehicles is expected to increase from 700 million to 2.5 billion in the next 50 years [4]. Therefore, improving vehicular fuel economy becomes a need.

On the other hand, according to the reports from the U.S. Environmental Protection Agency (EPA), a significant portion of harmful emission is from the vehicles, i.e., vehicles account for about 75% carbon monoxide (CO) emissions, about 35% carbon dioxide (CO_2,) about 45% nitrous oxide (NOx) emissions, and amount for nearly 40% volatile organic compounds emissions [5]. The total carbon emission by 2030 is projected to be around 40 billion metric tons [6]. Therefore, to address the problems of dwindling fossil fuel reserves and air pollution, it is essential to develop new ways of transportation targeting high efficiency, fuel utilization, and better performance.

1.2 The Opportunities and Challenges of Fuel Cell Vehicles

Battery electric vehicles (BEVs), hybrid electric vehicles (HEVs), plug-in hybrid electric vehicles (PHEVs), and fuel-cell vehicles (FCVs) are the emerging means of transportation either to replace or reduce the conventional internal combustion engine (ICE), by using 3-phase electric motor for

propulsion through three-phase inverter. In this Section, the characteristics and properties of different types of electric vehicles are discussed and compared.

A BEV, also known as all-electric vehicle, is propelled by electric motor powered by rechargeable battery packs. ICE and fuel system are completely eliminated from the vehicle. The battery packs can be charged from renewable sources such as wind, solar, etc. or conventional AC grid utility or DC grid in a micro-grid. Therefore, BEVs provide the following merits due to the absence of ICE and fuel system [7]:

- High energy efficiency: BEVs convert about 59-62% of the electrical energy from the grid to power at the wheels.
- Zero emission.
- Independency of crude oil.
- High performance: BEVs provide quiet and smooth operation and require less maintenance.

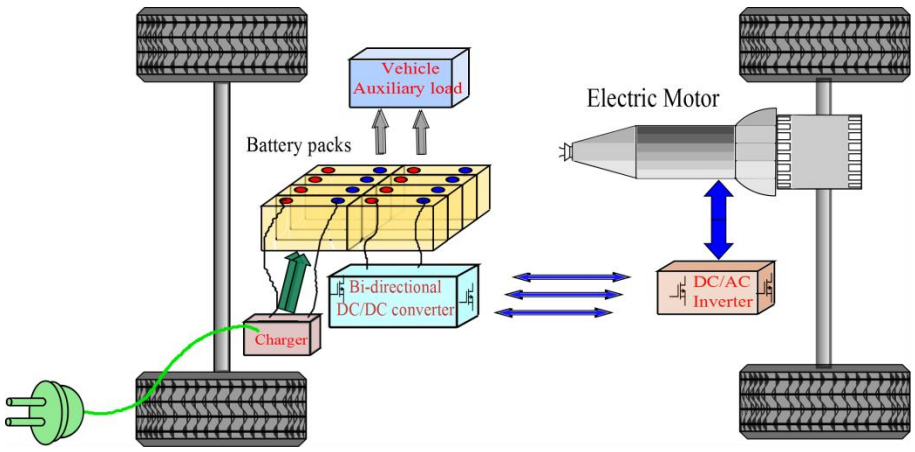


Fig. 1.3. Architecture of a BEV.

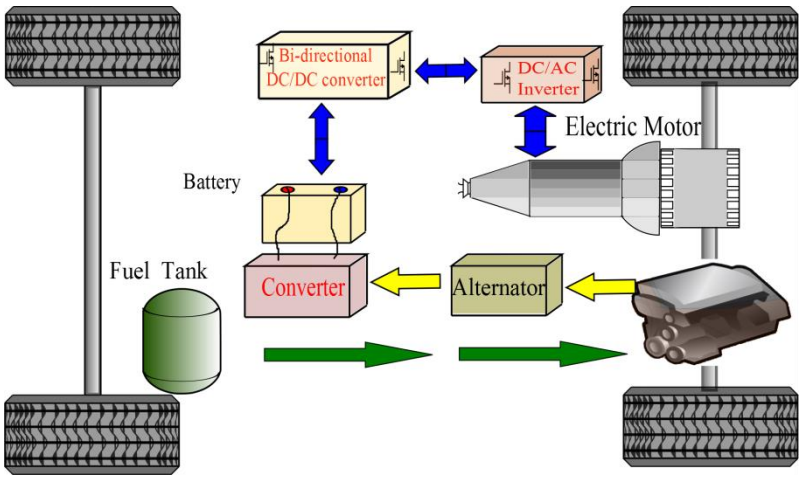


Fig. 1.4. Architecture of a HEV.

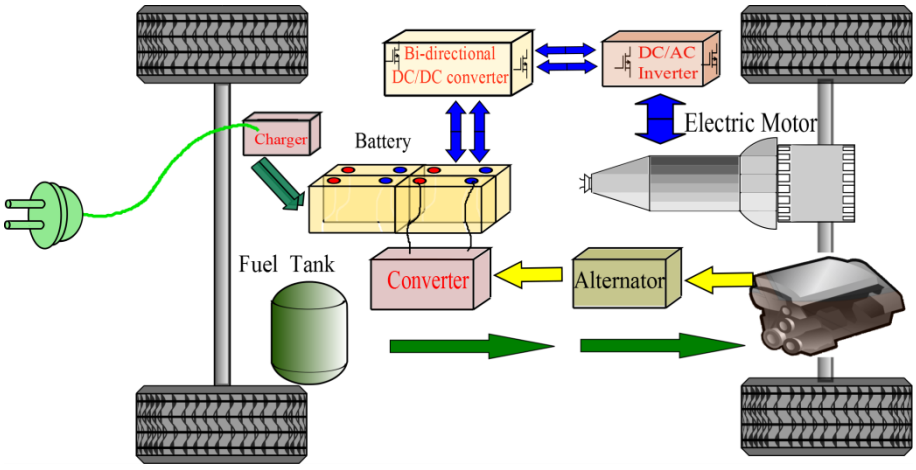


Fig. 1.5. Architecture of a PHEV.

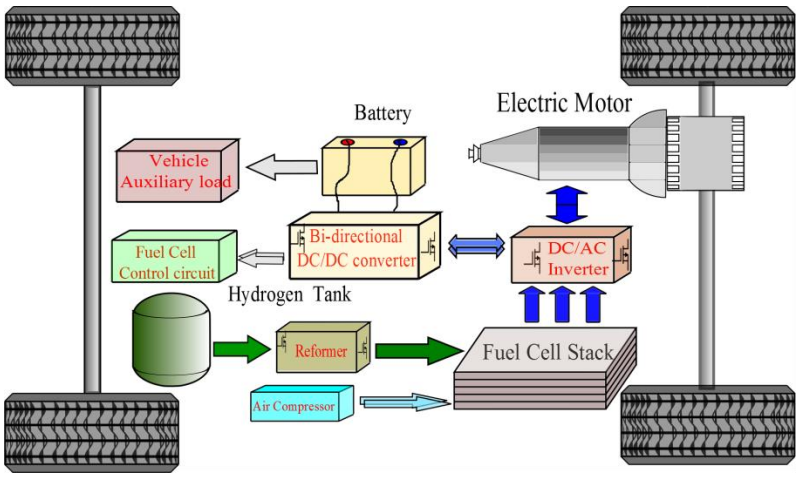


Fig. 1.6. Architecture of a FCV

The substantial drawbacks of BEVs are short driving range (about 100-200 miles), longer charging (refueling) time (4 to 8 hours for slow charging

and 30 min for fast charging), and large volume and heavy weight of battery pack [8].

HEV combines a conventional ICE propulsion system with an electric propulsion system consisting of energy storage system (ESS) and electric motor, as shown in Fig. 1.4. The incorporation of electric propulsion system allows the use of smaller engines than conventional ICE vehicles. The engine can be turned-off during idle or low speed states by utilizing the energy stored in the ESS [9]. The ESS can also assist the ICE drivetrain operating at the most efficient range thus enormously enhancing the fuel economy and reducing the emission [3].

PHEV is a one kind of HEVs with larger rechargeable energy storage that can be charged by connecting a plug to an external electric power source, which gives PHEVs a much larger all-electric range and reduces their petroleum consumption. As illustrated in Fig. 1.5, the ESS can be recharged either from the grid by plugging into an electrical outlet or by the ICE. The PHEVs batteries are capable of powering the vehicle purely on electricity at a normal speed over significant distances (approximately 40 miles) [10].

Due to government tax incentives and high oil prices, HEVs and PHEVs have already enjoyed commercial success. Since the first groundbreaking HEVs, Toyota Prius and Honda Insight, were introduced to the automotive market, a number of automakers initiated HEVs and PHEVs research programs and subsequently developed several vehicle models worldwide [11-12]. Commercially available HEVs include Toyota Prius, Toyota Highlander Hybrid, Toyota Camry Hybrid, Lexus RX 400h, Honda Insight, Honda Civic Hybrid, Honda Accord Hybrid, and Ford Escape Hybrid [13]. In August 2013,

Toyota launched the 4th generation of the Prius and the Prius family reached global cumulative sales of 3.8 million units by June 2013 [11-12].

A typical architecture of a FCV is illustrated in Fig. 1.5. The hydrogen is either stored on board or obtained from reforming the hydrocarbon fuel such as gasoline, natural gas, methanol, or ethanol. This hydrogen rich gas from the reformer is fed to the anode of the fuel cell stack. The fuel cell stack generates electrical energy in dc form after reaction of hydrogen fuel and oxygen from air, i.e., oxidization. The dc output is converted to ac through a 3-phase inverter to drive electric motor. As long as continuity of the fuel supply is maintained, the electric motor can propel the vehicle quietly, smoothly, and efficiently. It requires overall less maintenance compared to ICE vehicles.

The comparison of the above-mentioned types of electric vehicles (EVs) is summarized in [14]. The predicted greenhouse gases, oil consumption and urban air pollution for different EVs scenarios over the 21st century for the US light duty vehicle fleet are compared. HEVs and PHEVs can contribute to reduce greenhouse gases emission only to very limited level. Similarly, HEVs and PHEVs powered by fuels are unlikely to reduce oil consumption considerably and remove urban air pollution completely. Overall, we can conclude that HEVs and PHEVs are not the ultimate solutions for energy crisis and emission problem. Because they still depend heavily on crude oil and emit considerable amount of greenhouse gas. To achieve the long-term goal of zero-carbon emission and substantially cut dependence on oil, BEVs and FCVs are only choice at present. In the report of IEA of 2008, BEVs and FCVs are considered as the most promising alternative powertrain technologies of future sustainable road transport system.

A comparison between BEVs and FCVs in terms of mass, volume, greenhouse gases, fueling time, energy efficiency, fueling infrastructure and cost is given in [14-15]. The recent advancements in battery technology still cannot satisfy BEVs with sufficient energy storage, driving range, fast charging (refueling) ability and low cost. With zero-emission, satisfied driving range, short refueling time, highest potential efficiency, and high reliability, FCVs exhibit significant potential in transportation. Although FCVs are quite promising to serve as next generation transportation system, they are still restricted by several challenges. These issues are briefly discussed below.

1) Development of fuel cell stacks and related system: The polymer electrolyte fuel cell (PEFC), also known as the proton exchange membrane fuel cell (PEMFC) is the most popular for vehicle application. However, a few issues like optimal purification of hydrogen [16], components degradation, and durability [17-18], are under research and development. Fuel cell stack durability in real-world environments is currently about half of what is needed for commercialization [19]. The targets set by the US Department of Energy (DOE) for FCVs is to be 60% efficient, 30US$/kW cost and a nominal lifetime of at least 5000h [19].
2) Currently FCVs are more expensive than ICE vehicles and hybrid vehicles. According to report of US DOE, the fuel cell system cost projected to high-volume of 500,000 units per year is $47/kW in 2012 [19]. To achieve widespread commercialization, the cost is the key bottleneck and must be reduced further to be economically competitive.

3) The barriers of hydrogen production, storage, transmission and refueling infrastructures do not yet support the widespread adoption of FCVs.
4) Compressed hydrogen gas tank on FCVs acquires more space than a gasoline tank. Onboard hydrogen storage is challenging without sacrificing on space, weight, safety, and or cost of vehicles. New techniques like liquid storage at sub-zero temperatures or materials-based storage are still under research [20].

Although there are currently no fuel cell cars available for commercial sale, several major automotive industries have been manufacturing and testing their FCVs. Since 2009, over 20 FCV demonstration cars such as Mazda 5 Hydrogen RE Hybrid, Volkswagen Caddy-Maxi HyMotion, Hyundai Tucson-ix35 FCEV, Mercedes-Benz-F800 have been tested in labs [21-22]. USA and Canada have tested the FCVs on road too. Ballard designed fully integrated fuel cell modules delivering 75 kW and 150 kW for local bus transportation in London which operates up to 19 hours without refueling [23]. As one of the essential enabling technologies of FCVs, power electronic converters play a key role in the commercialization of FCVs, which motivated the research of this thesis.

1.3 Power Conditioning System Architecture of Fuel Cell Vehicles

In FCVs, basically fuel cell stack oxidizes hydrogen gas and generates electrical energy in DC form. Power converters are responsible for conditioning the generated electrical energy to propel the vehicle smoothly

and efficiently. Also, the power electronic converters should satisfy the ever growing auxiliary load demand like electrical steering, air-conditioning, information, entertainment etc. in the vehicle. Generally power electronics in FCVs need to accomplish the following tasks [13, 24]:

- Voltage conversion: Fuel cell is a typical low voltage high current source of energy. The low output voltage generated by the fuel cell needs to be boosted to suitable voltage level to drive electric motor for propulsion. In addition, voltage conversion between energy storage and traction inverter should be performed.
- Energy management: The energy flow from both fuel cell and energy storage system should be well managed to obtain optimal vehicle performance and overall reduced fuel consumption [25-26].
- Electronic control: Power electronics act as a controller for electric traction motor, fuel cell support system and ESS.

Four different power system architectures for FCVs are illustrated in Fig. 1.7 to Fig. 1.10 [27-28]. FCVs suffer from slow dynamic response to load variation due to their slow internal electrochemical and mechanical characteristics. Therefore, secondary source of energy storage that can deliver quick power is needed. As shown in Fig. 1.7 to Fig. 1.10, ESS such as battery or supercapacitor is usually utilized for cold start up, to absorb the regenerative braking energy and to achieve good transient performance.

Fig. 1.7 shows the conventional topology where fuel cell stack itself develops the variable high voltage dc bus [29-32]. High-voltage variable dc bus voltage of either 255V-425V [29-30] or 150-300V [31-32] from the fuel cell stack has

been proposed. A bidirectional DC/DC converter is used to boost low voltage ESS to match fuel cell dc bus voltage. A standard 3-phase inverter (traction inverter) is directly connected at fuel cell bus to invert the fuel cell stack voltage to drive the traction motor. This architecture is simple to realize and cost effective. The main issue with this topology is that fuel cell stack delivering high voltage needs to be selected and employed. However, the output voltage of fuel cell stack depicts a wide variation with the fuel flow, fuel pressure, and stack temperature. For example, the low fuel cell stack voltage corresponds to highest (rated) power and therefore supplies low voltage to traction inverter and motor at rated power. Design of efficient and compact bidirectional dc/dc converter to boost from low voltage ESS to higher variable voltage and maintaining high efficiency at low total harmonic distortion (THD) of three phase inverter whose dc link voltage is varying is a challenge. Besides, there is no galvanic isolation between fuel cell and the motor drive [33].

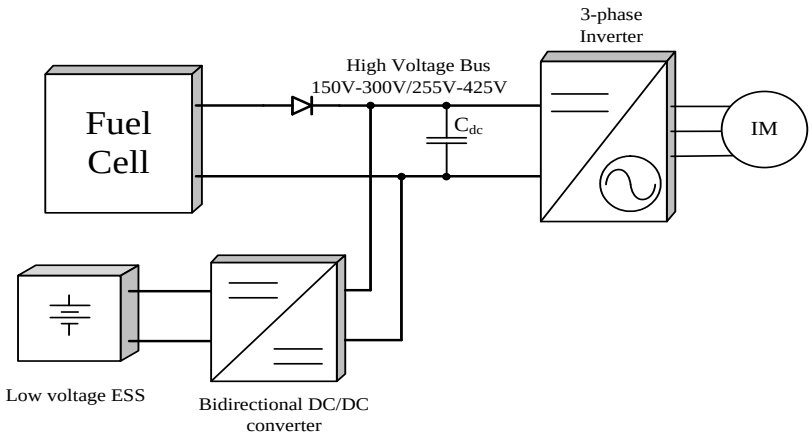


Fig. 1.7. Type 1, power system architecture of FCV with variable high voltage dc bus.

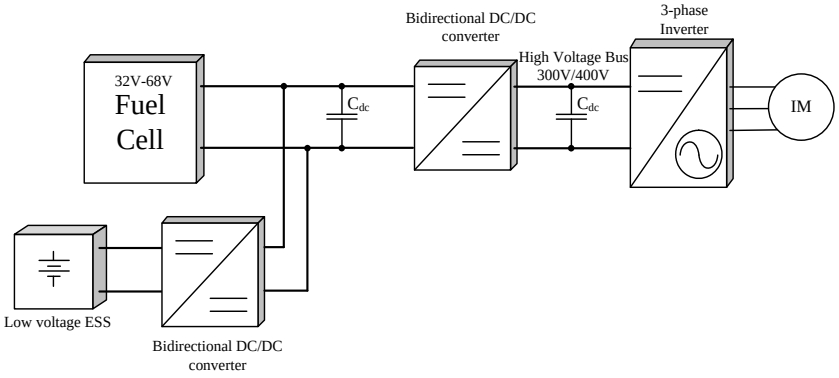


Fig. 1.8. Type 2, power system architecture of FCV with variable low voltage dc bus.

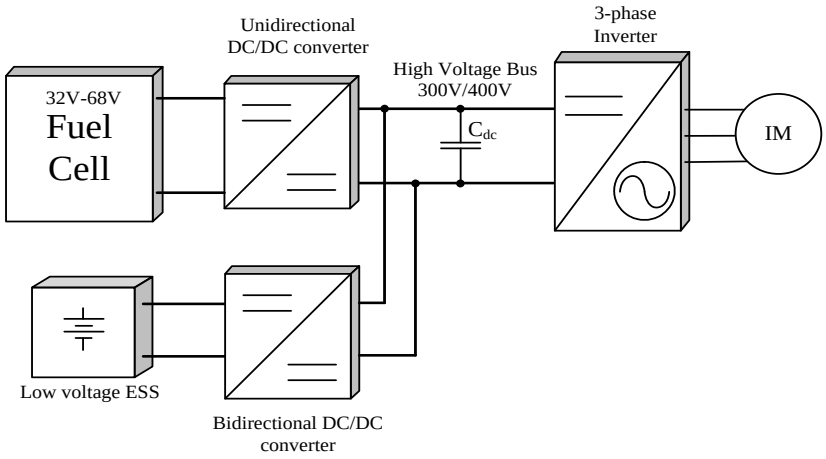


Fig. 1.9. Type 3, power system architecture of FCV with fixed high voltage dc bus.

Fig. 1.8 (type 2) and Fig. 1.9 (type 3) show other two alternative architectures for FCV, where variable low voltage dc bus from fuel cell stack is adopted [27-28]. A fixed high voltage dc bus is developed. A front-end DC/DC converter is utilized to boost the low voltage from fuel cell stack to the peak value needed by the traction inverter. The difference between type 2 and 3 is that the low voltage ESS is directly connected through bidirectional DC/DC converter to the fuel cell stack for type 2 while for type 3 the ESS is connected to fixed high voltage dc bus. The challenge with type 2 is to design a bidirectional DC/DC converter which can maintain high and flat efficiency through wide variation of fuel cell stack voltage. For type 3, to design an efficient bidirectional DC/DC converter with a high boost ratio is difficult.

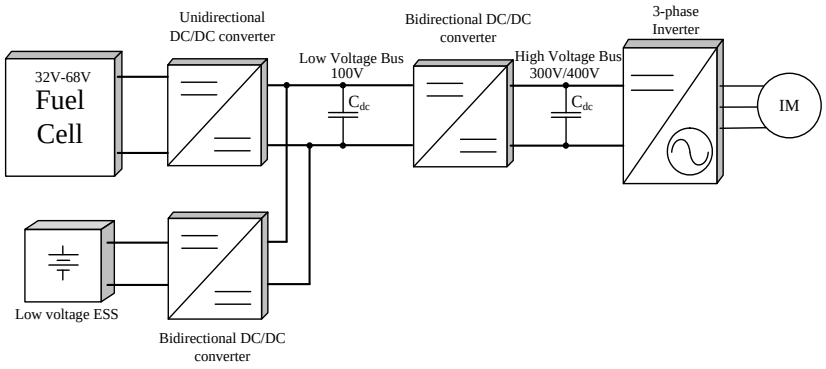
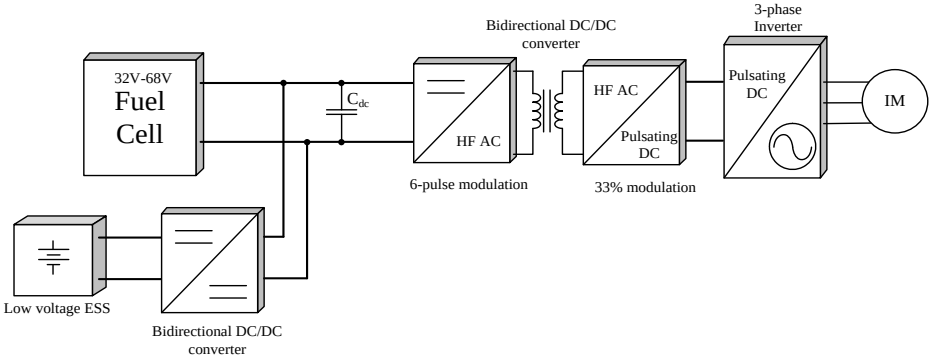
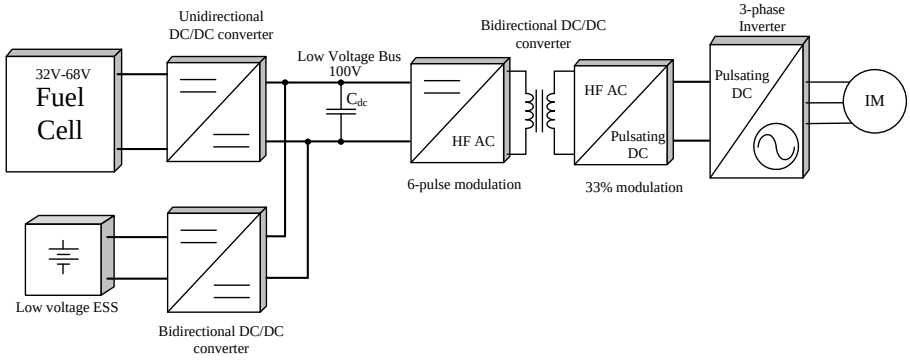


Fig. 1.10. Type 4, power system architecture of FCV with both fixed low voltage and fixed high voltage dc bus.



(a)



(b)

Fig. 1.11. Type 5, modified power system architecture of FCV. (a) Variable low voltage dc bus and high voltage pulsating dc bus, (b) fixed low voltage dc-link and high voltage pulsating dc bus.

In Fig. 1.10, an additional DC/DC converter is included to obtain a constant low voltage dc bus [28, 33]. The low voltage ESS is connected to fixed low voltage dc bus. Since the voltage gain of the bidirectional converter is nearly constant, it is easier to design the converter having maximum

efficiency. Constant dc voltage also simplifies control of 3-phase inverter and traction drive. However, the additional DC/DC converter may deteriorate the overall efficiency and will add to the cost and size. Pulsating high voltage dc bus without large electrolytic capacitor is proposed in [35-37] as shown by Fig. 1.11. Different hybrid modulation techniques have been introduced to control the front-end dc/pulsating dc converter and the back-end pulsating dc/ac converter, which can reduce the switching losses and increase the efficiency.

Low voltage fuel cell stack ranging from 32V-68V is more suitable for compact vehicles like fuel cell cars with power rating up 5kW. While for the high power rating (higher than 100kW) FCVs like fuel cell buses, high voltage fuel cell stack may be preferred [18]. Therefore, it is necessary to select and design a suitable architecture according to specific application requirements. Similar architectures as shown in Fig. 1.7 to Fig. 1.11 can also be employed in other low voltage high current applications such as solar and fuel cell based standalone UPS applications.

1.4 Problem Definitions and Research Objectives

As one of the essential enabling technologies, power electronics plays a vital role for low voltage high current applications. Major requirements for the power conditioning system are summarized as follows [27]:

1) Cost effective. Electrical and electronic system account for 20% to 30% of the total cost of a modern vehicle [13]. Power electronics is one of the essential enabling technologies that can provide an option to compensate the cost gap.

2) Low weight, small volume and high power density.
3) High reliability and fault tolerance. Approximately 10-15 years life span is expected for the operation of power electronics.
4) Modular and scalable. Modular and scalable design can help improve the manufacturability.
5) High efficiency.
6) Low electromagnetic interference (EMI). To increase the electromagnetic compatibility, soft-switching is generally preferred at high switching frequency.
7) Electric isolation.

   Galvanic isolation is preferred to prevent electric leakage/electric shock.

Overall efficiency is of a major concern in these applications to utilize the fuel at the best and needs to be concretely addressed [38]. The overall purpose of the research is to develop low cost, high density, integrated and modular power electronics. The problems of existing research and corresponding specific objectives are pointed out as follows:

Issue 1: A front-end DC/DC converter is generally employed to boost the low fuel cell stack voltage to the high dc bus voltage. Soft-switching is desired for small size, light weight and high efficient system design. Fuel cell is an unregulated low voltage current intensive source and its voltage and current vary in a wide range. For the present application, retaining soft-switching over a wide variation in input voltage and operating range of load is a challenge. Several soft-switching converters lose soft switching at higher

input voltage and light load conditions [39]. Therefore, design of a front-end DC/DC converter with a wide soft-switching range is a challenge.

- Objective 1: To develop front-end DC/DC converter interfacing the fuel cell stack and high voltage dc bus with extended soft-switching range, low current-ripple, and high current capability.

Issue 2: Bidirectional DC/DC converter is required to interface the low voltage ESS and high voltage dc bus. Current-fed converter is a competitive choice for low voltage high current ESS application. Usually active-clamp circuits or passive snubber circuits have been used to limit the device voltage spike at turn-off for current-fed converters. These auxiliary circuit either deteriorate the converter's efficiency or increase the complexity (additional components and relevant driving requirements) resulting in higher cost, and poor reliability. Besides, it is difficult to design a stable wide bandwidth controller for boost converter due to its non-minimum phase characteristics.

- Objective 2: To investigate and propose bidirectional DC/DC converter topologies with low cost, high reliability, high gain, high power handling capacity, and high efficiency.
- Objective 3: To design and implement a low cost and effective control system for the proposed converter.
- Objective 4: To propose and develop modular multi-cell bidirectional DC/DC converter for different specific application needs especially for higher power application.

1.5 Thesis Contributions

The major contributions of the thesis are summarized as follows:

- A magnetizing inductance assisted extended range soft-switching three-phase current-fed DC/DC converter is proposed to interface the low voltage fuel cell stack to a high voltage dc bus.
- Novel bidirectional snubberless naturally commutated soft-switching current-fed DC/DC converters are proposed to interface the ESS to high voltage dc bus.
    1) Current-fed dual active bridge (CFDAB) isolated DC/DC converter.
    2) Current-fed bidirectional three-phase isolated DC/DC converter.
    3) Modular multi-cell current-fed bidirectional full-bridge voltage doubler.
- Small signal modeling of proposed bidirectional CFDAB converter and closed loop control implementation with Cypress PSoC 5.

1.6 Thesis Outline

The thesis is laid out into seven Chapters to explain the individual contributions. The thesis is organized as follows:

A magnetizing inductance assisted modified design to achieve extended range soft-switching of a current-sharing three-phase AC link active-clamped (ZVS) current-fed DC/DC converter is proposed and studied in Chapter 2. The detailed steady-state analysis and operation has been explained with operating

waveforms and equivalent circuits. Simulation results using PSIM 9.0.4 are presented to verify the proposed analysis and design. An experimental converter prototype rated at 300W has been developed, and tested in the laboratory to practically confirm and demonstrate the converter performance over wide variations in input voltage and output power.

A snubberless naturally clamped zero current commutated (ZCC) soft-switching CFDAB DC/DC converter is proposed and studied in Chapter 3. Proposed converter serves as the power conditioner between ESS and high voltage dc bus. A novel secondary modulation technique is proposed to naturally clamp the device voltage across the low voltage primary side eliminating the necessity for traditional active-clamp circuit or passive snubbers. Steady state analysis, design, simulation results using PSIM 9.0.4 and experimental results from laboratory prototypes are demonstrated. Experiment results clearly justify the soft-switching (zero-current switching (ZCS) of primary side devices and zero-voltage switching (ZVS) of secondary side devices). Device natural voltage-clamping (NVC) and zero current commutation (ZCC) are inherent and load independent.

Small signal model of the proposed bidirectional naturally commutated CFDAB converter has been derived by using state-space averaging technique in Chapter 4. Relevant transfer functions are determined. A closed two-loop controller is designed and implemented on Cypress PSoC 5. The effectiveness of the designed controller has been verified by simulation and experimental results during transient operation of load.

Current-fed full-bridge voltage doubler DC/DC converter (CF-FBVD) is proposed in Chapter 5 as a modular power electronics building block. Six

different possible configurations of the proposed modular multi-cell converter are researched. A design example of interleaved two cells for the parallel input series output (PISO) configuration has been investigated. The secondary modulation method proposed in Chapter 3 has been applied to clamp the voltage across the primary side switches naturally with zero current commutation. Experimental results have been demonstrated. Multi-cell design reduces the input and output filter requirements and achieves low ripple magnitude. It is usually employed to scale the power level.

Proposed secondary modulation technique in Chapter 3 has been extended for three-phase topology for high power applications. Three-phase designs are employed to enhance the power handling capacity and reliability of the converter while obtaining merits of lower input current ripple, reduction of passive components' size, reduced device voltage and current ratings, and better thermal distribution. Steady-state analysis and operation have been studied. Simulation waveforms using PSIM 9.0.4 are shown to verify the accuracy of the proposed analysis and design. A lab prototype has been developed in the laboratory to validate the performance of the converter.

Chapter 7 gives a summary of research contributions of this thesis and further mentions recommendations for the possible future work.

Chapter 2

Magnetizing Inductance Assisted Extended Range Soft-switching Three-phase AC Link Current-fed DC/DC Converter

2.1 Introduction

This Chapter mainly focuses on the design of the front-end DC/DC converter interfacing the fuel cell stack and high voltage dc bus connected to the traction inverter of FCVs. The converter is unidirectional and should boost the low fuel cell stack voltage up to traction inverter DC voltage. In addition to voltage boost function, the converter should be suitable for fuel cell application. The characteristics and properties of fuel cell are briefly introduced in Section 2.2. Based on fuel cell characteristics, the requirements of the front-end DC/DC converter is summarized in Section 2.3. Then high frequency (HF) transformer isolated unidirectional DC/DC converter such as PWM and resonant converters are reviewed and compared in Section 2.4. An extended range soft-switching (ZVS) three-phase ac link current-sharing current-fed isolated DC/DC converter is proposed in Section 2.5. Section 2.6 presents the detailed steady-state operation and analysis during different intervals of operation of the proposed converter. A complete design procedure illustrated by a design example is given in Section 2.7. The analysis and design have been verified by simulation results using PSIM 9.04 and

experimental results from a laboratory prototype in Section 2.8. This Chapter is concluded in Section 2.9.

2.2 Fuel Cell Characteristics and Properties

A fuel cell is an electrochemical device that converts the chemical energy of a fuel into electrical energy directly. Classification of fuel cells mainly include the alkaline fuel cell (AFC), proton exchange membrane (PEM) fuel cell, direct methanol fuel cell (DMFC), molten carbonate fuel cell (MCFC), phosphoric acid fuel cell (PAFC), and solid oxide fuel cell (SOFC) [40]. PEM fuel cells are more suitable for FCVs owing to their high power density, relatively low operating temperature, smaller size, and rapid start-up [40-41]. A typical diagram of a PEM fuel cell is given in Fig. 2.1. It consists of anode, cathode, electrolyte, and catalyst. At the anode, hydrogen reacts with the catalyst and decomposes into protons and electrons. The positively charged protons then conducted through the electrolyte, while the negatively charged electrons are forced to travel through the external circuit, creating a current and supplying energy. At the cathode, oxygen reacts with electron, producing the byproduct water and heat [40-41].

Fig. 2.2 shows the voltage-current characteristic of a fuel cell, which can be divided into three regions R-1, R-2, R-3 [42-43] involving different losses. Region R-1 is dominated by activation loss due to the slow rate of the electrochemical reaction [42-43]. Region R-2 is dominated by resistive loss occurring due to the resistance from the flow of ions in the electrolyte and electrons through the external circuit [42-43]. Concentration loss is caused by

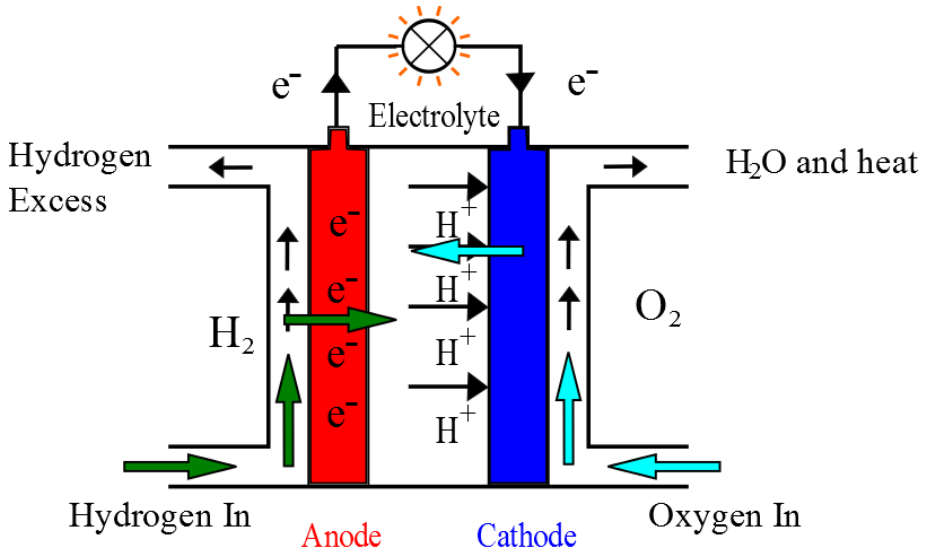


Fig. 2.1. PEM fuel cell diagram.

consumption of reactant at the electrode by the reaction, leading to loss of potential due to inability of the surrounding material to maintain the initial fluid concentration [41].

Fig. 2.2 also shows how the voltage of the fuel cell varies with the output current. As shown in Fig. 2.2, the output voltage of the fuel cell decreases with increase in current drawn from it. The boundary of R-2 and R-3 regions is known as optimum point (knee point), providing the maximum power output. At high current density (region R-3), the fuel cell will experience a sharp voltage drop due to the reactant starvation/concentration loss. Prolonged operation in the region R-3 may damage the fuel cell [42-43], thus the fuel cell is generally operated in region R-2.

The performance of fuel cell is influenced by multiple operating variables including temperature, fuel pressure/fuel flow, gas composition, reactant utilization, current density, cell design and other factors (impurities, cell life) [41]. Fig. 2.3 shows fuel cell voltage-current characteristics at different fuel flow [42-43]. As the fuel flow increases, the optimum/knee point shifts to

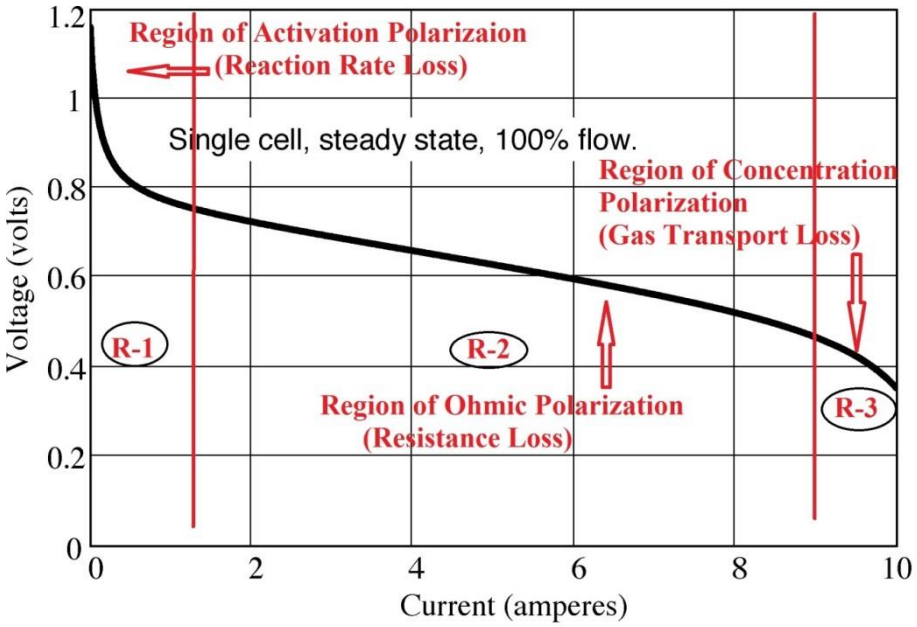


Fig. 2.2. Fuel cell voltage-current characteristic [42].

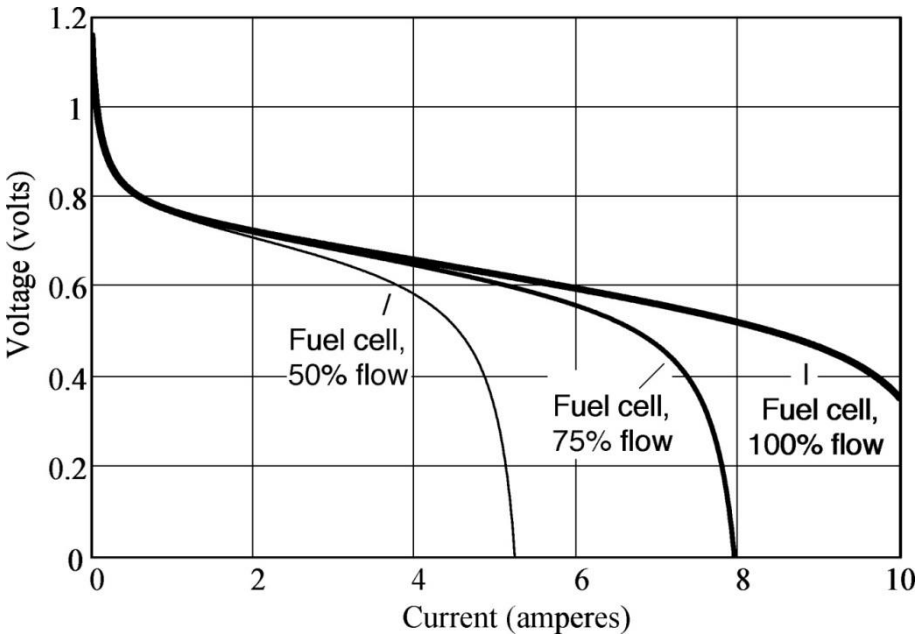


Fig. 2.3. Fuel cell voltage-current characteristic at different fuel flow [42].

higher current density region but the fuel cell output voltage decreases. Therefore, the power generated by the fuel cell can be controlled by controlling the fuel flow. As illustrated by the Fig. 2.2 and Fig. 2.3, the output voltage of single cell is about 0.4V~0.8V at different load conditions for a given fuel flow rate. From the above introduction, it can be concluded that fuel cell is an unregulated low voltage, current intensive source and its voltage and

current varies over a wide range. The fuel cells are stacked in series to achieve higher voltage level. However, in most of cases, the output voltage of the fuel cell stack still cannot meet high voltage requirement in various applications.

Therefore, a DC/DC converter needs to be employed to elevate the low dc fuel cell stack voltage up to the required value [40-44]. The front-end DC/DC converter should be able to mitigate such variation, stabilize output voltage and control the power flow.

The requirements of this front-end DC/DC converter are summarized as follows:

1) High boost ratio.

   For a typical fuel cell stack, the output voltage is around several tens of volts such as 22V-41V [44], 32V-52V [42], and 30V-60V. While dc voltage bus in FCVs usually varies from 300V to 400V [40]. Therefore a high boost ratio of ten to twenty is quite necessary.

2) The ability to accommodate wide range of source voltage and load.

3) Low input current ripple.

   As discussed earlier, fuel cell stacks should not be allowed to operate in region R-3 (Fig. 2.2) concerning stability, reliability and lifetime of fuel cell stack. However, while feeding low frequency alternating current to the electric motor in FCVs, low frequency harmonic components may appear at the fuel cell stack. This low frequency ripple may shift the operating point from region R-2 to R-3 and may result in possible shut down (Fig. 2.2). In [45-47], the magnitude of the low frequency ripple should be minimized to increase the durability of fuel cell and utilization of the fuel. The high frequency current ripple

caused by the switching of converter also plays a critical role in the catalyst lifetime of fuel cell stacks [48]. In particular, sharp current rise/fall and large magnitude of high frequency ripple should be avoided.

4) Isolation.

   In major fuel cell applications, HF transformer isolated front-end DC/DC converters are preferred to provide high voltage step-up ratio and as well the electrical isolation between the fuel cell stack and the high voltage dc [35]. This also allows series connection at the output of DC/DC converters adding to scalability and design flexibility for higher power application.

5) Compact design, lightweight and high efficiency.

   High frequency operation is necessary to realize compact, lightweight, and low cost converter. Hard switched converter suffers from high switching losses, high component stress, and electromagnetic interference (EMI) at high switching frequency [44]. Therefore, soft-switching is desired and implemented to raise the switching frequency of semiconductor devices above 20 kHz till MHz range to obtain the objectives [44].

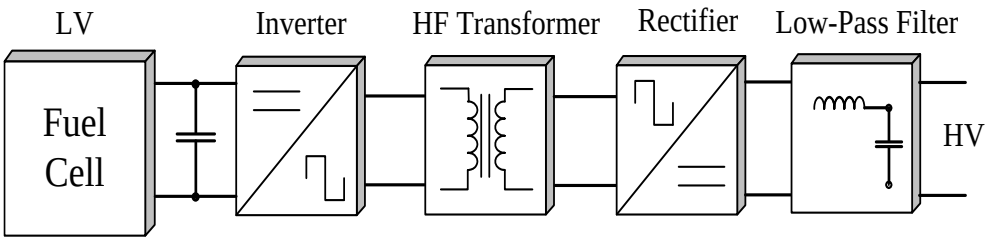


Fig. 2.4. Configuration of voltage-fed HF transformer isolated DC/DC converter for low voltage high current applications.

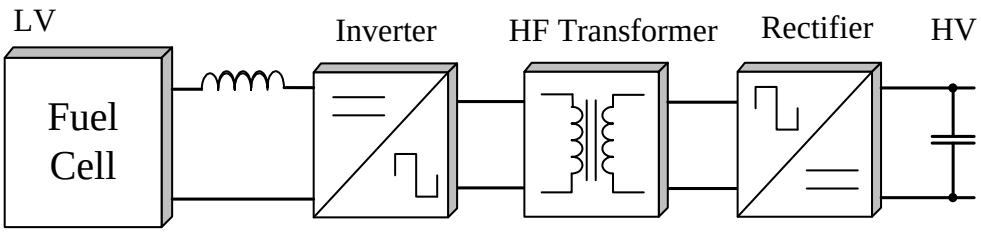


Fig. 2.5. Configuration of current-fed HF transformer isolated DC/DC converter for low voltage high current applications

2.3 A Brief Review of High Frequency Transformer Isolated DC/DC Converter Topologies

DC/DC converters can be categorized into two major types, voltage-fed and current-fed as shown in Fig. 2.4 and Fig. 2.5. Each can be further classified into PWM and resonant converters. Voltage-fed converter employs a large capacitor in parallel with the source while current-fed converter employs an inductor in series with the source.

2.3.1 Voltage-fed PWM DC/DC Converter

Voltage-fed PWM converters can be divided into two types: (1) single-ended topology and (2) double-ended topology depending on the core utilization of the transformer. For single ended topologies (flyback, forward), the flux of the core swings in only one quadrant of the B-H curve while for the double-ended topologies (half-bridge, full-bridge, push-pull etc.) the flux swings in two quadrants [49]. The core utilization of double-ended topologies is better, which affects the size and weight of the converter crucially. Besides, the transformer of double-ended topologies can be further optimized over full duty cycle range [49]. Also double ended topologies are modular, scalable and are preferred for higher power applications. Therefore, the double-ended

topologies are more suitable for FCVs where high power density and high power transferring ability are desired.

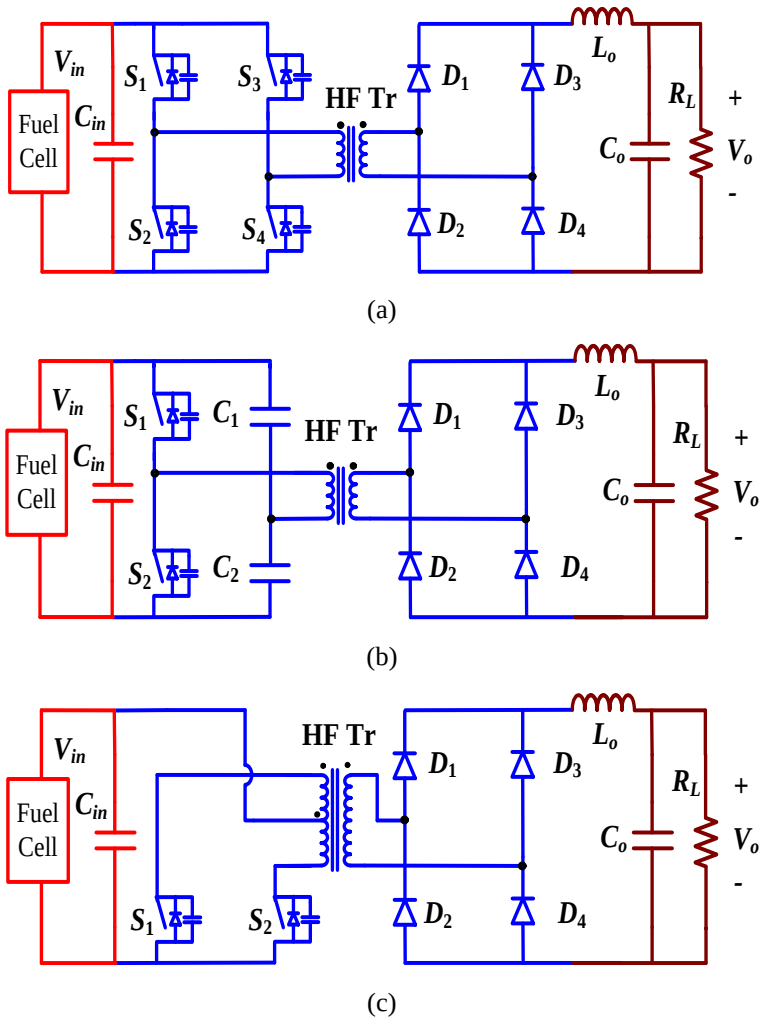


Fig. 2.6. Voltage-fed HF transformer isolated DC/DC converters. (a) Full-bridge converter (b) half-bridge converter (c) push-pull converter.

Table 2.1: The comparison of three different voltage-fed DC/DC converters.

Topologies	Advantages	Disadvantages
Push-pull	Least number of components Ground connected switches	Twice voltage rating Low transformer windows utilization
Half-bridge	Good transformer window utilization Less number of active components	Twice the current rating More number of passive components Unbalance problem due to split capacitors Not compatible with current-mode control
Full-bridge	Reasonable device rating High power transferring capacity Good transformer window utilization	High number of active components High driving requirement

Push-pull, half-bridge and full-bridge configurations are three basic double-ended topologies as shown in Fig. 2.6, advantages and disadvantages of which are compared in Table 2.1. The push-pull topology requires the least number of components and all the primary switches are connected to the ground reducing the gate driving requirement. The disadvantages of the push-pull topology are high voltage stress across switches (2x of input voltage) and transformer utilization issue due to center-tapped transformer design. Half-bridge and full-bridge topologies are free from these two drawbacks. The voltage stress across switches equals input voltage and transformer utilization is better with its simpler design. The merit of half-bridge is that it has less number of active components resulting lower cost and driving requirement.

Owing to higher power transferring capacity and modular configuration among all three topologies, voltage-fed full-bridge topology has potential for FCVs application. Phase-shifted modulation technique is widely adopted for front-end DC/DC conversion [50-65]. Energy stored in the leakage inductance of the transformer is utilized to achieve ZVS soft-switching of the semiconductor devices. This technique suffers from the following problems.

- Limited soft-switching range.

  The lagging-leg of the full-bridge converter tends to lose ZVS at light load conditions. Loss of ZVS implies high switching losses at high switching frequency resulting in low efficiency and EMI issue. The ZVS range can be extended by increasing the leakage inductance of the transformer [50] or by adding an external series inductor [51]. However, adding a large series inductance reduces the power transfer capability of the converter and voltage gain due to the effective duty

cycle loss of the converter. Additional auxiliary circuits have been proposed to extend the ZVS range [52-56]; however a considerable amount of power is dissipated in the auxiliary circuits [52-56].

- Voltage overshoot and ringing across rectifier diodes.

  Voltage overshoot and ringing across rectifier diodes are caused by the resonance between the transformer leakage inductance and parasitic capacitance of the rectifier diodes. Reducing the value of leakage inductance is one of the solutions, but it will reduce the ZVS range. RCD snubber circuit [57] and an active-clamping circuit [58] are often used to suppress the voltage spikes across the diodes. Several energy recovery clamp circuits (ERCCs) have also been proposed to accommodate the issues of the voltage spikes in [59-65]. Although such techniques are able to solve the problem, they increase the complexity of the converter and degrade the efficiency.

- High circulating current through the devices and magnetics.

  During the freewheeling intervals, the reflected current from the output circulates through the primary side, causing additional conduction loss.

2.3.2 Current-fed PWM DC/DC Converter

The voltage-fed converters have low switch voltage ratings enabling the use of switches with low on-state resistance. This can significantly reduce conduction loss of primary side switches. However, voltage-fed converters suffer from several limitations, i.e., high pulsating current at input, limited soft-switching range, rectifier diode ringing, duty cycle loss (inductive output filter), higher circulating current through devices and magnetics, and relatively

low efficiency for high voltage amplification and high input current specifications [39].

Voltage-fed topologies employ considerably large electrolytic capacitor to suppress the large input current ripple, resulting in large size, high cost and shortened lifetime. Compared with voltage-fed converters, current-fed converters exhibit the following merits:

1) Smaller input current ripple, which is beneficial to extract and maintain stable maximum power point from fuel cell system and extend its lifespan.

2) Lower transformer turns-ratio: Current-fed converters are boost derived converters and have built-in boost function. Therefore, current-fed converters have lower transformer turns ratio, which can simplify the design and reduce losses.

3) Negligible diode ringing and free from duty cycle loss due to capacitive output filter.

4) Easier current control ability. The input current can be directly and precisely controlled. Besides, the fuel cell stack output current is proportional to hydrogen flow rate as illustrated by Fig. 2.3. Therefore, if the fuel cell stack current is directly and precisely controlled, the amount of hydrogen utilized in a direct hydrogen system could be better controlled [48].

With these merits, current-fed converters have been justified and demonstrated as a suitable option for low voltage high current applications (fuel cell, PV, batteries). Different topologies of current-fed PWM DC/DC converters have been researched. As illustrated in Fig. 2.7, full-bridge, half-bridge, and push-pull topologies have been proposed for the low voltage side

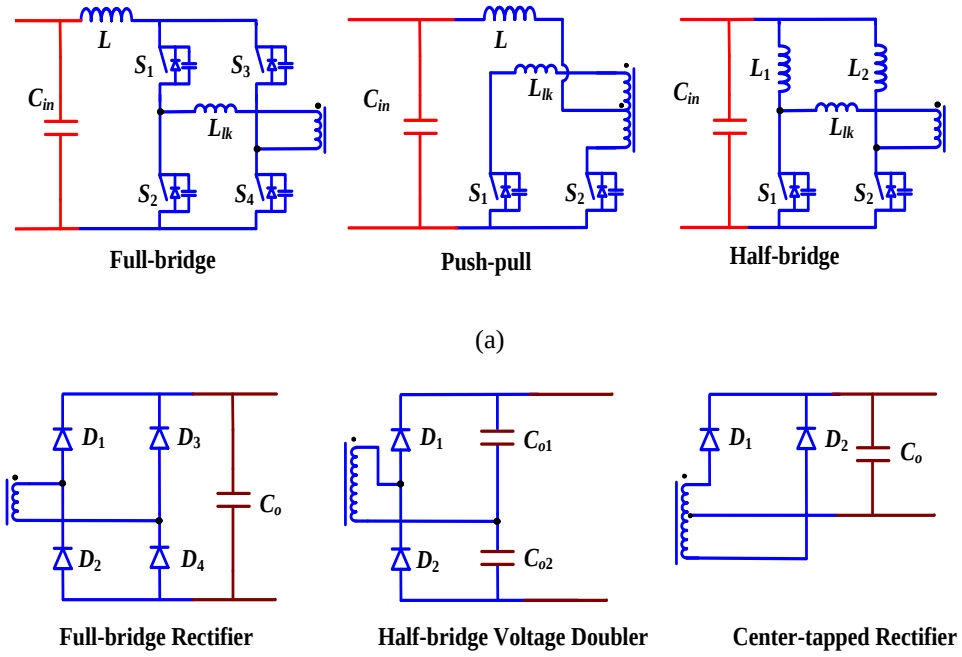


Fig. 2.7. Conventional current-fed PWM DC/DC converter topologies. (a) Three typical topologies for the low voltage inverter stage. (b) Three typical topologies for the high voltage side rectifier stage.

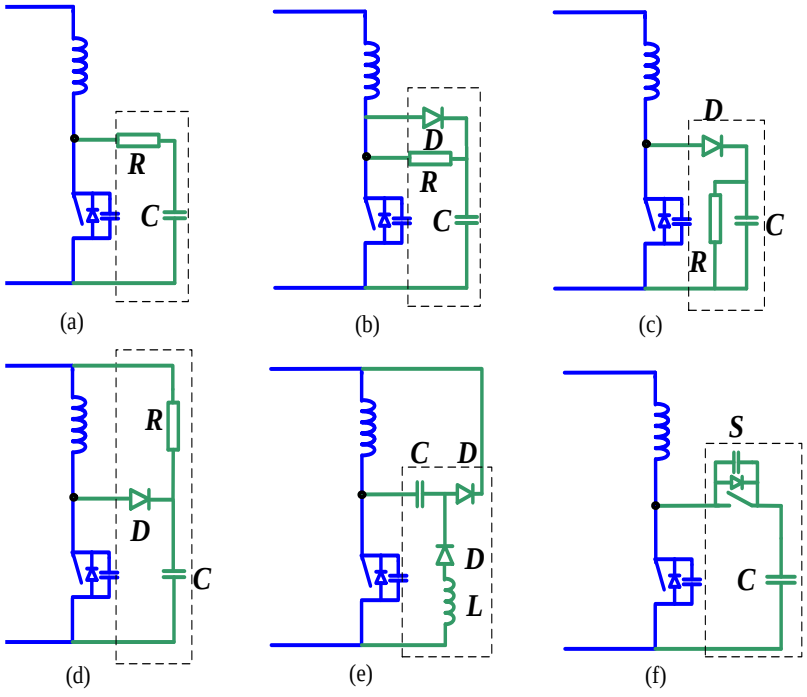


Fig. 2.8. Snubbers for suppressing the voltage spike: (a) Dissipative RC snubber, (b)(c)(d) Dissipative RCD snubber,(e) Non-dissipative energy recovery LC snubber, and (f) active-clamping snubber.

inverter stage. For the high voltage side rectifier stage, there exist some popular topologies like full-bridge diode rectifier, half-bridge voltage doubler, and center-tapped rectifier. However, the major drawback of current-fed converters is high voltage spike across device at turn-off owing to the energy stored in the leakage inductance [66]. Snubbers are generally required to limit the voltage spike to prevent the switching device from a permanent breakdown. Different snubber circuits such as dissipative, regenerative, and active snubbers etc. have been proposed as shown in Fig. 2.8 [67]. These snubbers are employed to accommodate the whole boost inductor current until the HF transformer current is fully built up to the level of the boost inductor current

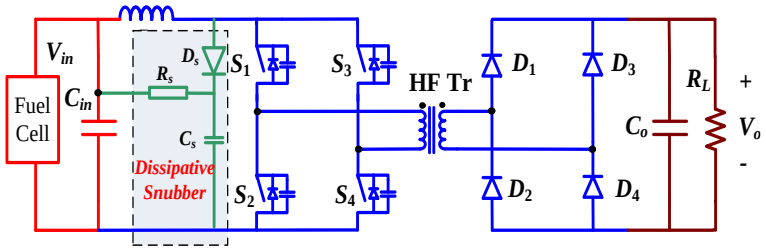


Fig. 2.9. Current-fed full-bridge DC/DC converter employing dissipative snubbers.

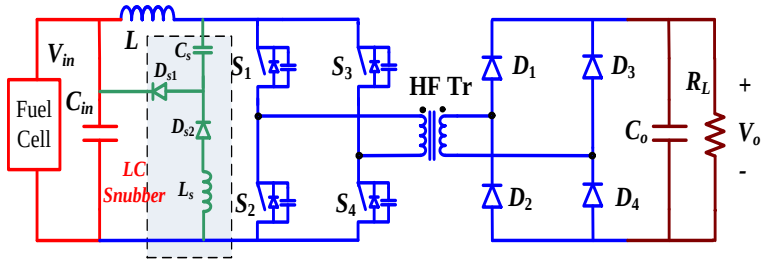


Fig. 2.10. Current-fed full-bridge DC/DC converter employing non-dissipative snubbers.

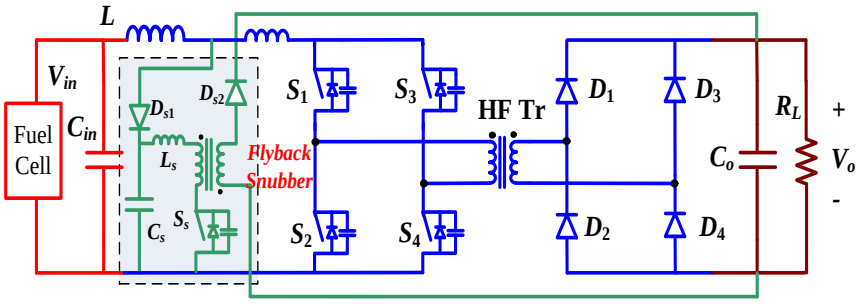


Fig. 2.11. Current-fed full-bridge DC/DC converter with an auxiliary flyback snubber.

[66]. Fig. 2.9 illustrates current-fed full-bridge converters using the conventional dissipative snubbers like RC or RCD snubbers [68-69]. Dissipative snubbers lead to low efficiency owing to the energy dissipated in the snubber resistor. To improve the efficiency, energy recovery LC snubbers have been proposed as shown in Fig. 2.10 [70-73]. The LC snubber stores the surge energy in the capacitor during device turn-off. Once the switch is turned on, the capacitor is reset and energy stored in the inductor is fed back to the input instead of being dissipated. However, the conventional LC snubber has several problems like complex structure, difficult optimal design, and do not assist in soft-switching. In [74], an auxiliary flyback snubber including a capacitor, a diode and a flyback converter was introduced to recycle the absorbed energy as illustrated in Fig. 2.11. The flyback snubber alleviates the voltage spike and transfers the trapped energy to the load. The circuit operates with hard switching. A similar auxiliary snubber was proposed in [75] to clamp the voltage across primary switches, recycle the absorbed energy to the load, and assist in achieving ZVS of the primary switches. However, both of those two auxiliary snubbers are too complex.

Active-clamping snubber circuit [66, 69, 72, 76-80], which consists of a switch and a capacitor, is proposed to clamp the device voltage. The energy stored in the leakage inductor can be recycled, thus solving the energy loss problem. With a proper parametric design, ZVS of primary switches can be achieved. Several examples of typical current-fed half-bridge topologies employing active-clamping techniques are displayed in Fig. 2.12 [72]. The active-clamping circuit proposed in Fig. 2.12(a) can achieve (ZVS both at turn-on and turn-off, but the voltages across the auxiliary switches are twice as

those of the main switches [72]. The active-clamping snubber circuits need floating active device(s) and high value of HF clamp capacitor for accurate and effective clamping.

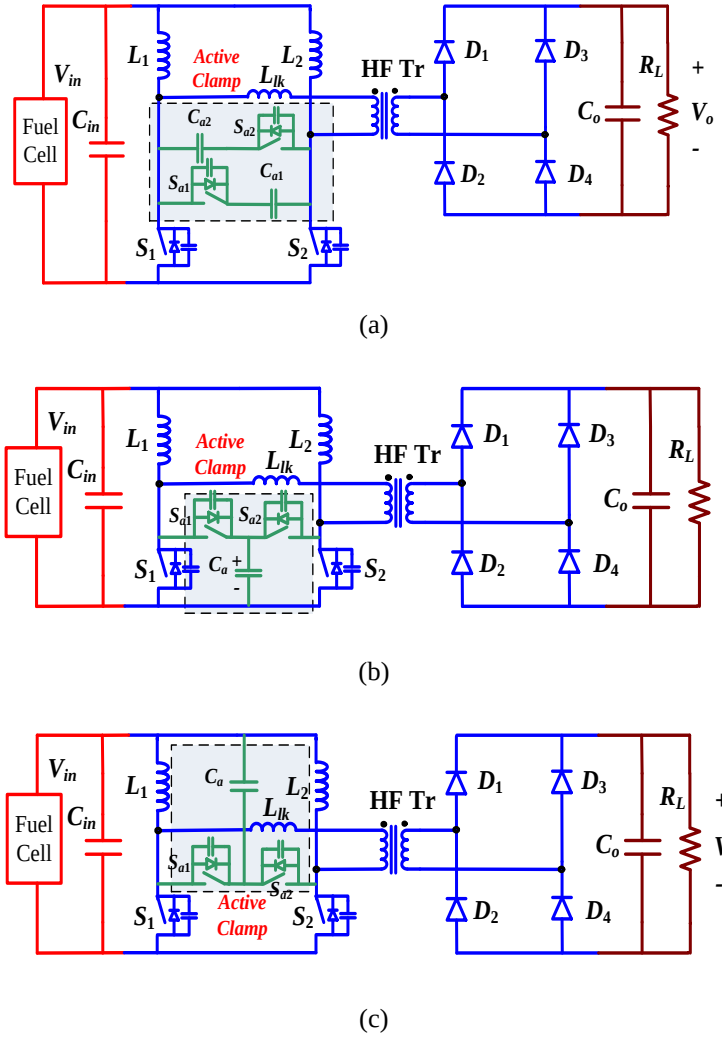


Fig. 2.12. Current-fed L-type half-bridge DC/DC converters with three different types of active-clamping circuits.

Another approach is to apply ZCS to divert the current away from the switches before turning them off. In [81], external auxiliary circuits are utilized to achieve ZCS and reduce the circulating current for current-fed full-bridge topology as illustrated in Fig. 2.13. For the topology shown in Fig. 2.14 [82], the transformer leakage inductance and device output capacitance are used to create a quasi-resonant path to facilitate ZCS. The shortcoming is that

four extra diodes are connected in series with the main switches to reduce the circulating loss. This brings more conduction losses and increases the cost and circuit footprints. For the topology proposed in [83] as shown in Fig. 2.15, an external circuit consisting of two uni-directional switches and a resonant capacitor is employed to obtain ZCS turn-on/off of the switches. The ringing due to the interaction of the transformer leakage inductance and switch capacitance is major limitation of this technique. Higher voltage rating devices or dissipative snubbers are needed.

In [84], an external boost converter is added to provide a path for the boost inductor current and send the trapped energy to the load as shown in Fig. 2.16. A small inductor is needed to achieve ZCS turn-on/off. Although the trapped energy can be recycled, the auxiliary circuits still contributes to a significant amount of loss. The higher cost and circuit complexity are two major concerns.

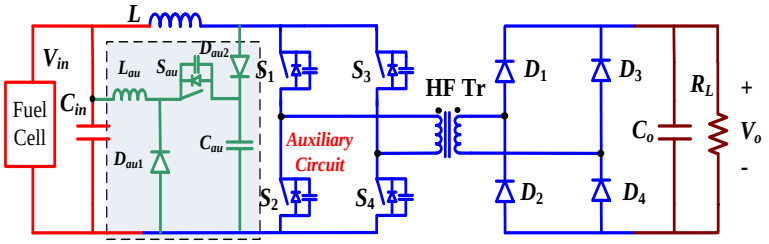


Fig. 2.13. Current-fed ZCS full-bridge DC/DC converter with parallel auxiliary circuit.

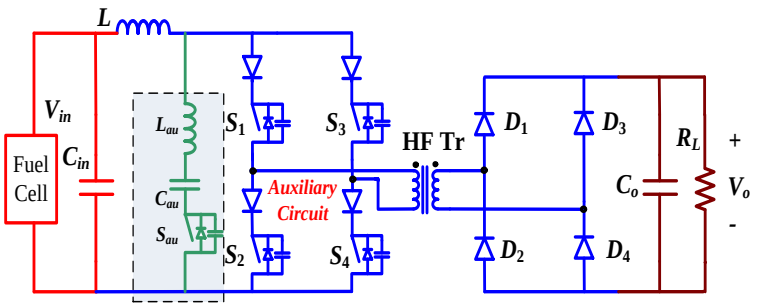


Fig. 2.14. Current-fed ZCS full-bridge DC/DC converter with current-blocking diodes.

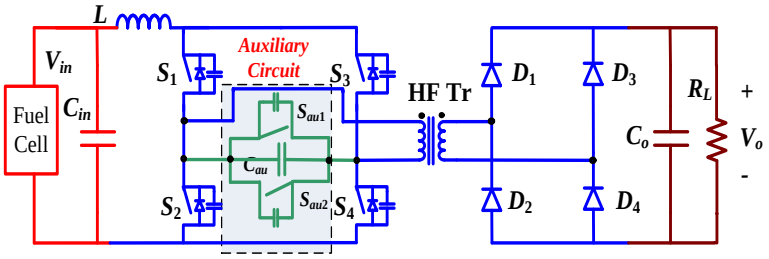


Fig. 2.15. Current-fed ZCS full-bridge DC/DC converter with snubber energy.

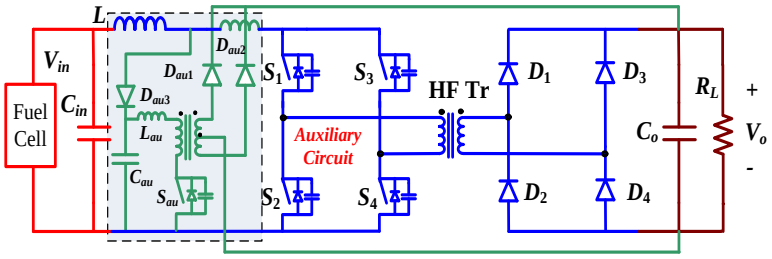


Fig. 2.16. Current-fed ZCS full-bridge DC/DC converter with an external boost converter.

2.3.3 Resonant-type DC/DC Converter (Voltage-fed and Current-fed)

Since 1980's, the resonant converters have arisen as a hot research topic and significant amount of research efforts were diverted to this area. The resonant concept, basically, is to incorporate resonant tanks (consisting of capacitor(s) and inductor(s)) to create oscillatory voltage and/or current waveforms so that ZVS or ZCS soft-switching of semiconductor devices can be achieved. The classification of resonant-type DC/DC converter is shown in Fig. 2.17 [85].

For the conventional resonant converters, three most popular topologies including Series Resonant Converter (SRC) [86-87], Parallel Resonant Converter (PRC) [88-89], and Series Parallel Resonant Converter (SPRC) [90] have been intensively investigated. The main problems with these resonating techniques are high circulating energy for low voltage high current specifications, high turn-off current at high input voltage conditions [91]. Thus

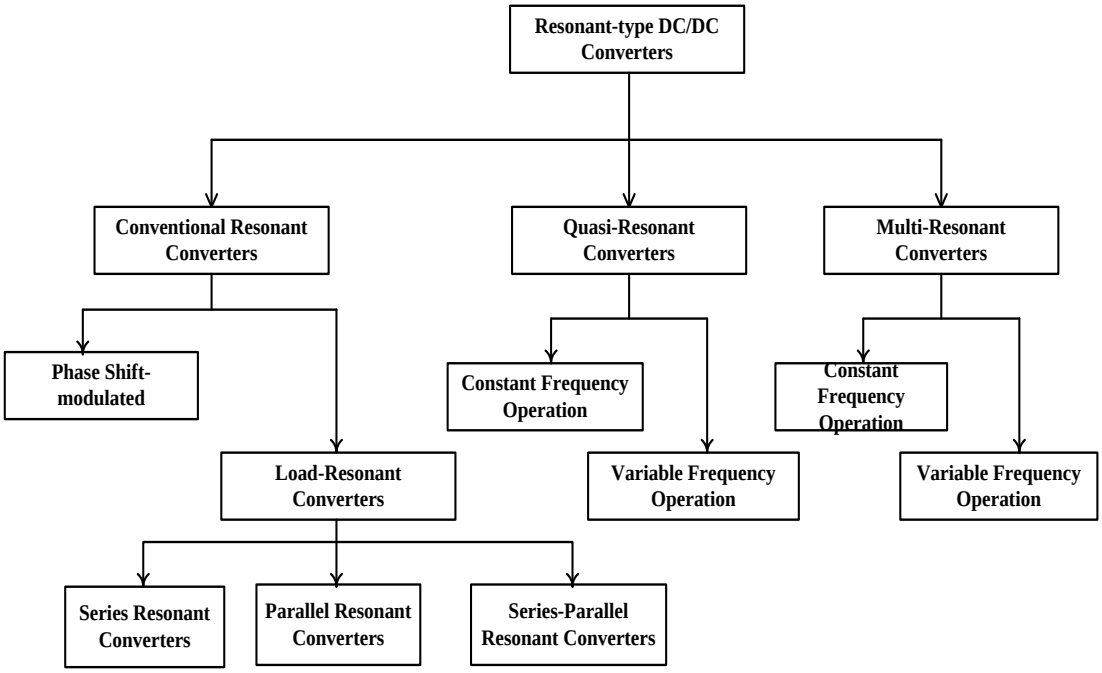


Fig. 2.17. Classification of resonant-type DC/DC converter [85].

conduction loss and switching loss will increase at high input voltage condition making these techniques not suitable for wide voltage and power range application like fuel cells, solar, energy storage, etc. [91].

Quasi-Resonant Converters (QRCs) can be viewed as a hybrid of PWM and resonant converters [92]. QRCs are derived from conventional PWM converters by replacing the power switches with the resonant switch [92]. A large family of ZCS-QRCs [93-96] and ZVS-QRCs [97-99] are derived from conventional PWM converters. The switch current and/or voltage waveforms are forced to oscillate in a quasi-sinusoidal manner so that ZCS and/or ZVS can be realized. Both ZCS-QRCs and ZVS-QRCs have *half-wave* and *full-wave* mode of operations [92].

Tabisz and FC Lee introduced the concept of Multi-Resonant converters (MRCs) in 1988 [100-103]. The MRCs' resonating tank incorporates all major parasitics in the resonant circuit, including the switch output capacitance,

diode junction capacitance and transformer leakage inductance, which allow MRCs to operate with soft-switching for all the semiconductor devices [104]. Constant off-time, variable-frequency control is required for ZVS-QRCs and MRCs and constant on-time, variable-frequency control is required of ZCS-QRCs [104]. However, they can be modified to operate at constant-frequency control [105].

Recently, considerable amount of research has been contributed towards current-fed HF transformer isolated resonant converters due to the inherent high boost capability, which make them more promising for high boost applications [106-111]. However, compared with the PWM converters, resonant converters have much higher peak current/voltage, possibly resulting in higher conduction loss [49]. Also higher VA rating devices may be needed. Besides, many resonant converters require variable frequency control for the output regulation. The variable frequency control scheme makes the control complex and difficult to optimize the design of magnetics with respect to volume and efficiency [112].

2.3.4 Problem Definition

This Chapter mainly focuses on investigating the novel techniques to improve the overall performance of the front-end DC/DC converters with wide input voltage range and load variation. In the above literature survey of HF transformer isolated DC/DC converter, different topologies including PWM converters, resonant converters, voltage-fed and current-fed converters, QRCs, etc. have been reviewed. It is found that current-fed converters are better options for high voltage amplification and high input current applications. The

main advantages are smaller input current ripples, high boost ratio, and direct and easier current control ability. Considering that the resonant converters suffer from the problems of high resonant current/voltage, high circulating energy, difficult control, and optimize design for wide range voltage and load specifications, PWM converters seem to be more promising.

Comparison of various soft-switching DC/DC converters, which can be possibly applied to fuel cell application, has been studied in [39]. It has been shown that two-inductor active-clamped current-fed converter has desirable features for fuel cell application like reduced peak currents, lower input current ripple, wide ZVS range, high efficiency, and free from duty cycle loss and rectifier diode ringing [44]. Although, two-inductor active-clamped current-fed converter exhibits comparatively large range of soft-switching, the converter still loses ZVS at light load condition for rated input voltage and also for the input voltage above the rated values [39, 44]. Therefore, to retain soft-switching over a wide variation in source voltage and power transfer is a challenge. Loss of soft-switching and with HF operation results in significantly low efficiency. This is a typical case when fuel cell voltage changes with temperature, fuel flow, and fuel pressure. A nearly flat efficiency curve is desired for better fuel/source utilization.

The objectives of this Chapter is to design and develop a DC/DC converter interfacing the fuel cell stack and high voltage dc with extended soft-switching range, low current-ripple, high boost ratio, high power transferring ability, and high efficiency.

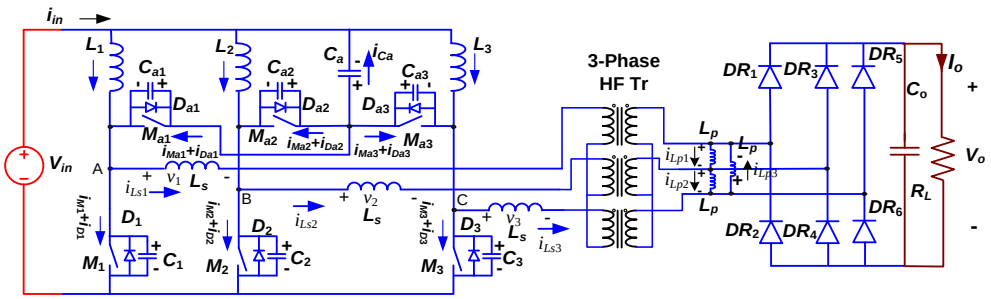


Fig. 2.18. Three-phase AC link current-sharing active-clamped current-fed isolated DC/DC converter.

2.4 Proposed Three-phase AC link Current-sharing Active-clamped Current-fed Isolated DC/DC Converter

In this Chapter, a modified three-phase ac link active-clamped ZVS current-fed DC/DC converter, shown in Fig. 2.18, is proposed. This configuration is a competitive topology in the area of power supplies/converters, designed for high power applications with high voltage conversion ratio. FCVs are one among such applications, which require the low dc voltage of the fuel cell stack to be boosted up to the level of peak of the motor rated voltage for traction inverter to invert. Boost-function of current-fed converter offers the advantage of high voltage conversion with a relatively lower transformer turns ratio. For higher power applications, three-phase configuration [115] and interleaved approaches (multi-cell) [116] have been adopted over single-phase to increase the power handling capacity while achieving high efficiency and reduced thermal requirements. However, three phase converter has higher power density than single-phase and lesser number of components compared with interleaved converter. Three-phase AC link conversion offers the following merits:

1. High power transferring ability

2. Reduced size of input boost inductors
3. Reduction in size of input and output filters due to increased 3x ripple frequency [117],
4. Reduced value of auxiliary clamped capacitor
5. Reduced peak current stresses across the components.
6. Relatively lower average and RMS current through the devices owing to current sharing, which reduce conduction losses as well as turn-off losses,
7. High efficiency due to reduced conduction losses in switches due to current sharing compared to single–phase design.
8. Higher power density and lower cost compared to interleaved topology.

2.5 Operation and Analysis of the Converter

The following assumptions are made to study and understand operation and analysis of the converter: a) Boost inductors L_1, L_2 and L_3 are large to maintain constant current through them. b) Clamp capacitor C_a is large to maintain constant voltage across it. c) All switches and diodes are ideal. d) Series inductors L_{s1}, L_{s2} and L_{s3} include the leakage inductances of the transformer. e) Magnetizing inductances of the HF transformer are part of parallel inductance L_{p1}, L_{p2} and L_{p3}. The analysis of the converter can be divided into two parts and is discussed next.

2.5.1 Discontinuous Auxiliary Clamp Capacitor Current

This condition arises when source/input voltage is low. In this case, only one main switch is off at a time. Duty cycle D of the main switches is higher

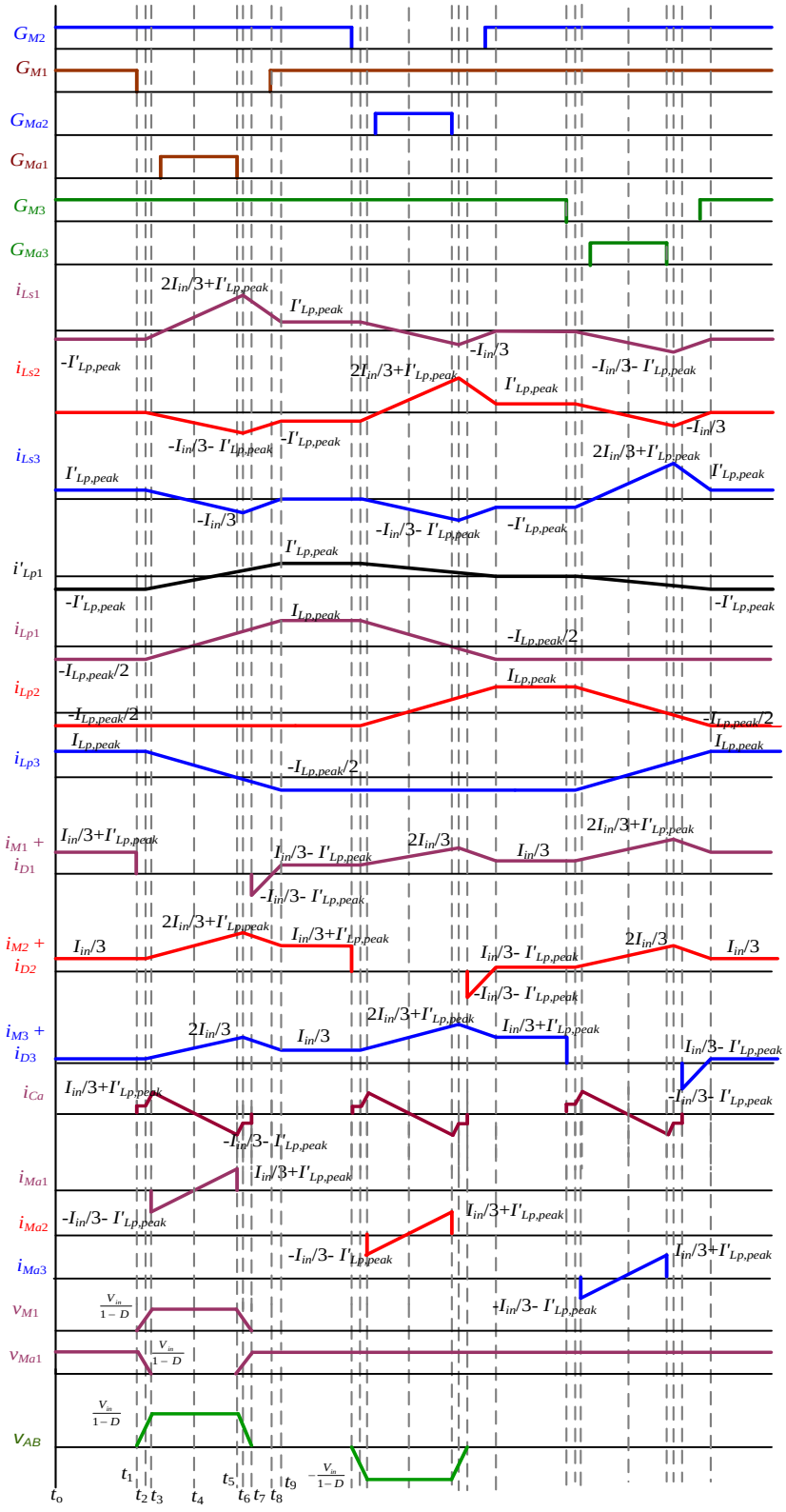


Fig. 2.19. Operating waveforms of the proposed converter in discontinuous auxiliary clamp capacitor current case (case A).

than 0.66 (D > 0.66) and all three main switches can be on at a time. Steady-state operating waveforms are shown in Fig. 2.19. The main switches M_1, M_2

and M_3 are operated with gating signals phase-shifted with each other by 120^o with an overlap. The overlap varies with the duty cycle value. The converter operation in one third HF cycle is explained using the equivalent circuits shown in Fig. 2.20.

Interval 1 (Fig. 2.20a; $t_o < t < t_1$): In this interval, all the main switches M_1, M_2 and M_3 are ON. Boost inductors L_1, L_2 and L_3 are storing energy. Power is transferred to the load by the output filter capacitor C_o. The series and parallel inductors are shorted and constant currents flow through them are given by

$$i_{Ls1} = -I'_{Lp,peak} \quad i_{Ls2} = 0 \quad i_{Ls3} = I'_{Lp,peak}$$

$$i_{Lp1} = i_{Lp2} = -I_{Lp,peak}/2 \quad i_{Lp3} = I_{Lp,peak} \tag{2-1}$$

where i_{Ls1}, i_{Ls2} and i_{Ls3} are series inductor currents, i_{Lp1}, i_{Lp2} and i_{Lp3} are parallel inductor' currents, $I_{Lp,peak}$ is the peak value of current through the parallel inductors L_{p1}, L_{p2} and L_{p3} (on secondary side). $I'_{Lp,peak}$ is the peak value of line current through parallel inductors reflected from secondary side to primary, given by

$$I'_{Lp,peak} = \frac{3 \cdot n \cdot I_{Lp,peak}}{2} \tag{2-2}$$

$$I'_{Lp,peak} = \frac{V_{in}}{3 \cdot f_s \cdot (L_s + L'_p)} \tag{2-3}$$

Here, n is the turns ratio of the transformer, L_p' is the per phase inductance of parallel inductor reflected to primary side (from delta to star), given by

$$L'_p = \frac{L_p}{3 \cdot n^2} \tag{2-4}$$

Voltage across the auxiliary capacitor C_a is

$$V_{Ca} = \frac{D}{1-D} V_{in} \tag{2-5}$$

where duty ratio of main switches M_1, M_2 and M_3, $D = T_{on}/T_s$; T_{on} = main switch conduction time and T_s = switching period.

Voltage across the auxiliary switches is

$$V_{Ma1} = V_{Ma2} = V_{Ma3} = V_{in} + V_{Ca} = \frac{V_{in}}{1-D} \tag{2-6}$$

Currents through main switches M_1, M_2 and M_3 are given by

$$i_{M1} = I_{in}/3 + I'_{Lp,peak} \tag{2-7}$$

$$i_{M2} = I_{in}/3 \tag{2-8}$$

$$i_{M3} = I_{in}/3 - I'_{Lp,peak} \tag{2-9}$$

Voltage across the rectifier diodes

$$V_{DR} = V_o/2 \tag{2-10}$$

Interval 2 (Fig. 2.20b; $t_1 < t < t_2$): At $t = t_1$, main switch M_1 is turned off. Boost inductor L_1 current (i_{L1}) and series inductor current (i_{Ls1}) start charging the main switch snubber capacitor C_1 and discharging the auxiliary switch snubber capacitor C_{a1} linearly in proportion to their capacitances value. Final voltages across the main switch M_1 and auxiliary switch M_{a1} reach $V_{M1}(t_2) = V_o/n$ and $V_{Ma1}(t_2) = V_{in}+V_{Ca}-V_o/n$.

Interval 3 (Fig. 2.20c; $t_2 < t < t_3$): Snubber capacitors C_1 and C_{a1} are still charging and discharging. Main switch voltage v_{M1} rises from V_o/n to $V_{in}+V_{Ca}$. A voltage $v_1 = 2\cdot(v_{M1} - V_o/n)/3$ appears across the series inductor in phase A and

current through it (i_{Ls1})starts increasing linearly. A negative voltage v_2=v_3= –(v_{M1}–V_o/n)/3 appears across the series inductors in phase B and C and current through them (i_{Ls2} and i_{Ls3}) start increasing linearly in negative direction. Rectifier diodes DR_1, DR_4 and DR_6 are forward biased and start conducting and power is transferred to the load. Voltage across main switch is given by

$$v_{M1} = \frac{V_o}{n} + (\frac{I_{in}}{3} + I'_{Lp,peak}) \cdot \frac{1}{(C_1 + C_{a1})} \cdot (t - t_2) \qquad (2\text{-}11)$$

The currents through the series inductors, given by

$$i_{Ls1} = -I'_{Lp,peak} + \frac{2}{3} \cdot \frac{v_{M1} - (V_o / n)}{L_s} \cdot (t - t_2) \qquad (2\text{-}12)$$

$$i_{Ls2} = -\frac{1}{3} \cdot \frac{v_{M1} - (V_o / n)}{L_s} \cdot (t - t_2) \qquad (2\text{-}13)$$

$$i_{Ls3} = I'_{Lp,peak} - \frac{1}{3} \cdot \frac{v_{M1} - (V_o / n)}{L_s} \cdot (t - t_2) \qquad (2\text{-}14)$$

The currents through the parallel inductors are given by

$$i_{Lp1} = -\frac{I_{Lp,peak}}{2} + \frac{V_o}{L_p} \cdot (t\text{-}t_2) \qquad (2\text{-}15)$$

$$i_{Lp2} = -\frac{I_{Lp,peak}}{2} \qquad (2\text{-}16)$$

$$i_{Lp3} = I_{Lp,peak} - \frac{V_o}{L_p} \cdot (t\text{-}t_2) \qquad (2\text{-}17)$$

Currents through the main switches M_2 and M_3 are given by

$$i_{M2} = \frac{I_{in}}{3} + \frac{1}{3} \cdot \frac{v_{M1} - (V_o / n)}{L_s} \cdot (t - t_2) \qquad (2\text{-}18)$$

$$i_{M3} = \frac{I_{in}}{3} - I'_{Lp,peak} + \frac{1}{3} \cdot \frac{v_{M1} - (V_o / n)}{L_s} \cdot (t - t_2) \qquad (2\text{-}19)$$

Currents through the conducting rectifier diodes are given by

$$i_{DR1} = \frac{i_{Ls1}}{n} - (i_{Lp1} - i_{Lp3}) \tag{2-20}$$

$$i_{DR4} = -\frac{i_{Ls2}}{n} + (i_{Lp2} - i_{Lp1}) \tag{2-21}$$

$$i_{DR6} = -\frac{i_{Ls3}}{n} + (i_{Lp3} - i_{Lp2}) \tag{2-22}$$

The clamp capacitor current i_{Ca} increases linearly and reaches its peak value at the end of this interval that is equal to $I_{Ca,peak} = I_{in}/3 + I'_{Lp,peak} - i_{Ls1}(t_3)$. Since this interval is very small and the series inductor currents do not change too much, the peak auxiliary clamp capacitor current is $I_{Ca,peak} \cong I_{in}/3 + I'_{Lp,peak}$.

At the end of this interval, the auxiliary switch snubber capacitor C_{a1} is discharged completely to zero and the main switch snubber capacitor C_1 is charged to its full voltage, equal to $V_{in}+V_{Ca}$. Final values are: $v_{Ca1}(t_3) = v_{Ma1}(t_3) = 0$; $v_{M1}(t_3) = v_{C1}(t_3) = V_{in} + V_{Ca} = \frac{V_{in}}{1-D}$.

Interval 4 (Fig. 2.20d; $t_3 < t < t_4$): In this interval, the anti-parallel body diode D_{a1} of the auxiliary switch M_{a1} starts conducting and M_{a1} can be gated for ZVS turn on. Current through the series inductor i_{Ls1} is increasing with the slope of $[2/3\cdot(V_{in} + V_{Ca} - V_o/n)/L_s]$. Currents through the series inductors i_{Ls2} and i_{Ls3} are decreasing with the slope of $[-1/3\cdot(V_{in} + V_{Ca} - V_o/n)/L_s]$.

The currents through the series inductors, given by

$$i_{Ls1} = i_{Ls1}(t_3) + \frac{2}{3} \cdot \frac{V_{Ca} + V_{in} - (V_o/n)}{L_s} \cdot (t - t_3) \tag{2-23}$$

$$i_{Ls2} = i_{Ls2}(t_3) - \frac{1}{3} \cdot \frac{V_{Ca} + V_{in} - (V_o/n)}{L_s} \cdot (t - t_3) \tag{2-24}$$

$$i_{Ls3} = i_{Ls3}(t_3) - \frac{1}{3} \cdot \frac{V_{Ca} + V_{in} - (V_o/n)}{L_s} \cdot (t - t_3) \tag{2-25}$$

Currents through the parallel inductors are given by

$$i_{Lp1} = i_{Lp1}(t_3) + \frac{V_o}{L_p} \cdot (t - t_3) \tag{2-26}$$

$$i_{Lp2} = -\frac{I_{Lp,peak}}{2} \tag{2-27}$$

$$i_{Lp3} = i_{Lp3}(t_3) - \frac{V_o}{L_p} \cdot (t - t_3) \tag{2-28}$$

Current through main switches M_2 and M_3 are given by

$$i_{M2} = i_{M2}(t_3) + \frac{1}{3} \cdot \frac{V_{Ca} + V_{in} - (V_o / n)}{L_s} \cdot (t - t_3) \tag{2-29}$$

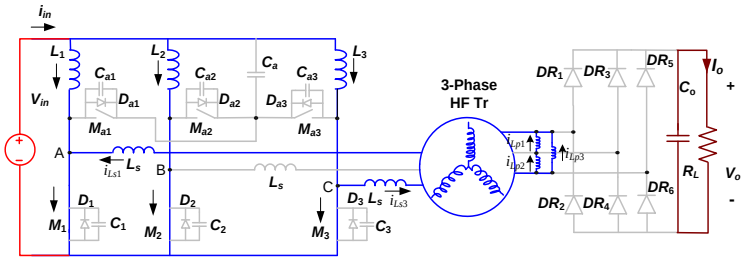
$$i_{M3} = i_{M3}(t_3) + \frac{1}{3} \cdot \frac{V_{Ca} + V_{in} - (V_o / n)}{L_s} \cdot (t - t_3) \tag{2-30}$$

Current through the auxiliary capacitor during this interval is decreasing and is given by

$$i_{Ca} = I_{Ca,peak} - \frac{2}{3} \cdot \frac{V_{Ca} + V_{in} - \frac{V_o}{n}}{L_s} \cdot (t - t_3) \tag{2-31}$$

At the end of this interval, i.e., $t = t_4$, i_{Ca} reaches zero. Final values are: $i_{Ls1}(t_4) = I_{in}/3$, $i_{Ls2}(t_4) = -I'_{Lp,peak}/2 - I_{in}/6$, $i_{Ls3}(t_4) = I'_{Lp,peak}/2 - I_{in}/6$; $i_{M2}(t_4) = I'_{Lp,peak}/2 + I_{in}/2$, $i_{M3}(t_4) = -I'_{Lp,peak}/2 + I_{in}/2$. $i_{Ca}(t_4) = 0$;

Interval 5 (Fig. 2.20e; $t_4 < t < t_5$): In this interval, the series inductor current i_{Ls1} increases above $I_{in}/3$ with the same slope as interval 4. The auxiliary capacitor current i_{Ca} decreases linearly (negative direction). The currents through the parallel inductors are increasing or decreasing with the same slope as interval 4.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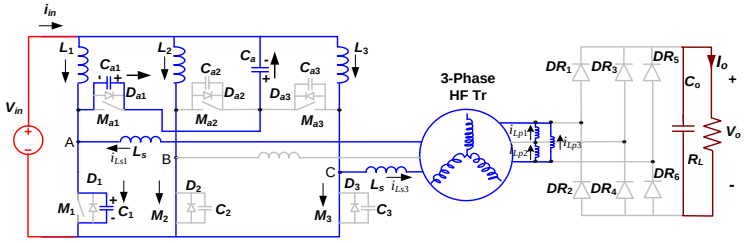
(a)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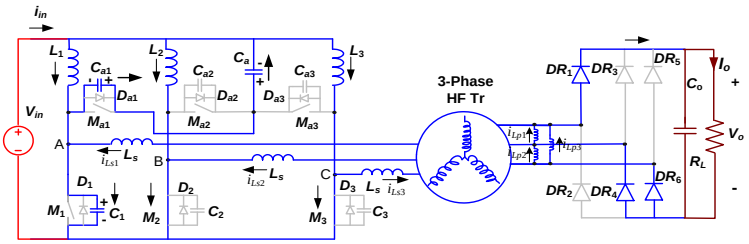
(b)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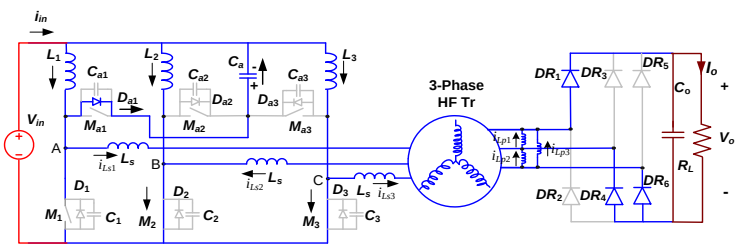
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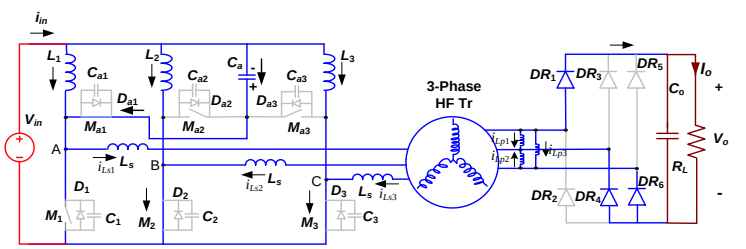
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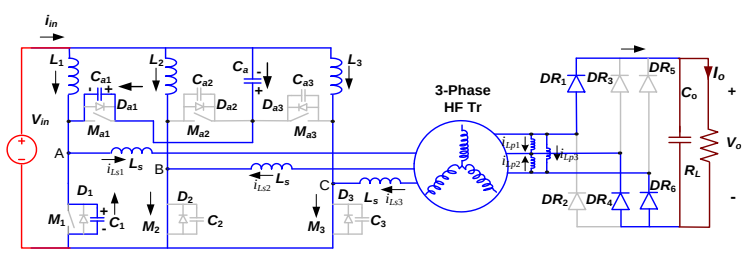
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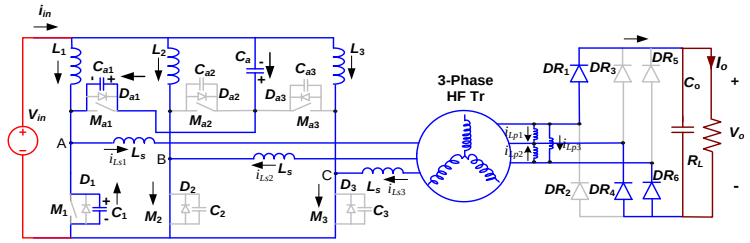

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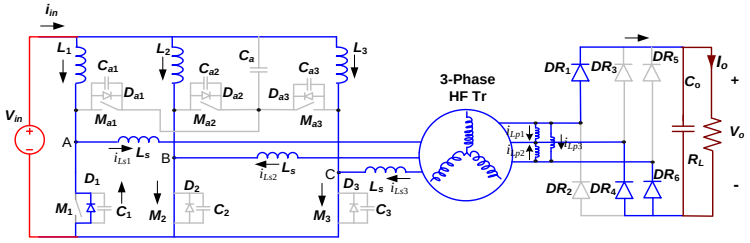

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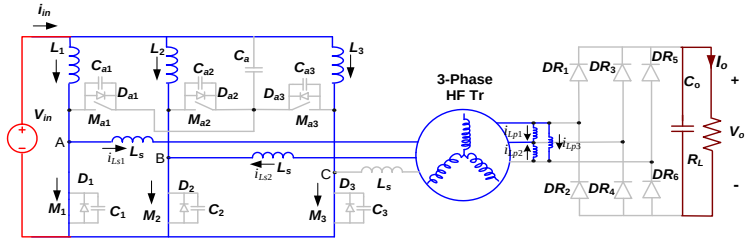


(i)

Fig. 2.20. Equivalent circuits during different intervals of operation of the proposed converter.

At the end of this interval, i.e., $t = t_5$, i_{Ca} reaches negative peak $I_{Ca,peak}$. Final values are: $i_{Ls1}(t_5) = I_{in}/3+I_{Ca,peak} \cong 2I_{in}/3 + I'_{Lp,peak}$, $i_{Ls2}(t_5) = -I_{in}/3-I'_{Lp,peak}$, $i_{Ls3}(t_5) = -I_{in}/3$; $i_{M2}(t_5) = 2I_{in}/3 + I'_{Lp,peak}$, $i_{M3}(t_5)=2 I_{in}/3$, $i_{Ca}(t_5)= -I_{Ca,peak}$;

Interval 6 (Fig. 2.20f; $t_5 < t < t_6$): The auxiliary switch M_{a1} is turned off at $t = t_5$. The series inductor current i_{Ls1} charges C_{a1} and discharges C_1. The series inductor L_{s1} resonates with snubber capacitors C_{a1} and C_1. This period is very small and the series inductor current increases very little in this interval. The resonant frequency is given by

$$\omega_r = \frac{1}{\sqrt{L_{s1}\cdot(C_1 + C_{a1})}} \qquad (2\text{-}32)$$

Voltage across the capacitor C_1 or switch M_1 is given by

$$v_{M1} = (V_{Ca} + V_{in}) - v_{Ma1} \tag{2-33}$$

where voltage across the switch M_{a1} (or capacitor C_{a1}) is given by

$$v_{Ma1} = (\frac{I_{in}}{3} + I'_{Lp,peak}) \cdot \sqrt{\frac{L_{s1}}{(C_1 + C_{a1})}} \cdot \sin(\omega_r \cdot (t - t_5)) \tag{2-34}$$

$$i_{Ls1} = (\frac{2I_{in}}{3} + I'_{Lp,peak}) \cdot \cos(\omega_r \cdot (t - t_5)) \tag{2-35}$$

Main switch currents are given by

$$i_{M2} = \left(\frac{2I_{in}}{3} + I'_{Lp,peak}\right) \cdot \cos(\omega_r \cdot (t - t_5)) \tag{2-36}$$

$$i_{M3} = \left(\frac{2I_{in}}{3}\right) \cdot \cos(\omega_r \cdot (t - t_5)) \tag{2-37}$$

At the end of this interval, C_1 discharges to V_o/n and C_{a1} charges to ($V_{Ca} + V_{in} - V_o/n$). Final values are (ignoring small current rise in this interval): $v_{Ma1}(t_6) = V_{Ca} + V_{in} - V_o/n$; $v_{M1}(t_6) = V_o/n$; $i_{Ls1}(t_6) = I_{in}/3 + I_{Ca,peak} \cong 2I_{in}/3 + I'_{Lp,peak}$, $i_{Ls2}(t_6) = -I_{in}/3 - I'_{Lp,peak}$, $i_{Ls3}(t_6) = -I_{in}/3$; $i_{M2}(t_6) = 2I_{in}/3 + I'_{Lp,peak}$, $i_{M2}(t_6) = 2\, I_{in}/3$.

Interval 7 (Fig. 2.20g; $t_6 < t < t_7$): The current i_{Ls1} is still charging C_{a1} and discharging C_1 in a resonant fashion. This period is also very small and the series inductor current decreases very little in this interval. The resonant frequency is given by (2-32). At the end of this interval, the capacitor C_1 discharges completely to zero and capacitor C_{a1} charges to its initial value. Final values are: $v_{M1}(t_7) = 0$; $v_{Ma1}(t_7) = V_{Ca} + V_{in}$.

Interval 8 (Fig. 2.20h; $t_7 < t < t_8$): In this interval, anti-parallel body diode D_1 of main switch M_1 starts conducting and now M_1 can be gated for ZVS turn-on. The series inductor current i_{Ls1} decreases with a negative slope

of $[2/3 \cdot V_o/(n \cdot L_{s1})]$. The series inductor currents i_{Ls2} and i_{Ls3} increase with a positive slope of $[1/3 \cdot V_o/(n \cdot L_{s1})]$.

$$i_{Ls1} = i_{Ls1}(t_7) - \frac{2}{3} \cdot \frac{V_o}{n \cdot L_{s1}} \cdot (t - t_7) \tag{2-38}$$

$$i_{Ls2} = i_{Ls2}(t_7) + \frac{1}{3} \cdot \frac{V_o}{n \cdot L_{s2}} \cdot (t - t_7) \tag{2-39}$$

$$i_{Ls3} = i_{Ls3}(t_7) + \frac{1}{3} \cdot \frac{V_o}{n \cdot L_{s3}} \cdot (t - t_7) \tag{2-40}$$

This interval ends when the series inductor current i_{Ls1} reaches $I_{in}/3$. Final values are: $i_{Ls1}(t_8) = I_{in}/3$, $i_{Ls2}(t_8) = -I_{in}/6 - I'_{Lp,peak}/2$, $i_{Ls1}(t_8) = -I_{in}/6 + I'_{Lp,peak}/2$.

Interval 9 (Fig. 2.20i; $t_8 < t < t_9$): Switch M_1 turns on with ZVS. The current through the switch M_1 starts increasing. The series inductor current decreases with the same slope and is being transferred to switch M_1. The interval ends when the series inductor current i_{Ls1} equals to parallel inductor current $I'_{Lp,peak}$ and switch M_1 current reaches to $I_{in}/3 - I'_{Lp,peak}$.

$$i_{Ls1} = \frac{I_{in}}{3} - \frac{2}{3} \cdot \frac{V_o}{n \cdot L_{s1}} \cdot (t - t_8) \tag{2-41}$$

$$i_{Ls2} = -\frac{I_{in}}{6} - \frac{I'_{Lp,peak}}{2} + \frac{1}{3} \cdot \frac{V_o}{n \cdot L_{s2}} \cdot (t - t_8) \tag{2-42}$$

$$i_{Ls3} = -\frac{I_{in}}{6} + \frac{I'_{Lp,peak}}{2} + \frac{1}{3} \cdot \frac{V_o}{n \cdot L_{s3}} \cdot (t - t_8) \tag{2-43}$$

$$i_{M1} = \frac{2}{3} \cdot \frac{V_o}{n \cdot L_{s1}} \cdot (t - t_8) \tag{2-44}$$

$$i_{M2} = \frac{I_{in}}{2} + \frac{I'_{Lp,peak}}{2} - \frac{1}{3} \cdot \frac{V_o}{n \cdot L_{s2}} \cdot (t - t_8) \tag{2-45}$$

$$i_{M3} = \frac{I_{in}}{2} - \frac{I'_{Lp,peak}}{2} - \frac{1}{3} \cdot \frac{V_o}{n \cdot L_{s3}} \cdot (t - t_8) \qquad (2\text{-}46)$$

Final values are: $i_{Ls1}(t_9) = I'_{Lp,peak}$, $i_{Ls2}(t_9) = -I'_{Lp,peak}$, $i_{Ls3}(t_9) = 0$; $i_{M1}(t_9) = I_{in}/3 - I'_{Lp,peak}$; $i_{M2}(t_9) = I_{in}/3 + I'_{Lp,peak}$; $i_{M3}(t_9) = I_{in}/3$; $i_{Lp1}'(t_9) = I'_{Lp,peak}$, $i_{Lp2}'(t_9) = -1/2 \cdot I'_{Lp,peak}$, $i_{Lp3}'(t_9) = -1/2\ I'_{Lp,peak}$.

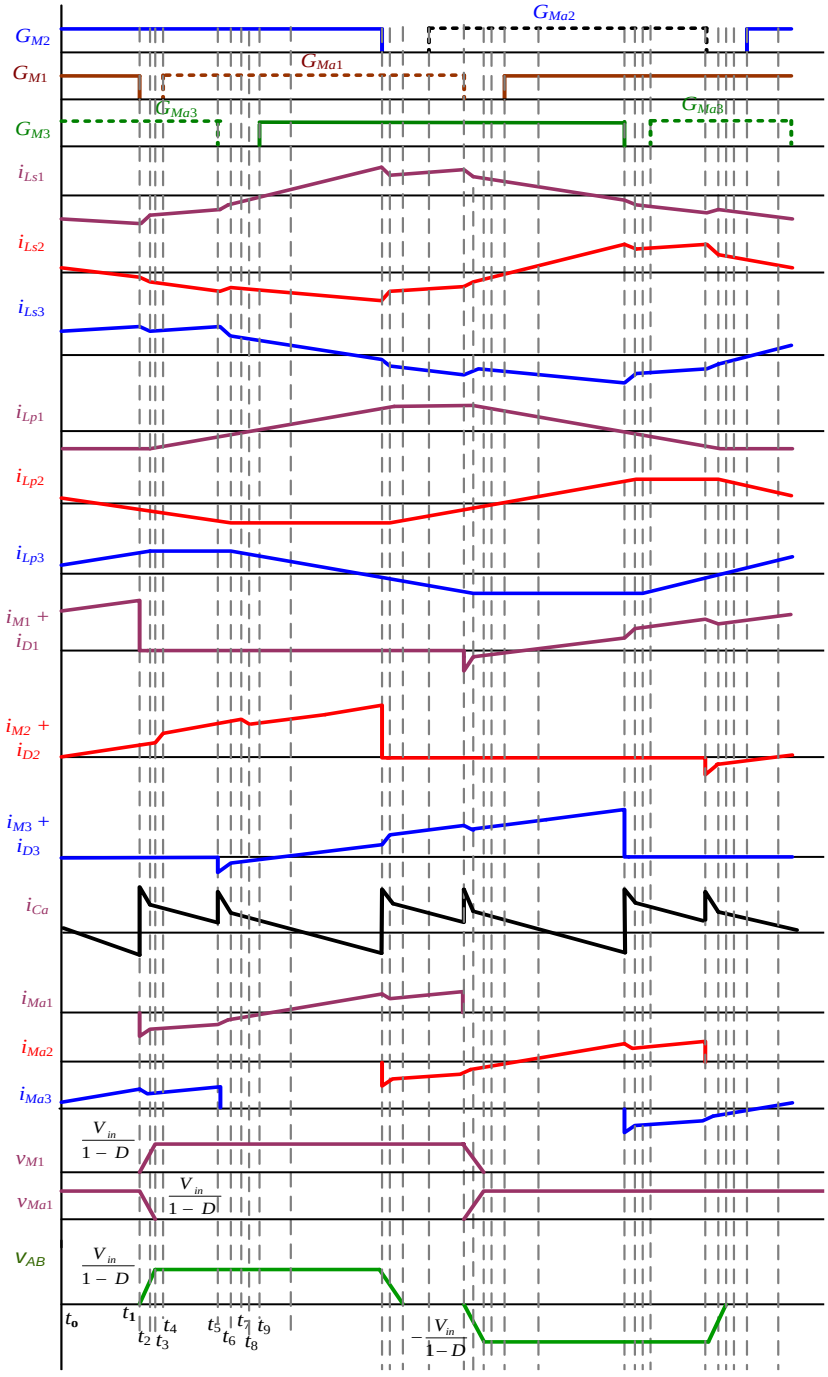


Fig. 2.21 Operating waveforms of the proposed converter in continuous auxiliary clamp capacitor current case (case B).

Table 2.2: Turn-on devices during different intervals of case B

Interval	Turn-on devices
t_0-t_1	M_1 M_2 M_{a3} DR_2 DR_4 DR_5
t_1-t_2	M_2 M_{a3} DR_2 DR_4 DR_5
t_2-t_3	M_2 M_{a3} DR_4 DR_5
t_3-t_4	M_2 M_{a3} DR_1 DR_4 DR_5
t_4-t_5	M_{a1} M_2 M_{a3} DR_1 DR_4 DR_5
t_6-t_7	M_{a1} M_2 D_3 DR_1 DR_4 DR_5
t_7-t_8	M_{a1} M_2 D_3 DR_1 DR_4
t_8-t_9	M_{a1} M_2 D_3 DR_1 DR_4 DR_6

2.5.2 Continuous Auxiliary Clamp Capacitor Current

This condition arises when source/input voltage is high. In this case, duty cycle of the main switches is less than 0.66 (D < 0.66) and at least one main switch is off at a time or all three main device cannot be conducting simultaneously. The steady-state operating waveforms are shown in Fig. 2.21. Here we just provide conducting devices during different intervals in a one third cycle of HF cycle in Table 2-2. For the rest of the cycle, the intervals are repeated in the same sequence with other symmetrical devices conducting to complete the full HF cycle.

2.6 Design of the Converter

In this Section, converter design procedure is illustrated by a design example for the following specifications: input voltage V_{in} = 22 V to 41 V, output voltage V_o = 350 V, output power P_o = 300W, minimum load = 10% (30 W), switching frequency f_s = 100 kHz.

(1) Average input current is $I_{in} = P_o/(V_{in})$. Assuming an ideal efficiency of 100%, I_{in} = 13.6 A.

(2) D_{max} is selected at minimum input voltage, i.e., V_{in} = 22 V and full load based on maximum switch voltage rating $V_{SW(max)}$ using

$$D_{max} = 1\text{-}\ (V_{in}/V_{SW(max)}) \tag{2-47}$$

For $V_{SW(max)}$ = 110 V, D_{max} = 0.8.

(3) Inductor values L_s and L_p: Inductor value L_s is selected at minimum input voltage and full load condition using

$$L_s = \frac{R_L}{f_s}\left[\frac{(V_{in}/V_o)^2}{(1+L_s/L_p')} - \frac{(V_{in}/V_o)\cdot(1\text{-}D_{\max})}{n}\right] \tag{2-48}$$

Selecting the inductance values for a certain rated power P_o and switching frequency f_s depends upon the transformer turns ratio n, inductor ratio L_p'/L_s and the maximum duty cycle D_{max} at full load chosen earlier.

Now the transformer turns ratio $n = N_s/N_p$, is selected to maintain $D > 0.5$, i.e., voltage regulation with load and input voltage variation given by

$$D = 1 - \frac{n\cdot V_o}{V_{in}}\left[\frac{(V_{in}/V_o)^2}{(1+L_s/L_p')} - \frac{L_s\cdot f_s}{R_L}\right] \tag{2-49}$$

and realizable value of L_s including transformer leakage given by (2-48). Also, n should be such that L_s is positive, using (2-48)

$$n > (1\text{-}D_{\max})\cdot\frac{V_o}{V_{in}}\cdot(1+L_s/L_p') \tag{2-50}$$

Therefore, minimum value of n = 3.5 for L_p'/L_s = 10.

Inductor ratio L_p'/L_s is selected based on the ZVS range, given by (2-51) and main switch RMS current given by (2-52), which should be low for high converter efficiency.

$$I_{in,critical} \geq \frac{3}{2}\cdot\sqrt{\frac{\left[\frac{t_f\cdot\left(I_{in,FL}/3+I'_{Lp,peak}\right)}{\left(\frac{V_{in}}{1-D_{FL}}\right)}\right]_{FL}\cdot\left[\left(\frac{V_{in}}{1-D_{RL}}\right)^2\right]_{RL}}{L_s}}-\frac{3}{2}\cdot I'_{Lp,peak} \tag{2-51}$$

Here, t_f is fall time of the switches during turn-off (higher value is taken between fall times of main and auxiliary switches). Subscripts "*FL*" and "*RL*" denotes full load and reduced load conditions.

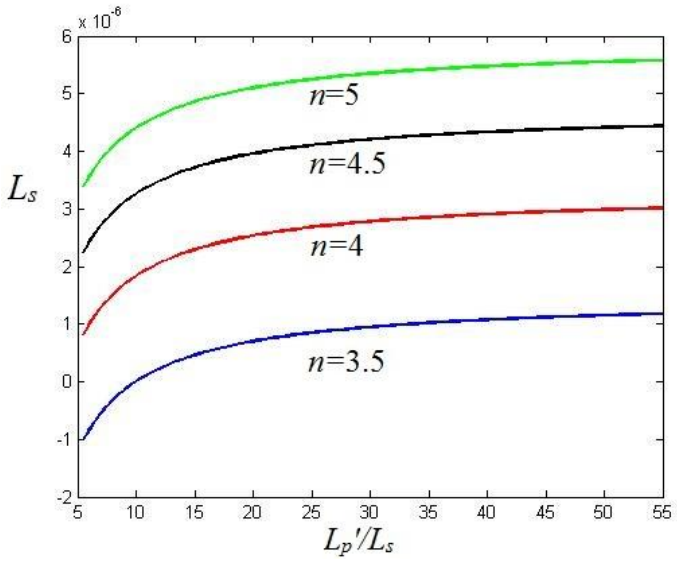
$$I_{sw,rms}=\sqrt{(I'_{Lp,peak})^2\cdot\left(\frac{4}{3}D-\frac{2}{3}\right)+I_{in}^2\cdot\left(\frac{2}{27}+\frac{D}{27}+\frac{2}{9}\cdot\frac{T_{DR}}{T_s}\right)+I_{in}\cdot I'_{Lp,peak}\cdot\left(\frac{8}{9}\cdot(D-1)+\frac{T_{DR}}{T_s}\right)} \tag{2-52}$$

Here T_{DR} is rectifier diode conduction time given by

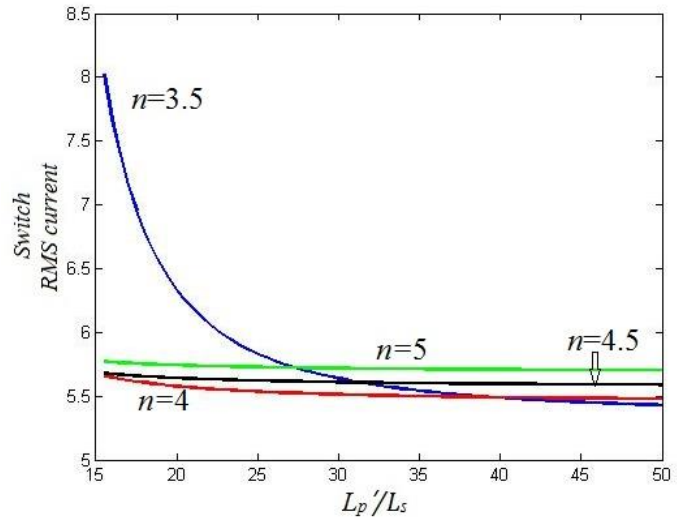
$$T_{DR}=\frac{n\cdot V_{in}}{V_o\cdot f_s\left(1+\frac{L_s}{L_p'}\right)} \tag{2-53}$$

Fig. 2.22(a) shows the calculated values of L_s with respect to inductor ratio L_p'/L_s for four values of turns ratio n. Fig. 2.22(a) illustrates that for a higher turns ratio, value of L_s is higher which corresponds to higher ZVS range. However, from Fig. 2.22 (b), higher turns ratio increases the peak and RMS currents through the switches, leading to low converter efficiency. So it is necessary to set a tradeoff between ZVS range and efficiency. Turns ratio n=4 gives an acceptable choice. From Fig. 2.22 (b), for a given n, switch RMS current decreases as the ratio L_p'/L_s increases. For the selected value of n =4, reduction in RMS current is negligible for L_p'/L_s > 15. Therefore, an inductor ratio of L_p'/L_s = 15 is selected.

From the above discussions, using D_{max} = 0.8, n = 4 and L_p'/L_s = 15, calculated values are L_s = 2μH, L_p' =30 μH or L_p = 480 μH. If transformer magnetizing inductance L_m (secondary-side), is higher than the design value of



(a)



(b)

Fig. 2.22. Variation of (a) value of series inductance L_s (H), and (b) switch RMS current (A), with respect to inductor ratio L_p'/L_s for various transformer turns ratio n.

L_p, then an external inductor is connected in parallel on secondary side of the transformer, and its value is given by

$$L_{p,ex} = \frac{L_m}{\left(\frac{L_m}{L_p} - 1\right)} \tag{2-54}$$

(4) Values of boost inductors are given by

$$L_1 = L_2 = L_3 = (V_{in})(D)/[(\Delta I_{in})(f_s)] \tag{2-55}$$

where ΔI_{in} is the boost inductor ripple current. For ΔI_{in} = 0.5 A, $L_1 = L_2$, L_3 =352 μH. Maximum voltage across the inductors = V_{Ca} = 88 V, given by (2-5).

(5) Inductors' ratings: The RMS current through the series and parallel inductors, are

$$I_{Ls,rms} = \sqrt{(I'_{Lp,peak})^2 \cdot \left(D - \frac{1}{3}\right) + I_{in}^2 \cdot \left(\frac{2}{9} \cdot \frac{T_{DR}}{T_s}\right) + I_{in} \cdot I'_{Lp,peak} \cdot \left(\frac{2}{3} \cdot (D-1) + \frac{T_{DR}}{T_s}\right)} \tag{2-56}$$

$$I_{Lp,rms} = \frac{2}{3} \cdot \frac{I'_{Lp,peak}}{n} \cdot \left(\frac{1}{2} - \frac{3}{4} \cdot \frac{T_{DR}}{T_s}\right)^{1/2} \tag{2-57}$$

Using (2-2), $I'_{Lp,peak}$ = 2.29A. $I_{Lp,rms}$ is calculated to be 0.22A. Peak current through the parallel inductor $I_{Lp,peak} = I'_{Lp,peak} \cdot 2/(3 \cdot n)$ = 0.38 A. Using (2-53) and (2-56), $I_{Ls,rms}$ = 3.96A. Peak current through L_s is, $I_{Ls,peak} = 2 \cdot I_{in}/3 + I'_{Lp,peak}$ = 11.36 A. Maximum voltage across $L_s = 2 \cdot V_o/(3 \cdot n)$ = 58.3 V. Maximum voltage across $L_p = V_o$= 350 V.

(6) Switch current ratings: RMS current through the main switches $I_{sw,rms}$ can be calculated by (2-52). RMS current through the auxiliary switches is given by

$$I_{auxsw,rms} = \left(I_{in} + 3I'_{Lp,peak}\right) \cdot \left[(1-D)/27\right]^{1/2} \tag{2-58}$$

The values of $I_{sw,rms}$ and $I_{aux,rms}$ are calculated to be 5.75A and 1.76 A respectively. Peak currents through main switches $I_{sw,peak} = 2I_{in}/3 + I'_{Lp,peak}$ = 11.36A and auxiliary switches $I_{aux,peak} = I_{in}/3 + I'_{Lp,peak}$ = 6.82 A.

(7) Auxiliary capacitor: substituting in (2-5), V_{in} = 22 V and D = 0.8, V_{Ca} = 88 V. The value of auxiliary capacitor C_a is

$$C_a = \frac{I_{Ca,peak} \cdot \sqrt{(1-D)}}{6 \cdot \pi \cdot f_s \cdot \Delta V_{Ca}} \tag{2-59}$$

Peak current through C_a is $I_{Ca,peak} = I_{in}/3 + I'_{Lp,peak}$ = 6.82 A. For a ripple voltage of ΔV_{Ca} = 2 V, $C_a \cong$ 0.81 μF.

RMS current through auxiliary capacitor is

$$I_{Ca,rms} = I_{Ca,peak} \cdot \sqrt{((1-D))} \tag{2-60}$$

Here, $I_{Ca,\text{rms}}$ = 3.05A. Auxiliary capacitor carries a current of 300 kHz (triple the switching frequency).

(8) Output rectifier diodes: Average rectifier diode current is given by

$$I_{DR,avg} = P_o/(3V_o) \tag{2-61}$$

Here, $I_{DR,avg} \cong 0.29$ A. Voltage rating of rectifier diodes, $V_{DR} = V_o = 350$ V.

(9) Output capacitor: Value of output filter capacitor C_o is

$$C_o = \frac{(I_0)\cdot\left(\frac{T_s}{3} - T_{DR}\right)}{\Delta V_o} \tag{2-62}$$

ΔV_o = Allowable ripple in output voltage. $C_o = 1\mu$F for $\Delta V_o = 0.75$ V. Its voltage rating is, $V_o = 350$ V.

(10) Snubber design: The equation for the calculation of snubber capacitors is given by

$$(C_1 + C_{a1}) = \frac{t_f \cdot \left(\frac{I_{in}}{3} + I'_{Lp,peak}\right)}{\left(\frac{V_{in}}{1-D}\right)} \tag{2-63}$$

Here, t_f = fall time of the switches during turn-off. $C_1 = C_{oss,M1}$; $C_{a1} = (C_1+C_{a1}) - C_{oss,M1}$.

For the selected main and auxiliary switches IRFB4127PbF (V_{ds} = 200 V, I_D =76 A, R_{dson} = 20 mΩ, C_{oss} = 410 pF, t_f = 22 ns), the calculated values of snubber capacitors are C_1 = 0.410 nF, C_{a1} = 0.545 nF. Snubber capacitors' voltage rating is equal to switch voltage rating, given by (2-6) or (2-47) and is = 110 V.

Table 2.3: Comparison of components' ratings.

Components	Items	Single-phase (two-inductor) converter	Three-phase Converter
Main switches	V_{pk}	110V	110V
	I_{peak}	21.48A	11.36A
	I_{rms}	9.29A	5.75A
Auxiliary switches	V_{pk}	110V	110V
	I_{peak}	7.88A	6.82A
	I_{rms}	2.03A	1.76A
Clamp capacitor	Capacitance	1.4μF	0.8μF
	V_{pk}	88V	88V
	I_{peak}	7.88A	6.82A
	I_{rms}	2.88A	3.05A
Output Capacitor	Capacitance	3μF	1μF
	V_{pk}	350V	350V
Diode	I_{avg}	0.43A	0.29A
	V_{pk}	350V	350V
Boost Inductor	Inductance	352μH	352μH
	I_{avg}	6.8A	4.5A

(11) ZVS Conditions: (A) To achieve ZVS of the auxiliary switches, in interval 2, the dead-gap between the main switch gating signal G_{M1} and auxiliary switch gating signal G_{Ma1} should be of sufficient duration to allow charging and discharging of the snubber capacitors C_1 and C_{a1}, respectively, by the boost inductor current $I_{in}/3$. The value is given by

$$T_{dg1} = \frac{(C_1 + C_{a1}) \cdot \left(\frac{V_{in}}{1-D} \right)}{I_{in}/3 + I'_{Lp,peak}} \tag{2-64}$$

(B) For ZVS of the main switches, in interval 5 the charging and discharging of the snubber capacitors C_{a1} and C_1 should be done by the series inductor current in a quarter of the resonant period and is equal to the dead-gap between the auxiliary switch gating signal G_{Ma1} and main switch gating signal G_{M1} and is given by

$$T_{dg2} = \frac{\pi}{2}\sqrt{L_s \cdot (C_1 + C_{a1})} \tag{2-65}$$

T_{dg1} = 22 ns and T_{dg2} = 82 ns. Identical dead-gaps $T_{dg1} = T_{dg2}$ = 82 ns is provided between the main and auxiliary gating signals.

(C) To achieve ZVS of the main switches, the energy stored in the series inductor L_s must be sufficient to charge C_{a1} and discharge C_1. It gives.

$$L_s \cdot I_{Ls,peak}^{\ 2} \geq (C_1 + C_{a1}) \cdot (\frac{V_{in}}{1-D})^2 + C_a \Delta V_{Ca}^{\ 2} \tag{2-66}$$

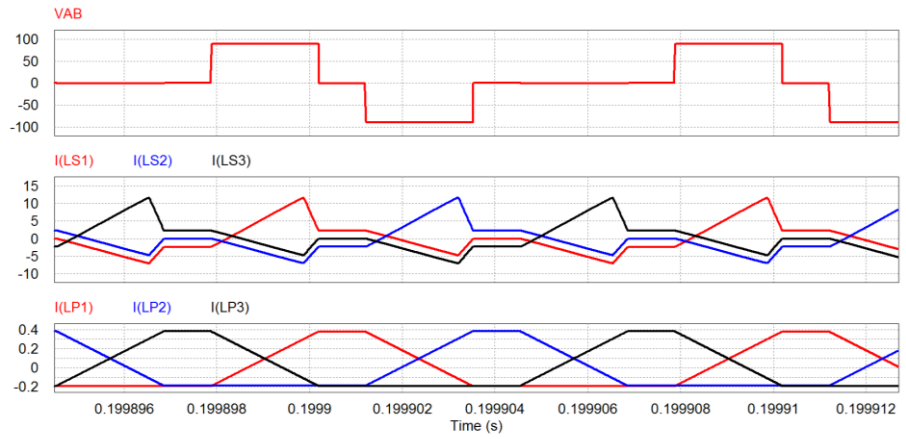
A comparison of components' ratings between the proposed three-phase converter and the single-phase converter [118] for similar specifications is shown in Table 2-3. Peak currents through the main and auxiliary switches in proposed converter are obviously reduced, which alleviates the peak current stress of switching devices. Since input current is being shared among three phases, RMS currents through the active components (main and auxiliary switches) and passive components are also reduced. This will bring a reduction in the conduction losses in switches and size of passive components.

2.7 Simulation and Experimental Results

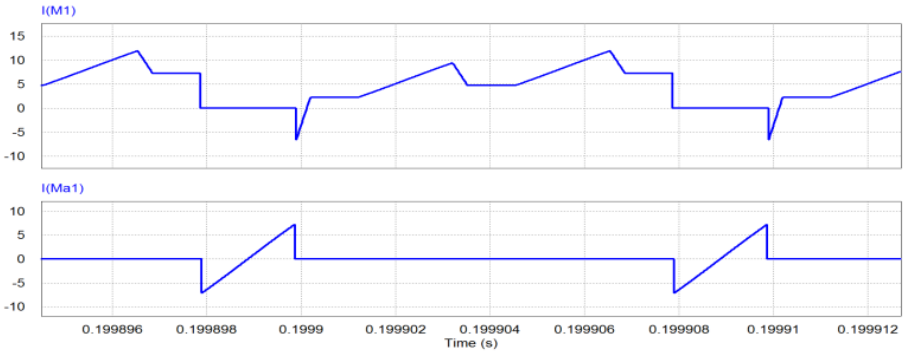
The proposed converter is designed for 300W and was first simulated using PSIM 9.0.4 to verify the proposed converter analysis and design. Later, an experimental converter prototype was developed in the research lab to test and demonstrate the converter performance for wide variations in source voltage and output power values. To obtain the simulation results, simulation is run for several HF cycles until the state variables reach a steady-state. Device capacitances and passive snubbers across the devices are included in

the simulation to acquire waveforms which are closer to practical converter system.

Simulation results for two extreme operating conditions of V_{in} = 22 V at full load and *Vin* = 41 V at 10% load are presented in Fig. 2.23 and Fig. 2.24, respectively. Current waveforms through three series and parallel inductors are illustrated in Figs. 2.23 (a) and 2.24(a) and are phase-shifted with each other by 120 °. Voltage waveform across the transformer phases v_{AB} is also shown. Compared to lower voltage (22V) (Fig. 2.23), the duty cycle value is lower at high voltage (41V) (Fig. 2.24). Therefore, v_{AB} lasts for longer time i.e., 1-*D* (main switch off duration). It causes an increase in peak value of magnetizing

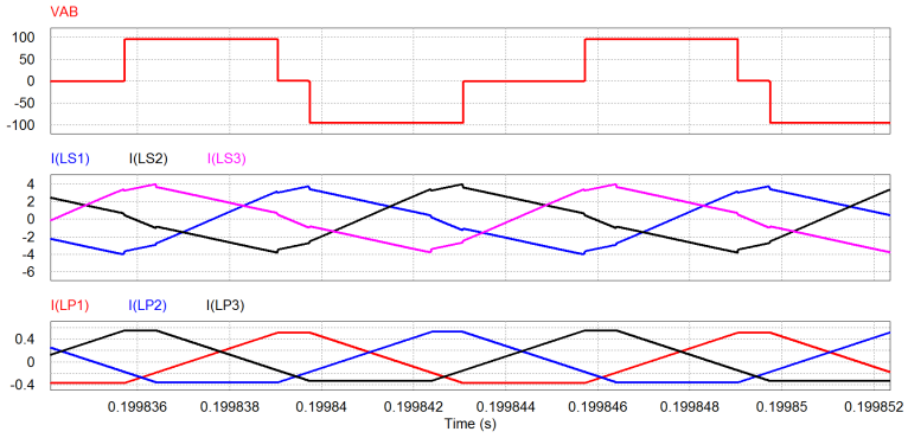


(a)

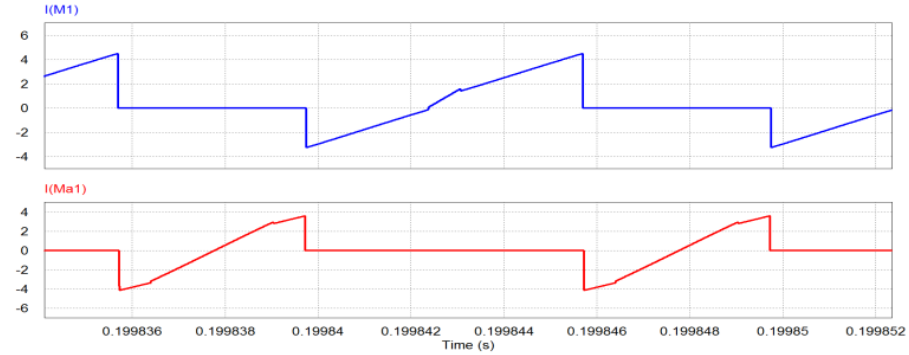


(b)

Fig. 2.23. Simulation waveforms at V_{in} = 22 V and full load: (a) voltage v_{AB}, series inductor currents i_{Ls1}, i_{Ls2} and i_{Ls3}, and parallel inductor currents i_{Lp1} i_{Lp2} and i_{Lp3} (b) main switch M_1 current i_{M1}, auxiliary switch M_{a1} current i_{Ma1}.



(a)



(b)

Fig. 2.24. Simulation waveforms at V_{in} = 41 V and 10% load: (a) voltage v_{AB}, series inductor currents i_{Ls1}, i_{Ls2} and i_{Ls3}, and parallel inductor currents i_{Lp1} i_{Lp2} and i_{Lp3} (b) main switch M_1 current i_{M1}, auxiliary switch M_{a1} current i_{Ma1}.

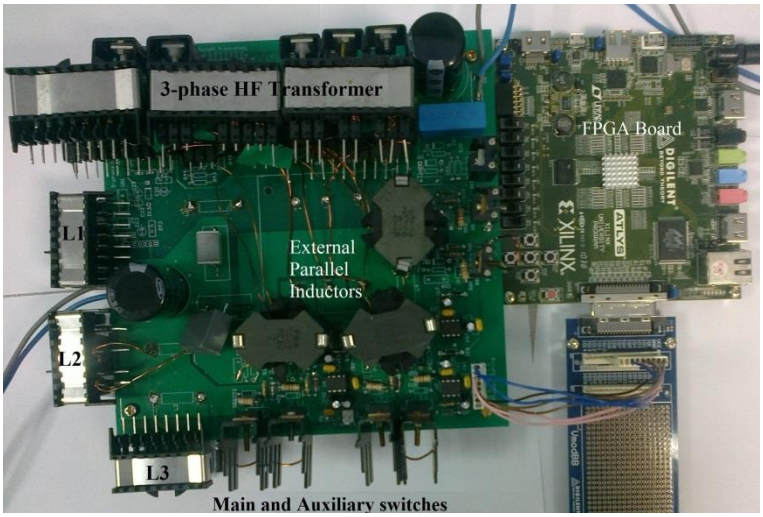


Fig. 2.25. 300 W laboratory prototype of current-fed three-phase DC/DC converter with active-clamp.

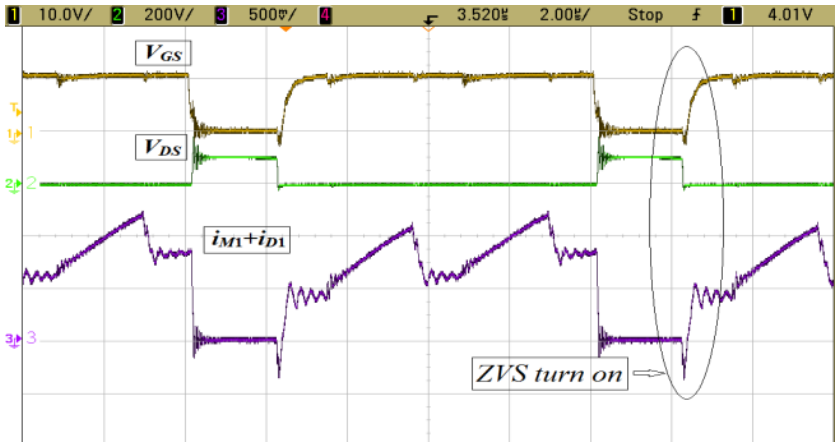
(parallel inductor) currents and consequently in peak value of series inductor currents. Higher value of peak current assures ZVS of main switches at high

input voltage and low power condition due to increased energy storage than conventional converter. As shown in part (b) of Figs. 2.23-2.24, the anti-parallel body diodes of switches (main and auxiliary) conduct prior to the conduction of their switches, which verifies ZVS turn-on of the switches.

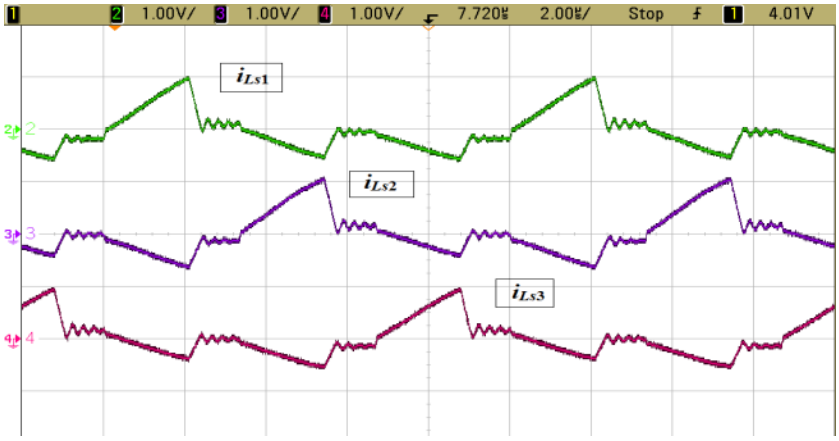
Photo of experimental 300 W converter prototype developed in research lab for the given specifications is shown in Fig. 2.25. The details of the experimental converter are as follows. IRFB4127PbF (main switches and auxiliary switches); IDD05SG60C (SiC Schottky rectifier diodes); HF transformer: PC47ETD49-Z ferrite core, primary turns = 7, secondary turns = 28, leakage inductance (reflected to primary side) = 2.1 μH, magnetizing inductance (secondary side) = 3.4mH; external parallel inductor: TDK5901PC40Z, = 458 μH; boost inductors: PC47ETD39-Z ferrite core, L_1 ~ L_3 = 450 μH. Gating signals for the switches have been generated using Spartan-3 FPGA board. IR2181 driver ICs are used for gating the MOSFETs.

Experimental results are shown in Figs. 2.26-2.29 for V_{in} = 22 and 41 V at rated load and 10% load. Experimental waveforms coincide with theoretical operating and simulation waveforms.

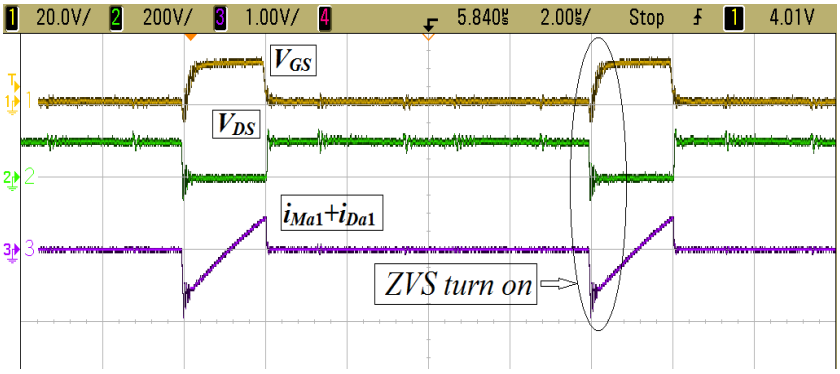
Waveforms of series inductors' currents of these four extreme operating conditions are illustrated by part (b) in Figs. 2.26-2.29 and are phase-shifted with each other by 120˚as expected due to such phase-shift pattern in gating signals of three main switches. Parts (a) and (c) of Figs. 2.26-2.29 clearly confirm the ZVS of main and auxiliary switches for all four different operating conditions. In waveforms shown in part (a) of Figs. 2.26-2.29, main switches are triggered (v_{GS}) after voltage across them (v_{DS}) reaches zero, i.e., device capacitance is fully discharged. On the other hand, anti-parallel body diode



(a)

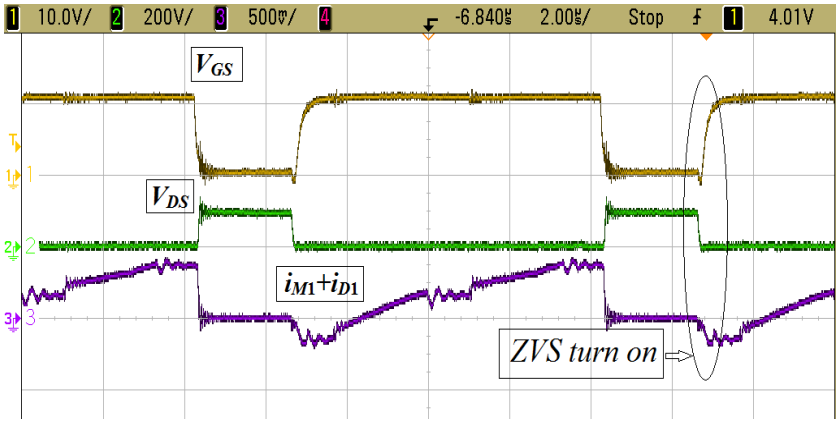


(b)



(c)

Fig. 2.26. Experimental waveforms at V_{in} = 22 V and full load (x-axis: 2 µs/div): (a) main switch gate voltage v_{GS} (10 V/div), voltage v_{DS} (200 V/div) and main switch current i_{M1}+ i_{D1} (5A/div), (b) series inductor currents i_{Ls1}, i_{Ls2} and i_{Ls3} (10 A/div), and (c) auxiliary switch gate voltage v_{GS} (20 V/div), voltage v_{DS} (200 V/div) and auxiliary switch current i_{Ma1}+ i_{Da1} (10A/div).



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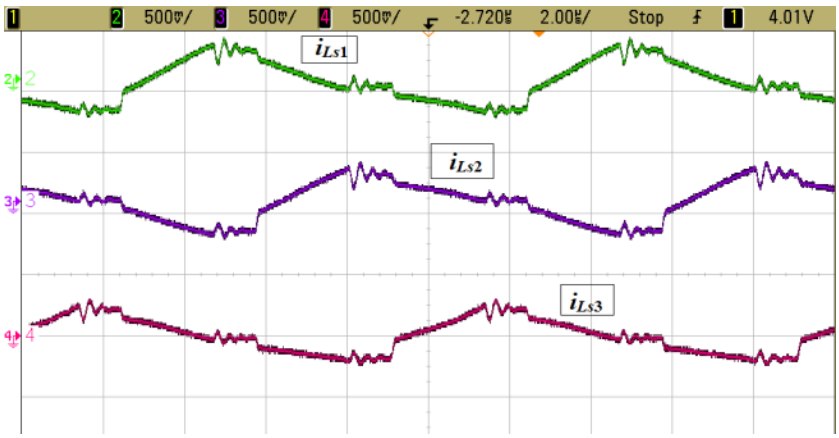

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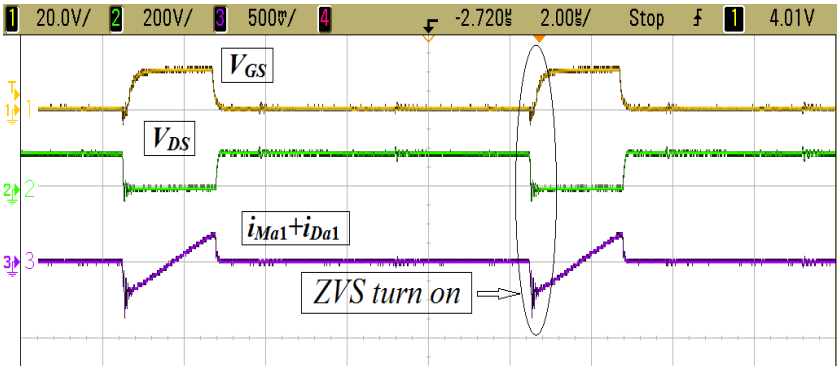

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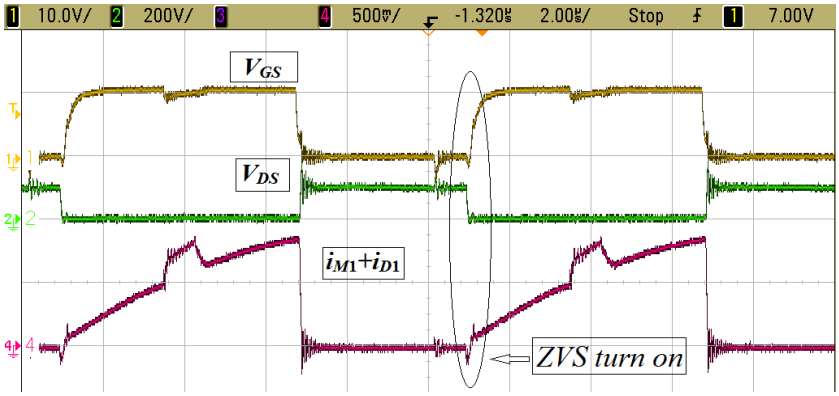
Fig. 2.27. Experimental waveforms at V_{in} = 22 V and 10% load (x-axis: 2 µs/div): (a) main switch gate voltage v_{GS} (20 V/div), voltage v_{DS} (200 V/div) and main switch current i_{M1}+ i_{D1} (5A/div), (b) series inductor currents i_{Ls1}, i_{Ls2} and i_{Ls3} (5 A/div), and (c) auxiliary switch gate voltage v_{GS} (20 V/div), voltage v_{DS} (200 V/div) and auxiliary switch current i_{Ma1}+ i_{Da1} (5A/div).



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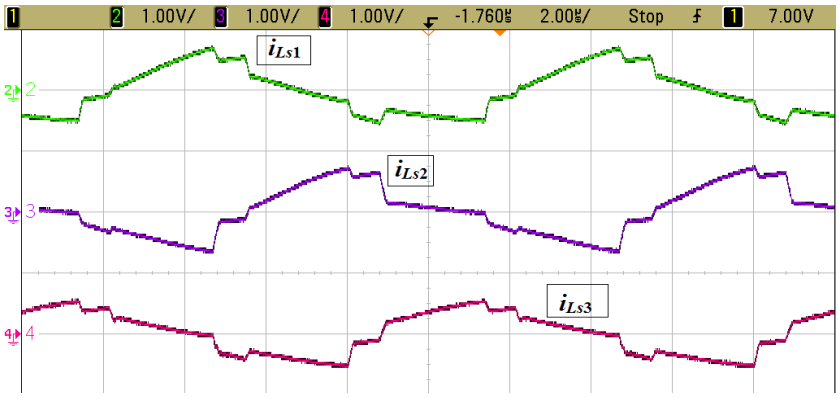

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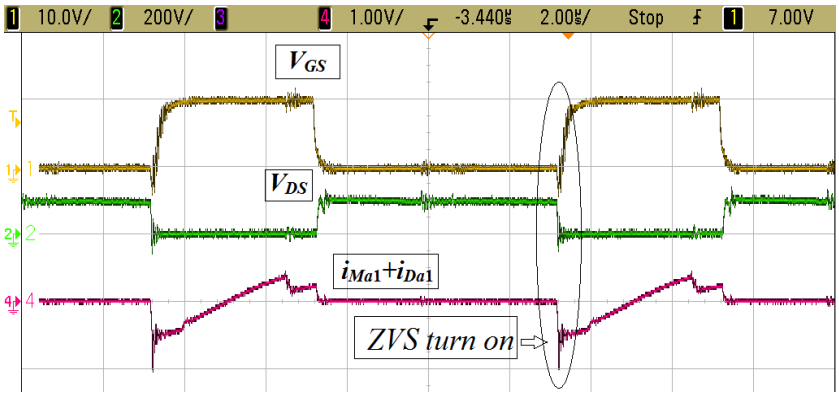
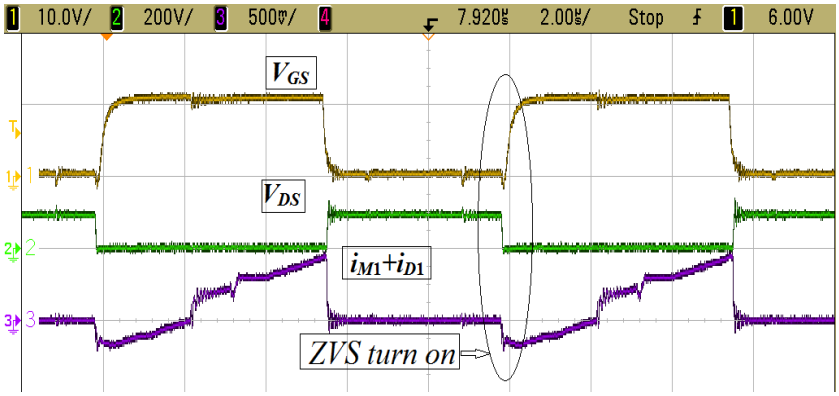


(c)

Fig. 2.28. Experimental waveforms at V_{in} = 41 V and full load (x-axis: 2 µs/div): (a) main switch gate voltage v_{GS} (10 V/div), voltage v_{DS} (200 V/div) and main switch current i_{M1}+ i_{D1} (5A/div), (b) series inductor currents i_{Ls1}, i_{Ls2} and i_{Ls3} (10A/div), and (c) auxiliary switch gate voltage v_{GS} (10 V/div), voltage v_{DS} (200 V/div) and auxiliary switch current i_{Ma1}+ i_{Da1} (10A/div).



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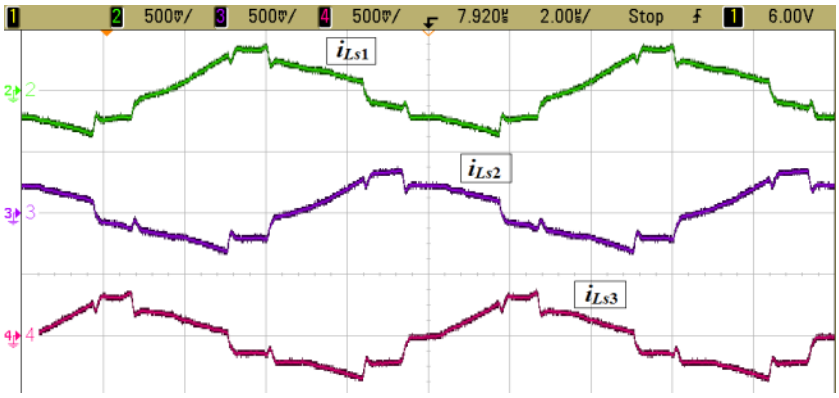

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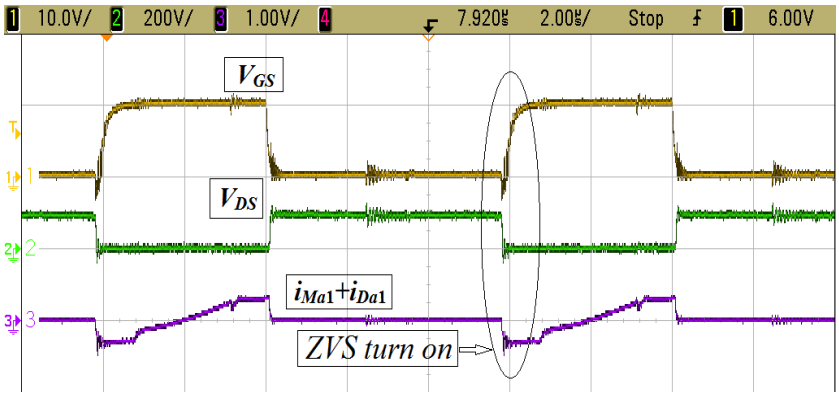


(c)

Fig. 2.29. Experimental waveforms at V_{in} = 41 V and 10% load (x-axis: 2 µs/div): (a) main switch gate voltage v_{GS} (10 V/div), voltage v_{DS} (200 V/div) and main switch current i_{M1}+ i_{D1} (5A/div), (b) series inductor currents i_{Ls1}, i_{Ls2} and i_{Ls3} (5 A/div), and (c) auxiliary switch gate voltage v_{GS} (10 V/div), voltage v_{DS} (200 V/div) and auxiliary switch current i_{Ma1}+ i_{Da1} (10A/div).

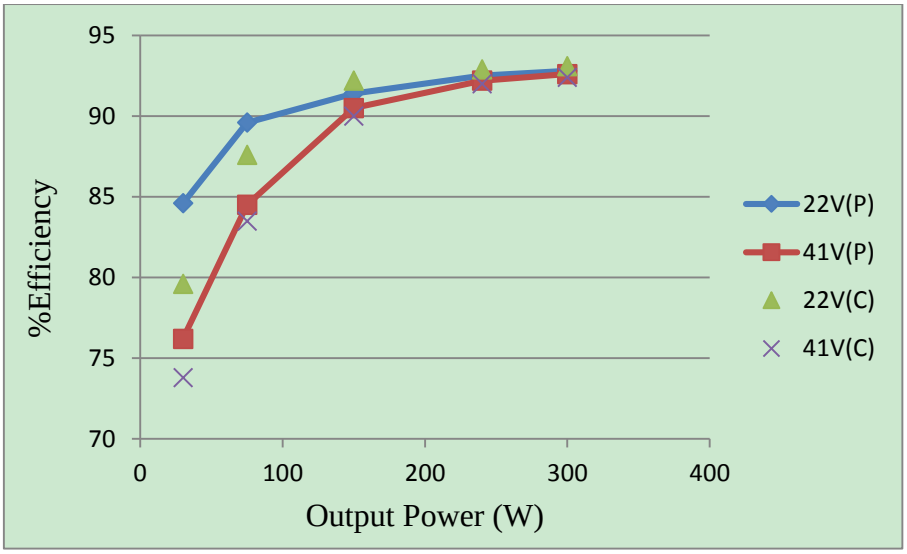


Fig. 2.30. Plot of efficiency versus output power for different load condition with V_{in} = 22 V and V_{in} = 41 V for the proposed converter (P) and conventional converter without external inductor (C).

conducts prior to its switch's conduction, confirming the ZVS turn on of main switches. Similarly, in part (c) of Figs. 2.26-2.29, auxiliary clamp circuit switches are triggered (v_{GS}) after voltage across them (v_{DS}) reaches zero, i.e., their snubber capacitances are fully discharged. Anti-parallel body diode of the auxiliary switches is conducting first causing zero voltage across the devices, before they start conducting current, resulting in ZVS turn-on of the auxiliary switches. Therefore, it is clear from the given experimental results that all the converter devices maintains soft-switching under wide range of the source or input voltage and output power variation. The converter does not lose ZVS and thus the proposed design achieves the objective.

Fig. 2.30 shows measured efficiency for different load at V_{in} = 22 V and V_{in} = 41 V for the proposed design and the developed laboratory prototype. While maintaining ZVS, converter is able to achieve 93% efficiency at rated load. SiC schottky diodes on secondary reduce reverse recovery losses. Above 85% efficiency is obtained up to 10% load at V_{in} = 22 V and 20% load at V_{in} = 41 V.

For a comparison, efficiency measurements for conventional converter without external parallel inductors are also provided in Fig. 2.30. In brackets (P) and (C) stand for proposed converter and conventional converter, respectively. At rated load condition, V_{in} = 22V, the efficiency values for proposed design and conventional topology are quite close and almost coincide with each other because magnetizing current is very low (of the order of mA) and leakage inductance of non-ideal transformer assists in soft switching at rated load condition. However, below 35% load, conventional converter loses soft switching and proposed converter thus gains higher efficiency. The difference reaches more than 5% at 10% load. It can be even higher at higher switching frequency. At source voltage above rated value, V_{in} = 41V, the proposed converter has higher efficiency throughout the output power variation. Hence, it is necessary to select a proper design of transformer magnetizing inductance with respect to leakage inductance to have flat or high efficiency curve throughout the variation in load and input voltage which can bring much benefit in real application.

Fully hard switching converter will need devices of above 2x voltage rating due to turn-off voltage spike across the devices and conduction losses will be nearly 2x due to increased $R_{ds,on}$ (high voltage devices). It will have low efficiency throughout the load and voltage variation. Then, there will be a significant difference in efficiency curve at light load because switching losses are proportional to switching frequency and dominate at light load and increased source voltage.

Above all, wide range soft-switching as demonstrated allows raising the switching frequency of operation. The proposed extended range soft-switching design maintains high efficiency due to soft-switching.

2.8 Summary and Conclusions

In this Chapter, the characteristics and properties of fuel cells are introduced first. Since the fuel cell is an unregulated low voltage current intensive source and its voltage and current varies over a wide range, a front-end DC/DC converter needs to be employed to boost the low dc voltage to match the load specifications and profile. The requirements of this front-end DC/DC converter are summarized as high boost ratio, capable of accommodating wide range of source voltage and load, low input current ripple, high density, isolation and high power transferring ability. Subsequently, a detailed literature review of DC/DC converters has been done. Different current-fed, voltage-fed, PWM and resonant converters have been discussed. The two-inductor active-clamped current-fed converter has been justified to be a suitable topology for fuel cell applications with the merits of reduced peak currents, wide soft-switching range, high efficiency, and free from rectifier diode ringing and secondary side snubbers. However, maintaining ZVS soft switching for wide variation in input voltage and load conditions is still a challenge.

Magnetizing inductance based L-L type active-clamped half-bridge current-fed converter has been extended to realize a three-phase converter. The concept is utilized to modify a three-phase circuit topology. An extended range soft-switching (ZVS) three-phase ac link current-sharing current-fed

isolated DC/DC converter with magnetizing inductance effect is studied in this Chapter. Weakened magnetizing inductance in voltage-fed converters results in significant circulating current through the devices. It increases the device conduction and turn-off losses and therefore significant reduction in efficiency. However, the same has insignificant effect on nominal efficiency (rated load) and on the other hand improves the light load efficiency for current-fed converters. The proposed three-phase converter avails current sharing resulting in reduced device current ratings and low conduction losses and higher power density. Aided by magnetizing inductances, the converter maintains ZVS at high input voltage and low output power because of increased peak leakage (series) inductance current, i.e., higher energy to discharge device/snubber capacitances. Lower average and RMS currents through components are achieved owing to current sharing by three phases. Input/output ripple frequency is 3x switching frequency and results in small size input and output filters. Experimental results on 300W aboratory converter prototype validate claimed ZVS for wide range of output power (rated down to 10%) and source voltage (22V to 41V). Complete steady-state operation, analysis, and design of the converter are reported and verified by simulation results.

Chapter 3

Naturally Clamped Zero Current Commutated Soft-switching Current-fed Dual Active Bridge (CFDAB) DC/DC Converter

3.1 Introduction

In Chapter 2, the magnetizing inductance assisted extended soft-switching three-phase AC link current-fed DC/DC converter has been discussed. ZVS of all switches over wide variations of source voltage and output power has been achieved. Proposed three-phase converter is suitable to interface the low voltage fuel cell stack to high voltage dc bus that accommodates wide range of fuel cell voltage and power variations with temperature, fuel flow, and fuel pressure. As discussed in Chapter 1, FCVs suffer from slow dynamic response to load variation due to their slow internal electrochemical, mechanical, and thermal dynamic characteristics and therefore, needs supplementary source of energy that can deliver quick power [5, 13, 119]. An auxiliary energy storage system (ESS) such as battery or supercapacitor is usually utilized for cold start up, absorbing the regenerative braking energy and achieving good performance during transient operation.

Functional diagram of a typical fuel cell powered propulsion system is shown in Fig. 1.7. Fuel cell stack is connected to high voltage dc bus acting as

the main source. A bidirectional DC/DC converter is required to interface low voltage ESS to the high voltage dc bus, managing power flow between ESS and dc bus. This DC/DC converter plays a vital role in coordination with main source and auxiliary source, which needs to meet the following requirements: 1) High step-up ratio to boost low battery voltage up to high voltage fuel cell bus. 2) Bidirectional power flow. The converter should be able to supply energy during cold start-up and transition operation in forward direction and absorb energy during regenerative braking in reverse direction. 3) Low input current ripple. 4) High power handling capacity. 5) High-frequency operation to realize a compact, lightweight, high power density and low cost system. 6) Ability to accommodate wide variations of input/output voltage and load conditions. 7) High efficiency. High efficiency thereby results into better source utilization and higher output.

The objectives of this Chapter are to investigate the novel bidirectional DC/DC converters satisfying the above mentioned requirements. The objectives are realized and outlined in various Sections as follows: Different bidirectional DC/DC converters have been reviewed, and the corresponding merits and demerits have been discussed in Section 3.2. Then a novel naturally clamped zero current commutated soft-switching current-fed dual active bridge (CFDAB) DC/DC converter is proposed to solve the existing problem in literature in Section 3.3. Steady-state operation of the converter is explained and its mathematical analysis is reported in Section 3.4. Detailed converter design procedure is illustrated in Section 3.5. Analysis and design are verified by simulation results using PSIM 9.0.4 in Section 3.6. Experimental results on

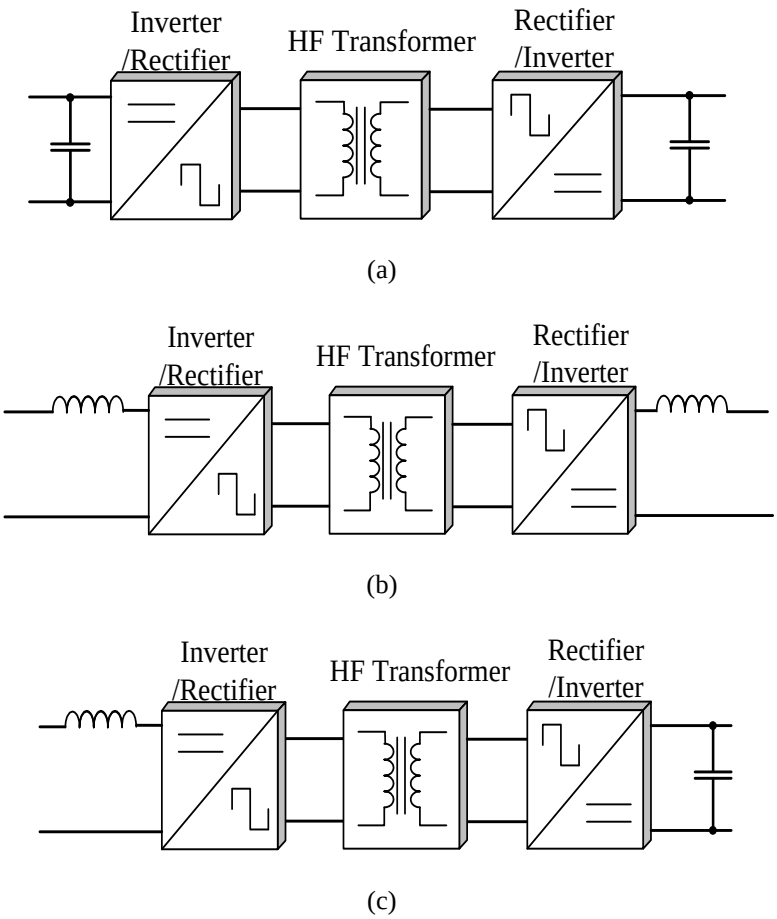
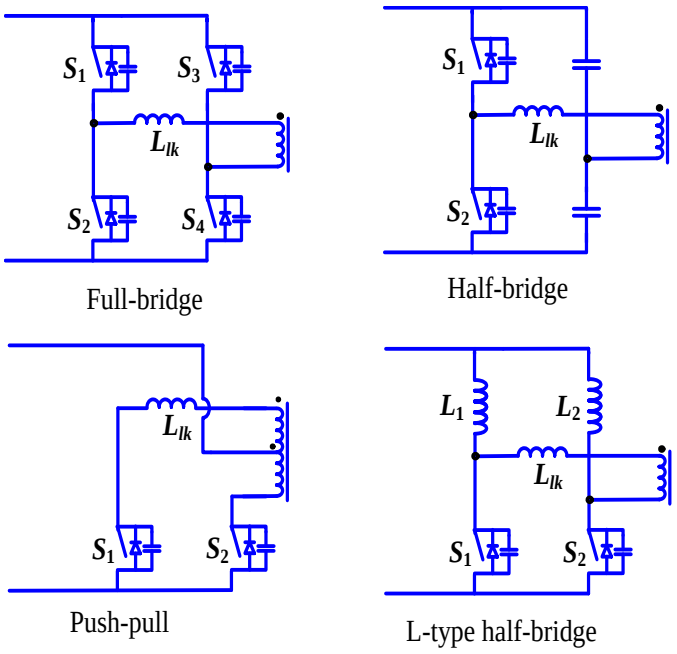


Fig. 3.1. Topology categorization of bidirectional DC/DC converters based on voltage-fed and current-fed input/output: (a) Dual voltage-fed topology, (b) Dual current-fed topology, (c) Combination of voltage-fed and current-fed topologies.

a laboratory prototype of 250W are demonstrated to validate and exhibit the converter performance in Section 3.6. The Chapter is concluded in Section 3.7.

3.2 Survey of Bidirectional DC/DC Converter

Bidirectional DC/DC converters can be divided into non-isolated and isolated converters. Although non-isolated converters are simple and cost effective [120-122], high frequency (HF) transformer isolated converters are preferred for FCVs application owing to high voltage step-up function, galvanic isolation and flexibility of system configuration (dual outputs, series



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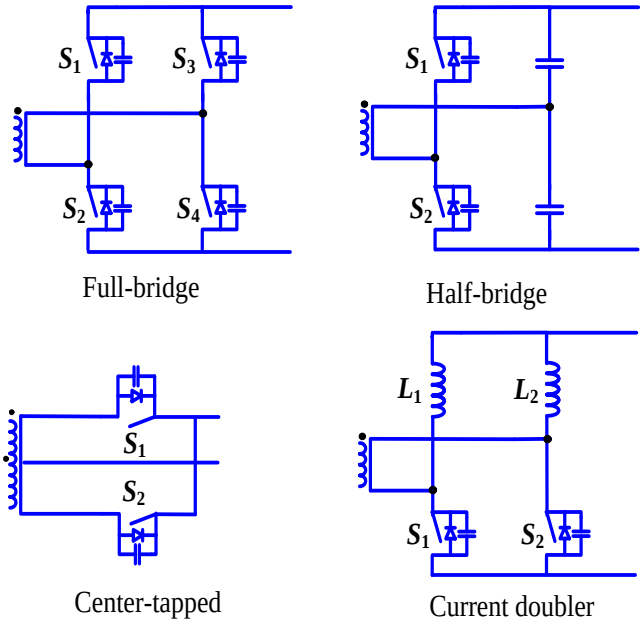


(b)

Fig. 3.2. Major inverter and consequent rectifier topologies used for bidirectional DC/DC converter in Fig. 3.1. (a) Inverter topologies, (b) Rectifier topologies.

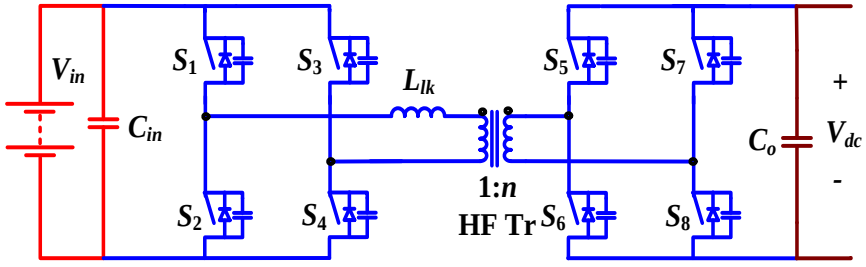


Fig. 3.3. Bidirectional Dual Active Bridge (DAB) PWM DC/DC converter.

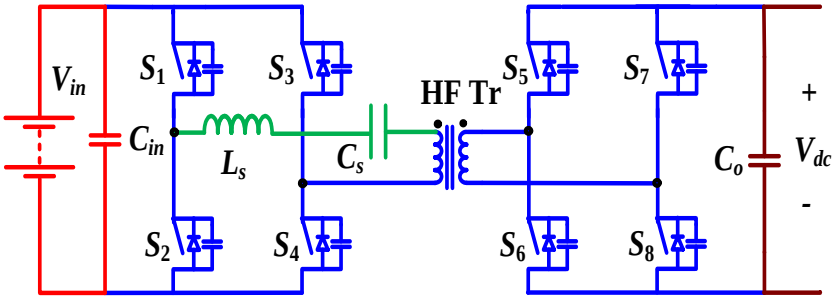


Fig. 3.4. Bidirectional series resonant DAB DC/DC converter.

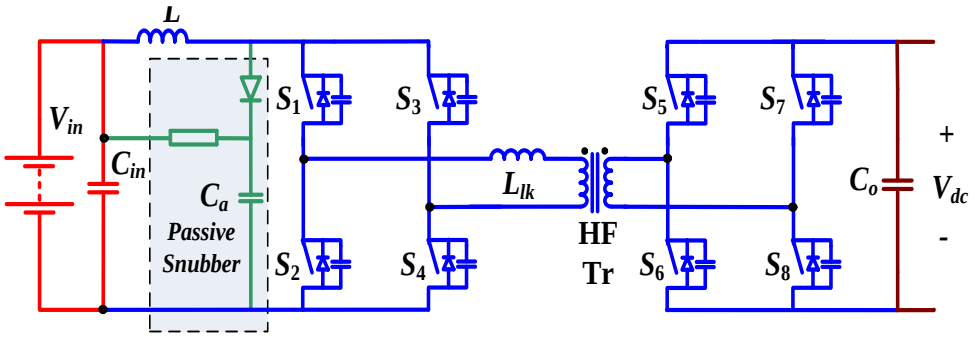
and/or parallel connections) [74]. Isolated converters enhance safety, reliability and flexibility of the system [123].

Isolated bidirectional DC/DC converters can be categorized into three types: (a) dual voltage-fed topology, (b) dual current-fed topology, (c) combination of voltage-fed and current-fed topologies as illustrated in Fig. 3.1 [124]. Here, voltage-fed means that the converter is connected to a voltage source or dc capacitor in parallel while current-fed means that the converter is connected to a current source or dc inductor in series. Fig. 3.2 gives several major double-ended isolated inverter and consequent rectifier topologies for bidirectional DC/DC converters [124]. These topologies can be combined to form a variety of bidirectional DC/DC converter circuits.

One of the most popular topologies is the dual active bridge (DAB) converter as shown in Fig. 3.3, consisting of two voltage-fed full bridges topologies across the transformer windings. DAB converter provides high performance, high efficiency, galvanic isolation, inherent soft-switching, and immunity to parasitic inductance. The control of DAB is flexible and generally fixed frequency phase-shift modulation with fixed duty cycle is employed. Power transferring is controlled by varying the phase-shift between the two voltage waveforms appearing across the two sides of the HF transformer. ZVS

soft-switching is achieved for all semiconductor devices constituting the two bridges. One of the drawbacks of the DAB is high circulating current and relatively low efficiency at light load conditions. The operation of DAB is optimized when the voltage conversion ratio is equal to the transformer turns ratio. When the voltage conversion ratio deviates far from the transformer turns ratio, the converter's efficiency deteriorates seriously because of high circulating current [123]. Several alternative hybrid modulation techniques that combine the phase-shift and duty cycle control have been introduced to extend soft switching range and improve efficiency of voltage-fed DAB converter. These include the trapezoidal and triangular methods [125-127], the phase-shift-plus-one modulation methods [128], and the dual phase-shift control [129]. However, these methods bring intensive computational complexity. Fig. 3.4 presents a series resonant DAB converter. The main drawback of this converter is that the series capacitor has to handle the full load current, resulting in high volume and cost [123, 130].

A combination of voltage-fed and current-fed topologies to develop bidirectional DC/DC converter is shown in Fig. 3.5 to Fig. 3.7. Compared with voltage-fed converters, current-fed converters deliver merits of smaller input current ripple, lower rectifier diode voltage rating, reduced transformer turns-ratio, negligible rectifier diode ringing, no duty cycle loss, and easier current controllability [39,113-114], i.e., current-fed converters can directly and precisely control the charging and discharging current of ESS. This helps in achieving higher charging/discharging efficiency, longer cycle life and shorter charging time of ESS [131]. Thus current-fed converter is more apt for low voltage high current applications.



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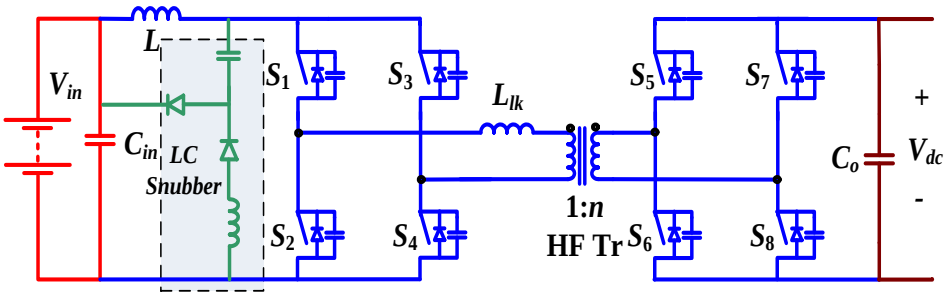

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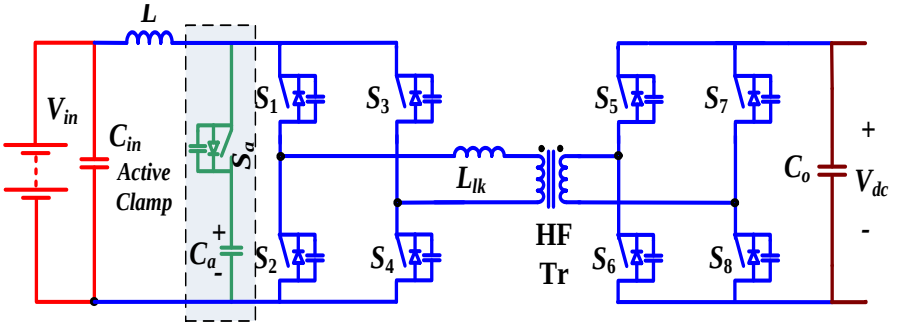

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Fig. 3.5. Bidirectional DC/DC converter based on a current-fed full-bridge topology at the low voltage side and a voltage-fed full-bridge at the high voltage side. (a) Employing a passive RCD snubber. (b) Employing an energy recovery snubber. (c) Employing an active-clamping snubber.

For the current-fed topology at the low voltage side, three typical topologies i.e. full-bridge [132-136], half-bridge [72, 118, 137], and push-pull [138-139] have been researched elaborately. As discussed in Chapter 2, one drawback of current-fed converters is the voltage spike induced by the energy trapped in the transformer leakage inductance resulting in higher component stress and lower conversion efficiency. Normally, passive RCD snubbers [132,

135], energy recovery snubbers/energy recovery auxiliary circuit [71, 74] or active-clamping snubbers [72, 118, 132-134, 138] are employed to absorb the surge voltage and assist in soft-switching as illustrated in Fig. 3.5. The problem with RCD passive snubbers is that the energy absorbed by the clamping capacitor is dissipated on the resistor resulting in low efficiency. For energy recovery snubbers/energy recovery auxiliary circuits [74, 135], although the trapped energy can be recycled, they still contribute to a significant amount of loss.

Active-clamp circuits [72, 118, 132-134, 138], which consist of active switch(es) and capacitor(s), have been used to clamp voltage spike and recycle the energy. However, they suffer from the disadvantages like high number of components, high peak current stress, higher circulating current at light load, and reduced boost capacity.

For current-fed bidirectional converter, the voltage-fed (high voltage) side switches provide the flexibility to preset the current flowing through leakage inductance to the boost inductor current before the commutation of current-fed side switches thus reducing or eliminating the need of snubber circuit. This is referred to active commutation technique [135, 140-141]. In [140], this commutation time has to be precisely controlled limiting practical applications while reference [141] suffers from the voltage spike because the output switch capacitance resonates with the leakage inductance. For the soft-commutation method proposed by [135], the energy consumption of the passive snubber can be reduced but can’t be completely eliminated.

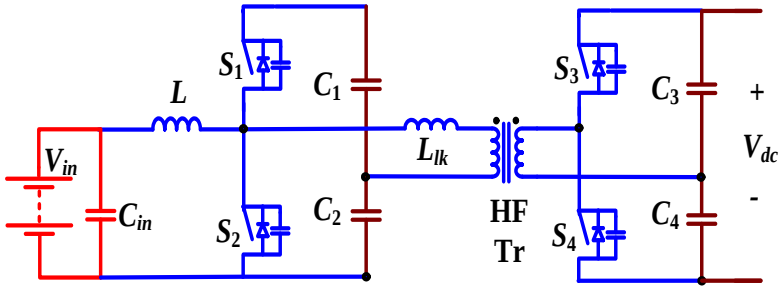


Fig. 3.6. Bidirectional DC/DC converter based on a current-fed half-bridge topology at the low voltage side and a voltage-fed half-bridge at the high voltage side.

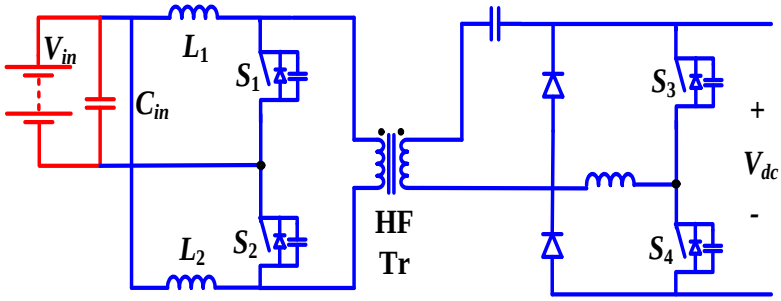


Fig. 3.7. Asymmetrical bidirectional isolated dc-dc converter.

A dual half-bridge bidirectional DC/DC converter is proposed to minimize the number of switching devices [142] as shown in Fig. 3.6. However, this topology requires four split capacitors that handle full-load current and occupy a considerable volume of the converter. It may need additional control to avoid the possibility of voltage imbalance across the capacitors. Also, the topology is not modular in nature and so not easily scalable for higher power. Peak current through the primary switches are > 2.5x the input current and the top and bottom switches share unequal currents.

Fig. 3.7 shows an asymmetrical half-bridge bidirectional DC/DC converter [143]. Two inductors are used at the low voltage side and a series blocking capacitor is placed to prevent transformer saturation, which may limit the power transferring capacity of the circuit.

3.3 Proposed Naturally Clamped Zero Current Commutated Current-fed Dual Active Bridge (CFDAB) DC/DC Converter

In this Chapter, a novel secondary modulation based naturally clamped soft-switching bidirectional snubberless current-fed dual active bridge (CFDAB) converter is proposed as shown in Fig. 3.8. Natural commutation or voltage clamping with zero current switching of primary devices is achieved by the proposed secondary modulation and this eliminates the need for passive or active-clamp snubber making it snubberless and novel. Switching losses are reduced significantly owing to soft-switching of semiconductor devices, i.e., ZCS of primary switches and ZVS of secondary switches. Soft-switching permits higher switching frequency modulation with smaller magnetics. In reverse direction, the converter acts as a standard voltage-fed full-bridge isolated DC/DC converter with inductive output filter. Standard phase-shift modulation can be employed to achieve ZVS of high voltage side devices and ZCS of low voltage side devices with relatively low circulating current [144-145].

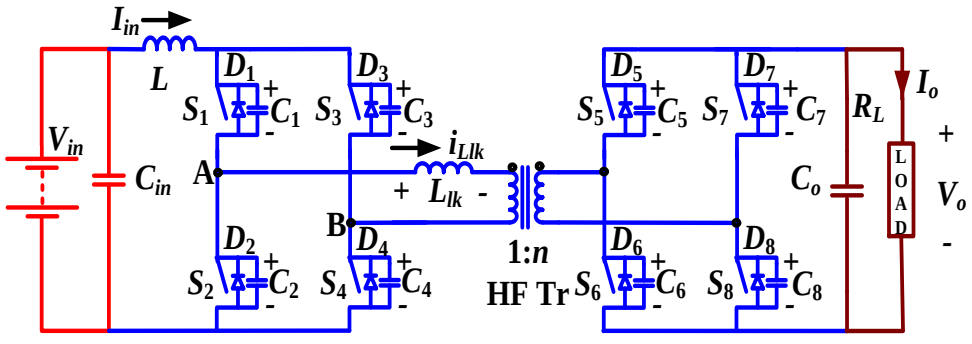


Fig. 3.8. Proposed ZCS current-fed dual active bridge (CFDAB) DC/DC converter

3.4 Operation and Analysis of the Converter

In this Section, steady-state operation and analysis with zero current commutation (ZCC) and natural voltage clamping (NVC) concept has been explained. Before turning-off of the diagonal switch pairs of primary side switches (say S_1-S_4), the other pair (say S_2-S_3) is turned-on. Reflected output voltage V_o/n appears across the transformer primary. It diverts the current from one switch pair to the other pair through transformer causing current through incoming switch pair to rise and the current through the outgoing switch pair to fall to zero naturally resulting in ZCC. Later, the body diodes across the switch pair start conducting and their gating signals are removed leading to ZCS turn-off of the devices. Commutated device capacitances start charging with NVC.

For the sake of simplicity and easiness of understanding, the following assumptions are made to study the steady-state operation and analysis of the converter: a) Boost inductance L is large enough to maintain constant current through it. b) All the components are ideal. c) Inductance L_{lk} includes the leakage inductance of the transformer. d) Magnetizing inductance of the transformer is infinitely large.

The steady-state operating waveforms are shown in Fig. 3.9. The primary switches pairs S_1-S_4 and S_2-S_3 are operated with identical gating signals phase-shifted by 180^o with an overlap. The overlap varies with duty cycle, and the duty cycle should be kept above 50%. The steady-state operation of the converter during different intervals in a one half HF cycle is explained using the equivalent circuits shown in Fig. 3.10.

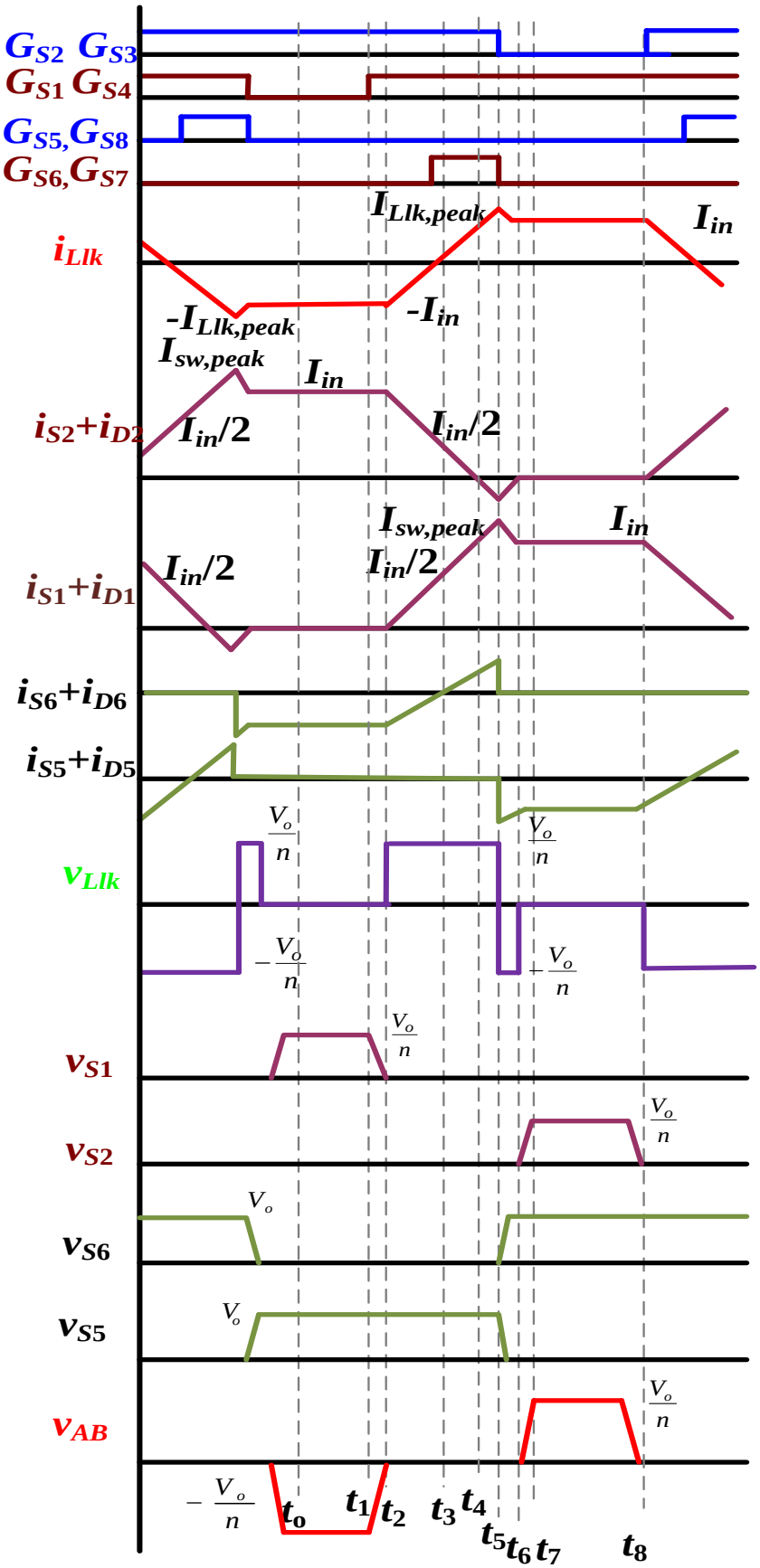


Fig. 3.9. Operating waveforms of the proposed ZCS CFDAB DC/DC converter.

Interval 1 (Fig. 3.10a; $t_0 < t < t_1$): In this interval, the primary side H-bridge switches S_2 and S_3 and anti-parallel body diodes D_6 and D_7 of the secondary side H-bridge switches are conducting. The current through inductor L_{lk} is negative and constant. Power is transferred to the load through the HF transformer. The non-conducting secondary devices S_5 and S_8 and the non-conducting primary devices S_1 and S_4 are blocking output voltage V_o and reflected output voltage V_o/n respectively. The values of current through various components are: $i_{S2} = i_{S3}=I_{in}$, $i_{S1} = i_{S4}=0$, $i_{Llk}=-I_{in}$, $i_{D6} = i_{D7}= I_{in}/n$. Voltage across the switches S_1 and S_4: $V_{S1} =V_{S4} = V_o/n$. Voltage across the switches S_5 and S_8: $V_{S5} =V_{S8} = V_o$.

Interval 2 (Fig. 3.10b; $t_1 < t < t_2$): At $t = t_1$, primary switches S_1 and S_4 are turned-on. Snubber capacitors C_1 and C_4 discharge in a short period of time.

Interval 3 (Fig. 3.10c; $t_2 < t < t_3$): Now all four primary switches are conducting. Reflected output voltage V_o/n appears across leakage inductance L_{lk} and causes its current to increase linearly. It causes currents through previously conducting devices S_2 and S_3 to reduce linearly. It results in conduction of switches S_1 and S_4 with zero current which helps in reducing associated turn-on loss. The currents through various components are given by

$$i_{Llk} = -I_{in} + \frac{V_o}{n \cdot L_{lk}} \cdot (t - t_2) \tag{3-1}$$

$$i_{S1} = i_{S4} = \frac{V_o}{2n \cdot L_{lk}} \cdot (t - t_2) \tag{3-2}$$

$$i_{S2} = i_{S3} = I_{in} - \frac{V_o}{2n \cdot L_{lk}} \cdot (t - t_2) \tag{3-3}$$

$$i_{D6} = i_{D7} = \frac{I_{in}}{n} - \frac{V_o}{n^2 \cdot L_{lk}} \cdot (t - t_2) \tag{3-4}$$

Since the anti-parallel body diodes D_6 and D_7 are conducting, switches S_6 and S_7 can be gated for ZVS turn on. At the end of this interval $t=t_3$, D_6 and D_7 commutates naturally. Primary current reaches zero and ready to change polarity. Current through all primary devices reaches $I_{in}/2$. Final values are: $i_{Llk}=0$, $i_{S1}= i_{S2} = i_{S3}= i_{S4}=I_{in}/2$, $i_{D6} = i_{D7}= 0$.

Interval 4 (Fig. 3.10d; $t_3 < t < t_4$): In this interval, the secondary H-bridge devices S_6 and S_7 are turned on with ZVS. Currents through all the switching devices continue to increase or decrease with the same slope as interval 3. At the end of this interval, primary devices S_2 and S_3 commutate naturally with ZCC and their respective currents i_{S2} and i_{S3} reach zero obtaining ZCS. The full current, i.e. input current I_{in} is taken over by other devices S_1 and S_4, and transformer current changes polarity. Final values are: $i_{Llk}= I_{in}$, $i_{S1}=i_{S4}=I_{in}$, $i_{S2} = i_{S3}=0$, $i_{S6} = i_{S7}= I_{in}/n$.

Interval 5 (Fig. 3.10e; $t_4 < t < t_5$): In this interval, the primary current or leakage inductance current i_{Llk} increases further with the same slope. Anti-parallel body diodes D_2 and D_3 start conducting causing extended zero voltage to appear across the outgoing or commutated switches S_2 and S_3 to ensure ZCS turn-off. Now, the secondary devices S_6 and S_7 are turned-off. At the end of this interval, currents through the transformer, switches S_1 and S_4 reach their peak value. This interval should be very short to limit the peak current though the transformer and switches, and so their kVA ratings.

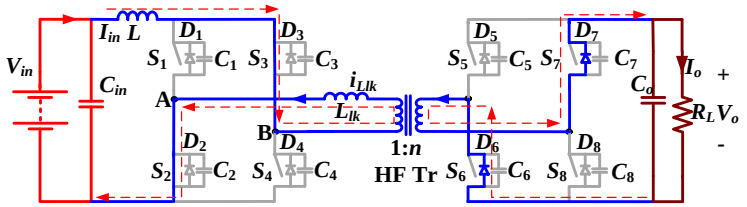
The currents through operating components are given by

$$i_{Llk} = I_{in} + \frac{V_o}{n \cdot L_{lk}} \cdot (t - t_4) \tag{3-5}$$

$$i_{S1} = i_{S4} = I_{in} + \frac{V_o}{2n \cdot L_{lk}} \cdot (t - t_4) \tag{3-6}$$

$$i_{D2} = i_{D3} = \frac{V_o}{2n \cdot L_{lk}} \cdot (t - t_4) \tag{3-7}$$

$$i_{S6} = i_{S7} = \frac{I_{in}}{n} + \frac{V_o}{n^2 \cdot L_{lk}} \cdot (t - t_4) \tag{3-8}$$



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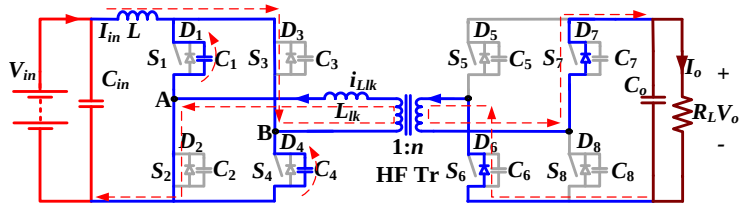

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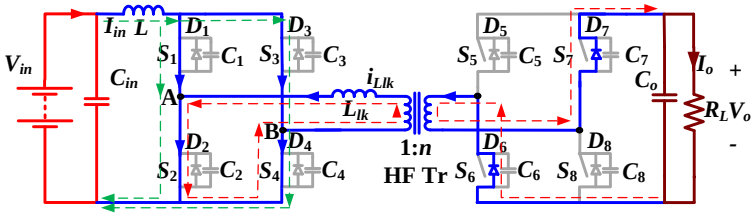

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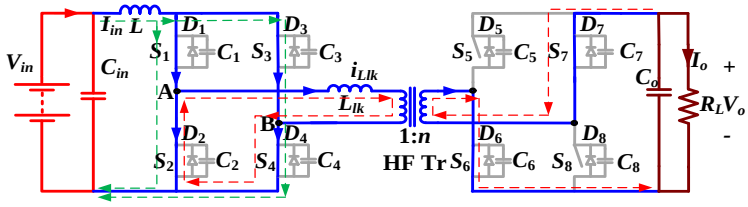


(d)

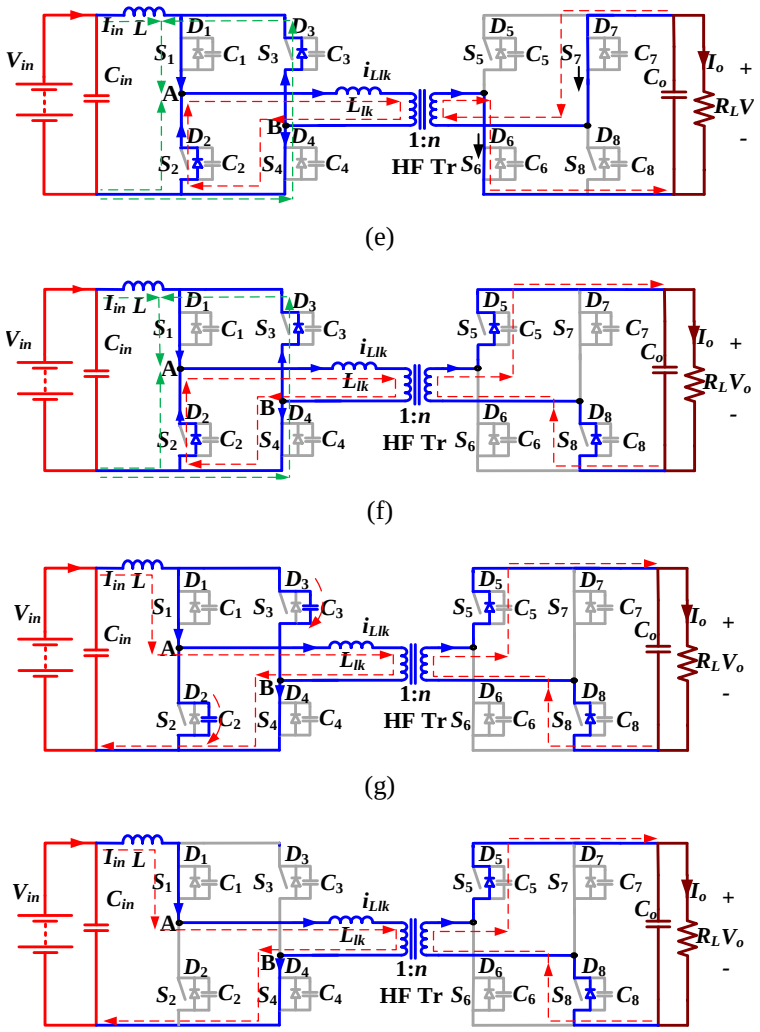


Fig. 3.10. Equivalent circuits during different intervals of operation of the proposed converter for the waveforms shown in Fig. 3.9.

Interval 6 (Fig. 3.10f; $t_5 < t < t_6$): During this interval, secondary switches S_6 and S_7 are turned-off. Anti-parallel body diodes of switches S_5 and S_8 take over the current immediately. Therefore, the voltage across the transformer primary reverses polarity and the current through it starts decreasing. The currents through the switches S_1 and S_4 and body diodes D_2 and D_3 also start decreasing.

The currents through operating components are given by

$$i_{S6} = i_{S7} = \frac{I_{in}}{n} + \frac{V_o}{n^2 \cdot L_{lk}} \cdot (t - t_4) \tag{3-8}$$

$$i_{Llk} = I_{Llk,peak} - \frac{V_o}{n \cdot L_{lk}} \cdot (t - t_5) \tag{3-9}$$

$$i_{S1} = i_{S4} = I_{sw,peak} - \frac{V_o}{2n \cdot L_{lk}} \cdot (t - t_5) \tag{3-10}$$

$$i_{D2} = i_{D3} = I_{D2,peak} - \frac{V_o}{2n \cdot L_{lk}} \cdot (t - t_5) \tag{3-11}$$

$$i_{D5} = i_{D8} = \frac{I_{Llk,peak}}{n} - \frac{V_o}{n^2 \cdot L_{lk}} \cdot (t - t_5) \tag{3-12}$$

At the end of this interval, currents through D_2 and D_3 reduce to zero and are commutated naturally. Currents through S_1 and S_4, and transformer reach I_{in}. Final values: $i_{Llk} = i_{S1} = i_{S4} = I_{in}$, $i_{D2} = i_{D3} = 0$, $i_{D5} = i_{D8} = I_{in}/n$.

Interval 7 (Fig. 3.10g; $t_6 < t < t_7$): In this interval, snubber capacitors C_2 and C_3 charge to V_o/n in a short period of time. Switches S_2 and S_3 are in forward blocking mode now.

Interval 8 (Fig. 3.10h; $t_7 < t < t_8$): In this interval, currents through S_1 and S_4, and transformer are the constant input current I_{in}. Current through the anti-parallel body diodes of the secondary switches D_5 and D_8 is I_{in}/n.

The final values are: $i_{S1} = i_{S4} = i_{Llk} = I_{in}$, $i_{S2} = i_{S3} = 0$, $i_{D5} = i_{D8} = I_{in}/n$. Voltage across the switches S_2 and S_3: $V_{S2} = V_{S3} = V_o/n$.

In this half HF cycle, current has transferred from one diagonal switch pair to the other diagonal switch pair, and the transformer current has reversed its polarity.

3.5 Design of the Converter

In this Section, converter design procedure is illustrated with a design example for the following specifications: input voltage V_{in} = 12 V, output voltage V_o = 150 to 300V, nominal output voltage = 288V, output power P_o = 250W, switching frequency f_s = 100 kHz. The design equations are presented to determine the components' ratings. It helps in the selection of the components as well as to predict the converter performance theoretically.

(1) Average input current is $I_{in} = P_o/(\eta V_{in})$. Assuming an ideal efficiency η of 95%, I_{in} = 21.9 A.

(2) Maximum voltage across the primary switches is

$$V_{P,SW} = \frac{V_o}{n} \tag{3-13}$$

(3) Voltage conversion ratio or input and output voltages are related as

$$V_o = \frac{n \cdot V_{in}}{2 \cdot (1-d)} \tag{3-14}$$

where d is the duty cycle of primary switches.

(4) Leakage inductance of the transformer or series inductance L_{lk} is calculated by

$$L_{lk} = \frac{V_o \cdot (d-0.5)}{2 \cdot n \cdot I_{in} \cdot f_s} \tag{3-15}$$

(5) RMS current through the primary switches is given by

$$I_{P,rms} = I_{in}\sqrt{\frac{2-d}{3}} \tag{3-16}$$

The selection of transformer turns-ratio is associated with device rms current and conduction losses, in particular primary side semiconductor

devices because they carry higher currents. Higher value of turns-ratio reduces the maximum voltage across the primary switches that permit the use of low voltage devices with low on-state resistance (from (3-13)). However, selection of higher value of turns-ratio yields higher switch rms current (from (3-14) and (3-16)). Maximum duty cycle is obtained accordingly from (3-14). Therefore, an optimal value of *n* should be selected to limit the conduction losses to obtain the best converter efficiency and components' utilization. An optimum value of n =10 at d = 0.8 are selected to achieve low overall conduction losses for the given specifications. Output voltage can be regulated from 150 V to 300 V by modulating the duty ratio between 0.6 and 0.8 with battery voltage variation. Leakage inductance from (3-15) is calculated as L_{lk} = 2.05 μH.

(6) RMS current through the transformer primary is given by

$$I_{Llk,rms} = I_{in}\sqrt{\frac{5-4d}{3}} \tag{3-17}$$

(7) Value of boost inductor is given by

$$L = \frac{V_{in}\cdot(d-0.5)}{\Delta I_{in}\cdot f_s} \tag{3-18}$$

where ΔI_{in} is the boost inductor ripple current. For ΔI_{in} = 1 A, L = 36 μH.

(8) Average current through the secondary devices is given by

$$I_{av} = P_o/(2V_o) \tag{3-19}$$

Here, $I_{av} \cong 0.42$ A. Voltage rating of secondary side devices, V_o = 300V.

(9) Average current through the anti-parallel body diodes of secondary devices is given by

$$\bar{i}_D = \frac{I_{in} \cdot (7 - 6d)}{8n} \tag{3-20}$$

(10) RMS current through the secondary side switches is given by

$$I_{S,rms} = \frac{I_{in}}{2n}\sqrt{\frac{2d-1}{3}} \tag{3-21}$$

(11) VA rating of HF transformer is given by

$$VA_{x-mer} = \frac{V_o \cdot I_{in}}{n}\sqrt{\frac{2\cdot(5-4d)\cdot(1-d)}{3}} \tag{3-22}$$

The calculated value is $VA_{X\text{-}mer}$ = 321.9 VA.

These equations are derived on the condition that anti-parallel diode conduction time (e.g. interval 6) is quite short and negligible with the intention to ensure ZCS of primary switches without significantly increasing the peak current through the switches. However, at light load of converter, (fuel cell stack is supplying most of the power to motor), the body diode conduction time is relatively large and (3-14) is not valid any more. Due to the longer extended body diode conduction, the output voltage is boosted to higher value than that of nominal boost converter. For such cases, (3-14) is modified into following equation:

$$V_o = \frac{n \cdot V_{in}}{2 \cdot (1 - d - d')} \tag{3-23}$$

Where d' is given by,

$$d' = d - 0.5 - \frac{2 \cdot n \cdot I_{in} \cdot L_{lk} \cdot f_s}{V_o} \tag{3-24}$$

From (3-24), it can be observed that for a given value of L_{lk} and V_o, d' increases as the load is decreased. At full load, d' = 0 and (3-23) is converted to (3-14).

(13) The relation between the output power and duty cycle is given by

$$P = \frac{n \cdot v_{in}^{\ 2} - v_o \cdot v_{in} \cdot (3 - 4 \cdot d)}{4 \cdot n \cdot L_{lk} \cdot f_s} \tag{3-25}$$

3.6 Simulation and Experimental Results

The proposed converter has been simulated for given specifications and calculated components' values using software package PSIM 9.0.4 for input voltage V_{in} = 12 V, output voltage V_o = 300 V, output power P_o = 250W, device switching frequency f_s = 100 kHz. Simulation results are illustrated in Fig. 3.11 and Fig. 3.12.

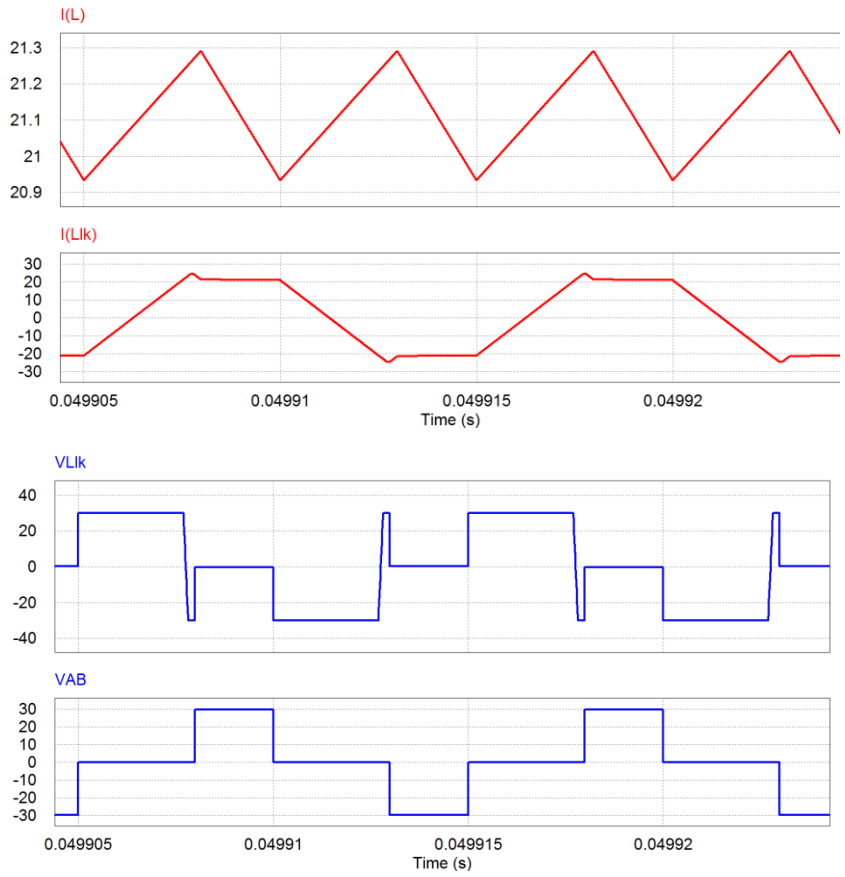


Fig. 3.11. Current waveforms through input inductor *I(L)*, and leakage inductance *I(L_{lk})*, voltage waveform across leakage inductance *V(L_{lk})* and voltage waveform V_{AB}.

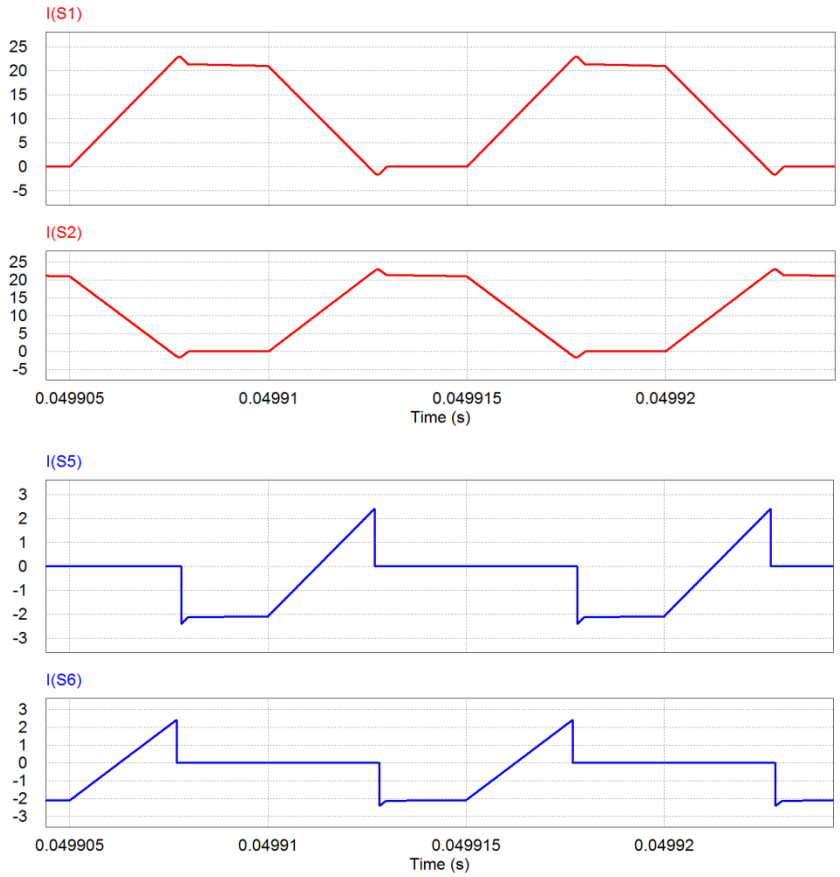


Fig. 3.12. Current waveforms through primary switches I(S_1) and I(S_2) and secondary switches I(S_5) and I(S_6).

Fig. 3.11 and Fig. 3.12 coincide exactly with the theoretically predicted waveforms. It verifies the steady-state operation and analysis of the converter and proposed secondary modulation technique presented in Section 3.4.

Current waveforms through the input inductor L and transformer leakage inductance L_{lk} are shown in Fig. 3.11. The ripple frequency of input inductor current i_L is 2x device switching frequency f_s resulting in a reduction in size. The peak current through inductor L_{lk} above the constant value is caused by the extended conduction of anti-parallel body diode of the corresponding primary switch to ensure ZCS turn-off. The current is continuous and has low peak value. Voltage waveform V_{AB} in Fig. 3.11 shows that voltage across the primary switches is naturally clamped at low voltage i.e., V_o/n. Leakage

inductance voltage V_{Llk} clearly justifies the change in slopes of transformer primary current i_{Llk} waveform. Fig. 3.12 shows current waveforms through primary switches S_1 and S_2 and secondary switches S_5 and S_6 including the currents flowing through their respective body diodes. The current waveforms of two diagonal pairs on primary and secondary sides (S_1 *vs.* S_2, S_5 *vs.* S_6) are phase-shifted with each other by 180^o due to modulation signals. Owing to proposed novel secondary side modulation, the currents through primary switches S_1 and S_2 naturally decrease to zero and then corresponding anti-parallel body diodes start conduction before the switches are turned off (i.e. gate signal removed), which ensures ZCS turn-off. As shown in current waveforms of S_5 and S_6 in Fig. 3.12, the anti-parallel diodes of switches conduct prior to the conduction of corresponding switches, which verifies ZVS of the secondary side switches.

A laboratory prototype of the proposed converter rated at 250W as shown in Fig. 3.13 has been developed to demonstrate its performance experimentally. Details of the experimental converter are given in Table 3.1. Gating signals for the devices have been generated using Xilinx Spartan-3 FPGA board. Two IR2181 are used to drive the primary side MOSFETs and two IR21814 are used to drive the secondary side MOSFETs.

3.6.1. Boost Mode (Discharging Mode)

The specifications of the boost mode: battery voltage V_{in} = 12 V, dc bus voltage V_o = 300 V, discharging power P=250W, device switching frequency f_s = 100 kHz. Energy is transferred from the battery to the dc bus.

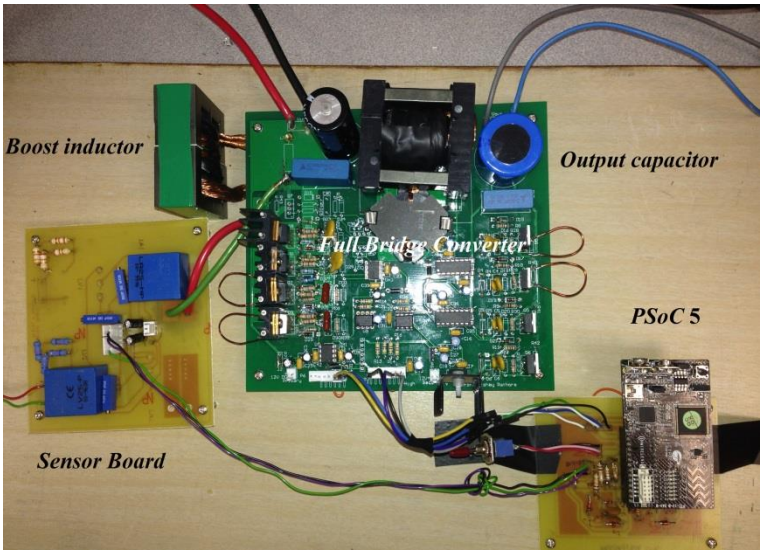


Fig. 3.13. Photograph of the laboratory prototype.

Table 3.1: Major components' parameters of experimental prototype.

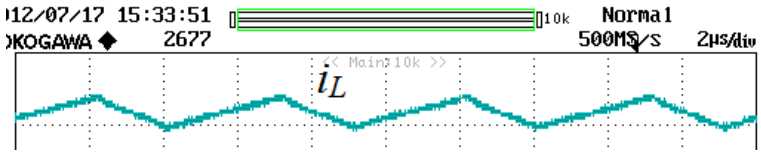
Components	Parameters
Primary switches $S_1 \sim S_4$	IRFB3006PBF 60V, 195A. $R_{ds,on} = 2.1$ mΩ
Secondary switches $S_5 \sim S_8$	IPP60R125CP 650V, 11A. $R_{ds,on} = 0.125$Ω
HF transformer	PC47ETD44-Z ferrite core Primary turns N_1=4 Secondary turns N_2=40 Leakage inductance reflected to primary = 180nH
External series inductor L_{lk}	TDK5901PC40Z L_{lk}=1.5 µH
Input boost inductor L	3C90ETD54 ferrite core turns N = 8 L=16.4 µH
Input capacitors C_{in}	4.7 mF, 50V electrolytic 2.2 µF high-frequency film capacitor
Output capacitors C_o	220uF, 450V electrolytic capacitor 0.68uF, 450V high frequency film capacitor

Experimental results are shown in Fig. 3.14 and Fig. 3.15. Experimental results match closely with the theoretical operating waveforms (Fig. 3.9) and the simulation results. Experimental waveforms clearly demonstrate ZVS of secondary switches and ZCS of primary switches. Fig. 3.14 (a) and Fig. 3.15 (a) show the boost inductor current waveforms with 2x device switching frequency and low ripple magnitude. Fig. 3.14 (b) and Fig. 3.15 (b) show the transformer primary voltage V_{AB} that is voltage across primary devices (positive for $V_{ds,S2}$ and negative for $V_{ds,S1}$).The device voltage is clamped at a

low voltage, which allows the use of low voltage devices. Primary current i_{Llk} is continuous unlike traditional hard-switching and active-clamped converters, and as expected from analysis and simulation results has low peak.

Fig. 3.14 (c)-(d) and Fig. 3.15 (c)-(d) show that the gating signals to the primary switches $V_{gs,S1}$ (top switch S_1) and $V_{gs,S2}$ (bottom switch S_2) are removed first before voltage $V_{ds,S1}$ and $V_{ds,S2}$ across them, respectively, starts rising. There is a clear gap between these two waveforms that is caused by conduction of the anti-parallel body diode of respective switch ensuring their ZCS turn-off. The switch current naturally falls to zero because of proposed modulation and then becomes negative due to anti-parallel body diode conduction confirming the ZCC of primary switches. Fig. 3.14 (e)-(f) and Fig. 3.15 (e)-(f) obviously show the ZVS turn on of the secondary switches. Gating signals to secondary switches $V_{gs,S5}$ (Top switch S_5) $V_{gs,S6}$ (Bottom switch S_6) appears when voltage across them $V_{ds,S5}$ and $V_{ds,S6}$, respectively is zero already. Besides, its body diode conducts prior to switch's conduction causing zero voltage across the secondary switches confirming their ZVS.

On the other hand, the turn-on procedure of primary switches is also demonstrated in waveforms shown in Fig. 3.14 (c)-(d) and Fig. 3.15 (c)-(d). Before turning on, the voltage across primary switch is clamped at V_o/n=30V. When this switch is gated on, the current through it is rising at a slope of *di/dt* = 7.5A/μs from zero. With this limited *di/dt* and low voltage across it, the turn-on switching transition loss (due to overlap of switch voltage and current during switching transition time) is negligible. Considering ZCS turn-off of the primary switches and ZVS turn-on of the secondary side switches mentioned above, the total switching losses are reduced enormously.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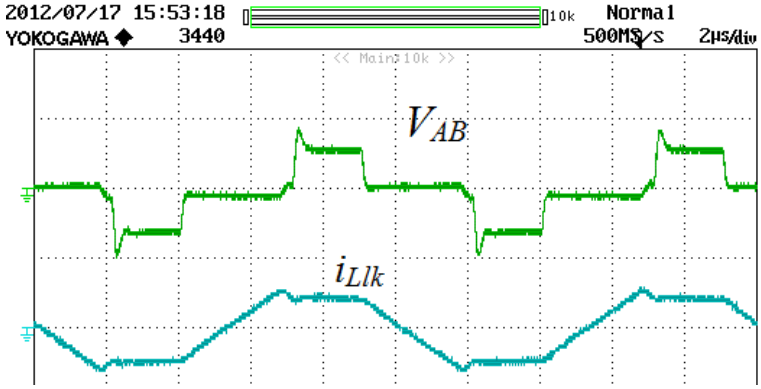
10k
Normal
500MS/s
2µs/div
i_L

(a)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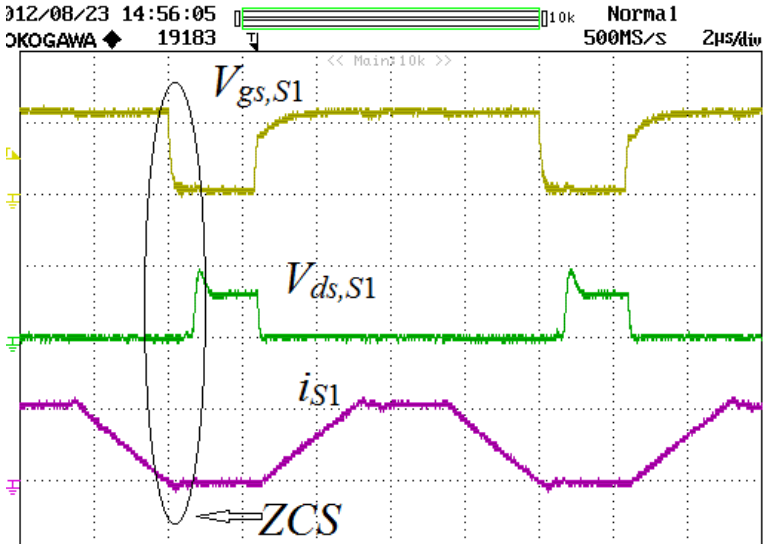
YOKOGAWA
3440
10k
Normal
500MS/s
2µs/div
V_{AB}
i_{Llk}

(b)


012/08/23 14:56:05
OKOGAWA
19183
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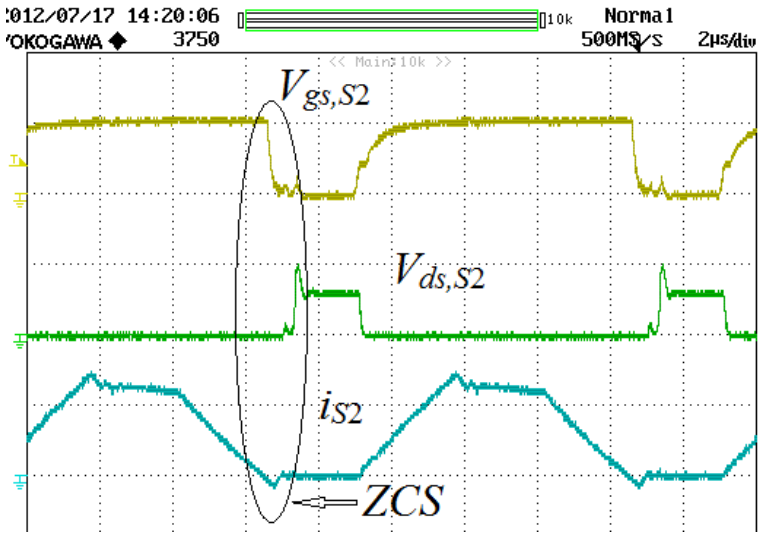
Normal
500MS/s
2µs/div
$V_{gs,S1}$
$V_{ds,S1}$
i_{S1}
ZCS

(c)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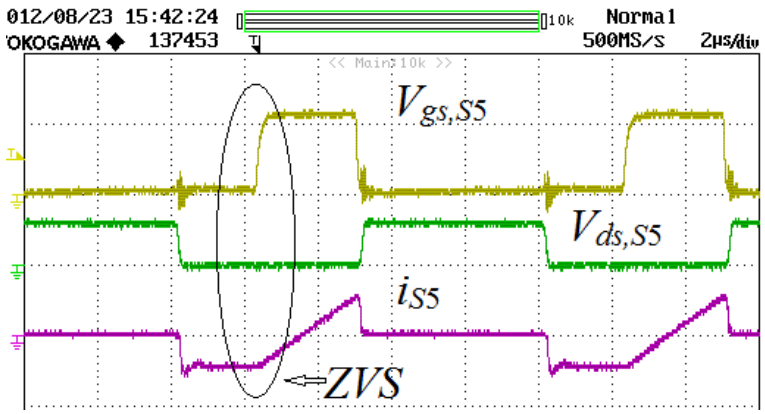
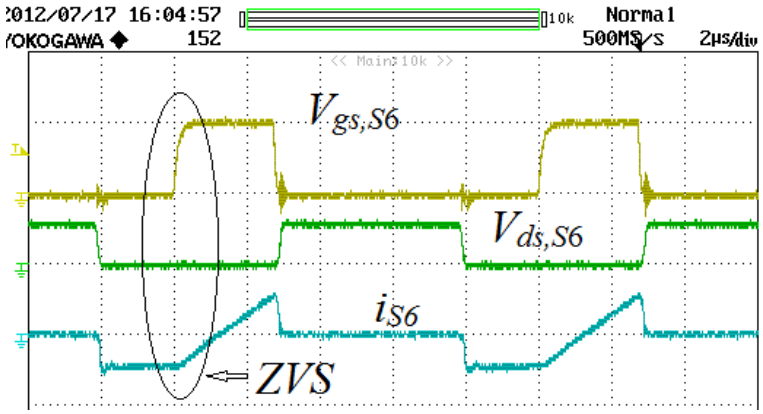
OKOGAWA
3750
10k
Normal
500MS/s
2µs/div
$V_{gs,S2}$
$V_{ds,S2}$
i_{S2}
ZCS

(d)



(e)



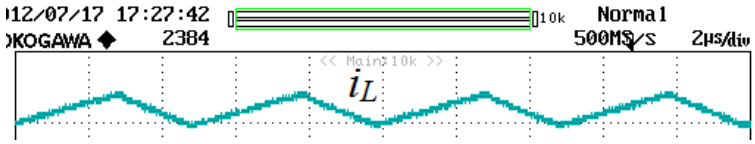
(f)

Fig. 3.14. Experimental results for output power of 250W at 300V in boost mode. (a) Boost inductor current i_L (5A/div), (b) Voltage across the transformer v_{AB} (50V/div) and current through the primary winding i_{Llk} (50A/div), (c-d) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (50V/div) of primary side devices and currents through them (20A/div). (e-f) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (500V/div) across secondary side devices and currents through them (5A/div).

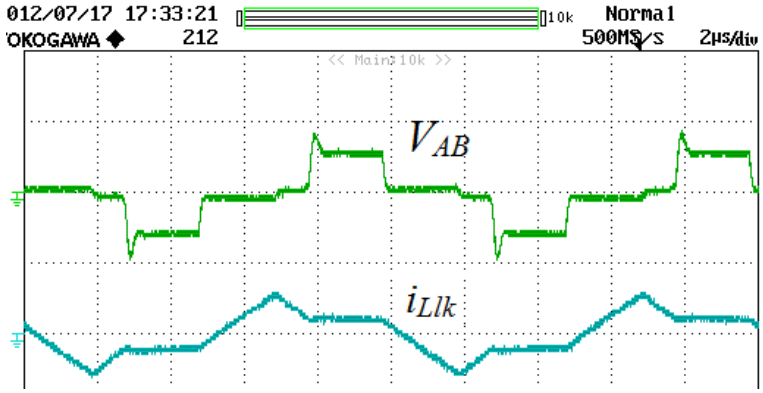
In addition, primary switches of low voltage rating (< 100V) and low on- state resistance can be used resulting in lower conduction loss and higher efficiency.

As shown in Fig. 3.14 and Fig. 3.15, the peak current through the primary switches and transformer is higher than the input current to ensure ZCS of primary devices. Though the peak current increases with reduction in load, the rms value of current through primary switch and transformer reduces with reduction in load current. Thus the conduction losses in primary switches reduce with reduction in output power unlike voltage-fed resonant converters.

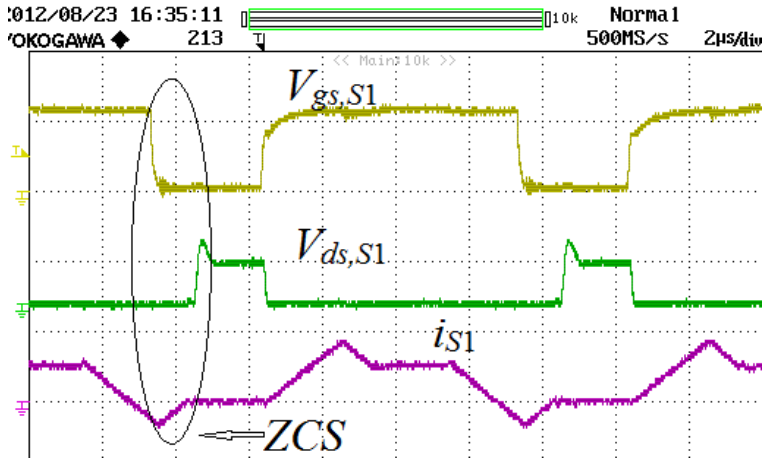
For the experimental prototype, efficiency of 93% for 250W and 92.3% for 100W is obtained in the forward direction.



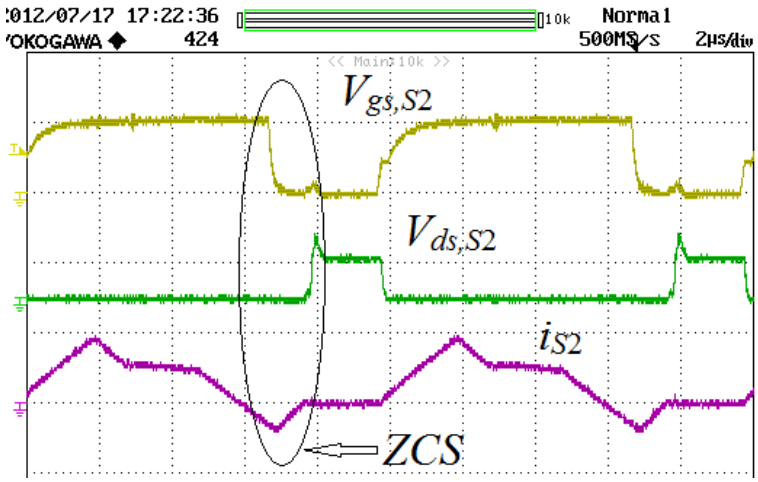
(a)



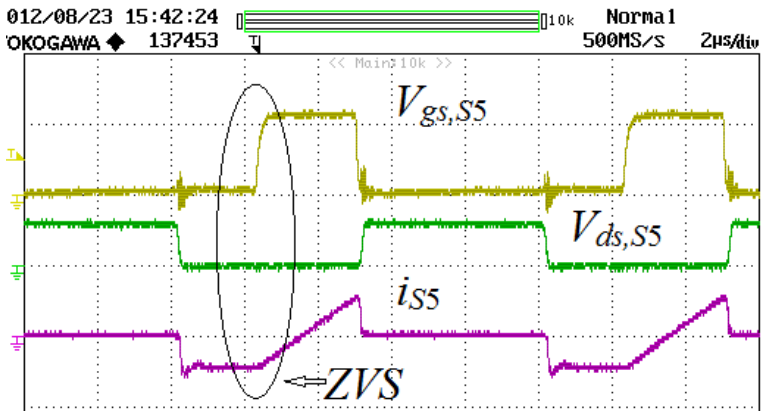
(b)



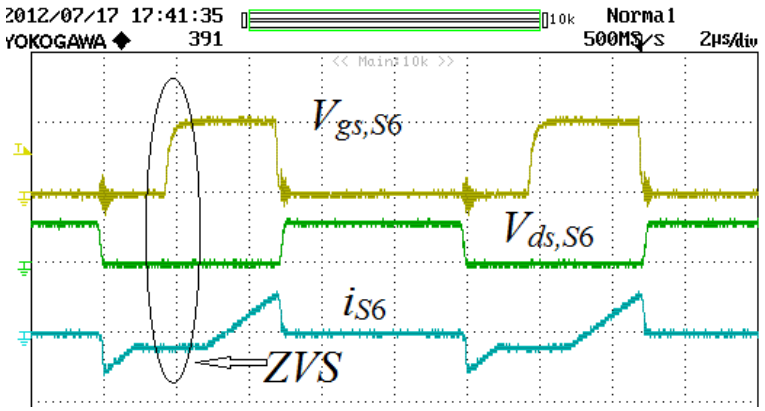
(c)



(d)



(e)



(f)

Fig. 3.15. Experimental results for output power of 100W at 300V in boost mode. (a) Boost inductor current i_L (5A/div), (b) Voltage across the transformer v_{AB} (50V/div) and current through primary winding i_{Llk} (50A/div), (c-d) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (20V/div) across primary side devices and currents through them (20A/div). (e-f) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (500V/div) across secondary side devices and currents through them (5A/div).

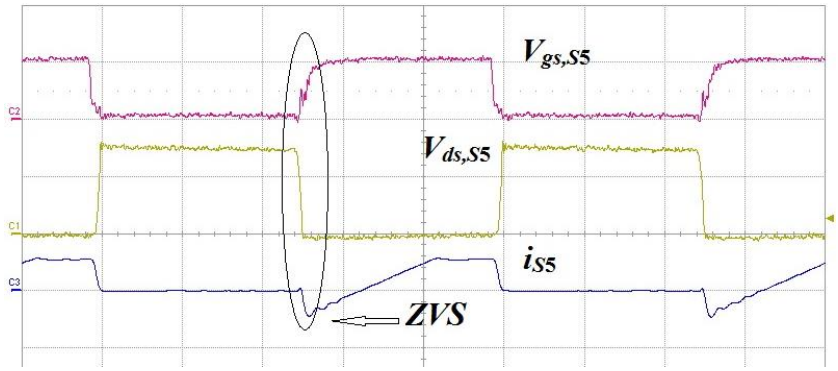
3.6.2 Buck Mode (Charging Mode)

The specifications of the buck mode: battery voltage V_{in} = 10 V, dc bus voltage V_o = 300 V, charging power P= 250W, device switching frequency f_s = 100 kHz. The energy is transferred from the dc bus to the battery. The regenerative braking energy can be fed back and recharge the low voltage storage from high voltage bus, thus increasing the overall system efficiency.

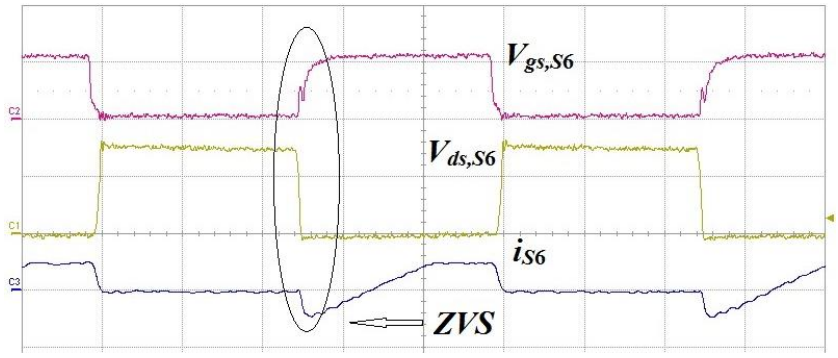
In reverse direction, the converter acts as a standard voltage-fed full-bridge isolated DC/DC converter with inductive output filter. At low voltage

side, devices need not be controlled because body diodes of the devices can take over as high-frequency rectifier. The secondary side diagonal switch pairs S_5-S_8 and S_6-S_7 operated with identical gating signals phase-shifted with each other by 180^o with a well-defined dead time gap.

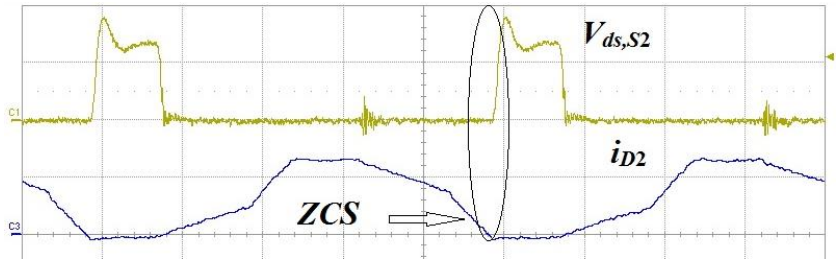
As illustrated in Fig. 3.16, ZVS of high voltage side devices and ZCS of low voltage side devices have been achieved by employing standard phase-shift modulation [144-145].



(a)



(b)



(c)

Fig. 3.16. Experimental results for output power of 250W at 300V in buck mode. (a-b) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (200V/div) across secondary side devices and currents through them (5A/div). (c) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (20V/div) across primary side device and current (20A/div).

Table 3.2: Loss distribution estimation from the loss model.

Loss type	Power loss (W)	Percentage
Primary switches conduction loss	2.6	1.04%
Primary switches switching loss	1	0.4%
Secondary switches conduction loss	0.2	0.08%
Secondary switch diodes loss	2.5	1%
Secondary switches switching loss	0.11	0.04%
Boost inductor loss	3.6	1.44%
HF transformer loss	2.65	1.05%
Total loss	12.66	5.05%

Loss distribution from the above loss model is shown in Table 3.2. Due to other hidden and constant losses, the efficiency difference exits. It is observed that boost inductor and HF transformer consume a large percentage of total loss. A considerable part of total loss is conduction loss of devices. Compared to similar topologies with active-clamping or RCD snubber, efficiency can be improved nearly 2%.

3.7 Summary and Conclusions

A novel naturally clamped zero current commutated soft-switching bi-directional current-fed dual active bridge (CFDAB) isolated DC/DC converter has been proposed. The steady-state operation, analysis, and design are studied and explained. Simulation and experimental results clearly confirm and demonstrate the claimed ZCC and NVC of primary devices without any snubber. ZCS of primary and ZVS and secondary devices reduces the switching losses significantly. Soft-switching is inherent and load independent. Once ZCC, NVC, and soft-switching are designed to obtain at rated power, it is guaranteed to happen at reduced load unlike voltage-fed PWM and resonant

converters. Turn-on switching transition loss of primary devices is also shown to be negligible. Hence maintaining soft-switching of all devices substantially reduces the switching loss and allows higher frequency of operation to realize a compact and high density design. Proposed secondary modulation achieves natural commutation of primary devices and clamps the device voltage at low voltage (reflected output voltage). The device voltage is independent of duty cycle. It, therefore, eliminates requirement of active-clamp or passive snubbers. Usage of low voltage devices results in low conduction losses in primary devices, which is significant due to higher currents on primary side. The proposed modulation method is simple and easy to implement. Topology is modular, simple to be interleaved and scalable for higher power applications. These merits make the converter promising for interfacing low voltage dc bus with high voltage dc bus for higher current applications such as FCVs, front-end DC/DC power conversion for renewable (fuel cells/PV) inverters, UPS, microgrid, V2G, and energy storage. The specifications are taken for FCV but the proposed modulation, design, and the demonstrated results are suitable for any general application of current-fed converter (high step-up). Similar merits and performance will be achieved.

A closed loop control system is required to maintain a constant dc bus voltage for the following inversion stage while accommodating the varying source voltage, sudden load changes, and system parameters' deviations. The next Chapter deals with the small signal modeling (SSM) and closed loop design for the proposed CFDAB DC/DC converter.

Chapter 4

Small Signal Analysis and Control Design of Zero Current Commutated Current-fed Dual Active Bridge (CFDAB) DC/DC Converter

4.1 Introduction

In Chapter 3, a naturally commutated bidirectional current-fed dual active bridge (CFDAB) isolated DC/DC converter has been proposed. The proposed modulation technique solves the major voltage spike issue associated with current-fed converters. It thus eliminates the need for external active-clamping circuit or passive snubbers. Open-loop study and results have been demonstrated. A closed loop control system is compulsory to maintain a constant output voltage for the following inverter stage to accommodate the varying source voltage, sudden load changes, and system parameters' deviations. Small signal modeling (SSM) is a widely adopted technique to analyze the performance of nonlinear systems such as PWM converters [146]. Small signal model of the converter is important to design closed-loop controller to obtain a good transient performance of the converter [147]. The SSM and closed loop control implementation of the proposed CFDAB DC/DC converter are not yet been researched.

The objectives of this Chapter are to derive small signal model and to design a closed two-loop average current controller to regulate the output voltage of the converter. Small signal model of the converter has been derived using state space averaging in Section 4.2. Closed loop control system employing two-loop average current control approach is designed in Section 4.3. Simulation results using PSIM 9.0.4 is given to verify the controller design and converter performance in Section 4.4. Experimental results from a 250W converter prototype are also demonstrated to show the transient response of the converter for step changes in load. This Chapter is concluded in Section 4.5.

4.2 Small Signal Modeling of the Converter Using State-space Averaging

In this Section, state-space equations for each interval of operation are described. Then small signal ac model is derived based on state-space averaging. For the analysis, the following assumptions are made:

a) All components are assumed to be ideal and lossless.

b) Series inductor L_{lk} includes the leakage inductance of the HF transformer.

c) Magnetizing inductance is infinitely large.

Steady-state operating waveforms are shown in Fig. 4.1, which is the same as Fig. 3.9 of Chapter 3. The charging and discharging durations of the snubber capacitors are very short and therefore are neglected here. The converter operates in continuous conduction mode. Fixed-frequency duty cycle modulation method is used to regulate the output voltage. The equivalent circuits for different interval's operation in a one half cycle are shown in Fig.

4.2. The steady-state equations for these equivalent circuits in a state variable format have been given. Then the state-space averaging is derived by performing the averaging process on the steady-state equations.

State variables defined for the small signal modeling of the converter are: 1) Currents through the input inductor i_L. 2) Transformer or series inductor current i_{Llk}. 3) Output voltage v_o. 4) Input voltage v_{in}.

Interval 1 (Fig. 4.2a; $t_0 < t < t_1$): In this interval, the primary side H-bridge switches S_2 and S_3 and the anti-parallel body diodes D_6 and D_7 of secondary side H-bridge switches are conducting. The current through inductor L_{lk} is negative. Power is transferred to the load through HF transformer. The non-conducting secondary devices S_5 and S_8 are blocking output voltage V_o and the non-conducting primary devices S_1 and S_4 are blocking the reflected output voltage V_o/n. State equations of this interval are:

$$\left(L + L_{lk}\right)\frac{di_L}{dt} = v_{in} - \frac{v_o}{n} \tag{4-1}$$

$$i_{Llk} = -i_L \tag{4-2}$$

$$C_o \frac{dv_o}{dt} = \frac{i_L}{n} - \frac{v_o}{R_L} \tag{4-3}$$

Interval 2 (Fig. 4.2b; $t_1 < t < t_2$): Now all the four primary switches are conducting. Reflected output voltage V_o/n appears across the leakage inductance L_{lk} and causes its current to increase linearly. It causes currents through previously conducting devices S_2 and S_3 to reduce linearly. Switches S_1 and S_4 start conducting with zero current which helps in reducing associated turn-on loss. Since the anti-parallel body diodes D_6 and D_7 are conducting,

switches S_6 and S_7 can be gated for ZVS turn on. State equations for this interval are:

$$L\frac{di_L}{dt} = v_{in} \tag{4-4}$$

$$L_{lk}\frac{di_{Llk}}{dt} = \frac{v_o}{n} \tag{4-5}$$

$$C_o\frac{dv_o}{dt} = -\frac{i_{Llk}}{n} - \frac{v_o}{R_L} \tag{4-6}$$

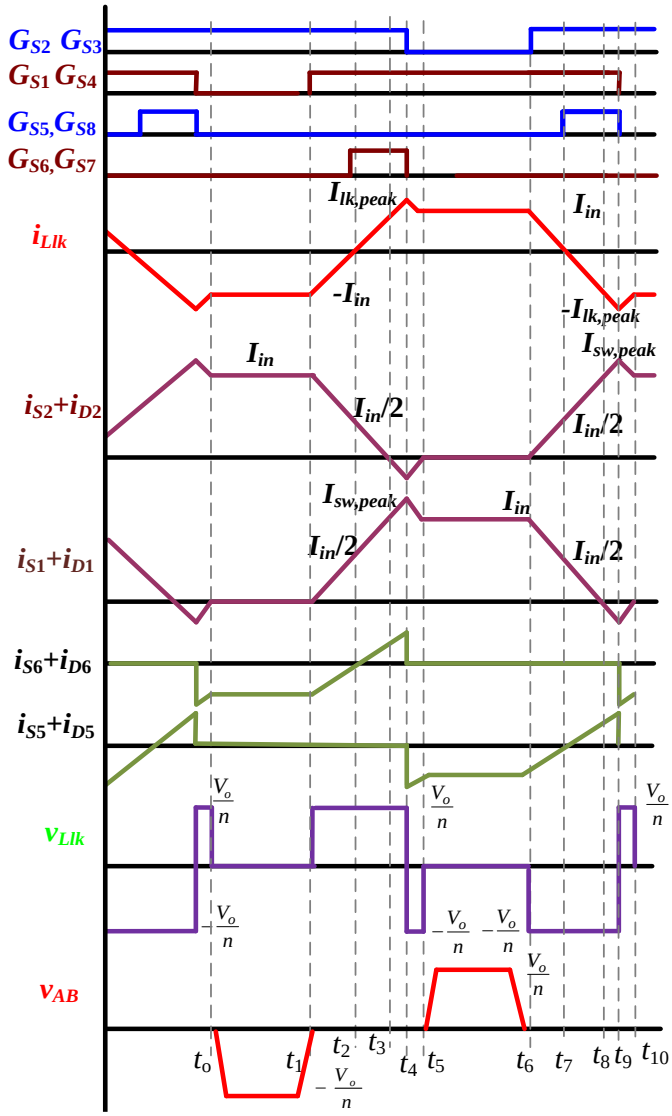


Fig. 4.1. Operating waveforms of proposed zero current commutated CFDAB DC/DC converter.

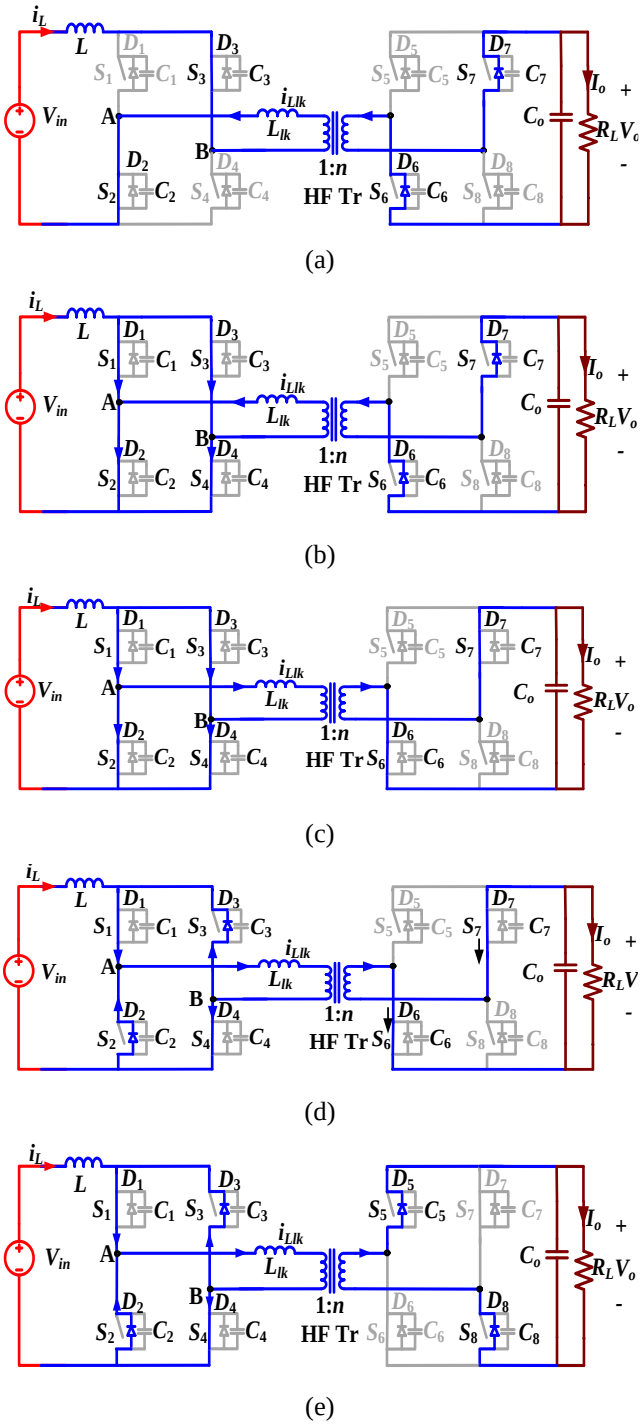


Fig. 4.2. Equivalent circuits during different intervals of operation for the waveforms shown in Fig. 4.1.

Interval 3 (Fig. 4.2c; $t_2 < t < t_3$): In this interval, the secondary H-bridge devices S_6 and S_7 are turned on with ZVS. Currents through all the switching devices continue increasing or decreasing with the same slope as interval 2. At the end of this interval, primary devices S_2 and S_3 commutate naturally and

their respective currents i_{S2} and i_{S3} reach zero obtaining ZCS. The full current, i.e., input current I_{in} is taken over by other devices S_1 and S_4, and the transformer current changes polarity. State equations of interval 2 hold good for this interval too.

Interval 4 (Fig. 4.2d; $t_3 < t < t_4$): In this interval, the primary current or leakage inductance current i_{Llk} increases further with the same slope. Anti-parallel body diodes D_2 and D_3 start conducting causing extended zero voltage to appear across the outgoing or commutated switches S_2 and S_3 to ensure ZCS turn-off. At the end of this interval, currents through the transformer, switches S_1 and S_4 reach their peak value. This interval should be very short to limit the peak current though the transformer and switches, and so their kVA ratings. State equations for this interval are:

$$L\frac{di_L}{dt} = v_{in} \tag{4-7}$$

$$L_{lk}\frac{di_{Llk}}{dt} = \frac{v_o}{n} \tag{4-8}$$

$$C_o\frac{dv_o}{dt} = -\frac{i_{Llk}}{n} - \frac{v_o}{R_L} \tag{4-9}$$

Interval 5 (Fig. 4.2e; $t_4 < t < t_5$): During this interval, the secondary switches S_6 and S_7 are turned-off. Anti-parallel body diodes of switches S_5 and S_8 take over the current immediately. Therefore, the voltage across the transformer primary reverses polarity and the current through it starts decreasing. The currents through the switches S_1 and S_4 and body diodes D_2 and D_3 also start decreasing. At the end of this interval, currents through D_2

and D_3 reduce to zero and are commutated naturally. Currents through S_1 and S_4, and transformer reach I_{in}. State equations for this interval are:

$$L\frac{di_L}{dt} = v_{in} \tag{4-10}$$

$$L_{lk}\frac{di_{Llk}}{dt} = -\frac{v_o}{n} \tag{4-11}$$

$$C_o\frac{dv_o}{dt} = \frac{i_{Llk}}{n} - \frac{v_o}{R_L} \tag{4-12}$$

Similar state equations for the other half cycle can also be derived symmetrically. State equations are averaged over a HF cycle. The average value for the rate of change of i_{Llk} over one complete HF cycle is zero and the averaged state equation is

$$L_{lk}\cdot\left\langle\frac{di_{Llk}}{dt}\right\rangle = 0 \tag{4-13}$$

Therefore the sate variable i_{Llk} is omitted for the following analysis. To simplify the analysis, the effect of L_{lk} over the current variation of input inductor is neglected. Define: $d_1T_s = t_1\text{-}t_o$, $d_2T_s = t_2\text{-}t_1$, $d_3T_s = t_3\text{-}t_2$, $d_4T_s = t_4\text{-}t_3$, $d_5T_s = t_5\text{-}t_4$, $d_6T_s = t_6\text{-}t_5$, $d_7T_s = t_7\text{-}t_6$, $d_8T_s = t_8\text{-}t_7$, $d_9T_s = t_9\text{-}t_8$, $d_{10}T_s = t_{10}\text{-}t_9$. The averaged state equations of defined state variables over a HF cycle are given:

$$L\cdot\left\langle\frac{di_L}{dt}\right\rangle = v_{in} - \left(d_1 + d_6\right)\cdot\frac{v_o}{n} \tag{4-14}$$

$$C_o\cdot\left\langle\frac{dv_o}{dt}\right\rangle = i_{average} - \frac{v_o}{R_L} \tag{4-15}$$

where $i_{average}$ is the average current feeding the output capacitor and load from secondary side H-bridge switches and is given by

$$i_{average} = \frac{i_L}{n} \cdot (d_1 + d_6) \tag{4-16}$$

Substituting (4-16) in (4-15),

$$C_o \cdot \left\langle \frac{dv_o}{dt} \right\rangle = \frac{i_L}{n} \cdot (d_1 + d_6) - \frac{v_o}{R_L} \tag{4-17}$$

The duty ratio of the main switches including conduction of the reverse anti-parallel diodes are defined as

$$d = d_{S1} = d_{S4} = d_2 + d_3 + d_4 + d_5 + d_6 + d_7 + d_8 + d_9 \tag{4-18}$$

$$d = d_{S2} = d_{S3} = d_1 + d_2 + d_3 + d_4 + d_7 + d_8 + d_9 + d_{10} \tag{4-19}$$

The turn-off durations of the main switches are

$$1 - d = d_5 + d_6 = d_1 + d_{10} \tag{4-20}$$

The extended body diodes conduction durations of main switches are (half of the total conduction time of corresponding body diodes)

$$d'' = d_5 = d_{10} \tag{4-21}$$

Where d'' is given by,

$$d'' = d - 0.5 - \frac{2 \cdot n \cdot i_L \cdot L_{lk} \cdot f_s}{V_o} \tag{4-22}$$

where f_s is the switching frequency, n is the turns ratio of HF transformer.

The state equations can be simplified as shown in the following equations in terms of above defined duty cycles ratios.

$$L\left\langle \frac{di_L}{dt} \right\rangle = v_{in} - 2 \cdot (1 - d - d'') \cdot \frac{v_o}{n} \tag{4-23}$$

$$C_o \cdot \left\langle \frac{dv_o}{dt} \right\rangle = 2 \cdot \frac{i_L}{n} \cdot (1 - d - d'') - \frac{v_o}{R_L} \tag{4-24}$$

$$d'' = d - 0.5 - \frac{2 \cdot n \cdot i_L \cdot L_{lk} \cdot f_s}{v_o} \tag{4-25}$$

Introducing perturbation around the steady state values of the state variables and input voltage such that, $i_L = I_L + \hat{i}_L$, $v_{in} = V_{in} + \hat{v}_{in}$, $v_o = V_o + \hat{v}_o$, $d = D + \hat{d}$ and $d'' = D'' + \hat{d}''$. And the state equations are modified as following

$$L\frac{d\left(I_L + \hat{i}_L\right)}{dt} = \left(V_{in} + \hat{v}_{in}\right) - 2 \cdot \left(1 - D - \hat{d} - D'' - \hat{d}''\right) \cdot \frac{V_o + \hat{v}_o}{n} \tag{4-26}$$

$$C_o\frac{d\left(V_o + \hat{v}_o\right)}{dt} = \frac{2 \cdot \left(I_L + \hat{i}_L\right)}{n} \cdot \left(1 - D - \hat{d} - D'' - \hat{d}''\right) - \frac{\left(V_o + \hat{v}_o\right)}{R_L} \tag{4-27}$$

$$\left(D + \hat{d} - 0.5 - D'' - \hat{d}''\right) \cdot \left(V_o + \hat{v}_o\right) = 2 \cdot n \cdot \left(I_L + \hat{i}_L\right) \cdot L_{lk} \cdot f_s \tag{4-28}$$

Neglecting the second order terms and the steady state or dc terms, results in the following equations.

$$L\frac{d\hat{i}_L}{dt} = \hat{v}_{in} - 2 \cdot \left(1 - D - D''\right) \cdot \frac{\hat{v}_o}{n} + 2 \cdot \left(\hat{d} + \hat{d}''\right) \cdot \frac{V_o}{n} \tag{4-29}$$

$$C_o\frac{d\hat{v}_o}{dt} = \frac{2 \cdot \hat{i}_L}{n} \cdot \left(1 - D - D''\right) - \frac{2 \cdot I_L}{n} \cdot \left(\hat{d} + \hat{d}''\right) - \frac{\hat{v}_o}{R_L} \tag{4-30}$$

$$\left(D - 0.5 - D''\right) \cdot \hat{v}_o + \left(\hat{d} - \hat{d}''\right) \cdot V_o = 2 \cdot n \cdot L_{lk} \cdot f_s \cdot \hat{i}_L \tag{4-31}$$

Arranging (4-31) results in

$$\hat{d}'' = \frac{\left(D - 0.5 - D''\right) \cdot \hat{v}_o}{V_o} + \hat{d} - \frac{2 \cdot n \cdot L_{lk} \cdot f_s \cdot \hat{i}_L}{V_o} \tag{4-32}$$

Eliminating $\hat{d}''$ using (4-32) gives

$$L\frac{d\hat{i}_L}{dt} = \hat{v}_{in} + \frac{4D - 3}{n} \cdot \hat{v}_o + \frac{4 \cdot V_o}{n} \cdot \hat{d} - 4 \cdot L_{lk} \cdot f_s \cdot \hat{i}_L \tag{4-33}$$

$$C_o \frac{d\hat{v}_o}{dt} = -\frac{4 \cdot I_L}{n} \cdot \hat{d} - \left[\frac{2 \cdot I_L \cdot \left(\mathrm{D} - 0.5 - D'' \right)}{n \cdot V_o} + \frac{1}{R_L} \right] \cdot \hat{v}_o + \left[\frac{4 \cdot I_L \cdot L_{lk} \cdot f_s}{V_o} + \frac{2 \cdot \left(1 - D - D'' \right)}{n} \right] \cdot \hat{i}_L \quad (4\text{-}34)$$

Taking Laplace transform results in the following equations

$$(4 \cdot L_{lk} \cdot f_s + Ls) \cdot \hat{i}_L(s) - \frac{4D-3}{n} \cdot \hat{v}_o(s) = \frac{4 \cdot V_o}{n} \cdot \hat{d}(s) + \hat{v}_{in}(s) \quad (4\text{-}35)$$

$$\left[\frac{4 \cdot I_L \cdot L_{lk} \cdot f_s}{V_o} + \frac{2 \cdot \left(1 - D - D'' \right)}{n} \right] \cdot \hat{i}_L(s) - \left[\frac{2 \cdot I_L \cdot \left(\mathrm{D} - 0.5 - D'' \right)}{n \cdot V_o} + \frac{1}{R_L} + C_o s \right] \cdot \hat{v}_o(s) = \frac{4 \cdot I_L}{n} \cdot \hat{d} \quad (4\text{-}36)$$

Writing in matrix form

$$\begin{bmatrix} \hat{i}_L(s) \\ \hat{v}_o(s) \end{bmatrix} = [A(s)] \cdot \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} \cdot \hat{d}(s) + [A(s)] \cdot \begin{bmatrix} 1 \\ 0 \end{bmatrix} \cdot \hat{v}_{in}(s) \quad (4\text{-}37)$$

where $b_1 = \frac{4 \cdot V_o}{n}$, $b_2 = \frac{4 \cdot I_L}{n}$.

$$A(s) = \begin{bmatrix} 4 \cdot L_{lk} \cdot f_s + Ls & -\frac{4D-3}{n} \\ \frac{4 \cdot I_L \cdot L_{lk} \cdot f_s}{V_o} + \frac{2 \cdot \left(1 - D - D'' \right)}{n} & -\left[\frac{2 \cdot I_L \cdot \left(\mathrm{D} - 0.5 - D'' \right)}{n \cdot V_o} + \frac{1}{R_L} + C_o s \right] \end{bmatrix}^{-1}$$

The matrix A(s) is represented as follow

$$A(s) = \frac{1}{|A(s)|} \cdot \begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix}$$

$$A_{11} = -\left[\frac{2 \cdot I_L \cdot \left(\mathrm{D} - 0.5 - D'' \right)}{n \cdot V_o} + \frac{1}{R_L} + C_o s \right]$$

$$A_{12} = \frac{4D-3}{n}$$

$$A_{21} = -\left[\frac{4 \cdot I_L \cdot L_{lk} \cdot f_s}{V_o} + \frac{2 \cdot \left(1 - D - D'' \right)}{n} \right]$$

$$A_{22} = 4 \cdot L_{lk} \cdot f_s + L \cdot s$$

$$|A(s)| = -(L \cdot C_o) \cdot s^2 - \left[\frac{2 \cdot L \cdot I_L \cdot \left(\mathrm{D} - 0.5 - D''\right)}{n \cdot V_o} + \frac{L}{R_L} + 4 \cdot L_{lk} \cdot f_s \cdot C_o \right] \cdot s -$$

$$4 \cdot L_{lk} \cdot f_s \cdot \left[\frac{2 \cdot I_L \cdot \left(\mathrm{D} - 0.5 - D''\right)}{n \cdot V_o} + \frac{1}{R_L} \right] + \frac{4D - 3}{n} \cdot \left[\frac{4 \cdot I_L \cdot L_{lk} \cdot f_s}{V_o} + \frac{2 \cdot \left(1 - D - D''\right)}{n} \right]$$

Control-to-output Transfer Function

From (4-36), the control-to-output transfer function is obtained by setting $\hat{v}_{in} = 0$. It results in the following equation

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{1}{|A(s)|} \cdot \begin{bmatrix} A_{21} & A_{22} \end{bmatrix} \cdot \begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \frac{N_1(s)}{|A(s)|} \tag{4-38}$$

where, $N_1(s) = \dfrac{4 \cdot I_L \cdot L}{n} \cdot s - \dfrac{8 \cdot V_o \cdot \left(1 - D - D''\right)}{n^2}$

4.3 Controller Design: Two Loop Average Current Control

In this Section, the two-loop average current control design procedure is illustrated. The specifications of the converter: input voltage V_{in} = 12 V, output voltage V_o = 300V, output power P_o = 250W, switching frequency f_s = 100 kHz, leakage inductor or series inductor L_{lk} = 2 μH, boost inductor L = 18 μH, transformer turns ratio n = 10, output capacitor C_o = 220 μF, full-load resistance R_L = 360 Ω.

Bode plot of the control-to-output voltage transfer function given by (4-38) is given in Fig. 4.3. It is easy to find that phase margin (PM) and gain margin (GM) of the system without controller are negative. This makes the system sensitive to small disturbances in input or source voltage and/or load.

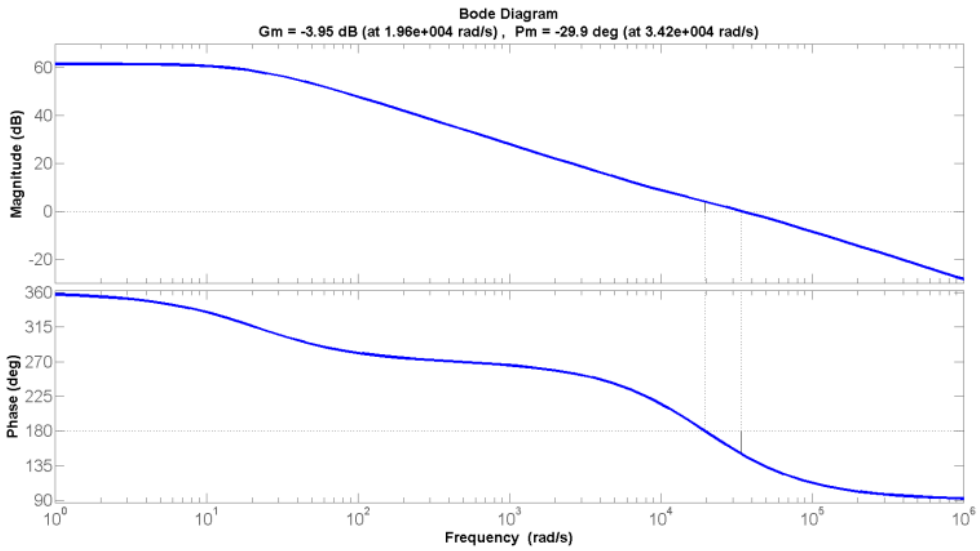


Fig. 4.3. Control to output voltage transfer function of the system without controller.

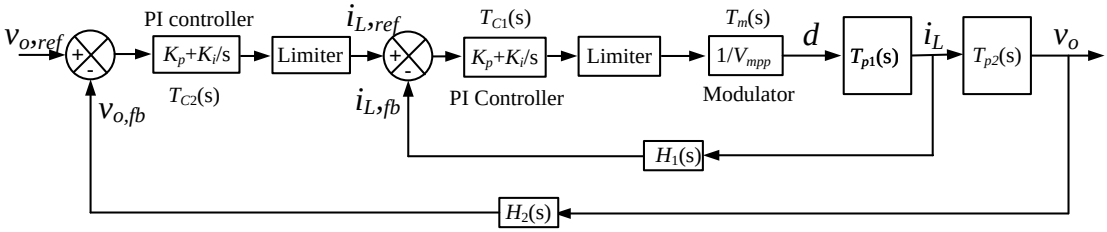


Fig. 4.4. Complete two-loop average current control system schematic diagram.

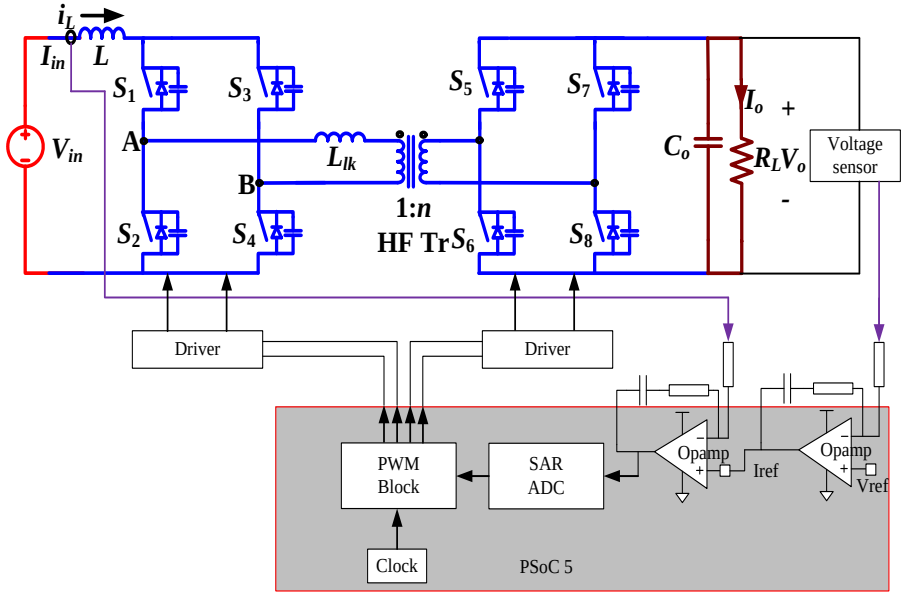


Fig. 4.5. Block diagram showing closed loop control system.

A closed two-loop controller is proposed to regulate the output voltage. The schematic diagram of two-loop control system is shown in Fig. 4.4, which

consists of outer voltage control loop and inner current control loop. Two loops are designed separately. Outer voltage loop bandwidth (BW) is set much lower than the inner current loop, which simplifies the design [148-149]. Therefore the inner current loop has fast dynamics with higher BW than the outer voltage loop. The inductor current is able to change more quickly than the output voltage.

The overall control system has been implemented using Programmable System-on-Chip 5 (PSoC) from Cypress Semiconductor [150] as shown by the block diagram in Fig. 4.5. PSoC provides unique array of configurable blocks including MCU, memory, analog peripheral (ADC, OPAMPs, analog MUX and configurable digital filters) and digital peripheral functions (timer, counter and PWM blocks) in a single chip. This feature makes it quite convenient in power electronics design. As shown by the Fig. 4.5, PI controllers have been realized using OPAMPs with external passive elements like resistor, capacitors and zener diodes. Analog output acquired at the output of the current controller is converted to digital using successive approximate register (SAR) ADC. This digital value is used to control the PWM block to generate gate signals of 100 kHz. Duty ratio is calculated according to the value obtained from the ADC. Voltage control loop regulates the output voltage by generating reference for the input inductor current, $i_{L,ref}$. Inductor current i_L is tuned to this reference value by adjusting the duty ratio of the switches.

4.3.1 Design of Current Control Loop:

The schematic diagram of the inner current control loop is shown in Fig. 4.6. Input inductor current is fed back to the error amplifier with the gain of

H_1(s). Output of the PI controller is sent to the modulator to generate the gating signals. Then inductor current i_L is regulated by adjusting the duty ratio of the switches.

Duty ratio to the inductor current transfer function is derived from (4-37) and given by,

$$\frac{\hat{i}_L(s)}{\hat{d}(s)} == \frac{1}{|A(s)|}\cdot\begin{bmatrix}A_{11} & A_{12}\end{bmatrix}\cdot\begin{bmatrix}b_1\\ b_2\end{bmatrix} = \frac{N_2(s)}{|A(s)|} \tag{4-39}$$

where, $N_2(s) = -\frac{4\cdot V_o\cdot C_o}{n}\cdot s - \frac{4\cdot V_o}{n}\cdot\left[\frac{2\cdot I_L\cdot\left(\mathrm{D}-0.5-D''\right)}{n\cdot V_o}+\frac{1}{R_L}\right]+\frac{4\cdot I_L}{n}\cdot\frac{4D-3}{n}$

For the given specifications, duty ratio to inductor current transfer function is given by,

$$T_{p1}(s) = \frac{\hat{i}_L(s)}{\hat{d}(s)} = \frac{0.0264s + 0.667}{7.92\times10^{-6}s^2 + 0.00019s + 0.004} \tag{4-40}$$

Frequency response curve of current loop without controller is plotted in Fig. 4.7, which shows a PM = 92.2 °at 628krad/s. Thus PI controller is needed to achieve stability and meet response criteria over a certain range. A PI controller is designed to increase the low frequency gain and reduce the steady-state error between the desired and actual inductor current.

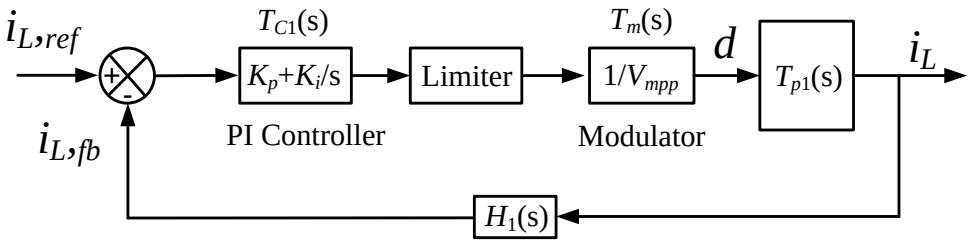


Fig. 4.6. Inner current control loop schematic diagram.

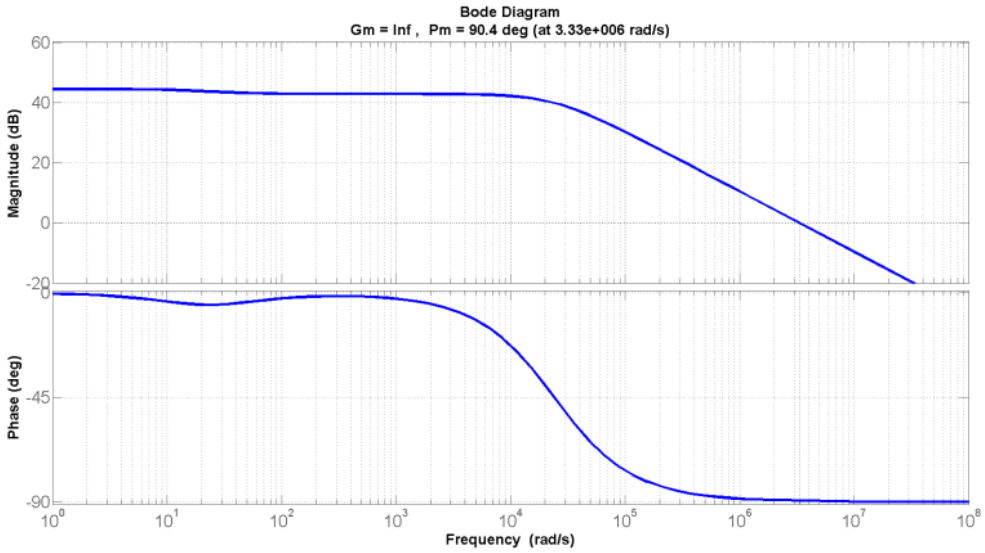


Fig. 4.7. Bode plot of current control loop without controller: PM=92.2 °at 628krad/s.

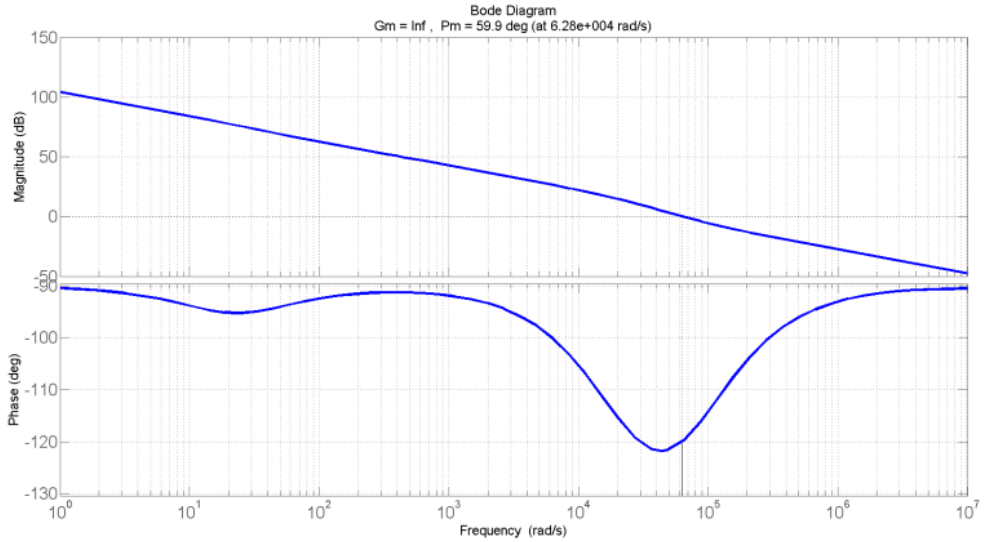


Fig. 4.8. Bode plot of current control loop with PI controller: PM=59.9 °at f_c=62.8krad/s.

Transfer function of a PI controller is given by,

$$T_{C1}(s) = K_p + \frac{K_i}{s} = \frac{K_p(s + K_i / K_p)}{s} \tag{4-41}$$

Open loop transfer function of the current loop is given by,

$$T_{OL1}(s) = T_{C1}(s) \cdot T_m(s) \cdot T_{p1}(s) \cdot H_1(s) \tag{4-42}$$

Where $H_1(s)$ is the current feedback gain and $T_m(s)$ is the overall gain of the designed modulator.

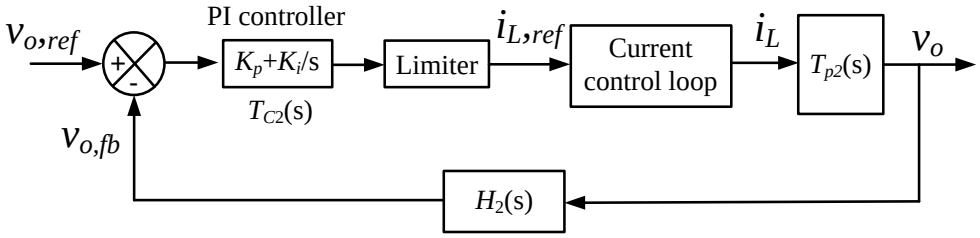


Fig. 4.9. Outer voltage control loop schematic diagram.

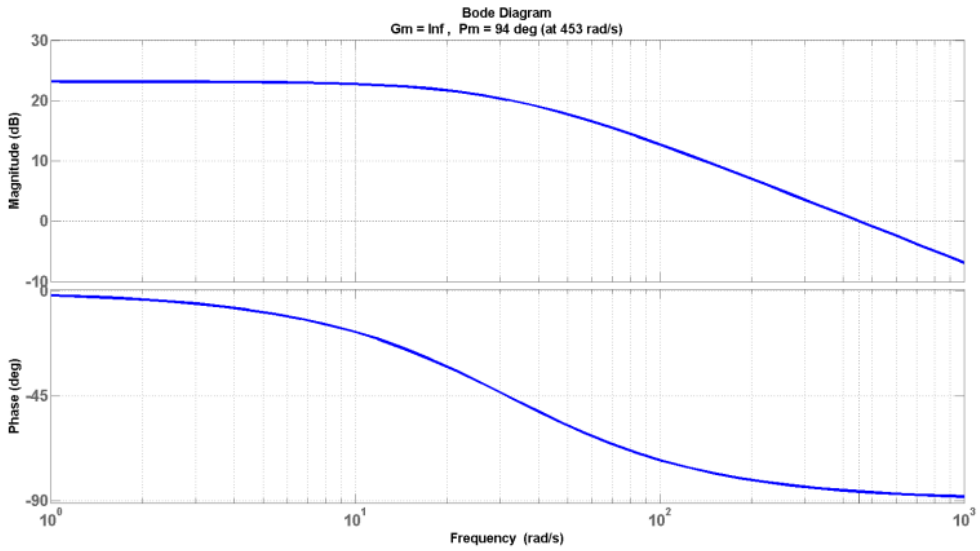


Fig. 4.10. Bode plot of voltage control loop without controller: PM=94 ºat 453 rad/s.

LEM sensor LA25-NP is used to sense the inductor current and to provide the isolation between power circuit and controller. Here current feedback gain is chosen as $H_1(s)$ =1/10.

The voltage signal at the output of the current controller (limited to the range of 0 to 3.3V) is converted from analog to digital and used to control duty ratio of PWM blocks. They work together serving as the modulator. The duty ratio of the primary switches is restricted to the range or 0.55 to 0.8. Considering the gain of ADC (the modulator phase lag introduced by conversion delay of ADC has been neglected) and subsequent digital process, overall gain of the modulator is given as,

$$T_m(s) = \frac{1}{13.2} \tag{4-43}$$

For the given specifications, open loop transfer function of the current loop is given by,

$$T_{OL1}(s) = \frac{K_p\left(s + K_i / K_p\right)}{s} \cdot \frac{0.0002s + 0.005}{7.92 \times 10^{-9} s^2 + 0.00019s + 0.004} \tag{4-44}$$

PI controller parameters are designed to obtain PM of 60 º[151] at the gain crossover frequency of 10 kHz (62.83krad/s). It results in the gain K_p and integrator time constant K_p/K_i as 1.69 and 13.4 μs respectively. Bode plot for current control loop with designed PI controller is shown in Fig. 4.8. PM=59.9 ºis achieved at f_c=10 kHz. Low frequency gain is improved.

4.3.2 Voltage Control Loop:

Outer voltage control loop regulates the output voltage at the reference value by setting inductor current reference as shown in Fig. 4.9. Inner current control loop has faster dynamics compared to outer voltage loop. Hence, the current loop dynamics are neglected during the design of voltage controller [152]. Its transfer function is not included and the perturbation in duty cycle can be neglected. Therefore, inductor current to output voltage transfer function T_{p2}(s) is obtained as

$$T_{p2}(s) = \frac{\hat{v}_o(s)}{\hat{i}_L(s)} = \frac{\frac{4 \cdot I_L \cdot L_{lk} \cdot f_s}{V_o} + \frac{2 \cdot \left(1 - D - D''\right)}{n}}{C_o s + \frac{2 \cdot I_L \cdot \left(D - 0.5 - D''\right)}{n \cdot V_o} + \frac{1}{R_L}} = \frac{0.1}{0.00022s + 0.00694} \tag{4-45}$$

LEM sensor LV25-P is used to sense output voltage and also to provide the necessary isolation. Here voltage feedback gain is chosen as

$$H_2(s) = \frac{1}{200} \tag{4-46}$$

PI controller transfer function $T_{C2}(s)$ is given by (4-40).

Overall open loop transfer function of the voltage loop is given by,

$$T_{OL2}(s) = T_{C2}(s) \cdot T_{p2}(s) \cdot H_2(s) \cdot \frac{1}{H_1(s)} \tag{4-47}$$

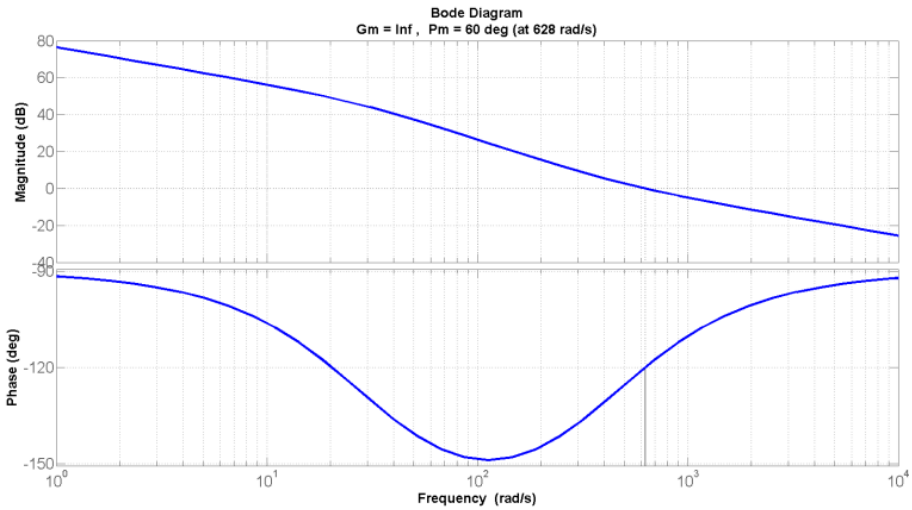


Fig. 4.11. Bode plot of voltage control loop with PI controller: PM=60 °at f_c=628rad/s.

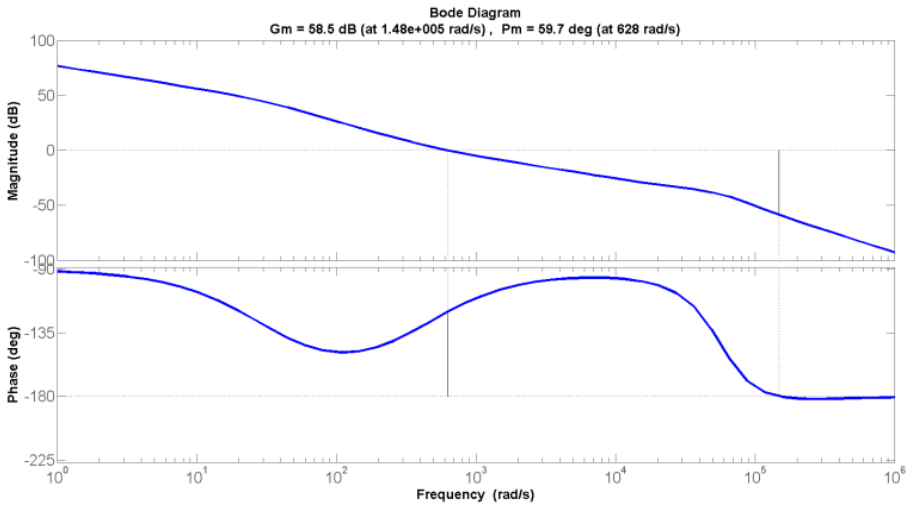


Fig. 4.12. Frequency response of the overall system with both the current and the voltage controllers.

$$T_{OL2}(s) = \frac{K_p\left(s + K_i / K_p\right)}{s} \cdot \frac{0.005}{0.00022s + 0.00694} \tag{4-48}$$

Fig. 4.10 shows the bode plot of voltage control loop without controller indicating PM of 94 º at 453 rad/s. Gain crossover frequency for voltage controller is selected 100 times slower than that of inner current loop. Hence the phase margin should be 60 ºat the gain crossover frequency of 100 Hz (628 rad/s). It results in the gain K_p and integrator time constant K_p/K_i as 23.2 and 2.46ms respectively. Required PM is achieved from this design of PI parameters, which can be observed from the frequency response of voltage control loop in Fig. 4.11.

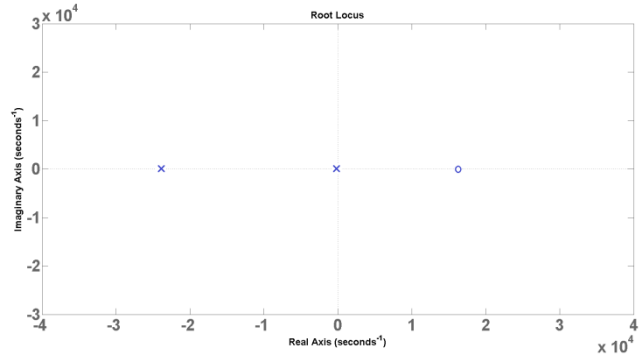
Taking into account dynamics of current control loop, overall transfer function of the system can be written as given in (4-49).

$$T_{OL}(s) = \left[\frac{T_{C1}(s) \cdot T_{p1}(s) \cdot T_m(s) \cdot H_1(s)}{1 + T_{C1}(s) \cdot T_{p1}(s) \cdot T_m(s) \cdot H_1(s)}\right] \cdot T_{C2}(s) \cdot T_{p2}(s) \cdot H_2(s) \cdot \frac{1}{H_1(s)} \tag{4-49}$$

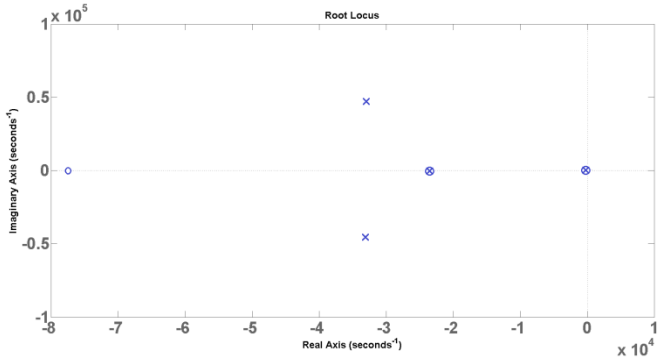
Bode plot for the overall system T_{OL}(s) has been drawn as shown in Fig. 4.12. Gain at lower frequency is high indicating zero steady state error. The PM of 59.7 ºat 628rad/s has been achieved resulting in a stable system with better control against disturbances.

The pole-zero maps of control-to-output transfer function without controller in (4-38) and with the complete two-loop control system (4-49) are plotted in Fig. 4.13. It should be observed from Fig. 4.13 (a) that control-to-output transfer function has right-half-plane (RHP) zero, which is the common in boost-type converter, and may limit the system dynamic response and introduce instability. The root-locus of open-loop converter is very close to

imaginary axis, the stability margin will be limited. It should be noticed from Fig. 4.13 (b) that with complete closed two-loop controller, nearly imaginary poles and RHP zeros have been eliminated, thus increasing the stability of the compensated system .



(a)



(b)

Fig. 4.13. Pole-zero maps of: (a) control to output voltage transfer function of the system without controller (equation 4-38); (b) the overall system with both the current and the voltage controllers (equation 4-49).

4.4 Simulation and Experimental Results

Simulation has been carried out using software package PSIM 9.0.4 based on controller design in Section 4.3. Simulation results are illustrated in Fig. 4.14 to Fig. 4.15. The output load is changed from 100% to 50% and vice versa. It can be observed that the overshoot or undershoot of output voltage is less than 1.5V for both step changes in load. Similarly, the overshot and undershoot in the boost inductor current is also within reasonable limit during

transient of sudden load changes. The settling time of both input boost inductor current and output voltage is around 20ms. These excellent transient performances allow the converter to operate continuously and safely.

A 250W experimental prototype with the designed controller has been built. Performance of experimental prototype driven by the designed controller has been tested for step changes in load for fixed 12V input voltage. Fig. 4.16 to Fig. 4.17 give the variations of inductor current i_L, voltage V_{AB}, output voltage V_O and output current i_O with respect to time for step change in load from full load to half load. The same waveforms for step change in load from half load to full load are shown in Fig. 4.18 to Fig. 4.19. It is clearly shown that output voltages remains constant with negligible overshoot and undershoot in spite of step changes in load. The variations of inductor current i_L and output current i_O are also within safe limiting values. During the transient time period, the voltage V_{AB} is unaffected. Hence, the switches do not experience any high voltage stress during transition ensuring safe operation of switches.

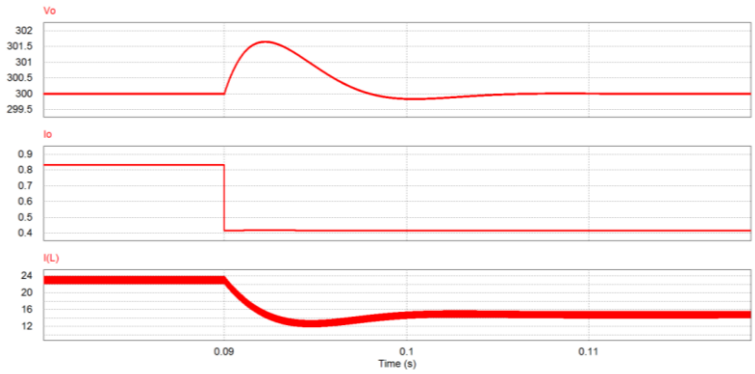


Fig. 4.14. Simulation waveforms for V_{in}=12V with step change in load from full load to half load.

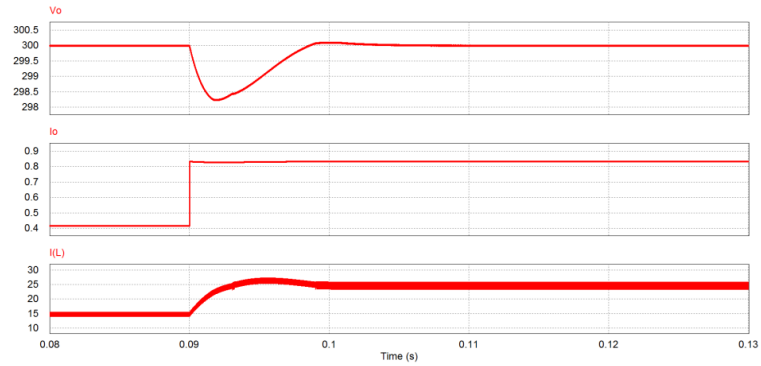


Fig. 4.15. Simulation waveforms for V_{in}=12V, step change in load from half load to full load.

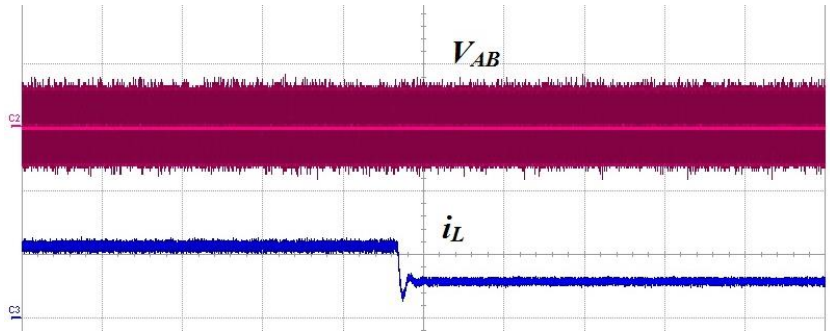


Fig. 4.16. Experimental results for step change in load from full load to half load (200ms/div): (1) Voltage V_{AB} (50V/div), (2) Inductor current i_L (20A/div).

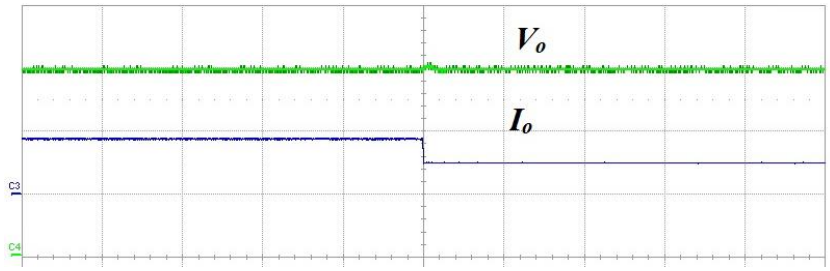


Fig. 4.17. Experimental results for step change in load from full load to half load (100ms/div): (1) Output voltage V_O (100V/div), (2) Output current i_O (1A/div).

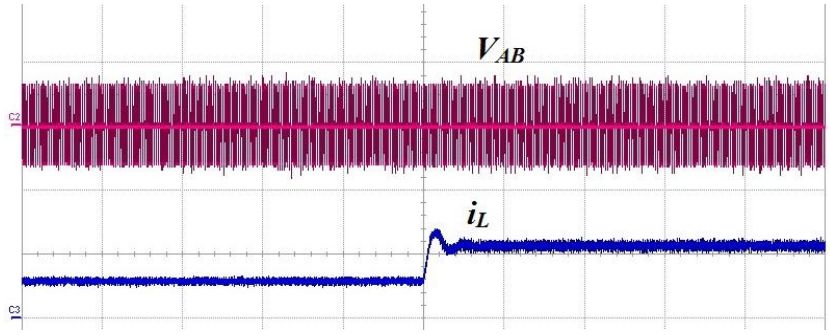


Fig. 4.18. Experimental results for step change in load from half load to full load (100ms/div): (1) Voltage V_{AB} (50V/div), (2) Inductor current i_L (20A/div).

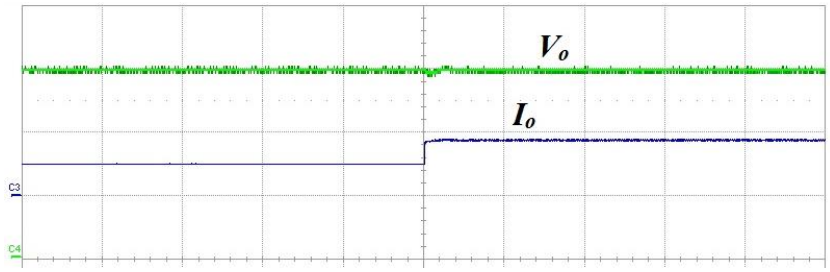


Fig. 4.19. Experimental results for step change in load from half load to full load (100ms/div): (1) Output voltage V_O (100V/div), (2) Output current i_O (1A/div).

4.5 Summary and Conclusions

Small signal model of naturally commutated current-fed full-bridge isolated DC/DC converter using state-space averaging method is derived. A closed two-loop controller is designed and implemented on mixed signal processor Cypress PSoC 5, which is compact, flexible and easy to configure. Average current control with fixed frequency duty cycle modulation is employed. The designed controller regulates the output voltage and currents by automatically adjusting the duty cycle of semiconductor devices. A detailed procedure to design the inner current control loop and the outer voltage loop are discussed for the given system specification. Two PI controllers are designed to meet the set frequency response requirements. Simulation results using PSIM 9.0.4 are presented. The designed controller is implemented and tested for a converter prototype of 250W. Experimental results are demonstrated to show the transient performance of the converter with the controller.

Chapter 5

Modular Multi-cell Current-fed Full-bridge Voltage Doubler (CF-FBVD) Bidirectional DC/DC Converter

5.1 Introduction

In Chapters 3 and 4, a novel current-fed dual active bridge (CFDAB) is proposed and studied for fuel cell applications with innovative secondary side modulation with zero current commutation. Small signal modeling (SSM) and transfer functions are derived for the closed loop control. In this Chapter, multi-cell bidirectional current-fed full-bridge voltage doubler (CF-FBVD) converter is explored for higher power applications.

For the rapid commercialization of renewables and electric transportation, power electronics plays a significant role. To scale the system for high power applications, modular power electronics need to be researched and developed. Modular power electronics provide the following features and advantages [153]:

- Scalability
- Modularity
- High reliability
- Manufacturability in high volume

Power Electronics Building Block (PEBB) is a broad concept towards designing modular power electronic systems incorporating the integration of power devices, gate drives, and other components to functional blocks [154-155]. The adoption of functional building blocks simplifies the design, testing, onsite installation, and maintenance work for different specific customer applications. With the standardization of interfaces of the building blocks, control, or protection requirements, the value of PEBB can be enhanced [153-154]. The first step of designing PEBB is to investigate generalized modular power electronic topologies. It should be modular in nature and capable of scaling up/down to address different specifications such as the device stresses, and power rating for a broad set of applications. The objective of this Chapter is to present a generalized modular power electronic topology and to develop a bidirectional DC/DC converter for low voltage high current applications. This Chapter is outlined as follows: In Section 5.2, various typical HF transformer isolated DC/DC converters are discussed and compared for the given specifications. The merits of the proposed CF-FBVD are illustrated. Six different configurations of CF-FBVD for different applications are listed and discussed in Section 5.3. Section 5.4 describes the converter's steady state operation. A complete design procedure is implemented in Section 5.5. The performance is evaluated by experimental results obtained from a 500 W prototype in Section 5.6. The Chapter is concluded in Section 5.7.

5.2 Study of Bidirectional DC/DC Converters

Various bidirectional HF transformer isolated DC/DC converter topologies have been discussed in Chapter 2. In this Section, four possible

DC/DC converter configurations including voltage-fed dual active full-bridge (VF-DAB) [156-157], current-fed dual active half-bridge (CF-DAHB) [142], current-fed dual active full-bridge (CF-DAFB) with active-clamp [158-160] and the proposed current-fed full-bridge voltage doubler (CF-FBVD) are designed, discussed, and compared. The design for each converter follows the specifications below:

Input voltage (from the ESS) V_{in}=12V.

Output voltage (dc bus voltage) V_o=300V.

Output power P_o=1kW

Switching frequency f_s=100 kHz.

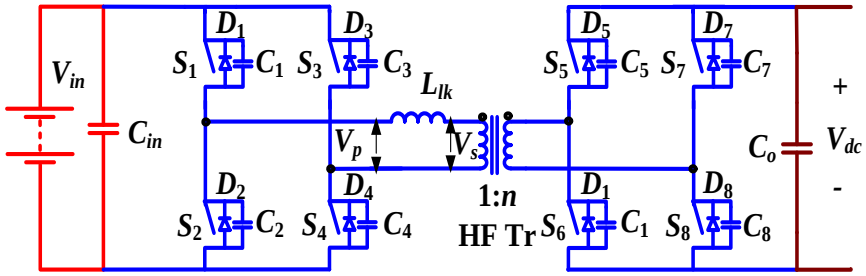


Fig. 5.1. VF-DAB DC/DC converter.

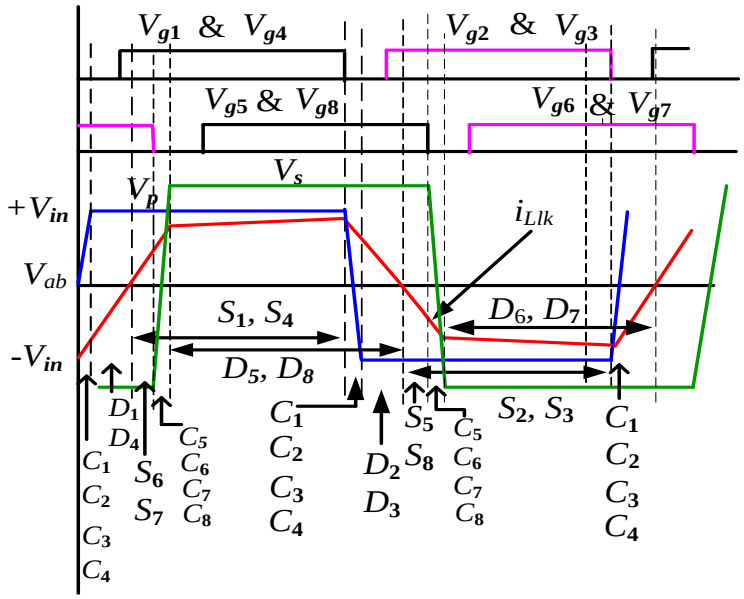


Fig. 5.2. Operating waveforms of secondary controlled VF-DAB DC/DC converter.

5.2.1 Voltage-fed Dual Active Full-Bridge (VF-DAB) DC/DC Converter

Fig. 5.1 shows VF-DAB isolated DC/DC converter. Its steady-state operating waveforms are shown in Fig. 5.2. Primary-side switches are operated by a fixed gating pattern. The secondary bridge is controlled to produce phase difference between primary voltage (v_p) and secondary voltage (v_s) of the HF transformer to regulate the output voltage against variations in load and source voltage [156-157]. This converter has been analyzed in [156-157]. All primary switches are expected to achieve ZVS for all input voltage and load conditions if $nv_p > V_o$. n=secondary to primary turns ratio of transformer.

Based on the analysis and design procedure given in [156-157], the components' values calculated for the given specifications are: n = 25, L_{lk}= 0.5 µH, C_1- C_4 = 0.68 nF, C_5- C_8 = 0.12 nF, C_o = 50 µF, f_s=100 kHz.

5.2.2 Current-fed Dual Active Half-Bridge (CF-DAHB) DC/DC Converter

The circuit diagram and operating waveforms of CF-DAHB are shown in Fig. 5.3 and Fig. 5.4, respectively. The number of switching devices is minimized compared to the conventional full-bridge bidirectional DC/DC converters. Converter achieves ZVS in both directions of power flow.

The converter is designed based on the analysis and design given in [142]. The components values calculated for the given specifications are: n=12.5, L_{lk}= 0.4 µH, L=7.5 µH, C_1- C_2 = 2.89 nF, C_3- C_4= 0.12 nF, C_{o1}- C_{o4} = 50uF, f_s=100 kHz..

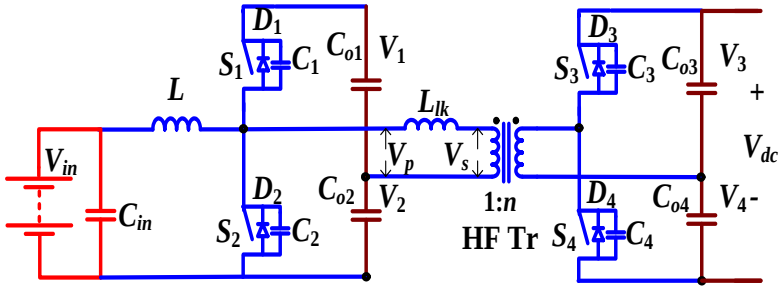


Fig. 5.3. CF-DAHB DC/DC converter.

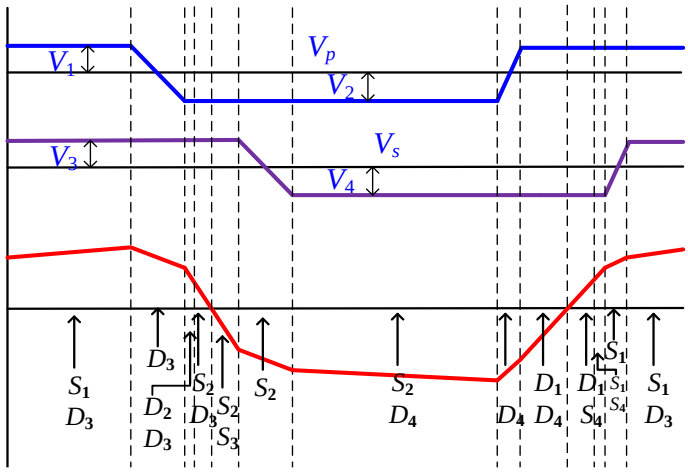


Fig. 5.4. Operating waveforms of CF-DAHB DC/DC converter.

5.2.3 Current-fed Dual Active Full-Bridge (CF-DAFB) DC/DC Converter with Active-clamp

Fig. 5.5 and Fig. 5.6 show the circuit diagram and operating waveforms respectively, for the CF-DAFB DC/DC converter with auxiliary active-clamping circuit. The active-clamping circuit is added to absorb device turn-off voltage spike and assist in soft-switching. ZVS of main as well as auxiliary circuit devices are achieved.

The complete analysis and design of this converter have been presented in [158-160] and the calculated components values are n=12.5, L_{lk}= 0.2 µH, L=4.5 µH, C_1- C_4 = 1nF, C_5- C_8 = 0.12 nF, C_o = 50 µF, f_s=100 kHz.

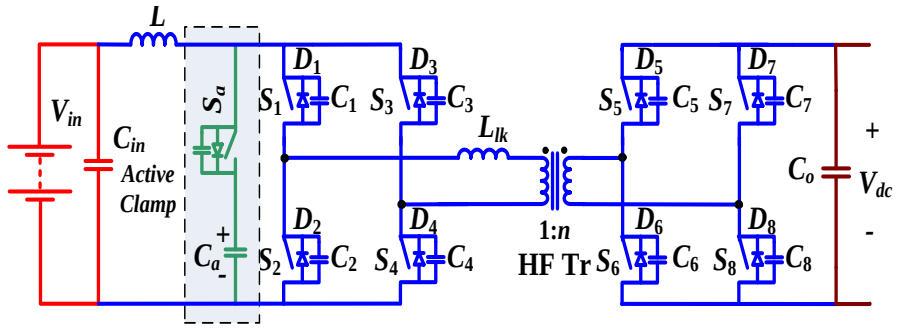


Fig. 5.5. CF-DAFB DC/DC converter with active-clamp.

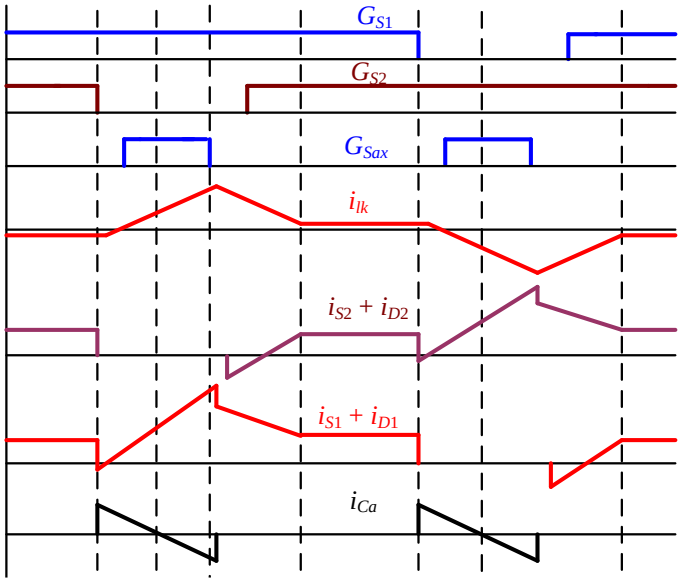


Fig. 5.6. Operating waveforms of CF-DAFB DC/DC converter with active-clamp.

5.2.4 Secondary Modulation Based Current-fed Full-Bridge Voltage Doubler (CF-FBVD)

In Chapter 3, a novel secondary modulation based zero current commutated naturally clamped soft-switching bidirectional current-fed dual active bridge (CFDAB) converter has been proposed, eliminating the need for an active-clamp or passive snubbers. Switching losses are reduced significantly owing to ZCS of primary switches and ZVS of secondary switches that also permits higher switching frequency operation with reduced magnetics. The proposed topology has reduced circulating current and switching losses and therefore, is expected to show better part-load efficiency

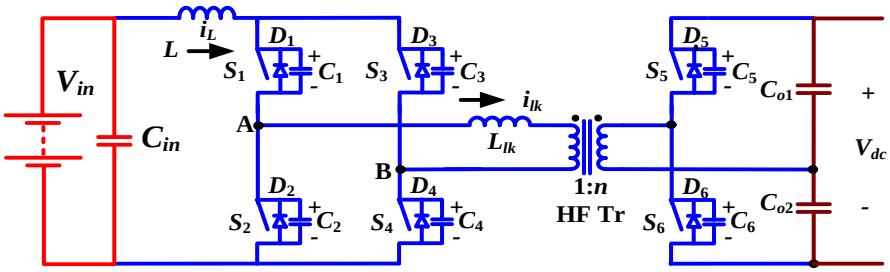


Fig. 5.7. Proposed secondary modulation based CF-FBVD DC/DC Converter

than hard-switching and active-clamp current-fed converters. In forward direction, the converter acts as an isolated boost (current-fed full-bridge) converter and in reverse direction, the converter acts as voltage-fed DC/DC converter with inductive output filter. Here, voltage doubler or half-bridge is selected to reduce number of switches, the transformer turns ratio, and voltage ratings of secondary side devices as illustrated by Fig. 5.7.

The design has already been given in Chapter 3. Calculated components' values are: n=5, L_{lk}= 0.5 µH, L=4.5 µH, C_1- C_4 = 1nF, C_5- C_6 = 0.3 nF, C_o = 50 µF, f_s=100 kHz.

5.2.5 Comparison and Selection

Table 5.1 gives a comparison of these four bidirectional isolated converter topologies in terms of the number of components, voltage and current ratings, soft switching range, etc., for the above mentioned specifications. Though CF-DAHB topology has the least number of active components, the total device rating (TDR) of primary switches is very high with current carrying capacity of up to 3x the battery current. Another drawback of this topology is that four split capacitors are required. These four split dc capacitors have to handle full load current, and occupy a considerable

volume of the converter. CF-DAFB with active-clamp topology suffers from disadvantages like high number of switches, high peak current, high circulating current at light load, and limited soft-switching range.

It is clear from Table 5.1 that CF-FBVD has less peak current resulting in reduction of circulating current and lower conduction losses. As can be seen from Table 5.1, peak HF switch voltages of both VF-DAB and CF-FBVD are both rather low. For VF-DAB, the voltage is clamped at battery voltage by input capacitor. For the proposed CF-FBVD, the voltage across primary devices is also clamped at a rather low reflected voltage making it possible to utilize low voltage rating semiconductor devices with low on-state resistance. Although on-state resistance of primary device of VF-DAB is lower, the conduction loss in primary devices is still much higher compared to the loss of CF-FBVD. It is due to higher switch RMS current of VF-DAB as clearly illustrated by Table 5.1. On the other hand, from theoretical analysis and simulation verification, it is observed that the switch peak and RMS current of VF-DAB increase with rise in input voltage, thereby increasing the conduction losses in primary side switches and reducing the converter efficiency. For the present application, once the battery is charged to a higher voltage than its nominal value, both switch peak and RMS current go higher and the efficiency falls. However, for the proposed CF-FBVD, in that scenario, it maintains higher efficiency when the battery voltage fluctuates and load current reduces. The input current ripple of VF-DAB converters is much higher than that of CF-FBVD topologies thus a large input filter is required. CF-FBVD is a modified configuration of CFDAB proposed in Chapter 3 with voltage doubler at the load side. It reduces the two active devices and associated driving

circuits. High power single-cell design, better battery utilization, lower peak current, lower transformer kVA rating, reduced circulating current, and better part load efficiency make CF-FBVD more promising for FCVs/EVs [114].

Table 5.1: Comparison of four bidirectional DC/DC converter topologies at V_{in} = 12 V and full load (1 kW).

Topology	CF-DAHB	CF-DAFB with active-clamp	VF-DAB	CF-FBVD
Number of switches	4	9	8	6
Number of capacitors	4	2	2	2
Number of inductors	1	1	0	1
Primary switch current peak (A)	262.5	172.8	175	86.4
Primary switch current RMS (A)	80 and 147.5	56.7	98.6	52.5
Primary switch voltage stress (V)	24	30	12	30
Secondary switch current peak (RMS) (A)	15.9 (9.2)	13.8 (4)	7 (4)	17.3 (9)
Secondary switch voltage stress (V)	300	300	300	300
Transformer turns ratio	-	12.5	25	5
Duty cycle range	0 < d < 1	0 < d < 1	0 < d < 1	0.5 < d < 1
Input filter	Not required	Not required	Required	Not required
Soft switching	ZVS	ZVS	ZVS	ZCS/ZVS
Soft switching range	wide	limited	limited	wide

5.3 Proposed Modular Multi-cell Current-fed Full-bridge Voltage Doubler (CF-FBVD) Bidirectional DC/DC Converter

Different energy storages like Li-ion battery, NiMH battery, Lead-Acid Battery, and Supercapacitors have been used as ESS. They have obvious different energy density and power density profiles. High power density energy storage is required to supply or absorb the high transient power. However, high energy density devices are used to supply the energy continuously for sufficient long transient time. Composite energy storage system (CESS) comprising both high power and high energy density devices has been proposed to improve the performance of ESS [161]. Besides, the

internal operating bus voltage is not fixed. Low voltage bus interfacing energy storage evolves from traditional 12V system to a higher voltage system like recently arising 42V Power Net, dual voltage power system [162]. High voltage bus interfacing electrical motor is also diverse with existing examples such as variable dc bus voltage of 255V-425V [29], 150-300V [32], fixed voltage 400V [163], or 800V [164]. The power capacity requirement of ESS varies as well, ranging from several kW in passenger car to tens of kW in heavy duty buses. Therefore, modular power electronics needs to be researched to match different sources, different operating bus voltages, and different load requirements.

In this Section, CF-FBVD is proposed as a modular PEBB. The primary and secondary sides of modular multi-cell CF-FBVD are connected in series, parallel, or combination of them, respectively according to input/output voltages and/or the output power. Six different possible configurations of the proposed modular multi-cell CF-FBVD are given in Fig. 5.8 [161]. Each cell is interleaved with a phase-shift of $2\pi/n$. For the Parallel Input Parallel Output (PIPO) configuration as shown in Fig. 5.8 (a), different cells are connected in parallel simply. The input/output currents are shared among all cells and power transferring capacity is enhanced. The Parallel Input Series Output (PISO) configuration presented in Fig. 5.8 (b) is proposed for high power high output voltage application. Series output and parallel output can be combined together to obtain optimized design of voltage/current ratings of devices while satisfying the dc bus voltage requirement. Configurations of PIPO, PISO, or the combination of them are mainly suitable for low voltage high current

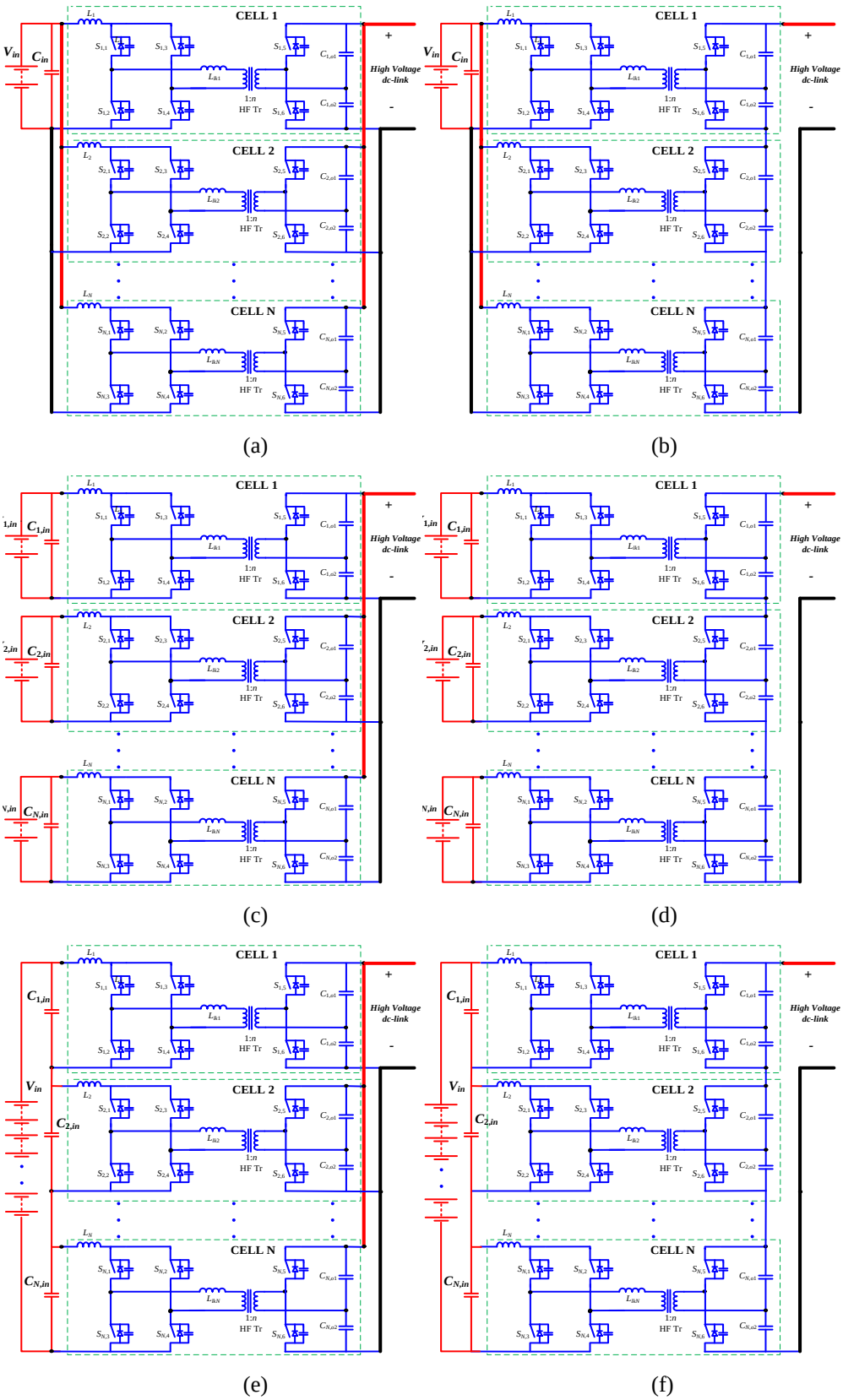


Fig. 5.8. Different possible configurations of the proposed modular CF-FBVD multi-cell DC/DC converter. (a) Parallel Input Parallel Output (PIPO); (b) Parallel Input Series Output (PISO); (c) Multiple Input Parallel Output (MIPO); (d) Multiple Input Series Output (MISO); (e) Series Input Series Output (SISO); (f) Series Input Parallel Output (SIPO).

application like supercapacitor/ultracapacitor. Generally, the terminal voltage of supercapacitor is low (less than 45V). However, the high power handling capacity is necessary since supercapacitor is a high power density source. Configurations of Multiple Input Parallel Output (MIPO) and Multiple Input Series Output (MISO) as illustrated by Fig. 5.8(c-d) are introduced to interface different sources. These two configurations provide advantages: 1) Individual active power control of each cell: Manufacturing tolerances and operating conditions may cause differences among multiple energy storage units. Individual control permits individual charging/discharging profiles of each storage unit to achieve maximum utilization and better performance. 2) Allowing integration of different types of energy storage devices. 3) Higher reliability. In case of failure of one of the cells, system can still function at reduced power. In some cases, some batteries are connected in series to obtain high source voltage and high energy/power density. Series Input Series Output (SISO) and Series Input Parallel Output (SIPO) as presented in Fig. 5.8 (e-f) or the combinations of them are better feasible for such high input voltage high output voltage applications.

The proposed modular multi-cell CF-FBVD offers the following features and merits [164]:

- Reduced voltage or current ratings of semiconductor devices and passive capacitors. As shown in Table 5.2, the current ratings of components are decreased by a factor of n with n cells in parallel. Similarly, voltage ratings of components are reduced to $1/n$ when n cells are connected in series.

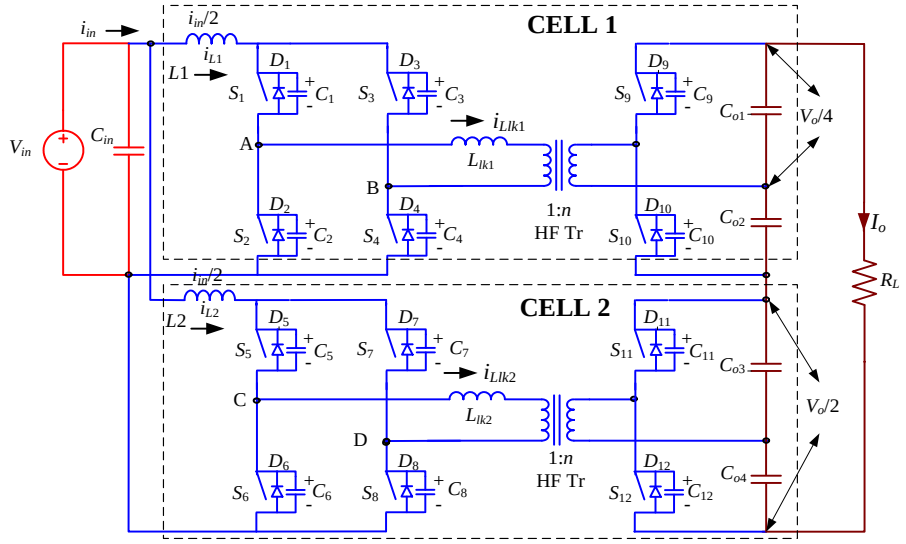


Fig. 5.9. A design example of two cells for the PISO configuration of the proposed modular CF-FBVD multi-cell DC/DC converter.

Table 5.2: Comparison of switch voltage/current stress for the six configurations under the same output power.

	PISO	PIPO	MISO	MIPO	SISO	SIPO
Primary Switch Current Rating	1/n	1/n	1/n	1/n	1	1
Primary Switch Voltage Rating	1	1	1	1	1/n	1/n
Secondary Switch Current Rating	1	1/n	1	1/n	1	1/n
Secondary Switch voltage Rating	1/n	1	1/n	1	1/n	1

- Reduced turns ratio of the HF transformer.
- Reduced input and output filters requirements. The input current and output voltage ripple frequency can be increased by a factor of *n* and ripple magnitude can be reduced considerably because of ripple cancellation effect.
- Components availability and easy thermal distribution. Modular multi-cell design provides flexibility in device selection and design optimization etc.

In this Chapter, a design example of two interleaved cells for the PISO configuration of the proposed multi-cell modular CF-FBVD as shown in Fig. 5.9 is studied.

5.4 Operation and Analysis of the Converter

For simplifying the study of operation and analysis, the following assumptions are made for the operation and analysis of the converter: a) Boost inductors L_1 and L_2 are large enough to maintain constant current through them. Output capacitors Co_1, Co_2, Co_3, and Co_4 are large enough to maintain constant voltage across them; b) All components are ideal; c) Series inductors L_{lk1} and L_{lk2} include the leakage inductances of the HF transformers; and d) Magnetizing inductances of the transformers are infinitely large.

The steady-state operating waveforms are shown in Fig. 5.10. The primary switches pairs S_1-S_4 and S_2-S_3 in Cell 1 are operated with identical gating signals phase-shifted with each other by 180^o and the duty cycle should be kept above 50%. The same is true for the switches pairs S_5-S_8 and S_6-S_7 in Cell 2. The phase difference between gating signals of switches pairs S_1-S_4 and S_5-S_8 is 90^o. The converter operation during different intervals in a one quarter cycle is explained with the help of equivalent circuits shown in Fig. 5.11. For the rest of the HF cycle, the intervals are repeated in the same sequence with other symmetrical devices conducting to complete the full HF cycle.

Interval 1 (Fig. 5.11a; $t_0 < t < t_1$):

CELL 1: In this interval, primary switch S_2 and S_3 and anti-parallel body diode D_{10} of secondary side switches are conducting. The current through

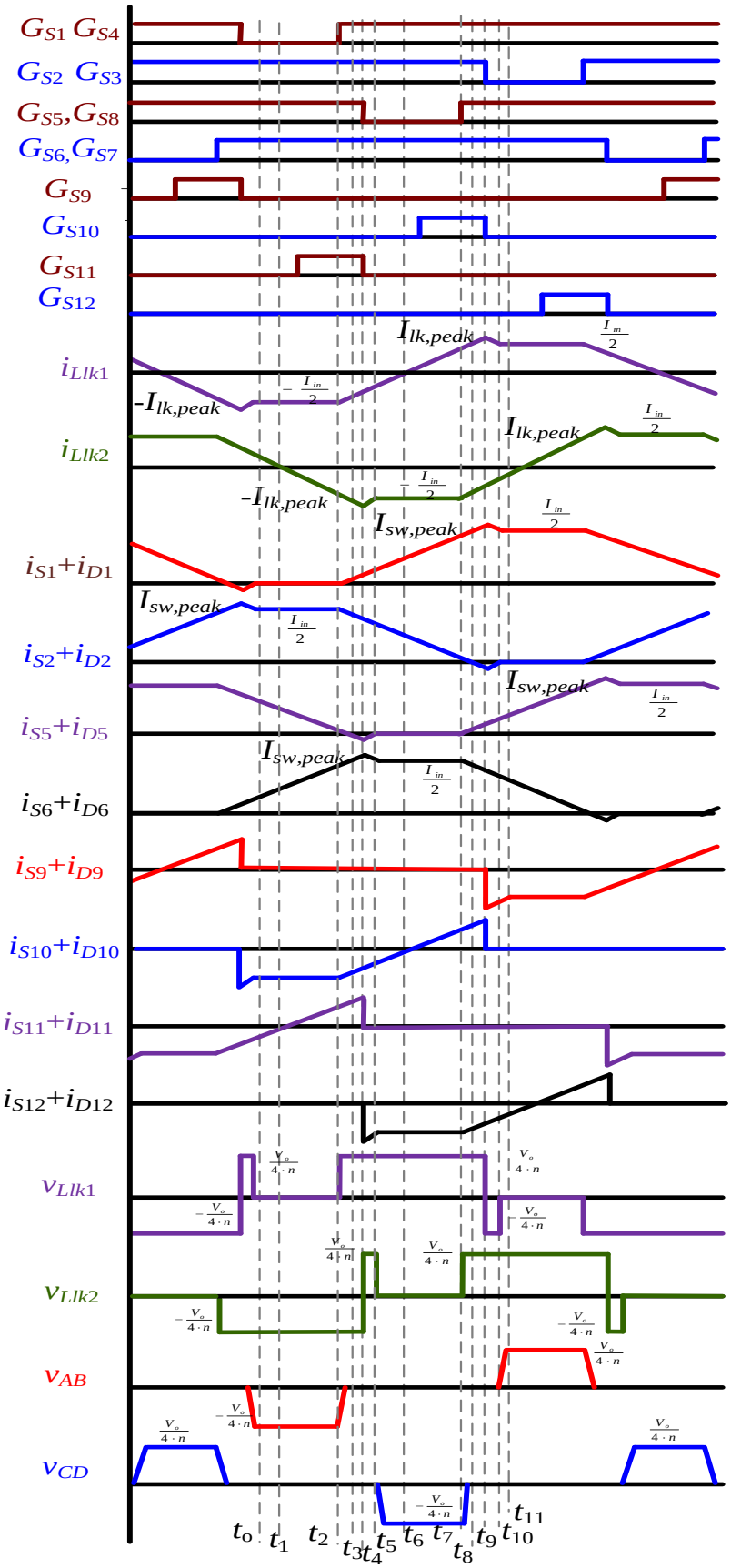
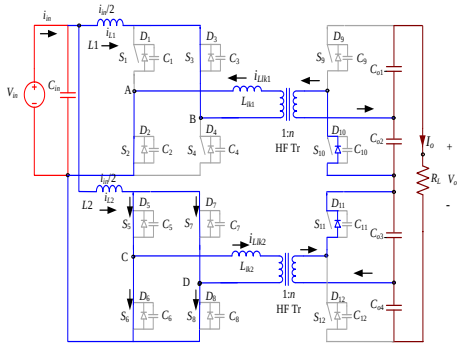
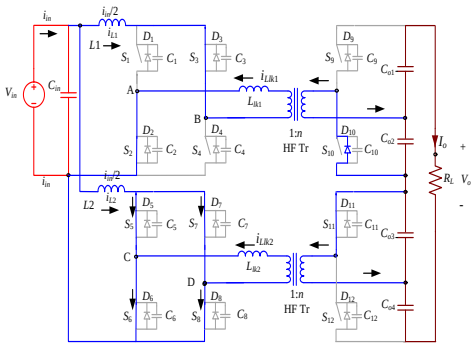


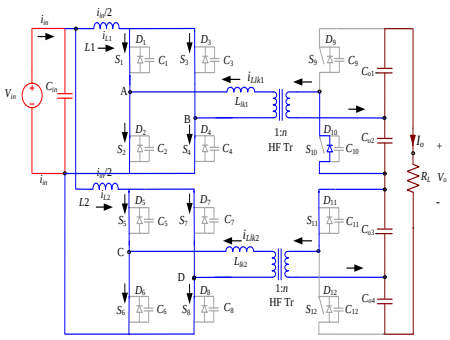
Fig. 5.10. Operating waveforms of proposed ZCS current-fed dual active bridge converter.



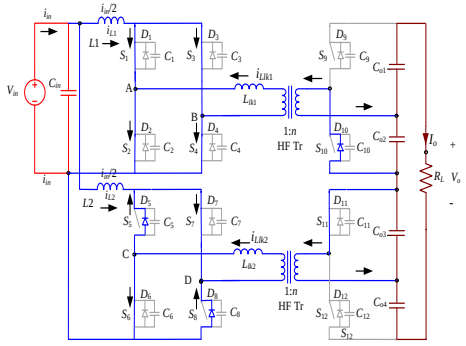
(a)



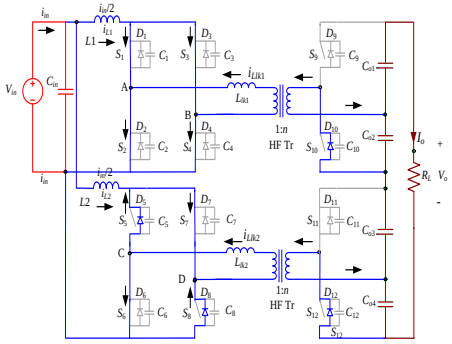
(b)



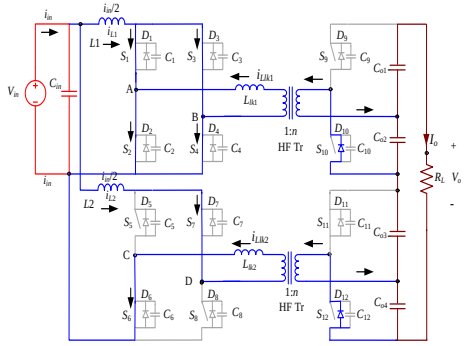
(c)



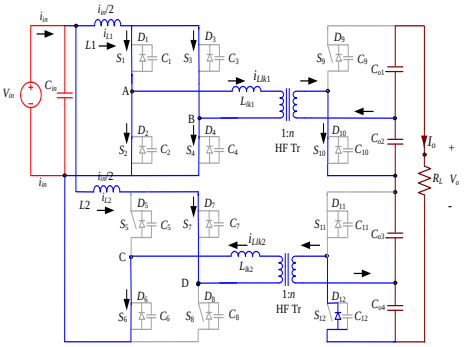
(d)



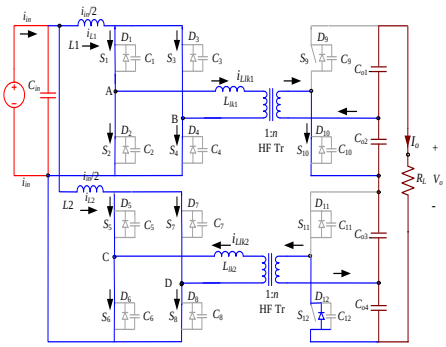
(e)



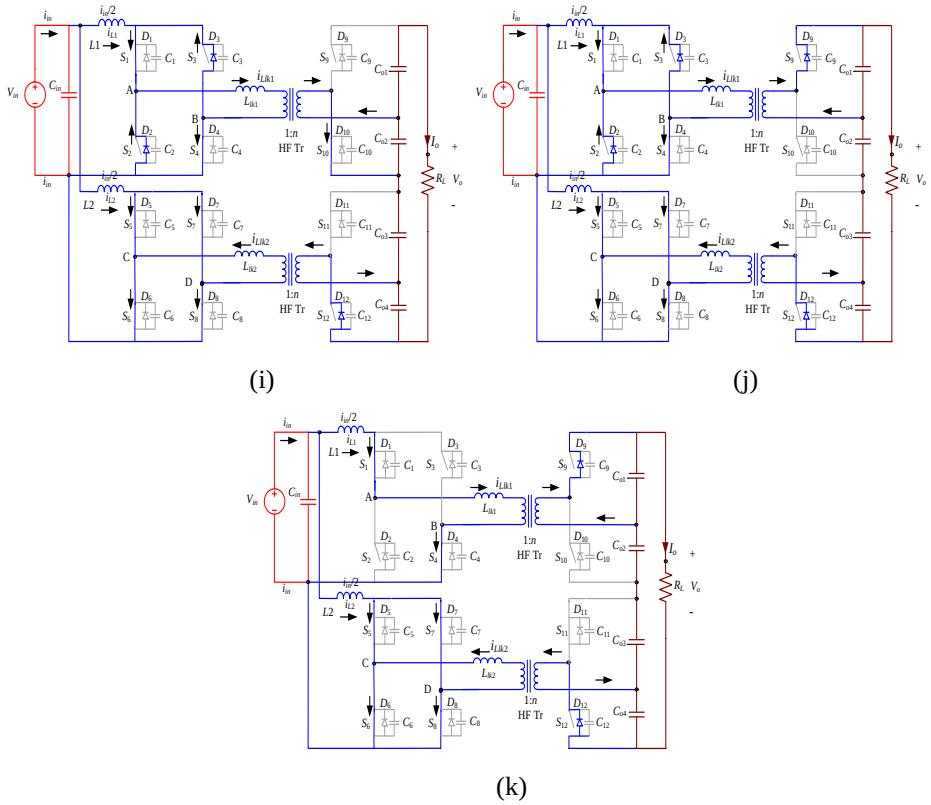
(f)



(g)



(h)



(i) (j)

(k)

Fig. 5.11. Equivalent circuits during different intervals of operation of the proposed converter.

inductor L_{lk1} is negative and constant. The currents through main components: $i_{S2} = i_{S3}=I_{in}/2$, $i_{S1} = i_{S4}=0$, $i_{Llk1}=-I_{in}/2$, $i_{D10}= I_{in}/2n$. Voltages across the switches S_1 and S_4 :$V_{S1} =V_{S4} = V_o/4n$.

CELL 2: In this interval, all four primary switches of Cell 2 are conducting. Negative voltage equal to $V_o/4n$ appears across the inductor L_{lk2} and current through it decreases linearly. The currents through the switching devices are given by

$$i_{Llk2} = I_{Llk2}(t_0) - \frac{V_o}{4n \cdot L_{lk}} \cdot (t - t_0) \tag{5-1}$$

$$i_{S5} = i_{S8} = I_{S5}(t_0) - \frac{V_o}{8n \cdot L_{lk}} \cdot (t - t_0) \tag{5-2}$$

$$i_{S6} = i_{S7} = I_{S6}(t_0) + \frac{V_o}{8n \cdot L_{lk}} \cdot (t - t_0) \tag{5-3}$$

$$i_{D11} = \frac{I_{Llk2}(t_0)}{n} - \frac{V_o}{4n^2 \cdot L_{lk}} \cdot (t - t_0) \tag{5-4}$$

Before the end of this interval $t=t_1$, the anti-parallel body diode D_{11} of switches S_{11} is conducting. S_{11} can be gated on for ZVS turn on. Final values: $i_{Llk2}=0$, $i_{S5}= i_{S6} = i_{S7}= i_{S8}=I_{in}/4$, $i_{D11}= 0$.

Interval 2 (Fig. 5.11b; $t_1 < t < t_2$):

CELL 1: Interval 2 stays the same with interval 1.

CELL 2: In this interval, S_{11} is turned on with ZVS. Currents through all the switching devices of Cell 2 continue to increase or decrease with the same slope as interval 1.

Interval 3 (Fig. 5.11c; $t_2 < t < t_3$):

CELL 1: At $t = t_2$, primary switches S_1 and S_4 are turned on. The corresponding snubber capacitors C_1 and C_4 discharge in a very short period of time. And then all four primary switches of Cell 1 are conducting. A positive voltage equal to $V_o/4n$ appears across the inductor L_{lk1} and current through it starts increasing linearly. Switches S_1 and S_4 start conducting with zero current which helps in reducing associated turn-on loss. The currents through the devices are given by

$$i_{Llk1} = -\frac{I_{in}}{2} + \frac{V_o}{4n \cdot L_{lk}} \cdot (t - t_2) \tag{5-5}$$

$$i_{S1} = i_{S4} = \frac{V_o}{8n \cdot L_{lk}} \cdot (t - t_2) \tag{5-6}$$

$$i_{S2} = i_{S3} = \frac{I_{in}}{2} - \frac{V_o}{8n \cdot L_{lk}} \cdot (t - t_2) \tag{5-7}$$

$$i_{D10} = \frac{I_{in}}{2n} - \frac{V_o}{4n^2 \cdot L_{lk}} \cdot (t - t_2) \tag{5-8}$$

CELL 2: In this interval, currents through all the devices of Cell 2 continue to increase or decrease with the same slope as interval 2. At the end of this interval, the switch currents i_{S5} and i_{S8} reach zero obtaining ZCS of S_5 and S_8. Final values: i_{Llk2}=-I_{in}/2, i_{S6}=i_{S7}=I_{in}/2, i_{S5} = i_{S8}=0, i_{S11} = I_{in}/2n

Interval 4 (Fig. 5.11d; $t_3 < t < t_4$):

CELL 1: In this interval, currents through all the switching devices of Cell 1 continue to increase or to decrease with the same slope as interval 3.

CELL 2: In this interval, the current through inductor L_{lk2} keeps decreasing and body diodes D_5 and D_8 start conducting. At the end of this interval, currents through inductor L_{lk2}, switches S_6 and S_7 reach their peak values. This interval should be very short to limit the peak current though the components reducing the current stress and kVA ratings.

The currents through the operating components are given by

$$i_{Llk2} = -\frac{I_{in}}{2} - \frac{V_o}{4n \cdot L_{lk}} \cdot (t - t_4) \tag{5-9}$$

$$i_{S6} = i_{S7} = \frac{I_{in}}{2} + \frac{V_o}{8n \cdot L_{lk}} \cdot (t - t_4) \tag{5-10}$$

$$i_{D5} = i_{D8} = \frac{V_o}{8n \cdot L_{lk}} \cdot (t - t_4) \tag{5-11}$$

$$i_{S11} = \frac{I_{in}}{2n} + \frac{V_o}{4n^2 \cdot L_{lk}} \cdot (t - t_4) \tag{5-12}$$

Interval 5 (Fig. 5.11e; $t_4 < t < t_5$):

CELL 1: In this interval, currents through all the switching devices of Cell 1 continue increasing or decreasing with the same slope as interval 3.

CELL 2: During this interval, switches S_5 and S_8 are switches off. Since body diodes D_5 and D_8 are conducting, S_5 and S_8 are ZCS turned off. At the same moment, secondary switch S_{11} is turned off. Anti-parallel body diode of switch S_{12} takes over the current immediately. The voltage across the inductor L_{lk2} becomes positive and the current through it starts increasing. The currents through the switches S_6 and S_7 and body diodes D_5 and D_8 start decreasing.

The currents through the operating components are given by

$$i_{Llk2} = -I_{lk,peak} + \frac{V_o}{4n \cdot L_{lk}} \cdot (t - t_5) \tag{5-13}$$

$$i_{S6} = i_{S7} = I_{sw,peak} - \frac{V_o}{8n \cdot L_{lk}} \cdot (t - t_5) \tag{5-14}$$

$$i_{D5} = i_{D8} = I_{D2,peak} - \frac{V_o}{8n \cdot L_{lk}} \cdot (t - t_5) \tag{5-15}$$

$$i_{D12} = \frac{I_{lk,peak}}{n} - \frac{V_o}{4n^2 \cdot L_{lk}} \cdot (t - t_5) \tag{5-16}$$

At the end of this interval, currents through D_5 and D_8 reduce to zero. Final values: $i_{Llk2} = I_{in}/2$, $i_{S6}=i_{S7}=I_{in}/2$, $i_{D5} = i_{D8}=0$, $i_{D12} = I_{in}/2n$.

Interval 6 (Fig. 5.11f; $t_5 < t < t_6$):

CELL 1: In this interval, currents through all the switching devices of Cell 1 continue to increase or decrease with the same slope as interval 3.

Before the end of this interval $t=t_6$, the body diode D_{10} of switch S_{10} is conducting. S_{10} can be gated on for ZVS turn on. Final values: $i_{Llk1}=0$, $i_{S1}= i_{S2} = i_{S3}= i_{S4}=I_{in}/4$, $i_{D10} = 0$.

CELL 2: Snubber capacitors C_5 and C_8 charge to $V_o/4n$ in a very short period of time. Constant current flows through switch S_7, inductor L_{lk2}, S_6 and the body diode of the secondary switch S_{12}. The currents through main components: $i_{S6} = i_{S7}=I_{in}/2$, $i_{S5} = i_{S8}=0$, $i_{Llk2}=-I_{in}/2$, $i_{D12}= I_{in}/2n$. Voltage across the switches S_5 and S_8:$V_{S5}=V_{S8} = V_o/4n$.

5.5 Design of the Converter

In this Section, design is illustrated by a design example with a converter of the following specifications: Minimum input voltage V_{in} = 12 V, output voltage V_o = 150 to 300V, nominal output voltage=300V, output power P_o = 500W, switching frequency f_s = 100 kHz. The design equations are presented to determine the components' ratings. It facilitates the selection of the components and to analytically predict the performance of the converter.

(1) Average input current is $I_{in} = P_o/(\eta V_{in})$. Assuming an ideal efficiency η of 95%, I_{in} = 43.9 A.

(2) Maximum voltage across the primary switches is

$$V_{P,SW} = \frac{V_o}{4 \cdot n} \tag{5-17}$$

(3) Voltage conversion ratio or input and output voltages are related as

$$V_o = \frac{2 \cdot n \cdot V_{in}}{1-d} \tag{5-18}$$

(4) Leakage inductance of the transformer or series inductance L_{lk} is calculated using the following euqation

$$L_{lk} = \frac{V_o \cdot (d-0.5)}{4 \cdot n \cdot I_{in} \cdot f_s} \tag{5-19}$$

(5) RMS current through the primary switches is given by

$$I_{P,rms} = \frac{I_{in}}{2}\sqrt{\frac{2-d}{3}} \tag{5-20}$$

The calculated value is $I_{P,rms}$ = 13.85 A.

(6) The output power can be derived as

$$P = \frac{4n \cdot v_{in}{}^{2} - v_o \cdot v_{in} \cdot (3-4 \cdot d)}{16 \cdot n \cdot L_{lk} \cdot f_s} \tag{5-21}$$

The transformer turns ratio selection is based on conduction losses, which mainly consists of the conduction losses in the primary switches because they carry higher currents. Increasing the turns ratio can reduce the maximum voltage across the primary switches, which makes it possible to use low voltage rating switches with lower on-state resistance (from (5-17)). Leakage inductance of the transformer L_{lk} decreases with the increase of turns-ratio, thus improving the power transferring ability of the converter (from (5-21)). Power transferring capacity is limited by the leakage inductance of the HF transformer. In addition, when the converter works in reverse direction to absorb the energy owing to regenerative braking, smaller leakage inductance will result in smaller duty cycle loss. However, higher turns ratio yields higher switch RMS current (from (5-18) and (5-20)). Voltage regulation over varying fuel cell dc bus with varying battery terminal voltage is another concern to be addressed during design. An optimum turns ratio n = 2.5 and duty ratio d = 0.8 are selected to achieve low overall conduction losses. Output voltage can be regulated from 150V to 300V by modulating the duty ratio from 0.5 to 0.8. Leakage inductance of L_{lk} = 2.05 μH is obtained from (5-19) for the above given values.

(7) RMS current through the primary winding of each HF transformer is given by the following equation

$$I_{Llk,rms} = \frac{I_{in}}{2}\sqrt{\frac{5-4d}{3}} \tag{5-22}$$

The calculated value of $I_{Llk,rms}$ = 17A.

(8) Value of boost inductor is given by

$$L = \frac{V_{in}\cdot(d-0.5)}{\Delta I \cdot f_s} \tag{5-23}$$

where ΔI is the boost inductor ripple current. For ΔI = 1 A, L = 36 μH.

(9) Average current and RMS current through the body diodes of secondary devices is given by

$$\bar{i}_D = \frac{I_{in}\cdot(7-6d)}{16n} \tag{5-24}$$

$$I_{D,rms} = \frac{I_{in}}{4n}\sqrt{\frac{11\text{-}10d}{3}} \tag{5-25}$$

The calculated value of $I_{D,rms}$ = 4.39 A.

(10) RMS current through the secondary side switches is given by

$$I_{S,rms} = \frac{I_{in}}{4n}\sqrt{\frac{2d-1}{3}} \tag{5-26}$$

The calculated value of $I_{S,rms}$ = 1.96 A.

Voltage rating of secondary side devices = V_o/2 = 150V.

(11) VA rating of each HF transformer is given by

$$VA_{x-mer} = \frac{V_o \cdot I_{in}}{8n}\sqrt{\frac{2\cdot(5-4d)\cdot(1-d)}{3}} \tag{5-27}$$

The calculated value is $VA_{X\text{-}mer}$ = 321.9 VA.

A loss modeling of proposed converter can be done by considering the static loss of primary and secondary side switches, boost inductors, output capacitors, HF transformer and switching loss of switches.

(12) The conduction loss of each boost inductor is given by

$$P_{L,Con} = R_L \cdot I_{L,rms}^2 = \frac{R_L \cdot I_{in}^2}{4} \tag{5-28}$$

where R_L is ohmic resistance of boost inductor.

The conduction loss of primary and secondary side switches are given by

$$P_{P,Con} = r_{P,on} \cdot I_{P,rms}^2 = \frac{r_{P,on} \cdot I_{in}^2 \cdot (2-d)}{12} \tag{5-29}$$

$$\begin{aligned} P_{S,Con} &= r_{S,on} \cdot I_{S,rms}^2 + r_D \cdot I_{D,rms}^2 + v_D \cdot \bar{i}_D \\ &= \frac{r_{S,on} \cdot I_{in}^2 \cdot (2d-1)}{48 \cdot n^2} + \frac{r_D \cdot I_{in}^2 \cdot (11-10d)}{48 \cdot n^2} + \frac{v_D \cdot I_{in} \cdot (7-6d)}{16 \cdot n} \end{aligned} \tag{5-30}$$

where $r_{P,on}$ and $r_{S,on}$ are the on-resistance of primary and secondary side switches respectively. r_D is the forward voltage of body diode of secondary side switches.

The switching loss of the primary (ZCS) and secondary side switches (ZVS) is given by

$$P_{P,Sw} = P_{Sw,on} + P_{Sw,off} = C_{snubber} \cdot V_p^2 \cdot f + 0 = \frac{C_{snubber\_p} \cdot V_o^2 \cdot f}{16 \cdot n^2} \tag{5-31}$$

$$P_{S,Sw} = P_{Sw,on} + P_{Sw,off} = 0 + \frac{I_{off}^2 \cdot t_f^2 \cdot f_s}{24 \cdot C_{snubber\_s}} = \frac{I_{off}^2 \cdot t_f^2 \cdot f_s}{24 \cdot C_{snubber\_s}} \tag{5-32}$$

Where t_f is the fall time of the secondary side switches during turn-off. $C_{snubber\_p}$ and $C_{snubber\_s}$ is the snubber capacitance of primary and secondary switches respectively.

The copper loss of HF transformer is given by

$$P_{Tr,Copp} = r_{pri} \cdot I_{Llk,rms}^2 + r_{\sec} \cdot \frac{I_{Llk,rms}^2}{n^2} \tag{5-33}$$

where r_{pri} and r_{sec} are ohmic resistances of primary and secondary sides of HF transformer respectively.

The core loss of boost inductor and HF transformer can be calculated by the following empirical formula [165].

$$P_{L\_core} = C_m V_c f^x B_{AC}^y \tag{5-34}$$

where V_c represents effective core volume , C_m, x and y are the coefficient of the related core material, B_{AC} is AC flux density.

The equivalent series resistance (ESR) loss of output capacitors is given by

$$P_{cap} = r_{cap} \cdot (I_{S,rms}^2 + I_{D,rms}^2) \tag{5-35}$$

where r_{cap} is the ESR of each output capacitor.

The total loss is given by

$$\begin{aligned} P_{loss} &= P_{L,Con} \cdot 2 + \left(P_{P,Con} + P_{P,Sw}\right) \cdot 8 + \left(P_{S,Con} + P_{S,Sw}\right) \cdot 4 \\ &+ (P_{L,core} + P_{Tr,core}) \cdot 2 + P_{Tr,Copp} \cdot 2 + P_{cap} \cdot 4 \end{aligned} \tag{5-36}$$

The transfer efficiency is given by

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{in} \cdot I_{in} - P_{loss}}{V_{in} \cdot I_{in}} \tag{5-37}$$

These equations are derived on the condition that anti-parallel diode conduction time is quite short and negligible with the intention to ensure ZCS of primary switches without significant increase in peak current of the switches. However, at light load, the body diode conduction time is comparatively large and (5-18) is not valid any more. Due to extended body diode conduction, the output voltage is boosted to higher value than nominal boost converter. Equation (5-18) is modified to

$$V_o = \frac{2n \cdot V_{in}}{(1 - d - d')} \tag{5-38}$$

Where d' is given by,

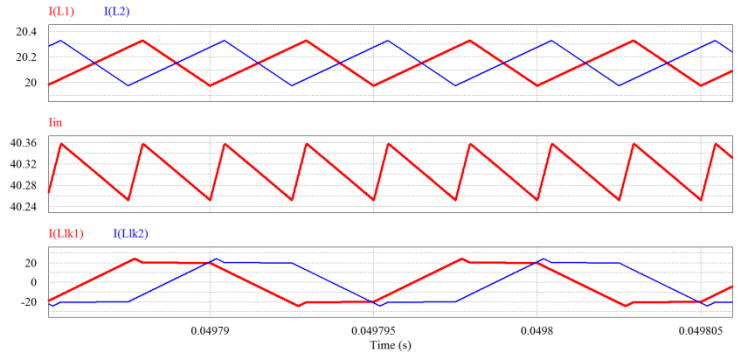
$$d' = d - 0.5 - \frac{4 \cdot n \cdot I_{in} \cdot L_{lk} \cdot f_s}{V_o} \tag{5-39}$$

From (5-38), it can be observed that for a given value of L_{lk} and V_o , d' increases as the load is decreased.

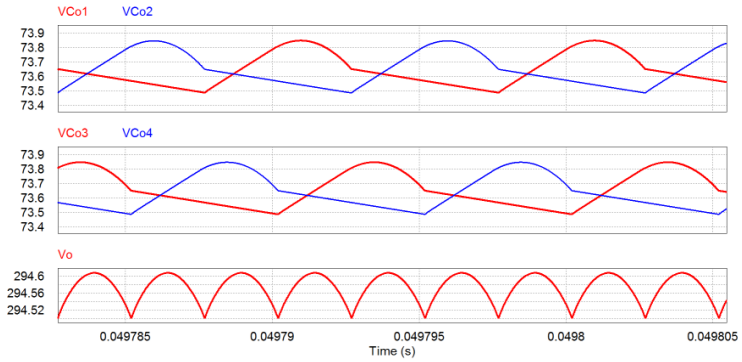
5.6 Simulation and Experimental Results

The proposed converter has been simulated using software package PSIM 9.0.4 and later a prototype rated at 500W was developed and tested in research lab to verify the steady-state analysis and simulation results. The specifications of the converter: input voltage V_{in} = 12 V, nominal output voltage V_o = 300 V, output power P_o = 500W, device switching frequency f_s = 100 kHz. Simulation results are illustrated in Fig. 5.12and Fig. 5.13, which coincide closely with theoretical operating waveforms shown in Fig. 5.10.

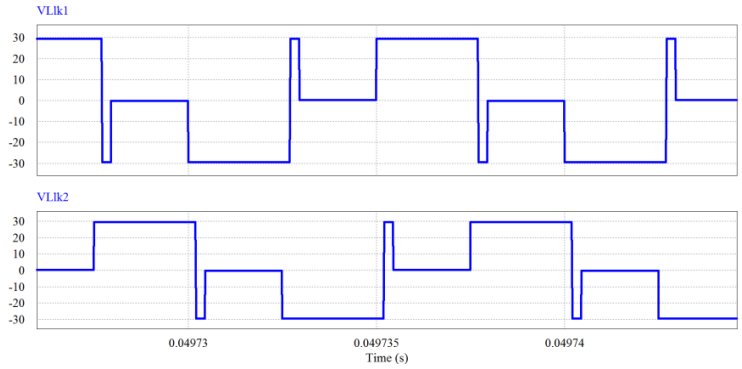
Simulation waveforms of input boost inductor currents $I(L_1)$, $I(L_2)$, input current I_{in}, series inductor currents $I(L_{Llk1})$ and $I(L_{Llk2})$ are shown in Fig. 5.12.



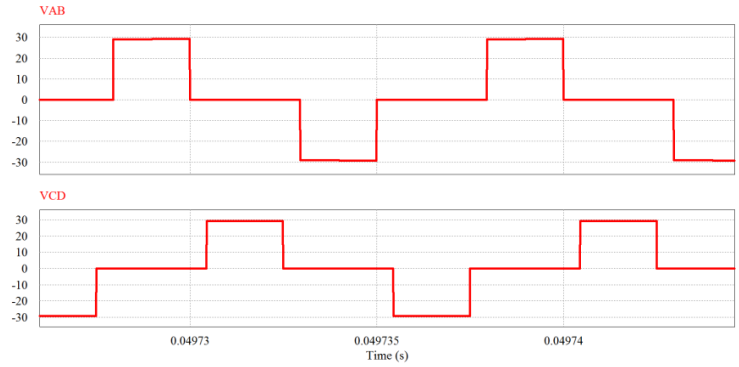
(a)



(b)

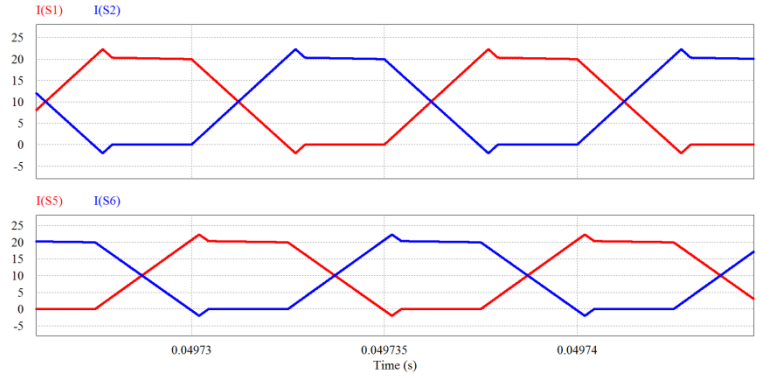


(c)

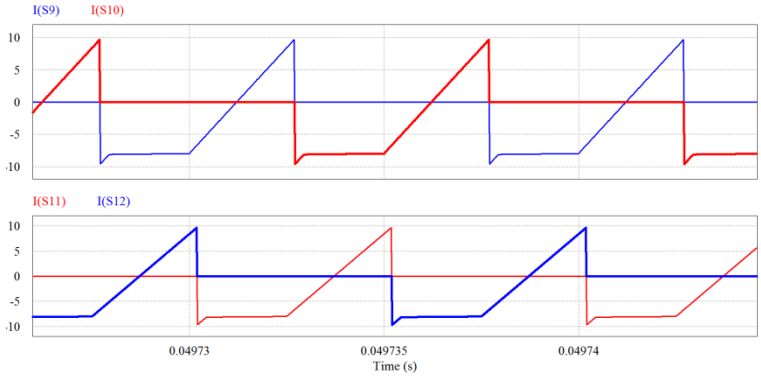


(d)

Fig. 5.12. Simulation waveforms: (a) input boost inductor currents $I(L_1)$, $I(L_2)$, input current I_{in}, series inductor currents $I(L_{Llk1})$ and $I(L_{Llk2})$, (b) Voltages across output capacitors V_{Co1} ,V_{Co2} ,V_{Co3} ,V_{Co4} and output voltage V_O, (c) voltage waveforms $V(L_{Llk1})$, $V(L_{Llk2})$, (d) voltage waveforms V_{AB} and V_{CD}



(a)



(b)

Fig. 5.13. Simulation waveforms: (a) primary switch currents $I(S_1)$, $I(S_2)$, $I(S_5)$ and $I(S_6)$, (b) secondary switch currents $I(S_9)$, $I(S_{10})$, $I(S_{11})$ and $I(S_{12})$.

The ripple frequency of input boost inductor currents is 2x device switching frequency. Currents $I(L_1)$ and $I(L_2)$ are phase-shifted with each other by nearly 180 °. Thus the input current I_{in} is of considerably low current ripple because of ripple cancellation of $I(L_1)$ and $I(L_2)$. The ripple frequency of I_{in} is 4x device of switching frequency, which reduces the requirements of input capacitor C_{in}. Fig. 5.12 (b) clearly shows voltages across output capacitors of each Cell (Co_1 and Co_2, Co_3 and Co_4) are phase-shifted with each other by 180˚. Voltage across Co_1 of CELL 1 is phase-shifted by 90º with Co_3 of CELL 2. Cancellation effect results in much lower output ripple magnitude which alleviates the output filter requirement. The peak currents through series inductors L_{Llk1} and L_{Llk2} above the constant value are caused by the extended conduction of body diodes of corresponding primary switches ensuring their

ZCS turn off. As shown by the voltage waveforms V_{AB} and V_{CD} in Fig. 5.12 (d), the voltages across the primary switches, which are equal to V_{AB} or V_{CD}, are naturally clamped at low voltage i.e., $V_o/4n$.

Fig. 5.13 shows simulation waveforms of currents through primary switches $I(S_1)$, $I(S_2)$, $I(S_5)$, and $I(S_6)$ and secondary switches $I(S_9)$, $I(S_{10})$, $I(S_{11})$, and $I(S_{12})$. The negative parts of these waveforms correspond to currents flowing through their respective body diodes. ZCS of primary switches are clearly illustrated. $I(S_1)$, $I(S_2)$, $I(S_5)$, and $I(S_6)$ naturally decrease to zero owing to secondary side modulation and then corresponding anti-parallel body diodes conduct before gating signals are removed which ensures ZCS turn-off of the primary switches. As shown in current waveforms $I(S_9)$, $I(S_{10})$, $I(S_{11})$ and $I(S_{12})$ in Fig. 5.13 (b), the body diodes of switches conduct before the devices start conducting confirming ZVS of the secondary side switches. The phase relationships between switches pairs of both cells are also obviously demonstrated by Fig. 5.12 and Fig. 5.13.

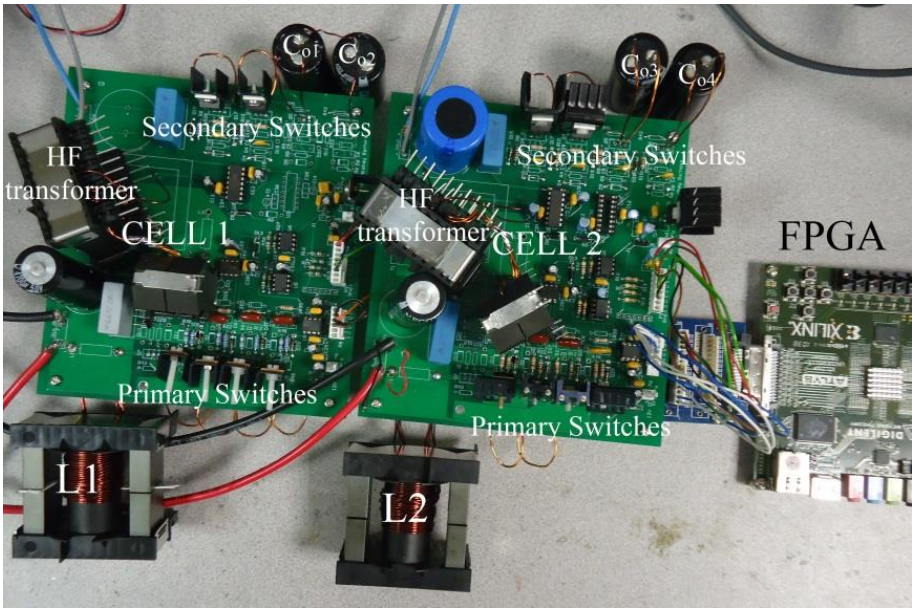
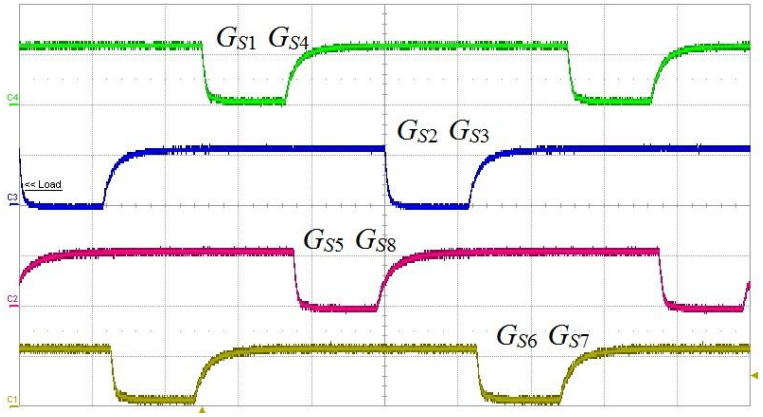


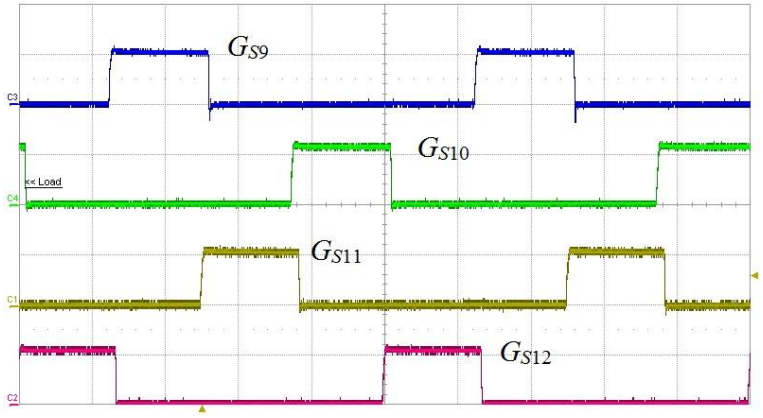
Fig. 5.14. Photograph of the laboratory prototype.

Table 5.3: Major components' parameters of experimental prototype

Components	Parameters
Primary switches $S1 \sim S4$ $S5 \sim S8$	IRFB3006PBF 60V, 195A. $R_{ds,on} = 2.1\ m\Omega$
Secondary switches $S9 \sim S10$ $S11 \sim S12$	IRFB4127 200V, 76A. $R_{ds,on} = 0.02\Omega$
HF transformers	PC47ETD44-Z ferrite core Primary turns N_1=4 Secondary turns N_2=10 Leakage inductance reflected to primary L_{lk}= 1.6 µH
Input boost inductor L_1 L_2	3C90ETD59 ferrite core turns $N = 8$
Input capacitors C_{in}	4.7 mF, 50V electrolytic 2.2 µF high-frequency film capacitor
Output capacitorsC_{o1}~ C_{o4}	680uF, 200V electrolytic capacitor



(a)



(b)

Fig. 5.15. Gating signals of all the switching devices for output power of 500W at 300V. (a) primary side switches, (b) secondary side switches (x-axis: 2 µs/div, y-axis: 10V/div).

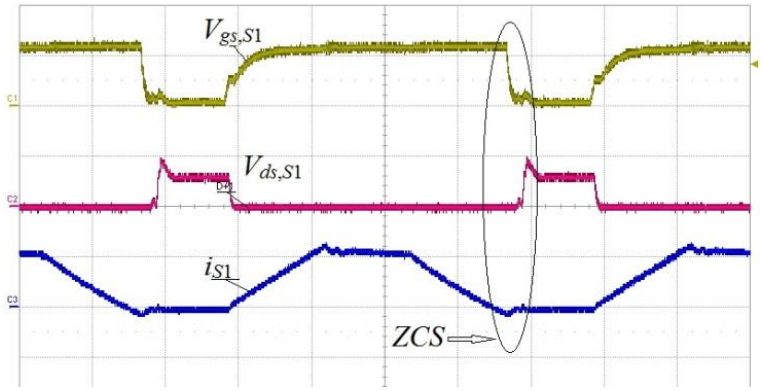
A laboratory prototype of the proposed converter rated at 500W as shown in Fig. 5.14 has been developed and tested to demonstrate its performance. Details of the experimental converter are given in Table 5.3. Gating signals for

the switches have been generated using Xilinx Spartan-3 FPGA board. Two IR2181 are used to drive the primary side MOSFETs and one IR21814 are used to drive the secondary side MOSFETs. Gating signals are illustrated in Fig. 5.15. These gating signals of two switch pairs of each cell are phase-shifted with each other by 180^o and two cells are shifted by 90^o.

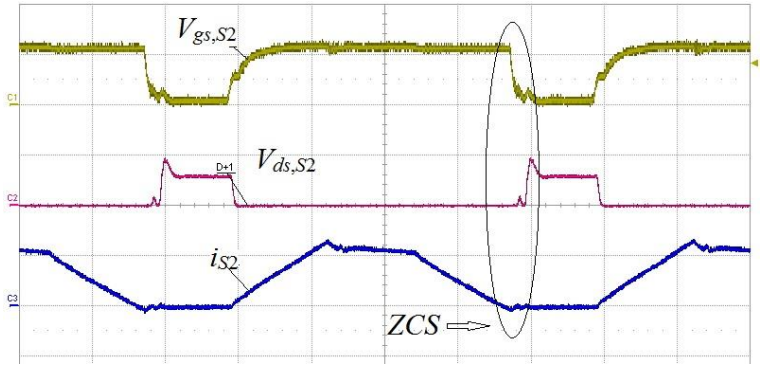
Experimental results are shown in Fig. 5.16 to Fig. 5.19 that matches closely with theoretical predicted waveforms and simulation waveforms. It can be obviously observed that ZCS of primary switches and ZVS of secondary switches at both full load (Fig. 5.16) and at partial load (Fig. 5.17) are achieved. In waveforms shown in Figs. 5.16 (a)-(b) and Figs. 5.17 (a)-(b), gating signal of primary switch V_{gs} is first removed before the switch voltage V_{ds} starts rising. The clear gap between these two waveforms corresponds to the conduction of the anti-parallel body diode of the respective switch. Due to secondary modulation, the switch current naturally falls to zero and then becomes negative because of the conduction of body diode, confirming the ZCS turn off of the primary switches. Figs.5.16 (c)-(d) and Figs.5.17 (c)-(d) clearly show the ZVS turn on of the secondary switches. Gating signal V_{gs} is applied to secondary switch when switch voltage V_{ds} is zero. Also, its body diode conducts prior to its switch's conduction, which verifies ZVS of secondary devices. Figs. 5.16 (a)-(b) and Figs. 5.17 (a)-(b) show the voltage across the primary devices is clamped at a rather low voltage that enables the use of low voltage rating devices to reduce conduction loss. Therefore the proposed modulation method obtains soft switching of all devices and clamped device voltage without additional active-clamping or passive snubbers circuits.

Additionally, the turn-on procedure of primary switches is also demonstrated in waveforms shown in Figs. 5.16 (a)-(b) and Figs. 5.17 (a)-(b). Before turning on, the voltage across primary switch is clamped at $V_o/4n$=30V. When the switch is gated on, the current through it is rising at a slope of *di/dt* =7.5A/μs from zero. With this limited *di/dt* through primary switch and low clamped voltage across it, the turn-on loss (due to overlap of switch voltage and current during switching transition time) is low. Considering ZCS turn-off of the primary switches and ZVS turn-on switching transition loss of the secondary side switches mentioned above, the total switching losses are reduced enormously. In addition, primary switches of low voltage rating (60V) with low on-state resistance can be used resulting in lower conduction loss and higher efficiency.

Fig. 5.18 (a) shows waveforms of voltage across the HF transformers and current through the primary windings of both cells. The HF bipolar voltage is clamped at a low voltage without ringing and spikes due to zero-current commutation. Currents through the primary windings i_{Llk1} and i_{Llk2} are continuous unlike traditional hard-switching and active-clamped converters. Current through primary and secondary side devices of both cells are illustrated in Fig. 5.18 (b)-(c) and are in good agreement with theoretical operating waveforms and simulation results. It can be clearly observed that S_1 and S_2 of Cell 1 (S_5 and S_6 of Cell 2) are phase-shifted by 180^o. S_1 of Cell 1 is phase-shifted by 90^o with S_5 of Cell 2. Similar phase shift relationship holds true for the corresponding secondary side switches. These current waveforms also clearly demonstrate ZCS of primary switches and ZVS of secondary switches of both cells.



(a)



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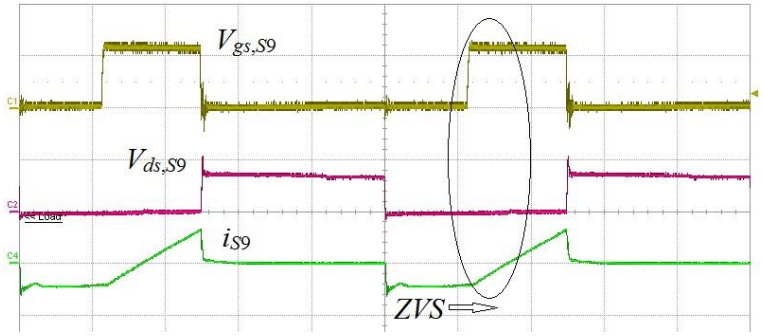

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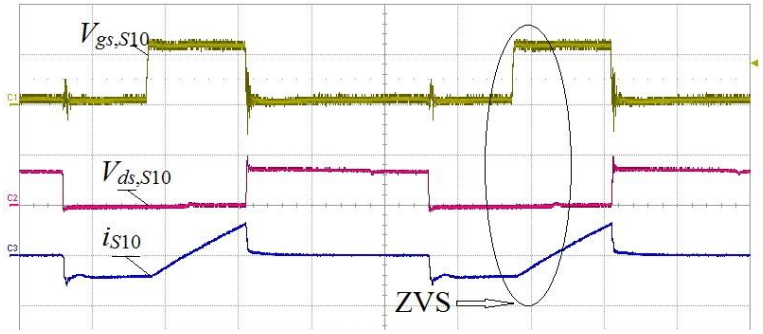
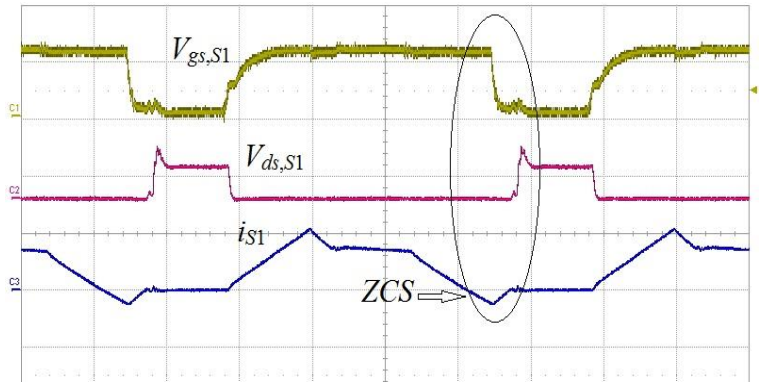
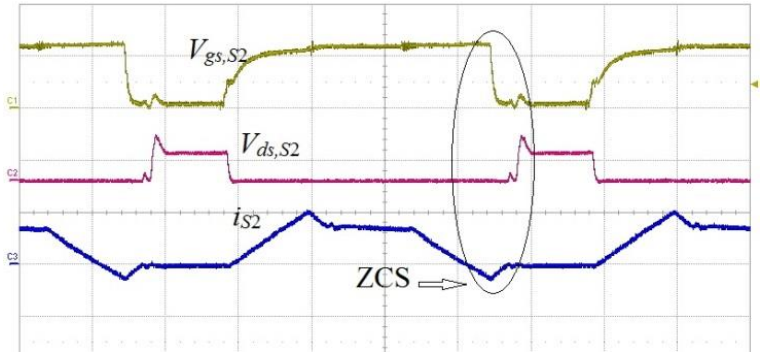


(d)

Fig. 5.16. Experimental results for output power of 500W at 300V (x-axis: 2 µs/div): (a-b) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (50V/div) across the primary side MOSFETs and currents through them (20A/div). (c-d) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (200V/div) across the secondary side MOSFETs and currents through them (20A/div).



(a)



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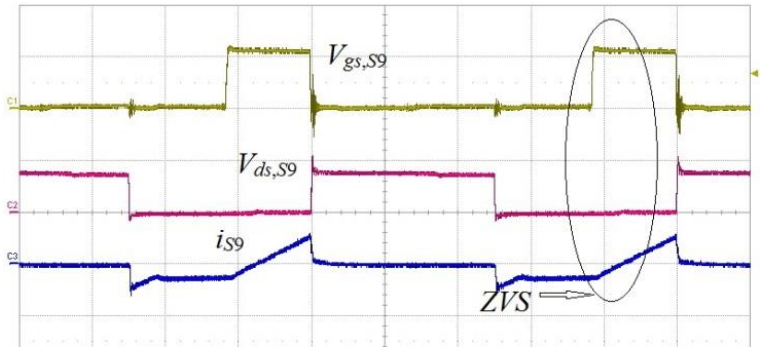

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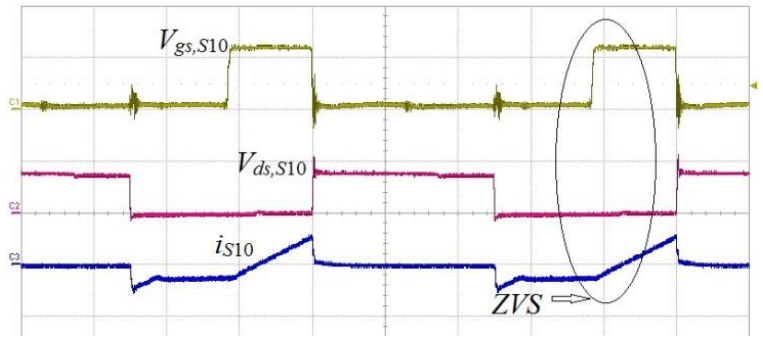
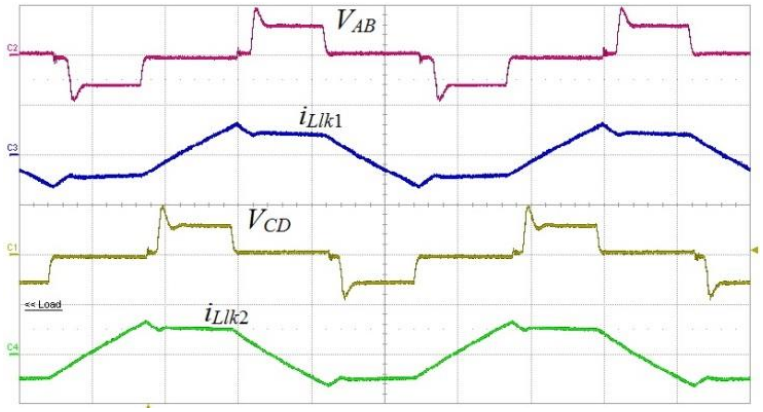
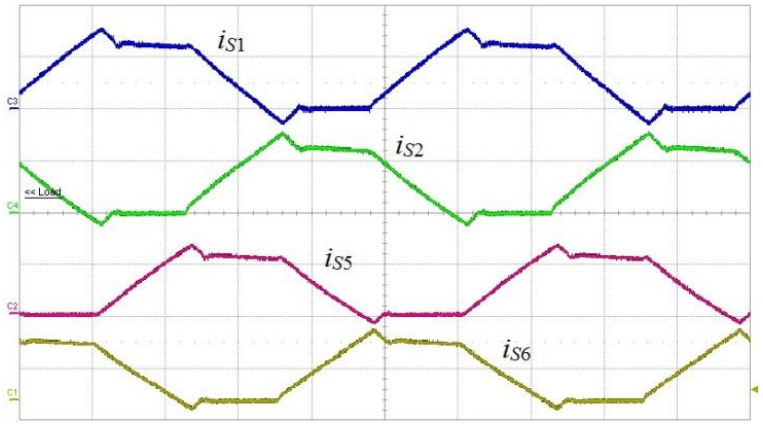


(d)

Fig. 5.17. Experimental results for output power of 250W at 300V (x-axis: 2 µs/div): (a-b) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (50V/div) across the primary side MOSFETs and currents through them (20A/div). (c-d) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (200V/div) across the secondary side MOSFETs and currents through them (20A/div).



(a)



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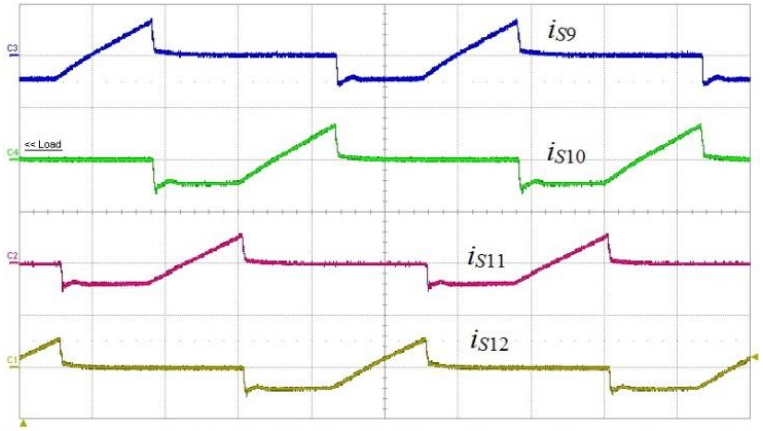


(c)

Fig. 5.18. Experimental results for output power of 500W at 300V (x-axis: 2 µs/div): (a) Voltage across the HF transformer v_{AB} and v_{CD} (50V/div) and currents through the primary windings i_{Llk1} and i_{Llk2} (50A/div), (b) Currents through the primary side MOSFETs (20A/div). (d) Currents through the secondary side MOSFETs (20A/div).

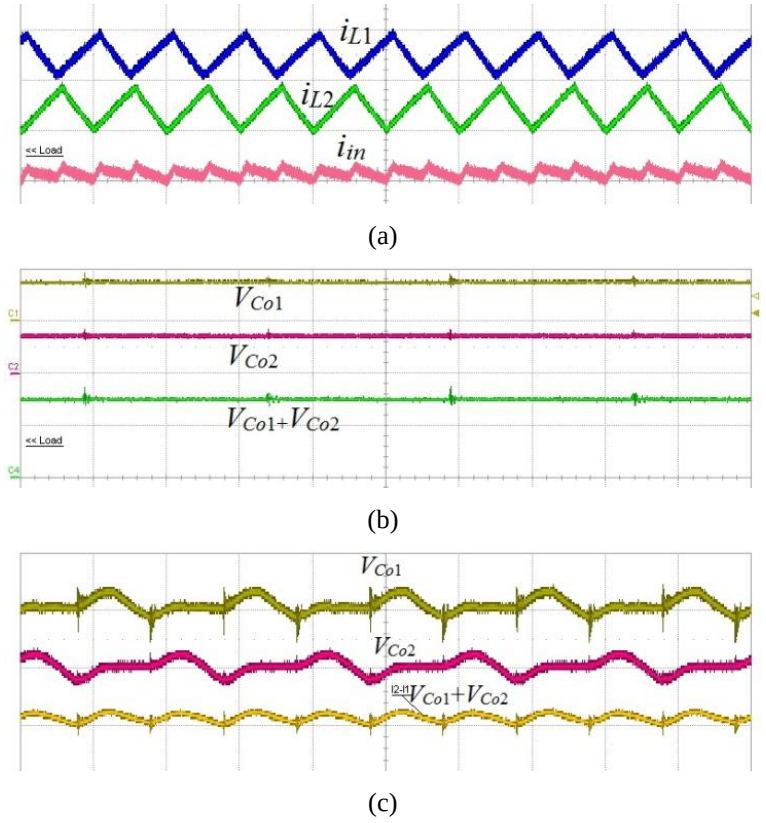


Fig. 5.19. Experimental results for output power of 500W at 300V (x-axis: 2 µs/div): (a) Boost inductor current waveforms i_{L1}, i_{L2} and input current i_{in} (2A/div, 5 µs/div), (b) Voltages across output capacitors of CELL 1(50V/div, 2 µs/div), (c) Scaled voltages across output capacitors of CELL 1(10V/div, 5 µs/div).

Input boost inductor currents $i(L_1)$, $i(L_2)$ with 2x device switching frequency and input current i_{in} with 4x device switching frequency are shown in Fig. 5.19 (a) and they aligns with simulation waveforms shown in Fig. 5.12 (a). The phase shift between $i(L_1)$ and $i(L_2)$ is close to 180 °. The ripple magnitudes are around 2A because the values of input boost inductors used in prototype are smaller than designed values. But ripple cancellation effect results in much smaller ripple in input current. The ratio of $\Delta\, i_{in}/i_{in}$ is around 1.3%. High input current ripple frequency and low ripple magnitude reduce the size of input capacitor and improve the utilization and lifetime of battery.

The voltage across output capacitors Co_1, Co_2 and the total voltage across them is displayed in Fig. 5.19. It can be seen that voltage across Co_1 and Co_2

are equal and balanced, which indicates that the proposed topology and modulation doesn't bring unbalance problems. Some minor parasitic ringing is noticed due to stray inductances of wiring connections and parasitic capacitances in PCB. As shown by Fig. 5.19 (c), Voltages across output capacitors Co_1, Co_2 are phase-shifted with each other by 180˚. The output voltage ripple is reduced due to ripple cancellation effect.

5.7 Summary and Conclusions

In this Chapter, four different topologies of soft-switching bi-directional DC/DC converters have been discussed and compared. CF-FBVD is selected, further studied and analyzed as a modular PEBB for FCVs/EVs. A detailed design procedure of interleaved two cells for the PISO configuration of the proposed multi-cell modular CF-FBVD has been presented. The secondary side modulation method discussed in Chapter 3 has been applied to clamp the device voltage at primary side with zero current commutation. It, therefore, eliminates the necessity for external active-clamp circuit or passive snubbers to absorb the switch turn-off voltage spike, a major challenge in traditional current-fed converters. Zero-current switching (ZCS) of primary side devices and zero-voltage switching (ZVS) of secondary side devices are achieved, which significantly reduces the switching losses. Interleaving approach is adopted over single-cell to increase the power handling capacity gaining the merits of lower input current ripple, reduction of passive components' size, reduced device voltage and current ratings, reduced conduction losses due to current sharing, and better thermal distribution. Considering input current is shared between interleaved cells, conduction loss of primary side, a

considerable part of total loss, is significantly reduced and higher efficiency can be achieved to obtain a compact and higher power density system. Steady state operation, analysis, and design of the proposed topology have been presented. Simulation is conducted over software package PSIM 9.0.4 to verify the accuracy of the proposed analysis and design. A 500 W prototype has been built and tested in the laboratory to validate the converter performance.

Chapter 6

Current-fed Three-Phase Bidirectional DC/DC Converter with Natural Clamping and Zero Current Commutation

6.1 Introduction

In Chapter 5, interleaved modular current-fed full-bridge voltage doubler (CF-FBVD) has been proposed and studied for high power applications. It provides the merits of modularity, scalability, high reliability, fault tolerance, and reduced filter requirements. The main issue with this interleaved CF-FBVD is higher number of devices and associated gate driving requirements. In this Chapter, current-fed three-phase bidirectional DC/DC converter with natural clamping and zero current commutation is investigated to obtain a trade-off among power transferring capacity, number of devices, cost, and efficiency.

A three-phase topology was introduced by Ziogas in the HF DC/DC conversion area [166]. Three-phase topology offers the following benefits: 1) Reduction in device current ratings, 2) Reduction in size of input and output filters due to increased 3x ripple frequency, 3) Lower average and RMS current through the devices owing to current sharing, which reduces the conduction losses, 4) Reduction in transformer size due to better core utilization [167-170]. Therefore, these merits make the three-phase topology a

better candidate for higher current applications compared to single-phase topology. Compared with multi-cell interleaved converter, three-phase converter has lesser number of components. A variety of three-phase current-fed DC/DC converters with active-clamping circuits have been proposed using [167-174]: full-bridge [171], half-ridge [172], and push-pull [173] configurations. As discussed in Chapter 3, like single-phase active-clamped converter, three-phase active-clamped topologies are also limited by high peak current, high circulating current at light load, and reduced boost capacity. In [174], a three-phase half-bridge converter with passive snubber is presented. The main issue is considerably low efficiency. Resonant soft-switching has been applied in three-phase DC/DC converters in [175-176]. However, they suffer from high voltage/current stress, circulating current and also a considerable increase in the volume of reactive power elements.

In Chapter 3, a secondary modulation technique is proposed to solve the voltage spike problem eliminating the necessity for external active-clamping circuit or passive snubbers. This technique is possible to be modified and extended for three-phase circuit as shown in Fig. 6.1. In the reverse direction, the asymmetrical duty control method [174] has been applied to obtain wide range of soft-switching. Steady-state operation of the converter is explained and its mathematical analysis is reported in Section 6.2. Detailed converter design procedure is illustrated in Section 6.3. Analysis and design are verified by simulation results using PSIM 9.0.4 in Section 6.4. Experimental results on a laboratory prototype of 750W are demonstrated to validate the converter performance in Section 6.5. This Chapter is concluded in Section 6.6.

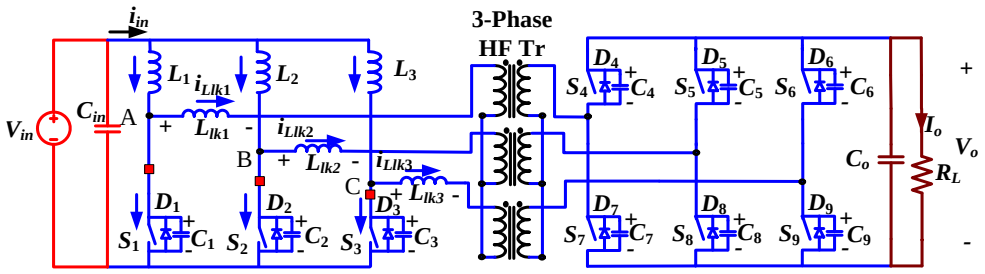


Fig. 6.1. Three-phase AC link snubberless current-fed isolated DC/DC converter.

6.2 Comparison of Three Current-fed Converters

In this Section, a theoretical comparison between three-phase active-clamped current-fed ZVS topology [167], single-phase ZCS topology [137], and proposed snubberless three-phase current-fed ZCS topology has been presented. The parameters, specifications and components of the theoretical prototypes are given as follows.

1) Specifications: Input voltage V_{in} = 42 V, output voltage V_o = 300 V, HF transformer turns ratio n=1.786, output power P_o =5kW, device switching frequency f_s = 100 kHz, I_{in} = $P_o/(\eta V_{in})$= 125.3A (η=0.95), $\frac{T_{DR}}{T_S} = \frac{n \cdot V_{in}}{V_o}$ =0.25, duty cycle d=0.8 (active-clamped ZVS [167]) and d=0.75 (single-phase ZCS [167] and proposed three-phase ZCS).

2) The single-phase ZCS topology: boost inductors: L = 50 μH, T300-60D, micrometals iron power cores, turns number N_L=26, 6 strands of AWG10 wires, r_L=2 mΩ; HF transformer: turns ratio n=1.8; E80/38/20, 3C95 ferrite cores; primary turns number N_p=20, 2000 strands AWG38 litz wires and r_{pri}=2.6 mΩ; secondary turns number N_s=36, 1000 strands AWG38 litz wires and r_{sec}=13.5mΩ. Primary switches: IXFK180N25T; secondary switches: FCH041N60F; series

inductors: L_{lk} = 3 μH, PC47RM14Z, air-gapped ferrite cores, turns number N=10, 2000 strands of AWG38 wires and r_{Llk}=1.5mΩ.

3) The three-phase active-clamped ZVS topology: The boost inductors: L = 60 μH, three T250-63, micrometals iron power cores, turns number N_L=26, 4 strands of AWG10 wires and r_L=1.8 mΩ. HF transformer: turns ratio n=1.8; three independent E65/32/27, 3C95 ferrite cores; primary turns number N_p=10, 1200 strands AWG38 litz wires and r_{pri}=2.5mΩ; secondary turns number N_s=18, 600 strands AWG38 litz wires and r_{sec}=9mΩ. Primary switches: IXFB170N30P; auxiliary clamping switches: IXFB170N30P; secondary switches: FCH041N60F; series inductors: L_{lk} = 0.7 μH, three PC47RM14Z, air-gapped ferrite cores, turns number N=4, 1200 strands of AWG38 wires and r_{Llk}=0.4mΩ.

4) The proposed three-phase ZCS topology: The boost inductors: L = 60 μH, three T250-63, micrometals iron power cores, turns number N_L=26, 4 strands of AWG10 wires and r_L=1.8 mΩ. HF transformer: turns ratio n=1.8; three independent E65/32/27, 3C95 ferrite cores; primary turns number N_p=10, 1200 strands AWG38 litz wires and r_{pri}=2.5mΩ; secondary turns number N_s=18, 600 strands AWG38 litz wires and r_{sec}=9mΩ. Primary switches: IXFK180N25T; secondary switches: FCH041N60F; series inductors: L_{lk} = 0.9 μH, three PC47RM14Z, air-gapped ferrite cores, turns number N=2, 1200 strands of AWG38 wires and r_{Llk}=0.2mΩ.

The comparison of critical voltage and current ratings has been illustrated in Table 6.1. It is clear from Table 6.1 that that peak current stress through the

transformer and the secondary side switches of proposed three-phase ZCS converter is considerably lower. In addition, devices' VA rating is comparatively low in the proposed topology resulting in better switch (silicon) utilization. Due to low effective duty cycle owing to transformer leakage, active-clamped current-fed topology has reduced boost capacity compared to proposed topology. The voltage across the primary switches of the proposed topology is clamped at lower voltage than active-clamped topology. Therefore, proposed topology needs devices of comparatively low voltage rating with low $R_{ds,on}$ results in lower conduction losses.

Table 6.2 gives the comparison of losses and efficiency between active-clamped ZVS, single-phase ZCS, and proposed three-phase ZCS topologies at full load condition. The loss is estimated from the loss model presented in [165]. Compared with three-phase active-clamped topology, the proposed three-phase ZCS topology completely eliminates the losses from auxiliary clamp circuit. Since the primary switches of the proposed topology are naturally clamped at lower voltage, the conduction loss are also reduced compared with active-clamped topology. Therefore, the proposed topology can achieve higher efficiency mainly due to reduced losses associated with the clamp circuit and the main primary switches. Compared with the single-phase ZCS topology, the proposed three-phase ZCS topology has lower average and RMS current through the devices owing to current sharing among three phases, resulting in significantly reduced conduction loss. Therefore, the proposed topology can achieve higher efficiency. The device stress and devices' VA rating of three-phase topology is also much lower.

Table 6.1: Comparison of parameters between three-phase active-clamped ZVS, single-phase ZCS, and proposed ZCS current-fed topologies.

Parameters	Three-phase active-clamped ZVS	Single-phase ZCS	Proposed three-phase ZCS
Peak current through transformer	$2I_{in}/3$ (83.5A)	$I_{in}/2$(62.7A)	$I_{in}/3$ (41.8A)
RMS current through transformer	$I_{in}\sqrt{\frac{2}{9}\cdot\frac{T_{DR}}{T_s}}$ (29.5A)	$I_{in}\sqrt{\frac{5-4d}{12}}$ (51.2A)	$I_{in}\sqrt{\frac{4-3d}{27}}$ (31.9A)
Peak current through primary switches	$2I_{in}/3$ (83.5A)	I_{in}(125.3A)	$2I_{in}/3$ (83.5A)
RMS current through primary switches	$I_{in}\sqrt{\cdot\left(\frac{2}{27}+\frac{d}{27}+\frac{2}{9}\cdot\frac{T_{DR}}{T_s}\right)}$ (50A)	$I_{in}\sqrt{\frac{2-d}{3}}$ (80.9A)	$I_{in}\sqrt{\frac{7-3d}{27}}$ (52.5A)
Peak current through clamping switches	$I_{in}/3$ (41.8A)	--	--
RMS current through clamping switches	$I_{in}\cdot\sqrt{(1-d)/27}$ (10.8A)	--	--
Peak current through secondary switches/diodes	$2I_{in}/3n$ (46.8A)	$I_{in}/2n$ (35.2A)	$I_{in}/3n$ (23.4A)
Average current through secondary diodes	$I_{DR,avg} = P_o/(3V_o)$ (5.6A)	$\bar{I}_{Dav}=\frac{I_{in}\cdot(3-2d)}{8n}$ (13.2A)	$\bar{I}_{D\_up,av}=\frac{I_{in}\cdot(10-9d)}{36n}$ (6.3A) $\bar{I}_{D\_below,av}=\frac{I_{in}\cdot(4-3d)}{18n}$ (6.8A)
RMS current through secondary switches	-	$I_{S,rms}=\frac{I_{in}}{4n}\sqrt{\frac{2d-1}{3}}$ (7.2A)	$I_{S\_up,rms}=\frac{I_{in}}{9n}\sqrt{\frac{3d-2}{2}}$ (2.76A) $I_{S\_below,rms}=\frac{I_{in}}{9n}\sqrt{3d-2}$ (3.89A)
Voltage across primary switches	$\frac{V_{in}}{1-d}$ (210V)	$\frac{V_o}{n}$ (168V)	$\frac{V_o}{n}$ (168V)
Primary devices VA rating	10.5 kVA	13.6kVA	8.8 kVA

Table 6.2: Comparison of losses and efficiency between three-phase active-clamped ZVS, single-phase ZCS, and proposed ZCS current-fed topologies at full load condition.

Loss type	Three-phase active-clamped ZVS	Single-phase ZCS	Proposed three-phase ZCS
Primary switches conduction losses	135W	168.8W	106.6W
Primary switches switching losses	15.6W	8.5W	12.7W
Secondary switches /diodes losses	40.3W	70.8W	49.2W
Boost inductor losses	Core loss (8.1W) Copper loss(11.2W)	Core loss (8.1W) Copper loss(15.6W)	Core loss (8.9W) Copper loss(11.2W)
HF transformer losses	Core loss (4.0W) Copper loss (13.9W)	Core loss (1.3W) Copper loss (17.7W)	Core loss (4.0W) Copper loss (16.3W)
Series inductors loss	Core loss (1.3W) Copper loss (1.2W)	Core loss (1.5W) Copper loss (3.9W)	Core loss (1.5W) Copper loss (0.6W)
Clamping switches conduction losses	10.8W	-	-
Clamping switches switching losses	4.2W	-	-
Total losses	245.6W	296.2W	211W
Efficiency	95.3%	94.4%	96%

The calculated efficiency of these two topologies versus output power for load conditions from 10% to 100% is shown in Fig.6.2. It is clear to find that the proposed ZCS converter achieves high efficiency than active-clamped converter at high load condition. The efficiency improvement of the converter is mainly resulting from reduced losses associated with clamp circuit and main primary switches.

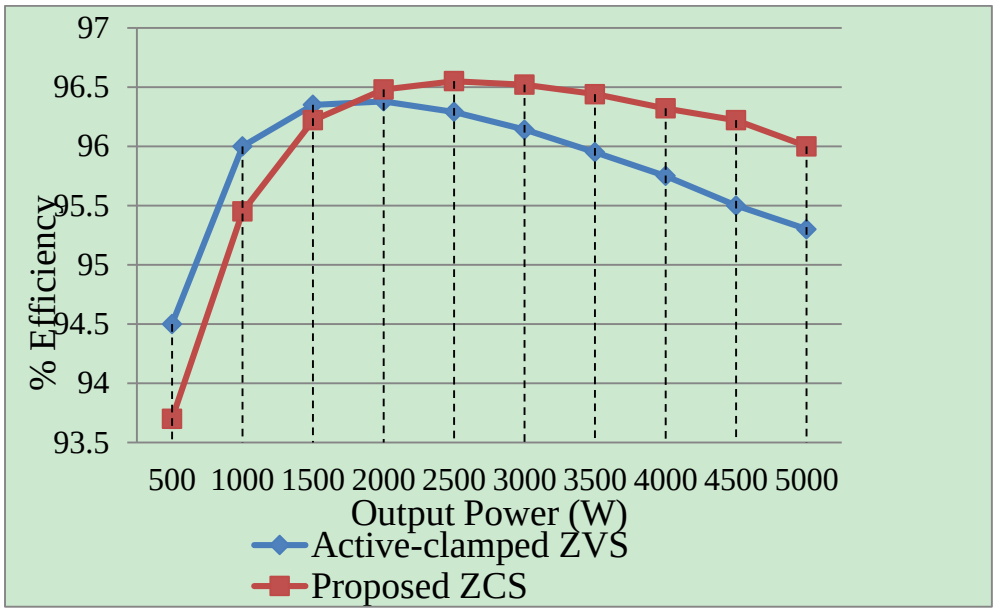


Fig. 6.2. Calculated efficiency of the proposed three-phase ZCS converter and three-phase active-clamped ZVS converter.

6.3 Operation and Analysis of the Converter

In this Section, steady-state operation and analysis of the proposed bidirectional current-fed three-phase topology are presented. For the sake of simplicity, the following assumptions are made to study the operation and explain the analysis of the converter: a) Boost inductors L_1, L_2 and L_3 are large enough to maintain constant currents through them. b) All components are ideal and lossless. c) Series inductors L_{lk1}, L_{lk2} and L_{lk3} include the leakage

inductances of HF transformers and are assumed equal to L_{lk}. d) Magnetizing inductances of the transformers are infinitely large.

The modulation signals of secondary switches are illustrated in Fig. 6.3 and briefly explained here. The primary side: the primary switches $S_1 \sim S_3$ are operated with gating signals phase-shifted by 120^o with an overlap. The overlap varies with duty cycle. The duty cycle is defined in Fig. 6.3. The secondary side: Secondary devices S_4 & S_8 are turned-off synchronously with primary devices S_2, S_5 & S_9 are turned-off synchronously with S_3, and S_6 & S_7 are turned-off synchronously with S_1. Secondary side devices $S_4 \sim S_9$ can be turned-on at any instant within the range illustrated by the black shaded lines in Fig. 6.3. The turn-on procedure of S_4 & S_8 is explained here as an example. Ideally switch S_4 can be turned on anytime in between the moment when S_1 is turned-off and the moment $t=t_3$ (for ZVS turn-on) at which phase-A current changes polarity. Switch S_8 can be turned-on anytime between the moment when S_3 is turned-off and the moment $t=t_1$ (for ZVS turn-on). Practically if switch S_8 is turned-on later than the moment when S_1 is tuned-off, the leakage inductance L_{lk2} may resonate with the parasitic capacitances of S_5 and S_8. Therefore in our experiment, S_4 and S_1 are turned-on synchronously and S_8 and S_3 are turned on synchronously. The modulation signals for the rest secondary switches follow the same principles as illustrated in Fig. 6.3. The steady-state operation of the topology during different intervals in a $1/3^{rd}$ of HF cycle is explained using the equivalent circuits shown in Fig. 6.4.

Interval 1 (Fig. 6.4a; $t_o < t < t_1$): In this interval, primary side devices S_2 and S_3 and body diodes D_4 and D_9 of secondary side switches are conducting. The currents through series inductors L_{lk1} and L_{lk3} are constant. Power is

transferred to the load through three-phase HF transformer. The non-conducting secondary devices are blocking output voltage V_o and the non-conducting primary device S_1 is blocking reflected output voltage V_o/n. The values of currents through various components are: i_{S1}=0, i_{S2} =I_{in}/3, i_{S3}=2I_{in}/3, i_{Llk1}= I_{in}/3, i_{Llk2}= 0, i_{Llk3}=-I_{in}/3, i_{D4} = i_{D9}= I_{in}/3n. Voltage across the switches S_1: V_{S1} = V_o/n. Voltage across the switches S_5, S_6, S_7 and S_8: V_{S5}=V_{S6} =V_{S7} =V_o, V_{S8}=0.

Interval 2 (Fig. 6.4b; $t_1 < t < t_2$): At $t = t_1$, primary switches S_1 is turned-on. Snubber capacitor C_1 discharges in a very short period of time.

Interval 3 (Fig. 6.4c; $t_2 < t < t_3$): Now all primary devices S_1 ~ S_3 are conducting. Reflected output voltage V_o/n appears across series inductors L_{lk1}, L_{lk2} and L_{lk3} and causes their currents to increase/decrease linearly. It causes currents through previously conducting devices S_2 and S_3 to reduce linearly and incoming switch S_1 to rise. The currents through various components are given by

$$i_{Llk1} = \frac{I_{in}}{3} - \frac{2 \cdot V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_2) \tag{6-1}$$

$$i_{Llk2} = \frac{V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_2) \tag{6-2}$$

$$i_{Llk3} = -\frac{I_{in}}{3} + \frac{V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_2) \tag{6-3}$$

$$i_{S1} = \frac{2 \cdot V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_2) \tag{6-4}$$

$$i_{S2} = \frac{I_{in}}{3} - \frac{V_o}{3n \cdot L_{lk}} \cdot (t - t_2) \tag{6-5}$$

$$i_{S3} = \frac{2 \cdot I_{in}}{3} - \frac{V_o}{3n \cdot L_{lk}} \cdot (t - t_2) \tag{6-6}$$

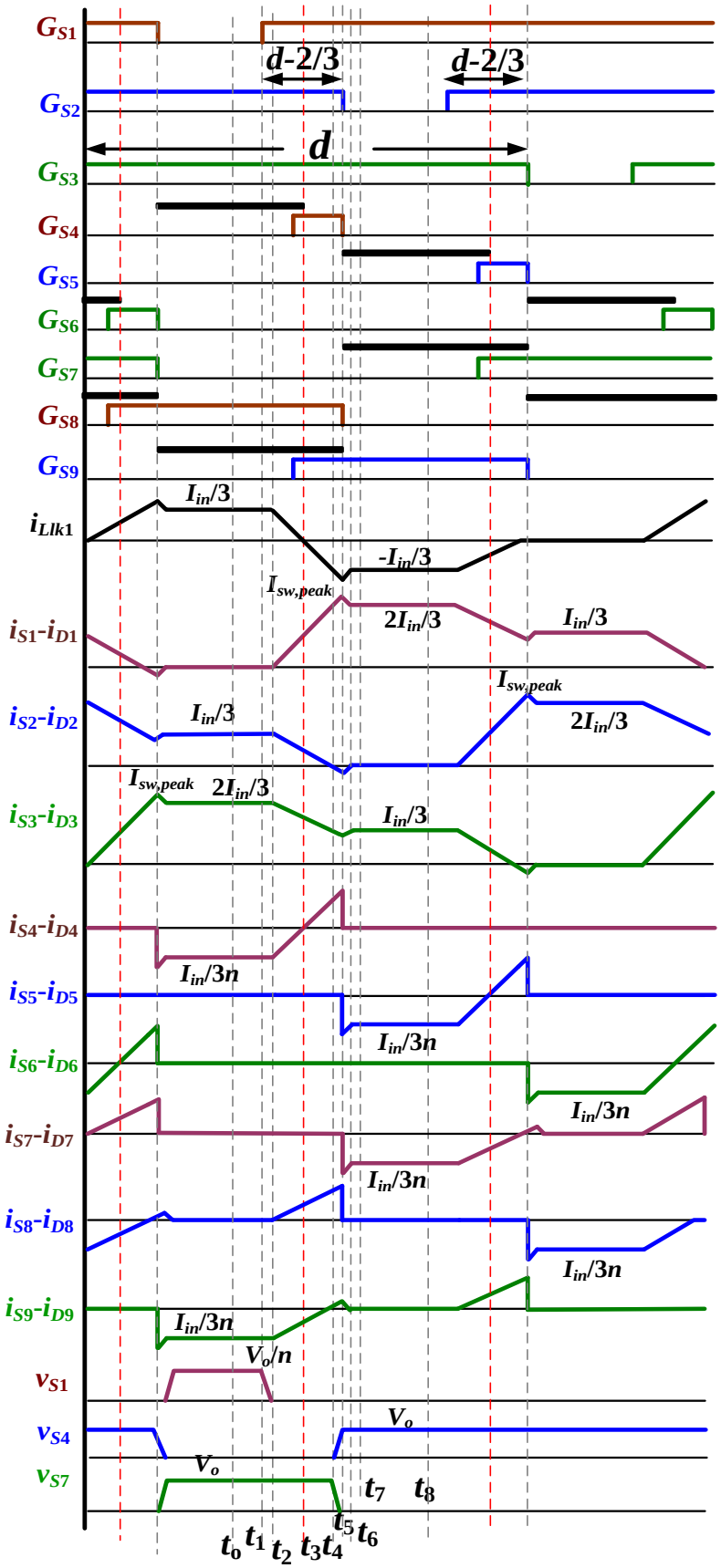
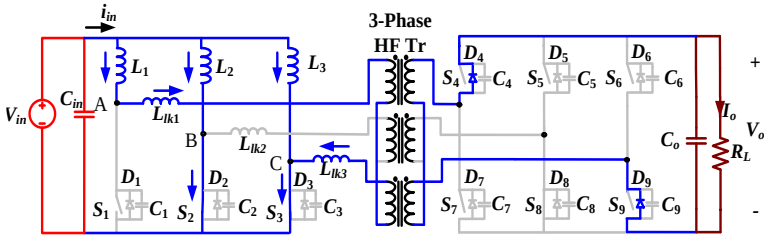


Fig. 6.3. Operating waveforms of proposed ZCS current-fed three-phase converter shown in Fig. 6.1.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3-Phase
HF Tr
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B
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L_1
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L_{lk1}
L_{lk2}
L_{lk3}
D_1
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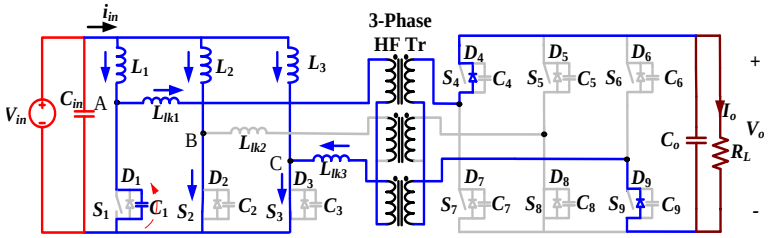
(a)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HF Tr
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L_{lk3}
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D_3
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D_6
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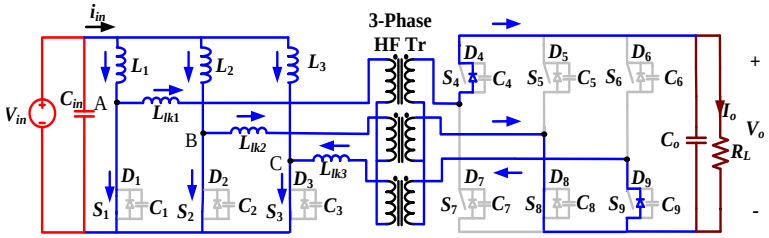
(b)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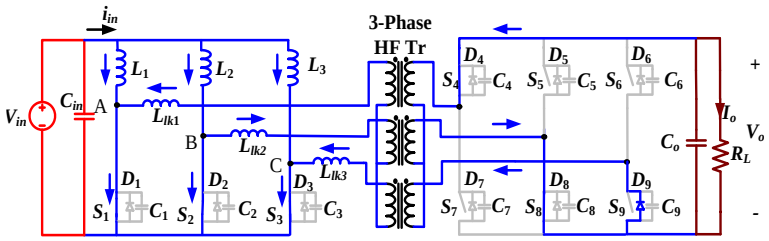
(c)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L_{lk3}
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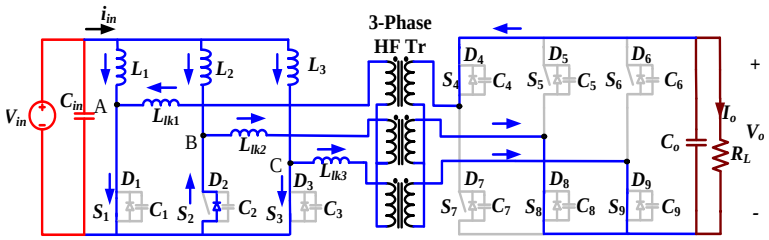
(d)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D_2
D_3
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C_1
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C_2
S_3
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D_4
D_5
D_6
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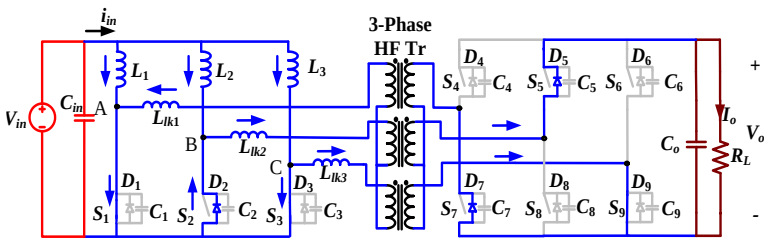
(e)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L_{lk1}
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L_{lk3}
D_1
D_2
D_3
S_1
C_1
S_2
C_2
S_3
C_3
D_4
D_5
D_6
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(f)

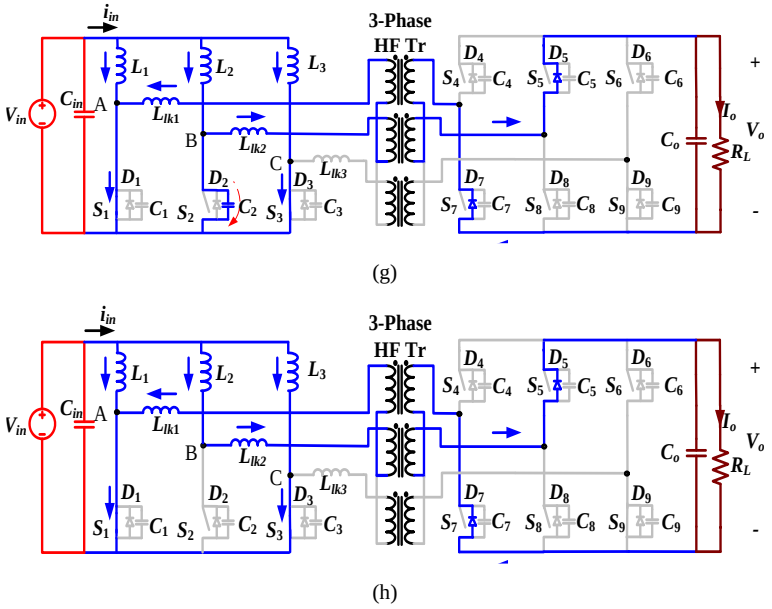


Fig. 6.4. Equivalent circuits during different intervals of operation of the proposed converter in boost mode.

Since voltages across S_4, and S_9 are zero owing to their respective body diodes conduction, these switches can be gated for ZVS turn on. At the end of this interval $t=t_3$, D_4 commutates naturally. Primary current i_{Llk1} reaches zero and ready to change polarity. Final values are: $i_{Llk1}=0$, $i_{Llk2}= I_{in}/6$, $i_{Llk3}=-I_{in}/6$, $i_{S1}=I_{in}/3$, $i_{S2}=I_{in}/6$, $i_{S3}= I_{in}/2$, $i_{D4}= 0$, $i_{S8}= I_{in}/6n$, $i_{D9}= I_{in}/6n$.

Interval 4 (Fig. 6.4d; $t_3 < t < t_4$): In this interval, secondary device S_4 and S_9 are turned on with ZVS. Currents through all the switching devices continue increasing or decreasing with the same slope as interval 3. At the end of this interval, primary device S_2 commutates naturally with ZCC obtaining ZCS. Input current I_{in} is taken over by other devices S_1 and S_3, and transformer current i_{Llk1} changes polarity. Final values are: $i_{Llk1}=-I_{in}/3$, $i_{Llk2}= I_{in}/3$, $i_{Llk3}=0$, $i_{S1}=2I_{in}/3$, $i_{S2}=0$, $i_{S3}= I_{in}/3$, $i_{S4}= I_{in}/3n$, $i_{S8}= I_{in}/3n$, $i_{D9}=0$.

Interval 5 (Fig. 6.4e; $t_4 < t < t_5$): In this interval, leakage inductance current i_{Llk1} keeps decreasing. Body diode D_2 starts conducting causing extended zero voltage across the outgoing switch S_2 to ensure ZCS turn-off.

Current i_{Llk3} changes polarity and starts increasing in positive direction. At the end of this interval, current through S_1 reaches its peak value. This interval should be very short to limit the peak current though components, and so their kVA ratings. Final values are: i_{Llk1}=-$I_{lk,peak}$, i_{Llk2}= $I_{lk,peak}$, i_{Llk3}= $I_{D2,peak}$, i_{S1}=$I_{sw,peak}$, i_{D2}= $I_{D2,peak}$, i_{S3}= I_{in}/3- $I_{D2,peak}$. The currents through operating components are given by

$$i_{Llk1} = -\frac{I_{in}}{3} - \frac{2 \cdot V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_4) \tag{6-7}$$

$$i_{Llk2} = \frac{I_{in}}{3} + \frac{V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_4) \tag{6-8}$$

$$i_{Llk3} = \frac{V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_4) \tag{6-9}$$

$$i_{S1} = \frac{2 \cdot I_{in}}{3} + \frac{2 \cdot V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_4) \tag{6-10}$$

$$i_{D2} = \frac{V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_4) \tag{6-11}$$

$$i_{S3} = \frac{I_{in}}{3} - \frac{V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_4) \tag{6-12}$$

Interval 6 (Fig. 6.4f; $t_5 < t < t_6$): During this interval, secondary switches S_4 and S_8 are turned-off. Body diodes of switches S_5 and S_7 take over the current immediately. Therefore, the voltage across the transformer reverses polarity and the current through L_{lk1}, starts increasing. The currents through S_2 and body diodes D_5 and D_7 start decreasing.

The currents through operating components are given by

$$i_{Llk1} = -I_{lk,peak} + \frac{V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_5) \tag{6-13}$$

$$i_{Llk2} = I_{lk,peak} - \frac{2 \cdot V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_5) \tag{6-14}$$

$$i_{Llk3} = I_{D2,peak} - \frac{V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_5) \tag{6-15}$$

$$i_{S1} = I_{sw,peak} - \frac{V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_5) \tag{6-16}$$

$$i_{D2} = I_{D2,peak} - \frac{2 \cdot V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_5) \tag{6-17}$$

$$i_{S3} = \frac{I_{in}}{3} - I_{D2,peak} - \frac{V_o}{3 \cdot n \cdot L_{lk}} \cdot (t - t_4) \tag{6-18}$$

At the end of this interval, current through D_2 reduces to zero. Final values: i_{Llk1}=-I_{in}/3, i_{Llk2}= I_{in}/3, i_{Llk3}=0, i_{S1}=2I_{in}/3, i_{S2}=*0*, i_{S3}= I_{in}/3, i_{D5}= I_{in}/3*n*, i_{D7}= I_{in}/3*n*, i_{D9}=0.

Interval 7 (Fig. 6.4g; $t_6 < t < t_7$): In this interval, snubber capacitor C_2 charges to V_o/n in a short period of time. Switches S_2 is in forward blocking mode now.

Interval 8 (Fig. 6.4h; $t_7 < t < t_8$): In this interval, currents through S_1 and S_3, and transformer are constant. Current through anti-parallel body diodes of the secondary switches D_5 and D_7 is I_{in}/n. Voltage across the switches S_2 V_{S2} = V_o/n. Voltage across the switches S_4, S_6, S_8 and S_9: V_{S4}=V_{S6} =V_{S8} = V_o , V_{S9}=0. In this one third HF cycle, current has transferred from one phase of primary to the other one.

Zero current commutation (ZCC) and natural voltage clamping (NVC) concepts are summarized here. When all three primary switches are on, reflected output voltage V_o/n appearing across the transformer primary is used to divert the current from one switch to other two switches through the transformer. This causes the currents through two conducting switches to rise

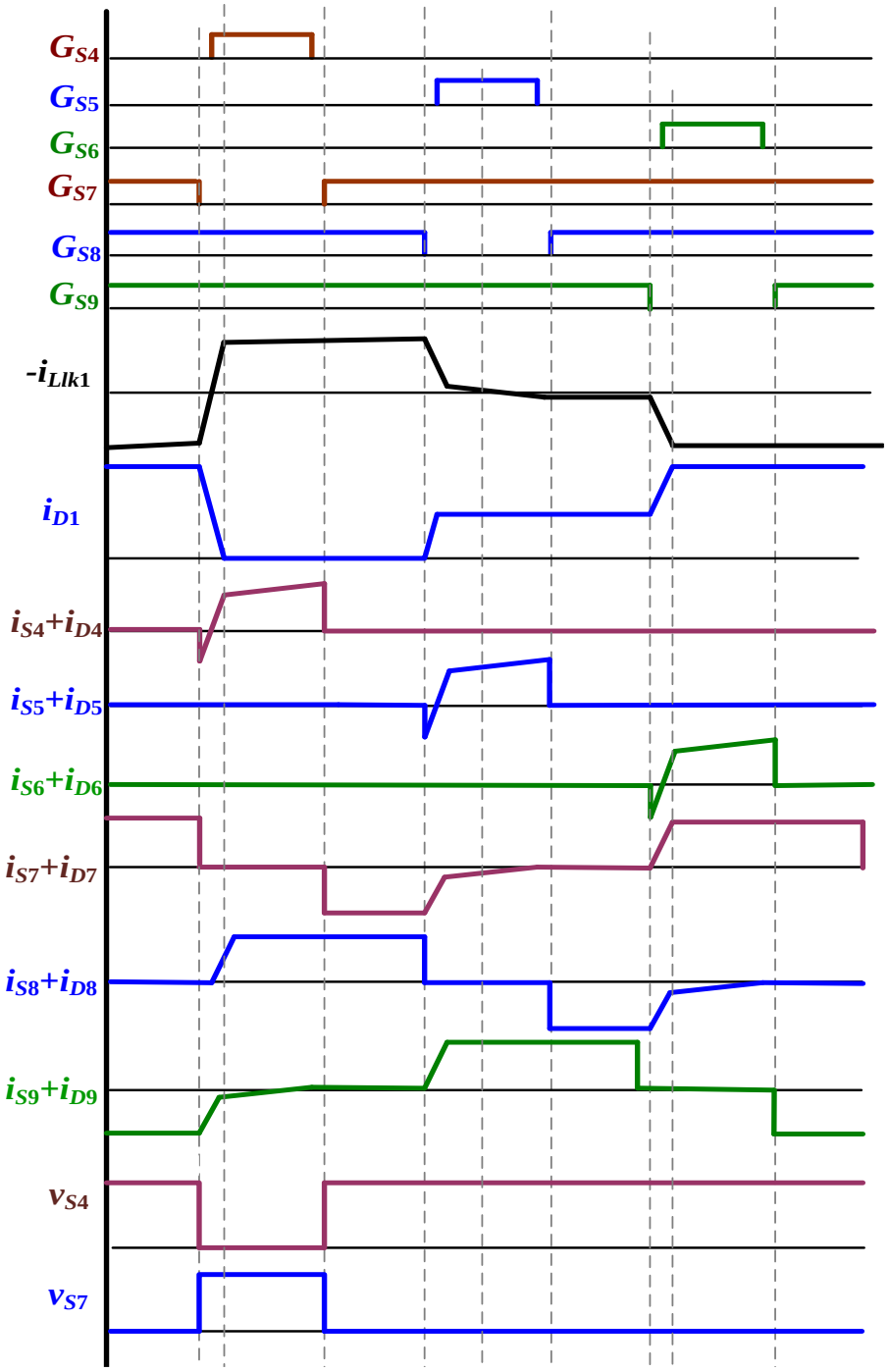


Fig. 6.5. Operating waveforms of the proposed three-phase converter in buck mode.

and current through outgoing switch to fall to zero naturally resulting in ZCC. Later its body diode starts conducting and now the gating signal is removed leading to ZCS turn-off of the device. Commutated device's capacitance starts charging with natural voltage clamping. ZCC and NVC are solely achieved

through the modulation (software approach) without external circuit making it novel and snubberless.

In the reverse direction (buck mode), the converter acts as a standard voltage-fed full-bridge isolated DC/DC converter with inductive output filter. As shown by Fig. 6.5, standard phase-shift modulation can be employed to achieve ZVS of high voltage side and ZCS of low voltage side with relatively low circulating current. It has been detailed reported in [174] and therefore, this thesis does not emphasize on it.

6.4 Design of the Converter

In this Section, converter design is illustrated by a design example for the following specifications: input voltage V_{in} = 42 V, output voltage V_o = 300V, output power P_o = 750W, switching frequency f_s = 100 kHz. The design equations are presented to determine the components' ratings. It helps in components selection as well as to develop the loss model of the converter theoretically.

(1) Average input current is $I_{in} = P_o/(\eta V_{in})$. Assuming an ideal efficiency η of 95%, I_{in} = 18.7 A.

(2) Maximum voltage across the primary switches is

$$V_{P,SW} = \frac{V_o}{n} \tag{6-19}$$

(3) Voltage conversion ratio or input and output voltages are related as

$$V_o = \frac{n \cdot V_{in}}{(1-d)} \tag{6-20}$$

where d is the duty cycle of primary switches.

(4) Leakage inductance of the transformer or series inductance L_{lk} is calculated by the following equation

$$L_{lk} = \frac{V_o \cdot (d - \frac{2}{3})}{n \cdot I_{in} \cdot f_s} \tag{6-21}$$

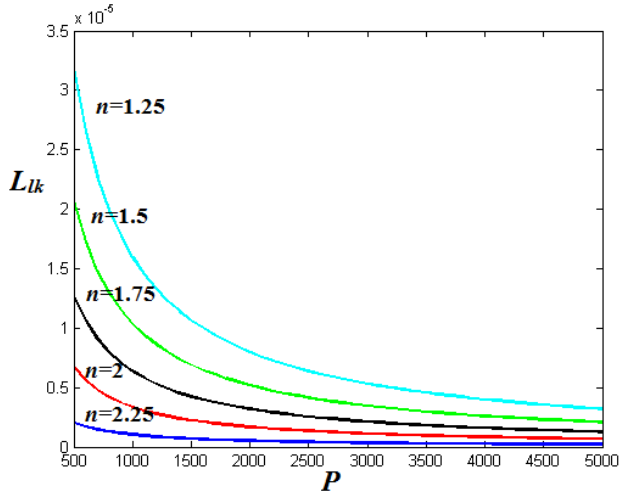
(5) RMS current through the transformer primary is given by

$$I_{Llk,rms} = I_{in} \sqrt{\frac{4 - 3d}{27}} \tag{6-22}$$

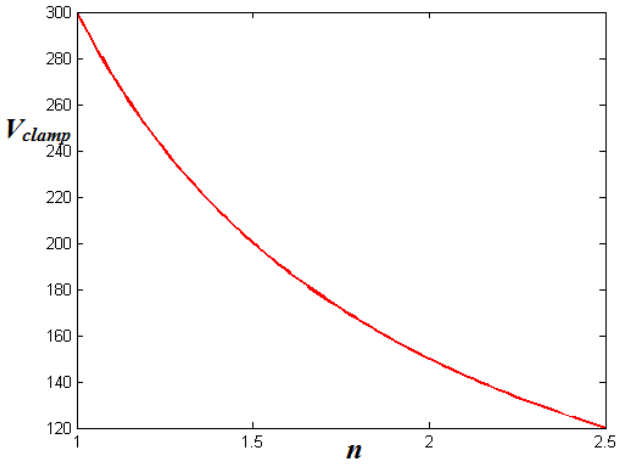
(6) The current and voltage stress of major components are given in Table 6.3. Fig. 6.6 (a) shows variation of series inductance L_{lk} (H) with respect to power transferring ability P (W) for five values of turns-ratio. When turns-ratio n=2.25, the maximum duty cycle d=0.685. For n=2, the maximum duty cycle d=0.72. Since the duty cycle should be kept higher than 0.66, limited duty cycle range will reduce control flexibility. The value of L_{lk} decreases with the increase in turns-ratio. It is also difficult to realize low leakage inductance with high turns-ratio. In addition, higher turns-ratio may lead to more transformer loss because of higher copper loss, higher eddy current from proximity effect and higher core loss due to larger size.

However, increasing the turns-ratio can reduce the maximum voltage across the primary switches, which permits use of low voltage devices with low on-state resistance (as shown by Fig. 6.6 (b)). Thus conduction losses in the primary side semiconductor devices can be significantly reduced. An optimum value of n =1.78 at d = 0.75 are selected to achieve low overall conduction losses for the given specifications [177]. Leakage inductance from

(6-21) is calculated as L_{lk} = 7.5 µH. The maximum voltage across the primary switches is $V_{P,SW}$ = 168V. Voltage rating of the secondary switches equals output voltage V_o = 300V. For the primary switches, MOSFET STW75NF30 (V_{ds} = 300 V, I_D = 60 A, R_{dson} = 37 mΩ) are selected. For the secondary switches MOSFET IPP60R125CP (V_{ds} = 650 V, I_D = 25 A, R_{dson} = 0.125 Ω) are selected.



(a)



(b)

Fig. 6.6. Variation of (a) Series inductance L_{lk} (H) with respect to power transferring ability P (W), and (b) Clamped voltage across primary switches V_{clamp} (V) for various transformer turns-ratio n.

Table 6.3: Current and voltage stress of major components.

Components	**Current Stress**			**Voltage Stress**
	Peak Current	Average Current	RMS Current	Peak voltage
Primary Switches $S_1 \sim S_3$	$2I_{in}/3$ (12.5A)	$\bar{I}_{P,av} = \frac{I_{in}}{3}$ (6.23A)	$I_{P,rms} = I_{in}\sqrt{\frac{7-3d}{27}}$ (7.84A)	V_o/n (168V)
Secondary Switches $S_4 \sim S_6$	$I_{in}/3n$ (3.5A)	$\bar{I}_{S\_up,av} = \frac{I_{in}(3d-2)}{36 \cdot n}$ (0.07A)	$I_{S\_up,rms} = \frac{I_{in}}{9n}\sqrt{\frac{3d-2}{2}}$ (0.41A)	V_o (300V)
Secondary Switches $S_7 \sim S_9$	$I_{in}/3n$ (3.5A)	$\bar{I}_{S\_below,av} = \frac{I_{in}(3d-2)}{18 \cdot n}$ (0.15A)	$I_{S\_below,rms} = \frac{I_{in}}{9n}\sqrt{3d-2}$ (0.58A)	V_o (300V)
Secondary Switches Body Diodes $D_4 \sim D_6$	$I_{in}/3n$ (3.5A)	$\bar{I}_{D\_up,av} = \frac{I_{in} \cdot (10-9d)}{36n}$ (0.95A)	$I_{D\_up,rms} = \frac{I_{in}}{9n}\sqrt{\frac{16-15d}{2}}$ (1.8A)	V_o (300V)
Secondary Switches Body Diodes $D_7 \sim D_9$	$I_{in}/3n$ (3.5A)	$\bar{I}_{D\_below,av} = \frac{I_{in} \cdot (4-3d)}{18n}$ (1.02A)	$I_{D\_below,rms} = \frac{I_{in}}{9n}\sqrt{7-6d}$ (1.84A)	V_o (300V)

(7) Value of each boost inductor is given by

$$L = \frac{V_{in} \cdot d}{\Delta I_{in} \cdot f_s} \tag{6-23}$$

where ΔI_{in} is the boost inductor ripple current. For ΔI_{in} = 1 A, L = 315 µH. For the boost inductor with high dc offset current here, dc winding losses and core saturation are the main limitations. To prevent the core from saturation, ferrite core 3C95ETD49 with 3mm air-gap is selected. 20 strands of SWG30 wires are used. Turns number is N_L=46 and measured value of boost inductor is L = 340 µH.

(8) HF transformer: Three independent HF transformers connected in Y-Y are employed. Ferrite core 3C95ETD49 with 16.9 cm^4 is chosen. Primary side turns number is N_1=26 and 20 strands of SWG30 wires are used. The secondary side turns number is N_2=46 and one strand of SWG21 wire is used. The leakage inductances of the transformer: L_{lk1}=1.13 µH, L_{lk2}= 1.19 µH and

L_{lk3}=1.26 µH. Their values are lower than the design value L_{lk} = 7.5 µH. Three additional external inductors using RM14PC40Z cores are connected in series.

6.5 Simulation and Experimental Results

A laboratory prototype rated at 750W as shown in Fig. 6.7 has been developed in research lab to experimentally demonstrate its performance. The proposed converter has been simulated for the above calculated components' values using software package PSIM 9.0.4. The converter has been tested on both boost mode (discharging mode) and buck mode (charging mode). The simulation and experimental results are shown in this Section.

6.5.1 Boost Mode (Discharging Mode)

The specifications of the boost mode: battery voltage V_{in} = 42 V, dc bus voltage V_o = 300 V, discharging power P= 750W, device switching frequency f_s = 100 kHz. Energy is transferred from the battery to the dc bus.

Simulation results are shown in Fig. 6.8 and Fig. 6.10. Fig. 6.8 and Fig. 6.10 coincide exactly with the theoretically predicted waveforms as shown in Fig. 6.2. It verifies the steady-state operation and analysis of the converter and proposed secondary modulation technique explained in Section II.

Experimental results are shown in Fig. 6.9 and Fig. 6.11. Experimental results match closely with the theoretical operating waveforms (Fig. 6.3) and the relevant simulation results. ZCS of primary switches and ZVS of secondary switches are clearly demonstrated by both simulation results and experimental results. Simulation waveforms in Fig. 6.8 (a) and

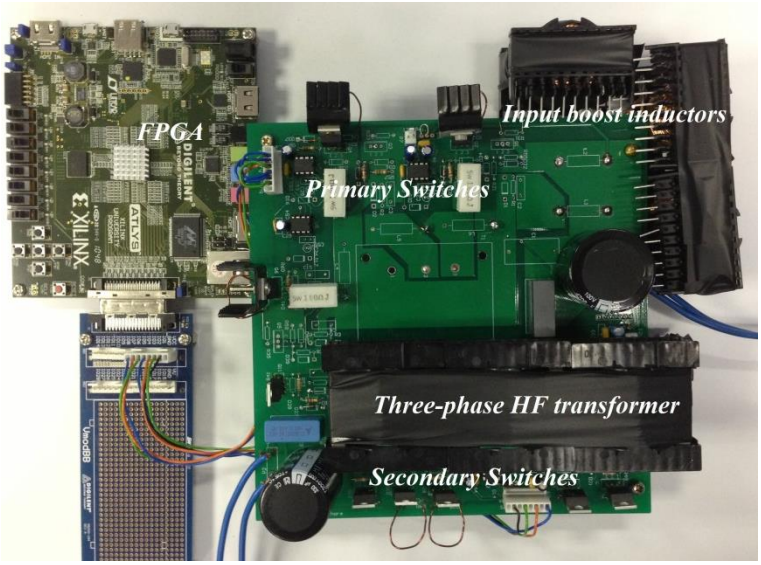
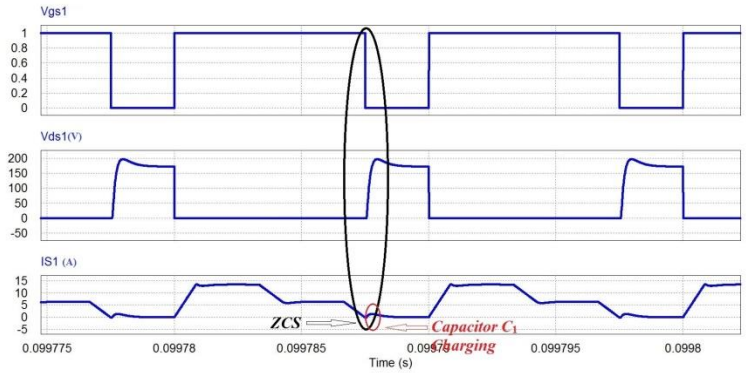


Fig. 6.7. Photograph of the laboratory prototype.

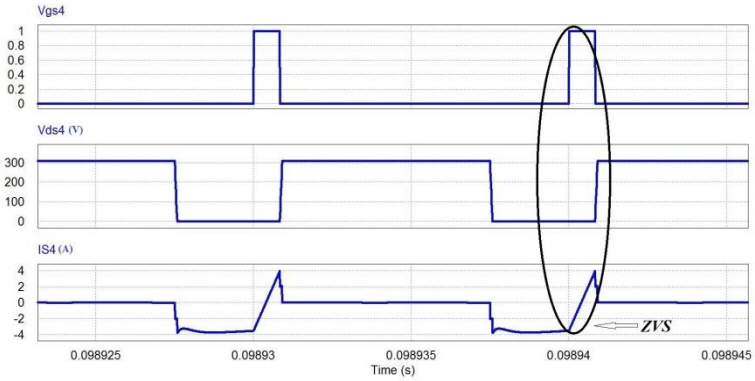
experimental results in Fig. 6.9(a) for output power of 750W at 300V show the gating signal to the primary switch $V_{gs,S1}$ is removed first before voltage $V_{ds,S1}$ starts rising. There is a clear gap between these two waveforms. The switch current naturally falls to zero because of proposed modulation and then becomes negative due to body diode conduction confirming the ZCC of primary switches. The conduction of body diode is more obvious for partial load condition as shown by Fig. 6.11(a). It should be observed that the voltage across the primary devices $V_{ds,S1}$ is naturally clamped without additional active-clamp or passive snubber. Current sensors are placed in the locations as illustrated by the red square pads in Fig. 6.1, which indicates the measured current waveform i_{S1} which includes the charging current of capacitor C_1. In waveforms Fig. 6.8(a) and Fig. 6.9(a), there is a small positive pulse of current showing up due to the charging of capacitor C_1 and $V_{ds,S1}$ is rising. Fig. 6.8(b)-(c) and Fig. 6.9(b)-(c) clearly indicates the ZVS turn on of the secondary switches. Gating signals to secondary switches $V_{gs,S4}$ (Top switch S_4) $V_{gs,S7}$ (Bottom switch S_7) appears when voltage across them $V_{ds,S4}$ and $V_{ds,S7}$,

respectively is zero already. Besides, its body diode conducts prior to switch conduction causing zero voltage across the secondary switches confirming their ZVS.

Inductor currents i_{L1}, i_{L2}, and i_{L3} and input current i_{in} with 3x device switching frequency are shown in Fig. 6.8(e) and Fig. 6.9(e). The phase shift among i_{L1}, i_{L2}, and i_{L3} is close to 120 °. Ripple cancellation effect results in much smaller ripple in input current. The ripple magnitudes of i_{L1}, i_{L2}, and i_{L3} are around 0.9A and of i_{in} is only 0.3A. High input current ripple frequency and low ripple magnitude reduce the size of input capacitor and improve the utilization and lifetime of battery. Similarly, simulation waveforms and experimental results at 50% load are presented in Fig. 6.10 and Fig. 6.11.



(a)



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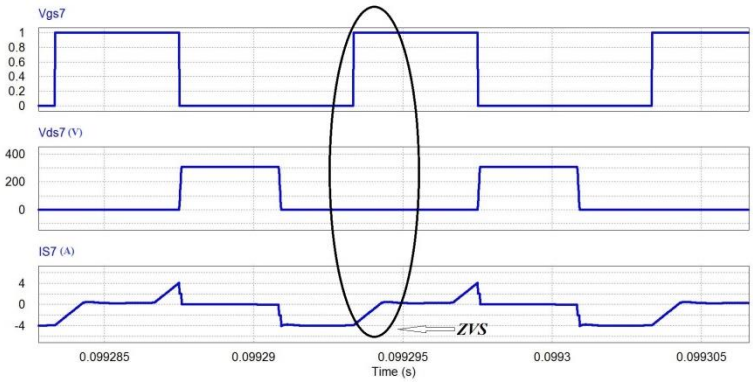

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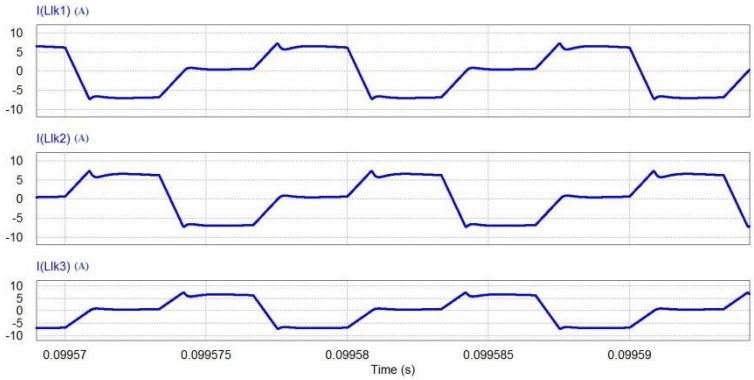

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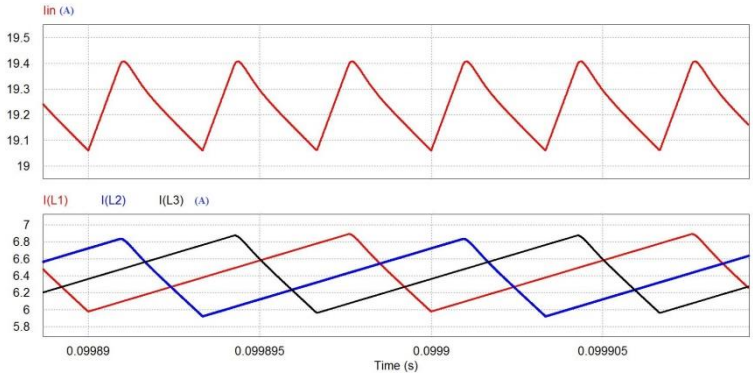

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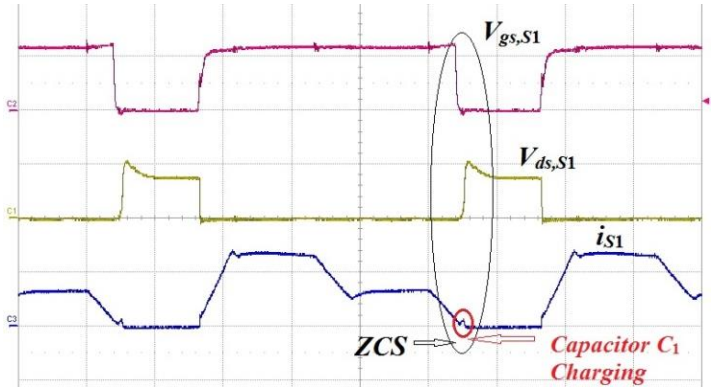
Fig. 6.8. Simulation waveforms at 750W power (boost mode).



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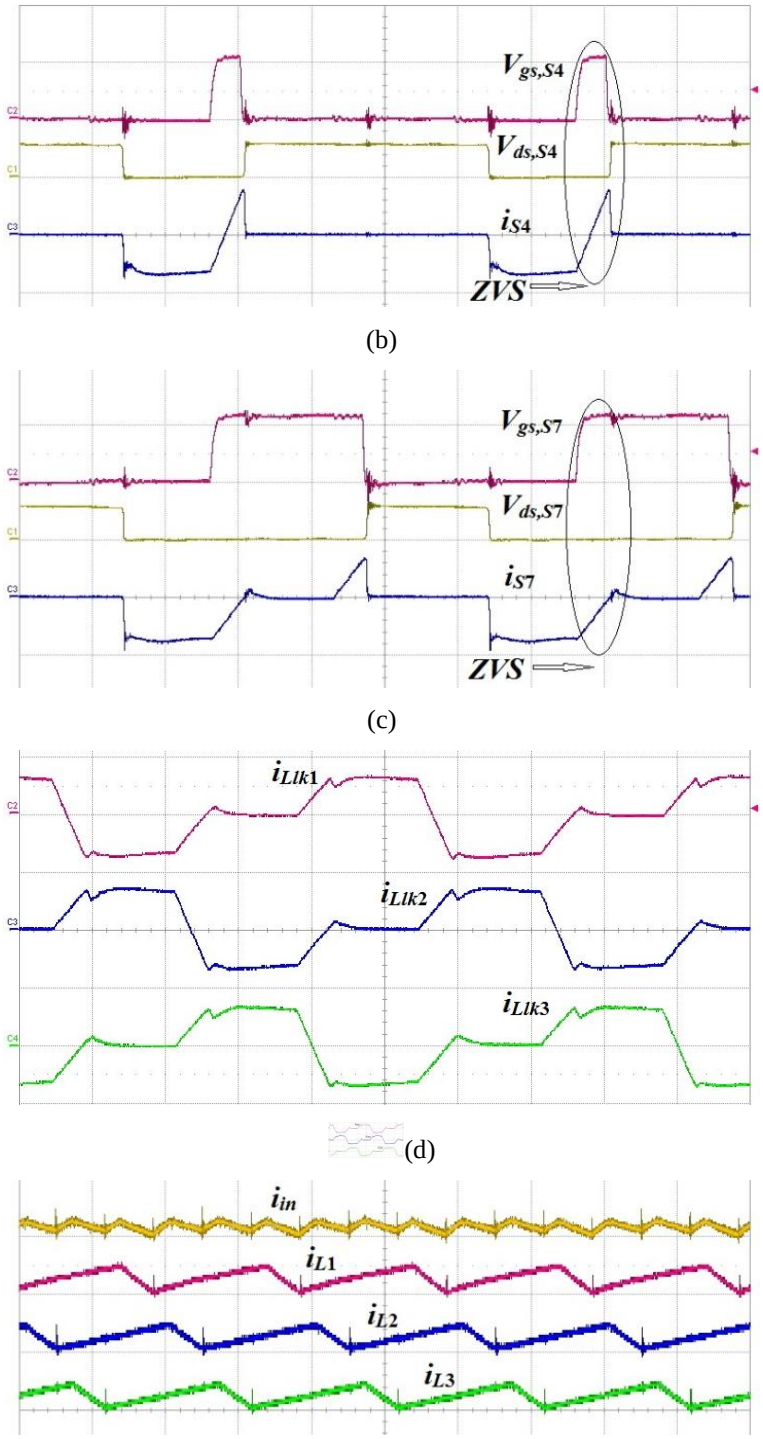
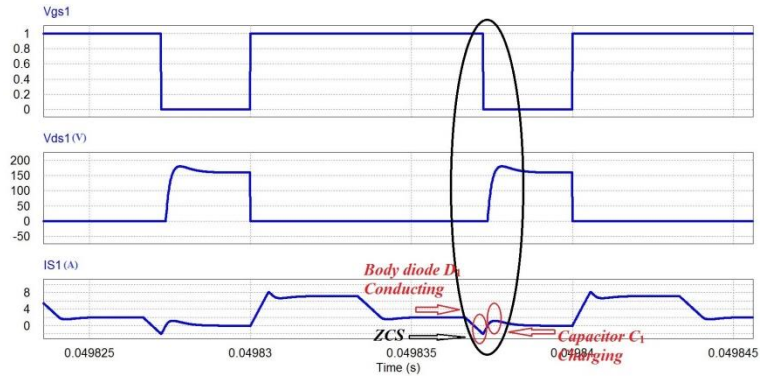


Fig. 6.9. Experimental results for output power of 750W at 300V (boost mode). (a) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (200V/div) of primary side device S_1 and current through it (10A/div). (b) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (500V/div) across secondary side device S_4 and current through it (5A/div). (c) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (500V/div) across secondary side device S_7 and current through it (5A/div). (d) Currents through series inductors i_{Llk1}, i_{Llk2}, and i_{Llk3} (10A/div), (e) Input current i_{in} and boost inductors currents i_{L1}, i_{L2}, and i_{L3} (2A/div).



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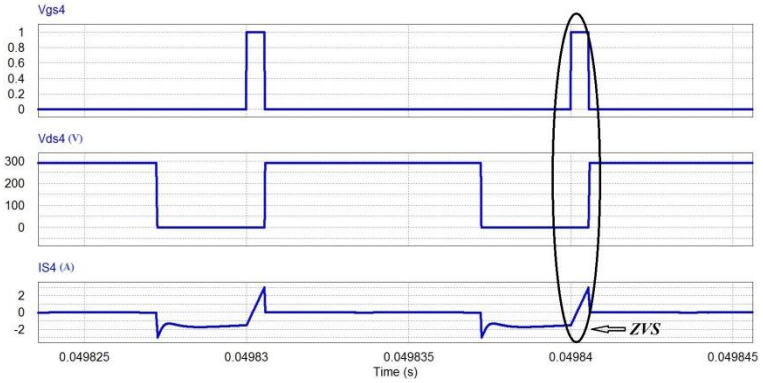

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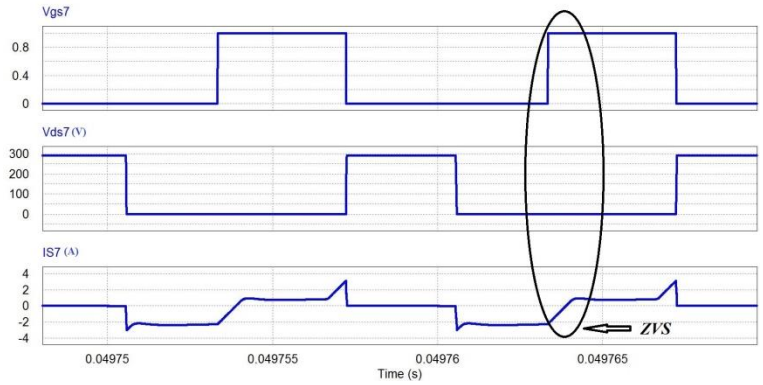

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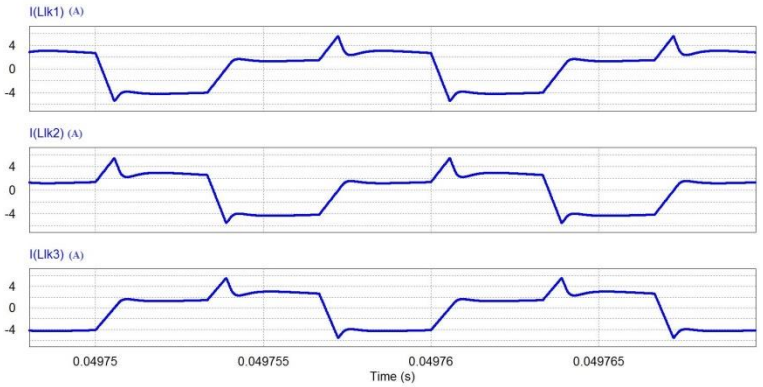

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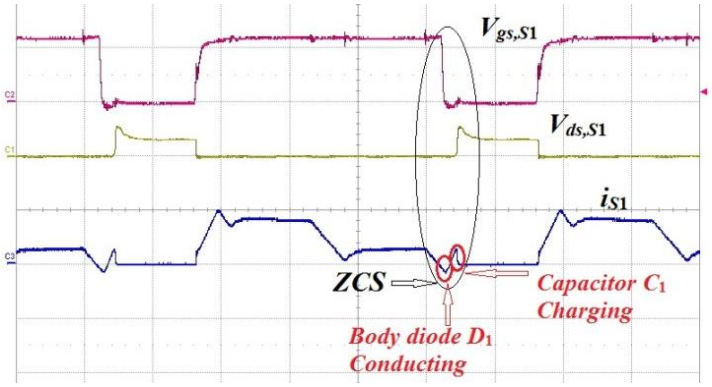
Fig. 6.10. Simulation waveforms at 375W (boost mode).



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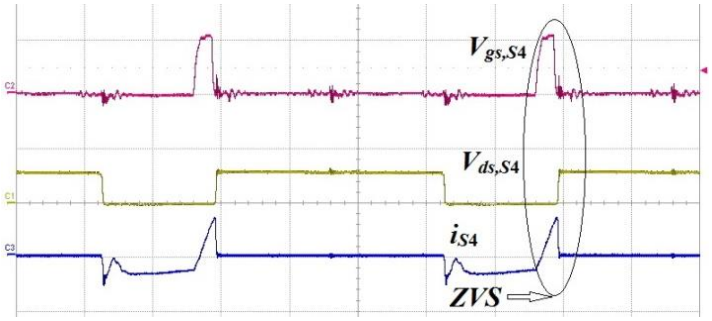

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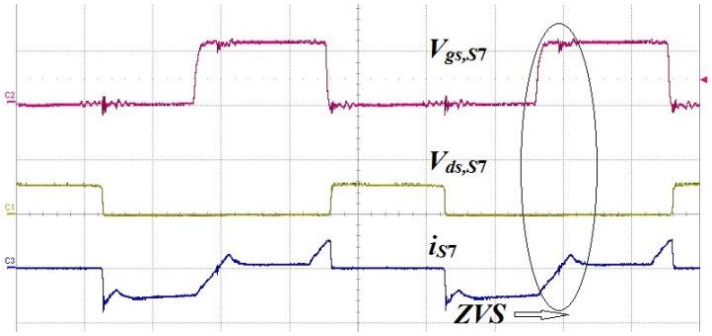

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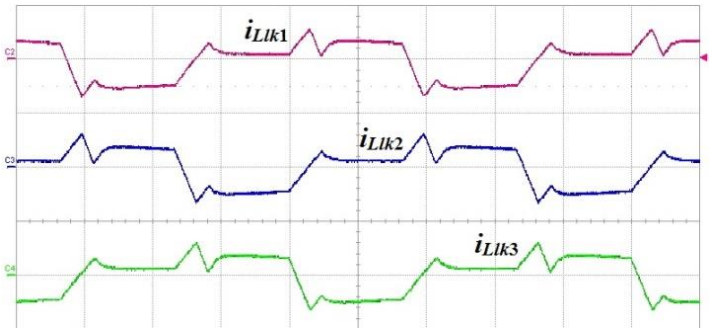

(d)

Fig. 6.11. Experimental results for output power of 375W at 300V (boost mode). (a) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (500V/div) of primary side device S_1 and current through it (10A/div). (b) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (500V/div) across secondary side device S_4 and current through it (5A/div). (c) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (500V/div) across secondary side device S_7 and current through it (5A/div). (d) Currents through series inductors i_{Llk1}, i_{Llk2}, and i_{Llk3} (10A/div).

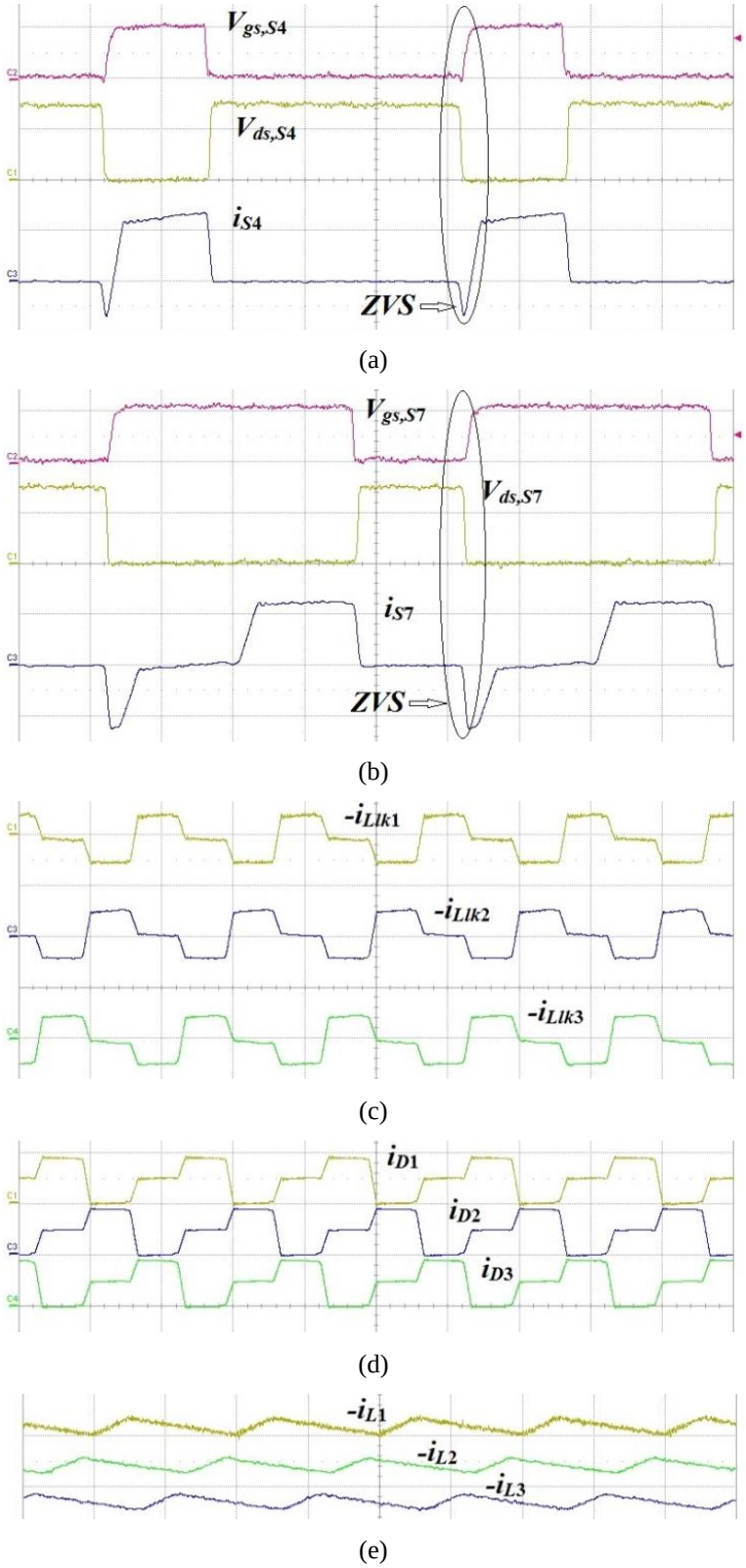

Fig. 6.12. Experimental results for output power of 450W at 300V (buck mode). (a) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (200V/div) of primary side device S_4 and current through it (2A/div). (b) Gate-to-source voltage V_{gs} (10V/div) and drain-to-source voltage V_{ds} (200V/div) across secondary side device S_7 and current through it (2A/div). (c) Negative currents through series inductors i_{Llk1}, i_{Llk2}, and i_{Llk3} (10A/div). (d) Currents through body diodes of primary switches i_{D1}, i_{D2}, and i_{D3} (10A/div). (e) Negative boost inductors currents i_{L1}, i_{L2}, and i_{L3} (2A/div).

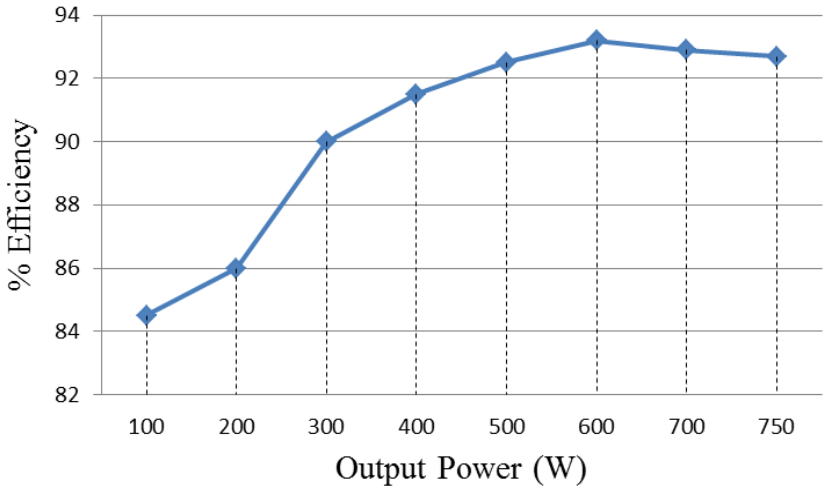

Fig. 6.13. Efficiency of the proposed three-phase ZCS converter.

ZCS of primary switches and ZVS turn-on of the secondary switches and voltage clamping are maintained even at lower loading conditions. It confirms that soft-switching and voltage clamping are inherent and load independent. As shown by Fig. 6.10 (a) and Fig. 6.11 (a), the peak current through the primary switch is higher than the following constant current to ensure ZCS of primary devices. This difference increases with the reduction of load. However, this increment in the proposed three-phase topology is lower than single phase topology in [167] adding extra merit to the three-phase design.

6.5.2 Buck Mode (Charging Mode)

The specifications of the buck mode: battery voltage V_{in} = 36 V, dc bus voltage V_o = 300 V, charging power P= 450W, device switching frequency f_s = 100 kHz. The energy is transferred from the dc bus to the battery. In the reverse direction, the converter acts as a standard voltage-fed full-bridge isolated DC/DC converter with a three-phase current tripler rectifier [174]. The experimental results are shown in Fig. 6.12. It should be observed find that ZVS of high voltage side switches has been achieved by using standard

phase-shift modulation method. The results match closely with the operating waveforms shown in Fig. 6.5. In [174], the three-phase current tripler rectifier is shown to be more efficient than full-bridge rectifier due to the reduced number of diodes that adds more advantages to the proposed converter.

Fig. 6.13 shows the mesured efficiency of proposed converter in boost mode operation. At rated output power of 750W, the measured converter loss and efficiency are 59W and 92.7%, respectively. At output power of 560W, the converter achieves the peak efficiency of 93.3% and measured loss is 40.2W. A considerable part of total loss is from the primary switches switching loss and high frequency magnetics. The percentage of this part of loss can be reduced with the increase of power level and optimized design of PCB and magnetics.

6.6 Summary and Conclusions

An innovative current-fed three-phase bidirectional DC/DC converter has been proposed, analyzed, and designed to achieve novel features of zero current commutation and natural device voltage clamping. Three-phase design permits reduced input and output filters requirements owing to ripple of 3x switching frequency. Current-sharing offers low current stress, low conduction losses, and higher efficiency. Soft-switching of all semiconductor devices, i.e., ZCS of primary and ZVS of secondary devices is achieved that reduces the switching losses significantly. Soft-switching, NVC and ZCC are inherent and load independent and is the novelty of proposed modulation. Simulation and experimental results clearly demonstrate and confirm the claimed soft-switching, ZCC, NVC of primary devices without any snubber or auxiliary

circuits. Once ZCC, NVC, and soft-switching are designed to be obtained at rated power, it is guaranteed to achieve at reduced load. For the buck mode operation, the asymmetrical duty control method has been applied to obtain wide range of soft-switching. The next Chapter presents summary of contributions of the conducted research and results delivered by this thesis. Recommendations for further work will also be discussed.

Chapter 7

Conclusions and Suggestions for Future Work

7.1 Introduction

This thesis is focused on analysis, design, and development of high-frequency soft-switching power conditioning system (PCS) for low voltage high current applications. Such applications include solar/fuel cell based utility interactive inverters, UPS, microgrid, V2G, and energy storage. Power electronics is an important component in regulating power from low voltage high current source to suitable form. Selection of power electronic converter topology is critical to realize high performance based on source profile, load profile, and electrical specifications. Current-fed converters are suitable for fuel cell applications due to low input current ripple, inherent high boost ratio, reduced circulating current, and easier current control ability. This thesis presents the analysis, design and control of soft-switching current-fed power converters for such applications. This Chapter summarizes and concludes the contribution of this thesis and recommends scope for future work. The research completed in the thesis is summarized in Section 7.2. The suggestions for future work are presented in Section 7. 3.

7.2 Conclusions

This thesis mainly focused on low voltage high current specifications. Unidirectional DC/DC PWM and resonant converters were reviewed and compared in Chapter 2. Three-phase AC-link active-clamped ZVS current-fed DC/DC converter was selected to serve as the front-end DC/DC converter interfacing the low voltage fuel cell stack and high voltage dc bus connecting to traction inverter. Achieving soft-switching over a wide variation of fuel cell voltage and power is a challenge. A new design with weakened transformer magnetizing inductance was proposed to achieve extended range soft-switching. This Chapter studied and explained steady-state operation and analysis, and delivered design including transformer magnetizing inductance effect. The proposed converter maintains ZVS of all power semiconductor devices over wide range of load (full load down to 10% load) and source voltage (22V and 41V). Current sharing resulted in reduced peak currents and conduction losses. The proposed converter combines the merits of three-phase configuration with ZCS of rectifier diodes, making it a competitive topology in the area of power supplies/converters for medium power applications requiring high voltage amplification ratio. An experimental converter prototype rated at 300W was designed, developed, and tested in the laboratory to demonstrate the converter performance over wide variations in source voltage and output power.

Traditional current-fed converters are well known for device turn-off voltage overshoot issue. A novel naturally clamped zero current commutated soft-switching bidirectional current-fed dual active bridge (CFDAB) isolated DC/DC converter has been proposed in Chapter 3. This proposed secondary

modulation technique naturally clamped the voltage across the primary side devices with zero current commutation (ZCC) eliminating the necessity for so far widely adopted active-clamp circuit or passive snubbers. Switching losses were limited significantly owing to ZCS of primary side devices and ZVS of secondary side devices. Soft-switching and voltage-clamping is inherent and load independent. The voltage across primary side devices is clamped at rather low reflected output voltage enabling the use of semiconductor devices of low voltage rating. Steady state operation, analysis, design, simulation results using PSIM 9.0.4, and experimental results were presented in this Chapter. The proposed snubberless topology is truely an isolated boost converter with 20% higher boost capacity compared to conventional active-clamped CFFB DC/DC converter.

Steady-state analysis is enough to study the converter operation, understand the electrical waveforms, design the components' values, and determine their ratings. However, small signal analysis is required to derive the small signal model and relevant transfer functions of the converter to develop a closed loop control to regulate the output voltage with possible variation in load and source voltage. A detailed small signal analysis of the proposed zero current commutated CFDAB DC/DC converter was presented in Chapter 4. Small signal model was derived by using state-space averaging technique and transfer functions were calculated. Design of closed two-loop controller was presented in detail and implemented on mixed signal processor Cypress PSoC 5. Simulation results using PSIM 9.0.4 and experimental waveforms from a 250W prototype with the designed controller were illustrated to verify the stability of the control system. Experimental results for

step change in load clearly showed satisfactory transient performance of the converter and the designed controller.

A modular multi-cell bidirectional current-fed full-bridge voltage doubler (CF-FBVD) was proposed for high power application in Chapter 5. Six configurations of CF-FBVD were proposed to match different specific application requirements. The input and output ripples were reduced considerably due to interleaving approach. A design example of PISO configuration was presented. Detailed steady state operation, analysis, and design were given. Simulation and experimental results from a 500W prototype were provided to validate the effectiveness of the converter design.

Interleaving results in reduced input and output filtering requirements, low device ratings and enhances power transfer capacity. However, it requires 2x the number of components and thus power density of the converter and the system is compromised. Therefore a three-phase converter may result into a better compromise over two interleaved cells.

A current-fed three-phase bidirectional DC/DC converter with natural clamping and zero current commutation was proposed and studied in Chapter 6. The secondary modulation technique proposed in Chapter 3 is modified and applied to the proposed three-phase circuit. Similarly, ZCS of primary side devices and ZVS of secondary side devices are also achieved. Soft-switching, ZCC and NVC are also inherent and load independent. Three-phase design permits reduced input and output filters requirements owing to ripple of 3x switching frequency. Steady state operation, analysis, and design were presented. Simulation results from PSIM 9.0.4 and experimental results from a

750W prototype built in the lab are provided in Chapter 6 to verify effectiveness of the proposed modulation technique.

7.3 Future Work

In this thesis, several current-fed soft-switching power converters for fuel cell applications have been researched and studied. Recommendations for future work have been discussed next.

1) Several generalized configurations of modular multi-cell bidirectional DC/DC converter have been proposed in Chapter 5. However, methods to determine the optimum configuration for the given input/output voltage, and power requirement should be researched.

2) As discussed in Chapter 5, the proposed multi-cell bidirectional DC/DC converter allows the integration of different energy storage sources and individual active power control. Advanced energy management control algorithms should be developed and validated to increase energy economy while maintaining high performance of the vehicle.

3) Experimentation with modules and integrated power modules (IPMs) with dedicated drivers for high power prototypes should also be tried.

4) The concept of power electronics building blocks (PEBB) discussed in Chapter 5 provides a way to hardware standardization of power electronic systems. CF-FBVD is proposed as a modular PEBB to satisfy different specific application needs. The development of advanced power electronics interfaces (APEI) including the

standardization of power electronics interfaces, control interface, communication interfaces should also be investigated to partition power electronics systems into flexible, plug-and-play building blocks.

5) The scope of developed soft-switching naturally-clamped bidirectional current-fed DC/DC converter technologies can be explored for microgrid application. In recent years, microgrid is a rapidly evolving concept that describes the concepts of managing continuous energy supply and options to consumers, and two-way power flow between users and utility. FCVs can serve as a part of distributed generation system and provide power to utility during peak demand or supply backup power for homes or businesses during power cut or grid failure. To convert DC voltage from fuel cell stack into utility AC voltage at line frequency and feeding current into utility line with low THD and high line power factor, it is necessary to integrate inverter with front-end DC/DC converter. Therefore an inverter along with grid-connected control can be explored to operate from fuel cell dc bus. CFDAB and current-fed push-pull converter based inverters for such applications (solar, micro-grid, UPS, etc.) have been explored [178-179].

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Appendices

Appendix A

Soft-switching Current-fed Push-pull Front-end Converter Based Inverter for Residential Photovoltaic Power System

A.1 Introduction

In Chapter 3, a novel secondary modulation technique is proposed to clamp the voltage across the primary side devices and therefore eliminates the necessity for active clamping circuit or passive snubbers. Switching losses are reduced significantly owing to ZCS of primary switches and ZVS of secondary switches. Soft-switching is inherent owing to proposed secondary modulation, load independent, and is maintained during wide variation of input voltage and power transfer capacity, and thus is also suitable for PV applications. In this appendix, a dual stage dc/ac inverter is proposed for the photovoltaic (PV) residential power system as shown in Fig.A.1, which is composed of a novel high step-up snubberless current-fed push-pull front-end converter and standard full-bridge inverter. Push-pull converter has only two primary devices with common ground to supply and results in simple and reduced gating requirement. Voltage doubler or half bridge is selected to reduce number of the

switches and the transformer turns ratio. With overall low number of active switches (primary and secondary), the converter is attractive for such applications.

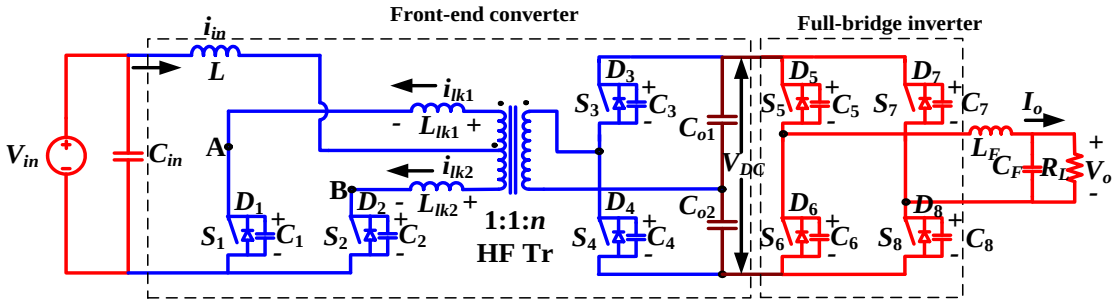


Fig. A.1. Proposed inverter with snubberless high step-up current-fed push-pull dc/dc converter.

A.2 Operation and Analysis of the Converter

In this Section, steady-state operation and analysis of proposed high step-up front-end current-fed converter have been explained. To simplify the analysis, the following assumptions are made: 1) Boost inductor L is large enough to maintain constant current through it. 2) All the components are ideal. 3) Series inductors L_{lk1} and L_{lk2} include the leakage inductances of the transformer. The total value of L_{lk1} and L_{lk2} is represented as L_{lk_T}. 4) Magnetizing inductance of the transformer is infinitely large.

The steady-state operating waveforms are shown in Fig. A.2. The primary switches S_1 and S_2 are operated with identical gating signals phase shifted with each other by 180^o with an overlap using fixed-frequency duty cycle modulation. The overlap varies with duty cycle, and the duty cycle should be kept above 50%. The steady-state operation of the converter during different intervals in a one half HF cycle is explained using the equivalent circuits shown in Fig. A.3. For the rest half cycle, the intervals are repeated in the same sequence with other symmetrical devices conducting to complete the full HF cycle.

Interval 1 (Fig. A.3a; $t_o < t < t_1$): In this interval, primary side switch S_2 and anti-parallel body diode D_3 of the secondary side switch are conducting. Power is transferred to the load through HF transformer. The non-conducting secondary device S_4 is blocking output voltage V_{DC} and the non-conducting primary device S_1 is blocking reflected output voltage V_{DC}/n. The values of current through various components are: $i_{S1} = 0$, $i_{S2} = I_{in}$, $i_{Llk1} = 0$, $i_{Llk2} = I_{in}$, $i_{D3} = I_{in}/n$. Voltage across the switch S_1: $V_{S1} = V_{DC}/n$. Voltage across the switch S_4: $V_{S4} = V_{DC}$.

Interval 2 (Fig. A.3b; $t_1 < t < t_2$): At $t = t_1$, primary switch S_1 is turned-on. The corresponding snubber capacitor C_1 discharges in a very short period of time. At the end of this interval, S_1 is fully conducting and C_1 is completely discharged.

Interval 3 (Fig. A.3c; $t_2 < t < t_3$): Now all two primary switches are conducting. Reflected output voltage appears across series inductors L_{lk1} and L_{lk2}, diverting/transferring the current through switch S_2 to S_1. It causes current through previously conducting device S_2 to reduce linearly. It also results in conduction of switch S_1 with zero current which helps reducing associated turn-on loss. The currents through various components are given by.

$$i_{Llk1} = i_{S1} = \frac{V_{DC}}{n \cdot L_{lk\_T}} \cdot (t - t_2) \tag{A-1}$$

$$i_{Llk2} = i_{S2} = I_{in} - \frac{V_{DC}}{n \cdot L_{lk\_T}} \cdot (t - t_2) \tag{A-2}$$

$$i_{D3} = \frac{I_{in}}{n} - \frac{2 \cdot V_{DC}}{n^2 \cdot L_{lk\_T}} \cdot (t - t_2) \tag{A-3}$$

Where $L_{lk\_T} = L_{lk1} + L_{lk2}$. Before the end of this interval $t = t_3$, the anti-parallel body diode D_3 is conducting. Therefore S_3 can be gated on for ZVS turn-on. At the end of

this interval, D_3 commutates naturally. Current through all primary devices reaches $I_{in}/2$. Final values are: $i_{Llk1}= i_{Llk2}=I_{in}/2$, $i_{S1}= i_{S2} =I_{in}/2$, $i_{D3} =0$.

Interval 4 (Fig. A.3d; $t_3 < t < t_4$): In this interval, secondary device S_3 is turned-on with ZVS. Currents through all the switching devices continue increasing or decreasing with the same slope as interval 3. At the end of this interval, the primary device S_2 commutates naturally with ZCC and the respective current i_{S2} reaches zero obtaining ZCS. The full current, i.e. input current is taken over by other device S_1. Final values are: $i_{Llk1}=i_{S1} =I_{in}$, $i_{Llk2}=i_{S2} =0$, $i_{S3} = I_{in}/n$.

Interval 5 (Fig. A.3e; $t_4 < t < t_5$): In this interval, the leakage inductance current i_{Llk1} increases further with the same slope and anti-parallel body diode D_2 starts conducting causing extended zero voltage to appear across commutated switch S_2 to ensure ZCS turn-off. Now, the secondary device S_3 is turned-off. At the end of this interval, current through switch S_1 reaches its peak value. This interval should be very short to limit the peak current though the transformer and switch reducing the current stress and kVA ratings. The currents through operating components are given by

$$i_{S1} = i_{Llk1} = I_{in} + \frac{V_{DC}}{n \cdot L_{lk\_T}} \cdot (t - t_4) \tag{A-4}$$

$$i_{D2} = -i_{Llk2} = \frac{V_{DC}}{n \cdot L_{lk\_T}} \cdot (t - t_4) \tag{A-5}$$

$$i_{S3} = \frac{I_{in}}{n} + \frac{2 \cdot V_{DC}}{n^2 \cdot L_{lk\_T}} \cdot (t - t_4) \tag{A-6}$$

Interval 6 (Fig. A.3f; $t_5 < t < t_6$): During this interval, secondary switch S_3 is turned-off. Anti-parallel body diode of switch S_4 takes over the current immediately. Therefore, the voltage across the transformer primary reverses polarity. The current through the switch S_1 and body diodes D_2 also start decreasing. The currents through

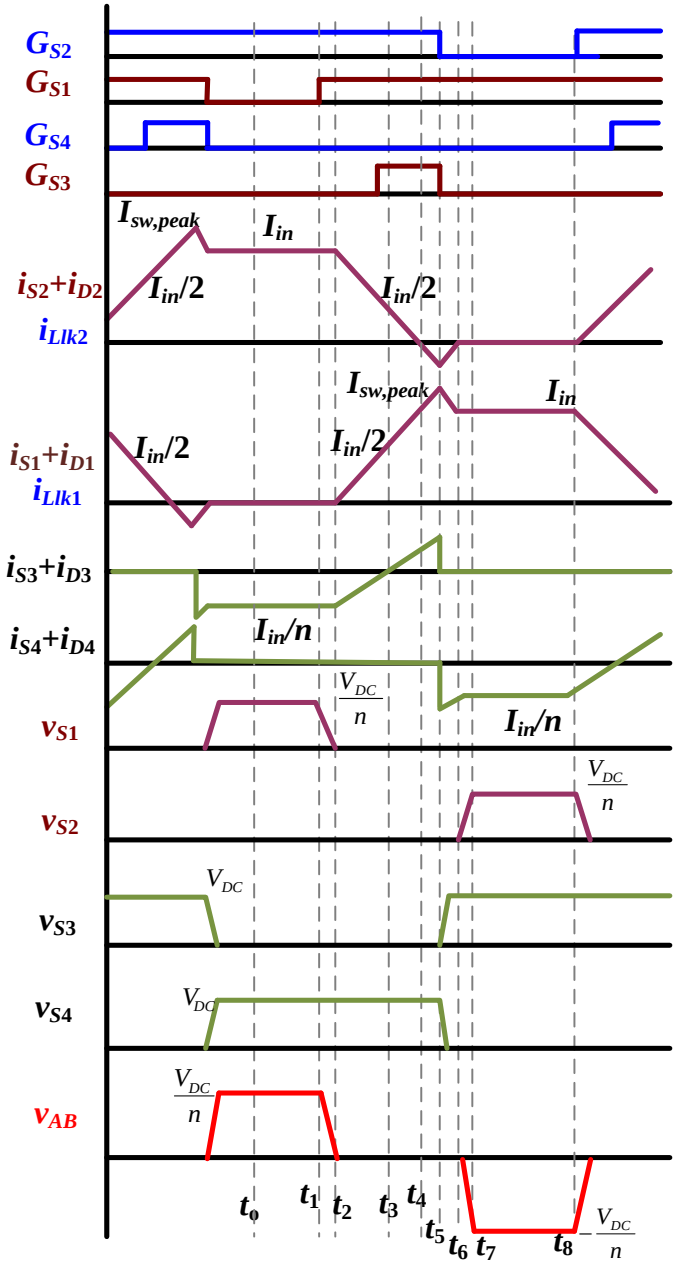
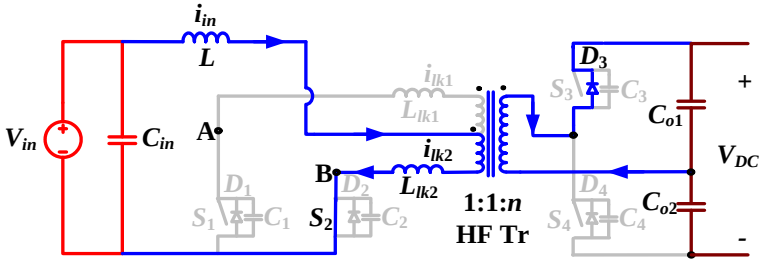
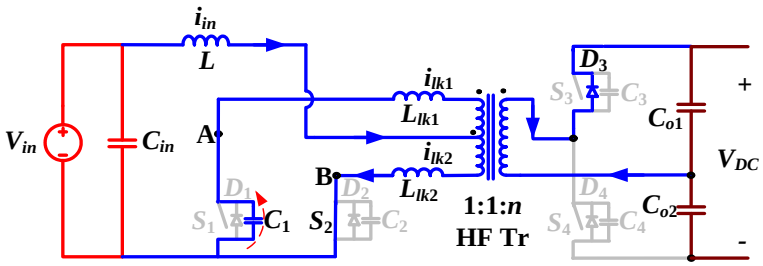


Fig. A.2. Operating waveforms of proposed high step-up ZCS current-fed push-pull isolated dc/dc converter shown in Fig. 3.



(a)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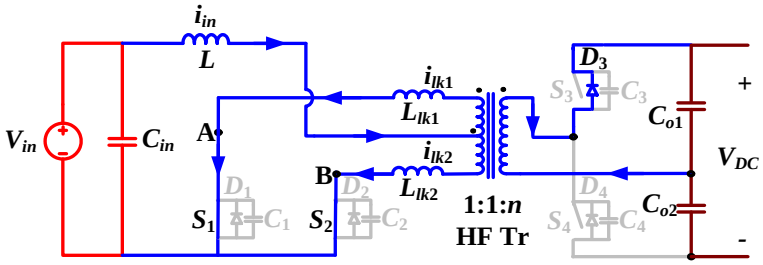
(b)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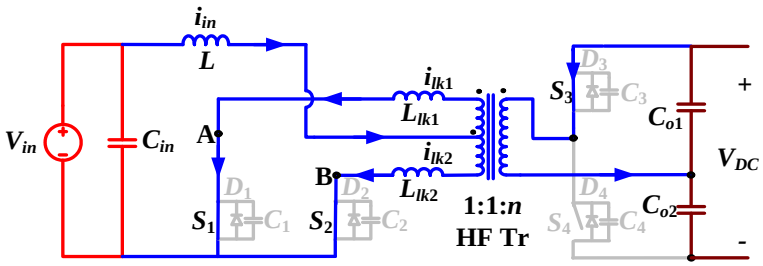
(c)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L
V_{in}
C_{in}
A
B
D_1
S_1
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D_2
C_2
i_{lk1}
L_{lk1}
i_{lk2}
L_{lk2}
1:1:n
HF Tr
D_3
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C_4
C_{o1}
C_{o2}
+
V_{DC}
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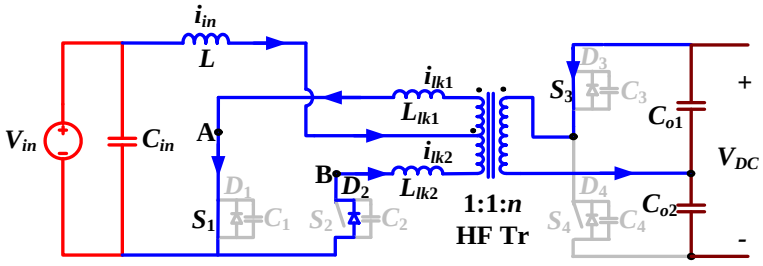
(d)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L_{lk1}
i_{lk2}
L_{lk2}
1:1:n
HF Tr
D_3
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C_{o1}
C_{o2}
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V_{DC}
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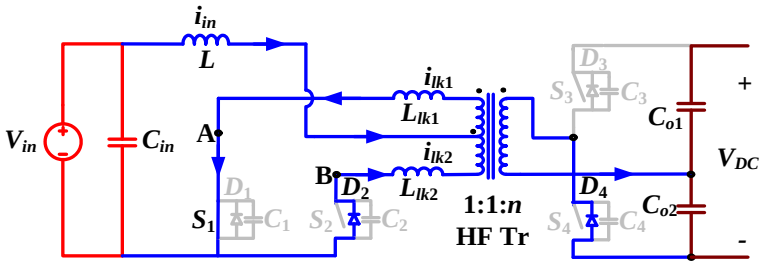
(e)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L_{lk1}
i_{lk2}
L_{lk2}
1:1:n
HF Tr
D_3
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C_3
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C_4
C_{o1}
C_{o2}
+
V_{DC}
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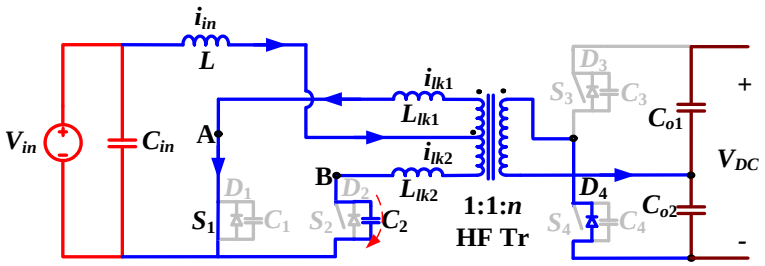
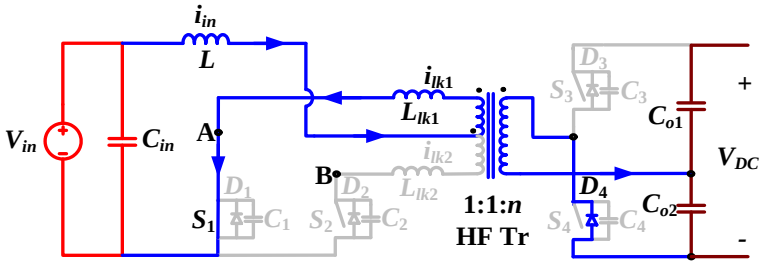
(f)



(g)



(h)

Fig. A.3. Equivalent circuits during different intervals of the operation of the proposed converter (Fig. 3) for the steady-state operating waveforms illustrated in Fig.4.

operating components are given by

$$i_{S1} = i_{Llk1} = I_{sw,peak} - \frac{V_{DC}}{n \cdot L_{lk\_T}} \cdot (t - t_5) \tag{A-7}$$

$$i_{D2} = -i_{Llk2} = I_{D2,peak} - \frac{V_{DC}}{n \cdot L_{lk\_T}} \cdot (t - t_5) \tag{A-8}$$

$$i_{D4} = \frac{I_{in}}{n} + 2 \cdot I_{D2,peak} - \frac{2 \cdot V_{DC}}{n^2 \cdot L_{lk\_T}} \cdot (t - t_5) \tag{A-9}$$

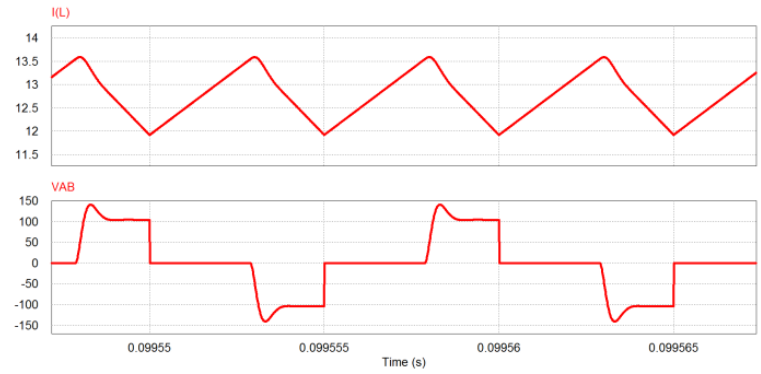
At the end of this interval, current through D_2 reduce to zero and is commutated naturally. Current through S_1 reaches I_{in}. Final values: $i_{Llk1} = i_{S1} = I_{in}$, $i_{Llk2} = i_{D2} = 0$, $i_{D4} = I_{in}/n$.

Interval 7 (Fig. A.3g; $t_6 < t < t_7$): In this interval, snubber capacitor C_2 charges to V_{DC}/n in a short period of time. Switch S_2 is in forward blocking mode now.

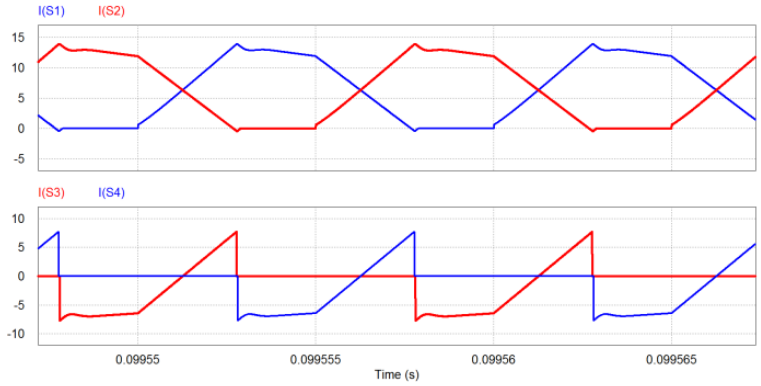
Interval 8 (Fig. A.3h; $t_7 < t < t_8$): In this interval, currents through S_1 and transformer are constant at input current I_{in}. Current through anti-parallel body diode of the secondary switch D_4 is at I_{in}/n. The final values are: $i_{Llk1} = i_{S1} = I_{in}$, $i_{Llk2} = i_{S2} = 0$,

$i_{D4} = I_{in}/n$. Voltage across the switch S_2 $V_{S2} = V_{DC}/n$. In this half HF cycle, current has transferred from switch S_2 to S_1, and the transformer current has reversed its polarity.

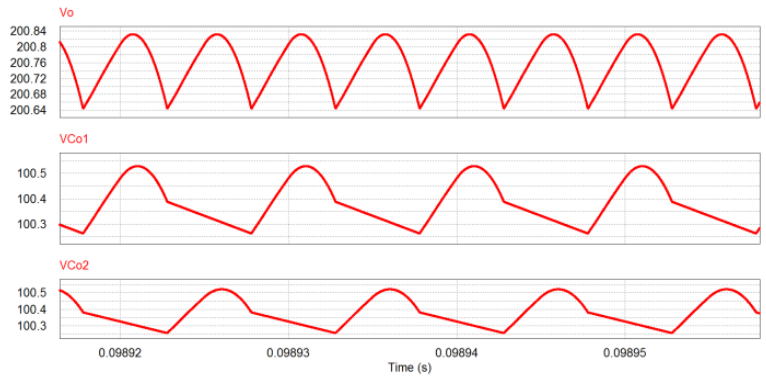
A.3 Simulation and Experimental Results



(a)

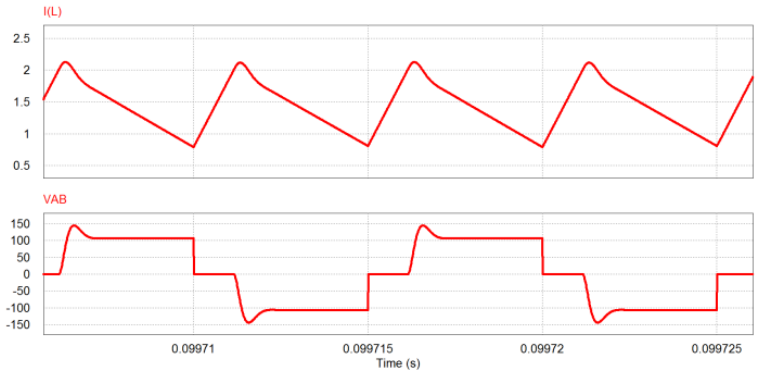


(b)

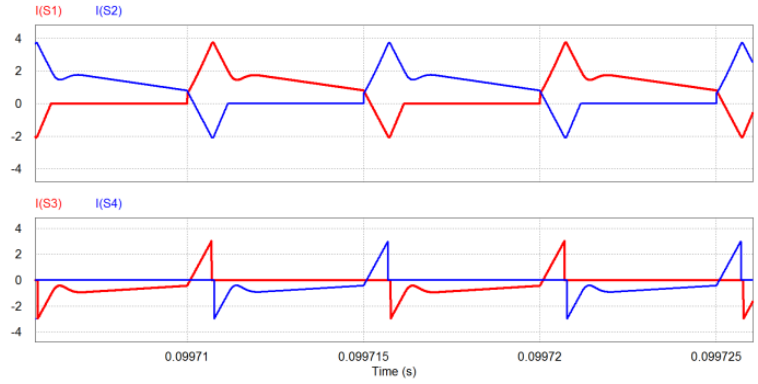


(c)

Fig. A.4. Simulation results at V_{in} = 22 V and peak power. (a) Current through input inductor i_L and voltage V_{AB}. (b) Primary switches currents i_{S1} and i_{S2} and secondary switches currents i_{S3} and i_{S4}. (c) Output voltage V_O and Voltages across output capacitors V_{Co1} and V_{Co2}.



(a)



(b)

Fig. A.5. Simulation results at V_{in} = 41 V and 20% power. (a) Current through input inductor i_L and voltage V_{AB}. (c) Primary switches currents i_{S1} and i_{S2} and secondary switches currents i_{S3} and i_{S4}.

The designed converter rated at 250W was first simulated using PSIM 9.0.4 and then built in the laboratory to verify the analysis, design and performance of the converter. Simulation results for two input voltage and load conditions of V_{in} = 22 V at full load and V_{in} = 41 V at 20% load are presented in Fig. A.4 and Fig. A.5, respectively, which coincides closely with theoretical operating waveforms in Fig. A.4. Fig. A.4 shows simulation results for an input voltage of 22V delivering 250W to the load. The ripple frequency of input boost inductor current is 2x device switching frequency, as shown by Fig. A.4 (a). The ripple magnitude is considerable low. Since MPP of PV modules is sensitive to current ripple, low ripple current will increase the utilization of PV modules. Fig. A.4 (c) clearly shows voltages across output capacitors (Co_1 and Co_2). They are phase shifted with each other by 180˚.

Cancellation effect results in much lower output ripple which alleviate output filter requirement.

As shown by the primary and secondary currents waveforms in (b) of Fig. A.4, ZCS of primary switches is achieved, where current goes to zero naturally and anti-parallel body diode starts conducting before gate signal is removed. The voltage across the switches is naturally clamped (Fig. A.4 (a)) avoiding the need of active clamping or passive snubber circuits. It is clear from Fig. A.4 (b) that the body diodes of the secondary switches S_3 and S_4 conduct before the devices start conducting, which verifies ZVS turn-on of the switches. Similarly, simulation waveforms for V_{in} = 41V and 20% load are presented in Fig. A.5. ZCS of primary switches and ZVS turn-on of the secondary switches are maintained even at lower loading conditions.

Table A.1 Major components' parameters of experimental prototype.

Components	Parameters
Primary switches $S1 \sim S2$	IRFB4127PBF 200V, 76A. $R_{ds,on}$ = 17mΩ
Secondary switches $S3 \sim S4$	IPA60R125CP 650V, 25A. $R_{ds,on}$ = 0.125Ω
Inverter switches $S5 \sim S8$	FGP5N60LS, 600V, 5A IGBT; IDD05SG60C, 600V, 5A SiC Schottky diode in parallel
HF transformers	3C95ETD49 ferrite core Primary turns N_1= N_2=26 Secondary turns N_3=48 Leakage inductance 1.8 µH and 1.9 µH
External series inductors L_{lk1} and L_{lk2}	TDK RM14 PC40Z L_{lk1}=11 µH and L_{lk2}=10.8 µH
Input boost inductor L	3C95ETD49 ferrite core turns N = 15 L=31 µH
Input capacitors C_{in}	4.7 mF, 50V electrolytic 2.2 µF high-frequency film capacitor
Output capacitors $C_{o1} \sim C_{o2}$	220uF, 400V electrolytic capacitor
Filter inductor	T300-40 MPP Powder core Number of turns N=285, L_F=5.5mH
Filter capacitor	0.47 µF, 1000V High frequency film capacitor

Experimental prototype of the PV inverter is built for the same specifications. The major components' parameters of the experimental prototype are given in Table A.1. Gate signals are generated using Xilinx Spartan-6 FPGA design platform. Variable resistors (rheostats) are used as load for testing. PV module exhibits highly nonlinear voltage-current characteristics and its MPP varies dramatically with solar irradiance and ambient temperature. For a typical PV module, the MPP voltage ranges from 20V to 45V at a power range of 100W to 300W. The power generation has high variability which can drop more than 80% due to passing clouds. PV inverter must maintain high performance over wide variations in input voltage and output power in order to achieve high efficiency of conversion.

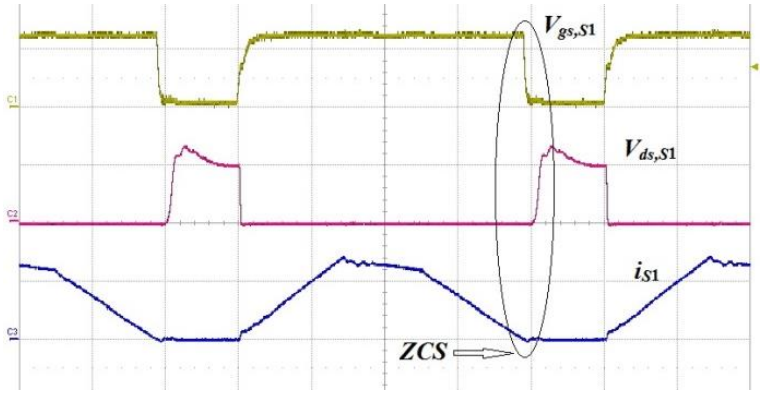
The experimental prototype has been tested under various input voltage and power conditions as shown in Figs. A.6-A.10. For V_{in} = 22V, results for peak power (load resistance of 48.4Ω), 50% power (96.8Ω) and 20% power (242Ω) are shown in Figs. A.6-A.8 respectively. Fig. A.9 and Fig. A.10 show results for V_{in} = 41V, peak power and 20% power conditions. The experimental results match closely with theoretical predicted waveforms and simulation waveforms, which obviously show that ZCS of primary switches and ZVS of secondary switches are achieved under various electrical conditions. Parts (a) of Figs. A.6-A.10 show gate-to-source V_{gs} and drain-to-source V_{ds} voltage waveforms across the primary devices, and the device current waveform. Current through the switch naturally goes to zero before the gate signal is removed. There is a clear gap between waveforms of V_{gs} and V_{ds}, which is caused by the conduction of the anti-parallel body diode of respective switch. This clearly confirms the ZCS of primary devices.

The gate-to-source V_{gs} and drain-to-source V_{ds} voltage waveforms across the secondary device and the secondary side device current waveforms are shown in parts

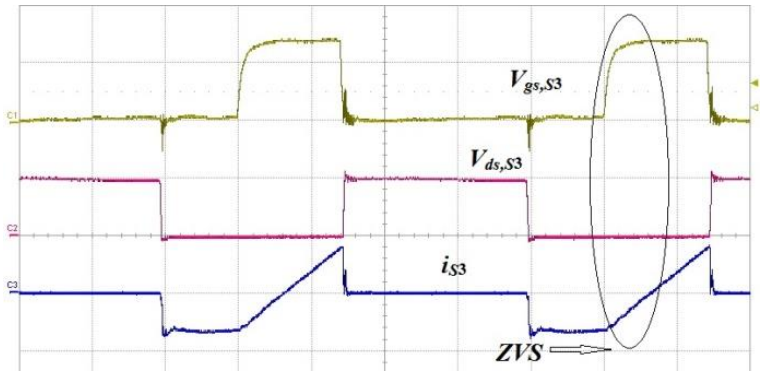
(b) of Figs. A.6-A.10. In the waveform, negative current corresponds to the conduction of anti-parallel body diode causing voltage across the switch $V_{ds} = 0$. Then the gate signal V_{gs} is applied when voltage across the device has already reached zero. Thereafter, switch starts conducting, i.e. positive value of current in the waveform (switch takes over the current with continuous zero voltage across it) resulting in zero voltage switching turn on. Voltage across the primary winding of the HF transformer V_{AB} is illustrated in parts (c) of Figs. A.6-A.10. The high-frequency bipolar voltage waveform clearly states the clamped devices' voltage due to natural or zero current commutation i.e. turn off. It can be also clearly observed that input boost currents ripple is 2x the switching frequency of device switching frequency, which brings a reduction of size of the input filter. As shown by Fig. A.11 (a), voltages across output capacitors C_{o1}, C_{o2} are phase shifted with each other by 180˚. The output voltage ripple is reduced due to ripple cancellation effect. Output voltage V_o and output current I_o at the inverter are shown in Fig. A.11. Part (b) gives the experimental result for peak load when 48.4Ω load is connected at the output of the inverter. Reduction in harmonics in output voltage (THD of less than 1%) due to LC filter is adequate to supply domestic loads. Experimental result for 50% load is presented in part (c) of Fig. A.11. Voltage between the midpoints of the inverter V_{inv} is also presented showing switching between zero and V_{DC}.

Fig. A.12 shows measured efficiency for different load conditions at V_{in} = 22 V and V_{in} = 41 V for the proposed front-end converter. The peak experimental efficiency of the proposed front-end dc/dc converter is obtained as 92.7% for V_{in} = 22 V and 94.8% for V_{in} = 41 V. The full-bridge inverter is nearly 97% due to low value of current. The efficiency of the overall inverter system is obtained as 87% to 90% for V_{in} = 22 V and 89.9% to 91.9%. Loss distribution estimation of proposed front-end converter at full

load condition with V_{in} = 22 V and V_{in} = 41 V is shown in Table A.2 and Fig. A.13. It is easy to find that with the increase of input voltage, the conduction loss of swatches and the copper loss of boost inductor and HF transformer reduce a lot. Thus the efficiency of V_{in} = 41 V is much higher than that of V_{in} = 22 V.



(a)



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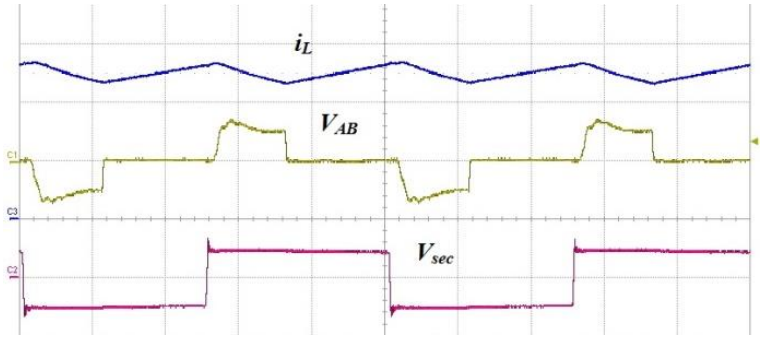
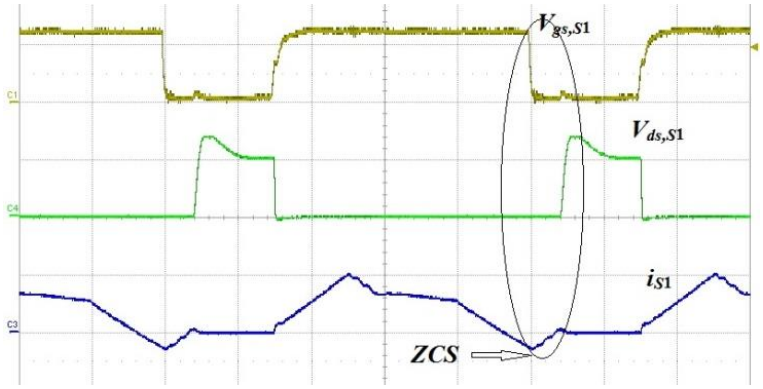
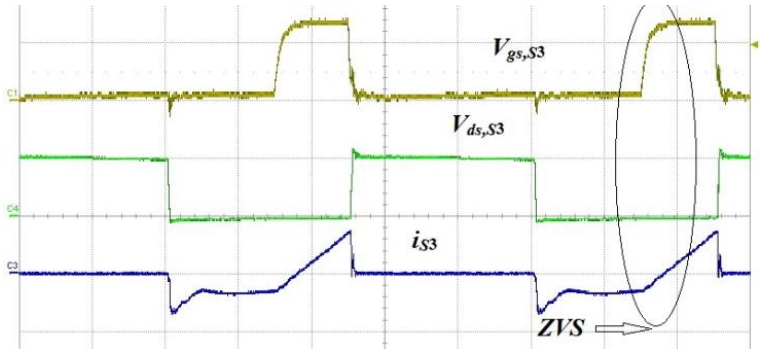


(c)

Fig. A.6. Experimental waveforms at V_{in} = 22 V and peak power (2 μs/div). (a) Primary switch voltages $v_{gs.S1}$ (10 V/div), $v_{ds.S1}$ (100V/div), and current i_{S1} (10 A/div). (b) Secondary switch voltages $v_{gs.S3}$ (10 V/div), $v_{ds.S3}$ (200 V/div), and current i_{S3} (10 A/div). (c) Input boost inductor current i_L (5 A/div), voltage v_{AB} (200 V/div), voltage across secondary of transformer v_{sec} (200 V/div).



(a)



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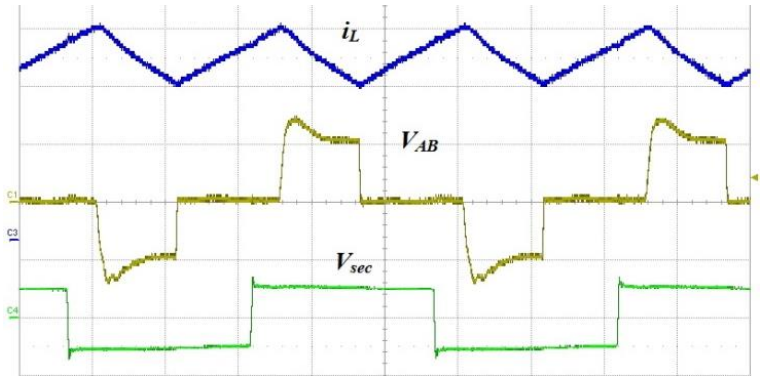
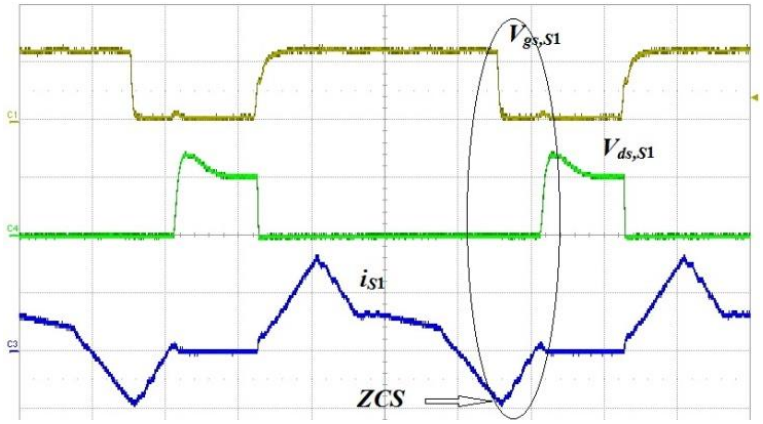
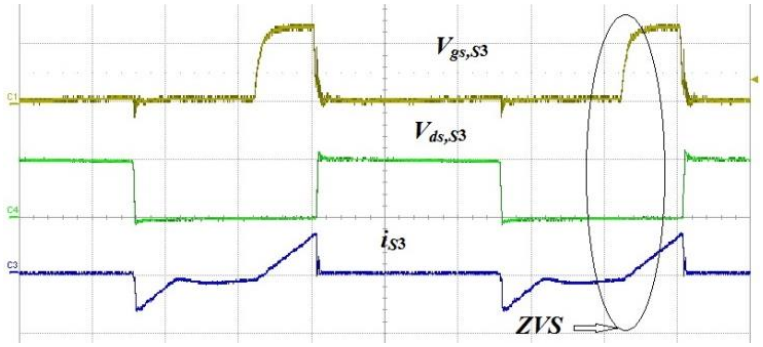


(c)

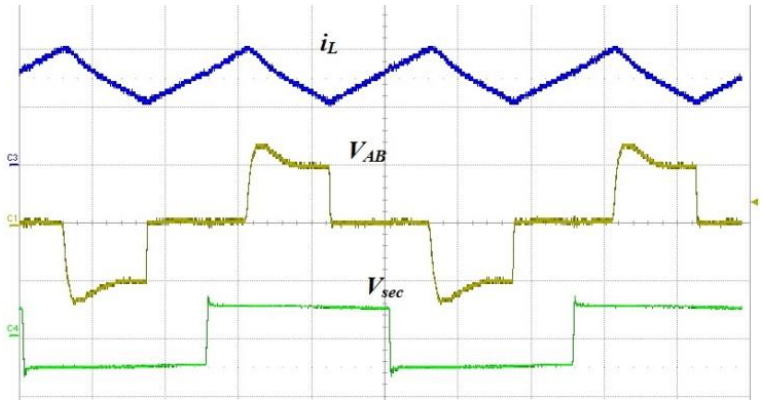
Fig. A.7. Experimental waveforms at V_{in} = 22 V and 50% power (2 µs/div). (a) Primary switch voltages $v_{gs,S1}$ (10 V/div), $v_{ds,S1}$ (100 V/div), and current i_{S1} (10 A/div). (b) Secondary switch voltages $v_{gs,S3}$ (10 V/div), $v_{ds,S3}$ (200 V/div), and current i_{S3} (10 A/div). (c) Input boost inductor current i_L (2 A/div), voltage v_{AB} (100 V/div), voltage across secondary of transformer v_{sec} (200 V/div).



(a)



(b)



(c)

Fig. A.8. Experimental waveforms at V_{in} = 22 V and 20% power (2 µs/div). (a) Primary switch voltages $v_{gs,S1}$ (10 V/div), $v_{ds,S1}$ (100 V/div), and current i_{S1} (5 A/div). (b) Secondary switch voltages $v_{gs,S3}$ (10 V/div), $v_{ds,S3}$ (200 V/div), and current i_{S3} (10 A/div). (c) Input boost inductor current i_L (2 A/div), voltage v_{AB} (100 V/div), voltage across secondary of transformer v_{sec} (200 V/div).

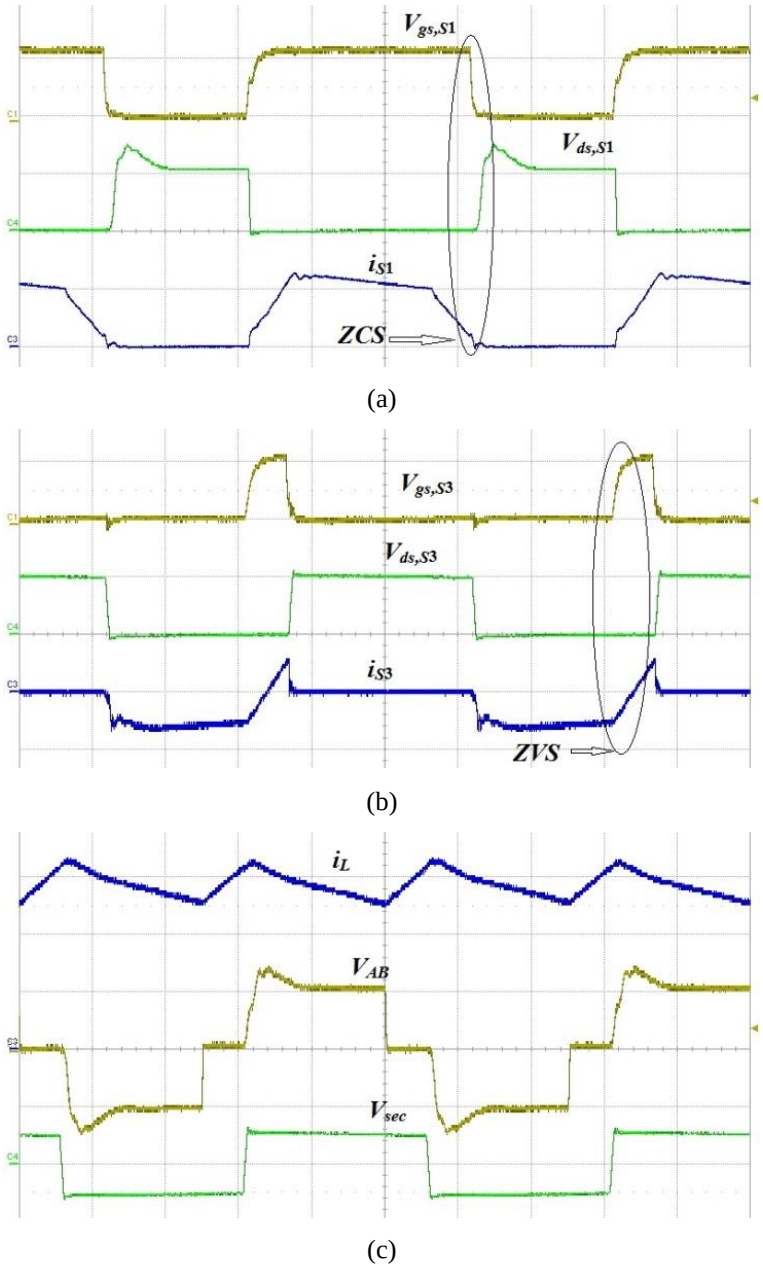


Fig. A.9. Experimental waveforms at V_{in} = 41 V and peak power (2 µs/div). (a) Primary switch voltages $v_{gs,S1}$ (10 V/div), $v_{ds,S1}$ (100 V/div), and current i_{S1} (5 A/div). (b) Secondary switch voltages $v_{gs,S3}$ (10 V/div), $v_{ds,S3}$ (200 V/div), and current i_{S3} (5 A/div). (c) Input boost inductor current i_L (2 A/div), voltage v_{AB} (100 V/div), voltage across secondary of transformer v_{sec} (200 V/div).

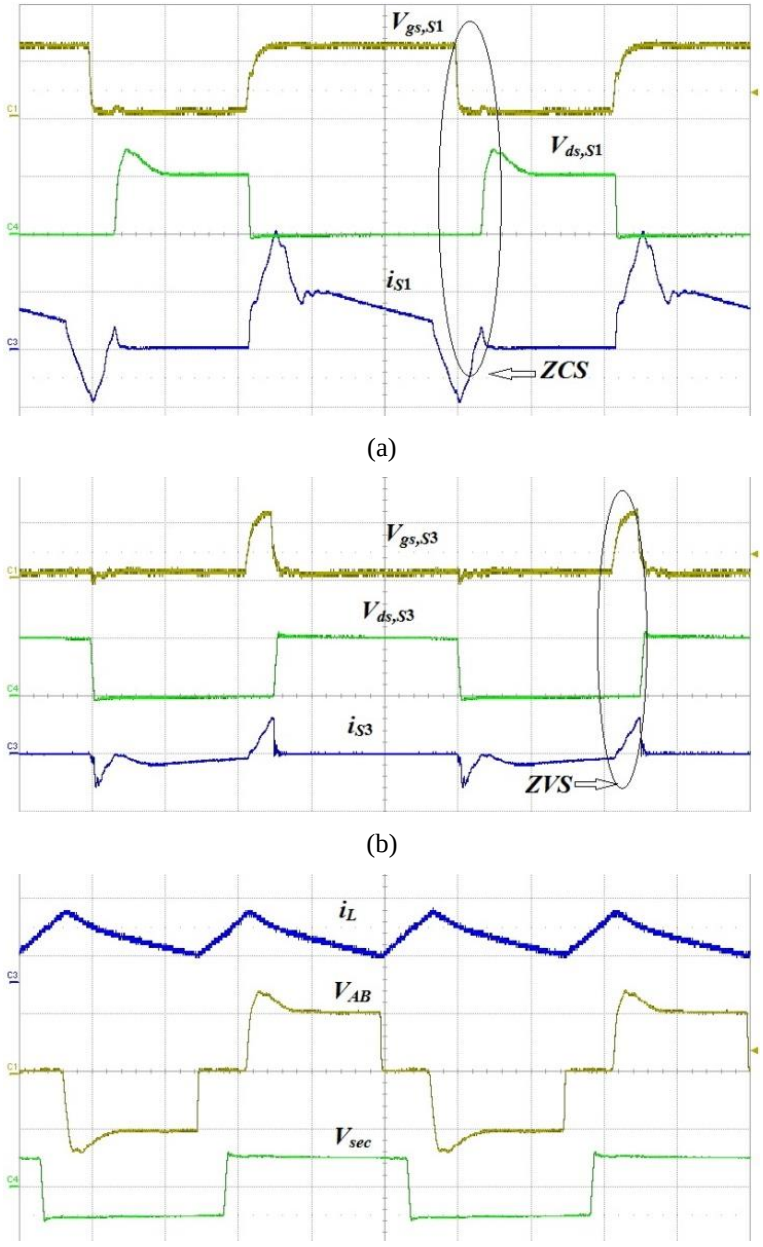


Fig. A.10. Experimental waveforms at V_{in} = 41 V and 20% power (2 µs/div). (a) Primary switch voltages $v_{gs,S1}$ (10 V/div), $v_{ds,S1}$ (100 V/div), and current i_{S1} (2 A/div). (b) Secondary switch voltages $v_{gs,S3}$ (10 V/div), $v_{ds,S3}$ (200 V/div), and current i_{S3} (5 A/div). (c) Input boost inductor current i_L (2 A/div), voltage v_{AB} (100 V/div), voltage across secondary of transformer v_{sec} (200 V/div).

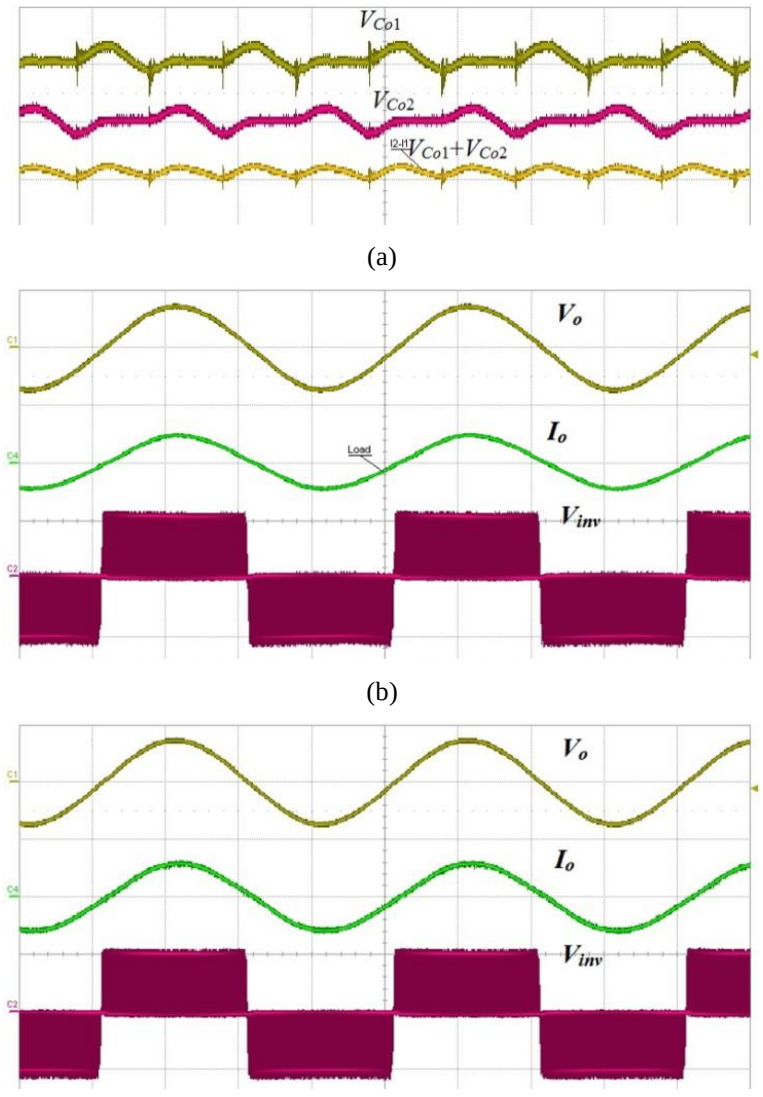


Fig. A.11. Experimental waveforms at V_{DC} = 200 V (5ms/div): (a) Scaled voltages across capacitors C_{o1} and C_{o2} (10V/div, 5 µs/div). (b) Output voltage V_o (200V/div), output current I_o (5A/div), and inverter output voltage V_{inv} (200V/div) at peak power (250W). (c) Output voltage V_o (200V/div), output current I_o (2A/div), and inverter output voltage V_{inv} (200V/div) at 50% power (125W).

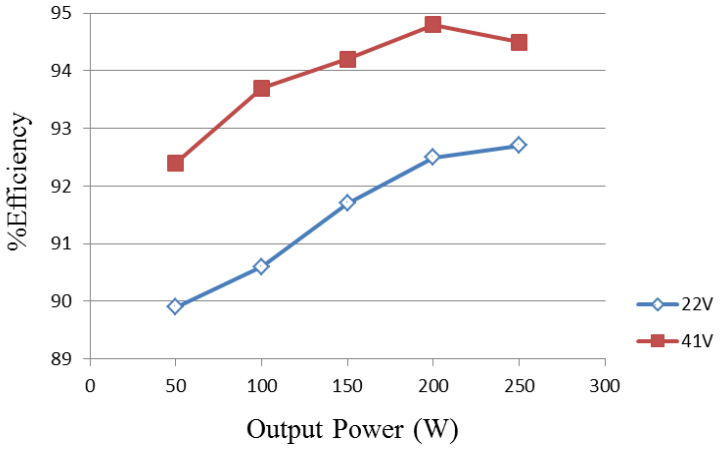


Fig. A.12. Plot of efficiency versus output power for different load conditions of proposed front-end converter with V_{in} = 22 V and V_{in} = 41 V.

Table A.2. Loss distribution estimation of the experimental front-end converter at full load condition with V_{in}=22V and V_{in}=41V

Loss type	Power loss (W) at V_{in}=22V	Power loss (W) at V_{in}=41V
Primary switches conduction loss	2.3	0.89
Primary switches switching loss	3.6	3.6
Secondary switches conduction loss	3.67	1.59
Secondary switches switching loss	0.05	0.05
Boost inductor loss	2.2	1.61
HF transformer loss	3.4	2.25
Series inductors loss	1.5	1.15
others	3	3.3
Total loss	19.7	14.5

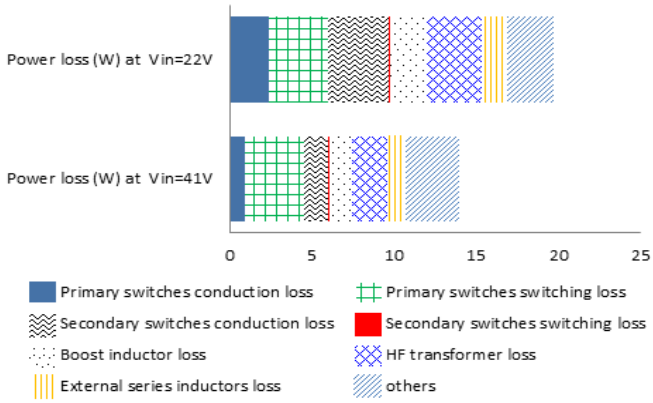


Fig. A.13. Estimated loss breakdown of the experimental front-end converter at full load condition with V_{in} = 22 V and V_{in} = 41 V.

Appendix B

In this Section, the derivation procedures of selected equations are given to help the readers understand the design of the converters.

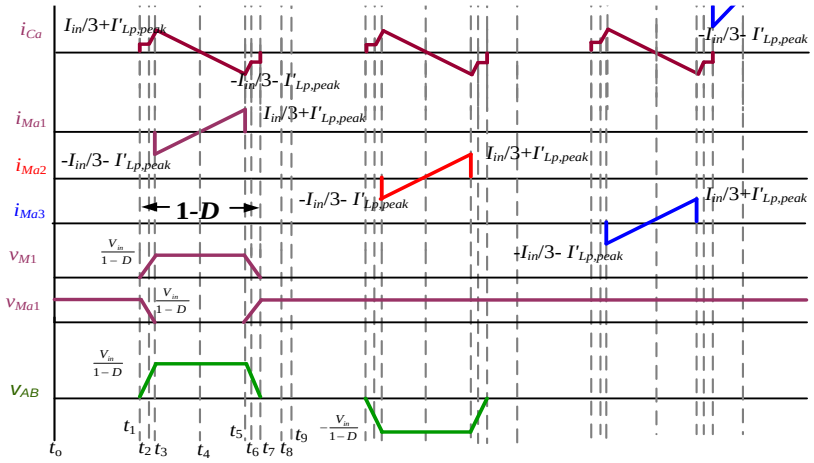


Fig. B.1 Operating waveforms of the proposed extended range soft-switching three-phase current-fed DC/DC converter.

RMS current through the auxiliary switches is given by (Equation 2-58):

$$I_{auxsw,rms} = \sqrt{\frac{\left(-\frac{I_{in}}{3}-I'_{Lp,peak}\right)^2+\left(\frac{I_{in}}{3}+I'_{Lp,peak}\right)^2+\left(-\frac{I_{in}}{3}-I'_{Lp,peak}\right)\left(\frac{I_{in}}{3}+I'_{Lp,peak}\right)}{3}\cdot(1-D)}$$
$$=\left(I_{in}+3I'_{Lp,peak}\right)\cdot\left[(1-D)/27\right]^{1/2}$$
(B-1)

The value of auxiliary capacitor C_a is (equation 2-59):

$$C_a = \frac{I_{Ca,peak}\cdot\frac{(1-D)}{2}\cdot T_s}{\Delta V_{Ca}} = \frac{I_{Ca,peak}\cdot(1-D)\cdot f_s}{2\cdot\Delta V_{Ca}\cdot f_s} \qquad \text{(B-2)}$$

RMS current through auxiliary capacitor is (equation 2-60):

$$I_{Ca,rms} = \sqrt{\frac{\left(I_{Ca,peak}\right)^2+\left(-I_{Ca,peak}\right)^2+\left(I_{Ca,peak}\right)\cdot\left(-I_{Ca,peak}\right)}{3}\cdot(1-D)\cdot 3} = I_{Ca,peak}\cdot\sqrt{(1-D)}$$
(B-3)

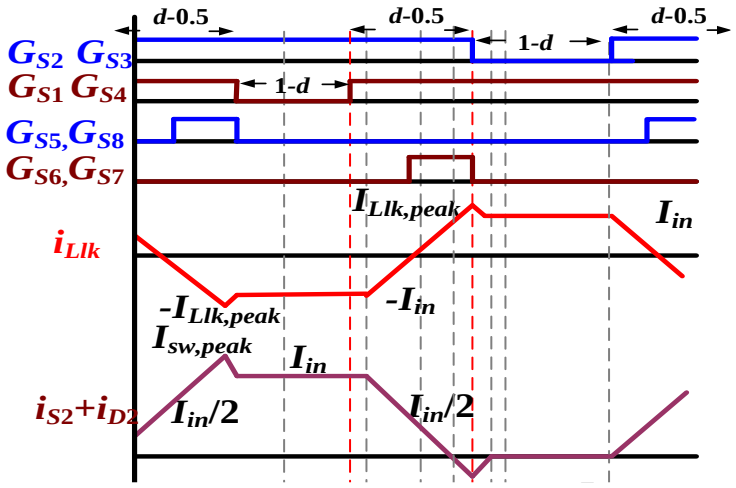


Fig. B.2. Operating waveforms of the proposed ZCS CFDAB DC/DC converter.

The equation are designed based on full-load condition, $I_{Llk,peak}$= I_{in}, for the period illustrated by the Fig. B.2 , the voltage across the leakage inductor is V_o/n, and the current variation through the leakage inductor is 2 I_{in}, therefore leakage inductance of the transformer or series inductance L_{lk} is calculated by (equation 3-15):

$$\frac{V_o}{n} = L_{lk}\frac{2\cdot I_{in}}{(d-0.5)\cdot T_s} \tag{B-4}$$

$$L_{lk} = \frac{V_o\cdot(d-0.5)}{2\cdot n\cdot I_{in}\cdot f_s} \tag{B-5}$$

RMS current through the primary switches is given by (equation 3-16):

$$I_{P,rms} = \sqrt{\frac{(I_{in})^2}{3}\cdot(d-0.5)+\frac{(I_{in})^2+(I_{in})^2+(I_{in})^2}{3}\cdot(1-d)+\frac{(I_{in})^2}{3}\cdot(d-0.5)} = I_{in}\sqrt{\frac{2-d}{3}} \tag{B-6}$$

RMS current through the transformer primary is given by (equation 3-17):

$$I_{Llk,rms} = \sqrt{\frac{(I_{in})^2+(-I_{in})^2+(I_{in})\cdot(-I_{in})}{3}\cdot(d-0.5)\cdot 2+\frac{(I_{in})^2+(I_{in})^2+(I_{in})^2}{3}\cdot(1-d)\cdot 2} = I_{in}\sqrt{\frac{5-4d}{3}} \tag{B-7}$$

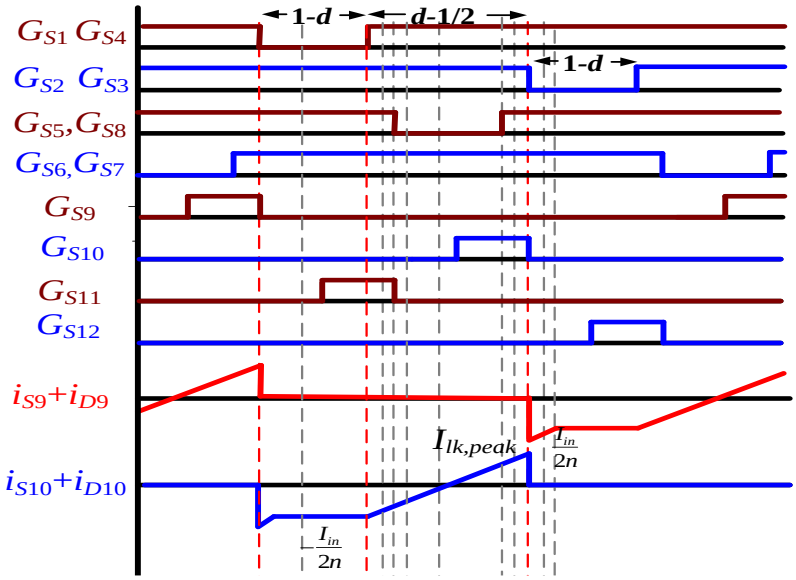


Fig. B.3. Operating waveforms of proposed interleaved ZCS current-fed CF-FBVD.

Average current and RMS current through the body diodes of secondary devices is given by (equations 5-24 and 5-25):

$$\bar{i}_D = \frac{I_{in}}{2n}\cdot(1-d) + \frac{I_{in}}{2n}\cdot\frac{1}{2}\cdot\frac{d-\frac{1}{2}}{2} = \frac{I_{in}\cdot(7-6d)}{16n} \qquad \text{(B-8)}$$

$$I_{D,rms} = \sqrt{\frac{\left(\frac{I_{in}}{2n}\right)^2 + \left(\frac{I_{in}}{2n}\right)^2 + \left(\frac{I_{in}}{2n}\right)\cdot\left(\frac{I_{in}}{2n}\right)}{3}\cdot(1-d) + \frac{\left(\frac{I_{in}}{2n}\right)^2 + 0 + 0}{3}\cdot\frac{d-\frac{1}{2}}{2}} = \frac{I_{in}}{4n}\sqrt{\frac{11\text{-}10d}{3}} \qquad \text{(B-9)}$$

RMS current through the secondary side switches is given by (equation 5-26)

$$I_{S,rms} = \sqrt{\frac{\left(\frac{I_{in}}{2n}\right)^2 + 0 + 0}{3}\cdot\frac{d-\frac{1}{2}}{2}} = \frac{I_{in}}{4n}\sqrt{\frac{2d-1}{3}} \qquad \text{(B-10)}$$

VA rating of each HF transformer is given by (equation 5-27):

RMS current through the primary winding of each HF transformer is given by the following equation

$$I_{Llk,rms} = \sqrt{\frac{\left(\frac{I_{in}}{2}\right)^2 + \left(\frac{I_{in}}{2}\right)^2 + \left(\frac{I_{in}}{2}\right)\cdot\left(\frac{I_{in}}{2}\right)}{3}\cdot(1-d)\cdot 2 + \frac{\left(-\frac{I_{in}}{2}\right)^2 + \left(\frac{I_{in}}{2}\right)^2 + \left(-\frac{I_{in}}{2}\right)\cdot\left(\frac{I_{in}}{2}\right)}{3}\cdot\left(d-\frac{1}{2}\right)\cdot 2} \quad \text{(B-}$$

$$= \frac{I_{in}}{2}\sqrt{\frac{5-4d}{3}}$$

11)

RMS voltage across the primary side of each HF transformer

$$V_{AB,rms} = \sqrt{\frac{\left(-\frac{V_o}{4n}\right)^2 + \left(-\frac{V_o}{4n}\right)^2 + \left(-\frac{V_o}{4n}\right)\cdot\left(-\frac{V_o}{4n}\right)}{3}\cdot(1-d) + \frac{\left(\frac{V_o}{4n}\right)^2 + \left(\frac{V_o}{4n}\right)^2 + \left(\frac{V_o}{4n}\right)\cdot\left(\frac{V_o}{4n}\right)}{3}\cdot(1-d)} \quad \text{(B-}$$

$$= \frac{V_o}{4n}\sqrt{\frac{2\cdot(1-d)}{3}}$$

12)

$$VA_{x-mer} = V_{AB,rms}\cdot I_{Llk,rms} = \frac{V_o\cdot I_{in}}{8n}\sqrt{\frac{2\cdot(5-4d)\cdot(1-d)}{3}} \quad \text{(B-13)}$$

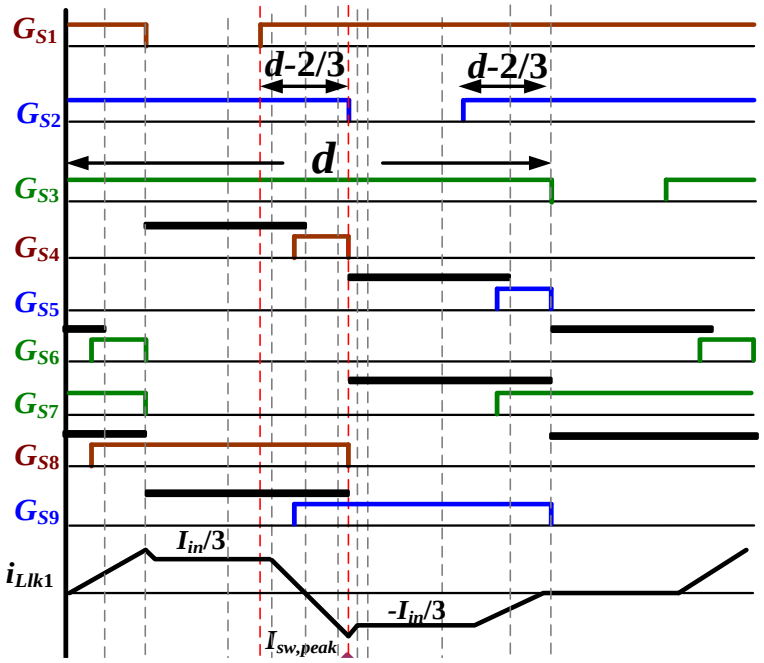


Fig. B.4. Operating waveforms of proposed ZCS current-fed three-phase converter

For the period illustrated by the Fig. B.4 , the voltage across the leakage inductor is $2V_o/3n$, and the current variation through the leakage inductor is 2 $I_{in}/3$, therefore Leakage inductance of the transformer or series inductance L_{lk} is calculated by the following equation (equation 6-21)

$$\frac{2V_o}{3n} = L_{lk}\frac{2\cdot\frac{I_{in}}{3}}{(d-\frac{2}{3})\cdot T_s} \quad \text{(B-14)}$$

$$L_{lk} = \frac{V_o\cdot(d-\frac{2}{3})}{n\cdot I_{in}\cdot f_s} \quad \text{(B-15)}$$

When one of the main switch is conducting (eg. S_1), the current flowing through the corresponding boost inductor(eg. L_1) is increasing. The voltage across the boost inductor is V_{in}, ΔI_{in} is the boost inductor ripple current, therefore (equation 6-23)

$$V_{in} = L\frac{\Delta I_{in}}{d\cdot T_s} \quad \text{(B-16)}$$

$$L = \frac{V_{in}\cdot d}{\Delta I_{in}\cdot f_s} \quad \text{(B-17)}$$

Appendix C

Converter loss modeling can be derived considering various losses in components of the converter and calculating them individually.

The conduction loss of boost inductor is given by

$$P_{L,Con} = r_L \cdot I^2_{L,rms} = r_L \cdot I^2_{in} \tag{C-1}$$

where r_L is ohmic resistance of boost inductor. It is associated with the quality (Q-factor) of the inductor.

The conduction loss of primary and secondary side switches are given by

$$P_{P,Con} = r_{P,on} \cdot I^2_{P,rms} = \frac{r_{P,on} \cdot I^2_{in} \cdot (2-d)}{3} \tag{C-2}$$

$$P_{S,Con} = r_{S,on} \cdot I^2_{S,rms} + v_D \cdot \bar{i}_D = \frac{r_{S,on} \cdot I^2_{in} \cdot (2d-1)}{12 \cdot n^2} + \frac{v_D \cdot I_{in} \cdot (7-6d)}{8 \cdot n} \tag{C-3}$$

where $r_{P,on}$ and $r_{S,on}$ are the on-state resistance of primary and secondary side switches respectively. v_D is the forward voltage of body diodes of secondary side switches.

The switching loss of primary (ZCS) and secondary side switches (ZVS) are given by

$$P_{P,Sw} = P_{Sw,on} + P_{Sw,off} = C_{snubber\_P} \cdot V_p^2 \cdot f_s + 0 = \frac{C_{snubber\_P} \cdot V_o^2 \cdot f_s}{n^2} \tag{C-4}$$

$$P_{S,Sw} = P_{Sw,on} + P_{Sw,off} = 0 + \frac{I_{off}^2 \cdot t_f^2 \cdot f_s}{24 \cdot C_{snubber\_s}} = \frac{I_{off}^2 \cdot t_f^2 \cdot f_s}{24 \cdot C_{snubber\_s}} \quad \text{(C-5)}$$

Where t_f is the fall time of the secondary side switches during turn-off. $C_{snubber\_p}$ and $C_{snubber\_s}$ is the snubber capacitance of primary and secondary switches respectively.

The copper loss of HF transformer is given by

$$P_{Tr,Copp} = r_{pri} \cdot I_{Llk,rms}^2 + r_{\sec} \cdot \frac{I_{Llk,rms}^2}{n^2} \quad \text{(C-6)}$$

where r_{pri} and r_{sec} are ohmic resistances of primary and secondary sides of HF transformer respectively.

The core loss of boost inductor and HF transformer can be calculated by the following empirical formula [165].

$$P_{L\_core} = C_m V_c f^x B_{AC}^y \quad \text{(C-7)}$$

where V_c represents effective core volume , C_m, x and y are the coefficient of the related core material, B_{AC} is AC flux density.

The total loss is given by

$$P_{loss} = P_{L,Con} + \left(P_{P,Con} + P_{P,Sw}\right) \cdot 4 + \left(P_{S,Con} + P_{S,Sw}\right) \cdot 4 + \left(P_{L,core} + P_{Tr,core}\right) + P_{Tr,Copp} \quad \text{(C-8)}$$

The transfer efficiency is given by

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_{in} \cdot I_{in} - P_{loss}}{V_{in} \cdot I_{in}} \quad \text{(C-9)}$$

List of Publications

Journals

1. P. Xuewei and A. K. Rathore, "Current-fed Soft-Switching Push-pull Front-end Converter Based Bidirectional Inverter for Residential Photovoltaic Power System," *IEEE Transactions on Power Electronics*, vol. 29, no. 11, pp. 6401-6451, Nov. 2014.
2. P. Xuewei and A. K. Rathore, "Novel Bidirectional Snubberless Naturally Commutated Soft-switching Current-fed Full-bridge Isolated DC/DC Converter for Fuel Cell Vehicles," *IEEE Transactions on Industrial Electronics*, vol. 61, no. 5, pp. 2307-2315, May 2014.
3. P. Xuewei and A. K. Rathore, "Novel Interleaved Bidirectional Snubberless Soft-switching Current-fed Full-bridge Voltage Doubler for Fuel Cell Vehicles," *IEEE Transactions on Power Electronics*, vol. 28, no. 12, pp. 5355-5546, Dec. 2013.
4. P. Xuewei, Prasanna U R and A. K. Rathore, "Magnetizing-inductance-assisted Extended range Soft-switching Three-phase AC-link Current-fed dc/dc Converter for Low DC voltage Applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 7, pp. 3317-3328, July 2013.
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8. P. Xuewei and A. K. Rathore, "Naturally Clamped Soft-switching Current-fed Three-Phase Bidirectional DC/DC Converter," *in press, IEEE*

*Transactions on Industrial Electronics (DOI:*10.1109/TIE.2014.2364159*).*

9. P. Xuewei and A. K. Rathore, "Small Signal Analysis of Naturally Commutated Current-fed Dual Active Bridge (CFDAB) Converter and Control Implementation using Cypress PSoC," *in press, IEEE Transactions on Vehicular Technology (DOI:10.1109/TVT.2014.2375828).*

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2. P. Xuewei and A. K. Rathore, "Current-fed Three-Phase Soft-switching DC/DC Converter with Natural Device Commutation and Voltage Clamping," *IEEE International Conference of the Industrial Electronics Society (IECON 2014),* Dallas, TX, USA, 2014.
3. P. Xuewei and A. K. Rathore, "Comparison of Bi-directional Voltage-fed and Current-fed Dual Active Bridge Isolated Dc/Dc Converters for Fuel Cell Vehicles/Energy Storage," *IEEE International Symposium on Industrial Electronics (ISIE)* 2014, Istanbul, Turkey, June 2014.
4. P. Xuewei and A. K. Rathore, "Soft-switching current-fed push-pull converter based bidirectional inverter for residential photovoltaic system," *IEEE International Symposium on Industrial Electronics (ISIE)* 2014, Istanbul, Turkey, June 2014.
5. P. Xuewei and A. K. Rathore, "Novel bidirectional snubberless naturally clamped ZCS current-fed full bridge voltage doubler: analysis, design, and experimental results," *IEEE Energy Conversion Congress and Exposition (ECCE),* USA, Denver, 2013.
6. Prasanna UR, P. Xuewei, A. K. Rathore, and K. Rajasekhara, "Architectural overview of fuel cell vehicle power conditioning: A survey of power converters," *IEEE Energy Conversion Congress and Exposition (ECCE),* USA, Denver, 2013.
7. P. Xuewei and A. K. Rathore, "Novel bidirectional snubberless soft-switching naturally clamped zero current commutated current-fed dual active bridge (CFDAB) converter for fuel cell vehicles," *IEEE Energy Conversion Congress and Exposition (ECCE),* USA, Denver, 2013.
8. P. Xuewei and A. K. Rathore, "Novel soft-switching snubberless naturally clamped current-fed full bridge front-end converter based bidirectional

inverter for renewable, microgrid, and UPS applications," *IEEE Energy Conversion Congress and Exposition (ECCE)*, USA, Denver, 2013.

9. P. Xuewei and A. K. Rathore, "Novel interleaved bidirectional snubberless naturally clamped zero current commutated soft-switching current-fed full-bridge voltage doubler for fuel cell vehicles," *IEEE Energy Conversion Congress and Exposition (ECCE)*, USA, Denver, 2013.
10. P. Xuewei, A. K. Rathore, and A.K.S. Bhat, "Analysis, design, and experimental results of soft-switching current-fed three-phase isolated dc/dc converter: CCM and DCM modes of operation for auxiliary clamp capacitor current," *IEEE International Conference of Power Electronics Drives and Energy Systems (PEDES)*, Bangalore, India, 2012.
11. P. Xuewei, Prasanna UR, and A. K. Rathore, "Magnetizing inductance assisted wide range ZVS three-phase AC link current-fed dc/dc converter with active-clamp: analysis, design and experimental results," *IEEE International Conference of the Industrial Electronics Society (IECON 2012)*, Montreal, Canada, 2012.
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