DESIGN OF INTEGRATED NEURAL/MUSCULAR STIMULATORS

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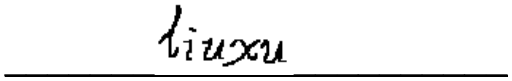
DECLARATION

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.



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SUMMARY

Neural/muscular stimulator has been used in medical therapies, as well as therapeutical devices. It delivers either current or voltage to the tissue through electrodes, evoking action potentials in the nerves or muscles. This thesis focuses on the power efficiency improvement of the neural/muscular stimulator and the cancellation of the artifacts introduced by the stimulation. A current-mode neural/muscular stimulator with an exponentially decaying stimulation current is first described. The use of exponentially decaying current makes the voltage on the stimulating electrode constant during the stimulation, which eliminates the headroom and increases the power efficiency. A simple exponentially decaying current generator is proposed based on Taylor series approximation and implemented in a 16-channel prototype stimulator IC. The prototype IC is fabricated in a 0.18-μm CMOS process with high-voltage LDMOS option, occupying a core area of 1.65 mm × 1.65 mm. The stimulator is tested with different loads, which mimics the electrode/tissue interface, and the measured results show that maximum stimulation power efficiency of 95.9% can be achieved at the output stage of the stimulator. Depending on the electrode impedance and stimulation current, the power efficiency can be improved by nearly 10% at the output stage, compared to traditional constant-current stimulators.

In the second part of the thesis, an artifact-suppression technique based on a referenced and tuned push-pull stimulation (RTPPS) scheme with a tri-polar electrode is presented. The stimulation pulses delivered to two working electrodes with a

common reference electrode are complementary and thus one counteracts with the other to suppress the stimulation artifact. A prototype 4-channel integrated recording and stimulation system is designed to demonstrate the proposed artifact-suppression technique and implemented in 0.18-μm CMOS technology. The chip can be externally programmed and work in four different modes, namely, recording (REC), stimulation (STIM), closed-loop recording-stimulation (REC-STIM) and closed-loop stimulation-recording (STIM-REC). Both in-vitro and in-vivo experiments are carried out using rats as an animal model. The results show that the stimulation artifact can be greatly reduced compared to the conventional bipolar stimulation with no artifact cancellation. The amplitude of the measured stimulation artifact is suppressed to only 10%-20% of the neural spikes to be recorded in the animal experiment.

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LIST OF ABBREVIATIONS

ACB	Active Charge Balancing
AP	Action Potential
APD	Action Potential Detector
BPF	Band pass filter
CAP	Compound action potential
CCG	Counter Current Generator
CE	Counter Electrode
DAC	Digital to Analog Convertor
DBS	Deep brain stimulation
ECG	Electrocardiogram
EEG	Electroencephalogram
ESD	Electro-Static Discharge
FES	Functional Electrical Stimulation
FF	Flip-flop
FPGA	Field Programmable Gate Array
GDC	Global digital control
HVAS	High-voltage artifact-suppressed stimulator
HVCD	High-Voltage Current Driver
LPF	Low pass filter
LSB	Least Significant Bit

MOS	Metal-oxide semiconductor
MSB	Most significant bit
PBS	Phosphate buffered saline
PD	Power down
PE	Power efficiency
RE	Reference electrode
REC	Recording
RFE	Recording front end
RTPPS	Referenced and Tuned Push-Pull Stimulation
SCG	Stimulation Current Generator
STIM	Stimulation
WE	Working Electrode

CHAPTER 1
INTRODUCTION

1.1 Background

In the past few decades, driven by the increasing demands from biomedical field aiming to cure neurological diseases and improve the quality of patients' daily life, researchers began to take advantage of the semiconductor technology to develop miniaturized and power efficient stimulators for implantable applications. Examples of such applications include deep brain stimulation (DBS) [1], pain management and relief [2], retinal/cochlear/neural prosthesis [3-4], and functional electrical stimulation (FES) [5].

1.1.1 Basic principles of Neural/Muscular Stimulation

The aim of electrical stimulation of tissue (nerve or muscle) is to trigger action potentials (AP) in axons, which requires the artificial depolarization of some portion of the axon membrane to a threshold voltage [6]. As shown in Fig. 1.1, in one of a bunch of muscle cells, the membrane forms a boundary that separates fluids within and outside the cell. Ions composition in both intracellular and extracellular fluid creates a transmembrane potential of about -90 mV in normal state (the potential of extracellular fluid is taken as reference at 0V). During stimulation, electric current charges the extracellular fluid through the stimulation electrode and decrease the

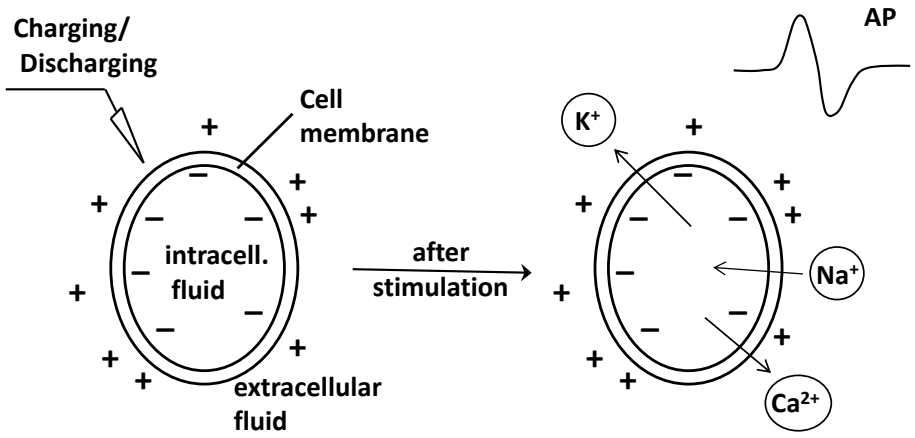


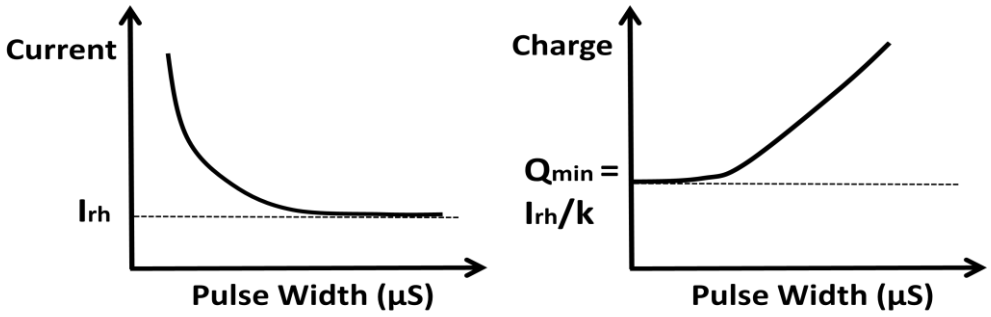
Figure 1.1 Principle of electrical stimulation.

potential of the extracellular fluid. Once the transmembrane potential rises from -90 mV to a threshold voltage (around -55 mV) due to electric charging, an AP is produced. When an AP occurs, the channel on the membrane is open and K^+ or Ca^{2+} ions go out of the cell until the membrane potential recovers to its rest state.

The relationship between the stimulation current sufficient for triggering an action potential and the stimulation duration is shown in Fig. 1.2(a). The threshold current I_{th} decreases with increasing stimulation pulse width. The minimum required stimulation current is called the rheobase current (I_{rh}). The following relationship [7] has been derived experimentally to quantify the strength-duration curve:

$$I_{th} = \frac{I_{rh}}{1 - \exp(-W / \tau_m)}$$

where I_{th} is the current required to reach threshold, I_{rh} is the rheobase current, W is the stimulation pulse width, and τ_m is the membrane time constant. Fig. 1.2(b) shows the charge-duration curve, which plots the threshold charge $Q_{th} = I_{th}W$ versus

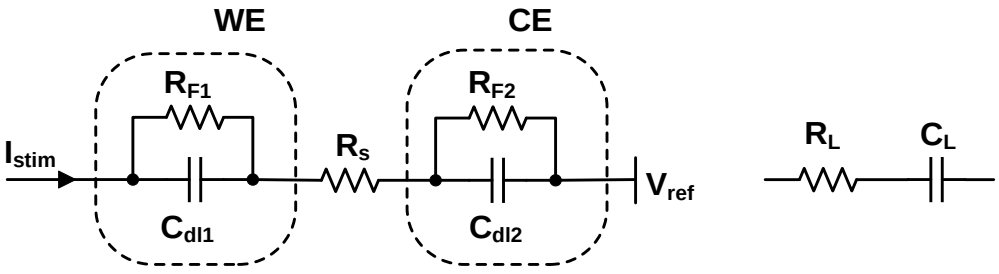


(a) (b)

Figure 1.2 Strength-duration and charge-duration curves for initiation of an action potential.

stimulation pulse width. It is found that an action potential can be excited either by a minimum current with a certain pulse width or a minimum amount of charge injected.

Monophasic and biphasic rectangular waveforms are two widely used stimulation waveforms in existing stimulators. In monophasic stimulation, a negative current pulse is generated to excite the tissue and an action potential is produced. Monophasic stimulation is effective to initiate an AP but it may damage the tissue and electrodes during long period stimulation due to the accumulated residual charge and electrochemical reactions. In biphasic stimulation, the output is a negative current pulse followed by a positive one. The first pulse (negative pulse) elicits the desired physiological effect and produces an AP, and the second pulse (positive pulse) reverses the direction of electrochemical processes occurred during the cathodic stimulating phase. Compared to monophasic stimulation, the biphasic stimulation greatly reduces the chance of tissue damage. In addition to aforementioned waveforms, non-rectangular stimulus waveforms have also been proposed, which may



(a) (b)

Figure 1.3 Electrical circuit models: (a) electrode-tissue interface, (b) simplified model.

offer safety benefits while maintaining stimulation efficacy [8].

Electrode materials used in neural stimulation should be biocompatible and non-toxic, and should have large charge storage capacity. Platinum (Pt), gold (Au), iridium (Ir), and palladium (Pd) have been commonly used for fabricating stimulation electrodes due to their relative resistance to corrosion. Especially, platinum and platinum-iridium alloys are common materials used for electrical stimulation of excitable tissue [6]. In general cases, two electrodes are placed in a tissue and electrical current passes from one electrode to another through the tissue. The electrode-tissue interface consists of a working electrode (WE) and a counter electrode (CE), as modeled in Fig. 1.3(a). R_S is solution resistance which exists between two electrodes. C_{dl1} and C_{dl2} are the double layer capacitors representing charge storage. R_{Fl} and R_{F2} are Faradaic resistors which are very large and can be neglected. The double layer capacitor of counter electrode (C_{dl2}) is rather large and can also be neglected [9]. Therefore, the electrode-tissue interface can be simply modeled as a series resistor R_L and a series capacitor C_L, as shown in Fig. 1.3 (b). The value of R_L and C_L depend on the tissue impedance as well

as the electrode properties.

There are two kinds of damages that could occur during stimulation: electrode corrosion and tissue damage.

$$2H_2O \rightarrow O^2\uparrow + 4H^+ + 4e^- \quad \text{(oxidation of water)} \quad (1\text{-}1)$$

$$Pt + 4Cl^- \rightarrow [PtCl4]^{2-} + 2e^- \quad \text{(corrosion)} \quad (1\text{-}2)$$

In reaction (1-1), water molecules are irreversibly oxidized, forming oxygen gas and hydrogen ions, and thus lowering the pH. Reaction (1-2) is the corrosion of a platinum electrode in a chloride-containing media. Irreversible Faradaic reactions result in a net change in the chemical environment, potentially creating chemical species that are damaging to tissue or the electrode [6]. Studies have shown that both charge per phase and charge density are important factors in determining neural damage [10]. Some studies showed that charge-balanced biphasic stimulation does not cause significant tissue damage at levels up to 2 $\mu C/mm^2$ per pulse. However, in order to prevent electrode corrosion, the charge-balanced waveform must not exceed 0.4 $\mu C/mm^2$ per

Table 1. Efficacious stimulation properties

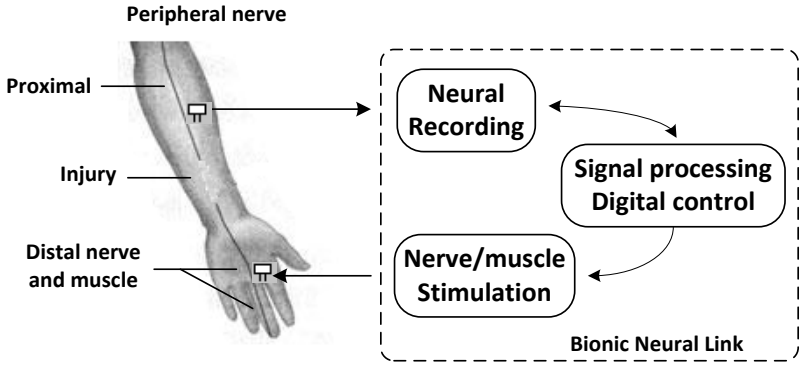
Stimulation duration	tens - hundreds μs
Stimuli source	minimum current or charge
Waveform	balanced and biphasic
Interphasic delay time	0 - 100 μs
Electrode-tissue model	a series capacitor and a series resistor
Safe level	0.4 $\mu C/mm^2$/phase

pulse, otherwise the electrode potential is driven to damaging positive potentials during the anodic (reversal) phase and interphasic delay time [11-12]. The electrode potential must be kept within a potential window (safety window) where irreversible electrochemical reactions do not happen at levels that are intolerable to the physiological system or the electrode [6]. Current density in each stimulation cycle also affects the damage on tissue. It is concluded that under the experimental conditions used in a reported study, the Q value (charge per phase) was the most important stimulus value in predicting neural damage. The level of 0.3 - 0.4 μC/ph is demonstrated to be safe in long time stimulation [13]. Table I summarizes the efficacious and safe stimulation parameters.

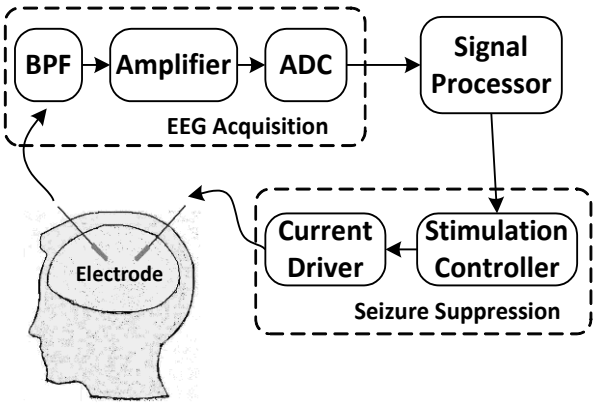
1.1.2 Design Consideration of Neural/Muscular Stimulation System

Most neural/muscular stimulation systems consist of voltage/current generation circuit, output driver, and digital control circuit. One of the major concerns in developing implantable stimulation system is the power efficiency, which is defined as the ratio of power delivered to the load (P_{load}) to the total power consumed by the stimulator (P_{tot}). Stimulation power efficiency is becoming increasingly important due to the limited power budget in the implantable circuit and systems nowadays. It determines the battery lifetime or the required coil size for wireless power transfer. Stimulator with high power-efficiency also generates less heat and reduces the risk of tissue damage [14]. The techniques of improving power-efficiency of the stimulator will be discussed in chapter 2.

Another concern is the stimulation artifact. It is known that neural/muscular stimulators have been mostly applied in neural prosthesis systems, and neural recording is also involved in these applications to sense and generate trigger signal for stimulation or to provide assessment of stimulation efficacy and tissue status to enable closed-loop control for stimulator or simultaneous neural recording and stimulation



(a)



(b)

Figure 1.4 Concept of (a) Bionic neural link and (b) Epileptic seizure detection and suppression using a closed-loop neural recording and stimulation system.

[1], [15-22]. In aforementioned applications, the stimulation induced artifact usually exists and is an undesired signal recorded during stimulation. As the artifact voltage is overwhelmingly large compared with the neural signals (a few tens to several

hundreds of millivolts), the artifact could easily corrupt the neural signal and overload the recording amplifier. Consequently it affects the quality of neural recording and neural spike detection. In the applications where the stimulation is controlled by the action potential (AP), such as the peripheral nerve prosthesis in [19], when the AP is detected, it triggers the stimulator and stimulates the muscle, as shown in Fig. 1.4(a). The large stimulation pulse causes the artifact which is subsequently picked up by the recording amplifier as a false AP and a false stimulation will be triggered. The situation is even worse in multi-channel neural recording and stimulation system [23]. In the closed-loop neural recording and stimulation application, such as epileptic seizure detection and suppression, when epileptic seizure episode in EEG is detected, the stimulator is triggered and generates pulses to stimulate certain region in the brain and suppress the epileptic seizure [24-26], as shown in Fig. 1.4(b). To avoid stimulation induced artifact, the recording amplifier has to be reset when artifact is detected, and the normal recording can only be resumed after the stimulation when the stimulator is turned off [27].

1.2 Motivation

As mentioned before, power efficiency of the neural/muscular stimulator is an important performance and needs to be improved. While, other performances such as chip area, safety, and stimulation effectiveness of neural/muscular stimulator also need to be considered and balanced in circuit design. Besides, stimulation artifact is

always a problem existing in the applications of closed-loop neural prosthesis systems. Therefore, this work focuses on two problems, namely, the power-efficiency of the neural/muscular stimulators and the stimulation-artifact cancellation. The objectives are (1) to develop a power efficient neural/muscular stimulator, in particular, to eliminate the headroom existing in the stimulators that employ constant current pulse stimulation, without sacrificing other performance of the stimulator, and (2) to suppress the stimulation induced artifact without the need to disable the recording amplifier in recording/stimulation systems.

1.3 Research Contributions

A technique to further enhance the power efficiency of the output stage of the stimulator is proposed, in which an exponential stimulation current is employed. The proposed method eliminates the remaining headroom at the output stage and can also be employed together with the supply adaptation technique to obtain the maximum power efficiency. The proposed technique is demonstrated in a prototype 16-channel stimulator with a novel exponential current generator. In addition, the stimulator developed in this research integrates many functions on chip, including high voltage compliance, active charge balance, high power efficiency and small chip area. Maximum stimulation power efficiency of 95.9% can be achieved at the output stage of the stimulator, which is higher than most previous current-mode stimulators. Depending on the electrode impedance and stimulation current, the power efficiency

can be further improved by nearly 10% at the output stage, compared to traditional constant-current stimulator.

A stimulation artifact cancellation technique with a tri-polar electrode using referenced and tuned push-pull stimulation (RTPPS) scheme is also proposed to suppress the artifact with no blanking of the recording channels is needed. Unlike the previously reported artifact suppression techniques, the RTPPS cancels the artifact at the stimulation site before it propagates to the recording front-end. The RTPPS uses a tri-polar stimulation configuration with two working electrodes and one reference electrode. The stimulation currents delivered by two working electrodes are complement to each other. By doing so, the impact of large stimulation voltage fluctuation propagated to the recording site can be significantly reduced. The proposed concept is demonstrated with a prototype integrated 4-channel closed-loop neural recording/stimulation system in both in-vitro and in-vivo experiments.

1.4 List of Publications

The following publications from this study have been either published or submitted.

[1] Xu Liu, Lei Yao, et al., "A 16-channel 24-V 1.8-mA power efficiency enhanced neural/muscular Stimulator with exponentially decaying stimulation current," *IEEE Int. Symposium on Circ. and Syst*., 2015, accepted.

[2] Xu Liu, Lei Yao, et al., “Stimulation artifact suppression with a referenced and tuned push-pull stimulator,” submitted.

[3] Xu Liu, Lei Yao, Minkyu Je, Ng Kian Ann, Yong Ping Xu, “An artifact-suppressed stimulator for neural recording and stimulation system”, *Singapore provisional application patent*, IME ref: PAT12-071/MMD-009, filed, Sep. 2012.

[4] Lei Yao, J. Zhao, P. Li, Xu Liu, Y. P. Xu, M. Je, “Implantable stimulator for biomedical applications", *IEEE MTT-S International Microwave Workshop Series on RF and Wireless Technologies for Biomedical and Healthcare Applications (IMWS-BIO)*, Dec. 2013, pp. 1-3.

[5] K.A. Ng, Xu Liu, Jianming Zhao, Li Xuchuan, Shih-Cheng Yen, Minkyu Je, Yong Ping Xu, Ter Chyan Tan, “An inductively powered CMOS multichannel bionic neural link for peripheral nerve function restoration,” *IEEE Asian Solid State Circuits Conference (A-SSCC)*, 2012, pp. 181 – 184.

[6] Yong Ping Xu, Shih-Cheng Yen, K.A. Ng, Xu Liu, Ter Chyan Tan, “A bionic neural link for peripheral nerve repair,” *IEEE Annu. Int. Conf. Eng. in Medicine and Biology Society (EMBC)*, 2012, pp. 1335 – 1338.

[7] J.Y.J. Tan, Xu Liu, K. H. Wee, Shih-Cheng Yen, Yong Ping Xu, T.C. Tan, “A monolithic programmable nerve/muscle stimulator,” *IEEE Annu. Int. Conf. Eng. in Medicine and Biology Society (EMBC)*, 2011, pp. 511 – 514.

[8] J.Y.J. Tan, Xu Liu, K. H. Wee, Shih-Cheng Yen, Yong Ping Xu, “A programmable muscle stimulator based on dual-slope charge balance,” *IEEE Asian Solid State Circuits Conference (A-SSCC)*, 2011, pp. 197 – 200.

1.5 Organization of the Thesis

The organization of this thesis is as follows:

Chapter 2 presents the literature review on recent advances in power-efficient neural/muscular stimulator, and artifact-suppressed closed-loop stimulation and recording system. Chapter 3 deals with the design and implementation of the proposed power efficient neural/muscular stimulator and measurement results. Chapter 4 describes the design and implementation of artifact-suppressed neural/muscular stimulator, as well as the in vitro and in vivo experiment results. Conclusion and future work are presented in Chapter 5.

CHAPTER 2

LITERATURE REVIEW

2.1 Power Efficient Neural/Muscular Stimulator

The neural or muscular stimulation can be performed in voltage, charge or current mode, as shown in Fig. 2.1. The voltage-mode stimulator shown in Fig. 2.1(a) generates a voltage directly on the tissue load. If only the output stage is considered, the power efficiency of the stimulator is given by

$$PE(t) = \frac{P_{load}(t)}{P_o(t)} = \frac{V_{load}(t) \cdot I_{load}(t)}{V_{stim}(t) \cdot I_o(t)} = \frac{V_{load}(t)}{V_{stim}(t)} \tag{2-1}$$

in which $V_{load}(t)$ is the voltage over the load, $V_{stim}(t)$ is the stimulation voltage and $I_o(t)$ is the resultant current in the output stage, respectively. It is known that the voltage-mode stimulation provides the highest power efficiency [28-30] because ideally V_{load} equals to V_{stim} at the output stage of the stimulator. Nonetheless, its

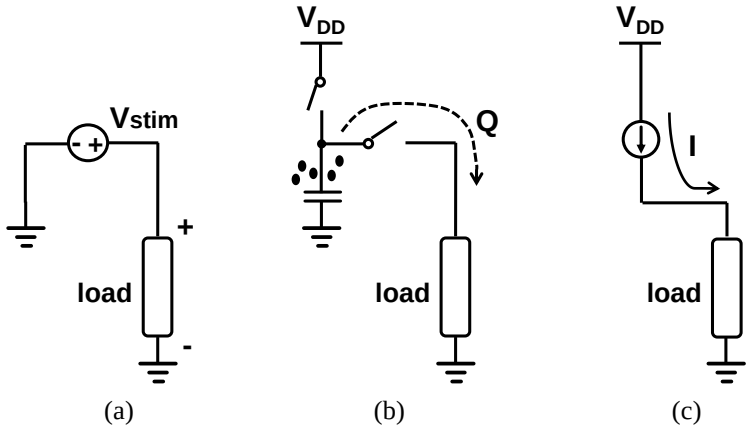


Figure 2.1 Conceptual diagrams of the stimulators based on (a) voltage-mode, (b) charge-mode, and (c) current-mode stimulation.

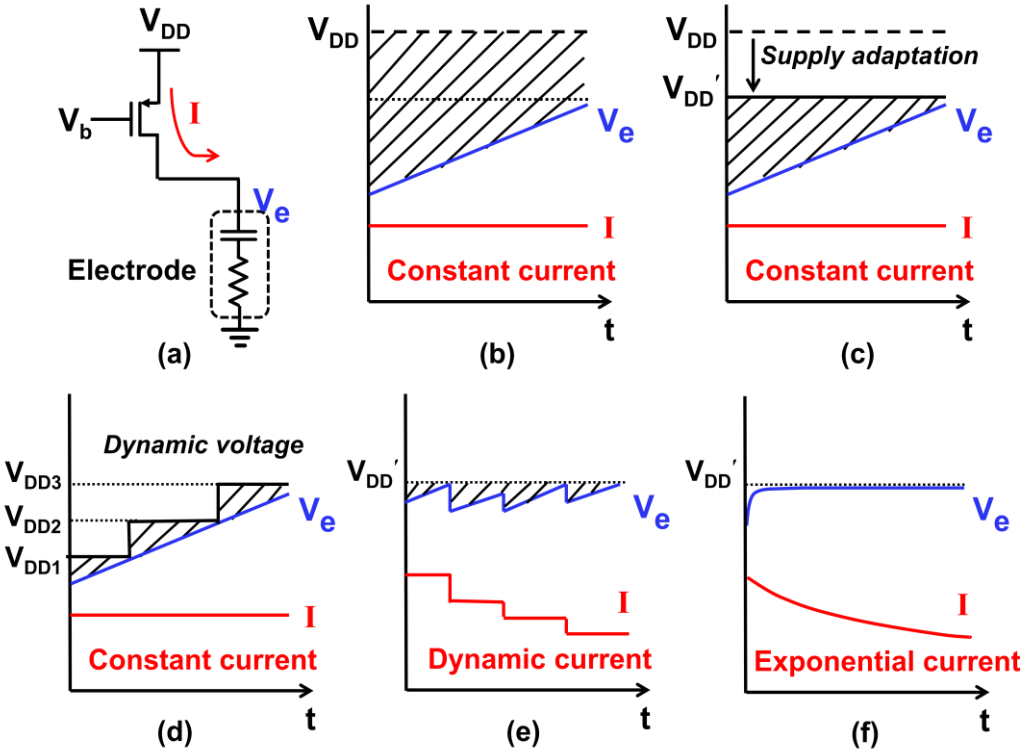


Figure 2.2. (a) Simplified model of the current-mode stimulator, (b) Power wasted (shaded area) in conventional stimulators (c) in supply adaptation method, (d) in dynamic voltage scaling (e) in dynamic current control, and (f) proposed time-continuous exponential current stimulation.

uncontrolled or inaccurately controlled current and charge injection makes the voltage-mode stimulation inappropriate for clinical applications. The charge-mode stimulation as shown in Fig. 2.1(b) has accurate control over the amount of injected charge. However, it requires large capacitors (~μF), which prevents its adoption in implantable applications particularly when the multi-channel stimulation is required. The above-mentioned deficiencies of voltage-mode and charge-mode stimulation methods make the current-mode stimulation the most widely adopted method in biomedical applications [5], [31-36].

However, traditional current-mode stimulator with constant stimulation current

usually has the lowest power efficiency compared to voltage-mode and charge-mode stimulators [30], [32]. This is because the power efficiency of current-mode stimulators depends on the load (electrode) impedances and degrades dramatically when the voltage across the load $V_{load}(t)$ is low, as illustrated in Fig. 2.2(a) and (b). The shaded headroom area indicates the power wasted by the stimulation circuit, which reduces the overall power efficiency of the stimulator.

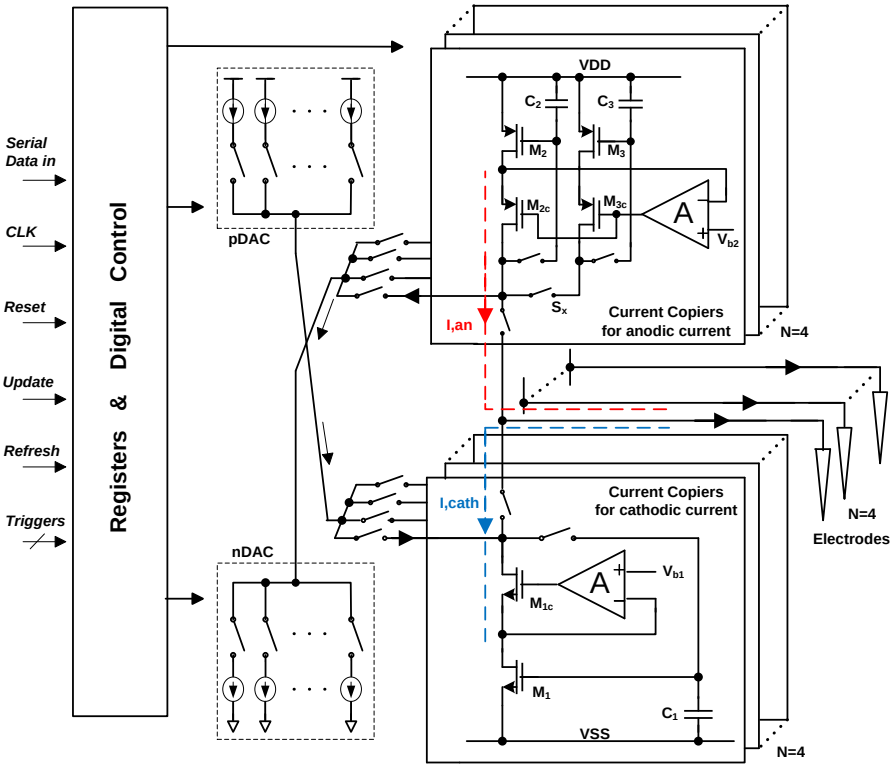


Fig. 2.3 A traditional current-mode stimulator [23].

Fig. 2.3 shows a general neural/muscular stimulator [23]. It contains a digital control block, two DACs, and two groups of current copiers. Amplifiers are used at the output branch to increase the output impedance. Constant anodic and cathodic current can be generated and output to the electrodes. A single power supply of 3.3V is used for the

chip. As mentioned previously, the power efficiency of this traditional constant current stimulator is not high due to the headroom across transistors M_1 and M_2.

In order to overcome this drawback, that is, to eliminate the shaded area shown in Fig. 2.2(b), several techniques have been reported. A supply adaptation technique was proposed, in which the supply voltage is adjusted according to the maximum voltage on the electrode [14], [37]. Its system architecture is shown in Fig. 2.4. The adaptive rectifier in the power management circuit can output adjustable supply voltage ranging from 2.5 V to 4.6 V (at 2.8 mA loading) to power the stimulator. The desired supply voltage is determined by the load maximum voltage during stimulation

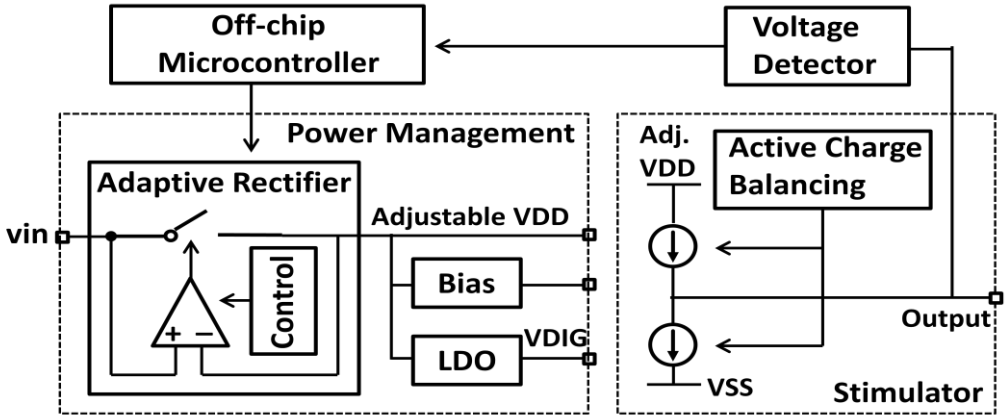


Figure 2.4 Overall architecture of the power-efficient stimulation system using supply adaptation technique [14].

through the voltage detector and controlled by an off-chip microcontroller. The active charge balancing circuit in the stimulator removes the residual charge after each stimulation pulse to prevent tissue damage. As indicated in Fig. 2.2(c), this power-efficient stimulator using supply adaptation technique reduces the shaded area, but not completely. Dynamic voltage and current scaling techniques have been

proposed to further improve the PE by adjusting the supply voltage [33], [38] or the stimulation current [39] in number of steps, as shown in Fig. 2.2(d) and (e). However the shaded area still cannot be completely eliminated unless a large number of steps is used, which requires more control circuits and computation resources to achieve optimal power efficiency.

The stimulator [33] using dynamic voltage scaling techniques is shown in Fig. 2.5. A DC-DC converter providing 3V, 6V, 9V and 12V supply for stimulation is designed. During stimulation, the electrode voltage is detected and compared to different reference voltages, and meanwhile the corresponding stimulation voltage (Vstim) is chosen and applied. Power efficiency can be improved by using this dynamic voltage scaling technique. Besides non-ideal power efficiency of DC-DC converter, the

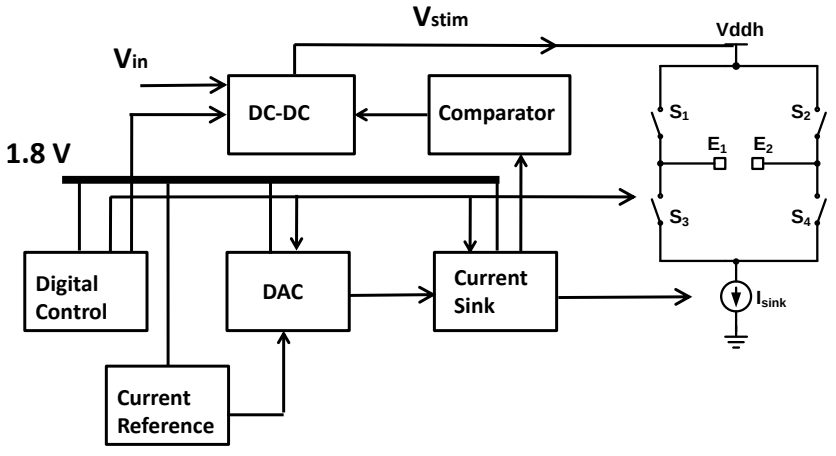


Fig. 2.5 Stimulator using dynamic voltage scaling technique [33].

limited number of voltage steps still make the stimulator unable to completely remove the headroom, as shown in Fig. 2.2(d).

Another stimulator [39] shown in Fig. 2.6 using dynamic voltage scaling technique is proposed trying to further improve the power efficiency at the output stage. The supply voltage V_{DD} of the electrode driver is generated from rectified voltage (V_{RF}) separately by a regulation switch (S_0). A capacitor (C_{DD}) reduces the ripple on V_{DD}. A continuous-time comparator, a Schmitt trigger and a controller constitute a feedback loop, which is active throughout all RF cycles of each stimulation period. The comparator compares V_{RF} with V_{DD}. The Schmitt trigger compares Vs with an upper threshold and a lower threshold. The binary output signals Y_1 and Y_2 of these two units are fed into the controller, which, in turn, drives S_0 with a binary output signal Y_S. During stimulation, the voltage Vs is kept within a very small window similar to Ve as shown in Fig. 2.2(e). The headroom voltage across current source (Is) can be adjusted to a small value, as such, the power efficiency is improved. However, to achieve a very small ripple of Vs, capacitor CDD must be very large (1.5 nF, in their

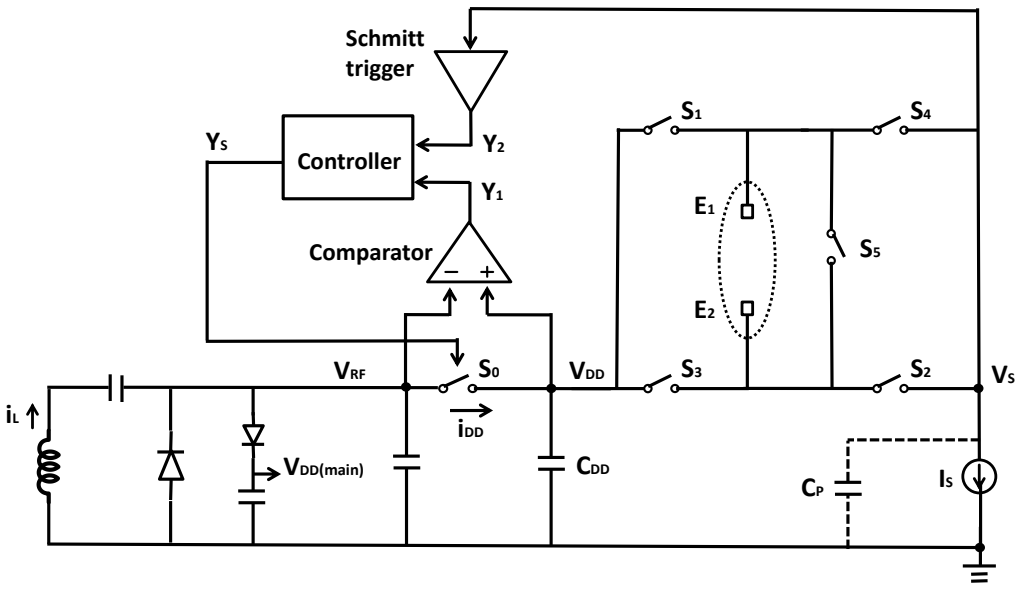


Fig. 2.6 Another stimulator using dynamic voltage scaling technique [39].

design), making the stimulator not suitable for implantable applications. Besides, the

power efficiency is still not completely optimized due to the ripple on Vs.

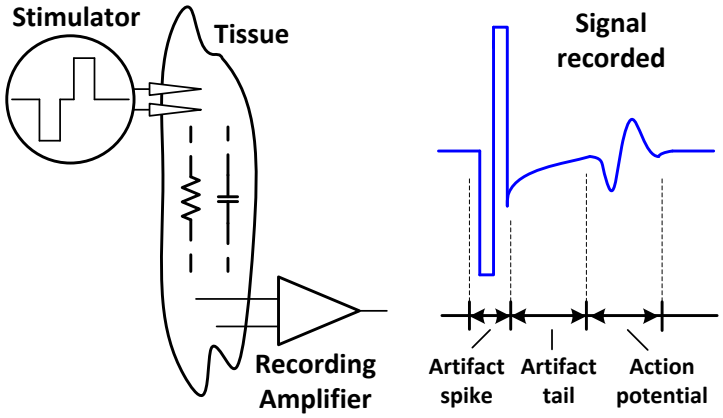
In this work, a technique that uses exponentially decaying stimulation current to eliminate the headroom and improve the power efficiency of the stimulator is proposed and will be described in Chapter 3. With an exponentially decaying stimulation current, as shown in Fig. 2.2(f), the voltage on the stimulation electrode can be made relatively constant and thus minimizes the power wasted in the triangular shaded area (as in Fig. 2.2(b) and (c)) which is caused by the capacitive loading from the electrode. The proposed method can also be employed together with the supply adaptation technique (as in Fig. 2.2(c)) to obtain the maximum power efficiency.

2.2 Stimulation-Artifact Suppressed Stimulator

2.2.1 Origin of Stimulation Artifact

Most neural/muscular recording and stimulation systems consist of multiple recording and stimulation channels, action potential detection and data processing circuit, stimulation circuitry, and electrodes. During the operation, the large stimulation current causes the tissue potential to change and this tissue potential fluctuation will propagate to the recording site and cause artifacts [40] as illustrated in Fig. 2.7. For bipolar stimulation, there are two stimulation electrodes, namely, a working and a reference electrode. During stimulation, most of the biphasic current flows between the working and the reference electrode through the tissue being stimulated. In the cathodic phase, the electric potential near working electrode decreases since the

stimulator sinks current from the reference electrode. While in the anodic phase, the electric potential near working electrode increases since the stimulator sources current to the reference electrode through the tissue-electrode interface. The amplitude of this



(a) (b)

Figure 2.7 (a) Origin of the stimulation induced artifact and (b) recorded action potential with artifact.

voltage variation is usually from several hundred millivolts to several volts. It depends on several factors, including electrode impedance and power-supply voltage at the output stage of the stimulator. Furthermore, this large voltage variation at the stimulation site can propagate to the recording front end (RFE) through the tissue which is a volume conductor. Although the coupled voltage signal is attenuated when reaching the recording sites, it is still much larger than the neural signal to be recorded, and hence it could saturate the recording amplifier, causing the artifact [41-42].

Fig. 2.7 (b) illustrates the recorded stimulation artifact waveform in a typical neural recording and stimulation system, in which the evoked action potential (AP) is

recorded after an undesired artifact spike. The RFE is initially saturated by the large stimulation artifact, followed by a long artifact tail before the amplifier is fully recovered and ready to record next AP [40]. The RFE output becomes saturated because of its high gain (usually 500 – 1000 times) and the long recovery time is required due to the time constant of the high-pass filter in RFE, which is usually very large (2-10 ms) in order to block the DC offset without attenuating the useful low-frequency signal. As a result, the next AP can only be observed after the recording amplifier fully recovers. Such a stimulation artifact can be observed in most of the closed-loop recording and stimulation systems [19-23], [43].

Though the amplitude of the recorded artifact spike is determined by several factors such as distance between recording and stimulation sites, gain of the amplifier, and electrode impedance [41-42], [44-45] it is typically hundreds of millivolts that is ten to hundred times higher than the amplitude of the neural signals recorded.

2.2.2 Stimulation Artifact Cancellation

Several stimulation artifact cancellation techniques have been reported previously. Blanking technique [20], [46-51] and digital signal processing [52] have been used to cancel the artifact. In the blanking technique, the RFE is switched off or disabled (input is short to ground) during stimulation period and turned on after the stimulation is completed to continue the recording. As shown in Fig. 2.8, the recording amplifier and two capacitors (C_I and C_F) are used to amplify nerve signals. A very large resistor

R_F is used in the feedback path to provide a dc current path to bias the input. The discharge amplifier helps the electrode return to its pre-stimulation voltage after stimulation. The recording amplifier is disabled during stimulation and enabled after 2 ms when the stimulation ends [22]. This method is effective in some applications, such as EMG signal observation, because the evoked neural spike usually emerges with latency causing no overlap between artifact spike and AP. But in some other applications, such as neural prosthesis or deep brain stimulation (DBS), the neural responses in the cathodic and anodic stimulation phases also need to be recorded. In such applications, if blanking technique is employed, the neural signals during the "blanking" period cannot be recorded and thus some important neural information may be missed.

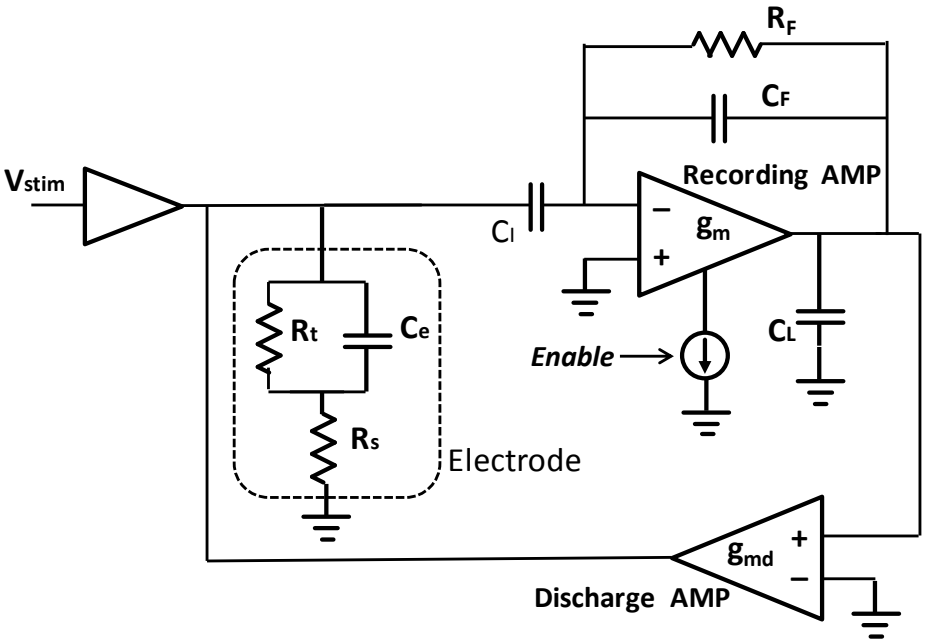


Figure 2.8 Recording, stimulation, and artifact elimination system with blanking technique [22].

The artifact cancellation using digital signal processing can be divided into two categories: post-signal processing and real-time signal processing. In post-signal processing, the recorded neural signal together with artifact is acquired. The artifact is subsequently removed by specific algorithms such as subtraction, time-delayed de-correlation and adaptive filtering in digital domain, either in hardware of software [53-58]. One disadvantage of post-signal processing is that the RFE must have large dynamic range so that the artifact does not saturate the amplifier. In real-time signal processing for artifact cancellation, the artifact can be removed in real-time by using analog or digital signal processing implemented in hardware [59-61]. The merit of removing artifact using digital processing compared with blanking is that no neural spikes are missing in the recording, but they are computationally intensive.

Another artifact suppressing technique reported is the localized stimulation [62-63], where the stimulation current returns to a local ground. Although this reduces the artifact amplitude at input of the recording amplifier, and allows the amplifier to quickly recover to the normal state, the artifact is still not effectively suppressed especially when the large stimulation current is applied. Its effectiveness also depends on the distance between recording site and stimulation site.

Several other artifact cancellation methods have also been proposed. In [64], neural recording is carried out only in the mid-phase between cathodic and anodic stimulation phases to avoid the artifact. In [65-66], high-frequency short-duration

pulses or other specific patterns are adopted for stimulation. However the stimulation parameters (i.e. pulse width, amplitude, and frequency) are usually determined by the application and not by the artifact cancellation.

Aforementioned solutions for artifact suppression are mainly on the effort of recording amplifier design or data processing. To realize a bidirectional stimulation and recording system where both recording-stimulation and stimulation-recording mode can be applied, we need to suppress both artifact-spike and artifact-tail. If the stimulation artifact can be cancelled at the stimulation site, we could avoid disabling (blanking) the RFE and record all neural spikes during stimulation, and simplify the

Table 2. Summary of stimulation-artifact cancellation techniques

Artifact Cancellation Technique	**Advantage**	**Disadvantage**
Blanking	Easy to implement, Save computation resource.	No recording in blanking period.
Localized stimulation	No extra circuit is used, Save computation resource.	Effectiveness depends on current amplitude and distance between electrodes. Require more than one reference electrodes.
Digital signal processing	No data/signal missing.	Require large dynamic range in RFE and extra software/ hardware implementation, Computationally intensive.
Special recording/ stimulation pattern control	No extra circuit is used, No data/signal miss, Save computation resource.	Limited flexibility of stimulation parameters.

backend digital processing and save time/computation resource. Table 2 summarizes the advantages and disadvantages of the existing stimulation-artifact cancellation techniques.

CHAPTER 3

DESIGN OF NEURAL/MUSCULAR STIMULATOR FOR ENHANCED POWER EFFICIENCY

3.1 Theoretical Analysis

3.1.1 Current Waveform for High Power Efficiency

To deliver enough current to the high impedance load, the output stage of the current-mode stimulator is used to amplify the stimulation current and increase output voltage compliance. The output stage of the stimulator is usually powered under a supply from 10 V to 20 V and the rest of the circuits are operating under a low supply voltage in order to reduce the power consumption. With a current amplification ratio of 6 to 10, nearly 95% - 99% of the power is consumed at the output stage during stimulation. If only the output stage is considered, the power efficiency at the output stage can be calculated by

$$PE(t) = \frac{P_{load}(t)}{P_o(t)} = \frac{V_e(t) \cdot I_{stim}(t)}{V_{DD} \cdot I_{stim}(t)} = \frac{V_e(t)}{V_{DD}}, \quad (3\text{-}1)$$

where I_{stim} is the stimulation current, V_{DD} is the supply voltage of the output stage. V_e(t) is determined by the load impedance and stimulation current, which is always smaller than V_{DD}. Thus the current-mode stimulator usually has the lowest power efficiency.

In order to maximize the power efficiency, a constant voltage close to V_{DD} is preferred on the stimulation electrode. Based on the circuit model in Fig. 2.2(a), the voltage on

the load during stimulation is

$$V_e(t) = I(t) \times R_L + \int_0^t \frac{I(t)}{C_L} dt \tag{3-2}$$

where $V_e(t)$, $I(t)$, R_L and C_L are the electrode voltage, stimulation current, load resistance, and load capacitance, respectively. The constant load voltage can be realized during stimulation when the following equation is fulfilled:

$$\frac{dV_e(t)}{dt} = \frac{d}{dt}\left(I(t) \times R_L + \int_0^t \frac{I(t)}{C_L} dt \right) = 0 \tag{3-3}$$

By solving (3-3), $I(t)$ can be expressed as

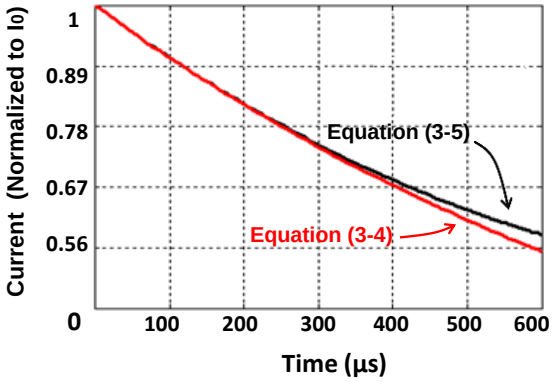
$$I(t) = I_0 \exp(-\frac{t}{R_L C_L}) \tag{3-4}$$

where I_0 is the initial value of the stimulation current. The exponentially decaying current in (3-4) can be expressed by its Taylor Series. Considering that ($t/ R_L C_L$) is usually small (around 0.2) in biomedical applications [67], high order terms can be neglected and (3-4) can be approximated by the 2nd-order Taylor series as given below.

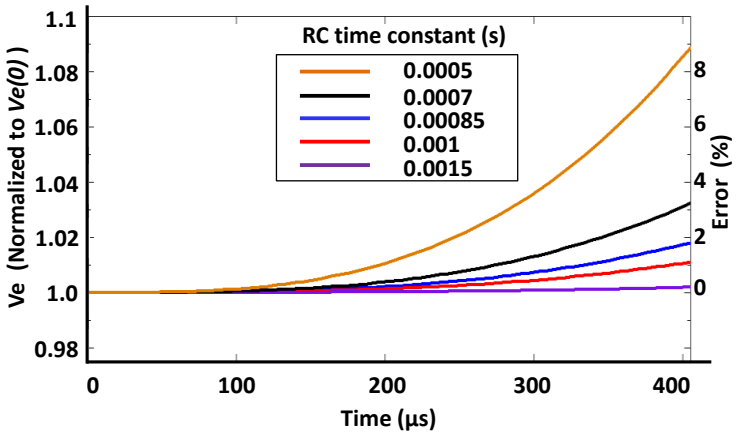
$$\begin{aligned} I(t) &\approx I_0 \left(1 + \left(-\frac{1}{R_L C_L} \right) t + \frac{1}{2} \left(\frac{1}{R_L C_L} \right)^2 t^2 \right) \\ &= \frac{I_0}{2} \left(1 + (1 - \frac{1}{R_L C_L} t)^2 \right) \end{aligned} \tag{3-5}$$

Fig. 3.1(a) shows that the error of (3-5), resulting from the approximation, is less than 0.6% at stimulation duration of 200 μs and maximum 5.6% at 600 μs under a typical electrode load of 10 kΩ and 100 nF [67]. Fig. 3.1(b) shows the electrode voltage V_e calculated by integrating the approximated current in (3-5). Different $R_L C_L$ are used

for covering the range of load variation from 50% to 150% of the default R_LC_L value (1 ms) and it is found that the electrode voltage, V_e, is nearly constant (variation less than 3%) for t < 250 μs.



(a)



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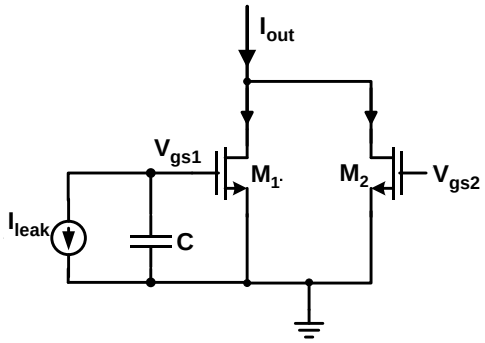


(c)

Figure 3.1 (a) Comparison between the ideal exponential current waveform and its 2nd-order Taylor series approximation (exponentially decaying current waveform), (b) electrode voltage calculated by integrating the exponentially decaying current, (c) exponentially decaying current generation circuit.

3.1.2 Exponentially Decaying Current Generation

Fig. 3.1(c) is the proposed exponentially decaying current generation circuit according to (3-5). Transistors M_1 and M_2 have the identical size. Using the long-channel MOS transistor model and ignoring the channel length modulation effect [68], the output current I_{out} can be expressed as

$$\begin{aligned} I_{out}(t) &= \frac{\beta}{2}(V_{gs0} - V_{thn})^2 + \frac{\beta}{2}(V_{gs0} - V_{thn} - \frac{I_{leak}}{C}t)^2 \\ &= \frac{2\beta(V_{gs0} - V_{thn})^2}{4}\left(1 + \left(1 - \frac{I_{leak}}{C(V_{gs0} - V_{thn})}t\right)^2\right) \end{aligned} \tag{3-6}$$

where β is the MOS transistor transconductance parameter, V_{gs0} (= $V_{gs1}(0)$ = $V_{gs2}(0)$) is the initial gate-source voltage of M_1 and M_2, and V_{thn} is the threshold voltage of NMOS transistors.

Comparing (3-5) and (3-6), to obtain the exponentially decaying current waveform, the following condition has to be satisfied:

$$\frac{I_{leak}}{C(V_{gs0} - V_{thn})} = \frac{1}{R_L C_L}. \tag{3-7}$$

the values of design parameters of the proposed circuit such as C, I_{leak} and β, V_{gs0}, can be determined to produce a desired exponential current waveform, resulting in a nearly constant V_e.

To maximize the power efficiency of the stimulator with a specific load, equation (3-7) should be satisfied. We set the value of capacitor C to be 2 pF and assume that the initial overdrive voltage (V_{gs0}-V_{thn}) of the transistor is 400 mV, and then the I_{leak} is

calculated as 800 pA when the default R_LC_L value (10K•100n Ω•F) is used. Practically, R_L and C_L have a wide range based on the electrode shape and implantation environment [31], [67], [9]. Besides, the initial overdrive voltage (V_{gs0}-V_{thn}) also changes due to process variation. Therefore, I_{leak} needs to be tunable to satisfy (3-7).

A current splitter structure [69] is used to generate I_{leak}. Controlled by an adjustable external current source *Is* (i.e. 200nA ~ 5μA), the current splitter can generate an output current ranging from 140 pA to 3.5 nA which can cover R_LC_L value from 2.3×10^{-4} Ω·F to 5.7×10^{-3} Ω·F. By tuning I_{leak} through the external current source I_S, (3-7) can be satisfied for the desired time constant ($R_L'C_L'$).

3.2 Implementation of Power-Efficient Stimulator with Exponentially Decaying Current

The proposed exponentially decaying current generator is integrated in a 16-channel stimulation system for proof of concept. The block diagram of the prototype stimulator with proposed exponentially decaying stimulation current is shown in Fig. 3.2. It consists of a global digital controller, a 6-bit DAC, and 16 stimulation channels. The stimulation channels can be selectively powered down to minimize the overall power consumption. Each channel consists of a current copier, an exponentially decaying current generator, a high-voltage current driver and an active charge-balancing circuit. The global digital controller is to receive and decode the commands. Especially, the 6-bit DAC is shared by 16 channels to save the total chip

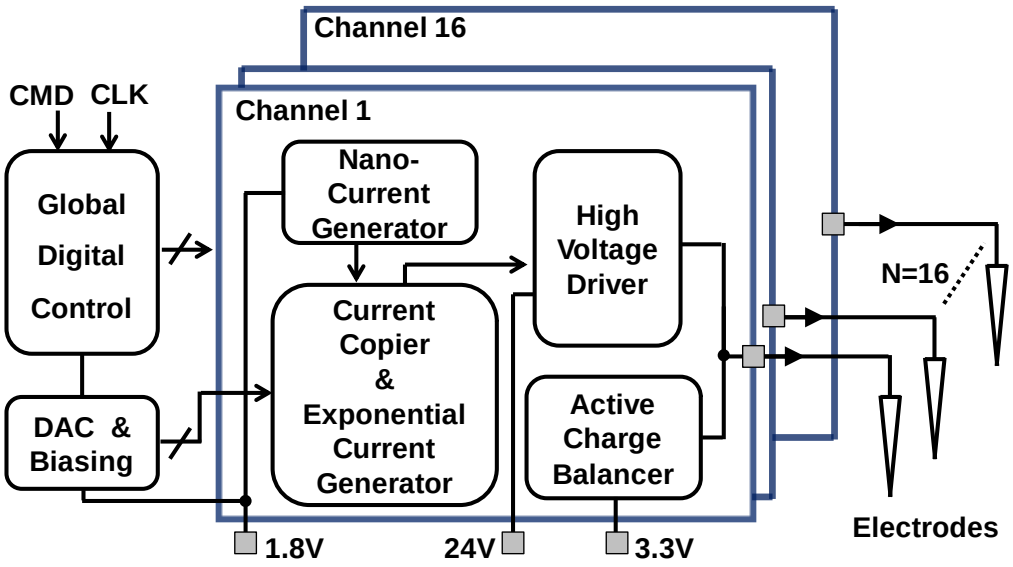


Figure 3.2. System archetecture of the 16-channel stimulator IC.

area and power and is controlled by the global digital block. The DAC sequentially generates current source for the current copier in each channel. The proposed exponentially decaying current generator provides the optimized stimulation waveform for high power efficiency. The generated biphasic exponentially decaying current is amplified and delivered to the stimulation site by a high-voltage current driver with nearly 24-V compliance. The active charge-balancing circuit removes the residual charge produced by the mismatched biphasic stimulation current using a pulse insertion technique [9].

3.2.1 DAC Design

DAC is needed in most neural/muscular stimulators to set the stimulation current. The output current of a stimulator is usually made selectable in a wide range so that it can be used for different applications. For example, a current larger than 500 μA may be needed to stimulate a muscle, while, a current less than 100 μA is large enough to

excite an AP in a nerve [19]. Therefore, a current-mode DAC is suitable for providing such stimulation source current since its output current can be easily controlled and programmed. In our design, to meet the general specifications of stimulator as mentioned in Chapter 1, a 6-bit DAC circuit whose output current ranges from 4 μA to 252 μA with a step current of 4 μA is designed. After going through a current copier circuit and a high-voltage output stage, the final output current of the stimulator will range from about 30 μA to 1.6 mA.

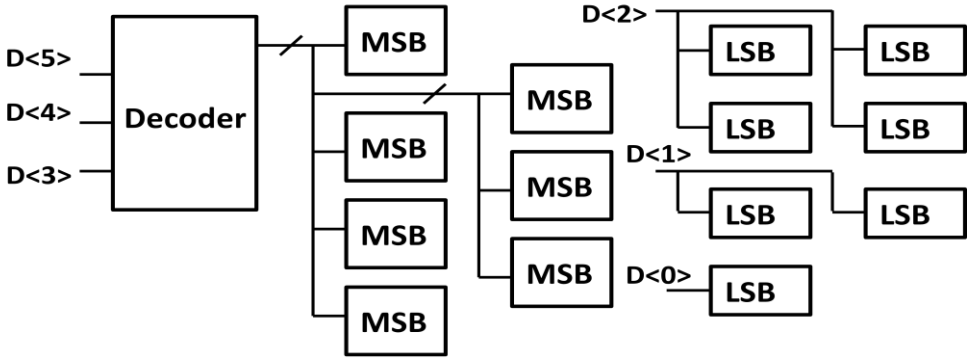
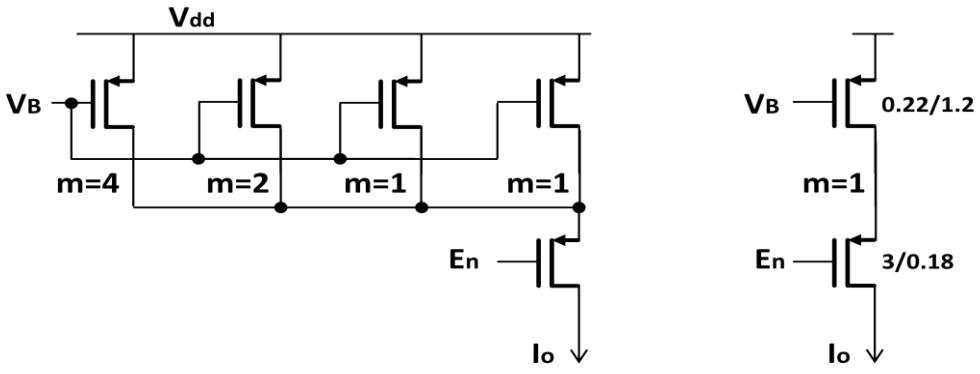


Figure 3.3 Architecture of DAC current cells.



(a) (b)

Figure 3.4 Schematic: (a) MSB current unit cell (b) LSB current unit cell.

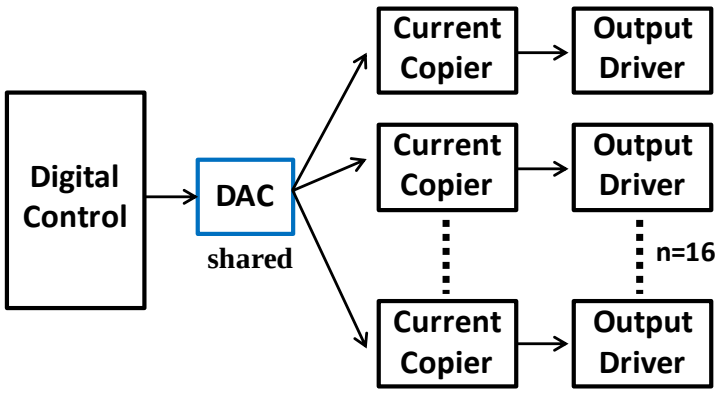
This 6 bit DAC circuit consists of a 3-to-7 thermometer decoder [70], 7 MSB current unit cells, and 7 LSB current unit cells, as shown in Fig. 3.3 and Fig. 3.4. These 7 LSB current unit cells are controlled by D<2:0> through direct switch control and the MSB unit cells are controlled by D<5:3> through the thermometer decoder. The output current of LSB and MSB unit cell are set to 4 μA and 32 μA, respectively.

3.2.2 Current Copier and Exponentially Decaying Current Generation Circuit

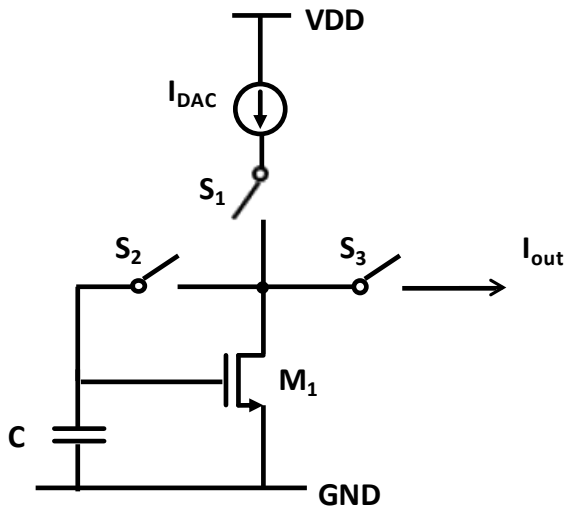
In traditional multi-channel stimulators, each channel is driven by a local DAC circuit so that the amplitude of stimulation current can be set differently from other channels. However, in some applications, such as retinal prosthesis, where large number of channels are needed, the local DACs will occupy large chip area and increase the overall power consumption. In this design, only one global DAC is used and shared among all 16 channels, as shown in Fig. 3.5(a). Current copying technique [71-72] is therefore adopted to enable the DAC sharing.

A simplified current copier circuit [73] is shown in Fig. 3.5(b). The current copier converts the current to the gate-source voltage and stored on the gate capacitance and capacitor C. During "pre-charging" state, S_1 and S_2 are closed, S_3 is open, the capacitor C is charged and gate-source voltage of transistor M_1 will be sampled. Then, S_2 will be open after pre-charging finishes, and V_{gs} of M_1 holds its value. During "stimulating" state, S_1 and S_2 are open, S_3 is closed, and the same amount of current

generated by M_1 will flow to the output stage.



(a)

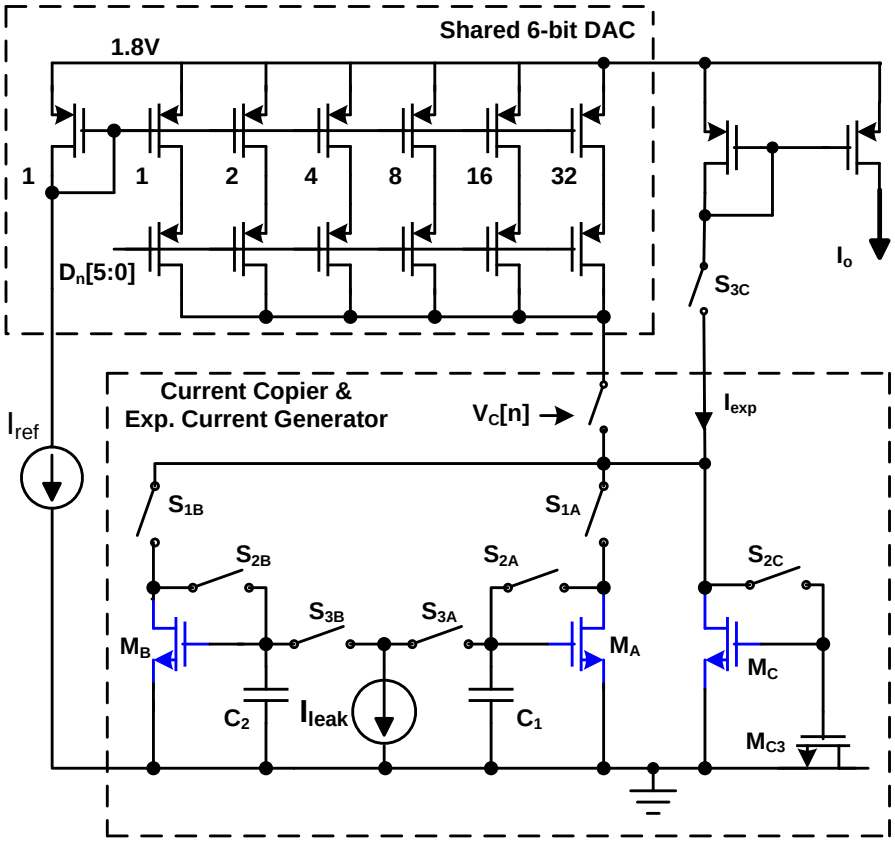


(b)

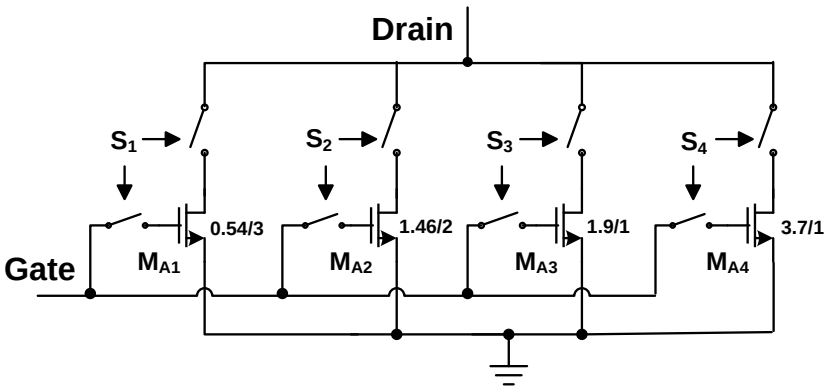
Figure 3.5 (a) DAC sharing in multichannel stimulator, (b) schematic of a simplified current copier circuit.

Noticed that both exponentially decaying current generator (shown in Fig. 3.1(c)) and current copier circuit (shown in Fig. 3.5) consist of transistors and capacitors and have similarity in structure, we combine these two functions together and make a new circuit featuring both current copying and exponential current generating as shown in

Fig. 3.6(a). In this combined current copier and exponentially decaying current generator, a switched transistor array M_C is used to generate the constant current term in equation (3-6) mentioned in section 3.1.2, and two identical transistor arrays M_A



(a)



(b)

Figure 3.6 (a) Schematic of the shared 6-bit DAC and the current copier/exponentially decaying current generator in single-channel, (b) switched transistor array M_A used in the current copier.

and M_B are used to generate the time-dependent current term in (3-6). To determine the value of capacitors and the amplitude of current sink (I_{leak}) in the circuit, (3-7) has to be satisfied to configure the design parameters. Consequently, assuming a constant initial overdrive voltage V_{gs0}-V_{thn} = 400mV, the values of I_{leak} and C (C_1 and C_2 in Fig. 3.6(a)) can be derived from the values of R_L and C_L. In the design, we set the value of C to be around 2 pF. For the capacitor implementation, since the M_{C3} is used to keep the gate-source voltage of M_C constant, the MOS capacitor is used to save the chip area due to its large capacitance density. For C_1 and C_2, MIM capacitors are used to provide constant capacitance for the varying voltage across the capacitors.

Practically, R_L and C_L have a wide range based on the electrode shape and implantation environment [31], [67], [9]. In the design, although we set a default value of I_{leak} to be 800 pA based on the typical load with R_L = 10 kΩ and C_L = 100 nF [67], for different loads, I_{leak} needs to be tuned to cover a wide range of R_L and C_L, to satisfy equation (3-7). The value of required I_{leak} according to different load conditions (R_LC_L) is presented in Fig. 3.7. The red curve shows the relationship between I_{leak} and 1/RC of the load when a large current (D=001111, 60 μA) is generated from the DAC. The black curve shows the simulation results when a small current (D=000111, 28 μA) is applied. This can be explained according to equation (3-7). Large current results in high overdrive voltage and hence a larger I_{leak} is needed in order to satisfy the condition in equation (3-7).The simulation results of the current copier and exponentially decaying circuit also reveals that the required I_{leak} has a

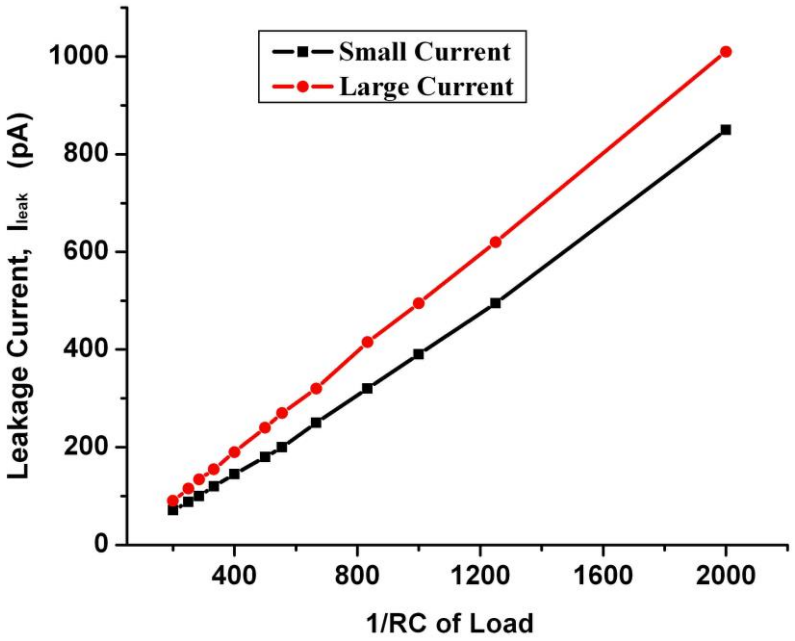


Figure 3.7 Simulation result of the required I_{leak} vs. diffent loads.

linear relationship with the reciprocal of time constant under the fixed load. In other words, the circuit can be easily tuned to fit different loads in different applications.

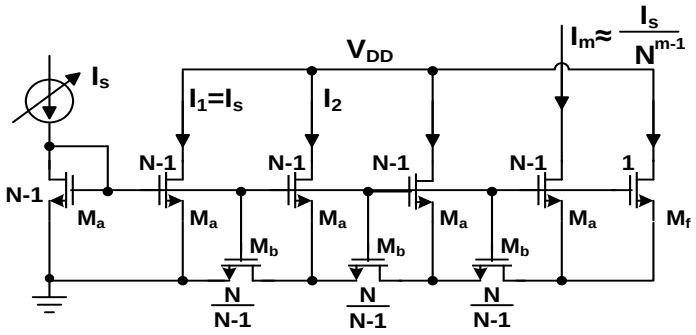


Figure 3.8 Ultra low current generator.

The schematic of current splitter [69] which generates I_{leak} is shown in Fig. 3.8. In this current splitter, the gate nodes of all transistors are connected together. In the 1st-order cell (the first branch generating current I_1), the current I_1 is equal to the reference

current I_s, and the current flowing through M_b is approximately N times smaller than I_1. In this design, N is set to 10 and a 4th-order current splitting is used to generate I_{leak} of several hundred picoamperes.

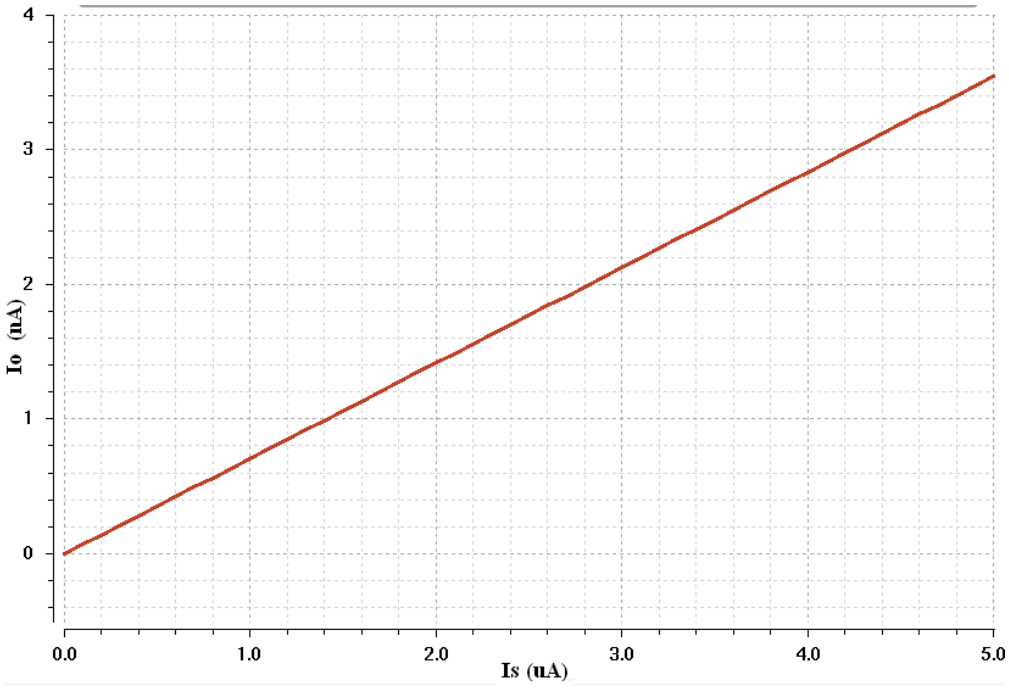
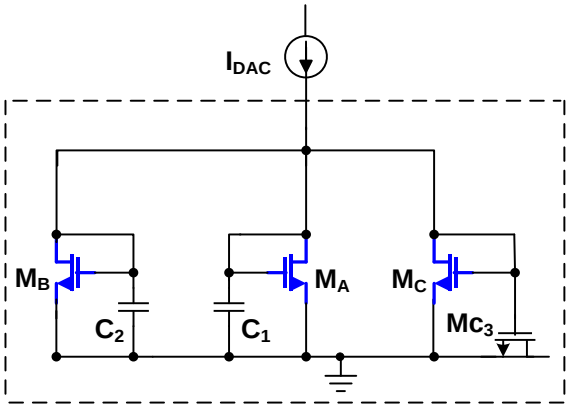


Figure 3.9 Simulation result: input current (I_S) vs output current (I_{leak}) of current splitter.

Fig. 3.9 shows the relation between input and output current of the current splitter. When the input current (*Is*) is tuned from 0 to 5 μA, the output current of the splitter ranges from 0 to 3.6 nA. The result shows good linearity which guarantees the tuning ability of the exponentially-decaying current stimulator.

The current copier and exponentially decaying current generation circuit operates in three phases. First, in the current-replication phase, the control signal from the global digital controller connects the circuit to the DAC output. The switches S_{1A}, S_{2A}, S_{1B},



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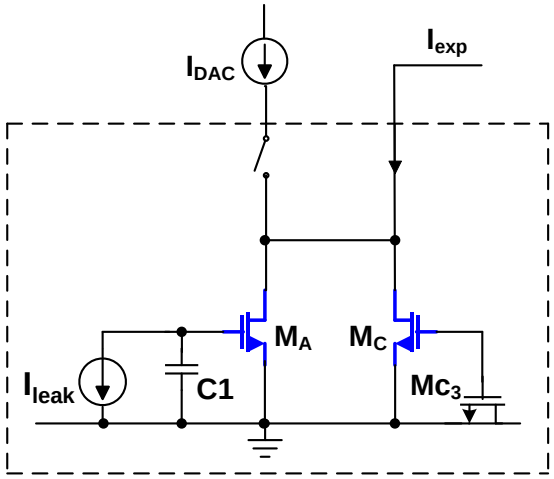

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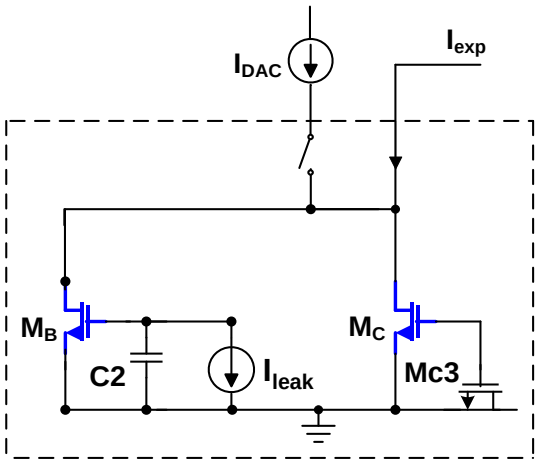


(c)

Figure 3.10 Operation of the current copier and exponentially decaying current generator circuit: (a) current-replication phase, (b) cathodic stimulation phase, and (c) anodic stimulation phase.

S_{2B} and S_{2C} in Fig. 3.6(a) are closed so that the DAC output current I_{DAC} can flow into transistor arrays M_A, M_B and M_C, as shown in Fig. 3.10(a). Since these three transistor arrays have the same size, they conduct the same amount of current (I_{DAC}/3) through each and the same gate-source voltages are stored in the capacitors C_1, C_2 and M_{C3}, respectively. As the cathodic stimulation phase starts, the circuit is disconnected from the DAC output and operates with the gate-source voltages stored in the capacitors. Since the current flowing through M_A and M_C forms the exponentially decaying current I_{exp} in the cathodic stimulation phase, the switches S_{1A} and S_{3A} are closed while all the other switches are open, as shown in Fig. 3.10(b). Similarly, during the anodic stimulation phase shown in Fig. 3.10(c), the circuit remains disconnected from the DAC output, and I_{exp} is generated from M_B and M_C using the gate-source voltages stored in C_2 and M_{C3} with S_{1B} and S_{3B} closed.

To support variable strengths of stimulation, the DAC generates I_{DAC} which varies over the range from 4 μA to 252 μA. Therefore, the initial overdrive voltage ($V_{gs0} - V_{thn}$) of the transistors in current copier cells also varies with the current, which requires I_{leak} to be tuned accordingly. To reduce its required tuning range, the switched transistor arrays M_A, M_B and M_C are implemented in the circuit shown in Fig. 3.6(b) to maintain the initial overdrive voltage relatively constant over the range of I_{DAC}.

The switches S_1, S_2, S_3 and S_4 in Fig. 3.6(b) are controlled using the logic shown in Table 3.1. For the n^{th} stimulation channel, as the 6-bit DAC input code D_n[5:0]

TABLE 3.1
SWITCHED TRANSISTOR ARRAY CONTROL LOGIC

D_n[5:0]	I_{DAC}	S_1	S_2	S_3	S_4
$0 \le D_n \le 4$	$0 \le I_{DAC} \le 16$ μA	1	0	0	0
$5 \le D_n \le 16$	20 μA $\le I_{DAC} \le$ 64 μA	0	1	0	0
$17 \le D_n \le 36$	68 μA $\le I_{DAC} \le$ 144 μA	0	0	1	0
$37 \le D_n \le 63$	148 μA $\le I_{DAC} \le$ 252 μA	0	0	0	1

becomes larger, the DAC output current I_{DAC} increases and the larger transistor in the array is chosen. In order to avoid taking up too much extra area and simplify the design of transistor array as well as its control circuit, only 4 transistors are used in each array. The entire I_{DAC} range is divided into 4 regions responding to these 4 transistors. For different regions, different transistors are activated. The transistors are sized proportional to the average I_{DAC} values in the corresponding regions. By doing so, the initial overdrive voltage ($V_{gs0} - V_{thn}$) of the transistors can be kept within the range from 300 mV to 460 mV, as shown in Fig. 3.11. While it ranges from 100 mV

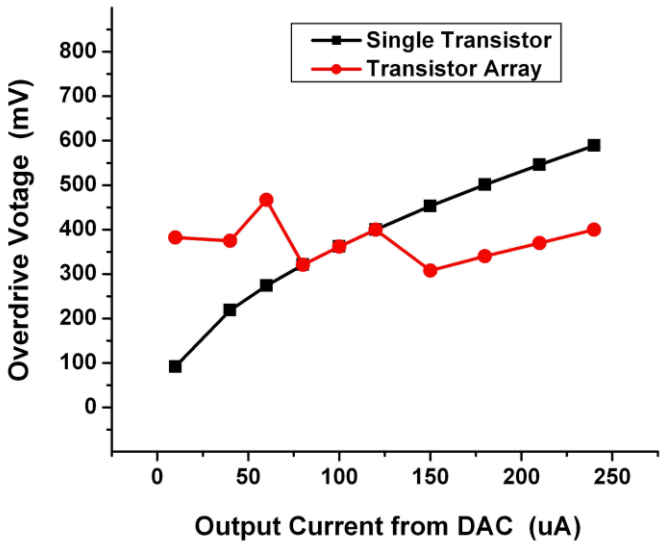


Figure 3.11 Simulation result: overdrive voltage vs. current.

to 600 mV if single transistor is used. With the transistor array, the full swing of the tunable I_{leak} can be reduced by nearly 75% and thus improves the tunability.

3.2.3 High-Voltage Output Stage and Active Charge Balancing Circuit

Output stage of the stimulator amplifies the stimulation current and provides large voltage compliance in order to deliver sufficient current to the high impedance load. In order to provide sufficient stimulation strength even when the load impedance is high, output stage is designed in a 0.18-μm 24-V high-voltage CMOS process. The

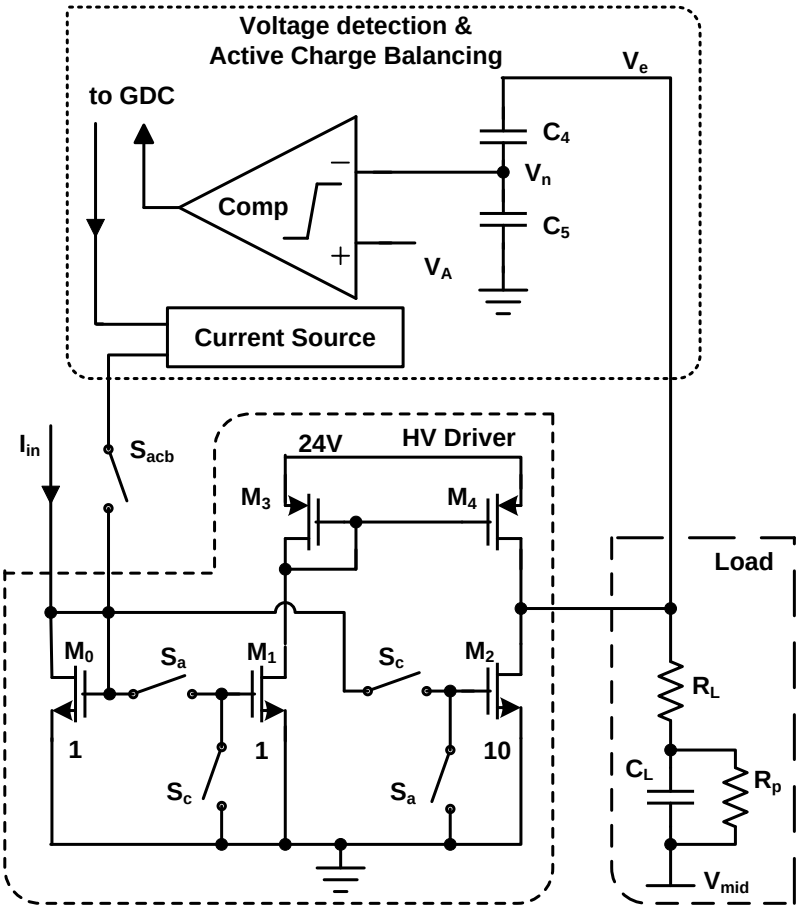


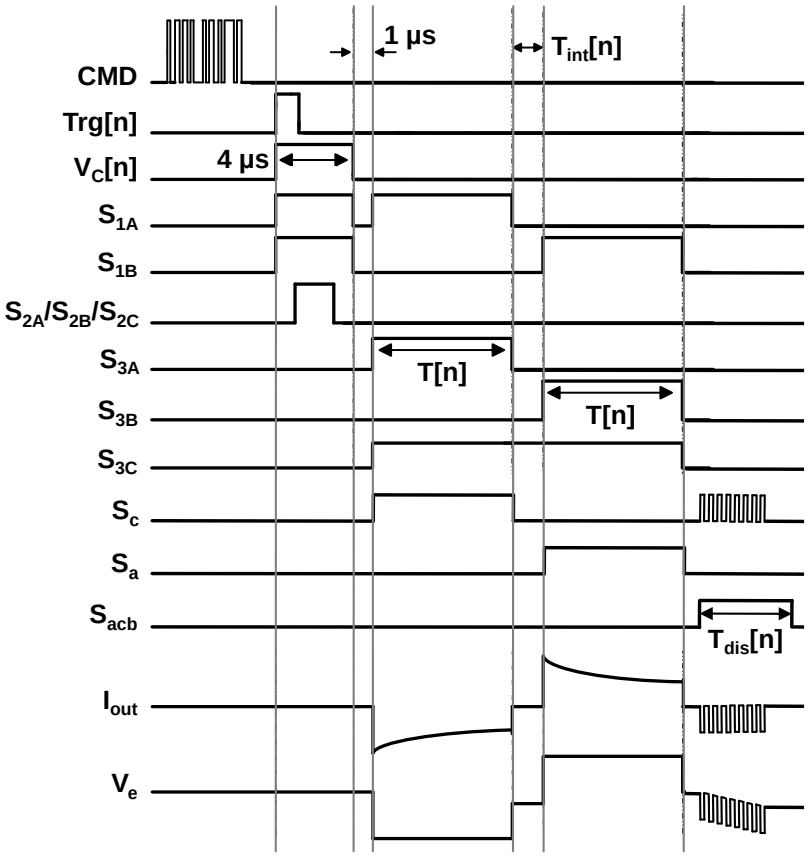
Figure 3.12 High-voltage output stage and active charge balancing circuit.

high-voltage output driver transforms the monophasic current to the biphasic current for cathodic and anodic stimulations. As shown in Fig. 3.12, the current mirror composed of M_0 and M_2 forms the anodic stimulation path, and the cathodic stimulation path consists of two pairs of current mirrors (M_0-M_1 pair and M_3-M_4 pair). Since M_0-M_2 and M_3-M_4 pairs mirror the current with the ratio of 1:10, nearly 90% of current is consumed in the final load-driving branch.

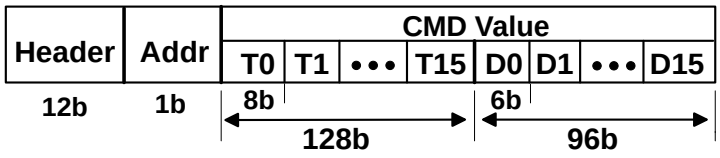
An active charge-balancing circuit (ACB) is added to remove the residual charge using the pulse insertion technique in [9]. First, before each stimulation cycle, electrode voltage (*Ve*) equals to the reference voltage (V_{mid}), and the node voltage between capacitor C_4 and C_5 (V_n) is initially set equal to V_A. After each stimulation, the electrode potential (*Ve*) is sampled by a capacitive voltage divider and compared with V_A by a comparator. If $V_n > V_A$ ($Ve > V_{mid}$), GDC will send a short pulse to close switches S_{acb} and S_c, delivering a sink current to absorb the excessive residual charge on the electrode. ACB keeps inserting pulses until V_n is slightly smaller than V_A. If $V_n < V_A$ ($Ve < V_{mid}$), in the similar way, the stimulator will deliver an anodic current pulse, until finally the voltage on the electrode is kept within a safety level (V_{mid} ±50mV).

3.2.4 Global Digital Controller

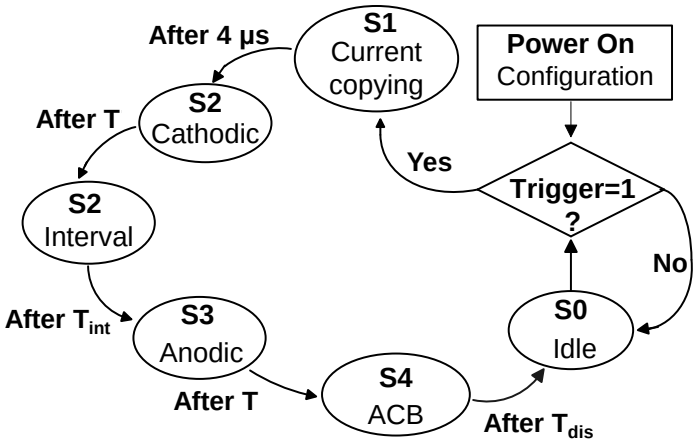
The global digital controller (GDC) provides the control signals of switches between the shared DAC and 16 stimulation channels as well as the switches in the current



(a)



(b)



(c)

Figure 3.13 System operation: (a) digital control timing diagram, (b) command frame format, and (c) control state diagram.

copier, exponentially decaying current generator, active charge balancer, and high-voltage output driver for each channel.

The timing diagram of control signals used for system operation is shown in Fig. 3.13(a). Firstly, the stimulation parameters such as $T[n]$, $T_{dis}[n]$ and $D_n[5:0]$ for all 16 channels are set by decoding the incoming commands to configure the stimulation duration and amplitude of each channel. The command frame format is shown in Fig. 3.13(b). When the n^{th} channel is triggered, the digital code presenting the current amplitude of the selected channel goes to the DAC input through a multiplexer. $V_C[n]$ is set to logic 1 to connect the channel with the DAC output and the switches are configured to operate the channel in the current-replication phase for 4 μs. The cathodic stimulation phase then begins 1 μs after $V_C[n]$ goes back to logic 0. By using the initial gate-source voltages stored during the current-replication phase, the transistor arrays M_A and M_C (in Fig. 3.6(a)) generate the exponentially decaying stimulation current during $T[n]$. After delivering the cathodic stimulation current, there is an interphasic delay of 30 μs before the anodic phase starts. In the anodic stimulation phase, the exponentially decaying current generated by M_B and M_C is steered into the high-voltage driver. The active charge balancing operation is initiated after the anodic stimulation phase and sustained for $T_{dis}[n]$. For multi-channel operation, as it takes 4 μs for the selected channel to copy its current from the DAC output, the multi-channel triggering signals should come in with a minimum interval of 4 μs.

The GDC module is designed by a staff member of Institute of Microelectronics (IME) Singapore as part of the collaboration and the detail digital implementation is reported in [74].

3.3 Measurement Results

The prototype stimulator with exponentially decaying stimulation current is fabricated in a 0.18-μm CMOS technology with 24-V high-voltage LDMOS option. The core area is 1.65 mm × 1.65 mm and the total die area including pads is 2.5 mm × 2.5 mm. The microphotograph of the fabricated stimulator IC is shown in Fig. 3.14.

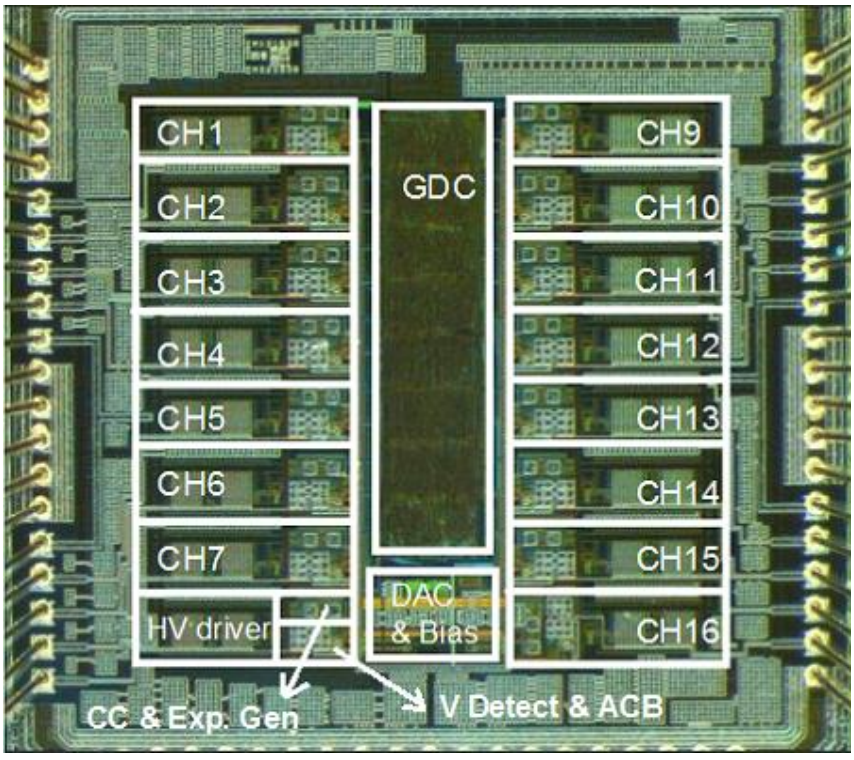
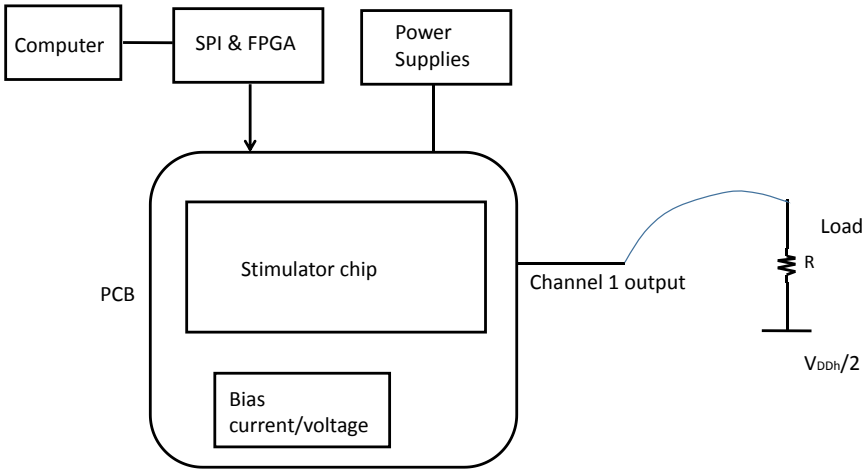


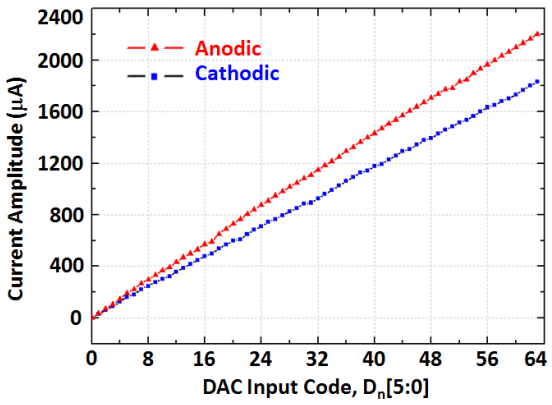
Figure 3.14 Die microphotograph of 16-channel stimulator IC.

3.3.1 Test Bench Measurement Results

As the DAC input code increases from 1 to 63, the measured cathodic stimulation current ranges from 28 μA to 1.8 mA while the anodic current changes from 34 μA to 2.2 mA, as shown in Fig. 3.15. The mismatch of cathodic and anodic current is



(a)



(b)

Figure 3.15 (a) Measurement setup. (b) Cathodic and anodic stimulation current measured with varying the DAC input code.

attributed to the channel length modulation effect of high-voltage transistors in the high-voltage output stage. The current matching would be better if a cascode structure is used for current sources in the high-voltage driver design, however both chip area

and voltage headroom would be increased at the output branch which leads to a small degradation of power efficiency.

Figure 3.16 (a)-(c) compare the constant-current stimulation and exponential-current stimulation in terms of measured stimulation current and electrode voltage waveforms. Figure 3.16(d) shows the measured power efficiency (PE) v.s. stimulation current. In the measurement, three electrode models with different R_L and C_L are used:

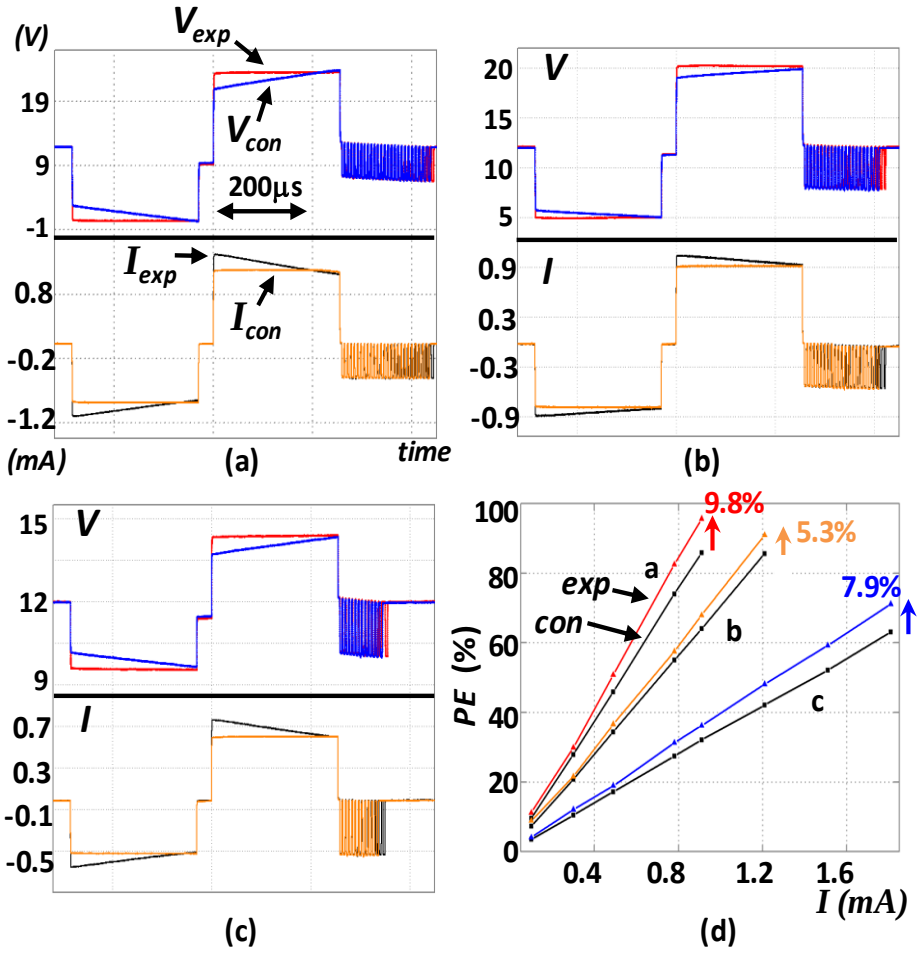


Figure 3.16 Measured waveforms of the stimulation currents and electrode voltages: (a) R_L = 10 kΩ and C_L = 100 nF load impedance, (b) R_L = 8 kΩ and C_L = 300 nF load impedance, (c) R_L = 3.7 kΩ and C_L = 240 nF load impedance, and (d) power efficiency v.s. stimulation current at the output stage.

10-kΩ resistor and 100-nF capacitor (default value) for typical electrode impedance [67], 3.7-kΩ resistor and 240-nF capacitor electrode [9] and 8-kΩ resistor and 300-nF capacitor electrode [31]. The constant-current stimulation can be carried out by disabling the exponentially decaying current generator. For all three electrodes models, the constant current stimulation shows a voltage headroom which lowers the power efficiency. In the case of the exponentially decaying current stimulation, the electrode voltage is almost constant during stimulation after tuning the external current source to fit actual loads. The power efficiency of output stage, shown in Fig. 3.16(d), is calculated by integrating (3-1) over the cathodic and anodic phase, respectively, and taking the average value, using the measured electrode voltage waveforms. For default electrode impedance, the maximum power efficiency of 95.9% is achieved at 910 μA stimulation current, which is 10% improvement from 85.9% efficiency of the constant-current stimulation. For the other two electrode models, as shown in plot b and c in Fig. 3.16(d), a PE improvement of 5.3% and 7.9% is achieved, respectively. It also suggests that the power-efficiency improvement is larger at larger stimulation current. The maximum power efficiency is only limited by the headroom voltage of PMOS and NMOS on the output stage. Considering the power consumption of the entire system (including GDC, DAC, etc), the overall stimulation power efficiency is 87.8% using default electrode model. This overall power efficiency can be further improved by design optimization of other function blocks (GDC, biasing, etc).

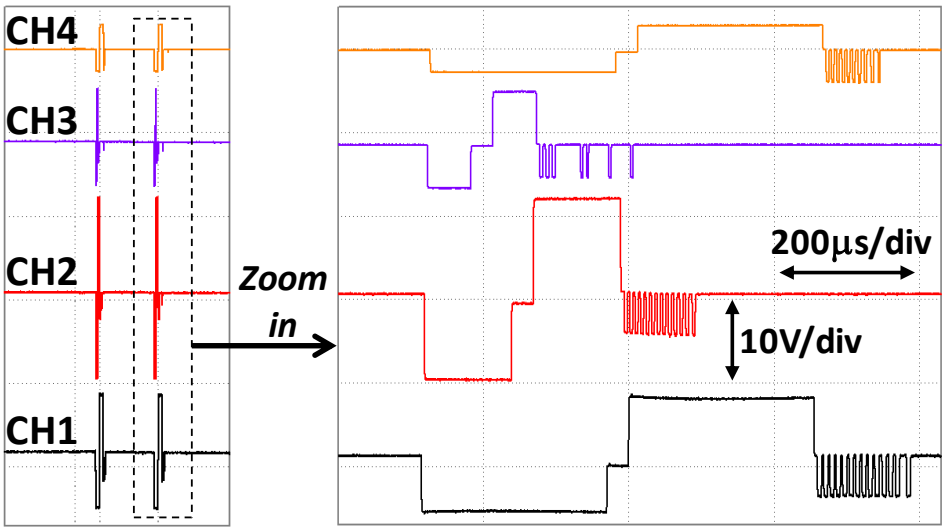


Figure 3.17 Measured multi-channel stimulation waveforms (zoomed-in plot on the right): electrode voltage waveforms captured from the first 4 channels.

TABLE 3.2
PARAMETERS USED IN MULTI-CHANNEL STIMULATION TEST

Channel	D_n[5:0]	I_{DAC}	$T[n]$
1	20	80 µA	255 µs
2	35	140 µA	120 µs
3	20	80 µA	60 µs
4	10	40 µA	255 µs

Figure 3.17 shows the electrode voltage waveforms measured during multi-channel stimulation. Channel 1 and channel 2 are connected with a 10-kΩ resistor and a 100-nF capacitor in series as the load impedance, while channel 3 and channel 4 are connected with a 8-kΩ resistor and a 300-nF in series as the load impedance. The waveforms are captured from 4 channels configured with different stimulation parameter values (amplitude and duration). The parameter values used for all these 4 channels are summarized in Table 3.2. The zoomed-in electrode voltage waveforms

are shown on the right. The negative pulses after the anodic phase are for charge balancing. I_s is tuned to 1.2 μA for channel 1, 1.3μA for channel 2, 0.5 μA for both channel 3 and channel 4. I_s is slightly different for the same R_L and C_L due to the different V_{gs}-V_{thn} caused by different stimulation currents. The measured result indicates that the DAC can be shared among multiple channels with the current-replication technique while facing different load impedance and setting stimulation parameters of each channel independently with different values.

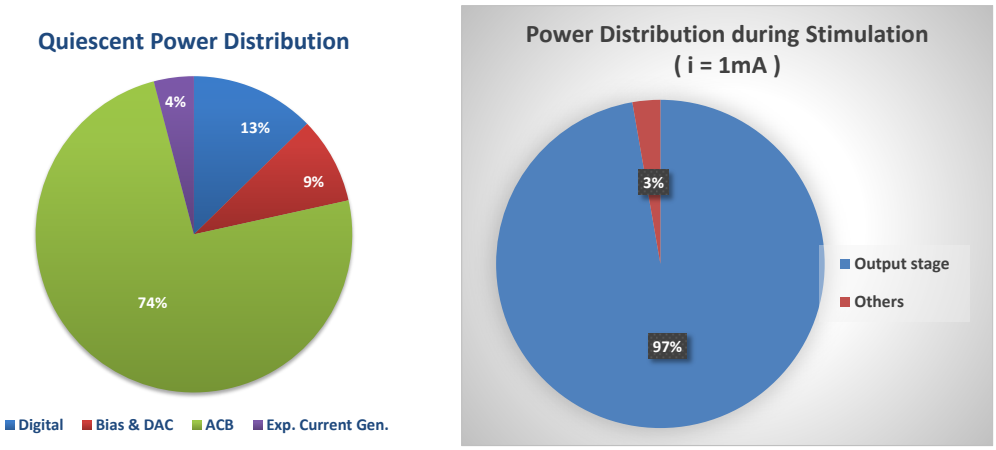
The overall performances and comparison are summarized in Table 3.3. The measured total quiescent power is about 720 μW for 16 channels. Digital circuit takes 50 μA. For quiescent power consumption distribution, DAC and biasing consume 35 μA

TABLE 3.3
PERFORMANCE COMPARISON OF CURRENT-MODE STIMULATORS

Parameter	**[33]**	**[39]**	**[14]**	**This work**
Process	0.18 μm CMOS	0.18 μm CMOS	0.5 μm CMOS	0.18 μm CMOS
Number of channels	8	1	4	16
Core area	5.4 mm^2	N.A.	2.25 mm^{2*}	2.72 mm^2
Stimulation Current waveform	constant	constant	constant	exp.
Max. stimulation duration	N.A.	200 μs	512 μs	255 μs
Max. current amplitude	500 μA	1 mA	2.5 mA	1.8 mA
Max. voltage compliance	11.5 V	3 V	4.6 V	11.5 V
Quiescent power consumption (per channel)	23 μW	53 μW	N.A.	45 μW
Max. PE of output stage (Eq. 1)	83.3%**	***	68%	95.9%

*including pads, **calculated on simulation result in an ideal case, *** PE depends on the ripple amplitude.

under 1.8-V supply, active charge balancer consumes 160 μA under 3.3-V supply, and exponentially decaying current generator consumes 16 μA under 1.8-V supply. Fig. 3.18 shows the power distribution. During stimulation, output stages consume most power due to its 24-V supply. It suggests the most effective way to further improve power efficiency is increasing the current mirror ratio at the output stage. In future design, enabling switches can be added in active charge balancing circuit to shut down the amplifiers and decrease the quiescent power consumption.



(a) (b)

Fig. 3.18 Distribution of (a) quiescent power consumption and (b) power consumption in the stimulation phase.

3.3.2 In-Vitro Measurement Results

To verify the proposed method with real electrodes, an *in-vitro* experiment has been conducted using the 16-channel neural/muscular stimulator developed in this work. In the *in-vitro* experiment, phosphate buffered saline (PBS, 1x, pH=7.4, NaCl concentration: 8.0g/L) solution is used to emulate the tissue environment. Cuff

electrodes [75] and concentric bipolar electrodes (SNE-100, 10 mm) [76] are connected with the stimulator IC to deliver the stimulation current into PBS. The stimulation current levels are randomly selected from 100 μA to 1.6 mA. The voltage waveforms on the cuff electrode and concentric bipolar electrode are captured for further analysis and calculation.

Figure 3.19 shows the measured voltage waveforms on the cuff electrode with the constant stimulation current and exponentially decaying stimulation current, respectively. The constant current is set at 278 μA (D=001001). In Fig. 3.19, I_s is manually tuned to 4.6 μA for exponential stimulation current to optimize power

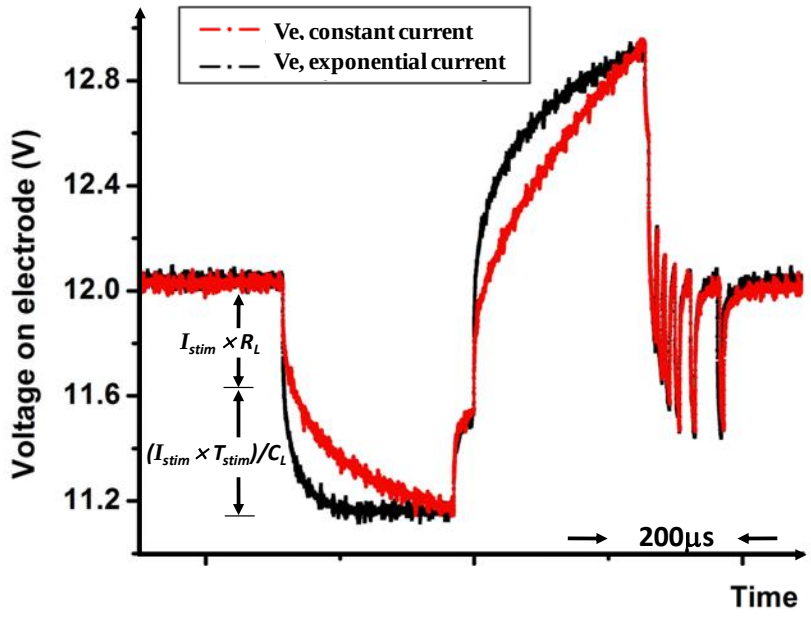


Figure 3.19 Voltage waveforms measured with the cuff electrode when the constant current stimulation and proposed exponentially decaying current stimulation are applied, respectively.

efficiency. The same experiment is done with the concentric bipolar electrode and the results are shown in Fig. 3.20 (I_{stim} = 418 μA, I_s = 1.8 μA). The results show that the exponentially decaying current stimulator reduces the headroom in conventional stimulator for both cuff electrode and concentric bipolar electrode. It's also noticed that the voltage swing on the two electrodes are only 0.9 V and 5 V, respectively, due to either the small stimulation current or the low impedance of the electrodes, which results in low power efficiency even with the exponentially decaying stimulation

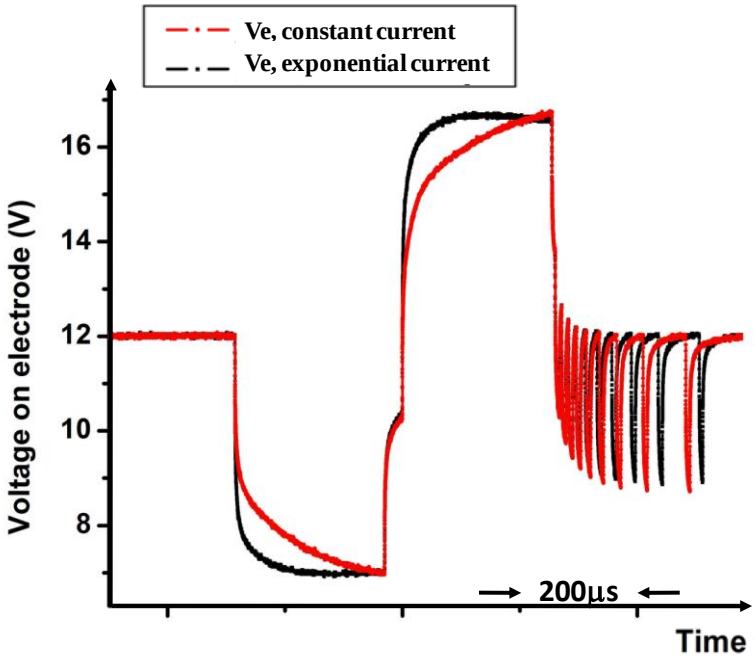


Figure 3.20 Voltage waveforms measured with the concentric bipolar electrode when the constant current stimulation and proposed exponentially decaying current stimulation are applied, respectively.

current. This problem happens in low-impedance applications and can be solved by either using smaller power supply voltage and reference voltage (lower V_{DD} and V_{mid}) or combining with supply adaptation technique (introduced in Chapter 2, Fig. 2.2). If supply adaptation technique is also integrated in this stimulator and thus only a 0.5-V

headroom is remained, the power efficiency would be improved from 42% to 53% for the cuff electrode and from 76% to 87% for the concentric bipolar electrode, respectively (the power efficiencies are calculated by integrating (3-1) over the stimulation duration using the measured electrode voltage waveforms, assuming a 0.5-V constant headroom is remained). The non-ideality of the voltage waveforms (V_e is not completely constant) is caused by the simplified first-order RC model for the electrode-electrolyte interface. We also noticed that V_e is not constant during anodic stimulation phase when cuff electrode is used (in Fig. 3.19) because electrode-electrolyte impedance is different in cathodic phase and anodic phase during stimulation and a larger I_{leak} should have been applied to fit the smaller $R_L'C_L'$ in anodic phase.

3.3.3 In-Vivo Measurement Results

To test the proposed method in practical use with real electrode [77] and in a biological environment, an animal experiment has been conducted using the prototype 16-channel neural/muscular stimulator. Figure 3.21 shows the *in-vivo* experiment setup. The stimulator chip is soldered on a printed circuit board (PCB) and the power supply provides 24 V to the PCB. The laptop and FPGA are used to program stimulation parameters by sending the commands to the stimulator IC. Concentric bipolar needle electrodes [77] are inserted into the right leg muscle of the anesthetized rat. When the stimulation is triggered, the voltage waveforms on the electrodes are

captured by the oscilloscope.

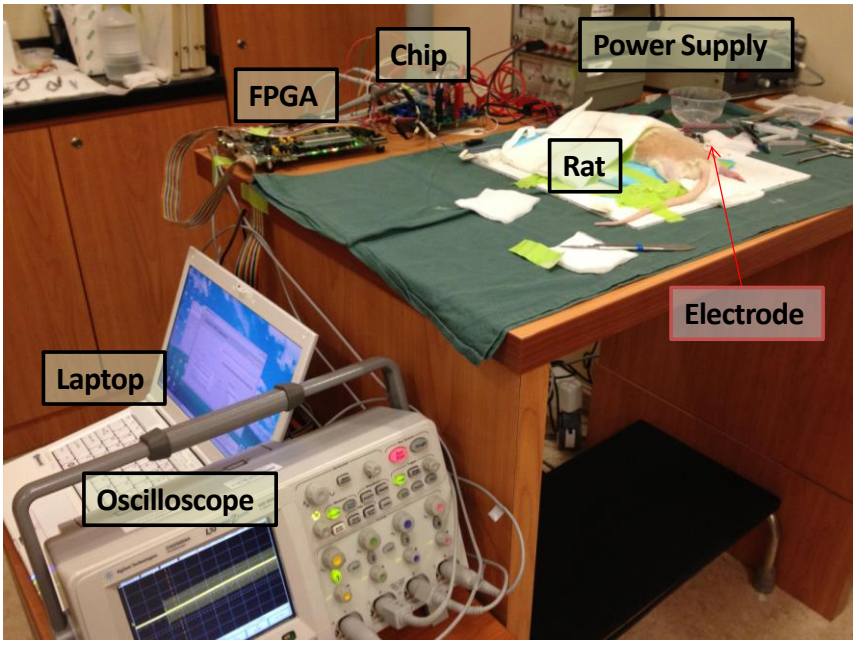


Figure 3.21 In vivo experiment setup using a rat animal model.

Muscle contraction is successfully observed using both constant stimulation current and exponentially decaying current. Fig. 3.22(a) and (b) show the measured voltage waveforms on the electrode with exponentially decaying current and constant current, respectively. The current is set around 900 μA in Fig. 3.22(a), while the I_s is manually tuned to 4.5 μA for the exponentially decaying current waveform in Fig. 3.22(b). The power efficiency of the output stage is calculated to be 72.5% for the constant-current stimulation and 80.5% for the exponentially-decaying current stimulation, respectively. The Power efficiency improvement of 8% is achieved at the output stage, which agrees well with the bench-top testing result. The lower power efficiency compared with the bench top measurement is due to a headroom voltage of about 2 V

(equivalent to the rectangular area in Fig. 2.2) observed in the in-vivo experiment,

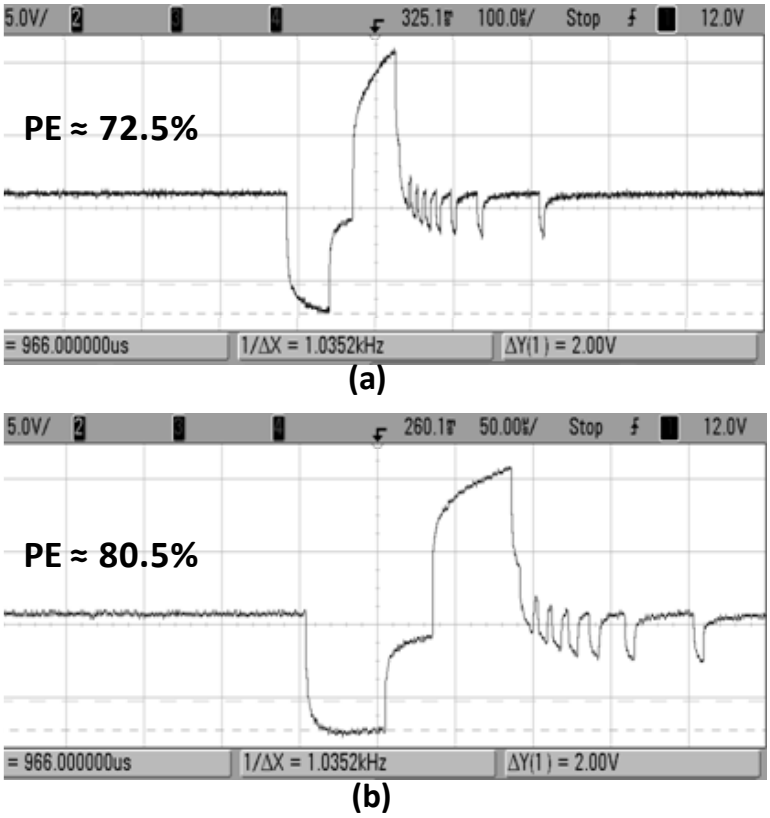


Figure 3.22. Electrode voltage waveforms measured in the in-vivo experiment: measured waveform (a) when the constant current and (b) when the exponentially decaying current is used for simulation.

which degrades the power efficiency. This can be avoided by either lower the supply voltage or employ the supply adaptation technique, mentioned in Section I, to remove the headroom. In the anodic phase, it is observed that the electrode voltage is not ideally flat. This is probably due to the polarization of the electrode-tissue interface, resulting in different load impedance for different stimulation phases. This problem could be solved by setting different I_{leak} values in the cathodic and anodic phases in the future design. In this work, I_s is manually adjusted to fit different loads. In future work, on-chip automatic calibration of I_s is also possible through an impedance

measurement circuit, similar to those in [78-79], or by monitoring the voltage on the electrode.

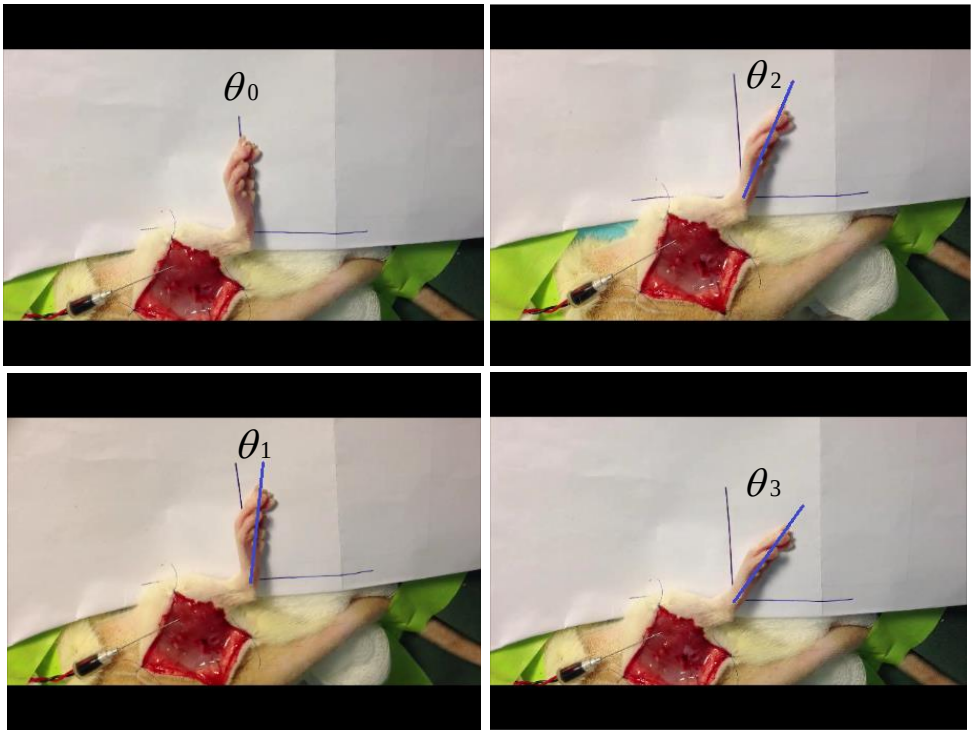


Fig. 3.23 Foot movement vs. stimulation current: the stimulation current level is set to d=0, d=10, d=20, and d=40, respectively (from 0 to 1.1 mA).

Fig. 3.23 shows the foot response according to different stimulation current levels. It can be seen from the figure that the larger the stimulation current used, the larger root dorsiflexion is achieved.

3.4 Summary

An exponentially decaying current stimulator has been proposed to further eliminate the headroom in conventional stimulator and improve the power efficiency. The

proposed concept has been demonstrated in a 16-ch neural/muscular stimulator IC. The DAC is shared by 16 channels to save the chip area. The measurement result with different loads has shown a maximum power efficiency improvement of nearly 10% at the output stage compared to traditional constant-current stimulator and the maximum power efficiency of output stage is 95.9%. The measurement results also suggest that power efficiency improvement increases with electrode with large impedance and under high stimulation current.

The stimulator IC has been tested *in-vivo* using an anesthetized rat. When the initial stimulation current amplitude of the exponentially decaying current stimulator is set larger than 267 μA, the desired muscle contraction is observed. The active charge-balancing circuit ensures to maintain the electrode voltage within ±50 mV with respect to the reference voltage. The stimulator IC can be used for multi-channel neural/muscular stimulation.

CHAPTER 4

DESIGN OF NEURAL/MUSCULAR STIMULATOR FOR ARTIFACT CANCELLATION

In this chapter, we propose an artifact cancellation technique with a tri-polar electrode using referenced and tuned push-pull stimulation (RTPPS) scheme to suppress the artifact with no blanking of the recording channels is required. The RTPPS uses a tri-polar stimulation configuration with two working electrodes and one reference electrode. The stimulation currents delivered by two working electrodes are complementary to each other. By doing so, the impact of large stimulation voltage fluctuation propagated to the recording site can be significantly reduced. The proposed concept is demonstrated with a prototype system integrating four recording channels and four stimulation channels, in both in-vitro and in-vivo experiments.

4.1 Proposed RTPPS for Artifact Cancellation

The proposed RTPPS scheme aims to cancel the artifact at the stimulation site so that the artifact will not affect the recording site. In conventional bipolar stimulation configuration, the biphasic current (cathodic-then-anodic) flows from a working electrode to a reference electrode. As a result, the stimulation current causes a voltage change at the interface of the working electrodes. This voltage signal is coupled to the input of recording front end (RFE) through tissue and causes artifact. In our proposed

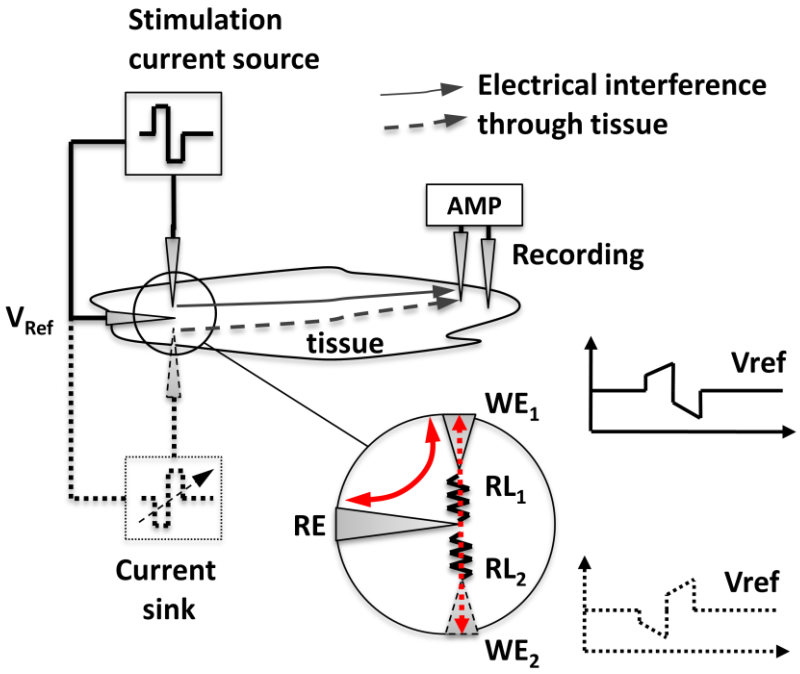


Figure 4.1 The proposed artifact-suppressed stimulator.

stimulator, as shown in Fig. 4.1, an additional working electrode (WE2) is introduced, which carries the stimulation current out of phase with the working electrode WE1. A reference electrode (RE) is placed in the middle of the two working electrodes. This forms a tri-polar electrode. Under this configuration, WE2 counteracts the stimulation from WE1 and thus cancels the coupling from the stimulation site to the input of the RFE. Hence the artifact can be removed. In ideal case, the voltage at the reference electrode is constant. The stimulation currents for WE1 and WE2 are generated by two current generators, namely, the stimulation current generator (SCG) and the counter current generator (CCG). Considering the impedance asymmetry of the two working electrodes, the CCG is designed to be tunable. The proposed RTPPS eliminates the voltage fluctuation on the stimulation site and hence reduces the stimulation induced artifact.

4.2 4-Channel Neural Recording and Stimulation System Implementation

To verify the proposed concept, a 4-channel neural recording/stimulation system is designed. Fig. 4.2 shows the system block diagram. The system consists of four-channel RFEs, four action potential detectors (APD), digital logic control, power down (PD) control, biasing circuit and four high-voltage artifact-suppressed stimulators (HVAS). The system can be configured either for multi-channel neural recording applications using RFE channels or multi-channel neural/neuromuscular stimulation using HVAS channels. With both RFE and HVAS channels active, the system can be configured in four modes: recording (REC), stimulation (STIM),

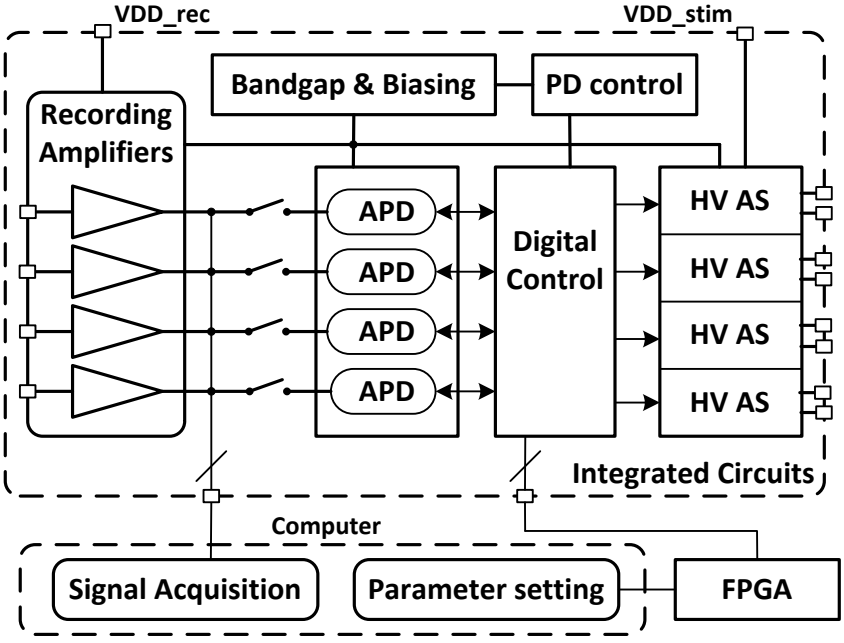


Figure 4.2 System block diagram of 4-channel neural recording/stimulation system.

closed-loop recording-stimulation (REC-STIM) and stimulation-recording (STIM-REC). In REC and STIM mode, the system only performs neural signal recording and electrical stimulation, respectively. In REC-STIM mode, the system performs neural signal recording, action potential detection, and action potential triggered stimulation. In STIM-REC mode, the stimulator generates stimulation pulses for the specific muscles or neurons, while the RFE is used to monitor stimulation invoked neural signals. In all stimulation related modes, passive charge balancing (PCB) circuit is used to remove the residual charge after each stimulation pulse to prevent tissue damage.

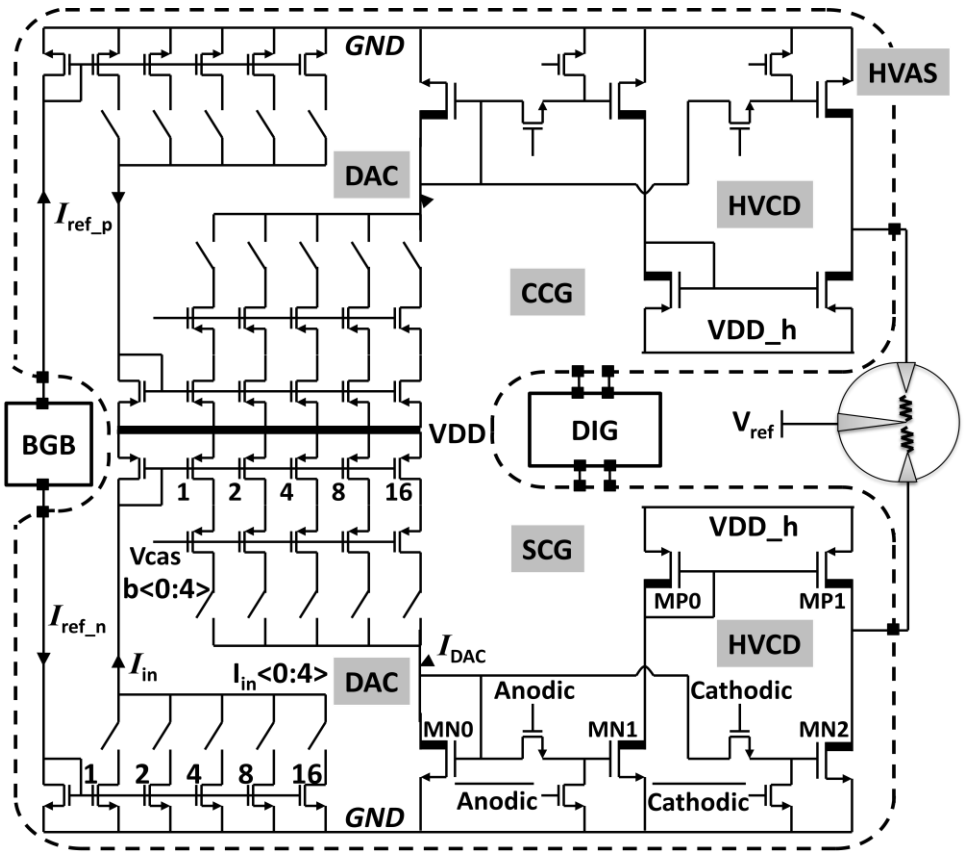


Figure 4.3 Schematic of HVAS (in each channel) .

4.2.1 High-Voltage Artifact-Suppressed Stimulator

Fig. 4.3 shows the circuit schematic of one stimulator channel, which includes two 10-bit digital-to-analog convertors (DACs) and two high-voltage current drivers (HVCD). The bottom DAC and HVCD forms stimulation current generator (SCG), while the upper DAC and HVCD constitutes counter current generator (CCG). During the stimulation, both SCG and CCG output biphasic currents to the stimulation target, but are out of phase. The stimulation current amplitude is set by programming I_{in}*<0:4>* and *b<0:4>* of DAC blocks. The stimulation pulse duration is determined by the timing control of *cathodic* and *anodic* in high-voltage current driver blocks. To reduce the chip power consumption, the DAC is powered by 1.8-V supply, and the high-voltage current driver is powered by 24 V. The output voltage compliance is therefore about 22 V to deliver sufficient stimulation current. The reference voltage is set to a half *VDD_h*. The current amplitudes of both SCG and CCG are set by DACs and controlled by digital blocks. In practice, considering the asymmetries of two working electrodes WE1 and WE2 with respect to RE and two electrode-tissue interfaces, the current amplitude of CCG is made tunable to compensate any mismatch between the two electrode interfaces.

4.2.2 Recording Front End and Action Potential Detector

The RFE, shown in Fig. 4.4, consists of a neural amplifier, a band pass filter (BPF), and a buffer. RFE has a programmable gain of 54/60 dB. The high- and low-pass

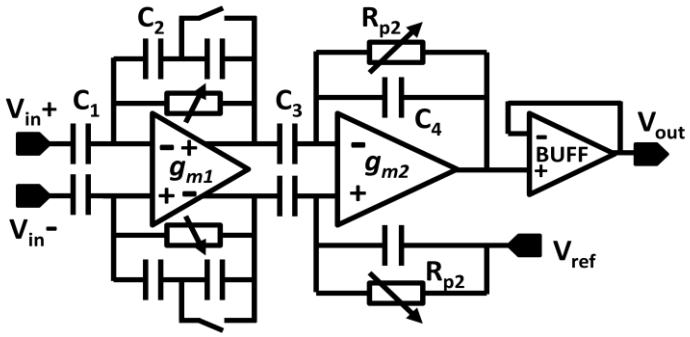
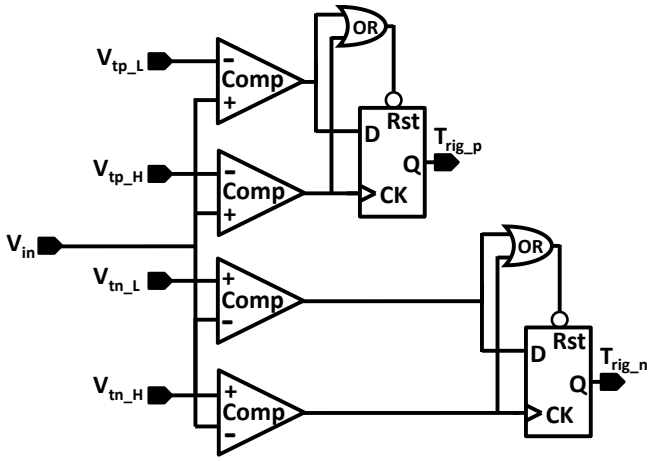
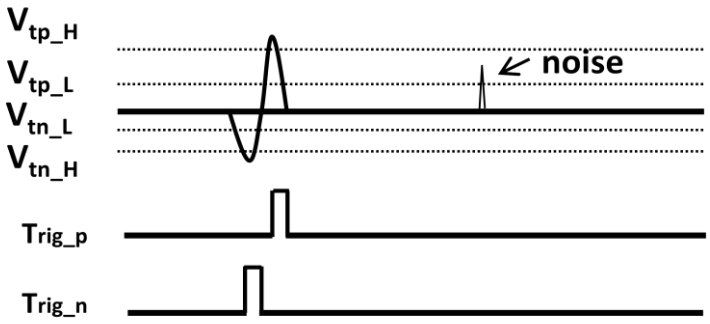


Figure 4.4 Neural recording front-end (RFE) circuit.



(a)



(b)

Figure 4.5 (a) Action potential detector circuit and (b) functionality illustration of the circuit.

cutoff frequencies can be programmed for different recording modes (spikes only, LPF only, or both). This RFE module is designed by a staff member of Institute of Microelectronics (IME) Singapore as part of the collaboration and the details of RFE

design are described in [80-81].

The APD is a simple threshold detector, as shown in Fig. 4.5(a). It contains four comparators and two flip-flops (FF). The APD detects both positive and negative spikes, depending on which comes first. The upper two comparators and FF detect positive spikes. The threshold voltage levels are set by V_{tp_H} and V_{tp_L}, the output trigger signal is asserted when the amplitude of the spike exceeds V_{tp_H} and becomes nil when the amplitude of the spike drops below V_{tp_L} as shown in Fig. 4.5(b). This hysteresis window (between V_{tp_H} and V_{tp_L}) provides some noise immunity to the detector. Similarly, the lower two comparators and FF detect negative spikes. The hysteresis window can be tuned by V_{tn_L} and V_{tn_H}. The trigger signal generated from APD is sent to the digital control block of the system which controls the stimulator. With these two triggering signals from positive and negative threshold detectors, simple spike pattern recognition distinguishing biphasic spikes from electrical glitches is enabled.

4.2.3 Digital Control Block

The main functions of the digital control block are to set stimulation parameters and control the stimulation. The digital block has a default command which determines the stimulation parameters such as amplitude and duration. These parameters can also be programmed by an external FPGA through a serial command. The command

format, control timing and function flow of the digital block are shown in Fig. 4.6.

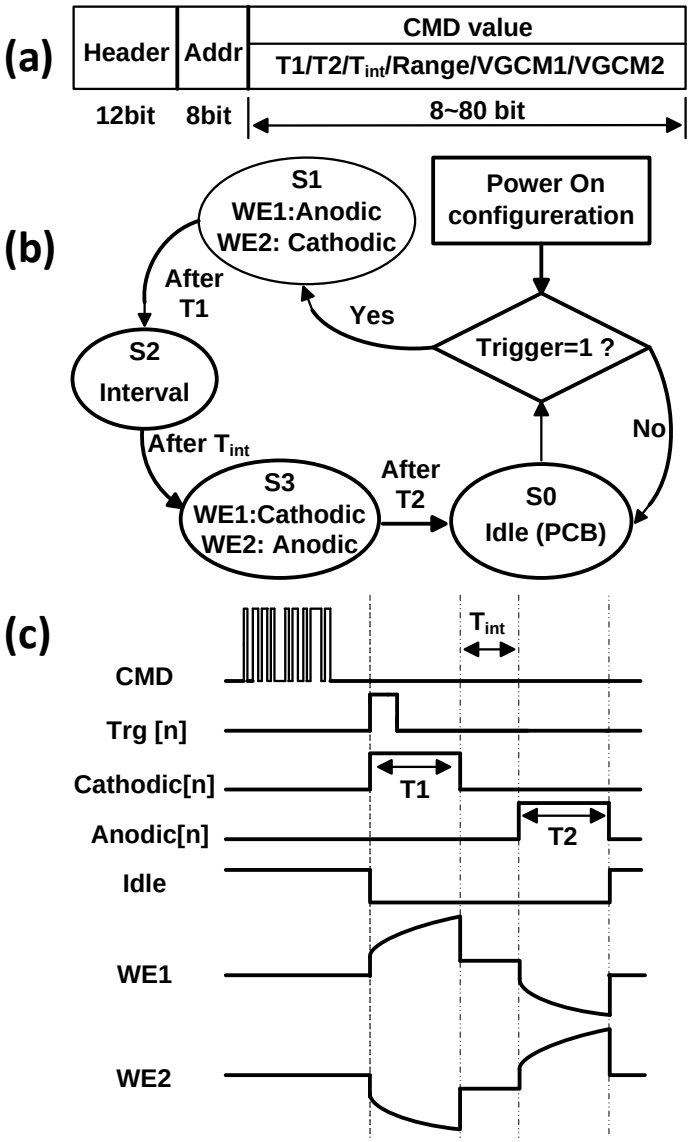


Figure 4.6 (a) command frame, (b) stimulator control state machine, and (c) timing and voltage waveforms of control and output signals.

Stimulation parameters are decoded from the command frame and stored in global digital control registers. In a typical scenario, several command frames are sent first to configure stimulation parameters. When a spike signal is detected by APD, the embedded finite state machine (FSM) generates control signals such as *bs/c*<0:4>,

Iin_s/c<0:4>, *cathodic*, *anodic* and *idle* to deliver a predefined biphasic stimulus. After each stimulation pulse, the external switches connect electrodes WE1, WE2 and RE are short together during the idle phase for passive charge balancing (PCB), as shown in Fig. 4.6(b). The interphasic delay between cathodic and anodic phases can be programmed in the range from 0 μs to 255 μs. The detailed stimulation control timing and output waveforms are shown in Fig. 4.6(c).

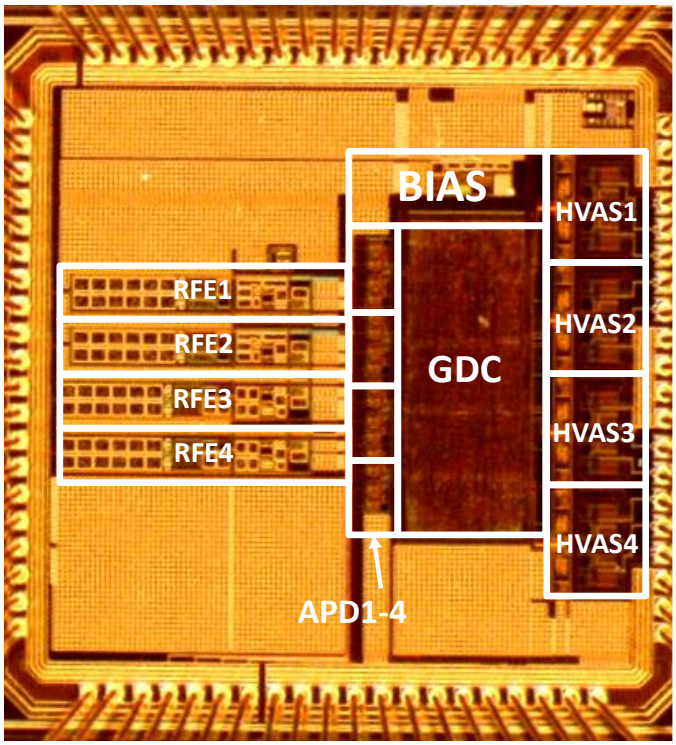
This digital control module is designed by a staff at IME as part of the collaboration. For the completeness of the thesis, the control timing and function flow of the digital block are described in this section only.

4.3 Measurement Results

The 4-to-4-channel closed-loop neural recording and stimulation system with artifact-suppression stimulator is implemented in 0.18-μm HV CMOS technology with LDMOS option. The chip microphotograph is shown in Fig. 4.7(a). The total chip area is 2 mm by 2 mm. Summary of the measured performance is shown in Fig. 4.7(b).

4.3.1 Bench-top Measurement Results

Fig. 4.8 shows the measured output waveforms of two independent HVAS channels of the system. In each channel, the cathodic and anodic current amplitudes are set by two



System	
No. of channels	4 REC + 4 STIM
Area	2mm × 2mm
Recording channel	
Gain	54/60 dB
Bandwidth	0.2Hz – 5.8kHz
Input noise	4.9μVrms
power @ 1V	2.4μW/ch
Stimulation channel	
Mode	Current-mode, RTPPS
Compliance voltage	24V
Current amplitude	1.4μA – 1.4mA
Pulse duration	16μs – 4ms
Interphasic delay	0μs – 255μs
Pulse waveform	10 bits, Arbitrary
Quiescent power	75.2μW/ch

(a) (b)

Figure 4.7 (a) 4-channel recording/stimulation IC microphotograph and (b) summary of measured IC performance.

independent 10-bit DACs. It can generate arbitrary stimulation current waveforms including exponential, triangular, ramp, and constant waveforms, respectively, depending on the application requirement. Pulse durations T_1 and T_2 are also adjustable in the range from 16 μs to 4 ms.

Fig. 4.9 demonstrates test results of the chip configured in REC-STIM mode. In this configuration, the recording electrodes of RFE and the stimulation electrodes of HVAS are electrically isolated. An ECG signal generated from a function generator is used as a dummy neural action potential signal to the input of one RFE channel. The amplitude of ECG pulse is set as 800 μV peak-to-peak with frequency of 100 Hz. The

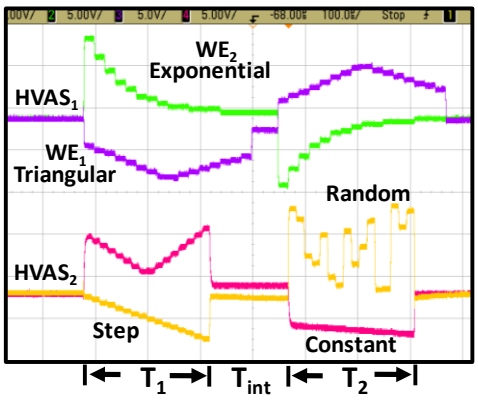
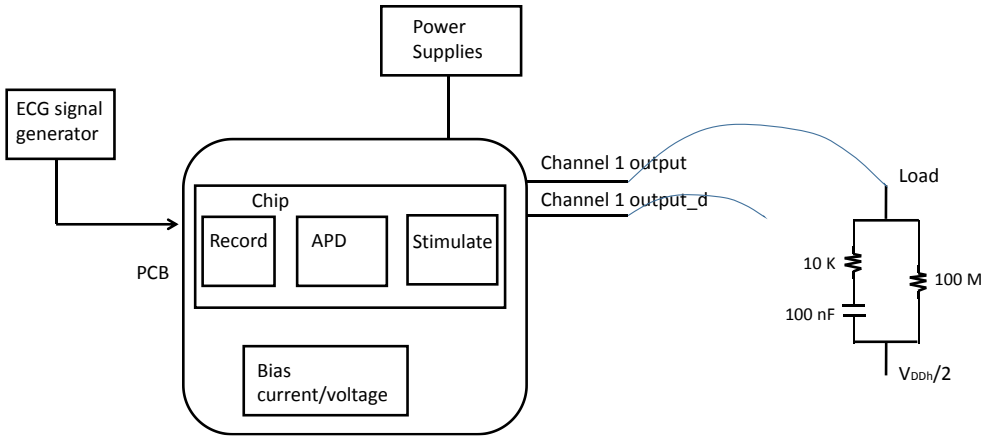
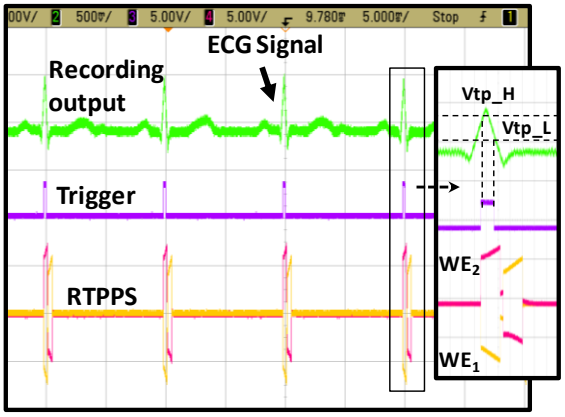


Figure 4.8 Arbitrary stimulation waveforms from two HVAS channels.



(a)



(b)

Figure 4.9 (a) Test-bench measurement setup. (b) Measurement results on one channel: output waveforms of recording circuit, APD, and the HVAS stimulator.

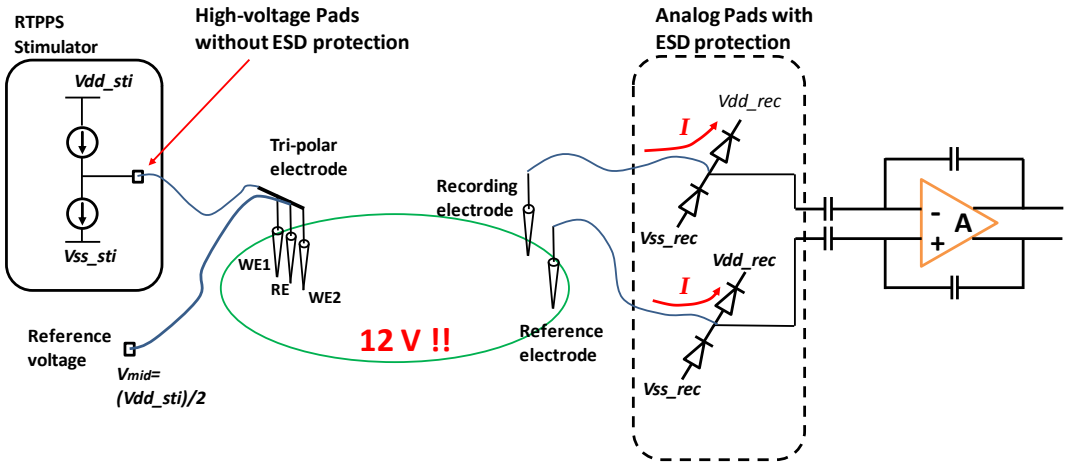
gain of RFE is set as 60 dB (1000 V/V). The band-pass filter of RFE is turned off. As shown in Fig. 4.9, the APD detects the output of RFE and generates the trigger signal for HVAS. Biphasic stimulation pulses are generated by HVAS and delivered to the

electrode nodes, namely WE_1, WE_2 and RE. The current waveform is configured as constant current of 600 μA with pulse duration of 320 μs. The reference voltage on RE is set at 12 V. A dummy load (a 10-kΩ resistor and a 100-nF capacitor in series) is used between each stimulation output and the reference voltage source.

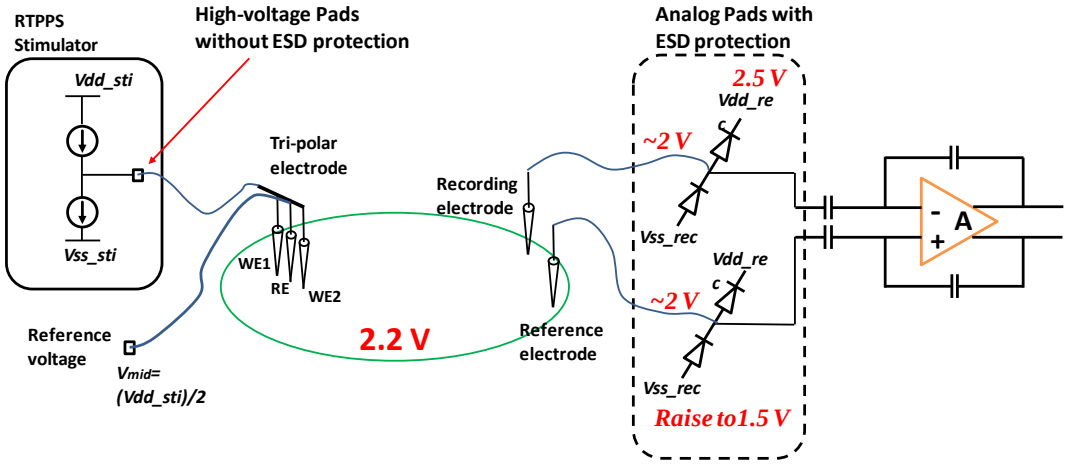
4.3.2 In-Vitro Test

To demonstrate the proposed artifact-suppression technique, an experiment is done with recording and stimulation electrodes in Phosphate buffered saline (PBS) as shown in Fig. 4.10(a). Two chips are used in this experiment. One chip is configured in REC mode while the other chip is configured in STIM mode. The voltage of the HVAS reference electrode RE is set at 2.2 V. But this reference voltage (2.2 V) in the solution may activate the ESD protection circuit at the input of the recording circuit that is powered by 1-V supply, if stimulation and recording circuits share a same ground, as shown in Fig. 4.10 (a).

To protect the input transistors of REC chip from breaking down, two chips are used in the experiment, and the ground of REC chip *VSS_R* is separated from the ground of STIM chip *VSS_S* and raised to 1.5 V, as shown in Fig. 4.10(b). An ECG signal source with a peak-to-peak amplitude of 2.5 mV connected to a metal wire immersed in PBS is used to emulate the neural signal, of which the ground is connected to *VSS_R*. One HVAS stimulation channel and two RFE recording channels are used for



(a)



(b)

Fig. 4.10 (a) ESD pad induced problem in closed-loop recording and stimulation system. (b) Solution for experiment setup: raise ground.

stimulation and signal recording, respectively. Two concentric bipolar stimulation electrodes are tied together with the shared reference electrode to form dummy tri-polar electrode (WE1, WE2, and RE) and placed at the right side of the PBS solution container and two single needle electrodes connected to two recording channels are placed at the left side of the container. The gain of RFE is set as 60 dB (1000 V/V). The band-pass filter of RFE is turned off. The stimulator is

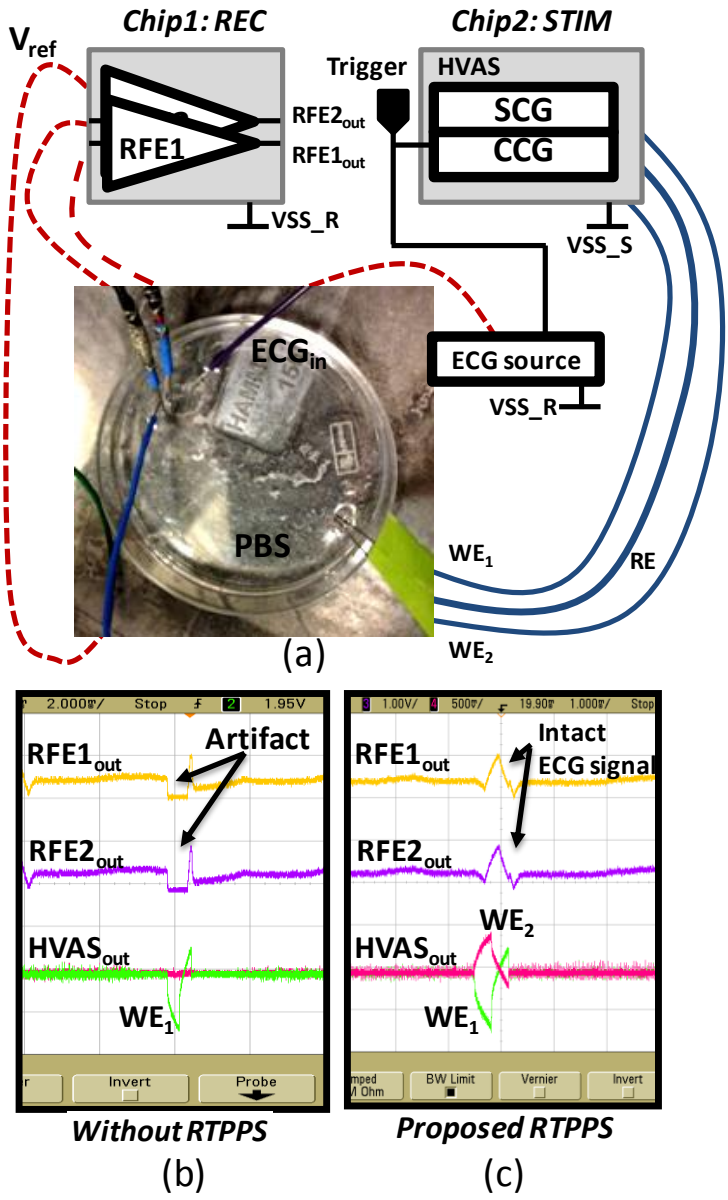


Figure 4.11 (a) In-vitro test setup and (b)-(c) measurement results with and without RTPPS: the top and middle traces show recording outputs from REF channel 1 and 2, respectively. The bottom two traces are the measured voltages on two working stimulation electrodes.

externally triggered to generate the stimulation current (constant current, amplitude = 300 μA, duration = 320 μs), and after 100 μs, the ECG generator outputs an ECG signal to mimic the neural signal evoked by the stimulation (Fig. 4.11(a)). In this scenario, the ECG peak falls within the stimulation period. As shown in Fig. 4.11(b), with the conventional method using a biploar electrode (CCG is disabled), the

stimulation artifact saturates the output of the recording amplifiers. In contrast, with proposed artifact-suppressed stimulator (CCG is enabled), the intact ECG signal is recorded on both channel 1 and channel 2 during the stimulation period, as shown in Fig. 4.11(c). This shows the proposed RTPPS can effectively suppress the stimulation artifact and recording channels are not contaminated by the stimulation.

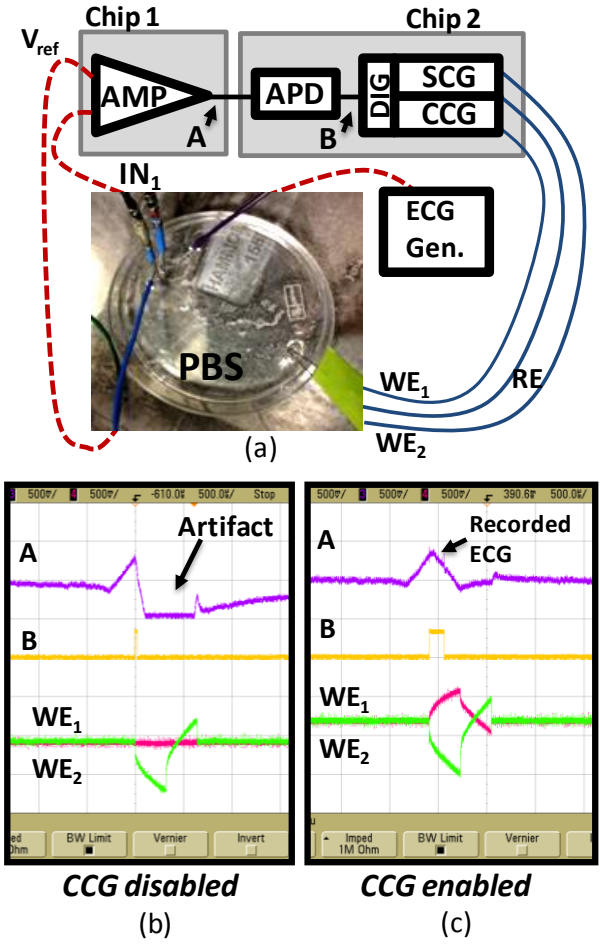


Figure 4.12 In-vitro test setup and results in REC-STIM mode. The top trace is the output signal from recording amplifier. Middle trace is APD output, and the bottom two traces are the voltages on two working stimulation electrodes.

In the REC-STIM mode, as shown in Fig. 4.12(a), one recording channel is used to

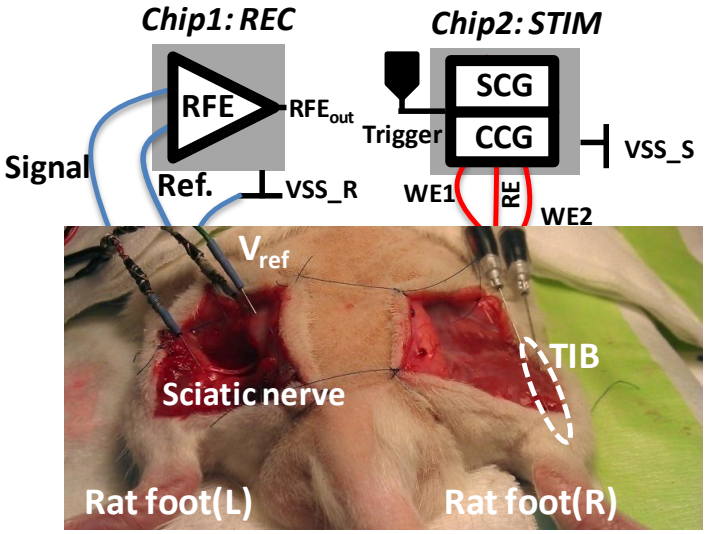
record the ECG signal when the ECG spike is detected the stimulator is triggered, delivering the stimulation current to the PBS solution. It is observed that when CCG is disabled, the stimulation artifact saturates the output of the recording amplifier, as shown in Fig. 4.12(b), which needs a long period of time to recover to the normal state before it can perform recording again. However, with CCG enabled in Fig.4.12(c), an intact ECG signal is recorded during the stimulation period and the saturation is not observed at the output of the recording amplifier.

The aforementioned two in-vitro experiments have demonstrated the functionality and effectiveness of the proposed artifact-suppression stimulator in the close-looped recording and stimulation system.

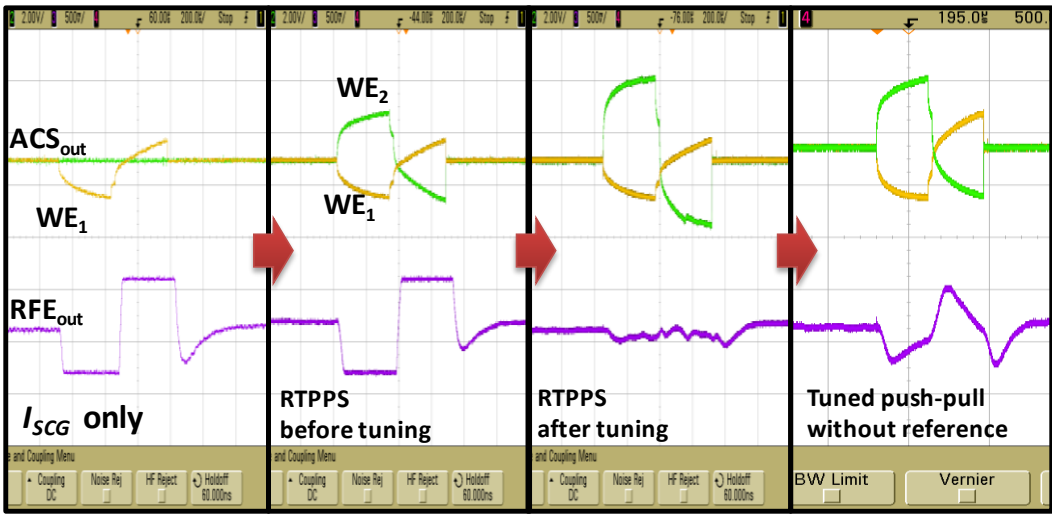
4.3.3 Animal Experiment

Two in-vivo experiments with a rat animal model are carried out using the proposed RTPPS. The first experiment is to demonstrate that the artifact generated from muscle stimulation can be suppressed at the input of the recording channel. The second experiment is setup in STIM-REC mode, where the system stimulates the nerve and subsequently records the neural spike induced by the nerve stimulation. The experiment shows that with the proposed RTPPS, the stimulation artifact does not affect the recording channel. Both experiments are compared with the conventional bipolar stimulation.

1) Muscle stimulation: The experiment setup is shown in Fig. 4.13(a). The same chip configuration and ground/power arrangement are used as in Fig. 4.11. The recording needle electrode is inserted into the sciatic nerve on the left side of an anesthetized rat and two concentric stimulation electrodes are inserted in the tibialis anterior (TIB) muscle of the right leg. Since the commercial tri-polar electrode is not available, two concentric electrodes are put together and share the same reference voltage to emulate a tri-polar stimulation electrode. The voltage waveforms on recording and stimulation electrodes are probed and observed using an oscilloscope. First of all, a biphasic stimulation pulse (amplitude = 90 μA, pulsewidth = 320 μs) is delivered to the muscle through WE1 and RE by activating SCG only. Fig. 4.13(b) shows the output waveforms at RFE output. It is observed that the stimulation artifact is coupled to the input of RFE through the tissue and saturates its output. Fig. 4.13(c) shows the RFE output when both SCG and CCG are enabled and tri-polar stimulation is performed. The artifact is still observed. This is due to the asymmetry between the two electrode-tissue interfaces of WE1 and WE2. In Fig. 4.13(d), the current amplitude generated from CCG is tuned (to a larger value in this case). After the tuning, the stimulation artifact is significantly suppressed. Lastly, for comparison, in Fig. 4.13(e) the reference voltage is disconnected from the reference electrode in the tri-polar electrode configuration to emulate the conventional push-pull bipolar stimulator [63]. In this case, we find that the artifact is a little smaller than the conventional bipolar



(a)



(b) (c) (d) (e)

Figure 4.13. (a) In-vivo test setup to observe muscle stimulation artifact suppression (recording in sciatic nerve), and (b) - (e) top traces are the stimulation pulse waveforms and the bottom trace is the output from RFE.

stimulator, but still cannot be substantially suppressed due to the asymmetry of two stimulation interfaces. In conventional push-pull stimulators, the current tuning is inapplicable since there is no reference point for tuning. Therefore, the shared reference electrode must be present. In aforementioned experiments, successful

muscle recruitment on rat's right foot is observed.

2) Nerve stimulation and recording: Fig. 4.14(a) shows the in-vivo experiment setup for concurrent neural stimulation and recording on the sciatic nerve of an anesthetized rat and the measurement results. The chips configuration and ground/power arrangement are the same as in Fig. 4.11(a). Two concentric electrodes are tied together to form a tri-polar (WE1, WE2, and RE) electrode and attached to the sciatic nerve. Note that these two concentric electrodes however may not be positioned well within the nerve cross-section. This coarse arrangement leads to a possible asymmetric coupling between stimulation and recording sites, which results in asymmetric voltage waveforms at WE1 and WE2 for artifact suppression in this experiment. Two single-needle electrodes are used for recording. One recording electrode is inserted into the nerve which is about 5 mm away from the stimulation site while the other one is placed in the animal body as a reference. Firstly, a stimulation pulse train is delivered to the nerve from the stimulator. For each pulse, the amplitude is set to 53 μA and the pulse width is 320 μs for both cathodic and anodic phases, with an interphasic delay of 25 μs. Foot dorsiflexion (FD) is observed and evoked compound action potential (CAP) is recorded. In Fig. 4.14(b) the two test results with and without RTPPS are plotted in the same graph. The top trace is the stimulation pulse waveform used in RTPPS mode. Middle trace is the recorded RFE response with RTPPS enabled and the bottom trace is the recorded REF response without RTPPS. Using conventional bipolar stimulation method without RTPPS

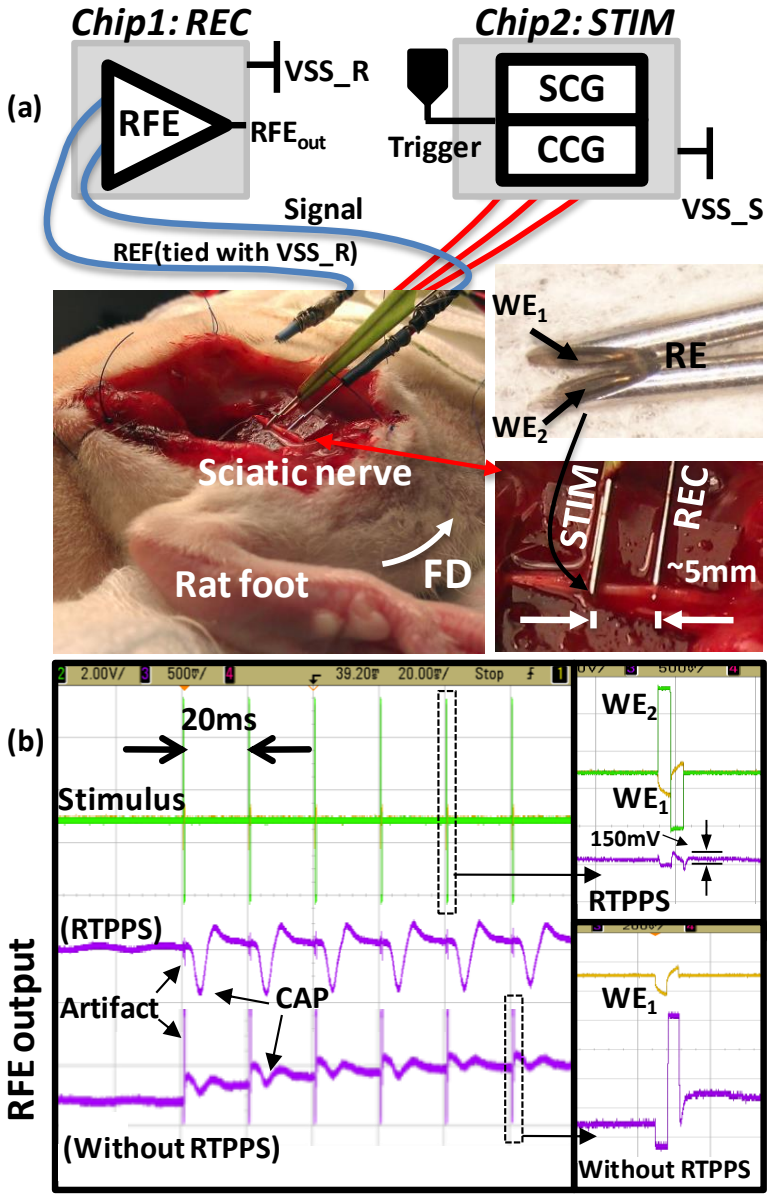
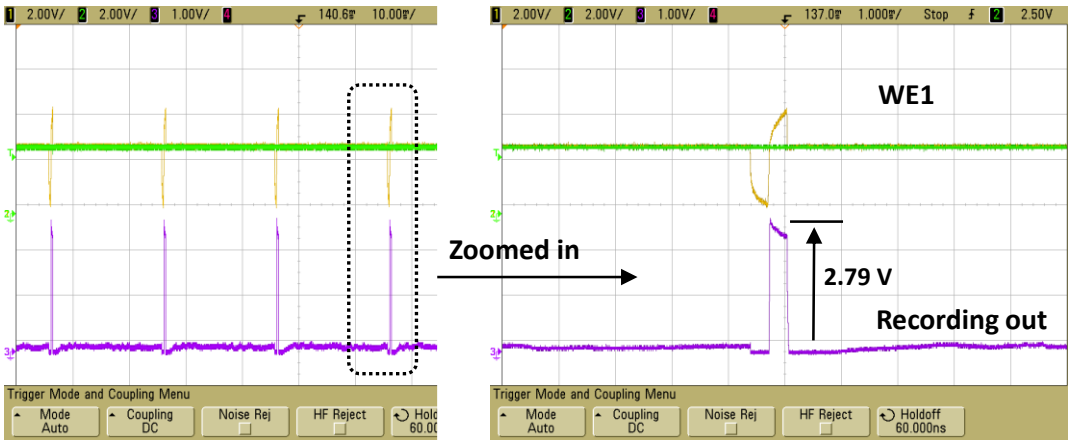


Figure 4.14. (a) In-vivo test setup to observe neural stimulation artifact suppression and (b) test results including comparison to conventional bipolar stimulation.

(CCG disabled), the large artifact is caused by saturation of the amplifier and DC voltage drift is observed at the RFE output. In contrast, when RTPPS is enabled with CCG tuned properly, the stimulation artifact is substantially suppressed. A series of evoked neural spikes can be clearly seen on the oscilloscope and the amplitude of the

suppressed artifact is reduced to 80-150 mV peak-to-peak, which is only 10% - 20% of the CAP signal recorded. The different amplitudes of the recorded CAP signal are caused by the different stimulation current path in the two setups. In RTPPS, the stimulation current flows from WE1 to WE2, while in bipolar stimulation the same current flows from WE1 to RE. Since the distance between WE1 and WE2 is much larger than the distance between WE1 and RE in this coarse tri-polar electrode configuration, as shown in Fig. 4.14(a), more nerve cells are activated in RTPPS, producing a larger CAP. Besides, the tri-polar electrode used in this experiment and its placement are not ideal thus introducing some mismatch and the tuning of CCG in Fig. 4.14(b) almost hits the limit to compensate this mismatch. The efficacy of artifact suppression is expected to be even more significant when a true or better tri-polar electrode is used.



(a) (b)

Fig. 4.15 (a) Artifact recorded in rat experiment using bipolar stimulation (SCG only) with a 3.3-V recording circuit. (b) Zoomed-in waveforms of electrode voltage and recorded artifact.

It’s noticed from experiment result (Fig. 4.14(b)) that the amplified stimulation artifact exceeds the 1-V compliance of recoding circuit. In order to determine the artifact amplitude, a 3.3-V power supplied recording circuit [23] with the same gain (60 dB) is used to replace chip 1 shown in Fig. 4.14(a) and record the amplitude of stimulation artifact. As shown in Fig. 4.15, the amplitude of artifact caused by anodic stimulation pulse is 2.79 V. Therefore, a peak-to-peak stimulation artifact around 5.58 V is found in this bi-phasic nerve stimulation. By using proposed RTPPS, an artifact suppression of more than 31 dB ($20\times\lg\frac{5.58}{0.15}$) is achieved. Both stimulation artifact spike and tail are suppressed without any blanking.

4.4 Summary

A new stimulation artifact suppression scheme RTPPS is presented and demonstrated in this chapter. A 4-to-4 channel neural recording and stimulation IC is designed, which can be configured in REC, STIM, REC-STIM and STIM-REC modes. In the proposed RTPPS, Two working electrodes WE1 and WE2 are symmetrically arranged with respect to the shared reference electrode RE, forming a tri-polar stimulation electrode. The biphasic stimulation pulse from the working electrode WE1 is counteracted by the complementary stimulation pulse from the second working electrode WE2, which greatly suppresses the stimulation artifact generated by the stimulation pulse. The mismatch between two stimulation currents, as well as that between the two electrode-tissue interfaces can be corrected by tuning the current

amplitude delivered to the second working electrode (WE2). The efficacy of the proposed RTPPS method to suppress stimulation induced artifact has been demonstrated in both bench-top and in-vivo experiments. An artifact suppression of more than 31 dB is achieved.

CHAPTER 5

CONCLUSION AND FUTURE WORKS

5.1 Conclusion

Two prototype neural/muscular stimulators aimed to improve the power efficiency and suppress the artifact suppression, respectively, have been presented in this thesis. The first 16-channel power- and area-efficient stimulator employs an exponentially decaying stimulation current. The analysis has shown that of the power efficiency of the output stage in current-mode stimulator can be improved by using exponentially decaying stimulation current as compared to the constant current. A novel exponential current generator is therefore proposed and implemented in the prototype stimulator to improve the power efficiency. The current copying technique is also adopted to realize DAC sharing, which greatly reduces the overall chip area for the multichannel stimulator. Large output voltage compliance (±11.5V) is achieved by using high-voltage output stage to ensure the effectiveness of neural/muscular stimulation. Stimulation parameters such as current amplitude and pulse width are programmable to realize stimulation flexibility. The stimulation safety is guaranteed by using active charge balancing. Integrating all aforementioned functions, this stimulator has been fabricated in a 0.18 μm CMOS process with 24-V LDMOS option. The maximum power efficiency of 95.9% at the output stage only and 87.8% for the overall stimulator have been achieved in bench top test with dummy load. A 10% improvement in PE compared to the constant current stimulation is observed.

The second prototype stimulator is implemented for artifact suppression in closed-loop neural/muscular recording and stimulation system. The analysis of stimulation-artifact origin in a closed-loop system has been given and a referenced and tuned push-pull stimulation (RTPPS) method with tri-polar electrode is proposed to cancel the stimulation artifact. The prototype artifact-suppressed stimulator features 1.4-mA maximum stimulation current, 24-V voltage compliance, arbitrary waveform generation, and stimulation artifact suppression. Measurement results have shown that the stimulation artifact is greatly reduced compared to the traditional bipolar stimulator. Both in-vitro and in-vivo test have been carried out, in which the CAP can be clearly observed with RTPPS without the need for blanking the RFE. The amplitude of the suppressed artifact is reduced to 80-150 mV peak-to-peak, which is only about 10% - 20% of the CAP signal recorded. The measured artifact suppression is more than 31 dB.

5.2 Future work

The power efficiency improvement of the stimulator using exponentially decaying current is dependent on the electrode-tissue interface. In this work, I_s is manually adjusted to fit different loads. In future work, on-chip automatic calibration of I_s can be made possible through real-time feedback control of current tuning by monitoring the voltage on the electrode to get suitable exponentially decaying current for a practical electrode.

Secondly, the 16-channel stimulator has a maximum delay of 64 μs. Since the current copier circuit needs 4 μs to refresh the capacitor for each channel and there are 16 channels in total, if any two of 16 channels refresh at the same time, the clash between stimulation and refreshing may occur and the output current could be disturbed. In this design each trigger signal requires a 4-μs interval time between. In the future design, two sets of current copier cells can be used and the refreshing mechanism can be changed accordingly to allow exact simultaneous triggering without any delay.

Thirdly, mismatch between negative and positive output current of the stimulator due to the channel length modulation effect of the transistors at HV output driver has been observed, which may cause undesired residual charge during stimulation or require a longer charge-balancing time. This current mismatch is attributed to the simple current mirror circuit used in the output stage. Cascode structure or other output current drivers with high output impedance could be used in the future design to minimize the mismatch.

Finally, an integration version of neural/muscular stimulator design with both high power efficiency and artifact suppression can be implemented in one chip for a high-performance stimulation system.

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