MATERIAL PROCESSING AND DEVICE APPLICATIONS OF ORGANIC AND METAL OXIDE SEMICONDUCTOR MATERIALS

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NATIONAL UNIVERSITY OF SINGAPORE

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Thesis Declaration

I hereby declare that this thesis is my original work and it has been written by me in its entirety, under the supervision of A/Prof. Wu Jishan, Chemistry Department, National University of Singapore, between 2010 and 2014.

I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

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SUMMARY

To date, it has received so much attention in the development of low-cost, large area, flexible and lightweight devices by using organic and metal oxide semiconducting materials. Generally, the conventional silicon based semiconductors have high charge carrier mobilities for the thin film transistor devices. However, the thin films of conventional semiconductor usually need high processing temperature and dustless conditions, which significantly increase the fabricating cost. Most importantly, the silicon based materials cannot be processed on flexible substrates due to their poor stretching characteristics. However, compared to the conventional silicon based semiconductors, the organic and metal oxide based semiconductor materials exhibit low cost, good processibility, and can be fabricated on flexible substrates.

Organic and metal oxide based semiconductors have various applications as key components of numerous electronic and optoelectronic devices, including field effect transistors (FETs), photovoltaics (PVs), and light emitting diodes (LED). Especially for the field effect transistor, a lot of efforts have been done to develop new materials to improve device performance with high charge carrier mobility and good air stability.

In chapter **1**, the introduction to charge transport mechanism, charge carrier mobility characterization, organic field effect transistors, recent progress in PAH based semiconductors, organic semiconductor alignment methods, and metal oxide

based transistors and interlayers for solar cells were reviewed separately. In chapter **2**, stepwise cyanation of tetrabromonaphthalene diimide gave a series of cyanated compounds. The electron affinity showed a good linear relationship with the number of the cyano groups, and the extremely low-lying LUMO energy levels of tri- and tetracyano- NDIs made them unstable to moisture. The mono- and di-cyanated NDIs however could be obtained as stable n-type semiconductors and used for air-stable n-channel OFETs with moderate electron mobilities. It implies that we need to find a good balance between the materials' stability and device stability by careful control of the electron affinity when designing the n-type organic semiconductor materials.

In chapter **3**, large disc-like ovalene diimides were investigated for the n-type semiconductors. The large disc-like molecule ovalene was firstly used as a building block for the design of n-type semiconductors. The C2-symmetry ovalene diimide (ODI) and the dicyano-ovalene diimide (ODI-CN) were prepared for the first time from bisanthene building block. Due to attachment of electron-withdrawing imide and cyano groups, ODI-CN exhibited stable n-type transistor behavior. After processing optimization, high electron mobilities up to 0.51 cm^2/Vs in air and 1.0 cm^2/Vs in N_2 atmosphere were achieved in solution processing OFET devices.

In chapter **4**, in order to further increase the transistor performance, thin film alignment technique was applied using slot die coating. Solvent ratio, substrate temperature and coating speed proved crucial to the final crystal morphology and thin film uniformity. POM and AFM images showed that millimeter-sized and highly

oriented crystalline domains were achieved at proper coating conditions. Polarized UV-vis proved that crystal anisotropy exists in the thin film and the value is about 2.5 (at 588 nm). XRD results gave a good explanation that the single crystal growth direction is along the π-π stacking direction. Finally, an average saturation regime mobility of 1.8 $cm^2V^{-1}s^{-1}$ has been achieved in the ambient condition for TIPS-pentacene thin film transistor devices. In chapter **5**, slot die coated technique was also applied to the polymer system. The crystalline polymer thin film could be better tuned by the solution shearing force, and high-performance slot die coated devices were achieved. Meanwhile, low voltage devices using native grown AlO_x modified with octadecylphosphonic acid self-assembled monolayer were succssfully fabricated and exhibited charge carrier mobility of 1.6-2.0 $cm^2V^{-1}s^{-1}$.

In order to replace the unstable n-type organic semiconductor materials, n-type metal oxide were introduced. In chapter **6**, ZnO semiconducting thin film and TFT devices through hydrolyzing ZnO precursors with different water content were conducted. It was found that introducing controlled amount of water molecules, either in the form of water vapor during annealing or as an additive in the ZnO precursor solutions, could enhanced the ZnO thin film quality by improving the yield of polycrystalline ZnO from its hydroxides. However, excessive amount of water molecules in the ZnO precursor was undesirable due to the formation of acceptor-like traps in ZnO thin film, led to lower TFT mobility, greater V_T shift and hysteresis voltage, thus degrading TFT performances. In chapter **7**, in order to enhance the

charge carrier mobilities of the ZnO thin films, F and LiF-codoped ZnO thin films have been successfully prepared from aqueous solution at low processing temperature. It was found that F and LiF doping at the appropriate amounts enhanced the oxide film quality and reduced defect sites. The TFTs based on LiF doped ZnO thin films revealed largely improved device performance with average electron mobility up to 8.9 $cm^2V^{-1}s^{-1}$ compared with the mobility of 1.6 $cm^2V^{-1}s^{-1}$ for non-doped ZnO TFTs. Our results suggest that LiF doping can be a useful technique to produce more reliable and low temperature solution-processed oxide semiconductor TFTs.

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α	Absorption coefficient
ε_0	Permittivity of free space
ε_r	Dielectric constant
λ	Wavelength
T	Lifetime
1-OT	1-octanethiol
A	Accepter
Al	Aluminum
AFM	Atomic force microscopy
Ag	Silver
AlO_x	Aluminium oxide
Au	Gold
C	Capacitance
$CHCl_3$	Chloroform
Cr	Chromium
CMOS	Complementary metal–oxide–semiconductor
CV	Cyclic Voltammetry
CYTOP	(Poly(perfluorobutenylvinylether)) amorphous fluoropolymer
DCB	Dichlorobenzene

D	Donor
DOS	Density of states
DLCs	Discotic liquid crystals
DPP	Diketopyrrolopyrrole
DPPT-TT	Diketopyrrolopyrrole-dithienylthieno[3,2-b]thiophene
DSC	Differential Scanning Calorimetry
EC	Electrochromic
Eg	Band gap
F	Fluorine
FETs	Field effect transistors
FESEM	Field emission scanning electron spectroscopy
hν	Photon energy
H_2O	Water
HBC	Hexabenzocoronenes
HfO_2	hafnium (IV) oxide
HMDS	Hexamethyldisilazane
HOMO	Highest occupied molecular orbital
IPA	Iso-propanol
ITO	Indium doped tin oxide
IZO	Indium doped zinc oxide
IGZO	Indium gallium doped zinc oxide

IZTO	Indium zinc doped tin oxide
IGO	Indium doped gallium oxide
k_B	Boltzmann constant
LB	Langmuir-Blodgett
LC	Liquid crystal
LEDs	Light emitting diodes
LUMO	Lowest unoccupied molecular orbital
MISFET	metal–insulation–semiconductor field-effect transistor
N_2	Nitrogen
NDI	Naphthalene Diimide
ODI	Ovalene-3,4:10,11-bis(dicarboximide)
ODI-CN	7,14-Dicyano-ovalene-3,4:10,11-bis(dicarboximide)
ODTS	Octadecyltrichlorosiane
ODPA	N-octadecylphosphonic acid
OFET	Organic field effect transistor
OPV	Organic photovoltaic cells
OTS	Octyltrichlorosilane
OTMS	Octadecyltrimethoxysilane
OTMS-C8	Octyltrimethoxysilane
PAH	Polyaromatic hydrocarbon
PEN	Poly(ethylenenaphthalate)

PET	Polyethylene terephthalate
PenDI	6,13-Dicyano pentacene-2,3:9,10-bis(dicarboximide)
PDI	Perylenediimde
PDQT	Poly(Diketopyrrolopyrrole-Quaterthiophene)
PFBT	Pentafluorobenzenethiol
PI	Polyimide
PL	Photoluminescence
PLED	Polymer light-emitting diodes
PMMA	Poly(methyl methacrylate)
PVA	Polyvinyl alcohol
PVP	Poly(4-vinylphenol)
POM	Polarizing Optical Microscope
PTS	Phenyltrichlorosilane
PVs	Photovoltaic
q	Electron charge
RT	Room temperature
RFID	Radio frequency identification
SAM	Self-assembled monolayer
SCLC	Space-charge limited current
T	Transmittance
TFT	Thin film transistor

TGA	Thermal Gravimetric Analysis
TIPS-pentacene	6,13-bis(triisopropylsilylethynyl) pentacene
TiOx	Titanium oxide
TOF	Time of flight
TOF-SIMS	Time-of-flight Secondary Ion Mass Spectrometer
TT	Dithienylthieno[3,2-*b*]thiophene
UPS	Ultraviolet photoelectron spectroscopy
V_{th}	Threshold voltage
UV	Ultraviolet
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
ZnO	Zinc oxide

Chapter 1 Introduction

To date, it has received so much attention in the development of low-cost, large area, flexible and lightweight devices by using organic and metal oxide semiconducting materials. Up to now, the conventional amorphous silicon based semiconductors have achieved much progress with charge carrier mobility around 1.0 $cm^2V^{-1}s^{-1}$. However, the thin films of conventional semiconductor usually need high processing temperature and dustless conditions, which significantly increase the fabricating cost. Most importantly, the silicon based materials cannot be processed on flexible substrates due to their poor stretching characteristics. Nevertheless, compared to the conventional silicon based semiconductors, the organic and metal oxide based semiconductors exhibit low cost, good processibility, and can be fabricated on flexible substrates.

Organic and metal oxide semiconductors have various applications as key components of numerous electronic and optoelectronic devices, including field effect transistors (FETs), photovoltaics (PVs), and light emitting diodes (LEDs). Especially for the field effect transistor, a lot of efforts have been done to develop new materials to improve device performance with high charge carrier mobility and good air stability.

In this chapter, the introduction to charge transport mechanism, charge carrier mobility characterization, organic field effect transistors, recent progress in polyaromatic hydrocarbon (PAH) based semiconductors, organic semiconductor

alignment methods, and metal oxide based transistors will be reviewed separately.

1.1 Charge transport and related mechanisms

The study of electron and hole transport in organic materials has a long history which dates back to 60 years ago. Later on, lots of work about these studies had been done by many groups. In the mid 1970s, Scher group using the continuous time random walk model laid the theoretical description of hopping transport in disordered materials.[1] Untill today, the exact nature of charge transport in organic semiconductors is still open to debate. However, a general idea can be obtained using the disordered semiconductors and highly ordered organic single crystals as the standards. Depending on the degree of order, the charge carrier transport mechanism in organic semiconductors can fall between two extreme cases: band or hopping transport. Band transport is typically observed in highly purified molecular crystals at not too high temperatures. However, since electronic delocalization is weak, the bandwidth is small as compared to inorganic semiconductors (typically a few kT at room temperature only). Therefore, the value of room temperature mobility in molecular crystals reaches only in the range 1 to 10 cm^2/Vs. In the other extreme case of an amorphous organic solid hopping transport prevails which leads to much lower mobility values (at best around 10^{-3} cm^2/Vs).

Localization in conjugated organic materials occurs via the formation of polarons. A polaron results from the deformation of the conjugated chain under the action of the

charge. In other words, in a conjugated molecule, a charge is self-trapped by the deformation. This mechanism of self-trapping is often described through the creation of localized states in the gap between the valence and the conduction bands.

A useful model to describe the charge transport in organic materials is that of the small polaron, developed by Holstein.[2] It is a one-dimensional, one-electron model (that is, the electron-electron interactions are neglected). The total energy of the system is the sum of three terms (the lattice energy, electron dispersion energy, and the polaron banding energy).

The charge carrier mobility is temperature and field dependence. For temperature dependent mobility, when the mobility is extrapolated at the zero-field limit, the fit of the Monte Carlo (MC) results leads to the following expression:

$$\mu(T) = \mu_0 \exp[-\left(\frac{2\sigma}{3k_B T}\right)^2] = \mu_0 \exp[-\left(\frac{T_0}{T}\right)^2], \quad (1)$$

where σ representing the width of the diagonal disorder, μ_0 is mobility at room temperature, k_B is Boltzmann constant, T_0 is room temperature. Since the temperature helps in overcoming the barriers introduced by the energetic disorder in the system, the temperature talking about here only depends on the amplitude of σ. This expression deviates from an Arrhenius-like law, and this expression generally fit the experimental data well, as a result of the limited range of temperatures available.

The impact of an external electric field is to lower the energy barrier for electron get into the conduction band since part of this energy comes from being pulled by the electric field. In the presence of energetic disorder only, the Monte Carlo results

generally yield a Poole-Frenkel behavior when electric fields larger than 10^4-10^5 V/cm:

$$\mu(E) = \mu_o \exp(\beta\sqrt{E}) \quad (2)$$

where μ_o is the low field mobility, β is Poole–Frenkel coefficient, and E is the applied electric field.[3] The field dependence becomes more pronounced as the extent of energetic disorder grows. The increase in electric field amplitude is also accompanied by an increased diffusion constant.

1.2 Characterization of charge carrier mobility

Charge carrier mobility can be determined experimentally by various techniques.[4-5] Results from methods that measure mobility over macroscopic distances (~1 mm) are often dependent on the purity and order in the material. Methods that measure mobility over microscopic distances are less dependent on these characteristics. We briefly describe below the basic principles of some of the most used methods.

1.2.1 Time-of-flight (TOF)

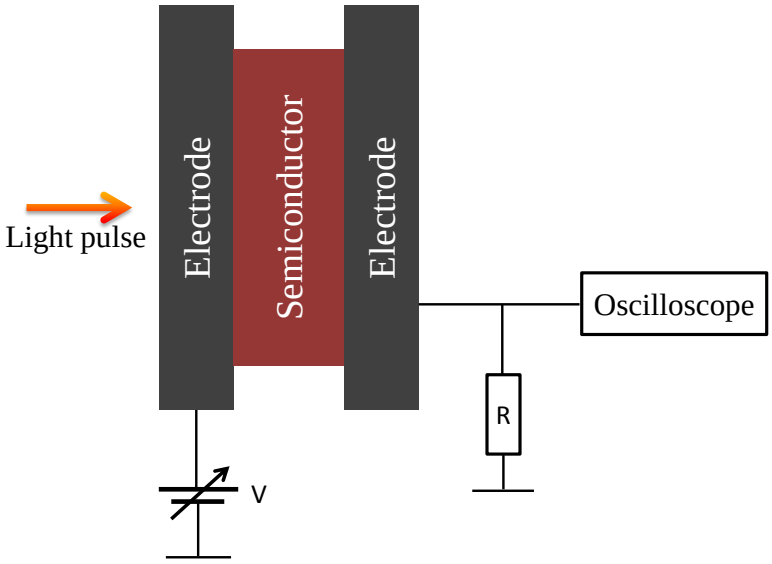

Figure 1.1 The setup of the TOF technique.

Here, a few microns thick organic layer is sandwiched between two electrodes. The material is first irradiated by a laser pulse in the proximity of one electrode to generate charges. Depending on the polarity of the applied bias and the corresponding electric field (in the 10^4-10^6 V/cm range), the photo-generated holes or electrons migrate across the material toward the second electrode. The current at that electrode is recorded as a function of time. A sharp signal is obtained in the case of ordered materials while in disordered systems a broadening of the signal occurs due to a distribution of transient times across the material. The mobility of the holes or electrons is estimated via:

$$\mu = \frac{v}{F} = \frac{d}{Ft} = \frac{d^2}{Vt} \quad (3)$$

where d is the distance between the electrodes, F is the electric field, t is the averaged transient time, and V is the applied voltage. TOF measurements clearly show the

impact of structural defects present in the material on charge carrier mobility. Charge carrier mobilities in organic materials were first measured with the TOF technique by Kepler[6] and Leblanc[7].

1.2.2 Field-effect transistor (FET) configuration

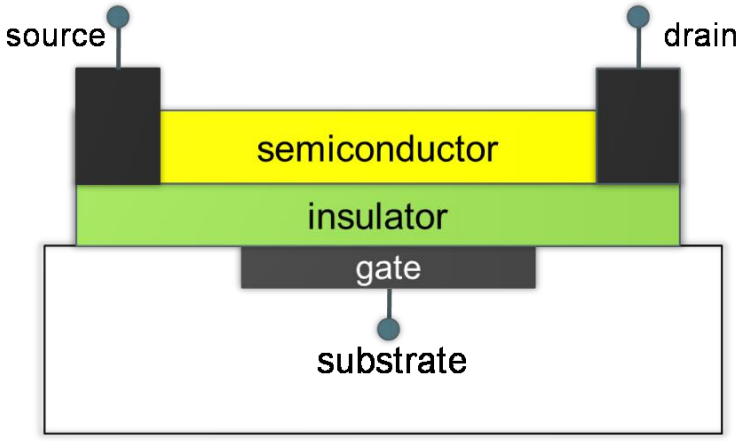

Figure 1.2 The structure of thin film transistor.

The carrier mobilities can be extracted from the electrical characteristics measured in a field-effect transistor (FET) configuration. As reviewed by Horowitz,[8] the I-V (current-voltage) expressions derived for inorganic-based transistors in the linear and saturated regimes prove to be readily applicable to organic transistors (OFETs). These expressions read in the linear regime:

$$I_{SD} = \frac{W}{L}\mu C_i(V_G - V_T)V_{SD},\ V_D < V_G - V_T \quad (4)$$

And in the saturated regime:

$$I_{SD} = \frac{W}{2L}\mu C_i(V_G - V_T)^2,\ V_D > V_G - V_T \quad (5)$$

Here, I_{SD} and V_{SD} are the current and voltage bias between source and drain, respectively, V_G denotes the gate voltage, V_T is the threshold voltage, C_i is the

capacitance of the gate dielectric, and W and L are the width and length of the conducting channel. In FETs, the charges migrate within a very narrow channel (at most a few nanometers wide) at the interface between the organic semiconductor and the dielectric.[9] Transport is affected by structural defects within the organic layer at the interface, the surface morphology and polarity of the dielectric, and/or the presence of traps at the interface (that depends on the chemical structure of the gate dielectric surface). Contact resistance at the source and drain metal/organic interfaces also plays an important role; the contact resistance becomes increasingly important when the length of the channel is reduced and the transistor operates at low fields; its effect can be accounted for via four-probe measurements.[10]

The charge carrier mobilities extracted from the OFET I-V curves are generally higher in the saturated regime than those in the linear regime as a result of different electric-field distributions. The mobility can sometimes be found to be gate-voltage dependent;[11] this observation is often related to the presence of traps due to structural defects and/or impurities (that the charges injected first have to fill prior to establishment of a current) and/or to dependence of the mobility on charge carrier density (which is modulated by V_G).[12]

The dielectric constant of the gate insulator is another important parameter; for example, measurements on rubrene single crystals[13] and polytriarylamine chains[14] have shown that the carrier mobility decreases with increasing dielectric constant due to polarization (electrostatic) effects across the interface; the polarization induced at

the dielectric surface by the charge carriers within the organic semiconductor conducting channel, couples to the carrier motion, which can then be cast in the form of a Frolich polaron.[15]

1.2.3 Space-charge limited current (SCLC)

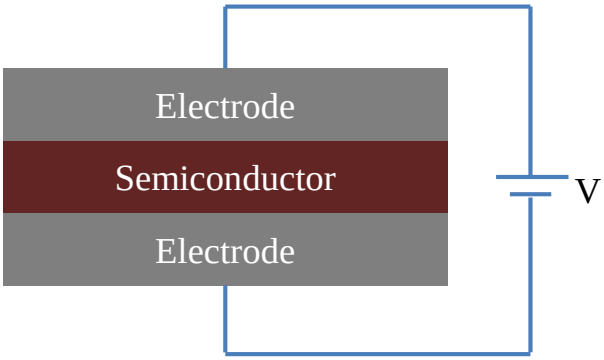

Figure 1.3 The structure of a SCLC based device.

The mobilities can also be obtained from the electrical characteristics of diodes built by sandwiching an organic layer between two electrodes (provided that transport is bulk limited and not contact limited). The choice of the electrodes is generally made in such a way that only electrons or holes are injected at low voltage. In the absence of traps and at low electric fields, the current density *J* scales quadratically with applied bias *V*. Such behavior is characteristic of a space-charge limited current (SCLC); it corresponds to the current obtained when the number of injected charges reaches a maximum because their electrostatic potential prevents the injection of additional charges.[16] In that instance, the charge density is not uniform across the material and is largest close to the injecting electrode.[17] In this regime, when neglecting diffusion contributions, the J-V characteristics can be expressed as:

$$J = \frac{9}{8} \epsilon_0 \epsilon_r \mu \frac{V^2}{L^3} \quad (6)$$

where ε_r denotes the dielectric constant of the active layer and L is the device thickness. (Note that a field-dependence of the mobility has to be considered at high electric fields.) The J-V curves become more complex in the presence of traps. They first exhibit a linear regime, where transport is injection-limited, followed by a sudden increase for an intermediate range of applied biases; finally, the V^2 dependence of the trap-free SCLC regime is reached. The extent of the intermediate region is governed by the spatial and energetic distribution of trap states, which is generally modeled by a Gaussian[18] or exponential distribution[19].

1.3 Organic field effect transistors

1.3.1 Introduction

Organic field effect transistors (OFETs) were first described in 1986.[20] They have attracted increasing interests in both academic and industrial institutions, and the potentially cost-effective circuitry-based applications in flexible electronics,[21] such as flexible radio-frequency identity tags,[22] smart labels,[23] sensor devices,[24] and simple displays,[25] will benefit from this fast development. However, it is still far from satisfactory for real applications. The focus of recent attention has been devoted to improving device performance and stability, to reducing the fabrication cost, to exploring new applications, and to developing simple fabrication techniques. Overcoming these challenges relies on the development of novel organic

semiconductors and optimization of devices.

1.3.2 Basic principles of field effect transistors

The concept of the thin film transistor (TFT) was first introduced by Weimer in 1962.[26] This structure is well adapted to low conductivity materials, and is now currently used in amorphous silicon transistors. As seen in Figure 1.2, the source and drain electrodes form ohmic contacts directly to the conducting channel. Unlike both the structures described above, there is no depletion region to isolate the device from the substrate. Low off current is only guaranteed by the low conductivity of the semiconductor. A second crucial difference to the metal–insulation–semiconductor field-effect transistor (MISFET) is that, although the TFT is an insulated gate device, it operates in the accumulation regime and not in the inversion regime. For this reason, care has to be taken when transferring the equations of the drain current from the MISFET to the TFT. In fact, the absence of a depletion region leads to a simplification of the Equation as the following:

$$I_d = \frac{W}{L}\mu C_i(V_G - V_T - \frac{V_D}{2})V_D \quad (7)$$

Here, the threshold voltage is the gate voltage for which the channel conductance (at low drain voltages) is equal to that of the whole semiconducting layer.

1.3.3 The important parameters

1) Mobility

The current-voltage characteristics in the different operating regimes of

field-effect transistors can be described analytically assuming the gradual channel approximation. That is, the field perpendicular to the current flow generated by the gate voltage is much larger than the electric field parallel to the current flow created by the drain voltage.

In the linear regime, the drain current is directly proportional to V_G, and the field effect mobility in the linear regime (μ_{lin}) can be extracted from the gradient of I_D versus V_G at constant V_D.

$$I_d = \frac{W}{L} C_i \mu \left(V_G - V_T - \frac{V_D}{2} \right) V_D, \; V_D < V_G - V_T \tag{8}$$

In the saturation regime, the channel is pinched off when $V_D = V_G - V_T$. The current cannot increase anymore and saturates. The square root of the saturation current is directly proportional to the gate voltage.

$$I_{Dsat} = \frac{W}{2L} C_i \mu (V_G - V_T)^2, \; V_D > V_G - V_T \tag{9}$$

$$\sqrt{I_{Dsat}} = \sqrt{\frac{W}{2L} C_i \mu} (V_G - V_T) \tag{10}$$

Equation (10) predicts that plotting the square root of the saturation current against gate voltage would result in a straight line. The mobility is obtained from the slope of the line, while the threshold voltage corresponds to the extrapolation of the line to zero current. However, in the saturation regime, the density of charge varies considerably along the conducting channel, from a maximum near the source to practically zero at the drain. As will be seen in the following, the mobility in organic semiconductors is not constant, rather, it largely depends on various parameters, which include the density of charge carriers, with the consequence that in the

saturation regime, the mobility is not constant along the channel, and the extracted value only represents a mean value. For this reason, it is often more judicious to extract the mobility in the linear regime, where the density of charge is more uniform. This is usually done through the so-called transconductance g_m,[27] which follows from the first derivative of Equation (3) with respect to the gate voltage.

$$g_m = \frac{\partial I_D}{\partial V_G} = \frac{W}{L} C_i \mu V_D \quad (11)$$

This equation assumes that the mobility is gate voltage independent. However, the mobility is gate voltage dependent. Under such circumstances, Equation (5) should contain an extra term involving $\partial\mu/\partial V_G$, so that its use is limited to cases where the mobility is slowly varying with the gate voltage. Furthermore, the method is very sensitive to limitations of charge injection and retrieval at source and drain electrodes.

2) Current on/off ratio

Another important parameter of FETs that can be extracted from the transfer characteristics is the current on/off ratio, which is the ratio of the drain current in the on-state at a particular gate voltage and the drain current in the off-state (I_{on}/I_{off}). For clean switching behavior of the transistor, this value should be as large as possible. In situations where contact resistance effects at the source-drain electrodes can be neglected, the on-current mainly depends on the mobility of the semiconductor and the capacitance of the gate dielectric. The magnitude of the off-current is determined by gate leakage, especially for unpatterned gate electrodes and semiconductor layers, by the conduction pathways at the substrate interface, and by the bulk conductivity of

the semiconductor, which can increase due to unintentional doping.[28]

3) Threshold voltage

Threshold voltages can originate from several effects and depend strongly on the semiconductor and dielectric used. Built-in dipoles, impurities, interface states, and, in particular, charge traps contribute to the threshold voltage.[29] Note that, independent of the cause of V_{th}, it can be reduced by increasing the gate capacitance and thus inducing more charges at lower applied voltages. The threshold voltage is not necessarily constant for a given device. When organic transistors are operated for an extended time, V_{th} tends to increase. This bias stress behavior has a significant effect on the applicability of organic transistors in circuits and is presently under intense investigation.[30] A shift of the threshold voltage on the time scale of current-voltage measurements causes current hysteresis (usually the forward scan shows higher currents than the reverse scan). Large stable threshold shifts, e.g., induced by polarization of a ferroelectric gate dielectric, can be used in organic memory devices.

1.4 Review of the development of semiconductor materials in OFETs

The mobilities of organic semiconductors have achieved significant progress in OFETs from the initially reported 10^{-5} $cm^2V^{-1}s^{-1}$ for polythiophene in 1986[31] to 10 $cm^2V^{-1}s^{-1}$ for present diketopyrrolopyrrole (DPP) based polymers[32]. The high mobility of organic semiconductors over conventional amorphous silicon indicates large

potential application of organic electronic devices. In the last two decades, the p-type semiconductor materials have achieved much progress because of their easy design and synthetic approach. However, the development of n-type organic semiconductors still lags behind that of p-type organic semiconductors due to low device performance, ambient instability, and complex synthesis. Owing to their important roles in organic electronics such as p–n junctions, bipolar transistors, and complementary circuits, it is desirable to develop stable n-type semiconductor materials with high charge carrier mobility for organic field effect transistors.

1.4.1 P-type materials

P-type organic semiconductors mainly contain acene, heteroacene, as well as their correlated oligomers and polymers, and two-dimensional disk-like molecules. Several comprehensive reviews have given detailed information about these compounds. Some representative p-type semiconductors are shown in Chart 1.1.

Pentacene as the benchmark of organic semiconductors was first reported in 1970s, but the numerous OFETs applications were only conducted recently.[33] With strong intermolecular interactions and herringbone packing motif, pentacene exhibited efficient charge transport. Hence, polycrystalline thin film of pentacene and tetracene showed surprisingly high mobility approaching 0.1 $cm^2V^{-1}s^{-1}$[34] and 3.0 $cm^2V^{-1}s^{-1}$[35], respectively. The substituted tetracene derivative rubrene showed the highest charge carriers mobility with 20 $cm^2V^{-1}s^{-1}$ for single crystal device in the FET

configuration.[36] This implies that the conjugated acene is a good building block for the p-type semiconductors. Later on, more core-extended hexa-*peri*-benzocoronenes (HBC) containing two-dimensional (2D) aromatic core was reported and showed typically discotic columnar liquid crystalline phases. As a result, the HBC showed enhanced mobility along the column due to the solid state organization. Moreover, HBC-based OFETs by zone casting method exhibited a high mobility up to $0.01 cm^2V^{-1}s^{-1}$.[37] The chemistry based on acene has paved the way for designing efficient p-type semiconducting materials.

The sulfur containing heteroacenes and their derivatives constitute another large group of p-type aromatic hydrocarbons, as shown in Chart 1.1. The thienoacenes and their derivatives were also synthesized and investigated as semiconductors for p-type materials. The tetrathienoacene with aryl groups had a higher mobility up to 0.14 $cm^2V^{-1}s^{-1}$ by vapor deposition.[38] The asymmetric oligoacene such as the tetraceno-thiophene were also synthesized and showed similar mobility compared to their centrosymmetric counterparts processed in the same conditions.[39] The sulfur-sulfur interaction in the packing motif was believed to enhance the charge carrier transport. The introduction of sulfur and other heteroatoms induced different energy alignments and crystal packing, which promotes the development of p-type materials.

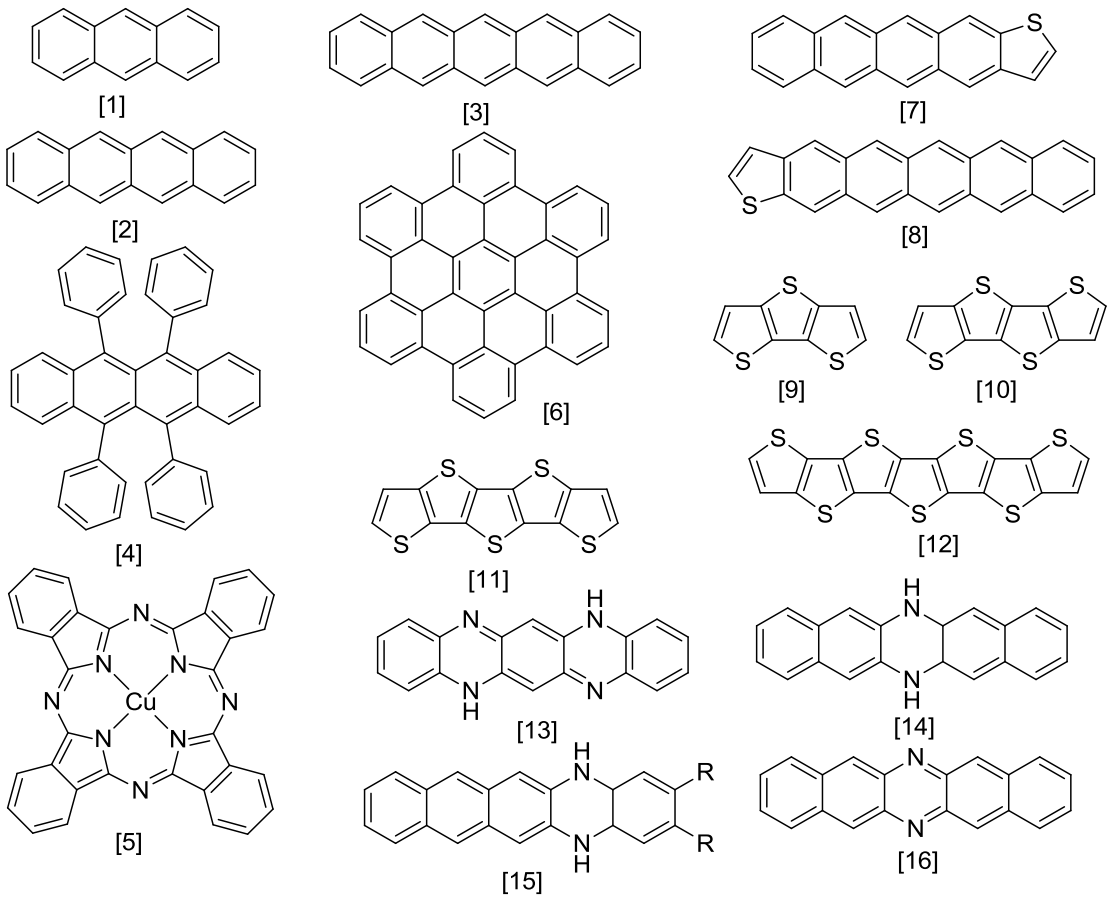

Chart 1.1. Chemical structures of some p-type semiconducting materials.

1.4.2 N-type materials

The N-type organic semiconductors have received much attention due to its important roles for p-n diodes, bipolar transistors and complementary circuits etc. To date, n-type organic semiconductors with high mobility are relatively rare and significantly lagging behind p-type semiconductors, and most of the n-type materials are still air unstable in ambient conditions due to its high lowest unoccupied molecular orbital (LUMO) energy level. De Leeuw (1997) reasoned that the air unstable problem is due to redox reaction with oxygen and water.[40] Based on this result, we can calculate the LUMO energy level and it should be lower than -3.97 eV

in order to be stable towards water and oxygen. N-type organic semiconductors mainly contain halogen-substituted n-type semiconductors that could be converted from p-type materials, perylene derivatives, naphthalene derivatives, and fullerene-based materials and so on (Chart 1.2).

The important n-type semiconductor material perfluoropentacene was first reported by Sakamoto et al.[41] This molecule adopted similar crystal packing to pentacene, and transistors fabricated from vacuum deposited films showed a high mobility up to 0.11 $cm^2V^{-1}s^{-1}$ and an on/off ratio of 10^5. It was thought that attaching fluorine atoms could lower the LUMO energy level of this compound. However, the LUMO energy level is not low enough to make the OFET device stable in the ambient condition. Similarly, the 2,5,8,11,14,17-hexafluoro-hexa-*peri*-hexabenzocoronene was synthesized by Kikuzawa *et al*. from hexakis(4-fluorophenyl)benzene.[42] This fluorinated compound was also suitable for the fabrication of n-channel transistors due to the decreased LUMO energy level, showing a mobility of 1.6×10^{-2} $cm^2V^{-1}s^{-1}$ and an on/off ratio of 10^4. Based on these results, they showed that the halogen substitution is a proper way to obtain n-type semiconductors.

Naphthalene diimide and perylene diimides derivatives are two of the most studied n-type materials used in OFETs. Simple naphthalene and perylene diimides can be prepared from bisanhydrides and primary amines. Generally, the behaviors of aromatic diimide in transistors show n-type character due to imide functionalization. Then, cyano or halogen was introduced to improve the air stability. Naphthalene

diimide substituted with electron-withdrawing CN groups at the core position was reported by Jones et al..[43] This molecule showed a mobility as high as 0.11 $cm^2V^{-1}s^{-1}$ as well as good ambient stability compared to unsubstituted compound. Cyano substituted perylene diimide was also reported by the same group.[44] The good air stability was also observed which indicates that cyano substituent is another efficient way to lower the LUMO energy level and achieve stable n-type materials. Later on, the core-expand NDI bearing two 2-(1,3-dithiol-2-ylidene)malonitrile moieties at the core needs to be mentioned due to its good solution processability and good air stability.[45]

Based on these results, it could be an efficient way to achieve stable n-type materials by combining imide functionalization and cyano or halogen substitutions. Electron deficient aromatic diimides have attracted increasing attention as promising n-type semiconductors for OFETs. The materials of this class showed not only highly planar conjugated backbone, but also easily tunable electronic properties through core and imide-nitrogen substituents with electron withdrawing groups and alkyl chains, respectively.

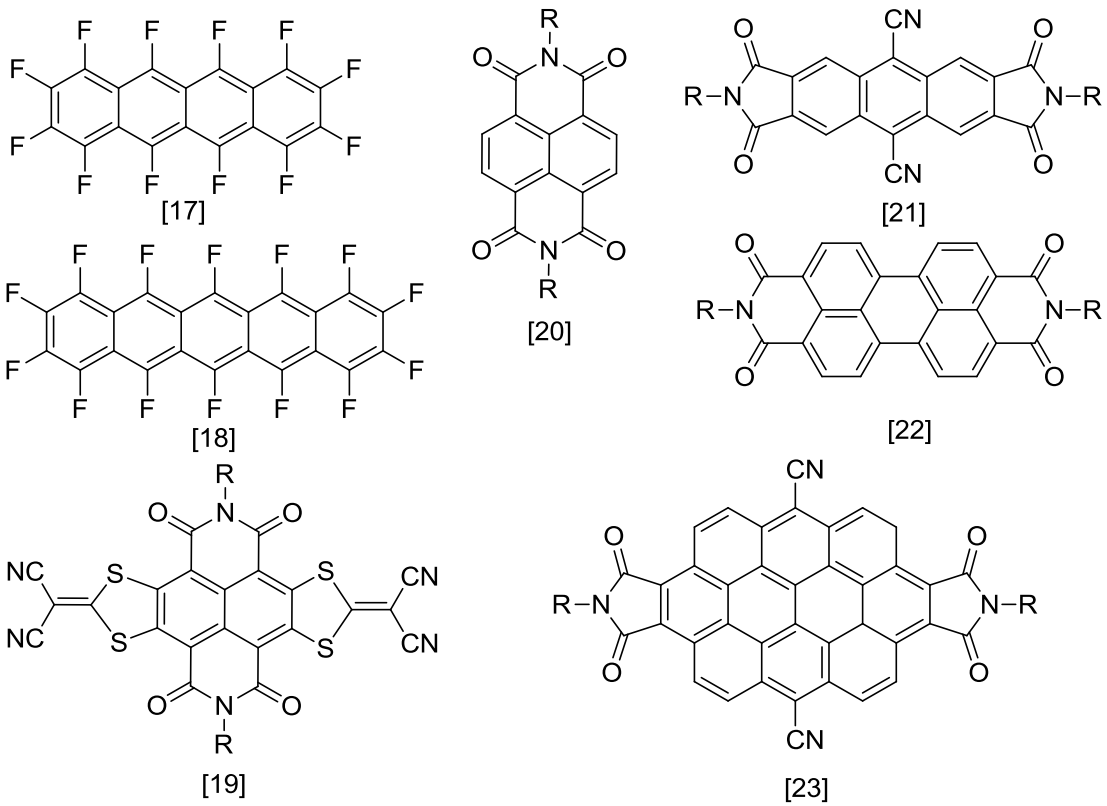

Chart 1.2 Chemical structures of some n-type semiconducting materials.

1.5 Semiconductor alignment technique

Depositing of crystalline organic semiconductors with controlled in-plane orientation is one important issue for high performance OFETs. It is generally accepted that charge transport in organic materials occurs via the hopping mechanism, which depends on the degree of orbital overlap between the molecules. Since charge carriers are preferentially transported along the π–π stacking direction in organic semiconductors, macroscopically aligned organic films have potentially higher mobilities, and provide more unusual properties, such as optically and electrically anisotropic characteristics. Therefore, many deposition techniques have been investigated for patterning and alignment of organic semiconductors.[46] The techniques

mainly contain 1) mechanical forces alignment, such as friction-transfer, nanoimprinting, and the Langmuir-Blodgett (LB) technique; 2) depositing the organic semiconductors directly on the alignment layers prepared by different methods, such as rubbing, and photoirradiation; 3) growing the organic semiconductors on inorganic single crystals; 4) using magnetic or electric-field induced alignment; 5) using solution processed technique to align organic semiconductors on isotropic substrates.

Among the solution processing techniques, the traditional techniques such as spin coating and drop casting cannot control the thin film orientation. Therefore, some methods have been used to overcome this issue. For example, zone-casting offers a route to control the orientation of the deposited layers.[47] In this process, a continuously supplied solution is spread by means of a nozzle onto a moving support. The solution and the support are thermally controlled. Under appropriate rates of solvent evaporation and solution supply, a stationary gradient of concentration is formed within the meniscus, which results in directional crystallization. Dip-coating is another technique to give a better thin film alignment in solution processed devices.[48] This process can be controlled by the substrate lift rate, solvent evaporation, and capillary flow. The drying speed which influences the thin film morphologies can be quantitatively controlled during the dip-coating process by adjusting the substrate lifting rate.

Solution-sheared deposition is a recently developed approach that can deposit highly crystalline and aligned thin films on isotropic substrates.[49] This method is

related to doctor blading, which employs a blade to distribute a viscous solution over a substrate. A small volume of an extremely diluted organic solution is sandwiched between two preheated silicon substrates which move relatively to each other at controlled speed. The bottom wafer is the device substrate, and the top wafer acts as the shearing tool, and is modified to be hydrophobic. The motion of the wafers exposes a liquid front that rapidly evaporates to produce a seeding film containing multiple crystal grains. These crystals are nucleation sites for the remaining molecules in solution, and thus propagate along the direction of the shearing.

1.6 Metal oxide based thin film transistors

Organic and metal oxide semiconductors are two types of materials that are currently being investigated as potential alternatives to amorphous silicon used in new electronic device applications. Organic semiconductors can transport both holes and/or electrons, however, most of the organic semiconductors reported to date are p-type semiconductors. While only relatively few examples of solution processed n-type semiconductors that exhibit competitively high performance and environmental stability. This problem has hindered the development of low cost, all organic complementary logic circuits. Compared to n-type organic semiconductors, n-type metal oxide possesses better device performance and better air stability due to its intrinsic doping. Moreover, n-type metal oxide semiconductors are advancing rapidly and outperform organic electronics within only a few years in terms of charge

carrier mobilities. However, oxide semiconductors suffer from one main drawback which is the distinct lack of hole transporting compounds with appreciable charge carrier mobilities. The problem lies in the deep valence band edge which is typically around -7 eV and localised nature of the hole transport states which comprising of oxygen 2p orbitals. Up to now, a lot of approaches have been reported to develop new material systems and to dope the intrinsic oxide. Unfortunately, most of them are not successfully. In the future, the hybrid materials should be the future direction which combines the advantages of each material.

1.6.1 Recent Progress of n-Type Oxide TFTs

ZnO, IGZO and others including ZTO, ITO, IZO, IZTO and IGO have been extensively studied recently.[50] In the binary, ternary and quaternary compounds, the thin film composition has significantly effect on the electrical properties. For the thin film deposition, most used deposition technique is sputtering (more than 90%), and low cost solution processed technique is desirable.

Solution processed technique is compatible with the printing process which showed much lower cost compared to the vacuum based technique. There are two types of metal oxide precursors mostly used, nanoparticle dispersion and molecular precursor. For the nanoparticle dispersion route, the thin film showed some instability due to the large surface area. For sol-gel based precusor, it usually needs high temperature annealing (above 400 ^{o}C) to remove carbon impurities. Recently, several methods have been used to develop low temperature annealed metal oxide thin film,

such as "sol-gel on chip", combustion reaction, and using deep UV to convert the metal oxide precursor to final ZnO thin film.[51]

1.7 Objectives and Outline of the thesis

In view of the above review, it is well-known that much progress has been made in developing organic and metal oxide semiconductor materials in the past two decades. Meanwhile, for large scale fabrication of low-cost devices, solution based film deposition processes at low temperatures with high charge mobility are highly desirable. Currently, there are only few studies on solution processable air-stable high performance organic n-type semiconductor, large area semiconductor thin film alignment, low-temperature solution deposited metal oxide, and some important issues still need further investigation.

1) The energy level has important effects on the device stability. Therefore, how to correlate the energy level with the device stability needs to be further discussed in terms of thermodynamic stability and kinetic stability aspects.
2) The structure-morphology-property relationships of n-type aromatic diimides are still unclear, so it is necessary to give detailed investigations about this study.
3) The surface morphology is critically related with device performance, and detailed studies about the thin film alignment should be given.

4) N-type metal oxide is an alternative to n-type organic semiconductors, however, the process conditions and doping processes are still needed to give a detailed study.

The main aim of this study was to investigate the structure-morphology-properties relationships of the organic semiconductors from the structural modification, energy levels, device process conditions, thin film alignment and replacement by n-type metal oxide.

The results of this present study could enrich the study of this area, and may provide guidelines for designing new n-type air-stable aromatic diimide compounds, thin film alignment process, and synthesis of metal oxide. This thesis focuses on structure design, energy level analysis, and device applications to systematically study the structure-morphology-property relationships of the n-type semiconductors. The thin film alignment and n-type metal oxide will also be investigated in this study, and may involve many engineering issues. Since engineering issues are not the focus of this study, they will only be discussed briefly.

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Chapter 2 Effects of Energy Level on Air Stability of N-Type Naphthalene Diimide Semiconductor Materials through Stepwise Cyanation

2.1 Introduction

The N-type organic semiconductors have received much attention due to its important roles for p-n diodes, bipolar transistors and complementary circuits etc.[1] To date, n-type organic semiconductors with high mobility are relatively rare and significantly lagging behind p-type semiconductors, and most of the n-type materials are still air unstable in ambient conditions due to its high lowest unoccupied molecular orbital (LUMO) energy level. Electron deficient aromatic diimides have attracted increasing attention as promising n-type semiconductors for OFETs. The materials of this class showed not only highly planar conjugated backbone, but also easily tunable electronic properties through core and imide-nitrogen substituents with electron withdrawing groups and alkyl chains, respectively. Among them, naphthalene diimide (NDI)[2] based molecules have been intensively investigated as n-type semiconductors for organic field effect transistors (OFETs). The interest stems from the early observation of the n-type behavior[2c] as well as the versatile tuning of their chemical and electronic properties by varying the substituents at the imide position[3] or on the naphthalene

backbone.[4] In order to achieve applicable electron transporting materials with high charge carrier mobility and good air stability, introduction of electron-withdrawing cyano groups into the NDI framework has become an important strategy.[5]

2.2 Results and discussion

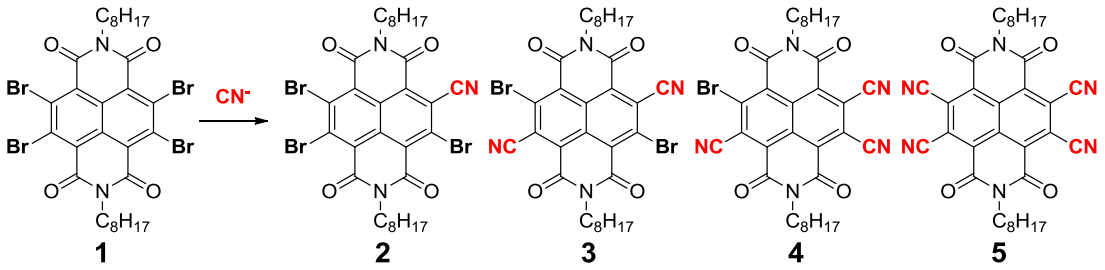

Figure 2.1 The chemical structures of compound **1-5**. (Synthesis was done by Dr. Ye Qun)

In this section, we studied the step cyanated NDIs for air-stable n-channel OFETs. The chemical structures of compounds **1-5** are shown in Figure 2.1. The electrochemical properties of compounds **1-3** were investigated by cyclic voltammetry (Figure 2.2). **2** exhibited two reversible reduction waves with half-wave potential $E_{1/2}^{red}$ at -0.66 and -1.11 V (vs. Fc^{+}/Fc). **3** showed two similar reversible reduction waves with $E_{1/2}^{red}$ at -0.45 and -1.00 V, and one quasi-reversible reduction wave with $E_{1/2}^{red}$ at -1.56 V. **1** showed three quasi-reversible reduction waves with $E_{1/2}^{red}$ at -0.89, -1.26 and -1.48 V. The LUMO energy levels of **1**, **2** and **3** were estimated to be -4.02, -4.21 and -4.42 eV, respectively, based on the onset potential of the first reduction wave. It was worth mentioning that after replacement of one bromine atom with a cyano group, the LUMO energy level was reduced by ca. 0.2 eV,

showing a good linear relationship with the number of CN groups (Figure 2.2).

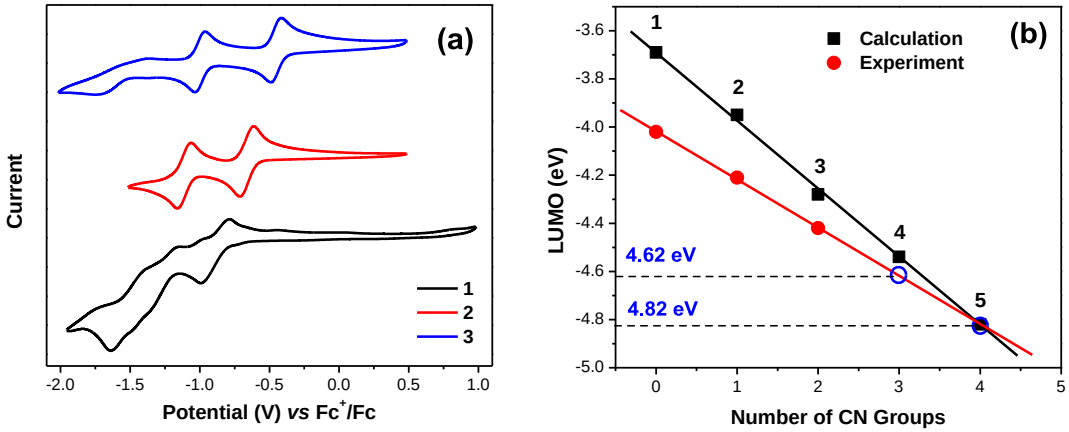

Figure 2.2 (a) Cyclic voltammograms of **1-3** measured in dry CH_2Cl_2; (b) plots of the calculated (DFT at B3LYP/6-31G* level) and experimental LUMO energy levels of **1-5** with the number of CN groups.

DFT calculations have been performed at the B3LYP/6-31G* level of theory, as implemented in the *Gaussian 09* program package. The geometries of **1-5** were fully optimized in gas phase using the default convergence criteria without any constraints and confirmed by frequency calculations. The calculated HOMO and LUMO profiles and energy level data are also shown in Figure 2.3. DFT (B3LYP/6-31G*) calculations predicted that the LUMO energy levels of **1-5** are -3.69, -3.95, -4.25, -4.54, and -4.82 eV (Figure 2.3), which also exhibit a good linear relationship with the number of CN groups (Figure 2.2). Thus, it is reasonable to make a linear extrapolation of the experimental plot and the LUMO energy levels of **4** and **5** are estimated to be -4.62 and -4.82 eV, respectively. The very low-lying LUMO energy levels reflect the highly electron-deficient nature of **4** and **5**, which would be the most possible origin of their instability.

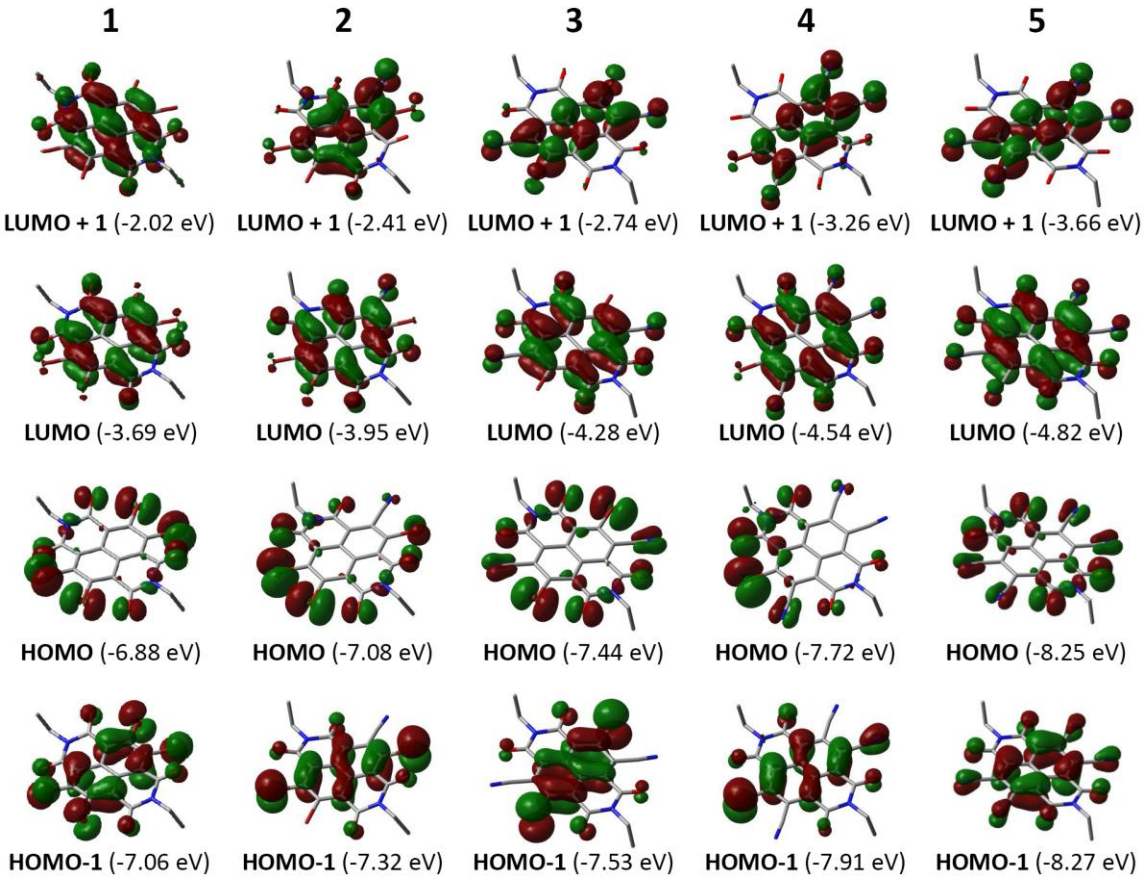

Figure 2.3 Calculated HOMO and LUMO orbital profiles and energy levels for molecules **1-5**.

Field effect transistors with **1-3** as active component were fabricated in a bottom-gate, top-contact configuration. Thin film of semiconductor materials was deposited at different substrate temperature T_d by vapor deposition onto p+-Si wafer with 200 nm of thermally grown SiO_2 as the dielectric layer. The SiO_2 substrate was modified by either octadecyltrimethoxysilane (OTMS) or CYTOP (poly(perfluorobutenylvinylether)) amorphous fluoropolymer or without any modification. The typical transfer and output curves measured in N_2 on OTMS modified substrate with T_d = 60 ^oC are shown in Figure 2.4 and the device characteristics data at various T_d temperatures are shown in Table 2.1. All the devices exhibit typical n-channel behavior and the highest FET electron mobility measured in

N_2 is 0.018, 5.1×10^{-4} and 0.050 $cm^2V^{-1}s^{-1}$ for **1**, **2** and **3**, respectively. The electron mobilities are dependent on T_d and dielectric surface treatment. For example, the mobility of **3** increased from 0.018 $cm^2V^{-1}s^{-1}$ at RT to 0.050 $cm^2V^{-1}s^{-1}$ for thin film deposited at 100 ^oC. The thin film on OTMS/SiO_2 exhibited higher performance (0.050 $cm^2V^{-1}s^{-1}$) compared to bare SiO_2 substrates which only gave a low mobility of 2.4×10^{-5} $cm^2V^{-1}s^{-1}$. The threshold voltage (V_{th}) shifted toward to the negative value with the increase of the number of cyano groups from **1** to **2** and to **3**, indicating the higher the electron affinity, the easier to create mobile electrons at low gate bias. The I_{on}/I_{off} ratio of all devices showed a high valve of 10^4-10^6 compared to other high affinity materials. The reason that I_{on}/I_{off} was enhanced for OTMS treated substrate is due to an efficient decrease in I_{off} compared to the bare SiO_2 which gives a lower I_{on}/I_{off} ratio (10^2-10^3).

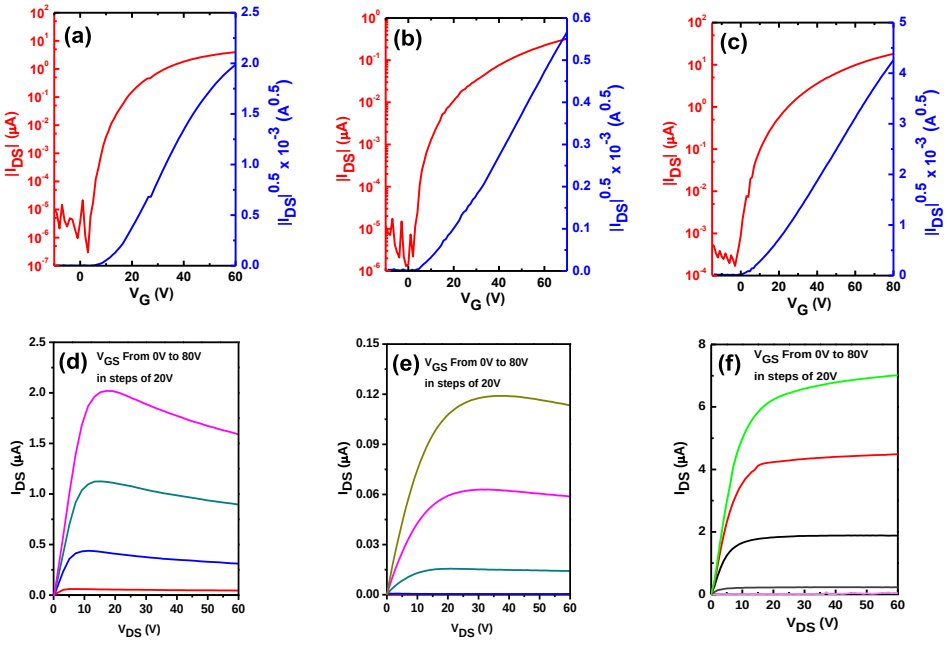

Figure 2.4 Representative OFET transfer and output characteristics of **1** (a, d), **2**(b, e), and **3** (c, f) thin films (T_d = 60 ^oC) on OTMS modified substrates in N_2.

Table 2.1 OFET characteristics for 1-3 measured in N2 on OTMS modified substrates.

		In N_2			In air		
	T_d (^oC)	$\mu(e)$ [$cm^2V^{-1}s^{-1}$]	V_T [V]	On/off	$\mu(e)$ [$cm^2V^{-1}s^{-1}$]	V_T [V]	On/off
1	RT	0.011	19-24	10^6	4.0×10^{-5}	44-48	10^4
	60	0.018	15-20	10^6	1.2×10^{-5}	46-49	10^3
	100	0.012	14-19	10^5	4.3×10^{-5}	50-56	10^3
2	RT	3.7×10^{-4}	12-18	10^5	4.5×10^{-5}	3-7	10^4
	60	3.9×10^{-4}	13-17	10^5	1.1×10^{-4}	6-9	10^4
	100	5.1×10^{-4}	12-17	10^5	3.2×10^{-5}	4-9	10^4
3	RT	0.018	3-6	10^5	1.9×10^{-3}	-1-4	10^4
	60	0.036	3-7	10^5	5.3×10^{-3}	3-5	10^4
	100	0.050	4-7	10^4	9.0×10^{-3}	2-4	10^4
	140	0.031	3-6	10^3	2.0×10^{-3}	1-3	10^3

Thin films of **1**-**3** deposited at different T_d exhibited a similar X-ray diffraction pattern which can be correlated to a lamellar packing mode (Figure 2.5) with a $d_{(001)}$ spacing of 17.0, 17.8, and 18.5 Å, respectively. Thin film of **2** showed less intense and broader diffraction peaks compared with **1** and **3**, indicating a less ordered microstructure. Atomic force microscopy (AFM) images revealed highly crystalline surface microstructure and the crystallite size tended to increase with increasing T_d for all compounds (Figure 2.6), which explains the higher mobility at the higher substrate temperature due to minimized grain boundaries. Thin film of **2** exhibited smaller grains and much more grain boundaries, which limit the efficient charge transport and correspond to lower charge carrier mobility.

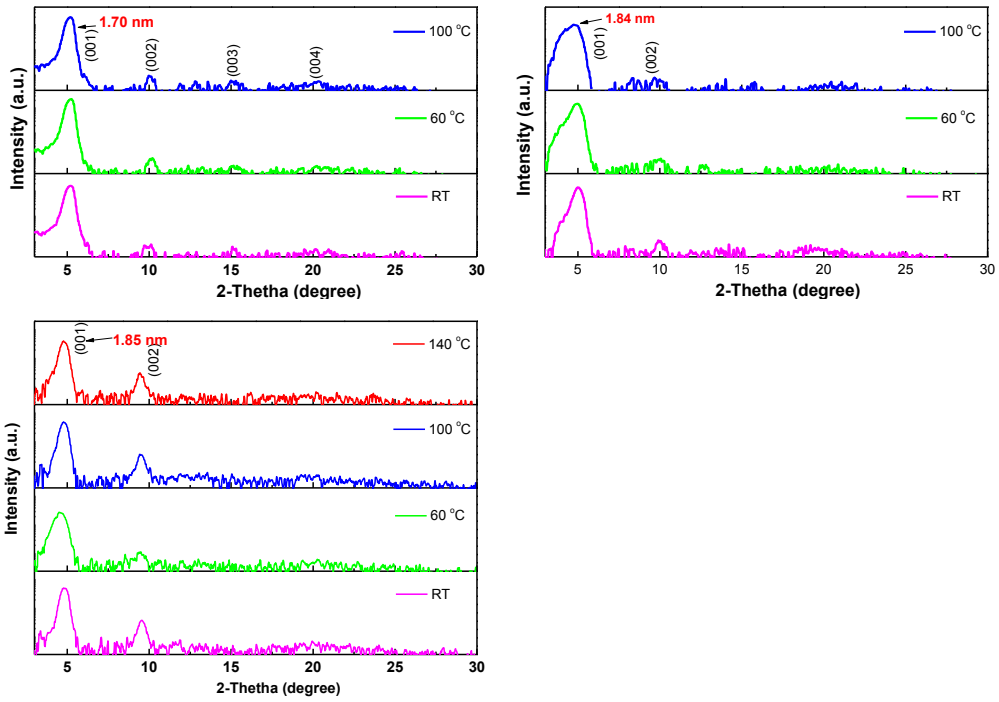

Figure 2.5 X-ray diffraction patterns in logarithmic scale of the thin film of **1-3** deposited at the indicated substrate temperature on OTMS modified SiO_2 substrates.

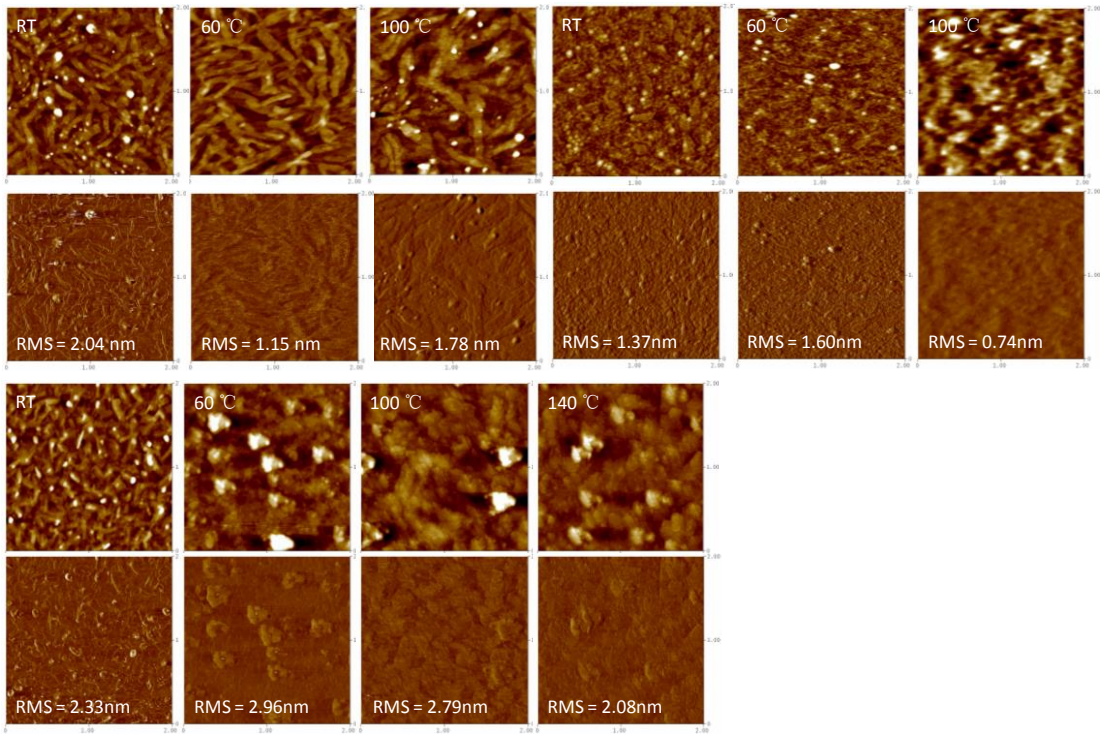

Figure 2.6 Tapping-mode AFM images of the thin film of **1-3** deposited at the indicated substrate temperature on OTMS modified SiO_2 substrates.

The OFET devices operated in ambient conditions showed different degradation (Table 2.1). **1** with the lowest electron-affinity exhibited the largest device variations (~1000×) while **3** with the highest electron-affinity showed a smaller decrease in charge carrier mobility by a factor of ~10×. This trend gave a sign that the n-type ambient sensitivity could be decreased with the increase of electron affinity. The V_{th} of **1** was significantly shifted to positive voltage with about 15~30 V due to electron traps at the interface between the semiconductor and dielectric. However, the V_{th} of **2** and **3** were both slightly shifted to negative voltage perhaps due to unintentional doping by electron-rich chemical functionalities and/or the local electric field.[5] The electron trap sites like silanol groups on SiO_2 could be neglected when the LUMO of semiconductor is lower than -3.8 eV,[7] which may also explain the good device stability of **2** and **3**.

OFETs on CYTOP/SiO_2 bilayer substrates showed comparable performance to that on OTMS-modified substrates, showing the highest electron mobilities of 0.017, 5.1×10^{-4}, and 0.047 $cm^2V^{-1}s^{-1}$ for **1**, **2** and **3**, respectively, when measured in N_2 (Figure 2.7 and Table 2.2). The OFET devices also gave a more positive V_{th} and a larger I_{on}/I_{off} ratio. When the devices were operated in ambient conditions, the mobility showed a smaller decrease (~2×). Thin films of **1-3** deposited on CYTOP/SiO_2 exhibited similar XRD pattern but with enhanced reflection intensity (Figure 2.8) compared to the OTMS/SiO_2 substrate, *indicating* more ordered packing. The surface morphology also changes slightly (Figure 2.9).

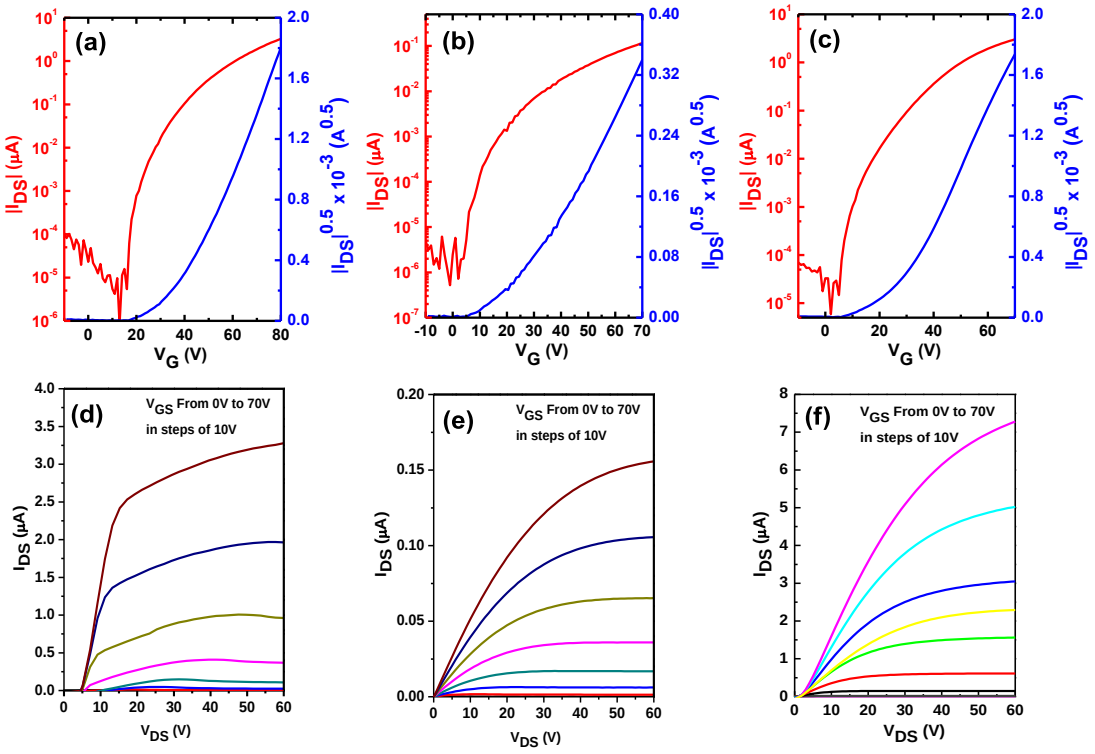

Figure 2.7 Representative OFET transfer and output characteristics of **1** (a, b), **2**(c, d), and **3** (e, f) thin films (T_d = 60 °C) on CYTOP modified substrates in N_2.

Table 2.2 OFET characteristics data for **1-3** measured in N_2 and in air on CYTOP modified substrates.

		In N_2			In air		
	T_d (°C)	μ(*e*) [$cm^2V^{-1}s^{-1}$]	V_T [V]	On/off	μ(*e*) [$cm^2V^{-1}s^{-1}$]	V_T [V]	On/off
1	RT	0.017	37-45	10^6	0.013	47-55	10^6
	60	0.018	39-47	10^6	0.01	46-54	10^5
	100	0.016	34-41	10^6	0.007	57-62	10^5
2	RT	2.8×10^{-4}	23-31	10^5	2.0×10^{-4}	27-33	10^5
	60	3.7×10^{-4}	16-24	10^5	3.6×10^{-4}	16-25	10^5
	100	5.1×10^{-4}	17-23	10^5	4.9×10^{-4}	20-25	10^5
3	RT	0.008	9-13	10^5	5.5×10^{-3}	14-23	10^4
	60	0.010	13-20	10^5	8.5×10^{-3}	17-24	10^5
	100	0.019	12-16	10^5	0.010	10-15	10^5
	140	0.047	14-18	10^5	0.018	11-16	10^6

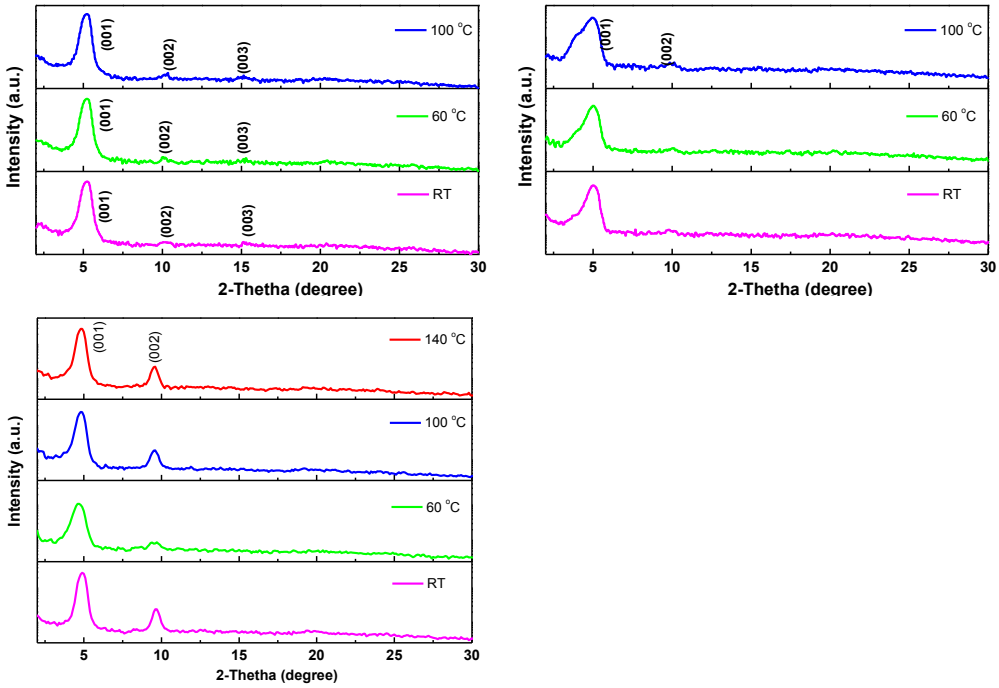

Figure 2.8 X-ray diffraction patterns in logarithmic scale of the thin film of **1-3** deposited at the indicated substrate temperature on CYTOP modified SiO_2 substrates.

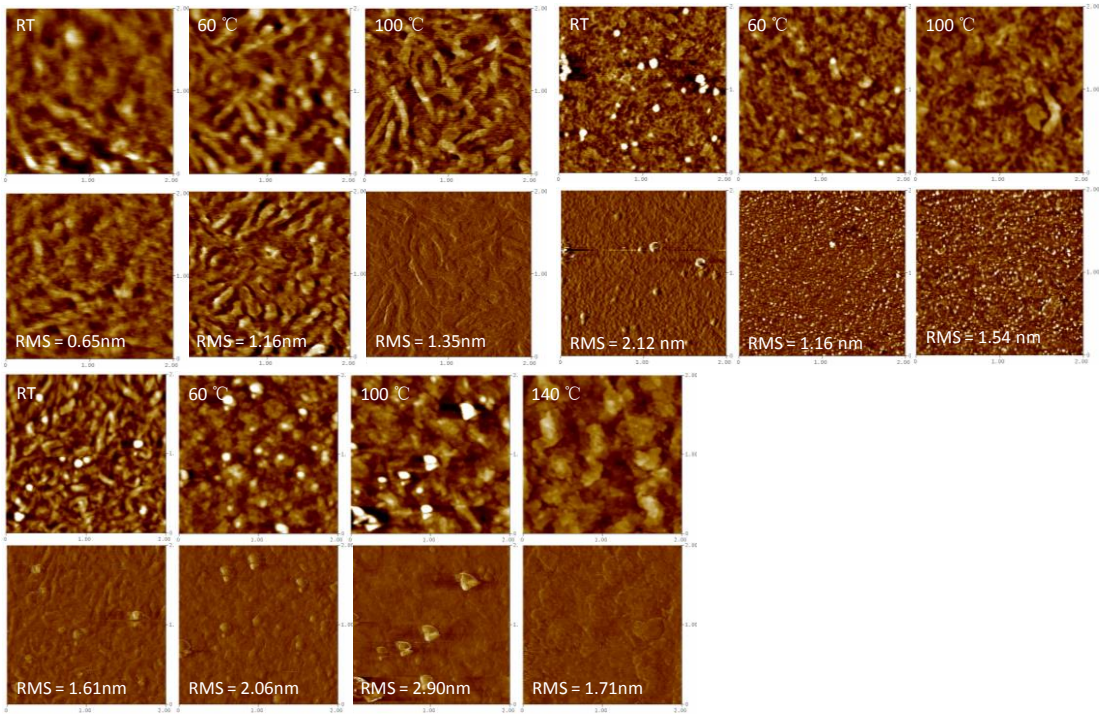

Figure 2.9 Tapping-mode AFM images of the thin film of **1-3** deposited at the indicated substrate temperature on CYTOP modified SiO_2 substrates (top: height mode; bottom: phase mode).

2.3 Experimental part

Top-contact, bottom-gate configuration was used for all OFETs devices. Thin films of semiconductors about 30 nm were deposited from vapor phase on p+-Si wafer with 200 nm of thermally grown SiO_2 as the dielectric layer. The wafers were cleaned with acetone and isopropanol, then immerse in a piranha solution for 8 minutes. Followed by rinsing with deionized water, and then spin casting with 3 mM OTMS solution in trichloroethylene and placed in an environment saturated with ammonia vapor for 7 hours at room temperature prior to semiconductor film deposition. The CYTOP/SiO_2 bi-layer dielectric was formed by spin coating (3000 rmp/s, 60s) the CYTOP solution (CTL-809M : CT-Solv.180 = 1:3) onto the cleaned SiO_2 substrates. The dielectric surface was characterized by water contact angle goniometer, and showed a highly hydrophobicity (112 °). The surface roughness was evaluated by tapping-mode AFM and gives an average RMS roughness of 0.40 nm. Finally, the capacitance of CYTOP/SiO_2 bi-layer dielectric was characterized by capacitance voltage measurement unit (4210-CVU) and gives a capacitance of 12.5 nF/cm^2, and the dielectric constant was estimated about 2.1~2.2. Semiconductor materials thin film were deposited at T_d = rt, 60, 100, 140 ^oC by vapour deposition (1×10^{-7} Torr, 0.2 Å/s). The devices were completed by depositing Au (60 nm thick) onto the thin films through a shadow mask with a channel width of 150 um and length of 4 mm. The thin films were characterized with OFET measurements, X-ray diffraction and tapping-mode atomic force microscopy. The FET devices were

characterized using a Keithley SCS-4200 semiconductor parameter analyzer in the N_2 atmosphere or in air. The FET mobility was extracted using the following equation in the saturation regime from the gate sweep: $I_D = W/(2L)C_i\mu(V_G-V_T)^2$; where I_D is the drain current, μ is the field-effect mobility, C_i is the capacitance per unit area of the gate dielectric layer (SiO_2, 200 nm, C_i = 17.2 nF cm^{-2}), and V_G and V_T are gate voltage and threshold voltage, respectively. W and L are respectively channel width and length. Tapping-mode Atomic Force Microscopy (TM-AFM) was performed on a Nanoscope V microscope (Veeco Inc.) X-ray diffraction (XRD) patterns of the thin film were measured on a Bruker-AXS D8 DISCOVER with GADDS X-ray diffractometer. Copper Kα line was used as a radiation source with λ = 1.5418 Å.

2.4 Conclusions

In summary, stepwise cyanation of tetrabromo-naphthalene diimide **1** gave a series of cyanated compounds **2-5**. The electron affinity showed a good linear relationship with the number of the cyano groups and the extremely low-lying LUMO energy level of **4** and **5** make them unstable to moisture. The mono- and di-cyanated NDIs **2** and **3** can be obtained as stable n-type semiconductors and used for air-stable n-channel OFETs with moderate electron mobilities. This research implies that on the way to search new high performance n-type semiconductors, we need find a good balance between the materials stability and device stability by careful control of the electron affinity. Most importantly, this study showed compound **3** could be a great

potential building block for constructing NDI-based semiconductor materials. Moreover, the stepwise control of cyanation method points out a way for synthesizing the high affinity n-type semiconducting materials.

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Chapter 3 Disc-like 7,14-Dicyano-ovalene-3,4:10,11-bis(dicarboximide) as a Solution Processible n-Type Semiconductor and the Effects of Device Processing on Electrical Performance

3.1 Introduction

Organic semiconductors have attracted intensive academic and commercial interest due to their intriguing optoelectronic properties and potential applications for electronics.[1] Among various building blocks for organic semiconductors, discotic liquid crystals (DLCs) typically comprising a rigid aromatic core and flexible peripheral chains have attracted growing attention.[2] These disc-like molecules offer the ability to self-assemble into columnar superstructures together with the self-healing of structural defects in mesophases, leading to high one-dimensional charge-carrier mobility along columns, while potentially being more readily processed from solution or from an isotropic melt. Various DLCs based on triphenylene,[3] hexabenzocoronene (HBC),[4] porphyrin,[5] and phthalocyanine[6] have been investigated and used as p-type semiconductors in electronic devices. N-type semiconductors based on disc-like molecules can be obtained by using similar design concept, thus naphthalene diimide[7] and perylenediimde (PDI) derivatives[8] have been successfully

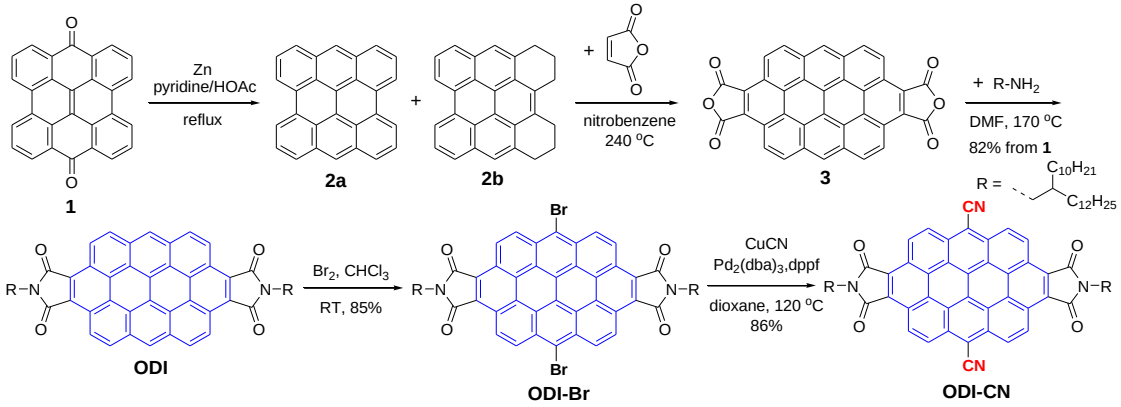
used for n-channel organic field-effect transistors (OFETs). However, in most cases, the thin films were made by vapor deposition technique and only recently, FET electron mobility of 0.08 cm^2/Vs was achieved for PDIs by solution processing.[8d] Larger size coronene diimide derivatives were also prepared and high space charge limited current (SCLC) mobilities were measured, but no FET mobility was reported.[9] It has been also proposed that increased core sizes could lead to stronger intermolecular interactions, and, hence, possibly increase charge carrier mobility.[10-11] Therefore, we are interested in exploring the potential of an even larger size aromatic molecule, namely ovalene, as a building block for solution processible n-type semiconductors. The oval-shaped ovalene[12] is an insoluble material due to strong intermolecular interactions. Soluble ovalene tetraesters exhibited hexagonal columnar LC phase,[13] but no OFET devices and charge carrier mobility data have been reported so far.

In this chapter, we report the first synthesis, physical characterizations and FET applications of ovalene-3,4:10,11-bis(dicarboximide) (ODI) and 7,14-dicyano-ovalene-3,4:10,11-bis(dicarboximide) (ODI-CN) (Scheme 3.1). In particular, the ODI-CN is supposed to be an appropriate n-type semiconductor based on the following considerations: (1) attachment of strong electron-withdrawing –CN and dicarboximide groups will significantly enhance the electron affinity; (2) introduction of branched dove-tailed alkyl chains will not only solubilize the insoluble ovalene core, but also lead to highly ordered columnar LC materials; (3) unlike other

high-symmetry DLCs substituted by insulating aliphatic chains (e.g. six-fold symmetric alkylated HBCs), ODI-CN has a C_2 symmetry and this makes inter-column charge transport more feasible.

3.2 Results and discussion

3.2.1 Organic field effect transistors based on ODI-CN



Scheme 3.1 Synthesis of ODI and ODI-CN (done by Dr. Li Jinling).

The Scheme 3.1 outlines the synthesis of ODI and ODI-CN. Treatment of bisanthenequinone 1 with zinc dust and acetic acid in refluxing pyridine gave a mixture of bisanthene 2 and partially hydrogenated bisanthene, which were used directly in the subsequent Diels-Alder reaction with maleic anhydride in refluxing nitrobenzene to afford crude ovalene dicarboxylic anhydride 3 as an insoluble material. Imidization of the 3 with 2-decyltetradecan-1-amine afforded the ODI in overall 82% yield for three steps. Bromination of ODI selectively took place at the most reactive 7,14- positions and gave the 7,14-dibromoovalene diimide (ODI-Br) in 85% yield. Pd(OAc)2-mediated cyanation of ODI-Br by using CuCN successfully

afforded ODI-CN in 86% yield.

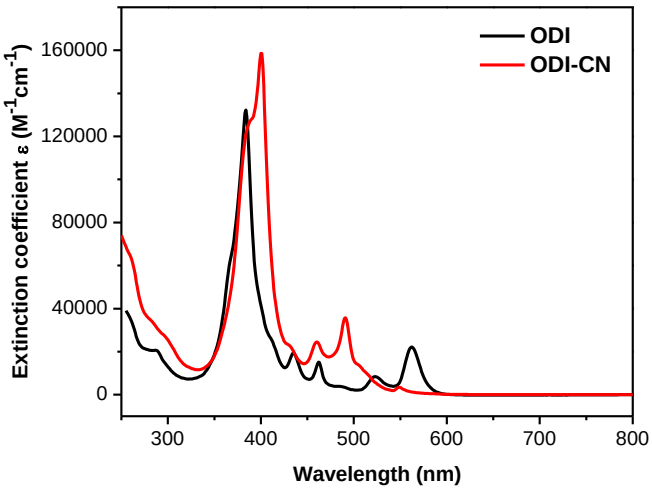


Figure 3.1 UV-vis absorption of **ODI** and **ODI-CN** in dilute chloroform solutions (concentration = $1x10^{-5}$ M for absorption spectra).

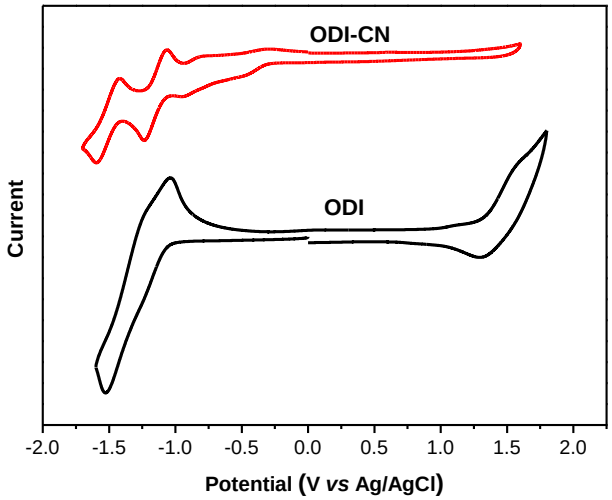


Figure 3.2 Cyclic voltammograms of **ODI** and **ODI-CN** in chlorobenzene with 0.1 M Bu_4NPF_6 as the supporting electrolyte.

ODI exhibits good solubility in normal organic solvents such as chloroform, toluene, THF and chlorobenzene etc.. ODI-CN shows relatively poor solubility in these common solvents at room temperature but it can be easily dissolved at elevated temperature. The longest absorption maxima of ODI and ODI-CN in chloroform are located at 560 and 548 nm, respectively (Figure 3.1). Cyclic voltammetry (Figure 3.2) revealed a low lying LUMO energy level (-3.90 eV) for ODI-CN, which is 0.76 eV

lower than that for ODI (-3.14 eV).

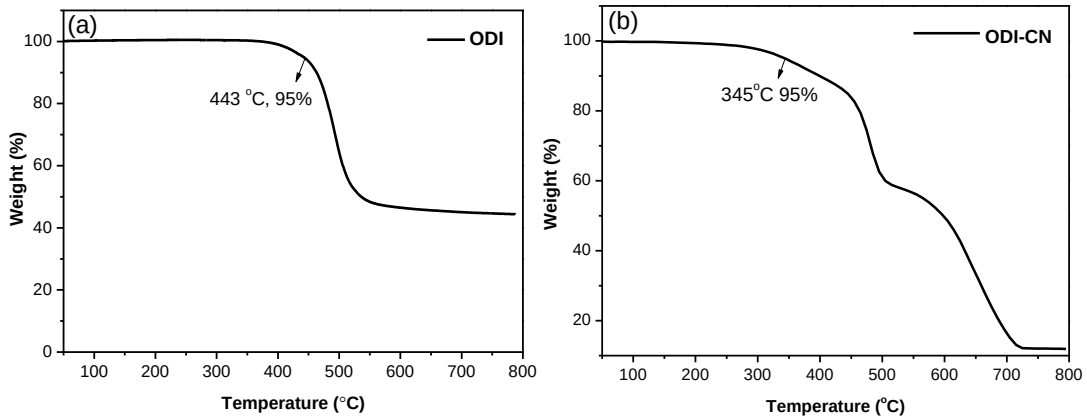


Figure 3.3 Thermogravimetric analysis (TGA) curves of **ODI** (a) **ODI-CN** (b).

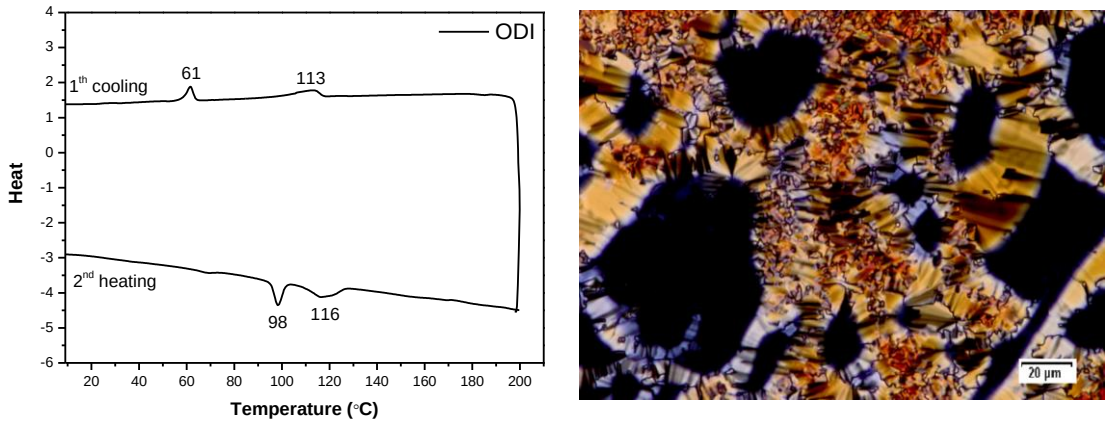


Figure 3.4 Differential scanning calorimetry (DSC) thermograms of **ODI** (second heating and first cooling scans are given, 10 °C min^{-1}under N_2, left) andpolarizing optical microscopy (POM) image of **ODI-CN_2** at 350 °C during heating.

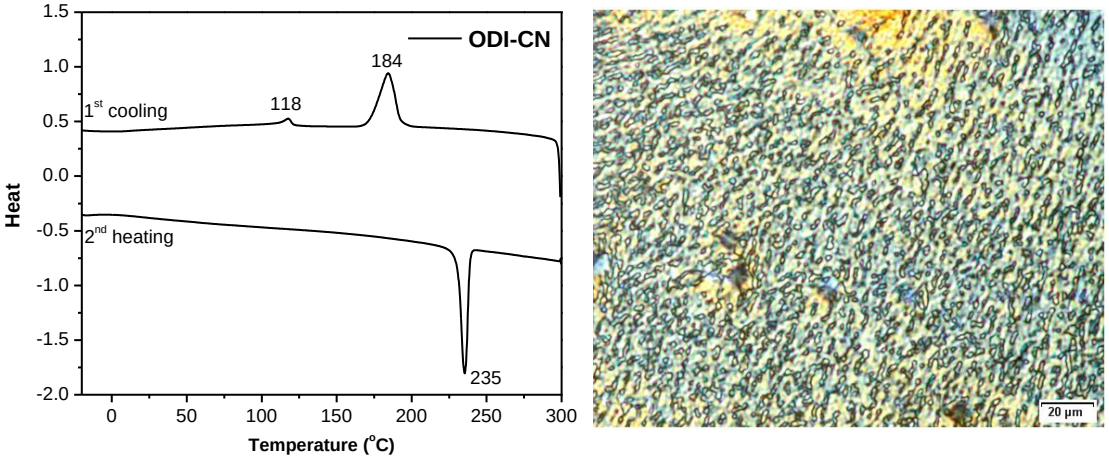


Figure 3.5 Differential scanning calorimetry (DSC) thermograms of **ODI-CN** (second heating and first cooling scans are given, 10 °C min^{-1}under N_2, left) and

polarizing optical microscopy image of **ODI-CN** at 300 ^{o}C during heating.

ODI exhibited higher thermal stability (decomposition temperature (T_d) = 443 ^{o}C) than ODI-CN (T_d = 345 ^{o}C) in N_2 atmosphere probably due to the relatively poor thermal stability of CN group (Figure 3.3). **ODI** showed a monoclinic plastic crystalline phase at room temperature and a hexagonal ordered columnar liquid crystalline phase between 98 and 116 ^{o}C (Figure 3.4). **ODI-CN** displayed a transition from plastic crystalline phase to liquid crystalline phase at 236 ^{o}C (Figure 3.5). Both ODI and ODI-CN do not enter isotropic phase below 500 ^{o}C, indicating very strong interactions between these large-size ovalene molecules.

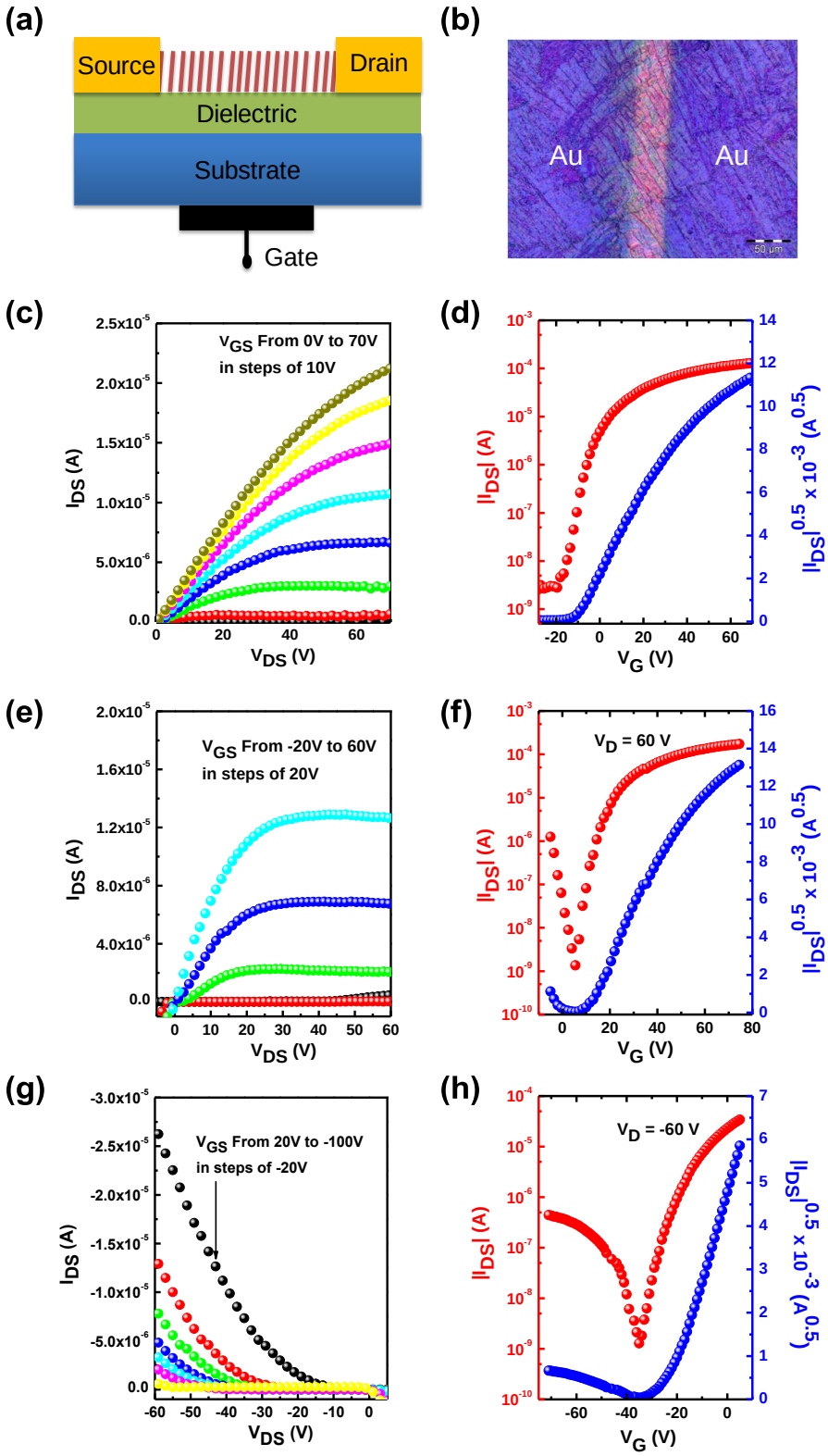


Figure 3.6 (a) the device structure used in this study. (b) the optical image of the device. Output (c, e, g) and transfer (d, f, h) characteristic of the OFETs based on ODI-CN thin films prepared by drop casting DCB solution onto OTMS-modified SiO_2/Si substrate followed by annealing at 230 ^oC. (c-d): measured in N2 (W/L = 500/50 um); (e-h): measured in air (W/L = 1000/50 um).

Table 3.1 Characteristics of ODI-CN based FET devices.

Run	solvents	surface	μ_{sat}^{max}	μ_{sat}^{ave}	V_T[V]	On/Off
1	$CHCl_3$	Bare[a]	0.036	0.02(0.004)	14	10^5-10^6
2	$CHCl_3$	OTS[a]	0.014	0.01(0.003)	15	10^5-10^6
3	DCB	Bare[a]	0.054	0.04(0.004)	13	10^5-10^6
4	DCB	OTS[a]	0.037	0.03(0.004)	13	10^5-10^6
5	DCB	OTMS[a]	0.51 (*e*)	0.36(0.03)	4	10^3-10^4
			0.02 (*h*)	0.01(0.004)	-40	10^2-10^3
6	DCB	Bare[b]	0.1	0.06(0.005)	10	10^5-10^6
7	DCB	OTS[b]	0.06	0.045(0.004)	4	10^5-10^6
8	DCB	OTMS[b]	1.0	0.65(0.06)	-15	10^4-10^5

Charge transport properties of ODI and ODI-CN were investigated in OFETs. ODI, although showing ordered self-assembly, did not show obvious FET activity in air and nitrogen atmosphere. However, OFETs based on ODI-CN showed typically n-channel character. Devices were fabricated and measured with bottom gate, top-contact geometries in air and nitrogen atmosphere. The thin films were prepared either by spin coating from hot chloroform solution or drop-casting from hot 1,2-dichlorobenzene (DCB) solution onto the substrates with a temperature of 100 ^oC. The dielectric surfaces (SiO_2) were either modified by octyltrichlorosilane (OTS) or octadecyltrimethoxysilane (OTMS) or unmodified (bare). The devices were annealed around the liquid crystalline phase transition temperature at 230 ^oC, which showed improved FET mobility. Typical output and transfer characteristics are shown in Figure 3.6. In nitrogen atmosphere, all the devices fabricated from DCB solution show typical n-type behavior and the electron mobility derived from the saturation

regime (μ_e) reach up to 0.1, 0.06 and 1.0 $cm^2V^{-1}s^{-1}$ for devices with bare, OTS, and OTMS-treated SiO_2/Si substrate, respectively (Table 3.1). The maximum μ_e dropped to 0.054, 0.037 and 0.51 $cm^2V^{-1}s^{-1}$, respectively, when measured in air. Interestingly, the devices modified with OTMS showed ambipolar behavior in ambient air conditions upon oxygen doping,[14] with μ_h and μ_e up to 0.02 $cm^2V^{-1}s^{-1}$ (average 0.01 $cm^2V^{-1}s^{-1}$) and 0.51 $cm^2V^{-1}s^{-1}$ (average 0.36 $cm^2V^{-1}s^{-1}$), respectively (Figure 3.6 e-h). This phenomenon might be attributed to that OTMS self-assembled monolayer could change the surface energy and surface roughness, which could minimize the charge traps through different nucleation and growth behaviour of the organic semiconductors.[15]

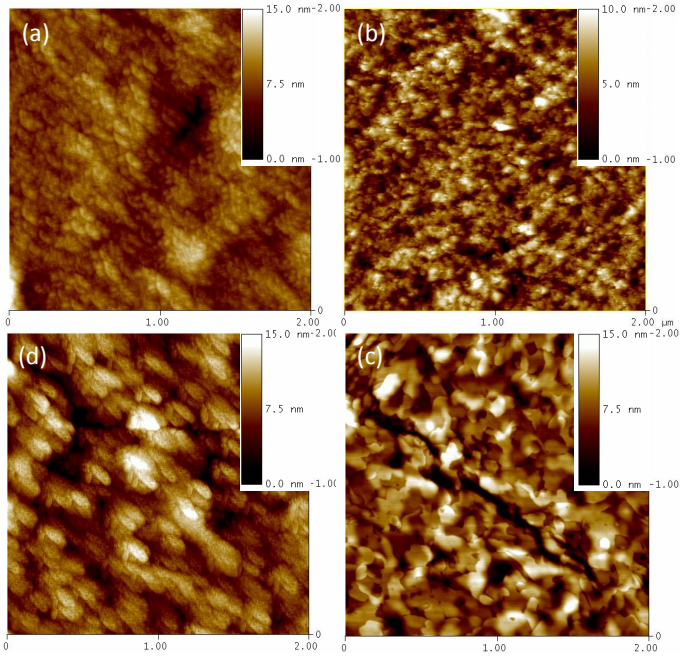


Figure 3.7 Tapping mode AFM images of the thin films of ODI-CN on bare (a, c), and OTS (b, d) modified SiO_2/Si substrate processed from chloroform solution.

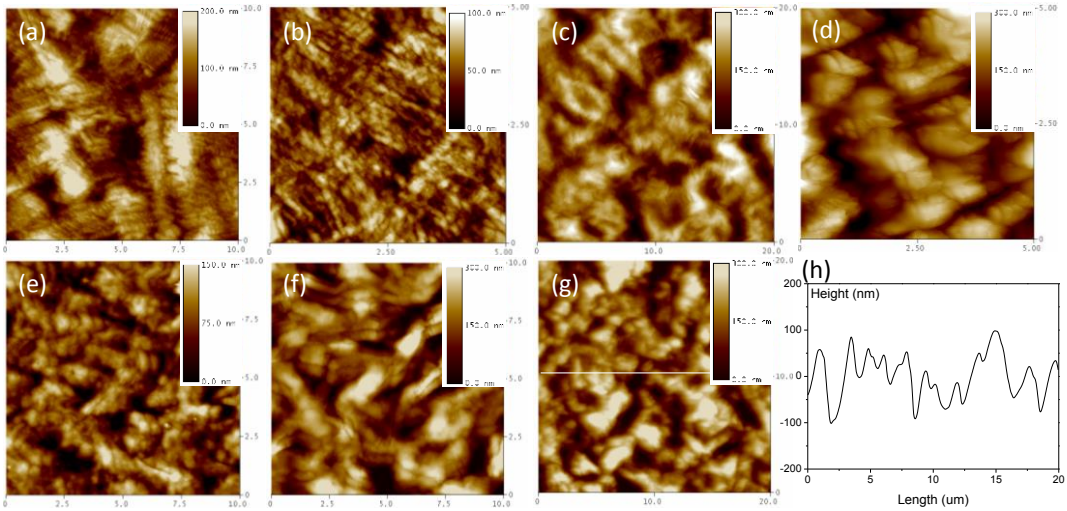


Figure 3.8 Tapping mode AFM images of the thin films of ODI-CN on different SiO_2/Si substrate without annealing (a-c) and with thermal annealing (d-g) processed from DCB solution. (a, e): on bare substrate; (b, f): on OTS treated substrate; (c, d, g) on OTMS treated substrate. (d) is the zoom-in image of figure (g), and (h) is the section profile of figure (g).

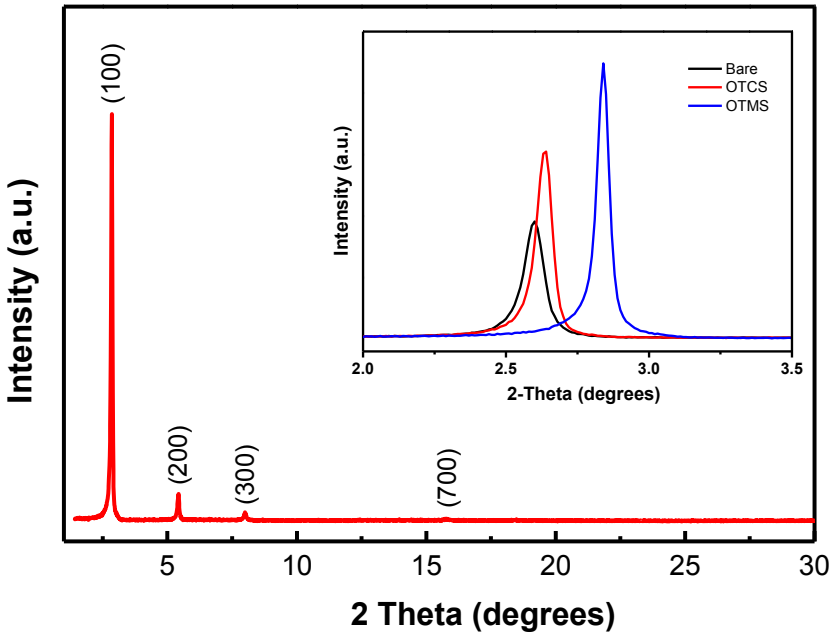


Figure 3.9 XRD pattern of ODI-CN thin film prepared by drop-casting from DCB solution onto OTMS treated substrate followed by annealing. Insert are (100) X-ray diffraction pattern on different substrates (left) and the proposed lamellar packing mode (right).

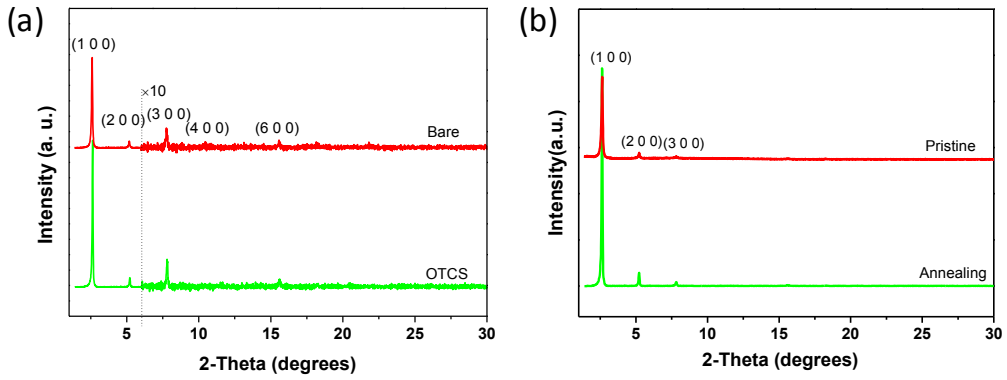


Figure 3.10 (a) XRD patterns of pristine and OTS-modified surface with a solution of DCB, then annealed at 230^{o}C, and (b) OTMS treated surface without/with thermal annealing.

AFM and thin film XRD were used to understand the morphology and molecular order of ODI-CN thin films casted from chloroform or DCB solution on different substrates, with/without annealing (Figure 3.7-3.8). In all cases, thermal annealing around liquid crystalline phase significantly increased crystalline grain size (Figure 3.8), and thin films casted from DCB solution showed larger grain size up to several micrometers (Figure 3.7). In addition, under same casting/annealing condition, the crystalline grain size increased from bare substrate to OTS to OTMS-treated substrate. The XRD patterns of the thin films after annealing exhibited intense Bragg's diffraction peaks (Figure 3.9-3.10), indicating the formation of large crystals on the surface of the substrate. A typical lamellar structure can be easily assigned based on a series of (100), (200), and (300) reflection peaks, which are correlated to a layer-like packing mode. In accordance with the AFM image studies, the as-cast thin films from DCB showed stronger reflection than that from chloroform, and the thermally annealed film exhibited higher molecular order than that before annealing (Figure

3.10). As a result, thin films casted from DCB followed by annealing displayed higher charge carrier mobility. In addition, the shortening of the inter-plane distance from bare substrate (33.9 Å) to OTMS modified substrate (30.9 Å) give a reasonable explanation that more dense packing and higher degree of crystallinity in the latter gave a 6-8 fold increase in electron mobility (Figure 3.9). Moreover, the devices also displayed good air stability due to the low-lying LUMO energy level (-3.9 eV). There was almost no change on the device performance after storing in air for two weeks for the devices with OTMS modified substrate. The kinetic stability of the highly crystalline dense packing could be another contributor to the air stability.

3.2.2 Complementary Circuits based on ODI-CN

Bottom-gate bottom-contact structure was employed to evaluate the electronic performance. This configuration is highly desirable since it could reduce fabrication steps and production costs and compatible with conventional lithographic processing. Nevertheless, especially for n-type materials, the charge injection efficiency in bottom-contact devices between electrodes and semiconductor materials is lower compared to top-contact devices due to large injection barrier at the metal/semiconductor interface arising from energy mismatch between work-function of electrodes and LUMO energy level of semiconductor materials. And another key problem is the limited charge injection area in the bottom-contact devices. The main source of contact resistance is ascribes to different film growth morphology over the interface between the SiO_2 channel region and metal electrodes. Therefore, the

interface between semiconductor and electrodes becomes more and more important when optimize the OFET devices. The most used technique to improve the device performance is to treat the electrodes surface with self-assembled monolayer (SAM), such as the thiol reagent which could change the work function of the electrode and film morphology on the electrode surface. Here we report the fabrication and characterization of bottom-gate, bottom-contact transistors by using **ODI-CN** as active component and the complementary circuits performance using p-type pentacene and n-type **ODI-CN**.

The characteristics data for the devices under different fabrication conditions are summarized in Table 3.2. All the devices were tested in air and operated as a typical n-channel field effect transistor, showing a high performance with an average electron mobility of 0.01 $cm^2V^{-1}s^{-1}$, threshold voltage of 10~20V and current on/off ratio of more than 10^5. The charge carrier mobility values are substantially increased after thermal annealing at 240 ^oC (near the crystalline phase-to-liquid crystalline transition temperature of **ODI-CN**) compared with the devices without thermal annealing or annealed at lower temperature (200 ^oC). Compared to top-contact device (run 1), the bottom-contact devices could produce comparable performance after proper treatment. The smaller variation between treated devices (OTS-modified substrates and 1-OT and PFBT-modified Au electrodes) and untreated ones (bare substrates and Au electrodes after solvent cleaning) reflect the good intrinsic materials properties of **ODI-CN**.

Table 3.2 Electrical characteristic of the **ODI-CN** OFETs based on bottom contact structure.

solvents	Au surface treatment	SiO_2 Surface treatment	T_A[°C]	μ_{sat}[cm^2/Vs]	V_{th}[V]	On/Off
DCB	none	OTS	240	0.03[a]	10-15	10^6
DCB	none	bare[b]	200	0.001	10-15	10^5-10^6
DCB	none	bare	240	0.006	10-15	10^5-10^6
DCB	none	OTS	240	0.002	15-20	10^5-10^6
DCB	1-OT	OTS	200	0.002	5-10	10^5-10^6
DCB	1-OT	OTS	240	0.007	9-14	10^5-10^6
DCB	PFBT	OTS	200	0.001	15-25	10^5-10^6
DCB	PFBT	OTS	240	0.006	15-25	10^5-10^6
DCB/$CHCl_3$[c]	none	bare	200	0.003	5-15	10^5-10^6
DCB/$CHCl_3$	none	bare	240	0.01	10-20	10^5-10^6
DCB/$CHCl_3$	1-OT	OTS	200	0.005	10-20	10^5-10^6
DCB/$CHCl_3$	1-OT	OTS	240	0.02	10-20	10^5-10^6

T_A: annealing temperature; [a] top-contact structure, and the other devices are in a bottom-contact configuration;[b] the surface was not treated with OTS; [c] the solution in DCB solution was first drop-casted onto the substrate and the film was annealed to form large-size grains, then the cracks and voids between grains were filled with the $CHCl_3$ solution through spin coating.

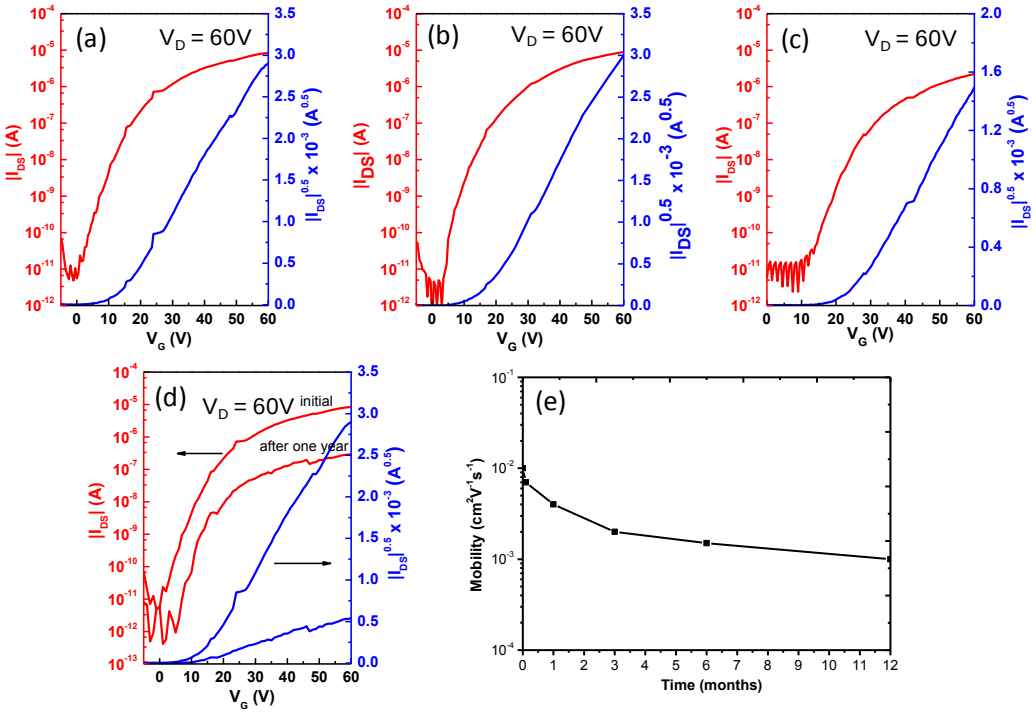


Figure 3.11 The transfer characteristics of bare Au (a); Au/1-OT (b) and Au/PFBT (c) based devices. (d) Shows the stability of the device for 1-OT treated electrode after one year. (e) The charge carrier mobility versus the storing time (months) of 1-OT treated device.

The performance of these bottom-contact devices is a little lower than that for the top-contact devices, which can be explained by the increased contact resistance of the bottom-contact structure due to different crystal nucleation and growth on the contact and dielectric surface and limited charge injection areas.[16-17] Therefore, the devices performance could be improved by reducing the contact resistance through proper surface treatment and film morphology optimization. The air-stability of the devices was also investigated with a relative humidity of 30-40% under ambient air. It turned out that the device showed relative good air stability and only a little decrease of the performance was observed after storing in air for two months, and the devices still showed electron mobility of 1×10^{-3} $cm^2V^{-1}s^{-1}$ even after storing in air for one year

(Figure 3.11 (d)-(e)). It was thought that the imide and cyano groups in **ODI-CN** help to lower down the LUMO energy level (-3.9 eV) and to promote the dense packing of the molecule, which is in accordance with the electrochemical data and X-ray diffraction results.

The superior stability and mobility of the OFETs based on **ODI-CN** make it suitable to complement well-established p-type semiconductors (e.g. pentacene) for complementary inverters. Pentacene is a well-established p-type semiconductor with reported OFET mobility in the range of 0.1-3 $cm^2V^{-1}s^{-1}$, and threshold voltages of ~0 V.[34] The intention of this work is to demonstrate the practicality of the OFETs based on **ODI-CN** by realization of CMOS circuits. The fabrication and characterization of a CMOS inverter with the p-type OFET based on pentacene (as the pull-up driver) and the n-type OFET based on **ODI-CN** (as the pull-down driver) will be delineated next.

Table 3.3 Electrical characteristics of the pentacene-based OFETs.

Td [^oC]	Au surface treatment	SiO_2 Surface treatment	$\mu_{sat}[cm^2/Vs]$	$V_{th}[V]$	On/Off
80	none	OTS[a]	0.24	-7~-10	10^5-10^6
80	none	bare[b]	0.27	-15~-17	10^2-10^3
80	1-OT	OTS	0.28	-18~-20	10^5-10^6
80	PFBT	OTS	0.21	-14~-16	10^5-10^6

[a] top contact device; [b] the surface was not treated with OTS, only cleaned with piranha solution.

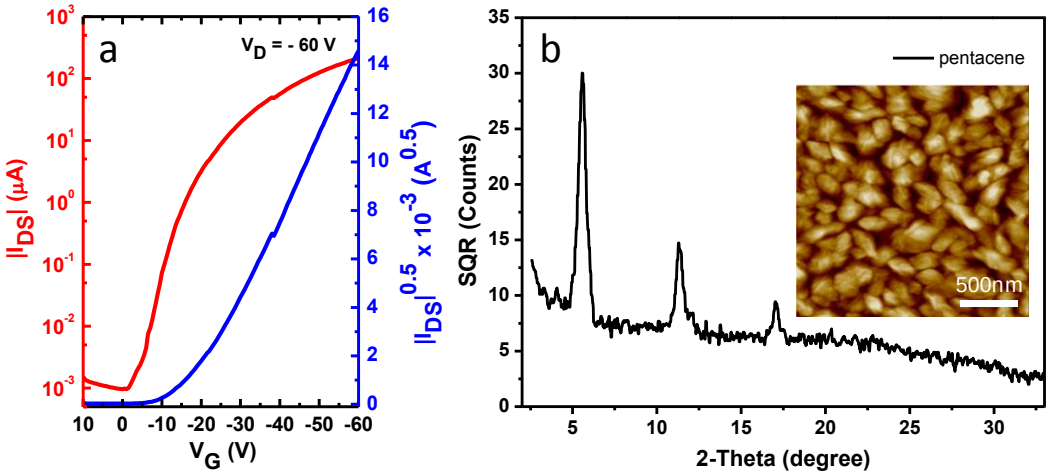


Figure 3.12 (a) Transfer characteristics of bottom-contact device at V_D = -60 V for the evaporated pentacene thin film with the same modification as the **ODI-CN** (W/L= 6000/50 μm). (b) X-Ray diffraction pattern of the thin film of the pentacene. Inset is the AFM image (2 μm ×2 μm) of the terrace-like islands.

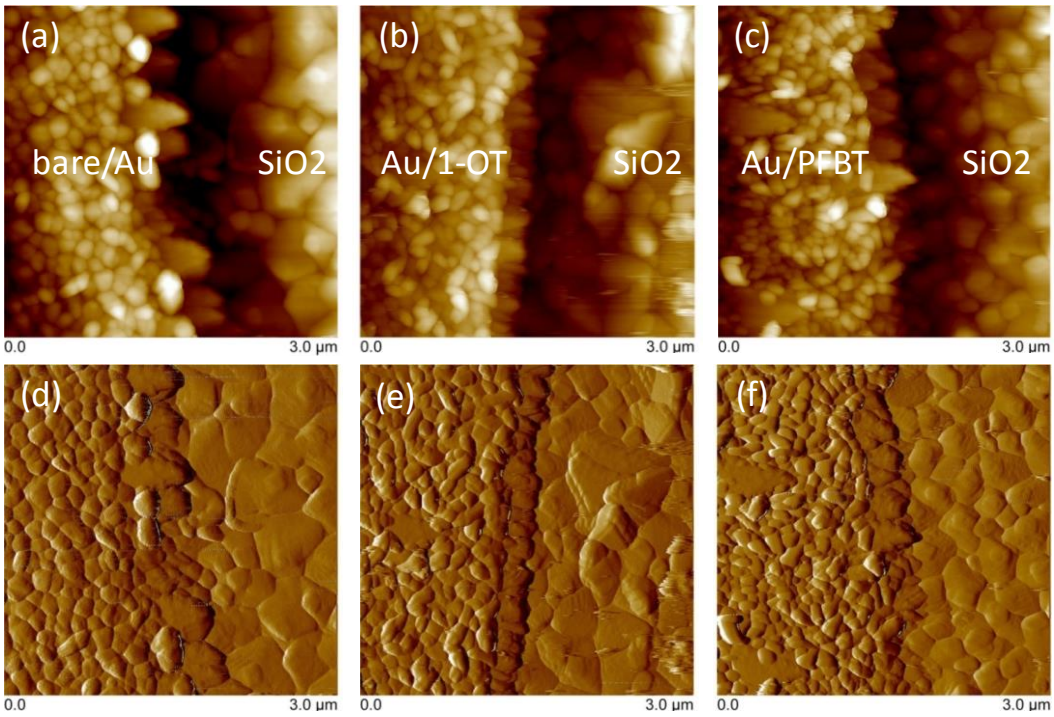


Figure 3.13 AFM images of pentacene films with different surface treatment at the interface between the gold electrode and silicon oxide surface. (a, d) bare Au without surface treatment; (b, e) 1-OT treated Au surface and (c, f) PFBT-treated Au surface.

The same device structure was chosen to investigate the device performance of the evaporated pentacene (from Aldrich). Prior to depositing pentacene film, the substrates were treated with the same method to that for **ODI-CN**. Later on, 400 Å

thick thin films of pentacene were deposited at a rate of 0.1-0.2 Å/s, with a substrate temperature (T_{sub}) of 80 ^{o}C. The devices were characterized under ambient conditions and typical transfer characteristic is shown in Figure 3.12 (a) and the device performance data are collected in Table 3.3. FET mobility of 0.3 $cm^2V^{-1}s^{-1}$, V_{th} of -15 ~ -20V, and current on/off ratio of 10^5 were extracted from the saturation region of the transfer curve. The polycrystalline structure was also demonstrated by the X-ray diffraction and AFM measurements. The XRD diffraction pattern showed intense reflection peaks which are correlated to a lamellar packing structure with an interlayer distance of 15.8 Å (Figure 3.12 (b)). The AFM image showed terrace-like islands formed on the substrates (insert in Figure 3.12 (b)).

The correlation of morphology and device performance of the cleaned bare and SAM-treated pentacene OFETs was investigated. The scan regions of the boundary between electrode and channel were chosen to inspect the morphology of the interface. As can be seen from Figure 3.13, the difference in morphology between untreated and SAM-treated Au electrodes at the boundary is significant. The crystallinity of the pentacene film is discontinuous in the vicinity of bare Au electrodes, and pentacene forms small grains with many grain boundaries on the Au surface. This indicates that a morphological transition region was arisen from the Au electrode. Nevertheless, the AFM images at the interface between SAM treated Au electrodes and dielectric exhibited continuous film morphology, and the morphological transition region near the electrodes is eliminated. Therefore, 1-OT treated Au electrodes were used as the

contact for the circuit fabrication to achieve the optimum n-channel operation.

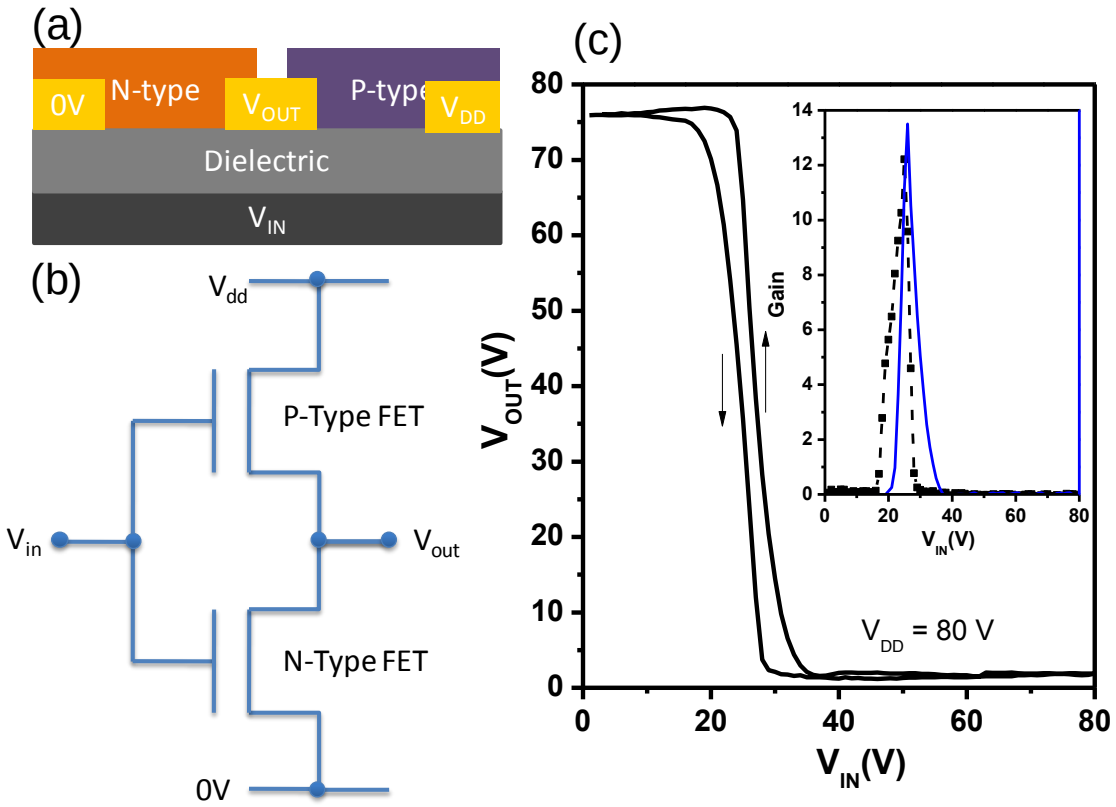


Figure 3.14 (a) The structure of a complementary metal oxide semiconductor (CMOS) inverter fabricated in this study. (b) The corresponding schematic representation of the CMOS inverter. (c) The V_{OUT}-V_{IN} transfer characteristic of the CMOS inverter; the gain of the CMOS inverter as a function of V_{IN} is shown in the inset.

The CMOS inverter with the p-type OFET based on pentacene (as the pull-up driver) and the n-type OFET based on ODI-CN (as the pull-down driver) was realized. The CMOS inverter depicted in Figure 3.14 was fabricated by on a Si/SiO_2 wafer by first patterning Au to form the V_{DD}, 0 V and V_{OUT} electrodes. The heavily doped Si serves as the common gate, while the SiO_2 forms the dielectric for the n- and p-type OFETs. The n-type OFET is first fabricated by depositing and patterning ODI-CN, followed by the p-type OFET by evaporation of pentacene using shadow mask. 400 Å thick thin films of pentacene were deposited at a rate of 0.1-0.2 Å/s, with a substrate temperature of 80 ^{o}C. The same surface treatment methods and procedures are applied

to the n-type and p-type OFET fabrication. The schematic of the CMOS inverters are depicted in Figure 3.14. The inverters are characterized at ambient conditions and at room temperature.

The V_{OUT}-V_{IN} transfer characteristic for a CMOS inverter with V_{DD} = 80 V is plotted in Figure 3.14. V_{OUT} of the CMOS inverter showed a sharp inversion at V_{IN} of ~30 V that translates to a maximum voltage gain ($-dV_{OUT}/dV_{IN}$) of 13. It is not unexpected to observe that the V_{OUT}-V_{IN} transfer characteristic is not fully symmetric, with the CMOS inverter threshold voltage slightly less than $V_{DD}/2$. The inverter threshold voltage is defined by the value of V_{IN} when $V_{OUT} = V_{DD}/2$. This observation suggests two possible arguments, or a combination of both. First, the threshold voltage of the n-type OFET is lower than the p-type OFET, i.e. $V_{T(n\text{-}type)} < |V_{T(p\text{-}type)}|$. Second, the mobility of the n-type OFET is higher than the p-type OFET. In a separate OFET performancecharacterization, the mobility of the p-type OFET based on pentacene was found to feature an average mobility of ~0.1 $cm^2V^{-1}s^{-1}$, and thus on average, one order higher than the n-type OFET based on ODI-CN. This suggests that the asymmetric V_{OUT}-V_{IN} transfer characteristic of the CMOS inverter is likely because the threshold voltage of the n-type OFET is lower than the p-type OFET. The voltage swing of the CMOS inverter is observed to be slightly lower than V_{DD}, with the voltage swing (and thus the noise margin) even lower as V_{DD} (and V_{IN}) is reduced. This suggests that the OFET's I_{on}/I_{off} decreases as V_{DD} is reduced – a well-established attribute of supply voltage scaling. Nevertheless, the voltage swing of the CMOS

inverter can be improved by increasing the I_{on}/I_{off} of both the n- and p-type OFETs. The observed hysteresis at V_{OUT} between the assertion and de-assertion sweeps of V_{IN} is due to the hysteresis behavior of the OFET devices during on/off sweeps. The CMOS inverters demonstrate high ambient stability by maintaining the above performance after exposure in air for two months.

3.3 Experimental part

Top-contact, bottom-gate FET devices were prepared under ambient conditions. A heavily p-doped silicon wafer with a 200-nm thermal SiO_2 layer was used as the substrate/gate electrode. The SiO_2/Si substrate was cleaned with acetone, then immerse in a piranha solution for 8 minutes, followed by rinsing with deionized water, and then re-immersed in a solution of OTS in toluene at 65 ℃ for 20 minutes. The semiconductor layer was deposited on top of the OTS-modified and untreated SiO_2 surface by spin-coating the solution of **ODI-CN** in chloroform (6 mg/mL) at 1500 rpm for 60 seconds or drop-casting the solution in dichlorobenzene (4 mg/mL). Subsequently, gold source/drain electrode pairs were deposited by thermal evaporation through a metal shadow mask to create a series of FETs with various channel length (L = 100 or 150 μm) and width (W = 1 or 4 mm) dimensions. The bottom-contact devices were fabricated using standard photolithography technique followed by evaporation of 95 nm gold on 5 nm titanium was used to define source and drain electrodes of 30-100 μm channel lengths and 10 mm channel widths. The

SiO_2 dielectric was modified by OTS. The Au electrode was modified by 1-octanethiol. The semiconductor layer was deposited on top of the OTS-modified SiO_2 surface by same solution process. The thin films were annealed at 250 ℃ under vacuum for 1h. The FET devices were then characterized using a Keithley SCS-4200 probe station under ambient conditions in the dark.

Bottom-gate bottom-contact structure was employed to evaluate the electronic performance. For the device fabrication, a heavily doped p-type Si wafer (purchased from Silicon Quest International, Inc.) served as the gate electrode and 200 nm of thermally grown SiO_2 was used as the dielectric layer. Firstly, the source and drain electrodes were patterned using standard photolithography methods (5 nm Ti adhesive layer and 95 nm Au layer). The devices have a channel width (W) of 2-10 mm and a channel length (L) of 30-100 μm. Prior to depositing the active layers, the substrates were cleaned with acetone, isopropyl alcohol (IPA), and piranha solution. Then the gate dielectric surfaces were treated with 0.1 M 1-octyltrichlorosilane (OTS) in anhydrous toluene for 20 min at 60 ℃ to improve the surface energy and eliminate the surface traps.[25] While the gold source/drain electrodes were treated with 1 mM 1-octanethiol (1-OT) in ethanol for 18 h to line-up the energy band at the semiconductor-metal interface,[26] pentafluorobenzenethiol (PFBT) performed in 10 mM ethanol solution for 30 min was also used to give a comparison. The optimum surface treatment process were obtained through various combination of gold, thiol (1-OT, PFBT), and organosilane (OTS). The modified surface was characterized with

water contact angle goniometer. Then 0.4 wt% solution of **ODI-CN** in 1,2-dichlorobenzene (DCB) was casted onto the substrates with a temperature of 100 ^{o}C. The devices were then annealed at 240 ^{o}C for 30 min in the N_2 atmosphere. For some devices, $CHCl_3$ solution was further spin coated on the substrate to fill the cracks and voids between grains. The field-effect mobility of the fabricated transistor was extracted using the following equation in the saturation regime from the gate sweep: $I_D = W/(2L)C_i\mu(V_G-V_T)^2$, where I_D is the drain current in the saturated regime, μ is the field-effect mobility, C_i is the capacitance per unit area of the gate dielectric layer (SiO_2, 200 nm, C_i = 17 nF cm^{-2}), V_G and V_T are gate voltage and threshold voltage, and W and L are channel width and length, respectively.

3.4 Conclusions

In this work, a large disc-like molecule ovalene was firstly used as a building block for the design of n-type semiconductors. The *C2*-symmetry ovalene diimide (ODI) and the dicyano-ovalene diimide (ODI-CN) were prepared for the first time from bisanthene building block. The ODI-CN showed typical n-type behavior in solution processed OFETs with electron mobility up to 1.0 cm^2/Vs measured in N_2 and 0.51 cm^2/Vs in air. The devices also exhibited very good stability. Thus, the ODI-CN represents one of the best solution processible n-type semiconductors reported so far. Overall, this study provided a guidance for optimizing the OFET performance by carefully controlling the surface morphology to improve the device

performance, and also showed a new route for designing new n-type and ambipolar semiconductors for optoelectronics devices.

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Chapter 4 Controlled Growth of Large Area High Performance Small Molecule Organic Single Crystalline Transistors by Slot Die Coating Using Mixed Solvent System

4.1 Introduction

The rapid development of organic material design and device processing has led to great progress for solution processed organic field effect transistors (OFETs).[1-5] Nevertheless, the large area solution-processed high-performance devices still remain challenging.[6-9] Conventional solution-processed thin film transistors fabricated by spin-coating or drop-casting methods cannot control the crystal growth behavior and crystal orientation to get high performance and large area production.[10-11] The control of crystal orientation and growth direction on channel regions has posed significant technical challenges. Therefore, many deposition techniques have been used for patterning and alignment of organic semiconductors. Among them, friction-transfer technique,[12] rubbing alignment technique,[13] photo-alignment technique,[14] magnetic alignment,[15] Langmuir-Blodgett (LB) technique,[16] zone-casting technique,[17] and solution-shearing technique[18] *etc*. are promising to produce highly aligned thin films. However, most of them are not suitable for convenient, large area production to commercialize. Based on this consideration, new deposition technique is still

desirable for realizing the industrial application like roll-to-roll printing.

Recently, solution-processed small molecule semiconductor, 6,13-bis(triisopropylsilylethynyl) pentacene (TIPS-pentacene, Figure 4.1a), has been reported to exhibit charge carrier mobility values exceeding 1 $cm^2V^{-1}s^{-1}$.[19-23] The bulky group substitution allows the molecules to have a face-to-face orientation which increases the π-orbital overlap and potentially increases the charge carrier mobility. However, most of them are based on blend systems and showed relatively large device-to-device performance variations due to poor control of phase distribution and morphology.[24-25]

In this study, we employed a simple and large-area compatible deposition technique, slot die coating, to produce highly aligned TIPS-pentacene single crystal arrays on the substrates. This coating technique has been used in many fields for lacquer and paint industry due to its reliable, accurate, and reproducible properties for the thin film production. And it has been reported in the area of organic photovoltaic cells (OPV), polymer light-emitting diodes (PLED), and electrochromic devices (EC).[26] Most importantly, this technique saves raw materials and has a good control on film thickness, uniformity as well as batch to batch variations.

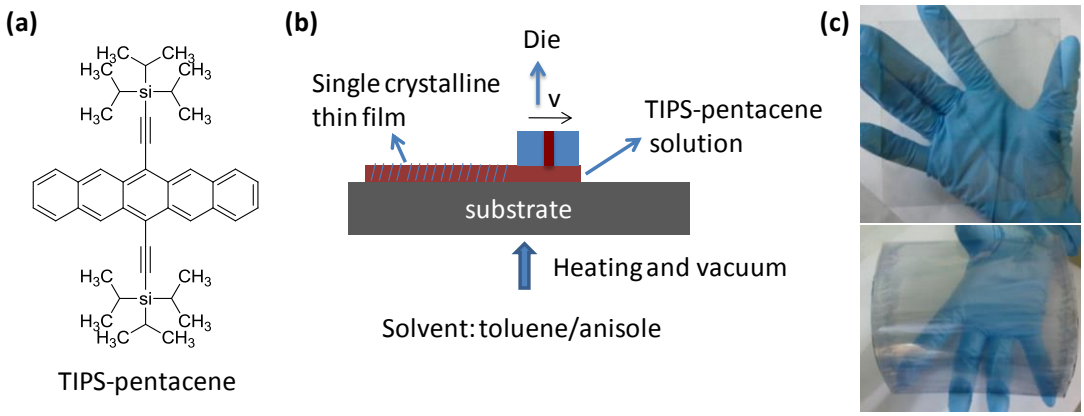

Figure 4.1 (a) Molecular structure of TIPS-pentacene, (b) schematic diagram of the slot die coating method, and (c) 10 cm × 10 cm of glass substrate (top) and PEN substrate (bottom) coated with TIPS-pentacene thin film.

4.2 Results and discussion

The slot die coating process is illustrated schematically in Figure 4.1b, the substrates were fixed by a temperature-controlled vacuum suction plate and preheated to certain temperature. A small volume of organic solution was coated on the substrate surface by a slot die with different coating gap ranging from 15 um to 90 um. The drawn down speed is controllable in the range of 0.1 – 19.9 mm/s and 20 - 100 mm/s. The pre-exposed seeding film can act as nucleation sites for remaining molecules in the solution to grow along the coating direction. The key differences and improvements of this work over the previously proposed techniques are the easy control of single crystal growth behavior and the growth direction, and versatility in large area application.

The crystallization of TIPS-pentacene is influenced by several factors such as processing method, solvent type, the rate of solvent evaporation, and surface energy of the substrate. Several studies have been conducted to control the crystallization of

the TIPS-pentacene by solution processed methods like drop-casting, inkjet printing, and dip coating techniques.[27-31] For these techniques, however, in order to facilitate the crystal growth, the substrates used need to be pre-patterned, which makes these processes complicated. Herein, our simple coating process does not require additional patterning procedure for the fabrication of large area and high performance thin film transistors. Mixed solvent systems toluene/anisole with different ratios was chosen to control solvent evaporation properties. The TIPS-pentacene has a good solubility in toluene (6.57 wt%), while a poor solubility (1.5 wt%) in anisole. Moreover, toluene has a lower boiling point than anisole, so when toluene is evaporated, the solution can easily crystallize to afford single crystalline thin films. Meanwhile, coating speed and substrate temperature can also influence the crystal formation and finally results in different device performances. At lower coating speed, discontinuous large crystal domains were formed. At higher coating speed, isotropic spherulitic crystal films with no preferential orientation was observed. Only at proper coating speed, oriented crystal domains with lengths of up to centimeters could be formed with long axis parallel to the coating direction. Higher substrate temperature is usually corresponding to faster solvent evaporation rate, which does not allow the thin film to have enough time to self-organize, and results in less oriented crystal thin films. The solvent ratio of toluene/anisole also plays a critical role in determining the crystallization behavior. When anisole volume increased, the solution has larger crystallization rate due to poor solubility and results in smaller crystal domains. This

controlled solution coating has been proved to be an effective way to prepare TIPS-pentacene thin films with highly oriented crystalline grains over a relatively large area. Figure 4.1c shows the glass and poly(ethylenenaphthalate) (PEN) substrates (10 cm × 10 cm) coated with TIPS-pentacene with a good thin film uniformity and crystal alignment using this method.

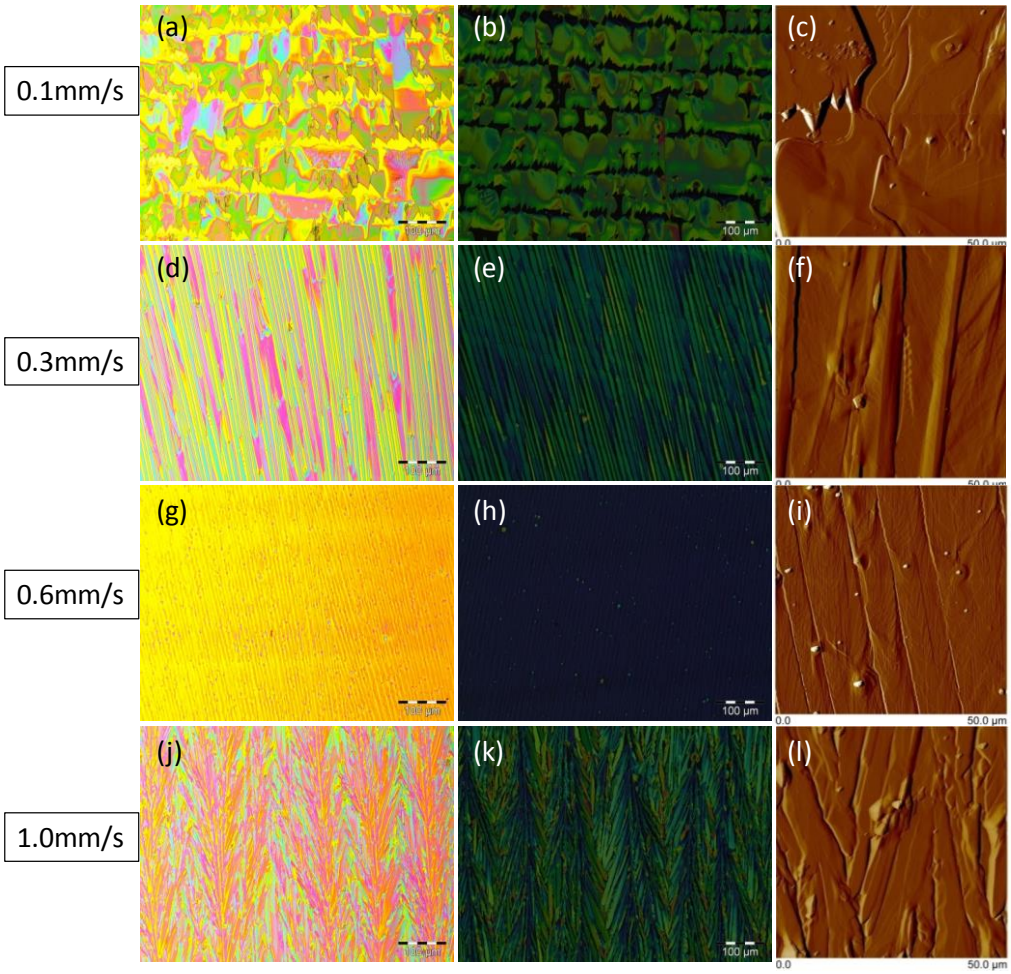

Figure 4.2 Bright field (a, d, g, j), cross-polarized (b, e, h, k) optical microscopy images and corresponding AFM images (c, f, i, l) of slot die coated thin films. The TIPS-pentacene thin films were formed at coating speed of 0.1 mm/s, 0.3 mm/s, 0.6 mm/s, and 1.0 mm/s, respectively.

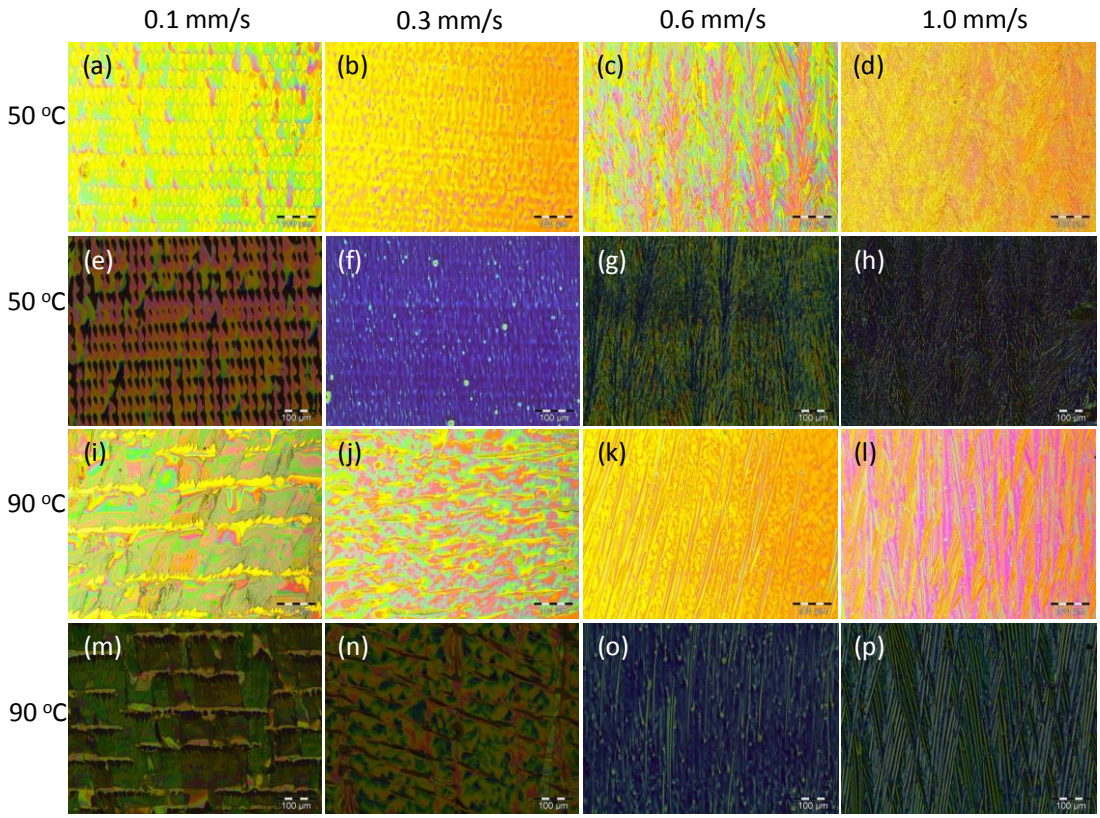

Figure 4.3 Bright field (a-d, i-l) and cross-polarized (e-h, m-p) optical microscopy images of slot die coated thin films at different coating speeds and substrate temperatures.

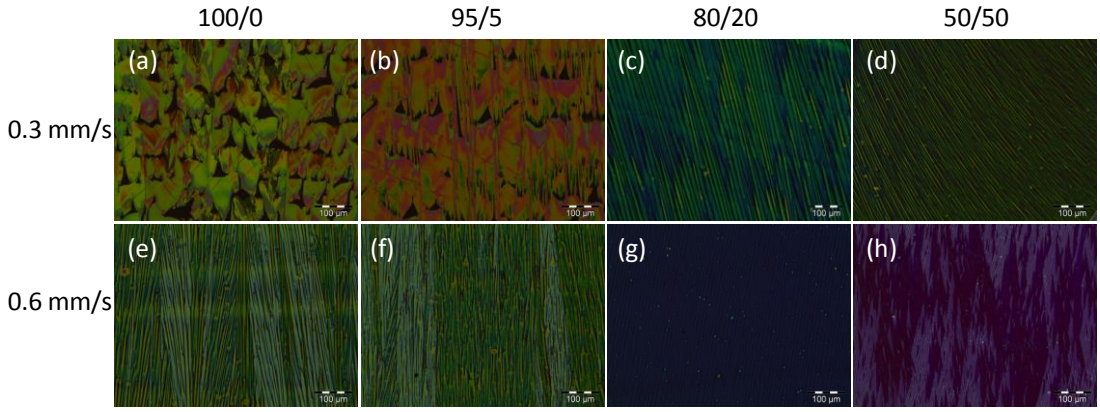

Figure 4.4 Polarized optical microscopy images of slot die coated thin films at different solvent ratios.

The thin film morphologies were evaluated using optical microscopy and tapping-mode atomic force microscopy (AFM). The thin film images are shown in Figure 4.2-4.4. It was found that for each substrate temperature, the average size of TIPS-pentacene crystal tends to decrease at higher coating speed. For the same

coating speed, the higher substrate temperature tends to form larger crystal domains. At the optimized conditions, millimeter-sized and highly oriented crystalline domains were achieved. When anisole volume increased, the crystal sizes decreased significantly due to faster crystallization rate. These large crystals cross the source and drain electrodes, which is helpful for promoting charge-carrier transport. Moreover, larger crystal domains have less grain boundaries and defects, which result in less charge traps in the channel. Different orientated ribbons could be achieved at higher coating speed. Crystals grown at 0.6 mm/s exhibited the best film uniformity, which is consistent with the polarizing optical microscopy (POM) images.

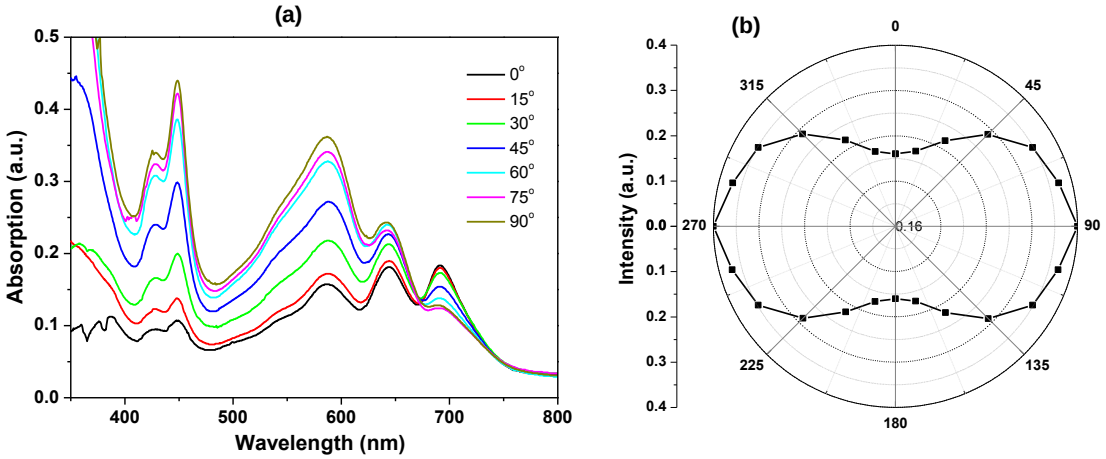

Figure 4.5 (a) Polarized UV-vis absorption spectra of slot die coated thin film with coating speed of 0.4 mm/s. (b) Absorbance dependency of linearly polarized light (588 nm) with the polarization direction rotated from 0 to 360°. The coating direction is parallel to the 0° axis.

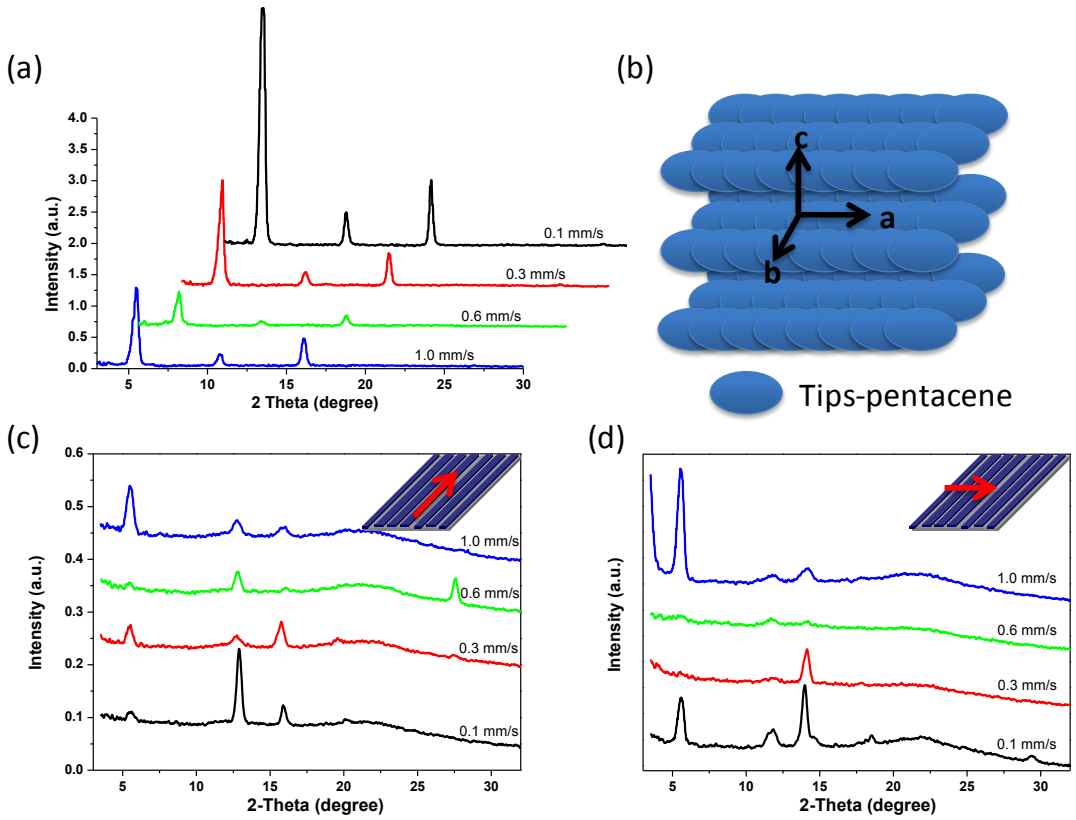

Figure 4.6 (a) Out-of-plane X-ray diffraction pattern for the coated TIPS-pentacene crystalline thin films at different coating speeds. (b) Schematic illustrations of crystal growth for TIPS-pentacene. 2D-XRD patterns with near grazing angle of the incidence beam direction parallel to the crystal array (c), and perpendicular to the crystal array (d).

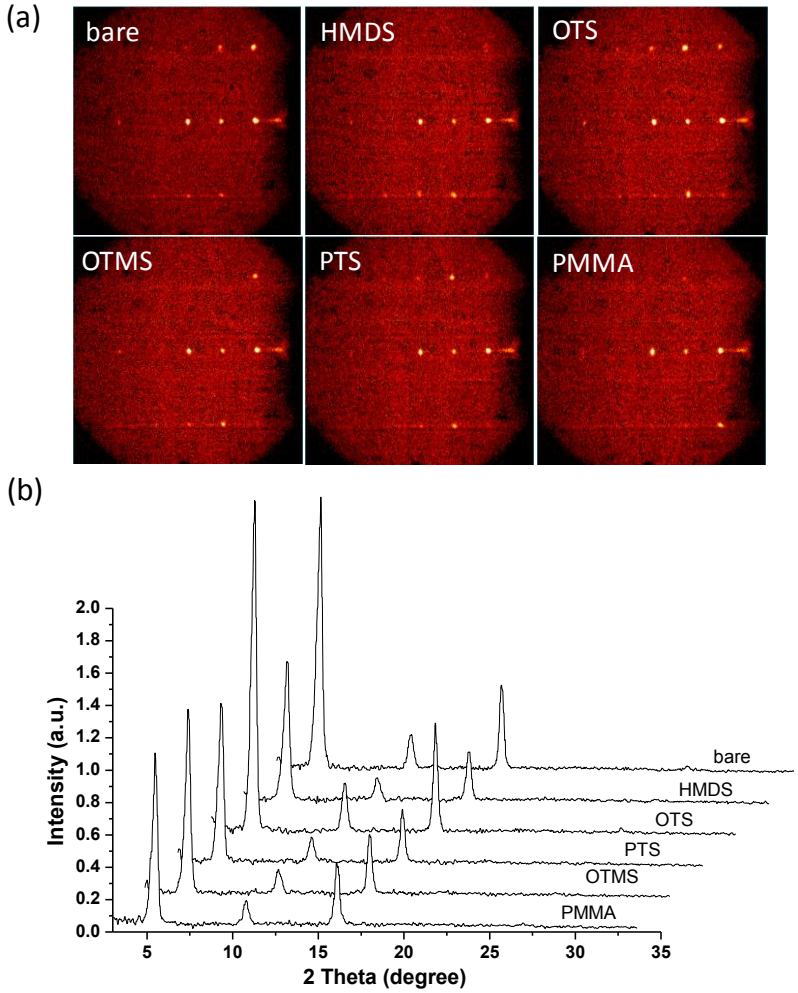

Figure 4.7 Out-of-plane X-ray diffraction images (a) and corresponding patterns (b) for the coated TIPS-pentacene crystalline thin films based on different surface treatments.

Thin film microstructures were also investigated by UV-Vis absorption spectroscopy and 2D X-ray diffraction (XRD) technique. The aligned thin-film exhibits strong absorption peaks at 425, 450, 588, 648, 700 nm which are similar to those of reported TIPS-pentacene thin films.[32] The crystal anisotropy of the aligned thin film was checked by polarized UV-vis absorption spectroscopy (Figure 4.5). When rotating the polarizer step by step, we observed that the absorption intensity changed gradually with the angle between the polarizer and crystalline thin film. The degree of the crystal anisotropy could be estimated by the intensity ratio and the value

obtained is about 2.5 (at 588 nm). While for thin film microstructure, the strong and sharp XRD diffraction peak observed at 5.42^{o} indicates a well-organized molecular structure with an interplanar *d*-spacing of 16.3 Å (Figure 4.6-4.7). This value corresponds to its *c*-axis length (16.8 Å) which is similar to the single crystal data.[33] The (00l) intensity decreased with increasing the coating speed from 0.1 mm/s to 0.6 mm/s. However, when the coating speed is 1.0 mm/s, the (00l) peak intensity increased, which is not only due to the increased crystallinity but also related to the thin film thickness. The crystal anisotropy properties were also investigated using 2D XRD with the X-ray parallel to the thin film with a grazing angle (1^{o}). When the X-ray direction is along the single crystal growth direction, XRD profiler shows an obvious π-π stacking peak at 27.7^{o} with a π-π stacking distance of 3.22 Å. Another peak at around 6.9 Å which belongs to (011) peak indicates that the crystal growth is along the *a*-axis direction. These results are consistent with other aligned single ribbons due to the strong π-π stacking along crystal growth direction.[34] When substrate rotates 90^{o}, the π-π stacking band disappears, and two peaks around 7.4 Å and 6.3 Å appear which belong to 100 and $10\bar{1}$ peaks. The *d*-spacing value is smaller than the previously reported value due to lattice strain. These results give a good explanation why the single crystal growth direction is along the π-π stacking direction, and this applied shearing force could well control this crystal growth direction through crystal lattice strain.

For the OFET device fabrication, bottom-gate top-contact device structure was

used to evaluate the electrical performance. Highly n+-doped Si wafer with a pristine silicon oxide layer (200 nm) was used as the substrate, and washed with acetone, isopropyl alcohol (IPA), respectively. TIPS-pentacene was dissolved in toluene/anisole mix solvent with a concentration of 3 wt%. The active layer was deposited under different substrate temperatures, and different coating speeds (Figure 1b). Solvent ratio, substrate temperature and coating speed proved crucial to the final crystal morphology and thin film uniformity. After depositing the crystalline films on the substrates, short vacuum annealing process was used to remove the solvent residue which could act as the traps in the thin film. Then Au electrodes were deposited on the thin films to form the source and drain. The fabrication and measurements were all performed in ambient condition.

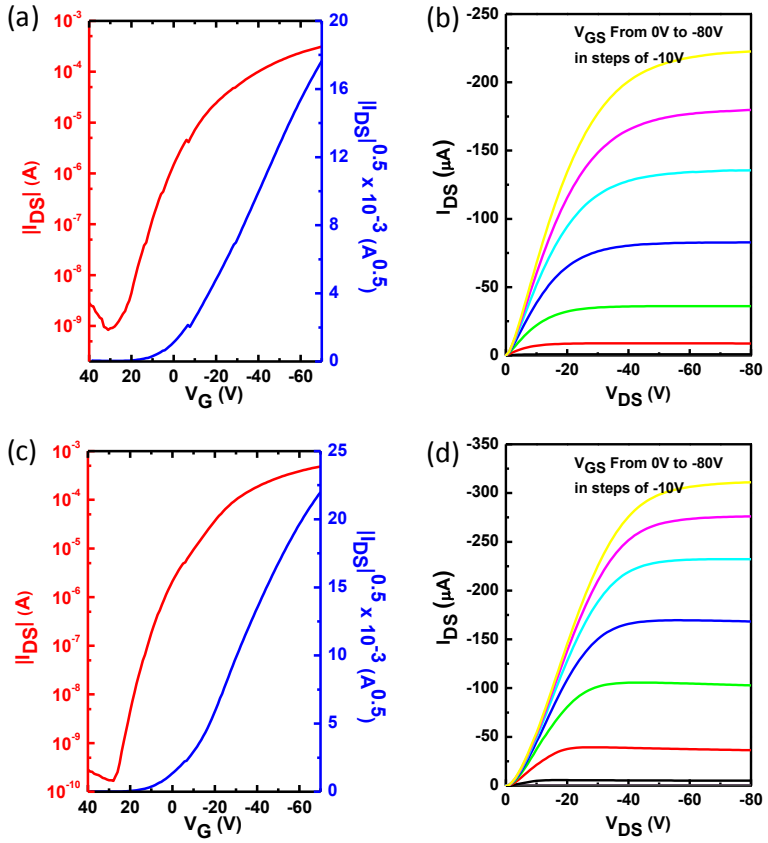

Figure 4.8 Typical transfer (V_{DS} = - 70 V) and output characteristics of the TIPS-pentacene crystal array at the optimized conditions on the bare (a, b) and OTS modified substrates (c, d). The charge carrier mobilities caculated from the curves are 0.92 $cm^2V^{-1}s^{-1}$ (a) and 1.71 $cm^2V^{-1}s^{-1}$ (c), respectively.

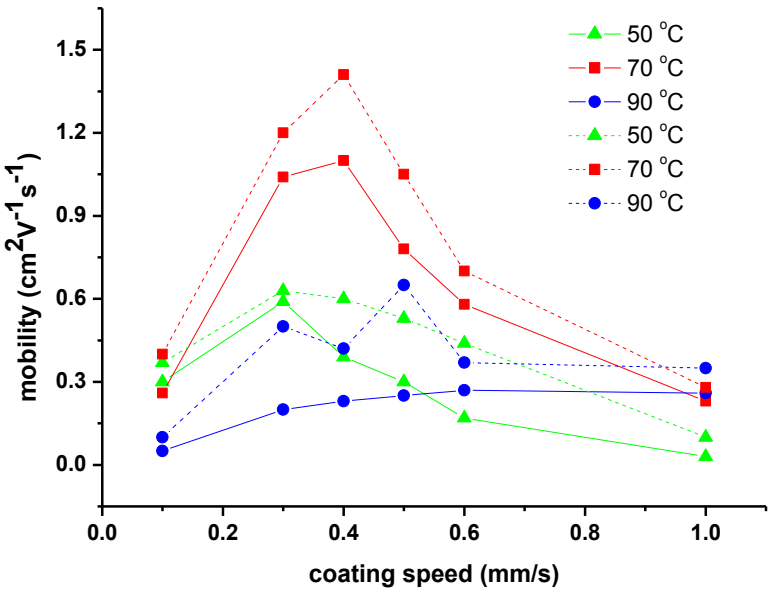

Figure 4.9 Average (solid line) and maximum (dash line) charge carrier mobility of transistors fabricated from TIPS-pentacene thin films coated at different speeds and different substrate temperatures on bare substrates.

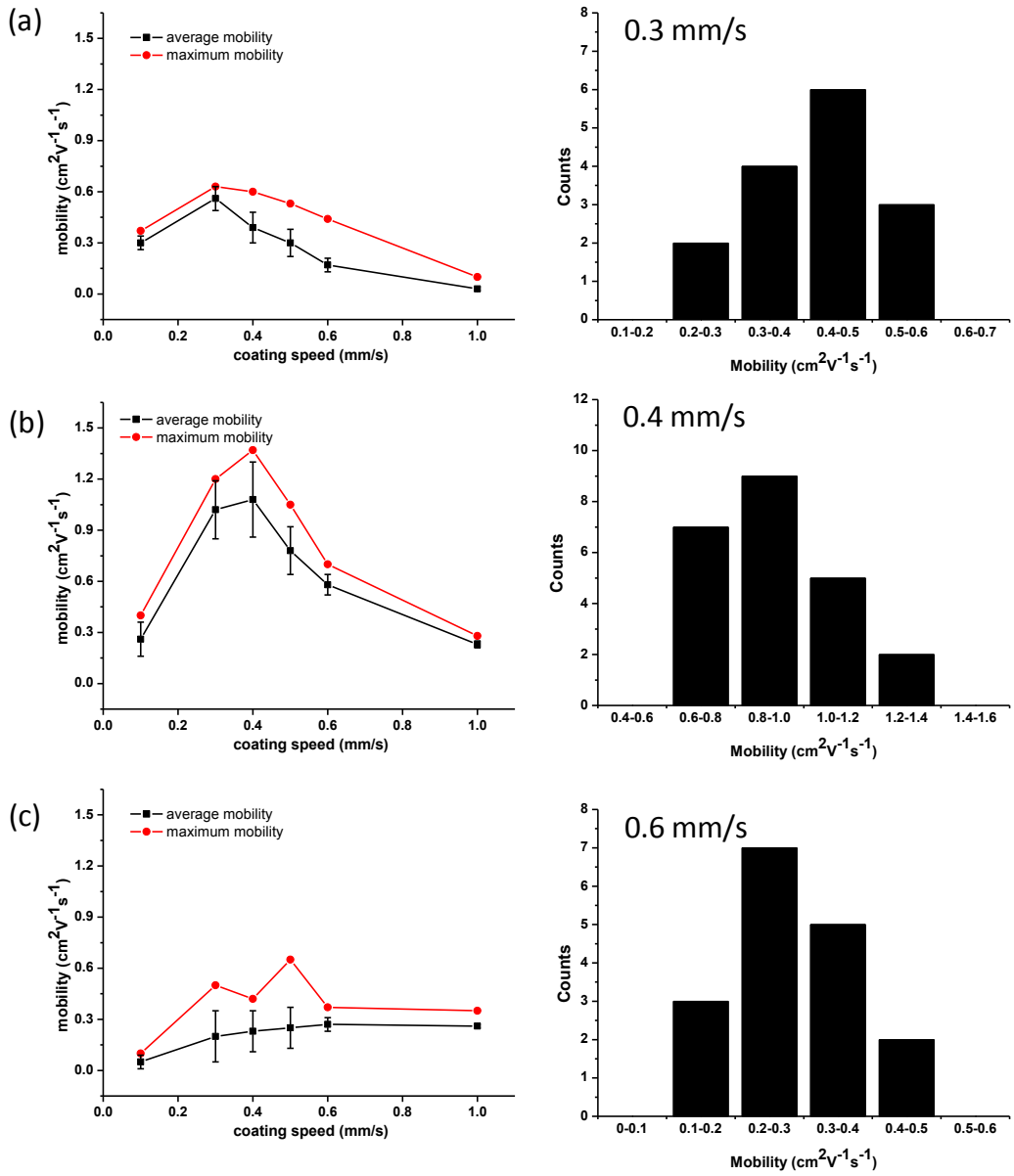

Figure 4.10 Average and maximum mobility of transistors fabricated from TIPS-pentacene thin films at different substrate temperatures ((a) 50 ^{o}C, (b) 70 ^{o}C, and (c) 90 ^{o}C) and the histograms of the best devices at each temperature on bare substrates.

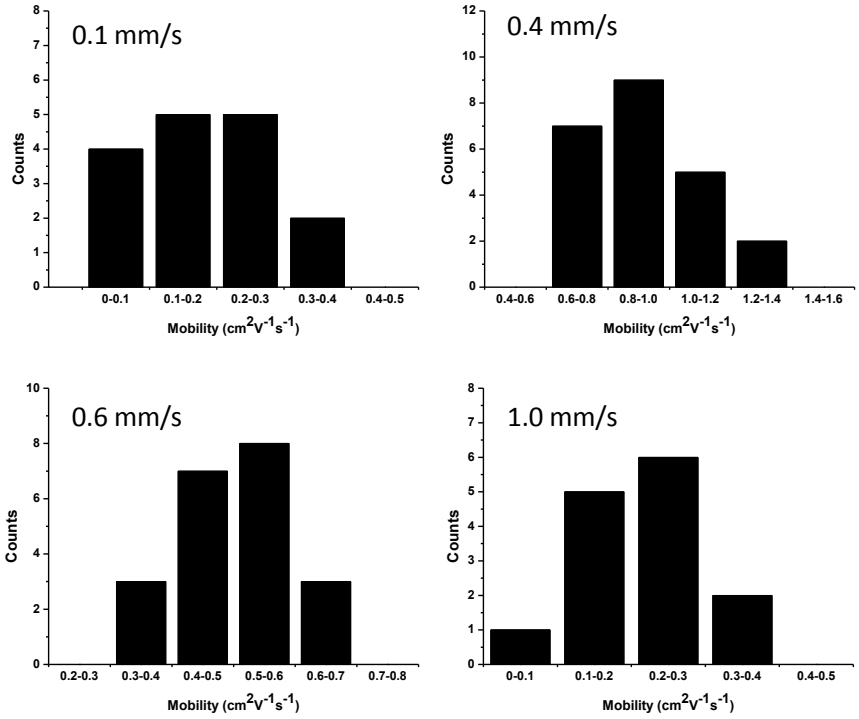

Figure 4.11 Histograms of the OFET mobility of TIPS-pentacene thin films at different coating speeds with substrate temperature of 70 ^{o}C on bare substrates.

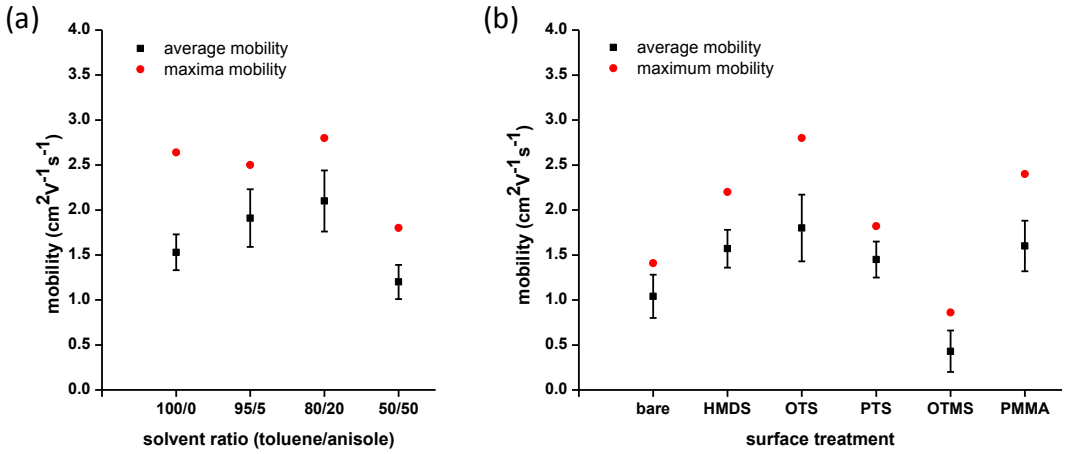

Figure 4.12 (a) Average and maximum charge carrier mobility of transistors fabricated from TIPS-pentacene thin film at different solvent ratios. (b) Average and maximum charge carrier mobility of transistors fabricated from TIPS-pentacene thin film with different surface treatments.

The transfer and output characteristics of top-contact TIPS-pentacene without surface treatment are shown in Figure 4.8 (a, b). The device was operated as p-type field effect transistor, and revealed an average hole charge carrier mobility around 1.0

$cm^2V^{-1}s^{-1}$ with high I_{on}/I_{off} of 10^6, and small threshold voltage of 10 V after optimization. This mobility is 100 times higher than spin-coated device (~0.01 $cm^2V^{-1}s^{-1}$) using same solution, and also higher than that of thermally evaporated thin film device which was limited by the higher grain boundary density. The electric performances at different coating speeds and different substrate temperatures as well as different solvent ratio were shown in Figure 4.9. As shown in Figure 4.9, for each temperature like 70 ^oC, the mobility firstly increased to 1.08 $cm^2V^{-1}s^{-1}$ at a coating speed of 0.4 mm/s. Then the mobility decreased to 0.23 $cm^2V^{-1}s^{-1}$ when the coating speed increased to 1.0 mm/s due to decreased crystallite size and alignment. With the temperature increasing from 50 ^oC to 90 ^oC, we can observed that higher temperature needs higher coating speed to give better aligned thin films and better device performances. When anisole solvent added into the TIPS-pentacene solution, it was found that the charge carrier mobility firstly increased as the ratio reached up to 20%, then the mobility decreased as the anisole content increased to 50%. It was thought to be the unfavorable crystal growth due to fast crystallization, as shown in Figure 4.4. The device performances are well correlated with the surface morphology. Generally, the larger and more highly oriented crystalline domains give better device performance. The device uniformity was shown in Figure 4.10-4.11. Compared to drop casted or ink-jet printed thin film, the thin films fabricated using this technique have better uniformity.[35] Previously, the unaligned thin films from drop casting exhibited mobility varying by several orders of magnitude, however, for our aligned

TIPS-pentacene thin films, the device mobilities values are consistently around same order with narrow distribution. The statistical investigation based on over 20 individual devices revealed an average mobility around 1.0 $cm^2V^{-1}s^{-1}$ with the highest mobility up to 1.35 $cm^2V^{-1}s^{-1}$ under the optimized condition at 70 ^oC and coating speed of 0.4 mm/s. In order to improve the device performance, surface treatments with organosilanes and polymers were performed, which is believed to reduce the surface traps like the hydroxyl groups on the dielectric surface and lower the surface energy. As shown in Figure 4.12, after surface modification, the average charge carrier mobility reaches up to 1.8 $cm^2V^{-1}s^{-1}$ for 1-octyltrichlorosilane (OTS) modified substrate and the maximum mobility can reach up to 3.0 $cm^2V^{-1}s^{-1}$. The on/off ratio reaches up to 10^7, and threshold voltage is -10 V. This performance is one of the highest values achieved by single small molecules systems. Figure 4.8 shows the output characteristics of the device. At high drain voltage, the drain current exhibited a well defined saturation behavior. For other surface treatments, the average mobilities achieved are 1.44, 1.35, 0.43, and 1.56 $cm^2V^{-1}s^{-1}$ for HMDS, PTS, OTMS-C8, and PMMA, respectively (Figure 4.12). The dielectric surface properties and organic crystallinity on the dielectric surface have important effects on the device performance.[36] The thin film anisotropy was also checked using thin film transistors (Figure 4.13). Large device variation (about 4×) can be observed due to different transport paths when the current direction parallel or perpendicular to alignment direction. The electrical anisotropy could be influenced by crystal anisotropy and

grain boundaries. Here, the latter factor dominates the electrical anisotropy in TIPS-pentacene thin films.[35, 37-38] As can be seen from the optical images, the deep defects also known as high-angle grain boundaries which need to be crossed in the charge transport.

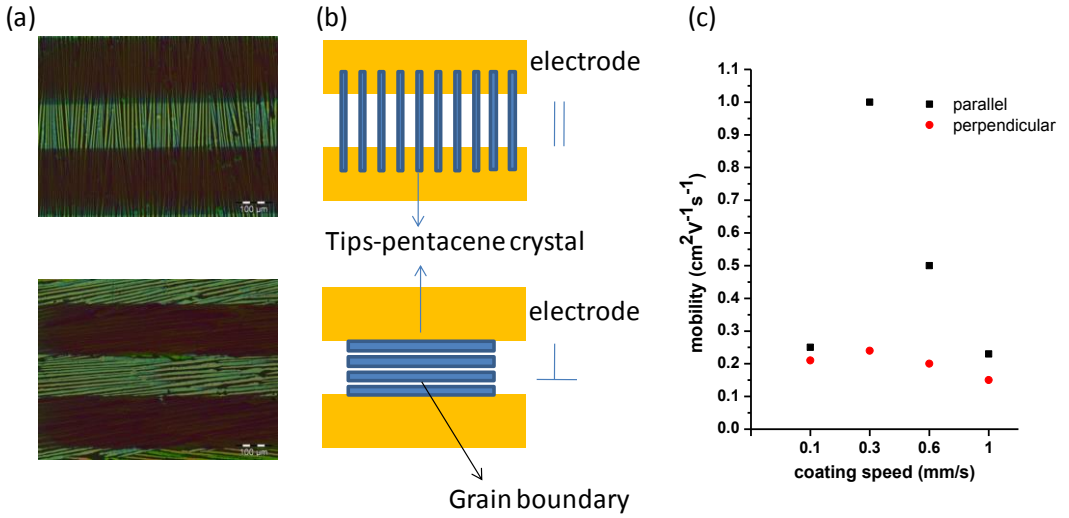

Figure 4.13 (a) Optical microscopy images of parallel and perpendicular thin film transistors fabricated from TIPS-pentacene films. (b) Proposed orientation of the single crytal arrays in the thin film devices. (c) Charge carrier mobility of aligned TIPS-pentacene devices.

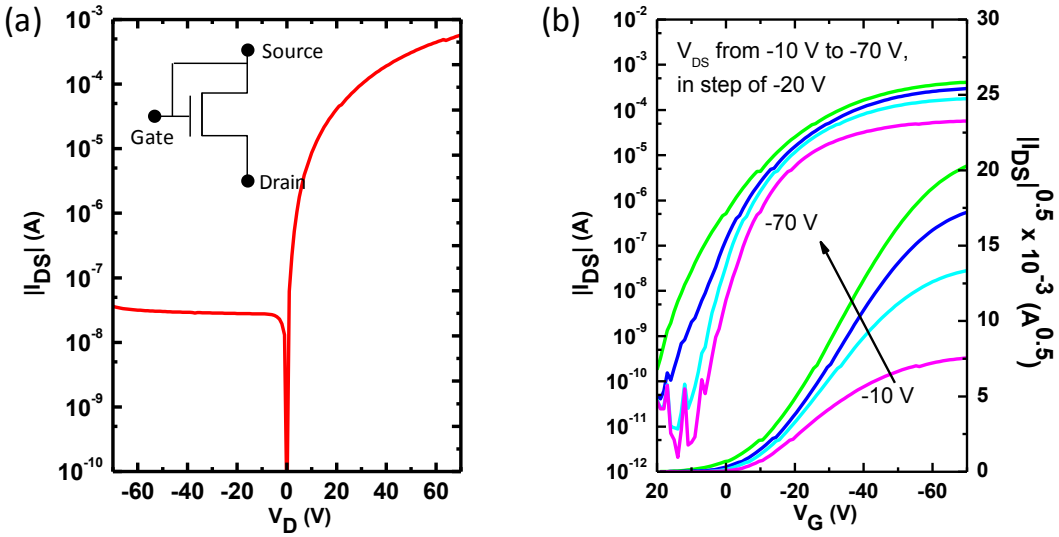

Figure 4.14 (a) I-V curve for a typical transistor diode from -70 V to 70 V. (b) transfer characteristics of the device under different V_{DS}.

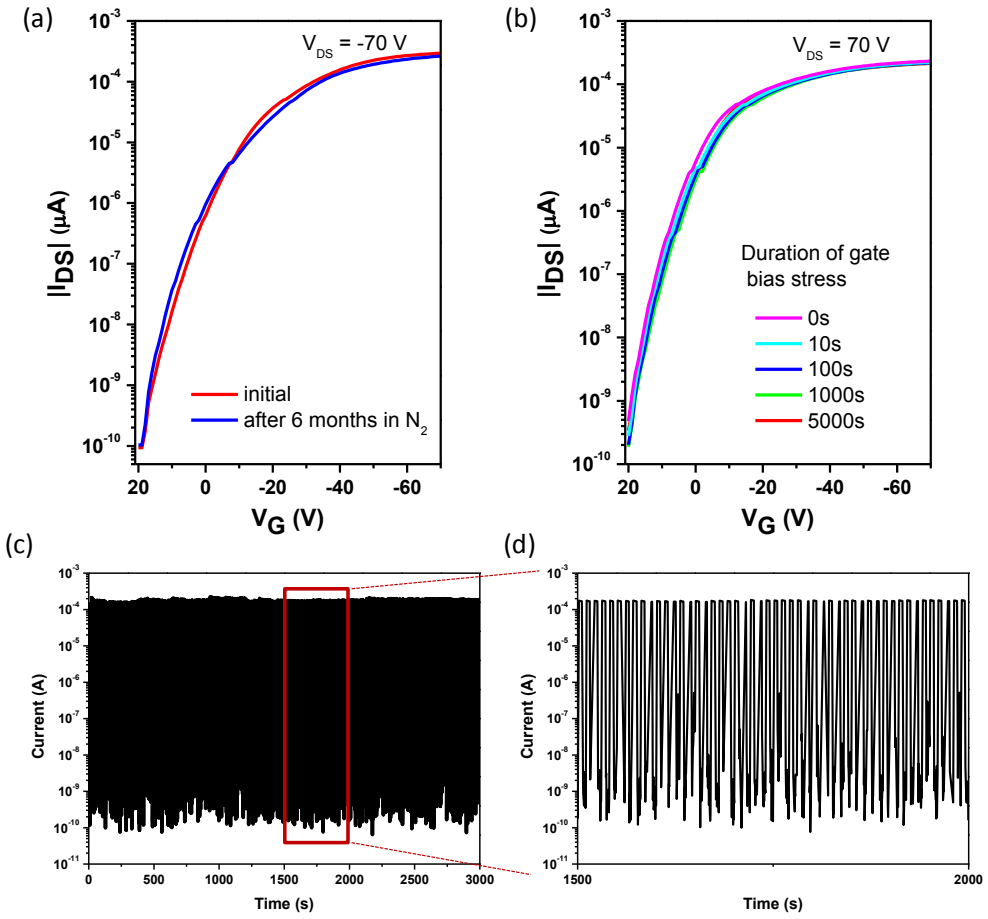

Figure 4.15 (a) Transfer curves of the prepared device and the device after 6 months in N_2. (b) Stability of transfer characteristics of a representative device under different bias stress conditions. (c, d) Cycle stability of a representative device with a continuous on (V_G = - 70 V) and off (V_G = 0 V) cycles for 3000s.

The electrical properties were further characterized using transistor diode by connecting the source and gate electrodes. As can be seen from Figure 4.14, the transistor diode showed good transfer characteristics with positive bias. Figure 4.14b shows transfer characteristics of the device under different V_{DS}. As can be seen, at lower field (V_{DS} = -10 V or -30 V), the $(I_{DS})^{1/2}$ – V_G plot was slightly bending due to surface traps at high gate voltage. The device stabilities were also checked. As shown in Figure 4.15, the transfer curves showed no appreciable changes over time when storing in N_2 atmosphere when exclude water and oxygen. The bias stress test

exhibited no significantly shift with a gate bias of -20 V for duration of up to 5000 s. In addition, the device also displayed excellent operating cycle stability when continuously on-off over a period of 3000 s.

CMOS inverters were realized combined two connected transistors with n-type **PenDI** as N-MOS and p-type TIPS-pentacene as P-MOS using solution processed methods. A common gate (Si) was used as the input voltage. Due to the difference in mobility between **PenDI** (~0.08 $cm^2V^{-1}s^{-1}$) and TIPS-pentacene (~1.0 $cm^2V^{-1}s^{-1}$), the n-channel transistor size was designed 8× larger than that of the p-channel transistor ((*W*/*L*) p : (*W*/*L*)n of 1 : 8). The transfer characteristics and signal gain of the inverter measured at different supply voltages (V_{DD}) are depicted in Figure 4.16. As expected, the inverter shows good response, V_{OUT} of the inverter exhibited a sharp inversion at V_{IN} of ~40 V at V_{DD} of 80 V, which corresponds to a maximum voltage gain ($-dV_{OUT}/dV_{IN}$) of 57.

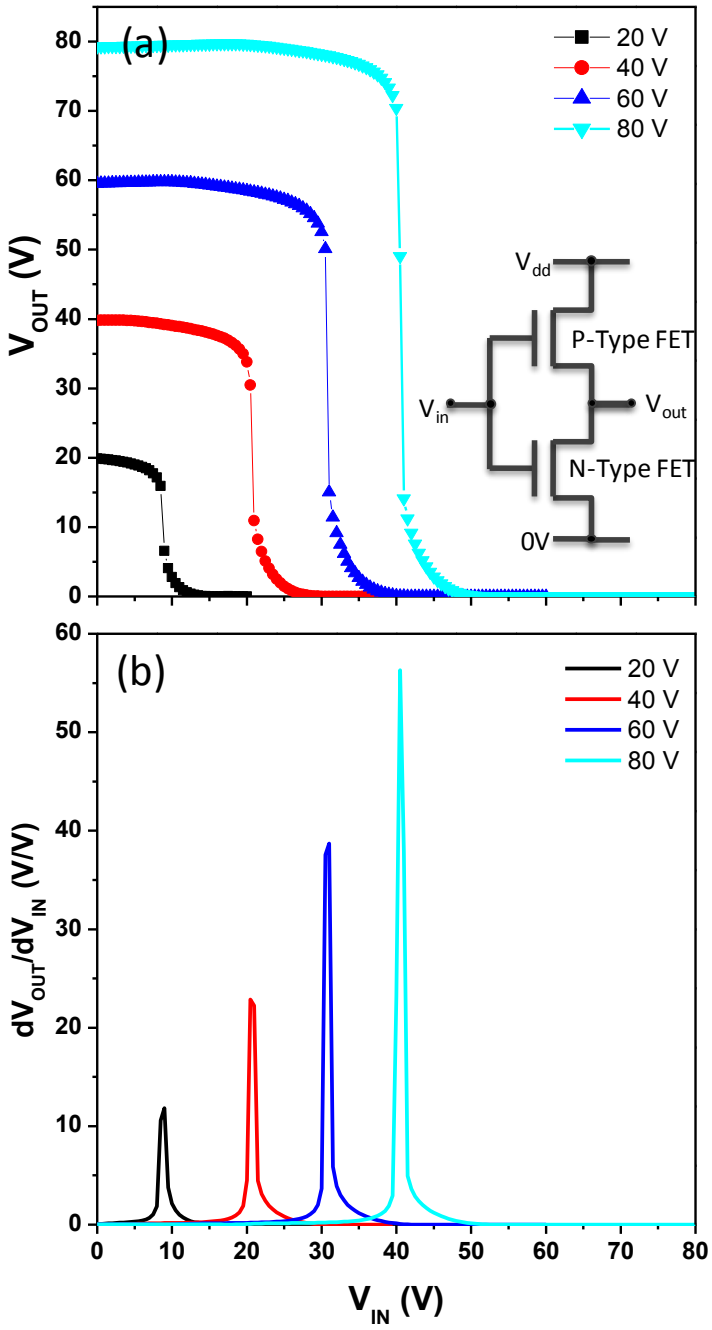

Figure 4.16 (a) Voltage transfer characteristics of a complementary inverter with various supplied voltages. (inset: schematic representation of the inverter) (b) The plots of gains ($-dV_{OUT}/dV_{IN}$) that correspond to the voltage transfer curves.

4.3 Experimental

Top-contact devices were prepared under ambient condition. A heavily n-doped silicon wafer with a 200-nm thermal SiO_2 layer was used as the substrate/gate

electrode. The SiO_2/Si substrate was cleaned with acetone, and IPA. The surface treatment can be seen in the reference. [39] The HMDS (hexamethyldisilazane), OTS (1-octyltrichlorosilane), OTMS-C8 (octyltrimethoxysilane) treatments were done by immersing the substrates in 0.1 M toluene solution at 60 ^oC for 20 min. The PTS (phenyltrichlorosilane) was treated for 1h instead. PMMA (Poly(methyl methacrylate)) (M_W 120,000) was dissolved in n-butyl-acetate at a concentration of 50 mg/mL. The solution was deposited by spin-coating at 4000 rpm for 1 min and cured at 180 °C for 1 h. The resulting device capacitance was measured with capacitance voltage measurement unit (4210-CVU) to be 8.3 nF/cm^{-2} on 200 nm SiO_2. The semiconductor layer was deposited on top of the organosilanes modified and untreated SiO_2 surface by coating the solution of TIPS-pentacene in toluene/anisole mixed solvent. The thin films were then vacuum annealed at 90 ^oC for 0.5 h. Subsequently, gold source/drain electrode pairs were deposited by thermal evaporation through a metal shadow mask to create a series of FETs with various channel length (L = 50 - 100 um) and width (W = 1 mm) dimensions. The FET devices were then characterized using a Keithley SCS-4200 probe station under ambient condition in the dark. To minimize the leakage current, small trenches in the thin film around the electrodes were created with a needle. The devices were isolated to reduce the fringing effects which can induce an overestimation of drain current and large leakage current.

Model coatmaster 510 film applicator and drying time recorder units (ERICHSEN) were used to produce the thin film. TIPS-pentacene was purchased

from Sigma-Aldrich. UV-vis absorption spectra were recorded on a Shimadzu UV-1700 spectrophotometer. POM images were recorded on a polarizing optical microscopy (OLYMPUS BX51). AFM images were recorded on a tapping mode atomic force microscopy (AFM) (Bruker ICON-PKG AFM). XRD measurements were performed on a 2D GADDS X-ray diffraction (XRD) (Bruker-AXS D8 DISCOVER GADDS).

4.4 Conclusions

In summary, we have described a new large area thin film production technique for solution processed organic field effect transistors. An average saturation regime mobility of 1.8 $cm^2V^{-1}s^{-1}$ has been achieved in the ambient condition. This method implied that large area high performance solution processed organic thin film transistors and logic circuits on the plastic substrates could be realized in the future. This technique can also combine with surface chemistries to control the single crystalline film growth region for integrating organic materials into practical devices. Moreover, the device performance can be further improved using other high performance organic materials and optimized device structures.

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Chapter 5 Convenient Slot Die Coating Induced Polymer Self-assembly and Alignment for High Performance Thin Film Transistor with Low Operating Voltage

5.1 Introduction

Solution-processable organic semiconductors are of interest for large-area, low-cost, and flexible printed electronics, e.g. flexible displays, radio frequency identification (RFID) tags, and large-area sensors.[1-9] Polymer-based organic semiconductors inherently facilitate solution processing and have the mechanical robustness necessary for flexibility and large area applications. Up to now, impressive progress has been made in enhancing organic thin film transistor (OTFT) mobility to 1.0−3.3 $cm^2V^{-1}s^{-1}$, with mobility values exceeding 8.0 $cm^2V^{-1}s^{-1}$ for unipolar *p*-channel transistor and nearing 1.0 $cm^2V^{-1}s^{-1}$ for unipolar *n*-channel transistor reported recently for polymer-based systems.[10-15]

The solution processable organic semiconductor polymers have been deposited using a variety of printing methods such as inkjet-printing, spray coating, gravure printing, and *etc*.[16-19] However, many of the printing processes result in lower and inconsistent OTFT performances, in comparison to spin-coating, due to the difficulty in controlling the morphology of deposited semiconductor films. For example,

organic semiconductor film deposited *via* inkjet printing onto non-absorbing substrates typically resulted in significant "coffee-ring" effects, leading to a non-uniform film morphology.[19] Therefore, the deposition method and process condition play important roles for OTFT performance even for a well-designed polymer.

To date, several studies have been conducted to control the crystallization of the polymer thin films through solution processing methods such as drop-casting, dip-coating, and solution shearing. The solution sheared polymer thin film was reported by Yang *et al*. to show higher performance compared to the spin-coated thin film, with the former exhibiting unprecedentedly high hole and electron mobility values of 3.97 and 2.20 $cm^2V^{-1}s^{-1}$, respectively.[20] Recently, solution-processed small molecule semiconductors, such as 6,13-bis(triisopropylsilylethynyl)pentacene (TIPS-pentacene), have been reported to exhibit high charge carrier mobility of 1.0 $cm^2V^{-1}s^{-1}$ using slot die coating technique by our group.[21] This technique saves raw materials and controls film uniformity reliably, accurately, and reproducibly. The slot die coating is scalable to large areas and is, therefore, applicable for the fabrication of large area low cost electronics. It has not yet to be applied for solution processed polymer alignment. The working mechanism is same to last chapter with the substrates were fixed by a temperature-controlled vacuum suction plate and preheated to certain temperature (100 ^oC). A small volume of polymer solution was coated on the substrate surface by a slot die with different coating speed ranging from 0.1 – 1.5

mm/s. The pre-exposed seeding film can act as nucleation sites for remaining molecules in the solution to grow along the coating direction.

5.2 Results and discussion

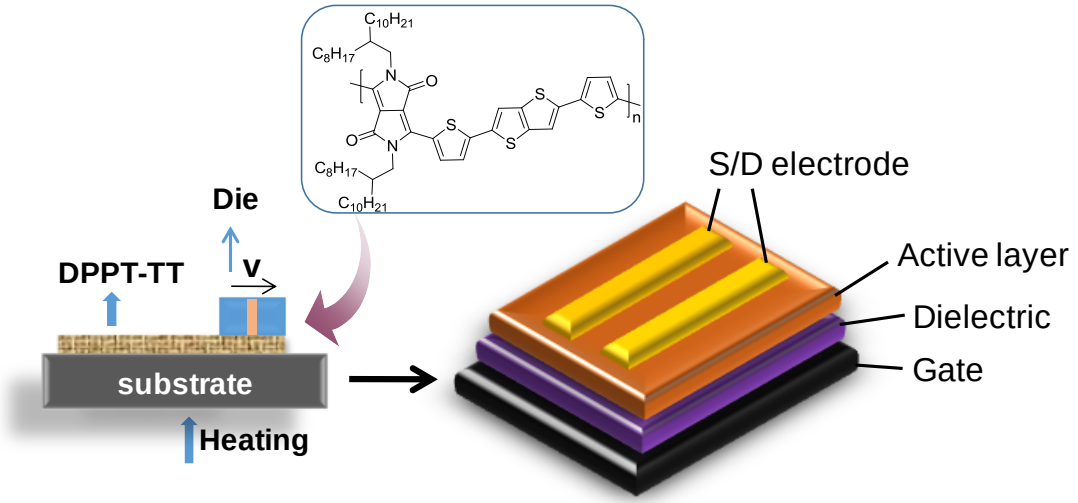

Figure 5.1 The chemical structure of the DPPT-TT, and the illustration of the thin fim processing and transistor structure.

The conjugated donor-acceptor (D-A) copolymer DPPT-TT has a relatively stronger donor moiety, dithienylthieno[3,2-*b*]thiophene (TT) and a comparatively weaker acceptor moiety, *N*-alkyl diketopyrrolo-pyrrole (DPP) (Figure 5.1). This simple polymer has been previously reported as a high mobility polymer semiconductor that exhibits hole charge carrier mobility above 1.0 $cm^2V^{-1}s^{-1}$, and demonstrates good lifetime stability in ambient conditions.[12, 22-24] All of these advantages enable it to be a good replacement for amorphous Si:H as a hole transport semiconductor for TFTs and its applications. In this work, a systematic study is performed on slot die coated DPPT-TT polymer for enhancing polymer alignment and

OTFT performance. The OTFT field mobility of 10.2 $cm^2V^{-1}s^{-1}$ achieved using slot die coated DPPT-TT polymer as the semiconductor, which is two to three times higher than that obtained using spin-coated polymer. In order to reduce the OTFT operating voltage, a native grown AlO_x on an Al gate is used as gate dielectric with slot-die coated DPPT-TT as the semiconductor. This device exhibits good transistor characteristics with the field mobility of 1.6 - 2.0 $cm^2V^{-1}s^{-1}$ at -3 V drain bias voltage. In addition, these low-voltage OTFTs exhibit linearly increasing drain current with increasing temperature in the range of 25-70 ℃ during measurement.

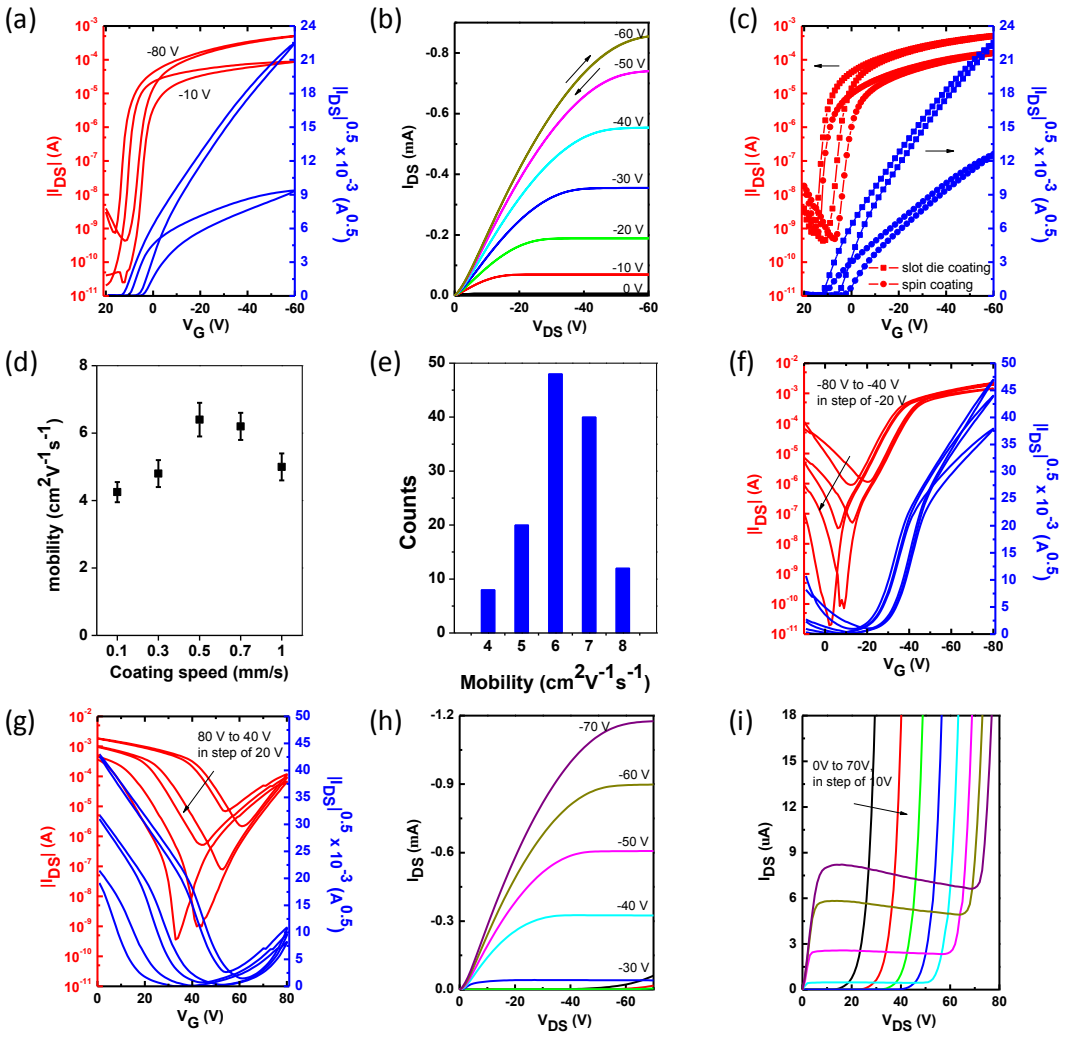

Figure 5.2 (a-b) The transfer and output curves of the slot die coated device tested in

ambient condition. (c) The comparison of slot die coating and spin coated devices. (d) The device mobilities as a function of coating speeds. (e) The mobilities distribution of the slot die coated devices. (f-i) The transfer and output curves of the slot die coated device tested in N_2 condition.

To study the electrical behavior and π-stacking characteristics of DPPT-TT with different deposition methods, a bottom gate, top-contact thin-film transistor configuration with DPPT-TT as the semiconductor layer was used. Both slot die coating and spin-coating were used to prepare the polymer thin films on 1-octadecyltrichlorosilane (ODTS)-modified SiO_2/Si substrates. The DPPT-TT polymer was dissolved in 1,2-dichlorobenzene at the concentration of 0.4 wt%. The semiconductor deposition was carried out in ambient condition for both spin coating and slot die coating. During the slot die coating process, the polymer semiconductor solution was coated onto ODTS-modified substrates heated at 100 ^oC, as illustrated in Figure 1b. The coating speed was varied from 0.1 mm/s to 1.0 mm/s. The thickness was controlled by the gap between the die and substrate and similar film thicknesses were obtained despite the different coating speeds. The DPPT-TT thin films were annealed at 160 ℃ for 15 min in vacuum after slot die coating or spin coating before source/drain electrode deposition. Figure 5.2 shows the typical transfer and I-V characteristics of fabricated OTFTs. The devices showed mainly *p*-type behavior when measured in ambient condition (Figure 5.2(a-b)), and ambipolar behavior in inert N_2 environment (Figure 5.2(f-i)). This charge transport behavior was induced by the interaction between the radical anions and the molecular oxygen and water in the atmosphere due to its lower electron affinity of DPPT-TT.[25-26] In ambient condition,

the OTFTs with slot die coated polymer thin films exhibited excellent hole mobility values ranging from 4.6-7.2 $cm^2V^{-1}s^{-1}$, compared with hole mobility values of 1.8-2.4 $cm^2V^{-1}s^{-1}$ obtained with spin coated films. The significant enhancement in performance can be attributed to the increased crystallinity and alignment in DPPT-TT film as a direct result of the slot die coating process. Investigation of the hole mobility as a function of coating speed showed that maximum OTFT mobility is obtained at a coating speed of 0.5 mm/s (Figure 5.2d). When measured in N_2 condition, the OTFTs exhibited ambipolar behavior with exceptional hole mobility values up to 8.9-10.2$cm^2V^{-1}s^{-1}$ and electron mobility values of 1.0-1.2 $cm^2V^{-1}s^{-1}$. In comparison, the spin coated OTFTs showed poorer performance with hole mobility values of 4.3-4.8 $cm^2V^{-1}s^{-1}$and electron mobility values of 0.6-0.8 $cm^2V^{-1}s^{-1}$. The hole mobility was approximately an order of magnitude higher than the electron mobility regardless of the deposition method for the DPPT-TT due to the smaller charge injection barrier for holes with respect to the gold contacts. In order to investigate the process repeatability, multiple batches of OTFT were fabricated using the optimized slot die coating speed of 0.5 mm/s. The statistical distribution of the measured hole charge carrier mobility values in air condition for 128 OTFTs is presented in Figure 5.2e. The transfer curves of the OTFTs exhibited a small degree of hysteresis that can be ascribed to surface traps and/or conformation changes of the polymer chains under an electrical bias.[27-30] Without thermal annealing, the OTFT exhibited poorer performance, with hole mobility values of 2.1-2.5 $cm^2V^{-1}s^{-1}$ and a

larger degree of hysteresis due to a higher number of surface traps.

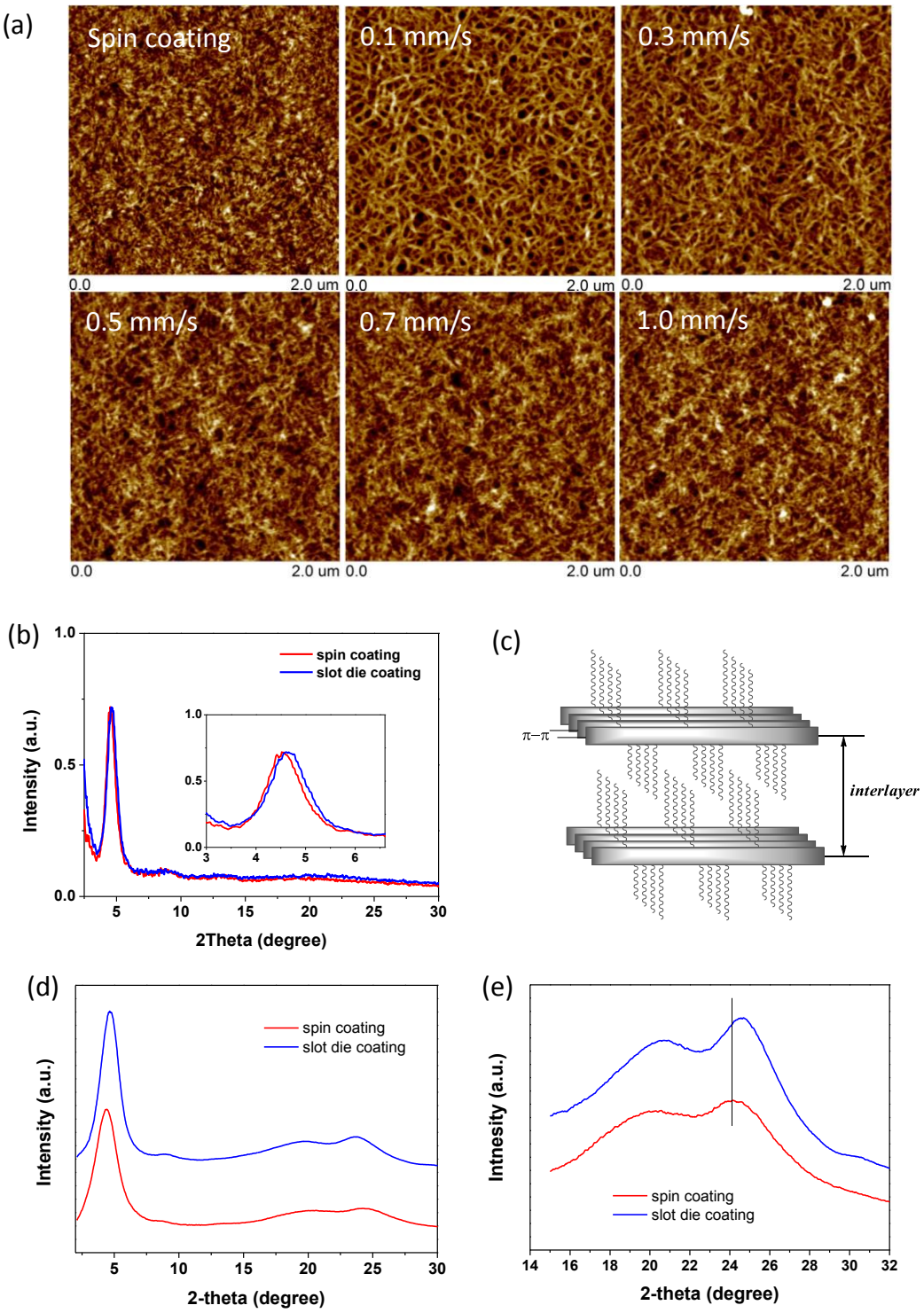

Figure 5.3 (a) AFM images of the spin coated and slot die coated devices with different coating speeds. (b) XRD intensity graphs of spin coated and slot die coated thin films on ODTS-modified Si/SiO_2 substrates. (c) Illustrative lamellar structures of the polymer thin film. (d) 2-D XRD pattern intensity graph obtained with the incident X-ray parallel to the thin film stack. (e) The in-plane diffraction peak for spin coating

and slot die coating based thin films.

To understand the effects of slot die coating on the surface morphology and microstructure of the thin film, tapping mode AFM and 2D X-ray diffraction (XRD) were conducted. The AFM images of the spin coated thin film showed a three-dimensional polymer network with well-defined grains (Figure 5.3a). In comparison, the slot die coated thin films showed nanofibrous networks with higher degrees of crystallinity (Figure 5.3a). At low coating speeds, the thin film exhibited loose nanofibres; while at higher coating speeds (0.5-0.7 mm/s), the nanofibrous networks were denser with reduced surface roughness. This morphology implies the good connectivity between grains due to strong intermolecular interactions brought about by the shearing force during the slot die coating process. The intimate interconnections among the crystalline grains are responsible for the excellent charge transport performance of the OTFTs. Increasing the coating speed further to 1.0 mm/s resulted in the formation of smaller grains and, thus, increased grain boundaries that constitute additional barriers to charge transport. The optimized slot die coating speed obtained in this study is 0.5-0.7 mm/s. XRD analysis of spin coated and slot die coated thin films on ODTS-modified Si/SiO_2 substrates was conducted (Figure 5.3b). The results confirmed that both thin films were crystalline in nature with a single distinct diffraction peak around $2\theta = 4.6^{o}$, corresponding to a *d* spacing of 19.2 Å. This value is similar as that reported in the literature for the copolymer PDQT.[13] However, the slight shift in the 2θ peak to the higher degree for the slot die coated

thin film suggests a smaller *d*-spacing compared to the spin coated film. Therefore, it is reasonable to believe that the shearing force during the slot die coating results in a larger extent of interdigitation of the polymer alkyl chains or a tilted molecular plane. To further substantiate the molecular orientation in the polymer thin films, 2D transmission XRD measurements were carried out on the spin coated and slot die coated thin films removed from the ODTS-modified substrates. The incident X-ray was oriented parallel to the film. As shown in Figure 5.3(d-e), the XRD image and diffractogram obtained with the incident X-ray parallel to the film exhibited diffraction patterns similar to those obtained from the thin film cast on the Si/SiO_2 substrate near the out-of-plane axis. Moreover, the thin films exhibited two in-plane diffraction peaks around 20.6^o and 24.2^o, which are attributed to the ordered side-chain packing and π-π stacking, respectively. The caculated spacing values are 4.30 Å and 3.68 Å, respectively. The π-π stacking distance slightly decreased from 3.68 Å to 3.62 Å for the slot die coated thin film (Figure 5.3e). The decreased π-π stacking distance is beneficial for the charge transport due to higher intermolecular obital overlap. The XRD results above unambiguously revealed the formation of a highly ordered layer-by-layer lamellar packing motif with an edge-on orientation for the slot die coated polymer thin films (Figure 5.3c). This type of molecular organization is particularly favorable for charge carrier hopping through π-π stacks in an OTFT device. Therefore, the enhancements in molecular ordering by improving co-planarity and increasing intermolecular interactions through slot die coating and

post-annealing have yielded higher OTFT hole mobility.

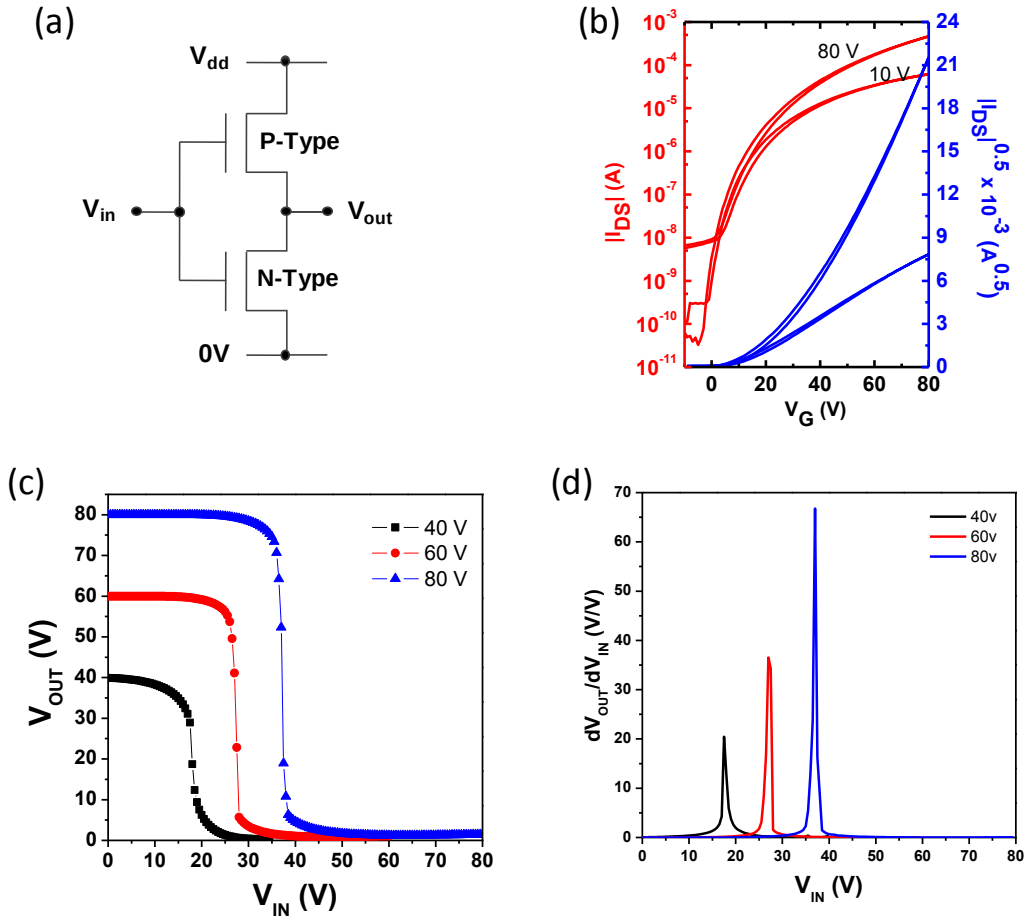

Figure 5.4 (a) The schematic electrical connections of inverter. (b) The n-channel operation of ZnO-based device. (c-d) Voltage transfer characteristics of a complementary inverter with various supplied voltages and corresponding voltage gains ($-dV_{OUT}/dV_{IN}$).

Although both holes and/or electrons transporting organic semiconductors materials have been developed in recent years, most of the organic semiconductors reported to date are *p*-type semiconductors. Due to the instability of the radical anion towards water and oxygen species in ambient conditions,[26] only a few solution processed *n*-type semiconductors that exhibit competitively high performance and environmental stability have been reported.[17] The lack of *p*- and *n*-type semiconductors with comparable performance and stability is a major hindrance to the

development of low cost, all polymer based complementary logic circuits. Compared to *n*-type organic semiconductors, the development of *n*-type metal oxides such as ZnO is advancing rapidly, with the metal oxide semiconductors outperforming their organic counterparts in terms of device performance and air stability due to their intrinsic doping. However, this also means that metal oxide semiconductors suffer from the main drawback of the lack of hole transporting compounds with appreciable charge carrier mobility. The problem lies in the deep valence band edge, which is typically around -7 eV, and the localized nature of the hole transport states which comprises of oxygen 2p orbitals.[31] Therefore, the hybrid materials system consisting of the *p*-type organic materials and *n*-type metal oxide would be a natural choice for CMOS circuit development. In this study, the CMOS inverter with the *p*-type TFTs based on DPPT-TT (as the pull-up driver) and the *n*-type TFTs based on ZnO (as the pull-down driver) was realized.[23] A common gate (Si) was used as the voltage input. The inverters were characterized in ambient condition. In a separate OTFT performance characterization, the average mobility value of the ZnO TFT was around 2.0 $cm^2V^{-1}s^{-1}$ (Figure 5.4b). The V_{OUT}-V_{IN} transfer characteristics for a CMOS inverter measured at different supply voltages (V_{DD}) is plotted in Figure 5.4d. As expected, the inverter showed excellent response. V_{OUT} of the inverter exhibited a sharp inversion at V_{IN} of ~37 V at V_{DD} of 80 V, which corresponds to a maximum voltage gain ($-dV_{OUT}/dV_{IN}$) of 66 (Figure 5.4e).

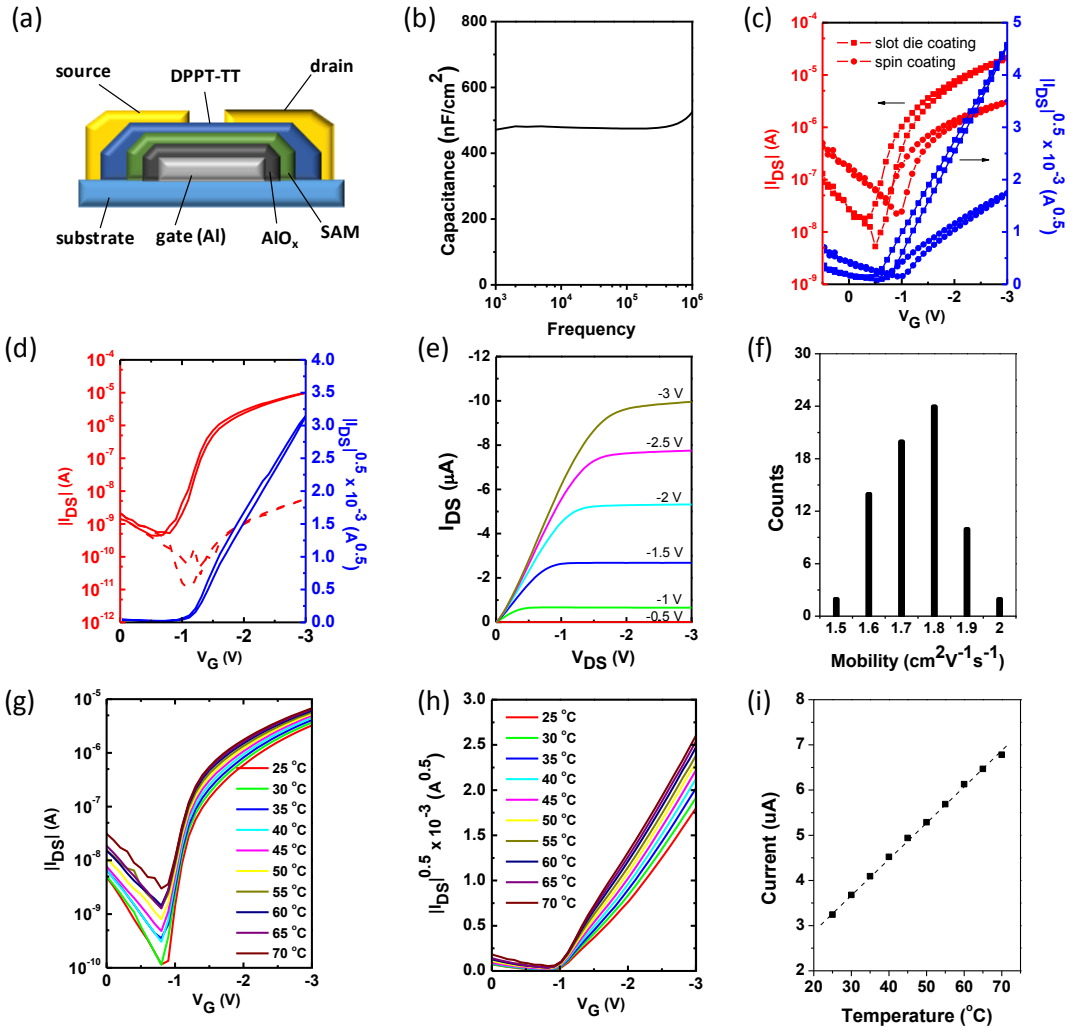

Figure 5.5 (a) The schematic representation of the low-voltage transistor. (b) AlO_x-ODPA dielectric capacitance as a function of frequency. (c) Transfer characteristics of slot die coated and spin coated devices. (d-e) The transfer and output curves of the slot die coated device with AlO_x-ODPA dielectric. (f) Mobilities distribution of the slot die coated device. The transfer characteristics (g) and sqrt root of the source-drain current (h) of thermal sensors based on the low voltage device in the range of 25 -70 ^oC. c) The source–drain current at various temperatures (in the range 25 -70 ^oC).

The achievement of high-performance integrated circuits not only requires OTFTs with high carrier mobility but also with low operating voltages. However, most of the solution processed OTFTs based on the organic semiconductor polymers usually require high voltage operation, which leads to high power consumption and incompatibility with other electronics components for application development.

Recently, an organic circuit with very low power consumption that used a self-assembled monolayer gate dielectric has been demonstrated, paving the way for low-voltage devices in future organic electronics fabrication.[34-35] In an effort to reduce the operating voltage of the slot die coated OTFTs, the ultrathin AlO_x gate dielectric was formed using oxygen plasma treated Al gate. N-octadecylphosphonic acid (ODPA) was employed to modify the AlO_x surface in order to reduce the gate leakage current and improve the device performance by reducing the number of trap sites. The device structure is shown in Figure 5.5a. The capacitance measurements carried out on the same devices yield a geometric capacitance in the range 400–600 nF/cm^2 (obtained between 1kHz and 1MHz), as shown in Figure 5.5b. These results are consistent with previously reported values by Klauk*et al.*[32-33] To prepare low-voltage organic transistors employing SAM dielectrics, we deposited the polymer thin film with spin coating and slot die coating onto the ODPA-treated AlO_x dielectric. Figure 5.5(c-e) shows the transfer and I-V characteristics of the low voltage OTFT. The transistors exhibit excellent operating characteristics with minimal hysteresis and low leakage current. The as-prepared transistors exhibited*p*-channel characteristics with a charge carrier mobility of 1.6-2.0 $cm^2V^{-1}s^{-1}$at less than -3 V drain bias. From the transfer characteristics of the device, on/off ratio of 10^5 and threshold voltage of -0.5 V were obtained. The mobility statisticaldistribution under the optimized conditions was measured for 64 devices as shown in Figure 5.5f.

Recent studies have demonstrated the use of OTFTs and their integrated circuits

in pressure and thermal sensors.[9,34]Among them, D−A conjugated polymers have attracted considerable attention due to the uniformity and conformability of their thin films. The thermal sensitivity of the low operating voltage DPPT-TT OTFTs was studied and the results were shown in Figure 5.5 (g-h). A good temperature response of the OTFTs was observed between 25 ^{o}C to 70 ^{o}C which is the temperature range of human skin and is of interest to biologists. The source-drain current vs temperature is shown in Figure 5.5 (i): the current increases linearly as the temperature increases; and the current change (ΔI_{DS}) is1 μA for an increase of temperature by 10 ^{o}C. The response of organic semiconductors to temperature change has been understood to adopt the charge hopping mechanism. The charge transport is governed by the Arrhenius law $\mu=\mu_o \exp(-E_A/ k_B T)$, where E_A corresponds to the activation energy and k_B is the Boltzmann constant. Since the temperature helps in overcoming the energy barriers introduced by the energetic disorder, the charge mobility and source-drain current increases with increasing the temperature.

5.3 Experimental section

Top-contact devices were prepared under ambient condition. A heavily n-doped silicon wafer with a 200-nm thermal SiO_2 layer was used as the substrate/gate electrode. The SiO_2/Si substrate was cleaned with acetone, and IPA. The surface treatment can be seen in the reference. The ODTS (1-octadecyltrichlorosilane) treatments were done by vapor treatment for 3h at 120 ^{o}C in the vacuum. The AlO_x

dielectric was processed in the following: 50 nm patterned Al gate electrode deposited on the Si substrate with thermal evaporation, then treated with O_2 plasma for 20 min, and after that the substrate was treated with 3 mM ODPA solution in IPA for 18 h, after washed with IPA, and dried with N_2 gas. The resulting device capacitance was measured with capacitance voltage measurement unit (4210-CVU) to be 400-600 nF/cm^{-2}. The semiconductor layer was deposited on top of the organosilanes modified SiO_2 and ODPA modified AlO_x surface by coating the solution of DPP in DCB solvent with a concentration of 4 mg/mL. The thin films were then vacuum annealed at 160 ^oC for 10 min in vacuum oven. Subsequently, gold source/drain electrode pairs were deposited by thermal evaporation through a metal shadow mask to create a series of FETs with various channel length (L = 50 - 100 um) and width (W = 1 mm) dimensions. The FET devices were then characterized using a Keithley SCS-4200 probe station under ambient condition or N_2 glovebox in the dark. The temperature measurement was controlled by the model 9700. To minimize the leakage current, small trenches in the thin film around the electrodes were created with a needle. The devices were isolated to reduce the fringing effects which can induce an overestimation of drain current and large leakage current.

Model coatmaster 510 film applicator and drying time recorder units (ERICHSEN) were used to produce the thin film. AFM images were recorded on a tapping mode atomic force microscopy (AFM) (Bruker ICON-PKG AFM). XRD measurements were performed on a 2D GADDS X-ray diffraction (XRD)

(Bruker-AXS D8 DISCOVER GADDS).

5.4 Conclusions

In conclusion, slot die coating processes for diketopyrrolopyrrole-based copolymer (DPPT-TT) that resulted in high OTFT charge carrier mobility values of 4.6 - 7.2 $cm^2V^{-1}s^{-1}$ when measured in ambient, and 8.9-10.2 $cm^2V^{-1}s^{-1}$ when measured in nitrogen were developed in this study. The OTFT performance was increased by up to three times compared to that of the spin coated devices. Moreover, a hybrid inverter based on *p*-type DPPT-TT and *n*-type ZnO with good switch characteristics at different V_{dd} operation was realized. Furthermore, the OTFT device with native grown AlO_x as the dielectric exhibited good operating characteristics with the operating voltage below 3 V. These low-voltage OTFTs also demonstrated good temperature sensing characteristics that can be further developed for diagnostic applications. This study showed the feasibility of this technique not only for small molecule system but also suitable for polymer system.

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Chapter 6 Water Induced Zinc Oxide Thin Film Formation and its Transistor Performance

6.1 introduction

Metal oxides for thin film transistors (TFTs) have gained increasing interests in past few years due to their high electron mobility, moderate processing temperature, high optical transparency, and so on.[1-6] Traditionally, metal oxide TFTs have been processed by vacuum deposition such as sputtering,[7] pulsed laser deposition,[8] and chemical vapor deposition.[9] These processes are costly for large area deposition and incompatible for plastic substrates due to high processing temperatures. Solution based deposition processes are desirable for simple to practice, easy to pattern, and scalable to large area.[10-14] Recent reports have shown that metal oxide based thin film semiconductor can be prepared from various soluble metal oxide precursors through the hydrolysis process.[15-17] The hydrolysis process is induced by incorporating an aqueous catalyst (acid or base) to the precursor solution before the thin film formation. The precipitation or metal oxide gel may be formed, during the hydrolysis, due to high reactivity of metal oxide precursors.[18] In contrast to hydrolysis, the non-hydrolyzed process requires high temperature calcinations, which cannot be accommodated by low thermal budget materials/processes.

Recent studies have shown that annealing metal oxides in humid environment

(water vapor) enhanced TFT performance due to increased metal oxide formation.[18] Other studies discovered that water adsorption at the metal oxide semiconductor surface changed its conductivity and introduce hysteresis in TFTs.[19-20] Hence, it is important to quantify water effects in ZnO thin film formation (hydrolysis process), quality, and the ZnO TFT performance.

In this study, an in-depth investigation is conducted to reveal the effects of water incorporation in ZnO precursor solutions for ZnO thin film formation and its TFT device performance. Using water as an additive in ZnO precursor eliminates water vapor assisted annealing during the formation of ZnO thin film, and yields a simple in-situ hydrolysis process within the ZnO film. The TFTs are test vehicles for characterizing ZnO thin film semiconductor. The device environmental stability and voltage bias stability are studied to demonstrate the ZnO TFTs robustness for practical applications.

6.2 Results and discussion

6.2.1 Thin film surface characterization

A 50 nm ZnO thin film on Si substrate is characterized by 2D XRD and the result is shown in Figure 6.1a. The presence of weak diffraction peaks infers a weak Wurzite crystalline phase. The crystalline Wurzite structure with weak (002) orientation is further confirmed with a compressed ZnO nanoparticle sample (here not shown).

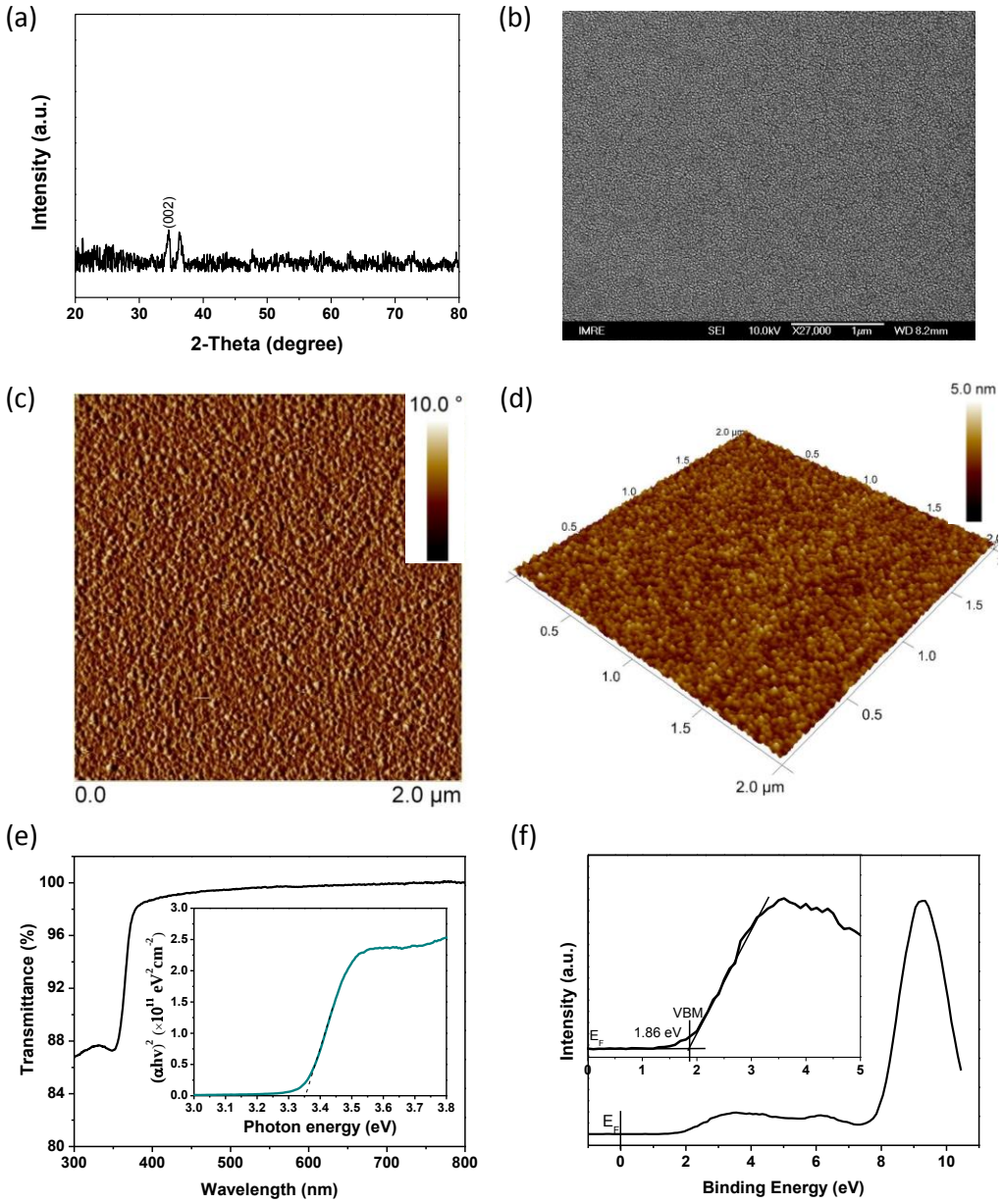

Figure 6.1 (a) Two-dimensional XRD pattern of ZnO thin film annealed at 250 ℃ on silicon substrate. (b) The FESEM image of the ZnO thin film annealed at 250 ℃ on silicon substrate. (c-d) The phase and topography images 250 ℃ annealed ZnO thin film on silicon substrate. (e) Optical transmission spectra of the ZnO thin film on quartz substrate (Inset is the absorption coefficient as a function of photon energy). (f) Valence band spectrum of the ZnO thin film (Inset is the zoom-in image of the spectra near Fermi-energy of ZnO surface).

The ZnO surface morphology is studied using FESEM and tapping-mode AFM. The FESEM image shows a smooth surface with the crystal size in the nanometer range (Figure 6.1b). This is further confirmed by tapping-mode AFM analysis. As

shown in Figure 6.1c-d, the phase and topography images reveal high quality thin film with surface roughness of 0.33 nm. The ZnO grain sizes are estimated to be about 6.2 nm from the AFM images. This grain size was believed to be beneficial to the mobility and adatom diffusion on the semiconductor surface.[21]

The optical transmission spectra of the ZnO thin film on quartz substrate is shown in Figure 6.1e. From the transmittance spectra, the absorption coefficient as a function of photon energy is obtained. The thin film has good transparency in the visible region with corresponding optical band gap of 3.33~3.35 eV (inset) obtained using the Tauc model,[22] and the Davis Mott model[23] in the high absorbance region. The obtained optical band gap is similar to that of polycrystalline ZnO (3.37 eV).[24]

The valence band (VB) spectrum of the thin film is obtained by high resolution XPS, shown in Figure 6.1f and the insert. From the zoomed-in spectrum near Fermi-energy at the ZnO film surface (the inset), the valence band maximum (VBM) of 1.86 eV (calibrated) is calculated.

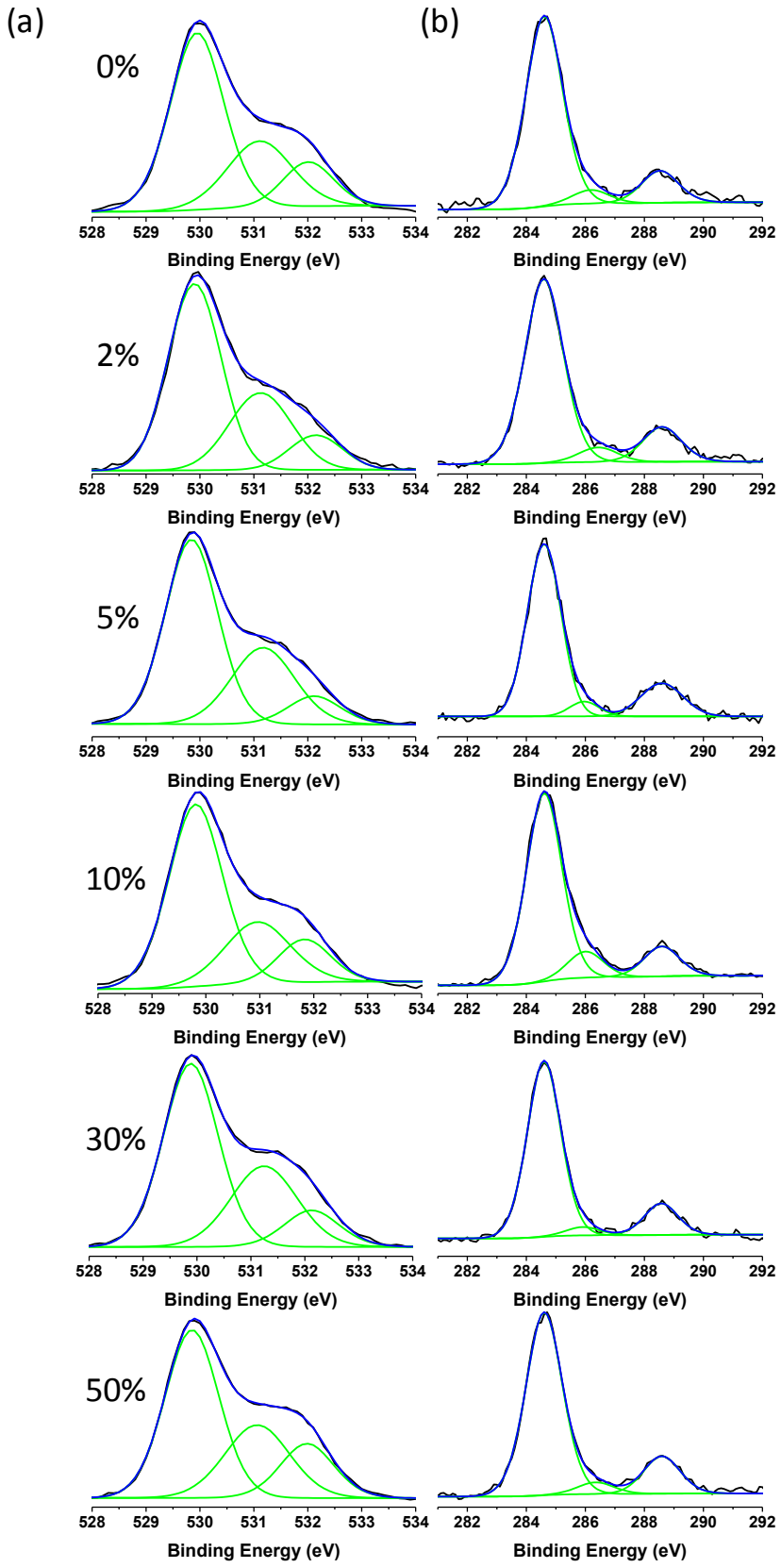

Figure 6.2 O1s (a) and C1s (b) XPS spectra for annealed (at 250 ^{o}C) ZnO thin films with different water contents from volume ratio of 0% to 50% in the precursor solutions.

XPS analysis is used to differentiate oxygen states in the ZnO thin films obtained from ZnO precursor solutions containing different water ratios. Figure 6.2 displays the detailed C 1s and O 1s scans. There is no noticeable difference in peak shape and main peak position for the ZnO films annealed at 250 ^{o}C. The three O1s core level peaks under the broad shouldered oxygen peak can be assigned to a ZnO lattice peak (529.9 eV), ZnO lattice peak in the oxygen-deficient region (531.2 eV), and Zn hydroxide peak (532.1 eV).[25] For dry-annealed ZnO film with 0% water in the precursor, the metal hydroxides are about 14.0%, while the data obtained from ZnO film with 2% water incorporation only show 6.3% hydroxides at the same annealing conditions. By increasing water volume percentage to 50% in ZnO precursor, ZnO hydroxides are increased to 17% which is the result of the O-H bond in H_2O trapped in the bulk thin films. Higher hydroxide content means more defect sites, which deteriorate the charge carrier mobility resulting in poor TFT device performance. For C 1s core levels, the peak located at 284.6 eV, as a reference peak, is attributed to C-C and C-H moieties. The higher binding energy peaks can be assigned to carbon oxide groups.[26]

Thin film transistor characterization

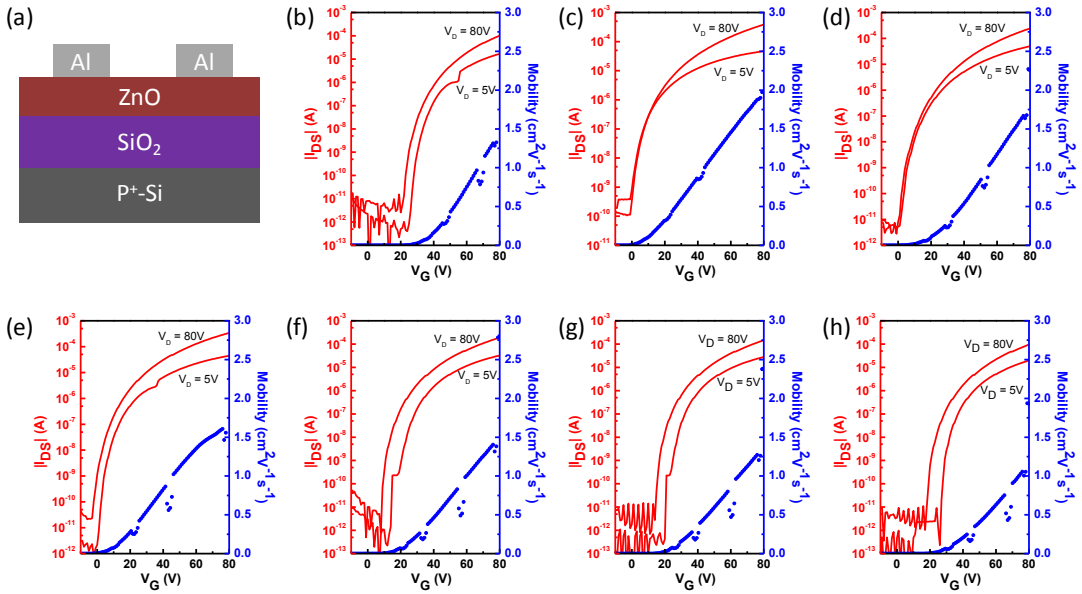

Figure 6.3 (a) The device structure used in this study. (b-h) Transfer curves of ZnO TFTs fabricated with different conditions (dry annealing, water vapor annealing, water volume ratio of 2%, 5%, 10%, 30% and 50% in the precursor solutions, respectively). Red: drain current; blue: extracted field-effect mobility as a function of gate voltage. The transfer characteristics were acquired with a source–drain voltage of 5 V and 80 V.

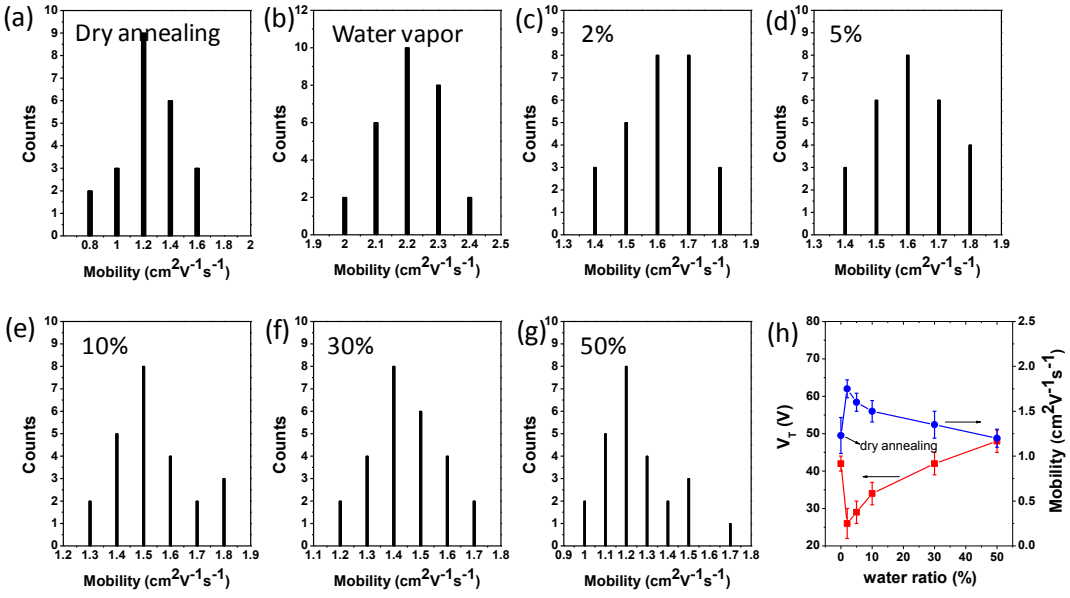

Figure 6.4 (a-g) The statistical data of the mobility based on the ZnO thin film with different water ratio, (h) the V_T and mobility as a function of water ratio in the precursor solutions.

Table 6.1 Field-effect mobility (μ), threshold voltage (V_T), and current on/off ratio ($I_{on/off}$) of ZnO TFTs made from different ZnO precursor solutions and process conditions.

Water content	μ_{ave} [$cm^2V^{-1}s^{-1}$]	μ_{aged} [$cm^2V^{-1}s^{-1}$][a]	V_T [V]	I_{On}/I_{Off}
0%	1.2±0.4	1.5±0.2	41-45	10^6-10^7
Water vapor[b]	2.2±0.2	-	25-29	10^7-10^8
2%	1.7±0.2	2.3±0.1	27-31	10^7-10^8
5%	1.7±0.2	2.3±0.1	28-32	10^7-10^8
10%	1.5±0.2	2.2±0.1	34-38	10^7-10^8
30%	1.4±0.3	2.0±0.2	40-43	10^6-10^7
50%	1.2±0.4	1.9±0.2	46-50	10^6-10^7

a) TFT mobility after aging in N_2 conditions for two weeks. b) The device treated with water vapor during annealing.

The ZnO thin film transistor is a test vehicle for studying the semiconducting characteristics of the ZnO film. Figure 6.3a shows the TFT based on a bottom gate and top contact structure with typical channel length (*L*) and channel width (*W*) of 100 μm and 1000 μm, respectively. The TFT transfer curves measured by Keithley 4200 are shown in Figure 6.3b-h. The TFTs exhibit excellent switch characteristics at given drain bias voltages. Figures 6.4 (a-g) present statistics of field effect mobility (μ) of the ZnO TFTs at different water contents and different process conditions. Figure 6.4h summarizes the average mobility and the threshold voltage (V_T) with standard deviation for different precursor solutions. The ZnO film, with 0% water incorporation, after dry annealing at 250 ^oC resulted low TFT performances: low field effect mobility (1.2 $cm^2V^{-1}s^{-1}$) and high V_T shift (41-45V). With annealing temperature increased to 350 ^oC, the mobility of the TFT device increases to 2.0 $cm^2V^{-1}s^{-1}$. When the ZnO film is annealed with present of water vapor at 250 ^oC, the TFT device mobility is 2.2 $cm^2V^{-1}s^{-1}$ with lower V_T shift (25-29 V): 80% increasing in

mobility comparing to that of dry annealed devices at the same temperature. This is expected due to more efficient ZnO conversion from its hydroxides and further by electron donation of polar water molecules to enhance free carrier concentration and conductivity during the charge transfer between ZnO and water molecules ($H_2O(g) \rightarrow H_2O^+(ad) + e^-$).[18-19] An illustration of this phenomenon is given in Figure 6.5. Similarly, the thin films with 2% and 5% water have also resulted in good transistor performance with higher filed mobility (up to 1.8 $cm^2V^{-1}s^{-1}$) and relatively lower V_T shift. In addition, less hysteresis of transfer curves is observed due to less charge traps existed in the ZnO films (Figure 6.6). When increasing water content further in the precursor solutions, the ZnO TFT performances are lower with decreased μ, increased V_T and turn-on voltage, summarized in Figure 6.4h. It is generally believed that the lower TFT performances are the result of increased trap density from excessive water in the ZnO film. The trap sites are formed during charge transport. The trap concentration can be estimated by the displacement of V_T ($N_{tr} = C_i\Delta V_T/e$), which is increased with increasing water content. In the case of 50% water content, the calculated trap concentration at the ZnO semiconductor and dielectric interface is 5.1×10^{12} cm^{-2}, the highest in the study. The positive V_T shift is the result of enhanced acceptor like traps from the extra water trapped in the ZnO thin films.[19] When testing the device in vacuum or N_2 environment, hysteresis diminishes as a result of the desorption of H_2O molecules from the ZnO film, thus reducing surface induced traps.

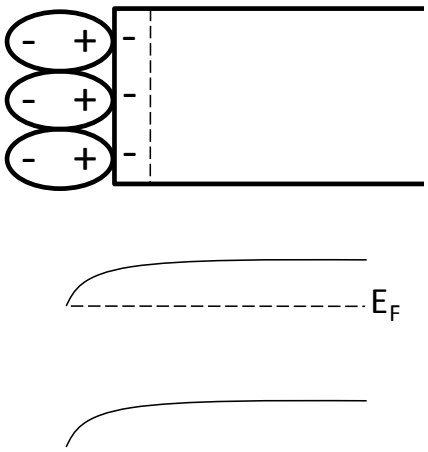

Figure 6.5 Illustration of polar water molecule and ZnO interaction and ZnO band bending as results of water assisted annealing.

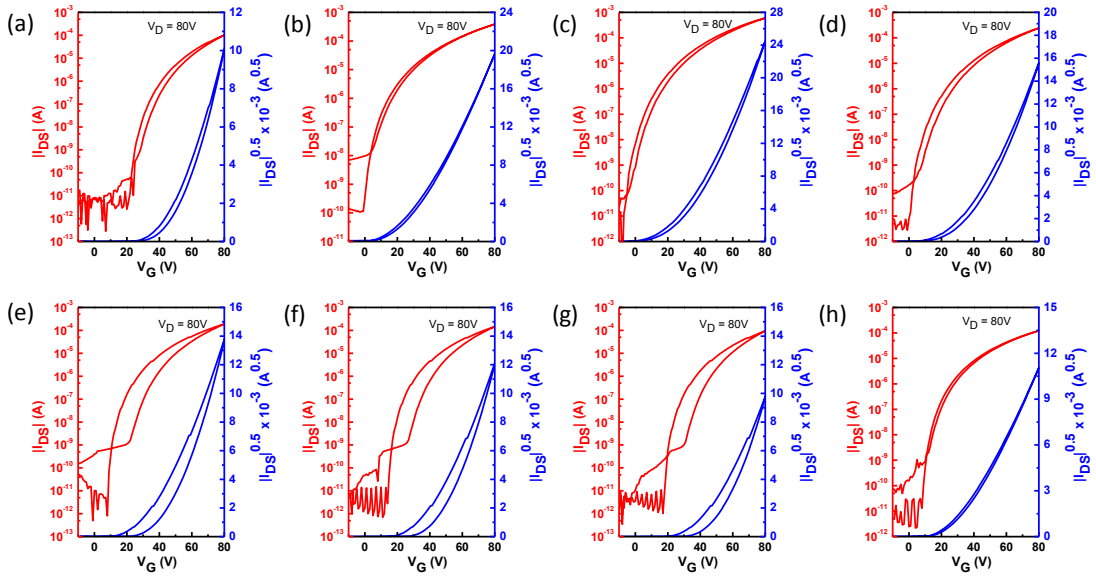

Figure 6.6 The hysteresis voltage (Vh) from the typical transfer characteristics of the ZnO devices based on different conditions (dry annealing, water vapor annealing, and water volume ratio of 2%, 5%, 10%, 30% and 50%) (a-g). (h) The TFT device of (e) test in N2 conditions.

There are two experiments to quantify aging effects: 1) in the air with constant humidity (40%) for one week, and 2) in the vacuum or inert condition (water and oxygen free) for two weeks. With the devices are stored in the air, the V_T shift is toward the negative voltage direction and the off current is increased rapidly from 10^{-12} Amp to 10^{-8} - 10^{-9} Amp resulting in lower On/Off current ratio (Figure 6.7). This

was reported as surface-induced time-dependent instability effect.[27] When the devices are stored in the vacuum or inert environment, the ZnO TFTs from precursors with 2%-30% water show improved performances. The device mobility μ and threshold voltage V_T approach to their equilibrium values at 2.0-2.3 $cm^2V^{-1}s^{-1}$ and 23-30 V respectively. The turn-on voltage is around 0 V, shown in Figure 6.8. This is clearly evidence of 1) the conversion from Zn hydroxides (e.g. $Zn(OH)_2$) to ZnO has reached its equilibrium and 2) the extra water has been removed from ZnO film at the given extended time and environment conditions. In the case of TFTs made of ZnO precursors with 0% and 50% water, the devices exhibited lower performances even after aging in the vacuum or inert environment, which suggests that the defects introduced during the formation of the ZnO thin film are permanent: the lack of water during hydrolysis (0% water) and excessive water (50% water) incurring trapping sites in the ZnO thin film.

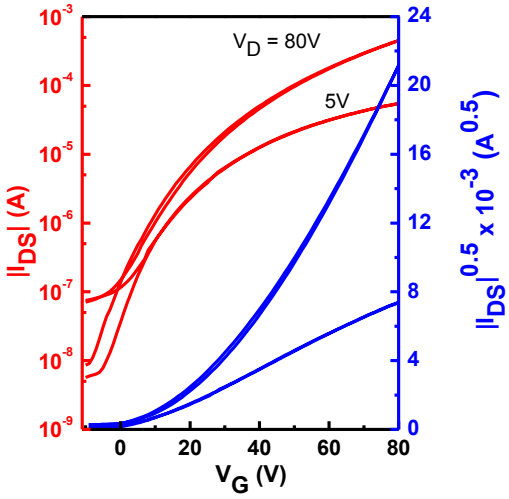

Figure 6.7 Transfer characteristics of TFTs based on ZnO films after stored in air for one week.

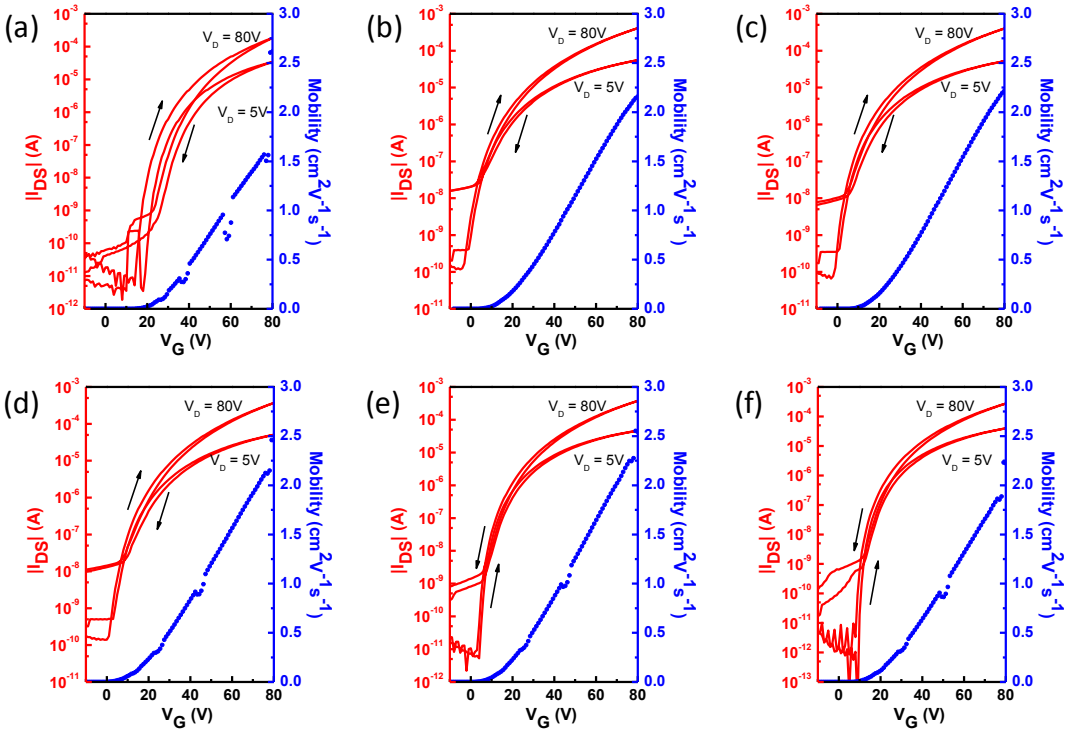

Figure 6.8 The device stabilities of the ZnO thin film with different water ratio in the precursor solutions stored in N_2 for two weeks tested in ambient conditions (a: dry annealing, b-f: water volume ratio of 2%, 5%, 10%, 30% and 50%).

The conversion mechanism from the ammonia–aqueous ZnO precursor solution to ZnO semiconductor is illustrated in Scheme 6.1.[28-29] When water is introduced into the precursor solution, the solution pH is decreased resulting in complex ($Zn(NH_3)_4^{2+}$) to Zn^{2+} and NH_4^+ ions deformation. Then the Zn^{2+} and OH^- react to form zinc hydroxide ($Zn(OH)_2$) which is easily decomposed to ZnO at about 100 ^oC.

1) $ZnO + 4NH_3(aq) + H_2O(l) \longrightarrow Zn(NH3)_4^{2+}(aq) + 2OH^-$

2) $\xrightarrow[pH\downarrow]{+4H_2O} Zn^{2+} + 4NH_4^+(aq) + 6OH^-$

3) $\longrightarrow Zn(OH)_2(s) + 4\ NH_3(g) + 4H_2O(l)$

4) $Zn(OH)_2 \xrightarrow{\triangle} ZnO(s) + H_2O(g)$

Scheme 6.1 Schematic description of the mechanism for ammonia-ZnO precusor solution.

When excessive water is introduced during the ZnO film formation, the water is adsorbed by the bulk thin film. These water molecules act as acceptor-like traps in the TFT source/drain channel, thus the trap density increased. As shown in Table 5.1, the V_T has changed from 27 V to 46 V when the water content increased from 2% to 50%, and the mobility has decreased from 1.8 $cm^2V^{-1}s^{-1}$ to 1.2 $cm^2V^{-1}s^{-1}$ accordingly. Therefore, only small amount of water, 1-2% crystalline water, is sufficient to enhance the ZnO solubility in ZnO precursor solution and to promote the hydrolysis during the ZnO film formation.

The low temperature processability of ZnO has been evaluated in this study. A set of experiments are designed to investigate the annealing temperature and subsequent aging effects on the TFTs performances. Figure 6.9 (a-b) shows typical I_{DS}-V_G transfer characteristics and field effect mobility for TFTs fabricated using ZnO semiconducting film casted by ZnO precursor with 2% water and annealed at 150 ℃. The devices are characterized again after 12 hrs storage in vacuum or nitrogen environment. The average mobility obtained from the low temperature annealed TFT devices is 0.15 $cm^2V^{-1}s^{-1}$, comparing to 1.76 $cm^2V^{-1}s^{-1}$ of same configured device annealed at 250 ℃. The reduced mobility is the result of incomplete ZnO lattice formation at 150 ℃. It is worth notice that the low temperature processed TFTs exhibit very good electrical field response, e.g. excellent saturation characteristics and large I_{on}/I_{off} ratio. After the device stored in the nitrogen or vacuum environment for 12 hrs, the device performances increase more than 2× due to water desorption

resulting the reduction of traps density (Figure 6.9b). The extended thermal annealing at 150 ℃ for 12 hrs gives even higher TFT performances (μ = 0.36 $cm^2V^{-1}s^{-1}$) due to continuous ZnO conversion at the extended annealing time at the elevated temperature. The performance of the ZnO TFT annealed at 150 ℃ in this study is higher than most n-type TFTs (organic and inorganic) processed at similar temperature. Therefore, the lower temperature conversion of Zn hydroxide to ZnO using the proposed ZnO precursors with calculated water content can enable the low cost printed electronics applications.

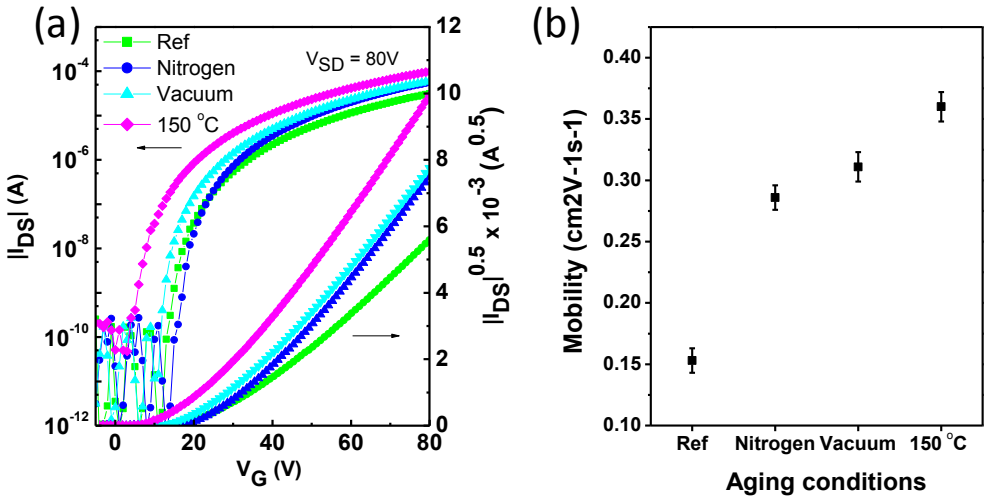

Figure 6.9 (a-b) The transfer and output characteristics of ZnO TFTs at annealing temperature of 150 ^oC test in N_2 conditions.

The operational stability of ZnO thin film transistors is evaluated with on/off cycle test and bias stress test. As shown in Figure 6.10 a,c, the TFT annealed at the present of water vapor results near constant current during the on/off cycle (Figure 6.10 a) and almost no hysteresis and V_T shift (Figure 6.10 c). However, as shown in Figure 6.10 b, d, the TFT with 10% or more water content results decreased

on-current during the on/off cycles (Figure 6.10b) and drafted threshold voltage under the positive voltage stress (Figure 6.10d), which indicate the existence of the bulk traps by excessive water in the ZnO semiconductor film.

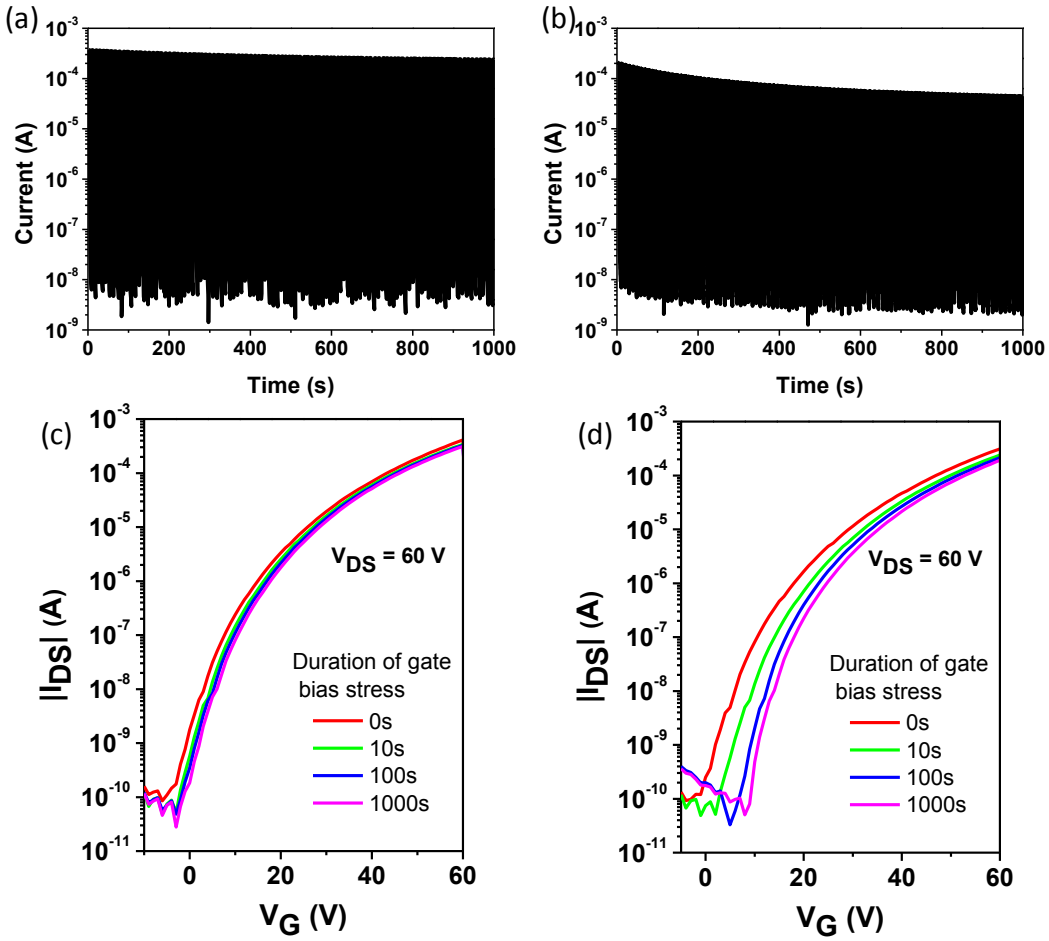

Figure 6.10 Dynamic stress test of a ZnO TFT with water vapor annealing (a) and 10% water content in the precursor solutions (b) during continuous cycling between ON (VG = 60 V) and OFF (VG = 0 V) states; bias stress test of the ZnO TFT with water vapor annealing (c) and 10% water content in the precursor solutions (d) with + 20 V bias.

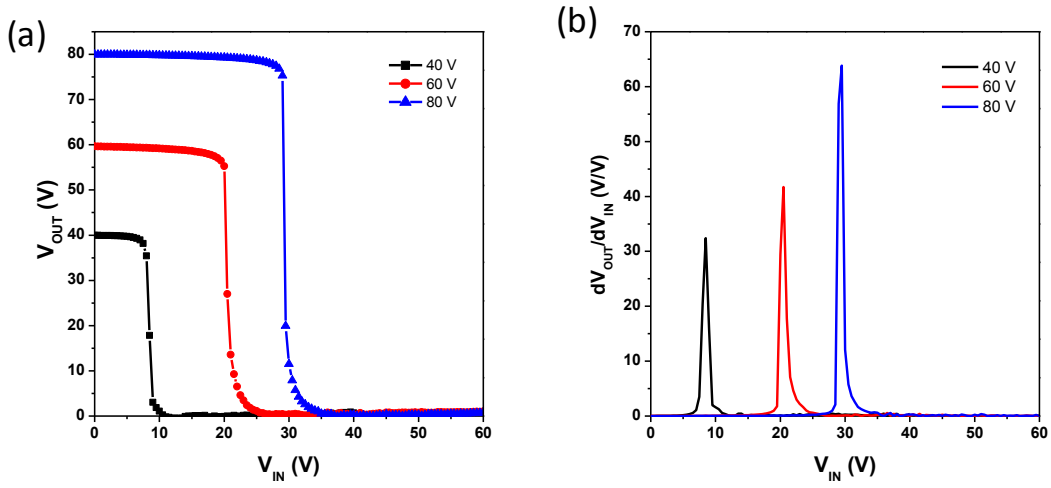

Figure 6.11 (a) Voltage transfer characteristics of a complementary inverter of TIPS-pentacene and N-type ZnO with various supplied voltages. (b) The plots of gains ($-dV_{OUT}/dV_{IN}$) that correspond to the voltage transfer curves.

CMOS inverters were realized combined two connected transistors with n-type ZnO as N-MOS and p-type TIPS-pentacene as P-MOS using slot die coating method. A common gate (Si) was used as the input voltage. Due to the difference in mobility between ZnO and TIPS-pentacene, the CMOS inverter threshold voltage shift less than $V_{DD}/2$. The transfer characteristics and signal gain of the inverter measured at different supply voltages (V_{DD}) are depicted in Figure 6.11. As expected, the inverter shows good response, V_{OUT} of the inverter exhibited a sharp inversion at V_{IN} of ~30 V at V_{DD} of 80 V, which corresponds to a maximum voltage gain ($-dV_{OUT}/dV_{IN}$) of 64.

6.3 Experimental part

The precursor is prepared by dissolving the ZnO powder (Sigma Aldrich) in ammonium solution (Sigma Aldrich) to form 0.1M ($Zn(NH_3)_4^{2+}$) complex. For the device fabrication, a heavily doped p-type Si wafer (purchased from Silicon Quest

International, Inc.) was served as the gate electrode and 200 nm of thermally grown SiO_2 was used as the dielectric layer. Prior to spin coating ZnO precursors, the Si/SiO_2 substrates were cleaned with acetone, isopropyl alcohol (IPA) and then treated with Ar plasma to facilitate the thin film formation. After that, ZnO precursors were spun coated at 3000 rpm for 30 s to result in ZnO precursor thin film with around ~10 nm thickness. Then the substrates were annealed at 150 ^{o}C to 250 ^{o}C for 1h. Finally, Al electrodes were deposited on the ZnO thin film with a shadow mask. The transistors were characterized with Keithley 4200 semiconductor analyzer in the air condition or N_2-filled glove box. The field-effect mobility of the fabricated transistor was extracted using the following equation in the saturation regime from the gate sweep: $I_D = W/(2L)C_i\mu(V_G–V_T)^2$, where I_D is the drain current in the saturated regime, μ is the field-effect mobility, C_i is the capacitance per unit area of the gate dielectric layer (SiO_2, 200 nm, C_i = 17 nF cm^{-2}), V_G and V_T are gate voltage and threshold voltage, and W and L are channel width and length (1000μm/100μm), respectively.

Surface properties of the ZnO film were characterized by two-dimensional X-ray diffraction (2D XRD) on the Bruker-AXS D8 DISCOVER GADDS.The transmittance spectra of the ZnO films deposited onto quartz substrates were characterized by using an UV-3600 Shimadzu UV-Vis-NIR spectrophotometer. The surface morphology and the roughness of the ZnO film deposited on silicon substrate were studied by tapping-mode atomic force microscopy (TM-AFM) performed on a Bruker ICON-PKG atomic force microscope. X-ray photoelectron spectroscopy (XPS)

experiments were carried out at the Escalab 220i, monochromatic Al-Ka (1486.6 eV) as the radiation sources.UPS experiments which were carried out at the Escalab 220i, and He I (21.2 eV) as the excitation sources.

6.4 Conclusions

In summary, this study investigated ZnO semiconducting film formation and ZnO TFT performances through hydrolyzing ZnO precursors with different water concentration. It was found that introducing controlled amount of water molecules, either in the form of water vapor during annealing or as an additive in the ZnO precursor solutions, has enhanced the ZnO thin film quality by improving the yield of polycrystalline ZnO from its hydroxides. However, excessive amount of water molecules in the ZnO precursor was undesirable due to the formation of acceptor-like traps in ZnO thin film, led to lower TFT mobility, greater V_T shift and hysteresis voltage, thus degrading TFT performances. In addition, this study has also found that the water vapor or the optimal amount of crystalline water promoted ZnO hydrolysis at low temperature (as low as 150 ^oC) and resulted in desirable performances of the ZnO thin film transistors. The low temperature processability of the ZnO precursor enables many low cost printed and flexible electronics applications.

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Chapter 7 Solution-Processed Doped ZnO Films for High Performance Low Temperature Thin Film Transistors

7.1 Introduction

ZnO-based metal oxide semiconductors have been intensively studied as an active channel material for thin film transistor (TFTs) and solar cells.[1-3] Compared to n-type organic materials, inorganic ZnO shows several advantages such as inexpensive, oxidation stable and transparent in the visible region.[4] It can also combine with stable p-type semiconductor FETs for hybrid complementary inverters and logic circuits.[5] However, most ZnO films are deposited by expensive vacuum based techniques such as radio frequency (RF) sputtering,[6] pulsed laser deposition,[7] and physical vapor deposition,[8] or from a sol-gel precursor solution,[9] which usually needs high temperature annealing process to remove the carbon impurities and convert to ZnO. All these processes are incompatible with large area deposition and plastic substrates due to high cost and/or high temperature process. Therefore, solution-processed deposition technique is desirable, which is simple, controllable, and compatible with large area process.

Previously, Keszler*et al*. reported a carbon free method with low temperature process.[10] However, the intrinsic mobility of ZnO is low which restricts its applications. Therefore, developing high performance ZnO thin films is essential in

future plastics electronics. Recently, Li doped ZnO have been reported as a good n-type cationic doping source as electron donor with superior performance up to 50 $cm^2V^{-1}s^{-1}$.[11-12] In addition, the fluorine (F), the radius of which is close to that of oxygen, has been proved to be an appropriate anionic doping candidate with lower lattice distortion compared with Sn, Ga and In doping. Recent investigations revealed that incorporation of low concentration F in ZnO thin film could significantly improve the transmittance in visible region and the mobility of charge carries.[13-14] The question was arising whether we can combine these different dopants to give a synergetic doping effect on the pristine ZnO.

In this chapter, we investigate incorporation of F and alkaline metal (Li, Na, K) into ZnO using aqueous solution processing route. The doped ZnO thin films exhibited electron mobility of 0.54 $cm^2V^{-1}s^{-1}$ when processed at 150 ^oC, and when the temperature of calcination increased to 300 ^oC, the average electron mobility could reach up to 8.9 $cm^2V^{-1}s^{-1}$, with a maximum value of 11.2 $cm^2V^{-1}s^{-1}$ for the F and Li co-doped ZnO. The doping process is facile, and controllable, and the solution is easily prepared using commercial available materials.

7.2 Results and discussion

Generally, most of the used dopants for ZnO are metallic cation dopants, while few studies were reported with the halogen anion dopants. Among the anion dopants, F is the most effective dopant for ZnO matrix. Firstly, the F ion have similar size with

O ions (F^-:1.31 A, O^{2-}:1.38A), which could avoid the lattice distortions. Secondly, when F substitutes an oxygen ion, it could produce a free electron which acts as the charge carrier, and enhance the charge mobility of the TFTs. Furthermore, the F ion could occupy an oxygen vacancy sites acting as the electron trap sites, and finally improve the bias stress stability of the TFTs.

Firstly, the electrical properties of these F doped ZnO were investigate by thin film transistors. Bottom-gate top-contact TFTs architecture was employed in this study. Figures 7.1 show typical transfer plots for TFTs fabricated on Si/SiO_2 with different molar ratio F at a pre-annealing temperature of 300 ℃. These TFTs exhibit excellent n-type response, with high charge carrier mobility and large I_{on}/I_{off} ratio. As the doping concentration has important effect on the final device performance. Therefore, we investigated ZnO:F films fabricated from precursor solutions having various F/Zn ratios. Figure 1b shows the TFTs charge carrier mobilities as a function of the F/Zn ratio for ZnO:F based devices.From the figure, it is clear that when the F content is increased, the electron mobility in saturation increased from 1.0 to 2.6 $cm^2V^{-1}s^{-1}$ with an excellent I_{on}/I_{off} of 10^8 at a doping ratio of 10 mol%. The good charge transport achieved at lower annealing temperature for ZnO:F is the result of the lower conversion temperatures needed for conversion of metal hydroxide to oxide lattices. For the optimum metal composition F/Zn = 10 mol%, we also investigated the effect of annealing the films at temperature of 250 ℃. It was found that when annealing temperature decreased from 300 ℃ to 250 ℃, the mobility decreased from

2.6 to 0.3 $cm^2V^{-1}s^{-1}$ correspondingly due to incomplete ZnO lattice formation.

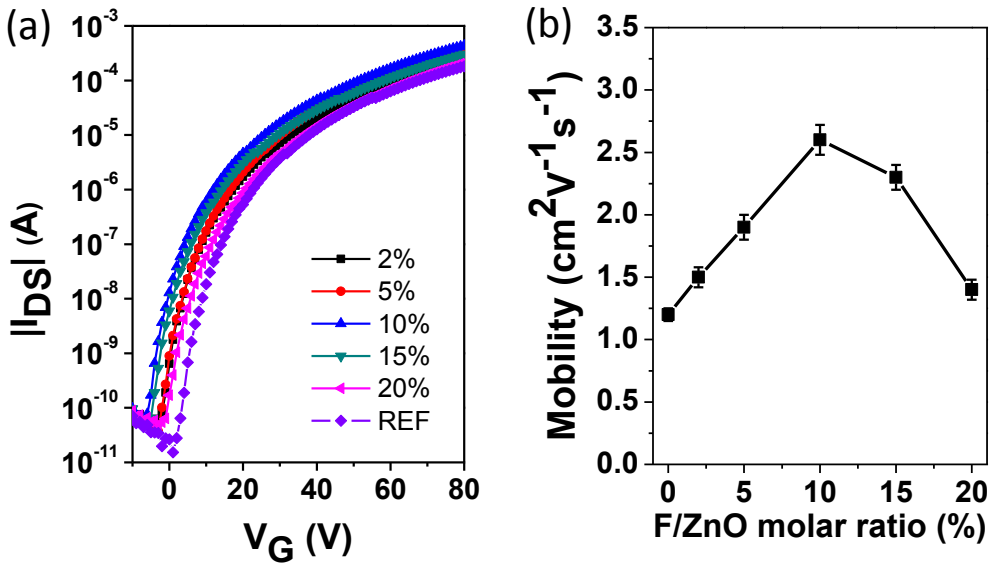

Figure 7.1 (a) The transfer characteristics of the undoped ZnO and F doped ZnO TFTs and (b) the average charge carrier mobilities of the undoped ZnO and F doped ZnO TFTs.

The doping effect on the electrical properties could be well understood by the first principle calculation.[13] According to the calculation, it is evident that F is energetically favorable and could be dominant in ZnO:F, which has been experimentally supported. Fluorine ions occupied at oxygen sites could result in a diminishing of the oxygen vacancies, which can be confirmed by the decrease in the absorption in the visible region due to oxygen vacancies. With high fluorine doping concentration, F_i could appear and act as deep acceptors. The high concentration fluorine in ZnO films may lead to the change in grain size and increase the scattering process, and therefore the majority carries mobility is decreased.

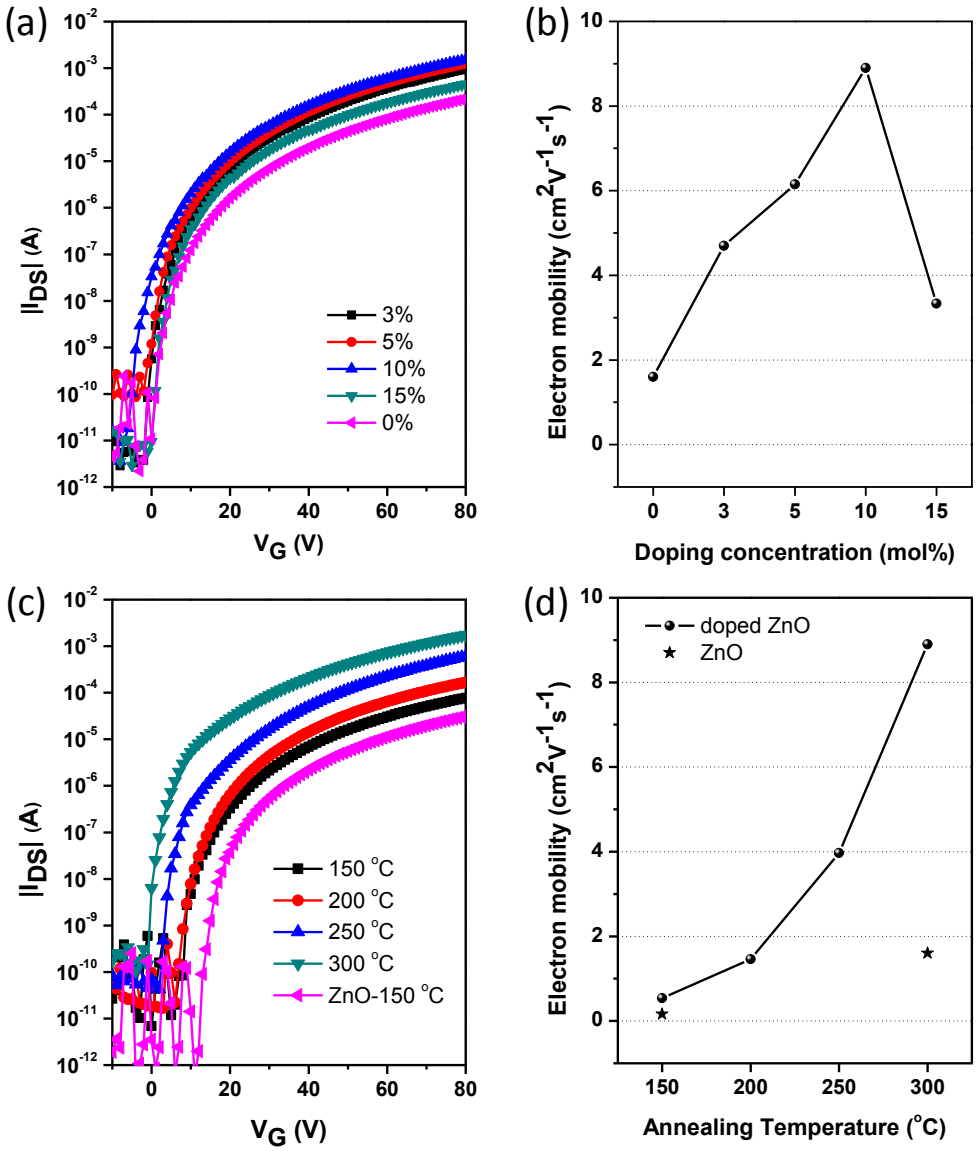

Figure 7.2 (a) The transfer characteristics of LiF doped ZnO TFTs with different doping concentrations. (b) Electron mobility of the LiF doped ZnO TFTs as a function of doping concentrations. (c) The transfer characteristics of 10 mol% LiF doped ZnO TFTs with different annealing temperatures. (d) Electron mobility of the 10 mol% doped ZnO TFTs as a function of annealing temperatures.

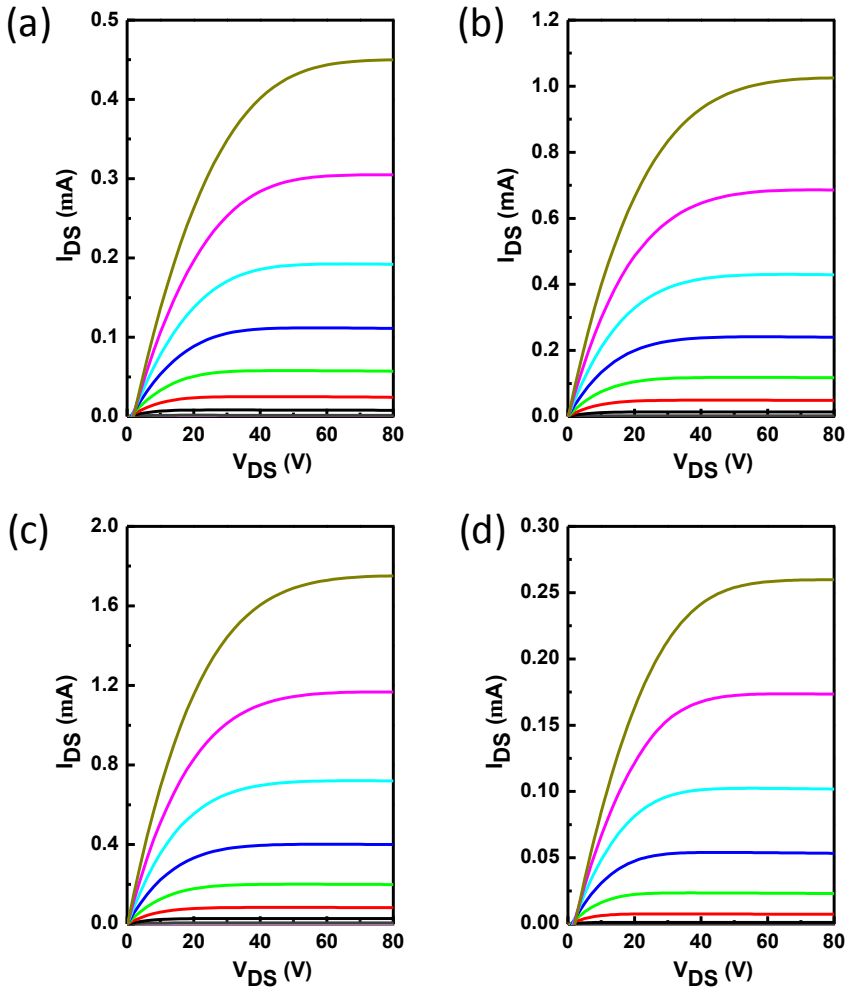

Figure 7.3 The output characteristics of TFTs based on the LiF doped ZnO thin films with the doping molar ratio of 3% (a), 5% (b), 10% (c), and 15% (d) after thermal annealing at 300 ^{o}C for 1h in air (channel = 500 μm/100 μm).

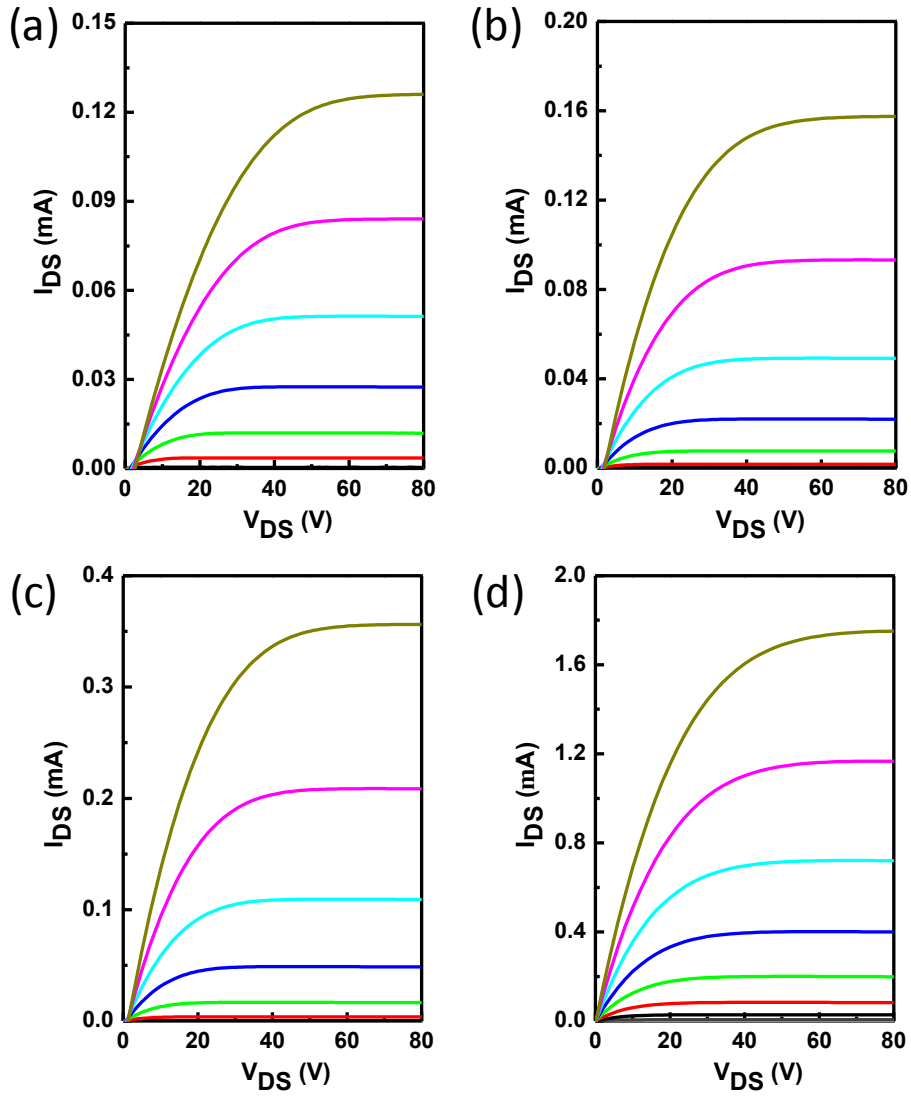

Figure 7.4 The output characteristics of the TFTs based on the 10 mol% LiF doped ZnO thin films under annealing temperature of 150 ^{o}C (a), 200 ^{o}C, 250 ^{o}C (c), and 300 ^{o}C (d) in air.

Then we investigated the effect of alkaline metal (Li used here) incorporation on the TFTs performance. The electrical properties of the Li and F co-doped ZnO films were also characterized by thin film transistors using same structure. Figure 7.2-7.4 showed the transfer and output characteristics for the as-fabricated devices with and without LiF doping. The TFTs exhibited excellent operating characteristics within the operating voltage. Linear behavior at low V_{DS} indicates an ohmic contact at the

Al/ZnO interface. The dopant concentration has significant effect on the device performance (Figure 7.2(a-b), Figure 7.3). The drain current increased upon introducing the LiF into ZnO up to 10 mol%. However, when the doping concentration increased to 15 mol%, the current decreased significantly due to more charge traps formed by excess LiF impurities. In this case, the Li (F) appears to exist at substitutional (interstitial) sites as an acceptor.[13-15] After optimization, the 10mol% LiF doped ZnO films after annealing at 300 ^{o}C exhibited the best performance with average mobility of 8.9 $cm^2V^{-1}s^{-1}$ with a threshold voltage (V_{th}) of 20V, and current on/off ratio of 10^7-10^8. The maximum electron mobility could reach up to 11.2 $cm^2V^{-1}s^{-1}$. This value is among the highest values reported for the low temperature solution-processed ZnO based TFT devices.[16]

In order to investigate the low temperature processability, the TFT devices with different annealing temperature ranging from 150 ^{o}C to 300 ^{o}C were fabricated and the results were shown in Figure 7.2(c-d) and Figure 7.4. Electron mobility up to 0.54 $cm^2V^{-1}s^{-1}$ could be achieved with good transistor operation even when annealed at 150 ^{o}C, indicating that low temperature solution-processed oxide TFTs on flexible substrates could be achievable with carbon-free ZnO thin films as the active layer. When the annealing temperature increased, the electron mobility of the ZnO films increased significantly from 0.54 $cm^2V^{-1}s^{-1}$ to 8.9 $cm^2V^{-1}s^{-1}$ when the thin films were annealed at 300 ^{o}C. This could be ascribed to the increased crystallinity and particle size. Consistent with these results, the threshold voltage and turn-on voltage (V_{on})

gradually decrease with the annealing temperature increase. The charge density in the channel layer, corresponding to the turn-on voltage, increased to $7.44 \times 10^{17} cm^{-3}$ when the doping ratio increased to 10% using the equation $N_T = C_i V_{on}/(qt)$, where C_i is the gate insulator capacitance per unit area, q is the elementary charge, and t is the thickness of active layer. The increment of carrier concentration, which was induced by interstitial Li doing and substitutional F doping, could enhance the field effect mobility.[17]

For the doping mechanism, it has been proved that the Li in the ZnO matrix prefers interstitial sites to substitutional sites due to low electron affinity. When Li occupies the interstitial sites ($Li \rightarrow Li_i^+ + e^-$), it can produce electrons and improve the carrier concentration, which results in high electron mobility.[15] Meantime, the results showed that F occupied in substitutional oxygen sites ($F \rightarrow F_O + e^-$) is more energetically favorable compared to fluorine interstitial sites (F_i).[13] The F_O can effectively diminish oxygen vacancies and decrease the absorption in visible region. The enhancement of the carrier concentration could be explained by the surface passivation effect and the removal of the in-grain scattering centers. Therefore, the co-doping of cation (Li) and anion (F) could have synergistic effect to combine both advantages, which not only increases the carrier concentration, but also decreases the optical absorption. This is desirable for the transparent TFTs.

The operational stability of these thin films was also checked with on/off cycle test in the ambient conditions. As shown in Figure 7.5, the current of the 10mol% LiF

doped ZnO thin film TFT only exhibited slightly current decrease in the initial stage of the on/off cycles, which understood as a “burn-in” effect at the initial stage for all materials and interfaces to be stabilized under the constant voltage bias.

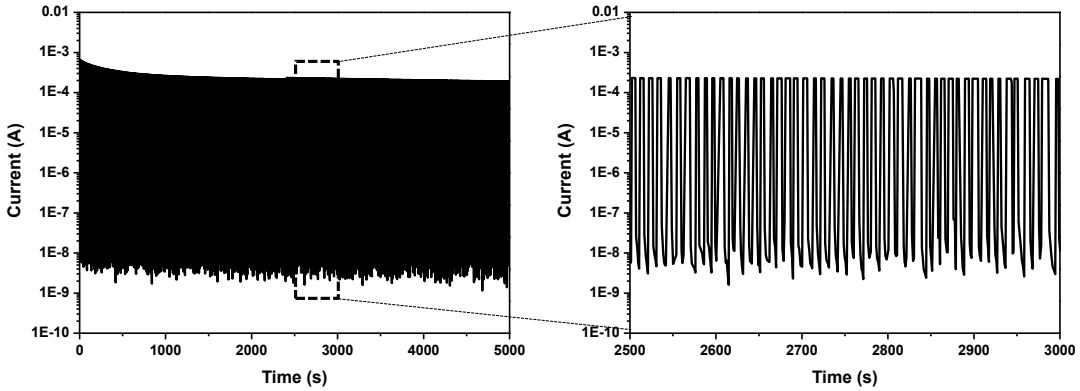

Figure 7.5 Dynamic stress test of a 10 mol% LiF doped ZnO TFT during continuous cycling between ON (V_G = 60 V) and OFF states (V_G = 0 V).

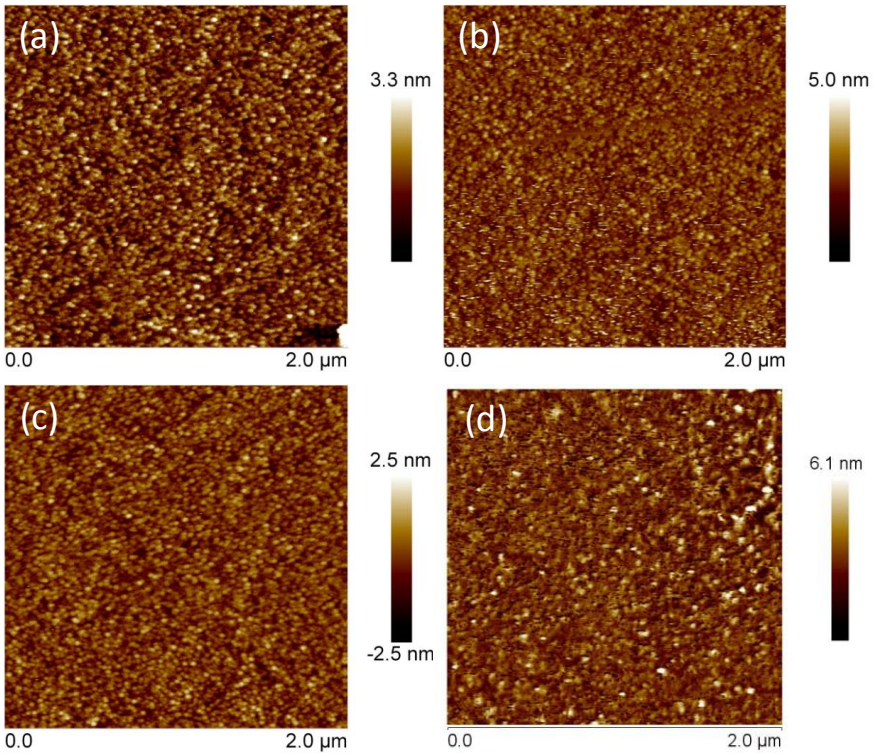

Figure 7.6 The AFM images (2 μm×2 μm) of the LiF doped ZnO thin films with doping concentrations of 3% (a), 5% (b), 10% (c), and 15% (d).

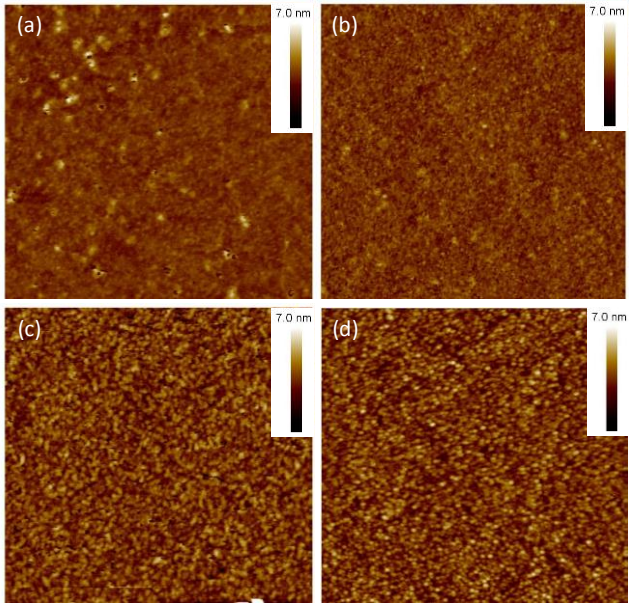

Figure 7.7 The AFM images (2 μm × 2 μm) of LiF doped ZnO thin films annealed at 150 ^{o}C (a), 200 ^{o}C (b), 250 ^{o}C (c), and 300 ^{o}C (d). The RMS values of surface roughness at different annealing temperatures were 0.267 nm (150 ^{o}C), 0.313 nm (200 ^{o}C), 0.403 nm (250 ^{o}C), and 0.485 nm (300 ^{o}C).

The morphology and microstructure of the thin films surface with different annealing temperatures and different doping concentrations were investigated by the tapping-mode AFM and 2D XRD. For different doping concentrations, the topography images almost do not show changes and reveal good quality films with a mean square root (RMS) of surface roughness of 0.47~ 0.51 nm(Figure 7.6). However, the surface morphologies are more related to the annealing temperature (Figure 7.7). Low temperature (150 ^{o}C) annealing gave a smoother and featureless morphology. When the temperature was increased to 250 ^{o}C, the film became more crystalline and had a distinct granular structure. The surface roughness and grain size increased with the increasing of the annealing temperatures. The RMS values of surface roughness at different annealing temperatures were 0.267 nm (150 ^{o}C), 0.313 nm (200 ^{o}C), 0.403 nm (250 ^{o}C), and 0.485 nm (300 ^{o}C), and the grain sizes were estimated to be about

22 ~ 36 nm at 300 ^{o}C. The microstructures of the thin films were evaluated by 2D XRD, the nanoparticle powder of pristine and doped ZnO showed crystalline wurzite structure with weak (002) orientation. However, the thin film annealing at 300 ^{o}C exhibited substantial c-axis oriented growth with preferential (002) orientation (Figure 7.8).The result is consistent with literature reported.[16]

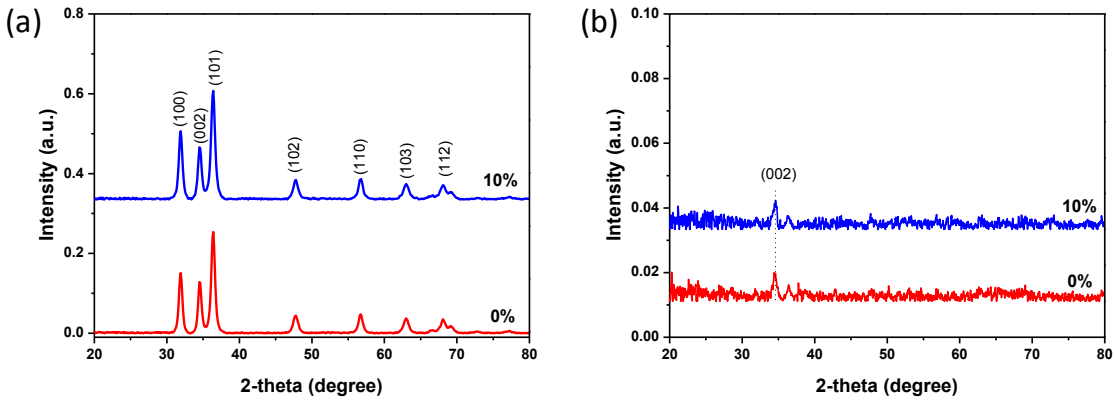

Figure 7.8 X-ray diffraction pattern of the pristine and 10% LiF doped ZnO based on nanoparticle powder (a) and ca. 50 nm thin film (b) after annealing at 300 ^{o}C.

The optical transmittance was measured to investigate the doping effect of LiF on the ZnO optical band gap. Figure 7.9(a) shows the transmittance spectra of the ZnO film with/without LiF doping on the quartz substrates after annealing at the selected temperature (150 ^{o}C-300 ^{o}C) for 10 min. It can be seen that all ZnO films have good transmittances above 95% over the visible wavelength range. From the transmittance spectra, the absorption coefficient as a function of photon energy has been plotted (Figure 7.9(b)), from which the optical band gap of each ZnO film can be easily measured. The absorption coefficient α can be calculated as follows[18]:$T = A\exp(-\alpha d)$, where T is the transmittance of the ZnO film, A is a constant and

approximately unity, and d is the film thickness. The optical band gap of the ZnO films is determined by applying the Tauc model,[19] and the Davis Mott model[20] in the high absorbance region:$\alpha h\nu = D(h\nu - E_g)^n$,where $h\nu$ is the photon energy, E_g is the optical band gap, D is a constant, and n equals to 1/2. The direct optical band gap of the ZnO thin films with/without LiF doping was obtained by plotting $(\alpha h\nu)^2$ versus $h\nu$, as shown in Figure 7.9(b).The E_g value can be obtained by extrapolating the linear portion to the photon energy axis. It can be seen that the band gaps of the ZnO films slightly increased to 3.441eV from 3.386eV after doping with LiF. With annealing temperature increase, the optical band gap values of the doped ZnO films were 3.376eV (200 ^oC), 3.343 eV (250 ^oC), and 3.325 eV (300 ^oC), respectively. The widening of the optical band gap after doping could be explained by Burstein-Moss effects.[21] The doubly occupied state is restricted which need extra energy to excite valence electrons to higher states in the conduction band.

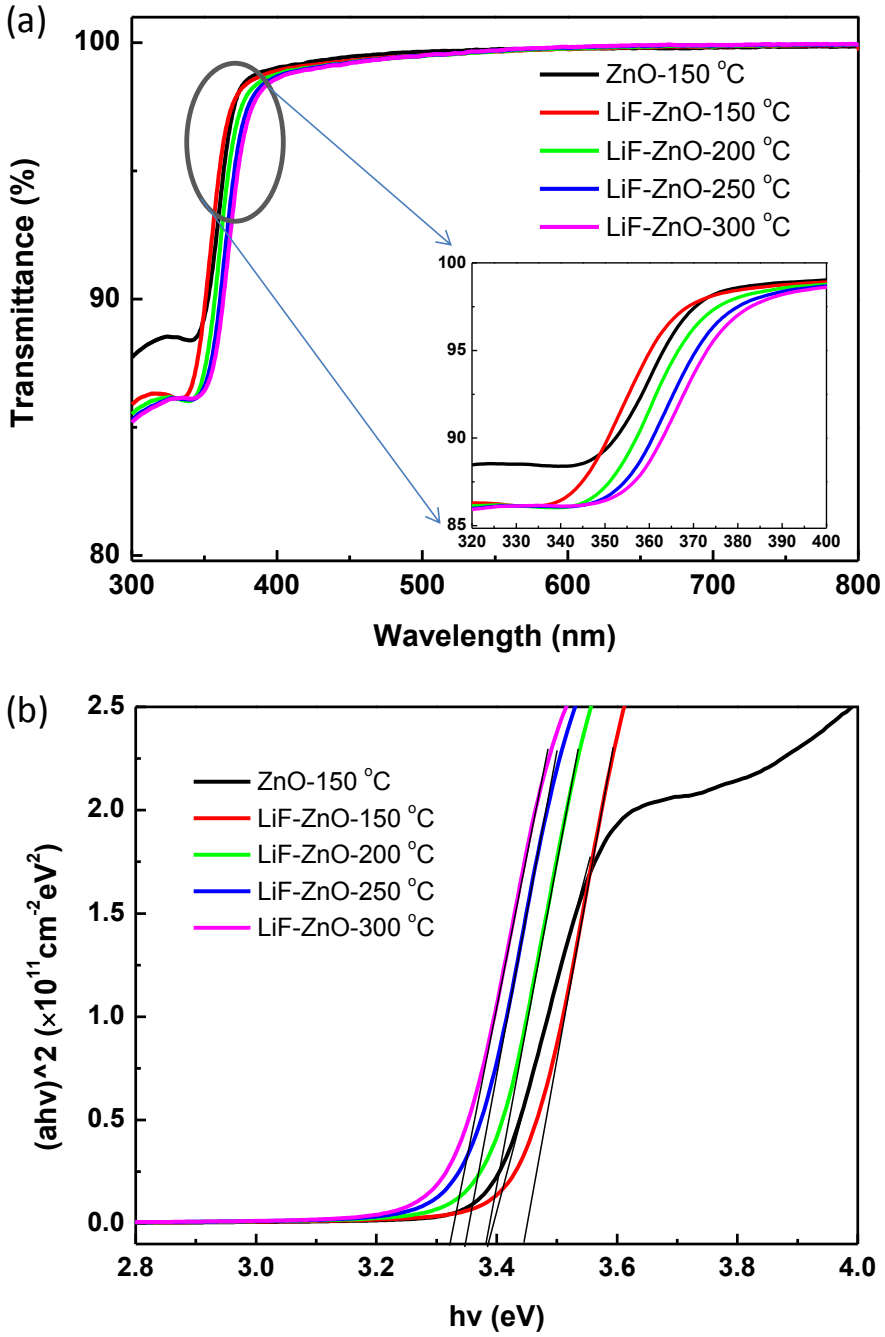

Figure 7.9 (a) Optical transmission spectra of the ZnO and 10 mol% LiF-doped ZnO thin films on quartz substrates after annealing at different temperatures. (b) The absorption coefficient as a function of photon energy.

The chemical structures of LiF doped ZnO was further studied using XPS analysis, as shown in Figure 7.10, due to resolution problem, the F 1s and Li 1s peaks

were not obviously detected. The XPS measurements were also taken to analysis the structural evolution of the thin film after doping. Figure 7.11 shows the O1s XPS spectra for ZnO and 10 mol% doped ZnO thin film annealed at 300 ^{o}C. The peaks centerd at 529.9, 531, and 532 eV can be assigned to oxygen in oxide lattice without vacancy, with oxygen vacancies, and oxygen in hydroxide, respectively. The XPS data indicate that the ZnO thin film annealed at 300 ^{o}C contain large amounts of oxide lattice with or without oxygen vacancies and small amounts of metal hydroxide. At lower annealing temperature, the metal hydroxide content is larger up to 13%, however, upon thermal annealing at higher degree, the metal hydroxide can gradually converted into oxide via thermally-driven condensation process. In the ZnO thin film transistors, the oxygen vacancies and metal hydroxide in the thin film could be act as the trap sites which need to be filling and limit the charge carrier mobility. For LiF doped ZnO thin film, F can occupy the oxygen vacancy sites to reduce the electron trap site and improve the bias stress stability. On the other hand, the fluorine can form hydrogen bonding with hydroxyl groups (-OH) due to its high electro negativity. This can passivate the trap sites of the hydroxyl groups to further improve the stability.

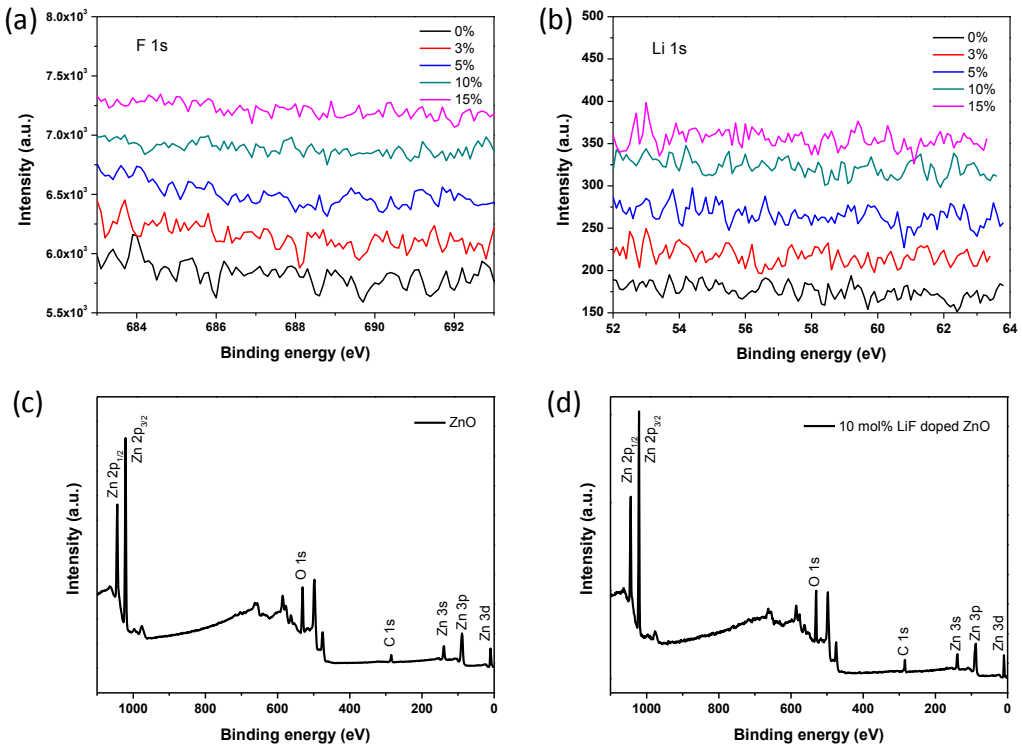

Figure 7.10 The F 1s (a) and Li 1s (b) spectra of the LiF doped ZnO with the doping molar ratio of 0%, 3%, 5%, 10%, and 15% after thermal annealing at 300 ^{o}C for 1h in air. (c-d) the XPS survey spectra of ZnO and 10 mol% LiF doped ZnO.

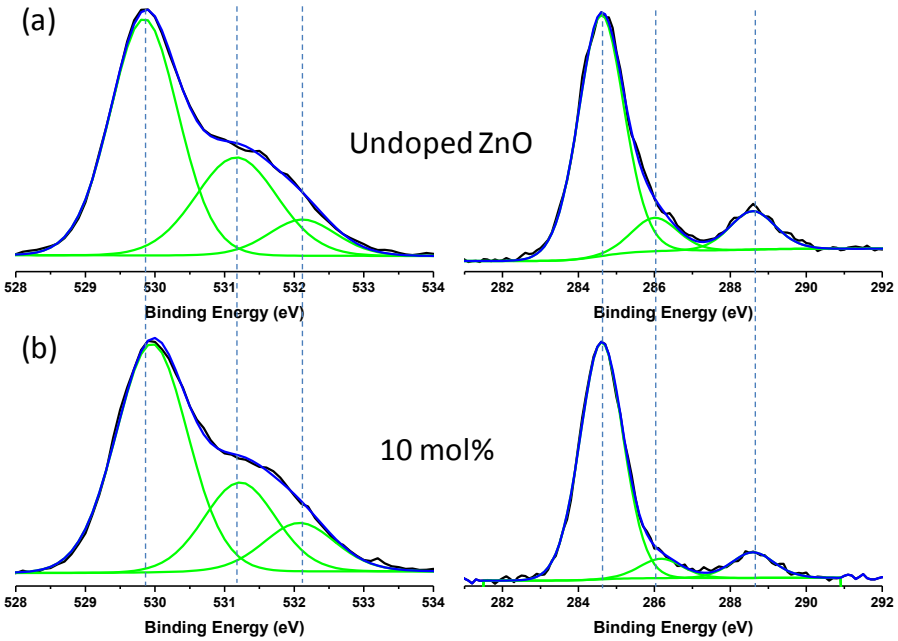

Figure 7.11 XPS spectra of the O1s and C1s core level line for the solution-processed ZnO films with F doping levels of (a) 0.0 mol%, (b) 10 mol%. The three peaks corresponding to the oxide lattice without oxygen vacancies, the oxide lattice with oxygen vacancies, and hydroxide.

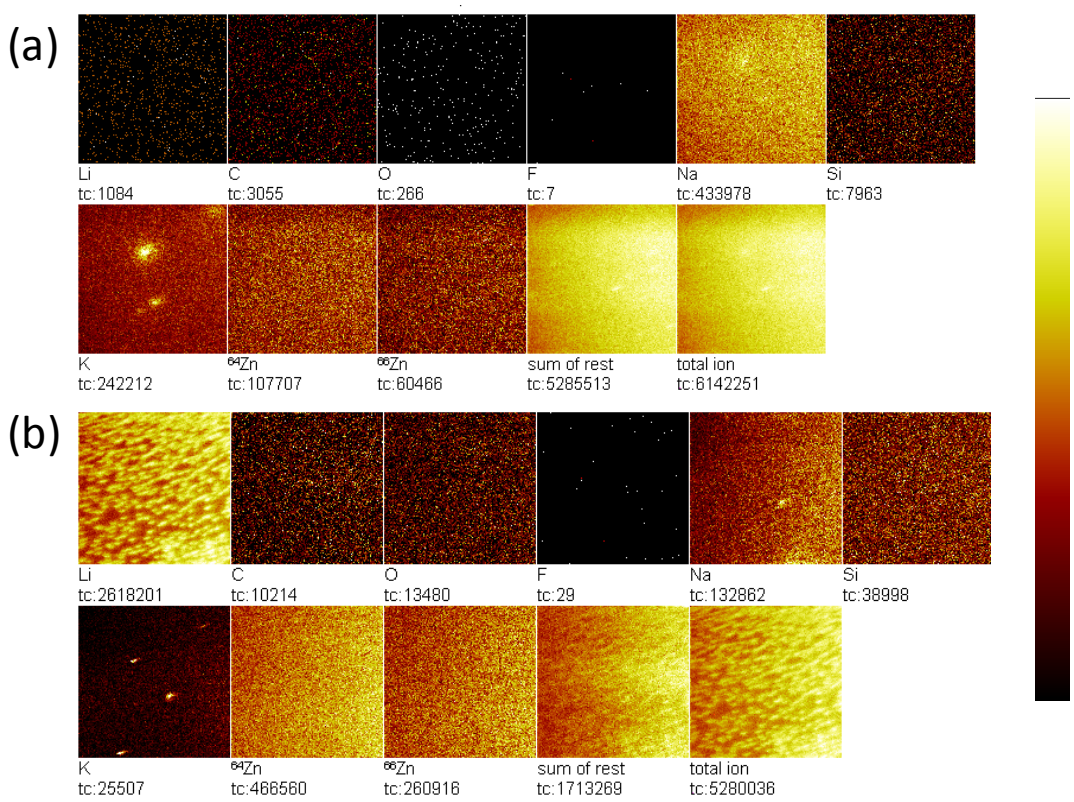

Figure 7.12 The TOF-SIMS results of the pristine and 10% LiF doped ZnO after thermal annealing at 300 ^{o}C for 1h in air.

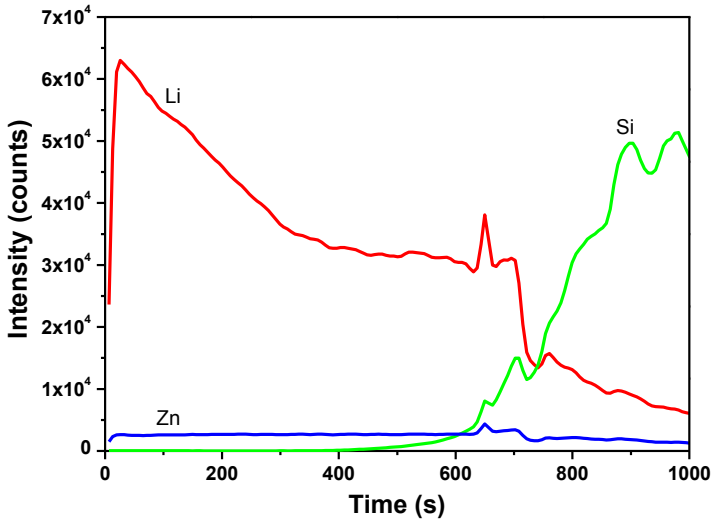

Figure 7.13 The TOF-SIMS depth profile of the LiF doped ZnO with the doping molar ratio of 10% after thermal annealing at 300 ^{o}C for 1h in air.

To confirm the doping ions exist in ZnO films, we carried out TOF-SIMS measurement. The results were shown in figure 7.12-7.13, the Li ion could be well observed, and the depth profile also gives good evidence that high intensity of Li

cations was detected.

7.3 Experimental part

The precursor is prepared by dissolving the ZnO powder (Sigma Aldrich) in ammonium solution (Sigma Aldrich) to form 0.1M ($Zn(NH_3)_4^{2+}$) complex. For different doped ZnO, different molar ratio of NH_4F or LiOH +NH_4F (Sigma Aldrich) was added to the precursor solution and refrigerated for several hours to promote the powder dissolution. For the device fabrication, a heavily doped p-type Si wafer (purchased from Silicon Quest International, Inc.) was served as the gate electrode and 200 nm of thermally grown SiO_2 was used as the dielectric layer. Prior to spin coating ZnO precursors, the Si/SiO_2 substrates were cleaned with acetone, isopropyl alcohol (IPA) and then treated with Ar plasma to facilitate the thin film formation. After that, ZnO precursors were spun coated at 3000 rpm for 30 s to result in ZnO precursor thin film with around ~10 nm thickness. Then the substrates were annealed at 150 ^oC to 300 ^oC for 1h. Finally, Al electrodes were deposited on the ZnO thin film with a shadow mask. The transistors were characterized with Keithley 4200 semiconductor analyzer in the N_2-filled glove box. The field-effect mobility of the fabricated transistor was extracted using the following equation in the saturation regime from the gate sweep: $I_D = W/(2L)C_i\mu(V_G–V_T)^2$, where I_D is the drain current in the saturated regime, μ is the field-effect mobility, C_i is the capacitance per unit area of the gate dielectric layer (SiO_2, 200 nm, C_i = 17 nF cm^{-2}), V_G and V_T are gate

voltage and threshold voltage, and W and L are channel width and length (500μm/100μm or 1000μm/100μm), respectively.

Surface properties of the ZnO film were characterized by two-dimensional X-ray diffraction (2D XRD) on the Bruker-AXS D8 DISCOVER GADDS.The transmittance spectra of the ZnO films deposited onto quartz substrates were characterized by using an UV-3600 Shimadzu UV-Vis-NIR spectrophotometer. The surface morphology and the roughness of the ZnO film deposited on silicon substrate were studied by tapping-mode atomic force microscopy (TM-AFM) performed on a Bruker ICON-PKG atomic force microscope. X-ray photoelectron spectroscopy (XPS) experiments were carried out at the Escalab 220i, monochromatic Al-Ka (1486.6 eV) as the radiation sources.UPS experiments which were carried out at the Escalab 220i, and He I (21.2 eV) as the excitation sources. Time-of-flight Secondary Ion Mass Spectrometer (TOF-SIMS) was performed with the following conditions: Bismuth gun, 25keV, raster at 300 um by 300 um for 300 scan, at positive polarity (good ion yield for Li ions, but poor ion yield for F).

7.4 Conclusions

In summary, F and LiF-doped ZnO thin films have been successfully prepared from aqueous solution at low processing temperature. LiF doping at the appropriate amounts enhanced the oxide film quality and reduced defect sites. The TFTs based on LiF doped ZnO thin films revealed largely improved device performance with average

electron mobility up to 8.9 $cm^2V^{-1}s^{-1}$ compared with the mobility of 1.6 $cm^2V^{-1}s^{-1}$ for non-doped ZnO TFTs. Our results suggest that LiF doping can be a useful technique to produce more reliable and low temperature solution-processed oxide semiconductor TFTs. This study showed that ZnO thin film properties could be well tuned by introducing various doping sources and applied in the optoelectronic device applications.

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Chapter 8 Conclusions and Outlook

The overall objective of this thesis is to investigate the structure-property relationships of organic semiconductors from the structural modification, energy levels, device process conditions, thin film alignment, and their replacement by metal oxide.

Since the electron affinity of the semiconductor materials are correlated with the materials and device properties, the material stability and device stability with respect to energy levels were discussed in detail in chapter 2. The stepwise cyanation of tetrabromonaphthalene diimide gave a series of cyanated compounds. The electron affinity showed a good linear relationship with the number of the cyano groups, and the extremely low-lying LUMO energy levels of tri- and tetracyano- NDIs made them unstable to moisture. The mono- and di-cyanated NDIs however obtained as stable n-type semiconductors and used for air-stable n-channel OFETs with moderate electron mobilities. The devices exhibited typical n-channel behavior and the highest FET electron mobility measured in N_2 was 0.018, 5.1×10^{-4} and 0.050 $cm^2V^{-1}s^{-1}$ for tetrabromo, mono- and di-cyanated NDIs, respectively. It was found that the electron mobilities were dependent on T_d and dielectric surface treatment. Although the electron mobilities of these compounds were not high enough for practical application, this research implies that on the way to search new high performance n-type semiconductors, it is necessary to find a good balance between the materials' stability

and device stability by careful control of the electron affinity.

In order to find out the optimized condition for the materials processing, device processing - crystal morphology - device performances relationship were investigated using large disc-like ovalene diimides based n-type semiconductor material. The large disc-like molecule ovalene was firstly used as a building block for the design of n-type semiconductors. The C_2-symmetry ovalene diimide (ODI) and the dicyano-ovalene diimide (ODI-CN) were prepared for the first time from bisanthene building block. Due to attachment of electron-withdrawing imide and cyano groups, ODI-CN exhibited stable n-type transistor behavior. After process optimization, high electron mobilities up to 0.51 cm^2/Vs in air and 1.0 cm^2/Vs in N_2 condition were achieved in solution processing OFET devices. The device also displayed good air stability. A possible explanation is that dense solid state packing enhances the device stability. Moreover, the device performance from ODI-CN is better than that from most solution processible n-type semiconductors reported so far. It is believed that the charge carrier mobilities could be further improved when combined with film alignment techniques.

Although the process engineering have achieved much progress for these semiconductors, the charge carrier mobilities of these compounds still lag behind the single crystal device due to poor thin film orientation. In order to further increase the transistor performance, thin film alignment technique was applied using slot die coating. Solvent ratio, substrate temperature and coating speed were proved crucial to

the final crystal morphology and thin film uniformity. POM and AFM images showed that millimeter-sized and highly oriented crystalline domains were achieved at proper coating conditions. Polarized UV-Vis proved that crystal anisotropy exists in the thin film and the value is about 2.5 (at 588 nm). XRD results gave a good explanation that the single crystal growth direction is along the π-π stacking direction. Finally, an average saturation regime mobility of 1.8 $cm^2V^{-1}s^{-1}$ has been achieved in the ambient condition for TIPS-pentacene thin film devices. Moreover, the single crystalline devices showed good operational stability and bias stress stability, which is desirable for practical applications.

Later on, to prove the feasibility of this method, slot die coated technique was also applied to the polymer system. The crystalline polymer thin film could be better tuned by the solution shearing force, and high-performance slot die coated devices were achieved with hole mobilities up to 7.0 $cm^2V^{-1}s^{-1}$ in air condition and 8.9 $cm^2V^{-1}s^{-1}$ in N_2 atmosphere. Meanwhile, low voltage devices using native grown AlO_x modified with octadecylphosphonic acid self-assembled monolayer were succssfully fabricated and exhibited charge carrier mobility of 1.0 $cm^2V^{-1}s^{-1}$. This method implied that large area high performance solution processed organic thin film transistors and logic circuits on the plastic substrates could be realized in the future.

Due to the unstable nature of n-type organic semiconductor materials, n-type metal oxides were introduced in chapter 6. ZnO semiconducting thin film and TFT devices through hydrolyzing ZnO precursors with different water content were

conducted. It was found that introducing controlled amount of water molecules, either in the form of water vapor during annealing or as an additive in the ZnO precursor solutions, has enhanced the ZnO thin film quality by improving the yield of polycrystalline ZnO from its hydroxides. However, excessive amount of water molecules in the ZnO precursor were undesirable due to the formation of acceptor-like traps in ZnO thin film, leading to lower TFT mobility, greater V_T shift and hysteresis voltage, thus degrading TFT performances. In addition, this study has also found that the water vapor or the optimal amount of crystalline water promoted ZnO hydrolysis at low temperature (as low as 150 ^oC) and resulted in desirable performances of the ZnO thin film transistors. The low temperature processability of the ZnO precursor enables low cost printed and flexible electronics applications.

It is worth to mention that the intrinsic mobility of ZnO is still poor, to further enhance the charge carrier mobilities of the ZnO thin films is desirable. In chapter 7, F and LiF-codoped ZnO thin films have been successfully prepared from aqueous solution at low processing temperature. It was found that F and LiF doping at the appropriate amounts enhanced the oxide film quality and reduced defect sites. The TFTs based on LiF doped ZnO thin films revealed largely improved device performance with average electron mobility up to 8.9 $cm^2V^{-1}s^{-1}$ compared with the mobility of 1.6 $cm^2V^{-1}s^{-1}$ for non-doped ZnO TFTs. Our results suggest that LiF doping can be a useful technique to produce more reliable and low temperature solution-processed oxide semiconductor TFTs.

This thesis has provided valuable insight for designing new n-type air-stable aromatic diimide compounds. Moreover, it extends the previous work on the structure-morphology-property relationships of aromatic diimides compounds, thin film alignment, and metal oxide thin film processing and device applications.

Although these semiconductors showed good device performance and relatively good device stability, however, the device performance is critically related to the device structure and interface engineering. Furthermore, the complex synthesis is not compatible with the large area fabrication process. How to make a balance between materials stability and device stability is difficult to control. It should be pointed out that most of the device processing steps are conducted in the N_2 atmosphere excluding the oxygen and water. However, in the actual production process, all the fabrication steps should be conducted in the ambient conditions to simplify the production process and lower production costs. To achieve this target, it is rational to apply some highly ambient stable materials in these processing engineering methods.

Based on my understanding, the flexible, low-voltage devices in plastic electronics should be an interesting area for future research. Since the wearable devices have become a trend in recent years, to fabricate flexible, low-voltage devices is disable for future optoelectrics. For example, to make flexible devices, some polymer substrates like polyethylene terephthalate (PET), polyethylene naphthalate (PEN), and polyimide (PI) should be used, and some high dielectric constant dielectric like hafnium (IV) oxide (HfO_2), cross-linked poly(4-vinylphenol) (PVP) or

polyvinyl alcohol (PVA) should be used to lower down the operating voltage and energy consumtion. Besides these well-developed fields, the sensor application in biology field should be a new avenue of this field. The OFET device is sensitive to most of chemical environment and environmental parameters; it is promising to apply these devices in the biology field to minitor some important parameter change like PH, pressure, temperature, and etc.