Low-Power High-Data-Rate Transmitter Design for Biomedical Application

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A thesis submitted for the degree of Doctor of Philosophy

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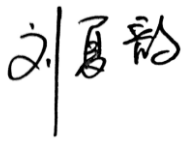
2014

Declaration

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.



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Liu Xiayun

August, 2014

Acknowledgments

At first, I would like to express my deepest thanks and gratitude to my supervisor Prof. Heng Chun-Huat for his advice and instruction with kindness and wisdom on research as well as on personality in the past five years.

Second, my profound thanks must be extended to Dr. Mehran Mohammadi Izad, as his enthusiasm in research greatly encouraged me. Moreover, thanks to the abundant discussions with and advices from him, my horizon has been broadened significantly, both theoretically and experimentally.

Third, my heart-felt thanks also go to my friends Dr. Jun Tan, Dr. Wen-Sin Liew, Dr. Mahmood Khayatzadeh, Mr. Ti Li, Mr. Lei Wang, Mr. Xiaoyang Zhang, Mr. Yongfu Li, Ms. Dingjuan Chua, Mr. Wenfeng Zhao, Mr. Jianming Zhao, Mr. Xuchuan Li, Mr. Rui Pan, Ms. Lianhong Zhou, and Mr. Tong Wu for their kind help on the study itself, as well as understanding and tolerance of my heavy equipment occupancy. Besides, I'd like to thank my friend Dr. San-Jeow Chen, Dr. Yuan Gao for the chance to work with the transmitter project at Institute of Microelectronics (IME).

Thanks for the Economic Development Board (EDB) IC Design Postgraduate Scholarship (ICPS).

Lastly, my forever gratitude goes to my parents and husband for their great love and support.

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Abstract

For implantable and wearable biomedical applications, such as wireless neural recording and capsule endoscopy, there has been an increasing demand for the development of wireless transmitter (TX) with low power consumption and high data rate. In this thesis, two energy-efficient TXs are proposed.

Firstly, a 900-MHz QPSK/16-QAM band-shaped TX will be presented. Unlike the conventional TX, injection locking coupled with quadrature modulation is utilized to achieve band-shaped QPSK/16-QAM modulation with effective sideband suppression of more than 38 dB. Fabricated in 65-nm CMOS, the TX achieves maximum data rate of 50 Mbps/100 Mbps for QPSK/16-QAM with 6% EVM, while occupying only 0.08 mm^2. Under 0.77-V supply, the TX attains energy efficiency of 26 pJ/bit and 13 pJ/bit respectively with and without activating band shaping.

Secondly, a multi-channel reconfigurable 401~406 MHz GMSK/PSK/QAM TX with band shaping is realized in 65nm CMOS with an area of 0.4 mm^2. Using DLL-based phase-interpolated synthesizer and injection-locked ring oscillator, the TX attains 1 kHz frequency resolution as well as multi-phase output without the need of phase calibration. Through direct quadrature modulation at digital PA, the TX achieves less than 6% EVM for data rate up to 12.5 Mb/s. The band shaping maximizes the spectral efficiency with ACPR

of -33 dB. Consuming 2.57 mW, the TX attains an energy efficiency of 103 pJ/bit.

List of Symbols and Abbreviations

ACPR	Adjacent Channel Power Ratio
AM	Amplitude Modulation
BFSK	Binary Frequency-Shift Keying
BS	Band Shaping
BW	Bandwidth
CSD	Canonical Signed Digit
DAC	Digital-to-Analog Converter
DLL	Delay-Locked Loop
DPA	Digital Power Amplifier
ΔΣM	Delta Sigma Modulator
ECG	Electrocardiography
EEG	Electroencephalography
EMG	Electromyography
EVM	Error Vector Magnitude
FCC	Federal Communications Commission
FIR	Finite Impulse Response
FM	Frequency Modulation
GFSK	Gaussian Frequency-Shift keying

GI	Gastrointestinal
ICD	Implantable Cardioverter-defibrillators
ILO	Injection-Locking LC Oscillator
ILRO	Injection-Locking Ring Oscillator
LO	Local Oscillator
ISI	Inter-Symbol Interference
ISM	Industrial, Scientific, and Medical
MedRadio	Medical Device Radio Communications Service
MEMS	Microelectromechanical System
MICS	Medical Implant Communication Service
MSps	Mega Symbol per Second
MUX	Multiplexer
OOK	On-Off Keying
O-QPSK	Offset Quadrature Phase-Shift Keying
PA	Power Amplifier
PIDI	Phase-Interpolated Dual-Injection
PLL	Phase-Locked Loop
PM	Phase Modulation
QAM	Quadrature Amplitude Modulation
QFN	Quad Flat No Lead

QPSK	Quadrature Phase-Shift Keying
π /4-DQPSK	π/4-Shifted Differential Quadrature Phase-Shift Keying
RC	Raised Cosine
RF	Radio Frequency
RO	Ring Oscillator
ROM	Read Only Memory
RRC	Root Raised Cosine
SAR	Successive Approximation
TX	Transmitter
WBAN	Wireless Body Area Network
WLAN	Wireless Local Area Network

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CHAPTER 1
INTRODUCTION

1.1 Background

Wireless technology has provided great mobility and comfort for people in a variety of fields such as cellular telephones, wireless local area network (WLAN) (i.e. Wi-Fi, Bluetooth), GPS units and mobile satellite service technology used in South Pole, and so on.

In the biomedical area, implantable and wearable medical devices for measuring physiological signals, e.g. electrocardiography (ECG), electroencephalography (EEG), electromyography (EMG), and neural signal, also benefit from the rapid growth of wireless technology. Conventionally, inductive telemetry is used for these devices. Despite of the low power consumption, external and implantable devices of these near-field systems must be closely placed in order to construct the required inductive link. This greatly restricts the mobility of both patients and doctors. Therefore, far-field

radio frequency (RF) telemetry is proposed to enhance the device communication range and thus improve the mobility. Zarlink [1] envisages the future of medical operation, as illustrated in Fig. 1.1, where the RF telemetry removes the attachment on body surface that limits mobility.

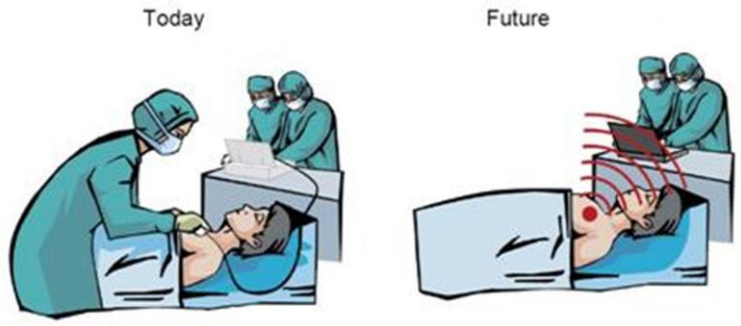


Fig. 1.1. RF telemetry benefits: operating room.

RF telemetry is widely adopted in biomedical area. A typical example is the wireless implantable multi-channel neural recording system. Simultaneous neural signal recording is very useful in studying complex neural basis behavior for the understanding of brain function. One of the potential usages is to replace the function of an impaired nervous system with artificial devices for human body. As shown in Fig. 1.2, neural signal collected through arrays of miniature in-vivo MEMS electrodes will be digitized and transmitted to an external computer for further classification and processing. As perceived in this example, the major constraints of the implantable system are the form factor and total power consumption of the implantable device.

Wireless capsule endoscopy is another interesting application of the RF telemetry. The wireless endoscopy system shown in Fig. 1.3 [1] was designed by Given Imaging incorporated with Zarlink Semiconductor. After being swallowed by the patient, the capsule passes through the digestive tract,

meanwhile the RF transmitter (TX) relays the camera image to a data recorder attached to the SensorBelt around the patient's waist which then download the data to a handheld device that enable real-time gastrointestinal (GI) tract. This capsule endoscopy can reveal the pathologies and diseases of small intestine that were otherwise undetectable using traditional diagnostic tools.

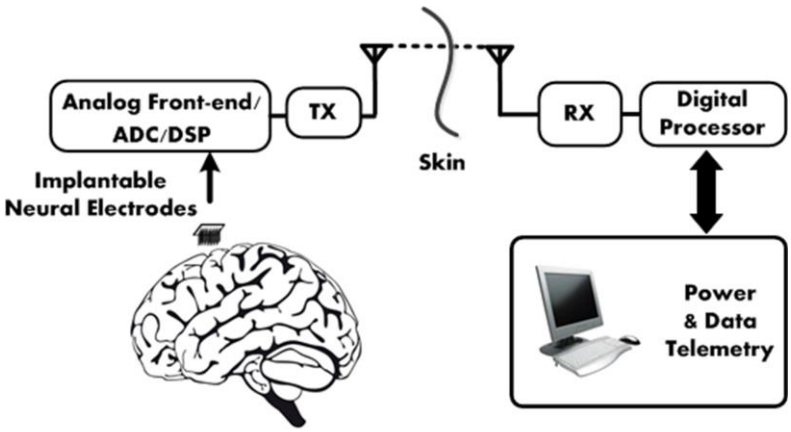


Fig. 1.2. RF TX for a multichannel neural recording system.

(a) (b)

Fig. 1.3. (a) Diagnostic procedure. (b) Pillcam by Given Imaging.

Apart from the above two examples, a wearable wireless body area network (WBAN) also emerges as a key technology for medical and consumer electronics, especially for healthcare monitoring [2]. Equipped with various sensors, the patient can be monitored remotely by doctor from time to time without the need of having the patient visiting the clinic or hospital. The doctor can easily analyze the patient vital condition based on the acquired vital signals, e.g. ECG, EEG, EMG, blood pressure, body temperature, etc.

1.2 Research Objective

Although wireless communication systems have been well developed in the cellular and WLAN domain, these technologies cannot be used directly for medical application such as WBAN. Since the TX architectures in cellular and WLAN devices are usually optimized for high performance and long distance communication, they are too complicated to achieve a small device size and the strictly regulated emission power level of medical applications. Therefore, the design and development of energy-efficient RF TX for biomedical applications is a real challenge.

The first challenge is power consumption. As RF telemetry usually consumes more power than inductive telemetry, high power consumption implies higher system cost, weight, and form factor, mainly due to the need of larger power capacity. Example on low-power devices with small form factor can be found in pacemaker, implantable cardioverter defibrillator (ICD), and long-range long-duration untethered animal tracking system. In short, battery-life time of the implanted device must be extended, and the transceiver needs to be

optimized under limited energy capacity, while maintaining acceptable performance.

Besides the low power consumption, there is an increasing demand for high data rate. For example, in the neural recording system, a huge amount of data needs to be transmitted out of the body to be further analyzed. Normally, simultaneous recording of the brain function requires more than 100 channels. The desired raw data rate can be estimated as follow [3] :

$$DR = CH \times f_s \times B \tag{1.1}$$

where DR is the required data rate, CH is the channel number, f_s refers to the sampling frequency, and B is the bit resolution per sample. If a maximum of 128 simultaneous recording channels are used in this system and each channel is sampled at 40 kS/s with 8-bit resolution, the raw data rate will exceed 40 Mbps. Clearly, as the number of channels increases, precise recording calls for high data rate as much as 100 Mbps or higher. Similarly, in the endoscopy system, for real-time high-quality image (typically 640×480 pixels) transmission with frame rate of 10fps (16 bit color per pixel), the required data rate is as high as 50 Mbps. In the future, if the frame rate of biomedical images is upgraded to the currently main frame rate standard (24 fps), which is identical to TV and movie-making, even higher data rate will be required.

The main objective of this work is to develop a wireless TX with optimized energy efficiency for biomedical application. Firstly, a novel architecture will be proposed to save power and cost. Secondly, to enable high data rate transmission, advanced modulation scheme such as 16-quadrature amplitude modulation (16-QAM) will be utilized in the TX. Thirdly, to lower the adjacent channel interference and maximize the spectrum efficiency, the TX

side-lobe will be suppressed. Lastly, the TX will be designed to support multiple channels.

1.3 Research Contribution

The main contributions of my research works lie in the design of low-power high-data-rate TX dedicated for biomedical applications.

The first contribution of my works is the design of a 13-pJ/bit 900 MHz QPSK/16-QAM band-shaped TX. The novelty of this work is that the injection locking oscillator coupled with quadrature modulation digital PA offers a very efficient way to achieve band-shaped QPSK/16-QAM modulation with effective sideband suppression of more than 38 dB, thus leads to significantly area and power savings. The TX maximum data rate is 50 Mbps/100 Mbps for QPSK/16-QAM with 6% EVM while occupying only 0.08mm^2 active area in a standard 65-nm CMOS technology. Under 0.77-V supply, the TX achieves energy efficiency of 26 pJ/bit and 13 pJ/bit respectively with and without activating band shaping. This TX mainly aims for high data rate applications such as neural recording system and capsule endoscopy.

The second contribution of my work is the design of a 401~406 MHz GMSK/PSK/QAM TX with band shaping in a 65-nm CMOS with 0.4 mm^2 active area. With the usage of a DLL-based phase interpolated synthesizer and an injection-locked ring oscillator, the TX attains 1 kHz frequency resolution as well as multi-phase output without the need of phase calibration. Through direct quadrature modulation at a digital PA, the TX achieves less than 6%

EVM for data rate up to 12.5 Mb/s. The band shaping maximizes the spectral efficiency with ACPR of -33 dB. Consuming 2.57 mW, the TX attains an energy efficiency of 103 pJ/bit. The TX targets the WBAN with specified MICS frequency band.

The publications achieved to date are listed below:

[1] Xiayun Liu, Mehran M. Izad, Libin Yao, and Chun-Huat Heng, “A 13pJ/bit 900MHz QPSK/16-QAM Band Shaped Transmitter Based on Injection Locking and Digital PA for Biomedical Applications,” IEEE J. Solid-State Circuits, vol. 49, no. 11, pp. 2408-2421, Nov. 2014.

[2] Xiayun Liu, Mehran M. Izad, Libin Yao, and Chun-Huat Heng. "A 13-pJ/bit 900-MHz QPSK/16-QAM transmitter with band shaping for biomedical application," In Proc. IEEE Asian Solid State Circuits Conf. (A-SSCC), 2013, pp. 189-192.

[3] Xiayun Liu, Yuan Gao, Wei-Da Toh, San-Jeow Cheng, Minkyu Je and Chun-Huat Heng, "A 103 pJ/bit Multi-channel Reconfigurable GMSK/PSK/16-QAM Transmitter with Band-shaping," In Proc. IEEE Asian Solid State Circuits Conf. (A-SSCC), accepted.

1.4 Organization of the Thesis

This thesis is organized as follows:

Chapter 2 reviews the conventional TX architecture with various modulation schemes and pulse-shaping filters.

Chapter 3 presents the proposed 900 MHz QPSK/16-QAM band-shaped TX, including the detailed descriptions and circuit implementation for each of the functional blocks. The chip verification and measurement results will also be presented.

Chapter 4 proposes a multi-channel 401~406 MHz GMSK/PSK/16-QAM band-shaped TX, accompanied by chip verification and measurement results.

Chapter 5 summarizes and concludes this thesis.

CHAPTER 2
EXISTING TX DESIGNS FOR BIOMEDICAL APPLICATION

2.1 Transmitter Architecture

2.1.1 Mixer-Based TX

Although two-step architecture is widely used in today's communication system since it can circumvent the problem of local oscillator (LO) pulling with superior I/Q mismatch[4], direct-conversion architecture is usually adopted in low-power systems for biomedical application [3, 5-26], due to its simplicity and high level of integration.

Fig. 2.1 shows the architecture of a conventional direct up-conversion transmitter. This quadrature upconverter topology is suitable for both linear and nonlinear modulation. As illustrated in the figure, the baseband data will

first go through the digital-to-analog convertors (DACs) and reconstruction low-pass filters. The resulting I/Q signals will be up-converted by phase-locked loop (PLL) based mixers. They are then summed together and sent to the power amplifier (PA) and matching network for transmission.

This architecture suffers from a few drawbacks if it is used in a low power implementation for biomedical application. Firstly, in order to avoid over heating of the body tissue, the required output power of the PA for is generally low. Therefore, the carrier generation block (such as PLL) normally dominates the power dissipation and dictates the transmitter efficiency. The requirements for phase noise and frequency calibration also limit the power consumption for PLL [27]. Secondly, the long PLL settling time prohibits the duty cycling of data transmission which is widely adopted in biomedical application so that the TX can be powered down to conserve energy. Thirdly, large device size is required to overcome I/Q path mismatch and offset, and thus does not favor biomedical implementation targeting small form factor. Finally, high speed DACs and wide-band filters required for high data rate are usually achieved at the expense of higher power dissipation.

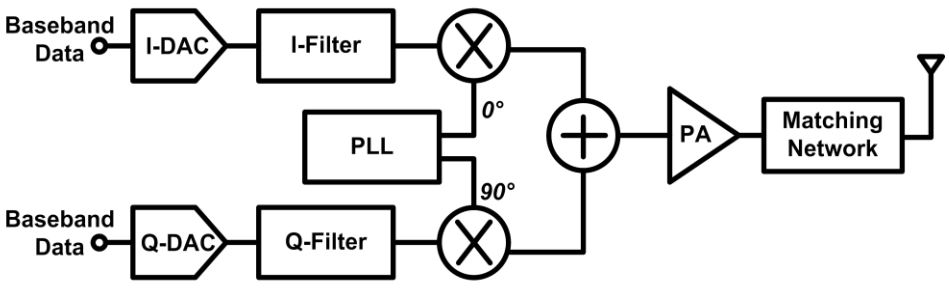


Fig. 2.1. Conventional mixer based TX.

2.1.2 Polar TX

Another popular architecture is polar TX, as shown in Fig. 2.2. I/Q data are converted into magnitude and phase components through the Cartesian-to-polar coordinate transformation. Fractional-N PLL and supply modulated PA are employed to achieve both amplitude modulation (AM) and phase modulation (PM). Several works [28-31] have described the benefits of the polar TX over the conventional Cartesian counterparts based on I/Q upconversion. Improved efficiency is achieved through the polar architecture since the TX can adopt a nonlinear but highly-efficient PA for the AM path. However, this architecture requires wideband PM and unequal delay compensation between the PM and the AM paths. Also, its architectural complexity does not favor low-power implementation either.

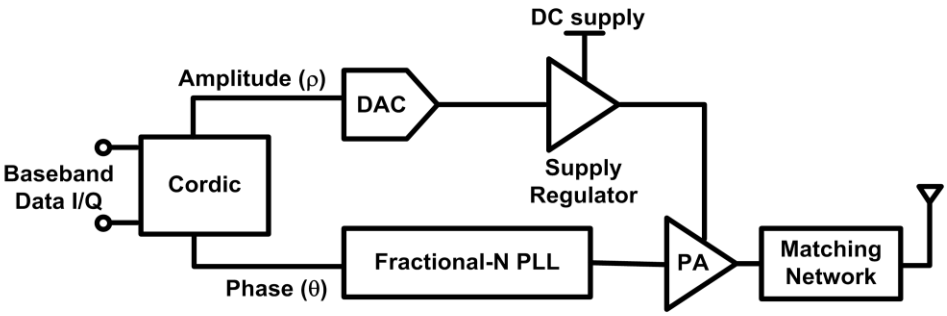


Fig. 2.2. Conventional polar TX.

2.1.3 MUX-based TX

To circumvent the power hungry problems for mixer-based TX, in [3, 17], a phase multiplexer (MUX) is employed to select the quadrature phases generated from the frequency synthesizer. As shown in Fig. 2.3, the

quadrature mixers in the conventional transmitter are replaced by the phase MUX. This architecture eliminates the usage of power-hungry high-speed DACs and wide BW analog filters while realizing offset quadrature phase-shift keying (O-QPSK) modulation. Although it offers a better alternative to accomplish low power consumption and high data rate, the use of multi-phase PLL still prevents a further reduction of power consumption. Additionally, long PLL start-up time also limits its duty-cycling capability.

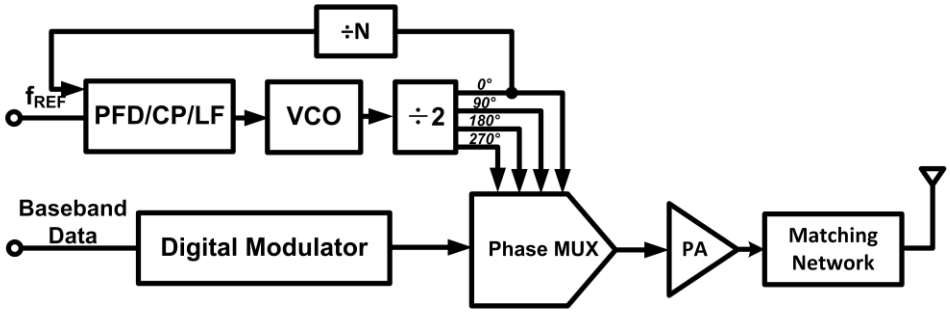


Fig. 2.3 A MUX-based TX.

2.1.4 ILO based TX

Early in the 17th century, the Dutch scientist Christiaan Huygens observed the pendulums of two clocks synchronize with each other when they are placed close enough. Since then, injection of a periodic signal into an oscillator which leads to interesting locking or pulling phenomena has been studied in various works [32-35]. Injection-locking oscillator (ILO) is commonly used in frequency division, quadrature generation [36] and low phase noise application[35]. The basic principle of injection locking can be simply described as, if a sinusoidal current, I_{inj}, with proper amplitude and frequency is injected into an oscillator, the oscillator will oscillate at ω_{inj} instead of its

free-running frequency, ω_0, within a certain frequency range. Depending on the ratio of the injected frequency and oscillator frequency, injection-locking oscillators can be categorized into three types: first-harmonic ($\omega_{inj} = \omega_0$), super-harmonic ($\omega_{inj} > \omega_0$) and sub-harmonic ($\omega_{inj} < \omega_0$) injection locking.

Recently, sub-harmonic ILO based TX [20, 37-39] has gained popularity in the implementation of low power transmitter system. The sub-harmonic locking phenomenon mathematically behaves like a first order integer-N PLL. However, unlike an actual PLL, it does not require phase detector, charge pump, loop filter and divider. It should be pointed out that frequency divider operating at the same frequency as the VCO could be power hungry. In addition, a ring oscillator (RO) based PLL normally requires high power RO to achieve a reasonably good phase noise performance [27] . Hence, the PLL alone could result in tens of mW power consumption [40-42]. By replacing power hungry PLL with ILO, this architecture shows greater promise with low power consumption and high energy efficiency for biomedical application.

Ref [14] further developed the ILO based TX from simple OOK and FSK modulation into QPSK/O-QPSK modulation in order to achieve tens of Mbps data rate. The PSK modulation is achieved by directly modifying the free-running frequency of an LC oscillator since there will always be phase shift when $\omega_{inj} \neq \omega_0$. However, the calibration of the switched capacitor bank for reasonable error vector magnitude (EVM) is non-trivial and requires significant design overhead. Furthermore, the use of LC oscillators in both works at sub-GHz range also incurs significant area penalty.

On the other hand, a recently-published 8PSK TX [24] has revealed an energy-efficient injection-locking ring oscillator (ILRO) based architecture for

phase modulation and shown promising performance for biomedical application. Therefore, ILRO is adopted in this work. It is chosen as the main frequency generation for three reasons. Firstly, it offers a promising solution to achieve low power dissipation and low phase noise. The poor phase noise performance of a typical RO is improved as the ILRO phase noise characteristic tends to follow its injected reference [20, 24]. Secondly, fast settling time for ILRO allows the TX to operate in the form of "sniffing" or "wake up". This is also desirable for low-data rate application, where the data is buffered and transmitted at the highest possible data rate for a short interval to reduce the average current consumption and the time window to avoid interference [43]. Thirdly, a RO readily provides the multi-phase output required for both PSK and QAM modulation without the need of additional power hungry frequency divider.

2.2 Modulation Scheme

Modulation schemes can be classified into three categories: frequency modulation (FM), amplitude modulation (AM), and phase modulation (PM). For TX design, the choice of modulation scheme dictates the design specifications for each building block, such as power amplifier linearity and receiver complexity. Different modulation schemes exhibit trade-offs among bandwidth efficiency, power efficiency, and etc.

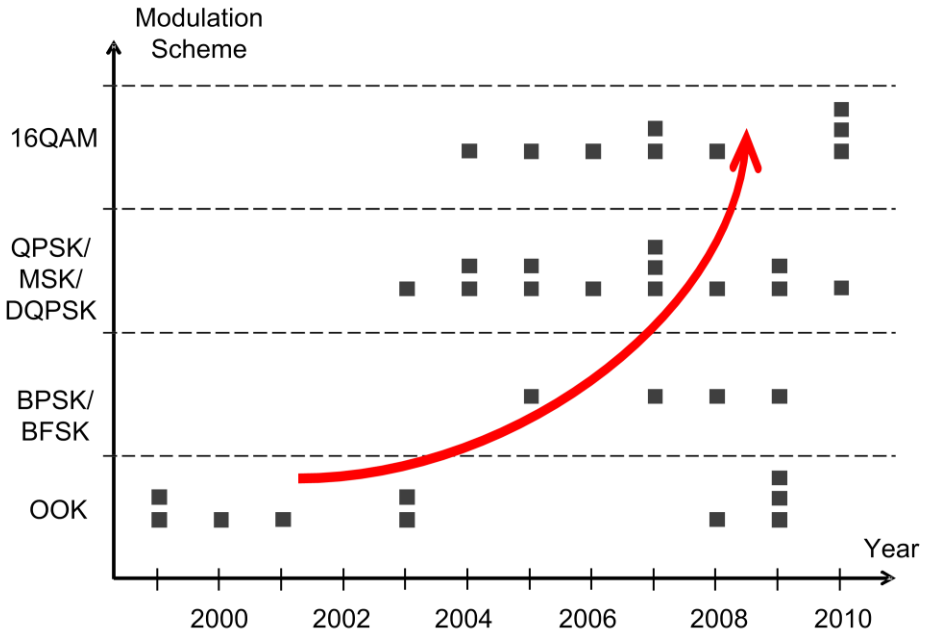


Fig. 2.4. Modulation trend for TX above 60 GHz.

In the area of cellular communication, modulation schemes evolved from analog modulation (first generation, 1G) to digital modulation (second generation, 2G) [44]. From 2G to 4G, besides the improvement in multiplexing systems, improved digital modulation schemes from earlier standard PSK to more efficient system such as 64-QAM are being proposed. Similar trend can be observed for TX above 60 GHz, as shown in Fig. 2.4. More complex modulation has been adopted over the time span from 1999 to 2010.

Meanwhile, in the biomedical area, simple modulation scheme remains the popular choice. Many RF TXs adopt OOK or FSK [10-13, 20, 45] due to the more power efficient non-linear PA adopted by these modulation schemes. In return, poor spectral efficiency is observed for these modulation schemes.

Recently, for neural recording and capsule endoscopy which require high data-rate uplink, PSK has emerged as a promising candidate capable of transmission with twice the bandwidth energy efficiency as compared to OOK and BFSK [3, 8, 14, 17, 23, 24, 46]. Moreover, due to the relatively low output power and supply voltage level for implantable devices, this choice will not lead to significant degradation in PA efficiency.

In this works, more advanced modulation scheme, such as QAM, is explored in order to achieve higher data rate with higher spectral efficiency than PSK. As shown in Fig. 2.5, at the same date rate, 16-QAM occupied smaller bandwidth compared to BFSK, BPSK, QPSK, and 8-PSK, with spectral efficiency equal to 4. Equivalently, this translates to higher data rate under identical bandwidth compared to other modulations.

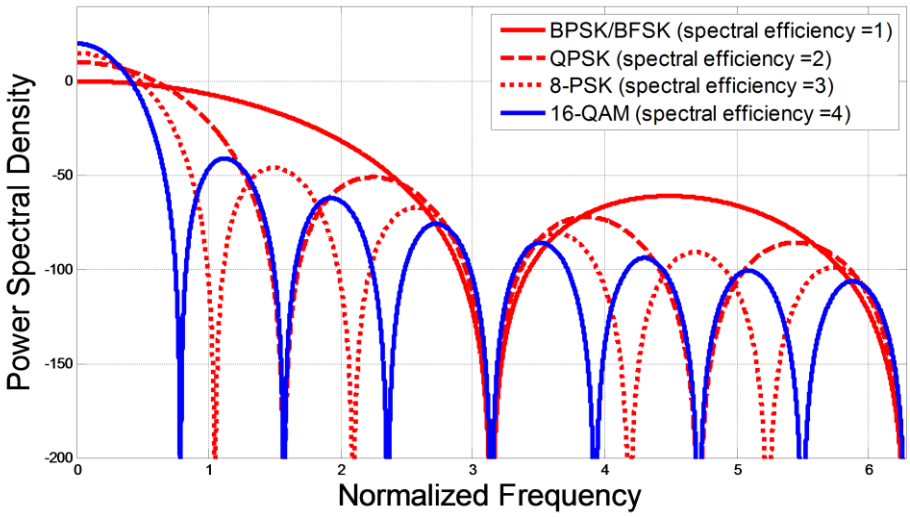


Fig. 2.5. Comparison of occupied bandwidth for different modulation schemes at the same data rate.

2.3 Pulse-Shaping Filter

Rectangular pulses are not suitable for transmitting data because of the large bandwidth requirement. Thus, pulse-shaping filter is generally used to reduce the transmission bandwidth while preserving the important data information. The most commonly used pulse-shaping filter is raised cosine (RC) filter. An ideal raised cosine filter is a low-pass Nyquist filter with zero impulse response at the intervals of $\pm T_{S,}$ as shown in Fig. 2.6. This helps eliminate the inter-symbol interference (ISI). Conventionally, a raised cosine filter is split into two root-raised cosine (RRC) filters.

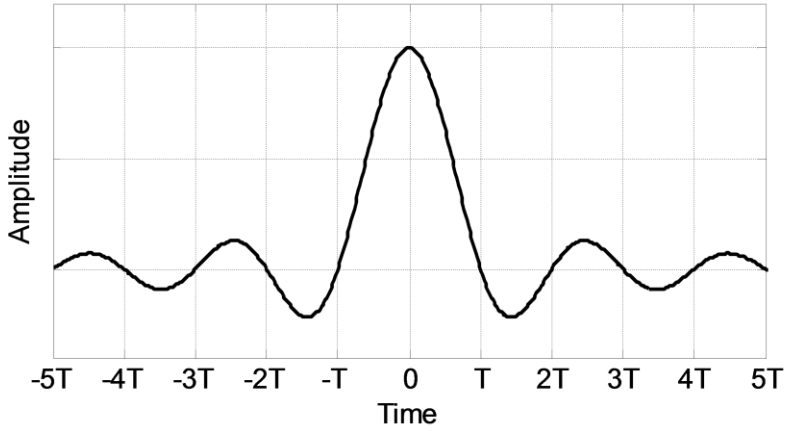


Fig. 2.6. Impulse response of the RC filter.

The red curve shown in Fig. 2.7 illustrates the output spectrum of the recently proposed QPSK/8-PSK TX systems [3, 14, 24]. To reduce power consumption, most of them do not attempt pulse-shaping filter. As illustrated, the resulted spectrum exhibits first side lobe as high as -15dB below the main lobe, which is detrimental for multi-channel transmission and adjacent channel interference. If the RRC filter is adopted, the adjacent channel interference

will be much lower, as shown by the blue curve in Fig. 2.7, which is beneficial for multi-channel transmission.

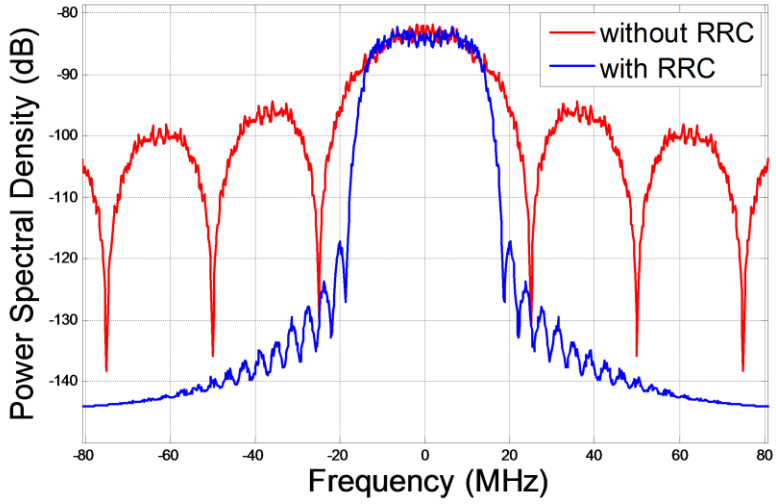


Fig. 2.7. Output spectrum of the recent proposed QPSK TX without RRC vs TX with RRC.

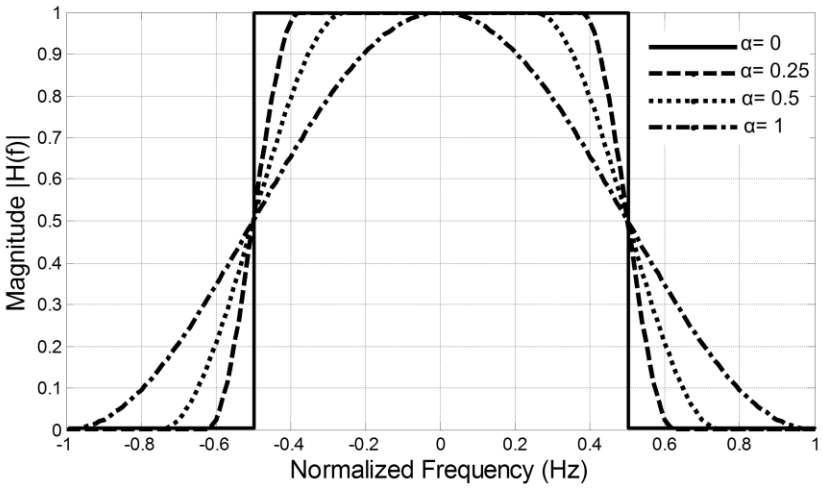


Fig. 2.8. Occupied bandwidth of RC filter with different α.

As shown in Fig. 2.8, the occupied bandwidth of the RC filter is determined by the roll-off factor as follows [44]:

$$BW = Symbol\ Rate \cdot (1 + \alpha) \tag{2.1}$$

Typical value of α ranges from 0.2 to 0.5. Although a smaller α indicates smaller bandwidth, it increases the duration of filter impulse response and also increases receiver complexity in order to ensure high accuracy of sample time placement as compared to a lager α. For both works presented in this thesis, α=0.4 is adopted.

2.4 Summary

Conventional transmitter architectures including mixer-based TXs and polar-based TXs are not suitable for low power biomedical applications because of higher system complexity, while the injection locking oscillator based TX is becoming a promising candidate. On the other hand, spectral efficiency is a major concern for high data-rate uplink. To enable maximum spectral efficiency, more advanced modulation scheme (i.e. QAM) as well as the pulse shaping filter should be incorporated into the TX system.

CHAPTER 3
DESIGN OF QPSK/16-QAM TRANSMITTER WITH BAND SHAPING

3.1 Introduction

In this chapter, injection locking architecture coupled with direct quadrature modulation at PA is proposed to achieve both phase and amplitude modulations in an energy efficient manner. The resulting TX can provide both QPSK and 16-QAM with band shaping (BS). Compared to QPSK and 8-PSK, 16-QAM improves the bandwidth efficiency by 100% and 33% respectively for a given data rate. At the same time, the TX also suppresses the side lobe by 38 dB. Thanks to the simplicity of the proposed TX, energy efficiency of 26 pJ/bit can be achieved with BS. By deactivating BS, the energy efficiency can be lowered by half to 13 pJ/bit. The architecture is digitally intensive and can benefit from future technology node scaling.

The rest of the chapter is arranged as follows. Section 3.2 illustrates the proposed TX architecture, while Section 3.3 discusses the CMOS implementation for each block. Section 3.4 shows the experimental results and the comparison between this work and other TX works. Section 3.5 concludes this chapter.

3.2 Transmitter Architecture

As discussed in Chapter 2, an oscillator locks to the N^{th} harmonic of an injected signal if the free-running frequency of the oscillator is close to that harmonic. This sub-harmonic locking phenomenon causes the oscillator output frequency to become N times the injection signal frequency. Therefore, it can provide a compact, low-power and low-noise solution for frequency synthesis with extremely fast transient response [47, 48].

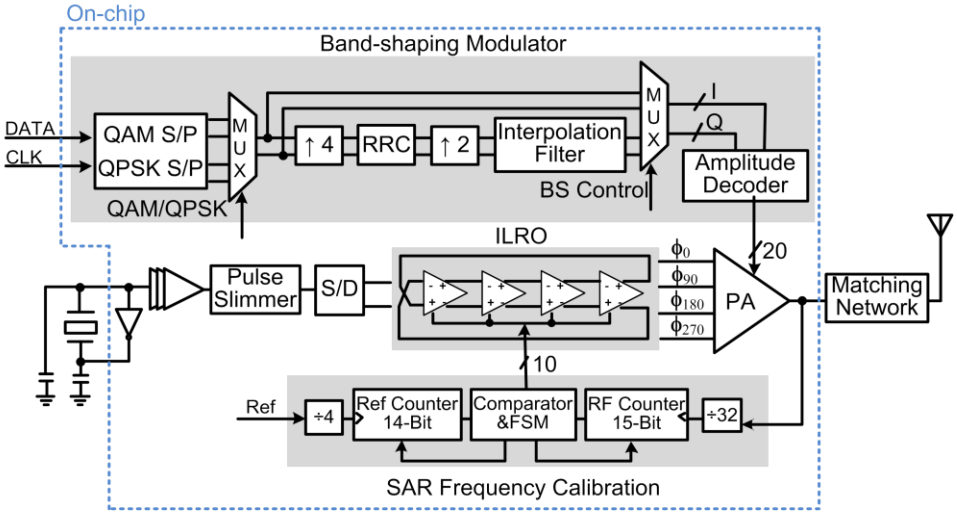
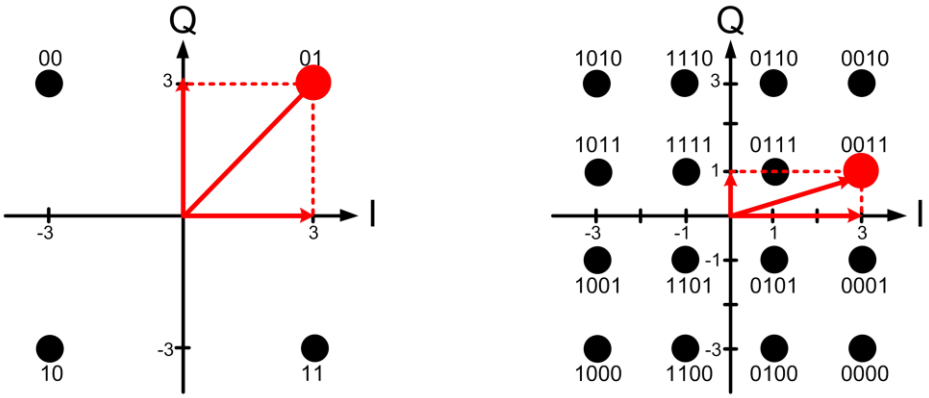


Fig. 3.1. Proposed TX architecture.

The proposed TX architecture is shown in Fig. 3.1. In this architecture,

injected reference of 100 MHz is chosen to go through the pulse slimmer and single to differential block, and injected into a ring oscillator with free-running frequency around 900 MHz, so that the ring oscillator will lock to the 9th harmonic of the injected reference. The injection-locked ring oscillator (ILRO) forms the core of TX which provides 4-phase output (ϕ_0, ϕ_{90}, ϕ_{180}, ϕ_{270}) with good phase noise.



(a) (b)

Fig. 3.2. Constellation of (a) QPSK (b) 16-QAM.

Direct quadrature modulation at PA is proposed here to provide both phase and amplitude modulations. The underlying principle being a carrier with arbitrary amplitude and phase components can always be split into in-phase and quadrature-phase components with corresponding amplitudes. As an example, to synthesize 0011 in the 16-QAM constellation plot shown in Fig. 3.2(b), in-phase (ϕ_0) component with amplitude of 3 and quadrature-phase (ϕ_{90}) component with amplitude of 1 can be combined, and so is the QPSK demonstrated in Fig. 3.2(a). The concept can be easily extended to enable BS by providing multiple amplitude level for the 4-phase outputs. This will enable

the fine phase and amplitude tuning required for BS. Unlike conventional quadrature modulation in Fig. 2.1, high power RF blocks, such as mixers, PLL, etc., are eliminated. Compared to polar modulation in Fig. 2.2, sophisticated fractional-N synthesizer is not required for phase modulation thanks to the direct quadrature modulation concept at PA which only requires 4 phases. Hence, the proposed injection-locked oscillator coupled with direct quadrature modulation would result in very energy efficient TX. In addition, the proposed TX is also highly digital intensive as shown in Fig. 3.1, which would benefit from future technology scaling.

3.3 Design Consideration

The performance of the transmitter is characterized by EVM and spectrum of its transmitting signal. This in turns depends on the quality of the band shaping and generated carrier (e.g., phase noise, phase and frequency accuracy). This section examines the design considerations of the carrier generation and pulse shaping of baseband data.

3.3.1 EVM Consideration

For the QPSK and the 16-QAM in this design, each constellation point is obtained by combining two quadrature components with different amplitudes. Thus the ideal modulated output and the one with phase error and amplitude error can be modeled as the following equations:

$$V_{ideal} = V_1 \cos(\omega t) + V_2 \sin(\omega t) \tag{3.1}$$

$$V_{mout} = V_1(1 + \Delta V_1)\cos(\omega t + \theta_1) + V_2(1 + \Delta V_2)\sin(\omega t + \theta_2) \tag{3.2}$$

where V_1 and V_2 are the desired amplitude for the in-phase and quadrature-phase components, ΔV_1 and ΔV_2, and θ_1 and θ_2 are their corresponding amplitude errors and phase errors. By subtracting (3.1) and (3.2), the resulting amplitude error ΔM_{rms} and phase error θ_{rms} of the modulated signal can be obtained as follows:

$$\Delta M_{rms} \approx \frac{1}{\sqrt{V_1^2 + V_2^2}} \sqrt{V_1^2 V_2^2(\theta_1^2 + \theta_2^2) + V_1^4 \Delta V_1^2 + V_2^4 \Delta V_2^2} \tag{3.3}$$

$$\theta_{rms} \approx \frac{1}{V_1^2 + V_2^2} \sqrt{V_1^2 V_2^2(\Delta V_1^2 + \Delta V_2^2) + V_1^4 \theta_1^2 + V_2^4 \theta_2^2} \tag{3.4}$$

By assuming similar amplitude and phase error in both the in-phase and quadrature-phase components, the EVM can be expressed as [49]:

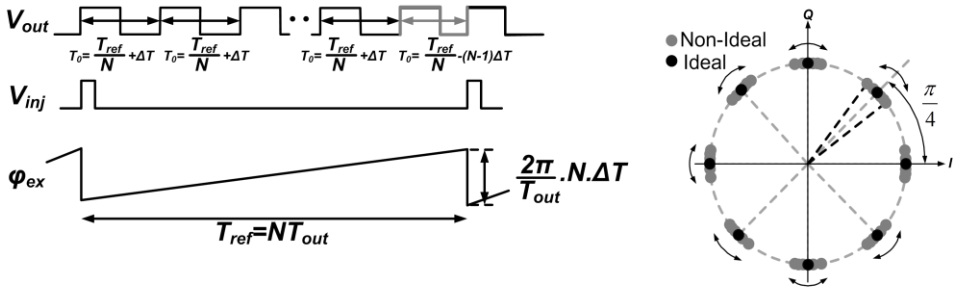
$$\begin{aligned} EVM &\approx \sqrt{\left(\frac{\Delta M_{rms}}{OI}\right)^2 + (\sin\theta_{rms})^2} \times 100\% \\ &\approx \sqrt{\left(\frac{\Delta M_{rms}}{\sqrt{V_1^2 + V_2^2}}\right)_{rms}^2 + (\theta_{rms})^2} \times 100\% \end{aligned} \tag{3.5}$$

Where OI is the ideal amplitude equals to $\sqrt{V_1^2 + V_2^2}$. Hence, to achieve a given EVM, ΔM_{rms} and θ_{rms} can be determined accordingly with (3.5). This will in turns translate to the desired amplitude and phase errors. As phase error depends on both the systematic and random phase error, we can then work out the individual requirement such as the phase noise, the random phase mismatch and the systematic phase error. The phase noise and random phase

mismatch will determine the crystal phase noise requirement and the delay cell sizing requirement. On the other hand, based on the systematic phase error as described later, the desired frequency resolution can be estimated. The amplitude errors will determine the mismatch requirement for the PA unit amplifier.

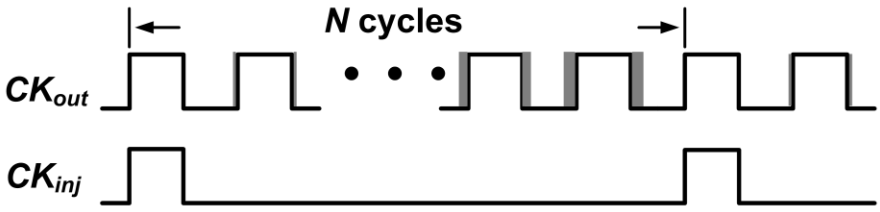
A. Systematic Phase Error

The locking mechanism in RO based on the current starved inverters has been illustrated in [50]. Here, we only examine the phase error caused by the frequency deviation between the injection signal and the free-running frequency in the ILRO. For sub-harmonic injection, the injection signal will only correct the oscillator frequency in the first output cycle of the RO. For the next N-1 cycles, there is no injection signal and the RO will oscillate at its free-running frequency. As shown in Fig. 3.3(a), $\varphi_{ex}(t)$ is a saw-tooth waveform caused by the periodic correction if Nth harmonic of the injected signal is close to free-running frequency.

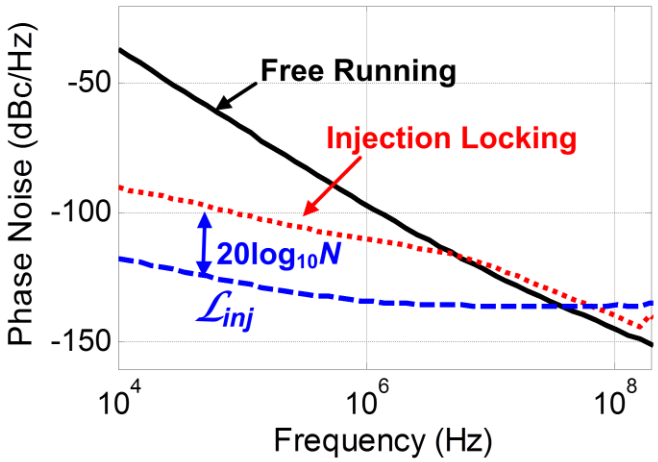


(a) (b)

Fig. 3.3 (a) Behavior of the sub-harmonic injection-locked oscillator when $f_0 \neq N.f_{ref}$. (b) Effect of phase modulation on the constellation.



(a)



(b)

Fig. 3.4. Effect of injection locking on oscillator in (a) Time domain perspective. (b) Frequency domain perspective from simulation.

The periodic correction can be considered as phase modulation (PM) as illustrated in Fig. 3.3(b). The RMS phase error can be calculated as follows [24]:

$$\theta_{error,rms} = \sqrt{\frac{1}{T_{ref}} \int_{T_{ref}} (\varphi_{ex}(t))^2 dt} = \frac{2\pi}{T_{out}} \cdot \frac{N.\Delta T}{\sqrt{3}} = \frac{2\pi.N.\Delta f}{\sqrt{3} f_0} \tag{3.6}$$

where $\Delta T = T_0 - \frac{T_{ref}}{N} = \frac{1}{f_0} - \frac{1}{f_{out}}$ and $\Delta f = N f_{ref} - f_0$. In the frequency domain, the periodic correction causes spurs. The spur level can be calculated as follows [51]:

$$Spur\ (dBc) \approx 20 \log\ (N \cdot \frac{|f_{out} - f_o|}{f_{out}}) \tag{3.7}$$

Hence, a successive approximation (SAR) frequency calibration algorithm has been incorporated on-chip to fine-tune the RO free-running frequency to match the 9th harmonics of injected reference. The measured spur level can indicate the resulted frequency deviation.

B. Random Phase Error

The performance of the TX is also affected by two sources of random phase error. The first is phase noise. In the time domain, jitter of a free-running oscillator accumulates over time. If the ILRO is an Nth sub-harmonic injection, the injection locking corrects the zero crossing of the oscillator every N oscillator period, thereby resetting the accumulation of jitter as shown in Fig. 3.4(a). Ref [35] pointed that the phase noise within the locking range would be constrained to $\mathcal{L}_{inj}$+20log$N$, where $\mathcal{L}_{inj}$ is the phase noise of the sub-harmonic injection signal. In order to verify it, phase noise of the RO with and without injection locking is simulated in Cadence. As shown in Fig. 3.4(b), the RO phase noise can be significantly improved, which corroborate the theory.

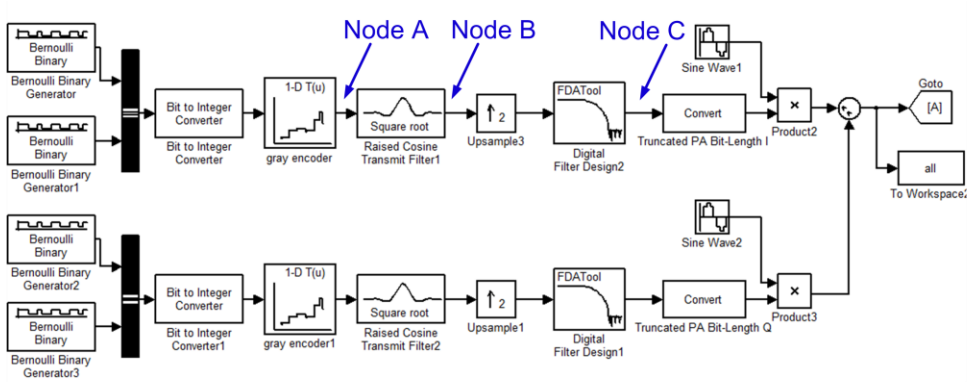
Another source of random phase error is the random mismatch between delay cells. Each stage provides a mean phase step of $\pi/4$(delay of $T/8$) with a standard deviation of σ_θ. This mismatch manifests itself as a distortion of the constellation according to (3.5). In this work, this mismatch is minimized by properly sizing the delay cells and a circuit technique which will be discussed in the next section.

3.3.2 Spectrum Consideration

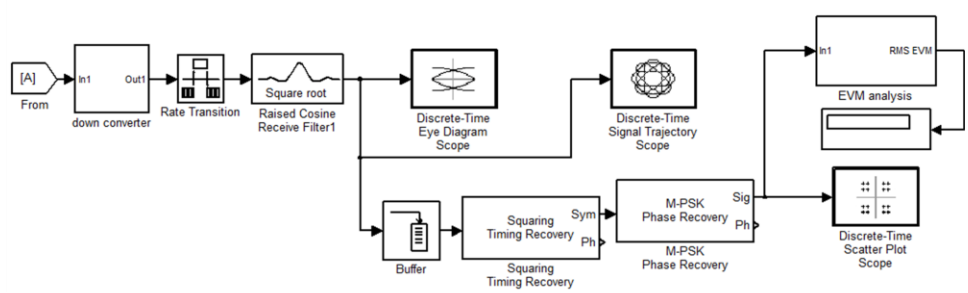
To achieve the desired modulation and BS, the incoming serial data is first converted into parallel I/Q data depending on the desired modulation (2 bits/symbol for QPSK and 4 bits/symbol for 16-QAM). If BS is activated, I/Q data will then be up-sampled by 4 times before passing through the RRC filter (α=0.4). FIR filters instead of ROM is adopted here for the RRC filter implementation to provide flexibility in filter coefficient tuning. Following that, it is further up-sampled by 2 times before going through an interpolation filter. The up-sampling will push the unwanted image further away from the targeted output. If BS is deactivated, I/Q data will be sent to the decoder directly, bypassing the intermediate up-sampler and RRC filter to conserve energy.

Another way of realizing BS is to up-sample the data by 8 times directly and passes it to the RRC filter. However, this will require higher order RRC filter working at twice the clock frequency. Simulation results show that this method will consume more than twice the power as compared to up-sample by 4+2 times. Therefore the up-sampling is divided into two steps.

To verify the band-shaping function, a MATLAB Simulink model of the proposed 16-QAM TX is constructed for system simulation, as shown in Fig. 3.5(a). RX shown in Fig. 3.5(b) is also built to examine the resulting eye diagram, the trajectory and the EVM. As illustrated, Node A is the original I/Q pulse wave, Node B indicates the output data which is up-sampled by 4 times and followed by RRC filter. Node C shows the data which is further interpolated by 2. The simulated symbol rate is 25 MSps. As can be seen



(a)



(b)

Fig. 3.5. MATLAB Simulink model of (a) proposed TX. (b) RX.

from Fig. 3.6, Node A exhibits high side lobe, similar to Fig. 2.7 without band shaping. Through RRC filter, the side lobes in spectrum of Node B are suppressed, however, the nearest image is visible at 4 × the symbol rate, which is 100 MHz away from the center. After a further up-sampling by 2 times, the nearest image is now moved to 200 MHz away from the center, and can be easily suppressed by the matching network and antenna.

The targeted side lobe suppresion is 38 dB in the system design. As shown in Fig. 3.5, the baseband modulator output needs to be truncated before sending to the PA to avoid overdesign. Three parameters are being considered in the system simulation to decide the digital PA bit-length, PA power consumption, TX EVM performance, and side-lobe suppression. From Fig. 3.7, it has been

determined that the 6-bit signed PA bit-length for I/Q path is sufficient for the desired BS with more than 38 dB side lobe suppression, with acceptable EVM. Therefore, 5-bit amplitude control per phase (0°, 90°, 180°, 270°) is adopted.

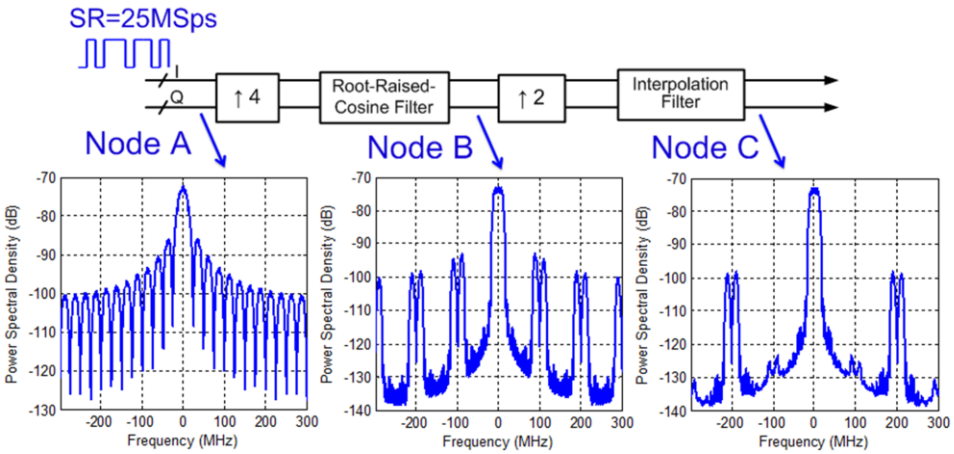


Fig. 3.6. Output spectrum of (a) Node A (b) Node B(c) Node C.

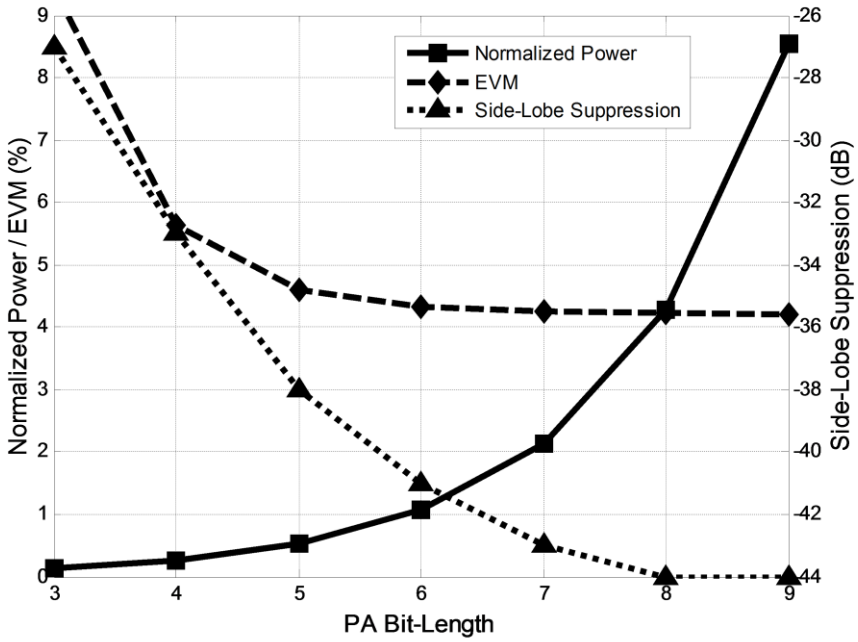


Fig. 3.7. PA bit-length vs. power, EVM, and side-lobe suppression.

3.4 Circuit Implementation

3.4.1 Crystal Oscillator

A crystal circuit is built on-chip to better evaluate the phase noise and energy efficiency performance of the TX. An off-chip 100MHz fundamental mode crystal from Micro Crystal Switzerland is adopted. Fig. 3.8 illustrates the standard RLC circuit model for the crystal simulation. Given that R_S = 15 Ω, C_S = 4.6 fF, C_P = 2.3 Pf, ω_S =100 MHz, the calculated L_S using the following equation is about 550.65 μH.

$$L_S\omega_S = \frac{1}{C_S\omega_S} \tag{3.8}$$

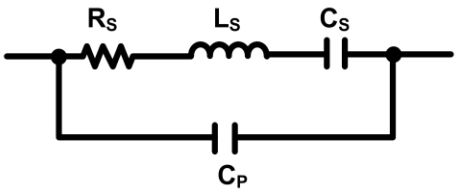


Fig. 3.8. LC model for crystal.

Fig. 3.9 displays the schematic of the Pierce crystal oscillator circuit which is popular for its low power dissipation [52, 53]. The transistor M_6, two capacitors C_1, C_2 and the bias resistor R_1 provide the negative transconductance to overcome the resonator losses. The circuit is followed by a common source amplifier to amplify the output amplitude.

Fig. 3.10 shows the simulated magnitude and phase response of the crystal oscillator. To ensure the oscillator starts oscillating, loop gain is designed be larger than 1 at the oscillation frequency.

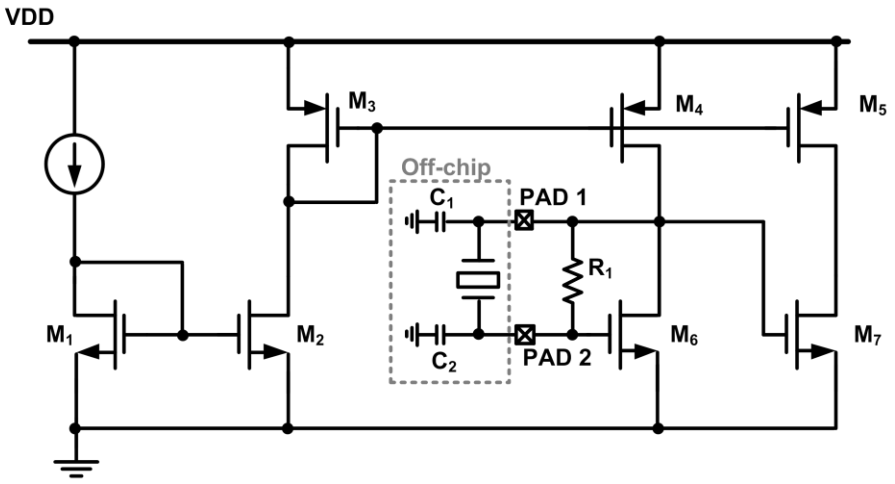
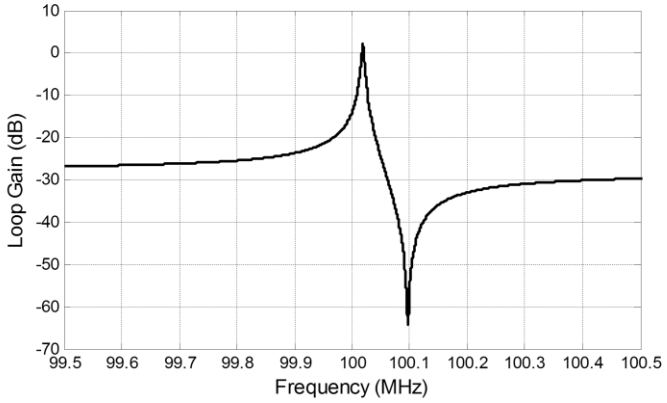
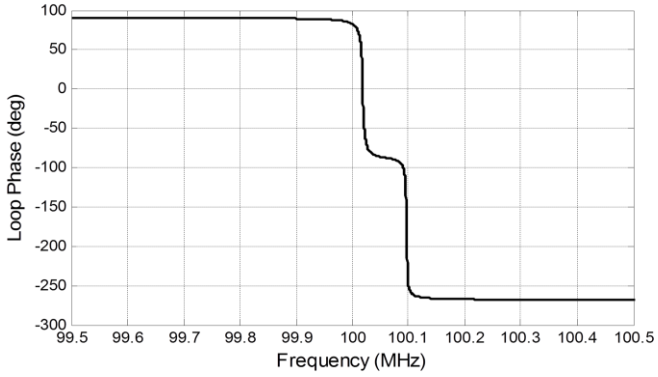


Fig. 3.9. Schematic of the Pierce crystal schematic.



(a)



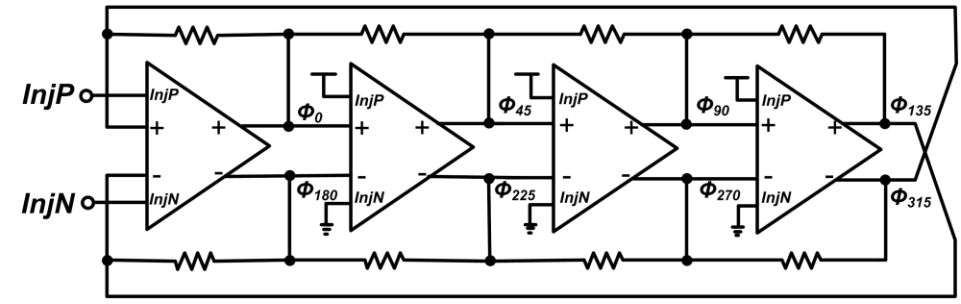
(b)

Fig. 3.10 (a) Magnitude and (b) phase response of the crystal oscillator.

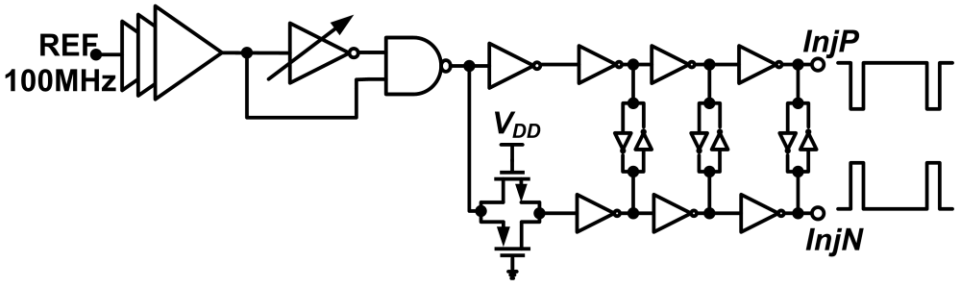
3.4.2 Injection-Locked Ring Oscillator

Similar to [24], ILRO is adopted to provide energy efficient multi-phase oscillator output with good phase noise. Instead of 8 phases in [24], only 4 phases are required for QPSK and 16-QAM quadrature modulation. A four-stage pseudo-differential ring oscillator is shown in Fig. 3.11(a). The pulse slimmer shown in Fig. 3.11(b) ensures that the width of the injection pulse is less than half of the RO period. It generates the injected pulse for ring oscillator first, and then the differential pulse is injected through M_7 and M_{15}, as can be seen in Fig. 3.11(c). M_8-M_{10} and M_{11}-M_{13} are the dummy devices in order to balance the loading of the differential paths. Since the total number of inversions in the loop is even, the circuit is easy to latch up. To avoid this issue, four pairs of cross coupling inverters are introduced in the ring oscillator, shown in Fig. 3.11(c). The size of the cross coupling inverters need to be carefully chosen so that the RO can start oscillation from any initial condition. In this design, the size of the cross coupling inverter is 1/10 of the main inverter stage (M_1-M_4). A 10-bit binary-weighted array is used to digitally control the ring oscillator frequency to cover the desired operation frequency range across PVT. Based on the previous analysis, by designing the frequency resolution to be less than 0.2 MHz in the worst case, it will result in a systematic phase error of less than 0.4°.

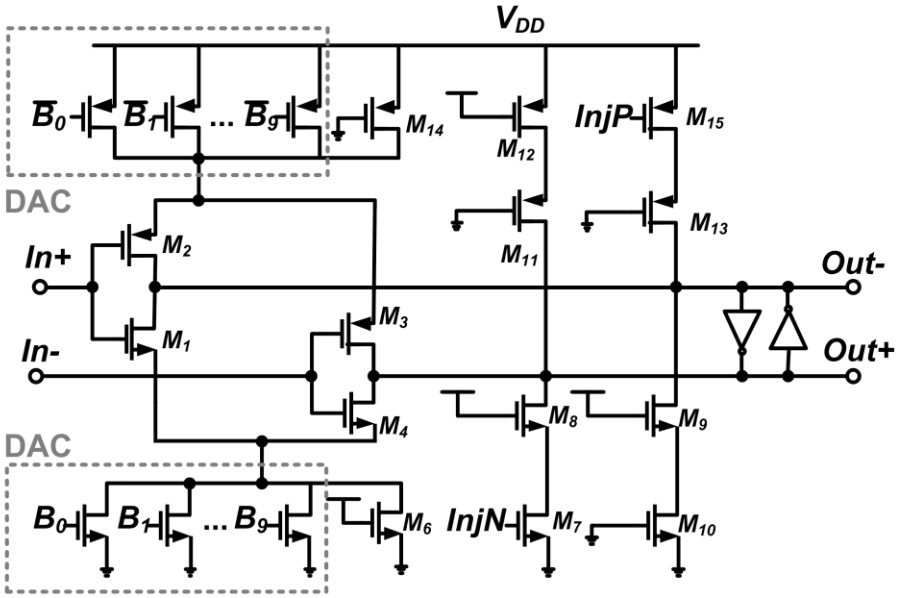
The phase mismatch of the RO due to the delay cell mismatch will affect the EVM performance directly, as mentioned in the previous Section 3.3.1. Although a larger delay cell with better matching can be adopted, it will result in higher power consumption. Multiphase injection can also improve the matching. However, an additional ring oscillator is needed, which



(a)



(b)



(c)

Fig. 3.11. (a) Implementation of ILRO (b) Pulse slimmer (c) Detailed schematic of the delay cell.

increases the power consumption. Thus, a mismatch filtering technique [54] is employed here to improve the output phase matching while achieving better matching without significant power penalty.

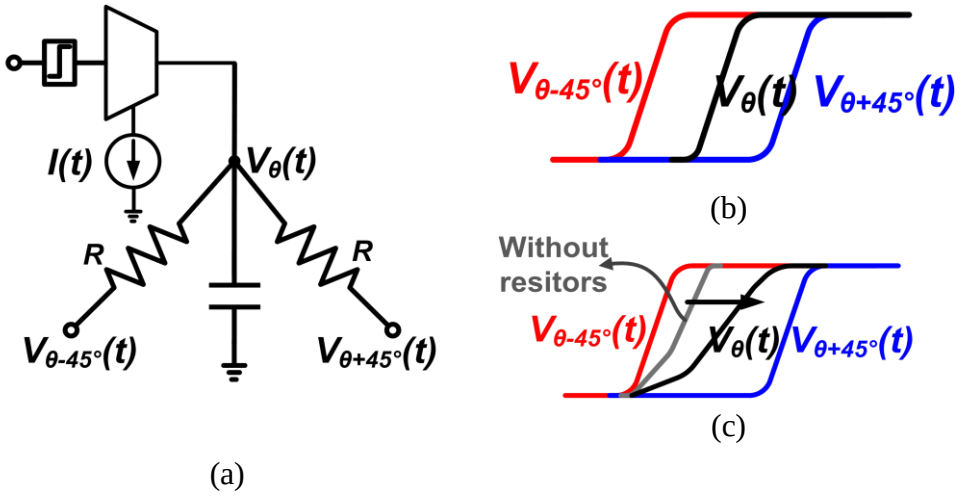


Fig. 3.12. Effect of mismatch filtering resistors. (a) Simplified model. (b) Waveforms in the ideal case and the presence of mismatch.

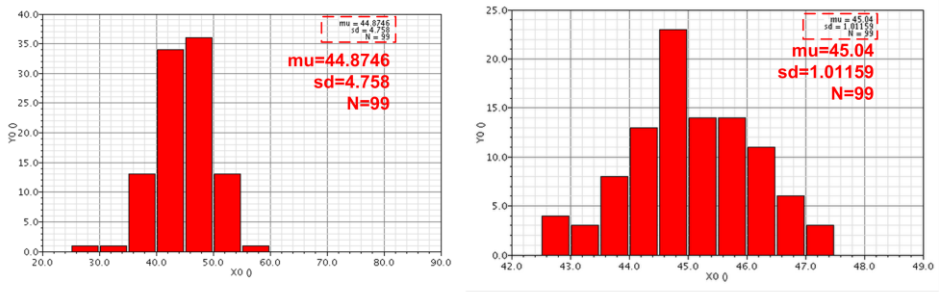
Shown as Fig. 3.12, each stage output phase node is coupled to the two neighboring phase nodes so that the current phase will not wander too far away from the designed position. The net current, $I_{net}(t)$ can be derived as follows [54]:

$$I_{net}(t) = I(t) + \frac{\frac{V_{\theta-45^\circ}(t) + V_{\theta+45^\circ}(t)}{2} - V_\theta(t)}{R/2} \tag{3.9}$$

Where

$$V_\theta(t) = \int I_{net}(t) \cdot \frac{1}{C} \cdot dt \tag{3.10}$$

According to (3.9) and (3.10), smaller R will result in better phase mismatch. However, smaller resistor will also introduce more *4kT/R* noise to the RO. In this design, R value is chosen to be 9 kΩ so that the noise it incurs is negligible to the RO phase noise. According to the Monte Carlo simulation shown in Fig. 3.13, the phase mismatch improves from 4.8° to 1° after adopting the mismatch filtering technique.



(a) (b)

Fig. 3.13. Monte Carlo simulation for phase mismatch: (a) without resistor network (b) with resistor network.

3.4.3 Power Amplifier

The digital PA with embedded phase multiplexer and amplitude control is shown in Fig. 3.14. It consists of 4 amplifier cores driven by 4 output phases (ϕ_0, ϕ_{90}, ϕ_{180}, ϕ_{270}) from ILRO. The bottom transistors are connected to the respective ILRO output phases whereas the top transistors are used to activate the corresponding phase. To achieve 5-bit amplitude control for each output phase, the transistors within each amplifier core are further segmented into an array of 31 transistor pairs. Direct quadrature modulation is achieved through current summing from two activated phase branches with different current amplitude. The combined output current is then sent to an off-chip impedance matching network before driving the 50-Ω antenna. The 20-bit control (5 bit/phase × 4 phases) for the PA is provided from band-shaping modulator. It should be pointed out that this PA differs from the RF DAC. For the RF DAC, all unit amplifiers are driven by the same carrier output and only the amplitude control is achieved. In this circuit, the amplifier cores are driven by RF carrier

with different phases. Hence, both the phase and amplitude controls are achieved in this PA. Based on the previous section, 1% mismatch between each amplifier core are chosen. Combining with the earlier phase errors (excluding the RO phase noise), this will give rise to an EVM of 2.1%.

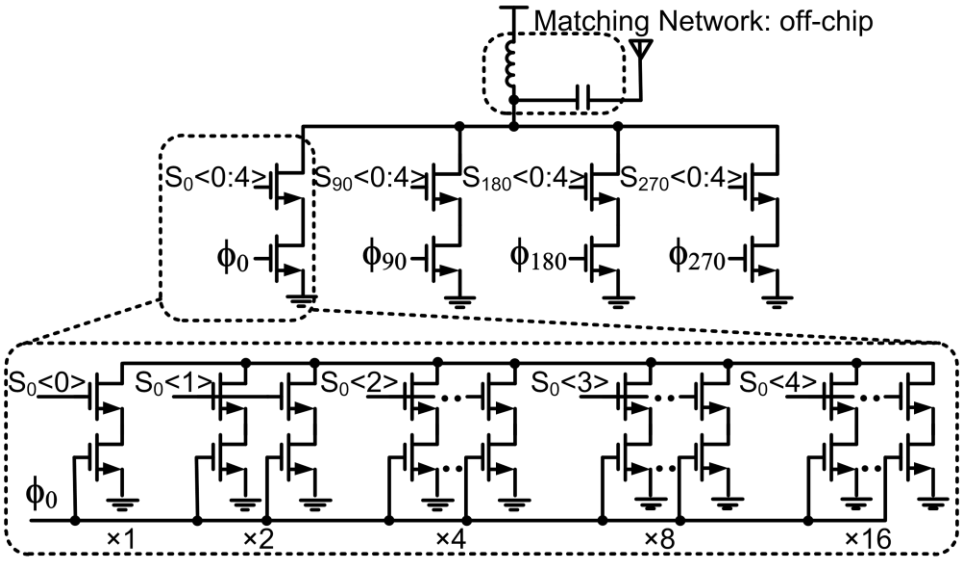
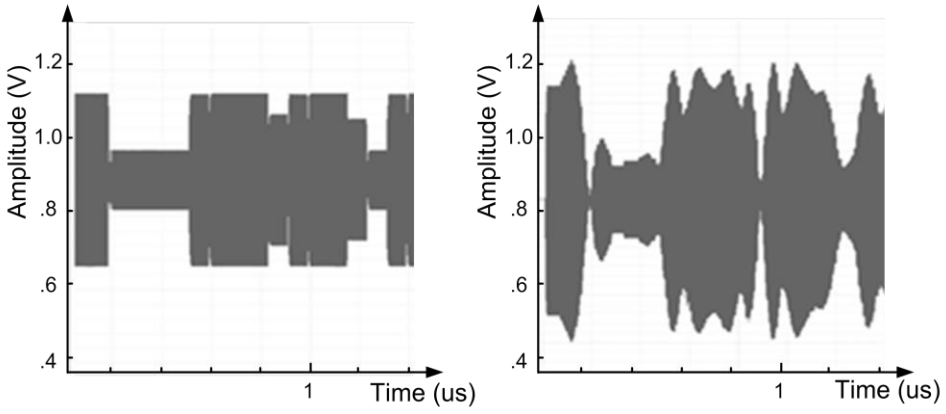


Fig. 3.14. Digital power amplifier with direct phase and amplitude modulation.



(a) (b)

Fig. 3.15. Time-domain waveform of PA output (a) without BS (b) with BS.

Fig. 3.15 shows the time-domain waveform of PA output with band shaping

and without band shaping. Without band shaping, there will be abrupt changes which leads to high side lobe. With band shaping, the phase and amplitude change gradually, thus spectrum in frequency-domain exhibits low side lobe.

One issue that has to be noted is the kick-back noise from the PA to the ILRO. Since the proposed PA directly combine the current of different phases together, the combined output will result in kick-back noise, due to the parasitic capacitances Cgs and Cgd shown in Fig. 3.16, and cause two ILRO phase output to affect one another and reduce the ILRO phase accuracy. Moreover, as the top transistors switch on and off, the capacitance seen at the input gate of the bottom transistors also changes [55]. Therefore buffers have to be inserted between ILRO and PA to circumvent the kick-back issue.

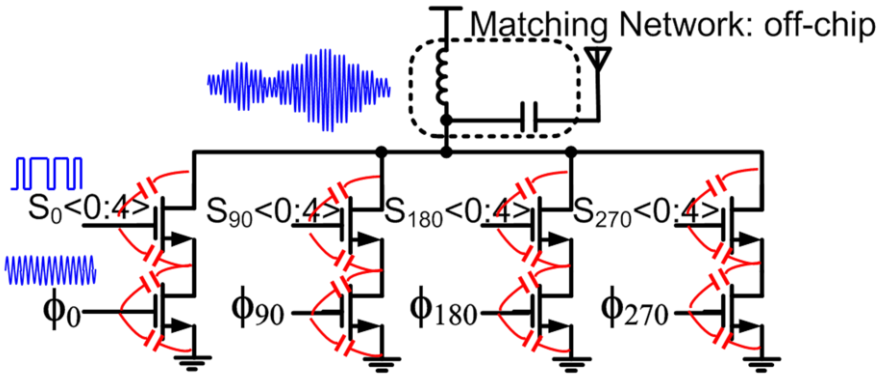
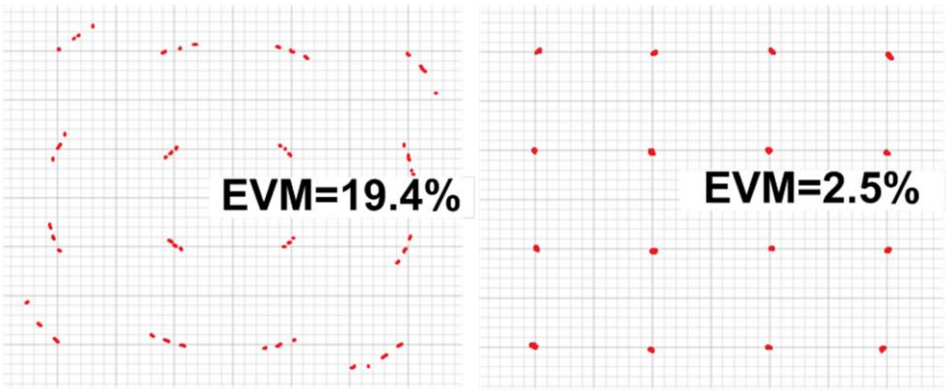


Fig. 3.16. Kick-back noise due to parasitic capacitance.

Fig. 3.17 illustrates the system simulated EVM performance with and without buffer between ILRO and PA. As illustrated, EVM worsen to 19.4% without the buffer as compared to EVM of 2.5% with the buffer.



(a) (b)

Fig. 3.17. Simulated EVM performance of TX (a) with buffer between ILRO and PA (b) without buffer between ILRO and PA.

3.4.4 SAR Frequency Calibration

The SAR frequency calibration as illustrated in Fig. 3.1 is similar to the one in [56]. The divided reference frequency f_{ref}, and RF frequency f_{rf} are counted during a fixed window period, shown in Fig. 3.18.

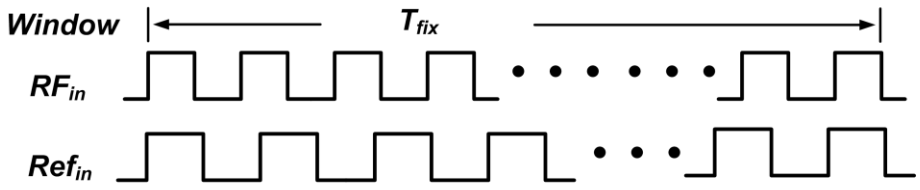


Fig. 3.18. Fixed counter window for frequency calibration.

The window period determines the measurable frequency resolution. The longer the period of T_{fix}, the more accurate the frequency calibration will be. Meanwhile the frequency error of SAR due to the edge uncertainty is shown as follows:

$$Error_{max} = \pm\frac{1}{2}LSB \tag{3.11}$$

Assuming that the accuracy needed for RO is Δf = 0.1 MHz, RF_{in} is divided by M = 32. If the designed error is smaller than the one in (3.11), the calculated window period is shown as follows:

$$T_{fix} \geq \frac{M}{\Delta f} \tag{3.12}$$

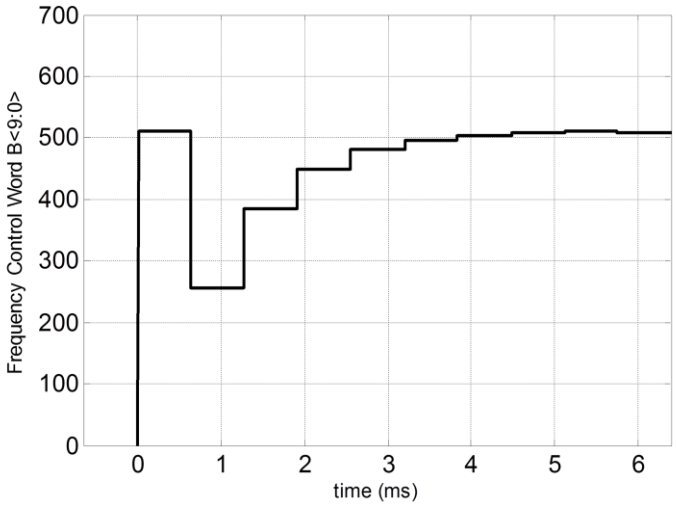


Fig. 3.19. SAR algorithm for frequency tuning.

Therefore, there is a trade-off between the calibration time and the frequency accuracy. The block named “Comparator & FSM” shown in Fig. 3.1 will compare the divided input reference frequency and divided RO free-running frequency through simple counter. The comparison outcome will be used to digitally control the ring oscillator. Fig. 3.19 indicates the SAR algorithm which determines the 10-bit DAC control for RO. This block can be turned off after calibration and the digital implementation enables digital storage of the control words with only leakage power.

3.4.5 FIR Filter Implementation

The direct form transpose finite impulse response (FIR) filter architecture shown in Fig. 3.20 is adopted for RRC filter and interpolation filter due to its simplicity.

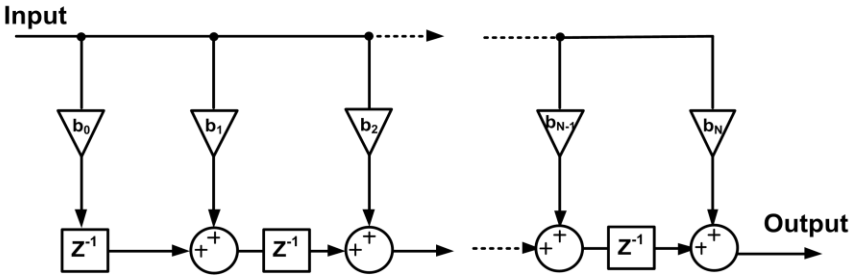


Fig. 3.20. Direct form transposed FIR filter.

The taps of RRC filter are investigated in MATLB. The length of the frequency filter impulse response is given as follows:

$$L = 2 \times N \times Group\ delay + 1 \tag{3.13}$$

where N is the upsampling factor and the *Group delay* is the number of symbol periods between the start of the filter's response and the peak of the filter's response. Then the number of taps is decreased while observing the spectrum and EVM performance. The minimum number of taps is chosen such that no significant deterioration on spectrum and EVM are observed. In this design, N=4 and *Group delay*=3 is chosen for 25 taps RRC filter. Then the number of taps is decreased to 21. Fig. 3.21 shows the impulse response of the designed 21 taps RRC filter.

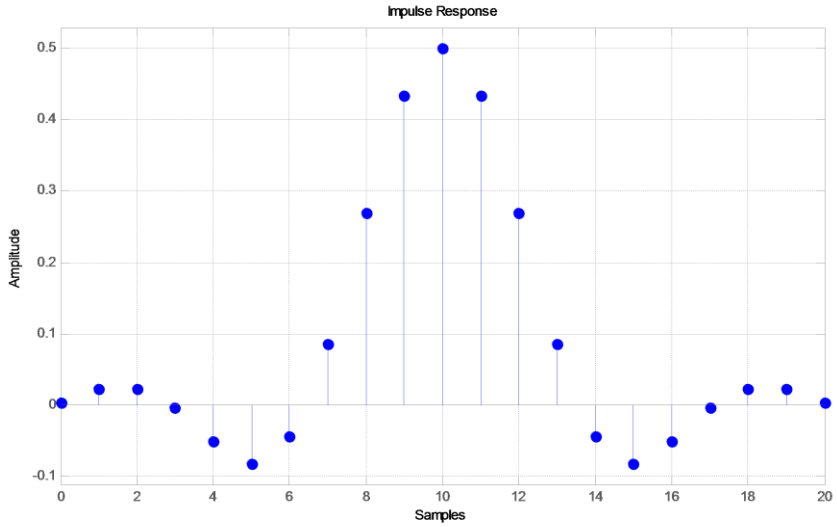


Fig. 3.21. Impulse response of designed RRC filter.

After determining the number of filter taps, the number of bits for filter coefficients is investigated next. As illustrated in Fig. 3.22, the ideal RRC filter with double precision coefficients shown in red curve exhibits low side lobe of up to 50 dB at 40 MHz away. When the coefficients are truncated down to 8 bits, the side lobe suppression is larger than the expected specifications. On the other hand, the simulated EVM only change by 0.5% when the bit-length is decreased from 14 bits to 7 bits. Thus, a RRC filter bit length of 9 bits is chosen in the final design based on side lobe and EVM considerations.

The truncated product bits and accumulator bits are also determined to have minimal impact on the spectrum and EVM. A similar method is employed for the interpolation filter design. The interpolation filter is a half-band low-pass filter for efficient interpolation by a factor of 2. Table 3.1 shows the final bit-length implementation for all filters. It should be noted that all the multipliers constants are represented by canonical signed digit (CSD) owing to

the direct form transpose architecture, thus can be easily realized through shifter and adder which significantly reduce the area and cost of hardware implementation.

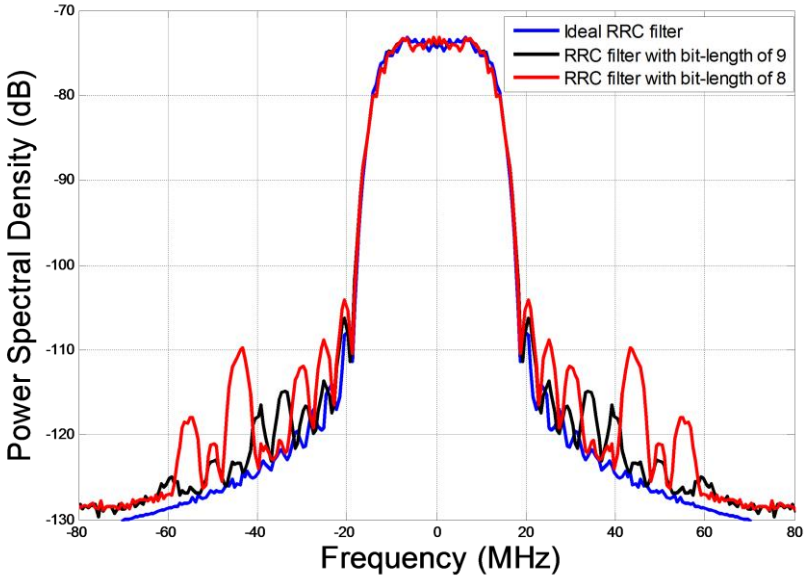


Fig. 3.22. Output spectrum of RRC filter with different coefficient bit-length.

Table 3.1. Digital bits for filter design.

	Taps	Coefficient bit-length	Sum. and Prod. bit-length	Output bit-length
RRC filter	21	9	11	10
Interpolation filter	11	8	12	6

3.5 Chip Verification and Measurement Results

Fig. 3.23 shows the test setup. The TX output is measured using Agilent N9030A PXA spectrum analyzer. Agilent 8133A pulse generator and E3631A

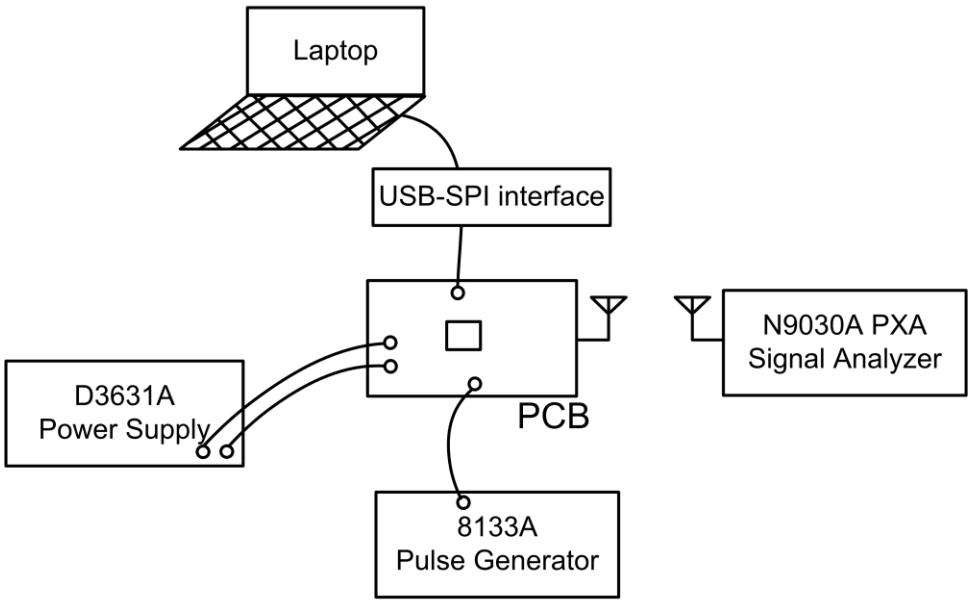


Fig. 3.23. Simple test setup diagram.

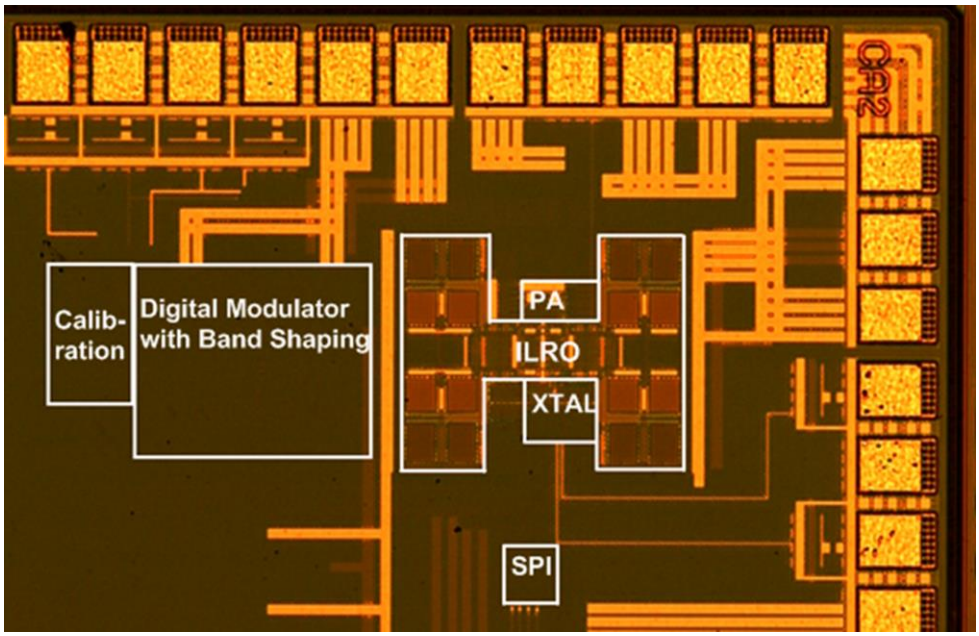


Fig. 3.24. Die photo.

power supply are also used to generate clean clock source and supply. The digital control signals are sent to the chip via freescale USB-SPI interface. The chip is packaged in Quad Flat No lead (QFN) and all the measurements have

been performed on the packaged chips using a socket.

The chip is fabricated in 65-nm CMOS technology. Due to the highly digital nature of the architecture and the absence of area-hungry PLL, the TX only occupies an active area of 0.08 mm^2 as shown in Fig. 3.24. The only off-chip components needed are the matching network and the 100 MHz crystal.

The measured tuning range of RO covers 0.81-1 GHz under 0.77-V supply voltage. The measured locking range of the ILRO is from 885 to 925 MHz. Fig. 3.25 shows the measured phase noise under free running and injection locking. The phase noise at 100 kHz improves by about 40 dB. The ILRO achieves a total integrated RMS jitter of 1.54°. To enable high energy efficiency, the crystal oscillator power consumption is capped at 115 μW. If the crystal oscillator power is increased to 380 μW, a 7-dB improvement at 1 MHz offset in phase noise is noted.

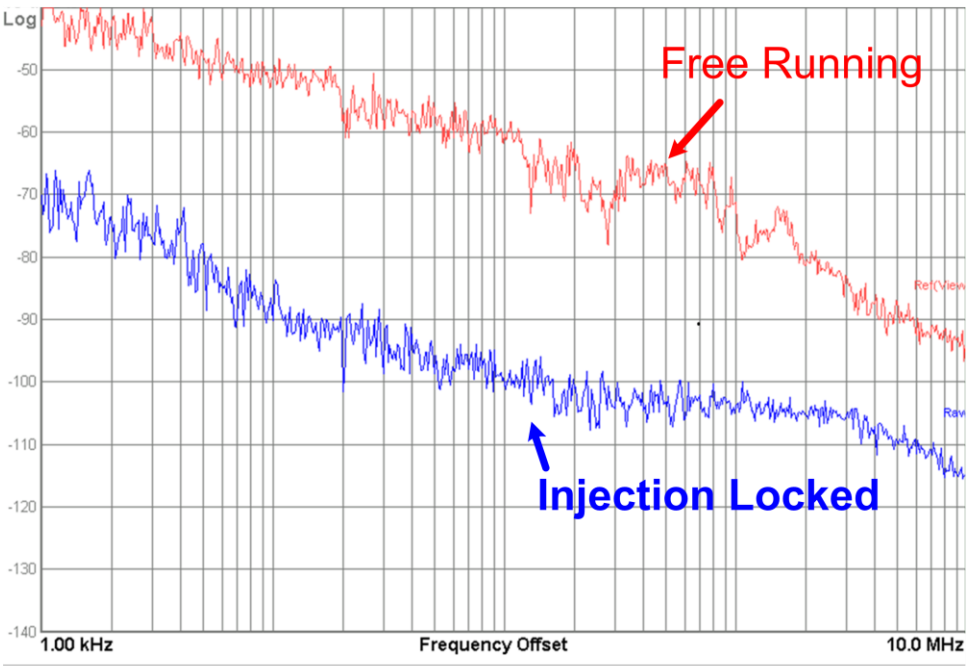


Fig. 3.25. Measured phase noise under free running and injection locking.

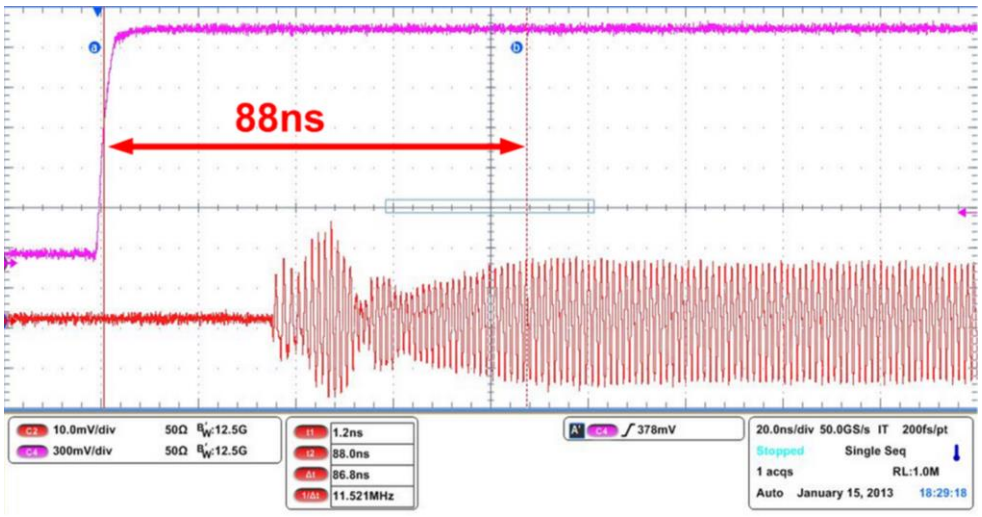


Fig. 3.26 Measured settling time.

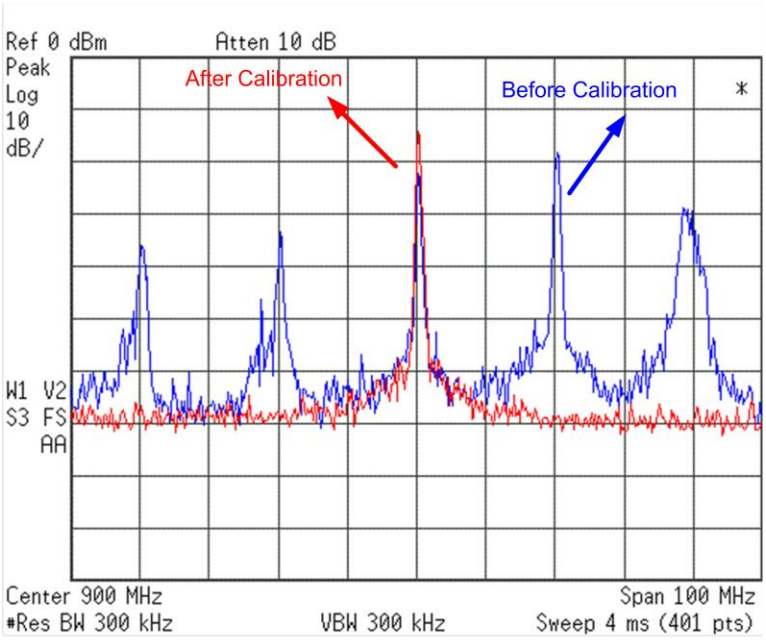


Fig. 3.27. Spectrum of ILRO before and after frequency calibration.

The ILRO also shows a fast start-up time of less than 88 ns as illustrated in Fig. 3.26, which is critical for burst-mode operation to maximize the duty cycling (ratio of sleep mode to active mode) for power savings.

Fig. 3.27 shows the ILRO spectrum before and after frequency calibration. Before the calibration, the free-running frequency is out of locking range and

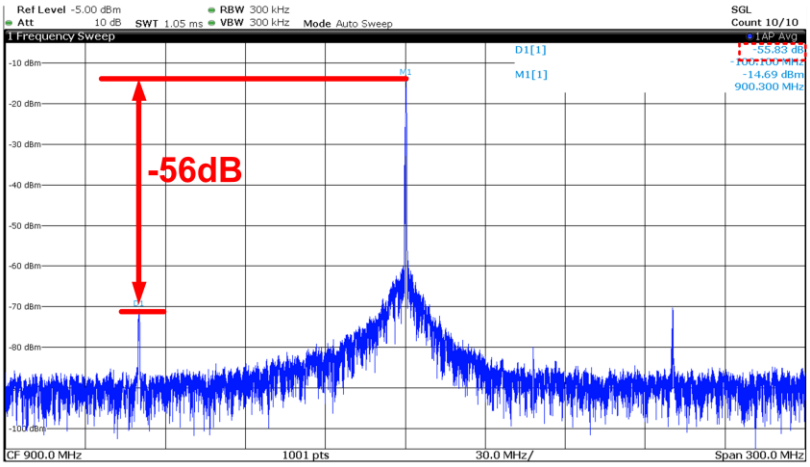


Fig. 3.28. Measured spurious tones performance of ILRO.

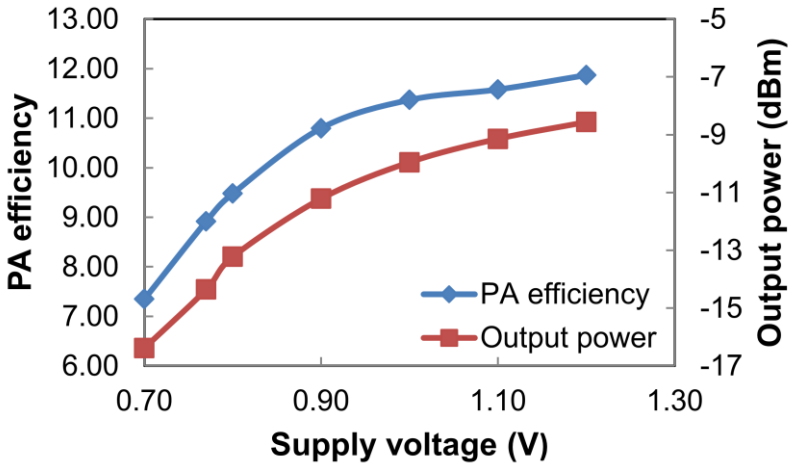


Fig. 3.29. Measured PA efficiency versus supply voltage.

the ring oscillator is under fast beat condition [33]. After frequency calibration, the reference spur of the ILRO can be lowered to -56 dBc as shown in Fig. 3.28.

The PA efficiency is defined as the ratio of the output power to the average DC power consumption of the PA. As can be seen in Fig. 3.29, PA efficiency of 9% is achieved at 0.77-V supply under modulation while delivering -15 dBm output power. When the supply voltage increases to 1.2 V, the PA efficiency is 12% with output power of -9 dBm.

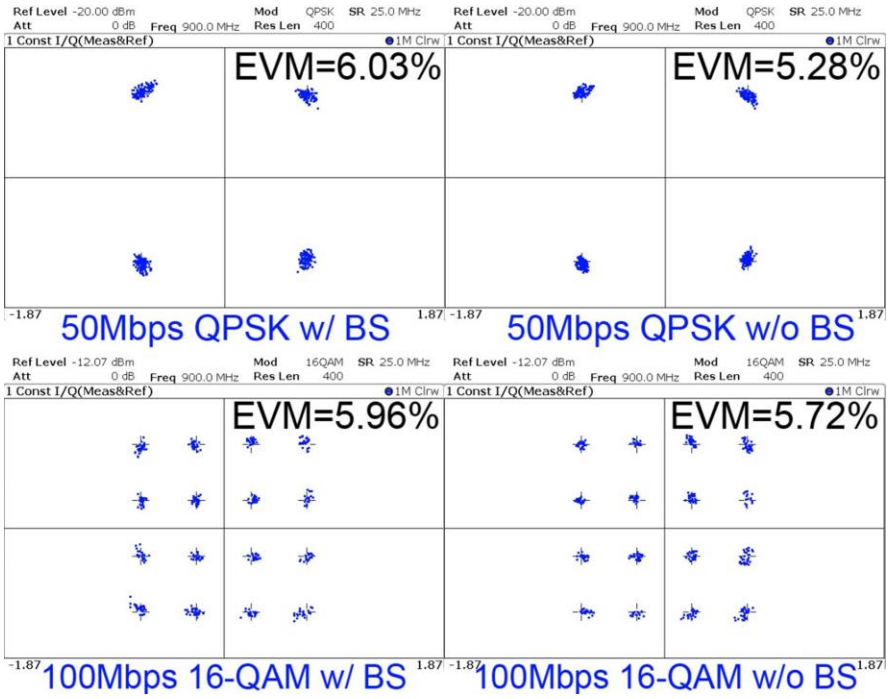


Fig. 3.30. Measured EVM for QPSK/16-QAM at 25 MSps with/without BS.

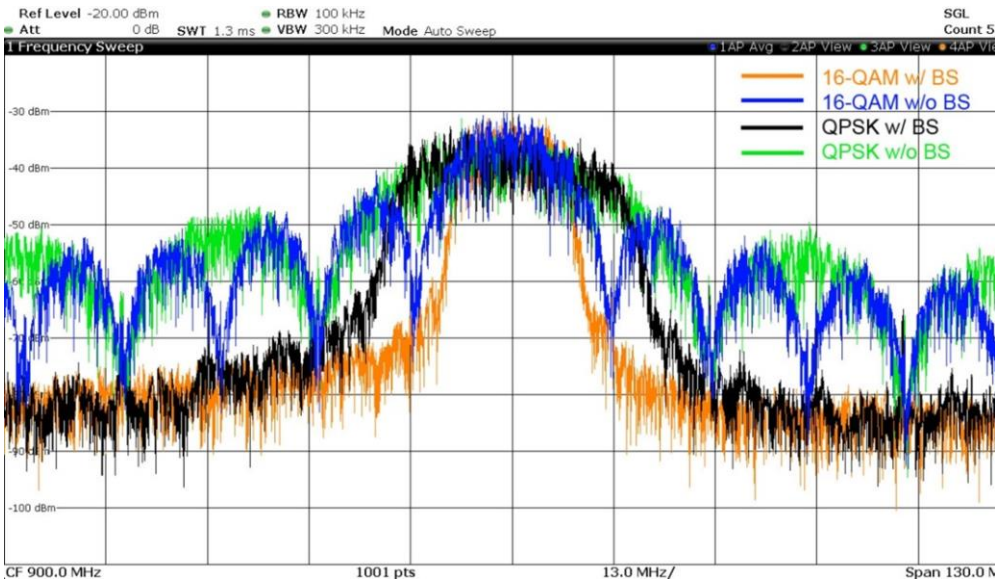


Fig. 3.31. Comparison of output spectrum with/without BS for QPSK and 16-QAM at 50 Mbps.

The measured constellation for QPSK/16-QAM with and without BS is shown in Fig. 3.30. For QPSK at 50 Mbps and 16-QAM at 100 Mbps, EVMs better

than 6% are observed.

Fig. 3.31 presents the output spectrum with fixed data rate of 50 Mbps. As illustrated, 38 dB side-lobe suppression is achieved with BS, which is 25 dB more compared to TX without BS. In addition, 16-QAM mode is also twice more spectral efficient than QPSK. To verify the robustness of the TX system, similar measurement has been done across 10 chips.

Fig. 3.32 plots the EVM performance at different data rate under different modulation. Only 1% EVM variation is observed for the collected data over 10 chips. It should be noted that 16-QAM can reach 200 Mbps data rate with EVM better than 9%.

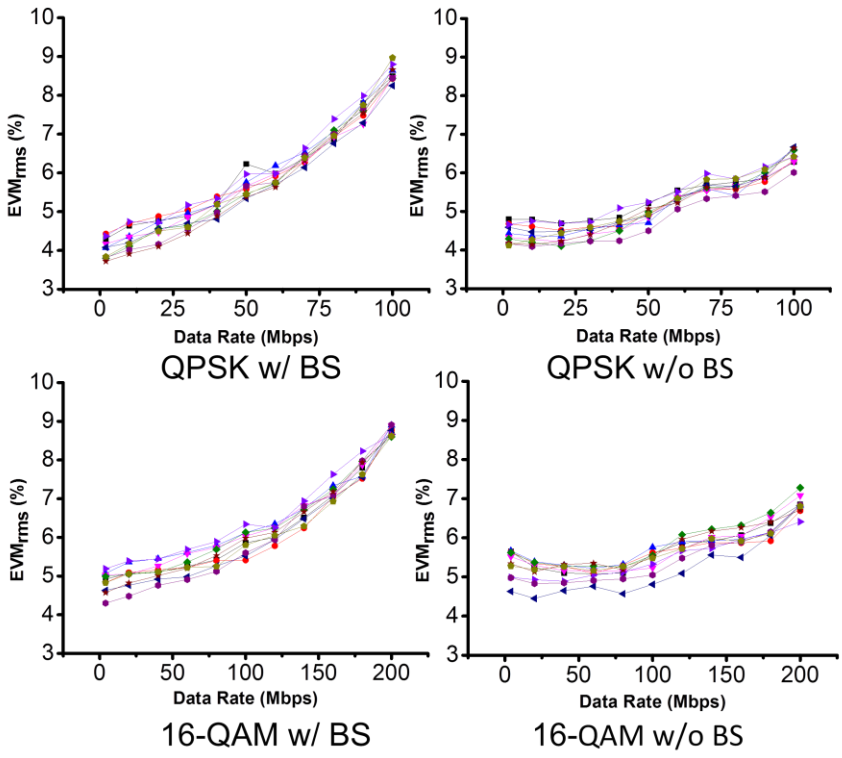


Fig. 3.32. Measured TX EVM variations versus data rate across 10 chips.

Table 3.2. TX Power Breakdown.

Modulation	QPSK w/o BS	QPSK w/ BS	16-QAM w/o BS	16-QAM w/ BS
Data Rate	50 Mbps	50 Mbps	100 Mbps	100 Mbps
ILRO & Buffer	660 μW			
Pulse Gen. & S/D	58 μW			
XTAL	115 μW			
PA	394 μW			
Digital Modulator	67 μW	1.31 mW	73 μW	1.33 mW
Total	1.29 mW	2.54 mW	1.3 mW	2.56 mW

Table 3.3. Performance Comparison.

	Liu CICC'08	**Liu ASSCC'11**	**Diao ASSCC'10**	**Izad CICC'12**	**Zhang RFIC'12**	**This work**
Frequency (MHz)	**400**	**2400**	**900**	**915**	**350-578**	**900**
Modulation	**O-QPSK**	**HS-OQPSK**	**O-QPSK/ QPSK**	**O-QPSK/ 8PSK**	**16-QAM***	**QPSK/16-QAM**
Data Rate (Mbps)	**15**	**2**	**50**	**55**	**7.5**	**100**
Output Power (dBm)	**-7/-15**	**-3**	**-3.3/-15**	**-15**	**0.23**	**-9/-15**
Power (mW)	**3.48**	**15**	**5.88/3**	**0.938**	**4.9**	**2/1.3 (w/o BS) 3.3/2.6 (w/ BS)**
Area (mm^2)	**0.7**	**0.35**	**0.28**	**0.038**	**0.7**	**0.08**
Band Shaping	**No**	**Yes, >29dB**	**No**	**No**	**No**	**Yes, >38dB**
Energy/Bit (nJ/Bit)	**0.23**	**7.5**	**0.12/0.06**	**0.017**	**0.65**	**0.02/0.013 (w/o BS) 0.033/0.026 (w/ BS)**
FOM (μW×bit/nJ)	**870**	**66.8**	**3977/527**	**1860**	**1622**	**6290/2433 (w/o BS) 3812/1216 (w/ BS)**
Supply (V)	**1.2**	**1.5**	**1.4**	**0.8**	**1.5**	**1.2/0.77**
Technology	**0.18 μm**	**0.18 μm**	**0.18 μm**	**65nm**	**0.18 μm**	**65nm**

* Circular constellation based 16-QAM.

Under 0.77-V supply, the TX consumes 2.6 mW and 1.3 mW respectively with and without BS while transmitting at 25 MSps with -15 dBm output power. The digital portion which provides BS consumes 50% of the total power as illustrated in Table 3.2. This power can be further reduced by adopting ROM based RRC filter. The TX performance is compared with other similar multi-PSK and 16-QAM TX in Table 3.3. For in-vivo transmitter applications, most transmitters have limited output power at the range of -15 dBm [8, 14, 24]. Due to the lower output power, PA does not limit the overall transmitter energy efficiency. At this output power level, this work achieves the highest data rate of 100 Mbps and energy efficiency of 13 pJ/bit (without BS) compared to others. Due to the simplicity of the proposed TX architecture, the energy efficiency only worsens to 26 pJ/bit with BS. To provide a fair comparison with other transmitters that achieved higher output power level, we adopt FOM shown in (3.14) that is commonly used [8].

$$FOM = \frac{P_{out} \times Data\ rate}{Power\ consumption} (\mu W \cdot bit/nJ) \tag{3.14}$$

As illustrated, this work achieves the best FOM of 6290 μW×bit/nJ while delivering maximum output power of -9dBm without BS. This is 1.6 times better than other transmitters without BS. With BS, our FOM only deteriorates to 3812 μW×bit/nJ, which is about 57 times better than other transmitter with BS.

Fig. 3.33 places this work along with recently reported low-power TXs for similar applications which shows that we achieve the highest data rate and highest energy efficient for TX architecture among the transmitter architectures with BS.

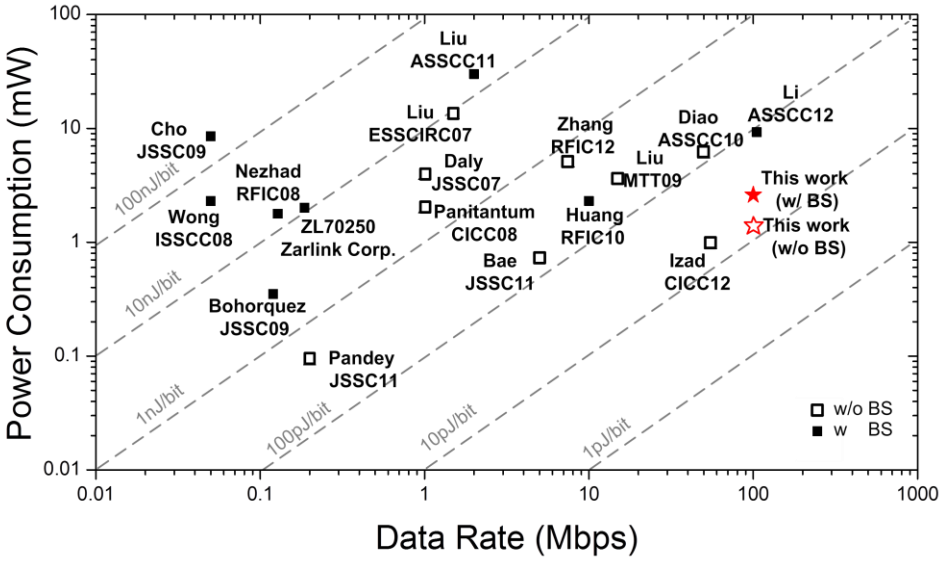


Fig. 3.33. Energy efficiency comparison of low-power TXs.

CHAPTER 4
DESIGN OF MULTI-CHANNEL RECONFIGURABLE GMSK/PSK/16-QAM TRANSMITTER WITH BAND SHAPING

4.1 Introduction

In the previous chapter, a 900 MHz 13-pJ/bit QPSK/16-QAM TX for biomedical application has been proposed. As shown in Fig. 3.1, the proposed architecture adopts energy efficient ILRO with direct phase and amplitude modulation at the digital PA. This provides an energy efficient way of achieving complex 16-QAM modulation and band shaping. Nevertheless, the sub-harmonic injection locking results in fixed output frequency which is limited by the reference frequency.

Recently, FCC has set aside 401~406 MHz for MedRadio or MICS with channel spacing of 300 kHz, targeting for low-data-rate applications. Ref [57]

reported an energy efficient multi-channel multi-modulation TX architecture targeting for WBAN. However, the employed QPSK modulation without band-shaping needs large bandwidth and would not meet the required adjacent channel power ratio (ACPR) specifications (<26 dB). In addition, the use of injection locked LC oscillator (ILO) for multi-phase generation requires careful calibration of resonant tank frequencies which is also not addressed in that work.

Based on the work in Chapter 3 and [57], this chapter aims to propose an improved energy efficient TX for WBAN in four ways. Firstly, the TX is designed to accommodate multiple channels. Secondly, the TX is design to support multiple modulations such as PSK and FSK to maximize the reconfigurability. More spectral efficient modulation techniques, such as 16-QAM are also added to achieve higher data rate with the same given bandwidth. Its spectral efficiency is twice better than QPSK as mentioned in Chapter 2. Thirdly, band shaping is incorporated into PSK and 16-QAM modulation schemes to meet the specified ACPR. Lastly, injection-locked ring oscillator (ILRO) is employed to provide readily available multi-phases without any need of phase calibration.

In Section 4.2, the architecture of the improved energy efficiency TX is proposed. Section 4.3 describes the circuit-level design. The experimental results are presented in Section 4.4 and Section 4.5 draws the conclusions.

4.2 Transmitter Architecture

The proposed TX architecture is shown in Fig. 4.1. Similar to [57], a phase-interpolated dual-injection (PIDI) DLL-based synthesizer is used to provide tunable reference to achieve multi-channel capability. For FSK modulation, the PIDI synthesizer is controlled by the filtered FSK data. For PSK/16-QAM modulation, the synthesizer input is fixed to locate the output frequency at the desired frequency channel. The operation principle of the new PIDI synthesizer will be explained detail in the Section 4.3.1.

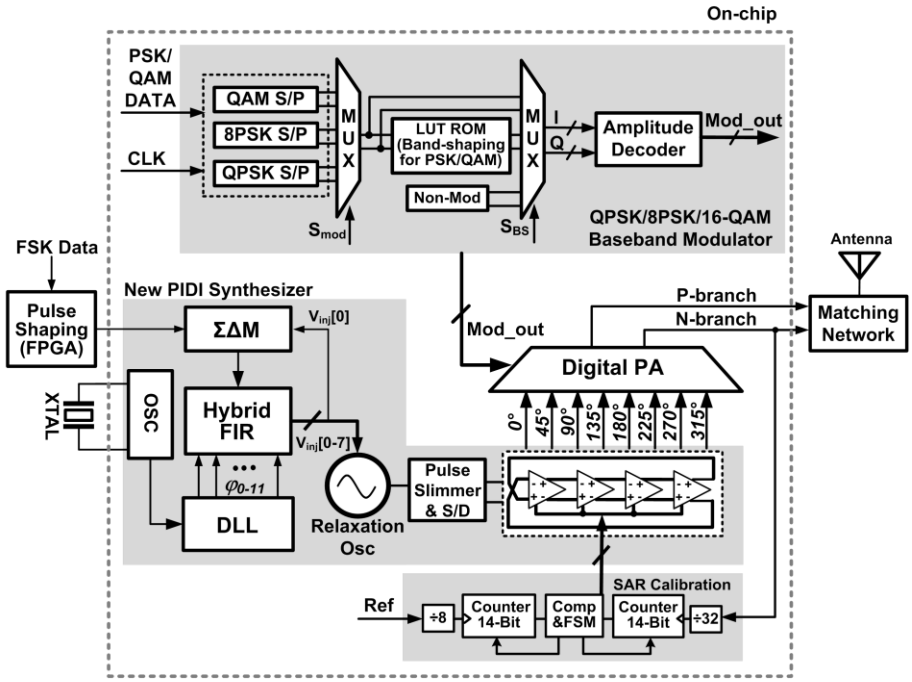
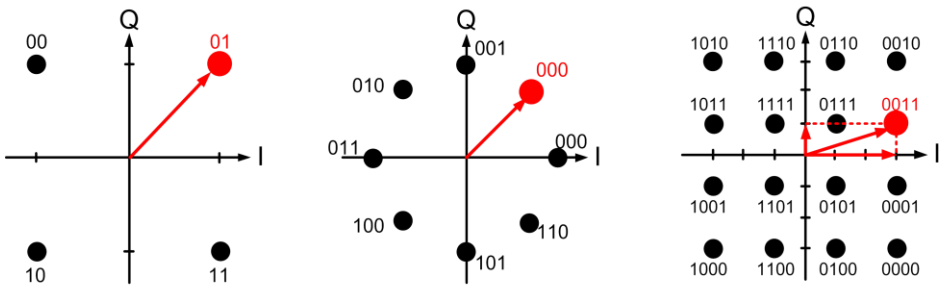


Fig. 4.1. Proposed TX architecture.

As shown, the ILO in [57] is replaced by a pseudo-differential four stage ILRO. This ILRO can readily output the 8 phases (ϕ_0, ϕ_{45}, ϕ_{90}, ϕ_{135}, ϕ_{180}, ϕ_{225}, ϕ_{270}, ϕ_{315}) needed for QPSK, 8-PSK and 16-QAM modulation without any

need of phase calibration. To reduce the output reference spurs, a simple frequency calibration circuit, similar to the SAR frequency calibration mentioned in Chapter 3, is incorporated to match the ILRO free-running frequency and the 3rd harmonics of the injected reference. The use of ILRO also eliminates two additional off-chip inductors needed for ILO in [57].

The eight phases from ILRO will drive the 8-phase branches within the DPA to realize direct modulation which is capable of supporting QPSK/8-PSK/16-QAM modulation. Instead of generating QPSK and 8-PSK from two quadrature phases in Fig. 3.2, 4 phases and 8 phases are directly chosen to represent each constellation point for QPSK and 8-PSK respectively, as illustrated in Fig. 4.2(a) and Fig. 4.2(b). Only the 16-QAM constellation plot is generated from quadrature phases with different amplitudes. Additional buffer is inserted between DPA and ILRO to prevent kick-back noise during phase switching. The DPA drives an external matching network which boosts the output impedance to the DPA while providing impedance matching to the antenna for better PA output efficiency.



(a) (b) (c)

Fig. 4.2. Constellation plot of: (a) QPSK (b) 8-PSK (c) 16-QAM.

4.3 Circuit Implementation

4.3.1 Proposed PIDI Synthesizer

Fractional-N frequency synthesizer is a popular choice to provide multi-channel support due to its fine frequency tuning capability. However, its PLL-based architecture limits the overall power consumption. Firstly, the quantization step of the fractional-N synthesizer depends on the VCO period. For transmitter targeted at MICS band, the quantization step is limited to 1/406 MHz or 2.46ns. This poses a limit on the achievable quantization phase noise. Higher VCO frequency can be adopted to reduce the quantization noise. However, this will imply higher power consumption due to the higher operation frequency of VCO and frequency divider. In this work, in order to preserve the energy efficiency of ILRO without subjected to the limit of quantization phase noise, we propose a PIDI DLL-based synthesizer to achieve multi-channel support [57].

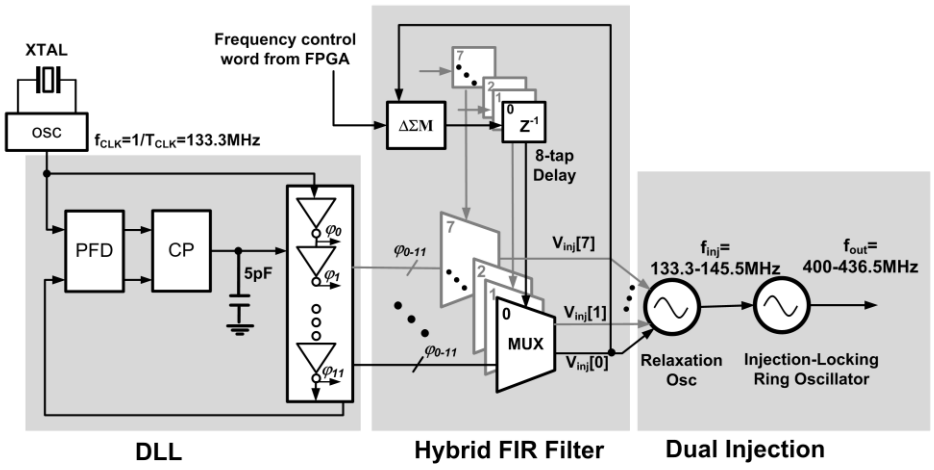


Fig. 4.3. Block diagram of the PIDI synthesizer.

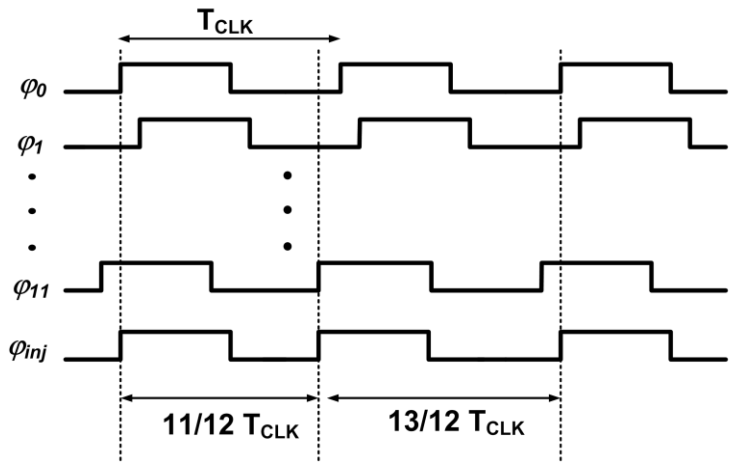


Fig. 4.4. Operation of the frequency interpolator.

Fig. 4.3 describes the detail block diagram of the proposed PIDI synthesizer. It contains three main parts, namely a DLL, a hybrid FIR filter and dual injection oscillator. First, a fundamental mode 133 MHz crystal oscillator is adopted to provide low power on-chip reference for the subsequent DLL. Once the DLL is locked, it will produce 12 evenly spaced clock phases (φ_0, φ_1 …, φ_{11}), all with f_{CLK} = 133.3 MHz. The 2-bit output (-2, -1, 0, 1) generated by a 15-bit delta-sigma modulator (ΔΣM) will randomly select four phases to construct the desired clock period, this results in an output waveform with an average clock period that is a fractional number between $\frac{11}{12}T_{clk}$ and T_{clk}. As illustrated in Fig. 4.4, at the sampling cycle, if the current chosen phase is φ_0 and the next chosen phase is φ_{11}, the clock period will be $\frac{11}{12}T_{clk}$. If the next phase is φ_0, it will correspond to a period of $\frac{13}{12}T_{clk}$. The DSM output will determine the resulting clock period, and thus the next chosen clock phase. Using this principle, quantization noise of the proposed architecture is only $\frac{1}{12}T_{clk}$, which is 0.625 ns. This is equivalent to a fractional-N synthesizer

employing a 1.6 GHz VCO. However, the proposed architecture only contains a DLL running at 133 MHz.

The resulting output exhibits the desired fundamental average frequency component with noise shaping. As sub-harmonic injection locking mechanism is employed, it is the 3rd harmonic average frequency component that will be used for injection. Due to the non-linearity introduced by the harmonic, i.e. x^3, noise folding occurs which increases the close-in phase noise around the 3rd harmonic. In order to minimize this noise folding effect, hybrid FIR at the first injection oscillator is employed to suppress the high frequency components due to noise shaping. As shown in Fig. 4.5 from MATLAB simulation, the noise spectrum at higher frequency is suppressed. Hence, when its 3rd harmonic component is used for injection signal for the 2nd injection oscillator, the closed-in phase noise around the 3rd harmonic will be significantly reduced.

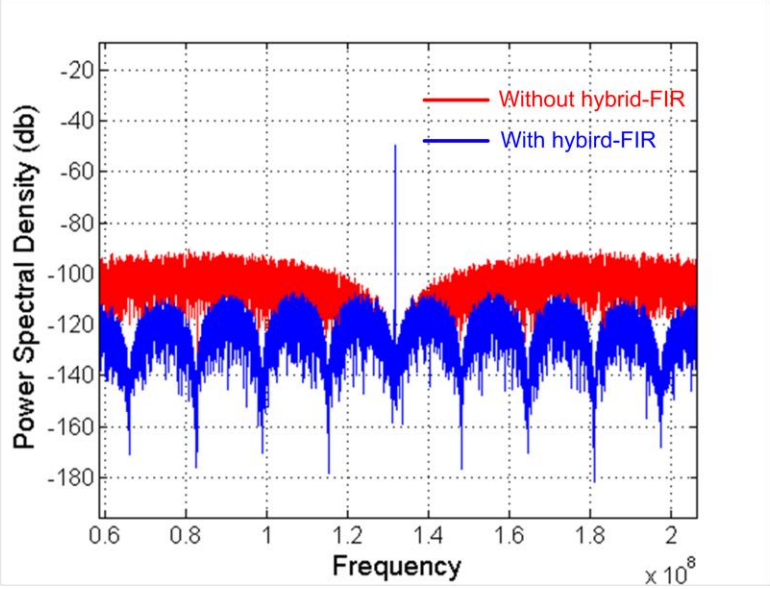
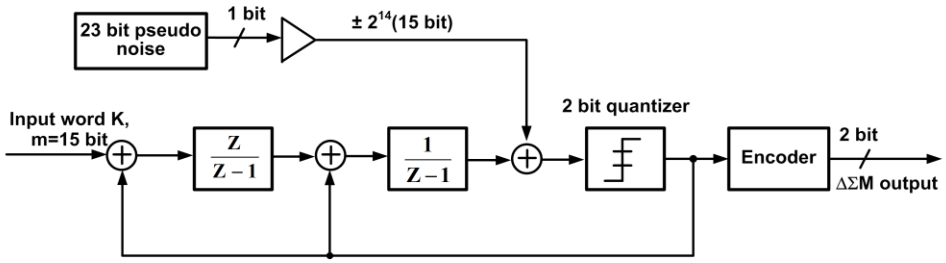
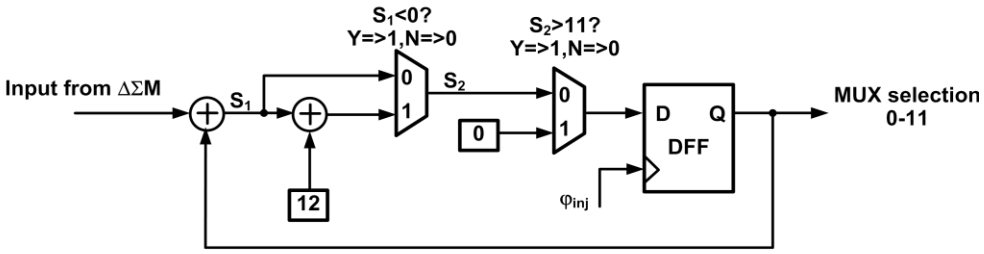


Fig. 4.5. Output spectrum of the hybrid-FIR filter.



(a)



(b)

Fig. 4.6. Block diagram of: (a) 2nd-order ΔΣM with dithering (b) frequency interpolator.

The ΔΣM with dithering and frequency interpolator are as shown in Fig. 4.6. This is a 2nd-order digital delta sigma modulator with an internal bit-length of 21 bits to account for logic overflow. The ΔΣM has an input resolution of 15 bits and 2-bits output. If the output of the ΔΣM is -2, -1, 0, 1, the average output value *N* can be expressed as:

$$N = \frac{K}{2^m} - 0.5 \tag{4.1}$$

where *K* is the input word and *m* is the bit-length of the input equal to 15 in this design. The noise shaping effect of the 2nd-ΔΣM is shown in Fig. 4.7. There is also a 23-bit linear feedback shift register (LFSR) based pseudo random sequence which provides the dithering for the ΔΣM. The frequency

interpolator block in Fig. 4.6(b) receives its input from the ΔΣM block, then select one DLL output taps among φ_0, φ_1 …and φ_{11} during each f_{inj} cycle.

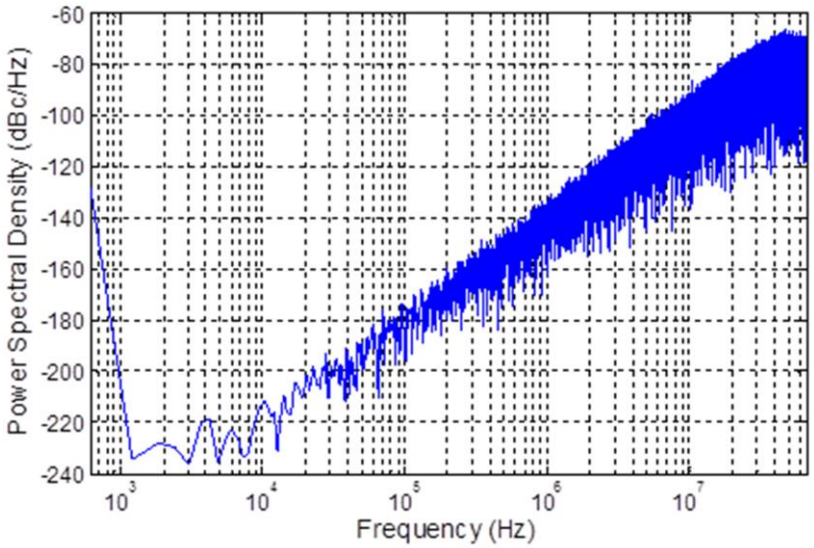


Fig. 4.7. Noise shaping from 2nd-order ΔΣM.

The resulting clock signal is then boosted up by the first injection-locked relaxation oscillator with embedded FIR to boost the fundamental frequency component while suppressing the high frequency noise-shaped component due to DSM. Its output is then used as injection signal for the sub-harmonic locking ILRO to obtain output frequency ranging from 400MHz to 436.5MHz. This dual injection scheme helps suppress the noise folding effect and out-of-band noise. Fig. 4.8 shows the schematic of the first injection-locked relaxation oscillator. The relaxation oscillator has the same architecture as the one in [58]. It is a typical source-coupled oscillator topology. M_3 and M_4 form the gain stage and the frequency of the RC oscillator can be tuned through the varactor C_1. The 8-taps of delayed output from hybrid FIR filter is combined and injected through the current source transistors M_1 and M_2. The fundamental injected frequency is then extracted and boosted by the relaxation

oscillator with its high frequency noise-shaped components suppressed. It consumes only 147 μW.

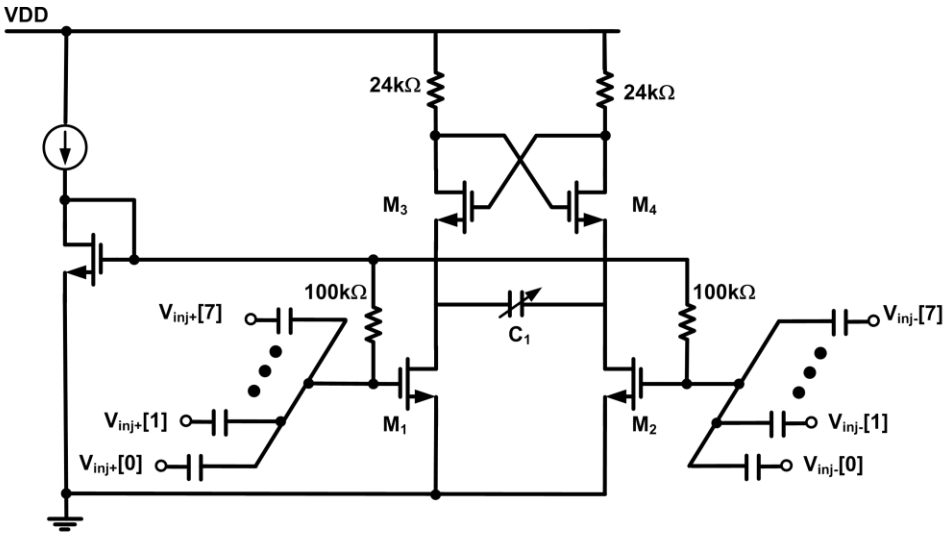


Fig. 4.8. Schematic of the relaxation oscillator.

The second sub-harmonic ILRO similar to Chapter 3 is employed to achieve multi-phase output with low power. The delay cell has been optimized for 401-406 MHz with almost half of the ILRO power consumption in Chapter 3. Mismatch filtering resistors, matched dummy loading and careful layout are used to minimize phase mismatch between the ILRO outputs. From simulation, the combined techniques result in 1° phase mismatch. One key advantage of this architecture compared to [57] is that it eliminates any need of output phase calibration.

4.3.2 Digital Power Amplifier

Fig. 4.9 shows the simplified schematic of the DPA with 8 phase branches. Each phase branch consists of a 5-bit transistor array which provides the adjustable phase current component. By summing the adjustable phase current component from two phase branches at the matching network, various constellation points for QPSK/8-PSK/16-QAM modulations can be obtained. Band-shaping can also be achieved by providing smooth constellation point transition through the 5-bit amplitude control for each phase current component. For GMSK modulation, only the phase branch of ϕ_0 with fixed current amplitude within the DPA is activated. The frequency input to PIDI synthesizer is then tuned according to the input data to achieve the desired frequency modulation and Gaussian filter shaping.

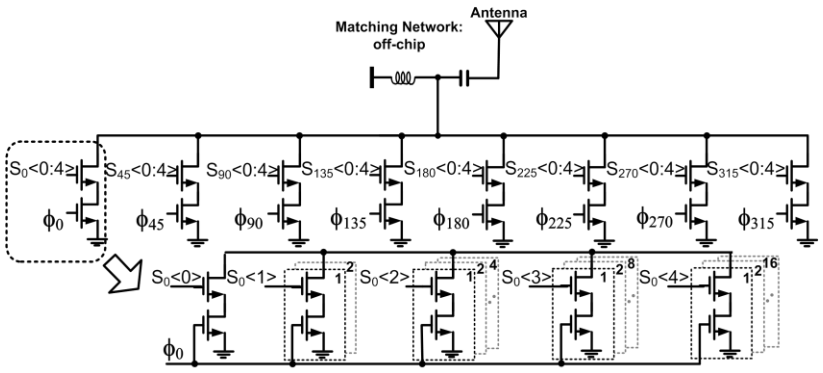


Fig. 4.9 Simplified schematic of DPA.

From the simulation, it is observed that by using NMOS only phase branches within the DPA for summing will give rise to a DC output offset current as shown in Fig. 4.10. Coupled with the input data clock signal, it will give rise to a close-in clock spur around the output spectrum. This close-in spur could deteriorate the EVM and violate the spectral mask. It is found from the

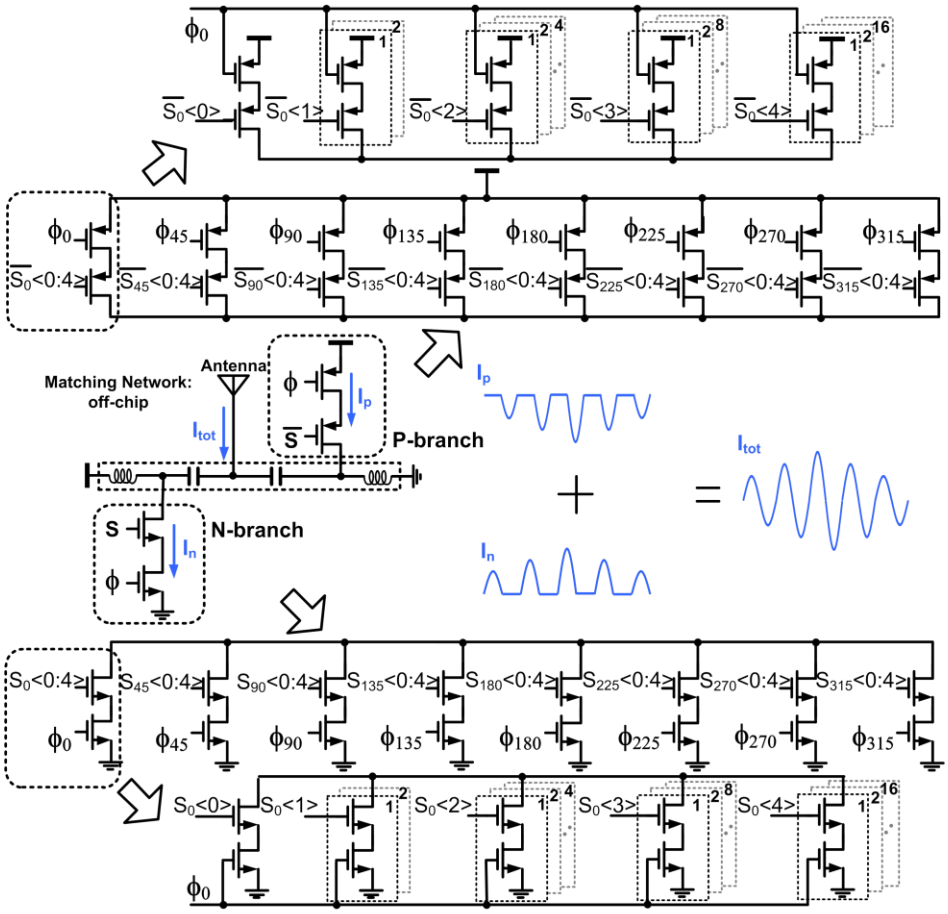
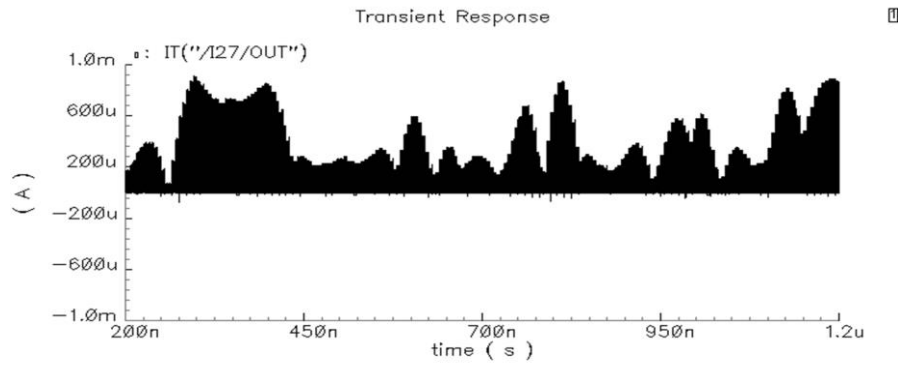


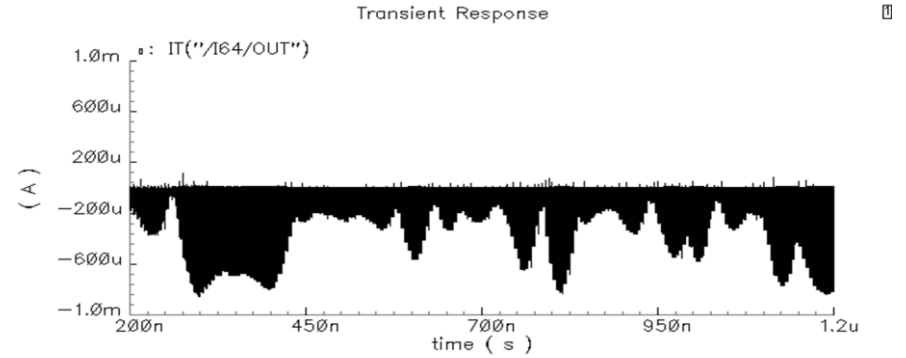
Fig. 4.10. Modified schematic of DPA.

simulation that the spur can be suppressed if the DC output offset current can be reduced. Hence, we proposed to add in a PMOS branches to balance the common mode current due to the NMOS phase branches. The idea is similar to [59] where the common mode voltage signal is cancelled whereas here the common mode current signal is cancelled. During the positive ϕ cycle, the NMOS phase branches will sink the output current while the PMOS phase branches are off, which gives rise to an output current with a positive offset. During the negative ϕ cycle, the PMOS phase branches will source the output current while the NMOS phase branches are off which results in an output current with a negative offset. If the PMOS sourcing current matches to the

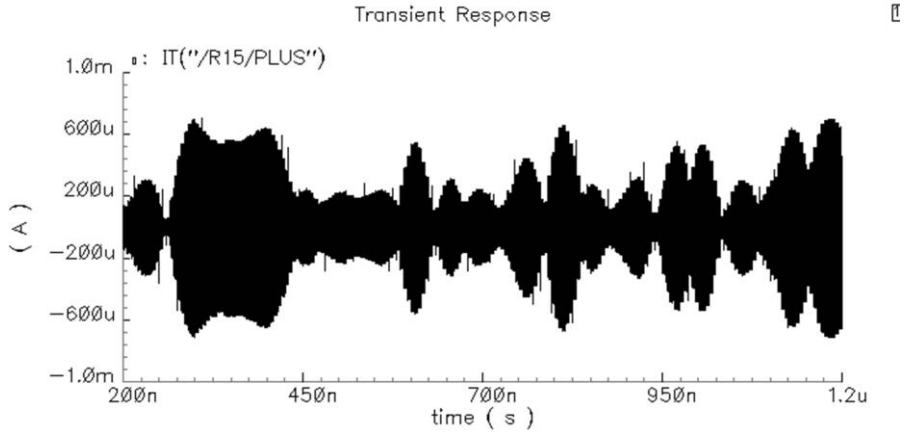
NMOS sinking current, this will give rise to a zero DC offset current on average as shown in Fig. 4.10 and thus eliminate the close-in clock spur.



(a)

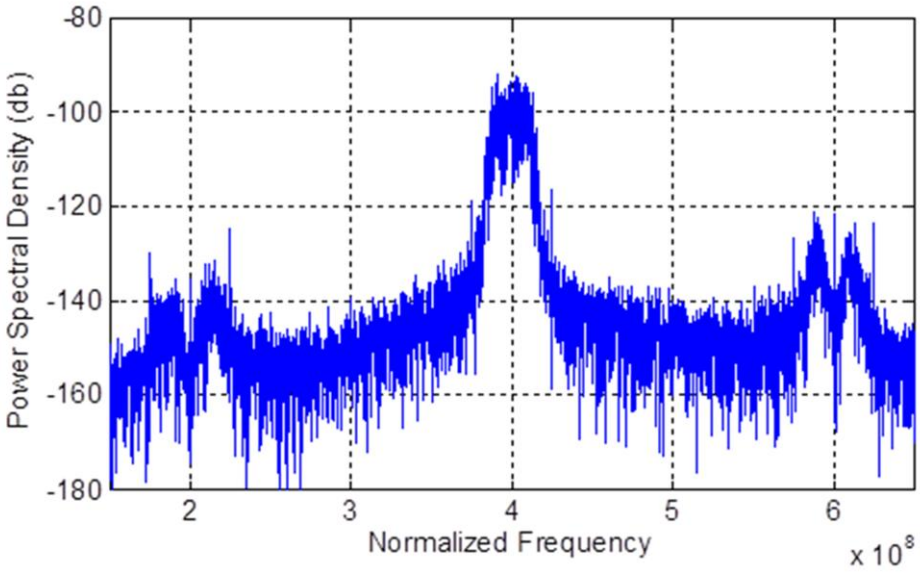


(b)

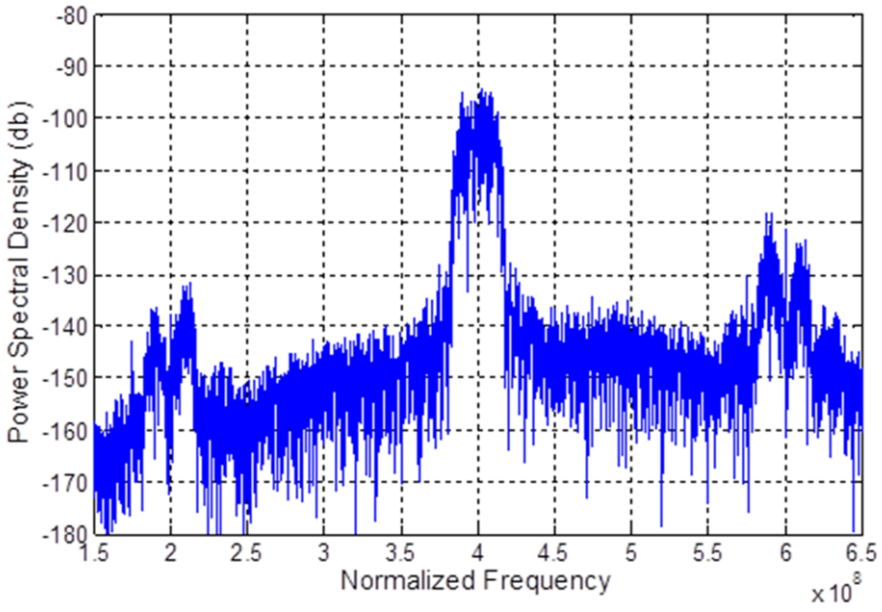


(c)

Fig. 4.11. Current Output of (a) N-branch DPA (b) P-branch DPA (b) N-branch + P-branch DPA.



(a)



(b)

Fig. 4.12. Simulated spectrum (a) N-branch DPA (b) N-branch + P-branch DPA.

The simulated PA output current is shown as Fig. 4.11. Fig. 4.11 (a) and (b) shows the I_n and I_p respectively and Fig. 4.11(c) is I_{tot}. Fig. 4.12 illustrates the

simulated spectrum of the N-branch DPA and the modified DPA. As shown in Fig. 4.12 , for N-branch only DPA, the clock spurs appear at *N*×*upsampling clock* and *N*×*upsampling clock* ± *symbol rate*. For the modified DPA, as shown in Fig. 4.12(b), the clock spurs are successfully suppressed.

4.3.3 QPSK/8-PSK/16-QAM Band Shaping Modulator

The DPA is controlled by QPSK/8-PSK/16-QAM baseband modulator shown in Fig. 4.13. External data can be employed as input for normal operation while on-chip pseudo random generator is used for quick testing. Depending on the desired modulation schemes, the data will be first converted into parallel I/Q data. If band-shaping is needed, I/Q data will go through a look-up-table (LUT) stored in read only memory (ROM) to give an equivalent filter output. Otherwise, LUT will be bypassed to achieve higher energy efficiency.

The design of the band shaping filter is similar to the one described in Section 3.3.2 and Section 3.4.5. In the previous sections, the 8 times up-sampling is divided into two steps to save the power. In this design, since the LUT provides the up-sampled and filtered output directly, 8 times up-sampling and higher order RRC can be adopted for the ROM calculation.

An upsampler with a factor of 8 followed by a RRC filter model is built in MATLAB Simulink for verification. The *Group delay* in (3.13) is chosen to be 3 based on the simulation of spectrum performance. According to (3.13), the

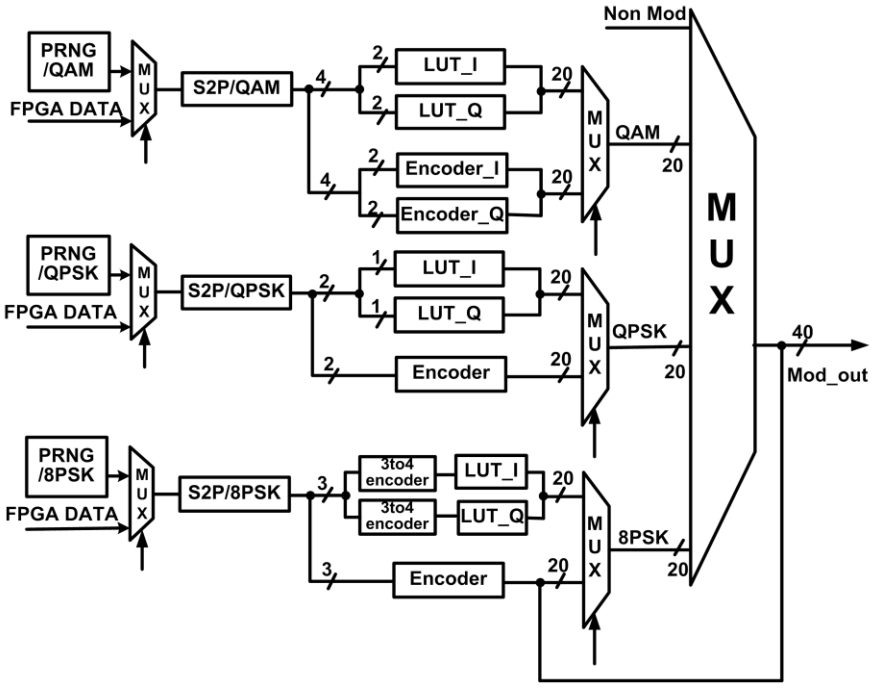


Fig. 4.13. Algorithm of QPSK/8-PSK/16-QAM band-shaping modulator.

number of taps is 2×8×3+1=49. Then it is decreased to 41 while observing the spectrum and EVM performance, similar to Section 3.4.5. The impulse response of the 41 taps RRC filter is shown as Fig. 4.14.

For a discrete-time FIR filter as shown in Fig. 3.20, the output is a weighted sum of the current and a finite number of previous values of the input, shown as follows:

$$\begin{aligned} y[n] &= b_0 x[n] + b_1 x[n-1] + \cdots + b_N x[n-N] \\ &= \sum_{i=0}^{N} b_i \cdot x[n-i] \end{aligned} \tag{4.2}$$

where $x[n]$ is the input, $y[n]$ is the output, b_i is the coefficient and N is the filter order.

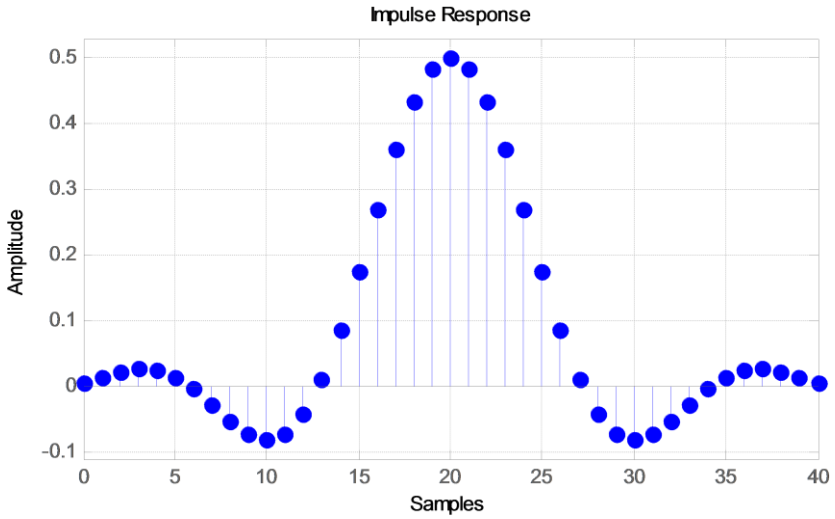


Fig. 4.14. Impulse response of the designed 41 taps RRC filter.

As mentioned in Section 3.4.5, the *Group delay* is the number of symbol periods between the start of the filter's response and the peak of the filter's response. Therefore, the output is related with current 6 input symbols if *Group delay* equal to 3. Thus, for 2-bit QPSK, the ROM address is 2^6=64. For 4-bit 16-QAM, the ROM address is 4^6=4096. Then each input symbol will be interpolated with 7 zeroes for 8 upsampling. These 6×8=48 samples are multiplied by the coefficient and sum together according to (4.2), i.e. sample 1 to sample 41 determine the output $y[1]$, sample 2 to sample 42 determine the output $y[2]$, sample 8 to sample 48 determine the output $y[8]$, and so on. Totally, for each address with 48 interpolated samples, there will be 8 outputs.

All the ROM values are calculated in MATLAB and coded using Verilog. Table 4.1 shows the example of the ROM for QPSK. $y[1]$ to $y[8]$ are the 8 serial-out outputs. The ROM output is truncated into 6-bit to control the digital PA according to the EVM performance and spectrum analysis. Each signed 6-bit output has been decoded as unsigned number while the MSB indicates

the polarity.

Table 4.1 Example of ROM for QPSK.

Output / Address	$y[1]$	$y[2]$	$y[3]$	$y[4]$	$y[5]$	$y[6]$	$y[7]$	$y[8]$
000000	101011	101010	101010	101010	101010	101010	101010	101010
000001	101011	101100	101100	101100	101100	101100	101100	101100
…								
111111	010101	010110	010110	010110	010110	010110	010110	010110

Therefore, the ROM array size for 16-QAM is 4096×48. For QPSK, the ROM array size is 64×48. Since all the calculation and decoding have been completed in MATLAB, the LUT reduces the power consumption almost by half compared to the direct digital FIR filter implementation in Chapter 3.

4.4 Chip Verification and Measurement Results

The measurement setup is similar to the one in Chapter 3, as shown in Fig. 4.15. FPGA is used to control the ΔΣM input for FSK modulation. The chip die is bond-wired and packaged into a QFN40 package which is soldered on the PCB for testing.

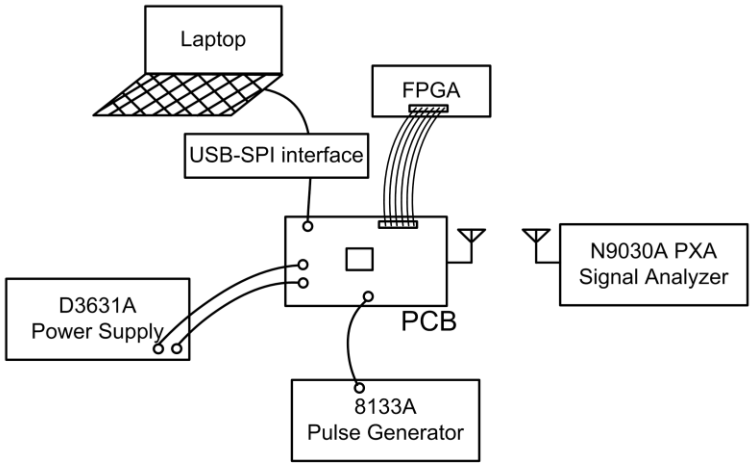


Fig. 4.15. Simple test setup diagram.

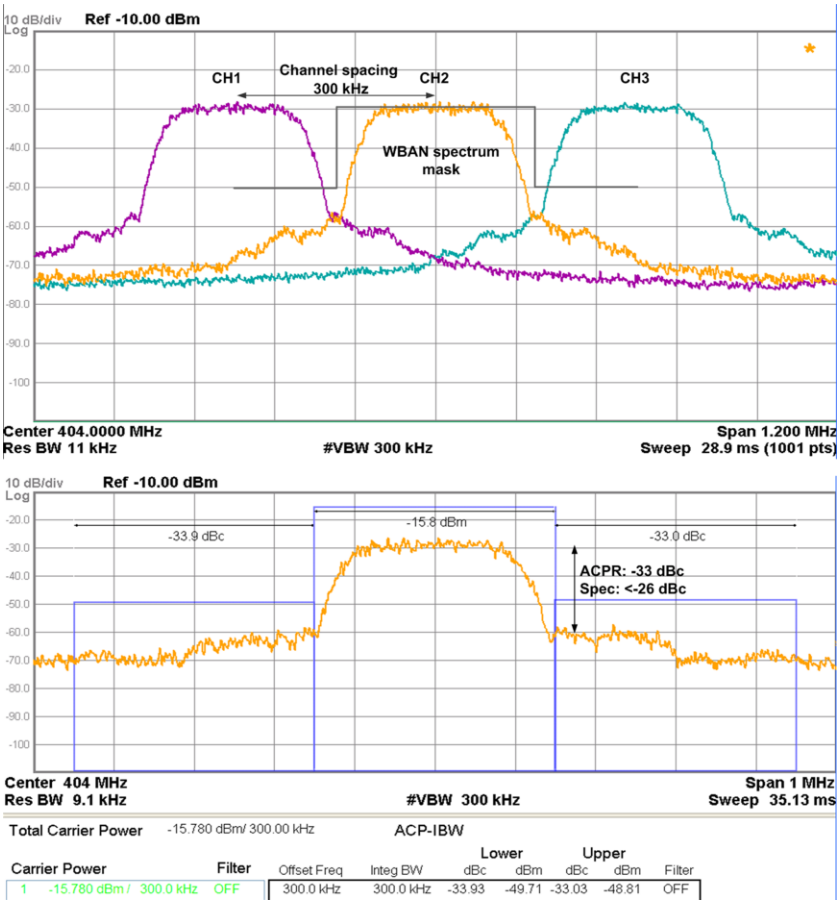


Fig. 4.16. Three adjacent 16-QAM channels output spectrum with 300 kHz spacing and channel ACPR.

The TX is implemented in 65-nm CMOS technology. The output frequency of TX covers from 400 MHz to 436.4 MHz, which can easily meet the MedRadio requirement. The measured 16-QAM spectrum of three adjacent 300-kHz channels and the ACPR are shown in Fig. 4.16. Thanks to the band-shaping and spectral-efficient modulation, each channel can now support up to 750 kb/s without violating the spectral mask and the ACPR is -33 dB. The measured frequency resolution is 1 kHz.

Fig. 4.17 shows the power spectrum for GMSK/QPSK/8-PSK/16-QAM with band-shaping for the same data rate of 187.5 kb/s. As illustrated, more than 30-dB side-band suppression can be achieved. Band shaping can be disabled to achieve higher energy efficiency with poorer spectral efficiency.

The measured EVM is shown in Fig. 4.18. All modulation achieves EVM better than 6%, meeting the requirement for all desired modulations. For the maximum given bandwidth of 5 MHz, the TX can achieve 12.5 Mb/s. If wider bandwidth can be allocated, the TX can achieve 25 Mb/s using 16-QAM with EVM less than 7.29%.

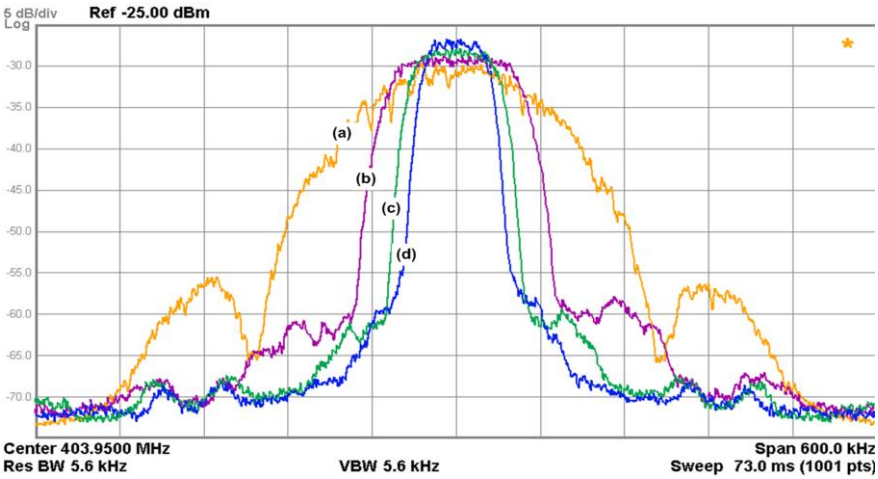


Fig. 4.17. Output spectrum of (a) GMSK (b) QPSK (c) 8-PSK (d) 16-QAM for 187.5 kb/s data rate.

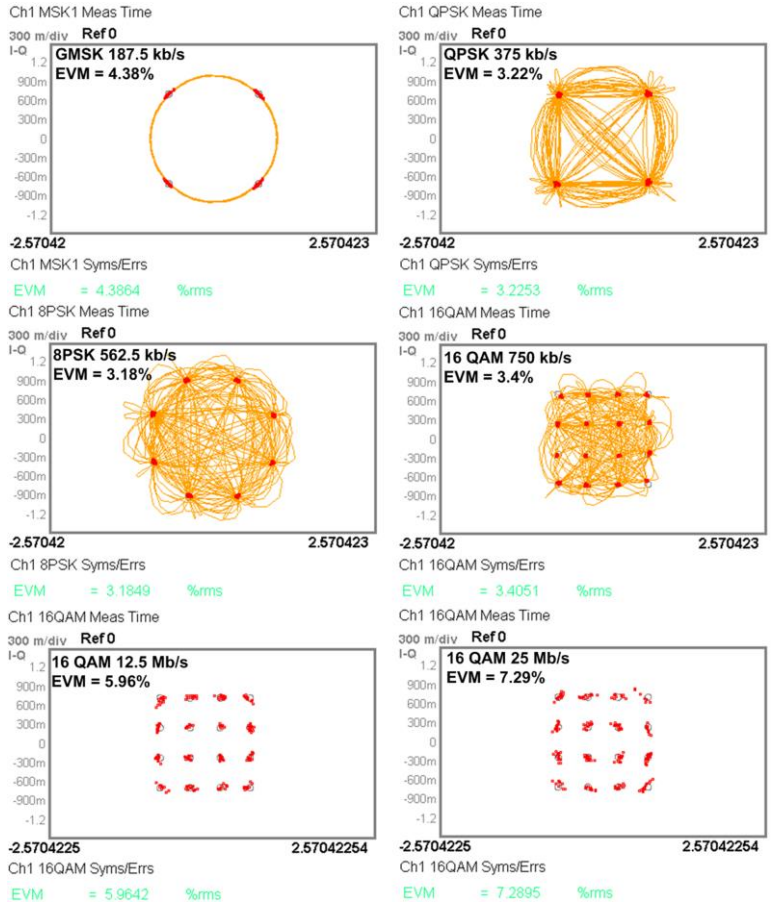


Fig. 4.18. Measured EVM of GMSK/QPSK/8-PSK/16-QAM at different data rates.

The TX performance is summarized and compared with others in Table 4.2 This design is the only TX that supports FSK, PSK and 16-QAM modulations. It consumes power of 2.46 mW for FSK, and 2.58 mW for both PSK and 16-QAM. The TX supports band shaping with more than 30-dB side-band suppression, which maximize the spectral efficiency with ACPR of -33 dB. The TX also achieves energy efficiency of 103 pJ/bit for 16-QAM at 25 Mbps. The TX occupies an active area of 0.4 mm^2. The area is larger than [57] because of the on-chip ILRO and the digital signal processing employed for band shaping. Fig. 4.19 shows the die photo and Fig. 4.20 illustrates the power breakdown.

Table 4.2 Performance Summary and Comparison.

Reference	J. Pandey JSSC May. 2011	J. Bae JSSC Apr.2011	Y. Liu ISSCC 2012	Cheng ISSCC 2013	**This work**
Frequency (MHz)	400 MICS /ISM	920 SIM	2300-2400 BAN /BLE	400-436.4 WBAN/ISM	**401-406 MICS/MedRadio**
Modulation	FSK	FSK	FSK/PSK	FSK/PSK*	**GMSK/PSK /16-QAM#**
Channel Selection	NO	YES	YES	YES	**YES**
Max Data Rate (Mbps)	0.2	5	2	5(FSK) 20(QPSK)	**25 (16-QAM)**
Output Power (dBm)	-17	-10	-1	-8	**-15**
Power (mW)	0.09	0.7	5.4	2.2	**2.46(FSK) 2.58(PSK/16-QAM)**
Phase Noise (dbc/Hz)	-105.3@ 300kHz	-120@ 1MHz	-111@ 1MHz	-107@ 1MHz	**-105@ 1MHz**
In-band Phase Noise (dbc/Hz)	-104	NA	-86	-98	**-99**
Band Shaping	NO	YES	NO	Only for GMSK	**Yes (>30 dB)**
Energy/Bit (pJ/Bit)	450	140	2700	110-440	**103**
Area(mm^2)	0.04	0.35	1.22	0.23+	**0.4**
Supply (V)	1	0.7	1.2	0.9	**0.9**
Technology	130nm	180nm	90nm	65nm	**65nm**

*Phase calibration is done manually and is not included

#No phase calibration

+Two additional off-chip inductors for 2nd ILO

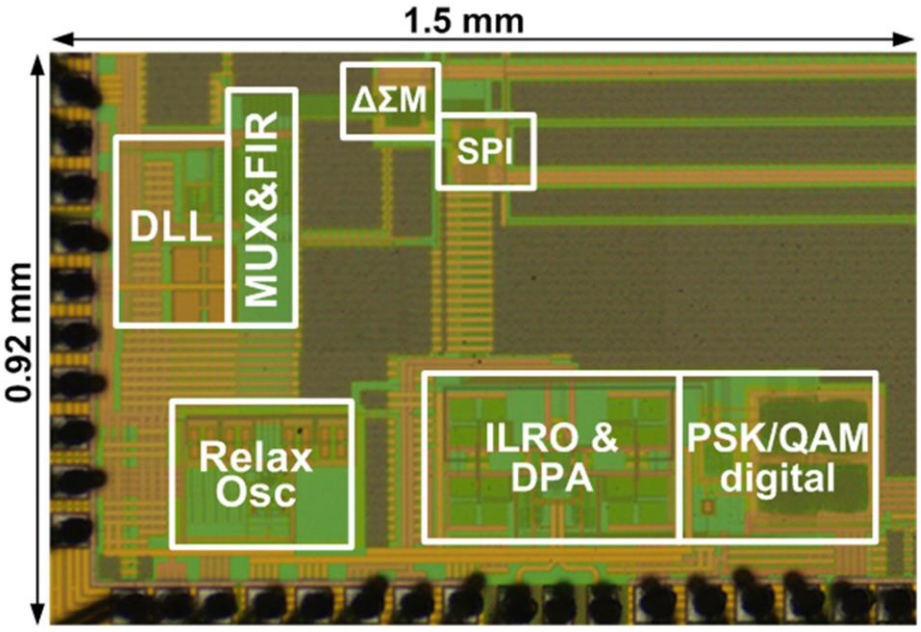


Fig. 4.19. Die photo.

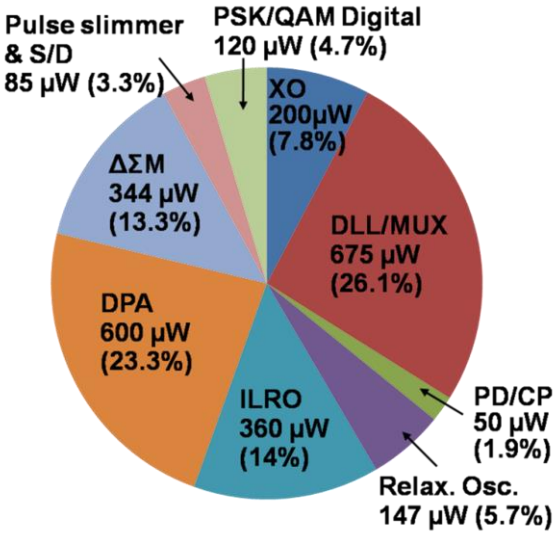


Fig. 4.20. TX power breakdown.

CHAPTER 5
CONCLUSION AND FUTURE WORKS

5.1 Conclusion

Biomedical implantable and wearable system calls for high energy efficiency wireless TX. The works presented in the thesis covers the details of the TX design and implementation as well as chip verification.

Firstly, the background for biomedical application is introduced, and the conventional TX design including architecture and modulation scheme are reviewed.

Secondly, for high-data-rate applications such as neural recording and capsule endoscopy, a 13-pJ/bit 900 MHz QPSK/16-QAM band-shaped TX is presented. Unlike the conventional TX architecture, this work adopts an injection-locking oscillator coupled with a quadrature modulation digital PA

to realize QPSK/16-QAM modulation in an energy efficiency way with effective side-band suppression of more than 38 dB. Under 0.77-V supply, the TX achieves 26 pJ/bit and 13 pJ/bit respectively with and without activating band shaping.

Thirdly, based on the first work, a multi-channel 401~406 MHz GMSK/PSK/16-QAM TX is proposed. This reconfigurable TX targetes at supporting both the low data rate WBAN as well as the high data rate applications. Multiple channels are achieved using a DLL-based dual injection phase interpolated synthesizer. Benefits from ILRO, the DIPI synthesizer can generates 8 phases directly without phase calibration. Implemented in 65-nm CMOS, the TX attains less than 6% EVM for data rate up to 12.5 Mb/s with energy efficiency of 103 pJ/bit.

5.2 Future Works

Although the N/P branch DPA proposed in Chapter 4 will cancel the DC offset theoretically, the mismatch between the N branch and P branch will still increase the spur level. Thus, other mismatch cancellation technique may need to be explored for future research.

Another promising direction is the investigation of the new PIDI synthesizer. Firstly, DLL can also be replaced by an injection locking oscillator to generate multi-phases. Secondly, since the ring oscillator is adopted as second stage injection, the suppression of noise folding is slightly worse than the one used in LC oscillator, which is worthwhile to be improved.

The research conducted over the past four years focuses on the design of the energy efficient TX for biomedical applications. To be applied in the wireless neural recording system or capsule endoscopy, a system-on-chip solution is required. The TX should be integrated with other blocks such as digital baseband, receiver, JPEG encoder IC, etc. Our earlier work [60] demonstrated a Transceiver SoC with QPSK TX which worked well in the implantable device. Replacing that QPSK TX with the proposed work is the next step forward.

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