DESIGN OF LOW-POWER LOW-VOLTAGE SUCCESSIVE-APPROXIMATION ANALOG-TO-DIGITAL CONVERTERS

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Declaration

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

LI YONGFU
15TH JULY 2014

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Design of Low-Power Low-Voltage Successive-Approximation Analog-to-Digital Converters

by

Li Yongfu

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Abstract

This dissertation proposes new circuit design techniques for Successive-Approximation-Register (SAR) Analog-to-Digital Converters (ADCs) and capacitive-array Digital-to-Analog Converter (DACs). A dual-channel, configurable 4-to-10-bit SAR ADC is proposed and fabricated in 130-nm CMOS technology. It operates at a supply voltage of 0.6-V and achieves a maximum sampling rate of 250-kS/s and a FOM of 24-fJ/step. To reduce the area and power consumption per channel, the ADC uses a dual-capacitive-arrays DAC architecture and reuses multiple building blocks, such as the DACs, the comparator and the SAR logic, for the dual-channel ADC. To minimize the switching power consumption across all resolution modes, an energy-efficient charge-recovery switching scheme is proposed. It achieves a 3.6-to-77.5$\times$ reduction compared to the conventional charge-redistribution scheme.

As the resolution of the ADC increases, the matching requirements for the unit capacitors (i.e., increase the area of the unit capacitor) and the number of unit capacitors in the conventional binary-weighted capacitive-array (CBW) DAC increases exponentially, thus increasing the area, the switching power consumption and the settling time in the DAC. Therefore, two methods are proposed to address these challenges in high resolution ($>$10-bit) capacitive-array DACs.

First, a placement strategy is proposed to address the layout's mismatches, where a matrix-adjustment method is proposed to optimize the size of the CBW DAC, different placement techniques and weighting methods are proposed for the placement of active and dummy unit capacitors. The resulting star-like placement increases the degree of dispersiveness (i.e., reduce random mismatch), reduces the first-order oxide-gradient-induced mismatches and the second-order lithographic errors and achieves a more symmetrical routing compared to existing works. A homogenization method is also proposed to reduce the asymmetrical fringing

mismatches among the capacitive-array, thus improving the systematic mismatch between the capacitive-array and the dummy capacitors.

Second, two new types of split capacitive-array DAC architectures are proposed to reduce the area, the power consumption and improve the linearity compared to the CBW DAC and the conventional binary-weighted split capacitive-array with a fractional attenuation capacitor (BWA) DAC. A design methodology is proposed to determine the segmentation degree in the DAC for optimum performance. For a 12-bit SAR ADC, the proposed DACs reduce the input load capacitance and area by $2\times$ and $4\times$, respectively, and the switching power by $15\times$ and $15.5\times$, respectively, compared to the CBW DAC. It also improves the linearity, minimizes the mismatch variation and reduces the switching power by $3.75\times$ and $3.87\times$, respectively, compared to the BWA DAC.

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List of Abbreviations

ADC . . . . . Analog-to-Digital Converter
BWA . . . . . Conventional Binary-Weighted Split Capacitive-Array
. . . . . with a Fractional Attenuation Capacitor
CBW . . . . . Conventional Binary-Weighted Capacitive-Array
DAC . . . . . Digital-to-Analog Converter
DCA . . . . . Dual-Array Capacitive-Array
DNL . . . . . Differential Non-Linearity
ENOB . . . . . Effective Number of Bits
FFT . . . . . Fast Fourier Transform
FOM . . . . . Figures of Merit
GHz . . . . . Gigahertz
INL . . . . . Integral Non-Linearity
LSB . . . . . Least Significant Bit
MIM . . . . . Metal-Insulator-Metal
MHz . . . . . Megahertz
MSB . . . . . Most Significant Bit
NP . . . . . Non-Deterministic Polynomial-Time
S/H . . . . . Sample-and-Hold
SAR . . . . . Successive-Approximation-Register
SA . . . . . Simulated-Annealing
SFDR . . . . . spurious-free dynamic range
SNDR . . . . . Signal-to-Noise Distortion Ratio

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Chapter 1

Introduction

1.1 Development of analog-to-digital converters (ADCs)

For the past two decades, the rapid development of complementary metal oxide semiconductor (CMOS) technologies has decreased the power supply voltages, and along with the dynamic power. Power Supply voltages of 5-V, 3.3-V, 2.5-V, 1.8-V and 1.2-V have followed as CMOS line spacings shrank to 0.6-μm, 0.35-μm, 0.25-μm, 0.18-μm, 0.13-μm and sub-100nm. One of the keys to the success of these systems has been the advance in analog-to-digital converters (ADCs) which convert the continuous-time signals to the discrete-time, binary-coded form. ADCs are ubiquitous critical components for information processing, computing, data transmission, and control systems. Despite the large variety of ADCs for various applications, their performances can be summarized by a relatively small number of parameters: sampling rate, resolution (number of bits per sample), signal-to-noise distortion ratio (*SNDR*), spurious-free dynamic range (*SFDR*) and power dissipation [1].

A widely adopted figures of merit (*FOM*), also called *Walden′s* figures of merit, can be used to benchmark all the state-of-the-art ADCs. This *FOM* is the most commonly used for Nyquist ADCs considering resolution, bandwidth and power consumption in order to provide a platform for energy efficiency comparison [2, 3].

$$FOM = \frac{P}{2^{ENOB} \times f_s} \tag{1.1}$$

where P is the power dissipation, f_s is the Nyquist sampling rate, and *ENOB* is the *effective number of bits* defined by the SNDR as:

$$ENOB = \frac{SNDR_{dB} - 1.76}{6.02} \tag{1.2}$$

Figure 1.1 shows the developments of the state-of-the-art ADCs in the *IEEE International Solid-State Circuits Conference (ISSCC)* and *IEEE Symposium on VLSI Circuit (VLSI)* over the last decade [4]. The ADCs are arranged according to their sampling frequency and resolution. A close study of those ADCs developed over the last five years shows that there are three key areas of developments. The first key development is for the application in miniature wireless sensors, which enable remote military surveillance, environmental monitoring, chemical detection and medical monitoring, requiring 8-to-12-bits of resolution at less than 1 MHz frequency. The second key development is for the military radar, software defined radio and terrestial and satellite telecommunications, which require 8-to-14-bits resolution and sampling rates of a few tens of megahertz (MHz) to a few hundreds of MHz range. Most of the academia research have focused on these two research areas. The third development is for high speed instrumentation and optical communication applications, which require more than tens of gigahertz (GHz) sampling rate and additional dedicated on-chip peripheral circuits such as synthesizer, memory blocks

and DSP processors to accomplish the test measurement.

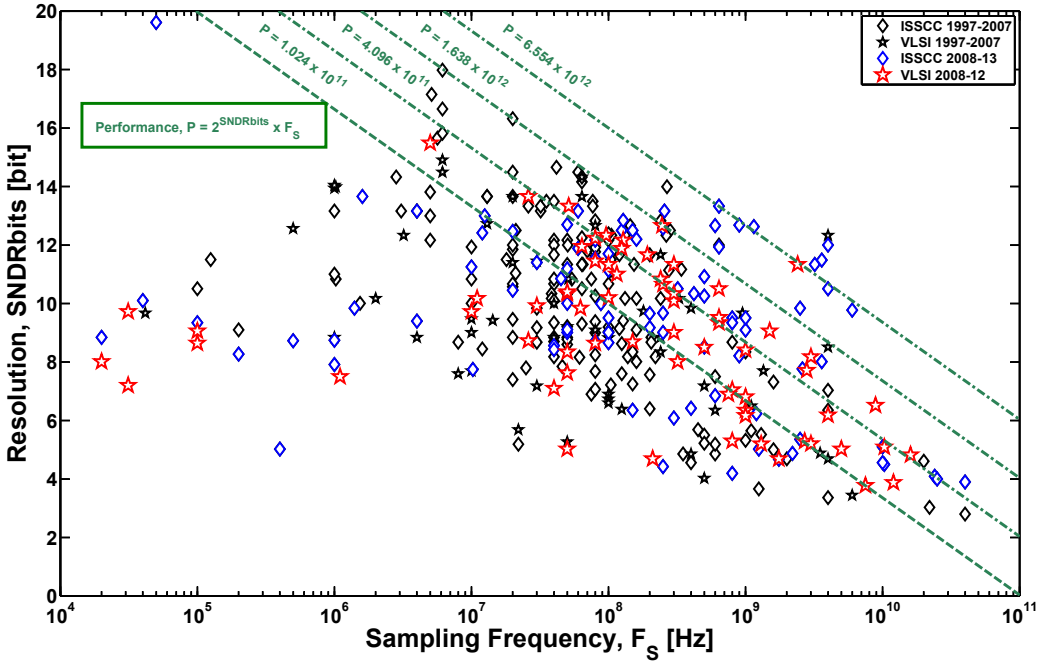

Figure 1.1: Recent research trend of ADC based on Resolution and Sampling Speed [4].

Figure 1.2 compares the energy efficiency versus resolution for the state-of-the-art ADCs. Each green line indicates different orders of magnitude of FOM. It is clearly shown that the performances of the ADCs have improved more than 100× over the last five years.

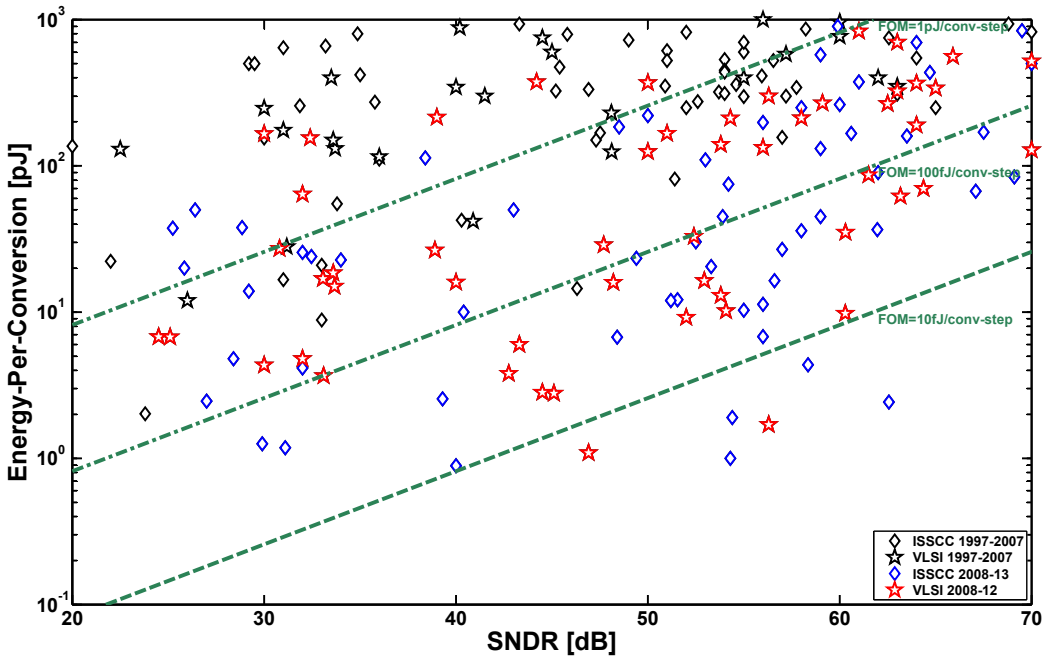

Figure 1.2: Recent research trend of ADC based on FOM [4].

Figure 1.3 shows the FOM of the state-of-the-art ADCs across the years [4]. In particular, the successive-approximation-register (SAR) ADC (highlighted in blue and red) has become the most popular architecture over the last five years [4]. The green line indicates the improvement of SAR ADCs over the years and it is estimated that the performances of the SAR ADCs have improved by 1000× over the last five years. Generally, the FOM of the state-of-the-art SAR ADCs are at least 10× better than other architectures and the best FOM on record is a SAR ADC [4]. This is because the SAR ADC has a lower design complexity compared to other ADCs' architectures, such as pipelined and oversampled sigma delta converters.

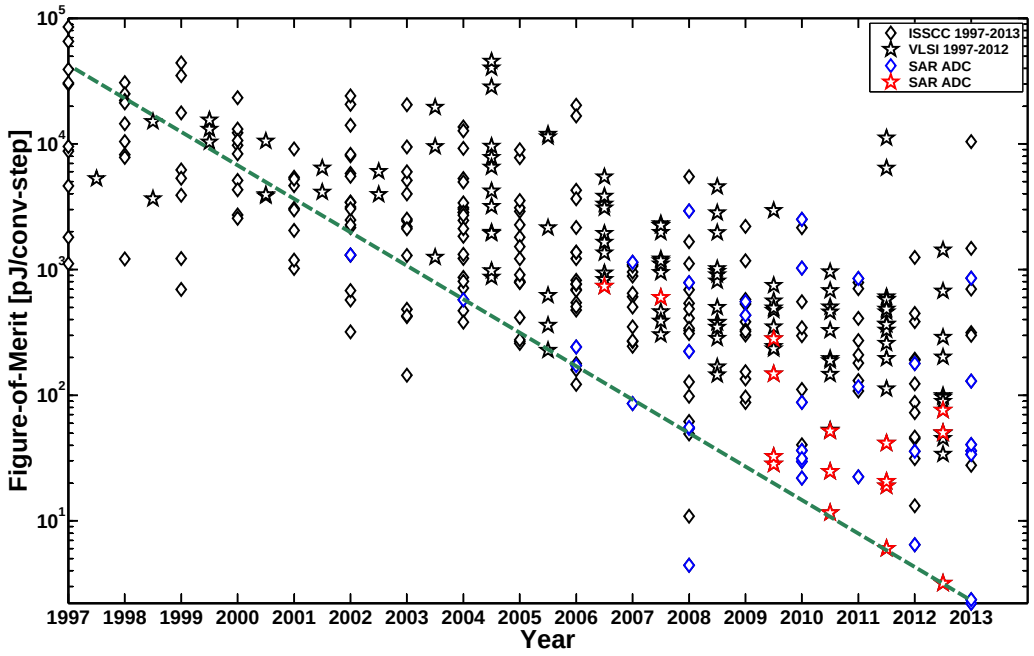

Figure 1.3: Recent research trend of ADC across the years.

1.2 Organization of the dissertation

This dissertation outlines the study and design of low-power SAR ADC and DAC and it is a result of the research performed at the VLSI/Signal Processing Laboratory and Bioelectronics Laboratory, Department of Electrical and Computer Engineering, National University of Singapore between August 2009 and July 2014. The research during this period has resulted in the following publications and journal submissions:

1. **Yongfu Li**, Yong Lian and Perez, V., "Design optimization for an 8-bit microcontroller in wireless biomedical sensors," *IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Nov. 2009, pp.33-36.
2. **Yongfu Li**, Zhe Zhang and Yong Lian, "Energy-efficient charge-recovery switching scheme for dual-capacitive-arrays SAR ADC," *Electronics Letters*, vol. 49, no. 5, pp.330-332, 2013.
3. **Yongfu Li**, Zhe Zhang, Dingjuan Chua and Yong Lian, "Placement for binary-weighted capacitive-array in SAR ADC using multiple weighting methods", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 33, no. 9, pp.1277-1287, 2014.
4. **Yongfu Li** and Yong Lian, "An improved binary-weighted split capacitive-array DAC for high resolution SAR ADCs," *Electronics Letters*, vol. 50, no. 17, pp.1194-1195, 2014.
5. **Yongfu Li**, Wei Mao, Zhe Zhang and Yong Lian, "An ultra-low voltage comparator with faster comparison time and reduced offset voltage," *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2014.
6. **Yongfu Li**, Zhe Zhang and Yong Lian, "A Dual-Channel 0.6-V 250-kS/s 4-to-10-bit Resolution-Reconfigurable SAR ADC for Sensor Applications," under review by *IEEE Journal of Solid-State Circuits*.

7. **Yongfu Li** and Yong Lian, "An unary-binary segmentation with multiple-split capacitive-array DAC architecture for high resolution SAR ADC," submitting to *IEEE Transactions on Circuits and Systems – II: Express Briefs*.
8. **Yongfu Li**, Xiaoyang Zhang, Zhe Zhang and Yong Lian, "A 0.4-to-1.2-V fully-digital low-dropout voltage regulator with fast-transient algorithm", submitting to *IEEE Transactions on Circuits and Systems – I: Regular Papers*.
9. **Yongfu Li**, Zhe Zhang, Xiaoyang Zhang and Yong Lian, "A 726-nW, 940-mVpp, 1-kpulses/s all-digital 3-to-5-GHz impulse UWB transmitter using in 130-nm CMOS", submitting to *IEEE Transactions on Circuits and Systems – II: Express Briefs*.
10. Zhe Zhang, **Yongfu Li**, Koen Mouthaan and Yong Lian, A Miniature inductorless IR-UWB transceiver for wireless short-range communication and vital-Sign, under review by *IEEE Transactions on Biomedical Circuits and Systems*.
11. Xiaoyang Zhang, Zhe Zhang, **Yongfu Li**, Changrong Liu, Yong-Xin Guo and Yong Lian, "A 2.89-μW fully integrated UWB event-driven ECG sensors for dry electrode Use", submitting to *IEEE Transactions on Biomedical Circuits and Systems*.

The contributions and the outline of this dissertation is organized as follows:

Chapter 2: The first chapter begins with the discussion of the fundamentals of the SAR ADC. The discussion is then further extended to various advanced architectures used in the SAR ADCs and DAC architectures. This study allows everyone to have a broader understanding of SAR ADC.

Chapter 3: In the design of a low power SAR ADC, the switching power consumption in the capacitive-array DAC constitutes a significant part of the total power consumption and it even determines the lower bound on the ADC power consumption [5]. It is instructive to have a thorough understanding of the switching power consumption of different types of switching methods. This study leads to the development of a charge-recovery switching method for the dual-capacitive-array DAC architecture. The proposed switching method achieves 98.7% and 46.9% reduction in switching energy and area respectively while maintaining the switching energy constant for different output codes. This scheme achieves the lowest switching energy among existing switching schemes [6].

Chapter 4: The miniature sensor requires multiple ADC channels to sense various telemetry readings. In order to reduce the area and power consumption per channel, the SAR ADC with the dual-capacitive-array DAC architecture, as described in Chapter 3, is extended to multiple-channel ADC, which reuses multiple building blocks, such as the DACs, the comparator and the SAR logic. It operates at a supply voltage of 0.6-V and achieves a maximum sampling rate of 250-kS/s and a FOM of 24-fJ/step. To meet various application-level constraints, the ADC is able to configure its resolution from 4-to-10-bit with a scalable SAR control logic. To minimize the switching power consumption across all resolution modes, the energy-efficient charge-recovery switching method achieves a 3.6-to-77.5$\times$ reduction compared to the conventional charge-redistribution scheme.

As the resolution of the ADC increases, the matching requirements for the unit capacitors (i.e., increase the area of the unit capacitor) and the number of unit capacitors in the conventional binary-weighted capacitive-array (CBW) DAC increase exponentially, thus increasing the area, the switching power consumption and the settling time in the DAC. Therefore, two methods are proposed to address these challenges in high resolution (>10-bit) capacitive-array DACs.

Chapter 5: First, a placement strategy is proposed to address the layout's mismatches, where a matrix-adjustment method is proposed to optimize the size of the CBW DAC and different placement techniques and weighting methods are proposed for the placement of active and dummy unit capacitors. The resulting star-like placement increases the degree of dispersiveness (i.e., reduce random mismatch), reduces the first-order oxide-gradient-induced mismatches and the second-order lithographic errors and achieves a more symmetrical routing compared to existing works. A homogenization method is also proposed to reduce the asymmetrical fringing mismatches among the capacitive-array, thus improving the systematic mismatch between the capacitive-array and the dummy capacitors.

Chapter 6: Second, two new types of split capacitive-array DAC architectures are proposed to reduce the area, the power consumption and improve the linearity compared to the CBW DAC and the conventional binary-weighted split capacitive-array with a fractional attenuation capacitor (BWA) DAC. A design methodology is proposed to determine the segmentation degree in the DAC for optimum performance. For a 12-bit SAR ADC, the proposed DACs reduce the input load capacitance and area by 2× and 4×, respectively, and the switching power by 15× and 15.5×, respectively, compared to the CBW DAC. It also improves the linearity, minimizes the mismatch variation and reduces the switching power by 3.75× and 3.87×, respectively, compared to the BWA DAC.

Finally, Chapter 7 concludes the research findings and suggests future work.

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Chapter 2

Successive approximation analog-to-digital converters

2.1 Basic operation

During the conversion from an analog signal to a digital code word, the ADC performs three different tasks, i.e., sampling, quantization and comparison. Similarly, for a SAR ADC, these three tasks correspond to the sample-and-hold (S/H) sampling circuit, the capacitive-array DAC and the comparator, as shown in figure 2.1. A digital finite state machine (itself called a SAR control logic) applies a binary search algorithm to the DAC and search through all possible quantization levels before converging to the final digital word, which is a digital representation of the analog input. The digital code corresponds to a voltage range defined by the reference voltages, V_{REFP} and V_{REFN}, where the analog input voltage lies.

The details of the conversion process for an N-bit SAR ADC are first described conceptually in [7]. Basically, the SAR ADC operates in 2 different phases: *sampling*, during which the input voltage is stored and *bit-cycling*, during which bits of the corresponding digital word are successively resolved. The entire process

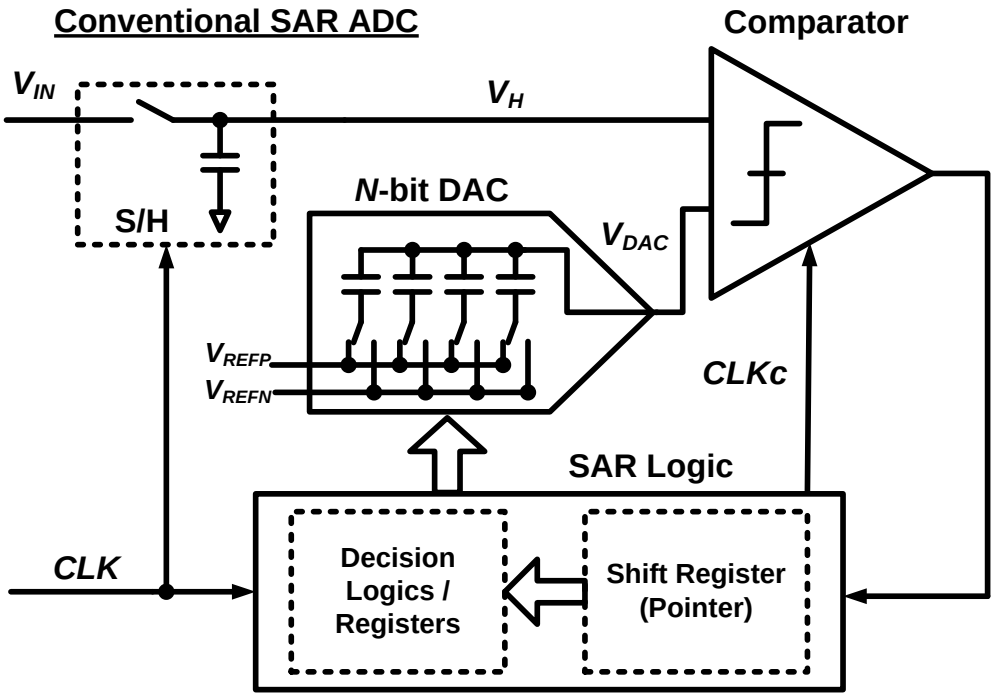

Figure 2.1: Schematic diagram of a N*-bit conventional SAR ADC.*

requires at least N+1 clock periods to complete one conversion cycle.

A detailed switching method is described as follow:

1. *Sampling Phase*: The input analog signal, V_{IN} is fed through a *S/H* sampling circuit so that the sampled voltage, V_H does not change during the entire conversion phase. The output voltage of capacitive-array DAC, V_{DAC} is reset to V_{REFN}.
2. *Bit-cycling Phase*: During the first clock cycle, the MSB capacitor C_1 is connected to V_{REFP} while the remaining capacitors connected to V_{REFN}. The comparator compares and determines if the sampled voltage V_H is larger or smaller than the output voltage of the capacitive-array DAC. The MSB bit (D[1]) is determined and stored in the SAR control logic.
3. In the next bit cycle, the capacitor C_2 is connected to V_{REFP} and C_1 is connected to V_{REFP} if D[1] is 1, else C_1 is connected to V_{REFN}. The SAR control logic changes the output of the DAC according to comparator's output.

V_H is compared to the output of the DAC and the next MSB bit (D[2]) is determined.

4. Step 3 is repeated for the next N - 1 cycle until the output of the DAC converges to the value of V_H within the resolution of the converter.

An example of the voltage waveform of the conventional switching procedure is shown in figure 2.2. The entire process can be simplified into a flow-chart, as shown in figure 2.3.

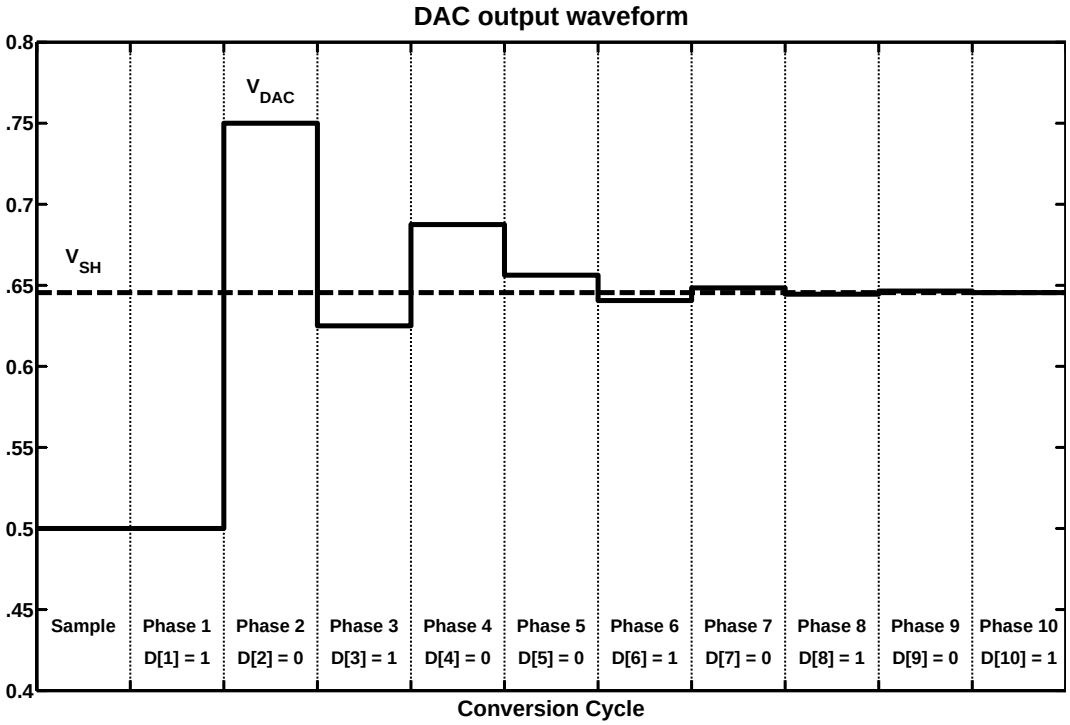

Figure 2.2: Waveform of the conventional switching procedure for a N-bit DAC output waveform.

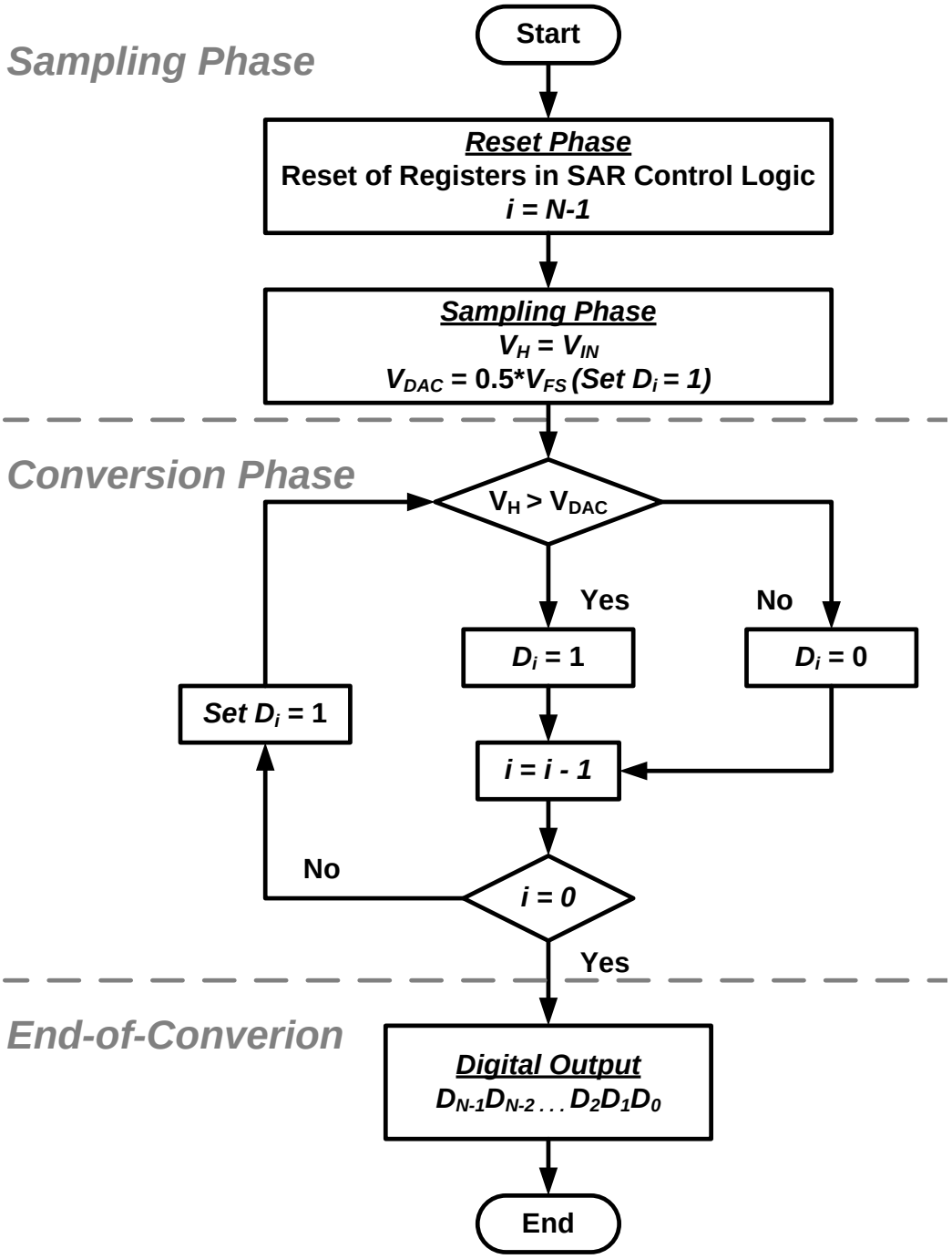

Figure 2.3: Flow Chart for a N-bit conventional SAR ADC.

2.1.1 Conventional charge-redistribution SAR ADC

Beside the architecture as shown in figure 2.1, the conventional binary-weighted SAR ADC can also be used without any additional sampling capacitor for the *S/H* circuit as shown in figures 2.4 and 2.5. This is one of the earliest SAR ADC architecture, which is know as "charge-redistribution" converter [7]. The sampling capacitor is realised by the capacitive-array DAC itself through the "top plate sampling" technique (figure 2.4) or the "bottom plate sampling" technique (figure 2.5) [8]. During the sampling phase, the input signal is stored on the capacitive-array DAC. During the bit cycling phase, the bottom plates of the capacitors are switched one after the other from V_{REFN} to V_{REFP} and the V_{DAC} converses to V_{VREFP}. Each technique has its own merits and flaws. For example, the "top plate sampling" technique does not requires any additional sampling switches but the *S/H* switches induce additional parasitic capacitances, reducing the input voltage range of the SAR ADC. On the other hand, the "bottom plate sampling" technique minimizes the effect of channel charge injection and improves the switches' linearity but it requires additional switches and non-overlapping clock circuit, increasing the design complexity and area.

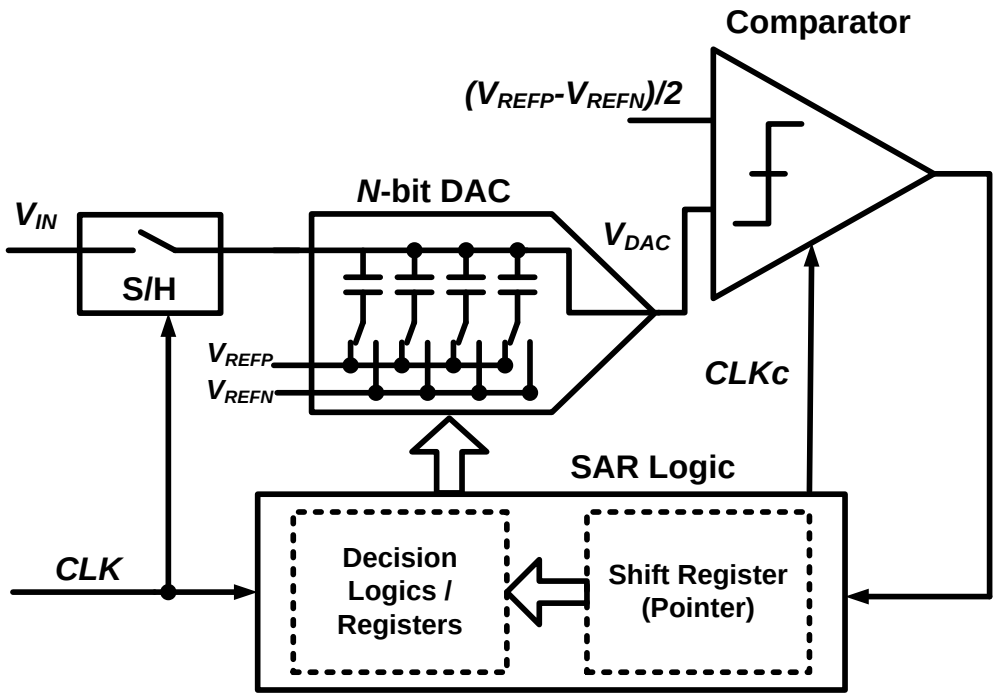

Figure 2.4: Schematic diagram of a N-bit conventional SAR ADC using the top plate sampling technique and without an explicit S/H circuit.

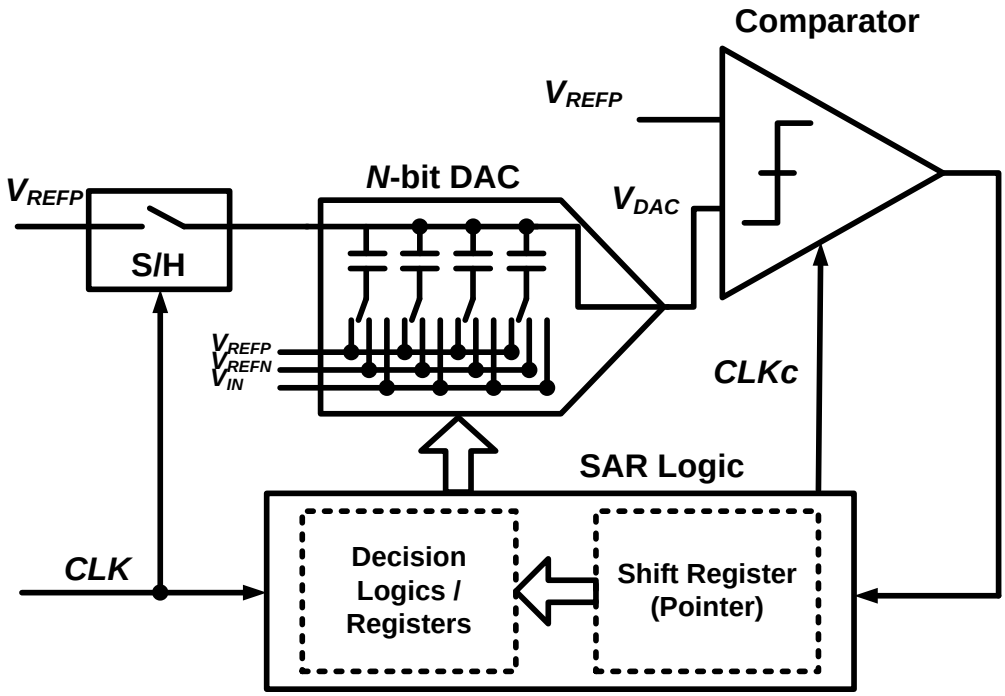

Figure 2.5: Schematic diagram of a N-bit conventional SAR ADC using the bottom plate sampling technique without an explicit S/H circuit.

2.2 Advanced techniques in SAR ADC architectures

Technology scaling continues to benefit the SAR ADCs due to the reduction of switching energy and minimum capacitor size, but the wafer cost for advanced CMOS prcoess (65-nm to 28-nm) continues to increase during the recent years, which is due to poor yield and high production cost [9, 10]. Therefore, in order to further improve the energy efficiency of the SAR ADCs, it is important to achieve architectural innovation that can be used in any technology. Recent research efforts in SAR ADCs have led to the numerous developments of different SAR ADC architectures, which improve the sampling rate and energy efficiency. A deeper understanding of these advanced SAR ADC architectures is necessary. The key techniques will be discussed in the following sections and a comprehensive summary of all the reported state-of-the-art SAR ADC architectures from *IEEE ISSCC* and *VLSI* are listed in Appendix A.

2.2.1 Asynchronous SAR ADCs

In the design of a high speed SAR ADC, a phase-locked loop is needed to provide the high frequency clock but it increases the design complexity and hardware overhead. An asynchronous system provides a convenient solution by generating the fast clock internally through control signal and comparator's latching time [11–23]. Thus, the sampling rate is equal to the clock rate and it does not need any additional phase-locked loop circuit. However, one of the greatest challenge is to reduce the risk of metastability in the asynchronous SAR ADC [24]. The on-going research is to design a more robust asynchronous logic and metastable detector to address this issue.

2.2.2 Pipelined-SAR ADCs

The traditional pipelined ADCs can easily achieve high sampling rate but it dissipates considerable amount of power in the amplifiers and require complex calibration schemes to achieve high accuracy. Furthermore, technology scaling has severely aggravated the design of the analog circuits. Recently research developments have demonstrated that the SAR ADCs [17, 23, 25, 26] are capable of achieving a higher energy efficiency than the traditional pipelined ADCs [27–31] for 10-to-12-bit and 50-to-100-MS/s specifications.

To take the advantage of the high-resolution property in the pipelined architecture, the two-stages pipelined-SAR ADCs were developed, which are potentially capable of achieving both high resolution and high conversion efficiency [32–36]. The first-stage of the architecture uses the capacitive-array DAC to perform residue amplification and the second stage uses the SAR ADC to replace the flash ADC in the conventional pipelined ADC and thus eliminating the need for more pipeline stages and lower the number of operational amplifiers.

2.2.3 Time-interleaved SAR ADCs

Another effective way to increase the ADC's sampling rate is to use the time-interleaving SAR ADCs [22, 37–42]. To further improve the resolution, the time-interleaved technique can be incorporated into pipelined-SAR architecture [43, 44]. However, the time-interleaving ADCs introduce channel mismatch problems (i.e., channel gain and offset, bandwidth mismatches) and the *FOM* of the ADC does not improve or might even deteriorates because more power is required by the complex calibration circuits that become necessary to reduce the error between channels. Therefore, developing a low-cost high-efficiency digital calibration technique is one of the popular topics for the high-speed SAR ADCs.

2.2.4 Multi-bit per cycle (flash) SAR ADCs

Comparing with the time-interleaved SAR ADC topology, another effective way to improve the ADC's sampling rate is to employ a multi-bit per cycle SAR ADC architecture [45]. He *et al* proposed a two-bit per cycle SAR ADC with interpolative resistive DACs and calibration logic to achieve an area of 0.028-mm^2 [46]. Later, Hong *et al* proposed a two-bit per cycle SAR ADC using reduced capacitive-array DACs and non-binary decision scheme to reduce the static power consumption and relax the requirement for DAC settling time [47]. Lien *et al* proposed an asynchronous subranged two-bit per cycle SAR ADC with coarse resistive DACs and fine capacitive-array DACs to reduce the number of switches and lower matching requirement of a resistive DAC [16].

This type of architecture inherently has no timing mismatch issue and thus, it is comparable to a time-interleaving SAR ADC. The ADC's sampling rate increases significantly from one to two-bit per cycle because the number of bit cycles diminishes by a factor of 2. However, more than two-bit per cycle is not recommended because a M-bit per cycle SAR ADC requires a minimum $2^M - 1$ number of comparators and DACs, which increases the area and the power consumption. In addition, the comparators' offset induces linearity errors, which degrades the ADC accuracy.

2.3 Type of DAC architecture

The DAC plays a pivotal role in the design of a SAR ADC. For a high resolution SAR ADC, the overall accuracy and linearity are primarily determined by its DAC's matching characteristics. These DACs can be broadly classified into four categories, namely switched-current DACs [48, 49], resistive R-2R DACs [50–54],

resistive-string DACs [46, 55] and capacitive-array DACs.

Early implementations used switched-current and resistive R-2R DACs, but such DACs consume static power and make them unsuitable for low power applications. Although these DACs can be made lower power by duty cycling, they require series switches to pass rail-to-rail voltages. This limits the amount of voltage scaling in the ADC, or requires a large number of bootstrapped switches [56], thus increasing power and area. Resistive-string DACs and capacitive-array DACs are the most commonly-used architectures in the current state-of-the-art SAR ADCs. A good understanding of these DACs is necessary to achieve architectural innovation in the SAR ADC and the following sections will discuss these architectures.

2.3.1 Resistive-string DAC

The simplest structure of the resistive DAC is the kelvin divider or resistive-string DAC. It has recently been reconsidered for the use of high-speed multi-bit/cycle SAR ADC architectures [16, 55]. A N-bit resistive-string DAC simply consists of 2^N equal resistors in series and 2^N switches, one between each node of the chain and the output. This architecture is simple, and is inherently monotonic. The output is taken from the appropriate tap by closing just one of the switches. Unlike the capacitive-array DAC, a resistive-string DAC is able to provide multiple reference voltages simultaneously, which is a much more suitable choice for the multi-bit/cycle SAR ADC architecture. However, one problem with this architecture is that the output is always connected to 2^N - 1 switches that are off and one switch that is on. For larger resolutions, a large parasitic capacitance appears at the output node, resulting in a slower sampling rate.

2.3.2 Conventional binary-weighted capacitive-array (CBW) DAC

Among all the DAC architectures, the capacitive-array DAC architecture is the most popular choice due to its zero quiescent current, which makes it appropriate for low-power applications. The charge-redistribution technique allows the *S/H* function to be realised by the capacitive-array DAC itself. The conventional way of implementing the capacitive-array DAC is the CBW DAC architecture, as shown in figure 2.6 and the value of each capacitor in the CBW DAC is given by

$$C_i = 2^{N-i}C_o, \qquad 1 \leq i \leq N. \tag{2.1}$$

As the resolution of the SAR ADC increases, the DAC requires a more stringent matching requirement for the unit capacitor (i.e. increases the area of the unit capacitor) and the total number of capacitors in the CBW DAC increase exponentially, thus increasing the area, the switching power consumption and the settling time in the DAC [57]. The capacitor matching and parasitic capacitances directly affect the non-linearity parameters of the ADC such as the INL and DNL. In this dissertation, a placement strategy is proposed to address the layout's mismatches, which will be discussed in Chapter 5.

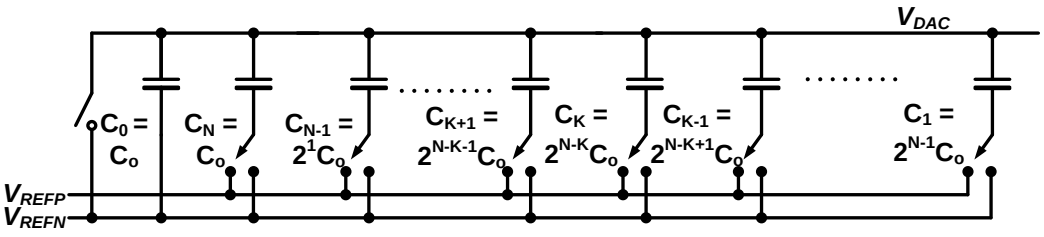

Figure 2.6: Schematic diagram of a CBW DAC.

2.3.3 Binary-weighted split capacitive-array with attenuation capacitor (BWA) DAC

Beside the layout's mismatches, the switching power consumption and the settling time in the CBW DAC have limited the efficiency and the maximum sampling rate of the SAR ADC. The BWA DAC architecture provides an alternative solution to alleviate the performance problems in the CBW DAC [11, 23, 45, 58–62]. As shown in figure 2.7, the BWA DAC is divided into a K-bit MSB sub-array and a (N-K)-bit LSB sub-array, where the value of each capacitor is given by

$$C_i = \begin{cases} 2^{K-i}C_o, & 1 \le i \le K, \\ 2^{N-i}C_o, & K+1 \le i \le N, \\ C_o, & i = 0, \end{cases}$$
$$C_M = \frac{2^{N-K}}{2^{N-K}-1}C_o, \tag{2.2}$$

where C_o is the capacitance of the unit capacitor, C_M is the attenuation capacitor and the total number of the capacitors are decreased by a factor of 2^K. The total capacitance in each sub-array is

$$C_{MSB,total} = \sum_{i=1}^{K} C_i = (2^K - 1)C_o,$$
$$C_{LSB,total} = C_o + \sum_{i=K+1}^{N} C_i = (2^{N-K})C_o. \tag{2.3}$$

The key advantage of such architectures is that the size of the total capacitance does not increase exponentially with the resolution compared to the CBW DAC, reducing the switching power consumption and improving the settling time. The key limitation lies in the parasitic capacitances that destroy the desired binary ratio of the capacitive-array DAC, degrading the ADC's linearity. DAC mismatch calibration

circuits can improve the linearity of the split capacitive-array DAC [63–65] but limited resolution range. Therefore, in this dissertation, two new types of split capacitive-array DAC architectures are proposed to reduce the area, the power consumption and improve the linearity compared to the CBW DAC and the BWA DAC. Further details will be discussed in Chapter 6.

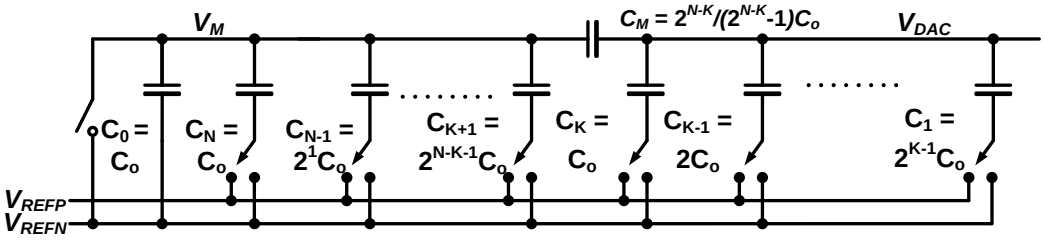

Figure 2.7: Schematic diagram of a BWA DAC.

2.3.4 Passive charge sharing capacitive-array DAC

The CBW DAC can be used for passive charge sharing (instead of charge redistribution) to sample the input signal and to perform the binary-scaled feedback during the bit-cycling phase. This type of architecture processes the sampled signal in the charge domain instead of voltage domain and it avoids the use of power-consuming reference buffers [12, 66]. The ADC uses tracking capacitors to pre-track the input signals in all clock phases except during the sampling phase. Therefore, it has sufficient time to track the input and no settling problems occur. In the sampling phase, the input is sampled on a capacitor and during the conversion cycle, the charge is added to or subtracted from the sampling capacitor until the result converges to zero. For differential inputs, the sampled signals converge together and the average processed voltages become lower than the charge-redistribution SAR ADC, posing a great challenge to overcome the thermal noise limit in charge sharing SAR ADCs. This architecture also requires a complex switching network to perform

the charge addition and substraction, which easily affects the linearity of the DAC. As such, it is more intuitive to develop a more energy efficient switching method for the CBW DAC rather than charge sharing DAC.

2.3.5 Non-binary (sub-radix-2) capacitive-array DAC

In the design of a high speed SAR ADC, the SAR ADC suffers from DAC settling issues and the incompletely settled DAC leads to a wrong decision. Thus, the DAC settling issue limits the sampling rate of the SAR ADC. A non-binary weighted capacitive-array can tolerate DAC settling error at the cost of increased design complexity and hardware overhead [67]. This technique generates more decision levels and reduces the effective input range by a factor smaller than 2 after each bit cycling phase. Therefore, even if a wrong decision happens during a conversion, as long as the remaining bit cycling operations are correct, it is possible to get a correct digital output code at the cost of extra bit cycles. There are several digital codes for each input voltage. By generating more decision levels, a certain range of errors do not have influence on the conversion result. However, it increases the design complexity and hardware overhead. It needs extra circuits, such as ROM and arithmetical unit to correct the digital output code and it is not easy to achieve matching layout for non-binary scaled capacitive-array. Liu *et al* first reported a binary-scaled error compensation method which results in less hardware and the capacitive-array is binary-scaled which is favoured in device matching for layout [26].

Chapter 3

Analytical Study Of The Capacitive-Array DAC's Switching Methods

3.1 Introduction

In the design of a low power SAR ADC, the switching power consumption in the capacitive-array DAC constitutes a significant part of the total power consumption and it even determines the lower bound on the ADC power consumption [5]. The switching power consumption depends on the total capacitance, input signal swing, and the switching method used. Therefore, it is instructive to have a thorough understanding of the switching power consumption for the various switching methods, such as charge-recycling switching [68], energy-saving switching [69], set-and-down switching [70], V_{CM} charge-recovery switching [23]. Furthermore, each method has a different impact on the comparator's dynamic offset, the DAC's linearity and the ADC's dynamic performance. For example, switching methods in [70–72] does not have a constant common-mode input throughout the entire

bit-cycling phase, thus causing the dynamic offset of the comparator to vary and degrading the ADC's linearity [73].

For ease of understanding, all calculations are demonstrated with a 3-bit differential SAR ADC. The differential architecture is preferred because it is less susceptible to supply and substrate noises and increases input signal swing with a good common-mode noise rejection.

3.2 Analysis of switching energy

The switching power consumption can be analyzed by calculating the total energy drawn from the reference voltages V_{REFP} and V_{CM} when switching the capacitive-array. An example of the switching power consumption of the reference voltage, V_{REFP}, due to the capacitor switching for an N-bit SAR ADC can be calculated

$$P_{REFP} = \frac{V_{REF}}{T_S} \sum_{i=1}^{N} Q_i \tag{3.1}$$

where V_{REF}, V_{REFP}, V_{CM} and V_{REFN} are related by

$$V_{REF} = V_{REFP} - V_{REFN}, \tag{3.2}$$

$$V_{CM} = 0.5 \times (V_{REFP} - V_{REFN}). \tag{3.3}$$

where T_S is the time period for the entire conversion phase. In most structures, one clock cycle is allocated for the sampling phase and N clock cycles for the bit cycling phase. Therefore, T_S = (N+1)/f_{CLK} where f_{CLK} is the clock frequency of the SAR ADC. Q_i can be calculated at each clock cycle and it can be generalized into the sampling to MSB transition phase and the bit cycling phase.

3.2.1 From sampling to MSB transition phase

The fundamental principle of sampling the input voltages, V_{IP} and V_{IN} to the capacitive-array DACs can be generally classified into the conventional charge-redistribution sampling technique (figure 3.1), the top plate sampling technique (figure 3.2) and the bottom plate sampling technique (figure 3.3) [8]. It is assumed that at the beginning of the bit-cycling phase, the input voltages have been fully sampled and that the sampling switches are open.

For the conventional charge-redistribution sampling technique (figure 3.1), the input voltages, V_{IP} and V_{IN} are sampled onto the bottom-plate of the capacitive-array DACs. During the transition to the bit-cycling phase, the total charge Q_1 that supplies from the reference voltages V_{REFP} and V_{CM} to the capacitive-array DACs is

$$\begin{aligned}
Q_1 &= \triangle\, Q[DACp_0 \rightarrow DACp_1] + \triangle\, Q[DACn_0 \rightarrow DACn_1] \\
&= C_3[(V_{REFP} - V_{DACP,1}) - (V_{IN} - V_{DACP,0})] \\
&+ \sum_{i=0}^{2} C_i[(V_{REFP} - V_{DACN,1}) - (V_{IP} - V_{DACN,0})] \\
&= 4C[(V_{REFP} - (V_{CM} - V_{IN} + V_{REF}/2)) - (V_{IN} - (V_{CM}))] \\
&+ 4C[(V_{REFP} - (V_{CM} - V_{IP} + V_{REF}/2)) - (V_{IP} - (V_{CM}))] \\
&= \underline{\underline{4CV_{REF}}}.
\end{aligned} \tag{3.4}$$

The amount of switching energy for N-bit SAR ADC is $2^{N-1}CV_{REF}^2$ and it is noted that there is no difference between the switching power consumptions for the SAR ADC with and without an explicit *S/H* circuit. This is due to the fact that although the initial charge is different, the voltage changes across the capacitors are the same for these two cases.

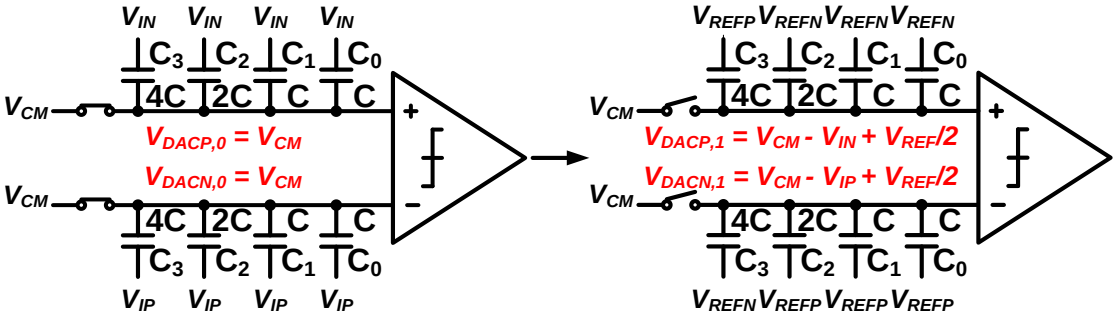

Figure 3.1: Conventional charge-redistribution sampling technique.

For the top-plate sampling technique (figure 3.2), the input voltages , V_{IP} and V_{IN} are sampled onto the top-plate of the capacitive-array DACs while the bottom-plate are reset to the reference voltage V_X. The total charge Q_1 that supplies from the reference voltage V_X to the capacitive-array DACs is

$$\begin{aligned} Q_1 &= \triangle Q[DACp_0 \rightarrow DACp_1] + \triangle Q[DACn_0 \rightarrow DACn_1] \\ &= \sum_{i=0}^{3} C_i[(V_X - V_{DACP,1}) - (V_X - V_{DACP,0})] \\ &+ \sum_{i=0}^{3} C_i[(V_X - V_{DACN,1}) - (V_X - V_{DACN,0})] \\ &= \underline{0}. \end{aligned} \tag{3.5}$$

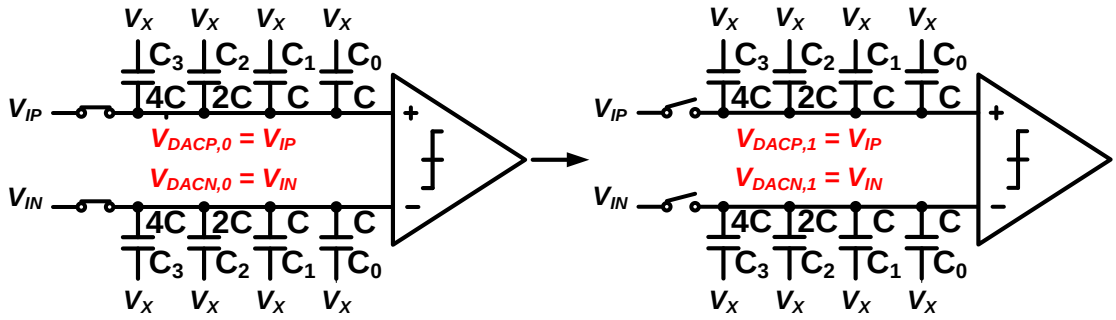

Figure 3.2: Top plate sampling technique.

Similarly, for the bottom-plate sampling technique (figure 3.3), the input voltages, V_{IP} and V_{IN} are sampled onto the bottom-plate of the capacitive-array DACs while the top-plate are reset to the reference voltage V_X. The total charge Q_1 that supplies from the reference voltage V_X to the capacitive-array DACs is

$$\begin{aligned} Q_1 &= \triangle\, Q[DACp_0 \rightarrow DACp_1] + \triangle\, Q[DACn_0 \rightarrow DACn_1] \\ &= \sum_{i=0}^{3} C_i[(V_Y - V_{DACP,1}) - (V_{IN} - V_{DACP,0})] \\ &+ \sum_{i=0}^{3} C_i[(V_Y - V_{DACN,1}) - (V_{IP} - V_{DACN,0})] \\ &= 4C[(V_Y - (V_X - V_{IN} + V_Y)) - (V_{IN} - V_X)] \\ &= 4C[(V_Y - (V_X - V_{IP} + V_Y)) - (V_{IP} - V_X)] \\ &= \underline{0}. \end{aligned} \tag{3.6}$$

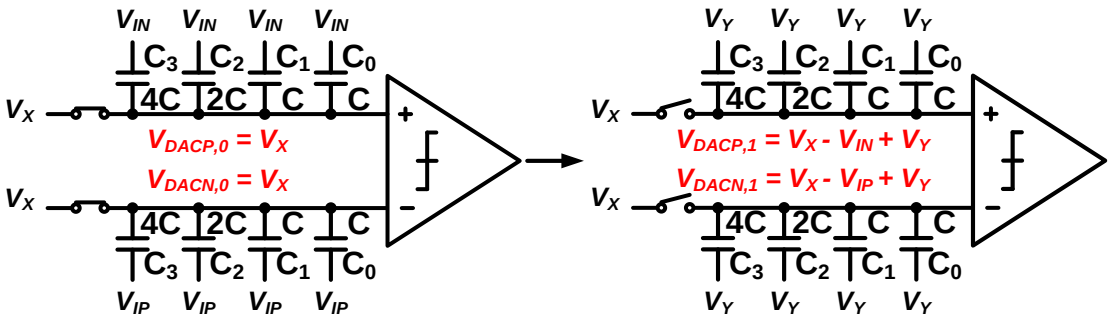

Figure 3.3: Bottom plate sampling technique.

The top-plate and bottom-plate sampling techniques do not drawn any energy from the reference voltages. The merits and flaws for implementing each technique have been discussed in Chapter 2.1.1.

3.2.2 Bit-cycling phase

At every period in the bit-cycling phase, the capacitive-array DAC goes through either "up" or "down" transition occurs. An "up" transition occurs when only a capacitor is required to be switched from one reference voltage to another. As shown in figure 3.4, the second largest capacitor, $2C$ is switched from V_{REFN} to V_{REFP}. A "down" transition occurs when the larger capacitor is switched to a lower voltage reference and the smaller capacitor is switched to a higher voltage reference. As shown in figure 3.5, the capacitor, $4C$ is switched down from V_{REFP} to V_{REFN} while the capacitor, $2C$ is switched up from V_{REFN} to V_{REFP} simultaneously. Intuitively, the switching energy for these two transitions are different.

In the "up" transition (figure 3.4), the total charge $Q_{2,UP}$ that supplies from the reference voltage V_{VREFP} to the capacitive-array DACs is

$$\begin{aligned}
Q_{2,UP} =& \triangle Q[DACp_1 \rightarrow DACp_2] + \triangle Q[DACn_0 \rightarrow DACn_1] \\
&= C_3[(V_{VREFP} - V_{DACP,2}) - (V_{VREFP} - V_{DACP,1})] \\
&+ C_2[(V_{VREFP} - V_{DACP,2}) - (V_{VREFN} - V_{DACP,1})] \\
&+ \sum_{i=0}^{1} C_i[(V_{VREFP} - V_{DACN,2}) - (V_{VREFP} - V_{DACN,1})] \\
&= 4C[(V_{VREFP} - 5V_{VREF}/4 + V_{VIN}) - (V_{VREFP} - V_{VREF} + V_{VIN})] \\
&+ 2C[(V_{VREFP} - 5V_{VREF}/4 + V_{VIN}) - (V_{VREFN} - V_{VREF} + V_{VIN})] \\
&+ 2C[(V_{VREFP} - 3V_{VREF}/4 + V_{VIP}) - (V_{VREFP} - V_{VREF} + V_{VIP})] \\
&= \underline{\underline{CV_{REF}}}. \qquad (3.7)
\end{aligned}$$

In the "down" transition (figure 3.5), the total charge $Q_{2,DOWN}$ that supplies from the reference voltage V_{VREFP} to the capacitive-array DACs is

$$\begin{aligned}
Q_{2,DOWN} =& \triangle Q[DACp_1 \rightarrow DACp_2] + \triangle Q[DACn_0 \rightarrow DACn_1] \\
&+ C_2[(V_{VREFP} - V_{DACP,2}) - (V_{VREFN} - V_{DACP,1})] \\
&+ C_3[(V_{VREFP} - V_{DACN,2}) - (V_{VREFN} - V_{DACN,1})] \\
&+ \sum_{i=0}^{1} C_i[(V_{VREFP} - V_{DACN,2}) - (V_{VREFP} - V_{DACN,1})] \\
&= 2C[(V_{VREFP} - 3V_{VREF}/4 + V_{VIN}) - (V_{VREFN} - V_{VREF} + V_{VIN})] \\
&+ 4C[(V_{VREFP} - 5V_{VREF}/4 + V_{VIP}) - (V_{VREFN} - V_{VREF} + V_{VIP})] \\
&+ 2C[(V_{VREFP} - 5V_{VREF}/4 + V_{VIP}) - (V_{VREFP} - V_{VREF} + V_{VIP})] \\
&= \underline{\underline{5CV_{REF}}}. \qquad (3.8)
\end{aligned}$$

The switching energy for the "down" transition is five times more than the switching energy for the "up" transition.

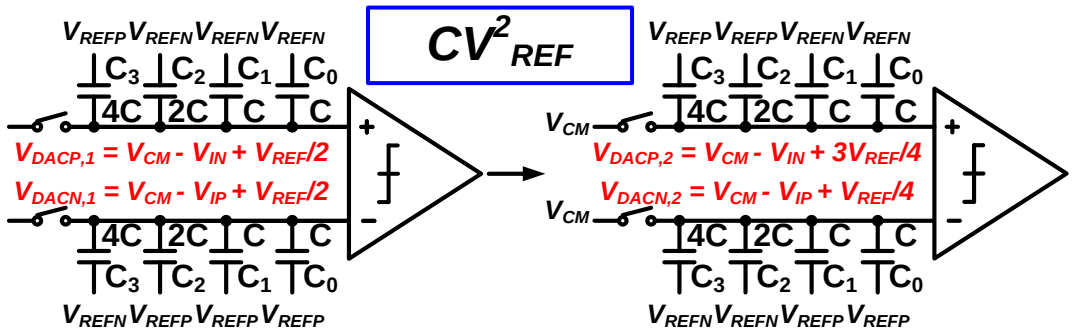

Figure 3.4: An example of an "up" transition in the capacitive-array DAC.

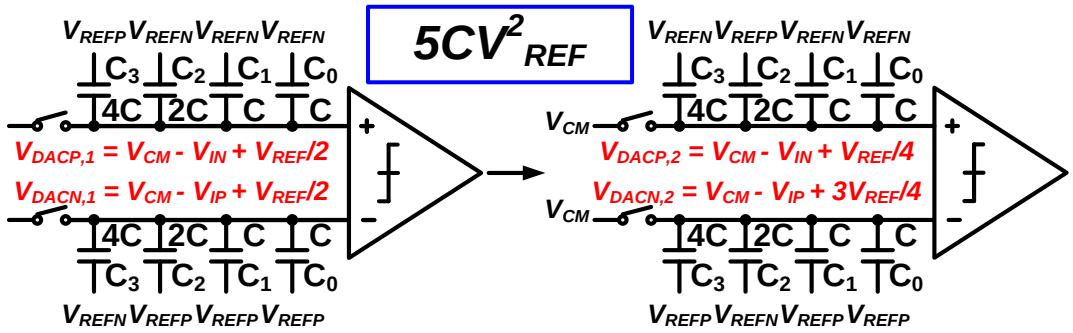

Figure 3.5: An example of a "down" transition in the capacitive-array DAC.

3.3 Examples of switching methods

3.3.1 Charge-redistribution switching method for the CBW DAC

From the earlier analyses in Section 3.2, the binary search procedure is simple and intuitive. However, it is not an energy efficient switching scheme, especially when the unsuccessful trials occur. An example of a 3-bit SAR ADC with the charge-redistribution switching method is shown in figure 3.7. The quantitative energy consumption of each switching phase is also shown in the figure 3.7.

The average switching energy for an N-bit SAR ADC using the switching method can be derived as:

$$E_{ave} = \sum_{i=1}^{N} (2^{N+1-2i})(2^i - 1)CV_{REF}^2, \tag{3.9}$$

For a 10-bit ADC, this switching method consumes 1363.33-CV_{REF}^2. As shown in figure 3.6, the efficient switching occurs when all the attempts are successful.

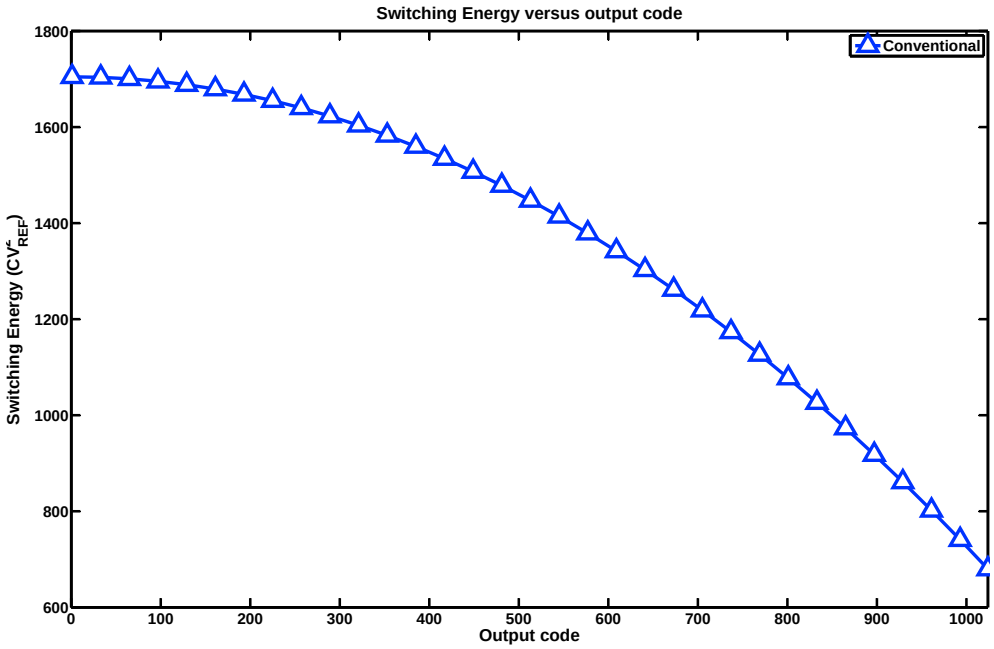

Figure 3.6: Switching energy versus output code

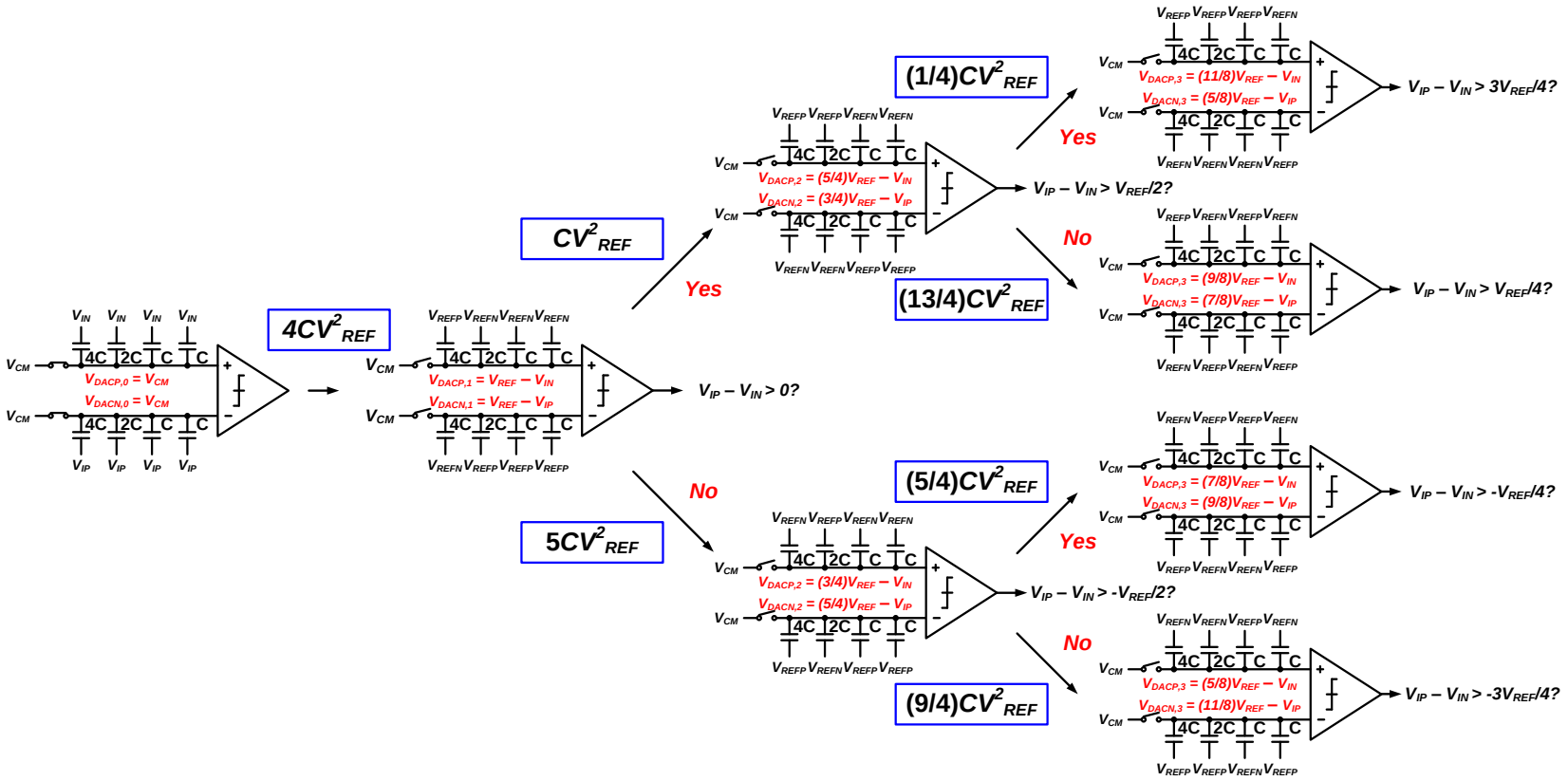

Figure 3.7: A 3-bit SAR ADC with the conventional switching method.

3.3.2 Charge-redistribution switching method for the BWA DAC

As discussed in Chapter 2.3.2, the BWA DAC architecture reduces the total number of the capacitors by a factor up to $2^{N/2+1}$. In order to calculate the overall power consumption of this architecture due to capacitor switching, the total charge that supplies to the capacitive-array DAC during the K-bit MSB and (N-K)-bit LSB conversions can be calculated separately and then substituted back in equation (3.1).

The total charge consumption during the first K-bit is the same as a K-bit binary-weighted capacitive DAC.

$$\sum_{i=1}^{K} Q_i = 2^K C_o V_{REF} \times \Big\{ \frac{5}{6} - \left(\frac{1}{2}\right)^K - \frac{1}{3}\left(\frac{1}{4}\right)^K - \frac{1}{2}\left(\sum_{i=1}^{K-1} \frac{D_i}{2^i}\right)^2 - \left(\frac{1}{2}\right)^K \sum_{i=1}^{K-1} \frac{D_i}{2^i} \Big\}, \tag{3.10}$$

where $D_1, D_2, \ldots, D_K$ are the binary outputs of the ADC.

To calculate the total charge consumption during the next $N-K$ clock cycles, one must consider that each of the K-bit MSB capacitors is connected to either V_{REFP} or V_{REFN} based on the value of $D_1, D_2, \ldots, D_K$ digital bits already determined during the previous clock cycles. The charge consumption in the following clock cycle is obtained from

$$Q_i = C_i V_{REF} + \left(C_i + \sum_{j=K+1}^{i-1} C_j D_j\right)(V_{M_{i-1}} - V_{M_i}) + \left(\sum_{j=1}^{K} C_j D_j\right)(V_{DAC_{i-1}} - V_{DAC_i}), \qquad K+1 \le i, \tag{3.11}$$

where V_{M_i} and V_{DAC_i} (node voltages annotated in figure 2.7) are given by

$$V_{M_i} = V_{REF} \times \left\{ \frac{C_i + \sum_{j=1}^{K} C_j D_j}{C_{MSB,total} + C_M || C_{LSB,total}} \times \frac{C_M}{C_M + C_{MSB,total}} + \frac{C_i + \sum_{j=K+1}^{i-1} C_j D_j}{C_{LSB,total} + C_M || C_{MSB,total}} \right\} \tag{3.12}$$

and

$$V_{DAC_i} = V_{REF} \times \left\{ \frac{\sum_{j=1}^{K} C_j D_j}{C_{MSB,total} + C_M || C_{LSB,total}} + \frac{C_i + \sum_{j=K+1}^{i-1} C_j D_j}{C_{LSB,total} + C_M || C_{MSB,total}} \times \frac{C_M}{C_M + C_{MSB,total}} \right\}, \tag{3.13}$$

substituting equations (3.12) and (3.13) in (3.11) and the total charge consumption can be obtained.

For a 10-bit ADC with MSB:LSB=5:5 segmentation, this switching method consumes only 87.29-CV_{REF}^2, achieving a 93.6% energy reduction.

3.3.3 Step-and-down switching method for the CBW DAC

An example of top-plate sampling technique is demonstrated in the step-and-down switching method. It was first reported for a 10-bit SAR ADC with a differential CBW DAC [70]. A detailed switching method is described as follow:

1. *Sampling Phase*: The differential input signals, V_{IP} and V_{IN}, are sampled through the top plate of the CBW DAC while the bottom plates of the capacitors are reset to V_{REFP}.
2. *Bit-cycling Phase*: The *S/H* sampling switches are turned off and the comparator directly performs the first comparison without switching any capacitor.
3. According to the comparator's output, the largest capacitor on the higher voltage potential side is switched to V_{REFN} and the other side remains unchanged.
4. Step 2 – 3 are repeated for the next N - 1 cycles until the output of the DAC converges towards V_{REFN}.

From the discussions in Section 3.2.1, during the sampling phase, the DAC does not draw any energy from the V_{REFP}. During each bit cycle, there is only one capacitor switched, which reduces both charge transfer in the DAC and the transitions of the control circuit and switch buffer, resulting in smaller power dissipation. This method uses one of the least number of switches and unit capacitors and it does not require upward transition. However, the common-mode voltage from the DAC gradually decreases from V_{CM} to V_{REFN}. Since the common-mode voltage is not fixed at any particular voltage, therefore the performance of the SAR ADC is limited by the comparator's signal-dependent dynamic offset. Furthermore, the harmonic distortions tend to be more severe through the use of top-plate sampling technique.

An example of a 3-bit SAR ADC with the step-and-down switching method is shown in figure 3.8. The average switching energy for an N-bit SAR ADC using the switching method can be derived as:

$$E_{ave} = \sum_{i=1}^{N-1} (2^{N-2-i}) C V_{REF}^2. \tag{3.14}$$

For a 10-bit ADC, this switching method consumes only 255.5-CV_{REF}^2, achieving a 81% energy reduction.

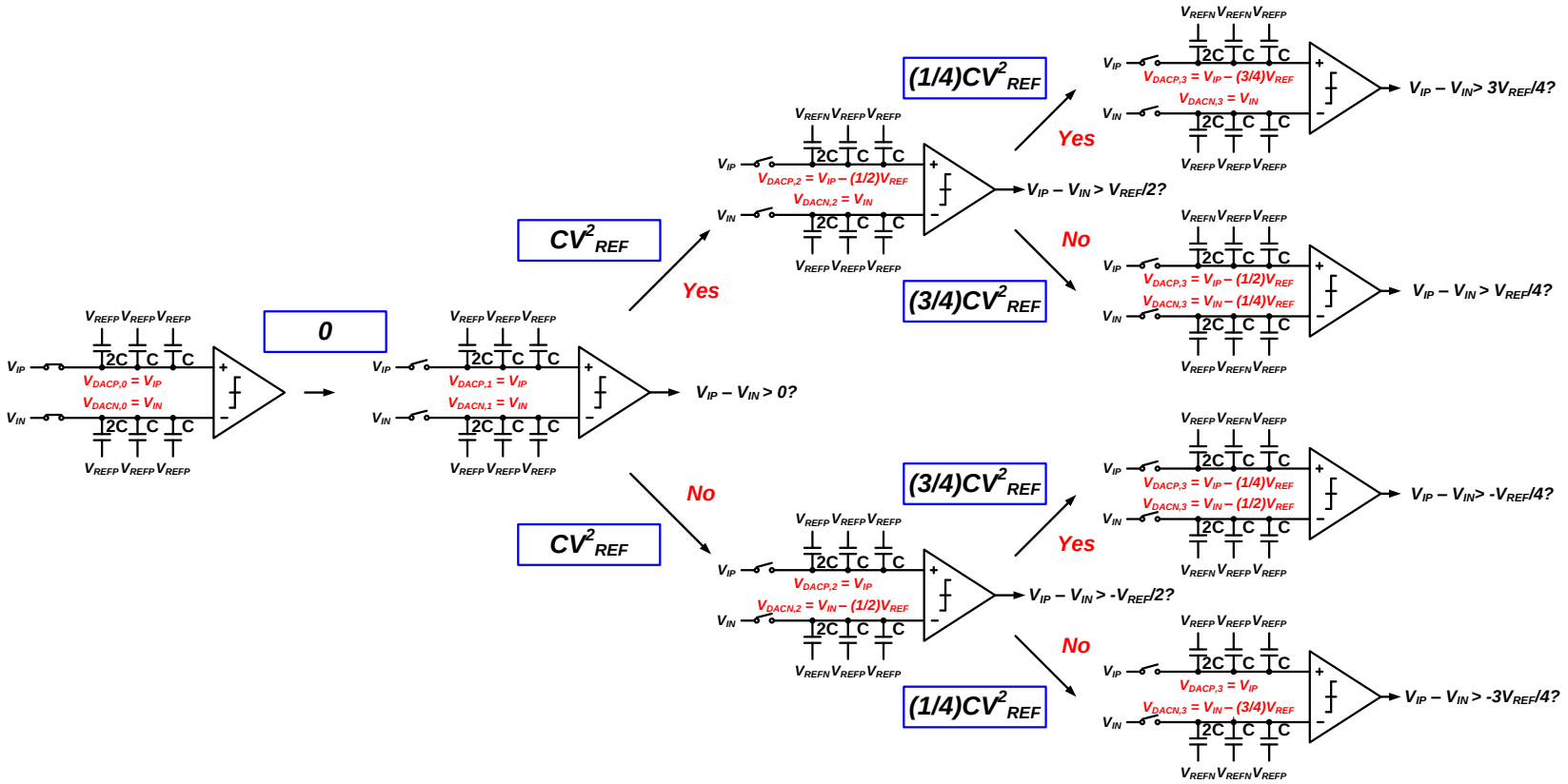

Figure 3.8: A 3-bit capacitive array with set-and-down switching method.

3.3.4 V_{CM}-based switching method for the CBW DAC

An example of top-plate sampling technique is demonstrated in the V_{CM}-based switching method. It operates in a similar way as the set-and-down switching method [23]. A detailed swithing method is described as follow:

1. *Sampling Phase*: The differential input signals, V_{IP} and V_{IN}, are sampled through the bottom plate of the CBW DAC while the top plates of the capacitors are reset to V_{CM}.
2. *Bit-cycling Phase*: The bottom plate of the CBW DAC are switched to V_{CM}. The top plate settles down to $2\times V_{CM}$ - V_{IP} and $2\times V_{CM}$ - V_{IN} and the comparator performs the first comparison.
3. According to the comparator's output, the largest capacitor on the higher voltage potential side is switched to V_{REFN} and the other side is switched to V_{REFP}.
4. Step 2 – 3 are repeated for the next N - 1 cycles until the output of the DAC converges towards V_{CM}.

Both switching methods reduce the size of the capacitive-array DAC and do not draw any energy from the reference voltages V_{REFP} and the V_{CM} during the sampling to MSB transition phase. The use of the bottom plate technique reduces any signal-dependent charge injection effect. During the bit-cycling phase, the energy used by the differential DACs is complementary. The charge-recovery effect corresponds to a compensation of the charge transferred from one DAC capacitive-array to the complementary capacitive-array and thus no energy is required from the V_{CM} during the bit-cycling phase. The "down" transition does not consume switching energy while the "up" transition in the complementary DAC would only require the capacitors to charge from V_{CM} to V_{REFP}, reducing the energy by 50% compared to the set-and-down switching method.

An example of a 3-bit SAR ADC with the V_{CM}-based switching method is shown in figure 3.9. The average switching energy for an N-bit SAR ADC using the switching method can be derived as:

$$E_{ave} = \sum_{i=1}^{N-1} (2^{N-2-2i})(2^i - 1)CV_{REF}^2. \tag{3.15}$$

For a 10-bit ADC, this switching method consumes only 170.17-CV_{REF}^2, achieving a 87.25% energy reduction.

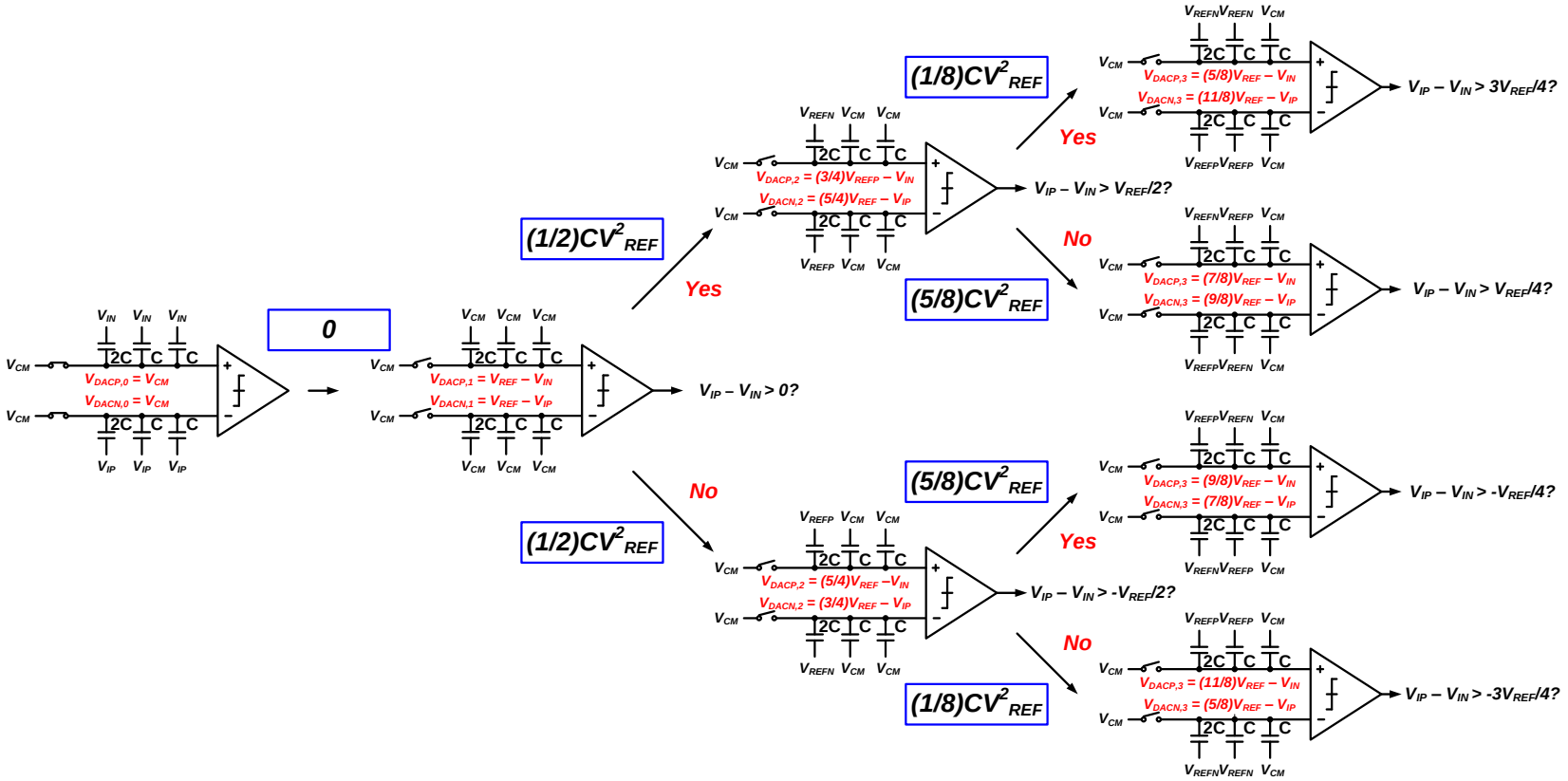

Figure 3.9: A 3-bit capacitive array with V_{CM}-based switching method.

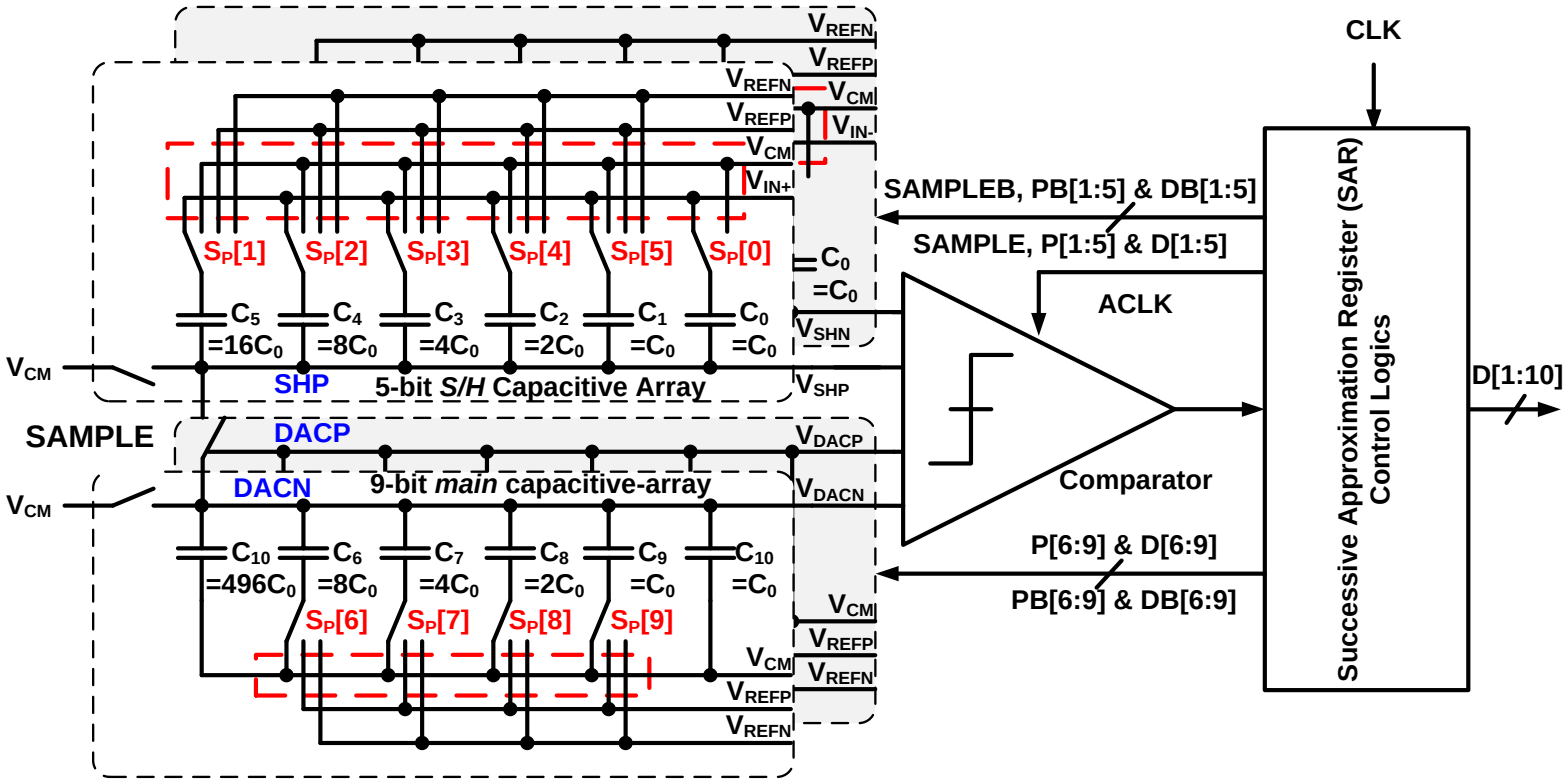

Figure 3.10: Schematic diagram SAR ADC architecture using the dual-capacitive-array DAC.

3.4 Charge-recovery switching method for the dual-capacitive-array DAC architecture

From the earlier analyses, the switching of capacitors for the first few MSB capacitors in the capacitive-array consume the most significant amount of energy and this energy is proportional to the corresponding changes in voltage level and the total capacitance to be switched. To circumvent the high switching energy, a SAR ADC with a dual-array capacitive-array (DCA) DAC is proposed [6]. This architecture samples the analog voltage signals and performs the first few MSB bit-cycling on a differential *S/H* capacitive-arrays while the remaining bits are obtained through the bit-cycling on a differential *N*-bit *DAC* capacitive-arrays. As such, the switching energy for the first few MSB capacitors is significantly smaller.

Figure 3.10 shows an example of a 10-bit SAR ADC using the proposed DCA DAC. The differential DCA DAC networks consist of a differential 5-bit *S/H* (*SHP* and *SHN*) and a 9-bit *main* (*DACP* and *DACN*) capacitive-arrays. The SAR control logic consists of shift registers, storage registers and DAC switching block, which control the DAC capacitive network to perform the binary search during the bit-cycling phases.

Each SAR conversion goes through four phases, i.e. sampling, (*B*+1)-bit coarse bit-cycling, (*N*-*B*-1)-bit fine bit-cycling and end-of-conversion. A detailed switching method is described as follow:

1. *Sampling Phase*: The differential input signals, V_{IN+} and V_{IN-}, are sampled through the bottom plate of the *S/H* capacitive-arrays while the top plates of the capacitors are reset to V_{CM}. Both plates of the *main* capacitive-arrays are also reset to V_{CM}.

2. *Coarse Bit-cycling Phase*: These switches are turned off and the bottom plate of the *S/H* capacitive-arrays are switched to V_{CM}. The *S/H* capacitive-array settles down to V_{SHP} = V_{CM} - V_{IP} and V_{SHN} = V_{CM} - V_{IN}. The *main* capacitive-array remains at V_{CM}. Then the comparator performs the first comparison.
3. If $V_{SHP} > V_{SHN}$, $S_P[1]$ goes to V_{REFN} and $S_N[1]$ goes to V_{REFP} while other switches remain connected to V_{CM}. V_{SHP} and V_{SHN} take the values of (V_{CM} - V_{IN+} - V_{CM}/2) and (V_{CM} - V_{IN-} + V_{CM}/2), respectively. If $V_{SHP} < V_{SHN}$, $S_P[1]$ goes to V_{REFP} and $S_N[1]$ goes to V_{REFN} while other switches remain connected to V_{CM}. V_{SHP} and V_{SHN} become (V_{CM} - V_{IN+} + V_{CM}/2) and (V_{CM} - V_{IN-} - V_{CM}/2), respectively.
4. Step 2 – 3 are repeated for the next B cycles until the output of the *S/H* capacitive-arrays converge towards V_{CM}.
5. *Fine Bit-cycling Phase*: For the remaining (N-B-1)-bits, the output voltages, V_{DACN} and V_{DACP} converge towards V_{SHP} and V_{SHN} respectively in a similar fashion as coarse resolutions but the switches $S_P[N-1:B+1]$ and $S_N[N-1:B+1]$ are switched to opposite reference voltages.

The proposed switching method is summarized in the flow chart as shown in figure 3.11 and an example of voltage waveforms are illustrated in figure 3.12.

Due to the charge-recovery effect in a differential structure, the conversion process corresponds to a compensation of the charge transferred to *SHP* or *DACP* capacitive-arrays with charge coming from *SHN* or *DACN* capacitive-arrays and vice-versa [23]. Hence, no charge flows through the common mode terminal. One of the key advantages of the proposed scheme is that the common-mode voltage of the reference signals is fixed. This minimizes any signal-dependent offset caused by the variation of the input common-mode voltage. Secondly, this switching scheme uses bottom-plate sampling instead of top-plate sampling and thus, the *main* capacitive

arrays are insensitive to any parasitic effects. Lastly, this approach only requires (N-1)-bit array for *main* capacitive-array.

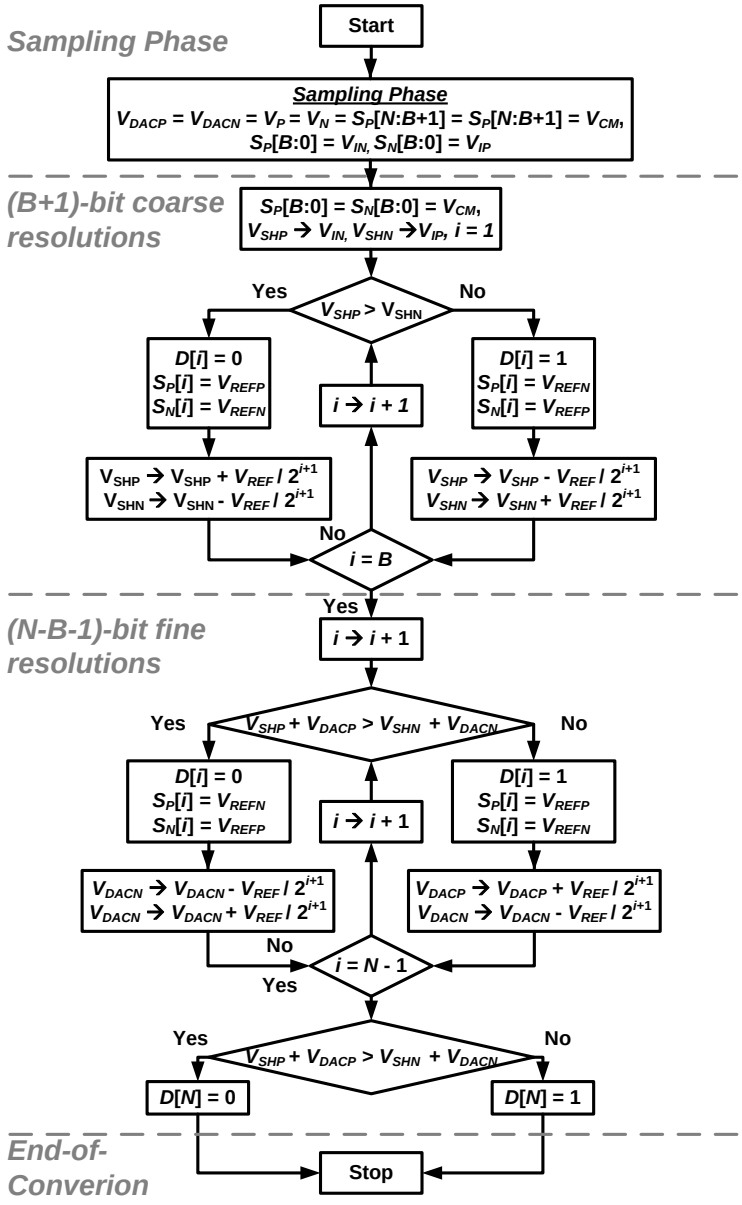

Figure 3.11: Flow chart of the proposed switching scheme.

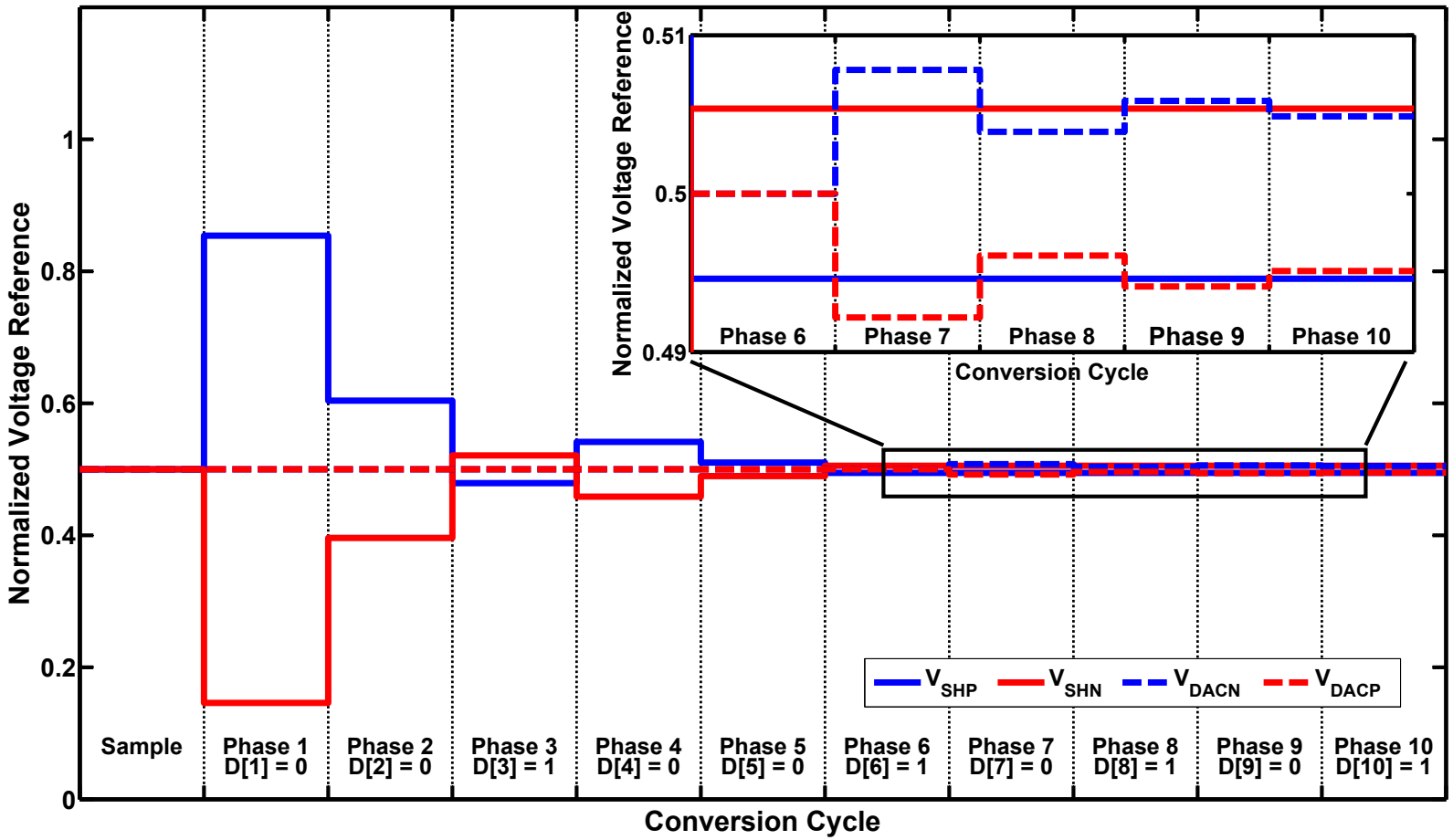

Figure 3.12: Waveforms of signals V_{SHP}, V_{SHN}, V_{DACN} *and* V_{DACP}.

The behavioral simulation assumes equal unit capacitors for the differential capacitive array(s) in different architectures. The average switching energy, E_{avg} for conventional charge-redistribution switching scheme is 1365.3-CV_{REF}^2 while E_{avg} for the proposed switching scheme is 17.59-CV_{REF}^2. Hence, the proposed scheme achieves 98.7% reduction in switching energy. In addition, the standard deviation of this switching energy according to output code is only 2.3-CV_{REF}^2. The charge-recycling switching [68], set-and-down [70], V_{CM} charge-recovery [23] and tri-level [71] switching achieved 37.5% (E_{avg} = 852.3-CV_{REF}^2), 81% (E_{avg} = 255.50-CV_{REF}^2), 87.5% (E_{avg} = 170.17-CV_{REF}^2) and 96.89% (E_{avg} = 42.41-CV_{REF}^2) reduction, respectively.

Figure 3.13 shows a comparison of switching energy for the various switching schemes versus the output code [23, 70, 71]. Table 3.1 summarizes the features of various switching schemes. It is clear that the proposed scheme achieves significant improvement compared to existing ones. With the additional switches for V_{CM} sampling, the proposed ADC architecture is able to reduce the total number of capacitors in the DAC capacitive arrays by 47% compared to the conventional design, which in turn results in an area-efficient SAR ADC.

Table 3.1: Comparison of various switching schemes

Switching Procedure	Avg. Switching Energy (CV_{ref}^2)	Energy Saving	Area Reduction
CBW	1363.33	Reference	Reference
BWA	87.29	93.6%	93.75%
V_{CM}-based [23]	170.17	87.25%	50%
Set-and-down [70]	255.50	81.26%	50%
Tri-level [71]	42.41	96.89%	75%
This work	17.59	98.7%	46.9%

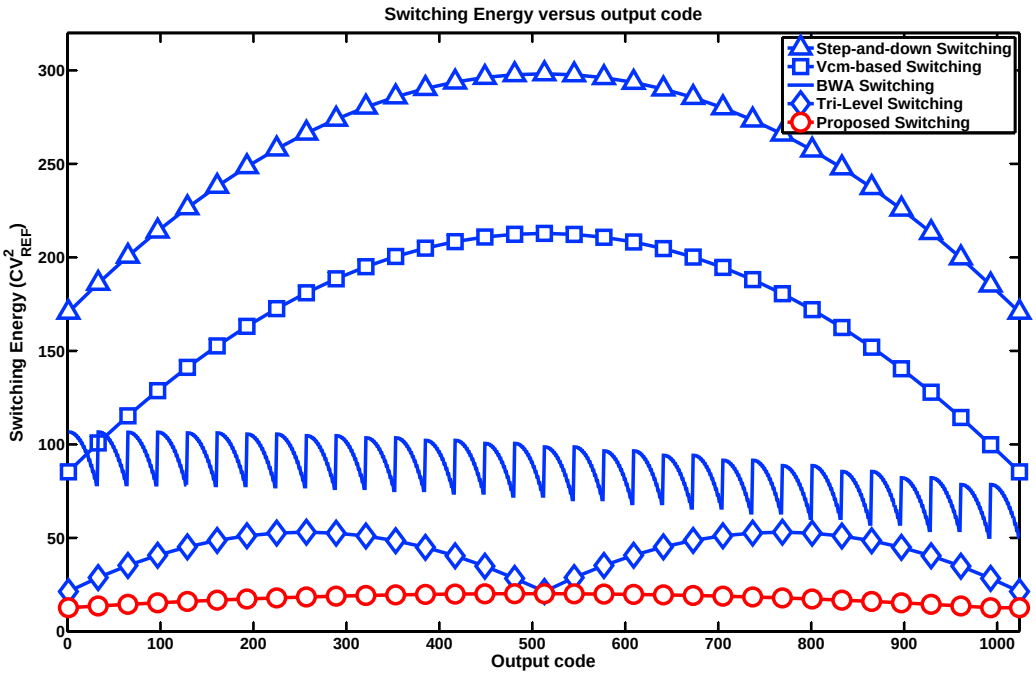

Figure 3.13: Switching energy versus output code

3.5 Summary

A detail analysis of basic binary switching scheme is presented, which is followed by a review of different type of the state-of-the-art switching methods. Then, a charge-recovery switching method is proposed for the dual-capacitive-arrays architecture. The experimental results show that the proposed switching method achieves the lowest switching energy among existing switching schemes [6].

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Chapter 4

Dual-Channel, Time-Interleaved, Reconfigurable Resolution SAR ADC

4.1 Introduction

The recent introduction of Internet-of-Things led to the growing interest in the miniaturized sensors, especially on wearable wireless sensors for health-care applications [74]. These sensors have to deal with different types of signal at limited power budget and low cost [75]. A typical sensor interface consists of a band-limited operational amplifier and an analog-to-digital converter (ADC). Particularly, the ADCs play the utmost important role, providing an interface bridging analog signal to micro-controller unit. Its performance and flexibility are critical, which requires the ADC to digitize multiple types of analog signal, adapts to varying bandwidth and dynamic range requirements while maintaining energy-efficiency and area-efficiency. In other words, configurable resolution and bandwidth are necessary to maximize the energy-efficient and provide an area saving for a broad range of applications.

Successive-approximation-register (SAR) ADC is a widely adopted ADC architecture for sensor applications due to its manageable design complexity and highly energy efficient architecture [9]. Earlier configurable SAR ADC designs provide either adjustable resolutions [76, 77] or scalable sampling rate [14]. The configurable resolution (7-to-10 bits) and scalable sampling rate (up to 4 MS/s) SAR ADC was introduced in [15], in which the custom-designed digital-to-analog converter (DAC) with sub-fF unit capacitor reduces the switching power significantly. However, it requires an accurate extraction tool, a more careful layout and an additional calibration circuits to correct the linearity. The parasitic capacitances of the DAC attenuate the maximum input dynamic range of the ADC. A 5-to-10-bit resolution SAR ADC with voltage scaling from 0.4-to-1.0-V and sampling rate scaling up to 2-MS/s at 1.0-V was presented in [78]. The ADC uses split-capacitive-array DACs to achieve rail-to-rail input dynamic range while reducing the input load capacitances and switching energy in the lower resolution modes, but the code dependent error increases at the lower resolution modes, thus degrading the linearity of the ADC.

In addition to the reconfigurability challenges, in the multi-channel system, a common strategy in minimizing power and area is to share a single ADC among many sensors and amplifiers using the sequential sampling (time-multiplexing) method. Additional buffers and analog multiplexing circuitry are required to maintain signal linearity to the ADC, which incur additional power. Operating at low supply voltages further exacerbates the design issues in analog circuitry and increases the settling time of the capacitive-array DAC. In contrast, a dedicated ADC can be used to interface with an individual sensor but it is typically impractical because of severe area overhead with the capacitive-array DAC.

In this paper, several key techniques are presented in the proposed dual-channel,

time-multiplexing, 4-to-10-bit reconfigurable SAR ADC, to address issues in the existing designs. First, the ADC operates at a supply voltage of 0.6-V to achieve an optimal energy-efficiency across all the resolution modes. Under the 10-bit resolution mode operation, the ADC is able to operate at a maximum sampling rate of 250-kS/s per channel to accommodate high bandwidth and multi-channel requirements. Second, a resolution-reconfigurable dual-capacitive-arrays DAC with an energy-efficient switching charge-recovery switching method reduces the switching power consumption and minimizes the input common-mode variation so that the comparator's dynamic offset is minimized. Third, a dual-channel time-interleaved SAR ADC with dedicated sample-and-hold (S/H) capacitive-array per channel, relaxes the settling time requirement, cuts down the number of analog multiplexing circuitry by $2\times$ and reduces the total area by sharing a differential 9-bit capacitive-array DAC. As the multiplexing is performed in the digital domain, the power consumption per channel as well as the system complexity could be reduced. To further optimize the circuit, custom-designed switches for the *S/H* and *main* capacitive-arrays, configurable resolutions SAR logics and a single comparator are proposed and shared for both input channels. The prototype has achieved an optimal power efficiency of 24-fJ/conversion-step and occupies an active area of 0.086-mm^2 per channel.

4.2 System Architecture

This section describes the details of the proposed dual-channel SAR ADC architecture with the energy-efficient charge-recovery switching method and presents the trade-offs and techniques used to achieve resolution reconfigurability in the ADC.

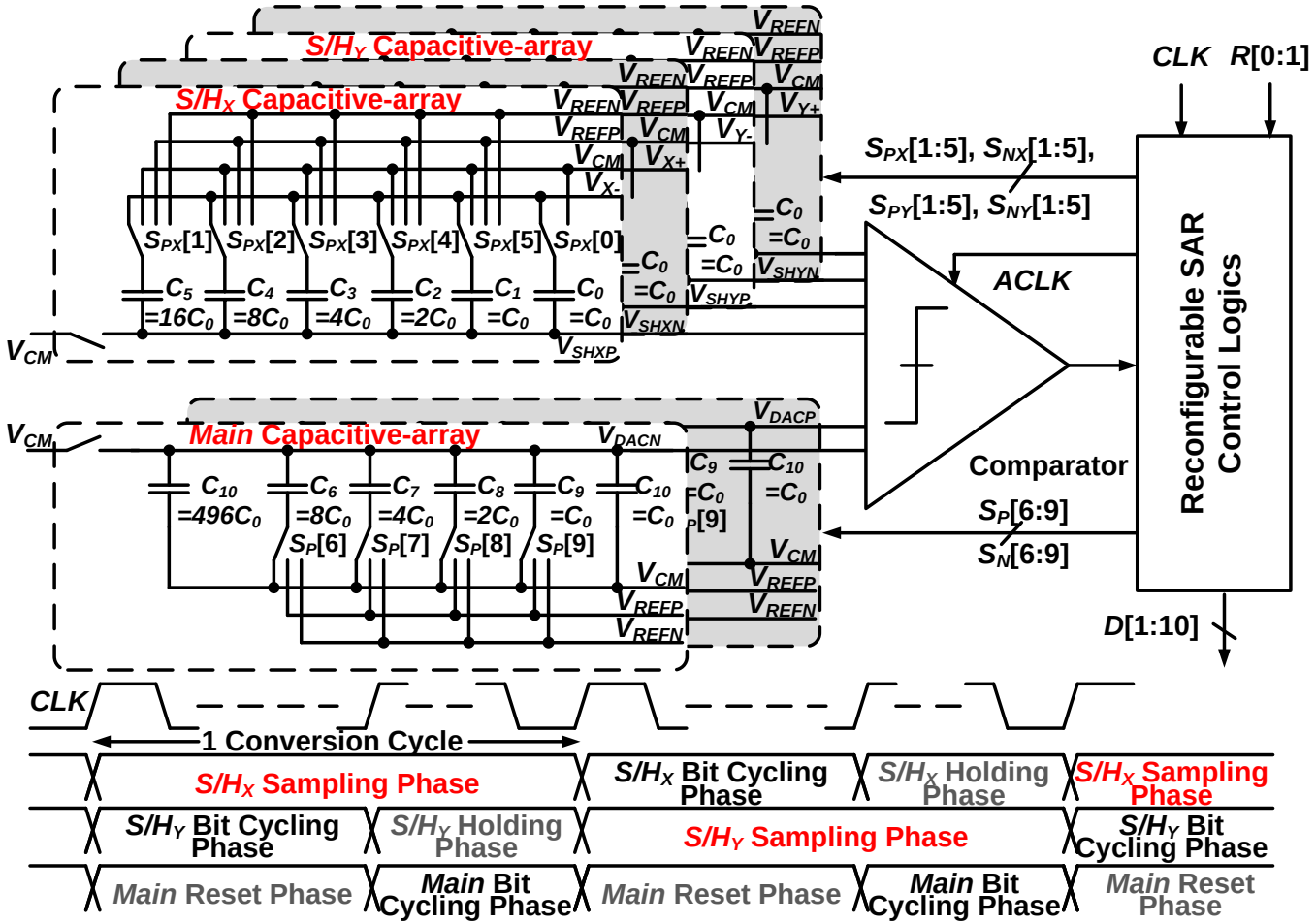


Figure 4.1: The proposed resolution-reconfigurable SAR ADC architecture and the ADC conversion plan.

4.2.1 ADC architecture

Figure 4.1 shows the architecture of the proposed dual-channel 4-to-10-bit resolution-reconfigurable SAR ADC. The fundamental building blocks consist of a multiple-input dynamic comparator, differential 5-bit *S/H* capacitive-arrays for each input channel, namely S/H_X and S/H_Y, differential 9-bit *main* capacitive-arrays and fully custom designed reconfigurable SAR control logics. Note that the proposed charge-recovery switching method requires a differential 9-bit DAC instead of a differential 10-bit DAC for achieving 10-bit resolution. To achieve better accuracy at a supply voltage of 0.6-V, a differential architecture is chosen to suppress the power and substrate noise and to improve common-mode rejection. The conversion plan of the dual-channel, time-interleaved SAR ADC is shown in figure 4.1 and the conversion cycle for each channel begins with *S/H* sampling phase, *S/H* bit-cycling phase and *main* bit-cycling phase.

Let us consider the conversion cycle for the channel S/H_X. During the S/H_X sampling phase, the ADC samples differential input signals on bottom plates of the S/H_X capacitive arrays while the top plates of the S/H_X, S/H_Y and DAC capacitive arrays reset to V_{CM}. Next, the ADC turns off these switches and the bottom-plates of the S/H_X capacitive arrays are switched to the V_{CM}, resulting in the equivalent output voltages

$$\begin{aligned} V_{SHXP} &= V_{CM} - V_{X-}, \\ V_{SHXN} &= V_{CM} - V_{X+}, \\ V_{SHYP} &= V_{SHYN} = V_{CM}, \\ V_{DACP} &= V_{DACN} = V_{CM}. \end{aligned} \tag{4.1}$$

If $V_{SHXP} > V_{SHXN}$, $S_{PX}[1]$ goes to V_{REFN} and $S_{NX}[1]$ goes to V_{REFP} while other switches remain connected to V_{CM}. V_{SHXP} and V_{SHXN} take the values of ($V_{CM} - V_{X-} - V_{CM}/2$) and ($V_{CM} - V_{X+} + V_{CM}/2$), respectively. If $V_{SHXP} < V_{SHXN}$, $S_{PX}[1]$ goes to V_{REFP} and $S_{NX}[1]$ goes to V_{REFN} while other switches remain connected to V_{CM}. V_{SHXP} and V_{SHXN} become ($V_{CM} - V_{IN+} + V_{CM}/2$) and ($V_{CM} - V_{IN-} - V_{CM}/2$), respectively. Consequently, the *S/H*$_X$ bit-cycling is performed for the next B cycles and the output voltages, V_{SHXP} and V_{SHXP} converge towards V_{CM}. For the remaining (N-B-1)-bit, the output voltages, V_{DACP} and V_{DACN} converge towards V_{SHXN} and V_{SHXP} in a similar fashion as coarse resolutions but the switches, $S_{XP}[B+1:N-1]$ and $S_{XN}[B+1:N-1]$ are switched to opposite reference voltages. The switching mechanism is summarized into a flow chart as described in figure 3.11, where N and B are the resolution of the SAR ADC and the *S/H* capacitive-array, respectively. Figure 3.12 provides an illustration of the waveforms of signals V_{SHN}, V_{SHP}, V_{DACP} and V_{DACN}, where N and B are chosen to be 10 and 5, respectively.

To realise the dual-channel ADC, the *S/H*$_X$ and *S/H*$_Y$ capacitive arrays alternate between the bit-cycling phase and the sampling phase while the DAC capacitive arrays alternate the holding phase and the bit-cycling phase. Thus, this architecture would only need one set of N-1-bit differential DAC capacitive arrays to realise the dual-channel ADC. This provides an area reduction compared to the conventional approach without any additional comparator.

4.2.2 Energy-efficient charge-recovery switching energy

In order to compare the energy-efficiency of our proposed switching method with various state-of-the-art switching methods [23, 70, 71], the simulation results for various switching methods are shown in figure 3.13. For a fair comparison, the behavioral simulation assumes the unit capacitor used are the same for a 10-bit differential SAR ADC architecture. Results are normalized to units of CV_{ref}^2. The average switching energy, E_{avg} for the conventional charge-redistribution switching method is 1365.3-CV_{ref}^2 while E_{avg} for the proposed switching method is 17.59-CV_{ref}^2, which amounts to a reduction of 98.7% or 77.5$\times$ in the switching energy. When the conventional charge-redistribution switching method is compared with other state-of-the-art switching methods, the set-and-down [70], the V_{CM} charge-recovery [23] and the tri-level [71] switching have achieved a reduction of 81% (E_{avg} = 255.50-CV_{ref}^2), 87.5% (E_{avg} = 170.17-CV_{ref}^2) and 96.89% (E_{avg} = 42.41-CV_{ref}^2), respectively. It can be seen that the switching energy of the proposed method is among the highest energy-efficient reported.

4.2.3 Resolution reconfigurability in DAC architecture

To minimise the switching energy at any given bit resolution, three switching methods were reported to scale the DAC resolution by bit-cycling the desired number of bits in a N-bit DAC [76–78]. The first method, *MTD1*, is to start the bit-cycling at the most-significant-bit (MSB) capacitor and stop at the desired resolution [76, 77]. This enables a fixed dynamic range across all resolution modes but it is a very energy-inefficient method as most of the switching power is consumed during the bit-cycling of the first few MSB capacitors. The second method, *MTD2*, is to start somewhere in the middle of the array and always bit-cycle to the least-significant-bit (LSB) capacitor. The unused MSB capacitors attenuate the DAC output which reduces the input voltage range significantly. The third method, *MTD3*, is to insert switches between the top plates of the capacitors so that the inactive capacitors are not connected to the DAC [78]. The capacitive parasitics and non-linearity effects in these switches affect the overall linearity of DAC output. Although the use of boosted minimum-size switches help to alleviate these issues, there will be penalties in silicon area, power dissipation and design complexity.

Our approach is to improvise our switching method in the dual-capacitive-arrays architecture to achieve the resolution reconfigurability and to circumvent the existing trade-offs. For the resolution modes less than 6-bit, the the output voltages, V_{DACP} and V_{DACN} remain at V_{CM} while the S/H_X and S/H_Y capacitive arrays alternate between bit-cycling and sampling phases. The bit-cycling starts from C_5 in *S/H* capacitive-arrays and stop at the desired resolution. For the resolution beyond 6-bit, the first 6-bit MSB are derived from the *S/H* capacitive-arrays while the remaining bits are derived from the *main* capacitive-arrays. In the *main* capacitive-arrays, the bit-cycling starts from C_6 and stop at the desired resolution. This approach allows rail-to-rail input signal range across all resolution modes without affecting

the linearity at lower resolution modes.

In this work, we have chosen B to be 5 so that the MSB capacitor of the *S/H* capacitive-array is 32× smaller than the MSB capacitor of the conventional 10-bit capacitive-array DAC and thus improving the energy-efficiency significantly. Figure 4.2 shows the average switching energy across 4-to-10-bit resolution modes for each of the switching methods, showing that our switching method has achieved the best energy-efficient compared with the other methods. With the choice of $B = 5$, our method achieves a 3.6-to-77.5× and 3.3-to-6.5× reduction in switching energy compared to the conventional charge-redistribution switching method using 4-bit to 10-bit DACs and *MTD3* [78], respectively.

It is noted that the matching requirements for the *S/H* capacitive-arrays has to be the same or similar to that of the *main* capacitive-arrays. As such, the arrangement and the size of the unit capacitors in the *S/H* capacitive-arrays are very important. The arrangement of the unit capacitors in capacitive arrays is derived from our placement methodology described in Chapter 5. This is to achieve the highest possible degree of dispersion to mitigate mismatches in the DAC architecture. To meet the matching requirements for dual-capacitive arrays architecture, a unit capacitor, C_0, of 55-fF is used. However, the total sampling capacitance of the *S/H* capacitor network is only 1.76-pF.

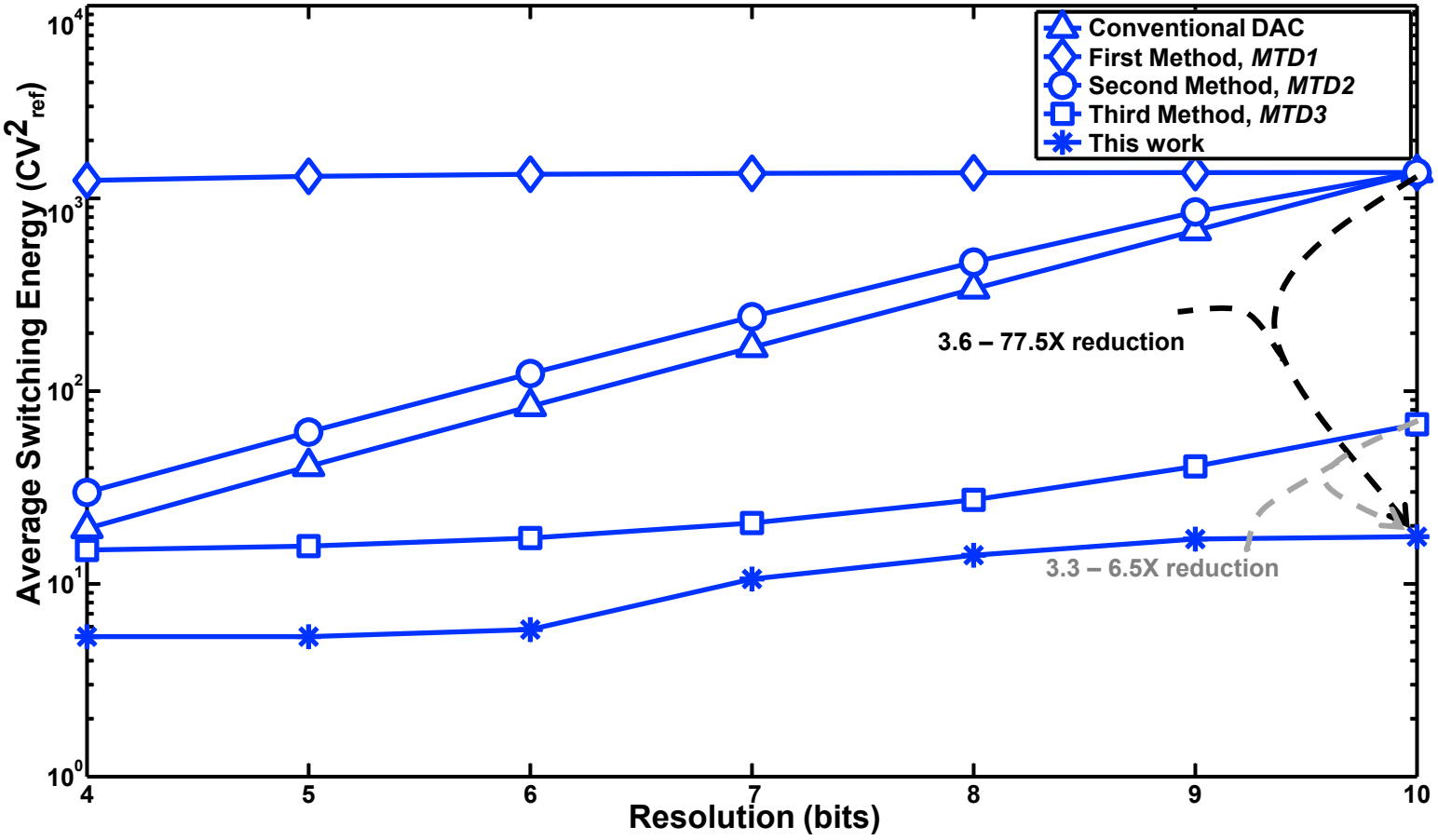


Figure 4.2: Energy savings across resolution of the proposed switching scheme compared to the conventional scheme.

4.3 Implementation of Key Building Blocks

This section describes the important building blocks, such as a reconfigurable SAR control logic, a switching network and a multiple-input comparator, which simplify the design of a dual-channel resolution-reconfigurable SAR ADC. The design objectives and our implementation strategies for each building block will be presented in the following sections.

4.3.1 Reconfigurable SAR Control Logic

Figure 4.3 shows the block diagram of our proposed reconfigurable SAR control logic. The basic requirement of the control logic consists of a clock generator, a resolution decoder logic and a SAR control logic. Generally, the registers in the control logic consume significant power and evidences from previous works have shown that the digital power consumption has constituted more than 50% of total power consumption [13, 17, 18, 61, 79, 80]. Therefore, we propose three circuit techniques to simplify the SAR control logic block and the switches. First, we propose to use our custom-designed latch and register for the sequential and storage registers, respectively. This helps to achieve a higher energy-efficiency as the additional delay margin can be used for trading power at a lower supply voltage. Second, we adopt a dual-edge triggered clocking strategy in these circuits to utilize all the clock edges and improves the overall operating speed. Third, we propose an embedded resolution control logic in the sequential register to simplify the complexity of the reconfigurable SAR control logic.

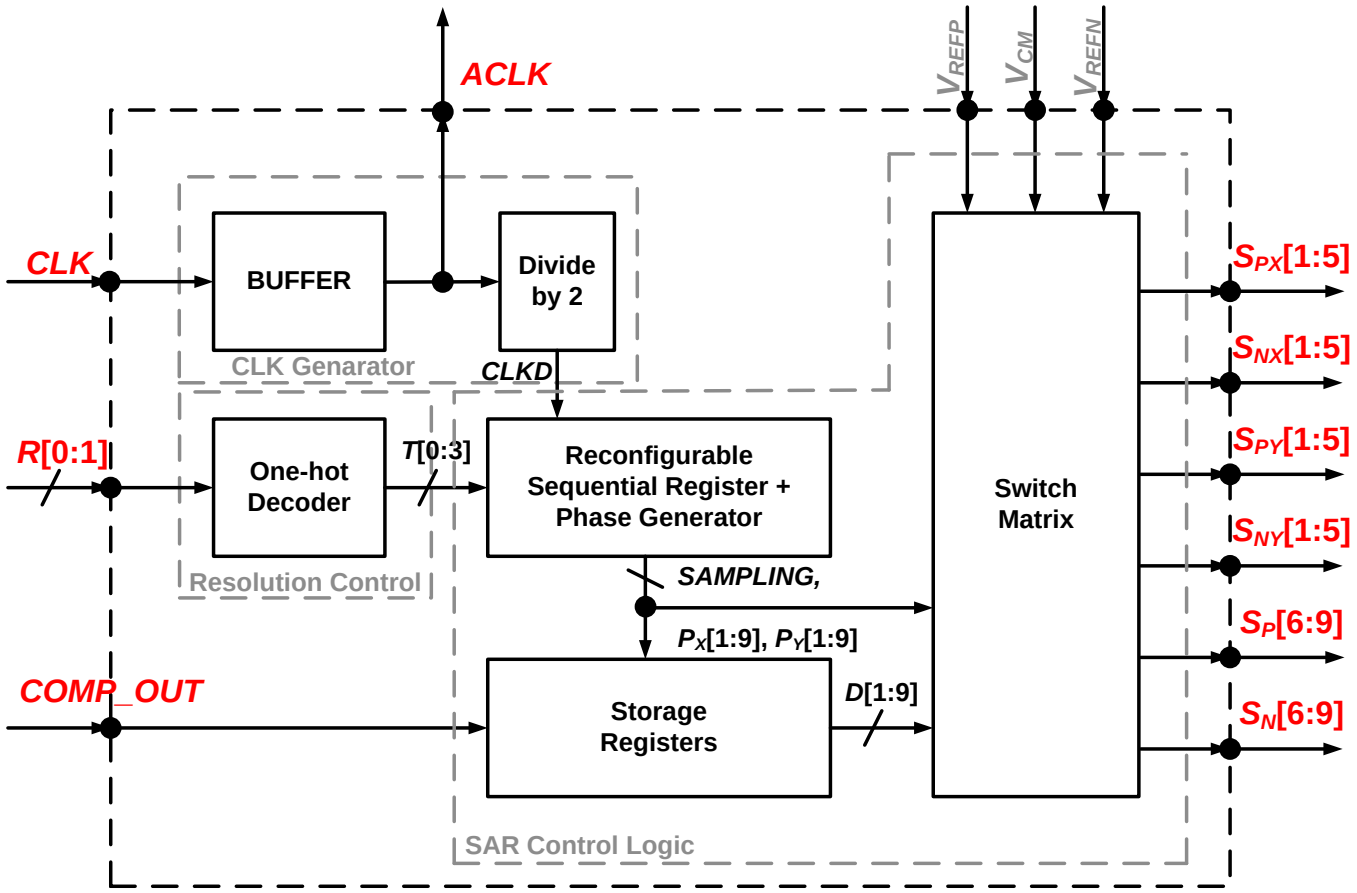
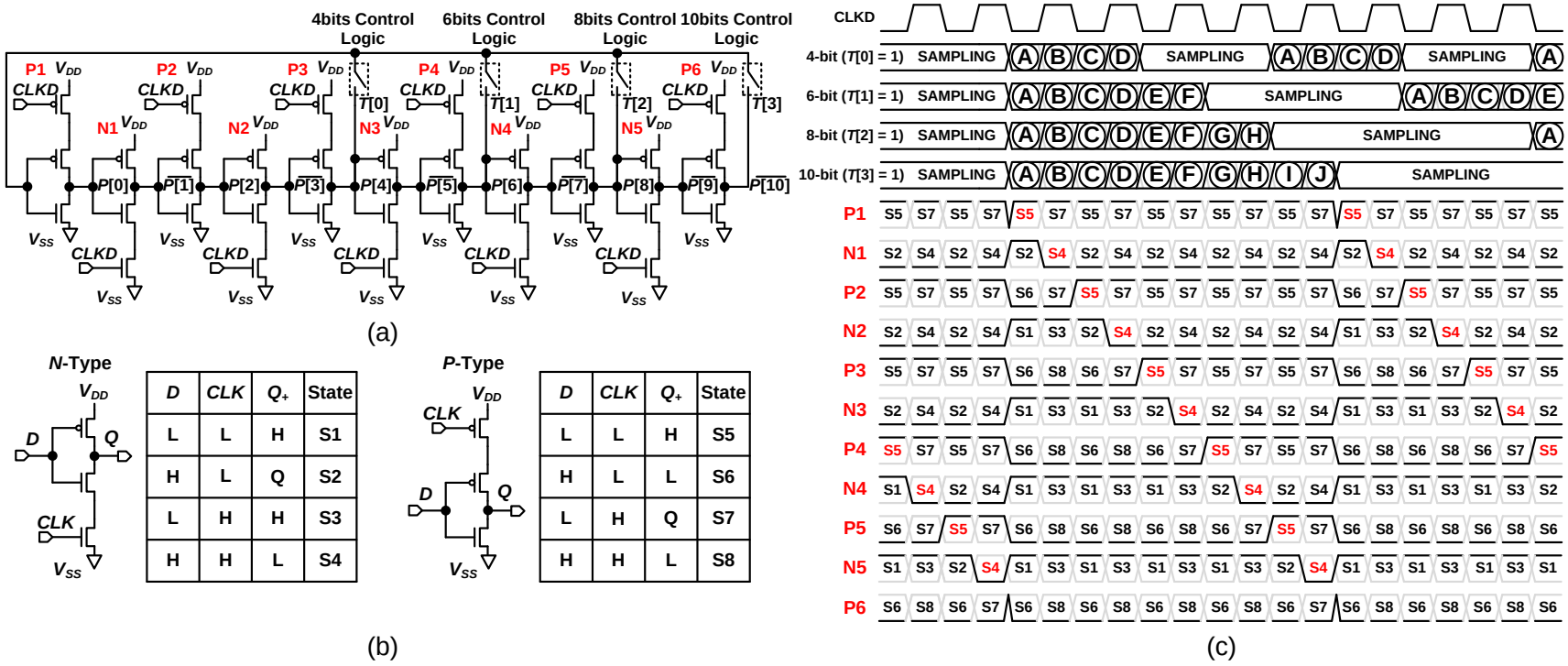


Figure 4.3: A 4-bit to 10-bit dual-channel SAR control logic.

4.3.1.1 Sequential Registers

A reconfigurable sequential registers with embedded resolution control logic is proposed, as shown in figure 4.4(a). Instead of using the foundry registers in the sequential registers in SAR ADC [81], we propose to use *N*-type, from N1 to N5 and *P*-type, from P1 to P6, tri-state inverters to generate these signals. Each tri-state inverter would only require 3 transistors and their corresponding truth tables and state notations are shown in figure 4.4(b). The first 5 rows in the timing diagram of figure 4.4(c) illustrate the signal, *CLKD* and the timing sequences under different resolution modes. For example, in the 10-bit resolution mode, the main goal of this circuit is to generate a pulse, $P[0]$ with the *P*-type tri-state inverters (P1 and P6) and toggle the subsequence signals in the tri-state inverters by half of *CLKD* cycle with respect to each other. The pulse signal is terminated when it propagates from a *P*-type tri-state inverter (P6) to another *P*-type tri-state inverter (P1). The states notation for the respective tri-state inverters and the propagation of the signals through these inverters are illustrated in the timing diagram in figure 4.4(c). The proposed sequential registers simplify the conventional design, require half of the input clock's frequency and reduce any unnecessary switching energy compared to the conventional sequential registers, leading to significant energy and area savings.

For the resolution setting, the circuit would only need a one-hot decoder to decode the input signals, $R[0:1]$ into $T[0:3]$, which sets the corresponding switches and provides a resolution control from 4-bit to 10-bit in 2-bit increments. Basically, the switches changes the number of tri-state inverters in the sequential registers and changes the number of states. The control logic can be easily customized to incorporate 1-bit increments and individual resolution mode control. Therefore, the proposed reconfigurable sequential registers simplifies the reconfigurability of the SAR control logic.



D	CLK	Q_+	State
L	L	H	S1
H	L	Q	S2
L	H	H	S3
H	H	L	S4

D	CLK	Q_+	State
L	L	H	S5
H	L	L	S6
L	H	Q	S7
H	H	L	S8

Figure 4.4: (a) Reconfigurable Shift Register built on tri-state inverter chain with the configurable timing sequence. (b) The schematic diagrams of tri-state inverter and the corresponding truth table and state notation. (c) Example of a 10-bit shift register with the corresponding waveform.

4.3.1.2 Storage registers

In the bit-cycling phase, the rising edge of the output signals from the sequential registers trigger the storage registers sequentially and store the decision output from the comparator. At the end of every conversion cycle, these registers are reset for the next conversion cycle [81]. In this work, we adopt the dual-edge triggered clocking strategy by using the rising edge and falling edge of the output signals from the sequential registers to latch and reset the storage registers, respectively.

Figure 4.5 shows the schematic, the truth table and the timing diagram of the proposed flip-flop. It is constructed using *SP-PN-PN* basic stages [82]. When the data, D, is logic '1' during the clock's rising edge, N_2 remains close to V_{DD} and N_3 is pulled to V_{SS}. The digital outputs, Q and QB change to V_{DD} and V_{SS} respectively. Similarly, when the data, D, is logic '0' during the clock's rising edge, N_2 is pulled to V_{SS} and N_3 remains close to V_{DD}. The digital outputs, Q and QB change to V_{SS} and V_{DD} respectively. When the clock remains V_{DD}, any input changes do not propagate to the output. At the clock transition, when CLK changes from V_{DD} to V_{SS}, N_2 and N_3 are pulled to V_{DD} by transistor M_4 and M_7 respectively. Thus, both digital outputs, Q and QB change to V_{SS}. The digital outputs of this register are resembled to the return-to-zero signals. The proposed registers do not require additional clock phase and transistor for end of the conversion.

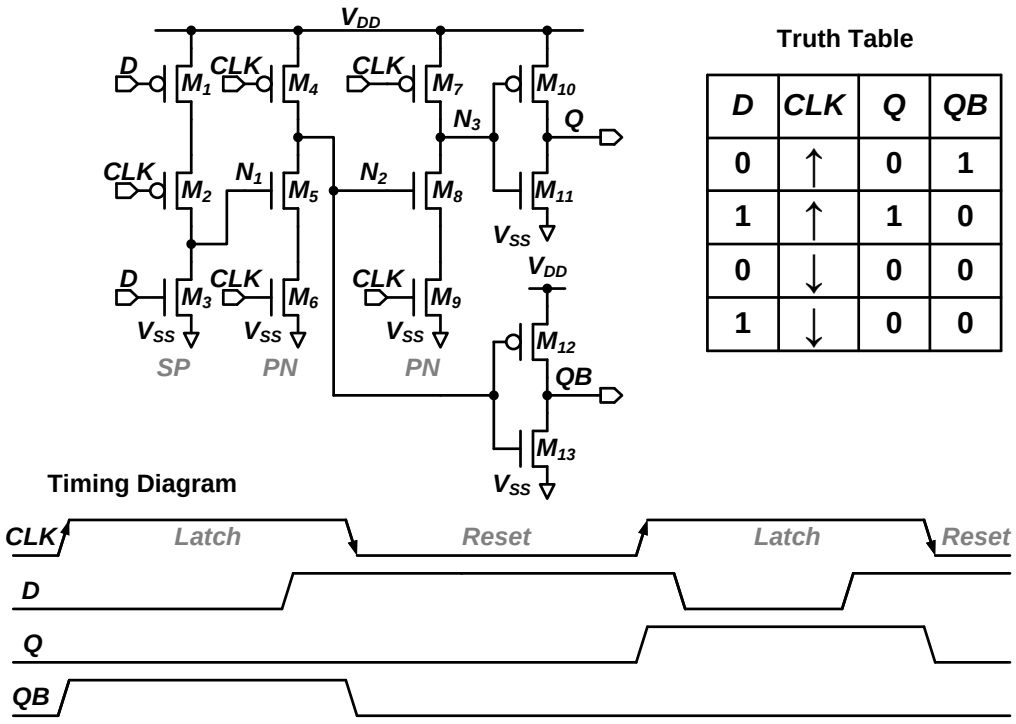


Figure 4.5: Schematic and truth table of proposed flip-flop with auto-reset.

4.3.2 Switching network

The switch matrix consist of sampling switches and references switches, which are connected to the bottom plates of each capacitor in *S/H* and *main* capacitive-arrays, as shown in figure 4.3. The "bottom-plate sampling" technique is used to sample the differential input signals onto the bottom plates of *S/H* capacitive-arrays and to minimize the charge injection effect.

4.3.2.1 Sampling switches

Bootstrapping technique helps to achieve better linearity, faster settling time and minimize the signal-dependent charge injection effect at a low supply voltage. In this work, we propose a modified bootstrapped circuit to sample the input signal onto the capacitors in the *S/H* capacitive-arrays, as shown in figure 4.6. This reduces the number of transistors and storage capacitor, C_S, which results in a more hardware-efficient sampling circuit and reduces any clock skew difference between the sampling switches.

4.3.2.2 Reference switches

The *S/H* and *main* reference switches can be realised from the circuits shown in figures 4.7 (a) and (b), respectively. The transmission gates are used to reduce the on-impedance when switching the V_{CM} reference voltage to the capacitive-arrays. The stacking transistors technique are used to reduce the leakage in the standby mode when switching the V_{REFP} and V_{REFN} reference voltages to the capacitive-arrays [83]. The arrangement of switches only require control signals derived directly from the sequential registers and the storage registers without any additional combination logic, which leads to a lean logic design for our proposed switching method.

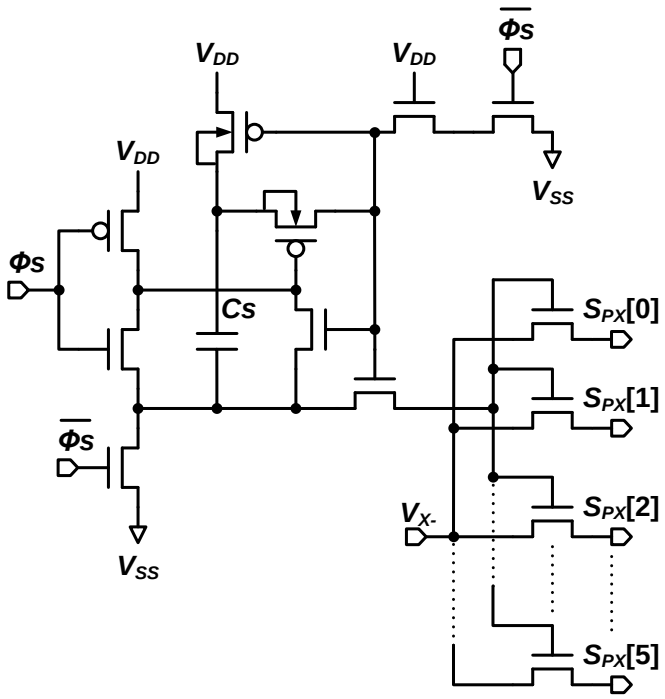


Figure 4.6: A schematic showing an integrated bootstrapped sampling switches for S/H$_X$ *capacitive array.*

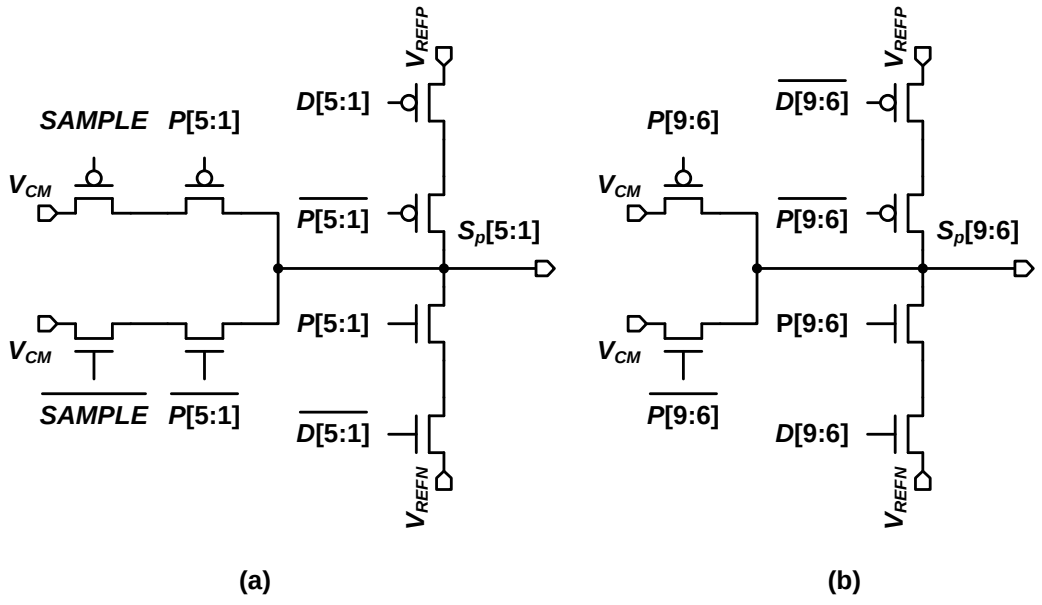


Figure 4.7: Schematic of (a) a S/H *Switch (b) a* main *Switch.*

4.3.3 Multiple-input comparator design

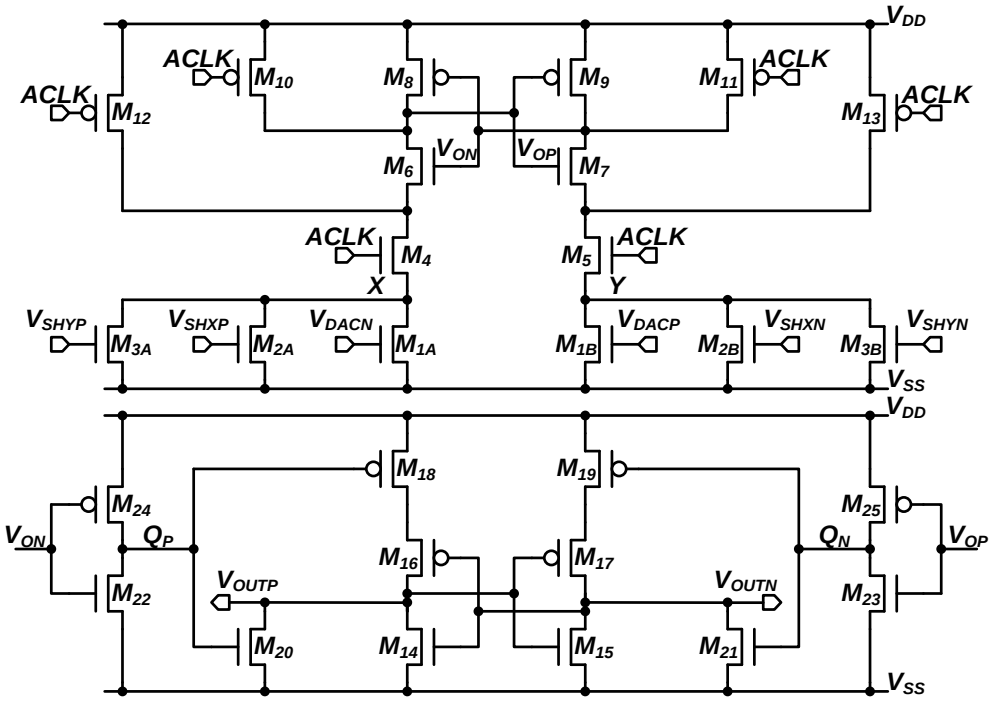


Figure 4.8: Proposed multiple-input dynamic latched comparator.

Figure 4.8 shows the schematic of the dynamic latched comparator used in this ADC. Since the switching method maintains the common-mode voltage during the bit-cycling, it helps to suppress the ADC performance degradation caused by the signal-dependent offset and N-type low-threshold voltage (low-V_{TH}) input pairs are used to ensure a higher gain at the low voltage operation.

During the reset phase, $ACLK$ sets to V_{SS} and the comparator outputs V_{OP} and V_{ON} set to V_{DD}. All the internal nodes are either set to V_{DD} or V_{SS}, eliminating any memory effect from the previous cycle. During the regeneration phase, $ACLK$ sets to V_{DD}, the different voltage signals present at the input pairs will result in the different currents flowing at nodes X and Y .

The cross-coupled inverters made of M_6 - M_9 will start to regenerate and force

either V_{OP} or V_{ON} to V_{DD}. The inverters made of M_{22} - M_{25} buffer V_{OP} and V_{ON}, avoid the kickback noise generated by the SR-NOR latch. The SR-NOR latch will force one output to V_{DD} and the other to V_{SS} according to the comparison result.

Multiple-channel, time-interleaved ADC architecture can be realised using the comparator through the following analysis. The currents at nodes X and Y can be derived as

$$\begin{aligned} I_X &= \mu_n C_{OX} \frac{W}{L}(V_{SHYP} + V_{SHXP} + V_{DACN} - 3V_{THN} - \frac{3V_X}{2})V_X, \\ I_Y &= \mu_n C_{OX} \frac{W}{L}(V_{SHYN} + V_{SHXN} + V_{DACP} - 3V_{THN} - \frac{3V_Y}{2})V_Y, \end{aligned} \tag{4.2}$$

where μ_n, C_{OX} and V_{THN} are charge-carrier effective mobility, gate oxide capacitance per unit area and threshold voltage of N-type transistors, respectively. W and L are the channel width and length of all the input transistors, M_{1A} - M_{3A} and M_{1B} - M_{3B}. In the beginning of regeneration phase, the V_X is approximately equal to V_Y, the current difference between X and Y is derived as

$$I_X - I_Y = \mu_n C_{OX} \frac{W}{L}(V_{SHYP} + V_{SHXP} + V_{DACN} - V_{SHYN} - V_{SHXN} - V_{DACP})V_X. \tag{4.3}$$

As shown in figure 4.1, during the S/H_X sampling phase, V_{SHXP}, V_{SHXN}, V_{DACP} and V_{DACN} are reset to V_{CM} while the bit-cycling is performed on the S/H_Y capacitive arrays and (4.3) can be simplified to

$$I_X - I_Y = \mu_n C_{OX} \frac{W}{L}(V_{SHYP} - V_{SHYN})V_X. \tag{4.4}$$

Thus, the comparator is able to resolve (B+1)-bit resolution from the S/H_Y capacitive arrays, as shown in figures 3.11 and 3.12. Then, during DAC bit-cycling phase, V_{SHYP}, V_{SHYN}, V_{SHXP} and V_{SHXN} remain unchange and V_{DACP} and V_{DACN} start to

change according to the comparison result and (4.3) can be simplified to

$$I_X - I_Y = \mu_n C_{OX} \frac{W}{L}(V_{DACN} - V_{DACP} + \Delta V_{SHY})V_X \tag{4.5}$$

where ΔV_{SHY} is the residual charges after the (B+1)-bit-cycling phase. The DAC bit-cycling phase is performed for the next (N-B-1)-bit resolution and V_{DACP} - V_{DACN} converges to ΔV_{SHY}. The other channel can be analyzed in a similar fashion.

4.4 Measurement results

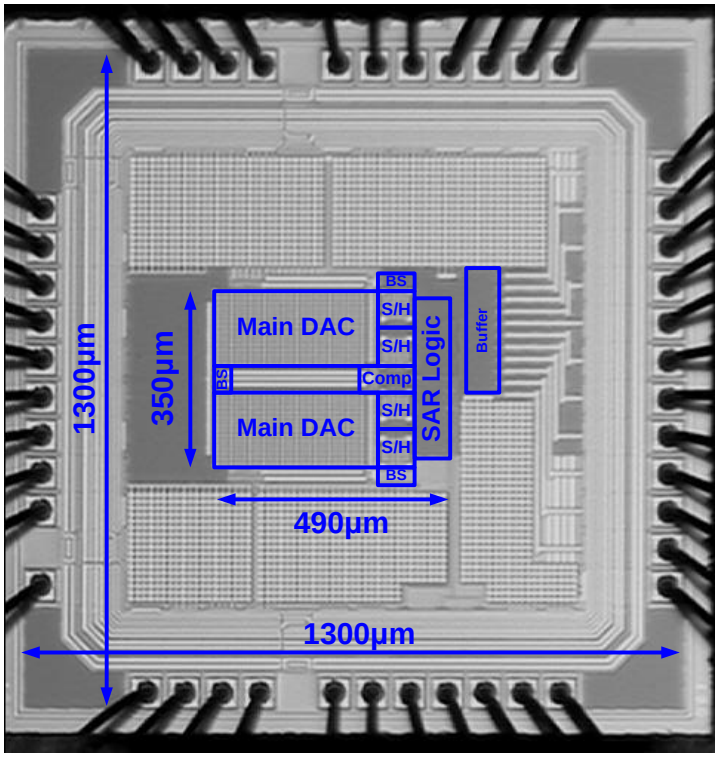


Figure 4.9: Micrograph of entire ADC prototype.

The prototype ADC was fabricated in a 130-nm CMOS process and the chip micrograph is shown in figure 4.9. The dual-channel ADC core occupies an active area of 490-µm × 350-µm and the total area is 0.172 mm^2. Each *S/H* and *main* capacitive-arrays occupy an active area of 65-µm × 65-µm and 160-µm × 300-µm, respectively. The *main* capacitive arrays occupy about 56% of the total area, which indicates that additional channels will only marginal increase the total area due to the common sharing of the main capacitive-arrays.

Table 4.1: ADC Performance Summary

Specification	Measurement Result			
Technology	Globalfoundries 130-nm			
Core Area (mm^2)	0.086			
Supply Voltage (V)	0.6			
Common-Mode (V)	0.3			
Input Range (V_{PP})	1.16			
Input Capacitance (fF)	1760			
Sampling Rate (kS/s)	250			
Peak DNL (LSB)	+0.46 / -0.28			
Peak INL (LSB)	+0.83 / -0.75			
Resolution Mode (bit)	4	6	8	10
Power (μW)	1.8	2.1	3.3	3.9
SNDR @ DC (dB)	25.84	37.73	49.50	57.94
SNDR @ Nyquist (dB)	25.83	37.80	48.96	55.07
SFDR @ Nyquist (dB)	37.1	50.2	62.0	68.1
FOM @ DC (fJ/c-s)	450	133	54	24
FOM @ Nyquist (fJ/c-s)	450	132	57	33

The measurement of the prototype are summarized in Table 4.1. The testing setup is shown in Appendix B. The prototype is measured at a supply voltage of 0.6-V with a sampling rate up to 250-kS/s in all resolution modes. The average input signal swing of the ADC is 1.16-V_{PP}. The gain error is resulting from the parasitic capacitance of the S/H capacitive arrays and comparator input pairs.

4.4.1 Static Performance

Figure 4.10 shows the measured data of the differential nonlinearity (DNL) and the integral nonlinearity (INL) at a supply voltage of 0.6-V and a sampling rate of 250-kS/s in the 10-bit mode. The maximum DNL and INL are +0.46/-0.28 LSB and +0.83/-0.75 LSB, respectively. The sawtooth pattern in INL arises from the mismatch between *S/H* and *main* capacitive-arrays and the linearity can be improved by increasing the size of the unit capacitor in the *S/H* capacitive-arrays with negligible increase in the total area and switching power.

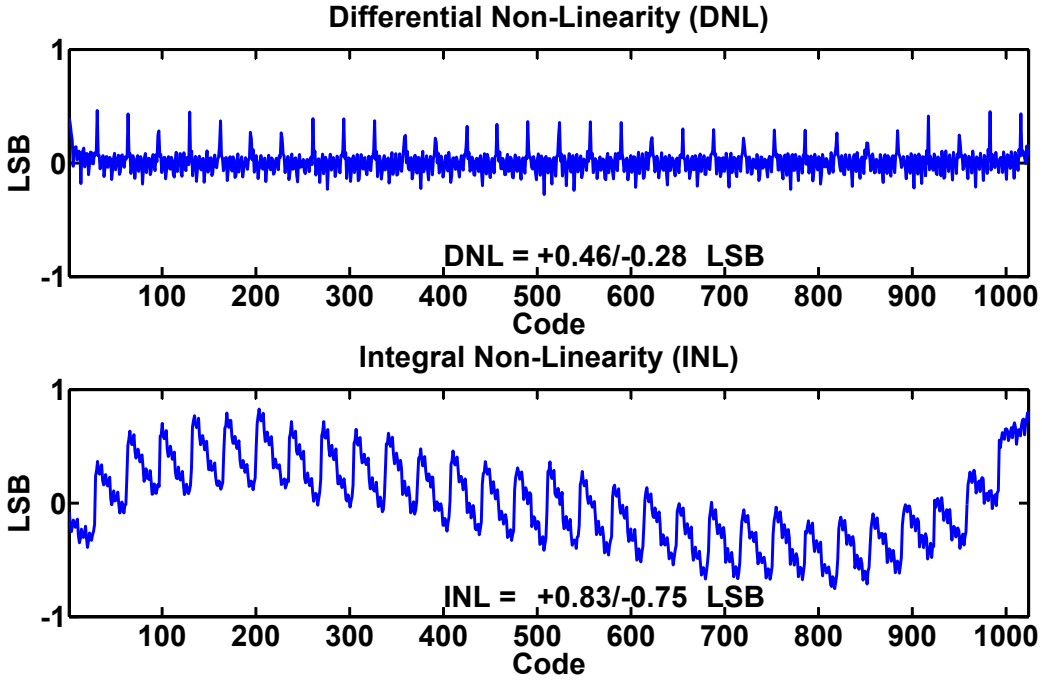


Figure 4.10: Measured DNL and INL at f_S = 250-kS/s in 10-bit mode.

4.4.2 Dynamic Performance

Figure 4.11 shows 8192-points fast fourier transform (FFT) plots in the 10-bit mode. The measured signal-to-noise and distortion ratio (SNDR) and spurious-free dynamic range (SFDR) near-DC tone input are 57.9-dB and 71.6-dB, respectively. The measured SNDR and SFDR near-nyquist tone input are 55.0-dB and 68.1-dB, respectively. Figure 4.12 shows the SNDR versus the input frequency for all resolution modes at supply voltage of 0.6-V and sampling rate of 250-kS/s.

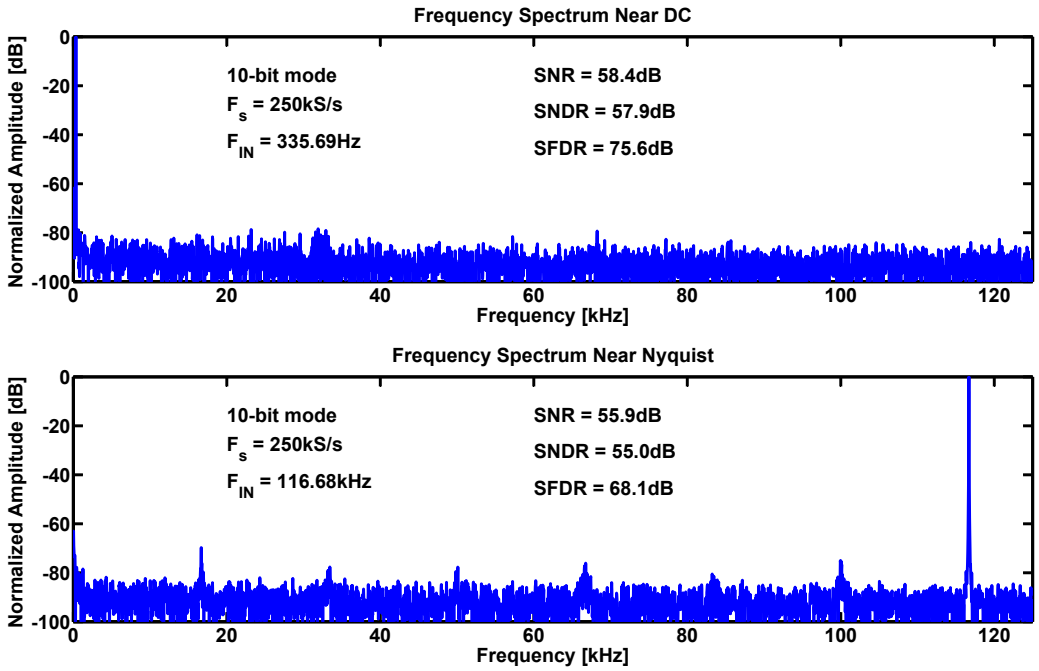


Figure 4.11: Measured FFT with 8192-points at 250kS/s with input tone at 335.69-Hz and 116.68-kHz, respectively

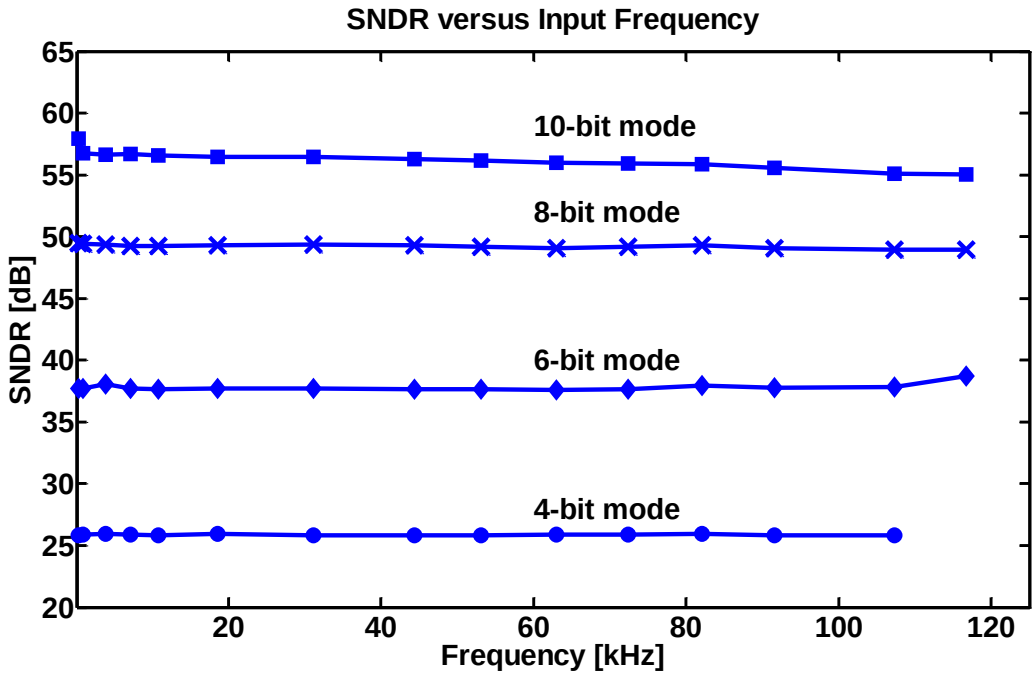


Figure 4.12: Measured SNDR vs. input frequency over all resolution modes at f_s = 250kS/s at 0.6-V.

4.4.3 Power Consumption and Figure-of-Merit

Table 4.2 compares the ADC in 10-bit mode with other state-of-the-art SAR ADCs [58, 78, 84–86]. To compare with other state-of-the-art SAR ADCs, a commonly used *Walden* FOM for ADCs considering resolution, bandwidth and power consumption is given by

$$FOM = \frac{P}{2^{ENOB} \times 2 \times f_{in}} \tag{4.6}$$

where P is the power consumption, and $ENOB$ is measured at the stated f_{in} [3]. In the 10-bit mode, the ADC achieves one of the highest sampling rate and a FOM of 24-fJ/conversion-step at a supply voltage of 0.6-V and a sampling rate of 250-kS/s, which is comparable to the current state-of-the-art ADCs. Figure 4.13 shows the energy-per-conversion versus SNDR for the proposed ADC and recently reported

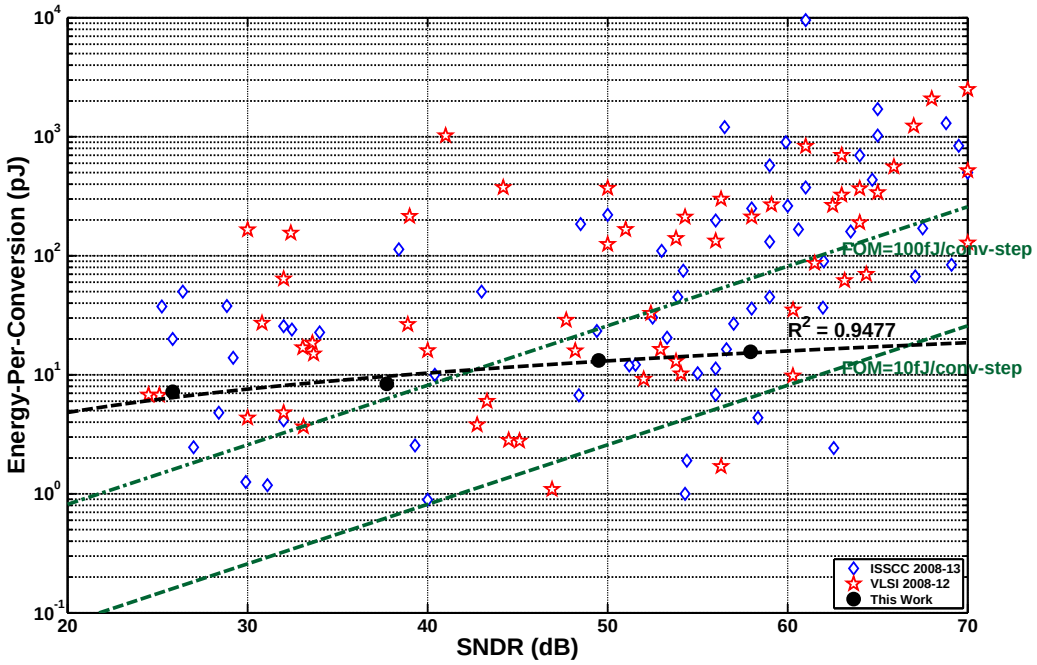


Figure 4.13: Comparison to State-of-The-Art works [4].

designs over the last five years [4]. Even without the use of sub-fF capacitors, the measurement result has shown that this work achieves a energy efficiency close to the state-of-the-art result over a wide range of resolutions. A linear regression analysis on the energy-per-conversion versus SNDR for the proposed ADC achieves 0.9477 for the coefficient of determination, which demonstrate a linear scaling of energy across different resolution modes.

Table 4.2: Comparison to State-of-The-Art SAR ADCs

Design	ISSCC '08 [58]	ASSCC '09 [84]	JSSC '11 [85]	JSSC '12 [86]	JSSC '13 [78]	This work
Technology (nm)	180	180	180	180	65	130
Core Area (mm^2)	0.24	0.24	0.125	0.082	0.212	0.086
Supply Voltage (V)	1	1	0.6	0.6	0.5	0.6
Input Range (V_{PP})	0.8	2	1.2	1.13	1.0	1.16
Sampling rate (kS/s)	100	500	100	200	20	250
DNL (LSB)	<0.55	+0.76/-0.8	+0.4/-0.7	+0.25/-0.23	<0.57[1]	+0.46/-0.28
INL (LSB)	<0.7	+0.76/-0.76	+0.8/-0.7	+0.38/-0.34	<0.58[1]	+0.83/-0.75
SNDR @ DC (dB)	58	-	-	57.98	-	57.94
SNDR @ Nyquist (dB)	56.3	58.4	57.7	57.46	55.0	55.07
SFDR @ Nyquist (dB)	64.2	75	67	66.7	68.8	68.1
Power (μW)	3.8	43	1.3	1.04	0.206	3.9
FOM (fJ/c-s)	56 @ DC 71@Nyquist	124	21	8.03	22.4	24 @ DC 33 @ Nyquist

[1]Measured @ 0.6-V,100kS/s

4.5 Summary

A design approach for an energy-efficiency dual-channel reconfigurable resolution SAR ADC for the sensor applications is presented. The SAR ADC has a reconfigurable 4-to-10-bit resolution and a maximum sampling rate of 250-kS/s, operating at a supply voltage of 0.6-V. The use of time-interleaving architecture relaxes the design requirements for *S/H* circuits and reduces the number of switches by 2× in the analog multiplexer. The proposed energy-efficient charge-recovery switching method circumvents existing trade-offs in resolution-reconfigurable DAC architectures and achieves a 3.6-to-77.5× reduction in 4-to-10-bit resolution modes compared to conventional DAC architecture. Along with the proposed multiple-input comparator, the proposed architecture achieves one of the smallest area (without the use of custom-made capacitor) for a 10-bit SAR ADC. Custom-designed digital logics with dual-edge triggered clocking techniques are used to reduce the digital power consumption and further simplify the digital control logic. Thus, the proposed ADC achieves a FOM of 24-fJ/conversion-step in 10-bit mode.

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Chapter 5

Placement Strategy For The Conventional Binary-Weighted Capacitive-Array DAC

5.1 Introduction

State-of-the-art SAR ADCs have offered a power-efficient solution but with limited accuracies (<10-bit) [4]. As the resolution of the SAR ADC increases, the overall accuracy and linearity of the SAR ADC are primarily determined by its DAC's matching characteristics, which demands for a more stringent matching requirement for the unit capacitors (i.e. increases the area of the unit capacitor) and the total number of capacitor increase exponentially [57]. Thus, it is harder to achieve accurate capacitance ratios in the layout, which are affected by systematic and random mismatches. The systematic mismatch is caused by identical devices with asymmetrical environments, while the random mismatch is caused by statistical fluctuations in processing conditions or material properties [87, 88]. An ideal placement for the DAC array should try to minimize the systematic mismatches,

followed by the random mismatch.

There are two popular mismatch evaluation models to quantify the random mismatch and the first-order systematic mismatch. First, the two-dimensional spatial correlation model quantifies the degree of dispersiveness in the layout [89]. A higher degree of dispersiveness indicates that there is a smaller random mismatch in the layout. Second, the two-dimensional oxide gradient model estimates the oxide-gradient-induced mismatch (i.e., first-order systematic mismatch) in the capacitive array [90, 91]. Although a common-centroid arrangement averages the effect of first-order systematic mismatch, it is a non-deterministic polynomial-time (NP) hard optimization problem and thus, this model quantifies the degree of symmetry and the degree of coincidence in a common-centroid arrangement. Similarly, a higher degree of symmetry and coincidence indicates that there is a smaller first-order systematic mismatch in the layout.

Since then, numerous placement methods have been reported to deal with arbitrary shapes and devices in the layout, which based on the evaluation models to determine the optimal layout. The heuristic search approach aims to maximize the degree of dispersiveness in the layout but the placement might not have a common-centroid arrangement and thus resulting a systematic mismatch [92]. Pairs representation techniques are introduced to handle symmetry, common-centroid and general placement simultaneously but they do not yield the optimal layout for the CBW DACs [93–97]. The simulated-annealing-based (SA-based) approach aims to increase the degree of dispersiveness and minimize oxide-gradient-induced mismatch simultaneously but the resulting placement increases the complexity of the wiring [98, 99].

Besides the first-order systematic mismatch, no previous studies take into account of the following systematic mismatches for the placement of the binary-weighted capacitive array, such as the second-order lithographic errors, the proximity effects,

the symmetry and the complexity of the wiring and the far range fringing fields effects. For example, in the nanometer CMOS technologies, the interconnect parasitic capacitances have reached the order of femtofarads while the capacitance of unit capacitors in the DAC has reduced to the scale of a few femtofarads for state-of-the-art SAR ADCs [14, 18, 41, 86, 100]. Any asymmetry in the wiring scheme can easily cause more problems than are solved [88].

Beside the placement constraints, many existing methods face exponential increase in the computational runtime to determine the optimal layout because of the number of combinations continuous to grow astronomically with the increasing resolution bits. In a N-bit CBW DAC, the number of combinations can be expressed as

$$Combinations = {}^{S}C_1 \times {}^{S-1}C_1 \times ... \times {}^{S-2^{j-1}}C_{2^{j-1}} \times ... \times {}^{S-2^{N-1}}C_{2^{N-1}}, \qquad (5.1)$$

where ${}^{S-2^{j-1}}C_{2^{j-1}}$ is the number of possible combinations for placing 2^{j-1} unit capacitors of C_j^A in $A_{L\times W}$ and is equivalent to $S!/[2^{j-1}!(S-2^{j-1})!]$ combinations. For example, a 10-bit C_{typeA} array in $A_{32\times 32}$, has approximately 3×10^{604} number of combinations. The number of combinations for the CBW DAC, grows astronomically beyond 10-bit and thus it is harder to achieve the optimization goal with any existing computational resources.

A new placement strategy to address the mismatches in the layout for the CBW DAC, which incorporates a matrix-adjustment method for the DAC, different placement techniques and weighting methods for the placements of active and dummy unit capacitors. The resulting placement addresses both systematic and random mismatches. The following four systematic mismatches, such as the first-order process gradients, the second-order lithographic errors, the proximity effects, the wiring complexity and the asymmetrical fringing parasitics, are considered.

5.2 Terminology and review of evaluation models

5.2.1 Terms and definitions for the capacitive-array DAC

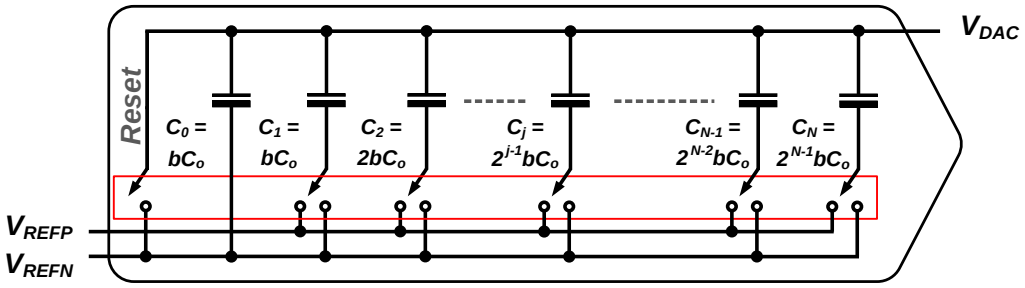


Figure 5.1: N-bit Conventional Binary-weighted capacitive array DAC.

In a N-bit CBW DAC, as shown in figure 5.1, there are N+1 capacitors denoted by $C = \{C_0, C_1, C_2, \ldots, C_j, \ldots, C_N\}$ with a ratio of $C_0 : C_1 : C_2 : C_3 : \ldots : C_j : \ldots : C_N$ be $b : b : 2b : 4b : \ldots : 2^{j-1}b : \ldots : 2^{N-1}b$, where $0 \leq j \leq N$ and $b \in \mathbb{Z}^+$. For the layout implementations, C_{typeA} in [70, 101] and C_{typeB} in [76, 102] are known to be the most common architectures adopted when realizing the N-bit capacitive array, where $C_{typeA} = \{C_0^A, C_1^A, C_2^A, \ldots, C_N^A\} = 1 : 1 : 2 : 4 : \ldots : 2^{N-1}$ and $C_{typeB} = \{C_0^B, C_1^B, C_2^B, \ldots, C_N^B\} = 2 : 2 : 4 : 8 : \ldots : 2^N$. C_{typeB} is often chosen in implementations because every element in C_{typeB} is made up of even number of unit capacitors and thus, improving the symmetry of the layout. C_{total} is the total number of unit capacitors in C and it is placed in a $A_{L\times W}$ matrix. The size of $A_{L\times W}$ is denoted by S, where $\{S = L\times W : L, W \in \mathbb{Z}^+\}$. Let $a_{l,w}$ denote the entry in the l-th row and w-th column, where $0 \leq l \leq L$ and $0 \leq w \leq W$. Each entry in $A_{L\times W}$ can be placed with either one unit capacitor from C or one dummy unit capacitor, C_{dummy}. The total number of dummy unit capacitors in $A_{L\times W}$ is denoted as C_D, where C_D = S - C_{total}.

To have a fair comparison with other previous works as those in [89, 91, 92, 98, 99], two mismatch evaluation models are adopted in this paper [89, 91]. The following subsection reviews these two models in the context of C_{typeA} architecture and the parameters of the models are defined.

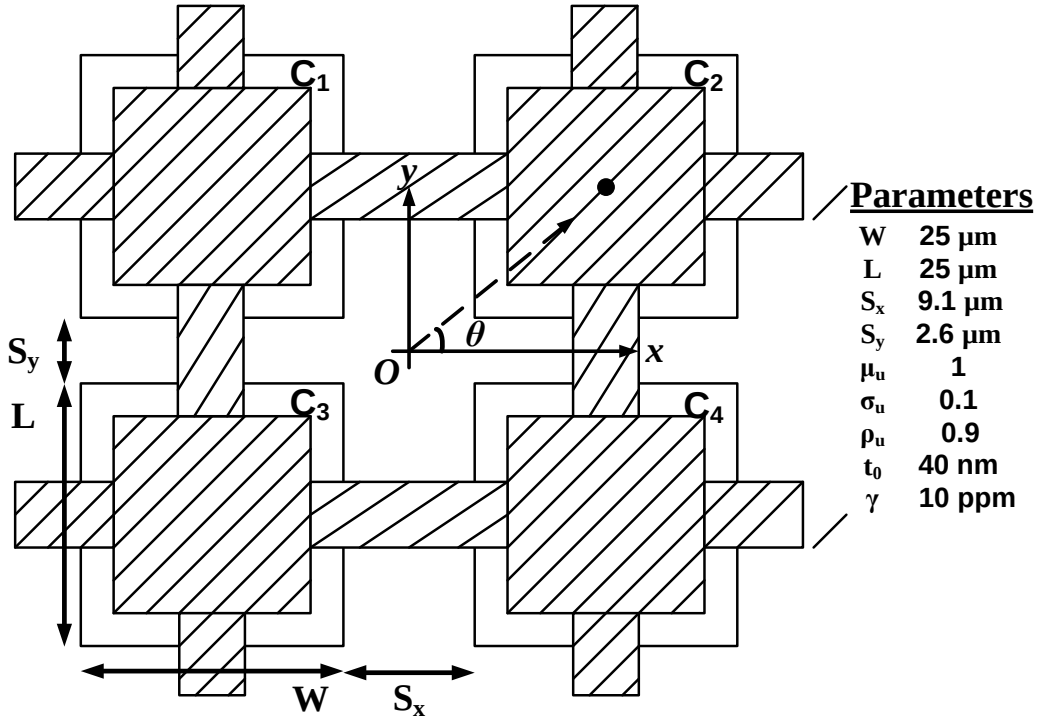


Figure 5.2: Experimental Setup for the geometry of unit capacitors and mismatch parameters.

5.2.2 Random mismatch model - two-dimensional spatial correlation model

The spatial correlation model of any two unit capacitors C_{om} and C_{on}, in the C_{typeA} is defined as $\rho_{m,n}$,

$$\rho_{m,n} = \rho_o^{D(m,n)}, \tag{5.2}$$

where ρ_o is the correlation coefficient between any two unit capacitors and the distance $D(m,n)$ between C_{om} and C_{on} is

$$D_{m,n} = \sqrt{(x_m - x_n)^2 + (y_m - y_n)^2} \times L_D, \tag{5.3}$$

where (x_m, y_m) and (x_n, y_n) are coordinates of C_{om} and C_{on} respectively and L_D is dependent on the process and size of the devices. To simplify (5.2) and (5.3), we assume L_D = 1 to observe the relationship between correlation and random mismatch. It is assumed that all unit capacitances have the same variances and the correlation coefficient between any two unit capacitors ρ_o is 0.9, as shown in figure 5.2. Therefore, the variance of any capacitor in C_{typeA}, C_i^A, which consists of 2^i unit capacitors, where $0 \leq i \leq N$-1 can be simplified to

$$\begin{aligned} Var(C_i^A) &= \sum_{a=1}^{2^i} Var(C_o) + 2\sum_{a=1}^{2^i-1}\sum_{b=a+1}^{2^i} Cov(C_{ia}, C_{ib}) \\ &= Var(C_o) \times (2^i + 2\sum_{a=1}^{2^i-1}\sum_{b=a+1}^{2^i} \rho_{a,b}), \end{aligned} \tag{5.4}$$

where Var(C_o) is the variances of the unit capacitor and Cov(C_{ia}, C_{ib}) is the covariance of C_{ia} and C_{ib}.

Similarly, given any two capacitors in C_{typeA}, C_i^A and C_j^A, which consist of 2^i and 2^j unit capacitors respectively, where $0 \leq i,j \leq N$-1, the correlation coefficient of C_i^A and C_j^A is the summation of the correlation coefficients of all the capacitor pairs in C_i^A and C_j^A. It can be simplified to

$$\begin{aligned}\rho_{i,j} &= \frac{Cov(C_i^A, C_j^A)}{\sqrt{Var(C_i^A)Var(C_j^A)}} \\ &= \frac{\sum_{a=1}^{2^i}\sum_{b=1}^{2^j}\rho_{a,b}}{\sqrt{\left(2^i + 2\sum_{a=1}^{2^i-1}\sum_{b=a+1}^{2^i}\rho_{a,b}\right)\left(2^j + 2\sum_{a=1}^{2^j-1}\sum_{b=a+1}^{2^j}\rho_{a,b}\right)}},\end{aligned} \tag{5.5}$$

where Cov(C_i^A,C_j^A) is the covariance of C_i^A and C_j^A. Var(C_i^A) and Var(C_j^A) are variances of capacitors C_i^A and C_j^A, respectively.

For a N-bit CBW DAC, the total correlation coefficient, L, is the summation of the correlation coefficients of all the capacitor pairs

$$L = \sum_{i=1}^{N}\sum_{j=i+1}^{N+1}\rho_{i,j}. \tag{5.6}$$

It was reported that a higher total correlation coefficient, L, leads to a lower variation in the capacitive array or a higher matching capacitance ratio [89]. This model provides an insight to the degree of randomness and dispersion in the capacitive array.

5.2.3 First-order process mismatch - oxide gradient model

After the placement of C_{typeA}, the effective capacitor ratio becomes $C_0^{A*} : C_1^{A*} : C_2^{A*} : C_3^{A*} : \ldots : C_j^{A*} : \ldots : C_N^{A*}$. Let $\{C_{j1}^{A*}, C_{j2}^{A*}, C_{j3}^{A*}, \ldots, C_{j2^{j-1}}^{A*}\}$ denote the set of 2^{j-1} unit capacitors belonging to C_j^{A*}. The total capacitance of C_j^{A*} is the summation of the capacitance of the unit capacitors in C_j^{A*}.

Assume that the capacitive array is affected by a linear oxide gradient γ in the direction specified by an angle θ, as shown in figure 5.2. Due to the oxide gradient, different unit capacitors located at the different locations experience different oxide thicknesses and therefore the effective capacitance of any unit capacitor is

$$C_{ji}^{A*} = C_o \frac{t_o}{t_i}, \tag{5.7}$$

where C_u is the unit capacitance, t_o is the oxide thickness at the origin *0* and t_i is the equivalent oxide thickness at location (x_i ,y_i)

$$t_i = t_o + \gamma(x_i \cos\theta + y_i \sin\theta). \tag{5.8}$$

The ratio mismatch is then calculated for all the pairs of capacitor in C_{typeA}. The capacitance ratio mismatch, M in C_{typeA} is defined as

$$\begin{aligned} M &= \max\left(\left|\frac{\frac{C_j^{A*}}{C_k^{A*}} - \frac{C_j^A}{C_k^A}}{\frac{C_j^A}{C_k^A}}\right|\right) \times 100\% \\ &= \max\left(\left|\frac{C_j^{A*}}{C_k^{A*}}\frac{C_k^A}{C_j^A} - 1\right|\right) \times 100\%, \end{aligned} \tag{5.9}$$

where $0 \leq j, k \leq N{+}1$. Since the gradient angle cannot be predicted, the mismatch is estimated through $0^\circ \leq \theta \leq 180^\circ$ and the maximum mismatch value is obtained.

This model provides an insight to the degree of symmetry and coincidence which is very important for binary-weighted capacitive array in nanometer CMOS technologies [90]. A smaller capacitance mismatch ratio, M, yields a smaller systematic mismatch in the capacitive array. To have a fair comparison with other works, we assume that the oxide thickness t_o is 40 nm, the oxide gradient γ is 10 parts per million and the width and length of a unit capacitor, C_u is 25 μm (W) by 25 μm (H) with a spacing of 9.1 μm (S_x) by 2.6 μm (S_y) respectively, as shown in figure 5.2.

5.3 Placement strategy

The proposed placement strategy first adjusts the matrix size based on the parameters listed in figure 5.2 and the type of binary-weighted capacitive array under consideration, e.g. C_{typeA} or C_{typeB}. As it will be explained in Section 5.3.1, the matrix size has a great influence on the final placement result and the degree of symmetry (first-order process gradient effects). The next step is to prioritize of the placement of the dummy capacitors and the capacitive array, respectively. This eliminates the second-order lithographic errors and the proximity effects and maximizes the degree of dispersiveness that can be achieved by the capacitive array. In order to simplify the routing in the common-centroid layout, the diagonal weighting is proposed for the placement of the capacitive array and thus allowing us to use a simple "rectangular and diagonal" wiring method to connect the capacitors together. Finally, the homogenizing algorithm is applied to the matrix and this allows a better distribution of parasitic capacitances amongst the capacitive array. The flow chart, as shown in figure 5.3, provides the details of our proposed placement strategy.

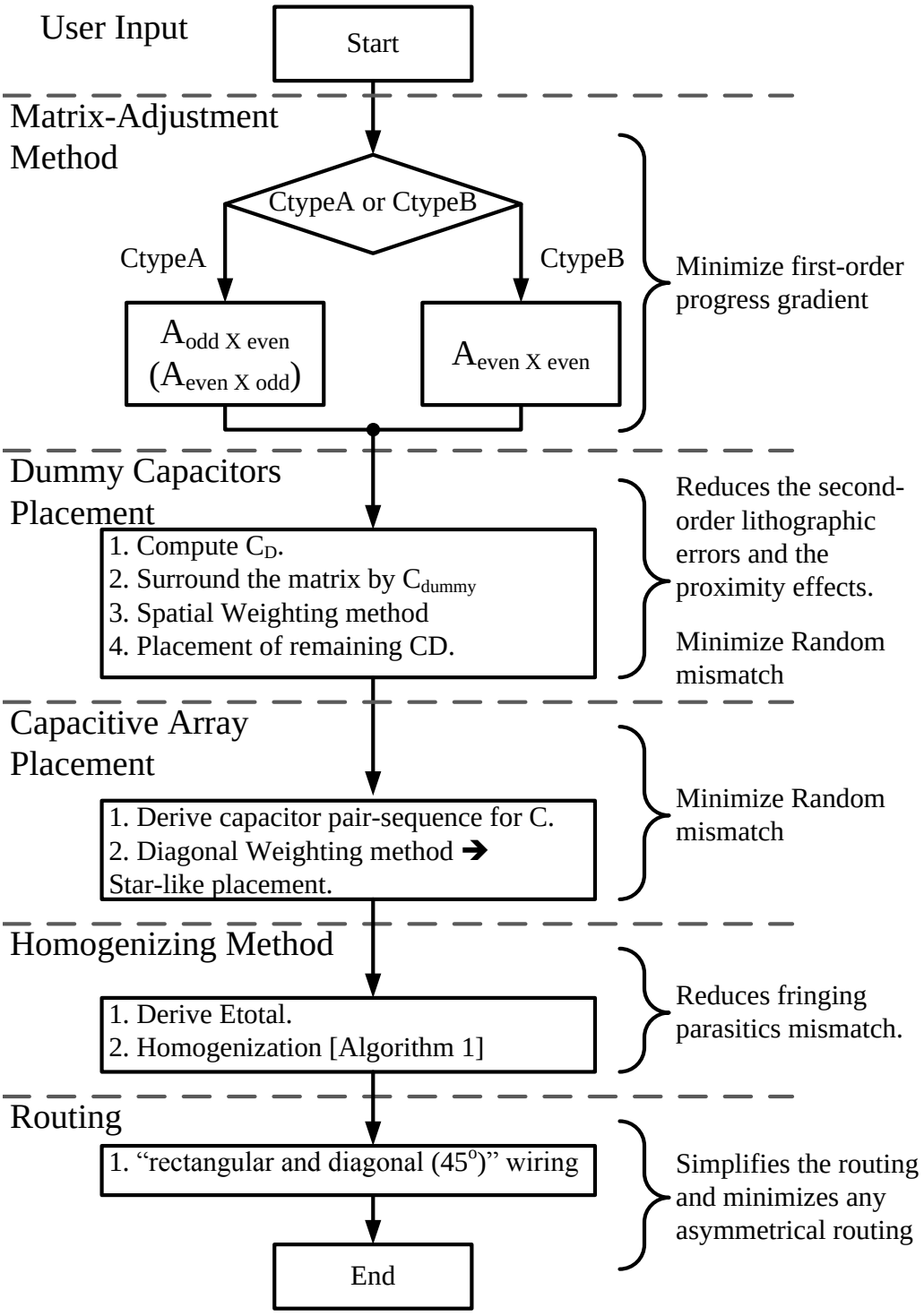


Figure 5.3: Flow chart illustrating the various techniques used in the proposed placement strategy.

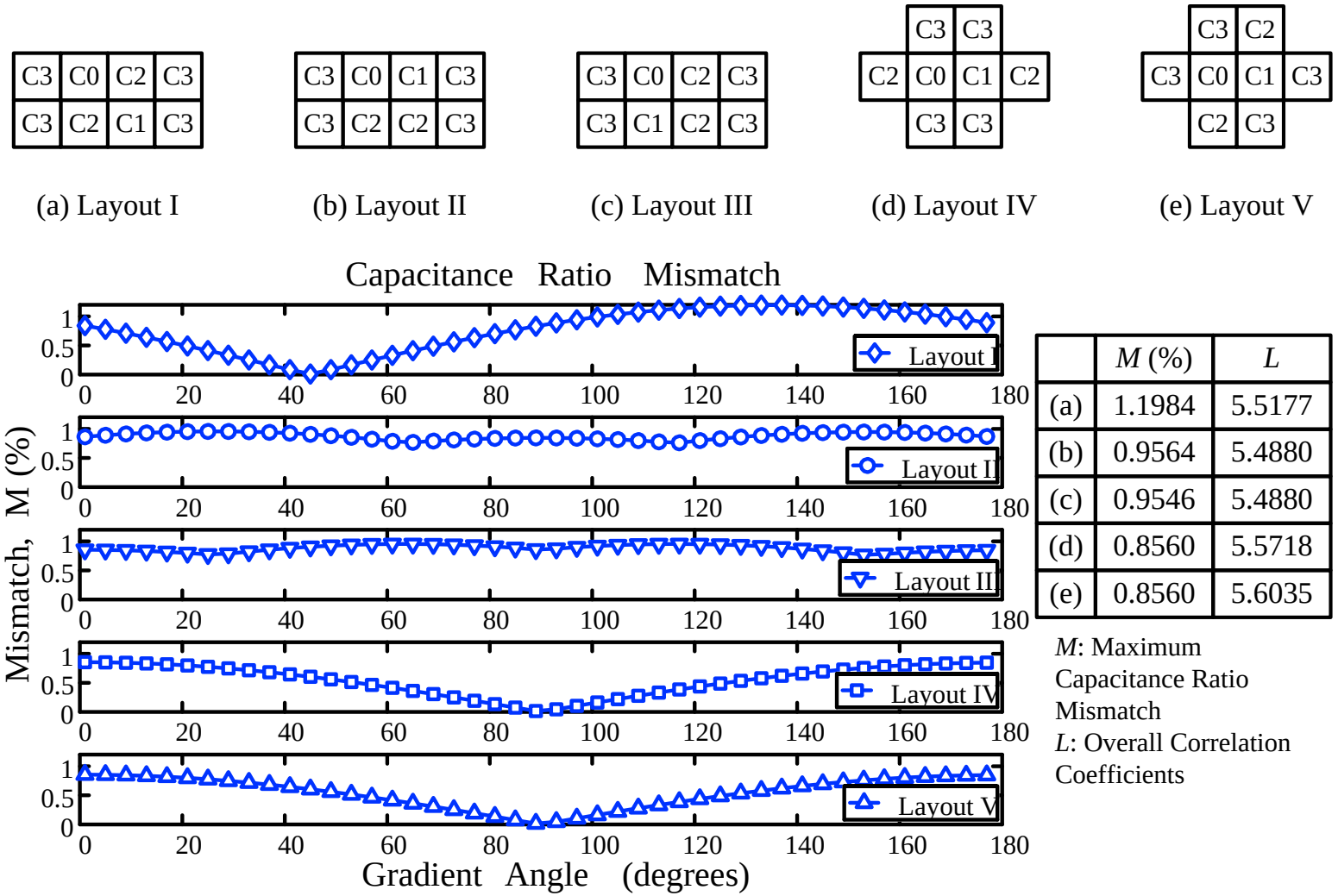
5.3.1 Matrix-adjustment method

Based on the oxide gradient model and the spatial correlation model, all the different possible layouts for the 3-to-5-bit C_{typeA} and C_{typeB} capacitive arrays in different matrix sizes were investigated. Five different examples of a 3-bit C_{typeA} layout are presented in figure 5.4, for the discussion of our matrix-adjustment method. Figure 5.4(a) shows a layout (Layout I) in $A_{2\times4}$ with partial symmetry about the origin where C_0^A and C_1^A are placed diagonally. Figures 5.4(b) and (c) show layouts (Layout II and III) in $A_{2\times4}$ with partial symmetry about the y-axis and the x-axis respectively, where C_0^A and C_1^A are placed on adjacent sides. This adjacent side placement of C_0^A and C_1^A resulted in decreased M and L, as shown in the table in figure 5.4. Figures 5.4(d) and (e) show layouts (Layout IV and V) in $A_{3\times4}$ with symmetry about the x-axis and partial symmetry about the origin, respectively. By changing the matrix to $A_{3\times4}$, there are further improvements in M and L. The results were calculated based on the input parameters listed in Section 5.2 except that S_x and S_y are 9.1 μm as this allows equal spacing between unit capacitors. The plots of capacitance ratio mismatch variation with respect to the gradient angle for these placements, as shown in figure 5.4, provide us with insightful details about the symmetrical property of the layout. Based on all the layouts investigated in this experiment, the following observations were made.

1. C_{typeA} contains an odd-numbered unit capacitor in C_0^A and C_1^A and thus, it is harder to achieve minimal M in $A_{odd\times odd}$ or $A_{even\times even}$. $A_{odd\times even}$ or $A_{even\times odd}$ provides a better symmetry for C_{typeA} capacitive arrays.
2. Adjacent side placements for the odd-numbered capacitors yield a smaller M. Thus, it is preferred that C_0^A and C_1^A are placed on adjacent sides and they should be placed near the center of a matrix.

3. The diagonal placements of capacitor pairs, from C_2 to C_N, yield a higher L than adjacent side placements.
4. C_{typeA} achieves better symmetry when it has a symmetrical mismatch variation.

The same evaluation method is applied to C_{typeB} and figure 5.5 shows an example of 2 different layouts of a 3-bit C_{typeB} in $A_{6\times6}$ and $A_{7\times6}$. The diagonal placements of the even-numbered capacitor pairs and the matrix-adjustment to $A_{even\times even}$ in the the C_{typeB} has reduced M and improved L. Therefore, we propose to adjust the size of the matrix, $A_{L\times W}$ according to the types of capacitive array. The modification to the matrix size does not have a significant impact on the overall area.



	M (%)	*L*
(a)	1.1984	5.5177
(b)	0.9564	5.4880
(c)	0.9546	5.4880
(d)	0.8560	5.5718
(e)	0.8560	5.6035

M: Maximum Capacitance Ratio Mismatch
L: Overall Correlation Coefficients

Figure 5.4: Experimental placements for 3-bit C_{typeA} in $A_{2\times4}$ and $A_{3\times4}$.

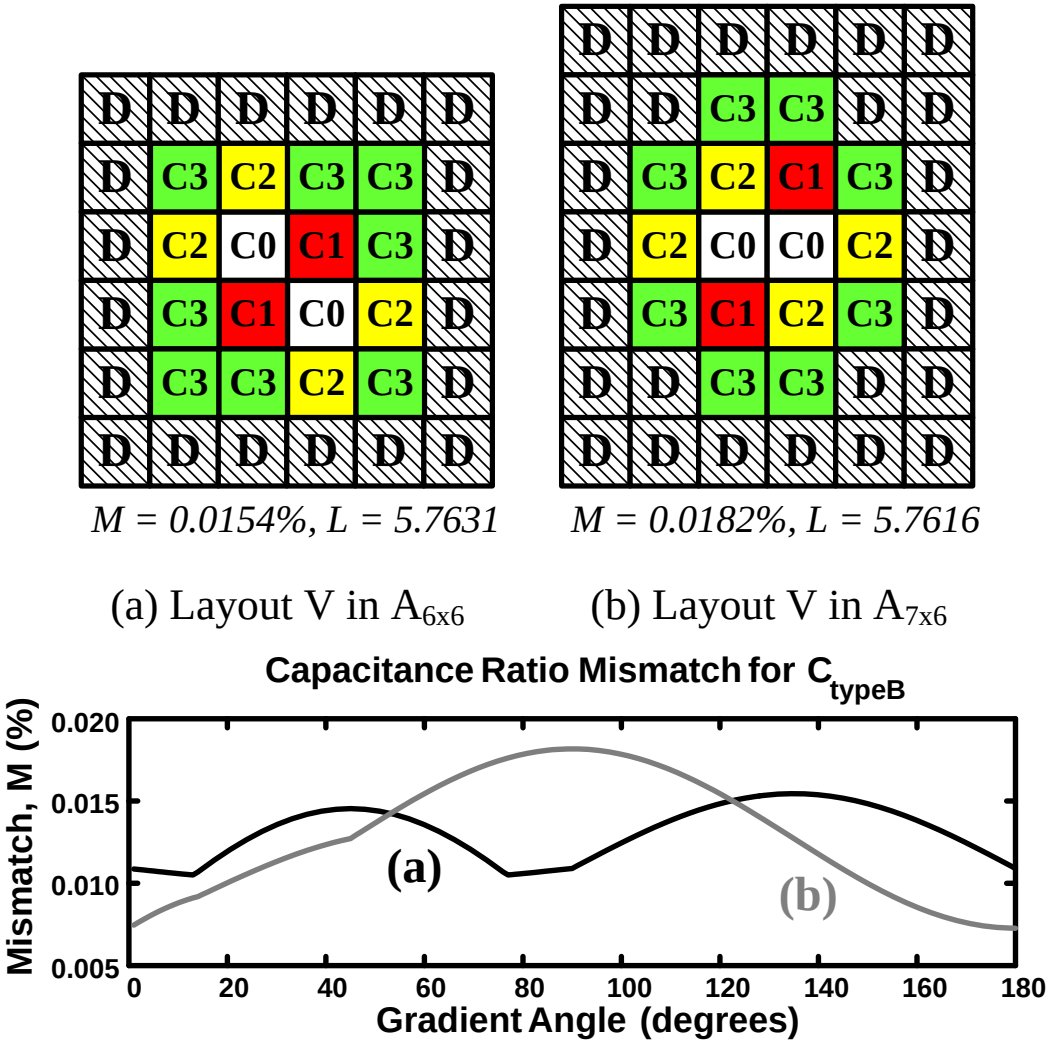


Figure 5.5: Experimental placements for 3-bits C_{typeB} capacitive arrays in $A_{6\times6}$ and $A_{6\times7}$.

5.3.2 Dummy capacitors placement using spatial weighting method

After the matrix has been adjusted to achieve minimal M, the next priority is the placement for the dummy unit capacitors. Although the dummy unit capacitors do not induce mismatches, their location affects the matching of the capacitive array. To minimize these mismatches, it is important to consider the placement for the dummy unit capacitors. C_D is computed based on the matrix size and the capacitive array. These dummy unit capacitors are first added into the perimeter of the capacitive array to act as adjacent structures and therefore minimizes the second-order lithographic errors. Two weighting methods are evaluated to determine the best choice for prioritizing the location for the remaining dummy unit capacitors in $A_{L\times W}$.

The distance weighting method was first used for the matrix to pair-sequence transformation [91, 99]. The distance from the entry $a_{l,w}$ to the center of $A_{L\times W}$ is defined as

$$d_{l,w} = \sqrt{(x_l - x_c)^2 + (y_w - y_c)^2}, \tag{5.10}$$

where (x_l, y_w) is the coordinate of $a_{l,w}$ and (x_c, y_c) is the coordinate of the center entry of $A_{L\times W}$. The entries with the same distance are classified into the same weight and these weights are prioritized from the shortest distance to the longest distance.

The spatial weighting method is based on the spatial correlation model [92]. $L_{l,w}$ denotes the sum of the correlation coefficients between the entry $a_{l,w}$ and the rest of dummy unit capacitors. Due to the symmetry of the matrix, the entries with the same total correlation coefficient are classified into the same weight and these weights are prioritized from the highest total spatial correlation coefficient to the lowest total spatial correlation coefficient. Figures 5.6(a) and (b) show examples of the completed entry assignment using the distance weighting method and the

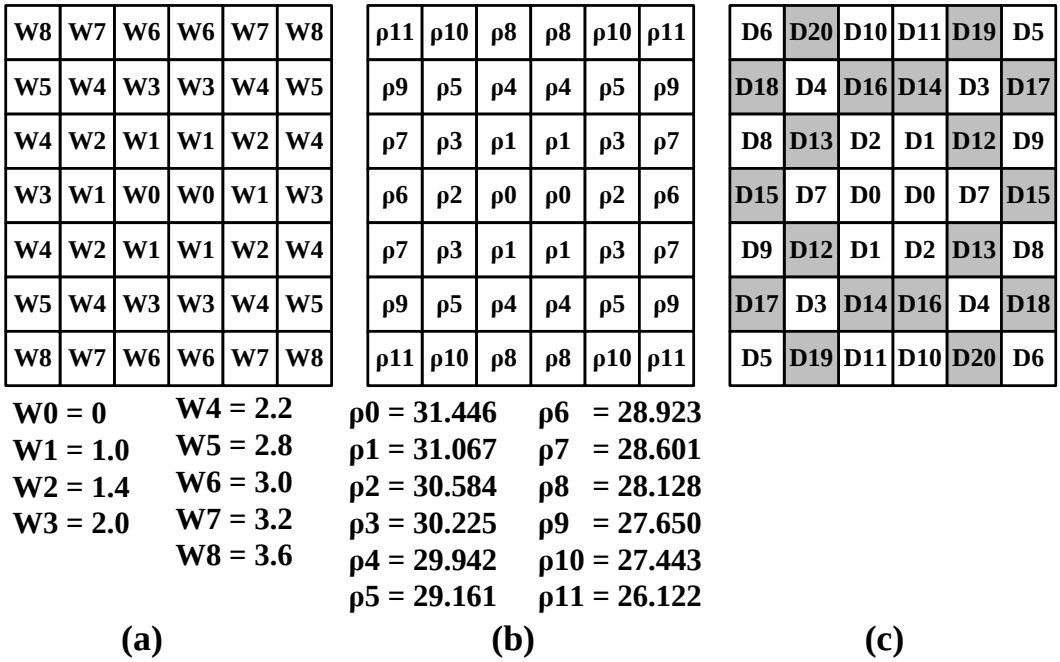
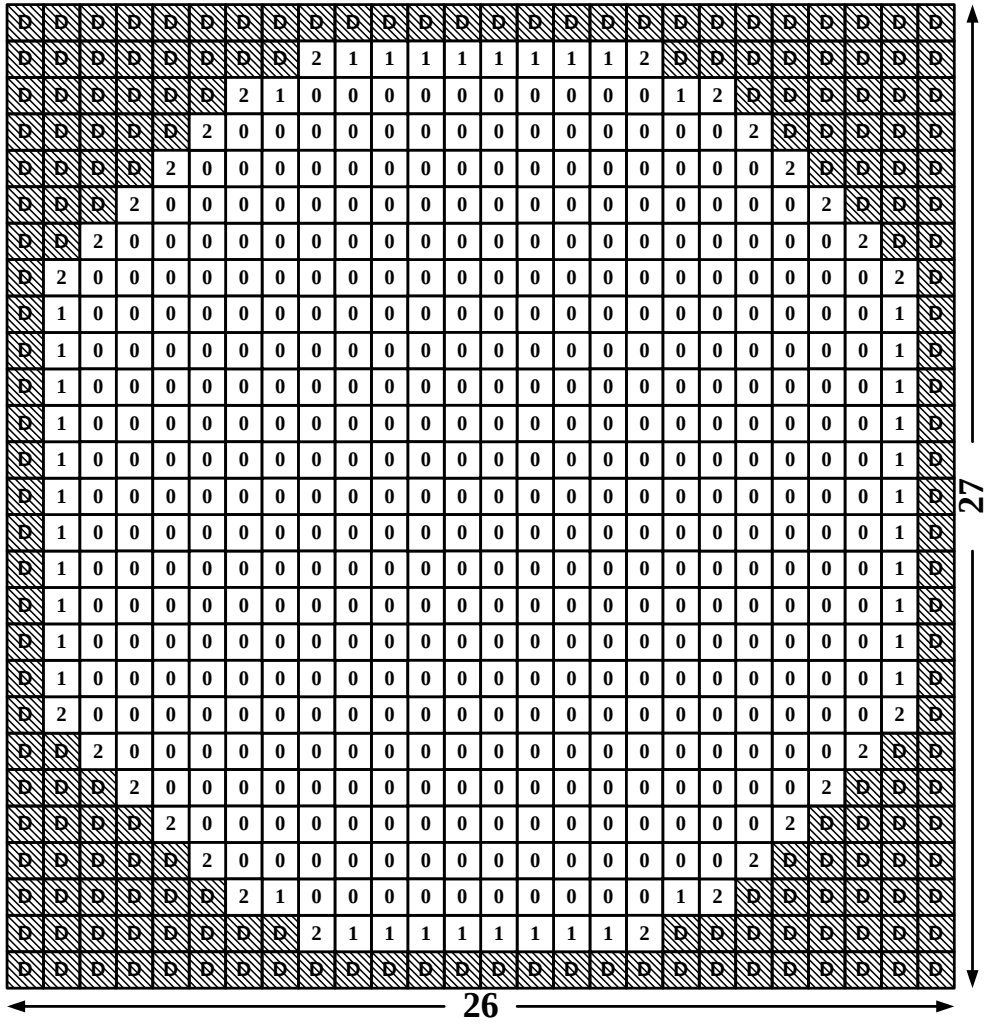


Figure 5.6: Illustrations of entry weight definitions (a) Distance weight (b) Spatial correlation weight (c) Diagonal weight.

spatial weighting method for the matrix $A_{7\times6}$, respectively. Note that $W0$ and $\rho0$ denote the shortest $d_{l,w}$ and highest $L_{l,w}$, respectively. Comparing the distance weighting method and the spatial weighting method, the latter method provides a clearer differentiation between the different types of entries. Therefore, the spatial weighting method is used for the placement of the dummy unit capacitors. The dummy unit capacitors are assigned starting from the smallest $L_{l,w}$ so that the capacitive array is able to achieve the maximal L in $A_{L\times W}$. A placement layout of the dummy capacitors for a 9-bit C_{typeA} capacitive array is shown in figure 5.7.



C	E	E_i/E_{i-1}
$C_0 = 1$	$E_0 = 0$	-
$C_1 = 1$	$E_1 = 0$	-
$C_2 = 2$	$E_2 = 0$	-
$C_3 = 4$	$E_3 = 0$	-
$C_4 = 8$	$E_4 = 0$	-
$C_5 = 16$	$E_5 = 4$	-
$C_6 = 32$	$E_6 = 6$	1.5
$C_7 = 64$	$E_7 = 12$	2
$C_8 = 128$	$E_8 = 24$	2
$C_9 = 256$	$E_9 = 48$	2

Figure 5.7: Placement dummy unit capacitors and dummy edge computation for 9-bit C_{typeA} capacitive array with dummy unit capacitors in $A_{27\times26}$.

5.3.3 Capacitive-array placement using diagonal weighting method

The next priority is the placement of capacitive array, C. According to the experiment in Section 5.3.1 and the spatial weighting method, a diagonal weighting method for the placement of capacitive array is proposed.

In the diagonal weighting method, a pair of two diagonal entry weights is defined to be diagonally opposite and equidistant with respect to the center of $A_{L\times W}$. This method is broken down into the following steps.

1. The first pair of entry weights in C_{typeA}, denoted as $D0$, is the first two entries closest to the center of the matrix, $A_{odd\times even}$. Figure 5.8(a) illustrates the first pair of entry weights, $D0$ in $A_{7\times 6}$.
2. The next entry pair, $D1$, is placed one unit distance away from the previous pair, $D0$, starting clockwise from the 12-o'clock position. $D2$ is then placed mirroring $D1$ about the center of the matrix.
3. Step (2) is repeated iteratively where the subsequent odd-entry pairs are placed in clockwise order from the 12-o'clock position at $\sqrt{2}$ unit distance away from the previous pair of odd-entry diagonal weights. The following even-entry pair is placed mirroring the previous odd-entry pair. This sequence repeats till the entry pairs reach the boundary of the dummy unit capacitors. Figure 5.8(b) illustrates the location of entry pairs, $D1$ to $D6$ in $A_{7\times 6}$. It is noted that the elements placed resemble the alphabet 'X'.
4. The next pair of entry weights, $D7$, is placed to the nearest empty entry clockwise from the 3-o'clock position with respect to the center of the matrix.
5. The following even-entry pair, $D8$, is placed clockwise from the 3-o'clock position $\sqrt{(2i+k_x)^2+k_y^2}$ unit distance away from the center of the matrix, where i increments from 1 and (k_x, k_y) is equivalent to (0.5, 1).

6. The subsequent even-entry pair, $D10$, is then placed diagonally opposite to $D8$ with respect to the diagonal line forming the bottom right leg of the 'X'. All subsequent even-entry pairs are then placed sequentially above and below this diagonal line until they reach the boundary of the dummy unit capacitors.
7. The corresponding odd-entry pairs are placed mirroring the even-entry pairs about the y-axis.
8. Steps (4)-to-(7) are repeated iteratively until Step (4) reaches the boundary of the dummy unit capacitors.
9. The remaining diagonal entry weights are defined using the distance weighting method [99]. Figure 5.6(c) shows an example of completed assignment with diagonal weighting method for matrix $A_{7\times6}$.

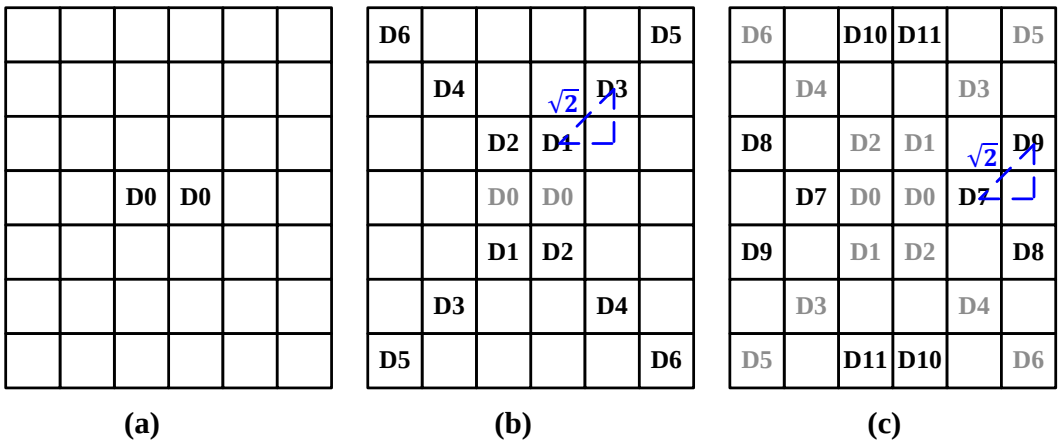


Figure 5.8: Illustrating the procedure of defining diagonal weights.

The diagonal weighting method for the C_{typeB} is similar to C_{typeA} except that the first two pairs of entry weights, $D0$ and $D1$, are selected from the 12-o'clock and 3-o'clock positions at the closest distance to the center of the matrix $A_{even\times even}$ and (k_x, k_y) is equivalent to (1.5, 0.5).

A capacitor pair-sequence is formed by iteratively pairing two unit capacitors in C, starting from C_0 to C_N, which is modified from [99]. Similarly, a diagonal pair-sequence is formed starting from $D0$. Then, the capacitor pairs are assigned to the corresponding diagonal pairs. Figure 5.9 shows the placement of C_{typeA} in $A_{L\times W}$.

The proposed placement method for capacitive array ensures that unit capacitors in C_N are placed adjacent sides to the rest of unit capacitors and allows C_N to be evenly distributed across the matrix. Since the majority of unit capacitors from C_2 to C_{N-1} are surrounded by C_N, electrical mismatch is minimized. It is assumed that there are negligible far range fringing effects from capacitors diagonal to the unit capacitor. Compared to Hakkarainen *et al.*'s method, the proposed method does not require additional dummy capacitors to improve the electrical matching [103].

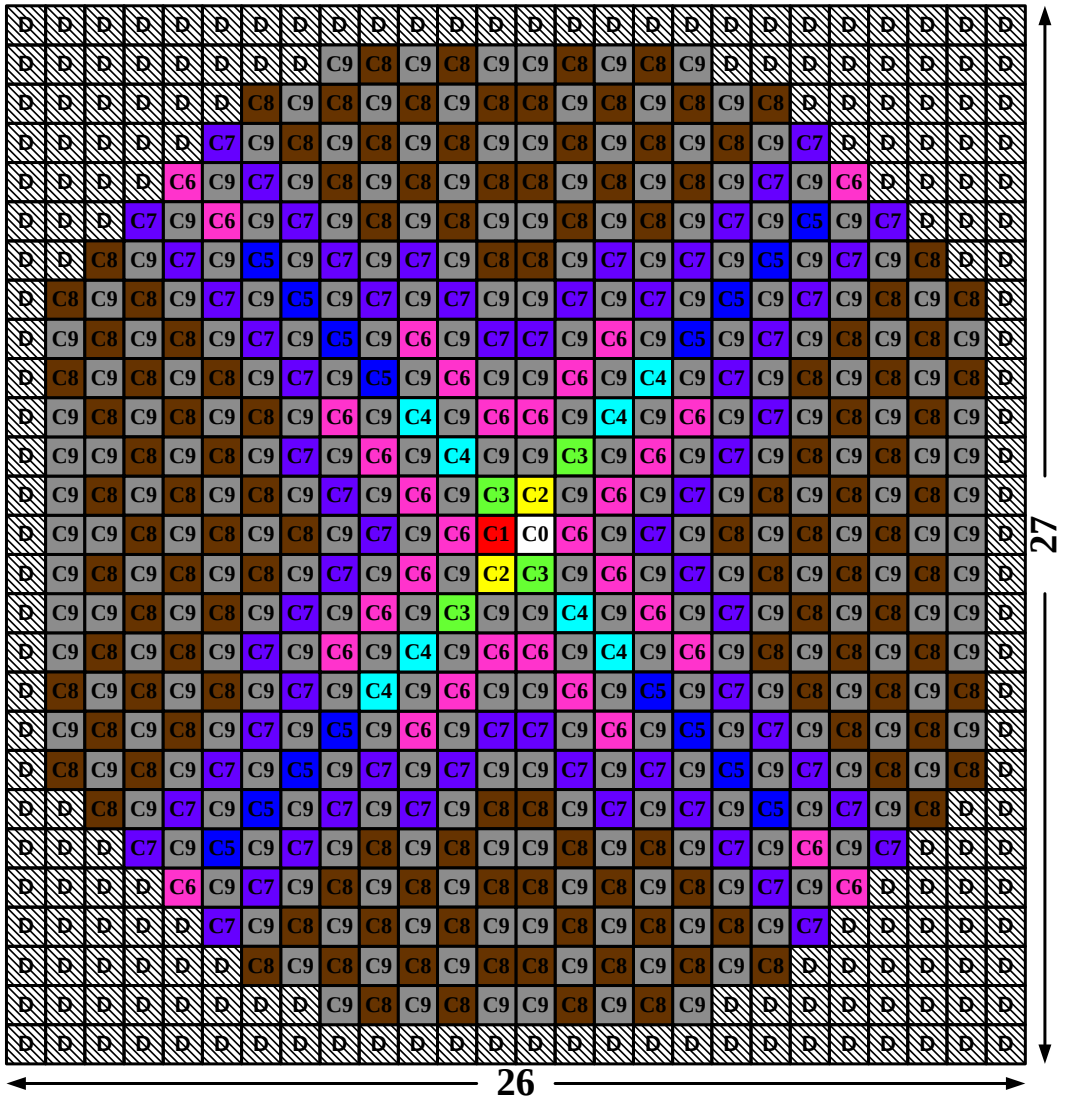


Figure 5.9: The placement result of 9-bit C_{typeA} capacitive array with dummy unit capacitors in $A_{27\times26}$.

5.3.4 Homogenizing algorithm with edge weighting method

To further improve the electrical mismatch for unit capacitors adjacent to the dummy capacitors, we focus on the optimization of the placements of these unit capacitors such that the fringing field effects are distributed across the capacitive array in a binary fashion.

Any entry, $a_{l,w}$ with an active unit capacitor, is assigned with an edge weight, which is denoted by $E_{l,w}$, where $E_{l,w}$ is the sum of dummy unit capacitors that are placed adjacent side to the entry $a_{l,w}$. Let E_c denote a set of edge weights belonging to the capacitive array with a ratio $E_{c,0} : E_{c,1} : E_{c,2} : \ldots E_{c,j} : \ldots : E_{c,N}$, where $E_{c,j}$ is the summation of all $E_{l,w}$ belonging to C_j. Let E denote a set of edge weights with a ratio $E_0 : E_1 : E_2 : \ldots E_j : \ldots : E_N$, where E_j is defined as

$$E_j = \frac{E_{total}}{2^{j+1}} + \frac{2^{j+1} + 2 - mod(E_{total} - (2^{j+1} - 2), 2^{j+1})}{2^{j+1}}, \tag{5.11}$$

and E_{total} denotes the sum of all the edge weights in $A_{L\times W}$. E_j provides an estimated number of unit capacitors from C_j that is required to be placed adjacent side to dummy unit capacitors. The goal is to ensure that the ratio between E_j and E_{j-1} is close to 2 and $E_{c,j}$ is equivalent to E_j. This method allows a better distribution of fringing fields amongst the capacitive array and improves the overall electrical matching. Figure 5.7 provides an example of dummy edge computation for a 9-bit C_{typeA} capacitive array.

After an initial placement has been generated, a homogenizing algorithm is initialized and $E_{l,w}$ entries, which are greater than zero, are swapped to meet the goal (the pseudocode is shown in Algorithm 1). We adopt a look-up table to speed up the swapping process and update the pair-sequence order.

Algorithm 1 Homogenization

Input: $C, E, A_{L\times W}$
Output: $A_{L\times W}$

while $E \neq E_c$ **do**
  for $i = 0$ to N **do**
    while $E[i] > E_c[i]$ **do**
      Search for highest diagonal entry weight $\in C_i$;
      Search for lowest diagonal entry weight $\in C_j$ whose $E[j] < E_c[j]$ and $j > i$;
      Swap the entry pair-sequence and update E_c
    end while
  end for
end while

5.3.5 Routing

The star-like placement technique allows the capacitors C_N and C_{N-1} to be distributed evenly and diagonally across the layout. This placement allows "rectangular and diagonal (45°)" wiring technique to be used so that a simple and symmetrical routing can be achieved. Each capacitor would only require one to two rectangular wires and several diagonal (45°) wires for routing. To avoid any congestion, the rectangular wires and the diagonal wires can be drawn on different metal layers. Furthermore, the DAC switches, as shown in figure 5.1, can be sub-divided into 4 smaller sets of switches and placed at different side of the array so that the long rectangular wires can be totally removed. Further protection against routing parasitics is provided by a grounded metal shield over the entire array with one hole per unit capacitor to access each bottom plate [54]. While this method adds extra parasitic capacitance from both the bottom plate and the top common plate to ground, the shielding makes the weighted capacitors insensitive to routing parasitics. Figure 5.10 illustrates an example of a 3-bit C_{typeB} capacitive array, which was built by connecting metal-insulator-metal (MIM) capacitors with routing below the shielding layer.

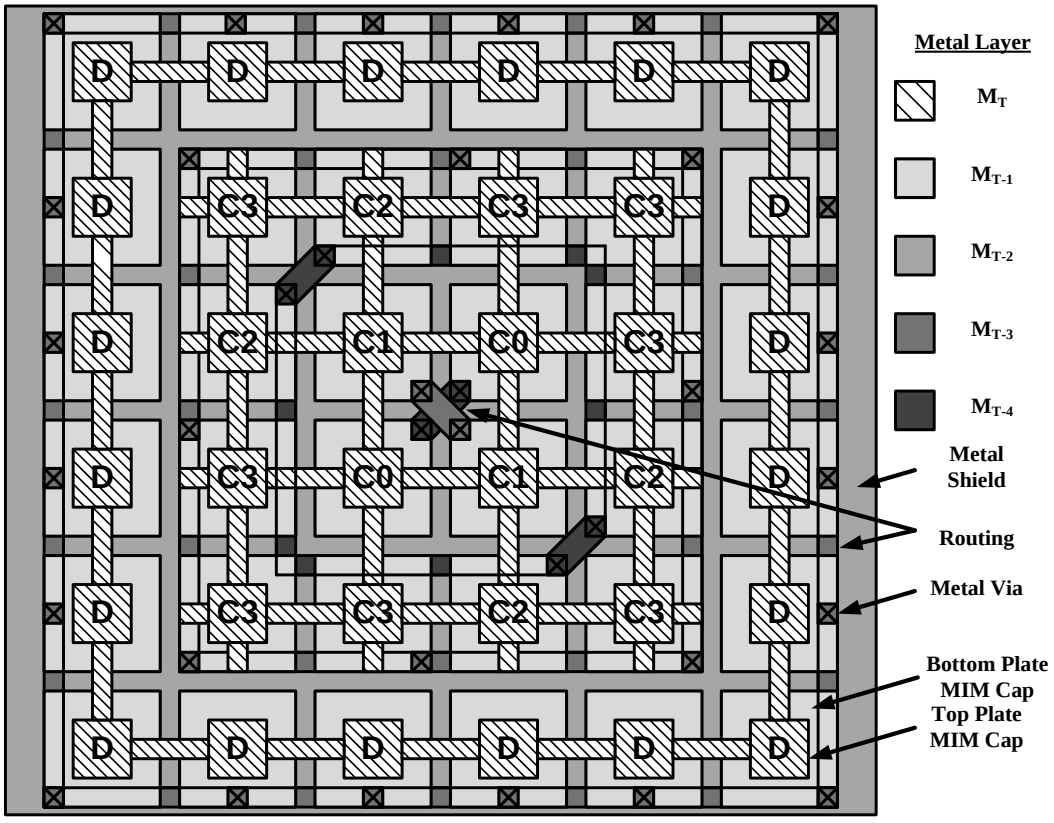


Figure 5.10: Layout details showing the parasitic shielding and 45° routing used in 3-bits C_{typeB} capacitive array layout.

5.3.6 Example of a 9-bit C_{typeA} CBW DAC

An example of a capacitor placement for 9-bit C_{typeA} with dummy unit capacitors in $A_{27\times26}$ is shown in figure 5.11. The capacitive array is surrounded by the dummy unit capacitors to minimize the second-order lithographic errors and the proximity effects. The dummy unit capacitors are placed strategically to maximize the overall spatial correlation coefficient for the capacitive array. The placement resembles a star-like pattern and thus maximizing the overall spatial correlation coefficient as well as to achieve a simple and symmetrical wiring connection. The coloured rectangular wires and diagonal wires represent the wiring of the capacitors. The wiring scheme shows that the connections are much simpler and symmetrical compared to the routing methods presented in [91, 99]. The adjustment of the unit capacitors from C_5^A to C_9^A achieves a more homogeneous distribution of fringing fields at the edge of the capacitive array within C_{typeA}. This minimizes the mismatch due to the unequal fringing mismatch.

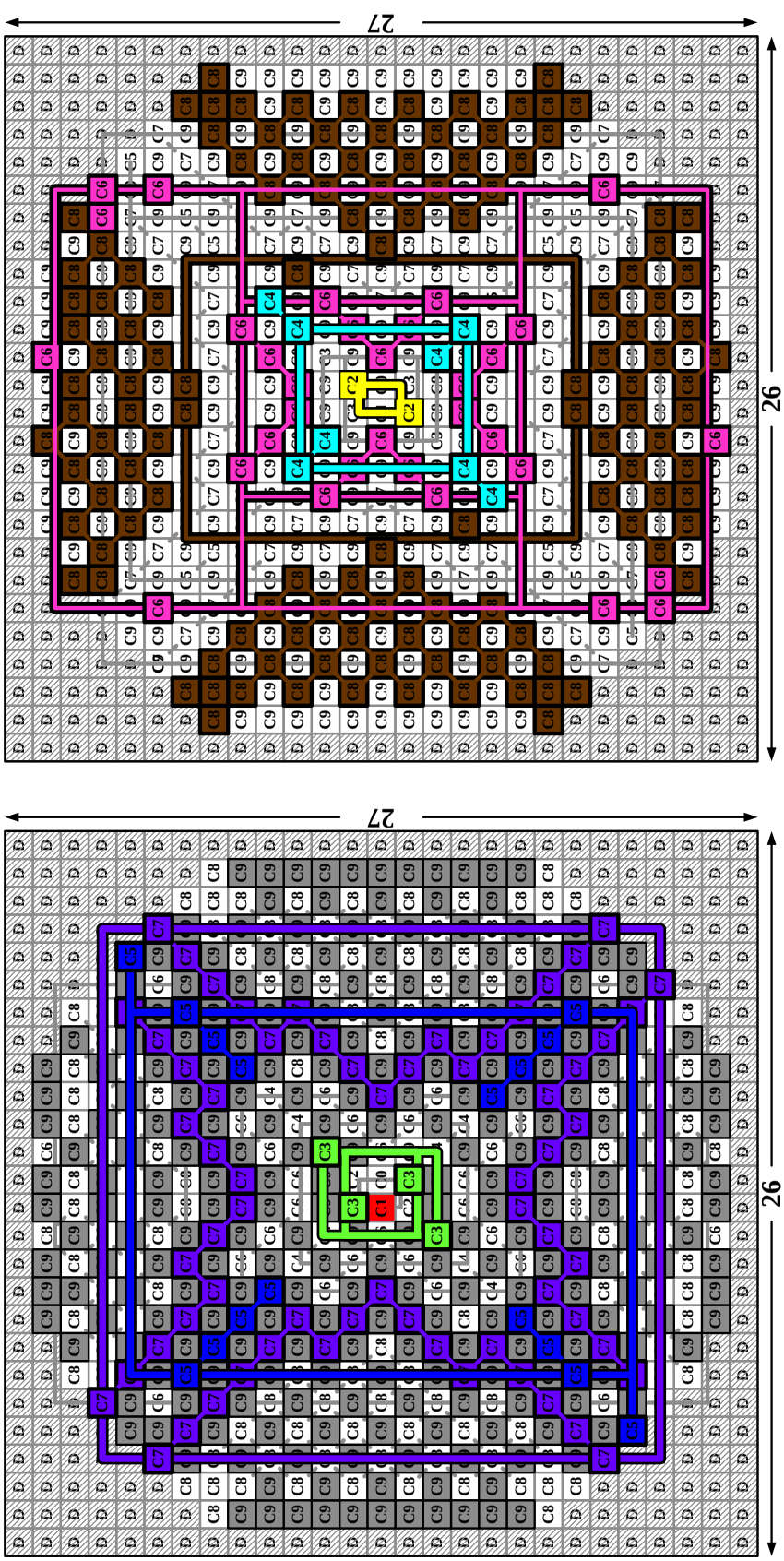


Figure 5.11: Final placement result of 9-bit C_{typeA} capacitive array with dummy unit capacitors in $A_{27\times26}$. The coloured rectangles and diagonal wires represent the routing connection of the capacitors.

5.4 Experimental results

The proposed placement algorithm for the binary-weighted capacitive DAC was implemented in the Matlab® programming language and simulated on a 3.00-GHz Intel Core2 Duo computer with 4.0 GB-RAM.

In this experiment, the proposed placement has been implemented on the 2-to-12-bit C_{typeA} and the 2-to-11-bit C_{typeB} arrays. The capacitive arrays with non-square placements were placed in a square matrix with the use of additional dummy capacitors so that it can achieve better matching than a rectangular matrix. For each type of the capacitive arrays, the value of the capacitance mismatch ratio, M, the value of the overall correlation coefficient, L, and the computational runtime are listed. The runtime is acquired based on an average of 100 iterations. Table 5.1 shows the experimental results for the 2-to-12-bit C_{typeA} and the 2-to-11-bit C_{typeB} capacitive arrays.

From our experimental results in Table 5.1, the C_{typeB} capacitive array achieves a smaller M than the C_{typeA} capacitive array for resolutions below 8-bit. M begins to increase for both types of capacitive array when the resolution increases beyond 9-bit resolutions. As seen in (5.8) under the Section 5.2.3, the parameters, t_o, γ, S_x, S_y, W and L affect the effective capacitance of the unit capacitor due to the variation of the oxide thickness at different locations. Therefore, the second term in (5.8) has a greater influence on the variation of the effective oxide thickness when the size of the matrix increases. From our experimental results in Table 5.2, M is minimized through increasing oxide thickness, t_o, or decreasing oxide gradient, γ, for higher resolution DACs. However, t_o and γ are process dependent parameters, thus the size of unit capacitor (W and H) and the spacing between unit capacitors (S_x and S_y) can only be adjusted to minimize M for the higher resolution DACs. Our proposed

routing method allows the spacing between the unit capacitors to be minimized, which also minimizes M. Comparing the experimental results (Table 5.1) for the layout using the methods in [96, 97], which are one of the common common-centroid layouts, our proposed placement has increased the degree of dispersiveness and reduced the capacitance mismatch ratio for both types of capacitive arrays.

Table 5.3 compares our works with other state-of-the-art works [92, 99]. Figure 5.12 shows the mismatch variation with the gradient angle for the three different placements of the SAR_9bit. From these results, our proposed placement strategy achieves a smaller capacitance mismatch ratio and a faster computational runtime with a comparable overall spatial correlation coefficient.

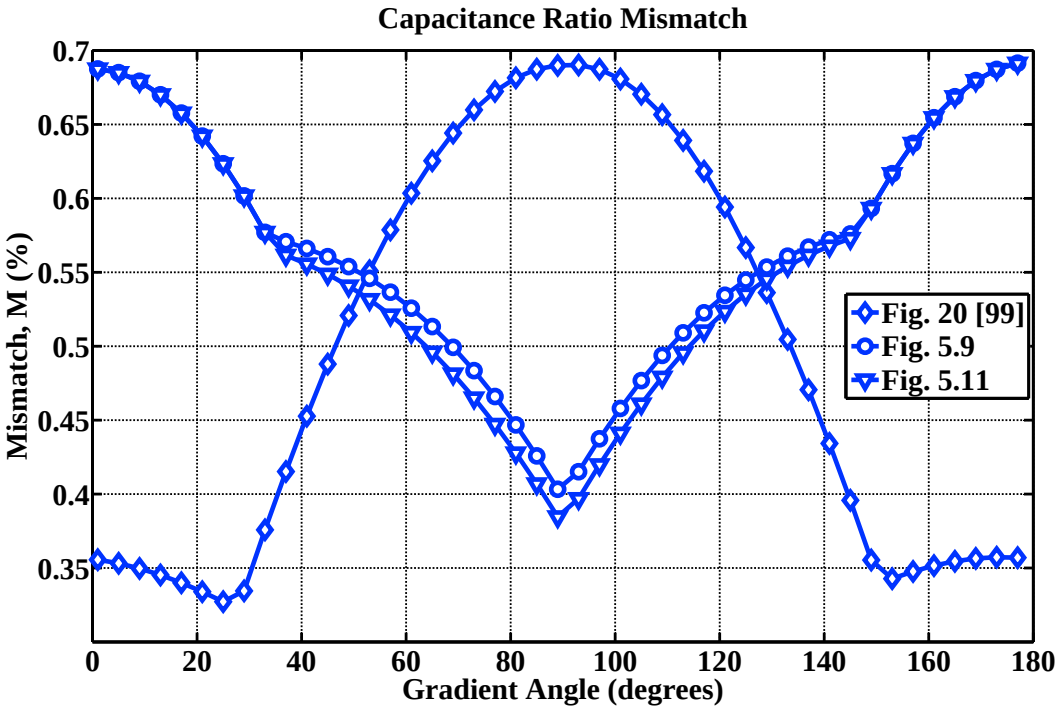


Figure 5.12: Oxide-gradient-induced mismatches of three different placement for 9-bit C_{typeA} capacitive array.

Table 5.1: Experimental Results with our proposed placement and common-centroid placement in [97]. (M: capacitance mismatch ratio; L: overall correlation coefficients)

C_{typeA} Capacitive Array									
Array Name	Matrix Size	Method 1 [97]		Method 2 [97]		Matrix Size	This Work		Time (s)
		M^1	L^2	M^1	L^2		M^1	L^2	
SAR_2bit	2×2	1.103	2.727	1.102	2.762	5×4	0.692	2.762	0.1
SAR_3bit	2×4	2.264	5.203	1.103	5.502	5×6	0.692	5.604	0.1
SAR_4bit	4×4	3.345	8.556	1.103	9.263	7×6	0.692	9.326	0.1
SAR_5bit	4×8	5.619	12.113	1.103	13.707	9×8	0.692	13.978	0.1
SAR_6bit	8×8	7.984	16.381	1.103	19.128	11×10	0.692	19.408	0.1
SAR_7bit	8×16	12.706	19.898	1.103	24.653	15×14	0.692	25.331	0.2
SAR_8bit	16×16	17.926	23.729	1.103	30.913	19×18	0.692	31.692	0.3
SAR_9bit	16×32	28.468	25.363	1.120	35.381	27×26	0.692	37.875	1.0
SAR_10bit	32×32	40.963	27.406	1.539	41.228	35×34	1.030	42.554	11.2
SAR_11bit	32×64	68.226	26.913	3.214	42.477	49×48	1.400	47.012	35
SAR_12bit	64×64	105.565	27.990	4.786	45.705	67×66	3.899	48.589	440

C_{typeB} Capacitive Array									
Array Name	Matrix Size	Method 1 [97]		Method 2 [97]		Matrix Size	This Work		Time (s)
		M^1	L^2	M^1	L^2		M^1	L^2	
SAR_2bit	2×4	0.010	2.865	0.010	2.865	6×4	0.015	2.872	0.1
SAR_3bit	4×4	0.025	5.651	0.015	5.740	6×6	0.017	5.765	0.1
SAR_4bit	4×8	0.068	9.163	0.044	9.409	8×8	0.026	9.550	0.1
SAR_5bit	8×8	0.133	13.283	0.066	14.009	10×10	0.066	14.135	0.1
SAR_6bit	8×16	0.336	17.281	0.178	18.843	14×14	0.131	19.383	0.2
SAR_7bit	16×16	0.619	21.257	0.267	24.580	18×18	0.269	24.746	0.3
SAR_8bit	16×32	1.492	23.385	0.712	24.580	26×26	0.358	30.861	0.9
SAR_9bit	32×32	2.719	25.537	1.085	34.401	34×34	1.085	34.774	10.4
SAR_10bit	32×64	6.572	25.296	2.855	36.188	48×48	1.354	39.880	32
SAR_11bit	64×64	12.402	26.394	4.367	39.258	66×66	4.022	40.125	400

[1]Assumes that the oxide thickness, t_o, is 40 nm, the oxide gradient, γ, is 10 parts per million and the width and length of a unit capacitor, C_o, is 25 μm (W) by 25 μm (H) with a spacing of 9.1 μm (S_x) by 2.6 μm (S_y) respectively.

[2]Assume that all unit capacitances have the same variances and the correlation coefficient between any two unit capacitors ρ_o is 0.9.

Table 5.2: Study of Capacitance mismatch ratio, M, on 8-to-11-bit C_{typeA} with varying oxide thickness, t_o and oxide gradient, γ

Oxide thickness, t_o (nm)		30	40	50	60
Name	Size	Capacitance mismatch ratio, M			
SAR_8bit	19 × 18	1.034	0.774	0.619	0.515
SAR_9bit	27 × 26	1.049	0.774	0.619	0.515
SAR_10bit	35 × 34	1.761	1.084	0.755	0.515
SAR_11bit	49 × 48	2.445	1.465	0.998	0.735
Oxide gradient, γ (ppm)		5	10	15	20
Name	Size	Capacitance mismatch ratio, M			
SAR_8bit	19 × 18	0.386	0.774	1.163	1.554
SAR_9bit	27 × 26	0.386	0.774	1.256	1.978
SAR_10bit	35 × 34	0.386	1.084	2.164	3.655
SAR_11bit	49 × 48	0.386	1.465	3.032	5.201

[1]Assumes that the width and length of a unit capacitor, C_o, is 25 μm (W) by 25 μm (H) with a spacing of 5.3 μm (S_x) by 5.3 μm (S_y) respectively.

Table 5.3: Comparisons of capacitance mismatch ratio, overall correlation coefficients, and running time for the heuristic algorithm [92], SA algorithm [99] and our work. (M: capacitance mismatch ratio; L: overall correlation coefficients)

Array	Matrix	Heuristic Algorithm [92]			SA Algorithm [99]			Matrix	This Work		
Name	Size	M^1	L^2	Time (s)	M^1	L^2	Time (s)	Size	M^1	L^2	Time (s)
SAR_8bit	16 × 16	0.800	32.074	602	0.695	32.111	235	19 × 18	0.692	31.692	0.3
SAR_9bit	32 × 16	1.077	38.072	20503	0.878	38.654	681	35 × 18	0.856	36.625	1.0
SAR_9bit	23 × 23	-	-	-[3]	0.695	39.243	820	27 × 26	0.692	37.875	1.0
SAR_10bit	32 × 32	-	-	-[3]	1.146	45.515	5130	35 × 34	1.030	42.554	11.2

[1]Assumes that the oxide thickness t_o is 40 nm, the oxide gradient γ is 10 parts per million and the width and length of a unit capacitor, C_o is 25 μm (W) by 25 μm (H) with a spacing of 9.1 μm (S_x) by 2.6 μm (S_y) respectively.

[2]Assume that all unit capacitances have the same variances and the correlation coefficient between any two unit capacitors ρ_o is 0.9.

[3]No result is reported

5.5 Summary

In conclusion, it is important to achieve a zero mean offset or zero systematic mismatch in the binary-weighted capacitive array as random mismatch cannot be totally eliminated. The proposed placement strategy considers the random mismatch and the four systematic mismatches (such as the first-order process gradient, the second-order lithographic errors, the proximity effects, the wiring complexity and the far range fringing fields effects) during the placement of the capacitive array. This results in a more symmetrical and common-centroid placement for the capacitive array, which is evident from the reduction of first-order oxide gradient. Additional dummy unit capacitors are placed adjacent to the capacitive array to reduce the second-order lithographic errors and the proximity effects. The capacitive array resembles a star-like placement so that it simplifies the wiring scheme and minimizes the number of asymmetrical wiring compared to existing works. A homogenization algorithm is proposed to equalize fringing mismatches among the capacitive array. The analytical approach has improved the computational runtime significantly while achieving comparable degree of dispersiveness compared to the state-of-the-art works.

Chapter 6

Capacitive-Array DAC Architectures for High Resolution SAR ADCs

6.1 Introduction

In Chapter 5, a placement strategy was developed to achieve an optimal layout for the CBW DAC. However, as the resolution of the SAR ADC increases, the input capacitance and the total number of unit capacitors in the CBW DAC increase exponentially and it is increasingly difficult to minimize both systematic and random mismatches. This also causes an exponential increase in power dissipation and a reduction of speed due to large charging time-constant.

To overcome these challenges, the BWA DACs have been recently reconsidered for the 8-to-10-bit SAR ADCs [58, 65, 104–106]. This architecture uses a fewer number of unit capacitors, reducing the layout area and mismatches as well as reducing the switching energy and the settling time. An attenuation capacitor, C_M, is used to separate the N-bit binary-weighted capacitive-array into a K-bit most significant bit (MSB) binary-weighted capacitive sub-array and a (N-K)-bit least significant bit (LSB) binary-weighted capacitive sub-array [57], where the required

attenuation capacitor, C_M, is

$$C_M = \frac{2^{N-K}}{2^{N-K}-1} C_o, \tag{6.1}$$

and C_o is the capacitance of the unit capacitor. The input capacitance and the switching power consumption can be further reduced by introducing an additional segmentation into the BWA DACs [63, 105, 107, 108].

The value of the attenuation capacitor, C_M is derived as in equation 6.1 such that the ratio between C_{K+1} and $\sum_{i=1}^{K} C_i \parallel C_M$ is 1:1, which results in a fractional value except when K is equal to 1. Due to the process variations and the finite lithography manufacturing grids, it is impossible to implement the value exactly [62, 109]. This results in a mismatch between C_{K+1} and $\sum_{i=1}^{K} C_i \parallel C_M$, which is further worsened due to the parasitic capacitances. These undesirable non-ideal effects would result in the code-dependent error, thus degrading the ADC's performance [62]. As shown in figure 6.1, the green, blue and red lines indicate the characteristics of the ideal DAC, the CBW DAC and the BWA DAC, respectively. The parasitic capacitances in the CBW DAC cause a gain error (blue line) but has no effect on the ADC's linearity. For the BWA DAC, the parasitic capacitances in the MSB and LSB sub-arrays are completely uncorrelated and this causes different gain error in the MSB and LSB sub-arrays (a disjoint function, as shown in the red line). However, since the gain error in the LSB sub-array is a code-dependent error, which will degrade the linearity of the ADC.

In order to compensate for these non-linear effects from the parasitic capacitances and the fractional errors in the attenuation capacitors, one of the common calibration techniques is to use an extra capacitive-array DAC to improve the linearity of the main capacitive-array DAC [105, 106]. The DAC calibration technique requires an additional voltage reference, V_{CM} to correct the mismatch between the sub-arrays.

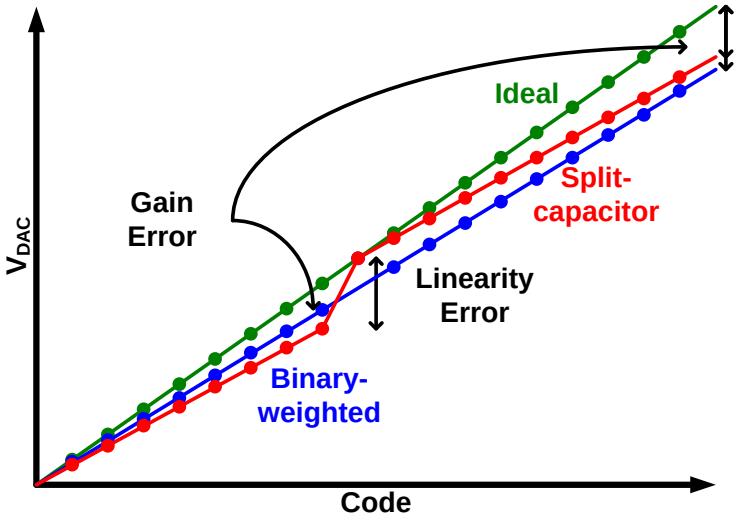


Figure 6.1: Linearity of the CBW and BWA DACs.

An additional calibration circuit is needed to minimize the comparator's offset; otherwise, this offset will result in a mismatch in the DAC, causing a linearity error. So far, this type of calibration technique has been shown to be ineffective at high resolution SAR ADCs [108, 110]. Therefore, it is important to design the BWA DAC with an optimal segmentation degree (i.e. the number of bits in the MSB sub-array) so that the mismatch can be corrected easily.

In the first part of the chapter, the total area, the power consumption and the linearity of the CBW and BWA DACs will be discussed. Based on the analyses, two new types of split capacitive-array DAC are proposed. These architectures have optimized segmentation degree to reduce the area, the switching power consumption and improve the linearity compared to the CBW DAC and the BWA DAC. To have a fair comparison between all the DAC architectures, a 12-bit single-ended SAR ADC with charge-redistribution switching method will be used.

6.2 CBW DAC and BWA DAC

The CBW DAC and the BWA DAC architectures are discussed in Chapter 2 and the analysis of the switching power consumption for these architectures are discussed in Chapter 3. Figures 6.2(a) and 6.2(b) show the schematic diagram of a SAR ADC with the CBW DAC and a SAR ADC with the BWA DAC, respectively. The value of each capacitor in the CBW DAC is given by

$$C_i = 2^{N-i}C_o, \qquad 1 \leq i \leq N, \tag{6.2}$$

while the BWA DAC is divided into a K-bit MSB sub-array and a (N-K)-bit LSB sub-array, where the value of each capacitor is given by

$$C_i = \begin{cases} 2^{K-i}C_o, & 1 \leq i \leq K, \\ 2^{N-i}C_o, & K+1 \leq i \leq N, \\ C_o, & i = 0, \end{cases}$$
$$C_M = 2^{N-K}C_o, \tag{6.3}$$

where C_o is the capacitance of the unit capacitor.

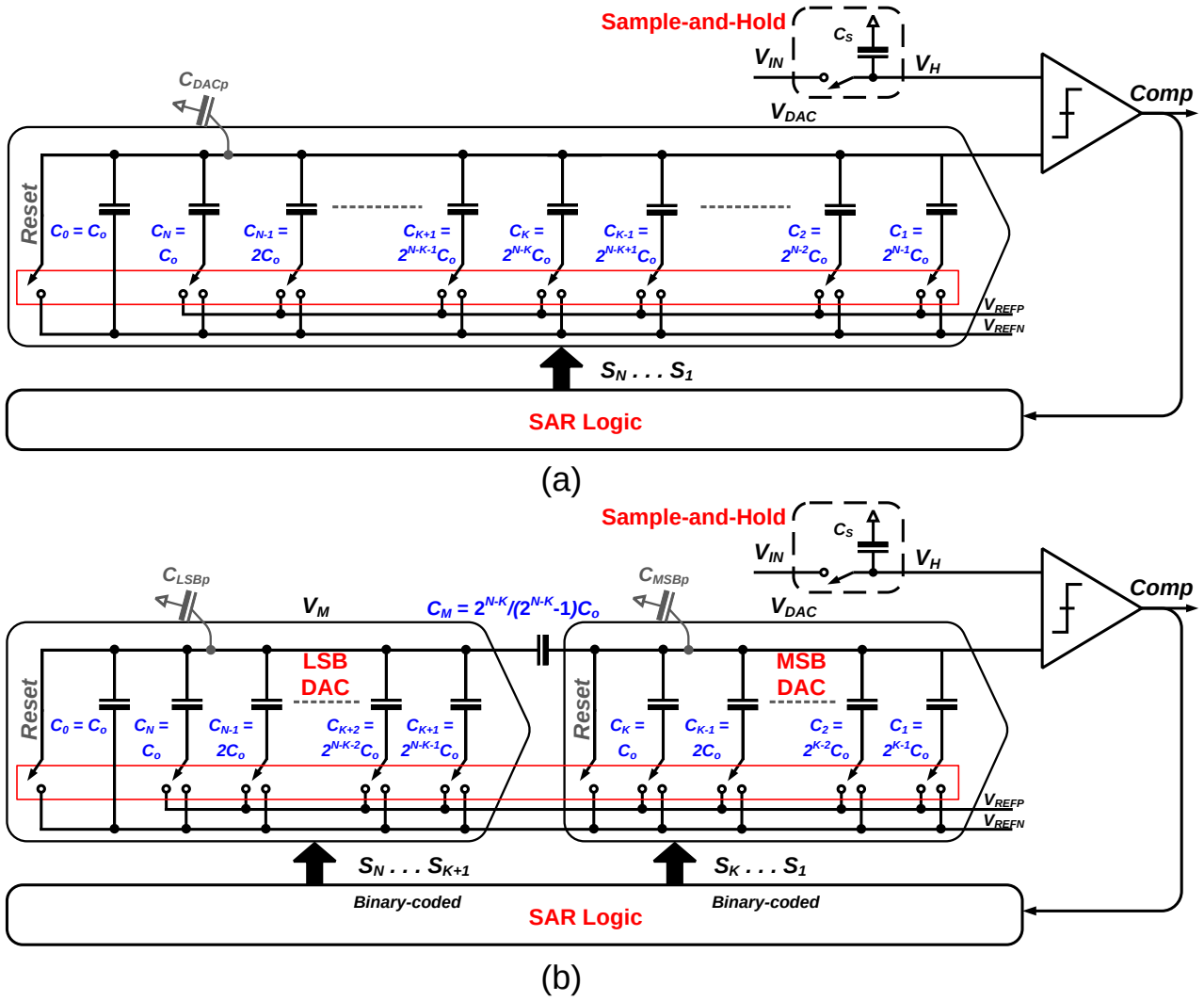


Figure 6.2: Schematic diagram of a single-ended N-bit SAR ADC using (a) the CBW DAC and (b) the BWA DAC.

6.2.1 Area requirement

The input capacitance and the total number of unit capacitors in the CBW DAC varies with different segmentation degrees in the BWA DAC. The total number of unit capacitors can be derived based on equation (6.3). As shown in figure 6.3, the BWA DAC uses the least number of unit capacitances when the segmentation degree is half of the DAC resolution (i.e. $N/2$). This is approximately equal to $2^{\lfloor N/2 \rfloor}C_o + 2^{\lceil N/2 \rceil}C_o$. Thus, this provides a $2\times$ to $2^{N/2-1}\times$ reduction compared to the CBW DAC.

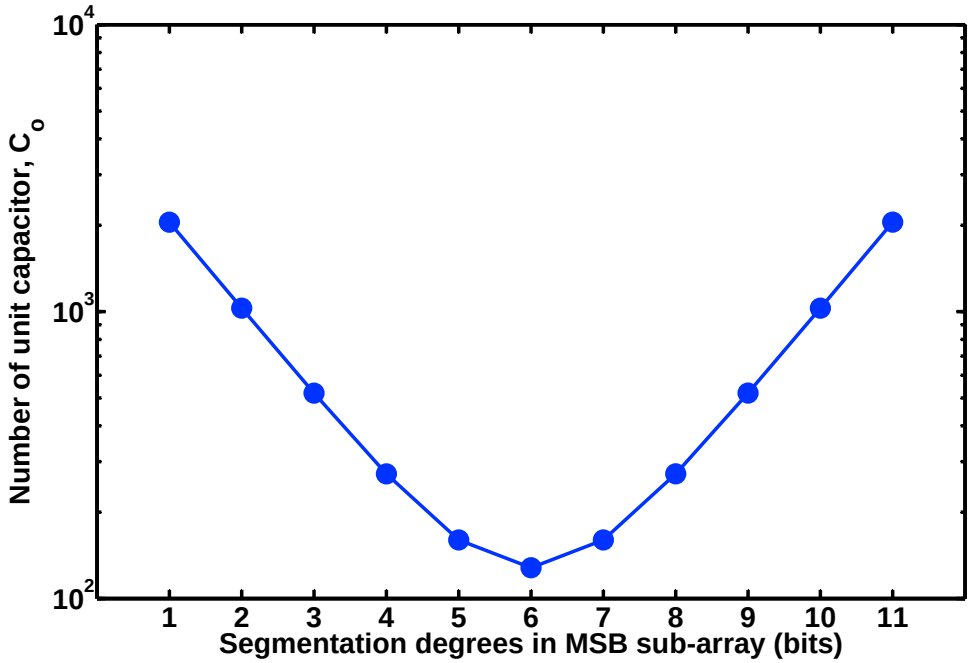


Figure 6.3: Total number of unit capacitor required for a 12-bit SAR ADC using the BWA DAC with different segmentation degrees.

6.2.2 Power consumption due to the capacitors' switching

The analysis of the switching power consumption for the CBW DAC and BWA DAC architectures are discussed in Chapter 3. The average switching energy, E_{avg}, for the 12-bit charge-redistribution SAR ADC using the CBW DAC is 2729.5 CV_{REF}^2. On the other hand, the average switching energy, E_{avg}, for the 12-bit charge-redistribution SAR ADC using the BWA DAC varies from 86.3 CV_{REF}^2 to 1365.0 CV_{REF}^2, as shown in figure 6.4. Significant power savings are achieved with segmentation degrees ranging from 4-to-8.

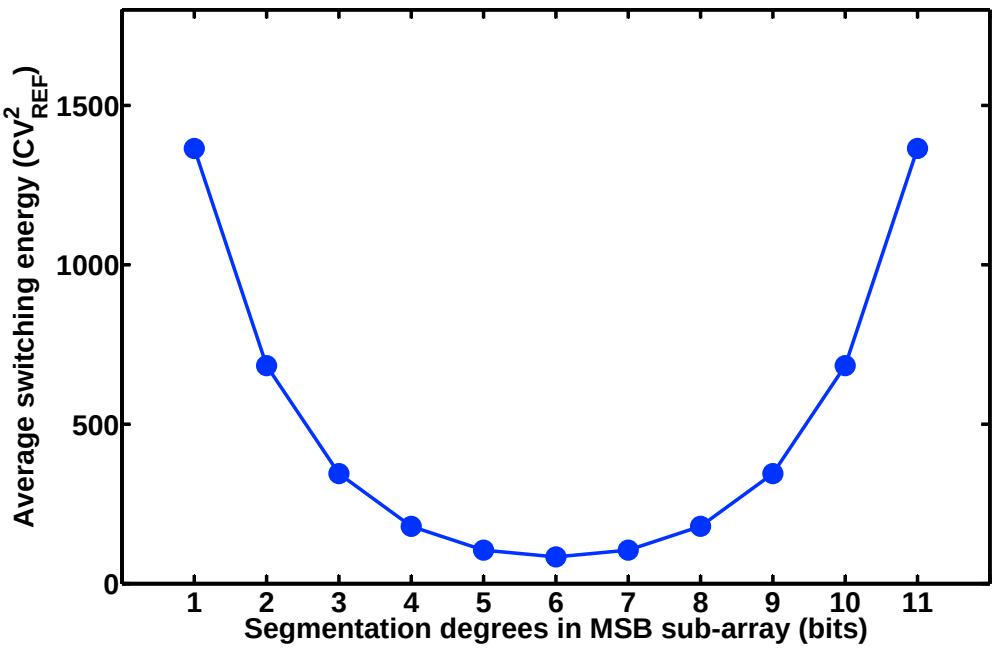


Figure 6.4: Switching energy consumption of a 12-bit charge redistribution SAR ADC using the BWA DAC with different segmentation degrees.

6.2.3 Linearity analysis

The SNDR is a measurement of the purity of the ADC's output signal and it provides a good indication of the overall linearity and dynamic performance of the ADC. In practice, the linearity of the DAC in the SAR ADC is affected by the matching properties of the capacitors as well as the parasitic capacitances. The minimum size of C_o is determined by the *kT/C* noise requirement, the minimum capacitor matching requirement or the design rules of the technology. In the high-resolution SAR ADCs (>10-bit), it is often limited by the minimum capacitor matching requirement. In this work, Monte Carlo experiments (based on 1000 simulations per experiment) were performed on the 12-bit charge-redistribution SAR ADC using the CBW DAC. This helps to determine the SAR ADC's dynamic performance. The unit capacitors and the attenuation capacitors were assumed to have a distributed Gaussian random profile with 5% top-plate and 10% bottom-plate parasitic capacitances, which has similar characteristics as the Metal-Insulator-Metal capacitors [109]. It should be noted that only the DAC non-idealities have been considered while all other blocks are assumed ideal, therefore the linearity of the ADC is equal to the linearity of the DAC.

In order to achieve a reasonable trade-off between performance and power, a general rule of thumb of SNDR greater than 68.3-dB (ENOB >11-bit) is required [111]. In this case, the ENOB is calculated based on the adjusted amplitude of the input waveform to compensate for the full-scale error, which results from the parasitic capacitances in the DAC.

6.2.3.1 CBW DAC

To determine the minimum size of the C_o for a 12-bit charge-redistribution SAR ADC using the CBW DAC, the Monte Carlo experiments were carried out. The standard deviations of the unit capacitors were varied from 0.5% to 5% with 0.5% increments. The results indicate that a maximum standard deviation of 1% would be sufficient to achieve a mean μ_{SNDR} of 71.83-dB (ENOB of 11.64-bit) with a standard deviation σ_{SNDR} of 1.07-dB. In the CBW DAC, the parasitic capacitances due to the capacitive DAC will only cause a gain error without affecting the linearity.

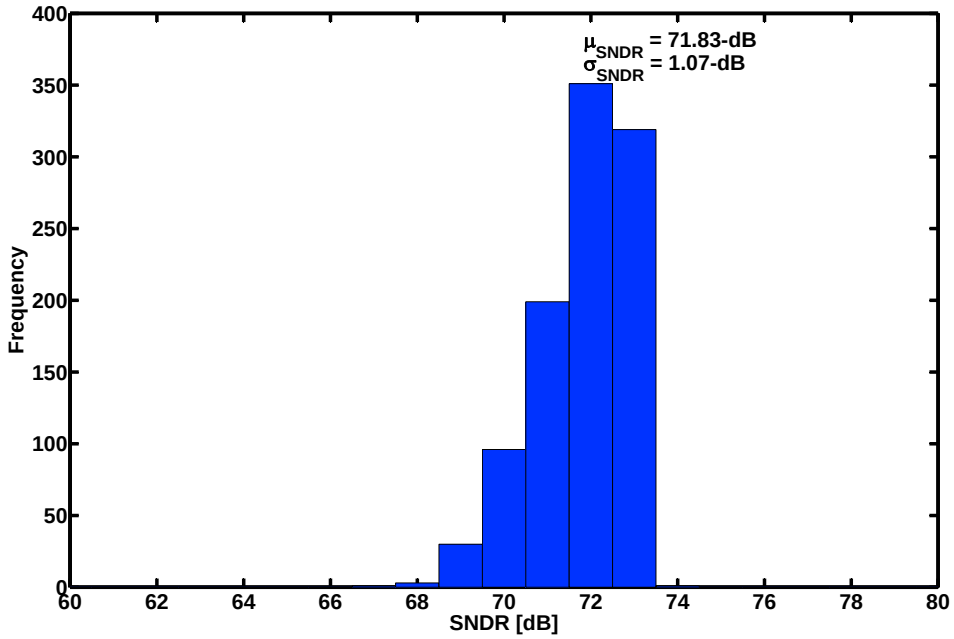


Figure 6.5: The histogram of the SNDR with 1000 Monte Carlo simulations for a 12-bit charge-redistribution SAR ADC using the CBW DAC with 1% standard deviation in the unit capacitor.

6.2.3.2 BWA DAC

In order to investigate the effect of the segmentation degree on the BWA DAC, Monte Carlo experiments were performed on a 12-bit charge-redistribution SAR and the results are shown in figure 6.6. The SNDR improves with increasing segmentation degrees in the MSB sub-array. The traditional approach of choosing a segmentation degree of six (around $N/2$) would not be able to meet the requirement, instead a segmentation degree of ten and above would be required.

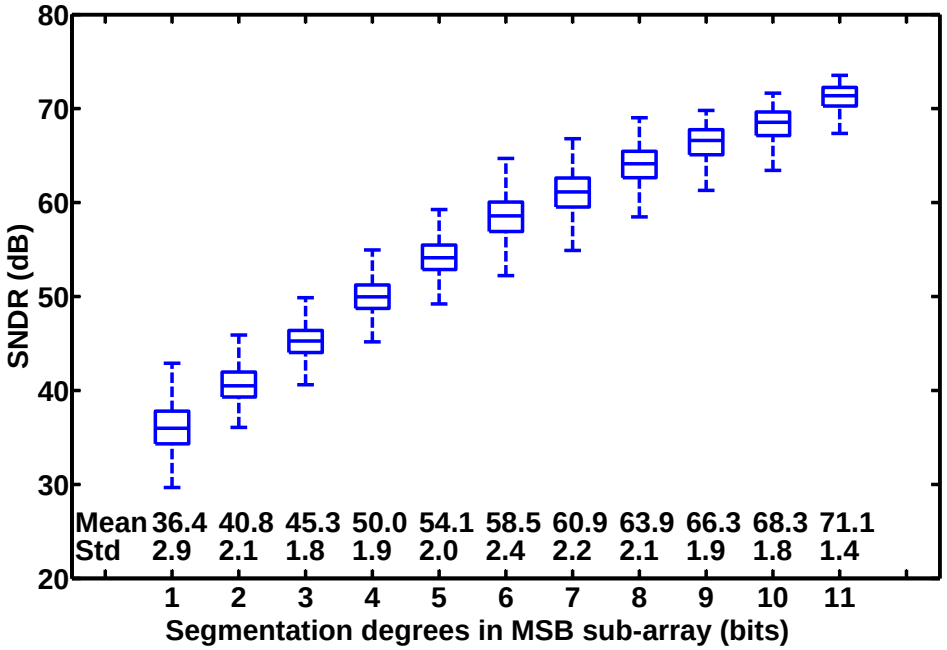


Figure 6.6: The histogram of the SNDR with 1000 Monte Carlo simulations for a 12-bit charge-redistribution SAR ADC using the CBW DAC with different segmentation degrees.

6.3 Architecture I - an improved binary-weighted split capacitive-array DAC

In order to improve the linearity of the BWA DAC, an optimum choice for the segmentation degree is required but such optimization does not readily improve the yield's variation. Therefore, an improved split-capacitive-array DAC architecture is proposed, as shown in figure 6.7. The attenuation capacitor is integer multiples of the unit capacitors as opposed to a fractional multiple in the BWA DAC architecture. This allows an easier implementation in the layout and also improves the variation in the SAR ADC. An optimized segmentation degree for the DAC architecture is determined based on the area, the switching power consumption and the linearity of the SAR ADC.

In the improved split-capacitive-array DAC, the capacitive-array is divided to a K-bit MSB sub-array and a (N-K)-bit LSB sub-array, but the value of each capacitor is given by

$$C_i = \begin{cases} 2^{N-i-1}C_o, & 1 \leq i \leq K, \\ 2^{N-i}C_o, & K+1 \leq i \leq N, \\ C_o, & i = 0, \end{cases}$$
$$C_M = 2^{N-K-2}C_o, \tag{6.4}$$

where C_o is the capacitance of the unit capacitor.

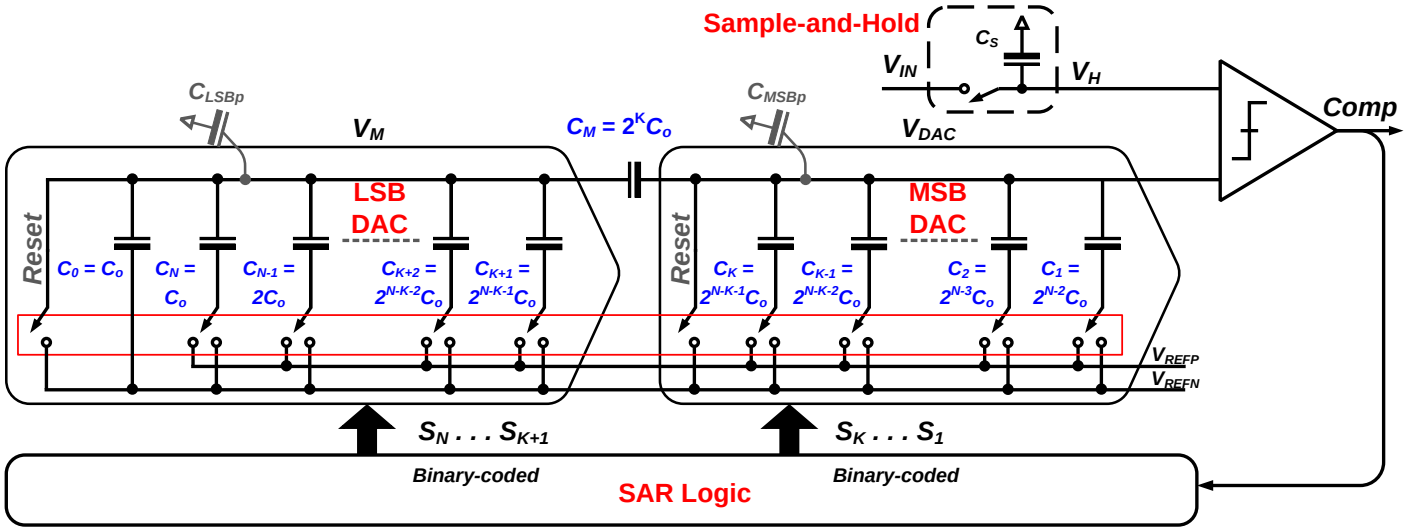


Figure 6.7: Schematic diagram of a single-ended N*-bit SAR ADC using the proposed 2-segmented split capacitive array DAC.*

6.3.1 Area requirement

This architecture has an input capacitance of $2^{N-1}C_o$, which has a $2\times$ reduction in the input load capacitance compared to the CBW DAC. The total number of unit capacitors can be derived based on equation (6.4). As shown in figure 6.8, the required total number of unit capacitors decrease with an increasing segmentation degree. It can be concluded that there would not be any significant decrease in the number of unit capacitors when the segmentation degree is greater than $N/2$.

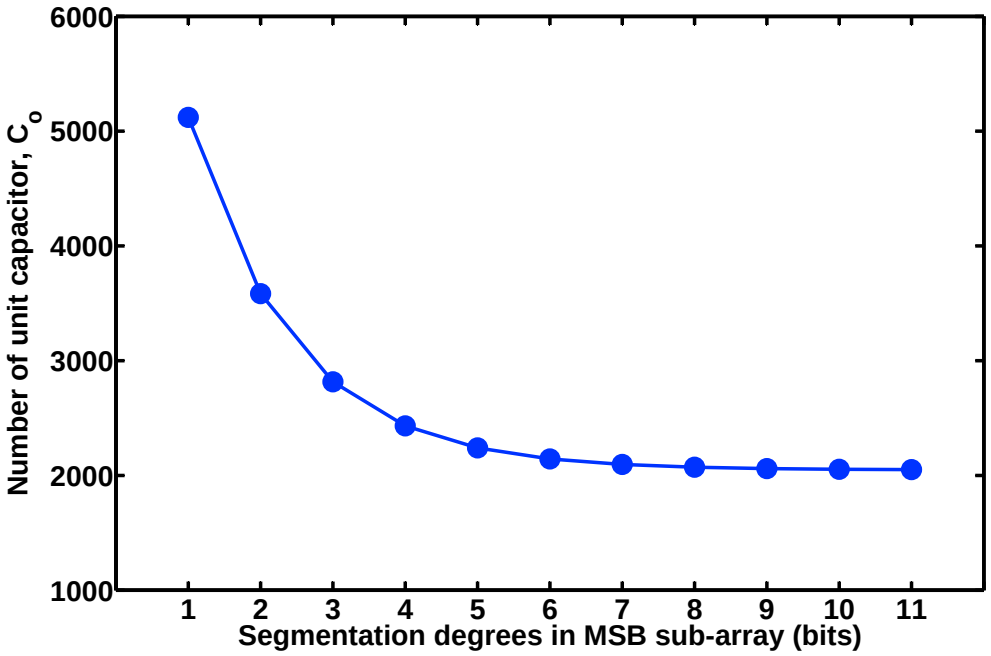


Figure 6.8: Total number of unit capacitor required for a 12-bit SAR ADC using the improved split-capacitive-array DAC with different segmentation degrees.

6.3.2 Power consumption due to the capacitors' switching

The analysis of the switching power consumption analysis for the architecture is similar to that of the BWA DAC architecture. The average switching energy, E_{avg}, varies from 93.88 CV^2_{REF} to 1578.2 CV^2_{REF}, as shown in figure 6.9. The average switching energy is reduced by 1.7× to 29× compared to the 12-bit charge-redistribution SAR ADC using the CBW DAC. Similar to the BWA DAC, significant power savings can be achieved with a segmentation degree ranging from 4-to-8. The switching power consumption for other resolution modes follow a similar trend and the minimum switching power can be achieved when the segmentation degree is around $N/2$.

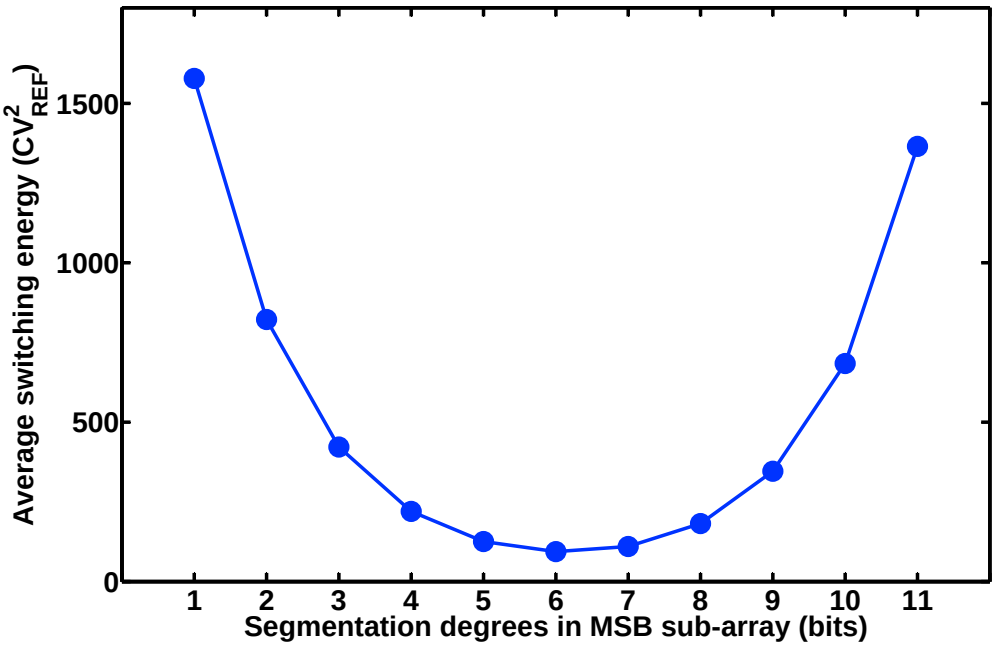


Figure 6.9: Switching energy consumption of a 12-bit charge redistribution SAR ADC using the improved split-capacitive-array DAC with different segmentation degrees.

6.3.3 Linearity analysis

Similar to the analysis in the BWA DAC architecture, the parasitic capacitances of the improved split-capacitive-array DAC come from the top- and bottom-plate parasitic capacitance of the attenuation capacitor C_M as well as the top-plate parasitic capacitances of the MSB sub-array and the LSB sub-array which can be calculated as

$$\begin{aligned} C_{MSBp} &= \beta C_b + \alpha C_{MSB,total}, \\ C_{LSBp} &= \alpha C_b + \alpha C_{LSB,total}, \end{aligned} \tag{6.5}$$

where α and β are the percentage of top- and bottom-plate parasitic capacitances of each capacitor, respectively. C_{MSBp} results in gain error and has no effect on the ADC's linearity whereas C_{LSBp} contributes to a code-dependent error, which degrades the linearity of the ADC.

In order to investigate the effect of the segmentation degree, Monte Carlo experiments were performed on a 12-bit charge-redistribution SAR and the results are shown in figure 6.10. The SNDR improves with increasing segmentation degrees in the MSB sub-array. For the same segmentation degree, the 12-bit SAR ADC using the improved split-capacitive-array DAC has a higher SNDR and a smaller deviation compared to the 12-bit SAR ADC using the BWA DAC. To explain this improvement, let us consider the case when the segmentation degree is eight bits (K = 8). The attenuation capacitor, C_M in the BWA DAC is (8/7)C_o while C_M in the improved split-capacitive-array DAC is 16C_o. If the (8/7)C_o is assumed to have a mismatch of δ%, then the 16C_o capacitor will only have a mismatch of $\frac{\delta}{\sqrt{16}}$%. Furthermore, the C_{LSBp} has a smaller influence on the improved DAC compared to the BWA DAC. Therefore, a segmentation degree of eight or higher would be

sufficient.

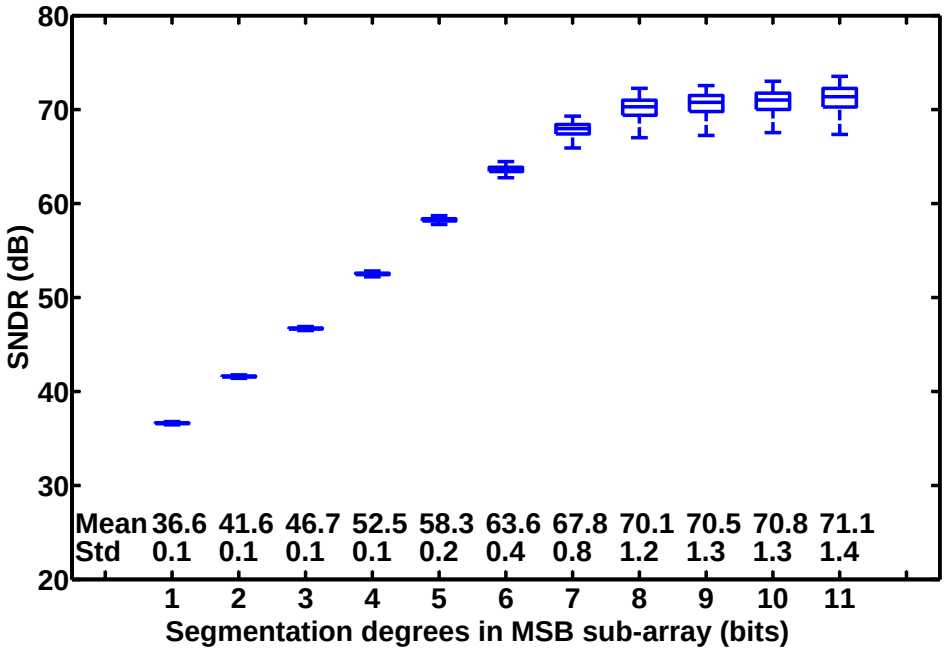


Figure 6.10: The histogram of the SNDR with 1000 Monte Carlo simulations for a 12-bit charge-redistribution SAR ADC using the improved split-capacitive-array DAC with different segmentation degrees.

6.3.4 Optimum choice of segmentation degree

The presented analysis considers the area (figure 6.8) and the power dissipation (figure 6.9) of the DAC as well as the ADC's dynamic performance (figure 6.10) based on different segmentation degrees in the split capacitive-array DAC. A segmentation degree of eight or higher is required to achieve the optimum trade-offs. Therefore, the proposed split-capacitive-array DAC with a MSB:LSB=8:4 segmentation is determined, which reduces the input capacitance by 2× and the switching power by 15× as compared to the CBW DAC. It also improves the SAR ADC's dynamic performance and the switching power by 3.75× as compared to the BWA DAC with MSB:LSB=10:2 segmentation.

6.4 Architecture II - an unary-binary segmentation with multiple-split capacitive-array DAC architecture

To further reduce the area and the switching power consumption, a three-segmented unary-binary split-capacitive-array DAC architecture is proposed. Figure 6.11 shows the single-ended N-bit SAR ADC using the proposed DAC architecture. The capacitive-array DAC is partitioned into three parallel sub-arrays with a ratio of K:J:L, where K is the number of bits in the MSB sub-array (C_1, C_2, . . . , C_K), J is the number of bits in the

MID sub-array (C_{K+1}, C_{K+2}, . . . , C_{K+J}), L is the number of bits in the LSB sub-array (C_{K+J+1}, C_{K+J+2}, . . . , C_{K+J+L}). The first few MSB capacitors C_1-C_4 are unary-weighted while the remaining MSB capacitors C_5-C_K are binary-weighted. The unary-binary segmentation reduces the DNL yield with negligible area and power consumption overhead [112]. A 1-bit LSB segmentation (L = 1) is chosen to achieve the highest linearity in the three-segmented split capacitive-array DAC.

The value of each capacitor in this architecture is given by

$$
\begin{aligned}
C_i &= \begin{cases} 2^{N-i-2}C_o, & 1 \le i \le K, \\ 2^{N-i-1}C_o, & K+1 \le i \le K+J, \\ C_o, & i = 0, N, \end{cases} \\
C_L &= 2C_o, \\
C_M &= 2^{N-K-1}C_o,
\end{aligned} \tag{6.6}
$$

where C_o is the capacitance of the unit capacitor.

The total capacitance in each sub-array is

$$\begin{aligned} C_{MSB,total} &= \sum_{i=1}^{K} C_i = (2^{N-2} - 2^{N-K-2})C_o, \\ C_{MID,total} &= \sum_{i=K+1}^{K+J} C_i = (2^{N-K-1} - 1)C_o, \\ C_{LSB,total} &= 2C_o. \end{aligned} \tag{6.7}$$

To simplify the analysis, it is assumed that all the MSB capacitors are binary-weighted since it does not affect the area and the power consumption. The linearity analyses of the unary-binary segmentation is dealt with separately.

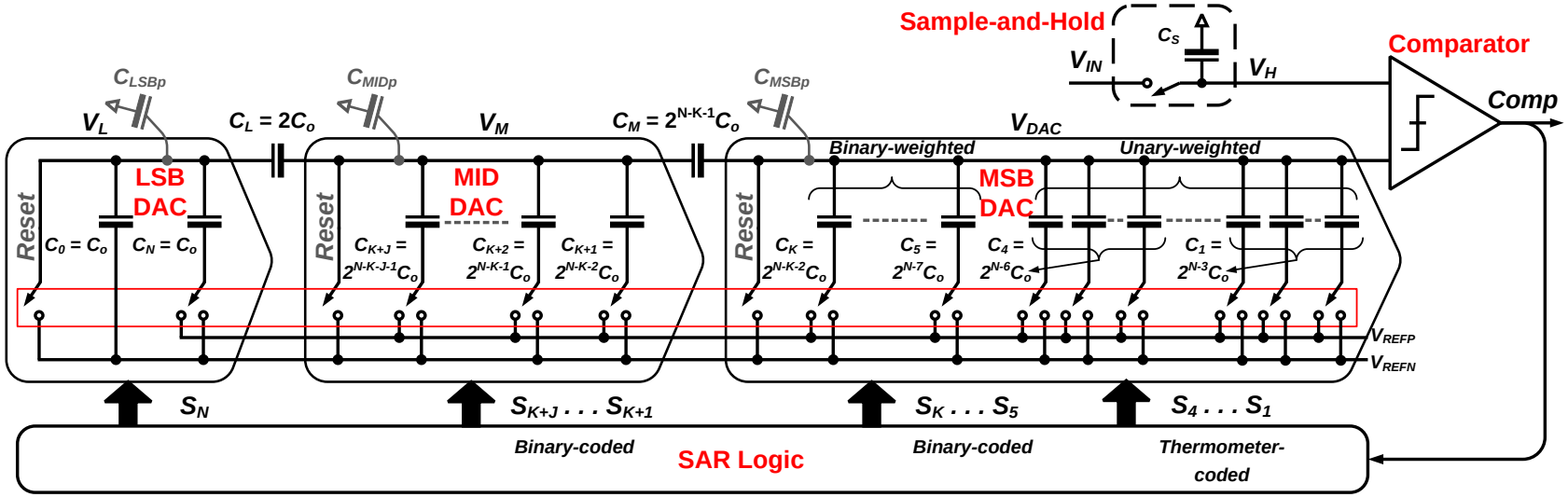


Figure 6.11: Schematic diagram of a single-ended N*-bit SAR ADC using the proposed 3-segmented split capacitive array DAC.*

6.4.1 Area requirement

This architecture has an input capacitance of $2^{N-2}C_o$, which has a $4\times$ reduction compared to the CBW DAC. The total number of unit capacitors can be derived based on equation (6.7). As shown in figure 6.12, the required total number of unit capacitors varies with the segmentation degree and the total number of unit capacitors decrease with an increasing segmentation degree. It can be concluded that there would not be any significant decrease in the number of unit capacitors when the number of bits in the MSB sub-array, K, is greater than $N/2$..

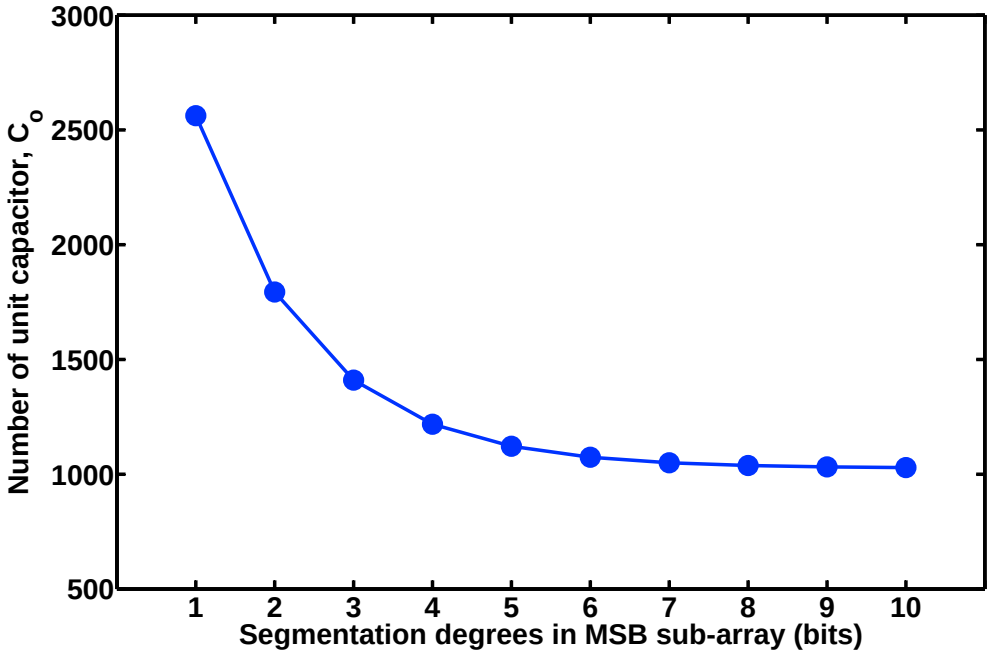


Figure 6.12: Total number of unit capacitor required for a 12-bit SAR ADC using the 3-segmented split-capacitive-array DAC with different segmentation degrees.

6.4.2 Power consumption due to the capacitors' switching

Similar to the analysis in Chapter 3, the total charge that V_{REF} delivers to the capacitive DAC during the K-bit MSB, the J-bit MID and the 1-bit LSB conversions can be calculated separately and then substituted back into equation (3.1). To simplify the calculation, the first four bits in the MSB sub-array are assumed to be binary-weighted.

The total charge consumption during the first K-bit is the same as a K-bit binary-weighted capacitive DAC.

$$\sum_{i=1}^{K} Q_i = 2^K C_o V_{REF} \times \left\{ \frac{5}{6} - \left(\frac{1}{2}\right)^K - \frac{1}{3}\left(\frac{1}{4}\right)^K - \frac{1}{2}\left(\sum_{i=1}^{K-1} \frac{D_i}{2^i}\right)^2 - \left(\frac{1}{2}\right)^K \sum_{i=1}^{K-1} \frac{D_i}{2^i} \right\}, \tag{6.8}$$

where $D_1, D_2, \ldots, D_K$ are the binary outputs of the ADC.

To calculate the total charge consumption during the next J clock cycles, one must consider that each of the K-bit MSB capacitors is connected to either V_{REFP} or V_{REFN} based on the value of $D_1, D_2, \ldots, D_K$ digital bits already determined during the previous clock cycles. The charge consumption in the following clock cycle is obtained from

$$Q_i = C_i V_{REF} + \left(C_i + \sum_{j=K+1}^{i-1} C_j D_j \right) (V_{M_{i-1}} - V_{M_i}) + \left(\sum_{j=1}^{K} C_j D_j \right) (V_{DAC_{i-1}} - V_{DAC_i}), \qquad K+1 \le i \le K+J, \tag{6.9}$$

where V_{M_i} and V_{DAC_i} (node voltages annotated in figure 6.11) are given by

$$V_{M_i} = V_{REF} \times \Bigg\{ \frac{\sum_{j=1}^{K} C_j D_j}{C_{MSB,total} + C_M || (C_{MID,total} + (C_{LSB,total} || C_L))} \times \frac{C_M}{C_M + C_{MID,total} + (C_{LSB,total} || C_L)} + \frac{C_i + \sum_{j=K+1}^{i-1} C_j D_j}{C_{MID,total} + (C_M || C_{MSB,total}) + (C_{LSB,total} || C_L)} \Bigg\} \tag{6.10}$$

and

$$V_{DAC_i} = V_{REF} \times \Bigg\{ \frac{\sum_{j=1}^{K} C_j D_j}{C_{MSB,total} + C_M || (C_{MID,total} + (C_{LSB,total} || C_L))} + \frac{C_i + \sum_{j=K+1}^{i-1} C_j D_j}{C_{MID,total} + (C_M || C_{MSB,total}) + (C_{LSB,total} || C_L)} \times \frac{C_M}{C_M + C_{MSB,total}} \Bigg\}, \tag{6.11}$$

substituting equations (6.10) and (6.11) in (6.9) and the total charge consumption can be obtained.

The charge consumption for switching the capacitor, C_N is almost negligible compared to total charge consumption, however, for completeness, the charge consumption for switching C_N is

$$Q_N = C_N V_{REF} + C_N (V_{L_{N-1}} - V_{L_N}) + \left(\sum_{j=1}^{K+J} C_j D_j \right) \times (V_{DAC_{N-1}} - V_{DAC_N} + V_{M_{N-1}} - V_{M_N}), \tag{6.12}$$

where V_{L_N}, V_{M_N} and V_{DAC_N} (node voltages annotated in figure 6.11) are given by

$$V_{M_N} = V_{REF} \times \Bigg\{ \frac{\sum_{j=1}^{K} C_j D_j}{C_{MSB,total} + C_M || (C_{MID,total} + (C_{LSB,total} || C_L))} \times \frac{C_M}{C_M + C_{MID,total} + (C_{LSB,total} || C_L)} + \frac{\sum_{j=K+1}^{K+J} C_j D_j}{C_{MID,total} + (C_M || C_{MSB,total}) + (C_{LSB,total} || C_L)} + \frac{C_N}{C_{LSB,total} + (C_L || C_{LSB,total})} \times \frac{C_L}{C_L + C_{MID,total} + (C_M || C_{MSB,total})} \Bigg\}, \tag{6.13}$$

$$V_{L_N} = V_{REF} \times \Bigg\{ \frac{\sum_{j=1}^{K} C_j D_j}{C_{MSB,total} + C_M || (C_{MID,total} + (C_{LSB,total} || C_L))} \times \frac{C_M}{C_M + C_{MID,total} + (C_{LSB,total} || C_L)} \times \frac{C_L}{C_L + C_{LSB,total}} + \frac{\sum_{j=K+1}^{K+J} C_j D_j}{C_{MID,total} + (C_M || C_{MSB,total}) + (C_{LSB,total} || C_L)} \times \frac{C_L}{C_L + C_{LSB,total}} + \frac{C_N}{C_{LSB,total} + (C_L || C_{LSB,total})} \Bigg\} \tag{6.14}$$

and

$$V_{DAC_N} = V_{REF} \times \Bigg\{ \frac{\sum_{j=1}^{K} C_j D_j}{C_{MSB,total} + C_M || (C_{MID,total} + (C_{LSB,total} || C_L))} + \frac{\sum_{j=K+1}^{K+J} C_j D_j}{C_{MID,total} + (C_M || C_{MSB,total}) + (C_{LSB,total} || C_L)} \times \frac{C_M}{C_M + C_{MSB,total}} + \frac{C_N}{C_{LSB,total} + (C_L || C_{LSB,total})} \times \frac{C_M}{C_M + C_{MSB,total}} \times \frac{C_L}{C_L + C_{MID,total} + (C_M || C_{MSB,total})} \Bigg\}. \tag{6.15}$$

By substituting equations (6.13), (6.14) and (6.15) in (6.12), the total charge consumption during the 1-bit LSB bit-cycling can be obtained.

The overall switching power consumption for the DAC architecture can be calculated by substituting equations (6.8), (6.9) and (6.12) in (3.1). As shown in figure 6.13, the average switching energy, E_{avg}, varies from 70 CV_{REF}^2 to 896.2 CV_{REF}^2, which is 3× – 39× more energy-efficient compared to the 12-bit charge-redistribution SAR ADC using the CBW DAC. Significant power savings can be achieved with a segmentation degree ranging from 3-to-8. The switching power consumption for other resolution modes follow a similar trend and the minimum switching power can be achieved when the segmentation degree is around $N/2$.

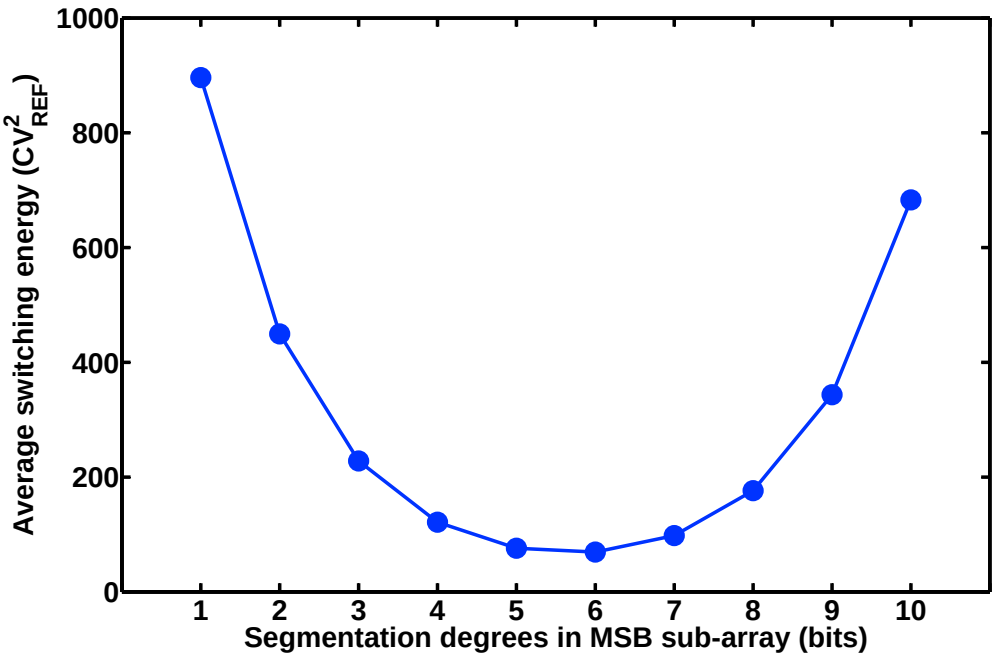


Figure 6.13: Switching energy consumption of a 12-bit charge redistribution SAR ADC using the 3-segmented split-capacitive-array DAC with different segmentation degrees.

6.4.3 Linearity analysis

The linearity analysis is similar to the previous section, the parasitic capacitances for the 3-segmented split-capacitive-array DAC come from the top- and bottom-plate parasitic capacitance of the attenuation capacitance C_M and C_L as well as the top-plate parasitic capacitance of the sub-arrays which can be calculated as

$$\begin{aligned} C_{MSBp} &= \beta C_M + \alpha C_{MSB,total}, \\ C_{MIDp} &= \beta C_L + \alpha C_M + \alpha C_{MID,total}, \\ C_{LSBp} &= \alpha C_L + \alpha C_{LSB,total}, \end{aligned} \tag{6.16}$$

where α and β is the percentage of top- and bottom-plate parasitic capacitances of each capacitor, respectively. The parasitic capacitance C_{MSBp} will result in gain error and has no effect on the ADC's linearity whereas the parasitic capacitances C_{MIDp} and C_{LSBp} contribute to a code-dependent error, which degrade the linearity of the ADC.

In order to investigate the effect of the segmentation degree, Monte Carlo experiments were performed on a 12-bit charge-redistribution SAR and the results are shown in figure 6.14. The SNDR also improves with the increasing segmentation degrees in the MSB sub-array.

6.4.4 Optimum choice of segmentation degree

The presented analysis considers the area (figure. 6.12) and the power dissipation (figure 6.13) from the DAC as well as the ADC's dynamic performance (figure 6.14) based on different segmentation degrees in the split capacitive-array DAC. In order to achieve a SNDR of more than 68.3-dB (ENOB >11-bit) for the 12-bit SAR ADC with the proposed split capacitive DAC, a segmentation degree of eight or higher is

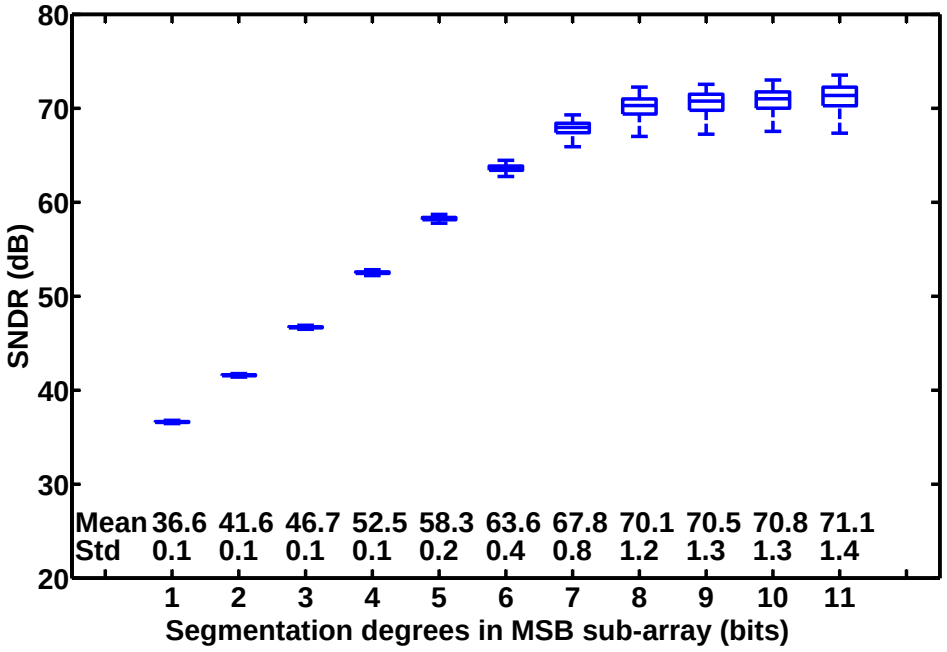


Figure 6.14: The histogram of the SNDR with 1000 Monte Carlo simulations for a 12-bit charge-redistribution SAR ADC using the 3-segmented split-capacitive-array DAC with different segmentation degrees.

required. Therefore, it can be concluded that the optimum value of the segmentation degree is eight bits in the MSB sub-array (MSB:MID:LSB=8:3:1).

6.4.5 Unary-Binary Segmentation In MSB Sub-Array

To further improve the SNDR and minimize its standard deviation, the first four MSB bits are replaced with the unary-weighted bits in order to reduce the standard deviation of DNL with negligible area and power consumption overhead [112]. The result indicates that the mean μ_{SNDR} of the SAR ADC improves from 68.31-dB (ENOB of 11.05-bit) to 68.77-dB (ENOB of 11.13-bit) while the standard deviation σ_{SNDR} decreases from 1.56-dB to 1.07-dB.

6.5 Comparison with other structures

To have a fair comparison with the CBW DAC and the BWA DAC, the optimal segmentation degree for each split-capacitive-array DAC is determined to achieve the minimum μ_{SNDR} of 68.0-dB (ENOB of 11.0-bit) with the minimum area and the minimum switching power consumption. The performance of each capacitive-array DACs are summarized in table 6.1. For a 12-bit SAR ADC, both proposed DACs reduce the input load capacitance and area by $2\times$ and $4\times$, respectively, and the switching power by $15\times$ and $15.5\times$, respectively, compared to the CBW DAC. It also improves the linearity, minimizes the mismatch variation and reduces the switching power by $3.75\times$ and $3.87\times$, respectively, compared to the BWA DAC.

Table 6.1: Performance Comparison for a 12-bit SAR ADC

Design	SNDR [dB]		Energy	Area
	μ_{SNDR}	σ_{SNDR}	$[CV_{REF}^2]$	$[C_o]$
12-bit CBW DAC	71.83	1.07	2730	4096
BWA DAC (MSB:LSB=10:2)	68.30	1.77	683.7	$1028\frac{4}{3}$
Architecture I (MSB:LSB=8:4)	70.10	1.20	182.0	2072
Architecture II (MSB:MID:LSB=8:3:1)	68.77	1.07	176.40	1038

6.6 Summary

In conclusion, the proposed split-capacitive-array architectures have achieved reductions in the total area of the ADC, the DAC's settling time and the switching power consumption without sacrificing much of the ADC's dynamic performance.

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Chapter 7

Conclusion

In the first part of this dissertation, several circuit design techniques are proposed to reduce the area and the power consumption and enhance the sampling speed of a SAR ADC. A highly configurable, dual-channel SAR ADC is proposed and fabricated in GLOBALFOUNDRIES 1P8M 0.13-μm CMOS process. The ADC operates at a supply voltage of 0.6-V to achieve an optimal energy-efficiency across all the resolution modes. In the 10-bit resolution mode operation, the ADC is able to operate at a maximum sampling rate of 250-kS/s per channel to accommodate high bandwidth and multi-channel applications. A 4-to-10-bit resolution-reconfigurable dual-capacitive arrays DAC with an energy-efficient charge-recovery switching scheme reduces the switching power consumption and minimizes the input common-mode variation so that the comparator's dynamic offset is minimized. In addition, a dedicated sample-and-hold (S/H) capacitive array is used per channel, relaxing the settling time, reducing the number of analog multiplexing circuitry by 2×. The total area is also reduced by sharing a differential 9-bit capacitive-array DAC. As the multiplexing is performed in the digital domain, the power consumption per channel as well as the system complexity is reduced. To further optimize the circuit, custom-designed S/H and DAC switches, configurable resolutions SAR

logics and a single comparator to share among both input channels are proposed.

The second part of this dissertation explores several ways to improve the linearity and reduce the mismatch for the high resolution capacitive-array DACs, which is necessary for the high resolution SAR ADCs. First, a placement strategy is proposed to address the layout's mismatches in the CBW DAC. A matrix-adjustment method is proposed to optimize the array of the CBW DAC. Various placement techniques and weighting methods are proposed for the placement of active and dummy unit capacitors. The star-like placement increases the degree of dispersiveness (i.e., reduce random mismatch), reduces the first-order oxide-gradient-induced mismatches and the second-order lithographic errors and achieves a more symmetrical routing compared to existing works. A homogenization method is also proposed to reduce the asymmetrical fringing mismatches among the capacitive-array, thus improving the systematic mismatch between the capacitive-array and the dummy capacitors.

Second, two new types of split capacitive-array DAC architectures are proposed to reduce the area, the power consumption and improve the linearity compared to the CBW DAC and the BWA DAC. For a 12-bit SAR ADC, the proposed DACs reduce the input load capacitance and area by $2\times$ and $4\times$, respectively, and the switching power by $15\times$ and $15.5\times$, respectively, compared to the CBW DAC. It also improves the linearity, minimizes the mismatch variation and reduces the switching power by $3.75\times$ and $3.87\times$, respectively, compared to the BWA DAC.

7.1 Future works

There are some research topics, extending from this dissertation, which can further improve the system resolution, scalability and power efficiency of the SAR ADC.

7.1.1 Low-voltage power management circuits

Since this dissertation focus on a low voltage ADC, it follows then that an efficient on-chip DC-DC converter and low-dropout regulator capable of delivering power at a voltage supply of at least 500-mV is needed in order to make the ADC a more integrated system.

Till date, there are only a few reported works in literature on low voltage management circuits. One such example is a DC-DC converter capable of delivering power in the μW to mW range at a load voltage from 1.1-V down to 300-mV [113]. However, the high output voltage ripple and poor supply noise rejection ratio from the DC-DC converter will not be suitable for ADC's reference voltages. A voltage regulator will be needed to improve these parameters. Yet, none of the existing analog voltage regulators are able to meet this requirement. As such, there is a potential research area in low voltage power management circuits.

7.1.2 Comparator offset using digital calibration techniques or redundancy techniques

In this dissertation, larger transistor sizings were used to maintain small comparator's offset, which has resulted in significant increases in parasitic capacitance and area. Special circuit techniques can be used to reduce the comparator's offset. In a low voltage system, digital offset calibration techniques are preferred over the conventional analog circuit techniques such as auto-zeroing, correlated double sampling, and chopper stabilization [57, 114, 115]. One common method for digital offset calibration of a dynamic latched comparator is reduced by adding capacitor banks on the comparator's outputs [19, 116]. These load capacitances are controlled digitally to reduce the offset voltage. The resolution of the calibration is determined by the size of the load capacitance and digital

word. This results in a lower operating speed and a larger area in a high resolution ADC. Another technique is the comparator redundancy technique. It improves the ADC's performance without increasing the power significantly compared to the sizing technique. Comparator redundancy has been demonstrated successfully in 0.2-V flash ADC [117]. However, it increases the system complexity for digital correction logic.

Alternatively, the time-domain comparator can used to replace the voltage-domain comparator since it has a low input-referred noise and a small input-offset voltage [58, 85]. Besides, the time-domain comparator is realised by inverters so it is suitable in low voltage system.

7.1.3 Digital correction for channel mismatch

In this dissertation, a dual-channel SAR ADC was presented. This architecture can be further extended to multiple channels. One of the key challenges for such designs is the channel mismatch problem. To diminish the gain error and offset between ADC channels, developing a simple but effective digital correction algorithm is necessary.

7.1.4 DAC calibration techniques

For CBW DACs, the capacitance of the DAC array increases exponentially with the resolution, which increases the switching energy, the area, and the settling time. In the BWA DAC, the capacitive-array is divided into smaller binary weighted capacitive arrays, which are connected by a bridge capacitor [11, 23, 45, 58–62]. The size of the total capacitive-array does not increase exponentially with the resolution compared to the CBW DAC. This architecture reduces switching power consumption and improves the settling time. However, this architecture is vulnerable to the

distortion, which is caused by the parasitic capacitances associated with the bridge capacitor as well as the mismatches of the binary-weighted capacitive-arrays. In this dissertation, two split-capacitive-arrays DACs are proposed for the 12-bit SAR ADC, which improve the dynamic performance of the SAR ADC and reduces the switching power consumption and the area. DAC calibration methods can be used to further improve the dynamic performance beyond 12-bit SAR ADC [63–65]. However, current techniques are complex and requires significant silicon area. Therefore, developing a simple but effective digital calibration algorithm is necessary.

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Appendix A

Summary For The State-Of-The-Art SAR ADC From ISSCC and VLSI Symposium

This Appendix provides a summary of various ADCs' design parameters and design strategies reported from *IEEE International Solid-Sate Circuits Conference* and *IEEE Symposium on VLSI Circuits*. These information identifies the main design techniques used in recent SAR ADCs architecture and the research direction for SAR ADCs in the recent years.

Table A.1: ADC Performance Summary from ISSCC paper 1997 - 2012

Year	**Process [μm]**	**Title**	**Contributions & Techniques**	**SNDR [dB]**	**Power**	**Frequency [MHz]**	**FOM [fJ/step]**
1997 [118]	1.00	A MOSFET-only, 10 b, 200 ksample/s A/D converter capable of 12 b linearity untrimmed	1) Current division ladder 2) network based on MOS	56.5	12-mW	0.2	109,340
2002 [67]	0.13	A 1.2V 10b 20MSample/s non-binary successive approximation ADC in 0.13μm CMOS	1) Non-binary / 2) Bit-Redundancy (1st Reported)	55.0	12-mW	20	1,306
2004 [37]	0.09	A 6b 600MHz 10mW ADC array in digital 90nm CMOS	1) 8 Channels TI-SAR 2) RAM data storage 3) Offset technique (DSP)	31.0	10-mW	600	575
2006 [119]	0.18	A 25μW 100kS/s 12b ADC for Wireless Micro-Sensor Applications	1) 8/12b Scalable SAR ADC 2) 3 stage pre-amplifier 3) Self-timed bit-cycling	65.0	25-μW	0.1	172
2006 [11]	0.13	A 6b 600MS/s 5.3mW Asynchronous ADC in 0.13μm CMOS	1) 2 Channels TI-SAR 2) Asynchronous clock 3) Foreground off-chip cal.	33.0	5.3-mW	600	242

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Table A.1 – *Continued from previous page*

Year	**Process [μm]**	**Title**	**Contributions & Techniques**	**SNDR [dB]**	**Power**	**Frequency [MHz]**	**FOM [fJ/step]**
2007 [12]	0.09	A 65fJ/Conversion-Step, 0 - 50MS/s 0-0.7mW 9bit Charge Sharing SAR ADC in 90nm Digital CMOS	1) Passive Charge Sharing 2) Asynchronous clock	46.3	290-μW 50% (D) 50% (A)	50	85.9
2007 [120]	0.13	A 14b 40MS/s Redundant SAR ADC with 480MHz Clock in 0.13μm CMOS	1) Pipelined, TI-SAR 2) Redundant SAR ADC 3) DEM calibration	83.0	66-mW 26% (D) 74% (A)	40	142.3
2008 [66]	0.09	An 820μW 9b 40MS/s Noise-Tolerant Dynamic SAR ADC in 90nm Digital CMOS	1) Noise Tolerant Charge Sharing SAR ADC 2) Flexible offset comp.	53.3	820-μW 35% (D) 65% (A)	40	54.3
2008 [121]	0.065	Highly-Intereleaved 5b 250MS/s ADC with Redundant Channels in 65nm CMOS	1) 36 Channels TI SAR 2) 6 redundant channel	53.3	1.2-mW	40	54.3
2008 [21]	0.09	A 150MS/s 133μW 7b ADC in 90nm Digital CMOS Using a Comparator-Based Asynchronous Binary-Search Sub-ADC	1) 2-step CABS SAR 2) DAC subtracts 1/4 of FS	40.0	133-μW	150	54.3

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Table A.1 – *Continued from previous page*

Year	**Process [μm]**	**Title**	**Contributions & Techniques**	**SNDR [dB]**	**Power**	**Frequency [MHz]**	**FOM [fJ/step]**
2008 [122]	0.065	A 1.9μW 4.4fJ/conversion-step 10b 1MS/s Charge-Redistribution ADC	1) Lowest FoM 2) Dynamic comparator	54.4	1.9-μW 65% (D) 35% (A)	1	4.4
2008 [58]	0.18	A 9.4-ENOB 1V 3.8μW 100kS/s SAR ADC with Time-Domain Comparator	1) 1st Time comparator 2) Split capacitor DAC array 3) Charge-Redistribution	58.0	3.6-μW	0.1	55.5
2008 [45]	0.13	A 32mW 1.25GS/s 6b 2b/step SAR ADC in 0.13μm CMOS	1) 2b/step (1st Reported) 2) 5fF unit capacitor 3) Flip-flop bypass SAR	32.0	32-mW 30% (D) 70% (A)	1250	787.2
2008 [123]	0.09	A 24GS/s 6b ADC in 90nm CMOS	1) 16 Channels TI SAR 2) 10 SAR ADC/Channel 3) CML to CMOS clock	26.4	1.2-W	2400	2930
2009 [124]	0.045	A 1.1V 50mW 2.5GS/s 7b Time-Interleaved C-2C SAR ADC in 45nm LP Digital CMOS	1) 16 Channels TI SAR 2) C-2C Capacitor Array	34.0	50-mW	2500	488.5

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Table A.1 – *Continued from previous page*

Year	Process [μm]	Title	Contributions & Techniques	SNDR [dB]	Power	Frequency [MHz]	FOM [fJ/step]
2009 [22]	0.13	A 600MS/s 30mW 0.13μm CMOS ADC Array Achieving Over 60dB SFDR with Adaptive Digital Equalization	1) 10 Channels TI SAR 2) Adaptive Digital Filter 3) Non-binary (1.86 bit)	43.0	30-mW 51% (D) 49% (A)	600	433
2010 [125]	0.25	An 18b 12.5MHz ADC with 93dB SNR	1) 2-Stage, 2b/step SAR 2) Non-binary Redundancy 3) Dithering for linearity	80.0	105-mW	12.5	1028
2010 [25]	0.13	A 12b 22.5/45MS/s 3.0mW 0.059mm^2 CMOS SAR ADC achieving over 90dB SFDR	1) Non-binary (1.86 bit) 2) Perturbation based Cal. 3) Dynamic Vt comparison	67.1	3.02-mW 40% (D) 60% (A)	45	36.3
2010 [32]	0.065	A 0.06mm^2 8.9b ENOB 40MS/s pipelined SAR ADC in 65nm CMOS	1) 2 Stage Pipelined ADC 1st Stage 4b & 2nd Stage 6b 2) 1.5b/cycle redundancy	52.5	1.21-mW 50% (D) 50% (A)	40	87.8
2010 [64]	0.065	A 10b 50MS/s 820μW SAR ADC with On-Chip Digital Calibration	1) Comparator offset cal. 2) CDAC linearity error cal.	56.6	820-μW 45% (D) 55% (A)	50	29.7

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Table A.1 – *Continued from previous page*

Year	**Process [μm]**	**Title**	**Contributions & Techniques**	**SNDR [dB]**	**Power**	**Frequency [MHz]**	**FOM [fJ/step]**
2010 [26]	0.065	A 10b 100MS/s 1.13mW SAR ADC with binary-scaled error compensation	1) 3.2 fF Unit Capacitor 2) Binary-scaled DAC 3) Digital error correction	56.0	1.13-mW 41% (D) 59% (A)	100	21.9
2010 [13]	0.09	A 30fJ/conversion-step 8b 0-to-10MS/s asynchronous SAR ADC in 90nm CMOS	1) 1fF Unit Capacitor 2) Self-synchronization 3) Asynchronous clock	48.4	69-μW 58% (D) 42% (A)	10	31.4
2010 [126]	0.065	A 40GS/s 6b ADC in 65nm CMOS	1) Synthesizer and PA 2) CML to CMOS converter 3) On-chip memory	25.2	1.5-W	40000	2512
2011 [38]	0.065	A 480mW 2.6GS/s 10b 65nm CMOS time-interleaved ADC with 48.5dB SNDR up to Nyquist	1) 64 Channels TI SAR 2) CML to CMOS converter 3) Current mode Non-binary	48.5	480-mW	2600	849
2011 [55]	0.065	A 0.024mm^2 8b 400MS/s SAR ADC with 2b/cycle and resistive DAC in 65nm CMOS	1) 2b/cycle, interpolated FE 2) Cross-coupled bootstrap 3) Resistive DAC array	40.4	4-mW	400	117

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Table A.1 – *Continued from previous page*

Year	**Process [μm]**	**Title**	**Contributions & Techniques**	**SNDR [dB]**	**Power**	**Frequency [MHz]**	**FOM [fJ/step]**
2011 [127]	0.065	A resolution-reconfigurable 5-to-10b 0.4-to-1V power scalable SAR ADC	1) Scalable SAR ADC 5-10b 2) Power gating 3) 4-bit offset tuning	55.0	206-nW	0.02	22.4
2012 [79]	0.065	A 90MS/s 11MHz bandwidth 62dB SNDR noise-shaping SAR ADC	1) Noise Shaping SAR ADC 2) FIR-IIR filter 3) DAC is an 8b	62.0	806-μW 75% (D) 25% (A)	88	35.8
2012 [128]	0.04	A 70dB DR 10b 0-to-80MS/s current -integrating SAR ADC with adaptive dynamic range	1) Built-in variable gain 2) Digital post-processing 3) Charge-sharing	54.2	6-mW	80	178.8
2012 [15]	0.04	A 7-to-10b 0-to-4MS/s flexible SAR ADC with 6.5-to-16fJ/conversion-step	1) Scalable SAR ADC 7-10b 2) 0.6fF Unit Capacitor	58.3	17.4-μW	4	6.5

Table A.2: ADC Performance Summary from VLSI paper 1997 - 2012

Year	**Process [μm]**	**Title**	**Contributions & Techniques**	**SNDR [dB]**	**Power**	**Frequency [MHz]**	**FOM [fJ/step]**
2006 [129]	0.065	A 500MS/s 5b ADC in 65nm CMOS	1) 6 Channels TI SAR 2) Spilt-Cap. Switching 3) Preamplifier-Comparator	26	6-mW 52% (D) 48% (A)	500	740
2007 [42]	0.13	A 1.35 GS/s, 10b, 175 mW time-interleaved AD converter in 0.13μm CMOS	1) 16 Channels TI SAR 2) 2 Stage-Pipelined/Chan. 3) Overrange (Non-binary)	48.1	175-mW	1350	600
2009 [17]	0.13	A 0.92mW 10-bit 50-MS/s SAR ADC in 0.13μm CMOS process	1) Set-and-down Switching 2) Asynchronous Logic	52.8	0.92-mW 58% (D) 42% (A)	50	52
2009 [19]	0.13	A 6-bit 50-MS/s threshold configuring SAR ADC in 90-nm digital CMOS	1) Programmable Vth to implement SAR Algorithm. 2) MOS Cap.	32.0	240-μW 32% (D) 68% (A)	50	150
2009 [80]	0.13	A 12b 11MS/s successive approximation ADC with two comparators in 0.13μm CMOS	1) 2 comparator to reduce offset meta-stability 2) 1.877 Bit redundancy	62.4	3.57-mW 73% (D) 27% (A)	11	311

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Table A.2 – *Continued from previous page*

Year	**Process [μm]**	**Title**	**Contributions & Techniques**	**SNDR [dB]**	**Power**	**Frequency [MHz]**	**FOM [fJ/step]**
2009 [61]	0.18	A 1.3μW 0.6V 8.7-ENOB successive approximation ADC in a 0.18μm CMOS	1) Time comparator 2) Split capacitor 3) 150fF Unit Capacitor	53.8	1.3-μW 73% (D) 27% (A)	0.1	166
2010 [33]	0.065	A 12b 50MS/s 3.5mW SAR assisted 2-stage pipeline ADC	1) 2 stage Pipeline of SAR 1st Stage 6b & 2nd Stage 7b	64.4	3.5-mW	50	52
2010 [18]	0.18	A 1V 11fJ/conversion-step 10bit 10MS/s asynchronous SAR ADC in 0.18μm CMOS	1) Digital Error Correction 2) Multi-comparator reduces meta-stability and power	60.3	98-μW 51% (D) 49% (A)	10	11
2010 [130]	0.09	A 9-bit 150-MS/s 1.53-mW subranged SAR ADC in 90-nm CMOS	1) Sub-range ADC 2) Flash thermometer Cap 3) SAR - 2.2fF Cap	54.1	1.53-mW	150	24.7
2011 [131]	0.13	A 96-channel full data rate direct neural interface in 0.13μm CMOS	1) 23.7fF Unit Capacitor	60.3	1.1-μW	0.0313	41.5

Continued on next page

Table A.2 – *Continued from previous page*

Year	**Process [μm]**	**Title**	**Contributions & Techniques**	**SNDR [dB]**	**Power**	**Frequency [MHz]**	**FOM [fJ/step]**
2011 [132]	0.13	BioBolt:A minimally-invasive neural interface for wireless epidural recording by intra-skin communication		45.1	87-nW	0.0313	18.9
2011 [133]	0.04	A 0.5V 1.1MS/sec 6.3fJ/conversion-step SAR-ADC with tri-level comparator in 40nm CMOS	1) Tri-level comparator with metastable detection 2) 0.5fF Unit Capacitor	46.9	1.2-μW	1.1	6.3
2011 [20]	0.09	A 1-V, 8b, 40MS/s, 113μW charge-recycling SAR ADC with a 14μW asynchronous controller	1) Charge Recycling 2) Asynchronous Logic	44.5	1.2-μW	40	20.6

Appendix B

PCB Design And Test Setup

A 3.5" $\times$ 2.5" PCB was designed and fabricated on a 2-layer, FR-4 material with 40-mils thickness for the ADC testing. The PCB layout is shown in figure B.1. The Stanford DS360 and the Stanford CG635 generators provide the low distortion differential input sources and clock source, respectively. Digital outputs are level shifted up using off-chip 74AVC8T245 transceiver from NXP Semiconductor. These digital outputs will be captured by the Agilent 16802A Logic analyzer and the data is post-processed in Matlab to obtain the FFT spectrum and static measurements. All supplies are regulated by Analog Device, ADP 225, which can be set to a minimum output voltages from 0.5 V to 5.0 V and these supplies are heavily de-coupled on the test PCB as well as on-chip. The current is measured using Keithley 2604B SourceMeter SMU instrument. Figure B.2 summarizes the list of equipment used for the testing.

The chip was packaged using chip-on-board technique to minimize the PCB parasitics. The chip bonding diagram and the pins labeling are shown in figure B.3.

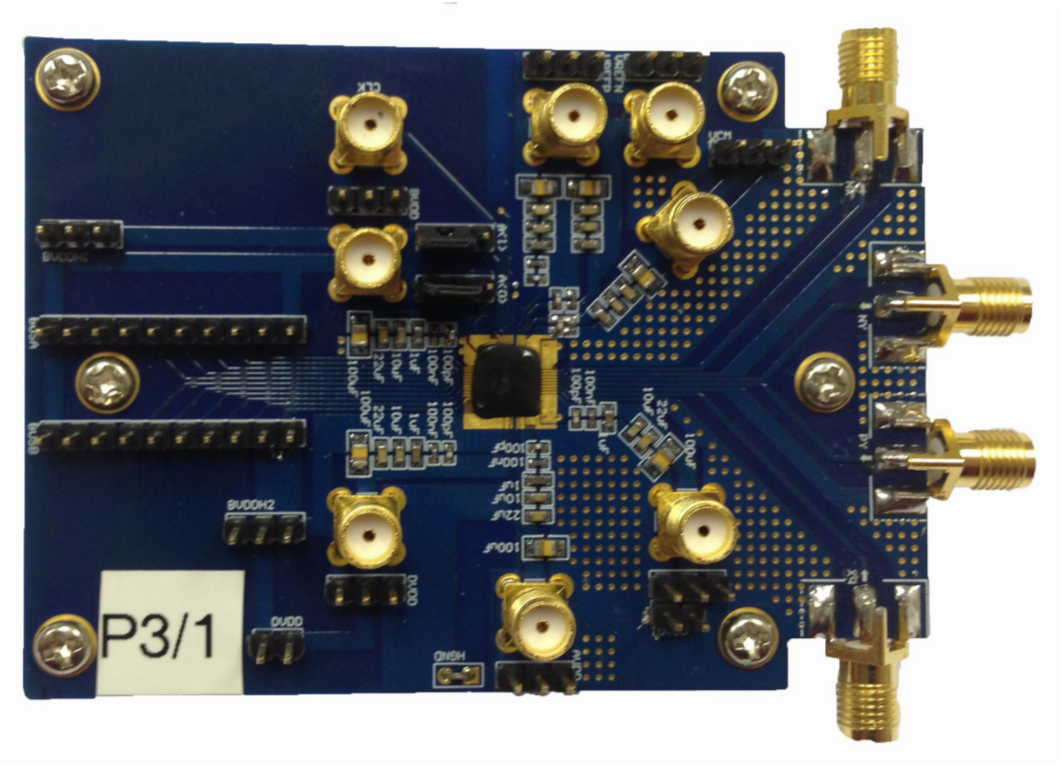


Figure B.1: PCB layout with COB packaging.

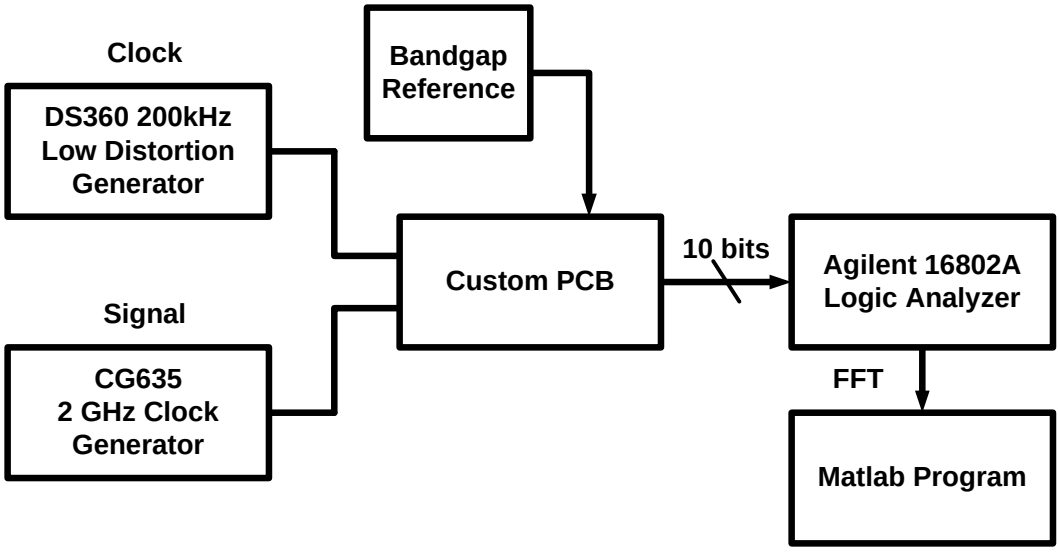
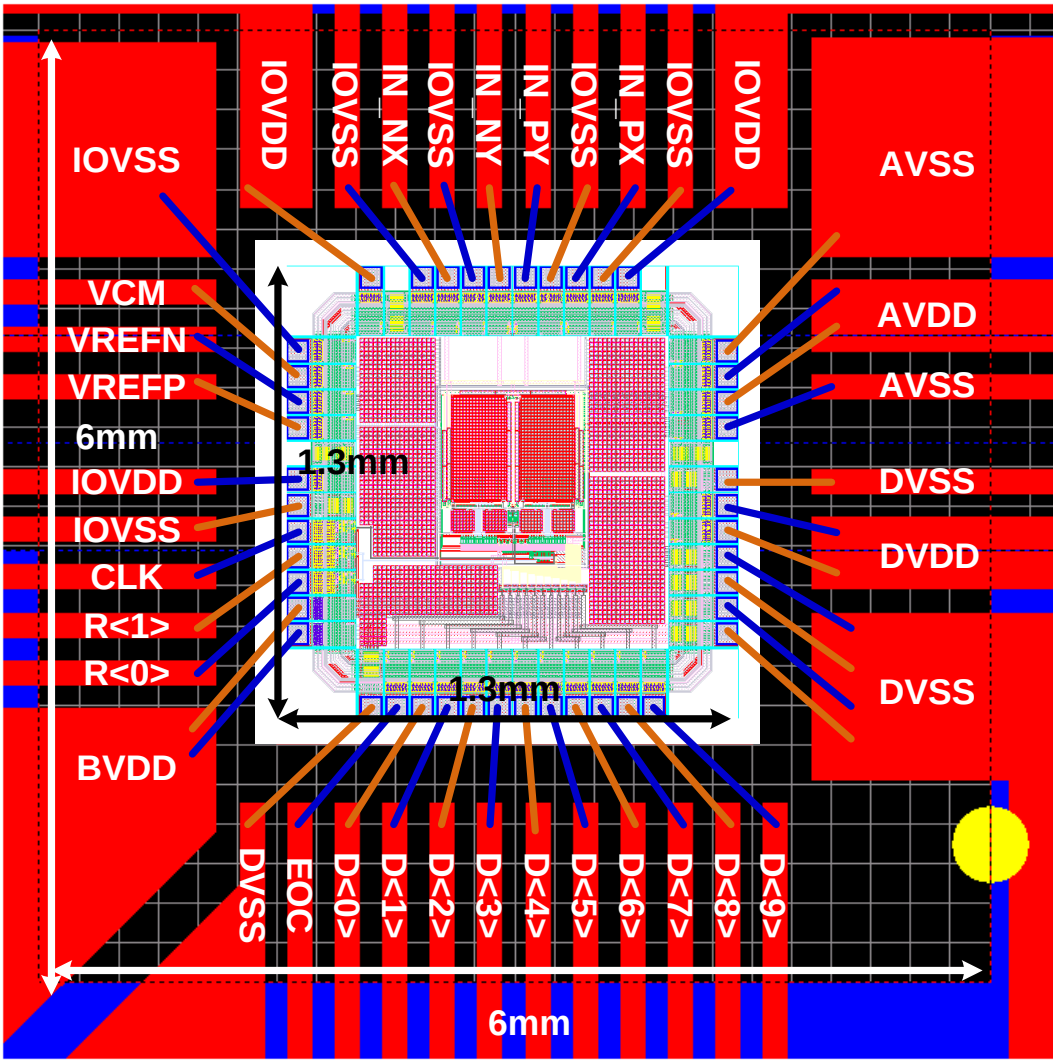


Figure B.2: Testing plan with listed equipment.

Bonding Diagram



- Die size 1.3 x 1.3 mm^2
- Bond pad size 60 x 60 μm^2
- Bond pad spacing 14 µm
- Bond pad number 42 pads
- Die Thickness 19 mils
- Landing Pad Width 6 mils
- Landing Pad Spacing 6 mils

Figure B.3: Bonding diagram of the ADC test chip.

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