TEMPERATURE SENSORS IN SOI CMOS FOR HIGH TEMPERATURE APPLICATIONS

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DECLARATION

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Jerrin Pathrose Vareed

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SUMMARY

HT temperature sensors are critical circuit blocks in oil-well instrumentation, where temperatures of deep reservoirs go above 200°C. The temperature information is used to obtain the reservoir characteristics as well as temperature compensation of other circuits. This research proposes two temperature sensor designs based on threshold voltage and bandgap principle in SOI CMOS technology.

The first design is a temperature sensor front-end based on threshold voltage temperature dependency operating up to 250°C. The core of the design is threshold voltage extraction technique. The proposed threshold voltage extraction circuit eliminates the non-linear temperature dependent mobility and mobility ratio terms, thus achieving wide operating temperature range. The voltage reference proposed as part of this front-end achieves a mean box-model temperature coefficient of 27 ppm over a temperature range of -25 to 250°C, which is the lowest reported in the HT category. The temperature inaccuracy of the front-end is within ±1.8% for the temperature range of 275°C. This design has one of the widest operating temperatures reported in literature.

The second design is a time-domain bandgap based temperature sensor operating up to 225°C. The architecture does not have an explicit bandgap reference and only requires the ratio of two diode voltages to obtain ratiometric measurement. This is achieved through a mapping function at the digital back-end. The sensor is implemented with simple time-domain

architecture, resulting in lower power consumption. The design achieves a worst-case inaccuracy of +1.6°C/-1.5°C and consumes only 20μA from a 4.5-V supply. A simple one-point calibration technique at room temperature is done in this work. The proposed architecture has the best FOM reported in the HT category. To the best of author's knowledge, this design is the first bandgap based temperature sensor operating above 200°C.

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LIST OF ABBREVIATIONS

LWD	LOGGING WHILE DRILLING
SOI	SILICON-ON-INSULATOR
BOX	BURIED OXIDE LAYER
PDSOI	PARTIALLY DEPLETED SOI
FDSOI	FULLY DEPLETED SOI
ZTC	ZERO TEMPERATURE COEFFICIENT
ADC	ANALOG-TO-DIGITAL CONVERTER
DAC	DIGITAL-TO-ANALOG CONVERTER
BGR	BANDGAP REFERENCE
TC	TEMPERATURE COEFFICIENT
CTAT	COMPLEMENTARY TO ABSOLUTE TEMPERATURE
PSRR	POWER SUPPLY REJECTION RATIO
RTD	RESISTANCE TEMPERATURE DETECTOR
DSP	DIGITAL SIGNAL PROCESSOR
SAR	SUCCESSIVE APPROXIMATION REGISTER
CTAT	COMPLEMENTARY TO ABSOLUTE TEMPERATURE
DEM	DYNAMIC ELEMENT MATCHING
FOM	FIGURE-OF-MERIT
FPGA	FIELD PROGRAMMABLE GATE ARRAY
EEPROM	ELECTRICALLY ERASABLE PROGRAMMABLE READ-ONLY
COB	CHIP-ON-BOARD

CHAPTER 1

INTRODUCTION

Integrated Circuits are classified into various categories based on their temperature range of operation as given in TABLE 1-1. Though there is no

TABLE 1-1: TEMPERATURE RANGE OF ICS

Category	**Lower**	**Upper**
Commercial	0°C	70°C
Industrial	-40°C	85°C
Extended	-40°C	125°C
Military	-55°C	125°C
High Temperature	-55°C	>125°C

standard upper limit for the high temperature category, in the context of this research it is referred to as the temperatures which ensure robust operations for the major high temperature applications such as oil and gas exploration, jet engine, military and automotive electronics. The conventional bulk CMOS does not operate reliably at high temperatures above 125°C. Therefore, technology, design and measurement method need to be reconsidered to meet the application requirements. In addition, deep understanding of temperature property of devices is also required to enable wide temperature range of operation. This thesis is dedicated to high temperature category of integrated circuits, temperature sensors in particular.

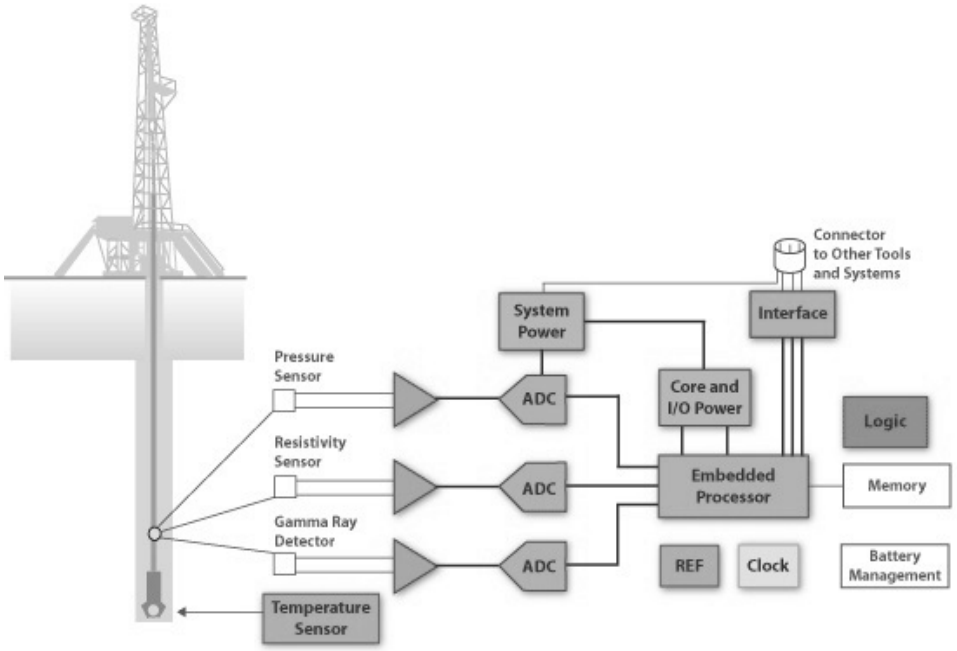


Figure 1.1: Simplified down-hole instrumentation system (TI).

1.1 High Temperature Electronics

High temperature electronics has various applications in automotive, aircraft, space, oil-well instrumentation etc. The integrated circuits developed in this research target applications for oil and gas exploration in deep sea, which operate in harsh environments such as extremely high temperatures and pressures. The temperature range that is required is 25°C to (200-300°C) depending on the depth of the well. Due to the declining oil and gas reserves, the industry is motivated to drill deeper and hence the temperatures could reach up to 300°C.

In oil and gas industry, information about the well is logged to understand the well characteristics. Electrical, acoustic, nuclear and electromagnetic measurements are carried out using the sensors in the tool string. Individual measurement or a combination of these is used to determine the petro-physical

characteristics such as porosity, saturation, hydrocarbon content etc. which ultimately determine commercial feasibility of the well for exploration. The logging is done using wireline (after drilling) or Logging While Drilling (LWD) method. In LWD, the instrumentation is attached to the drill collar and the various parameters are logged during the drilling process. This allows the making of real-time decisions about the direction of drilling and prospects of the well. Figure 1.1 shows a simplified block diagram of a down-hole instrumentation system [1]. The instrumentation needs to withstand high temperature and pressure which increases with the depth of the well. The instrumentation also needs to be very compact. On-chip instrumentation can significantly reduce the size of the electronics and more sensors could be incorporated into the tool string. This has significant impact on the oil industry and has generated great interest in High Temperature IC's for oil-well instrumentation.

1.2 Technologies for HT design

Leakage current, latch-up susceptibility, electromigration etc. are the important factors which result in the failure of CMOS IC's at high temperatures. Though high temperature circuits have been demonstrated in bulk CMOS by design techniques [2], [3], it shifts the focus away from the core performance of the circuit designed and focus is more on ensuring HT operation. One of the key issues of HT operation is the leakage current, which is proportional to the junction area and increases with temperature, and it can be 4-5 orders of magnitude greater at 250°C than at 25°C. Hence, for robust operation, alternative process options need to be explored. The HT process

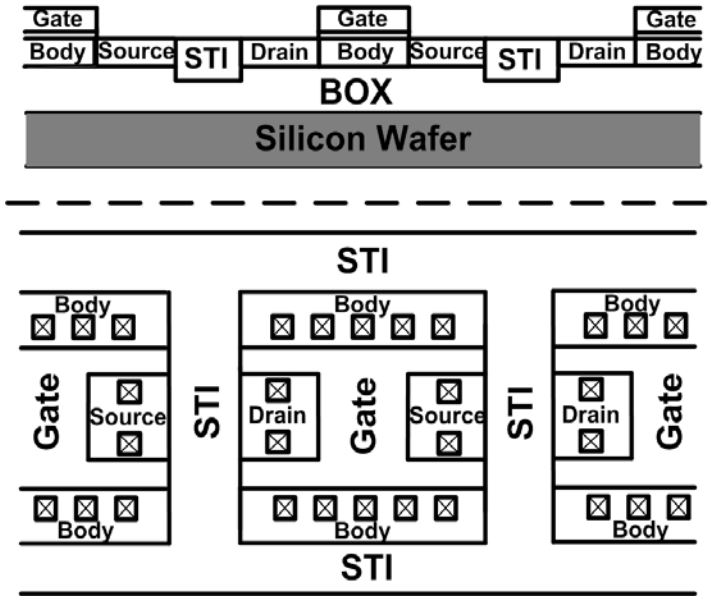


Figure 1.2: SOI device cross section and layout.

options available are wide bandgap materials such as Silicon Carbide (SiC), Gallium Arsenide (GaAs), diamond and SOI. Among them, SOI is a more popular technology, since it is well established and commercial SOI processes are available.

The advantage of SOI over bulk CMOS for high temperature ICs are as following. Firstly, the junction leakage is reduced because of the reduced PN junction area due to the Buried Oxide Layer (BOX). Secondly, latch-up is completely eliminated in SOI because the devices are fully dielectrically isolated, laterally by trench isolation and vertically by BOX isolation. Hence, the parasitic bipolar transistors that enable latch-up do not exist. Figure 1.2 shows the cross-section and layout of an SOI device and illustrates the lateral and vertical isolation of SOI transistors. In addition to the reduction of junction leakage current, sub-threshold leakage is reduced in HT SOI processes as a result of the increased threshold voltage.

Transistors in SOI processs are classified as Partially Depleted SOI (PDSOI) and FDSOI (Fully Depleted SOI), depending on the thickness of the active silicon layer (at the surface above the BOX) relative to the depths of the source-drain junction and channel depletion layers in the device with the operating voltages applied. For a PDSOI transistor, the silicon surface layer is thicker than the depth of the depletion region in the channel, whereas for an FDSOI transistor, the silicon surface layer is equal to the depth of the depletion region in the channel. Thus, the bulk of the transistor will be partially depleted in PDSOI or fully depleted in FDSOI. To form a FDSOI transistor, the channel doping concentration must be low enough that the depletion region extends throughout the entire thickness of the silicon layer. When the silicon surface layer is thicker than about 200nm, the transistor will typically be partially depleted, unless the channel doping concentration is very low, in which case the resulting threshold voltage would be too low for practical CMOS applications.

Both FDSOI and PDSOI have pros and cons. The advantages of FDSOI over PDSOI are:

1) The sub-threshold slope of FDSOI is steeper compared to PDSOI. It allows low threshold voltages of FDSOI transistors for acceptable sub-threshold leakages. It also has low parasitic capacitance. These features make it suitable for low-voltage and low- power applications.
2) The electrical effects due to floating body effects such as ‘kink’ effect(discontinuity in the I_{ds} vs V_{ds} curve) is lesser for FDSOI compared to PDSOI.

However, the disadvantages of FDSOI include:

1) A body contact cannot be added to FDSOI, because a resistive body region does not exist under most operating conditions.
2) The device parameters such as threshold voltage of any CMOS device are sensitive to the silicon surface film thickness. This results in an additional source of process variance in the fabrication of FDSOI CMOS due to the smaller silicon thickness.

These are the reasons why, at present, the fabrication of commercial CMOS on SOI typically employs partially depleted (PD) devices and hence for this research PDSOI is adopted.

1.3 HT Temperature Sensor

The main focus of this research is temperature sensors operating at high temperatures above 200°C. HT temperature sensor is a critical component in any oil-well instrumentation system. To measure the temperature, a temperature independent reference voltage is needed. Hence, design of voltage reference is an integral part of digital temperature sensor design. The sections 1.3.1 and 1.3.2 below give a brief overview of temperature sensor and voltage reference.

1.3.1 Temperature Sensor

Temperature sensor is a ubiquitous part of any electronic appliance today and is widely used in instrumentation and control systems. Figure 1.3 shows the global temperature sensor market classified on the type of industry of application. The popular temperature sensing methods are using RTD (Resistance Temperature Detector), thermocouple, thermistor and semiconductor thermal properties. The choice of the sensing method depends

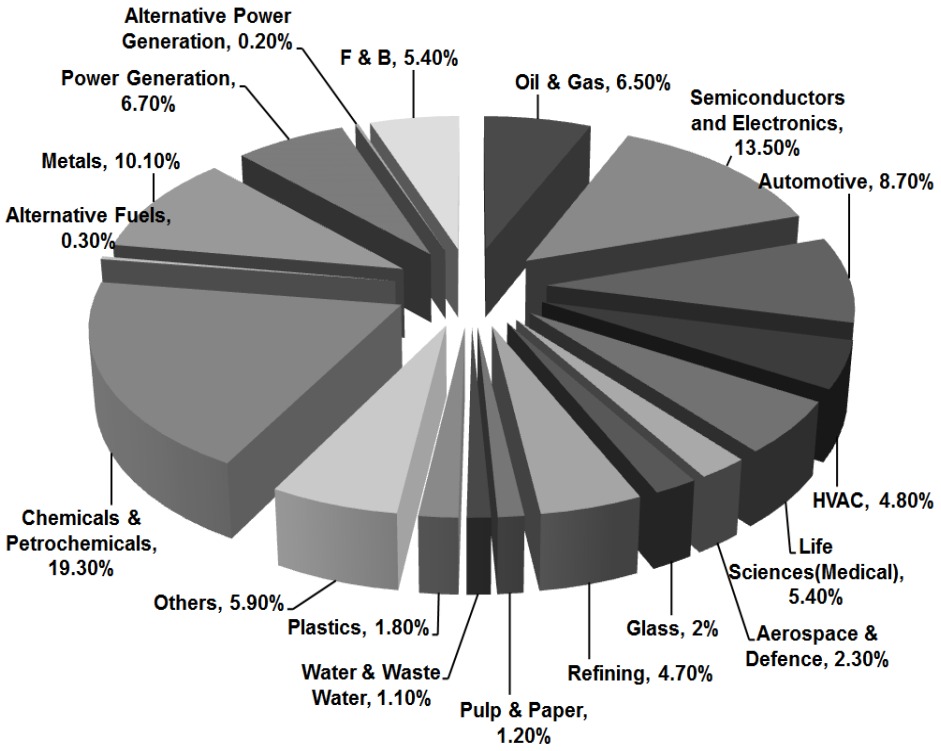


Figure 1.3: Global temperature sensor market (2011) [4].

on the temperature range of operation, linearity, accuracy, package, area occupied etc. The applications of temperature sensors can be broadly categorized into:

1) Temperature control, such as in thermostat.

2) On-board or chip temperature measurement, such as in microprocessors, for system performance and reliability.

3) Temperature compensation for circuits and systems whose performance varies with temperature.

4) Temperature information can also be used to sense some physical quantity which has a strong correlation to temperature.

Integrated sensors can be designed based on different sensing methods as given below.

1) The most popular among them is the bandgap based temperature sensor which is based on the temperature dependency of base-emitter voltage of a BJT or forward voltage of a diode which has a complementary to absolute temperature (CTAT) characteristic. Majority of industry grade sensors belong to this category. The early smart temperature sensors are mostly in bipolar technologies [5], [6], [7]. Since 1990's, bandgap temperature sensors based on CMOS technology have been published, which makes use of parasitic BJTs available in the CMOS process. Some of the pioneer CMOS designs are by Krummenacher [8] (1990) and Bakker [9] (1996).
2) The other popular temperature sensing method that is compatible with latest CMOS processes is the time-domain temperature sensors which are fully digital in nature [10]. The sensing principle of these sensors is based on the temperature dependency of inverter delay chains.
3) Resistor based temperature sensors [11] are based on the temperature dependence of on-chip resistors for sensing.
4) Recently, thermal diffusivity based temperature sensors have been reported. The sensing principle of these sensors is based on the time taken for the heat to diffuse through the substrate, which is dependent on thermal diffusivity [12].

Some of the key performance parameters of temperature sensors are operating temperature range, accuracy (including number of calibration points), power consumption and chip area. The weightage of the performance parameters varies from application to application.

1.3.2 Voltage Reference

For digitization of temperature, a temperature independent voltage reference is essential. In addition to the functionality as temperature independent reference for digital temperature sensor, voltage references also have applications in biasing circuits, ADC, DAC and power management circuits, etc.

Since most semiconductor physical parameters have temperature dependency, a temperature independent voltage is not readily available. Zero-order references such as reverse biased zener diode voltages are available but not suitable for precision application such as temperature sensing. Hence, at least first-order compensated references are always preferred, i.e the temperature independent reference is constructed from the cancellation of TC's (Temperature Coefficient) of two voltages which has well defined and reproducible temperature properties.

The most popular voltage reference is the Bandgap Voltage Reference (BGR). The idea was first proposed by Hilbiber in 1964 [13]. Since then a variety of circuit topologies based on the principle have been published. Some of the classic designs are by Wildlar [14], [15], Kuijk [16] and Brokow [17]. The basic principle of operation for BGR is the TC cancellation of forward voltage of a diode or base emitter voltage (V_{BE}) of a bipolar transistor with a ΔV_{BE} voltage (difference of V_{BE}'s of two transistors). The former has a CTAT (Complementary to absolute temperature) characteristic and the latter has PTAT characteristic. MOS transistor based voltage references have also been reported as they are fully compatible with CMOS processes. Their operating principles are mostly based on circuit topologies, which cancel the

temperature dependency of mobility or threshold voltage of the MOS transistors. In [18] , the inverse temperature dependency of mobility is used to cancel the threshold voltage temperature dependency of the MOS transistor and in [19] the difference of the threshold voltages of two transistors with similar temperature dependency but different absolute value is used, so that the difference of the two threshold voltages is temperature independent. Effectiveness of the temperature compensation over wide temperature range is evaluated by the box model TC metric [20]. A good TC is mandatory for application of voltage references for smart temperature sensor design. In addition to TC, the other performance metric is Power Supply Rejection Ratio (PSRR), since ideal voltage reference needs to be supply independent. Other parameters, such as power consumption, is also important.

1.4 Research Scope and Objectives

The main objective of this research is to design a smart temperature sensor and a voltage reference for ruggedized electronics system operating at temperatures above 200°C. The intended application is the data logging system for oil well drilling, where both temperature sensor and voltage reference are needed. The operating temperature can be as high as 250°C. The temperature sensor is used during the logging process where, temperature, together with other electrical measurements, is logged for understanding of the oil-well characteristics. It is also used for temperature compensation of other function blocks in the system. The voltage reference is used as a temperature independent reference for the temperature sensor and is also a critical part of other blocks in the system, such as power management blocks and bias circuits.

Few existing temperature sensors can operate above 200°C and their performances are limited at high temperature. The research in this thesis aims to develop temperature sensors and voltage references with enhanced performance and wide operating temperature range above 200°C.

1.5 Research Contributions

The research in this thesis has made the following contributions:

The SOI technology is not a familiar technology for the mainstream circuit designers. Hence, device and technology study is done and differences from bulk CMOS are identified. Prototype circuits are fabricated and high temperature measurement methods were identified. This ground work enabled progress of this PhD research as well as for the HT electronics group.

A new temperature sensor front-end based on threshold voltage extraction principle is proposed and demonstrated. The voltage reference is also designed as part of the temperature sensor front-end and achieves the best TC reported in the HT category. In addition, this design has one of the widest temperature range reported in literature.

In the second part of this thesis, a new time-domain architecture for a bandgap based temperature sensor without an explicit bandgap reference is proposed. It is power and area efficient and achieves excellent performance in the high temperature category. This architecture is not limited to SOI and high temperature applications and can be easily ported to bulk CMOS for applications such as microprocessor thermal monitoring. To the best knowledge of the author, this design is the first bandgap based temperature

sensor operating above 200°C and has the best FOM in this category of temperature sensors operating above 200°C.

1.6 Publications

The following publications are generated from the research in this thesis.

[1] J. Pathrose, L. Zou, K. T. C. Chai, M. Je, and Y. P. Xu, "Temperature Sensor Front End in SOI CMOS Operating up to 250°C," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 61, pp. 496-500, 2014.

[2] J. Pathrose, C. Liu, K.T.C Chai and Y.P Xu, "A Time-Domain Bandgap Temperature Sensor for High Temperature Applications," (Accepted for publication in *IEEE Transactions on Circuits and Systems II: Express Briefs*).

[3] J. Pathrose, L. Zou, K. T. C. Chai, M. Je, and Y. P. Xu, "A time-domain smart temperature sensor without an explicit bandgap reference in SOI CMOS operating up to 225°C," in *2013 IEEE Asian Solid-State Circuits Conference (A-SSCC)*, 2013, pp. 173-176.

[4] J. Pathrose, X. Gong, L. Zou, J. Koh, K. T. C. Chai, M. Je, and Y. P. Xu, "High temperature bandgap reference in PDSOI CMOS with operating temperature up to 300°C," in *2012 IEEE International Symposium on Radio-Frequency Integration Technology (RFIT)*, 2012, pp. 110-112.

[5] L. Zou, J. Pathrose, K. T. C. Chai, M. Je, and Y. P. Xu, "Sample-and hold circuit with dynamic switch leakage compensation," *Electronics Letters,* vol. 49, pp. 1323-1325, 2013.

A provisional patent also has been filed for the project which is given below.

[1] Jerrin Pathrose, Yong Ping Xu, Minkyu Je, Lei Zou, Kevin TC Chai, Jeongwook Koh, "Vth Extraction Circuit in SOI CMOS for Temperature Sensor and Voltage Reference," *SG provisional patent*, filed on 31 Jan. 2013 (SG 201300779-4).

1.7 Organization of the thesis

The thesis is organised as follows:

Chapter 2 is the literature review and divided into two parts. First part discusses the techniques for HT and wide temperature design with emphasis on biasing and leakage compensation. The second part presents the existing works on various smart temperature sensor designs. This part is further divided into sensing mechanisms and voltage reference which is part of the sensor front-end. Various categories of sensing mechanisms in literature are studied and the trade-offs are identified for each category.

Chapter 3 presents the proposed threshold voltage based temperature sensor front-end. It describes the threshold voltage temperature dependency, the proposed extraction circuit, the voltage reference design and the simulation results. The experimental results on silicon and discussion, as well as the comparison with other state-of-the-art works and the limitations of the design are presented in the end.

Chapter 4 describes the proposed time-domain smart temperature sensor design based on bandgap sensing principle. Two versions of the design are presented. The architecture, simulation and measurement results of both

versions are given. The discussion and comparison with other state-of-the-art works are also presented.

Chapter 5 summarizes the findings of this thesis. The future works are also suggested at the end of the Chapter.

CHAPTER 2

LITERATURE REVIEW

Integrated temperature sensors have become popular during last 30-40 years. Several sensing methods, architectures and design techniques have been established during this period. This Chapter reviews the existing designs and discusses the advantages and disadvantages of each. As the research focus in this thesis is on temperature sensors for high temperature applications, the existing HT design techniques are first reviewed. Finally, the works reviewed in this chapter are summarized.

2.1 HT design techniques

The initial HT designs are mostly in bulk CMOS and use circuit techniques to mitigate leakage issues. In addition to leakage compensation, various temperature compensation techniques have also been proposed for wide temperature range design. These techniques will be reviewed in the following sub-sections below.

2.1.1 Leakage Compensation

Leakage current is the most important factor which prevents bulk CMOS circuits from robust operation at high temperatures. Designs using mainstream bulk CMOS have been demonstrated to operate up to 250°C. They apply leakage compensation techniques to extend the temperature range. However, these techniques introduce additional design constraints which limit the sensor performance. The major source of leakage current is the drain (source) reverse

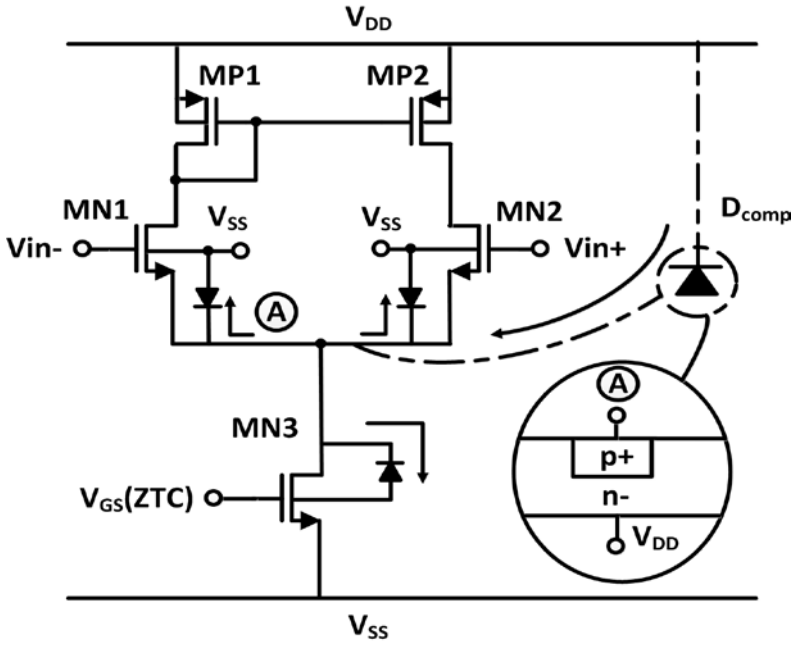


Figure 2.1: Differential pair leakage compensation [22].

biased diode junction leakage current. This leakage is dominated by generation-recombination leakage up to 130-150°C and diffusion leakage for temperatures above that. Reference [21] models the leakage current in conventional CMOS processes and its effect on the characteristics of typical analog sub-circuits.

The leakage compensation applied to the differential input stage and output stage of an op-amp is given in [22]. The technique is to match the leakage current at each critical node so that the operating point is maintained over the temperature range of interest. For example, the node *A* in Figure 2.1, has an imbalance in the leakage currents (all leakage currents flowing out of the node) and hence it results in a drift in the bias conditions with temperature. Therefore, a compensation diode D_{comp} is added to match the leakage current at this node. The junction area of the diode should be such that it can balance the leakage currents of MN1, MN2 and MN3. For the output stage shown in Figure 2.2 , the leakage current matches as far as the direction of current flow

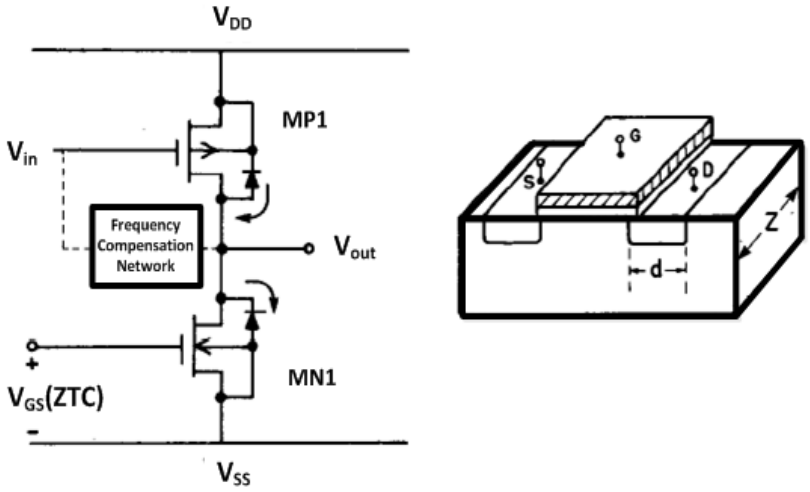


Figure 2.2: Output stage leakage [22].

is concerned. However, for magnitude cancellation, the area of the reversed biased diodes should also match. The condition for complete cancellation is

$$W_P(MP1) \cdot d_p(MP1) = W_N(MN1) \cdot d_n(MN1) \quad (1)$$

where d_p, d_n , W_p and W_n are the diffusion length of NMOS, diffusion length of PMOS, width of NMOS, width of PMOS transistor respectively. However, the sizing is determined by the various performance metrics such as driving strength, slew rate, bandwidth etc. which are crucial for operation in the normal temperatures. One option is to use compensation diode with appropriate sizing like in Figure 2.1 , but this is at the expense of additional capacitance. Thus, there is a trade-off between temperature range and the performance. This is a serious constraint in realizing the full potential of the circuit and hence alternate technology options need to be considered. SOI technology is very promising in this regard and has given more flexibility to the designer to optimize the performance. Therefore, in this research SOI technology is adopted.

2.1.2 Biasing

For HT and wide temperature range operation, the biasing techniques should be robust and stabilize the performance of the circuit. Two biasing techniques have been commonly adopted. They are Zero Temperature Coefficient (ZTC) biasing and g_m/I_d method.

2.1.2.1 ZTC

ZTC biasing point corresponds to a gate voltage/drain current operating point which remains constant with temperature. ZTC biasing [22] is one of the important techniques in high temperature design especially for OTA. The principal advantages of ZTC technique are [23]:

1) It maintains a constant operating point over a wide range of temperatures such that no transistors operate out of saturation.
2) It allows for a similar relative decrease in transconductance of the transistor such that the poles and zeros keep the same relative position, thus ensuring stability of the circuit over a wide range of temperatures.
3) Design simplicity and ensures reliable circuit operation when several stages are used.

ZTC technique, as shown in Figure 2.3, has been very effective in maintaining stable operating point and hence reliable circuit operation as proven in [23]. It provides a bias point that is temperature independent. However, it results in performance degradation of the amplifier over wide temperature ranges.

The main disadvantages of ZTC are:

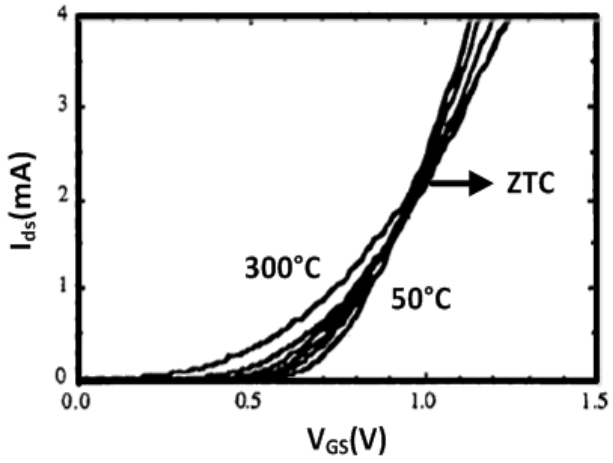


Figure 2.3: ZTC bias point [23].

1) The ZTC bias point corresponds to strong inversion region for bulk as well as PDSOI, unlike in FDSOI [23] where ZTC bias point is in the moderate inversion region. The high overdrive voltage associated with ZTC bias for PDSOI as well as bulk CMOS results in reduced intrinsic gain due to the low g_m as well as reduced signal swing.
2) The g_m decrease with temperature can affect the small signal performances of the amplifier like gain, bandwidth etc., especially when the amplifier is required to operate over a wide range of temperatures.

2.1.2.2 g_m/I_d

g_m/I_d is a design technique that allows a unified design methodology in all regions of operation of the MOS transistor [24]. In this method, the relationship between the ratio of the transconductance g_m over dc drain current I_D and the normalized drain current $I_N = I_D/(W/L)$ is used as a fundamental design metric. The choice of g_m/I_D is for the following three reasons [24]:

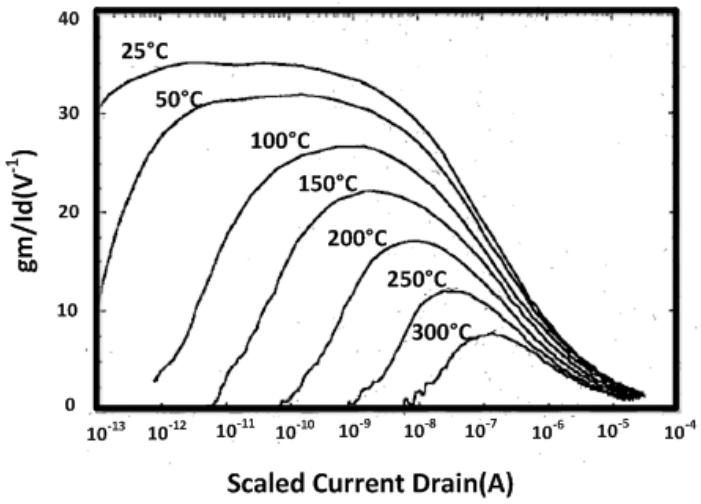


Figure 2.4: g_m/I_D curves of SOI NMOS transistor for various temperatures [24].

1) Many performance metrics of analog circuits can be expressed in terms of g_m/I_D. For example, the dc gain A_V of a common source amplifier can be expressed in the form

$$A_V = -\frac{g_m}{I_D} V_A \tag{2}$$

where V_A is the Early Voltage which controls the small signal output conductance.

2) g_m/I_D gives an indication of the device operating region. It has a maximum value of $1/(nV_T)$ where n is the sub-threshold slope factor and V_T is the thermal voltage. The value decreases as the operating point moves towards strong inversion.

3) g_m/I_D can be used for calculating the transistor dimensions based on the desired performances.

Figure 2.4 shows the g_m/I_D vs. $(I_D/(W/L))$ plot for different temperatures. The maximum plateau value on the left and hyperbolic behaviour on the right side of the figure corresponds to weak and strong inversion, respectively. In

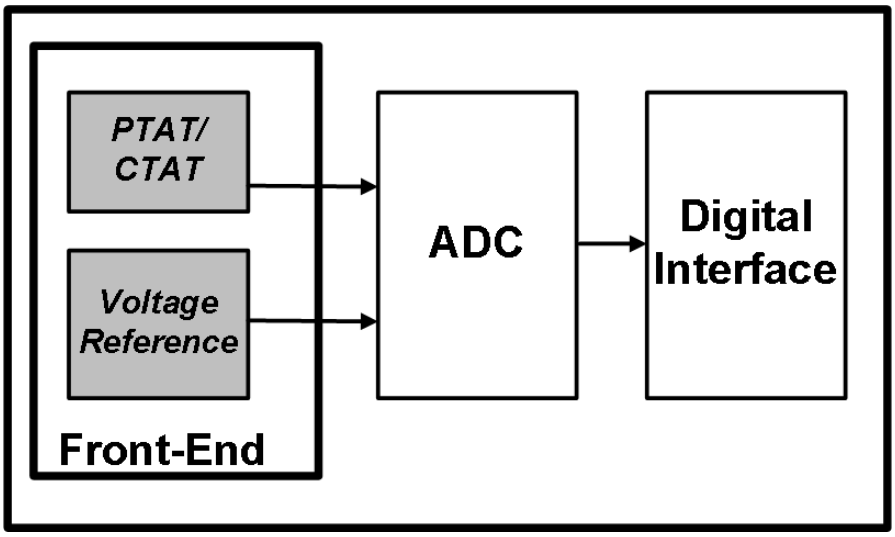


Figure 2.5: Typical smart temperature sensor architecture.

between comes the moderate inversion. By applying the g_m/I_D design methodology, the plot can be used for design at specified temperatures. From the plot it can be observed that, for stabilization of g_m/I_D over wide range of temperatures, the transistor has to be operated in the strong inversion region. At lower I_D, the leakage current dominates at higher temperatures and g_m/I_D tends to zero as can be seen from Figure 2.4. The low value of g_m/I_D is because leakage current superimposes on the sub-threshold channel current at higher temperatures. In strong inversion the g_m/I_D degradation with temperature is due to the decrease in mobility.

2.2 Smart Temperature Sensor

The typical architecture of a smart temperature sensor is shown in Figure 2.5. It consists of an analog temperature sensor front-end (CTAT or PTAT signal and voltage reference) [25], [26] and an ADC for digitization. The temperature signal is compared with various temperature independent reference voltage levels to digitize the temperature. This is equivalent to taking ratio of the temperature signal to the reference voltage, which is the

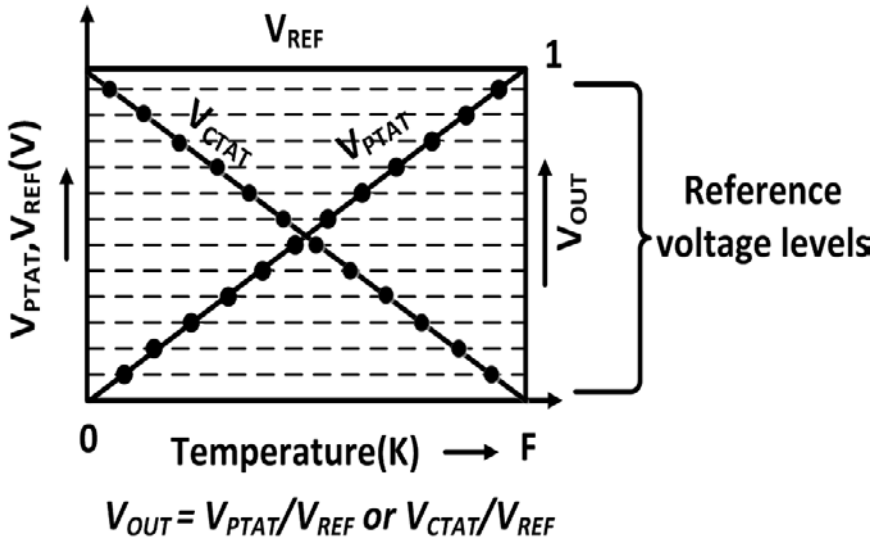


Figure 2.6: Ratiometric concept for temperature measurement.

concept of ratiometric measurement [7]-[9]. Figure 2.6 illustrates the ratiometric sensing technique for a general temperature sensor for either PTAT voltage V_{PTAT} or CTAT voltage V_{CTAT} and reference voltage V_{REF}. Here, V_{OUT} is the ratiometric output and the dotted lines are the various ratiometric outputs or the reference voltage levels corresponding to different temperatures. F is the full scale temperature. From the ratiometric output V_{OUT}, the temperature in Kelvin is obtained by simple linear scaling, namely, $F \times V_{OUT}$ for PTAT output and $F \times (1\text{-}V_{OUT})$ for CTAT output.

2.1.3 Voltage Reference

Voltage reference is a critical circuit for ratiometric measurement of temperature as illustrated in Figure 2.6. So far, bandgap reference is the most popular category of voltage references. In addition, references based on mobility and a threshold voltage has also been proposed.

The basic principle of a BGR is to cancel the temperature coefficient (TC) of the base-emitter voltage V_{BE} which has a negative TC or Complementary to

Absolute Temperature (CTAT) characteristic, with a PTAT voltage from the difference of two base-emitter (ΔV_{BE}) biased at different current densities, which has a positive TC. V_{BE} can be expressed using the following equation

$$V_{BE} \approx V_{go} - \frac{T}{T_r}[V_{go} - V_{BE}(Tr)] - (\eta - x)V_T \ln(\frac{T}{T_r}) \quad (3)$$

where V_{go} is the base-emitter voltage at 0°K, equal to the bandgap voltage of silicon which is ≈ 1.2V, $V_{BE}(Tr)$ is the V_{BE} at reference temperature T_r , η is a process dependent constant and x is the temperature dependent exponential of the bias current. As observed from the equation, there is a linear term as well as a non-linear logarithmic term which results in non-linearity. However, the non-linear term is much smaller compared to the linear temperature dependency and hence the first and most important target is to cancel the linear component using a PTAT voltage.

The PTAT voltage, $\Delta V_{BE,}$ or CTAT voltage, V_{BE}, along with the reference forms the temperature sensor front-end. Several topologies have been proposed for BGR with high performance. Two BGR designs, one in the conventional temperature [27] and one in the high temperature category [28] are discussed here. One of the main error sources in any BGR design is the process variation of V_{BE} , the main reason for which is the process spread of saturation current I_s which is dependent on base doping and transistor area. Analysis in prior literature shows that a difference of ΔI_s, (I_s+ ΔI_s) due to process variation results in a V_{BE} variation of $-V_T \cdot (\Delta I_s / I_s)$ which has a PTAT characteristic. Moreover, since V_{BE} at 0°K is a physical constant, namely, the bandgap voltage, the process variation of V_{BE} has just one degree of freedom and hence one-point calibration is enough to mitigate the process variation.

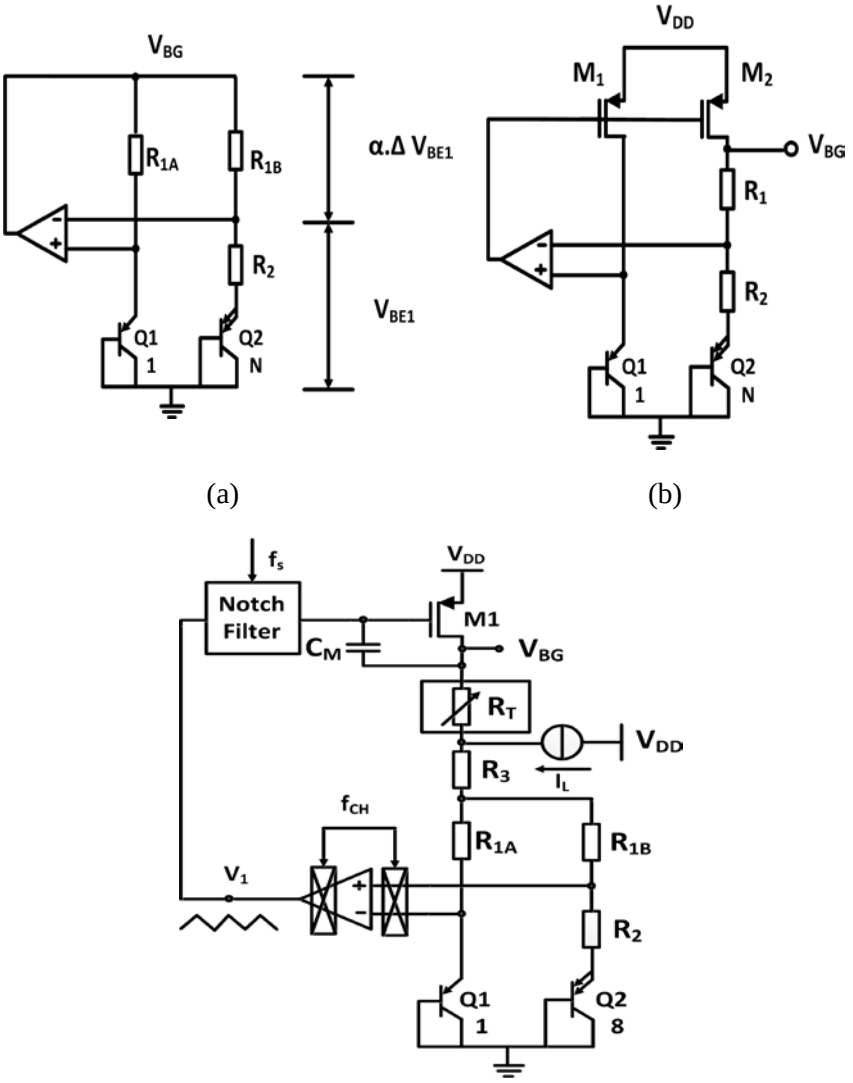


Figure 2.7: (a), (b) Typical BGR circuits, and (c) circuit in [27].

This is one of the significant advantages of BGR based reference, as well as temperature sensor.

Two of the typical designs for a bandgap reference are given in Figure 2.7 (a), (b). Design (b) eliminates the loading effect of the amplifier in (a) and thus avoids the buffer stage for the op-amp. The mismatch between the transistors M1 and M2 in (b) due to threshold voltage and aspect ratio mismatch results in a non-PTAT error. Hence a BGR with several improvements is reported in

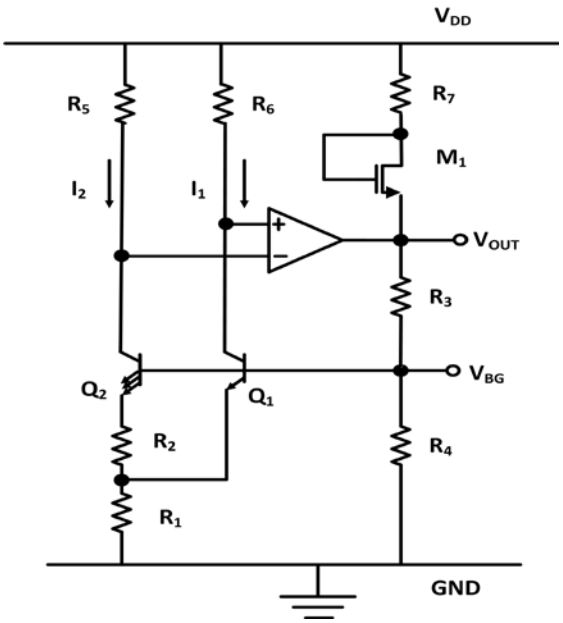


Figure 2.8: High temperature BGR using lateral PNP [28].

[27], as shown in Fig. 2.7(c). Reference [27] identifies that the major sources of error are resistor and transistor mismatches, V_{BE} and ΔV_{BE} process variation, V_{BE} non-linearity, op-amp offset and errors due to packaging stress and presents various techniques to remove the error sources in a BGR, as well as design considerations of a general BGR.

This design adopts a matched resistor topology and uses substrate PNP as the sensing element. As op-amp offset typically results in a non-PTAT error, the error cannot be cancelled by trimming and the error also has a statistical variation. Hence, chopper stabilization is applied for offset cancellation. Chopping technique is adopted due to the fact that it has a continuously available output, unlike auto-zero cancellation where output is available only during one phase. However, chopping typically needs large external capacitors to remove the high frequency ripple due to the up-modulated offset. In this work the ripple is removed by a switched-capacitor notch filter [29], [30] in the feedback loop as shown in Figure 2.7 (c). V_{BE} process variations as well as

other PTAT errors due to mismatches are removed by trimming R3. R_T is part of the resistor R_3 which can be trimmed. I_L models the leakage current of the switches used for trimming. R_3 is selected as the trimmable resistor due to leakage current considerations. The error due to leakage current increases by $I_L.R_3$, if R_{1A} is trimmed instead of R_3. To reduce stress related errors, the dies are packaged with a stress-relieving coating between the die and the molding.

The high temperature bandgap reference in [28] is one of the few works operating above 200°C. It is implemented in FDSOI technology. The device used is lateral-pnp transistor derived from SOI transistor using body as base and the gate biasing is such that the transistor is in accumulation region. The use of lateral-pnp facilitates the adoption of the classical BGR topology [16] in Figure 2.8 unlike substrate-pnp where substrate is grounded always. Nevertheless, substrate PNP is still a superior device in terms of better BJT characteristics. The amplifier used is a single stage OTA and the biasing technique applied is ZTC biasing which is the popular technique for HT designs, which is explained in Section 2.1.2.1. This design achieves a TC of 100ppm and consumes 200µA from a 4.5-V supply.

The non-BGR category of references is based on the temperature dependency of mobility and threshold voltages (V_{th}) of MOS transistors. They have simpler circuit topologies and less error sources compared to BGR. References based on V_{th} difference of same type of devices (NMOS or PMOS) have been reported [31]–[33]. In these works, different V_{th} is generated with additional process steps, which is costly or may not be feasible in the available commercial processes.

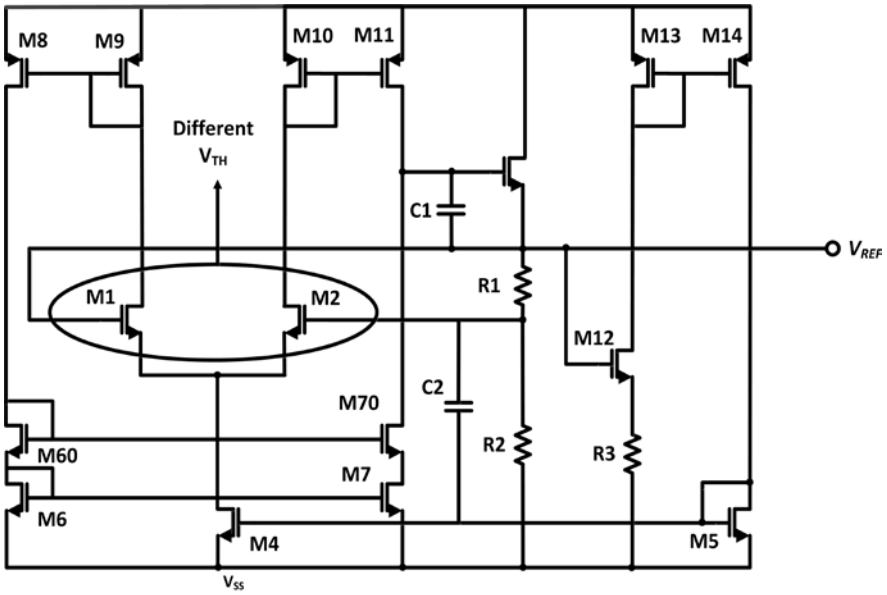


Figure 2.9: Threshold voltage based HT reference [33].

The high temperature work among these [33] achieves a TC of 50ppm for a temperature up to 200°C. The circuit topology of [33] is shown in Figure 2.9. This design uses a thin film (100nm) Separation by Implantation of Oxygen (SIMOX) technology which is similar to SOI technology and thus reduces leakage current at high temperatures. The design has an op-amp in feedback configuration. The differential pair transistors M1 and M2 are fabricated to have different threshold voltages by virtue of the different doping concentrations. Since M1 and M2 are biased by identical drain currents, the V_{GS} difference is same as the V_{TH} difference and hence the output is a temperature independent voltage which is proportional to the difference of threshold voltages.

Voltage references based on threshold voltage properties with transistors operating in sub-threshold region are useful in low power applications [34]–[36]. However, the leakage currents at high temperatures, as well as large mismatch and process variations, limit the robustness of such references.

Voltage references based on V_{GS} difference [37] and threshold voltage difference of NMOS and PMOS transistors [38] have good TC, but have limited temperature range up to 130°C. The mobility ratio term for the reference voltage in [37] limits the operating temperature range since complete compensation is achievable only at a desired reference temperature, and therefore its application for temperature sensing is limited to temperature threshold detection [39], [40] at the reference temperature.

SiC technology based designs are gaining popularity for HT designs, though it is costly. An HT design has been published recently [41], which is based on the temperature dependencies of mobility of SiC transistor and the TC of a Schottky diode. The design achieves a mean box model TC of 71ppm with a power consumption of 1.8mA and a PSRR of -47.6db@100Hz, up to 250°C.

2.1.4 Temperature Sensor

Various sensing mechanisms have been proposed for smart temperature sensors. These include bandgap based temperature sensors, time-domain temperature sensors, resistor based and most recently thermal diffusivity based temperature sensors. In the following sub-sections, overviews of these temperature sensors are presented.

2.1.4.1 Bandgap based temperature sensors

Bandgap based temperature sensors have been the widely adopted sensing mechanism because of the robustness of the temperature characteristics of BJT and its well established design methodology. Bandgap based temperature sensor designs are predominantly voltage domain temperature sensors.

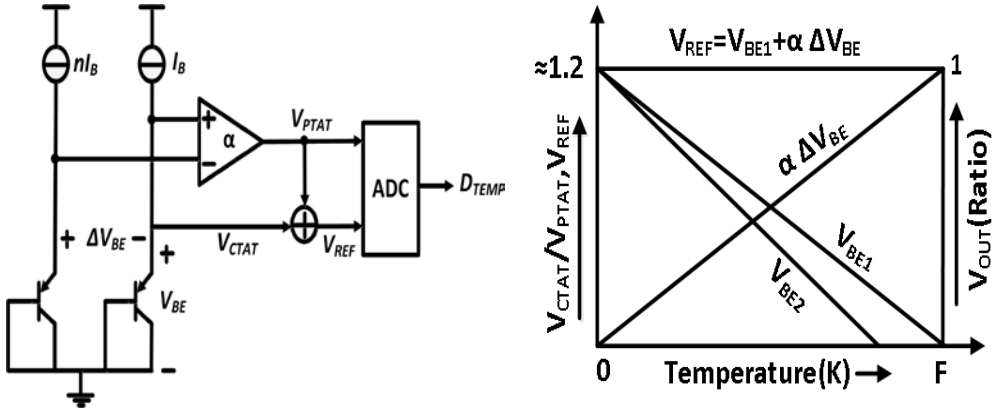


Figure 2.10: Operating principle and bandgap voltages characteristics.

The front-end (Figure 2.5) of a bandgap smart temperature sensor is well known and is based on the BGR principle which is explained in Section 2.1.3. The PTAT voltage V_{PTAT} (sensing signal) and V_{REF} (BGR) are generated by the front-end. The ADC does the ratiometric measurement as shown in Figure 2.6 of V_{PTAT} and V_{REF} and hence synthesizes the digital output. The operating principle and the corresponding bandgap front-end voltage characteristics are shown in Figure 2.10. The sensing device is substrate PNP transistor which is a parasitic device in CMOS process. It is preferred over lateral PNP because of its more ideal exponential characteristics due to factors such as more one-dimensional flow of current, less variations in saturation current due to lithographic errors in emitter area [42].

The bandwidth requirement for the temperature sensor is dependent on various factors such as thermal mass of package, power dissipated etc. Therefore, typical target for temperature sensors is around 10 conversions per second. Typical inaccuracies in the normal temperature range are within ±2°C for well-designed sensors in this category.

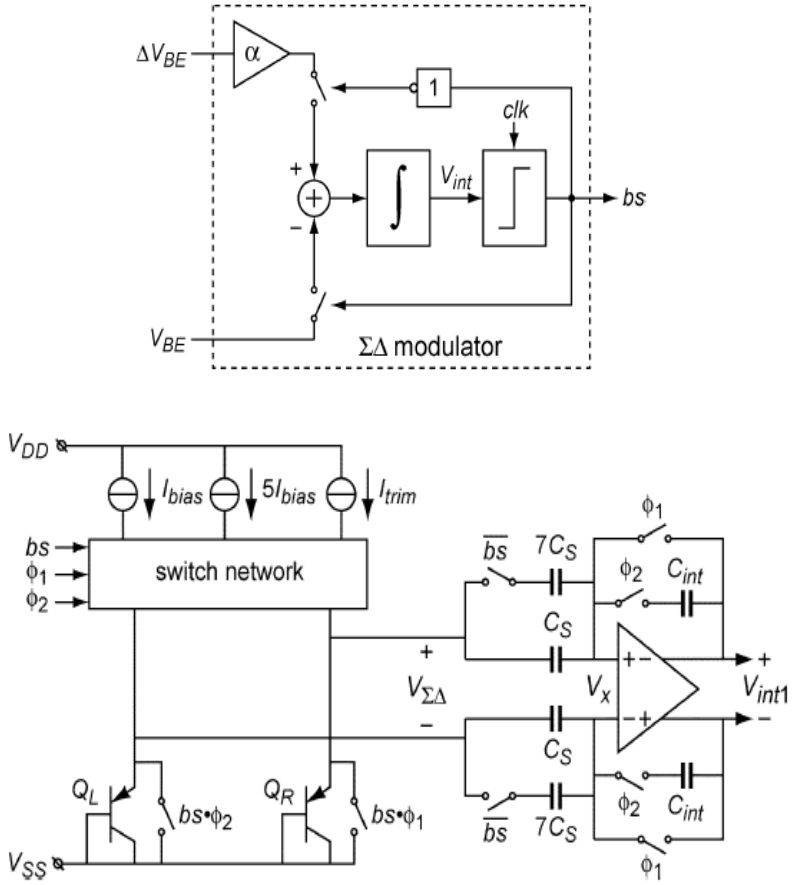


Figure 2.11: Block diagram and simplified circuit diagram [44].

Some of the notable CMOS smart sensor bandgap designs are [9], [43], [44]. Reference [9] is one of the pioneer works in this area. This work achieves a 2-point calibrated inaccuracy of ±1°C (uncalibrated accuracy of ±7°C) for a temperature range of -40 to 120°C. Precision techniques such as DEM, nesting chopping technique, curvature correction etc. are applied to reduce the errors and errors have been reduced to ±0.5°C [43] and ±0.1°C [44] for temperatures up to 120°C and 125°C respectively. [43] and [44] use low stress ceramic packages and the individual trimming is done after packaging to remove errors due to packaging.

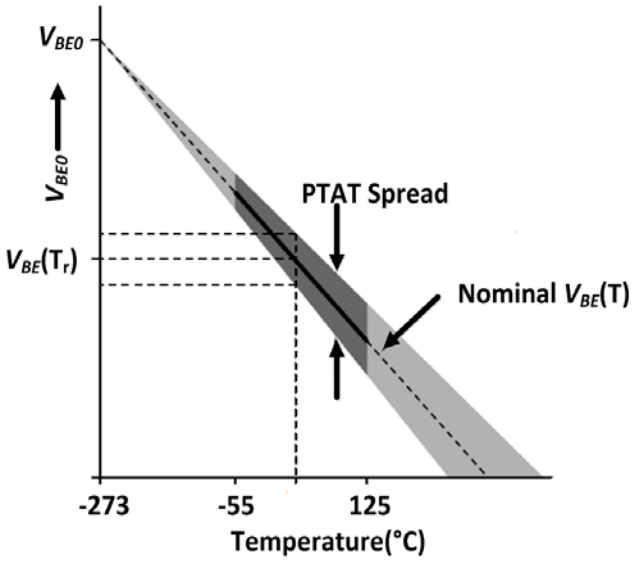


Figure 2.12: V_{BE} process spread.

This section will discuss the state-of-the-art temperature sensor based on bandgap principle [44]. This design achieves a state-of-the-art accuracy of ±0.1°C and operates up to 125°C. It is achieved by a combination of precision techniques and excellent device characterisation. The A-to-D conversion is done based on the sigma-delta modulation (SDM) principle and charge balancing. Figure 2.11 shows the block diagram and simplified circuit diagram of the temperature sensor. V_{BE} and $\alpha\Delta V_{BE}$ are integrated depending on the comparator output *bs* so that effectively the average input to the integrator is zero i.e the charge added by $\alpha\Delta V_{BE}$ is removed by V_{BE}. The average value of the bitstream μ is given by the following equation

$$\mu = \frac{\alpha\Delta V_{BE}}{V_{BE} + \Delta V_{BE}} = \frac{V_{PTAT}}{V_{REF}} \tag{4}$$

which corresponds to the ratiometric output V_{OUT} shown in Figure 2.6. The switched capacitor implementation of the design also facilitates offset and 1/f noise cancellation by correlated double sampling (CDS) technique.

Temperature dependencies of V_{BE} are the core of the front-end design. One of the major advantages of bandgap sensors is that the process variation of V_{BE} has just one degree of freedom about the 0K point. This facilitates one-point calibration at any temperature to mitigate this process variation. Figure 2.12 demonstrates this characteristic in a simplified way [42]. In addition, V_{BE} also has a curvature which is dependent on a process parameter as well as the temperature dependency of the bias current. To facilitate one point calibration of V_{BE}, the bias current needs to be trimmed. Trimming is achieved conventionally by adjusting the emitter areas or bias current of transistors by switchable transistors and current sources. Trimming is done in this work by a sigma-delta DAC which trims the bias current. This saves chip area when compared to the previous approaches such as binary scaled current/resistor trimming. It also achieves high resolution compared to other approaches. To improve the matching, Dynamic Element Matching (DEM) is applied, i.e the unit current sources are switched in the sigma-delta cycles and hence the mismatch errors are averaged out.

In spite of multiple error sources, the voltage domain bandgap temperature sensors achieve excellent accuracy using a combination of various error correction techniques, as well as excellent device characteristics. However, the design depends on analog intensive precision techniques and circuit design applied here are more suitable for early technology nodes. Recently, the same voltage domain bandgap sensors have been demonstrated in latest technologies [45] using vertical NPN transistors. However, precision analog intensive design in nanometer technology nodes is still a challenge.

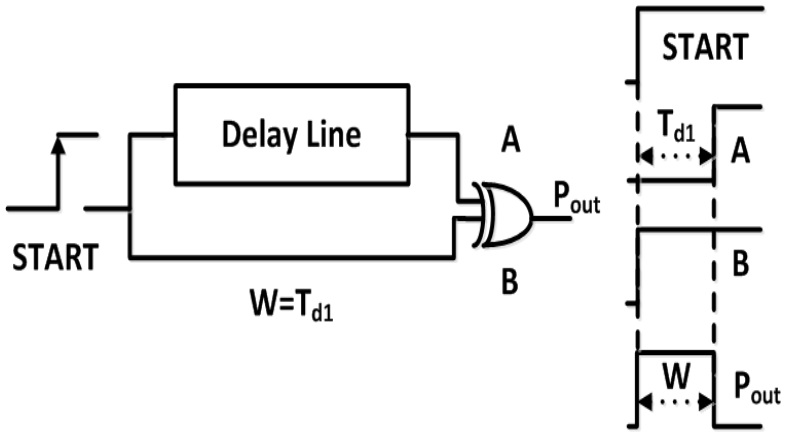


Figure 2.13: Basic temperature-to-pulse generator [10].

2.1.4.2 Time-domain delay chain temperature sensors

Time-domain temperature sensors based on delay chains was proposed so as to be fully compatible with digital CMOS processes. The basic building block of these temperature sensors is the temperature-to-delay cell as shown in Figure 2.13. Once the temperature dependent delay is obtained, it is digitized by a Time-to-Digital (TDC) converter [10]. The delay line invariably is made up of inverter chains whose propagation delay (average of low to high and high to low delay) is given by the following equation.

$$T_P = \frac{(L/W)C_L}{\mu C_{OX}(VDD - V_{TH})} \ln\left\{\frac{1.5V_{DD} - 2V_{TH}}{0.5V_{DD}}\right\} \quad (5)$$

where μ is the mobility, V_{TH} is the threshold voltage, V_{DD} is the power supply, W/L is the aspect ratio of an inverter with an equivalent NMOS and PMOS, C_L is the loading capacitance of the inverter. Here the temperature dependent factors are μ and V_{TH}. Since V_{DD} is much higher than V_{TH} , μ becomes the major temperature dependent factor. Mobility decreases with temperature and therefore T_P has a PTAT characteristic.

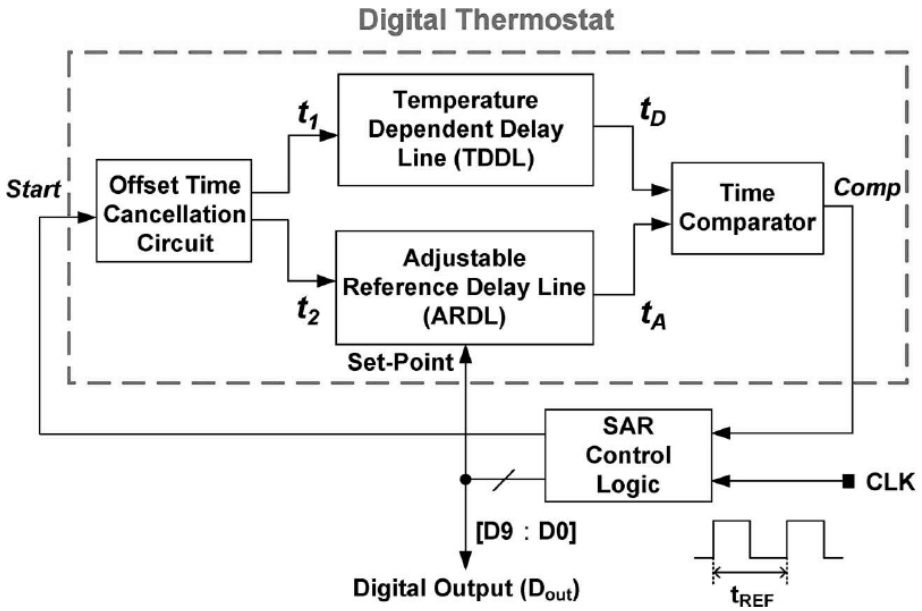


Figure 2.14: Time-domain SAR smart temperature sensor [46].

An implementation of the concept is given in [46] and the proposed architecture is in Figure 2.14. This is an improved version of [47] with SAR control logic to speed up the set-point programming. Temperature Dependent Delay Line (TDDL) produces a delay which is proportional to temperature. Offset cancellation circuit reduces or eliminates the delay at the lower end of the temperature range, thus reduces the measurement time and the output bits required. The time comparator is used to find the delay difference between the ARDL and TDDL delay lines and the SAR control logic adjusts the set-point so that ARDL delay matches TDDL delay.

The mobility dependence on temperature has a non-linear characteristic and therefore the propagation delay too has a curvature. The non-linearity error still exists even though the aspect ratios of TDDL are optimized for linearity enhancement. To mitigate this problem, instead of having a temperature compensated ARDL cell, a non-linearity is introduced in the ARDL cell, with the effect of linearizing the digital time-domain output as

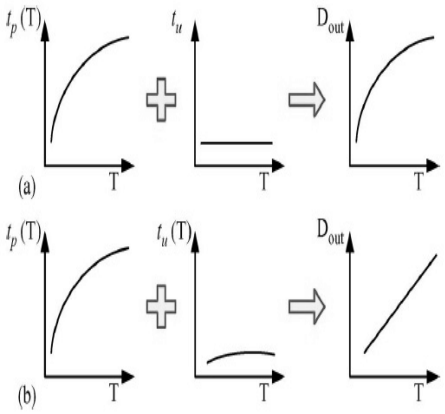


Figure 2.15: Linearity enhancement technique [46].

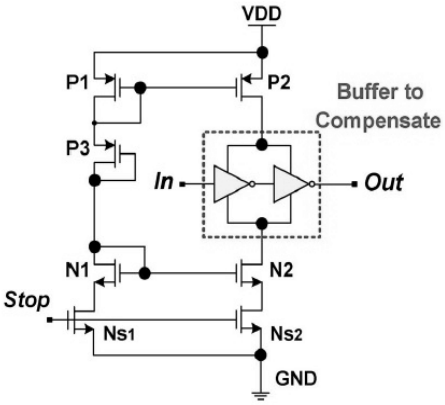


Figure 2.16: ARDL delay cell [46].

shown in Figure 2.15. The ARDL cell is shown in Figure 2.16. For an optimum V_{GS} voltage of P3 which is set by sizing of P1, P3 and N1 the conduction current is temperature independent. To achieve curvature compensation, the devices are sized such that minor temperature sensitivity is introduced to match the curvature of TDDL. However, this temperature compensation technique is only applicable for a small temperature range of 90°C as demonstrated in this work. The proposed design occupies and area of 0.6mm^2 in 0.35µm technology with 100 TDDL delay cells and 1024 ARDL delay cells and achieves a worst case inaccuracy of 0.6°C.

This category of sensors is the first fully-digital temperature sensors to be reported and hence can be seamlessly integrated into the latest CMOS technologies. One potential disadvantage is the limitation for spot sensing applications where the spatial temperature variation is to be measured since the temperature sensing is done by the entire delay chain in this case. As can be inferred from (5), the delay has a direct dependence on V_{DD} and therefore suffers from inherent supply rejection. In addition, two-point calibration is always needed for these sensors to mitigate the process variation.

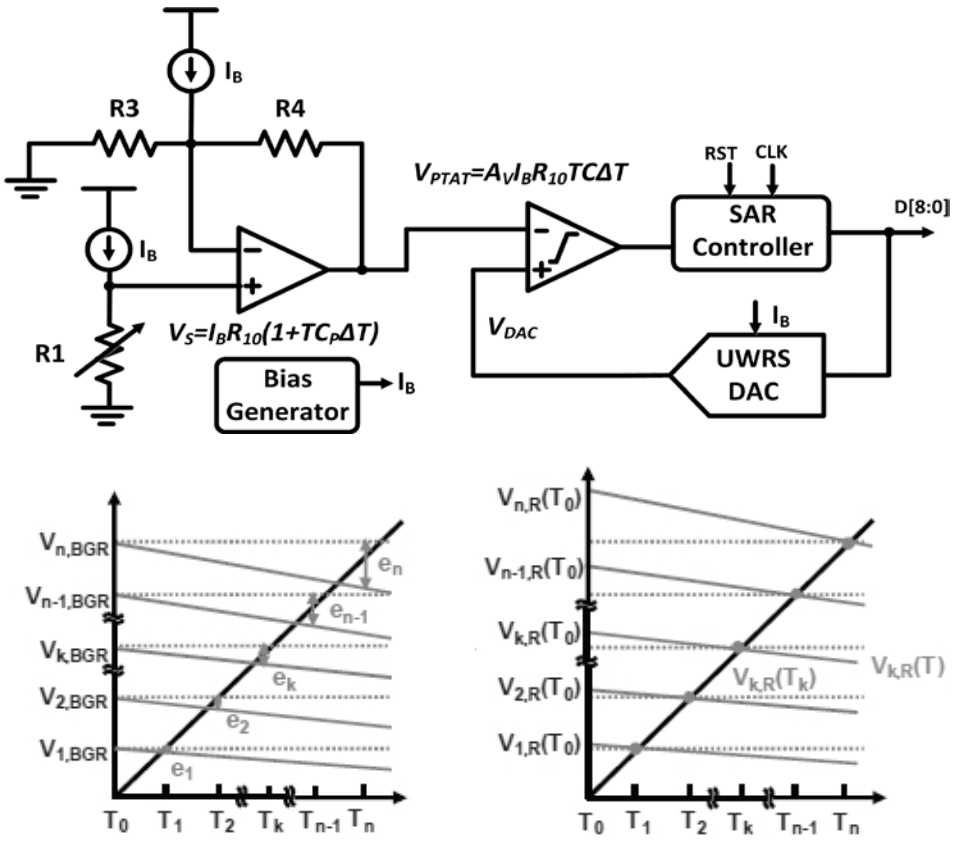


Figure 2.17: Block diagram and BGR free digitization technique [11].

2.1.4.3 Resistor Based

Platinum resistor based temperature sensors have been proposed for their precision and wide temperature range. Similarly, The TC of on-chip resistors has been used for temperature sensing purposes [11], [48]. The state-of-the-art resistor TC based temperature sensor is proposed in [11]. The temperature signal V_{PTAT} is generated as shown in the block diagram of Figure 2.17. SAR control logic is used to digitize the PTAT signal with the reference voltages derived from a BGR free resistor string. The expression for the PTAT output voltage is given by

$$V_{PTAT} = A_V \cdot I_B \cdot R_{10} \cdot TC \cdot \Delta T \quad (6)$$

where $A_V = (1+R_4/R_3)$ and TC is the difference of the TC's of R_1 and R_3 (R_4). To maximize the temperature sensitivity, resistors with positive temperature coefficient TC_P is chosen for R_1 and negative temperature coefficient TC_N for R_3, R_4 are used. To obtain the desired PTAT signal the relationship $R_{10} = R_{30} \parallel R_{40}$ needs to be satisfied which is attained by one-point calibration. R_{10}, R_{30}, R_{40} are the resistance values of R_1, R_3, R_4 at 0°C.

Conventionally, a BGR is required for the DAC in SAR digitization. However, obtaining a precise BGR with minimum TC for temperature sensing application is non-trivial. The contribution of this work is in avoiding the use of a precision BGR for the SAR logic. The desired reference voltages obtained from an ideal BGR are shown by dotted lines in Figure 2.17. If a BGR is not used, assuming negative TC for the voltages, it results in an error in the reference voltages e_1, e_2, …e_n for the different reference levels. To solve this problem, the authors propose an Unevenly Weighted Resistor String (UWRS) DAC. The resistor string UWRS DAC produce the desired reference levels $V_{k,BGR}$, by designing the nominal reference voltage at T_0 for each k to be

$$V_{k,R}(T0) = \frac{V_{k,BGR}}{1 + TC_N \cdot (T_k - T_0)} \tag{7}$$

The temperature characteristics in (7) achieved in this design by adding compensating resistors of 0.5 R_{LSB} value into appropriate positions in the resistor string. This work has achieved state-of-the-art results for resistor based smart temperature sensor with an accuracy of 0.5°C for a temperature range of 100°C and consumes 20µA of current from 1.8V power supply.

The most critical requirement of this design is resistors whose TCs are well characterized and with less spread. In addition, some resistances may have a

second-order temperature coefficient, which contributes to non-linearity error for the temperature sensor. Considering the value of sensing resistors, which is 80 kilo-ohms, 100 kilo-ohms and 400 kilo-ohms for R1, R3, R4, respectively and hence the area occupied, this sensing method may not suitable for spot sensing/ spatial temperature detection within a chip, but suitable for general purpose applications.

2.1.4.4 Thermal Diffusivity

In the high temperature category of sensors, thermal diffusivity based sensors are promising. The advantage is their un-calibrated accuracy, which is limited only by lithographic spread and not by wafer-to-wafer or batch-to-batch spread. Hence, the accuracy has been found to improve with technology node. Almost all the category of sensors so far needs at least one-point calibration to achieve a decent performance. However, thermal diffusivity based sensors achieve comparable accuracy without calibration.

The basic sensing element of thermal diffusivity based sensor [49] is the Electrothermal Filter (ETF) the schematic and CMOS implementation of which is given in Figure 2.18. The ETF consists of a heater and a temperature sensor. The heat generated from the heater element diffuses through the substrate to create temperature fluctuations in the sensor. The time it takes for the heat to diffuse is a function of absolute temperature. The temperature dependent factor is known as thermal diffusivity D which has a temperature dependency of $1/T^{1.8}$. The phase shift Φ_{ETF} at the sensor output is given by the following equation

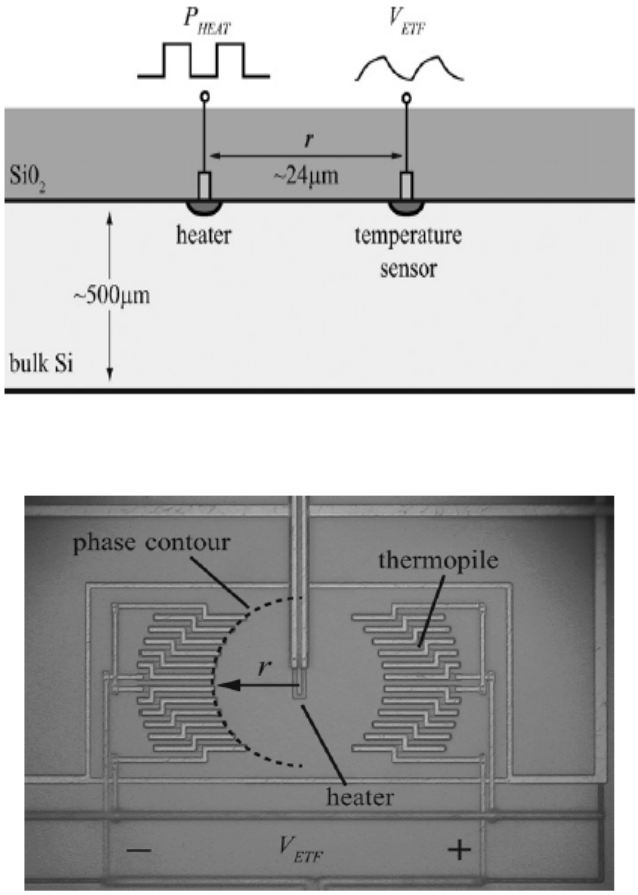


Figure 2.18: ETF schematic and CMOS layout [49].

$$\Phi_{ETF} = -r\sqrt{\frac{\Pi f_{drive}}{D}} \tag{8}$$

where f_{drive} is the driving frequency of the heater, r is the distance to the heater which in this work is 24μm and is accurately determined especially in latest technologies. Therefore if the f_{drive} is constant, Φ_{ETF} has an almost linear dependency with temperature of $T^{0.9}$. The heater in this work is a p+ diffusion resistor and the sensor is a thermopile made up of a series of diffusion/aluminium junctions.

One of the advantages of this category of sensor is that due to its time-domain nature, ETF's are unaffected by leakage currents. The buried oxide layer in SOI improves the SNR when compared to bulk CMOS

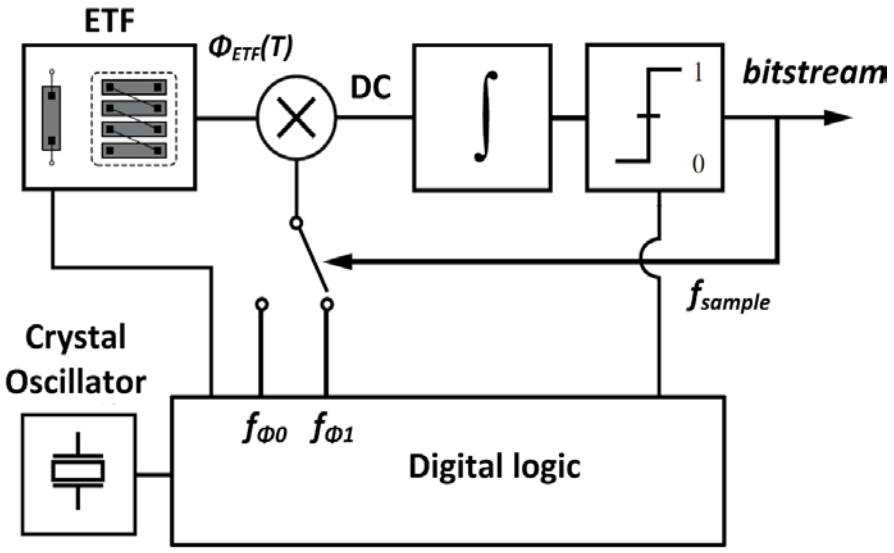
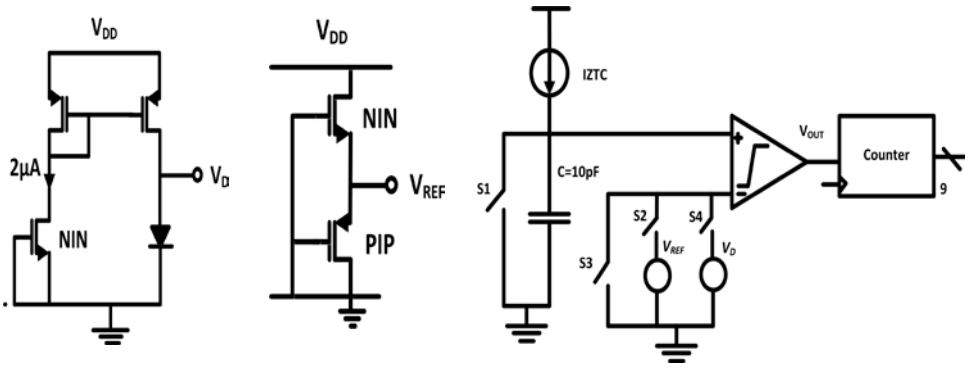


Figure 2.19: PDΣΔM read-out [49].

implementations [50], [51] due to the reduction in heat loss by the buried oxide layer. The output of the sensor is a phase shifted signal at a known frequency and hence the readout circuit is a phase detector.

The sensor achieves a 3σ un-calibrated accuracy of ±0.6°C up to 225°C. This category of sensors has the best reported un-calibrated accuracy. The design consumes a power of 3.5mW and occupies an area of 1mm^2. The limitation of power is due to the fact that the sensing mechanism is based on heat dissipation and the heat is generated by an electrical source. Due to the thermal isolation by BOX layer in SOI the power needed for heat source is lesser for SOI when compared to bulk CMOS. For optimum performance of this category of sensors thermal modelling of the ETF is essential [52]. This may need interdisciplinary expertise when compared to other category of sensors where the sensing mechanism is based on CMOS devices such as BJT, transistor, resistor etc.



(a) **(b)** **(c)**

Figure 2.20: (a) V_D, (b) V_{REF} and (c) ADC [54].

2.1.4.5 Time-domain ratiometric sensors

Two designs coming under this category are discussed in this section. One is a recent work from Intel [53]. Other design [54] is for high temperature work operating above 200°C. Both designs follow the ratiometric principle of comparing a temperature dependent signal to a temperature independent voltage reference. However, the ratiometric measurement is done in time-domain.

The technology used in [54] is FDSOI. The temperature dependent signal, generated by a SOI PIN diode V_D which has a CTAT characteristic and the reference voltage V_{REF} [55] are shown in Figure 2.20 (a) and (b), respectively. The ratiometric output is given by

$$\alpha = \frac{V_D}{V_{REF}} \tag{9}$$

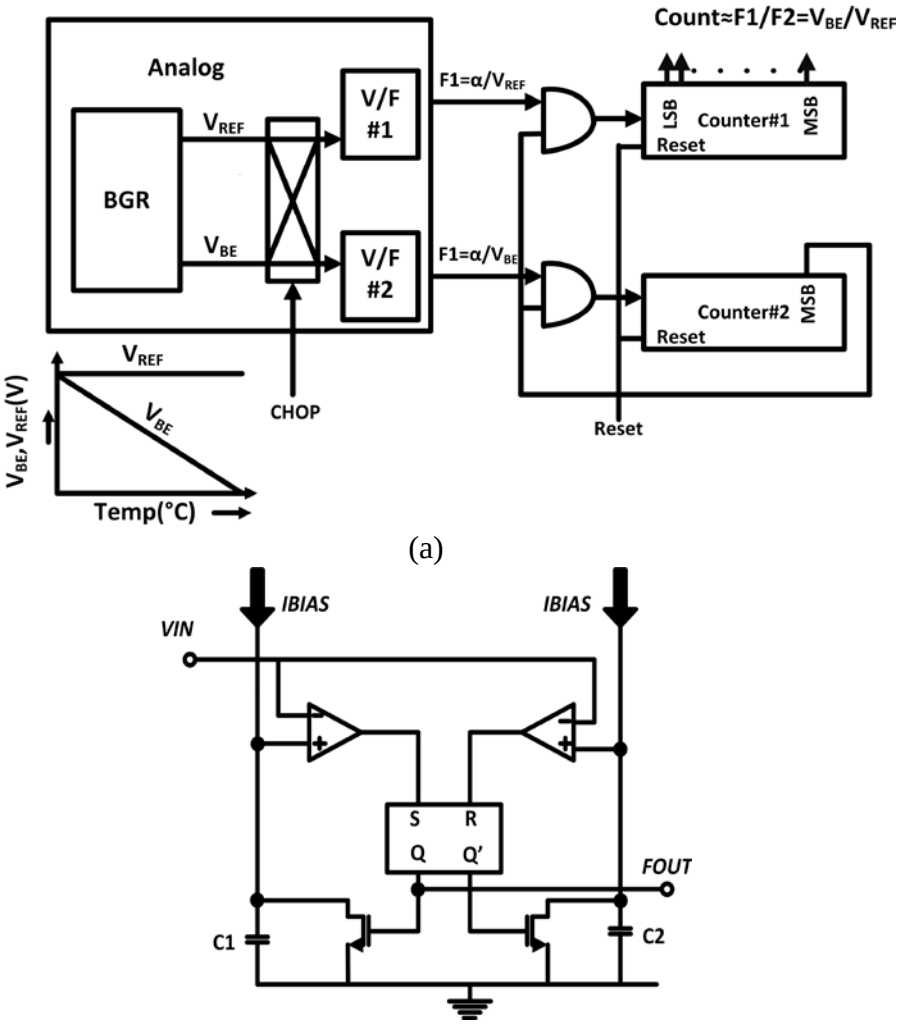


Figure 2.21: (a) Architecture (b) V/F converter.

The temperature sensor architecture is shown in Figure 2.20 (c). It is based on a conventional TDC architecture. The capacitor is charged with a ZTC current and the count to reach V_D is compared to reach the count $V_{REF,}$ which is fixed. The circuit achieves a temperature error of 3.9°C after 2-point calibration and 2.85°C after 7-point calibration. From the analysis by the author, it is found that the major reason for inaccuracy is the non-linearity/TC of the reference voltage V_{ref}. The total power consumption is 50µA from a 3 V supply. The

main advantage of this design is that the architecture is simple and hence power consumption is low. The architecture needs a precision voltage reference operating over a wide temperature range with good TC. The high temperature V_{ref} generator of this design [55] has a high TC which deteriorates the temperature performance. Another requirement of this architecture is that of a precise ZTC current which may be challenging to realize considering the process dependencies.

The second design in [53] is based on ratiometric principle and designed for thermal monitoring purposes. The main requirement for these applications is compactness so that the sensor can be placed in multiple locations. The accuracy requirements are relaxed and the typical accuracy needed is ±1°C at throttle and ±5°C at 50°C.

The architecture of this sensor is shown in Figure 2.21 (a). The analog part consists of a BGR which generates V_{BE} and V_{REF} and two voltage-to-frequency converters. The voltage to frequency converters are used to convert V_{REF} and V_{BE} to frequencies F_1 and F_2, respectively. The schematic of the V/F converter is given in Figure 2.21 (b). This sensor achieves a 3σ accuracy of <4.5°C after sensor and BGR calibration (resistor trimming) at 100°C. The design consumes 3.8mW of power and occupies a chip area of 0.02mm^2 and is fabricated in 32nm technology node.

2.2 Summary

Initial high temperature designs were done in bulk CMOS. Leakage at high temperatures is a bottleneck for robust operation bulk CMOS. This calls for special care with respect to leakage compensation/reduction in bulk CMOS

TABLE 2-1: SUMMARY OF VOLTAGE REFERENCE PERFORMANCE

Parameter	[33]	[28]	[41]	[27]
Technology	SIMOX	FDSOI	SiC	0.16-µm CMOS
Temperature Range	25–200°C	25–300°C	25–250°C	-40 – 125°C
TC(ppm)	50	100	71(mean)	5–12
Type	Threshold Voltage	Bandgap	Diode/ Mobility	Bandgap
Extra Masks	Yes	No	No	No
Samples	1	1	2	61
Calibration	N.A	N.A	N.A	1
Current	N.A	200µA	1.8mA	55µA
PSRR	N.A	N.A	-47.6db @100Hz	-74db@DC

[22]. Use of SOI technology enabled the circuit designer to focus on the performance of the circuit without being limited by leakage. Recently, SiC technology has also been used for HT design.

TABLE 2-1 summarizes the performance of the salient voltage reference designs discussed in the review. From the table it is found that there is further scope for performance improvement in the HT category and in turn, the HT

TABLE 2-2: SUMMARY OF TEMPERATURE SENSOR PERFORMANCE

Parameter	[54]	[49]	[46]	[44]	[53]
Process	FDSOI	0. 5µm SOI BiCMOS	0.35µm CMOS	0.7µm CMOS	32nm CMOS
Sensing	PIN Diode	Thermal Diffusivity	Delay Line	Bandgap	Bandgap
Calibration Points	2	0	2	1	1
Current	50µA	700µA	12µA	75µA	3.8mA
Accuracy	3°C	0.6°C	0.6°C	0.1°C	2.25°C
Area	N/A	$1mm^2$	$0.6mm^2$	$4.5mm^2$	$0.02mm^2$
Temperature Range	25 – 250°C	-70 – 225°C	0 – 90°C	-55 – 125°C	20 – 100°C
Inaccuracy FOM*	N/A	$5.6x10^5$	$2.3x10^4$	$2.3x10^3$	$3.1x10^3$

temperature sensor performance. TABLE 2-2 summarizes the performance of the salient temperature sensor designs discussed in the review. As far as HT operation is concerned, to the best knowledge of the author there is no BGR based temperature sensor operating above 200°C.

In this thesis, a non-BGR temperature sensor front-end based on threshold voltage operating up to 225°C and a time-domain bandgap smart temperature sensor up to 250°C are presented.

CHAPTER 3

THRESHOLD VOLTAGE BASED SMART TEMPERATURE SENSOR FRONT-END

This chapter proposes a temperature sensor front-end based on threshold voltage temperature dependency of NMOS and PMOS transistors. The core of this design is the threshold voltage (V_{th}) extraction cell. The proposed topology does not need op-amp or BJT's. The temperature information can be extracted from the ratiometric output of the CTAT and the reference voltage. The front-end achieves one of the widest operating temperatures reported in literature. The sections below describe the design.

3.1 Threshold Voltage Temperature Dependence

The V_{th} dependencies for bulk CMOS and thick film PD-SOI CMOS are analyzed in [56]. The TC of V_{th} is given by

$$\frac{\partial V_{th}}{\partial T} = \frac{\partial \phi}{\partial T}\left[1 + \frac{q}{C_{ox}}\sqrt{\frac{\varepsilon_{si} N_a}{kT \ln(N_a / n_i)}}\right] \tag{10}$$

where the Fermi potential Φ and intrinsic carrier concentration n_i is given by the following equations [57]

$$\phi = \frac{kT}{q}\ln\left(\frac{N_a}{n_i}\right),\ n_i = 3.9 \cdot 10^{16} \cdot T^{3/2} \cdot e^{-(Eg/2kT)} \tag{11}$$

q is the electron charge, k is the Boltzmann constant, N_a is the doping concentration, ε_{si} is the silicon permittivity, C_{OX} is the gate capacitance per unit area and E_g is the silicon bandgap energy. Substituting for n_i in Φ and

differentiating (11) we get,

$$\frac{\partial \phi}{\partial T} = 8.63 \times 10^{-5} \left[\ln(N_a) - 38.2 - \frac{3}{2} \left\{ 1 + \ln(T) \right\} \right] \qquad (12)$$

From (10) and (12) it is inferred that the dominant process dependent parameter for TC is the doping concentration N_a. The standard deviation of N_a in the SOI process we use is around 5%. However, the presence of N_a in the natural logarithm and square root term reduces the dependency of threshold voltage TC on N_a. This makes V_{th} a good candidate for temperature sensing with regard to the impact of process variation on TC. The temperature dependence of n_i in (10) and *ln(T)* term in (12) results in higher order terms for V_{th} TC and introduces non-linearity. The temperature dependency of V_{th} from (10) and (12) can be modeled as [58],

$$V_{th}(T) = V_{th}(T_{nom}) + (K_{t1} + \frac{K_{t1l}}{L_{eff}} + K_{t2} \times V_{bseff})(\frac{T}{T_{nom}} - 1) \qquad (13)$$

where K_{t1}, K_{t1l} and K_{t2} represent V_{th} TC dependency on the process parameter, channel length and body bias respectively. For the PDSOI process used in this work, K_{t1}, K_{t1l} and K_{t2} have the values corresponding to V_{th} TC of -2.11mV/°C, -0.103mV·µm/°C and 0.07mV/V°C, respectively, for NMOS transistors. The corresponding values for PMOS transistors are -2.2mV/°C, -0.1·mV·µm/°C and 0.067mV/V°C. It is noted in (13) that, in addition to circuit tuning, the V_{th} TC can also be tuned by channel length and body bias.

3.2 V_{TH} Extraction and CTAT Voltage Generation

The analysis in Section 3.1 shows that the threshold voltage of either PMOS or NMOS is a good candidate to implement a CTAT voltage, provided that the

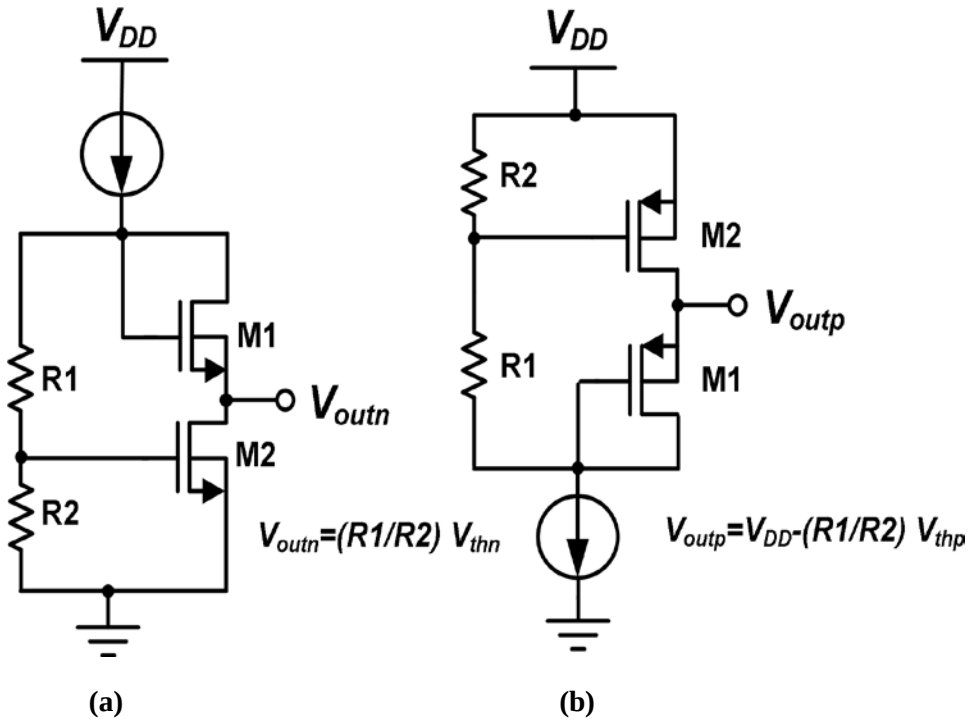


Figure 3.1: (a) NMOS and (b) PMOS threshold voltage extraction cells.

threshold voltage can be extracted. A simple V_{th} extraction topology based on square-law model is proposed in this work. The circuit structure has been used for a voltage reference in [34], based on sub-threshold operation characteristics of CMOS transistors. In this work, the topology is converted to V_{th} extraction circuit by operating the transistors in strong inversion and saturation region and applying square-law model to derive V_{th} extraction conditions. The proposed NMOS and PMOS V_{th} extraction cells are shown in Figure 3.1 (a) and (b). Based on simple voltage division principle in Figure 3.1 (a) we get,

$$(V_{outn} + V_{GS1}) \cdot \frac{R2}{R1 + R2} = V_{GS2} \tag{14}$$

From (14), V_{outn} can be written as,

$$V_{outn} = V_{GS2}\left(1 + \frac{R1}{R2}\right) - V_{GS1} \tag{15}$$

Applying square law for the strong inversion operation and neglecting channel length modulation effect, V_{GS} is typically expressed as,

$$V_{GSi} = V_{THi} + \sqrt{\frac{2I}{k_i}} \tag{16}$$

where, $k_i=\mu_n Cox(W_i/L_i)$. Substituting, for V_{GS} from (16) in (15), the expression for the output voltage for NMOS cell is given by

$$V_{outn} = \left(V_{TH2} + \sqrt{\frac{2I}{k_2}} \right)\left(1 + \frac{R1}{R2} \right) - \left(V_{TH1} + \sqrt{\frac{2I}{k_1}} \right) \tag{17}$$

Simplifying (17) we get,

$$V_{outn} = \frac{R1}{R2} V_{thn2} + V_{thn2} - V_{thn1} + \sqrt{2I}\left((1 + \frac{R1}{R2}) \frac{1}{\sqrt{k_2}} - \frac{1}{\sqrt{k_1}} \right) \tag{18}$$

If $V_{thn1} \approx V_{thn2} \approx V_{thn}$,

$$V_{outn} = \frac{R1}{R2} V_{thn} + \sqrt{2I}\left((1 + \frac{R1}{R2}) \frac{1}{\sqrt{k_2}} - \frac{1}{\sqrt{k_1}} \right) \tag{19}$$

The BOX isolation in PD-SOI CMOS process allows separate body contact for each NMOS and PMOS transistor. Taking advantage of this, the body effect can be eliminated by connecting the body to the source of the MOSFET. Hence, threshold voltage mismatch due to body bias of M1 and M2 is eliminated.

If the following condition is satisfied for (19),

$$1 + \frac{R1}{R2} = \sqrt{\frac{k2}{k1}} \tag{20}$$

the output voltage is simply the extracted V_{th} scaled by the resistor ratio, that is,

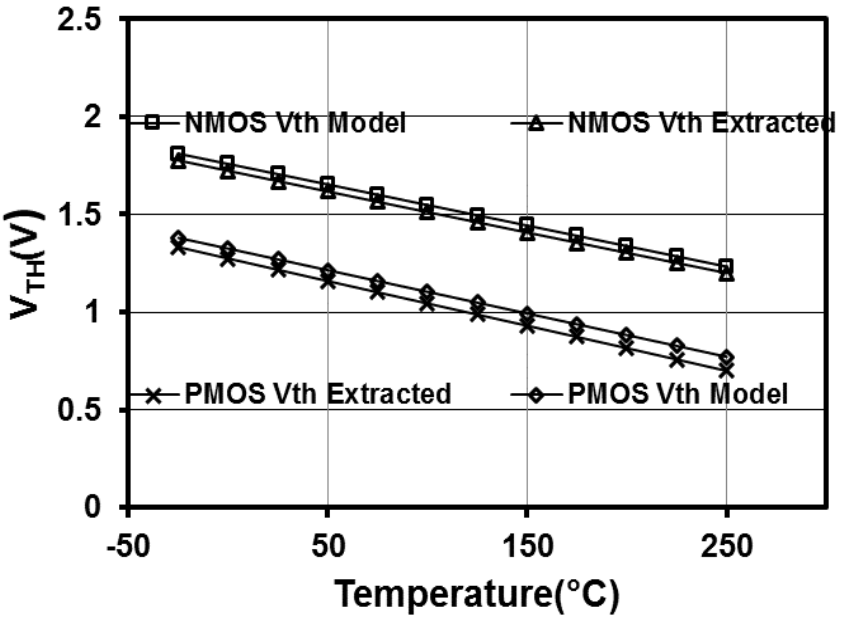


Figure 3.2: Simulated threshold voltages (from V_{th} extraction cell and device model) versus temperature.

$$V_{outn} = \frac{R1}{R2} V_{thn} \tag{21}$$

The complementary circuit gives PMOS V_{th} as shown in Figure 3.1(b). The matching condition in (20) is temperature independent since the ratio of resistors and NMOS gain factors are temperature independent. The matching condition does not contain the mobility ratio factor, as in [37] , [39], and [40]. In addition, the absolute value of V_{th} and its TC can be scaled by the resistor ratio in (21). A conventional supply independent bias circuit is used to generate the bias current for the V_{th} extraction cell. Though the bias current is PTAT, the temperature dependence has negligible effect on the output voltage due to the complete cancellation of current term in (19) if the matching condition in (20) is satisfied. The simulated extracted V_{th} for both NMOS and PMOS transistors from the proposed circuit, in comparison with the V_{th} obtained from the device models, is shown in Figure 3.2. The TC of the extracted threshold voltages closely matches those from the device models.

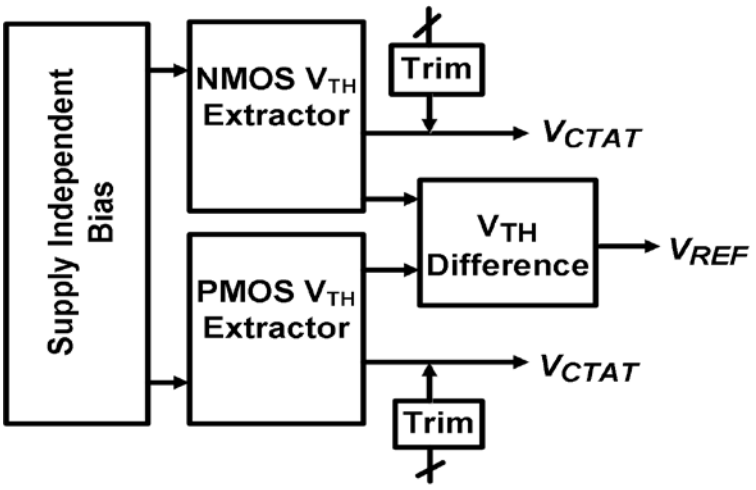


Figure 3.3: Block diagram of the proposed V_{th} based voltage reference.

Hence it shows that the proposed circuit can be used to extract V_{th} and generate a CTAT voltage for temperature sensing. The DC mismatch is due to the higher order effects such as channel-length modulation, series resistance, and mobility degradation effects which are ignored in square law model.

3.3 Voltage Reference

It is noted in Figure 3.2 that V_{th} TCs of NMOS and PMOS have similar temperature dependency. Thus the V_{th} difference between the two devices is temperature independent, which is a good candidate to realize voltage reference. Based on this concept, a voltage reference topology employing the threshold voltage extraction cells described in the last section is proposed.

Figure 3.3 shows the block diagram of the proposed V_{th} based voltage reference, where the difference of the threshold voltages from NMOS and PMOS is temperature independent. Figure 3.4 is the schematic of voltage reference. As shown by the dotted line blocks, there is an NMOS and a

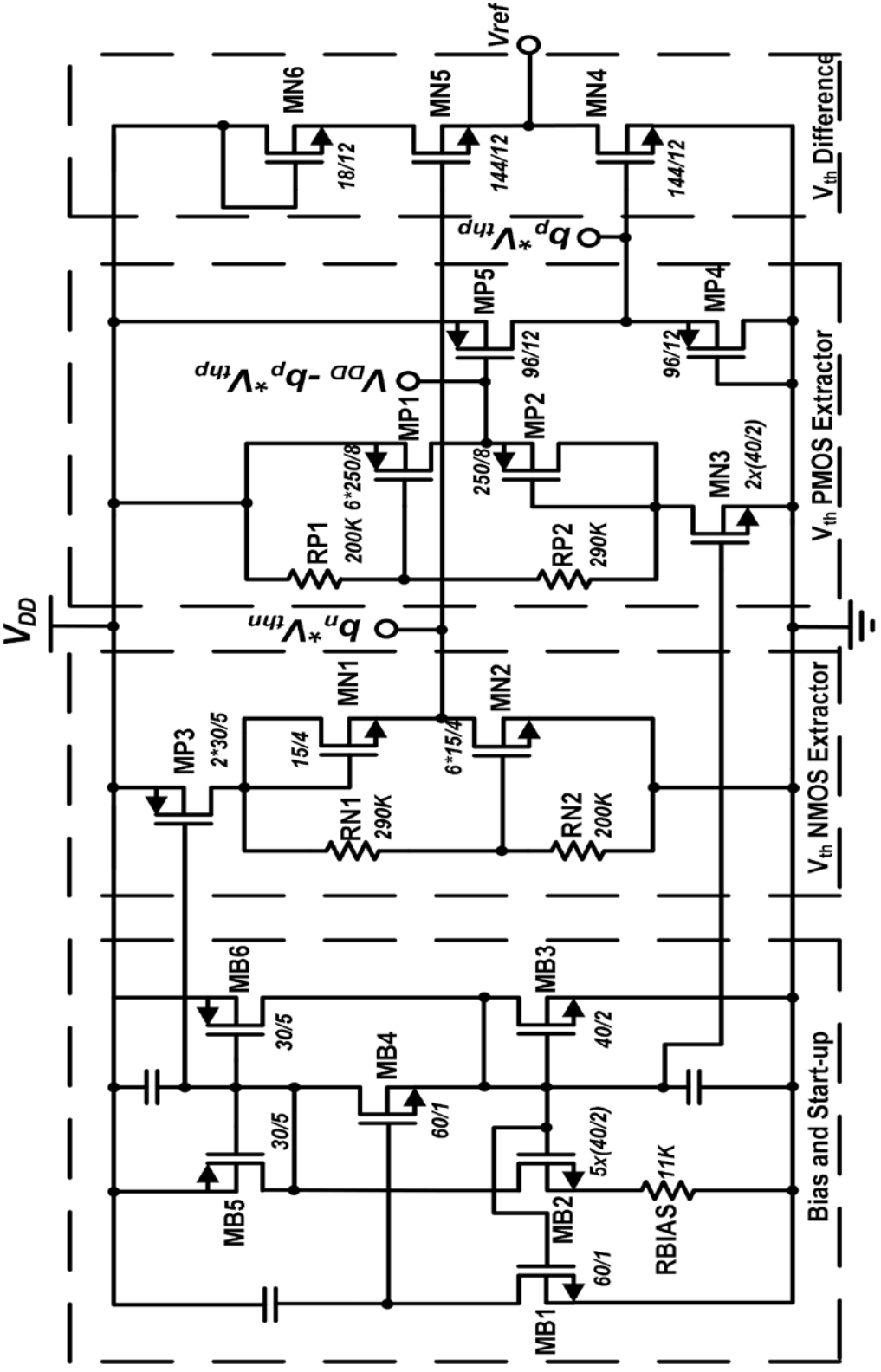


Figure 3.4: Schematic of the proposed voltage reference.

PMOS V_{th} extractor. The outputs of NMOS extractor and PMOS extractor are scaled by a factor b_n and b_p respectively, which are realized by the resistor ratio in (21). Since the PMOS extraction cell outputs $(V_{DD}- b_pV_{thp})$, MP4 and MP5 are added to obtain b_pV_{thp} with respect to GND. The difference of the extracted threshold voltages, b_nV_{thn} and b_pV_{thp} , is obtained by NMOS transistors MN4 and MN5. Since both transistors have same drain current, if channel length modulation and V_{th} mismatch is ignored, $V_{gs}(MN5) = V_{gs}(MN4) = b_pV_{thp}$. Thus, the output voltage, V_{ref} is

$$V_{ref} = V_g(MN5) - V_{gs}(MN4) = b_nV_{thn} - b_pV_{thp} \tag{22}$$

where, b_n and b_p are set by *RN1/RN2,* and *RP2/RP1,* respectively. The subtraction error of (b_nV_{thn} - b_pV_{thp}) due to channel length modulation (of MN4 and MN5) is minimized by the diode connected transistor MN6. The V_{GS} of MN6 reduces the V_{DS} difference of MN5 and MN4 and thus minimizes the channel length modulation effect.

Substituting (13) into (22) and ignoring body-bias parameter V_{bseff} (since source-body of all transistors are tied together), it yields,

$$\begin{aligned} V_{ref} &= b_nV_{thn}(T_{nom}) - b_pV_{thp}(T_{nom}) + \\ &[b_nK_{t1n} - b_pK_{t1p} + b_n\frac{K_{t1ln}}{L_{effn}} - b_p\frac{K_{t1lp}}{L_{effp}}](\frac{T}{T_{nom}} - 1) \end{aligned} \tag{23}$$

To obtain a first order compensated V_{ref}, it requires the V_{th} TCs of NMOS and PMOS to match, that is,

$$b_nK_{t1n} - b_pK_{t1p} + b_n\frac{K_{t1ln}}{L_{effn}} - b_p\frac{K_{t1lp}}{L_{effp}} = 0 \tag{24}$$

In the chosen process, the first order V_{th} TC of NMOS and PMOS (K_{t1n},K_{t1p}) differs by 0.09 mV/°C. Thus, (24) can be satisfied by selecting different

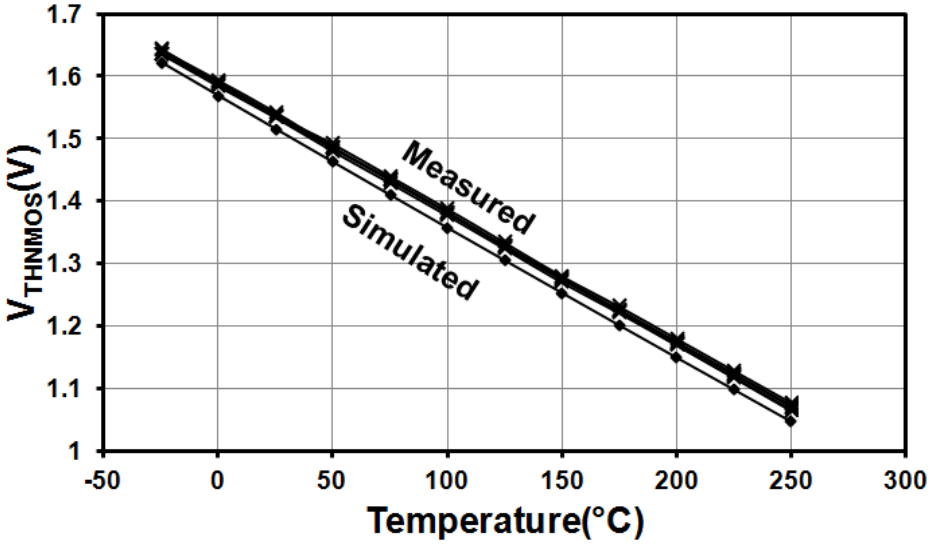


Figure 3.5: Measured and simulated extracted NMOS V_{th}.

channel lengths for PMOS and NMOS, while choosing the same value for b_n and b_p. Alternatively, if identical channel lengths are selected, b_n and b_p can be adjusted to cancel the residual TC. In this design, equal b_n and b_p are chosen, which allows an integer ratio of *k2/k1* in (20) for NMOS and PMOS V_{th} extractors and hence better matching.

The extraction and the difference are completely done in voltage domain to avoid current conversion and the associated error sources. Resistors RN1 and RP1 is made trimmable to fine tune the reference. This is done to take into account the mismatch and process variations which can alter the reference TC. As inferred from (10) and (12), there are non-linear terms for V_{th} TC which calls for higher order compensation for precision performance. This work aims to obtain the best TC by the first order compensation.

3.4 Experimental Results and Analysis

The chip is fabricated in a 1-µm PDSOI CMOS process. The maximum operating voltage is 5.5V. The buried oxide (BOX) thickness is 1µm, gate oxide thickness is 25nm and the active silicon thickness is 250nm. High

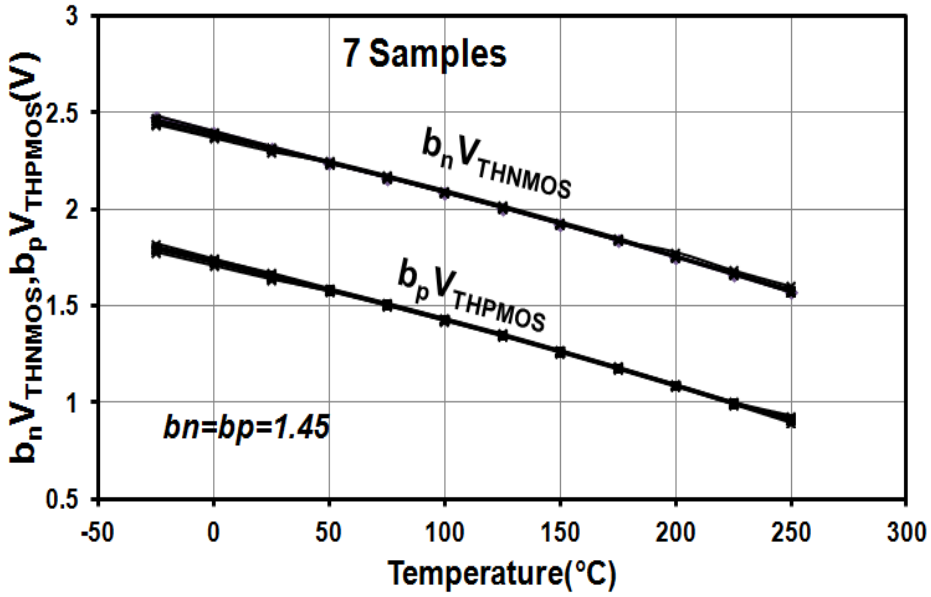


Figure 3.6: Measured extracted NMOS and PMOS V_{th} (scaled, trimmed).

temperature Rogers *RO4003C* PCB with Chip-on-Board (COB) packaging is used for the temperature measurement. Figure 3.5 shows the measured and simulated temperature dependence of the extracted NMOS voltage (V_{outn}) for 7 samples from -25 to 250°C. The measured CTAT TC after linear curve fit is -2.14mv/°C, which is close to that obtained from the simulation and is consistent over 7 samples. However, there is a DC shift which is expected with process variation. Figure 3.6 shows the measured extracted and scaled NMOS and PMOS threshold voltages (b_nV_{thn}, b_pV_{thp}). From Figure 3.6, we find that TC variation from simulation, as well as from device to device, is within 0.1 mv/°C for the seven samples.

The linearity of PMOS and NMOS CTAT outputs is estimated by the Pearson product-moment correlation coefficient (PMCC). TABLE 3-1 shows the mean and standard deviation of PMCC for the 7 samples. The non-linearity of the CTAT is due to the higher order terms in the V_{th} TC, which can be inferred from (10) and (12).

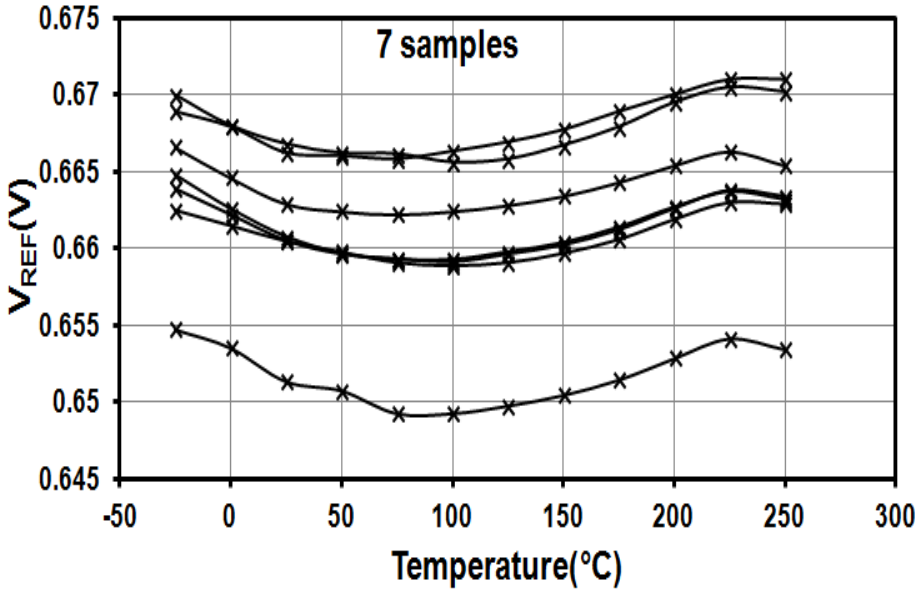


Figure 3.7: Measured output of the voltage reference.

Figure 3.7 shows the measured reference voltages for 7 samples after 2-point calibration at 25°C and 200°C. This is done by trimming resistors RN1 and RP1 by a 4-bit on-chip tunable resistor R_{Trim}. The trim range and resolution is determined from estimated process, mismatch variations and the designed V_{ref} TC. The target of the trim network is to match the V_{ref} voltages at the calibration temperatures. Note that RN1 and RP1 are trimmed at the same time using the same trimming bits, thus reducing the overhead of the trimming bits. Changing the trim bits adjusts the NMOS and PMOS TC's in opposite directions and hence tunes V_{ref} TC. Trim bits were set based on calibration of one sample and then applied to all the 7 samples. This proves the batch calibration feasibility of our circuit. The binary weighted resistor R_{Trim} is shown in Figure 3.8.

The reference voltage exhibits a mean box model TC of 27ppm and 18.7ppm for a temperature range from -25 to 250°C and 25 to 150°C respectively. The spread of the absolute value of reference for the samples is

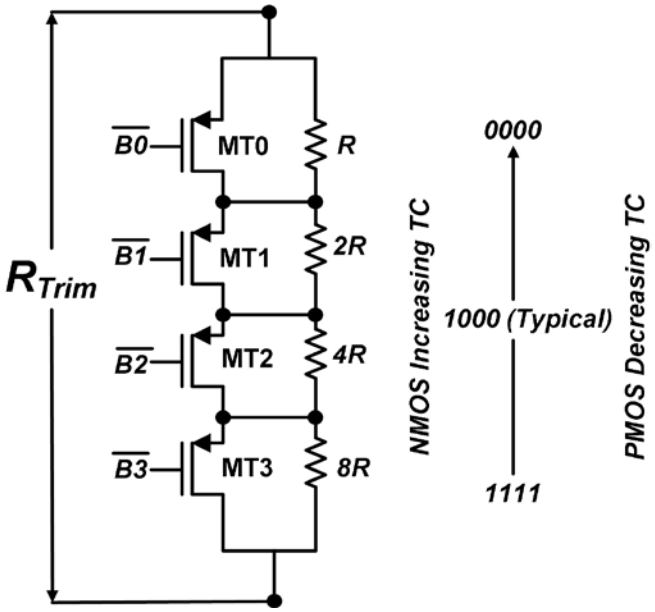


Figure 3.8: Binary-weighted trim resistor.

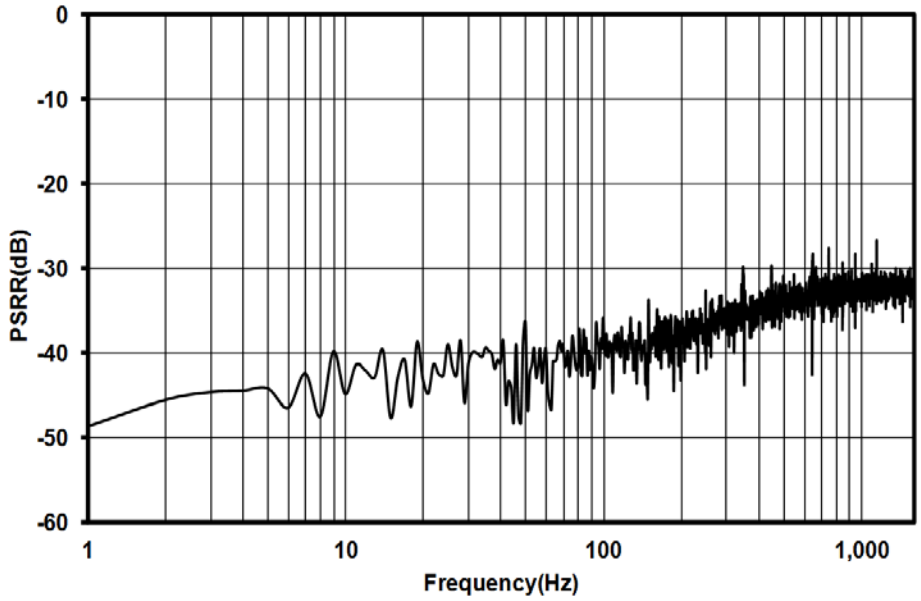


Figure 3.9: Measured PSRR of the voltage reference.

19mV which is due to die-to-die V_{th} variation. The measured PSRR of the reference is -48dB@1Hz, as shown in Figure 3.9.

The ratiometric temperature output (V_{CTAT}/V_{REF}) (Figure 2.6) for this design is given by

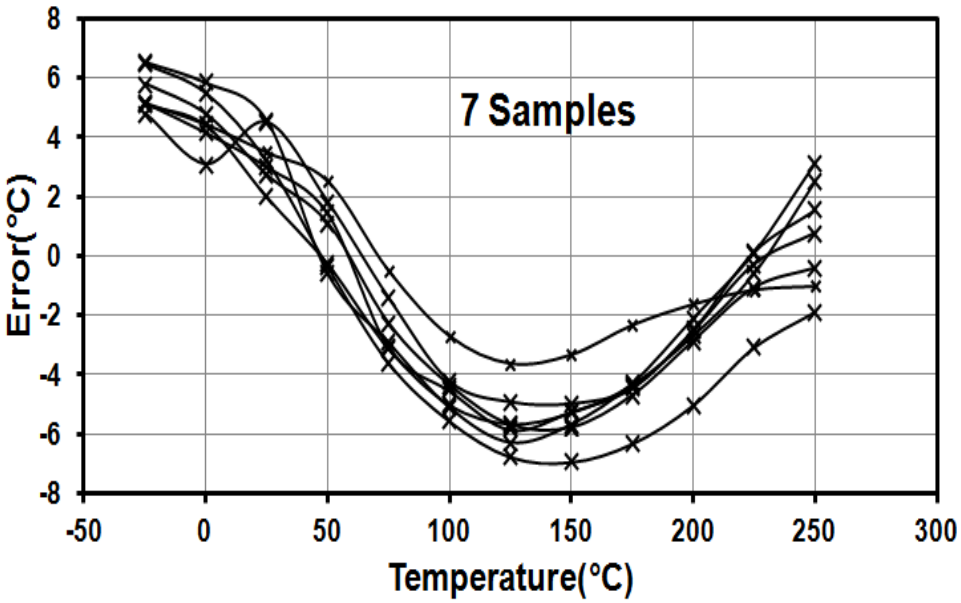


Figure 3.10: Measured temperature error of 7 samples from ratiometric output.

$$\rho = b_n V_{thn} / (k \cdot V_{ref}) \tag{25}$$

where k is the factor which sets $b_n V_{thn}$ (V_{CTAT}) equal to the reference at t=T_A, where T_A is the lowest temperature of operation i.e $\rho=1@(T=T_A)$. The temperature in degree Celsius, D_{TEMP} is obtained from ratiometric output ρ, using the following equation

$$D_{TEMP} = F(1-\rho) + T_A \tag{26}$$

where F is the full scale temperature (ρ varies from 1 to 0). Figure 3.10 shows the temperature error thus obtained. It is inferred that mean temperature error over the entire temperature range for all the samples is less than ±1.8%. It is also observed that the measurement results from 7 samples have relatively consistent curvature which facilitates batch calibration. One solution for reduction of this curvature error can be adopted from bandgap sensor designs [44] where ratiometric curvature correction is applied. Though a first-order compensated V_{ref} in Figure 3.7 looks ideal as reference for smart temperature

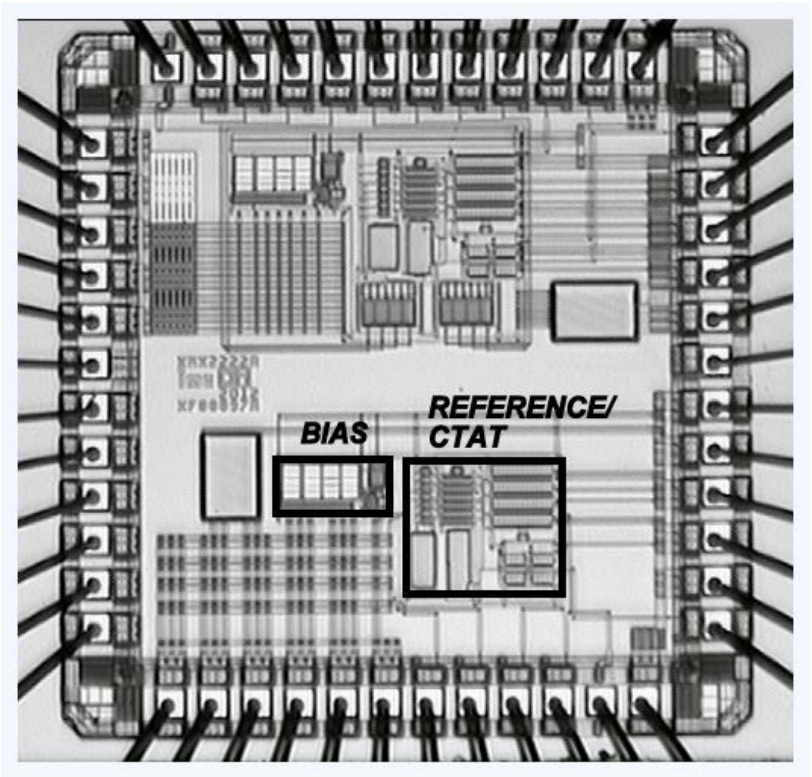


Figure 3.11: Chip microphotograph.

TABLE 3-1: STATISTICAL LINEARITY OF CTAT OUTPUTS

PMCC[a,b]	**NMOS(b_n V_{thn})**	**PMOS(b_p V_{thp})**
Mean	-0.9989	-0.9989
Standard Deviation	0.00048	0.00035

[a]*PMCC of -1 shows perfect CTAT relationship,*[b]*7 samples*

sensor, it is found that if V_{ref} is given a positive slope it results in an inverse non-linearity in ρ which cancels the second order non-linearity due to curvature of V_{TH}'s. This ratiometric curvature correction principle is able to significantly reduce the non-linearity error in bandgap based references. This can be considered in future design to further improve the performance.

Figure 3.11 shows the chip microphotograph. The effective core area

TABLE 3-2: VOLTAGE REFERENCE PERFORMANCE COMPARISON

Parameter	**This Work**		**[33]**	**[28]**	**[59]**	**[41]**	**[37]**	**[38]**
Category	High Temperature						Normal Temperature	
Technology	**1-µm PDSOI**		SIMOX	FDSOI	1-µm PDSOI	SiC	0.6-µm CMOS	0.35-µm CMOS
Temperature Range	**-25–250°C**	**25–150°C**	25-200°C	25-300°C	25-300°C	25-250°C	0-100°C	0-130°C
TC(ppm)	**27**[a]	**18.7**[a]	50	100	138	71[a]	36.9[a]	11.8
Type	**Threshold Voltage**		Threshold Voltage	Bandgap	Bandgap	Diode/ Mobility	Threshold Voltage	Threshold Voltage
Extra Masks	**No**		Yes	No	No	No	No	No
Samples	**7**		1	1	1	2	15	5
Calibration	**2**		N.A	N.A	2	N.A	0	4
Current	**118µA**		N.A	200µA	95µA	1.8mA	9.7µA	8µA
PSRR	**-48dB@1Hz**		N.A	N.A	N.A	-47.6dB @100Hz	-47dB @100Hz	-72dB @DC
PMCC (Sensor)	**-0.9989**[a]		N.A	N.A	N.A	-0.99979	N.A	N.A

[a]Mean , N.A = Data not available

is 0.23mm^2. TABLE 3-2 gives the performance comparison of voltage reference with the other works in high temperature category (operating above 200°C) as well as normal temperature. The proposed reference has achieved the lowest TC of 27ppm (mean) in the high temperature category. The temperature range is extended by 100°C compared with [33] . Compared with the state-of-the-art references based on threshold voltage in normal temperature range [37], [38], this design achieves a comparable TC in a temperature range that is more than doubled. To the best of author's knowledge, the temperature range of operation (275°C) is one of the widest ranges reported.

The temperature sensor front-end designs such as those in [25], [26], [60], [61] give the temperature information just based on the temperature sensing PTAT output and does not take into account the voltage reference effect on the temperature measurement. [25], [26] demonstrates the relative temperature error due to the difference of the PTAT outputs for various samples, whereas [60], [61] shows the PTAT output characteristics of the sensor. However, the measured temperature of our design is based on combination of both the temperature dependent CTAT signal as well as the reference and therefore gives the absolute temperature performance of the complete front-end. Though the ratiometric temperature error is on the higher side, curvature correction techniques could be considered in future to further improve the work. The primary goal was to prove the feasibility of the sensing method proposed by going with ideal scenario of linear CTAT and minimal TC for the reference. The near consistent curvature in the error for the seven samples also makes batch calibration possible.

The circuit topology leverages the separate body contact for NMOS and PMOS transistors to eliminate the effect of body bias on the accuracy. This can be justified since such an option is available in the state-of-the-art SOI technologies and conventional twin-well, triple-well processes. Techniques such as ratiometric curvature correction can further improve the performance. The voltage reference designed in this temperature sensor front-end can be also be used as a general purpose voltage reference for other applications such as power management circuits, biasing circuits etc.

CHAPTER 4

TIME-DOMAIN SMART TEMPERATURE SENSOR

This Chapter presents a time-domain bandgap temperature sensor operating over a wide temperature range from 25°C to 225°C. Compared to threshold voltage based front-end this design needs only one-point calibration to mitigate the process variation. The proposed smart temperature sensor eliminates the explicit bandgap reference through a mapping function and only requires the ratio of two V_{BE} voltages to obtain ratiometric temperature measurements. Two temperature sensor chips are implemented. The second chip is an improved version of the first chip. The rest of the chapter describes the details of the design.

4.1 Proposed Technique for Ratiometric Temperature Measurement

As discussed in Section 2.2 the front-end of a smart temperature sensor consists of a PTAT or CTAT voltage and a voltage reference. The digitization of the temperature is done by an ADC, which generates the ratiometric output ((V_{CTAT} or V_{PTAT})/V_{REF}). Figure 4.1 shows the CTAT and PTAT voltages specific to a bandgap temperature sensor. V_{BE1} and V_{BE2} are base emitter voltages of two BJT's biased at different current densities and has a CTAT characteristic. The difference between V_{BE1} and V_{BE2}, ΔV_{BE} has a positive TC which is scaled by a factor α to match the negative TC of V_{BE}.

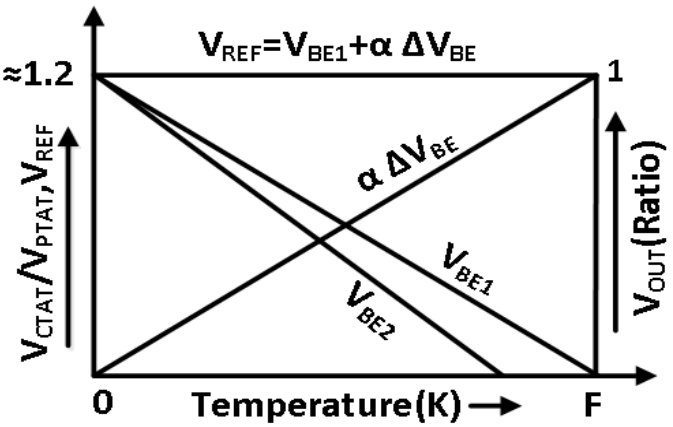


Figure 4.1: Bandgap CTAT/PTAT voltages and reference.

The ratiometric output of a bandgap sensor is expressed by the following equation

$$V_{OUT} = \frac{V_{CTAT}}{V_{REF}} or \frac{V_{PTAT}}{V_{REF}} = \frac{V_{BE}}{V_{REF}} or \frac{\alpha \Delta V_{BE}}{V_{REF}} \tag{22}$$

The expression for CTAT ratiometric output in (22) can be written in the simplified form below

$$V_{OUT} = \frac{V_{BE1}}{V_{REF}} = \frac{V_{BE1}}{V_{BE1} + \alpha \Delta V_{BE}} = \frac{1}{1 + \alpha(1 - \frac{V_{BE2}}{V_{BE1}})} \tag{23}$$

We can observe from (23) that the ratiometric CTAT output is just a function of V_{BE2}/V_{BE1} and α. Similarly, PTAT output is also a function of V_{BE2}/V_{BE1} and α, but with a slightly more complex expression. Thus, the ratiometric output can be expressed in a general form as,

$$V_{OUT} = R(\frac{V_{BE2}}{V_{BE1}}, \alpha) \tag{24}$$

where R is a function which represent (23). V_{OUT} can be obtained if we can synthesize the V_{BE2}/V_{BE1} ratio and use the function R for mapping which can be implemented at the digital back-end. CTAT output is used in this work to demonstrate the technique due to its simpler mapping function as compared

with PTAT. The parameter α is the scaling factor to match the TC's of the PTAT and CTAT voltages. This factor needs to be precisely controlled to obtain the desired output. α is usually a ratio of capacitors or resistors in majority of sensor designs and is precisely controlled by techniques such as trimming in case of resistors or dynamic element matching (DEM) for capacitors. Due to implementation of the mapping function in digital domain, α can be moved to the digital back-end as well. The major process variation in a bandgap sensor is the variation of V_{BE}. However, V_{BE} has just one degree of freedom about the 0 K point [42] and hence it is just a TC change. This can be mitigated by one-point calibration by either bias current trimming or adding a compensating PTAT voltage. Alternatively, we can trim α to compensate for the TC change of V_{BE}. A technique for digital trimming of α implemented at the back-end is given in Section 4.3.2.

The V_{BE} ratio is obtained by a time-to-digital conversion technique. This results in a simple low-power architecture for the smart temperature sensor. The acquired ratio is converted to ratiometric output by the mapping function R implemented in the digital processing block. The ratiometric output is converted to reading in degree Celsius by linear scaling as given by the following equation

$$Temp(^{\circ}C) = F(1 - V_{OUT}) - B \quad \text{.....(25)}$$

where F is the full scale temperature corresponding to V_{BE1} of 0V and B=-273° K. Two versions of the proposed ratiometric temperature sensor are presented in this Chapter.

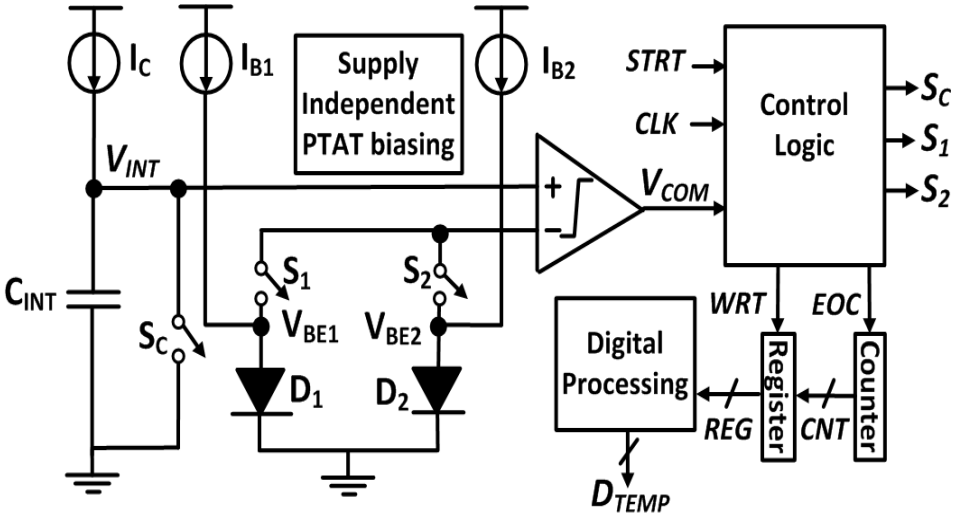


Figure 4.2: Sensor architecture version 1.

4.2 Temperature Sensor Version 1

This section describes design of version 1 of the proposed temperature sensor. This design was the proof-of-concept for the proposed technique which was later further improved by version 2.

4.2.1 Architecture and operation

The architecture of version 1 is shown in Figure 4.2. D_1, D_2 are diffusion-well diodes available in the process. V_{BE1} and V_{BE2} are obtained by biasing D_1 and D_2 at different current densities. The difference of V_{BE1} and V_{BE2} is given by the equation

$$\Delta V_{BE} = V_{BE1} - V_{BE2} = \frac{kT}{q} \ln\left(\frac{I_{B1} \cdot A_2}{I_{B2} \cdot A_1}\right) \tag{26}$$

where A_1 and A_2 are the area of D_1 and D_2, respectively. In this design different areas and bias currents are chosen to maximize ΔV_{BE} and therefore the dynamic range of the V_{BE} ratio.

The circuit operation is as follows. The integration capacitor C_{INT} is

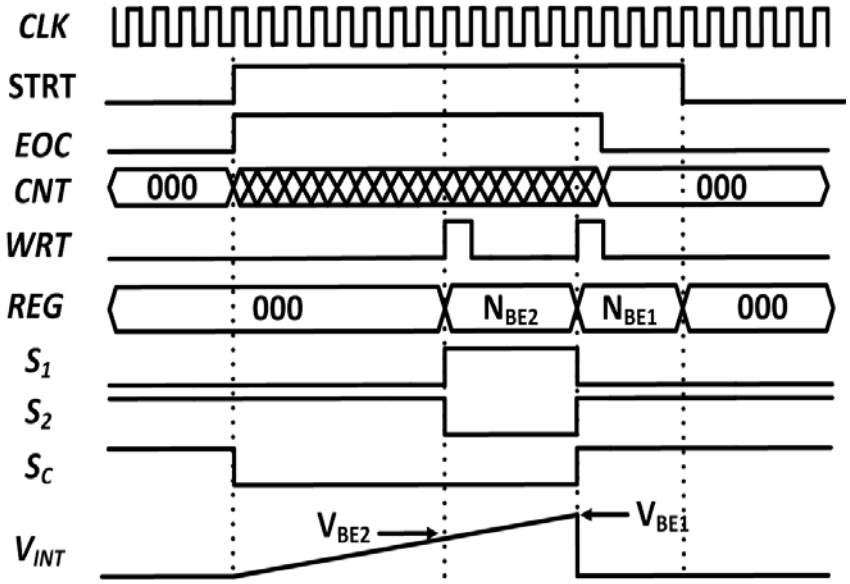


Figure 4.3: Timing diagram for version 1.

discharged by switch S_C in the reset state (*STRT*=0). S_2 is closed and S_1 open in this state. When *STRT* signal goes high, switch S_C is open, the 10-bit counter starts counting and C_{INT} starts charging to V_{BE2}. When the integration voltage V_{INT} equals V_{BE2} the comparator goes low, which triggers the control logic to write the count N_{BE2} to the register *REG* through *WRT* signal. The comparator is reset, S_2 is open, S_1 is closed, and the counter continues the count till V_{INT} equals $V_{BE1.}$ At this point, comparator goes low and the new count N_{BE1} is written to the register through the *WRT* signal. The timing diagram for a single readout operation is given in Figure 4.3. Thus, V_{BE2} and V_{BE1} are converted to counts N_{BE2} and N_{BE1}, respectively. The V_{BE} ratio is the same as the count ratio as given by the following equation

$$\frac{V_{BE2}}{V_{BE1}} = \frac{\frac{I_C}{C_{INT}}(N_{BE2} \cdot T_{CLK})}{\frac{I_C}{C_{INT}}(N_{BE1} \cdot T_{CLK})} = \frac{N_{BE2}}{N_{BE1}} \tag{27}$$

Thus from (24), we get

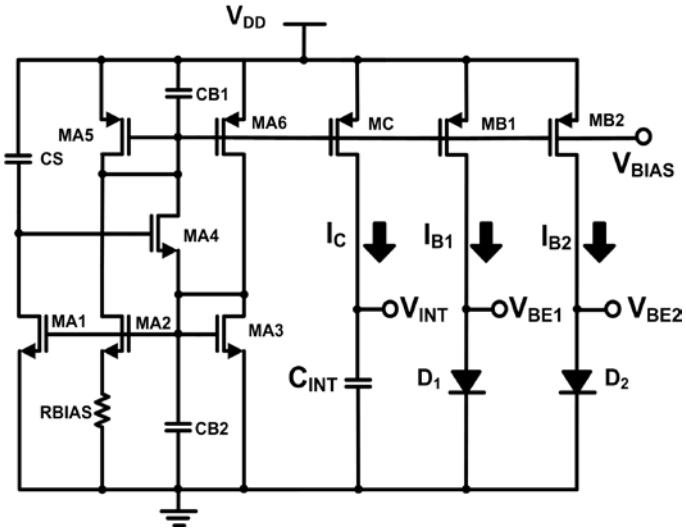


Figure 4.4: Bias circuit schematic of version 1.

$$V_{OUT} = R(\frac{N_{BE2}}{N_{BE1}}, \alpha) \tag{28}$$

i.e, the ratiometric output V_{OUT} effectively becomes the same function R of the count ratio. The design parameters are chosen from the conversion time and expected accuracy. The total conversion time is designed to be 100ms which is typical for a temperature sensor. The digital processing/calibration can be done in less than 1ms. Hence, N_{BE1}*T_{CLK} is 99ms. The non-linearity of the diode results in a total curvature error of around 2.5°C p-p. Resolution is selected to be 7-12 times divided by the accuracy which corresponds to .2-.4°C. 10-bit is found to be the optimal number of bits for replication of count ratio which is equivalent to the voltage ratio within the targeted resolution. To achieve the conversion time requirement, F_{CLK} $(1/T_{CLK})$ of 10.3 KHz is chosen.

4.2.2 Circuit Design

The charging current I_C, the bias currents for the diodes, I_{B1} and I_{B2} and the bias for the comparator is derived from a supply independent constant-g_m bias circuit [62]. The circuit schematic of the bias circuit is shown in Figure 4.4.

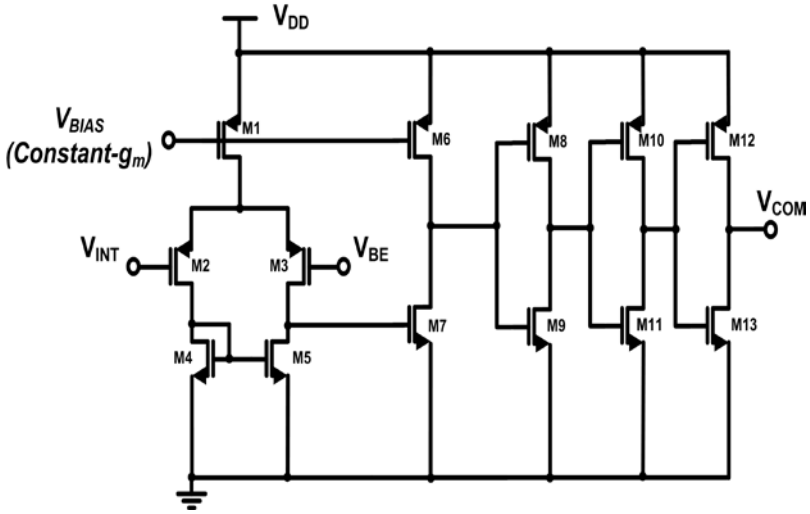


Figure 4.5: Comparator schematic version 1.

The self-biasing nature of the circuit makes the bias supply independent. The transistors MA2, MA3, MA5, MA6 and resistor RBIAS constitute the core of the constant-g_m bias circuit. To avoid the undesirable operation point of zero current, start-up circuit [63] consisting of transistors MA1, MA4 and capacitor CS is added. The start-up circuit does not consume any static current. CB1 and CB2 are the bypass capacitors.

To generate the V_{BE} difference and hence the ratio depends on the ratio of current densities. The current density ratio could be achieved by either current scaling or area scaling or both. By going for just current scaling, we can have a single diode and current sources which can be switched. This method will result will result in high power consumption but less area for the diodes. By going for just area scaling, a single current source can be switched between the two diodes. However, the area ratio of the diode would be large. Even if area is not a concern for the design it is not advisable to adopt a large area ratio due to matching deterioration due to spatial effects. Hence, in this design both area and current scaling was adopted due to the drawbacks of other two approaches

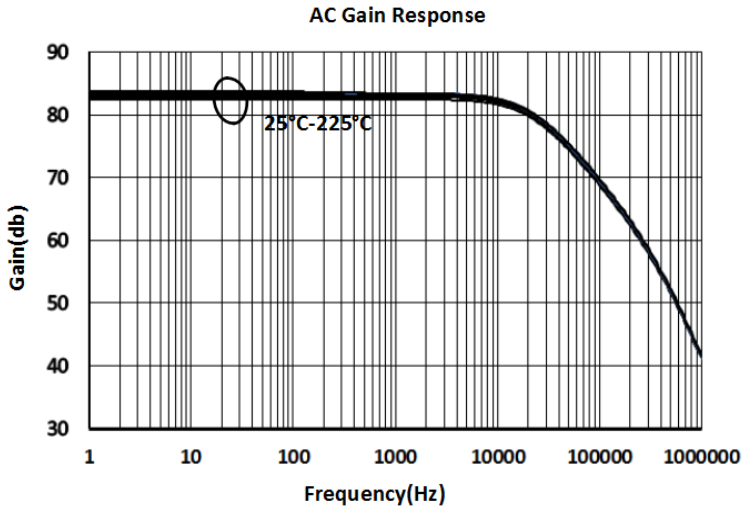


Figure 4.6: Gain plot for various temperatures.

mentioned above. The selected design values are $I_{B1} = 3I_{B2}$ and $A_2=14A_1$ which results in a V_{BE} ratio of 0.875 – 0.7 for a temperature range of 25 – 225°C. Current ratio of 1:3 will not affect the power budget and an area ratio of 1:14 is still compact and makes common centroid layout possible.

The minimum bias current is selected as 1µA because of diode model inaccuracies at lower currents, especially at higher temperatures. This bias current is also sufficient to make the -1 term non-ideality in the current equation of diode insignificant. Due to the low speed requirement (10 kHz clock), the comparator is a conventional two-stage open-loop comparator with a gain of 80dB, corresponding to a resolution of 0.3mV. The schematic is shown in Figure 4.5. PMOS differential input pair is selected to meet the low common mode voltage requirement (V_{BE1} and V_{BE2}).

For majority of HT designs, ZTC biasing is used to achieve stable biasing point over the operating temperature range. However, ZTC technique has some limitations. ZTC biasing point corresponds to strong inversion region of operation in PDSOI technology which reduces the intrinsic gain. In addition, ZTC biasing also affects the parameters such as gain, bandwidth etc. due to

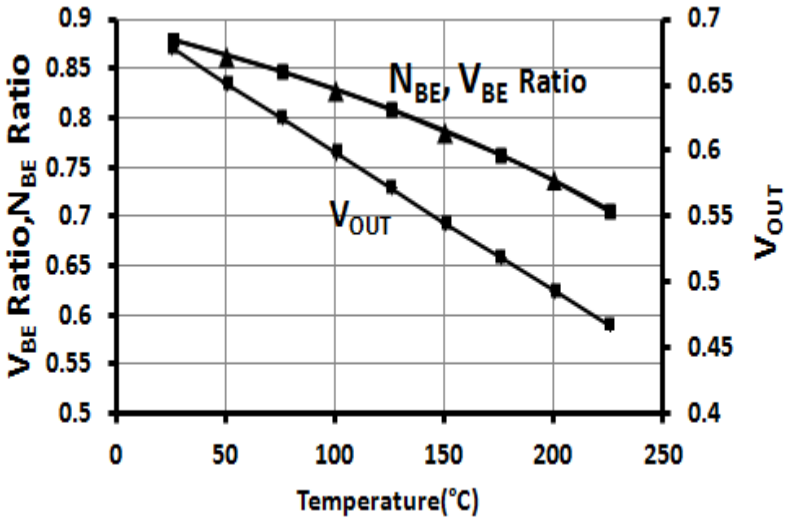


Figure 4.7: Simulated voltage, count ratio comparison and mapped ratiometric output V_{OUT}.

decrease of g_m with temperature. Therefore, in this work, constant-g_m biasing technique is applied to stabilize the gain of the open-loop comparator over the entire temperature range of operation by stabilization of the transconductance g_m. Applying this bias technique, the transconductances are matched proportionally to conductance of the resistor RBIAS. By selecting RBIAS as the sum of two resistors with opposite TCs and ratioing appropriately, the temperature dependency of g_m due to RBIAS is minimized.

Figure 4.6 shows the simulated AC gain response for various temperatures from 25-225°C. The gain is stabilized within 1.5dB over the desired temperature range of operation. However, the bias point shifts with temperature need to be taken care for robust operation over entire temperature range. This shift can be estimated from the below calculations.

g_m can be expressed by the following equation

$$g_m = \mu C_{OX}(\frac{W}{L})V_{DSAT} \tag{29}$$

Figure 4.8: Measurement set-up.

As observed from the equation, mobility is the temperature dependent factor here. Hence, for g_m to be constant, V_{DSAT} has to compensate the change of mobility. Mobility has an exponential temperature characteristic which decreases with temperature. The rate of change of mobility of NMOS transistors in higher than that of PMOS. There is a 45.6%, 57% decrease in mobility for PMOS and NMOS transistors respectively for a temperature range from 25-225°C in the process used for this design. This results in approximately 45.6%, 57% increase in V_{DSAT} for PMOS and NMOS transistors. Therefore, such variation of V_{DSAT} could disturb the saturation region of operation of the transistor which ensures the operation of the circuit. Therefore, this worst case scenario of bias point of each transistor needs to be taken into consideration at higher temperatures.

One of the main advantages of the proposed circuit is that the temperature dependency as well as the precision of I_C and C_{INT} is not important in this design. This is due to the fact that as long as I_C and C_{INT} remains the same for both counts, ratio is unaffected by the absolute magnitude of the current which

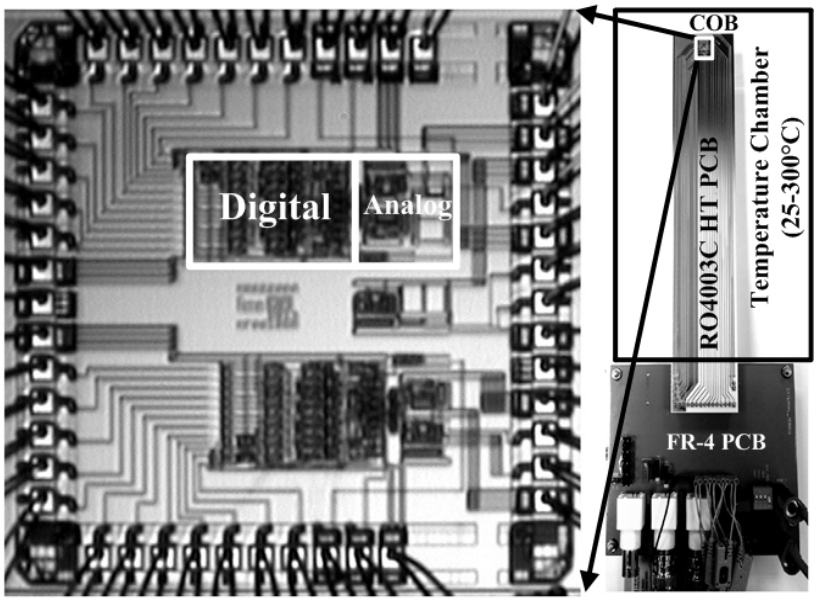


Figure 4.9: Chip microphotograph of version 1.

can be observed from (27). Thus, the temperature specification of the bias circuit is greatly relaxed. This is proved by the fact that, I_C is derived from the constant-g_m bias circuit, which has a PTAT current characteristic.

Figure 4.7 shows the simulated V_{BE} ratio (V_{BE2}/V_{BE1}), count ratio (N_{BE2}/N_{BE1}), and ratiometric output voltage (V_{OUT}). Thus, the circuit effectively converts the temperature signal into time domain and is subsequently digitized by the digital processing block. In this version of design, the digital processing is done offline.

4.2.3 Measurement Results and Discussion

The chip is fabricated in a 1-µm commercial PDSOI CMOS process. The measurement set-up and chip microphotograph are shown in Figure 4.8 and Figure 4.9. The active area of the temperature sensor is 0.45mm^2. The die is attached to a Rogers RO4003C HT PCB (T_g >280°C) with a conductive adhesive (Chip-on-board packaging). The bond pad on which the die is attached, is connected to ground plane to reduce the thermal resistance.

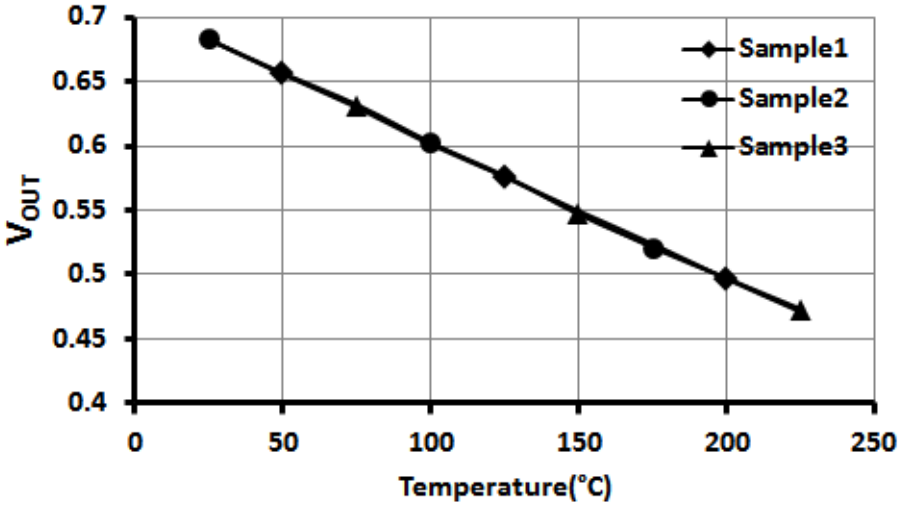


Figure 4.10: Measured Ratiometric output for 3 samples.

There is no solder mask on the HT PCB and hence the copper is exposed. To further ensure thermal stabilization, after the temperature has been ramped up, the measurements were taken only after 20-25 minutes. During measurement, the outputs for at least 100 cycles were observed to ensure that the temperature reading is consistent which ensures that the reading corresponds to the stabilized temperature and not to transients induced by the equipment and environment.

Figure 4.10 shows the ratiometric output V_{OUT} from 3 samples after calibration at 25°C and the samples match very well. Figure 4.11 shows the measured temperature error in degree Celsius after applying linear scaling (25) for the 3 samples. The temperature error is within ±2°C for the three samples.

One of the sources of temperature error for this design is the error due to comparator offset. The effect of comparator offset on V_{BE} ratio is given by the following equation,

$$\frac{V_{BE2}(Actual)}{V_{BE1}(Actual)} = \frac{V_{BE2}(Ideal) \pm V_{OFFSET}}{V_{BE1}(Ideal) \pm V_{OFFSET}} \tag{30}$$

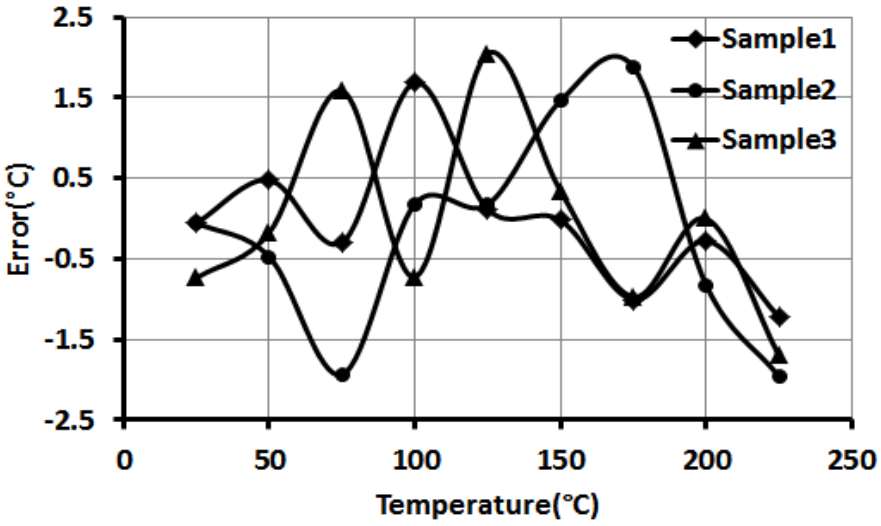


Figure 4.11: Measured Temperature error of 3 samples.

It can also be expressed in terms of the counts in time-domain. The corresponding counts N_{OFFSET} due to V_{OFFSET} is

$$N_{BE} = \frac{V_{BE}}{(I_C / C_{INT}) \cdot T_{CLK}} \Rightarrow N_{OFFSET} = \frac{V_{OFFSET}}{(I_C / C_{INT}) \cdot T_{CLK}} \tag{31}$$

Thus, we get

$$\frac{N_{BE2}(Actual)}{N_{BE1}(Actual)} = \frac{N_{BE2}(Ideal) \pm N_{OFFSET}}{N_{BE1}(Ideal) \pm N_{OFFSET}} \tag{32}$$

Since V_{OFFSET} appears in both numerator and denominator of (30), the error introduced by the comparator offset is effectively reduced when the ratio is taken. The worst-case error occurs at the highest temperature (225°C) where V_{BE2} and V_{BE1} are at minimum, and thus for the same comparator offset, the error introduced is the largest at 225°C, as indicated in (30) or (32). After applying common-centroid and other matching techniques in the layout, assuming a maximum pessimistic offset of 5mV, the maximum error due to offset is 2°C@225°C, as shown in Figure 4.12. At the low end of the

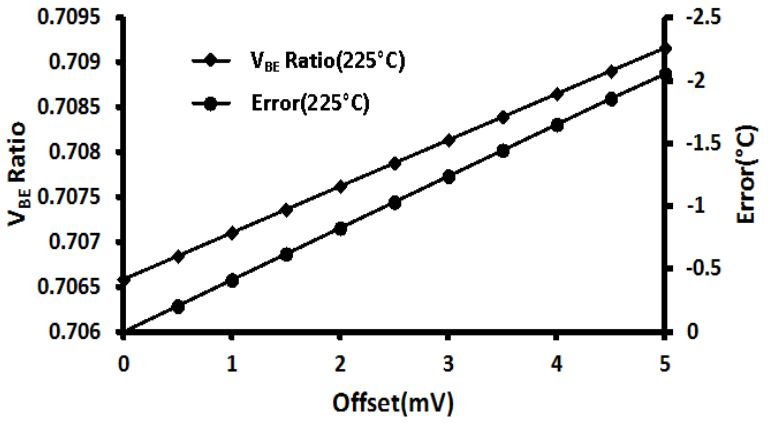


Figure 4.12: Simulated V_{BE} ratio and temperature error (at worst case temperature of 225°C) vs. comparator offset.

temperature range near room temperature, the error is much less, around 1.2°C.

In addition to the above error analysis due to a fixed offset voltage, it is also known that offset is a random phenomenon and hence statistical variation applies for the samples. In addition, offset also has a temperature dependency which makes the effect of offset worse. Therefore, it is necessary to eliminate this error for improvement of the architecture. In addition, techniques to further optimize the design could also be explored.

4.3 Temperature Sensor Version 2

To further improve the performance of version 1, another version of the design is presented. The version 2 incorporates offset cancellation and further optimizes the power and area and improves the accuracy. In addition, the digital processing and calibration is implemented on an FPGA and interfaced v the sensor chip.

4.3.1 Circuit Design

The architecture of version 2 design is as shown in Figure 4.13.

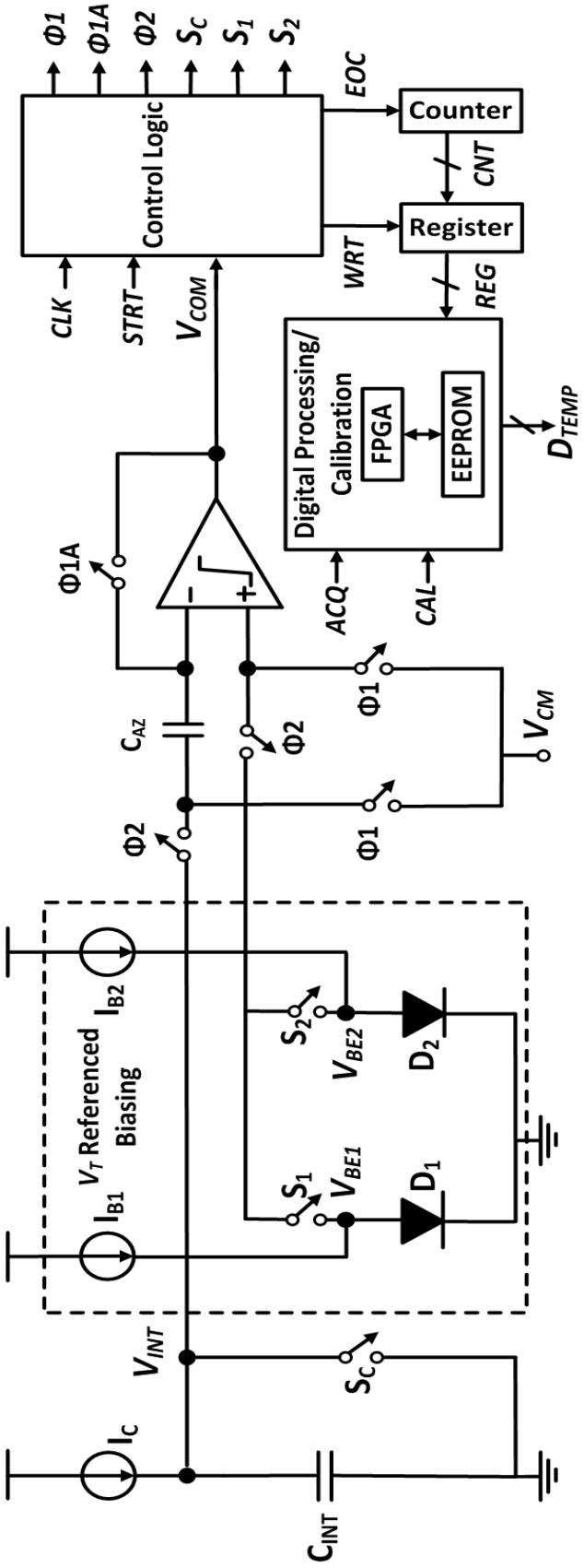


Figure 4.13: Sensor architecture version 2.

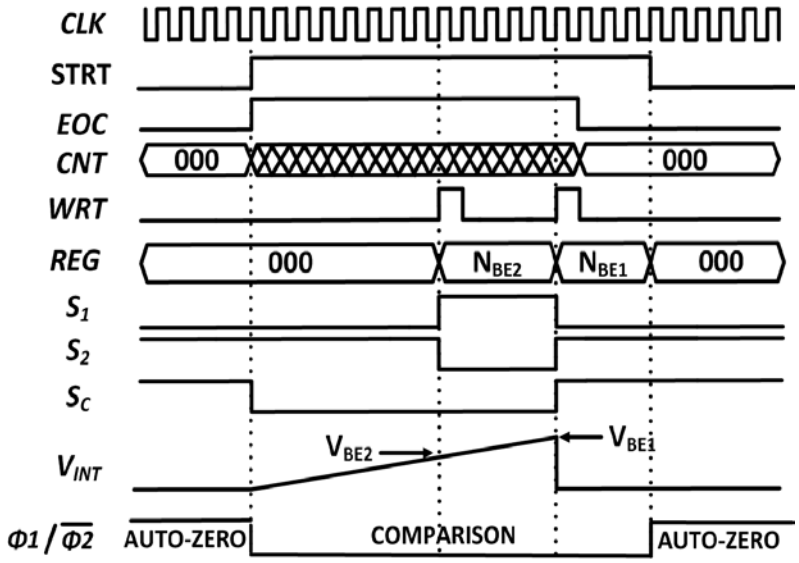


Figure 4.14: Timing diagram for version 2.

The operating principle is similar to version 1. Though the effect of offset is effectively reduced due to the offset count in both numerator and denominator, but not completely cancelled, the error still exists as shown in Section 4.2.3.

To completely eliminate the error due to offset, auto-zero technique is applied for comparator offset cancellation. Thus, non-idealities due to offset voltage in version 1 which is also temperature dependent are eliminated by auto-zero offset cancellation. Phase *Φ1* is the auto-zero phase where offset is sampled onto to the auto-zero capacitor C_{AZ}, and *Φ2* is the comparison phase. *Φ1* and *Φ2* are non-overlapping clocks. *Φ1A* is an advanced version of *Φ1* due to charge injection considerations [64]. Charge injection due to the unity-gain switch is the charge injection which needs to be taken into account. The effect is minimized by choosing a transmission gate switch and sizing the switches for optimal cancellation in the desired operating voltage and temperature range. The timing diagram including the offset cancellation phase is shown in Figure 4.14.

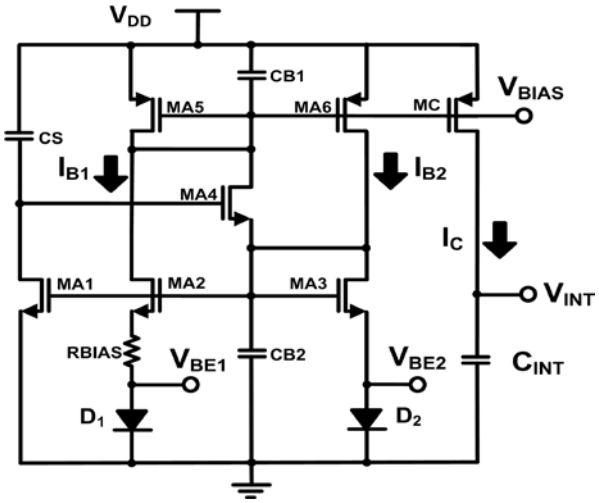


Figure 4.15: Bias Circuit schematic for version 2.

In this version, the bias circuit is modified. Bias currents I_{B1}, I_{B2} and diodes D_1, D_2 are part of conventional thermal voltage (V_T) referenced self-biasing circuit as shown in Figure 4.15. The charging current I_C and the bias for the comparator are also derived from the same circuit. The self-bias current generated is mirrored by *MC* to obtain the charging current I_C. V_T referenced biasing approach results in further optimizing power and area of the architecture by virtue of less branches and embedded diodes in the bias circuitry.

Due to the low speed requirement (10 kHz clock), a two-stage, auto-zeroed open-loop comparator with gain of 80dB as shown in Figure 4.16 is adopted in this design. Compared to version 1 comparator, miller compensation capacitor C_C is required due to the unity-gain feedback configuration in auto-zero phase. However, during the comparison phase when the comparator is in open-loop mode, C_C is disconnected which optimizes the speed of the comparator for this design. Constant-g_m bias technique is used in version 1 for comparator gain stabilization over wide temperature range. The reason for this is the PTAT nature of the bias current, which stabilizes g_m. V_T reference bias with the

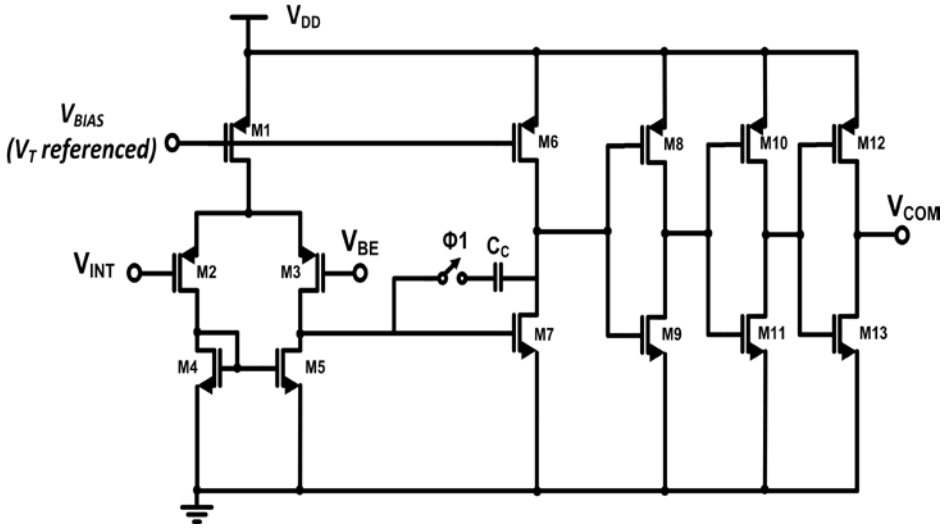


Figure 4.16: Open-loop comparator schematic.

embedded diodes also has a PTAT bias current, hence achieves the same effect. Push-pull inverters are cascaded to improve the driving capability with minimum propagation delay.

4.3.2 Digital Processing and Calibration

The counts are converted to the ratiometric output V_{OUT} by the digital processing block which implements the mapping function R (23). Digital processing block is implemented on an FPGA for flexibility. The processing block has two modes depending on control signal (CAL/ACQ) - calibration and acquisition mode. In the calibration mode, a one-time calibration is done at room temperature to compute the calibrated α value, $\alpha(CAL)$, which is then written to an EEPROM through an I^2C interface. $\alpha(CAL)$ is computed by the following equation which is derived from (23)

$$\alpha(CAL) = \frac{1 - V_{OUT}(IDEAL, 25^{O}C)}{V_{OUT}(IDEAL, 25^{O}C)\left\{1 - \frac{N_{BE2}(25^{O}C)}{N_{BE1}(25^{O}C)}\right\}} \tag{33}$$

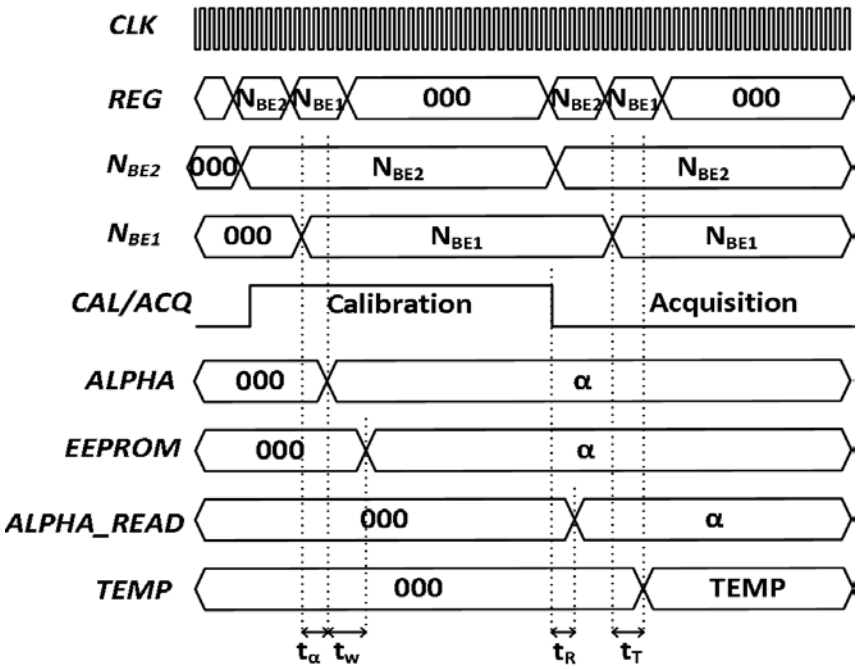


Figure 4.17: Calibration and digital processing timing diagram.

where, $V_{OUT}(IDEAL,25°C)$ is the ideal ratiometric output corresponding to a temperature of 25°C. N_{BE2} and N_{BE1} are the measured counts at 25°C.The difference between ideal α (obtained from simulations) and α *(CAL)* depends on the V_{BE} process variation as well as circuit process variations which are PTAT in nature. The precision of parameter α is conventionally achieved by techniques such as trimming, DEM etc. in the analog front-end. However, in this design, α trimming as well as sensor calibration is achieved at the digital side and hence the precision required of the analog front-end is greatly relaxed. This is one of the major advantages of this technique.

In the acquisition mode, the two counts are stored in registers, α *(CAL)* is read from the EEPROM and computation of the ratiometric output V_{OUT} is done using function *R*. The ratiometric output is converted to reading in degree Celsius by simple linear scaling as shown in (25). All the computations in the digital processing block are in floating point. The calibration and digital

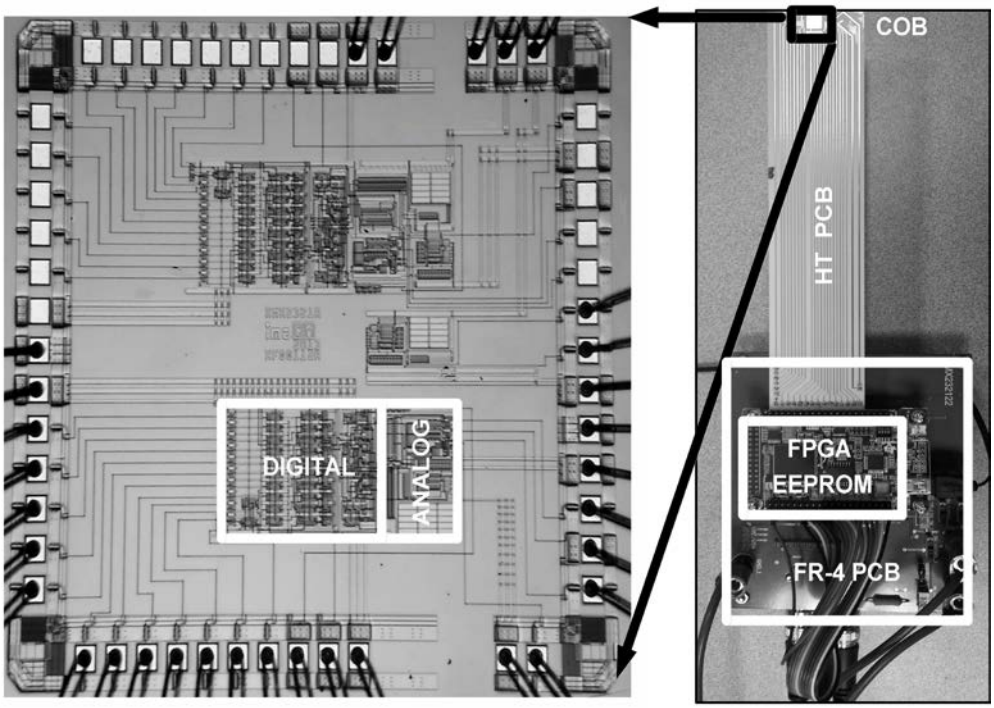


Figure 4.18: Die-photo and high temperature measurement set-up.

processing steps is shown by the timing diagram given in Figure 4.17. t_R, t_W are the time for α read and write to EEPROM through I^2C interface. t_α, t_T are the time for α and temperature computation respectively. The total time taken for read, write and computation for calibration and acquisition is less than 1ms.

4.3.3 Experimental Results and Analysis

The chip is fabricated in a 1µm commercial PDSOI CMOS process. Vertical isolation of the devices is done by BOX layer and lateral isolation by trench isolation which results in much lesser PN junction area. Therefore, leakage current is reduced by 2-3 orders of magnitude when compared to bulk CMOS. This enables robust high temperature operation for the PDSOI process. In addition, tungsten metallization is used, whose 3-4 times higher sheet resistance need to be considered in the layout design.

The chip microphotograph and measurement set-up is shown in Figure 4.18. The active area of the temperature sensor is $0.41mm^2$. High Temperature

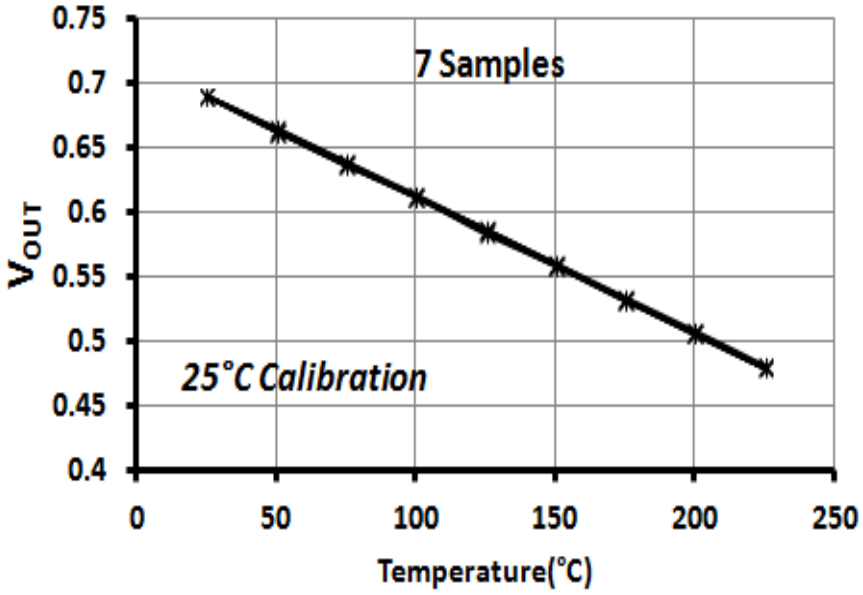


Figure 4.19: Measured ratiometric output of 7 samples.

Rogers *RO4003C* PCB with COB (Chip-on-board) packaging is used for measurement. The bond pad on which the die is attached is shorted to ground plane for faster thermal stabilization. Altera Cyclone IV FPGA and Microchip EEPROM are used for digital processing and calibration implementation.

Figure 4.19 shows the ratiometric output V_{OUT} from 7 samples after calibration at 25°C and the samples match very well. Figure 4.20 shows the measured temperature error in degree Celsius after applying linear scaling (25) for the 7 samples. The temperature error is within +1.6°C to -1.5°C for all the 7 samples. The version 1 of this design has an inaccuracy of ±2°C for just three samples. The improvement is due to the elimination of errors due to comparator offset by auto-zeroing. The device to device spread of the error is also eliminated by offset cancellation.

The temperature error is found to be non-linear for the samples. This can be attributed to the V_{BE} errors caused by spread in silicon diodes due to

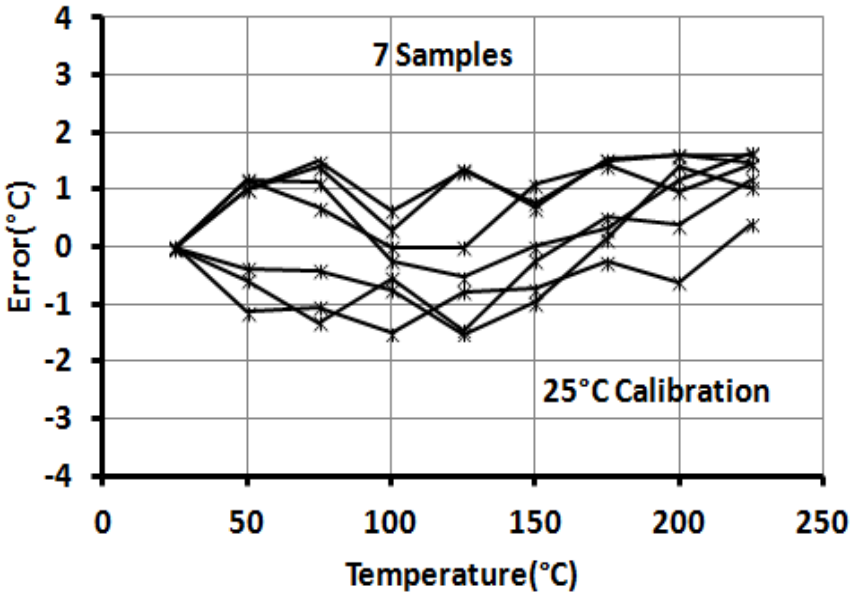


Figure 4.20: Measured temperature error of 7 samples.

recombination current, errors due to bias resistor spread, mismatch etc. Use of robust substrate PNP transistors could reduce the error spread. However, substrate PNP is not realizable in SOI process due to BOX isolation. The sensor draws a current of only 20µA at and operates from 4.5 V to 5 V supply voltage, 20% reduction from 25µA in the version 1 chip. The error due to self-heating effect is negligible due to the low power consumption. The improvement in area and power is made by the optimization of bias circuit in version 2.

A time-domain bandgap smart temperature sensor for oil-well instrumentation application is presented in this chapter. One-point calibration at room temperature achieves a worst case inaccuracy of 1.6°C for seven samples. The fabricated temperature sensor consumes only 20µA from a 4.5-V supply and occupies an active area of 0.41mm^2. The errors due to offset in version 1 of the architecture are eliminated by auto-zero technique and

TABLE 4-1: TEMPERATURE SENSOR PERFORMANCE COMPARISON

Key Parameters	Version 2	High Temperature			Normal Temperature		
		[54]	[49]	Version 1	[46]	[44]	[53]
Process	1µm PDSOI CMOS	FDSOI	0. 5µm SOI BiCMOS	1µm PDSOI CMOS	0.35µm CMOS	0.7µm CMOS	32nm CMOS
Sensing	Bandgap	PIN Diode	Thermal Diffusivity	Bandgap	Delay Line	Bandgap	Bandgap
Calibration Points	1	2	0	1	2	1	1
Current	20µA	50µA	700µA	25µA	12µA	75µA	3.8mA
Accuracy	1.6°C	3°C	0.6°C	2°C	0.6°C	0.1°C	2.25°C
Area	0.41mm^2	N/A	1mm^2	0.45mm^2	0.6mm^2	4.5mm^2	0.02mm^2
Temperature Range	25 - 225°C	25-250°C	-70-225°C	25 - 225°C	0 - 90°C	-55 - 125°C	20-100°C
Inaccuracy FOM(nJ%^{2})*	2.2x10^4	N/A	5.6x10^5	4x10^4	2.3x10^4	2.3x10^3	3.1x10^3
Resolution(°C)	0.28	0.8	0.026	0.28	0.09	0.01	0.19

**Inaccuracy FOM = Energy/Conversion * (Relative inaccuracy) ^2, Relative Inaccuracy (%) = 100*Max Error / Specified temperature range*
**Small FOM indicates better performance*

the architecture of version 1 is further optimized for area and power with accuracy improvement for more samples. Calibration is done at the digital back-end and hence precision of analog front-end is relaxed. It has lowest power and smallest chip area, as well as best FOM, among previously reported temperature sensors operating beyond 200°C [49], [54] as shown in TABLE 4-1.

Bandgap based temperature sensors have achieved the best performance as far as accuracy is concerned. One of the reasons for the superior performance is the superior device characteristics of the substrate PNP transistor which is robust. In addition, one-point calibration can mitigate the process spread in a bandgap temperature sensor. This is a huge advantage of bandgap sensors from cost perspective and is the reason why bandgap front-end was persisted upon in this thesis. Only thermal diffusivity sensors have better characteristics than this with respect to calibration points. However, the difference in this design is the use of diodes in our design compared to BJT's in majority of sensors based on bandgap. This has resulted in additional non-ideality due to recombination current and more process spread which is one of the drawbacks of our design. Based on the proposed concept of this design, we have a simplified architecture which is power efficient, and in this design the precision factor and calibration is moved to the digital back-end without the need for trimming. The simplification of analog front-end and time-domain approach also makes our design easily portable to lower technology nodes which may not be possible for conventional bandgap designs due to their analog intensive nature. The focus of this thesis has been to demonstrate a temperature sensor for high temperature category. Other architectures have achieved state-of-the-art performance especially in the conventional

temperature category. To better/match the performance of those architectures, further incremental improvements cycles are needed for this design.

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 Conclusion

In this thesis, two temperature sensor designs for high temperature applications have been proposed and demonstrated in a PDSOI CMOS technology. The first design is a smart temperature sensor front-end based on threshold voltage. With a newly proposed threshold voltage extraction circuit, a well-defined CTAT signal with consistent TC over different samples has been obtained. A precision voltage reference, has also been proposed as part of the analog front-end, but can be used alone, and achieved a mean box-model temperature coefficient of 27 ppm over a temperature range of -25 to 250°C, which is the lowest reported in the HT category. The temperature sensor has yielded a measured temperature error of ±6°C over the temperature range of -25 to 250°C. All samples show consistent curvature behaviour, which means that the error may be further minimized by employing curvature compensation technique.

The second design is a time-domain bandgap based smart temperature sensor. The proposed architecture does not need an explicit bandgap reference and has a simple architecture. The improved version of the temperature sensor has achieved a worst-case inaccuracy of +1.6°C/-1.5°C and consumes only 20μA from a 4.5-V supply. The simplified analog circuitry, time-domain architecture and predominantly digital nature also make the sensor more suitable for porting to the latest technology nodes for future applications. This

design has achieved the best FOM in the HT category of temperature sensors and is believed to be the first bandgap based temperature sensor operating above 200°C.

5.2 Future Work

The threshold voltage front-end presented in this work requires two-point calibration to mitigate the process variations which is costly in a mass production environment. Hence, a better calibration technique or process variation immune architecture based on the concept could be developed. Though the voltage reference has achieved good TC, the temperature error from the front-end is on the higher end, ±6°C. Therefore, to improve the temperature error performance, techniques such as ratiometric curvature correction or other novel curvature correction techniques may be implemented.

The time-domain ratiometric temperature sensor has achieved good performance in the HT category. However, there is further scope for performance improvement, such as accuracy and power, when compared to state-of-the-art sensors in military/commercial temperature range category. Better calibration technique at the digital back-end and digitally assisted techniques could be explored to further reduce the error.

BIBLIOGRAPHY

[1] Texas Instruments. “Down Hole Drilling”. Internet: http://www.ti.com/solution/down_hole_drilling, Nov. 11, 2009 [Dec. 03, 2013].

[2] L. J. Palkuti, J. Prince, and A. S. Glista, Jr., "Integrated Circuit Characteristics at 260°C for Aircraft Engine-Control Applications," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology,* vol. 2, pp. 405-412, 1979.

[3] J. Haslett, F. Trofimenkoff, I. Finvers, F. Sabouri, and R. Smallwood, "High temperature electronics using silicon technology," in *Solid-State Circuits Conference, 1996. Digest of Technical Papers. 42nd ISSCC., 1996 IEEE International*, 1996, pp. 402-403.

[4] T. Rajender. “Temperature Sensor Technology Transition and End-user Growth Trends”. Internet: http://www.sensorsmag.com/sensors-mag/temperature-sensor-technology-transition-and-end-user-growth-9321, Dec. 16, 2011 [Dec. 03, 2013].

[5] A. J. M. Eoomkamp and G. C. M. Meijer, "An Accurate Biomedical Temperature Transducer with On-Chip Microcomputer Interfacing," in *Solid-State Circuits Conference, 1985, ESSCIRC '85. 11th European*, 1985, pp. 214-217.

[6] M. J. S. Smith, L. Bowman, and J. D. Meindl, "Analysis, design, and performance of micropower circuits for a capacitive pressure sensor IC," *IEEE Journal of Solid-State Circuits,* vol. 21, pp. 1045-1056, 1986.

[7] G. C. M. Meijer, R. Van Gelder, V. Nooder, J. V. Drecht, and H. Kerkvliet, "A Three-Terminal Wide-Range Temperature Transducer with Microcomputer Interfacing," in *Solid-State Circuits Conference, 1986. ESSCIRC '86. Twelfth European*, 1986, pp. 161-163.

[8] P. Krummenacher and H. Oguey, "Smart temperature sensor in CMOS technology," *Sensors and Actuators*, vol. A21-A23, pp. 636–638, Mar. 1990.

[9] A. Bakker and J.H. Huijsing, "Micropower CMOS temperature sensor with digital output," *IEEE Journal of Solid-State Circuits*, vol.31, no.7, pp.933,937, Jul 1996.

[10] C. Poki, C.-C. Chen, T. Chin-Chung, and L. Wen-Fu, "A time-to-digital-converter-based CMOS smart temperature sensor," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 1642-1648, 2005.

[11] W. Chun-Kuan, C. Wei-Shan, and L. Tsung-Hsien, "A 80kS/s 36µW resistor-based temperature sensor using BGR-free SAR ADC with a unevenly-weighted resistor string in 0.18µm CMOS," in *VLSI Circuits (VLSIC), 2011 Symposium on*, 2011, pp. 222-223.

[12] C. van Vroonhoven and K. Makinwa, "Thermal diffusivity sensors for wide-range temperature sensing," in *Sensors, 2008 IEEE*, 2008, pp. 764-767.

[13] D. F. Hilbiber, "A new semiconductor voltage standard", *ISSCC Digest Technical Papers*, vol. 7, pp. 32–33, 1964.

[14] R. J. Widlar, "Some circuit design techniques for linear integrated circuits", *IEEE Transactions on Circuit Theory*, vol. CT-12, no. 4, pp. 586–590, December 1965.

[15] R. J. Widlar, "Low voltage techniques", *IEEE Journal of Solid-State Circuits*, vol. SC-13, no. 6, pp. 838–846, December 1978.

[16] K. K. Kuijk, “A precision reference voltage source”, *IEEE Journal of Solid-State Circuits*, vol. SC-8, no. 3, pp. 222–226, June 1973.

[17] A. P. Brokaw, “A simple three-terminal IC bandgap reference”, *IEEE Journal of Solid-State Circuits*, vol. SC-9, no. 6, pp. 388–393, December 1974.

[18] I. M. Filanovsky and A. Allam, "Mutual compensation of mobility and threshold voltage temperature effects with applications in CMOS circuits," *IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications,* vol. 48, pp. 876-884, 2001.

[19] H. J. Oguey and B. Gerber, "MOS Voltage Reference based on Polysilicon Gate Work Function Difference," in *Solid State Circuits Conference - ESSCIRC 79, Fifth European*, 1979, pp. 28-30.

[20] Gray & Meyer, Analysis and Design of Analog Integrated Circuits, 4th Ed., Wiley, 2004.

[21] F. S. Shoucair, H. Wei, and J. Prem, "Electrical Characteristics of Large-Scale Integration Silicon MOSFET's at Very High Temperatures,Part III: Modeling and Circuit Behavior," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology,* vol. 7, pp. 146-153, 1984.

[22] F. S. Shoucair, "Design Consideration in High Temperature Analog CMOS Integrated Circuits," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology,* vol. 9, pp. 242-251, 1986.

[23] D. Flandre, L. Demeus, V. Dessard, A. Viviani, B. Gentinne, and J. P. Eggermont, "Design and application of SOI CMOS OTAs for high-temperature environments," in *Solid-State Circuits Conference, 1998. ESSCIRC '98. Proceedings of the 24th European*, 1998, pp. 404-407.

[24] J. P. Eggermont, D. De Ceuster, D. Flandre, B. Gentinne, P. G. A. Jespers, and J. Colinge, "Design of SOI CMOS operational amplifiers for applications up to 300°C," *IEEE Journal of Solid-State Circuits,* vol. 31, pp. 179-186, 1996.

[25] L. Lu, B. Vosooghi, J. Chen, and C. Li, "A Subthreshold-MOSFETs-Based Scattered Relative Temperature Sensor Front-End With a Non-Calibrated ± 2.5°C 3σ Relative Inaccuracy From -40°C to 100°C," *IEEE Transactions on Circuits and Systems I: Regular Papers,* vol. 60, pp. 1104-1112, 2013.

[26] L. Li, S. T. Block, D. E. Duarte, and L. Changzhi, "A 0.45-V MOSFETs-Based Temperature Sensor Front-End in 90 nm CMOS With a Noncalibrated ±3.5°C 3σ Relative Inaccuracy From -55°C to 105°C," *IEEE Transactions on Circuits and Systems II: Express Briefs,* vol. 60, pp. 771-775, 2013.

[27] G. Guang, Z. Cheng, G. Hoogzaad, and K. A. A. Makinwa, "A Single-Trim CMOS Bandgap Reference With a 3σ Inaccuracy of ±0.15% From -40°C to 125°C," *IEEE Journal of Solid-State Circuits,* vol. 46, pp. 2693-2701, 2011.

[28] S. Adriaensen, V. Dessard, and D. Flandre, "A bandgap circuit operating up to 300°C using lateral bipolar transistors in thin-film CMOS-SOI technology," in *SOI Conference, 1999. Proceedings. 1999 IEEE International*, 1999, pp. 20-21.

[29] A. Bakker and J. H. Huijsing, "A CMOS chopper opamp with integrated low-pass filter," in *Proc. ESSCIRC,* 1997, pp. 200–203.

[30] R. Burt and J. Zhang, "A micropower chopper-stabilized operational amplifier using a SC notch filter with synchronous integration inside the

continuous-time signal path," in *IEEE ISSCC Dig. Tech. Papers*, 2006, pp. 354–355.

[31] H. J. Oguey and B. Gerber, "MOS voltage reference based on polysilicon gate work function difference," *IEEE J. Solid-State Circuits,* vol. 15, pp. 264-269, 1980.

[32] R. A. Blauschild, P. A. Tucci, R. S. Muller, and R. G. Meyer, "A new NMOS temperature-stable voltage reference," *IEEE J. Solid-State Circuits,* vol. 13, pp. 767-774, 1978.

[33] C. Eisenhut and J. W. Klein, "SIMOX voltage references for applications up to 275°C using the threshold voltage difference principle," in *SOI Conference, 1997. Proceedings., 1997 IEEE International*, 1997, pp. 110-111.

[34] G. De Vita and G. Iannaccone, "An ultra-low-power, temperature compensated voltage reference generator," in *Proceedings of the IEEE 2005 Custom Integrated Circuits Conference*, 2005, pp. 751-754.

[35] G. De Vita and G. Iannaccone, "A Sub-1-V, 10 ppm/°C, Nanopower Voltage Reference Generator," *IEEE J. Solid-State Circuits,* vol. 42, pp. 1536-1542, 2007.

[36] K. Ueno, T. Hirose, T. Asai, and Y. Amemiya, "A 0.3- μW, 7 ppm/°C CMOS Voltage reference circuit for on-chip process monitoring in analog circuits," in *Solid-State Circuits Conference, 2008. ESSCIRC 2008. 34th European*, 2008, pp. 398-401.

[37] L. Ka Nang and P. K. T. Mok, "A CMOS voltage reference based on weighted ΔV_{GS} for CMOS low-dropout linear regulators," *IEEE J. Solid-State Circuits,* vol. 38, pp. 146-150, 2003.

[38] Z. Ze-kun *et al.*, "A CMOS Voltage Reference Based on Mutual

Compensation of Vtn and Vtp,"*IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 59, pp. 341-345, 2012.

[39] M. Assaad *et al*., "Design and characterisation of ultra-low-power SOI-CMOS IC temperature level detector," *Electronics Letters*, vol. 48, pp. 842-844, 2012.

[40] M. Assaad, P. Gerard, L.A. Francis, and D. Flandre., "Ultra low power, harsh environment SOI-CMOS design of temperature sensor based threshold detection and wake-up IC," in *SOI Conference (SOI), 2010 IEEE International*, 2010, pp. 1-2.

[41] V. Banu *et al*., "High temperature-low temperature coefficient analog voltage reference integrated circuit implemented with SiC MESFETs," in *ESSCIRC (ESSCIRC), 2013 Proceedings of the*, 2013, pp. 427-430.

[42] M. A. P. Pertijs and J. H. Huijsing, *Precision Temperature Sensors in CMOS technology*: Springer Netherlands, 2006.

[43] M. A. P. Pertijs, A. Niederkorn, Xu Ma, B. McKillop, A. Bakker, J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ±0.5°C from -50°C to 120°C," *IEEE Journal of Solid-State Circuits*, vol.40, no.2, pp.454,461, Feb. 2005.

[44] M. A. P. Pertijs, K. A. A. Makinwa, and J. H. Huijsing, "A CMOS smart temperature sensor with a 3σ inaccuracy of ±0.1°C from -55°C to 125°C," *IEEE Journal of Solid-State Circuits*, vol. 40, pp. 2805-2815, 2005.

[45] F. Sebastiano, L.J. Breems, K. A. A. Makinwa, S. Drago, D.M.W. Leenaerts, B. Nauta, "A 1.2-V 10-µW NPN-Based Temperature Sensor in 65-nm CMOS With an Inaccuracy of 0.2°C(3σ) From 70°C to 125°C," *IEEE Journal of Solid-State Circuits*, vol.45, no.12, pp.2591,2601, Dec. 2010.

[46] C. Poki, C. Chun-Chi, P. Yu-Han, W. Kai-Ming, and W. Yu-Shin, "A Time-Domain SAR Smart Temperature Sensor With Curvature Compensation and a 3σ Inaccuracy of -0.4°C ~ +0.6°C Over a 0°C to 90°C Range," *IEEE Journal of Solid-State Circuits*, vol. 45, pp. 600-609, 2010.

[47] C. Poki, C. Tuo-Kuang, W. Yu-Shin, and C.-C. Chen, "A Time-Domain Sub-Micro Watt Temperature Sensor With Digital Set-Point Programming," *IEEE Sensors Journal*, vol. 9, pp. 1639-1646, 2009.

[48] X. Tang, W.-T. Ng, and K.-P. Pun, "A 0.9 V 5 kS/s resistor-based time-domain temperature sensor in 90 nm CMOS with calibrated inaccuracy of − 0.6 °C/0.8 °C from 40 °C to 125 °C," in Proc. IEEE Asian Solid-State Circuits Conference., Nov. 2013, pp. 169–172.

[49] C. P. L. van Vroonhoven and K. A. A. Makinwa, "An SOI thermal-diffusivity-based temperature sensor with ±0.6°C (3σ) untrimmed inaccuracy from −70°C to 225°C," *Sensors and Actuators A: Physical*, vol. 188, pp. 66-74, 2012.

[50] S. M. Kashmiri, X. Sha, and K. A. A. Makinwa, "A Temperature-to-Digital Converter Based on an Optimized Electrothermal Filter," *IEEE Journal of Solid-State Circuits*, vol. 44, pp. 2026-2035, 2009.

[51] C. P. L. van Vroonhoven, D. D'Aquino, K. A. A. Makinwa, "A thermal-diffusivity-based temperature sensor with an untrimmed inaccuracy of ±0.2°c (3s) from −55°c to 125°c,"*Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2010 IEEE International* , vol., no., pp.314,315, 7-11 Feb. 2010.

[52] S. Xia and K. A. A. Makinwa, "Design of an Optimized Electrothermal Filter for a Temperature-to-Frequency Converter," *2007 IEEE Sensors*, vol.,

no., pp.1255,1258, 28-31 Oct. 2007.

[53] J. Shor, K. Luria, and D. Zilberman, "Ratiometric BJT-based thermal sensor in 32nm and 22nm technologies," in *Solid-State Circuits Conference Digest of Technical Papers (ISSCC), 2012 IEEE International*, 2012, pp. 210-212.

[54] B. Rue and D. Flandre, "A SOI CMOS Smart High-Temperature Sensor," in *SOI Conference, 2007 IEEE International*, 2007, pp. 111-112.

[55] S. Adriaensen, V. Dessard, , D. Flandre, "25 to 300°C ultra-low-power voltage reference compatible with standard SOI CMOS process," *Electronics Letters* , vol.38, no.19, pp.1103,1104, 12 Sep 2002.

[56] G. Groeseneken, J. P. Colinge, H. E. Maes, J. C. Alderman, and S. Holt, "Temperature dependence of threshold voltage in thin-film SOI MOSFETs," *IEEE Electron Device Letters*, vol. 11, pp. 329-331, 1990.

[57] R. S. Muller and T. I. Kamins, *Device Electronics for Integrated Circuits*, 2nd ed. New York: Wiley, 1986, p. 56.

[58] UC Berkely Device Group. (30th August 2013). BSIMSOI. Available: http://www-device.eecs.berkeley.edu/bsim/?page=BSIMSOI.

[59] J. Pathrose *et al*., "High temperature bandgap reference in PDSOI CMOS with opeating temperature up to 300°C," in *Radio-Frequency Integration Technology, 2012. IEEE International Symposium on*, 2012, pp. 110-112.

[60] L. Li, L. Changzhi, and C. Jinghong, "An all-CMOS low supply voltage temperature sensor front-end with error correction techniques," in *2012 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2012, pp. 2973-2976.

[61] S. T. Block, L. Yiran, Y. Yi, and L. Changzhi, "0.6-2.0 V, All-CMOS temperature sensor front-end using bulk-driven technology," in *2010 IEEE Dallas Circuits and Systems Workshop (DCAS)*, 2010, pp. 1-4.

[62] J.M. Steininger,"Understanding wide-band MOS transistors,", IEEE Circuits and Devices Magazine,vol.6, no.3, pp.26-31, May 1990.

[63] Mandal, S.; Arfin, S.; Sarpeshkar, R., "Fast startup CMOS current references," *Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on*, vol., no., pp.4 pp., 21-24 May 2006.

[64] D.G. Haigh and B. Singh, "A Switching Scheme for Switched-Capacitor Filters which Reduces Effect of Parasitic Capacitances Associated with with Control Terminals," *Proc. IEEE Int. Symp. on Circuits and Systems,* vol. 2, pp.586-589, Jun. 1983.