SOURCE/DRAIN ENGINEERING IN INGAAS N-MOSFETS FOR LOGIC DEVICE APPLICATIONS

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DECLARATION

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information that have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Sujith Subramanian

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Table of Contents

DECLARATION .... **iii**

Acknowledgements .... **iv**

Table of Contents .... **vi**

Summary .... **ix**

List of Tables .... **xii**

List of Figures .... **xiii**

List of Symbols .... **xxv**

Chapter 1 Introduction **1**

1.1 Background 1
1.2 Scaling Challenges of Transistors 2
1.2.1 Leakage currents 3
1.2.2 Random dopant fluctuation 5
1.2.3 Power constrained scaling 5
1.3 Motivation for Using III-V Materials 6
1.4 Challenges for III-V CMOS Logic 9
1.4.1 Realization of high-quality gate stack 10
1.4.2 Integration on a Si platform 12
1.4.3 III-V P-MOSFETs 13
1.4.4 Source/Drain regions with low C_{GD} and R_{SD} 14
1.4.5 Density of States (DOS) Bottleneck 15
1.5 Objective and Organization of Thesis 16

Chapter 2 Source/Drain Series Resistance in InGaAs N-MOSFETs **18**

2.1 Introduction 18
2.2 Concept of Source/Drain Series Resistance 18
2.3 Elements of Source/Drain Resistance 19
2.4 Source/Drain Engineering in III-V N-MOSFETs 21

2.5 Self-Aligned Metallic Contacts for InGaAs N-MOSFETs 23
2.5.1 Ni-InGaAs Contact Technology 24
2.5.2 Other Self-Aligned Contact Schemes 31
2.6 Summary 34
Chapter 3 Selective Wet Etching Process for Contact Formation in InGaAs N-MOSFETs with Self-Aligned Source and Drain 35
3.1 Introduction 35
3.2 Experimental Procedures 38
3.2.1 Method of Determining the Etch Rate and Selectivity 38
3.2.2 Selection of Chemicals and Conditions 39
3.3 Results and Discussion 41
3.3.1 Selective Etch of Ni over Ni-InGaAs 41
3.3.2 Selective Etch of NiPt over NiPt-InGaAs 49
3.4 Conclusion 57
Chapter 4 Embedded Metal Source/Drain for $In_{0.53}Ga_{0.47}As$ N-Channel Ultra-Thin Body Field-Effect Transistor 58
4.1 Introduction 58
4.2 InGaAs UTB-FET with an *e*MSD Architecture 60
4.2.1 Formation of Ni-InAlAs 60
4.2.2 Device Fabrication 62
4.2.3 Results and Discussion 65
4.3 Evaluating eMSD Architecture for Future Technology Nodes: A Simulation Study 74
4.3.1 Structure and Parameters Used for Simulation 74
4.3.2 Effect of S/D Thickness on the Parasitic Capacitance (C_{GD}) 77
4.3.3 Effect of S/D Thickness on the Parasitic Resistance (R_{SD}) 80
4.3.4 Influence of S/D Thickness on Short Channel Effects 84
4.3.5 InGaAs FinFET with *e*MSD to Reduce Short Channel Effects 85
4.4 Conclusion 87
Chapter 5 $P_2S_5/(NH_4)_2S_x$-Based Sulfur Monolayer Doping for Source/Drain Extensions in InGaAs N-MOSFETs 88
5.1 Introduction 88

5.2 SMLD of InGaAs using P_2S_5 and $(NH_4)_2S_x$ 91
5.2.1 Motivation for Using P2S5/(NH4)2Sx 91
5.2.2 Surface Chemistry 91
5.2.3 Blanket and TLM Sample Preparation 92
5.3 Material Characterization 94
5.4 Optical Characterization Using IRSE 100
5.4.1 Motivation for Using IRSE 100
5.4.2 Details of the Measurement 101
5.4.3 Results and Discussion 102
5.5 MOSFET Fabrication and Characterization 107
5.6 Conclusion 112
Chapter 6 Conclusion and Future Directions 114
6.1 Conclusion 114
6.2 Contributions of This Thesis 115
6.2.1 Selective Etching Process for the Formation of Self-Aligned Metallic S/D for InGaAs N-MOSFETs 115
6.2.2 *e*MSD Architecture for InGaAs N-MOSFETs with Self-Aligned Ni-InGaAs S/D 115
6.2.3 $P_2S_5/(NH_4)_2S_x$-Based Monolayer Doping Technique for SDEs in InGaAs N-MOSFETs 116
6.3 Future Directions 116
References 119
Appendix 158
List of Publications 158

Summary

Source/Drain Engineering in InGaAs N-MOSFETs for Logic Device Applications

by

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For the past four decades, silicon (Si) based complementary metal-oxide-semiconductor (CMOS) technology has been dominating digital integrated circuits (ICs) in the semiconductor industry. Over the years, as transistors are scaled down and their performance enhanced, the need for these devices to consume lower power has become essential. Power consumption in ICs can be minimized by reducing the supply voltage (V_{DD}) and leakage currents in the transistor. In the past few years, improvement in device performance has been brought about through innovations in the design of the MOSFET (such as strain engineering). However, it will be challenging to continue this performance enhancement of Si CMOS transistors in the near future, due to the fundamental limitations in the material properties of Si. Due to these fundamental limits, reducing the V_{DD} further would have direct repercussions on the device performance. Therefore, non-Si electronic materials have been explored for future logic applications. InGaAs, with its high electron mobility, is an attractive candidate to replace Si as the channel layer for N-MOSFETs at sub-10 nm technology nodes.

However, several challenges need to be overcome before this technology can be successfully integrated in the IC manufacturing process.

In this thesis, source/drain (S/D) engineering for InGaAs N-MOSFETs is explored. Contact metals with low bulk resistivities, and low contact resistivities on highly n-type doped (n^{++}) InGaAs are needed to reduce S/D resistances (R_{SD}) and in turn boost the drive current of the MOSFETs. Due to their material properties, Ni based alloys (such as Ni-InGaAs and NiPt-InGaAs) are attractive materials for potential use as S/D contacts in InGaAs N-MOSFETs. Therefore, a selective etching process was developed to evaluate the feasibility of using Ni-InGaAs and NiPt-InGaAs as contact materials in an InGaAs N-MOSFET. The etch rates of Ni-InGaAs and NiPt-InGaAs in several wet etch chemistries were extracted using various characterization techniques. Subsequently, the selectivities of etching Ni and NiPt over Ni-InGaAs and NiPt-InGaAs, respectively, were determined. High selectivities were obtained for HCl and HNO_3 based chemistries, making them the most favorable choices for the selective removal of Ni and NiPt over Ni-InGaAs and NiPt-InGaAs, respectively.

For achieving transistors with high drive current and switching speed, it is important to minimize the parasitic gate-to-drain capacitance (C_{GD}) and R_{SD}. In addition, at sub-10 nm technology nodes, advanced structures such as ultra-thin body FETs are required to reduce the short channel effects (SCE). In this thesis, an embedded metal S/D (*e*MSD) architecture was developed to reduce R_{SD} and C_{GD} in InGaAs n-channel UTB-FETs. Long channel devices with Ni-InGaAs/Ni-InAlAs *e*MSD were successfully demonstrated with the help of the selective etching process developed earlier. In addition, the viability of using the eMSD design at future technology nodes was evaluated using technology computer aided design (TCAD) simulations. The results indicated that UTB-FETs with R_{SD} and C_{GD} that meet the International

Technology Roadmap for Semiconductors (ITRS) requirements, can be achieved using the *e*MSD design. In addition, 3D structures such as fin field effect transistors (FinFETs) would be eventually required to further reduce SCEs such as drain-induced-barrier-lowering (DIBL).

To further reduce the R_{SD} in InGaAs N-MOSFETs, ultra-shallow S/D extension (SDE) regions with low resistances are required. These ultra-shallow junctions have to be very abrupt and highly doped. Hence, sulfur monolayer doping (SMLD) using $P_2S_5/(NH_4)_2S_x$ solution was developed for the formation of SDEs in InGaAs N-MOSFETs. The n^{++}-InGaAs films formed using SMLD were studied using various characterization methods. The electrical resistivities, carrier relaxation times and active doping concentration (N_D) of the shallow n^{++}-InGaAs films were then extracted using Infrared Spectroscopic Ellipsometry (IRSE). Sub-10 nm n^{++}-InGaAs layers were realized using SMLD with N_D of ~1.7×10^{19} cm^{-3}. The SMLD process using $P_2S_5/(NH_4)_2S_x$ was demonstrated on planar InGaAs N-MOSFETs and the effect of the dopant activation conditions on device performance was studied.

List of Tables

Table 1.1. Scaling trends to improve integrated circuit performance [5]. 3

Table 2.1. Benchmarking the various self-aligned contact schemes on $In_{0.53}Ga_{0.47}As$...33

Table 3.1. Etch rates of Ni and Ni-InGaAs in various etch chemistries. 40

Table 3.2. Chemical reactions between Ni and HCl or HNO_3 [251]. 40

Table 3.3. Etch selectivity of Ni over Ni-InGaAs in different etchants. 49

Table 4.1. Summary of the parameters used in the 2D simulation. 77

Table 4.2. Comparison of the merits of the different S/D architectures. 86

Table 5.1. Electrical and physical parameters for SMLD and in situ doped n^{++}-InGaAs samples. 105

Table 5.2. The activation efficiency calculated from the active and total sulfur dose obtained from IRSE and SIMS measurements. 106

List of Figures

Fig. 1.1. Plot of the electron (black circles) and hole mobilities (blue squares) at 300 K, for Si, germanium (Ge) and various III-V compound semiconductors. 7

Fig. 1.2. (a) Electron mobility (μ_e) versus composition x for $In_xGa_{1-x}As$. μ_e increases with higher indium composition. (b) Electron effective mass m_e* versus composition x for $In_xGa_{1-x}As$. m_e* decreases with increasing indium composition, leading to higher μ_e in (a). (c) Band gap E_G versus composition x for $In_xGa_{1-x}As$. $In_xGa_{1-x}As$ offers a wide range of E_G from 0.36 eV to 1.42 eV...7

Fig. 1.3. Comparison of $I_{D,Sat}$-V_{GS} between a Si N-MOSFET (blue solid curve) and an InGaAs N-MOSFET (red solid curve). A higher I_{ON} can be achieved for the InGaAs N-MOSFET at the same gate overdrive (V_{GS}-V_T). Furthermore, using an InGaAs N-MOSFET allows the down-scaling of V_{DD} without compromising I_{ON}. The InGaAs and Si N-MOSFETs are assumed to have the same subthreshold swing (S)...9

Fig. 1.4. Schematic illustrating the key technical challenges faced in the realization and integration of high mobility III-V channel MOSFET on Si substrates for future logic applications.................................10

Fig. 2.1. (a) Schematic illustrating the different resistance components in an InGaAs N-MOSFET (in the linear regime). The total resistance R_T of the transistor is the summation of the channel resistance R_{CH}, and the parasitic resistance $R_{SD} = R_{SOURCE} + R_{DRAIN}$. (b) The scaling trend for R_{CH} and R_{SD} in Si N-MOSFETs (taken from Ref. [164]). As R_{CH}

reduces with gate length, R_T becomes dominated by R_{SD}. Therefore, R_{SD} needs to be minimized to achieve a high I_{ON} in the transistor. .19

Fig. 2.2. Schematic illustrating the parasitic resistance components of an InGaAs N-MOSFET. 20

Fig. 2.3. Schematic illustrating the process of Ni-InGaAs formation...........24

Fig. 2.4. (a) As-deposited Ni film (~30 nm) on an InGaAs/InP substrate. (b) The ~45 nm thick Ni-InGaAs film formed after the samples were annealed at 250 °C. (c) High resolution TEM of the Ni-InGaAs/InGaAs interface. Crystalline Ni-InGaAs was formed and the atomic compositions of Ni, In, Ga, and As were 51, 12, 14, and 23, respectively. These figures are taken from Ref. [226]....................24

Fig. 2.5. (a) TEM image of the Ni-InGaAs/InGaAs sample. (b) The SAD pattern obtained from the region shown in (a). The diameter of the circle is 150 nm. (c) High resolution TEM image of Ni-InGaAs/InGaAs. The corresponding diffraction patterns are shown in the inset. (d) Unit cell of Ni-InGaAs phase. Ni-InGaAs shows a NiAs (B8) type of structure. These figures are taken from Ref. [227]. 25

Fig. 2.6. (a) R_S of Ni-on-InGaAs samples annealed at various temperatures for a fixed time of 60 s. The inset shows an illustration of the formation of Ni-InGaAs (bottom) by annealing as-deposited Ni-on-InGaAs (top) at temperature T_{anneal} for time t_{anneal}. (b) Time evolution of R_S for ~28 nm of deposited Ni on InGaAs annealed at 250 °C. These figures are taken from Ref. [227]...26

Fig. 2.7. Correlation between the as-deposited Ni thickness and the corresponding Ni-InGaAs thickness. A linear relationship is observed. A thickness ratio of ~1: 1.7 for Ni to Ni-InGaAs was extracted. This figure is taken from Ref. [227]. 27

Fig. 2.8. (a) R_S of Ni-InGaAs as a function of T_{anneal}. The samples were annealed for 5 min in vacuum. R_S before and after selective wet etching of unreacted metal is also plotted. (b) ρ_C of Ni-InGaAs as a function of T_{anneal} on samples with (blue stars) and without (black

diamond-shaped dots) SiO_2 cap. This figure was taken from Ref. [156]..27

Fig. 2.9. (a) Schematic illustrating the cross-section of Ni-InGaAs Schottky diodes and (b) the corresponding energy band diagram at the Ni-InGaAs/InGaAs interface [231]..29

Fig. 2.10. (a) Schematic of the process flow used in the fabrication of an InGaAs N-MOSFET with Ni-InGaAs self-aligned S/D. Cross-sectional TEM images of various parts of the MOSFET are shown in (b)-(d). Ni-InGaAs was ~43 nm thick. A distinct interface between Ni-InGaAs and InGaAs was observed. These figures are taken from Ref. [232]..30

Fig. 2.11. (a) I_D-V_{GS} and G_M-V_{GS} plot of an $In_{0.7}Ga_{0.3}As$ N-MOSFET with self-aligned Ni-InGaAs S/D. The device with L_G = 1 µm has an I_{ON} of ~100 µA/µm and peak G_M of 74 µS/µm at V_D = 1.1 V. (b) I_D-V_D characteristics of the same transistor at various gate overdrives (V_{GS} - V_T), from 0 V to 2.5 V. These figures are taken from Ref. [232]..30

Fig. 2.12. (a) R_S versus T_{anneal} for Pd-InGaAs formed from the reaction between palladium (Pd) and InGaAs. Anneal time is fixed at 60 s. The R_S values for Ni-InGaAs are plotted for reference. The dashed lines indicate the R_S of as-deposited Ni and Pd. (b) R_S versus T_{anneal} for Co-InGaAs formed from the reaction between Co and InGaAs. Anneal time is fixed at 60 s. Co-InGaAs was formed at 350 ºC. The dashed line indicates the R_S of as-deposited Co. (a) is taken from Ref. [233] and (b) is taken from Ref. [234]. 32

Fig. 3.1. An illustration of the process flow used to form self-aligned metallic S/D in an InGaAs N-MOSFET which involves (a) a blanket deposition of Ni over the sample, (b) an annealing step to react Ni and InGaAs to form Ni-InGaAs, and (c) a selective etch to remove the unreacted Ni...36

Fig. 3.2. Schematic of the samples used for determining the etch rates of Ni-InGaAs and Ni; (a) Unpatterned or blanket sample comprising of Ni-InGaAs formed on $In_{0.53}Ga_{0.47}As$/InP substrate, (b) blanket sample

comprising of Ni deposited on silicon dioxide (SiO_2) on a Si substrate, and (c) patterned Ni film formed on SiO_2 on Si. 37

Fig. 3.3. R_S^{-1} versus time (t) plot for various etch chemistries: (a) HF:H_2O (1:100), (b) HNO_3:H_2O (1:10), (c) HNO_3:H_2O (1:20), (d) HCl (concentrated), (e) HCl:H_2O (1:10) 25 °C, (f) HCl:H_2O (1:10) 50 °C, (g) HCl:H_2O (1:10) 70 °C, (h) HCl:H_2O (1:10) 90 °C. The R_S increases with time indicating a decrease in the metal thickness. ...42

Fig. 3.4. Cross-sectional TEM image of the Ni-InGaAs formed on the $In_{0.53}Ga_{0.47}As$/InP substrate. From the image, the thickness of the Ni-InGaAs film was estimated to be 86 nm. All the TEM in this Chapter was done by a colleague, Dr. Qian Zhou. 43

Fig. 3.5. Thickness of the metal film (t_f) versus time (t) plot for various etch chemistries: (a) HF:H_2O (1:100), (b) HNO_3:H_2O (1:10), (c) HNO_3:H_2O (1:20), (d) HCl (concentrated), (e) HCl:H_2O (1:10) 25 °C, (f) HCl:H_2O (1:10) 50 °C, (g) HCl:H_2O (1:10) 70 °C, (h) HCl:H_2O (1:10) 90 °C. The thickness can be observed to decrease with time. 44

Fig. 3.6. The etch rate of Ni in the various etch chemistries which are obtained from the R_S method and from surface profiler measurements. HNO_3:H_2O (1:10), HNO_3:H_2O (1:20), HCl (concentrated) etch Ni faster compared to HCl:H_2O (1:10) chemistries. The etch rate of Ni in HCl:H_2O (1:10) increases with higher temperatures. The etch rate from the surface profiler method was slightly higher than those from the R_S method. This suggests that the etch rates could have a pattern dependence...45

Fig. 3.7. Surface profiler measurements showing the step height of the patterned Ni sample at different times during the etching process in: (a) HNO_3 (1:10) and (b) HNO_3 (1:20)..45

Fig. 3.8. The etch rate of Ni-InGaAs in the various etch chemistries which are obtained from the R_S method and from TEM images. HCl (concentrated) etches Ni-InGaAs the slowest. HNO_3:H_2O (1:10) etches Ni-InGaAs faster compared to HNO_3:H_2O (1:20). The etch

rate of Ni-InGaAs in HCl:H_2O (1:10) at room temperature was low and it increased with higher temperatures. It was also observed that HF: H_2O (1:100) etches Ni-InGaAs at a slow rate. 47

Fig. 3.9. Cross-sectional TEM images of the Ni-InGaAs remaining on the $In_{0.53}Ga_{0.47}As$/InP substrate after a 3 minute etch (at 25 °C) in: (a) HCl (concentrated) and (b) HNO_3 (1:20). 47

Fig. 3.10. Schematic of the samples used for determining the etch rates of NiPt-InGaAs and NiPt; (a) Blanket sample comprising of Ni-InGaAs formed on $In_{0.53}Ga_{0.47}As$/InP substrate, and (b) blanket sample comprising of NiPt deposited on a Si substrate. 50

Fig. 3.11. Surface roughness of Ni-InGaAs and NiPt-InGaAs formed at different annealing temperatures. The as-deposited NiPt and Ni films are represented using the dotted line. They have similar RMS roughness. The figure in the inset shows the AFM image taken from the surface of a NiPt-InGaAs sample formed at 500 °C (50 µm × 50 µm area). 50

Fig. 3.12. Cross-sectional TEM images of the samples used to determine the etch rates. (a) As-deposited NiPt on Si substrate, and (b) NiPt-InGaAs formed on $In_{0.53}Ga_{0.47}As$/InP substrate. 51

Fig. 3.13. R_S^{-1} versus time (t) plots for various etch chemistries: (a) HCl (concentrated), (b) HCl:H_2O (1:10), (c) HNO_3:H_2O (1:10), (d) HF:H_2O (1:100). 54

Fig. 3.14. Thickness of the metal film (t_f) versus time (t) plots for various etch chemistries: (a) HCl (concentrated), (b) HCl:H_2O (1:10), (c) HNO_3:H_2O (1:10), (d) HF:H_2O (1:100)..54

Fig. 3.15. Comparison of etch rates between (a) NiPt and Ni, and (b) NiPt-InGaAs and Ni-InGaAs using the various etch chemistries that were obtained from R_S method. 56

Fig. 3.16. Comparison of etch selectivities between NiPt over NiPt-InGaAs and Ni over Ni-InGaAs using various etch chemistries. The incorporation

of Pt into Ni-InGaAs improves the etch selectivity of HCl and HNO_3 chemistries. 56

Fig. 4.1. (a) UTB-FET with thin S/D suffers from a high R_{SD}. (b) It can be resolved by using a UTB-FET with a Raised S/D structure (RSD). However, this increases the number of process steps during device fabrication and increases the C_{GD}; thus, reducing the switching speed of the transistor. (c) Both problems can be resolved using the UTB-FET with embedded metal S/D (*e*MSD). (d) C_{GD}-R_{SD} of UTB-FETs. UTB-FET with *e*MSD provides a low R_{SD} without compromising C_{GD}. 59

Fig. 4.2. Schematic illustrating the samples used for investigating the reaction of Ni with InAlAs. (a) ~30 nm thick Ni was deposited on unpatterned $In_{0.53}Ga_{0.47}As$/InP (control sample) and reacted to form Ni-InGaAs. (b) ~30 nm thick Ni was deposited on unpatterned $In_{0.52}Al_{0.48}As$/InP and reacted to form Ni-InAlAs. The formation temperature was varied from 200 °C to 400 °C (in steps of 50 °C). Sheet resistance (R_S) of Ni-InGaAs and Ni-InAlAs alloys were extracted using four-point-probe measurements. 60

Fig. 4.3. R_S of Ni-InGaAs and Ni-InAlAs alloys formed using different annealing temperatures. R_S of both the alloys are comparable. 61

Fig. 4.4. Process flow for the fabrication of an n-channel InGaAs UTB-FET with self-aligned *e*MSD. The S/D was formed by depositing ~35 nm of Ni, which was then annealed to form Ni-InGaAs/Ni-InAlAs *e*MSD. 63

Fig. 4.5. (a) Device layout, and (b) top-view SEM image of the fabricated UTB-FET. (c) The cross-sectional TEM image (along A-A') of the UTB-FET with self-aligned *e*MSD. (d) A magnified view of the gate and drain regions, and (e) an HR-TEM image of the TaN/Al_2O_3/InGaAs/InAlAs stack. The ultra-thin InGaAs channel

layer was 10 nm thick and the Ni-InGaAs/Ni-InAlAs *e*MSD layer was ~65 nm thick. 64

Fig. 4.6. (a) I_D, I_G versus V_{GS} for control device (triangles) and UTB-FET (circles), and (b) $G_{M,ext}$-V_{GS} curves of a UTB-FET with *e*MSD. I_{ON}/I_{OFF} ratio of ~10^6 and a peak $G_{M,ext}$ of 118 μS/μm at V_D =1.2 V were obtained. 66

Fig. 4.7. I_D-V_D plot for the control device (triangles) and UTB-FET with *e*MSD (circles). Gate overdrive (V_{GS}-V_T) was varied from 0 to 2.5 V in steps of 0.5 V. 67

Fig. 4.8. Schematics of back-to-back diodes formed on (a) bulk-InGaAs/InP, and (b) on ultra-thin InGaAs/InAlAs *e*MSD layer. (c) *I-V* curves show a ~10^3 reduction in reverse current due to the presence of the InAlAs barrier layer [Energy band gap (E_G) = 1.48 eV]. 68

Fig. 4.9. Schematic of back-to-back diodes structures on (a) bulk-InGaAs/InP, and (b) on ultra-thin InGaAs with an InAlAs barrier layer on InP, used for the TCAD simulation. (c) The simulated *I-V* curves for the bulk-InGaAs/InP structure and (d) the corresponding energy band diagram across B-B' (no voltage bias applied). *I-V* curves shows good agreement with the experimental results for $\phi_{B,P,InGaAs}$ = 0.5 eV. (e) The simulated *I-V* curves for the ultra-thin InGaAs/InAlAs/InP structure, and (f) the corresponding energy band diagram across C-C' (no voltage bias applied). A $\phi_{B,P,InAlAs}$ of 0.65 eV was extracted by matching the simulation results with the experimental results shown in Fig. 4.8 (c). 70

Fig. 4.10. R_S-t_{METAL} of UTB-FET with *e*MSD and Ni-InGaAs. The R_S of the 65 nm thick *e*MSD was 20 Ω/square. 71

Fig. 4.11. (a) Schematic of the cross-section (A-A') of the device shown in Fig. 4.5 (b). The S/D probe spacing from the device channel (P_{SP}) was ~50 μm. (b) Plot of the total resistance (R_T = V_D/I_D) as a function of V_{GS} in the linear regime (V_D = 0.1 V) of the same device as in Fig. 4.6. The components of R_{SD} are shown in the inset of (b). It consists of the *e*MSD resistance (R_{eMSD}) and the contact resistance (R_C) between

Ni-InGaAs and the InGaAs channel. Their percentage contribution to R_{SD} is ~25 % and ~75 %, respectively. 72

Fig. 4.12. Benchmarking (a) *S* of UTB-FET with *e*MSD, bulk-InGaAs N-MOSFETs with metal S/D, UTB-FETs with thin metallic S/D, and multi-gate FETs with metal S/D, and (b) R_{SD} of InGaAs N-MOSFET with *e*MSD with reported R_{SD} of bulk-InGaAs N-MOSFETs and UTB-FETs with thin metallic S/D. 74

Fig. 4.13. Schematics of the structures used for the 2D simulation: (a) UTB-FET with thin S/D (control), (b) UTB-FET with RSD, and (c) UTB-FET with *e*MSD. 75

Fig. 4.14. Schematic showing the different capacitance components in a UTB-FET. 78

Fig. 4.15. C_{GD} as a function of V_{GS} for different V_D in InGaAs UTB-FETs with (a) thin S/D, (b) RSD, and (c) *e*MSD. The parasitic components can be observed at low V_{GS} where inversion layer in the channel is yet to be formed. The RSD architecture results in a high parasitic capacitance due to an increase in C_{DOF}. 79

Fig. 4.16. C_{GD} as a function of V_{GD} is compared for the different S/D architectures. C_{GD} for devices with *e*MSD thicknesses are comparable to the control structure. C_{GD} increases with *d* for the RSD architecture due to higher C_{DOF}. 80

Fig. 4.17. Schematic showing the different resistance components in a UTB-FET. 81

Fig. 4.18. I_D as a function of V_{GS} for different V_D in InGaAs UTB-FETs with (a) thin S/D, (b) RSD, and (c) eMSD. In the control sample, for L_G of 15 nm, I_D of ~0.9 mA/µm at V_D of 0.63 V was obtained. A higher DIBL was observed for the RSD and eMSD structures. 81

Fig. 4.19. I_D is compared with varying *d*. The comparison is done at a V_{GS} - V_T of 0.5 V due to DIBL effect in the *e*MSD structure. 82

Fig. 4.20. Current density contours (V_{GS} - V_T = 0.5V, V_D = 0.63 V) for (a) thin S/D, (b) RSD, and (c) *e*MSD architectures. A current crowding effect

was observed in the RSD structure, resulting in a higher effective R_C. This in turn lowers I_D. Higher I_D for the *e*MSD design is due to the lower R_{CH} and R_{SD} resulting from DIBL effect and spreading of the current at SDE/ Ni-InGaAs interface, respectively. 83

Fig. 4.21. (a) Extracted values of R_T for the various architectures as a function of *d*. (b) Comparison of the different resistance components R_{CH} and R_{SD} in the different structures. R_{CH} was estimated by taking the potential difference across the channel 0.5 nm below the gate oxide. A lower parasitic resistance of ~110 Ω·μm was achieved using the *e*MSD structure. 84

Fig. 4.22. DIBL as a function of *d*, for the various S/D architectures. DIBL increases with *d* for RSD due to the increase in $C_{DOF.}$ DIBL increases with *d* for *e*MSD due to the increase in C_{DIF}. 85

Fig. 4.23. Schematic of the structure used for the simulation. FinFET with *e*MSD structure was simulated with *d* of 35 nm.............................85

Fig. 4.24. Comparison of the device performance: (a) I_D vs V_{GS}, and (b) the SCE between UTB-FET and FinFET with *e*MSD. The I_D is comparable to that of the planar UTB-FET. The *S* and the DIBL are reduced (~20%) by using the 3D device architecture..86

Fig. 5.1. Cross-sectional schematic illustrating the SMLD process on fin and nanowire structures. This technique is capable of achieving abrupt junctions that are conformal and free of implant damage. Therefore, it is a promising method for forming SDEs for 3D structures such as FinFETs or nanowire transistors in future logic applications..........89

Fig. 5.2. Schematic showing a (001) InGaAs surface after treatment with $(NH_4)_2S_x$, or $P_2S_5/(NH_4)_2S_x$. Hydrolysis of P_2S_5 results in the

formation of various thiophosphates. These thiophosphates can react and form compounds on the InGaAs surface..................................90

Fig. 5.3. Schematics illustrating the key steps involved in formation of the TLM structures. 93

Fig. 5.4. (a) *I-V* characteristics of TLM structures obtained from a sample treated with $P_2S_5/(NH_4)_2S_x$, and (b) the corresponding plot of total resistance R_T versus contact spacing d_{SP}. The inset in (b) shows a top-view Scanning Electron Microscope (SEM) image of a set of fabricated TLM structures. 93

Fig. 5.5. (a) Sheet resistance R_S (in Ω per square, denoted as Ω/□) and (b) contact resistivity ρ_C of samples treated with $(NH_4)_2S_x$, or $P_2S_5/(NH_4)_2S_x$ solution. The samples were annealed at different temperatures ranging from 550 °C to 700 °C for 300 s. R_S decreases with increasing anneal temperature due to an increase in active dopant concentration and a larger junction depth. Lower R_S was obtained for samples treated with $P_2S_5/(NH_4)_2S_x$ at lower activation temperatures. Higher ρ_C at higher activation temperatures suggests a decrease in the active dopant concentration at the InGaAs surface. 96

Fig. 5.6. Sheet resistance R_S as a function of annealing time for samples treated with $P_2S_5/(NH_4)_2S_x$ solution and annealed at 600 °C. R_S decreases as the annealing time for the dopant activation step is increased. 96

Fig. 5.7. Sheet resistance R_S as a function of treatment time for samples treated with $P_2S_5/(NH_4)_2S_x$ solution. R_S remains constant even as the treatment time is increased from 10 minutes to 60 minutes. This indicates that the sulfur layer on the InGaAs surface saturates within 10 minutes of treatment. 97

Fig. 5.8. SIMS profiles of samples doped using (a) $P_2S_5/(NH_4)_2S_x$ or (b) $(NH_4)_2S_x$ solution. The samples treated with $P_2S_5/(NH_4)_2S_x$ exhibit a higher sulfur dose than those treated with $(NH_4)_2S_x$ for the same dopant activation conditions. A small amount of phosphorus (P) can

be seen at the InGaAs surface for the samples treated with $P_2S_5/(NH_4)_2S_x$. 99

Fig. 5.9. The effect of the time delay t_{delay} between the $P_2S_5/(NH_4)_2S_x$ treatment step and the SiO_2 capping step was examined. For the samples treated with $P_2S_5/(NH_4)_2S_x$, it can be seen that the sulfur dose after dopant activation at (a) 550 °C, and (b) 600 °C reduces as t_{delay} increases. This is attributed to desorption of sulfur from the InGaAs surface. Therefore, to maintain a high sulfur dose, it is important to cap the samples immediately after the $P_2S_5/(NH_4)_2S_x$ treatment. 99

Fig. 5.10. Schematic of the samples used for IRSE measurements; (a) n^{++}-InGaAs layers using SMLD or *in situ* doping on p-type InGaAs/InP substrate, (b) undoped p-type InGaAs/InP substrate, and (c) InP substrate. The surface layer was modeled using the Bruggeman approximation. 102

Fig. 5.11. Imaginary part of the pseudo dielectric function $<\varepsilon_2>$ obtained from SMLD samples. (a) $<\varepsilon_2>$ from the $P_2S_5/(NH_4)_2S_x$ based samples for the entire energy range (0.05 - 0.65 eV), and (b) a magnified view of the energy range (0.05 - 0.2 eV) where the signals from the SMLD samples can be distinguished from the undoped sample. (c) $<\varepsilon_2>$ from the $(NH_4)_2S_x$ based samples for the entire energy range (0.05 - 0.65 eV), and (d) a magnified view of the energy range (0.05 - 0.2 eV) where the signals from the SMLD samples can be distinguished from the undoped sample. 103

Fig. 5.12. The process flow for fabrication of InGaAs N-MOSFETs with S/D formed using $P_2S_5/(NH_4)_2S_x$ SMLD. Different dopant activation conditions were used. 108

Fig. 5.13. Top-view SEM image of an InGaAs N-MOSFET with a gate length of 1 μm and with S/D regions doped by $P_2S_5/(NH_4)_2S_x$ SMLD. The dopants were driven in and activated by annealing at 600 °C for 180 s for this device. 108

Fig. 5.14. (a) I_D-V_{GS}, and (b) $G_{M,int}$-V_{GS} characteristics of the planar transistor shown in Fig. 5.13. The device has a reasonable subthreshold swing

(S) and negligible DIBL. Peak $G_{M,int}$ of 140 µS/µm can be observed at V_D of 1.1 V. 109

Fig. 5.15. I_D-V_D characteristics of the same device in Fig. 5.14, with gate overdrive (V_{GS} - V_T) varying from 0 V to 2 V in steps of 0.2 V. V_T was obtained using the maximum transconductance method [165]. The device suffers from high S/D resistance, as the current has to flow through the ultra-shallow doped region over a long distance of ~5 µm between the channel and the S/D contact. 109

Fig. 5.16. (a) I_{ON} (solid symbols) at gate overdrive (V_{GS} - V_T) of 1 V, and I_{OFF} (open symbols) at (V_{GS} - V_T) of -0.5 V at V_{DS} of 0.6 V and (b) peak $G_{M,int}$ at V_D of 0.6 V are plotted as a function of the gate length. Comparison was made between samples with different annealing temperatures for dopant activation. The annealing time was kept fixed at 300 s. Using a lower thermal budget helps to achieve high I_{ON} and peak $G_{M,int}$. 110

Fig. 5.17. (a) I_{ON} (solid symbols) at gate overdrive (V_{GS} - V_T) of 1 V, and I_{OFF} (open symbols) at (V_{GS} - V_T) of -0.5 V at V_D of 0.6 V and (b) peak $G_{M,int}$ at V_D of 0.6 V are compared for samples annealed at a fixed temperature of 600 °C for different durations. As in the case of lower annealing temperature, a shorter annealing time leads to a lower thermal budget, which gives better gate stack quality and therefore better device performance...111

Fig. 5.18. Box plots showing the statistical distribution of S for devices with different dopant activation conditions. Comparison is made between samples with different (a) annealing temperatures and (b) annealing times. A higher thermal budget for dopant activation results in degradation of the gate stack, which leads to higher S. This can be avoided by using a gate-last process scheme...............................111

List of Symbols

a, c	Lattice parameters
A^*	Richardson's constant
A_{CHIP}	Area of semiconductor chip
A_{D}	Area of diode
A_{eff}	Effective contact area
A_{G}	Gate area
A_{pole}	Magnitude of the pole
C_{DIF}	Inner fringing capacitances at the drain side
C_{DOF}	Outer fringing capacitances at the drain side
C_{ellips}	Fitting parameter in the Drude model
C_{GD}	Gate-to-drain capacitance
$C_{\mathrm{GD,inv}}$	Inversion capacitance at the drain side
C_{GG}	Total gate capacitance
C_{GS}	Gate-to-source capacitance
$C_{\mathrm{GS,inv}}$	Inversion capacitance at the source side
C_{InGaAs}	InGaAs capacitance
C_{OF}	Parasitic outer fringing capacitances
C_{OX}	Gate oxide capacitance
C_{OUT}	Output capacitance per transistor
C_{SIF}	Inner fringing capacitances at the source side
C_{SOF}	Outer fringing capacitances at the source side
d	Thickness of the S/D
D_{it}	Interface trap density
d_{SP}	TLM contact spacing

E_C	Conduction band energy
E_G	Energy band gap
E_F	Fermi energy
E_P	Plasmon energy
E_{PH}	Photon energy
E_{pole}	Pole energy
E_V	Valence band energy
f	Clock frequency
G_D	Drain transconductance
G_M	Transconductance
$G_{M,ext}$	Extrinsic transconductance
$G_{M,int}$	Intrinsic transconductance
I	Current
I_D	Drain current
$I_{D,Sat}$	Saturation drain current
I_G	Gate leakage current
I_{LEAK}	Leakage current of the transistor
I_{OFF}	Off-state current
I_{ON}	On-state current
I_S	Diode saturation current
I_{SS}	Source-to-drain sub-surface leakage
I_{S2D}	Direct source-to-drain leakage
K	Boltzmann constant
k	Dimensionless scaling factor
k_{d1}, k_{d2}, and k_{d3}	Equilibrium rate constants
L_C	Contact length

L_G	Gate length
L_{Ni}	Nickel contact pad length
L_{SDE}	Source-drain extension length
$L_{S/D}$	Lateral diffused length of the deep source-drain region
L_T	Transfer length
$m*$	Effective mass of carriers
m_e*	Electron effective mass
n	Electron carrier concentration
N	Doping concentration
N_A	P-type doping concentration
N_D	N-type doping concentration
$N_{S,Source}$	Carrier concentration near the source edge
N_T	Total number of transistors in a chip
p	Hole carrier concentration
P_{CHIP}	Power consumption per chip
P_D	Dynamic power
p_{O2}	Partial pressure of O_2 in the solution
P_S	Static power
P_{SP}	Probe spacing from the channel
q	Elementary charge
Q_G	Gate charge
Q_{inv}	Inversion charge density
r	Etch rate
r_C	Backscattering coefficient
r_{Ni}	Etch rate of Nickel
$r_{Ni\text{-}InGaAs}$	Etch rate of Ni-InGaAs

R_{C}	Contact resistance
$R_{C,eff}$	Effective contact resistance
R_{CH}	Channel resistance
R_{DRAIN}	Drain resistance
R_{eMSD}	Resistance of the *e*MSD regions
R_{METAL}	Metal contact resistance
R_{S}	Sheet resistance
R_{SD}	Source-drain series resistance
$R_{S/D}$	Deep S/D resistance
R_{SDE}	Source-drain extension resistance
$R_{S,eMSD}$	Sheet resistance of the *e*MSD
R_{SOURCE}	Source resistance
R_{T}	Total resistance
S	Subthreshold swing
T	Temperature
t	Time
T_{anneal}	Annealing temperature
t_{anneal}	Annealing time
t_{delay}	Time delay between $P_2S_5/(NH_4)_2S_x$ treatment and deposition of the SiO_2 capping layer
t_{f}	Thickness of film
$t_{f,Ni}$	Thickness of nickel film
$t_{f,Ni-InGaAs}$	Thickness of Ni-InGaAs film
T_{InGaAs}	Thickness of InGaAs
t_{METAL}	Metal thickness
t_{Ni}	Nickel thickness
$T_{n-InGaAs}$	Thickness of n-type doped InGaAs

T_{OX}	Oxide thickness
T_P	Propagation delay of a CMOS inverter
V	Voltage
V_D	Drain voltage
V_{DD}	Supply voltage
V_{GS}	Gate voltage
v_{inj}	Injection velocity
V_T	Threshold voltage
$V_{T,lin}$	Linear threshold voltage
$V_{T,Sat}$	Saturation threshold voltage
W_C	Contact width
W_G	Gate width
W_{Ni}	Nickel contact pad width
x	Indium composition
X_{JSDE}	Junction depth of the source-drain extension
$X_{JS/D}$	Junction depth of the deep source-drain
α	Dimensionless scaling factor
ε_0	Permittivity of free space
ε_S	Permittivity of the semiconductor
κ	Relative permittivity
μ_e	Electron mobility
μ_{EFF}	Effective channel mobility
μ_h	Hole mobility
$\hbar$	Planck’s constant
ρ	Bulk resistivity
ρ_C	Contact resistivity

ρ_{InGaAs}	Resistivity of InGaAs
$\rho_{n\text{-}InGaAs}$	Resistivity of n-type doped InGaAs
ρ_{Ni}	Resistivity of nickel
$\rho_{Ni\text{-}InGaAs}$	Resistivity of Ni-InGaAs
ρ_{NiPt}	Resistivity of nickel platinum
$\rho_{NiPt\text{-}InGaAs}$	Resistivity of NiPt-InGaAs
ρ_{SDE}	Source-drain extension region resistivity
$\rho_{S/D}$	Resistivity of the deep source-drain region
ϕ_B	Effective barrier height
$\phi_{B,N}$	Effective electron barrier height
$\phi_{B,P}$	Effective hole barrier height
$\phi_{B,P,InAlAs}$	Schottky barrier height of Ni-InAlAs on p-InAlAs
$\phi_{B,P,InGaAs}$	Schottky barrier height of Ni-InAlAs on p-InGaAs
η	Diode ideality factor
μ_{max}	Maximum mobility
μ_{min}	Minimum mobility
τ_e	Carrier relaxation time
$<\varepsilon_2>$	Imaginary part of the pseudo dielectric function

Chapter 1

Introduction

1.1 Background

Modern complementary metal-oxide-semiconductor (CMOS) logic circuits are designed using n-channel and p-channel metal-oxide-semiconductor field-effect transistors, henceforth denoted as N-MOSFETs and P-MOSFETs, respectively. CMOS technology is predominantly silicon (Si) based as the Si semiconductor material is readily available and cheap. Since the early 1970s, the continuous success of semiconductor companies has heavily depended on the 'down-scaling' of the metal-oxide-semiconductor field-effect transistor (MOSFET). Over the years, transistor dimensions have been scaled down to realize high-performance MOSFETs with high ON-state current (I_{ON}). In addition, dimension scaling increases the packing density (number of transistors per unit area), which in turn reduces cost per transistor. Furthermore, down-scaling the supply voltage (V_{DD}) reduces power consumption in circuits, which in turn reduces packaging and cooling costs.

Intel's latest processor, code-named 'Ivy Bridge' at the 22-nm technology node, packs about 1.4 billion transistors in a 160 mm^2 area [1]. A transistor behaves like a switch in logic circuits. It is expected to switch at extremely fast speeds while consuming very low energy. Intel's Ivy Bridge runs 4000 times faster and consumes 5000 times lesser energy compared to its first processor, the '4004' [2]. Furthermore, the cost per transistor has reduced by a factor of about 50,000 in the last 40 years [2].

Down-scaling of V_{DD} is one of the main challenges currently faced by Si CMOS technology [3]. As mobility enhancement in Si MOSFETs reaches its limits, further scaling of V_{DD} compromises the switching speed of the transistor. Therefore, new materials, processes, and device architectures have to be developed to overcome the physical scaling limits of conventional Si MOSFETs.

1.2 Scaling Challenges of Transistors

The scaling of transistors in CMOS technology has followed Moore's law, which states that the number of transistors in integrated circuits (ICs) doubles roughly every two years [4]. However, it is essential that the circuit performance and power consumption of the chip do not deteriorate as the device dimensions are scaled down. In 1970, Dennard *et al.* [5] proposed a scaling methodology to enhance integrated circuit performance without increasing power consumption (Table 1.1). Power consumption per chip (P_{CHIP}) can be expressed as follows [6]:

$$P_{CHIP} \propto f \cdot C_{OUT} \cdot V_{DD}^2 \cdot N_T + V_{DD} \cdot I_{LEAK} \cdot N_T, \quad (1.1)$$

where f is the frequency of signal change that scales by a factor of $1/k$, C_{OUT} is the total output capacitance per transistor which scales by a factor of k, N_T is the total number of transistors ($N_T \propto \alpha/k^2$), and I_{LEAK} is the leakage current of the transistor. As I_{LEAK} is negligible in devices with large gate length (L_G), P_{CHIP} is dominated by the first term in Equation (1.1). This means that if the chip area (A_{CHIP}) is constant (i.e. $\alpha = 1$), then $N_T \propto 1/k^2$ and P_{CHIP} remains constant. However, in recent years, power consumption has not been reduced adequately through V_{DD} scaling and P_{CHIP} has increased by ~10^5 times [6]. Furthermore, I_{LEAK} becomes significant as L_G is scaled down aggressively. The following subsections describe the background information on the various effects that limit transistor scaling.

Table 1.1. Scaling trends to improve integrated circuit performance [5].

Circuit or device parameters	Symbol	Scaling factor
Gate length	L_G	k
Gate width	W_G	k
Gate oxide thickness	T_{OX}	k
Supply voltage	V_{DD}	k
Drive current in saturation regime	$I_{D,Sat}$	k
$I_{D,Sat}$ per unit W_G	$I_{D,Sat}$ /μm	1
Gate oxide capacitance	C_{OX}	k
Propagation delay	T_P	k
Chip area	A_{CHIP}	α
Number of transistors	N_T	α/k^2
Power consumption per chip	P_{CHIP}	α

* α and k are dimensionless scaling factors.

1.2.1 Leakage currents

Quantum-mechanical tunneling of carriers through energy barriers [i.e. channel-gate dielectric barrier, source/drain (S/D)-to-substrate barrier, and S/D-to-channel barrier] in highly scaled MOSFETs results in leakage currents, which in turn increases power dissipation. These leakage currents are: (i) gate leakage (I_G) by tunneling mechanism, (ii) source-to-drain sub-surface leakage (I_{SS}), and (iii) direct source-to-drain leakage (I_{S2D}) by tunneling of carriers through the channel barrier.

In Si CMOS technology, as the device dimensions are scaled down, the silicon dioxide (SiO_2) gate dielectric thickness (T_{OX}) was reduced to achieve good electrostatic gate control over the channel region. Reducing T_{OX} leads to a higher gate oxide capacitance (C_{OX}) which can be expressed in the following equation:

$$C_{OX} = \frac{\varepsilon_0 \cdot \kappa \cdot A_G}{T_{OX}}, \tag{1.2}$$

where ε_0 is the permittivity of free space, κ is the relative permittivity of the dielectric, and A_G ($L_G \cdot W_G$) is the area of the gate. However, the decrease in T_{OX} results in an increase in I_G due to the tunneling of electrons or holes from the channel to the gate (through the gate dielectric) for N-MOSFETs and P-MOSFETs, respectively. A higher C_{OX} can also be achieved by increasing κ of the gate dielectric [7], which can be achieved by using Si oxynitride composites [8]-[11] or high-κ dielectrics [12]-[26].

A second significant source of leakage is the I_{SS}. I_{SS} is a result of poor gate control of the electrostatic potential at regions between the source and the drain that are far away from the dielectric-channel interface. As L_G is scaled down, the drain voltage (V_D) pulls down the potential barrier near the source region resulting in I_{SS} [27]. 3D structures such as fin field effect transistors (FinFETs) or nanowire transistors have been proposed to minimize I_{SS} [28]-[41]. The wrap around gate architectures in these devices provide excellent electrostatic gate control even at the sub-surface regions, thus, reducing I_{SS}.

The third leakage current component is I_{S2D}. This component becomes significant as the L_G becomes less than 10 nm (at room temperature) [42]. This extra tunneling current tends to be smaller than the other leakage components at such device dimensions [3].

1.2.2 Random dopant fluctuation

In the current Si CMOS technology, doping concentration (N) in regions such as the channel or S/D of MOSFETs, are well controlled by the conventional beam-line ion implantation and annealing process. However, this process cannot accurately control the position of the dopants, which results in spatial fluctuations in the local doping concentration. This leads to a device-to-device variation in the threshold voltage (V_T) of the MOSFETs. As L_G is scaled down to sub-22 nm, the V_T is eventually controlled by 100 dopant atoms or less, which makes it difficult to keep the V_T variation low.

This effect can be reduced by moving the dopants away from the channel surface using retrograde doping [43]-[46]. Another approach is to use an undoped channel and tuning the V_T by varying the work function of the metal gate [47]-[49] or using multiple-gate architectures [50]-[52].

1.2.3 Power constrained scaling

There are two main types of power dissipation in a CMOS circuit: (a) dynamic and (b) static. In CMOS technology, dynamic power (P_D) is a result of the switching action during logic operations. P_D is a strong function of V_{DD} as shown below [53]:

$$P_{D} \propto C_{OUT} \cdot V_{DD}^{2} \cdot f \ . \tag{1.3}$$

P_D can be minimized by reducing the V_{DD}. The other component is the static power (P_S), which manifests during the holding of the logic states between the switching operations [53]:

$$P_{S} \propto I_{LEAK} \cdot V_{DD} \ . \tag{1.4}$$

I_{LEAK} is a combination of the different leakage currents described in Section 1.2.1. P_{S} is unavoidable and becomes a dominant factor as the device dimensions are scaled down. Decreasing I_{LEAK} by the various methods explained earlier in Section 1.2.1, reduces P_{S}.

1.3 Motivation for Using III-V Materials

The carrier transport in transistors with extremely small L_{G} is typically in the quasi-ballistic or ballistic regime. The saturation drain current ($I_{\text{D,Sat}}$) of such a transistor is limited by the thermal injection velocity (v_{inj}) and is given by [54]-[55]:

$$I_{\text{D,Sat}} = q \cdot N_{\text{S,Source}} \cdot v_{\text{inj}} \cdot \left(\frac{1 - r_{\text{C}}}{1 + r_{\text{C}}} \right) = C_{\text{OX}} \cdot W_{\text{G}} \cdot v_{\text{inj}} \cdot \left(\frac{1 - r_{\text{C}}}{1 + r_{\text{C}}} \right) \cdot \left(V_{\text{GS}} - V_{\text{T}} \right), \qquad (1.5)$$

where q is the elementary charge (1.6×10^{-19} C), $N_{\text{S,Source}}$ is the carrier concentration near the source edge, r_{C} is the backscattering coefficient which is a measure of the number of carriers that are scattered back to the source, and V_{GS} is the gate voltage. The injection velocity and $N_{\text{S,Source}}$ are a function of the effective mass of the charge carriers in the channel material [56]-[57]. Materials with a small effective mass along the transport direction (high v_{inj}) and a large effective mass [i.e. high density of states (DOS)] in the transverse direction are desired to achieve high $I_{\text{D,Sat}}$ in MOSFETs.

Since the last decade, strain techniques have been employed in Si MOSFET to boost its channel mobility [58]-[68] and achieve high $I_{\text{D,Sat}}$. However, Si technology is reaching its limits in terms of mobility enhancement using strain engineering. One method to attain high channel mobility, and therefore $I_{\text{D,Sat}}$ in MOSFETs, is to replace the Si channel with high-mobility materials that have high intrinsic carrier mobilities and low effective mass for the carriers. III-V compound semiconductors are promising

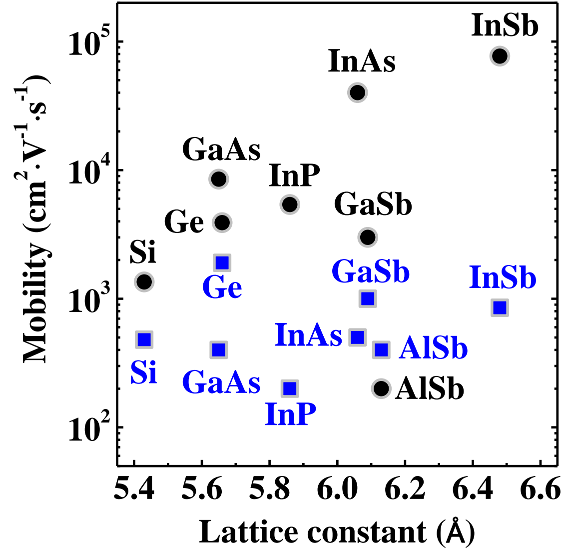


Fig. 1.1. Plot of the electron (black circles) and hole mobilities (blue squares) at 300 K, for Si, germanium (Ge) and various III-V compound semiconductors.

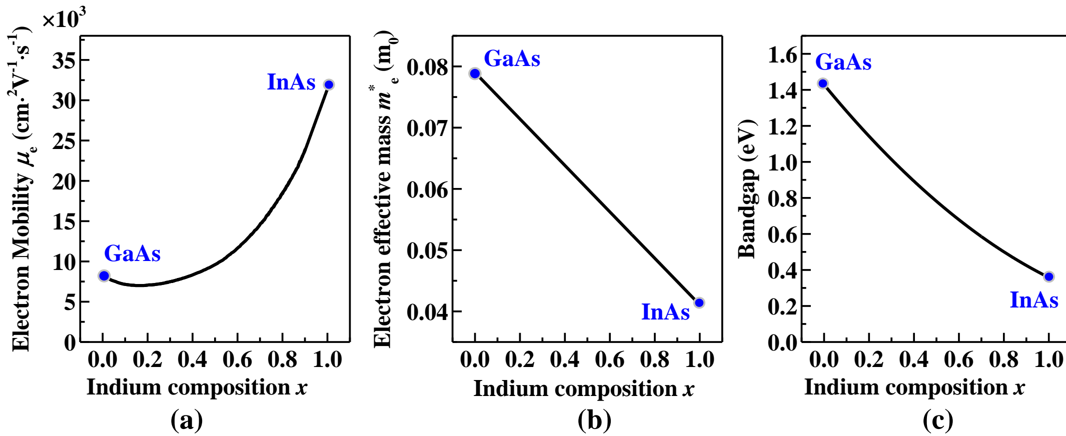


Fig. 1.2. (a) Electron mobility (μ_e) versus composition x for $In_xGa_{1-x}As$. μ_e increases with higher indium composition. (b) Electron effective mass m_e* versus composition x for $In_xGa_{1-x}As$. m_e* decreases with increasing indium composition, leading to higher μ_e in (a). (c) Band gap E_G versus composition x for $In_xGa_{1-x}As$. $In_xGa_{1-x}As$ offers a wide range of E_G from 0.36 eV to 1.42 eV.

candidates for potential use as channel materials in N-MOSFETs, due to their high electron mobility (μ_e) [Fig. 1.1] [69].

In addition, III-V MOSFETs can be fabricated using the conventional "top-down" lithography processes currently used in Si CMOS. Furthermore, III-V compound semiconductors provide a wide selection of band gaps and materials. Hence, III-V

heterostructures allow greater flexibility in band gap engineering and device design for both high-performance and low-power applications, compared to Si-based heterostructures [such as Si/silicon germanium (SiGe)].

Due to these advantages, III-V materials have been studied extensively (including various arsenides and antimonides) [70]-[95], for potential application in CMOS technology. Indium gallium arsenide (InGaAs) is a promising alternative for possible use as the channel material of N-MOSFETs [95]. The μ_e of InGaAs, as a function of the indium composition (x), is plotted in Fig. 1.2 (a) [96]. μ_e increases with increasing x due to a reduction in the electron effective mass (m_e*) [97], as shown in Fig. 1.2 (b). The minima observed in Fig 1.2 (a), in the region of x ~ 0.1 to 0.2, can be attributed to alloy scattering [96]. In addition, InGaAs offers a wide range of band gaps from 0.36 eV [indium arsenide (InAs) with $x = 1$] to 1.42 eV [gallium arsenide (GaAs) with $x = 0$] as illustrated in Fig. 1.2 (c) [98].

According to the International Technology Roadmap for Semiconductors (ITRS), InGaAs could be used in CMOS technology as early as 2018 [99]. Fig 1.3 illustrates $I_{D,Sat}$ versus V_{GS} of an InGaAs N-MOSFET and a Si N-MOSFET. Although the DOS in InGaAs is lower than that in Si, the higher v_{inj} of InGaAs results in a higher I_{ON} at the same off-current (I_{OFF}) [at a fixed gate overdrive (V_{GS} - V_T)] compared to the Si N-MOSFET [69]. The high I_{ON} in turn reduces the propagation delay (T_P) of the CMOS inverter [100]:

$$T_P \approx \frac{C_L \cdot V_{DD}}{4} \cdot \left(\frac{1}{I_{ON,N}} + \frac{1}{I_{ON,P}} \right), \tag{1.6}$$

where C_L is the total load capacitance of the CMOS inverter. $I_{ON,N}$ and $I_{ON,P}$ are the ON-state current of the N-MOSFET and the P-MOSFET, respectively. Furthermore, by replacing the channel of the N-MOSFET with InGaAs, the supply voltage can be

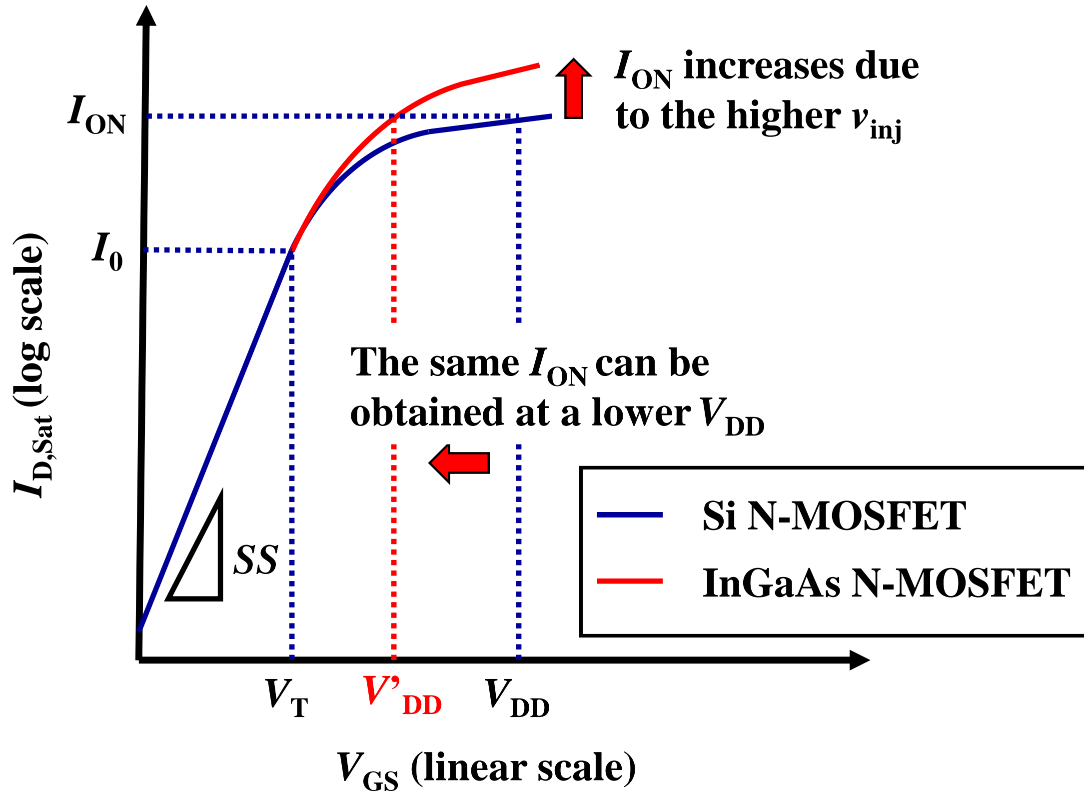


Fig. 1.3. Comparison of $I_{D,Sat}$-V_{GS} between a Si N-MOSFET (blue solid curve) and an InGaAs N-MOSFET (red solid curve). A higher I_{ON} can be achieved for the InGaAs N-MOSFET at the same gate overdrive (V_{GS}-V_T). Furthermore, using an InGaAs N-MOSFET allows the down-scaling of V_{DD} without compromising I_{ON}. The InGaAs and Si N-MOSFETs are assumed to have the same subthreshold swing (S).

reduced (V'_{DD}) to maintain the same I_{ON} and I_{OFF}. Since these devices have a low P_D (at a fixed switching frequency) [Equation (1.3)], they can be used in low operating power (LOP) applications.

1.4 Challenges for III-V CMOS Logic

Several challenges need to be overcome before Si can be replaced with a new channel material at future technology nodes. If III-V materials are introduced in the sub-10 nm technology nodes, they will have to outperform the Si alternative. In addition, the III-V transistors must be realized in a cost-efficient manner and should

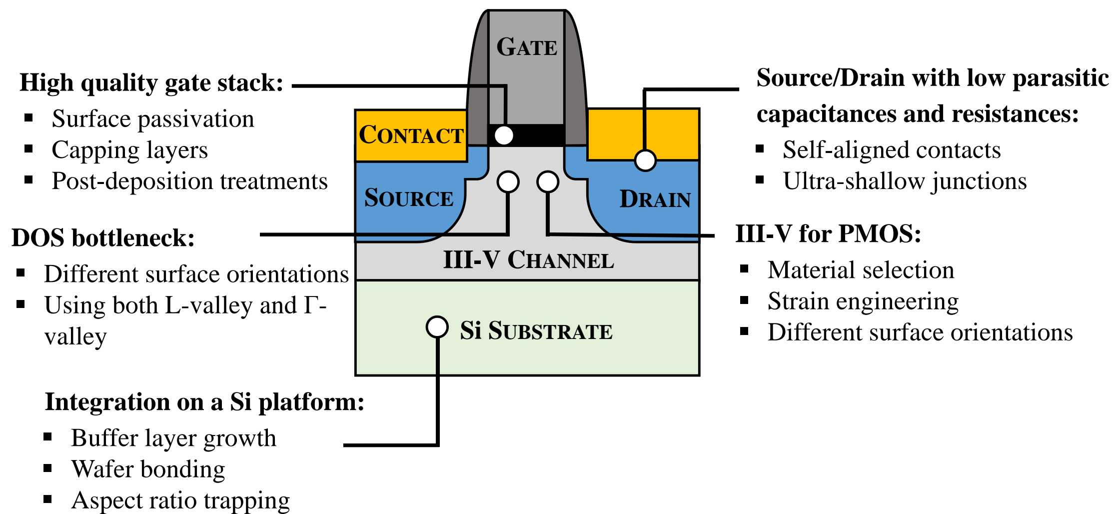


Fig. 1.4. Schematic illustrating the key technical challenges faced in the realization and integration of high mobility III-V channel MOSFET on Si substrates for future logic applications.

be scalable over a few technology nodes. Some of the problems that need to be addressed include: (i) formation of a high-quality gate stack (with minimal trap density), (ii) achieving low gate-to-drain capacitances (C_{GD}) and S/D resistances (R_{SD}), (iii) realizing high-performance III-V P-MOSFETs, (iv) integration of III-V transistors on a Si platform, and (v) "DOS bottleneck". Fig. 1.4 illustrates these key challenges. These technical challenges are described in the following subsections.

1.4.1 Realization of high-quality gate stack

The gate stack of a MOSFET typically consists of a metal gate and a high-κ dielectric layer. The gate stack is an important part of a transistor as it controls its switching behavior. A high-quality interface with minimal defects between the gate-dielectric and the channel is necessary for the gate to function properly. Hence, the dielectric must be free of trapped charges and other defects, have a smooth interface with minimal interfacial imperfections, and have high thermal stability. The native oxides of III-V have very poor electrical properties in comparison with that of Si. A high interface state trap density (D_{it}) between the gate dielectric, and the channel

interface results in 'Fermi level pinning' [101]. This phenomenon, which is common in III-V materials, inhibits the ability of the gate to modulate the surface potential of the channel [101]. Moreover, the high surface roughness at the dielectric channel interface, D_{it}, and the defects or traps in the gate dielectric severely degrades the mobility of carriers in the channel. The mobility degradation can be attributed to mechanisms such as phonon, coulomb, and surface roughness scattering [102]-[103]. Therefore, a high-quality dielectric-channel interface is paramount in fully utilizing the advantages of III-V materials over Si in terms of mobility and v_{inj}.

In 2003, GaAs MOSFET with aluminum oxide (Al_2O_3) deposited using atomic layer deposition (ALD) was demonstrated [104]. During ALD, native oxide on the GaAs surface was removed in the early stages of deposition [105]-[107], which was followed by the immediate deposition of the high-κ dielectric (i.e. Al_2O_3). Subsequently, this ALD process was demonstrated on InGaAs [108], InAs [109], and indium phosphide (InP) [110] MOSFETs with promising results. Several techniques to passivate III-V surfaces have been investigated to improve the quality of gate stacks deposited on III-V materials in order to reduce the amount and influence of dielectric and interface defects. These include (i) surface cleaning prior to deposition [111]-[112], (ii) inserting interfacial layers between the dielectric and the channel [113]-[114], (iii) post-deposition treatments [111], [115], (iv) alternate high-κ dielectrics [116]-[117], (v) changing the surface orientation of the III-V material [118]-[120], and (vi) using a buried-channel device structure [121]-[122]. The best results have been obtained in an InGaAs buried-channel structure, where the gate stack consists of an InP capping layer, and an ALD $TaSiO_x$ dielectric [121]. The performance of this InGaAs N-MOSFET exceeded that of the state-of-the-art Si N-MOSFET [69].

1.4.2 Integration on a Si platform

The integration of III-V transistors on a Si substrate is a key challenge that needs to be addressed. Integration is essential as it decreases the production cost due to the existing mature Si processing technology. Various integration techniques have been proposed including (a) buffer layer growth [73], [123]-[124], (b) III-V-on-insulator (III-V-OI) [125]-[127], and (c) aspect ratio trapping (ART) [128]-[133].

Direct growth of III-V materials on Si is extremely challenging due to their large lattice mismatch. The abrupt lattice transition can be resolved by employing a buffer layer such as $In_xAl_{1-x}As$ or $Al_xGa_{1-x}As$, where the lattice constant is gradually increased from that of Si to the lattice of the desired III-V material. The misfit dislocations and defects are confined in the buffer layer, allowing the growth of defect-free III-V layers that are fully relaxed or slightly strained. Successful integration of $In_{0.7}Ga_{0.3}As$ and $In_{0.53}Ga_{0.47}As$ MOSFETs have been demonstrated on Si by molecular beam epitaxy (MBE) [121] and metal organic chemical vapor deposition (MOCVD) [124] techniques, respectively. However, the buffer layer thickness which is typically around 1 μm has to be drastically reduced to ensure the feasibility of this approach. A thin buffer layer is essential because it requires shorter growth time. A shorter growth time increases the throughput during the fabrication process, which in turn reduces cost of production.

Another way to integrate III-V on Si is by the layer transfer of the desired III-V material onto a Si substrate covered by a dielectric such as SiO_2 or Al_2O_3, which is similar to the well-established silicon-on-insulator (SOI) technology. The desired III-V layer grown on a donor wafer is transferred to an oxide-covered Si substrate by direct wafer bonding and etch back process [125], or by epitaxial layer transfer [126]-[127]. Similar to SOI, the III-V-OI layer can be either relaxed or strained [134].

However, the main challenge for this approach is that it requires expensive sacrificial donor wafers. For example, to produce III-V-OI on a 12 inch Si wafer, the III-V layers need to be grown on a 12 inch donor wafer, which is not only challenging, but also expensive.

Recently, a promising integration approach called ART was introduced which allows direct growth of III-V material on Si without the need of a thick buffer layer [131]. In this technique, the III-V materials are grown in high-aspect-ratio SiO_2 trenches on Si. The dislocations formed during the growth of the III-V materials on Si (induced by large lattice mismatch) are terminated on the SiO_2 sidewalls. Hence, the material that grows out of the trench is free of dislocations and can be used for device fabrication. Ge, GaAs and InP films have been grown using ART [128]-[133]. ART combined with epitaxial lateral overgrowth (ELO) produces uniform films with low defect density [131]. GaAs MOSFETs have been demonstrated using ART-ELO [128].

Although there are several promising integration approaches, detailed studies on the defect density and solutions to minimize these defects have not been explored. Furthermore, achieving both N-MOSFETs and P-MOSFETs with different channel materials and lattice constants on a same planar surface will be extremely challenging. These critical issues needs to be addressed in the near future.

1.4.3 III-V P-MOSFETs

There is a large imbalance between μ_e and hole mobility (μ_h) in III-V materials, as seen in Fig. 1.1. There is not a single material with both μ_e and μ_h above 5000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and 1500 $cm^2 \cdot V^{-1} \cdot s^{-1}$, respectively. In addition, μ_h is significantly lower than μ_e, which results in a lower I_{ON} for the P-MOSFET compared to the N-MOSFET. Therefore, a future where III-V N-MOSFETs and P-MOSFETs, made of different materials with different lattice constants, seems inevitable. A μ_h of ~1500 $cm^2 \cdot V^{-1} \cdot s^{-1}$

in indium gallium antimonide (InGaSb) [135], ~ 1300 $cm^2 \cdot V^{-1} \cdot s^{-1}$ in gallium antimonide (GaSb) [136], and ~1,200 $cm^2 \cdot V^{-1} \cdot s^{-1}$ in indium antimonide (InSb) [137] have been achieved. These are now the most promising candidates for channel materials in III-V P-MOSFETs. Uniaxial strain has been used in the channel of Si P-MOSFETs to boost their performance to match that of the N-MOSFET [138]. This approach can be explored for III-V semiconductor materials [139]-[141]. III-V P-MOSFETs using GaAs [142], InGaAs [143], GaSb [144], and InGaSb [144] have been demonstrated. However, their performance still lags behind that of the III-V N-MOSFETs. Currently, Ge P-MOSFET technology [145], which is more mature, has the advantage over III-V P-MOSFETs.

1.4.4 Source/Drain regions with low C_{GD} and R_{SD}

Low C_{GD} and R_{SD} are vital to achieve transistors with high I_{ON} and short T_P. C_{GD} is slightly higher due to the higher permittivity of the III-V materials over Si (about 10 % higher for $In_{0.53}Ga_{0.47}As$). Moreover, the device structure has a significant impact on C_{GD}. Parasitic outer fringing capacitances (C_{OF}), associated with the gate sidewalls, become dominant as the devices scale down [138]. For instance, introducing raised S/D architectures increases C_{OF}, as the proximity between the S/D and the gate sidewall reduces. Similarly, high R_{SD} is a significant concern at future CMOS technology nodes. The channel resistance (R_{CH}) in III-V MOSFETs decreases significantly as the L_G scales down aggressively. Therefore, the I_{ON} is eventually limited by R_{SD}. R_{SD} becomes more critical in advanced device structures such as FinFETs [74]-[75] and nanowire transistors [146]-[149].

A self-aligned S/D architecture can be used to reduce R_{SD}. In this scheme, the contacts are formed without an optical alignment to the gate. Self-alignment reduces

the distance between the gate and the contact, thus reducing R_{SD}. Self-aligned contacts have been successfully demonstrated on III-V HEMTs with promising results [150]-[151]. The resistivity of the S/D regions has to be small to reduce R_{SD}. Compared to Si MOSFETs, a lower R_{SD} can be achieved with InGaAs as the S/D material. Although the active n-type doping that can be achieved in InGaAs (mid-10^{19} cm^{-3}) is lower than that of Si (mid-10^{20} cm^{-3}), a lower resistivity can be attained due to the much higher μ_e [> 1000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ (at room temperature)] [152] in InGaAs compared to Si [< 100 $cm^2 \cdot V^{-1} \cdot s^{-1}$ (at room temperature)].

Furthermore, a very low Ohmic contact resistance (R_C) is required between the contact metal and the highly n-type doped S/D regions. A low contact resistivity (ρ_C) of ~1×10^{-8} $\Omega \cdot cm^2$ on n-type $In_{0.53}Ga_{0.47}As$ has been shown using *in situ* deposited molybdenum (Mo) contacts [153]-[154]. Hence, Mo is a good candidate for non-self-aligned contacts in InGaAs N-MOSFETs. However, for self-aligned contacts on InGaAs, the lowest ρ_c was obtained for nickel-indium gallium arsenide (Ni-InGaAs) metallic contacts (~1×10^{-6} $\Omega \cdot cm^2$) [155]-[156]. The ρ_c of Ni-InGaAs needs to be reduced further to compete with the *in situ* Mo contacts.

1.4.5 Density of States (DOS) Bottleneck

As mentioned in Section 1.3, when III-V channel materials are introduced at future technology nodes, MOSFETs will be operating in the quasi-ballistic or ballistic regime. At such extremely scaled device dimensions, $I_{D,Sat}$ will depend on v_{inj} and DOS [Equation 1.5]. Although the small transport mass of the charge carriers in III-V materials leads to a high v_{inj}, they have low DOS in the Γ-valley. The low DOS will decrease the inversion charge (Q_{inv}) in the channel of a MOSFET (at a given V_{GS}), which will reduce $I_{D,Sat}$. This is commonly known as the "DOS bottleneck" [157].

The key to realizing high-performance III-V MOSFETs at sub-10 nm technology nodes is to increase the DOS while maintaining a high-enough v_{inj}. The DOS bottleneck can be overcome by changing the surface orientations of the III-V materials and using the L-valley along with the Γ-valley [158]-[162].

1.5 Objective and Organization of Thesis

III-V materials are projected to replace Si as the channel in sub-10 nm technology generations and beyond. At such small dimensions, key changes in the fundamental materials, processes, and device structures are required to achieve the important device performance goals. The objective of this thesis is to address some of the issues faced by the current III-V device technology. The research in this thesis focuses on solutions for contact and doping challenges in the S/D of InGaAs N-MOSFETs.

Chapter 2 presents a literature review on the basic concepts and components of S/D series resistance in an InGaAs N-MOSFET, background information on the contact technologies used for III-V materials and the current status of research on self-aligned contact technology for InGaAs N-MOSFETs.

In Chapter 3, a selective etching process is developed to ascertain the feasibility of using self-aligned metallic contacts in an InGaAs N-MOSFET fabrication process. This Chapter explores the selective etching of Ni over Ni-InGaAs and NiPt over NiPt-InGaAs. The etch rates and selectivities of these metals and metallic alloys, in various wet etch chemistries, is extracted using sheet resistance method, transmission electron microscopy images and surface profiler measurements.

In Chapter 4, a novel InGaAs n-channel ultra-thin body FET with an embedded metal S/D (*e*MSD) design is demonstrated. The *e*MSD architecture helps to reduce R_{SD}

without increasing process complexity or compromising C_{GD}. The feasibility of using the *e*MSD design at future technology nodes is evaluated using technology computer aided (TCAD) simulations.

In Chapter 5, sulfur monolayer doping (SMLD) using $P_2S_5/(NH_4)_2S_x$ solution is studied for possible use in the formation of S/D extensions of InGaAs N-MOSFETs. This technique is capable of achieving abrupt, ultra-shallow, and damage-free junctions with high doping concentrations. The SMLD samples are characterized using micro-4-point probe measurements, transmission line model structures, and secondary ion mass spectrometry analysis. Infrared spectroscopic ellipsometry is used to extract electrical resistivities, carrier relaxation times, and active carrier concentration of the shallow and highly n-type doped InGaAs films. This Chapter demonstrates the SMLD process on planar InGaAs N-MOSFETs, and investigates the effect of the dopant activation conditions on device performance.

Chapter 6 documents the contributions of this thesis and possible directions for future work.

Chapter 2

Source/Drain Series Resistance in InGaAs N-MOSFETs

2.1 Introduction

This Chapter documents a review of recent work in the literature, so as to provide basic understanding of recent technological developments that are related to this thesis research. Sections 2.2 and 2.3 of this Chapter describe the concept of source/drain (S/D) resistances (R_{SD}) and its various components in an InGaAs n-channel metal-oxide-semiconductor field effect transistor (N-MOSFET). Subsequently, a history of S/D engineering in III-V MOSFETs is presented in Section 2.5. In addition, self-aligned S/D contact technology for InGaAs N-MOSFETs is introduced in Section 2.4, with emphasis on nickel-indium gallium arsenide (denoted as Ni-InGaAs) based metallic contacts.

2.2 Concept of Source/Drain Series Resistance

As mentioned in Chapter 1, in a transistor, high ON-state current (I_{ON}) can be achieved by minimizing the total resistance (R_T). R_T (in the linear regime) is the series combination of channel resistance (R_{CH}) and R_{SD}. R_T can be expressed as [163]:

$$R_T = R_{CH} + R_{SD} \ . \tag{2.1}$$

Fig. 2.1 (a) shows R_T between the source and drain terminals of an InGaAs N-MOSFET. As the gate length (L_G) is scaled down, R_{CH} becomes smaller and R_T

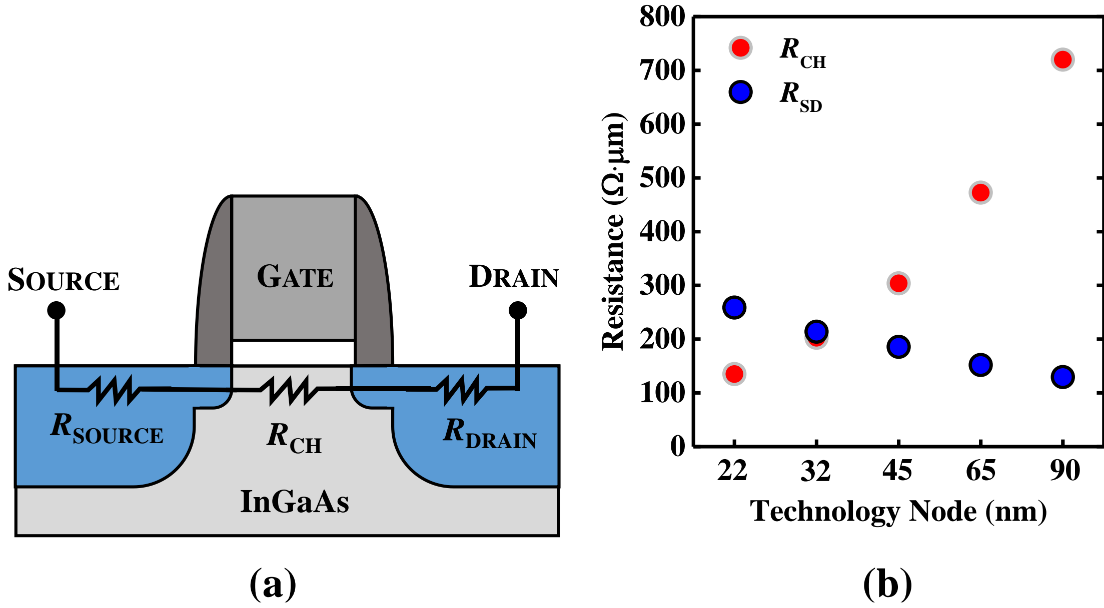


Fig. 2.1. (a) Schematic illustrating the different resistance components in an InGaAs N-MOSFET (in the linear regime). The total resistance R_T of the transistor is the summation of the channel resistance R_{CH}, and the parasitic resistance $R_{SD} = R_{SOURCE} + R_{DRAIN}$. (b) The scaling trend for R_{CH} and R_{SD} in Si N-MOSFETs (taken from Ref. [164]). As R_{CH} reduces with gate length, R_T becomes dominated by R_{SD}. Therefore, R_{SD} needs to be minimized to achieve a high I_{ON} in the transistor.

is dominated by R_{SD} [163]. Moreover, R_{SD} becomes comparable to R_{CH} at the 22 nm technology node [164] [Fig. 2.1 (b)]. Therefore, beyond the 22 nm technology node, R_{SD} becomes a bottleneck for improving device performance.

2.3 Elements of Source/Drain Resistance

R_{SD} of an InGaAs N-MOSFET can be mainly divided into three separate resistance components: (a) S/D extension (SDE) resistance (R_{SDE}), (b) deep S/D resistance ($R_{S/D}$), and (c) contact resistance (R_C) at the contact-semiconductor interface. Fig. 2.2 highlights these components. Assuming an ideal box-like doping profile, R_{SDE} and $R_{S/D}$ can be expressed as [165]:

$$R_{SDE} = \frac{\rho_{SDE} \cdot L_{SDE}}{W_G \cdot X_{JSDE}}, \tag{2.2}$$

and $$R_{\mathrm{S/D}} = \frac{\rho_{\mathrm{S/D}} \cdot L_{\mathrm{S/D}}}{W_{\mathrm{G}} \cdot \left(X_{\mathrm{JS/D}} - T_{\mathrm{InGaAs}} \right)}, \tag{2.3}$$

where ρ_{SDE} is the extension region resistivity, L_{SDE} is the extension length, W_{G} is the gate width, X_{JSDE} is the junction depth of the SDE, $\rho_{\mathrm{S/D}}$ is the resistivity of the deep S/D region, $L_{\mathrm{S/D}}$ is the lateral diffused length of the deep S/D region, $X_{\mathrm{JS/D}}$ is the junction depth of the deep S/D, and T_{InGaAs} is the thickness of InGaAs consumed during 'silicide-like' contact formation.

The resistivity of InGaAs (ρ_{InGaAs}), in the S/D and the SDE regions can be expressed as [165]:

$$\rho_{\mathrm{InGaAs}} = \frac{1}{n \cdot q \cdot \mu_{\mathrm{h}} + p \cdot q \cdot \mu_{\mathrm{e}}} \approx \frac{1}{n \cdot q \cdot \mu_{\mathrm{e}}}, \tag{2.4}$$

where q is the elementary charge (1.6×10^{-19} C), n and p are electron and hole carrier concentration, respectively. μ_{e} and μ_{h} are the electron and hole carrier mobility, respectively.

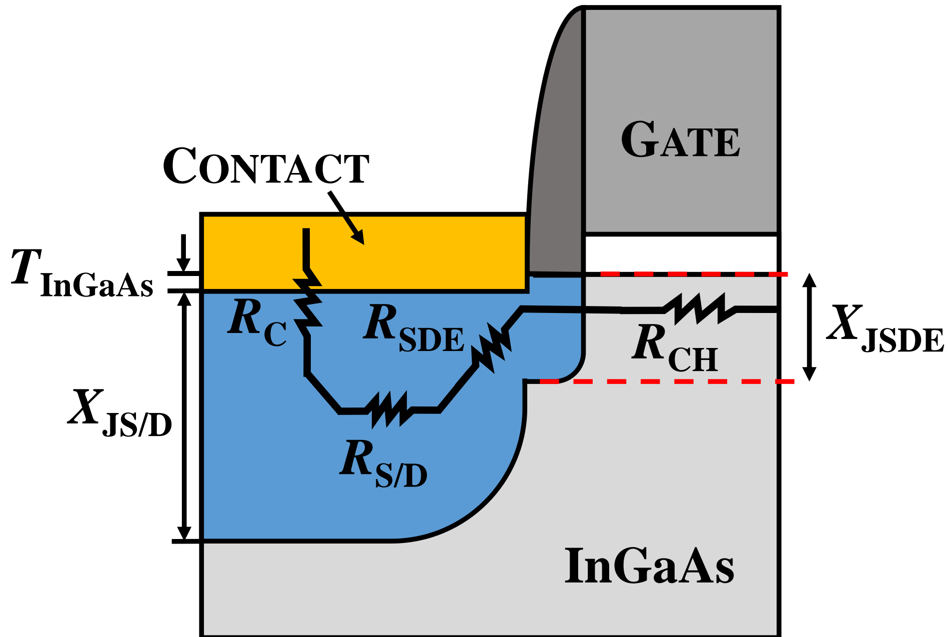


Fig. 2.2. Schematic illustrating the parasitic resistance components of an InGaAs N-MOSFET.

R_C depends on the specific contact resistivity (ρ_C), the sheet resistance of the semiconductor (R_S), the width of the contact (W_C), length of the contact (L_C), and transfer length (L_T). R_C is given by [166]:

$$R_C = \frac{\sqrt{\rho_C \cdot R_S}}{W_C} \cdot \coth\left(\frac{L_C}{L_T}\right). \tag{2.5}$$

As seen in Equation (2.5), it is evident that R_C is a strong function of ρ_C, which is given by [166]:

$$\rho_C \propto \exp\left(\frac{4 \cdot \pi \cdot \sqrt{\varepsilon_S \cdot m_e^*}}{\hbar} \cdot \frac{\phi_{BN}}{\sqrt{N_D}}\right), \tag{2.6}$$

where π is the ratio of a circle's circumference to its diameter, ε_S is permittivity of the semiconductor, m_e^* is the electron effective mass, $\phi_{B,N}$ is the electron Schottky barrier height (SBH), $\hbar$ is Planck's constant, and N_D is the doping concentration of the semiconductor.

From Equations (2.2), (2.3), and (2.5), it can be inferred that R_{SD} strongly depends on parameters such as W_C, X_{JSDE}, $X_{JS/D}$, N_D, L_{SDE}, and $L_{S/D}$. X_{JSDE} and $X_{JS/D}$ need to be minimized to reduce short channel effects (SCEs). However, this leads to high R_{SD}. Thus, engineering the other parameters such as N_D, L_{SDE}, and $L_{S/D}$ becomes imperative. R_{SD} can be reduced by increasing N_D, reducing $L_{S/D}$, and reducing the $\phi_{B,N}$ between the contact metal and the highly n-type doped (n^{++}) S/D regions.

2.4 Source/Drain Engineering in III-V N-MOSFETs

Si CMOS technology employs a self-aligned S/D scheme to reduce R_{SD} [167]. However, in the case of III-V MOSFETs, S/D contacts are typically non-self-aligned and typically formed using a lift-off process [73], [85], [168]-[191]. Non-self-aligned

contacts lead to a large $L_{S/D}$, resulting in a high $R_{S/D}$ [Equation (2.3)], which in turn increases R_{SD} and decreases I_{ON}. Moreover, contacts for III-V MOSFETs have been predominantly gold (Au) based, such as TiPtAu and NiAuGe [168]-[191]. However, Au is a contaminant in Si devices. Hence, gold-free contacts are necessary when Si and III-V MOSFETs are integrated on a common platform in the future. Thus, new Si CMOS compatible contact materials, with low-resistances, are required for S/D contacts in III-V MOSFETs. Furthermore, if III-V fin field effect transistors (FinFETs) are introduced at future technology nodes to control SCEs, reducing R_{SD} would become more critical in achieving high I_{ON}. III-V FinFETs would suffer from high R_{SDE} because of the narrow width of the fins (smaller W_G) used in these devices [Equation (2.2)]. One solution to reduce R_{SDE} is to form self-aligned metallic contacts on these small fins, which decreases R_S at the SDE regions, thus reducing R_{SDE}. Moreover, a self-aligned contact scheme reduces $L_{S/D}$ and improves the scalability of the transistor. Section 2.5 elucidates the concept of self-aligned contacts for InGaAs N-MOSFETs.

R_{SD} and I_{ON} are also affected by N_D of the S/D and SDEs. High quality ultra-shallow junctions are required in the SDE regions for suppressing source-to-drain leakage and SCEs such as drain-induced-barrier-lowering (DIBL), especially in sub-10 nm MOSFETs. High N_D in the SDE regions reduces R_{SDE} through a reduction in ρ_{SDE} [Equation (2.2)]. Furthermore, R_C decreases as N_D is increased due to the lowering of ρ_C at the metal-semiconductor interface. The highest N_D of InGaAs reported in the literature is ~6×10^{19} cm^{-3} that was achieved by *in situ* doping [192]. However, this is lower than the active n-type doping that can be achieved in Si (>10^{20} cm^{-3}). Moreover, incorporating *in situ* doping in device fabrication processes is challenging as it requires selective growth of the III-V material in the S/D regions. Furthermore, doping techniques that are conformal are required to form SDEs of 3D structures such

as FinFETs and nanowire transistors. In the future, as the fin pitch is decreased to reduce the device dimensions, realizing conformal doping profiles will become even more challenging. Conventional beam-line ion implantation used in the industry will not be able to achieve this goal. Furthermore, ion implantation induces crystal damage and defects at small fin dimensions that would otherwise be difficult to recover due to a lack of sufficient crystalline seed for crystal regrowth, resulting in higher leakage current and R_{SD}. Hence, new doping techniques that can produce abrupt and ultra-shallow junctions with high N_D, few defects, and conformality are necessary (described in Chapter 5).

2.5 Self-Aligned Metallic Contacts for InGaAs N-MOSFETs

Self-aligned silicides ('salicide') have been used to form the S/D contacts of MOSFETs in Si CMOS technology. In a salicide contact scheme, the S/D contacts are formed adjacent to the gate (separated by a spacer). The proximity of metal contacts to the channel helps to reduce $R_{S/D}$. This salicide process is well established for Si MOSFETs. Several silicides such as nickel silicide (NiSi) [193]-[204], cobalt silicide (CoSi) [205]-[210], titanium silicide (TiSi) [211]-[215], platinum silicide (PtSi) [216]-[220], and nickel-platinum silicide (NiPtSi) [221]-[225] have been studied extensively. To exploit the advantages of this self-aligned contact scheme, metallic alloys such as Ni-InGaAs, cobalt-InGaAs (Co-InGaAs) and palladium-InGaAs (Pd-InGaAs) were studied for potential use in InGaAs N-MOSFETs.

2.5.1 Ni-InGaAs Contact Technology

(a) Ni-InGaAs formation process

Fig. 2.3 depicts the Ni-InGaAs formation process. Native oxide is removed from InGaAs surface by cleaning the samples using dilute hydrofluoric acid (DHF) or hydrochloric acid (HCl). Subsequently, nickel (Ni) is deposited on the InGaAs surface and annealed at 250 °C or above to form Ni-InGaAs. Fig. 2.4 shows the cross-sectional Transmission Electron Microscopy (TEM) images of the Ni-InGaAs formation process [226]. The as-deposited Ni thickness was ~30 nm [Fig. 2.4 (a)]. This Ni layer was then annealed at 250 °C to form ~ 45 nm thick Ni-InGaAs [Fig. 2.4 (b)]. Ni-InGaAs had a crystalline structure as shown in the high resolution TEM image in Fig. 2.4 (c).

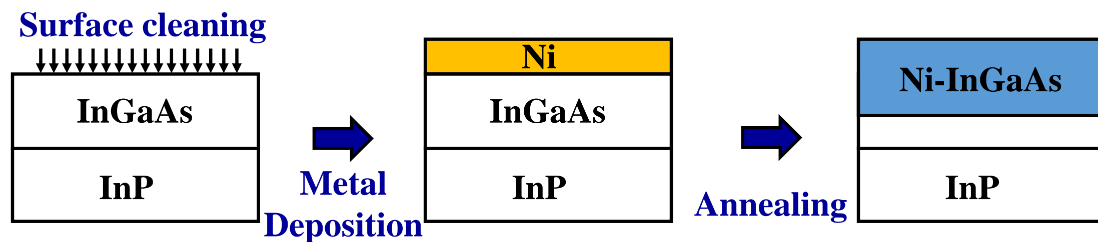


Fig. 2.3. Schematic illustrating the process of Ni-InGaAs formation.

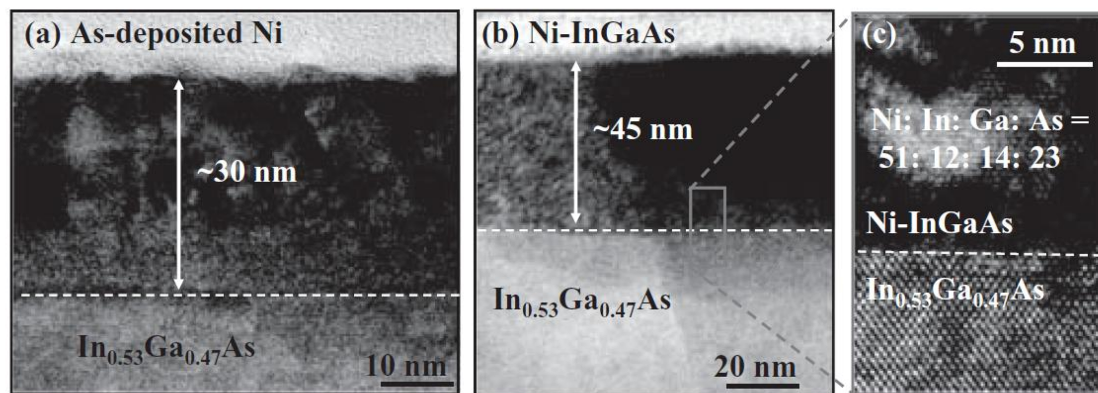


Fig. 2.4. (a) As-deposited Ni film (~30 nm) on an InGaAs/InP substrate. (b) The ~45 nm thick Ni-InGaAs film formed after the samples were annealed at 250 °C. (c) High resolution TEM of the Ni-InGaAs/InGaAs interface. Crystalline Ni-InGaAs was formed and the atomic compositions of Ni, In, Ga, and As were 51, 12, 14, and 23, respectively. These figures are taken from Ref. [226].

(b) Crystal structure of Ni-InGaAs

The crystal structure of Ni-InGaAs was studied by Ivana *et al.* [227]. High resolution TEM and X-Ray Diffraction (XRD) were used to study the Ni-InGaAs film formed at 250 °C. Fig. 2.5 (a) and 2.5 (b) display the cross-sectional TEM images and the selective area diffraction (SAD) pattern (taken from the region indicated by the white circle), respectively. The SAD pattern shows a highly epitaxial Ni-InGaAs layer. Analysis of the diffraction pattern reveals a hexagonal crystal structure for the Ni-InGaAs film [Fig. 2.5 (c)]. Fig. 2.5 (d) illustrates a model of the unit cell of

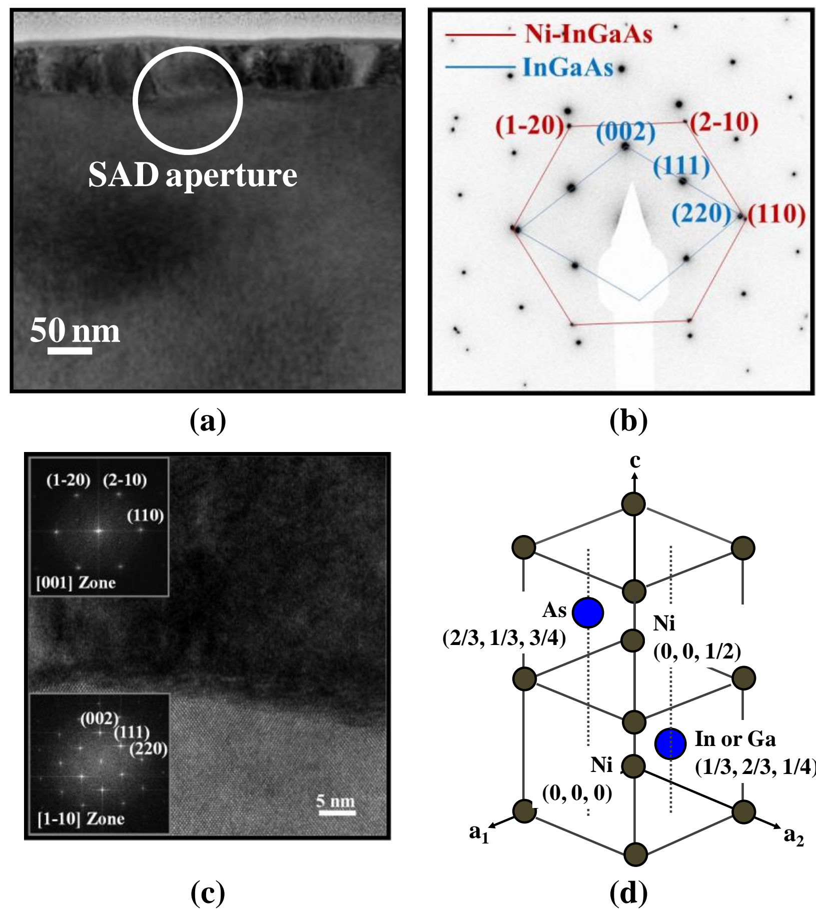


Fig. 2.5. (a) TEM image of the Ni-InGaAs/InGaAs sample. (b) The SAD pattern obtained from the region shown in (a). The diameter of the circle is 150 nm. (c) High resolution TEM image of Ni-InGaAs/InGaAs. The corresponding diffraction patterns are shown in the inset. (d) Unit cell of Ni-InGaAs phase. Ni-InGaAs shows a NiAs (B8) type of structure. These figures are taken from Ref. [227].

Ni-InGaAs. The composition and structure of the Ni-InGaAs film resemble the NiAs (B8) structure [228]-[230]. In this structure, Ni atom occupies the (0, 0, 0) and (0, 0, 1/2) positions, a gallium (Ga) or indium (In) atom occupies the (1/3, 2/3, 1/4) positions, and an arsenic (As) atom occupies the (2/3, 1/3, 3/4) positions. The lattice parameters of Ni-InGaAs were extracted to be a = 0.396 ± 0.002 nm and c = 0.516 ± 0.002 nm.

(c) Other material properties of Ni-InGaAs

Ivana *et al*. studied the effect of the annealing temperature T_{anneal} and time t_{anneal} on the reaction between Ni and InGaAs [227]. Ni with different thicknesses t_{Ni} were deposited on InGaAs/InP substrates and annealed at different temperatures, ranging from 200 to 350 °C, for 60 s. The R_S of the annealed samples were then measured [Fig 2.6 (a)]. There was no significant reaction observed at 200 °C. However, a very

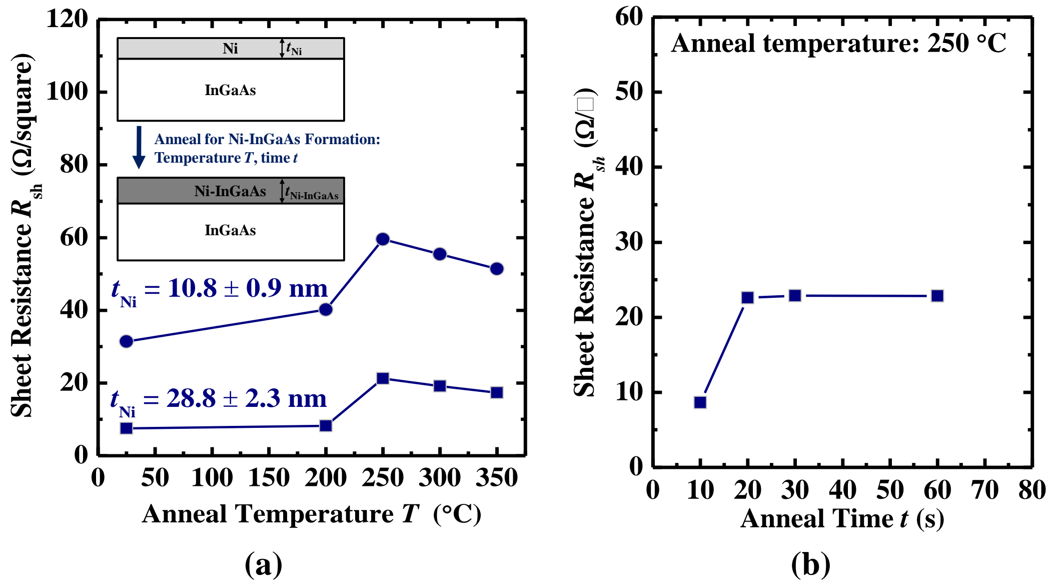


Fig. 2.6. (a) R_S of Ni-on-InGaAs samples annealed at various temperatures for a fixed time of 60 s. The inset shows an illustration of the formation of Ni-InGaAs (bottom) by annealing as-deposited Ni-on-InGaAs (top) at temperature T_{anneal} for time t_{anneal}. (b) Time evolution of R_S for ~28 nm of deposited Ni on InGaAs annealed at 250 °C. These figures are taken from Ref. [227].

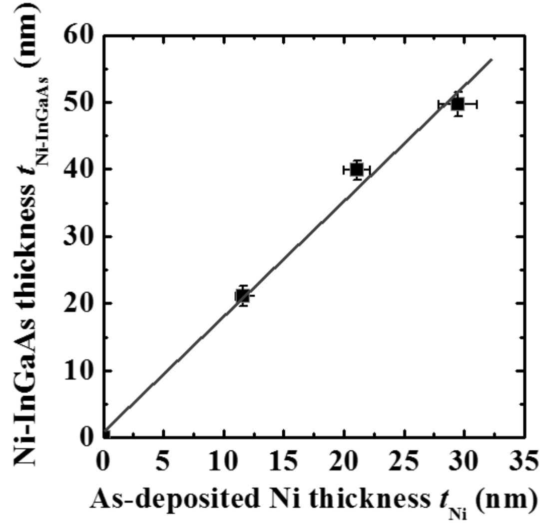


Fig. 2.7. Correlation between the as-deposited Ni thickness and the corresponding Ni-InGaAs thickness. A linear relationship is observed. A thickness ratio of ~1: 1.7 for Ni to Ni-InGaAs was extracted. This figure is taken from Ref. [227].

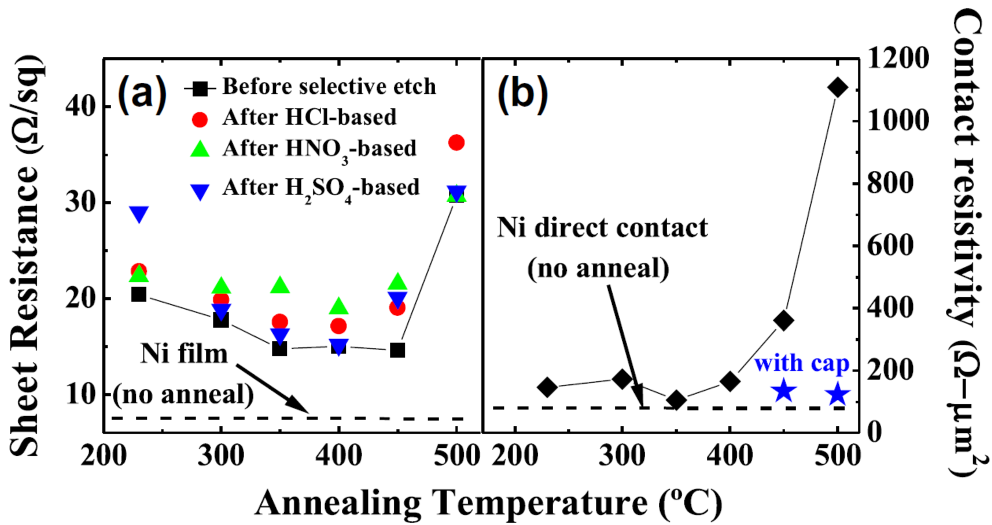


Fig. 2.8. (a) R_S of Ni-InGaAs as a function of T_{anneal}. The samples were annealed for 5 min in vacuum. R_S before and after selective wet etching of unreacted metal is also plotted. (b) ρ_C of Ni-InGaAs as a function of T_{anneal} on samples with (blue stars) and without (black diamond-shaped dots) SiO_2 cap. This figure was taken from Ref. [156].

thin intermixed layer was suspected to have formed at the Ni/InGaAs interface. The Ni layer was fully consumed to form a uniform Ni-InGaAs layer, at T_{anneal} = 250 °C and above, for t_{anneal} = 60 s. Ni-InGaAs was found to have a higher resistivity than Ni. The effect of t_{anneal} was also investigated. Samples were annealed at 250 °C for different

annealing times. Fig. 2.6 (b) plots R_S as a function of annealing time. R_S increased and later saturated as the annealing time exceeded 20 s, which indicates the completion of the reaction between Ni and InGaAs. In addition, it was seen that 1 nm of Ni reacted with $In_{0.53}Ga_{0.47}As$ to form ~1.7 nm of Ni-InGaAs (Fig. 2.7).

A similar study was conducted by Czornomaz *et al.* [156]. Fig. 2.8 (a) shows R_S as a function of the annealing temperature. The results were the same as those reported by Ivana *et al.* [227]. Fig. 2.8 (b) shows the ρ_C of Ni-InGaAs as a function of T_{anneal}. ρ_C of ~ 1.46×10^{-6} $\Omega\cdot cm^2$ was obtained on $In_{0.53}Ga_{0.47}As$ with N_D of 1×10^{19} cm^{-3} at 230 °C. ρ_C was relatively constant up to 400 °C, and increased at higher annealing temperatures, which suggested that the electrical properties of Ni-InGaAs degrade at temperatures above 400 °C. The thermal stability of the Ni-InGaAs contacts improves in the presence of a silicon dioxide (SiO_2) capping layer, which is deposited before the annealing step. Ni-InGaAs formed in the presence of an SiO_2 capping layer showed a very stable ρ_C of about 1 to 1.5×10^{-6} $\Omega\cdot cm^2$ at temperatures up to 500 °C, which makes Ni-InGaAs suitable for standard CMOS backend processing.

(d) Schottky barrier height of Ni-InGaAs on $In_{0.53}Ga_{0.47}As$

The band alignment of Ni-InGaAs on unintentionally n-type doped $In_{0.53}Ga_{0.47}As$ (~ 1×10^{16} cm^{-3}) was studied by Mehari *et al.* [231]. The SBH for electrons $\phi_{B,N}$ was extracted using temperature dependent current-voltage (*I-V*) characteristics of Ni-InGaAs Schottky contacts to n-$In_{0.53}Ga_{0.47}As$. Fig. 2.9 (a) shows the schematic of the Schottky diode used for this experiment while Fig. 2.9 (b) portrays the corresponding energy band diagram at the Ni-InGaAs/InGaAs interface. The measurements were conducted within a temperature range of 80-300 K. $\phi_{B,N}$ of ~ 0.24 eV was extracted from the diode measurements. The Schottky diodes showed

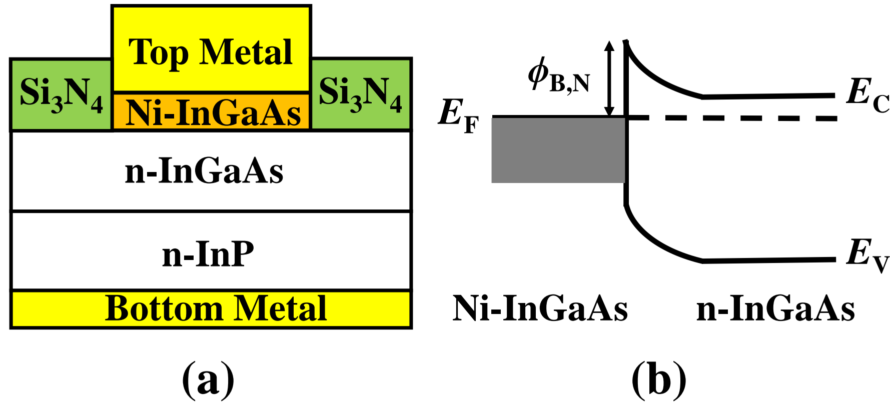


Fig. 2.9. (a) Schematic illustrating the cross-section of Ni-InGaAs Schottky diodes and (b) the corresponding energy band diagram at the Ni-InGaAs/InGaAs interface [231].

nearly ideal *I-V* facilitating the accurate extraction of $\phi_{B,N}$, which was attributed to the lack of native oxides and contaminants at the Ni-InGaAs/InGaAs interface. These results indicated that to achieve better Ohmic contacts further improvements are required to reduce $\phi_{B,N}$ between Ni-InGaAs and n^{++}-InGaAs.

(e) InGaAs N-MOSFETs with Ni-InGaAs Self-Aligned Source/Drain

$In_{0.7}Ga_{0.3}As$ N-MOSFETs with self-aligned Ni-InGaAs S/D were first demonstrated by Xingui *et al.* [232]. Fig. 2.10 (a) elucidates the key steps in the process flow used for the device fabrication. The InGaAs sample was cleaned using HCl, ammonium hydroxide (NH_4OH) and ammonium sulfide [$(NH_4)_2S$] solutions to remove native oxide, excess arsenic and passivate the surface, respectively, prior to gate dielectric deposition. Subsequently, ~7 nm aluminum oxide (Al_2O_3) was deposited using atomic layer deposition (ALD). Tantalum nitride (TaN) gate electrode was then sputtered, and patterned using optical lithography and a chlorine-based plasma etching process. ~27 nm of Ni was then sputtered, and the samples were annealed at 250 °C for 60 s to form Ni-InGaAs S/D regions. The device fabrication process was completed

with the selective removal of unreacted Ni using hot HCl. The TEM images in Fig 2.10 (b)-(d) show the various cross-sections of the $In_{0.7}Ga_{0.3}As$ channel MOSFET.

Fig. 2.11 displays the electrical characteristics of a transistor with L_G = 1 µm and W_G = 50 µm. I_{ON} and peak transconductance (G_M) values of ~100 µA/µm and

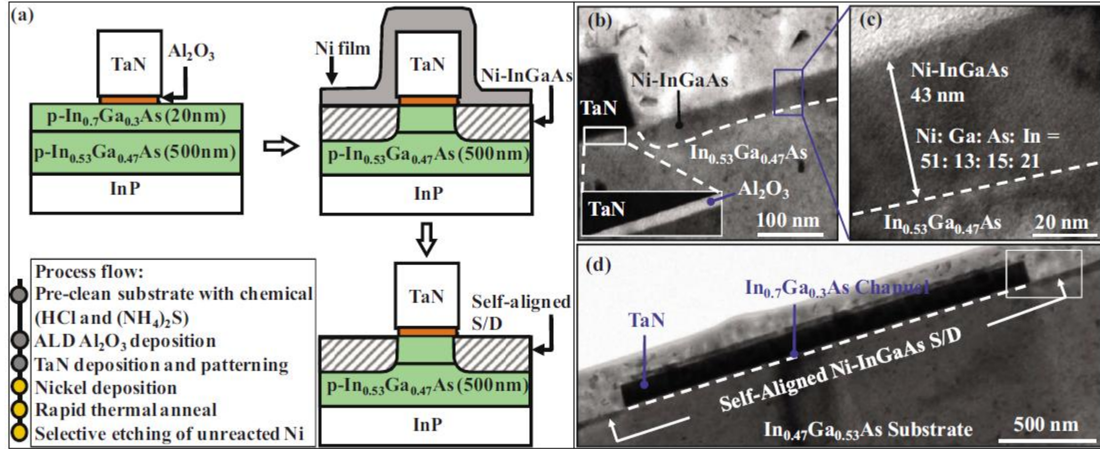


Fig. 2.10. (a) Schematic of the process flow used in the fabrication of an InGaAs N-MOSFET with Ni-InGaAs self-aligned S/D. Cross-sectional TEM images of various parts of the MOSFET are shown in (b)-(d). Ni-InGaAs was ~43 nm thick. A distinct interface between Ni-InGaAs and InGaAs was observed. These figures are taken from Ref. [232].

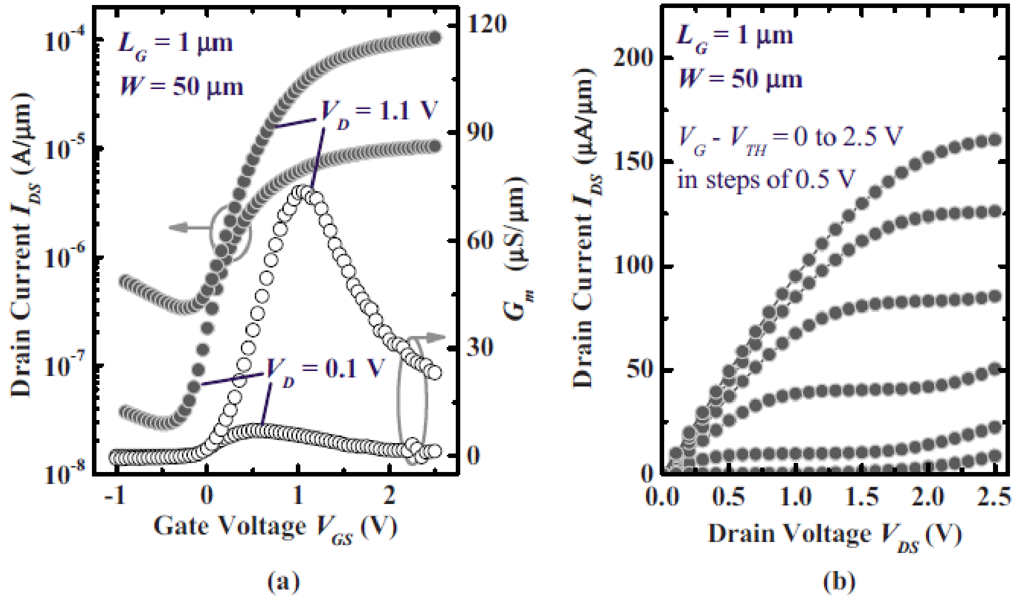


Fig. 2.11. (a) I_D-V_{GS} and G_M-V_{GS} plot of an $In_{0.7}Ga_{0.3}As$ N-MOSFET with self-aligned Ni-InGaAs S/D. The device with L_G = 1 µm has an I_{ON} of ~100 µA/µm and peak G_M of 74 µS/µm at V_D = 1.1 V. (b) I_D-V_D characteristics of the same transistor at various gate overdrives (V_{GS} - V_T), from 0 V to 2.5 V. These figures are taken from Ref. [232].

74 μS/μm at drain voltage (V_D) of 1.1 V, respectively were obtained [Fig. 2.11 (a)]. The threshold voltage (V_T) of the device was 0.1 V. The I_{ON} and peak G_M were low, due to the large L_G and equivalent SiO_2 thickness of the gate dielectric (~3.5 nm). The device exhibited an ON-state current to OFF-state current (I_{ON}/I_{OFF}) ratio of ~10^3. The drain current (I_D) versus V_D of the transistor at various gate overdrives (V_{GS} - V_T) from 0 to 2.5 V, in steps of 0.5 V, are plotted in Fig. 2.11 (b). The device showed good saturation and pinch-off characteristics. Furthermore, an R_{SD} of 8.9 kΩ·μm was extracted, which is high compared to the International Technology Roadmap for Semiconductors (ITRS) requirements, and entails further improvement.

2.5.2 Other Self-Aligned Contact Schemes

Self-aligned contacts based on Pd-InGaAs [233] and Co-InGaAs [234] have also been explored for potential use in InGaAs N-MOSFETs. 20 nm thick Pd-InGaAs film formed at 250 ºC had an R_S of 77.3 Ω/square [Fig. 2.12 (a)], which was higher than that of Ni-InGaAs of comparable thickness, i.e. Pd-InGaAs has a higher bulk resistivity than Ni-InGaAs. Pd-InGaAs on n-type $In_{0.53}Ga_{0.47}As$ with N_D of 2×10^{18} cm^{-3} has a ρ_C of ~8.35×10^{-5} $\Omega \cdot cm^2$, which is one order of magnitude higher than that of Ni-InGaAs. Similarly, cobalt (Co) reacts with $In_{0.53}Ga_{0.47}As$, at temperatures as low as 350 ºC, to form Co-InGaAs. R_S of the ~60 nm Co-InGaAs film, formed at 350 ºC, was ~14 Ω/square [Fig. 2.12 (b)]. Co-InGaAs forms Ohmic contacts on n-type $In_{0.53}Ga_{0.47}As$ with N_D of 5×10^{19} cm^{-3}. An R_C and ρ_C of ~1.12 kΩ·μm and ~6.25×10^{-4} $\Omega \cdot cm^2$, respectively were extracted from TLM measurements. ρ_C of Co-InGaAs is higher than that of Ni-InGaAs. $In_{0.53}Ga_{0.47}As$ N-MOSFET with Co-InGaAs as metallic S/D material was demonstrated using a fabrication process flow similar to that explained in the previous Section.

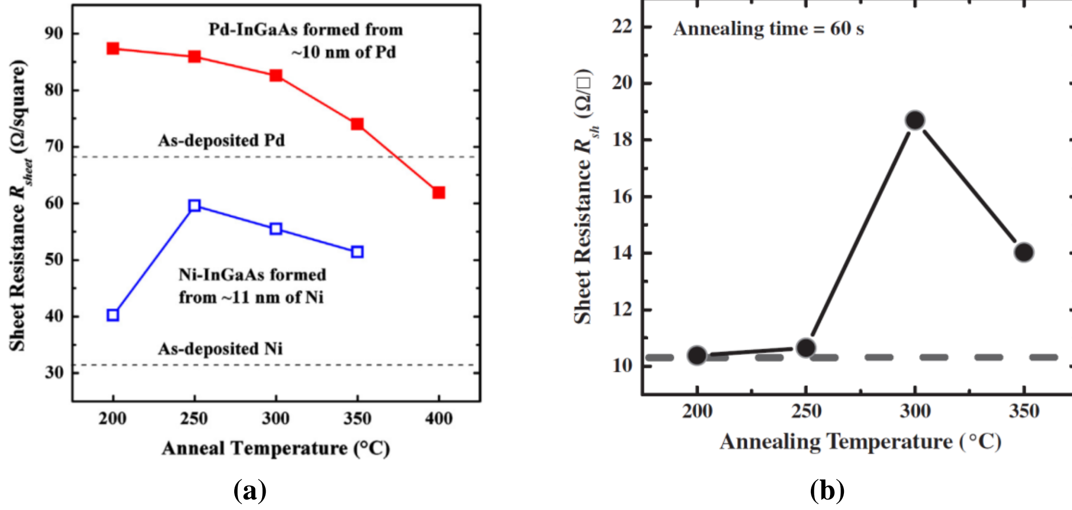


Fig. 2.12. (a) R_S versus T_{anneal} for Pd-InGaAs formed from the reaction between palladium (Pd) and InGaAs. Anneal time is fixed at 60 s. The R_S values for Ni-InGaAs are plotted for reference. The dashed lines indicate the R_S of as-deposited Ni and Pd. (b) R_S versus T_{anneal} for Co-InGaAs formed from the reaction between Co and InGaAs. Anneal time is fixed at 60 s. Co-InGaAs was formed at 350 ºC. The dashed line indicates the R_S of as-deposited Co. (a) is taken from Ref. [233] and (b) is taken from Ref. [234].

Table 2.1 summarizes the properties of various contact schemes on $In_{0.53}Ga_{0.47}As$. The lowest ρ_C achieved for Ni-InGaAs on n^{++}-$In_{0.53}Ga_{0.47}As$ (N_D of 5×10^{19} cm^{-3}) was ~1×10^{-6} Ω·cm^2 [155]. This ρ_C is still two orders of magnitude higher than that required by ITRS (i.e. 1×10^{-8} Ω·cm^2) [239]. The high ρ_C observed is attributed to the high $\phi_{B,N}$ of ~0.24 eV [156]. ρ_C can be further reduced by increasing the In composition in $In_xGa_{1-x}As$ to minimize the SBH at the metal/semiconductor interface. Moreover, $\phi_{B,N}$ approaches zero at In composition of 0.7 [235]. Hence, increasing the In composition (x) to 0.7 or even further to that of InAs (x = 1) is beneficial in achieving low ρ_C. The reaction of Ni with InAs to form Ni-InAs has been explored [237], [242]. The R_S of ~10 nm thick Ni-InAs film was 110 Ω/square [241]. Due to the lower $\phi_{B,N}$, a lower ρ_C of ~1.7×10^{-7} Ω·cm^2 was obtained for Ni-InAs on n^{++}-InAs (N_D of 1×10^{19} cm^{-3}) [242], compared to Ni-InGaAs on n^{++}- $In_{0.53}Ga_{0.47}As$.

Table 2.1. Benchmarking the various self-aligned contact schemes on $In_{0.53}Ga_{0.47}As$.

Parameters	Ni-InGaAs/ $In_{0.53}Ga_{0.47}As$	Co-InGaAs/ $In_{0.53}Ga_{0.47}As$	Pd-InGaAs/ $In_{0.53}Ga_{0.47}As$
Bulk resistivity (μΩ·cm)	77.5 [156] 96 [226] 125 [235] 135 [236]	84 [234]	154 [233]
Contact resistivity (Ω·cm²)	1.46×10^{-6} ($N_D = 1 \times 10^{19}$ cm^{-3}) [156] 5.4×10^{-4} ($N_D = 2 \times 10^{18}$ cm^{-3}) [226] 1×10^{-6} ($N_D = 5 \times 10^{19}$ cm^{-3}) [155]	6.25×10^{-4} ($N_D = 5 \times 10^{19}$ cm^{-3}) [234]	8.35×10^{-5} ($N_D = 2 \times 10^{18}$ cm^{-3}) [233]
Electron SBH (eV)	0.239 ± 0.01 [156] 0.12 [235] -0.1 ± 0.1 [227]	0.12 [238]	–

In addition, preliminary studies by one of our collaborators revealed that the ρ_C can also be reduced by inserting a capping layer, such as InP, between Ni and InGaAs before

the reaction step. The reduction in ρ_C was attributed to the prevention of Ga out-diffusion from the Ni-InGaAs/InGaAs interface. Using this approach, ρ_C of Ni-InGaAs on n^{++}-$In_{0.53}Ga_{0.47}As$ with N_D of 3×10^{19} cm^{-3} was reduced to 4×10^{-8} $\Omega\cdot cm^2$, which is closer to the ITRS requirements. The ρ_C can be further reduced to 1×10^{-8} $\Omega\cdot cm^2$ by increasing the N_D of the S/D regions [Equation (2.6)].

Co-InGaAs and Pd-InGaAs based contact technologies need to be explored and developed further to match Ni-InGaAs in terms of its electrical properties (such as R_S and ρ_C). The results from the literature review suggest that Ni-InGaAs is the most mature and viable contact material choice for InGaAs N-MOSFETs. This thesis, thus, focuses on developing techniques to improve and optimize Ni-InGaAs contact metallization technology for potential application in InGaAs N-MOSFETs.

2.6 Summary

In this Chapter, the current status of research on self-aligned contact technologies for InGaAs N-MOSFETs was reviewed. The basic concepts and components of S/D series resistance in an InGaAs N-MOSFET were introduced in Sections 2.2 and 2.3, and a brief history on the contact technologies used for III-V materials is documented in Section 2.4. A literature review on self-aligned contact technologies for InGaAs transistors was presented in Section 2.5 with a detailed focus on Ni-InGaAs based contacts, which include the details of the Ni-InGaAs formation process, its crystal structure, other material properties (such as R_S and ρ), band alignment with InGaAs and the integration of Ni-InGaAs in InGaAs MOSFETs. A brief discussion on other contact schemes such as Pd-InGaAs and Co-InGaAs was also included.

Chapter 3

Selective Wet Etching Process for Contact Formation in InGaAs N-MOSFETs with Self-Aligned Source and Drain

3.1 Introduction

As mentioned in Chapter 2, a self-aligned contact scheme can be used to reduce the source/drain (S/D) resistances (R_{SD}) in an InGaAs n-channel Metal-Oxide Semiconductor Field-Effect Transistor (N-MOSFET). The most important qualities that determine the appropriate metal to be used in the self-aligned metallization process are: (1) low bulk resistivity (ρ), and (2) low contact resistivity (ρ_C) to the highly n-type doped (n^{++}) InGaAs S/D regions. Several self-aligned contact schemes using metallic alloys such as Ni-InGaAs [155], [156], [226], [227], [235], [236], Co-InGaAs [234] and Pd-InGaAs [233] have been explored. Both the lowest ρ of 77.5 μΩ·cm [156] and the lowest ρ_C of ~1 × 10^{-6} Ω·cm^2 [155] on n^{++}-$In_{0.53}Ga_{0.47}As$ [with a doping concentration (N_D) of 5 × 10^{19} cm^{-3}] were achieved using Ni-InGaAs alloy. This makes Ni-InGaAs the most promising option for the contact metal in InGaAs N-MOSFETs.

The fabrication process of an InGaAs N-MOSFET with metallic self-aligned S/D was illustrated in Chapter 2. It requires a blanket nickel (Ni) deposition over a gate stack, an annealing step to initiate the reaction between Ni and InGaAs, and a selective etching process that removes the excess Ni after the formation of Ni-InGaAs (as shown in Fig. 3.1). However, the selective etch process of Ni over Ni-InGaAs has not been explored in depth. In this Chapter, the etch rates of Ni-InGaAs metallic film and Ni in hydrochloric acid (HCl), nitric acid (HNO_3), hydrofluoric acid (HF) and Sulfuric Peroxide Mixture (SPM) etch chemistries were determined

systematically using sheet resistance (R_S) method, step height measurements, and cross-sectional Transmission Electron Microscopy (TEM) characterization. The etch selectivity of Ni over Ni-InGaAs in various etchants were determined. The results of this work is paramount for realizing Ni-InGaAs self-aligned S/D in InGaAs N-MOSFETs.

Nickel platinum (NiPt) silicide (NiPtSi) and NiPt germanide (NiPtGe) have been identified as potential candidates for self-aligned S/D contacts in silicon (Si) and germanium (Ge) MOSFETs, respectively, at future technology nodes [243]-[247]. InGaAs N-MOSFETs are expected to replace Si N-MOSFETs at sub-10 nm technology nodes, when they would potentially be integrated alongside other Si and Ge devices on a common platform. Therefore, using a common NiPt based contact scheme for the Si, Ge and InGaAs devices would be advantageous in reducing the number of steps in the fabrication process steps. This in turn increases throughput and reduce the cost of production. Therefore, the material properties of nickel platinum indium gallium arsenide (NiPt-InGaAs) was studied by our research group [248]. In this study, NiPt with ~15 atomic percentage platinum (Pt) composition was used to form NiPt-InGaAs. The NiPt film was deposited by co-sputtering Ni and Pt. With the incorporation of Pt, an improvement in the thermal stability of Ni-InGaAs was observed. The R_S of NiPt-InGaAs was higher than that of Ni-InGaAs for annealing temperatures of up to

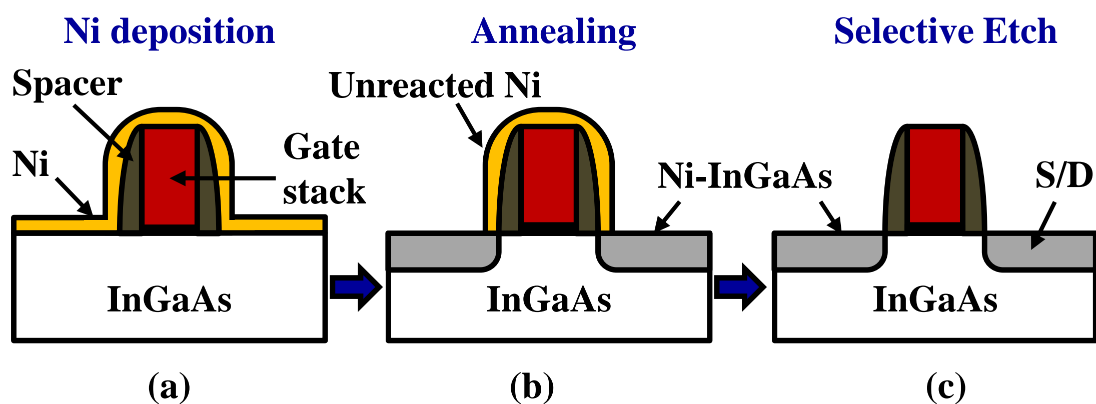
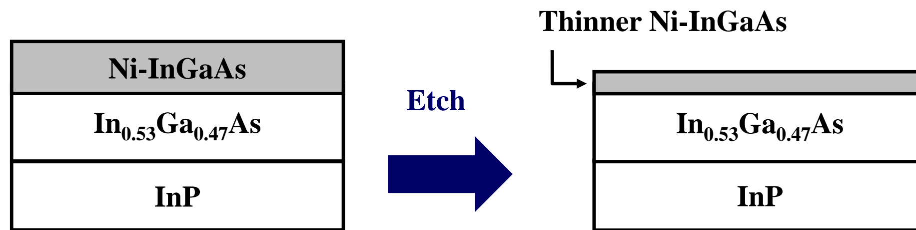
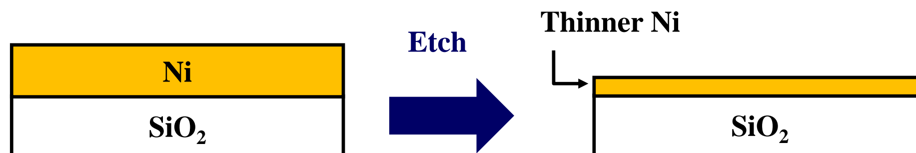


Fig. 3.1. An illustration of the process flow used to form self-aligned metallic S/D in an InGaAs N-MOSFET which involves (a) a blanket deposition of Ni over the sample, (b) an annealing step to react Ni and InGaAs to form Ni-InGaAs, and (c) a selective etch to remove the unreacted Ni.

400 °C. However, as the formation temperature was increased, the R_S values of NiPt-InGaAs decreased to below that of Ni-InGaAs, due to the enhanced thermal stability. The ρ_C of NiPt-InGaAs on n^{++}-$In_{0.53}Ga_{0.47}As$ with N_D of ~2×10^{19} cm^{-3} was ~4×10^{-5} $\Omega \cdot cm^2$. The ρ_C extracted was comparable to that of Ni-InGaAs on n^{++}-$In_{0.53}Ga_{0.47}As$ with the same N_D. In addition, the ρ_C of NiPt-InGaAs was consistent at formation temperatures up to 500 °C, whereas the ρ_C of Ni-InGaAs increased due to thermal degradation. These results indicated that NiPt-InGaAs was also a suitable metal to form self-aligned S/D contacts in InGaAs MOSFETs. Hence, it was important to develop an etch process that selectively etches NiPt over NiPt-InGaAs. The etch selectivity of NiPt over NiPt-InGaAs was extracted using the R_S method. The details are presented in Section 3.3.2.





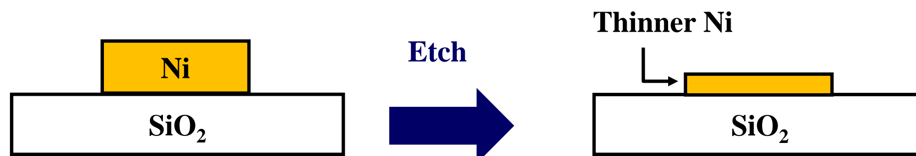


Fig. 3.2. Schematic of the samples used for determining the etch rates of Ni-InGaAs and Ni; (a) Unpatterned or blanket sample comprising of Ni-InGaAs formed on $In_{0.53}Ga_{0.47}As$/InP substrate, (b) blanket sample comprising of Ni deposited on silicon dioxide (SiO_2) on a Si substrate, and (c) patterned Ni film formed on SiO_2 on Si.

3.2 Experimental Procedures

3.2.1 Method of Determining the Etch Rate and Selectivity

The samples used for determining the etch rates of Ni and Ni-InGaAs are shown in Fig. 3.2. Blanket (unpatterned) Ni-InGaAs/ $In_{0.53}Ga_{0.47}As$ /InP samples as shown in Fig. 3.2 (a) were used for obtaining the etch rate of Ni-InGaAs. The etch rate of Ni-InGaAs can be deduced from R_S measurements and from cross-sectional TEM images obtained from samples that were etched for different times in an etchant. Ni-InGaAs was formed by annealing Ni on $In_{0.53}Ga_{0.47}As$/InP substrate at 250 °C for 5 minutes.

Fig. 3.2 (b) and 3.2 (c) show blanket and patterned Ni films formed on 100 nm thick SiO_2/Si substrates. The Ni films were annealed at 250 °C for 5 minutes. This was done to simulate the conditions in a MOSFET fabrication process, where the excess Ni will also go through the annealing process. The etch rate of Ni in various etchants can be obtained by monitoring the film thickness by R_S method (for blanket sample) or by step height measurement using surface profiler (for patterned sample) during etch.

The R_S values of blanket Ni-InGaAs/$In_{0.53}Ga_{0.47}As$/InP can be obtained by four-point probe measurements. The R_S of a conductive film is given by

$$R_S = \frac{\rho}{t_f} \tag{3.1}$$

where ρ is the resistivity of the film, and t_f is the thickness of the film. During the etch process, t_f decreases and R_S increases over time t. The etch rate r of the conductive film is given by

$$r = \left|\frac{dt_f}{dt}\right| = \left|\rho \cdot \frac{d\left(R_S^{-1}\right)}{dt}\right|. \tag{3.2}$$

Thus, the etch rates of Ni-InGaAs [Fig. 3.2 (a)] and Ni [Fig. 3.2 (b)], $r_{Ni\text{-}InGaAs}$ and r_{Ni}, respectively, can be obtained for a given etchant. The selectivity of the etching process can then be calculated as the ratio of the etch rates of Ni and Ni-InGaAs, i.e.

$$\text{Selectivity} = \frac{r_{\text{Ni}}}{r_{\text{Ni-InGaAs}}} \quad . \tag{3.3}$$

3.2.2 Selection of Chemicals and Conditions

Chemicals that are known etchants of Ni were chosen for this experiment. Etching of Ni has been well documented. Many etch chemistries etch Ni at a rapid rate, such as HCl, HNO_3, Aqua-Regia [HCl:HNO_3:H_2O (3:1:2)], SPM [H_2SO_4:H_2O_2 (4:1)], HCl:H_2O_2 (4:1), HCl:HNO_3 (5:1), and HF:HNO_3 (1:1) [249]-[255]. The rate at which these etchants etch Ni-InGaAs would be determined. An etchant that etches Ni quickly but etches Ni-InGaAs slowly will be one with high etch selectivity.

The blanket Ni-InGaAs/$In_{0.53}Ga_{0.47}As$/InP and Ni/SiO_2/Si samples were etched in the various etchants and the R_S method was used to obtain the etch rates. The etch rate of Ni in most of these chemistries was very high (more than 1000 nm/minute). Also, in the case of HCl:HNO_3 (5:1), Aqua-Regia, HCl:H_2O_2 (4:1), and HF:HNO_3 (1:1) etch chemistries, it was observed that a few tens of nanometer of Ni-InGaAs was etched away in seconds. The SPM solution not only removed the Ni- InGaAs quickly but also etched away the underlying InGaAs layer in approximately one minute. These results are summarized in Table 3.1. These etch chemistries were eliminated in future rounds of experiments as the selectivities could not be easily determined.

Since HF etching is commonly used in the process flow of fabricating InGaAs N-MOSFETs, HF:H_2O (1:100) solution was also added to the list of etchants, to determine the effects of an HF dip on Ni-InGaAs thickness. HCl and HNO_3 were the focus of the rest of the etching experiments here. The equations for the chemical reactions of Ni in HCl and HNO_3 are shown in Table 3.2 [251].

Table 3.1. Etch rates of Ni and Ni-InGaAs in various etch chemistries.

Chemical	Etch rate (nm/minute)		Comment
	r_{Ni}	$r_{Ni-InGaAs}$	
70 % HNO_3	>50	> 150	Ni-InGaAs etched extremely fast.
$HCl:HNO_3:H_2O$ (3:1:2)	> 120	Very high*	Ni-InGaAs etched away extremely fast.
$H_2SO_4:H_2O_2$ (4:1)	> 120	Very high*	The 1 μm InGaAs under the Ni-InGaAs etched away within 1 minute.
$HCl:H_2O_2$ (4:1)	> 100	Very high*	Ni-InGaAs etched away extremely fast.
$HCl:HNO_3$ (5:1)	> 100	Very high*	Not good for Ni-InGaAs. The surface was damaged.
$HF:HNO_3$ (1:1)	Very high*	Very high*	Removes Ni-InGaAs within a few seconds.

* The film was etched away within a few seconds. The etch rate was >1000 nm/min.

Table 3.2. Chemical reactions between Ni and HCl or HNO_3 [251].

Acid	Solution	Chemical reaction scheme
Hydrochloric acid (HCl)	All	$Ni^0 + 2HCl \rightarrow Ni^{2+} + 2Cl^{2-} + H_2(g)$
Nitric acid (HNO_3)	Diluted	$Ni^0 + 8HNO_3 \rightarrow 3Ni^{2+} + 6NO_3^- + 2NO(g) + 4H_2O$
Nitric acid (HNO_3)	Concentrated	No reaction

Dilute HNO_3 solutions were prepared by mixing concentrated HNO_3 (70 % HNO_3) solution with H_2O in the ratios 1:10 and 1:20 [HNO_3 (1:10) and HNO_3 (1:20), respectively]. The etching was then performed at room temperature (25°C).

Dilute HCl solution was prepared by mixing concentrated HCl (36 % HCl) solution with H_2O in the ratio of 1:10 [HCl (1:10)]. Etching using HCl-based chemistry was carried out at four different temperatures, 25 °C, 50 °C, 70 °C and 90 °C.

A separate sample was used for each etch chemistry. The samples were etched right after the Ni-InGaAs formation to prevent surface oxidation which can affect the etch rate. The sample was dipped in the etchant using a sample holder for 30 seconds. Etching was quenched with deionized water (DIW). The R_S of the sample was then measured using a four-point probe. This process was repeated using the same sample for 6 times.

3.3 Results and Discussion

3.3.1 Selective Etch of Ni over Ni-InGaAs

The plots of R_S^{-1} versus time (t) for different etch chemistries as measured by the four-point probe on the Ni-InGaAs/$In_{0.53}Ga_{0.47}As$/InP and Ni/SiO_2/Si samples are shown in Fig. 3.3. Since the p-type InGaAs has a R_S that is much higher than Ni-InGaAs, the current was assumed to flow completely through this layer. The negative slopes in the plots indicate that the R_S of the conductive films increase with etch time. The R_S of a conductive film is inversely proportional to the thickness of the film, assuming that the resistivity of the film is a constant. Fig. 3.3 indicates that the thicknesses of the films reduce linearly over time.

A cross-sectional TEM image of the Ni-InGaAs/InGaAs/InP sample after the formation of Ni-InGaAs is shown in Fig. 3.4. It was used for determining the bulk resistivity of the conductive film. The thickness of the Ni-InGaAs film ($t_{f,Ni\text{-}InGaAs}$)

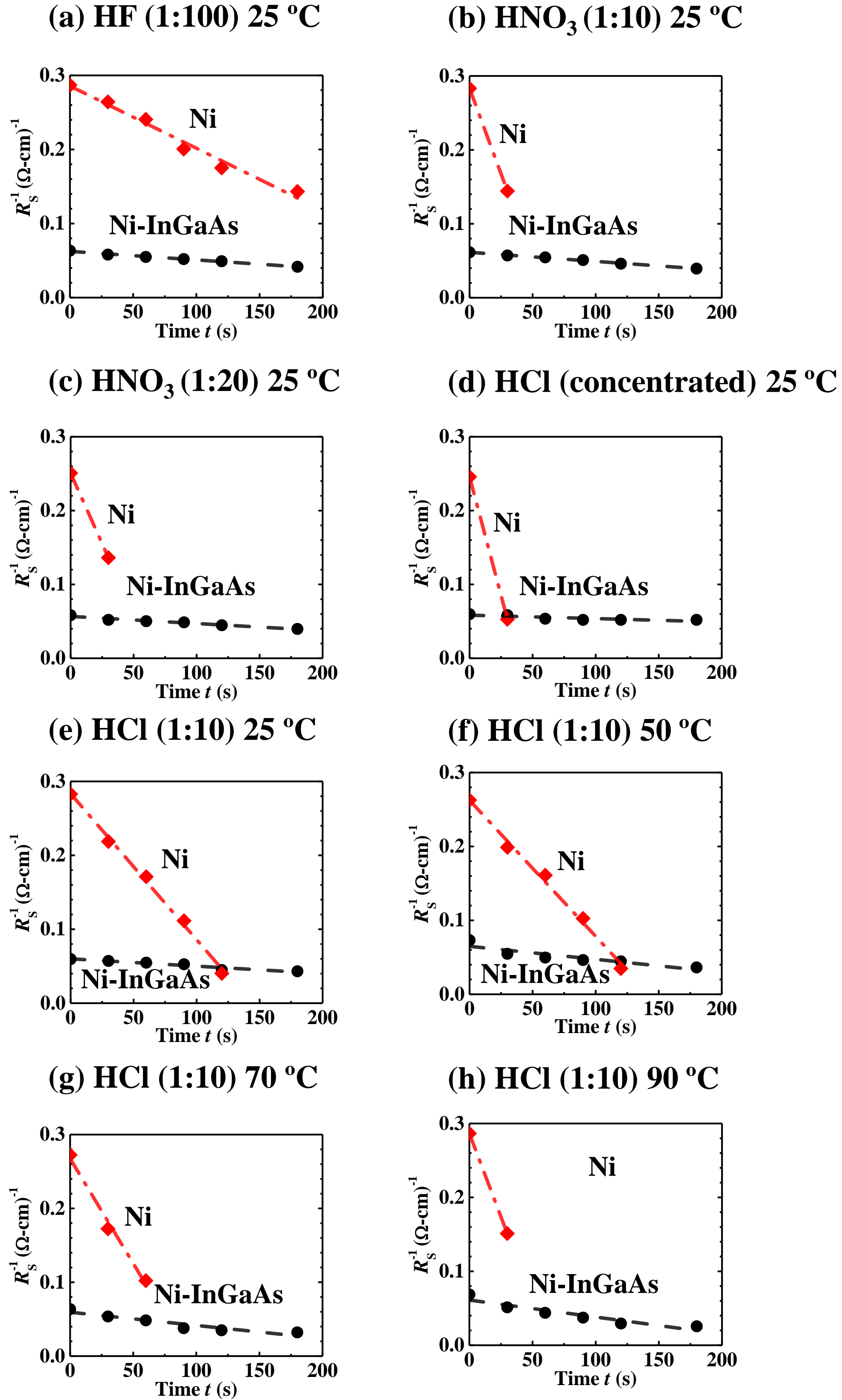


Fig. 3.3. R_S^{-1} versus time (t) plot for various etch chemistries: (a) HF:H_2O (1:100), (b) HNO_3:H_2O (1:10), (c) HNO_3:H_2O (1:20), (d) HCl (concentrated), (e) HCl:H_2O (1:10) 25 °C, (f) HCl:H_2O (1:10) 50 °C, (g) HCl:H_2O (1:10) 70 °C, (h) HCl:H_2O (1:10) 90 °C. The R_S increases with time indicating a decrease in the metal thickness.

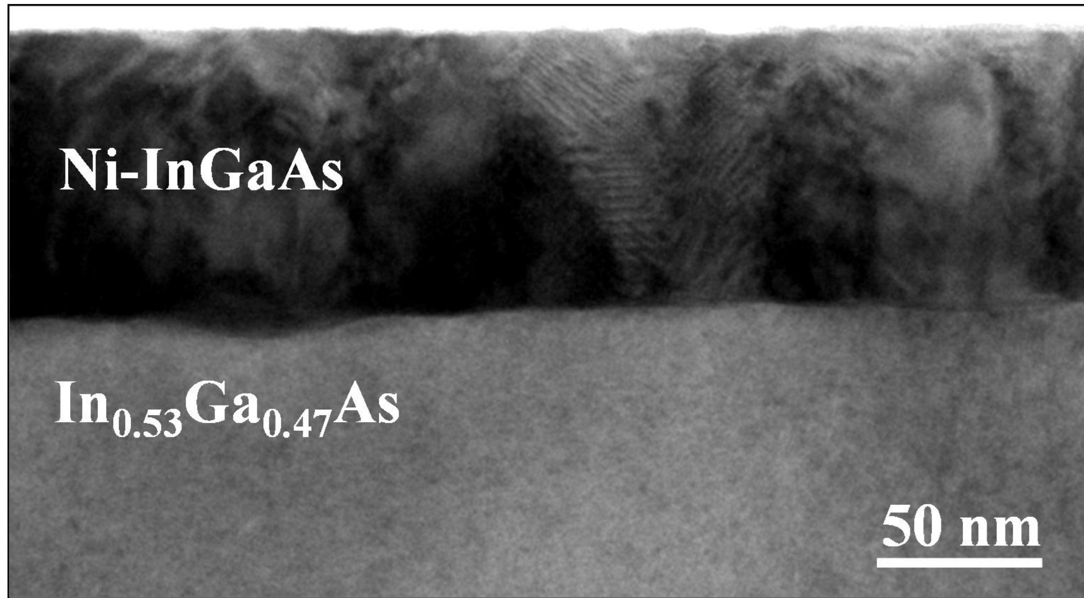


Fig. 3.4. Cross-sectional TEM image of the Ni-InGaAs formed on the $In_{0.53}Ga_{0.47}As$/InP substrate. From the image, the thickness of the Ni-InGaAs film was estimated to be 86 nm. All the TEM in this Chapter was done by a colleague, Dr. Qian Zhou.

was measured to be approximately 86 nm. The step height of the patterned Ni/SiO_2/Si sample ($t_{f,Ni}$) was measured using a surface profiler, and the thickness was found to be approximately 45 nm. Using Equation (3.1), the resistivity of bulk Ni (ρ_{Ni}) and Ni-InGaAs ($\rho_{Ni\text{-}InGaAs}$) was calculated to be 15.9 µΩ-cm and 137.7 µΩ-cm, respectively. Therefore, knowing the ρ_{Ni} and $\rho_{Ni\text{-}InGaAs}$ values and using the R_S^{-1}- t data, the thicknesses of the Ni and Ni-InGaAs films versus time during the chemical etch can be determined, as shown in Fig. 3.5.

The etch rates (in nm/minute) of the conductive films, in different etch chemistries were calculated using Equation (3.2). The etch rates for Ni in the various etchants are shown in Fig. 3.6. It was observed that HNO_3 (1:20), HNO_3 (1:10), and concentrated HCl etched the Ni film at a rapid rate of approximately 36, 44, and 61 nm/minute, respectively. HCl (1:10) etched Ni at a slower rate of about 19 nm/minute at room temperature. However, the etch rate increased as the temperature

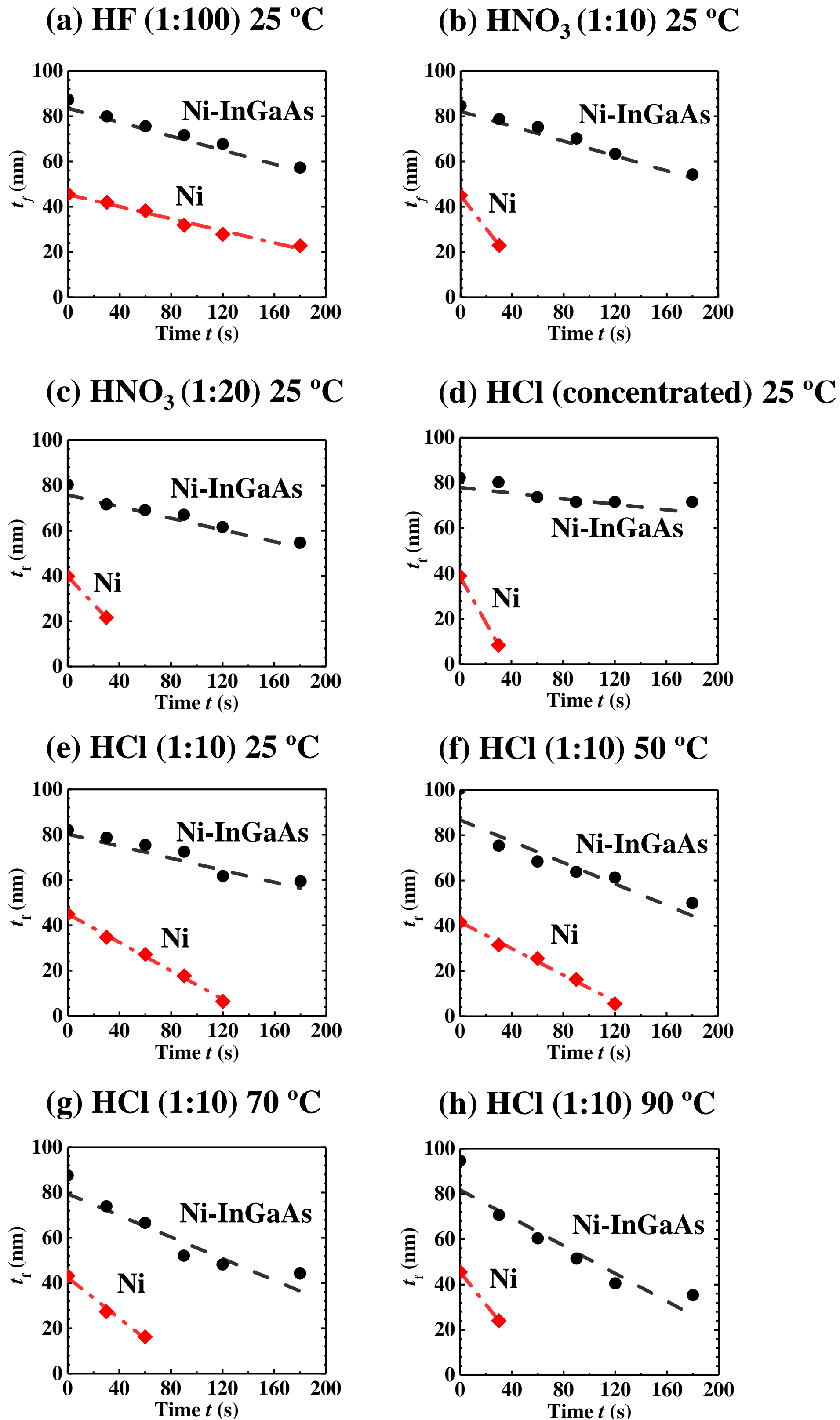


Fig. 3.5. Thickness of the metal film (t_f) versus time (t) plot for various etch chemistries: (a) HF:H_2O (1:100), (b) HNO_3:H_2O (1:10), (c) HNO_3:H_2O (1:20), (d) HCl (concentrated), (e) HCl:H_2O (1:10) 25 °C, (f) HCl:H_2O (1:10) 50 °C, (g) HCl:H_2O (1:10) 70 °C, (h) HCl:H_2O (1:10) 90 °C. The thickness can be observed to decrease with time.

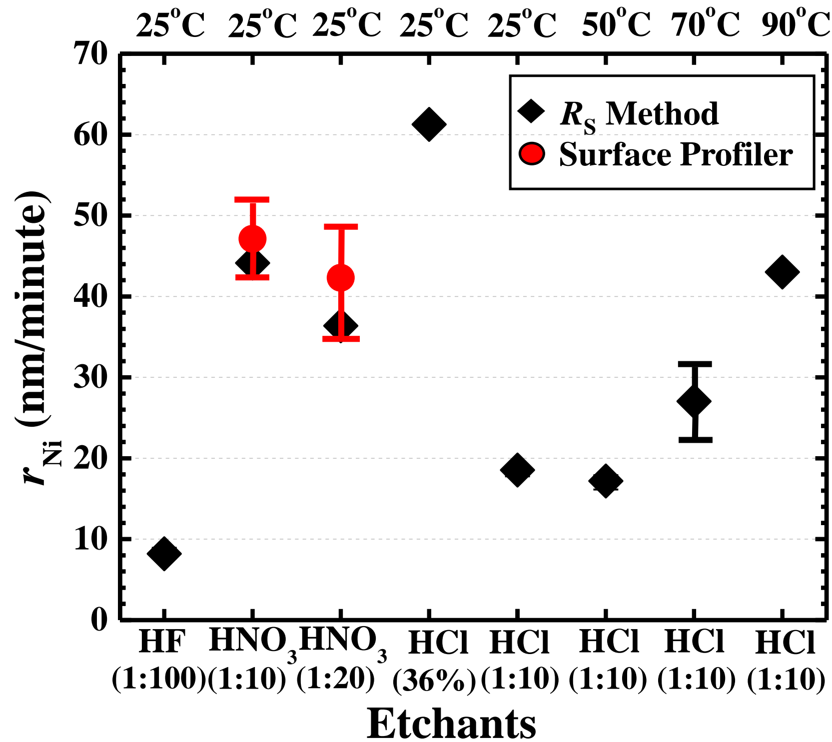


Fig. 3.6. The etch rate of Ni in the various etch chemistries which are obtained from the R_S method and from surface profiler measurements. HNO_3:H_2O (1:10), HNO_3:H_2O (1:20), HCl (concentrated) etch Ni faster compared to HCl:H_2O (1:10) chemistries. The etch rate of Ni in HCl:H_2O (1:10) increases with higher temperatures. The etch rate from the surface profiler method was slightly higher than those from the R_S method. This suggests that the etch rates could have a pattern dependence.

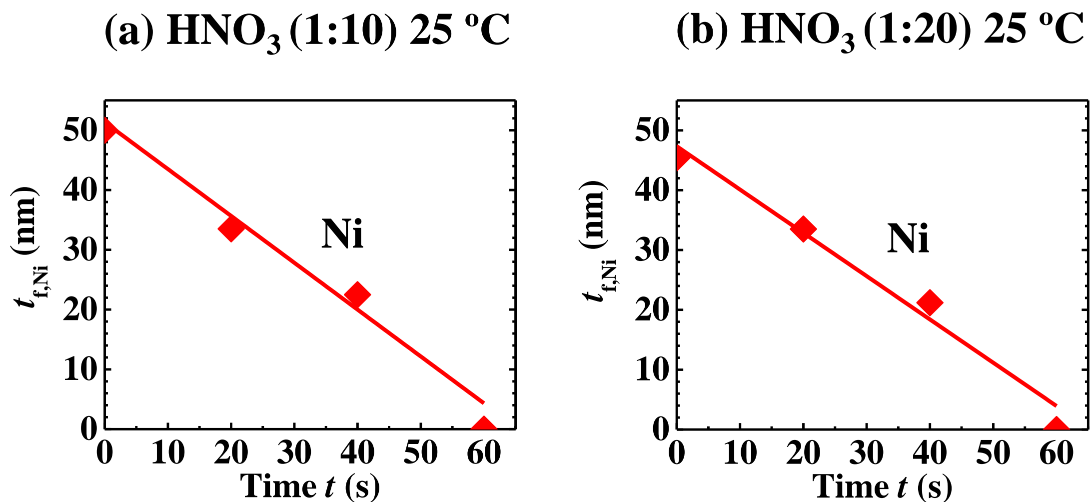


Fig. 3.7. Surface profiler measurements showing the step height of the patterned Ni sample at different times during the etching process in: (a) HNO_3 (1:10) and (b) HNO_3 (1:20).

was increased, and it was about 43 nm/minute at 90 °C. This indicates that for a particular etchant, the etch rate of Ni is a function of temperature.

Step height measurements were carried out using surface profiler on the patterned Ni samples after etching in the HNO_3 (1:10) and HNO_3 (1:20) solutions. The average value of the step heights measured on the sample was calculated. This was used to plot the thickness versus time, as shown in Fig. 3.7. The differences in etch rates obtained from the R_S method and the surface profiler can be related to the error from the surface profiler measurement due to its low resolution. The etch rates obtained are shown in Fig. 3.6. The error bar for the etch rates obtained by surface profiler measurements was large because the etch rates of the patterns at the edges are higher than those at the center of the sample.

The etch rates of Ni-InGaAs in the different etchants are plotted in Fig. 3.8. It was observed that the concentrated HCl solution etched Ni-InGaAs at a rate of (4 to 6 nm/minute) than the dilute HCl solutions. The etch rate of Ni-InGaAs in HCl (1:10) was low, around 8 nm/minute at room temperature, and increased with higher temperatures to about 20 nm/minute. This implies that the etch rate of Ni-InGaAs in an etch chemistry is a function of temperature. The etch rate of Ni-InGaAs in the HNO_3 solution depends on the ratio of HNO_3 to H_2O in the etch chemistry; HNO_3 (1:10) has a slightly higher etch rate of about 10 nm/minute compared to HNO_3 (1:20) which has an etch rate of approximately 7 to 10 nm/minute. It was also observed that Ni-InGaAs was etched in HF (1:100) with a etch rate of approximately 9 nm/minute. Different slopes can be obtained during the linear fitting of the data points (shown in Fig. 3.5) extracted from the R_S method. These gradients are plotted as error bars in Fig. 3.6 and Fig. 3.8.

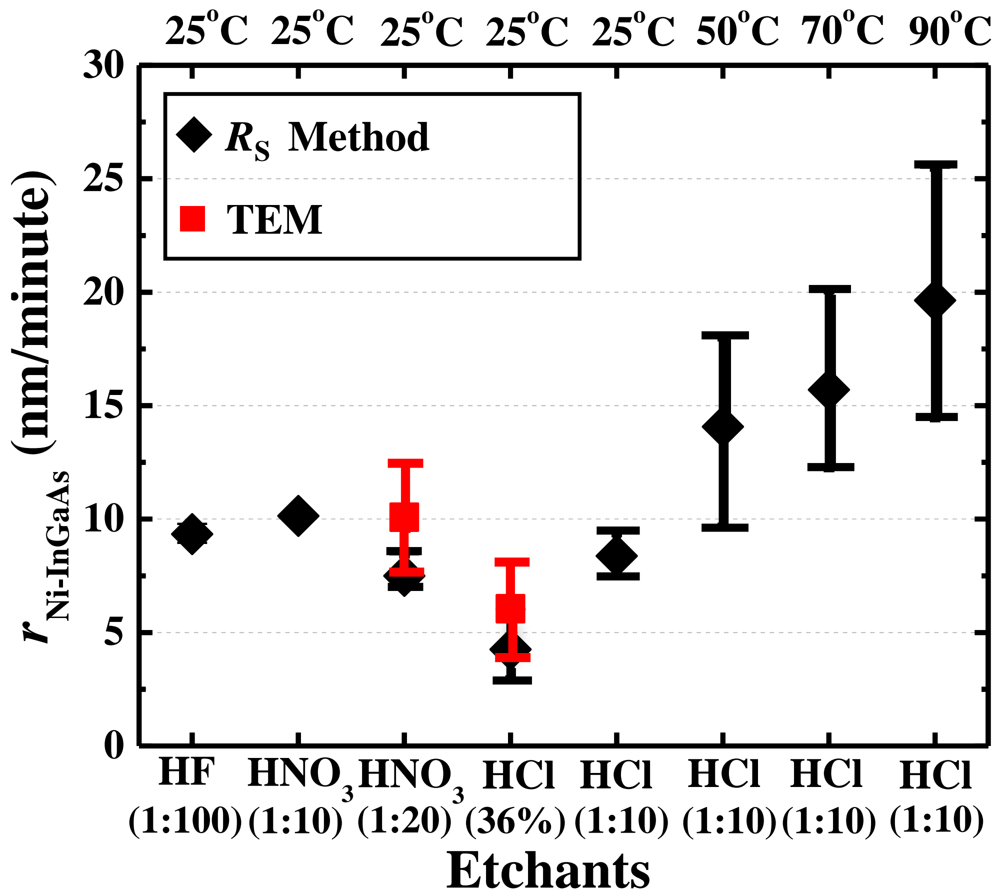


Fig. 3.8. The etch rate of Ni-InGaAs in the various etch chemistries which are obtained from the R_S method and from TEM images. HCl (concentrated) etches Ni-InGaAs the slowest. HNO_3:H_2O (1:10) etches Ni-InGaAs faster compared to HNO_3:H_2O (1:20). The etch rate of Ni-InGaAs in HCl:H_2O (1:10) at room temperature was low and it increased with higher temperatures. It was also observed that HF: H_2O (1:100) etches Ni-InGaAs at a slow rate.

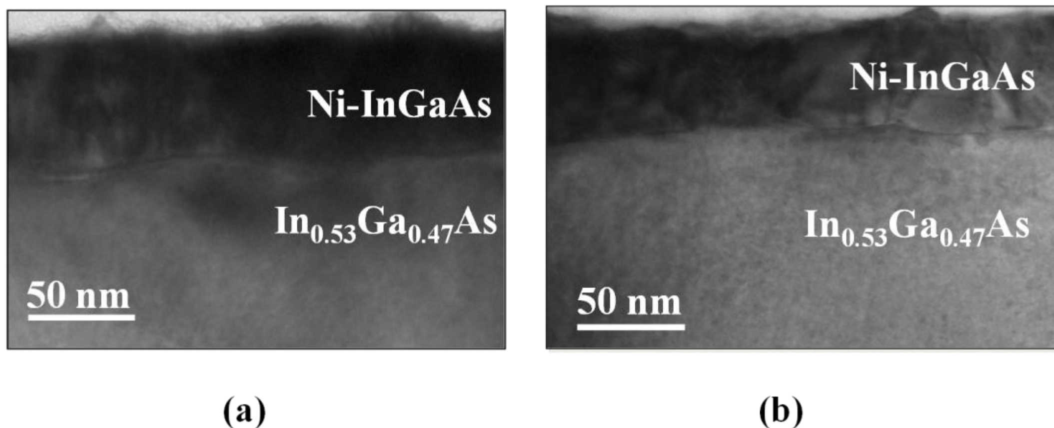


Fig. 3.9. Cross-sectional TEM images of the Ni-InGaAs remaining on the $In_{0.53}Ga_{0.47}As$/InP substrate after a 3 minute etch (at 25 °C) in: (a) HCl (concentrated) and (b) HNO_3 (1:20).

Fig. 3.9 (a) shows the cross-sectional TEM image that was obtained from the blanket Ni-InGaAs sample after etching 3 minutes in concentrated HCl, while Fig. 3.9 (b) shows the TEM image of the sample after a 3 minute etch in HNO_3 (1:20). The etch rates calculated from these TEM images are plotted in Fig. 3.8. The average value of thickness of the Ni-InGaAs layer, from different regions of the TEM was obtained. As the initial thickness of the layer (Fig. 3.4), the thickness after etching (Fig. 3.9) and duration of etching is known, the etch rate can be calculated. There was a difference in the etch rates obtained from the TEM images and the R_S method. This can be due to the roughness of the Ni-InGaAs layer after etching over the blanket sample. The roughness can be attributed to the non-uniformity in the distribution of Ni in the Ni-InGaAs layer. The error bar for the etch rates obtained from the TEM images in Fig. 3.8, was due to the deviation of the actual thickness from the average thickness of the film.

The etch selectivities obtained for various etchants are summarized in Table 3.3. Concentrated HCl gave the highest selectivity of approximately 15.6. The disadvantage of using the concentrated HCl solution is that it also etches the InP substrate; this is not an issue for InGaAs MOSFETs integrated on a silicon substrate. HNO_3 solutions give an etch selectivity of about 4.3 to 4.5. HCl (1:10) solutions give selectivities in the range of 3.2 to 2.2. At 25 °C, the etch rates of both Ni and Ni-InGaAs in HCl (1:10) are low. When the temperature was increased to 50 °C, both the etch rates increased but the selectivity was slightly reduced. As the temperature was increased beyond 50 °C, the etch rate of Ni increased faster than the etch rate of Ni-InGaAs. This resulted in an improvement in the selectivity.

Table 3.3. Etch selectivity of Ni over Ni-InGaAs in different etchants.

Chemical	Selectivity ($r_{Ni}/r_{Ni\text{-}InGaAs}$)
DHF (1:100) 25°C	0.9
HNO_3 (1:10) 25°C	4.6
HNO_3 (1:20) 25°C	4.4
36 % HCl 25°C	15.6
HCl (1:10) 25°C	2.3
HCl (1:10) 50°C	3.2
HCl (1:10) 70°C	3.8
HCl (1:10) 90°C	2.2

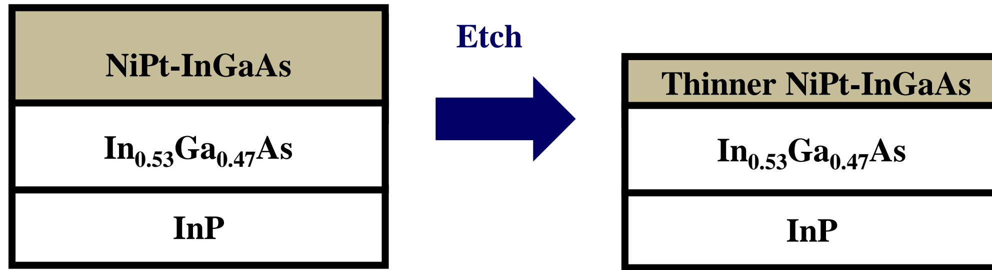
The results of this study facilitated in the selection of the etchant (concentrated HCl) that was used in the selective etch process during the fabrication of the InGaAs N-MOSFET, discussed in Chapter 4.

3.3.2 Selective Etch of NiPt over NiPt-InGaAs

(a) Sample preparation

NiPt film with ~3 atomic percentage Pt composition was used for developing the selective etch process. The NiPt film was sputtered on the samples using a single composite target. The etch rates and selectivities were obtained using the R_S measurement method. Blanket NiPt-InGaAs/$In_{0.53}Ga_{0.47}As$/InP and NiPt/Si samples were used to obtain the etch rates of NiPt-InGaAs and NiPt, respectively. This is presented in Fig. 3.10. NiPt was deposited on InGaAs/InP samples and annealed at temperatures varying from 250 to 500 °C (for 60 s) to form NiPt-InGaAs. Subsequently,

(a) NiPt-InGaAs Etch Rate obtained by Sheet Resistance Method



(b) NiPt Etch Rate obtained by Sheet Resistance Method

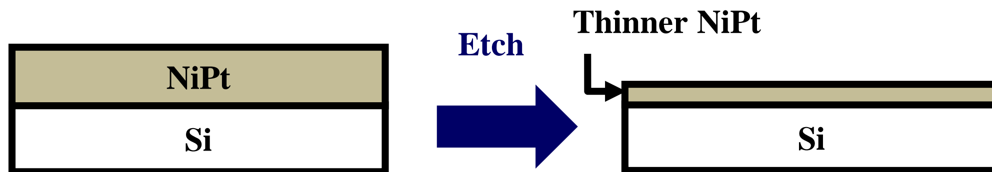


Fig. 3.10. Schematic of the samples used for determining the etch rates of NiPt-InGaAs and NiPt; (a) Blanket sample comprising of Ni-InGaAs formed on $In_{0.53}Ga_{0.47}As$/InP substrate, and (b) blanket sample comprising of NiPt deposited on a Si substrate.

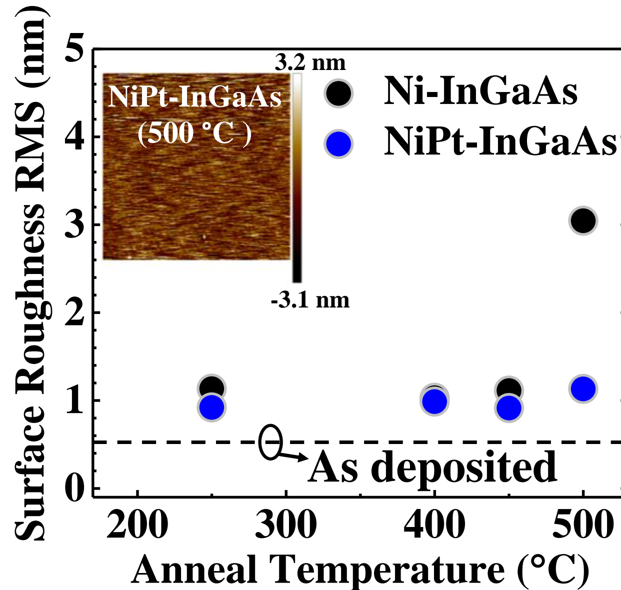


Fig. 3.11. Surface roughness of Ni-InGaAs and NiPt-InGaAs formed at different annealing temperatures. The as-deposited NiPt and Ni films are represented using the dotted line. They have similar RMS roughness. The figure in the inset shows the AFM image taken from the surface of a NiPt-InGaAs sample formed at 500 °C (50 μm × 50 μm area).

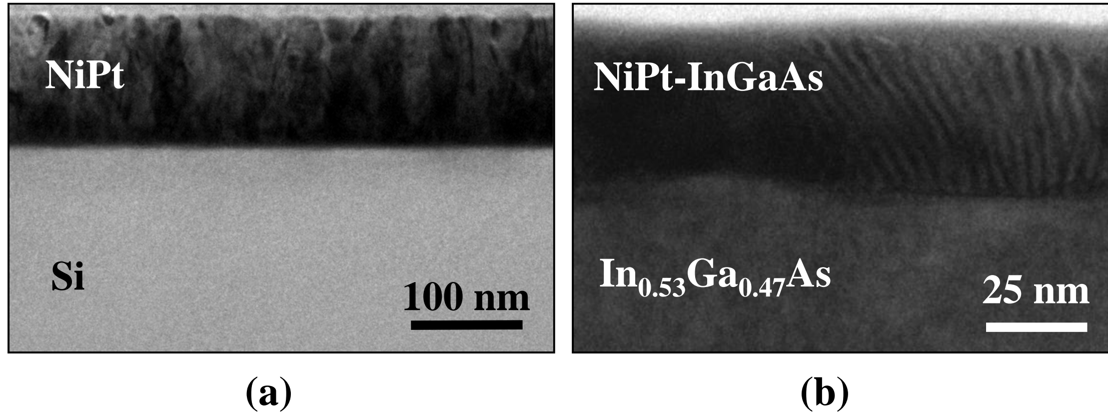


Fig. 3.12. Cross-sectional TEM images of the samples used to determine the etch rates. (a) As-deposited NiPt on Si substrate, and (b) NiPt-InGaAs formed on $In_{0.53}Ga_{0.47}As$/InP substrate.

the surface morphology of the NiPt films were characterized using Atomic Force Microscopy (AFM) measurements. Fig. 3.11 shows the comparison of surface roughness between Ni-InGaAs and NiPt-InGaAs films formed at different annealing temperatures. It can be seen that the surface roughness of Ni-InGaAs and NiPt-InGaAs are comparable at temperatures up to 450 °C. The surface of Ni-InGaAs degrades at 500 °C, as indicated by the high surface root mean square (RMS) roughness of ~ 3.1 nm. This could be a result of indium (In) or arsenic (As) out-diffusion. The NiPt-InGaAs surface remains smooth at 500 °C. This implies that the Pt incorporation improves the thermal stability of the film. This is consistent with the results for the NiPt film with higher Pt composition [248].

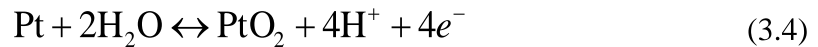
The NiPt-InGaAs film formed at 250 °C was used for determining the etch rate and selectivity. The NiPt and NiPt-InGaAs films were found to be ~96 nm and ~42 nm thick, respectively as shown in the cross-sectional TEM images in Fig. 3.12. Using Equation (3.1), the resistivity of bulk NiPt (ρ_{NiPt}) and NiPt-InGaAs ($\rho_{NiPt\text{-}InGaAs}$) were calculated to be 19.9 μΩ-cm and 179.7 μΩ-cm, respectively.

(b) Selection of chemicals for NiPt

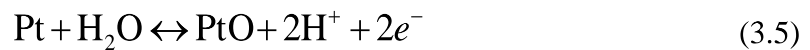
As Pt is a noble metal, aggressive acids such as Aqua Regia [250] or SPM [250], [256] are typically used for its etching. However, these solutions tend to etch InGaAs at very high rates, as mentioned in Section 3.2.2. Thus, these etchants are unsuitable for etching NiPt-InGaAs. Moreover, as the percentage of Pt (~3 %) in NiPt is still quite small, it follows that solutions based on HCl and HNO_3 (i.e. acids that etch Ni) should also successfully etch NiPt films. Furthermore, HCl and HNO_3 based chemistries have also been shown to selectively remove NiPt over NiPtSi [257]. Hence, the NiPt and NiPt-InGaAs samples were etched in HCl and HNO_3 chemistries. The effect of an HF dip on NiPt-InGaAs was also investigated. The etching mechanism of Pt in acidic solutions is discussed in the next Subsection.

(c) Mechanism of Pt etch in acidic media

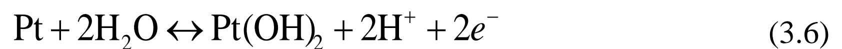
The etching of Pt is a two-step process: (1) oxidation of the Pt film to form various Pt oxides, and (2) dissolution of these oxides in the acidic solution. The oxides of Pt were studied by Sun *et al.* [258]. The postulated components of these oxides consisted of, α-Pt oxides (PtO, PtO_2) and hydrated β-Pt oxides [$Pt(OH)_2$, $Pt(OH)_4$]. The chemical reactions for the formation of these oxides under a potentiostatic condition in H_2O can be given as [256]:



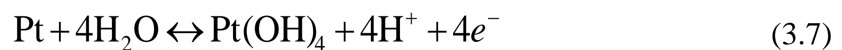
$$\mathrm{Pt} + 2\mathrm{H_2O} \leftrightarrow \mathrm{PtO_2} + 4\mathrm{H^+} + 4e^- \quad (3.4)$$



$$\mathrm{Pt} + \mathrm{H_2O} \leftrightarrow \mathrm{PtO} + 2\mathrm{H^+} + 2e^- \quad (3.5)$$



$$\mathrm{Pt} + 2\mathrm{H_2O} \leftrightarrow \mathrm{Pt(OH)_2} + 2\mathrm{H^+} + 2e^- \quad (3.6)$$

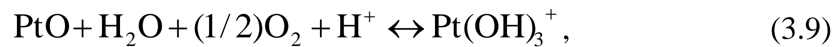


$$\mathrm{Pt} + 4\mathrm{H_2O} \leftrightarrow \mathrm{Pt(OH)_4} + 4\mathrm{H^+} + 4e^- \quad (3.7)$$

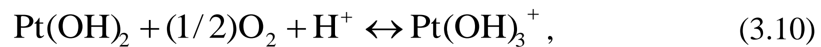
Although PtO_2 in Equation (3.4) is the most thermochemically stable phase, other oxides and hydroxides [Equations (3.5), (3.6) and (3.7] have also been detected on the surface of Pt in an aqueous solution [257]. These oxides can then be dissolved using acidic solutions.

Dissolution of Pt oxides in sulfuric acid (H_2SO_4) has been studied [259]. In this study, the valence state of the dissolved Pt in H_2SO_4 solution was found to be 4^+. Hence, the dissolved Pt oxide species was anticipated to be $Pt(OH)_3^+$. In addition, the solubility of Pt was found to be proportional to $[H^+]$ in the solution. The following reactions were suggested for the dissolution of Pt oxides and hydroxides in a H_2SO_4 based etchant (in an O_2 environment) [259]:

$$\mathrm{PtO_2 + H_2O + H^+ \leftrightarrow Pt(OH)_3^+}, \tag{3.8}$$
$$[\mathrm{Pt(OH)_3^+}] = k_{\mathrm{d1}} \cdot [\mathrm{H^+}]$$



$$\mathrm{PtO + H_2O + (1/2)O_2 + H^+ \leftrightarrow Pt(OH)_3^+}, \tag{3.9}$$
$$[\mathrm{Pt(OH)_3^+}] = k_{\mathrm{d2}} \cdot [\mathrm{H^+}] \cdot p_{\mathrm{O_2}}^{1/2}$$



$$\mathrm{Pt(OH)_2 + (1/2)O_2 + H^+ \leftrightarrow Pt(OH)_3^+}, \tag{3.10}$$
$$[\mathrm{Pt(OH)_3^+}] = k_{\mathrm{d3}} \cdot [\mathrm{H^+}] \cdot p_{\mathrm{O_2}}^{1/2}$$

where k_{d1}, k_{d2}, and k_{d3} are the equilibrium rate constants and p_{O2} is the partial pressure of O_2 in the solution. Furthermore, it was found that the solubility of Pt was enhanced when HCl was added to the H_2SO_4 solution and that the solubility of Pt was proportional to the $[Cl^-]$ in the solution. This was explained as follows: Cl^- is a well-known ligand of Pt in stable platinum-chloro-complexes (for example, chloroplatinic acid $[(H_3O)_2PtCl_6 \cdot xH_2O]$) [260]. Therefore, addition of HCl results in the additional formation of chloroplatinic complexes, which favored the forward reaction in

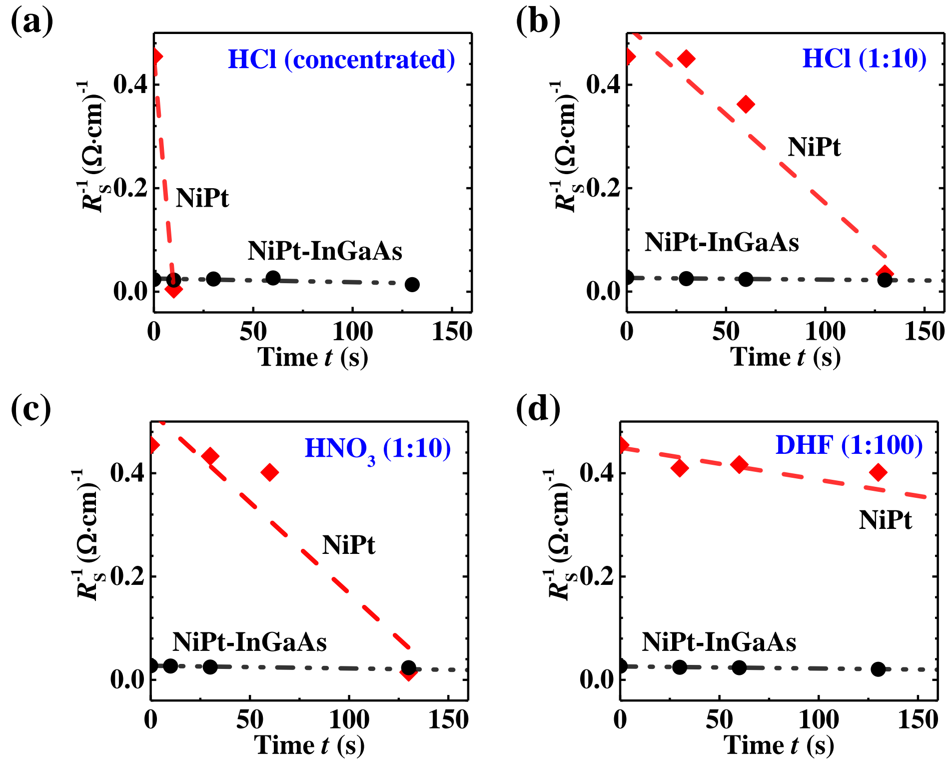


Fig. 3.13. R_S^{-1} versus time (t) plots for various etch chemistries: (a) HCl (concentrated), (b) HCl:H_2O (1:10), (c) HNO_3:H_2O (1:10), (d) HF:H_2O (1:100).

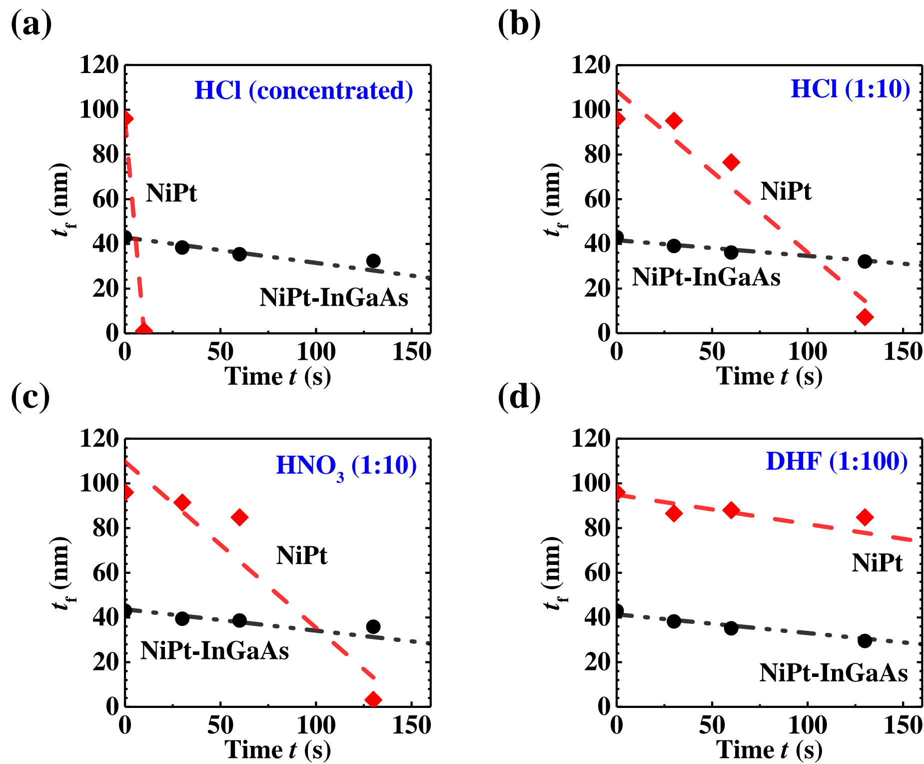


Fig. 3.14. Thickness of the metal film (t_f) versus time (t) plots for various etch chemistries: (a) HCl (concentrated), (b) HCl:H_2O (1:10), (c) HNO_3:H_2O (1:10), (d) HF:H_2O (1:100).

Equations (3.8)-(3.11). This in turn increases the solubility of Pt. These results suggested that the etch rate of NiPt will be higher compared to Ni in HCl based chemistries, as the solubility of Pt increases in the presence of Cl^- ions.

(d) Results of the experiment

Fig. 3.13 shows the R_S^{-1}-t data for both films in the various etchants. Using ρ and R_S, the t_f vs t data was obtained (as shown in Fig. 3.14). The etch rates (in nm/minute) of NiPt and NiPt-InGaAs were then calculated using Equation (3.2). This is illustrated in Fig. 3.15. The etch rates of NiPt and NiPt-InGaAs in the different etchants are shown in Fig. 3.15 (a) and 3.15 (b), respectively. The etch rates of Ni and Ni-InGaAs in the same etchants are shown for comparison. The etch rate of NiPt in concentrated HCl, HNO_3 (1:10), HCl (1:10), and HF (1:100) were ~569, 44, 41, and 7.5 nm/minute, respectively. The etch rate of NiPt films in HCl chemistries was higher compared to Ni films, whereas the etch rates in HNO_3 and HF chemistries have not changed significantly. The higher etch rate of NiPt in HCl compared to Ni, can be attributed to the enhancement of Pt etching due to the presence of Cl^- [as explained in Subsection (c)]. The etch rate of NiPt-InGaAs in the same etchants were ~11, 7, 5.6, and 6.5 nm/minute, respectively. The error bars were obtained the same way as explained in Section 3.3.1. The incorporation of Pt results in a lower etch rate for HCl and HNO_3 chemistries. This in turn aids in achieving a good selective etching process that is required for FET fabrication. The corresponding selectivities calculated using Equation (3.3) (shown in Fig. 3.16) were ~52, 6.2, and 7.3 were obtained in concentrated HCl, HNO_3 (1:10) and HCl (1:10) solutions, respectively. The higher etch selectivity for NiPt over NiPt-InGaAs compared to Ni over Ni-InGaAs provides a larger process window during the selective etch step.

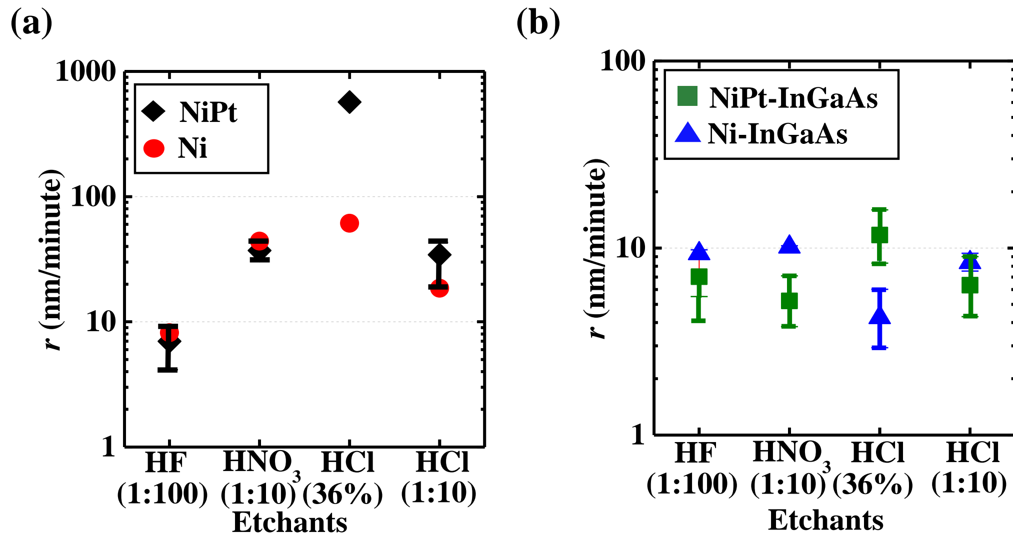


Fig. 3.15. Comparison of etch rates between (a) NiPt and Ni, and (b) NiPt-InGaAs and Ni-InGaAs using the various etch chemistries that were obtained from R_S method.

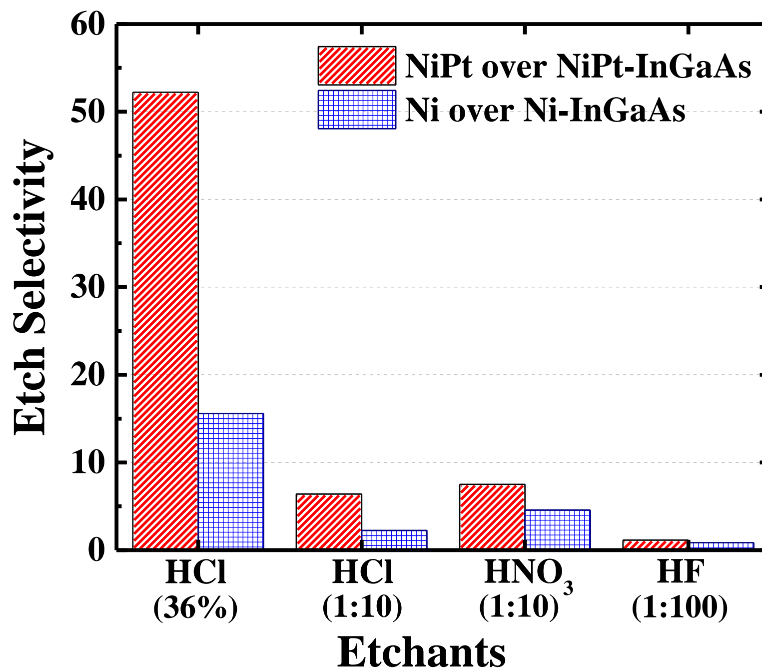


Fig. 3.16. Comparison of etch selectivities between NiPt over NiPt-InGaAs and Ni over Ni-InGaAs using various etch chemistries. The incorporation of Pt into Ni-InGaAs improves the etch selectivity of HCl and HNO_3 chemistries.

3.4 Conclusion

Self-aligned contacts are required in InGaAs MOSFETs to reduce $R_{SD.}$ Ni-InGaAs is a promising material for S/D contacts in InGaAs FETs, due its low ρ and ρ_C to n^{++}-$In_{0.53}Ga_{0.47}As$. In order to realize InGaAs N-MOSFETs with Ni-InGaAs metallic S/D, a selective etching process (to remove Ni over Ni-InGaAs was developed to study the feasibility of using Ni-InGaAs contacts in the MOSFET fabrication process. Selective etching of Ni over Ni-InGaAs using various wet etch chemistries was reported in this Chapter. The R_S method was used to obtain the etch rates and the selectivity. The results were further verified by TEM images and surface profiler measurements. HCl and HNO_3 based chemistries provided the best results. The etch rate of Ni in HNO_3 (1:20), HNO_3 (1:10), and concentrated HCl was ~36, 44, and 61 nm/minute, respectively; whereas the etch rates of Ni-InGaAs using the same wet etch chemistries were ~ 7, 10, and 4 nm/minute, respectively. Concentrated HCl was found to have the highest selectivity of approximately 15.6. HNO_3 (1:10) and HNO_3 (1:20) solutions provide good selectivities of 4.3 and 4.5, respectively. These results indicates that HCl and HNO_3 chemistries can be used for the selective etch process during contact formation in InGaAs N-MOSFET with self-aligned Ni-InGaAs source and drain. In addition, it was observed that the etch selectivity of Ni-InGaAs can be improved by the incorporation of Pt (forming NiPt-InGaAs). Higher selectivities of 52.2, 6.4, and 7.5 were obtained in concentrated HCl, HNO_3 (1:10) and HCl (1:10) solutions, respectively for NiPt over NiPt-InGaAs compare to Ni over Ni-InGaAs. The higher selectivities provides a larger process window during the selective etch process. The results from this feasibility study showed that both Ni-InGaAs and NiPt-InGaAs are viable options for self-aligned contacts in InGaAs MOSFETs.

Chapter 4

Embedded Metal Source/Drain for $In_{0.53}Ga_{0.47}As$ N-Channel Ultra-Thin Body Field-Effect Transistor

4.1 Introduction

At future technology nodes, device architectures that help in reducing parasitic resistances and capacitances are required, in order to achieve a high ON-state current (I_{ON}) and faster switching speed in MOSFETs. At aggressively scaled gate lengths (L_G), advanced device structures such as the Ultra-Thin Body Field-Effect Transistor (UTB-FET) are required for suppression of short channel effects (SCEs). One way of implementing InGaAs UTB-FET is to form an ultra-thin InGaAs-on-insulator using wafer bonding technique [261]-[269]. Another way is to epitaxially grow an ultra-thin InGaAs on a quasi-insulating material such as indium aluminium arsenide (InAlAs) which has a larger band gap compared to InGaAs. In both cases, high source/drain (S/D) resistance (R_{SD}) results from the thin S/D design [Fig. 4.1 (a)], which can be resolved by using a Raised S/D (RSD) structure [Fig. 4.1 (b)]. However, implementing an RSD results in an increase in the gate-to-drain capacitance (C_{GD}). In addition, highly n-type doped (n^{++}) InGaAs layers have to be selectively re-grown in the S/D regions during the fabrication of MOSFETs with the RSD architecture. This selective re-growth process is challenging and requires additional lithography steps, which in turn increases the process complexity. These additional processing steps reduce the throughput and increase the cost of production.

In this Chapter, an InGaAs UTB-FET with embedded Metal Source/Drain (*e*MSD) [Fig. 4.1 (c)] architecture is explored for the first time. This design can be potentially used in InGaAs N-MOSFETs to reduce R_{SD} and C_{GD}, using a simple fabrication process. The UTB-FET was realized with the help of the selective etching process that was explained in the previous Chapter. An InAlAs barrier layer below the ultra-thin InGaAs was used as a quasi-insulating material to suppress the sub-surface source-to-drain leakage current (I_{SS}). InAlAs was selectively converted to a metallic material (Ni-InAlAs) in the S/D regions to achieve a thick *e*MSD, which helps to reduce R_{SD} without increasing C_{GD}. The impact of using an *e*MSD architecture in InGaAs

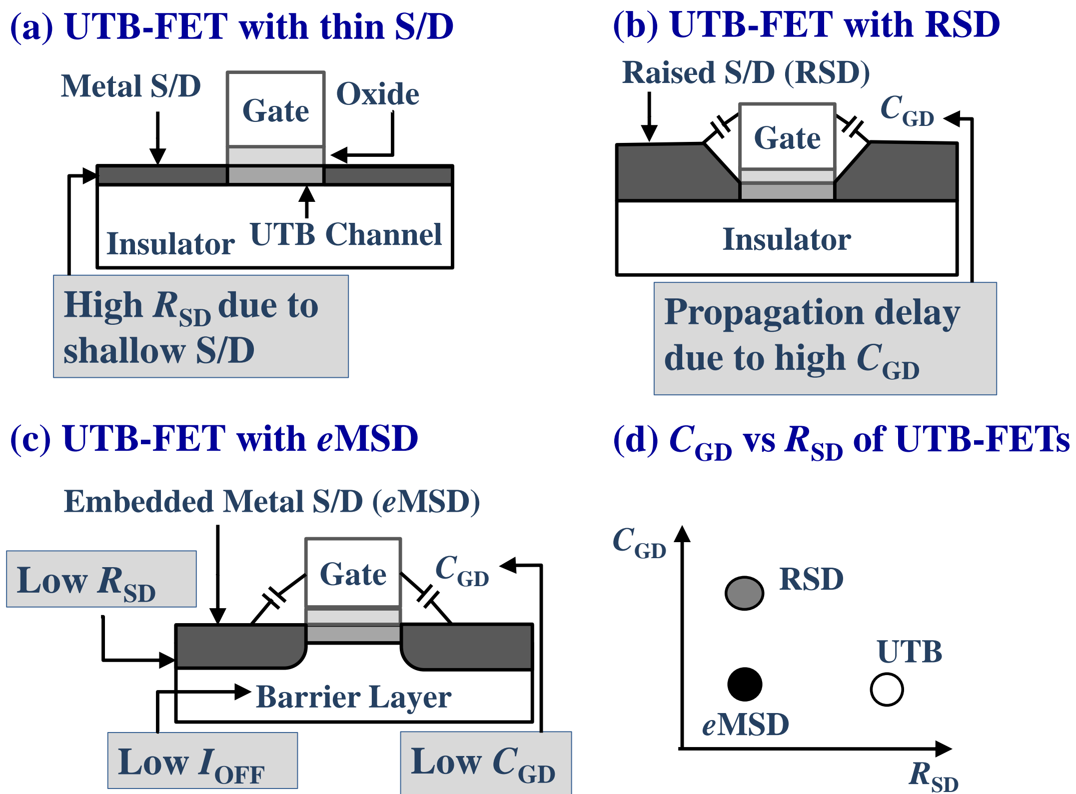


Fig. 4.1. (a) UTB-FET with thin S/D suffers from a high R_{SD}. (b) It can be resolved by using a UTB-FET with a Raised S/D structure (RSD). However, this increases the number of process steps during device fabrication and increases the C_{GD}; thus, reducing the switching speed of the transistor. (c) Both problems can be resolved using the UTB-FET with embedded metal S/D (*e*MSD). (d) C_{GD}-R_{SD} of UTB-FETs. UTB-FET with *e*MSD provides a low R_{SD} without compromising C_{GD}.

UTB- FETs at future technology nodes is discussed in Section 4.3 of this Chapter. The parasitic resistance and capacitance components in the various architectures shown in Fig. 4.1, were obtained using Technology Computer Aided Design (TCAD) simulations. The advantages of using *e*MSD architecture are also highlighted.

4.2 InGaAs UTB-FET with an *e*MSD Architecture

4.2.1 Formation of Ni-InAlAs

To realize the InGaAs UTB-FETs with an *e*MSD, it was important to confirm if Nickel (Ni) reacts with InAlAs to form Ni-InAlAs alloy. The procedure used to verify this result is illustrated in Fig. 4.2. The starting substrates consisted of 500 nm thick $In_{0.53}Ga_{0.47}As$ with a p-type doping concentration (N_A) of 5×10^{16} cm^{-3} on an InP

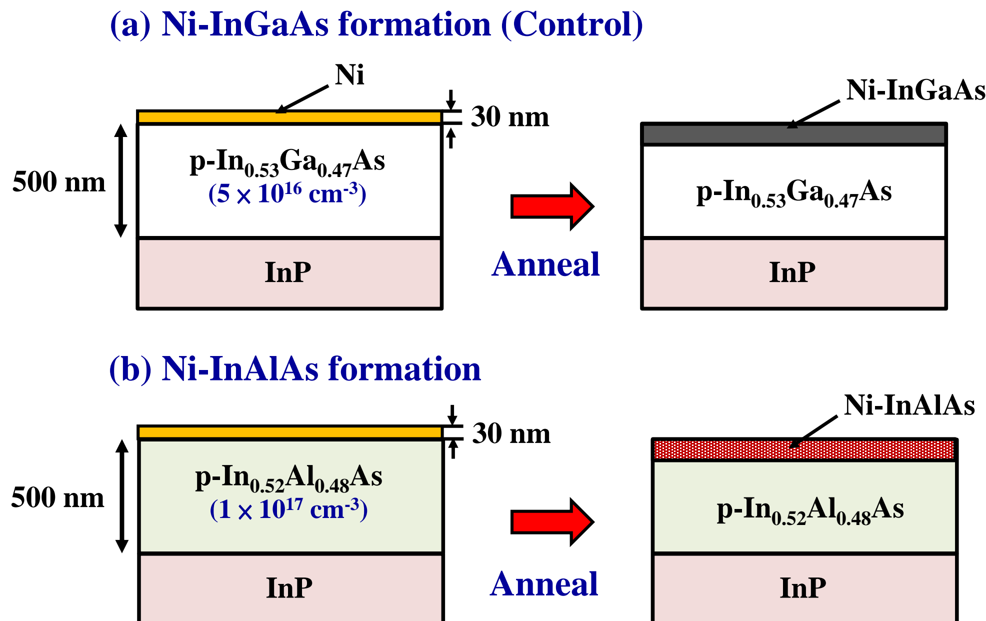


Fig. 4.2. Schematic illustrating the samples used for investigating the reaction of Ni with InAlAs. (a) ~30 nm thick Ni was deposited on unpatterned $In_{0.53}Ga_{0.47}As$/InP (control sample) and reacted to form Ni-InGaAs. (b) ~30 nm thick Ni was deposited on unpatterned $In_{0.52}Al_{0.48}As$/InP and reacted to form Ni-InAlAs. The formation temperature was varied from 200 °C to 400 °C (in steps of 50 °C). Sheet resistance (R_S) of Ni-InGaAs and Ni-InAlAs alloys were extracted using four-point-probe measurements.

substrate [Fig. 4.2 (a)], and 500 nm thick $In_{0.58}Al_{0.42}As$ with N_A of 1×10^{17} cm^{-3} on an InP substrate [Fig. 4.2 (b)]. The samples were first cleaned using diluted hydrofluoric acid (DHF). Subsequently, ~30 nm Ni was deposited on both the substrates. The Ni thickness was carefully chosen to ensure that neither the InGaAs nor the InAlAs layer was fully consumed during the reaction. The samples were annealed using a rapid thermal process to form Ni-InGaAs and Ni-InAlAs. The alloy formation temperature was varied from 200 °C to 400 °C (in steps of 50 °C). The sheet resistance (R_S) of the metallic alloys were then extracted using four-point-probe measurements. The comparison of R_S between Ni-InGaAs and Ni-InAlAs, formed using different annealing temperatures, are shown in Fig. 4.3. Similar to the case of Ni-InGaAs, the reaction between Ni and InAlAs occurs at annealing temperatures of 250 °C and above. It can be observed that the R_S of Ni-InAlAs is comparable to that of Ni-InGaAs over the full range of annealing temperatures.

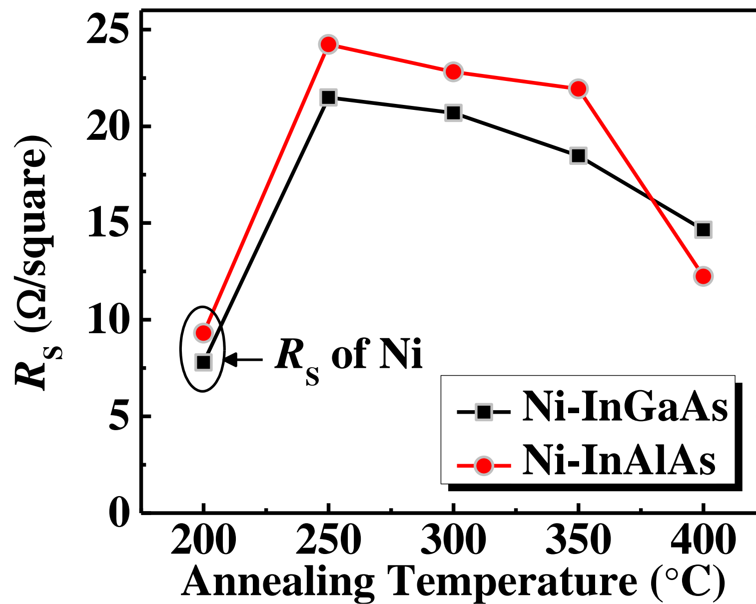


Fig. 4.3. R_S of Ni-InGaAs and Ni-InAlAs alloys formed using different annealing temperatures. R_S of both the alloys are comparable.

4.2.2 Device Fabrication

Fig. 4.4 summarizes the process flow used to fabricate InGaAs UTB-FETs with *e*MSD. The starting substrate consisted of epitaxially grown p-type InGaAs (10 nm) and InAlAs on a p-type bulk InP wafer. The N_A of InGaAs and InAlAs are the same as mentioned in the previous Section. The InGaAs and InAlAs layers were lattice matched to the InP substrate. Pre-gate cleaning was performed using hydrochloric acid (HCl) and ammonium hydroxide (NH_4OH) solutions for native oxide removal. The sample was then immersed in ammonium sulfide $(NH_4)_2S_x$ solution for surface passivation, which was done to suppress the surface oxidation which occurs while transferring the sample to the atomic layer deposition (ALD) chamber for gate dielectric deposition. A ~6 nm thick aluminum oxide (Al_2O_3) layer was deposited using the ALD, which was followed by a post-deposition anneal at 300 °C for 60 s. A ~100 nm thick tantalum nitride (TaN) layer was then sputtered and patterned using optical lithography. Dry etching in chlorine (Cl_2) based plasma completed the metal gate formation. The sample was subsequently dipped in DHF ($HF:H_2O$ = 1:100) to remove Al_2O_3 on the S/D regions. Next, ~35 nm of Ni was deposited using e-beam evaporator. The sample was annealed at 250 °C for 90 s after the Ni deposition to form the Ni-InGaAs/Ni-InAlAs *e*MSD. The last step of the process involved the selective removal of Ni from the gate sidewalls (to isolate the gate from the S/D). The selective etch was carried out using concentrated HCl due to its high selectivity in etching Ni over Ni-InGaAs (as shown in Chapter 3).

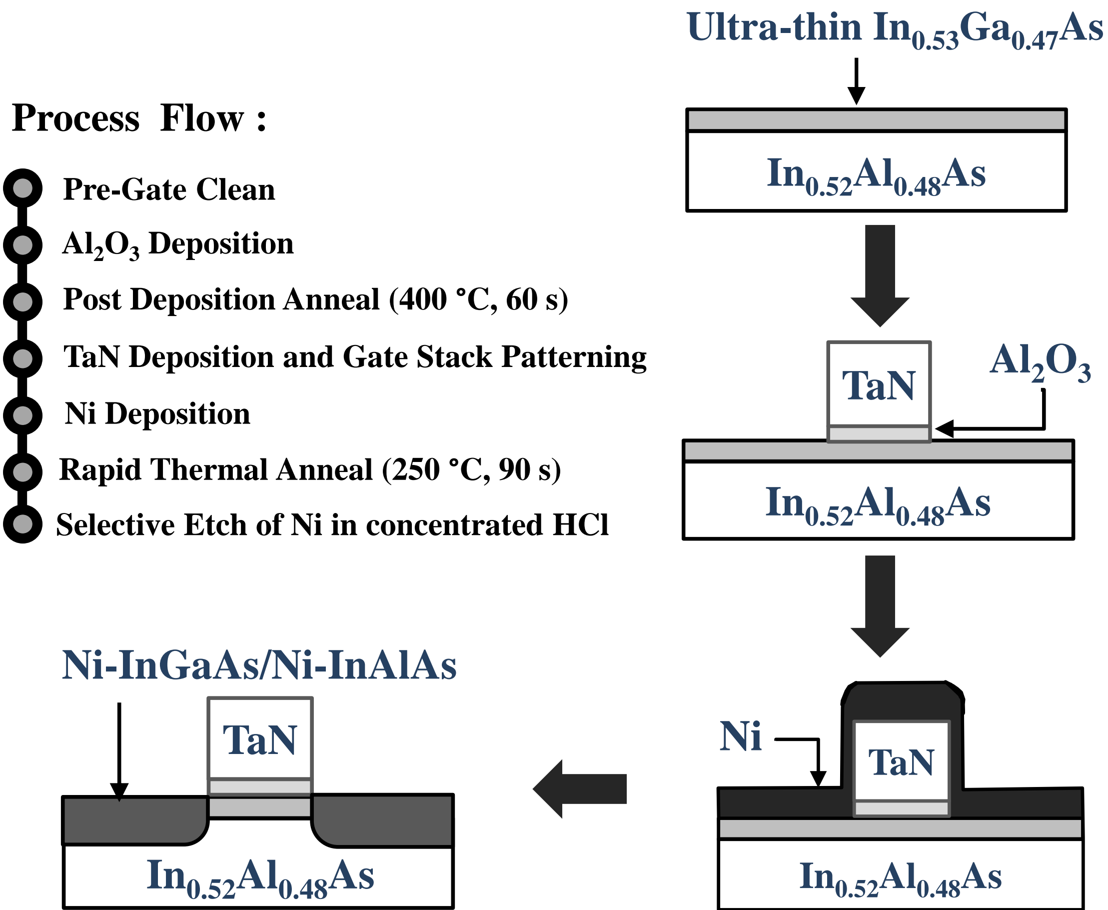


Fig. 4.4. Process flow for the fabrication of an n-channel InGaAs UTB-FET with self-aligned *e*MSD. The S/D was formed by depositing ~35 nm of Ni, which was then annealed to form Ni-InGaAs/Ni-InAlAs *e*MSD.

The layout and top-view Scanning Electron Microscopy (SEM) image of a UTB-FET with *e*MSD are shown in Fig. 4.5 (a) and (b), respectively. The UTB-FET has an L_G = 2 μm and gate width (W_G) of 50 μm. The cross-section along A-A' of the transistor [Fig. 4.5 (b)] was captured using Transmission Electron Microscopy (TEM) [Fig. 4.5 (c)]. A magnified view of the gate and S/D regions [highlighted in Fig. 4.5 (c)] is illustrated in Fig. 4.5 (d). The as-deposited Ni thickness was large enough to consume the entire InGaAs layer as well as part of the InAlAs layer to form ~65 nm of the Ni-InGaAs/Ni-InAlAs *e*MSD. A high-resolution TEM image of the TaN/Al_2O_3/InGaAs/InAlAs stack is shown in Fig. 4.5 (e). The thickness of the

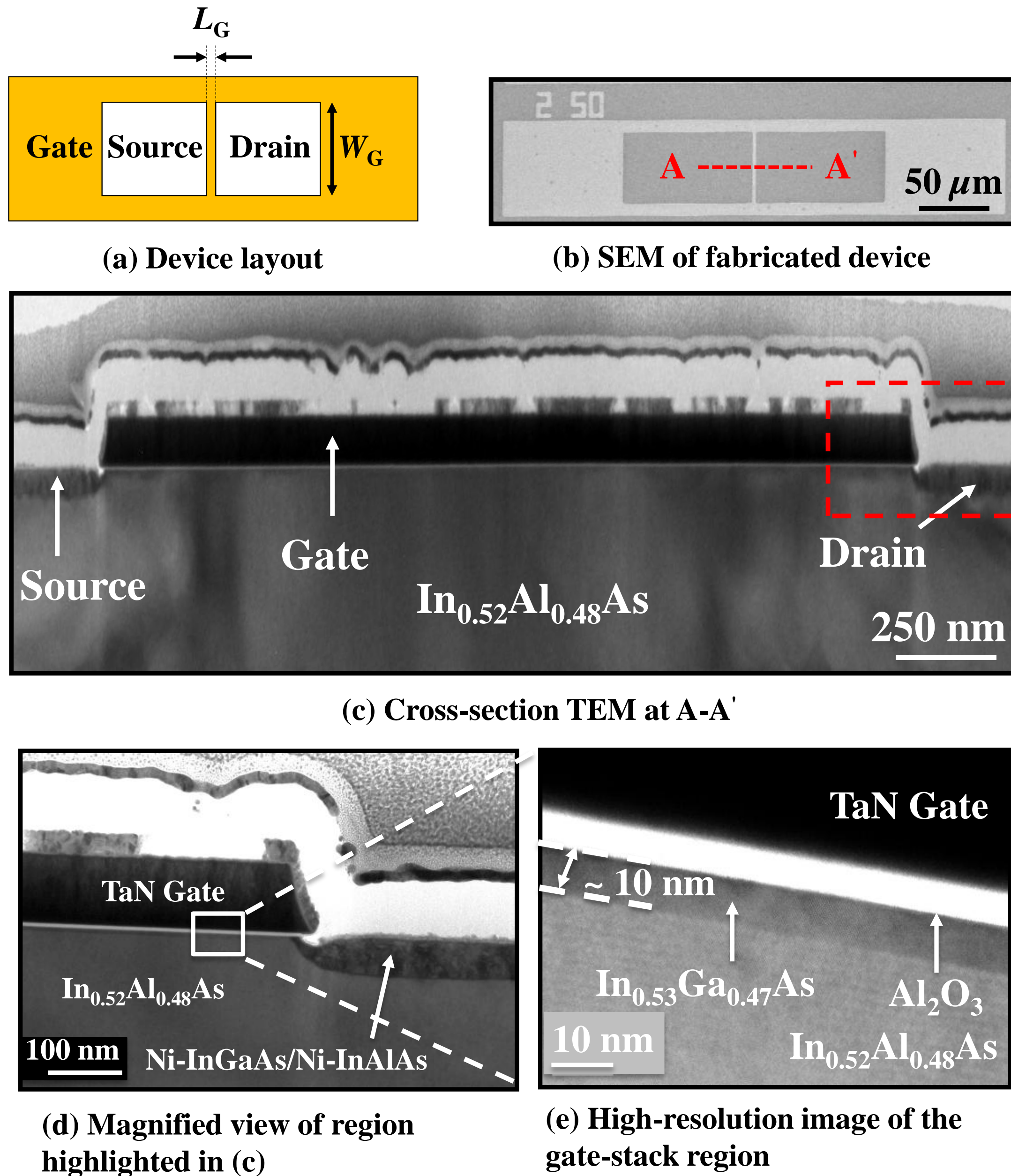


Fig. 4.5. (a) Device layout, and (b) top-view SEM image of the fabricated UTB-FET. (c) The cross-sectional TEM image (along A-A') of the UTB-FET with self-aligned *e*MSD. (d) A magnified view of the gate and drain regions, and (e) an HR-TEM image of the TaN/Al_2O_3/InGaAs/InAlAs stack. The ultra-thin InGaAs channel layer was 10 nm thick and the Ni-InGaAs/Ni-InAlAs *e*MSD layer was ~65 nm thick.

ultra-thin InGaAs channel and Al_2O_3 gate dielectric were ~10 nm and ~6 nm, respectively. The TEM was done at the Institute of Materials Research and Engineering (IMRE) as a paid service. The fabricated devices were then electrically characterized.

4.2.3 Results and Discussion

Drain current (I_D), and gate leakage current (I_G) are plotted versus gate voltage (V_{GS}) for a UTB-FET with *e*MSD having $L_G = 2$ µm and $W_G = 50$ µm at applied drain voltage (V_D) of 0.1 and 1.2 V [shown in Fig. 4.6 (a)]. A saturation threshold voltage ($V_{T,Sat}$) of ~0.25 V was obtained using a constant current method with a fixed current level of 10 µA/µm. The device shows good transfer characteristics, low OFF-state current (I_{OFF}), high I_{ON}/I_{OFF} ratio of ~10^6, and subthreshold swing (S) of 125 mV/decade. The S can be further improved by scaling the equivalent oxide thickness (EOT) and by improving the interface quality between the gate dielectric and the channel. The gate-dielectric interface can be improved by reducing the interface trap density (D_{it}). It can be extracted using the following equation [165]:

$$D_{it} = \frac{C_{OX}}{q} \cdot \left(\frac{q \cdot S}{2.3 \cdot K \cdot T} - 1 \right) - \frac{C_{InGaAs}}{q}, \qquad (4.1)$$

where K is the Boltzmann constant, T is the temperature, and q is the elementary charge. C_{OX} and C_{InGaAs} are the gate oxide capacitance and the InGaAs channel capacitance, respectively. C_{OX} was calculated by the parallel plate capacitance formula, using a relative permittivity (κ) of 7.9, and oxide thickness (T_{OX}) of 6 nm. Similarly, C_{InGaAs} was calculated using $\kappa = 13.9$, and InGaAs thickness $T_{InGaAs} = 10$ nm. Using Equation (4.1), the D_{it} value was estimated to be $\sim 1.53 \times 10^{12}$ states/eV^{-1} cm^{-2}. D_{it} needs to be reduced further to improve the S. For instance, a lower D_{it} can be achieved by using a buried InGaAs channel with an InP capping layer and a $TaSiO_x$ gate dielectric [270].

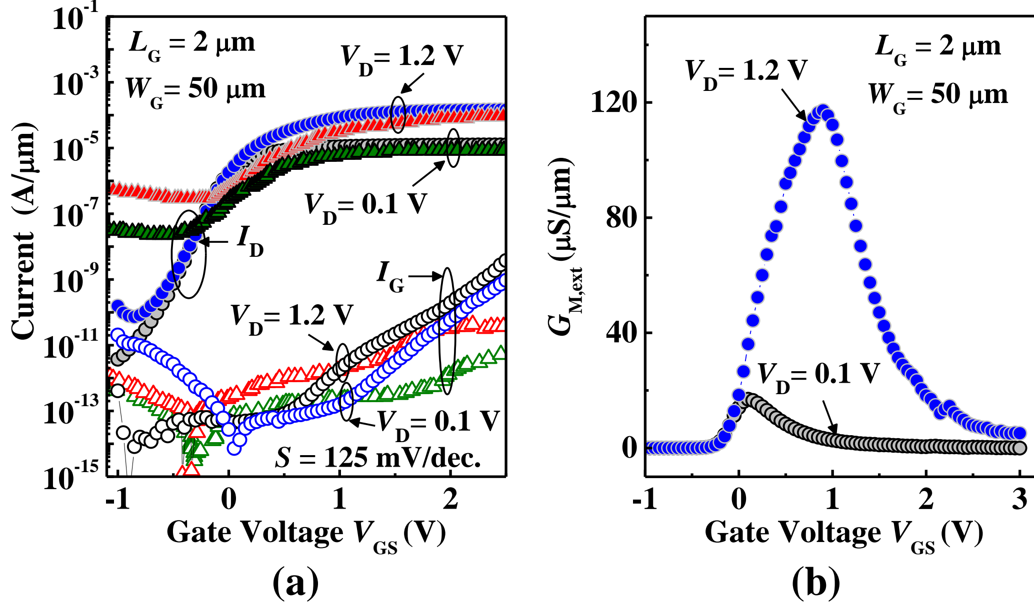


Fig. 4.6. (a) I_D, I_G versus V_{GS} for bulk-InGaAs MOSFET (triangles) and UTB-FET (circles), and (b) $G_{M,ext}$-V_{GS} curves of a UTB-FET with *e*MSD. I_{ON}/I_{OFF} ratio of ~10^6 and a peak $G_{M,ext}$ of 118 µS/µm at V_D =1.2 V were obtained.

The device exhibits an I_{ON} of ~140 µA/µm at gate overdrive (V_{GS} - V_T) of 2 V. The low I_{OFF} observed was due to presence of the InAlAs barrier layer that reduces I_{SS}.

Fig. 4.6 (b) shows the extrinsic transconductance ($G_{M,ext}$) of the UTB-FET with *e*MSD. A peak $G_{M,ext}$ value of 118 µS/µm (at V_D = 1.2 V) was measured. The peak intrinsic transconductance ($G_{M,int}$) was then derived by taking out the effect of R_{SD} using [271]:

$$G_{M,int} = \frac{G_M^0}{1-(R_{SOURCE}+R_{DRAIN})\cdot G_D\cdot(1+R_{SOURCE}\cdot G_M^0)}, \tag{4.2}$$

where

$$G_M^0 = \frac{G_{M,ext}}{1-R_{SOURCE}\cdot G_{M,ext}}, \tag{4.3}$$

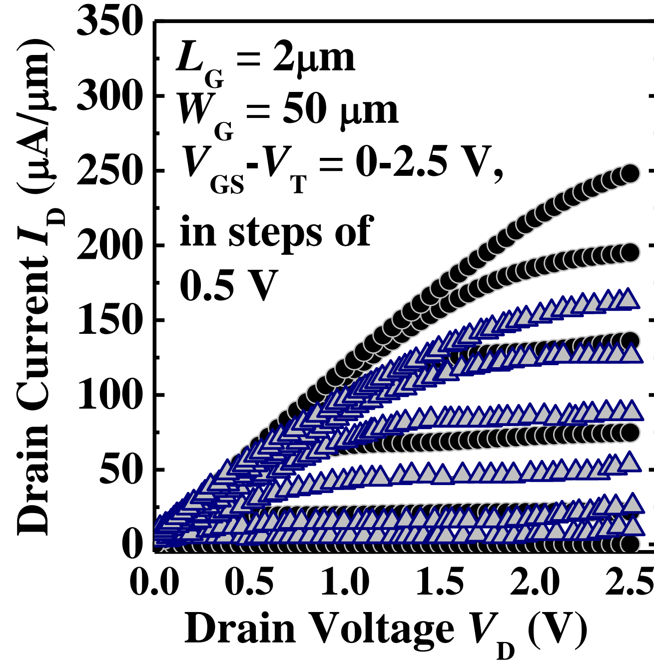


Fig. 4.7. I_D-V_D plot for bulk-InGaAs MOSFET (triangles) and UTB-FET with *e*MSD (circles). Gate overdrive (V_{GS}-V_T) was varied from 0 to 2.5 V in steps of 0.5 V.

where R_{SOURCE} and R_{DRAIN} are the resistances of source and drain, respectively. In a long channel device, the measured drain conductance G_D ($\partial I_D/\partial V_D$) is negligible and hence $G_{M,int}$ equals to G_M^0. The extracted value for peak $G_{M,int}$ was ~223 μS/μm at V_D = 1.2 V. $G_{M,int}$ is free from R_{SD} and is directly related to the carrier mobility in the InGaAs channel. Fig. 4.7 shows the I_D-V_D characteristics of the UTB-FET with *e*MSD at various gate overdrives from 0 to 3 V in steps of 0.5 V. The device demonstrates good saturation and pinch-off characteristics.

In Fig 4.8 (c), current-voltage (*I*-*V*) characteristics of the source-to-drain back-to-back diode measured from the UTB-FET with *e*MSD [Fig. 4.8 (b)] is compared with that from a bulk InGaAs N-MOSFET with Ni-InGaAs S/D (fabricated in a different experiment) [Fig. 4.8 (a)]. The current *I* (A/μm) was normalized by W_G for both the devices. The reverse leakage current of the diode with the InAlAs barrier (i.e. the *e*MSD structure) was ~3 orders of magnitude lower than that without the InAlAs barrier layer. This indicates that the Schottky contact at the Ni-InAlAs/InAlAs

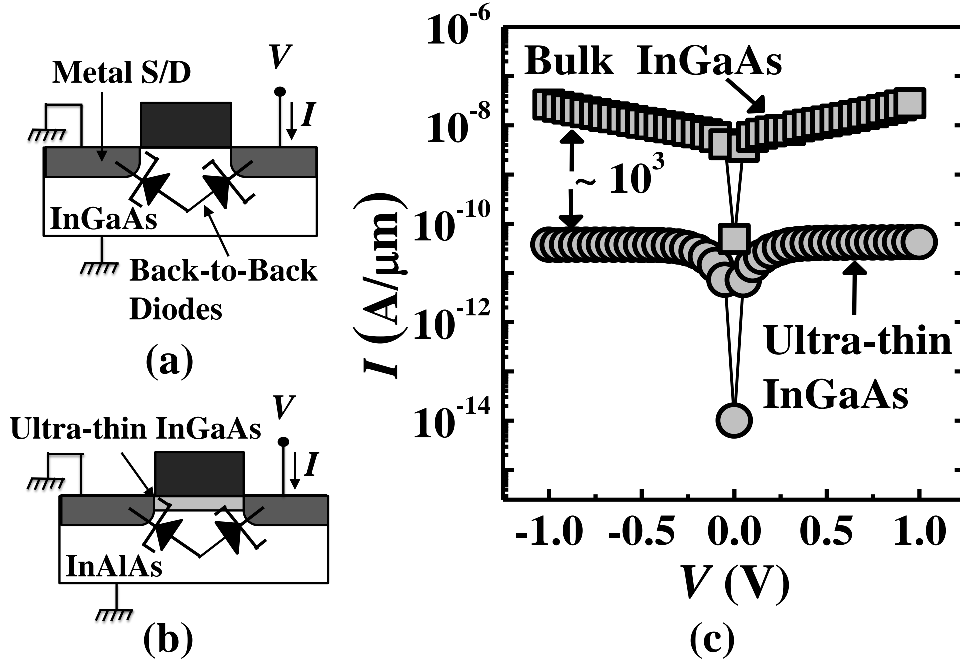


Fig. 4.8. Schematics of back-to-back diodes formed on (a) bulk-InGaAs/InP, and (b) on ultra-thin InGaAs/InAlAs *e*MSD layer. (c) *I-V* curves show a ~10^3 reduction in reverse current due to the presence of the InAlAs barrier layer [Energy band gap (E_G) = 1.48 eV].

interface results in significantly reduced reverse leakage current as compared to that at the Ni-InGaAs/InGaAs interface. This can be attributed to the higher hole Schottky barrier height ($\phi_{B,P}$) at the Ni-InAlAs/p-InAlAs interface compared to the Ni-InGaAs/p-InGaAs interface.

TCAD simulations (using Sentaurus) were used to obtain the hole Schottky barrier height of Ni-InAlAs on p-$In_{0.52}Al_{0.48}As$ ($\phi_{B,P,InAlAs}$). Fig. 4.9 (a) and (b) show the schematics of the back-to-back diodes simulated on bulk InGaAs/InP and UTB-InGaAs/InAlAs/InP structures, respectively. The dimensions and parameters (such as N_A) of the structures simulated were chosen to match that of the actual fabricated devices. In these simulations, a thermionic *I-V* model was used for the metal-semiconductor junction, and is given by the following equations [165]:

$$I = I_S \cdot \left(e^{q \cdot V / \eta \cdot K \cdot T} - 1 \right), \tag{4.4}$$

and $$I_S = A_D \cdot A^* \cdot T^2 \cdot e^{-q \cdot \phi_B / K \cdot T},\qquad (4.5)$$

where I_S is the saturation current, A_D is the area of the diode, A^* is the Richardson's constant, ϕ_B is the effective barrier height, and η is the ideality factor. The tunneling current component was neglected in both the structures due to the low N_A of the p-InGaAs and p-InAlAs layers [165]. Furthermore, the metal-semiconductor junction is assumed to be defect free. For the back-to-back diodes on the bulk-InGaAs/InP structure, 0.5 eV hole Schottky barrier height for Ni-InGaAs on InGaAs ($\phi_{B,P,InGaAs}$) was calculated from the energy band gap of $In_{0.53}Ga_{0.47}As$ (0.74 eV) [272] and the electron Schottky barrier height $\phi_{B,N}$ (0.24 eV) [231] for Ni-InGaAs on InGaAs. *I-V* characteristics obtained from the simulations [red circles in Fig. 4.9 (c)] was consistent with the experimental results. The corresponding energy band diagram (at equilibrium) at the Ni-InGaAs/InGaAs interface (across B-B') is shown in Fig. 4.9 (d).

The structure shown in Fig. 4.9 (b) was used to extract $\phi_{B,P,InAlAs}$. There are two different Schottky barriers in this structure: (i) $\phi_{B,P,InGaAs}$ between Ni-InGaAs and the 10 nm $In_{0.53}Ga_{0.47}As$ layer on top of the sample, and (ii) $\phi_{B,P,InAlAs}$ between Ni-InAlAs and the $In_{0.52}Al_{0.48}As$ barrier layer. The simulations were performed with $\phi_{B,P,InGaAs}$ fixed at 0.5 eV [based on Fig. 4.9 (c)] and $\phi_{B,P,InAlAs}$ was varied to match the *I-V* curves with the experimental results depicted in Fig. 4.8 (c). *I-V* curves from the simulation matched the experimental results at $\phi_{B,P,InAlAs}$ = 0.65 eV [Fig. 4.9 (e)]. The $\phi_{B,P}$ for various metals on p-$In_{0.52}Al_{0.48}As$ is typically in the range of 0.6 to 0.8 eV [273]-[277]. The $\phi_{B,P,InAlAs}$ extracted using the simulation was consistent with these results. The corresponding energy band diagram (at equilibrium) for $\phi_{B,P,InAlAs}$ = 0.65 eV at the Ni-InAlAs/InAlAs interface (across C-C') is shown in Fig. 4.9 (f).

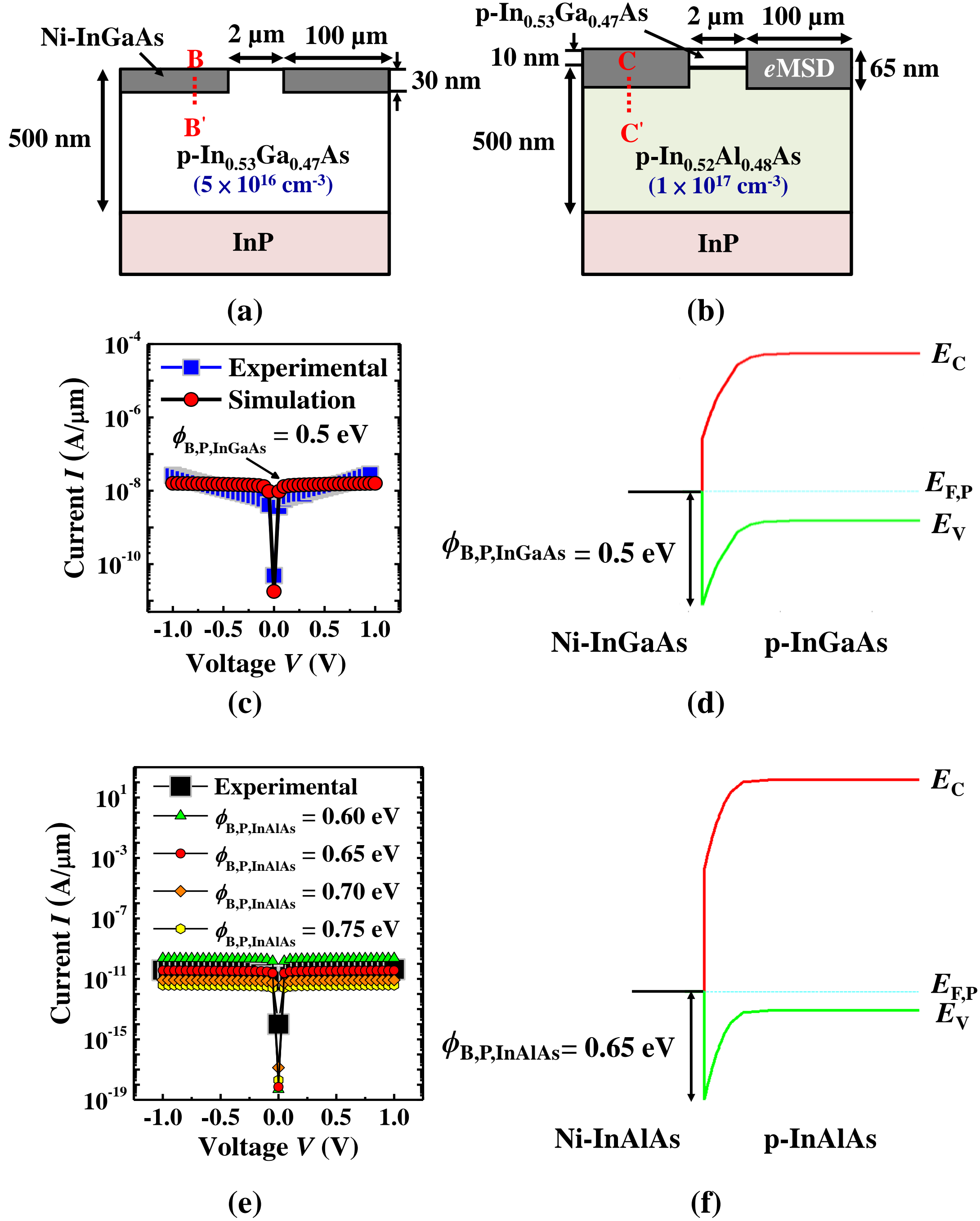


Fig. 4.9. Schematic of back-to-back diodes structures on (a) bulk-InGaAs/InP, and (b) on ultra-thin InGaAs with an InAlAs barrier layer on InP, used for the TCAD simulation. (c) The simulated *I-V* curves for the bulk-InGaAs/InP structure and (d) the corresponding energy band diagram across B-B' (no voltage bias applied). *I-V* curves shows good agreement with the experimental results for $\phi_{B,P,InGaAs} = 0.5$ eV. (e) The simulated *I-V* curves for the ultra-thin InGaAs/InAlAs/InP structure, and (f) the corresponding energy band diagram across C-C' (no voltage bias applied). A $\phi_{B,P,InAlAs}$ of 0.65 eV was extracted by matching the simulation results with the experimental results shown in Fig. 4.8 (c).

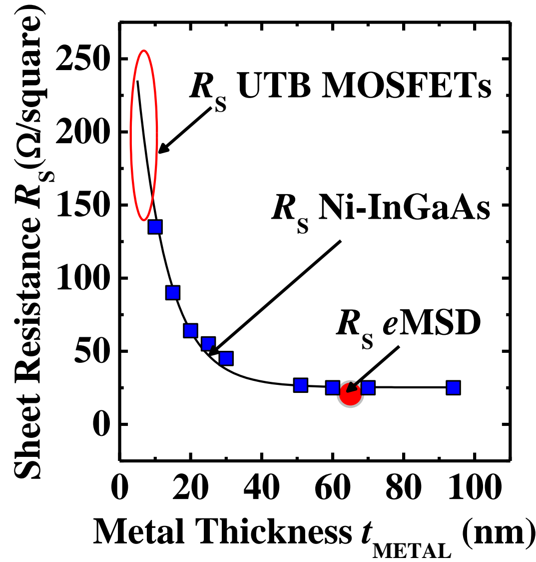


Fig. 4.10. R_S-t_{METAL} of UTB-FET with *e*MSD and Ni-InGaAs. The R_S of the 65 nm thick *e*MSD was 20 Ω/square.

R_S of the ~65 nm thick *e*MSD was ~20 Ω/square (as shown in Fig. 4.10). The R_S of Ni-InGaAs, as a function of its thickness, is plotted as a solid curve. This curve was plotted by fitting data points (shown in the blue squares) obtained from other experiments. In a UTB-FET with thin S/D consisting of Ni-InGaAs, the R_S of the Ni-InGaAs S/D is as high as ~135 Ω/square for a body thickness of 10 nm. By adopting the *e*MSD structure with a thickness of ~65 nm, R_S can be reduced by ~7 times for the same body thickness.

Fig. 4.11 (a) shows the schematic of a cross-section of the device shown in Fig. 4.5 (b). The dimension of the source or drain region was 50 μm × 100 μm. Fig. 4.11 (b) plots the total resistance (R_T) in the linear regime (V_D = 0.1 V), as a function of V_{GS}, for the same device in Fig. 4.6. The R_{SD} value was derived from the R_T at high V_{GS}, due to a reduction in the channel resistance (R_{CH}) (as the device is turned ON). The equation for the solid curve (black line) in Fig. 4.11 (b) is given by [165]:

$$R_T = R_{SD} + R_{CH} = R_{SD} + L_G \cdot \left[W_G \cdot \mu_{EFF} \cdot C_{OX} \cdot \left(V_{GS} - V_T\right)\right]^{-1}, \quad (4.6)$$

where μ_{EFF} is effective channel mobility. Equation (4.6) was used to fit the data points, represented by black circles, in Fig. 4.11 (b). During the data fitting, μ_{EFF} was assumed to be constant in the region of strong inversion, resulting in a slight overestimation of the extracted R_{SD}. The fitted curve was extrapolated to a large V_{GS} of 7 V, and the value of R_{SD} was then extracted to be ~8 kΩ·µm [illustrated in Fig. 4.11 (b)].

The main elements of R_{SD} (Ω·µm) are (i) the resistance of the *e*MSD regions (R_{eMSD}), and (ii) the contact resistance (R_C) between the Ni-InGaAs contact and the InGaAs channel. R_{SD} can be expressed by the following equation:

$$R_{SD} = 2 \cdot \left(R_{eMSD} + R_C \right). \tag{4.7}$$

Since the probes were landed in the center of the S/D regions, the S/D probe distance from the channel (P_{SP}) was ~50 µm during the measurement. Based on the device S/D geometry shown in Fig. 4.11 (a), R_{eMSD} can be calculated as:

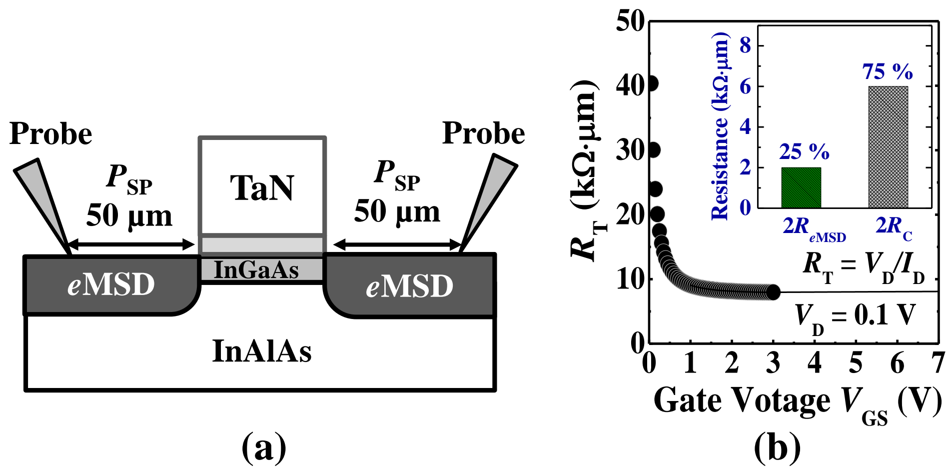


Fig. 4.11. (a) Schematic of the cross-section (A-A') of the device shown in Fig. 4.5 (b). The S/D probe spacing from the device channel (P_{SP}) was ~50 µm. (b) Plot of the total resistance ($R_T = V_D/I_D$) as a function of V_{GS} in the linear regime (V_D = 0.1 V) of the same device as in Fig. 4.6. The components of R_{SD} are shown in the inset of (b). It consists of the *e*MSD resistance (R_{eMSD}) and the contact resistance (R_C) between Ni-InGaAs and the InGaAs channel. Their percentage contribution to R_{SD} is ~25 % and ~75 %, respectively.

$$R_{eMSD} = P_{SP} \cdot R_{S,eMSD}\,, \qquad (4.8)$$

where $R_{S,eMSD}$ is the sheet resistance of the *e*MSD. $R_{S,eMSD}$ = 20 Ω/square for 65 nm thick *e*MSD regions. Based on Equations (4.7) and (4.8), the Ni-InGaAs/Ni-InAlAs *e*MSD contributes ~2 kΩ·µm to the total R_{SD}. This value is ~25 % of the extracted R_{SD}. The remaining ~75 % can be attributed to the R_C between Ni-InGaAs and the inversion layer formed in the InGaAs channel [Equation (4.7)]. The high R_C could be due to a relatively high $\phi_{B,N}$ (~0.24 eV) between Ni-InGaAs and inversion layer [231] in the $In_{0.53}Ga_{0.47}As$ channel. Further optimization, to reduce R_{eMSD} and R_C, is necessary to minimize the R_{SD}. Moreover, placing thick metal pads closer to the InGaAs channel can reduce P_{SP}, which in turn reduces R_{eMSD} [Equation (4.8)]. For example, a 10 times reduction in probe spacing correspondingly results in a 10 times reduction in the resistance contribution from the *e*MSD. Furthermore, R_C between the Ni-InGaAs layer and the InGaAs channel can be decreased by reducing $\phi_{B,N}$. This can be achieved by increasing the In composition in the channel [235] and/or by inserting a highly doped n-type InGaAs S/D extension region in between the two layers [155]. In order to achieve this, a doping technique that can attain abrupt, ultra-shallow junctions with high n-type doping concentrations (N_D) was developed. The details of this doping technique are discussed in Chapter 5.

Fig. 4.12 (a) shows a benchmarking plot of the S obtained from the UTB-FET with *e*MSD with results from bulk-InGaAs N-MOSFETs with Ni-InGaAs S/D [261], [278], UTB-FETs with thin metallic S/D [262], [263], [268], and multi-gate FETs with Ni-InGaAs S/D [155], [262] reported in the literature. The S reported here is lower than those of bulk-InGaAs FETs and comparable to those of UTB-FETs with thin S/D. The R_{SD} of the UTB-FET with *e*MSD is lower than that of the UTB-FETs with thin metallic S/D [262]-[263] [Fig. 4.12 (b)].

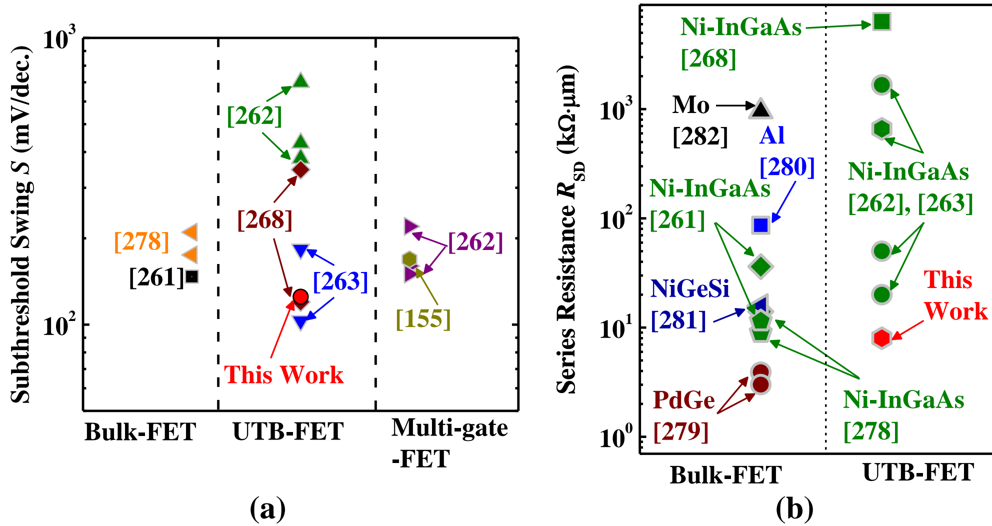


Fig. 4.12. Benchmarking (a) S of UTB-FET with *e*MSD, bulk-InGaAs N-MOSFETs with metal S/D, UTB-FETs with thin metallic S/D, and multi-gate FETs with metal S/D, and (b) R_{SD} of InGaAs N-MOSFET with *e*MSD with reported R_{SD} of bulk-InGaAs N-MOSFETs and UTB-FETs with thin metallic S/D.

4.3 Evaluating eMSD Architecture for Future Technology Nodes: A Simulation Study

The *e*MSD architecture was successfully demonstrated on long channel (L_G = 2 µm) planar InGaAs UTB-FETs as described in the previous Section. For a fixed channel thickness of 10 nm, a lower R_{SD} was obtained for the UTB-FET with *e*MSD compared to the UTB-FETs with the thin S/D. However, InGaAs MOSFETs are projected to be used in mass production in year 2018 [99], where the L_G would be ≤ 15 nm for logic applications. Therefore, it is important to analyse the effect of the *e*MSD design when it is incorporated in an ultra-short channel InGaAs MOSFET. This was done through TCAD simulations and is discussed in the following subsections.

4.3.1 Structure and Parameters Used for Simulation

The different structures used for the simulation are shown in Fig. 4.13: (a) UTB-FET with thin S/D (control), (b) UTB-FET with RSD, and (c) UTB-FET with

*e*MSD. The thickness of the S/D (*d*) was varied for UTB-FETs with both RSD and *e*MSD architectures. The effects of *d* on the parasitic capacitance and resistance components, and on the overall device performance were studied.

The simulations were carried out using a TCAD simulator (Silvaco), in which the non-linear Poisson equation and the current continuity equation were self-consistently solved for electrons. $In_{0.53}Ga_{0.47}As$ n-MOSFETs with L_G of 15 nm were simulated to ensure that they represent the actual devices, as projected by the

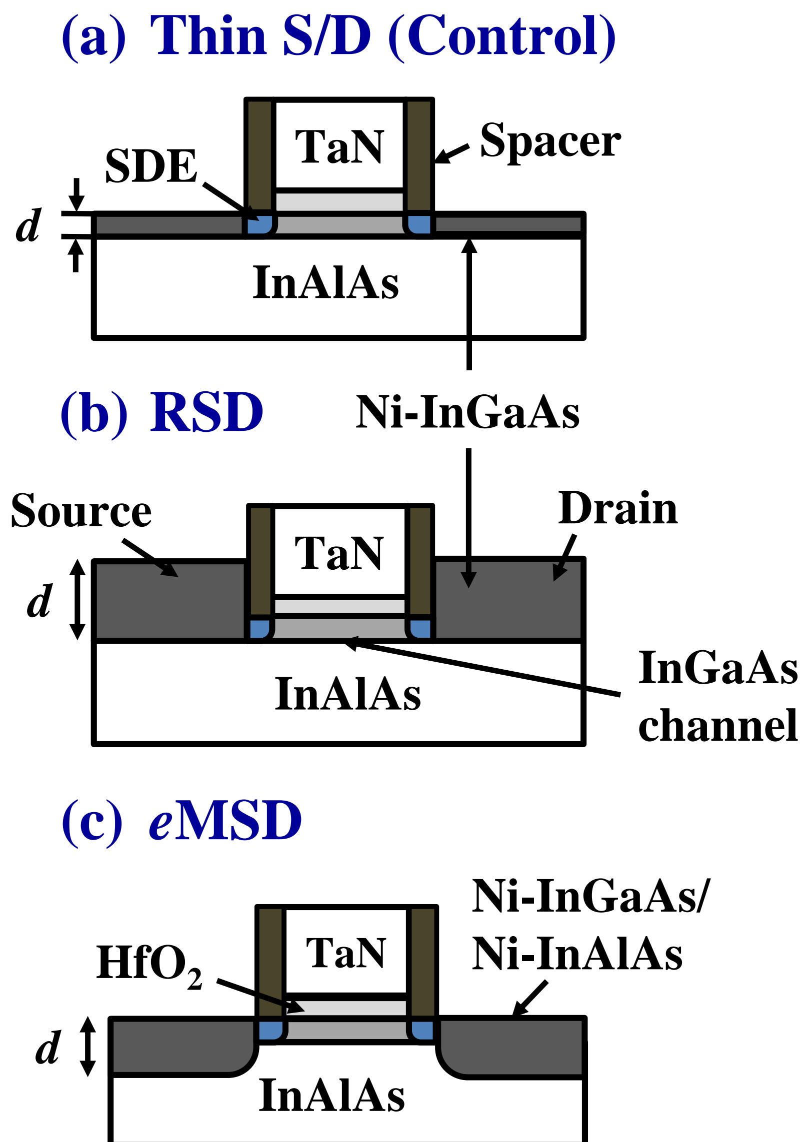


Fig. 4.13. Schematics of the structures used for the 2D simulation: (a) UTB-FET with thin S/D (control), (b) UTB-FET with RSD, and (c) UTB-FET with *e*MSD.

ITRS for III-V high-performance logic technology [99]. The interface between the Ni-InGaAs contacts and the S/D extension regions was modeled as an Ohmic metal-semiconductor interface with specified contact resistivity (ρ_C) of 1×10^{-8} $\Omega\cdot cm^2$. This ρ_C was chosen as it represents the requirements of ITRS for MOSFETs at sub-22 nm technology nodes [239]. The electrical resistivity of Ni-InGaAs and Ni-InAlAs were calculated based on the results from the R_S and the metal thicknesses obtained from the previous Section of this Chapter.

Mechanisms such as phonon, impurity, and carrier-carrier scattering, as well as screening of ionized impurities by charge carriers, are accounted for using the Philips Unified Mobility Model [283]. A field-dependent mobility model was used to account for the dependence of the carrier mobility on the electric field perpendicular to the gate oxide [284].

A high N_D is required in the S/D extension regions to reduce R_{SD}. The N_D of the S/D extension (SDE) was fixed at 5×10^{19} cm^{-3}, which is comparable to the highest N_D achieved on *in situ* Si-doped $In_{0.53}Ga_{0.47}As$ [192]. The maximum and minimum electron mobility (μ_{max} and μ_{min}) in the Philips Unified Mobility Model were set at 12000 $cm^2/V\cdot s$ and 1000 $cm^2/V\cdot s$, respectively. Based on these mobility values, the concentration-dependent electron mobility in the S/D extension was ~1140 $cm^2/V\cdot s$. This result is consistent with experimentally obtained electron mobility values of 1266 and 740 $cm^2/V\cdot s$ at active N_D of 3.6×10^{19} and 6×10^{19} cm^{-3}, respectively [153], [285]. The control device had a d of 5 nm, which was same as the thickness of the InGaAs channel. RSD and *e*MSD structures were simulated using d of 15, 25, and 35 nm. Table 4.1 summarizes the key parameters of the simulation.

Table 4.1. Summary of the parameters used in the 2D simulation.

Gate Stack	n^{++}-InGaAs SDE
Metal Gate: TaN TaN thickness = 50 nm TaN work function: 4.65 eV	Length = 5 nm Depth = 5 nm Doping = 5×10^{19} cm^{-3}
Gate dielectric: HfO_2 HfO_2 dielectric constant = 22 HfO_2 thickness = 3 nm	**Spacer**
	Material = Si_3N_4 Length = 5 nm Height = 50 nm Dielectric constant = 7.5
p-type InGaAs Channel	
Thickness = 5 nm Undoped channel	**p^{++}-InAlAs Barrier layer**
Metal S/D	Thickness = 30 nm Doping = 3×10^{19} cm^{-3}
Material = Ni-InGaAs or Ni-InAlAs Contact resistivity = 1×10^{-8} Ωcm^2	**Philips Unified Mobility Model**
	Max. mobility = 12000 cm^2/Vs Min. mobility = 1500 cm^2/Vs

4.3.2 Effect of S/D Thickness on the Parasitic Capacitance (C_{GD})

The various capacitance components in a MOSFET are shown in Fig. 4.14. The C_{GD}, gate-to-source capacitance (C_{GS}), and total gate capacitance (C_{GG}) were obtained from the 2D simulations where

$$C_{GD} = \partial Q_G / \partial V_D \big|_{V_S, V_G}, \tag{4.9}$$

$$C_{GS} = \partial Q_G / \partial V_S \big|_{V_D, V_G}, \tag{4.10}$$

$$C_{GG} = \partial Q_G / \partial V_G \big|_{V_D, V_S}, \tag{4.11}$$

where Q_G is the gate charge. In a UTB-FET, $C_{GG} = C_{GD} + C_{GS}$. Additionally, gate oxide capacitance (C_{OX}) is given by

$$C_{\mathrm{OX}} = \frac{\kappa \cdot \varepsilon_0 \cdot L_{\mathrm{G}}}{T_{\mathrm{OX}}}, \tag{4.12}$$

where ε_0 is vacuum permittivity and κ is the relative permittivity of the gate oxide.

As illustrated in Fig. 4.14, the N-MOSFET has a symmetric structure. It is well known that when MOSFETs operate in the linear regime, both source and drain regions are connected to the electron inversion layer, and C_{GG} is symmetrically partitioned between the source and the drain, i.e. $C_{\mathrm{GD}} \approx C_{\mathrm{GS}} \approx C_{\mathrm{GG}}/2$. However, as the channel is pinched off in the saturation regime, $C_{\mathrm{GS}} \approx 2/3 \cdot C_{\mathrm{GG}}$, and $C_{\mathrm{GD}} \approx 0$. The parasitic capacitance components are given by [286]-[287]:

$$C_{\mathrm{GD}} = C_{\mathrm{GD,inv}} + C_{\mathrm{DOF}} + C_{\mathrm{DIF}}, \tag{4.13}$$

$$C_{\mathrm{GS}} = C_{\mathrm{GS,inv}} + C_{\mathrm{SOF}} + C_{\mathrm{SIF}}, \tag{4.14}$$

where $C_{\mathrm{GD,inv}}$ and $C_{\mathrm{GS,inv}}$ are the inversion capacitances at the drain and source side, respectively. C_{DOF} and C_{SOF} are the outer fringing capacitances, and C_{DIF} and C_{SIF} are the internal fringing capacitances on the source and drain, respectively.

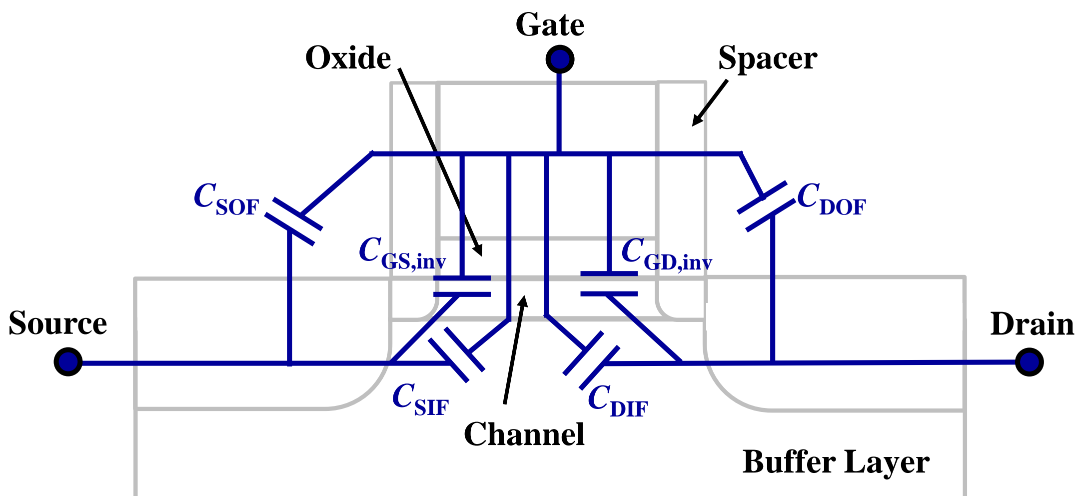


Fig. 4.14. Schematic showing the different capacitance components in a UTB-FET.

The impact of d on the parasitic capacitances was evaluated by comparing the C_{GD} extracted from the different structures. Fig. 4.15 shows the comparison of C_{GD} versus V_{GS} for the control, RSD, and *e*MSD architectures. RSD and *e*MSD structures have d of 35 nm. At $V_D = 0.05$ V and low V_{GS} (before inversion occurs), C_{GD} (or C_{GS}) comprises of parasitic capacitance components. As the channel forms at higher V_{GS}, C_{GD} increases due to increase in $C_{GD,inv}$. At a fixed V_{GS} (where inversion layer is formed), increase in V_D pinches off the inversion layer at the drain side, in turn reducing C_{GD}. It can be inferred from Fig. 4.15 that the parasitic capacitance is higher (~four times) for the device with the RSD compared to the control structure, which can be attributed to an increase in the capacitance between the TaN gate and the RSD (C_{DOF}). The slight increase in C_{GD} for the *e*MSD structure is due to an increase in C_{DIF}.

Fig. 4.16 shows C_{GD} versus V_{GD} ($V_{GD} = V_{GS} - V_D$) for the different structures, where the effect of d on the parasitic capacitances is demonstrated. For the *e*MSD structure, the capacitance does not change significantly as d increases. Whereas, in

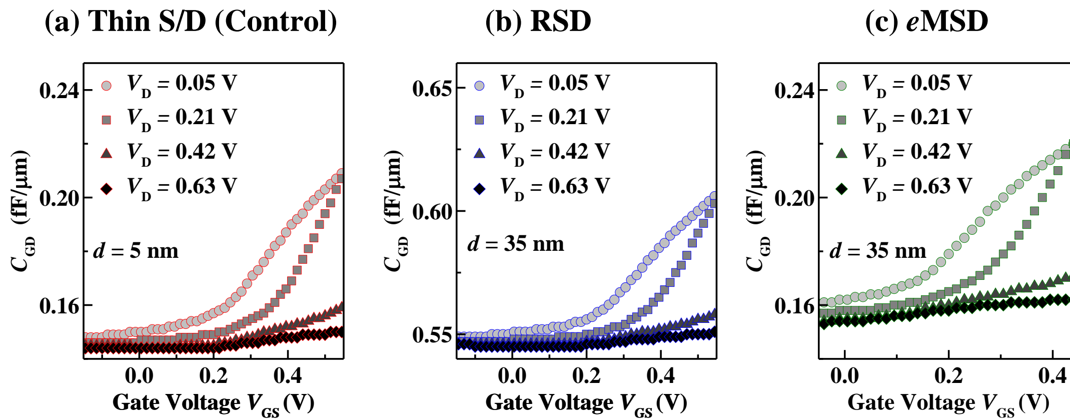


Fig. 4.15. C_{GD} as a function of V_{GS} for different V_D in InGaAs UTB-FETs with (a) thin S/D, (b) RSD, and (c) *e*MSD. The parasitic components can be observed at low V_{GS} where inversion layer in the channel is yet to be formed. The RSD architecture results in a high parasitic capacitance due to an increase in C_{DOF}.

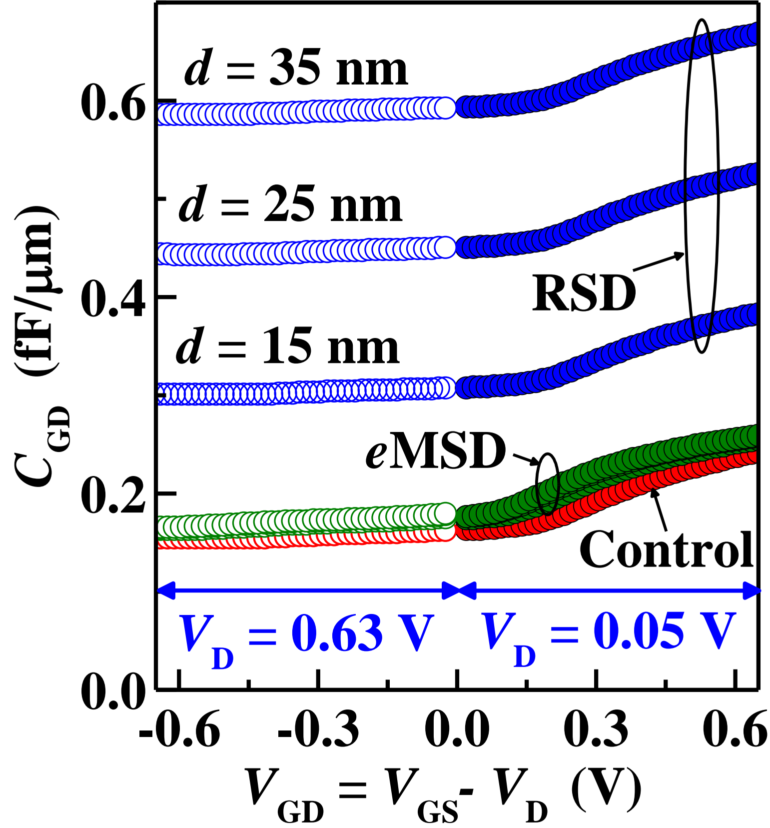


Fig. 4.16. C_{GD} as a function of V_{GD} is compared for the different S/D architectures. C_{GD} for devices with *e*MSD thicknesses are comparable to the control structure. C_{GD} increases with d for the RSD architecture due to higher C_{DOF}.

the case of RSD design, a definite increase in the C_{GD} was seen with an increase in d, which indicates that the effect of C_{DOF} on C_{GD} is more prominent than C_{DIF}. Parasitic capacitance of ~0.16 fF/µm which meets the ITRS requirements of 0.18 fF/µm [99] can be obtained by using the *e*MSD design.

4.3.3 Effect of S/D Thickness on the Parasitic Resistance (R_{SD})

Fig. 4.17 shows the various resistance components in a conventional MOSFET. The total resistance R_T is given by

$$R_T = R_{CH} + 2\cdot(R_{SDE} + R_{S/D} + R_C + R_{METAL}), \tag{4.15}$$

where $R_{S/D}$ and R_{SDE} are the S/D and S/D extension resistances, R_C is the contact resistance between the metal and the n^{++}-S/D region, and R_{METAL} is the resistance of the metal contacts.

Fig. 4.18 shows the comparison of the I_D versus V_{GS} (at V_D of 0.05 and 0.63 V) of the control device, UTB-FETs with RSD, and UTB-FETs with *e*MSD architectures. RSD and *e*MSD structures have *d* of 35 nm. In the control sample: for L_G of 15 nm,

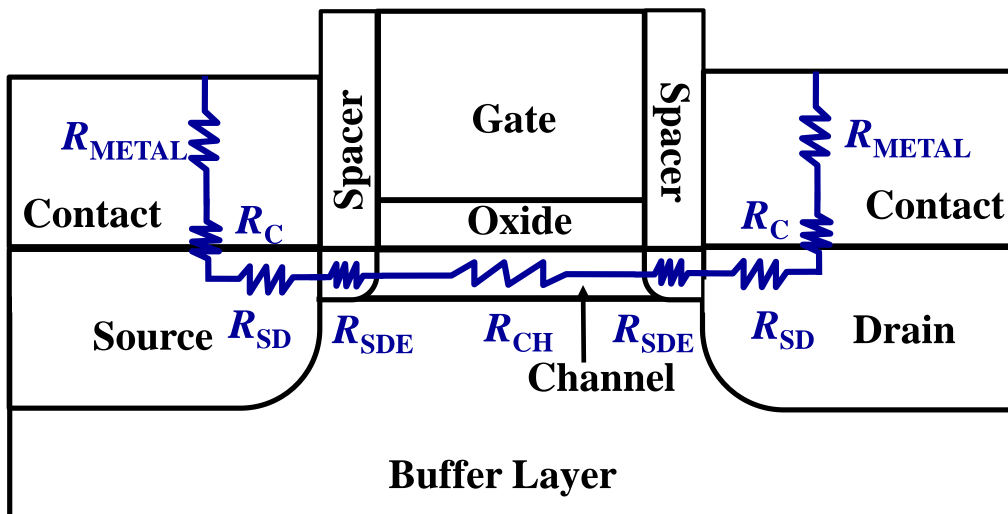


Fig. 4.17. Schematic showing the different resistance components in a UTB-FET.

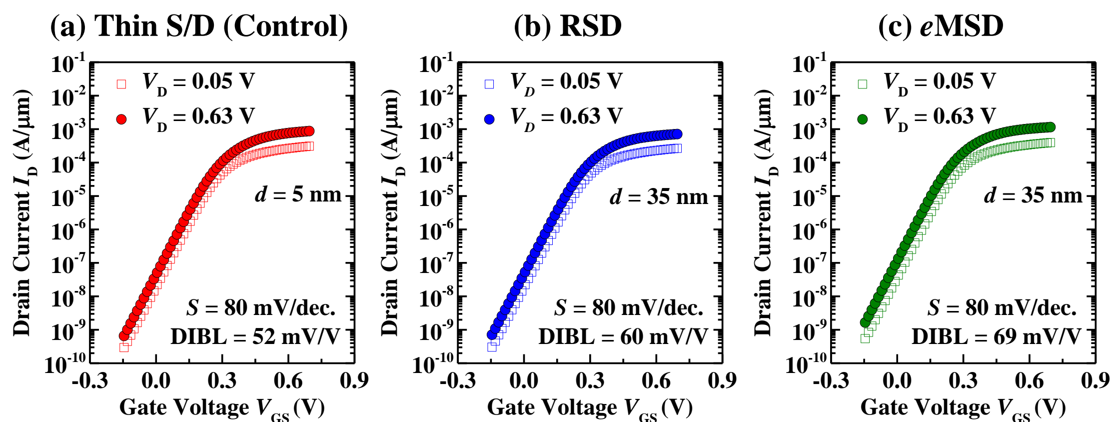


Fig. 4.18. I_D as a function of V_{GS} for different V_D in InGaAs UTB-FETs with (a) thin S/D, (b) RSD, and (c) eMSD. In the control sample, for L_G of 15 nm, I_D of ~0.9 mA/μm at V_D of 0.63 V was obtained. A higher DIBL was observed for the RSD and eMSD structures.

I_D of ~0.9 mA/µm at V_D of 0.63 V was obtained, which was consistent with the values reported by Eugene *et al.* [288] The device had an S of ~80 mV/decade and drain-induced-barrier-lowering (DIBL) of ~52 mV/V. A $V_{T,Sat}$ of ~0.19 V was obtained using a constant current method with a fixed current level of 10 µA/µm. It can be seen that the subthreshold and off-state characteristics of the device are not affected by the variation in d. However, an increase in DIBL can be seen in the UTB-FETs with RSD (~60 mV/V) and *e*MSD (~69 mV/V) architectures. I_D (at V_{GS} = V_D = 0.63 V) as a function of d for the various structures is plotted in Fig. 4.19. The comparison was done at a fixed gate overdrive of 0.5 V, as the $V_{T,Sat}$ changes with d for the *e*MSD structure, due to an increase in C_{DIF}. This leads to a DIBL effect, which reduces $V_{T,Sat}$. A ~ 27 % increase in I_D over the control structure can be obtained by employing the *e*MSD architecture.

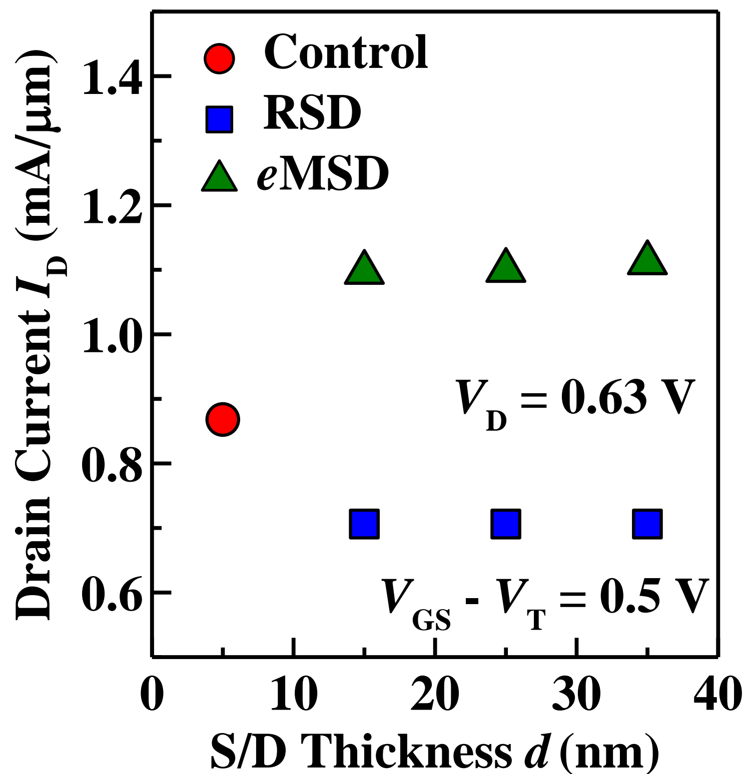


Fig. 4.19. I_D is compared with varying d. The comparison is done at a V_{GS} - V_T of 0.5 V due to DIBL effect in the *e*MSD structure.

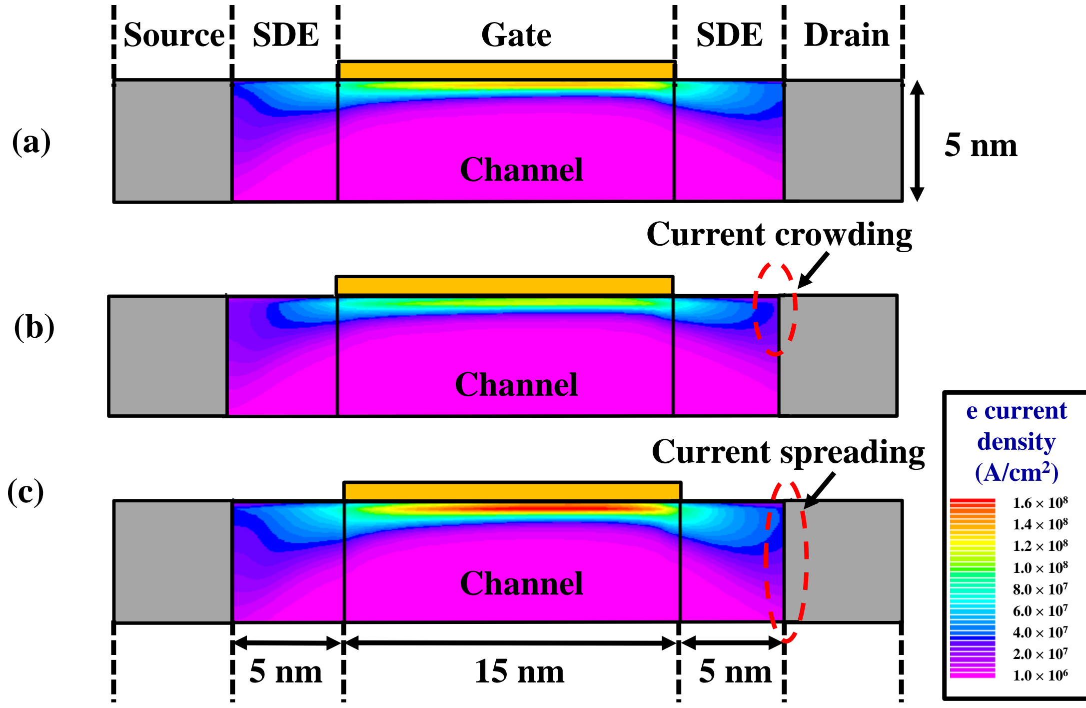


Fig. 4.20. Current density contours (V_{GS} -V_T = 0.5V, V_D = 0.63 V) for (a) thin S/D, (b) RSD, and (c) *e*MSD architectures. A current crowding effect was observed in the RSD structure, resulting in a higher effective R_C. This in turn lowers I_D. Higher I_D for the *e*MSD design is due to the lower R_{CH} and R_{SD} resulting from DIBL effect and spreading of the current at SDE/ Ni-InGaAs interface, respectively.

Current density contours in the channel region at V_{GS} -V_T = 0.5 V, and V_D = 0.63 V are presented in Fig. 4.20. The higher I_D observed in *e*MSD is due to: (1) a decrease in R_{CH} because of the DIBL effect, and (2) an increase in the effective contact area (A_{eff}), which in turn reduces the effective contact resistance ($R_{C,eff}$) due to the current spreading at the SDE and S/D interface (as seen in Fig. 4.20). The decrease in I_D for the RSD structure can be attributed to a reduction in A_{eff} resulting in a higher $R_{C,eff}$ at the SDE and S/D interface due to current crowding effect [288].

R_T in the linear regime (V_D = 0.05 V) as a function of *d* for the different structures is plotted in Fig. 4.21 (a). The values are obtained at a fixed V_{GS} -V_T of

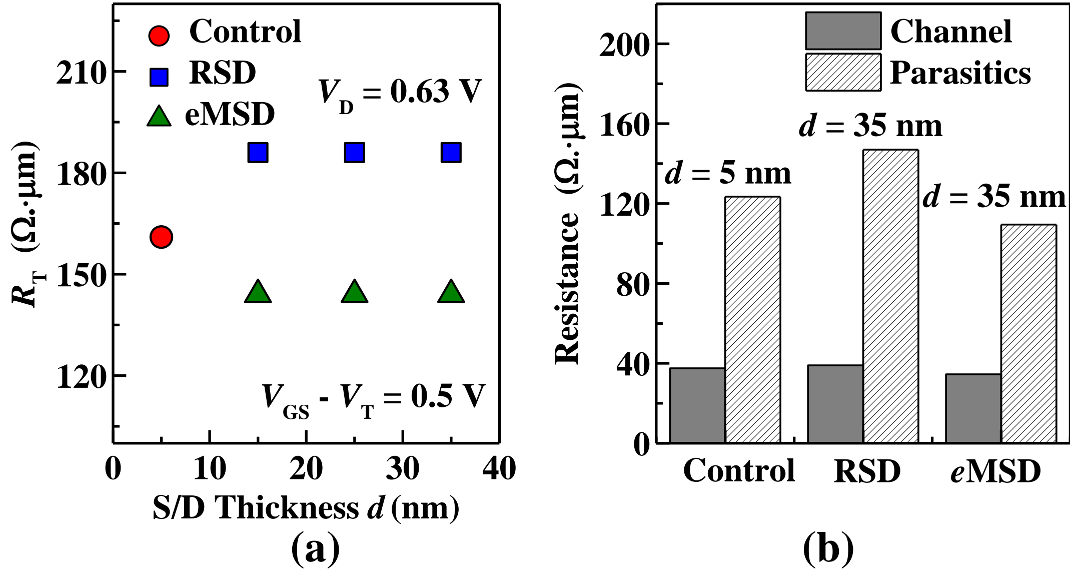


Fig. 4.21. (a) Extracted values of R_T for the various architectures as a function of *d*. (b) Comparison of the different resistance components R_{CH} and R_{SD} in the different structures. R_{CH} was estimated by taking the potential difference across the channel 0.5 nm below the gate oxide. A lower parasitic resistance of ~110 Ω·µm was achieved using the *e*MSD structure.

0.5 V. The trends in R_T are consistent with those observed for I_D. R_{CH} and R_{SD} components are plotted in Fig. 4.21 (b). R_{CH} was calculated by taking the potential difference across the channel, 0.5 nm below the gate oxide [288]. A lower R_{SD} of ~110 Ω·µm, can be achieved using the *e*MSD architecture, which is below the ITRS requirement of 131 Ω·µm [99].

4.3.4 Influence of S/D Thickness on Short Channel Effects

DIBL as a function of *d* for the various device structures is plotted in Fig. 4.22. DIBL increases as *d* is increased for both RSD and *e*MSD structures, which can be attributed to an increase in C_{DOF} and C_{DIF}. The effect of C_{DIF} on the channel is higher than that of C_{DOF} due to the presence of the silicon nitride (Si_3N_4) spacer. This leads to a higher DIBL for the UTB-FET with *e*MSD. In order to reduce the effects of C_{DIF},

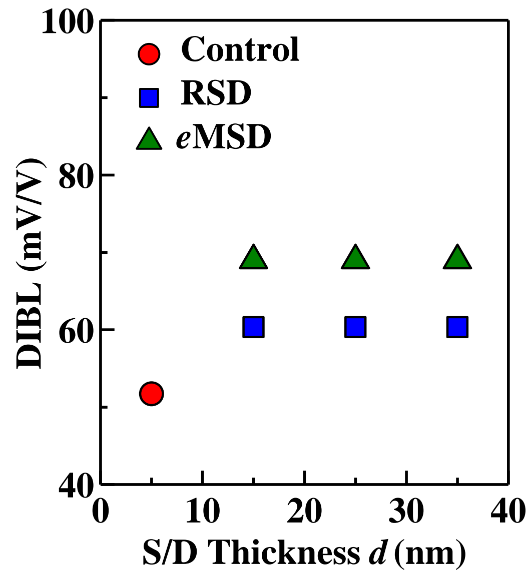


Fig. 4.22. DIBL as a function of d, for the various S/D architectures. DIBL increases with d for RSD due to the increase in C_{DOF}. DIBL increases with d for *e*MSD due to the increase in C_{DIF}.

3D structures such as fin field effect transistors (FinFETs), where the gate has a better electrostatic control over the channel is required. This is discussed in the next Section.

4.3.5 InGaAs FinFET with *e*MSD to Reduce Short Channel Effects

In order to further reduce the SCEs such as DIBL and S in UTB-FETs, 3D

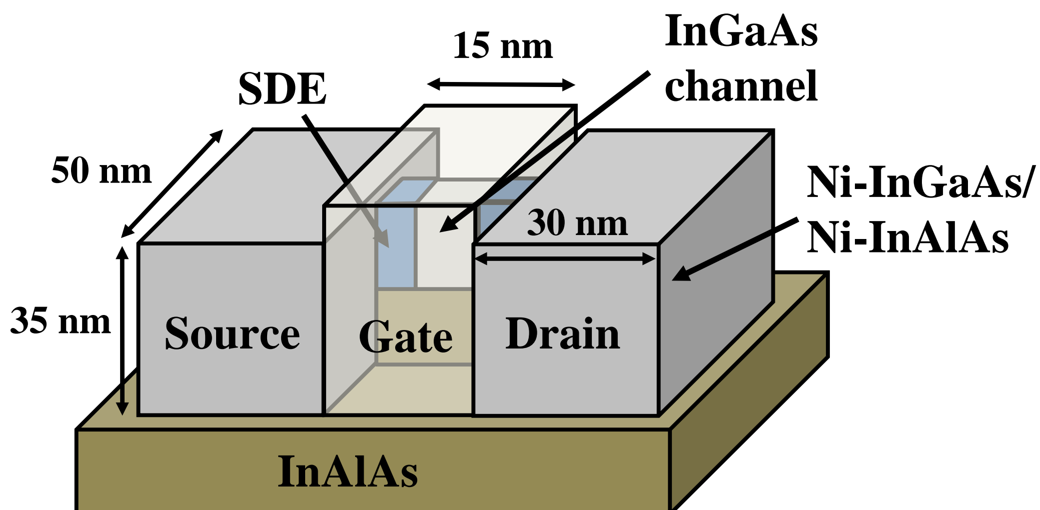


Fig. 4.23. Schematic of the structure used for the simulation. FinFET with *e*MSD structure was simulated with d of 35 nm.

structures such as FinFETs are necessary. Hence, to study the improvements in the short channel behavior, InGaAs FinFET with *e*MSD was simulated. A schematic of the structure used for simulation is shown in Fig. 4.23. The FinFET has a channel width of 10 nm.

Fig. 4.24 (a) shows the comparison of the I_D versus V_{GS} plot, between the planar UTB-FET and FinFET with *e*MSD design. These structures had a *d* of 35 nm. In the FinFET structure, for L_G of 15 nm, I_D was ~0.8 mA/µm at V_D of 0.63 V.

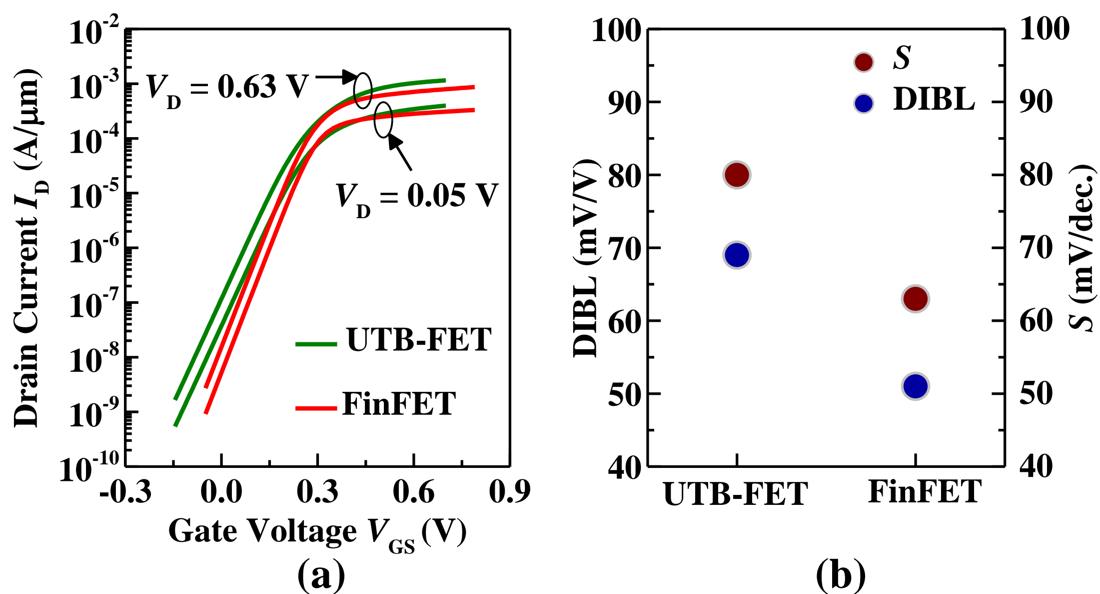


Fig. 4.24. Comparison of the device performance: (a) I_D vs V_{GS}, and (b) the SCE between UTB-FET and FinFET with *e*MSD. The I_D is comparable to that of the planar UTB-FET. The *S* and the DIBL are reduced (~20%) by using the 3D device architecture.

Table 4.2. Comparison of the merits of the different S/D architectures.

	UTB-FET with thin S/D	UTB-FET with RSD	UTB-FET with *e*MSD
Parasitic Capacitances	Low	High	Low
Parasitic Resistances	High	Low	Low
Fabrication Process	Simple	Complex	Simple

The comparison of SCE between the two structures is shown in Fig. 4.24 (b). A ~20 % reduction in S and DIBL can be achieved by using the 3D structure due to the improved electrostatic gate control. The key advantages of using *e*MSD are highlighted in Table 4.2.

4.4 Conclusion

A novel *e*MSD architecture that can achieve low R_{SD} and C_{GD} without increasing the process complexity was realized on InGaAs n-channel UTB-FETs. InGaAs UTB-FETs with L_G = 2 μm were realized and they exhibited good transfer characteristics, low I_{OFF}, high I_{ON}/I_{OFF} ratio of ~10^6, and an S of ~125 mV/decade. The higher $\phi_{B,P}$ (0.65 eV) of the InAlAs barrier layer reduces the sub-surface source-to-drain leakage current (~10^3), which in turn decreases I_{OFF}. For a given channel thickness of 10 nm, a lower R_S of 20 Ω/square was obtained for the UTB-FET with *e*MSD compared to an R_S of 135 Ω/square for the UTB-FET with thin S/D, which resulted in a reduction in the R_{SD}. Furthermore, the effect of the S/D thickness on the R_{SD} and C_{GD} of short channel planar InGaAs UTB-FETs were evaluated using TCAD simulations. An R_{SD} of ~110 Ω·µm, was achieved using the *e*MSD architecture with d = 35 nm, which is below the ITRS requirement of 131 Ω·µm. Similarly, a C_{GD} of ~0.16 fF/µm, which meets the ITRS requirements of 0.18 fF/µm, can be realized by using the *e*MSD design. However, the *e*MSD design resulted in an increased DIBL in the planar devices, due to an increase in the internal fringing capacitances. The simulation study showed that the DIBL effect can be effectively minimized (~20 %) with the help of the 3D FinFET structure.

Chapter 5

$P_2S_5/(NH_4)_2S_x$-Based Sulfur Monolayer Doping for Source/Drain Extensions in InGaAs N-MOSFETs

5.1 Introduction

As previously discussed in Chapter 4, highly n-type (n^{++}) doped source/drain extensions (SDEs) are required in between the Ni-InGaAs metal source/drain (S/D) and the inversion layer in the InGaAs channel to minimize S/D resistance (R_{SD}). The low R_{SD} results in high ON-state current (I_{ON}) in the saturation regime. In addition, abrupt, ultra-shallow and damage-free SDEs are needed to reduce drain-induced-barrier-lowering (DIBL) and suppress the OFF-state leakage current from the source to the drain. Monolayer doping (MLD) is a process where a few monolayers of dopant atoms are assembled on the surface of the semiconductor and are driven in and activated using an annealing step. This is a promising technique for achieving such ultra-shallow junctions.

MLD has been demonstrated on Si substrates in the past [289]-[294]. It has been shown that this technique is capable of achieving abrupt, ultra-shallow, and damage-free junctions with high doping concentrations. Sulfur monolayer doping (SMLD) using $(NH_4)_2S_x$ solution has been demonstrated on gallium arsenide (GaAs) [295]-[296], indium arsenide (InAs) [297], and InGaAs [298]-[299]. MLD of InGaAs using Si as a dopant was also demonstrated recently [300]. Si, which is commonly used to dope InGaAs, can lead to either n-type or p-type doping, due to its amphoteric nature. This can be avoided by using sulfur as the dopant. The principle behind the SMLD

technique on InGaAs is illustrated in Fig. 5.1 [301]. A pre-clean is performed to remove native oxide from the sample surface prior to SMLD. The samples are then treated with sulfur-containing solution and capped with a dielectric to prevent the sulfur from desorbing from the surface. Finally, the samples are annealed using a rapid thermal process (RTP) for driving in the sulfur atoms and for dopant activation. SMLD can achieve conformal doping, which is important for 3D structures such as fin field effect transistors (FinFETs) and nanowire transistors. Additionally, the defects and crystal damage resulting from ion implantation can be avoided by using SMLD.

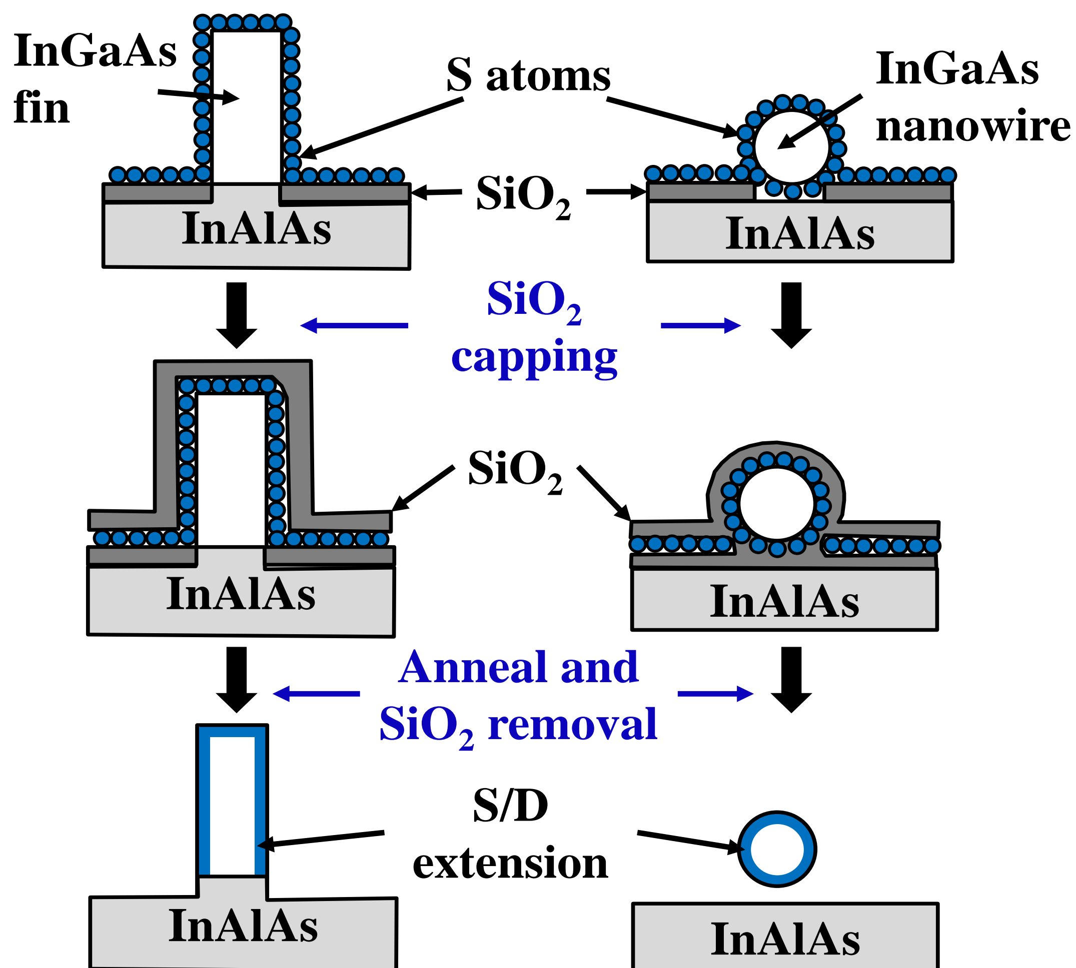


Fig. 5.1. Cross-sectional schematic illustrating the SMLD process on fin and nanowire structures. This technique is capable of achieving abrupt junctions that are conformal and free of implant damage. Therefore, it is a promising method for forming SDEs for 3D structures such as FinFETs or nanowire transistors in future logic applications.

In this Chapter, SMLD for $In_{0.53}Ga_{0.47}As$ using a solution based on phosphorus pentasulfide (P_2S_5) and $(NH_4)_2S_x$ is studied for the first time. The impact of adding P_2S_5 in the $(NH_4)_2S_x$ solution [denoted as $P_2S_5/(NH_4)_2S_x$] on the doping process is investigated. Sheet resistances (R_S) of the SMLD samples are extracted from micro-4-point probe (μ4PP) measurements and Transmission Line Model (TLM) structures. Sulfur profiles after the dopant activation step are obtained using Secondary Ion Mass Spectrometry (SIMS) analysis. Furthermore, optical characterization of the n^{++}-$In_{0.53}Ga_{0.47}As$ layers, formed using the SMLD process, is explored using Infrared Spectroscopic Ellipsometry (IRSE) for the first time. Electrical resistivities ($\rho_{n\text{-InGaAs}}$), carrier relaxation times (τ_e) and active n-type doping concentration (N_D) are obtained from the shallow n^{++}-InGaAs films. They are extracted by modeling the dielectric response of the doped films with a Drude-like free carrier response [302].

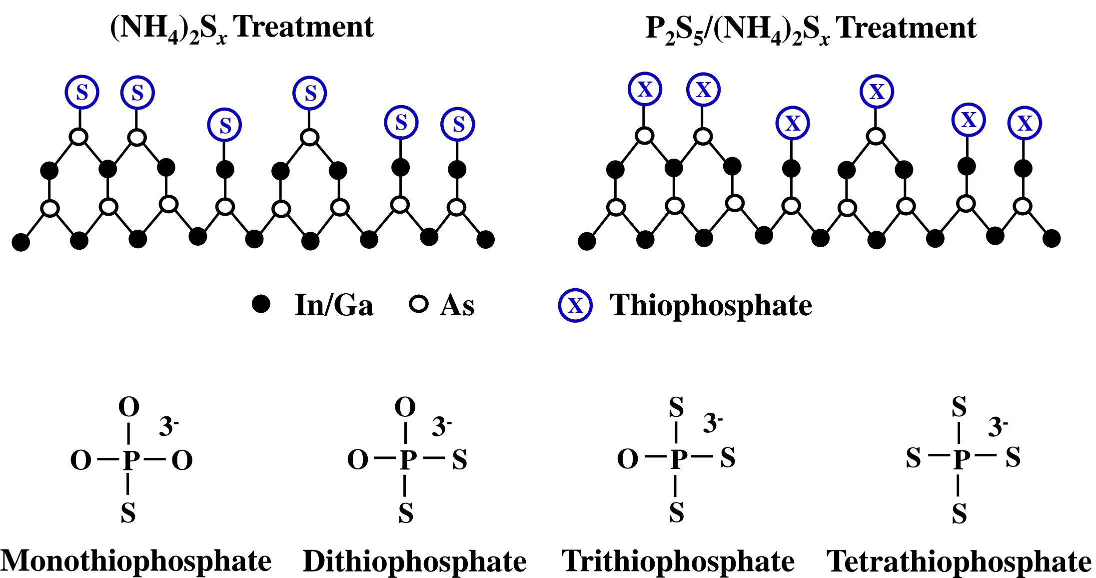


Fig. 5.2. Schematic showing a (001) InGaAs surface after treatment with $(NH_4)_2S_x$, or $P_2S_5/(NH_4)_2S_x$. Hydrolysis of P_2S_5 results in the formation of various thiophosphates. These thiophosphates can react and form compounds on the InGaAs surface.

InGaAs N-MOSFETs that employ SMLD for source/drain (S/D) junction formation are demonstrated for the first time using a gate-first scheme. The effect of the dopant activation step on the performance of the transistors is also studied.

5.2 SMLD of InGaAs using P_2S_5 and $(NH_4)_2S_x$

5.2.1 Motivation for Using P2S5/(NH4)2Sx

Passivation of GaAs surfaces using $P_2S_5/(NH_4)_2S_x$ and $(NH_4)_2S_x$ has been studied extensively [303]-[311], with $P_2S_5/(NH_4)_2S_x$ treatment preferred to $(NH_4)_2S_x$. Studies show that when P_2S_5 is added to the $(NH_4)_2S_x$ solution [311], the resulting sulfur layer degrades more slowly when exposed to air and is thus more robust. Moreover, the addition of P_2S_5 to $(NH_4)_2S_x$ has been shown to reduce the surface roughness of the sample after treatment [312]. Achieving a smooth surface after the doping process is important for achieving good contacts. It has also been shown that a higher dose of sulfur can be incorporated by using $P_2S_5/(NH_4)_2S_x$ as compared to $(NH_4)_2S_x$ solution [312]-[313].

5.2.2 Surface Chemistry

X-ray photoelectron spectroscopy (XPS) studies have shown that treatment of the InGaAs surface using $(NH_4)_2S_x$ helps to remove the surface oxides, such as Ga_2O_3, In_2O_3, and As_2O_3 [314]. The treatment results in the formation of Ga_2S_3, In_2S_3, and As_2S_3 compounds on the InGaAs surface.

In the case of $P_2S_5/(NH_4)_2S_x$ treatment of InGaAs, one possible explanation of the surface mechanisms was provided by Hwang *et al.* [315]. Another explanation follows that the P_2S_5 or P_4S_{10} hydrolyzes in sodium hydroxide (NaOH) to give various thiophosphate ions [316]. Since $(NH_4)_2S_x$ has a similar pH (~11) as NaOH, a similar mechanism can be expected when P_2S_5 hydrolyzes in $(NH_4)_2S_x$ solution. These

thiophosphate groups can then react and form compounds with In, Ga, and As (Fig. 5.2). This also explains the high sulfur dose observed after $P_2S_5/(NH_4)_2S_x$ treatment, as the thiophosphate groups provide more sulfur atoms.

5.2.3 Blanket and TLM Sample Preparation

(a) Blanket samples for μ4PP measurements and SIMS characterization

Two SMLD solutions were prepared: $(NH_4)_2S_x$ and $P_2S_5/(NH_4)_2S_x$. For the $P_2S_5/(NH_4)_2S_x$ solution, powdered P_2S_5 was dissolved in $(NH_4)_2S_x$ solution (20 % in H_2O) at a concentration of 1.6 mg/ml. The pH of the solution after the dissolution of P_2S_5 was approximately 11-12. The starting substrate consists of a 500 nm thick p-type InGaAs (N_A of 2×10^{16} cm^{-3}) epitaxially grown on InP. The samples were first cleaned using diluted hydrochloric acid (HCl:H_2O = 1:3) to remove native oxide prior to SMLD. They were then separately treated in $P_2S_5/(NH_4)_2S_x$ and $(NH_4)_2S_x$ solutions at room temperature for 30 minutes. After treatment, the samples were removed from the solutions and blown dry using nitrogen without rinsing in deionized water. The samples were then loaded into an electron beam evaporator chamber within 30 minutes of blow-drying. A silicon dioxide (SiO_2) capping layer (~15 nm thick) was deposited to prevent out-diffusion of sulfur during the subsequent dopant activation anneal. The capping conditions are critical and can affect the SMLD process. A low temperature capping layer deposition process is required. It has been reported that using a higher temperature for the capping layer deposition results in out-diffusion of the sulfur into the capping layer. This results in a reduction of the active dopant concentration and dopant activation efficiency. [298]. The samples were annealed for 300 s using RTP at temperatures ranging from 400 °C to 700 °C to drive in and activate the dopants.

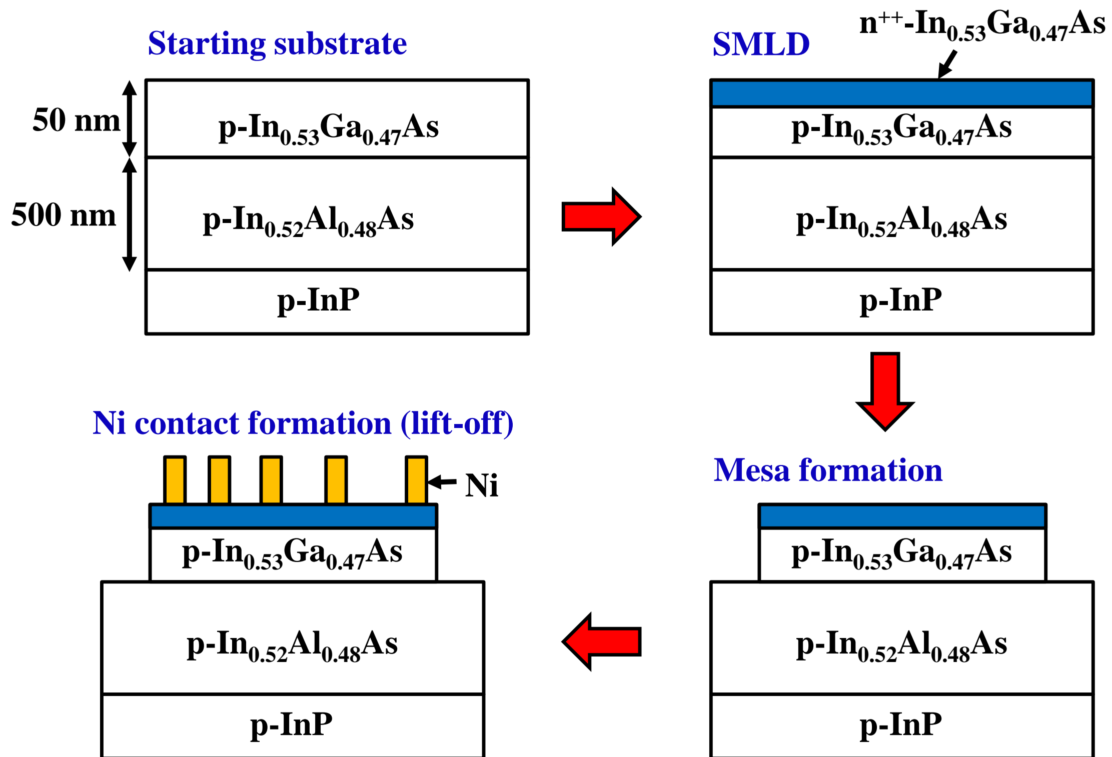


Fig. 5.3. Schematics illustrating the key steps involved in formation of the TLM structures.

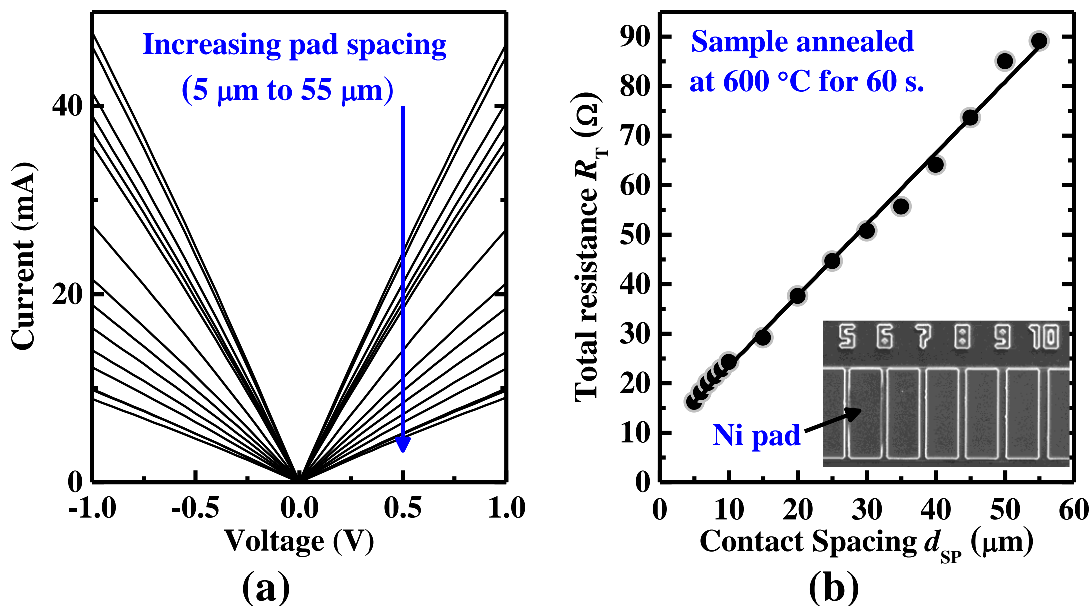


Fig. 5.4. (a) *I-V* characteristics of TLM structures obtained from a sample treated with $P_2S_5/(NH_4)_2S_x$, and (b) the corresponding plot of total resistance R_T versus contact spacing d_{SP}. The inset in (b) shows a top-view Scanning Electron Microscope (SEM) image of a set of fabricated TLM structures.

(b) TLM structures to extract sheet resistance and contact resistivity

Fig. 5.3 illustrates the key steps in TLM structure fabrication. The starting wafer consisted of a 50 nm thick $In_{0.53}Ga_{0.47}As$ with N_A of ~2 × 10^{16} cm^{-3} on 500 nm thick $In_{0.52}Al_{0.47}As$ with N_A of ~1 × 10^{17} cm^{-3}, epitaxially grown on InP wafers (N_A of ~1 × 10^{19} cm^{-3}). Highly doped n^{++}-InGaAs films were formed on the sample using the SMLD process described in the previous Section. Subsequently, mesas were formed using dry etching in chlorine based chemistry. Thereafter, Ni contact pads were formed using a lift-off process to complete the TLM structure.

5.3 Material Characterization

The R_S of the doped InGaAs samples formed by SMLD was measured using TLM structures and μ4PP measurements. The samples used were 1 cm × 1 cm in dimension. The R_S values plotted in the subsequent figures are the average of 3-5 measurements taken from different random locations on each sample.

Fig. 5.4 (a) shows the TLM current-voltage (I-V) characteristics obtained from a sample treated with $P_2S_5/(NH_4)_2S_x$ and annealed at 600 °C for 60 s. I-V curves were acquired from two adjacent Ni pads. The contact spacings (d_{SP}) were 5, 6, 7, 8, 9, 10, 15, 20, 25, 30, 35, 40, 45, 50, and 55 μm. The corresponding plot of total resistance (R_T) versus d_{SP} is shown in Fig. 5.4 (b). From the R_T-d_{SP} plot, the R_S of the n^{++}-InGaAs, contact resistance (R_C), and transfer length (L_T) can be obtained. R_S was extracted from the slope of the plot. The intercept at d_{SP} = 0 gives R_C from the two Ni contact pads. The L_T of the two Ni contacts was determined when R_T becomes zero. From these parameters, the contact resistivity (ρ_C) was extracted using [165]:

$$R_C = \frac{\rho_C}{L_T \cdot W_{Ni}} \cdot \coth\left(\frac{L_{Ni}}{L_T}\right), \quad (5.1)$$

$$\text{for } L_{\text{Ni}} \leq 0.5 \cdot L_{\text{T}}, \qquad \rho_{\text{C}} \approx R_{\text{C}} \cdot L_{\text{Ni}} \cdot W_{\text{Ni}}$$

$$\text{for } L_{\text{Ni}} \geq 1.5 \cdot L_{\text{T}}, \qquad \rho_{\text{C}} \approx R_{\text{C}} \cdot L_{\text{T}} \cdot W_{\text{Ni}}$$

where L_{Ni} and W_{Ni} are the length and width of Ni contact pad, respectively.

The R_{S} obtained from samples treated with $P_2S_5/(NH_4)_2S_x$ and $(NH_4)_2S_x$ solutions are plotted as a function of annealing temperature in Fig. 5.5 (a). Doping was observed in samples that were annealed at temperatures as low as 550 °C. R_{S} decreases as the annealing temperature increases due to higher dopant activation and an increase in the junction depth. At low temperatures of 550 °C and 600 °C, the R_{S} measured using µ4PP was lower than that of the TLM structures. This can be attributed to a possible error in the µ4PP measurement where R_{S} was underestimated due to penetration of the probes through the ultra-shallow n^{++}-layer [317]. The two measurement techniques were in good agreement as the junctions get deeper at higher annealing temperatures.

The R_{S} values at low activation temperatures (e.g. 600 °C) indicate the presence of a higher concentration of active dopants for the samples treated with $P_2S_5/(NH_4)_2S_x$ than for samples treated with $(NH_4)_2S_x$ only. This is a result of the higher dose of sulfur incorporated into the InGaAs for $P_2S_5/(NH_4)_2S_x$ treatment as compared to $(NH_4)_2S_x$ treatment. The specific ρ_{C} is plotted as a function of annealing temperature in Fig. 5.5 (b). The increase in ρ_{C} with increasing annealing temperature is a consequence of the reduction in active dopant concentration at the InGaAs surface. A lower ρ_{C}, which indicates a higher active surface concentration, is observed for the samples treated with $(NH_4)_2S_x$. The lift-off process used in the fabrication of the TLM structures could have contributed to the poor interface between the Ni and the n^{++}-InGaAs, resulting in a relatively high ρ_{C}. The process flow needs to be optimized to reduce ρ_{C}. Further reduction in ρ_{C} can be achieved by using a more appropriate contact metal. For example,

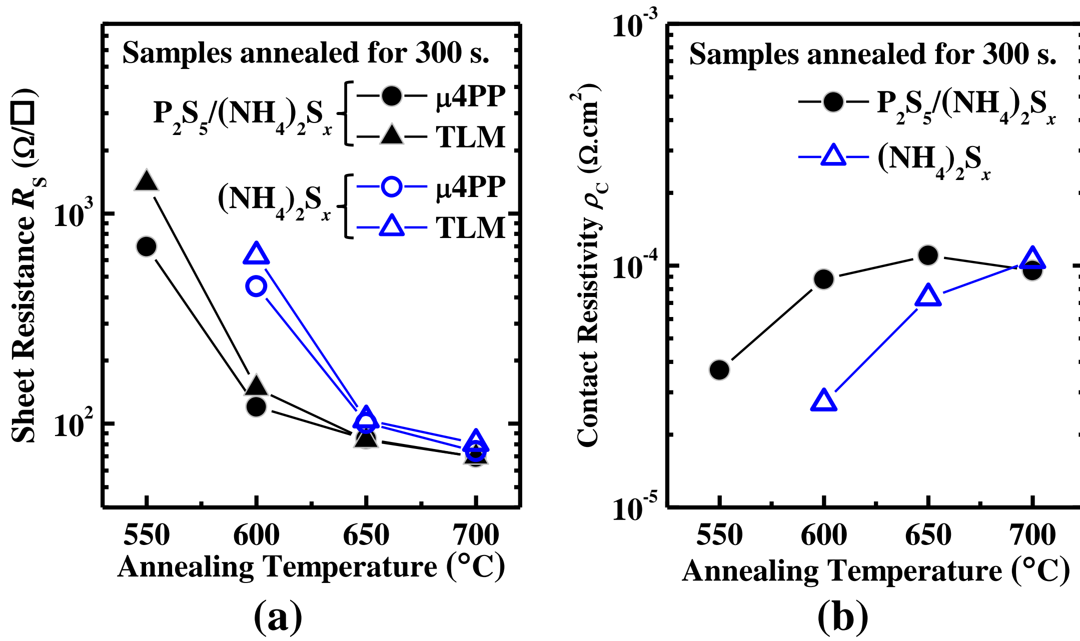


Fig. 5.5. (a) Sheet resistance R_S (in Ω per square, denoted as Ω/□) and (b) contact resistivity ρ_C of samples treated with $(NH_4)_2S_x$, or $P_2S_5/(NH_4)_2S_x$ solution. The samples were annealed at different temperatures ranging from 550 °C to 700 °C for 300 s. R_S decreases with increasing anneal temperature due to an increase in active dopant concentration and a larger junction depth. Lower R_S was obtained for samples treated with $P_2S_5/(NH_4)_2S_x$ at lower activation temperatures. Higher ρ_C at higher activation temperatures suggests a decrease in the active dopant concentration at the InGaAs surface.

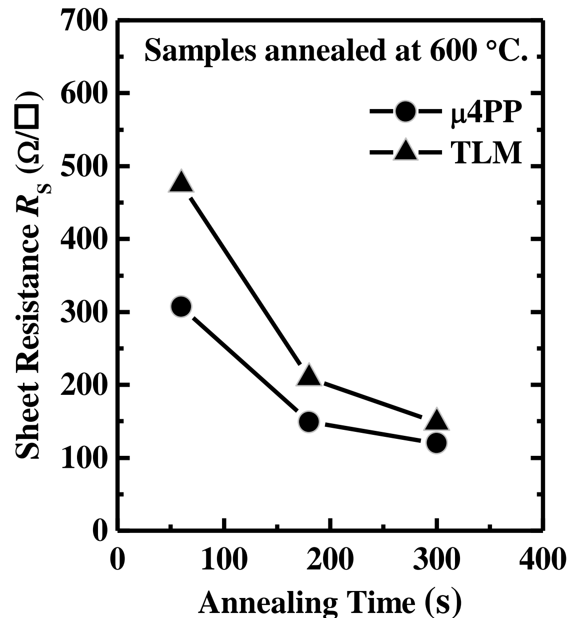


Fig. 5.6. Sheet resistance R_S as a function of annealing time for samples treated with $P_2S_5/(NH_4)_2S_x$ solution and annealed at 600 °C. R_S decreases as the annealing time for the dopant activation step is increased.

by using Ni-InGaAs [155] or molybdenum [318] that have lower ρ_C than Ni on n^{++}-InGaAs. ρ_C can also be reduced by increasing N_D of the n^{++}-InGaAs layer.

The effect of annealing time on the samples treated with $P_2S_5/(NH_4)_2S_x$ was studied. Fig. 5.6 shows R_S as a function of annealing time for samples annealed at 600 °C. Reduction in R_S with longer anneal time can be attributed to higher activation of the dopants and deeper junctions. Fig. 5.7 illustrates the effect of treatment time for samples that were immersed in the $P_2S_5/(NH_4)_2S_x$ solution for different durations followed by dopant activation. R_S remains constant over the whole range. This suggests that the sulfur layer formed after treatment is self-limiting and saturates after a treatment time of 10 minutes or possibly less.

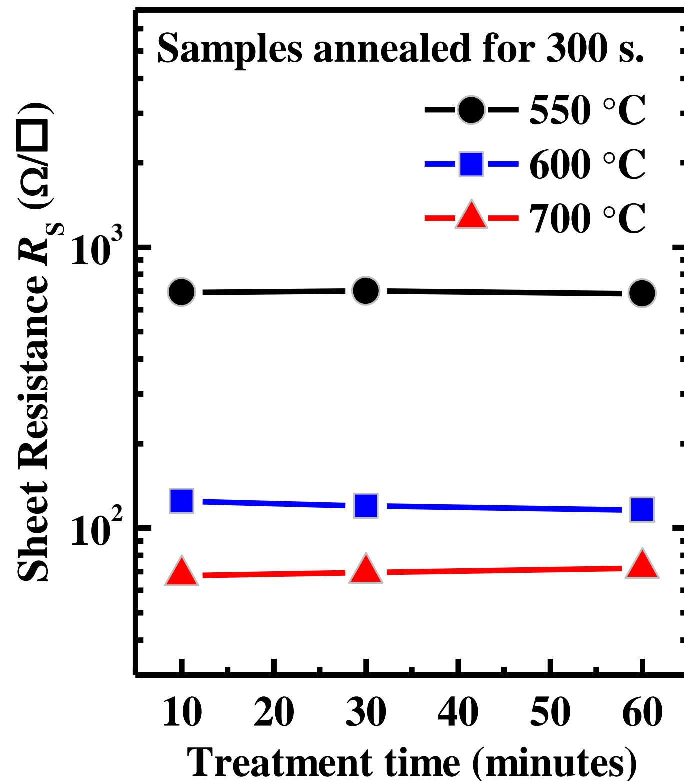


Fig. 5.7. Sheet resistance R_S as a function of treatment time for samples treated with $P_2S_5/(NH_4)_2S_x$ solution. R_S remains constant even as the treatment time is increased from 10 minutes to 60 minutes. This indicates that the sulfur layer on the InGaAs surface saturates within 10 minutes of treatment.

Further characterization was performed on samples annealed at 550 °C for 300 s or 600 °C for 60 s. These annealing conditions were expected to have steep and shallow doping profiles. SIMS was performed on these samples after SiO_2 cap removal using dilute hydrofluoric acid (DHF). All the SIMS in this Chapter, was done at the Institute of Materials Research and Engineering (IMRE) as a paid service. The sulfur profiles obtained for samples treated with the $P_2S_5/(NH_4)_2S_x$ and $(NH_4)_2S_x$ solutions are shown in Fig. 5.8 (a) and (b), respectively. The initial 2-3 nm of InGaAs was ignored due to surface artifacts from the SIMS measurement. There was no residual sulfur observed at the InGaAs surface. The sulfur dose was calculated by integrating the concentration-versus-depth curve.

Samples treated with $P_2S_5/(NH_4)_2S_x$ had a higher sulfur dose of ~5.4×10^{14} cm^{-2} to ~7×10^{14} cm^{-2} compared to ~2×10^{14} cm^{-2} obtained for samples treated with $(NH_4)_2S_x$. The higher dose from $P_2S_5/(NH_4)_2S_x$ treatment is consistent with what has been reported in the literature on GaAs HEMTs [312]-[313]. Two regions with different diffusivity were observed in the SIMS profiles. This is similar to what was reported by Loh *et al.* for SMLD on InGaAs using $(NH_4)_2S_x$ [299]. A small amount of phosphorus was seen near the InGaAs surface for samples treated with $P_2S_5/(NH_4)_2S_x$. This is probably a result of thiophosphate groups that attach themselves to the InGaAs surface during the treatment.

In a separate round of experiments, the time delay (t_{delay}) between $P_2S_5/(NH_4)_2S_x$ treatment and deposition of the SiO_2 capping layer was varied. SIMS profiles obtained from samples with different t_{delay} after dopant activation at 550 ˚C for 300 s or 600 ˚C for 60 s are compared in Fig. 5.9 (a) and (b), respectively. It can be seen that sulfur has not been completely desorbed from the InGaAs surface even after a t_{delay} of 90 minutes. However, the dose was reduced to ~1.5×10^{14} cm^{-2} to ~2.1×10^{14} cm^{-2}. This means that

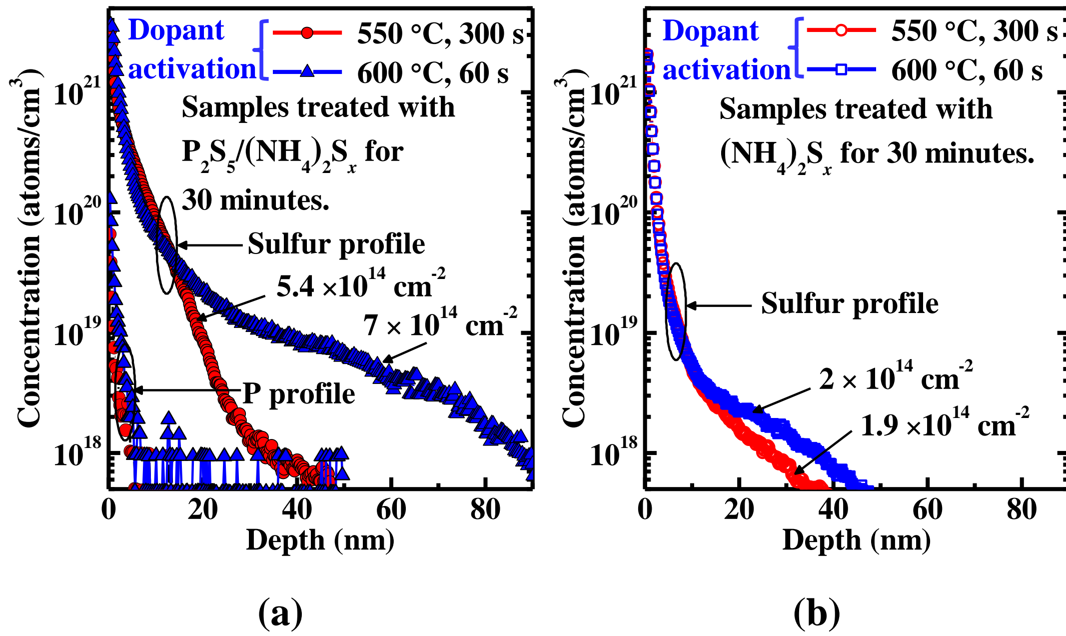


Fig. 5.8. SIMS profiles of samples doped using (a) $P_2S_5/(NH_4)_2S_x$ or (b) $(NH_4)_2S_x$ solution. The samples treated with $P_2S_5/(NH_4)_2S_x$ exhibit a higher sulfur dose than those treated with $(NH_4)_2S_x$ for the same dopant activation conditions. A small amount of phosphorus (P) can be seen at the InGaAs surface for the samples treated with $P_2S_5/(NH_4)_2S_x$.

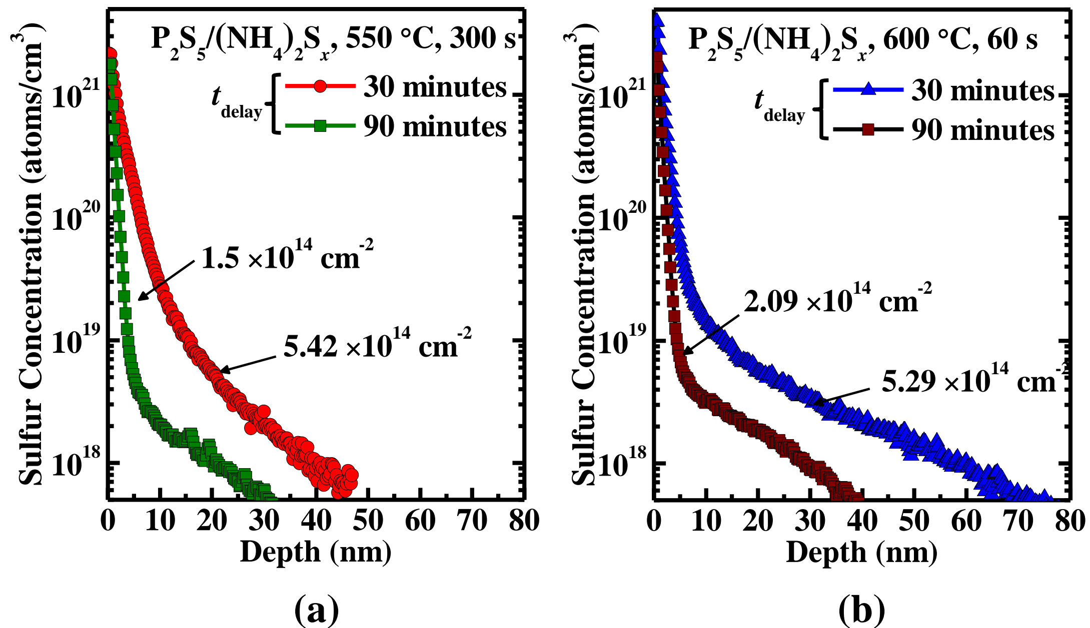


Fig. 5.9. The effect of the time delay t_{delay} between the $P_2S_5/(NH_4)_2S_x$ treatment step and the SiO_2 capping step was examined. For the samples treated with $P_2S_5/(NH_4)_2S_x$, it can be seen that the sulfur dose after dopant activation at (a) 550 ˚C, and (b) 600 ˚C reduces as t_{delay} increases. This is attributed to desorption of sulfur from the InGaAs surface. Therefore, to maintain a high sulfur dose, it is important to cap the samples immediately after the $P_2S_5/(NH_4)_2S_x$ treatment.

to achieve a higher dose of sulfur, the samples must be capped with SiO_2 with minimum t_{delay}. On the other hand, a lower dose results in more abrupt and shallow sulfur profiles. SIMS characterization gives only the chemical profile of sulfur in InGaAs. However, obtaining an active carrier concentration profile is challenging in the case of InGaAs, especially for ultra-shallow junctions. The junction depth depends on the background doping concentration of the sample. For example, if the doping concentration of the p-type InGaAs is 5×10^{18} cm^{-3}, sub-10 nm junctions can be achieved using the SMLD process.

5.4 Optical Characterization Using IRSE

5.4.1 Motivation for Using IRSE

R_S and N_D of doped layers in semiconductors are typically extracted using electrical techniques such as four-point-probe measurement, TLM and Hall Effect measurements. As mentioned in the previous Section, penetration of probes through ultra-shallow junctions can result in erroneous R_S values. Likewise, TLM and Hall measurements are prone to error if the underlying layers in the heterostructures do not provide good current confinement in the doped region of interest. As mentioned in the previous Section, active carrier junction depth for ultra-shallow junctions in InGaAs cannot be determined from the chemical profile acquired from SIMS. IRSE, which is a non-contact and non-destructive technique, is a promising alternative. IRSE has been used for the electrical and physical characterization of semiconductor heterostructures [302]. IRSE was applied to characterize sub-100 nm Si junctions formed by excimer laser annealing on bulk Si and Si-on-insulator [319]. R_S values for junction depths down to ~30 nm have been reported [319].

Active carriers can modify the optical response of a material in the infrared range. In the case of a doped semiconductor, the infrared dielectric response is dominated by free carrier absorption. Parameters such as $\rho_{\text{n-InGaAs}}$, τ_e, and N_D can be determined from the dielectric response using a classical Drude model. The thickness of the doped layer ($T_{\text{n-InGaAs}}$) can also be obtained from ellipsometry. The $T_{\text{n-InGaAs}}$ extracted could be related to the active carrier junction depth. R_S is calculated from $\rho_{\text{n-InGaAs}}$ and $T_{\text{n-InGaAs}}$ of the doped layer.

5.4.2 Details of the Measurement

IRSE measurements were carried out at room temperature (25 °C) using an infrared variable angle spectroscopic ellipsometer (IR-VASE). The ellipsometric angles Ψ and Δ were acquired at an angle of incidence of 65° from 0.05 to 0.65 eV. The complex dielectric function of the n^{++}-InGaAs film was described using an optical dispersion model given by [320]:

$$\varepsilon(E_{\text{PH}}) = C_{\text{ellips}} + \frac{-\hbar^2}{\varepsilon_0 \cdot \rho \cdot \left(\tau \cdot E_{\text{PH}}^2 + i \cdot \hbar \cdot E_{\text{PH}}\right)} + \frac{A_{\text{pole}}}{\left(E_{\text{pole}}^2 - E_{\text{PH}}{}^2\right)}, \tag{5.2}$$

where E_{PH} is the photon energy, C_{ellips} is a fitting parameter that is independent of energy, $\hbar$ is the Planck's constant, and ε_0 is the permittivity of free space. The second term is related to the Drude lineshape that describes the free electron behavior in the conduction band. $\rho_{\text{n-InGaAs}}$ and τ_e are related to the plasmon energy (E_P) and are given by [320]:

$$E_{\text{P}} = \hbar \cdot \sqrt{\frac{1}{\varepsilon_{opt} \cdot \varepsilon_0 \cdot \rho \cdot \tau}} = \hbar \cdot \sqrt{\frac{N \cdot q^2}{\varepsilon_{\text{opt}} \cdot \varepsilon_0 \cdot m^*}}, \tag{5.3}$$

where

$$\varepsilon_{\text{opt}} = C_{\text{ellips}} + \frac{A_{\text{pole}}}{E_{\text{pole}}^{2}}. \tag{5.4}$$

A_{pole} is the magnitude of the pole, E_{pole} is the pole energy, q is the elementary charge, and m^* is the effective mass of the carriers. The third term in Equation (5.2) accounts for the dispersion caused by absorption outside the measured spectral range. The thicknesses of p-type InGaAs, n^{++}-InGaAs and the other adjustable parameters in the model were fitted by a least-square procedure which follows the Levenberg-Marquardt algorithm [321]. Since the infrared wavelengths are not sensitive to the surface, the thickness of the surface layer was kept fixed at ~2√2 times the surface roughness values obtained from Atomic Force Microscopy (AFM) measurements [322]. Root mean square (RMS) roughness of ~0.3 to 0.8 nm was observed on the InGaAs samples after the SMLD process.

5.4.3 Results and Discussion

IRSE was performed on the SMLD samples shown in Fig. 5.10. *In situ* n-type (Si doped) InGaAs films with known N_D of ~1×10^{19} cm^{-3} were also characterized to verify the results obtained from the SMLD samples. *In situ* samples with different

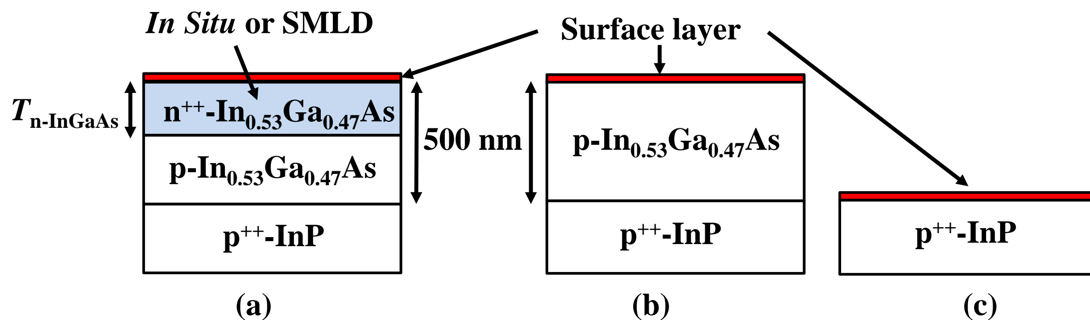


Fig. 5.10. Schematic of the samples used for IRSE measurements; (a) n^{++}-InGaAs layers using SMLD or *in situ* doping on p-type InGaAs/InP substrate, (b) undoped p-type InGaAs/InP substrate, and (c) InP substrate. The surface layer was modeled using the Bruggeman approximation.

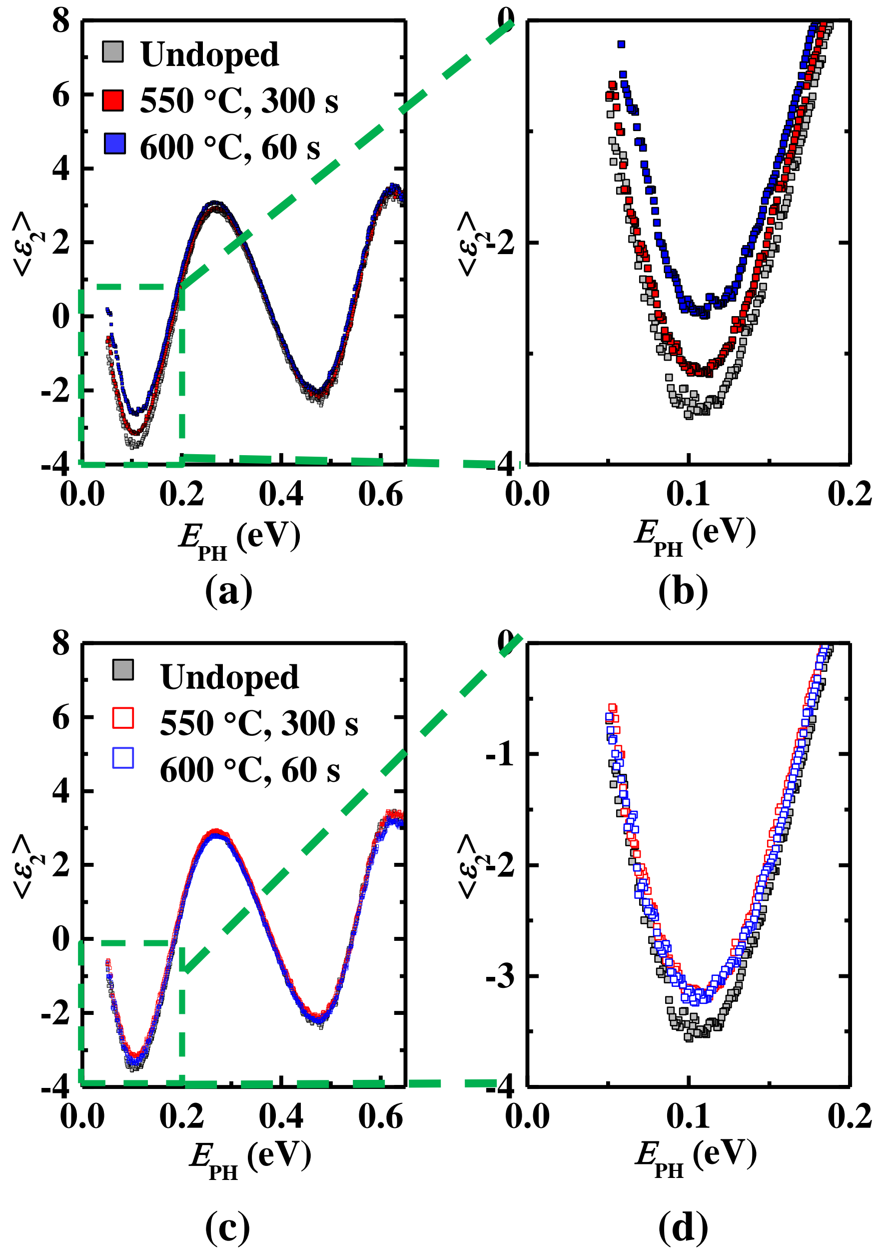


Fig. 5.11. Imaginary part of the pseudo dielectric function $<\varepsilon_2>$ obtained from SMLD samples. (a) $<\varepsilon_2>$ from the $P_2S_5/(NH_4)_2S_x$ based samples for the entire energy range (0.05 - 0.65 eV), and (b) a magnified view of the energy range (0.05 - 0.2 eV) where the signals from the SMLD samples can be distinguished from the undoped sample. (c) $<\varepsilon_2>$ from the $(NH_4)_2S_x$ based samples for the entire energy range (0.05 - 0.65 eV), and (d) a magnified view of the energy range (0.05 - 0.2 eV) where the signals from the SMLD samples can be distinguished from the undoped sample.

$T_{\text{n-InGaAs}}$ were formed by wet etching the n^{++}-InGaAs (100 nm)/p-InGaAs (400 nm)/InP substrate using phosphoric acid chemistry (H_3PO_4:H_2O_2:H_2O = 1:5:20) for different time durations. The samples used for the IRSE measurement are shown in Fig. 5.10.

The SMLD and *in situ* doped samples were modeled as a four-layer system which consists of highly doped (p^{++}) InP substrate, p-type InGaAs film, the n^{++}-InGaAs film and a surface layer [shown in Fig. 5.10 (a)]. The surface layer was modeled as a thin film consisting of 50 % n^{++}-InGaAs and 50 % voids in the Bruggeman approximation [323]. In order to model the n^{++}-layer, it was vital to know the complex dielectric functions of the underlying layers. Hence, the p-type InGaAs layer and the InP substrate were characterized separately using the samples shown in Fig. 5.10 (b) and (c), respectively. Their dielectric functions were then used in modelling the SMLD and *in situ* doped samples.

The imaginary part of pseudo-dielectric function ($<\varepsilon_2>$) for the SMLD samples formed using the $P_2S_5/(NH_4)_2S_x$ and $(NH_4)_2S_x$ solutions are shown in Fig. 5.11 (a) and (c), respectively. The $<\varepsilon_2>$ from the starting substrate (undoped) is plotted for comparison. Although the signal from p-type InGaAs layer dominates $<\varepsilon_2>$, the SMLD samples can be distinguished from the starting substrate in the energy range below 0.2 eV as shown in Fig. 5.11 (b) and (d). An upward shift in $<\varepsilon_2>$ was observed with the formation of the n^{++}-layer on the p-type InGaAs/InP substrate. A point-by-point fit [321] was used in order to confirm that the modeled dielectric function is a realistic representation of the true dielectric function of n^{++}-InGaAs.

The activation efficiency for the different splits was determined from the ratio of the active carrier dose from IRSE measurements and the total sulfur dose from the SIMS profile. They are presented in Table 5.2. The SMLD samples formed using $P_2S_5/(NH_4)_2S_x$ solution show higher active sulfur dose compared to the samples formed with $(NH_4)_2S_x$ solution. This is consistent with the lower R_S values observed for the $P_2S_5/(NH_4)_2S_x$ based samples as seen in Fig. 5.5. The activation efficiency at 550 °C, 300 s and 600 °C, 60 s was ~1-2 %. The activation efficiency achieved using the SMLD

process is slightly lower than that reported by Yum *et al*. [298], which can be attributed to the lower thermal budget used for the dopant activation.

The parameters obtained from the fits are summarized in Table 5.1. N_D and electron mobility (μ_e) were calculated from $\rho_{n\text{-InGaAs}}$ and τ_e by using an electron effective mass $m_e^* = 0.074\ m_e$ [324], where m_e is the electron mass. The SMLD samples had a higher $\rho_{n\text{-InGaAs}}$ and a lower τ_e than the *in situ* samples. The increase in τ_e can be

Table 5.1. Electrical and physical parameters for SMLD and in situ doped n^{++}-InGaAs samples.

Sample #	Sample Type	$\rho_{n\text{-InGaAs}}$ (mΩ·cm)	τ_e (fs)	$T_{n\text{-InGaAs}}$ (nm)	N_D (10^{19} cm^{-3})	μ_e (cm^2·V^{-1}·s^{-1})
1	*In situ*	0.729	33.2	35.2	1.1	790
2	*In situ*	0.533	43.9	45.0	1.1	1044
3	*In situ*	0.448	52.3	56.6	1.1	1242
4	*In situ*	0.375	62.3	86.6	1.1	1481
5	*In situ*	0.320	72.4	106.7	1.1	1720
6	$P_2S_5/(NH_4)_2S_x$ (550 °C, 300 s)	1.46	10.3	3.8	1.7	245
7	$P_2S_5/(NH_4)_2S_x$ (600 °C, 60 s)	1.2	1.8	7.5	1.17	42
8	$(NH_4)_2S_x$ (550 °C, 300 s)	1.46	11.9	2.7	1.5	282
9	$(NH_4)_2S_x$ (600 °C, 60 s)	1.08	13.4	3.1	1.05	660

Table 5.2. The activation efficiency calculated from the active and total sulfur dose obtained from IRSE and SIMS measurements.

Sample # from Table 5.1	Chemical solution	Annealing condition	Active carrier dose (cm^{-2})	Total Sulfur dose (cm^{-2})	Activation Efficiency (%)
6	P_2S_5/ $(NH_4)_2S_x$	550 °C, 300 s	6.5×10^{12}	5.4×10^{14}	1.2
7	P_2S_5/ $(NH_4)_2S_x$	600 °C, 60 s	8.8×10^{12}	7×10^{14}	1.25
8	$(NH_4)_2S_x$	550 °C, 300 s	4.1×10^{12}	1.9×10^{14}	2.1
9	$(NH_4)_2S_x$	600 °C, 60 s	3.2×10^{12}	2×10^{14}	1.6

attributed to the higher impurity and surface scattering in the ultra- thin n^{++}-layers formed in the SMLD samples. N_D of ~1.1×10^{19} cm^{-3} was observed in the *in situ* samples regardless of $T_{n\text{-}InGaAs}$. This is consistent with the N_D of the *in situ* doped starting substrate (i.e. ~1×10^{19} cm^{-3}), and verifies the fitting accuracy of the Drude model. The n^{++}-InGaAs layers formed using SMLD were less than 10 nm thick, and had an N_D of ~ 1.05×10^{19} - 1.7×10^{19} cm^{-3}. The N_D and $T_{n\text{-}InGaAs}$ obtained were comparable to those reported by Kort *et al*. [325]. A larger $T_{n\text{-}InGaAs}$ can be observed for the samples annealed at 600 °C compared to those annealed at 550 °C. This reflects the trend observed in the SIMS shown in Fig. 5.8. The $T_{n\text{-}InGaAs}$ for $P_2S_5/(NH_4)_2S_x$ samples annealed at 550 °C was larger than that of the sample treated with $(NH_4)_2S_x$. This is also illustrated in the SIMS results [Fig. (5.8)].

R_S values of ~3 - 5 kΩ/□ were extracted for the sub-10 nm SMLD films from the IRSE measurements. This suggests that N_D higher than 1.7×10^{19} cm^{-3} is required in the ultra-thin n^{++}-InGaAs layers in order to meet the International Technology

Roadmap for Semiconductors (ITRS) target of R_S < 1 kΩ/□ [99]. R_S can be reduced by improving the activation efficiency. Further improvements in the activation efficiency can be achieved by employing dopant activation techniques such as spike annealing or laser annealing. The R_S obtained from IRSE was higher than that from the TLM structures, which could be due to the approximation of the n^{++}-layer as a box-type region. This discrepancy between IRSE and TLM results can be reduced by introducing active dopant profiles in the ellipsometry model. In order to obtain these active dopant profiles, techniques such as spreading resistance profiling (SRP) and electrochemical capacitance-voltage (ECV) measurements need to be developed for characterizing ultra-thin n^{++}-InGaAs junctions.

5.5 MOSFET Fabrication and Characterization

Planar InGaAs N- MOSFETs were fabricated to demonstrate the $P_2S_5/(NH_4)_2S_x$ SMLD technique. The process flow and schematics for the fabrication of the MOSFETs are shown in Fig. 5.12. The starting substrate consists of 50 nm thick $In_{0.53}Ga_{0.47}As$ and 500 nm thick $In_{0.52}Al_{0.48}As$ epitaxially grown on an InP substrate. The doping concentration of the InGaAs and InAlAs layers are same as that used in TLM fabrication [Section 5.2.3]. Pre-gate clean using HCl and ammonium hydroxide (NH_4OH) solutions was carried out to remove any native oxide and impurities on the InGaAs surface. Subsequently, surface passivation was done using $(NH_4)_2S_x$ solution. This was followed by gate stack deposition and post-deposition anneal at 300 °C for 60 s. The gate stack consists of a ~100 nm thick TaN metal gate layer on top of a ~5.5 nm thick Al_2O_3 dielectric layer. After gate patterning, Al_2O_3 was removed in the S/D regions using DHF (HF:H_2O = 1:100). The samples were then immersed in the $P_2S_5/(NH_4)_2S_x$ solution for 30 minutes, after which they were capped with a 15 nm thick SiO_2 layer followed by dopant activation anneal. Different annealing conditions were

used for dopant activation and their effects on the device performance were studied. Mesa isolation was then performed and palladium germanide (PdGe) S/D contacts were formed to complete the fabrication.

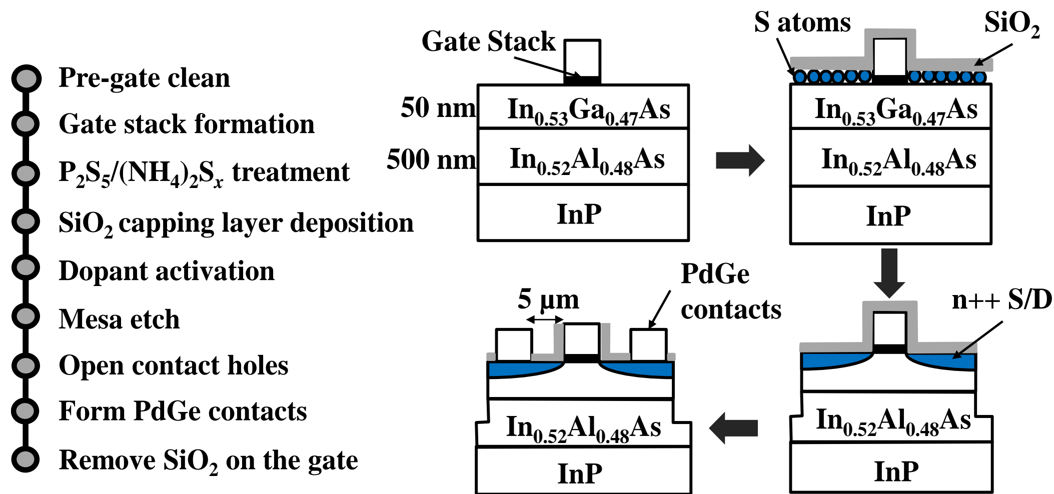


Fig. 5.12. The process flow for fabrication of InGaAs N-MOSFETs with S/D formed using $P_2S_5/(NH_4)_2S_x$ SMLD. Different dopant activation conditions were used.

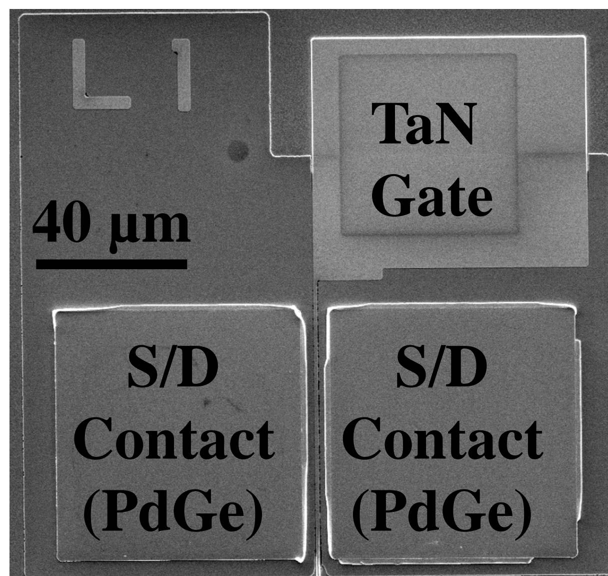


Fig. 5.13. Top-view SEM image of an InGaAs N-MOSFET with a gate length of 1 µm and with S/D regions doped by $P_2S_5/(NH_4)_2S_x$ SMLD. The dopants were driven in and activated by annealing at 600 °C for 180 s for this device.

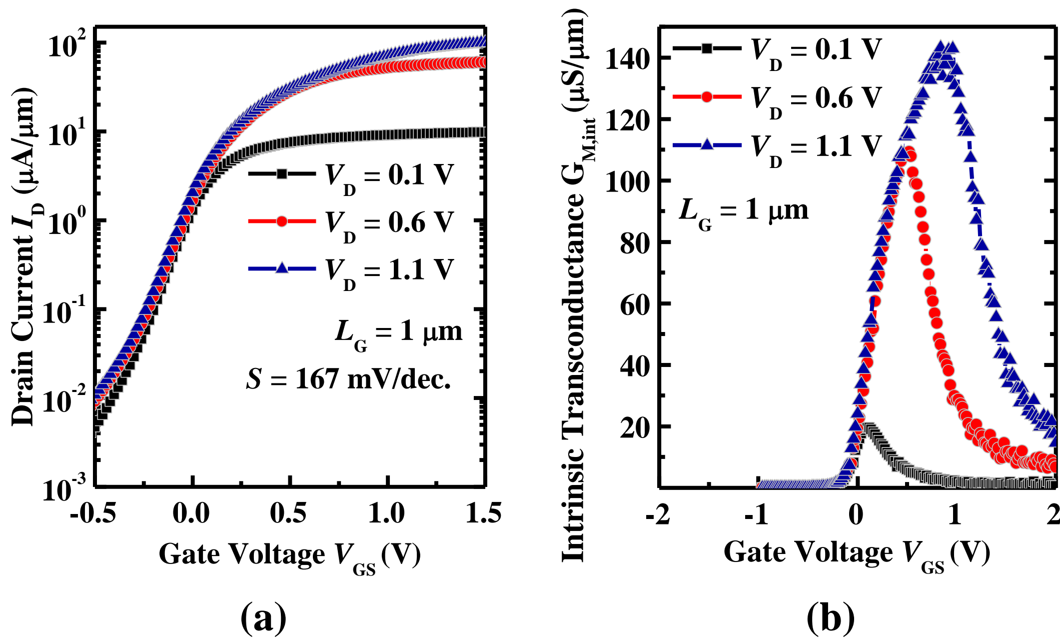


Fig. 5.14. (a) I_D-V_{GS}, and (b) $G_{M,int}$-V_{GS} characteristics of the planar transistor shown in Fig. 5.13. The device has a reasonable subthreshold swing (S) and negligible DIBL. Peak $G_{M,int}$ of 140 μS/μm can be observed at V_D of 1.1 V.

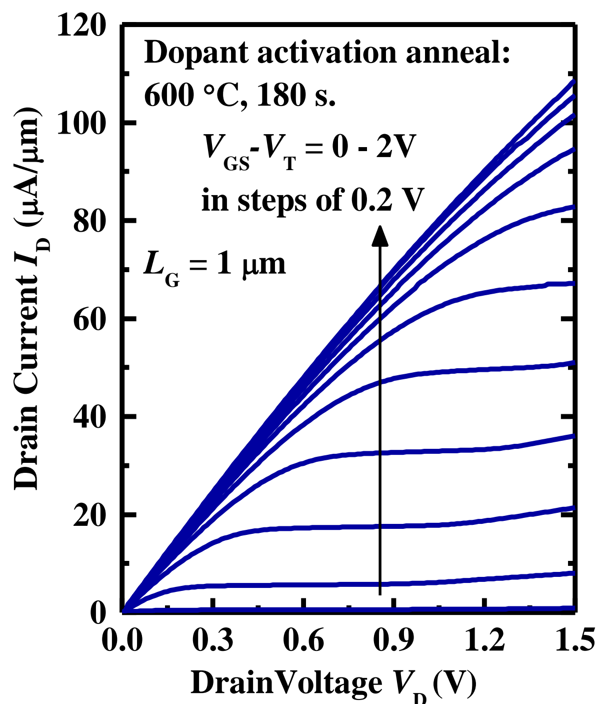


Fig. 5.15. I_D-V_D characteristics of the same device in Fig. 5.14, with gate overdrive (V_{GS} - V_T) varying from 0 V to 2 V in steps of 0.2 V. V_T was obtained using the maximum transconductance method [165]. The device suffers from high S/D resistance, as the current has to flow through the ultra-shallow doped region over a long distance of ~5 μm between the channel and the S/D contact.

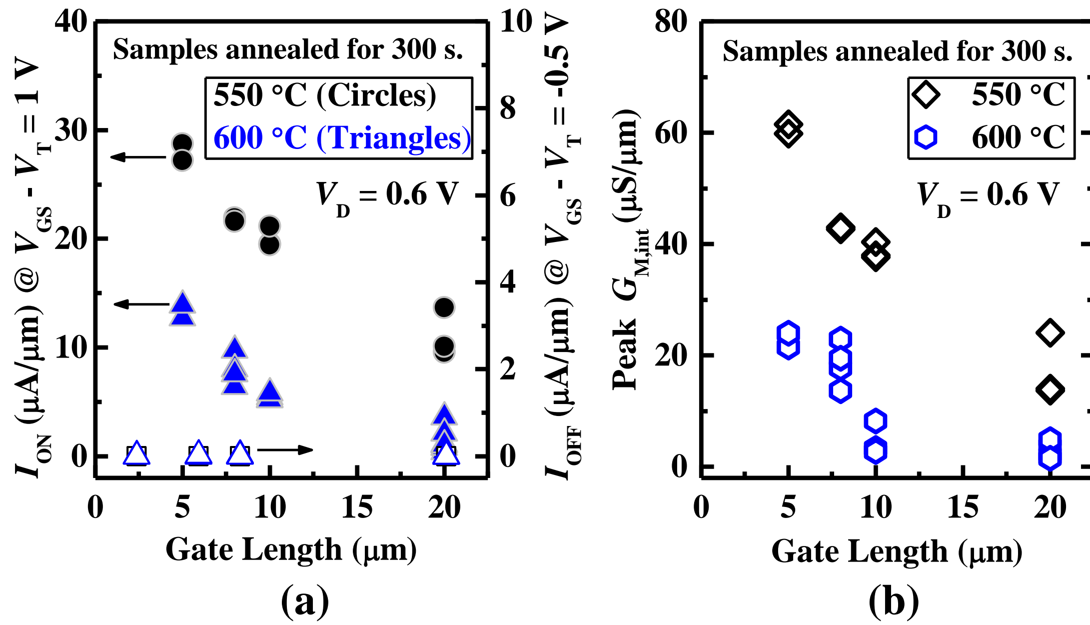


Fig. 5.16. (a) I_{ON} (solid symbols) at gate overdrive (V_{GS} - V_T) of 1 V, and I_{OFF} (open symbols) at (V_{GS} - V_T) of -0.5 V at V_{DS} of 0.6 V and (b) peak $G_{M,int}$ at V_D of 0.6 V are plotted as a function of the gate length. Comparison was made between samples with different annealing temperatures for dopant activation. The annealing time was kept fixed at 300 s. Using a lower thermal budget helps to achieve high I_{ON} and peak $G_{M,int}$.

Fig. 5.13 shows a top-view SEM image of a fabricated device with a gate length (L_G) of 1 µm. Dopant activation in the S/D regions of this device was achieved by annealing at 600 °C for 180 s. Drain current (I_D) and intrinsic transconductance ($G_{M,int}$) of the device are plotted versus gate voltage (V_{GS}) in Fig. 5.14. The slightly negative threshold voltage ($V_{T,lin}$ = -0.0677 V) can be attributed to the low doping in the channel and the work function of the TaN metal gate. The threshold voltage can be adjusted and made positive by using higher p-type doping in the channel or by using a metal gate with a higher work function. Gate stack degradation due to the high thermal budget in the dopant activation step results in the high subthreshold swing (S) as seen in Fig. 5.14. The device has a $G_{M,int}$ of ~140 µS/µm at V_D = 1.1 V. I_D is plotted versus the drain voltage (V_D) in Fig. 5.15 for the same device in Fig. 5.14. Since the current from the channel has to flow through the ultra-shallow n^{++}-layer in the S/D regions over a

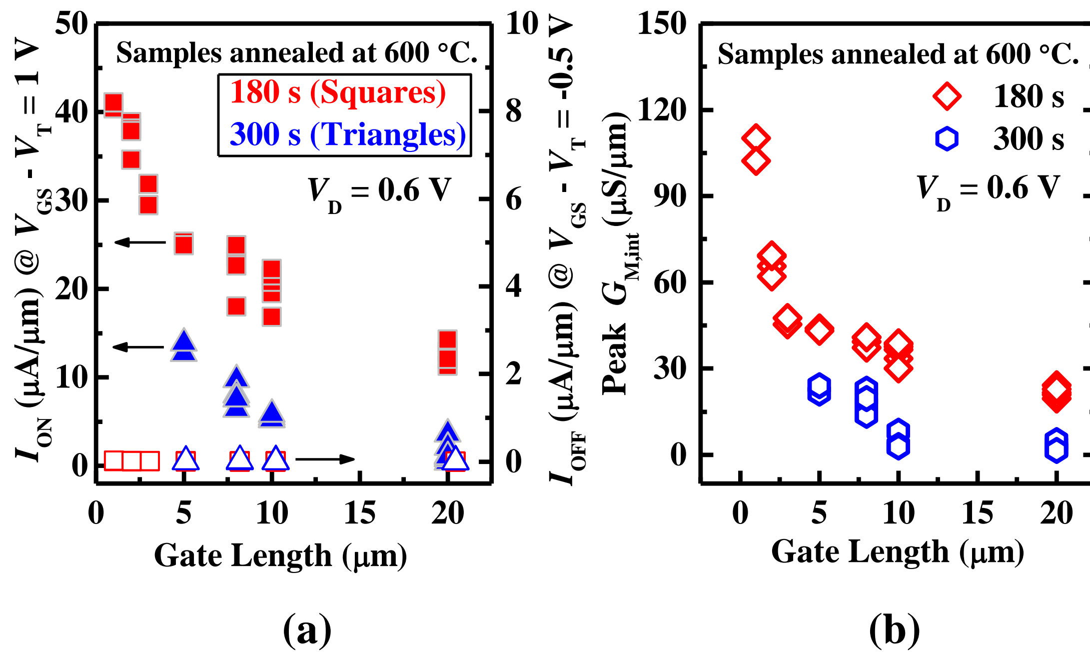


Fig. 5.17. (a) I_{ON} (solid symbols) at gate overdrive (V_{GS} - V_T) of 1 V, and I_{OFF} (open symbols) at (V_{GS} - V_T) of -0.5 V at V_D of 0.6 V and (b) peak $G_{M,int}$ at V_D of 0.6 V are compared for samples annealed at a fixed temperature of 600 °C for different durations. As in the case of lower annealing temperature, a shorter annealing time leads to a lower thermal budget, which gives better gate stack quality and therefore better device performance.

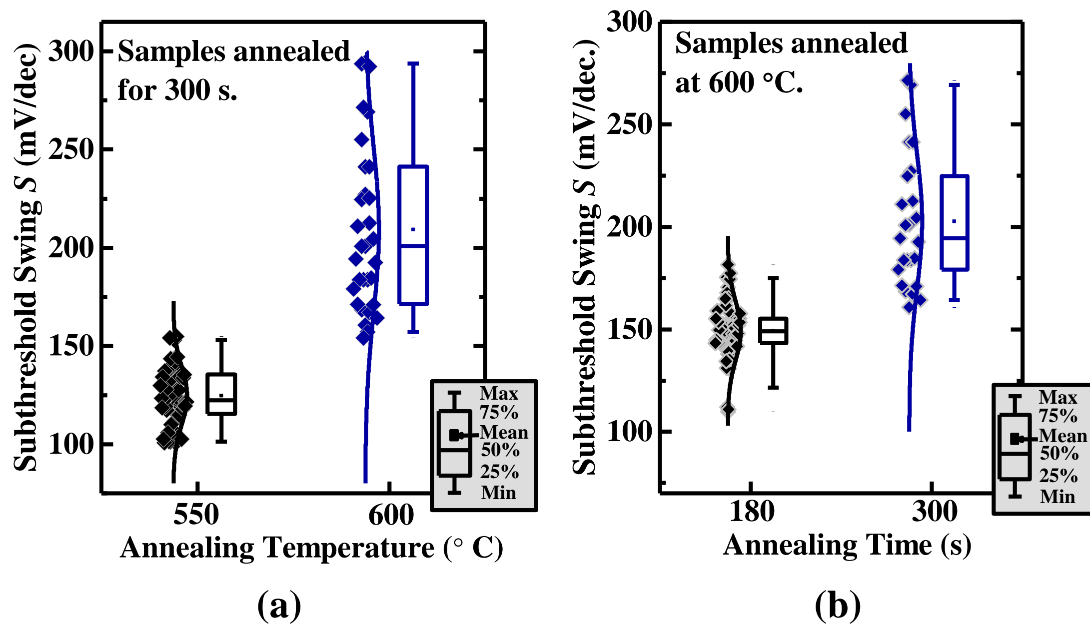


Fig. 5.18. Box plots showing the statistical distribution of S for devices with different dopant activation conditions. Comparison is made between samples with different (a) annealing temperatures and (b) annealing times. A higher thermal budget for dopant activation results in degradation of the gate stack, which leads to higher S. This can be avoided by using a gate-last process scheme.

distance of ~5 μm before it reaches the PdGe contacts, a large R_{SD} was observed. However, at future technology nodes, the SMLD process is best suited for doping the SDEs of devices where the metal contacts are a few nanometers away from the gate. These devices will have significantly lower R_{SD}. The resistance may be further reduced by increasing the dopant activation efficiency. This can be achieved by using techniques such as spike annealing or laser annealing, which can be used to apply higher annealing temperatures to improve the dopant activation. In addition, the shorter annealing time used in these methods reduce the diffusion of the dopants and does not compromise the junction depth.

The effect of different dopant activation conditions on the performance of the device was examined. There was a significant reduction in the ON-state current (I_{ON}) and peak $G_{M,int}$ at a gate overdrive (V_{GS} - V_T) of 1 V as the annealing temperature (Fig. 5.16) or time (Fig. 5.17) was increased. The I_{OFF} for all the devices was between 0.1 and 20 nA/μm. The reduction in I_{ON} and peak $G_{M,int}$ at increased thermal budgets can be attributed to the degradation of the interface between the gate dielectric and the channel. This was confirmed by the statistical distribution of the S for different dopant activation conditions (Fig. 5.18), which shows that an increase in thermal budget results in higher S for the devices. However, this will not be an issue if a gate-last scheme is used for device fabrication, where the S/D are formed before the gate stack formation.

5.6 Conclusion

SMLD using $P_2S_5/(NH_4)_2S_x$ solution was investigated for potential use in the formation of SDEs of InGaAs N-MOSFETs. The SMLD technique does not suffer from implant damage and has the potential to facilitate conformal doping for 3D structures in future logic device applications. Dopant activation was achieved at temperatures as

low as 550 °C for samples treated with $P_2S_5/(NH_4)_2S_x$. Sulfur profiles with steep slopes (< 1.5 nm/decade), which are required to achieve the abrupt and shallow junctions necessary for SDEs, were realized. A higher sulfur dose in the range of ~5.4×10^{14} cm^{-2} to ~7×10^{14} cm^{-2} was observed for samples treated with $P_2S_5/(NH_4)_2S_x$ compared to that of ~2×10^{14} cm^{-2} for samples treated with $(NH_4)_2S_x$, which resulted in higher N_D and lower R_S at dopant activation temperatures of 550 °C and 600 °C. The SMLD samples were characterized using IRSE. Parameters such as $\rho_{n\text{-InGaAs}}$, τ_e, and N_D were extracted from the shallow n^{++}-InGaAs films. This study suggests that IRSE is a useful technique to characterize heavily doped ultra-thin InGaAs films. Roughly 3-4 nm thick n^{++}-InGaAs layers were achieved using SMLD with N_D of as high as 1.7×10^{19} cm^{-3}. N_D higher than 1.7×10^{19} cm^{-3} is required to meet the ITRS target of R_S < 1 kΩ/□. Planar InGaAs N-MOSFETs, with S/D regions formed using $P_2S_5/(NH_4)_2S_x$-based SMLD, were demonstrated. The effect of the dopant activation conditions on device performance was studied. Higher annealing temperature or annealing time during dopant activation results in a degradation in I_{ON}, $G_{M,int}$, and S, which was due to gate stack degradation. This study suggests that a gate-last scheme is more suited for device fabrication to avoid the detrimental effect of the dopant activation anneal on the gate stack.

Chapter 6

Conclusion and Future Directions

6.1 Conclusion

'Power consumption' is a major limiting factor in further scaling of silicon (Si) metal-oxide-semiconductor field effect transistors (MOSFETs) for logic device applications. The power density in a semiconductor chip can be reduced by lowering the operating voltage (V_{DD}). However, as we reach the limits of mobility enhancement in Si MOSFETs, reducing V_{DD} would have a detrimental impact on the drive current and switching speed of the transistors. This can be resolved by replacing Si with a new channel material, in which the charge carriers travel at a much higher velocity. InGaAs, with its high electron mobility, is currently the most promising candidate to replace Si as the channel material in N-MOSFETs.

However, there are several challenges that need to be overcome before InGaAs can be used for mass production in the semiconductor industry. Some of these challenges include: high source/drain (S/D) resistances (R_{SD}) and high gate-to-drain capacitances (C_{GD}). Simple and cost efficient process technologies that reduce these parasitic components are vital in realizing high performance MOSFETs.

This thesis has explored and developed new process techniques and device architectures that can reduce R_{SD} in an InGaAs N- MOSFET without increasing the C_{GD} or process complexity. The contributions of this thesis are summarized in Section

6.2. In addition, suggestions on possible future directions for expanding on the research in this thesis are provided in Section 6.3.

6.2 Contributions of This Thesis

6.2.1 Selective Etching Process for the Formation of Self-Aligned Metallic S/D for InGaAs N-MOSFETs

A selective wet etching process for the removal of Ni over Ni-InGaAs was developed [326]. The study showed that HCl and HNO_3 based chemistries had high selectivities in etching Ni over Ni-InGaAs. It was also observed that the addition of Pt into Ni-InGaAs provided a larger process window during the selective etch process. The results of this study assisted in the realization of InGaAs N-MOSFETs with metallic self-aligned S/D [155], [226], [238], [327], [328]. Companies such as SEMATECH and TSMC (Europe) have shown interest in this work and are using it as a reference to develop a selective etching recipe that is suitable for industrial application.

6.2.2 *e*MSD Architecture for InGaAs N-MOSFETs with Self-Aligned Ni-InGaAs S/D

An *e*MSD architecture was proposed for InGaAs n-channel UTB-FETs, to reduce R_{SD}. This *e*MSD design is easier to fabricate and has a lower C_{GD} compared to a raised S/D architecture. InGaAs UTB-FETs with *e*MSD comprising of Ni-InGaAs and Ni-InAlAs were demonstrated [328]. This was achieved with the help of the selective etching process that was earlier developed (discussed in Chapter 3). For a channel thickness of 10 nm, a lower R_{SD} was obtained for the UTB-FET with *e*MSD compared to those with thin S/D reported in literature. Further analytical studies were performed using simulations to study the potential application of the *e*MSD architecture

in future technology nodes. The simulation study indicated that R_{SD} and C_{GD} that meet the International Technology Roadmap for Semiconductors (ITRS) requirements can be achieved for InGaAs N-MOSFETs by using the *e*MSD architecture.

6.2.3 $P_2S_5/(NH_4)_2S_x$-Based Monolayer Doping Technique for SDEs in InGaAs N-MOSFETs

In order to further reduce R_{SD}, sulfur monolayer doping (SMLD) technique using $P_2S_5/(NH_4)_2S_x$ solution was developed for use in the formation of S/D extensions (SDEs) in InGaAs N-MOSFETs [301], [329]. This technique helped in attaining sulfur profiles with steep slopes required to realize the abrupt and shallow junctions necessary for SDEs. Moreover, this technique has the potential for conformal doping which is needed for SDEs of 3D structures, such as fin field effect transistors (FinFETs) or nanowire transistors. The electrical and physical properties of the n^{++}-InGaAs layers formed using SMLD were characterized. Infrared spectroscopic ellipsometry was used to extract various parameters of the ultra-thin highly n-type doped (n^{++}) InGaAs layers formed using SMLD [329]. Sub-10 nm n^{++}-InGaAs films were realized with active doping concentration as high as 1.7×10^{19} cm^{-3}. The SMLD technique was demonstrated on planar InGaAs N-MOSFETs, and the effect of the dopant activation conditions on device performance was evaluated.

6.3 Future Directions

Although new and promising S/D engineering technologies were explored and developed in this thesis for advanced InGaAs N-MOSFETs, further work needs to be done to optimize and improve these technologies before they can be adopted in the semiconductor industry at future technology nodes.

The selective etching process explained in Chapter 3 was developed on blanket (unpatterned) samples. The etch rates and selectivities on patterned samples (where devices are densely packed) needs to be investigated, as they could be affected by effects such as micro and macro loading. Furthermore, the selective etch was developed using coupon size samples (1 cm × 1 cm). This process needs to be optimized for larger wafers (up to 450 mm in diameter) that are typically used in the semiconductor industry. The uniformity of the etching over such large areas also needs to be investigated.

The *e*MSD architecture needs to be demonstrated on short channel InGaAs transistors (UTB-FETs or FinFETs) to verify the results obtained from the simulation study explored in Chapter 4. In addition, to further reduce R_{SD} in the InGaAs UTB-FETs with *e*MSD, the ρ_C between Ni-InGaAs and n^{++}-InGaAs needs to be lowered to below 1×10^{-8} $\Omega\cdot cm^2$. Moreover, it is important to understand the reason behind the high ρ_C observed for Ni-InGaAs. This is in spite of the fact that the work functions of metals tend to pin near the conduction band of InGaAs. A possible reason for the high ρ_C could be due to the presence of interfacial layers such as excess elemental In, Ga, or As at the interface between Ni-InGaAs and InGaAs, after reaction of Ni with InGaAs. Preliminary studies performed by one of our collaborators shows that Ga out-diffuses during the formation of Ni-InGaAs. This results in non-stoichiometry of InGaAs at the interface between Ni-InGaAs and InGaAs, thus attributing to a high ρ_C. The study also shows that inserting a capping layer between Ni and InGaAs before the reaction can help to suppress the Ga out-diffusion. ρ_C as low as ~4×10^{-8} $\Omega\cdot cm^2$ on n^{++}-$In_{0.53}Ga_{0.47}As$ (with active donor concentration of 3×10^{19} cm^{-3}) have been achieved. This is the lowest ρ_C obtained for Ni-InGaAs contacts, making it a very promising material to be used as S/D contacts in InGaAs N-MOSFETs. Further work needs to be done to reduce ρ_C below 1×10^{-8} $\Omega\cdot cm^2$. This could be accomplished by increasing the doping

concentration and the indium content in the S/D regions. The material and the thickness of the capping layer are some of the other parameters that can be varied to reduce ρ_C, and in turn the R_{SD}.

Further optimization is required for the SMLD technique to lower the R_{SD}. This can be done by improving the dopant activation efficiency. The activation efficiency can be improved by employing techniques such as spike annealing and laser annealing. Similarly, choosing the correct material for capping layer is critical to achieve higher activation efficiencies [298]. Although, the SMLD process was successfully demonstrated on planar $In_{0.53}Ga_{0.47}As$ N-MOSFETs, the feasibility of this doping technique for 3D devices such as FinFETs and nanowire transistors needs to be explored.

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Appendix

List of Publications

Journal Publications

1. **S. Subramanian**, Ivana, Q. Zhou, X. Zhang, M. Balakrishnan, and Y.-C. Yeo, "Selective wet etching process for Ni-InGaAs contact formation in InGaAs N-MOSFETs with self-aligned source and drain," *Journal of the Electrochemical Society*, vol. 159, no. 1, pp. H16 - H21, 2012.
2. **S. Subramanian**, E. Y.-J. Kong, D. Li, S. Wicaksono, S. F. Yoon, and Y.-C. Yeo, "$P_2S_5/(NH_4)_2S_x$-Based Sulfur Monolayer Doping for Source/Drain Extensions in N-Channel InGaAs FETs", *IEEE Transactions on Electron Devices*, vol. 61, no. 8, pp. 2767-2773, 2014.

Conference Publications

1. **S. Subramanian**, Ivana, and Y.-C. Yeo, "Embedded metal source/drain (eMSD) for series resistance reduction in $In_{0.53}Ga_{0.47}As$ n-channel ultra-thin body field-effect transistor (UTB-FET)," *International Symposium on VLSI Technology, Systems, and Applications* (*VLSI-TSA*), pp. 1-2, 2012.
2. **S. Subramanian**, E. Y.-J. Kong, D. Li, S. Wicaksono, S. F. Yoon, and Y.-C. Yeo, "$P_2S_5/(NH_4)_2S_x$-based sulfur mono-layer doping technique to form sub-10 nm ultra-shallow junctions for advanced III-V logic devices," *International Conference on Solid-State Devices and Materials* (*SSDM*), 2013.

Publications as co-author

1. V. R. D'Costa, **S. Subramanian**, D. Li, S. Wicaksono, S. F. Yoon, and Y.-C. Yeo, "Infrared spectroscopic ellipsometry study of sulfur-doped $In_{0.53}Ga_{0.47}As$ ultra-shallow junctions," *Applied Physics Letters*, vol. 104, pp. 232102, 2014.