INTERFACE STUDIES FOR MICROCRYSTALLINE SILICON THIN-FILM SOLAR CELLS DEPOSITED ON TCO-COATED PLANAR AND TEXTURED GLASS SUPERSTRATES

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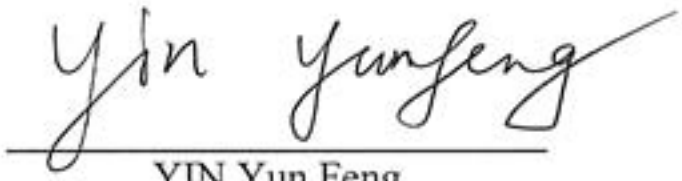
DECLARATION

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.



YIN Yun Feng
15 August 2014

Acknowledgement

A PhD is a really long and challenging journey. On the way, it is full of thorns and rocks. Often, you will feel exhausted - and sometimes even overwhelmed. Loneliness and depression may harass at times. However, it is also covered by the flowers and fruits, which can be obtained only when you reach the destination. Those who experience this process can really understand the hardship of a PhD. Here, I would like to deliver my sincere appreciation to those who gave me help materially and/or mentally during my four years of PhD life. Without their support, I may have fallen down in the half way and couldn't finish this journey at the end.

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Abstract:

An interface optimization for microcrystalline silicon (µc-Si:H) thin-film solar cells on glass superstrates is undertaken, focusing on the two most important interfaces of this type of solar cell: the most important interface regarding the electrical solar cell performance (i.e. the p/i interface and buffer layers being inserted at the p/i interface) as well as the most important interfaces regarding the optical solar cell performance (i.e. the textured glass/TCO interface as well as the textured TCO/µc-Si:H interface). The influence of the surface morphology on the µc-Si:H thin-film growth and on the solar cell performance is investigated. First, a standard thin-film µc-Si:H deposition process is established at SERIS (baseline). Then, the boron-doped µc-Si:H p-layers (< 30 nm thick) are optimized on different types of glass superstrates, by using a "layer-by-layer" deposition method. A wide crystallinity range (i.e. 0 - 70 %) and high conductivity (> 1 S/cm) is achieved by using this novel deposition method. Next, different buffer layers (e.g. intrinsic a-Si:H and intrinsic µc-Si:H layers with different crystallinity) are introduced at the p/i interface, and their influence on the solar cell performance is investigated experimentally. A 10 - 20 nm thick amorphous buffer layer with percolated µc-Si:H grains is shown to be the optimum buffer layer in terms of solar cell efficiency improvement. Numerical simulations are used to explain the main phenomena observed when introducing a buffer layer at the p/i interface of the solar cell. Finally, textured glass superstrates are investigated for the use in µc-Si:H thin-film solar cell processing. The light scattering and the corresponding short-circuit current I_{sc} enhancement of µc-Si:H solar cells deposited on aluminium-induced textured (AIT) glass superstrates (using a recently patented industrial viable glass structuring technology) having a double-texture (i.e. micro-textured glass and nano-textured TCO) was investigated. An I_{sc} enhancement using AIT glass superstrates could be

demonstrated compared to the conventional standard planar glass superstrates covered with nano-textured TCO. However, thus far, also an increase in local shunt formation has been observed. A further increase of the autocorrelation length (i.e. the mean feature size) of the textured glass shows a large potential to improve the μc-Si:H thin-film solar cell efficiency, by reducing the shunting probability of the device while maintaining a high optical scattering performance.

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ΔE_F: Quasi Fermi level splitting

Δn: Excess carrier density

Ec/ΔEc: Conduction band/conduction band offset

$E_F/E_{Fe}/E_{Fh}$: Fermi level/electron quasi Fermi level/hole quasi Fermi level

E_{ff}: Conversion efficiency

EQE/IQE: External quantum efficiency/Internal quantum efficiency

Ev/ΔEv: Valence band/valence band offset

FF: Fill factor

G: Generation rate

H: Haze value

J_o: Diode saturation current density

J_{sc}: Short-circuit current density

K: Boltzmann constant

l: Autocorrelation length

L_{diff}: Effective diffusion length

L_{drif}: Drift-assisted length

pFF: Pseudo fill factor

R_s: Series resistance

R_{shunt}: Shunting resistance

SC: Silane concentration

U: Recombination rate

V_{oc}: Open-circuit voltage

σ: Dark conductivity

τ: Minority carrier lifetime

Φ_B^h: Effective barrier height at the valence band for hole

List of Nomenclature

µc-Si:H:	Hydrogenated microcrystalline silicon
AFM:	Atomic force microscopy
AIT:	Aluminium-induced texture
ASA:	Advanced Semiconductor Analysis programme
a-Si:H:	Hydrogenated amorphous silicon
EBIC:	Electron beam induced current
FIB:	Focused ion beam
HWCVD:	Hot wire chemical vapour deposition
LBL:	Layer by layer
p/i interface:	p-layer/i-layer interface
PECVD:	Plasma-enhanced chemical vapour deposition
SEM:	Scanning electron microscopy
TCO:	Transparent conductive oxide
VHF:	Very high frequency
XTEM:	Cross-sectional transmission electron microscopy

List of publications arising from this thesis

Journal papers:

[1] **Y. Yin**, J. Long, S. Venkataraj, J. Wang and A.G. Aberle, Fabrication of high-quality boron-doped microcrystalline silicon thin films on several types of substrates, Energy Procedia 25 (2012) 34-42.

[2] J. Long, **Y. Yin**, S.Y.R. Sian, Z. Ren, J. Wang, P. Vayalakkara, S. Venkataraj and A.G. Aberle, Doped microcrystalline silicon layers for solar cells by 13.56 MHz plasma-enhanced chemical vapour deposition, Energy Procedia 15 (2012) 240-247.

[3] **Y. Yin**, N. Sahraei, S. Venkataraj, S. Calnan, S. Ring, B. Stannowski, R. Schlatmann, A.G. Aberle and R. Stangl, Light scattering and current enhancement for microcrystalline silicon thin-film solar cells on aluminum-induced-textured glass superstrates with double texture, submitted to Thin Solid Films (August 2014).

[4] **Y. Yin**, N. Sahraei , S. Venkataraj, C. Ke, S. Calnan, S. Ring, B. Stannowski, R. Schlatmann, A.G. Aberle and R. Stangl, The thin-film growth study and structural defect characterization for microcrystalline silicon on aluminum-induced-textured glass having microscale surface texture, submitted to Journal of Non-Crystalline Solids (August 2014).

Conference papers:

[1] **Y. Yin**, J.D. Long, S. Venkataraj, Z.K. Ren and A.G. Aberle, The influence of an intrinsic buffer layer near the p/i interface on the performance of microcrystalline silicon thin-film solar cells. Proc. 27th European Photo-voltaic Solar Energy Conference, 2012, Germany, pp. 2576-2578.

[2] P. Vayalakkara, S. Venkataraj, J. Wang, J. Long, Z. Ren, **Y. Yin**, P.I. Widen-borg and A.G. Aberle, Aluminum induced glass texturing process on borosilicate and soda-lime glass superstrates for thin-film solar cells, Proc. 37th IEEE Photovoltaic Specialists Conference (PVSC), 2011, pp. 003080-003083.

Chapter 1: Introduction

PV as a means to reduce the greenhouse effect

Human society did develop at a very high speed during the last centuries, however at the cost of exhausting a huge amount of natural resources and causing severe environmental pollution. The greenhouse effect (an observed global temperature increase on earth, which is attributed to gas emission, primarily CO_2, into the atmosphere during the last two centuries) has attracted worldwide attention in recent years. One of the major reasons for the continuous increase of CO_2 emissions is the sharp rise of continuous demand for more energy consumption, mainly due to a steadily increasing demand from industrial use, public facilities (traffic) as well as individual housing (heating). Therefore, it deems necessary to look for some new and green methods to cover the ever increasing demand for energy. Meanwhile, an international long-term goal has been set up to reduce worldwide greenhouse gas emissions towards half the amount of today by 2050, and to build up a low-carbon society [1]. Solar energy, which is widely considered as an environment-friendly, sustainable and renewable energy source, brings us hope to solve these problems.

It is now expected by many that photovoltaic (PV) power generation will play an important role in the reduction of CO_2 emissions and power supply in the future [2]. Besides, further improving the conversion efficiency of the solar cells and PV modules is still a critical step in order to promote the worldwide application of PV systems. According to a roadmap for the development of PV systems, PV2030+ [3], a conversion efficiency of 25 % is targeted for PV modules by 2025. In a long-term view, PV systems are expected to achieve ultra-high efficiency by 2050, targeting an energy conversion efficiency of 40 % or higher at a much lower manufacturing cost than today.

By 2100, most of the fossil energy resources on earth are very likely consumed and new candidates for energy supply must be chosen. Solar energy does have a great potential to serve as the main energy source at that point in time. Hence, the research and development of PV technologies is a long-term project to develop a continuous stable energy resource. This important kind of research will have to be carried on in the near-term as well as in the long-term future.

Current status of PV development

Concerning the development of the various PV technologies, the deployment of PV modules progressively increased in recent years. In 2013, the global PV module production reached approximately 40 GW [4]. Crystalline silicon (c-Si) wafer-based products (including multi and mono c-Si) made up about 90% of module production in 2013 (see Figure 1.1). Furthermore, roughly 75 % of the c-Si module output was multi c-Si. The c-Si products dominate the market because of their relatively high efficiency (as compared to thin-film technologies) and because of the continuous drop of the price of solar-grade silicon wafers.

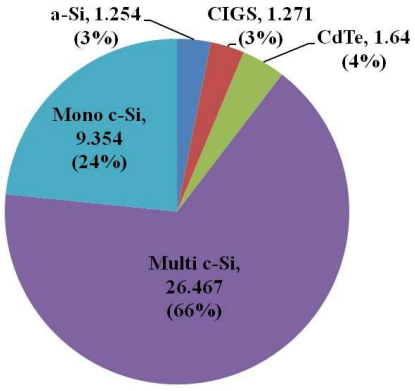


Figure 1.1: Global PV module production (in GW) categorized by technology in 2013 [4]. The share of each technology in percent is indicated in brackets.

On the other hand, thin-film PV technologies, such as copper-indium-gallium-selenide (CIGS), cadmium telluride (CdTe) and silicon thin-film solar cells (i.e. a-Si:H and µc-Si:H solar cells as well as their tandem version, i.e. an a-Si:H/µc-Si:H

double-junction solar cell, which is also called a “micromorph” solar cell), have a relatively low market share, which declined from 19 % in 2009 to around 10 % in 2013 [4]. All the various thin-film products (CIGS, CdTe, thin-film Si) have very similar market share of around 3 - 4 %, with CdTe solar cells having the highest production volume (1.64 GW) followed by CIGS (1.27 GW) and Si thin-film (1.25 GW), see Figure 1.1. To maintain or even increase the market share, it is critical to further improve the efficiency of the various thin-film solar cells and to further reduce the cost of thin-film PV modules.

Current status of thin-film PV development

Although currently the solar cell efficiency of thin-film technologies still lags behind wafer based c-Si technology, thin-film technologies have their own advantages and potential. For thin-film technologies, a small quantity of photoactive material is needed, as the absorber layers are only several hundreds of nanometres or a few micrometres thick. These layers can be obtained directly from the deposition from the gas phases, thus avoiding expensive crystallization technology and material consuming sawing technology. Besides, the total number of the processing steps is largely reduced as compared to the full production chain for c-Si solar cells, for example the module production process for thin-film technology can be directly integrated into the cell production process ('monolithic integration'). As a consequence, the thin-film technologies have the advantage of comparatively low production costs per unit area. At the same time, as compared to the wafer-based technology, thin-film technology also shows the prospect of much lower energy pay-back time [2]. In addition, thin-film solar cells can be fabricated on flexible substrates, such as polymer or stainless steel foils, and they provide a wider range of potential applications in different areas [5, 6]. However, as mentioned above, thin-film technology still suffers from the major issue of low conversion efficiency. Also

transferring the technologies developed in the laboratories towards mass production in industry is still a big challenge.

Among the various thin-film PV technologies, silicon thin-film technologies - including amorphous silicon (a-Si:H) and microcrystalline silicon (μc-Si:H) as well as their related alloys - have the advantages that they have abundant raw material supply and that they already have succeeded in other industrial sectors, such as flat-panel displays. It has been reported that the worldwide capacity for a-Si:H thin-film solar cell manufacturing reached 10 GW by the end of 2010 [7]. But at present, as compared to the other two thin-film technologies CIGS and CdTe, silicon thin-film PV still has a significantly lower conversion efficiency: CIGS solar cells can reach an efficiency of 20.8 % [8-10], and CdTe solar cells also have reached values above 20 % [11], whereas the thin-film silicon solar cell efficiency, even when using double-junction or triple-junction concepts, is still in the 12.0 - 13.4 % range, see Table 1.1

Table 1.1 The current status of silicon thin-film solar cells and modules.

Material and structure	Conversion efficiency (%)	Area (cm^2)	V_{oc} (V)	J_{sc} (mA/cm^2)	FF (%)	Measurement institution and date	Notes
Official data published in Progress in Photovoltaics "Solar cell efficiency tables (version 43)"[9]							
a-Si single junction	10.1 ± 0.3	1.036	0.886	16.75	67.8	NREL (7/09)	Oerlikon Corp. SCE
microcrystalline Si single junction	10.8 ± 0.3	1.036	0.523	28.24	73.2	AIST (9/13)	AIST
a-Si/nc-Si tandem cell	12.3 ± 0.3	0.962	1.365	12.93	69.4	AIST (7/11)	Kaneka Corp. SCE
a-Si/nc-Si tandem module	13.4	3827	136.7	510 (mA)	73.7	AIST (10/05)	Kaneka Corp. ICE
a-Si/a-Si/a-SiGe triple junction	12.1 ± 0.7	0.27	2.297	7.56	69.7	NREL (10/96)	USSC. SCE
a-Si/nc-Si/nc-Si triple junction	13.4 ± 0.4	1.006	1.963	9.52	71.9	NREL (7/12)	LG Electronic
a-Si/a-SiGe/ a-SiGe module	10.4 ± 0.5	905	4.353	3.285 (A)	66.0	NREL (10/98)	USSC. SCE
a-Si/a-SiGe/nc-Si module	10.5 ± 0.4	14316	224.3	0.991 (A)	67.9	AIST (9/12)	LG Electronic

ICE: initial conversion efficiency
SCE: stabilized conversion efficiency

This gap in efficiency is the critical bottleneck that limits its development and competition with other types of solar cells. Table 1.1 shows the present status of silicon thin-film solar cells and their related modules, as reported by either research institutes or solar companies. For single-junction solar cells (i.e. a-Si:H or µc-Si:H cells), the best achieved efficiencies are around 10 - 11 % (after initial degradation, i.e. stabilized conversion efficiency, named SCE in Table 1.1). For tandem solar cells (i.e. a-Si:H/µc-Si:H), the initial efficiency can reach values above 14 %, but the stable efficiency is still around 12 - 13 %. Thus the efficiency improvement for the single-junction cells enabling an efficiency improvement for the corresponding multi-junction cells is still the most important task for future development of silicon thin-film PV.

Hydrogenated microcrystalline silicon (µc-Si:H) thin-film solar cells

Considering a-Si:H single-junction solar cells, an optimized initial conversion efficiency can reach values as high as 10 - 12 %, using an ~300 nm thick silicon a-Si:H(i) film as a solar cell absorber [12]. However, a-Si:H solar cells suffer from a serious light induced degradation (LID), due to the Staebler-Wronski effect [13]. The solar cell efficiency degrades by up to 20 % relative due to initial exposure to sunlight, until it finally stabilizes. As a result, the best-achieved stable a-Si:H conversion efficiency nowadays is about 10 %, as shown in Table 1.1. Furthermore, a-Si:H solar cells have very poor red response, meaning that their spectral response is negligible for excitation wavelengths larger than 800 nm, because the a-Si:H bandgap is typically in the range of 1.7 - 1.8 eV. In order to make use of the near-infrared band of the solar spectrum (AM1.5 spectrum), tandem solar cell approaches are pursued. Typically, a combination of an a-Si:H top cell with a thin-film silicon bottom cell (having a lower bandgap) is needed, such as a-SiGe (1.4 eV) or µc-Si:H (1.1 eV). Considering a-SiGe, it also suffers from the Staebler-Wronski effect, i.e. there is a significant efficiency reduction during initial exposure to sunlight. Hydrogenated

microcrystalline silicon, µc-Si:H, is a much better thin-film silicon candidate for a bottom cell in a tandem configuration, as it exhibits a nearly perfect bandgap for near-infrared light and nearly no LID. The work of this thesis therefore focuses on the study of efficiency improvement potentials for µc-Si:H thin-film solar cells. Currently, the best-achieved stable single-junction µc-Si:H solar cell efficiency is around 10.8 %, while the corresponding value of a-Si:H/µc-Si:H tandem solar cells is around 12.3 %, see Table 1.1. Thus the efficiency enhancement for single-junction µc-Si:H solar cells is imperative to the efficiency enhancement and practical application of tandem thin-film silicon solar cells.

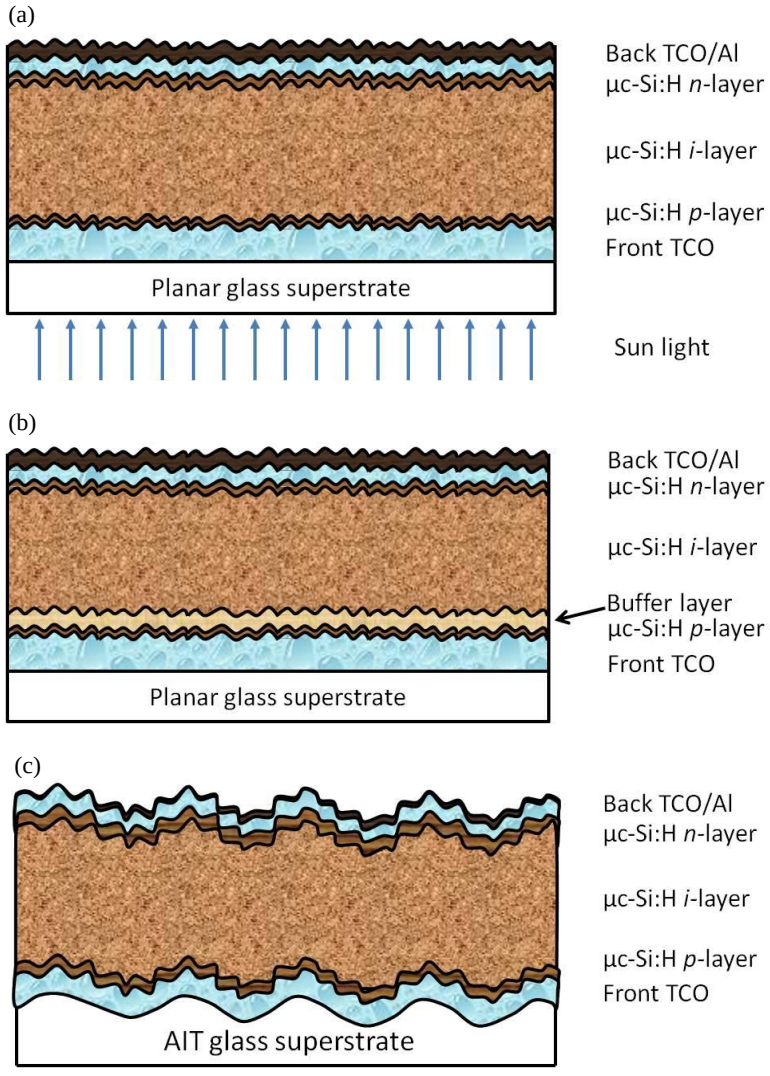


Figure 1.2: Schematics of (a) conventional µc-Si:H solar cell structure; (b) µc-Si:H solar cell having a buffer layer introduced at the p/i interface; (c) µc-Si:H solar cell using a double-textured superstrate, i.e. microtextured glass covered with nano-textured TCO.

A typical structure of a single-junction μc-Si:H thin-film solar cell is illustrated in Figure 1.2(a). It has a p-i-n superstrate configuration (i.e. the sunlight enters the solar cell through the glass superstrate), consisting of electrically active μc-Si:H multi-layers (doped/intrinsic/doped μc-Si:H) sandwiched between two transparent conductive oxide layers (TCOs) and therefore containing many interfaces. It has been reported that optimized interfaces are essential for achieving high-efficiency μc-Si:H thin-film solar cells [14-20]. Interfaces between the electronically active layers of the μc-Si:H solar cell are very crucial for the electrical performance of the solar cells, especially the p-layer/i-layer interface (p/i-interface), which is near to where most of the photo-generated electron-hole pairs are created. Therefore, this interface has great influence on the blue response in the quantum efficiency (QE) of μc-Si:H solar cells, affecting the final short-circuit current as well as the open-circuit voltage of the solar cell [19-23], and therefore needs careful optimization. Various buffer layers, such as a-Si:H and SiO_x, have been inserted at this interface in order to improve the μc-Si:H solar cell performance [21-23]. Given the importance of the p/i interface, a systematic study of different buffer layers modifying the electronic performance of this interface should be carried out. This has not been done so far, and thus will be performed in this thesis. Other interfaces, such as the glass/TCO and TCO/μc-Si:H interfaces, are especially important for the optical performance of μc-Si:H solar cells, as they determine the light scattering and light trapping ability for μc-Si:H, especially within the long-wavelength range (i.e. for photons with a wavelength above 700 nm). Without careful optimization, these interfaces may even become the main loss mechanism of the μc-Si:H solar cell efficiency [14, 20, 22]. Typically, the front TCO layer is textured by wet-chemical etching, leading to a single-textured nanotextured TCO/μc-Si:H interface [14, 15]. Using a double texture, i.e. additionally deploying a microtextured glass/TCO interface is reported to be able to significantly increase the short-circuit current of the μc-Si:H solar cell [24]. In this thesis, an industrially compatible glass texturing process, namely the aluminium-induced texture (AIT),

which has recently been developed and patented [25, 26], is used to investigate the influence of using a double-texture for μc-Si:H solar cells in order to enhance light trapping.

Improving the electrical performance of μc-Si:H solar cells: Investigation of buffer layers being introduced at the p/i-interface

To improve the electrical performance of a μc-Si:H solar cell, a buffer layer introduced at the p/i interface can improve the solar cell efficiency [21-23, 27-30], as illustrated in Figure 1.2(b). Different buffer layers at the p/i interface function differently. Some buffer layers can serve as barrier layers to suppress impurity diffusion [21]. Other buffer layers serve as seeding layers to facilitate the growth of the μc-Si:H i-layer [31]. Finally, some other buffer layers use the so-called "electrical quenching effect" to suppress the diode current J_0 and improve the open-circuit voltage of the solar cell [22, 23]. However, little work has been done in previous studies in relation to a comparison of various buffer layers. In this study, various buffer layers processed by various methods are used to investigate their overall impact on the solar cell's electrical performance. A comparison will be made to select the one which contributes the most to the PV efficiency. Furthermore, the role of the various buffer layers and their influence on the solar cell efficiency will be analysed by means of numerical computer simulation. Up to now, most of the research work mainly focused on the experimental investigation of inserting one specific buffer layer at the p/i interface. The theoretical understanding of buffer layers and their impact on the μc-Si:H thin-film solar cell performance is still quite limited [32], and a comparative study of different buffer layers is missing to the author's knowledge. Both will be provided within this thesis, using the "Advanced Semiconductor Analysis" (ASA) software developed by TU Delft university [33, 34], in order to support experimental results comparing various buffer layers to the same standard reference, i.e. a μc-Si:H thin-film solar cell without a buffer layer.

Improving the optical performance of μc-Si:H solar cells: Investigation of a double-textured superstrate using aluminium-induced texture glass (AIT glass)

To improve the optical performance of the solar cell, conventional TCO texturing achieved by either using wet-chemical surface etching [14, 15] or by growing a TCO layer with natural surface texture [35] and providing a nanotextured TCO surface, is used for light trapping. It provides good light trapping properties for wavelengths up to 650 nm, but the scattering ability for near-infrared light (700 - 1100 nm) is quite modest. Recently, glass texturing techniques, such as imprint texturing [36] or ion-etch texturing [37], leading to a microtextured glass surface, have been proposed in order to improve the scattering ability for infrared light. However, these techniques do not seem to be industrially feasible for PV applications. In this study, we propose the aluminium-induced texture (AIT) method for glass texturing, which was developed in the last 10 years and patented [25, 26, 38], and which is believed to be industrially feasible, i.e. be compatible with large-area, high-throughput, low-cost processing [26, 38]. Thus, a double-textured glass superstrate, consisting of micro-textured AIT glass and nanotextured TCO (using wet-chemical etching) is investigated, as shown in Figure 1.2(c). The AIT method enables us to obtain an industrially feasible microtextured glass surface with typical feature size in the range of 1-3 μm (‘AIT glass’). Using a double-textured superstrate (consisting of microtextured glass covered with nanotextured TCO), a further improvement of the light trapping ability within the μc-Si:H solar cells seems possible. The corresponding short-circuit current enhancement as compared to using a conventional single-textured superstrate (consisting of planar glass covered with nanotextured TCO, see Figure 1.2(a)), will be investigated in this thesis.

It is well known that the growth of μc-Si:H layers depends on the surface morphology of the superstrate [39]. Quite often, when μc-Si:H is deposited onto microstructured surfaces, an increase of the number of local shunts (defective regions) is observed, degrading the solar cell efficiency [40]. Thus, the influence of the

μc-Si:H film growth when processed on AIT glass superstrates will also be investigated.

Structure of this thesis

Chapter 1 highlights the importance of the exploitation of solar energy and gives a general review of the current status of various PV technologies. As discussed above, it is important to improve the efficiency of single-junction Si thin-film solar cells. This thesis mainly focuses on the study of improving the efficiency of μc-Si:H thin-film solar cells. In **Chapter 2**, some background information and a literature review relevant to the research topics in this thesis are given. A reference μc-Si:H deposition process for intrinsic and boron-doped layers is established, as briefly described in Appendix B. Based on the standard μc-Si:H deposition process established on planar glass, **Chapter 3** describes the development of a high-quality boron-doped μc-Si:H window layer on different superstrates, i.e. planar glass and textured glass (bare or coated with a TCO layer), using the "layer-by-layer" deposition method. **Chapter 4** investigates the introduction of different buffer layers at the p/i interface of μc-Si:H thin-film solar cells. Four different types of buffer layer were applied experimentally, using three different deposition methods: (1) amorphous buffer layers, (2) amorphous buffer layers with isolated μc-Si:H grains, (3) amorphous buffer layers with percolated μc-Si:H grains, and (4) highly crystallized buffer layers. The influence of these buffer layers and their thickness variation on the I-V performance of the solar cell is experimentally investigated. Using numerical computer simulation, **Chapter 5** studies the influence of these different buffer layers, including a thickness variation, on the I-V performance theoretically, enabling us to explain the main experimental observations. To improve the light trapping ability, **Chapter 6** investigates the use of double-textured superstrates, consisting of microtextured AIT glass covered with a nanotextured TCO layer, for μc-Si:H thin-film solar cell applications. The surface morphology of the various superstrates used (i.e. a conventional single nanotextured

TCO reference superstrate, compared to two different double-textured AIT superstrates, using an intermediate or a large feature size for the microtextured glass) and the corresponding impact on the thin-film light scattering as well as on the thin-film μc-Si:H growth are investigated. Finally, **Chapter 7** provides a brief summary of the results obtained in this thesis, as well as a list with some recommended future work.

Chapter 2: Background and literature review

2.1 Hydrogenated microcrystalline silicon (µc-Si:H) thin-films

Generally, according to the arrangement of the atoms, silicon can be categorized into crystalline and amorphous silicon. As shown in Figure 2.1, crystalline silicon has an ordered structure and the silicon atoms are arranged in a periodic lattice. For amorphous silicon, the atom arrangement is disturbed and the length and the angle of the bonds between silicon atoms vary (for example, the bond angle has a variation of up to 10°). Therefore, there is no long-range order of the atoms in an amorphous Si sample, although the short-range order is still kept. Hydrogenated microcrystalline silicon (µc-Si:H) is a mixed-phase material containing both crystalline silicon regions and amorphous silicon regions. It can be considered as crystalline zones being embedded within an amorphous silicon lattice network, as shown in Figure 2.1(c).

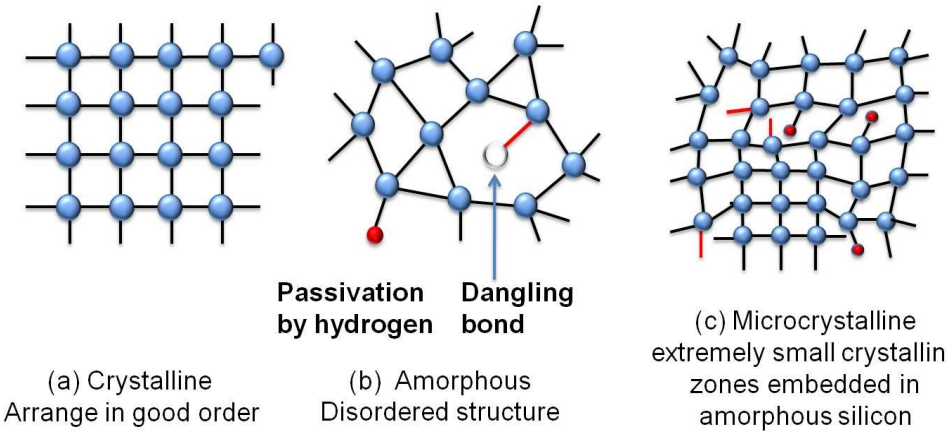


Figure 2.1: Simplified schematic of various silicon thin-film lattice structures, i.e. (a) crystalline silicon, c-Si or epi-Si, (b) amorphous silicon, a-Si:H, (c) microcrystalline silicon, µc-Si:H.

The crystalline volume fraction (or 'crystallinity') is a significant parameter to determine the electrical and optical properties of thin-film µc-Si:H. For example, the bandgap of a µc-Si:H layer increases as the crystallinity decreases (i.e., as more a-Si:H is contained in the film) [41, 42]. The bandgap of a typical µc-Si:H thin-film layer as used in solar cells is about 1.18 eV [43], which is very close to that of c-Si (1.12 eV). Besides, µc-Si:H can absorb photons with wavelengths up to 1100 nm, while a-Si:H absorbs only up to 800 nm. Therefore, thin-film µc-Si:H is in principle a suitable absorber for the red/infrared part of the solar spectrum. However, compared to thin-film a-Si:H it has only a moderate absorption coefficient, ranging from 10^2 to 10^3 cm^{-1} at near-infrared wavelengths [44]. As a result, a typical thickness of the intrinsic absorber layer of µc-Si:H solar cells in the range of 10 µm would be needed in order to guarantee a sufficient photon absorption. However, due to the successful application of light trapping technologies, this thickness can be significantly reduced (typical µc-Si:H absorber thickness: about 2 - 3 µm). However, the µc-Si:H absorber layer thickness is still nearly ten times larger than the typical absorber layer thickness used in a-Si:H solar cells. Thus, if aiming at tandem applications, it is necessary to develop high-rate µc-Si:H deposition techniques in order to improve the throughput of the fabrication process. Generally, a very-high-frequency (VHF) PECVD process at about 40 - 60 MHz is used in industry. Even higher frequencies (above 100 MHz) are sometimes used in the lab to achieve high-rate µc-Si:H deposition [45]. Recently, a high-pressure depletion method has been proposed to fabricate high-quality µc-Si:H films combined with VHF technology, to produce high-efficiency solar cells [46, 47]. As an alternative to PECVD, hot-wire chemical vapour deposition (HWCVD) has also been successfully applied to process µc-Si:H films and solar cells [48-50].

2.2 PECVD technique and μc-Si:H thin-film deposition

2.2.1 PECVD technique

In general, thin film deposition can be either realized via physical vapour deposition (PVD), such as evaporation or sputtering, or via chemical vapour deposition (CVD), that is using chemical reactions of gases. In the early days, amorphous silicon was obtained by evaporation or sputtering of silicon. However, such kind of amorphous silicon films have a high defect density caused by poorly coordinated silicon atoms (i.e. "broken" silicon-silicon bonds which are not passivated by hydrogen, called 'dangling bonds'). This material was unsuited for semiconductor device fabrication. At the end of the 1960s, people realized that those dangling bonds can get passivated by hydrogen atoms, originating, for example, from the plasma excitation of silane (SiH_4) and hydrogen (H_2) gases. The resulting material was termed 'hydrogenated amorphous silicon', a-Si:H. It was reported that a-Si:H films had good photoconductivity [51], indicating a low defect density in the film so that photogenerated excess electrons/holes can be transported through the film, rather than being trapped by the defects. This opened opportunities for a-Si:H to be applied to electronic devices, such as silicon thin-film solar cells. The first a-Si:H solar cells were reported in 1976 [52]. In 1979 followed the first report (by Usui *et al.*) about the fabrication of μc-Si:H films by PECVD [53]. Concerning the current PECVD technology development, PECVD a-Si:H as well as PECVD μc-Si:H are widely used for mass production within the photovoltaic industry.

The typical PECVD process is conducted in a parallel-plate configuration. A plasma reactor is used, that usually consists of a vacuum chamber, a pair of parallel electrodes, a power supply system, a gas supply system, a pumping system and an

exhaust handling system. Appendix A describes some details of the PECVD system (MVSystems, Inc., USA) used in this thesis.

PECVD is a complicated process, which involves a series of interactions between plasma, gas reactions, products of the gas reactions, surrounding surfaces and the substrate for deposition. In general, the PECVD process includes four major steps:

1. Electron impact dissociation of the feeding gases;
2. Chemical reactions between the gases;
3. Transport and deposition of the radicals towards the substrate surface (surface reaction);
4. Stable growth of the film.

When a sufficiently high RF power is applied to the parallel electrodes in the vacuum chamber which is filled with the corresponding reaction gases at low pressure (i.e. SiH_4 and H_2 in case of processing intrinsic thin-film silicon and additional phosphine (PH_3), or diborane (B_2H_4), if processing doped layers), it triggers the generation of a low pressure plasma, named as "glow discharge". The plasma is ignited by the generation of electrons and ions by ionization of the gas atoms and molecules, in a similar way as in a fluorescent light bulb. Glow is the emitted light which results from the de-excitation of the excited molecular and atomic species. Next, a series of secondary electrons emit from the electrodes and they contribute to the ionisation of the feeding gases. As a result, the glow discharge is sustained between the two electrodes by the inelastic electron impact processes.

The plasma contains electrons, positive and negative ions, neutral atoms, molecules, and free radicals. As shown in Figure 2.2 [54], because the electrons have much higher thermal velocity than ions, they can reach the electrodes faster and make the electrodes slightly negative compared to the plasma bulk. In order to guarantee the total charge neutrality and zero net current, an electric field is built up near the

electrodes to retard the electrons and accelerate the ions. This electric field exists in front of the electrodes with a small distance (in the order of millimetres). This region is mainly filled with ions and, thus, is positively charged. As illustrated in Figure 2.2, it is termed as "sheath" in the vicinity of the two electrodes. The field-free plasma volume between the two sheaths is called the plasma bulk. The power spent in the plasma bulk is used for the decomposition of the feeding gases, but the power spent in the sheaths is generally taken as a loss. However, the electric fields in the sheath directly impact the transport of the radicals near the substrate surface and are therefore mainly responsible for the ion bombardment, which is a critical factor for the thin-film properties [55]. In Chapter 6.3, we will investigate μc-Si:H thin-film growth as a function of different surface morphologies, and discuss about the impact of ion flux on the resulting thin-film growth. At a higher plasma excitation frequency, the sheaths become thinner (i.e., less power loss), resulting also in a lower energy for the ion bombardment. Thus, lower defect densities within the thin film can be obtained in this case.

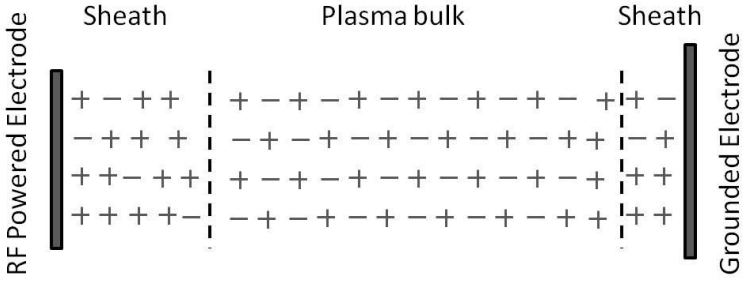


Figure 2.2: Schematic of the plasma between the two parallel electrodes [54].

As discussed above, PECVD is a complex process. In order to deposit high-quality silicon thin films for device fabrication, various deposition parameters must be taken into consideration, such as discharge power, excitation frequency, substrate temperature, gas pressure, gas flow rate, and electrode geometry (electrode pattern and

spacing). The general influence of these parameters on the thin-film properties, and on the resulting solar cell performance, will be briefly discussed in the following.

2.2.2 µc-Si:H thin-film deposition and growth mechanisms

The growth mechanism of PECVD µc-Si:H thin films has been studied extensively, and several growth models have been proposed to describe the growth behaviour, such as the surface diffusion model [56], the etching model [57] and the chemical annealing model [58], which shall be briefly described in the following.

When the plasma is triggered, a large amount of precursors (SiH_3) are generated from the decomposition of the silane (SiH_4) gas. The precursors randomly distribute among the plasma species until they reach the surface of the film. Because the film surface is full of dangling bonds, some of the precursors are caught immediately and connected to the silicon network. However, a large amount of the precursors can move freely and will diffuse along the surface of the film to look for energetically stable places. However, because of the high density of surface dangling bonds, the diffusion length of the precursors is limited (it is reported to be less than 10 nm at 250 ˚C [59]).

Surface diffusion model

According to the "surface diffusion model" proposed by Matsuda (1983) [56], a sufficient surface coverage by hydrogen atoms enhances the precursor diffusion length and thus helps the formation of the crystalline phase. There exists a very high density of hydrogen atoms in the plasma due to the fact that a high hydrogen gas flow is used during the µc-Si:H deposition. The large number of hydrogen atoms provides

a good passivation of the surface dangling bonds, and at the same time the released energy (local heating) makes the precursors more active. Therefore, the diffusion length of the precursors increases, benefitting the growth of the crystalline phase, which is more stable energetically. This process is illustrated in Figure 2.3.

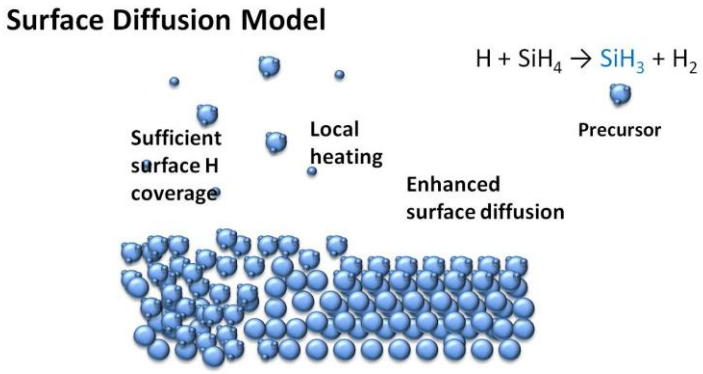


Figure 2.3: Schematic of the "surface diffusion model" for the growth mechanism of µc-Si:H films.

Etching model

Tsai *et al.* (1989) proposed an "etching model" to explain the role of plasma surface etching in the formation of the µc-Si:H film [57]. During the deposition, the hydrogen atoms tend to etch the surface of the film. The amorphous phase, due to its disordered structure, has weak silicon bonds and is prone to be etched away. But, on the other hand, the crystalline phase - having stronger bonds - is left and keeps growing. Therefore, the "etching" and "growth" are the two factors in competition with each other to determine the film deposition. This process is illustrated in Figure 2.4. This "etching effect" during µc-Si:H film deposition will be frequently used to discuss the observed phenomena, for example the dependence of µc-Si:H thin-film growth on the substrate morphology, as discussed in Chapter 6 of this thesis.

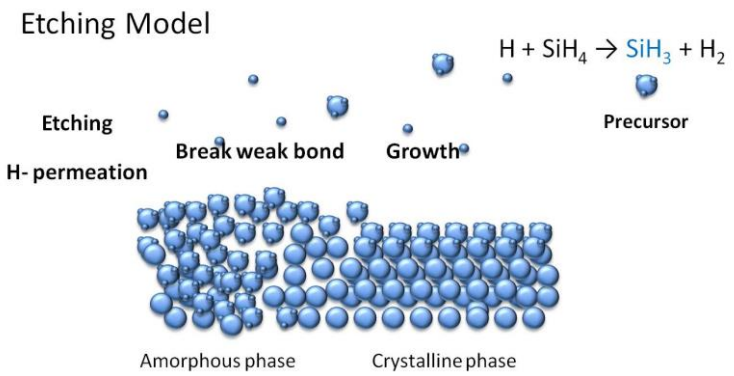


Figure 2.4: Schematic of the "etching model" for the growth mechanism of µc-Si:H films.

Chemical annealing model

In 1995, Nakamura *et al.* proposed a "chemical annealing model" to explain the relation between the plasma action and silicon structure variation [58], see Figure 2.5. With certain ion energy, the hydrogen atoms can permeate into the sub-surface of the film and cause structural relaxation. In this case, the silicon lattice has a chance to re-arrange the amorphous network into an ordered network. Later, Fujiwara (2002) experimentally showed that a high intrinsic stress (> 750 MPa) due to the hydrogen permeation into the a-Si:H network is essential for the nucleation formation of µc-Si:H [60]. They highlighted the importance of the stress-induced µc-Si:H nucleation and pointed out it is the requisite to cause crystallization of the amorphous network through the formation of a flexible network.

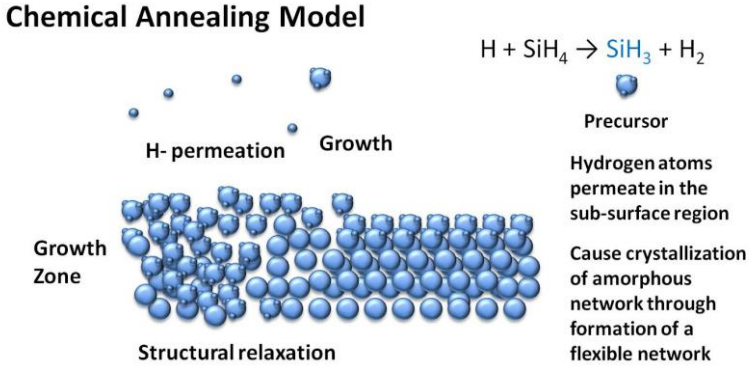


Figure 2.5: Schematic of the "chemical annealing model" for the growth mechanism of µc-Si:H films.

The above growth models describe the silicon thin-film growth behaviour under the effect of the plasma. Based on the special characteristics of the growth behaviour of µc-Si:H, a high input power and high hydrogen gas flow are required to facilitate the formation of µc-Si:H thin films. In Chapter 3, a "layer-by-layer" deposition method will be established and used to fabricate very thin (20 - 30 nm) doped µc-Si:H layers with different crystallinity. The physical principles used for this deposition method stem from these three growth models. Besides, these three models will also be applied to explain the observed phenomena in Chapter 6 when µc-Si:H layers are processed onto superstrates with different surface morphologies.

2.3 µc-Si:H thin-film solar cells

Although the study of the fabrication and properties of µc-Si:H films started in the early 1970s, the first applications of µc-Si:H as absorber layer in solar cells were only reported in the early 1990s by Wang (1990) [61] and Fluckiger (1992) [62]. Later, a breakthrough in the application of µc-Si:H on single-junction solar cells was reported by a group from IMT in Neuchatel in 1994, i.e. an efficiency of 4.6% and high short-circuit current density of up to 21.9 mA/cm^2 were achieved [63]. At the same time, it was discovered that µc-Si:H solar cells hardly suffer from light-induced degradation, which is an enormous advantage over the amorphous counterparts (i.e. a-Si:H and a-SiGe:H solar cells). From then on, µc-Si:H solar cells attracted high attention and intensive research was conducted over the following 20 years. Various aspects were investigated, such as an improvement of the deposition process [64-68], an in-depth study of the thin-film material properties [44, 69-73], an application of µc-Si:H layers in multi-junction device architectures [74, 75], an implementation of light trapping technologies [15, 76-78], and an optimization of the PV device performance [20, 22,

79-81]. As of today, the best single-junction µc-Si:H solar cell efficiency is reported to be up to 10.7 % [82-84].

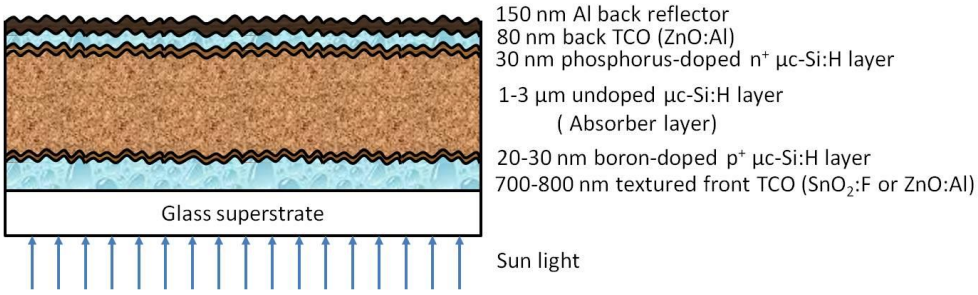


Figure 2.6: Schematic of the conventional structure of a µc-Si:H thin-film solar cell in a p-i-n superstrate configuration.

Generally, µc-Si:H thin-film solar cells consist of two transparent conductive oxide layers (TCO) serving as contact layers, one boron-doped µc-Si:H layer (*p*-layer or window layer) serving as a hole collector, one un-doped intrinsic µc-Si:H layer (*i*-layer) serving as absorber layer, one phosphorus-doped µc-Si:H layer (*n*-layer) serving as an electron collector and of a rear-side silver or aluminium layer, serving as a back reflector and as an additional contact layer. The typical device architecture of a µc-Si:H thin-film solar cell in a p-i-n configuration (that is using a superstrate, i.e. the light is entering the solar cell through the glass) is illustrated in Figure 2.6.

There are some special requirements for each layer. For example, the front TCO layer mainly serves as an electrode providing good contact with the hole collecting window layer (*p*-layer). Therefore, the basic requirements for the properties of the front TCO layer are sufficiently high electrical conductivity (1×10^3 - 1×10^4 S/cm) and optical transparency (transmission > 85%) in the visible spectral range as well as in the near-infrared. At present, several semiconductor materials, such as SnO_2:F, In_2O_3:Sn (ITO), and doped ZnO (ZnO:Al or ZnO:B), are used as TCO for thin-film solar cell fabrication. Quite often, a thin rear-side TCO is used for the purpose of providing a better contact to the electron collecting µc-Si:H layer (n-layer), as a direct µc-Si:H/Al contact exhibits an unfavourable Schottky barrier. Furthermore, this thin

TCO layer serves as a diffusion barrier to prevent metal diffusion into the Si layers, which may cause local shunting of the device. Concerning the doped μc-Si:H layers, a high doping efficiency (a low activation energy) is required to form a high built-in potential within the solar cells (needed for efficient charge carrier collection within the intrinsic absorber layer) and to ensure a high conductivity in order to reduce the series resistance of the solar cell. More details concerning the development of a p-type window layer will be discussed in Chapter 3.

According to the deposition sequence for each layer, silicon thin-film solar cells can be categorized into a p-i-n superstrate and into a n-i-p substrate configuration (with the incident sunlight entering via the glass superstrate or via the deposited thin-film layers, respectively). Regardless of the configuration, the incident light always enters the solar cell via the *p*-layer. This is because holes have a much shorter diffusion length (or drift length or carrier lifetime) than electrons in thin-film silicon layers. When the light enters the Si absorber layer, a large amount of electron-hole pairs are generated at the region near the *p*-layer and the holes only need to pass a short distance to reach the hole-collecting p-layer, while the electrons have to travel a longer distance to reach the other terminal (the electron-collecting n-layer). Thus, the excess carrier recombination within the intrinsic absorber layer is lower compared to the case where most of the holes have to travel a longer distance. In general, the p-i-n configuration (as used within this thesis) is preferably applied to transparent superstrates, such as glass, whereas the n-i-p configuration is applied to opaque substrates, such as stainless steel or polymer foils. The words “superstrate” and “substrate” are merely used to distinguish the different thin-film configurations, i.e. incident light always penetrates a superstrate first, while it always reaches a substrate at the very last. In this thesis, all the experiments use the p-i-n superstrate configuration.

In general, all *doped* thin-film silicon films, i.e. doped a-Si:H and doped µc-Si:H, are very defective and cannot be used as an absorber layer for thin-film solar cells. Hence, un-doped (so called intrinsic) films have to be used. This is the reason why thin-film silicon solar cells (i.e. a-Si:H and µc-Si:H solar cells) have a p-i-n structure rather than a p-n structure, which is conventionally used for wafer based crystalline silicon solar cells.

Until today, the highest single-junction µc-Si:H thin-film solar cell efficiency (around 10.7 %) is still much lower as compared to other thin-film technologies, i.e. CIGS and CdTe, which now reach single-junction cell efficiencies of above 20 %, as discussed in Chapter 1. To further improve the silicon thin-film solar cell efficiency, there are two main problems which have to be addressed.

First, the short-circuit current should be further enhanced by using some novel light trapping technologies. Currently, the highest reported current densities of thin-film silicon solar cells are about 30 mA/cm^2 [85, 86], however so far using non-industrial light trapping schemes. According to theoretical calculations, in principle, the photogenerated current of thin-film silicon solar cells should be able to reach values as high as 36 mA/cm^2 [14]. Thus, further current enhancement seems possible. An advanced and industrially viable light trapping scheme suitable for thin-film µc-Si:H solar cells will be described in Chapter 6 of this thesis, investigating the use of an industrially viable double-textured glass superstrate (consisting of micro-structured AIT glass covered with nanotextured TCO) for µc-Si:H solar cell applications.

Second, the defect density in the intrinsic µc-Si:H absorber layer (*i*-layer) is still too high, i.e. in the range of 10^{15} - 10^{16} cm^{-3} [87], especially as compared to c-Si which has a defect density as low as 10^{10} cm^{-3}. The high defect density of µc-Si:H limits the I-V performance of the solar cell (i.e. resulting in a relatively low open-

circuit voltage). Hot wire chemical vapour deposition, HWCVD, is a recently developed ion damage free deposition method (compared to the standard parallel-plate PECVD process, which always results in some ion damage), which shows a potential to improve the electronic quality for the intrinsic µc-Si:H absorber layer [64, 65]. Apart from this, it has been shown that a buffer layer which is processed with low defect density (i.e. using HWCVD) and being introduced at the p/i interface of the µc-Si:H solar cell, is also able to improve the solar cell efficiency (while all other layers were still processed by PECVD) [88]. This indicates that the µc-Si:H solar cell efficiency can be improved by inserting a proper buffer layer at the p/i interface of the solar cell. This topic will be addressed in Chapters 4 and 5 of this thesis. In Chapter 4, 4 different buffer layers with varying defect density and different conductivity are investigated experimentally: (1) an a-Si:H buffer layer, (2) an a-Si:H buffer layer with isolated µc-Si:H grains, (3) an a-Si:H buffer layer with percolating µc-Si:H grains and (4) a highly crystallized µc-Si:H buffer layer. In Chapter 5, these structures are analysed by means of numerical computer simulation.

2.4 Review of improving the electrical performance of a µc-Si:H solar cell by introducing a buffer layer at the p/i interface

In this section, a brief review of previous works reported by other groups and a summary of the state of the art is given in respect to improving the electrical performance of a µc-Si:H solar cell by introducing a buffer layer at the p/i interface. In addition, the main limitations and shortages of the current research work are pointed out. Further investigations of this topic are carried out in Chapter 4 of this thesis (by means of experiments) and in Chapter 5 (by means of numerical computer simulation).

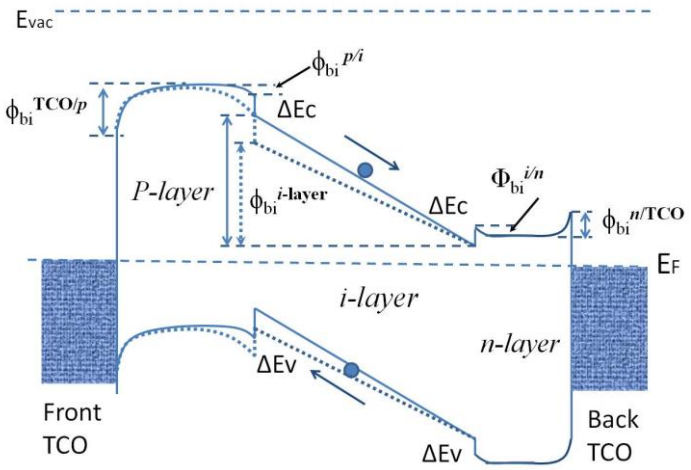


Figure 2.7: Band diagram of a typical p-i-n silicon thin-film solar cell structure (not to scale). Two band bending situations are sketched by solid lines and dotted lines. The built-in potential (ϕ_{bi}) across several layers and interfaces is also illustrated.

An optimized p/i interface is essential for achieving high-efficiency µc-Si:H thin-film solar cells [16]. A proper design of the p/i interface or the insertion of a buffer layer at the p/i interface can improve the solar cell efficiency [22]. Several works have been carried out, and in the following they shall be categorized into three major areas, corresponding to the main physical impact of the p/i interface (or of the buffer layer) as illustrated in Figure 2.7. The p/i interface (or the buffer layer) can impact: (1) the band offset (ΔE_c and ΔE_v) or the corresponding potential barrier between the neighbouring materials/layers and thus influencing the carrier transport across that interface [27, 89, 90]; (2) the band alignment or the corresponding built-in potential (ϕ_{bi}) within the solar cell, and thus influencing the excess carrier collection efficiency of the solar cell [17, 89-93]; (3) the interface defect states and thus influencing the recombination rate at the interface region and therefore the open-circuit voltage of the solar cell [17, 18, 28-30, 94, 95]. Figure 2.7 also illustrates the built-in potential (ϕ_{bi}) between the neighbouring layers and the total built-in potential (ϕ_{bi}^{total}) of the solar cell, which is defined in Eqn. 2.1. The introduction of a buffer layer at the p/i interface can also impact the $\phi_{bi}^{p/i}$ and $\phi_{bi}^{i\text{-}layer}$, and thus the change of the ϕ_{bi}^{total} which leads to the variation of the band bending within the solar cell.

$$\phi_{bi}^{total} = \phi_{bi}^{TCO/p} + \phi_{bi}^{p/i} + \phi_{bi}^{i\text{-}layer} + \phi_{bi}^{i/n} + \phi_{bi}^{n/TCO}; \quad (2.1)$$

Therefore, the p/i interface (or a buffer layer introduced at the p/i interface) is a critical factor to determine the PV efficiency and stability of µc-Si:H solar cells.

History of p/i interface optimization and the use of a buffer layer in µc-Si:H thin-film solar cells

In their studies, Nasuno et al. (2002) and Matsui et al. (2003) pointed out that a significant contamination of the p/i interface and the region adjacent to it stems from an impurity diffusion from the bottom layers, leading to a significant drop in open-circuit voltage (V_{oc}) as well as in short-circuit current (J_{sc}) [18, 96]. A poor blue response is also observed in the corresponding quantum efficiency curve. Later, Taira et al. (2003) proposed that a 20 nm thick a-Si:H buffer layer inserted at the p/i interface can effectively control the impurity profiles and suppress the impurity diffusion, which resulted in an improved PV efficiency [97]. Since then, more research works on the interface study for µc-Si:H cells were carried out. Donker et al. (2007) reported a V_{oc} of above 600 mV, obtained by using a 15 nm thick HWCVD buffer layer after the *p*-layer deposition [19, 88]. They attributed the high V_{oc} to the fact that HWCVD is an ion bombardment free deposition method and thus the ion damage to the p/i interface is avoided. However, the authors did not reveal the structural material composition of this buffer layer.

Soderstrom et al. (2008) used a buffer layer with low crystallinity at the n/i interface (using a n-i-p substrate configuration) to limit the formation of voids and porous areas. They showed that solar cells using such a buffer layer were able to keep good performance (i.e. no local shunting) if the cells were fabricated on rough substrates [98]. Meanwhile, Yue (2008) and Yan (2010) also showed that an a-Si:H buffer layer used at the p/i interface can effectively reduce the shunt current and therefore

improve the V_{oc} [22, 99]. However, the authors did not state the deposition conditions for this buffer layer and there is no strong proof that the buffer layer used is really pure a-Si:H. Furthermore, the method used to estimate the thickness of the buffer layer was not stated in this paper. More recently, Bugnon (2014) used an ~6 nm thick SiO_x buffer layer at the p/i interface and showed that it can improve the blue response of the solar cell (thereby also increasing the I_{sc}), but also the V_{oc} due to an "electrical quenching effect" as well as the fill factor (*FF*) because SiO_x facilitates the nucleation of the µc-Si:H films [23]. A high PV efficiency (10.9%) was reported and SiO_x was proposed to be a promising material as buffer layer to be applied in µc-Si:H thin-film solar cells. It is important to know which type of buffer layer is the best to improve a given µc-Si:H solar cell process (not using a buffer layer). However, little work has been carried out comparing different buffer layers with respect to the resulting solar cell performance. This will be done in Chapters 4 and 5 of this thesis.

Characterization methods used for buffer layers

Although a series of studies were done on the application of a specific buffer layer at the p/i interface to study its influence on the solar cell I-V performance, the work on the corresponding buffer layer characterization is quite limited. In general, Raman spectroscopy was used to determine the structural composition (crystallinity) of the buffer layer [23]. However, because the buffer layer is typically very thin (several nm to several tens of nm) and inserted between the p-layer and i-layer, the collected Raman signal also contains information from the p-layer and the i-layer. In this case, the Raman signal that stems from the buffer layer itself only contributes a small part to the observed total Raman signal. Therefore, a Raman measurement typically cannot accurately reflect the real crystallinity of such a buffer layer. In order to overcome this issue, in this thesis cross-sectional transmission electron microscopy (XTEM) is used for the characterization of the various buffer layers, in order to reveal the real situation near the p/i interface.

2.5 Review of improving the optical performance of a µc-Si:H thin-film solar cells by varying the superstrate surface morphology

To reduce manufacturing cost and excess carrier recombination, the µc-Si:H absorber layer should be as thin as possible. However, due to the material's finite absorption coefficient, it is difficult to generate a sufficiently high photogeneration rate within the µc-Si:H film for a single pass of the light through the film. Therefore, light scattering technologies have to be used to enhance the effective light path within the thin-film absorber [15, 76, 77]. With the help of light trapping methods, photo-generated currents of above 30 mA/cm^2 can be generated in 3 µm thick µc-Si:H films [85, 86].

The conventional thin-film light trapping is achieved by either etching the front transparent conductive oxide (TCO) layer of the solar cell prior to the µc-Si:H deposition, or by growing the TCO layer with a self-organized surface texture [100]. This usually creates a nanotextured TCO surface, with typical feature sizes ranging from several tens of nanometres to several hundred nanometres [14, 15, 100]. This surface texture generally provides good light trapping properties for wavelengths up to 650 nm, but the ability to scatter near-infrared light from 700 to 1100 nm is quite modest. To overcome this problem, surface textures with a larger feature size are needed [36].

Photolithography has been used to create periodic honeycomb patterns with micro-scale size, and a significant improvement of near-infrared light absorption was shown for substrate-type n-i-p µc-Si:H thin-film solar cells [86, 101]. For superstrate-type p-i-n µc-Si:H thin-film solar cells, a texturing of the glass superstrate (leading to a microtextured glass surface) has been proposed recently, i.e. using imprint-textured glass [36], or using rough glass obtained by 3d texture transfer (ion etching) [37]. We propose to use aluminium-induced texture (AIT) glass [25, 26, 38] instead, which has

been developed in recent years and which is believed to be compatible with the large-area, high-throughput and low-cost requirements for industrial PV production.

It has already been theoretically proven, using numerical computer simulation, that a multitextured superstrate (i.e. using a microtextured glass surface together with a nanotextured TCO surface) has an excellent light scattering potential for the entire wavelength range from 300 to 1100 nm, because of the superimposed scattering behaviour [102]. Experimentally, a double-textured superstrate has already been investigated, i.e. using ion-etched textured glass in combination with a self-organized textured (MOCVD made) TCO, proving a short-circuit current enhancement ΔI_{sc} of 1.5 mA/cm^2 compared to the planar glass/textured TCO reference superstrate [24].

In this thesis, we use a different double-textured superstrate, which we consider to be more industrially viable, i.e. an aluminium-induced texture (AIT) glass (micro-texture) covered with an acid-etched TCO (nanotexture), and compare its light trapping ability to a standard single-textured reference superstrate (i.e. planar glass covered with texture-etched TCO). As already published, this double-textured AIT superstrate displays excellent light scattering abilities (studying the thin-film scattering into air) for the entire wavelength range from 300 nm to 1200 nm [38]. In this thesis, we process µc-Si:H thin-film solar cells on such AIT superstrates and investigate their scattering ability into silicon by measuring the short-circuit current enhancement as compared to a single-textured reference superstrate (see Chapter 6).

2.6 Aluminium-induced texture (AIT) process to obtain microtextured glass superstrates

The textured glass used in this thesis is realised with the so called “aluminium-induced texture” (AIT) method [25, 26, 38]. The AIT method enables us to obtain an

industrially feasible microtextured glass surface with typical feature sizes in the range of 1 - 3 µm. It is realized via a thermally activated chemical reaction at approximately 600 °C between the glass and a thin, sacrificial aluminium layer:

$$4\ Al + 3\ SiO_2 \rightarrow 2\ Al_2O_3 + 3\ Si; \qquad \textbf{(2. 2)}$$

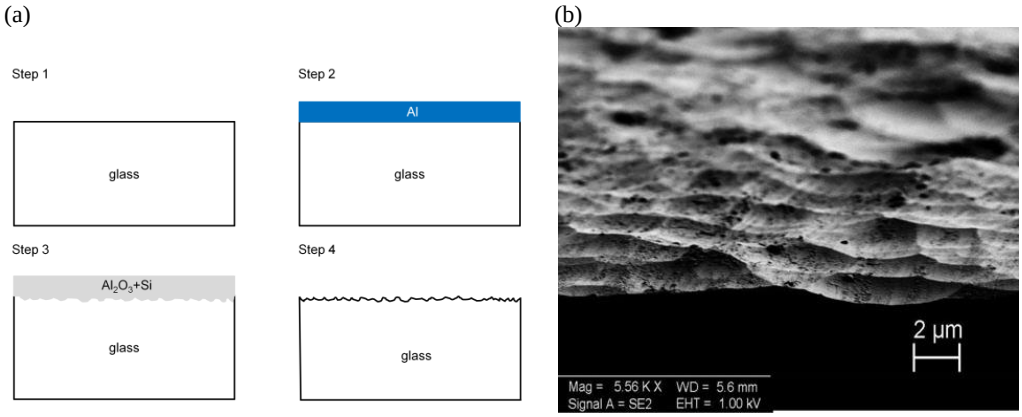


Figure 2.8: (a) Schematic of the AIT process [103], by courtesy of Y. Huang, SERIS. (b) SEM image of bare AIT glass surface [38], by courtesy of S. Venkataraj, SERIS.

Figure 2.8(a) shows the typical process of making an AIT glass sheet. The bare, planar glass coated with a thin Al layer by evaporation or sputtering is sent to an oven for a thermal annealing process at approximately 600°C. The redox reaction between the Al and glass (SiO_2) etches the glass surface. After removing the reaction products by wet-chemical etching, the glass surface will show random dimple-like surface features, as shown in the SEM micrograph of Figure 2.8(b). By changing the Al thickness, the reaction time and the etching time, the surface morphology of the AIT glass (i.e. mean feature size as well as root mean square roughness) can be varied controllably. More details on the AIT process can be found in Refs. [26, 38, 103].

Chapter 3: Development of high-quality boron-doped µc-Si:H p^+ window layer on different superstrates[1]

3.1 Requirements of µc-Si:H *p*-layers to be used as window layer

Boron-doped µc-Si:H *p*-layers play an important role as a hole collecting layer for thin-film silicon solar cells and must meet several requirements, as follows:

① Window layer:

As discussed in Chapter 2.3, in most of the cases light should enter the silicon thin-film solar cell through the *p*-layer. This is also the reason why the layer is called "window layer". Basically, the doped hole collecting layer of a thin-film silicon solar cell is an electronically "dead layer", i.e. the photogenerated minority carriers (i.e. the electrons in the p-layer) can't be collected due to the very high recombination rate and short lifetime in this heavily doped layer (more details see Chapter 5). The light absorbed in this layer is taken as an optical loss. Therefore, the layer should be as thin as possible. Furthermore, the window layer should have a low absorption, i.e. be optically "transparent". In general, µc-Si:H (especially for highly crystallized films) has a much lower absorption coefficient than a-Si:H in the 300 - 700 nm range [104]. As a result, it is more suitable to be used as window layer. Recently, to further reduce its light absorption, it was proposed to use microcrystalline silicon alloys, such as µc-SiC:H [105-107] or µc-SiO_x:H [108-111]. These alloys have a large bandgap (close to 2 eV) and good conductivity (due to the existence of the crystalline phase in the film), which are considered as new promising materials for window layers.

[1] The content of this chapter has been published in Energy Procedia **25**, 2012, pp. 34-42.

② Hole collector:

The hole and electron collecting *p*- and *n*-layers of a thin-film silicon solar cell create a depletion region over the entire *i*-layer (the solar cell absorber) and build up an internal electrical field across the absorber layer (see Figure 2.7 or Figure 5.4, where a typical band bending situation of a thin-film solar cell is sketched). This is to extract the photogenerated e-h pairs (the *p*-layer collects holes and the *n*-layer collects electrons). Therefore, a *p*-layer requires a low activation energy, which is defined as the distance from the Fermi level to the valence band edge for a *p*-layer, indicating a high doping efficiency, in order to build up a large built-in potential (V_{bi}) for the solar cell and thus improve the carrier collection efficiency.

③ Contact layer:

In general, there is a Schottky barrier between a metal and un-doped silicon. The same situation applies for the contact between TCO (ZnO:Al or SnO_2:F) and a µc-Si:H *i*-layer (contacting by a TCO instead of a metal). As a result, it needs a heavily doped layer to reduce this Schottky barrier and form an ohmic contact. Otherwise, there will be a potential drop, leading to a high series resistance stemming from a hindered carrier transport over this barrier, which would diminish the *FF*. The doped layer should therefore have a good doping efficiency and a high conductivity.

④ Seeding layer:

The µc-Si:H *i*-layer is deposited onto the µc-Si:H *p*-layer (in the p-i-n superstrate configuration). As a result, the *p*-layer should have high enough crystallinity (i.e., contain a certain amount of crystalline phase) in order to serve as a seeding layer, facilitating the *i*-layer growth (thereby avoiding the formation of an amorphous incubation layer) [112].

In this chapter, based on the above requirements and using a "layer-by-layer" method, experiments are conducted to develop high-quality boron-doped μc-Si:H *p*-layers on different superstrates. First, a baseline (i.e. not using the "layer-by-layer" method) was built up for intrinsic and doped μc-Si:H thin-film layer processing, as stated in Appendix B. These baseline process parameters serve as a reference to establish the "layer-by-layer" method discussed in this chapter. In principle, a similar optimization process can also be applied to the phosphorus-doped μc-Si:H *n*-layer (however this was not investigated in this thesis, as the p-layer optimization is much more critical for thin-film silicon solar cell optimization).

3.2 Development of improved p-typed μc-Si:H window layers on different superstrates using the "layer-by-layer" growth method

Because boron atoms tend to remove hydrogen atoms from the surface of the silicon film, it is prone to prevent the nucleation and the crystalline phase growth [113]. As a result, it is difficult to fabricate a very thin *p*-type μc-Si:H film (below 30 nm) with high crystallinity (> 60%) and conductivity (> 1 S/cm). One effective solution which has been reported and used by many groups is using very-high-frequency plasma excitation (VHF) [114, 115]. But, on the other hand, VHF may lead to serious deposition uniformity problems when used for the fabrication of large-area samples. Another solution to improve the properties of very thin films is to reduce the thickness of the incubation layer, so that the nucleation starts at the early stage of the film growth and the crystalline phase can dominate in the later growth process. Generally, the thickness of the incubation layer is about 10 to 15 nm in the standard deposition process. This means that there is not much room for the crystalline phase growth in the very thin film. Recently, Cabarrocas *et al*. showed that the incubation layer can be reduced to below 5 nm thickness by using the layer-by-layer (LBL)

method [116, 117]. Consequently, the µc-Si:H p-layer with only 20 nm thickness can still reach high crystallinity and conductivity because of hydrogen diffusion and etching effects leading to the reduction of the incubation layer thickness. In this chapter, the LBL method is used for the deposition of very thin (< 30 nm) p-layers onto various superstrates, i.e. (1) planar glass, (2) planar glass coated with a ZnO:Al thin film, and (3) textured glass, using the "aluminium-induced texture" method, as already described in the previous chapters of this thesis, i.e. AIT glass with micro-textured rough surface. The effects of hydrogen plasma treatment steps on the films' structural properties (crystallinity) and electrical properties (dark conductivity) are investigated and the best results achieved on the various types of superstrates are presented.

3.2.1 Experimental details for "layer-by-layer" deposition method

All films were deposited onto A3 size (30 × 40 cm^2) soda-lime glass sheets. The used deposition conditions for the baseline reference layers (see Appendix B for the baseline process) are listed in Table 3.1.

Table 3.1 Deposition conditions for all the experiments in this study

Deposition parameter	Value
Substrate temperature (°C)	200
Pressure (Torr)	1.2
Input power (W)	60
Gas flow rate (sccm)	SiH_4 : 4; H_2: 196; B_2H_6: 1.6

The layer-by-layer (LBL) method is a technology where µc-Si:H deposition and hydrogen plasma treatment are conducted alternately during the deposition process. A schematic of the LBL method is shown in Figure 3.1. The number of cycles (i.e., a H_2

plasma treatment followed by the deposition of a thin µc-Si:H layer) or the length of the plasma treatment process were varied in our experiments. The thickness of all films fabricated in this work was in the range of 25 - 30 nm. Before µc-Si:H deposition, a very thin boron-doped amorphous Si layer (about 3 - 4 nm) was deposited onto each superstrate as the first step. There were two reasons for this. First, in this way the µc-Si:H depositions in all the experiments had the same initial interface, whereby this is an interface between a-Si:H and µc-Si:H (i.e., a Si-Si interface) rather than an interface between glass (mainly SiO_2) and Si or a TCO (such as ZnO:Al) and Si. Thus, influences from the initial growth interface are ruled out here. Secondly, the thin a-Si:H layer can directly serve as an incubation layer for nucleation and crystalline phase growth, which can accelerate the µc-Si:H layer's growth process [118].

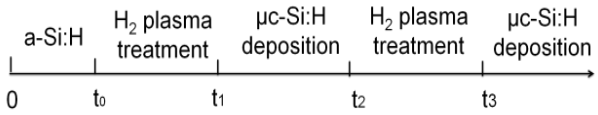


Figure 3.1: Schematic of the LBL method used in this work for µc-Si:H thin-film deposition. The H_2 plasma treatment and the µc-Si:H deposition are alternately conducted during the entire process.

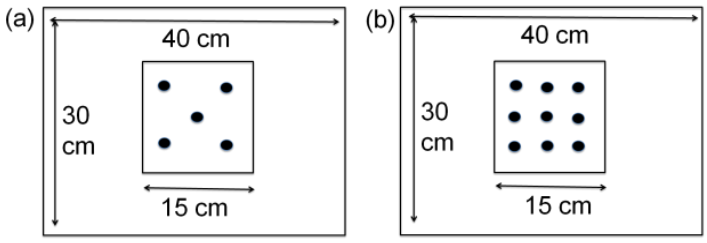


Figure 3.2: The crystallinity measurement positions (a) and conductivity measurement positions (b) on A3 size soda-lime glass for each sample.

The crystallinity of the films was measured by Raman spectroscopy, using a laser producing 514 nm light, and more details are stated in Appendix E. The conductivity σ (S/cm) was calculated via:

$$\sigma = 1/ (R\square \times t); \qquad (3.\ 1)$$

$R_{\square}$ is the sheet resistance measured with a four-point probe instrument and t is the film thickness measured with a Stylus profilometer. The crystallinity and conductivity measurements were conducted at five and nine locations, respectively, near the centre of the A3 size glass sheet, as shown in Figure 3.2.

3.2.2 Influence of hydrogen plasma treatment on Si film properties

In order to fabricate a very thin µc-Si:H film with high crystallinity, it is necessary to reduce the incubation layer's thickness and to make the nucleation start as early as possible. As reported in the literature, a good atomic hydrogen coverage of the film surface benefits the nucleation process [56]. The hydrogen atoms can permeate into the sub-surface region of the film, and this permeation process leads to a structural relaxation followed by a structural reconstruction and next, the generation of stress to form more rigid Si networks where the nucleation starts from [119]. Because of the formation of these flexible networks and the structural re-arrangement, they cause localized crystallization of the amorphous network [58, 119]. At the same time, during the deposition, the hydrogen plasma would tend to etch the surface of the film. Because of this etching effect, amorphous networks with weak Si-Si bonds will be etched away. As a result, the amorphous phase becomes less and the crystalline phase with strong enough bonding will be left and keeps growing [57]. Thus, when the film is exposed to the hydrogen plasma, it is good for the crystalline phase growth and finally gets a high crystallinity for the µc-Si:H film. Based on this principle, a series of hydrogen plasma treatment experiments was conducted.

For standard depositions without any special action, such as hydrogen or CO_2 plasma treatment, it is difficult to make thin µc-Si:H films with high crystallinity and conductivity on an amorphous layer [117]. In most of these cases, the Si film shows no microcrystalline sign because of the "epitaxy-like growth" of the amorphous

network even if the film is deposited using the microcrystalline growth regime [56, 57, 118]. The conductivity of such films is in the range of 10^{-5} - 10^{-4} S/cm measured by the co-planar configuration [120], which is close to that of the a-Si:H boron-doped layer. In the present study, a very low silane concentration ($S_c = [SiH_4] / [SiH_4 + H_2 + B_2H_6]$) of about 2 % was used for the common deposition of µc-Si:H thin film on amorphous Si layer. As can be seen from Figure 3.3, the crystallinity values of the thin films without hydrogen plasma treatment are below 10 % or even approach 0 %, which means that the Raman signal merely shows the 480 cm^{-1} peak (corresponding to a-Si:H). The best conductivity achieved for those thin films is about 3.5×10^{-2} S/cm.

As can be seen in Figure 3.3, the hydrogen plasma treatment significantly improves the conditions for the growth of the crystalline phase. For a fixed duration (60 s) of each hydrogen plasma treatment step, an increasing number of cycles improves both the crystallinity and the conductivity of the Si film. For 15 cycles and above, the films have crystallinity values of more than 60 % and an excellent conductivity of above 1 S/cm. This results from the hydrogen atoms' penetration into the sub-layer, which facilitates the structural re-arrangement and crystallization. The high crystallinity gives rise to a better doping efficiency, because the crystalline phase is much easier to be doped than the amorphous phase. However, continuing to increase the treatment cycle numbers has some side effects. It may degrade the film's thickness uniformity. In this case, the film at the edge of the superstrate may be lost or much thinner than the film at the centre. In our experiments, without using a shower head to control the gas flow, the film at the pump side of the chamber (i.e., where the gases are pumped out) got much thinner (or eventually even got lost) compared to the film formation at the gas side (where the gases are injected). This is because the hydrogen plasma treatment step disrupts the Si deposition process. As a result, the more plasma treatment steps are used during the experiment, the poorer the films' thickness uniformity will be. This side effect will also degrade the film's properties,

such as a lower conductivity as shown in Figure 3.3(b). To reduce this side effect, according to our experiments, some improvement can be achieved by slightly increasing the process pressure. The residence time (τ_{res}) of the SiH_4 gas in the chamber can be estimated from Equation (3.2) [121]. It indicates that an increase of the pressure may prolong the residence time of the gas in the chamber, which is good for the stabilization of the Si deposition process.

$$\boldsymbol{\tau_{res} = F_{SiH4}\, pV/kT}\,; \tag{3. 2}$$

where F_{SiH4} is the flow rate of SiH_4, p is the process pressure, V is the volume of the chamber, k is the Boltzmann constant, and T is the gas temperature.

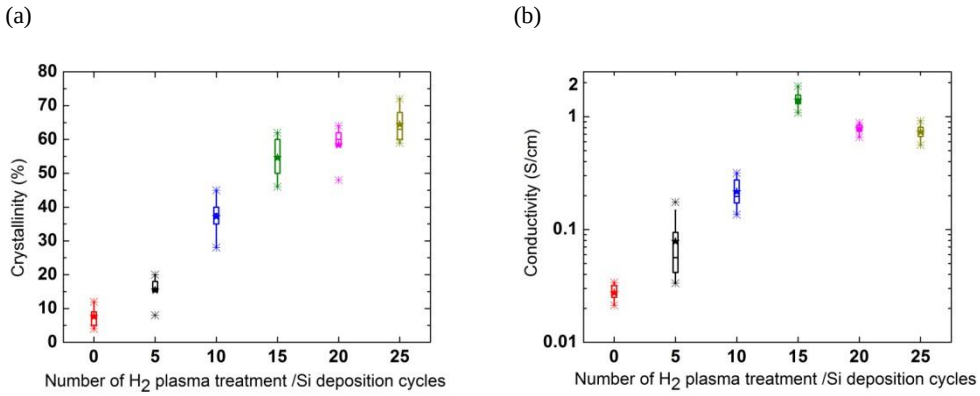


Figure 3.3: Measured dependence of (a) the Si film crystallinity and (b) electrical conductivity on the number of H_2 plasma treatment/Si deposition cycles. The duration of each hydrogen plasma treatment step was 60 s. The final Si film thickness was in the range of 25-30 nm for both graphs.

On the other hand, for a fixed plasma treatment cycle number of 10 times, Figure 3.4 shows that the crystallinity and conductivity both increase with increasing duration of the H_2 plasma treatment step. However, the increase is not as large as in the case of increasing plasma treatment cycles (see Figure 3.3). When the treatment duration is long enough (> 120 s), the crystallinity and conductivity values start to saturate. This indicates that the hydrogen plasma treatment's etching effect may also be saturated and, after that, the hydrogen plasma imposes the ion bombardment on the surface of the film. As a result, the hydrogen plasma may further weaken the Si-Si

bonding. This in turn will generate more dangling bonds and defects, which degrades the film's quality. From this point of view, it is not advisable to prolong the hydrogen plasma treatment duration. Instead, increasing the number of treatment cycles and correspondingly shortening the treatment duration seems to be a better choice.

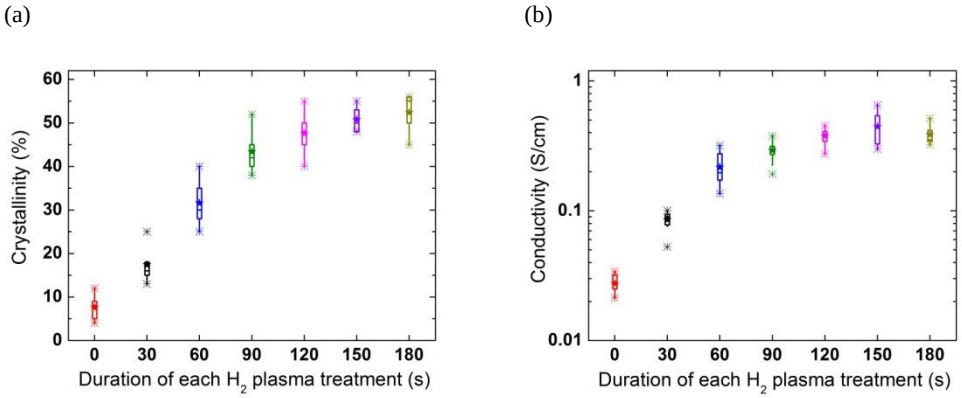


Figure 3.4: Measured dependence of (a) the Si film's crystallinity and (b) the electrical conductivity on the duration of each hydrogen plasma treatment step. The number of hydrogen plasma/Si deposition cycles was fixed at 10. The final Si film thickness was in the range of 25-30 nm for both graphs.

3.2.3 µc-Si:H p-layer deposition onto TCO-coated planar glass

The properties of the µc-Si:H film not only depend on the deposition conditions, such as rf power, process pressure and gas flow rates, but are also strongly affected by the initial growth interface. Often, the µc-Si:H films are deposited onto bare glass sheets to examine their properties. However, when they are deposited onto TCO-coated (e.g., SnO_2:F or ZnO:Al) glass sheets, the results may be quite different. First, the TCO materials are highly conductive. Their presence may result in a change of the local electromagnetic field distribution near the superstrate surface and thus may affect the glow discharge. This may cause a process recipe drift compared to depositions onto bare glass (which is a non-conductive superstrate). Second, under the situation of high superstrate temperature and a high hydrogen concentration in the gas phase, the TCO's surface region may be easily chemically deoxidized by the hydrogen atoms, forming a very thin defect-rich layer at its surface. On such an initial

growth interface, it is difficult for the Si film to nucleate and to develop a crystalline phase [122]. Therefore, the incubation layer may be much thicker for a TCO-coated superstrate than for a bare glass superstrate. Thus, it is more difficult to fabricate a very thin µc-Si:H film with high crystallinity and conductivity on TCO-coated superstrates.

In order to avoid the chemical deoxidization reaction at the TCO surface, one possible solution is to lower the superstrate temperature. Drevillon has reported that tin oxide is deoxidized by hydrogen at 200 °C, but is stable below 150 °C, while zinc oxide still displays quite a good stability at about 200 °C [123]. In the present study, the LBL method was also used for µc-Si:H thin film deposition onto glass coated with ZnO:Al made by sputtering. As mentioned above, before the µc-Si:H deposition, a very thin amorphous Si layer was deposited onto the TCO. In this way, the interface becomes Si-Si rather than TCO-Si, with the additional benefit that the amorphous Si layer also serves as a protection layer for the TCO. Therefore, it is effective to avoid the formation of the inactive layer at the TCO surface. Using 15 hydrogen plasma/Si deposition cycles and a fixed hydrogen plasma duration of 60 s, about 30 nm thick boron-doped µc-Si:H thin films with a crystallinity value larger than 60 % were successfully grown on the TCO-coated superstrates.

3.2.4 µc-Si:H p layer deposition onto textured glass sheets (AIT glass)

Apart from the impacts of superstrate or interface properties discussed above, the superstrate morphology also has a strong influence on the µc-Si:H film growth and even on the solar cells' performance [39, 40, 124]. The superstrate morphology's influences include the surface roughness, the structural shape of the texture (for example V-shape or U-shape), the opening angle of the structures, and so on. All

these factors will affect the μc-Si:H film growth, especially in the initial stage. In this study, p-type μc-Si:H films were deposited onto glass sheets that were textured on one surface with the AIT method [125, 126]. The AIT glass sheets have a high surface roughness value of about 500 - 600 nm and a high haze value of above 50 %, as measured by an optical profiler and a digital haze meter, respectively. A typical SEM image of the surface of an AIT glass sample is shown in Figure 3.5.

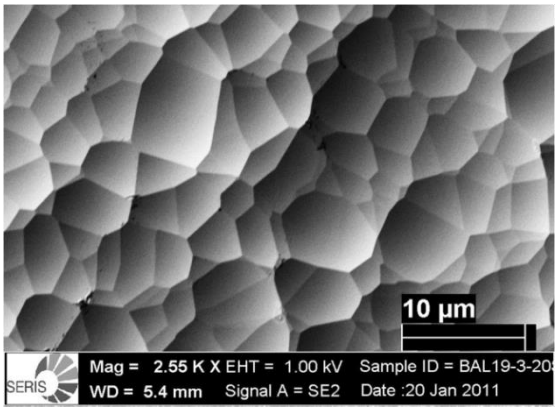


Figure 3.5: Top-view SEM image of an AIT glass surface.

The Si films were deposited with the LBL method, using 10 hydrogen plasma/Si deposition cycles with a fixed hydrogen plasma duration of 60 s. The properties of the resulting p-layers on planar glass and AIT glass are quite different, as can be seen from Table 3.2. It is found that the film on the textured glass superstrate has both higher crystallinity and higher conductivity than the one on the planar glass, although both were grown with the same deposition conditions. This indicates that the super-strate surface morphology plays an important role for the film growth.

Table 3.2 Properties of μc-Si:H p-layers grown with identical deposition conditions on planar glass and AIT glass.

30 nm thick p-layer properties	On planar glass	On textured glass
Crystallinity (%)	> 30	> 50
Conductivity (S/cm)	> 0.2	> 0.5
Surface roughness (nm)	0	500 - 600

Due to the high surface roughness, the textured superstrate (see Figure 3.5) has a much larger surface area than the planar superstrate. Furthermore, the texture seems to result in a better hydrogen coverage of the growth interface, which in turn produces a higher crystallinity of the film (see Chapter 2.2.2). Generally, a high crystallinity (i.e., a high fraction of crystalline material in the film) will be good for improving the doping efficiency. Thus, the conductivity of the textured film is higher than that of the planar film, see Table 3.2.

With respect to the influence of the surface roughness on the μc-Si:H film growth, Li *et al*. have shown by XTEM observations that there are more crystallites on a rougher region than on the flat region at the superstrate/silicon interface [40]. They also pointed out that the different chances of forming silicon nucleation sites on the tips and in the valleys of a textured superstrate surface will bring in the structural inhomogeneity of the film. In our study, a much rougher superstrate was used for μc-Si:H film deposition than in Ref. [40]. Hence, the structural inhomogeneities are expected to be more serious. Furthermore, according to some reports in the literature, a very rough superstrate may not be acceptable for solar cell growth because it may cause the formation of micro-voids and micro-cracks at the TCO/silicon interface [39, 127, 128], which in turn cause serious shunting problems in devices (see Chapter 6). One possible solution may be to deposit a very thick (several μm) TCO layer onto the textured superstrate, giving a TCO surface that is less rough than the textured glass superstrate. Moreover, an Ar plasma treatment can be used for smoothening the TCO surface [127, 128], further reducing the negative growth aspects of the rough surface. Further investigation of the influence of the surface morphology of the superstrate on the thin-film growth will be carried out in Chapter 6.

3.3 The best-achieved structural and electrical properties of the µc-Si:H p- layers on different superstrates

Figure 3.6 shows a photograph of about 30 nm thick µc-Si:H p-layers deposited onto the different types of superstrates. The different colours are ascribed to the different optical scattering effect (i.e. between planar and textured superstrates) and the different reflection effect due to the different refractive index for each layer.

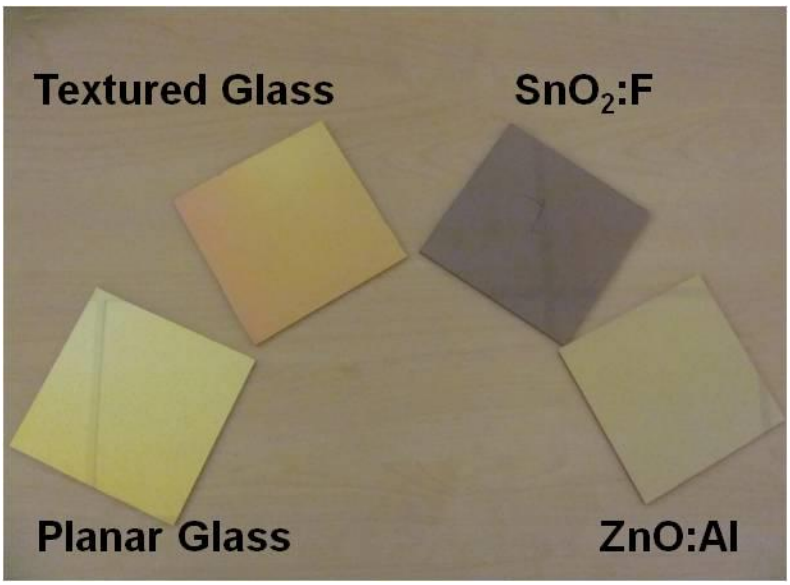


Figure 3.6: Photograph of boron-doped µc-Si:H p^+-layers deposited onto the four different types of superstrates.

Table 3.3 listed the best-achieved p-layer properties in this study. Specifically, in Chapter 3.2.2 it was shown that the layer crystallinity can be well controlled with the layer-by-layer method. It provides a very wide crystallinity range (i.e. 0 – 70 %) for the future study of the impact of the p-layer crystallinity on the solar cell I-V performance. Most importantly, this method can be widely and successfully applied to many different types of superstrates.

Table 3.3 The best-achieved structural and electrical properties of the 30 nm thick µc-Si:H *p*-layers on different superstrates. The symbol "X" means the film's conductivity on the TCO could not be measured.

30 nm thick P layer on	Planar glass	Planar glass with SnO_2:F	Planar glass with ZnO:Al	Textured glass
Crystallinity (%)	70	~ 55	~ 65	> 60
Conductivity (S/cm)	> 1	X	X	> 0.5
Uniformity	good	good	good	poor

3.4 Summary

In this chapter, a study of the µc-Si:H *p*-layer deposition on different types of superstrates was carried out. First, a brief introduction of the requirements for the *p*-layer was given. Next, experimental evidence was provided that the layer-by-layer method is capable of producing very thin (< 30 nm) *p*-layers with high crystallinity (above 60%) and high conductivity (above 1 S/cm). Most importantly, this method provides good control of the layer crystallinity over a very wide range (0 - 70 %) and is applicable to many different types of superstrates.

Chapter 4: Impact of a buffer layer at the p/i interface of µc-Si:H thin-film solar cells deposited on TCO-coated planar glass superstrates

4.1 Establishing a baseline for thin-film µc-Si:H solar cells at SERIS: No buffer layer (reference cells)

Crystallinity (i.e. the crystalline phase fraction) is a determining factor for the *I-V* parameters of µc-Si:H solar cells. In this section, the influence of the crystallinity of the intrinsic µc-Si:H absorber layer (*i*-layer) on the cell's *I-V* parameters is investigated. A certain range of crystallinity (used as "baseline") providing the best solar cell efficiency is selected for the cell fabrication in all the experiments in the following studies. Furthermore, it should be emphasized that the one-sun *I-V* parameters of the µc-Si:H cells are also significantly impacted by the cell thickness. In general, with increasing cell thickness, J_{sc} increases (more light will be absorbed) but V_{oc} decreases (because of higher excess carrier recombination in the absorber) [129].

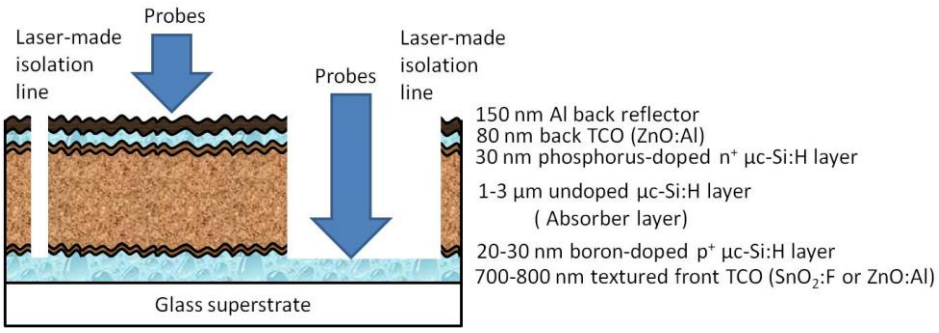


Figure 4.1: Cross-sectional schematic of the µc-Si:H thin-film solar cell after laser patterning. During the *I-V* measurements, three probes touch the front TCO and the other three probes touch the Al back contact.

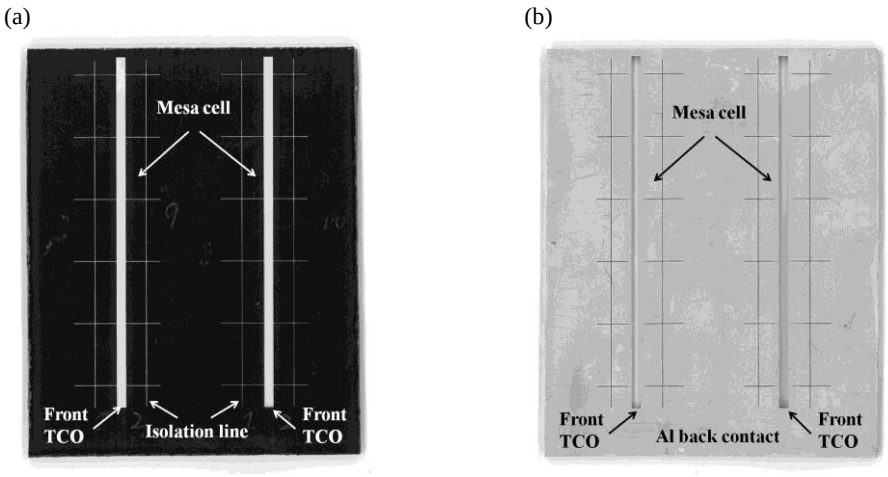


Figure 4.2: Photographs of the sample after the laser patterning process. (a) front side (glass side) and (b) rear side (Al back contact). For each sample, 20 identical mesa cells were processed (cell area of 1.02 cm^2, i.e. 1.7 cm × 0.6 cm).

In order to build up the baseline and shorten the time for cell fabrication, a series of µc-Si:H cells with a relatively thin absorber layer (around 1 µm), but with different crystallinity, were made on the planar glass coated with a nanotextured TCO layer. Figure 4.1 shows the cell structure. All cells were fabricated on A3 size (30×40 cm^2) commercial glass sheets coated with a SnO_2:F film with a nanotextured surface (commercial TCO glass sheet supplied by NSG Glass Corp.). In order to protect the SnO_2:F from the hydrogen plasma induced damage (which is commonly observed during µc-Si:H deposition [123]), a very thin layer of ZnO:Al film was coated onto the SnO_2:F by magnetron sputtering. Next, a 20 - 30 nm thick boron-doped µc-Si:H *p*-layer was deposited in a separate chamber of a conventional RF (13.56 MHz) parallel-plate PECVD system. Then followed the deposition of an around 1 µm thick intrinsic µc-Si:H absorber layer, followed by a phosphorus-doped µc-Si:H *n*-layer. Here, the intrinsic µc-Si:H films were fabricated with the "hydrogen profiling method" [130], [66] (the hydrogen gas flow rate was varied during the deposition to control the film growth and crystallinity), as described in more detail in Appendix B. The crystallinity of the µc-Si:H films was measured by Raman spectroscopy, using a green laser with an excitation wavelength at 514 nm. The Raman measurements were

performed from the *n*-layer side. They reveal the crystallinity of the last-deposited part of the µc-Si:H absorber layer. After the Raman measurements, an ZnO:Al/Al stack with approximate thicknesses of 80 and 150 nm, respectively, was deposited by magnetron sputtering onto the cells as the back reflector (also functions as back contact). Finally, laser scribing was applied to prepare µc-Si:H mesa cells with area of 1.02 cm^2, as shown in Figure 4.2. During the current density versus voltage (*I-V*) measurements under an AM1.5G solar simulator at room temperature, three probes touched the front TCO and the other three probes touched the Al back contact, providing the input voltage by one pair of probes and collecting the measured current signal by the other two pairs of probes, as described in the caption of Figure 4.1.

The experimental dependence of the one-sun *I-V* parameters on the crystallinity of the i-layer is shown in Figure 4.3.

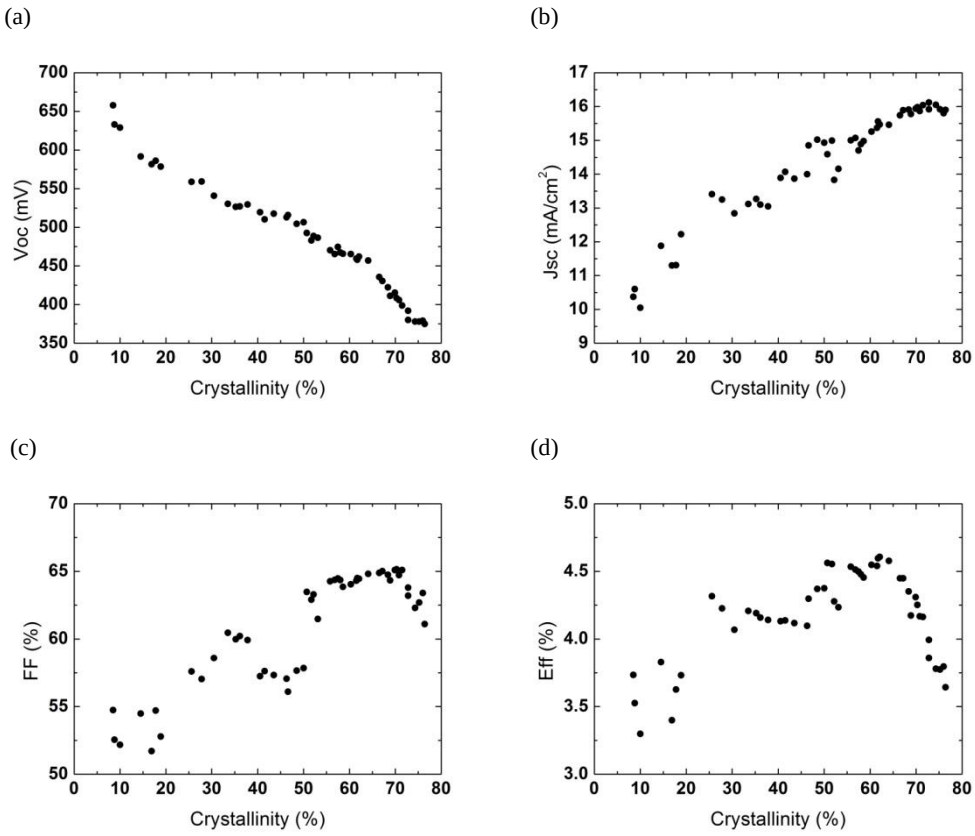


Figure 4.3: Experimental dependence of the one-sun *I-V* parameters of thin-film µc-Si:H solar cells on the Raman crystallinity of the 1 µm thick intrinsic µc-Si:H absorber layer. (a) open-circuit voltage, (b) short-circuit current, (c) fill factor, (d) conversion efficiency.

First, the V_{oc} is significantly impacted by the crystallinity of the i-layer, as shown in Figure 4.3(a). The roughly linear decrease of V_{oc} with increasing crystallinity can be explained as follows:

(a) Bandgap shrinking. Generally, the bandgap is about 1.75 eV for amorphous silicon and about 1.1 eV for crystalline silicon. When the crystallinity of the μc-Si:H film increases, its effective bandgap tends to decrease and finally gets close to 1.1 eV, making the μc-Si:H film behave more like c-Si. Since the bandgap of the absorber layer is one of the critical factors for V_{oc}, the shrinking bandgap due to the increasing crystallinity is one of the reasons for the decreasing V_{oc}.

(b) High paramagnetic defect density. As already reported, the μc-Si:H films have a high paramagnetic defect density at the level of 10^{16} - 10^{17} cm^{-3} according to electron spin resonance (ESR) measurements [65] and it increases significantly as the films become highly crystallized because hydrogen atoms were etched away from the grain boundaries [87]. Moreover, the defects will lead to non-radiative recombination in the μc-Si:H films [131] and weaken the internal electric field in the absorber layer, which can limit the quasi Fermi level splitting. As a result, the cells suffer from decreasing V_{oc} when the crystallinity increases.

(c) Formation of shunting paths. From the high-resolution TEM images, it can be observed that the highly crystallized μc-Si:H films contain a high density of grain boundaries [69]. These grain boundaries provide shunting paths, i.e. they can cause "localized shunting" of the diode, which decreases the V_{oc}.

Furthermore, the amorphous phase in the μc-Si:H films plays an important role in passivation of grain boundary and suppressing the shunting current. Therefore, a low crystallinity is needed to keep V_{oc} high enough as shown in Figure 4.3(a).

On the other hand, J_{sc} increases as the crystallinity increases, see Figure 4.3(b). The amorphous phase in the μc-Si:H film has a large bandgap, and thus negligible e-h

pair generation in the infrared wavelength region. Increasing crystallinity of the film reduces its bandgap, and thus increases the e-h pair generation by infrared wavelengths. As shown in Figure 4.4(a), with increasing crystallinity there is a clear enhancement of the EQE at long wavelengths (> 700 nm). Additionally, the carrier mobility is higher in the crystalline phase than in the amorphous phase, further enhancing the carrier collection.

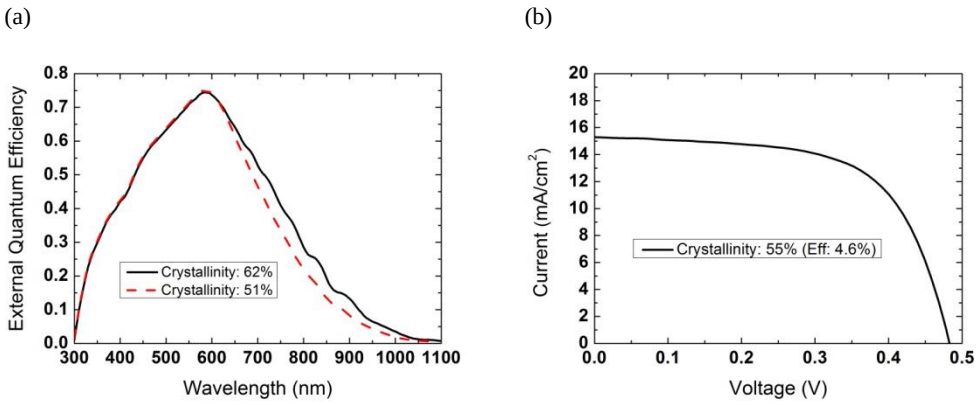


Figure 4.4: (a) Measured EQE curves of thin-film µc-Si:H solar cells having a "baseline" crystallinity in the range of 50 - 60 % of the 1 µm thick intrinsic µc-Si:H absorber layer. (b) One-sun *I-V* curve of a thin-film µc-Si:H solar cell having a "baseline" crystallinity of 55 % of the 1 µm thick intrinsic µc-Si:H absorber layer (the "baseline" crystallinity range was set to 50 - 60 %)

For *FF*, it initially improves as the crystallinity increases, see Figure 4.3(c). This effect can also be attributed to the better carrier mobilities in the crystalline phase, which causes a lower series resistance (R_s) in the solar cells. However, when the crystallinity exceeds about 70 %, the *FF* starts to drop because of increasing shunting issues.

Finally, the maximum efficiency occurs for a crystallinity in the 60 - 70 % range, due to the improved J_{sc}, as shown in Figure 4.3(d). However, the cells have relatively low V_{oc} (around 400 mV) in this range. High V_{oc} (above 500 mV) can be achieved when the crystallinity is around 50 % and, at the same time, the loss of the J_{sc} can be compensated by using light trapping methods. Therefore, a crystallinity in the 50 - 60 % range is considered to be the most suitable for fabrication of µc-Si:H cells. This

conclusion is supported by high cell efficiencies reported in the literature for such a crystallinity [132].

Based on the above analysis, a crystallinity in the 50 - 60 % range was used as baseline for solar cell fabrication in all the following experiments. Selected *I-V* and EQE curves of such 'baseline' µc-Si:H cells having a 1 µm thick absorber layer are shown in Figure 4.4. It is emphasised that the differences in EQE due to the different crystallinity (~50% and ~60%) only occur in the long wavelength region (> 650 nm). The blue response is not affected. Thus, the results for different buffer layers described in the following are not affected by a slight variation of the crystallinity of the baseline cells.

As compared to state-of-the-art µc-Si:H cells having efficiency of around 10.8 % (using a 3 µm thick absorber layer) [82, 83], there is still a large room for the improvement of our cell performance. First of all, further optimization of the surface morphology of the superstrate is required, to improve the absorption of long-wavelength photons (which is still quite weak, see Figure 4.4(a)). This topic will be further discussed in Chapter 6, by using textured glass as superstrates. Furthermore, the *FF* is still well below 70 % due to the high series resistance. Also, further optimization of all the interfaces to facilitate the carrier collection is still needed. This will simultaneously improve the cells' blue response. This interface optimisation is the main topic to be discussed in this chapter.

Although the baseline cells of this thesis have a low efficiency (~ 5 %) compared to state-of-the-art µc-Si:H cells, their quality is sufficient to address (i) the question whether different types of buffer layer can improve the cell efficiency and (ii) the question whether the absorption of long-wavelength photons can be improved by using textured glass. The investigation of these questions is the main topic of this PhD thesis.

4.2 Classification of different buffer layers

Four types of silicon films with different structural configuration (from standard a-Si:H to fully crystallized μc-Si:H films), see Figure 4.5, were used as buffer layer at the p/i interface of μc-Si:H solar cells:

① Type-I: Pure a-Si:H buffer layer as shown in Figure 4.5(a);

② Type-II: Buffer layer consisting of isolated nano-size μc-Si:H nuclei or grains embedded in the amorphous silicon matrix, as shown in Figure 4.5(b);

③ Type-III: Buffer layer consisting of percolating μc-Si:H grains or fibres embedded in the amorphous silicon matrix, as shown in Figure 4.5(c);

④ Type-IV: Highly crystallized μc-Si:H buffer layer as shown in Figure 4.5(d); compared to a Type-III buffer layer, it has much higher crystallinity and larger grains. As a result, this buffer layer contains more c-Si/c-Si grain boundaries.

Based on the above classification of the buffer layers, it is expected that the buffer layers containing more a-Si:H will cause higher V_{oc} (since a-Si:H is known for its excellent surface passivation of c-Si), while those containing more μc-Si:H will improve the carrier collection near the p/i interface (enhancing the blue response) and finally give higher J_{sc} (since μc-Si:H grains with higher carrier mobility will enhance carrier transport, especially when the film gets the formation of μc-Si:H percolation path to facilitate the carrier transport). Experiments will be carried out in the following sections to test these assumptions.

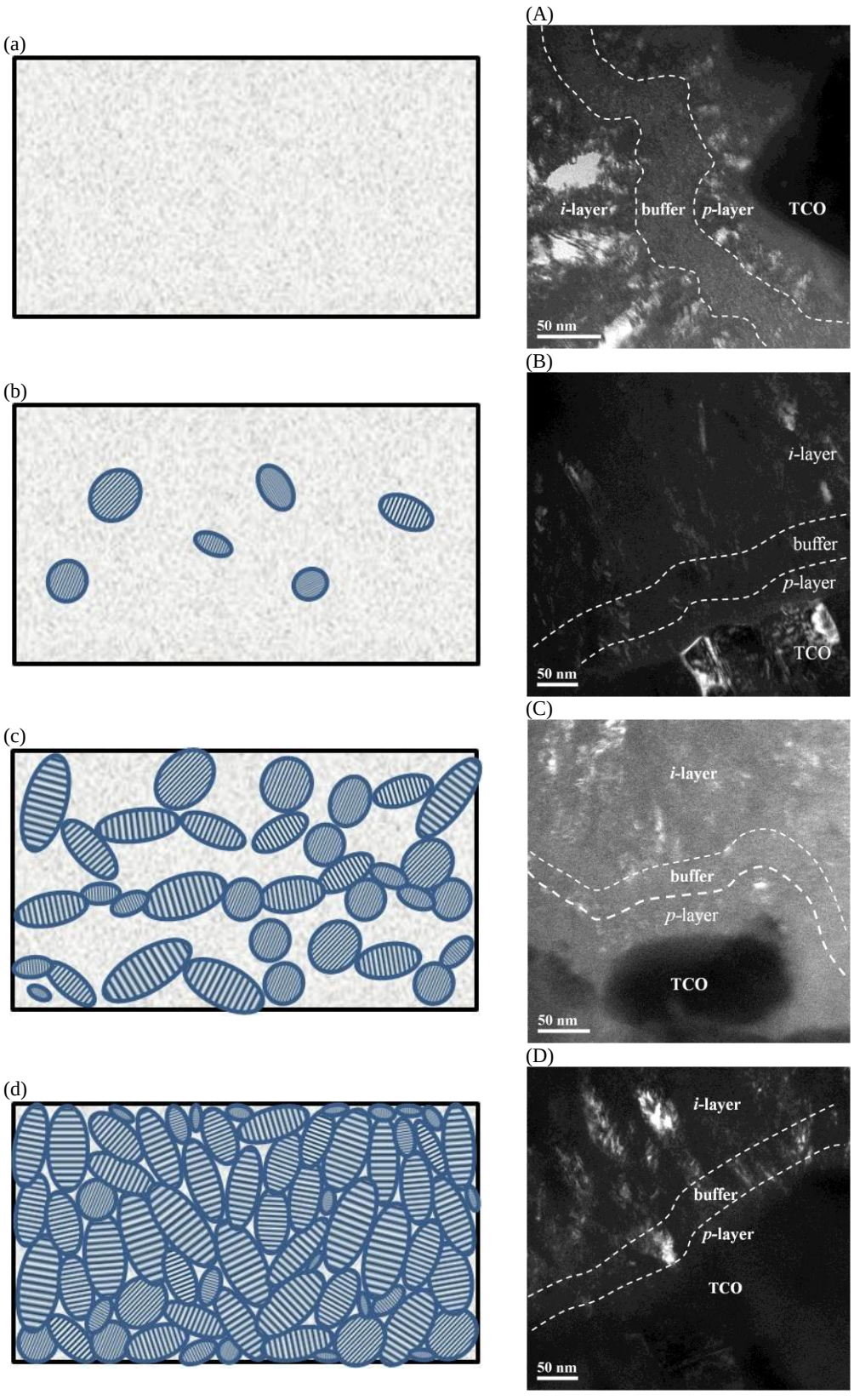


Figure 4.5: Schematics of the four types of investigated buffer layers, and their corresponding XTEM images. (a) Type-I buffer layer consisting of standard a-Si:H; (b) Type-II buffer layer, consisting of isolated μc-Si:H grains embedded in an a-Si:H matrix; (c) Type-III buffer layer, consisting of percolated μc-Si:H grains or fibres embedded in an a-Si:H matrix; (d) Type-IV buffer layer consisting of a "fully crystallized" μc-Si:H film.

4.3 Experimental methods used to produce different buffer layers

Different deposition conditions are needed to produce a-Si:H and µc-Si:H films. The deposition conditions for the four types of investigated buffer layers are schematically shown in Figure 4.6.

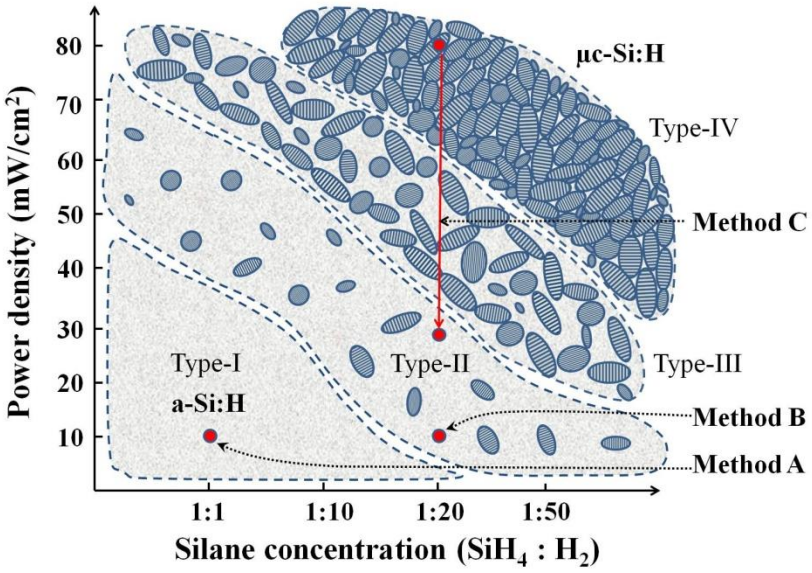


Figure 4.6: Schematic of deposition condition regions for the film evolution from standard a-Si:H to fully crystallized µc-Si:H.

Three types of methods were used to fabricate different types of buffer layers in this thesis, as also highlighted in the Figure 4.6. Table 4.1 listed the deposition parameters for the above three methods. In addition, more details about these three methods are given in the following sub-sections.

Table 4.1 Deposition parameters for the different deposition methods used to fabricate different types of buffer layers.

Deposition parameter	a-Si:H deposition	Transition region deposition	Power profiling deposition
Excitation frequency (MHz)	13.56	13.56	13.56
Substrate temperature (˚C)	200	200	200
Pressure (Torr)	0.5	0.5	1.8
Power density (mW/cm^2)	10	10	80 → 30
$Si:H_4 : H_2$	1:1	1:20	1:20

4.3.1 Method A: a-Si:H deposition

In general, to process standard a-Si:H (without the nucleation), a low discharge power and a low hydrogen gas flow rate are applied. 'Low discharge power' is used to maintain the ion energy at a relatively low level for the purposes of (1) avoiding the serious plasma etching of the film surface (which causes many dangling bonds and/or a disordered structure); (2) avoiding the formation of crystalline nuclei. A certain amount of hydrogen gas was also mixed with silane (SiH_4:H_2 = 1:1 - 1:10) to produce enough hydrogen atoms for surface passivation of dangling bonds. But a very large amount of hydrogen gas may also lead to nucleation. Thus, a low hydrogen gas flow rate was used in the experiments.

4.3.2 Method B: Deposition in the transition region (from a-Si:H to μc-Si:H)

As discussed above, a high hydrogen gas flow rate (*i.e.* SiH_4:H_2 > 1:20) may cause nucleation because of the hydrogen permeation into the a-Si:H network and structural relaxation [60]. In this case, the film deposition occurs in the transition region from a-Si:H to μc-Si:H. Method B uses a low discharge power and a high hydrogen gas flow rate to realize such conditions. In general, if the film is deposited onto glass using Method B, a Type-II buffer layer will be obtained as shown in Figure 4.6. However, when the film grows on a μc-Si:H *p*-layer, the initial epitaxial growth causes a Type-III buffer layer at the beginning but later it gradually changes towards Type-II material as the film becomes thicker. Therefore, the type of buffer layer obtained by Method B is thickness dependent (transition from Type-III to Type-II as a function of film thickness).

4.3.3 Method C: Power profiling method

As illustrated in Figure 4.6, the crystallinity or the type of the buffer layer is largely determined by the power density, which is a direct factor to impact the ion energy and the Si film growth [133]. This means that the growth of μc-Si:H can be well controlled by changing the input power. Based on this principle, a 'power profiling method' was designed and the input power was varied during the film deposition, as illustrated in Figure 4.7.

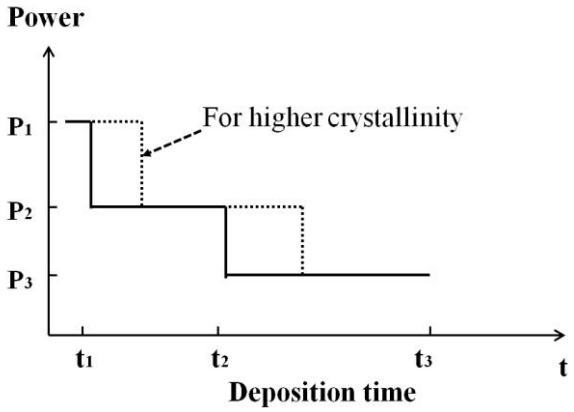


Figure 4.7: Schematic of "power profiling method".

Generally, a high power density strengthens the plasma surface etching, which tends to etch away the amorphous phase and facilitates the crystalline phase growth (see 'etching model' introduced in Chapter 2). Thus, in order to obtain a high-crystallinity film, high power is applied longer to facilitate the crystalline phase growth, see Figure 4.7. On the other hand, when the crystallinity reaches a certain level, one needs to reduce the power to suppress the further increase of the crystallinity. By doing so, the film crystallinity can be well controlled within a certain range. It should also be emphasized that Method C can produce Type-II, III and IV buffer layers at an independently chosen buffer layer thickness. This is different from Method B.

Finally, to sum up, one deposition method can produce different types of buffer layers. For example, by using the transition deposition method, an increasing buffer layer thickness (deposition time) will transfer the buffer layer from Type-III (for thin buffer layer) to Type-II (for thick buffer layer). By using the power profiling method, the buffer layer crystallinity can be tuned in a very broad range and Type-II, III and IV buffer layers can be produced. In the next section, these three methods will be used to produce the different types of buffer layers at the p/i interface of µc-Si:H solar cells.

4.4 Processing different types of buffer layers and investigating their influence on the *I-V* performance of thin-film µc-Si:H solar cells

In this section, a series of experimental investigations on the use of different types of buffer layers in order to enhance the solar cells' *I-V* performance (using *I-V*, Suns-V_{oc} and EQE) is carried out. First, various buffer layers with different material composition were realized by using the three methods discussed above and classified according to Chapter 4.2. Second, a series of solar cells with different types of buffer layers were processed, i.e. Sample-I-A (Type-I buffer layer using Method A), Sample-II-B (Type-II buffer layer using Method B), Sample-III-B (Type-III buffer layer using Method B), and so on. In principle, a thickness optimization of these buffer layers has to be performed. However, unfortunately, because the deposition equipment was destroyed by a fire incident, the optimization of the buffer layers had to be stopped prematurely (*i.e.* no thickness variation for Method A and C). Therefore, only preliminary data were obtained; nevertheless, they are sufficient to enable a clear classification of the buffer layers and to compare the various solar cells.

4.4.1 Reference (no buffer layer)

As a reference, Figure 4.8(a) shows an XTEM image of the region near the p/i interface of a µc-Si:H thin-film solar cell without a buffer layer. No clear interface can be observed between the *p*- and *i*-layer, as XTEM cannot distinguish between intrinsic and doped µc-Si:H of the same structural composition.

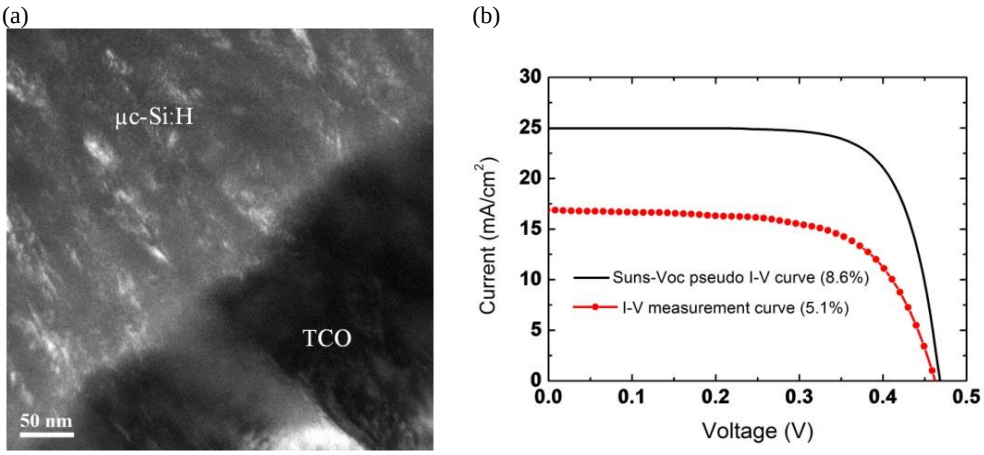


Figure 4.8: (a) XTEM image of a thin-film µc-Si:H reference solar cell (without buffer layer). No clear interface can be observed between the *p*- and *i*-layers. (b) One-sun *I-V* and suns-V_{oc} pseudo *I-V* measurements of a thin-film µc-Si:H reference solar cell (without buffer layer). The corresponding cell efficiencies are shown in the legend.

Figure 4.8(b) shows the one-sun *I-V* curve and Suns-V_{oc} pseudo *I-V* curve for the reference cell having an approximately 1.2 µm thick µc-Si:H absorber layer (crystallinity was in the 50 - 60 % range). In the following sections, except if stated otherwise, the µc-Si:H absorber layers of all solar cells had a fixed thickness of around 1.2 µm. The pseudo short-circuit current density of 25 mA/cm^2 was chosen because this value has been reported in the literature for high-efficiency thin-film µc-Si:H solar cells with p-i-n configuration and good light trapping [14]. The measured one-sun J_{sc} of our cells was still quite low at this point in time because the light trapping (textured surface) was not yet optimized (light trapping to improve the current will be investigated and realized in Chapter 6). Both measurements confirmed that the 1-sun V_{oc} of the reference cells is around 460 mV. However, the pseudo fill

factor, which is not affected by the series resistance, is much higher (73.6 %) than the *I-V* measured value (64 %). This indicates that the cell suffers from a high series resistance (3.6 Ωcm^2).

4.4.2 Method A (a-Si:H deposition): Processing of Type-I buffer layer

Using Method A, an approximately 30 nm thick a-Si:H buffer layer was inserted between the p/i interface of a µc-Si:H thin-film solar cell, as shown in Figure 4.9(a). It can clearly be distinguished between the µc-Si:H (*i.e. p*- and *i*-layer) and a-Si:H (buffer layer), since the crystalline phase appears bright in dark-field XTEM images. The buffer layer thus forms an a-Si:H/ µc-Si:H heterojunction at the interface. It is labelled as "Sample-I-A" for later comparison with other types of buffer layers.

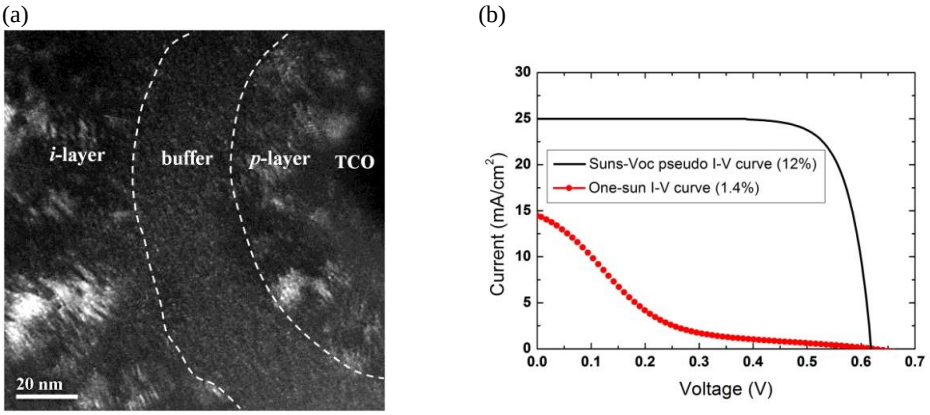


Figure 4.9: (a) XTEM image of a thin-film µc-Si:H solar cell, using a Type-I buffer layer processed by method A (amorphous silicon deposition). The thickness of the inserted buffer layer is ~30 nm. (b) One-sun *I-V* and suns-Voc pseudo *I-V* measurements for a thin-film µc-Si:H solar cell, using a Type-I buffer layer processed by method A (amorphous silicon deposition). The corresponding cell efficiencies are shown in the legend.

The measured one-sun *I-V* curve and pseudo *I-V* curve (from Suns-V_{oc}) are shown in Figure 4.9(b). Because the a-Si:H buffer layer was too thick and thus impeded the carrier collection, the extremely high series resistance (> 100 Ωcm^2) and non-linear recombination caused a S-shape *I-V* curve, as shown in Figure 4.9(b). However, the V_{oc} (625 mV) was very good. This is also confirmed by the pseudo *I-V* curve (which

is not affected by series resistance effects), giving a pV_{oc} of 621 mV and a *pFF* of 77.2 %.

As expected, both measurements verify that a very high V_{oc} can be obtained if an a-Si:H buffer layer is used (improvement from around 500 mV to above 600 mV). However, as mentioned above, a thickness optimization is still needed in future work (not included in this thesis).

4.4.3 Method B (deposition in the transition region): Processing of Type-II and Type-III buffer layers

The transition region deposition method (Method B) was used to produce a buffer layer at the p/i interface, as explained in Chapter 4.3.2 and using the deposition parameters of Table 4.1. As explained, using Method B, the resulting material configuration of the buffer layer is thickness dependent, see Figure 4.10. The initial growth starts from epitaxial growth on the µc-Si:H *p*-layer (seeding layer) thus forming a Type-III buffer layer (for small buffer layer thickness). With increasing thickness it gradually loses the epitaxial seeding information, and thus evolves towards a Type-II buffer layer.

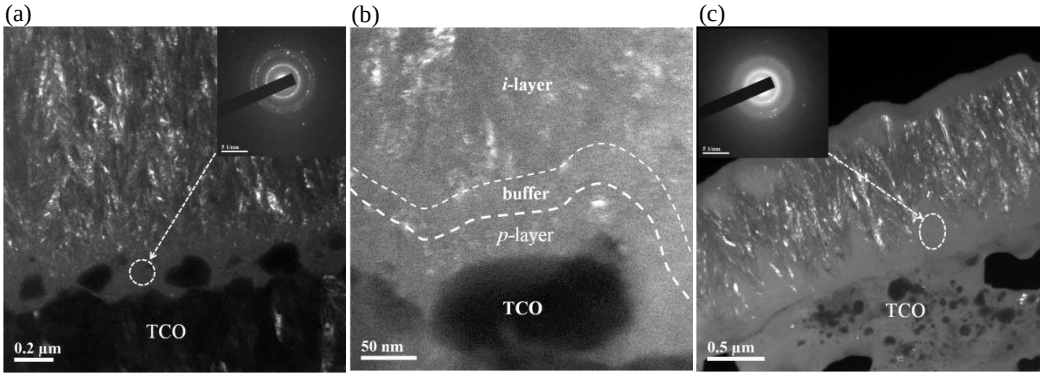


Figure 4.10: XTEM images of thin-film µc-Si:H solar cells, using a Type-II or Type-III buffer layer processed by Method B (deposition in the transition region). (a, b) thin Type-III buffer layer, achieved by using a deposition time of 140 s (estimated thickness of ~ 10 nm) shown in a (a) low-resolution image or a (b) high-resolution image. (c) Thick Type-II buffer layer, achieved by using a deposition time of 560 s (estimated thickness of ~40 nm) shown in a low-resolution image. The insets of (a) and (c) show the corresponding electron diffraction pattern.

Figure 4.10(a) and (c) show the material composition transition of the buffer layer for two different buffer layer thicknesses. If depositing a thin buffer layer (140 s deposition time, around 10 nm), the region near the *p/i* interface still contains a large fraction of µc-Si:H (Type-III buffer layer). The electron diffraction pattern inserted in Figure 4.10(a) displays both a series of diffuse halo rings and diffraction spots, which indicates that this region contains both amorphous and crystalline silicon phases. From the high-resolution image in Figure 4.10(b) it can be seen that some nanosized crystalline phases (bright areas) are embedded in the amorphous phases. When a thicker buffer layer was deposited (deposition time up to 560 s, around 40 nm thick), the region near the *p/i* interface consists of a very thick amorphous incubation layer with some isolated µc-Si:H grains (Type-II buffer layer), as can be seen from Figure 4.10(c). This incubation layer is confirmed by the fact that the diffraction spots nearly disappear and only some diffuse halo rings remain.

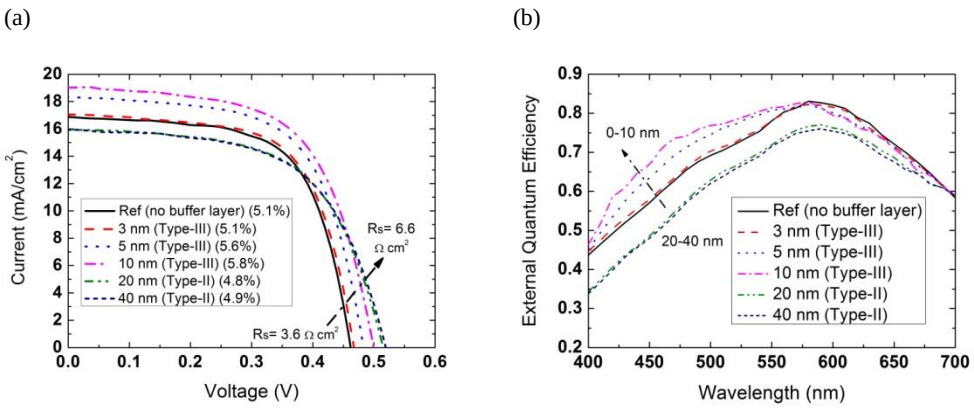


Figure 4.11: (a) One sun *I-V* measurements of thin-film µc-Si:H solar cells using a Type-II or Type-III buffer layer processed by method B (deposition in the transition region, variation of buffer layer thickness). The corresponding cell efficiencies are shown in the legend. (b) Measured EQE curves of thin-film µc-Si:H solar cells using a Type-II or Type-III buffer layer processed by method B (deposition in the transition region, variation of buffer layer thickness). For the sake of a better resolution, the EQE curves are only shown for the visible wavelength range (*i.e.* 400 - 700 nm).

One-sun *I-V* curves for the solar cells with various buffer layers are shown in Figure 4.11(a). The extracted *I-V* parameters are shown in Figure 4.12. The measured EQE curves in the visible wavelength range are displayed in Figure 4.11(b).

With increasing thickness, the buffer layer will cause a clear increase of the V_{oc}. For J_{sc}, it initially increases but then drops sharply when the buffer layer exceeds a certain thickness. Moreover, a thick buffer layer also deteriorates the *FF* of the solar cells. Thus, the maximum efficiency appears when a buffer layer with intermediate thickness is used (around 10 nm), as shown in Figure 4.11(a) and Figure 4.12, and labelled as "Sample-III-B". An efficiency increase of around 14 % (relative) was obtained as compared to the reference cell (i.e., no buffer layer), from 5.1 % to 5.8 %.

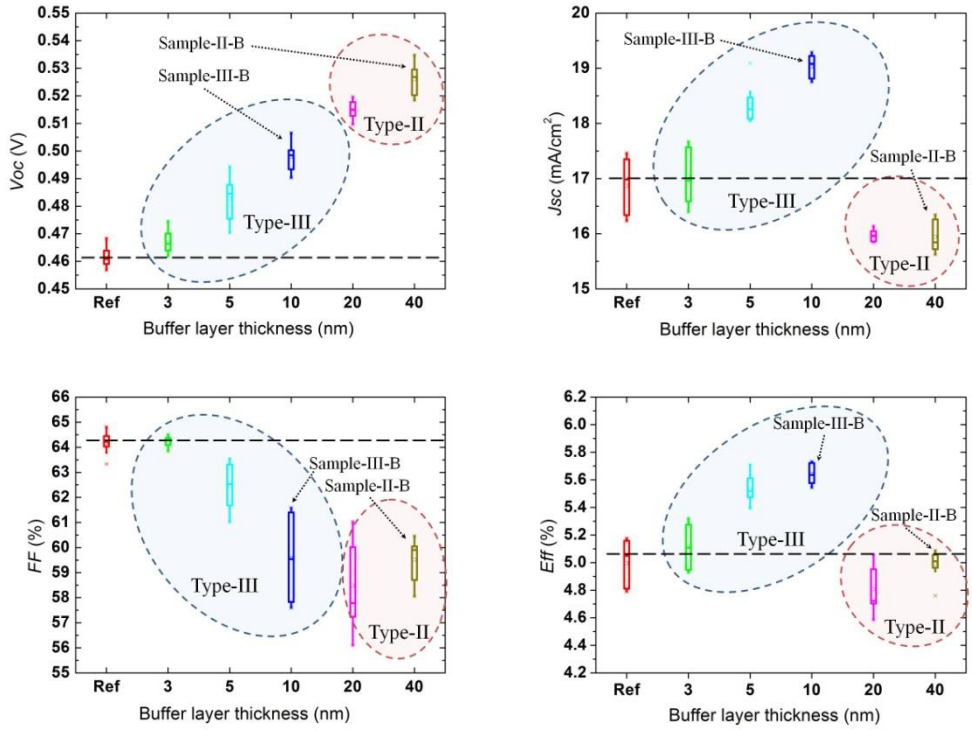


Figure 4.12: One-sun *I-V* parameters of thin-film µc-Si:H solar cells using a Type-II or Type-III buffer layer processed by method B (deposition in the transition region, variation of buffer layer thickness). The error bars indicate the spread of 10 identical mesa cells, which were processed and measured in all cases. For comparison, the I-V parameters of the reference sample (no buffer layer) are also indicated. The solar cells which are used further down for further comparisons are highlighted.

The increase of the V_{oc} can be attributed to the fact that more a-Si:H phases are contained in the buffer layer as it becomes thicker (see Sample-II-B). This evolution leads to a bandgap variation in this region. As a result, the higher bandgap of the more a-Si:H rich buffer layer will result in an increased V_{oc}. The same effect was

reported in earlier studies of a-Si:H solar cells, when a wide-bandgap buffer layer (a-SiC:H) was introduced at the p/i interface, causing a shift of the energetic position of the defects [16, 17]. Second, it has also been reported by Yue *et al.* that such kind of a-Si:H rich buffer layer can effectively lower the recombination rate at the interface and a significant decrease of reverse saturation current J_o was observed [22]. As a result, the V_{oc} can be enhanced significantly.

From Figure 4.12, when a thin buffer layer (Type-III) is used, the buffer layer does increase the J_{sc} of the cells (the J_{sc} of the Sample-III-B is higher than the reference cell without buffer layer). However, when a thick buffer layer is used, Sample-II-B has a lower J_{sc} than the reference cell. The variation of the J_{sc} by using different types of buffer layers comes from differences in the EQE for visible wavelengths, as shown in Figure 4.11(b). First of all, the thin buffer layer made by Method B, which turns out to be a Type-III buffer layer, contains the μc-Si:H percolated paths and facilitates the carrier transport and collection. But a thick buffer layer becomes Type-II and loses the percolated paths, which impedes the carrier transport. Therefore, a clear drop of J_{sc} can be observed when a thick buffer layer is used. Furthermore, additional explanations for the observed J_{sc} increase or improved blue response (when thin Type-II buffer layer are used) are: (1) the buffer layer inserted at the p/i interface can serve as a barrier layer to suppress the impurity diffusion from the bottom layers (*i.e.* boron diffusion [18]) and reduce the defect density near the interface, which has been reported in the literature using SIMS [21]. (2) This buffer layer was deposited with a low power density. Therefore, a low ion bombardment damage to the p/i interface and the region adjacent to it can be expected.

Furthermore, an apparent drop in the *FF* can be seen when the buffer layer gets thicker. This trend is clearly observed from both the *I-V* curves shown in Figure 4.11 and the extracted data shown in Figure 4.12. The poor *FF* can be attributed to the high series resistance resulting from the resistive buffer layer (because of the

existence of the a-Si:H phase). Especially for the Type-II buffer layer without the μc-Si:H percolation path, the carrier transport is impeded and the series resistance goes up further.

Table 4.2 Influence of the buffer layer processed by Method B (deposition in the transition region, variation of buffer layer thickness) on the one-sun *I-V* parameters of thin-film μc-Si:H solar cells.

	Thin buffer layer (Type-III)	**Thick buffer layer (Type-II)**
V_{oc}	Increase; Suppression of the saturation current J_o (electrical quenching effect); No a-Si:H incubation layer	Further increase; Suppression of the saturation current J_o (electrical quenching effect); Thick a-Si:H incubation layer appears;
J_{sc}	Increase; (better blue response) Suppression of the impurity diffusion ; Low ion damage, better p/i interface; μc-Si:H percolation paths maintain carrier transport.	Decrease; (poor blue response) Without μc-Si:H percolation paths and thus impeded carrier transport; Weak carrier collection;
FF	Decrease slightly; Resistive layer (because of the a-Si:H phase); Larger R_s	Decrease significantly; Impede the carrier transport; Highly resistive layer; Very large R_s

Table 4.2 summarizes the impacts of buffer layers made with transition region deposition conditions on the cells' *I-V* performances. In a brief summary, the maximum efficiency occurs when using this transition region deposition method to produce a thin Type-III buffer layer (around 10 nm) before the appearance of the a-Si:H incubation layer. It is the threshold of the μc-Si:H percolation path.

4.4.4 Method C (power profiling method): Processing of Type-II, Type-III and Type-IV buffer layers

A series of around 50 nm thick buffer layers having different crystallinity were deposited with the 'power profiling method' (Method C). This method allows producing Type-II, III, IV buffer layers as shown in Figure 4.13. The bright areas indicate the distribution of the crystalline phase in the film. For a highly crystallized film (Type-IV), as shown in Figure 4.13(a), μc-Si:H grains with relatively large size (several tens of nanometres) are formed and compacted. For the buffer layer having

intermediate crystallinity (Type-III), as shown in Figure 4.13(b), µc-Si:H grains in the nanometre scale (below 10 nm) are connected with each other to form a series of percolation paths. For the buffer layer having low crystallinity (Type-II), as shown in Figure 4.13(c), only some nuclei or nano-size µc-Si:H fibres can be observed and they are isolated by the amorphous phases without formation of percolation paths.

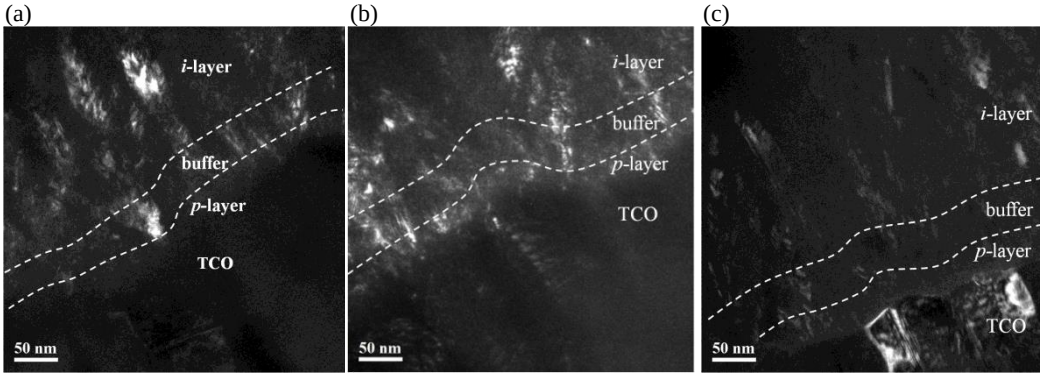


Figure 4.13: XTEM images of thin-film µc-Si:H cells, using a Type-II, Type-III or Type-IV buffer layer processed by method C (power profiling method, variation of crystallinity), i.e. (a) high crystallinity Type-IV buffer layer, (b) intermediate crystallinity Type-III buffer layer and (c) low crystallinity Type-II buffer layer.

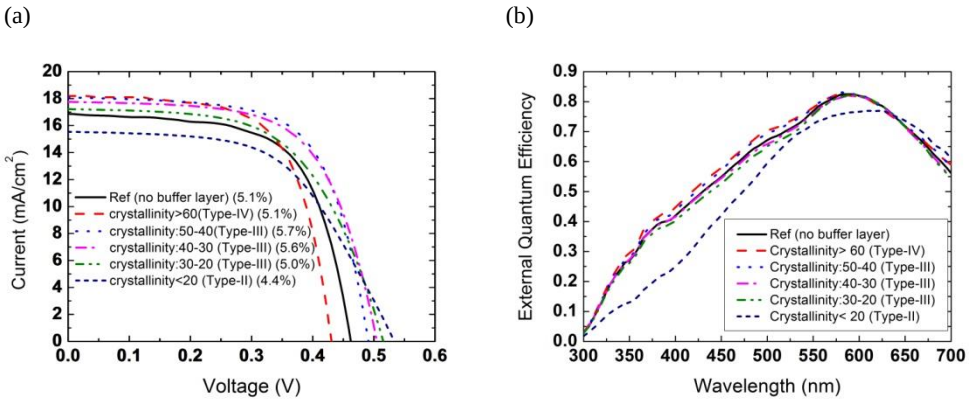


Figure 4.14: (a) One-sun *I-V* curves of thin-film µc-Si:H solar cells using a Type-II, Type-III or Type-IV buffer layer processed by Method C (power profiling method, variation of crystallinity). The thickness of the processed buffer layer is 50 nm. The corresponding cell efficiencies are indicated in the legend. (b) Measured EQE curves of thin-film µc-Si:H solar cells using a Type-II, Type-III or Type-IV buffer layer processed by Method C (power profiling method, variation of crystallinity). The thickness of the processed buffer layer is 50 nm.

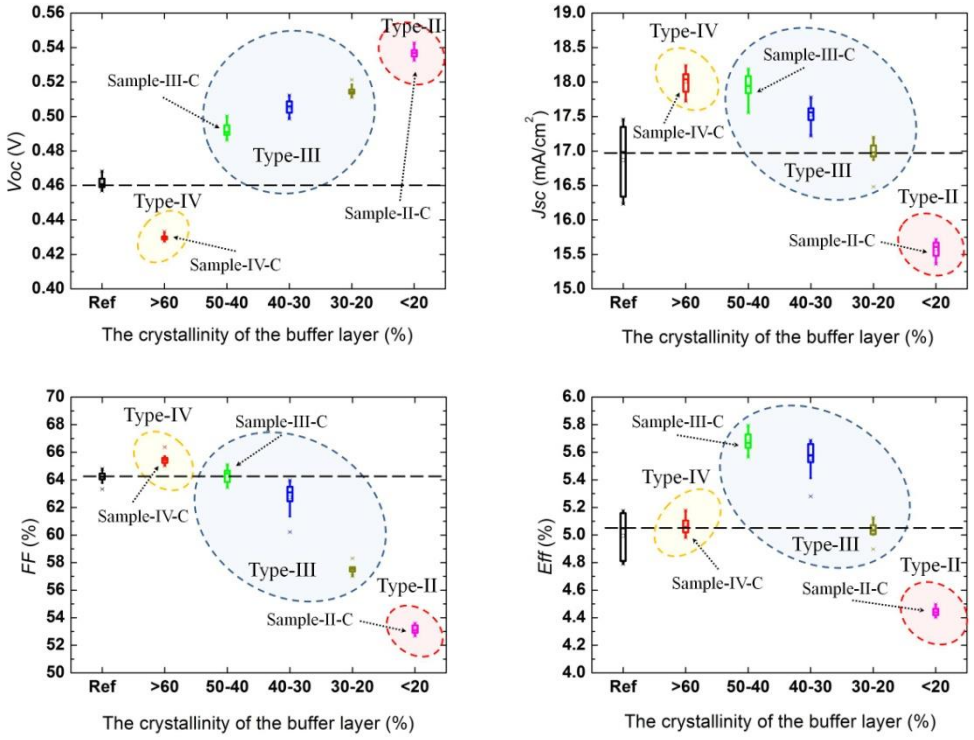


Figure 4.15: One sun *I-V* parameters of thin-film µc-Si:H solar cells using a Type-II, Type-III or Type-IV buffer layer processed by method C (power profiling method, variation of crystallinity). The thickness of the processed buffer layer is 50 nm. For comparison: the intrinsic µc-Si:H absorber layer has a crystallinity of 50 - 60 %, and the I-V parameters of the reference sample (no buffer layer) are also indicated. The solar cells which are used further down for comparisons are highlighted.

The one-sun *I-V* curves of the cells with Type-II, III and IV buffer layers produced by Method C are shown in Figure 4.14(a). Their EQE curves for the 300 - 700 nm wavelength range and the extracted *I-V* parameters are displayed in Figure 4.14(b) and Figure 4.15, respectively. From the experimental results of Figure 4.14 and Figure 4.15, it can be seen that solar cells having Type-III buffer layers achieve the highest efficiency. Again, the cells with Type-II buffer layer performed worse than the reference cells. Cells with Type-IV buffer layer had about the same efficiency as the reference cell.

Three samples were selected for comparison with the reference cell (no buffer layer), i.e. Sample-II-C, III-C and IV-C, as highlighted in Figure 4.15. First, the buffer layers having more a-Si:H (*i.e.* Sample-II-C and III-C) improve the V_{oc}. The

highly crystallized buffer layer (Type-IV) deteriorates the V_{oc}. On the other hand, the J_{sc} and *FF* get improved when more µc-Si:H phases are contained in the buffer layer (*i.e.* Sample-IV-C and III-C). As a result, the best PV efficiency must appear in between, which is the Type-III buffer layer.

It is well known in the literature that, in general, a high crystallinity leads to a low V_{oc} because of the higher mobility gap defects and lower band gap [134, 135]. Our experimental results also follow this trend. Furthermore, it should be emphasized that even if the bulk of the *i*-layer has the crystallinity of about 50 – 60 % (which should enable a V_{oc} of around 500 mV), the V_{oc} is still limited at a lower level if the film near the p/i interface is highly crystallized. For example using the Type-IV buffer layer, the crystallinity is close to 70 % as shown in Figure 4.13(a). In this case, the higher density of free and trapped carriers near the p/i interface becomes the dominant factor for the V_{oc} of the cells.

The major difference of the J_{sc} results from the discrepancy of the spectral response in the short wavelength region, see Figure 4.14(b). The µc-Si:H with low crystallinity near the p/i interface strongly reduces the blue response. It can be attributed to the loss of the µc-Si:H percolation path, as shown in Figure 4.13(c), and the decrease of the diffusion length (or lifetime) of the photogenerated carriers in the µc-Si:H with lower crystallinity. Therefore, the use of the µc-Si:H with low crystallinity (Type-II) as buffer layer will reduce the carrier collection efficiency. To improve the carrier collection, extended crystalline grains forming percolation paths are needed (Type-III buffer layer as shown in Figure 4.13(b)), which would be important for the electronic transport.

For the *FF*, it is also detrimental if the buffer layer is made with low crystallinity (Type-II). In the case of low crystallinity, the cell shows a high series resistance as indicated in the I-V curves of Figure 4.14(a), which is quite similar to the cells with a

thick a-Si:H buffer layer. It can also be attributed to the fact that a Type-II buffer layer loses the μc-Si:H percolation path and thus the carrier transport is impeded.

Finally, in a brief summary, the experimental results showed that the maximum PV efficiency is achieved when the buffer layer has a sufficiently high crystallinity (which is enough to form μc-Si:H percolation paths). A buffer layer with either very low or very high crystallinity will limit the cell *I-V* performance in certain ways.

4.5 Comparison of the impact of different types of buffer layers on the solar cell *I-V* performance

In the previous sections, the influence of the various buffer layers fabricated by different methods on the μc-Si:H cell I-V performance was stated. In this section, a comparison for the I-V parameters of the μc-Si:H cells with various buffer layers will be made. Figure 4.16 shows the one-sun I-V curves, EQE curves and pseudo I-V curves (from Suns-V_{oc} measurement) for the cells having different types of buffer layer. The extracted I-V parameters are listed in Table 4.3.

The one-sun I-V measurement results, as displayed in Figure 4.16(a), clearly demonstrate that only the Type-III buffer layers can significantly improve the solar cell efficiency (the Type-I cells are not included in this comparison, because their efficiencies are < 2 %). The efficiencies of the cells having the buffer layers processed by the various deposition methods described above show the following ranking:

$$\text{Type-III} > \text{Ref} \approx \text{Type IV} > \text{Type-II} \qquad (\text{for } Eff) \qquad (4.1)$$

The corresponding ranking for the open-circuit voltage is:

$$\text{Type-I} > \text{Type-II} > \text{Type-III} > \text{Ref} > \text{Type-IV} \qquad (\text{for } V_{oc}) \qquad (4.2)$$

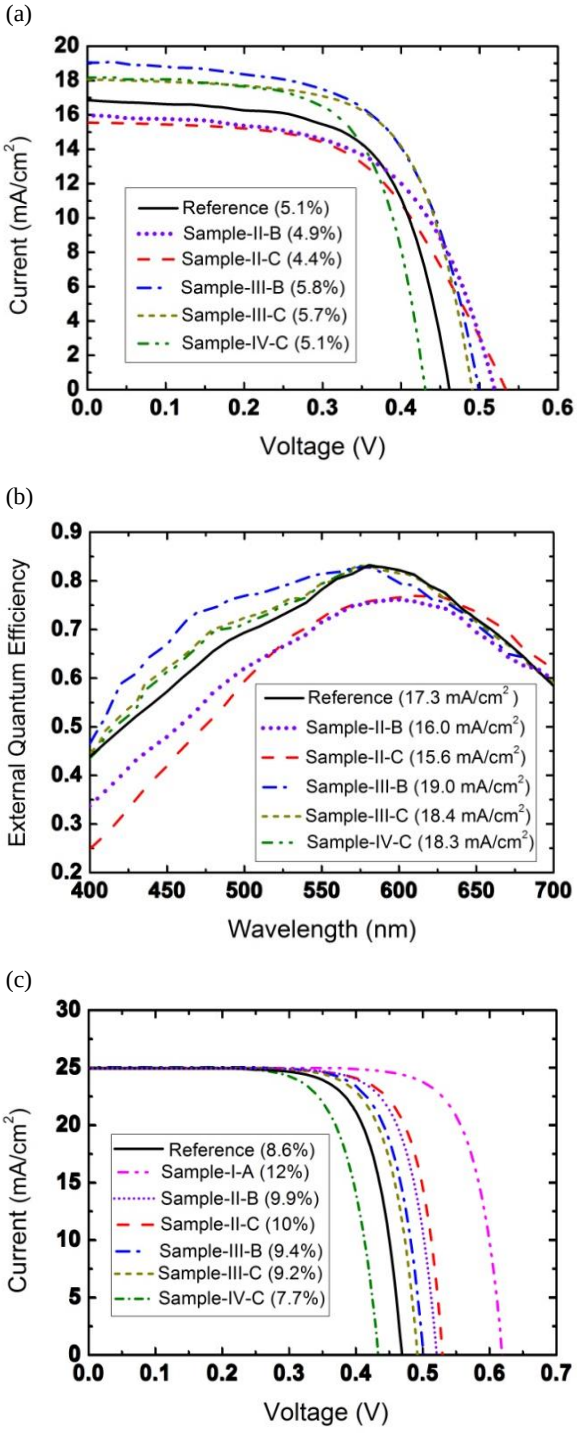


Figure 4.16: (a) Measured one-sun *I-V* curves of µc-Si:H solar cells having different types of buffer layer. The corresponding solar cell efficiency is stated in the legend. Sample-I-A is not included here because it has very poor efficiency (< 2 %). (b) Measured EQE curves of µc-Si:H solar cells having different types of buffer layer. The corresponding integrated J_{sc} values are stated in the legend (integration of the EQE curves in the 300 - 1100 nm range). For the sake of a better resolution, the EQE is only shown in the 400 - 700 nm range. (c) Pseudo *I-V* curves (from Suns-V_{oc} measurements) of µc-Si:H solar cells having different types of buffer layer. The corresponding solar cell pseudo efficiency is stated in the legend.

Table 4.3 Summary of one-sun I-V and pseudo I-V parameters of thin-film µc-Si:H solar cells having different types of buffer layer. The pseudo short-circuit current was set to 25 mA/cm^2 (corresponding to a state-of-art value for thin-film µc-Si:H solar cells).

	Ref	**I-A**	**II-B**	**II-C**	**III-B**	**III-C**	**IV-C**
***Eff* (%)**	5.1	1.4	4.9	4.4	5.8	5.7	5.1
V_{oc} (mV)	463	625	525	533	500	495	431
J_{sc} (mA/cm^2)	17.3	14.8	16	15.6	19	18.4	18.3
***FF* (%)**	64.0	15.0	58.5	53.5	61.2	63.0	65.2
R_s (Ωcm^2)	3.6	135	6.6	7.4	4.0	3.8	3.2
R_{sh} (Ωcm^2)	390	19	430	400	360	380	330
***pEff* (%)**	8.6	12.0	9.9	10.0	9.4	9.2	7.7
***1-Sun* V_{oc} (mV)**	468	621	522	530	502	492	432
***1-Sun* J_{sc} (mA/cm^2) (assumed)**	25.0	25.0	25.0	25.0	25.0	25.0	25.0
***pFF* (%)**	73.6	77.2	75.6	75.7	74.7	74.4	71.4

However, the J_{sc} values are also significantly impacted by the buffer layers, with highly crystallized buffer layers, or amorphous buffer layers containing percolating µc-Si:H grains, showing the highest J_{sc}. To evaluate the influence on the J_{sc}, the cells with different buffer layers were compared using *I-V* curves as well as using EQE curves (in the visible range), see Figure 4.16(a) and (b). This comparison gives the following ranking for J_{sc}:

$$\text{Type-III} \geq \text{Type-IV} > \text{Ref} > \text{Type-II} \qquad (\text{for } J_{sc}) \qquad (4.3)$$

The cells with Type-III and Type-IV buffer layers have a higher J_{sc} than the reference cell. The cells with Type-II buffer layer have a lower J_{sc} than the reference,

because Type-II buffer layers lost the μc-Si:H percolation path, which is necessary for carrier transport and collection.

Furthermore, the EQE curves confirmed the one-sun *I-V* measured results regarding the J_{sc}. EQE curves, see Figure 4.16(b), show that the buffer layers containing enough crystalline material (*i.e.* Type-III and Type-IV) improve the blue response. In particular, when the Type-III buffer layer was fabricated under the transition region just before the thick incubation layer appeared, the highest blue responses were obtained. In summary, the cells with an amorphous-rich Type-II buffer layer have a lower EQE (or J_{sc}) compared to the reference cells, while cells with a Type-III or Type-IV buffer layer have a higher EQE (or J_{sc}) compared to the reference cells. Thus, the EQE curves follow the same ranking as was previously observed for the J_{sc} of the solar cells:

$$\text{Type-III} \geq \text{Type-IV} > \text{Ref} > \text{Type-II} \qquad \text{(for EQE)} \qquad (4.4)$$

In order to enhance the EQE (and the J_{sc}), it seems necessary to include sufficient μc-Si:H to be at least above the percolation threshold.

The results for *FF* have a very similar trend as the EQE (and J_{sc}) in relation to the different types of buffer layer, as shown in Eqn. (4.5). In general, the buffer layers containing more of the amorphous phase will lead to a higher series resistance in the solar cells and therefore a poorer *FF*. The crystalline phase in the film has a benefit for the carrier transport. A sufficient amount of the crystalline phase is needed to form percolation paths and improve the *FF*.

$$\text{Type-IV} \geq \text{Ref} > \text{Type-III} > \text{Type-II} \qquad \text{(for } FF\text{)} \qquad (4.5)$$

Suns-V_{oc} was also used for the comparison of the cells with different buffer layers, see Figure 4.16(c) and Table 4.3. Suns-V_{oc} measurements are not influenced by the series resistance (R_s) and the 1-sun J_{sc} ('pseudo J_{sc}') is set to a reasonable value for

the device under test (in this thesis, the pseudo J_{sc} was set to 25 mA/cm^2). Basically, Suns-V_{oc} measurements show the 'pure *FF*' of the diode (without the effect of R_s).

The 1-Sun open-circuit voltages V_{oc} from the Suns-V_{oc} measurements are close to the V_{oc} values of the corresponding 1-Sun I-V measurements, see Table 4.3. The slight differences ($\leq$ 5 mV) between the two measurements are very likely due to small differences in the device temperature (note that the used Suns-V_{oc} tester does not have a temperature-controlled chuck, in contrast to the 1-Sun I-V tester). Thus, the more amorphous material there is in the buffer layer, the higher the 1-Sun V_{oc}:

$$\text{Type-I} > \text{Type-II} > \text{Type-III} > \text{Ref} > \text{Type-IV} \quad (\text{for the 1-Sun } V_{oc}) \qquad (4.6)$$

The pseudo *FF (pF*F) is also impacted by the buffer layer. A higher µc-Si:H content in the buffer layer will cause a lower *pFF*, see Table 4.3. Thus:

$$\text{Type-I} > \text{Type-II} > \text{Type-III} > \text{Ref} > \text{Type-IV} \quad (\text{for } pFF) \qquad (4.7)$$

Summing up the above comparison, there is a contrary trend of V_{oc} and J_{sc} as well as *FF* in regards to the crystallinity. Specifically, with increasing µc-Si:H content in the buffer layer the V_{oc} will drop, but J_{sc} and *FF* will improve. As a result, it is expected that an intermediate type of buffer layer (i.e. Type-II or Type-III) will give the best PV efficiency. Furthermore, it is more likely that the best candidate will be a Type-III buffer layer at the onset of µc-Si:H percolation, as this will increase J_{sc} significantly whereas V_{oc} can still be at a relatively high level. This expected behaviour has indeed been observed experimentally, since the cells with Type-III buffer layer exhibit the highest efficiencies. An independent thickness optimization for the Type-I buffer layer is necessary to fully confirm this hypothesis. However, using numerical simulations this result is (at least theoretically) confirmed, as described in the next chapter.

4.6 Summary

An experimental investigation of the impact of different types of buffer layers on μc-Si:H thin-film solar cells was made in this chapter. One-Sun solar cell parameters (i.e. open-circuit voltage, short-circuit current and fill factor) of various μc-Si:H cells with inserted buffer layer at the p/i interface were compared to the reference case, i.e. a cell without a buffer layer. The various buffer layers processed were classified into 4 categories, i.e. purely amorphous, amorphous with isolated μc-Si:H grains, amorphous with percolating μc-Si:H grains, and purely μc-Si:H. Three different methods to process these buffer layers were investigated. XTEM images showed the real situations for the structural composition at the p/i interface when using different deposition methods to produce the buffer layer. By analysing and comparing the results of 1-Sun I-V parameters (V_{oc}, J_{sc}, *FF* and *Eff*), EQE curves (in the 400 – 700 nm range) and Suns-V_{oc} curves (1-Sun V_{oc} and *pFF*), it was shown that the Type-III buffer layer containing μc-Si:H percolation paths in the amorphous matrix and processed with Method B (transition region deposition) gave the highest PV efficiency enhancement.

Chapter 5: Theoretical investigation of the impact of different types of buffer layers at the p/i interface of thin-film µc-Si:H solar cells on the solar cell performance

5.1 Requirements for the buffer layers

The quality of the p/i interface plays a critical role for the efficiency of µc-Si:H thin-film solar cells (in the p-i-n superstrate configuration), necessitating a careful optimization. The introduction of a buffer layer at the interface is one of the methods to reach this goal. In order to improve the performance of the solar cells, there are some requirements for the buffer layers used at the interface:

① Interface defect passivation:

The inserted buffer layer should help to reduce the recombination rate near the interface. For this, the material used as buffer layer should have either a low defect density and/or a large bandgap and/or a large interface charge (thus enhancing the field effect passivation; not discussed in this thesis).

② Band alignment:

In order to facilitate the carrier collection, the band alignment is a crucial factor that must be taken into consideration. For example, when a heterostructure is formed at the interface, the existence of band offset between the two materials can prevent the minority carriers to reach the contact (which decreases the recombination rate at this region) but on the other hand may also block the majority carriers and weaken the carrier collection (because of a high effective barrier height). Ideally, at each contact,

there is only one band offset blocking the minorities, but no band offset blocking the majorities from reaching the metal contact.

③ Conductivity:

In order to reduce the series resistance of the solar cells, a high conductivity for the buffer layer is needed. The a-Si:H and μc-Si:H buffer layers with low crystallinity are resistive and the buffer layer thickness should thus be as thin as possible. For buffer layers with μc-Si:H percolation paths inside them, this condition is less strict because of the improved carrier mobility (which is as good as in the μc-Si:H layer with high crystallinity).

Based on the requirements discussed above, three different types of buffer layers will be modelled, i.e. (1) an a-Si:H buffer layer, i.e. the Type-I buffer layer investigated in Chapter 4, (2) a highly crystallized μc-Si:H buffer layer, i.e. the Type-IV buffer layer investigated in Chapter 4, and (3) an a-Si:H buffer layer with percolated μc-Si:H grains, i.e. the Type-III buffer layer investigated in Chapter 4. A systematic investigation of the buffer layer properties will be carried out for each type of buffer layer, and their impact on the *I-V* performance of μc-Si:H solar cells will be investigated by means of numerical computer simulation.

5.2 Modelling of silicon thin-film layers and of a reference thin-film μc-Si:H solar cell (without using a buffer layer)

5.2.1 Overview of silicon thin-film layer modelling

Figure 5.1 shows the defect density distribution for a μc-Si:H (a) *i*-layer, (b) *p*-layer, (c) *n*-layer, as used in the numerical model. As discussed in Chapter 4, the

intrinsic µc-Si:H film with crystallinity of 50 - 60 % is used as absorber layer for device fabrication. It has been reported that the mobility gap E_g of the intrinsic layer in a p-i-n device is estimated to be around 1.18 eV and this value is widely used in many numerical simulations [43]. Because of the existence of the impurities (i.e. O, N) in the film serving as donor states within the bandgap, the Fermi level (E_F) of the undoped µc-Si:H is not located at the midgap; instead, it is above midgap, making the layer behave like *n*-type [136].

Because of the disordered structure in the a-Si:H phase, band tails exist at the edge of both the valence band and the conduction band, as shown in Figure 5.1. The defect density within these band tails extends towards midgap and drops exponentially. At the same time, dangling bonds in the a-Si:H form midgap states, modelled by two Gaussian distributions within the bandgap. Furthermore, for µc-Si:H - especially for highly crystallized layers - the grain boundaries are assumed to contain a higher density of dangling bonds (N_{DB}) due to the plasma etching, which makes a µc-Si:H layer even more defective than an a-Si:H layer [87]. In this case, the mainly dangling bond dominated defect density of a highly crystallized µc-Si:H Type-IV buffer layer, as classified in Chapter 4, is assumed to be generally one order of magnitude higher than an a-Si:H Type-I buffer layer or Type-III buffer layer (not containing or containing some percolating µc-Si:H grains). The typical defect densities for the various buffer layers are listed in Table 5.1.

In general, dangling bond defects (recombination centres) can be positive, neutral or negative charged, if occupied by zero, one or two electrons, respectively. In this thesis they are modelled by one donor-type and one acceptor-type Shockley-Read-Hall Gaussian dangling bond distribution, as described in [32].

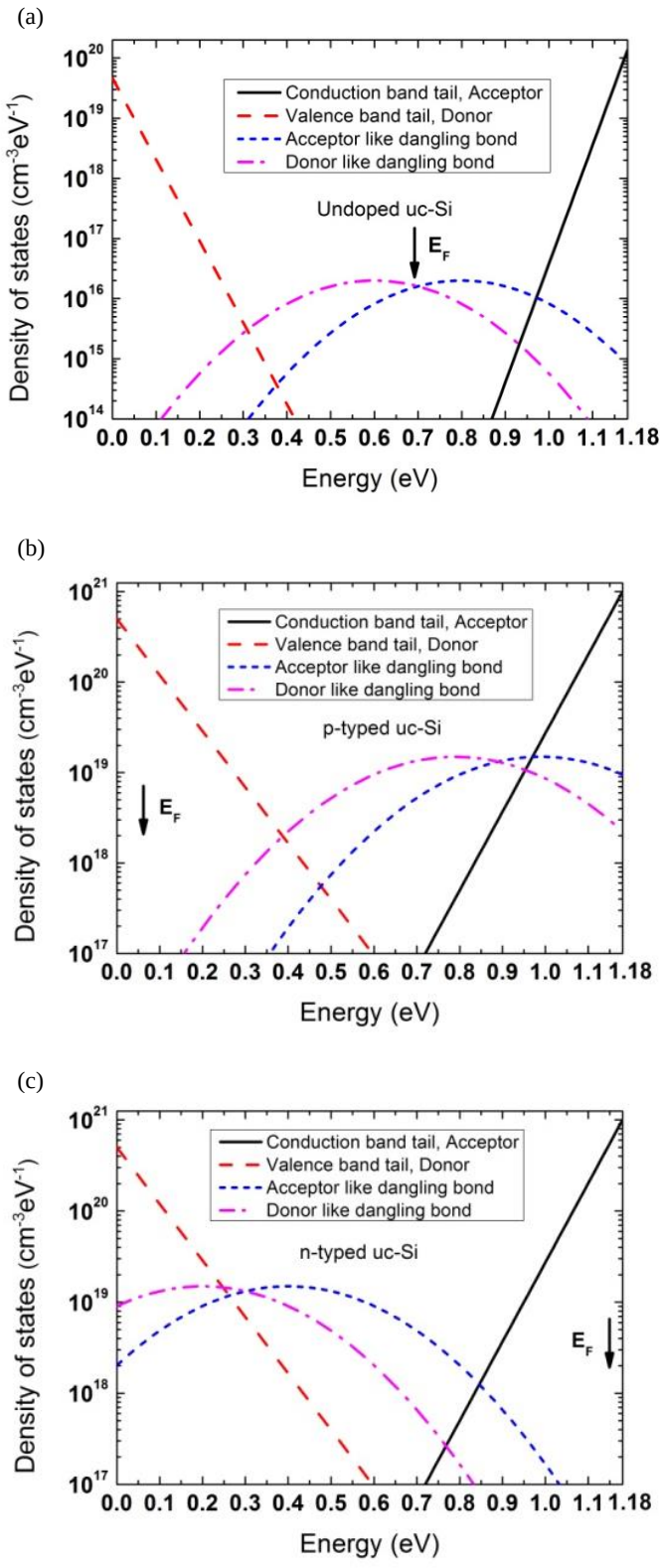


Figure 5.1: Defect density distribution used for modelling thin-film µc-Si:H layers, i.e. (a) *i*-layer, (b) *p*-layer and (c) *n*-layer, as used for modelling thin-film µc-Si:H solar cells. A positive correlation energy of 0.2 eV is assumed for modelling the donor and acceptor type Gaussian dangling bond states. E_F indicates the Fermi level position.

Table 5.1 Comparison of the selected electrical parameters for the μc-Si:H *i*-, *p*- and *n*-layer as well as the buffer layers of Type-I, III and IV. E_g is the mobility bandgap; E_F is the Fermi level measured from the valence band. μ_e and μ_h are the electron mobility in conduction band and hole mobility in the valence band, respectively. E_{char} is the characteristic energy defining the exponential slope of the tail states; N_{DB} is the concentration of the dangling bonds; σ_{DB} is the standard deviation of the Gaussian dangling bond distribution.

	μc-Si i-layer	**μc-Si p-layer**	**μc-Si n-layer**	**Type-I**	**Type-III**	**Type-IV**
E_g (eV)	1.18	1.18	1.18	1.80	1.50	1.10
E_F (eV)	0.69	0.06	1.15	1.0	0.85	0.66
μ_e (cm^2/Vs)	25	25	25	6	25	50
μ_h (cm^2/Vs)	5	5	5	2	5	10
Conduction band tails						
E_{char} (eV)	0.022	0.05	0.05	0.03	0.03	0.025
Valence band tails						
E_{char} (eV)	0.032	0.07	0.07	0.05	0.05	0.035
Dangling bonds						
N_{DB} (cm^{-3})	7.5×10^{15}	7.5×10^{18}	7.5×10^{18}	5×10^{15}	5×10^{15}	5×10^{16}
σ_{DB} (eV)	0.15	0.20	0.20	0.15	0.15	0.15

The defect distribution is expected to be very broad and the standard deviation of the Gaussian function is set to 150 meV. The neutral/positive defect peak (donor like dangling bonds) is located in the middle of the bandgap. The negative/neutral defect peek (acceptor like dangling bonds) is located above the neutral/positive defect peek, shifted by a positive correlation energy of 0.2 eV. In addition, the capture cross section of neutral states (σ_{neut}) are assumed to be 10^{-16} cm^2, whereas the capture cross section of charged states are assumed to be 10^{-15} cm^2. The main parameters describing the various μc-Si:H layers of a thin-film μc-Si:H solar cell as well as the various buffer layers are listed in Table 5.1. All other simulated parameters can be found in Appendix C, most of which are cited from Refs [32, 137, 138].

In order to push the Fermi level to the band edge, dopant atoms must be added and a high doping concentration is needed. To form a *p*-type doped layer, diborane (B_2H_6) is added into the SiH_4 and H_2 mixed gases. But at the same time, an increasing doping concentration will cause a higher defect density in the film. As a result, the conduction and valence band tails will further extend towards the midgap and have a

shallow slope (*i.e.* larger E_{char} values, or Urbach energies, as listed in Table 5.1) as compared to undoped films. At the same time, the density of the dangling bonds increases significantly (7.5×10^{18} cm^{-3} as compared to 7.5×10^{15} cm^{-3} for µc-Si:H *i*-layer) and the Gaussian peaks shift towards higher magnitude and conduction band edge for *p*-layer. When the doping concentration reaches about 10^{19} cm^{-3}, the activation energy of the *p*-layer can reach about 60 meV, as shown in Figure 5.1(b).

To form *n*-type doped layers, phosphine (PH_3) is added into the SiH_4 and H_2 mixed gases and it pushes the Fermi level towards the conduction band edge. When the doping concentration reaches 5×10^{19} cm^{-3}, the activation energy of the µc-Si:H n-layer can reach about 30 meV, as shown in Figure 5.1(c). Similar to the heavily doped *p*-layer, the conduction and valence band tails further extend towards to midgap and the Gaussian peaks of the midgap states shift to higher magnitude and closer to the valence band edge.

The different density distributions of the intrinsic and doped µc-Si:H layers are pictured in Figure 5.1. The corresponding main simulation parameters are compiled in Table 5.1. The different defect distributions will cause these layers to display different electrical properties. In the following sections, a detailed investigation of the electrical properties for each layer will be carried out.

5.2.2 Modelling of the intrinsic µc-Si:H absorber layer (*i*-layer)

In this section, an investigation of the correlation between the generation current (or generation rate G), quasi Fermi level splitting ΔE_F, minority carrier lifetime τ, and diffusion length (effective diffusion length L_{diff} and drift length L_{drif}) of the µc-Si:H *i*-layer will be carried out. It starts with the determination of the correlation between the generation rate G (which is equal to total recombination rate U under equilibrium

condition) and the excess carrier density Δn, based on the Shockley-Read-Hall (SRH) recombination statistics [139-141]. As a result, the lifetime τ, the quasi Fermi energy splitting ΔE_F, and the diffusion lengths L_{diff} and L_{drif} can be obtained accordingly. The calculation process is as follows:

First, the total recombination rate U is determined by the defect state distribution within the bandgap of the materials. The defect distribution (see Figure 5.1) for the μc-Si:H films can be described as D_1 (conduction band tail state, acceptor), D_2 (valence band tail state, donor), D_3 (acceptor-like dangling bond), and D_4 (donor-like dangling bond):

$$D_1(E) = N_{T,A} \exp\left[\frac{E-E_c}{E_{char,A}}\right]; \quad (5.1) \qquad D_2(E) = N_{T,D} \exp\left[\frac{E_v-E}{E_{char,D}}\right]; \quad (5.2)$$

$$D_3(E) = \frac{N_{DB}}{\sigma_{DB}\sqrt{2\pi}} \exp\left[-\frac{(E-E_{DB}^A)^2}{2\sigma_{DB}^2}\right]; \quad (5.3) \qquad D_4(E) = \frac{N_{DB}}{\sigma_{DB}\sqrt{2\pi}} \exp\left[-\frac{(E-E_{DB}^D)^2}{2\sigma_{DB}^2}\right]; \quad (5.4)$$

where $N_{T,A}$ and $N_{T,D}$ are the conduction and valence band edge densities; E_{char} is the tail characteristic energy; E_{DB}^A and E_{DB}^D are the peak locations for the acceptor-like and donor-like dangling bonds. σ_{DB} is the standard deviation of the Gaussian dangling bond distribution. All these parameter values are listed in Appendix C.

According to the SRH theory, the SRH recombination rate $U(E_d)$ for a continuous distribution of defects at the defect energy E_d can be expressed as:

$$U(E_d) = \frac{D(E_d)(np-n_i^2)}{\frac{n+N_C e^{-\beta(E_C-E_d)}}{\gamma_{th,h}\sigma_h} + \frac{p+N_V e^{-\beta(E_v-E_d)}}{\gamma_{th,e}\sigma_e}}; \quad (5.5)$$

where N_C and N_V are the effective density of states in the conduction and valence band; n and p are the electron and hole concentration; n_i is the intrinsic carrier concentration; $\gamma_{th,e}$ and $\gamma_{th,h}$ are the thermal velocities for electrons and holes; σ_e and σ_h are the capture cross sections for electrons and holes. β is defined as 1/kT (T is the absolute temperature and k is Boltzmann's constant).

Therefore, the recombination rates for the above four types of defects (i.e. U_1, U_2, U_3 and U_4) can be defined by integrating over the energy levels from the valence band to the conduction band. Furthermore, the total recombination rate U is equal to the sum of the recombination rate resulting from the above four types of defects. It can be expressed as:

$$U = U_1 + U_1 + U_1 + U_1 \; ; \tag{5.6}$$

The electron and hole concentrations (n and p) are defined as:

$$\mathrm{n} = \mathrm{n_0} + \Delta\mathrm{n}; \tag{5.7}$$

$$\mathrm{p} = \mathrm{p_0} + \Delta\mathrm{p}; \tag{5.8}$$

where n_0 and p_0 are the electron and hole densities under dark equilibrium condition; Δn and Δp are the excess carrier densities, which can be assumed to be equal under field-free conditions.

$$\Delta\mathrm{n} = \Delta\mathrm{p}; \tag{5.9}$$

Furthermore, under steady-state illumination and open-circuit condition, the generation rate G should be equal to the total recombination rate U:

$$\mathrm{G} = \mathrm{U}; \tag{5.10}$$

Based on the equations from (5.1) to (5.10), a correlation between generation rate G and excess carrier density Δn can be built up under open-circuit conditions. 'Wolfram Mathematica 9' was used to solve the above equation sets and determine the value of Δn for a given G. As a result, the minority carrier lifetime can be obtained as:

$$\tau = \frac{\Delta n}{G} = \frac{\Delta n}{U}; \tag{5.11}$$

Furthermore, the quasi Fermi level splitting can be obtained from [142]

$$\Delta E_F = \frac{kT}{q}\ln\left(\frac{np}{n_i^2}\right) = \frac{kT}{q}\ln\left(\frac{(n_o+\Delta n)(p_o+\Delta n)}{n_i^2}\right); \quad (5.12)$$

and the effective minority carrier diffusion length L_{diff} can be expressed as

$$L_{diff} = \sqrt{\frac{kT}{q}\mu\tau}\ ; \quad (5.13)$$

where μ is the effective carrier mobility.

A step-by-step calculation process and more details are given in Appendix D.

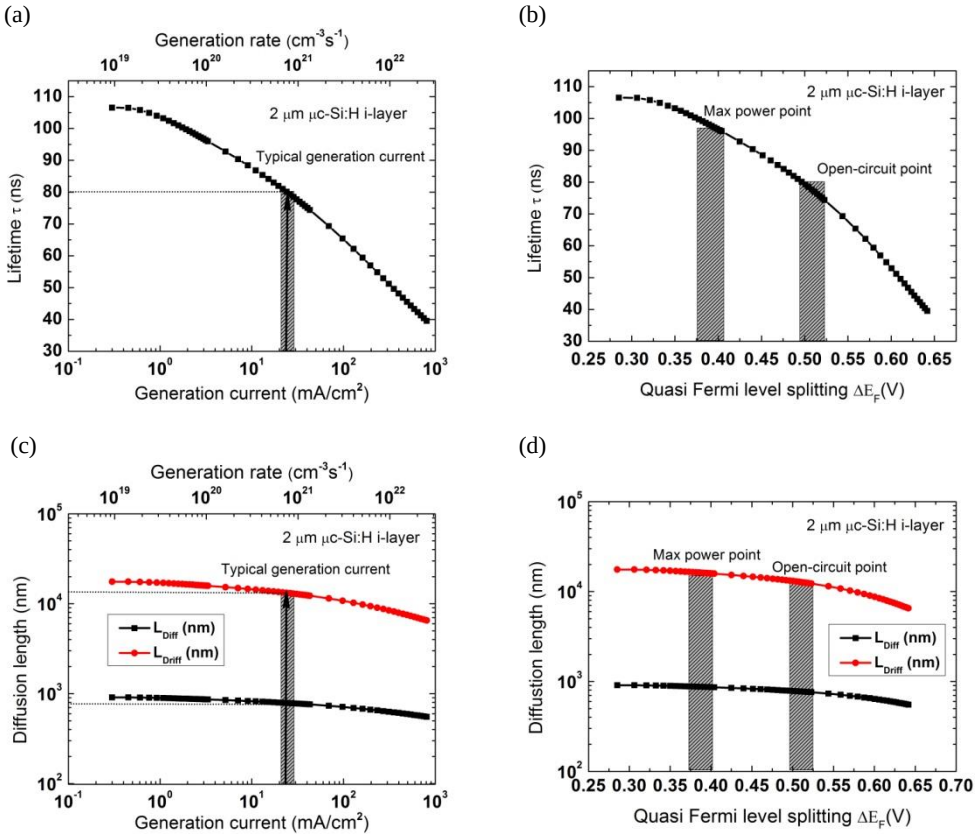


Figure 5.2: (Top) Simulated minority carrier lifetime τ of a μc-Si:H i-layer (a) versus generation current (or generation rate) within a 2 μm thick solar cell absorber film, (b) versus the quasi Fermi level splitting ΔE_F; (Bottom) simulated diffusion length L_{diff} and drift length L_{drif} of a μc-Si:H i-layer (c) versus generation current (or generation rate) within a 2 μm thick solar cell absorber film, (d) versus quasi Fermi level splitting ΔE_F. The typical ranges of generation currents or quasi Fermi energy splittings of μc-Si:H solar cells are also indicated.

Based on the above calculations, the relationships between τ, L_{diff}, G and ΔE_F can be determined, see Figure 5.2. As can be seen, the minority carrier lifetime and the effective diffusion length decrease as the generation rate increases. It is attributed to the fact that the total recombination rate in the film becomes higher (U = G). Furthermore, if we assume that the generation rate is constant over the film thickness L (*i.e.* 2 µm), a generation current I_G can be estimated from:

$$I_G = \int_0^L G(x) q dx = 1.6 \times 10^{-19} \times G \times L; \quad (5.14)$$

In general, by using proper light trapping technologies, the obtained short-circuit current under 1-Sun condition ranges from 20 to 30 mA/cm^2 for µc-Si:H cells, which is equal to a generation rate ranging from 6.25×10^{20} to 9.375×10^{20} cm^{-3}s^{-1} within a 2 µm thick film. This range is highlighted by the shaded area in Figure 5.2(a) and (c). Its corresponding open-circuit voltage and maximum power point are highlighted in Figure 5.2(b) and (d), respectively. Furthermore, in this study an intermediate short-circuit current value of 24 mA/cm^2, which has experimentally been achieved by a number of research groups, was selected as a reference for the simulation and highlighted by an arrow in Figure 5.2(a) and (c).

Table 5.2 Corresponding electrical parameters of an intrinsic µc-Si:H layer for a given thickness L (i.e. 1 µm and 2 µm) to generate a short-circuit current of 24 mA/cm^2.

L (µm)	**G (cm^{-3}s^{-1})**	**Δn (cm^{-3})**	**ΔE_F (V)**	**τ (ns)**	**L_{diff} (µm)**	**L_{drif} (µm)**	**L_{drif}/L**
1	1.5×10^{21}	9.39×10^{13}	0.5196	75.15	0.726	24.79	25.0
2	7.5×10^{20}	6.0×10^{13}	0.4967	80.07	0.7872	13.21	6.6

Table 5.2 lists the extracted parameters from Figure 5.2. If a short-circuit current of 24 mA/cm^2 is generated by using a 2 µm thick µc-Si:H film, the generation rate is equal to 7.5×10^{20} cm^{-3}s^{-1}.

From Figure 5.2(a), the lifetime τ can be estimated to be about 80 ns. Next, the quasi Fermi level splitting (about 0.5 V) can be obtained from Figure 5.2(b). Finally, the diffusion length L_{diff} can also be obtained from Figure 5.2(c) or (d), giving about 800 nm in this case. The same rule can be applied to the case when L is varied (*i.e.* 1 μm, as also listed in Table 5.2). As can be seen, if the same current can be generated by using a thinner film (*i.e.* 1 μm vs. 2 μm), it causes a higher ΔE_F and thus a higher V_{oc} can be obtained. This emphasizes the importance of having a light trapping scheme.

Furthermore, it should be emphasized that the diffusion length L_{diff} is even shorter than the film thickness L. It is attributed to the high defect density and short minority carrier lifetime in the μc-Si:H film. In μc-Si:H thin-film solar cells, the band bending due to the band alignment between the two terminals (*p*- and *n*-layer) causes a strong internal electrical field (*E*) within the absorber layer. This internal electrical field helps the carriers to drift across the absorber layer, called 'drift-assisted transport'. As a result, the 'effective diffusion length' can be re-defined as "drift length' (L_{drif}) and determined as:

$$L_{drif} = \mu\tau E \approx \mu\tau \frac{V_{bi}}{L}; \tag{5.15}$$

where V_{bi} is the built-in potential, estimated around 1.1 V for μc-Si:H solar cells from $V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{p_0 n_0}\right)$, μ is the carrier mobility and τ is the lifetime obtained from the above calculation. As shown in Figure 5.2 and listed in Table 5.2, the L_{drif} is much longer than the absorber layer thickness L.

Furthermore, it was reported that the high ratio of L_{drif} /L indicates a good carrier collection efficiency, which can be directly reflected from the improved fill factor *FF* [143]. More details and discussions on the L_{drif} /L ratio and the carrier collection efficiency can be found in the literature [143, 144].

5.2.3 Modelling of the boron-doped µc-Si:H hole-collecting layer (p-layer)

Applying the same calculation process to doped µc-Si:H layers, the impact of the generation rate and quasi Fermi level splitting on the minority lifetime and diffusion length can be obtained. The results are shown in Figure 5.3.

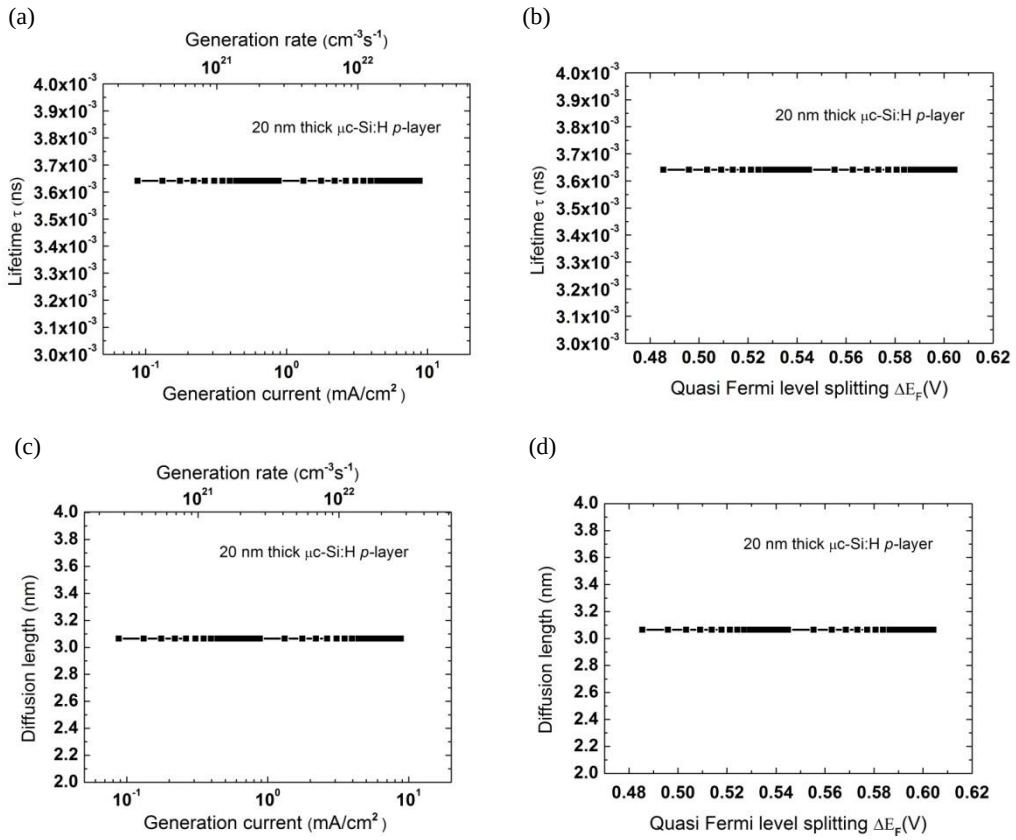


Figure 5.3: (Top) Simulated lifetime τ of a µc-Si:H *p*-layer (a) versus the generation current (or generation rate) within a 20 nm thick film, (b) versus the quasi Fermi level splitting ΔE_F; (Bottom) Simulated diffusion length L_{diff} of a µc-Si:H *p*-layer (c) versus the generation current (or generation rate) within a 20 nm thick film, (d) versus the quasi Fermi level splitting ΔE_F.

For the µc-Si *p*-layer, the minority carrier lifetime and diffusion length are both independent of the generation rate and the quasi Fermi level splitting. The lifetime is fixed at around 3.65×10^{-3} ms and the diffusion length is fixed at around 3.1 nm for a heavily doped *p*-layer. It can be attributed to the fact that the electron carrier concentration ($n_o \approx N_D$, where N_D is the doping concentration) is much higher than the excess carrier density Δn in the heavily doped *p*-layer. As a result, the recombination rate U

(U = G at V_{oc}) and excess carrier density Δn have a nearly linear relation in the SRH equation (5.5). It causes a constant τ value (since τ is the ratio between Δn and G). In this case, the minority carrier lifetime and diffusion length are not impacted by the generation rate or quasi Fermi level splitting but the total defect density determined by the doping concentration. On the other hand, as can be seen from the above results, the minority carrier lifetime and diffusion length of the doped μc-Si:H layer decrease significantly due to the very high defect density (nearly three orders of magnitude higher than for the undoped layer). Therefore, doped layers are not suitable to be used as absorber layer for solar cells.

5.2.4 Modelling of the phosphorus-doped μc-Si:H electron-collecting layer (*n*-layer)

As in the case of the *p*-layer, the minority carrier lifetime and diffusion length of the *n*-layer are also independent on the generation rate and quasi Fermi level splitting (the data were similar to the case for the *p*-layer and are thus not shown here). But because of the higher doping concentration than the *p*-layer, the lifetime and diffusion length further reduce to about 2.5×10^{-3} ns and 2.5 nm, respectively.

5.2.5 Modelling of the reference thin-film μc-Si:H solar cell (no buffer layer)

Based on the above electrical parameters for each layer (more details see Appendix C), a one-dimensional numerical device simulator called "Advanced Semiconductor Analysis" (ASA) and developed by Delft University, was used to simulate μc-Si:H thin-film solar cells without using a buffer layer.

A corresponding band diagram under dark equilibrium condition for μc-Si:H thin-film solar cells having a typical p-i-n structure is shown in Figure 5.4(a). The

depletion region created by the two doped layers spreads across the whole i-layer and a strong internal electrical field is formed within the i-layer (resulting from the band bending). As a result, the photogenerated electron-hole pairs are separated by this electrical field and driven to *p*-layer (hole collector) and *n*-layer (electron collector), respectively.

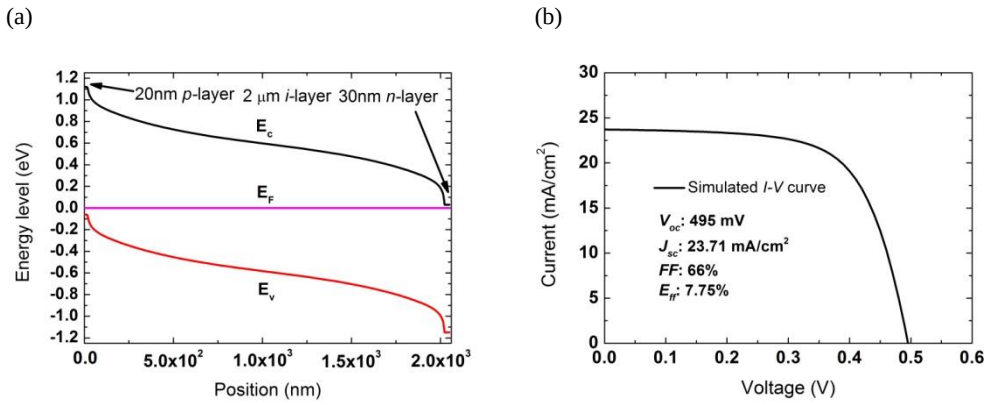


Figure 5.4: (a) Schematic of band diagram under dark equilibrium condition for μc-Si:H thin-film solar cell (reference, no buffer layer) having a p-i-n structure. (b) Simulated *I-V* curve for a reference μc-Si:H thin-film solar cell (no buffer layer) based on the electrical parameters for each layer listed in Appendix C.

Under illumination, a constant generation rate of 7.32×10^{20} $cm^{-3}s^{-1}$ was assumed, corresponding to a photogeneration current of 24 mA cm^{-2} within the μc-Si:H solar cell. That is, considering photon absorption within a 2 μm thick intrinsic μc-Si:H absorber layer (i-layer), a 20 nm thick *p*-layer and a 30 nm *n*-layer, the generation rate G was calculated according to $G = \frac{24\ mA/cm^2}{1.6\times10^{-19}C\times(2000+20+30)\times10^{-7}cm}$.

A PV efficiency of 7.75 % is obtained for the μc-Si:H thin-film reference solar cell, without any buffer layer. The simulated *I-V* curve and the corresponding solar cell parameters (efficiency, open-circuit voltage, short-circuit current and fill factor) are shown in Figure 5.4(b). They will be used as reference parameters within the subsequent study.

5.3 Modelling of buffer layers

In this section, a theoretical investigation of different types of buffer layers will be carried out. A Type-I (a-Si:H) and a Type-IV (highly crystallized µc-Si:H) buffer layer, which are considered as the two "extreme" cases, are investigated first. They are followed by the investigation of a Type-III (a-Si:H with percolated µc-Si:H grains) buffer layer, which is considered as an intermediate state between the former two buffer layers, and which has been proven experimentally to give the highest efficiency enhancement if being introduced at the p/i interface of a µc-Si:H thin-film solar cell (see Chapter 4). Similar to the previous study for the µc-Si:H *i*-layer and for the doped µc-Si:H layers, the defect distributions within the buffer layer will be described first. Next, based on the SRH theory, the interconnection between the minority carrier lifetime, diffusion length, generation rate, and quasi Fermi level splitting for these buffer layers will be discussed. Finally, in order to compare these buffer layers, it is assumed that they are illuminated under the same condition, i.e. at a constant generation rate of $7.5\times10^{20}\,cm^{-3}s^{-1}$ (corresponding to a photogeneration current of 24 mA cm^{-2} within the µc-Si:H thin-film solar cell, assuming an additional 10 nm thick buffer layer).

5.3.1 Overview of buffer layer modelling

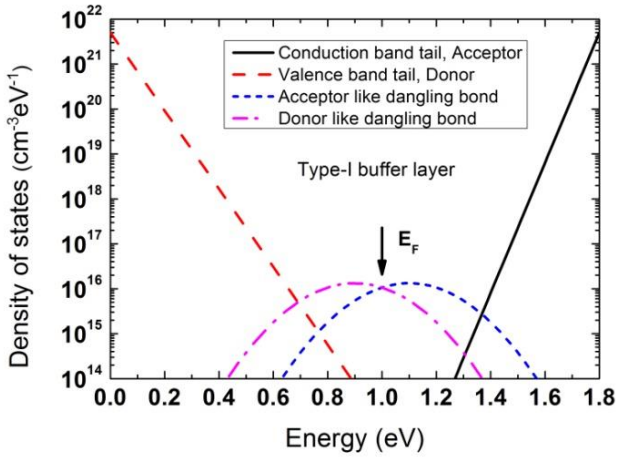
As compared to a lightly crystallized µc-Si:H *i*-layer used as a solar cell absorber layer, a fully crystallized Type-IV µc-Si:H buffer layer is assumed to have a slightly lower bandgap (i.e. 1.1 eV compared to 1.2 eV), see Table 5.3, in accordance to [43, 145]. Contrary, as compared to a µc-Si:H *i*-layer used as a solar cell absorber layer, a Type-I a-Si:H buffer layer has a much larger bandgap (i.e. E_g =1.8 eV compared to 1.2 eV). Furthermore it has a shallower slope of the conduction band and valence

band tails (i.e. a larger characteristic energy E_{char}, also called Urbach energy) as shown in Figure 5.5(a). However, the defect distribution of midgap states (dangling bonds) is also comparatively broad and thus the standard deviation of the Gaussian function is set to 150 meV as well, see Table 5.1. Besides, the Fermi level locates slightly above mid gap because of the stated impurity distribution and thus the undoped (intrinsic) a-Si:H behaves like a slightly n-typed layer.

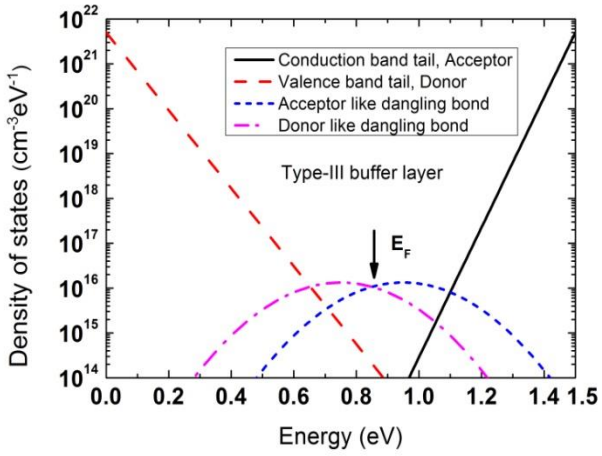
The Type-III (a-Si:H with percolated μc-Si:H grains) buffer layer can be considered in a first approximation as the intermediate state between a Type-I (a-Si:H) and a Type-IV (μc-Si:H) buffer layer. Its defect distribution can still be assumed to be the same as the Type-I buffer layer (still consisting mainly of a-Si:H), however the effective bandgap shrinks (i.e. to 1.5 eV, like observed in [41]), see Table 5.3 and illustrated in Figure 5.5(b). Furthermore, the μc-Si:H percolation paths contained in the Type-IV buffer layer improve the carrier mobility as compared to the Type-I buffer layer, as also listed in Table 5.3.

Type-IV buffer layers have a very high crystallinity (close to, or even above, 70 %). They contain a large amount of grain boundaries and, therefore, a very high defect density (*i.e.* dangling bonds). In the numerical simulation, the density of the dangling bonds N_{DB} for the Type-IV buffer layer was set to 5.0×10^{16} cm^{-3}, which is one order of magnitude higher than the Type-I buffer layer (a-Si:H layer) and as shown in Figure 5.5 and listed in Table 5.3. In addition, the high crystallinity also causes a bandgap shrinking to 1.1 eV as compared to the Type-I a-Si:H buffer layer (E_g: 1.8 eV). On the other hand, a Type-IV buffer layer has the highest crystallinity, causing the carrier mobility to improve further (see Table 5.3) and benefiting the carrier transport. It is thus expected to reduce the series resistance of the solar cells.

(a) Type-I buffer layer



(b) Type-III buffer layer



(c) Type-IV buffer layer

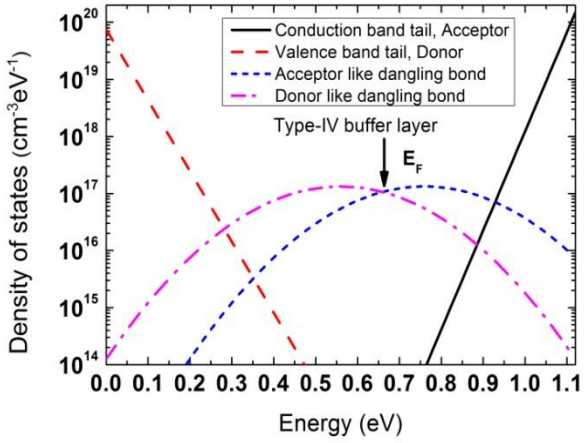


Figure 5.5: Defect density distribution for (a) a Type-I buffer layer, (b) a Type-III buffer layer and (c) a Type-IV buffer layer, as used in the numerical simulation model.

Table 5.3 Comparison of the most important electrical parameters for the different buffer layers compared to the intrinsic µc-Si:H absorber layer (i-layer) of the µc-Si:H solar cell. E_g is the mobility bandgap; ΔE_c is the conduction band offset towards the µc-Si:H absorber layer; ΔE_v is the valence band offset towards the µc-Si:H absorber layer; N_{DB} is the density of the dangling bonds; μ_e and μ_h are the electron mobility in conduction band and hole mobility in the valence band, respectively.

	µc-Si:H absorber layer	**Type-I buffer layer**	**Type-III buffer layer**	**Type-IV buffer layer**
E_g (eV)	1.2	1.8	1.5	1.1
ΔE_c (meV)	0	150	0*	0*
ΔE_v (meV)	0	470	320	-80
N_{DB} (cm^{-3})	7.5×10^{15}	5.0×10^{15}	5.0×10^{15}	5.0×10^{16}
μ_e (cm^2/Vs)	25	6	25	50
μ_h (cm^2/Vs)	5	2	5	10

* Note: The ΔE_c of Type-III and Type-IV layers is assumed to be zero for an 'extreme' case study. In reality, it should be a value in the 0 - 150 meV range.

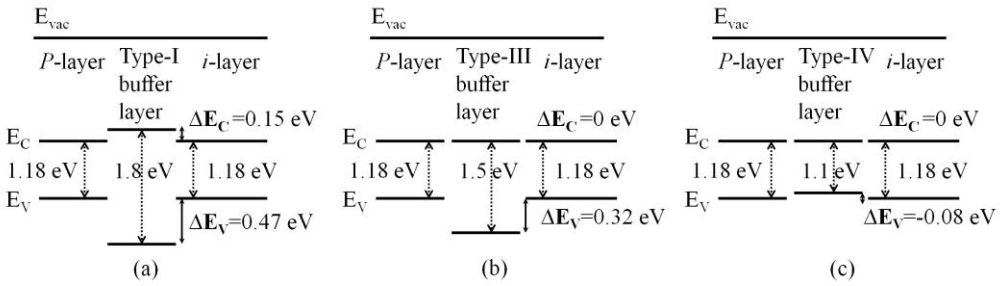


Figure 5.6: Schematic of the conduction band offset ΔE_c and valence band offset ΔE_v from different types of buffer layers (i.e. (a) Type-I (standard a-Si:H); (b) Type-III (a-Si:H layer with µc-Si:H percolation paths); and (c) Type-IV(highly crystallized µc-Si:H layer)) towards the i-layer.

In order to study the band alignment between the buffer layers and *i*-layer, the conduction and valence band offset values (ΔE_c and ΔE_v) towards the µc-Si:H absorber layer were listed in Table 5.3 and illustrated in Figure 5.6 for comparison. The a-Si:H used as Type-I buffer layer has both a conduction and a valence band offset towards the µc-Si:H *i*-layer, with the main band discontinuity appearing at the valence band side (*i.e.* $\Delta E_c = 0.15$ eV and $\Delta E_v = 0.47$ eV) [41, 42], as shown in Figure 5.6(a). It should be pointed out here that the conduction band offset of the Type-III and Type-IV buffer layers is simply assumed to be zero. This is simulating the most

'extreme' case study. In this case, the band offsets at the p/i interface don't block the minority carriers (electrons) but block the majority carriers (holes). However, in reality, ΔE_c can have any value, somewhere between 0 and 150 meV [41]. Based on this assumption, the Type-I buffer layer has the highest band offset at the valence band (470 meV), which leads to a serious blocking of the hole extraction, when introduced at the p/i interface of a µc-Si:H solar cell.

The "Advanced Semiconductor Analysis" (ASA) simulation program was used to simulate the band diagrams under dark equilibrium condition for µc-Si:H solar cells when various buffer layers were introduced at the p/i interface. In Figure 5.7(a) and (b), the band diagrams show that the introduction of a Type-I buffer layer at the p/i interface creates a conduction band offset ΔE_c as well as a valence band offset ΔE_v towards the *i*-layer. Considering the hole transport in the valence band, there will be a barrier to impede the hole collection into the hole collecting layer (*p*-layer). This energetic barrier, which is defined as the distance from the Fermi level to the valence band edge is called "effective barrier height" (Φ_B^h) [142]. Considering the electron transport in the conduction band, the ΔE_c will prevent the undesired electron back-diffusion into the *p*-layer and thus reduce the recombination rate.

Similar to a Type-I buffer layer, there is a valence band offset ΔE_v between the Type-III buffer layer and the *i*-layer, leading to an energetic barrier Φ_B^h, blocking the hole transport, as shown in Figure 5.7(c) and (d). However, this effective barrier height is now less compared to the one caused by the Type-I buffer layer.

Differently, a notch can be seen at the valence band when a Type-IV buffer layer is introduced at the p/i interface as shown in Figure 5.7(e) and (f). It is attributed to the smaller bandgap of the Type-IV buffer layer (1.1 eV) as compared to the intrinsic µc-Si:H absorber layer (1.18 eV). Now, the valence band offset from the Type-IV buffer layer towards the *i*-layer (ΔE_V = -80 meV) does not block the hole transport.

Instead, there is a small barrier height Φ_B^h between the *p*-layer and the Type-IV buffer layer at the valence band, as indicated in Figure 5.7(f). The impact of the effective barrier height will be further discussed in the following sections.

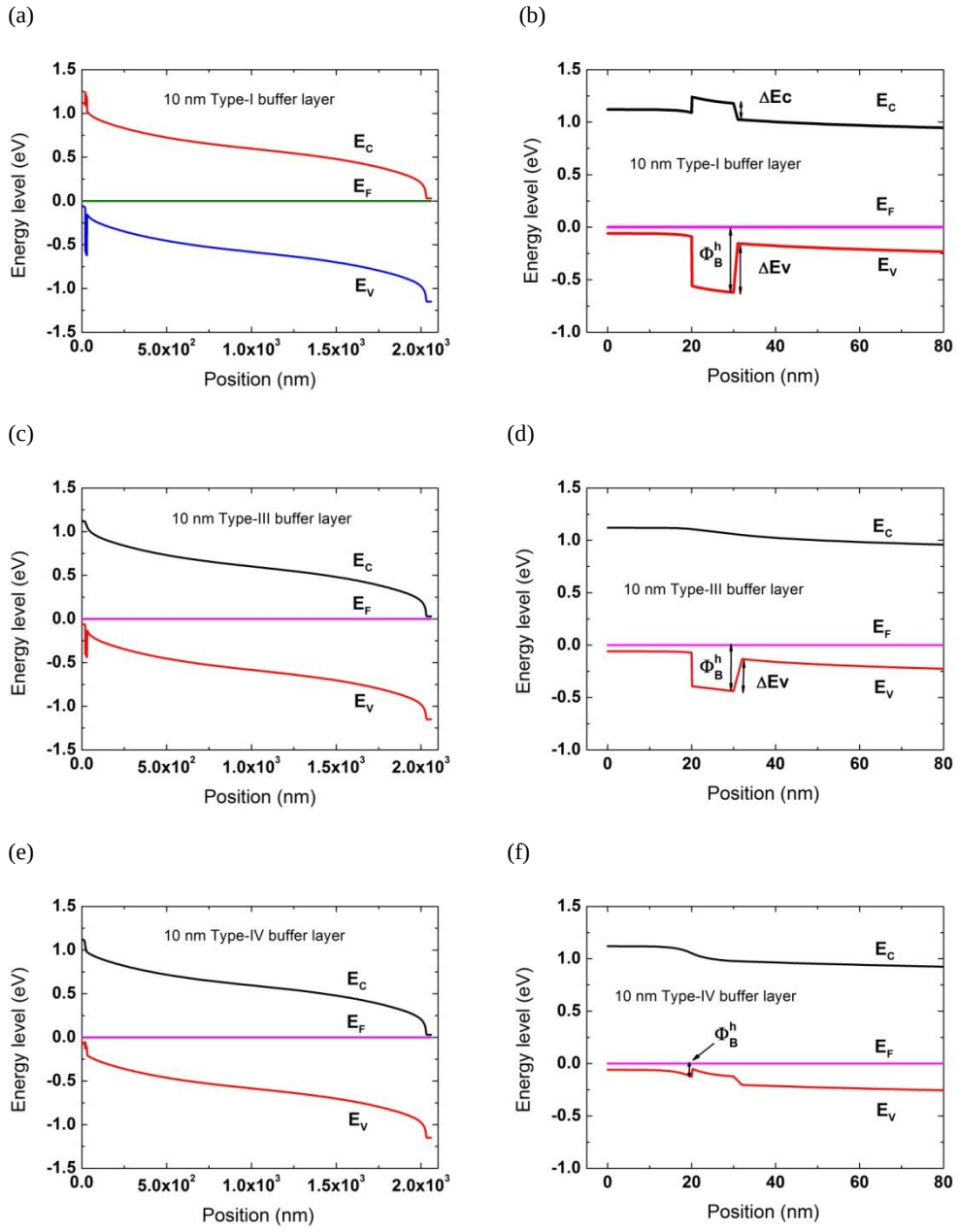


Figure 5.7: The band diagrams for µc-Si:H thin-film solar cells with 10 nm thick (a, b) Type-I buffer layer; (c, d) Type-III buffer layer; (e, f) Type-IV buffer layer at the p/i interface under dark equilibrium condition. Graphs (a, c, e) show the band diagram for the whole solar cell, while graphs (b, d, f) show the band diagram near the p/i interface.

5.3.2 Type-I (a-Si:H) buffer layer

Applying the same calculation process to the Type-I (a-Si:H) buffer layer as already done for the intrinsic µc-Si:H absorber layer of the solar cell (*i*-layer), the relationship between the minority carrier lifetime, the diffusion length, the generation rate, and the quasi Fermi level splitting can also be calculated for a buffer layer. This is shown in Figure 5.8 (the discussion about the drift length L_{drif} for all the buffer layers is not included as it is not a critical factor). Similar to the µc-Si:H *i*-layer (see Figure 5.2), the minority carrier lifetime and diffusion length drop with increasing generation rate and quasi Fermi level splitting. This can be attributed to the fact that more excess carriers are created when the generation rate G increases. It leads to a higher recombination rate U (U = G under V_{oc} condition) and therefore shorter minority carrier lifetime as well as diffusion length.

The shaded regions in Figure 5.8 indicate the typical generation rates and the corresponding open-circuit voltage as well as the maximum power point, if the solar cells (having a 2 µm thick absorber layer) generate a short-circuit current from 20 to 30 mA/cm^2 (corresponding to a generation rate of 6.25×10^{20} to 9.375×10^{20} cm^{-3}s^{-1}). In this case, within the 10 nm thick buffer layer, the generation current ranges from 0.1 to 0.15 mA/cm^2.

In order to compare to previous data (under the same illumination condition), a constant generation rate of 7.5×10^{20} cm^{-3}s^{-1} was selected, referring to a photo-generation current of 24 mA cm^{-2} within the µc-Si:H thin-film solar cell. As a result, within the 10 nm thick buffer layer, a generation current of 0.12 mA/cm^2 is generated as indicated in Figure 5.8(a) and (c) by an arrow. At the same time, the minority carrier lifetime can be read to be around 6.3 ns from Figure 5.8(a). In this case, the quasi Fermi level splitting is around 0.89 V, see Figure 5.8(b), and the diffusion length is around 128 nm, see Figure 5.8(c) or (d). As the diffusion length is much

larger than the buffer layer thickness, it is not necessary to discuss about the drift length in this case.

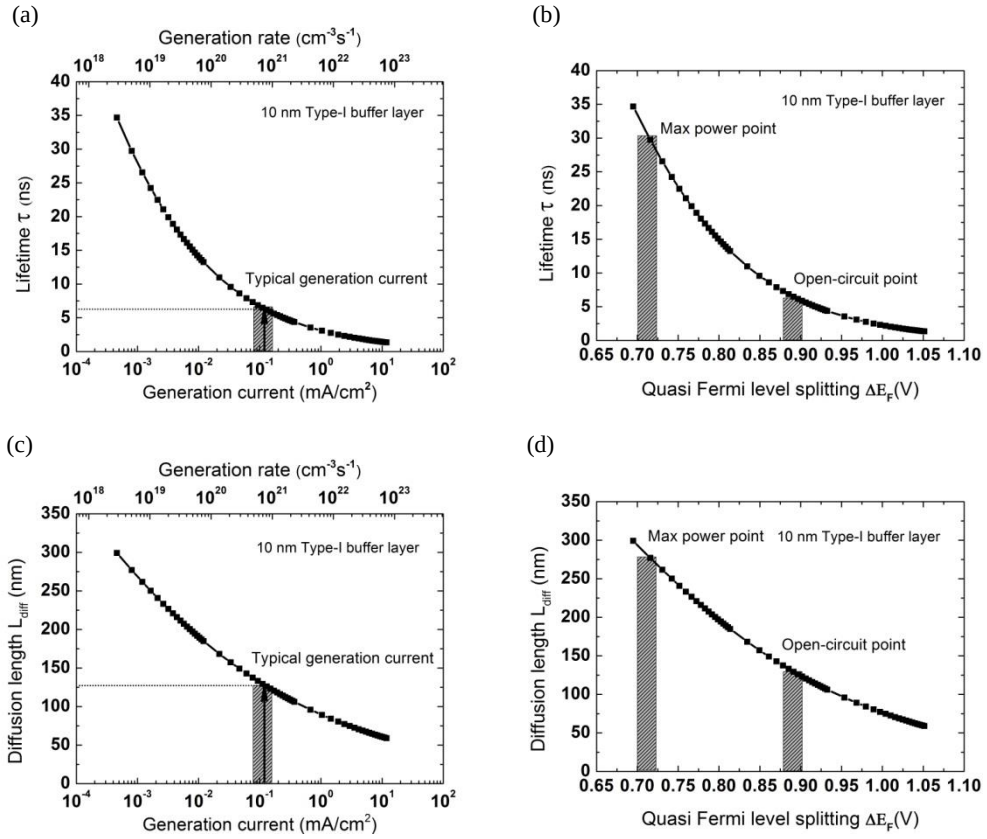


Figure 5.8: (Top) Simulated lifetime τ of a Type-I (a-Si:H) buffer layer (a) versus the generation current (or generation rate), considering a 10 nm thick film, (b) versus the quasi Fermi level splitting ΔE_F; (Bottom) Simulated diffusion length L_{diff} of a Type-I (a-Si:H) buffer layer (c) versus the generation current (or generation rate) considering a 10 nm thick film, (d) versus the quasi Fermi level splitting ΔE_F.

Furthermore, It should be emphasized that under the same generation rate (illumination condition), the Type-I (a-Si:H) buffer layer has much larger ΔE_F than the intrinsic µc-Si:H absorber layer of the solar cell (*i*-layer), i.e. 0.89 vs. 0.50 V.

5.3.3 Type-IV (highly crystallized µc-Si:H) buffer layer

The interconnection between the minority carrier lifetime, diffusion length, generation rate, and quasi Fermi level splitting for a Type-IV (highly crystallized

µc-Si:H) buffer layer is shown in Figure 5.9. The same generation rate of 7.5×10^{20} $cm^{-3}s^{-1}$ was selected.

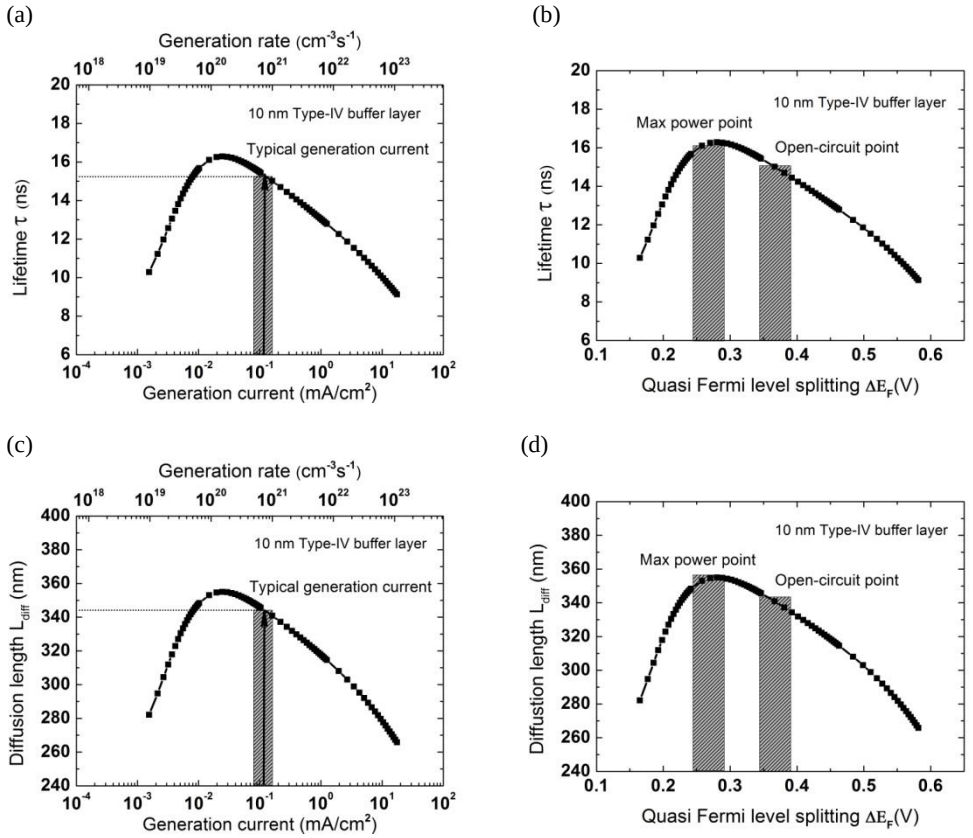


Figure 5.9: (Top) Simulated lifetime τ of a Type-IV (highly crystallized µc-Si:H) buffer layer (a) versus the generation current (or generation rate) considering a 10 nm thick film, (b) versus the quasi Fermi level splitting ΔE_F; (Bottom) Simulated diffusion length L_{diff} of a Type-IV (highly crystallized µc-Si:H) buffer layer (c) versus the generation current (or generation rate) considering a 10 nm thick film, (d) versus the quasi Fermi level splitting ΔE_F.

Within the 10 nm thick Type-IV buffer layer, the minority lifetime reaches around 15.3 ns, see Figure 5.9(a) and the corresponding ΔE_F is only around 0.35 V, see Figure 5.9(b). Besides, the diffusion length is estimated to be around 344 nm, see Figure 5.9(c) or (d). It should be pointed out that the quasi Fermi energy splitting ΔE_F for the Type-IV buffer layer (which is a highly crystallized film) is much lower than for the intrinsic µc-Si:H absorber layer (*i*-layer), i.e. 0.35 vs. 0.50 V under the same illumination condition. This can be attributed to the fact that the Type-IV buffer layer has a much higher defect density due to its higher crystallinity, which limits ΔE_F.

Therefore, it can be predicted that the Type-IV buffer layer used in the p/i interface will cause a high recombination rate at this region and limit the quasi Fermi level splitting for the solar cells. A lower V_{oc} can be expected to result.

5.3.4 Type-III (a-Si:H with percolated µc-Si:H grains) buffer layer

The interconnection between the minority carrier lifetime, diffusion length, generation rate, and quasi Fermi level splitting for Type-III (a-Si:H with percolated µc-Si:H grains) buffer layer is shown in Figure 5.10. The same generation rate of 7.5×10^{20} $cm^{-3}s^{-1}$ was selected.

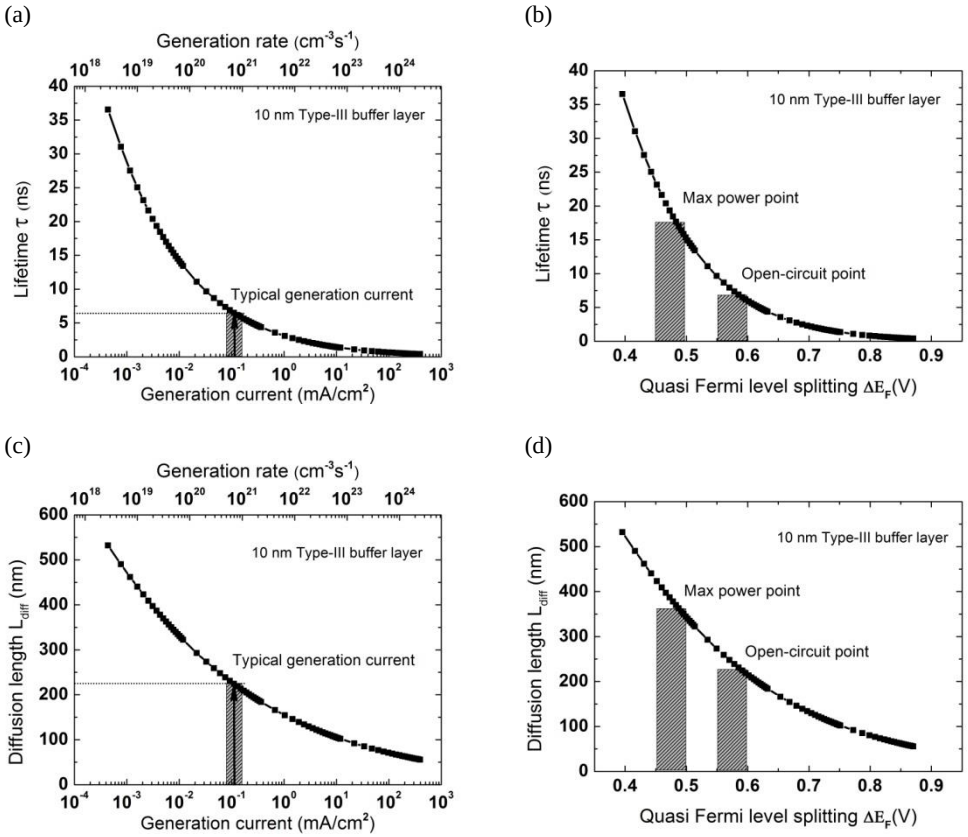


Figure 5.10: (Top) Simulated lifetime τ of a Type-III (a-Si:H with percolated µc-Si:H grains) buffer layer (a) versus generation current (or generation rate), considering a 10 nm thick film, (b) versus the quasi Fermi level splitting ΔE_F; (Bottom) Simulated diffusion length L_{diff} of a Type-III (a-Si:H with percolated µc-Si:H grains) buffer layer (c) versus the generation current (or generation rate) considering a 10 nm thick film, (d) versus the quasi Fermi level splitting ΔE_F.

Within the 10 nm thick Type-III buffer layer, the minority carrier lifetime reaches around 6.34 ns, see Figure 5.10(a) and it is very close to the Type-I buffer layer (6.32 ns). It results from the assumption that they have similar defect distribution. However, the diffusion length of the Type-IV buffer layer, see Figure 5.10(c) or (d) is larger compared to the Type-I buffer layer, i.e. 222 vs. 128 nm. This is due to the improved carrier mobility in the Type-III buffer layer (see Table 5.3) with the percolated μc-Si:H paths. In addition, under the same illumination condition, the Type-III buffer layer has smaller ΔE_F (around 0.59V, see Figure 5.10(b)) than the Type-I buffer layer due to their different band gaps (1.5 vs. 1.8 eV) although they have similar defect distribution. However, the ΔE_F for Type-III buffer layer is still larger than the μc-Si:H *i*-layer (0.59 vs. 0.497 V).

5.3.5 Comparison of the resulting buffer layer properties

A brief summary of the simulated resulting buffer layer properties compared to the intrinsic μc-Si:H absorber layer (i-layer), using the same illumination conditions, i.e. a constant generation rate of $G = 7.5\times10^{20}$ $cm^{-3}s^{-1}$, is presented in Table 5.4.

Table 5.4 Comparison of the simulated electrical parameters for different buffer layers (and for the μc-Si:H i-layer used as a reference) under the same illumination condition ($G = 7.5\times10^{20}$ $cm^{-3}s^{-1}$). L is the layer thickness; G is the generation rate; Δn is the excess carrier density; ΔE_F is the quasi Fermi level splitting; τ is the minority lifetime; and L_{diff} is the diffusion length.

	L (nm)	**G (cm^{-3} s^{-1})**	**Δn (cm^{-3})**	**ΔE_F (V)**	**τ (ns)**	**L_{diff} (nm)**
μc-Si:H i-layer	2000	7.5×10^{20}	6.0×10^{13}	0.4967	80.07	787.2
Type-I buffer layer	10	7.5×10^{20}	4.737×10^{12}	0.894	6.32	127.7
Type-III buffer layer	10	7.5×10^{20}	4.75×10^{12}	0.594	6.34	222
Type-IV buffer layer	10	7.5×10^{20}	1.15×10^{13}	0.351	15.3	344

In general, a higher bandgap and lower defect density of the buffer layer (compared to the reference intrinsic μc-Si:H absorber layer) should lead to a larger quasi Fermi level splitting ΔE_F. The corresponding numerical calculations confirm this trend and the sequence follows as:

$$\text{Type-I} > \text{Type-III} > \text{i-layer} > \text{Type-IV}; \quad (\Delta E_F \text{ for each layer}) \qquad (5.16)$$

It can be expected that when these buffer layers are introduced between the p/i interface of the reference thin-film μc-Si:H solar cell, they will correspondingly impact the quasi Fermi level splitting of the solar cell and the resulting open-circuit voltage of the solar cell should follow the same trend as (5.16).

Besides, the band offsets from the Type-I, III, IV buffer layers towards μc-Si:H i-layer were also compared in Table 5.3 and Figure 5.6. The effective barrier height resulting from the valence band offset at the p/i interface is a crucial factor to impact the hole transport and collection. The Type-I buffer layer has the largest valence band offset, and therefore it has the highest probability to impede the hole collection. Type-III buffer layer suffers from the same issue but not as seriously as Type-I buffer layer. Type-IV buffer layer doesn't have this problem. Thus it can be expected that especially the Type-I buffer layer may not be able to drive sufficient current across the barrier formed by the heterojunction, which would affect the resulting short-circuit current of the solar cell.

The carrier mobility is another important factor to determine the resistance of the buffer layer, which can be reflected from the L_{diff} listed in Table 5.4. The Type-I buffer layer has poor carrier mobility and it is expected to add a high series resistance component to the solar cell when introduced at p/i interface. On the other hand, a Type-IV buffer layer has good carrier mobility and therefore it is expected to reduce the series resistance to the solar cell. This could further improve the fill factor of the solar cell. A Type-III buffer layer has μc-Si:H percolated paths, which improve the

carrier mobility to the level of a µc-Si:H i-layer. Its impact on the series resistance is expected to be somewhere between the Type-I and Type-IV buffer layers.

5.4 Thickness dependence of the various buffer layers on the *I-V* performance of thin-film µc-Si:H solar cells

In this section, numerical modelling by using the ASA software [33, 34] is carried out to study the impact of the different types of buffer layers introduced into the p/i interface and their thickness variation on the *I-V* performance of µc-Si:H thin-film solar cells. The µc-Si:H cell without buffer layer is used as reference.

5.4.1 Type-I (a-Si:H) buffer layer

Simulated *I-V* performance of µc-Si:H solar cells using a different thickness of a Type-I buffer layer is shown in Figure 5.11, and compared to the reference case, i.e. not using a buffer layer. To simulate the *I-V* performance of the solar cells, a total photogeneration current of 24 mA cm^{-2} within the solar cell was assumed. That is, considering photon absorption within the 2000 nm thick µc-Si:H absorber layer (i-layer), the 20 nm thick hole collection layer (p-layer) and the 30 nm thick electron collection layer (n-layer) as well as within the buffer layer with a variable thickness of L nm, the constant generation rate G within the solar cell is calculated by:

$$G = \frac{24\ mA/cm^2}{1.6\times10^{-19}C\times(2000+20+30+L)\times10^{-7}cm}\ ; \qquad (5.17)$$

For example, if L = 0 (no buffer layer, reference cell), the generation rate G equals $G = 7.32\times10^{20}$ $cm^{-3}s^{-1}$. However, for a 50 nm thick buffer layer (L = 50 nm) one obtains $G = 7.14\times10^{20}$ $cm^{-3}s^{-1}$.

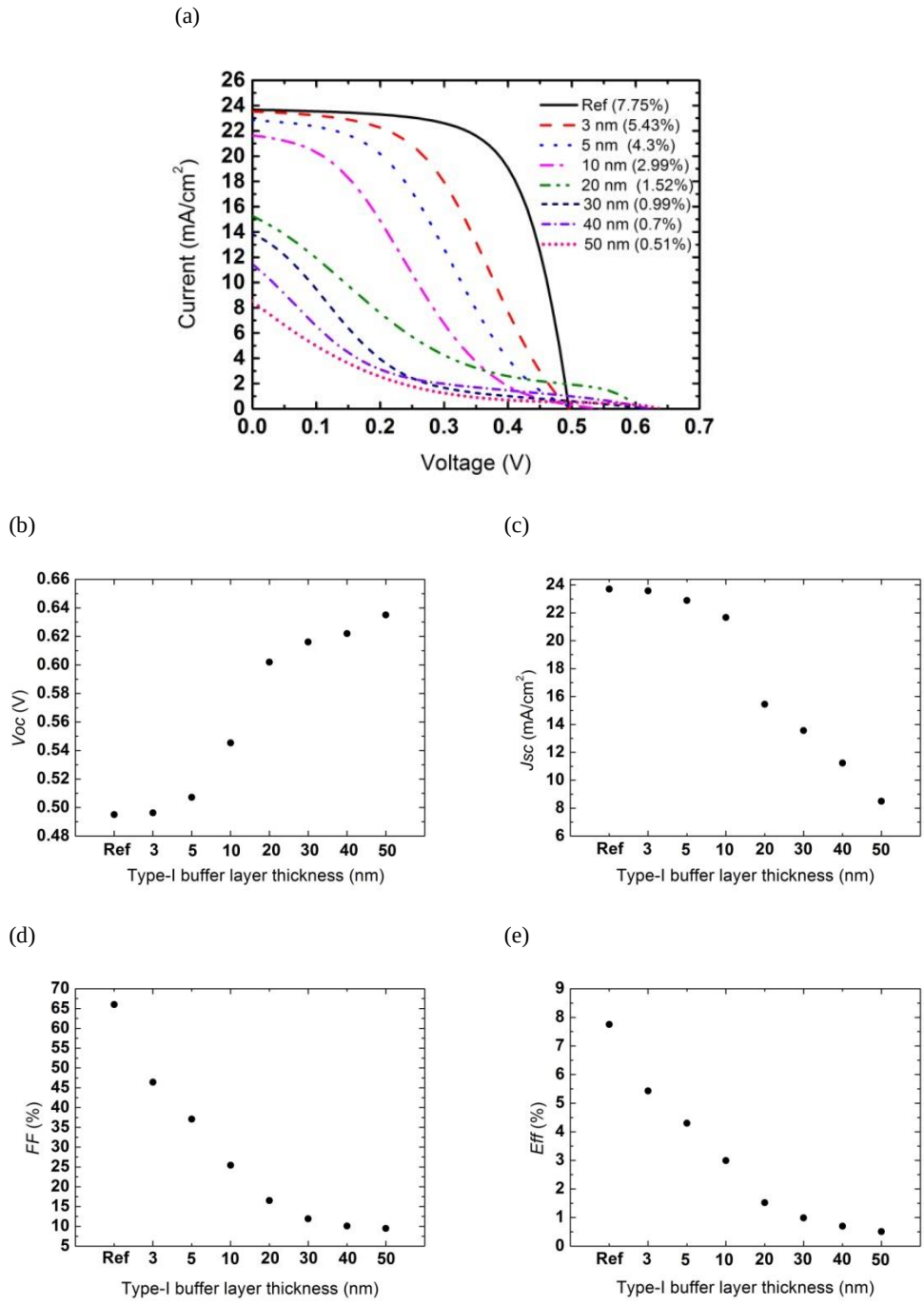


Figure 5.11: (a) Simulated *I-V* curves under a constant generation rate for μc-Si:H cells using a Type-I buffer layer with different thickness. The corresponding cell efficiencies are indicated in brackets. The influence of the thickness of the Type-I buffer layer on (b) the open-circuit voltage, (c) the short-circuit current, (d) the fill factor and (e) the conversion efficiency is shown.

The simulated I-V curves for the cells using Type-I buffer layers with different thickness are shown in Figure 5.11(a). As can be seen, the increase of the Type-I buffer layer thickness will cause a continuous drop of the PV efficiency. When it

becomes thicker than 30 nm, the I-V curve turns out to be 'S-shaped'. This simulated S-shape I-V curve was also observed in our experiments, see Chapter 4 and Figure 4.9(b).

Figure 5.11(b) to (e) show the impact of the buffer layer thickness on the I-V parameters of the solar cell. The V_{oc} increases compared to the reference case (not using a buffer layer) when the Type-I buffer layer is introduced, and it increases with increasing buffer layer thickness.

However, J_{sc} and - in particular - the fill factor *FF* drops, after the introduction of a Type-I buffer layer. J_{sc} can still maintain at a relatively high level when the buffer layer thickness is below 10 nm, but it starts to drop significantly when the thickness exceeds 20 nm. But the *FF* drops significantly, even for very thin (below 5 nm) Type-I buffer layers. Most importantly, as a consequence, the PV efficiency always drops if a Type-I buffer is used (being always lower than the efficiency of the reference cell), and worsening with increasing buffer layer thickness.

5.4.2 Type-IV (highly crystallized µc-Si:H) buffer layer

The simulated I-V performance of a µc-Si:H thin-film solar cells using Type-IV buffer layers of different thicknesses is shown in Figure 5.12. With increasing buffer layer thickness the PV efficiency initially improves compared to the reference case (not using a buffer layer), i.e. for thicknesses below 10 nm, but it drops again if the buffer layer thickness becomes larger than 20 nm.

The experiment performed in Chapter 4 showed that a 50 nm thick Type-IV buffer layer inserted at the p/i interface causes a clear drop of V_{oc} as compared to the reference cell. This is also confirmed by numerical simulation. The simulated V_{oc} remains at a level as high as the reference cell, as long as the Type-IV buffer layer is

thinner than 10 nm, but it starts to drop if thicker Type-IV buffer layers (above 20 nm) are used, see Figure 5.12(b).

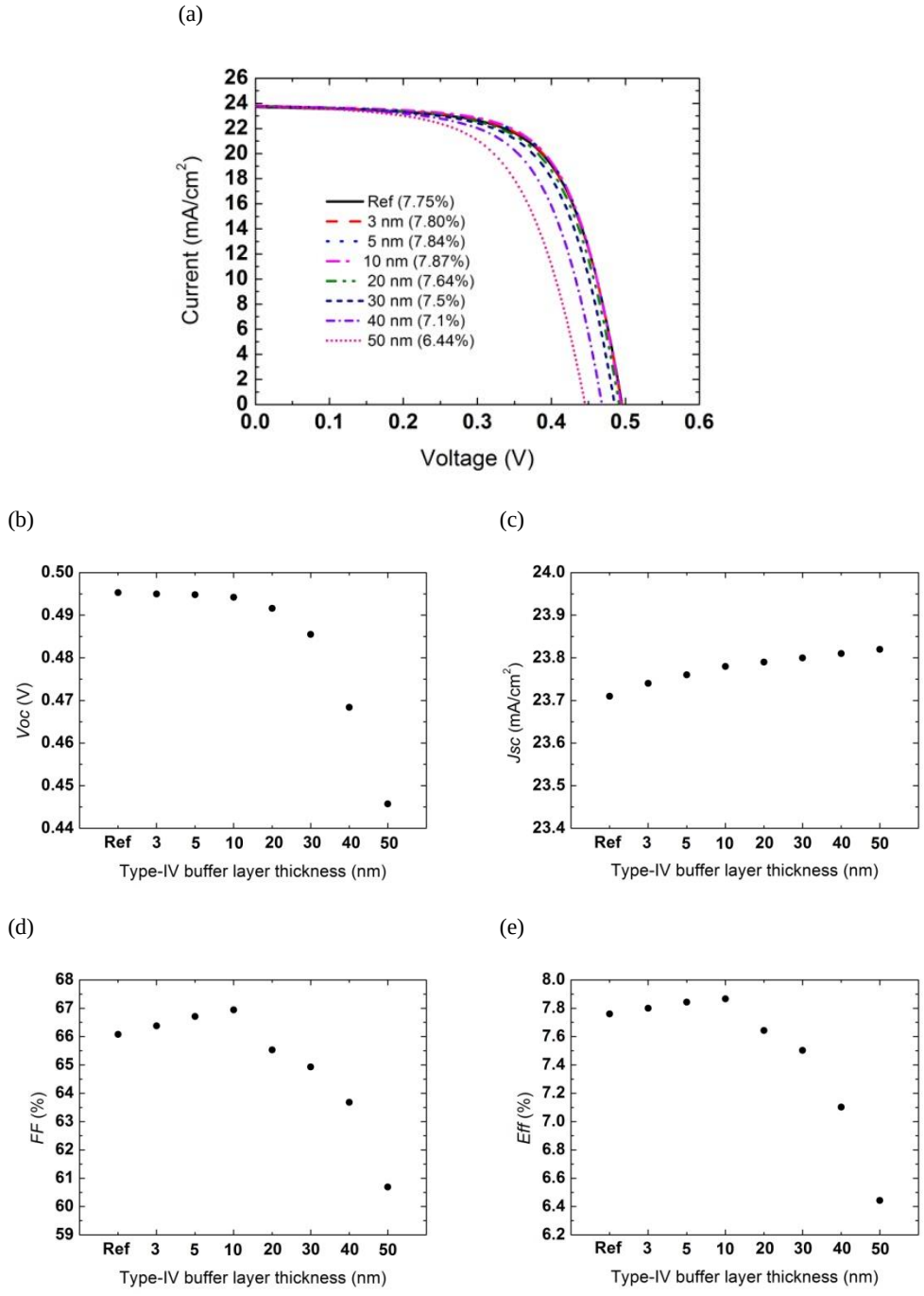


Figure 5.12: (a) Simulated *I-V* curves under a constant generation rate for µc-Si:H cells using a Type-IV buffer layer with different thickness. The corresponding cell efficiencies are indicated in brackets. The influence of the thickness of the Type-IV buffer layer on (b) the open-circuit voltage, (c) the short-circuit current, (d) the fill factor and (e) the conversion efficiency is shown.

Figure 5.12(c) shows that the J_{sc} gets slightly higher by using a Type-IV buffer layer, i.e. increasing with increasing buffer layer thickness (Please note: Using a Type-I buffer layer, the J_{sc} was decreasing with an increasing buffer layer thickness).

Considering the *FF*, as shown in Figure 5.12(d), it increases slightly when a thin Type-IV buffer layer (below 10 nm) is used, but it drops significantly if increasing the buffer layer thickness above 20 nm. Finally, Figure 5.12(e) shows there is an optimum thickness (around 10 nm) for a Type-IV buffer layer being introduced at the p/i interface of a µc-Si:H thin-film solar cell. The resulting maximum efficiency is slightly larger than the reference cell efficiency (not using a buffer layer), i.e. an efficiency increase of around 2 % (relative) has been simulated, increasing the solar cell efficiency by 0.15 % (absolute).

5.4.3 Type-III (a-Si:H with percolated µc-Si:H grains) buffer layer

The simulated I-V performance of a µc-Si:H cell using different Type-III buffer layer thicknesses is shown in Figure 5.13. Figure 5.13(a) shows the influence of the Type-III buffer layer thickness on the I-V curves. The efficiency improves significantly if thin Type-III buffer layers (below 20 nm) are used but it gradually drops when thicker Type-III buffer layers (above 30 nm) are used.

Similar to the Type-I buffer layer, the V_{oc} increases as the Type-III buffer layer becomes thicker, see Figure 5.13(b). But the V_{oc} enhancement due to the thickness increase is not as large as that for Type-I buffer layers. Indeed, this V_{oc} enhancement has already been observed experimentally as shown in Chapter 4, see Figure 4.12 and Figure 4.15.

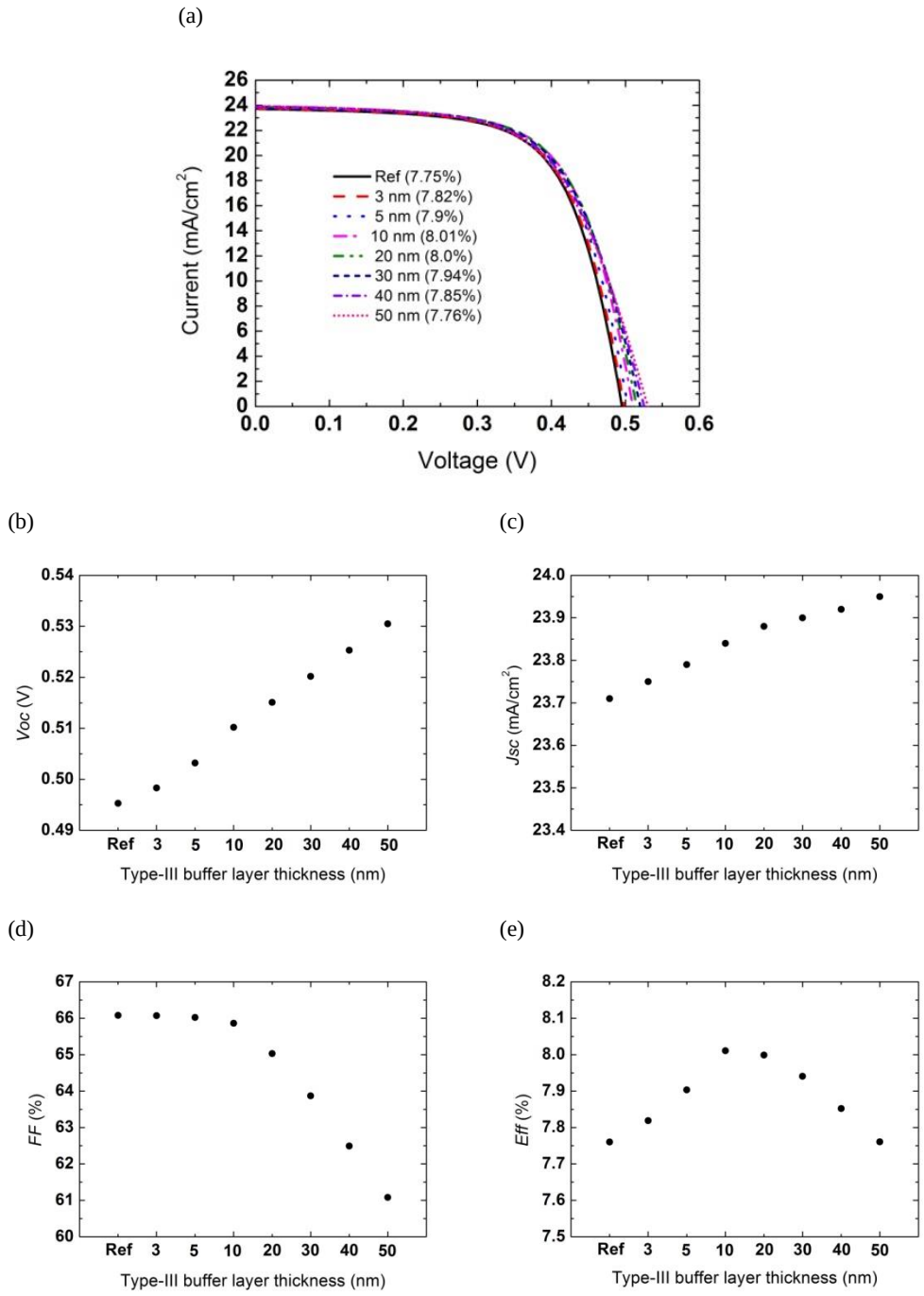


Figure 5.13: (a) Simulated *I-V* curves under a constant generation rate for µc-Si:H cells using a Type-III buffer layer with different thickness. The corresponding cell efficiencies are indicated in brackets. The influence of the thickness of the Type-III buffer layer on (b) the open-circuit voltage, (c) the short-circuit current, (d) the fill factor and (e) the conversion efficiency is shown.

Furthermore, the experimental results of Chapter 4 show that a significant increase of J_{sc} can be realized by using a Type-III buffer layer. However, the simulated results of Figure 5.13(c) show only a slight J_{sc} increase with increasing Type-III buffer layer

thickness, similar to the simulated Type-IV buffer layer. A possible reason for that might be the fact that a constant generation rate (within the solar cells) was used in the simulation, but in reality the buffer layer also absorbs some light and the real generation rate within the buffer layer is higher than the assumed value for the simulation.

For a Type-IV buffer layer, there is no serious impact on the *FF*, as long as the buffer layer thickness is below 10 nm, but it starts to decrease when the Type-III buffer layer thickness is larger than 20 nm, see Figure 5.13(d). This slight decrease of *FF* was also observed in the experiment, see Figure 4.12.

Finally, Figure 5.13(e) shows that there is an optimum Type-III buffer layer thickness, in the 10 - 20 nm range, causing a relative efficiency improvement of 3.3 % as compared to the reference cell (corresponding to an absolute efficiency enhancement of 0.26 %). This confirms the experimental observation, whereas an optimum efficiency increase has been observed if using a 10 - 20 nm thick Type-III buffer layer, see Figure 4.12. Compared to a Type-IV buffer layer, the simulated efficiency enhancement is now significantly higher, again agreeing with the experimental observations of Chapter 4. It should be further pointed out that even thick Type-III buffer layers (up to 50 nm) will still enhance the solar cell efficiency (compared to the reference cell, i.e. not using a buffer layer). Thus there is a rather broad process window for implementing a Type-III buffer layer. Again, this simulated result was also observed in the experiments of Chapter 4. Method B was used to process a Type-III buffer layer with a thickness variation from 3 to 10 nm, and Method C was used to process a 50 nm thick Type-III buffer layer at the p/i interface. The solar cell efficiencies using these buffer layers were always larger than the reference cell efficiency, for all Type-III buffer layer thicknesses investigated.

5.4.4 Comparison of the thickness dependence using different buffer layers

Figure 5.14 shows an efficiency comparison for the solar cells having different types of buffer layers. The solar cell without a buffer layer is used as a reference and marked by a dashed line. As can be seen, a Type-I buffer layer diminishes the efficiency even if only a very thin buffer layer is used, and the efficiency loss worsens with increasing buffer layer thickness. For a Type-IV buffer layer, the efficiency improves for thin buffer layers (up to 20 nm) and then the efficiency drops below the reference efficiency for buffer layer thicknesses above 20 nm. A 10 nm thick Type-IV buffer layer reaches the maximum efficiency enhancement. The introduction of a Type-III buffer layer always improves the PV efficiency, no matter if a thin or thick buffer layer is used. But again there is an optimum thickness of about 10 nm, leading to a maximum efficiency enhancement of 3.3 %. Thus the Type-III buffer layers deliver the maximum efficiency enhancement.

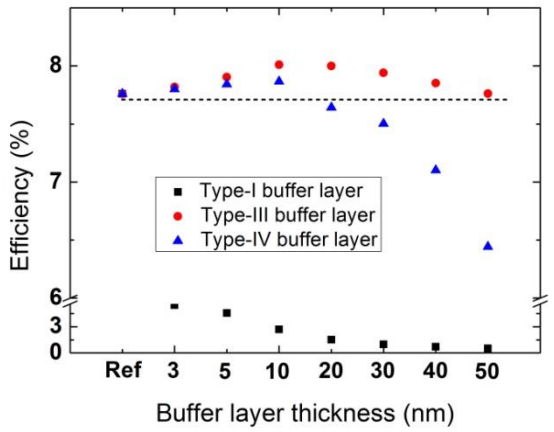


Figure 5.14: Comparison of the simulated conversion efficiency of µc-Si:H thin-film solar cells using either no buffer layer (reference case) or using a Type-I, Type-III or Type-IV buffer layer at the p/i interface of the solar cell, as a function of the buffer layer thickness.

According to this simulation, if there is an efficiency improvement, for all cases investigated, the maximum efficiency enhancement is achieved by using a buffer layer which is approximately 10 nm thick. Consequently, in the following sections,

the buffer layer thickness is always fixed at 10 nm, and the physical origin of the different behaviour of the different buffer layers will be investigated.

5.5 Discussion of the influence of the various buffer layers on the *I-V* performance of thin-film µc-Si:H solar cells

In the previous section, the numerical modelling was realized to simulate the influence of different types of buffer layers and their thickness on the I-V parameters of the solar cells. The simulated results agree well with the experimental data reported in Chapter 4 and reflect the general trend of the thickness dependence for each type of buffer layer. In this section, a series of theoretical investigations is carried out to explain the above observed phenomena.

5.5.1 Type-I (a-Si:H) buffer layer

Influence on short-circuit current

The simulated short-circuit current decreases with increasing Type-I buffer layer thickness, see Figure 5.11(c). The introduction of the Type-I buffer layer at the p/i interface will cause the change of the band diagram under the dark equilibrium condition as shown in Figure 5.15. As discussed in Chapter 5.3.1, the introduction of the Type-I buffer layer at the p/i interface leads to the formation of a conduction band offset (ΔE_c) and a valence band offset (ΔE_v) between the buffer layer and *i*-layer. Generally, these band offsets are determined by the material properties (*i.e.* electron affinity and bandgap) of the neighbouring layers and will not change if the buffer layer thickness is varied (*i.e.* $\Delta E_{C1} = \Delta E_{C2}$, $\Delta E_{V1} = \Delta E_{V2}$, where ΔE_{C1} and ΔE_{V1} are the band offsets for cell using a 10-nm Type-I buffer layer; and ΔE_{C2} and ΔE_{V2} are the

band offsets for cell using a 40-nm Type-I buffer layer). However, the effective barrier height $\Phi_B{}^h$ at the valence band, which is the most important quantity determining the hole transport (from the intrinsic absorber layer into the hole accumulation layer), is largely impacted by the buffer layer thickness, as shown in Figure 5.15. An increasing Type-I buffer layer thickness increases the effective barrier height (*i.e.* $\Phi_{B1}{}^h < \Phi_{B2}{}^h$), see Figure 5.15. Therefore an increasing buffer layer thickness will further block the hole transport into the p-layer.

The corresponding effective barrier height values as a function of buffer layer thickness are listed in Table 5.5. The significant drop of the J_{sc} with increasing buffer layer thickness, as observed in Chapter 5.4.1, is a direct consequence of the observed increase of effective barrier height with increasing buffer layer thickness, as shown in Table 5.5. The effective barrier height Φ_B determines the total electron or hole current J over a barrier Φ_B via thermionic emission, which can be expressed as [142]:

$$J = A^* T^2 \exp\left(-\frac{q\Phi_B}{kT}\right); \tag{5.19}$$

where A^* is effective Richardson constant, k the Boltzmann constant and T the absolute temperature. From Eqn. (5.19), a linear increase of $\Phi_B{}^h$ results in an exponential decrease of J.

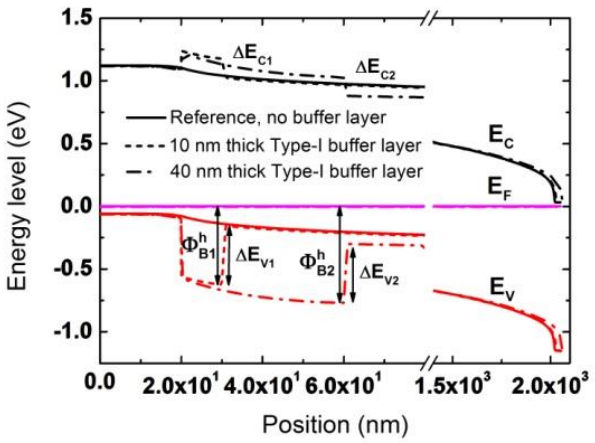


Figure 5.15: The band diagram of µc-Si:H cells having no (reference) and 10 nm as well as 40 nm thick Type-I buffer layer at the p/i interface under dark equilibrium condition. The change of the effective barrier height $\Phi_B{}^h$ was illustrated due to the buffer layer thickness variation.

Table 5.5 Type-I buffer layer thickness versus the effective barrier height for hole (Φ_B^h) at the valence band edge near the p/i interface. The pseudo shunt resistance (pseudo-R_{sh}) and the series resistance (R_s) were extracted from the simulated *I-V* curves for the µc-Si:H cells having different thicknesses of Type-I buffer layer.

Buffer layer thickness (nm)	**Ref**	**3**	**5**	**10**	**20**	**30**	**40**	**50**
Φ_B^h (eV)	0	0.58	0.592	0.621	0.672	0.721	0.767	0.808
pseudo-R_{sh} (Ωcm^2)	1025	473.3	338.4	165.6	40.4	33.7	27.8	25.6
R_s (Ωcm^2)	2.82	19.5	54	97.4	120.2	139.7	158.7	185.2
***FF* (%)**	66.1	45.9	38.2	21.6	16.5	11.9	10.1	9.5

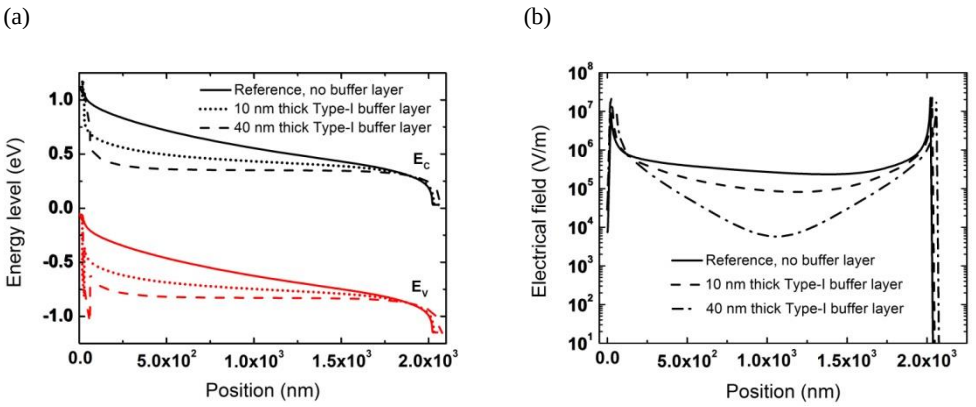


Figure 5.16: (a) The band diagram of µc-Si:H cells having no (reference) and 10 nm as well as 40 nm thick Type-I buffer layer at the p/i interface under the short-circuit condition (the quasi Fermi level E_{Fe} and E_{Fh} were removed). (b) The internal electrical field distribution within the µc-Si:H cells having no (reference) and 10 nm as well as 40 nm thick Type-I buffer layer at the p/i interface under short-circuit condition.

The introduction of the Type-I buffer layer at the p/i interface also causes the change of the band diagram under short-circuit condition as shown in Figure 5.16(a). It leads to a large band bending near the p/i interface and the band bending within the intrinsic µc-Si:H solar cell absorber (i.e. the built-in potential within the i-layer) decreases with increasing buffer layer thickness, see Figure 5.16(a). As the slope of the band bending reflects the strength of the electric field, the introduction of a Type-I buffer layer therefore weakens the electric field within the i-layer, and this effect becomes even more pronounced with increasing buffer layer thickness. The corres-

ponding internal electrical field distribution within a µc-Si:H cell using Type-I buffer layers of varying thickness is illustrated in Figure 5.16(b). The weakening of the internal electrical field will thus cause a poor excess carrier collection (reducing the drift diffusion length within the solar cell absorber) and thus a decreasing J_{sc}. This is an alternative explanation (though interconnected) for the decrease in J_{sc} with increasing Type-I buffer layer thickness.

Influence on open-circuit voltage

The V_{oc} increases with increasing Type-I buffer layer thickness. It can be determined from the quasi Fermi level splitting between the two terminals of the solar cells:

$$eV_{oc} = E_{Fh}(0) - E_{Fe}(L); \qquad (5.18)$$

Figure 5.17 illustrates and compares the band diagrams under open-circuit conditions of the µc-Si:H thin-film reference solar cell (not using a buffer layer) and a corresponding cell using a 40 nm thick Type-I buffer layer. In case that a Type-I buffer layer is introduced at the p/i interface, the ΔE_F (between the two terminals as indicated by the arrows in Figure 5.17) becomes larger than reference cell, reflecting the increase of V_{oc}. As obvious in Figure 5.17, within the Type-I buffer layer there is a much larger quasi Fermi energy splitting ΔE_F than in the intrinsic µc-Si:H absorber layer of the solar cell (i-layer), as already discussed in Chapter 5.3.2.

The simulated V_{oc} increases with increasing Type-I buffer layer thickness. This is because this buffer layer not only impedes the hole transport but also prevents the electrons (minority carriers) to enter the buffer layer and to recombine at the hole collecting layer (p-layer). It decreases the contact recombination and thus will suppress the dark saturation current J_o. An increasing buffer layer thickness will also

increase the conduction band barrier height (in full analogy to the valence barrier height as discussed before). This means excess electrons are more effectively blocked from reaching the p-layer and recombining there (reduced contact recombination) Therefore, a further increase of V_{oc} can be observed if a thicker Type-I buffer layer is used, as there is now less electron back diffusion and a further reduced J_o.

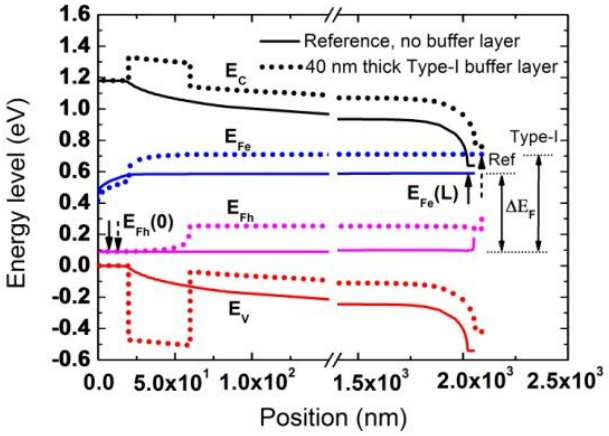


Figure 5.17: The band diagram of µc-Si:H cells having no (reference) and 40 nm thick Type-I buffer layer at the p/i interface under open-circuit condition. Comparison of the ΔE_F between the reference cell and the cell with 40 nm thick Type-I buffer layer is illustrated.

Influence on fill factor

The *FF* continuously drops with increasing Type-I buffer layer thickness. Table 5.5 lists the resulting pseudo-shunt and series resistances, pseudo-R_{sh} and R_s, extracted from the simulated I-V curves, using a simple fitting procedure towards the idealized one-diode solar cell model [146]. As can be seen, an increase of the buffer layer thickness will cause an extremely high series resistance (mainly resulting from the band offsets, leading to a barrier blocking holes from entering the hole collecting layer) and a significant drop of the pseudo-shunt resistance (again induced by the band offsets, thus not describing a real shunt). The poor pseudo-R_{sh} values (which are decreasing with increasing buffer layer thickness) are the reasons for the poor *FF*

values when using a Type-I buffer layer, which will also decrease with increasing buffer layer thickness.

It should be pointed out that the pseudo-R_{sh} values shown here do not reflect real shunts but result from the band offsets (blocking hole and electron transport), which are not accounted for using an ideal one-diode solar cell model during the fitting procedure, thereby extracting R_s and R_{sh} from the experimentally obtained I-V curves. This is why it has been called a 'pseudo' R_{sh}. Further note that also R_s will now contain two components, i.e. one "real" series resistance component (which is increasing with increasing buffer layer thickness) as well as a "pseudo-R_s" component, which again stems from the band offsets (blocking electron and hole transport).

In full analogy to the earlier discussion, the observed decrease in fill factor with increasing Type-I buffer layer thickness can also be explained by the weakening of the electric field within the intrinsic μc-Si:H absorber layer. According to the literature, a weakening of the electrical field within the absorber layer of a thin-film solar cell (p-i-n device configuration, i.e. requiring a field enhanced carrier collection) leads to a decrease in *FF* [147-149].

In summary, a Type-I buffer layer does bring a large enhancement of V_{oc}, but only if a comparatively thick buffer layer is used (> 10 nm). However, a thick buffer layer will significantly reduce the J_{sc} and (even more so) the *FF* (due to a blocked transport of excess carriers into the electron/hole accumulation layers, induced by the band offsets of the Type-I buffer layer). Therefore, finally, the efficiency gets reduced, i.e. a Type-I (a-Si:H) buffer layer is not able to enhance the efficiency of thin-film μc-Si:H solar cells.

5.5.2 Type-IV (highly crystallized µc-Si:H) buffer layer

Influence on short-circuit current

The simulated J_{sc} increases slightly with increasing Type-IV buffer layer thickness, see Figure 5.12(c). Figure 5.18 shows the impact of the Type-IV buffer layer thickness on the internal electrical field distribution. As can be seen, the thin Type-IV buffer layer (below 10 nm) hardly changes the electric field in the solar cell as compared to the reference cell without the buffer layer. Only when it becomes very thick (i.e. above 20 nm), the electric field in the bulk of the *i*-layer decreases slightly, as shown in Figure 5.18 for the cell with 40 nm thick Type-IV buffer layer. However, this slight drop of the electric field does not influence the carrier extraction, compare Figure 5.12(c). Besides, the effective barrier height listed in Table 5.6 is quite small (compared to a Type-I buffer layer) and does not change as the Type-IV buffer layer thickness increases. Thus the introduction of a Type-IV buffer layer at the p/i interface does not block the hole transport into the p-layer. Therefore, J_{sc} is not affected by the Type-IV buffer layer.

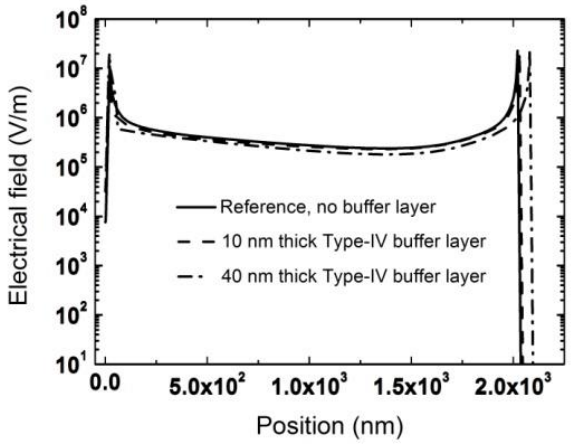


Figure 5.18: The internal electric field distribution within the µc-Si:H cells having no (reference) and 10 nm as well as 40 nm thick Type-IV buffer layer at the p/i interface under short-circuit condition.

Table 5.6 Type-IV buffer layer thickness versus the effective barrier height for hole (Φ_B^h) at the valence band edge near the p/i interface. Shunting resistance (R_{sh}) and series resistance (R_s) were extracted from the simulated *I-V* curves for the µc-Si:H cells having different thicknesses of Type-IV buffer layer.

Buffer layer thickness (nm)	Ref	3	5	10	20	30	40	50
Φ_B^h (eV)	0	0.08	0.08	0.08	0.08	0.08	0.08	0.08
pseudo-R_{sh} (Ωcm^2)	1025	994	985	932	883	787	638	535
R_s (Ωcm^2)	2.82	2.79	2.76	2.74	2.85	2.86	2.96	3.32
FF (%)	66.1	66.4	66.7	66.9	65.4	64.9	63.4	60.7

Influence on open-circuit voltage

The simulated V_{oc} decreases as the Type-IV buffer layer thickness increases, as shown in Figure 5.12(b).

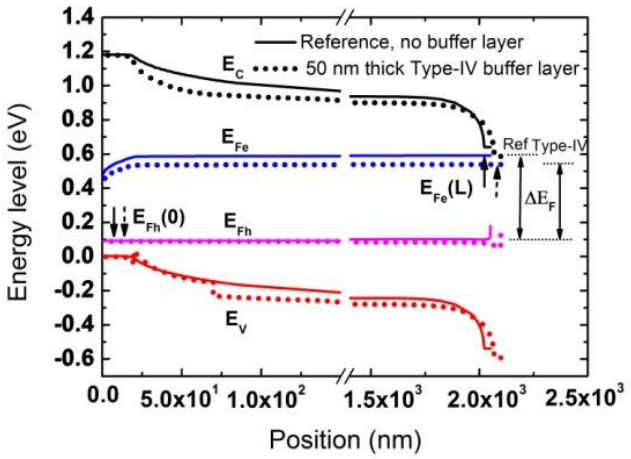


Figure 5.19: The band diagram of µc-Si:H cells having no (reference) and 50 nm thick Type-IV buffer layer at the p/i interface under open-circuit condition.

The band diagram under open-circuit condition in Figure 5.19 shows that the introduction of Type-IV buffer layer at the p/i interface limits the quasi Fermi level splitting between the two terminals (see the arrows) as compared to the reference cell

(without buffer layer). It causes the V_{oc} drop. As discussed in Chapter 5.3.3, Type-IV buffer layer has much lower ΔE_F than µc-Si:H *i*-layer at the same illumination condition due to the very high defect density and bandgap shrinking. It causes high recombination rate at the p/i interface and thus an increase of dark saturation current J_o, which becomes the limiting factor to the V_{oc}. This limiting effect aggravates as the Type-IV buffer layer becomes thicker.

Influence on the fill factor

The simulated *FF* improves when a thin (below 10 nm) Type-IV buffer layer is used but decreases when it is thicker than 20 nm, see Figure 5.12(d). Regarding the series resistance, it drops when a thin Type-IV buffer layer (below 10 nm) is used, see Table 5.6. It is attributed to the good carrier mobility in the Type-IV buffer layer, as discussed in Chapter 5.3.1. The drop of the R_s slightly improves the *FF* when thin Type-IV buffer layers are used, see Figure 5.12(d). However, when it is thicker than 20 nm, R_s starts to increase and can be ascribed to the slight decrease of the electric field in the bulk of *i*-layer, see Figure 5.18. On the other hand, because of the high defect density, a Type-IV buffer layer causes a high recombination rate at the p/i interface and thus leading to a significant drop of the pseudo-R_{shunt} (see Table 5.6). Finally, the combined effects from the R_{shunt} and R_s result in the variation of the *FF* when the Type-IV buffer layer thickness changes.

In summary, a Type-IV buffer layer causes a V_{oc} drop because it leads to a high recombination rate at the p/i interface (limiting ΔE_F). But it does not affect, or even slightly improves, the J_{sc} because it does not block the excess holes. Most dominantly, a thin Type-IV buffer layer (below 10 nm) will improve the *FF* due to its good carrier mobility and reduced R_s. If it gets too thick, however, (above 20 nm), it degrades the

FF due to the high recombination and a reduced R_{shunt}. Finally, a Type-IV buffer layer thickness of around 10 nm leads to a maximum efficiency enhancement.

5.5.3 Type-III (a-Si:H with percolated µc-Si:H grains) buffer layer

Influence on short-circuit current

The simulated J_{sc} slightly increases with increasing Type-III buffer layer thickness, see Figure 5.13(c). The corresponding electric field distribution, as shown in Figure **5.20**, indicates that the introduction of a Type-III buffer layer at the p/i interface of the µc-Si:H solar cell has no impact on the electric field in the bulk of the *i*-layer, even for very thick buffer layers (*i.e.* 40 nm thick). It means that the introduction of a Type-III buffer layer will not impact the carrier extraction from the bulk of the *i*-layer. This is the big difference as compared to the Type-I buffer layer, see Figure 5.16(b). It is a consequence of the different band alignments of the different buffer layers. A comparison will be made among them in the next chapter.

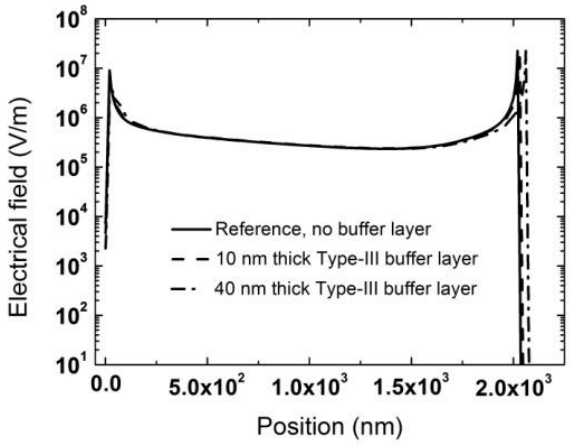


Figure 5.20: The internal electrical field distribution within the µc-Si:H cells having no (reference) and 10 nm as well as 40 nm thick Type-III buffer layer at the p/i interface under short-circuit condition.

Table 5.7 Type-III buffer layer thickness versus the effective barrier height for hole (Φ_B^h) at the valence band edge near the p/i interface. Shunting resistance (R_{sh}) and series resistance (R_s) were extracted from the simulated *I-V* curves for the μc-Si:H cells having different thicknesses of Type-III buffer layer.

Buffer layer thickness (nm)	**Ref**	**3**	**5**	**10**	**20**	**30**	**40**	**50**
Φ_B^h (eV)	0	0.419	0.427	0.439	0.457	0.470	0.479	0.487
pseudo-R_{sh} (Ωcm^2)	1025	1028	1037	1045	1026	997	961	923
R_s (Ωcm^2)	2.82	2.84	2.89	2.99	3.3	3.7	4.23	4.79
***FF* (%)**	66.1	66.1	66.0	65.9	65.0	63.9	62.5	61.1

Table 5.7 lists the values of the effective barrier height if different thicknesses of Type-III buffer layers are used. With increasing Type-III buffer layer thickness, the effective barrier height value also increases. However, even if a very thick Type-III buffer layer is used (*i.e.* 50 nm), the effective barrier height is still much smaller than in the case of a very thin (*i.e.* 3 nm) Type-I buffer layer (0.487 vs. 0.58 eV). The effect of hole blocking for a Type-III buffer layer is therefore not as serious compared to a Type-I buffer layer. Therefore, a Type-III buffer layer does not deteriorate the J_{sc}, it can even slightly increase it with increasing buffer layer thickness, in full analogy to the Type-IV buffer layers discussed before.

Influence on open-circuit voltage

The V_{oc} increases with increasing Type-III buffer layer thickness. The band diagram under open-circuit condition in Figure 5.21 shows that, similar to a Type-I buffer layer, a Type-III buffer layer also enhances the quasi Fermi level splitting as compared to the reference cell. It can again be ascribed to the fact that the Type-III buffer layer has larger ΔE_F than the *i*-layer under the same illumination condition, see Chapter 5.3.4.

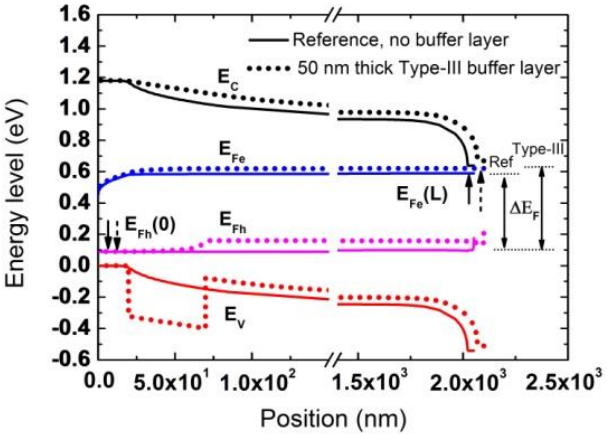


Figure 5.21: The band diagram of µc-Si:H cells having no (reference) and 50 nm thick Type-III buffer layer at the p/i interface under open-circuit condition.

Influence on fill factor

With increasing Type-III buffer layer thickness the simulated *FF* initially remains constant and then drops when the buffer layer thickness exceeds 10 nm, as shown in Figure 5.13(d). This corresponds to a slight decrease of the shunt resistance and an increase of the series resistance as shown in Table 5.7. The reason is the same as for the Type-I buffer layer, however the blocking effect due to the Φ_B^h is not that serious. If the Type-III buffer layer thickness is kept below 10 nm, the impact of the "blocking effect" is negligible.

In summary, similar to the Type-I buffer layer, a Type-III buffer layer does increase the V_{oc} with increasing buffer layer thickness. But it does not add serious side effects, such as a high recombination rate, high Φ_B^h ("blocking effect") and a weakening of the electric field within the bulk of the *i*-layer. Therefore, it slightly increases the J_{sc} (similar as the Type-IV buffer layer) and it does not harm the *FF* for buffer layer thicknesses smaller than 10 nm. Thus an approximately 10 - 20 nm thick Type-III buffer layer leads to a maximum efficiency improvement, see Figure 5.13(f).

5.5.4 Comparison of the impact of different types of buffer layers

As shown in Chapter 5.4.4, generally, an approximately 10 nm thick buffer layer (*i.e.* for Type-III and IV) introduced at the p/i interface gives the highest efficiency boost to the solar cells. In this section, the solar cells having 10 nm thick buffer layers of different types were selected for a comparison.

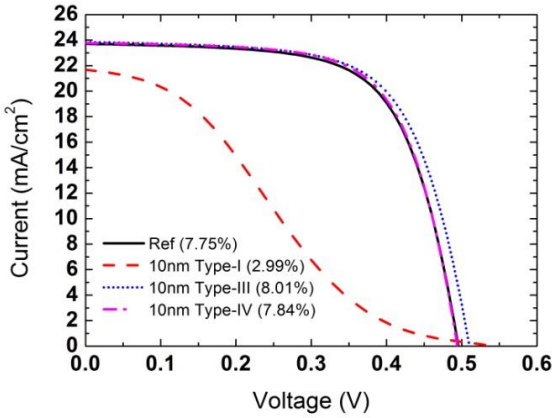


Figure 5.22: Comparison of the simulated *I-V* curves of a reference cell (i.e., no buffer layer) and cells with a 10 nm thick buffer layer (either Type-I or III or IV) at the p/i interface.

Figure 5.22 shows the simulated I-V curves of the selected solar cells. As can be seen, when a 10 nm thick Type-III or Type-IV buffer layer is introduced at the p/i interface, the cell efficiency gets a boost as compared to the reference cell. However, the Type-I buffer layer destroys the efficiency. Therefore, the efficiency trend is as follows:

$$\text{Type-III} > \text{Type-IV} > \text{Ref} > \text{Type-I}; \quad \text{(efficiency)} \tag{5.20}$$

These simulated results agree with the experimental result of Chapter 4.

Table 5.8 Summary and comparison of simulated *I-V* parameters of thin-film µc-Si:H solar cells having a 10 nm thick buffer layer of different type.

Buffer layer	E_{ff} (%)	V_{oc} (mV)	J_{sc} (mA/cm^2)	FF (%)	Φ_B^h (eV)	R_{sh} (Ωcm^2)	R_s (Ωcm^2)
N.A. (Ref)	7.75	495.0	23.70	66.00	0	1025	2.82
Type-I (10 nm)	2.99	541.8	21.67	25.43	0.621	165.6	97.4
Type-III (10 nm)	8.01	510.2	23.84	65.86	0.439	1045	2.99
Type-IV (10 nm)	7.87	494.2	23.78	66.94	0.08	932	2.74

Figure 5.23 compares the band diagrams under different conditions for the solar cells with a 10 nm thick buffer layer of different types. Under the dark equilibrium condition as shown in Figure 5.23(a), the introduction of the different buffer layers at the p/i interface mainly changes the band alignment near the p/i interface. It negligibly affects the band alignment in the other regions of the solar cell (i.e. the bulk of the i-layer and the region adjacent to the n/i interface) as compared to the reference cell (no buffer layer). The different types of buffer layer cause different effective barrier heights at the valence band near the p/i interface, as illustrated in Figure 5.23(a) by arrows. The corresponding Φ_B^h values are listed in Table 5.8. They show the following trend:

$$\text{Type-I} > \text{Type-III} > \text{Type-IV} > \text{Ref}; \quad (\text{effective barrier height, } \Phi_B^h) \qquad (5.21)$$

Figure 5.23(b) shows the influence of the different buffer layer types on the quasi Fermi level splitting in the solar cells, under open-circuit conditions. As shown in Chapter 5.3.5 and Eqn. (5.16), Type-I and Type-III buffer layers give the largest ΔE_F and the Type-IV buffer layer gives the smallest ΔE_F under the same illumination condition. Thus, the ΔE_F between the two terminals of the solar cells (or their V_{oc}) shows the following trend:

$$\text{Type-I} > \text{Type-III} > \text{Ref} > \text{Type-IV}; \qquad (\Delta E_F, \text{ or } V_{oc}) \qquad (5.22)$$

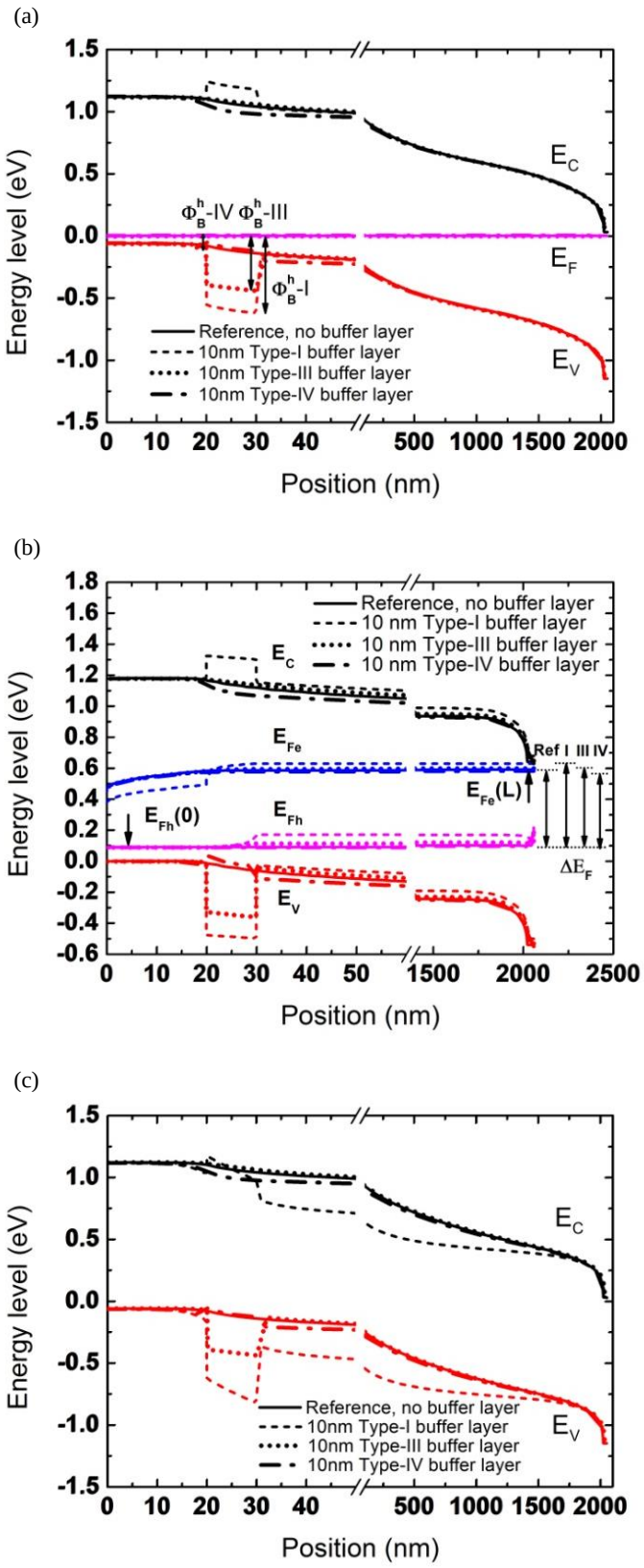


Figure 5.23: Comparison of band diagrams of the reference cell (no buffer layer) and cells with a 10 nm thick buffer layer (Type-I or III or IV) at the p/i interface under (a) dark equilibrium condition; (b) open-circuit condition; (c) short-circuit condition (quasi Fermi level E_{Fe} and E_{Fh} were removed for clarity).

Figure 5.23(c) shows the influence of the different buffer layer types on the band diagram under short-circuit condition. Type-III and Type-IV buffer layers only impact the band alignment near the p/i interface, but hardly change the band diagram in the bulk of the i-layer. The Type-I buffer layer causes a significant change of the band diagram, both near the p/i interface and in bulk of the i-layer. Especially in the bulk of the i-layer, it leads to flat bands and thus weakens the internal electric field. Considering the impact of the effective barrier height and the change of the band diagram, the short-circuit current and fill factor are influenced by the different types of buffer layers as follows:

$$\text{Type III} \approx \text{Type IV} \geq \text{Ref} > \text{Type I}; \quad \text{(short-circuit current)} \tag{5.23}$$

$$\text{Type IV} > \text{Ref} \geq \text{Type III} > \text{Type I}; \quad \text{(fill factor)} \tag{5.24}$$

Combining all the above effects, it follows that an around 10 nm thick buffer layer of type III gives the largest boost to the efficiency of the investigated µc-Si:H thin-film solar cells.

5.6 Summary

In this chapter, a systematic theoretical investigation of the influence of different types of buffer layers and their thickness variation on the I-V performance of µc-Si:H thin-film solar cells was carried out. Starting with the study of each single layer (i.e. µc-Si:H p-, i-, n- layer and Type-I, III and IV buffer layers), based on SRH recombination statistics, the relation between the generation rate and the excess carrier density was built up. Further, the interconnection between the minority carrier lifetime, diffusion length and quasi Fermi level splitting was determined and a brief comparison was made between each layer. Next, based on the calculated electrical parameters of each single layer, a numerical modelling was realized for µc-Si:H thin-

film solar cells having a p-i-n configuration (used as reference) and having different types of buffer layers being introduced at the p/i interface of the solar cell. By changing the buffer layer thickness, the impact of the different types of buffer layer on the I-V performance of the solar cells was obtained, i.e. investigating a type-I (a-Si:H) buffer layer, a type-IV (highly crystallized μc-Si:H) buffer layer and a type-III (a-Si:H with percolated μc-Si:H grains) buffer layer. The band diagrams (i.e. under dark equilibrium, open-circuit and short-circuit conditions), internal electrical field distribution and effective barrier height were used to analyse and explain the resulting changes of the I-V parameters of the solar cells by using the different types of buffer layers. The type-III buffer layer was shown to give the largest boost to the 1-Sun efficiency of the investigated μc-Si:H thin-film solar cells, due to its intermediate band gap (1.5 eV, compared to 1.8 eV for a-Si:H and 1.1 eV for μc-Si:H), its low defect density, its improved carrier mobility (compared to a type-I buffer layer) and due to its resulting moderate effective barrier height.

Chapter 6 Development of µc-Si:H thin-film solar cells[2] on TCO-coated textured glass superstrates (AIT glass)[3]

6.1 Experimental details for processing µc-Si:H thin-film solar cells on different superstrates

Three pieces of 10×10 cm^2 soda-lime glass sheets (3 mm thick) were used. Two of them were textured on one surface with the AIT method [25, 26, 150], the third was not textured (reference). By changing the Al thickness, reaction time and etching time, the surface morphology and the corresponding haze values of AIT glass sheets can be well controlled, see Ref. [38] for a detailed study. The surface morphology and haze values for visible light were measured using an atomic force microscope (Veeco, model DI-3100 Nanoman) and a digital hazemeter (BYK haze guard, model AT-4725, light source: tungsten lamp), respectively. The spectrally resolved haze values (ranging from 400 to 1200 nm) were measured by UV-VIS spectroscopy (Perkin-Elmer, Lambda 950). All three glass sheets (planar and textured) were cleaned with DI water and then coated with an aluminium-doped zinc oxide film (ZnO:Al or 'AZO'), using DC magnetron sputtering from a ceramic $ZnO{:}Al_2O_3$ tube target. Next, the AZO films were etched in a highly diluted HCl solution, leading to a nanoscale surface texture on the AZO films. Thus, one single-textured reference superstrate (planar glass covered with nanotextured TCO) and two double-textured AIT superstrates (microtextured glass covered with nanotextured TCO) were processed [38]. All glass sheets were then cut into two parts. Half of them were used as superstrates for thin-film solar cell fabrication, while the other half was used for

[2] The µc-Si:H thin-film solar cells studied in this chapter were processed at the "Photovoltaic Competence Centre Berlin" (PVcomB), an institute of the "Helmholtz-Centre Berlin" (HZB), Germany. The author is grateful for having been invited to PVcomB to do the µc-Si:H solar cell depositions.

[3] In July 2014, the content of this chapter has been submitted to the Journal of Non-Crystalline Solids for publication.

surface morphology characterisation. For solar cell fabrication, the AZO coated glass sheets were cut into 5×5 cm^2 pieces. They were then attached to a 30×30 cm^2 stainless steel sample holder and loaded into a conventional RF (13.56 MHz) PECVD system (Applied Materials, AKT 1600) for silicon thin-film deposition. Doped µc-SiO_x:H films, doped with either boron or phosphorus, were used as p-type or n-type hole/electron collecting layers of the p-i-n thin-film solar cell, with a target thickness in the range of 20 - 30 nm for the reference superstrate. The intrinsic µc-Si:H absorber layer (target thickness for the reference superstrate: 1.75 µm) was deposited at a temperature of 190 °C. It is emphasised that the resulting absorber layer thickness for the AIT glass superstrates is significantly lower (~1.5 µm), despite the fact that the same deposition run was used. This large thickness difference indicates a strong influence of the surface morphology on the film deposition by PECVD as, for example, highlighted in [151]. Next, a thin AZO film (~80 nm thick) combined with a 150 nm thick silver layer was deposited onto the thin-film silicon diode, serving as back surface reflector and rear contact of the solar cell. Finally, laser patterning was applied to define isolated cells with an area of 1.0×1.0 cm^2. The *I-V* characteristics of the cells were measured under standard test conditions (under an irradiance according to the AM1.5G spectrum and a controlled cell temperature of 25 °C), using a class AAA dual-light-source solar simulator (Wacom, WXS_156S_L2). In order to study local defect formation, cross-sectional images of the solar cells were taken by field emission transmission electron microscopy (XTEM, JEOL-JEM, 2010F). A focused ion beam (FIB, FEI NanoSEM 230) was used to create a cross section over an area of 20×3 μm^2 for EBIC measurement. During the FIB process, a "three-step cutting" method (ion current: 7 nA, 1 nA and 300 pA) was used to obtain a smooth cross section [152]. After the FIB process, the solar cells were placed onto a sample holder and sent to the SEM system (Carl Zeiss, model Auriga), where an EBIC system was attached to. Meanwhile, the two terminals of the solar cells were connected to the external current amplifier for the EBIC signal collection.

6.2 Surface morphology and haze of the superstrates

The surface morphology and the haze of different superstrates were investigated.

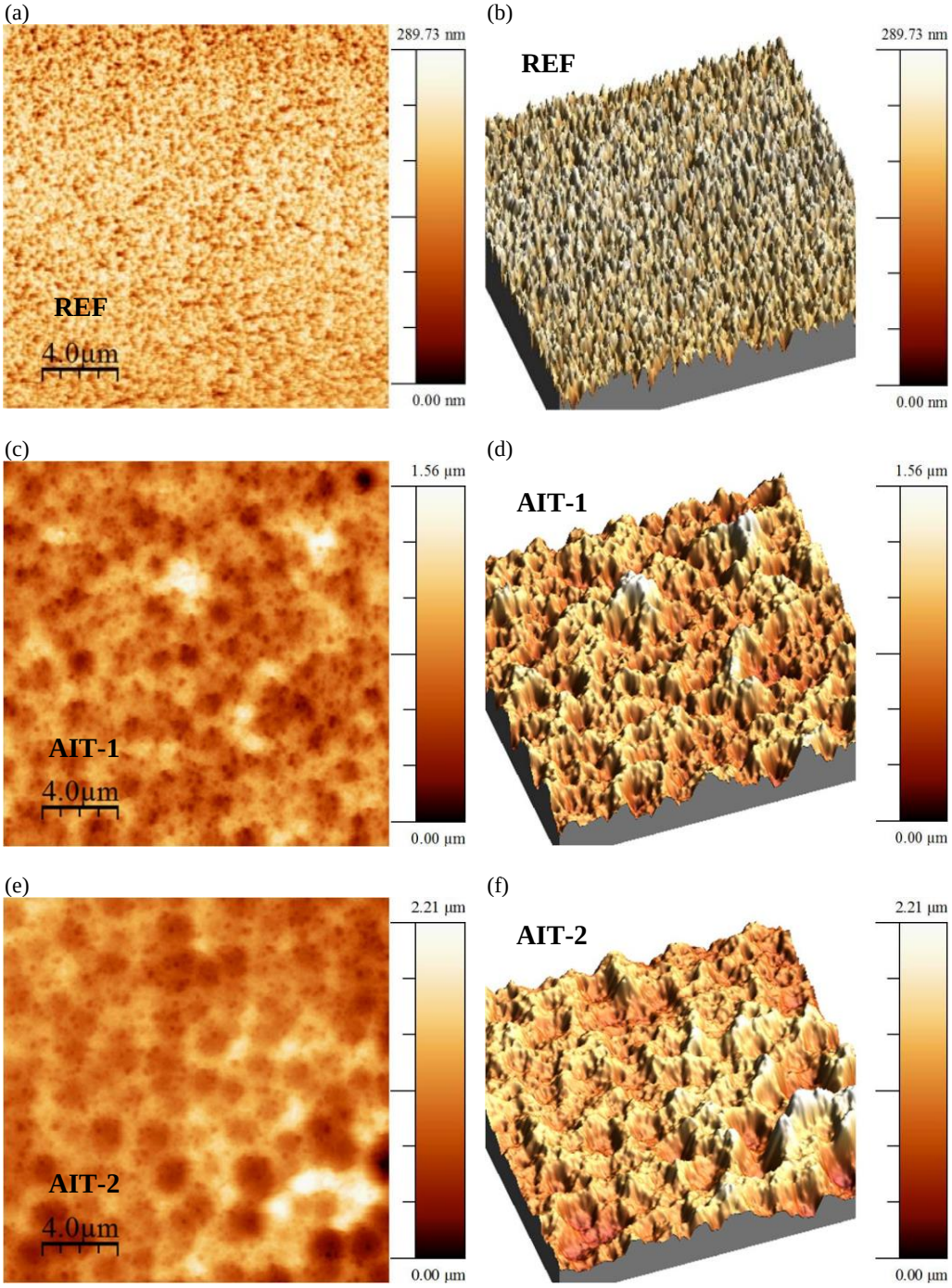


Figure 6.1: AFM images of the three different superstrates used in this study (a, c, e) in 2D format and (b, d, f) in 3D format. (a, b) Planar glass superstrate covered with nanotextured TCO (reference superstrate); (c, d, e, f) Microtextured AIT glass superstrate covered with nanotextured TCO. The AIT superstrate in (c, d) has an intermediate autocorrelation length *l* (mean feature size, i.e. 742 nm), while that in (e, f) has a large autocorrelation length (1050 nm).

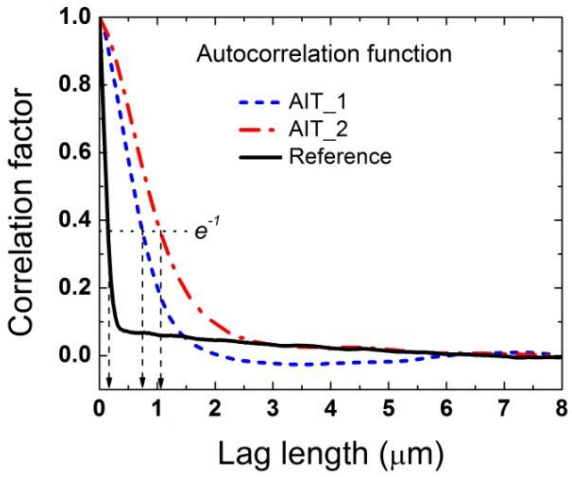


Figure 6.2: Determining the autocorrelation length *l* for the three different superstrates used in this study.

Table 6.1 Measured haze values of visible light and calculated surface morphology parameters for the different superstrates used. With the exception of haze, all parameters were measured after TCO deposition and TCO texturing, i.e. the AIT glass superstrates are double-textured (microtextured glass covered with nanotextured TCO).

	Reference	**AIT-1**	**AIT-2**
Haze (no TCO) (%)	0	50	70
Haze (with TCO) (%)	12	65	74
RMS (nm)	36	188	284
Autocorrelation length *l* (nm)	150	742	1050
Average surface angle (°)	20	40 (max at 30 and 50)	40 (max at 30 and 50)
Main feature size (nm)	100 - 500	600 - 2000	600 - 3000

The three different superstrates mentioned above were investigated by AFM. From the 20×20 μm^2 AFM images as shown in Figure 6.1, surface morphology information such as mean surface roughness, surface angle distribution and autocorrelation length were extracted, see Table 6.1. As compared to the reference superstrate (planar glass coated with nanotextured TCO), the AIT glass superstrates (microtextured glass

coated with nanotextured TCO) show quite different characteristics. As expected, the AIT samples have much higher surface roughness (RMS) than the reference sample (about 200 vs. 36 nm). Also the mean feature size of the textured superstrates (i.e., the autocorrelation length *l*) differs considerably: For the reference superstrate the autocorrelation length is as small as 150 nm, whereas the AIT-1 superstrate has a moderate autocorrelation length of about 750 nm and the AIT-2 superstrate has a large autocorrelation length of about 1050 nm, see Figure 6.2 and Table 6.1. Here, the autocorrelation length *l* is typically used as an indicator of the lateral feature size for randomly textured surfaces. The autocorrelation length can be derived from the autocorrelation function of the surface (referring to the correlation of a spatial series). The autocorrelation function is an indicator of spatial persistency (or similarity) of the surface structure to itself at two positions of the surface. The distance between these two points is called lag length [153]. Assuming that autocorrelation function can be presented by an exponential function, the autocorrelation length *l* is defined as the lag length for which the correlation factor equals to *1/e* (0.3678). As expected from the AFM images of the superstrates in Figure 6.1, the lateral feature size of the reference sample is much smaller than that of the AIT samples.

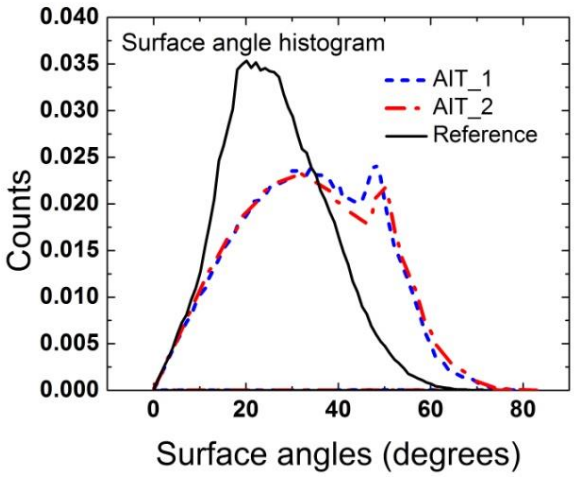


Figure 6.3: Surface angle distribution for the three different superstrates used.

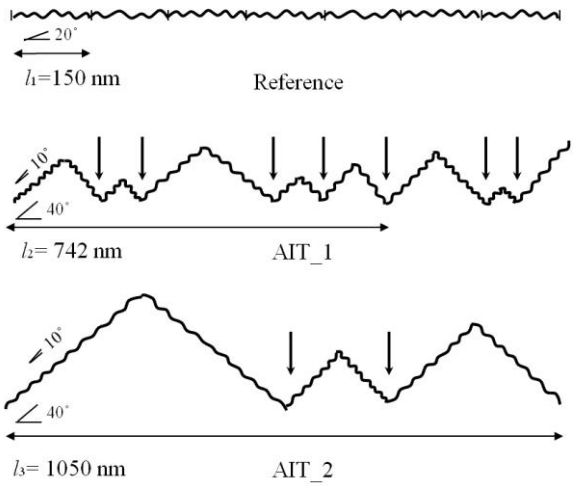


Figure 6.4: Schematic of the "simplified surface model" for the three different superstrates used.

Surface angle distributions were extracted from the AFM images, as described in [154], specifying the probability of encountering a specific surface angle between 0 degrees (flat surface) and 90 degrees (surface perpendicular to the substrate plane), see Figure 6.3. Interestingly, AIT-1 and AIT-2 have similar surface angle distributions. Both superstrates exhibit an average surface angle of 40 degrees, with a pronounced maximum at 30 and 50 degrees, respectively. Based on the extracted surface morphology data, a simplified surface morphology model describing the three different superstrates is proposed, see Figure 6.4. Referring to this simplified surface morphology model, the reference superstrate is nano-textured with an autocorrelation length (mean self-repeating feature size) of 150 nm and an average surface angle about 20 degrees due to the texture. The AIT glass superstrates are double-textured (microtextured glass and nanotextured TCO). They have an autocorrelation length (mean self-repeating feature size) of 742 or 1050 nm, respectively, an average surface angle of 40 degrees due to the microstructured glass and an additional average surface angle of +/- 10 degrees due to the superimposed nanotexture stemming from the etched TCO. Thus, the average surface angle in the nanotextured surface valleys ("kinks") of the double-textured AIT glass superstrates is either 30 or 50 degrees, see Figure 6.4. Furthermore, the number of "kinks" as well as the surface roughness

should correlate with the autocorrelation length *l* of the AIT glass superstrates (i.e. fewer "kinks" and higher surface roughness for AIT superstrates with higher auto-correlation length *l*).

"Kinks" are often found to be the sources of micro-cracks and thus also sources for recombination active regions within microcrystalline silicon solar cells [40]. They can also be sources for local shunt formation [127]. The schematic model clearly reveals that within a certain area, the AIT-1 superstrate (with moderate correlation length *l*) has a much higher density of "kinks" than the AIT-2 superstrate (with large correlation length *l*). This means that AIT glass superstrates with a larger auto-correlation length have a lower shunting probability for the fabricated µc-Si:H thin-film solar cells. The AIT-2 superstrate should therefore be less affected by local shunting, if used as a superstrate for µc-Si:H solar cell processing.

Haze measurements (diffuse scattering into air) for visible light (400 - 700 nm) were performed on the 3 superstrates, both before and after the application of the nanotextured TCO. Without TCO, the reference superstrate (planar bare glass) shows no haze at all, while the haze values of the two AIT superstrates vary significantly (50 % for AIT-1 and 70 % for AIT-2). After the application of nanotextured TCO, the haze values of the two AIT glass superstrates differ much less (65 vs. 74 %), despite the fact that the autocorrelation length of the two samples is significantly different (742 vs. 1050 nm). Compared to the haze of the reference superstrate (12 %), the haze of the AIT superstrates is much higher. Table 6.1 compiles the measured haze and surface morphology parameters of the three investigated superstrates.

Furthermore, the spectrally resolved haze was measured, see Figure 6.5. Considering µc-Si:H thin-film solar cells, the light scattering ability in the long-wavelength region (700 - 1100 nm) is most important. As can be seen in Figure 6.5, the haze values of the double-textured AIT superstrates improve significantly in the

long-wavelength region (compared to the single-textured reference superstrate). Therefore a stronger scattering of long-wavelength photons, and thus a higher short-circuit current enhancement ΔI_{sc} after µc-Si:H thin-film solar cell processing, can be expected for the AIT superstrates. Furthermore, it is expected that the AIT-2 superstrate will give a higher ΔI_{sc} than the AIT-1 superstrate.

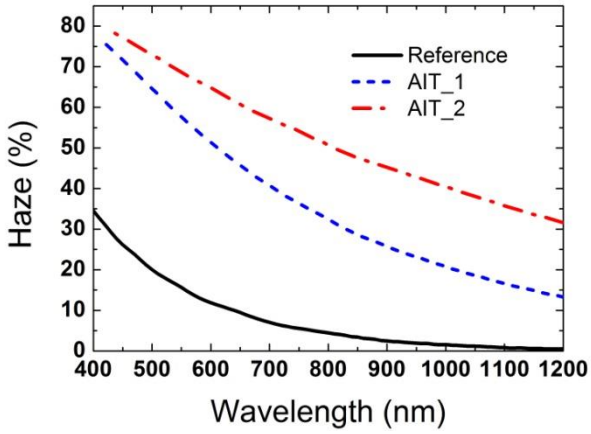


Figure 6.5: Spectrally resolved haze for the three investigated superstrates.

6.3 Microcrystalline silicon thin-film growth on the different superstrates

The growth mechanism of µc-Si:H films has been intensively studied and is well described by various growth models, such as the surface diffusion model [56], the etching model [57], and the chemical annealing model [58], see Chapter 2.1.2. These models stress the role of hydrogen atoms in the formation process of µc-Si:H, i.e. inducing a silicon network re-arrangement. Furthermore, the influence of the substrate on the initial µc-Si:H film growth (due to the different chemical nature of the substrates) has been studied [155-157]. More recently, the influence of the substrate surface morphology on the µc-Si:H film growth and on the resulting solar cell performance has been investigated [39, 40, 127, 158, 159]. In the present study,

XTEM images were taken to investigate the influence of the different surface morphologies of the used superstrates on the µc-Si:H film growth and structural composition. Furthermore, we highlight the significant difference of the µc-Si:H film growth behaviour on the specific surface provided by AIT process.

6.3.1 Microcrystalline silicon growth on the reference superstrate (planar glass covered with nanotextured TCO)

Microcrystalline silicon growth on planar or nanotextured planar substrates is well studied [69]. Typical columnar-shaped crystalline clusters (tapered columns with domed tops), separated by some low-density regions as sketched in Figure 6.6, are formed. This has been attributed to the low adatom mobility and to the growth death competition [160].

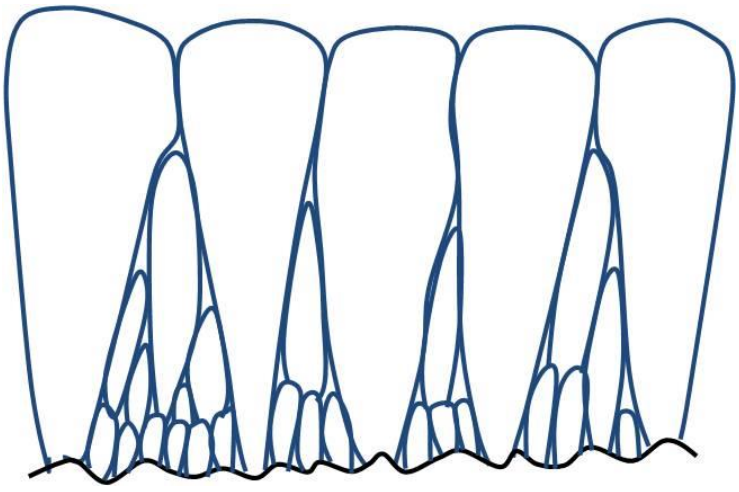


Figure 6.6: Schematic of columnar-shaped crystalline clusters resulting from µc-Si:H grown on the reference superstrate.

More recently, Teplin *et al*. attributed it to the different growth rates between the two different phases, as described by their "spherical cone model" [161, 162]. In the present study, the nanotexture of the TCO is too small to significantly alter the growth behaviour. Indeed, when depositing µc-Si:H on the reference superstrate, the

typical columnar shaped crystalline clusters were observed, see the dark-field XTEM image in Figure 6.7(a). The bright areas indicate crystalline regions whose periodic silicon lattices meet the Bragg condition, thus giving a diffraction effect in the TEM.

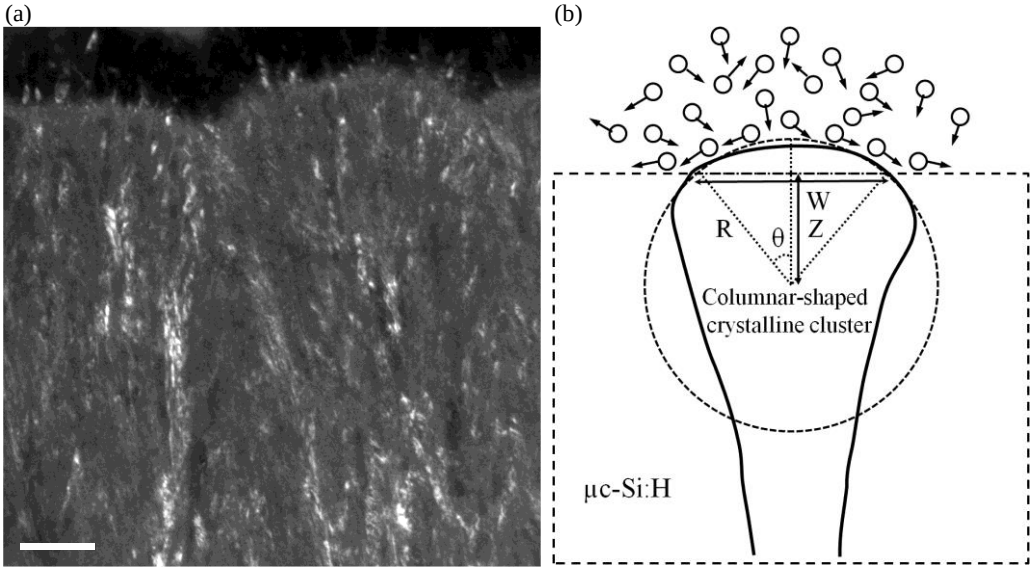


Figure 6.7: (a) Dark-field XTEM image showing the columnar-shaped crystalline clusters of Figure 6.6. (b) Schematic of the "spherical cone model" [161] describing the growth of µc-Si:H.

The obtained XTEM images can be analysed in order to extract the difference in growth rate for the two phases involved. According to the spherical cone model by Teplin *et al*. [161], the columnar shaped crystalline clusters observed in the µc-Si:H layer of Figure 6.7(a) and sketched in Figure 6.7(b) can be explained by assuming that the growth rate for the crystalline phase ($\gamma_{c\text{-}Si}$) is higher than the growth rate for the amorphous phase ($\gamma_{a\text{-}Si}$) during the µc-Si:H deposition process. This assumption is well supported by the etching model (hydrogen atoms tend to etch away the amorphous phase), as well as by the surface diffusion model (hydrogen atoms facilitate precursor transport from the amorphous phase to the crystalline phase). The difference of the growth rate between the two phases can then be estimated from the cone angle θ [161, 162], using Equation (6.1) (also see Figure 6.7(b)):

$$\cos\boldsymbol{\theta} = \frac{\boldsymbol{Z}}{\boldsymbol{R}} = \frac{\boldsymbol{\gamma_{a-Si}}}{\boldsymbol{\gamma_{c-Si}}} \;; \qquad (6.1)$$

where *R* is the radius of the cone and *Z* is the distance between the centre of the cone and the film surface. From Figure 6.7(a), *R* is about 480 nm and *Z* is about 330 nm. Therefore, θ is estimated to be 46 degrees. This means the crystalline phase grows about 30% faster than the amorphous phase. Furthermore, θ is a good indicator reflecting the surface diffusion of the precursors [163]. Generally, high surface diffusion will lead to a smooth surface and small θ. On the other hand, a large θ indicates poor surface diffusion, likely causing some voided structures in the film.

Summing up, according to our observations from XTEM images, the cone angle θ of the crystalline clusters formed within µc-Si:H is in the 40 - 50 degrees range if µc-Si:H is deposited onto our reference superstrate (planar glass covered with nano-textured TCO). This indicates that the crystalline phase grows 25 - 35 % faster than the amorphous phase. It also confirms results by Teplin *et al.* [162] obtained from AFM studies and thus supports the applicability of their "cone kinetics model" for the observed µc-Si:H film growth. However, it should be noted that θ will depend on the specific deposition conditions, like film thickness, silane concentration, substrate temperature and substrate morphology.

6.3.2 Microcrystalline silicon growth on the double-textured AIT glass superstrates (microtextured glass covered with nanotextured TCO)

It is well known that the growth of µc-Si:H is surface morphology dependent. As expected, the growth behaviour of µc-Si:H was considerably different when deposited onto the double-textured AIT glass superstrates (microtextured glass covered with nanotextured TCO). Fan-shaped crystalline silicon clusters were observed within the µc-Si:H films, as sketched in Figure 6.8(a). A corresponding XTEM image is shown in Figure 6.8(b).

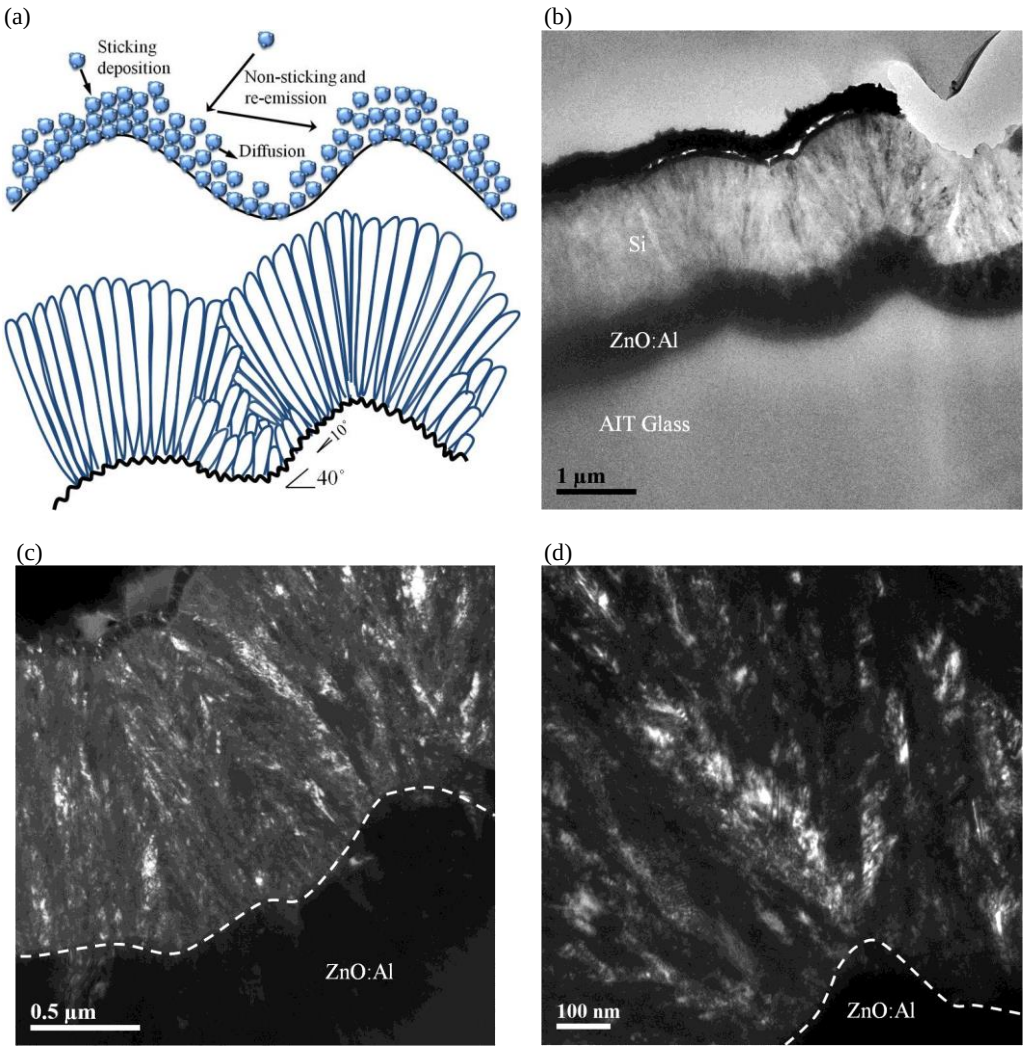


Figure 6.8: (a) Schematics of precursor deposition and fan-shaped crystalline clusters resulting from µc-Si:H grown on the double-textured AIT glass substrates (micro-textured glass covered with nanotextured TCO). XTEM images of (b) the whole structure (overview, 1 µm resolution), (c) µc-Si:H grown on the bottom and at the slope of a "hill" (0.5 µm resolution), (d) µc-Si:H grown of the on top of the "hill" (100 nm resolution).

Depositing onto planar or nanotextured superstrates, the µc-Si:H film growth can be well described by random fluctuation deposition and surface diffusion of the precursors [164]. However, if the superstrates are microtextured and the corresponding surface structures exhibit very large surface angles (like the AIT glass superstrates investigated in this work), the dynamics of the film growth becomes much more complex. In this case, effects like "shadowing" as well as "re-emission" must be taken into consideration [165]. Figure 6.8(a) illustrates the deposition process of precursors impinging on a very rough surface. Particles will more likely be captured

by the higher regions on the surface (leading to "shadowing" of the regions in the valleys). They can either stick to the surface or bounce off again ("re-emission"). All these combined effects will then determine the film growth.

The crystalline phase is observed to be always perpendicular to the local surface. According to the classical µc-Si:H growth model [166], the film's growth starts from well-separated nucleation centres followed by the coalescence of the initial nuclei. Later, it turns to the multilayer growth period, until finally its growth becomes stable and uniform. Under such a kind of growth mode, the crystalline phase will always be "perpendicular" to the local surface, as observed in Figure 6.8(c) (µc-Si:H growth on the "slope" of the microtexture induced by the AIT glass) and Figure 6.8(d) (µc-Si:H growth on top of a "hill" of the microtexture induced by the AIT glass). As a result, the growth of the crystalline phase will follow the superstrate surface morphology (i.e. the microtexture induced by the AIT glass) and finally the ensemble of crystalline clusters will turn fan-shaped, as illustrated in Figure 6.8(a) and (b).

The average cone angle θ of the crystalline clusters formed within the µc-Si:H layer is observed to be around 51 degrees when µc-Si:H is deposited onto AIT super-strates. Similar cone angles were observed for both AIT glass superstrates, i.e. AIT-1 (exhibiting a moderate autocorrelation length) and AIT-2 (exhibiting a large auto-correlation length). The observed average cone angle of 51 degrees is larger compared to the case where µc-Si:H is deposited on the reference superstrate (46 degrees). According to Equation (6.1), the ratio of $\gamma_{a\text{-}Si}/\gamma_{c\text{-}Si}$ decreases slightly if the film is deposited on AIT superstrates. This means the crystallinity of µc-Si:H films deposited on microtextured AIT glass superstrates is higher compared to the deposition on a nanotextured reference superstrate. This result can be confirmed by Raman measurements (Raman crystallinity). Similar findings have been reported for doped µc-Si:H(p^+) films [167]. Meanwhile, the larger θ of the µc-Si:H film grown on

the AIT superstrates indicates a poorer surface diffusion as compared to the film deposited on the reference superstrate.

Furthermore, the crystal size of the crystalline clusters (i.e. the width *W* of the crystalline phase in Figure 6.7(b)) shrinks if the µc-Si:H film is deposited on microtextured AIT glass superstrates. *W* gets as small as 100 nm (compared to 700 nm for deposition on a nanotextured reference superstrate, see Figure 6.7(a)), indicating that the film growth in the lateral direction was suppressed.

The observed difference in cone angle and size of the crystalline clusters formed within µc-Si:H film (deposited either on a reference superstrate or an AIT superstrate) can be attributed to much stronger surface etching caused by the incoming ion flux when the surface texture has a larger surface angle (as is the case for AIT glass superstrates), see Figure 6.9. It has been reported that ions play a key role in the µc-Si:H film growth [55] and that 70 % of the deposited film comes from the contribution of the ion flux as a main growth precursor [133]. At the same time, the ion energy has a great impact on the crystal size (*i.e.* high ion energy results in small crystallite size) [168]. Because of the electric field in the sheath, ions drift almost normally to the substrate and have narrow angular distribution of velocity [133], as shown in Figure 6.9. The effect of the ion flux E on the film can be divided into two parts. One is normal to the surface ($E_{\perp}$) and the other is parallel to the surface ($E_{=}$). $E_{\perp}$ causes ions to penetrate into the sub-layer and induces a structural relaxation of the silicon network. $E_{=}$ tends to etch the film surface. Generally, a moderate etching effect is beneficial to the formation of the crystalline phase and the creation of growth sites. However, in case the growing surface becomes very rough (*i.e.* the surface angle becomes very large, as is the case for the microtextured AIT glass superstrate), $E_{=}$ will increase and $E_{\perp}$ will decrease (assuming the same incident ion flux), see Figure 6.9. This means that surface etching becomes serious and finally can even suppress the growth of the crystalline phase. But at the same time, the amorphous phase suffers

even more from this etching effect, which results in the observed slight increase of the crystallinity when µc-Si:H is deposited onto AIT glass superstrates.

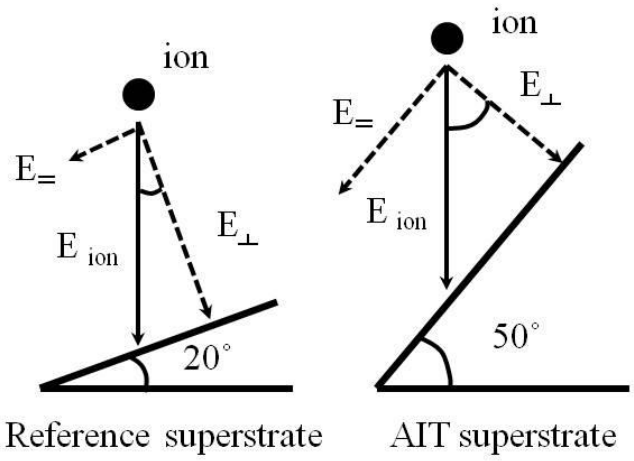


Figure 6.9: Schematic of ion flux impinging on the different superstrates used. Left: Reference superstrate (planar glass covered with nanotextured TCO), with an average surface angle of 20 degrees, Right: AIT glass superstrate (microtextured glass covered with nanotextured TCO), with a maximum average surface angle of 50 degrees.

Notably, the resulting film thickness also differs significantly if µc-Si:H is deposited onto a planar reference superstrate or onto a microtextured AIT glass superstrate: The µc-Si:H layers deposited onto the double-textured AIT glass superstrates are thinner (1.4 - 1.5 µm) compared to the layers deposited onto the single-textured reference superstrates (1.7 µm), for the same deposition time (i.e. using the same deposition run). This thickness difference can be attributed to the fact that the AIT superstrates have a larger surface area (around 13%) than the reference superstrate, see Table 6.2. This again stems from the larger average surface angle of the microstructured AIT glass. Furthermore, the re-emission processes on very rough (microtextured) surfaces also cause the precursors to take a longer time to settle, which reduces the deposition rate under otherwise identical deposition conditions.

Table 6.2 Surface area and thin-film thickness of µc-Si:H layers grown on the different superstrates used in this study (obtained from 20×20 µm^2 AFM and XTEM images, respectively).

	Reference	**AIT-1**	**AIT-2**
Surface area (µm^2)	461.0	516.3	520.3
Film thickness at the "top of a hill" (µm)	1.69 ± 0.02	1.52 ± 0.01	1.47 ± 0.02
Film thickness at the "bottom of a hill" (µm)		1.46 ± 0.02	1.36 ± 0.02

Furthermore, the thickness of µc-Si:H films deposited onto AIT glass superstrates is not homogeneous. Generally, in those regions where the microstructure of the AIT glass superstrate is elevated ("top of a hill" region), the µc-Si:H film will be thicker. This difference amounts to 50 nm for the AIT-1 superstrate (moderate autocorrelation length) and up to 100 nm for the AIT-2 superstrate (large autocorrelation length), see Table 6.2. A similar finding (thickness variation) has also been reported when the film was deposited onto silicon wafer substrates having a periodic honeycomb surface texture [86]. This difference can be explained by shading effects during the deposition. During the deposition, precursors have a higher probability of being deposited onto the "top of a hill" region, thus the growth rate in this region is higher. Hence, the crystalline phases in the higher regions grow faster and suppress the growth of those in the "bottom of the hill" regions. Furthermore, in the "bottom of a hill" region there is also a growth competition between the various crystalline phases stemming from the various surfaces involved: Due to constraints in space the crystalline phases with different growth direction compete against each other, thereby further slowing down the growth rate, see Figure 6.8(a) and (c). It is emphasised that especially in the "bottom of a hill" regions the collision of the different crystalline phases leads to the formation of grain boundaries with high defect densities, thus creating local recombination active regions within the µc-Si:H film. Even worse, such

regions are often the sources of micro-cracks and local shunts in the solar cell [40]. This will be studied in more detail in the following chapter.

Summing up, significant differences between µc-Si:H films deposited onto AIT glass superstrates and conventional superstrates were observed. The films on AIT glass are thinner, more inhomogeneous, more crystalline (but with smaller crystalline clusters), and probably exhibit more local defective regions. Obviously, results obtained on planar or nanotextured superstrates cannot directly be applied to superstrates with a microstructured surface texture (like AIT glass). Thus, an independent optimisation of the µc-Si:H deposition conditions using these microstructured superstrates has to be performed.

6.3.3 Tiny crack formation within µc-Si:H layers, grown on the double-textured AIT glass superstrates (micro-textured glass covered with nano-textured TCO)

The formation of tiny cracks and defective regions within the deposited µc-Si:H films is another important topic for solar cell applications, as these regions can cause local shunts within the solar cells. Python *et al*. [127] attributed the observed tiny cracks in µc-Si:H films deposited onto rough surfaces to the combination of strong shadowing effects, low surface diffusion length of the precursors, and selective etching of the amorphous phase. The surface morphology plays an important role in determining the formation of these cracks, such as surface roughness [40], average slope [158] and structure shape [39, 127], as well as the surface opening angle [40]. In this section, a further investigation on the crack formation will be carried out referring to the specific surface morphology of AIT superstrates (*i.e.* large surface angle and adjustable feature size). Local and extended defective areas ("cracks") are observed when depositing µc-Si:H films onto AIT glass superstrates, see Figure 6.10. A potential solution to reduce the probability of crack formation will be discussed.

If µc-Si:H is deposited onto very rough surfaces, its growth behaviour becomes more complex and it could even become a low-density or porous material. By analysing the XTEM images (see Figure 6.10), we explain the crack formation on the microtextured AIT surface as follow. In accordance to the literature [40, 127] and to our own experimental observations, local or extended defects ("cracks") will form above highly textured grooves, as observed in Figure 6.10(a) and (b) and sketched in Figure 6.11(a) and (b). Local cracks will form above V-shaped surface grooves with a small feature size *f*: As already discussed, the µc-Si:H film grows faster at the higher regions of the surface texture. If the feature size of the groove is small, the film finally closes up, thus preventing any more precursors from reaching the bottom regions and thus forming a porous structure, see Figure 6.10(a) and Figure 6.11(a). Extended cracks will form above V-shaped surface grooves with large feature size *f*: In that case there is a constant growth competition and extrusion between the growing neighbouring films, with their growth direction being directed against each other. When the growth fronts collide, they will cause a loose structure with high residual stress, see Figure 6.10(b) and Figure 6.11(b). In principle, cracks (local and extended) and defective regions should be detectable in electroluminescence (EL) measurements where they show up as dark spots within the EL images [159].

From Figure 6.3, the AIT glass superstrates have a large percentage of "V-shaped" surface textures with a surface angle of 50˚ or 30˚, respectively. Thus there will be many surface opening angles that are as steep as 180 – (2×50) = 80 degrees ("steep kinks") on the AIT glass superstrates. This is much smaller than the critical surface opening angle (110 degrees) proposed by Li *et al*. needed for crack or local shunt formation [40]. For comparison, the average surface opening angle for the reference superstrate is as shallow as 180 – (2×20) = 140 degrees, thus no - or much fewer - cracks or local shunts will form, see Figure 6.7(a).

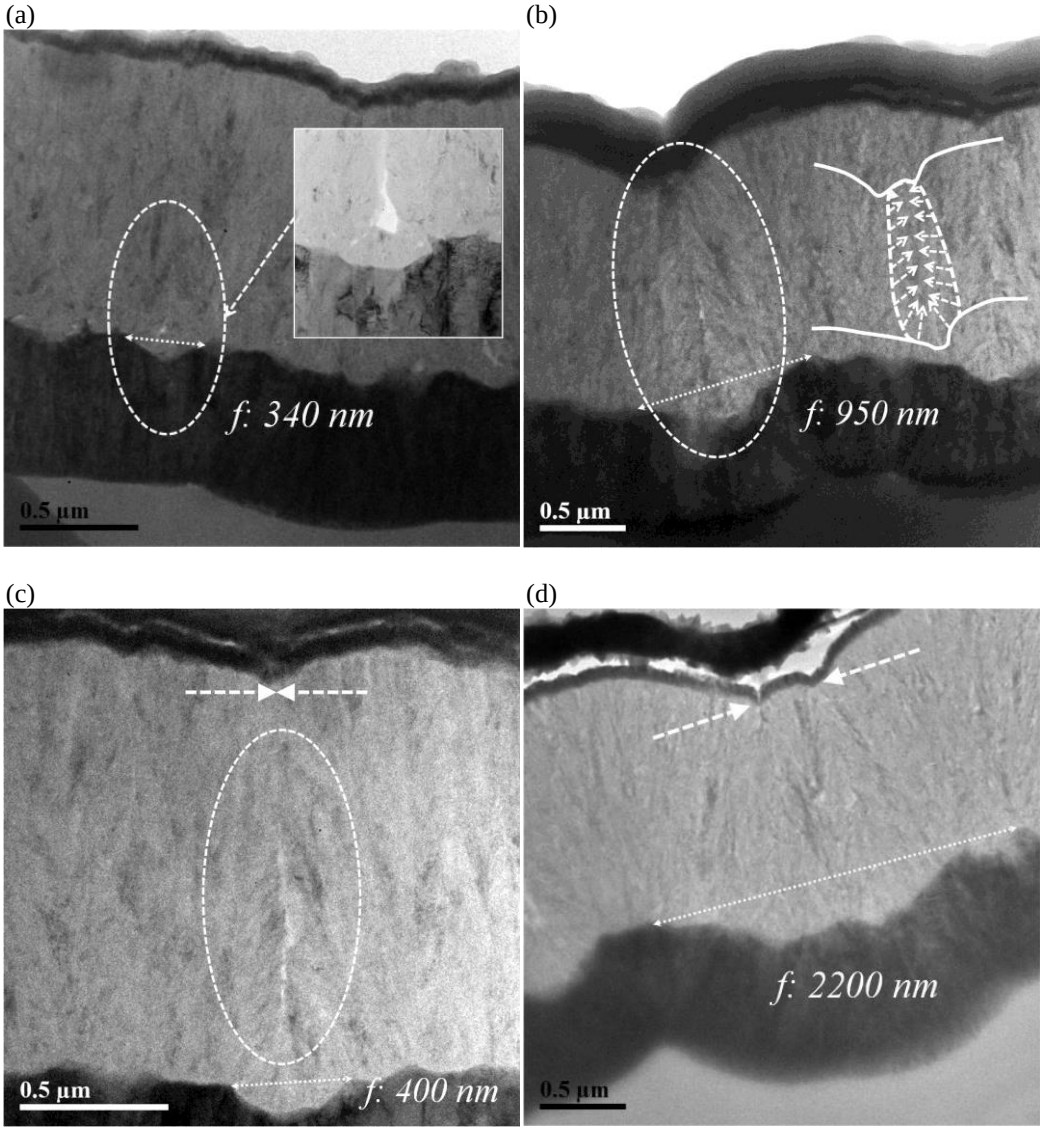
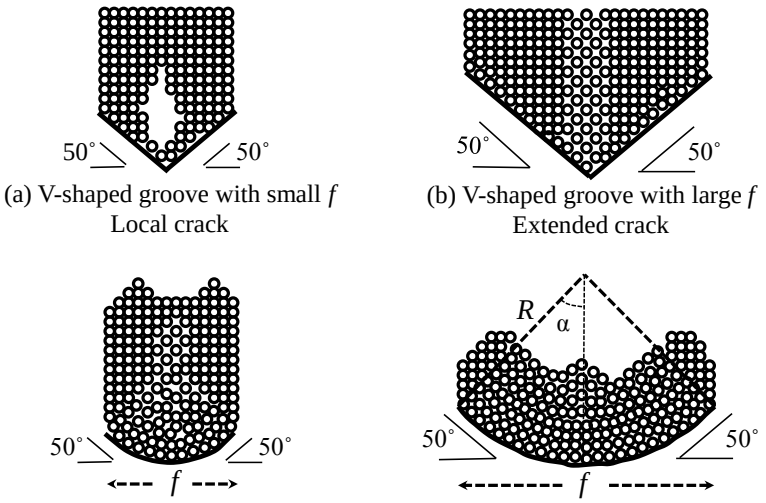


Figure 6.10: XTEM images showing the formation of cracks or defective areas within µc-Si:H layers grown on AIT glass superstrates (microtextured glass covered with nanotextured TCO). Two distinct surface morphologies can be observed, i.e. (a, b) steep "V-shaped grooves" and (c, d) "U-shaped grooves". V-shaped grooves cause local cracks if the feature size *f* of the groove is small (a), with typical *f* being in the 350 - 400 nm range, or they cause extended cracks if the feature size *f* of the grooves is large (b), with typical *f* being above 1 µm. U-shaped grooves cause local or extended cracks similar to V-shaped grooves if the feature size is small (c), however, no cracks were observed when the feature size *f* of the U-shaped groove was large (d). The arrows in (c) and (d) indicate the position of the growth fronts.

In general, AIT glass superstrates with moderate autocorrelation length *l* will have many more of such "steep kinks" than AIT glass superstrates with large auto-correlation length (i.e. AIT-1 has more "steep kinks" than AIT-2) within a certain area. Moreover, the "steep kinks" are considered to constitute the major source of

defect formation. These V-shaped grooves will cause (1) local cracks when the feature size *f* of the groove (the autocorrelation length *l* of the superstrate) is small; (2) extended cracks when the feature size *f* of the groove is large, see Figure 6.11 and XTEM images of Figure 6.10. Especially extended cracks which extend all the way up to the surface of the µc-Si:H layer are considered to be detrimental, as they can act as local shunts within the solar cell (providing paths for impurity diffusion and causing high local carrier recombination).



(a) V-shaped groove with small *f*
Local crack

(b) V-shaped groove with large *f*
Extended crack

(c) U-shaped groove with small *f*
Local crack

(d) U-shaped groove with large *f*
No crack

Figure 6.11: Schematic of crack formation within µc-Si:H layers grown on double-textured AIT superstrates (microtextured glass covered with nanotextured TCO). Left: V-shaped (a) and U-shaped (c) grooves with small feature size *f*, Right: V-shaped (b) and U-shaped (d) grooves with large feature size *f*. Crack formation will not occur for U-shaped grooves with large feature size *f*.

In reality, not only V-shaped kinks but also U-shaped kinks are observed for the AIT superstrates, see the XTEM images of Figure 6.10(c) and (d). It is because the observed surface angles do have a wide distribution, i.e. only the most frequently observed values are located at 50 and 30 degrees (see Figure 6.3). U-shaped grooves with small feature size *f* and steep opening angles of 80 degrees (which are frequently observed on the AIT-1 superstrate with its moderate autocorrelation length *l*) can also cause local or extended cracks, similar to the V-shaped grooves, as observed in

Figure 6.10(c) and sketched in Figure 6.11(c). The crack formation process will be analogous to the V-shape case discussed above. However, no cracks will be formed on U-shaped grooves with a large feature size *f* (which exist only on the AIT-2 super-strate, exhibiting a large autocorrelation length *l*). In this case, there is now enough space available for the film's growth and thus no serious film extrusion will occur, as observed in Figure 6.10(d) and schematically sketched in Figure 6.11(d).

Thus, steep V-shaped grooves are always detrimental. However, for steep U-shaped grooves, there exists a critical feature size *f* being associated to that groove, beyond which crack formation will be suppressed. In a previous study, Sai *et al.* [83] reported that crack formation is also influenced by the film thickness. For the AIT superstrates having very large surface angles, we further point out that, in order to avoid the film extrusion, it is necessary to prevent the collision of neighbouring growth fronts within the film, as indicated by the arrows in Figure 6.10(d). This requires the radius *R* of the U-shaped groove to be larger than the film thickness (*L*), as shown in Figure 6.11(d). In the case of the critical point (when $R = L$), a relation between the critical feature size *f* and film thickness *L* can be estimated:

$$f > 2\,\mathrm{L}\,\sin(\alpha); \tag{6. 2}$$

This means the feature size *f* should meet the above requirement in order to avoid the neighbouring film extrusion and the formation of cracks. In our case, the deposited µc-Si:H film thickness is $L = 1.4$ µm and the surface angle is $\alpha = 50^{\circ}$ for the AIT glass, thus the mean feature size *f* of the microtextured glass superstrates should be larger than 2.15 µm in order to suppress crack formation. If the targeted µc-Si:H film thickness becomes thicker, the mean feature size *f* should be increased accordingly. Aiming at micromorph thin-film solar cells (a-Si:H/µc-Si:H), the total Si film thickness *L* will generally exceed 2 µm. The average feature size *f* should thus be close to, or even larger than, 3 µm. In that case, however, it has to be investigated

whether a further extension of the feature size of the AIT superstrates will impact its optical scattering ability.

Summing up, local and extended cracks were observed when depositing µc-Si:H films onto AIT glass superstrates. Comparing the different AIT superstrates used, those with a larger autocorrelation length *l* are considered to be superior for thin-film solar cell applications: While showing similar (or even higher) haze, less local shunt formation can be expected, due to their surface morphology (i.e. fewer defect-creating "steep kinks"). A further enlargement of the autocorrelation length *l* of the AIT glass superstrates could further suppress local shunt formation. It has also been shown that increasing the substrate temperature improves surface diffusion of Si atoms (filling of the cracks) and is thus beneficial for the reduction of the crack density [169].

6.4 Microcrystalline silicon thin-film solar cells realized on the different superstrates used

Several 1-cm^2 µc-Si:H thin-film solar cells were processed on the three different superstrates discussed in the previous sections. Figure 6.12(a) and (b) show the corresponding one-sun *I-V* and EQE curves of the best µc-Si:H solar cells obtained on the various superstrates. Table 6.3 lists the extracted solar cell parameters.

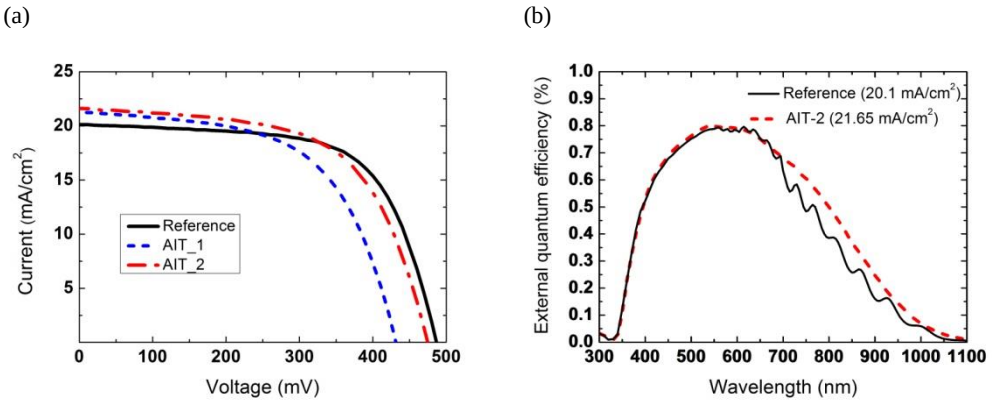


Figure 6.12: (a) Measured one-sun *I-V* curves of µc-Si:H solar cells processed on the three investigated superstrates; (b) External quantum efficiency of µc-Si:H solar cells processed on the reference superstrate and on the AIT-2 superstrate (the corresponding short-circuit current is indicated in the legend).

Table 6.3 One-sun *I-V* parameters of the best µc-Si:H solar cells processed on the three investigated superstrates.

Superstrate	J_{sc} (mA/cm^2)	V_{oc} (mV)	*FF* (%)	Rsh (Ωcm^2)	Eff (%)
REF	20.1	487	64.9	440	6.4
AIT-1	21.3	431	57.9	220	5.3
AIT-2	21.7	475	59.9	270	6.2

As expected, processing on double-textured AIT superstrates (microtextured glass covered with nanotextured TCO) does improve the light scattering within the solar cell: A significant J_{sc} increase of 1.2 and 1.6 mA/cm^2 (5.8 % and 7.7 % relative) was observed for the AIT-1 and AIT-2 superstrates, respectively, compared to processing on the reference superstrate (planar glass covered with nanotextured TCO), enhancing the short-circuit current density from 20.1 to 21.3 and 21.7 mA/cm^2, respectively. As expected, the current enhancement is mainly ascribed to the better light absorption for the infrared light (700 - 1100 nm), see the EQE curves in Figure 6.12(b), since the haze values in the long-wavelength region improved significantly by using AIT glass superstrates, as shown in Figure 6.5. Furthermore, given the fact that the µc-Si:H film thickness on the AIT glass superstrates (1.4 - 1.5 µm) is thinner than on the reference superstrate (1.7 µm), an even higher J_{sc} increase can be expected for identical film thicknesses. The AIT glass superstrate with the larger autocorrelation length, i.e. AIT-2 (which exhibits fewer "steep kinks" associated with local shunt formation), shows an even higher J_{sc} increase (compared to AIT-1). Further J_{sc} improvements seem possible by an optimisation of the AIT glass texturing process, aiming at an enhanced autocorrelation length l of the superstrates without affecting their light scattering abilities.

Thus, analysing only the measured ΔI_{sc}, using AIT glass superstrates clearly enhances the light scattering ability into silicon. However, analysing the resulting *I-V*

curves, all cells processed so far (even including the cells processed on the reference superstrate REF) do suffer from significant shunting. As expected, this shunting issue is much more severe if processing on AIT glass superstrates. Thus not only a shunt-induced steep slope in the 1-Sun *I-V* curves at low voltages is observed (for all three superstrates), in case of the AIT superstrates the low shunt resistance even affects the open-circuit voltage (and also the measured short-circuit current) of the solar cells, see Figure 6.12(a) and Table 6.3. In case of no shunting, the short-circuit current enhancement of the AIT superstrates ΔI_{sc} would be even higher than reported here. Again, in agreement with our expectations outlined above, the AIT superstrate with the larger autocorrelation length *l* (AIT-2) does suffer less from shunting compared to AIT-1. Indeed, defective areas ("cracks") were observed when depositing µc-Si:H films on AIT glass superstrates, i.e. above deep valleys ("kinks") which are induced by the AIT glass.

Further optimisation still needs to be done, i.e.: (1) Enhancing the autocorrelation length of AIT samples as much as possible, thus experimentally determining the maximum ΔI_{sc} possible from the use of AIT superstrates and simultaneously reducing the shunting probability. (2) Depositing different µc-Si:H thin-films onto the micro-textured AIT superstrates, which are better adapted to grow in a shunt-free way on a microstructured texture, i.e. using lower-crystallinity films. Generally, µc-Si:H films with crystallinity of 50 - 60 % are considered to be the best suited material for µ-Si:H solar cells (Ref. [132] and Chapter 4.1 of this thesis), when deposited on conventional superstrates (i.e. suitable for our reference superstrate, which is planar glass covered with nanotextured TCO). However, when deposited onto highly textured superstrates (i.e. on AIT glass), it is proposed to use lower-crystallinity films (40 - 50 %, with slightly poorer absorption of infrared wavelengths) or buffer layers [98]. Thus, it can be expected that by optimising the deposition conditions of µc-Si:H films on AIT glass superstrates, as well as the AIT process itself, it should be possible to

significantly reduce, or even eliminate, the local shunting problems experienced in our present experiments.

Based on the above analysis, µc-Si:H thin-film solar cells processed on AIT superstrates show a large potential to improve the PV efficiency, since (1) the improved light trapping (a higher short-circuit current density compared to a standard reference superstrate) has been proven by our experiments, and (2) a reduction or even elimination of the presently observed local shunt formation seems possible.

6.5 Electron beam induced current (EBIC) characterization of the structural defects observed within the µc-Si:H thin-film solar cells grown on AIT glass superstrates

In the previous chapters, a systematic investigation of crack formation in µc-Si:H films on AIT superstrates was performed. A fast and convenient characterization method is needed to detect the existence of these structural defects in the device. EBIC on FIB cross sections has been widely used in the field of integrated circuits (IC) for the purpose of failure analysis and device diagnostics [170]. Recently, the method was also applied to the study of solar cells, such as the determination of the junction location and depths [152], defect or dislocation detection [171], or the estimation of the minority carrier diffusion length [172]. Meanwhile, it was reported that this technology can also be applied to a-Si:H/µc-Si:H tandem solar cells, whereby the EBIC signal mainly comes from the µc-Si:H layers [173]. In this chapter, we demonstrate that this technology can be used for device diagnostics of µc-Si:H thin-film solar cells (processed on a single-textured reference superstrate or on double-textured AIT superstrates).

6.5.1 EBIC characterization of µc-Si:H thin-film solar cells processed on the reference superstrate (planar glass covered with nanotextured TCO)

During an EBIC (electron beam induced current) measurement, the locally induced current is collected from a charge carrier separating and collecting structure, such as a p-n junction or a Schottky barrier, while an electron beam is locally irradiating the sample and thus generating electron-hole pairs [174]. In the samples presented here, the electrons and holes are collected by the n/i and p/i junctions of the thin-film µc-Si:H solar cell, respectively.

Figure 6.13 shows cross-sectional images taken by a scanning electron microscope (SEM, using secondary electrons) combined with EBIC measurements, for a µc-Si:H thin-film solar cell processed on the reference superstrate (planar glass covered with a nanotextured TCO). A trench was milled using a focused Ga ion beam (FIB). The image in Figure 6.13(a) was obtained using a sample tilt of 52 degrees, so that the cross section of the solar cell can be 'illuminated' by the incoming electron beam. Figure 6.13(b) was obtained using EBIC, whereby the electron beam scanned across the entire area visible in the image. As can be clearly seen, the EBIC signal is limited to the silicon regions of the solar cell. Furthermore, the EBIC signal is strongest near the front region of the solar cell (i.e., the p/i interface), as expected for this type of cross-sectional image (note that the FIB milled exposed side wall has a very large surface recombination velocity, which affects the EBIC signal). Figure 6.13(c) shows the overlapped image combining the SE image and the EBIC image.

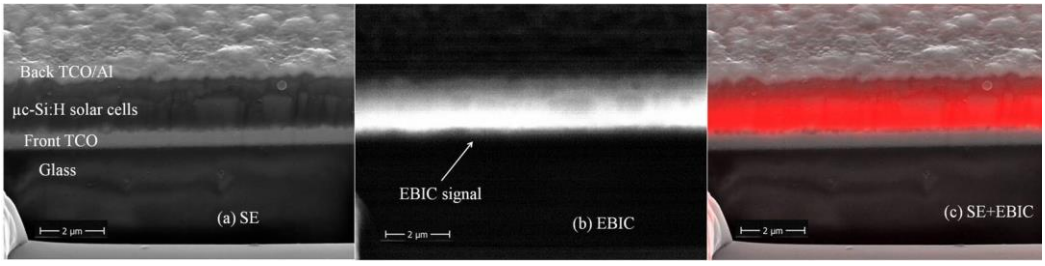


Figure 6.13: Cross-sectional images of a µc-Si:H thin-film solar cell processed on a reference superstrate (planar glass covered with a nanotextured TCO). (a) SE (SEM) image; (b) EBIC image; (c) combined SE and EBIC image.

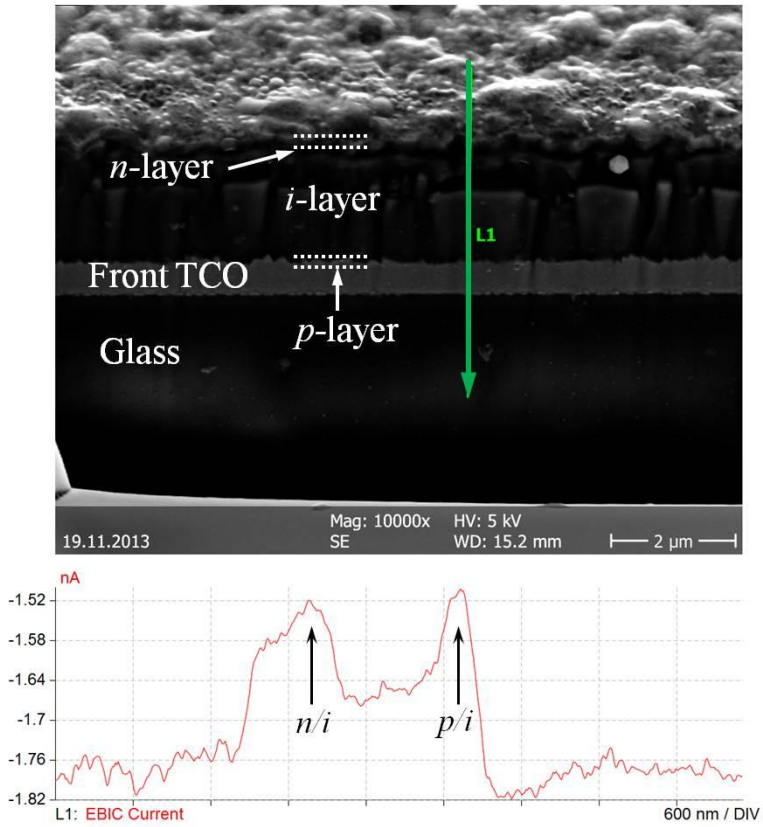


Figure 6.14: (Top) SEM image and (bottom) EBIC line scan of a µc-Si:H thin-film solar cell processed on the reference superstrate (planar glass covered with nano-textured TCO). The electron beam followed the line indicated by the arrow in the SEM image. The positions of the p/i and the i/n interfaces are indicated.

An EBIC measurement can also be performed using the 'line scan mode'. In this case, the electron beam irradiates along a certain direction and the collected current signal is recorded as a function of position. Figure 6.14 is an example obtained from the EBIC measurement under the line scan mode for a µc-Si:H thin film solar cell processed on the reference superstrate (planar glass covered with nanotextured TCO). The arrow in the graph indicates the line along which the electron beam was scanned. The resulting EBIC signal displays two peaks, which correspond to the locations of the p/i and i/n junctions. This is ascribed to the fact that the internal electric field within a µc-Si:H thin-film solar cell is highest near the p/i and i/n junctions (for comparison see also the simulated results of Figure 5.18(b)), and thus these regions have the highest charge carrier collection efficiency. Near these two junctions, the

EBIC signal will therefore be highest and thus these two peaks are good indicators for the junction locations. On a side note, the EBIC signal displays a very similar shape as the simulated internal electric field distribution shown in Figure 5.18(b). This is not surprising, since the internal electric field in the intrinsic μc-Si:H absorber layer and the charge collection efficiency as measured by EBIC are interconnected.

6.5.2 EBIC characterization of μc-Si:H thin-film solar cells processed on double-textured AIT glass superstrates (microstructured glass covered with nano-structured TCO)

In Chapter 6.4.1, it was shown that an EBIC measurement can be used for the determination of the location of the p/i and i/n junctions, using the line scan mode. Here, it will additionally be shown that EBIC can also be used for monitoring localized defects. Assuming that the defects which form above "kink-like" surface structures (see Chapter 6.3.3) are electrically active, these defective areas would show an enhanced recombination activity. Thus, locally generated electron-hole pairs in those regions would face a higher recombination probability and therefore a lower collection efficiency (corresponding to a lower EBIC signal). It can thus be expected that the EBIC signal will be lower in the "defective regions" compared to "good regions" of a μc-Si:H solar cell.

When the EBIC measurement is operated using the mapping mode (a scan over the whole cross-sectional area), a local contrast along the mapped solar cells should appear. The EBIC image can thus help to distinguish "good" from "defective" regions. This will be demonstrated in the following, by investigating the structural defects (tiny cracks or extended cracks) which form above the surface "kinks" of AIT superstrates (see Chapter 6.3.3).

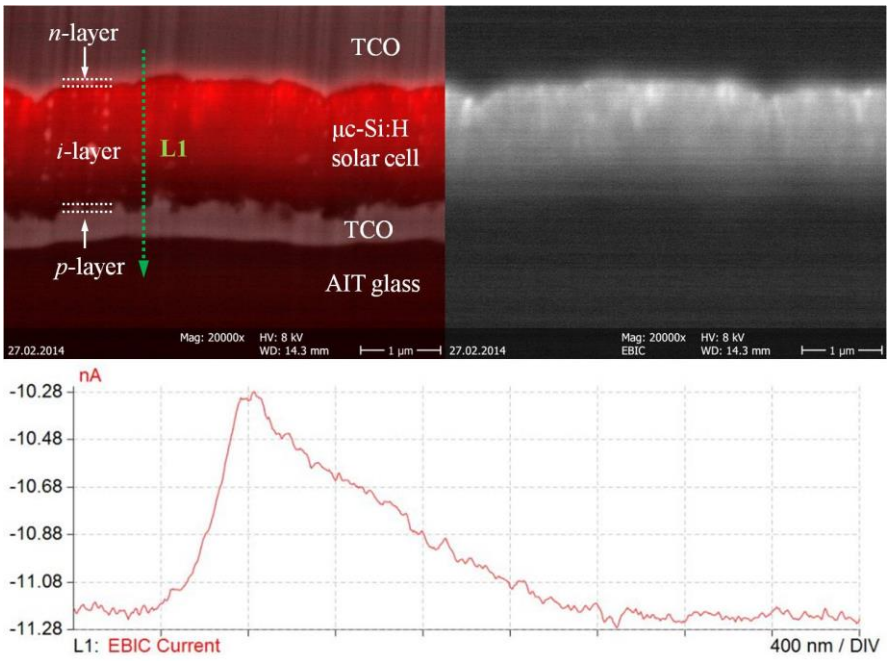
Figure 6.15 shows the combined SE-EBIC images (left) and the single EBIC images (right), as well as the EBIC line scans, for two locations where different types of structural defects have formed: (a) tiny local defects, i.e. “small surface cracks”, and (b) extended defects, i.e. a “large surface cracks” (for details see Chapter 6.3.3).

The electron acceleration voltage was 8 kV, which is the threshold voltage above which the EBIC signal starts to smear across the entire exposed cross section of the µc-Si:H solar cell.

As can be seen from the graphs, the regions with large EBIC signal follow the surface morphology of the superstrate. Compared to a µc-Si:H solar cell deposited onto a planar reference superstrate (i.e. having no microstructured surface “kinks”), the second peak indicating the p/i interface is missing for µc-Si:H solar cells deposited onto AIT glass superstrates, see Figure 6.15. This indicates defective regions close to the p/i interface, which are induced when growing µc-Si:H on a microtextured surface (as discussed in Chapter 6.3.3, compare Figure 6.10(a) and Figure 6.11(a)). These structural defects can be clearly observed using XTEM images, i.e. see Figure 6.10(a), but cannot be resolved using SEM. However, EBIC is able to resolve that these defects are electronically active (i.e. these are regions of high excess carrier recombination, thus there is no EBIC peak at the p/i interface).

In case of scanning an extended crack, which again can be resolved by XTEM, see Figure 6.10(c), but not by SEM, EBIC is now even able to resolve this defective region locally, see the “crack” in Figure 6.15(b). The EBIC line scan signal shows now only one sharp peak (corresponding to the n/i junction) and drops of significantly when reaching the area of the extended crack. The extended crack is electronically active, showing a very high local recombination rate, which can be detected by EBIC.

(a) Tiny local defects (“small surface cracks”)



(b) Extended defects (“large surface crack”)

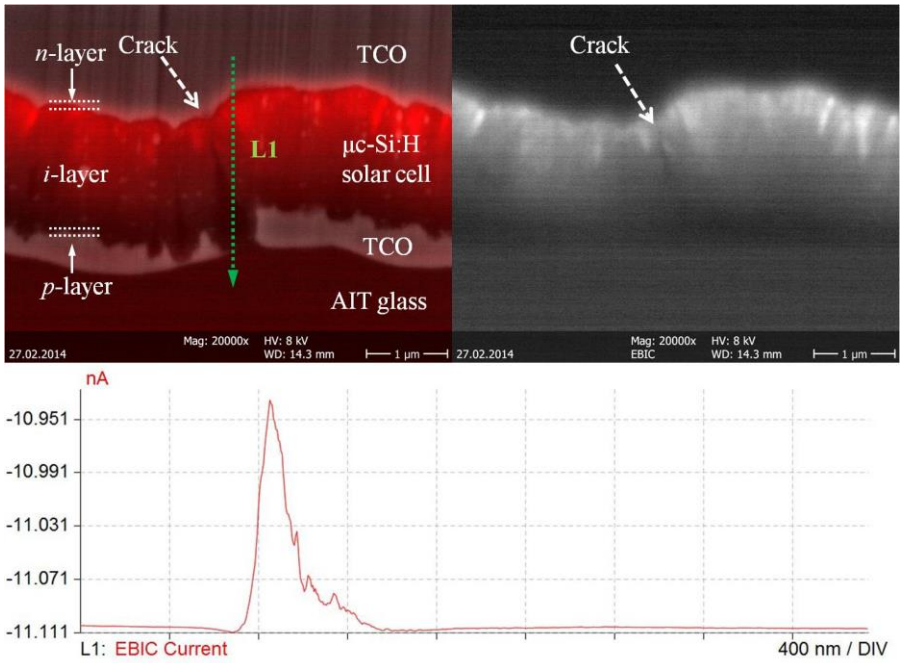


Figure 6.15: Combined SE-EBIC images (left) and corresponding single EBIC images (right) as well as EBIC line scans along the indicated green arrows (bottom) of µc-Si:H thin-film solar cells made on AIT glass superstrates, monitoring (a) tiny local defects, not resolved by SE but visible in EBIC (no peak related to the p/i interface), and (b) extended defects, which can be locally resolved by EBIC (“crack” in the EBIC image).

To sum up, in this section it was shown that the cross-sectional EBIC method can determine the material quality and detect defective regions which might form near the p/i interface of μc-Si:H solar cells on textured glass, by analysing the brightness contrast close to the p/i interface. The EBIC results clearly indicate that structural defects had formed during the μc-Si:H thin-film deposition onto microstructured AIT glass superstrates, and that these defects are electrically active. They cause a high recombination rate close to the p/i interface and might be the origin of the observed poor shunt resistance of μc-Si:H thin-film solar cells on AIT glass superstrates (see Chapter 6.4 and Table 6.3).

6.6 Summary

Microcrystalline silicon (μc-Si:H) thin-film solar cells were processed on aluminium-induced texture (AIT) glass superstrates. The influence of the surface topology on the optical scattering behaviour and on the μc-Si:H film growth was investigated, comparing a conventional reference superstrate (planar glass covered with nano-textured TCO) with two differently double-textured AIT glass superstrates (microtextured AIT glass covered with nanotextured TCO, exhibiting a moderate or a large autocorrelation length, respectively). Surface topology information, such as surface roughness, surface angle distribution and autocorrelation length (indicating the mean surface feature size), was extracted from AFM images. While the reference superstrate is single-textured, with a typical feature size of 300 nm, an autocorrelation length of 150 nm and an average surface angle due to the texture of 20 degrees, the AIT superstrates are double-textured, with a typical feature size of 1 - 2 μm, an average surface angle of 40 degrees (stemming from the microstructured glass) and an additional average surface angle of +/- 10 degrees due to the superimposed nanotexture. Scattering was investigated via haze measurements (scattering into air)

and via measurements of the short-circuit current enhancement (scattering into the silicon) relative to the reference superstrate (planar glass with nanotextured TCO). A significant haze increase was observed when using AIT superstrates, resulting in a short-circuit current enhancement of up to 7.7 %. However, local shunt formation also emerged. A decreasing shunting probability was observed to correlate with an increasing autocorrelation length (i.e., an increasing mean feature size) of the superstrate. XTEM was used to reveal the different growth behaviour of µc-Si:H films on different surface topologies, and to demonstrate the likely origin for the observed shunting (i.e. crack formation on top of V or U-shaped surface structures with a small feature size of < 1 µm). The crystalline clusters within µc-Si:H thin films deposited onto AIT glass superstrates have a slightly higher cone angle and thus a higher crystallinity, but a smaller crystal size (compared to depositing onto the reference superstrate, using the same deposition conditions). This can be attributed to the stronger surface etching of the incoming ion flux, given that the surface texture has a larger surface angle. The observed formation of tiny cracks (defective regions) on AIT superstrates exhibiting steep V or U-shaped surface structures was found to be dependent on the thin-film thickness L as well as on the autocorrelation length l of the superstrate. An increasing l will decrease the probability of local shunt formation. EBIC measurements proved that these structural defects are electrically active and that they cause a high (local) recombination in the device. A further enhancement of the autocorrelation length l (i.e., the mean feature size) of the AIT superstrates shows large potential to further improve the solar cell efficiency, i.e. by reducing the shunting probability while maintaining good light scattering abilities. Additionally, shunt formation can be further reduced by depositing films with lower crystallinity.

Thus, the use of double-textured AIT glass superstrates has a large potential to improve the efficiency of µc-Si:H thin-film solar cells.

Chapter 7: Summary and future work

In this thesis, the most important interfaces of μc-Si:H thin-film solar cells on glass superstrates were investigated to improve their PV efficiency: the interface which is most important for the electrical solar cell performance, i.e. the p/i interface, as well as the interfaces which are most important for the optical solar cell performance, i.e. the textured glass/TCO interface and the textured TCO/silicon layer interface. Furthermore, the influence of the surface morphology of the glass superstrate on the μc-Si:H film growth and on the solar cell I-V performance was investigated.

A "layer-by-layer" method was developed to fabricate thin (< 30 nm) boron-doped μc-Si:H *p*-layers with high crystallinity (above 60 %) and excellent conductivity (above 1 S/cm). Importantly, this method can be widely applied to many different types of superstrates, i.e. planar and textured glass (bare or coated with a TCO layer), with good control of the film crystallinity by changing the hydrogen treatment time and the number of cycles. Textured glass was prepared with the "aluminium-induced texture" (AIT) method, which is believed to be an industrially feasible method for PV applications.

The influence of a thin buffer layer inserted at the p/i interface of μc-Si:H thin-film solar cells on their electrical performance was experimentally investigated. Four different types of buffer layer were examined: (1) Type-I (a-Si:H) buffer layer, (2) Type-II (a-Si:H with isolated μc-Si:H grains) buffer layer, (3) Type-III (a-Si:H with percolated μc-Si:H grains) buffer layer, (4) Type-IV (highly crystallized layer) buffer layer, by using three different deposition methods: (1) standard a-Si:H deposition, (2) transition region deposition, (3) power profiling deposition. The following observations were made: The more amorphous phase is contained in the

buffer layer, the higher the open-circuit voltage (V_{oc}) of the solar cell. However, a significant drop of the short-circuit current (J_{sc}) and fill factor (*FF*) was observed using the Type-I buffer layer. In contrast, with increasing fraction of the crystalline phase in the buffer layer, the V_{oc} reduces but the J_{sc} and *FF* both improve, especially when the buffer layer was processed with "transition region deposition" conditions which cause less ion damage to the p/i interface. Finally, the Type-III buffer layer was shown to give the largest PV efficiency boost (around 15 % increase as compared to the buffer layer free reference cell).

With the help of numerical modelling, a theoretical analysis of the influence of the different types of buffer layers, and their thickness, on the I-V performance of the solar cells was performed. This theoretical analysis helped to explain the experimental observations described above. As a result, by means of experiments as well as simulations, a Type-III buffer layer (a-Si:H with percolated μc-Si:H grains) was identified as the best suited buffer layer for μc-Si:H thin-film solar cells.

The influence of different superstrate surface morphologies on (1) the optical scattering behaviour, on (2) the μc-Si:H thin-film growth, and on (3) the performance of μc-Si:H thin-film solar cells was investigated using different textured superstrates: A conventional reference superstrate (planar glass with nanotextured TCO) and two different double-textured superstrates (microtextured AIT glass covered with nano-textured TCO, exhibiting moderate and large autocorrelation length *l*, respectively). Compared to the reference superstrate, the AIT superstrates displayed a different surface morphology, i.e. a larger surface angle, a higher surface roughness, and a larger autocorrelation length. A significant haze increase was observed using AIT superstrates, resulting in a J_{sc} enhancement of up to 7.7 % compared to cells on the reference substrate. However, local structural defect formation also emerged in the films, causing local shunts and resulting in a PV efficiency degradation (despite the higher J_{sc}). A decreasing shunting probability was observed to correlate with an

increasing autocorrelation length of the AIT superstrates. XTEM was used to reveal the different growth behaviour of the μc-Si:H films on the different surface topologies, and to identify the origin for the observed local shunting. By further enhancing the autocorrelation length (i.e. the mean feature size) of the AIT superstrates, these superstrates have a large potential to improve the efficiency of μc-Si:H thin-film solar cells, by reducing the shunting probability while maintaining good light scattering abilities.

Recommended future work

There is still a large room for further improvements and new topics can be researched in future work.

① For example, boron-doped microcrystalline silicon alloys, such as μc-SiC:H [105-107] and μc-SiO_x:H [108-111], have attracted high attention in the past few years as they are considered a new promising window layer for silicon thin-film solar cells, which helps to reduce optical losses due to their large bandgaps.

② Furthermore, Bugnon (2014) reported that silicon oxide (SiO_x) can also be used as a buffer layer at the p/i interface of μc-Si:H thin-film solar cells and that it can significantly boost the PV efficiency [23].

③ In order to improve AIT glass superstrates for use in μc-Si:H solar cells, further optimization of its surface morphology with respect to reduced local shunt formation in the solar cells should be undertaken. Increasing the mean feature size of the surface texture seems to be a promising path.

④ Finally, further optimizing the μc-Si:H deposition process on AIT superstrates (i.e. reducing the crystallinity of the films) should be explored.

Appendix A: Plasma-enhanced chemical vapour deposition (PECVD) system used in SERIS

As shown in Figure A.1, the PECVD processes of this thesis were conducted in a parallel-plate plasma reactor that consists of a vacuum chamber, a pair of parallel electrodes, one power supply system, one gas supply system, one pumping system and one exhaust handling system.

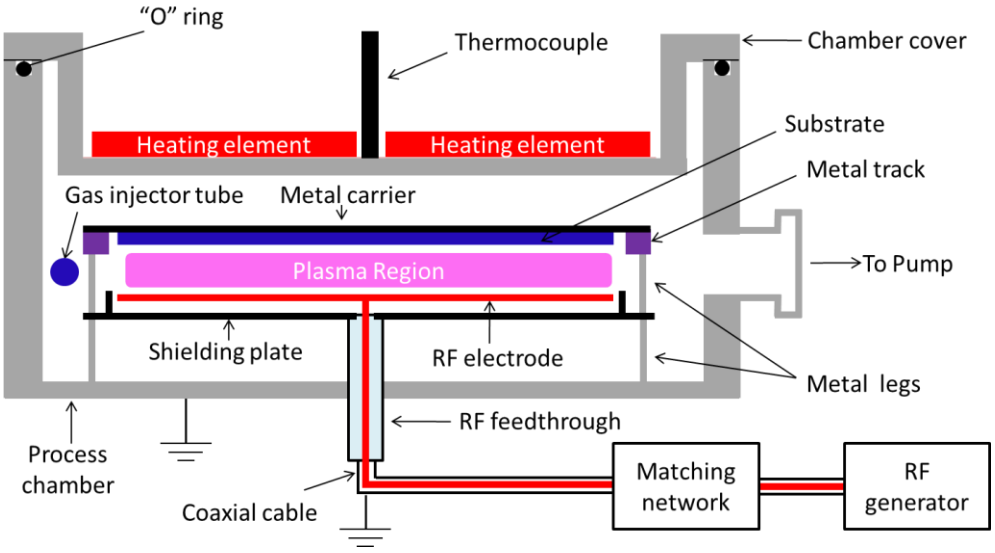


Figure A.1: Schematic of the PECVD system used in SERIS.

The PECVD reactor at SERIS used in the experiments of this thesis consists of the following components:

1. A vacuum chamber with a gas injector tube located on one side (called 'gas side'), allowing the gases to be injected into the chamber. On the opposite side ('pump side'), an exit connected to a turbo pump system from which the process gases are pumped out. Generally, the silane and dopant gas concentrations at the gas side are higher than on the pump side, if no shower head is used to distribute the gas flow. In this case, uniformity issues, such as thickness uniformity or crystallinity uniformity for µc-Si:H film, may exist and become more apparent as

the sample size increases. However, through optimizing the deposition conditions, such as properly lowering the gas pressure and rf power, the uniformity issue can be minimized.

2. A pair of parallel electrodes. One is earthed, while the other is driven by a 13.56 MHz rf generator. The glass substrate is mechanically clamped to the earthed electrode. In our system, this electrode is located near the top of the chamber and the sample substrate faces downwards. Such a configuration minimises the deposition of dust particles onto the samples, and thus minimises problems with pinholes or shunting paths in the deposited films. The directly powered electrode can also be designed as a shower head, to produce a uniformly distributed gas flow over the entire electrode area. Recently, in order to yield a uniform plasma over a very large area (larger than $1m^2$), a ladder-shaped electrode combined with phase modulation method was developed to fabricate uniform films [175-177]. In the PECVD process, the spacing between the two electrodes is a very critical parameter to determine the film quality. It limits the distance that radicals travel before reaching the film surface and affects the discharge-sustaining voltage V, which is a function of the product of gas pressure P and electrode distance d [178]. This phenomenon is well described by the famous "Paschen's law" and defined as:

$$\boldsymbol{V = \frac{aPd}{\ln(Pd) + b}}; \qquad \text{(A. 1)}$$

where the constants *a* and *b* depend on the composition of the gas. Generally, a small electrode distance *d* is preferred, to minimize the radicals residence time and avoid their gathering to form bigger clusters resulting in powder formation. In our experiments, d was around 15 mm.

3. A gas feeding system, which consists of many mass flow controllers, is used to control the gas flow rate. One should pay special attention to the difference

between the real gas flow rate and the value of the setting point. The offset may be different and dependent on the individual mass flow controller.

4. A RF generator and matching network. It supplies rf power to the electrodes generating the plasma. Both the standard industrial frequency (13.56 MHz) as well as a frequency in the VHF range (30 - 300 MHz) was available. In all experiments described in this thesis, a fixed RF frequency of 13.56 MHz was used.
5. Substrate heater: It is used to heat the sample to the required temperature. Generally, it is made up of several steel heating plates and heated up by electricity. The temperature is controlled by a PID temperature controller. There is also an offset between the real substrate temperature and the temperature value of the setting point. The offset was calibrated by the equipment supplier. According to the calibrated results, the substrate temperature is 100 - 120 °C lower than the setting point. When doing experiments, this offset must be taken into account. Actually, the real substrate temperature can have large variations during the deposition process, especially for μc-Si:H depositions using high discharge power and high gas pressure. During the PECVD process, some other factors which may influence the substrate temperature should also be taken into account, such as the problem of the heat transfer and dissipation in the vacuum condition and the fact that there is "plasma induced heating" (especially when the power density is very high) [179]. The target substrate temperature in our experiment was around 200 ˚C.

Appendix B: Establishing a baseline for µc-Si:H layers

B.1 Intrinsic µc-Si:H layer deposition

At SERIS, the µc-Si:H intrinsic (or 'undoped') layers, or *i*-layers, were deposited onto 30×40 cm^2 (A3 size) planar soda-lime glass sheets for optimization. A photograph of a sample is shown in Figure B.1(a).

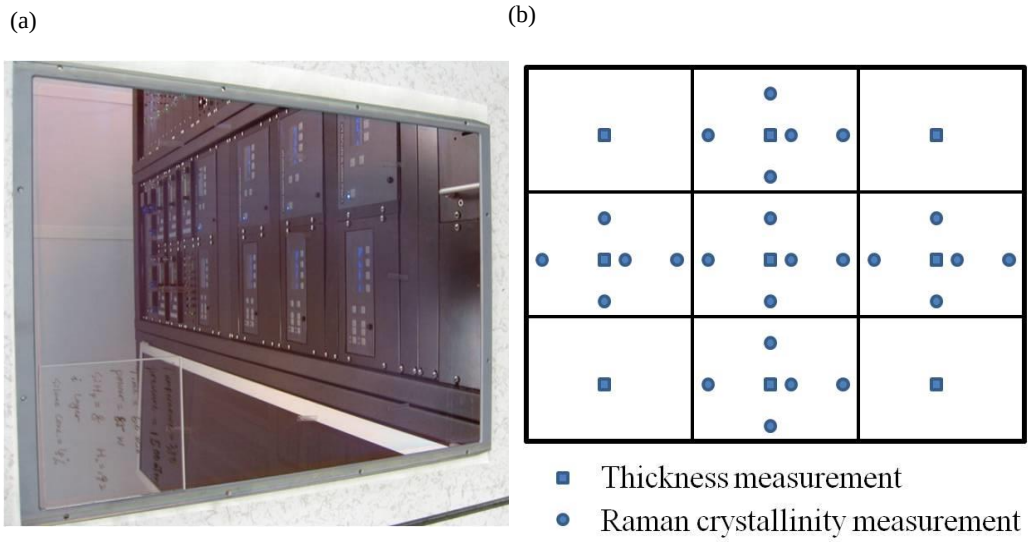


Figure B.1: (a) Photograph of a µc-Si:H film (deposition time 1 hr, film thickness ~400 nm) deposited onto a 30 × 40 cm^2 (A3) planar soda-lime glass sheet. (b) Selected positions for the thickness measurements and Raman crystallinity measurements. For these, the A3-sized sample was cut into 9 small pieces.

The A3-sized sample was divided into nine small pieces for various measurements. For film thickness measurement, stripes of Kapton tape were attached to the clean glass sheet at different places before the film deposition, as shown in Figure B.1(b) and labelled by squares. Before the film thickness measurement by using 'Stylus profiler' (Veeco, Dektak 150), the tapes were removed, locally exposing the glass. The stylus touched the sample surface and scanned from the exposed glass area to the film area. At the same time, the electrical signal due to the displacement of the stylus was recorded and displayed as a curve. When the stylus moved from the glass area to the edge of the film, the signal curve showed a very sharp step. The film thickness

can be estimated from the height of this step. The sample's crystallinity was estimated from Raman measurements, which is a non-destructive and fast optical method. The crystallinity derivation from the Raman measurements is described in Appendix E. Generally, five different points on each small sample were measured, as shown in Figure B.1(b) (see the circles).

The µc-Si:H *i*-layers were produced via PECVD, using a mixed gas flow of silane (SiH_4) and hydrogen (H_2). The silane concentration (SC), which is defined as the fraction of the silane gas (SiH_4) flow in the total gas flow (SiH_4 and H_2), is one of the most important factors for the growth of the µc-Si:H films, especially the crystallinity. To study its impact on the µc-Si:H film growth, the silane concentration was varied from 1 to 6 %, while all the other deposition parameters were kept fixed (*i.e.* input RF power 90 W, substrate temperature ~200 ˚C, pressure 1.8 Torr, deposition time 1 hour).

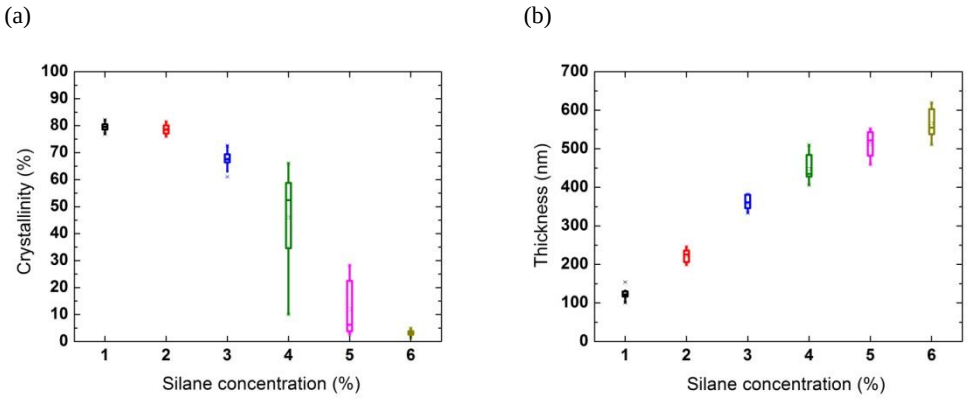


Figure B.2: (a) Raman crystallinity versus silane concentration (25 points were included in each condition); (b) Film thickness versus silane concentration (9 points were include in each condition).

Figure B.2(a) and (b) show the influence of the silane concentration on the Raman crystallinity and the thickness of the µc-Si:H films, respectively. With increasing silane concentration from 1 % to 6 %, a clear drop of the crystallinity of the films can be observed. In contrast, the film thickness increases nearly linearly.

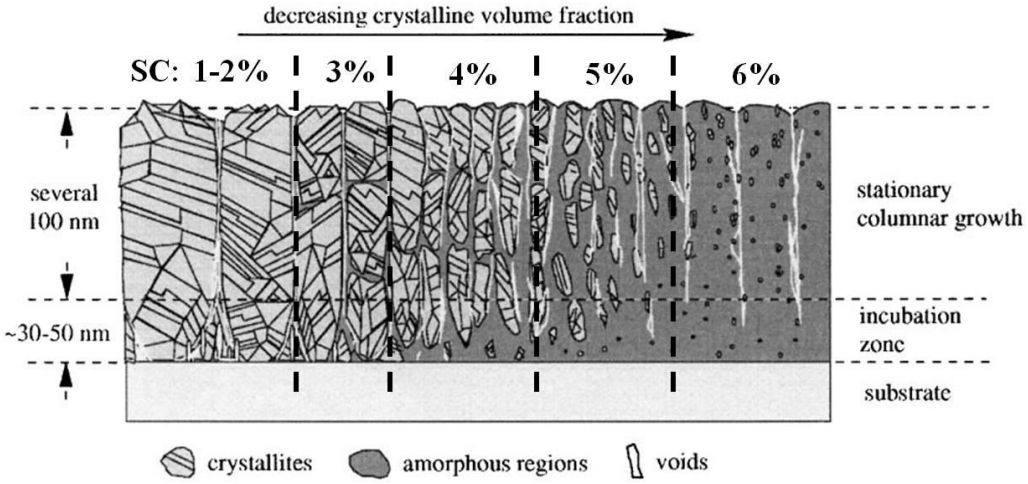


Figure B.3: Schematic of the crystallinity evolution of the μc-Si:H film vs. silane concentration (SC) [44].

Figure B.3 illustrates the material composition evolution process for the μc-Si:H film as the function of the silane concentration. In general, when the film was deposited under low silane concentration, it is apt to obtain highly crystallized films. As discussed in Chapter 2 for the growth mechanisms of μc-Si:H, high hydrogen gas flow provides a large amount of atomic hydrogen in the plasma and they tend to permeate into the sub-layer causing structural relaxation of the Si network. It facilitates the nucleation and therefore more nucleation sites are created. At the same time, the atomic hydrogen also tends to etch the film surface. The amorphous phase with weak Si bonding is apt to be etched away (this also limits the film deposition rate) and the crystalline phase with much stronger bond is left and keeping growing. Meanwhile, the etching effect also causes the H etched away from the grain boundaries and leaving more non-terminated bonds. Finally, the high H dilution in the plasma process results in a high crystallinity in the film and high defect density of grain boundaries. Thus, the film with high crystallinity (above 70 %) is not suitable for device fabrication and very low V_{oc} is obtained in this case. Once the silane concentration increases, the etching effect is weakened and more amorphous phases are contained in the film. The thin-skin of amorphous material can serve as a passivation layer of surface states reducing the paramagnetic defects in the film.

Meanwhile, the increasing silane gas provides more precursors (SiH_3) and enhances the deposition rate, which results in the increase of the film thickness as shown in Figure B.2(b). When SC reaches 6 % or above, the crystalline phase nearly disappears and only some nano-sized nuclei are embedded in the amorphous matrix, as shown in Figure B.3. Such transition state material is also called 'protocrystalline silicon'[180]. A very high V_{oc} (above 1 V) can be obtained if applying it in a-Si:H thin film solar cells [181-183].

As discussed above, if silane concentration keeps constant during the μc-Si:H deposition, a highly crystallized film is obtained at low SC and amorphous-rich film is obtained at high SC. For both of these cases are not suitable for μc-Si:H thin-film solar cell fabrication. Even at the intermediate SC (*i.e.* 3 - 4 %) which causes an intermediate crystallinity (40 - 60 %) at the end of the deposition, it still produces a thick incubation zone (about 30 - 50 nm) at the beginning of film growth for nucleation and crystallization (see Figure B.3). This thick amorphous incubation layer is harmful to the solar cell *I-V* performance, as also discussed and shown in chapter 4 about the Type-II buffer layer. As a result, in order to fabricate the μc-Si:H film with crystallinity around 50 - 60 % and keep it constant from the bottom to the top of the film, the silane concentration needs to be changed accordingly during the film deposition. At the very beginning of the film deposition, a low SC (*i.e.* 2 %) is needed to accelerate the nucleation and crystallization process and this deposited initial layer is called "seeding layer". Later, the SC can be gradually increased to the range of 3 - 4 % to control the film growth and make the crystallinity reach a certain range (*i.e.* 50 - 60 %). Prolonging the film deposition under SC of 3 - 4 % will lead to slow increase of crystallinity. As a result, in order to maintain the crystallinity within the target range (without further increase), a higher SC is used (*i.e.* 5 %) to suppress the further growth of the crystalline phase and keep this SC to the end of the film deposition. By doing so, a homogeneous film with constant crystallinity can be

obtained. And this deposition method is called “silane profiling method” or “hydrogen profiling method” (dependent on the way to change the silane concentration) as illustrated in Figure B.4.

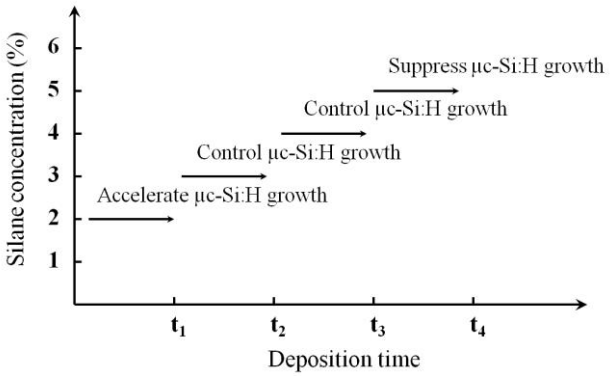


Figure B.4: Schematic of “hydrogen profiling method” (or “silane profiling method”). In general, by changing the silane concentration or the ratio between silane and hydrogen gas, the crystallinity of the film can be well controlled within a certain range.

Figure B.5(a) and (b) show the crystallinity and thickness distribution of the intrinsic µc-Si:H layer after three hours’ deposition on the A3-sized bare soda-lime glass sheet using above “hydrogen profiling method”. 45 points were measured from the sample and the contour plot was made by “Minitab 6”. In our PECVD system, no “shower head” was used to control the gas flow. Instead, a gas injector tube installed at the one side of the chamber was used to release the gases (called “gas side”). And the gases were pumped out from the other side of the chamber (called “pump side”). As a result, the silane concentration is always high at the “gas side” and becomes low at the pump side. As discussed above, the crystallinity and the thickness of the µc-Si:H film is largely impacted by the SC. Therefore, the crystallinity and the thickness have a gradient change over the sample from the “gas side” to the “pump side”, as shown in Figure B.5. It is not suitable to make “module” based on such non-uniform film. However, fortunately, within a certain area, the variations of the crystallinity and the thickness of the film are in an acceptable range. For example, in Figure B.5, a 20×20 cm^2 area was highlighted close to the pump side. Within this area,

which is large enough to make mini-module in the future study, the crystallinity variation is around 10 % and the thickness variation (Δ=[max-min]/[max+min]) is below 7 %. In this thesis, all the solar cells were selected from centre part of this area.

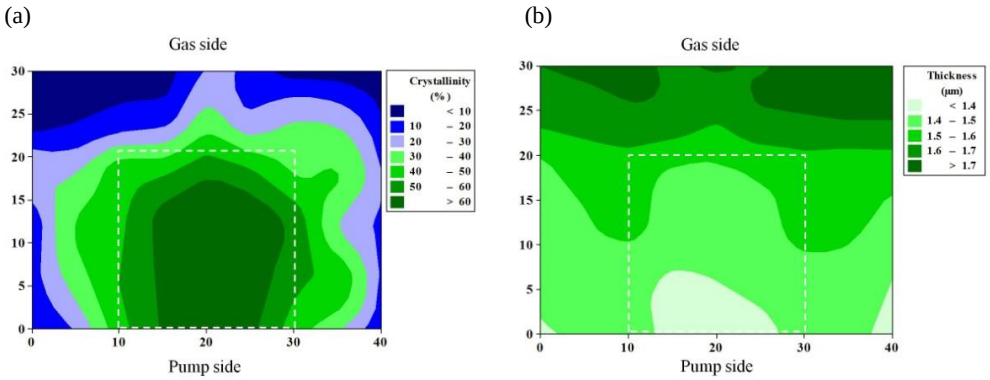


Figure B.5: (a) Crystallinity distribution and (b) film thickness distribution over the A3-sized sample (5 points × 9 pieces of small samples = 45 points were measured for mapping). The side of the sample close to the gas injector tube was marked as 'gas side'. The other side close to the gas exit was marked as 'pump side'.

B.2 Boron-doped μc-Si:H layer deposition

The growth of the μc-Si:H layer is significantly impacted by the deposition conditions, such as input power (or power density), gas concentration, excitation frequency, pressure, and temperature. In this section, it is selected several important deposition parameters for the study of their influence on the structural (crystallinity) and electrical (dark conductivity) properties of around 30 nm thick μc-Si:H *p*-layer. To study the influence of one parameter, other parameters are fixed (i.e. input power: 60 W; silane concentration: 2 % (SiH_4: 4 sccm, H_2: 196 sccm); 0.5 % B_2H_6 gas flow rate: 1.6 sccm; excitation frequency: 13.56 MHz; pressure: 1.2 Torr; substrate temperate: 200 ˚C; deposition duration: 20 min).

B.2.1 The influence of silane concentration

Silane (SiH_4) concentration is a very important parameter to determine the process of precursor deposition and plasma surface etching (more details see Chapter 2.2.2), which are the two critical factors to impact the crystallinity of the film. The influence of the silane concentration on the crystallinity of the *i*-layer has been well stated above. For *p*-layer, it takes the same effect. That is the high crystallinity can be obtained by using low silane concentration while crystallinity will decrease as the silane concentration increases. Besides, deposition rate increases as the silane concentration increases. Considering the both factors of high crystallinity and moderate deposition rate are needed, silane concentration of 2 % (corresponding gas flow rate: SiH_4: 4 sccm; H_2: 196 sccm) was selected for all the deposition of μc-Si:H *p*-layer (the same as *n*-layer) in this thesis.

B.2.2 The influence of input power

Figure B.6(a) shows the influence of the input power on the film crystallinity. Increasing the power enhances the crystallinity values at the beginning. However, further increasing the power will gradually spoil the crystallinity once the power exceeds a certain value (i.e. above 60 W as shown in the graph). To facilitate the nucleation and crystallization process, a moderate plasma surface etching is needed (see Chapter 2.2.2). A low input power can't supply sufficient ion energy for this etching effect and a low crystallinity will be obtained. The increasing power intensifies the etching effect and results in an improved crystallinity until it reaches a certain value. A stronger etching effect due to the further increasing power will break the crystalline silicon bonding and suppress the crystalline phase growth. In this case, the crystallinity decreases. It should be emphasized that the maximum crystallinity

value can be only obtained within a very narrow power range (i.e. 55 - 60 W in our experiment). Out of this range, only moderate or very low crystallinity values can be reached. We call this narrow power range as "process window", as highlighted in Figure B.6(a).

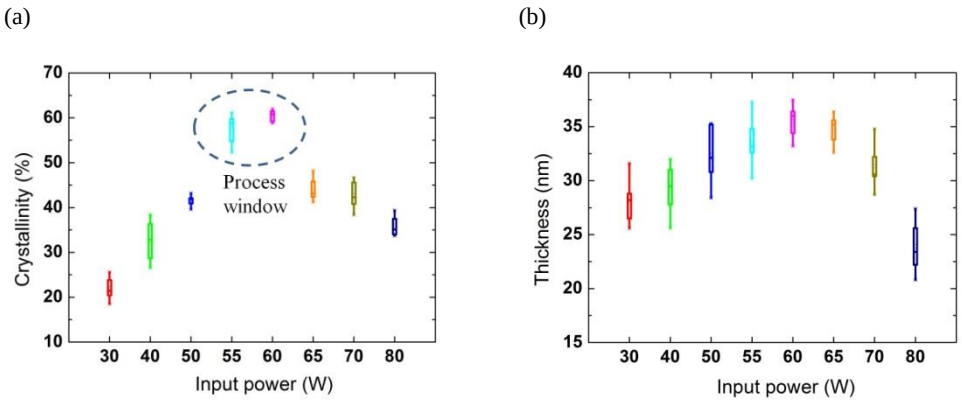


Figure B.6: The influence of the input power on the (a) crystallinity (25 data points were measured for each condition) and (b) thickness (9 data points were measured for each condition) of the *p*-layer.

The influence of the input power on the layer thickness is shown in Figure B.6(b). Increasing the power, on the one hand, decomposes more silane gas and creates more precursors (SiH_3), which tends to increase deposition rate or is called "deposition effect". But on the other hand, the plasma etching effect also intensifies, which tends to reduce the deposition rate. At the beginning, the "deposition effect" dominates and the deposition rate increases as increasing power. However, high power (i.e. reaching above 70 W) seriously intensifies the etching effect and finally reduces the deposition rate.

To obtain high crystallinity and good deposition rate, the input power of 60 W was selected and applied to all the *p*-layer deposition process.

B.2.3 The influence of the B_2H_6 gas flow rate

0.5% of B_2H_6 gas (diluted by H_2) was added into the silane and hydrogen gases to fabricate the *p*-layer. Figure B.7(a) shows that as B_2H_6 flow rate increases from 0.1 to 3.2 sccm, the crystallinity of the *p*-layer gradually decreases from 60 to 20 %. It is ascribed to the fact that boron atoms tend to remove hydrogen atoms from the surface of the film. And it is apt to prevent the nucleation and the crystallization process [112, 113]. Therefore, more B_2H_6 gas will spoil the crystallinity.

Figure B.7(b) shows dark conductivity improves as increasing the B_2H_6 gas flow rate to 1.6 sccm, but after that, the conductivity starts to drop if further increases B_2H_6 flow rate. The improvement of the conductivity at the beginning is contributed to the increasing doping concentration. And it further pushes the Fermi level to the valence band edge and reduces the activation energy. Later, the drop of the conductivity is ascribed to the fact that the crystallinity was spoiled by the high B_2H_6 flow as discussed above. Generally, amorphous phase has much poorer doping efficiency than crystalline phase in the film. Therefore, a reduced crystallinity causes a poor doping efficiency and lower conductivity even if more B_2H_6 gas was added into the mixed gases.

Besides, it was reported that the increasing B_2H_6 flow rate (or doping concentration) reduces the transmittance of the *p*-layer because B_2H_6 flow influences the layer crystallinity as discussed above [20]. Figure B.8 displayed the photographs of the as-deposited *p*-layers by using different B_2H_6 flow rate. As increasing the B_2H_6 flow rate from 0.8 to 3.2 sccm, the layer crystallinity reduces significantly, as shown in Figure B.7(a), and the colour of the layer changes from light yellow to deep yellow. Especially for the heavily doped layer shown in Figure B.8(c), it shows reddish when B_2H_6 flow rate reaches 3.2 sccm. It is a typical sign of amorphous layer or layer with low crystallinity, having relatively high absorption coefficient. Therefore, to reduce

the optical loss in *p*-layer, it is proposed to reduce the B_2H_6 flow and make balance with the doping efficiency.

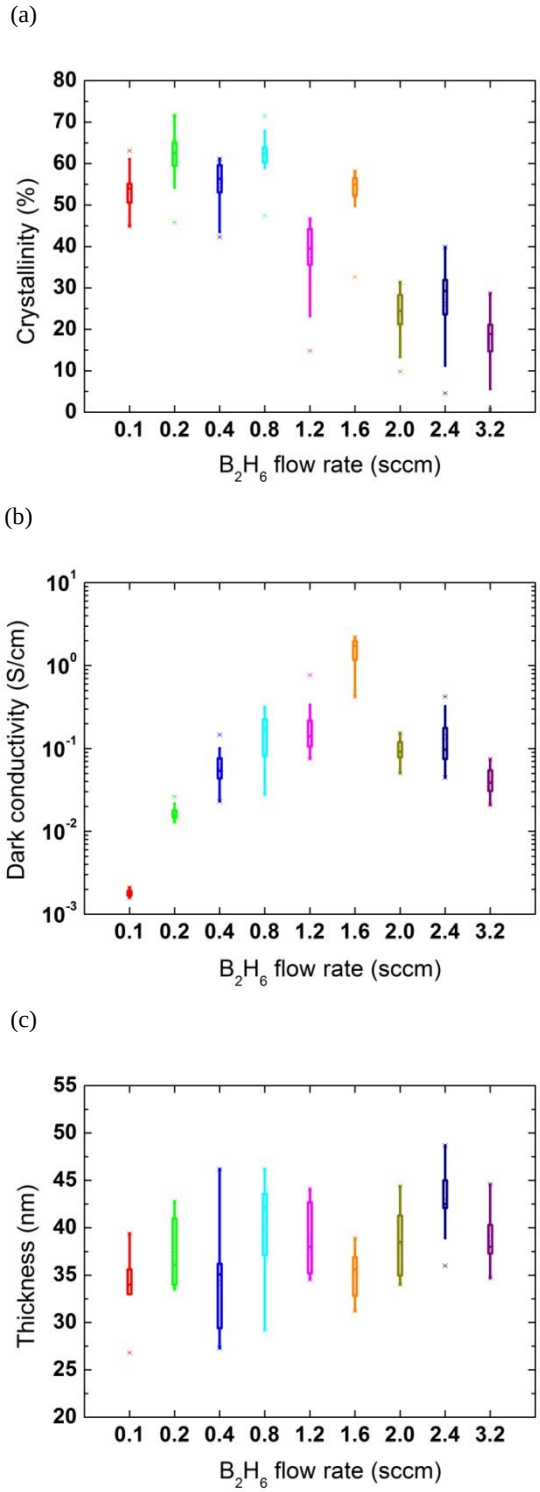


Figure B.7: The influence of the B_2H_6 gas flow rate on the (a) crystallinity (25 data points were measured for each condition) (b) dark conductivity (9 data points were measured for each condition) and (c) thickness (9 data points were measured for each condition) of the *p*-layer.

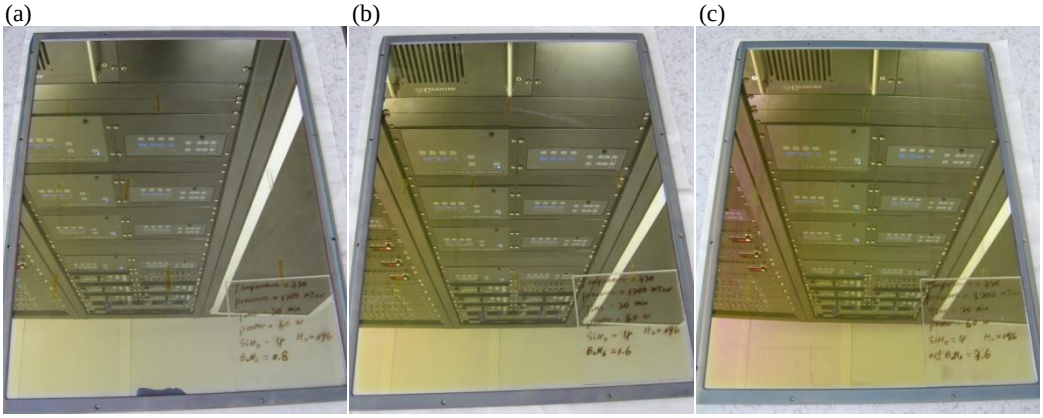


Figure B.8: Photographs of the *p*-layer (on bare planar soda-lime glass sheet) produced by SiH_4, H_2 and B_2H_6 mixed gases with different B_2H_6 gas flow rate: (a) 0.8 sccm (b) 1.6 sccm (c) 3.2 sccm.

Figure B.7(c) shows the increasing B_2H_6 flow slightly increases the layer thickness, which indicates a slight increase of deposition rate.

In this thesis for *p*-layer study, B_2H_6 flow rate of 1.6 sccm was selected for *p*-layer deposition because it contributes the maximum conductivity. However, for the solar cell fabrication, to reduce the optical loss, it will be reduced to around 1 sccm, which can also provide a relatively high conductivity.

B.2.4 The influence of other factors

Except for the above as-discussed deposition parameters, other factors, such as excitation frequency, substrate temperature, pressure, can also influence the structural and optical properties of the μc-Si:H *p*-layer. For example, by using very high frequency (VHF), it largely increases the deposition rate and grain size [45, 67]. By changing the pressure, the "process window" discussed in section B.2.2 will shift [184]. Besides, the growth of the μc-Si:H layer is also superstrate-dependent, due to the different chemical nature of the different superstrates [155, 156]. As a result, it is very likely that the layer properties (i.e. crystallinity and conductivity) will be

different if deposited on the different superstrates (i.e. bare glass and glass coated with TCO) even under the same deposition conditions. To solve this problem, a "layer-by-layer" method was developed and discussed in chapter 3 to further optimize the *p*-layer deposition.

B.3 Phosphorous-doped μc-Si:H layer deposition

The impact of the deposition conditions on the structural property and electrical property of μc-Si:H boron-doped p-typed layer has been discussed in chapter B.2. The similar optimization process can be also applied to μc-Si:H phosphorous-doped n-typed layer. For n-layer, very similar phenomena can be observed as stated in the above study for p-layer. The related experiment results have been published in Ref [184]. However, unlike the fact that the boron atoms tend to remove the hydrogen from the film surface and prevent the crystallization [113], phosphorous doesn't have such problem and μc-Si:H n-layer is much easier to reach high crystallinity. As a result, it is much easier to be doped and the conductivity of μc-Si:H n-layer can reach as several times higher as μc-Si:H p-layer under the same situations, i.e. the same layer thickness and doping concentration.

In this thesis, the deposition parameters used for μc-Si:H n-layer were listed as followed: Silane concentration 2 % (silane gas flow rate: 4 sccm, hydrogen gas flow rate: 196 sccm); Phosphine (PH_3) gas flow rate: 0.8 sccm; Input power: 55 W; Pressure: 1.5 Torr; substrate temperature: 200 ˚C.

Appendix C: Material parameters used in the simulation

Table C.1 The material parameters for each layer used in the simulation. E_g is the mobility bandgap; Nc and Nv are the effective density of states in the conduction and the valence band. E_F is the Fermi level measured from the valence band. E_i is the intrinsic Fermi energy. n_i is the intrinsic carrier concentration. n_0 and p_0 are the electron and hole concentration under equilibrium condition. μ_e and μ_h are the electron and hole mobility in the extended states. χ is the electron affinity. ε is the relative dielectric constant. E_{char} is the characteristic energy defining the exponential slope of the tail states. N_{Emob} is the density of states at the conduction band or valence band edge. σ_{neut}, σ_{neg}, σ_{pos} are the electron/hole capture cross section in neutral/charged tail states. E_{corr} is the correlation energy of dangling bonds. $\sigma_{e,neut}$, $\sigma_{e,pos}$, $\sigma_{h,neut}$, $\sigma_{h,neg}$ are the electron/hole capture cross section for neutral/charged dangling bonds. N_{DB} is the concentration of dangling bonds. E_{DB}^{Donor} and $E_{DB}^{Acceptor}$ are the peak positions of the donor-like and acceptor-like dangling bonds. σ_{DB} is the standard deviation of the Gaussian dangling bond distribution.

	µc-Si i-layer	**µc-Si p-layer**	**µc-Si n-layer**	**Type-I**	**Type-III**	**Type-IV**
Extended states						
E_g (eV)	1.18	1.18	1.18	1.8	1.5	1.1
N_C (cm^{-3})	4.8×10^{19}	4.8×10^{19}	4.8×10^{19}	2×10^{20}	2×10^{20}	4.8×10^{19}
N_V (cm^{-3})	2.4×10^{19}	2.4×10^{19}	2.4×10^{19}	2×10^{20}	2×10^{20}	2.4×10^{19}
E_F (eV)	0.69	0.06	1.15	1.0	0.85	0.66
E_i (eV)	0.581	0.581	0.581	0.9	0.75	0.541
n_i (cm^{-3})	3.97×10^{9}	3.97×10^{9}	3.97×10^{9}	1.42×10^{5}	4.74×10^{7}	1.27×10^{10}
n_0 (cm^{-3})	3.99×10^{11}	6.73	1.5×10^{19}	6.83×10^{6}	2.29×10^{9}	8.67×10^{11}
p_0(cm^{-3})	3.95×10^{7}	2.34544×10^{18}	1.05	2.94×10^{3}	9.84×10^{5}	1.86×10^{8}
μ_e (cm^2/Vs)	25	25	25	6	25	50
μ_h (cm^2/Vs)	5	5	5	2	5	10
χ (eV)	4.05	4.05	4.05	3.9	4.05	4.05
ε	11.9	11.9	11.9	11.9	11.9	11.9
Conduction band tails						
E_{char} (eV)	0.022	0.05	0.05	0.03	0.03	0.025
N_{Emob} ($cm^{-3}eV^{-1}$)	1.36×10^{20}	1×10^{21}	1×10^{21}	5×10^{21}	5×10^{21}	1.5×10^{20}
σ_{neut} (cm^2)	10^{-16}	10^{-16}	10^{-16}	10^{-16}	10^{-16}	10^{-16}
σ_{pos} (cm^2)	10^{-15}	10^{-15}	10^{-15}	10^{-15}	10^{-15}	10^{-15}
Valence band tails						
E_{char} (eV)	0.032	0.07	0.07	0.05	0.05	0.035
N_{Emob} ($cm^{-3}eV^{-1}$)	4.7×10^{19}	5×10^{20}	5×10^{20}	5×10^{21}	5×10^{21}	7.5×10^{19}
σ_{neut} (cm^2)	10^{-16}	10^{-16}	10^{-16}	10^{-16}	10^{-16}	10^{-16}
σ_{neg} (cm^2)	10^{-15}	10^{-15}	10^{-15}	10^{-15}	10^{-15}	10^{-15}
Dangling bonds						
E_{corr} (eV)	0.2	0.2	0.2	0.2	0.2	0.2
$\sigma_{e,neut}$ (cm^2)	10^{-16}	10^{-16}	10^{-16}	10^{-16}	10^{-16}	10^{-16}
$\sigma_{e,pos}$ (cm^2)	10^{-15}	10^{-15}	10^{-15}	10^{-15}	10^{-15}	10^{-15}
$\sigma_{h,neut}$ (cm^2)	10^{-16}	10^{-16}	10^{-16}	10^{-16}	10^{-16}	10^{-16}
$\sigma_{h,neg}$ (cm^2)	10^{-15}	10^{-15}	10^{-15}	10^{-15}	10^{-15}	10^{-15}
N_{DB} (cm^{-3})	7.5×10^{15}	7.5×10^{18}	7.5×10^{18}	5×10^{15}	5×10^{15}	5×10^{16}
E_{DB}^{Donor} (eV)	0.59	0.79	0.2	0.9	0.75	0.56
$E_{DB}^{Acceptor}$ (eV)	0.79	0.99	0.4	1.1	0.95	0.76
σ_{DB} (eV)	0.15	0.2	0.2	0.15	0.15	0.15

Appendix D: The calculation of the relation between the generation rate, excess carrier density, diffusion length, and quasi Fermi level splitting for a single layer based on the defect state distribution

Based on the defect state distribution for a certain material, the Shockley-Read-Hall (SRH) theory can be used to build up the relation between the generation rate G and excess carrier density Δn and, further, the diffusion length L_{diff} and quasi Fermi level splitting ΔE_F can be obtained. The detailed calculation process for intrinsic μc-Si:H layer as an example will be given below.

As discussed in Chapter 5.2, similar to a-Si:H, there are tail states and midgap states (i.e. dangling bonds) distributed within the bandgap for μc-Si:H. And defect distribution can be categorized as D_1 (conduction band tail state, acceptor), D_2 (valence band tail state, donor), D_3 (acceptor like dangling bond), and D_4 (donor like dangling bond). They can be express as:

$$D_1(E) = N_{T,A} \exp\left[\frac{E-E_c}{E_{char,A}}\right]; \qquad (D.1)$$

$$D_2(E) = N_{T,D} \exp\left[\frac{E_v-E}{E_{char,D}}\right]; \qquad (D.2)$$

$$D_3(E) = \frac{N_{DB}}{\sigma_{DB}\sqrt{2\pi}} \exp\left[-\frac{(E-E_{DB}^A)^2}{2\sigma_{DB}^2}\right]; \qquad (D.3)$$

$$D_4(E) = \frac{N_{DB}}{\sigma_{DB}\sqrt{2\pi}} \exp\left[-\frac{(E-E_{DB}^D)^2}{2\sigma_{DB}^2}\right]; \qquad (D.4)$$

where $N_{T,A}$ and $N_{T,D}$ are the density of state located at conduction and valence band edge; E_{char} is the characteristic energy; N_{DB} is the concentration of dangling bonds. E_{DB}^D and E_{DB}^A are the peak positions of the donor-like and acceptor-like dangling bonds. σ_{DB} is the standard deviation of the Gaussian dangling bond distribution. See Table C.1 in Appendix C.

According to the SRH theory, the SRH recombination rate $U(E_d)$ for a continuous distribution of defects at the defect energy E_d can be expressed as:

$$U(E_d) = \frac{D(E_d)(np-n_i^2)}{\frac{n+N_c e^{-\beta(E_c-E_d)}}{\gamma_{th,h}\sigma_h}+\frac{p+N_v e^{-\beta(E_v-E_d)}}{\gamma_{th,e}\sigma_e}}; \quad \text{(D.5)}$$

where N_C and N_V are the effective density of states in the conduction and valence band; n and p are the electron and hole concentration; n_i is the intrinsic carrier concentration; $\gamma_{th,e}$ and $\gamma_{th,h}$ (or expressed as γ_e and γ_h) are the thermal velocities for electron and hole; σ_e and σ_h are the capture cross section for electron and hole. β is defined as 1/kT (T is absolute temperature and k is Boltzmann's constant).

Therefore, the recombination rates for above four types of defects (i.e. U_1, U_2, U_3 and U_4) can be defined by integrating over the energy level from valence band to conduction band. Furthermore, the total recombination rate U is equal to the sum of the recombination rate resulted from the above four types of defects and can be expressed as:

$$U(E) = U_1 + U_3 + U_2 + U_4 =$$
$$\int_{E_v}^{E_c} \Bigg(\frac{\gamma_e\gamma_h\sigma_{TAE}\sigma_{TAH}(np-n_i^2)\times\left\{N_{T,A}\exp\left[\frac{E-E_c}{E_{char,A}}\right]\right\}}{\gamma_e\sigma_{TAE}\left(n+n_i\exp\left[\frac{E-E_i}{kT}\right]\right)+\gamma_h\sigma_{TAH}\left(p+n_i\exp\left[\frac{E_i-E}{kT}\right]\right)} +$$
$$\frac{\gamma_e\gamma_h\sigma_{GAE}\sigma_{GAH}(np-n_i^2)\times\left\{\frac{N_{DB}}{\sigma_{DB}\sqrt{2\pi}}\exp\left[-\frac{(E-E_{DB}^A)^2}{2\sigma_{DB}^2}\right]\right\}}{\gamma_e\sigma_{GAE}\left(n+n_i\exp\left[\frac{E-E_i}{kT}\right]\right)+\gamma_h\sigma_{GAH}\left(p+n_i\exp\left[\frac{E_i-E}{kT}\right]\right)} +$$
$$\frac{\gamma_e\gamma_h\sigma_{TDE}\sigma_{TDH}(np-n_i^2)\times\left\{N_{T,D}\exp\left[\frac{E_v-E}{E_{char,D}}\right]\right\}}{\gamma_e\sigma_{TDE}\left(n+n_i\exp\left[\frac{E-E_i}{kT}\right]\right)+\gamma_h\sigma_{TDH}\left(p+n_i\exp\left[\frac{E_i-E}{kT}\right]\right)} +$$
$$\frac{\gamma_e\gamma_h\sigma_{GDE}\sigma_{GDH}(np-n_i^2)\times\left\{\frac{N_{DB}}{\sigma_{DB}\sqrt{2\pi}}\exp\left[-\frac{(E-E_{DB}^D)^2}{2\sigma_{DB}^2}\right]\right\}}{\gamma_e\sigma_{GDE}\left(n+n_i\exp\left[\frac{E-E_i}{kT}\right]\right)+\gamma_h\sigma_{GDH}\left(p+n_i\exp\left[\frac{E_i-E}{kT}\right]\right)} \Bigg) \, dE; \quad \text{(D.6)}$$

where σ_{TAE} and σ_{GAE} are the electron capture cross-section for the acceptor tail and Gaussian states. σ_{TAH} and σ_{GAH} are the hole capture cross-section for the acceptor tail

and Gaussian states. σ_{TDE} , σ_{GDE} , σ_{TDH} and σ_{GDE} are the equivalents for donor states. And their values were listed in Table C.1. E_i is the intrinsic Fermi energy.

For intrinsic μc-Si:H, $N_c = 4.8 \times 10^{19} cm^{-3}$; $N_v = 2.4 \times 10^{19} cm^{-3}$; $E_g = 1.18\ eV$;

$$n_i = \sqrt{N_c N_v} \exp\left(\frac{-E_g}{2kT}\right) = \sqrt{4.8 \times 10^{19} \times 2.4 \times 10^{19}} \exp\left(\frac{-1.18}{2\times 0.0258}\right) = 3.9735 \times 10^{9}\ cm^{-3}; \quad \text{(D.7)}$$

$$E_i = \frac{E_c + E_v}{2} + \frac{kT}{2} \ln\left(\frac{N_v}{N_c}\right) = \frac{1.18+0}{2} + \frac{1}{2} \times 0.0258 \times \ln\left(\frac{2.4\times 10^{19}}{4.8\times 10^{19}}\right) = 0.581058\ eV; \quad \text{(D.8)}$$

$$n_0 = N_c \exp\left(\frac{E_{FN} - E_c}{kT}\right) = n_i \exp\left[\frac{E_F - E_i}{kT}\right] = 4.8 \times 10^{19} \times \exp\left[\frac{-0.49}{0.0258}\right] = 2.71 \times 10^{11}\ cm^{-3}; \quad \text{(D.9)}$$

$$p_0 = N_v \exp\left(\frac{E_v - E_{FP}}{kT}\right) = n_i \exp\left[\frac{E_i - E_F}{kT}\right] = 2.4 \times 10^{19} \times \exp\left[\frac{-0.69}{0.0258}\right] = 5.826 \times 10^{7}\ cm^{-3}; \quad \text{(D.10)}$$

Thermal velocity: $$v_{th} = \sqrt{3kT/m_{eff}}\ ; \quad \text{(D.11)}$$

$$\frac{m_h}{m_e} = 0.69\ ; \quad \text{(D.12)}$$

$$v_e = 0.83 v_h\ ; \quad \text{(D.13)}$$

Assume: $$v_e \approx v_h \approx 10^7 cm/s; \quad \text{(D.14)}$$

$$n = n_0 + \Delta n\ ; \quad \text{(D.15)}$$

$$p = p_0 + \Delta p\ ; \quad \text{(D.16)}$$

Assume: $$\Delta n = \Delta p\ ; \quad \text{(D.17)}$$

Under open-circuit condition, the generation rate G should be equal to the recombination rate U:

$$G = U\ ; \quad \text{(D.18)}$$

Combine the equations from (D.6) to (D.18), a relation between the recombination rate G and excess carrier density Δn can be built up. And to solve the above equations, "Wolfram Mathematica 9" was used. For a given generation rate, for example $G = 7.5\times 10^{20}$ $cm^{-3}s^{-1}$ (this means a short-circuit current of 24 mA/cm^2 is generated

within a 2 μm thick film), it corresponds to create an excess carrier density of 6.0×10^{13} cm^{-3} based on the above calculation. As a result, the minority carrier lifetime τ can be defined as:

$$\tau = \frac{\Delta n}{U} = \frac{\Delta n}{G} = \frac{6\times10^{13}}{7.5\times10^{20}} = 8\times10^{-8}s = 80\ ns\ ; \quad \text{(D.16)}$$

Quasi Fermi level splitting ΔE_F can be defined as:

$$\Delta E_F = \frac{kT}{q}\ln\left(\frac{np}{n_i^2}\right) = \frac{kT}{q}\ln\left(\frac{(n_0+\Delta n)(p_0+\Delta n}{n_i^2}\right) = 0.0258\ln\left(\frac{(2.71\times10^{11}+\Delta n)(5.83\times10^{7}+\Delta n}{n_i^2}\right) \approx$$

$$0.0258ln(\frac{\Delta n}{n_i})^2 \approx 0.4967\ V; \quad \text{(D.17)}$$

Diffusion length L_{diff} can be defined as (where μ is the effective carrier mobility):

$$L_{diff} = \sqrt{\frac{kT}{q}\mu\tau} = 787.2\ nm; \quad \text{(D.18)}$$

Drift length L_{drif} can be defined as:

$$L_{drif} = \mu\tau|E| \approx \mu\tau\frac{V_{bi}}{L} = 13.21\ \mu m; \quad \text{(D.19)}$$

where E is the internal electrical field; V_{bi} is the built-in potential; L is the film thickness.

Based on above calculation process, the relation between G, τ, Δn, ΔE_F, L_{diff} can be built up and shown in below Figure D.1.

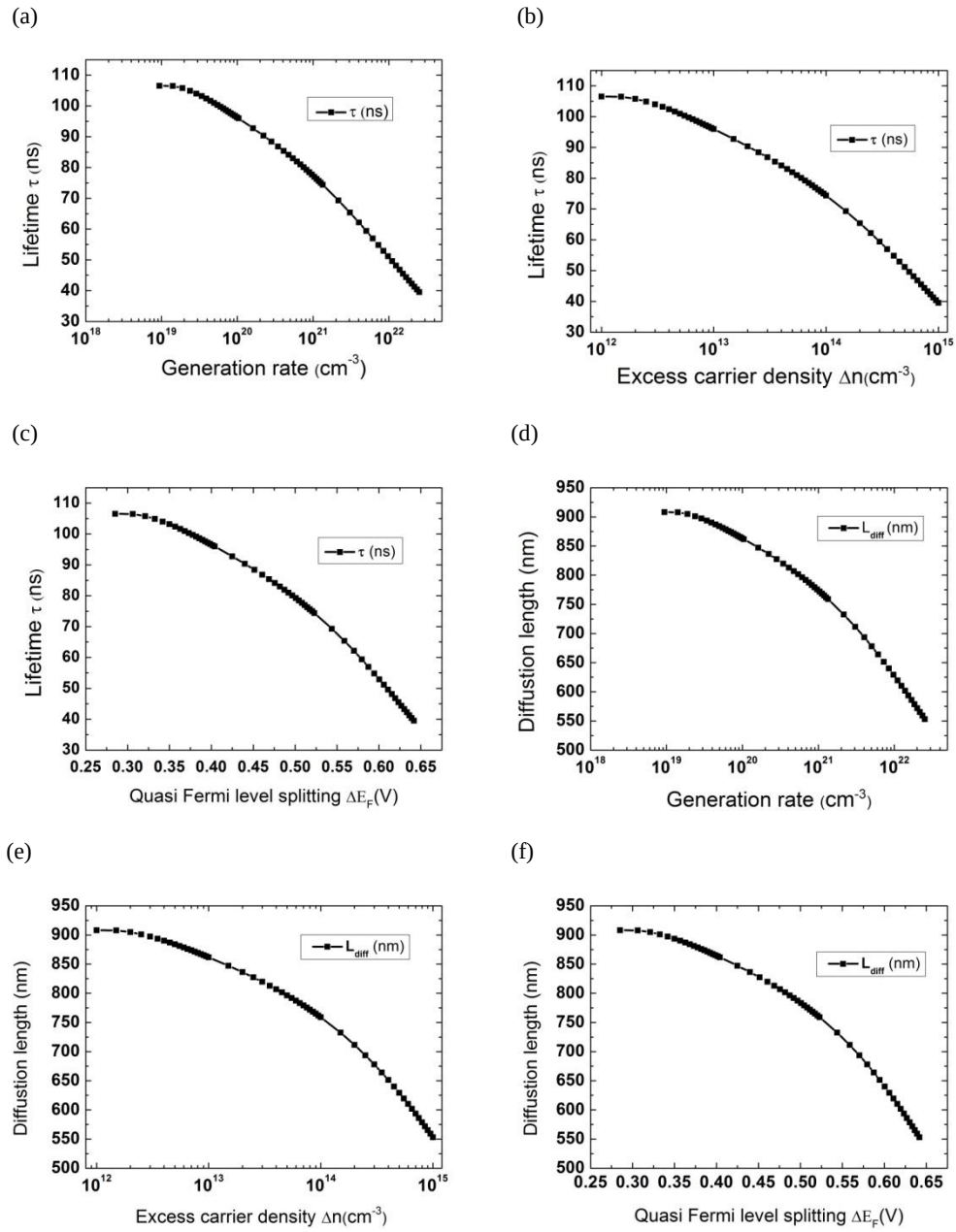


Figure D.1: Simulated minority lifetime τ of μc-Si:H layer versus (a) generation rate G, (b) excess carrier density Δn, (c) quasi Fermi level splitting ΔE_F; and simulated diffusion length L_{diff} of μc-Si:H layer versus (d) generation rate G, (e) excess carrier density Δn, (f) quasi Fermi level splitting ΔE_F.

Appendix E: Characterization methods used in this thesis

In this section, a brief introduction of the main characterization methods used in this thesis is given. These characterization methods are widely used in the thin-film community to determine the optical and electrical properties of various thin-film materials.

Raman spectroscopy and Raman crystallinity

Raman spectroscopy is based on the phenomenon of inelastic scattering of light, which was discovered in 1928 by C.V. Raman [185]. The electromagnetic radiation (i.e. the incoming photons) may trigger the vibrational and/or rotational motions of molecules or atoms (phonon) in a crystal lattice. In these interactions, the incoming photons either gain or lose energy. As a result, there is an energy shift (or frequency shift) for the scattered photons, which is called 'Raman shift'. It reveals the characteristics of the structures and chemical bonds in the materials. Raman spectroscopy has been widely used to investigate thin-film material structures, because it is sensitive, non-destructive and convenient.

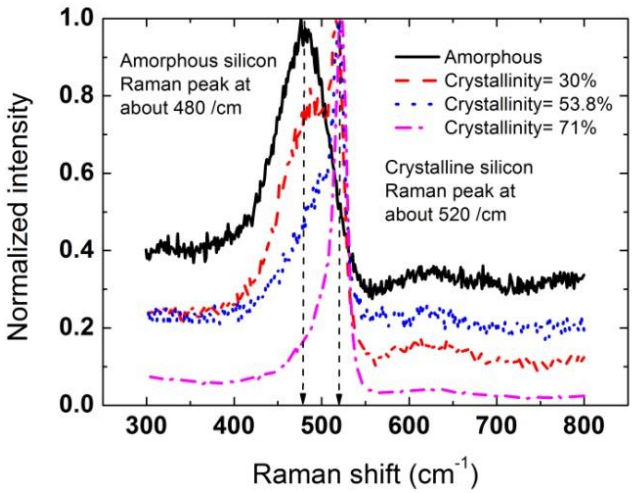


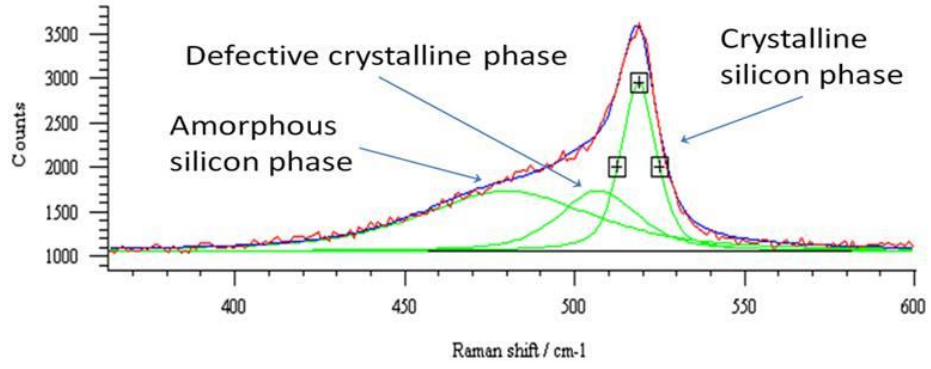
Figure E.1: Raman spectra for amorphous silicon and microcrystalline silicon with different crystallinity. All spectra have been normalized for comparison purposes.

For crystalline silicon, a sharp Raman peak can be observed at a Raman shift of 520 cm^{-1}. However, for amorphous silicon, a broad peak centred at around 480 cm^{-1} can be seen. For microcrystalline silicon, which is a mixed phase material containing crystalline silicon grains embedded in an amorphous silicon matrix, the Raman spectrum looks like the result of a combination of crystalline silicon and amorphous silicon, showing a sharp peak near 520 cm^{-1} and a broad peak near 480 cm^{-1}. Figure E.1 shows a set of normalized Raman spectra for both amorphous silicon and microcrystalline silicon having different crystallinity.

As can be seen from Figure E.1, there is an evolution of the shape of the spectrum when going from low to high crystallinity: The broad shoulder near 480 cm^{-1} gradually disappears and, at the same time, the peak near 520 cm^{-1} (representing the crystalline phase) has a slight shift towards higher wave numbers. This peak shift indicates the variation of the crystalline grain size. In this thesis, in order to perform Raman measurements, the corresponding silicon films are deposited onto soda-lime glass sheets. The Raman spectra presented in this thesis are measured by a Raman microscope (Renishaw Raman Scope System 2000), using a grating of 1800 lines/mm in a backscattering geometry with a 2 mW argon laser operating at a wavelength of 514 nm (green light). The incident light is focused on a spot of about 1 μm in diameter. The laser output power is set at a low level, to guarantee that there is no laser induced crystallization. The green laser source used here has a detection depth of about 100 nm when measuring microcrystalline silicon but only several tens of nanometres when measuring amorphous silicon.

To extract useful information from the obtained Raman spectrum, curve fitting is to be performed, as sketched in Figure E.2. This is an important procedure and the results obtained depend on the fitting method, especially in the case of μc-Si:H (as this material contains two silicon phases). Many curve fitting methods have been proposed, such as three Gaussian line profiles [69], five Gaussian line profiles [186],

or two asymmetrical Lorentzian line profiles [187]. Generally, "three Gaussian line profiles" is most widely used because of its simplicity and repeatability. We also use this method to calculate the crystallinity in all our experiments.



Curve Name	Centre	Width	Height	% Gaussian	Type	Area
Curve 1	480	60.7274	683.434	37.2971	Mixed	57355.3
Curve 2	507.075	27.655	686.949	47.4456	Mixed	25277.5
Curve 3	519	12.5767	1905.44	51.308	Mixed	31417.2

Figure E.2: Example of the three Gaussian line profile curve fitting method used for determining the µc-Si:H crystallinity from a measured Raman spectrum. Red curve: Raman measurement, green curves: fitted individual Gaussian components. Blue curve: Resulting fitted total contribution obtained by adding up the green curves.

Figure E.2 shows a Raman spectrum of a typical µc-Si:H film, together with the three Gaussian lines obtained by curve fitting. The first peak in the region of 460 - 490 cm^{-1} comes from the TO (transverse optic) vibrational mode of amorphous silicon. The second one arises near 500 - 510 cm^{-1} and, according to the literature, this peak can be attributed either to crystallites of diameters lower than 10 nm (i.e. nano-crystalline material) or to the bond dilation at the grain boundaries which can be interpreted as the defective part of the crystalline phase [188]. The third narrow peak, with a centre position in the 515 - 521 cm^{-1} range, is assigned to the TO mode in crystalline silicon. According to the three Gaussian line profile method, the resulting Raman crystallinity X_c is defined by:

$$\boldsymbol{X_c} = \frac{\boldsymbol{I_c + I_{dc}}}{\boldsymbol{I_c + I_{dc} + I_\alpha}}; \qquad \text{(E. 1)}$$

where I_c, I_{dc}, I_α are the integrated areas of the crystalline, defective crystalline and amorphous components, *i.e.* the values listed under the heading "Area" in Figure E.2.

Apart from the choice of the number of the peaks to do the curve fitting, the fitting results are also sensitive to the selection of some additional input parameters, such as the range of the data points used for the curve fitting, the information whether the peak positions are fixed or not during the fitting process, as well as the width of each peak. A deeper discussion can be found in Ref. [189].

Dark conductivity measurement

The conductivity σ, measured in S/cm, is a very important parameter that reflects the electrical property of thin-film materials. It can be measured either in the dark or under illumination. A fast and convenient method to obtain σ, or the corresponding sheet resistance of the thin film (measured in Ω/□), is using a "four point probe" (4PP) measurement system.

Optical measurements: UV-VIS spectroscopy

The optical properties of thin-film materials and superstrates are other important parameters that need to be considered when making solar cells. This includes the measurement of transmission, reflection and absorption as a function of the wavelength λ of the incoming light. From these measured results, some other parameters can be further derived, such as the absorption coefficient, the index of refraction, the optical bandgap (using a so called Tauc plot), and the estimation of the film thickness [190].

In this thesis, a UV-VIS spectrometer (Perkin-Elmer, Lambda 950) was used to measure these parameters. In order to study the scattering behaviour of the superstrates, the haze ratio H was calculated to reflect the optical scattering ability of the

superstrates having different surface morphology. It is defined as the ratio between the transmission of the diffuse light, $T_{diffuse}$, and total transmission T_{total}.

$$\boldsymbol{H = \frac{T_{diffuse}}{T_{total}}}; \qquad \textbf{(E. 2)}$$

$$\boldsymbol{T_{total} = T_{diffuse} + T_{specular}}; \qquad \textbf{(E. 3)}$$

where $T_{specular}$ is the transmittance of the specular light. T_{total} and $T_{specular}$ can be directly measured, see Figure E.3.

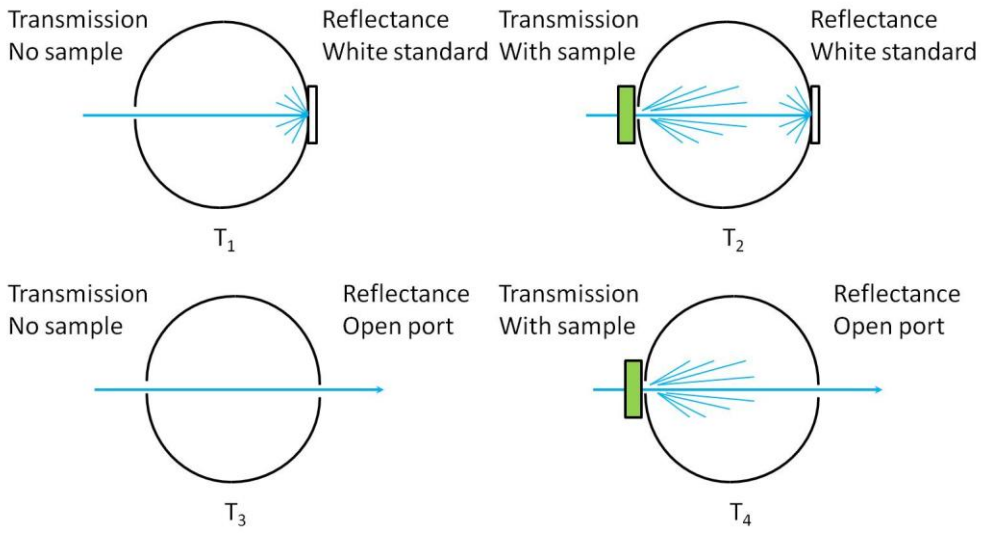


Figure E.3: Schematic of the measurement procedure used for haze calculation [191].

Figure E.3 shows the procedure for Haze measurement by using UV-VIS spectroscopy. It involves four transmission scans of the sample within a certain spectral range (*e.g.* 300 - 1200 nm). A series of wavelength dependent transmission curves are obtained for the 4 configurations as sketched in Figure E.3. The Haze value at a certain wavelength (H_λ) is then calculated by:

$$H_\lambda = [\ (T_4/T_2) - (T_3/T_1)\ ] \times 100\%\ ; \qquad \text{(E. 4)}$$

Thus a spectrally resolved haze is obtained, as shown in Chapter 6 of this thesis.

A faster method to obtain an integrated haze value is using a digital hazemeter (*i.e.* using the BYK Haze Guard, model AT-4725, light source: tungsten lamp), see

Chapter 6. A visible light pulse (400 - 700 nm) flashes onto the sample and a single haze value is reported on the panel screen. It renders an average value for the visual spectrum weighted with the human eye's response. This method is widely used in the glass industry.

Determination of film thickness: Stylus profiler

The determination of the film thickness and an estimate the thin-film deposition rate is frequently required in the thin-film community. Generally, mechanical or optical methods can be used for this purpose. The used "Stylus profiler" (Veeco, Dektak 150) is a typical thickness measurement tool using a mechanical method. A diamond stylus moves vertically to create contact with the sample surface and then moves laterally for a specified distance. It measures small surface variations via vertical displacements of the stylus, or vibrations as a function of position by recording the stylus vibration history (which is called "contact profilometry technique"). Therefore, it can also be applied to the measurement of surface topography, surface roughness and step size or heights. In this thesis, most of the thin-film thickness measurements are realized using this technology.

Characterisation of surface morphology: Atomic force microscopy

In this thesis, sample surface morphologies were measured by atomic force microscopy (AFM), due to superior precision and resolution. It records the vibration (or deflection) of a cantilever with a sharp tip by using a laser spot to map the sample surface in a very high resolution. It is widely used in various areas for surface characterization. In this thesis, we use an AFM (Veeco, model DI-3100 Nanoman) to study and compare the surface morphology of different superstrates and discuss how (i) it impacts the optical scattering behaviour of the various superstrates and (ii) it affects the μc-Si thin-film growth (see Chapter 6).

Material structure characterization: Transmission electron microscopy

The microstructure of materials can be characterised with a transmission electron microscope (TEM). A fine electron beam transmits through an ultra-thin specimen and interacts with the specimen as it passes through. The image is magnified and focused onto an imaging device. Figure E.4(a) shows a typical cross-sectional TEM (XTEM) image from a µc-Si:H thin-film solar cell, taken with a field emission TEM (JEOL-JEM, 2010F).

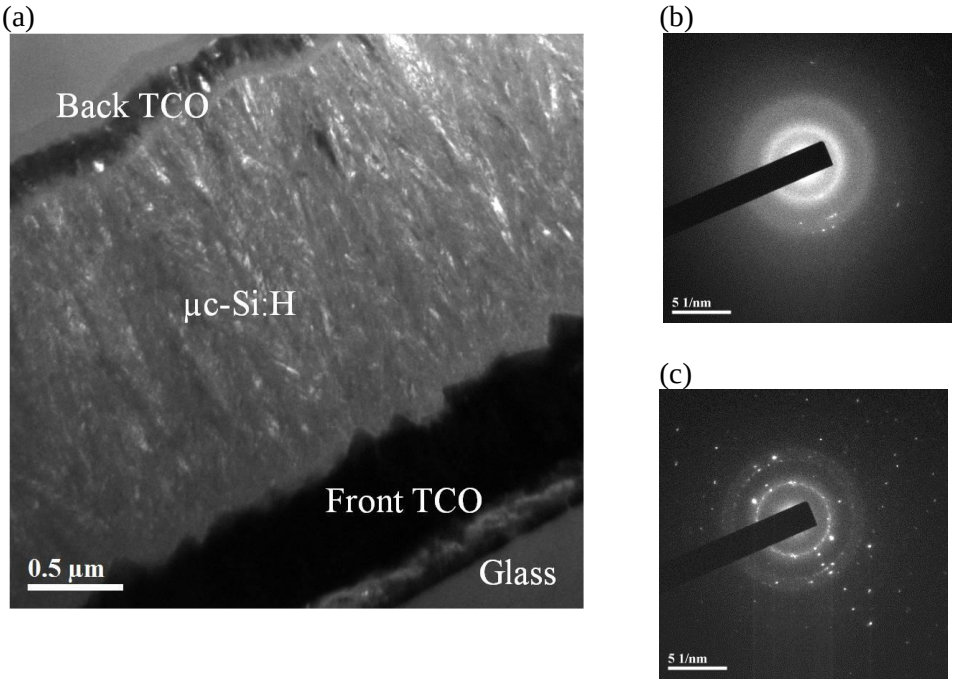


Figure E.4: (a) Typical XTEM image from a µc-Si:H thin-film solar cells; Diffraction pattern for (b) a-Si:H and (c) µc-Si:H.

The diffraction pattern from the TEM is an effective method to reveal the micro-structure of the material. When the material has an ordered structure (*e.g.* c-Si) and the atoms are arranged in a periodic way that meets the Bragg condition (Eqn. E.5), the electron beam gets diffracted and the electron diffraction effect occurs. In this case, a series of diffraction spots will appear on the dark background for the following condition:

$$n\lambda = 2d \sin(\theta) ; \qquad \text{(E. 5)}$$

where n is an integer, λ is the wavelength of incident ray (electron beam), d is the spacing between the lattice planes of the crystal, θ is the angle between the incident ray and the scattering lattice planes.

However, in case of imaging a-Si:H, it only displays a series of diffuse halo rings as shown in Figure E.4(b). In case of imaging μc-Si:H, which contains both a-Si and c-Si, its diffraction pattern displays both a series of diffuse halo rings and some discrete diffraction spots as shown in Figure E.4(c). These spots can be used to reveal the crystal orientation. In Chapter 4, the corresponding diffraction pattern obtained from imaging various thin-film buffer layers will be used to reveal the material composition of the buffer layers. In Chapter 6, high resolution XTEM images will be used to investigate the impact of the surface morphology on the μc-Si:H thin-film growth behaviour and on the formation of defective regions.

Solar cell characterization methods

(i) One-sun I-V measurement

The one-sun photovoltaic parameters, open-circuit voltage (V_{oc}), short-circuit current density (J_{sc}), fill factor (*FF*) and conversion efficiency (*Eff*) are the most widely used performance parameters of solar cells [192]. In this thesis, the *I-V* characteristics of the cells were measured under standard test conditions (i.e. AM1.5G spectrum, 1000 W/m^2 light intensity, cell temperature of 25 ˚C), using a class AAA dual light source solar simulator (Wacom, WXS_156S_L2).

(ii) Suns-Voc measurement

Quasi-steady-state photoconductance (QSSPC) and the "Suns-V_{oc}" technique are extensively used for the characterization of silicon wafer based solar cells [193]. In this thesis, we also applied the Suns-V_{oc} technique to test μc-Si:H thin-film solar cells. Using a photographic flash light, the light intensity as well as the sample's quasi-

steady-state V_{oc} are measured. Assuming a reasonable 1-sun short-circuit current density, a 'pseudo *I-V* curve' and a 'pseudo fill factor' are obtained. Since the measurements were performed under V_{oc} conditions, the resulting pseudo I-V curve is free of series resistance effects. A large-area Suns-V_{oc} system developed by SERIS was used in this thesis; for details on this tester see Ref. [194].

(iii) External quantum efficiency measurements

Another important parameter to assess the quality of a solar cell is the quantum efficiency (QE). It is wavelength dependent and measured over a range of wavelengths to characterize the photogenerated carrier collection efficiency at each photon energy. An internal and an external QE can be defined as follows:

$$\boldsymbol{EQE} = \frac{\boldsymbol{n_e}}{\boldsymbol{n_{incident\ photon}}}; \tag{E. 6}$$

$$\boldsymbol{IQE} = \frac{\boldsymbol{n_e}}{\boldsymbol{n_{absorbed\ photon}}} = \frac{\boldsymbol{EQE}}{\boldsymbol{1-Reflection-Transmission}}; \tag{E. 7}$$

where n_e is the flux of collected electrons (i.e., electrons per second) flowing into the external circuit at short-circuit conditions; $n_{incident\text{-}photon}$ is the incident photon flux on the cell; $n_{absorbed\text{-}photon}$ is the photon flux absorbed by the solar cell. One first measures the EQE of the solar cell and its transmission as well as reflection. Next, all these data are combined together to obtain the IQE (Eqn. E.7).

The internal QE (IQE) directly reflects the carrier collection efficiency and is mainly determined by the quality of the absorber layer of the solar cell. However, except for the material quality, external QE (EQE) is additionally impacted by some factors from outside of the solar cell, which cause optical loss, such as surface shading, reflection, and parasitic optical absorption in the TCO and window layers. Integration of the EQE spectrum over the wavelength range of the solar spectrum which can be absorbed by thin-film silicon layers (i.e. over a wavelength range from

300 to 1200 nm) gives the EQE-based short-circuit current density J_{sc} of the solar cell. In our experiment, the QE was measured with a Zolix system (solar cell scan 100, Zolix Instruments Co. Ltd.).

EBIC measurements

In some cases, the solar cells may suffer from local shunting issues resulting from defective regions which typically form above microtextured surface features exhibiting a large surface angle (for more information see Chapter 6 of this thesis). Therefore, a fast and simple method is needed for failure analysis. Cross-sectional electron beam induced current (EBIC) technology has been widely used in the field of integrated circuits (IC) for the purpose of device diagnostics [170]. During an EBIC measurement an electron beam irradiates the sample under investigation (for example a thin-film diode) and generates excess electron-hole pairs, and the system records the current collected by the diode's junction as a function of position and of externally voltage applied. Therefore, a charge carrier separating and collecting structure, such as a p-n junction or Schottky barrier, is required for EBIC measurements [174]. These charge carriers can either be collected or they recombine before being collected. The collection probability depends on the location of the generated e-h pairs, on the minority carrier diffusion lengths of the material, and on the potential distribution within the device under investigation. Therefore, the EBIC signal can be used to estimate the minority carrier diffusion length [172], which is a good indicator of the material quality. In this thesis, we will show that the EBIC technique is also a powerful tool to detect the structural defects in µc-Si:H thin-film solar cells, see Chapter 6.5 for more details.

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