HIGH-MOBILITY GERMANIUM-TIN FIELD-EFFECT TRANSISTORS: SURFACE PASSIVATION, CONTACT, AND DOPING TECHNOLOGIES

LANXIANG WANG

NATIONAL UNIVERSITY OF SINGAPORE

2014

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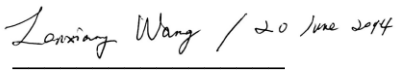
Declaration

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.



Lanxiang WANG
20 June 2014

Acknowledgements

"Where there is a will, there is a way."
Thomas Alva Edison

"天行健，君子以自强不息。"
《易》

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Lanxiang Wang

Singapore, June 2014

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Surface Passivation, Contact, and Doping Technologies

by

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Silicon (Si) complementary metal-oxide-semiconductor (CMOS) transistors have been widely used in electronics for the past several decades. The trend of scaling Si transistors towards higher packing density, faster speed, reduced cost, and lower power consumption per function has become a driving force of technological change. However, continual scaling of transistors into sub-10 nm regime meets great challenges. Exploring high-mobility channel materials to replace Si is deemed as a solution to extend the CMOS road map. In particular, germanium-tin ($Ge_{1-x}Sn_x$) have become of great interest due to its high career mobilities. This thesis aims to address various challenges in taking full advantage of $Ge_{1-x}Sn_x$ for future CMOS logic applications.

For $Ge_{1-x}Sn_x$ p-channel metal-oxide-semiconductor field-effect transistors (p-MOSFETs), ammonium sulfide [$(NH_4)_2S$] was first demonstrated to achieve high-quality gate stack. Single-crystalline $Ge_{0.958}Sn_{0.042}$ films were grown on Ge (100) substrate by a solid source

molecular beam epitaxy (MBE) system. Prior to gate dielectric deposition, $(NH_4)_2S$ passivation was done by treatment with $(NH_4)_2S$ aqueous solution (36%) for 10 minutes at 25 °C. The $(NH_4)_2S$-passivated $Ge_{0.958}Sn_{0.042}$ p-MOSFETs show decent transfer and output characteristics. A peak mobility of 509 $cm^2/V{\cdot}s$, which is higher than those of other (100)-oriented $Ge_{1-x}Sn_x$ p-MOSFETs reported so far, was obtained for the $(NH_4)_2S$-passivated transistors.

Next, incorporation of platinum (Pt) during the formation of nickel (Ni) stanogermanide was exploited for metallization scheme of $Ge_{1-x}Sn_x$ transistors. The surface of Ni/$Ge_{0.947}Sn_{0.053}$ sample becomes rough after annealing at 450 °C, which is the cause of the sharp increase in sheet resistance from 450 to 500 °C. The incorporation of Pt improves the thermal robustness by suppressing agglomeration during reaction between Ni and $Ge_{0.947}Sn_{0.053}$ at temperatures higher than 450 °C.

To realize high-performance $Ge_{1-x}Sn_x$ n-MOSFETs, high n-type dopant activation for low source/drain (S/D) resistance is critical. We first investigated $Ge_{0.976}Sn_{0.024}$ n^+/p junction formation using phosphorus ion (P^+) implant without heating the substrate during the implant. Various activation temperatures were investigated to activate the dopants. Activation temperature as low as 400 °C is demonstrated to obtain active doping concentration of 2.1×10^{19} cm^{-3} for P^+-implanted $Ge_{0.976}Sn_{0.024}$. In addition, we investigated the effect of P^+ implant temperature on the material properties and the electrical characteristics of epitaxial $Ge_{0.976}Sn_{0.024}$. Implant at elevated temperature of 400 °C was explored to maintain the single-crystallinity of $Ge_{0.976}Sn_{0.024}$ during implant and achieve a lower contact resistivity after activation at 450 °C as compared with the room-temperature implant.

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Symbol	Description	Unit
C	Capacitance	F/cm^2
C_{inv}	Capacitance in the inversion layer	F/cm^2
C_{it}	Capacitance associated with interface traps	F/cm^2
C_{OX}	Gate oxide capacitance	F/cm^2
d	Contact spacing	µm
D_{it}	Interface trap density	cm^{-2}/eV
D_n	Diffusion coefficient for electrons	cm^2/s
E_C	Energy of conduction band edge	eV
E_{CNL}	Charge neutrality level	eV
E_f	Fermi level	eV
E_{eff}	Effective vertical electrical field	eV
E_G	Bandgap	eV
E_V	Energy of valence band edge	eV
f	Frequency	Hz
G_m	Transconductance	S/µm
$\hbar$	Reduced Planck's constant	eV·s
I_B	Body current	A/µm
I_D	Drain current	A/µm
I_{Dark}	Dark current	A/cm^2
I_{DS}	Drain-to-source current	A/µm
I_{DSat}	Saturation drain current	A/µm
$I_{forward}$	Forward current	A/cm^2
$I_{reverse}$	Reverse current	A/cm^2
I_{OFF}	Off-state current	A/µm
I_{ON}	On-state current	A/µm
I_S	Source current	A/µm
J_F	Forward current density	A/cm^2
J_G	Gate leakage current	A/cm^2
J_n	Electron diffusion current density in the p-side	A/cm^2
J_{re}	Recombination-current density	A/cm^2
k	Boltzmann constant	eV/K
L_{CH}	Channel length	µm

L_G	Gate length	μm
m_e^*	Electron effective mass	kg
m_h^*	Hole effective mass	kg
n	Ideality factor	1
N	Channel doping concentration	cm^{-3}
N_A	Acceptor concentration	cm^{-3}
N_{inv}	Inversion carrier density	cm^{-2}
N_D	Donor concentration	cm^{-3}
N_S	Surface doping concentration	cm^{-3}
$N_{S,Source}$	Carrier concentration near the source edge	cm^{-3}
n_i	Intrinsic carrier concentration	cm^{-3}
n_s	Surface concentration of minority carrier	cm^{-3}
n_{Total}	Total phosphorus concentration	cm^{-3}
Q_f	Fixed oxide charge	C
q	Elementary charge	C
R_C	Contact resistance	Ω
R_{CH}	Channel resistance	Ω
R_D	Drain resistance	Ω
R_P	Projected range	nm
R_S	Source resistance	Ω
$R_{S/D}$	S/D parasitic resistance	Ω
R_{Sh}	Sheet resistance	Ω/square
R_{total}	Total resistance	Ω
r_c	Backscattering coefficient	1
S	Subthreshold swing	mV/decade
T	Temperature	K
t_{ox}	Thickness of SiO_2	nm
V	Voltage	V
V_{DD}	Supply voltage	V
V_{DS}	Drain voltage	V
V_{FB}	Flatband voltage	V
V_{GS}	Gate voltage	V
v_{inj}	Thermal injection velocity	m/s
V_{TH}	Threshold voltage	V
W	Gate width	μm
ΔE_C	Conduction band offset	eV

ΔE_G	Band gap narrowing	eV
ΔE_V	Valence band offset	eV
ΔL_G	Difference in the gate length	μm
ΔR_{total}	Difference in the total resistance	Ω
Z	Contact width	μm
Φ_B	Schottky barrier height	eV
μ_{eff}	Effective mobility	$cm^2/V{\cdot}s$
μ_{max}	The highest mobility in bulk semiconductor	$cm^2/V{\cdot}s$
ξ	Electric field	V/cm
ξ_o	Electric field at the location of maximum recombination	V/cm
ξ_{eff}	Effective vertical electric field	V/cm
σ_{GB}	Grain-boundary energy	J
σ_I	Interface energy	J
σ_S	Surface energy	J
ρ_C	Contact resistivity	J
τ_d	Time delay	s
τ_n	Carrier lifetime for electrons	s
θ_I	Contact angle at the interface	°
θ_S	Contact angle at the surface	°

List of Abbreviations

AFM	Atomic force microscopy
Al_2O_3	Aluminum oxide
Al	Aluminum
ALD	Atomic layer deposition
APBs	Anti-phase boundaries
As	Arsenic
a/c	amorphous/crystalline
B	Boron
CET	Capacitance equivalent thickness
Cl_2	Chlorine
CMOS	Complementary metal-oxide-semiconductor
CVD	Chemical vapor deposition
DHF	Dilute hydrofluoric acid
EDX	Energy dispersive X-Ray analysis
EOT	Equivalent oxide thickness
FinFET	Fin field-effect transistor
Ga	Gallium
GaAs	Gallium arsenide
Ge	Germanium
$Ge_{1-x}Sn_x$	Germanium-tin
HAADF-STEM	High angle annular dark field-scanning transmission electron microscopy
H_2SO_4	Sulfuric acid
HCl	Hydrochloric acid
HfO_2	Hafnium dioxide
HH	Heavy-hole
High-*k*	High dielectric constant (dielectric)
HP	High-performance
HRTEM	High-resolution transmission electron microscopy
HRXRD	High-resolution X-ray diffraction
H_2S	Hydrogen sulfide
IC	Integrated circuit
IEDM	International Electron Devices Meeting
IMRE	Institute of Materials Research and Engineering

$In_{1-a}Al_aP$	Indium aluminum phosphide
InAs	Indium arsenide
$In_{1-b}Ga_bAs$	Indium gallium arsenide
InP	Indium phosphide
InSb	Indium antimonide
ITRS	International Technology Roadmap for Semiconductors
LA	Laser annealing
$LaAlO_3$	Lanthanum aluminate
LH	Light-hole
LOP	Thermal injection velocity
MBE	Molecular beam epitaxy
MOCVD	Metal-organic chemical vapor deposition
MOSFET	Metal-oxide-semiconductor field-effect transistor
N_2	Nitrogen
Ni	Nickel
NiGe	Nickel germanide
Ni(GeSn)	Nickel stanogermanide
n-MOSFET	N-channel metal-oxide-semiconductor field-effect transistor
P	Phosphorus
P^+	Phosphorus ion
Pd	Palladium
PDA	Post deposition anneal
PECVD	Plasma enhanced chemical vapor deposition
PMA	Post metal annealing
PR	Photoresist
Pt	Platinum
$Pt_x(GeSn)_y$	Platinum stanogermanide
p-MOSFET	P-channel metal-oxide-semiconductor field-effect transistor
QW	Quantum well
RHEED	Reflection high-energy electron diffraction
rlu	Reciprocal lattice unit
RMS	Root-mean-square
RSM	Reciprocal space maps
RT	Room temperature
RTA	Rapid thermal annealing

S	Sulfur
Sb	Antimony
SBH	Schottky barrier height
SDE	Source/drain extension
SEM	Scanning electron microscopy
Si	Silicon
Si_2H_6	Disilane
$Si_{1-y}Ge_y$	Silicon-germanium
$Si_{1-x-y}Ge_ySn_x$	Silicon-germanium-tin
SIMS	Secondary ion mass spectrometry
SiO_2	Silicon dioxide
Sn	Tin
SPE	Solid-phase epitaxy
SRH	Shockley-Read-Hall
SRP	Spreading resistance probe
STI	Shallow trench isolation
S/D	Source/drain
TaN	Tantalum nitride
TCAD	Technology computer aided design
TEM	Transmission electron microscopy
TFET	Tunneling field-effect transistor
Ti	Titanium
TLM	Transfer length method
TMA	Trimethylaluminium
UHVCVD	Ultra-high-vacuum chemical vapor deposition
VB	Valence band
VLSIT	Symposium on VLSI Technology
XRD	X-ray diffraction
XPS	X-ray photoelectron spectroscopy
XTEM	Cross-sectional transmission electron microscopy
Zr	Zirconium
ZrO_2	Zirconium oxide
$(NH_4)_2S$	Ammonia sulfide

Chapter 1

Introduction

1.1 Background

1.1.1 The End of Classical MOSFET Scaling

Since the first demonstration by D. Kahng and M. M. Atalla in 1960 [1], the silicon (Si) metal-oxide-semiconductor field-effect transistor (MOSFET) using the abundant Si as the substrate and silicon dioxide (SiO_2) as the dielectric oxide of the transistor has become the basic building block of integrated circuits (IC). Enabled by MOSFET scaling, the number of transistors per chip increases tremendously in the past half century to meet the growing needs for electronic devices for computing, communication, and other applications. This persistent trend of transistor scaling was predicted by G. Moore in 1965 and is commonly referred to as Moore's law that the number of transistors on a chip doubles about every 24 months [2].

The classical MOSFET scaling requires that transistor dimensions (gate length L_G, gate width W, dielectric thickness t_{ox}, etc.) scale accordingly with the decrease of the supply voltage V_{DD}. The first benefit of the scaling is to make transistors smaller to increase the packing density every new generation, resulting in a chip with more functionality in a given area. Today, more than 100 million MOSFETs using Intel 22-nm technology can fit onto the head of a pin with

diameter of 1.5 mm [3]. Another advantage is to improve the circuit speed to obtain more sophisticated computing capability. In addition, the scaling leads to the average selling price per transistor falling more than 6 orders of magnitude from the year 1970 to 2000 [4], stimulating many exciting new applications, such as the tablet computer and smartphone. Finally, it is necessary to reduce power consumption. If the power consumption had not been scaled accordingly, running a microprocessor (operating a billion transistors at 2 GHz) using the 1970's 10-μm technology would require the power output of a power plant [5]. In brief, this trend enabled by the MOSFET scaling towards higher packing density, faster speed, reduced cost, and lower power consumption per function has become a driving force of technological change [6].

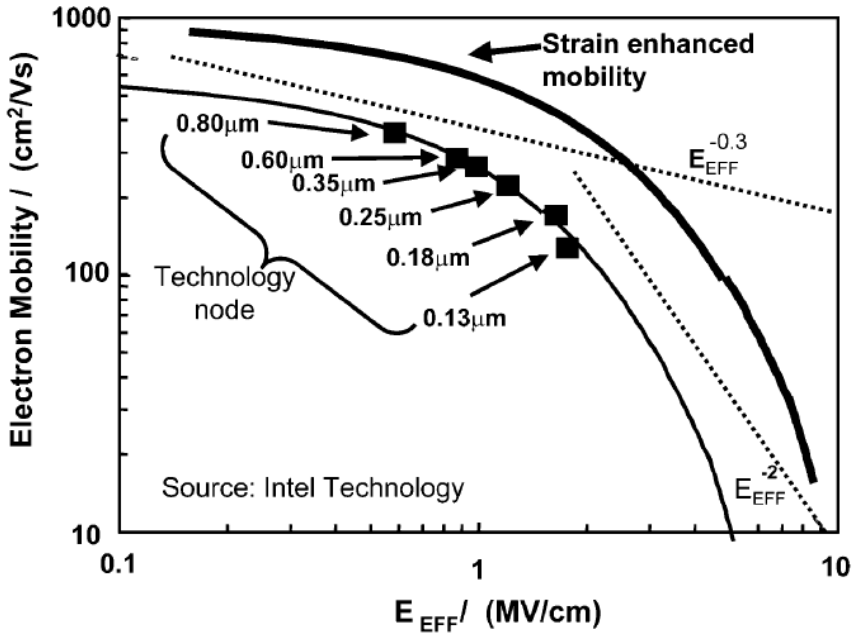


Fig. 1.1. Electron mobility versus technology scaling trend for various technology nodes. The electron mobility decreased from 400 cm^2/V-s at the 0.80-μm node to 120 cm^2/V-s at the 0.13-μm node. Fig. 1.1 reprinted from Ref. [8], with permission from IEEE Electron Devices Society, Copyright 2004.

This classical scaling was sufficient to deliver device performance improvement until the 0.13-μm node [7], when we reached the new millennium. Fig. 1.1 shows the electron mobility versus technology scaling trend for various technology nodes. As transistors are scaled to the sub-micrometer regions, it is difficult to improve MOSFET drive current I_{DSat} by just reducing L_G, as the effective carrier mobility μ_{eff} in the channel reduces monotonically from 400 cm^2/V-s at the 0.80-μm node to 120 cm^2/V-s at the 0.13-μm node.

The mobility degradation should result from the increasing scattering during carrier transport, due to the combined effect of the increasing channel doping concentration N and effective vertical electrical field E_{eff}. Following the classical scaling trend, both N and E_{eff} increase as the device dimensions decrease. The empirical relationships between μ_{eff} and N and between μ_{eff} and E_{eff} are given by Equations (1.1) [9] and (1.2) [10], respectively

$$\mu_{eff} = \mu_0 e^{-P_c/N} + \frac{\mu_{\max}}{(N/C_r)^{\alpha}+1} - \frac{\mu_1}{(C_S/N)^{\beta}+1}, \tag{1.1}$$

$$\mu_{eff} = \mu_0 \left(\frac{E_{eff}}{E_0}\right)^{-1/3}, \tag{1.2}$$

where $\mu_{\max}$ is the highest carrier mobility in bulk semiconductor, P_c, μ_0, μ_1, C_r, C_s, α, β and E_0 are the empirical parameters with positive values obtained by fitting the experimental results.

1.1.2 Challenges and Innovations in Scaling at Sub-100 nm Nodes

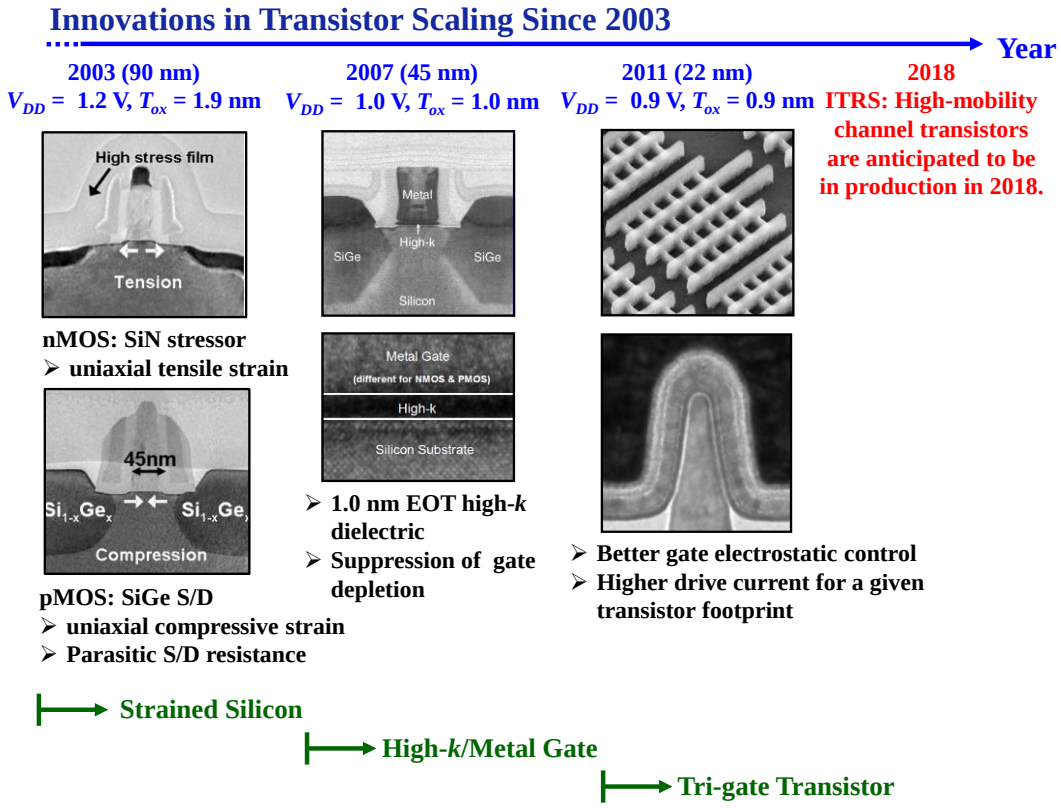


Fig. 1.2. Innovations in MOSFET scaling with the introduction of strain silicon, high-*k*/metal gate and tri-gate transistor technologies since 2003. Strained silicon technology was introduced to enhance the electron mobility of n-MOSFETs realized with silicon nitride high stress film and hole mobility of p-MOSFETs realized with silicon germanium source/drain stressors at the 90-nm node. The transistors integrated with high-*k*/metal gate technology instead of using SiO_2/polysilicon gate were in mass production to achieve lower gate leakage current and suppress the gate depletion at the 45-nm node. The revolutionary tir-gate transistors were released to achieve better gate electrostatic control and smaller footprint at the 22-nm node. Fig. 1.2 reprinted from Refs. [8], [13] and [17], with permission from IEEE Electron Devices Society, Copyright 2004, 2007, and 2012.

Continual innovations in transistor materials and structures have been developed to sustain Moore's law over the past decade as shown in Fig. 1.2. Particularly, strained silicon technology was introduced at the 90-nm technology in 2003 to offset the undesired mobility degradation as shown in Fig. 1.1 [8]. A silicon nitride capping layer is deposited on top of the n-MOSFET to induce uniaxial tensile strain in the channel to enhance the electron mobility. For p-

MOSFET, silicon germanium is utilized as the source and drain (S/D) to induce uniaxial compressive strain in the channel to enhance hole mobility and reduce S/D parasitic resistance R_{SD}.

SiO_2 has been the favored dielectric layer for Si MOSFET since the very beginning, and its thickness was successfully reduced to 1.2 nm at 65-nm node [11]. However, there is no room left for further scaling such a thin SiO_2 (only about four atomic layers), as any thickness reduction would result in the gate leakage current becoming unmanageable [12]. By utilizing an alternative gate dielectric using high dielectric constant (high-k) material with an equivalent oxide thickness (EOT) of 1.0 nm at the 45-nm node in 2007, n- and p-MOSFET gate leakage currents are reduced by more than 25 times and 1000 times, respectively [13]. In addition, the depletion region of gate electrode made of polysilicon, which acts like an additional dielectric layer, leads to a lower inversion carrier density and drive current. This issue is resolved by switching from the highly doped semiconductor gate to metal gate.

Other than gate leakage current discussed in the last paragraph, another important component of off-state current I_{OFF} is the S/D leakage current due to the insufficient gate control of the potential along a sub-surface leakage path. As the gate length reduces, the drain gains control of the channel potential, while the gate comparatively loses control [14]. Therefore, the drain voltage allows leakage current to flow at the sub-surface region by pulling down the potential barrier near the source region. To circumvent this scaling limitation, multiple-gate transistor or fin field-effect transistor (FinFET) structure is proposed [15]-[17]. With better gate electrostatic control from more than one side of the channel, this thin fin design reduces S/D leakage current significantly. Consequently, the introduction

of multiple-gate transistors at Intel's 22-nm technology in 2011 reverses the trend of increasing I_{OFF} at recent technology nodes [5].

1.1.3 The Use of High-Mobility Channel Materials

Unlike in the long channel transistors, carrier transport in the extremely scaled transistors in sub-100 nm regime is quasi-ballistic or ballistic. I_{DSat} of a transistor operating in quasi-ballistic or ballistic regime is limited by the thermal injection velocity v_{inj} and is given by Equation 1.3 or Equation 1.4 [18]-[19],

$$I_{DSat} = qN_{S,Source}v_{inj}\frac{1-r_C}{1+r_C} = C_{ox}Wv_{inj}\left(\frac{1-r_C}{1+r_C}\right)\left(V_{GS}-V_{TH}\right) \tag{1.3}$$

$$I_{DSat} = qN_{S,Source}v_{inj} = C_{ox}Wv_{inj}\left(V_{GS}-V_{TH}\right) \tag{1.4}$$

where q is the elementary charge, $N_{S,\,Source}$ is the carrier concentration near the source edge, r_c is the backscattering coefficient which is a measure of the number of carrier that backscatter to the source, C_{ox} is the gate oxide capacitance, V_{GS} is the gate voltage that equals to V_{DD} when the transistor is turned on, and V_{TH} is the threshold voltage. Experimentally, it was found that v_{inj} is proportional to low-filed mobility that is determined by conductivity effective mass [20]-[21]. Therefore, achieving small effective mass and thereby high low-field mobility is now critical to obtain high v_{inj} and I_{DSat}.

Beyond strained silicon technology, the use of high-mobility materials could be another solution to achieve high injection velocity and therefore drive current due to their high intrinsic bulk carrier mobilities and low conductivity effective mass. In the last decade, great deal of research is focused on high-

mobility germanium (Ge) and III-V compound semiconductors as alternative channel materials at future technology nodes [22]-[34].

The so-called high-mobility channel logic technology is anticipated to be in production in 2018 according to the International Technology Roadmap for Semiconductors (ITRS) (Fig. 1.2) [35]. To see the benefit of high-mobility channel transistors over Si channel transistors, Fig. 1.3 shows the comparison of transfer characteristics I_{DS} - V_{GS} between a high-mobility channel MOSFET (the red dashed curve) and a Si channel MOSFET (the black solid curve) in the saturation region ($V_{DS} = V_{DD}$). Compared with the Si channel MOSFET, the high-mobility channel transistor with a higher v_{inj} allows a higher on-state current I_{ON} at the approximately same I_{OFF} for a given gate overdrive voltage ($V_{DD} - V_{TH}$), resulting in an improved circuit speed determined by I_{ON}/CV_{DD}. On the other hand, the high-mobility channel transistor can also achieve a reduced supply voltage $V_{DD,Reduced}$ to maintain the same I_{ON} and approximately same I_{OFF}. This can be used for low operating power (LOP) technology due to the ability of achieving a low dynamic power determined by CV_{DD}^2. Table 1.1 shows the comparison of the Si channel high-performance (HP) and LOP technologies, and the high-mobility channel logic technology [35]. Here we only list the ratios in relation to the values in HP technology. Thus, not only does the technology using high-mobility materials offer higher speed than HP technology, but does so with the same low dynamic power as LOP technology.

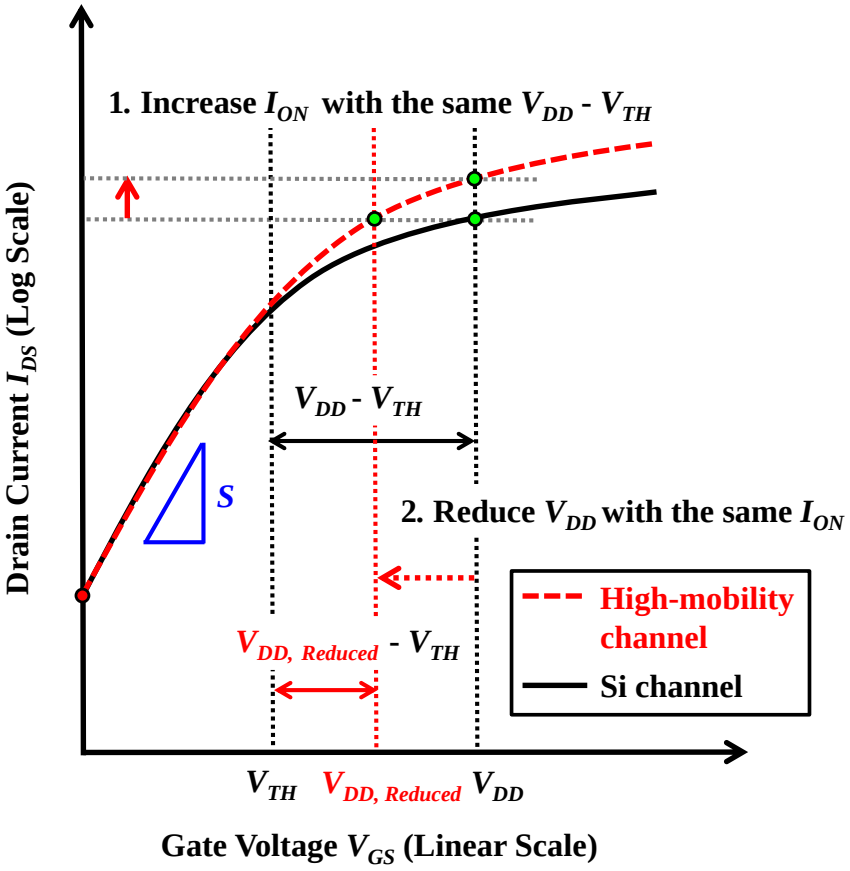


Fig. 1.3. Transfer characteristics I_{DS} - V_{GS} of a high-mobility channel MOSFET (red dashed curve) and a Si channel MOSFET (black solid curve) in the saturation region, respectively. High-mobility channel MOSFET can achieve an increased I_{ON} and approximately same I_{OFF} with the same gate overdrive voltage. In addition, high-mobility channel MOSFET can maintain the same I_{ON} and approximately same I_{OFF} with a smaller gate overdrive voltage.

Table 1.1. Comparison of Si channel HP and LOP technologies, and high-mobility channel technology [35]. The ratios in relation to the values in HP technology are listed.

	Si channel		High-mobility channel
	HP	LOP	
Speed (I_{ON}/CV_{DD})	1	0.5	1.5
Dynamic power (CV_{DD}^2)	1	0.5	0.6

1.1.4 Why $Ge_{1-x}Sn_x$?

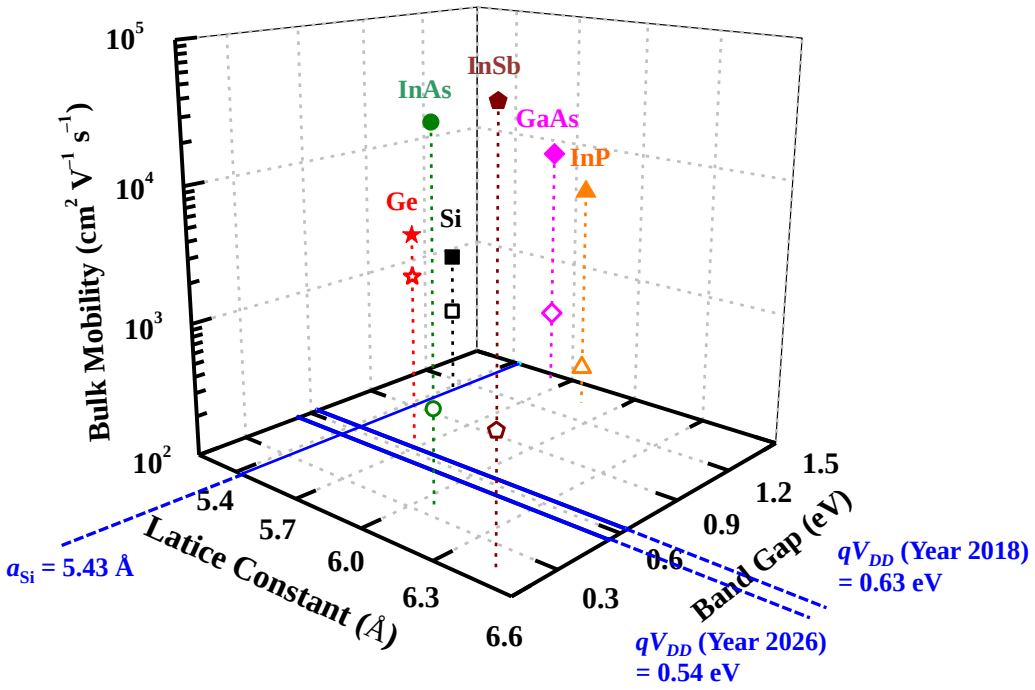


Fig. 1.4. Plot of the bulk mobilities, lattice constants, and band gaps for silicon, germanium and a variety of III–V compound semiconductors. Filled symbols and open symbols represent electron mobility and hole mobility, respectively. The lattice constant of Si (5.43 Å) and the supply voltages for the years 2018 (0.63 V) and 2026 (0.54 V) are highlighted. The material parameters are taken from Ref. [36].

Fig. 1.4 plots the bulk carrier mobilities, lattice constants, and band gaps for Si, Ge and a variety of III–V compound semiconductors including gallium arsenide (GaAs), indium phosphide (InP), indium arsenide (InAs), and indium antimonide (InSb). The band gap is important for selecting the next-generation channel material, as it affects the transistor off-state behavior. If the band gap is too small (e.g. 0.35 eV for InAs and 0.17 eV for InSb) relative to V_{DD} (which varies from 0.63 V in 2018 to 0.54 V in 2026 according to ITRS [35]), the transistor would suffer from high S/D leakage current resulting from not only thermionic emission but also band-to-band tunneling. From Fig. 1.4, it can be

observed that Ge has a sufficiently large band gap of 0.66 eV for future technology nodes.

For a high-mobility channel technology to be compatible with today's Si manufacturing process, the cost-effective integration of high-mobility materials on a large Si substrate is imperative. Due to the fragility of the high-mobility materials, the production and use of large bulk wafers made of such materials for device fabrication is challenging. In addition, incorporating the less abundant and more expensive high-mobility materials on a large (e.g. 300 mm) Si wafer reduces the considerable costs associated with developing non-Si bulk substrates. However, the direct growth of these materials on Si is prohibited by the massive defect formation that would arise from large lattice mismatch between the high-mobility material and Si. Therefore, integration of high-mobility materials on Si requires special techniques such as buffer-layer growth [33],[37]-[41] and aspect-ratio-trapping growth [42]-[45] techniques. Among the high-mobility materials as shown in Fig. 1.4, Ge has the smallest lattice mismatch to Si, making it easier to integrate on a Si substrate. In addition, the growth of polar materials such as III-V compound semiconductors on a non-polar material like Si results in crystallographic defects known as anti-phase boundaries (APBs) [46]-[47]. Ge, which is also non-polar, suffers no such problem.

Apart from having a reasonably large band gap and the lowest lattice mismatch to Si, Ge has the highest bulk hole mobility of 1900 cm^2/V-s and reasonably high bulk electron mobility of 3900 cm^2/V-s. The incorporation of tin (Sn) into the Ge lattice to form germanium-tin ($Ge_{1-x}Sn_x$) alloys shows promise for engineering the electronic properties, based on calculations using the empirical pseudopotential method done by K. L. Low *et al.* [48]. First, the light-hole

effective mass of $Ge_{1-x}Sn_x$ decreases as the Sn composition increases, resulting in the possible improvement of drive current of $Ge_{1-x}Sn_x$ p-MOSFETs by increasing the thermal injection velocity of holes [20]-[21]. In addition, the incorporation of a small amount of Sn ($x < 0.11$) reduces the longitudinal electron effective mass at L-point and therefore the conductivity effective mass of electrons, showing a way of achieving higher drive current of $Ge_{1-x}Sn_x$ n-MOSFETs by increasing the thermal injection velocity of electrons [20]-[21]. Fig. 1.5(a) shows the full band structure of $Ge_{0.89}Sn_{0.11}$ along high symmetry lines in the Brillouin zone. The calculated band gap energies of X, L, and Γ-point at various Sn compositions are shown in Fig 1.5(b). Notably, the transition from indirect to direct band gap should be achieved by alloying with Sn composition of 11% and above, resulting in a significant improvement of the thermal injection velocity of electrons.

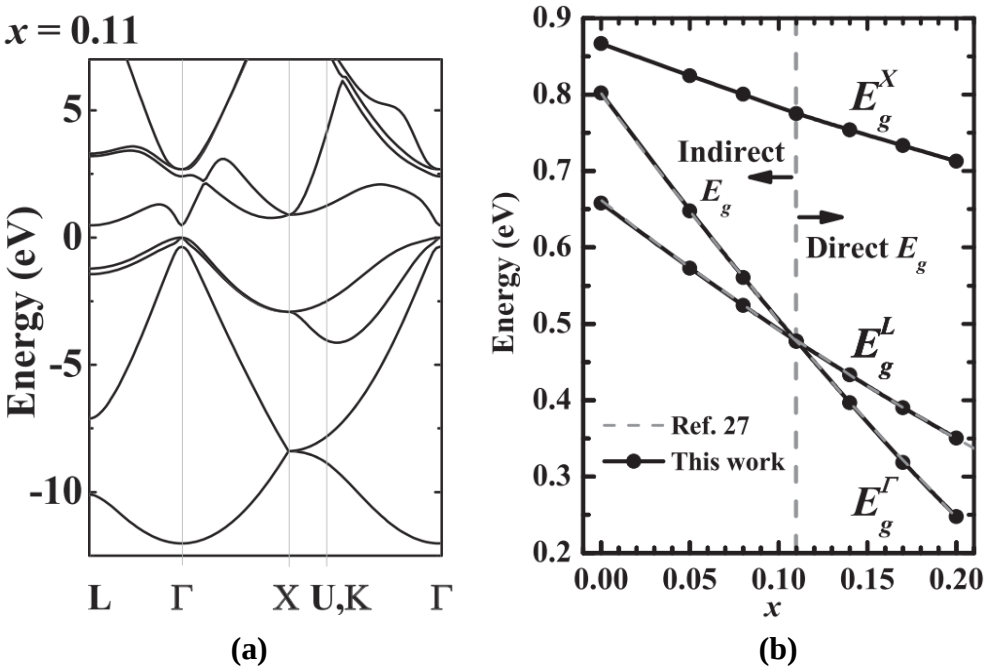


Fig. 1.5. (a) Full band structure of $Ge_{0.89}Sn_{0.11}$ along high symmetry lines in the Brillouin zone. (b) The calculated band gap energies of X, L, and Γ-point at various Sn compositions. Fig. 1.5 reprinted from Ref. [48], with permission from American Institute of Physics, Copyright 2012.

In short, $Ge_{1-x}Sn_x$ is predicted to have even smaller effective mass for electrons and holes and consequently higher carrier mobilities than Ge. The tradeoffs are a larger lattice constant and a smaller band gap, but lattice mismatch to Si is less of an issue with the use of growth techniques such as the aspect-ratio-trapping growth technique, while a sufficiently large band gap can be maintained for low Sn compositions. Therefore, $Ge_{1-x}Sn_x$ could potentially be an even more promising high-mobility material than Ge to replace Si as the channel material in MOSFETs. Furthermore, high-quality single-crystalline $Ge_{1-x}Sn_x$ has been successfully grown using molecular beam epitaxy (MBE) [49]-[57] and chemical vapor deposition (CVD) [58]-[60], and is ready for being developed as an important technical option for ultra-scaled MOSFET technologies.

To realize high-performance transistors using high-mobility materials as the channel, remarkable effort has been made from the academia and industry over the last decade. Take p-MOSFETs for example, Fig. 1.6 shows the research trend towards higher hole mobility from literatures reported on the flagship technical conferences: International Electron Devices Meeting (IEDM) and Symposium on VLSI Technology (VLSIT). The demonstrations of high-performance transistors using high-mobility materials such as $Si_{1-y}Ge_y$, Ge, and indium gallium antimonide ($In_{1-c}Ga_cSb$) have been reported in Refs. [22] - [34]. Please note that the mobility value in Ref. [22] is extracted at the effective field of 1 MV/cm, as the authors reported mobility as a function of effective field ranging from 0.7 MV/cm to 2.5 MV/cm. For the rest of references in Fig. 1.6, the mobility value is extracted at the effective field of 0.3 MV/cm, if mobility was plotted as a function of effective field, or is extracted at the inversion carrier

density of 5×10^{12} cm^{-2}, if mobility was plotted as a function of inversion carrier density.

Recently, $Ge_{1-x}Sn_x$ p-channel MOSFETs were demonstrated to have higher hole mobility than Ge control devices by experiment [61]-[63]. The high-quality $Ge_{1-x}Sn_x$ films were epitaxially grown on n-type Ge (100) substrates using MBE system. As an emerging material for scaling supply voltage towards 0.5 V for high performance transistors at sub-10 nm technology nodes [64], much research work needs to be done on $Ge_{1-x}Sn_x$, which is the focus of the work in this thesis.

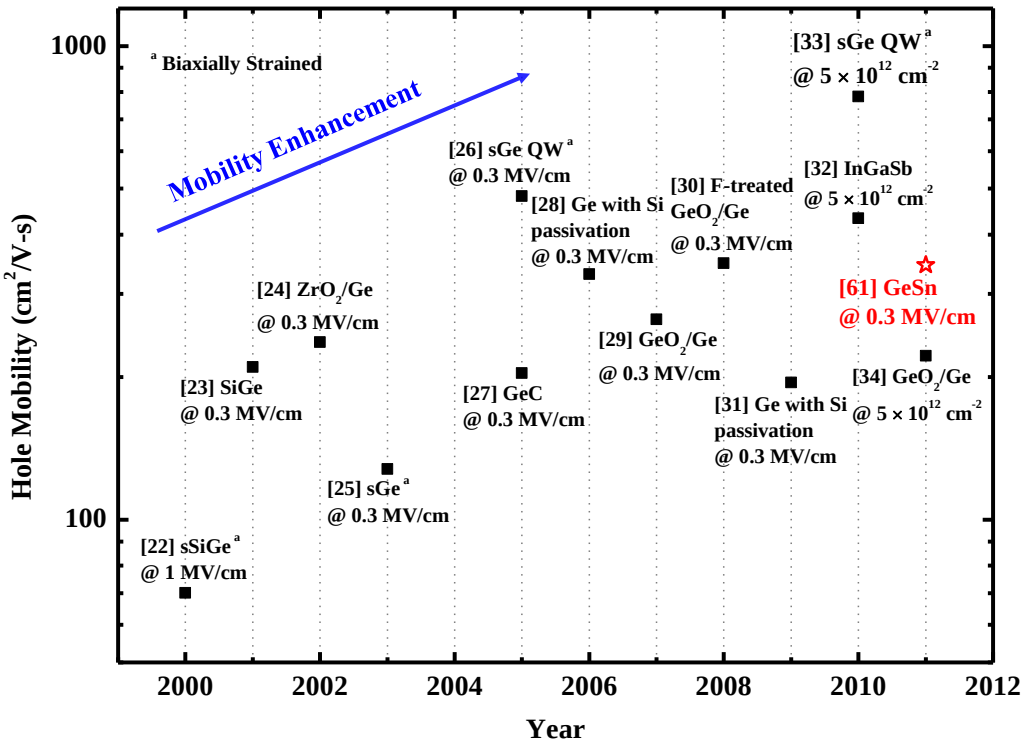


Fig. 1.6. Research on channel materials for p-MOSFETs from 2000 to 2011 for achieving high hole mobility [22]-[34]. The world's first $Ge_{1-x}Sn_x$ channel p-MOSFET is demonstrated in the year 2011 [61]. Please note that the mobility value in Ref. [22] is extracted at the effective field of 1 MV/cm, as the authors reported mobility as a function of effective field ranging from 0.7 MV/cm to 2.5 MV/cm. For the rest of references, the mobility value is extracted at 0.3 MV/cm, if mobility was plotted as a function of effective field, or is extracted at the inversion carrier density of 5×10^{12} cm^{-2}, if mobility was plotted as a function of inversion carrier density. The figure is modified from Fig. 1 in Ref. [61].

1.2 Thesis Outline and Original Contributions

Chapter 2 proposes a complementary metal-oxide-semiconductor (CMOS) using $Ge_{1-x}Sn_x$ n- and p-channel transistors integrated on Si substrate for sub-10 nm technology nodes. Many technical challenges have to be overcome for $Ge_{1-x}Sn_x$ MOSFETs before its possible mass production in the future. These include cost-effective integration of high-mobility $Ge_{1-x}Sn_x$ on large Si substrates, formation of high-quality gate stack, source/drain engineering for low-resistance.

This thesis aims to address various challenges in realizing high-mobility $Ge_{1-x}Sn_x$ MOSFETs for future logic applications. The technical contents discussed in this thesis are documented in Chapters 3 to 5.

Chapter 3 reports a surface passivation by treatment with ammonium sulfide [$(NH_4)_2S$], which is explored for the gate stack of high-mobility $Ge_{0.958}Sn_{0.042}$ p-MOSFETs. Single-crystalline $Ge_{0.958}Sn_{0.042}$ was epitaxially grown on Ge (100) substrate as the channel material. The $(NH_4)_2S$-passivated $Ge_{0.958}Sn_{0.042}$ p-MOSFETs show decent transfer and output characteristics, and demonstrate a higher peak μ_{eff} in comparison with those of other (100)-oriented $Ge_{1-x}Sn_x$ p-MOSFETs reported so far.

Chapter 4 investigates a thermally stable Pt-incorporated stanogermanide metallization scheme for $Ge_{1-x}Sn_x$ transistors. The surface of Ni/$Ge_{1-x}Sn_x$/Ge (100) sample becomes rough after annealing at 450 °C, which is the cause of the sharp increase in sheet resistance from 450 to 500 °C. The incorporation of Pt during the formation of Ni-stanogermanide was exploited to improve the thermal robustness by suppressing agglomeration during solid-state reactions between Ni and $Ge_{0.947}Sn_{0.053}$ at temperatures of 450 °C and above.

Chapter 5 documents the efforts towards highly doped n-type germanium-tin for low S/D resistance of $Ge_{1-x}Sn_x$ n-MOSFETs. Activation temperature as low as 400 °C was demonstrated to obtain active doping concentration of 2.1×10^{19} cm^{-3} for phosphorus-implanted $Ge_{0.976}Sn_{0.024}$. In addition, implant at elevated temperature of 400 °C was explored to maintain the single-crystallinity of $Ge_{0.976}Sn_{0.024}$ during implant and achieve a lower contact resistivity after activation at 450 °C as compared with the room-temperature implant.

This thesis ends with an overall conclusion and possible future research directions documented in Chapter 6.

Chapter 2

High-mobility Germanium-Tin Complementary Metal–Oxide–Semiconductor on Silicon: Benefits and Challenges

2.1 High-mobility Germanium-Tin CMOS on Silicon

As discussed in Chapter 1, germanium-tin ($Ge_{1-x}Sn_x$), which is predicted to have higher carrier mobilities μ_{eff} than germanium (Ge) [48], could potentially be a more promising high-mobility material than Ge to replace silicon (Si) as the channel material for future complementary metal-oxide-semiconductor (CMOS) technologies. Fig. 2.1 depicts a schematic of a group IV CMOS featuring high-mobility $Ge_{1-x}Sn_x$ n- and p-channel metal-oxide-semiconductor field-effect transistors (MOSFETs) integrated on Si. First, it is highly favorable to use a same material system (e.g. $Ge_{1-x}Sn_x$) for both n- and p-channel MOSFETs, as it can achieve process simplicity and consequently save considerable cost [65]. In addition, it is challenging to use a multiple material system (e.g. Ge p-MOSFETs and III-V n-MOSFETs [66]-[67]) with dissimilar chemistries and thermal properties on a single chip [68].

The key challenges highlighted in Fig. 2.1 have to be overcome before $Ge_{1-x}Sn_x$ CMOS becomes a strong candidate for sub-10 nm technology node applications. First, a cost-effective approach to integrating $Ge_{1-x}Sn_x$ on large Si

wafers is a crucial prerequisite. Second, a high-quality and thermodynamically stable gate stack for $Ge_{1-x}Sn_x$ MOSFETs has to be realized to fully exploit the benefits of its high bulk mobilities. Third, for source/drain (S/D), it is essential to develop thermally stable self-aligned S/D contact metallization and achieve high doping concentration for low S/D parasitic resistance $R_{S/D}$ for $Ge_{1-x}Sn_x$ MOSFETs. The current status and future perspectives of research on the above three aspects will be elucidated in detail in this Chapter.

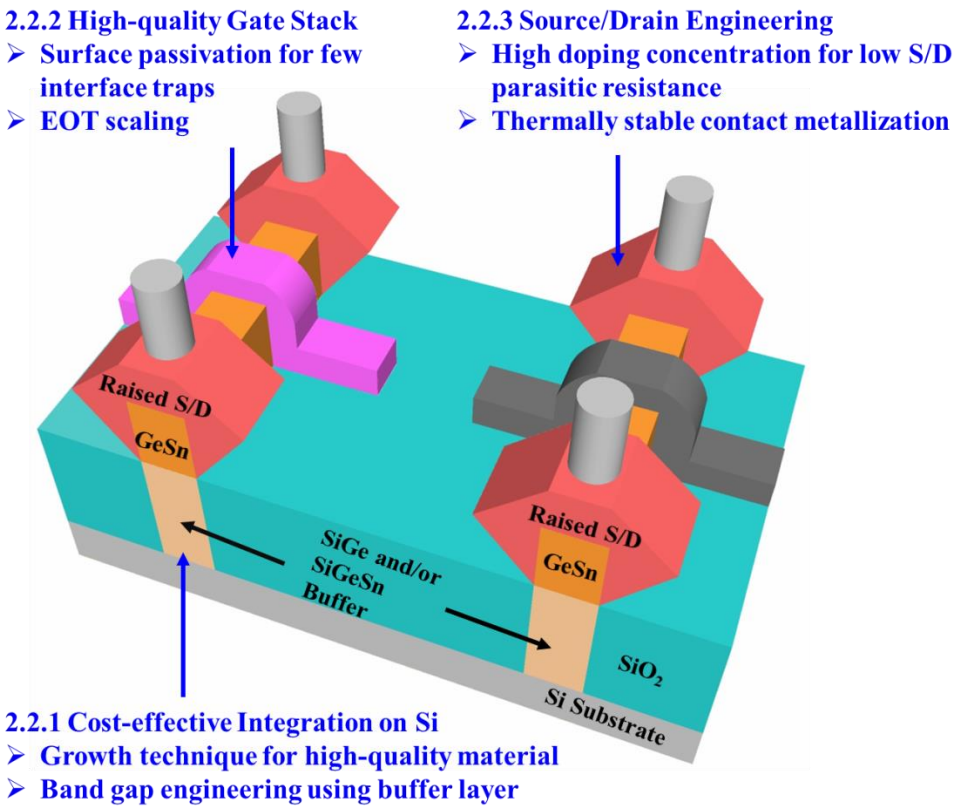


Fig. 2.1. Schematic of a group IV CMOS featuring $Ge_{1-x}Sn_x$ n- and p-channel transistors integrated on Si substrate. The key technical challenges faced are highlighted.

2.2 Key Challenges for High-mobility $Ge_{1-x}Sn_x$ CMOS on Si

2.2.1 Integration of $Ge_{1-x}Sn_x$ on Si

In this subsection, we first review the breakthrough of integrating Ge on Si by the aspect-ratio-trapping growth technique [42]-[45]. This approach can be utilized for growing high-quality $Ge_{1-x}Sn_x$ on Si cost-effectively for high-performance logic applications. In addition, if silicon-germanium ($Si_{1-y}Ge_y$) [69] and/or silicon-germanium-tin ($Si_{1-x-y}Ge_ySn_x$) [70]-[72] is used as the buffer layer for the $Ge_{1-x}Sn_x$ growth, there is an additional benefit of carrier confinement in the $Ge_{1-x}Sn_x$ layer due to the conduction and valence band offsets between the channel layer and the buffer layer.

a. The Aspect-Ratio-Trapping Growth Technique

Due to a large lattice mismatch of 4.2% between Ge and Si, growing Ge directly on Si generally leads to a large amount of dislocations, which are formed at the Si/Ge interface and are terminated at the top surface. In the early days, to accommodate the lattice mismatch, a thick buffer layer, which comprises a $Si_{1-y}Ge_y$ layer with composition gradually graded [Fig. 2.2(a)] [33],[37]-[40] or abruptly changed in a few steps [41], can be grown between the Si substrate and the top Ge layer. This results in the top Ge layer with much fewer dislocations, as most of the defects are confined to the thick buffer layer as shown in cross-sectional transmission electron microscopy (XTEM) image in Fig. 2.2(b). However, this process is extremely costly, as the most advanced buffer systems still take a long time to grow several micrometers-thick buffer layers [33].

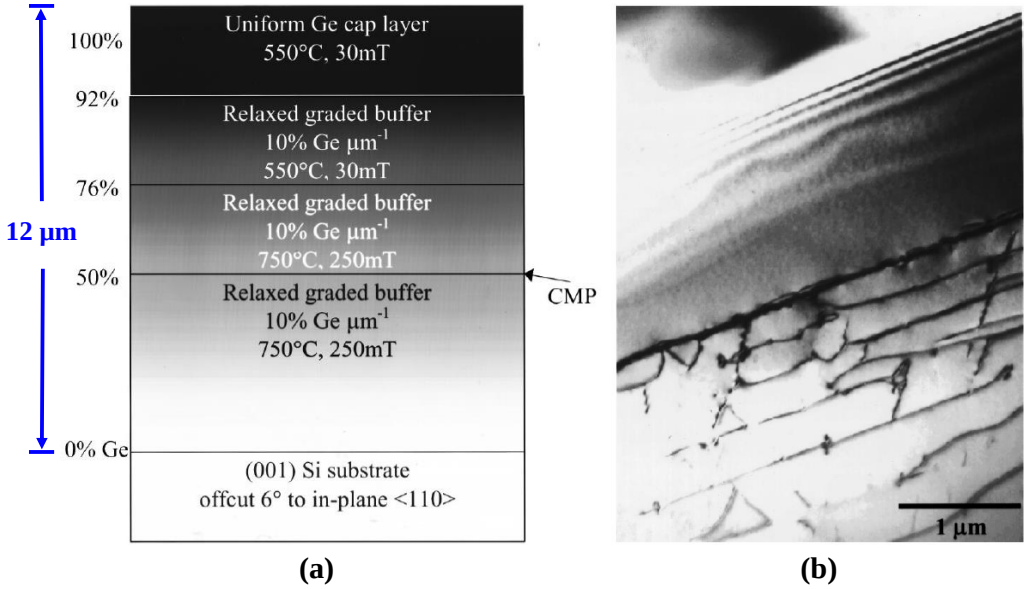


Fig. 2.2. (a) Schematic of the structure and growth conditions for Ge growth with graded $Si_{1-y}Ge_y$ buffer layer. The total epitaxial thickness is 12 µm. (b) XTEM image of the upper graded region and top Ge layer of the sample. With such a thick buffer layer, this method has allowed to grow Ge with a low dislocation density of 2.1×10^6 cm^{-2}. Fig. 2.2 reprinted from Ref. [39], with permission from American Institute of Physics, Copyright 1998.

To reduce the buffer-layer thickness, an aspect-ratio-trapping growth technique has been investigated for growing Ge (with or without $Si_{1-y}Ge_y$ buffer layer) within high-aspect-ratio silicon dioxide (SiO_2) trenches patterned on Si substrates [42]-[45]. The principle is to terminate dislocations at the oxide sidewalls and therefore to confine them to the bottom layer, resulting in a defect-free top layer [Fig. 2.3(a)]. In the {111} <110> diamond cubic slip systems, the misfit dislocations resulting from lattice mismatch between Ge and Si lie along <110> directions in the (100) growth plane. The threading dislocations then propagate along {111} planes in <110> directions, which are 45° to the (100) plane. Therefore, if the aspect ratio is greater than 1 [the dashed lines labeled in Figs. 2.3(b) and (c)], crystallography dictates that the threading dislocations will be trapped by the oxide sidewalls [42].

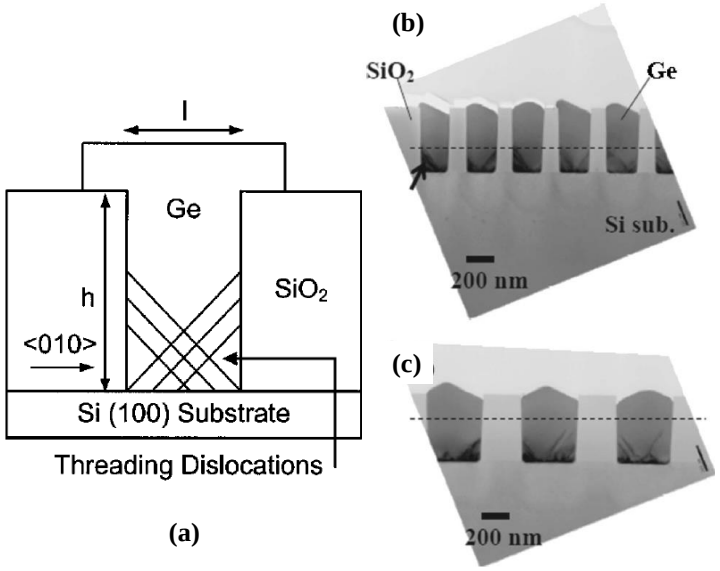


Fig. 2.3. (a) Schematic demonstrates the principle of the aspect-ratio-trapping growth technique. XTEM images of Ge in trenches of (b) 200 nm width and (c) 400 nm width showing dislocations that originate at the Ge/Si interface trapped by the sidewalls. The dashed lines indicate where the aspect ratio is 1. The schematic and TEM images are taken from, respectively. Fig. 2.3 reprinted from Refs. [42] and [43], with permission from American Institute of Physics, Copyright 2000 and 2007.

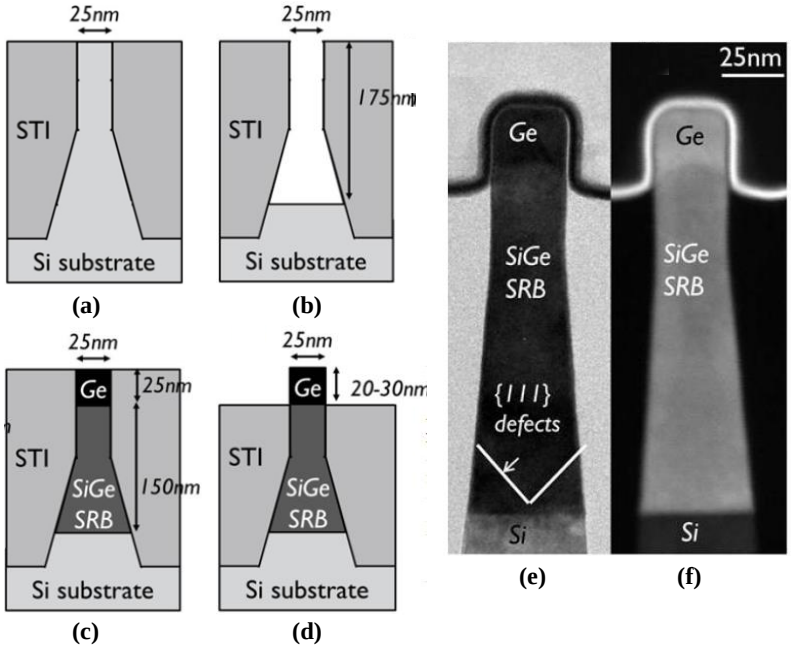
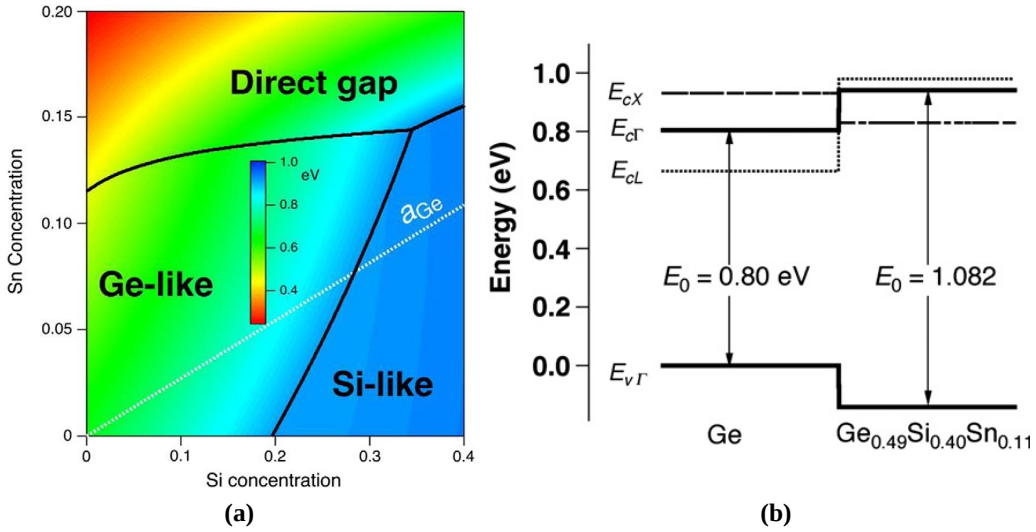


Fig. 2.4. Schematics depict the process of forming Ge fin using the aspect-ratio-trapping technique: (a) formation of Si bulk fin, (b) etching of 175-nm Si, (c) growth of 150-nm $Si_{0.25}Ge_{0.75}$ and 25-nm Ge, and (d) recess etching of STI. (e) XTEM and (f) high angle annular dark field-scanning transmission electron microscopy (HAADF-STEM) images of the Ge fin. Fig. 2.4 reprinted from Ref. [45], with permission from IEEE Electron Devices Society, Copyright 2013.

This method shows promise for growing Ge on Si with much thinner buffer layer. Using this approach, L. Witters *et al.* demonstrated Ge fin field-effect-transistors (FinFETs) that are integrated on 300-mm Si wafers [45]. Starting from a Si (100) wafer, a 175-nm SiO_2 trench with a large aspect ratio is formed [Figs. 2.4(a) and (b)]. 150-nm $Si_{0.25}Ge_{0.75}$ and 25-nm Ge are then deposited in the trench [(Fig. 2.4(c)]. The process is completed by recess etching of the shallow trench isolation (STI) to expose the Ge fin [Fig. 2.4(d)], as defects are confined to the bottom [Figs. 2.4(e) and (f)]. However, it should be noted that as the defect trapping at the oxide side walls is limited to one direction, there is no confinement of defects along the direction of the fin [73]. Further efforts need to be devoted to solve this problem.

b. Band Gap Engineering Using Buffer Layer

The aspect-ratio-trapping technique discussed above may provide a good solution to integrate $Ge_{1-x}Sn_x$ channel transistors on large Si substrates cost-effectively. Furthermore, $Si_{1-y}Ge_y$ [69] and/or $Si_{1-x-y}Ge_ySn_x$ [70]-[72] can be used as the buffer layer with the electrostatic benefit due to the conduction and valence band offsets between the channel and buffer layer. Fig. 2.5(a) shows the calculated electronic-character diagram of $Si_{1-x-y}Ge_ySn_x$ mapping the electronic structure versus Si and Sn concentrations [72]. Particularly, $Si_{1-x-y}Ge_ySn_x$ with a fixed Si-to-Sn ratio at ~4 (the labeled white dotted line) can be lattice-matched to Ge and shows a tunable band gap [70]-[72]. The Ge/$Si_{1-x-y}Ge_ySn_x$ interface can have Type-I band offsets to confine the carriers in Ge [Fig. 2.5(b)]. As Sn incorporation into Ge further reduces the band gap, so does the $Ge_{1-x}Sn_x$/$Si_{1-x-y}Ge_ySn_x$ interface.



(a) **(b)**

Fig. 2.5. (a) Calculated electronic-character diagram of $Si_{1-x-y}Ge_ySn_x$ alloys mapping the electronic structure versus Si and Sn concentrations. The white dotted line designates the composition with a fixed Si-to-Sn ratio at ~4 to exactly match the Ge lattice constant. (b) Calculated band alignment at a strain-free $Ge/Si_{1-x-y}Ge_ySn_x$ interface, showing Type-I band offsets to confine the carriers in the Ge layer. Fig. 2.5(a) reprinted from Ref. [72], with permission from Elsevier, Copyright 2014. Figure (b) reprinted from Ref. [71], with permission from Elsevier, Copyright 2010.

2.2.2 Formation of High-quality Gate Stack for $Ge_{1-x}Sn_x$ MOSFETs

Unlike SiO_2, the native oxides of Ge-based materials are unstable. The presence of Ge suboxides leads to a high density of interface traps resulting from dangling bonds at the dielectric/channel interface [74]-[75]. These interface traps can significantly degrade the μ_{eff} of Ge or $Ge_{1-x}Sn_x$ MOSFET by severe Coulomb scattering [76]. Without a proper passivation process to prevent native oxide formation, direct deposition of high-k dielectrics such as aluminium oxide (Al_2O_3) [77], zirconium oxide (ZrO_2) [78], hafnium oxide (HfO_2) [79], and lanthanum aluminate ($LaAlO_3$) [80] on Ge substrates result in high interface trap density D_{it}, low μ_{eff} for both electrons and holes, and high gate leakage current J_G. In addition, the subthreshold swing and off-state leakage current would degrade due to these traps.

Although the incorporation of Sn can achieve enhanced mobilities than Ge, Sn was found to segregate to the top surface right after the epitaxial growth of $Ge_{1-x}Sn_x$ [81]. In addition, subsequent high-temperature processes for transistor fabrication may further degrade the material quality [82]-[83]. Particularly, Sn segregation at the high-k/$Ge_{1-x}Sn_x$ interface would degrade the interface quality and the carrier mobility would be significantly affected. Therefore, the use of a low thermal budget process to form a high-quality gate stack for $Ge_{1-x}Sn_x$ MOSFETs is therefore imperative. This subsection focuses on the methods of forming high-quality gate stack for $Ge_{1-x}Sn_x$ MOSFETs.

a. Low-temperature Silicon Passivation

The use of an ultrathin interfacial Si layer inserted between the high-k dielectric and the channel of Ge p-MOSFETs is one of the most important technologies to suppress the mobility degradation [28],[33],[84]-[85]. In addition, high-performance Si-passivated $Ge_{1-x}Sn_x$ p-MOSFETs with a high effective mobility of 220 cm^2/V-s at an effective vertical electric field of 1 MV/cm have been demonstrated [61].

For $Ge_{1-x}Sn_x$ p-MOSFETs [61],[63],[86]-[91], the Si layer is grown at a low temperature of 370 °C by an ultra-high-vacuum chemical vapor deposition (UHVCVD) system with disilane (Si_2H_6) as the precursor. Fig. 2.6(a) shows a schematic illustrating the key features of $Ge_{1-x}Sn_x$ p-MOSFET with the passivation layer. The key concept is to suppress carrier scattering for $Ge_{1-x}Sn_x$ p-MOSFET resulting from few interface traps and moving the interface traps further away from the channel by inserting such a thin interface layer [Fig. 2.6(b)] [63]. In addition, the carriers (holes) are confined in the high-mobility $Ge_{1-x}Sn_x$ channel

due to the valence band offset at the Si/$Ge_{1-x}Sn_x$ interface. Fig. 2.6(c) shows a top-view scanning electron microscopy (SEM) image of a completed $Ge_{1-x}Sn_x$ p-MOSFET. XTEM and high-resolution TEM (HRTEM) images [Fig. 2.6(d)] reveal the existence of an ultrathin interfacial layer between the dielectric and channel.

However, the major issue of this surface passivation method is the inefficient scaling of equivalent oxide thickness (EOT) due to thickness of the interfacial layer. In addition, Si passivation might only be used for p-MOSFETs due to the negligible conduction band offset between $Ge_{1-x}Sn_x$ and Si. This results in electron trapping at the interfacial layer, the dielectric layer and their interface of Si-passivated $Ge_{1-x}Sn_x$ n-MOSFETs, which degrades the carrier mobility due to remote Coulomb scattering [92].

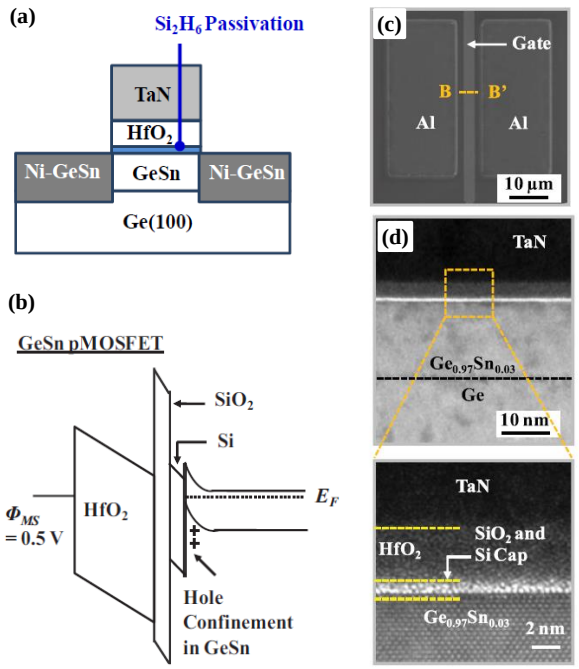


Fig. 2.6. (a) Schematic illustrating the key features of $Ge_{1-x}Sn_x$ p-MOSFET with Si passivation. (b) Band diagram of the $Ge_{1-x}Sn_x$ p-MOSFET operating in strong inversion regime. (c) Top-view SEM image of a completed $Ge_{1-x}Sn_x$ p-MOSFET. (d) XTEM image across line B–B' of the $Ge_{0.97}Sn_{0.03}$ show the good interface quality. The high-resolution image reveal the existence of an ultrathin interfacial layer between the dielectric and channel. Fig. 2.6 reprinted from Ref.[63], with permission from IEEE Electron Devices Society, Copyright 2012.

b. Indium Aluminum Phosphide Passivation

Another promising technique for passivating $Ge_{1-x}Sn_x$ surface is to use indium aluminum phosphide ($In_{1-a}Al_aP$). $In_{1-a}Al_aP$ with Al composition of 0.52 has a relatively large band gap of ~2.3 eV and is lattice-matched to Ge [93]. It has been successfully utilized as the passivation layer of high-performance Ge CMOS to achieve a record high electron mobility of ~958 cm^2/V-s at inversion carrier density of 6×10^{11} cm^{-2} for n-MOSFETs and a high peak hole mobility of ~390 cm^2/V-s for p-MOSFETs [94]. Prior to high-*k* dielectric deposition, an $In_{0.48}Al_{0.52}P$ layer is epitaxially grown on Ge surface at 650 °C using a metalorganic chemical vapor deposition (MOCVD) system [Fig. 2.7(a)]. The $In_{0.48}Al_{0.52}P$/Ge interface can achieve not only a valence band offset of ~0.86 eV but also a conduction band offset of ~0.84 eV [Fig. 2.7(b)] [93] to obtain good confinement for holes and electrons within the Ge channel layer [Fig. 2.7(c)]. Fig. 2.7(d) shows a top-view SEM image of a Ge fabricated MOSFET. XTEM [Fig. 2.7(e)] and HRTEM [Fig. 2.7(f)] images of the gate stack clearly shows the epitaxial interfacial layer between the dielectric layer and the Ge channel.

This interface passivation scheme can also be developed for $Ge_{1-x}Sn_x$ MOSFETs. However, as $Ge_{1-x}Sn_x$ is more thermally unstable than Ge [81]-[83], the temperature of $In_{1-a}Al_aP$ passivation should be reduced, as the pre-growth baking and growth temperatures are 650 °C [93]-[94]. Apart from the above two important passivation techniques, novel surface passivation techniques that can fulfill the necessary requirements – namely few interface traps and the capability of EOT scaling – need to be developed for $Ge_{1-x}Sn_x$ MOSFETs. This is the focus of Chapter 3 of this thesis.

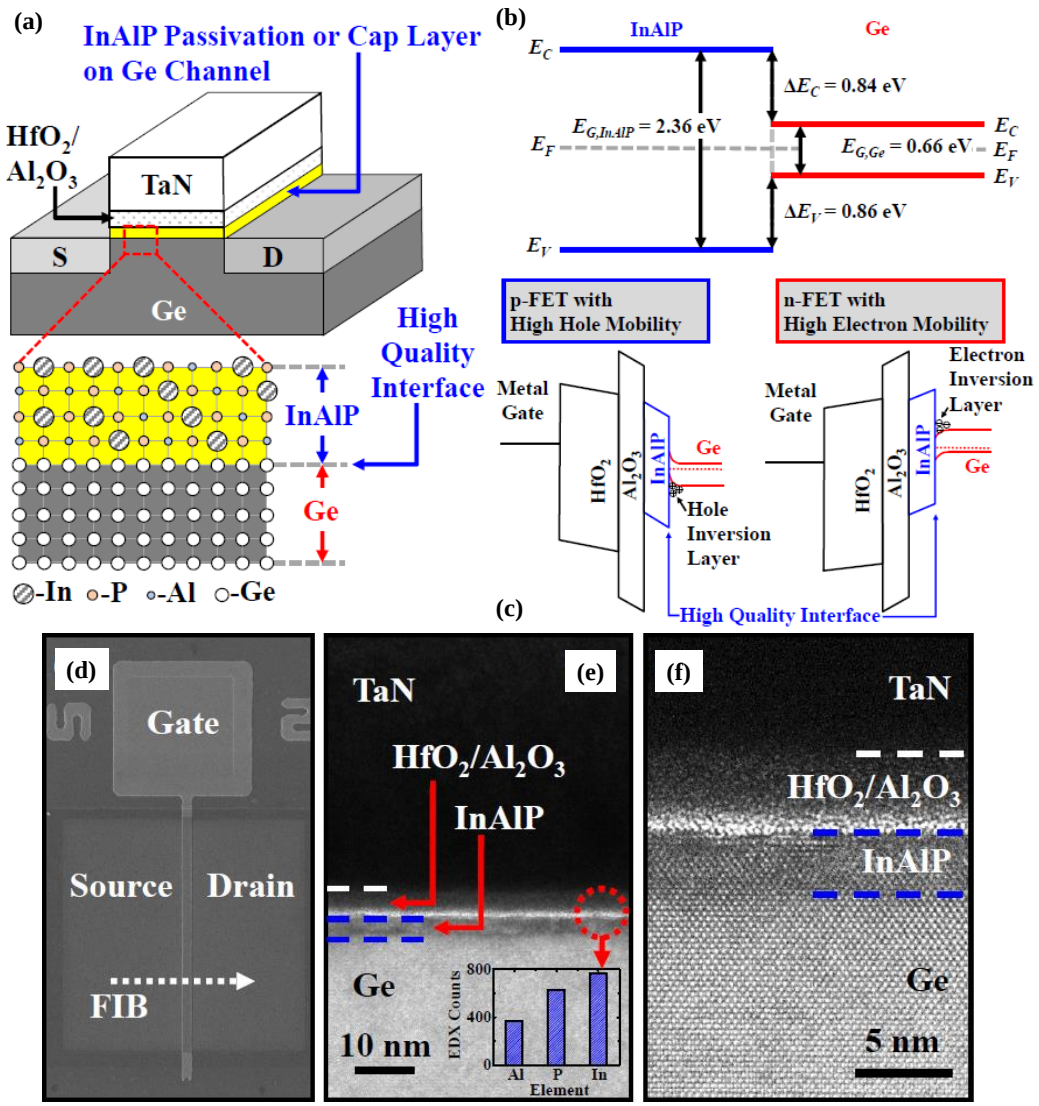


Fig. 2.7. (a) Schematic showing an $In_{1-a}Al_aP$ passivation scheme for Ge CMOS. The $In_{1-a}Al_aP$ layer is grown on the Ge surface prior to gate stack formation. (b) The $In_{1-a}Al_aP$-Ge interface has a conduction band offset of ~0.84 eV and a valence band offset of ~0.86 eV. (c) Band diagrams of an $In_{1-a}Al_aP$-capped Ge p-MOSFET (left) and an $In_{1-a}Al_aP$-capped Ge n-MOSFET (right) in strong inversion regime. Holes and electrons are confined within the Ge layer due to the large band offsets. (d) SEM image showing the structure of an $In_{1-a}Al_aP$-passivated Ge n-MOSFET. (e) TEM and (f) HRTEM images of the gate stack, clearly showing the epitaxial $In_{1-a}Al_aP$ passivation layer sandwiched between the Ge substrate and gate dielectrics. Figs. 2.7(a), (c)-(f) reprinted from Ref. [94], with permission from IEEE Electron Devices Society, Copyright 2013. Fig. 2.7 (b) reprinted from Ref. [93], with permission from American Institute of Physics, Copyright 2013.

2.2.3 Source/Drain Engineering

Apart from forming high-quality gate stack, it is critical to minimize $R_{S/D}$ of $Ge_{1-x}Sn_x$ MOSFETs by developing thermally stable self-aligned S/D contacts and achieving high doping concentration for low resistance S/D regions.

The total resistance R_{Total} is contributed by the channel resistance R_{CH} and $R_{S/D}$ [Fig. 2.8(a)]. R_{CH} decreases monotonically from the 90-nm technology node due to the combined effect of the use of mobility enhancement technology and channel length scaling [Fig. 2.8(b)]. In addition, the scaling of device dimensions such as S/D junction depth and metal contact area leads to the increase of $R_{S/D}$. As a result, $R_{S/D}$ becomes comparable to the R_{CH} at the 32-nm node [95], implying $R_{S/D}$ may be a bottleneck for achieving high I_{DSat} at the advanced technology nodes using high-mobility materials as the channel.

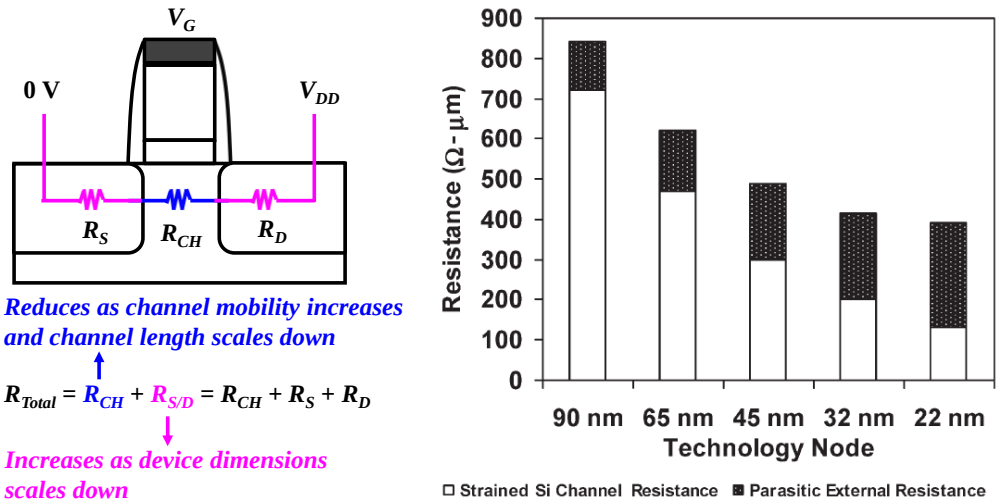


Fig. 2.8. (a) Schematic representing the R_{CH} and $R_{S/D}$. The sum of these resistances equals the R_{Total}. (b) Simulation showing R_{CH} and $R_{S/D}$ of n-MOSFET becoming equivalent at the 32-nm logic node. Fig. 2.8 (b) reprinted from Ref. [95], with permission from IEEE Electron Devices Society, Copyright 2008.

a. Thermally Stable Source/Drain Contacts for $Ge_{1-x}Sn_x$

The well-established self-aligned silicide and germanide processes are used for the S/D contact metallization for Si and Ge MOSFETs, respectively. Self-alignment of the S/D contacts to the gate brings it adjacent to the gate, minimizing the distance between the channel and the metal contact and therefore R_S and R_D. Nickel germanide (NiGe) formed by the solid-state reaction between Ni and Ge has been widely investigated as a self-aligned S/D contact material for Ge MOSFETs due to its low sheet resistance R_{Sh} and low formation temperature (> 250 °C) [96]-[110]. Likewise, nickel stanogermanide [Ni(GeSn)] formed by the solid-phase reaction of Ni and $Ge_{1-x}Sn_x$ is thus a potential self-aligned S/D contact material for $Ge_{1-x}Sn_x$ MOSFETs [111]-[113].

However, the surface roughness of NiGe increases as the reaction temperature increases from 400 to 600 °C [99]. The agglomeration of NiGe occurs at ~500 °C and above [100]-[102]. Similarly, the thermal stability of Ni(GeSn) has to be improved as it is also susceptible to agglomeration during annealing. As shown in the top-view SEM images in Fig. 2.9, agglomeration occurs for 10 nm Ni/50 nm $Ge_{0.935}Sn_{0.065}$ annealed at a relatively low temperature of 450 °C [112]. This issue could worsen in aggressively scaled devices with ultrathin Ni(GeSn) contacts, according to the model of agglomeration in polycrystalline thin films [114]. Consequently, a contact metallization process for $Ge_{1-x}Sn_x$ with good thermal stability is needed, and is the focus of Chapter 4.

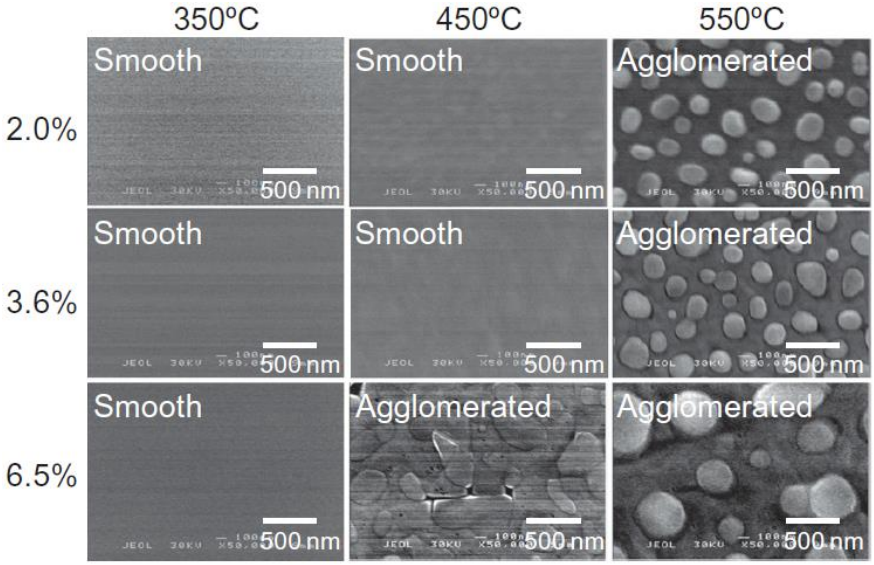


Fig. 2.9. SEM images of Ni/$Ge_{1-x}Sn_x$/Ge (100) samples with various Sn contents annealed at 350 °C, 450 °C, or 550 °C. A $Ge_{1-x}Sn_x$ layer with a thickness of 50 nm and a substitutional Sn composition of 2.0%, 3.6% or 6.5% was grown on the Ge (100) substrate. A 10 nm Ni layer was deposited, followed by RTA. Fig. 2.9 reprinted from Ref. [112], with permission from Elsevier, Copyright 2011.

b. Towards Highly Doped N-type $Ge_{1-x}Sn_x$

High doping concentration in the S/D region is needed to achieve low $R_{S/D}$ and thereby high I_{DSat} for $Ge_{1-x}Sn_x$ MOSFETs. The related study on $Ge_{1-x}Sn_x$ is lacking in the literature. Therefore, in Table 2.1, using Ge as the starting point, we benchmark the dopant activation in Ge using various doping methods including ion implant, *in situ* doping during the epitaxial growth, and gas phase doing, and activation methods including rapid thermal annealing (RTA) and laser annealing (LA) [115]-[122]. All the surface active concentration values are taken from the data in the references measured by the spreading resistance probe (SRP). P-type doping in Ge is of less an issue now, as ion implant has achieved an electrically active boron (B) concentration as high as 2×10^{20} cm^{-3} at the surface after RTA at 400 °C [118]. Likewise, activation of boron in $Ge_{1-x}Sn_x$ is not a problem [90].

Table 2.1. Research progress in doping in Ge. All the surface active concentration values are taken from the data measured by SRP.

	Doping Method	Activation Method	Temperature of Anneal or Growth (°C)	Surface Active Concentration (cm^{-3})
[115] Chui	Ion Implant	RTA	650	P: 2×10^{19}
			650	As: 8×10^{18}
			650	Sb: 8×10^{18}
[116] Chao	Ion Implant	RTA	400	B: 2×10^{20}
[117] Satta	Ion Implant	RTA	600	P: 2×10^{19}
[118] Chao	Ion Implant	RTA	600	P: 2×10^{19}
[119] Yu	*In situ* doping	N.A.	500	P: 1×10^{19}
[120] Morii	Gas phase	N.A.	600	As: 1×10^{19}
[121] Thareja	Ion Implant	LA	Unknown	Sb: 1×10^{20}

However, forming highly doped n-type Ge is more difficult as the dopants such as phosphorus (P), arsenic (As), and antimony (Sb) have low solubilities (e.g. 2×10^{20} cm^{-3} for P) [122] and high diffusion coefficients (e.g. 4.38×10^{-2} cm^2/s for P at temperatures ranging from 600 to 850 °C) [115]. As shown in Table 2.1, higher temperatures (> 500 °C) are needed for dopant activation of n-type dopants, as compared with p-type dopants. To obtain a relatively high concentration of active n-type dopants with a relatively shallow junction depth, there is a delicate balance between the diffusion of dopants and the high-temperature annealing requirement for dopant activation. Due to this balance, implant plus activation by RTA [115]-[118], *in situ* doping during epitaxy [119], or gas phase doping [120] can only obtain the highest active P concentration of ~2×10^{19} cm^{-3} at the surface.

Activation of n-type dopants should be more challenging and therefore its related research has higher impact. For design and fabrication of $Ge_{1-x}Sn_x$ n-MOSFETs, the investigation of n-type doping in $Ge_{1-x}Sn_x$ is imperative. The focus of Chapter 5 is n-type doping in $Ge_{1-x}Sn_x$.

2.3 Summary

In this Chapter, we review the current status of research on the technical challenges faced for $Ge_{1-x}Sn_x$ MOSFETs. First, the study on cost-effective integration of Ge on large Si is reviewed, which would provide an excellent solution for integrating $Ge_{1-x}Sn_x$ on Si. Second, it is critical to form high-quality gate stack for $Ge_{1-x}Sn_x$ MOSFETs. The surface passivation techniques using Si and $In_{1-a}Al_aP$ are discussed. Last, to minimize S/D parasitic resistance for obtaining high drive current of $Ge_{1-x}Sn_x$ MOSFETs, it is important to develop thermally stable self-aligned S/D contacts and to achieve high doping concentration for low resistance S/D regions.

Chapter 3

Germanium–Tin P-Channel Metal-Oxide Semiconductor Field-Effect Transistors with High Hole Mobility Realized by Ammonium Sulfide Passivation

3.1 Introduction

Germanium-tin ($Ge_{1-x}Sn_x$) has attracted great interest as an alternative channel material as it has higher carrier mobilities than germanium (Ge) and silicon (Si) [48],[61]-[64],[86]-[91],[123]-[131]. High-mobility $Ge_{1-x}Sn_x$ p-channel metal-oxide-semiconductor field-effect transistors (p-MOSFETs) with Si passivation have been demonstrated [61],[63],[86]-[91]. The effective mobility μ_{eff} of $Ge_{1-x}Sn_x$ p-MOSFETs with Si passivation is higher than that of the Ge control, owing to the Sn-induced chemical effect and the biaxial compressive strain in the $Ge_{1-x}Sn_x$ channel resulting from epitaxial growth of $Ge_{1-x}Sn_x$ film on Ge substrate [61].

High bulk carrier mobility of a semiconductor channel material may not necessarily lead to high μ_{eff} and therefore high drive current I_{Dsat}, if the quality of the interface between the gate dielectric and channel is poor. As discussed in Chapter 2, surface passivation of the $Ge_{1-x}Sn_x$ channel surface and development of

a thermodynamically stable high-quality gate stack are critical for realizing high-performance $Ge_{1-x}Sn_x$ MOSFETs.

Sulfur (S) passivation on Ge substrate can be achieved by means of treatment with ammonium sulfide [$(NH_4)_2S$] aqueous solution [65],[132]-[138], or by reactions in the gas phase using hydrogen sulfide (H_2S) [139]-[142] or elemental S [143]-[144]. After $(NH_4)_2S$ treatment, a thin GeS_x layer is formed, producing a passivated Ge surface that is almost free of Ge native oxides and thus has low D_{it} [65],[134]-[136]. Likewise, it is worthwhile to study the impact of $(NH_4)_2S$ surface passivation on the electrical characteristics of $Ge_{1-x}Sn_x$ MOSFETs.

In this Chapter, we investigate $Ge_{0.958}Sn_{0.042}$ p-MOSFETs with $(NH_4)_2S$ passivation for the first time. We report the results of the material characterization, including transmission electron microscopy (TEM), atomic force microscopy (AFM), X-ray diffraction (XRD), secondary ion mass spectroscopy (SIMS) and X-ray photoelectron spectroscopy (XPS). We also study the impact of $(NH_4)_2S$ passivation on the electrical characteristics of $Ge_{0.958}Sn_{0.042}$ p-MOSFETs. By performing $(NH_4)_2S$ passivation, a peak μ_{eff} of 509 $cm^2/V{\cdot}s$ was demonstrated. Part of this work was published in Refs. [130] and [131].

3.2 Experimental Details

3.2.1 Growth and Characterization of $Ge_{0.958}Sn_{0.042}$

$Ge_{1-x}Sn_x$ films in this work were grown on 4-inch arsenic-doped Ge (100) substrates at 180 °C by a solid source molecular beam epitaxy (MBE) system [56]. *Ex situ* pre-epitaxy cleaning was performed using dilute hydrofluoric acid (DHF) ($HF:H_2O$ = 1:10), followed by a pre-epitaxy baking at 650 °C for 30 minutes for native oxide removal. *In situ* reflection high-energy electron diffraction (RHEED) patterns reveal well-developed 2 × 1 reconstruction, indicating that the sample surface is free of native oxide. The base pressure in the growth chamber is 3×10^{-8} Pa. The $Ge_{1-x}Sn_x$ alloy was then grown by evaporating 99.9999% pure Ge and 99.9999% pure Sn from the effusion cells. The deposition rate of Ge or Sn can be adjusted by tuning the temperature of effusion cell. The Ge deposition rate was maintained at ~0.022 nm/s, while the Sn deposition rate was set to obtain the desired Sn composition (~4% in this work). The epitaxial $Ge_{1-x}Sn_x$ films are p-type with an unintentional doping concentration of 5×10^{16} cm^{-3} as obtained by Hall measurement, due to the presence of vacancies in the epitaxial films [145]-[147]. The above-mentioned MBE growth was done by our collaborators (Prof. Buwen Cheng's group) at the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China.

To calculate the substitutional Sn composition, high-resolution XRD (HRXRD) was performed. To obtain good XRD signal from the epitaxial film, a relative thick $Ge_{1-x}Sn_x$ film was used for material characterization. Cross-sectional TEM (XTEM) image in Fig. 3.1(a) shows ~140-nm-thick $Ge_{1-x}Sn_x$ film grown on Ge (100) substrate. The $Ge_{1-x}Sn_x$/Ge interface can be observed clearly.

High-resolution TEM (HRTEM) image in Fig. 3.1 (b) shows the single-crystalline $Ge_{1-x}Sn_x$ film without any observable defect near the $Ge_{1-x}Sn_x$/Ge interface.

The HRXRD (004) curve in Fig. 3.2 shows the well-defined peaks of $Ge_{1-x}Sn_x$ epitaxial layer and Ge (100) substrate. Based on previous studies from our group [61],[63],[86]-[91], the $Ge_{1-x}Sn_x$ thin film is fully-strained to the Ge (100) substrate. This should be the case for all the $Ge_{1-x}Sn_x$ ($x < 0.07$) films grown on Ge substrates by the MBE system used. Assuming tetragonal distortion of the $Ge_{1-x}Sn_x$ layer grown on Ge (100) substrate, the lattice constant of unstrained $Ge_{1-x}Sn_x$ is calculated to be 0.569255 nm using the HRXRD (004) curve. Taking the lattice constants of Ge and Sn to be 0.565754 nm and 0.649120 nm, respectively [148], the substitutional Sn composition is obtained to be 4.2% by applying Vegard's law. In addition, the AFM image in Fig. 3.3 shows the smooth $Ge_{0.958}Sn_{0.042}$ surface with a root-mean-square (RMS) roughness of 0.26 nm within a scanning area of 10 μm × 10 μm.

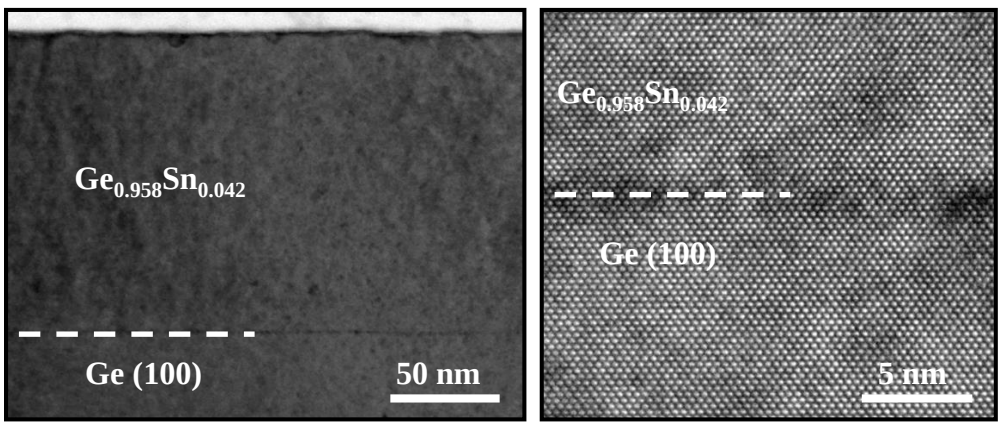


Fig. 3.1. (a) XTEM image of ~ 140-nm-thick epitaxial $Ge_{0.958}Sn_{0.042}$ film grown on Ge (100) substrate. (b) HRTEM image showing the periodic arrangement of atoms across the defect-free interface between $Ge_{0.958}Sn_{0.042}$ and Ge. The TEM was performed as an external service job at the Institute of Materials Research and Engineering (IMRE).

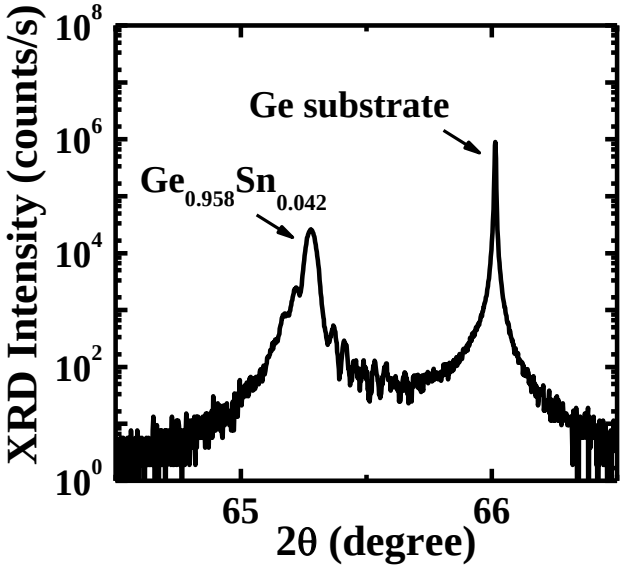


Fig. 3.2. HRXRD (004) curve showing the well-defined peaks of the $Ge_{1-x}Sn_x$ epitaxial film and Ge substrate. The substitutional Sn composition of the $Ge_{1-x}Sn_x$ film is ~4.2%. The HRXRD was performed as an external service job at IMRE.

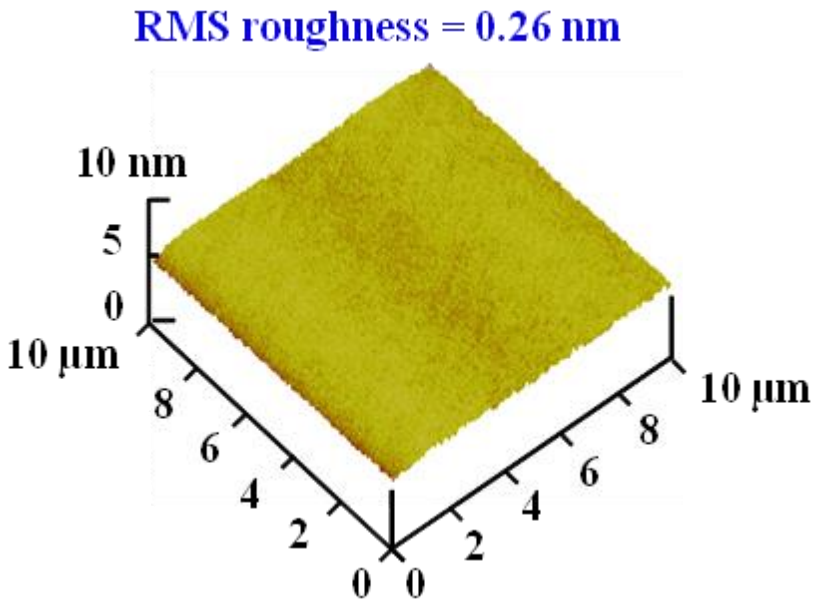


Fig. 3.3. AFM image of a smooth $Ge_{0.958}Sn_{0.042}$ film surface showing a RMS roughness of 0.26 nm within a scanning area of 10 µm × 10 µm.

3.2.2 Design Concept

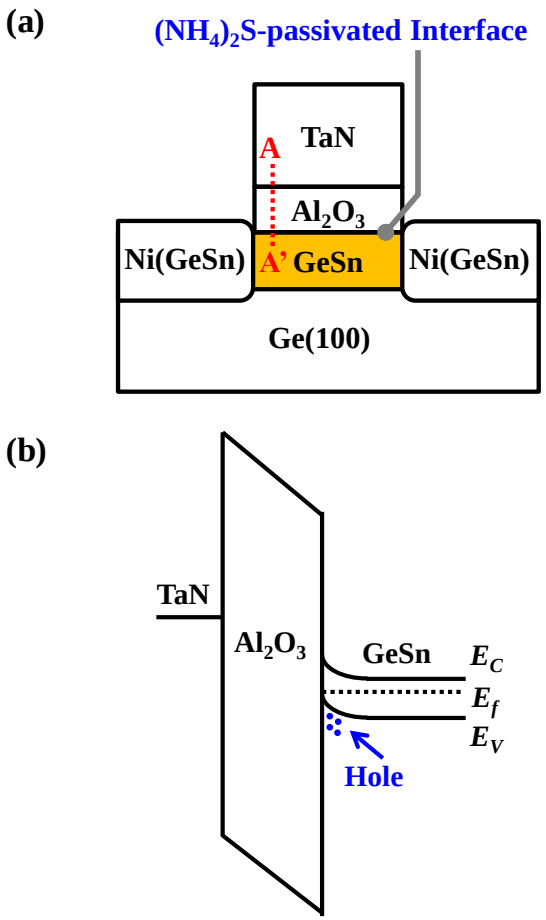


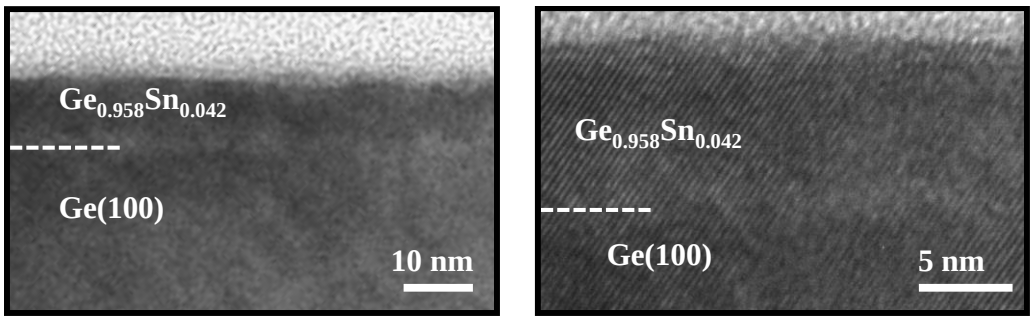
Fig. 3.4. (a) The schematic of a $Ge_{0.958}Sn_{0.042}$ p-MOSFET with $(NH_4)_2S$-passivated interface to prevent the native oxide formation before high-*k* deposition. (b) The energy band diagram across line A-A' of the $(NH_4)_2S$-passivated $Ge_{0.958}Sn_{0.042}$ transistor operating in the strong inversion regime. We assume there is no native oxide layer formed on the $(NH_4)_2S$-passivated $Ge_{0.958}Sn_{0.042}$ channel surface. E_C, E_V and E_f in the energy band diagram are the conduction band edge, valence band edge, and Fermi level, respectively.

To illustrate the concept of applying the surface passivation technique on the $Ge_{0.958}Sn_{0.042}$ channel surface, the schematic of a $Ge_{0.958}Sn_{0.042}$ p-MOSFET using $(NH_4)_2S$ passivation is shown in Fig. 3.4(a). Considering the Sn-induced chemical effect and compressive strain in $Ge_{0.958}Sn_{0.042}$ grown on Ge substrate [48],[149], the band gap was estimated to be ~70 meV smaller than that of Ge. Fig. 3.4(b) depicts the energy band diagram of the $(NH_4)_2S$-passivated $Ge_{0.958}Sn_{0.042}$ p-MOSFET across line A-A' operating in strong inversion regime,

based on the reported analysis of internal photoemission and photoconductivity [150]. S was used to passivate the dangling bonds at the $Ge_{0.958}Sn_{0.042}$ channel surface and to prevent the native oxide formation before Al_2O_3 deposition.

3.2.3 Transistor Fabrication

Figs. 3.5(a) and (b) show XTEM and HRTEM images of ~10-nm-thick $Ge_{0.958}Sn_{0.042}$ film grown on n-type Ge (100) substrate for transistor fabrication, respectively. A high-quality single-crystalline $Ge_{0.958}Sn_{0.042}$ film without observable defects at the surface and near the $Ge_{0.958}Sn_{0.042}$/Ge interface was detected. Obtaining a smooth surface is an essential prerequisite for achieving high-quality gate stack with low D_{it} between the high-k dielectric and channel. In addition, an excellent $Ge_{0.958}Sn_{0.042}$/Ge interface would not contribute to leakage current associated with defects beneath the channel and should be preferable for transistor fabrication.



(a) **(b)**

Fig. 3.5. (a) XTEM image of ~10-nm-thick epitaxial $Ge_{0.958}Sn_{0.042}$ film grown on Ge (100) substrate. (b) HRTEM image showing a high-quality single-crystalline $Ge_{0.958}Sn_{0.042}$ film without observable defects at the surface and near the $Ge_{0.958}Sn_{0.042}$/Ge interface. The TEM was done by Dr. Yue Yang in our group.

Fig. 3.6(a) illustrates the key process steps for fabricating $Ge_{0.958}Sn_{0.042}$ p-MOSFETs, highlighting the step of $(NH_4)_2S$ passivation. After $Ge_{0.958}Sn_{0.042}$ growth by MBE, phosphorus well implantation was performed on blanket $Ge_{0.958}Sn_{0.042}$ samples with a dose of 5×10^{12} cm^{-2} and implant energy of 20 keV. The implant was performed as an external service job at the INNOViON Corporation, San Jose, California, USA. A rapid thermal annealing (RTA) process at 450 °C for 3 minutes in a nitrogen gas (N_2) ambient was used for dopant activation. A cyclic pre-gate cleaning process was used for cleansing the $Ge_{0.958}Sn_{0.042}$ surface. It involves 5 cycles' treatment of the samples, with deionized water for 30 s followed by DHF ($HF:H_2O$ = 1:50) for 30 s in each cycle. After that, $(NH_4)_2S$ passivation was done by treatment with $(NH_4)_2S$ aqueous solution (36%) for 10 minutes at 25 °C.

All samples were then quickly loaded into an atomic layer deposition (ALD) system for growing ~6 nm of Al_2O_3 gate dielectric at 250 °C using trimethylaluminium (TMA) and H_2O as precursors, and N_2 as carrier gas. This was followed by reactive sputter deposition of 100 nm of tantalum nitride (TaN) as gate electrode and 10 nm of silicon dioxide (SiO_2) as hard mask. Gate lithography was performed by a mask aligner and TaN was patterned using a chlorine based plasma etching process. 50 nm of SiO_2 was then deposited by sputter and patterned to expose the active region. Self-aligned nickel stanogermanide [Ni(GeSn)] metallic source/drain (S/D) were formed by depositing 10 nm of Ni, followed by the solid-state reaction by a RTA process at 350 °C for 30 s in N_2 ambient. Selective removal of the unreacted Ni film using concentrated sulfuric acid (H_2SO_4) solution (96%) completes the device fabrication. Fig. 3.6(b) shows a top-view scanning electron microscopy (SEM)

image of the fabricated transistor. Except the ALD growth that was done by Dr. Xiao Gong in our group, the rest of the process steps were done jointly by Dr. Genquan Han in our group and the author.

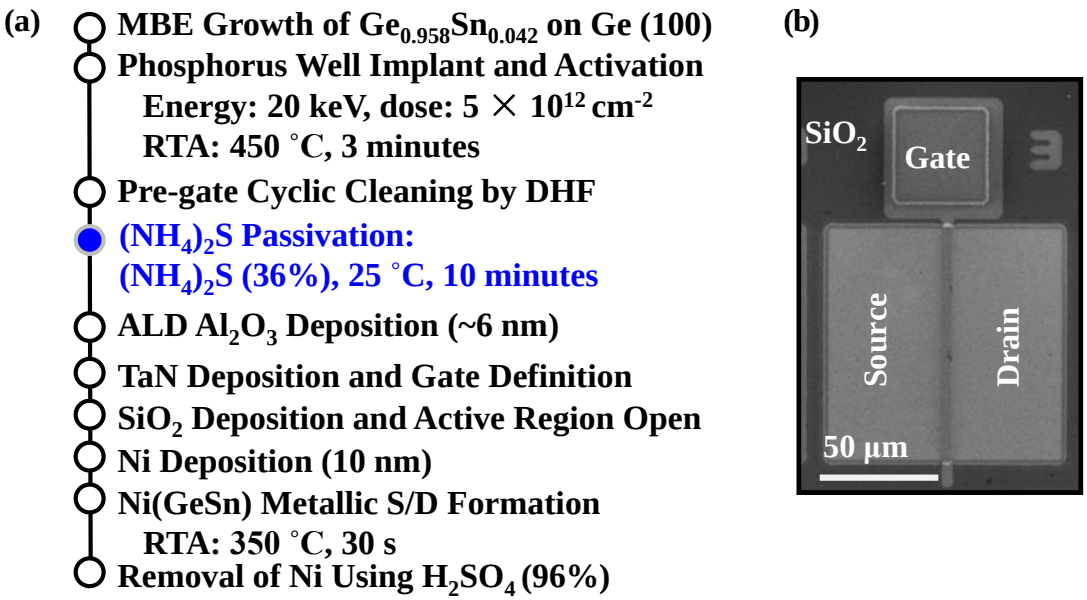


Fig. 3.6. (a) The process flow for fabricating $Ge_{0.958}Sn_{0.042}$ p-MOSFETs. Prior to deposition of Al_2O_3 by ALD, $(NH_4)_2S$ passivation was done by treatment with $(NH_4)_2S$ aqueous solution (36%) for 10 minutes at 25 °C. (b) A top-view SEM image of a fabricated p-MOSFET.

3.3 Result and Discussion

3.3.1 Electrical Characterization of $Ge_{1-x}Sn_x$ p-MOSFETs

Fig. 3.7 shows the inversion capacitance C – voltage V characteristics of a $Ge_{0.958}Sn_{0.042}$ p-MOSFET with $(NH_4)_2S$ passivation working from the depletion region to strong inversion region (where capacitance was measured between the gate and source/drain terminals). The gate length L_G and gate width W of the measured p-MOSFET are 15 and 100 μm, respectively. The frequency f of the measurement is 10, 30, 50, 80 or 100 kHz. Strong frequency dispersion is observed when the f varies from 10 to 100 kHz. This indicates that a large amount of interface trap charges are present in the $TaN/Al_2O_3/(NH_4)_2S$-passivated $Ge_{0.958}Sn_{0.042}$ stack [151]-[152].

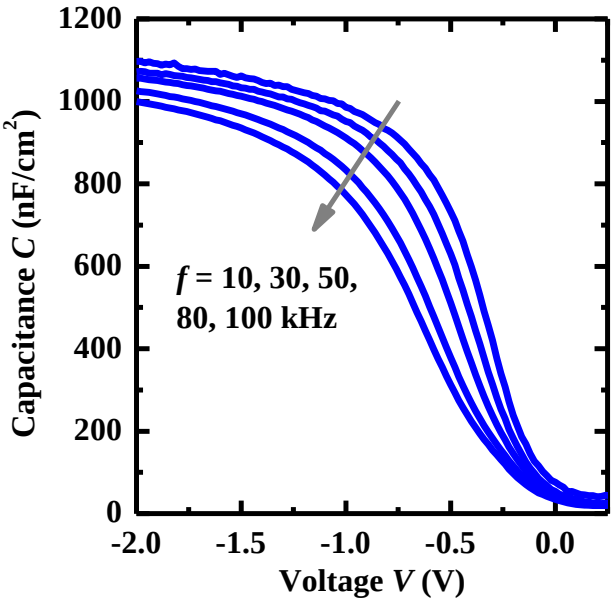


Fig. 3.7. Inversion C – V curve of $Ge_{0.958}Sn_{0.042}$ p-MOSFET with $(NH_4)_2S$ passivation. The capacitance was measured between the gate and source/drain terminals. The frequency of the measurement is 10, 30, 50, 80 or 100 kHz. Strong frequency dispersion indicates the existence of trap charges in the gate stack.

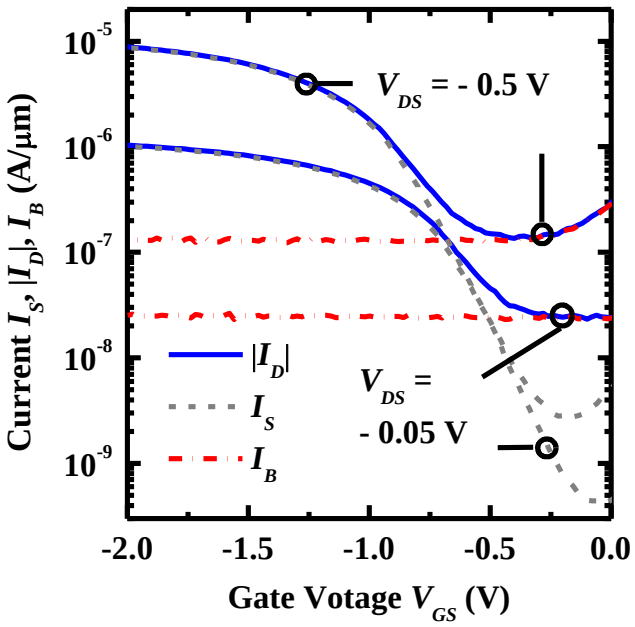


Fig. 3.8. $|I_D| - V_{GS}$, $I_S - V_{GS}$, and $I_B - V_{GS}$ curves of a $Ge_{0.958}Sn_{0.042}$ p-MOSFET with $(NH_4)_2S$ passivation in the linear (V_{DS} = - 0.05 V) and saturation (V_{DS} = - 0.5 V) regions. The transistor has high I_B, resulting in the leakage floor of $|I_D|$ is more than 1 order of magnitude higher than that of I_S in the subthreshold region.

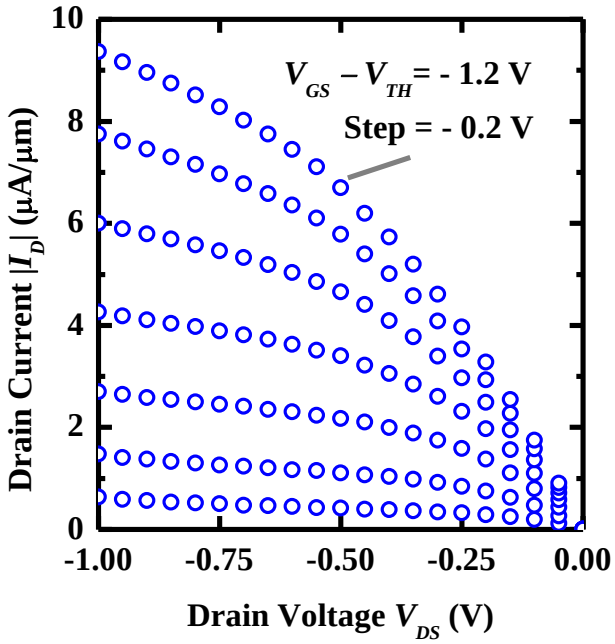


Fig. 3.9. $|I_D| - V_{DS}$ output characteristics of the same device at various gate overdrive voltages.

Fig. 3.8 plots the drain current $|I_D|$ – gate-to-source voltage V_{GS}, source current I_S – V_{GS} and body current I_B – V_{GS} curves in the linear (drain-to-source voltage V_{DS} = – 0.05 V) and saturation (V_{DS} = – 0.5 V) regions of a typical $Ge_{0.958}Sn_{0.042}$ p-MOSFET with $(NH_4)_2S$ passivation. Both the source and body terminals are connected to ground. L_G and W of the transistor are 5.5 μm and 100 μm, respectively. The transistor has high I_B, which is the drain-to-body junction reverse leakage current, resulting in the leakage current floor of $|I_D|$ is more than 1 order of magnitude higher than that of I_S in the subthreshold region.

It should be noted that the Ni(GeSn) metallic S/D structure was utilized for process simplicity. Compared with Si p/n junction diodes, typical metal/Si Schottky diodes have 10^3 to 10^8 larger reverse saturation currents, which are determined by thermionic emission of majority carriers over the Schottky barrier [5]. Si p-MOSFETs with metal silicide S/D have exhibited high leakage currents due to the reverse leakage current of the Schottky drain-to-body junctions [153]-[154]. For indium gallium arsenide ($In_{1-b}Ga_bAs$) channel n-MOSFETs with self-aligned Ni-InGaAs metallic S/D, X. Zhang *et al.* have demonstrated that the drain-to-body (Ni-InGaAs/p-$In_{1-b}Ga_bAs$) junction also suffers from high reverse leakage current, and forming an n^+-$In_{1-b}Ga_bAs$/p-$In_{1-b}Ga_bAs$ junction helps to suppress the junction leakage current significantly [155]. Likewise, the drain-to-body [(Ni(GeSn)/n-$Ge_{1-x}Sn_x$] junction reverse leakage current could be reduced by forming an p^+-$Ge_{1-x}Sn_x$/n-$Ge_{1-x}Sn_x$ junction with optimized conditions of p-type dopant implantation and activation.

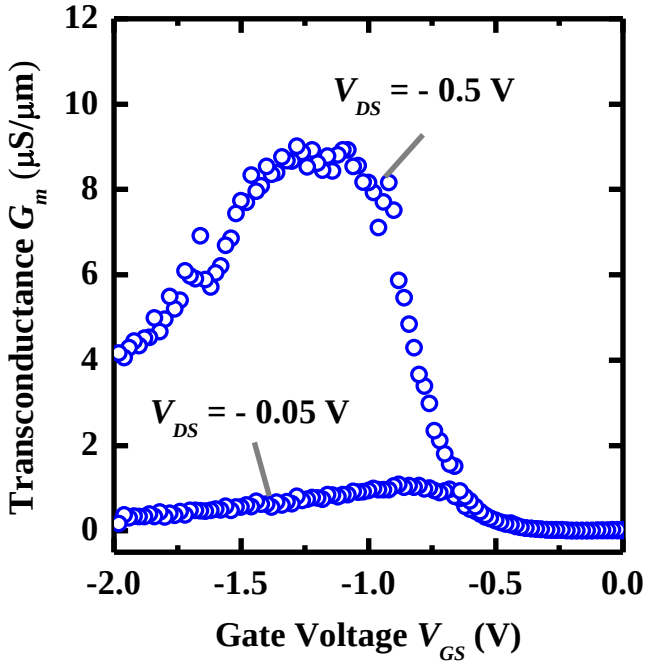


Fig. 3.10. G_m – V_{GS} characteristics of the same device in Fig. 3.8 at V_{DS} of – 0.05 V and – 0.5 V.

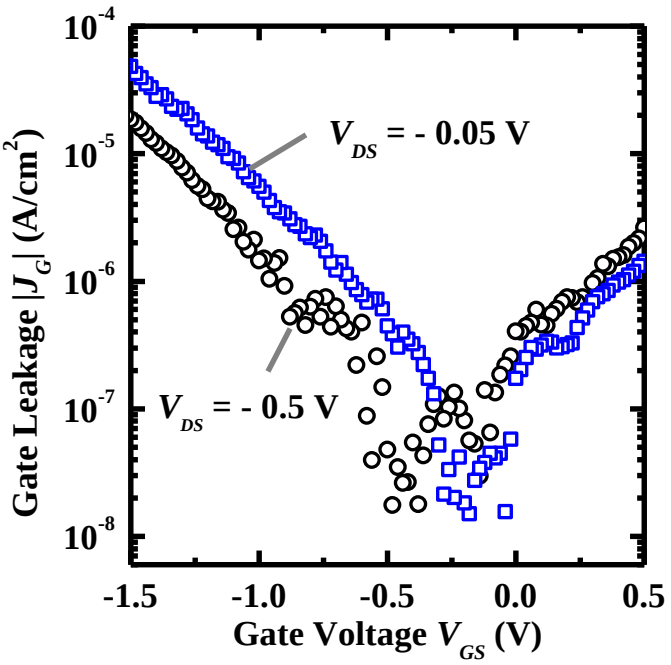


Fig. 3.11. $|J_G|$ – V_{GS} characteristics of the same device in Fig. 3.8 at V_{DS} of – 0.05 V and – 0.5 V. The measured $|J_G|$ was normalized by gate area with V_{GS} between – 1.5 V and 0.5 V. The $|J_G|$ of less than 10^{-5} A/cm^2 at a gate bias voltage of V_{TH} – 1 V was achieved, indicating the potential for further scaling of the dielectric layer.

Fig. 3.9 shows the $|I_D| - V_{DS}$ output characteristics of the same device. V_{GS} is varied from gate overdrive voltage $V_{GS} - V_{TH}$ of 0 to – 1.2 V in step of – 0.2 V. A key design parameter, the transconductance G_m, is the incremental change in I_D resulting from an incremental change in V_{GS} at a given V_{DS}. Fig. 3.10 shows the $G_m - V_{GS}$ characteristics at V_{DS} in the linear and saturation regions of the same device. Fig. 3.11 shows the gate leakage current density $|J_G| - V_{GS}$ characteristics of the same device at V_{DS} of – 0.05 V and – 0.5 V. The measured gate leakage current density was normalized by gate area with V_{GS} between – 1.5 V and 0.5 V. The gate leakage current density of less than 10^{-5} A/cm^2 at a gate bias voltage of $V_{TH} - 1$ V was achieved. This indicates the potential for further scaling of the dielectric layer.

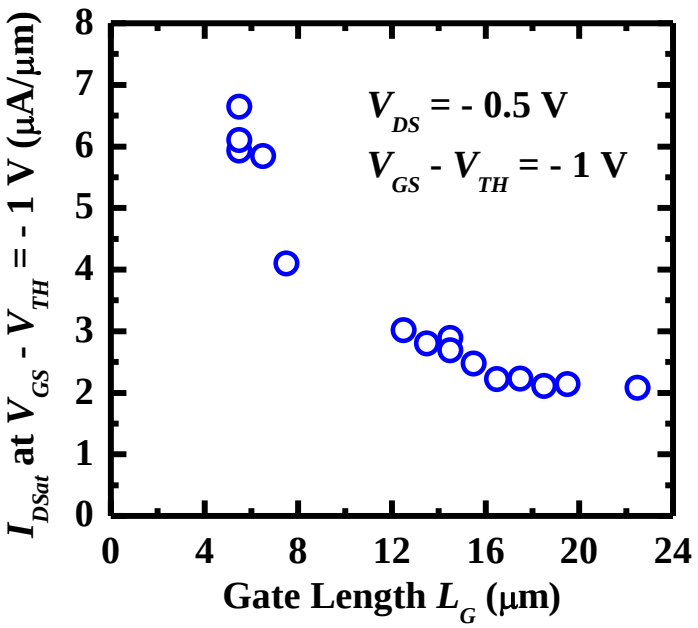


Fig. 3.12. I_{DSat} (measured at $V_{GS} - V_{TH}$ of – 1 V) versus L_G for $Ge_{0.958}Sn_{0.042}$ p-MOSFETs with $(NH_4)_2S$ passivation.

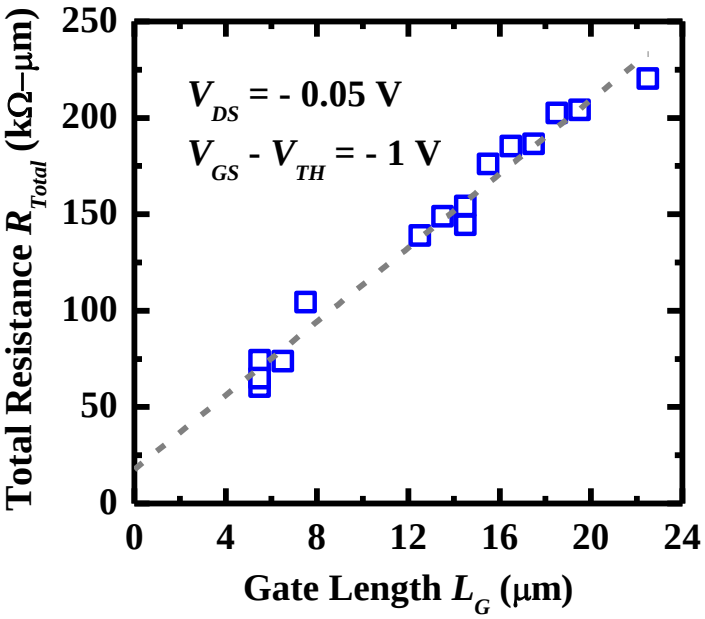


Fig. 3.13. R_{total} (between the source and drain terminals) versus L_G for $Ge_{0.958}Sn_{0.042}$ p-MOSFETs at V_{DS} = – 0.05 V and $V_{GS} – V_{TH}$ = – 1 V. The high S/D resistance significantly limits the drive current of the transistors. Experimental data points are plotted using symbols. Linearly fitted line is drawn using dashed line. The intercept of the linearly fitted line with the vertical axis yields $R_{S/D}$ (~18 kΩ-μm).

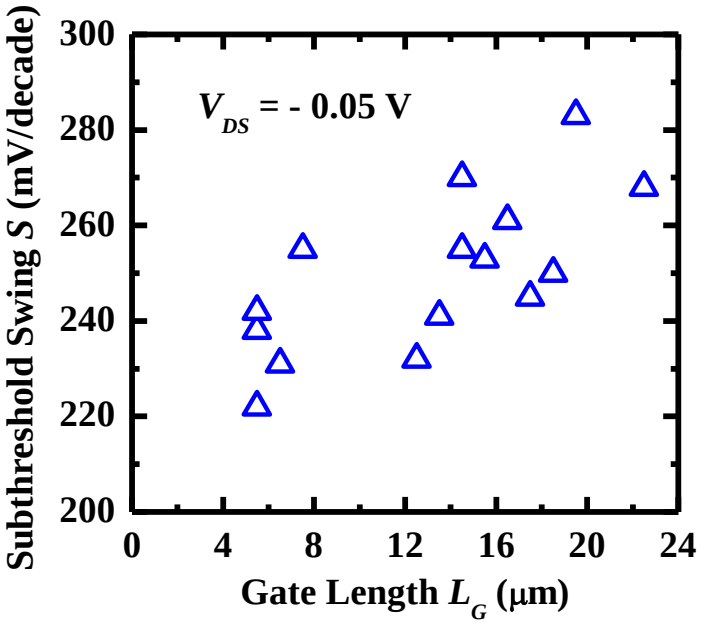


Fig. 3.14. S versus L_G for $Ge_{0.958}Sn_{0.042}$ p-MOSFETs at V_{DS} = – 0.05 V. The high subthreshold swing values in this work indicate that the density of interfacial state traps around mid-gap should be high.

Fig. 3.12 plots I_{DSat} (measured at $V_{GS} - V_{TH}$ of – 1 V and V_{DS} of – 0.5 V) versus L_G for $Ge_{0.958}Sn_{0.042}$ p-MOSFETs with $(NH_4)_2S$ passivation. It is noted that the transistors have relatively low drive currents in this work, which are severely affected by the high S/D series resistance $R_{S/D}$. $R_{S/D}$ is the sum of the source resistance R_S and drain resistance R_D, where R_S equals R_D because of device symmetry. Fig. 3.13 plots the total resistance R_{Total} between the source and drain terminals versus L_G for $Ge_{0.958}Sn_{0.042}$ p-MOSFETs at V_{DS} = – 0.05 V and $V_{GS} - V_{TH}$ = – 1 V. Measured data points are plotted as symbols. Linearly fitted line is drawn using dashed line. The intercept of the linearly fitted line with the vertical axis yields $R_{S/D}$ (~18 kΩ-μm), which is quite high as compared with that of other p-MOSFETs with self-aligned Ni(GeSn) metallic S/D in our group [88]. The high $R_{S/D}$ may result from the over etch of Ni(GeSn), when etching the unreacted Ni using concentrated H_2SO_4 solution. For selective etching of Ni with respect to NiGe, it is reported that the selectivity, which is the ratio of the etch rate of the target material being etched (6 nm/minute for Ni) to the etch rate of other material (1.7 nm/minute for NiGe), is low [156].

Subthreshold swing S is the number of millivolts required to increase V_{GS} to produce a factor of 10 increase in the decimal logarithm of I_S in the subthreshold region, which is an important device performance metric in evaluation of the gate stack interface quality. Fig. 3.14 plots S versus L_G for $Ge_{0.958}Sn_{0.042}$ p-MOSFETs at V_{DS} = – 0.05 V. The relatively high subthreshold swing values in this work indicate that the density of interfacial state traps around mid-gap should be high.

Fig. 3.15 shows the extracted μ_{eff} versus inversion carrier density N_{inv}. The effective mobility was extracted using a total resistance slope-based approach [157]

$$\mu_{eff} = \frac{1}{WqN_{inv}\dfrac{\Delta R_{total}}{\Delta L_G}}, \tag{3.1}$$

where ΔL_G and ΔR_{total} are the gate length difference of the two measured $Ge_{0.958}Sn_{0.042}$ p-MOSFETs used for mobility extraction and their difference in the total resistance extracted by I_S – V_{GS} characteristics in the linear region, respectively. N_{inv} is obtained by integrating the inversion C – V curve measured at f of 100 kHz as shown in Fig. 3.7. The $(NH_4)_2S$-passivated devices exhibit higher effective mobility than the universal Si hole mobility [158] in the entire inversion carrier density range.

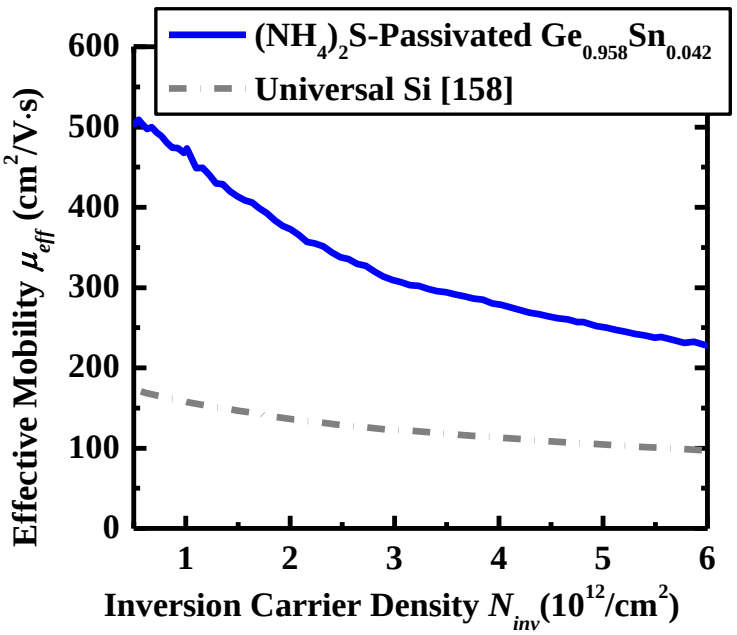


Fig. 3.15. μ_{eff} versus N_{inv} of $Ge_{0.958}Sn_{0.042}$ p-MOSFETs with $(NH_4)_2S$ passivation. $(NH_4)_2S$-passivated devices were observed to have higher hole mobility than the universal Si hole mobility in the entire N_{inv} range.

3.3.2 Physical Characterization of S-passivated $Ge_{1-x}Sn_x$ Surface

In this work, S was used to passivate the dangling bonds at the $Ge_{1-x}Sn_x$ channel surface during the passivation as illustrated in the schematic shown in Fig. 3.16(a). This helps to prevent the native oxide formation on the sample surface, before loading them into the ALD chamber for Al_2O_3 deposition.

SIMS was carried out to examine S distribution in the blanket S-passivated sample with a 2-nm Al_2O_3 capping layer. The S passivation layer is preserved after the deposition of high-*k* dielectric [Fig. 3.16(b)]. Apart from being an oxide-preventing layer, this interfacial layer may act as a barrier between the high-*k* dielectric and $Ge_{1-x}Sn_x$ channel to help to prevent interactions and inter-diffusion. Similar result was also observed for $(NH_4)_2S$-passivated Ge in Ref. [134].

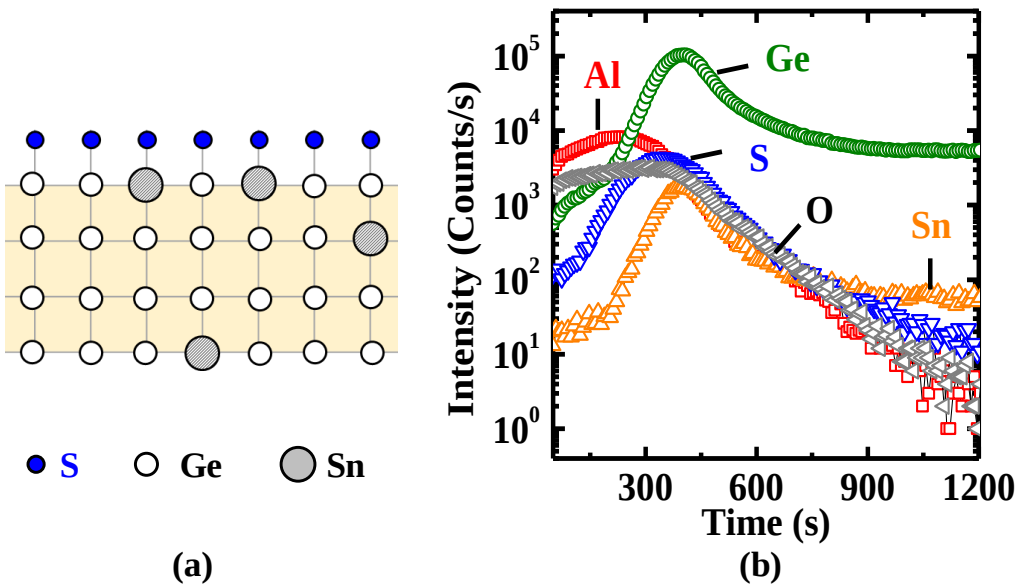


Fig. 3.16. (a) Schematic of S-passivated $Ge_{1-x}Sn_x$ surface. S is used to passivate the dangling bonds at the channel surface and prevent oxide formation before Al_2O_3 deposition. (b) SIMS profiles of S-passivated $Ge_{1-x}Sn_x$ surface with Al_2O_3 capping. SIMS was performed as an external service job at the Institute of Materials Research and Engineering.

To investigate the effect of $(NH_4)_2S$ passivation on the interfacial chemical bonding between the high-k gate dielectric and $Ge_{1-x}Sn_x$, samples with Al_2O_3 formed on $Ge_{1-x}Sn_x$ surfaces with and without $(NH_4)_2S$ passivation were prepared for XPS analysis. The measurement was performed using a VG ESCALAB 220i-XL imaging XPS, which was performed by Dr. Zheng Zhang in the Institute of Materials Research Engineering. Monochromatic aluminium (Al) Kα x-ray (1486.6 eV) was employed for analysis with photoelectron take-off angle of 90° with respect to the surface plane.

Fig. 3.17(a) and (b) show the Ge $2p_{3/2}$ and Sn $3d_{5/2}$ core level spectra, respectively, of $Ge_{0.958}Sn_{0.042}$ samples with or without $(NH_4)_2S$ passivation. Ge-O, Ge-Ge, Sn-Sn bonds were observed for the samples with or without $(NH_4)_2S$ passivation. Ge-O peak is reduced as compared with that for the non-passivated surface, indicating that $(NH_4)_2S$ passivation helps to supress the formation of Ge-O. However, Ge-O bond cannot be fully eliminated, implying that the surface is not fully covered by S. A recent study of the $(NH_4)_2S$-passivated Ge surface reveals that the Ge surface is not fully covered by S after the treatment, and the residual Ge oxides were detected regardless of the passivation time [137]. The presence of these residual oxides should not be desired in the gate stack, as it results in the high density of interface traps of the $Ge_{0.958}Sn_{0.042}$ p-MOSFETs. The large amount of interface traps can explain strong frequency dispersion in inversion $C-V$ curves (Fig.7) and large subthreshold swing values (Fig. 14).

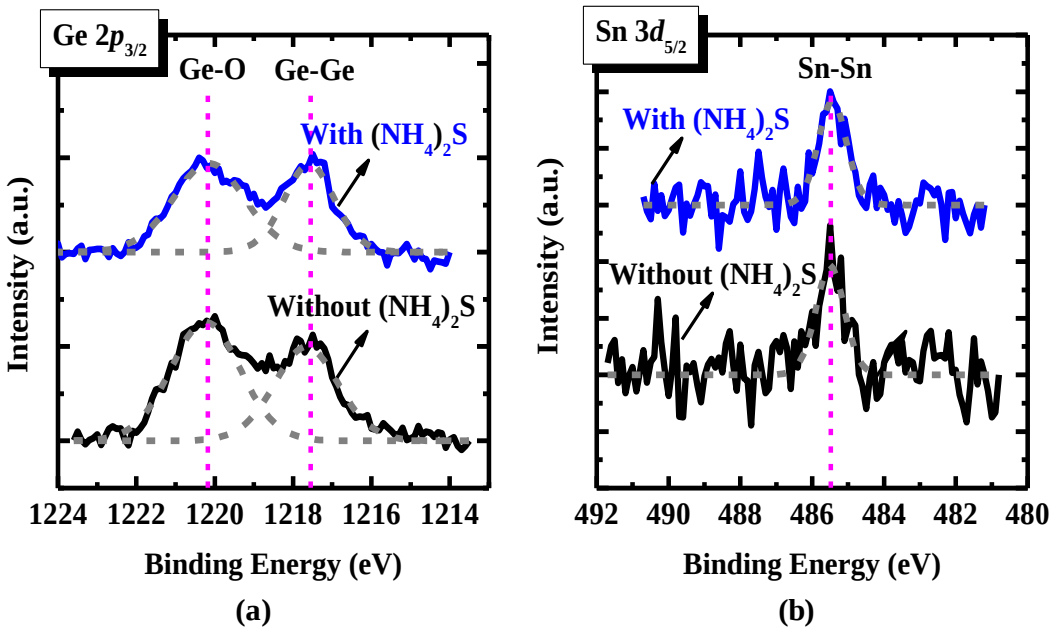


Fig. 3.17. (a) Ge $2p_{3/2}$ and (b) Sn $3d_{5/2}$ spectra of $Ge_{1-x}Sn_x$ samples with or without $(NH_4)_2S$ passivation.

3.3.3 Discussion

Quasi-ballistic transport dominates the drive currents of the transistors, as devices are scaled into deep sub-100 nm regime. In the quasi-ballistic regime, I_{Dsat} of a MOSFET is limited by the thermal injection velocity v_{inj} and is given by [18]-[19]

$$I_{Dsat} = C_{ox} W v_{inj} \left(\frac{1-r_c}{1+r_c} \right) (V_{GS} - V_{TH}), \tag{3.2}$$

where C_{ox} is the gate oxide capacitance and r_c is the backscattering coefficient. The thermal injection velocity was experimentally found to be proportional to the low field mobility [20]-[21]. Therefore, Fig. 3.18 benchmarks the extracted low-field carrier mobility, i.e. peak μ_{eff}, of the $Ge_{1-x}Sn_x$ p-MOSFETs with $(NH_4)_2S$ passivation in this work with the reported (100)-oriented $Ge_{1-x}Sn_x$ channel p-

MOSFETs so far in Refs. [61]-[63], [91], and [159]. It should be noted that the peak μ_{eff} value was obtained from the devices without post metal annealing (PMA) in Ref. [91]. Although PMA was demonstrated to increase peak mobility, we only focus on the impact of pre-gate passivation/cleaning techniques. $(NH_4)_2S$-passivated p-MOSFETs demonstrate the highest peak μ_{eff} among them, which indicates the potential to provide the highest v_{inj}.

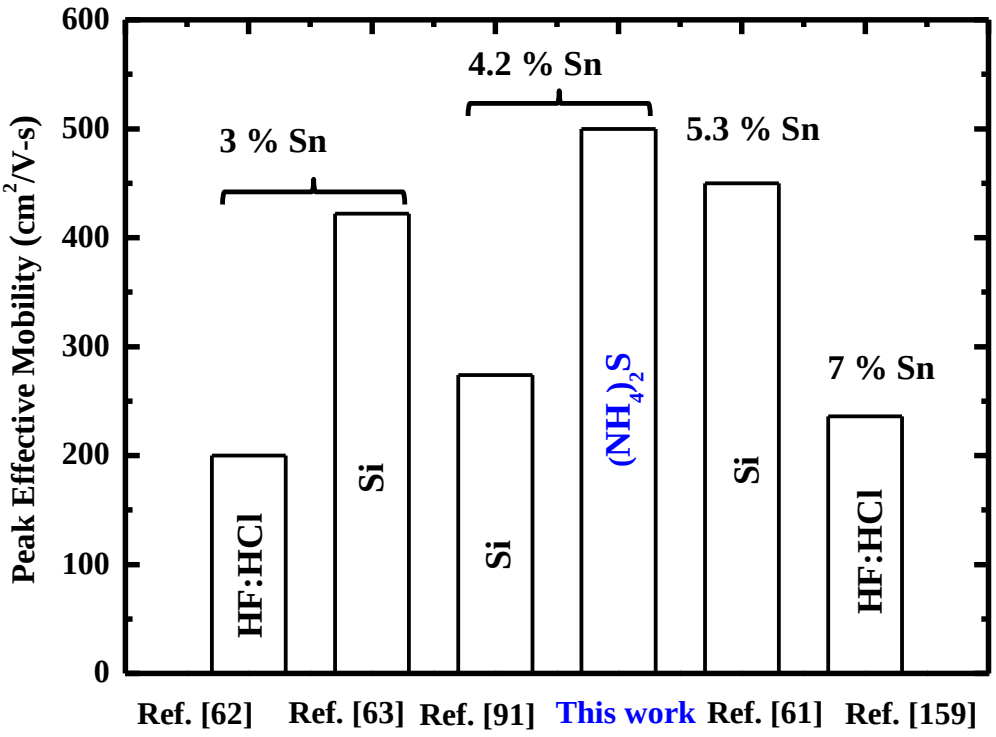


Fig. 3.18. Benchmarking of peak μ_{eff} of the (100)-oriented $Ge_{1-x}Sn_x$ p-MOSFETs achieved by different pre-gate passivation/cleaning techniques. $(NH_4)_2S$ passivation gives the highest peak mobility in low inversion carrier density region.

Since the devices we benchmarked here are long-channel transistors, the effective carrier mobility in high inversion carrier density region is still an important parameter, reflecting the carrier transport and scattering. Fig. 3.19 compares the effect of different pre-gate passivation/cleaning techniques on μ_{eff} extracted at N_{inv} of 5×10^{12} cm^{-2} of $Ge_{1-x}Sn_x$ p-MOSFETs in Refs. [61]-[63], [91], and [159]. The effective mobility of the $(NH_4)_2S$-passivated transistor degrades substantially with increasing inversion carrier density, leading to lower mobility in the high inversion carrier density region as compared with those with Si passivation reported in Refs. [61], [63], and [91]. The mobility degradation should be attributed to the combined effect of Coulomb scattering and inversion carrier loss due to interface traps located at the $Al_2O_3/Ge_{1-x}Sn_x$ interface.

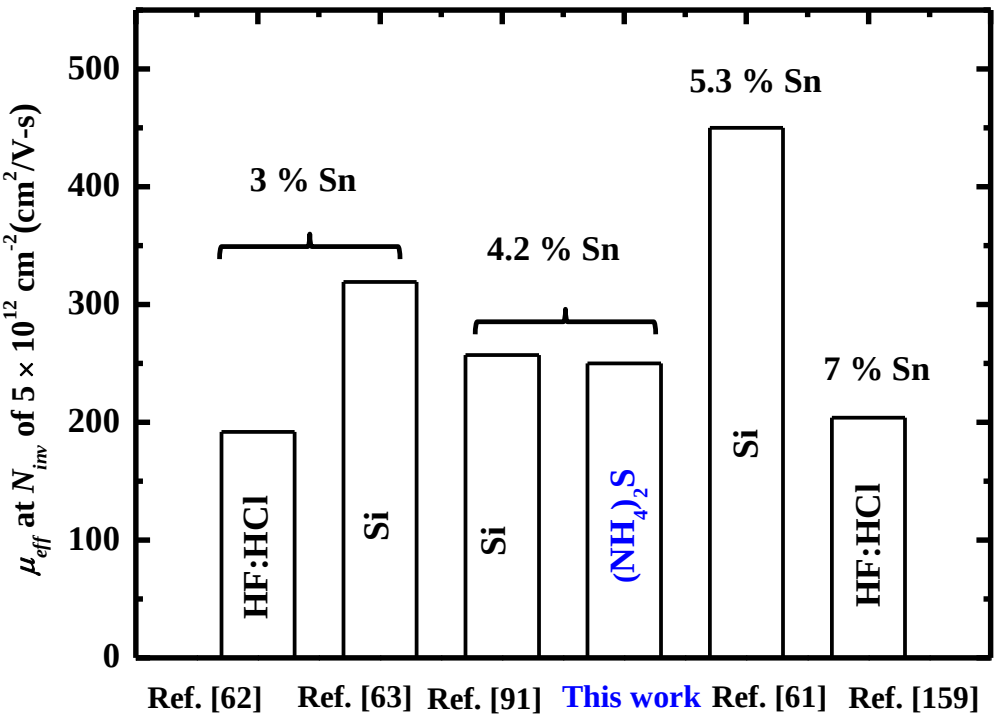


Fig. 3.19. Benchmarking of μ_{eff} extracted at N_{inv} of 5×10^{12} cm^{-2} of the (100)-oriented $Ge_{1-x}Sn_x$ p-MOSFETs achieved by different pre-gate passivation/cleaning techniques. μ_{eff} of $(NH_4)_2S$-passivated transistor drops substantially as N_{inv} increases.

The existence of interface traps in the gate stack should be attributed from the non-effective S passivation on the channel surface. The consequences of the presence of interface traps near the valence band edge of $Ge_{1-x}Sn_x$ can be explained by the energy band diagrams and the positions of Fermi level and the charge neutrality level E_{CNL}. The charge neutrality level of surface states is the position for the Fermi level that renders the surface without a net charge, where is shown to be located ~0.1 eV above the valence band edge of Ge surface by calculation [160] and experiment [161]. The charge neutrality level also locates near the valence band edge of $Ge_{1-x}Sn_x$ surface [162]. When the Fermi level is above the charge neutrality level, the interface is negatively charged due to the ionized acceptor-type states (occupied by electrons). When the Fermi level is below the charge neutrality level, the ionized donor-type states (empty or occupied by holes) build up a large number of positively charged interface charges.

Fig. 3.20(a) shows the interface trap density energy distribution of acceptor-type and donor-type traps and the energy band diagram near the n-type $Ge_{1-x}Sn_x$ surface channel of a p-MOSFET, when the Fermi level is located at the charge neutrality level. It is usually assumed the donor-type traps are present close to E_V and acceptor-type traps are located near E_C, as shown in the diagram [163]. The shaded area represents the total charged interface traps, associated with the positions of charge neutrality level and Fermi level. In this case, the transistor is in weak inversion region. Most of the acceptor-type traps that are above Fermi level and most of the donor-type traps that are located below Fermi level are therefore not ionized. On the contrary, when the transistor is operating in inversion regime as depicted in Fig. 3.20(b), the Fermi level of $Ge_{1-x}Sn_x$ moves down to below the charge neutrality level. Most of the donor-type traps that are

now located above the Fermi level become positively charged by consuming the inversion charges (holes). Therefore, these positively charged interface traps degrade the effective mobility by severe Coulomb scattering [76]. But at even higher inversion charge densities (in the strong inversion region), the trapped charge at the interface should be screened by the inversion carriers, which mitigates this effect on the mobility.

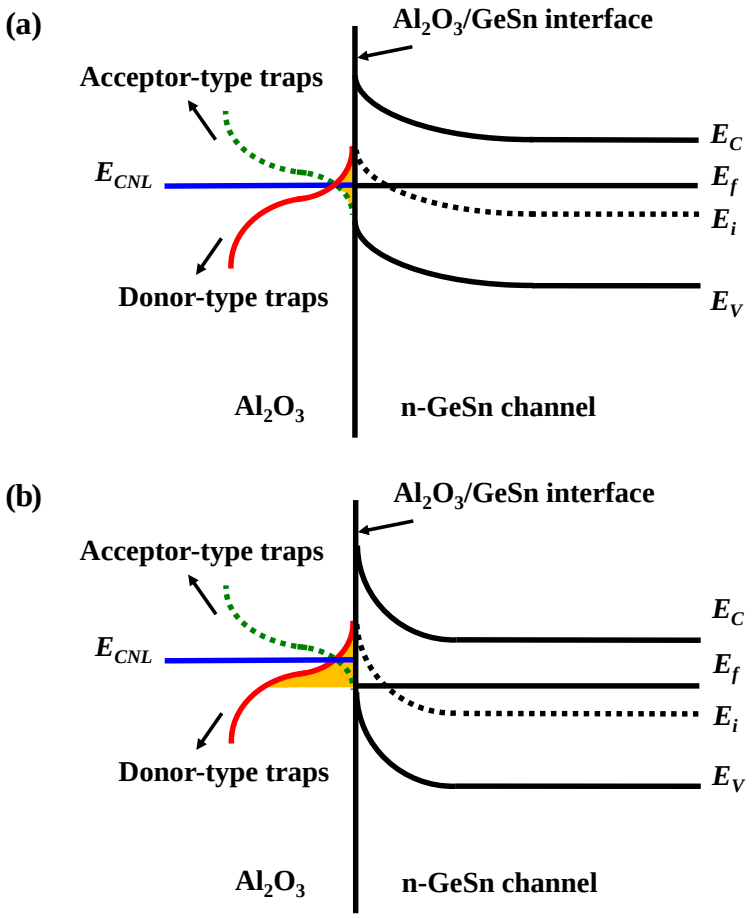


Fig. 3.20. Interface trap density energy distribution of acceptor-type and donor-type traps and energy band diagram near the n-type $Ge_{1-x}Sn_x$ surface channel of a p-MOSFET, (a) when the Fermi level is located at the charge neutrality level, or (b) when the transistor is operating in the strong inversion regime. It is commonly assumed that bands of donor-type and acceptor-type states are separate [163]. The shaded area represents the total charged interface traps, associated with the positions of charge neutrality level and Fermi level.

In addition, when the transistor is biased from the region depicted in Fig. 3.20(a) to region depicted in Fig. 3.20(b), a portion of the inversion carriers (holes) consumed by the donor-type traps in $Ge_{1-x}Sn_x$ surface plays another role in effective mobility degradation in the high inversion carrier density region. The extraction of mobility is based on the equation $I_S = \frac{W}{L_G}\mu_{eff} q N_{inv} V_{DS}$. R. Zhang *et al*. observed the inversion carrier loss due to large amount of interface traps near the valence band edge of Ge [165]. These interface traps are fast traps, which have small time constants and can respond at frequencies ranging from 1 kHz to 1 MHz. Therefore, the extracted inversion carrier density by integrating the inversion $C - V$ curve at 100 kHz (Fig. 3.7) includes two parts: 1) the inversion carriers that contribute to the current in the channel, and 2) the interface traps that do not supply any mobile carrier in the channel but just responds in the $C - V$ measurement. As a result, $N_{inv,}$ which was obtained by integrating the inversion $C - V$ curve, overestimates the actual mobile carriers that contribute to the current. This leads to underestimation of the mobility of the mobile carriers.

3.4 Summary

In this Chapter, surface passivation by treatment with $(NH_4)_2S$ aqueous solution (36%) was explored for the gate stack of high-mobility $Ge_{0.958}Sn_{0.042}$ p-MOSFETs with self-aligned Ni(GeSn) metallic S/D. High-quality single-crystalline $Ge_{0.958}Sn_{0.042}$ films were grown on Ge (100) substrate as the channel material. $Ge_{0.958}Sn_{0.042}$ p-MOSFETs with pre-gate $(NH_4)_2S$ passivation show decent transfer and output characteristics, and demonstrate a higher peak μ_{eff} in comparison with those of other (100)-oriented $Ge_{1-x}Sn_x$ p-MOSFETs reported so far. However, μ_{eff} in high N_{inv} region is still lower than that of those with low-temperature Si passivation.

Chapter 4

Improving the Thermal Stability of Nickel Stanogermanide by Incorporation of Platinum

4.1 Introduction

Germanium-tin ($Ge_{1-x}Sn_x$) alloy is a promising alternative channel material in metal-oxide-semiconductor field-effect transistors (MOSFETs) for high-performance logic applications, as it has higher mobilities than germanium (Ge) [48],[61]-[63],[86]-[91],[123]-[131]. In addition, $Ge_{1-x}Sn_x$ is lattice-mismatched to Ge, and can be utilized as source and drain (S/D) stressors to introduce compressive strain to Ge channel for hole mobility enhancement in Ge p-MOSFETs [111],[166]-[167].

Nickel germanide (NiGe) has been widely investigated as a self-aligned S/D contact material for Ge MOSFETs [96]-[110]. However, the poor thermal stability of NiGe inhibits its application to Ge MOSFETs. To resolve this issue, the incorporation of platinum (Pt) [168]-[169], zirconium (Zr) [170], palladium (Pd) [171] or titanium (Ti) [172] has been investigated to improve the thermal stability of NiGe by suppressing agglomeration during thermal annealing process.

Likewise, nickel stanogermanide [Ni(GeSn)] formed by the reaction of Ni and $Ge_{1-x}Sn_x$ can be a self-aligned S/D contact material for $Ge_{1-x}Sn_x$ MOSFETs, as well as Ge p-MOSFETs with $Ge_{1-x}Sn_x$ S/D stressors [111]-[113]. As discussed in

Chapter 2, the thermal stability of Ni(GeSn) has to be improved as it is also susceptible to agglomeration during anneal [112]. Particularly, degradation of Ni(GeSn) at temperatures between 350 °C and 500 °C may not be acceptable for back-end-of-line processes or for a gate-last process where anneals may be performed after contact formation, such as post-deposition anneal (PDA) [91],[173]-[174]. Therefore, a contact metallization process for $Ge_{1-x}Sn_x$ with good thermal stability is needed.

In this Chapter, a multi-phase Pt-incorporated stanogermanide metallization scheme on $Ge_{1-x}Sn_x$/Ge (100) substrate is investigated for the first time. The solid-phase reaction in a NiPt/$Ge_{1-x}Sn_x$/Ge (100) system is studied. Ni(GeSn) and $Pt_x(GeSn)_y$ phases are detected by X-ray diffraction (XRD). Therefore, the NiPt stanogermanide film formed on single-crystalline $Ge_{1-x}Sn_x$/Ge (100) substrate is hereafter referred to as [Ni(GeSn) + $Pt_x(GeSn)_y$]. Electrical characterization using micro four-point probes and material characterization using scanning electron microscopy (SEM), atomic force microscopy (AFM), and transmission electron microscopy (TEM) indicate that the incorporation of Pt improves the thermal robustness of stanogermanide contacts and suppresses agglomeration. A model is proposed to explain the agglomeration of Ni(GeSn) during the solid-state reaction of Ni and $Ge_{1-x}Sn_x$ at 450 °C and above and the effect of Pt incorporation. Part of this work is published in Refs. [175]-[176].

4.2 Experimental Details

Using 4-inch n-type Ge (100) wafers as starting substrates, $Ge_{1-x}Sn_x$ thin films were epitaxially grown by a solid source molecular beam epitaxy (MBE) system at 180 °C [56]. After *ex situ* pre-epitaxy cleaning in dilute hydrofluoric acid ($HF:H_2O$ = 1:10), the Ge wafers were loaded into the MBE growth chamber. This MBE growth, which has been discussed in detail in Chapter 3, was done by our collaborators (Prof. Buwen Cheng's group) at the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China.

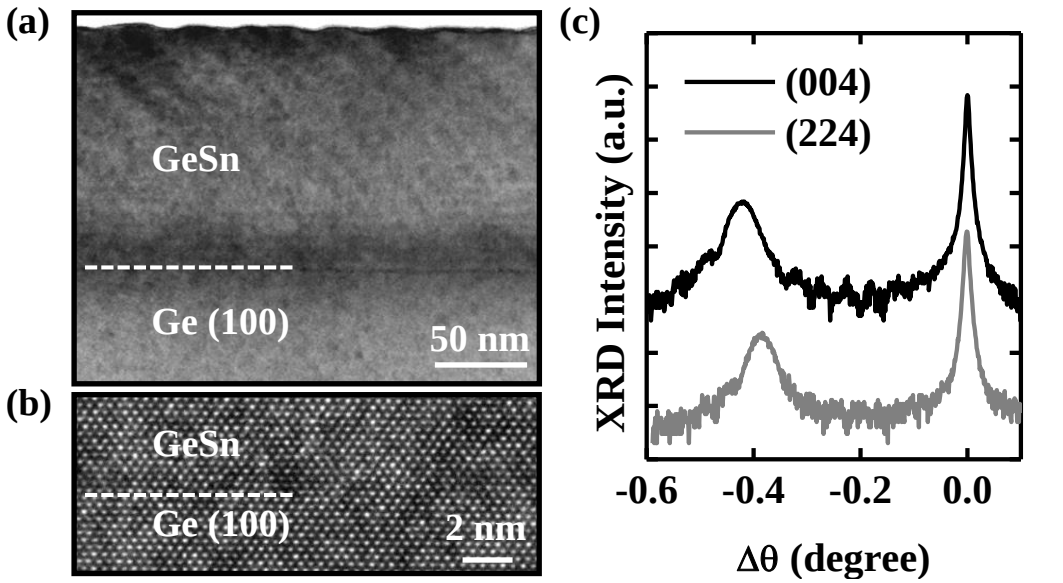


Fig. 4.1. (a) XTEM image of ~130-nm-thick epitaxial $Ge_{0.947}Sn_{0.053}$ film grown on Ge (100) substrate. (b) HRTEM image showing the periodic arrangement of atoms across the defect-free interface between $Ge_{1-x}Sn_x$ and Ge. (c) HRXRD (004) and (224) curves showing $Ge_{1-x}Sn_x$ grown on Ge (100) substrate is fully strained and the substitutional Sn composition is 5.3%. The TEM and HRXRD were performed as external service jobs at the Institute of Materials Research and Engineering (IMRE).

To calculate the substitutional Sn composition, high-resolution XRD (HRXRD) was performed on the as-grown $Ge_{1-x}Sn_x$ thin films. To obtain good XRD signal from the epitaxial film, a relative thick $Ge_{1-x}Sn_x$ film was used for material characterization. Fig. 4.1(a) shows the cross-sectional TEM (XTEM) image of ~130-nm-thick $Ge_{1-x}Sn_x$ film on Ge (100) substrate. Defect-free interface between single-crystalline $Ge_{1-x}Sn_x$ and Ge can be observed by high resolution TEM (HRTEM) as shown in Fig. 4.1(b). HRXRD (004) and (224) curves are shown in Fig. 4.1(c). The perpendicular and in-plane lattice constants of strained $Ge_{1-x}Sn_x$ are obtained to be 0.56461 nm and 0.57235 nm, respectively. Assuming tetragonal distortion of the epitaxial $Ge_{1-x}Sn_x$ layer grown on Ge (100) substrate, the lattice constant of unstrained $Ge_{1-x}Sn_x$ is calculated to be 0.56908 nm. Taking the lattice constants of Ge and Sn to be 0.564613 nm and 0.648920 nm, respectively [148], the Sn composition is obtained to be 5.3% by applying Vegard's law. The $Ge_{0.947}Sn_{0.053}$ film is fully strained to Ge (100) substrate.

~16-nm-thick $Ge_{0.947}Sn_{0.053}$ film grown on n-type Ge (100) substrate was used for this study. A cyclic clean was used for pre-deposition cleaning, which involves treating the wafers with deionized water followed by dilute hydrofluoric acid ($HF:H_2O$ = 1:50) in each cycle. 6 nm of mixture of Ni and Pt was deposited by co-sputtering in a magnetron sputtering system. The molar ratio of Ni to Pt is ~3, as obtained by Energy Dispersive X-Ray Analysis (EDX). For the control samples, 6 nm of pure Ni was deposited. All samples were subjected to a rapid thermal anneal (RTA) process in a nitrogen gas (N_2) ambient for metal stanogermanide formation. The annealing temperature is 350 °C, 450 °C, 500 °C, or 550 °C. The annealing time is kept at 30 s. Some of the metal stanogermanide samples formed at 350 °C were subjected to a second anneal in N_2 ambient at 500

°C for 60 s, which is a typical PDA condition used in transistor fabrication [91], [173]-[174]. All experimental splits are summarized in Table 4.1.

XRD was carried out to identify the phase and crystal orientation of the annealed samples. SEM and AFM were used to analyze surface morphology of the metal stanogermanide films. XTEM was used for analyzing the layer structure. Micro four-point probe measurement was employed to measure sheet resistance R_{Sh} of the stanogermanide film.

Table 4.1. Summary of experimental splits.

Sample ID	Metal(s)	Annealing Temperature(s) (°C)	Annealing Time(s)
1-1	Ni	350	30
1-2	Ni	450	30
1-3	Ni	500	30
1-4	Ni	550	30
1-5	Ni	350 (1^{st} anneal) + 500 (2^{nd} anneal)	30 (1^{st} anneal) + 60 (2^{nd} anneal)
2-1	Ni:Pt = 3:1	350	30
2-2	Ni:Pt = 3:1	450	30
2-3	Ni:Pt = 3:1	500	30
2-4	Ni:Pt = 3:1	550	30
2-5	Ni:Pt = 3:1	350 (1^{st} anneal) + 500 (2^{nd} anneal)	30 (1^{st} anneal) + 60 (2^{nd} anneal)

4.3 Characterization of Metal Stanogermanides

4.3.1 Phase Identification: XRD

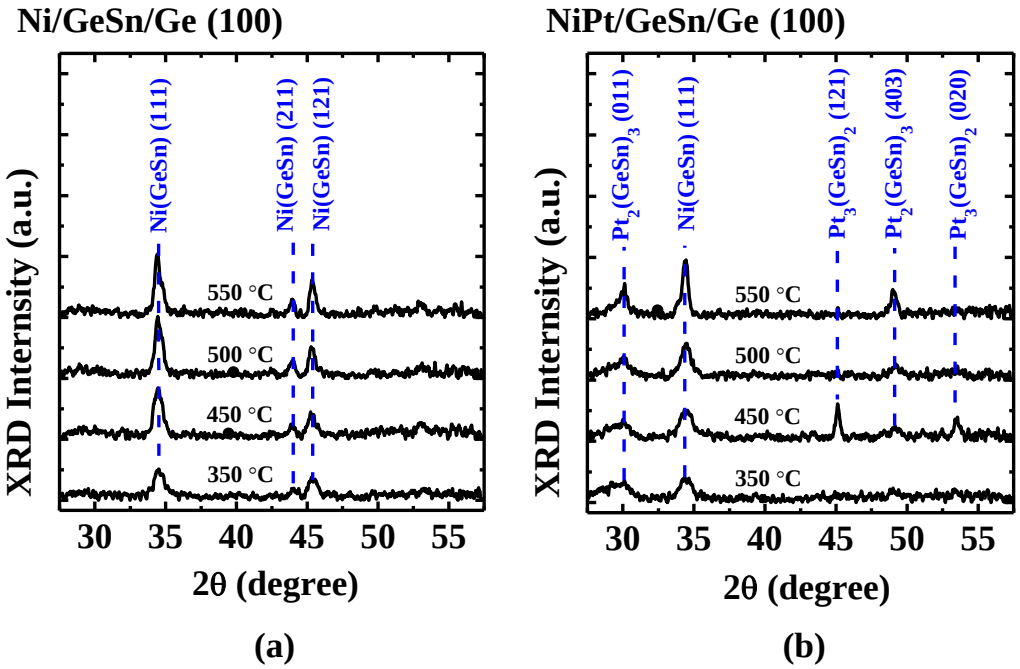


Fig. 4.2. XRD spectra of (a) Ni/$Ge_{1-x}Sn_x$/Ge (100) and (b) NiPt/$Ge_{1-x}Sn_x$/Ge (100) samples after annealing at various temperatures for 30 s. The XRD was performed as an external service job at the IMRE.

Fig. 4.2 illustrates XRD spectra obtained on (a) Ni/$Ge_{1-x}Sn_x$/Ge (100) and (b) NiPt/$Ge_{1-x}Sn_x$/Ge (100) samples after annealing at various temperatures for 30 s. Any peak of pure Sn or Sn alloys cannot be observed in all of the samples, probably because of the low substitutional Sn composition. Identical profiles are observed for Ni/$Ge_{1-x}Sn_x$/Ge (100) samples after annealing at temperatures ranging from 350 °C to 550 °C as shown in Fig. 4.2(a). Ni monostanogermanide is formed, with the Ni(GeSn) peaks closely coinciding with those of Ni monogermanide due to the small amount of Sn [112]-[113]. Likewise, the incorporation of Pt results in $Pt_2(GeSn)_3$ and $Pt_3(GeSn)_2$ peaks closely coinciding with those of Pt_2Ge_3 and Pt_3Ge_2, respectively, for NiPt/$Ge_{1-x}Sn_x$/Ge (100) samples

after annealing at temperatures ranging from 350 °C to 550 °C as shown in Fig. 4.2(b) [177].

4.3.2 Sheet Resistance: Micro Four-point Probe Measurement

R_{Sh} values of stanogermanide films formed at various temperatures were measured by micro four-point probes as shown in Fig. 4.3. It should be noted that the R_{Sh} of the Ni/$Ge_{1-x}Sn_x$/Ge (100) sample after annealing at 550 °C is too large to be measured by the micro four-point probes used in this work. For the Ni/$Ge_{1-x}Sn_x$/Ge (100) samples, R_{Sh} increases significantly from 52.5 to 8.8×10^3 Ω/square, indicating that there may be a substantial change of surface morphology from 450 to 500 °C. In contrast, R_{Sh} of [Ni(GeSn)+Pt_x(GeSn)$_y$] is relatively stable from 350 to 500 °C, indicating that the film quality is stable up to 500 °C.

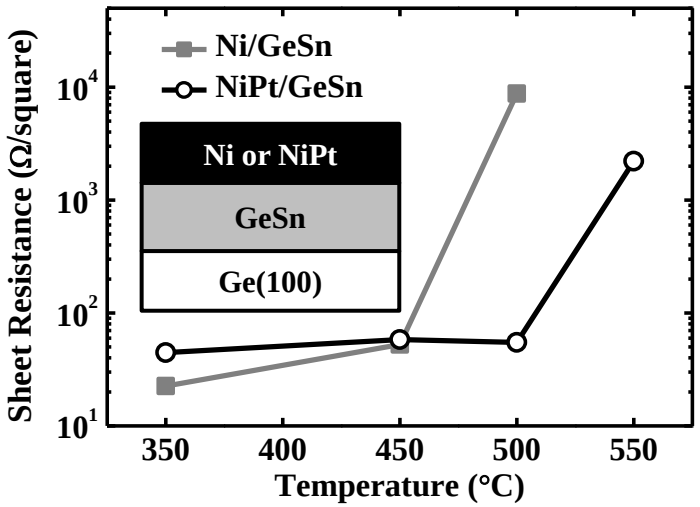


Fig. 4.3 R_{Sh} of Ni/$Ge_{1-x}Sn_x$/Ge (100) and NiPt/$Ge_{1-x}Sn_x$/Ge (100) samples after annealing at various temperature measured by micro four-point probes that was performed by Mr. Eugene Kong in our group.

4.3.3 Surface Morphology: SEM and AFM

Top-view SEM characterization was performed to examine the morphological evolution of the samples after annealing at different temperatures for 30 s. SEM images in Fig. 4.4 show the contrast in film morphology for Ni stanogermanide films from 350 to 550 °C. The surface of the Ni/$Ge_{1-x}Sn_x$/Ge (100) sample after annealing at 350 °C is smooth [Fig. 4.4(a)]. As the stanogermanidation temperature increases to 450 °C, the Ni stanogermanide film becomes rough as the exposed $Ge_{1-x}Sn_x$ surface begins to appear [Fig. 4.4(b)]. Discrete Ni(GeSn) islands are observed after annealing at 500 °C and beyond [Fig. 4.4(c) and (d)]. Similar result can be seen in Refs. [111] and [112]. This explains the sharp increase of R_{Sh} of Ni(GeSn) from 450 to 500 °C as shown in Fig. 4.4. SEM images of NiPt/$Ge_{1-x}Sn_x$/Ge (100) samples after annealing at various temperatures are shown in Fig. 4.5. After annealing at each temperature, the surface morphology of the Pt-incorporated stanogermanide film is observably better than that of pure Ni stanogermanide film. The NiPt/$Ge_{1-x}Sn_x$/Ge (100) sample remains smooth after annealing at 450 °C [Fig. 4.5(b)], and is still almost continuous after annealing at 500 °C [Fig. 4.5(c)]. Agglomeration occurs only after annealing at 550 °C [Fig. 4.5(d)]. The surface morphological evolution of NiPt/$Ge_{1-x}Sn_x$/Ge (100) sample after annealing at various temperatures is also consistent with the electrical characteristics as shown in Fig. 4.3.

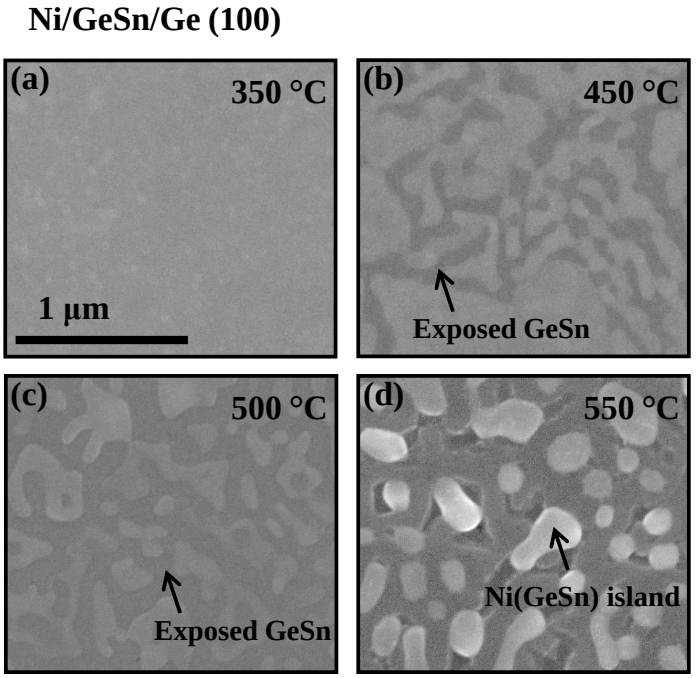


Fig. 4.4. Top-view SEM images of the Ni/$Ge_{1-x}Sn_x$/Ge (100) samples after RTA for 30 s at (a) 350 °C, (b) 450 °C, (c) 500 °C, and (d) 550 °C. Scale bar is shown in (a), and all the images are of the same scale.

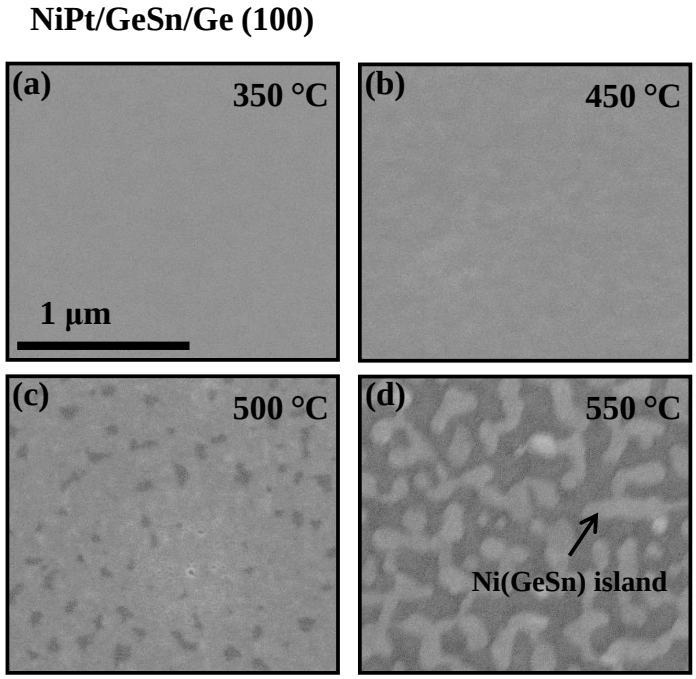


Fig. 4.5. Top-view SEM images of the NiPt/$Ge_{1-x}Sn_x$/Ge (100) samples after RTA for 30 s at (a) 350 °C, (b) 450 °C, (c) 500 °C, and (d) 550 °C. Scale bar is shown in (a), and all the images are of the same scale.

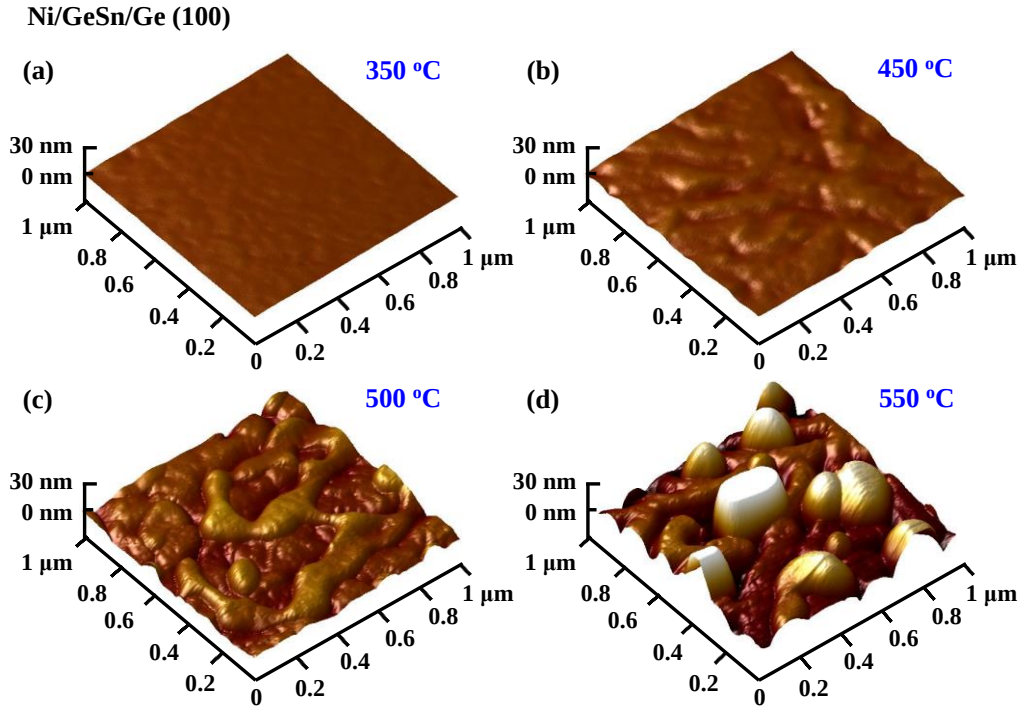


Fig. 4.6. AFM images of the Ni/$Ge_{1-x}Sn_x$/Ge (100) samples after RTA for 30 s at (a) 350 °C, (b) 450 °C, (c) 500 °C, and (d) 550 °C.

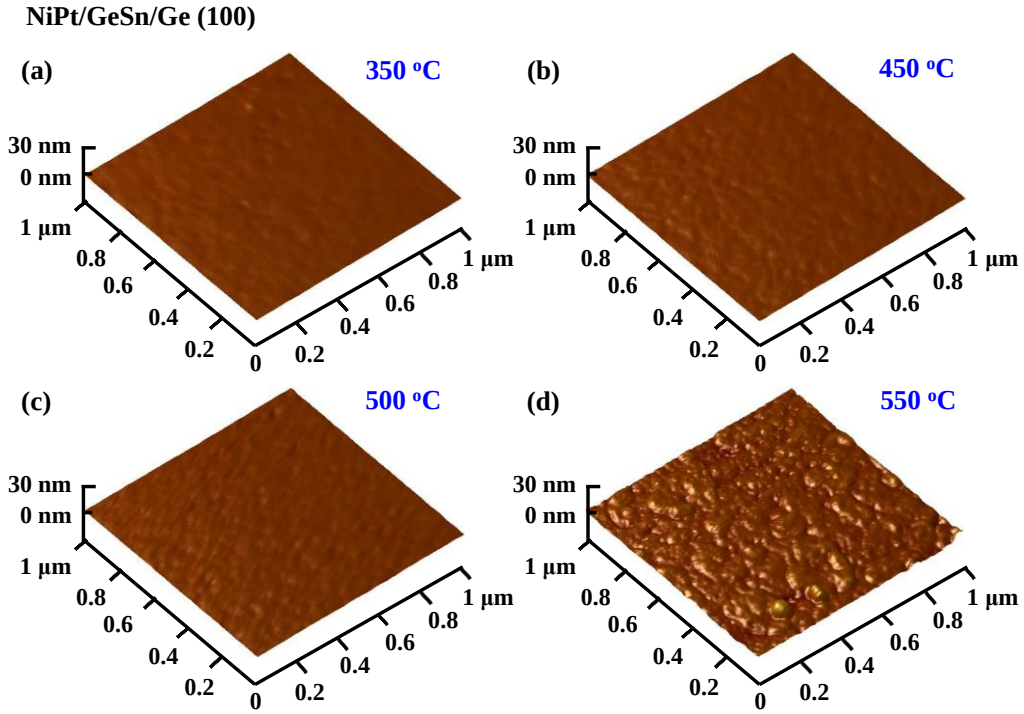


Fig. 4.7. AFM images of the NiPt/$Ge_{1-x}Sn_x$/Ge (100) samples after RTA for 30 s at (a) 350 °C, (b) 450 °C, (c) 500 °C, and (d) 550 °C.

AFM images in Figs. 4.6 and 4.7 show the surface morphology of Ni/$Ge_{1-x}Sn_x$/Ge (100) and NiPt/$Ge_{1-x}Sn_x$/Ge (100) samples after annealing for 30 s at different temperatures, respectively. The AFM scanning area is 1 μm × 1 μm. The Ni/$Ge_{1-x}Sn_x$/Ge (100) sample annealed at 350 °C for 30 s has a smooth surface [Fig. 4.6(a)]. Grain boundary grooving can be clearly observed for the Ni/$Ge_{1-x}Sn_x$/Ge (100) sample after annealing at 450 °C [Fig. 4.6(b)]. Further grain separation occurs for the sample after annealing at 500 °C [Fig. 4.6(c)]. The surface of Ni/$Ge_{1-x}Sn_x$/Ge (100) sample after annealing at 550 °C turns to be extremely rough due to the formation of large discrete islands [Fig. 4.6(d)]. The NiPt/$Ge_{1-x}Sn_x$/Ge (100) sample is still smooth after annealing at 350 °C [Fig. 4.7(a)], 450 °C [Fig. 4.7(b)] or 500 °C [Fig. 4.7(c)]. After annealing at 550 °C, the surface becomes rough due to agglomeration [Fig. 4.7(d)]. Based on the results of surface morphology inspected by SEM and AFM, Pt-incorporated stanogermanide films exhibit enhanced thermal stability up to 500 °C compared with pure Ni stanogermanide films.

4.3.4 Layer Structure: TEM

To examine the interfacial structure, XTEM images were taken on the Ni/$Ge_{1-x}Sn_x$/Ge (100) and NiPt/$Ge_{1-x}Sn_x$/Ge (100) samples after annealing at 450 °C and 500 °C. Grain boundary grooving can be clearly observed for the Ni/$Ge_{1-x}Sn_x$/Ge (100) sample after annealing at 450 °C, resulting in the non-uniformity of Ni stanogermanide film thickness [Fig. 4.8(a)]. Discrete Ni(GeSn) island and exposed $Ge_{1-x}Sn_x$ surface are observed after annealing at 500 °C [Fig. 4.8(b)]. In contrast, the thickness of the multi-phase Pt-incorporated stanogermanide film

formed at 450 °C is much more uniform than that of the Ni stanogermanide film formed at the same temperature [Fig. 4.9(a)]. In comparison with the agglomerated Ni(GeSn) film formed at 500 °C, the Pt-incorporated stanogermanides film formed at 500 °C is still continuous [Fig. 4.9(b)].

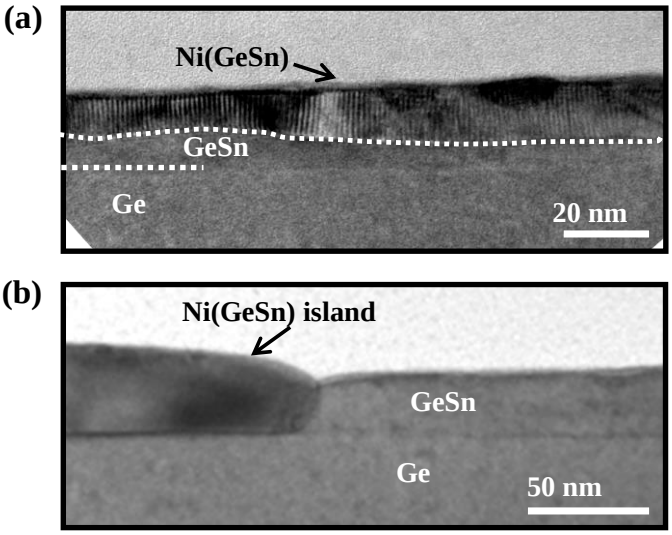


Fig. 4.8. XTEM images of Ni/$Ge_{1-x}Sn_x$/Ge (100) samples after annealing at (a) 450 °C and (b) 500 °C. The TEM in Fig. 4.8(a) and Fig. 4.9(a) were done by Dr. Qian Zhou in our group; the TEM in Fig. 4.8(b) and Fig. 4.9(b) were performed as external service jobs at IMRE.

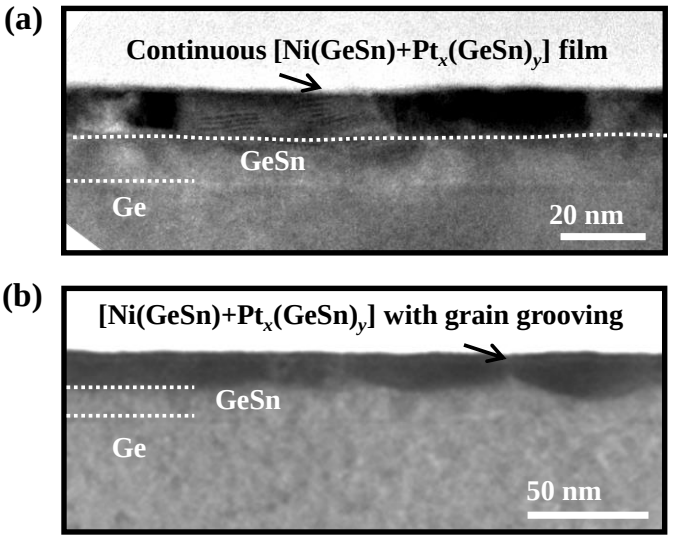


Fig. 4.9. XTEM images of NiPt/$Ge_{1-x}Sn_x$/Ge (100) samples after annealing at (a) 450 °C and (b) 500 °C.

4.3.5 Impact of Post-deposition Anneal

SEM and AFM images were taken on (a) Ni/$Ge_{1-x}Sn_x$/Ge (100) and (b) NiPt/$Ge_{1-x}Sn_x$/Ge (100) samples annealed at 350 °C for stanogermanide formation, which were then subject to PDA. After PDA, the Ni stanogermanide film becomes very rough, due to the formation of discrete stanogermanide islands as shown Fig. 4.10 (a) and Fig. 4.11(a). In contrast, the Pt-incorporated stanogermanide film is still continuous as shown in Fig. 4.10 (b) and Fig. 4.11(b), indicating there is no degradation after PDA.

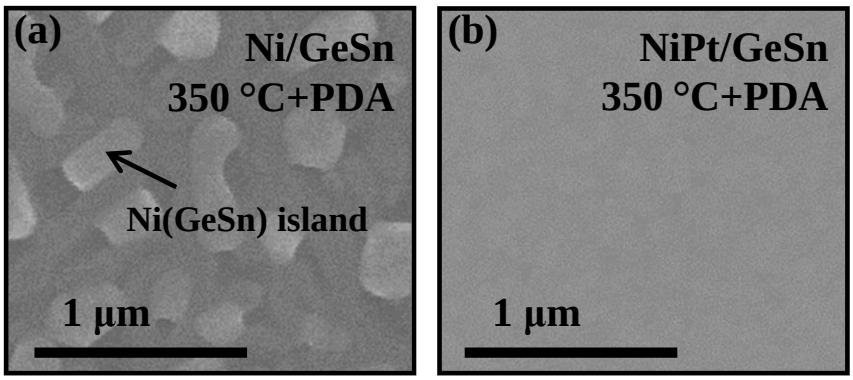


Fig. 4.10. Top-view SEM images of (a) Ni/$Ge_{1-x}Sn_x$/Ge (100) sample and (b) NiPt/$Ge_{1-x}Sn_x$/Ge (100) sample annealed at 350 °C for stanogermanide formation, which were then subject to a second anneal at 500 °C for 60 s (PDA).

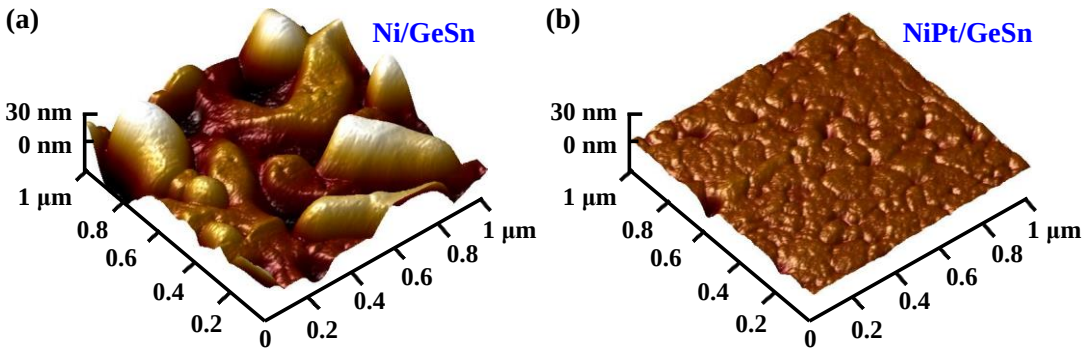


Fig. 4.11. AFM images of (a) Ni/$Ge_{1-x}Sn_x$/Ge (100) sample and (b) NiPt/$Ge_{1-x}Sn_x$/Ge (100) sample annealed at 350 °C for stanogermanide formation, which were then subject to PDA.

4.4 Discussion

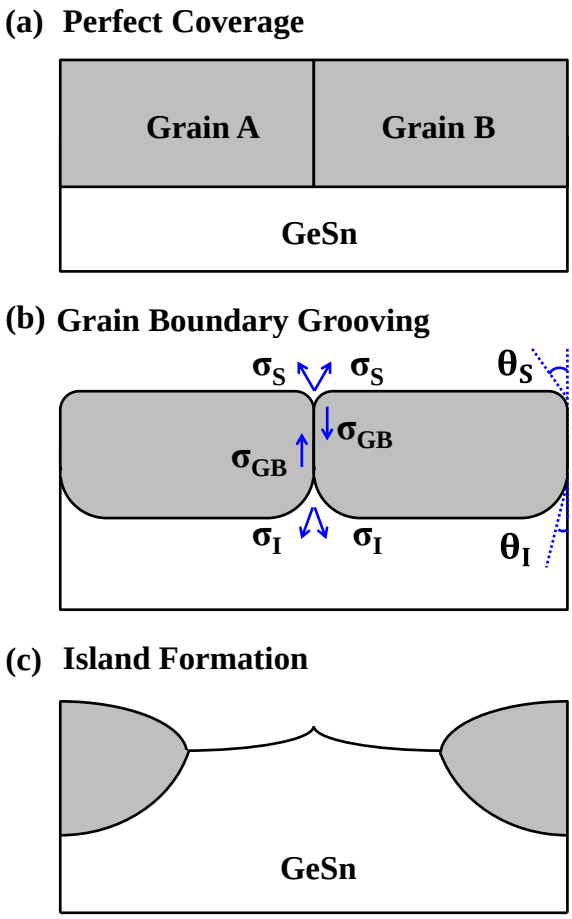


Fig. 4.12. Schematics illustrating the evolution of the stanogermanide films on single-crystalline $Ge_{1-x}Sn_x$ during annealing, starting from (a) perfect coverage, to (b) grain boundary grooving, and to (c) island formation.

Agglomeration is illustrated with Ni(GeSn)/$Ge_{1-x}Sn_x$ as shown in Fig. 4.12, where the morphological rearrangement is driven by the reduction in surface and interfacial energy during annealing [178]. A model is proposed to explain the agglomeration of metal stanogermanide during the reaction of metal and $Ge_{1-x}Sn_x$ and the effect of Pt incorporation. The evolution of stanogermanide films during annealing starts from perfect coverage [Fig. 4.12 (a)], to grain boundary grooving [Fig. 4.12(b)], and to island formation [Fig. 4.12(c)]. At the beginning, two identical stanogermanide grains cover the $Ge_{1-x}Sn_x$ perfectly. The transport of

atoms, typically through diffusion, results in the grain boundary grooving. When the grooves become sufficiently deep to expose the underlying $Ge_{1-x}Sn_x$ film, the discrete islands of metal stanogermanide are formed.

XRD results have revealed that the Pt-incorporated multi-phase stanogermanide film is a mixture of $Pt_x(GeSn)_y$ and Ni(GeSn) as shown in Fig. 4.2(b). In comparison with Ni-Ge bond (290 kJ/mol), the stronger Pt-Ge bond (400 to 500 kJ/mol) makes the atomic diffusion be more difficult at the surface and interface, and along grain-boundaries [168]. Therefore, the incorporation of Pt retards the transformation from perfect coverage of stanogermanide film on $Ge_{1-x}Sn_x$ [Fig. 4.12(a)] to grain boundary grooving [Fig. 4.12(b)].

When grain boundary grooving occurs, two local equilibrium balances need to be satisfied as shown in Fig. 4.12(b). They are the balance of the stanogermanide surface energy σ_S and the stanogermanide-stanogermanide grain-boundary energy σ_{GB} and the balance of the stanogermanide-$Ge_{1-x}Sn_x$ interface energy σ_I and σ_{GB}, respectively, as shown in Equations (4.1) and (4.2) [179]-[180].

$$\sigma_{GB} = 2\sigma_S \cos\theta_S , \tag{4.1}$$

$$\sigma_{GB} = 2\sigma_I \cos\theta_I , \tag{4.2}$$

where θ_S and θ_I are the contact angles at the surface and interface, respectively. Incorporating Pt in stanogermanide film reduces σ_{GB} upon alloying [181]. In addition, the incorporation of Pt has the effect of increasing σ_S and σ_I [182]-[183]. According to Equations (4.1) and (4.2), these two effects slow down the increasing of θ_S and θ_I, and therefore retard the transformation from grain boundary grooving to island formation.

XTEM images shown in Section 4.3.4 are the direct proof that the incorporation of Pt slows down the transformation from perfect coverage, to the grain boundary grooving, and to island formation. After annealing at 450 °C, the grain boundary grooving occurs only for the case of the Ni stanogermanide film [Fig. 4.8(a)]. Uniform [Ni(GeSn) + $Pt_x(GeSn)_y$] on $Ge_{1-x}Sn_x$ [Fig. 4.9 (a)] indicates that the Pt-incorporated stanogermanide film still covers the $Ge_{1-x}Sn_x$ almost perfectly. In addition, XTEM image in Fig. 4.8(b) shows evidence of island formation for the Ni/$Ge_{1-x}Sn_x$/Ge (100) sample after annealing at 500 °C. In contrast, XTEM image in Fig. 4.9(b) shows that the Pt-incorporated stanogermanide film is still continuous with slight grain boundary grooving after annealing at the same temperature. This confirms the onset of island formation is delayed due to the incorporation of Pt.

4.5 Summary

In this Chapter, a thermally stable Pt-incorporated stanogermanide metallization scheme is achieved. SEM and AFM images indicate that the surface of Ni/$Ge_{1-x}Sn_x$/Ge (100) sample becomes rough after annealing at 450 °C, which is the cause of the sharp increase in R_{Sh} from 450 to 500 °C. In contrast, SEM and AFM images show that the surface of NiPt/$Ge_{1-x}Sn_x$/Ge (100) sample is still smooth even after annealing at 500 °C, which is consistent with the result of sheet resistance measurement. Only the Pt-incorporated stanogermanide film formed at 350 °C is still smooth after a second anneal at 500 °C for 60 s.

The incorporation of Pt has the effect of slowing down the transformation not only from perfect coverage to grain boundary grooving, but also from grain boundary grooving to island formation. This explains that the incorporation of Pt improves the thermal robustness of stanogermanide contacts and suppresses agglomeration.

Chapter 5

Towards Highly Doped N-type Germanium-Tin: Low Annealing Temperature for Reduced Dopant Diffusion and the Use of Elevated Implant Temperature for Self-crystallization and Improved Dopant Activation

5.1 Introduction

Germanium-Tin ($Ge_{1-x}Sn_x$) can potentially be used in future logic applications, as it has higher carrier mobilities than Ge [48],[61]-[64],[86]-[91],[123]-[131]. To realize high-performance $Ge_{1-x}Sn_x$ n-channel metal-oxide-semiconductor field-effect transistors (n-MOSFETs) [92],[124],[125],[129] and $Ge_{1-x}Sn_x$ tunneling field-effect transistors (TFETs) [184]-[187], the source/drain (S/D) series resistance $R_{S/D}$ needs to be below 300 Ω-μm [35]. Therefore, high n-type dopant activation in $Ge_{1-x}Sn_x$ is needed.

Single-crystalline $Ge_{1-x}Sn_x$ grown by non-equilibrium processes such as molecular beam epitaxy (MBE) [49]-[57] and chemical vapor deposition (CVD) [58]-[60] is metastable. When metastable $Ge_{1-x}Sn_x$ is subsequently annealed during dopant activation, Sn segregation could occur and therefore x may decrease.

For annealing temperatures higher than 540 °C, high-resolution X-ray diffraction (HRXRD) analysis shows that the substitutional Sn composition in epitaxial $Ge_{0.922}Sn_{0.078}$ decreases gradually as annealing temperature increases [188]. $Ge_{1-x}Sn_x$ is less thermally stable for higher Sn compositions (e.g. x = 0.1 in Ref. [82]). Annealing at temperatures above 400 °C (e.g. dopant activation) results in not only Sn segregation but also nanodot formation, which is detrimental for transistor [82].

On the other hand, n-type dopants generally have high diffusion coefficients in Ge (e.g. 4.38×10^{-2} cm^2/s for phosphorus (P) at temperatures ranging from 600 °C to 850 °C [115]), rendering high-temperature dopant activation anneals unsuitable for shallow junction formation in Ge. If the incorporation of a small amount of Sn does not change the diffusion behavior of n-type dopants, high-temperature anneals may be likewise not preferable for activation of n-type dopants in $Ge_{1-x}Sn_x$. To obtain a high concentration of active n-type dopants with shallow junction depth, a delicate balance between dopant activation and dopant diffusion has to be achieved.

In the first part of this Chapter, we investigate $Ge_{0.976}Sn_{0.024}$ n^+/p junction formation using phosphorus ion (P^+) implant without heating the substrate during the implant. Various rapid thermal annealing (RTA) temperatures are investigated to activate the dopants. The electrically active P depth profile in the $Ge_{1-x}Sn_x$ is extracted using a spreading resistance probe (SRP). The current I – voltage V characteristics of the transfer length method (TLM) test structures that were used to extract contact resistivity and n^+/p junction diodes are also studied. Part of this work is published in Ref. [189].

Recently, it was reported that hot ion implant, which involves ion implantation at elevated substrate temperature (500 °C), can achieve a higher P activation in Ge than ion implantation at room temperature (RT) [190]. In addition, amorphizing ion implants have been shown to induce the formation of twin boundary defects or polycrystalline fin during silicon (Si) fin doping [191]. Hot implant avoids amorphization during implant due to self-crystallization and has been demonstrated as an excellent source/drain extension (SDE) doping technique for the narrow fins of FinFETs [192]-[194]. However, there are no reports of hot implant in $Ge_{1-x}Sn_x$ alloys so far.

Therefore, in the second part of this Chapter, we investigate the effect of P^+ implant temperature on the material properties of epitaxial $Ge_{1-x}Sn_x$ alloy and the electrical characteristics of TLM test structures and n^+/p junction diodes. Hot P^+ implant maintains the single-crystallinity of $Ge_{1-x}Sn_x$ during the implant. In addition, after post-implant RTA at 450 °C for 3 minutes, samples implanted at elevated temperature (400 °C) achieve a lower contact resistivity ρ_C than samples implanted at room temperature, indicating higher P dopant activation for hot P^+ implant in $Ge_{1-x}Sn_x$ after RTA. Part of this work is published in Ref. [195].

5.2 Material Characterization of $Ge_{0.976}Sn_{0.024}$

4-inch gallium-doped (5×10^{17} cm^{-3}) Ge (100) wafers were used as starting substrates for $Ge_{1-x}Sn_x$ growth and for fabrication of Ge control diodes. After *ex situ* pre-epitaxy cleaning in dilute hydrofluoric acid ($HF:H_2O = 1:10$), the Ge wafers were loaded into the growth chamber of a solid source MBE system. Single-crystalline $Ge_{1-x}Sn_x$ films were epitaxially grown at 180 °C [56]. $Ge_{1-x}Sn_x$ has an unintentional p-type doping concentration of 5×10^{16} cm^{-3}, as obtained by Hall measurement, due to the presence of vacancies in the films [145]-[147]. The MBE growth process was done by our collaborators (Prof. Buwen Cheng's group) at the Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China, and has been discussed in detail in Chapter 3.

Cross-sectional transmission electron microscopy (XTEM) image of a ~170-nm-thick $Ge_{1-x}Sn_x$ film on Ge substrate is shown in Fig. 5.1(a). High-resolution TEM (HRTEM) images depict a high-quality single-crystalline $Ge_{1-x}Sn_x$ film without observable defects near the $Ge_{1-x}Sn_x$/Ge interface [Fig. 5.1(b)] and at the surface [Fig. 5.1(c)]. Atomic force microscopy (AFM) image of the $Ge_{1-x}Sn_x$ surface shows a smooth surface with a root-mean-square (RMS) roughness of 0.37 nm with a scanning area of 10 μm × 10 μm as shown in Fig. 5.1(d). (004) and (224) reciprocal space maps (RSM) obtained using HRXRD [Figs. 5.2(a) and (b)] show that the film is fully strained to the Ge substrate and the substitutional Sn composition is determined to be 2.4%.

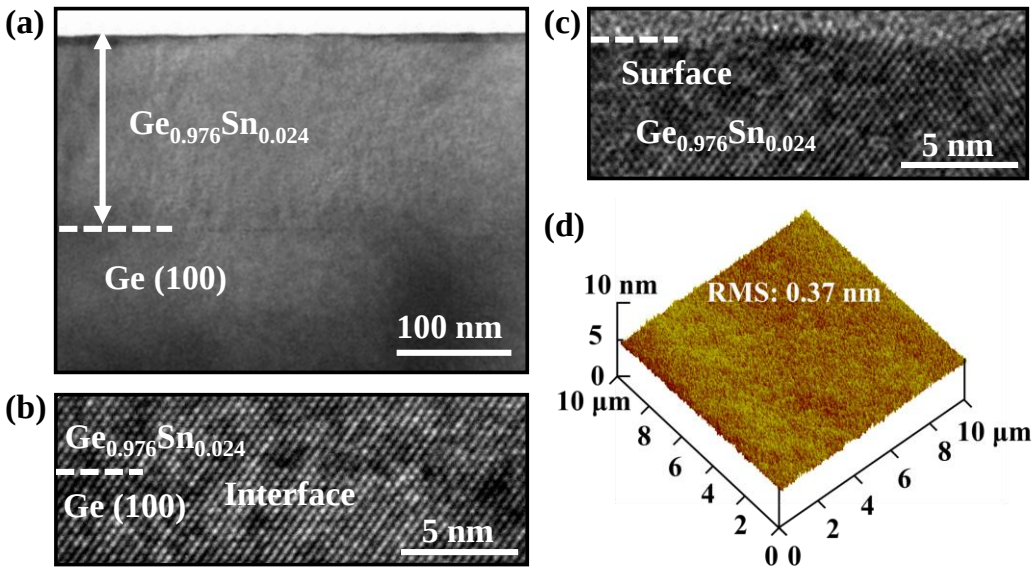


Fig. 5.1. (a) XTEM image of ~ 170-nm-thick epitaxial $Ge_{0.976}Sn_{0.024}$ film grown on Ge (100) substrate. HRTEM images of the defect-free (b) $Ge_{1-x}Sn_x$/Ge interface and (c) $Ge_{1-x}Sn_x$ surface. (d) AFM image of the $Ge_{1-x}Sn_x$ surface with a RMS roughness of 0.37 nm with a scanning area of 10 μm × 10 μm. The TEM was performed as an external service job at the Institute of Materials Research and Engineering (IMRE).

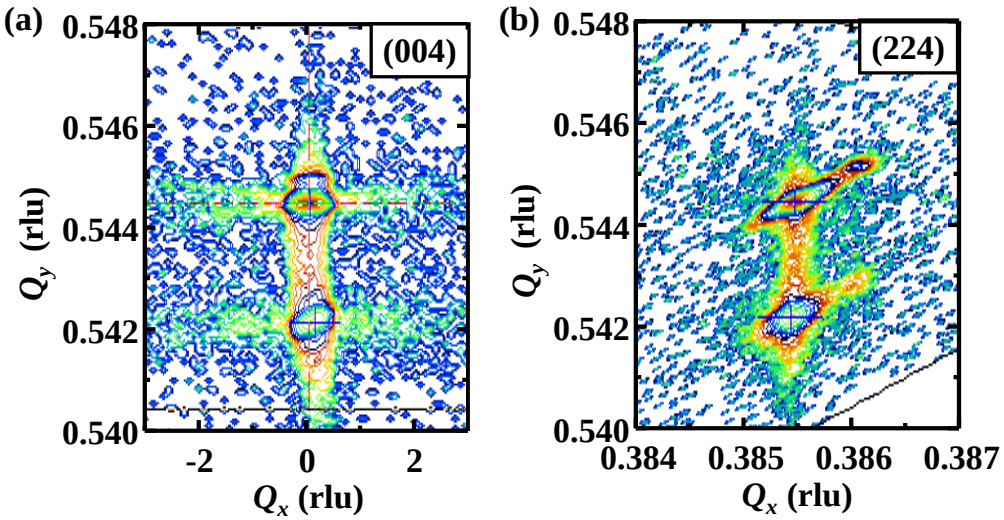


Fig. 5.2. (a) (004) and (b) (224) RSM obtained using HRXRD show that the $Ge_{1-x}Sn_x$ film has a substitutional Sn composition of 2.4% and is fully strained to the Ge substrate. The HRXRD was performed as an external service job at IMRE.

5.3 $Ge_{0.976}Sn_{0.024}$ n^+/p Junction Formation by RT P^+ Implant and RTA at Various Activation Temperatures

5.3.1 Experimental Details

To evaluate the properties of n^+/p junctions, TLM test structures formed on n^+-$Ge_{1-x}Sn_x$ regions and $Ge_{1-x}Sn_x$ n^+/p junction diodes were fabricated. A 100-nm-thick silicon dioxide (SiO_2) isolation layer was deposited by sputter, covered with patterned photoresist (PR), and etched to define active regions using a chlorine-based plasma etching process. P^+ implant was performed at energy of 20 keV and a dose of 2×10^{15} cm^{-2} into the active regions, followed by PR removal. The implant was performed as an external service job at the INNOViON Corporation, San Jose, California, USA. Dopant loss during subsequent thermal annealing activation by out-diffusion from Ge surface has been reported [196]. A 50-nm SiO_2 capping layer was then intentionally deposited by sputter to prevent most of this loss [197]. The samples were activated at 300 °C for 10 minutes, 350 °C for 10 minutes, or 400 °C for 5 minutes. After dopant activation, patterned PR was used as the mask to etch SiO_2 contact openings, followed by 100-nm-thick aluminum (Al) deposition by e-beam evaporator and liftoff to form metal contacts.

Secondary ion mass spectroscopy (SIMS) was used to examine P distribution in the implanted samples. The electrically active P depth profile in $Ge_{1-x}Sn_x$ was studied using SRP.

5.3.2 Electrical Characterization

Fig. 5.3(a) depicts the top-view scanning electron microscopy (SEM) image of a fabricated TLM test structure. The inset image of Fig. 5.4 shows the schematic of a TLM test structure in cross-sectional view and top view. Contact width Z is 100 μm; contact spacing d varies from 3 μm to 100 μm. Fig. 5.3 shows the $I - V$ characteristics of TLM test structures with various contact spacings d formed on the n^+-$Ge_{1-x}Sn_x$ regions activated using post-implant RTA at (b) 300 °C for 10 minutes, (c) 350 °C for 10 minutes, and (d) 400 °C for 5 minutes.

It has been demonstrated that the Fermi level E_f at the metal/Ge interface is pinned at the valence band edge E_V of Ge, resulting in a high electron Schottky barrier height (SBH) Φ_B and therefore a large ρ_C of metal/n-type Ge [161],[198]. Fermi level pinning toward E_V also occurs for metal/n-type $Ge_{1-x}Sn_x$ contacts [162]. Therefore, ohmic contact can only be achieved between metal and highly doped n-type $Ge_{1-x}Sn_x$, due to conduction via electron tunneling through the Schottky barrier.

Fig. 5.3(e) compares $I - V$ curves of TLM test structures with a given spacing of 3 μm for the three splits. The sample activated by annealing for 10 minutes at 300 °C or 350 °C does not yield a linear relationship between the voltage applied and the current that flows through the contacts (non-ohmic behavior). This indicates that the annealing is insufficient for phosphorus activation to form a highly doped n-type region. On the other hand, the sample activated at 400 °C for 5 minutes demonstrates ohmic behavior.

Fig. 5.4 shows the total resistance R_{Total} versus d obtained from the TLM test structure formed by annealing at 400 °C for 5 minutes, which shows ohmic

behavior. R_{Total} is given by I/V at V = 0.5 V and is linear function of d. The ρ_C is extracted to be 2.7 × 10^{-4} Ω-cm^2, which is given by $\frac{R_C^2 \times Z}{Slope}$. R_C is the contact resistance, given by $R_{Total}/2$ at the intercept of a linearly fitted line with the vertical axis (where d = 0) [199].

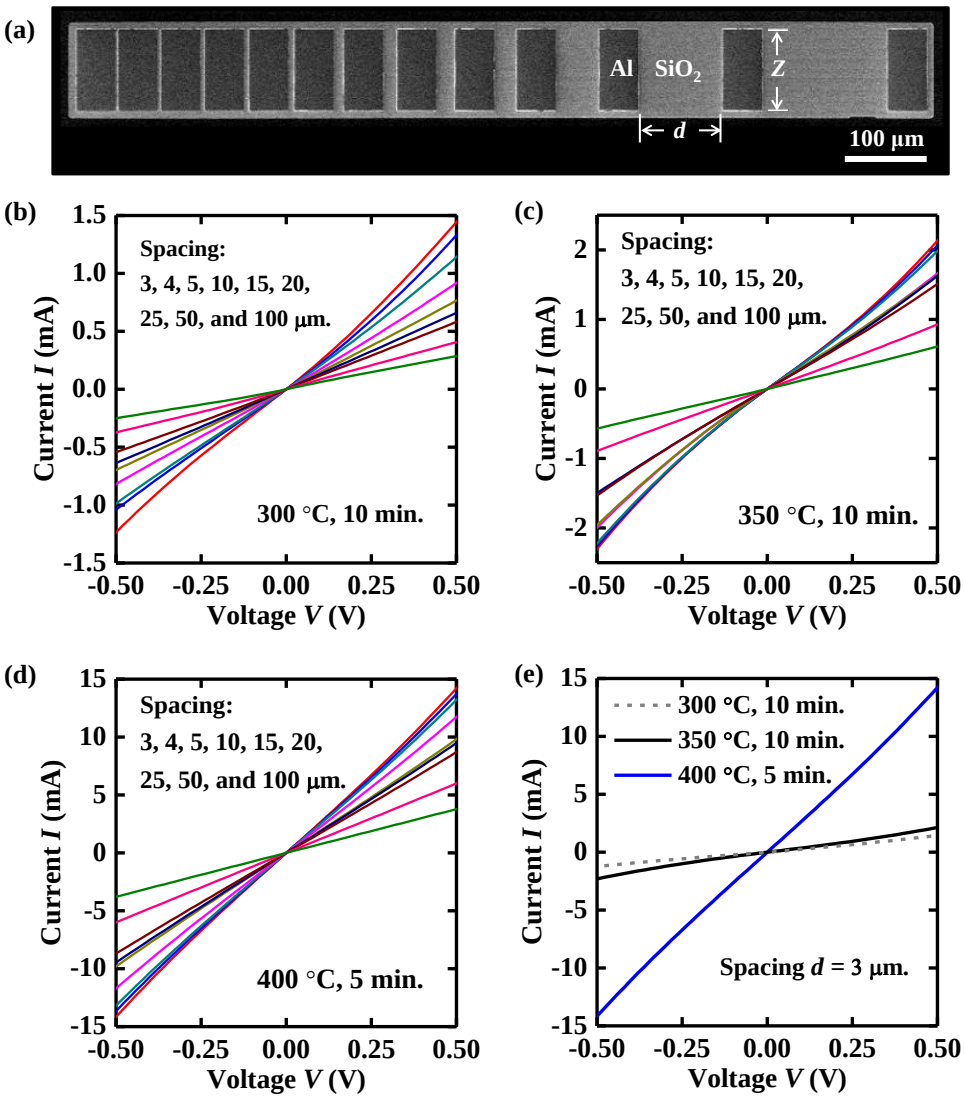


Fig. 5.3. (a) Top-view SEM image of the fabricated TLM test structure. Z is 100 µm; d varies from 3 µm to 100 µm. I – V characteristics of TLM test structures with various contact spacings formed on the n^+-$Ge_{1-x}Sn_x$ regions activated using post-implant RTA at (b) 300 °C for 10 minutes, (c) 350 °C for 10 minutes, and (d) 400 °C for 5 minutes. (e) Comparison of I – V curves of TLM test structures with a given spacing of 3 µm for the three splits. The TLM test structures activated for 10 minutes at 300 °C and 350 °C show non-ohmic behavior. On the other hand, the sample activated at 400 °C for 5 minutes demonstrates a good ohmic contact between Al and n^+-$Ge_{1-x}Sn_x$.

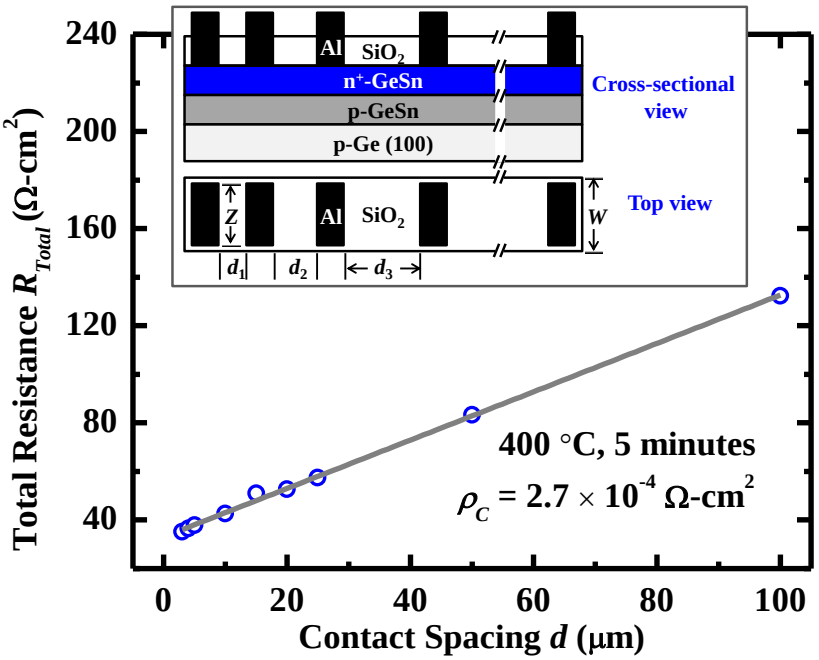


Fig. 5.4. R_{Total} versus d obtained from TLM test structure formed by post-implant annealing at 400 °C for 5 minutes. The inset image shows the schematic of a TLM test structure in cross-sectional view and top view. ρ_C of 2.7 × 10 $^{-4}$ Ω-cm^2 is obtained.

P SIMS depth profile of the as-implanted sample, and P SIMS and SRP depth profiles of the sample after activation at 400 °C for 5 minutes are shown in Fig. 5.5. The projected range of P^+ implant R_P in the as-implanted $Ge_{1-x}Sn_x$ is 16 nm. Low thermal budget is preferred to minimize dopant diffusion in this work. Negligible phosphorus diffusion is achieved during RTA at 400 °C, indicating the potential for shallow junction formation. The sample activated at 400 °C achieves a maximum active dopant concentration of 2.1 × 10^{19} cm^{-3}. Although SIMS shows phosphorus concentration near the sample surface can obtain 2 × 10^{20} cm^{-3} after activation at 400 °C, only 10% of phosphorus atoms are electrically active in $Ge_{1-x}Sn_x$.

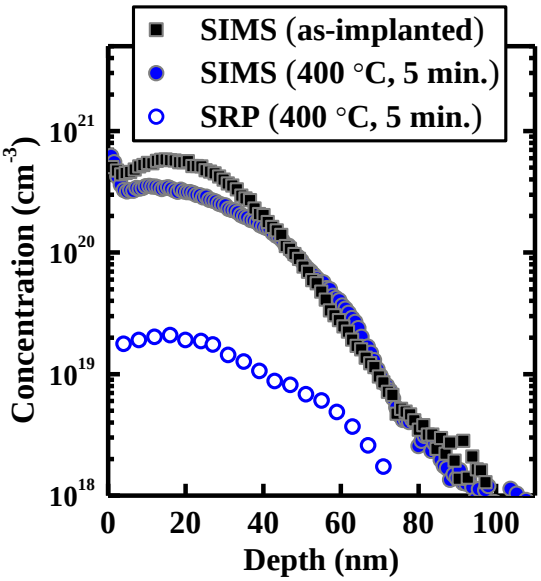


Fig. 5.5. P SIMS depth profile of the as-implanted sample, and P SIMS and SRP depth profiles of the sample after dopant activation at 400 °C for 5 minutes. Annealing at 400 °C for 5 minutes causes negligible P diffusion and achieves a maximum active electron concentration of 2.1×10^{19} cm^{-3}. The SIMS and SRP were performed as external service jobs at IMRE and Evans Analytical Group, Sunnyvale, California, USA, respectively.

Fig. 5.6(a) shows the $I - V$ characteristics of $Ge_{1-x}Sn_x$ n^+/p junction diodes formed by post-implant anneals at 300 °C for 10 minutes, 350 °C for 10 minutes, and 400 °C for 5 minutes, as well as the as-implanted sample without dopant activation. Forward current $I_{forward}$ in the series-resistance-limited regime ($V = -1.0$ V) increases and reverse current $I_{reverse}$ decreases monotonically as the activation temperature increases. A good rectifying diode was demonstrated using dopant activation temperature at 400 °C with the highest $I_{forward}$ and the lowest $I_{reverse}$.

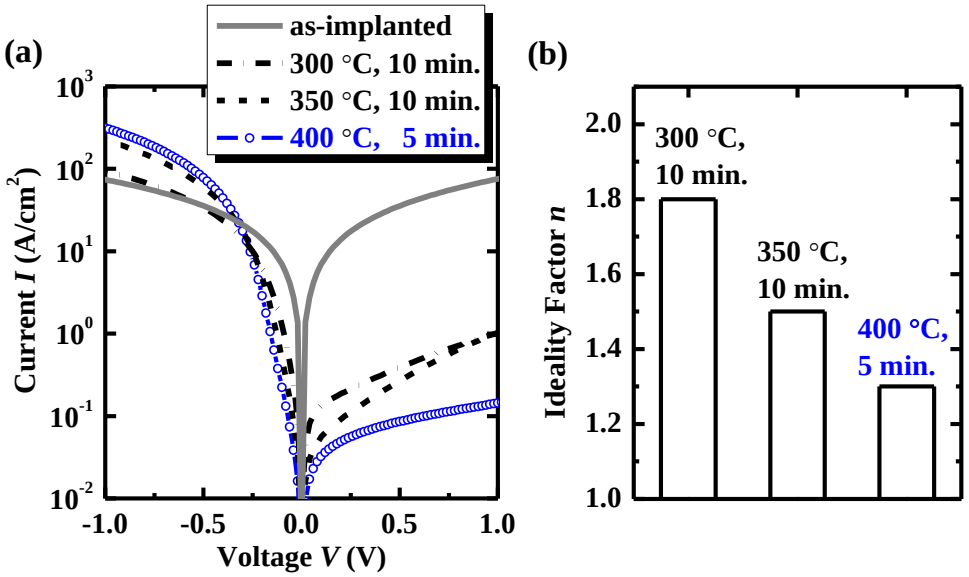


Fig. 5.6. (a) $I - V$ characteristics of $Ge_{1-x}Sn_x$ n^+/p junction diodes formed by annealing at 300 °C for 10 minutes, 350 °C for 10 minutes, and 400 °C for 5 minutes, as well as the as-implanted sample without dopant activation. (b) Comparison of n for n^+/p diodes activated by various annealing conditions. The diode formed by annealing at 400 °C for 5 minutes demonstrates the highest $I_{forward}$, the lowest $I_{reverse}$, and the smallest n.

The forward bias current density of an n^+/p junction in the non-series-resistance-limited regime J_F can be approximated by the sum of the electron diffusion current density in the p-side J_n and the recombination-current density J_{re} and is given by [200]

$$J_F = J_n + J_{re} = q\sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A}\exp\left(\frac{qV}{kT}\right) + \sqrt{\frac{\pi}{2}}\frac{kTn_i}{\tau_n\xi_o}\exp\left(\frac{qV}{2kT}\right), \tag{5.1}$$

where q is the elementary charge, D_n is the diffusion coefficient for electrons, τ_n is the carrier lifetime for electrons, n_i is the intrinsic carrier concentration, N_A is the acceptor impurity concentration, k is the Boltzmann constant, T is the temperature, and ξ_o is the electric field at the location of maximum recombination.

J_F is experimentally proportional to $\exp\left(\frac{qV}{nkT}\right)$, where n is the ideality factor of a diode. n equals 1 when J_n dominates, and n equals 2 when J_{re}

dominates. When both current densities are comparable, n has a value between 1 and 2. Comparison of ideality factor for $Ge_{1-x}Sn_x$ n^+/p diodes activated by different annealing conditions is shown in Fig. 5.6(b). According to Equation 5.1, the relatively high n of $Ge_{1-x}Sn_x$ diodes should be attributed to the low τ_n, due to not only the unrecovered implantation-induced defects, but also the defects because of low-temperature epitaxial growth of $Ge_{1-x}Sn_x$ on lattice-mismatched Ge substrate. Although n decreases as the dopant activation temperature increases, it should be noted the sample activated at 400 °C still has a relatively high n (1.3).

5.3.3 Comparison of $Ge_{1-x}Sn_x$ and Ge n^+/p Diodes

Fig. 5.7(a) shows $I - V$ characteristics of the $Ge_{1-x}Sn_x$ and Ge n^+/p diodes formed under various dopant activation conditions. A high $I_{forward}$ of 320 A/cm^2 at − 1 V is achieved for the $Ge_{1-x}Sn_x$ diode activated at 400 °C for 5 minutes, which is four times higher than that of the Ge control sample activated at 700 °C for 30 s and much higher than that of the Ge control sample activated at 400 °C for 5 minutes.

The $Ge_{1-x}Sn_x$ diode formed at 400 °C shows a higher $I_{reverse}$, compared with the Ge diodes. This is attributed to the following factors: 1) reduced band gap E_G in $Ge_{1-x}Sn_x$; 2) lower p-type doping concentration in the $Ge_{1-x}Sn_x$ epitaxial layer than in the Ge substrate; and 3) higher defect density in the epitaxial $Ge_{1-x}Sn_x$ film (due to low-temperature growth) than in the Ge substrate. Considering the compressive strain effect in $Ge_{0.976}Sn_{0.024}$ grown on Ge [48],[149], E_G of $Ge_{0.976}Sn_{0.024}$ is ~50 meV lower than that of relaxed Ge. In addition, the $Ge_{1-x}Sn_x$ has a p-type doping concentration of 5×10^{16} cm^{-3}, which is lower than that of the

Ge substrate (5×10^{17} cm^{-3}). A combined effect of the reduced E_G and the lower p-type doping concentration in $Ge_{1-x}Sn_x$ leads to 1.8 orders of magnitude higher diode current in the exponential region compared with the Ge control. In the reverse bias, the difference in the leakage current of $Ge_{1-x}Sn_x$ and Ge diodes is larger (2.9 orders of magnitude), of which 1.1 orders of magnitude should be attributed to the higher defect density in the $Ge_{1-x}Sn_x$.

$Ge_{1-x}Sn_x$ p-i-n photodetectors usually have more than 1 order of magnitude higher dark current I_{Dark} than the Ge control, possibly due to much higher generation-current density associated with recombination-generation centers within the depletion region as reported in Refs. [201] and [202]. I_{Dark} is the reverse leakage current that flows through the photodiode when no photons are entering the device, which is referred to as $I_{reverse}$ in diodes in this work [203].

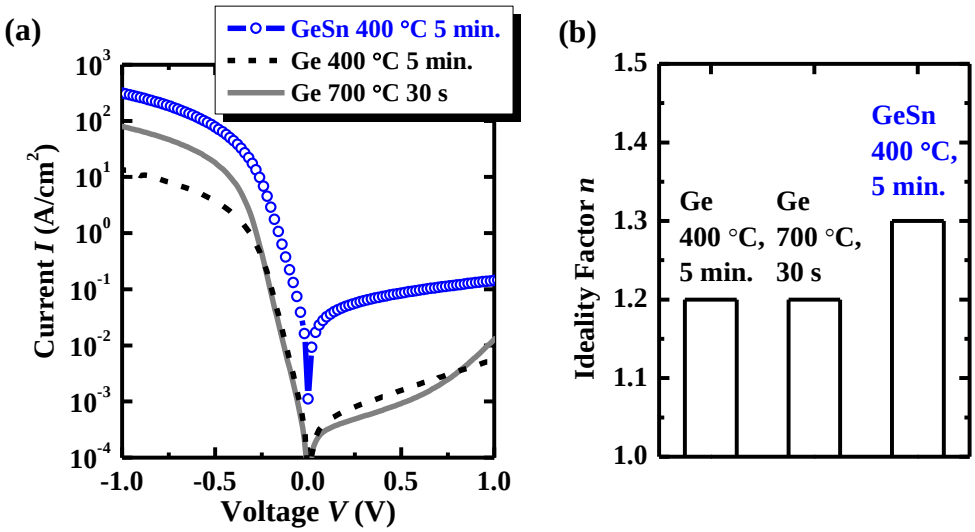


Fig. 5.7. (a) $I - V$ characteristics of a $Ge_{1-x}Sn_x$ n^+/p junction diode formed by post-implant annealing at 400 °C for 5 minutes, a Ge n^+/p junction diode formed by annealing at 400 °C for 5 minutes, and a Ge n^+/p junction diode formed by annealing at 700 °C for 30 s. (b) n of the n^+/p diodes showing in (a).

Fig. 5.7(b) shows the ideality factor of the $Ge_{1-x}Sn_x$ n^+/p diode activated at 400 °C is 1.3, which is higher than that of Ge diode activated at 400 °C or 700 °C. According to Equation 5.1, a smaller τ_n due to the higher defect density in $Ge_{1-x}Sn_x$ than in Ge could result in a higher n.

5.3.4 Discussion

Technology computer aided design (TCAD) simulation of the Al-contacted $Ge_{1-x}Sn_x$ n^+/p junction on Ge substrate was performed to solve Poisson's equation and the carrier continuity equations using a 2D device simulator Taurus Medici [204]. The specified physical models used in this simulation include the concentration-dependent mobility model, the parallel field mobility model, the Schottky barrier tunneling model, the Shockley-Read-Hall (SRH) recombination model, and the Auger recombination model. Fig. 5.8(a) depicts the $Ge_{1-x}Sn_x$ n^+/p junction on p-type Ge substrate with detailed parameters used for simulation. The thickness values of the Al, n^+-$Ge_{1-x}Sn_x$, p-$Ge_{1-x}Sn_x$ and p-Ge layers are 100 nm, 50 nm, 150 nm, and 10 µm, respectively. The width of the structure is 2 µm. The doping concentration of p-$Ge_{1-x}Sn_x$ and p-Ge are 5×10^{16} cm^{-3} and 5×10^{17} cm^{-3}, respectively. The doping concentration of n^+-$Ge_{1-x}Sn_x$ is 5×10^{18} cm^{-3}, 2×10^{19} cm^{-3}, 5×10^{19} cm^{-3} or 1×10^{20} cm^{-3}. The doped regions are uniformly doped for simplicity. The metal is connected to n^+-$Ge_{1-x}Sn_x$ with a Schottky barrier height of 0.58 eV [162],[198].

Fig. 5.8(b) shows $I - V$ characteristics of the $Ge_{1-x}Sn_x$ n^+/p diodes with various doping concentrations in n^+-$Ge_{1-x}Sn_x$ region. $I_{forward}$ increases monotonically with increasing doping concentration in n^+-$Ge_{1-x}Sn_x$ layer. Energy

band diagrams having an concentration of 2×10^{19} cm^{-3} (top) or 5×10^{18} cm^{-3} (bottom) of highly doped n-type $Ge_{1-x}Sn_x$ are shown in Fig. 5.9(a). Parts of the two band diagram curves (depth from 95 to 125 nm) are superimposed in Fig. 5.9(b), showing an obvious difference in the barrier width for electrons to tunnel. In addition, the more heavily doped semiconductor should be more conductive. Therefore, the more heavily doped split should have a lower series resistance of the diode, due to a lower contact resistance between Al and n^+-$Ge_{1-x}Sn_x$ because of a shallower barrier, and a lower resistance of n^+-$Ge_{1-x}Sn_x$ region. This leads to the enhancement of the forward bias current as shown in Fig. 5.8(b).

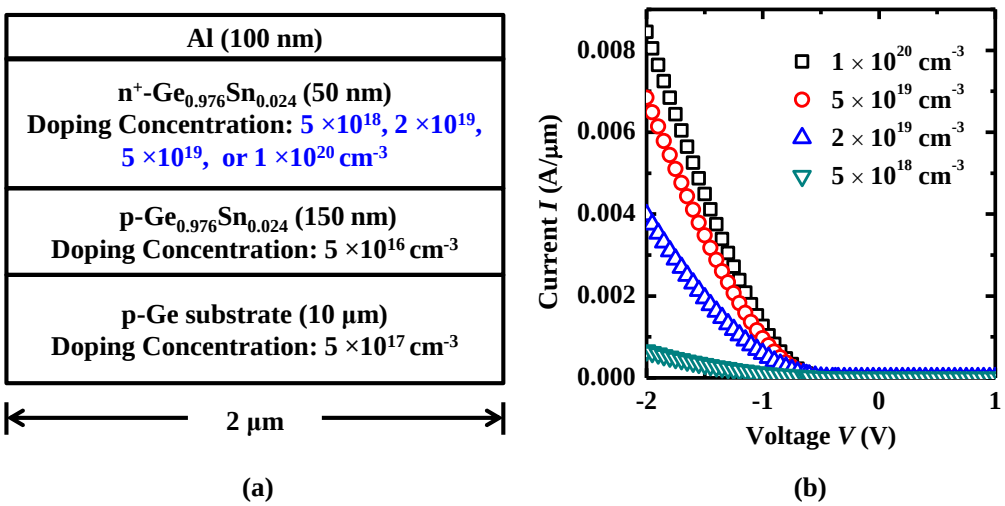


Fig. 5.8. (a) $Ge_{1-x}Sn_x$ n^+/p diode on p-Ge substrate used for simulation. Detailed parameters used in this simulation are shown. (b) $I_{forward}$ of $Ge_{1-x}Sn_x$ n^+/p diode increases monotonically with increasing doping concentration in n^+-$Ge_{1-x}Sn_x$ layer.

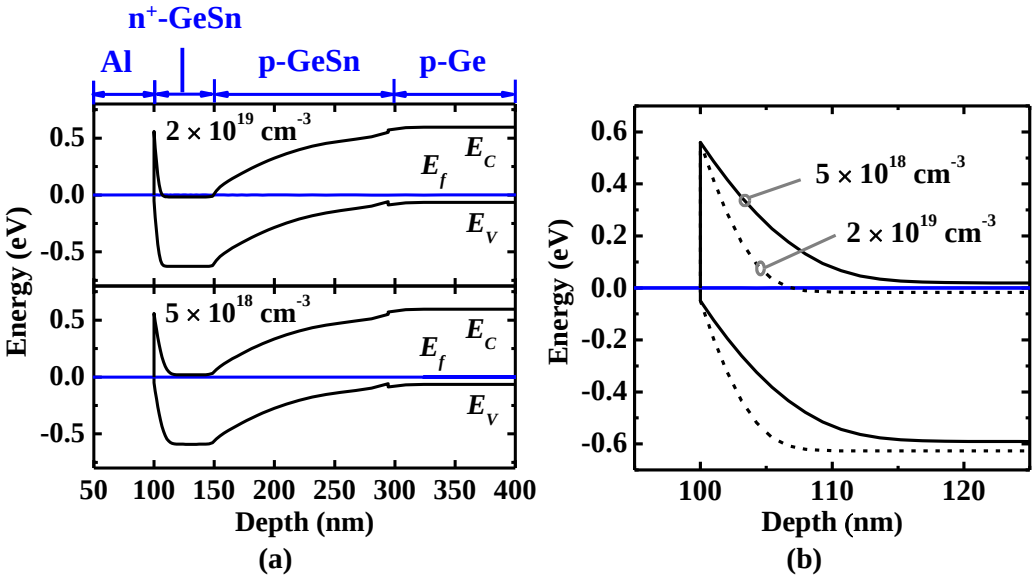


Fig. 5.9. (a) Energy band diagrams of a $Ge_{1-x}Sn_x$ n^+/p structure on Ge substrate with uniform dopant concentrations of (top) 2×10^{19} cm^{-3} or (bottom) 5×10^{18} cm^{-3} in the n^+-$Ge_{1-x}Sn_x$ region, with an Al contact to n^+-$Ge_{1-x}Sn_x$. (b) Superimposing the two curves in (a), highlighting the barrier width narrowing due to the higher doping concentration in the n^+-$Ge_{1-x}Sn_x$ region.

The combined effect of barrier width narrowing and improved conduction of n^+ region for the fabricated $Ge_{1-x}Sn_x$ diode formed by RTA at 400 °C with the most heavily doped n^+ region results in the lowest series resistance of the diode, which should be the reason that the diode formed by RTA at 400 °C achieves the highest $I_{forward}$ among the $Ge_{1-x}Sn_x$ diodes as shown in Fig. 5.6(a). Likewise, this effect also leads to the enhancement in $I_{forward}$ of the $Ge_{1-x}Sn_x$ diode as compared with Ge diodes [Fig. 5.7(a)].

The low activation of n-type dopants in Ge below 450 °C is mainly attributed to vacancies in Ge. The maximum activation level is closely linked to the vacancy concentration [117],[205],[206]. Although recrystallization of Ge after a high-dose P^+ implant occurs below 400 °C, annealing up to 450 °C should be needed for removal of acceptor-like defects (associated with vacancy in the Ge lattice) induced in Ge by implant [117],[205]. A large number of non-activated P

atoms in Ge are incorporated in the Ge lattice as dopant-vacancy inactive clusters [A_nV_m] (A ∈ {P, As, Sb}) [117],[205],[206]. High-temperature activation (> 450 °C) is therefore required to annihilate the residual defects, which are thermally unstable [207]. Therefore, the higher P activation in the $Ge_{1-x}Sn_x$ sample annealed at 400 °C could be due to trapping of vacancies in Ge by the incorporated Sn atoms, leading to a low concentration of the inactive P_nV_m [208].

5.4 Self-Crystallization and Improved Dopant Activation by Hot P^+ Implant in $Ge_{0.976}Sn_{0.024}$

5.4.1 Experimental Details

Fig. 5.10(a) depicts a schematic of the hot P^+ implant setup. The $Ge_{0.976}Sn_{0.024}$ samples were put on 12-inch Si carrying wafers during P^+ implant. The carrying wafer was then loaded into the ion implanter chamber and placed on a platen that can be heated by a heater. Fig. 5.10(b) shows platen temperature versus process time during the hot P^+ implant process. The platen temperature was set to 400 °C during hot P^+ implant. After the platen temperature was stable, P^+ implant was performed at an elevated temperature at energy of 20 keV and a dose of 2×10^{15} cm^{-2}. The temperature of the $Ge_{1-x}Sn_x$ samples, which cannot be measured directly, should be close to 400 °C during hot P^+ implant. After that, the wafers were moved from the platen to the load lock for cooling. P^+ implant at room temperature (~20 °C) using the same implant energy and dose was performed as the control. The implant was done by our collaborators at Applied Materials – Varian Semiconductor Equipment, Gloucester, Massachusetts, USA.

P depth profiles of the implanted samples with or without RTA were examined by SIMS. XTEM was performed to investigate the damage induced by implant and the possible residual disorder after thermal treatment. TLM test structures were fabricated to extract ρ_C and sheet resistance R_{Sh}. Diodes were fabricated to investigate the electrical characteristics of the n^+/p junction. The fabrication of TLM test structures and diodes were done by Dr. Pengfei Guo, Dr. Xiao Gong and Mr. Cheng Guo in our group, which are similar to the devices that have been discussed in Section 5.3.1. To achieve an excellent contact between the

diode samples and the stage of the probe station, 200 nm of nickel (Ni) was deposited on the back of the diode samples after removing the native oxides by a fluorine-based plasma etching process. This step was done by Dr. Bin Liu in our group.

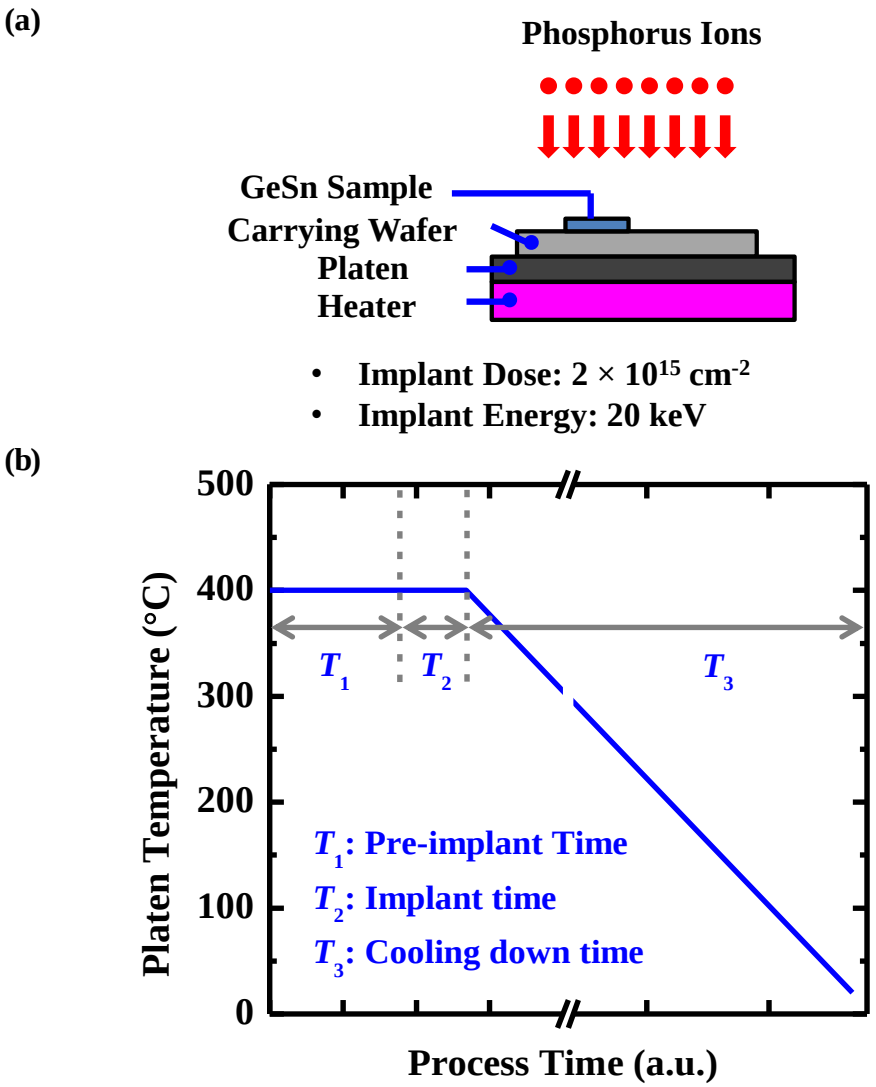


Fig. 5.10. (a) Schematic of the hot P^+ implant setup. P^+ implant performed at energy of 20 keV and a dose of 2×10^{15} cm^{-2}. (b) Platen temperature as a function of process time during the P^+ hot implant process. The implant was done by our collaborators at Applied Materials – Varian Semiconductor Equipment, Gloucester, Massachusetts, USA.

5.4.2 Material Characterization

Fig. 5.11(a) and Fig. 5.12(a) show the XTEM images of the as-implanted RT P^+ sample and the as-implanted hot P^+ sample, respectively. RT P^+ implant amorphizes the top 50 nm of the $Ge_{1-x}Sn_x$ sample, as the implanted dose of 2×10^{15} cm^{-2} is above the amorphization threshold dose in Ge [209]. The amorphous/crystalline (a/c) interface is relatively smooth after the high-dose implant [210]. On the contrary, for the sample implanted at 400 °C, the $Ge_{1-x}Sn_x$ lattice remains single-crystalline, due to the self-crystallization of $Ge_{1-x}Sn_x$ during implant. However, a defect band of ~60 nm wide was observed at ~40 nm from the surface.

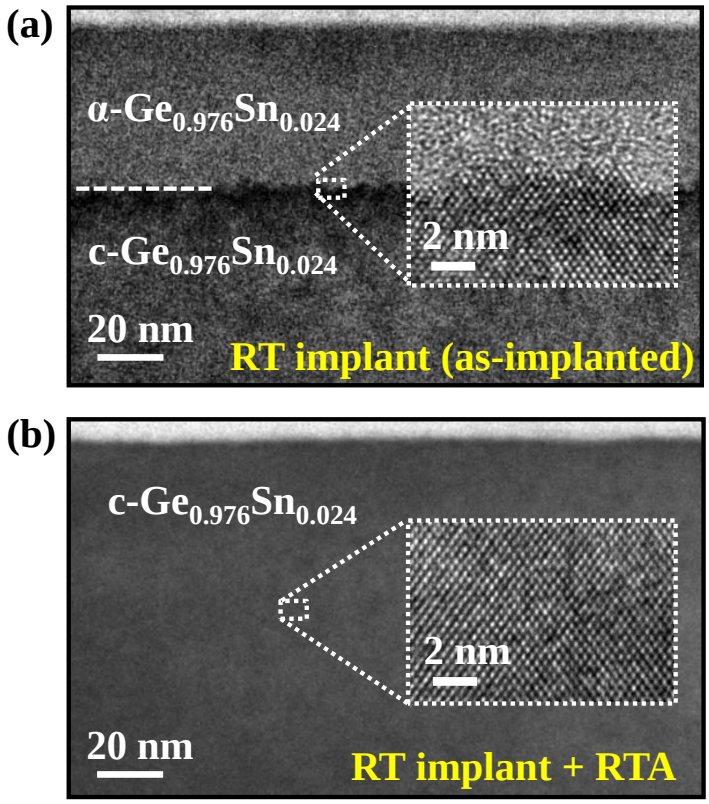


Fig. 5.11. XTEM images of (a) the as-implanted RT sample and (b) the sample after post-implant annealing at 450 °C for 3 minutes. RT P^+ implant amorphizes the top 50 nm of the sample. After SPE at 450 °C, the $Ge_{1-x}Sn_x$ film converts to single-crystalline without any observable defect. The TEM images were taken by Dr. Qian Zhou in our group.

The XTEM image in Fig. 5.11(b) shows that the RT-implanted $Ge_{1-x}Sn_x$ film converts to single-crystalline without observable defects, after 3 minutes of solid-phase epitaxy (SPE) at 450 °C. Fig. 5.12 (b) shows the XTEM image of the hot-implanted sample after annealing at 450 °C for 3 minutes. The left inset HRTEM image shows the lattice fringes near the surface. However, interstitial-type extended defects are observed in the right inset HRTEM image, which are dislocation loops on {111} planes as shown in the right inset HRTEM image [211].

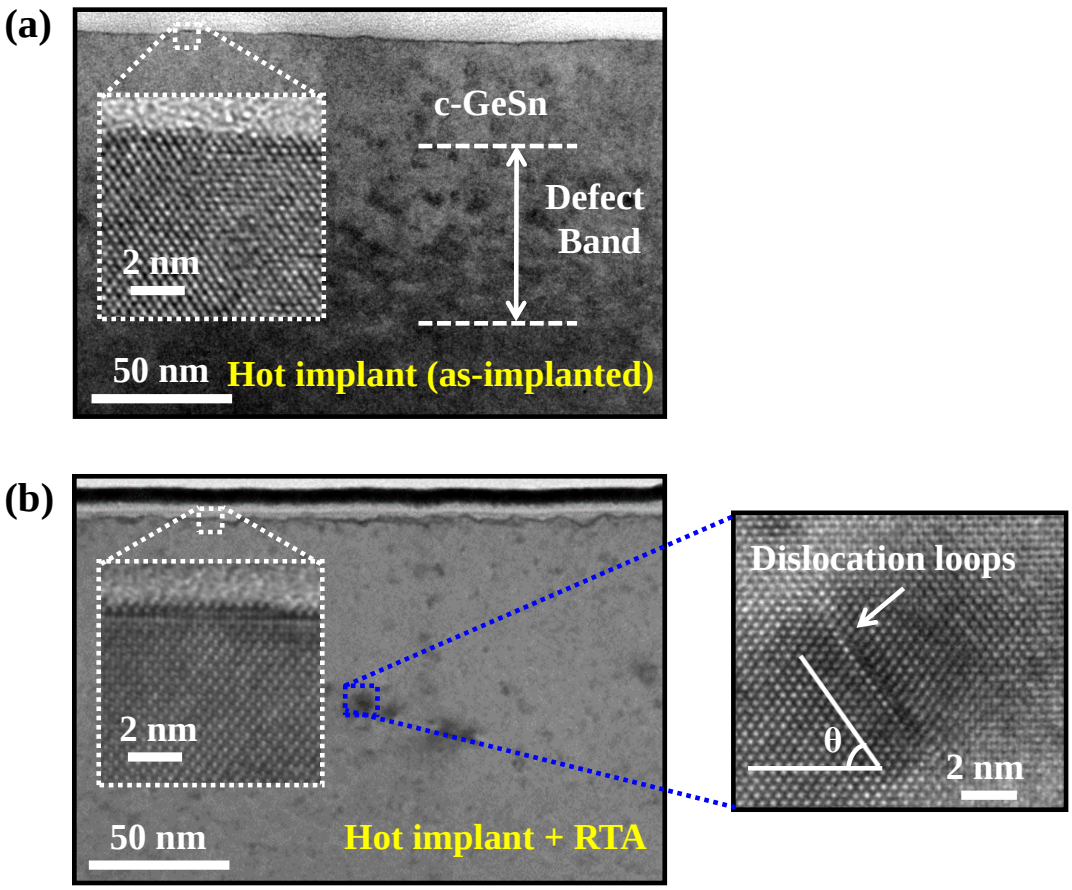


Fig. 5.12. (a) XTEM image of the as-implanted hot P^+ sample. The as-implanted hot-implanted sample remains single-crystalline, and a defect band is observed. (b) XTEM image of the sample implanted at 400 °C and annealed at 450 °C for 3 minutes. The left inset HRTEM image shows the lattice fringes near the surface, while the HRTEM image in the right inset shows a dislocation loop on the (111) plane. The TEM in (a) was done by Dr. Qian Zhou in our group; the TEM in (b) was performed as an external service job at IMRE.

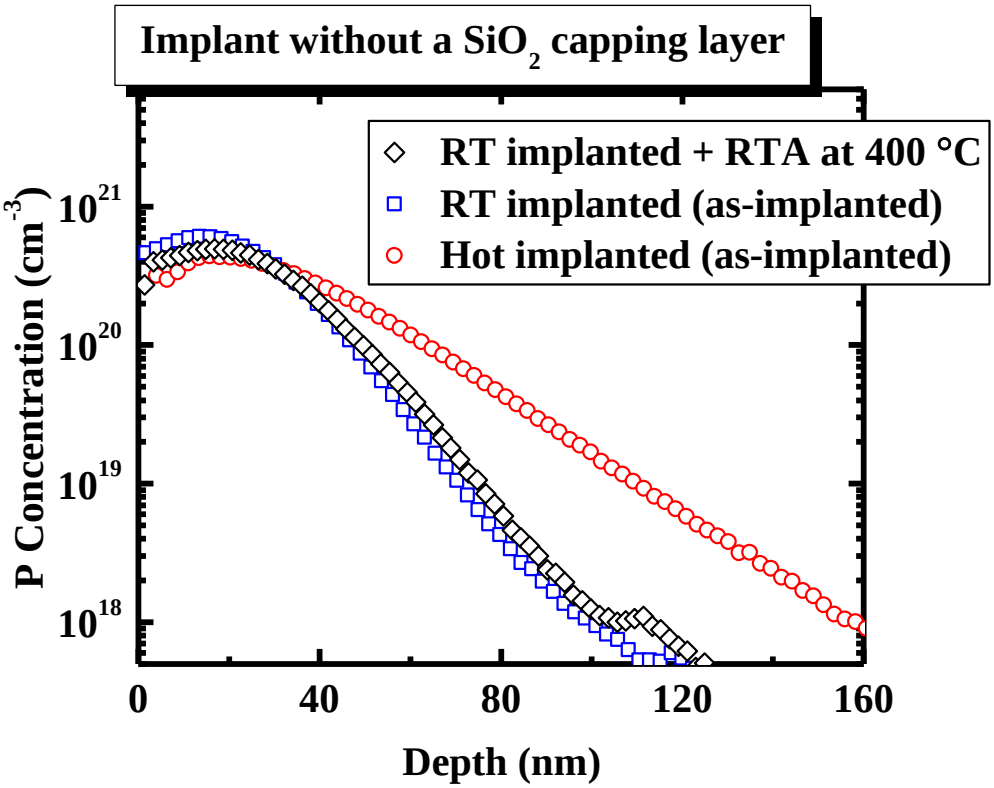


Fig. 5.13. P SIMS depth profiles for the samples right after implant at 20 °C and 400 °C, and the sample implanted at 20 °C after post-implant RTA at 400 °C. The hot-implanted sample has a deeper junction as compared with the one implanted at room termperature, due to the lack of an amorphous layer at the surface. In addition, RTA at 400 °C for 3 minutes causes negligible P diffusion. The SIMS was done by Dr. Sin Leng Lim at the Department of Physics, NUS.

Fig. 5.13 depicts P SIMS depth profiles for as-implanted samples implanted at 20 °C and 400 °C. The P SIMS depth profile for a sample implanted at room temperature followed by annealing at 400 °C for 3 minutes is included to confirm that the 400 °C RTA does not cause obvious P diffusion. The hot-implanted sample has a deeper junction due to the absence of an amorphous layer during implant, leading to more severe channeling effect. A shallower junction can be achieved by reducing the implant energy, therefore channeling is not a serious problem.

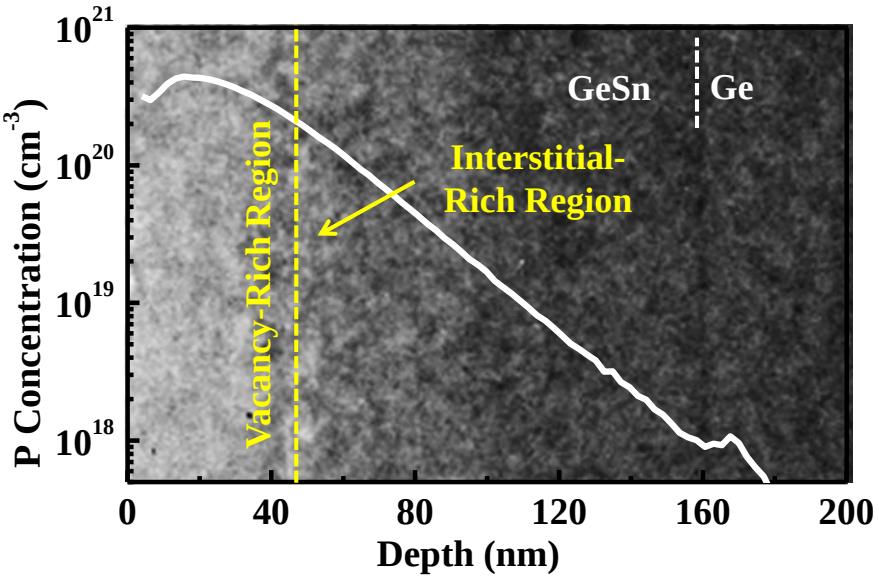


Fig. 5.14. P SMIS depth profile of the as-implanted hot P^+ sample in Fig. 5.13 superimposed on the XTEM image of the same sample. A vacancy-rich region and a interstitial-rich region are expected to exist.

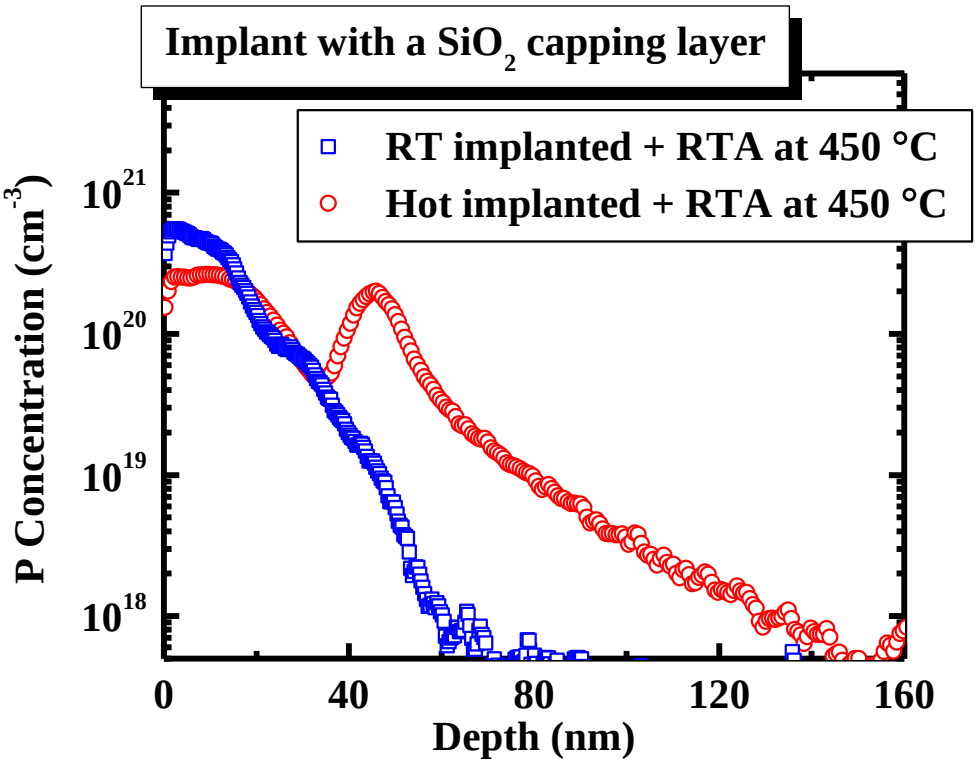


Fig. 5.15. Phosphorus depth profiles for samples implanted at 20 °C or 400 °C and annealed at 450 °C for 3 minutes. The SIMS was performed as an external service job at the IMRE.

Fig. 5.14 shows the P SIMS depth profile of the sample implanted at 400 °C in Fig. 5.13 superimposed on the XTEM image of the same sample. After hot P^+ implant, although there is no amorphization layer formed at the surface, the separation between interstitials and vacancies is expected to occur, leading to a vacancy-rich region towards the surface and a deeper interstitial-rich region in the bulk [212]-[213].

Fig. 5.15 shows P SIMS depth profiles for samples implanted at 20 °C and 400 °C and annealed at 450 °C for 3 minutes. The presence of an additional P peak deeper in the $Ge_{1-x}Sn_x$ after annealing at 450 °C for 3 minutes could indicate the presence of a vacancy-rich region and an interstitial-rich region in the single-crystalline $Ge_{1-x}Sn_x$ film, as vacancies can enhance P diffusion in the $Ge_{1-x}Sn_x$ matrix while a large number of interstitials act as a sink for vacancies and can suppress P diffusion [207],[214]-[215]. It should be noted that there is a 10-nm-thick SiO_2 capping layer for the samples during implant as shown in Fig. 5.15, which leads to a slight difference of the junction depth compared with the samples without SiO_2 capping layer during implant as shown in Figs. 5.13 and 5.14.

5.4.3 Electrical Characterization

Fig. 5.16 shows R_{total} versus d obtained from the TLM test strucute formed by implantation at 20 °C or 400 °C and annealing at 450 °C or 500 °C for 3 minutes. ρ_C and R_{Sh} are given by $\frac{R_C^2 \times Z}{Slope}$ and $Slope \times Z$, respectively. Fig. 5.17 shows that the samples implanted at 400 °C achieve lower (a) contact resistivity

between Al and n^+-$Ge_{1-x}Sn_x$ and (b) sheet resistance of n^+-$Ge_{1-x}Sn_x$ for both annealing temperatures, compared with the one implanted at 20 °C.

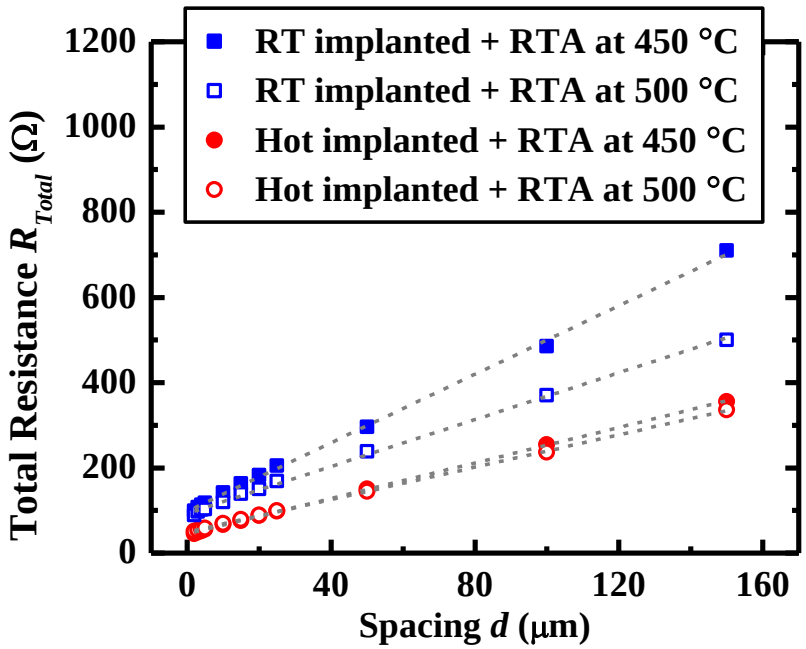


Fig. 5.16. R_{total} versus d obtained from TLM test structures formed by P^+ implant at various implant and annealing conditions.

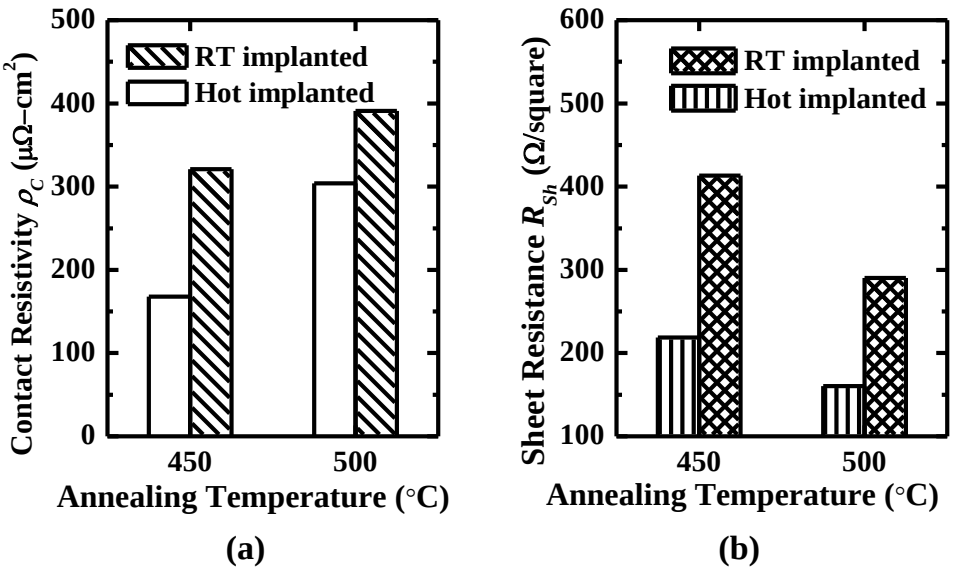


Fig. 5.17. After post-implant RTA at 450 °C or 500 °C for 3 minutes, the hot-implanted samples show both (a) lower ρ_C and (b) lower R_{Sh}, as compared with the RT-implanted samples.

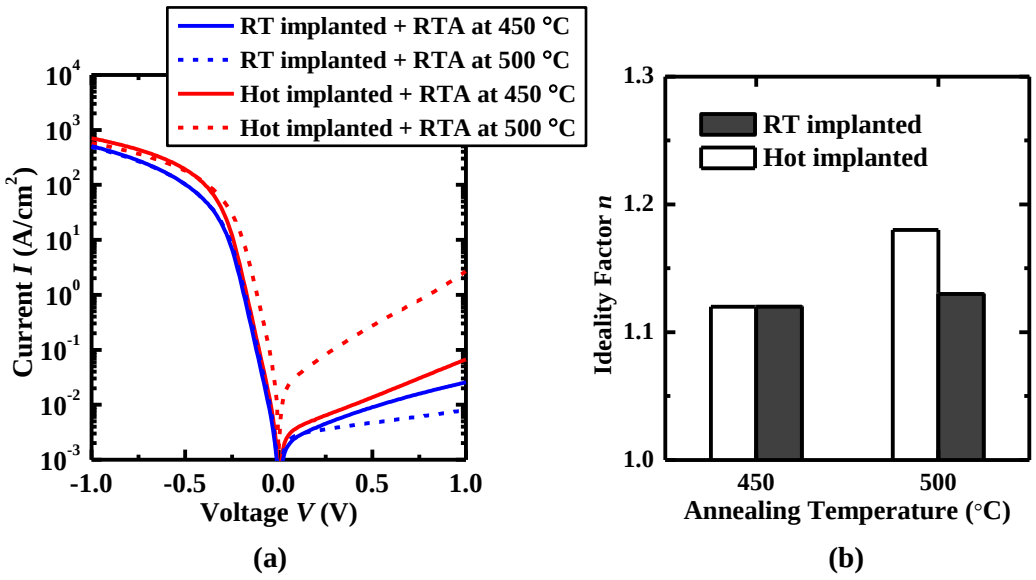


Fig. 5.18. (a) $I - V$ characteristics of n^+/p diodes formed by P^+ implant at various implant and annealing conditions. (b) The diodes formed by implantation at 20 °C or 400 °C and annealing for 3 minutes at 450 °C or 500 °C gives similar n.

Fig. 5.18(a) shows the $I - V$ characteristics of n^+/p diodes formed by implantation at 20 °C or 400 °C, followed by annealing at 450 °C or 500 °C for 3 minutes. Fig. 5.18(b) shows that the diodes formed by implantation at 20 °C or 400 °C and annealing for 3 minutes at 450 °C or 500 °C gives similar ideality factor, which is lower than 1.2. Paticularly, the RT-implanted sample activated at 450 °C or 500 °C shows lower n than that formed by implantation at 20 °C and annealing at 300 °C for 10 minutes (1.8), 350 °C for 10 minutes (1.5) or 400 °C for 5 minutes (1.3) as shown in Fig. 5.6(b). This indicates annealing at higher temperature (450 °C or 500 °C) could further improve the material qualty of the depletion region by reparing the defects due to either RT implantation or low-temperature growth process as dicussed in Section 5.3.3.

Fig. 5.19 shows the cumulative probability plots of (a) $I_{forward}$ and (b) the forward/reverse current ratio $I_{forward}/I_{reverse}$ of the n^+/p diodes, respectively. $I_{forward}$ and $I_{reverse}$ are extracted at biases of -1 V and 1 V, respectively. The sample

implanted at 400 °C and annealed at 450 °C gives the highest median $I_{forward}$, as a result of having the lowest R_S. Except for the sample implanted at 400 °C and annealed at 500 °C for 3 minutes, the rest of the splits show good rectifying behavior with the median $I_{forward}/I_{reverse}$ of more than 10^4. The degraded rectifying behavior of the diodes formed by hot P^+ implant is due to higher $I_{reverse}$, compared with those formed by RT implant. This could be attributed to the more defects located at the depletion region of the hot-implanted samples [Fig. 5.12(b)] than that of the RT-implanted samples [Fig. 5.11(b)], after dopant activation.

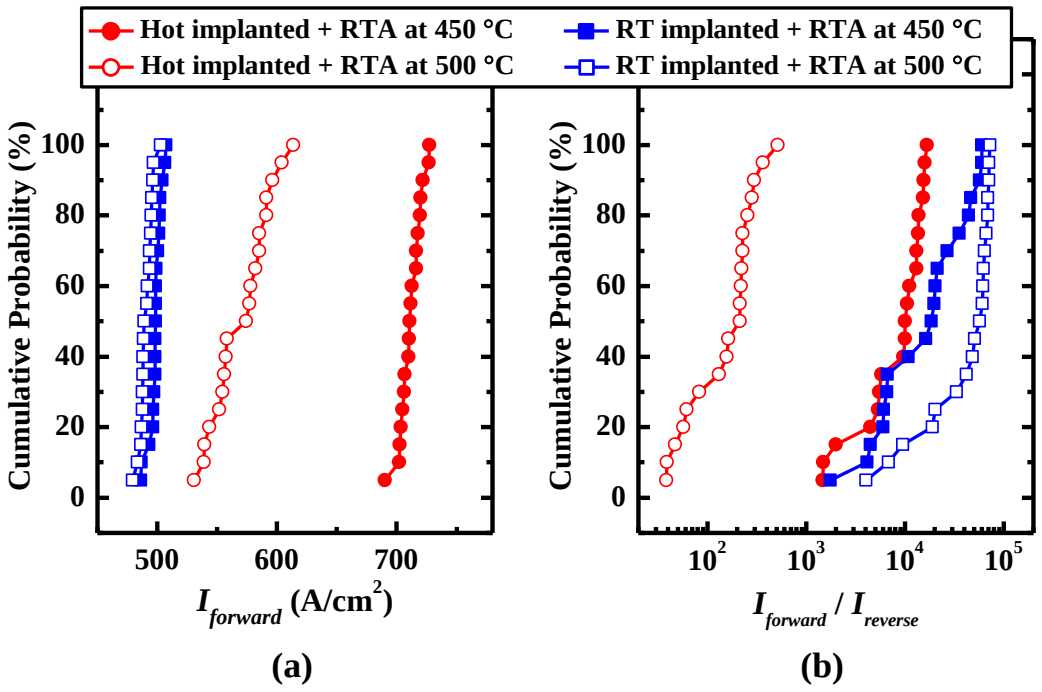


Fig. 5.19. (a) Cumulative probability plot shows that P^+ implant at 400 °C and annealed at 450 °C achieve the highest $I_{forward}$ at -1 V. (b) Cumulative probability plot shows most of the splits show good rectifying behavior with the median $I_{forward}/I_{reverse}$ of more than 10^4, except for the sample implanted at 400 °C and annealed at 500 °C for 3 minutes.

5.4.4 Discussion

For ohmic contacts between metal and highly doped semiconductor, current conduction is dominated by tunneling. ρ_C depends exponentially on the surface doping concentration N_S and the Φ_B, and is given by [216]

$$\rho_C \propto \exp\left(\frac{4\pi\phi_B}{qh}\sqrt{\frac{m^*\varepsilon_S}{N_S}}\right), \tag{5.2}$$

where h is the Planck constant, m^* is the effective mass of the carriers tunneling across the contact, ε_S is the dielectric constant of the semiconductor.

As E_f at the metal/$Ge_{1-x}Sn_x$ interface is pinned near E_V of $Ge_{1-x}Sn_x$ [162], all samples should have the same Φ_B. As the hot-implanted sample has lower ρ_C than the RT-implanted sample after post-implant RTA at 450 °C or 500 °C, the hot-implanted sample should have higher N_S, according to Equation 5.2. Besides, the hot-implanted sample has a lower total phosphorus concentration n_{Total} near the surface as shown in the P SIMS depth profiles for samples annealed at 450 °C (Fig. 5.15). Therefore, hot implant achieves higher N_S despite a lower n_{Total}, which indicates that it should have higher dopant activation rate given by N_S/n_{Total}. This result is important and consistent with the discovery of the improved P activation in Ge realized by hot implant compared to RT implant in Ref. [190]. M. A. Razali *et al.* claimed that hot P^+ implant in Ge can achieve low level of stable inactive P_nV_m (discussed in Section 5.3.4) and therefore good activation of P [190].

5.5 Summary

In this Chapter, a well-behaved $Ge_{0.976}Sn_{0.024}$ n^+/p junction diode was formed at a relatively low temperature of 400 °C for reduced dopant diffusion. The SRP analysis shows that a high concentration of P was achieved for P^+-implanted epitaxial $Ge_{1-x}Sn_x$ after dopant activation. Other than high carrier mobility, $Ge_{1-x}Sn_x$ alloy with a high P dopant concentration and low thermal budget for forming a shallow n^+/p junction is a promising candidate for future scaled high-mobility transistors.

In addition, hot P^+ implant was investigated on $Ge_{0.976}Sn_{0.024}$. Hot P^+ implant maintains the single-crystallinity of the $Ge_{1-x}Sn_x$ film during implant. After RTA at 450 °C for 3 minutes, the hot-implanted sample has a lower contact resistivity than the RT-implanted sample despite a lower total phosphorus concentration at the surface. Higher P dopant activation, together with a self-crystalline process, makes hot P^+ implant a promising technique in future $Ge_{1-x}Sn_x$ transistor applications.

Chapter 6

Conclusion and Future Work

6.1 Conclusion and Contributions of This Thesis

As continuous scaling of silicon (Si) metal-oxide-semiconductor field-effect transistors (MOSFETs) for better speed performance currently faces significant challenges, novel technologies and device structures are required to further enhance the drive current of the MOSFETs at a reduced supply voltage. Exploring high-mobility channel materials such as germanium (Ge) and III-V compound semiconductors to replace Si is deemed as a solution to extend the complementary metal-oxide-semiconductor (CMOS) road map.

Germanium-tin ($Ge_{1-x}Sn_x$), which is predicted to have even higher carrier mobilities than Ge [48], could potentially be a promising alternative channel material. The motivation of this thesis is to address various technical challenges in realizing $Ge_{1-x}Sn_x$ channel MOSFETs as a candidate for the sub-10 nm technology node applications. In particular, a surface passivation technique for $Ge_{1-x}Sn_x$ p-MOSFETs has been investigated to fully exploit the benefits of its high hole mobility. Next, a thermally stable self-aligned source/drain (S/D) contact metallization scheme for $Ge_{1-x}Sn_x$ MOSFETs has been developed. Last, we work on achieving high n-type doping concentration for low S/D parasitic resistance $R_{S/D}$ of $Ge_{1-x}Sn_x$ n-MOSFETs. The major conclusion and contributions of this work are elucidated in this section.

6.1.1 $Ge_{1-x}Sn_x$ p-MOSFETs with $(NH_4)_2S$ Passivation

Ammonium sulfide [$(NH_4)_2S$] passivation for the gate stack of high-mobility $Ge_{0.958}Sn_{0.042}$ p-MOSFETs was explored in Chapter 3 [131]. High-quality single-crystalline $Ge_{0.958}Sn_{0.042}$ films were epitaxially grown on Ge (100) substrate by a solid source molecular beam epitaxy (MBE) system. Before gate dielectric deposition, $(NH_4)_2S$ passivation was done by treatment with $(NH_4)_2S$ aqueous solution (36%) for 10 minutes at 25 °C. The $(NH_4)_2S$-passivated $Ge_{0.958}Sn_{0.042}$ p-MOSFETs show decent transfer and output characteristics, and demonstrate a higher peak effective mobility in comparison with those of other (100)-oriented $Ge_{1-x}Sn_x$ p-MOSFETs reported so far [61]-[63],[91],[159]. This passivation technique, which is compatible with a high-*k* dielectric deposition process, is attractive to form high-quality gate stack to explore the full potential of $Ge_{1-x}Sn_x$ at future technology nodes.

6.1.2 Improving Thermal Stability of Ni(GeSn) by Incorporation of Pt

A thermally stable platinum (Pt) -incorporated stanogermanide metallization scheme for $Ge_{1-x}Sn_x$ transistors was investigated in Chapter 4 [176]. The incorporation of Pt improves the thermal robustness by suppressing agglomeration during the solid-state reaction between Ni and $Ge_{1-x}Sn_x$. The surface of $Ni/Ge_{1-x}Sn_x$ sample becomes rough after annealing at 450 °C observed by scanning electron microscopy (SEM) and atomic force microscopy (AFM), which is the cause of the sharp increase in sheet resistance from 450 to 500 °C. In contrast, SEM and AFM images show the surface of $NiPt/Ge_{1-x}Sn_x$ sample is still reasonably smooth even after annealing at 500 °C, which is also consistent with

the result of sheet resistance measurement. Only the Pt-incorporated stanogermanide film formed at 350 °C is still smooth after a second anneal at 500 °C for 60 s. This NiPt-based contact scheme is therefore more attractive than the pure Ni-based one for integration in high-performance $Ge_{1-x}Sn_x$ MOSFETs.

6.1.3 Towards Highly Doped N-type $Ge_{1-x}Sn_x$

Chapter 5 documents the efforts towards highly doped n-type $Ge_{1-x}Sn_x$ for low $R_{S/D}$ of $Ge_{1-x}Sn_x$ n-MOSFETs. We first investigated $Ge_{0.976}Sn_{0.024}$ n^+/p junction formation using phosphorus ion (P^+) implant without heating the substrate during the implant [189]. Various rapid thermal annealing (RTA) temperatures were investigated to activate the dopants. Activation temperature as low as 400 °C is demonstrated to obtain active doping concentration of 2.1×10^{19} cm^{-3} for P^+-implanted $Ge_{0.976}Sn_{0.024}$. $Ge_{1-x}Sn_x$ alloy with a high dopant concentration and low thermal budget for forming a shallow n^+/p junction is a promising candidate for future scaled high-mobility transistors.

In addition, we investigated the effect of P^+ implant temperature on the material properties of epitaxial $Ge_{1-x}Sn_x$ alloy and the electrical characteristics of the transfer length method (TLM) test structures and n^+/p junction diodes [195]. Implant at elevated temperature of 400 °C was explored to maintain the single-crystallinity of $Ge_{0.976}Sn_{0.024}$ during implant and achieve a lower contact resistivity after activation at 450 °C as compared with the room-temperature implant. Higher phosphorus dopant activation, together with a self-crystalline process, makes hot implant a promising technique in future $Ge_{1-x}Sn_x$ transistor applications.

6.2 Future Directions

In summary, this thesis has developed several exploratory technology options to address various challenges in high-mobility $Ge_{1-x}Sn_x$ MOSFETs. Preliminary assessment of the various technology options on gate stack formation and source/drain engineering show promising results for realizing high-performance $Ge_{1-x}Sn_x$ MOSFETs. Moving forward, further exploration and more thorough analysis has to be dealt with for possible adoption in future CMOS technology nodes and high-volume manufacturing. In addition, more related studies need to done to further open up new research and development opportunities for $Ge_{1-x}Sn_x$ MOSFETs. Some of the suggestions for further directions are highlighted in this section.

6.2.1 Cost Effective Integration of $Ge_{1-x}Sn_x$ on Si Substrates

Given the maturity of Si manufacturing technology, it is very likely that Si will still be used for the overall substrate in mainstream manufacturing [217]. It is crucial to incorporate the less abundant and more expensive $Ge_{1-x}Sn_x$ on a large (e.g. 300 mm) Si wafer to reduce the considerable costs associated with developing non-Si bulk substrates. The aspect-ratio-trapping growth technique can be utilized for growing high-quality $Ge_{1-x}Sn_x$ on Si cost effectively for logic applications [42]-[44], [73]. This is, however, lacking in the literature. Furthermore, it has to be pointed out that there is no confinement of defects along the direction of the trench using the aspect-ratio-trapping technique, as the defect trapping at the oxide side walls is limited to one direction [73]. Further efforts also need to be devoted to solve this problem.

6.2.2 Surface Passivation for $Ge_{1-x}Sn_x$ p-MOSFETs

For further investigation on $(NH_4)_2S$-passivated $Ge_{1-x}Sn_x$ p-MOSFETs, an in-depth analysis of interface trap density energy distribution across the $Ge_{1-x}Sn_x$ band gap could be conducted by the frequency-dependent full conductance method [218]-[219]. In addition, alternative surface passivation techniques, which have been demonstrated to be promising for high-performance Ge p-MOSFETs, can also be explored for $Ge_{1-x}Sn_x$ p-MOSFETs, such as plasma post oxidation [165], high pressure oxidation [220], and passivation with indium aluminum phosphide [94].

6.2.3 Optimization of Pt Composition in Ni(GeSn) for $Ge_{1-x}Sn_x$ p-MOSFETs

The incorporation of Pt improves the thermal robustness of the stanogermanide as discussed in Chapter 4. As the molar ratio of Ni to Pt is ~3, the sheet resistance of the stanogermanide that is formed at 350 °C is higher than that of pure Ni(GeSn) due to the formation of high-resistive Pt_2Ge_3. Therefore, the Pt composition should be tuned. In addition, it is necessary to extract the contact resistance between the Pt-incorporated stanogermanide and p^+-$Ge_{1-x}Sn_x$, and a low contact resistance is desired. Furthermore, the optimized Pt-incorporated contact scheme should be integrated in $Ge_{1-x}Sn_x$ p-MOSFETs.

6.2.4 Realizing High-performance $Ge_{1-x}Sn_x$ n-MOSFETs

Although $Ge_{1-x}Sn_x$ n-MOSFETs have recently been demonstrated [92],[124],[125],[129], the drive current of the reported $Ge_{1-x}Sn_x$ n-MOSFETs is still low. There are still opportunities for further improving the performance of

$Ge_{1-x}Sn_x$ n-MOSFETs. First, it is critical to obtain low $R_{S/D}$ of $Ge_{1-x}Sn_x$ n-MOSFETs by achieving high doping concentration for low resistance S/D regions using the methods discussed in Chapter 5. In addition, more novel doping and/or activation techniques, such as S/D structure with *in situ* doping [119], laser annealing [121], and co-implantation [221], should be explored. Last, it is equally important to explore innovative gate stack formation technologies on $Ge_{1-x}Sn_x$ n-MOSFETs. The passivation using indium aluminum phosphide, which has been recently investigated on high-performance Ge n-MOSFETs [94], is one of the most promising technologies to explore.

6.2.5 Strain Techniques to Enhance the Hole Mobility of $Ge_{1-x}Sn_x$ P-MOSFETs

From the 90-nm technology node, strain engineering has been adopted as an important performance booster to significantly improve the effective carrier mobilities and therefore drive current of MOSFETs [8]. The simulation work done by X. Gong *et al.* [222] shows the induced uniaxial compressive strain results in reduced effective mass of $Ge_{1-x}Sn_x$ for the topmost valence band where holes primarily occupy. In addition, the uniaxial compressive strain increases the light-hole (LH) to heavy-hole (HH) band separation, reducing the interband scattering for holes. This indicates the hole mobility can be enhanced by inducing compressive strain in the $Ge_{1-x}Sn_x$ channel. Consequently, novel strain techniques, such as diamond like carbon [223] or phase-change liner stressor [224], should be explored to further enhance the hole mobility and thereby drive current of $Ge_{1-x}Sn_x$ p-MOSFETs.

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Appendix

List of Publications

Publications Related to This Thesis Work

[1] **L. Wang**, G. Han, S. Su, Q. Zhou, Y. Yang, P. Guo, W. Wang, Y. Tong, P. S. Y. Lim, C. Xue, Q. Wang, B. Cheng, and Y.-C. Yeo, "Metal stanogermanide contacts with enhanced thermal stability for high mobility germanium-tin field-effect transistor," *International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, 2012.

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Other Co-authored Publications

[7] H.-C. Chin, X. Gong, **L. Wang**, and Y.-C. Yeo, "Fluorine incorporation in HfAlO gate dielectric for defect passivation and effect on electrical characteristics of $In_{0.53}Ga_{0.47}As$ n-MOSFETs," *Electrochemical and Solid-State Letters*, vol. 13, pp. H440 - H442, 2010.

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