CONTACT AND SOURCE/DRAIN ENGINEERING FOR ADVANCED III-V FIELD-EFFECT TRANSISTORS

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B.Eng. (Hons.), NUS

A THESIS SUBMITTED

FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2014

DECLARATION

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information that have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Kong Yu Jin, Eugene

25 September 2014

Acknowledgements

First and foremost, I would like to thank my PhD supervisor, Prof. Yeo Yee-Chia, for his continuous support and guidance during my postgraduate studies here at the National University of Singapore (NUS). His ideas and inputs, financial support of my research, and willingness to always make time for discussions with me are highly appreciated. I am also thankful for his time and effort in providing valuable feedback that helps to improve the quality of my research publications as well as this dissertation. Special thanks also go to Prof. Chua Soo Jin and Assoc. Prof. Albert Liang Gengchiau for serving on my qualifying examination committee and providing useful comments and feedback on my research.

I am grateful to GLOBALFOUNDRIES Singapore and the Economic Development Board of Singapore for granting me a graduate scholarship. I have also benefited greatly from all the advice and knowledge imparted to us by Dr. Lap Chan, Dr. Ng Chee Mang, and Mr. Leong Kam Chew of GLOBALFOUNDRIES Singapore as part of the scholarship programme at GLOBALFOUNDRIES. The knowledge, which comprises both technical and business aspects, will stand me in good stead when I start work at GLOBALFOUNDRIES Singapore.

Next, I would like to give special mention to the staff and fellow students of Silicon Nano Device Laboratory (SNDL), who have formed an integral part of my postgraduate journey. Sincere thanks go to Mr. Patrick Tang, Mr. O Yan, and Ms. Yu Yi, and not forgetting the emergency response team (ERT) members, for providing technical and administrative support and ensuring the safety and proper functioning of the cleanrooms and lab. SNDL is indeed very fortunate to have such competent and dedicated staff. I am also especially grateful to all the post-docs and fellow students

that I have had the privilege of working with – in no particular order: Koh Shao Ming, Gong Xiao, Zhang Xingui, Guo Pengfei, Liu Bin, Zhou Qian, Sujith Subramanian, Samuel Owen, Ivana, Guo Huaxin, Guo Cheng, Goh Kian Hui, Low Kain Lu, Wang Lanxiang, Zhu Zhu, Tong Yi, Cheng Ran, Yang Yue, Ashvini Gyanathan, Zhan Chunlei, Phyllis Lim, Edwin Low, Pannirselvam, Vijay Richard D'Costa, Tong Xin, Wu Wenjuan, Han Genquan, Wang Wei, Liu Xinke, Maruf Amin Bhuiyan, Dong Yuan, Xu Xin, Han Han, Annie, Du Fang, Lei Dian, Li Lingzi, Sun Lu, Sandipan Chakraborty, Sachin Yadav, and anyone who has contributed in one way or another. I honestly believe that you are some of the most capable, knowledgeable, and helpful people I have known, and I am honoured and humbled to be able to know all of you and count you as friends.

I would like to express my gratitude to my collaborators at Applied Materials Inc. and the Institute of Materials Research and Engineering (IMRE) for all the fruitful discussions and collaborations, as well as the staff at IMRE and the Data Storage Institute (DSI) for their assistance with equipment usage and services rendered, such as X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM), and electron beam lithography (EBL), which have contributed significantly to my research.

Last but not least, I would like to thank my family and other friends outside of SNDL for all their support and encouragement during my postgraduate studies.

Table of Contents

DECLARATION 2
Acknowledgements 3
Table of Contents 5
Abstract 8
List of Tables 12
List of Figures 13
List of Symbols 24
List of Abbreviations 26

Chapter 1 Introduction 29
1.1 Background 29
1.2 Motivation for III-V Materials 32
1.3 Challenges of III-V CMOS Logic 33
1.3.1 High-quality gate stack 33
1.3.2 Low parasitic resistances 36
1.3.3 Integration on Si platform 41
1.4 Objectives of Thesis 44
1.5 Organization of Thesis 45

Chapter 2 Material Study for Salicide-Like Source/Drain Contact Metallization in InGaAs Metal-Oxide-Semiconductor Field-Effect Transistors 47
2.1 Introduction 47
2.2 Analysis of Metal Reaction with InGaAs 48
2.3 In-Depth Characterization of Pd-InGaAs 58
2.3.1 Sheet resistance analysis 60
2.3.2 XPS analysis 62
2.3.3 UPS analysis 64
2.3.4 Benchmarking with Ni-InGaAs 66
2.4 Conclusions 67

Chapter 3 Self-Aligned and Non-Self-Aligned Contact Metallization in InGaAs Metal-Oxide-Semiconductor Field-Effect Transistors: A Simulation Study 69

3.1 INTRODUCTION.....69

3.2 SIMULATION DETAILS.....70

3.3 RESULTS AND DISCUSSION.....73

3.4 CONCLUSIONS 86

Chapter 4 Towards Conformal Damage-Free Doping with Abrupt Ultra-Shallow Junction: Formation of Si Monolayers and Laser Anneal as a Novel Doping Technique for InGaAs n-MOSFETs.....87

4.1 INTRODUCTION.....87

4.2 BLANKET SAMPLE PREPARATION 89

4.3 MATERIAL CHARACTERIZATION 91

4.3.1 Disilane-treated samples 91

4.3.2 Silane-treated samples.....96

4.4 MOSFET FABRICATION AND CHARACTERIZATION 100

4.5 CONCLUSIONS 106

Chapter 5 Plasma Doping of InGaAs at Elevated Substrate Temperature for Reduced Sheet Resistance and Defect Formation.....107

5.1 INTRODUCTION.....107

5.2 BLANKET SAMPLE PREPARATION 108

5.3 MATERIAL CHARACTERIZATION 112

5.4 PLAD ON SMALL FIN STRUCTURES.....121

5.5 CONCLUSIONS 126

Chapter 6 Summary and Future Directions.....127

6.1 CONTRIBUTIONS OF THESIS.....127

6.1.1 Salicide-like S/D contact metallization for InGaAs MOSFETs 128

6.1.2 Comparison between self-aligned and non-self-aligned contact metallization in InGaAs n-MOSFETs.....129

6.1.3 Novel Si monolayer doping technique for InGaAs.....130

6.1.4 Plasma doping of InGaAs at elevated substrate temperature.....132

6.2 FUTURE DIRECTIONS 133

References **139**
List of Publications as First Author **160**
List of Publications as Second Author **161**

Abstract

Contact and Source/Drain Engineering for Advanced III-V Field-Effect Transistors

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Silicon (Si) has long been used as the channel material in the p-channel and n-channel metal-oxide-semiconductor field-effect transistors (p-MOSFETs and n-MOSFETs, respectively) that form the basis of today's complementary metal-oxide-semiconductor (CMOS) logic circuits. The scaling down of transistors has been an integral part of technology advancement for the microelectronics industry over more than five decades, providing the lower cost per transistor, greater functionality, and improved performance that have enabled increasingly powerful and sophisticated computers and gadgets. However, as technology scales beyond the 20 nm node, a roadblock is eventually encountered in the form of power consumption. To continue transistor scaling and further increase transistor density, lowering the supply voltage is mandatory in order to reduce power consumption.

A lower supply voltage, however, results in lower drive current and therefore slower transistors and circuits. To avoid sacrificing performance at reduced supply voltage, carrier mobilities higher than even strained Si can provide are required in the

MOSFET channels. High-mobility III-V compound semiconductors are a potential answer, offering the prospect of both high speed and low operating and standby power. Indium gallium arsenide (InGaAs), in particular, is a leading high-mobility III-V candidate for replacing Si in the channels of n-MOSFETs.

To harness the full potential of advanced short-channel III-V MOSFETs, the parasitic resistances outside the channel must be low, so as not to be performance-limiting. These parasitic resistances include the S/D resistance R_{SD}, S/D extension (SDE) resistance R_{SDE}, contact resistance R_c between the contact metallization and the S/D semiconductor, and metal resistance R_{metal}. R_{SD}, in particular, is a major resistance component in fin field-effect transistors (FinFETs) with narrow fin width and nanowire MOSFETs (NWFETs) with small wire diameter. At present, FinFETs have replaced planar MOSFETs as the main device architecture beyond the 22 nm technology node.

This thesis aims to find ways to meet the contact and S/D engineering challenges of advanced III-V MOSFETs in order to reduce parasitic resistances. More specifically, novel techniques for S/D contact formation and S/D doping in InGaAs n-MOSFETs are developed and investigated.

Self-aligned silicide or 'salicide' technology has become an essential part of Si CMOS, significantly reducing R_{SD} by forming S/D contact metallization that is self-aligned to the gate of the transistor. Ni-InGaAs, the first III-V salicide equivalent formed by directly reacting a metal (Ni) with InGaAs, emerged only recently (end 2010 and early 2011). In this thesis, the reaction of different metals with InGaAs is investigated to explore alternative salicide-like contact metallization technologies for InGaAs. Simulations are also carried out to determine the contact resistivity required and the continued relevance of salicide-like S/D contact metallization in InGaAs n-

MOSFETs at advanced technology nodes. The simulations illustrate the importance of salicide-like contact metallization at highly scaled dimensions, with reductions in R_c provided by the larger contact area compared to non-self-aligned contact metallization.

To obtain low R_{SD} and R_{SDE}, high doping concentration is needed in the S/D and SDE regions, especially for the ultra-shallow junctions demanded by short-channel MOSFETs to suppress leakage and short-channel effects. High S/D doping concentration is also essential for lowering R_c and enabling the abovementioned salicide-like contact metallization to meet contact resistivity targets. Hence, in conjunction with salicide-like technology, two doping techniques are also developed for InGaAs n-MOSFETs in this thesis. In addition to having the ability to form abrupt ultra-shallow junctions with high doping concentration, these techniques have to meet the challenges of conformally doping the S/D and SDE regions of three-dimensional (3D) MOSFETs such as FinFETs at highly scaled dimensions and pitches, where the incumbent beam-line ion implantation may start to face problems with conformality due to shadowing effects.

The first doping technique involves the formation of monolayers of Si on InGaAs by SiH_4 or Si_2H_6 gas treatment of the InGaAs surface, and can be described as a Si monolayer doping (MLD) technique. These Si monolayers act as a source of donors that are driven in and activated by a subsequent laser anneal to form n-type InGaAs. The second doping technique is plasma doping (PLAD), also using Si as an n-type dopant in InGaAs. The use of an elevated substrate temperature during PLAD is examined as a means of suppressing amorphization during implantation of the ions from the plasma, which is shown to be important in narrow fins where the fin geometry and a lack of sufficient crystalline seed for recrystallization leads to residual

corner defects after annealing. Both the Si MLD and PLAD techniques have the potential to enable 3D InGaAs MOSFETs to achieve conformal, highly doped S/D and SDE regions with abrupt, ultra-shallow junctions and few defects.

List of Tables

Table 2.1. Comparison of Ni-InGaAs and Pd-InGaAs formed by RTA at 250 °C for 60 s. 67

Table 3.1. Key parameters used in the simulations. 73

Table 4.1. Comparison with existing MLD works. 88

Table 5.1. Split table for samples doped by PLAD. 111

Table 5.2. Split table for samples doped by beam-line implant..... 111

List of Figures

Fig. 1.1. (a)-(f) Schematics illustrating a FinFET process flow, and (g)-(h) SEM images of a fabricated FinFET. The schematics and SEM images are from Ref. [35]. 31

Fig. 1.2. Schematic illustrating the key challenges for the use of III-V MOSFETs in CMOS logic. 33

Fig. 1.3. (a) Schematic and (b)-(c) cross-sectional TEM images of an $In_{0.7}Ga_{0.3}As$ n-MOSFET with an InP capping layer between the channel and the high-κ gate dielectric. This figure is taken from Ref. [107]. 35

Fig. 1.4. Schematic illustrating the parasitic resistance components of a MOSFET. 35

Fig. 1.5. Schematic illustrating the formation of salicide-like S/D contact metallization in InGaAs n-MOSFETs: Deposition of metal *M*, followed by RTA to induce reaction between *M* and InGaAs to form *M*-InGaAs contact metallization, and finally a selective etch to remove unreacted *M*. The *M*-InGaAs contact metallization needs to form a good ohmic contact to n^{++} InGaAs. 37

Fig. 1.6. Schematic illustrating the shadowing effect for beam-line ion implantation at narrow fin pitch. Ion implantation for one side of the fins is shown, with the other side implanted by rotating the wafer by 180°. The shadowing effect becomes more severe as fin pitch is reduced, and results in non-conformal doping as the bottom parts of the fins do not receive the ion implantation. 40

Fig. 1.7. (a) Cross-sectional TEM image of a graded buffer on Si substrate, with a III-V quantum well (QW) stack grown on top of it. (b) High-resolution TEM image of the QW device layers, showing good crystalline quality with no dislocations. The TEM images are from Ref. [57]. 42

Fig. 1.8. (a) Schematics for epitaxial layer transfer of InAs layers to a SiO_2-covered Si substrate to form an InAs-on-insulator substrate. (b) Cross-sectional SEM image of the donor wafer just before the layer transfer. (c)-(d) Cross-sectional TEM images of the InAs-on-insulator substrate. This figure is taken from Ref. [155]. 43

Fig. 1.9. (a) Schematic and (b) cross-sectional SEM image of GaAs on Ge grown on Si by the aspect ratio trapping technique. The dislocations, represented by thick black lines in (a), terminate on the SiO_2 sidewalls and are confined to the bottom of the trenches. This figure is taken from Ref. [156]. 43

Fig. 2.1. Process flow for the fabrication of TLM structures. 49

Fig. 2.2. Schematics illustrating the TLM process flow in Fig. 2.1. 50

Fig. 2.3. TEM images of Ti (a) as-deposited, and after 60 s anneal at (b) 300 °C, (c) 350 °C, or (d) 400 °C. EDX analysis was done at spots 1 to 3 in (c). 51

Fig. 2.4. TEM images of Co (a) as-deposited, and after 60 s anneal at (b) 300 °C, (c) 350 °C, or (d) 400 °C. EDX analysis was done at spots 4 to 6 in (b) and spots 7 to 10 in (c). 52

Fig. 2.5. TEM images of blanket samples of ~10 nm Pd on $In_{0.53}Ga_{0.47}As$ after 60 s isochronal anneal at (a) 200 °C, (b) 250 °C, and (c) 350 °C. 55

Fig. 2.6. High-magnification view of the interface between the Pd-InGaAs film and the $In_{0.53}Ga_{0.47}As$ substrate for the sample annealed at 250 °C for 60 s. 56

Fig. 2.7. (a) TLM *I-V* characteristics obtained for as-deposited Pd, and (b) the resulting plot of total resistance R_{total} versus TLM contact pad spacing d_{TLM}, from which contact resistance and specific contact resistivity values can be derived. The inset shows a schematic of the TLM structure, with the contact pads represented by gray rectangles (100-nm-thick Ni pads on top of the contact pads are not shown). Probing is done on two adjacent pads. 57

Fig. 2.8. (a) Contact resistance R_c and (b) specific contact resistivity ρ_c versus anneal temperature for Pd-InGaAs. Anneal time is fixed at 60 s. 58

Fig. 2.9. (a) SEM and (b) TEM images of an InGaAs MOSFET with Pd-InGaAs S/D contacts formed by a salicide-like process [178]. The red box in (b) overlays a TEM image with the unreacted Pd removed from the gate and spacer. 59

Fig. 2.10. Box plot and frequency distribution of R_{sheet} values for a 20-nm-thick Pd-InGaAs blanket sample formed by annealing at 250 °C for 60 s. The R_{sheet} values were measured in an 11 × 11 array of points with 100 μm step size, covering an area of 1 mm × 1 mm. 60

Fig. 2.11. Sheet resistance R_{sheet} versus anneal temperature for ~20 nm of Pd-InGaAs formed from ~10 nm of Pd. Anneal time is fixed at 60 s. The values for ~19 nm of Ni-InGaAs formed from ~11 nm of Ni on $In_{0.53}Ga_{0.47}As$ with the same doping concentration are also plotted for comparison. 61

Fig. 2.12. XPS spectra of bulk Pd-InGaAs (30-nm-thick) formed by 250 °C 60 s anneal. The Pd $3d_{5/2}$ peak in Pd-InGaAs is shifted 0.9 eV away from the Pd $3d_{5/2}$ peak position of 335.1 eV in elemental Pd. As 3d peaks indicate a shift of 1.2 eV in As $3d_{3/2}$ and $3d_{5/2}$ peaks in Pd-InGaAs from those in bulk $In_{0.53}Ga_{0.47}As$. 63

Fig. 2.13. He I UPS spectrum of 30-nm-thick Pd-InGaAs formed from 15 nm of Pd on $In_{0.53}Ga_{0.47}As$ by RTA at 250 °C for 60 s. The photon energy is 21.2 eV and the bias voltage is -5 V. The spectrum is plotted such that the Fermi edge is at zero binding energy. 64

Fig. 2.14. Benchmarking of the contact resistivities obtained for Ni-InGaAs and Pd-InGaAs formed on $In_{0.53}Ga_{0.47}As$ with different active doping concentrations. Ni-InGaAs and Pd-InGaAs were formed by reacting Ni and Pd, respectively, with $In_{0.53}Ga_{0.47}As$ by RTA at 250 °C for 60 s. 66

Fig. 3.1. Simulated n-MOSFETs with L_G of 15 nm, having (a) self-aligned metallization (SAM) or (b) non-self-aligned metallization (NSAM). The SAM is a 2.5-nm-thick salicide-like metallization (which may

be Ni-InGaAs), while the NSAM is a 2.5-nm-thick metal layer (which may be Mo) lining the tungsten via. 70

Fig. 3.2. (a) Schematic illustrating the scaling of S/D length L_{SD} with spacing d between the via and the gate edge, with the via kept centered in the S/D region. (b) Values of L_{SD} for each value of d..... 72

Fig. 3.3. I_d-V_g curves of $In_{0.53}Ga_{0.47}As$ MOSFETs having (a) SAM or (b) NSAM with d = 10 nm and with various values of ρ_c, showing identical subthreshold and OFF-state characteristics ($S \approx$ 95 mV/decade, DIBL ≈ 0.16 V/V, $V_{t,sat} \approx$ 0.18 V). $V_{t,sat}$ is determined by the constant current method with a fixed current level of 10 μA/μm. 74

Fig. 3.4. Drive current comparison of SAM and NSAM with various values of d and ρ_c. Compared to NSAM with the same d, SAM gives higher I_d at ρ_c larger than ~5×10^{-9} Ω·cm^2 due to larger A_{eff} and lower $R_{c,eff}$, but lower I_d at smaller ρ_c due to higher spreading resistance induced by its recessed geometry. 75

Fig. 3.5. Calculated L_C as a function of ρ_c for both SAM and NSAM. L_C increases with ρ_c, with the NSAM having larger L_C at the same ρ_c because of its lower $R_{sh,SD}$ and $R_{sh,m}$. The dashed lines indicate the values of L_{SD} for d = 10, 15, and 20 nm, which are compared with L_C for the SAM. For the NSAM, L_C is compared against L_V (= 15 nm). 76

Fig. 3.6. Calculated values of (a) R_{total} from simulated results and (b) $2R_{c,eff}$ as a percentage of R_{total} as d and ρ_c are varied for both SAM and NSAM in the linear regime. Both plots share the same legend. To meet the ITRS requirement (indicated by the dashed line), the SAM should have ρ_c less than 1×10^{-8} Ω·cm^2, while the NSAM needs ρ_c less than 5×10^{-9} Ω·cm^2. 78

Fig. 3.7. Schematic showing the series resistance bottleneck caused by the recessed geometry of the SAM, which leads to a more severe current crowding and therefore higher spreading resistance than the

NSAM. For a given SDE junction depth, a thicker SAM (larger t_{SAM}) results in a more serious current crowding problem. 79

Fig. 3.8. Current density contours (V_g = V_d = 0.63 V) for SAM and NSAM with d = 10 nm and ρ_c = 1×10^{-9} Ω·cm^2. Values indicated are in A/cm^2. Lateral profiles are taken along *A-A'* and *B-B'* in the source 0.5 nm below the SAM and NSAM, respectively, for various values of d and ρ_c and plotted in Figs. 3.9 to 3.11. 80

Fig. 3.9. Current density line profiles (V_g = V_d = 0.63 V) in the source 0.5 nm below the (a) SAM and (b) NSAM, with d = 10 nm and with various values of ρ_c. Diminishing gains can be observed as ρ_c is reduced, with the diminishing effect being smaller for the NSAM due to its larger $R_{c,eff}$. 81

Fig. 3.10. Current density line profiles (V_g = V_d = 0.63 V) along *A-A'* for SAM with various values of d and with (a) ρ_c = 1×10^{-7} Ω·cm^2 and (b) ρ_c = 1×10^{-9} Ω·cm^2. The profiles with ρ_c = 1×10^{-7} Ω·cm^2 are well-separated, while those with ρ_c = 1×10^{-9} Ω·cm^2 overlap in a 5-nm-wide region adjacent to the source extension. The current density at the source edge furthest from the source extension also exhibits much smaller differences for the various values of d at ρ_c = 1×10^{-7} Ω·cm^2 than at ρ_c = 1×10^{-9} Ω·cm^2. 81

Fig. 3.11. Current density line profiles (V_g = V_d = 0.63 V) along *B-B'* for NSAM with various values of d and with (a) ρ_c = 4×10^{-8} Ω·cm^2 and (b) ρ_c = 1×10^{-9} Ω·cm^2. The profiles have similar shapes for both large and small ρ_c, with small current peaks at the edges of the via due to current crowding. Changes in d result in roughly parallel shifts of the portion of the profile below the via, which defines A_{eff}. 82

Fig. 3.12. I_d as a function of ρ_c for SAM with various t_{SAM} and with d = 10 nm. A thinner SAM results in higher I_d due to less current crowding and therefore lower spreading resistance. The effect is bigger at low ρ_c, where R_c does not dominate. 83

Fig. 3.13. Simulated MOSFETs with L_G of 15 nm and raised S/D regions, having (a) SAM or (b) NSAM. S/D elevations of 5, 15, and 20 nm were simulated. 84

Fig. 3.14. I_d as a function of S/D elevation for SAM and NSAM with d = 10 nm and $\rho_c = 1\times10^{-9}$ Ω·cm^2. When the S/D regions are raised, the SAM no longer suffers from increased spreading resistance, allowing it to give higher I_d than the NSAM. 84

Fig. 3.15. I_d changes by less than 1% when the vias are misaligned by ±5 nm for both SAM and NSAM with d = 10 nm, $\rho_c = 1\times10^{-9}$ Ω·cm^2, and S/D elevation of 0 and 20 nm. 85

Fig. 4.1. Schematic of a fin structure illustrating the principle of the doping technique developed in this work, which has the potential to achieve conformal ultra-shallow doping with high doping concentration and abrupt junction without implant damage. At narrow fin widths, the sidewall junctions merge, rendering junction depth less important as it is determined by fin width. Nevertheless, junction abruptness and minimizing lateral dopant diffusion are crucial for short-channel devices. 89

Fig. 4.2. Process flow for fabricating blanket (001) $In_{0.53}Ga_{0.47}As$ samples with Si_2H_6 or SiH_4 treatment and laser anneal. 90

Fig. 4.3. R_{sheet} versus laser anneal fluence for Si_2H_6-treated $In_{0.53}Ga_{0.47}As$ samples. A single laser pulse was used. R_{sheet} decreases as fluence increases due to larger junction depth and higher dopant activation. R_{sheet} cannot be measured for laser fluence of 80 mJ/cm^2 and below. 92

Fig. 4.4. SIMS profiles for Si_2H_6-treated samples annealed at 127, 297, and 374 mJ/cm^2. The dashed lines indicate the InGaAs melt depth, which are estimated from the level or flat portion of the box-like profiles. 93

Fig. 4.5. SIMS profiles for Si_2H_6-treated samples annealed at 100 and 120 mJ/cm^2, with ultra-shallow melt depths of around 4 and 10 nm respectively, as indicated by the dashed lines. Very high Si concentration approaching 10^{21} cm^{-3} can be observed. The profile

for a fluence of 100 mJ/cm^2 exhibits little surface out-diffusion and good junction abruptness (~5.5 nm/decade). 95

Fig. 4.6. Estimated melt depth as a function of laser anneal fluence. Melt depth increases at higher laser anneal fluences due to higher temperatures induced near the InGaAs surface. 95

Fig. 4.7. (a) An example of the TLM *I-V* characteristics obtained from a SiH_4-treated sample, and (b) the resulting plot of total resistance R_{total} versus TLM contact pad spacing d_{TLM}, from which R_{sheet} of the InGaAs and ρ_c of the contact can be derived. The inset shows a schematic of the TLM structure, with the Ni contact pads represented by gray rectangles. Probing is done on two adjacent contact pads..... 97

Fig. 4.8. (a) R_{sheet} and (b) ρ_c versus laser fluence for samples treated with SiH_4 at 500 °C for 60 and 120 s. At each fluence, R_{sheet} and ρ_c are lower for the longer SiH_4 treatment time of 120 s due to a higher areal dose of Si dopants. R_{sheet} decreases as fluence increases due to larger junction depth and higher dopant activation. ρ_c first decreases then increases as fluence increases from 100 to 140 mJ/cm^2, due to better dopant activation but also more dopant out-diffusion at higher fluences. 97

Fig. 4.9. SIMS profiles for samples treated with SiH_4 at 500 °C for 120 s and laser annealed at 100, 120 and 140 mJ/cm^2. The profiles for fluences of 120 and 140 mJ/cm^2 are more box-like, while the profile for a fluence of 100 mJ/cm^2 has a very high Si concentration of ~5.25×10^{20} cm^{-3} at the InGaAs surface and a very steep slope of ~4 nm/decade. 98

Fig. 4.10. (a) Diode current-voltage characteristics showing high forward-to-reverse current ratio of 5 to 7 orders of magnitude. (b) Ideality factor of diodes versus diode size for various SiH_4 treatment times and laser anneal fluences. Both plots share the same legend. Diodes with a fluence of 100 mJ/cm^2 have very low *n* that is independent of L_{diode}. Diodes with a fluence of 120 and 140 mJ/cm^2

have higher n that also varies much more across diodes, which is attributed to melt-induced defects at the liquid-solid interface. 99

Fig. 4.11. (a) Process flow for fabricating planar InGaAs n-MOSFETs using the developed doping technique. Schematics of the transistor (b) after SiH_4 treatment and cap layer deposition and (c) after laser anneal are shown. 101

Fig. 4.12. SEM image of a completed $In_{0.53}Ga_{0.47}As$ n-MOSFET fabricated using the process flow in Fig. 4.11. 102

Fig. 4.13. Cross-sectional TEM image of an $In_{0.53}Ga_{0.47}As$ n-MOSFET with S/D doped by SiH_4 treatment at 500 °C for 120 s and laser anneal at 100 mJ/cm^2. The S/D contacts, which are 5 μm away from the gate, cannot be seen in this TEM image. 102

Fig. 4.14. High-magnification TEM images of the (a) channel and (b) S/D regions of the MOSFET in Fig. 4.13, with S/D regions doped by SiH_4 treatment at 500 °C for 120 s and laser anneal at 100 mJ/cm^2. Good crystalline quality is preserved in both regions and a good interface is maintained between the gate dielectric and the channel, with no laser-induced damage to the gate stack and channel. As there is no ion implantation, no implant-induced defects are created. .. 103

Fig. 4.15. I_g-V_g characteristics showing low gate leakage current after laser anneal at 100 mJ/cm^2, which confirms that gate stack integrity is not compromised. 104

Fig. 4.16. I_d-V_g characteristics of planar $In_{0.53}Ga_{0.47}As$ n-MOSFETs with S/D doped by SiH_4 treatment at 500 °C for (a) 60 s and (b) 120 s followed by laser anneal at a fluence of 100 mJ/cm^2, showing reasonable SS and negligible DIBL. 105

Fig. 4.17. I_d-V_d characteristics of the same pair of transistors as in Fig. 4.16, showing well-behaved output characteristics. V_t is the linear threshold voltage extracted by the maximum transconductance method. The low current level is due to high series resistance caused by the lack of deep S/D regions and the long distance

between the S/D contacts and the channel. Careful optimization of the doping technique is also required for R_{sheet} and ρ_c reduction. 106

Fig. 5.1. Process flow (solid bullets) for fabricating blanket samples using PLAD. Additional steps (open bullets) were carried out to form TLM structures and diodes on some of the fabricated blanket samples. 110

Fig. 5.2. Schematic illustrating the dissociation of SiH_4 and H_2 molecules into various chemical species in a plasma. Source: Fig. 26.1 in the *Springer Handbook of Electronic and Photonic Materials, 2006*. 110

Fig. 5.3. Secondary reactions in a SiH_4 or SiH_4/H_2 plasma. Source: Fig. 26.2 in the *Springer Handbook of Electronic and Photonic Materials, 2006*. 110

Fig. 5.4. Measured UV-VASE data (a) before RTA and (b) after RTA, obtained from samples doped by conventional beam-line implant. Solid lines are used for RT-BL samples, while dashed lines are used for ET-BL samples. The modeled ε_2 profile for 4.3 nm Al_2O_3 on 500 nm p^- $In_{0.53}Ga_{0.47}As$ on 500 μm p^+ InP is also plotted (open squares). 112

Fig. 5.5. (a) Low-magnification and (b) high-resolution TEM images of a blanket sample from Split P8 before RTA. An additional layer (~7 nm thick), determined by EDX to comprise of SiO_x and/or Si, was deposited on the Al_2O_3 by the plasma during PLAD. The InGaAs surface remains smooth and is not roughened by the PLAD, and the InGaAs shows good crystallinity with no visible defects for the given PLAD conditions of Split P8, even without RTA. 115

Fig. 5.6. Measured UV-VASE data (a) before RTA and (b) after RTA, obtained from samples doped by PLAD. Solid lines are used for RT-PLAD samples, while dashed lines are used for ET-PLAD samples. The modeled ε_2 profiles for 4 nm Al_2O_3 (cap layers present) or 1.7 nm InGaAs oxide (cap layers stripped), formed on 500 nm p^- $In_{0.53}Ga_{0.47}As$ on 500 μm p^+ InP, are also plotted (open squares). 115

Fig. 5.7. Si concentration depth profiles in InGaAs for Splits P7 and P8 before and after RTA, showing higher Si surface concentration and higher Si dose for ET-PLAD than for RT-PLAD. The Si surface concentration and Si dose increase after RTA for both RT-PLAD and ET-PLAD, due to diffusion of Si dopants from the Al_2O_3 cap into the InGaAs. 118

Fig. 5.8. Measured IR-VASE data for all PLAD splits after RTA at 600 °C for 60 s. The measured ε_2 profile for Split P8 before RTA and the modeled ε_2 profile for 5.5 nm native SiO_2 on 4 nm Al_2O_3 on 500 nm p^- $In_{0.53}Ga_{0.47}As$ on 500 μm p^+ InP are also plotted. 118

Fig. 5.9. R_{sheet} extracted from TLM structures for Splits P7 and P8 after RTA at 600 °C for 60 s. Lower R_{sheet} is obtained for ET-PLAD than for RT-PLAD, which may be attributed to a higher doping concentration and/or a thicker doped layer as seen from SIMS (Fig. 5.7) and IR-VASE (Fig. 5.8) data. 120

Fig. 5.10. Diodes formed by RT-PLAD and ET-PLAD exhibit similar diode characteristics, with a difference of ~6 orders of magnitude between forward and reverse currents, and reasonable ideality factor ranging from 1.28 to 1.35 121

Fig. 5.11. (a) Top-view SEM image of fins that were cut for TEM. The FIB cut is made along the line *A-A'*. (b) Tilt-view SEM image of standalone fins. 122

Fig. 5.12. Cross-sectional TEM image of a set of three 25-nm-wide fins from Split P1 after RTA. The fins are identical to each other, with rounded corners and vertical sidewalls. 123

Fig. 5.13. (a) Cross-sectional TEM image of a single 25-nm-wide fin from Split P1 after RTA. The dashed line indicates the interface between InGaAs and InAlAs. (b) High-magnification view of the top portion of the fin, showing that corner defects remain after anneal for fins that are amorphized during plasma ion implantation. 123

Fig. 5.14. High-magnification TEM image of the top portion of a 48-nm-wide fin from Split P1 after RTA. Like the fin in Fig. 5.13, corner defects

are present after anneal due to amorphization during plasma ion implantation, despite the larger fin width. 124

Fig. 5.15. (a) Cross-sectional TEM image of a 25-nm-wide fin from Split P6. The dashed line indicates the interface between InGaAs and InAlAs. (b) High-magnification view of the top portion of the fin, which shows that residual corner defects are absent after dopant activation anneal when the crystallinity of the fins is preserved during plasma ion implantation. 125

Fig. 5.16. High-magnification TEM image of the top portion of a 47-nm-wide fin from Split P6 after RTA. Like the fin in Fig. 5.15, no corner defects are present after anneal due to the suppression of amorphization during plasma ion implantation. 125

List of Symbols

A_{eff}	Effective contact area
C_{ox}	Gate dielectric capacitance of a MOSFET
d	Gap size between the via and the gate metal (not spacer)
D_{it}	Density of interface states
d_{TLM}	Contact pad spacing in a TLM structure
e	Elementary charge (1.6×10^{-19} C)
E_F	Fermi level
E_{vac}	Vacuum level
I	Current
I_d	Drain current of a MOSFET
$I_{d,sat}$	Saturation drain current of a MOSFET
I_g	Gate leakage current of a MOSFET
I_{off}	OFF-state current of a MOSFET
I_{on}	ON-state current of a MOSFET
L_C	Characteristic length
L_{diode}	Diode dimension
L_{eff}	Effective contact length
L_G	Gate length of a MOSFET
L_{SD}	Length of the source/drain regions
L_V	Via diameter
n	Diode ideality factor
N_d	Active donor concentration in a semiconductor
n_e	Electron concentration in a semiconductor
n_h	Hole concentration in a semiconductor
R_c	Contact resistance between a metal and a semiconductor
$R_{c,eff}$	Effective contact resistance

R_{ch}	Resistance of a MOSFET channel
R_{metal}	Resistance of a metal
R_{SD}	Resistance of the source/drain region of a MOSFET
R_{SDE}	Resistance of the source/drain extension region of a MOSFET
$R_{sh,SD}$	Sheet resistance of the source/drain region of a MOSFET
$R_{sh,m}$	Sheet resistance of the contact metallization
R_{sheet}	Sheet resistance
R_{total}	Total resistance
S	Subthreshold swing of a MOSFET
t_{NSAM}	Thickness of the non-self-aligned metallization
t_{SAM}	Thickness of the self-aligned metallization
V	Voltage
V_d	Voltage or bias applied to the drain of a MOSFET
V_{dd}	Supply voltage
V_g	Voltage or bias applied to the gate of a MOSFET
$V_{t,sat}$	Saturation threshold voltage of a MOSFET
V_t	Linear threshold voltage of a MOSFET
W	Channel width of a MOSFET
ε_2	Imaginary part of the pseudo-dielectric function
κ	Dielectric constant of a dielectric
μ	Carrier mobility in a MOSFET channel
μ_e	Electron mobility in a semiconductor
μ_h	Hole mobility in a semiconductor
μ_{max}	Maximum electron mobility
μ_{min}	Minimum electron mobility
ρ	Electrical resistivity of a semiconductor
ρ_c	Contact resistivity between a metal and a semiconductor

List of Abbreviations

2D	Two-dimensional
3D	Three-dimensional
AFM	Atomic force microscopy
ALD	Atomic layer deposition
AMAT	Applied Materials Inc.
CMOS	Complementary metal-oxide-semiconductor
CMP	Chemical mechanical polishing
DIBL	Drain-induced barrier lowering
DSI	Data Storage Institute
EBL	Electron beam lithography
EDX	Energy dispersive X-ray spectroscopy
ET-BL	Elevated-temperature beam-line ion implantation
ET-PLAD	Elevated-temperature plasma doping
FIB	Focused ion beam
FinFET	Fin field-effect transistor
HKMG	High-κ/metal-gate
III-V	Compound semiconductor comprising elements in Groups III and V of the periodic table
IMRE	Institute of Materials Research and Engineering
InGaAs	Indium gallium arsenide ($In_xGa_{1-x}As$, $0 \leq x \leq 1$)
IR-VASE	Infrared variable angle spectroscopic ellipsometry
ITRS	International Technology Roadmap for Semiconductors
LA	Laser anneal
MBE	Molecular beam epitaxy
MLD	Monolayer doping
MOSFET	Metal-oxide-semiconductor field-effect transistor

n^+	Moderately doped n-type
n^{++}	Heavily doped n-type
n-MOSFET	MOSFET with an n-type channel (electrons as inversion carriers)
NSAM	Non-self-aligned metallization
NWFET	Nanowire MOSFET
p^-	Lightly doped p-type
p^+	Moderately doped p-type
PLAD	Plasma doping
p-MOSFET	MOSFET with a p-type channel (holes as inversion carriers)
RF	Radio frequency
RMS	Root-mean-square
RTA	Rapid thermal anneal
RT-BL	Room-temperature beam-line ion implantation
RT-PLAD	Room-temperature plasma doping
S/D	Source/drain
SAM	Self-aligned metallization
sccm	Standard cubic centimeters per minute
SCE	Short-channel effect
SDE	Source/drain extension
SEM	Scanning electron microscopy
SIMS	Secondary ion mass spectrometry
SPM	Sulfuric peroxide mixture
SS	Subthreshold swing
TCAD	Technology Computer Aided Design
TEM	Transmission electron microscopy
TLM	Transfer length method
UPS	Ultra-violet photoelectron spectroscopy
UTB	Ultra-thin body

UV-VASE	Ultra-violet variable angle spectroscopic ellipsometry
VASE	Variable angle spectroscopic ellipsometry
XPS	X-ray photoelectron spectroscopy
μ-4PP	Micro four-point probes

Chapter 1

Introduction

1.1 BACKGROUND

For the past several decades, the microelectronics industry has seen aggressive shrinking of the transistors that form the basic building blocks of integrated circuits. Modern logic circuits rely on n-channel and p-channel metal-oxide-semiconductor field-effect transistors (n-MOSFETs and p-MOSFETs, respectively), known as complementary metal-oxide-semiconductor (CMOS) technology, with the cheap and abundant silicon (Si) being the dominant substrate material of choice. The scaling trend has followed Moore's law, which predicts a doubling of the number of transistors in integrated circuits roughly every two years, and is motivated by the increased packing density, faster switching speed, and lower switching energy that arise from transistor downsizing. The end result is lower cost per transistor, greater functionality, and improved performance.

A simple and well-known equation for the saturation drain current $I_{d,sat}$ of a long-channel MOSFET is given by

$$I_{d,sat} = \frac{1}{2}\mu C_{ox}\frac{W}{L_G}(|V_g - V_{t,sat}|)^2 \quad , \qquad (1.1)$$

where μ is the carrier mobility in the channel, C_{ox} is the gate dielectric capacitance per unit area, W is the channel width, L_G is the gate length, V_g is the applied gate bias (source grounded), and $V_{t,sat}$ is the saturation threshold voltage. Note that this equation describes only the MOSFET channel and does not include parasitic

resistances outside the channel. Effects such as polysilicon depletion in polysilicon gates and quantum confinement in the channel, which affect the overall gate-to-channel capacitance, are also not accounted for. Nevertheless, while this equation is very basic and may not hold for advanced MOSFETs at extremely scaled dimensions, it is useful for understanding the important role of scaling in enhancing MOSFET drive current performance. From (1.1), it is easily observed that a reduction in L_G produces an increase in $I_{d,sat}$, as will an increase in C_{ox} via a reduction of the gate dielectric thickness.

However, as transistor dimensions progress to the deep sub-micrometer regime and beyond, transistor scaling becomes increasingly difficult. Major scaling challenges include more severe short-channel effects (SCEs) at small L_G and increased susceptibility of thin dielectrics to breakdown, leading to high OFF-state leakage current as well as yield and reliability issues. Instead of relying exclusively on conventional scaling, various other techniques can also be used to enhance MOSFET performance. Strain techniques are an effective means of significantly boosting μ [1]-[11], and have been adopted in industry. For instance, Intel Corporation, widely regarded as the industry leader, employed a SiN liner stressor for n-MOSFETs and embedded SiGe source/drain (S/D) stressors for p-MOSFETs at the 90 nm technology node. Other than reducing the gate dielectric thickness, higher C_{ox} can also be achieved by increasing the dielectric constant κ of the gate dielectric, such as by nitriding the SiO_2 gate dielectric [12]-[15] or by using high-κ dielectrics [16]-[30]. In fact, gate leakage concerns have imposed a limit on SiO_2 thickness scaling and necessitated a switch to high-κ gate dielectrics. In addition, the increasing influence of polysilicon depletion on gate capacitance as gate dielectric thickness scales down has also mandated a switch to metal gates from polysilicon gates. The

first commercial chips featuring high-κ/metal-gate (HKMG) were produced by Intel at the 45 nm technology node in year 2007.

Another major development is fin field-effect transistors (FinFETs) [31]-[41], which were recently introduced for the first time in mass production by Intel at the 22 nm technology node in year 2011. Fig. 1.1 shows a FinFET fabrication process flow and scanning electron microscopy (SEM) images of a fabricated FinFET [35]. FinFETs are three-dimensional (3D) tri-gate MOSFETs with better gate electrostatic control of the channel, which helps to suppress SCEs [e.g. drain-induced barrier lowering (DIBL)], reduce leakage, and improve subthreshold performance (e.g. subthreshold swing). In addition, their 3D structure results in a smaller footprint for a given W, thus giving higher current per unit area. FinFETs are expected to replace planar MOSFETs as the main device architecture beyond the 22 nm node, with a possible progression to stacked or vertical gate-all-around nanowire MOSFETs (NWFETs) [42]-[53] further down the line.

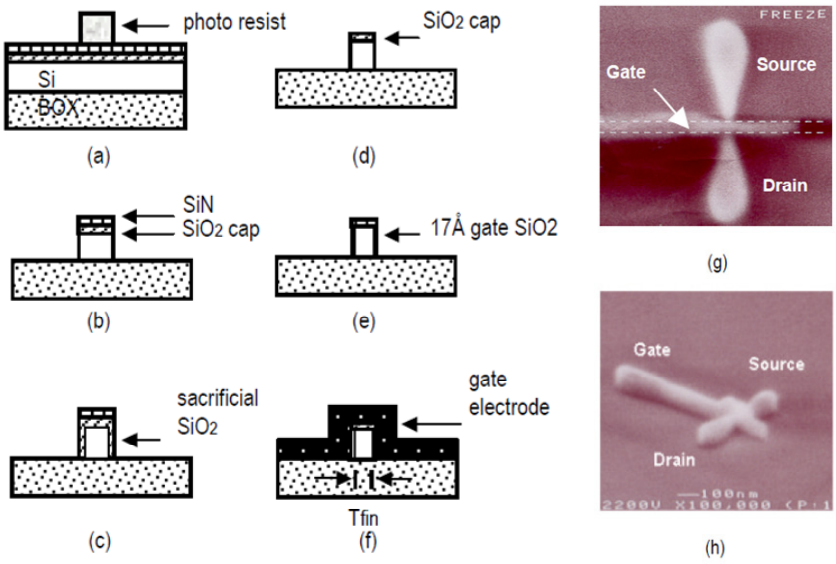

Fig. 1.1. (a)-(f) Schematics illustrating a FinFET process flow, and (g)-(h) SEM images of a fabricated FinFET. The schematics and SEM images are from Ref. [35].

1.2 MOTIVATION FOR III-V MATERIALS

Despite these efforts to continue the scaling trend and prolong silicon's status as the mainstay of the semiconductor industry, silicon is expected to eventually reach its scaling limit. The increased ON-state and OFF-state currents per transistor and the exponentially growing number of transistors in an integrated circuit combine to give rise to rapidly increasing operating and standby power consumption, such that as technology scales beyond the sub-20 nm regime, power consumption becomes the overriding concern rather than speed. For further increases in transistor density, it therefore becomes necessary to lower the supply voltage V_{dd} to reduce power consumption. However, from (1.1), it can be deduced that a lower V_{dd} (and hence lower V_g) is detrimental to drive current and switching speed.

High-mobility III-V semiconductor materials therefore have an important role to play as potential candidates to replace Si as the MOSFET channel material at advanced technology nodes, as their high carrier mobilities and injection velocities allow higher ON current I_{on} at the same OFF current I_{off}, or lower I_{off} at the same I_{on}, for a given V_{dd}. This enables III-V MOSFETs to maintain high performance at reduced V_{dd}. In other words, III-V MOSFETs hold great promise for achieving both high speed and low operating and standby power, which will enable the scaling trend to continue.

Attention has thus been devoted to the research of III-V materials [54]-[80], which include arsenides and antimonides, for potential application in CMOS technology. Among the possible III-V semiconductor materials to replace Si, indium gallium arsenide (InGaAs) is a leading contender for n-MOSFETs [80], and is the focus of the work in this thesis.

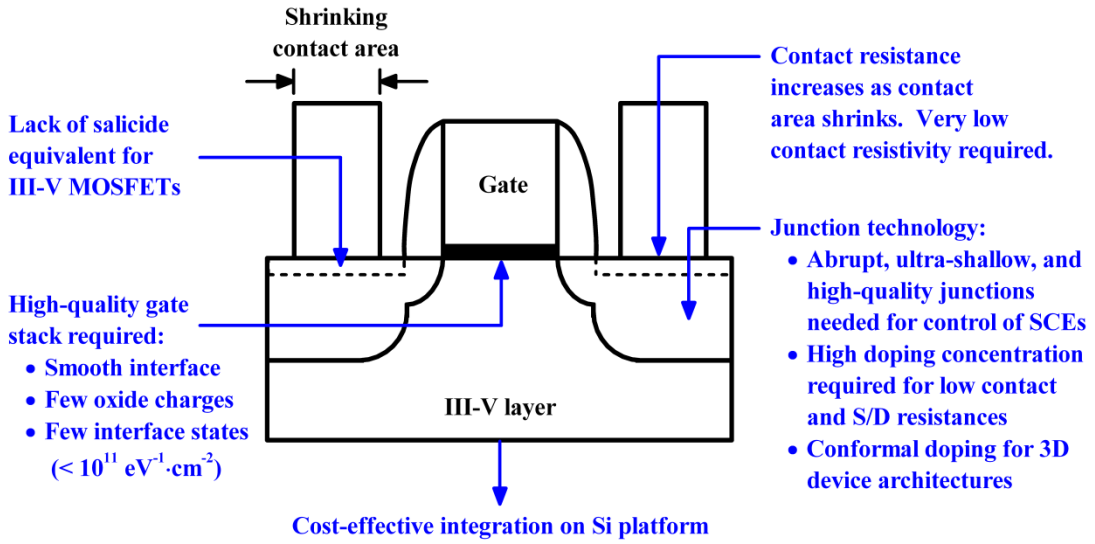

Fig. 1.2. Schematic illustrating the key challenges for the use of III-V MOSFETs in CMOS logic.

1.3 CHALLENGES OF III-V CMOS LOGIC

Many challenges have to be overcome before III-V MOSFETs can be used in mass production for CMOS logic circuits. These include the deposition of a high-quality gate stack, achieving low parasitic resistances, and cost-effective integration on a Si platform. The key challenges are illustrated in Fig. 1.2, and are discussed in the following subsections.

1.3.1 High-quality gate stack

One of the main challenges is the gate stack, which comprises the metal gate and high-κ gate dielectric. The gate modulates the electrostatic potential in the MOSFET channel in order to control the amount of charge in the channel and the barrier between the source and the channel, thereby turning the transistor on or off. In order for the gate to properly perform its function, a gate dielectric that has a minimal

amount of defects and a high-quality interface with the channel is required. A high density of interface states D_{it} at the interface between the gate dielectric and the channel causes Fermi level pinning, which inhibits the gate's ability to modulate the channel surface potential [81]. A rough dielectric-channel interface, high D_{it}, and high levels of defects and trapped charges in the gate dielectric can also severely degrade the mobility of carriers in the channel due to phonon, coulomb, and surface roughness scattering, as well as the trapping and de-trapping of carriers. This could negate the advantage that III-V materials have over Si in terms of carrier mobility and injection velocity, which defeats the purpose of using high-mobility channel materials.

Achieving a high-quality gate stack on III-V channel materials has proven to be difficult. The formation of native oxides on III-V surfaces tends to result in Fermi level pinning, and interface defects and states can also be formed when high-κ dielectrics are deposited on III-V materials [82]-[84]. Many techniques have been explored to improve the quality of gate stacks deposited on III-V materials [85]-[107] in order to reduce the amount and influence of dielectric and interface defects. These techniques include (i) surface cleaning (e.g. HCl), passivation [e.g. $(NH_4)_2S_x$], and pre-treatment (e.g. HBr) prior to gate stack formation, (ii) insertion of an interfacial layer (e.g. InP) between the gate dielectric and the channel, and (iii) post-deposition treatment (e.g. forming gas anneal). Fig. 1.3 shows a schematic and cross-sectional transmission electron microscopy (TEM) images of an $In_{0.7}Ga_{0.3}As$ n-MOSFET with an InP capping layer between the channel and the high-κ gate dielectric [107]. Alternatives to the commonly used Al_2O_3 and HfO_2 high-κ dielectrics have also been investigated [108]-[109].

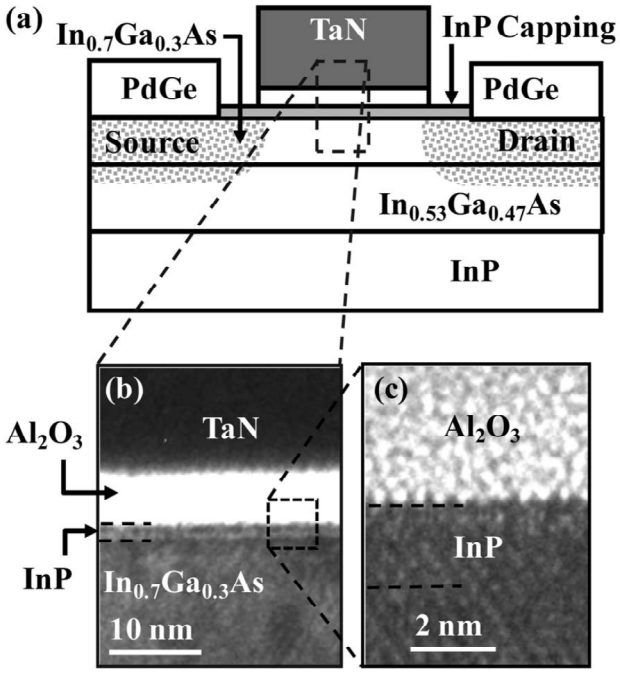

Fig. 1.3. (a) Schematic and (b)-(c) cross-sectional TEM images of an $In_{0.7}Ga_{0.3}As$ n-MOSFET with an InP capping layer between the channel and the high-κ gate dielectric. This figure is taken from Ref. [107].

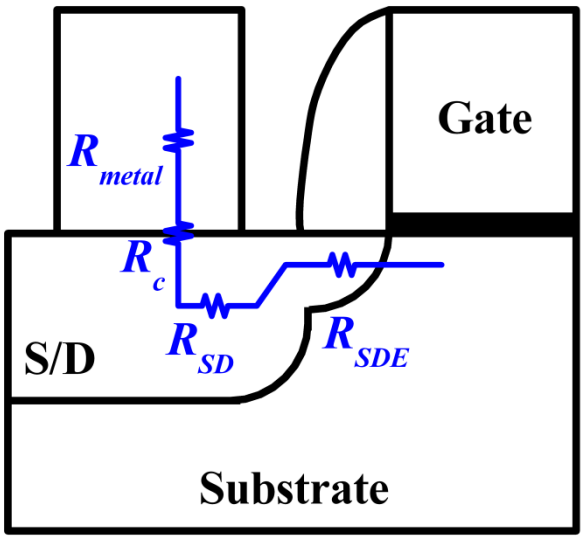

Fig. 1.4. Schematic illustrating the parasitic resistance components of a MOSFET.

1.3.2 Low parasitic resistances

The successful realization of a high-mobility channel with a high-quality gate stack in III-V MOSFETs is only half the battle won. To gain maximum benefit from high-mobility III-V MOSFETs and fully utilize their potential, another big challenge in the form of low parasitic resistances needs to be met. Fig. 1.4 illustrates the parasitic resistance components of a MOSFET, which include the S/D extension (SDE) resistance R_{SDE}, S/D resistance R_{SD}, contact resistance R_c between the contact metallization and the S/D semiconductor, and metal resistance R_{metal}. The employment of high-mobility channel materials and aggressively scaled L_G result in low channel resistance R_{ch} in III-V MOSFETs. With low R_{ch}, the parasitic resistances outside the channel need to be comparatively lower so that they do not limit drive current performance. R_{SD} also constitutes a significant portion of the total resistance for devices with the FinFET architecture [58]-[59], due to the very narrow fins that are required for good gate control [39]-[41]. Likewise, nanowire transistors [70]-[73] also face high R_{SD} due to the small diameter of the nanowire.

In Si CMOS technology, self-aligned silicide ('salicide') is used for the S/D contact metallization. Self-alignment of the S/D contact metallization to the gate brings it directly adjacent to the gate (separated by a spacer), thereby minimizing the distance and hence R_{SD} between the channel and the contact metallization. The salicide is formed by blanket deposition of a metal, followed by rapid thermal annealing (RTA) to induce reaction between the metal and the silicon S/D to form a metallic silicide, while the metal on the gate spacer and isolation regions remains unreacted. The unreacted metal is then selectively etched away, leaving S/D contact metallization that is self-aligned to the gate. This salicide process is well-established

for silicon, with extensive studies on various silicides [110]-[116] such as $TiSi_2$, $CoSi_2$, NiSi, and PtSi.

In III-V technology, self-aligned S/D contact metallization has been made before [117]-[118], but is not salicide-like. III-V MOSFETs did not have a salicide equivalent until the development of NiGeSi contact metallization for GaAs MOSFETs in year 2010 [119]-[121], which was formed by reacting Ni with a GeSi layer selectively grown on the GaAs S/D regions. A truly salicide-like S/D contact metallization in III-V MOSFETs would involve direct reaction between a metal and the III-V material. A schematic diagram for the formation of such salicide-like contact metallization in InGaAs n-MOSFETs is shown in Fig. 1.5.

Self-aligned Ni-InGaAs contact metallization formed by reacting Ni directly with InGaAs was subsequently developed [122]-[141]. Self-aligned Ni-InP [142] and NiInAs [143] S/D contact metallization, similarly formed by direct reaction between Ni and the III-V material (InP and InAs, respectively), were also

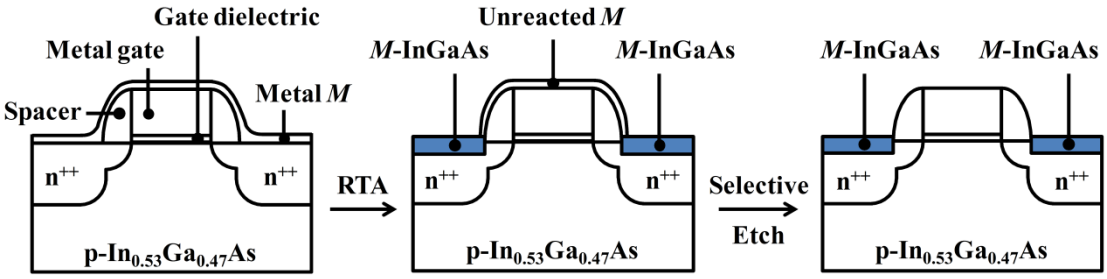

Fig. 1.5. Schematic illustrating the formation of salicide-like S/D contact metallization in InGaAs n-MOSFETs: Deposition of metal *M*, followed by RTA to induce reaction between *M* and InGaAs to form *M*-InGaAs contact metallization, and finally a selective etch to remove unreacted *M*. The *M*-InGaAs contact metallization needs to form a good ohmic contact to n^{++} InGaAs.

demonstrated. However, little else has been reported on alternative salicide-like contact metallization for III-V MOSFETs employing metals other than Ni. Regardless of the choice of contact metallization scheme (self-aligned or non-self-aligned) and the contact metal used, the contact resistivity ρ_c of the contact metallization on the S/D semiconductor must be low in order to achieve low R_c. So far, *in situ* Mo deposition has yielded the lowest ρ_c of $\sim 1\times10^{-8}$ $\Omega\cdot cm^2$ on $In_{0.53}Ga_{0.47}As$ [144]-[145] and $\sim 1\times10^{-9}$ $\Omega\cdot cm^2$ on $In_{0.65}Ga_{0.35}As$ [146], with mid-10^{19} cm^{-3} n-type active doping concentration. Mo is therefore a good candidate for non-self-aligned contact metallization in InGaAs n-MOSFETs. The lowest ρ_c obtained to date for Ni-InGaAs contact metallization is $\sim 1\times10^{-6}$ $\Omega\cdot cm^2$ on n-type $In_{0.53}Ga_{0.47}As$ with low- to mid-10^{19} cm^{-3} active doping concentration [136]-[137]. More work is needed to reduce the ρ_c of Ni-InGaAs in order for it to be competitive with Mo.

Other than contact formation, another important process module in the fabrication of MOSFETs is doping of the S/D and SDE regions, as it can significantly affect both the ON-state and subthreshold performances of the device. Abrupt, ultra-shallow, and high-quality junctions in the S/D and SDE regions are paramount for suppressing source-to-drain leakage and SCEs such as DIBL, especially in sub-10 nm MOSFETs. The electrical resistivity ρ of a semiconductor is given by

$$\rho = (en_e\mu_e + en_h\mu_h)^{-1} \quad , \qquad (1.2)$$

where e is the elementary charge (1.6×10^{-19} C), n_e is the electron concentration, μ_e is the electron mobility, n_h is the hole concentration, and μ_h is the hole mobility. An increase in doping concentration in the S/D and SDE regions therefore lowers R_{SD} and R_{SDE} through a reduction in ρ. This is especially important for ultra-shallow junctions, which would otherwise have high sheet resistance due to the thinness of the doped layer. The S/D doping concentration also plays an important role in reducing R_c, as

the ρ_c of a metal-semiconductor contact becomes smaller when the doping concentration at the semiconductor surface increases.

High doping concentration is therefore needed to minimize parasitic resistances and achieve a high drive current. The highest electron concentration that can be obtained for *in situ* Si-doped $In_{0.53}Ga_{0.47}As$ grown by MBE is found to be ~6×10^{19} cm^{-3} [147]. While this is lower than the mid-10^{20} cm^{-3} active n-type doping that can be achieved in silicon, the higher electron mobility of $In_{0.53}Ga_{0.47}As$ helps to bridge the gap and enables *in situ* Si-doped $In_{0.53}Ga_{0.47}As$ to achieve similar or better ρ. However, one disadvantage of *in situ* doping is the process complexity, as it requires selective growth of the III-V material, and may also involve a recess etch.

In addition to high doping concentration, 3D FinFETs require conformal doping to dope the sidewalls of the fins. Conformal doping with high doping concentration ensures that the drain current spreads more uniformly over the fin sidewalls to achieve a high I_{on}.

Beam-line ion implantation has so far been the primary doping technique employed in industry by virtue of its well-controlled dose and uniformity. Very low ion implant energies of a few keV and below are required for abrupt ultra-shallow junction formation. A pre-amorphization implant [148]-[150] may also be needed to suppress ion channeling. The use of ultra-low implant energies and the scaling up of wafer size have previously presented challenges to beam-line implantation throughput. Fortunately, the development of an advanced beam-line implanter with high beam current and excellent throughput has allowed beam-line implantation to meet the throughput needs of high-dose, ultra-low-energy implantations of large wafers.

However, as the fin pitch is scaled down, conformal doping becomes increasingly challenging and may not be sufficiently provided by conventional beam-line ion implantation. This is due to the directionality of the ion beam, which leads to shadowing effects (Fig. 1.6). At present, beam-line ion implantation remains a highly viable technique for doping FinFETs at the 14/16 nm technology node, but as the fin pitch continues to shrink, the angle limitations caused by shadowing could limit the use of beam-line implantation at advanced technology nodes. Furthermore, the crystal damage and defects caused by ion implantation become harder to repair at small fin dimensions due to a lack of sufficient crystalline seed for crystal regrowth, leading to higher leakage and series resistance. Therefore, new doping techniques that can fulfill the necessary requirements – namely high doping concentration, abrupt and ultra-shallow junctions with few defects, and conformal doping – need to be developed for III-V MOSFETs.

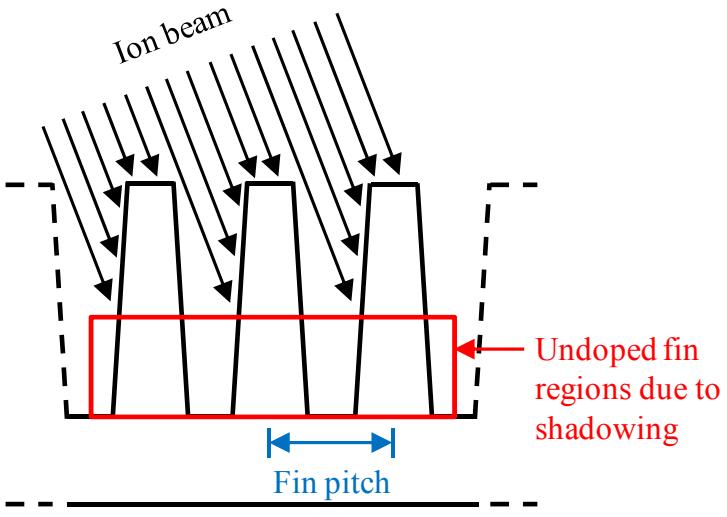

Fig. 1.6. Schematic illustrating the shadowing effect for beam-line ion implantation at narrow fin pitch. Ion implantation for one side of the fins is shown, with the other side implanted by rotating the wafer by 180°. The shadowing effect becomes more severe as fin pitch is reduced, and results in non-conformal doping as the bottom parts of the fins do not receive the ion implantation.

1.3.3 Integration on Si platform

Last but not least, a viable and cost-effective method is needed for large-scale integration of III-V MOSFETs on large Si substrates in order to keep equipment and manufacturing costs low. Possible methods that have been explored include buffer layer growth [57],[151],[152], III-V-on-insulator [153]-[155], and aspect ratio trapping [156]-[161].

In buffer layer growth, a graded buffer is grown on the Si substrate before the III-V device layers are grown. The III-V device layers cannot be grown directly on Si due to the large lattice mismatch, which will result in a low-quality film with many defects and dislocations. A graded buffer (which can comprise more than one layer) is therefore inserted between the III-V device layers and the Si substrate. The lattice constant of the graded buffer transitions gradually over the thickness of the buffer, starting from the lattice constant of Si at the bottom, and becoming equal or close to the lattice constant of the III-V device layers at the top. This allows the growth of relaxed or slightly strained III-V device layers that are defect-free, as the misfit dislocations and defects are confined to the buffer. Buffer layers tend to be made of ternary III-V compounds such as $In_xAl_{1-x}As$ and $Al_xGa_{1-x}As$, as their composition (the value of x) can be varied in order to provide a gradual transition in lattice constant. Fig. 1.7 shows cross-sectional TEM images of a graded buffer on Si substrate, with the III-V device layers grown on top of the buffer [57].

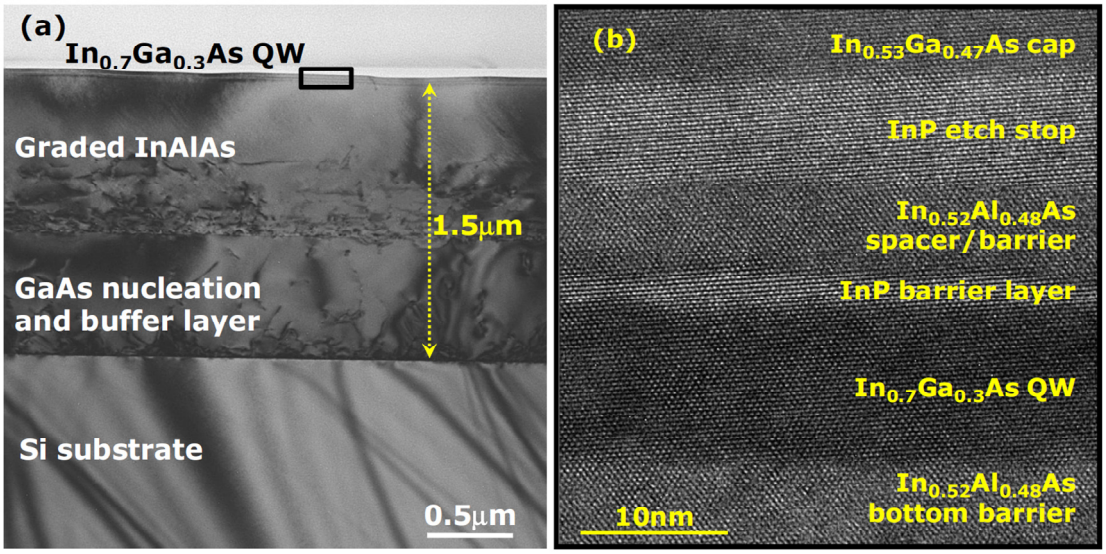

Fig. 1.7. (a) Cross-sectional TEM image of a graded buffer on Si substrate, with a III-V quantum well (QW) stack grown on top of it. (b) High-resolution TEM image of the QW device layers, showing good crystalline quality with no dislocations. The TEM images are from Ref. [57].

III-V-on-insulator is similar to silicon-on-insulator (SOI), which is well-established in Si technology, and is essentially a layer transfer technique. The desired III-V layer is first grown on a donor wafer, after which it is transferred to an oxide-covered Si substrate by direct wafer bonding and etchback [153], or by epitaxial layer transfer [154]-[155]. Fig. 1.8 illustrates the epitaxial layer transfer of InAs layers to form InAs-on-insulator [155]. Like SOI, the III-V-on-insulator layer can be relaxed or strained.

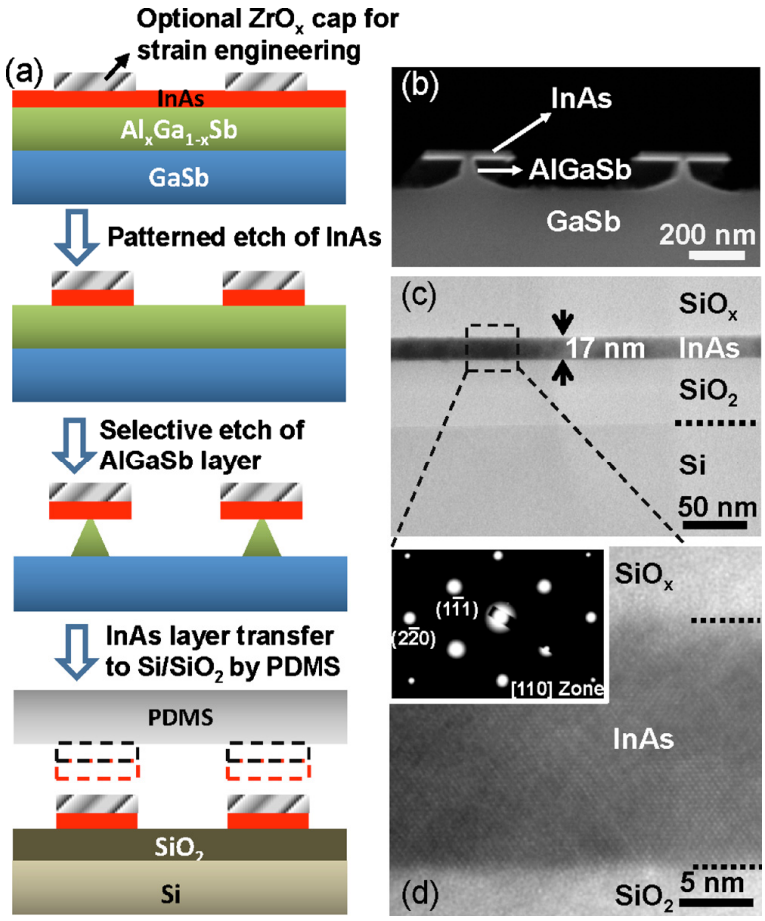

Fig. 1.8. (a) Schematics for epitaxial layer transfer of InAs layers to a SiO_2-covered Si substrate to form an InAs-on-insulator substrate. (b) Cross-sectional SEM image of the donor wafer just before the layer transfer. (c)-(d) Cross-sectional TEM images of the InAs-on-insulator substrate. This figure is taken from Ref. [155].

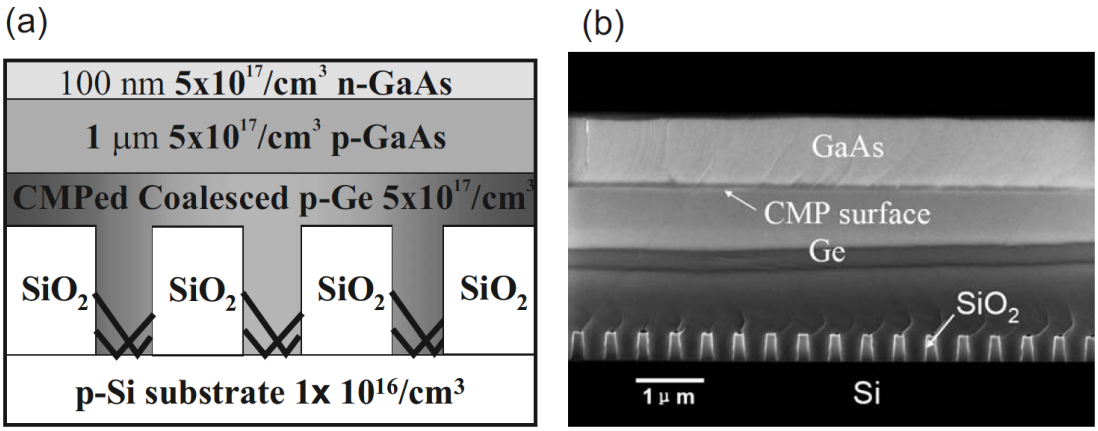

Fig. 1.9. (a) Schematic and (b) cross-sectional SEM image of GaAs on Ge grown on Si by the aspect ratio trapping technique. The dislocations, represented by thick black lines in (a), terminate on the SiO_2 sidewalls and are confined to the bottom of the trenches. This figure is taken from Ref. [156].

Aspect ratio trapping involves the growth of material in high-aspect-ratio SiO_2 trenches on Si. The Si substrate is exposed at the bottom of the SiO_2 trench. The dislocations induced by large lattice mismatch terminate on the SiO_2 sidewalls and are thus confined to the bottom of the trench, leaving high-quality material at the top of the trench that can be used for device fabrication. Fig. 1.9 shows the growth of Ge in SiO_2 trenches on Si, with epitaxial lateral overgrowth above the trenches, after which the Ge is planarized by chemical mechanical polishing (CMP) before the growth of GaAs buffer and device layers [156]. III-V materials can also be grown directly in the SiO_2 trenches [157]-[161].

Whichever integration method is used, top-quality III-V layers with minimal defects much be obtained for good device performance. Further complications (e.g. different lattice constants and thermal expansion coefficients) arise from the fact that the materials used for n-MOSFETs and p-MOSFETs may not be the same. Therefore, the integration of high-mobility materials on Si substrates is challenging.

1.4 OBJECTIVES OF THESIS

The research in this thesis focuses on contact and S/D engineering for InGaAs n-MOSFETs, taking a dual approach to tackling the dominance of parasitic resistances in high-mobility MOSFETs at highly scaled dimensions. Solutions to the S/D contact and doping challenges of InGaAs n-MOSFETs are explored, and are divided into two parts.

The first part of this thesis work examines S/D contact metallization technology for InGaAs n-MOSFETs, and comprises both experiments and simulations. The InGaAs equivalent of the salicide contact metallization technology used in Si is first studied by reacting different metals with InGaAs. This contact metallization

technology can potentially give significant reductions in R_{SD} for InGaAs n-MOSFETs, just as it has done for Si MOSFETs. However, the scaling down of the gate pitch means that contact areas are getting smaller, bringing along with it a concomitant increase in R_c which could become the dominant source of parasitic resistance. At the same time, contact plugs or vias that are not self-aligned to the gate can be brought very close to the gate by improved lithographic capabilities, reducing the benefit of lower R_{SD} provided by salicide-like contact metallization. Hence, two-dimensional (2D) simulations are performed not only to ascertain the ρ_c requirements for S/D contact metallization in InGaAs n-MOSFETs, but also to assess the importance of salicide-like contact metallization with respect to non-self-aligned contact metallization in InGaAs n-MOSFETs at advanced technology nodes.

In the second part of this thesis work, new doping techniques that can address the shortcomings of conventional beam-line ion implantation at advanced technology nodes are developed for InGaAs n-MOSFETs. These doping techniques not only aim to achieve the highly doped high-quality S/D or SDE regions with abrupt ultra-shallow junctions that are required for low parasitic resistances and low leakage, but also seek to provide doping solutions for 3D device architectures with highly scaled dimensions.

1.5 ORGANIZATION OF THESIS

Chapters 2 to 5 document the research work done, the results obtained, and the analysis of those results.

In Chapter 2, the reaction of various metals (Ti, Co, and Pd) with InGaAs is studied for the development of salicide-like contact metallization for InGaAs n-MOSFETs. The conditions for reaction between the metal and InGaAs are

determined, and the reaction products formed are characterized in terms of their material and electrical properties, such as thickness uniformity, work function, sheet resistance, and contact resistivity.

In Chapter 3, InGaAs n-MOSFETs employing either salicide-like or non-self-aligned S/D contact metallization are compared by means of 2D simulations, allowing the advantages of salicide-like contact metallization to be examined for InGaAs n-MOSFETs at advanced technology nodes.

In Chapter 4, a new technique capable of forming conformal, ultra-shallow, and abrupt junctions with high doping concentration in InGaAs n-MOSFETs is developed. The promising technique, which uses Si monolayers and laser anneal to form high-quality junctions without implant damage, is successfully demonstrated in planar InGaAs n-MOSFETs for the first time.

In Chapter 5, plasma doping (PLAD) is explored as another doping technique that can conformally dope the S/D or SDE regions of 3D InGaAs n-MOSFETs. The use of an elevated substrate temperature is also investigated as a means for suppressing amorphization during the introduction of dopants into InGaAs. This is potentially important for MOSFETs with the ultra-thin body (UTB), FinFET, or NWFET architectures, where recrystallization during the subsequent dopant activation anneal could prove problematic.

Chapter 6 summarizes the contributions of this thesis and provides possible future directions for building on the work that has been presented.

Chapter 2

Material Study for Salicide-Like Source/Drain Contact Metallization in InGaAs Metal-Oxide-Semiconductor Field-Effect Transistors

2.1 INTRODUCTION

In this Chapter, the equivalent of the self-aligned silicide ('salicide') in Si technology is explored for III-V metal-oxide-semiconductor field-effect transistors (MOSFETs).

In the selection of metals for this source/drain (S/D) contact metallization scheme, an important criterion that needs to be satisfied is the ability of the metal to react with III-V materials to form a low-resistance ohmic contact. There should also be good etch selectivity of the unreacted metal over the reaction product so that the unreacted metal can be removed completely to prevent shorting without adversely affecting the S/D contact metallization.

Salicide-like contact metallization formed by reaction of Ni with III-V materials such as InGaAs, InP, and InAs has been reported [122]-[143]. The reaction of other metals – namely Ti, Co, and Pd – with InGaAs is thus investigated for the formation of salicide-like contact metallization in InGaAs n-channel MOSFETs (n-MOSFETs). Like Ni, Ti and Co have been used to form silicides in Si technology [110]-[115] and therefore have known etchants for the removal of

unreacted Ti and Co. The choice of Pd is motivated by PdGe contact metallization reported in literature, which forms good ohmic contacts to III-V materials [162]-[171].

2.2 ANALYSIS OF METAL REACTION WITH INGAAS

It is first necessary to determine the annealing conditions required for the metals to react with InGaAs. 500-nm-thick (001) $In_{0.53}Ga_{0.47}As$ with a p-type doping concentration of ~2×10^{16} cm^{-3}, formed by molecular beam epitaxy (MBE) on bulk InP, was used as the starting substrate for all samples. The substrates were purchased from a vendor. Two kinds of samples were prepared: blanket samples and transfer length method (TLM) [172] samples. The blanket samples are used to ascertain the temperature at which various metals react with InGaAs to form a metallic product, which is necessary for a salicide-like process. The TLM samples are used for contact resistivity extraction. All the sample fabrication, characterization, and analysis were done by the author unless otherwise mentioned.

Blanket samples were prepared by cleaning the bare $In_{0.53}Ga_{0.47}As$ surface with dilute hydrofluoric acid ($HF:H_2O$ = 1:100) for 60 s, followed immediately by deposition of metal (Ti, Co, or Pd) by electron beam evaporation. The samples were then cut into pieces and each piece was annealed by a single rapid thermal anneal (RTA) at 200, 250, 300, 350, or 400 °C for 60 s in a N_2 ambient.

The first step in the fabrication of TLM samples was blanket implantation of Si at 7° tilt. Two implants were used: the first at a dose of 10^{14} cm^{-2} and an energy of 70 keV (projected range ≈ 66 nm), and the second at the same dose but with an energy of 25 keV (projected range ≈ 27 nm). A SiO_2 capping layer (~30 nm) was then deposited before dopant activation RTA at 600 °C for 60 s. The active donor

concentration is estimated to be ~2×10^{18} cm^{-3} [173]. Optical lithography for mesa isolation was performed and the mesa pattern was transferred to the SiO_2 layer by buffered oxide etch. The photoresist was then removed. Mesa etching was performed with sulfuric peroxide mixture (H_2SO_4:H_2O_2:H_2O = 1:1:20) (SPM) to a depth of ~300 nm to isolate the TLM structures. TLM contact pads were then defined by optical lithography and the pattern was transferred to the SiO_2 layer by etching. A 60 s dilute HF clean (HF:H_2O = 1:100) was carried out right before loading the samples into an electron beam evaporator chamber for metal (Ti, Co, or Pd) deposition. After deposition, photoresist lift-off was performed using acetone. The samples were then cut into pieces, with each piece undergoing a single RTA with conditions identical to those used for blanket samples. 100-nm-thick Ni pads were then deposited on the contact metal pads to ensure a metal stack with low sheet resistance, using the same deposition and lift-off process that was used for the metal deposition, including a 20 s dilute HF clean before deposition. Figs. 2.1 and 2.2 summarize the process flow for TLM sample fabrication.

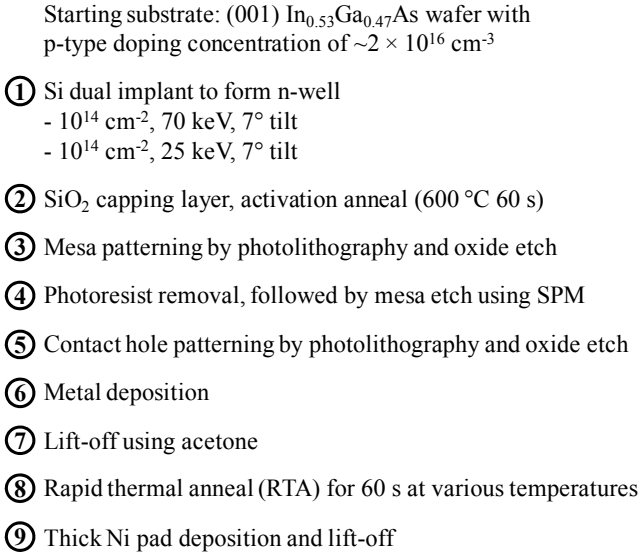

Fig. 2.1. Process flow for the fabrication of TLM structures.

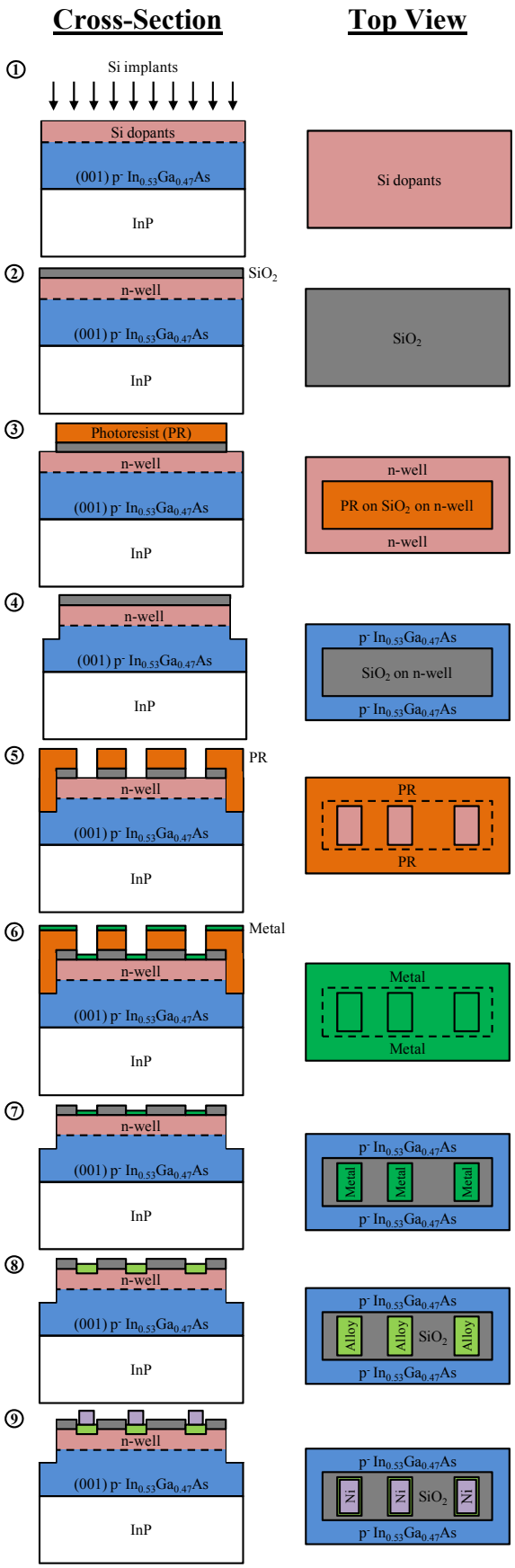

Fig. 2.2. Schematics illustrating the TLM process flow in Fig. 2.1.

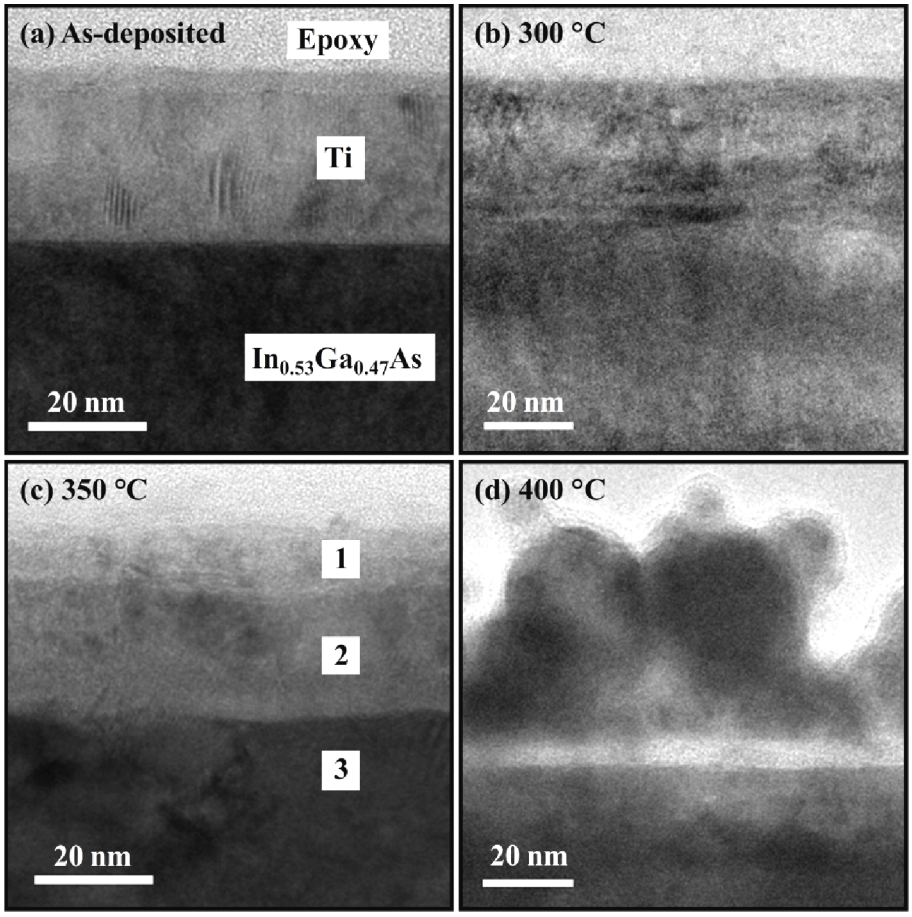

Fig. 2.3. TEM images of Ti (a) as-deposited, and after 60 s anneal at (b) 300 °C, (c) 350 °C, or (d) 400 °C. EDX analysis was done at spots 1 to 3 in (c).

Fig. 2.3 shows the transmission electron microscopy (TEM) images obtained from blanket samples of Ti on $In_{0.53}Ga_{0.47}As$ before and after annealing. All the TEM in this Chapter was done by a colleague, Dr. Qian Zhou, unless otherwise stated. ~30 nm of Ti was deposited on the $In_{0.53}Ga_{0.47}As$ substrate, as seen in Fig. 2.3(a), followed by annealing at a temperature of 300, 350, or 400 °C for 60 s.

It can be observed from Figs. 2.3 (b) and (c) that there is hardly any increase in the film thickness after annealing at 300 or 350 °C, suggesting that little reaction has taken place. However, the film appears to be badly degraded or agglomerated after 400 °C anneal [Fig. 2.3(d)]. Energy dispersive X-ray spectroscopy (EDX) with a

spot size of ~10 nm was carried out on the Ti sample annealed at 350 °C at the three spots indicated in Fig. 2.3(c). At spot 1, a mixture of Ti and O is detected, while at spot 2, the film is made up almost entirely of Ti, with a small amount of As. Spot 3 yields mostly In, Ga, and As, with a tiny amount of Ti. This confirms that there is little to no reaction between Ti and the $In_{0.53}Ga_{0.47}As$ substrate.

The TLM current-voltage (*I-V*) characteristics for as-deposited and annealed Ti samples are curves rather than straight lines, indicating that the contacts are not ohmic. As a result, contact resistance and contact resistivity values could not be extracted from the TLM data for Ti samples.

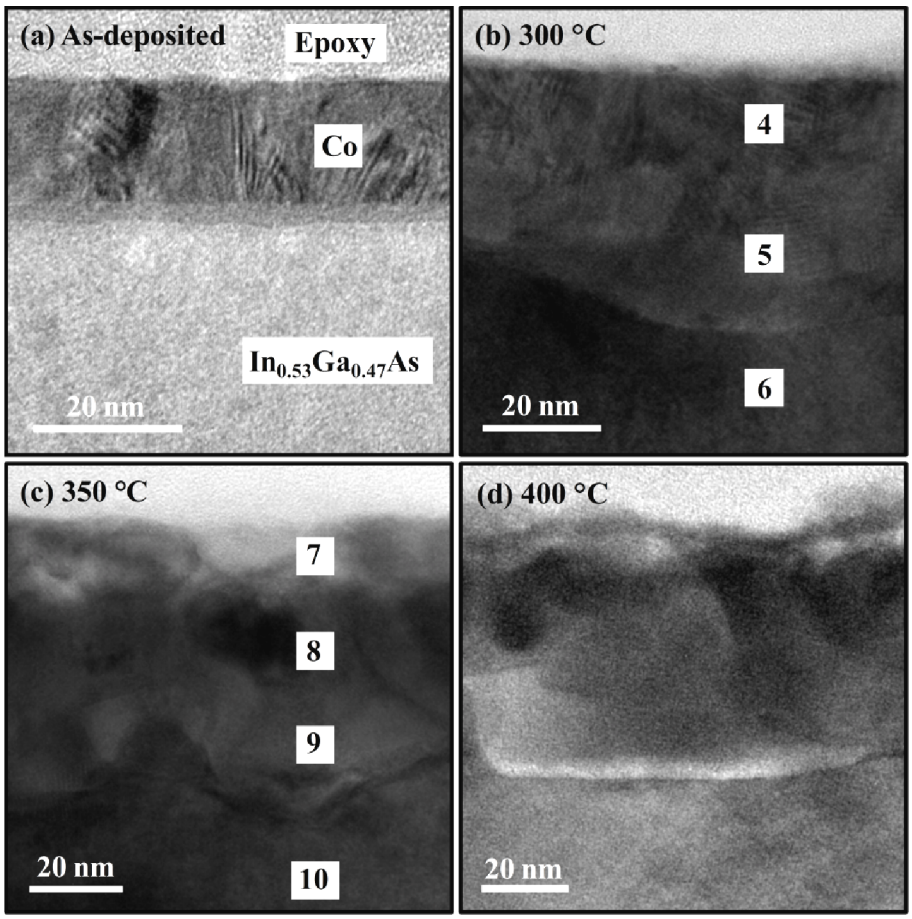

Fig. 2.4. TEM images of Co (a) as-deposited, and after 60 s anneal at (b) 300 °C, (c) 350 °C, or (d) 400 °C. EDX analysis was done at spots 4 to 6 in (b) and spots 7 to 10 in (c).

TEM images for ~20 nm of Co deposited on $In_{0.53}Ga_{0.47}As$ and annealed at various temperatures for 60 s are presented in Fig. 2.4. For the Co sample annealed at 300 °C [Fig. 2.4(b)], a change at the interface between Co and $In_{0.53}Ga_{0.47}As$ is observed. Co appears to have diffused into the $In_{0.53}Ga_{0.47}As$ substrate, as confirmed by the detection of a substantial amount (~35 atomic %) of Co by EDX at spot 5, while at spot 6, only In, Ga and As were detected. However, the diffusion of Co does not appear to be uniform, and there is still an almost 20 nm layer of Co remaining on the surface, as determined by EDX at spot 4, which shows the top layer to be almost entirely Co with tiny amounts of In, Ga and As.

After 350 °C anneal [Fig. 2.4(c)], the resultant film appears to be more uniform compared to the sample annealed at 300 °C [Fig. 2.4(b)], although the interface between the metal film and the substrate is very rough. In addition, the thickness of the film has increased to ~60 nm. These observations suggest a more uniform diffusion and reaction of the Co with the $In_{0.53}Ga_{0.47}As$ substrate to form Co-InGaAs. EDX at spots 7, 8, and 9 [Fig. 2.4(c)] indicate ~35-40 atomic % of Co mixed with In, Ga and As, while spot 10 yields only In, Ga and As. The absence of a layer of pure Co indicates that the Co has fully reacted with $In_{0.53}Ga_{0.47}As$. It is interesting to note that much more Ga (~46 atomic %) than As (~12 atomic %) is detected at spot 7, whereas there is much more As (~51 atomic %) than Ga (~6 atomic %) at spot 8, and comparable amounts of Ga and As (26-32 atomic %) at spot 9. Small amounts of In (2-6 atomic %) are detected at spots 7, 8, and 9.

For the sample annealed at 400 °C [Fig. 2.4(d)], the film has a thickness of ~60 nm, similar to that obtained by 350 °C anneal, and has an equally rough (if not rougher) morphology and interface with the $In_{0.53}Ga_{0.47}As$ substrate. The lack of

increase in the thickness of the metal film suggests that a 350 °C anneal may be sufficient for complete reaction.

The Co and Co-InGaAs TLM current-voltage (*I-V*) characteristics produced straight lines, indicating that Co and Co-InGaAs form ohmic contacts with the n-$In_{0.53}Ga_{0.47}As$ substrate. Contact resistivity values of the Co and Co-InGaAs contact metallization extracted from the TLM data were in the range of mid 10^{-4} $\Omega \cdot cm^2$.

Cross-sectional TEM images were obtained for Pd on $In_{0.53}Ga_{0.47}As$ after annealing at 200, 250 or 350 °C (Fig. 2.5). As-deposited Pd thickness was ~10 nm. After annealing, a single metallic film is seen on the $In_{0.53}Ga_{0.47}As$ substrate and confirmed by EDX to be made up of Pd, In, Ga, and As. This indicates that the deposited Pd was fully reacted to form Pd-InGaAs.

The Pd-InGaAs films formed at 200 and 250 °C [Figs. 2.5 (a) and (b)] look identical and have a similar atomic ratio of Pd:In:Ga:As (~58:9:14:19) as obtained by EDX. The EDX spot (~10 nm in diameter) was located approximately in the middle of the 20-nm-thick Pd-InGaAs film in the TEM cross-section. The atomic ratio can also be obtained by X-ray photoelectron spectroscopy (XPS), as discussed later. Both films are amorphous and have a thickness of ~20 nm, and they exhibit excellent smoothness, uniformity, and interfacial quality. Very low root-mean-square (RMS) roughness of ~0.7 nm in a 10 μm × 10 μm area was measured by an atomic force microscopy (AFM) scan of the film formed at 200 °C. A high-magnification TEM image of the sample annealed at 250 °C (Fig. 2.6) shows the good interface between the Pd-InGaAs film and the $In_{0.53}Ga_{0.47}As$ substrate. In contrast, the film formed at 350 °C has a degraded morphology and interface [Fig. 2.5(c)], which is detrimental, especially for shallow S/D junctions. The degraded morphology and interface could be due to the formation of polycrystalline film.

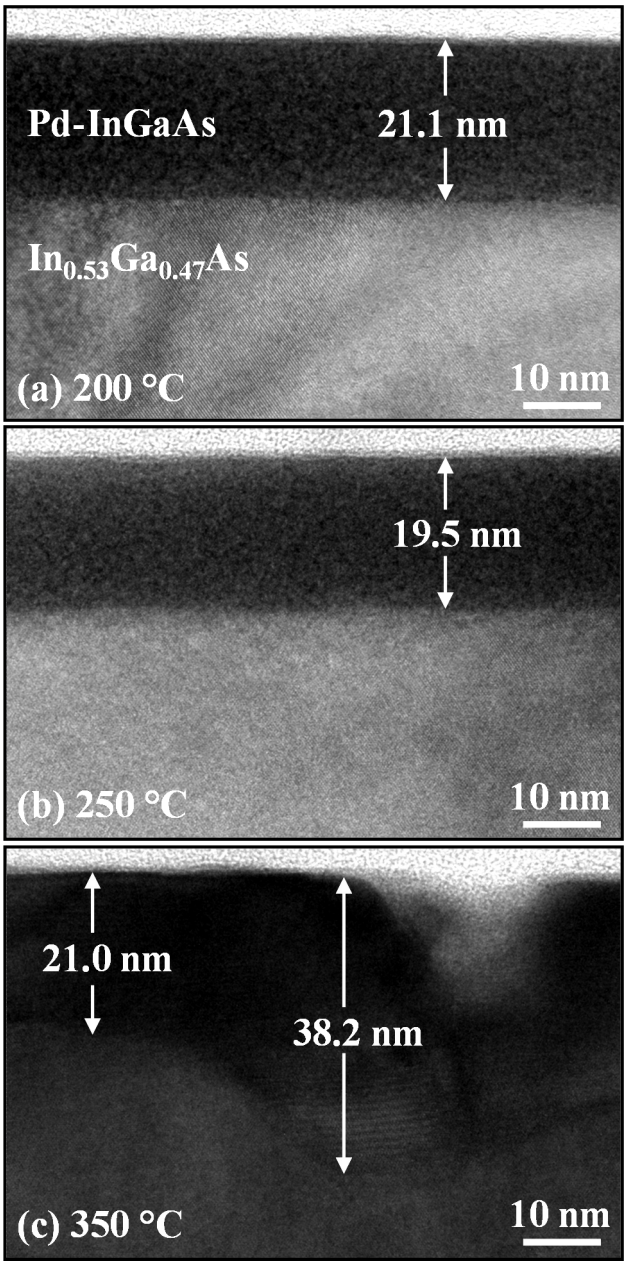

Fig. 2.5. TEM images of blanket samples of ~10 nm Pd on $In_{0.53}Ga_{0.47}As$ after 60 s isochronal anneal at (a) 200 °C, (b) 250 °C, and (c) 350 °C.

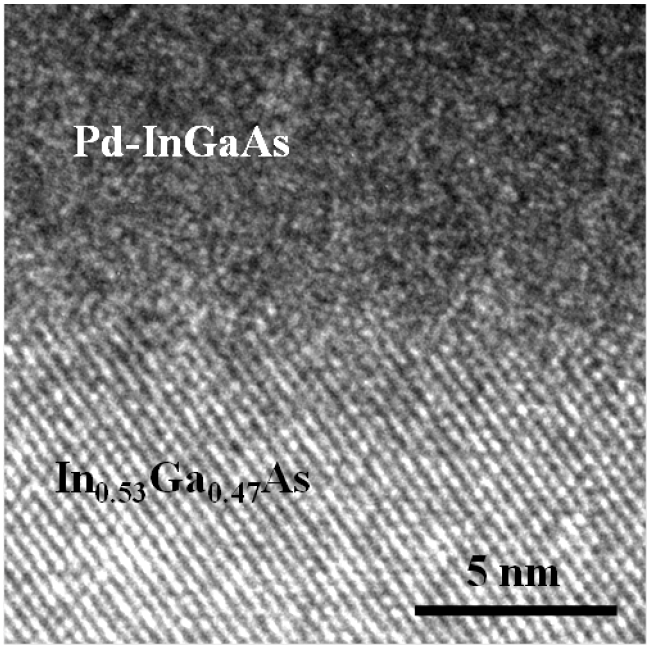

Fig. 2.6. High-magnification view of the interface between the Pd-InGaAs film and the $In_{0.53}Ga_{0.47}As$ substrate for the sample annealed at 250 °C for 60 s.

In studies of Si/Pd and Ge/Pd contact schemes on GaAs [163]-[164], Pd can react with GaAs at ~100 °C to form a metastable intermediate Pd_4GaAs phase. Hence, while a low temperature of 200 °C is sufficient to cause reaction between Pd and $In_{0.53}Ga_{0.47}As$, it may not be the lowest temperature required. This is in contrast to Ni-InGaAs and Co-InGaAs, which require an anneal temperature of at least about 250 °C and 350 °C, respectively, for their formation.

The Pd and Pd-InGaAs TLM *I-V* characteristics yielded straight lines, indicating that Pd and Pd-InGaAs form ohmic contacts with n-type $In_{0.53}Ga_{0.47}As$ with active doping concentration of $\sim 2\times10^{18}$ cm^{-3}. An example of the TLM *I-V* characteristics, obtained for as-deposited Pd (10 nm), is shown in Fig. 2.7(a), along with the resulting plot of total resistance R_{total} versus TLM contact pad spacing d_{TLM} in Fig. 2.7(b). Despite having a relatively large work function of 5.12 eV [174], Pd can

form an ohmic contact on n-type $In_{0.53}Ga_{0.47}As$ with such modest doping, which is likely due to Fermi level pinning towards the conduction band of the InGaAs. In fact, the charge neutrality level of $In_{0.53}Ga_{0.47}As$ is found to be ~0.2 eV below its conduction band [175]. The contact resistance and specific contact resistivity values extracted from the TLM *I-V* characteristics are plotted in Fig. 2.8, showing higher contact resistivity for Pd-InGaAs films formed at 250, 300, and 350 °C compared to as-deposited Pd.

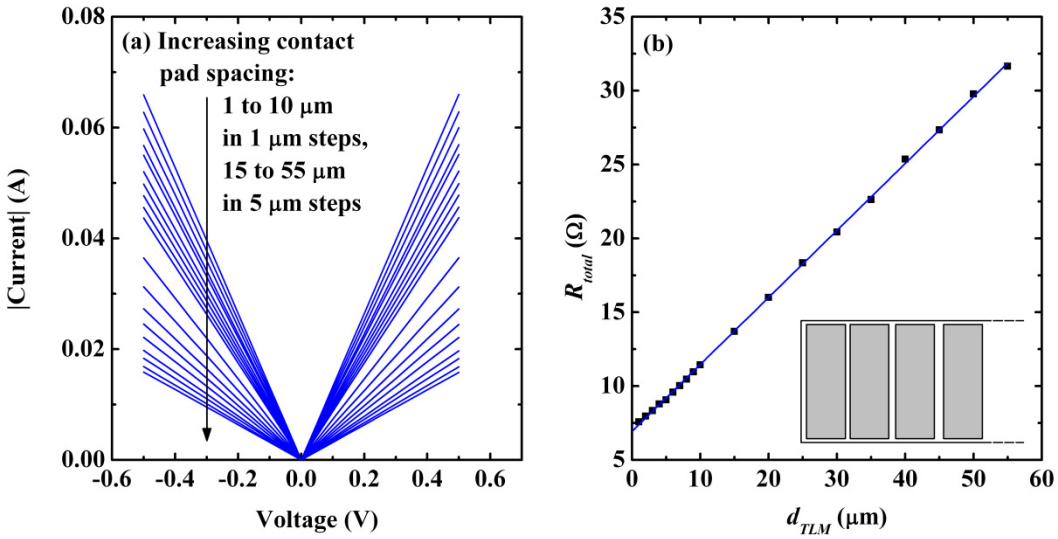

Fig. 2.7. (a) TLM *I-V* characteristics obtained for as-deposited Pd, and (b) the resulting plot of total resistance R_{total} versus TLM contact pad spacing d_{TLM}, from which contact resistance and specific contact resistivity values can be derived. The inset shows a schematic of the TLM structure, with the contact pads represented by gray rectangles (100-nm-thick Ni pads on top of the contact pads are not shown). Probing is done on two adjacent pads.

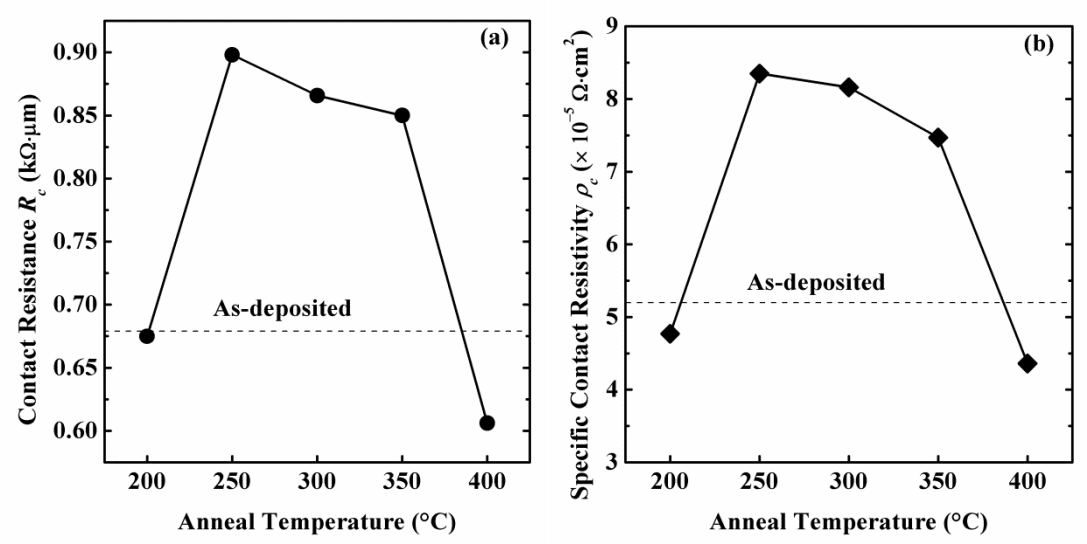

Fig. 2.8. (a) Contact resistance R_c and (b) specific contact resistivity ρ_c versus anneal temperature for Pd-InGaAs. Anneal time is fixed at 60 s.

2.3 IN-DEPTH CHARACTERIZATION OF PD-INGAAS

From the study of the reaction between Ti, Co, and Pd with InGaAs, Pd appears to be a better candidate for reaction with InGaAs to form salicide-like S/D contact metallization in InGaAs MOSFETs. Ti showed little or no reaction with InGaAs, while Co completely reacts with InGaAs at 350 °C to form a Co-InGaAs alloy with a rough interface with InGaAs. Further work on Co-InGaAs was done by a fellow student and is reported in Ref. [176]. Co-InGaAs is also studied and reported by another group in Ref. [177]. Pd, on the other hand, completely reacts with InGaAs at temperatures as low as 200 °C and possibly below, thereby requiring a lower thermal budget. The resulting Pd-InGaAs film also has superior smoothness, uniformity, interfacial quality, and contact resistivity than Co-InGaAs.

Therefore, Pd-InGaAs is studied in greater detail in this Chapter. Four-point probe measurements were done to extract sheet resistance, while X-ray and ultra-

violet photoelectron spectroscopy (XPS and UPS, respectively) were carried out on Pd-InGaAs formed at 250 °C. InGaAs MOSFETs featuring Pd-InGaAs S/D contacts formed by a salicide-like process were fabricated in collaboration with another fellow student, and are reported in Ref. [178]. Scanning electron microscopy (SEM) and TEM images of one such device are shown in Fig. 2.9 [178]. The TEM was done at the Institute of Materials Research and Engineering (IMRE) as a paid service.

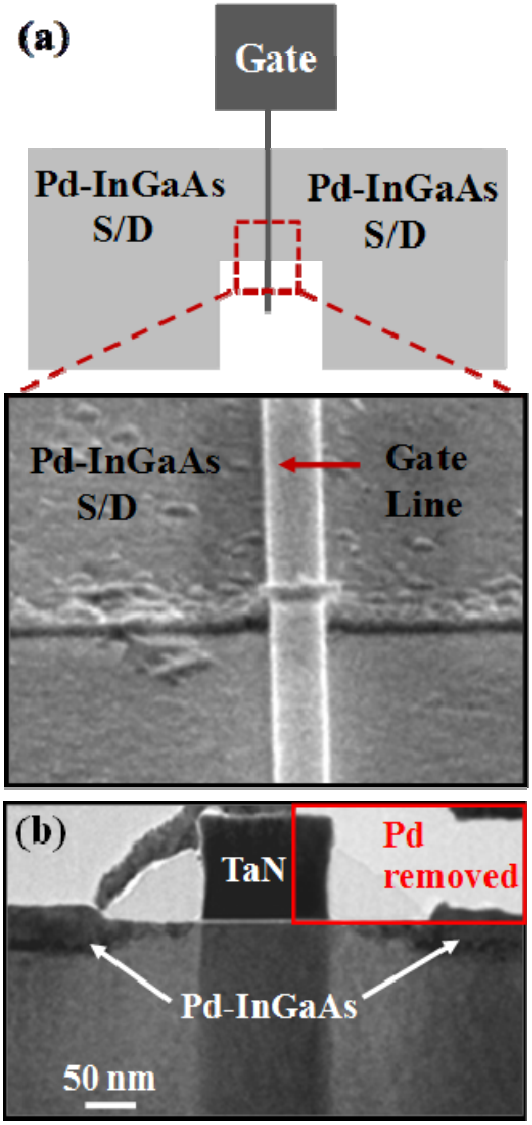

Fig. 2.9. (a) SEM and (b) TEM images of an InGaAs MOSFET with Pd-InGaAs S/D contacts formed by a salicide-like process [178]. The red box in (b) overlays a TEM image with the unreacted Pd removed from the gate and spacer.

2.3.1 Sheet resistance analysis

Sheet resistance R_{sheet} was measured using micro four-point probes (μ-4PP) with 10 μm probe spacing, which allows accurate measurement of the film alone for films as thin as 10 nm. To examine the uniformity of the Pd-InGaAs film, a fresh blanket sample was prepared for Pd-InGaAs (20 nm thick) formed at 250 °C. Measurements of R_{sheet} were carried out on this sample in an 11 × 11 array of points with 100 μm step size, covering an area of 1 mm × 1 mm. The step size of 100 μm is much larger than the μ-4PP's inter-probe spacing of 10 μm. The box plot of R_{sheet} is shown in Fig. 2.10, with a mean of 77.3 Ω/square. The R_{sheet} values have a tight distribution, with a very small standard deviation of 1.04 Ω/square, underlining the very good uniformity seen in the TEM images.

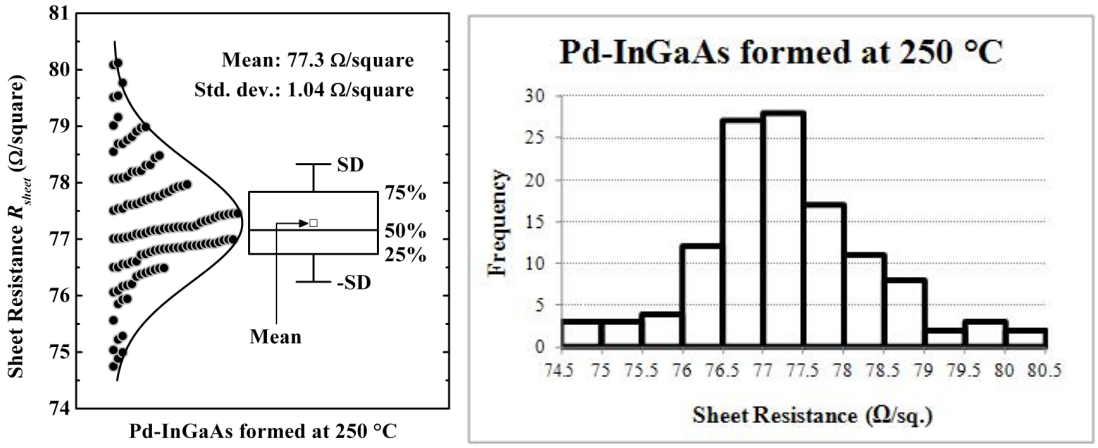

Fig. 2.10. Box plot and frequency distribution of R_{sheet} values for a 20-nm-thick Pd-InGaAs blanket sample formed by annealing at 250 °C for 60 s. The R_{sheet} values were measured in an 11 × 11 array of points with 100 μm step size, covering an area of 1 mm × 1 mm.

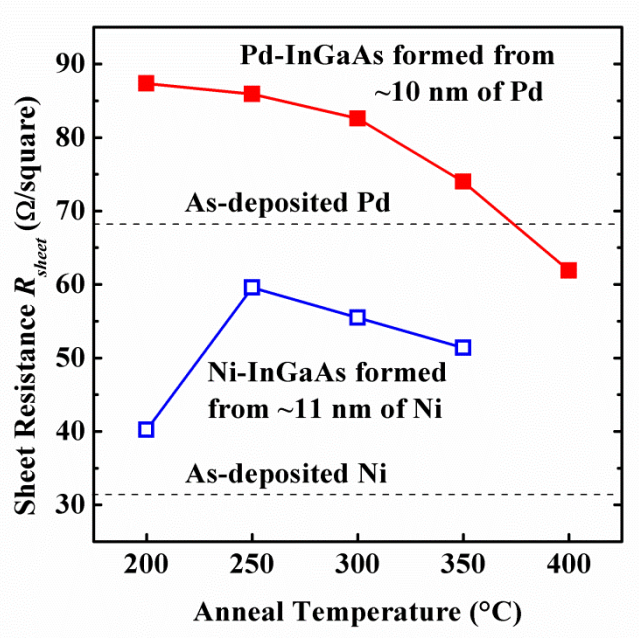

Fig. 2.11. Sheet resistance R_{sheet} versus anneal temperature for ~20 nm of Pd-InGaAs formed from ~10 nm of Pd. Anneal time is fixed at 60 s. The values for ~19 nm of Ni-InGaAs formed from ~11 nm of Ni on $In_{0.53}Ga_{0.47}As$ with the same doping concentration are also plotted for comparison.

The measured R_{sheet} of the metal film for various annealing conditions is plotted in Fig. 2.11. The mean of 77.3 Ω/square obtained in Fig. 2.10 for Pd-InGaAs formed at 250 °C is 10% lower than that in Fig. 2.11, due to run-to-run variation. It is observed that Pd-InGaAs has higher R_{sheet} than as-deposited Pd despite having twice the thickness. The Pd-InGaAs R_{sheet} decreases as its formation temperature increases, possibly due to the formation of different phases and/or polycrystalline film, as well as larger film thickness at higher temperatures.

For comparison, Ni-InGaAs data is also plotted in Fig. 2.11. The Ni-InGaAs blanket samples were fabricated the same way as the Pd-InGaAs samples, and the Ni-InGaAs formed from ~11 nm of Ni is ~19 nm thick, which is close in thickness to the ~20 nm of Pd-InGaAs formed from ~10 nm of Pd, allowing a fair comparison of R_{sheet}.

It can be seen that Pd-InGaAs formed by a 60 s anneal at 250 °C has an R_{sheet} that is ~44% higher than that of Ni-InGaAs formed by the same anneal conditions.

2.3.2 XPS analysis

XPS was performed by our collaborators Dr. Jisheng Pan and Dr. Zheng Zhang at IMRE. The XPS was done on bulk Pd-InGaAs (30 nm thick) formed by 250 °C anneal (Fig. 2.12). *In-situ* sputtering was done prior to XPS analysis to remove native oxide from the Pd-InGaAs surface. No shift was observed for In 3d and Ga 2p peaks. However, the Pd $3d_{5/2}$ peak in Pd-InGaAs shifted by 0.9 eV with respect to that in elemental Pd (335.1 eV), and a significant shift of 1.2 eV was observed in the As 3d peaks in Pd-InGaAs with respect to bulk $In_{0.53}Ga_{0.47}As$ substrate. These indicate the formation of new bonds, thus confirming the reaction between Pd and $In_{0.53}Ga_{0.47}As$.

The atomic ratio of Pd:In:Ga:As was extracted from the XPS data for Pd-InGaAs formed at 250 °C by integrating the area under the respective peaks of the various elements. As the XPS spot size is 400 μm, which is much bigger than the EDX spot size of 10 nm, XPS provides an atomic ratio that is averaged over a larger area. Pd $3d_{5/2}$, In $3d_{5/2}$, and Ga $2p_{3/2}$ peaks, together with either As $3d_{5/2}$ or As $2p_{3/2}$ peaks, were used. The As $3d_{5/2}$ signal provides information from a larger depth, while the As $2p_{3/2}$ signal is more surface-sensitive. Using the As $3d_{5/2}$ peak gives a Pd:In:Ga:As atomic ratio of ~57:10:21:12, which agrees quite well with the atomic ratio of ~58:9:14:19 obtained from EDX. This is to be expected, since the EDX data was obtained from the middle of the Pd-InGaAs film. On the other hand, using the As $2p_{3/2}$ peak gives a Pd:In:Ga:As atomic ratio of ~49:8:18:25. The Pd atomic percentage therefore appears to be higher deeper in the film than near the surface,

which could indicate that Pd is the main diffusing species in the reaction between Pd and InGaAs. A higher atomic percentage of As nearer the surface suggests possible segregation of As towards the surface, while the dissimilarity between the In:Ga ratio in the Pd-InGaAs film and that in the $In_{0.53}Ga_{0.47}As$ substrate could be due to In segregation, as seen in Ni-InGaAs formation [137], or Ga out-diffusion from InGaAs.

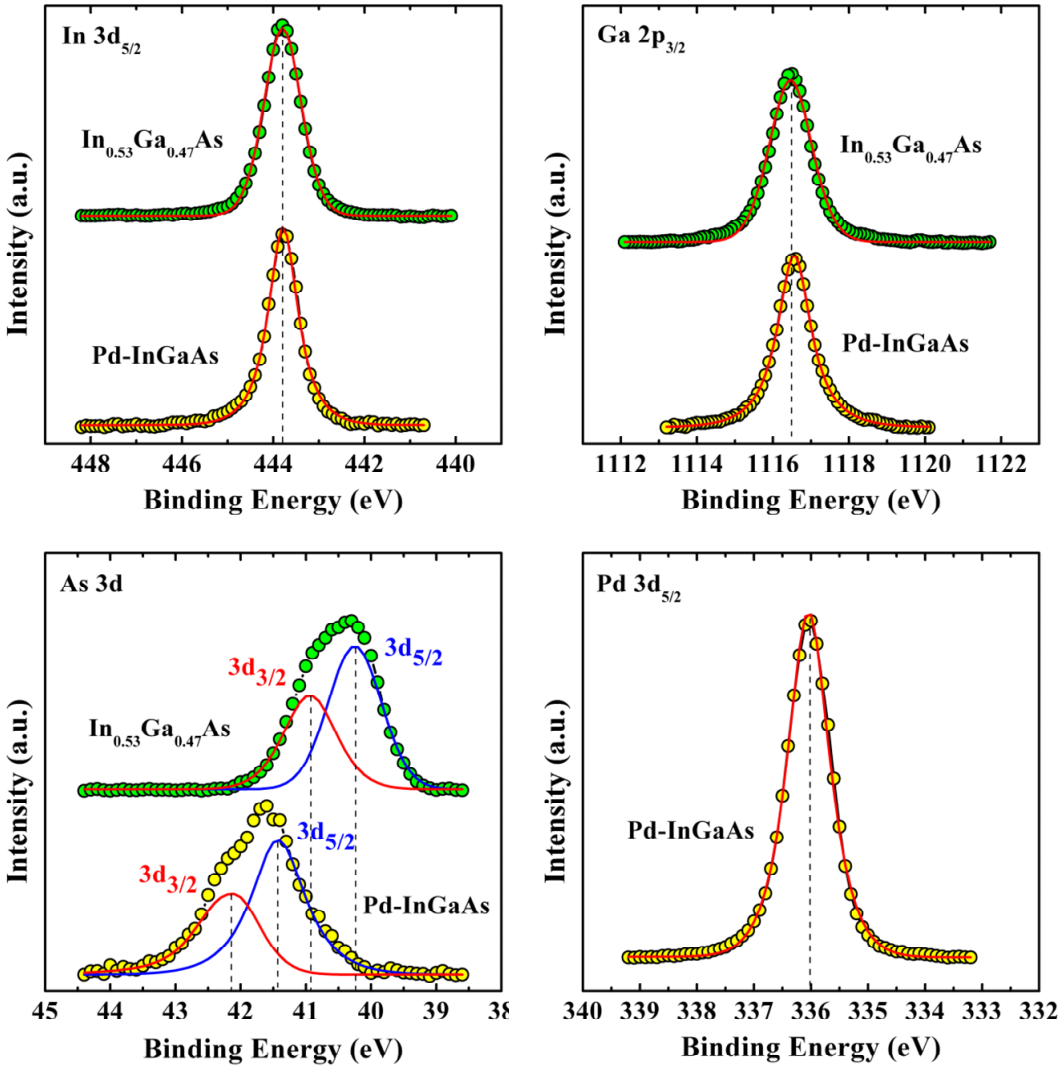

Fig. 2.12. XPS spectra of bulk Pd-InGaAs (30-nm-thick) formed by 250 °C 60 s anneal. The Pd $3d_{5/2}$ peak in Pd-InGaAs is shifted 0.9 eV away from the Pd $3d_{5/2}$ peak position of 335.1 eV in elemental Pd. As 3d peaks indicate a shift of 1.2 eV in As $3d_{3/2}$ and $3d_{5/2}$ peaks in Pd-InGaAs from those in bulk $In_{0.53}Ga_{0.47}As$.

2.3.3 UPS analysis

UPS is a technique that can be used to measure the work function of materials [179]-[180]. The work function of a metal is important in determining the Schottky barrier height, though the Schottky barrier height also depends on other factors such as Fermi level pinning and the presence of interfacial layers. UPS was carried out by Dr. Jisheng Pan and Dr. Zheng Zhang at IMRE on 30-nm-thick Pd-InGaAs formed at 250 °C, using He I radiation with photon energy of 21.2 eV. As with XPS, *in-situ* sputtering was done prior to UPS analysis to remove native oxide from the Pd-InGaAs surface. The sample was biased at -5 V in order for the electrons to have enough energy to overcome the work function of the UPS spectrometer.

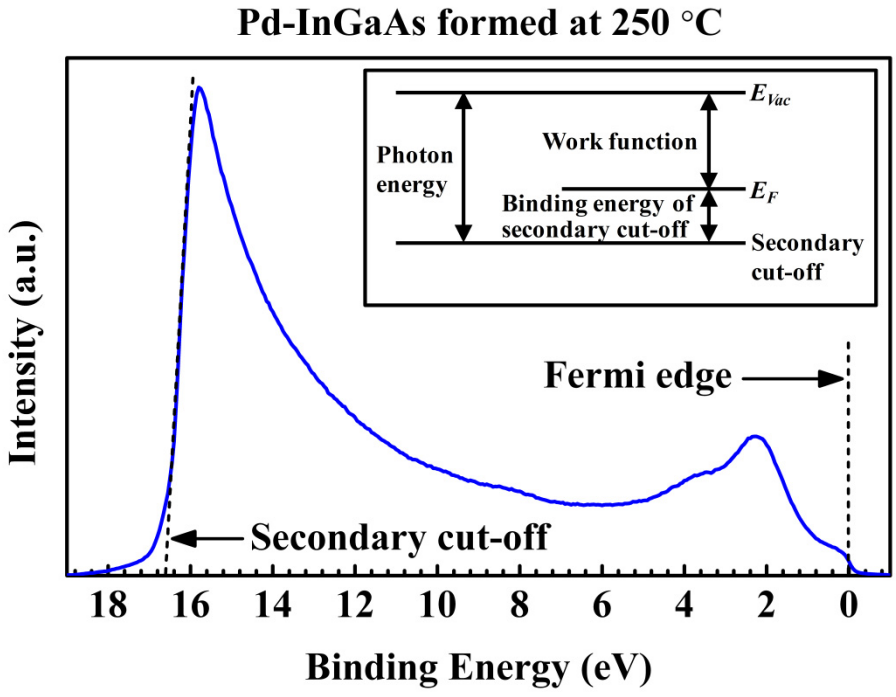

Fig. 2.13. He I UPS spectrum of 30-nm-thick Pd-InGaAs formed from 15 nm of Pd on $In_{0.53}Ga_{0.47}As$ by RTA at 250 °C for 60 s. The photon energy is 21.2 eV and the bias voltage is -5 V. The spectrum is plotted such that the Fermi edge is at zero binding energy.

The resulting UPS spectrum after background removal is shown in Fig. 2.13, which has been plotted such that the Fermi edge is at zero binding energy. For a metal like Pd-InGaAs, electrons can be detected starting from the Fermi edge. This is in contrast to a semiconductor, where the electrons with the highest energy are from the valence band maximum, which is lower than the Fermi level (i.e. at higher binding energy) for non-degenerate doping.

Because only filled energy states can emit photo-electrons, the Fermi edge shows up as a step, since the Fermi level E_F is the boundary between filled and empty states, with states above the Fermi level being empty while states below the Fermi level are filled. Therefore, the Fermi edge marks the onset of photoemission of electrons for metals. On the other hand, the secondary cut-off marks the end of the spectrum and represents electrons that have just enough energy to escape from the surface and reach the vacuum level E_{Vac}. The work function of the metal can therefore be derived by subtracting the horizontal axis intercept of the secondary cut-off (with the Fermi edge at zero binding energy) from the photon energy, as illustrated in the inset of Fig. 2.13. For the UPS spectrum in Fig. 2.13, the secondary cut-off intersects the horizontal axis at ~16.6 eV. With a photon energy of 21.2 eV, this gives a work function of ~4.6 ± 0.1 eV for Pd-InGaAs formed at 250 °C, placing its Fermi level quite close to the conduction band minimum of $In_{0.53}Ga_{0.47}As$. The work function of Pd, in contrast, is larger at 5.12 eV [174]. Pd-InGaAs formed at 250 °C is therefore expected to have lower contact resistivity than Pd, even in the presence of Fermi level pinning, but this is not the case (Fig. 2.8). A possible reason is the presence of other interfacial layers (e.g. excess elemental In, Ga, or As) at the Pd-InGaAs/InGaAs interface after the reaction between Pd and InGaAs, and requires further investigation.

2.3.4 Benchmarking with Ni-InGaAs

The contact resistivity of Pd-InGaAs is expected to reduce for higher substrate doping concentrations, and could approach the value of ~1×10^{-6} Ω·cm^2 obtained for Ni-InGaAs formed at 250 °C on n^{++} $In_{0.53}Ga_{0.47}As$ with doping concentration of ~5×10^{19} cm^{-3} [136]-[137]. Fig. 2.14 presents a benchmark of the contact resistivities obtained at various active donor concentrations N_d for Ni-InGaAs and Pd-InGaAs, which were formed by reaction of Ni or Pd, respectively, with $In_{0.53}Ga_{0.47}As$ at 250 °C for 60 s. Table 2.1 compares their formation temperature, work function, and sheet resistance. As the contact resistivity of Pd-InGaAs on $In_{0.53}Ga_{0.47}As$ ($N_d \approx 2\times10^{18}$ cm^{-3}) is lower than that of Ni-InGaAs on $In_{0.53}Ga_{0.47}As$ ($N_d \approx 1\times10^{18}$ cm^{-3}), Pd-InGaAs could have a Schottky barrier height that is lower than the value of 0.239 ± 0.01 eV reported for Ni-InGaAs [139].

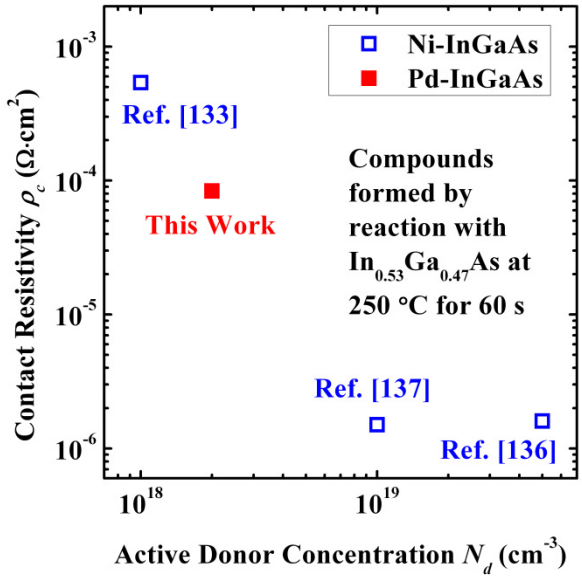

Fig. 2.14. Benchmarking of the contact resistivities obtained for Ni-InGaAs and Pd-InGaAs formed on $In_{0.53}Ga_{0.47}As$ with different active doping concentrations. Ni-InGaAs and Pd-InGaAs were formed by reacting Ni and Pd, respectively, with $In_{0.53}Ga_{0.47}As$ by RTA at 250 °C for 60 s.

Table 2.1. Comparison of Ni-InGaAs and Pd-InGaAs formed by RTA at 250 °C for 60 s.

	Metal *M*	
	Ni	**Pd**
Min. temperature for reaction with $In_{0.53}Ga_{0.47}As$	250 °C	200 °C (possibly lower)
M*-InGaAs **work function**	~5.1 eV (Ref. [129])	~4.6 eV
M*-InGaAs R_{sheet}	~60 Ω/square (~19 nm)	~77.3 Ω/square (~20 nm)

* *M*-InGaAs formed by RTA at 250 °C for 60 s.

2.4 CONCLUSIONS

Ti, Co, and Pd were investigated as possible candidates for the formation of salicide-like contact metallization in $In_{0.53}Ga_{0.47}As$ MOSFETs. While Ti does not appear to react with $In_{0.53}Ga_{0.47}As$ at temperatures up to 400 °C, Co completely reacts at 350 °C to form Co-InGaAs, and Pd completely reacts at 200 °C to form Pd-InGaAs. Co-InGaAs has a rough interface with InGaAs, while Pd-InGaAs films formed at 200 and 250 °C show excellent smoothness, uniformity and interfacial quality. The work function of the Pd-InGaAs formed at 250 °C was extracted to be ~4.6 ± 0.1 eV, and its sheet resistance at a thickness of 20 nm and its contact resistivity on n-type $In_{0.53}Ga_{0.47}As$ with ~2×10^{18} cm^{-3} doping concentration were determined to be ~77.3 Ω/square and ~8.35×10^{-5} Ω·cm^2, respectively. Further work on selective etching of

Pd over Pd-InGaAs is needed for further development and improvement of the salicide-like process used to form Pd-InGaAs contact metallization in InGaAs MOSFETs. Contact resistivity reduction by a few orders of magnitude is also required for Ni-InGaAs, Pd-InGaAs, and Co-InGaAs contact metallization in order to be competitive with Mo non-self-aligned contacts.

In the next Chapter, simulations are used to compare salicide-like contact metallization with non-self-aligned contact metallization in InGaAs MOSFETs and determine the level of contact resistivity required to meet performance targets at advanced sub-20 nm technology nodes.

Chapter 3

Self-Aligned and Non-Self-Aligned Contact Metallization in InGaAs Metal-Oxide-Semiconductor Field-Effect Transistors: A Simulation Study

3.1 INTRODUCTION

Self-aligned silicide-like (salicide-like) source/drain (S/D) contact metallization for InGaAs n-channel metal-oxide-semiconductor field-effect transistors (n-MOSFETs) was explored in the previous Chapter. The reaction of Ti, Co, and Pd with InGaAs was studied, with detailed characterization and analysis of Pd-InGaAs, adding on to reports on Ni-InGaAs salicide-like contact metallization [122]-[141]. This Chapter continues the work in the preceding Chapter by examining the continued need for such self-aligned contact metallization at highly scaled dimensions, as well as the values of contact resistivity ρ_c demanded by the performance targets laid out in the International Technology Roadmap for Semiconductors (ITRS) [181] for advanced technology nodes.

This is done by using two-dimensional (2D) simulations to compare the drive current performance of $In_{0.53}Ga_{0.47}As$ n-channel MOSFETs (n-MOSFETs) with self-aligned metallization (SAM) and those with non-self-aligned metallization (NSAM) for various gap sizes d between the via and the gate, and for various values of ρ_c at the interface between the contact metallization and the S/D region. It should be emphasized that the SAM refers to the contact metallization, and should not be

confused with self-aligned contact plugs or vias defined as SAC [182]. III-V MOSFETs are projected to be used in production in year 2018 and beyond, where the gate length L_G would be ~15 nm or smaller for III-V/Ge logic [181]. $In_{0.53}Ga_{0.47}As$ n-MOSFETs with L_G of 15 nm are therefore simulated, with efforts made to ensure that they are representative of the actual devices as projected by the ITRS for III-V high-performance logic technology [181].

3.2 SIMULATION DETAILS

Fig. 3.1 shows the structures studied: $In_{0.53}Ga_{0.47}As$ n-MOSFETs employing either SAM or NSAM. The simulations, which are carried out using the Technology Computer Aided Design (TCAD) simulator Synopsys Sentaurus, self-consistently solve the non-linear Poisson equation and the current continuity equation for electrons.

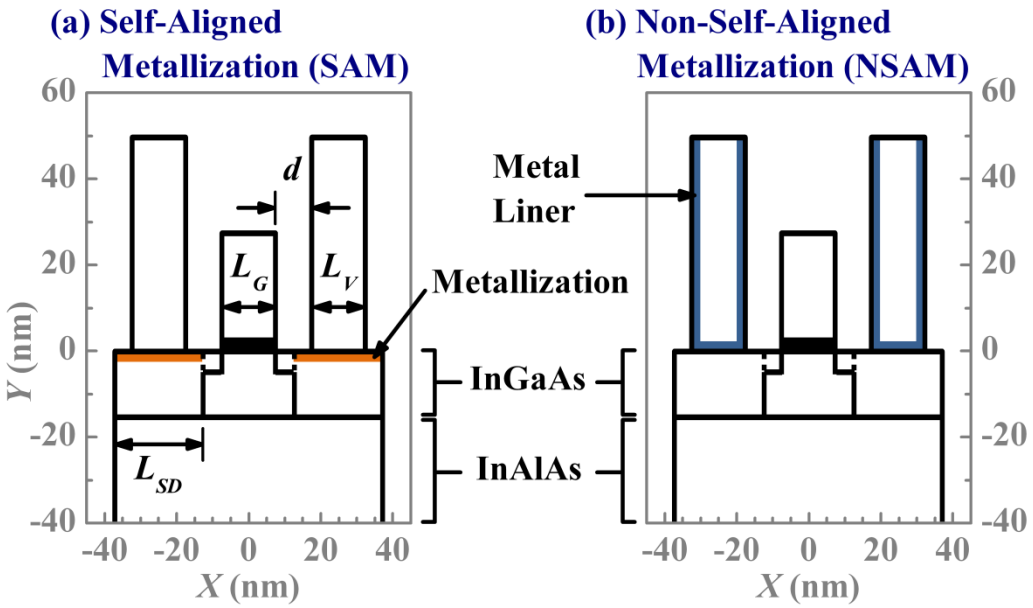

Fig. 3.1. Simulated n-MOSFETs with L_G of 15 nm, having (a) self-aligned metallization (SAM) or (b) non-self-aligned metallization (NSAM). The SAM is a 2.5-nm-thick salicide-like metallization (which may be Ni-InGaAs), while the NSAM is a 2.5-nm-thick metal layer (which may be Mo) lining the tungsten via.

The interface between the contact metallization (SAM or NSAM) and the S/D region is modeled as an Ohmic metal-semiconductor interface with a specified ρ_c (in $\Omega \cdot cm^2$). ρ_c is a variable that ranges from 1×10^{-9} to 1×10^{-7} $\Omega \cdot cm^2$. The Philips Unified Mobility Model [183] is used to account for phonon, impurity, and carrier-carrier scattering mechanisms as well as screening of ionized impurities by charge carriers. Dependence of the carrier mobility on the electric field perpendicular to the gate oxide is also accounted for through simultaneous use of a field-dependent mobility model [184].

The SAM is a salicide-like metallization (which may be Ni-InGaAs) that is recessed into the S/D, while the NSAM consists of a metal layer (which may be Mo) lining the tungsten via. The thickness t_{SAM} of the SAM is 2.5 nm, which is half the junction depth of the S/D extension (SDE). The electrical resistivity of the SAM material is chosen to be 1.8×10^{-4} $\Omega \cdot cm$, matching that of Ni-InGaAs. Mo is an attractive material for the NSAM because it has very low ρ_c of 1.3×10^{-8} and 1.1×10^{-8} $\Omega \cdot cm^2$ on n-type $In_{0.53}Ga_{0.47}As$ with active doping concentration of 3.6×10^{19} and 6×10^{19} cm^{-3}, respectively [144]-[145]. Therefore, the electrical resistivity of Mo is used for the metal liner in the NSAM. The via diameter L_V is fixed at 15 nm for both SAM and NSAM.

The S/D doping concentration of 5×10^{19} cm^{-3} is close to the highest electron concentration that can be obtained for *in-situ* Si-doped $In_{0.53}Ga_{0.47}As$ [147]. The maximum electron mobility μ_{max} in the Philips Unified Mobility Model takes the value of the electron mobility in bulk $In_{0.53}Ga_{0.47}As$ (12000 $cm^2/V \cdot s$), while the minimum electron mobility μ_{min} is set at 1000 $cm^2/V \cdot s$. Based on these values of μ_{max} and μ_{min}, the concentration-dependent electron mobility in the S/D works out to be ~1140 $cm^2/V \cdot s$. This compares well with experimentally obtained electron mobility

values of 1266 and 740 $cm^2/V{\cdot}s$ at active doping concentrations of 3.6×10^{19} and 6×10^{19} cm^{-3}, respectively [144]-[145].

The length of the S/D regions is denoted by L_{SD}. Gap sizes d of 10, 15, and 20 nm between the via and the gate are simulated. In CMOS technology scaling, all the device dimensions are scaled down. Therefore, L_{SD} scales together with d, with the via kept centered in the S/D region, as illustrated in Fig. 3.2. However, all other dimensions are kept constant as d and L_{SD} are varied, as the focus of this study is the effect of d and ρ_c on III-V MOSFET performance for SAM and NSAM.

Table 3.1 summarizes the key parameters of the simulation. A very fine mesh size of 0.1-0.5 Å was used in the top 2 Å of the channel just below the gate oxide, while a fine mesh size of 0.5-1 nm was used for the rest of the channel, as well as the SDE, S/D, and contact regions. A larger mesh size of 5-10 nm was used in the other parts of the structure. Simulation results were checked for independence of mesh size.

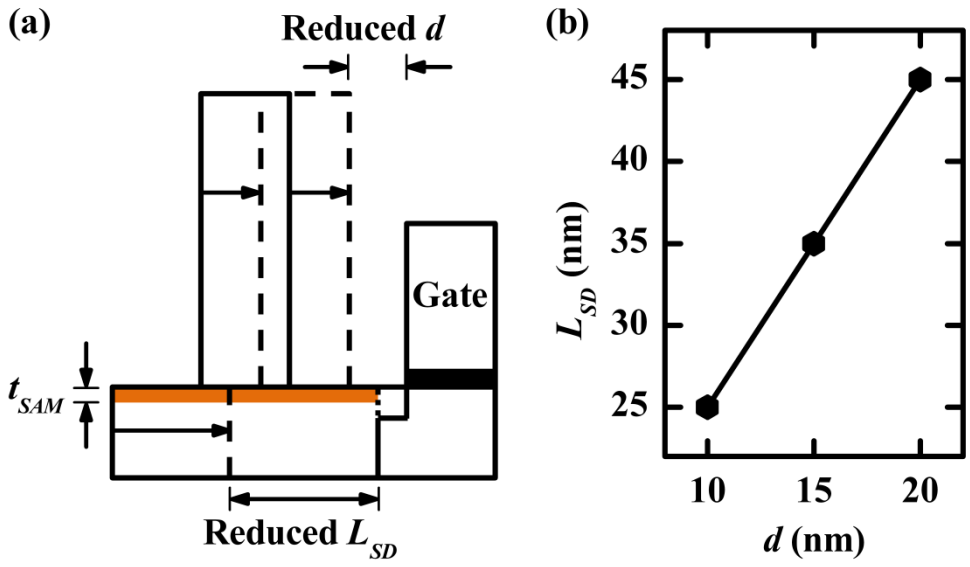

Fig. 3.2. (a) Schematic illustrating the scaling of S/D length L_{SD} with spacing d between the via and the gate edge, with the via kept centered in the S/D region. (b) Values of L_{SD} for each value of d.

Table 3.1. Key parameters used in the simulations.

Philips Unified Mobility Model	
Max. electron mobility, μ_{max} ($cm^2/V{\cdot}s$)	12000
Min. electron mobility, μ_{min} ($cm^2/V{\cdot}s$)	1000

TaN/HfO_2 Gate Stack and Tungsten Via	
TaN work function (eV)	4.65
HfO_2 ($\kappa = 22$) physical thickness (nm)	3
Via diameter, L_V (nm)	15

Self-Aligned Contact Metallization	
Thickness, t_{SAM} (nm)	2.5
Electrical resistivity ($\Omega{\cdot}cm$)	1.8×10^{-4}

Non-Self-Aligned Contact Liner	
Thickness, t_{NSAM} (nm)	2.5
Electrical resistivity ($\Omega{\cdot}cm$)	4.9×10^{-6}

n^{++} $In_{0.53}Ga_{0.47}As$ S/D	
Depth (nm)	15
Doping conc. (cm^{-3})	5×10^{19}

n^{+} $In_{0.53}Ga_{0.47}As$ SDE	
Depth (nm)	5
Length (nm)	5
Doping conc. (cm^{-3})	5×10^{18}

$In_{0.53}Ga_{0.47}As$ Channel	
Thickness (nm)	15
Undoped in top 5 nm, p-type (5×10^{18} cm^{-3}) in remaining 10 nm	

p^{+} $In_{0.52}Al_{0.48}As$ Barrier	
Doping conc. (cm^{-3})	5×10^{18}

3.3 RESULTS AND DISCUSSION

Fig. 3.3 plots drain current I_d versus gate voltage V_g at drain voltage V_d of 0.05 and 0.63 V for $In_{0.53}Ga_{0.47}As$ n-MOSFETs having SAM or NSAM, with d = 10 nm and with various values of ρ_c. The source is grounded for all simulations. MOSFETs with SAM and NSAM exhibit identical subthreshold and OFF-state characteristics, and their I_d-V_g curves overlap in the subthreshold regime for various values of d (not shown) and ρ_c (Fig. 3.3). Hence, I_d can be compared at the same OFF-state current I_{off} for SAM and NSAM with various values of d and ρ_c. Subthreshold swing S is ~95 mV/decade and drain-induced barrier lowering (DIBL) is ~0.16 V/V, as calculated by the equations:

$$S = \frac{dV_g}{d(\log I_d)} = \left[\frac{d(\log I_d)}{dV_g}\right]^{-1} \qquad (V_g < V_t) \quad , \tag{3.1}$$

$$\text{DIBL} = \frac{V_{t,lin} - V_{t,sat}}{V_{d,sat} - V_{d,lin}} \quad , \qquad (3.2)$$

where V_t is the threshold voltage, $V_{t,lin}$ and $V_{t,sat}$ are the linear and saturation threshold voltages respectively, and $V_{d,sat}$ and $V_{d,lin}$ are the saturation and linear drain biases respectively. Using the constant current method with a fixed current level of 10 μA/μm gives a $V_{t,sat}$ of ~0.18 V that is independent of d and ρ_c.

Simulated I_d (at $V_g = V_d = 0.63$ V) versus ρ_c for various values of d is plotted in Fig. 3.4 for both SAM and NSAM. Curves with the same symbol shape (square, circle, or triangle) represent the same d. Data points for SAM and NSAM are plotted using solid and open symbols, respectively. For each value of d in Fig. 3.4, I_d increases when ρ_c is reduced for both SAM and NSAM, with diminishing gains as the

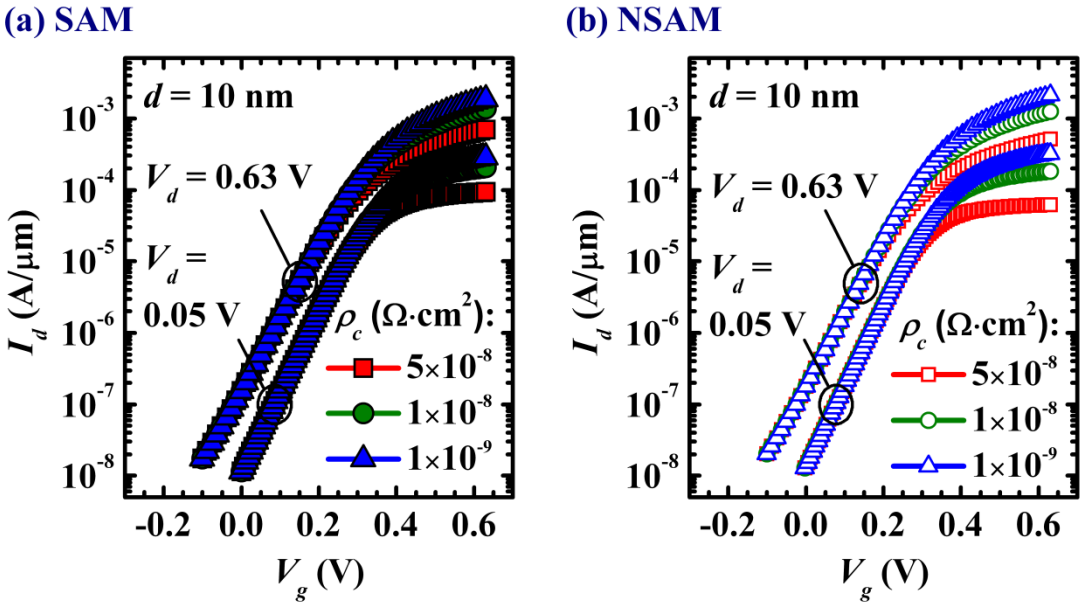

Fig. 3.3. I_d-V_g curves of $In_{0.53}Ga_{0.47}As$ MOSFETs having (a) SAM or (b) NSAM with d = 10 nm and with various values of ρ_c, showing identical subthreshold and OFF-state characteristics ($S \approx 95$ mV/decade, DIBL ≈ 0.16 V/V, $V_{t,sat} \approx 0.18$ V). $V_{t,sat}$ is determined by the constant current method with a fixed current level of 10 μA/μm.

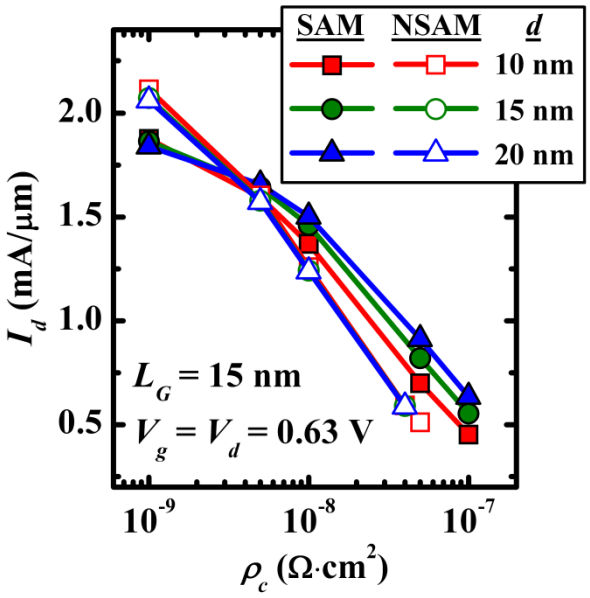

Fig. 3.4. Drive current comparison of SAM and NSAM with various values of d and ρ_c. Compared to NSAM with the same d, SAM gives higher I_d at ρ_c larger than ~5×10^{-9} Ω·cm^2 due to larger A_{eff} and lower $R_{c,eff}$, but lower I_d at smaller ρ_c due to higher spreading resistance induced by its recessed geometry.

contact resistance becomes less limiting. It is noted that at low ρ_c of 1×10^{-9} Ω·cm^2, the MOSFETs with NSAM achieve ~2.1 mA/μm at supply voltage V_{dd} of 0.63 V, which, together with the L_G of 15 nm and $V_{t,sat}$ of 0.18 V, is in line with the ITRS III-V high-performance logic technology requirements [181] that were used to calibrate the mobility models.

Fig. 3.4 reveals an interesting observation for the SAM when d is varied for ρ_c larger than ~5×10^{-9} Ω·cm^2: I_d does not decrease but instead increases when d and L_{SD} are increased. This is due to the increase in effective contact area A_{eff}, which reduces the effective contact resistance $R_{c,eff}$. At this point, it is useful to introduce a characteristic length L_C similar to that in a transmission line model [185], which can be calculated by

$$L_C = \sqrt{\frac{\rho_c}{R_{sh,SD} + R_{sh,m}}} \quad , \tag{3.3}$$

where $R_{sh,SD}$ is the sheet resistance of the InGaAs S/D below the contact and $R_{sh,m}$ is the sheet resistance of the contact metallization. Note that $R_{sh,SD}$ is 20% higher for the SAM than for the NSAM, as the SAM is recessed into the S/D regions, making the n^{++} S/D regions effectively thinner. $R_{sh,m}$ is calculated by dividing the electrical resistivity of the contact metallization (see Table 3.1) by its thickness (2.5 nm for both SAM and NSAM), and does not include the W via. Fig. 3.5 shows the calculated L_C versus ρ_c for both SAM and NSAM.

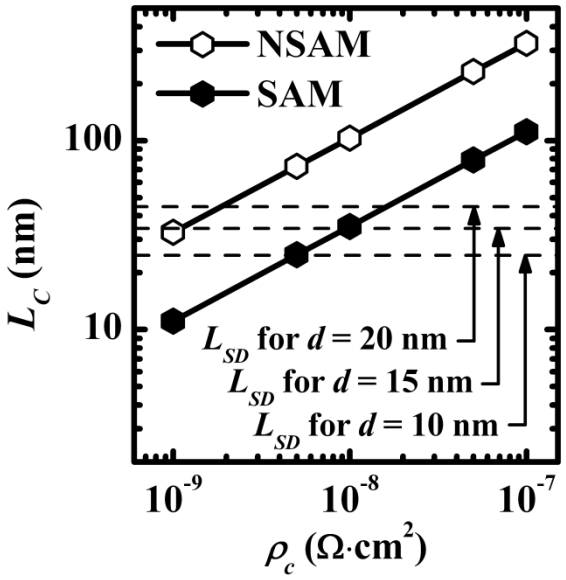

Fig. 3.5. Calculated L_C as a function of ρ_c for both SAM and NSAM. L_C increases with ρ_c, with the NSAM having larger L_C at the same ρ_c because of its lower $R_{sh,SD}$ and $R_{sh,m}$. The dashed lines indicate the values of L_{SD} for d = 10, 15, and 20 nm, which are compared with L_C for the SAM. For the NSAM, L_C is compared against L_V (= 15 nm).

It is observed that a comparison between L_C and the physical length of the contact bears significance. As the SAM spans the entire length of the S/D [Fig. 3.1(a)], its physical length is L_{SD}, which varies with d (Fig. 3.2). The SAM's A_{eff} and I_d increase with L_{SD} when its L_C is larger than its physical length L_{SD}. As shown in Fig. 3.5, for ρ_c more than or equal to 2×10^{-8} $\Omega\cdot cm^2$, the SAM has an L_C that is larger than L_{SD} at all three values of d, therefore an increase in L_{SD} as d increases from 10 to 20 nm enlarges A_{eff} and enhances I_d. At $\rho_c = 1\times10^{-8}$ $\Omega\cdot cm^2$, the SAM has an L_C that is larger than L_{SD} at d = 10 nm but equal to L_{SD} at d = 15 nm; hence, I_d benefits slightly from an increase in L_{SD} when d increases from 10 to 15 nm, but hardly increases when d increases from 15 to 20 nm. For ρ_c less than or equal to 5×10^{-9} $\Omega\cdot cm^2$, the SAM has an L_C that is smaller than L_{SD} at all three values of d, therefore negligible A_{eff} benefit is derived from any increase in L_{SD}. Based on this correlation of A_{eff} and I_d with the value of L_C relative to the physical length of the contact, the effective contact length L_{eff} can be taken to be the smaller of L_C and the physical length of the contact. The effective contact resistance $R_{c,eff}$ is then given by

$$R_{c,eff} = \frac{\rho_c}{A_{eff}} = \frac{\rho_c}{L_{eff}W} \quad , \qquad (3.4)$$

where W is the device width. W is taken to be 1 μm for $R_{c,eff}$ normalized to the device width in μm.

In contrast to the SAM, the NSAM does not enjoy an increase in A_{eff} when L_{SD} increases with d, since its physical length is determined by the fixed L_V (= 15 nm), not L_{SD} [Fig. 3.1(b)]. As its L_C is larger than L_V even at very low ρ_c of 1×10^{-9} $\Omega\cdot cm^2$ (Fig. 3.5), the NSAM's L_{eff} is equal to L_V. Therefore, A_{eff} and $R_{c,eff}$ do not change with d for the NSAM. The calculation of L_C for the NSAM without including the W via in $R_{sh,m}$ can be considered the limiting case, as including the W via would reduce $R_{sh,m}$ and make L_C even larger.

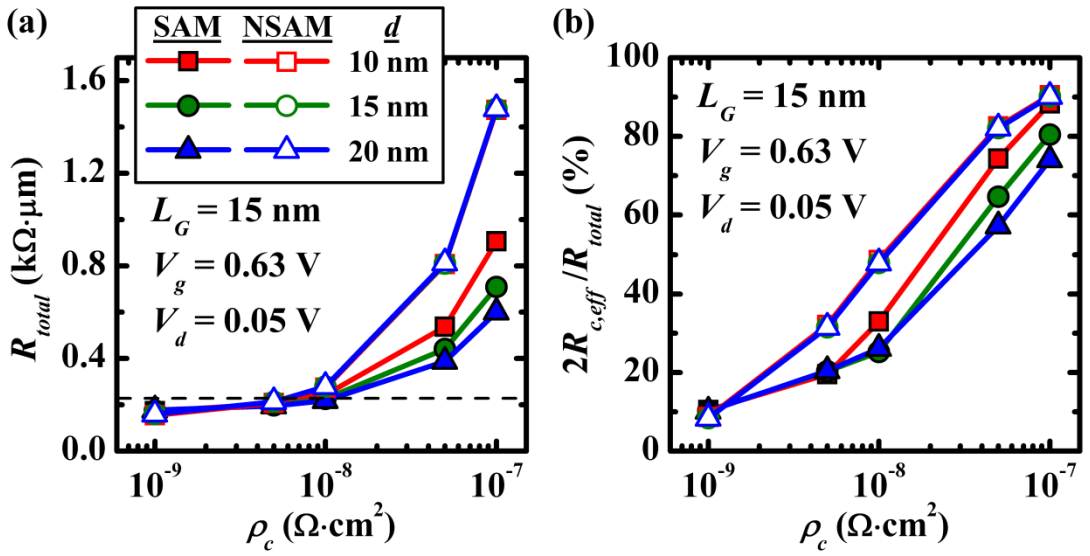

Fig. 3.6. Calculated values of (a) R_{total} from simulated results and (b) $2R_{c,eff}$ as a percentage of R_{total} as d and ρ_c are varied for both SAM and NSAM in the linear regime. Both plots share the same legend. To meet the ITRS requirement (indicated by the dashed line), the SAM should have ρ_c less than 1×10^{-8} Ω·cm^2, while the NSAM needs ρ_c less than 5×10^{-9} Ω·cm^2.

Fig. 3.6(a) plots total resistance R_{total} in the linear regime (V_g = 0.63 V, V_d = 0.05 V) versus ρ_c for both SAM and NSAM, while Fig. 3.6(b) plots total effective contact resistance $2R_{c,eff}$ as a percentage of R_{total}. $R_{c,eff}$ is calculated using (3.4), and R_{total} is given simply by V_d/I_d in the linear regime (V_g = 0.63 V, V_d = 0.05 V). As the SAM has a larger A_{eff} than the NSAM, $2R_{c,eff}$ makes up a smaller proportion of R_{total} for the SAM than for the NSAM at the same ρ_c. For the SAM, an increase in d and L_{SD} also produces a reduction in $R_{c,eff}$ for ρ_c above 1×10^{-8} Ω·cm^2. For the NSAM, $R_{c,eff}$ remains unchanged with d being varied. By taking the potential difference across the channel 0.5 nm below the gate oxide, the channel resistance R_{ch} is estimated to be ~100 Ω·μm (V_g = 0.63 V, V_d = 0.05 V). Given the ITRS requirement of 131 Ω·μm for the effective parasitic S/D series resistance for III-V high-performance logic [181], R_{total} should be lower than ~231

Ω·μm. From Fig. 3.6(a), the SAM should have ρ_c less than or equal to 1×10^{-8} Ω·cm^2, while the NSAM has a more stringent requirement of ρ_c less than or equal to 5×10^{-9} Ω·cm^2. This is due to the contact area advantage that the SAM has over the NSAM.

The SAM and NSAM curves in Fig. 3.4 intersect at ρ_c in the range of ~3×10^{-9} to ~5×10^{-9} Ω·cm^2. For ρ_c above this range, the SAM outperforms the NSAM with the same ρ_c because its larger A_{eff} gives a lower $R_{c,eff}$. Alternatively, the SAM can afford to have higher ρ_c than the NSAM for a given I_d. For ρ_c below 3×10^{-9} Ω·cm^2, the SAM gives lower I_d than the NSAM with the same ρ_c, despite being self-aligned. This is due to higher spreading resistance caused by the recessed geometry of the SAM, as schematically illustrated in Fig. 3.7.

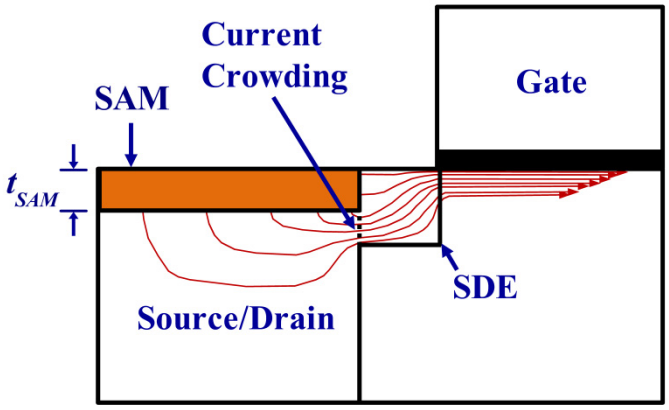

Fig. 3.7. Schematic showing the series resistance bottleneck caused by the recessed geometry of the SAM, which leads to a more severe current crowding and therefore higher spreading resistance than the NSAM. For a given SDE junction depth, a thicker SAM (larger t_{SAM}) results in a more serious current crowding problem.

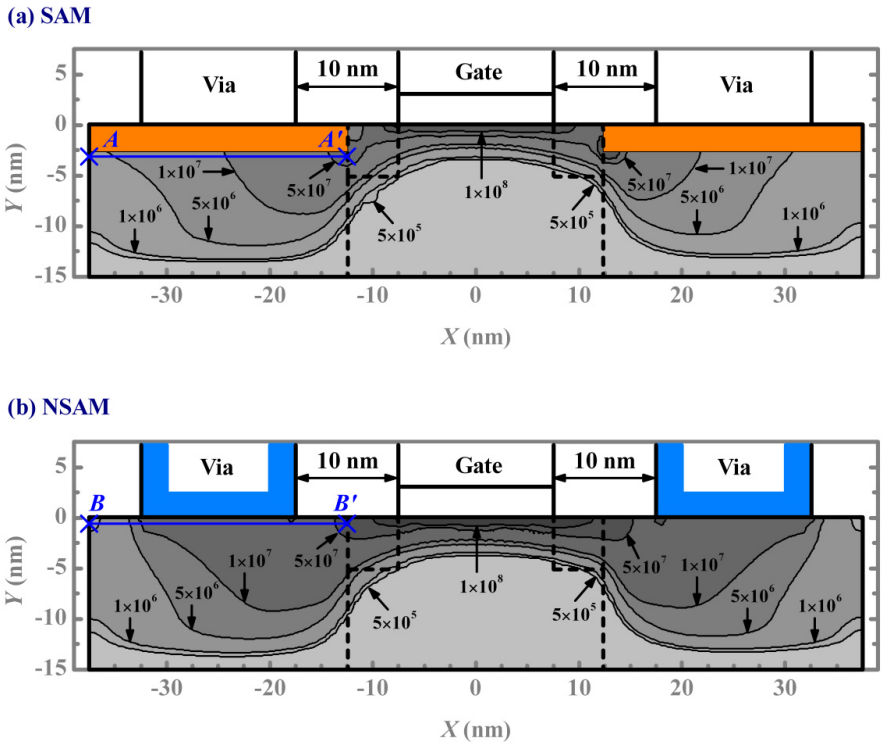

Fig. 3.8. Current density contours (V_g = V_d = 0.63 V) for SAM and NSAM with d = 10 nm and ρ_c = 1×10^{-9} Ω·cm^2. Values indicated are in A/cm^2. Lateral profiles are taken along *A-A'* and *B-B'* in the source 0.5 nm below the SAM and NSAM, respectively, for various values of d and ρ_c and plotted in Figs. 3.9 to 3.11.

Current density contours are presented in Fig. 3.8 for SAM and NSAM with d = 10 nm and ρ_c = 1×10^{-9} Ω·cm^2, illustrating the spreading of the current in the S/D regions. The SAM shows increased current density where the current flows between the S/D and the SDE regions. For the NSAM, the current in the S/D regions is confined by the via. Lateral profiles of the current density J in the source along a line 0.5 nm below the contact (indicated by *A-A'* and *B-B'* in Fig. 3.8 for SAM and NSAM, respectively) are also shown in Figs. 3.9 to 3.11 for various values of d and ρ_c. From the current density profiles with ρ_c = 1×10^{-9} Ω·cm^2, it is observed that the current density at *A'* is ~38-58% higher than at *B'* despite the SAM having ~10% lower I_d than the NSAM (Fig. 3.4). This indicates more severe current crowding for the SAM at the source edge adjacent to the source extension.

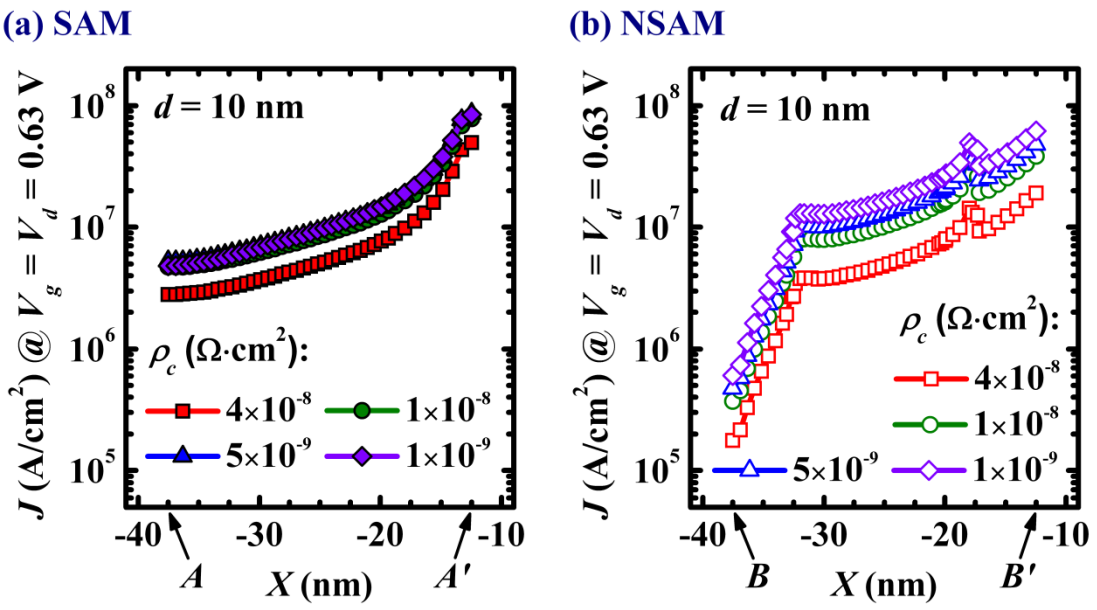

Fig. 3.9. Current density line profiles ($V_g = V_d = 0.63$ V) in the source 0.5 nm below the (a) SAM and (b) NSAM, with d = 10 nm and with various values of ρ_c. Diminishing gains can be observed as ρ_c is reduced, with the diminishing effect being smaller for the NSAM due to its larger $R_{c,eff}$.

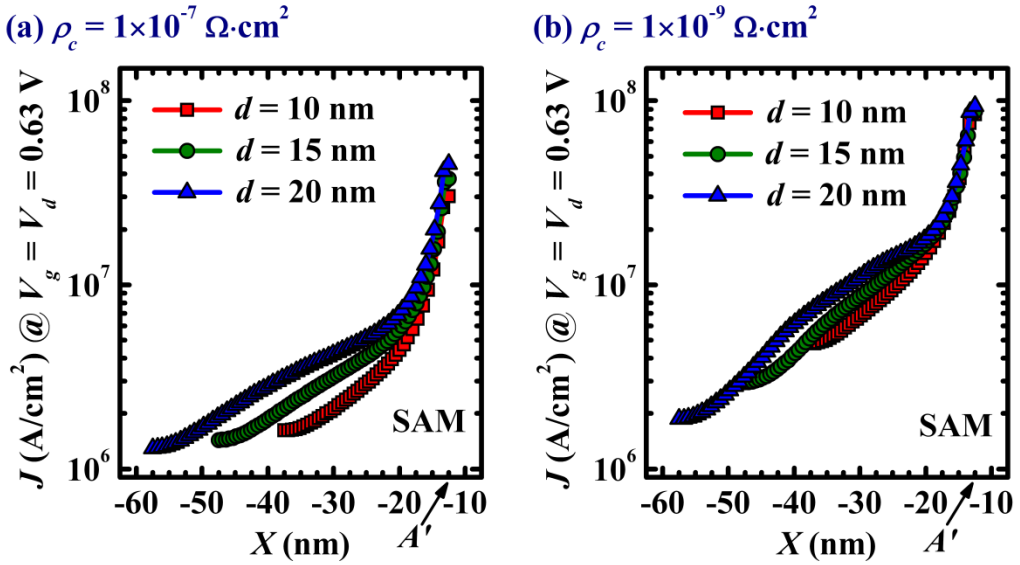

Fig. 3.10. Current density line profiles ($V_g = V_d = 0.63$ V) along *A-A'* for SAM with various values of d and with (a) $\rho_c = 1\times10^{-7}$ Ω·cm^2 and (b) $\rho_c = 1\times10^{-9}$ Ω·cm^2. The profiles with $\rho_c = 1\times10^{-7}$ Ω·cm^2 are well-separated, while those with $\rho_c = 1\times10^{-9}$ Ω·cm^2 overlap in a 5-nm-wide region adjacent to the source extension. The current density at the source edge furthest from the source extension also exhibits much smaller differences for the various values of d at $\rho_c = 1\times10^{-7}$ Ω·cm^2 than at $\rho_c = 1\times10^{-9}$ Ω·cm^2.

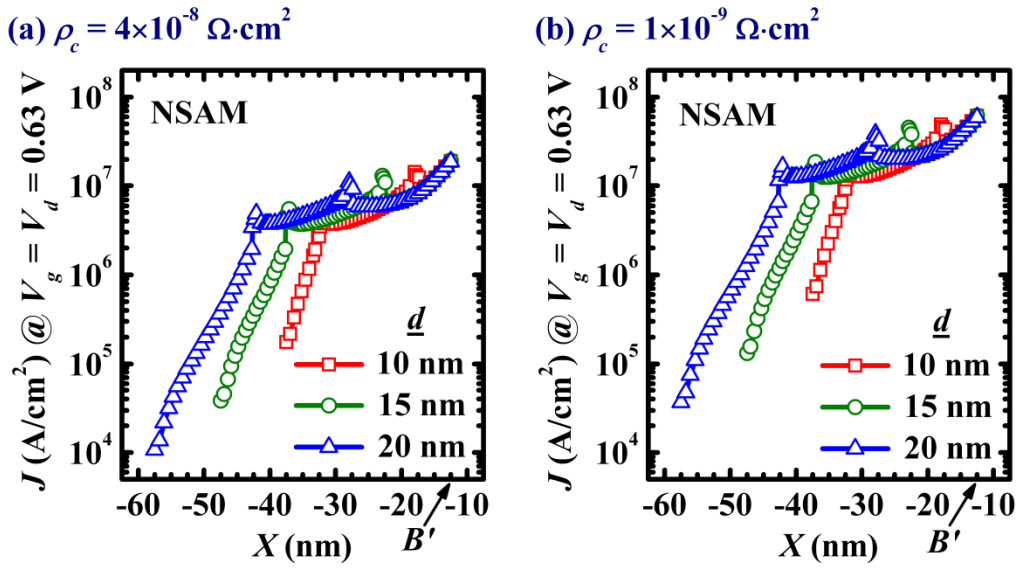

Fig. 3.11. Current density line profiles ($V_g = V_d = 0.63$ V) along *B*-*B'* for NSAM with various values of *d* and with (a) $\rho_c = 4\times10^{-8}$ Ω·cm^2 and (b) $\rho_c = 1\times10^{-9}$ Ω·cm^2. The profiles have similar shapes for both large and small ρ_c, with small current peaks at the edges of the via due to current crowding. Changes in *d* result in roughly parallel shifts of the portion of the profile below the via, which defines A_{eff}.

The observation of diminishing gains in I_d as ρ_c is reduced (Fig. 3.4) is also reflected in Fig. 3.9 where *d* is fixed at 10 nm. When ρ_c is reduced, *J* generally increases but the increment in *J* diminishes when ρ_c approaches 10^{-9} Ω·cm^2. Figs. 3.10 and 3.11 show the effect on the current density profile as *d* changes for SAM and NSAM respectively, at both high and low ρ_c. As shown in the transmission line model, the current density profile is influenced by L_C as well as the contact dimensions [185]. For the SAM with $\rho_c = 1\times10^{-7}$ Ω·cm^2 [Fig. 3.10(a)], there is clear separation between the current density profiles for the various values of *d*. However, as ρ_c is reduced, the profiles get closer and eventually overlap in a 5-nm-wide region adjacent to the source extension at ρ_c of ~1×10^{-8} Ω·cm^2 and below [Fig. 3.10(b)]. The current density at the source edge furthest from the source extension also exhibits much smaller differences for the various values of *d* at $\rho_c = 1\times10^{-7}$ Ω·cm^2 than at

$\rho_c = 1\times10^{-9}$ Ω·cm^2, suggesting that A_{eff} is limited by L_{SD} at $\rho_c = 1\times10^{-7}$ Ω·cm^2. These observations support the earlier conclusion that increases in d and L_{SD} result in larger A_{eff} and I_d for ρ_c above 1×10^{-8} Ω·cm^2, but do not appreciably increase A_{eff} and I_d for smaller ρ_c. For the NSAM (Fig. 3.11), the current density profiles have similar shapes for both larger (4×10^{-8} Ω·cm^2) and smaller (1×10^{-9} Ω·cm^2) ρ_c, with small current peaks at the edges of the via due to current crowding. Changes in d merely result in roughly parallel shifts (equal to the change in d) of the portion below the via, which defines A_{eff} for the NSAM.

The increased spreading resistance caused by the recessed geometry of the SAM can be alleviated by having a thinner SAM (Fig. 3.12), or by a raised S/D architecture as shown in Fig. 3.13. As t_{SAM} is reduced at low ρ_c of 1×10^{-8} Ω·cm^2 and below (where R_c is less dominant), I_d increases due to less current crowding and hence lower spreading resistance (Fig. 3.12).

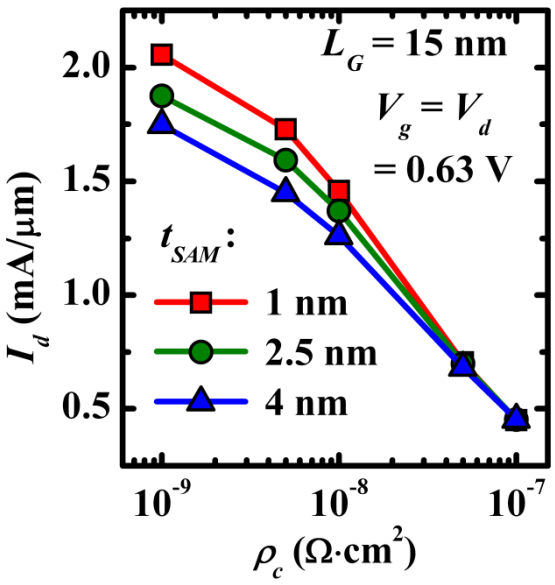

Fig. 3.12. I_d as a function of ρ_c for SAM with various t_{SAM} and with d = 10 nm. A thinner SAM results in higher I_d due to less current crowding and therefore lower spreading resistance. The effect is bigger at low ρ_c, where R_c does not dominate.

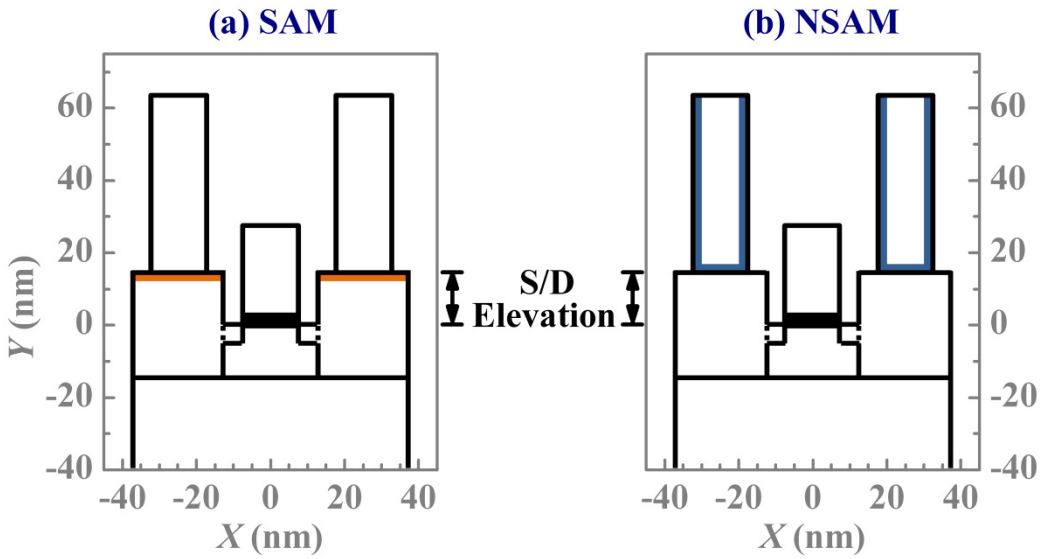

Fig. 3.13. Simulated MOSFETs with L_G of 15 nm and raised S/D regions, having (a) SAM or (b) NSAM. S/D elevations of 5, 15, and 20 nm were simulated.

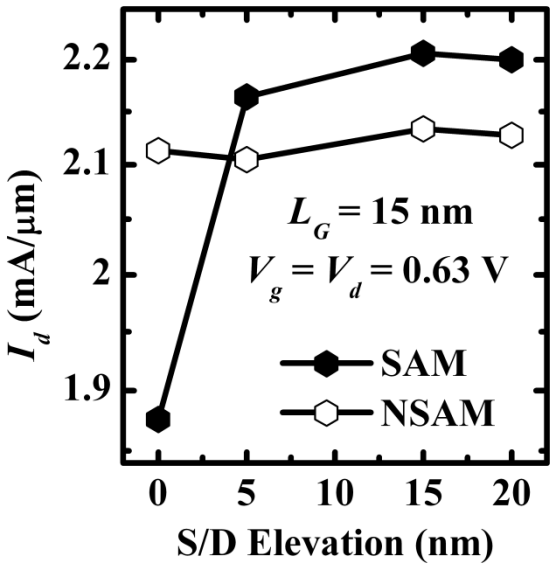

Fig. 3.14. I_d as a function of S/D elevation for SAM and NSAM with d = 10 nm and $\rho_c = 1\times10^{-9}$ Ω·cm^2. When the S/D regions are raised, the SAM no longer suffers from increased spreading resistance, allowing it to give higher I_d than the NSAM.

I_d as a function of S/D elevation for SAM and NSAM with d = 10 nm and ρ_c = 1×10^{-9} Ω·cm^2 is plotted in Fig. 3.14, showing that the SAM gives higher current than the NSAM once the current density bottleneck is relieved by the raised S/D.

The simulations have thus far assumed no misalignment of the vias, which are centered in the S/D regions. Fig. 3.15 plots I_d at $V_g = V_d$ = 0.63 V for misalignments of -5, 0, and 5 nm, with d = 10 nm and $\rho_c = 1\times10^{-9}$ Ω·cm^2 to allow maximum effect from any change in S/D resistance R_{SD}. Negative and positive misalignment refer to a shift of the vias towards the left and right, respectively, consistent with the x-axis defined in Fig. 3.1. For both raised and non-raised S/D and for both SAM and NSAM, the misalignments result in less than 1% change in I_d. Therefore, misalignment has negligible effect on drive current performance, due to the very small changes in R_{SD}.

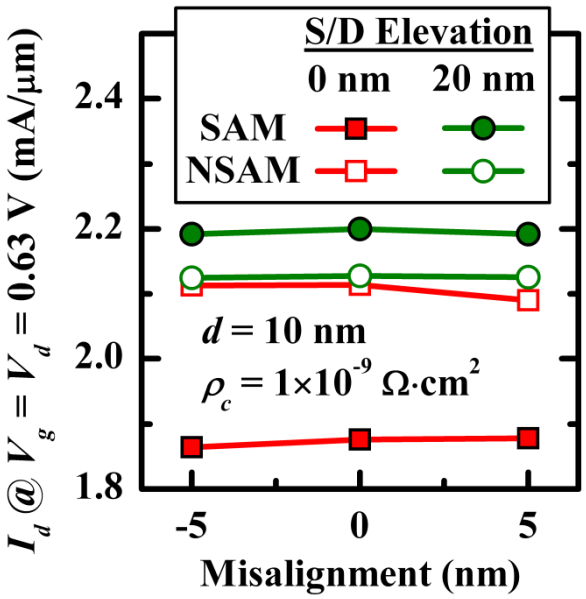

Fig. 3.15. I_d changes by less than 1% when the vias are misaligned by ±5 nm for both SAM and NSAM with d = 10 nm, $\rho_c = 1\times10^{-9}$ Ω·cm^2, and S/D elevation of 0 and 20 nm.

3.4 CONCLUSIONS

$In_{0.53}Ga_{0.47}As$ n-MOSFETs with self-aligned contact metallization were compared against those with non-self-aligned contact metallization by means of two-dimensional simulations. A gate length of 15 nm, gap sizes of 10-20 nm between the via and the gate, and ρ_c values ranging from 1×10^{-9} to 1×10^{-7} $\Omega\cdot cm^2$ at the interface between the contact metallization and the InGaAs source/drain region were simulated. Due to its larger effective contact area, the self-aligned contact metallization has a lower effective contact resistance than the non-self-aligned contact metallization with the same ρ_c, allowing it to give better drive current performance down to ρ_c as low as 3×10^{-9} $\Omega\cdot cm^2$. In addition, the advantage of the self-aligned contact metallization over the non-self-aligned contact metallization can be further enhanced with a raised S/D device structure.

Chapter 4

Towards Conformal Damage-Free Doping with Abrupt Ultra-Shallow Junction: Formation of Si Monolayers and Laser Anneal as a Novel Doping Technique for InGaAs n-MOSFETs

4.1 INTRODUCTION

In this Chapter, a simple and novel Si monolayer doping (MLD) technique involving disilane (Si_2H_6) or silane (SiH_4) treatment followed by laser anneal (LA) is developed as a means for achieving conformal, ultra-shallow, and abrupt n^{++} junctions in InGaAs n-channel metal-oxide-semiconductor field-effect transistors (n-MOSFETs).

The inadequacies of beam-line ion implantation at advanced technology nodes have motivated the development of novel doping techniques such as MLD [186]-[192]. Table 4.1 compares existing MLD works. Of these, only one is on InGaAs [192]. Furthermore, the application of MLD to III-V substrates has been limited to the use of sulfur as the dopant. Despite its amphoteric nature, Si is an attractive and preferred n-type dopant in InGaAs due to its low diffusivity and higher solubility compared to other n-type dopants such as S, Se, and Te [193]. In addition, our internal experiments show that the $(NH_4)_2S_x$ solution used for sulfur MLD can cause etching of III-V substrates such as GaAs and InGaAs, and may therefore require short, well-controlled treatment durations to avoid etching away the fin in a FinFET.

Table 4.1. Comparison with existing MLD works.

Ref.	Substrate	Monolayer Formation	Dopant
[186]	Si	Solution-based	P, B
[187]	Si	Solution-based	P, B
[188]	Si	Solution-based	P
[189]	GaAs	Solution-based	S
[190]	InAs	Solution-based	S
[191]	InP	Solution-based	S
[192]	InGaAs	Solution-based	S
This Work	InGaAs	Gas-based	Si

The principle of the doping technique developed in this Chapter is illustrated in Fig. 4.1. In order to prepare the InGaAs surface for the growth of Si monolayers, a pre-clean is first performed to ensure a high-quality surface free of native oxide. The InGaAs surface is then treated with a Si-containing gas precursor such as Si_2H_6 or SiH_4, which selectively forms a few monolayers of Si on the InGaAs source/drain (S/D) or S/D extension (SDE) regions. One advantage that gas-based MLD could have over solution-based MLD is the possibility of performing an *in situ* clean without breaking vacuum prior to monolayer formation. The Si monolayers serve as a dopant source that is conformal and does not introduce implant damage. A cap layer is then deposited (not shown), followed by laser anneal to drive in and activate the Si dopants. Laser anneal can potentially overcome the solid solubility limit of the dopant due to its metastable nature, allowing a high doping concentration to be achieved. In addition, its effects are highly localized to the surface, and the ultrafast irradiation reduces the thermal budget and minimizes dopant diffusion, enabling the formation of ultra-shallow and abrupt junctions.

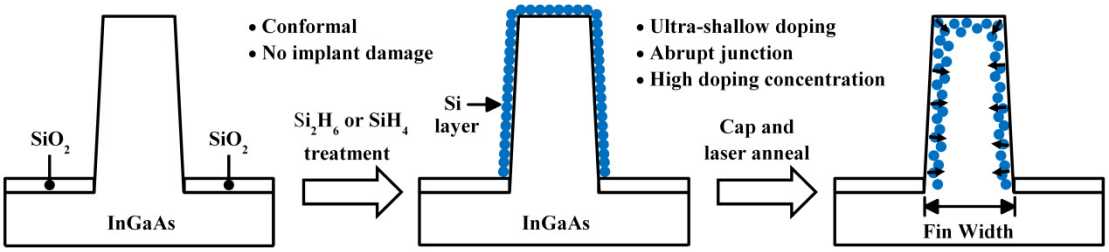

Fig. 4.1. Schematic of a fin structure illustrating the principle of the doping technique developed in this work, which has the potential to achieve conformal ultra-shallow doping with high doping concentration and abrupt junction without implant damage. At narrow fin widths, the sidewall junctions merge, rendering junction depth less important as it is determined by fin width. Nevertheless, junction abruptness and minimizing lateral dopant diffusion are crucial for short-channel devices.

Preliminary investigations of the use of rapid thermal anneal (RTA) instead of LA indicate that the Si dopants are not driven in even at temperatures as high as 800 °C for short annealing durations. Raising the RTA temperature is not feasible due to substrate degradation. On the other hand, LA likely induces very high temperatures at the InGaAs surface but in an extremely short time, enabling it to drive in and activate the Si dopants without surface degradation and out-diffusion of substrate elements.

The doping concentration that can be achieved may be evaluated by assuming the maximum areal dose per monolayer of Si to be the atomic density of the semiconductor surface. For (001) $In_{0.53}Ga_{0.47}As$, which has a surface atomic density of 5.8×10^{14} atoms/cm^2, each monolayer of Si can provide a total doping concentration of 5.8×10^{20} atoms/cm^3 for a junction depth of 10 nm.

4.2 BLANKET SAMPLE PREPARATION

Fig. 4.2 summarizes the process flow for fabricating blanket samples with either Si_2H_6 or SiH_4 treatment. All the sample fabrication, characterization, and

analysis were done by the author unless otherwise mentioned. The blanket samples are used for sheet resistance R_{sheet} measurement, secondary ion mass spectrometry (SIMS) analysis, and specific contact resistivity ρ_c extraction using the transfer length method (TLM) [172]. 500-nm-thick (001) $In_{0.53}Ga_{0.47}As$ with p-type doping concentration of ~2×10^{16} cm^{-3}, formed by molecular beam epitaxy (MBE) on bulk InP, was used as the starting substrate for all samples. The substrates were purchased from a vendor. The samples were first cleaned with a hydrochloric acid (HCl) solution for 3 min., followed by ammonium sulfide [$(NH_4)_2S_x$] passivation, after which they were immediately loaded into separate high-vacuum chambers for Si_2H_6 or SiH_4 treatment.

The Si_2H_6 treatment was carried out at a substrate temperature of 370 °C for 3000 s, with a Si_2H_6 flow rate of 50 standard cubic centimeters per minute (sccm) and a pressure in the order of 10^{-7} Torr. Prior to the Si_2H_6 treatment, the samples were

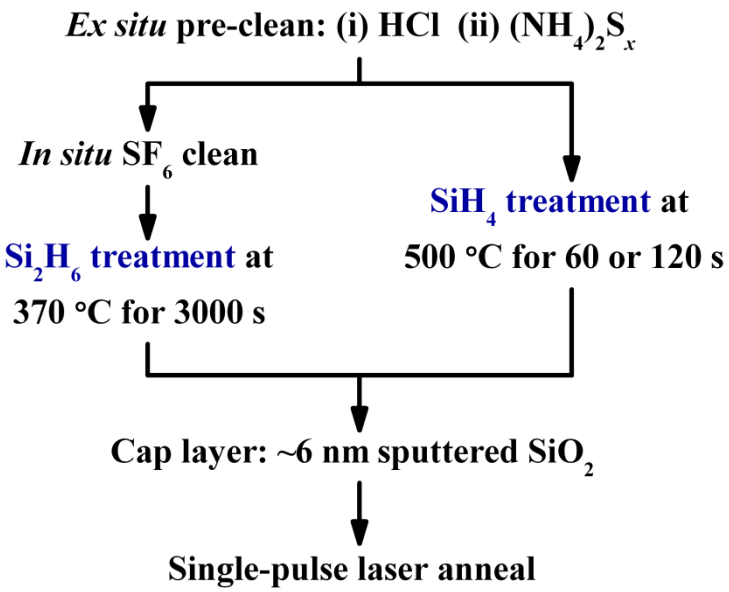

Fig. 4.2. Process flow for fabricating blanket (001) $In_{0.53}Ga_{0.47}As$ samples with Si_2H_6 or SiH_4 treatment and laser anneal.

treated *in situ* with SF_6 plasma at 300 °C for 50 s to remove any residual native oxide. The SiH_4-treated samples did not go through SF_6 plasma treatment. The SiH_4 treatment was done at a substrate temperature of 500 °C for 60 or 120 s, with a SiH_4 flow rate of 60 sccm (mixed with 250 sccm of N_2) and a pressure of 5 Torr. The Si_2H_6 and SiH_4 treatment conditions are similar to those previously reported for Si_2H_6 and SiH_4 passivation of GaAs and InGaAs surfaces [87]-[97]. Due to the much lower pressure, the formation of Si monolayers is much slower for Si_2H_6 treatment than for SiH_4 treatment. However, Si_2H_6 is easier to crack and dissociate than SiH_4, thereby allowing a lower substrate or processing temperature.

After Si_2H_6 or SiH_4 treatment, the samples were immediately capped with ~6 nm of sputtered SiO_2 to prevent oxidation of the Si monolayers and to serve as a cap layer for suppressing the out-diffusion of Si dopants and substrate elements in the subsequent laser anneal. A KrF excimer laser with a wavelength of 248 nm and a pulse width (full-width-half-maximum) of 23 ns was used for the laser anneal, with the samples subjected to a single pulse at various fluences to form a highly-doped n-type layer at the InGaAs surface. All the laser anneals in this Chapter were done by an external company as a paid service.

4.3 MATERIAL CHARACTERIZATION

4.3.1 Disilane-treated samples

After laser anneal, the SiO_2 cap layer was stripped using dilute hydrofluoric acid (HF). The R_{sheet} of the n^{++} InGaAs layer formed after Si_2H_6 treatment and laser anneal is plotted in Fig. 4.3 as a function of laser fluence. R_{sheet} was measured using

micro four-point probes, which do not penetrate the thin n^{++} InGaAs layer. In addition, the small probe spacing of 10 μm ensures that the current flows only in the n^{++} InGaAs layer, so that only the R_{sheet} of that layer is measured. As the fluence increases, R_{sheet} decreases due to larger junction depth and higher dopant activation. Si_2H_6-treated samples that were laser annealed at 80 mJ/cm^2 and below yielded very low current in the μA or sub-μA range when directly probed at a bias of 2 V and a probe separation of ~5-10 μm, which is one to two orders lower than the current obtained from probing the p-type InGaAs starting substrate at the same bias and probe separation. This indicates that 80 mJ/cm^2 is insufficient for driving in or activating the Si dopants, as some or all of the Si still remains on the surface of the InGaAs.

Fig. 4.4 shows the SIMS profiles obtained for Si_2H_6-treated samples laser-annealed at 127, 297, and 374 mJ/cm^2. All the SIMS in this Chapter was done at the

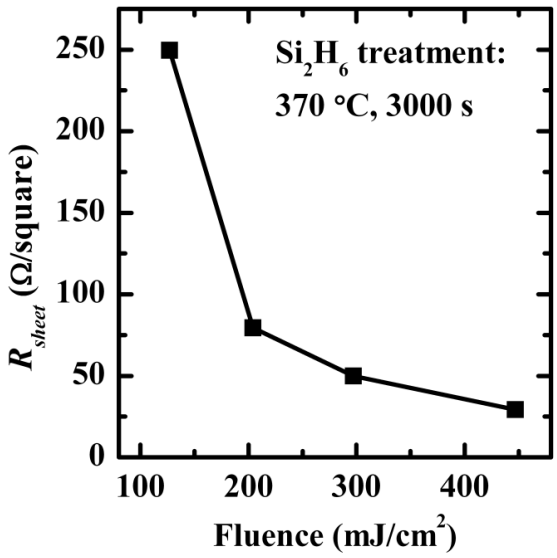

Fig. 4.3. R_{sheet} versus laser anneal fluence for Si_2H_6-treated $In_{0.53}Ga_{0.47}As$ samples. A single laser pulse was used. R_{sheet} decreases as fluence increases due to larger junction depth and higher dopant activation. R_{sheet} cannot be measured for laser fluence of 80 mJ/cm^2 and below.

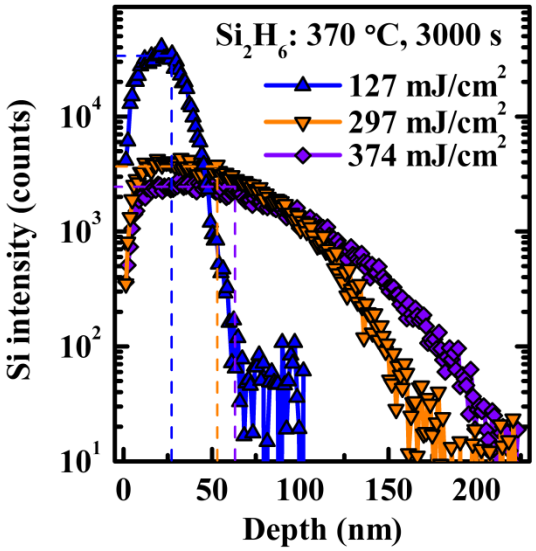

Fig. 4.4. SIMS profiles for Si_2H_6-treated samples annealed at 127, 297, and 374 mJ/cm^2. The dashed lines indicate the InGaAs melt depth, which are estimated from the level or flat portion of the box-like profiles.

Institute of Materials Research and Engineering (IMRE) as a paid service. As the laser photon energy (5 eV) is much larger than the band gap of $In_{0.53}Ga_{0.47}As$ (0.74 eV), significant heating from band gap absorption is expected. The box-like profiles suggest that melting occurred during the laser anneal, resulting in rapid redistribution of the Si dopants in the melted layer due to the much larger diffusivity in the liquid phase. Some out-diffusion of Si can be observed near the surface. The melt depth can be estimated from the level portion of the SIMS profile, and is observed to become larger as the fluence increases, confirming the increase in junction depth deduced from the decrease in R_{sheet} in Fig. 4.3. This is due to higher temperatures near the InGaAs surface at higher fluences, resulting in a larger depth at which the temperature falls below the melting point of $In_{0.53}Ga_{0.47}As$ (~1100 °C). It should be pointed out that the melt depth is only a rough estimate that is used as a gauge for determining the fluence required to form ultra-shallow junctions in $In_{0.53}Ga_{0.47}As$ by Si monolayer formation and laser anneal.

It is noted that GaAs annealed using a KrF excimer laser with the same wavelength, pulse width, and fluence [194] gives a larger melt depth than the InGaAs in this work, despite GaAs having a larger band gap (1.42 eV) and a higher melting point (~1240 °C). This is at least partly attributed to the layer of Si on the InGaAs surface. The presence of Si monolayers on the InGaAs and the thickness of those monolayers can influence the absorption of laser photons and thus affect the temperature profile and melt depth in the InGaAs. Factors such as optical reflectivity, attenuation constant, heat capacity, and thermal conductivity can also affect the fluence required for a given melt depth. For instance, the much larger thermal conductivity of GaAs compared to $In_{0.53}Ga_{0.47}As$ [195] could result in a broader temperature depth profile in GaAs and therefore a thicker layer in which the temperature rises above the melting point of the substrate.

The melt depth at the low fluence of 127 mJ/cm^2 is ~27 nm, which is still rather large. Hence, a fluence of less than 127 mJ/cm^2 is desired for ultra-shallow junction formation. Fig. 4.5 shows the SIMS profiles for Si_2H_6-treated samples annealed at 100 and 120 mJ/cm^2. The Si counts were converted to concentration by application of a relative sensitivity factor extracted from an $In_{0.53}Ga_{0.47}As$ sample that was implanted with a known Si dose and sputtered using the same SIMS beam conditions. Very high Si concentration approaching 10^{21} atoms/cm^3 can be observed, and ultra-shallow melt depths of around 10 and 4 nm are obtained for fluences of 120 and 100 mJ/cm^2, respectively. In addition, the profile for a fluence of 100 mJ/cm^2 exhibits little surface out-diffusion and good junction abruptness (~5.5 nm/decade). Estimated melt depth as a function of laser anneal fluence is plotted in Fig. 4.6, showing that the melt depth becomes more sensitive to laser anneal fluence as the fluence approaches 100 mJ/cm^2.

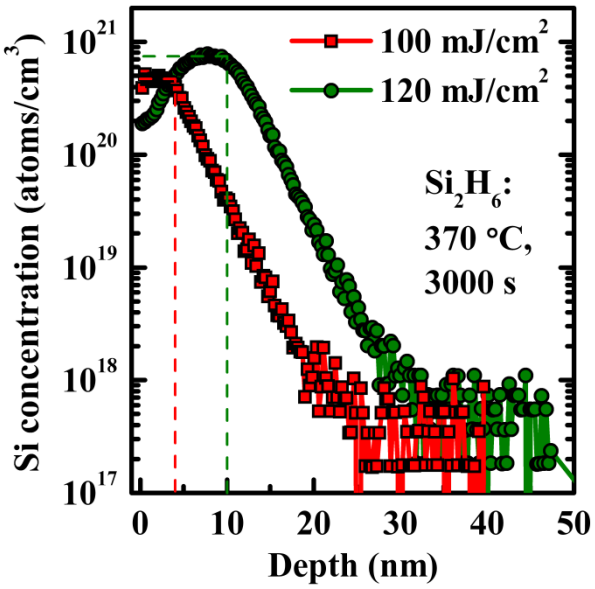

Fig. 4.5. SIMS profiles for Si_2H_6-treated samples annealed at 100 and 120 mJ/cm^2, with ultra-shallow melt depths of around 4 and 10 nm respectively, as indicated by the dashed lines. Very high Si concentration approaching 10^{21} cm^{-3} can be observed. The profile for a fluence of 100 mJ/cm^2 exhibits little surface out-diffusion and good junction abruptness (~5.5 nm/decade).

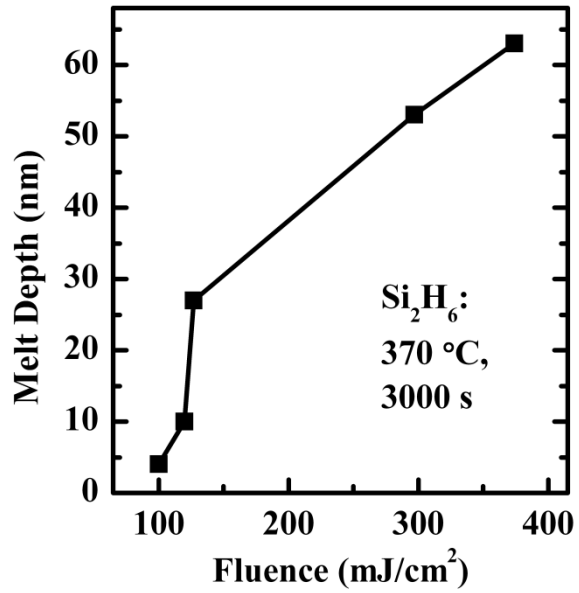

Fig. 4.6. Estimated melt depth as a function of laser anneal fluence. Melt depth increases at higher laser anneal fluences due to higher temperatures induced near the InGaAs surface.

4.3.2 Silane-treated samples

Based on the SIMS profiles from the Si_2H_6-treated samples, the laser anneal fluence was kept low at 100-140 mJ/cm^2 for the SiH_4-treated samples in order to form shallow junctions. After laser anneal, the SiH_4-treated blanket samples underwent mesa formation by wet etching and contact formation by Ni lift-off to form TLM structures for R_{sheet} and ρ_c extraction. An example of the TLM current-voltage (I-V) characteristics, extracted from a sample that was SiH_4-treated at 500 °C for 120 s and laser-annealed at 100 mJ/cm^2, is shown in Fig. 4.7(a), along with the resulting plot of total resistance R_{total} versus TLM contact pad spacing d_{TLM} in Fig. 4.7(b). Good ohmic characteristics are observed for all SiH_4-treated samples.

Fig. 4.8 plots R_{sheet} of the n^{++} InGaAs and ρ_c of Ni on the n^{++} InGaAs as a function of laser fluence for both SiH_4 treatment times. R_{sheet} measurements of the blanket samples by micro four-point probes prior to fabrication of TLM structures gave values similar to those extracted from the TLM structures. A longer SiH_4 treatment time gives lower R_{sheet} and ρ_c at each fluence due to a higher areal dose of Si dopants. Hence, the Si dose can be controlled by varying the SiH_4 treatment time. For both SiH_4 treatment times, a higher laser fluence results in a deeper junction and higher activation and therefore lower R_{sheet}, similar to the trend observed for Si_2H_6-treated samples in Fig. 4.3. It is also observed that ρ_c decreases as the laser fluence increases from 100 to 120 mJ/cm^2, but increases slightly when the fluence increases from 120 to 140 mJ/cm^2. This can be attributed to better dopant activation but also more surface out-diffusion at higher fluences, which respectively enhance and reduce the active dopant concentration at the surface. ρ_c is lower when the active dopant concentration at the surface is higher.

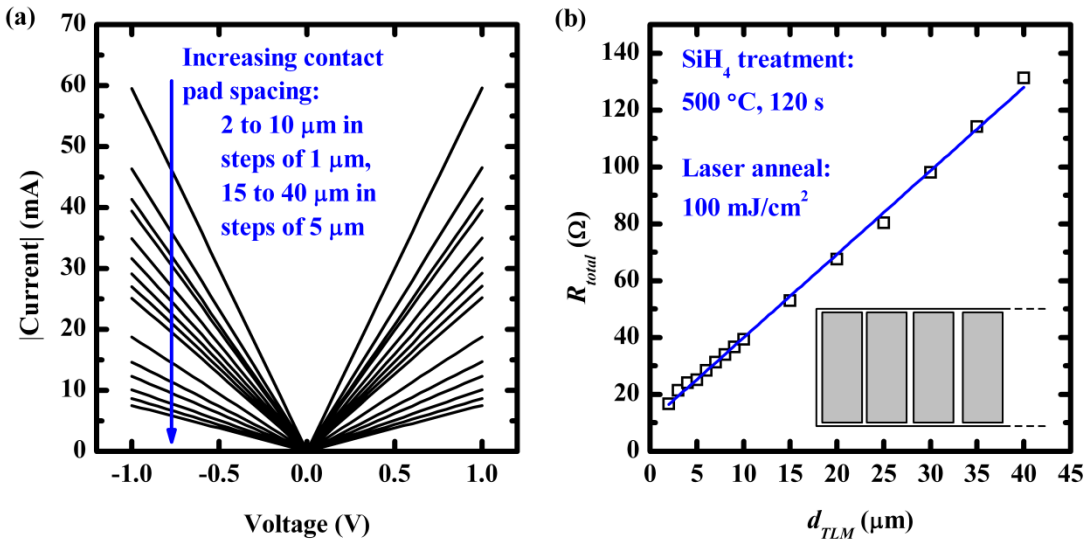

Fig. 4.7. (a) An example of the TLM *I-V* characteristics obtained from a SiH_4-treated sample, and (b) the resulting plot of total resistance R_{total} versus TLM contact pad spacing d_{TLM}, from which R_{sheet} of the InGaAs and ρ_c of the contact can be derived. The inset shows a schematic of the TLM structure, with the Ni contact pads represented by gray rectangles. Probing is done on two adjacent contact pads.

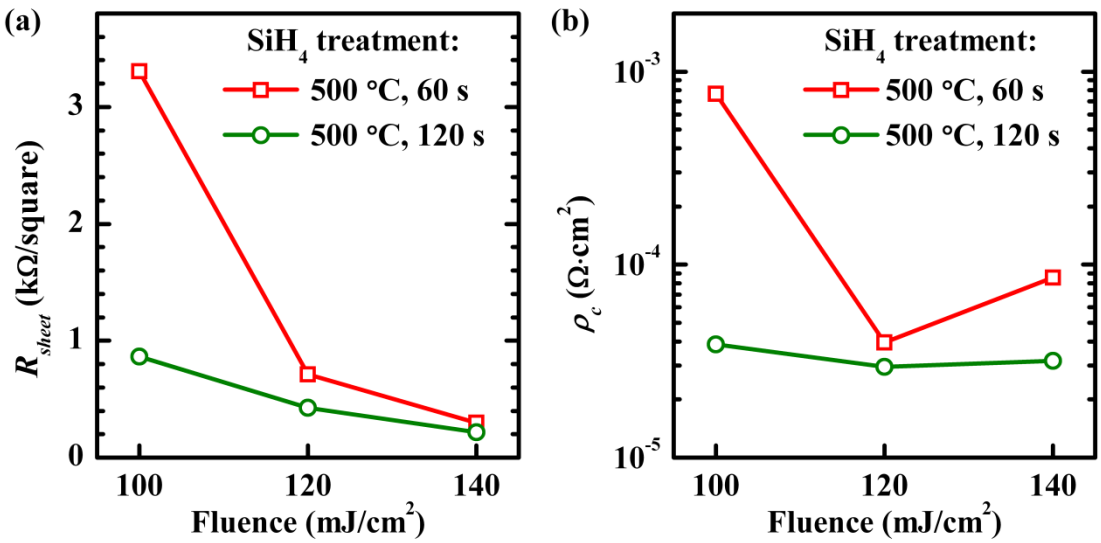

Fig. 4.8. (a) R_{sheet} and (b) ρ_c versus laser fluence for samples treated with SiH_4 at 500 °C for 60 and 120 s. At each fluence, R_{sheet} and ρ_c are lower for the longer SiH_4 treatment time of 120 s due to a higher areal dose of Si dopants. R_{sheet} decreases as fluence increases due to larger junction depth and higher dopant activation. ρ_c first decreases then increases as fluence increases from 100 to 140 mJ/cm^2, due to better dopant activation but also more dopant out-diffusion at higher fluences.

From the SIMS profiles shown in Fig. 4.9 for SiH_4 treatment time of 120 s, it is observed that the Si dopants are indeed driven in deeper at higher fluences, and that a fluence of 140 mJ/cm^2 appears to cause more surface out-diffusion than a fluence of 120 mJ/cm^2. It is also noted that the Si profiles for fluences of 120 and 140 mJ/cm^2 are more box-like, which could indicate melting of the InGaAs at these fluences but not at 100 mJ/cm^2. As with the Si_2H_6-treated samples, a fluence of 100 mJ/cm^2 gives the best Si profile, with a very high Si concentration of ~5.25×10^{20} cm^{-3} at the InGaAs surface and a very steep slope of ~4 nm/decade.

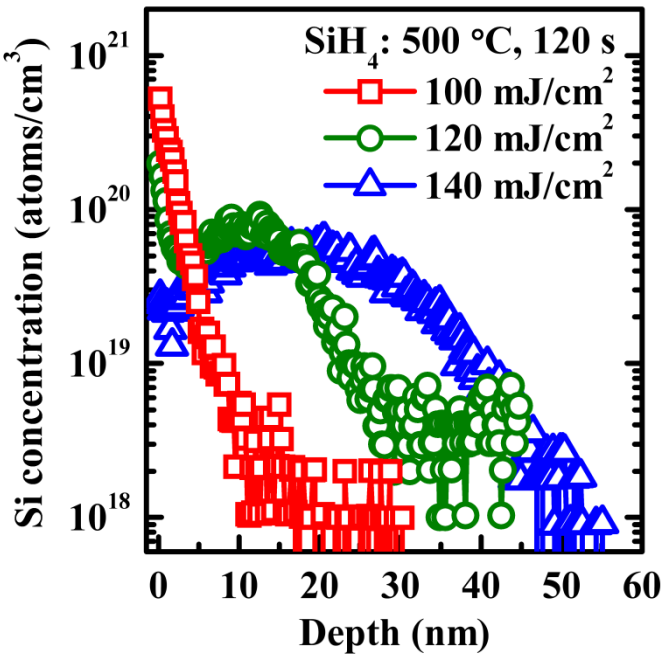

Fig. 4.9. SIMS profiles for samples treated with SiH_4 at 500 °C for 120 s and laser annealed at 100, 120 and 140 mJ/cm^2. The profiles for fluences of 120 and 140 mJ/cm^2 are more box-like, while the profile for a fluence of 100 mJ/cm^2 has a very high Si concentration of ~5.25×10^{20} cm^{-3} at the InGaAs surface and a very steep slope of ~4 nm/decade.

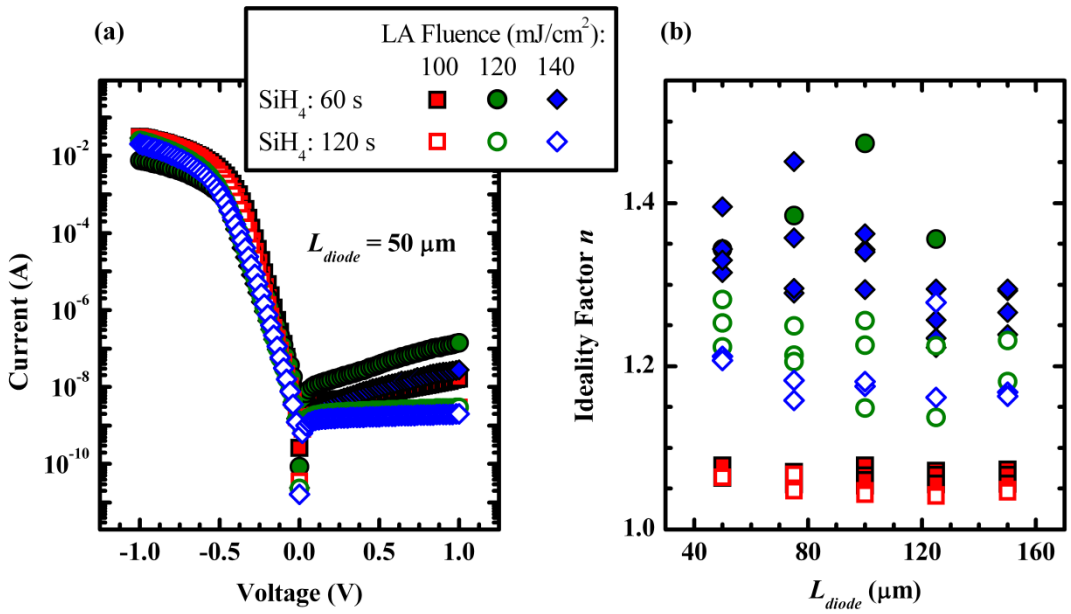

Fig. 4.10. (a) Diode current-voltage characteristics showing high forward-to-reverse current ratio of 5 to 7 orders of magnitude. (b) Ideality factor of diodes versus diode size for various SiH_4 treatment times and laser anneal fluences. Both plots share the same legend. Diodes with a fluence of 100 mJ/cm^2 have very low n that is independent of L_{diode}. Diodes with a fluence of 120 and 140 mJ/cm^2 have higher n that also varies much more across diodes, which is attributed to melt-induced defects at the liquid-solid interface.

Diodes were also fabricated from the SiH_4-treated samples, with mesa etching used to define the diodes and Ni lift-off used to form the top contacts. As the contacts to the n-doped InGaAs are ohmic, the measured diode characteristics are those of the p-n junction diodes formed by the Si MLD. Each diode has dimensions of $L_{diode} \times L_{diode}$, with L_{diode} ranging from 50 to 150 µm. Au was used to form an ohmic contact to the InP on the back side of the substrate. Fig. 4.10(a) plots the current-voltage characteristics of diodes with L_{diode} of 50 µm, showing well-behaved diodes with a large difference of 5 to 7 orders of magnitude between forward and reverse currents across the various SiH_4 treatment and laser fluence splits. The ideality factor n extracted from the current-voltage characteristics of diodes with various SiH_4

treatment times and laser anneal fluences is plotted versus L_{diode} in Fig. 4.10(b). The diode ideality factor is not expected to vary with diode size. The diodes with laser anneal fluence of 100 mJ/cm^2 exhibit very low n approaching unity, which is testament to the excellent junction quality due to the absence of implant damage, with n being relatively constant for various L_{diode}. On the other hand, the values of n for diodes with laser anneal fluence of 120 and 140 mJ/cm^2, although reasonable, are significantly higher and exhibit much larger diode-to-diode variations. This could be due to the occurrence of melting at fluences of 120 and 140 mJ/cm^2 (but not 100 mJ/cm^2) as seen from the SIMS profiles in Fig. 4.9, which results in the creation of defects at the liquid-solid interface during quenching. Lower n is also generally observed for the longer SiH_4 treatment time of 120 s due to higher doping concentration.

From the SIMS and diode data, it is clear that SiH_4 treatment followed by laser anneal at a fluence of 100 mJ/cm^2 is a promising technique for realizing very abrupt, ultra-shallow, and high-quality junctions with high n-type doping concentration in $In_{0.53}Ga_{0.47}As$ n-MOSFETs. Planar $In_{0.53}Ga_{0.47}As$ n-MOSFETs are thus fabricated as a first demonstration of this novel doping technique.

4.4 MOSFET FABRICATION AND CHARACTERIZATION

The process flow for fabricating planar $In_{0.53}Ga_{0.47}As$ n-MOSFETs with ultra-shallow and abrupt n^{++} S/D using SiH_4 treatment and laser anneal is illustrated in Fig. 4.11. The starting substrate, which was purchased from a vendor, is 500-nm-thick (001) $In_{0.53}Ga_{0.47}As$ with p-type doping concentration of ~2×10^{16} cm^{-3}, grown by MBE on InP. After a pre-gate clean using HCl solution and $(NH_4)_2S_x$ passivation, a

gate stack comprising 5 nm Al_2O_3 gate dielectric and 100 nm TaN gate metal was deposited. Following gate patterning and etching, residual Al_2O_3 in the S/D regions was removed using dilute HF. Next, HCl pre-clean and $(NH_4)_2S_x$ passivation were carried out, and the samples were then loaded immediately into the high-vacuum chamber used for SiH_4 treatment to selectively form Si monolayers in the S/D regions. After SiH_4 treatment at a substrate temperature of 500 °C for 60 or 120 s, a 6-nm-thick SiO_2 cap layer was immediately deposited, followed by laser anneal at 100 mJ/cm^2. The gate stack blocks the laser and shields the channel under it from receiving the laser anneal, thus allowing selective annealing of the S/D regions. MOSFET fabrication was completed by mesa etch for device isolation and Ni lift-off for S/D contact formation. It is pointed out that no deep S/D regions were formed. Fig. 4.12 shows a scanning electron microscopy (SEM) image of a completed device.

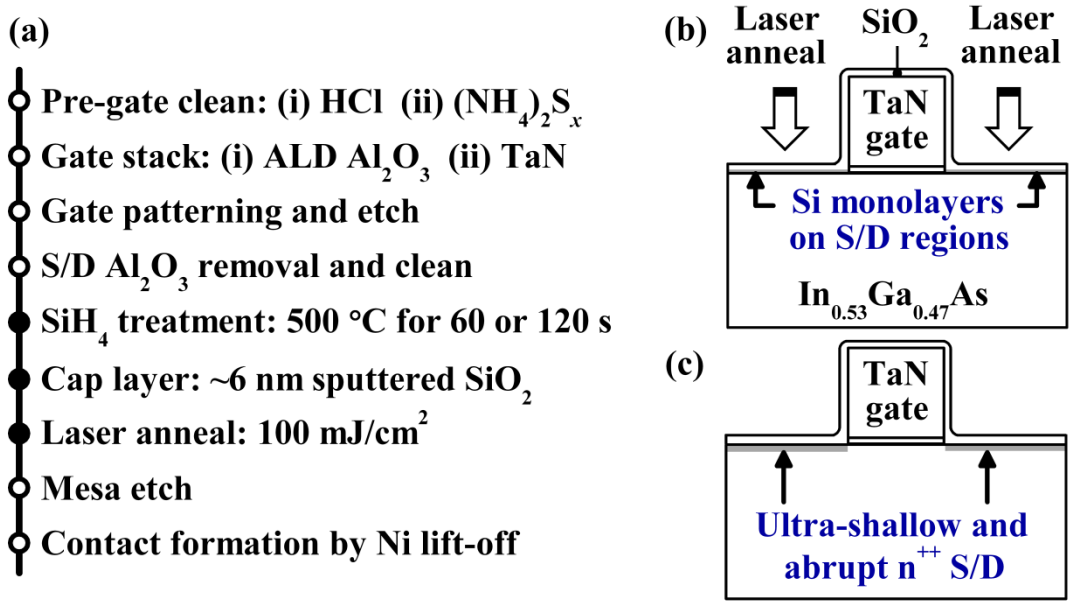

Fig. 4.11. (a) Process flow for fabricating planar InGaAs n-MOSFETs using the developed doping technique. Schematics of the transistor (b) after SiH_4 treatment and cap layer deposition and (c) after laser anneal are shown.

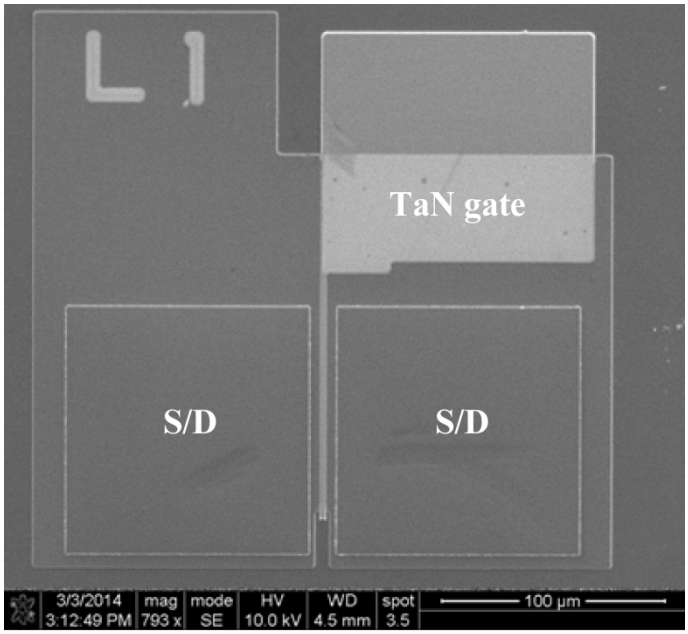

Fig. 4.12. SEM image of a completed $In_{0.53}Ga_{0.47}As$ n-MOSFET fabricated using the process flow in Fig. 4.11.

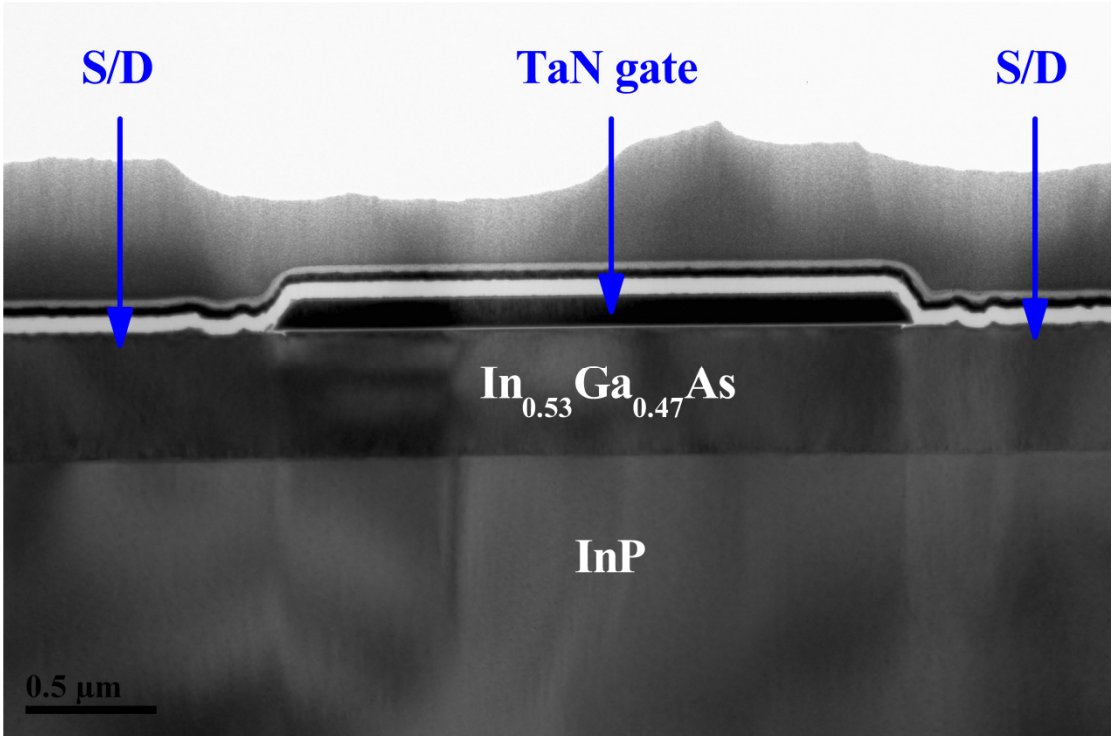

Fig. 4.13. Cross-sectional TEM image of an $In_{0.53}Ga_{0.47}As$ n-MOSFET with S/D doped by SiH_4 treatment at 500 °C for 120 s and laser anneal at 100 mJ/cm^2. The S/D contacts, which are 5 µm away from the gate, cannot be seen in this TEM image.

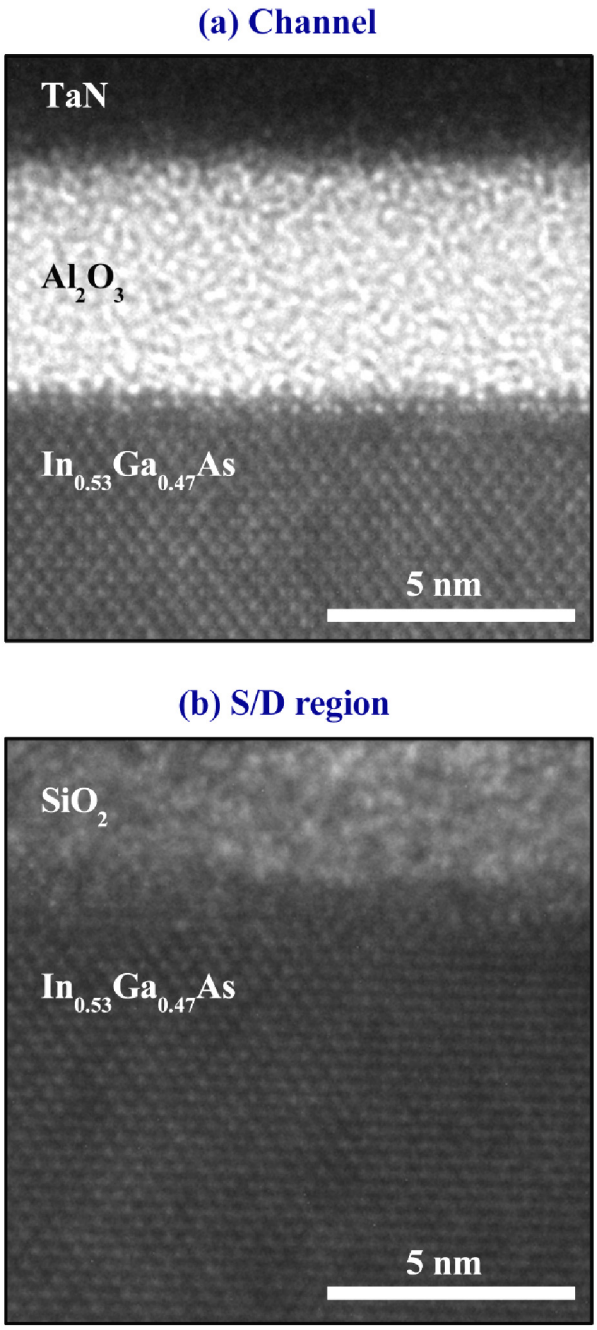

Fig. 4.14. High-magnification TEM images of the (a) channel and (b) S/D regions of the MOSFET in Fig. 4.13, with S/D regions doped by SiH_4 treatment at 500 °C for 120 s and laser anneal at 100 mJ/cm^2. Good crystalline quality is preserved in both regions and a good interface is maintained between the gate dielectric and the channel, with no laser-induced damage to the gate stack and channel. As there is no ion implantation, no implant-induced defects are created.

Figs. 4.13 and 4.14 show transmission electron microscopy (TEM) images of a MOSFET with S/D regions doped by SiH_4 treatment at 500 °C for 120 s and laser anneal at 100 mJ/cm^2. The TEM was done at IMRE as a paid service. Good crystalline quality is preserved in both the channel and S/D regions, and a good interface is maintained between the gate dielectric and the channel. Hence, the laser anneal at 100 mJ/cm^2 does not damage the gate stack, and does not require a reflective metal on top of the gate to protect it. The S/D regions are free from implant damage as no ion implantation was done. Further confirmation of gate stack integrity after laser anneal at 100 mJ/cm^2 is provided by the plot of gate current I_g versus gate voltage V_g in Fig. 4.15, which shows low gate leakage current.

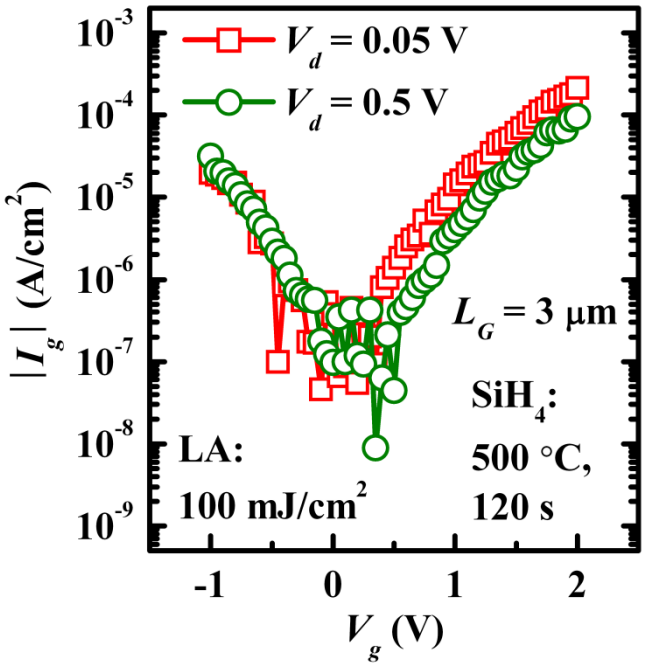

Fig. 4.15. I_g-V_g characteristics showing low gate leakage current after laser anneal at 100 mJ/cm^2, which confirms that gate stack integrity is not compromised.

Fig. 4.16 plots drain current I_d versus V_g for a pair of devices with SiH_4 treatment times of 60 and 120 s, showing good transfer characteristics with reasonable subthreshold swing (SS) and negligible DIBL. Plots of I_d versus drain voltage V_d for the same pair of transistors in Fig. 4.16 are shown in Fig. 4.17, exhibiting well-behaved output characteristics. The low current level is due to the high series resistance, caused by the lack of deep S/D regions and the large 5 μm separation between the channel and the Ni S/D contacts. In addition, the doping process needs to be optimized in order to reduce R_{sheet} and ρ_c.

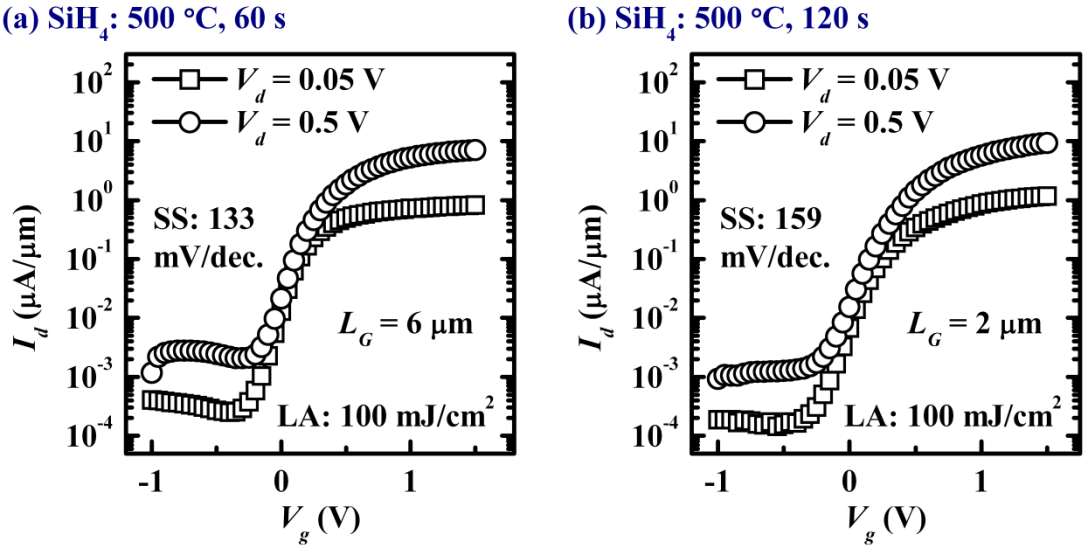

Fig. 4.16. I_d-V_g characteristics of planar $In_{0.53}Ga_{0.47}As$ n-MOSFETs with S/D doped by SiH_4 treatment at 500 °C for (a) 60 s and (b) 120 s followed by laser anneal at a fluence of 100 mJ/cm^2, showing reasonable SS and negligible DIBL.

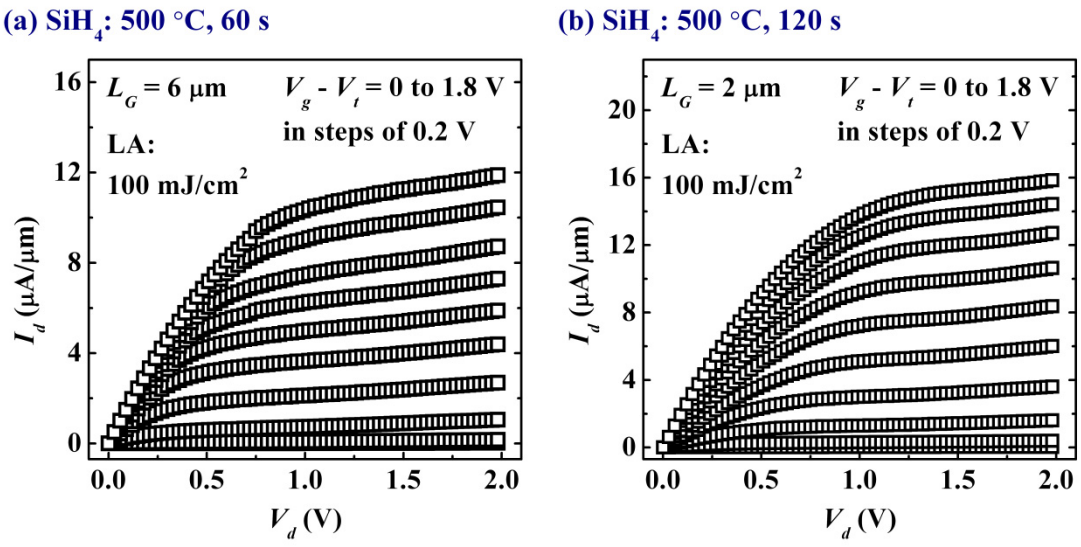

Fig. 4.17. I_d-V_d characteristics of the same pair of transistors as in Fig. 4.16, showing well-behaved output characteristics. V_t is the linear threshold voltage extracted by the maximum transconductance method. The low current level is due to high series resistance caused by the lack of deep S/D regions and the long distance between the S/D contacts and the channel. Careful optimization of the doping technique is also required for R_{sheet} and ρ_c reduction.

4.5 CONCLUSIONS

A novel doping technique based on the formation of Si monolayers followed by laser anneal was developed for InGaAs n-MOSFETs. The technique does not involve ion implantation, thereby eliminating implant damage, and is promising for realizing the conformal, ultra-shallow, and abrupt n^{++} junctions required in the source/drain or source/drain extension regions of highly scaled InGaAs n-MOSFETs with advanced three-dimensional device architectures. The technique was successfully implemented in planar $In_{0.53}Ga_{0.47}As$ MOSFETs as a first demonstration. Further optimization of the technique is needed to improve dopant activation and reduce sheet resistance and contact resistivity, and the performance of the doping technique can be studied for three-dimensional device structures such as FinFETs.

Chapter 5

Plasma Doping of InGaAs at Elevated Substrate Temperature for Reduced Sheet Resistance and Defect Formation

5.1 INTRODUCTION

Plasma doping (PLAD), a high-throughput ion implantation technique capable of achieving ultra-shallow junctions and conformal doping of three-dimensional (3D) structures such as fin field-effect transistors (FinFETs), is investigated in this Chapter as an alternative to conventional beam-line ion implantation for InGaAs at advanced technology nodes. In particular, PLAD at an elevated substrate temperature (denoted as "ET-PLAD") is studied for InGaAs for the first time, and compared against PLAD with the substrate kept at room temperature by cooling (denoted as "RT-PLAD").

The shadowing-induced angle limitations of beam-line implantation at advanced technology nodes open the door for the use of PLAD in future generations of FinFETs. PLAD, an application of plasma immersion ion implantation (PIII), is an implant-based doping method that has been widely studied as an alternative to beam-line ion implantation [196]-[223]. In PLAD, the wafer is immersed in a plasma with high ion density, and a negative bias is applied to the wafer to accelerate the ions from the plasma into the wafer. High implant currents with dose rates as high as 10^{16} $cm^{-2} \cdot s^{-1}$ are achievable, even at ultra-low implant energies of a few keV and below. Furthermore, the entire wafer surface receives the implants at the same time, resulting in an implantation time that is independent of the wafer size and eliminating the need

for the beam formation and transport and the wafer rotation and tilt required for beam-line ion implantation.

In addition, PLAD has been demonstrated to be capable of conformally and uniformly doping 3D trench and fin structures [214]-[221], including trenches with high aspect ratio and fins with narrow pitch. This is due to the angular distribution of the ions that are implanted into the wafer. Secondary electrons reflected between trench or fin sidewalls may also enhance the ion density there and help to improve sidewall doping [199].

However, the research on PLAD has largely focused on the formation of ultra-shallow junctions in Si [196]-[221], with scant reports of PLAD being used on other materials such as Ge [222] and III-V compound semiconductors [223]. Furthermore, previous reports on ET-PLAD show that an elevated substrate temperature during PLAD helps to suppress crystal defects and maintain crystallinity due to dynamic annealing as the ions are implanted, but these reports are confined exclusively to Si substrates [208]-[210].

5.2 BLANKET SAMPLE PREPARATION

The process flow for fabricating blanket InGaAs samples using PLAD is summarized in Fig. 5.1 (solid bullets). The starting substrate is 500-nm-thick (001) $In_{0.53}Ga_{0.47}As$ with p-type doping concentration of ~2×10^{16} cm^{-3}, grown on bulk InP with p-type doping concentration of ~5×10^{18} to ~5×10^{19} cm^{-3}. 4 nm of Al_2O_3 was deposited by atomic layer deposition (ALD), followed by PLAD at two different radio frequency (RF) biases, doses, and substrate temperatures, as indicated in Table 5.1. The Al_2O_3 prevents any deposition, etching, or sputtering processes from occurring

directly on the InGaAs surface during PLAD, and also serves as a capping layer for the subsequent dopant activation anneal.

An Applied Materials Inc. (AMAT) VIISta PLAD System, which has unique biasing capability to allow greater process flexibility and conformal doping, was used for the PLAD, with SiH_4 as the process gas for the plasma to provide the Si dopants. The SiH_4 dissociates in the plasma into species such as SiH_x^+, SiH_x^-, SiH_2, SiH_3, SiH, SiH^*, and Si^*, some of which can further dissociate into species such as Si, SiH, H_2, H, H_x^+, and H^*. Reactive species in the plasma can also undergo secondary reactions. The chemical species and secondary reactions in a SiH_4 or SiH_4/H_2 plasma are illustrated in Figs. 5.2 and 5.3.

Dopant activation was carried out by a rapid thermal anneal (RTA) at 600 °C for 60 s, forming a thin n^{++} layer at the InGaAs surface. For comparison, blanket samples doped by conventional beam-line ion implantation instead of PLAD and with 5-nm-thick Al_2O_3 were also prepared. The beam-line ion implantation splits are detailed in Table 5.2. All the PLAD and beam-line ion implantation in this Chapter were done by AMAT as part of a collaboration, while all other process steps were done by the author.

Some of the PLAD blanket samples underwent further process steps (indicated by open bullets in Fig. 5.1) to fabricate transfer length method (TLM) structures and diodes. These steps include mesa patterning and etch, contact hole patterning and etch, and contact metal deposition and lift-off. The TLM structures and diodes were fabricated together on each of these samples, and Au was sputtered on the back side of the samples to form an ohmic contact to the p^+ InP for diode measurements.

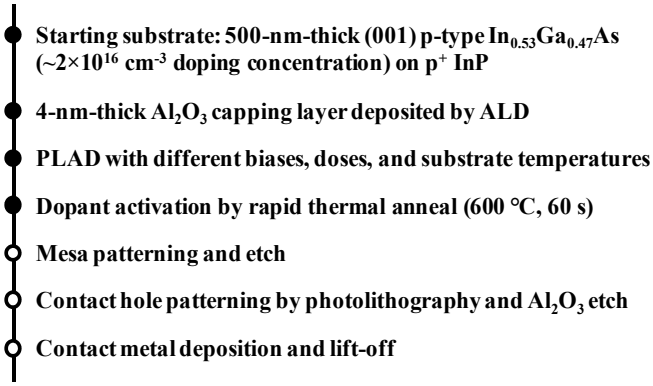

Fig. 5.1. Process flow (solid bullets) for fabricating blanket samples using PLAD. Additional steps (open bullets) were carried out to form TLM structures and diodes on some of the fabricated blanket samples.

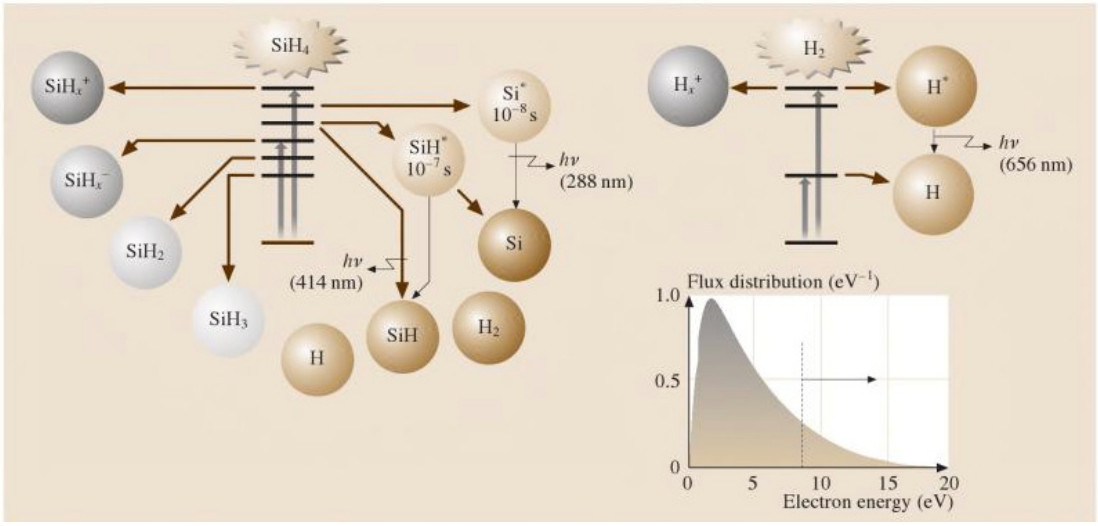

Fig. 5.2. Schematic illustrating the dissociation of SiH_4 and H_2 molecules into various chemical species in a plasma. Source: Fig. 26.1 in the *Springer Handbook of Electronic and Photonic Materials, 2006*.

Ion exchanging	$SiH_x^+ + SiH_4$	$\rightarrow SiH_x + SiH_4^+$
Ion–Molecule	$SiH_x + SiH_4$	$\rightarrow SiH_3 + SiH_3$
Neutral–Molecule	$SiH + SiH_4$	$\rightarrow Si_2H_5$
Disproportionation	$Si + SiH_4$	$\rightarrow SiH_3 + SiH$
Insertion	$SiH_2 + SiH_4$	$\rightarrow Si_2H_6$
Recombination	$SiH_2 + H_2$	$\rightarrow SiH_4$
Abstraction	$SiH_3 + SiH_4$	$\rightarrow SiH_4 + SiH_3$
	$H + SiH_4$	$\rightarrow H_2 + SiH_3$
Ion–Radical, Radical–Radical	less probable	

Fig. 5.3. Secondary reactions in a SiH_4 or SiH_4/H_2 plasma. Source: Fig. 26.2 in the *Springer Handbook of Electronic and Photonic Materials, 2006*.

Table 5.1. Split table for samples doped by PLAD.

Split	Species	Substrate bias (kV)	Dose (cm^{-2})	Substrate temperature (°C)
P1	Si	5	5×10^{14}	25
P2	Si	5	5×10^{14}	100
P3	Si	5	2×10^{15}	25
P4	Si	5	2×10^{15}	100
P5	Si	10.5	5×10^{14}	25
P6	Si	10.5	5×10^{14}	100
P7	Si	10.5	2×10^{15}	25
P8	Si	10.5	2×10^{15}	100

Table 5.2. Split table for samples doped by beam-line implant.

Split	Species	Energy (keV)	Dose (cm^{-2})	Tilt (°)	Substrate temperature (°C)
B1	Si	10	5×10^{14}	45	25
B2	Si	10	5×10^{14}	7	25
B3	Si	10	5×10^{14}	7	200
B4	Si	10	1×10^{15}	7	25
B5	Si	10	1×10^{15}	7	200
B6	Si	10	5×10^{14}	7	25
	S	11.4	5×10^{14}		
B7	Si	10	5×10^{14}	7	200
	S	11.4	5×10^{14}		
B8	Si	10	5×10^{14}	7	25
	Te	45	5×10^{14}		
B9	Si	10	5×10^{14}	7	200
	Te	45	5×10^{14}		

5.3 MATERIAL CHARACTERIZATION

The dielectric response of a material, obtained by ultra-violet variable angle spectroscopic ellipsometry (UV-VASE), can be used to assess its crystallinity [224]. Fig. 5.4 plots the imaginary part (ε_2) of the pseudo-dielectric function versus photon energy in the near-infrared to UV regime, obtained from blanket samples that underwent beam-line ion implantation. The modeled ε_2 profile for 4.3 nm Al_2O_3 on 500 nm p^- $In_{0.53}Ga_{0.47}As$ on 500 μm p^+ InP is also plotted, showing two sharp features that are characteristic of a pristine single-crystalline substrate. The optical constants of InGaAs and InP used in the modeling were obtained by characterizing separate calibration samples. All the VASE modeling (ultra-violet and infrared) in this Chapter was done by a colleague, Dr. Vijay Richard D'Costa, while all VASE measurements (ultra-violet and infrared) were done by the author.

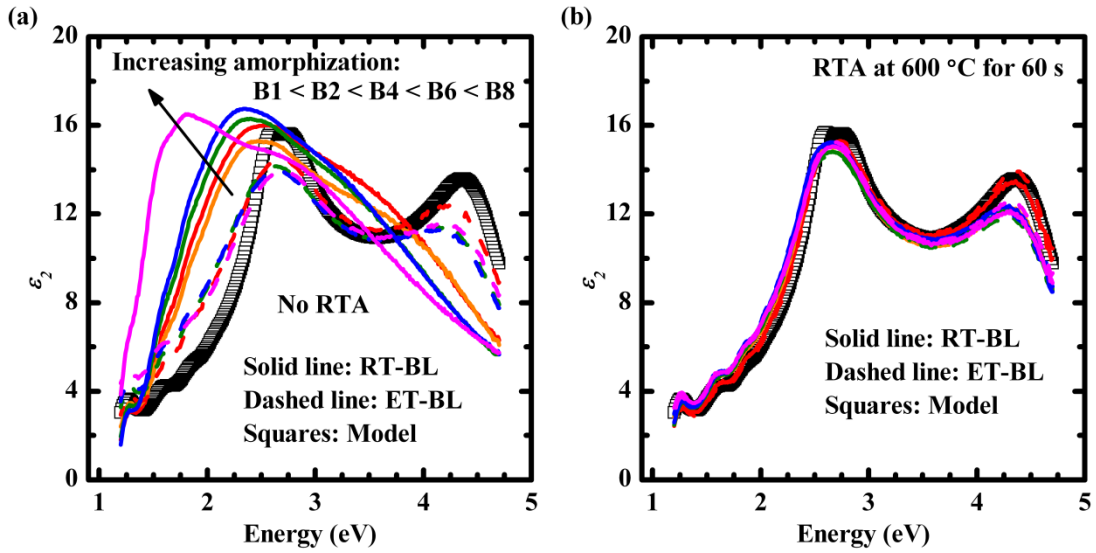

Fig. 5.4. Measured UV-VASE data (a) before RTA and (b) after RTA, obtained from samples doped by conventional beam-line implant. Solid lines are used for RT-BL samples, while dashed lines are used for ET-BL samples. The modeled ε_2 profile for 4.3 nm Al_2O_3 on 500 nm p^- $In_{0.53}Ga_{0.47}As$ on 500 μm p^+ InP is also plotted (open squares).

The benefit of an elevated substrate temperature during implantation for the as-implanted samples is illustrated in Fig. 5.4(a). The ε_2 profiles of splits with room-temperature substrates during beam-line implantation (denoted as "RT-BL") exhibit a single broad peak with big shifts relative to the modeled profile, indicating amorphization of the top portion of the InGaAs substrate. On the other hand, the splits with elevated substrate temperature during beam-line implantation (denoted as "ET-BL") have ε_2 profiles that are close to the modeled profile, indicating that crystallinity is preserved even before dopant activation anneal. A small amount of crystal damage accounts for the small differences between the ET-BL profiles and the modeled profile, but amorphization has been largely suppressed.

The as-implanted RT-BL splits show a trend of increasing amorphization as the implant dose or the mass of the implanted ions increases. A larger peak shift towards lower energies suggests a greater degree of amorphization, which manifests as a larger amount of crystal damage and/or a thicker amorphous layer. Split B1, with a tilt of 45°, shows the smallest shift in the ε_2 profile compared to the other splits (B2, B4, B6, and B8) which have a tilt of 7°. Split B4, which has the same implant energy as Split B2 but double the implant dose, exhibits a larger shift in the ε_2 profile than Split B2. Splits B6 and B8 have the same total dose as Split B4, but with half the dose comprising Si implants at the same energy and half the dose comprising either heavier S ions that cause more damage than Si (Split B6) or even heavier Te ions that cause even more damage than S (Split B8).

After RTA at 600 °C for 60 s [Fig. 5.4(b)], all the beam-line implant samples recover almost completely towards the pristine crystalline InGaAs, as shown by the close matching of their ε_2 profiles to the modeled one. N-type doping near the InGaAs surface and small variations in Al_2O_3 thickness could contribute to the small

deviations from the modeled profile. The strong recovery of crystallinity, even for samples that were amorphized by the beam-line implant, shows that the annealing conditions are sufficient for damage repair and recrystallization of the InGaAs. However, this does not make an elevated substrate temperature during implantation redundant, as the samples are blanket bulk substrates with a large crystalline base for crystal regrowth. Such a luxury is not afforded to fins with small dimensions, where amorphization of the fin can lead to a lack of sufficient crystalline seed for crystal regrowth and make it harder to repair the crystal damage and defects, ultimately resulting in higher leakage and series resistance.

All the TEM in this Chapter was done at the Data Storage Institute (DSI) as a paid service. Cross-sectional transmission electron microscopy (TEM) images of an as-implanted blanket sample from Split P8 (ET-PLAD) are presented in Fig. 5.5, showing excellent crystallinity with no visible defects even without RTA. In addition, the InGaAs surface remains smooth and is not roughened by the PLAD. An additional cap layer (~7 nm thick) on top of the 4-nm-thick Al_2O_3 can be seen, and is determined by EDX to comprise of SiO_x and/or Si. This additional layer was deposited by the plasma during PLAD, and should be minimized as it can affect the dopant concentration and dose in the InGaAs, and can also fill the gaps between fins and make it difficult to conformally dope fins with tight pitches. This can be resolved by tuning the PLAD conditions. For instance, when using B_2H_6 for PLAD, dilution with He or H_2 has been shown to reduce boron deposition [211]-[212].

Fig. 5.6 plots the ε_2 profiles obtained from UV-VASE measurements on PLAD blanket samples before and after RTA. The UV-VASE measurements for as-implanted samples were done with the cap layers present [Fig. 5.6(a)], since they are

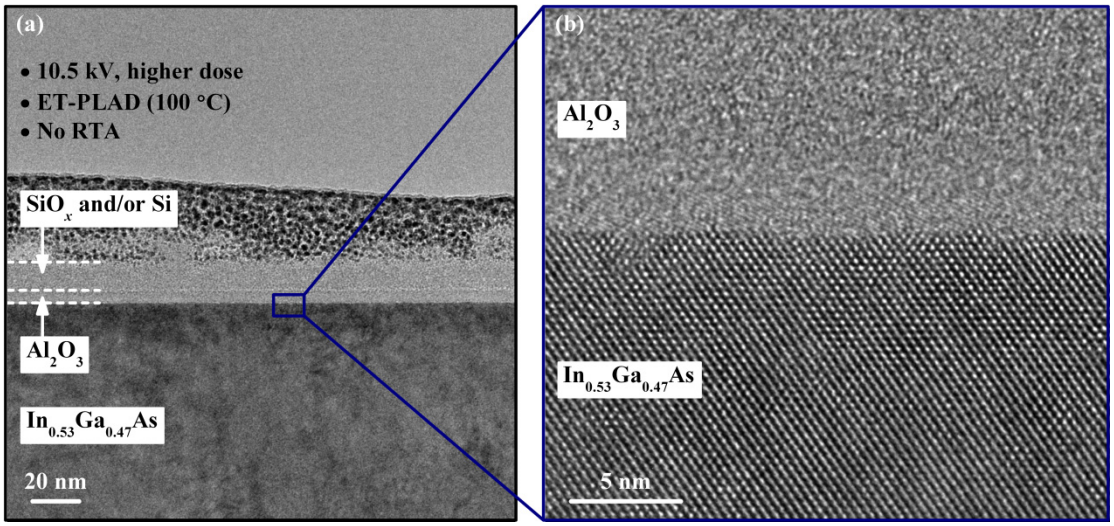

Fig. 5.5. (a) Low-magnification and (b) high-resolution TEM images of a blanket sample from Split P8 before RTA. An additional layer (~7 nm thick), determined by EDX to comprise of SiO_x and/or Si, was deposited on the Al_2O_3 by the plasma during PLAD. The InGaAs surface remains smooth and is not roughened by the PLAD, and the InGaAs shows good crystallinity with no visible defects for the given PLAD conditions of Split P8, even without RTA.

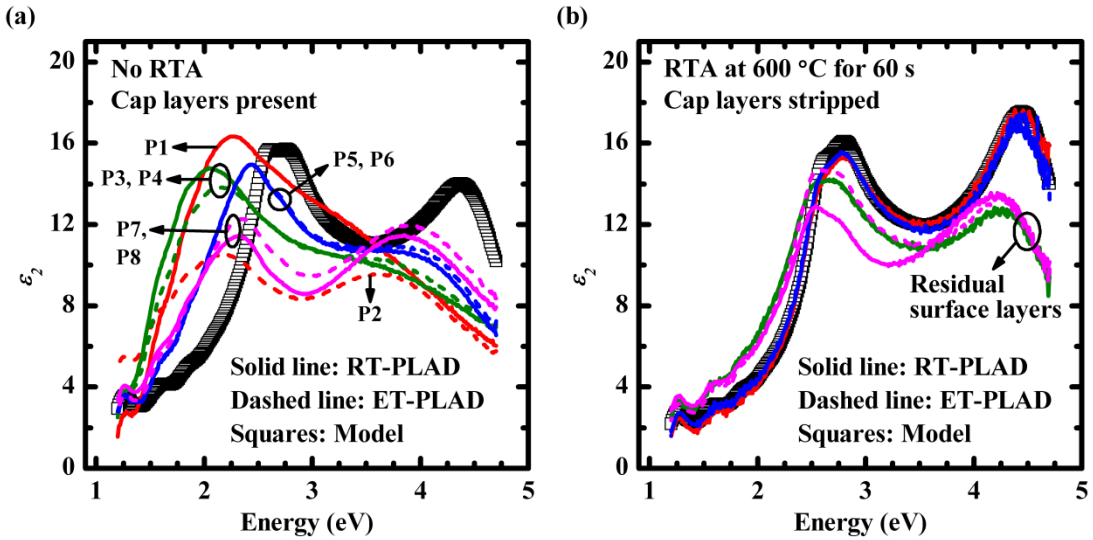

Fig. 5.6. Measured UV-VASE data (a) before RTA and (b) after RTA, obtained from samples doped by PLAD. Solid lines are used for RT-PLAD samples, while dashed lines are used for ET-PLAD samples. The modeled ε_2 profiles for 4 nm Al_2O_3 (cap layers present) or 1.7 nm InGaAs oxide (cap layers stripped), formed on 500 nm p^- $In_{0.53}Ga_{0.47}As$ on 500 μm p^+ InP, are also plotted (open squares).

needed for the dopant activation anneal. For the annealed samples, UV-VASE data was obtained before and after removal of the cap layers on the surface using a few cycles of buffered oxide etch, but only the data after removal is shown [Fig. 5.6(b)]. While the cap layers have some influence on the ε_2 profiles, as seen in the UV-VASE data from annealed samples prior to cap layer removal (not shown), they do not affect the assessment of crystallinity. The modeled ε_2 profiles for 4 nm Al_2O_3 (cap layers present) or 1.7 nm InGaAs native oxide (cap layers stripped), formed on 500 nm p^- $In_{0.53}Ga_{0.47}As$ on 500 μm p^+ InP, are also plotted in Figs. 5.6(a) and 5.6(b), respectively.

Without RTA [Fig. 5.6(a)], Splits P1, P3, and P4 exhibit amorphous characteristics, while the rest have likely maintained a fair degree of crystallinity. In fact, the excellent crystallinity of the as-implanted sample from Split P8 is verified by the TEM images in Fig. 5.5. Comparing Splits P1 and P2, it appears that ET-PLAD can help to suppress amorphization. However, a higher dose (Splits P3 and P4) is more amorphizing, such that an elevated substrate temperature of 100 °C during PLAD is unable to maintain crystallinity. In this case, a higher substrate temperature is required.

It is noted that a higher substrate bias for PLAD appears to be less amorphizing (Splits P5, P6, P7, and P8). This might seem contradictory, as one may expect higher energies to cause more amorphization as in the case of beam-line ion implantation. However, the PLAD mechanism is more complex than beam-line ion implantation. The ions that are implanted during PLAD have a distribution of angles, energies, and masses, due to collisions between ions and neutrals within the plasma sheath and the lack of mass separation. This stands in contrast to beam-line ion implantation, where mass analyzer magnets provide selection of ion mass, the ions are

accelerated (or decelerated) to a single desired energy, and the ion beam is directional. In PLAD, the plasma characteristics (e.g. density and pressure) and the substrate bias (e.g. magnitude, waveform, and frequency) have important influences on the dopant profile in the substrate and the properties of the doped layer. A larger substrate bias increases the maximum energy that can be attained by the implanted ions, but also increases the sheath thickness and results in more collisions between ions and neutrals in the sheath, which broadens the ion energy distribution and reduces the mean ion energy [202]-[204]. Increased collisions in the sheath also result in a higher proportion of lighter ions [204]. The broadened energy distribution, lower mean ion energy, and lighter ions could account for the reduced amorphization at larger substrate bias.

After RTA [Fig. 5.6(b)], all the PLAD samples recover almost completely towards the pristine crystalline InGaAs. The splits with a lower dose have ε_2 profiles that match almost perfectly with the modeled profile. The splits with a higher dose have residual surface layers that were not completely etched away, which alters their ε_2 profiles.

Secondary ion mass spectrometry (SIMS) was done on Splits P7 and P8 before and after RTA, and the Si concentration depth profiles in the InGaAs are plotted in Fig. 5.7. The SIMS was done at the Institute of Materials Research and Engineering (IMRE) as a paid service. The Si counts were converted to Si concentration by application of a relative sensitivity factor obtained from a calibration $In_{0.53}Ga_{0.47}As$ sample implanted with a known Si dose and analyzed using the same SIMS conditions. The surface-peaked Si profiles, which are typical of PLAD due to the ions possessing a distribution of energies, are beneficial for lowering contact resistivity.

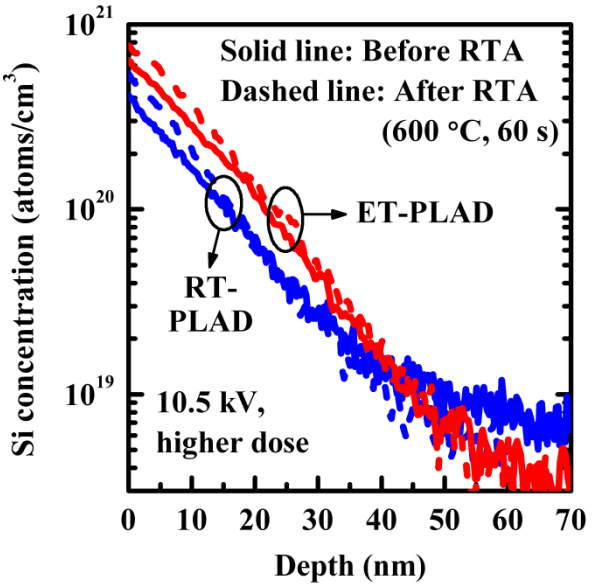

Fig. 5.7. Si concentration depth profiles in InGaAs for Splits P7 and P8 before and after RTA, showing higher Si surface concentration and higher Si dose for ET-PLAD than for RT-PLAD. The Si surface concentration and Si dose increase after RTA for both RT-PLAD and ET-PLAD, due to diffusion of Si dopants from the Al_2O_3 cap into the InGaAs.

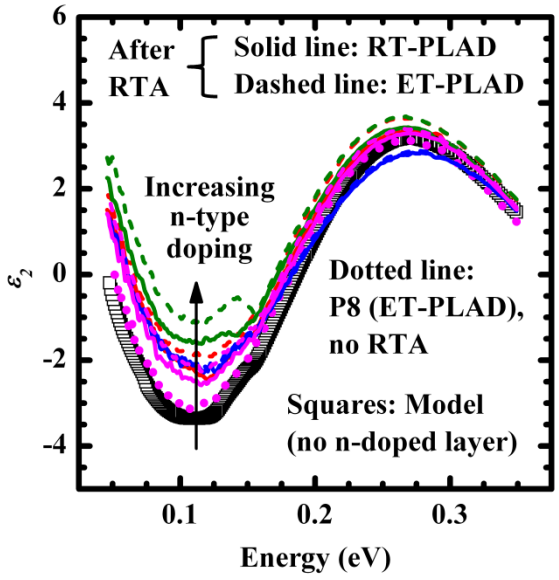

Fig. 5.8. Measured IR-VASE data for all PLAD splits after RTA at 600 °C for 60 s. The measured ε_2 profile for Split P8 before RTA and the modeled ε_2 profile for 5.5 nm native SiO_2 on 4 nm Al_2O_3 on 500 nm p^- $In_{0.53}Ga_{0.47}As$ on 500 μm p^+ InP are also plotted.

The additional SiO_x and/or Si layer that was seen in the TEM images in Fig. 5.5 can also be seen in the SIMS raw data (not shown). A portion of the total PLAD dose is lost due to deposition of this layer, and also due to some dopants stopping in the Al_2O_3. It is observed that ET-PLAD gives higher Si surface concentration and Si dose in the InGaAs than RT-PLAD. In addition, the Si surface concentration and Si dose increase after RTA for both RT-PLAD and ET-PLAD, due to diffusion of some Si dopants from the Al_2O_3 cap into the InGaAs. Before RTA, the Si doses in the InGaAs for RT-PLAD and ET-PLAD, calculated by integrating the Si concentration depth profiles in Fig. 5.7, are 4.7×10^{14} and 7.6×10^{14} cm^{-2}, respectively. After RTA, the doses increase to 5.5×10^{14} and 9.3×10^{14} cm^{-2}, respectively.

Infrared variable angle spectroscopic ellipsometry (IR-VASE) [225] was used to examine the activation of the Si dopants in the InGaAs. Fig. 5.8 plots the ε_2 profiles in the IR regime obtained from all the PLAD splits after RTA, along with the ε_2 profile from Split P8 (ET-PLAD) before RTA and the modeled ε_2 profile for 5.5 nm native SiO_2 on 4 nm Al_2O_3 on 500 nm p^- $In_{0.53}Ga_{0.47}As$ on 500 μm p^+ InP. The ε_2 profile from Split P8 before RTA shows only a slight increase in free carrier absorption compared to the modeled profile. Therefore, there is little active n-type doping before RTA, even for ET-PLAD with a substrate temperature of 100 °C. After RTA, significant increases in free carrier absorption are observed for all splits, indicating the activation of Si dopants, which forms a layer of n-type InGaAs. Further in-depth analysis of the IR-VASE data can also yield parameters such as electrical resistivity, mobility, and thickness of the charge layer. Preliminary analysis gives a mobility of ~800 $cm^2/V{\cdot}s$ for Split P4.

The current-voltage characteristics obtained from the TLM structures are highly linear (not shown), indicating the formation of good ohmic contacts on the n-

doped InGaAs. The sheet resistance R_{sheet} extracted from the TLM structures is plotted in Fig. 5.9 for Splits P7 and P8. Lower R_{sheet} is obtained for ET-PLAD than for RT-PLAD, which may be attributed to enhanced doping in the form of higher active doping concentration and/or a thicker n-doped layer, as seen from SIMS (Fig. 5.7) and IR-VASE (Fig. 5.8) data. In comparison, the sheet resistances extracted from TLM structures on samples doped by beam-line implant are ~250 to ~300 Ω/square. Fig. 5.10 shows the current-voltage characteristics of diodes with dimensions of $L_{diode}\times L_{diode}$ and the extracted ideality factor n, obtained from Splits P7 and P8. As the contacts to the n-doped InGaAs are ohmic, the measured characteristics are those of the p-n junction diodes formed by the PLAD. The RT-PLAD and ET-PLAD samples show similar diode characteristics, with a difference of ~6 orders of magnitude between forward and reverse currents, and an average ideality factor of 1.31 for RT-PLAD and 1.33 for ET-PLAD. Diodes fabricated on blanket RT-BL and ET-BL samples display a comparable ideality factor of ~1.3 to ~1.4.

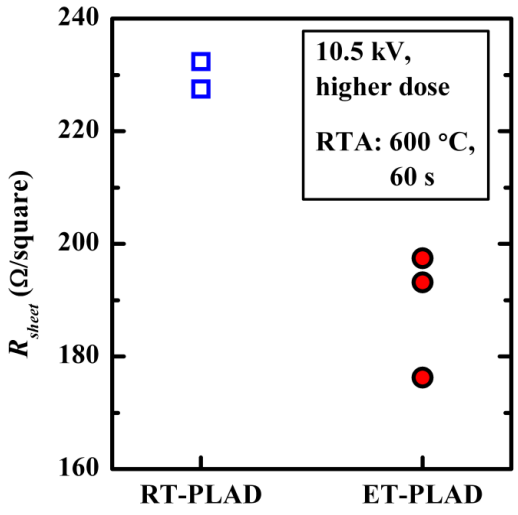

Fig. 5.9. R_{sheet} extracted from TLM structures for Splits P7 and P8 after RTA at 600 °C for 60 s. Lower R_{sheet} is obtained for ET-PLAD than for RT-PLAD, which may be attributed to a higher doping concentration and/or a thicker doped layer as seen from SIMS (Fig. 5.7) and IR-VASE (Fig. 5.8) data.

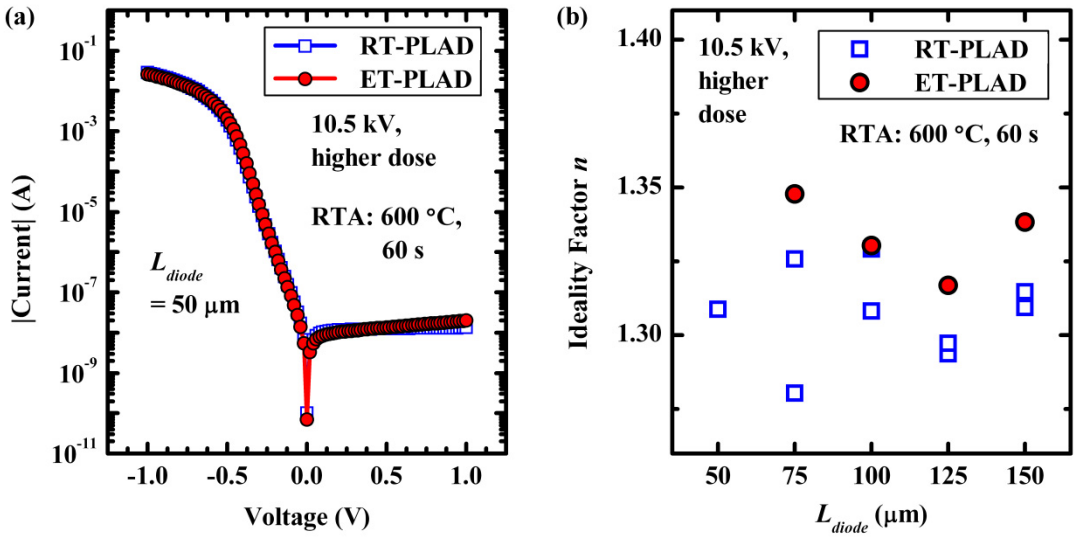

Fig. 5.10. Diodes formed by RT-PLAD and ET-PLAD exhibit similar diode characteristics, with a difference of ~6 orders of magnitude between forward and reverse currents, and reasonable ideality factor ranging from 1.28 to 1.35.

5.4 PLAD ON SMALL FIN STRUCTURES

Small fins defined by electron beam lithography (EBL), with widths ranging from 25 to 95 nm, were fabricated using the same process flow as in Fig. 5.1, except a different starting substrate was used and the mesa patterning and etch were done as the first step in order to form the fins prior to PLAD. The EBL was done at DSI as a paid service. The starting substrate for the fins is 50-nm-thick (001) $In_{0.53}Ga_{0.47}As$ with p-type doping concentration of ~5×10^{16} cm^{-3} on 500-nm-thick (001) $In_{0.52}Al_{0.48}As$ (undoped or with low p-type doping of ~1×10^{17} cm^{-3}), grown on bulk InP with p-type doping concentration of ~5×10^{18} to ~5×10^{19} cm^{-3}. The fin etch was ~100 nm deep, etching beyond the InGaAs into the InAlAs.

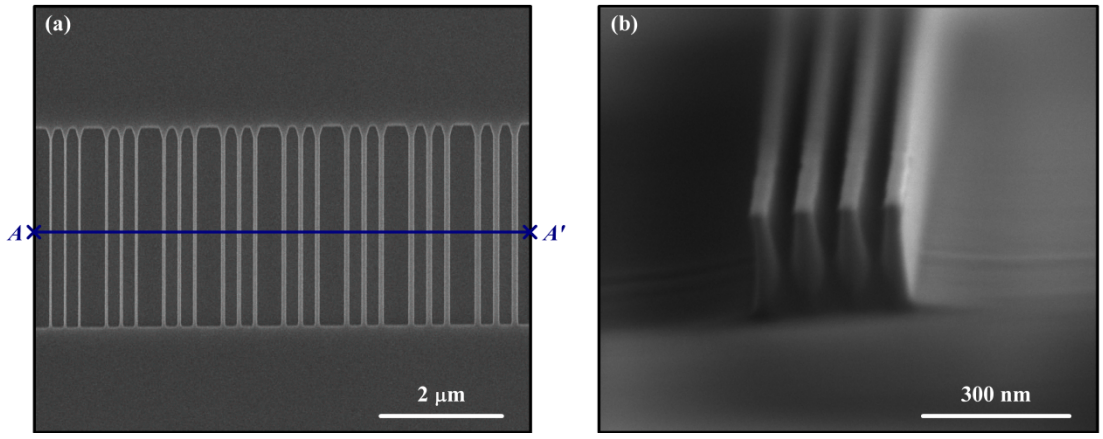

Fig. 5.11. (a) Top-view SEM image of fins that were cut for TEM. The FIB cut is made along the line *A-A'*. (b) Tilt-view SEM image of standalone fins.

The fins were used for TEM analysis to examine the InGaAs crystallinity after RTA. Fig. 5.11(a) shows a top-view scanning electron microscopy (SEM) image of fins that were cut for TEM, with the focused ion beam (FIB) cut line indicated by *A-A'*. All 24 fins in each sample were inspected by TEM for defects. A tilt-view SEM image of standalone fins is also provided in Fig. 5.11(b). Fins from Splits P1 and P6 were chosen for TEM based on the UV-VASE analysis of blanket samples (Fig. 5.6), which shows that the as-implanted PLAD samples from Splits P1 and P6 are amorphous and crystalline, respectively.

TEM images of fins from Split P1 are shown in Figs. 5.12, 5.13, and 5.14, while TEM images of fins from Split P6 are shown in Figs. 5.15 and 5.16. Some corner rounding of the fins is observed, which is desirable for reducing the electric field at the corners. However, extensive defects can be clearly seen at the corners of the fins from Split P1 (Figs. 5.13 and 5.14). These corner defects are similar to the multiple twin boundary defects along the {111} plane observed in Si fins doped by beam-line ion implantation in Ref. [221], and are consistently seen for all 24 fins of varying width (25-95 nm) in Split P1.

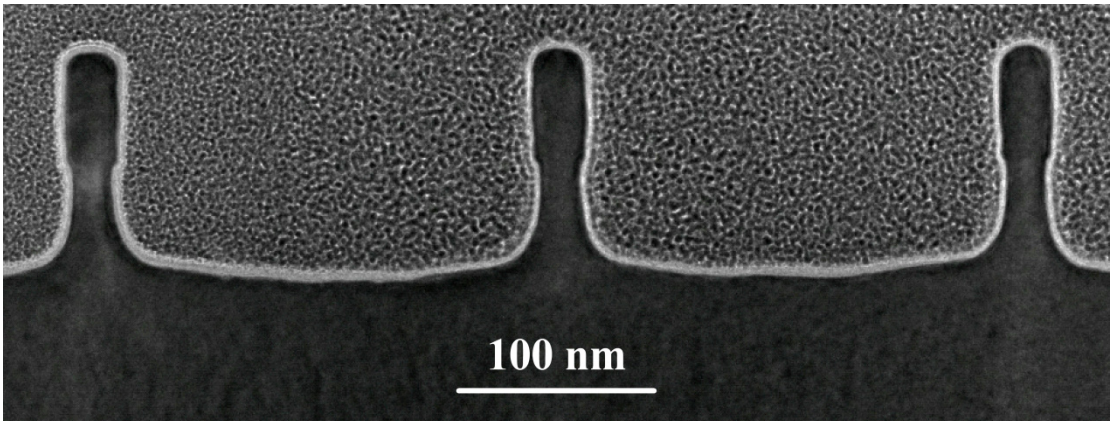

Fig. 5.12. Cross-sectional TEM image of a set of three 25-nm-wide fins from Split P1 after RTA. The fins are identical to each other, with rounded corners and vertical sidewalls.

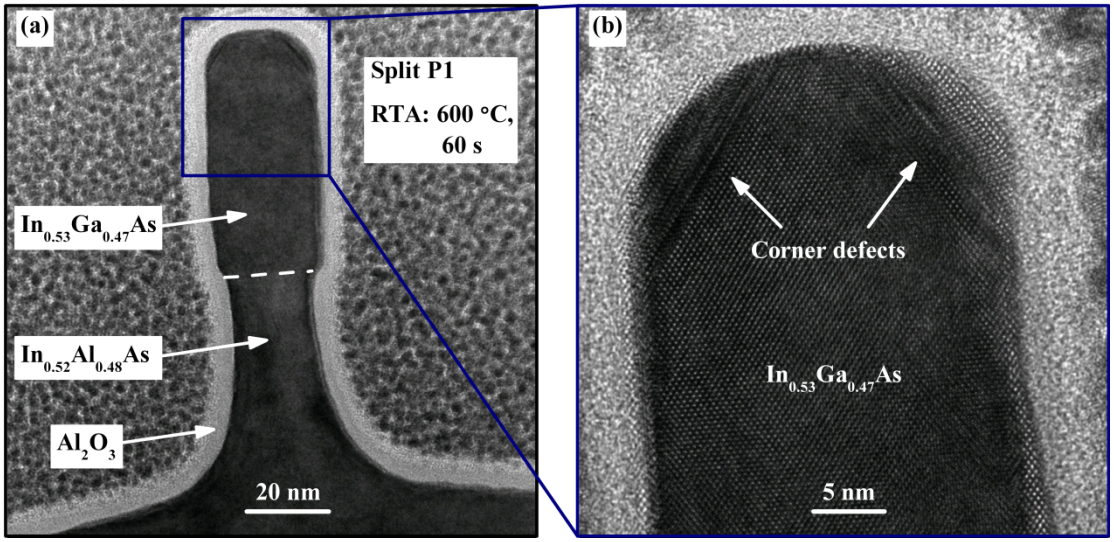

Fig. 5.13. (a) Cross-sectional TEM image of a single 25-nm-wide fin from Split P1 after RTA. The dashed line indicates the interface between InGaAs and InAlAs. (b) High-magnification view of the top portion of the fin, showing that corner defects remain after anneal for fins that are amorphized during plasma ion implantation.

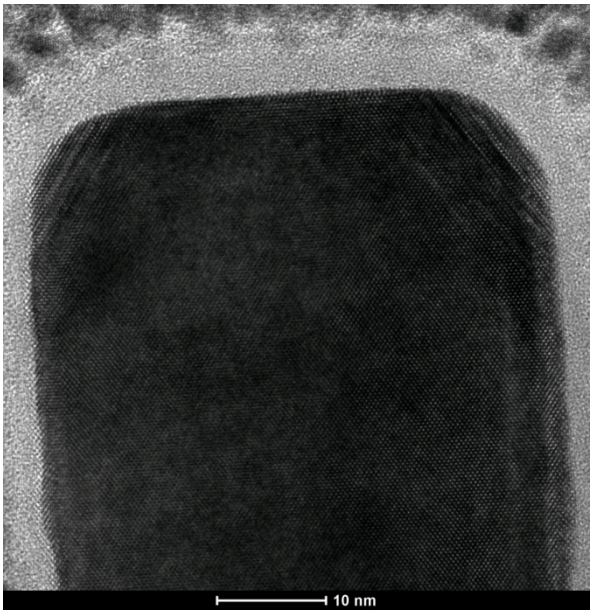

Fig. 5.14. High-magnification TEM image of the top portion of a 48-nm-wide fin from Split P1 after RTA. Like the fin in Fig. 5.13, corner defects are present after anneal due to amorphization during plasma ion implantation, despite the larger fin width.

On the other hand, the corner defects are suppressed for all 24 fins of varying width (25-95 nm) in Split P6, resulting in fins that are free of visible defects (Figs. 5.15 and 5.16). This highlights the importance of maintaining the crystallinity of the fins during implantation of the ions. By preventing amorphization in the as-implanted fins, the lack of crystalline seed for recrystallization and the presence of residual corner defects after RTA can be circumvented. This can be achieved by careful optimization of the PLAD conditions, possibly with the aid of an elevated substrate temperature during PLAD.

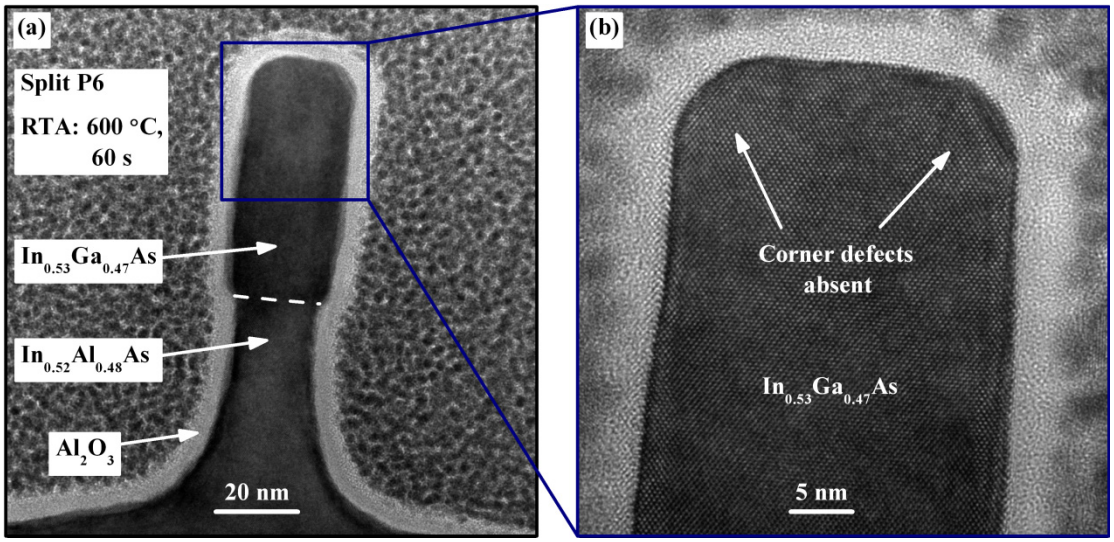

Fig. 5.15. (a) Cross-sectional TEM image of a 25-nm-wide fin from Split P6. The dashed line indicates the interface between InGaAs and InAlAs. (b) High-magnification view of the top portion of the fin, which shows that residual corner defects are absent after dopant activation anneal when the crystallinity of the fins is preserved during plasma ion implantation.

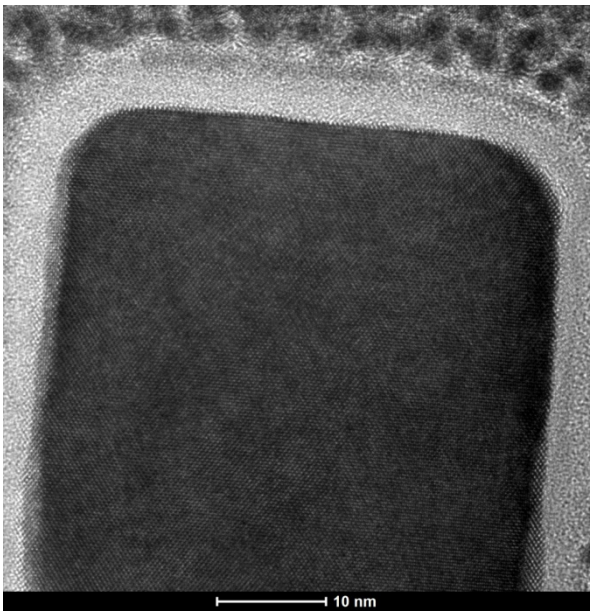

Fig. 5.16. High-magnification TEM image of the top portion of a 47-nm-wide fin from Split P6 after RTA. Like the fin in Fig. 5.15, no corner defects are present after anneal due to the suppression of amorphization during plasma ion implantation.

5.5 CONCLUSIONS

Plasma doping of InGaAs at an elevated substrate temperature was investigated for the first time and compared against plasma doping with the substrate kept at room temperature. An elevated substrate temperature during plasma doping can potentially help to maintain good crystallinity as-implanted. Elevated-temperature plasma doping also gave higher dose and surface concentration in blanket samples than room-temperature plasma doping, leading to lower sheet resistance. Small fins that are amorphized during plasma ion implantation are found to have residual corner defects after dopant activation anneal, whereas visible defects are absent in fins that remained crystalline during plasma ion implantation, showing the importance of avoiding amorphization in small fins.

Chapter 6

Summary and Future Directions

6.1 CONTRIBUTIONS OF THESIS

As explained in Chapter 1, high-mobility III-V semiconductors provide a compelling option for the replacement of Si as the channel material in metal-oxide-semiconductor field-effect transistors (MOSFETs), so as to maintain high performance in spite of the necessary reduction in supply voltage V_{dd} for lower power consumption.

However, the use of III-V MOSFETs in CMOS logic circuits faces challenges that need to be overcome before they are suitable for large-scale manufacturing, not least of which is the need for low parasitic resistances in MOSFETs with high-mobility channels and highly scaled dimensions. Crucially, the complexity and costs associated with the adoption of a disruptive technology such as III-V MOSFETs must be justified by substantial performance improvement and the ability to scale over multiple technology nodes. High parasitic resistances can limit the performance of III-V MOSFETs, preventing them from realizing their full potential and potentially jeopardizing their adoption in industry.

Therefore, this thesis has explored and developed contact and source/drain (S/D) engineering techniques for advanced InGaAs n-channel MOSFETs (n-MOSFETs), with the potential to not only achieve low parasitic resistances, but also fulfil the important requirements of abrupt, ultra-shallow, and high-quality junctions for control of short-channel effects (SCEs), and doping conformality for three-

dimensional (3D) device architectures such as fin field-effect transistors (FinFETs). These techniques are studied in Chapters 2 to 5, and the results and their significance are summarized in the following subsections. Finally, suggestions on possible future directions for expanding on the research in this thesis are provided in Section 6.2.

6.1.1 Salicide-like S/D contact metallization for InGaAs MOSFETs

The direct reaction of metals with InGaAs opens the doorway to the formation of self-aligned S/D contact metallization in InGaAs MOSFETs using a process similar to the self-aligned silicide ('salicide') formation process in Si technology [110]-[116]. Salicide formation has been an important technology for S/D resistance R_{SD} reduction in Si MOSFETs, as it places the S/D contact metallization directly adjacent to the gate spacer. Therefore, the formation of salicide-like contact metallization in InGaAs MOSFETs could also bring a similar benefit to InGaAs MOSFETs.

The reaction of Ti, Co, and Pd with $In_{0.53}Ga_{0.47}As$ was thus investigated by annealing for 60 s using different rapid thermal anneal (RTA) temperatures. Ti did not appear to react with $In_{0.53}Ga_{0.47}As$ up to 400 °C. On the other hand, Co completely reacts at 350 °C to form Co-InGaAs, and Pd completely reacts at 200 °C to form Pd-InGaAs. A low reaction temperature is important for minimizing S/D dopant diffusion and gate stack degradation. Both Co-InGaAs and Pd-InGaAs form ohmic contacts on n-type $In_{0.53}Ga_{0.47}As$ with active doping concentration of $\sim 2\times10^{18}$ cm^{-3}. X-ray photoelectron spectroscopy (XPS) analysis suggests that Pd could be the main diffusing species in the reaction with InGaAs.

Pd-InGaAs exhibits superior film properties compared to Co-InGaAs. Pd-InGaAs films formed at 200 and 250 °C are very uniform in both thickness and sheet resistance, and form a smooth interface with InGaAs. In contrast, Co-InGaAs forms a

rough interface with InGaAs. 20-nm-thick Pd-InGaAs formed at 250 °C has a sheet resistance of ~77 Ω/square.

Using ultra-violet photoelectron spectroscopy (UPS), the work function of the Pd-InGaAs formed at 250 °C is found to be ~4.6 ± 0.1 eV. Therefore, the Fermi level of Pd-InGaAs is close to the conduction band minimum of $In_{0.53}Ga_{0.47}As$, which should enable it to form a good ohmic contact on n-type $In_{0.53}Ga_{0.47}As$ with low contact resistivity ρ_c. However, the ρ_c of Pd-InGaAs on n-type $In_{0.53}Ga_{0.47}As$ with ~2×10^{18} cm^{-3} active doping concentration is ~8.35×10^{-5} $\Omega\cdot cm^2$, which is rather high. A higher substrate doping concentration will help to lower ρ_c, but the value of ρ_c may still be too high. This issue and the potential solutions will be discussed below in Section 6.2.

6.1.2 Comparison between self-aligned and non-self-aligned contact metallization in InGaAs n-MOSFETs

Simulations of $In_{0.53}Ga_{0.47}As$ n-MOSFETs with either self-aligned silicide-like (salicide-like) or non-self-aligned S/D contact metallization were used to ascertain the performance benefits derived from salicide-like contact metallization. For technological relevance, the simulated devices were calibrated to projections by the International Technology Roadmap for Semiconductors (ITRS) [181] for III-V high-performance logic technology. These include a gate length L_G of 15 nm, a supply voltage V_{dd} of 0.63 V, and a saturation threshold voltage $V_{t,sat}$ of 0.18 V.

The simulations show that while R_{SD} has a much less significant impact at highly scaled dimensions due to the close proximity of the via to the gate, self-aligned metallization (SAM) still provides drive current benefits over non-self-aligned

metallization (NSAM) with the same ρ_c due to its larger contact area, which reduces contact resistance R_c. The contact area advantage of SAM is especially important for small vias, which will continue to shrink with device scaling, leading to R_c becoming the dominant source of parasitic resistance.

The ρ_c needed in order to meet the ITRS parasitic S/D series resistance requirements for III-V high-performance logic is determined to be $\sim 1\times10^{-8}$ and $\sim 5\times10^{-9}$ $\Omega\cdot cm^2$ for SAM and NSAM, respectively. The lower R_c afforded by SAM allows it to outperform NSAM with the same ρ_c, down to values of ρ_c as low as 3×10^{-9} $\Omega\cdot cm^2$. At lower ρ_c, SAM gives lower performance than NSAM as it suffers from current crowding and higher spreading resistance induced by its recessed geometry, but this is eliminated by a raised S/D architecture, which allows SAM to outperform NSAM with the same ρ_c for any given value of ρ_c.

The results obtained from the simulations therefore clearly show the importance and usefulness of salicide-like S/D contact metallization, and provides ρ_c targets in order to meet ITRS requirements. From the simulations, it is also possible to determine the value of ρ_c needed for SAM to match or better the performance of NSAM with a given ρ_c.

6.1.3 Novel Si monolayer doping technique for InGaAs

A new Si monolayer doping (MLD) technique was developed for doping InGaAs n-type, and was successfully demonstrated in planar $In_{0.53}Ga_{0.47}As$ n-MOSFETs for the first time. This doping technique uses SiH_4 or Si_2H_6 gas treatment of the InGaAs surface to form Si monolayers on the InGaAs, with Si_2H_6 allowing a lower substrate or processing temperature. The dopant dose can be controlled by the

treatment time. Laser anneal is then used to drive in and activate the Si dopants to form n^{++} InGaAs.

At present, precious little has been reported on MLD for InGaAs, and the existing literature on MLD for III-V substrates has been confined to the use of sulfur (S) as the dopant [186]-[192]. Yet, Si remains the preferred dopant for n-type InGaAs [193]. The Si MLD technique developed therefore expands on MLD for InGaAs, and provides an alternative MLD solution for III-V materials.

The SiH_4 or Si_2H_6 gas treatment offers a way to conformally introduce dopants on the InGaAs surface, which is important for 3D device structures such as FinFETs and nanowire MOSFETs. A gas-based monolayer formation technique also offers the possible advantage of an *in situ* clean without breaking vacuum prior to monolayer formation. In addition, the use of laser anneal potentially allows doping concentrations above the solid solubility limit, and miminal dopant diffusion that enables abrupt ultra-shallow junction formation due to the ultrafast irradiation.

Experimental data shows that a laser anneal fluence of 100 mJ/cm^2 is able to produce n-type $In_{0.53}Ga_{0.47}As$ with very high doping concentrations (approaching 10^{21} atoms/cm^3 at the surface) and ultra-shallow junctions with good abruptness (~4-5 nm/decade) for both SiH_4 and Si_2H_6 treatments. Nearly ideal p-n junction diodes with ideality factor approaching unity were also formed on p-type $In_{0.53}Ga_{0.47}As$ by SiH_4 treatment at 500 °C and laser anneal at 100 mJ/cm^2. These were made possible by the absence of both implant-induced damage and melt-induced defects. $In_{0.53}Ga_{0.47}As$ n-MOSFETs with S/D regions doped by SiH_4 treatment at 500 °C and laser anneal at 100 mJ/cm^2 show well-behaved transfer and output characteristics, with crystalline channel and S/D regions and low gate leakage current.

Therefore, the Si MLD technique developed for InGaAs n-MOSFETs shows promise as an alternative to conventional beam-line ion implantation, which may not be suitable for conformally doping 3D device structures with extremely narrow pitch.

6.1.4 Plasma doping of InGaAs at elevated substrate temperature

Plasma doping (PLAD) was also studied as another doping option for InGaAs at advanced technology nodes. PLAD has been extensively reported for the doping of Si substrates [196]-[221], but has been largely neglected for other materials. PLAD is capable of forming ultra-shallow junctions with surface-peaked doping profiles, due to the range of energies of the ions implanted. PLAD also offers high throughput, thanks to high implant currents and simultaneous doping of the entire wafer surface. Most importantly, PLAD can conformally dope 3D structures such as trenches and fins [214]-[221], even those with high aspect ratio or narrow pitch. This is attributed to the distribution of angles that the implanted ions possess.

While conventional beam-line ion implantation has seen advancements that have enabled it to provide high throughput for high-dose, ultra-low-energy implantations of large wafers and is still suitable for 3D FinFET doping at the 14/16 nm technology node, its application could be restricted by angle limitations imposed by shadowing as fin pitch continues to shrink. In contrast, PLAD does not have the issue of a directional ion beam, and hence does not suffer from shadowing effects. Therefore, PLAD could have an important role to play in the doping of future generations of FinFETs. While PLAD has its own challenges in terms of process control (e.g. dose, contamination, uniformity, and repeatability), they can be overcome through the use of modeling, diagnostics, and sensors, which allows good process control comparable to that of beam-line ion implantation [207],[213].

Like beam-line ion implantation, PLAD is an implant-based doping technique. Therefore, it can also induce implant damage and can cause amorphization, although the amorphous layer may have slightly different properties due to the range of masses and energies of the implanted ions [202]. An elevated substrate temperature during PLAD provides dynamic annealing, and has been shown to suppress crystal defects and maintain crystallinity in Si substrates as-implanted [208]-[210]. However, this has not been reported for III-V substrates. Elevated-temperature PLAD (ET-PLAD) was thus studied for InGaAs for the first time.

ET-PLAD was found to provide higher Si dopant incorporation and lower sheet resistance in InGaAs than room-temperature PLAD (RT-PLAD). Of greater significance is the ability of an elevated substrate temperature to prevent amorphization of the InGaAs during PLAD. Small fins doped by PLAD highlight the importance of maintaining crystallinity during the plasma ion implantation, as residual corner defects after dopant activation anneal are observed in fins that are amorphized during PLAD, but not in fins where crystallinity is preserved throughout the process.

6.2 FUTURE DIRECTIONS

While promising new contact and S/D engineering technologies were explored and developed for advanced InGaAs n-MOSFETs, the technologies are still in the early stages of development. Much work is still needed to optimize the technologies and characterize their performance in advanced MOSFET architectures, creating opportunities for further research.

Salicide-like S/D contact metallization is a very recent development for III-V MOSFET technology. Ni-InGaAs contact metallization was first reported at the end of year 2010 [122]. Thus far, the lowest ρ_c reported for Ni-InGaAs on $In_{0.53}Ga_{0.47}As$ is ~1×10^{-6} $\Omega\cdot cm^2$, which is still not low enough despite a low- to mid-10^{19} cm^{-3} active donor concentration [136]-[137]. The ρ_c of ~8.35×10^{-5} $\Omega\cdot cm^2$ obtained for Pd-InGaAs on $In_{0.53}Ga_{0.47}As$, although at a lower active donor concentration of ~2×10^{18} cm^{-3}, is also rather high. Hence, the most pressing need for salicide-like contact metallization in III-V MOSFETs is a reduction in ρ_c. From the simulations in Chapter 3, the target ρ_c based on ITRS requirements is ~1×10^{-8} $\Omega\cdot cm^2$ for salicide-like S/D contact metallization. Therefore, the ρ_c of salicide-like S/D contact metallization such as Ni-InGaAs and Pd-InGaAs needs to be reduced by two to three orders of magnitude.

The ρ_c of Pd-InGaAs can be reduced by increasing the InGaAs doping concentration to mid-10^{19} cm^{-3}, possibly bringing it close to the 1×10^{-6} $\Omega\cdot cm^2$ obtained for Ni-InGaAs at the same doping concentration [136]-[137]. InGaAs with higher indium composition is also expected to produce lower ρ_c. However, these are not likely to be sufficient on their own, and other techniques will be required to achieve the desired ρ_c.

In order to reduce ρ_c to ~1×10^{-8} $\Omega\cdot cm^2$ and below, it is first necessary to gain more insight into the reasons for the ρ_c being high despite pinning of the Fermi level near the InGaAs conduction band and, in the case of Pd-InGaAs, a low work function. In fact, the work function of Pd-InGaAs (~4.6 eV) is lower than that of Pd (5.12 eV), yet its ρ_c is higher. The presence of interfacial layers such as excess elemental In, Ga, or As at the interface between Pd-InGaAs and InGaAs after reaction of Pd with InGaAs was cited as a possible reason in Chapter 2. Indeed, preliminary studies

performed by one of our collaborators show out-diffusion of substrate elements during the reaction between Ni and InGaAs, which results in InGaAs non-stoichiometry at the interface between Ni-InGaAs and InGaAs and leads to high ρ_c. It is found that the insertion of a capping layer between Ni and InGaAs can help to suppress the out-diffusion of substrate elements during the subsequent reaction, enabling the resulting Ni-InGaAs to achieve ρ_c as low as $\sim 4\times10^{-8}$ $\Omega\cdot cm^2$ on $In_{0.53}Ga_{0.47}As$ with active donor concentration of 3×10^{19} cm^{-3}. This is a major step towards ρ_c reduction for Ni-InGaAs contact metallization in InGaAs n-MOSFETs, as it makes Ni-InGaAs competitive with non-self-aligned Mo contact metallization, and can potentially be extended to other salicide-like contact metallization such as Pd-InGaAs.

Other than ρ_c reduction, another potential issue with Pd-InGaAs is its thermal stability, as a reaction or formation temperature of 350 °C results in a Pd-InGaAs film that has a degraded morphology and interface with InGaAs. While the formation temperature is not the same as the subsequent thermal budget that the Pd-InGaAs film can withstand without degradation, a low formation temperature tolerance could be indicative of poor thermal stability after formation. More studies are therefore needed to determine the thermal stability of the Pd-InGaAs film after it is formed. Ni-InGaAs exhibits degraded morphology and sheet resistance starting at 400 °C formation temperature, but the use of an interfacial layer between Ni and InGaAs has been shown to allow Ni-InGaAs formation temperatures of up to 500 °C without degradation [141]. An interfacial layer could therefore also be useful in the reaction between Pd and InGaAs if the thermal stability of the Pd-InGaAs film is a concern.

The selective etch of unreacted Pd, without affecting the Pd-InGaAs S/D contact metallization and other parts of the transistor, also requires further

development to improve the salicide-like process for Pd-InGaAs contact metallization in InGaAs MOSFETs. Extensive studies on selective wet etching of Ni have been done for Ni-InGaAs on both blanket [131] and transistor [141] samples, but no such reports exist yet for selective etching of Pd for Pd-InGaAs contact metallization.

The two-dimensional (2D) simulations in Chapter 3 can be extended to 3D simulations. While the 2D simulations give a good representation of the actual devices and provide useful and relevant insights, 3D simulations could give an even more accurate representation of 3D MOSFET architectures such as FinFETs, albeit at the cost of significantly increased simulation time and complexity.

The Si MLD technique developed in Chapter 4 is novel and thus not yet mature, and therefore needs to be optimized to achieve lower sheet resistance and contact resistivity. This can be done by incorporating more dopants or improving the activation efficiency. For instance, it has been reported that the material, stoichiometry, deposition method, and deposition temperature of the capping layer can affect the incorporation and activation of sulfur (S) dopants in InGaAs for S MLD, and that a bi-layer cap comprising a thin low-temperature oxide followed by a thicker high-temperature oxide works best in retaining S dopants on the surface during cap layer deposition and suppressing S outdiffusion during the activation anneal [192].

Various capping layer materials and thicknesses can therefore be studied for the Si MLD technique developed in Chapter 4 to get optimal doping, although the method used to deposit the capping layer should be conformal (e.g. atomic layer deposition) for 3D structures. A two-step anneal could also be explored, involving laser anneal at a low fluence of 100 mJ/cm^2 to achieve an abrupt ultra-shallow

junction with peak doping concentration at the surface, followed by a flash anneal or a second laser anneal for higher dopant activation without significant dopant diffusion.

Another obvious follow-up is the integration of the Si MLD technique in 3D MOSFETs such as FinFETs. While the planar $In_{0.53}Ga_{0.47}As$ n-MOSFETs demonstrated in Chapter 4 represent the first devices to successfully implement this novel Si MLD technique to dope the S/D regions, the performance of the doping technique needs to be evaluated for 3D devices in terms of conformality and resistance.

The application of the Si MLD technique to InGaAs with different indium compositions can also be investigated, with the different optical and thermal properties (e.g. band gap and thermal conductivity) potentially affecting the annealing conditions required for the optimal doping profile. In addition, gas-based MLD using other dopants can be explored, such as germane (GeH_4) treatment for the formation of germanium (Ge) monolayers.

The future research options suggested for the Si MLD technique developed in Chapter 4 can also be applied to the plasma doping (PLAD) of InGaAs that was studied in Chapter 5. These include the optimization of the capping layer and the dopant activation conditions for minimizing resistance, and the application of PLAD to InGaAs with different indium compositions, which may have different substrate temperature requirements for maintaining crystallinity during PLAD. The integration of PLAD in InGaAs FinFETs has also not been demonstrated before, providing an opportunity for further study. As part of the design and development of plasma-doped InGaAs FinFETs, an evaluation of sidewall doping at very narrow fin spacing, dopant profiling/mapping, and the extraction of top and sidewall sheet resistances from small

plasma-doped InGaAs fins patterned by electron beam lithography (EBL) would be useful.

In addition, the effect of the substrate temperature on sheet resistance can be investigated for PLAD. This has been reported for beam-line ion implantation, where it is proposed that increasing the amount of point defects without amorphization during implantation helps to improve Si activation in $In_{0.53}Ga_{0.47}As$ during the subsequent dopant activation anneal [226]. However, it should be pointed out that more non-amorphizing damage can also result in more residual defects (e.g. dislocation loops) after annealing, leading to higher leakage. Therefore, this warrants careful consideration.

Finally, co-dopants can also be introduced during PLAD. The doping of InGaAs by PLAD in Chapter 5 used only Si as an n-type dopant. Other n-type dopants such as S can be introduced together with Si into the InGaAs using PLAD, with the co-dopants implanted simultaneously or consecutively. Heavier elements, which cause more crystal damage as seen in the case of beam-line ion implantation, may require higher substrate temperatures during PLAD in order to maintain crystallinity.

From the lengthy discussion above, it is evident that there are many opportunities and avenues for continuing the research in this thesis. It is hoped that with further progress and optimization, at least a few of the promising contact and S/D engineering techniques developed in this thesis for advanced InGaAs MOSFETs will one day be production-worthy and ultimately help to advance technology by being adopted in industry.

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List of Publications as First Author

Journal Publications

1. **E. Y.-J. Kong**, Ivana, X. Zhang, Q. Zhou, J. Pan, Z. Zhang, and Y.-C. Yeo, "Pd-InGaAs as a self-aligned contact material on InGaAs," *Solid-State Electron.*, vol. 85, pp. 36-42, Jul. 2013.

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3. **E. Y.-J. Kong**, P. Guo, B. Liu, and Y.-C. Yeo, "Towards conformal damage-free doping with abrupt ultra-shallow junction: Formation of Si monolayers and laser anneal as a novel doping technique for InGaAs n-MOSFETs," *IEEE Trans. Electron Devices*, vol. 61, no. 4, pp. 1039-1046, Apr. 2014.

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1. **E. Y.-J. Kong**, X. Zhang, Ivana, Q. Zhou, and Y.-C. Yeo, "Pd-InGaAs as a new self-aligned contact material on InGaAs," *International Semiconductor Device Research Symposium (ISDRS)*, College Park, MD, USA, Dec. 7-9, 2011.

2. **E. Kong**, X. Gong, P. Guo, B. Liu, and Y.-C. Yeo, "Novel technique for conformal, ultra-shallow, and abrupt n^{++} junction formation for InGaAs MOSFETs," *International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, Hsinchu, Taiwan, Apr. 22-24, 2013.

List of Publications as Second Author

Journal Publications

1. S.-M. Koh, **E. Y.-J. Kong**, B. Liu, C.-M. Ng, G. S. Samudra, and Y.-C. Yeo, "Contact resistance reduction for strained n-FinFETs with silicon-carbon source/drain and platinum-based silicide contacts featuring tellurium implant and segregation," *IEEE Trans. Electron Devices*, vol. 58, no. 11, pp. 3852-3862, Nov. 2011.

2. H. X. Guo, **E. Y. J. Kong**, X. Zhang, and Y.-C. Yeo, "Germanium/Ni-InGaAs solid-state reaction for contact resistance reduction on n^+ $In_{0.53}Ga_{0.47}As$," *Japanese J. Applied Physics*, vol. 51, no. 4, Apr. 2012.

3. Ivana, **E. Y.-J. Kong**, S. Subramanian, Q. Zhou, J. Pan, and Y.-C. Yeo, "CoInGaAs as a novel self-aligned metallic source/drain material for implant-less $In_{0.53}Ga_{0.47}As$ n-MOSFETs," *Solid-State Electronics*, vol. 78, pp. 62-67, Jun. 2012.

4. S. Subramanian, **E. Y.-J. Kong**, D. Li, S. Wicaksono, S. F. Yoon, and Y-C. Yeo, "$P_2S_5/(NH_4)_2S_x$-based sulfur mono-layer doping for source-drain extensions in n-channel InGaAs FETs," *IEEE Trans. Electron Devices*, vol. 61, no. 8, pp. 2767-2773, Aug. 2014.

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1. S.-M. Koh, **E. Y. J. Kong**, B. Liu, C.-M. Ng, P. Liu, Z.-Q. Mo, K.-C. Leong, G. S. Samudra, and Y.-C. Yeo, "New tellurium implant and segregation for contact resistance reduction and single metallic silicide technology for independent contact resistance optimization in n- and p-FinFETs," *International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA)*, Hsinchu, Taiwan, Apr. 25-27, 2011, pp. 74-75.

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10 nm ultra-shallow junctions for advanced III-V logic devices," *International Conference on Solid-State Devices and Materials (SSDM)*, Fukuoka, Japan, Sep. 24-27, 2013.

Co-author contributions primarily comprise involvement in experiments, data collection and analysis, and technical discussions.

Also co-authored 3 journal publications, 2 letters/briefs, and 8 conference publications in addition to those first- and second-author publications listed above.