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Review of Nanosheet Transistors Technology

A B S T R A C T

Nano-sheet transistor can be defined as a stacked horizontally gate surrounding the channel on all direction. This new structure is earning extremely attention from research to cope the restriction of current Fin Field Effect Transistor (FinFET) structure. To further understand the characteristics of nano-sheet transistors, this paper presents a review of this new nano-structure of Metal Oxide Semiconductor Field Effect Transistor (MOSFET), this new device that consists of a metal gate material. Lateral nano-sheet FET is now targeting for 3nm Complementary MOS (CMOS) technology node. In this review, the structure and characteristics of Nano-Sheet FET (NSFET), FinFET and NanoWire FET (NWFET) under 5nm technology node are presented and compared. According to the comparison, the NSFET shows to be more impregnable to mismatch in ON current than NWFET. Furthermore, as comparing with other nano-dimensional transistors, the NSFET has the superior control of gate all-around structures, also the NWFET realize lower mismatch in sub threshold slope (SS) and drain induced barrier lowering (DIBL).

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مقال حول تقنية ترانزستورات الصفائح النانوية.

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الخلاصة

من الممكن تعريف ترانسستورات الصفائح النانوية على اساس انها عناصر مكونة من طبقات مجمعة بصورة افقية والقناة فيها محاطة بالبوابة من جميع الاتجاهات . حيث يكتسب هذا التركيب الجديد من (الترانسستورات) اهمية بالغة جدا من قبل الباحثين نتيجة السعي المتواصل والمستمر من قبلهم من أجل تصغير ابعاد الترانسستورات الحالية (تأثير المجال الزعنفية) الى اقل حجم ممكن. ولفهم خصائص وتراكيب هذه الترانزسستورات (الجديدة) وبصورة معمقة, قدم هذا البحث مراجعة ومسح تاريخي وعلمي لتطور صناعة الترانزسستورات المجالية (معدن –أوكسيد _شبه موصل). يتكون هذا الترانزسستور (الجديد) من بوابة مصنوعة من المعدن. تصل الابعاد (الجانبية) التصنيعية لترانزسستور الصفائح النانوية بحدود 3 نانوميتر. وكذلك تمت في هذه المراجعة دراسة ومقارنة تراكيب وخصائص لعدة انواع من الترانزسستورات (اقل من 5 نانوميتر) وهي ترانزسستورات الصفائح النانوية, الترانزسستورات المجالية الزعنفية, والترانزسستورات المجالية ذات القناة السلكية النانوية. وطبقا لهذه الدراسة والمقارنات, تبين بان هذا الانواع الجديدة من الترانزسستورات (ذات الصفائح النانوية) تمتلك خواص ومزايا منيعة لحالة عدم موائمة تيار التشغيل اكثر من النوع الاخر (الترانزسستورات المجالية ذات القناة السلكية النانوية). علاوة على ذلك ونتيجة المقارنات بين الانواع الثلاثة من حيث الابعاد الصغيرة, تبين بان الترانزسستورات ذات الصفائح النانوية تمتلك قابلية كبيرة جدا من ناحية السيطرة والتحكم على البوابة, واخيرا (نتيجة المقارنة) تبين بان الترانزسستورات من النوع (المجالية ذات القناة السلكية النانوية) هي الاقل موائمة مع منحني تحت العتبة وكذلك انخفاض الجهد نتيجة التيار المستحث.

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1. INTRODUCTION

In recent technology, the Nano-sheet Transistor is earning extremely high attention because it over comes on the physical limitation and fabrication challenges of the FinFET technology, and hence the performance improvements of the device is raising [1-2]. The NSFET is also known Multi Bridge Channel FET (MBCFET), the structure of NSFET is shown in Fig. 1 [3-4].

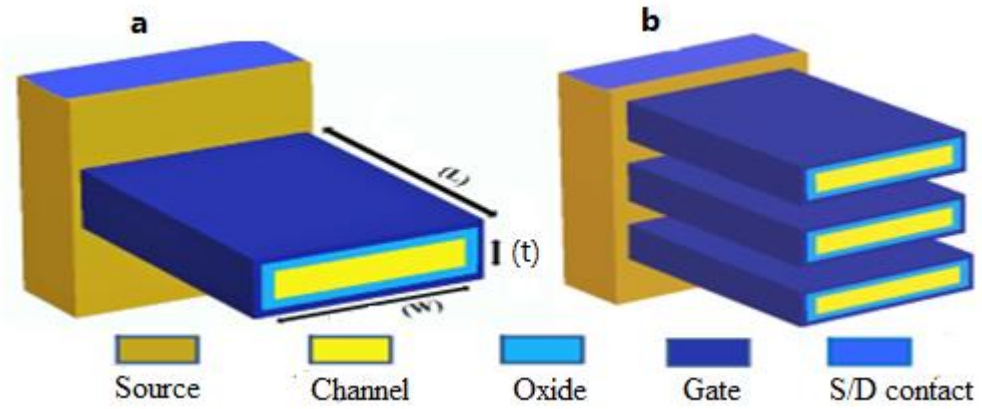

Fig. 1.NSFET structure (a) Single channel, (b) Multi channel. [4]

Fig. 1 (a) illustrates that the channel is surrounding by the gate in all directions, like a Gate All Around Field Effect Transistor (GAAFET), while in Fig. 1(b), the same channel of transistor in Fig. 1(a) but with multi configuration [5-6]. The characteristics of Nano-sheet transistor has been suggested by many researcher as a promising candidate for a large degree scaling in the process of manufacturing technology, Nano-sheet architecture has been proposed to substitute FinFET [7-8] and Nano-sheet technology node will be at 5nm lieu of 3nm [9]. NSFET exhibit excellent controlling on short channel, enables the effective width of the desired channel to be achievement in freedom, so the drive current ION will be higher as compared ION in FinFET [10-11]. Another advantages of NSFET has outstanding frequency response (faster) and support possibility multi-threshold- voltage [12]. Also NSFET offered better flexibility to self-heating effect (SHE) compared with FinFET [4]. On the other hand NSFET has a minimum of complex modeling design as in FinFET [8], and also it has a minimum of mismatch in threshold voltage and drain current as compared with NWFET, but it has a minimum of mismatch in Sub threshold Slope SS and DIBL [13].

Finally, NSFET can be resolved most problems and difficulties which are FinFET faced such as continuous scaling down (Fig. 2), short channel regression, manufacturing challenges and itself device performance was limited [14-16].

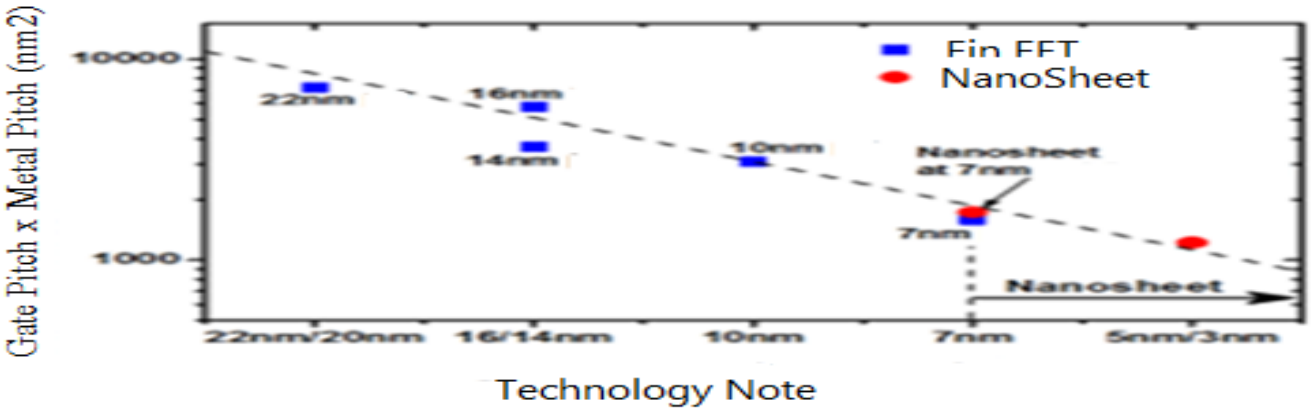

Fig. 2. Nanosheet structures will be a replacement of FinFET. [16]

2. NANO-SHEET AND FINFET

In 2019, Samsung Electronics company announced to modernize the process of a new node technology with 3nm nano-sheet [17]. This technology will represent a huge advancement in the world computing, and overcome all current physical limitation and electrical constraints. NSH technology will increase the performance of the device approximately 30-40%, saving the power consumption approximately 50% and saving the chip area approximately 45% [18-19]. NSFET or MBCFET (based on 3 nm), is considered the next generation of GAA technology [20]. Fig. 2 illustrates the downscaling of the technology nodes, where 22 nm processes (node) had been launched to the markets in 2012 and FinFET devices uses this process (22nm) based on Tri-Gate transistor, while 20 nm process is an intermediate half-node based on the 22 nm process [21-22].

The process of technology node (16 nm) launched in 2013, FinFET and NAND flash devices manufactured according to this node [23-24], while in 2014 multi-gate MOSFET devices is manufactured based on 14nm [23-24]. In 2016, later process is a non-planar development of planar CMOS technology at 10 nm [25]. Finally, 7 nm process (2018), where nano-sheet devices has been used and manufactured it according to the GAA and extreme ultraviolet lithography (EUV) technique. At this node (7 nm), began replacement FinFET device architecture by nano-sheet architecture, to boost further miniaturization to the 5nm and 3nm nodes [26-27].

Along the past decade, FinFET devices have been the major driver for fabrication logic gates-based on process technologies. Nevertheless, FinFET devices ultimately amount to a point where it cannot be scaled down further more [28]. In order to increase and continuous scaling down, the contact area between the gate and channel should be increase, and the method to make this is to use a GAA design as illustrated in Fig. 3 [29].

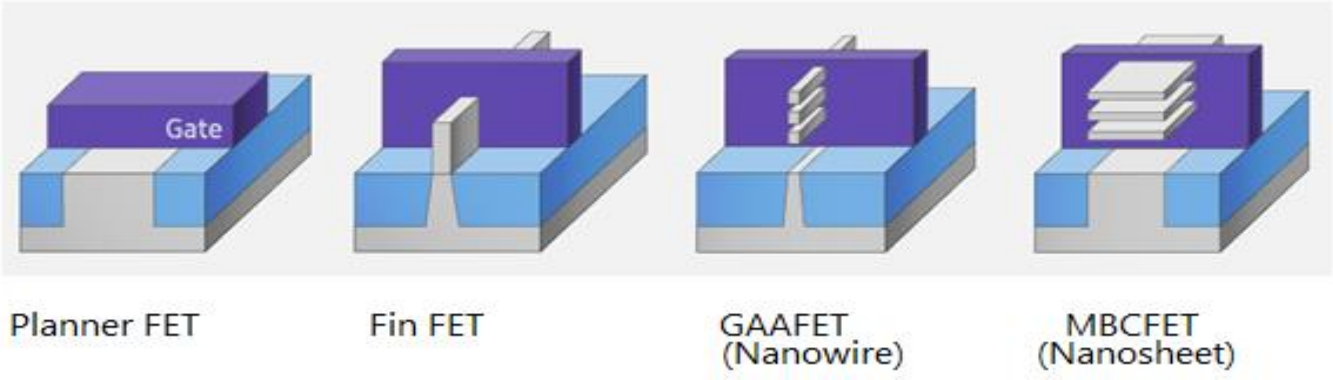

Fig. 3. Development of Field Effect Transistor from FinFET to MBCFET. [29]

GAA regulates the dimensions of the device to confirm that the gate is surrounding in four directions. This structure permits to GAA type to stack devices vertically instead of laterally [30].

The NSFET structure has a gate all around configuration that similar to the NWFET but unlike the structure of FinFET, its channel width is not limited, it is based on GAAFET [31-32]. Nano-sheet structures can responds to logic device needs at 5nm technology nodes and beyond. Stacked NS are fabricated with minimal deviation compared to the industry standard FinFET, essentially creates a device architecture with stacked layers of silicon sheets by retaining the silicon layers from a super lattice structure that consists of alternating crystal layers of silicon and silicon germanium internally developed EUV mask inspection tool.

The last form of GAA (Fig. 3) is nano-sheet devices or MBCFET, the channel seems to be horizontal sheet and hence the area of the channel is increased [33]. A key metric in MBCFET is width of the nano-sheet which defining the performance and power characteristics, that is to mean higher width, higher performance [34]. Another promise of MBCFET technology is reducing the operating voltage from 0.75 volts to 0.70 volts [35].

3. NSFET FABRICATION TECGNOLOGIES

NSFET devices can be fabricated with simple variation compared with the industry standard of the FinFET devices [8]. All the nano-sheets are intended to be stable in two dimension crystals under environmental conditions to show the rise in quality of the crystals[36-37]. The difference between FinFET and NSFET based on the structure is shown

in Fig. 4 [38]. we notice that more than one horizontal nano-sheet (multiple NS) can be used in MBCFET as a channel (surrounded with a gate in all directions) and these channels will be stacked vertically, while in FinFET, the channel (surrounded with a gate in three directions only) is limited , placed on vertically as a pillars and has a fixed height [38-40].

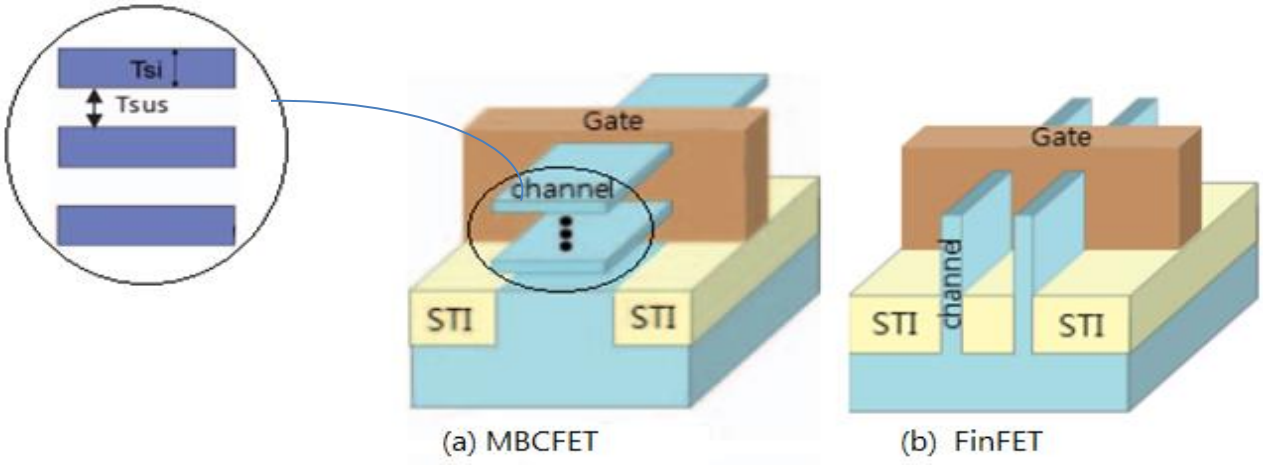

Fig. 4. Structureal comparison of FinFET and MBCFET. [38]

Different nano-sheet widths of MBCFET can be formed on the same wafer by using direct model, if the width of NS is narrow, then MBCFET can be used for low power applications or Static Random Access Memory (SRAM), while if the width was wider, the MBCFET can be used as high performance, so the optimization of the device can be achieved by using variable widths of NS [41]. The channel thickness of NSFET is defined as T_{si} , also known sheet thickness variation (STV) and the spacing between two sheets or suspension distance is defined as T_{sus} as shown in Figs. 4 and 5. if the channel thickness T_{si} is reduced, it will result to perpetuation of proper electrostatics, and if the space between two sheets T_{sus} is unequal ($T_{sus1} \neq T_{sus2}$), it will result to multiple threshold voltage (V_T) is been done, but if the distances between two sheets (T_{sus}) is minimum as possible as, the parasitic capacitance became minimize [42-45]. Fig. 5 illustrates the main steps of NSFET fabrications [46]. Meanwhile, NSFET is a GAA structure like the NWFET but unlike the NWFET its width of channel is not limited [47-48].

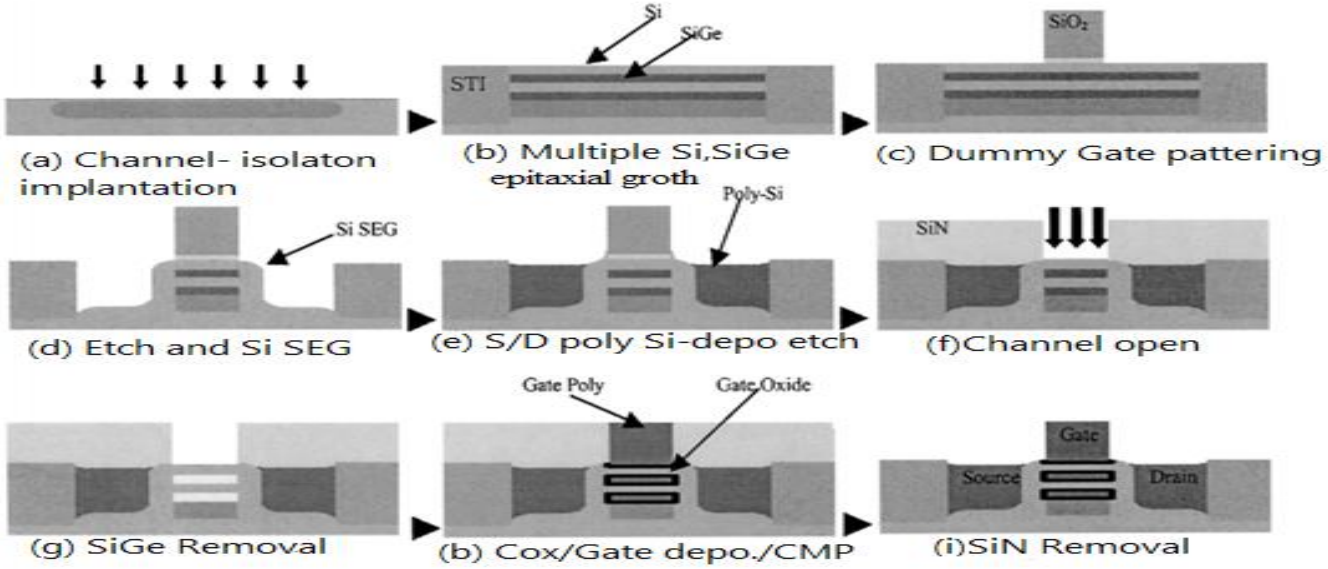

Fig. 5. Schematic diagrams for NSFET fabrication [47]

4. NSFET, FINFET AND NWFET COMPARISION

The electrical characteristics of NSFET is similar to the FinFET for the same cross section area but NSFET has the advantage of high on state current I_{ON} [49-50]. MBCFET exhibit the larger current (I_{ON}) is more 4.6 times comparison

with conventional MOSFET, sub threshold slope (SS) is an ideal value (≈ 60 mV/dec) [51-52], DIBL and I_{OFF} in Nanowire NWFET is better as compared to the NSFET [50]. Finally threshold voltage (V_T) in MBCFET is better as a compared with FinFET devices [53-57]. Fig. 6 illustrates the transient drain current response with time for FinFET, NWFET and NSFET. Fig. 7 shows the transfer characteristics of FinFET, NWFET and NSFET.

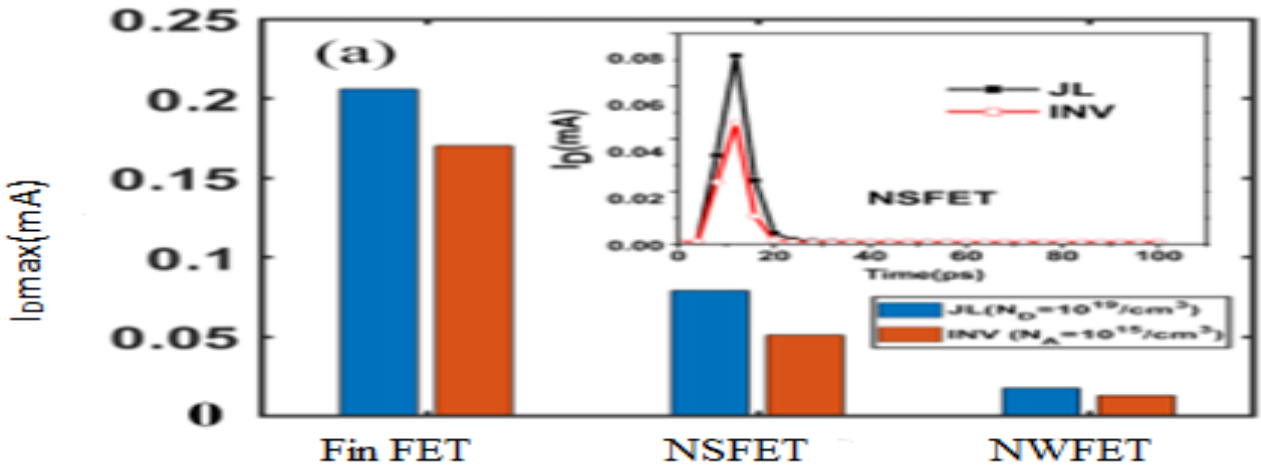

Fig. 6. Transient drain current vs. Time for the three transistors [52]

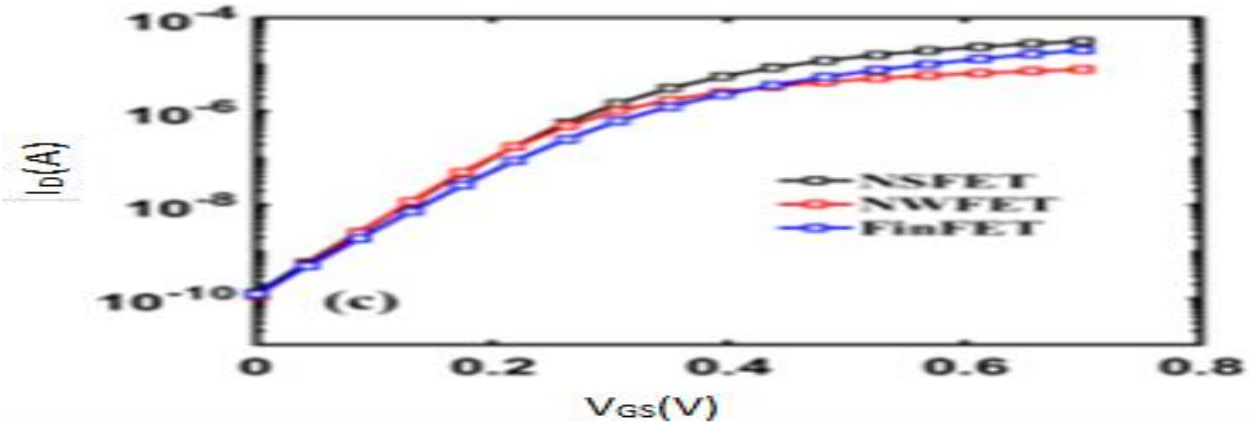

Fig. 7. Transfer charactersics of the three transistors [52].

TABLE 1
IMPORTANT COMPARISION PARAMETERS OF THE THREE STRUCTURE OF TRANSISTORS

Best value of	**NSFET Lg=12nm**	**FinFET Lg=15nm**	**NWFET Lg=12nm**	**Reference**
SS (mV/dec)	66	72		[31]
DIBL (mV/V)	32	55		[31]
V_T (mV)	0.315-0.337	0.276-0.338	0.231-0.262	[51]

5. CONCLUSION

This research reviews and presents the performances of NSFET and make a comparison with other nano-structure transistors like FinFET and NWFET. according to this comparison, the NSFET is the most nano-dimensional transistor suitable for the new 3nm node technology than the FinFET and NWFET because of its perfect electrical parameters like sub threshold Swing SS, DIBL, and Threshold voltage (V_T) with this node of technology. We found more dielectric in this structures and hence better ON current, also multi threshold voltages can be used in NSFET by using the verity metals in various gates. Finally to enhance the performance, at least dimensions, source and drain must be containing metals.

5. ACKNOWLWDGMENT

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