Ultra High Voltage IC design

With a 400V CMOS technology,
a dimmer application.

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Resumen Publicable

Con la popularización de tecnologías de fabricación de circuitos integrados de ultra alto voltaje (UHV), surge la posibilidad de diseñar circuitos integrados conectados directamente a la red de distribución, con aplicaciones en fuentes compactas, domótica, smart-grids, entre otras.

Este proyecto propone el diseño, fabricación y caracterización de circuitos en tecnología UHV. Se toma como ejemplo un atenuador por corte de fase de dos terminales.

Al momento de escribir esta tesis, no existen circuitos integrados comerciales que implementan un atenuador por corte de fase completo, ni se pudo encontrar artículos académicos haciendo referencia a dispositivos similares.

El circuito fue diseñado en una tecnología de 1 µm UHV MOS (XDM10 de XFAB) en una oblea de silicio sobre aislante (SOI). Puede operar con un ciclo de trabajo hasta 95 % de potencia (80 % en tiempo) y una carga de hasta 100 W, lo que es adecuado para lámparas atenuables de LED.

El área total de silicio ocupada es de 6.5 mm^2 sin contar pads. Debido a limitaciones tecnológicas, la versión final del atenuador es casi completamente integrada. Dos capacitores de bajo voltaje y cuatro diodos UHV quedan por fuera del ASIC.

Palabras Clave — circuitos integrados, ultra alto voltaje, dimmer, bajo consumo

Abstract

The advent of Ultra High Voltage (UHV) technologies for integrated circuit fabrication opens up new possibilities for the design of circuits that connect directly to the power distribution network, with applications in the design of compact power sources, domotics, smart-grids, etc.

This project proposes the design, fabrication and characterization of circuits in an UHV technology, of which a fully integrated two terminal phase-cut dimmer was chosen as an example.

At the time of writing this thesis, no commercially available integrated circuit exists that fully implements a phase cut dimmer, and no academic papers could be found referencing similar circuits.

The circuit was designed on a 1 µm UHV MOS technology in a silicon-on-insulator (SOI) wafer (XDM10 from XFAB). The dimmer can operate with a duty cycle of up to 95 % power (80 % time) and a load of up to 100 W which is adequate for modern domestic dimmable LED lights.

The total occupied silicon area is 6.5 mm^2 without pads. Because of technological limitations, the final version of the dimmer is almost fully integrated. Two low voltage capacitors and four UHV diodes are outside the ASIC.

Index Terms — integrated circuits, ultra high voltage, dimmer, low power

Acknowledgements

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Chapter 1

Introduction

1.1 The problem

Using extended and gradual diffusions, varying the levels of dopants, and utilizing also a thick gate oxide, ultra high voltage (UHV) technologies enable the fabrication of several variants of integrated MOS, BJTs, diodes and even IGBTs that can withstand up to hundreds of Volts [1, 2].

In the past, these technologies were highly specific and costly, but with the advent of domotics, LED lights, efficient power sources, micro-actuators and displays, their use has expanded to most consumer applications lowering the cost and having frequent multi-project wafer runs (MPW).

However, open fabs are still few and references with specific information such as [3, 4, 5] are scarce. Access to most information about UHV circuits is restricted, since most of the work on UHV requires a specific know-how and is being developed inside companies. Hence, academic work in this area results interesting.

A fully integrated phase cut dimmer was chosen as an example application to gain experience and propose innovative IC designs for feeding low power circuits.

1.2 In this thesis

Chapter 1 provides an introduction to the project including state of the art, the most significant design challenges, and the design specifications.

Chapter 2 is an introduction to the chosen fabrication technology, and a summary of the devices that were most significant to this project.

Chapter 3 describes in detail the schematic for each of the designed blocks, and the respective design decisions. This section also includes sizing of all components and devices.

Chapter 4 shows the schematics used for simulation and the results of said simulations for all blocks in the circuit.

Chapter 5 includes the physical layout of the circuit that was sent for fabrication, as well as a microscope image of the fabricated circuit.

Chapter 6 includes the measurements performed on the circuit after fabrication.

Chapter 7 provides a discussion and analysis of the results, and a comparison between expectations and final results.

Outside the main body of the thesis, two appendices are included that provide complimentary information to the main design activities.

Appendix A focuses on electrical current measurements for off-the-shelf lamps and an off-the-shelf discrete phase cut dimmer similar to the integrated dimmer that was designed in this project.

Appendix B includes the schematics and PCB layout that were necessary for connection to the integrated dimmer in the macroscopic world.

1.3 State of the art

Phase-cut dimmers are circuits that chop the 110 VAC to 230 VAC, 50 Hz to 60 Hz sine wave to the load to modulate power, as shown in Figure 1.1 and Figure 1.2 on the following page.

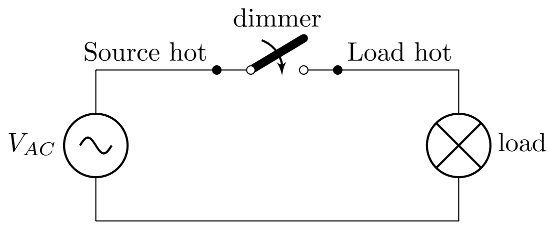


Figure 1.1: Application diagram of a phase cut dimmer

The classic implementation of this circuit uses a TRIAC as the main switch and a DIAC to trigger it because of its low cost although they present *leading-edge* limitations [6]. Over the last years, microcontroller [7] and IGBT [8] based solutions have been reported, which allow for a finer control of specially prepared LED and CFL lamps [9, 10].

Even though approximations to solving this problem such as [8] exist, no commercial integrated circuit (IC) exists that implements a complete dimmer with its own power management and a power switch stage.

1.3.1 Leading and Trailing Edge Dimmers

There are two basic dimmer strategies depending on the part of the sine wave that gets chopped called leading and trailing edge. Leading edge dimmers begin cutting off the AC sine wave right after it crosses zero, whereas trailing edge dimmers stop cutting off the AC sine wave when it crosses zero (see Figure 1.3 on page 14).

Classic TRIAC dimmers are of the leading-edge type because the TRIAC itself turns-off on the zero cross. On the other hand trailing edge dimmers are said to better control LED lamps because they usually represent a capacitive load, and an abrupt turn-on edge current spike is avoided.

1.4 Motivation

At the time of writing this thesis, no academic papers could be found referencing similar circuits.

BQN [11] is a local manufacturer and exporter of dimmer circuits, who has expressed interest in the development of this project for improving their existing technologies.

The research group at UCU has experience with HV technologies, and is looking to expand its areas of work into the novel UHV technologies and devices like integrated UHV IGBTs and diodes.

Therefore, academic research in this area is of interest.

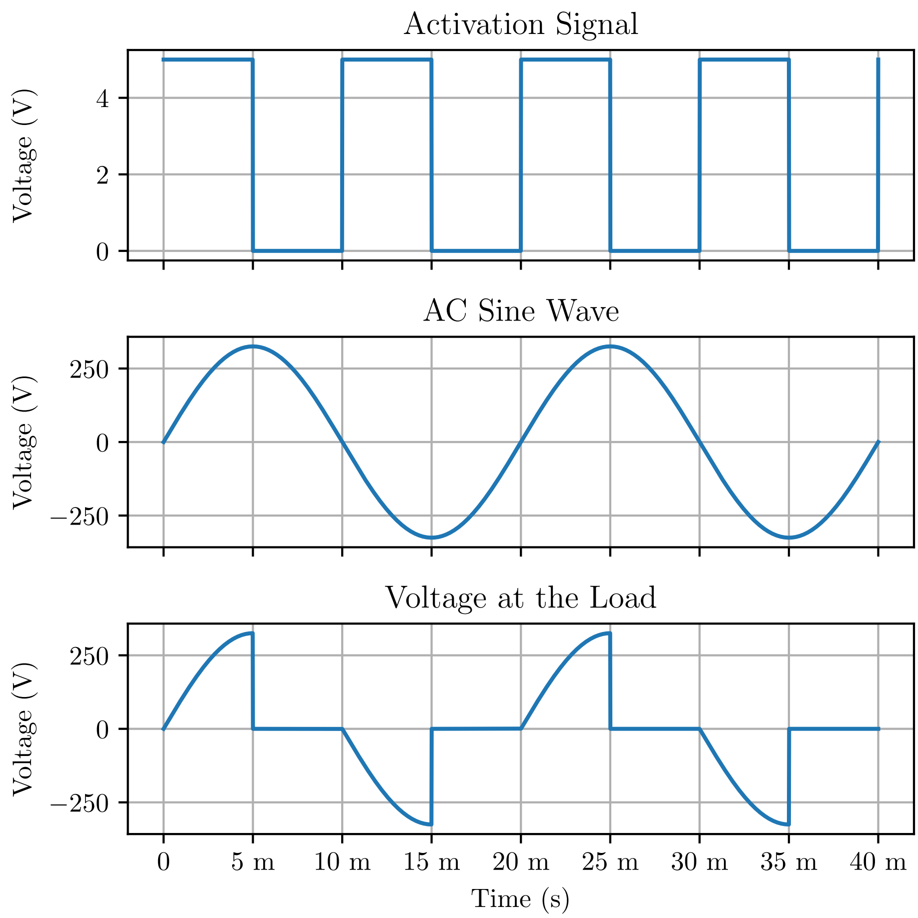


Figure 1.2: Load voltage example in a phase-cut dimmer.

1.5 Circuit Scheme

The proposed design is shown in Figure 1.4 on page 15, and it consists of six blocks that can be divided into power and logic related.

The power related blocks (double line in Figure 1.4 on page 15) are *Switches* through which power is delivered to the load, a *Gate Driver* to operate the switches, a *Power System* to manage and provide LV DC power to all the circuit blocks in Figure 1.4 on page 15 from the AC source, and a *Zero Crossing Detector* to keep the system in phase with the 50 Hz to 60 Hz sine wave.

The logic related blocks (single line in Figure 1.4 on page 15) are a *Delay Block*, that implements a finite state machine (FSM) to control the duty cycle of the switch activation, and an *Analog to Digital Converter* (ADC) to read an analog input to control the duty cycle.

Because the logic related blocks can be implemented with well-known and standard low power microcontrollers [7, 12], only the power related blocks are included in the current implementation of the design.

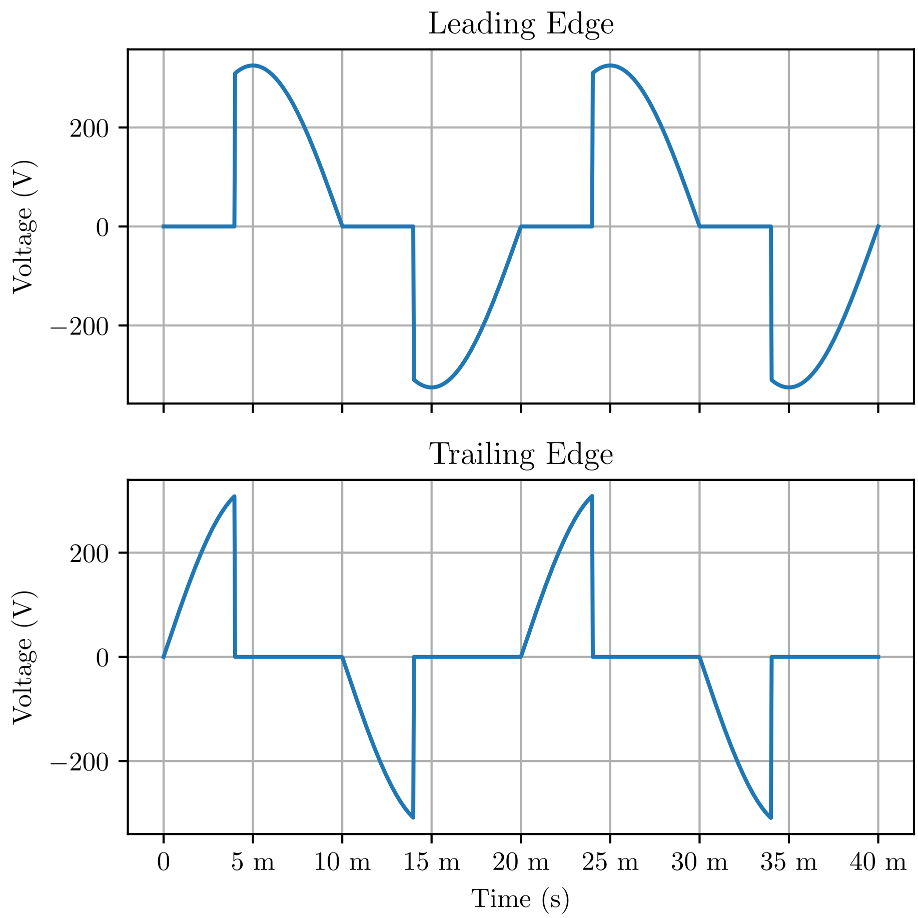


Figure 1.3: Dummy simulation to illustrate the difference between a trailing and leading edge dimmer.

1.6 Dimmer specifications

The aim of this project is to design, simulate and fabricate a functional prototype for an integrated phase cut dimmer.

Even though this is an academic project, decisions had to be made as if it were part of a commercial product. As such, the most important metrics are power consumption (limited by its ability to be embedded into a wall) and its ability to deliver power to a load.

A final design constraint was added to the silicon area it can occupy to be fabricated in a MPW, and have a low manufacturing cost compliant with a consumer application.

The full target specifications are shown in Table 1.1 on the following page.

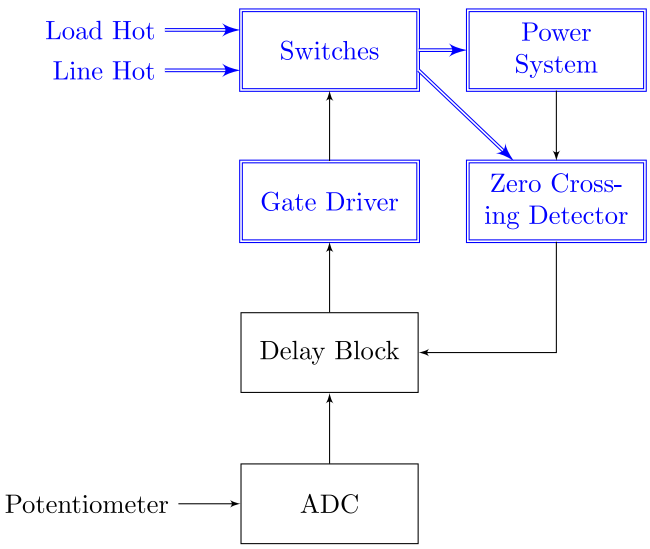


Figure 1.4: Top level blocks for the UHV dimmer. *Load Hot* and *Line Hot* are the dimmer terminals that connect to the load and to the grid respectively as shown in Figure 1.1 on page 12. *Potentiometer* is an extra analog input to control the duty cycle. Blue double line blocks represent power related blocks and single line blocks represent logic related blocks. Blue double line arrows represent UHV connections and single line arrows represent low voltage connections.

Measure		Value	Unit
Idle state power consumption	$\leq$	100	mW
On state power consumption	$\leq$	4	W
Max power percentage delivered to the load	$\geq$	95	%
Max power delivered to the load	$\geq$	100	W
Total silicon area	$\leq$	10	mm^2
Fully integrated		Yes	

Table 1.1: Target design specifications.

Chapter 2

UHV CMOS Technology Description

2.1 Introduction

The design of high voltage integrated circuits naturally requires the use of specially prepared fabrication technologies designed to withstand the elevated voltage levels of a typical domestic AC power network.

In this work, the selected process is XDM10 from XFAB [13, 14], a 1.0 µm Modular 350 V Trench Insulated BCD Process Technology on SOI wafer. This technology provides a wide variety of devices including high voltage MOS, BJTs and IGBTs, as well as regular 5 V core CMOS, high-resistivity poly resistors, 5 V Zener diodes, and Schottky diodes.

To withstand elevated UHV voltages, XDM10 includes dielectric trench insulation at wafer level [14]. Figure 2.1 on the next page shows a vertical cross section for low voltage CMOS transistors.

2.2 XDM10

There are three main aspects that make XDM10 from XFAB [13, 14] a suitable technology for UHV power switching applications.

First, the use of extended and gradual diffusions allows for UHV transistors with breakdown voltages of up to 400 V. The use of thick gate oxide allows for up to 20 V gate-source voltage, significantly higher than traditional CMOS technologies. Finally, trench isolation allows for UHV and LV devices to be fabricated in close proximity without the risk of latch up.

Figure 2.2 on page 18 shows a cross section of an UHV DMOS transistor displaying all three of these strategies.

XDM10 offers UHV MOSFETs, BJTs and IGBTs, as well as a 5 V CMOS core with a wide variety of ready to use digital and analogue cells. For analogue applications, several capacitor and resistor devices can be realized. Finally, isolating trenches allow for the use of forward diodes.

After careful study of the manufacturer's process specifications [15] and with aid of Spice simulations (Section 4.1), ni34b IGBTs were chosen as the main switching element of this circuit, because they provide the largest current per unit of area.

A summary of the available devices offered by the technology is shown in the tables indicated by Table 2.1 on the next page. All device characteristics are taken from the official XFAB

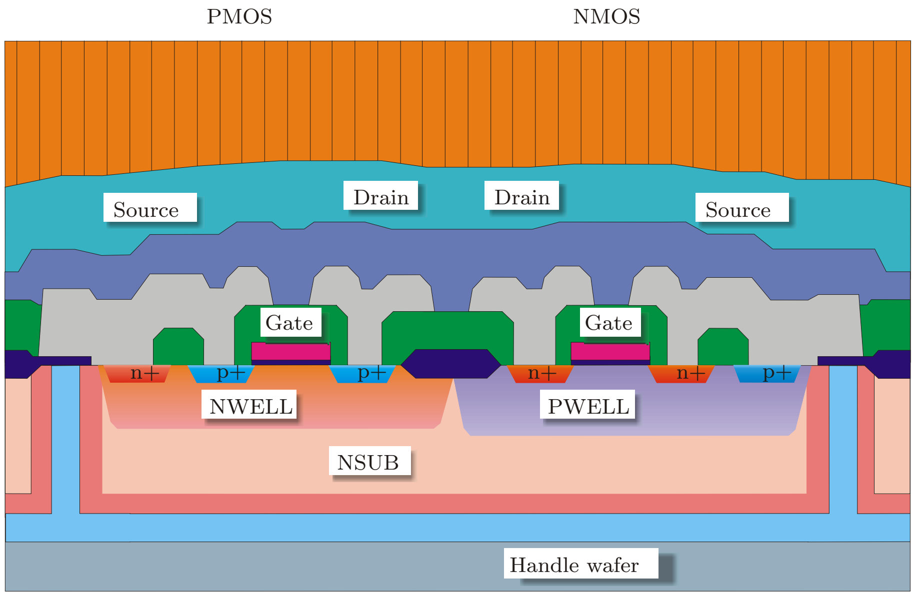


Figure 2.1: XDM10 core module cross section for low voltage CMOS transistors [15].

documentation [15, 16].

Device Type	Table	Page
LV CMOS	2.2	18
MV CMOS	2.3	18
UHV MOS	2.4	18
IGBT	2.5	19
BJT	2.6	19
Resistors	2.7	19
Diodes	2.8	19
Metal Layers	2.9	19

Table 2.1: Technology devices summary reference table.

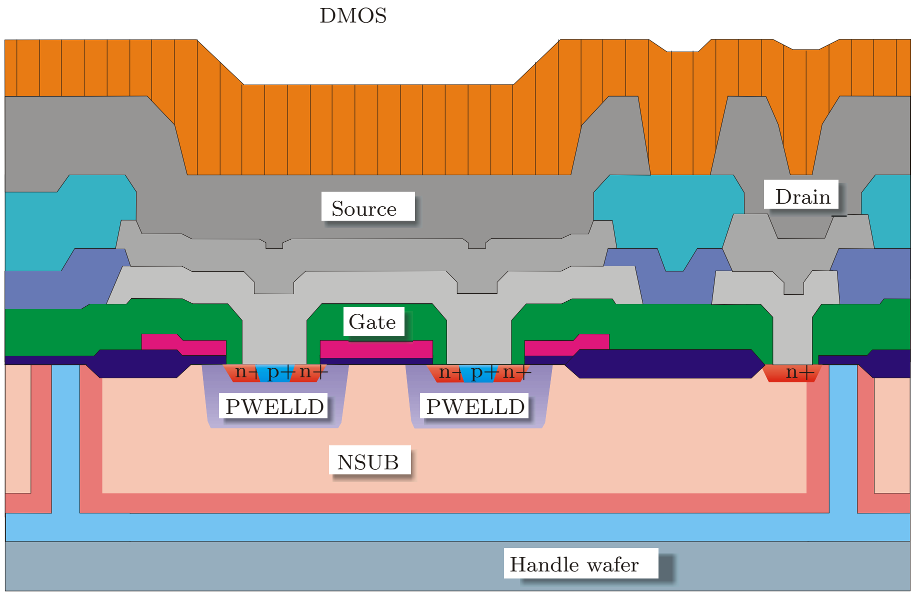


Figure 2.2: XDM10 core module cross section for an UHV DMOS transistor [15].

Device	Name	$\lvert V_T \rvert$ (V)	I_{DS} (µA/µm)	max $\lvert V_{DS} \rvert$ (V)	max V_{GS} (V)
5 V NMOS	ne	0.80	150	5.5	18
7 V NMOS	nea	0.86	150	7.0	18
5 V PMOS	pe	0.95	65	5.5	18
7 V PMOS	pea	0.95	65	7.0	18

Table 2.2: XDM10 LV CMOS device characteristics.

Device	Name	$\lvert V_T \rvert$ (V)	R_{ON} (kΩ · µm)	max $\lvert V_{DS} \rvert$ (V)	max V_{GS} (V)
20 V NMOS	nme	0.8	19	20	18
20 V PMOS	pme	0.75	60	20	18
15 V NMOS	nmea	0.78	15	15	18
20 V PMOS	pmea	0.62	45	20	18
32 V NMOS	nmeb	0.8	21	32	18

Table 2.3: XDM10 MV MOS device characteristics.

Device	Name	max $\lvert V_{DS} \rvert$ (V)	max V_{GS} (V)	max I_D (mA)
370 V DMOS, scalable	nd34a	340	20	20
370 V DMOS, 370 Ω	nd34bs	340	20	150
370 V DMOS, scalable, wide metal connect	nd34bsw	340	20	425

Table 2.4: XDM10 UHV MOS device characteristics.

Device	Name	$\lvert V_T \rvert$ (V)	$\max V_{CE}$ (V)	$\max V_{GE}$ (V)	$\max I_C$ (mA)
400 V IGBT	ni34b	1.7	340	20	220

Table 2.5: XDM10 IGBT device characteristics.

Device	Name	Beta (β)	V_{BE} (mV)	$\max V_{CE}$ (V)
370 V vertical	qnvd	65	650	330

Table 2.6: XDM10 BJT device characteristics.

Device	Name	R_S ($\Omega/\square$)	$\max V$ (V)
PWELLD	rpwd	1530	50
POLYD, P+ impl.	rpd	190	350

Table 2.7: XDM10 resistors device characteristics.

Device	Name	V (V)	max breakdown I (mA/µm)	max forward I (mA)
4.8 V Zener	dzeb	4.8	1	—
30 V Schottky	dsa	30	—	1

Table 2.8: XDM10 diodes device characteristics.

Device	Name	R_S ($\Omega/\square$)	$\max J/W$ (mA/µm)	$\max V$ (V)
Metal 1	rm1	0.05	0.8	350
Metal 2	rm2	0.05	0.8	350
Metal 3	rm3	0.013	7.0	350

Table 2.9: XDM10 power metal device characteristics.

Chapter 3

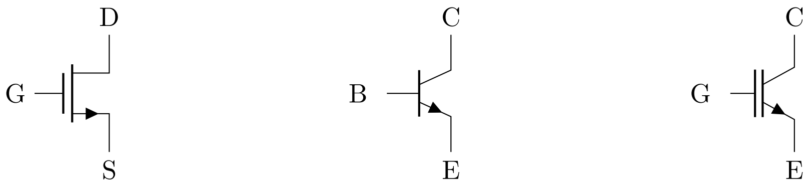
Circuit Description

3.1 UHV Power Switches

The UHV power switches are the element of the circuit that blocks or allows feeding power to the load. Their design is crucial to the ASIC because most of the occupied die area, and the total on-state power dissipation of the IC is determined by these switches.

The first decision is to select the device type.

The XDM10 technology offers three different types of transistors capable of switching up to 230 V rms: MOSFET, BJT and IGBT, as shown in Figure 3.1.



(a) MOSFET (b) BJT (c) IGBT

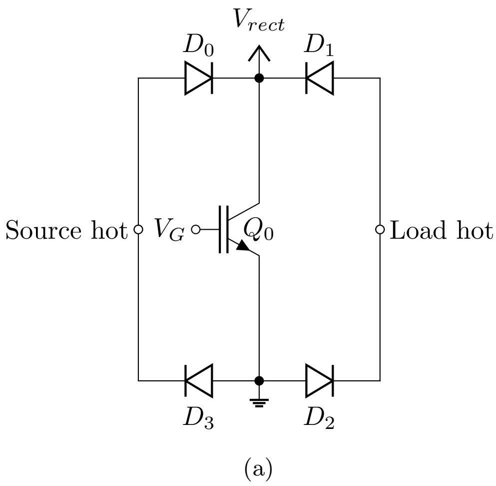
Figure 3.1: Switching device options offered by the working technology.

After careful study of the manufacturer's process specifications shown in Tables 2.4, 2.5, 2.6, ni34b IGBTs were chosen because they provide the largest current per unit of area. SPICE simulations for all corner models are included in Section 4.1.

The next step was choosing the connection configuration to the AC power source. Two options were considered as shown in Figure 3.2 on the next page.

The first one, consists of a diode bridge rectifier with a single transistor connected between the rectified terminals as described in [17]. When Q_0 is in conduction state, current will flow between *Source hot* and *Load hot* and the voltage between V_{rect} and *Gnd* will be near zero, as illustrated in Figure 3.3a on page 22. When Q_0 is in cut-off state, there will be no current flow between *Source hot* and *Load hot* and the voltage between V_{rect} and *Gnd* will be a rectified version of the AC power source.

The second option, shown in Figure 3.2b on the next page, consists of two series transistors, each in anti-parallel with a diode as described in [18]. When V_G is higher than the ground reference, one of Q_0 or Q_1 enter conduction state, and the diode in parallel to the other transistor



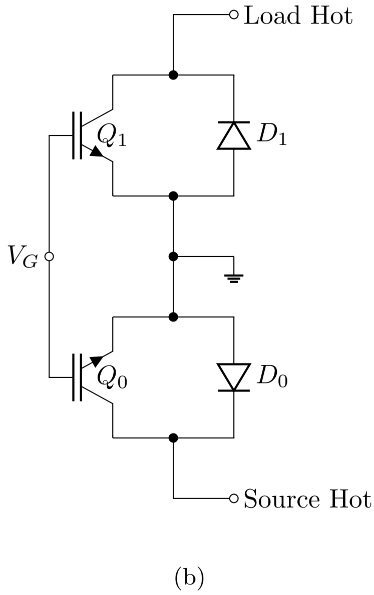


Figure 3.2: Switches block architecture options.

enters conduction state to close the circuit, as illustrated in Figure 3.3b on the following page. When the value of V_G is low with respect to ground, Q_0 and Q_1 will not enter conduction state, and there will be no current flow between *Source hot* and *Load hot*.

The main advantage of the first option over the second on is the existence of two circuit nodes V_{rect} and Gnd so at all times it can be assumed that $V_{rect} \geq Gnd$.

The main advantage of the second option over the second one is a lower on-state power consumption, since the current path includes a transistor and only one diode instead of two.

When considering the total silicon area, it is worth noting that the first option requires one UHV transistor against two, but four UHV diodes instead of two. For the target technology, it was found that UHV diodes occupy about twice the area than UHV IGBTs at the same current.

Finally, the option shown in Figure 3.2a was chosen because its V_{rect} and Gnd terminals simplify the design of the DC voltage sources to power the remaining ASIC's blocks.

Because Q_0 is a UHV IGBT, there are not many degrees of freedom for the designer, particularly width and length are fixed. The I–V curve for the base ni34b IGBT is presented in Figure 3.4 on page 23.

Heat dissipation of a base IGBT as a function of the power delivered to an AC load can be calculated from the I–V curve in Figure 3.4, as shown in Figure 3.5 on page 24. This is of interest, because both heat dissipation and power delivery to the load are specifications defined in Table 1.1 on page 15.

On-state heat dissipation for a given load can be reduced by connecting multiple unit IGBT devices in parallel. With the available silicon area in the MPW, it was determined that the largest possible multiplicity was $M = 3$.

Current density limitations established by the manufacturer were such that it was not possible to integrate the diodes D_{0-3} from Figures 3.2, and 3.3 on the following page into the MPW thus they will be later connected outside (discrete components).

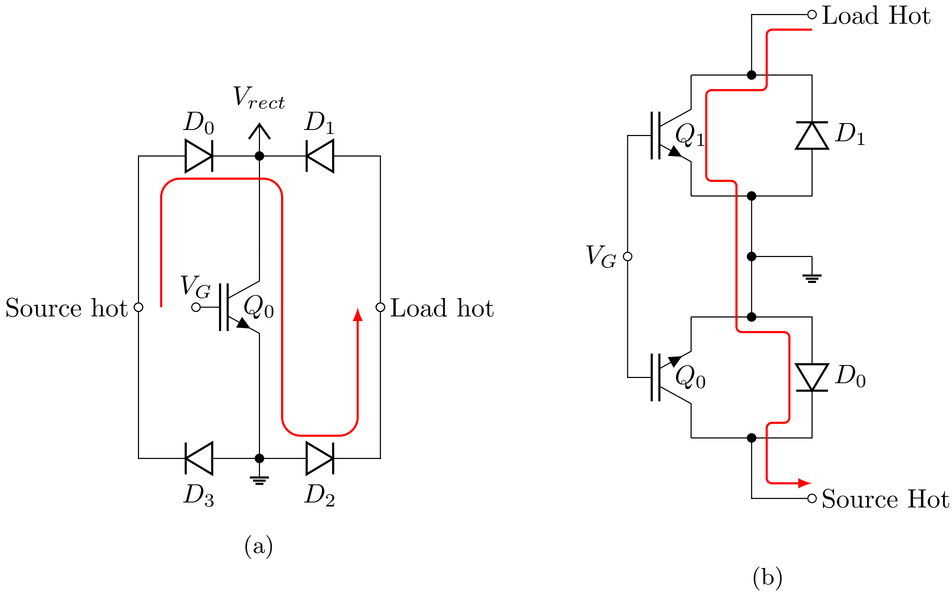


Figure 3.3: Current flow diagram (represented with red) on the switches block architecture options in Figure 3.2.

It was originally planned to include at least one UHV diode in the ASIC for characterization, as [15] is not consistent about the reason behind the current limitations. However, no UHV diodes could be included in the final ASIC because of silicon area constraints.

From now on, the switches block will be represented with the symbol in Figure 3.6 on page 24.

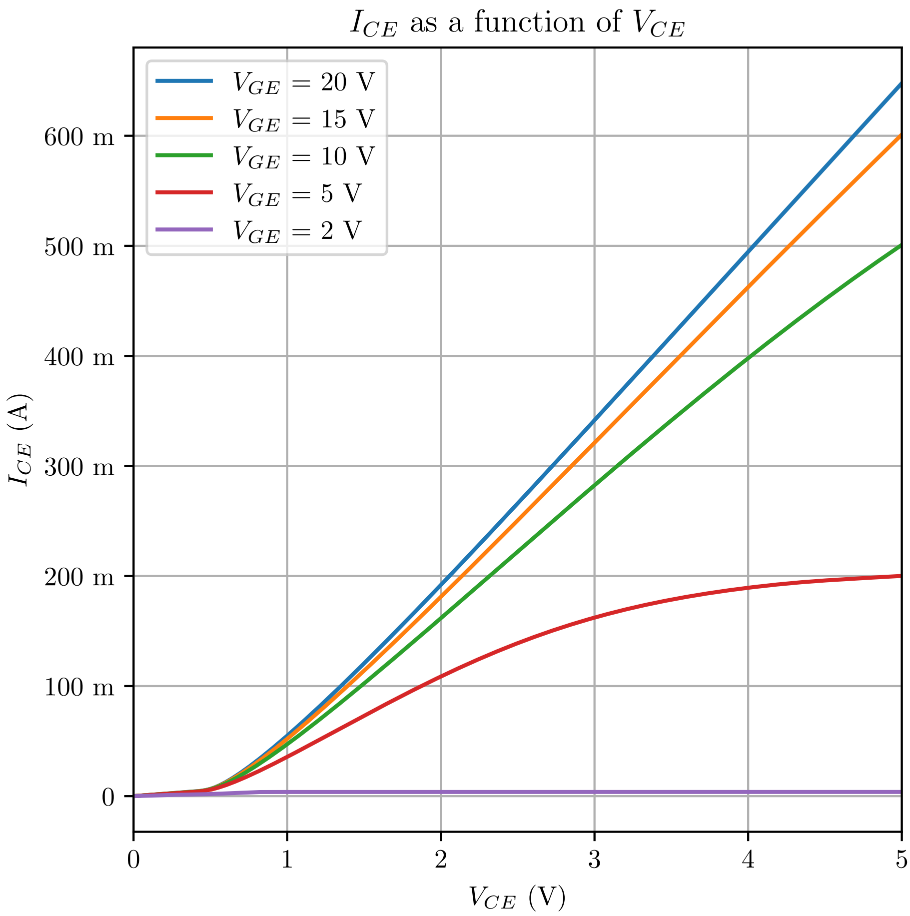


Figure 3.4: I–V curve for the unit IGBT included in XDM10.

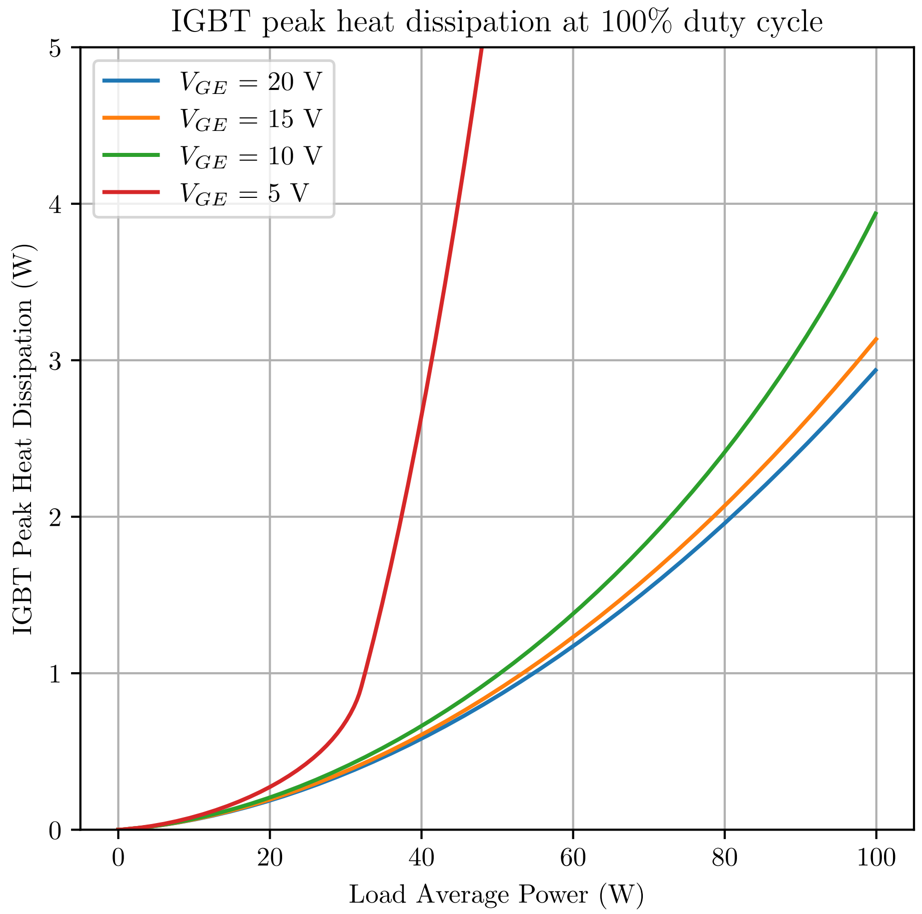


Figure 3.5: Peak heat dissipation for a unit IGBT device at 100 % duty cycle as a function of the power delivered to an AC load.

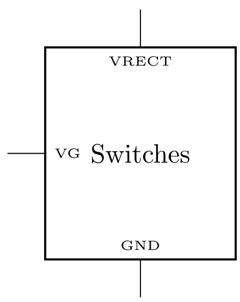


Figure 3.6: Symbol representing the Switches block. This block does not include diodes D_{0-3} which, for the moment, could not be integrated into the ASIC.

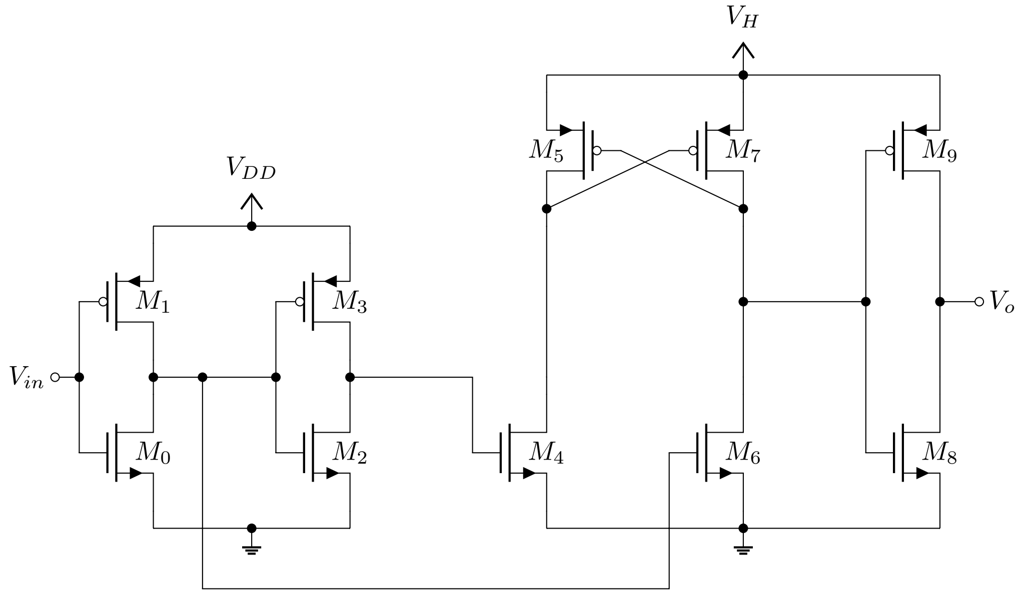


Figure 3.7: Schematic of a Gate Driver Level Shifter [21]. M_{0-3} are low voltage MOS transistors and M_{4-9} are high voltage MOS transistors. The bulk terminal of all MOS transistors is connected to the respective source.

3.2 Gate Driver

Controlling the gate of an IGBT like Q_0 from Figure 3.2a is not a trivial process. A low on-state gate voltage produces low channel conductivity, thus limiting the power delivery to the load. However, higher on-state gate voltages are harder to produce by the Power Management System, with diminishing conductivity returns.

In addition, the gate driver needs to be designed to be able to drive a large capacitive load of up to hundreds of pF like the gate of a UHV IGBT [19, 20].

An on state gate voltage level of 15 V was chosen as a compromise between the 5 V used for logic and 20 V, which is the maximum value supported by the technology. Figures 3.4 on page 23 and 3.5 on the previous page show that the difference between 15 V and 20 V is not significant for power delivery purposes.

The circuit implemented to operate as a gate driver consists of a blind range level shifter as described in [21], and is shown in Figure 3.7.

According to [21],

$$\frac{W_5/L_5}{W_4/L_4} = \frac{\mu_n}{2\mu_p} \frac{(V_{DD} - V_{TN})^2}{(V_H - V_{TP})V_{TP}} \tag{3.1}$$

Where W_i, L_i are the width and length respectively of the i-th transistor, μ_n and μ_p are the electron and hole mobilities, V_{DD} is the lower side supply voltage, V_H is the higher side supply voltage, and V_{TN} and V_{TP} are the threshold voltages for N and P high voltage MOS transistors respectively.

V_{DD} and V_H have been determined by design to be 5 V and 15 V respectively, and sensible approximations for V_{TN} and V_{TP} can be found in the manufacturer's data sheet. However, it is not trivial to determine μ_n and μ_p from the manufacturer provided documentation for HV transistors, and thus the relation between them was determined with aid of SPICE simulations.

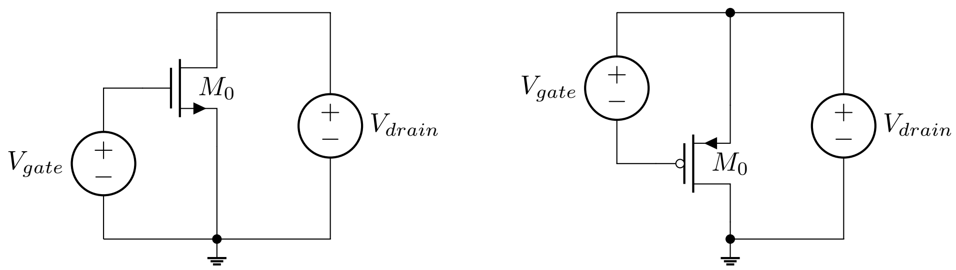
The relation between μ_n and μ_p can be determined by dividing the classic MOSFET drain source saturation current expression [22] as shown in Equations 3.2, 3.3.

$$I_{DSat} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_{th})^2 \tag{3.2}$$

$$\frac{\mu_n}{\mu_p} = \frac{I_{DSatN}}{I_{DSatP}} \frac{\frac{W_P}{L_P}}{\frac{W_N}{L_N}} \frac{(V_{GSP} - V_{thP})^2}{(V_{GSN} - V_{thN})^2} \tag{3.3}$$

Where I_{DSat} is the drain source saturation current, and C_{ox} is the gate oxide capacitance per area unit, which is equal for NMOS and PMOS transistors in the technology used.

With the circuit shown in Figure 3.8 and the transistor sizes in Table 3.1, I_{DSat} was determined by fixing V_{gate} and sweeping V_{drain} for an NMOS and a PMOS transistor.



(a) NMOS (b) PMOS

Figure 3.8: Test bench used to determine the transfer curve for HV (20 V) MOS devices. In all cases, bulk is connected to source.

	NMOS	PMOS	Unit
W	10.0	10.0	µm
L	3.0	4.5	µm
V_{th}	745	590	mV
V_{GS}	5.0	5.0	V

Table 3.1: MOS transfer SPICE simulation input data

Simulation results are shown in Table 3.2 and in Figure 3.9 on the following page.

	NMOS	PMOS	Unit
I_{DSat}	1.23	0.477	mA

Table 3.2: MOS transfer SPICE simulation results for the test bench shown in Figure 3.8.

By substituting the saturation current results into Equations 3.2 and 3.3, the size relations can be calculated as shown in Table 3.3 on page 28.

Finally, MOS transistors were given sizes. Low voltage MOS were given minimum size, and high voltage sizes were first calculated and later adjusted using SPICE simulations.

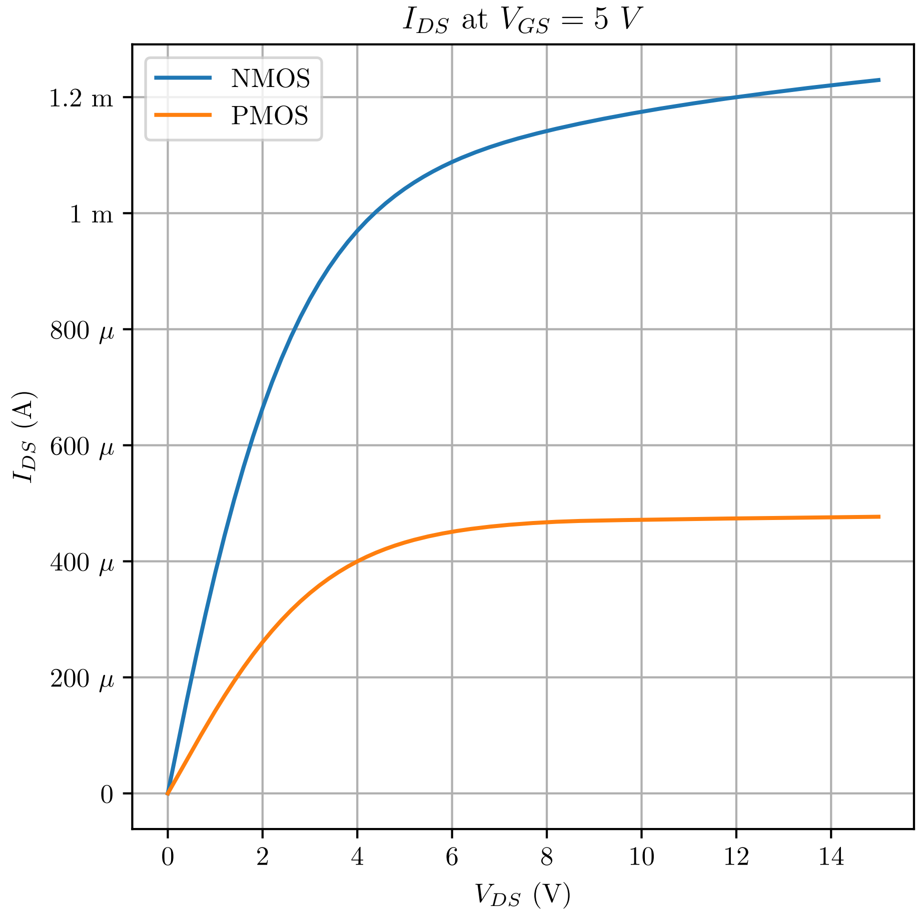


Figure 3.9: SPICE simulation results for the transfer curve of two HV (20 V) MOS devices with the sizes from Table 3.1 on the preceding page.

The final results are presented in Table 3.4 on the following page.

From now on, the gate driver block will be represented with the symbol in Figure 3.10 on the next page.

	Value
μ_n/μ_p	1.85
$\frac{W_5/L_5}{W_4/L_4}$	1.53

Table 3.3: Size relation for the Gate Driver MOS transistors according to Equations 3.2 and 3.3 with the results from the simulations shown in Table 3.2.

	max V (V)	Device Type	W (µm)	L (µm)
M_0	5	NMOS	10.0	1.2
M_1	5	PMOS	10.0	1.3
M_2	5	NMOS	10.0	1.2
M_3	5	PMOS	10.0	1.3
M_4	15	NMOS	10.0	3.0
M_5	15	PMOS	20.0	4.5
M_6	15	NMOS	10.0	3.0
M_7	15	PMOS	20.0	4.5
M_8	15	NMOS	10.0	3.0
M_9	15	PMOS	20.0	4.5

Table 3.4: Device dimensions for transistors in the Level Shifter shown in Figure 3.7 on page 25

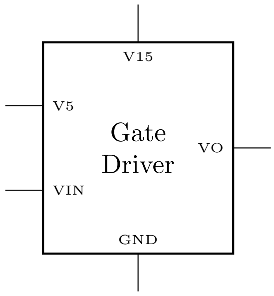


Figure 3.10: Symbol representing the Gate Driver block shown in Figure 3.7 on page 25.

3.3 Power Management

One of the biggest challenges in the design of the ASIC is to provide a reliable DC source to power the rest of the circuits from the AC grid.

The proposed dimmer in Figure 3.11 is a two-terminal device. Thus the dimmer will see the complete rectified AC sine wave when the switch is open, but voltage will fall to almost zero while power is being delivered to the load. This behaviour is illustrated in Figures 3.12 and 3.13 respectively.

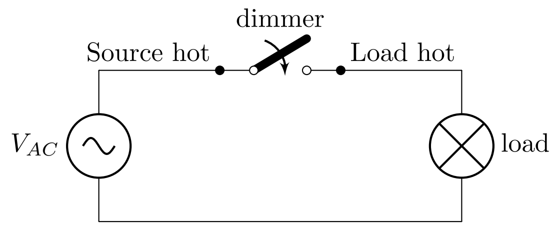


Figure 3.11: Application diagram of a phase cut dimmer

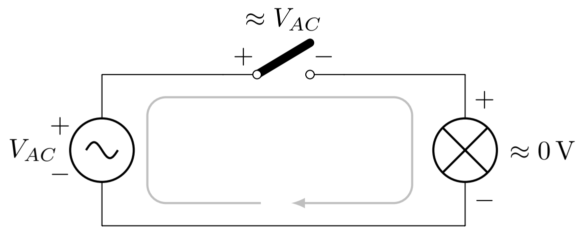


Figure 3.12: Two terminal phase cut dimmer in open state.

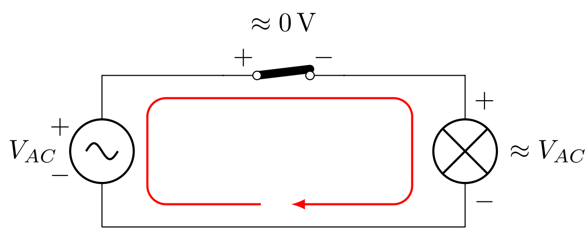


Figure 3.13: Two terminal phase cut dimmer in closed state.

However, the dimmer itself requires to power its internal circuits, and this power cannot be obtained when a near zero voltage is applied to its terminals. Thus a two-terminal dimmer cannot operate at 100 % duty cycle. A solution to this challenge is described in Section 3.3.1.

3.3.1 Maximum Duty Cycle

The amount of the energy per AC cycle that is actually delivered to the load as a function of the dimmer duty cycle can be studied by computing the quotient between the energy reaching the load when the dimmer is present and when the load is connected directly to the AC. This is shown in Eq. 3.4.

$$k = \frac{P_L}{P_{\max}} \tag{3.4}$$

Where k is the portion of the energy reaching the load, P_L is the average power reaching the load over an AC power cycle, and $P_{\max}$ is the average power that would reach the load over an AC power cycle if the load was connected directly to the AC.

$P_{\max}$ can be computed as the average value of the instant power transmitted to the load, as shown in Eq. 3.5. This is a well known equation and its result could be presented without further elaboration (see Eq 3.8). However, it is worth looking into the solution as it will make the process clearer to compute P_L.

$$P_{\max} = \frac{1}{T}\int_0^T \frac{v^2(t)}{R_L}\,\mathrm{d}t \tag{3.5}$$

Where T is the AC signal period, R_L is the effective load resistance and $v(t)$ is the AC voltage sine wave.

By substituting $v(t)$ by its explicit sine wave form from Eq. 3.6, it is possible to calculate the integral.

$$v(t) = \sqrt{2}\, V_{eff} \sin\left(\frac{2\pi}{T}t\right) \tag{3.6}$$

Where V_{eff} is the effective (rms) value for $v(t)$.

$$\begin{aligned} P_{\max} &= \frac{1}{T}\int_0^T \frac{v^2(t)}{R_L}\,\mathrm{d}t \\ &= \frac{1}{T}\int_0^T \frac{2\, V_{eff}^2\ \sin^2\left(\frac{2\pi}{T}t\right)}{R_L}\,\mathrm{d}t \\ &= \frac{2\, V_{eff}^2}{T\cdot R_L}\int_0^T \sin^2\left(\frac{2\pi}{T}t\right)\,\mathrm{d}t \end{aligned}$$

Making use of the trigonometric identity shown in Eq. 3.7 this equation can be further simplified.

$$\sin^2(x) = \frac{1-\cos(2x)}{2} \tag{3.7}$$

$$P_{\max} = \frac{2\, V_{eff}^2}{T\cdot R_L}\int_0^T \frac{1}{2} - \frac{1}{2}\cos\left(\frac{4\pi}{T}t\right)\,\mathrm{d}t$$

Because the terms of the integral are a constant value and a pure sinusoid over a multiple of its period, the result of the integral can be trivially solved to get the result shown in Eq. 3.8.

$$P_{\max} = \frac{2\, V_{eff}^2}{T\cdot R_L}\cdot\frac{T}{2}$$

$$P_{\max} = \frac{V_{eff}^2}{R_L} \tag{3.8}$$

For a trailing edge dimmer, P_L can be modelled as shown in Figure 3.14 with the same voltage sine wave from Eq. 3.5 on the previous page multiplied by a periodic step function $u(t)$ as shown in Eq. 3.10.

$$P_L = \frac{1}{T} \int_0^T \frac{v^2(t)\ u^2(t)}{R_L}\,\mathrm{d}t \tag{3.9}$$

$$u(t) = \begin{cases} 1 & if\ 0 < t + k \cdot \frac{T}{2} < D \cdot \frac{T}{2} \\ 0 & if\ D \cdot \frac{T}{2} < t + k \cdot \frac{T}{2} < \frac{T}{2} \\ k \in \mathbb{Z} \end{cases} \tag{3.10}$$

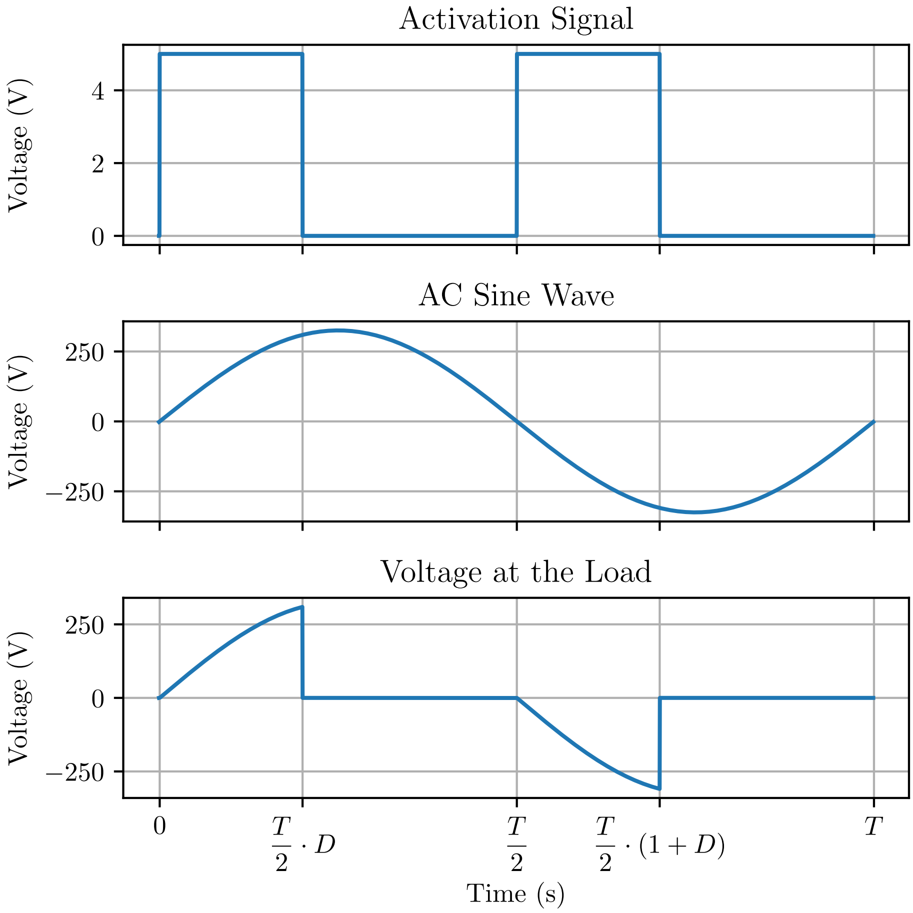


Figure 3.14: Chopped sine wave signal example, as seen by the load in a phase-cut dimmer.

Where D is the operating Duty Cycle for the dimmer.
By substituting Eq. 3.10 in Eq. 3.9 it is possible to obtain the following equation:

$$P_L = \frac{1}{T} \left(\int_0^{\frac{T}{2} \cdot D} \frac{v^2(t)}{R_L}\,\mathrm{d}t + \int_{\frac{T}{2}}^{\frac{T}{2} \cdot (1+D)} \frac{v^2(t)}{R_L}\,\mathrm{d}t \right)$$

With a symmetry argument for the sine function, it can be said that both integrals will give the same result, thus giving the following equation:

$$P_L = \frac{2}{T} \int_0^{\frac{T}{2} \cdot D} \frac{v^2(t)}{R_L} \, \mathrm{d}t$$

By substituting Eq. 3.6 on page 30 and Eq. 3.7 on page 30 the integral can be computed.

$$\begin{aligned} P_L &= \frac{2}{T} \int_0^{\frac{T}{2} \cdot D} \frac{2 \, V_{eff}^2 \, \sin^2\left(\frac{2\pi}{T} t\right)}{R_L} \, \mathrm{d}t \\ &= \frac{4 \, V_{eff}^2}{T \cdot R_L} \int_0^{\frac{T}{2} \cdot D} \sin^2\left(\frac{2\pi}{T} t\right) \, \mathrm{d}t \\ &= \frac{V_{eff}^2}{R_L} \left(D - \frac{1}{2\pi} \sin(2\pi D)\right) \end{aligned}$$

The final expression for the power reaching the load is shown in Eq. 3.11.

$$P_L = \frac{V_{eff}^2}{R_L} \left(D - \frac{\sin(2\pi D)}{2\pi}\right) \tag{3.11}$$

Because of the symmetry inherent to the sine function, the computation for a leading edge dimmer is analogous and provides the exact same result.

Finally, by substituting Eq. 3.8 on page 30 and Eq. 3.11 into Eq. 3.4 on page 30 the result for the power portion reaching the load is given in Eq. 3.12 and plotted in Figure 3.15 on the following page.

$$k = \frac{\frac{V_{eff}^2}{R_L}\left(D - \frac{\sin(2\pi D)}{2\pi}\right)}{\frac{V_{eff}^2}{R_L}}$$

$$k = D - \frac{\sin(2\pi D)}{2\pi} \tag{3.12}$$

Based on Eq. 3.12, a maximum duty cycle was arbitrarily chosen as shown in Table 3.5 to optimize power reaching the load.

	Value	Unit
D	80	%
k	95	%

Table 3.5: Maximum design duty cycle and power percentage reaching the load.

3.3.2 Circuit Implementation

As mentioned in Section 3.1 on page 20 and Section 3.3 on page 29, the Power Management System provides two DC levels from a rectified and potentially chopped voltage sine wave (Figure 3.14 on the previous page).

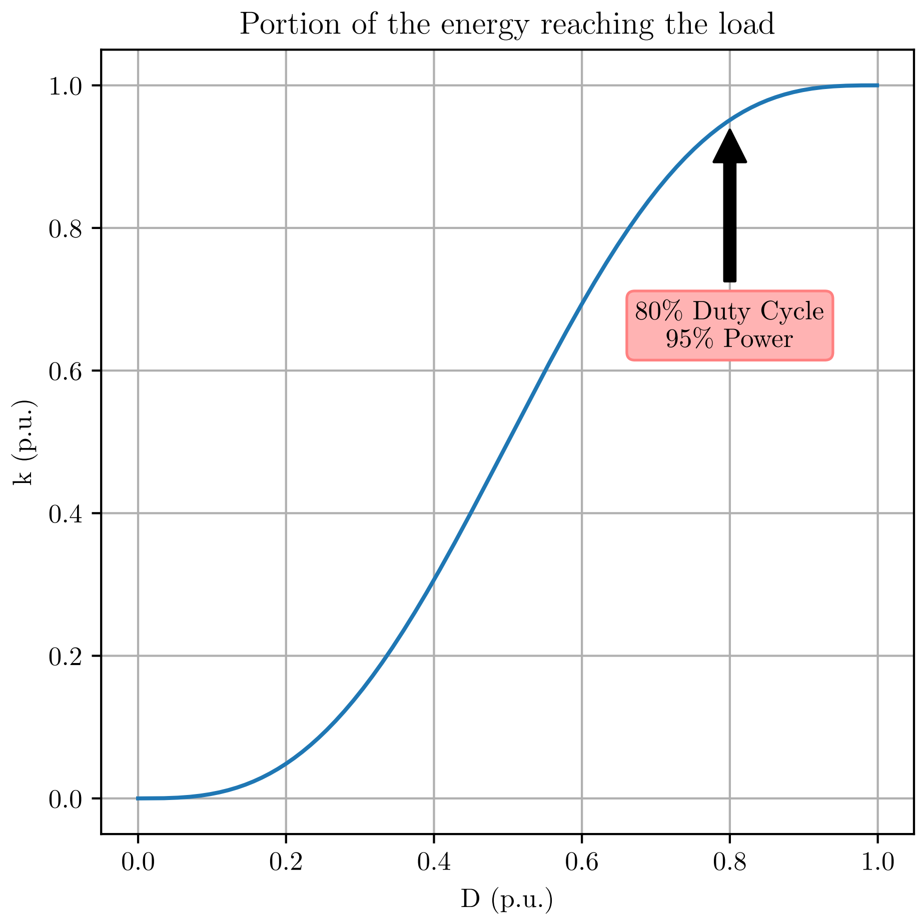


Figure 3.15: Portion of the energy reaching the load plotted against the dimmer duty cycle.

The DC voltages are obtained by harvesting charge from the load, and storing it in tank capacitors. The system must also be able to keep its DC voltages stable when working at a maximum dimmer duty cycle of 80 %, as specified in Table 3.5 on the preceding page, and draw in as little current as possible when the dimmer is not in use.

For this reason, two modes were designed for the Power Management System. The Low Power Mode is meant for idle state, and its main objective is drawing in as little current as possible while keeping its internal voltage sources. The High Power Mode is meant for quick charging of the internal voltage source capacitors, and for use when the ASIC is running at full capacity and maximum duty cycle.

A first approach with most functional components is shown in Figure 3.16 on the next page.

The lower part of the circuit consists of a series of 5 V Zener diodes D_{0-2} which will provide 5 V and 15 V when current flows through them. The excess current not required to excite the Zener diodes will be held by the tank capacitors C_0 and C_1 to be used by the other ASIC blocks.

Diode D_3 prevents the capacitor C_1 from leaking its charge into D_{0-2} and C_0, and diode D_4 prevents charge leaking from C_0 when the dimmer is on and V_{rect} is at a near zero value.

The upper part of the circuit implements the two operation modes, and can provide a low or

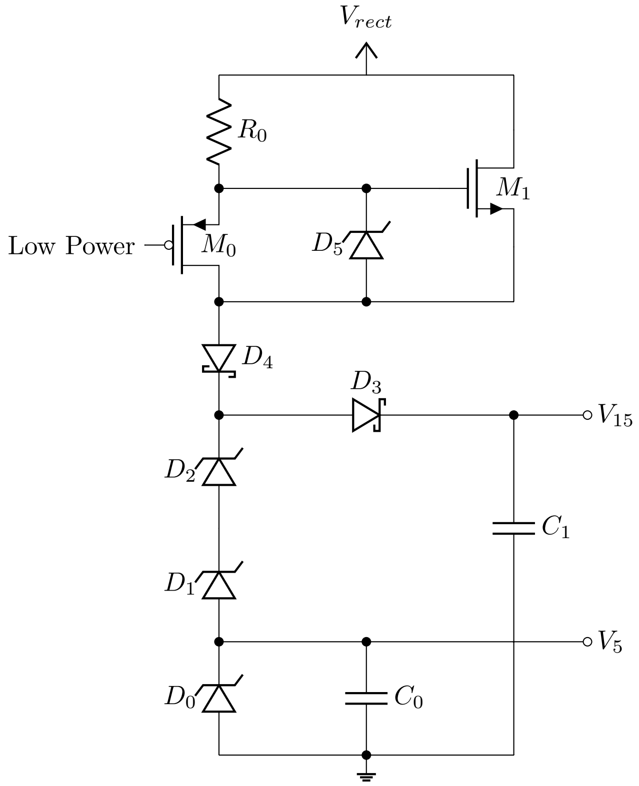


Figure 3.16: Simplified implementation for the Power Management System delivering 5 V and 15 V from a potentially chopped voltage sine wave. D_0, D_1, D_2 and D_5 are 5 V Zener diodes, D_3 and D_4 are Schottky diodes, M_0 is an HV (20 V) PMOS transistor and M_1 is an UHV NMOS transistor. All MOS transistors have their bulk connected to their sources, that are not included in the figure for the sake of simplicity

high resistance path for current from V_{rect} depending on the input signal *Low Power*.

Low power mode can be controlled from outside the ASIC with a 0 V to 5 V signal, which is adapted to the 0 V to 20 V range inside the ASIC with a pull up circuit.

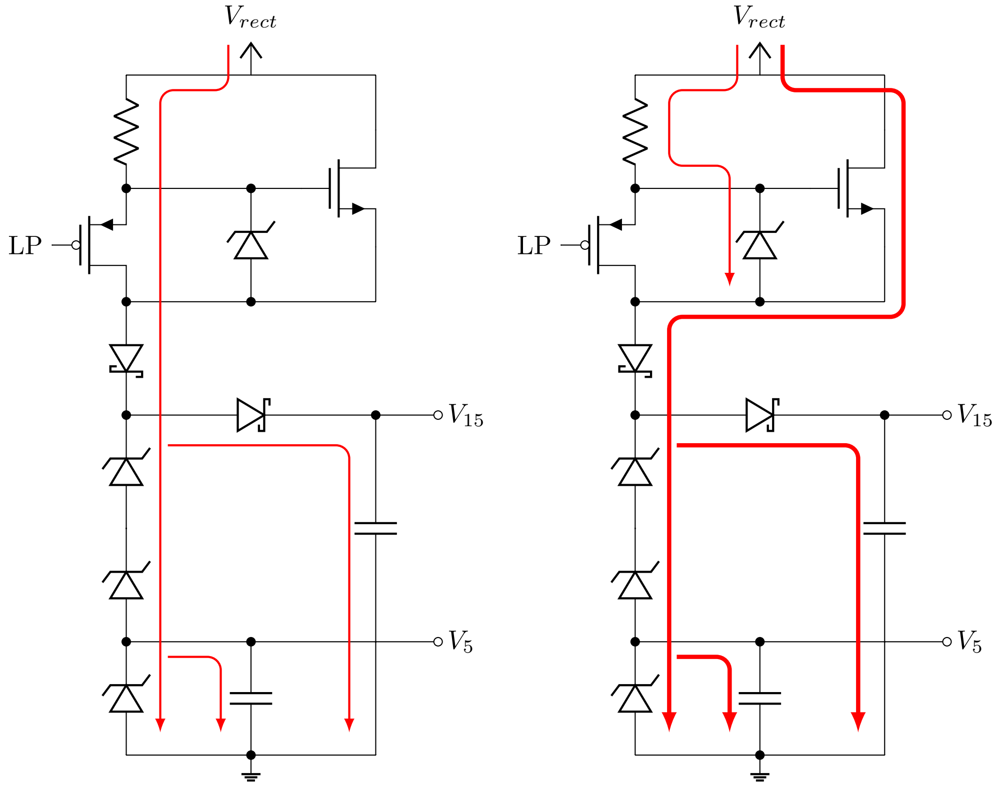
When *Low Power* is in low state, M_0 acts like a closed switch, causing the V_{GS} of transistor M_1 to be near zero, thus acting like an open switch. All current delivered to C_0 and C_1 is limited by a high value integrated poly resistor R_0. The current path can be observed in Figure 3.17a on the following page.

When *Low Power* is in high state, M_0 acts like an open switch, causing R_0 current to go through D_5 which will impose 5 V V_{GS} on transistor M_1 allowing for a larger current to reach C_0 and C_1. This current path can be observed in Figure 3.17b on the next page.

A MOS device M_1 was chosen over a low value resistor or other linear components because when operating in saturation mode it can provide a flat current transfer, allowing the circuit to draw in significant current when V_{rect} is near zero, and not excessive current at the peak.

Resistor R_0 can be sized by considering the current needed by the ASIC in idle state.

The 5 V source will have to power the logic for the ASIC, which is represented by a low power microcontroller and can be in the order of a few µA [12]. The 15 V DC source only powers the Gate Driver circuit from section 3.2 on page 25, which has negligible static current consumption,



(a) Low Power Mode. (b) High Power Mode.

Figure 3.17: Current path for the Power Management System in different power modes.

and thus can safely be ignored for this analysis.

Because of technology limitations, it was not possible to implement the Power Management System *as is*, and some new devices were introduced as depicted in Figures 3.18 on the next page and 3.19 on page 37.

The first problem found in the implementation was that transistor M_1 has fixed dimensions given by the technology, which causes it to draw excessive current ($\approx 35\,\mathrm{mA}$) when a V_{GS} of 5 V is applied. To compensate for this, a 20 V HV NMOS transistor M_2 was included as a source degeneration element [23]. A final issue arises with M_2 when Low Power Mode is activated, no current flows through M_{1-2} and large values of V_{SD} can be applied. For this reason, a 5 V Zener diode D_6 was added in parallel with M_2 to control its V_{SD} range.

The pull up network for controlling Low Power Mode was also included at this stage. It consists of two 20 V HV MOS transistors M_3 and M_4 which act as pull up logic. To ensure that M_4 is able to drive M_0, M_4 was given a far larger multiplicity. This solution was chosen over other more complex alternatives for its simplicity and robustness given the importance of the Power Management System in the ASIC as a whole.

Another significant change is the replacement of Zener diodes D_{0-2} with the block U_0 in Figure 3.20 on page 38. The reason for this change is the 1 mA maximum current specification for Zener diodes provided by the manufacturer. If their multiplicity is low, the Zener's current

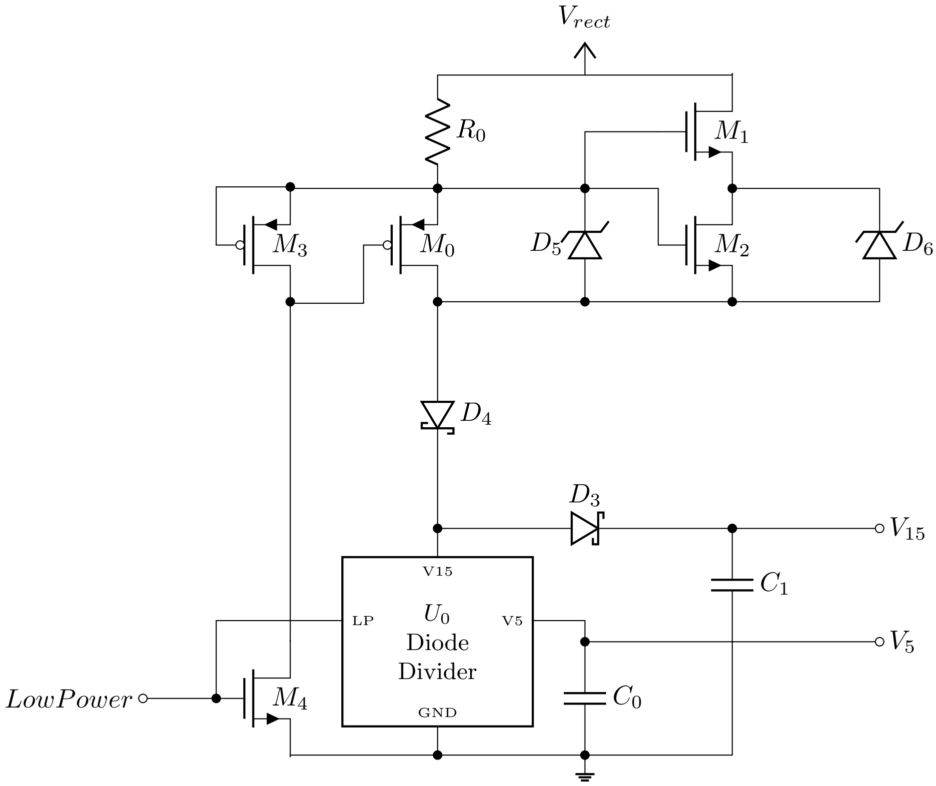


Figure 3.18: Power System that delivers 5 V and 15 V from a potentially chopped voltage sine wave. D_5 and D_6 are 5 V Zener diodes, D_3 and D_4 are Schottky diodes, M_0 and M_3 are HV (20 V) PMOS transistors, M_2 and M_4 are HV (20 V) NMOS transistors, M_1 is a UHV NMOS transistor, and U_0 is the voltage Diode Divider shown in Figure 3.19 on the following page. All MOS transistors have their bulk connected to their sources, that are not included in the figure for the sake of simplicity

when in High Power Mode (up to 14 mA) is too large. If their multiplicity is high, the current in Low Power Mode (≈ 200 µA peak) is not enough to reach their nominal voltage. Thus, a circuit that connects and disconnects Zener diodes according to the operation mode was designed, and is presented in Figure 3.19 on the following page. This block is represented with the symbol in Figure 3.20 on page 38.

The diode divider consists of three sub blocks, the first one consists of transistors M_{0-3} and is the series of two MOS inverters. Its main objective is to avoid loading the input named *LP* with a larger gate.

The second sub block consists of transistors M_{4-7}, implementing a simple level shifter to translate the input named *LP* from the 0 V to 5 V range to the 0 V to 15 V range. This sub block is like the simple level shifter implemented by M_3, M_4 in the Power Management System shown in Figure 3.18. Likewise, M_5 was given a far larger W/L than M_7 to ensure its driving capabilities.

The third sub block is the most interesting part of the diode divider. When the input named *LP* is in high state (meaning the ASIC is in low power mode), transistors M_8 and M_9 will be in open state. This means that the current will flow from the V_{15} terminal to *Gnd* through the

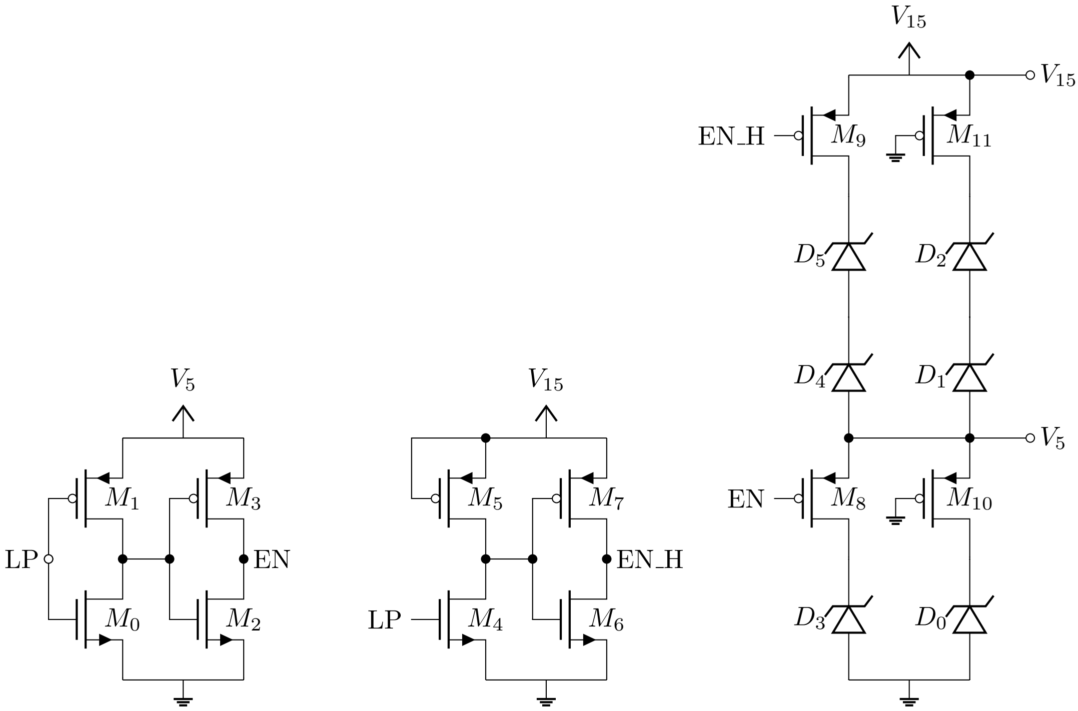


Figure 3.19: Diode voltage divider circuit that delivers 5 V and 15 V from a potentially chopped voltage sine wave. D_{0-5} are 5 V Zener diodes, M_0 and M_2 are LV NMOS transistors, M_1, M_3, M_8 and M_{10} are LV PMOS transistors, M_4 and M_6 are HV (20 V) NMOS transistors, M_5, M_7, M_9 and M_{11} are HV (20 V) NMOS transistors, All MOS transistors have their bulk connected to their sources, that are not included in the figure for the sake of simplicity

D_{0-2} diodes, which have low multiplicity, and (V_5, V_{15}) will be able to reach their desired voltage with a low current. When the input named *LP* is in low state (and the ASIC is in high power mode), transistors M_8 and M_9 will be in closed state. This means that current will flow from the V_{15} terminal to *Gnd* through both the D_{0-2} and D_{3-6} diodes. Because diodes D_{3-6} have high multiplicity, the larger currents drawn from the normal mode will not be out of the nominal values of any Zener diode. Transistors M_{10} and M_{11} are fixed in closed state, added for the sake of symmetry.

From now on, the Power Management System block will be represented with the symbol in Figure 3.21 on the next page.

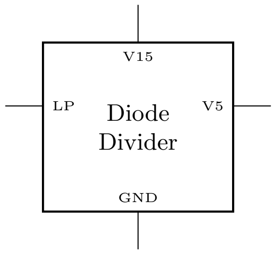


Figure 3.20: Symbol representation for the Diode Divider block shown in Figure 3.19 on the preceding page.

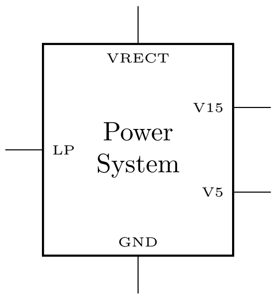


Figure 3.21: Symbol representation for the Power System block shown in Figure 3.18 on page 36.

3.3.3 Sizing

Prior to device sizing, it is necessary to estimate the current consumption in low and high power modes. Low power mode must power a modern low power microcontroller in idle state, which can be in the order of 45 µA with a clock of 1 MHz [12]. With this information, a nominal current of 200 µA was chosen for this application to provide a safety margin.

When operating in low power mode, the main current limiting element is the resistor R_0. By examining the full implementation of the Power Management System from Figure 3.18 on page 36, it is possible to notice that one of its terminals is fixed at 15 V and the other one varies according to a rectified voltage sine wave with amplitude $\sqrt{2} \times 230\,\text{V} \approx 325\,\text{V}$. Given that 15 V is considerably smaller than 325 V, a reasonable approximation for the average current consumption can be obtained by assuming that all of V_{rect} is applied directly to R_0.

If I_{avg} is the average power management system's current, T is the AC signal period, and V_{eff} is the AC signal effective value.

$$I_{avg} = \frac{2}{T}\int_0^{\frac{T}{2}} \frac{V_{rect}}{R_0}\,\mathrm{d}t \tag{3.13}$$

$$I_{avg} = \frac{2}{T}\int_0^{\frac{T}{2}} \frac{\sqrt{2}\cdot V_{eff}\sin(\frac{2\pi}{T}t)}{R_0}\,\mathrm{d}t$$

$$I_{avg} = \frac{2\sqrt{2}\cdot V_{eff}}{T\cdot R_0}\int_0^{\frac{T}{2}} \sin\left(\frac{2\pi}{T}t\right)\,\mathrm{d}t$$

$$I_{avg} = \frac{2\sqrt{2}\cdot V_{eff}}{\pi\cdot R_0} \tag{3.14}$$

A value of $R_0 \approx 1.04\,\text{M}\Omega$ is obtained, by substituting $V_{eff} = 230\,\text{V}$ and $I_{avg} = 200\,\mu\text{A}$ into Eq. 3.14, thus M_0 was given a W/L of 4.5/10 µm so that its saturation current is significantly higher than 200 µA.

Pull up transistor M_3 was given the same W and L as M_0 and a multiplicity $m = 8$ so that it can properly act as a pull up resistor. M_4 was given minimum dimensions ($W/L = 2.5/3.5$ µm).

Next, the high power mode components had to be sized.

A major design constraint is that the system must provide energy to the logic circuits even when working at the maximum duty cycle of 80 % as defined in Table 3.5 on page 32. In other words, the charge harvested at the first 20 % of an AC semi cycle in high power mode should at least be equal to the one harvested in a full cycle in low power mode, as shown in Eq. 3.15.

$$\min(Q_{hp}) \geq \max(Q_{lp}) \tag{3.15}$$

Where Q_{hp} is the charge that can be harvested in high power mode, and Q_{lp} is the charge that can be harvested in low power mode.

The best case scenario for Q_{lp} is when the ASIC never enters conduction state, and its value is given by the average current computed in Eq. 3.14 multiplied by the duration of an AC semi cycle. The worst case scenario for Q_{hp} is when the activation signal duty cycle (D) is at its highest.

The current limiting element for the high power mode is a MOS transistor in saturation mode. Because of this, current consumption can be considered constant, and the total charge can be expressed as the product of its current times a semi cycle period. This is shown in Eq. 3.16 on the next page.

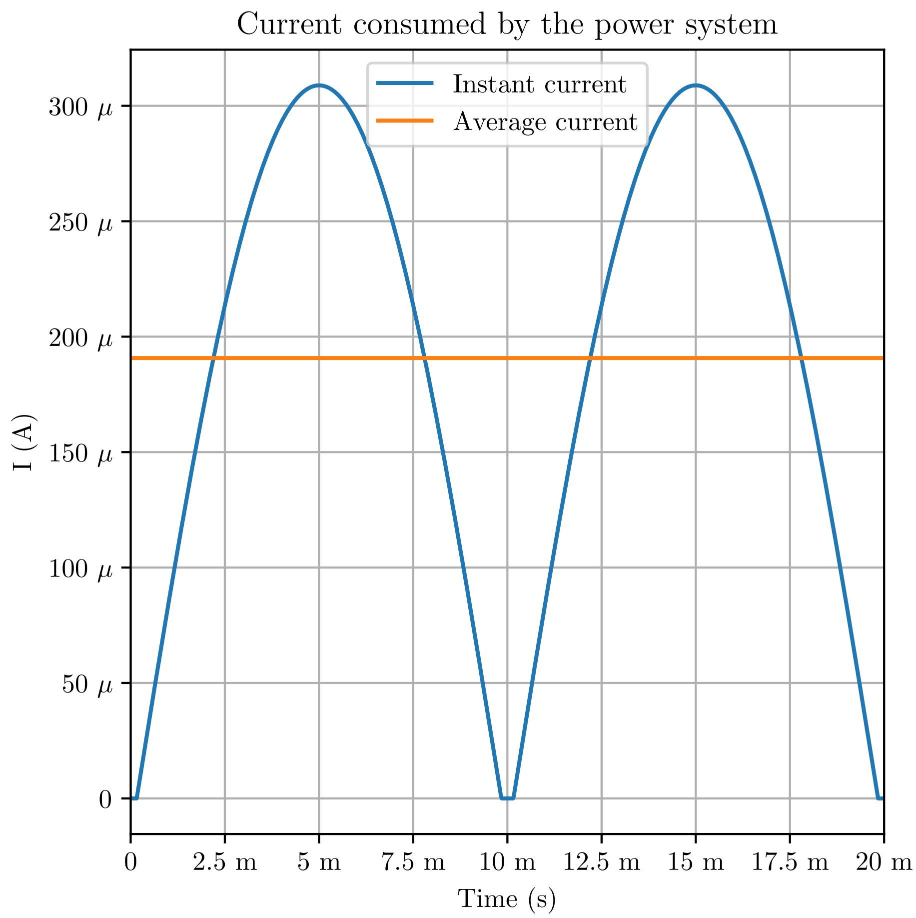


Figure 3.22: Current flow through the power management system in low power mode.

$$(1 - D) \cdot \frac{T}{2} \cdot I_{hp} \geq \frac{T}{2} \cdot I_{avg\_lp}$$

$$(1 - D) \cdot I_{hp} \geq I_{avg\_lp} \tag{3.16}$$

Where I_{hp} is the current drawn in high power mode, I_{avg_lp} is the average current consumed during low power mode defined in 3.14 on the preceding page, D is the activation signal duty cycle and T is the AC signal period.

As pointed in Table 3.5 on page 32, the maximum D value is 0.8, thus a lower bound for I_{hp} can be found by substitution as shown in Eq. 3.17.

$$I_{hp} \geq \frac{I_{avg\_lp}}{1 - D} = \frac{200\,\mu\text{A}}{0.2} = 1\,\text{mA} \tag{3.17}$$

Transistor M_1 was sized to handle this current. However, because M_1 is a UHV transistor, there are not many degrees of freedom for the designer, particularly width and length are fixed, hence its saturation current cannot easily be controlled. Transistor M_2 was then sized for the designed saturation current ($W/L = 16/3.5$ µm).

Diode D_5 was given minimum multiplicity ($m = 1$) since it should only take the same current as the Low Power mode, and diode D_6 was given minimum multiplicity ($m = 1$) because it should conduct current only when (M_1, M_2) are off, thus negligible current flows through. D_3 and D_4 were given dimensions so that they can conduce all current in a worst case scenario ($W/L = 21/2.0$ µm).

Capacitor C_0 is a crucial element for the ASIC, since it holds the charge to power the logic circuitry. A large C_0 is necessary to keep the logic voltage stable. A capacitance value can be found assuming a constant average current of 200 µA will be taken per AC semi cycle, and the worst case will happen when the duty cycle is at its maximum value and C_0 needs to hold the voltage stable for 80 % of a semi cycle, which is 8 ms for a 50 Hz signal. Given a constant current, the voltage fluctuation in a capacitor follows Eq. 3.18.

$$\Delta V = \frac{I \times \Delta t}{C} \tag{3.18}$$

Where ΔV is the voltage fluctuation, I is the applied current, Δt is the time interval, and C is the capacitance.

To improve the supply robustness supporting a wide range of microcontrollers, a worst case steady current of 2 mA and a voltage drop of 5 % were chosen. With this scenario, a capacitance value of ≈100 µF is obtained.

The main design constraint for capacitor C_1 is that it should not incur in a significant voltage drop when connected to the switches from section 3.1 on page 20 through the gate driver from section 3.2 on page 25. This size was determined with aid from SPICE simulations.

The final size/values for all devices from the power system shown in Figure 3.18 on page 36 are presented in Table 3.6.

Name	max V (V)	Device type	Dimension	Value	Unit
M_0	20	PMOS	W/L	10 / 4.5	µm/µm
M_1	350	NMOS	centre pieces	8	–
M_2	20	NMOS	W/L	16 / 3.5	µm/µm
M_3	20	PMOS	W/L	80 / 4.5	µm/µm
M_4	20	NMOS	W/L	2.5 / 3.5	µm/µm
D_3	40	Schottky Diode	W/L	21 / 2.0	µm/µm
D_4	40	Schottky Diode	W/L	21 / 2.0	µm/µm
D_5	5	Zener Diode	m	1	–
D_6	5	Zener Diode	m	1	–
R_0	350	Resistor	R	1.00	MΩ
C_0	5	Capacitor	C	100	µF
C_1	15	Capacitor	C	10	nF

Table 3.6: Device dimensions for the full implementation of the power system shown in Figure 3.18 on page 36

Finally, about the diode voltage divider U_0 in Figure 3.18 on page 36, and 3.19 on page 37.

Transistors M_0, M_1, M_2, M_3 constitute the series of two simple CMOS inverters, with arbitrary small dimensions ($W/L = 10/1.2$ µm for the NMOS and $W/L = 10/1.3$ µm for the PMOS).

Transistors M_4, M_5, M_6, M_7 also constitute MOS inverters ($W/L = 10/3.5$ µm for the NMOS and $W/L = 10/5.5$ µm for the PMOS). The PMOS transistor of the first stage (M_5) is working as a pull up resistor to change the voltage domain from 5 V to 15 V, and was given a multiplicity $m = 2$ to double its effective width and ensure its driving capabilities.

Diodes D_0, D_1, D_3 conduce current during low power mode, and their multiplicity is $m = 1$ so that they all reach their 5 V knee voltage with I_{lp}. Diodes D_3, D_4, D_5 conduce during Normal Mode, and their multiplicity is $m = 14$ so that the largest possible current is within their nominal value.

Transistors M_8 and M_9 give control over the connection of D_3, D_4, D_5, and they were given a large width ($W/L = 22340/1.3$ µm and $W/L = 22340/5.5$ µm respectively) to minimize their voltage drop when large currents flow through the diodes. Transistors M_{10} and M_{11} were included on the low power branch with $W/L = 160/1.3$ µm and $W/L = 160/5.5$ µm respectively, for the purpose of symmetry.

The final dimensions for all devices from the diode voltage divider shown in Figure 3.19 on page 37 are presented in Table 3.7.

Name	max V (V)	Device Type	Dimension	Value	Unit
M_0	5	NMOS	W/L	10 / 1.2	µm/µm
M_1	5	PMOS	W/L	10 / 1.3	µm/µm
M_2	5	NMOS	W/L	10 / 1.2	µm/µm
M_3	5	PMOS	W/L	10 / 1.3	µm/µm
M_4	15	NMOS	W/L	10 / 3.5	µm/µm
M_5	15	PMOS	W/L	20 / 5.5	µm/µm
M_6	15	NMOS	W/L	10 / 3.5	µm/µm
M_7	15	PMOS	W/L	10 / 5.5	µm/µm
M_8	5	PMOS	W/L	2240 / 1.3	µm/µm
M_9	15	PMOS	W/L	2240 / 5.5	µm/µm
M_{10}	5	PMOS	W/L	160 / 1.3	µm/µm
M_{11}	15	PMOS	W/L	160 / 5.5	µm/µm
D_0	5	Zener Diode	m	1	–
D_1	5	Zener Diode	m	1	–
D_2	5	Zener Diode	m	1	–
D_3	5	Zener Diode	m	14	–
D_4	5	Zener Diode	m	14	–
D_5	5	Zener Diode	m	14	–

Table 3.7: Device dimensions for the Power System Diode Divider shown in Figure 3.19 on page 37

All devices in this section could be integrated, with the exception of capacitors (C_0, C_1) because of the (100 µF, 10 nF) needed to hold the charge for up to 8 ms (80 % of a semi-cycle for a 50 Hz signal).

3.4 Zero Crossing Detector

Zero crossing detection is crucial for keeping the dimmer in phase with the 50 Hz to 60 Hz sine wave from the grid. For the designed IC, this is achieved with the circuit shown in Figure 3.23, which is based on [24, 25]

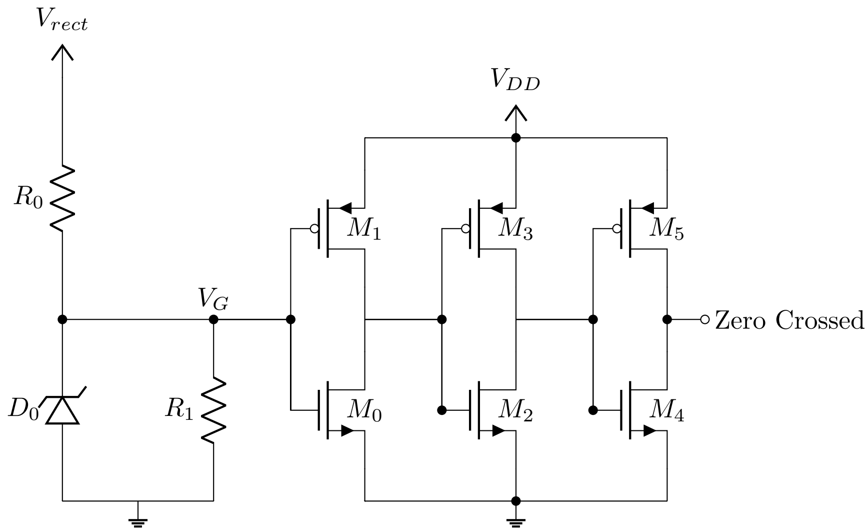


Figure 3.23: Zero Crossing Detector Where D_0 is a 5 V Zener diode, R_0 is a large integrated UHV resistor, R_1 is an integrated LV resistor, M_0, M_2, M_4 are low voltage NMOS transistors, and M_1, M_3, M_5 are low voltage PMOS transistors. MOS transistors have their bulk connected to their source, and a V_{DD} of 5 V is given.

The simplest approach to designing the Zero Crossing Detector is by ignoring resistor R_1. In this case, the value of V_G is trivially determined as 5 V when V_{rect} is greater than 5 V and 0 V otherwise. The following logical inverters then produce an output that is logically complimentary.

However, this approach is not ideal for the target ASIC. That is because V_{rect} is also connected to the Switches block described in Sect. 3.1 on page 20 and the Power Management System described in Sect. 3.3 on page 29.

As it was described in Sect. 3.3 on page 29, the Power System will only take current from V_{rect} when its voltage value is greater than 15 V. If this happens at the same time that the Switches block is in an open state, there will be no other circuit drawing in current from V_{rect} and intrinsic capacitances will not allow for V_{rect} to reach a low enough voltage to be detected by the Zero Crossing Detector.

The inclusion of R_1 remedies this situation by giving a conduction path for discharging parasitic and intrinsic capacitances connected to V_{rect} even for values under 5 V. With this new configuration, V_{rect} can now take arbitrarily small values.

For values of V_{rect} close to zero, V_G will behave as a voltage divider between R_0 and R_1, and diode D_0 will have no effect. Since M_0 and M_1 act as a logical inverter, the value of $Zero\ Crossed$ will be V_{DD}.

As the value of V_{rect} increases, there will be a point at which the value of V_G is larger than the threshold of the (M_0, M_1) inverter and the value of *Zero Crossed* will abruptly go to 0 V.

For very large values of V_{rect}, at which the (R_0, R_1) voltage divider would result in values of V_G larger than V_{DD}, diode D_0 will come into play limiting the V_G voltage to 5 V and preventing damage to $(M_0,\ M_1)$. This behaviour is shown in Eqs. 3.19, 3.20 and Figure 3.24.

$$V_G = \min\left(V_{rect} \cdot \frac{R_1}{R_0 + R_1}, 5\,\mathrm{V}\right) \tag{3.19}$$

$$Zero\ Crossed = \begin{cases} V_{DD} & if\ V_{rect} \cdot \frac{R_1}{R_0+R_1} \leq V_{th} \\ 0 & if\ V_{th} < V_{rect} \cdot \frac{R_1}{R_0+R_1} \end{cases} \tag{3.20}$$

Where V_{th} is the threshold voltage for the (M_0, M_1) inverter.

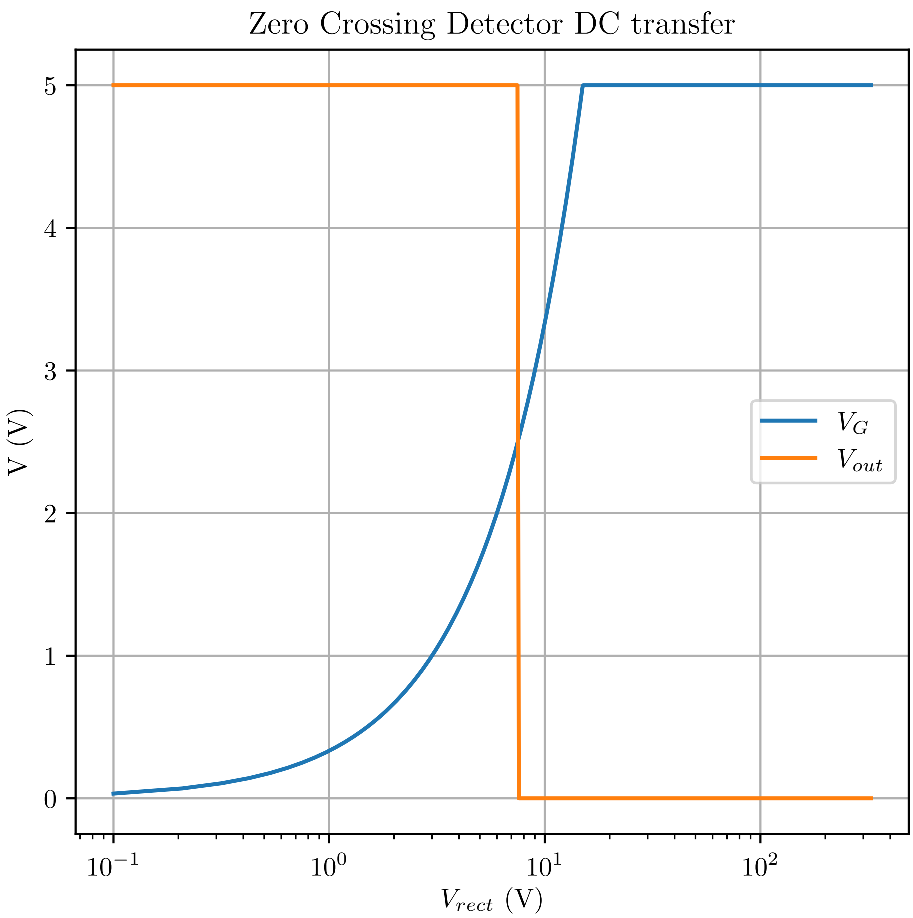


Figure 3.24: Expected DC transfer for the zero crossing detector from Figure 3.23.

From now on, the Zero Crossing Detector block will be represented with the symbol in Figure 3.25 on the next page.

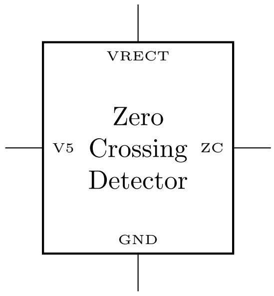


Figure 3.25: Symbol representation for the Zero Crossing Detector block shown in Figure 3.23 on page 43.

3.4.1 Sizing

The first decision that needs to be taken is for the value of resistor R_0, because it will be the current limiting element when V_{rect} has high voltage. Larger values will provide low power consumption, but large silicon areas that could be used by more sensitive blocks like the dimmer main Switches. Smaller values will take less area, but significantly increase power consumption. Finally, a compromise value of $1\,\mathrm{M\Omega}$ ($1026\,\mu\mathrm{m} \times 315\,\mu\mathrm{m}$) was chosen.

The choice of R_0 gives a maximum current consumption, and that information can be used to determine the multiplicity of Zener diode D_0 ($m = 1$).

The choice of R_0 also gives way to the choice of R_1, that will determine the linear range of operation for the Zero Crossing Detector. A value of $500\,\mathrm{k\Omega}$ ($968\,\mu\mathrm{m} \times 172\,\mu\mathrm{m}$) was chosen so that the linear range is active for values of V_{rect} smaller than 15 V, which is when the Power System will begin to draw in current. That way, current consumption from the AC source is optimized.

Transistors M_{0-5} were first given minimal dimensions and then fine tuned with SPICE simulations.

The final dimensions for all devices from the Zero Crossing Detector shown in Figure 3.23 on page 43 are presented in Table 3.8.

Name	max V (V)	Device Type	Dimension	Value	Unit
M_0	5	NMOS	W/L	6.6 / 3.0	µm/µm
M_1	5	PMOS	W/L	13.2 / 3.0	µm/µm
M_2	5	NMOS	W/L	6.6 / 3.0	µm/µm
M_3	5	PMOS	W/L	13.2 / 3.0	µm/µm
M_4	5	NMOS	W/L	6.6 / 3.0	µm/µm
M_5	5	PMOS	W/L	13.2 / 3.0	µm/µm
D_0	5	Zener Diode	m	1	–
R_0	350	Resistor	R	1	MΩ
R_1	5	Resistor	R	500	kΩ

Table 3.8: Device dimensions for the Zero Crossing Detector shown in Figure 3.23 on page 43.

3.5 Control Logic

To fully implement a dimmer, some control logic is necessary to manage the turning on and off of the switches as described in Section 3.1 on page 20.

The simplest possible control strategy would consist of a leading edge dimmer, which can be implemented to follow the flowchart presented in Figure 3.26 with two digital inputs (*Zero Crossed*, *Delay*) and one digital output *Switch*.

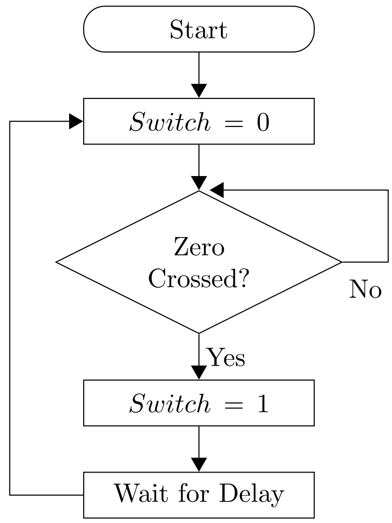


Figure 3.26: Flow chart for the control logic of a leading edge dimmer. *Zero Crossed* is the output of the Zero Crossing Detector circuit described in Section 3.4 on page 43, and *Delay* is a multi-bit digital input to specify the dimmer duty cycle. Digital output *Switches* represents the desired state of V_G of the switches described in Section 3.1 on page 20.

This flowchart could easily be translated into a FSM, the delay being implemented with a standard digital counter.

A trailing edge dimmer can also be implemented with slight modifications to Figure 3.26, as shown in Figure 3.27 on the next page.

However, the design of a trailing edge dimmer presents a more significant challenge for phase detection than a leading edge dimmer. A trailing edge dimmer should be in conduction state right until the AC current zero-cross, but that means that the voltage between the *Load Hot* and *Source Hot* terminals will be almost zero also. Thus the Zero Crossing Detector cannot be relied on for this purpose, and having the dimmer synchronous with the AC signal requires special care.

Another aspect to consider is the effect of a slight error in the duty cycle time constant. In the case of the leading edge dimmer, conduction begins after the AC signal crosses zero (detected with the Zero Crossing Detector) and a stops conducing after a certain delay. If the delay is slightly longer or shorter, the duty cycle would be slightly different, with no other major consequences. Moreover, this error will not accumulate over time, since the trigger for conduction is the zero crossing detection.

In the case of the trailing edge dimmer, conduction will end when the AC signal crosses zero, which presents a more significant challenge to measure from inside a dimmer with only

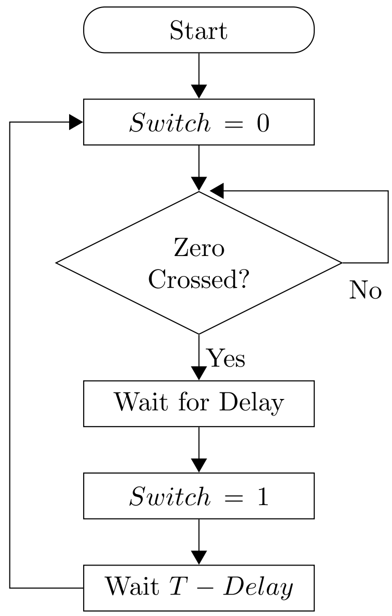


Figure 3.27: Flow chart for the control logic of a trailing edge dimmer. *Zero Crossed* is the output of the Zero Crossing Detector circuit described in Section 3.4 on page 43, *Delay* is a multi-bit digital input to specify the dimmer duty cycle, and T is a multi-bit digital value to specify the duration of one AC semi cycle. Digital output *Switches* represents the desired state of V_G of the switches described in Section 3.1 on page 20.

two terminals. Because the zero crossing detection cannot be used for syncing with the AC signal, a small error in the delay time constants can accumulate over time and cause unexpected behaviour. This drift can be minimized using more complex logic or extra circuitry that exceed the scope of this project.

A secondary logic block is necessary for controlling the low and high power modes. In its simplest version, this can be implemented with a standard digital comparator. If the *Delay* signal (controlling the dimmer duty cycle) is above a fixed threshold, then the dimmer should operate in High Power Mode, else in Low Power Mode.

Lab measurements are desirable for determining an empirically validated threshold for operation modes.

Because both options for the control logic can be implemented with a standard low power microcontroller [12] and presents no particular challenge from being implemented in a UHV technology, the implementation of this block was left for a future design stage.

Figure 3.28 on the following page shows the symbol used to represent the control logic block in the schematics for this document.

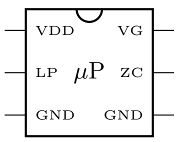


Figure 3.28: Symbol for the control logic block that implements a state machine like the ones shown in Figs. 3.26 on page 46, 3.27 on the preceding page

3.6 Top Level

After describing all basic components in Sections 3.1 on page 20, 3.2 on page 25, 3.4 on page 43 and 3.5 on page 46, it is possible to describe the interconnections at the Top Level schematic for the Dimmer ASIC shown in Figure 3.29.

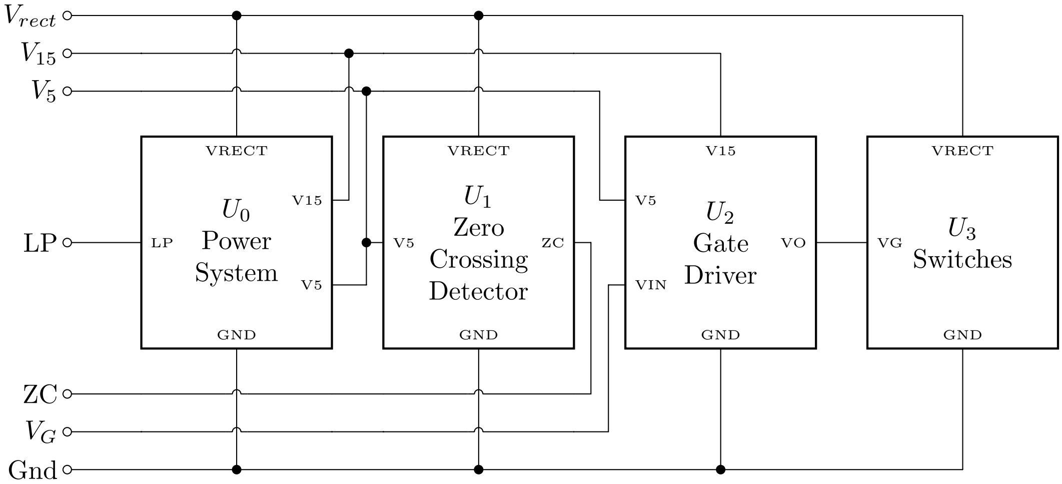


Figure 3.29: Dimmer ASIC top level diagram, using the Switches, Gate Driver, Power Management System, and Zero Crossing Detector symbols from Figures 3.25 on page 45, 3.6 on page 24, 3.10 on page 28, and 3.20 on page 38 respectively.

The Dimmer ASIC can be represented hierarchically with a single symbol as shown in Figure 3.30.

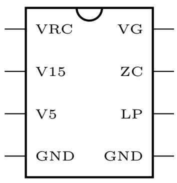


Figure 3.30: Dimmer ASIC symbol for the schematic shown in Figure 3.29

Taking into account all components that could not be integrated into the IC, a typical set up with all necessary components is shown in Figure 3.31 on the next page.

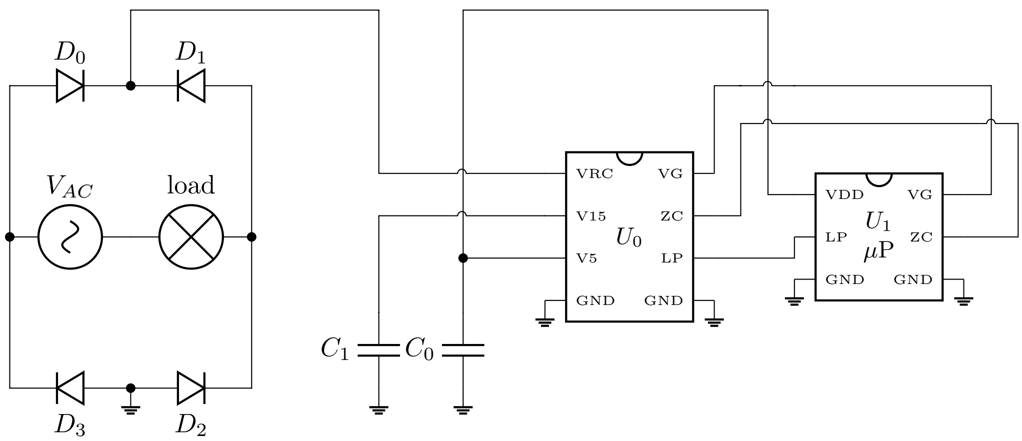


Figure 3.31: Dimmer ASIC typical set up with all necessary components. Where V_{AC} is the AC source, *load* is the load, D_{0-3} are 350 V discrete diodes, C_{0-1} are tank capacitors for the DC sources, U_0 is the Dimmer ASIC from Figure 3.30 on the preceding page and U_1 is a standard low power microcontroller as specified in Section 3.5 on page 46.

Chapter 4

Simulations

4.1 Switches

Because of the importance of the main switches, several simulations follow to validate the design. Simulations were performed for the three corner models given by the manufacturer: Typical Mean (TM), Worst Slow (WS) and Worst Power (WP).

Performing SPICE simulations for integrated IGBTs is a complex process that requires specialized tools. The original plan of using Synopsys HSPICE [26] could not be realized, because it does not have support for IGBTs, and offers MOS approximations instead. Mentor Eldo [27] and Tanner EDA [28] had to be licensed and used in its place. Setting up a proper design environment for modelling and working with IGBTs was a long process that took several months of work to show results.

The I–V curve for the IGBT is included in Figure 3.4, and heat dissipation as a function of power delivered to the load is included in Figure 3.5 on page 24, both in Section 3.1.

4.1.1 DC transfer

In Figure 4.1 on the next page a simulation setup is shown, to test the switches dissipated power in order to select an appropriate gate driving voltage.

Simulations were run for the maximum peak value of I_{CE} that the ASIC is designed to withstand, as shown in Table 4.1.

	Value	Unit
I_{CE}	500	mA

Table 4.1: Values for the devices in the schematic from Figure 4.1 on the following page.

Simulation results are shown in Figure 4.2 on page 53 and Table 4.2 on the following page.

At a first glance, the results are exactly the same for WP, TM and WS, probably because the SPICE simulation models provided by the manufacturer are not properly taking into account DC variations for their IGBTs.

A second observation is that the choice of $V_G = 15\,\mathrm{V}$ is high enough to be well into the flat region of the DC transfer, and a V_G of $20\,\mathrm{V}$ would not make a significant difference in conductivity.

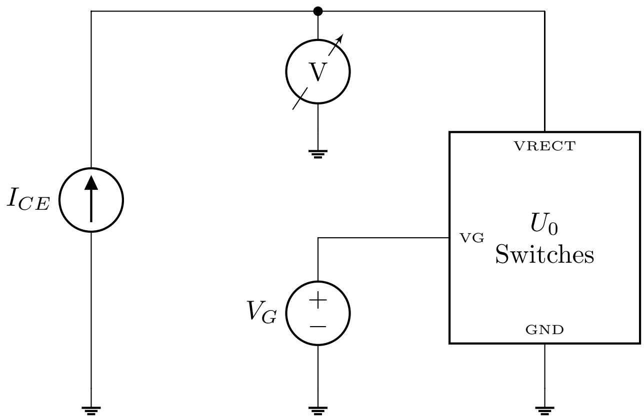


Figure 4.1: Schematic of the transient simulation setup for the Switches block. Where I_{CE} is the maximum peak current for which the ASIC is designed, V_G is the gate voltage that was swept, and U_0 is the Switches block specified in section 3.1 on page 20.

V_G	WP	TM	WS	Unit
5	1.56	1.56	1.56	W
10	1.02	1.02	1.02	W
15	0.947	0.947	0.947	W
20	0.913	0.913	0.913	W

Table 4.2: Switches DC simulation result.

4.1.2 Transient simulation

A test bench circuit was designed to measure dynamic power dissipation in the switches, as shown in Figure 4.3 on page 54.

Simulations were run for $V_G = 15\,\mathrm{V}$ that represents the closed state of the Switches. Results are shown in Figure 4.4 on page 55 and Table 4.3.

	WP	TM	WS	Unit
Peak Current	0.588	0.580	0.572	A
Peak Voltage	2.11	2.09	2.07	V
Peak Power	1.24	1.21	1.18	W
Average Power	0.661	0.651	0.638	W

Table 4.3: Simulation for Switches.

Table 4.3 shows power dissipation, in all cases is well under the target specifications from Table 1.1 on page 15.

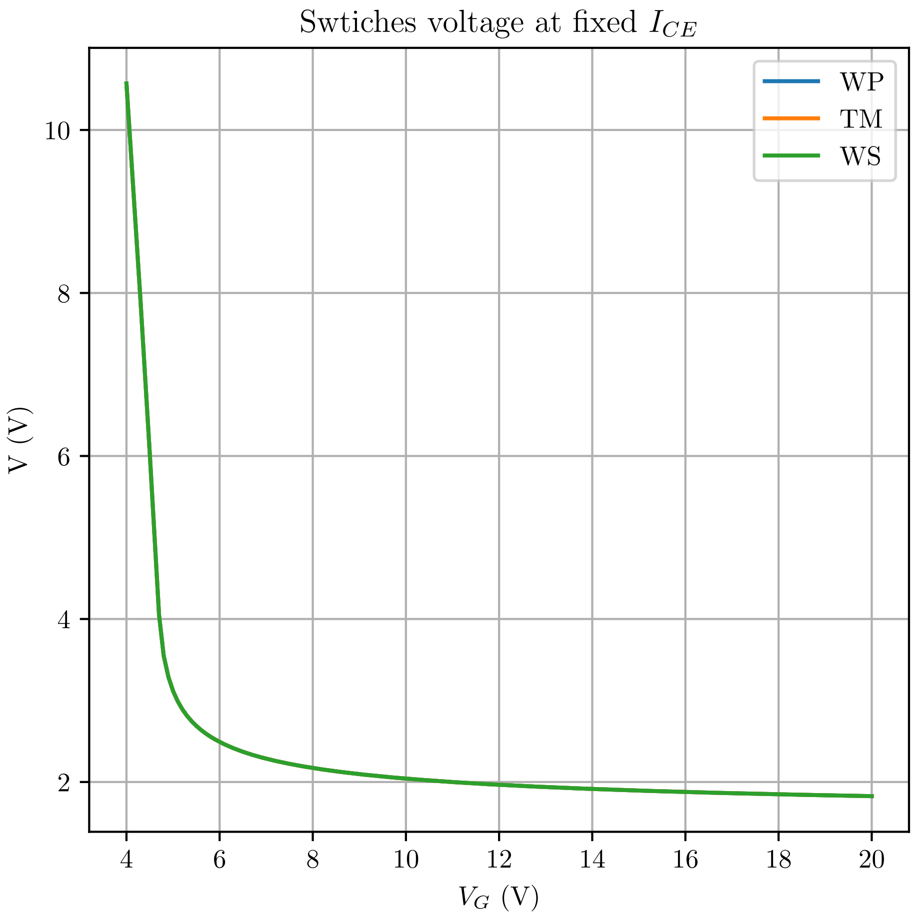


Figure 4.2: Simulation for Switches from Figure 4.1 on the preceding page.

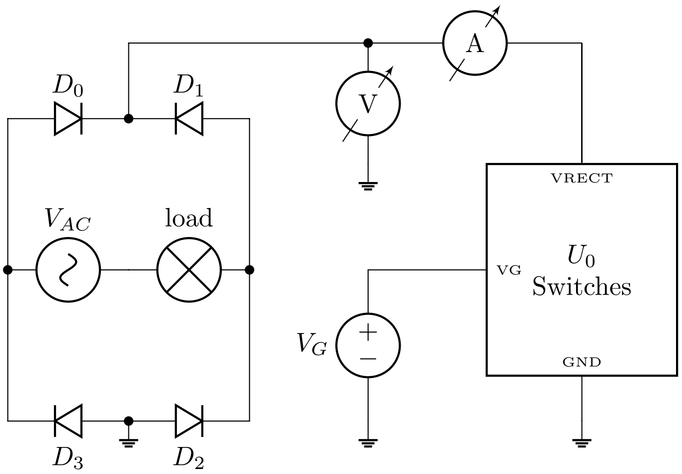


Figure 4.3: Schematic of the transient simulation done on the Switches block. Where V_{AC} is the AC source, *load* is a resistive load, V_G is a voltage source to control the conduction state, and U_0 is the Switches block specified in section 3.1 on page 20.

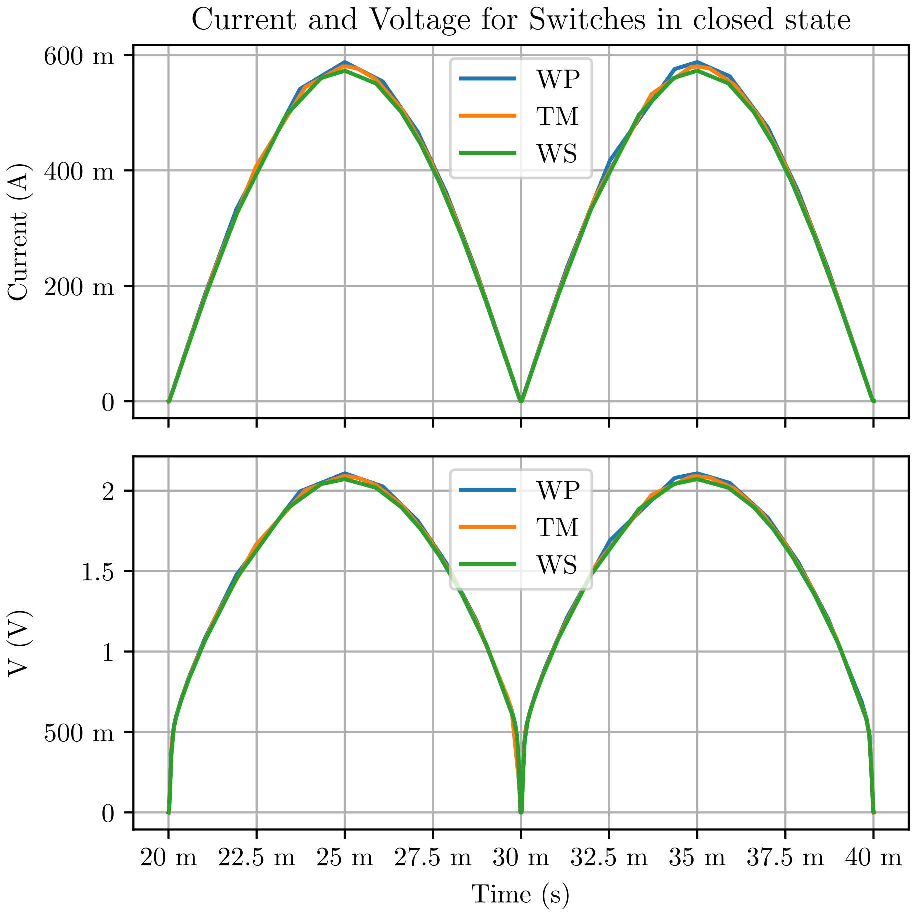


Figure 4.4: Simulation for Switches from Figure 4.3 on the previous page in closed state.

4.2 Power Management System

To validate the design, all simulations with exception of the start up transient from subsection 4.2.1 were performed for the three corners TM, WP, WS.

4.2.1 Start Up

A transient simulation of a power up sequence was done for the power management system in Figure 3.16 on page 34 for both low and high power modes. The simulation setup is shown in Figure 4.5.

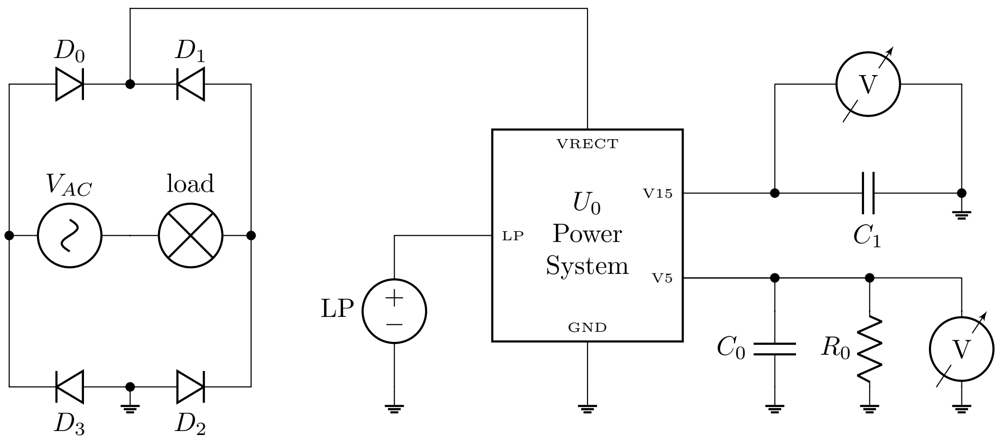


Figure 4.5: Schematic of the start up simulation done on the power management system. Where V_{AC} is the AC source, *load* is a resistive load, *LP* is a voltage source to control the operation mode, (C_0, C_1) are the 5 V and 15 V DC tank capacitors, and R_0 is used to emulate the current consumption from a low power microcontroller.

All components have the specifications in Table 4.4, and simulation results are shown in Figure 4.6 on the following page and Table 4.5 on the next page.

Device	Value	Unit
V_{AC}	230	V
f_{AC}	50	Hz
R_0	540	Ω
LP	0 to 5	V
C_0	10	nF
C_1	100	µF
R_0	10	kΩ

Table 4.4: Values for the devices in the schematic from Figure 4.5.

Low power mode is considerably slower, because the capacitors are charging at a lower current. However, in both cases, the circuit converges to the target voltage levels of 5 V and 15 V.

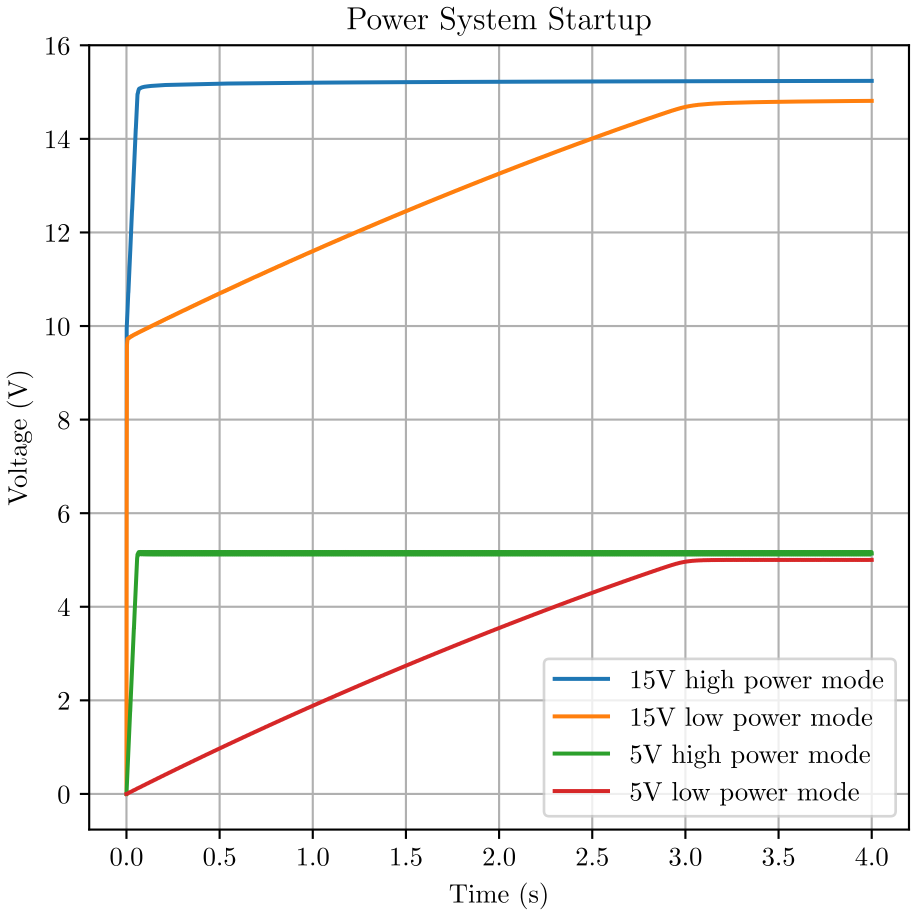


Figure 4.6: Power management circuit start up transient simulation for low and high power mode with the schematic shown in Figure 4.5 on the previous page.

Source	Mode	Final Value (V)	Convergence Time (s)
V_5	High Power Mode	5.15	0.0557
V_5	Low Power Mode	5.00	2.823
V_{15}	High Power Mode	15.24	0.0531
V_{15}	Low Power Mode	14.81	2.545

Table 4.5: Power management start up convergence voltage and time. Convergence is considered when 95 % of the final value is reached.

4.2.2 Steady State, Idle

A transient simulation was performed for the Power Management System to measure steady state current drawn in from V_{rect} at idle state for both low and high power mode. This will cause the largest power consumption for the Power Management System, because the main switches will never enter conduction, and thus V_{rect} will never be chopped.

The simulation set up shown in Figure 4.7 with capacitors C_0, C_1 charged to their steady state voltages, as shown in Table 4.6.

	Value	Unit
$V(C_0)$	5	V
$V(C_1)$	15	V

Table 4.6: Initial conditions for the transient simulation done on the Power Management System at maximum power conditions shown in Figure 4.7.

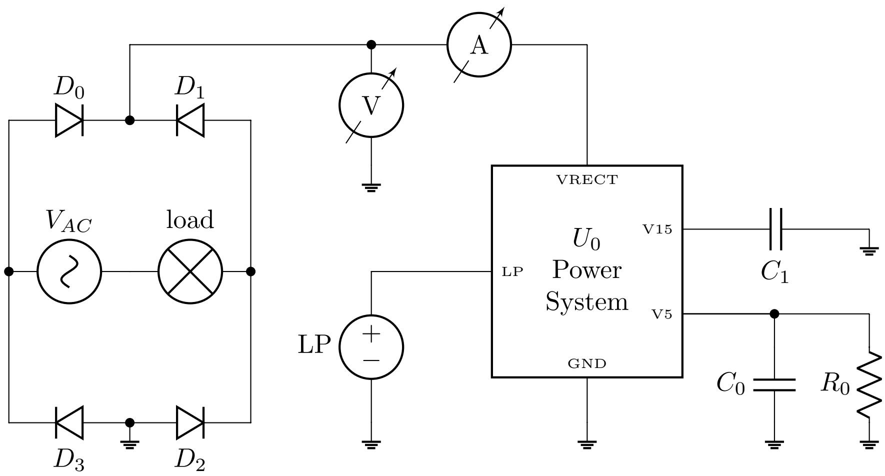


Figure 4.7: Schematic of the transient simulation done on the Power Management System at maximum power conditions. Where V_{AC} is the AC source, *load* is a resistive load, *LP* is a voltage source to control the operation mode, (C_0, C_1) are the 5 V and 15 V DC tank capacitors, R_0 is used to emulate the current consumption from a low power microcontroller, and U_0 is the Power Management System block from Figure 3.21 on page 38.

The simulation results are shown in Figure 4.8 on the following page and are summarized in Table 4.7 on page 60.

It is worth mentioning that current consumption has a very different behaviour in high power mode compared to Low Power Mode. Because it is limited by a MOS transistor, high power mode current tops at a nearly constant value that corresponds to the MOS saturation current. Low Power Mode current is considerably smaller and resembling a chopped and rectified sine wave, because it is limited by a linear integrated resistor.

Note in Table 4.7 on page 60, the average current consumption for all cases is well above the 45 µA required to power a low power microcontroller as described in Section 3.3.3 on page 39.

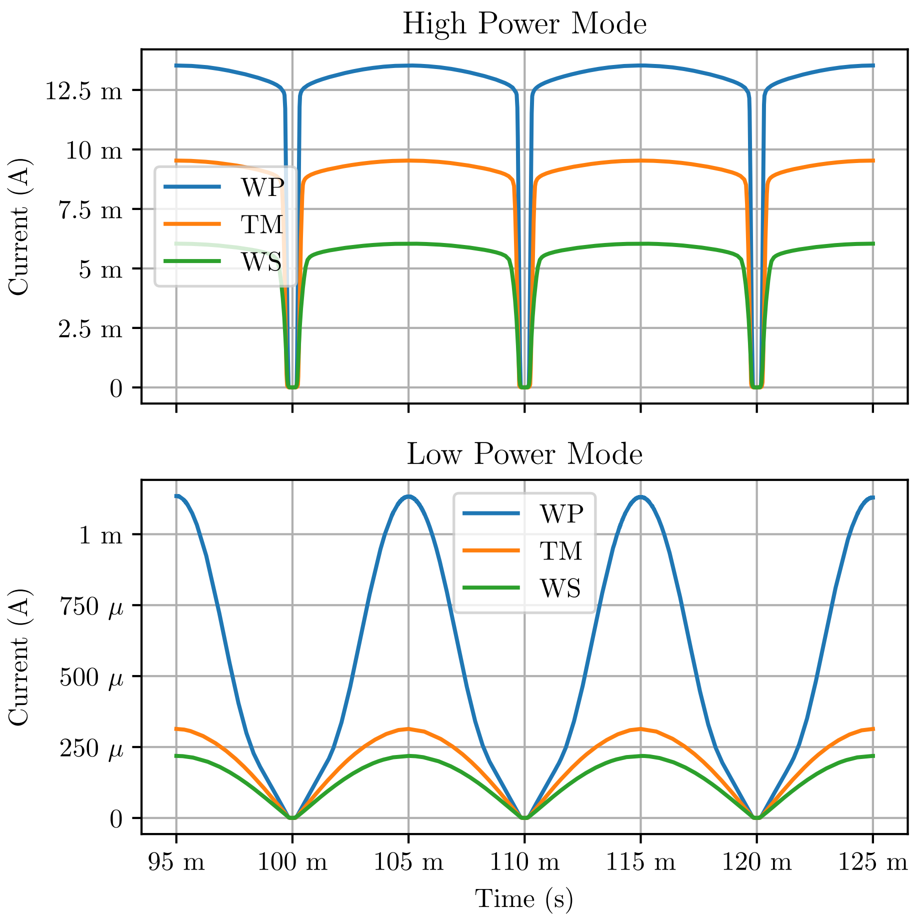


Figure 4.8: Power management circuit maximum power transient simulation for low and high power mode with the schematic shown in Figure 4.7 on the previous page.

The design goal of 200 µA LP average current was not met for TM and WS corners. This can easily be tuned by lowering the HV resistor value. However, it was a design decision not to change the resistor value to avoid excessive current consumption in the WP corner.

4.2.3 Steady State, Maximum Duty Cycle

A transient simulation was performed for the Power Management System to measure steady state current drawn in from V_{rect} at maximum duty cycle for both low and high power mode. This will cause the smallest power consumption for the Power Management System, because the Switches block will enter conduction state for most of the period, and thus V_{rect} will be significantly chopped.

The simulation set up shown in Figure 4.9 on page 61 with capacitors C_0, C_1 charged to their steady state voltages, as shown in Table 4.8 on the next page.

The simulation results are shown in Figure 4.10 on page 62 and are summarized in Table 4.9 on the next page.

	WP	TM	WS	Unit
LP Average Current	532.06	190.90	135.12	µA
HP Average Current	12.54	8.66	5.42	mA
LP Average Power	146.87	49.20	34.74	mW
HP Average Power	2.64	1.87	1.19	W

Table 4.7: Average current for the transient simulation done on the Power Management System at maximum power conditions shown in Figure 4.8 on the previous page.

	Value	Unit
$V(C_0)$	5	V
$V(C_1)$	15	V

Table 4.8: Initial conditions for the transient simulation done on the Power Management System at maximum duty cycle conditions shown in Figure 4.9 on the next page.

As indicated in Table 4.9, the average current consumption for all cases is not enough to power a small microcontroller. Thus for the dimmer to operate for a significant time period at the maximum duty cycle, high power mode should be enabled.

	WP	TM	WS	Unit
LP Average Current	25.66	16.46	11.74	µA
HP Average Current	2.25	1.57	929.81	µA
LP Average Power	3.48	2.20	1.56	mW
HP Average Power	231.55	165.24	103.03	mW

Table 4.9: Average current for the transient simulation of the Power Management System at maximum duty cycle condition.

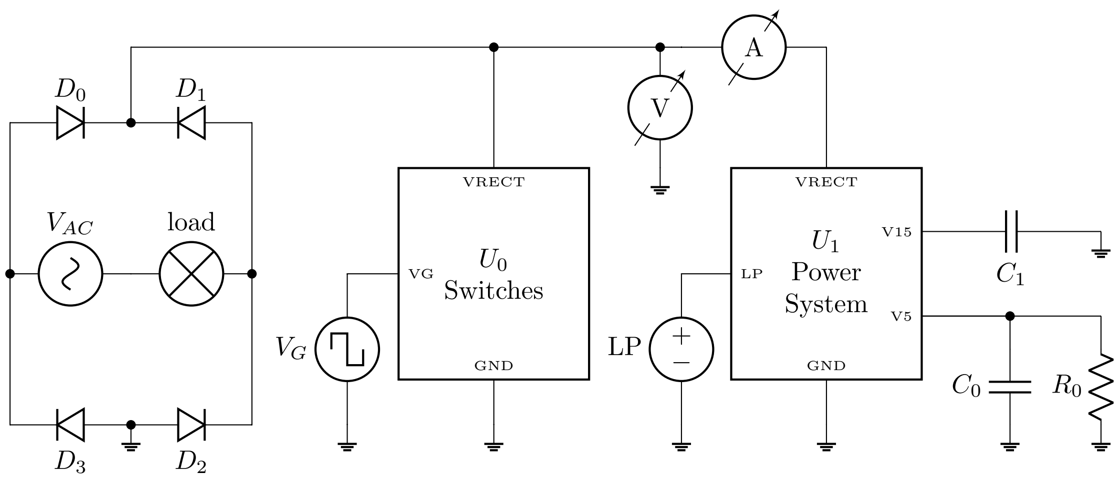


Figure 4.9: Schematic of the transient simulation done on the Power Management System at maximum duty cycle conditions. Where V_{AC} is the AC source, *load* is a resistive load, *LP* is a voltage source to control the operation mode, (C_0, C_1) are the 5 V and 15 V DC tank capacitors, R_0 is used to emulate the current consumption from a low power microcontroller, U_0 is the Switches block from Figure 3.6, and U_1 is the Power Management System block from Figure 3.21.

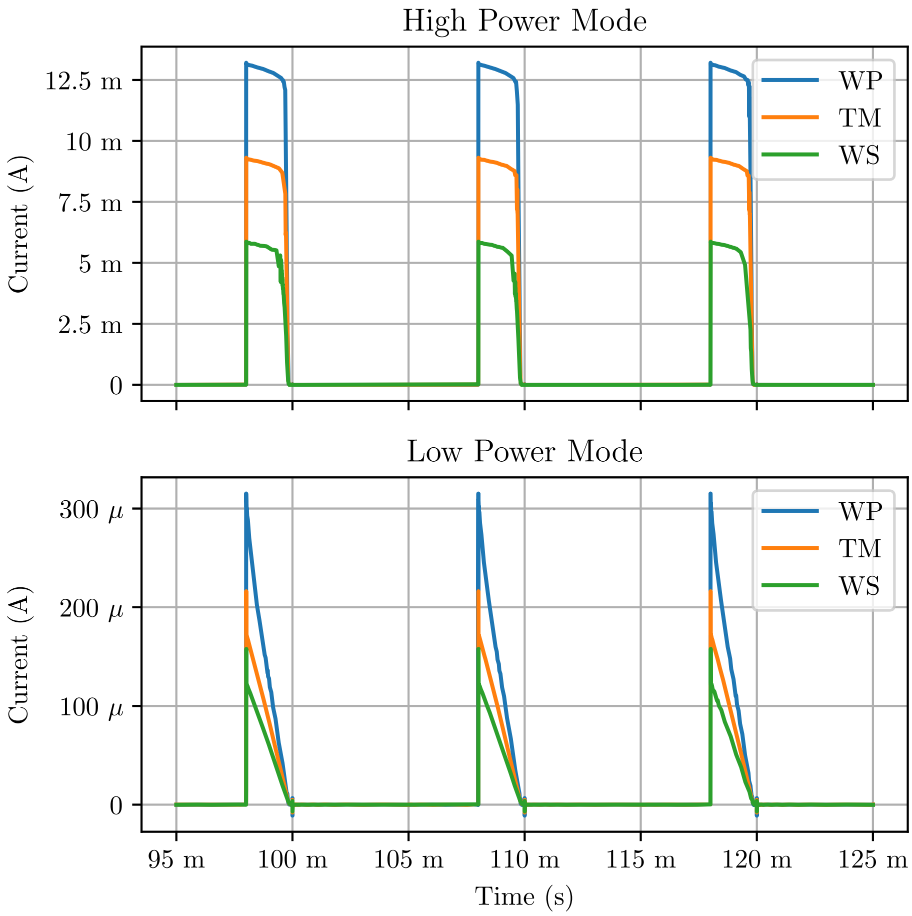


Figure 4.10: Power management circuit maximum duty cycle transient simulation for low and high power mode with the schematic shown in Figure 4.9 on the previous page.

4.3 Zero Crossing Detector

To validate the design, these simulations were performed for the three corner models given by the manufacturer: Typical Mean (TM), Worst Slow (WS) and Worst Power (WP).

4.3.1 Transient Simulation

The end application requires a zero crossing detection on a rectified V_{rect} signal with a very limited time close to the zero. It is crucial that the Zero Crossing Detector is able to detect these occurrences.

A transient simulation had to be performed to account for this aspect with the circuit shown in Figure 4.11, which also includes the Power Management System from section 3.3 on page 29 to include the effect of its capacitive load on V_{rect}.

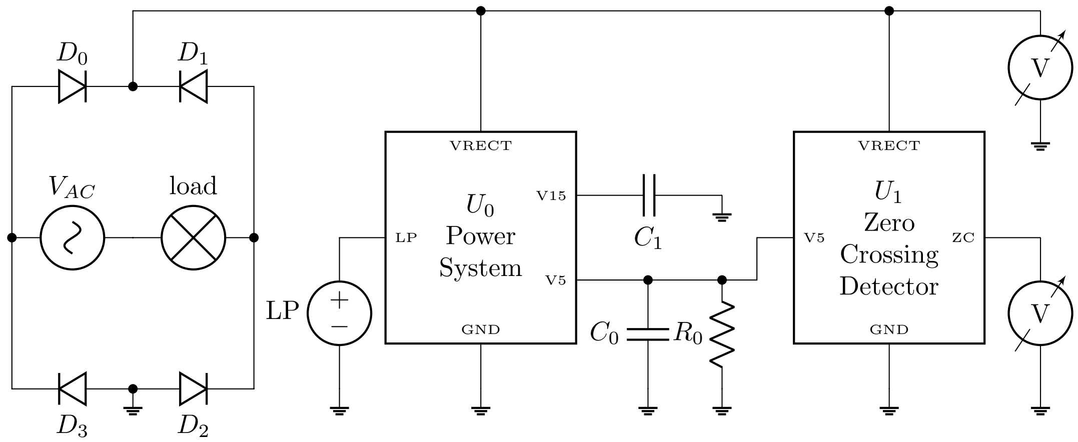


Figure 4.11: Schematic for the Zero Crossing detector transient simulator. Where V_{AC} is the AC source, *load* is a resistive load, *LP* is a 5 V voltage source to control the operation mode, (C_0, C_1) are the 5 V and 15 V DC tank capacitors, R_0 is used to emulate the current consumption from a low power microcontroller, U_0 is the Power Management System from Figure 3.18 on page 36, and U_1 is the Zero Crossing Detector from Figure 3.23 on page 43.

The transient simulation was performed with capacitors C_0, C_1 charged to their steady state voltages, as shown in Table 4.10.

	Value	Unit
$V(C_0)$	5	V
$V(C_1)$	15	V

Table 4.10: Initial conditions for the transient simulation done on the Zero Crossing Detector shown in Figure 4.11.

The results from a first simulation in typical mean conditions are shown in Figure 4.12 on the following page. The Zero Crossing Detector output behaves as expected, with a “high” value only when the rectified AC signal is near zero.

The results are shown in Figure 4.13 on page 65 with a focus on its detection threshold.

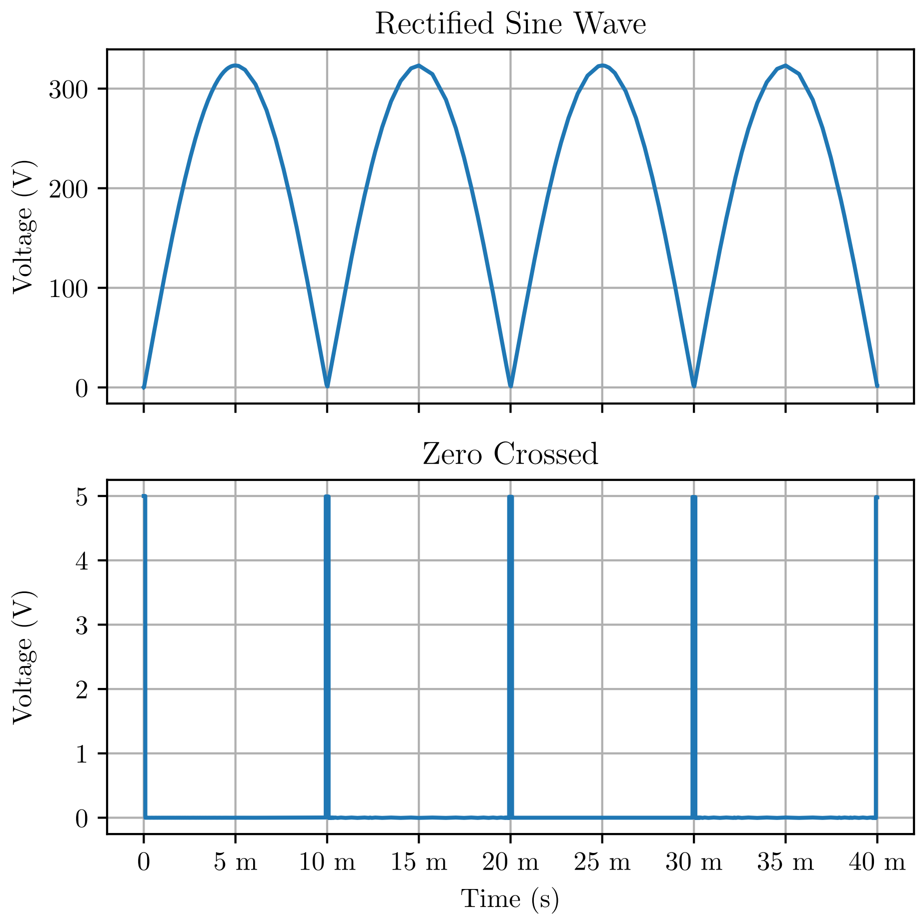


Figure 4.12: Zero Crossing detector transient simulation for the circuit shown in Figure 4.11 on the preceding page.

Note in Figure 4.13 on the following page, the Zero Crossing Detector output behaves as expected for all three corner cases.

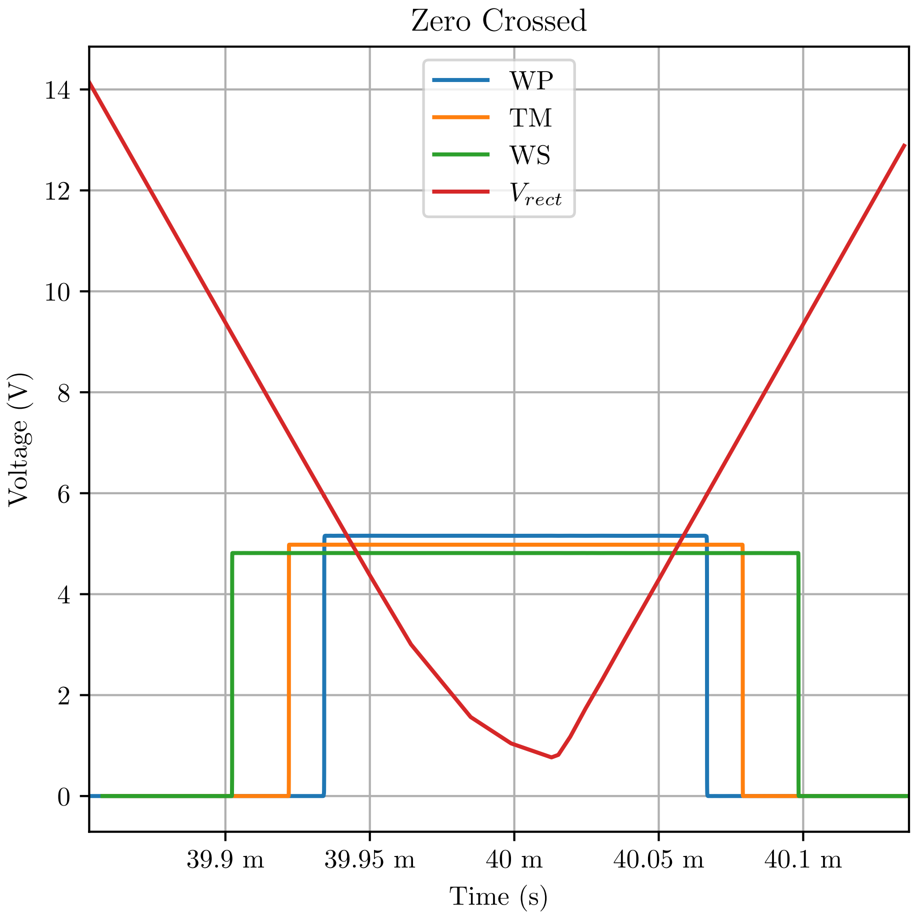


Figure 4.13: Zero Crossing detector transient corner simulations focusing on the detection threshold for the circuit shown in Figure 4.11 on page 63.

4.3.2 DC Transfer

To evaluate the threshold voltage of the Zero Crossing Detector, a DC Sweep SPICE simulation was performed using the setup in Figure 4.14.

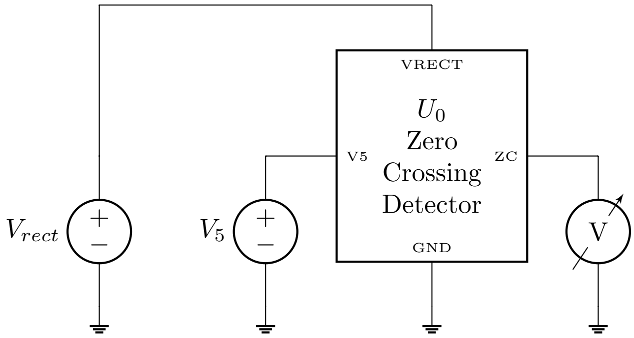


Figure 4.14: Schematic of the DC transfer simulation done on the Zero Crossing Detector circuit shown in Figure 3.23 on page 43. Where V_5 is a 5 V fixed DC source, U_0 is the Zero Crossing detector shown in Figure 3.25 on page 45, and V_{rect} is the DC source for which its value is swept from 0 V to 325 V.

The results are shown in Figure 4.15 on the following page and summarized in Table 4.11.

Corner	V_{th} (V)
WP	5.8
TM	7.1
WS	9.3

Table 4.11: Threshold voltage for the Zero Crossing Detector in corner simulations for the schematic shown in Figure 4.14.

By comparing the simulation results from Figure 4.15 on the following page with the expected outcome from Figure 3.24 on page 44 it can be concluded that the circuit works as expected.

The obtained threshold values are sufficient for the Zero Crossing Detector on V_{rect} for the ASIC, as it will be shown in Section 4.3.1 on page 63.

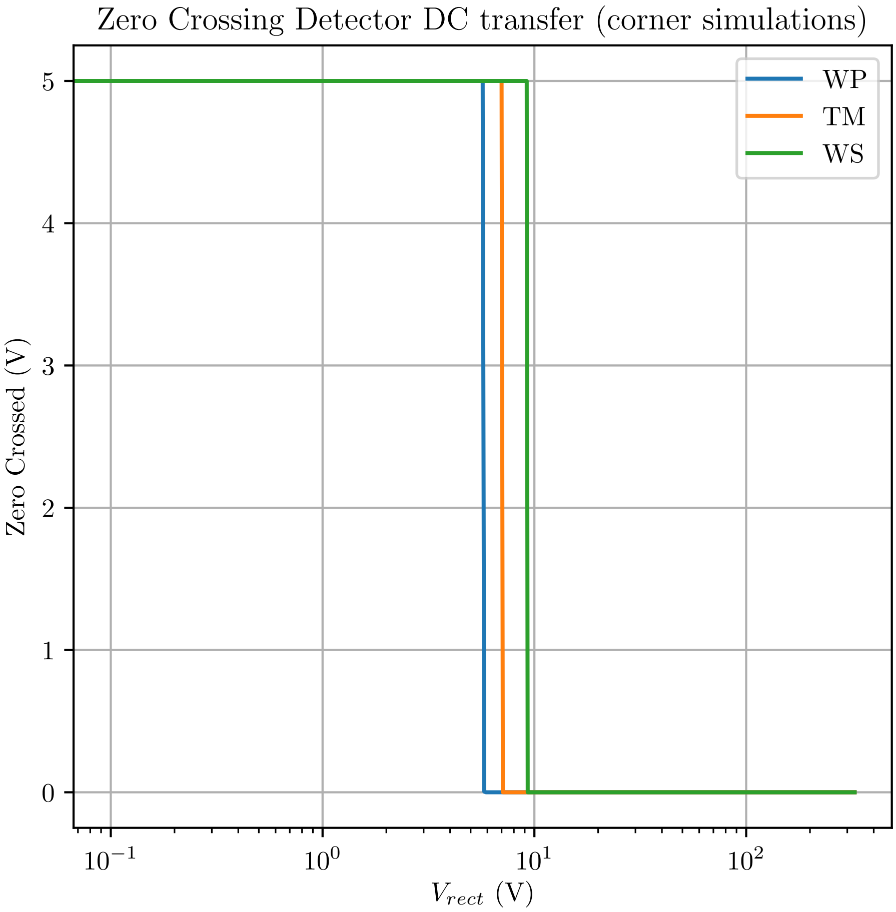


Figure 4.15: Zero Crossing detector DC transfer simulation results, from Figure 4.14 on the previous page.

4.4 Top Level Circuit

A transient simulation was performed at top level for the whole circuit with a configuration like in Figure 3.31 on page 50, emulating the microcontroller with selected voltage sources and a resistor.

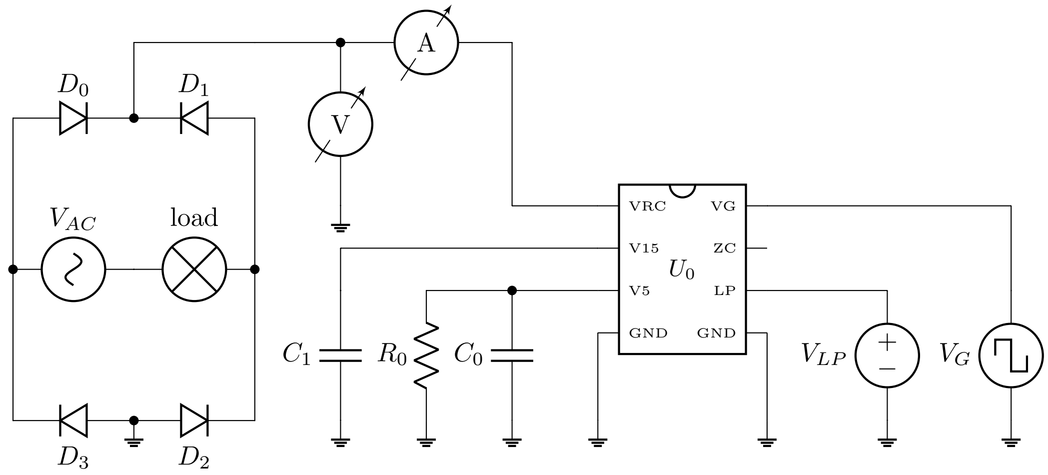


Figure 4.16: Top level transient simulation test bench. Where V_{AC} is the AC source, *load* is a resistive load, V_{LP} is a 5 V voltage source to control the operation mode, V_G is a square wave voltage source to emulate the dimmer activation signal, (C_0, C_1) are the 5 V and 15 V DC tank capacitors, R_0 is used to emulate the current consumption from a low power microcontroller, and U_0 is the Top Level Dimmer from Figure 1.4 on page 15.

The transient simulation was performed with capacitors C_0, C_1 charged to their steady state voltages, as shown in Table 4.12.

	Value	Unit
$V(C_0)$	5	V
$V(C_1)$	15	V

Table 4.12: Initial conditions for the transient simulation done at Top Level shown in Figure 4.16.

To validate the design, all simulations in this section except the typical condition from subsection 4.4.1 were performed for the three corners TM, WS, WP.

The simulations in this section took less than one hour for each run in the EDA servers at Universidad Católica del Uruguay.

4.4.1 Typical

A typical scenario transient simulation was run with V_G starting from an idle state to a square wave with the dimmer in low power mode to illustrate the working principles of the ASIC. The simulation results are shown in Fig 4.17 on the following page.

Comparing the simulation results in Figure 4.17 on the next page and the expected behaviour in Figure 1.2 on page 13, the whole system works as expected.

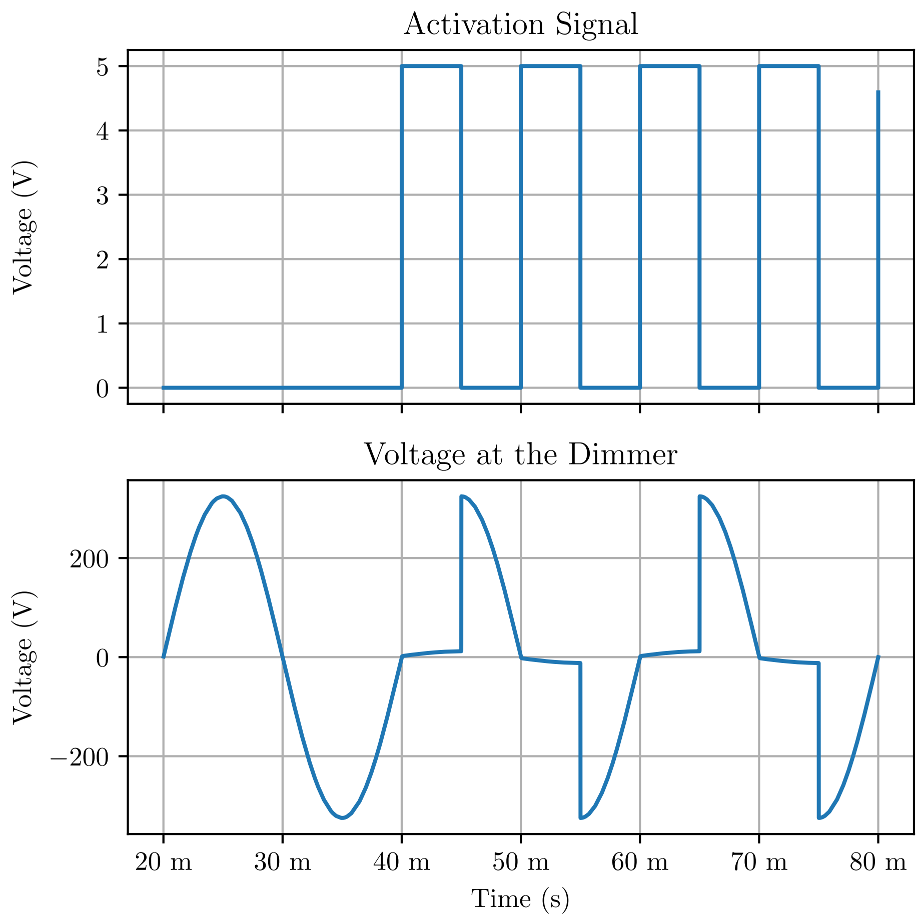


Figure 4.17: Top level transient simulation for the UHV dimmer, as shown in Figure 4.16 on the preceding page.

4.4.2 Idle state, low power mode

To measure idle state power consumption for the ASIC, a transient simulation was performed like in Figure 4.16 on the previous page, with V_{LP} set to 5 V and V_G fixed to 0 V.

The results are shown in Figure 4.18 on the following page and Table 4.13.

	WP	TM	WS	Unit
Average Power	223	100	70.9	mW

Table 4.13: Average Power consumed by the ASIC in idle state.

4.4.3 Maximum duty cycle, high power mode

To measure power consumption at maximum duty cycle for the ASIC, a transient simulation was performed like in Figure 4.16 on the preceding page, with V_{LP} set to 0 V and V_G oscillating

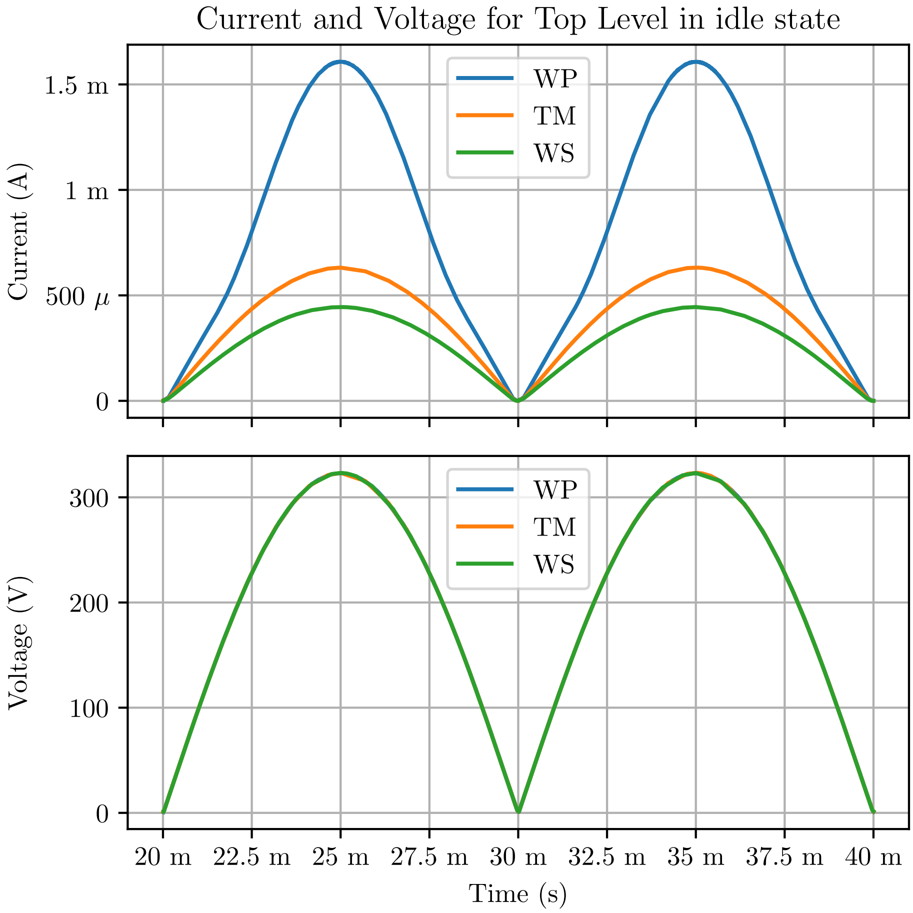


Figure 4.18: Top level transient simulation for the UHV dimmer in idle state using the schematic from Figure 4.16 on page 68.

with an 80 % duty cycle.

The results are shown in Figure 4.19 on the next page and Table 4.14 on the following page.

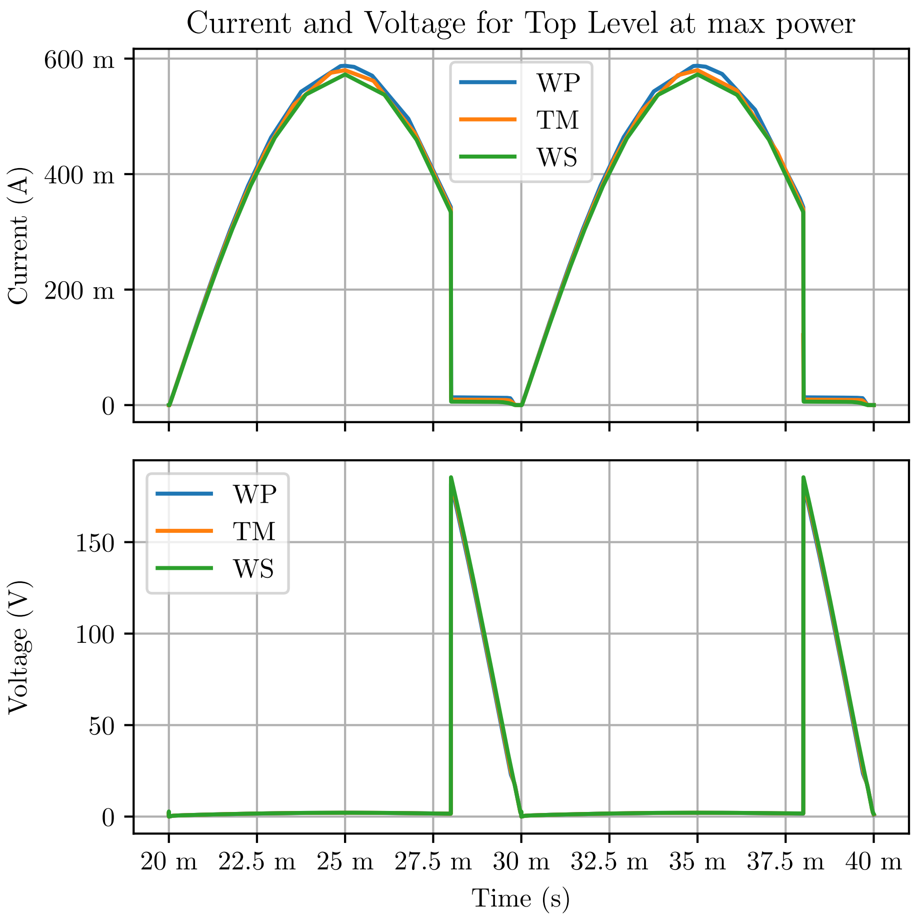


Figure 4.19: Top level transient simulation for the UHV dimmer at maximum duty cycle using the schematic from Figure 4.16 on page 68.

	WP	TM	WS	Unit
Average ASIC Power	857	782	713	mW
Average Load Power	87.7	85.3	83.0	W
P_{load}/P_{src}	97.2	96.0	94.8	%
P_{load}/P_{ideal}	89.6	87.1	84.7	%

Table 4.14: Average Power consumed by the ASIC in maximum duty cycle conditions. P_{load} represents the average power reaching the load, P_{src} represents the average power coming out from the AC source, P_{ideal} represents the power that would be reaching the load if the dimmer was not connected.

Chapter 5

Layout

5.1 Switches

The layout for the proposed implementation of the Switches block is shown on Figure 5.1.

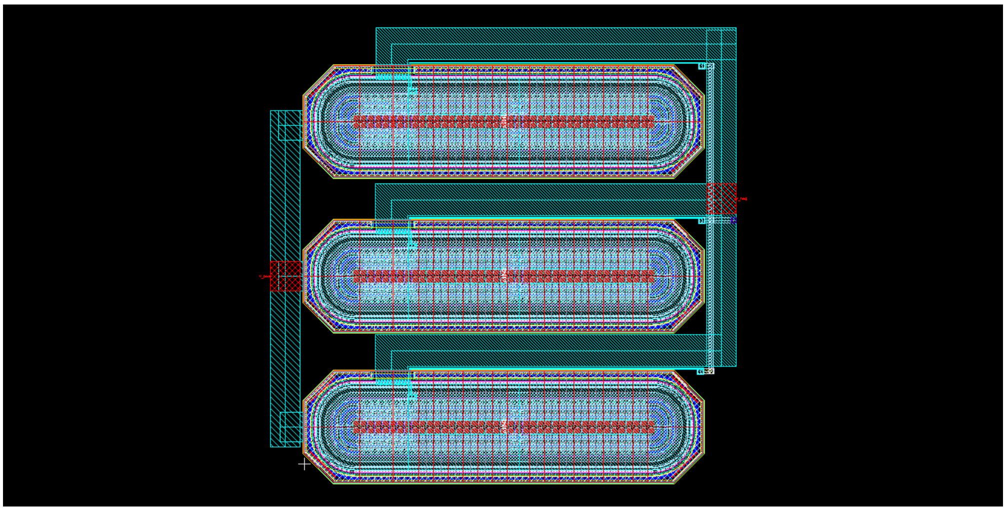


Figure 5.1: Switches layout of the UHV dimmer.

Three large devices that correspond to the three parallel IGBTs can easily be recognized as the main switches for the ASIC. Wires connecting these devices were drawn with the highest possible metal and very thick lines to support the largest possible current.

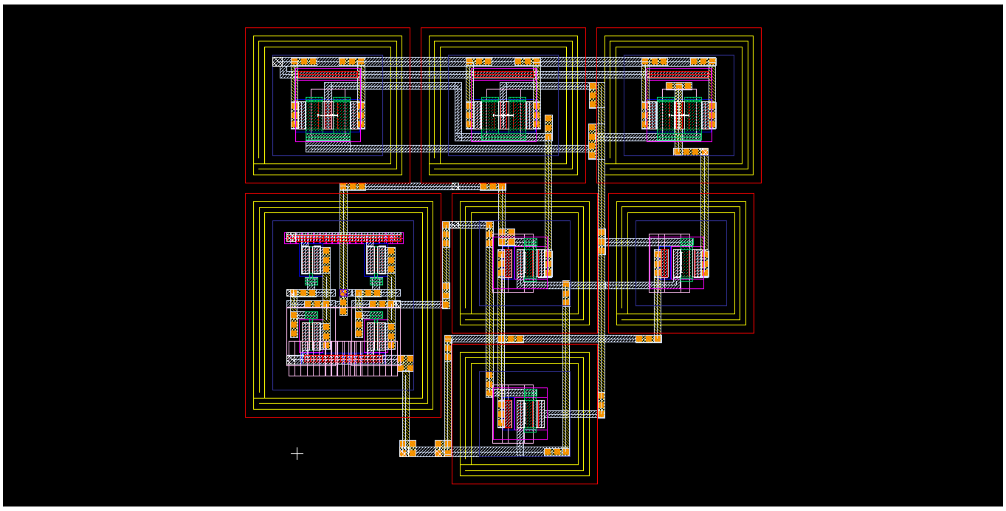
Layout dimensions are presented in Table 5.1.

	Value	Unit
W	1.89	mm
H	1.85	mm
Area	3.51	mm^2

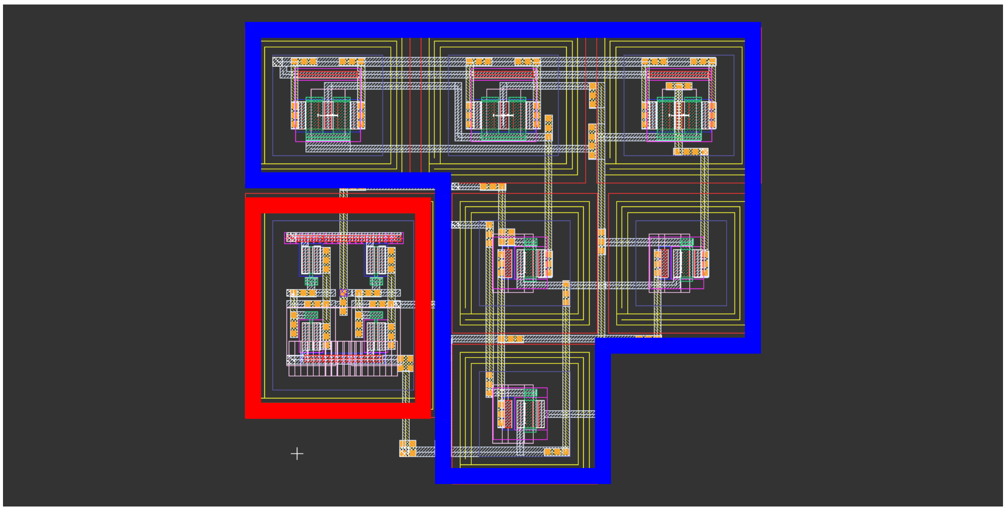
Table 5.1: Layout size for the switches in Figure 5.1.

5.2 Gate Driver

The layout of the Gate Driver block is shown on Figure 5.2.



(a) Gate Driver layout exported directly from the layout editor.



(b) Low voltage MOS transistors are shown in red, high voltage MOS are shown in blue.

Figure 5.2: Gate Driver layout of the UHV dimmer.

It is worth noting that every high voltage MOS transistor requires its own trench, thus their layout is significantly sparser.

Layout dimensions are presented in Table 5.2 on the following page.

	Value	Unit
W	189	µm
H	168	µm
Area	31 800	μm^2

Table 5.2: Layout size for the Gate Driver in Figure 5.2 on the preceding page.

5.3 Power Management System

5.3.1 Voltage Divider

The layout of the Voltage Divider block is shown on Figure 5.3 on the next page.

It is worth noting that low voltage MOS transistors require significantly less area than their high voltage counterparts because their low voltage allows them to share the same silicon trench.

Layout dimensions are presented in Table 5.3.

	Value	Unit
W	1.855	mm
H	0.722	mm
Area	1.34	mm^2

Table 5.3: Layout size for the Power Management System Voltage Divider in Figure 5.3 on the following page.

5.3.2 Full Implementation

The layout for the proposed implementation of the Power Management System block is shown on Figure 5.4 on page 76.

The most notable elements of this layout are the UHV resistor, and the UHV MOS transistor. These devices are significantly larger than the rest because of the isolation needed to handle ultra high voltage applied to them.

The dimensions for the proposed layout are given in Table 5.4.

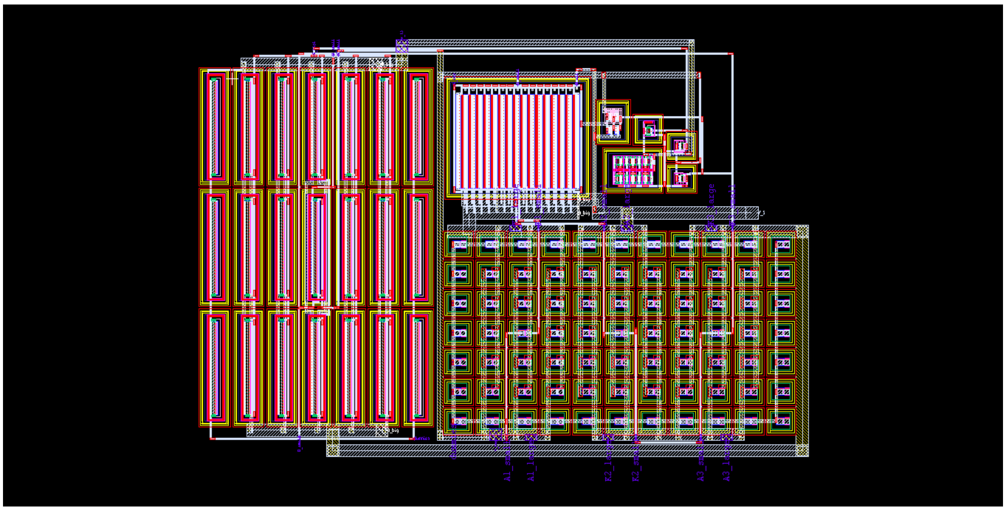
	Value	Unit
W	1.973	mm
H	1.851	mm
Area	3.65	mm^2

Table 5.4: Dimensions for the Power Management System layout shown in Figure 5.4 on page 76.

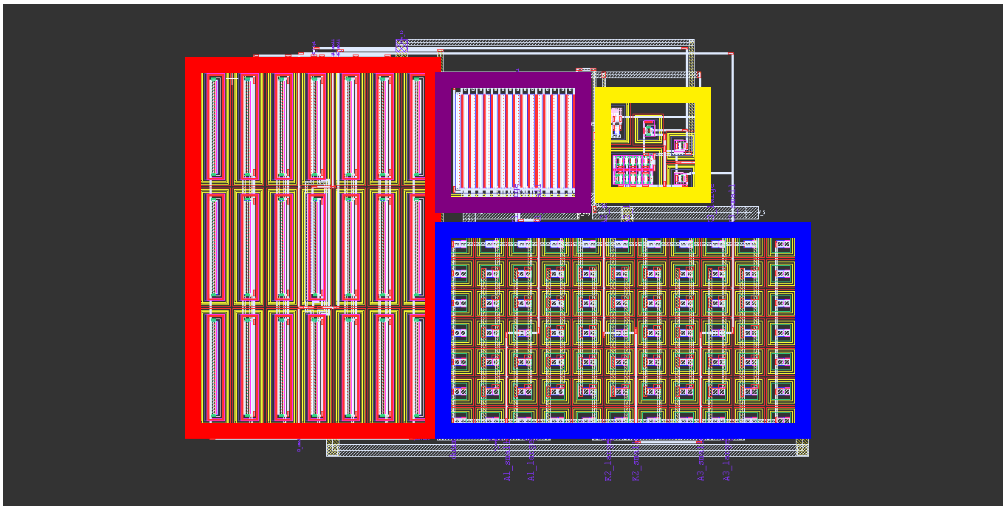
5.4 Zero Crossing Detector

The layout for the proposed implementation of the Zero Crossing Detector block is shown on Figure 5.5 on page 77.

The resistors take up significant area because their resistance value needs to be high to provide low power consumption.

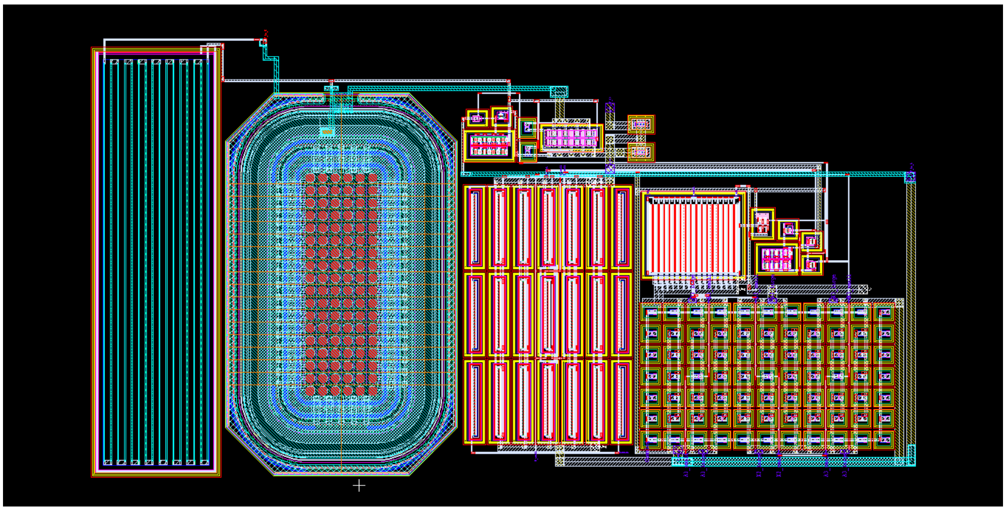


(a) Power System Voltage Divider layout exported directly from the layout editor.

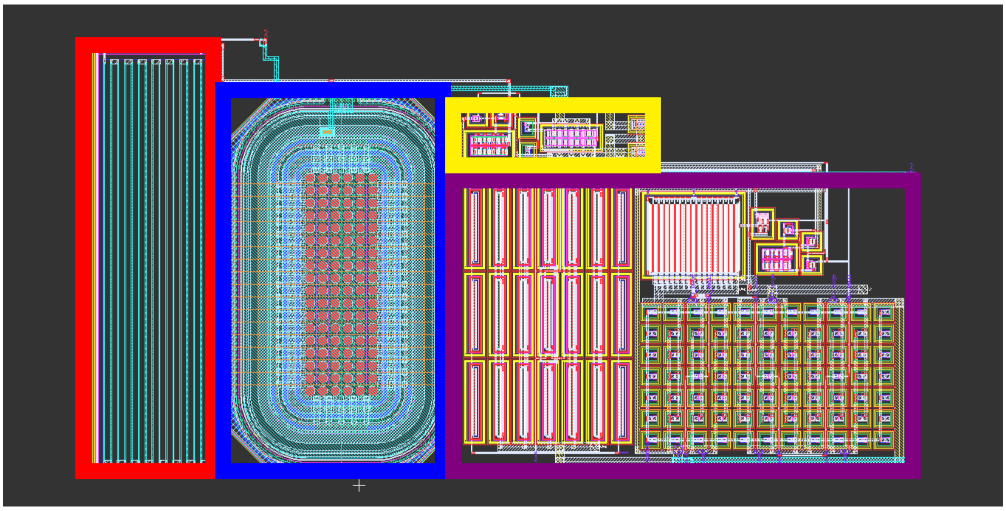


(b) High voltage switching MOS transistors are shown in red, Zener diodes in blue, low voltage MOS transistors in violet, and the remaining logic is shown in yellow.

Figure 5.3: Power System Voltage Divider layout of the UHV dimmer.

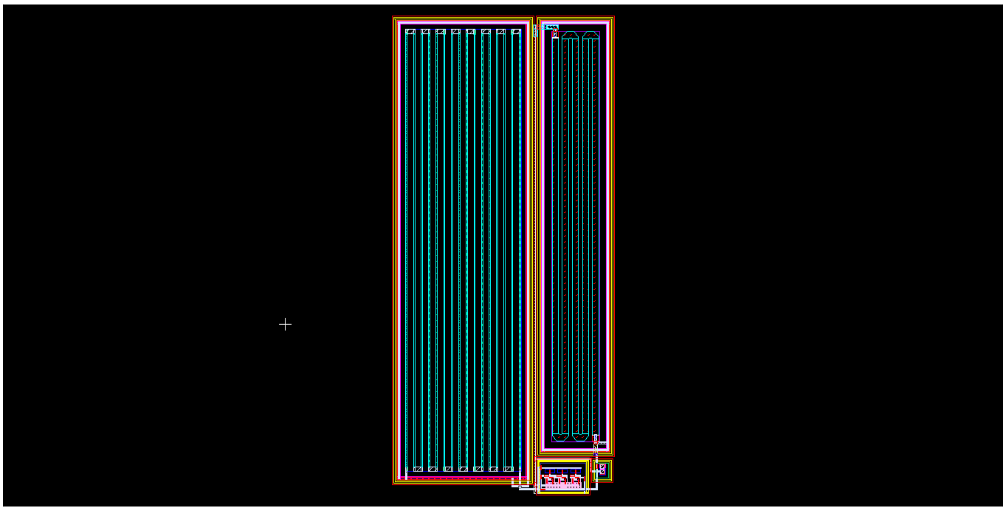


(a) Power System exported directly from the layout editor.

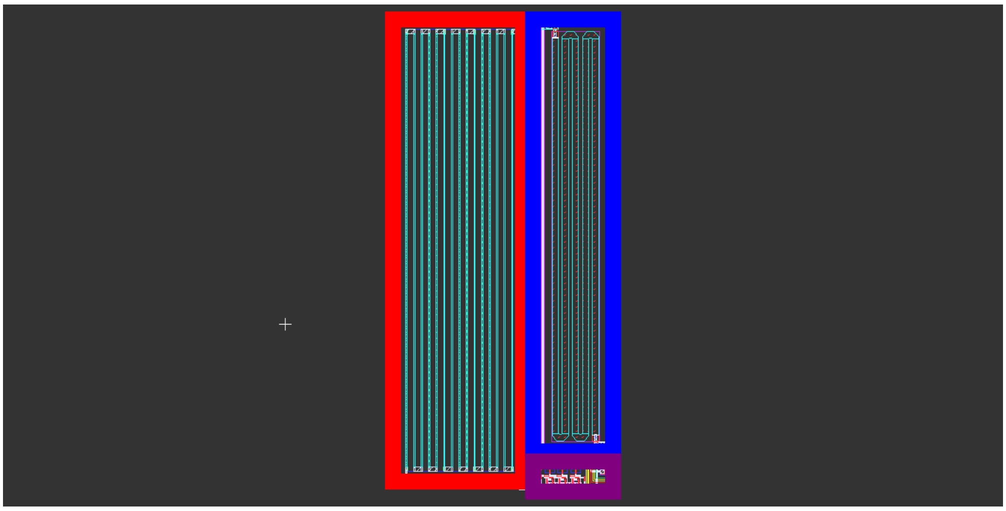


(b) The UHV resistor is shown in red, the UHV MOS transistor in blue, the voltage divider from Figure 5.3 on the previous page in violet, and the remaining logic is shown in yellow.

Figure 5.4: Power System layout of the UHV dimmer.



(a) Zero Crossing Detector exported directly from the layout editor.



(b) The UHV resistor is shown in red, the LV resistor in blue, and the remaining logic is shown in violet.

Figure 5.5: Zero Crossing Detector layout of the UHV dimmer.

The dimensions for the proposed layout are given in Table 5.5.

	Value	Unit
W	0.498	mm
H	1.852	mm
Area	0.922	mm^2

Table 5.5: Dimensions for the Zero Crossing Detector layout shown in Figure 5.5 on the preceding page.

5.5 Input/Output

The layout for the proposed implementation of the Input/Output (IO) block is shown on Figure 5.6 on the next page.

Most of the dimmer IO pads are low voltage digital signals that can be placed using the IO cells provided by the manufacturer [29]. These cells provide a ready to use rail-based ESD protection scheme.

However, high voltage IO pads cannot be protected with rail-based ESD protections and need to use custom designed pad-based ESD protections. HV NMOS devices were used to protect the V_5 and V_{rect} pads for their respective nominal 15 V and 350 V levels, following the design guidelines from [30, 31].

V_{rect} and Gnd were identified as high current nets, and thus were given multiple pads.

5.6 Top Level

The layout for the proposed implementation of the dimmer is shown on Figures 5.7 on page 80 and 5.8 on page 81.

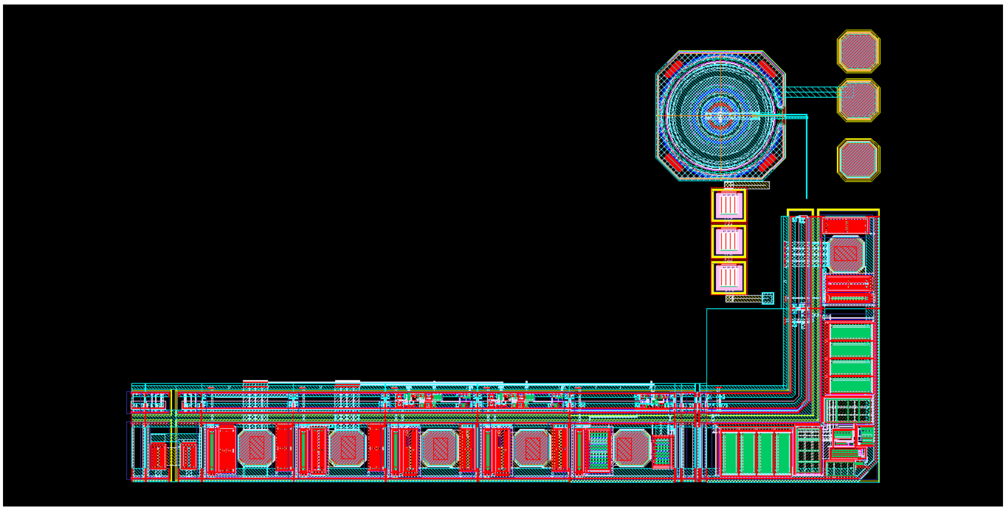
As recommended by the manufacturer, all UHV nets were routed using the highest metal offered by the technology because of its drastically higher conductivity and electromigration limits, as is shown in Table 2.9 on page 19.

On the top, right and bottom borders, the Input-Output (IO) blocks and ESD protections were placed following the manufacturer guidelines.

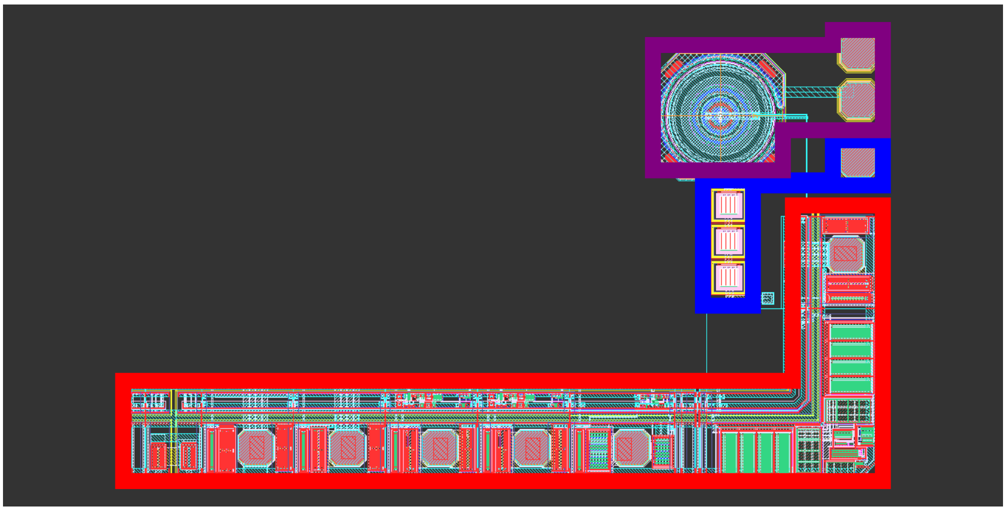
The total die area used by the IC is $10\,\mathrm{mm}^2$ ($W = L = 3.16\,\mathrm{mm}$), of which $6.5\,\mathrm{mm}^2$ are occupied by the dimmer itself.

If integrated diodes were used, it is estimated that the dimmer could be integrated in a die area of $12\,\mathrm{mm}^2$. Integrated capacitors are not a viable option, because 10 nF would require an approximate area of $8\,\mathrm{mm}^2$.

A microscope image of the fabricated ASIC is presented in Figure 5.9 on page 82.



(a) IO exported directly from the layout editor.



(b) The low voltage IO and ESD protections are shown in red, the 15 V net in blue, and the 350 V net in violet.

Figure 5.6: IO layout of the UHV dimmer.

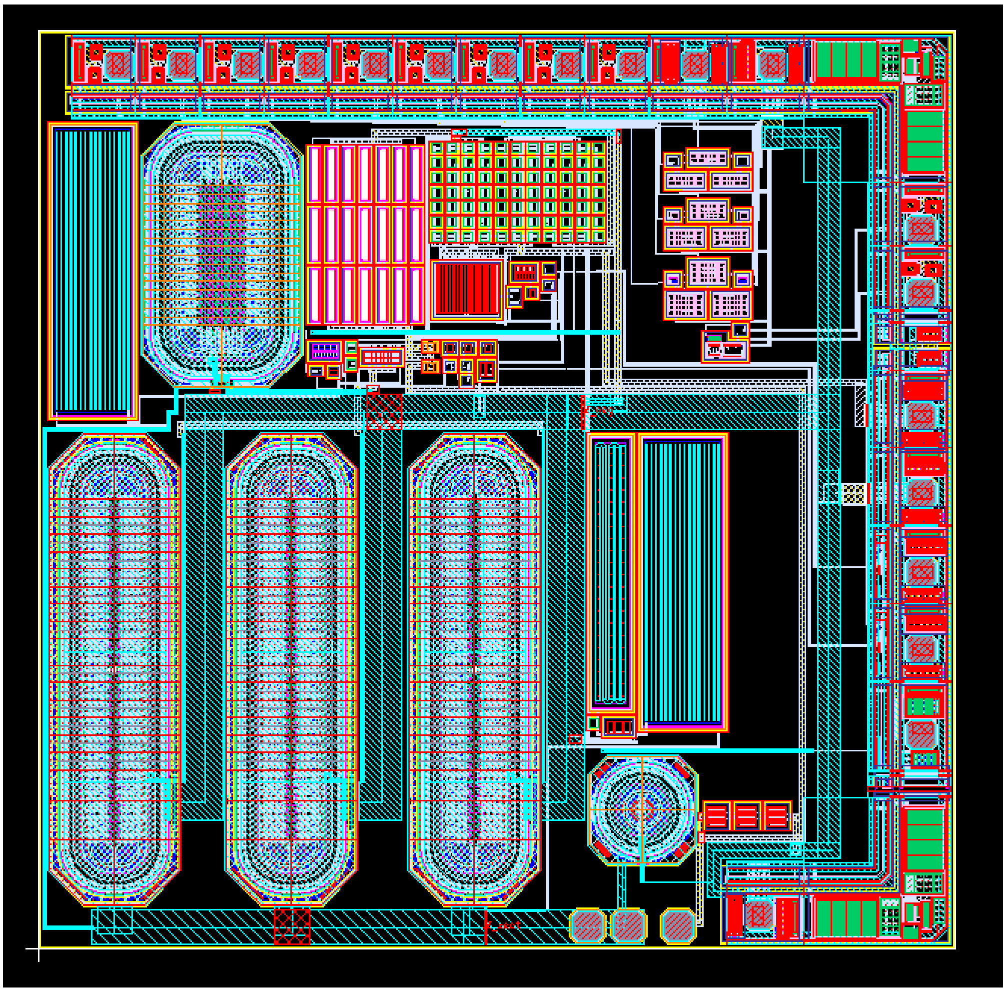


Figure 5.7: Top level layout of the UHV dimmer.

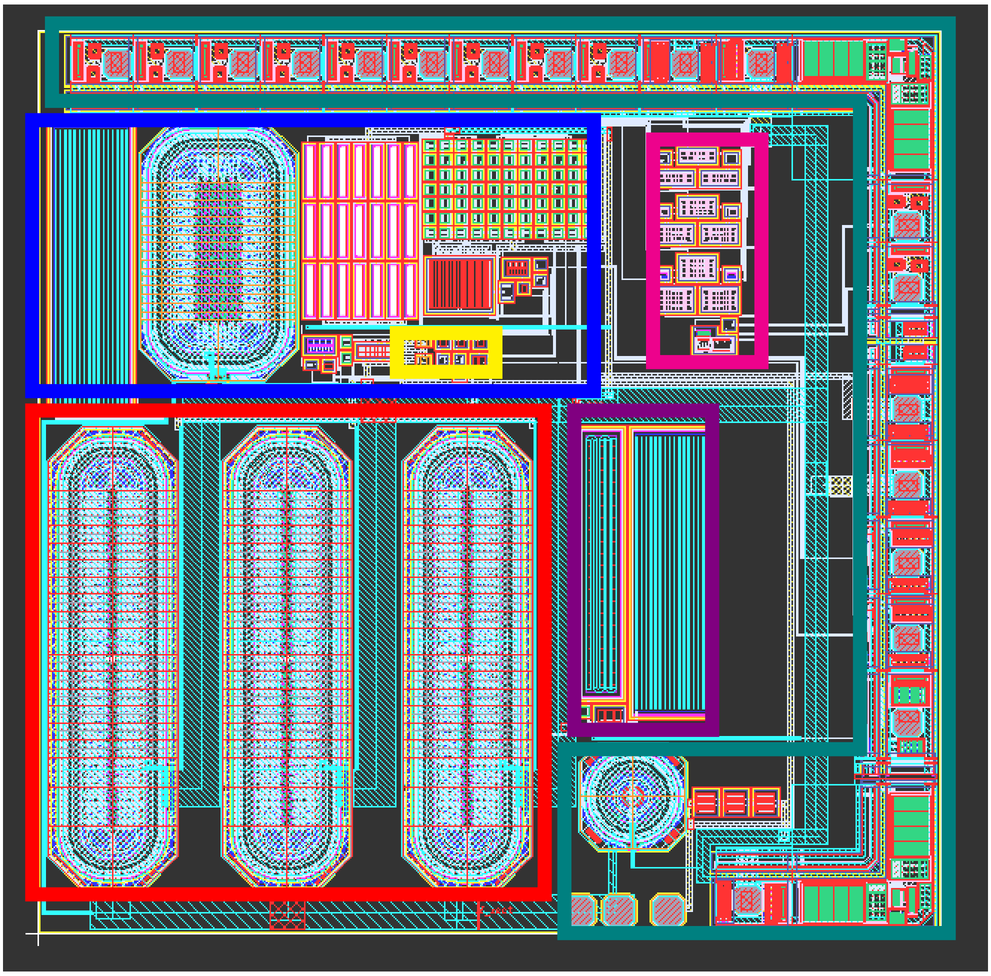


Figure 5.8: Annotated top level layout of the UHV dimmer. The Switches from Figure 5.1 are marked with red, the Power Management System from Figure 5.4 is marked with blue, the Zero Crossing Detector from Figure 5.5 is marked with violet, the Gate Driver from Figure 5.2 is marked with yellow. The IO blocks and ESD protections are marked with teal. The devices on the upper right section (magenta), as well as most of the IO blocks on the top and right borders correspond to a different, unrelated project and are not part of the UHV dimmer.

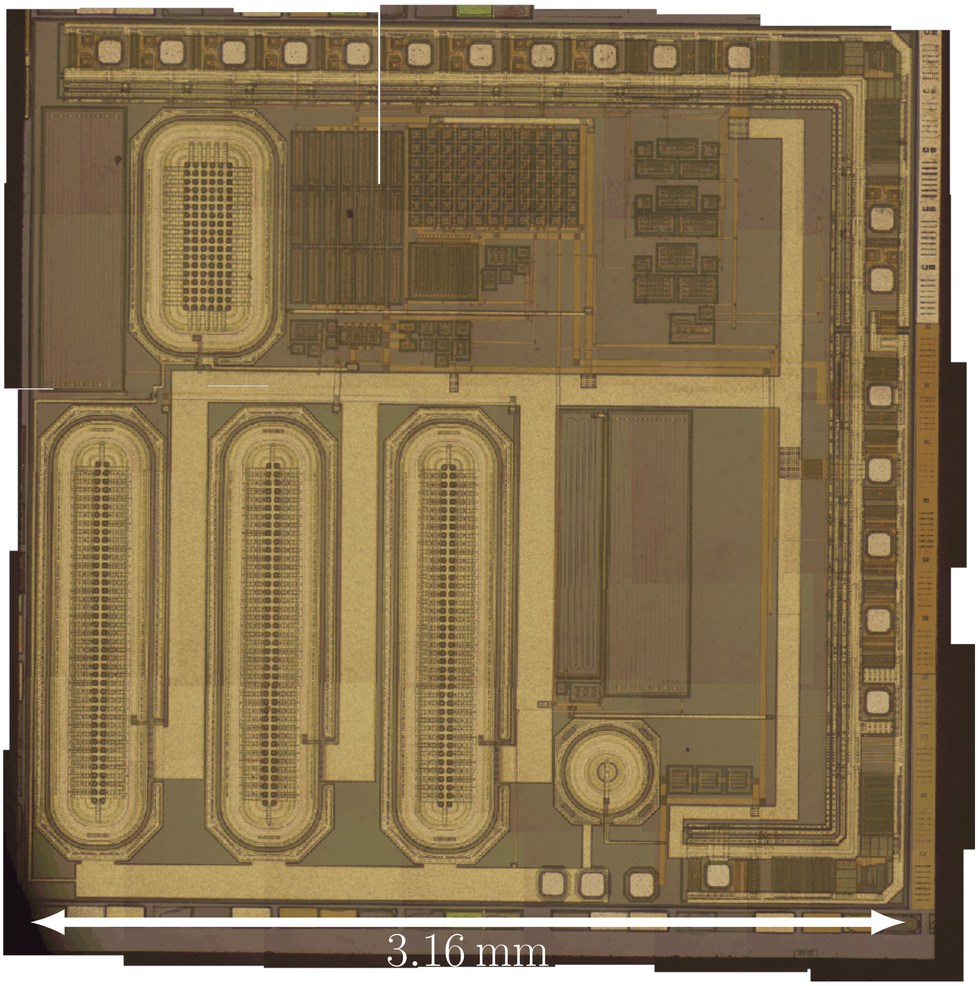


Figure 5.9: Photo of the fabricated ASIC reconstructed from smaller pictures taken with a microscope.

Chapter 6

Measurements

The ASIC was sent for fabrication in a MPW in September 2019, arriving in late February 2020, and encapsulated at early March 2020 in the lab at TEC — Costa Rica [32]. Figure 6.1 shows the physical bonding of the chip to a custom designed PCB (layout and schematics in Appendix B).

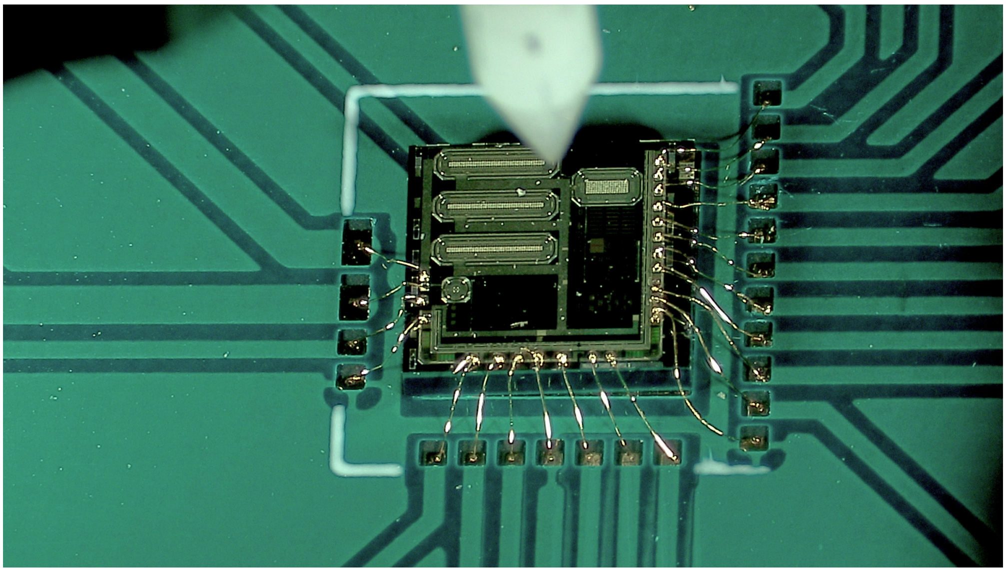


Figure 6.1: Physical bonding of the dimmer chip.

Just before starting to measure the chip, the global pandemic known as COVID-19 [33] caused the University Lab to close its doors until further notice [34] thus at the present, the only available measurements had to be done in a domestic setting with limited equipment. High Voltage measurements were not yet performed because of the lack of adequate equipment and for security reasons.

Measurement were performed with a Tektronix TDS 2014B [35] oscilloscope, while all the signals in this section were generated with a simple Siglent SDG1025 [36] generator.

Even though the ASIC was designed to work with a rectified sine wave signal, using a low voltage version provides certain inconveniences, the main one being that the waveform generator refers signals only to its own ground. Because they are later rectified, it is difficult to generate signals with respect to the ASIC ground, as necessary to test the Switches for different values of the duty cycle.

For this reason, DC, low voltage triangle and trapeze waveforms were also connected directly to VRC, as described in Section 6.1.

6.1 Setup

6.1.1 Low Voltage DC

Power Management System measurements (Section 6.2.1) were performed with the circuit configuration shown in Figure 6.2 and the components shown in Table 6.1.

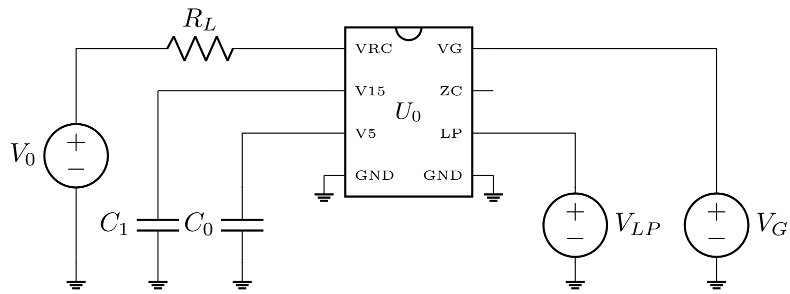


Figure 6.2: Measurement setup for a LV DC signal. V_{LP} and V_G voltage sources were controlled by physically connecting the ASIC terminals to V_5 or Gnd.

Name	Device Type	Value	Unit
V_0	Amplitude	20	V
R_L	Resistor	2	kΩ
C_0	Capacitor	100	µF
C_1	Capacitor	10	nF

Table 6.1: LV DC setup components.

6.1.2 Low Voltage Sine Waveform

Power Management System (Section 6.2.2), Switches (Section 6.3.1), and Zero Crossing Detector (Section 6.4.1) measurements were performed with the circuit shown in Figure 6.3 on the following page and the values shown in Table 6.2 on the next page.

6.1.3 Low Voltage Triangle Waveform

Power Management System (Section 6.2.3), and Switches (Section 6.3.3) measurements were performed with the circuit configuration shown in Figure 6.4 on page 86 and the components shown in Table 6.3 on the next page.

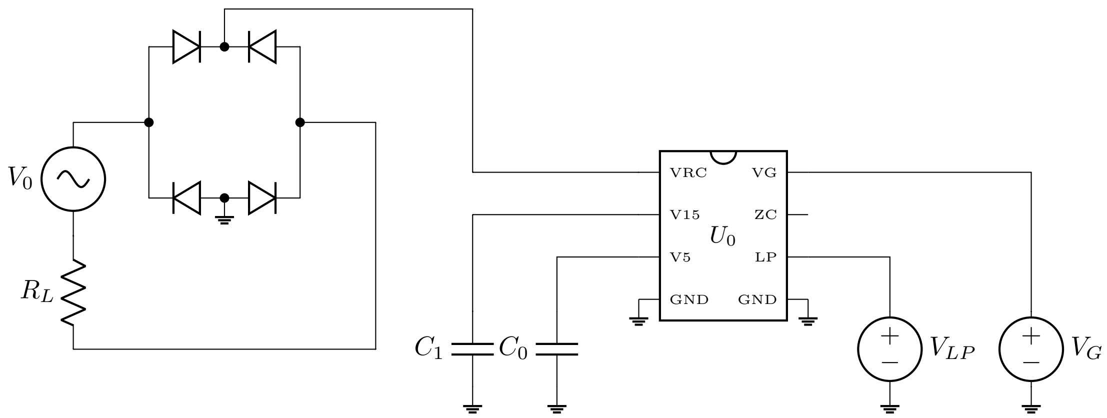


Figure 6.3: Measurement set up for a LV sine wave signal. For the diode bridge, the B40C3700–2200A [37] device was used. V_{LP} and V_G voltage sources were controlled by physically connecting the ASIC terminals to V_5 or Gnd.

Name	Device Type	Value	Unit
V_0	Amplitude	10	V
V_0	Frequency	50	Hz
R_L	Resistor	2	kΩ
C_0	Capacitor	100	µF
C_1	Capacitor	10	nF

Table 6.2: LV triangle wave signal setup components.

6.1.4 Low Voltage Trapeze Waveform

Power Management System (Section 6.2.4), and Switches (Section 6.3.2) measurements were performed with the circuit configuration shown in Figure 6.5 on the following page and the components shown in Table 6.4 on the next page.

Name	Device Type	Value	Unit
V_0	Amplitude	5	V
V_0	Offset	5	V
V_0	Frequency	100	Hz
R_L	Resistor	2	kΩ
C_0	Capacitor	100	µF
C_1	Capacitor	10	nF

Table 6.3: LV triangle wave signal setup components.

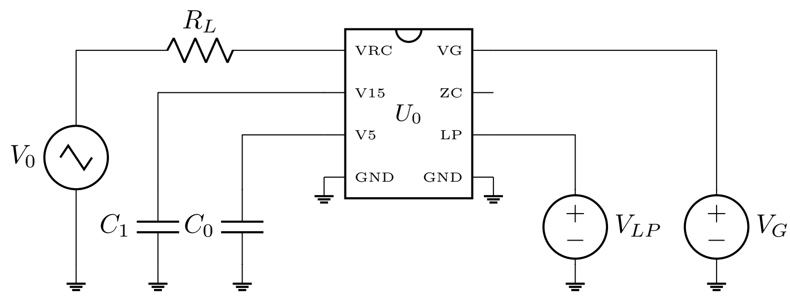


Figure 6.4: Measurement set up for a LV triangular wave signal. V_{LP} voltage source was controlled by physically connecting the ASIC terminals to V_5 or *Gnd*. V_G voltage source was controlled with the signal generator.

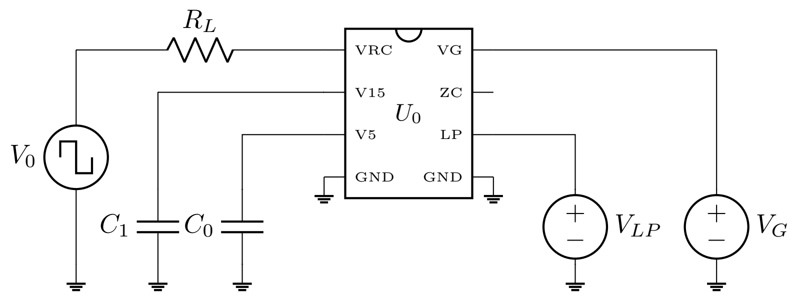


Figure 6.5: Measurement set up for a LV trapeze wave signal. V_{LP} voltage source was controlled by physically connecting the ASIC terminals to V_5 or *Gnd*. V_G voltage source was controlled with the signal generator.

Name	Device Type	Value	Unit
V_0	Amplitude	5	V
V_0	Offset	5	V
V_0	Frequency	100	Hz
R_L	Resistor	2	kΩ
C_0	Capacitor	100	µF
C_1	Capacitor	10	nF

Table 6.4: LV trapeze wave signal setup components.

6.2 Power Management System

6.2.1 Low Voltage DC

The Power Management System was tested with the setup from Section 6.1.1 by measuring the V_5 and V_{15} pins of the ASIC for high power mode with the switches in open state. The goal of this experiment was to attempt to have the V_5 and V_{15} sources reach their nominal 5 V and 15 V voltage levels.

The results are shown in Figure 6.6, and are summarized in Table 6.5. Finally, the average current consumption was calculated in Table 6.6 on the next page.

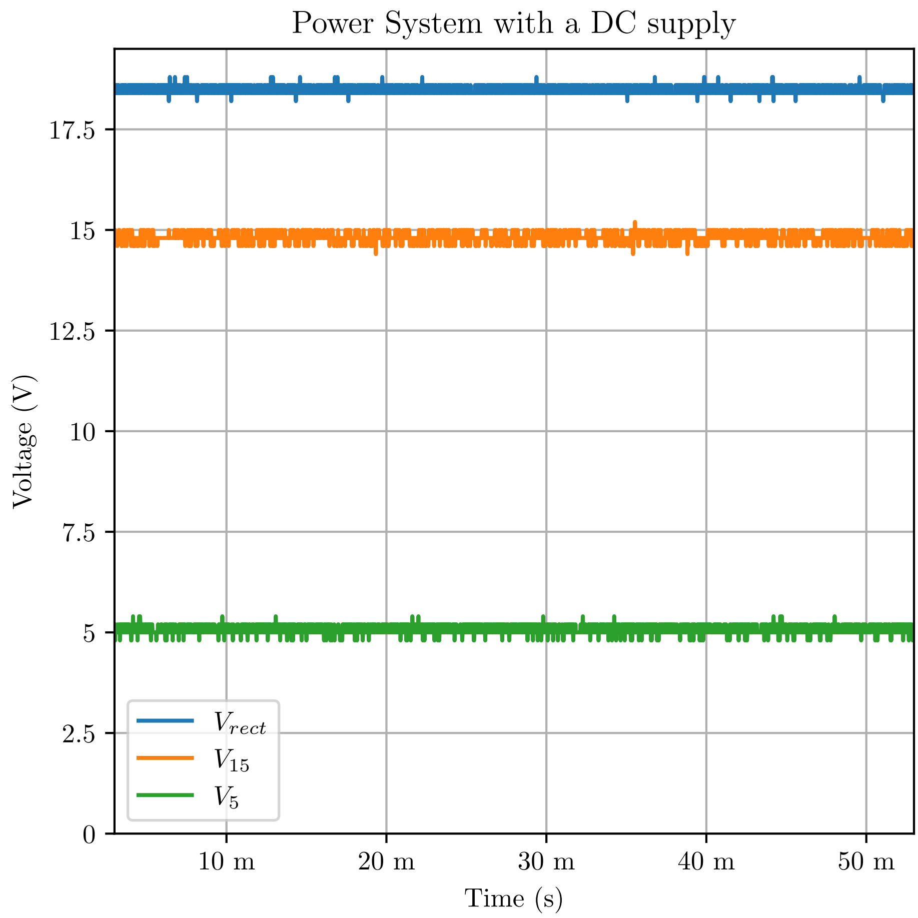


Figure 6.6: Power System measurement for a LV DC signal, in High Power Mode.

The DC voltage sources behave as expected and reach their nominal values. The current consumption for the ASIC in this mode is also within the specifications.

Mode	V_{rect}	V_{15}	V_5	Unit
High Power	18.47	14.81	5.06	V

Table 6.5: Average Voltage for the DC sources in the Power System measurement with a LV DC signal.

	Value	Unit
Average Current	650	µA
Simulated Average Current (TM)	300	µA
Simulated Average Current (WP)	1200	µA

Table 6.6: Average current consumed by the ASIC measurement with a LV DC signal.

6.2.2 Low Voltage Sine Waveform

The Power Management System was again tested with the setup from Section 6.1.2 by measuring the V_5 and V_{15} pins of the ASIC for both high and low power modes, with the switches in an open state.

The results are shown in Figures 6.7 on the following page and 6.8 on page 90 respectively, and are summarized in Table 6.7.

Mode	V_{rect}	V_{15}	V_5	Unit
Low Power	7.40	7.36	2.16	V
High Power	6.33	7.05	1.68	V

Table 6.7: Average Voltage for the DC sources in the Power System measurement with a LV sine wave signal.

As expected, the DC voltage sources cannot reach the nominal 5 V and 15 V with a maximum V_{rect} value of 10 V. Regardless of that, the V_5 and V_{15} pins effectively work as DC voltage sources.

It is worth noting that, counter intuitively, high power mode resulted in a lower average voltage. This can be explained by the fact that for this experiment the switches were fixed to an open state.

Lower currents associated with low power mode mean that parasitic and intrinsic capacitances from the switches and the diode bridge will take longer to discharge, and V_{rect} will not reach values close to zero as depicted in Figure 6.7 on the following page. High power mode will provide said capacitances with a more conductive path and hence V_{rect} can reach lower values, as shown in Figure 6.8 on page 90.

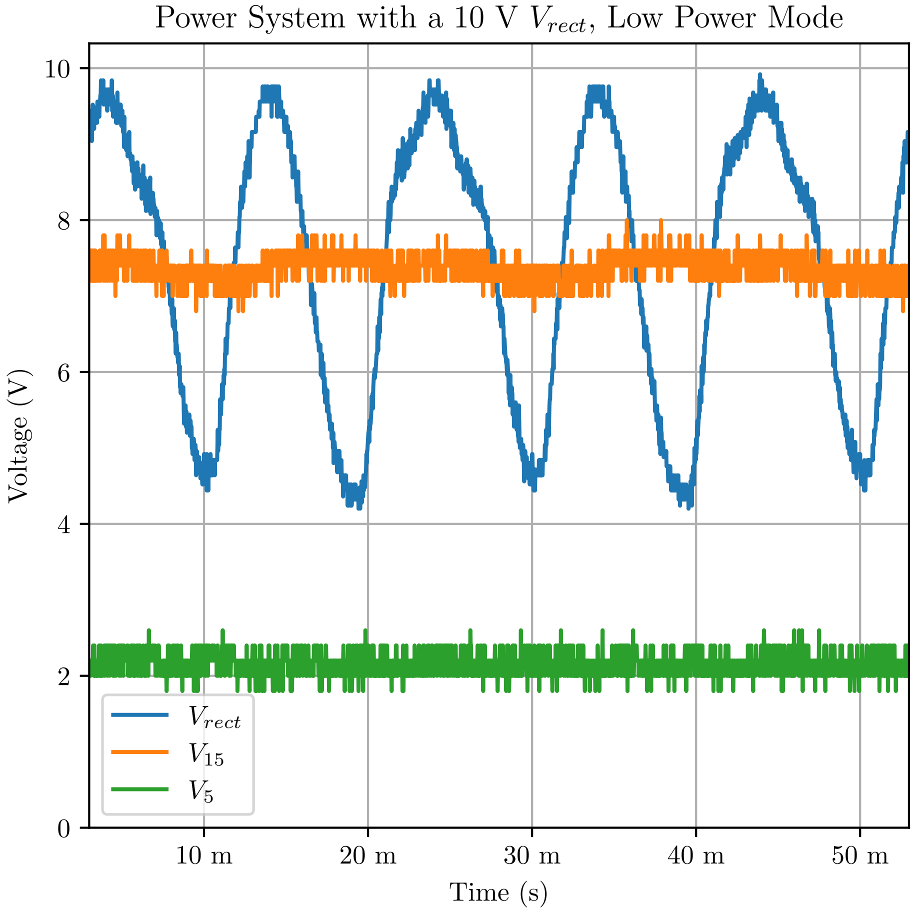


Figure 6.7: Power System measurement for a LV sine wave signal, in Low Power Mode.

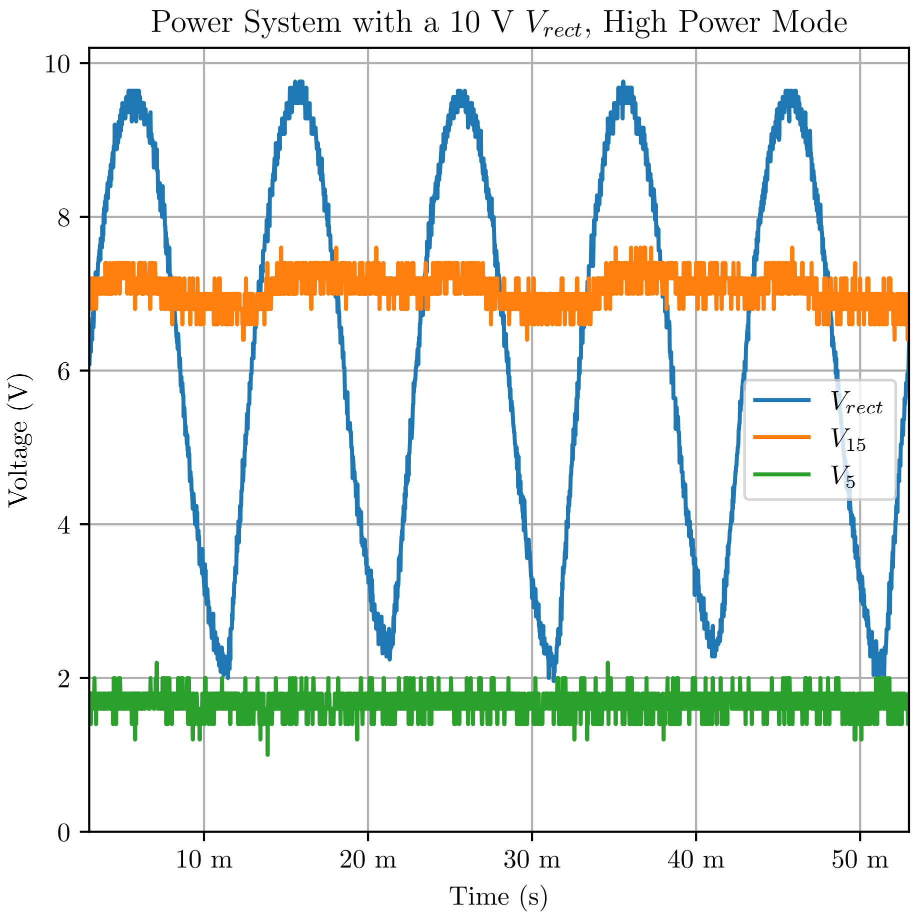


Figure 6.8: Power System measurement for a LV sine wave signal, in High Power Mode.

6.2.3 Low Voltage Triangle Waveform

The Power Management System was again tested with the setup from Section 6.1.3 by measuring the V_5 and V_{15} pins of the ASIC for both high and low power modes, with the switches in open state.

The results are shown in Figures 6.9 and 6.10 on the next page, and are summarized in Table 6.8.

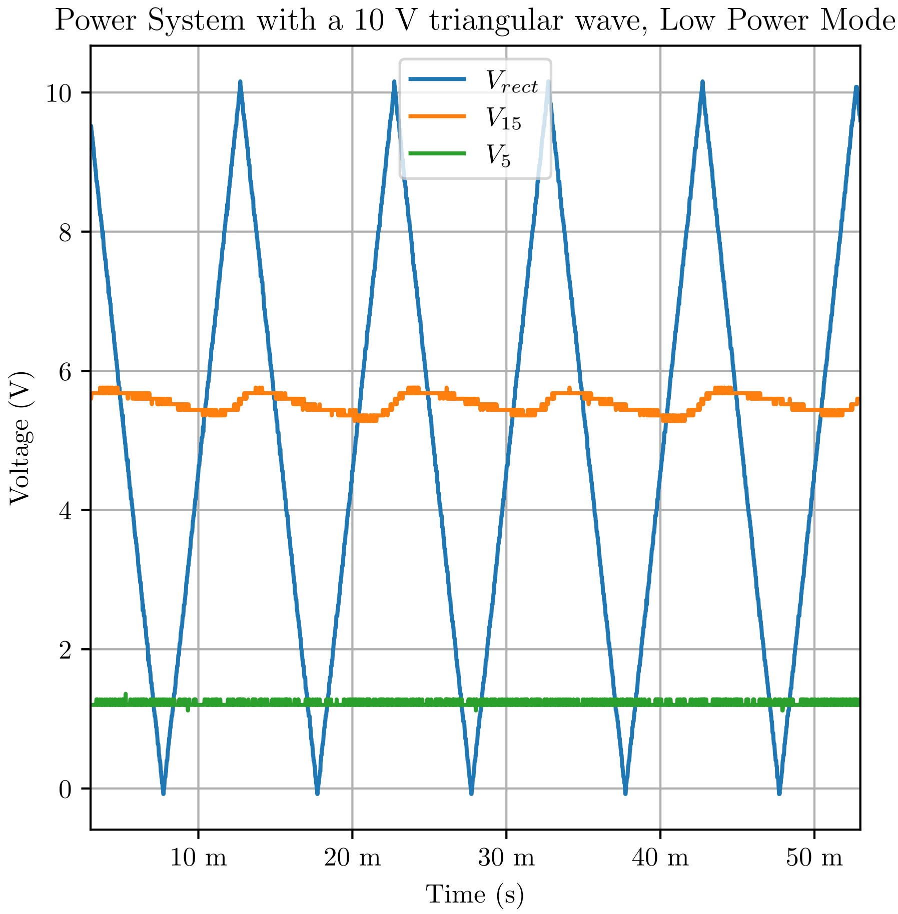


Figure 6.9: Power System measurement for a LV triangular wave signal, in Low Power Mode.

As expected, the DC voltage sources cannot reach the nominal 5 V and 15 V with a maximum V_{rect} value of 10 V. Regardless of that, the V_5 and V_{15} pins effectively function as DC voltage sources.

In this scenario, the 5 V DC source charges to about the same voltage regardless of operation mode, but the 15 V DC source has a significantly higher voltage in High Power Mode.

Note the 15 V power source charges with the rising edge of the triangular signal, and discharges with the falling edge.

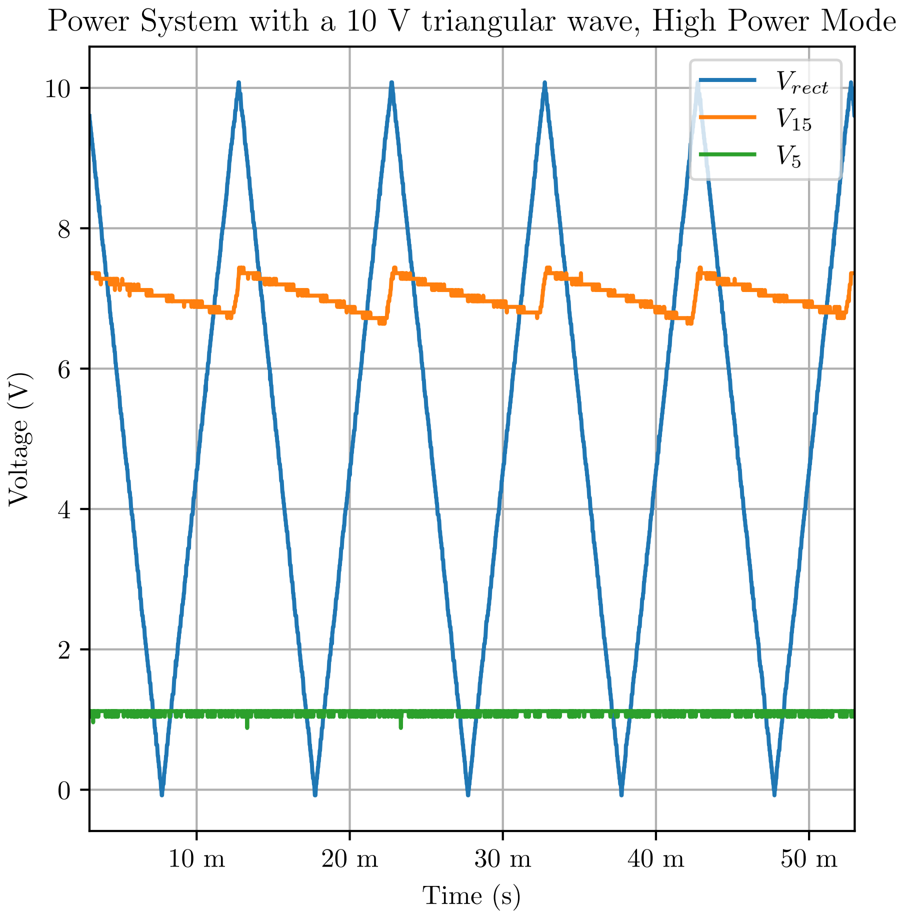


Figure 6.10: Power System measurement for a LV triangular wave signal, in High Power Mode.

Mode	V_{rect}	V_{15}	V_5	Unit
Low Power	5.01	5.53	1.22	V
High Power	5.01	7.05	1.11	V

Table 6.8: Average Voltage for the DC sources in the Power System measurement with a LV triangular wave signal.

6.2.4 Low Voltage Trapeze Waveform

The Power Management System was again tested with the setup from Section 6.1.4 by measuring the V_5 and V_{15} pins of the ASIC for both high and low power modes, with the switches in open state.

The results are shown in Figures 6.11 and 6.12 on the next page, and are summarized in Table 6.9.

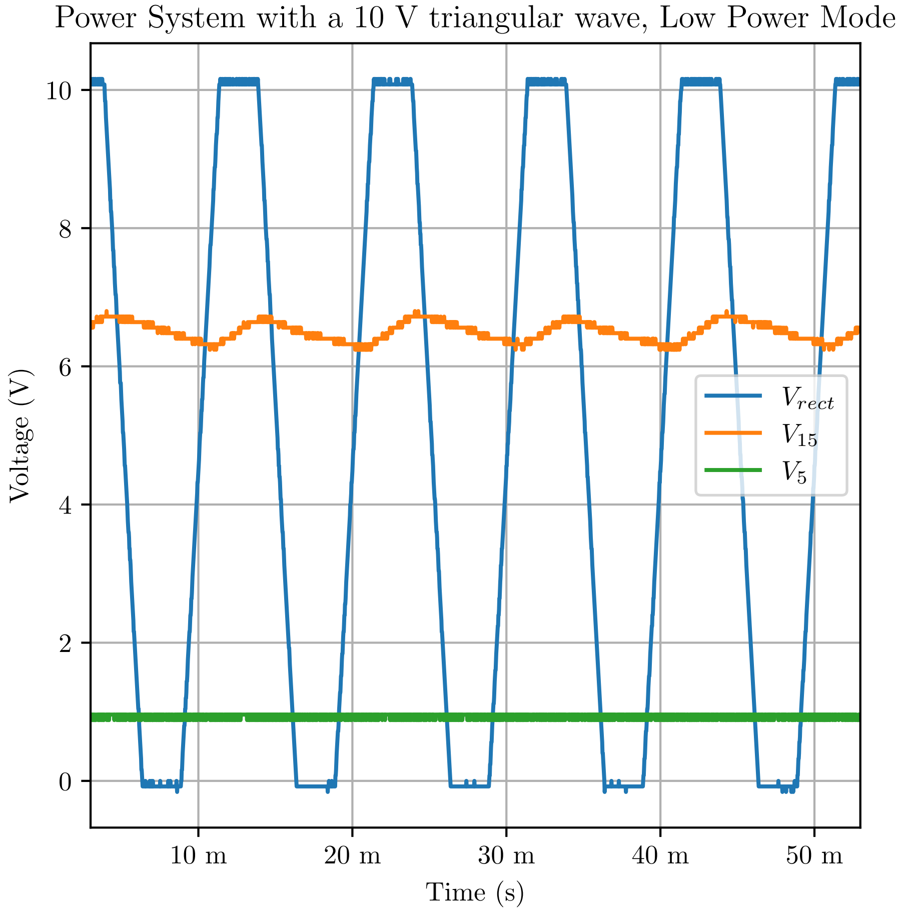


Figure 6.11: Power System measurement for a LV trapeze wave signal, in Low Power Mode.

As expected, the DC voltage sources cannot reach the nominal 5 V and 15 V with a maximum V_{rect} value of 10 V. Regardless of that, the V_5 and V_{15} pins effectively function as DC voltage sources.

In this scenario, both the 5 V and 15 V DC sources charge to significantly higher voltages in High Power Mode compared to Low Power Mode.

It can also be seen that the 5 V and 15 V power sources charge with the high level of the trapeze signal, and discharge with the low level.

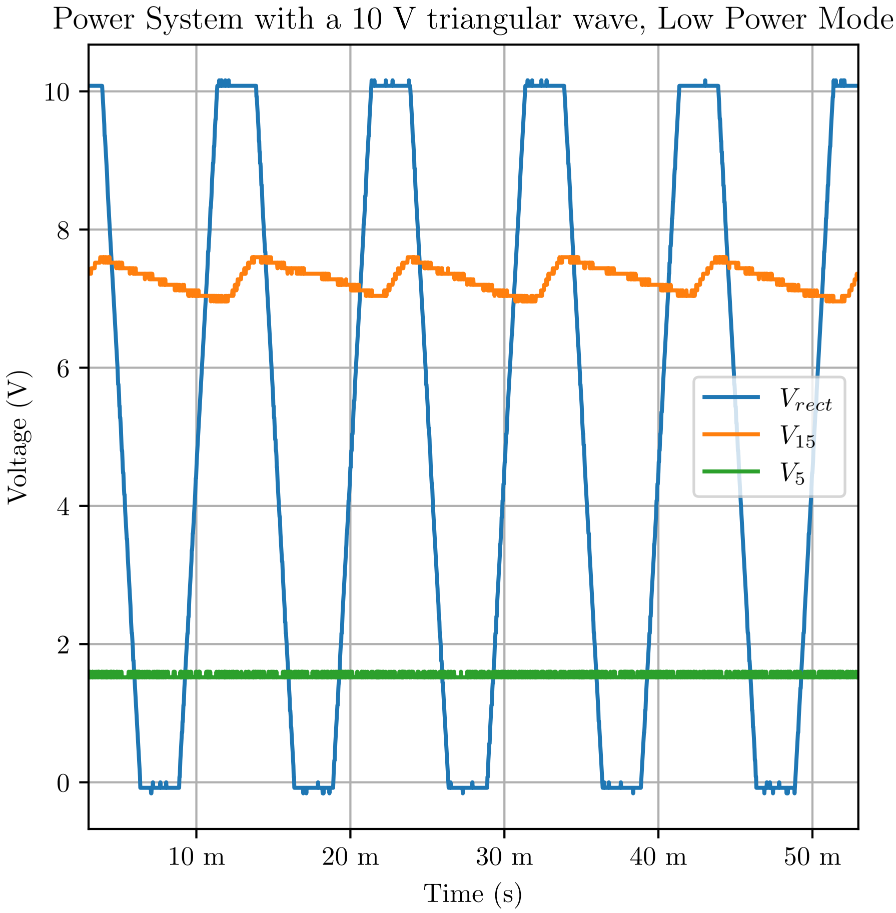


Figure 6.12: Power System measurement for a LV trapeze wave signal, in High Power Mode.

Mode	V_{rect}	V_{15}	V_5	Unit
Low Power	5.01	6.50	0.94	V
High Power	5.00	7.28	1.54	V

Table 6.9: Average Voltage for the DC sources in the Power System measurement with a LV trapeze wave signal.

6.3 Switches, Gate Driver

6.3.1 Low Voltage Sine Waveform

The Switches and Gate Driver behaviour was tested with the setup from Section 6.1.2 by connecting the VG pin to ground and V_5, as shown in Figure 6.13

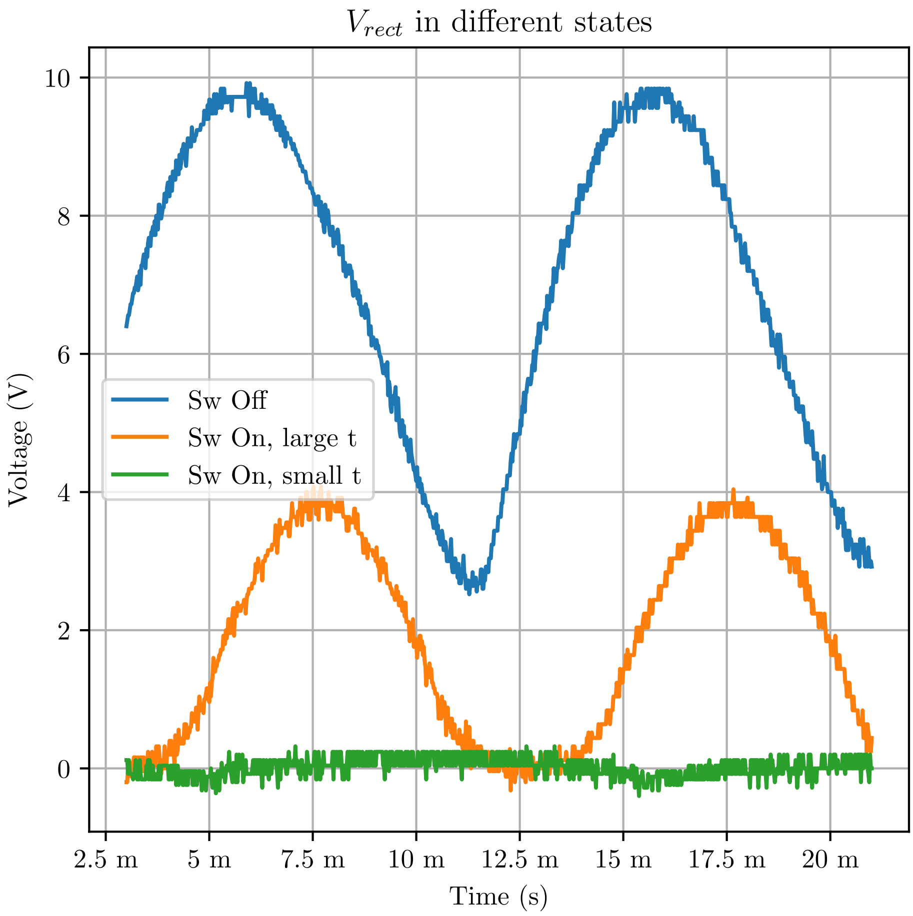


Figure 6.13: VRC measurement for a LV sine wave signal.

The Switches behave as expected in both open and closed states. It is worth noting that the behaviour of the closed Switches changes when the Switches remain closed for longer periods.

When the Switches are in a closed state and V_{rect} is near zero, the Power Management System cannot harvest charge. Eventually, the V_5 and V_{15} capacitors run out of charge and the Switches enter open state, until the capacitors are recharged and the cycle starts once again.

The curve shown in orange in Figure 6.13 shows an equilibrium point in which the Switches open just enough for the Power Management System to harvest the charge needed to stay at said level.

6.3.2 Low Voltage Trapeze Waveform

The Switches and Gate Driver behaviour was tested with the setup from Section 6.1.4 by connecting the VG pin to the signal generator to produce a square wave with different values of duty cycle, as shown in Figure 6.14

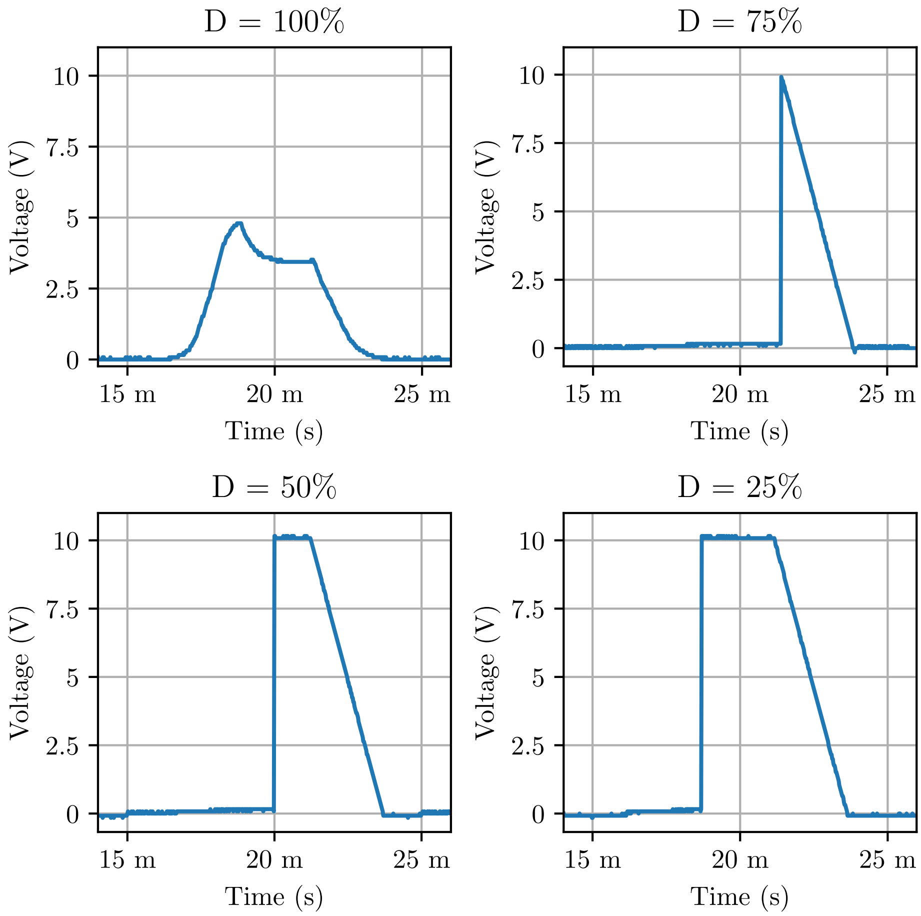


Figure 6.14: VRC measurement for a LV trapeze wave signal.

The ASIC behaves in this experiment as expected, with near 0 V when the Switches enter closed state, and near 10 V when the Switches enter open state.

Note in the $D = 100\,\%$ plot in Figure 6.14 is the equilibrium point in which the Switches open just enough for the Power Management System to harvest the charge needed to stay at said level when the Switches are closed for a long time.

6.3.3 Low Voltage Triangle Waveform

The Switches and Gate Driver behaviour was tested with the setup from Section 6.1.3 by connecting the VG pin to the signal generator to produce a square wave with different values of duty cycle, as shown in Figure 6.15 on the following page

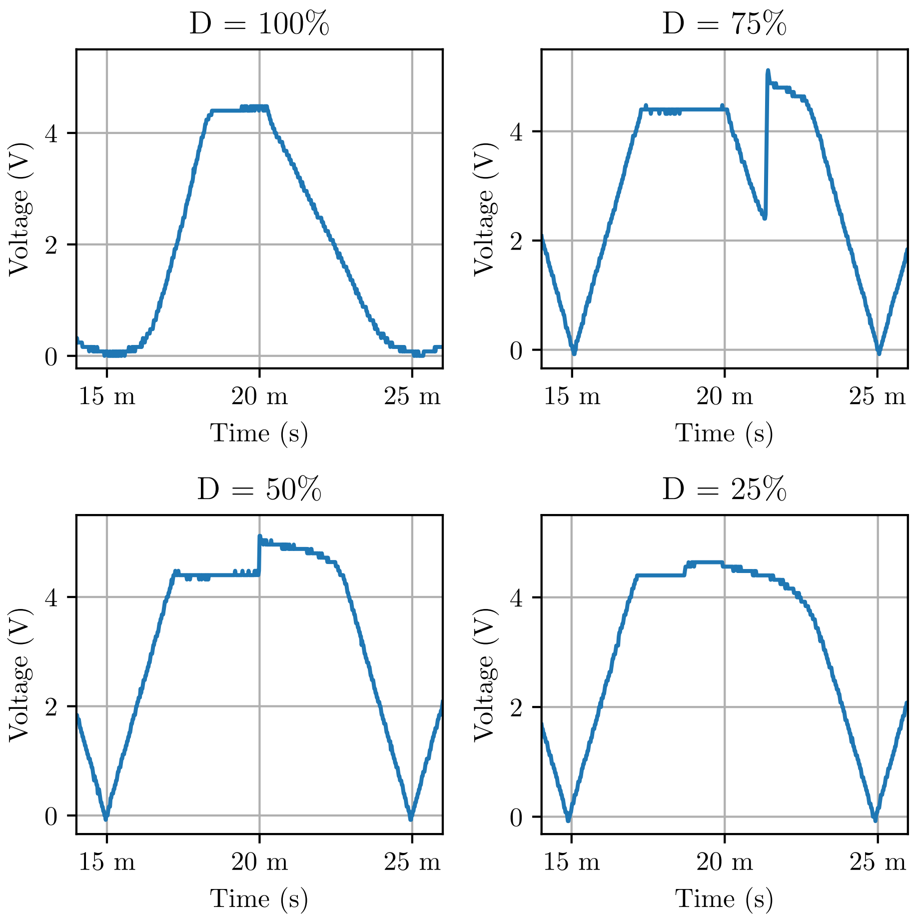


Figure 6.15: VRC measurement for a LV triangular wave signal.

Upon careful inspection, the VRC exhibits a jump in its value when the switches signal changes state.

However, the ASIC behaves in this experiment in a similar way as in Section 6.3.1. Having the Switches in a closed state means that the V_5 and V_{15} DC sources cannot harvest charge, causing their capacitors to discharge. Because having the Switches in closed state requires V_5 and V_{15}, the Switches will then enter open state until the capacitors charge and the cycle starts once again.

Figure 6.15 depicts the equilibrium point in which the Switches open just enough for the Power Management System to harvest the charge needed to stay at said level.

This is especially notorious with a triangular wave signal because it stays at its peak voltage for a relatively short time when compared to a sinusoid, giving a shorter period for the DC sources to charge.

6.4 Zero Crossing Detector

6.4.1 Low Voltage Sine Waveform

The Zero Crossing Detector was tested with the setup from Section 6.1.2 by measuring the ZCD pin of the ASIC for low power mode, with the switches in an open state. The results are shown in Figure 6.16.

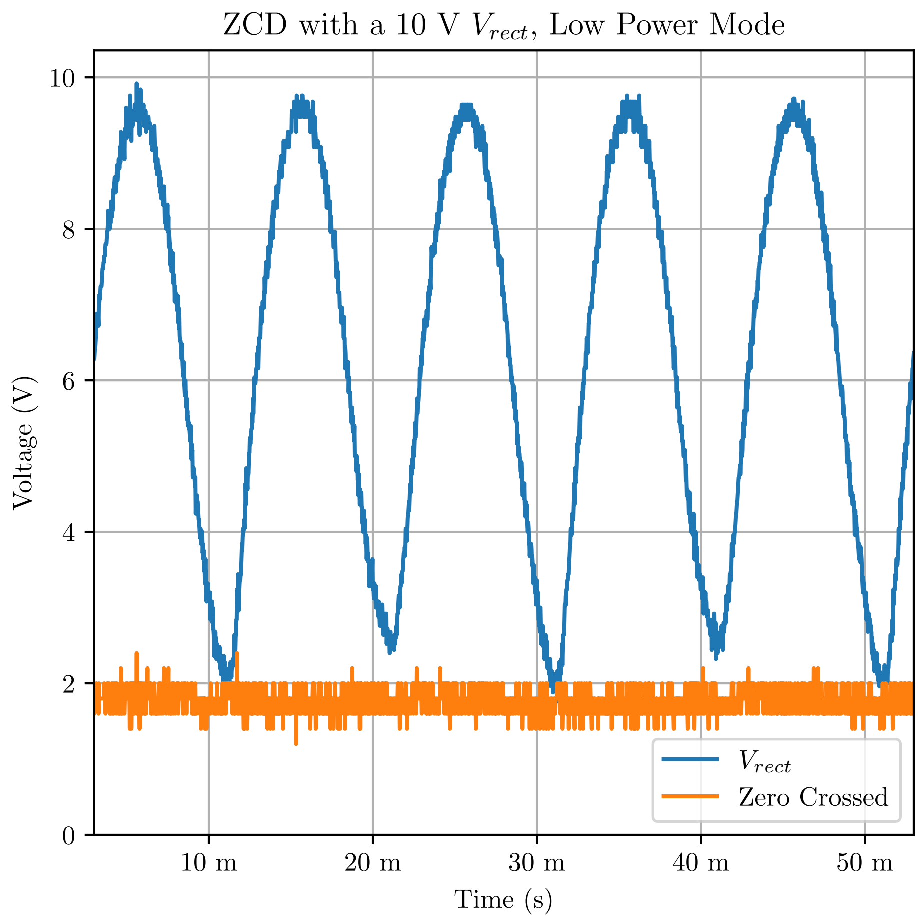


Figure 6.16: Zero Crossing Detector measurement for a LV sine wave signal.

The ZCD pin gave an output voltage equal to V_5 for the whole range of operation, which is not the expected behaviour. For V_{rect} values close to the 10 V peak, the output should be 0 V.

Chapter 7

Conclusions

In this work, an integrated dimmer composed of UHV switches, a gate driver, a power management system and a zero crossing detector was designed, simulated, and partially tested.

High voltage measurements have not yet been possible due to external constraints [33, 34], but the low-voltage functional validation of all sub blocks in the ASIC was successful, with the exception of the Zero Crossing Detector. High voltage measurements are necessary to validate the Zero Crossing Detector, because it is possible that the effective detection voltage threshold is higher than the low-voltage signals.

Table 7.1 shows a comparison between the target and final simulated specifications.

Measure		Target	Simulated	Unit	Comment	
Idle state power consumption	$\leq$	100	100	mW	at TM	✓
On state max. power consumption	$\leq$	4	0.857	W	worst case	✓
Max power percentage delivered	$\geq$	95	84.7	%		$\approx$
Max power delivered to the load	$\geq$	100	83.0	W		$\approx$
Total silicon area	$\leq$	10	10	mm^2		✓
Fully integrated		Yes	Almost	–		$\approx$

Table 7.1: Final design specifications, compared to target design specifications shown in Table 1.1 on page 15.

The specification for idle state power consumption could be met, and on state maximum power consumption is well below the target value. Because of the latter, larger values of duty cycle could be used to increase the power delivered to the load in future design stages.

The initial goal of designing a fully integrated phase cut dimmer could not be met, because of current density limitations of integrated UHV diodes, and the high value capacitors required by the power system.

If integrated diodes were used, it is estimated that both switches and diode configurations from Section 3.1 can be integrated in a die area of $12\,\mathrm{mm}^2$ at an estimated cost of 0.88 USD per unit, which is adequate according to BQN [11]. Thus, this dimmer shows potential for use in consumer applications.

7.1 Future Work

In future design stages, the following ideas could be worked on:

- Design a new version of the dimmer that includes the integrated UHV diodes. In a commercial product, this would simplify the installation process.
- Characterize and potentially redesign parts of the dimmer for different non-resistive loads, like capacitive and inductive loads.
- Implement the integrated control logic inside the dimmer to reduce current consumption and heat dissipation. This should allow for a smaller 5 V capacitor. Of the two options (leading and trailing edge), a trailing edge dimmer is the most interesting, because it provides a more significant design challenge and is generally better suited for modern low power lamps.
- Design a PCB that includes the dimmer and all the discrete components needed for it to function (diodes, capacitors, microcontroller). Measure and test the system as a whole.
- Attempt to use similar design architectures for other UHV applications, like motion sensor activated lights.
- Research alternative architectures for the Power Management System that are more robust to process variations. In the current implementation, current consumption in the WP corner is about three times larger than WS.

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Appendices

Appendix A

Load Measurements

Simulations in this project have all been done using a resistor to model the electrical behaviour of a load. However, it is necessary to test this hypothesis for commercially available lamps.

Measurements were performed with a commercially available two terminal dimmer, a small value sense resistor and four commercially available dimmable lamps, as shown in Figure A.1 and Table A.1.

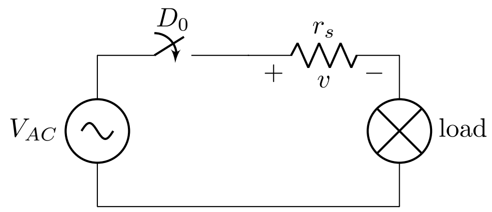

Figure A.1: Schematic for measuring current consumption from commercially available lamps. V_{AC} is the AC grid, D_0 is a commercial two terminal dimmer, r_s is a small resistor used to measure current, and *load* is the lamp of which the current response wants to be measured.

Model	Brand	P_{nom} (W)	Type
—	Philips [38]	100	Incandescent
LEDlustre 6–40W E27 P48 CL DT	Philips [38]	6	LED
LEDClassic 50W G120 E27 2000K GOLD D	Philips [38]	7	LED
IX1032	iXEC [39]	20	Dichroic LED

Table A.1: Commercially available lamps used to measure current with their respective model, brand, nominal power and type.

A resistor value of $10\,\Omega$ was chosen for r_s because it is small enough not to cause excessive voltage drop when operating with the 100 W lamp and large enough to be observable without special techniques for the low power lamps (6 W and 7 W).

A.1 Incandescent Lamp

Voltage and current measurements were performed for the circuit shown in Figure A.1 with the incandescent lamp from Table A.1. The results are shown in Figure A.2.

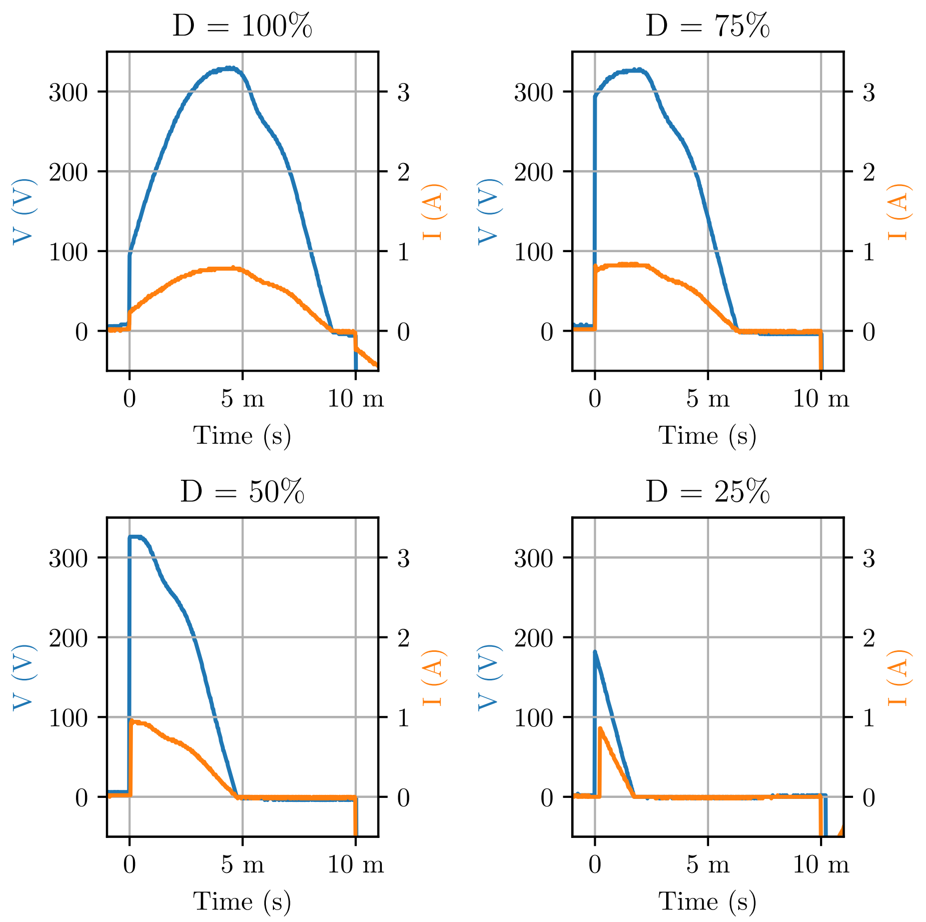

Figure A.2: Voltage and current for an incandescent lamp at different duty cycle (D) values.

As shown in Figure A.2, the incandescent lamp has an electrical response similar to that of a resistor. Thus, there is no appreciable distortion or phase shift in the AC current consumption with respect to the voltage.

Of all the lamps tested, the incandescent 100 W lamp provided the most intense light at full power and gave no flicker sensation.

A.2 LED Lamp 1

Voltage and current measurements were performed for the circuit shown in Figure A.1 on page 105 with the first LED lamp from Table A.1 on page 105. The results are shown in Figure A.3.

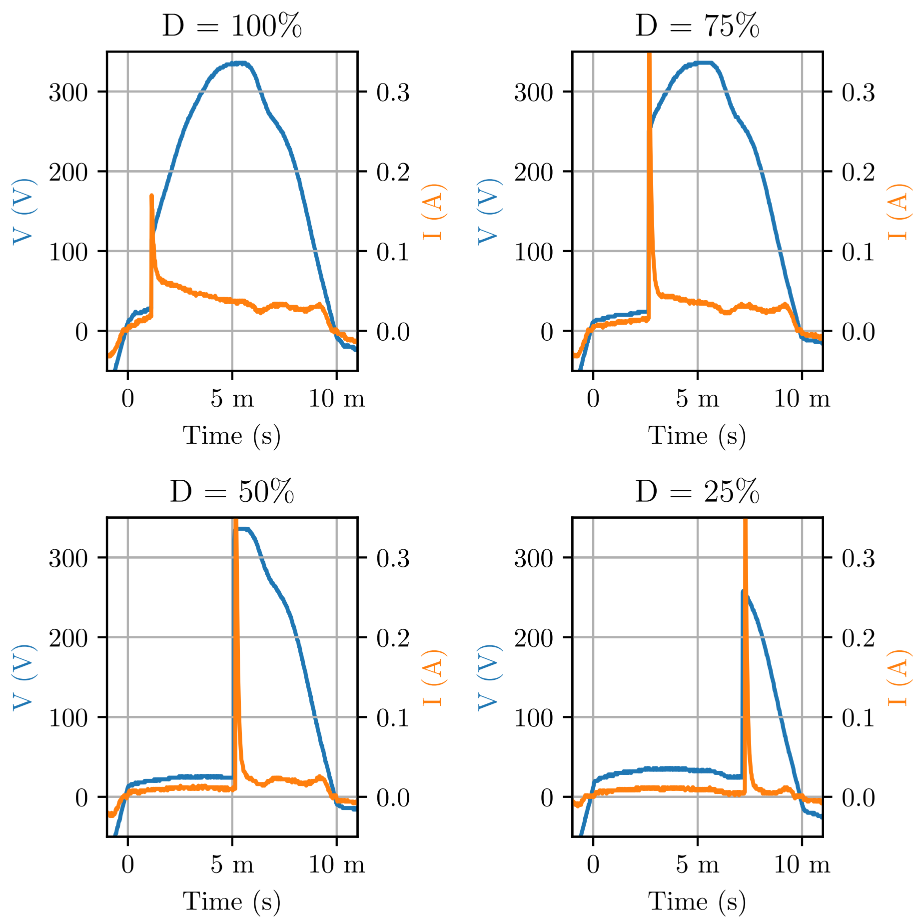

Figure A.3: Voltage and current for the first LED lamp at different duty cycle (D) values.

As shown in Figure A.3, the first LED lamp tested has a very non linear current consumption.

The first aspect that draws attention is a current peak when the dimmer begins conduction, that is more pronounced for smaller values of duty cycle. This behaviour is coherent with a capacitive load, that will have a current peak when a voltage step is applied. For the rest of the semi cycle, current consumption is relatively constant.

A closer inspection reveals that the residual voltage for the non conduction interval is much larger to that of the incandescent lamp shown in Figure A.2 on the previous page. This can also be attributed to residual charge in a capacitive load, similar to the first challenge described at the design of the Zero Crossing Detector from Section 3.4 on page 43.

Naked eye observation of this lamp gave a pleasant sensation for the range of operation of the dimmer with no flicker sensation.

A.3 LED Lamp 2

Voltage and current measurements were performed for the circuit shown in Figure A.1 on page 105 with the second LED lamp from Table A.1 on page 105. The results are shown in Figure A.4.

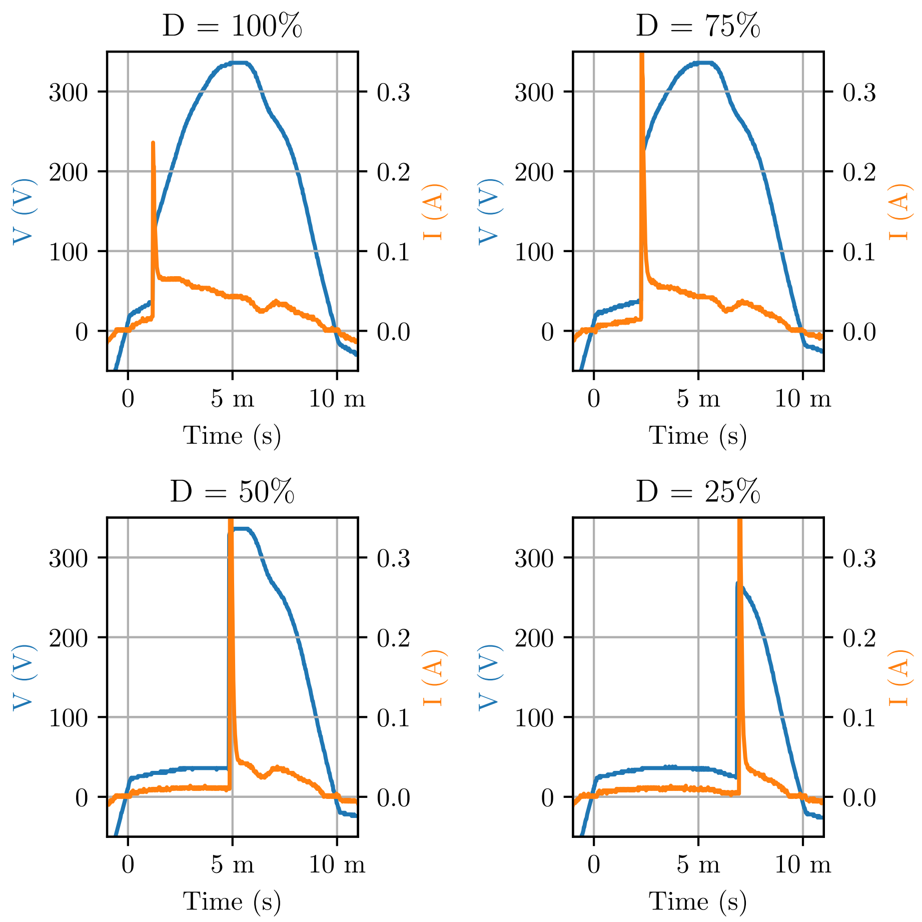

Figure A.4: Voltage and current for the second LED lamp at different duty cycle (D) values.

The electrical response of this lamp was extremely similar to that of Section A.2, and so is the analysis.

The main noticeable difference between the current consumption for this lamp and the one in Section A.2 is that the on state current consumption is no longer constant and has a downward slope that could be attributed to the discharge of a capacitor.

Naked eye observation of this lamp gave a pleasant sensation for the range of operation of the dimmer with no flicker sensation.

A.4 Dichroic LED Lamp

Voltage and current measurements were performed for the circuit shown in Figure A.1 on page 105 with the dichroic LED lamp from Table A.1 on page 105. The results are shown in Figure A.5.

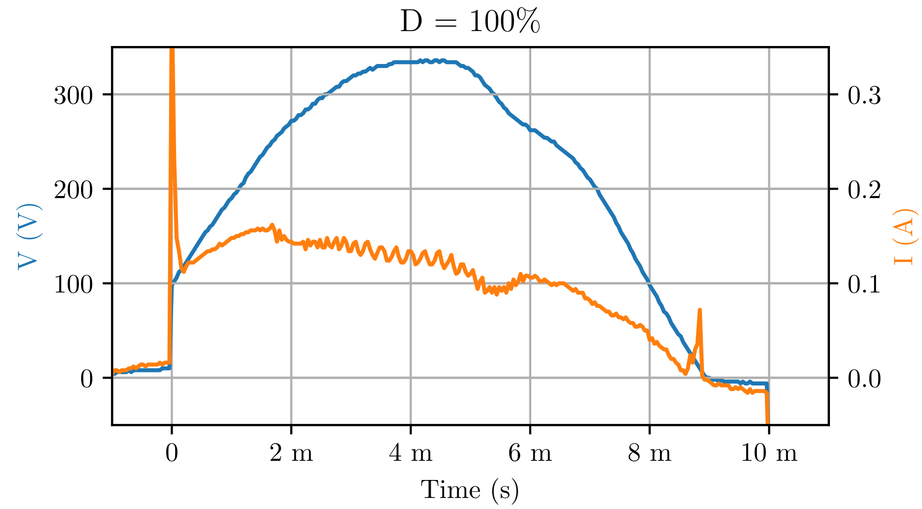

Figure A.5: Voltage and current for a dichroic LED lamp at different duty cycle (D) values.

Only one test could be done for this lamp at 100 % duty cycle, because the current peaks at the switching of the dimmer were in the order of several Ampere, and thus out of the point of operation for the dimmer and resistor r_s.

Attempting to operate this lamp at 75 % duty cycle for more than a few seconds caused visible damage to resistor r_s, and the commercial dimmer did not work as expected after the incident. Hence, no further experiments for this lamp were attempted.

Appendix B

Chip Bonding

The IC was manufactured and arrived without encapsulation, as shown in Figure B.1 on the next page.

For this reason, a PCB had to be designed to provide macroscopic terminals for connection with the chip. The schematic and layout of said PCB are shown in Figures B.2 on page 112 and B.3 on page 113 respectively.

The bonding diagram for the ASIC and the PCB is shown in Figure B.4.

A picture of the manufactured ASIC physically bonded to the PCB is shown in Figure 6.1 on page 83.

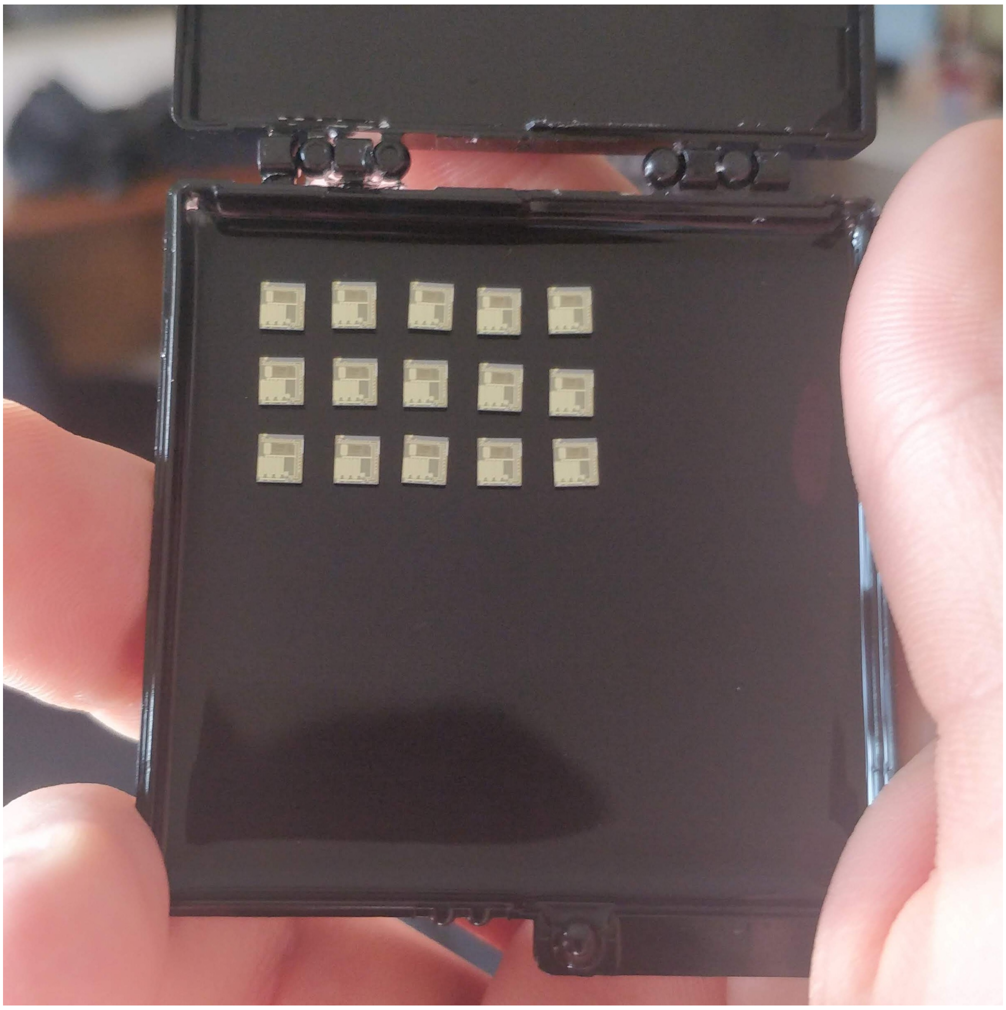

Figure B.1: Manufactured chip without encapsulation.

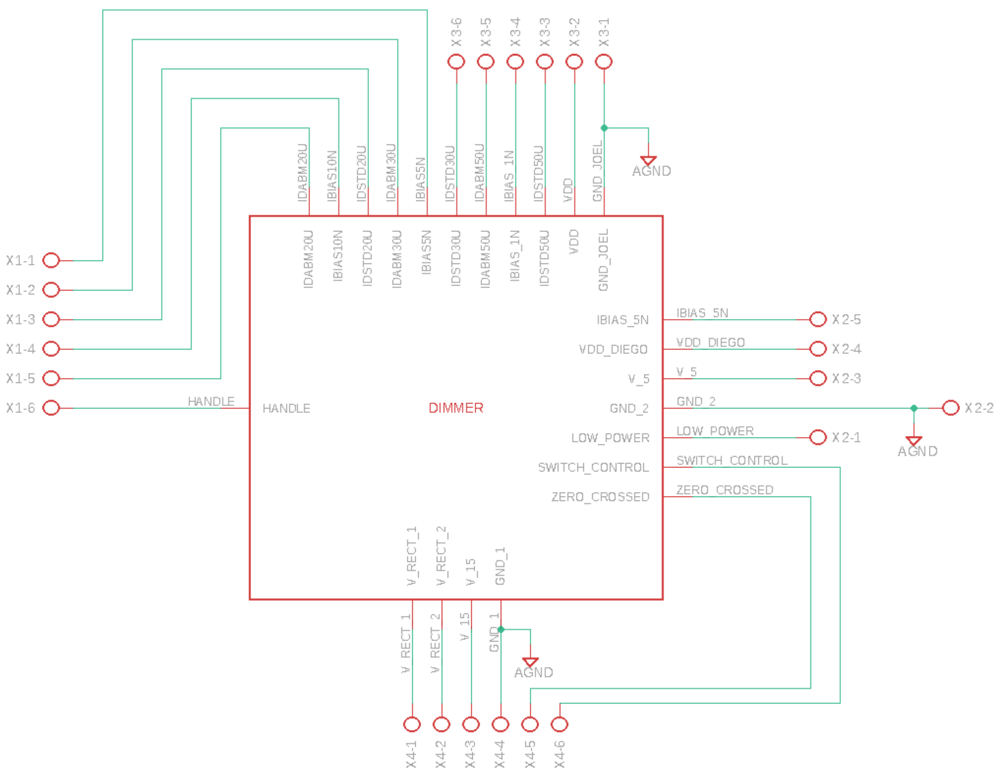

Figure B.2: Schematic of the PCB designed for bonding the dimmer ASIC.

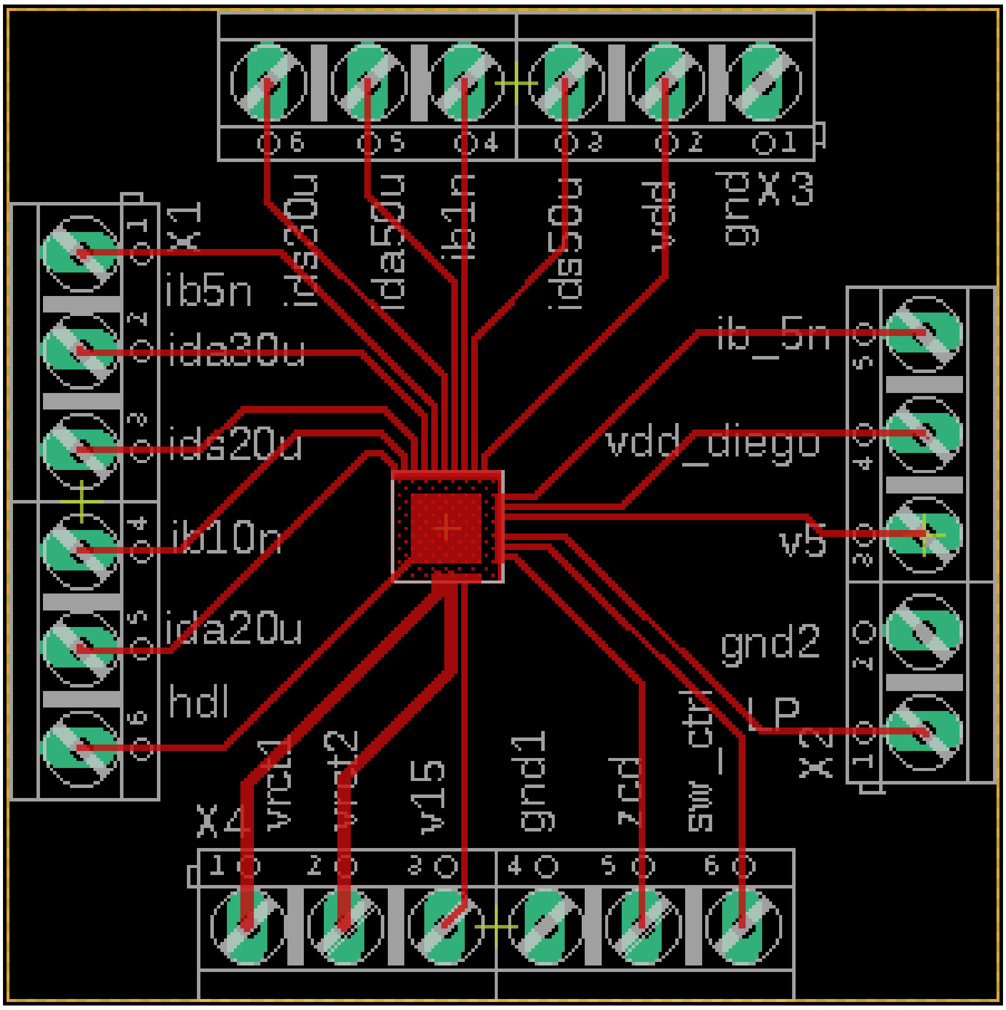

Figure B.3: Layout of the PCB designed for bonding the dimmer ASIC.

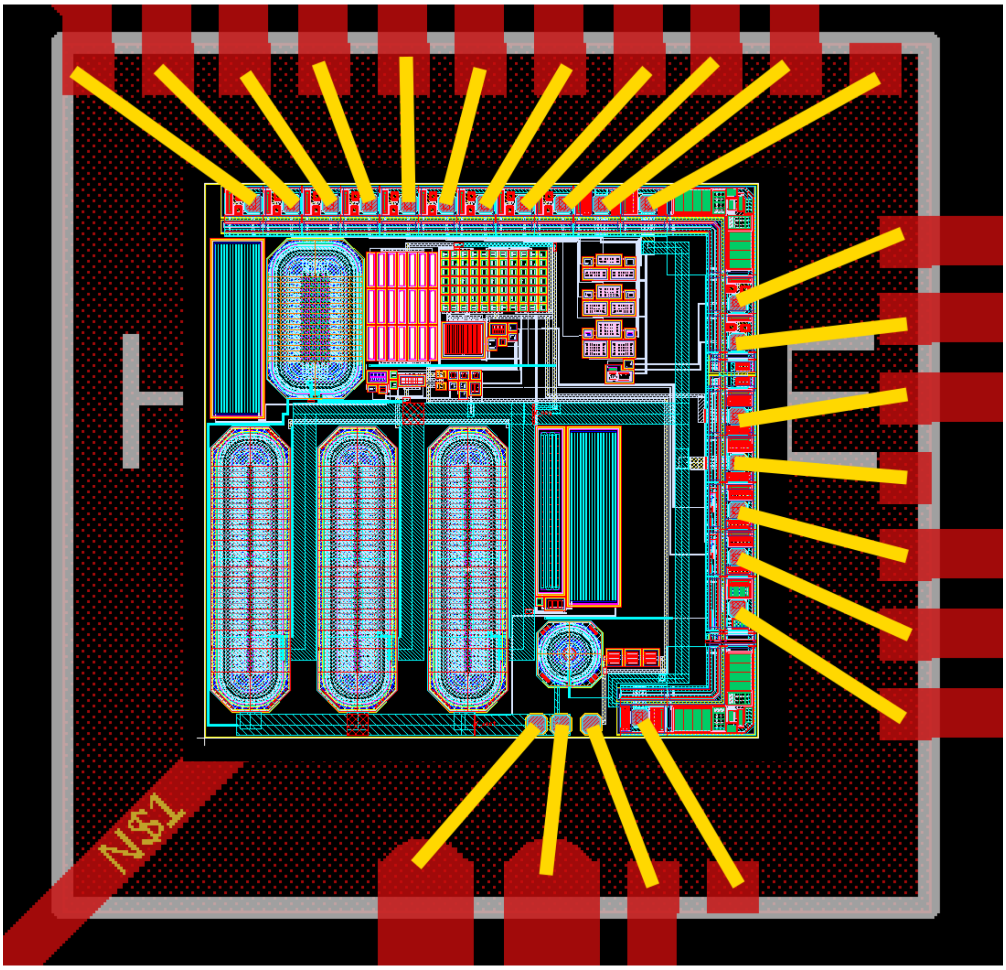

Figure B.4: Bonding diagram of the PCB from Figure B.3 and the ASIC from Figure B.1.