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Circuits and Systems for Inductive Power Transfer

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Investigar no es para genios formidables y países ricos. Es para seres humanos con ganas de descubrir y para países con problemas por resolver.

Gonzalo Perera

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Acknowledgments

First, I would like to thank my advisor, for trusting and supporting my work from the beginning.

After all this work, it is an honor to be evaluated by such a respectable committee. Therefore, I would like to especially thank Prof. Alfredo Arnaud, Prof. Alessandra Costanzo and Prof. Maysam Ghovanloo for their participation.

During the course of this work, I was fortunate enough to be welcomed into the Institut Supérieur D'électronique de Paris (ISEP) and the Génie Electrique et Electronique de Paris (GeePs). I would like to thanks to Prof. Amara Amara and Prof. Xun Zhang from ISEP and Prof. Lionel Pichon and his research group at GeePs. I have learned a lot by working in other research groups and I am very grateful for those opportunities.

I am also very thankful to all my colleagues, for their technical and emotional support during this last five years. I particularly wish to acknowledge Prof. Juan Pablo Oliver for valuable discussions and providing RFID tags and reader.

Last but not least, I would like to thanks to my family and friends. Although none of them will probably read this, I would never have completed this dissertation without their support, and I have been very lucky to have them always close to me during this journey.

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Abstract

Recently, the development of Wireless Power Transfer (WPT) systems has shown to be a key factor for improving the robustness, usability and autonomy of many mobile devices. The WPT link relaxes the trade-off between the battery size and the power availability, enabling highly innovative applications.

This thesis aims to develop novel techniques to increase efficiency and operating distance of inductive power transfer systems. We addressed the design of the inductive link and various circuits used in the receiver. Moreover, we performed a careful system-level analysis, taking into account the design of different blocks and their interaction. The analysis is oriented towards the development of low-power applications, such as Active Implantable Medical Device (AIMD) or Radio-Frequency Identification (RFID) systems.

Three main approaches were considered to increase efficiency and operating distance: 1) The use of additional resonant coils, placed between the transmitter and the receiver. 2) The receiver coil impedance matching. 3) The design of high-efficiency rectifiers and dc-dc converters.

The effect of the additional coils in the inductive link is usually studied without considering its influence on other parts of the WPT system. In this work, we theoretically analyzed and compared 2 and 3-coil links, showing the advantages of using the additional coil together with a matching network in the receiver. The effect of the additional coils in a closed-loop regulated system is also addressed, demonstrating that the feedback-loop design should consider the number of coils used in the link. Furthermore, the inclusion of one additional resonant coil in an actual half-duplex RFID system at 134.2 kHz is presented.

The maximum efficiency point can be achieved by adjusting the receiver coil load impedance in order to reach its optimum value. In inductive powering, this optimum impedance is often achieved by adapting the input impedance of a dc-dc converter in the receiver. A matching network can also be used for the same purpose, as have been analyzed in previous works. In this thesis, we propose a joint design using both, matching network and dc-dc converters, highlighting the benefits of using the combined approach.

A rectifier must be included in any WPT receiver. Usually, a dc-dc converter is included after the rectifier to adjust the output voltage or control the rectifier load impedance. The efficiency of both, rectifier and dc-dc converter, impacts not only the load power but also the receiver dissipation. In applications such as AIMDs, to get the most amount of power with low dissipation is crucial to fulfill safety requirements. We present the design of an active rectifier and a switched capac-

itor dc-dc converter. In low-power applications, the power consumption of any auxiliary block used in the circuit may decrease the efficiency due to its quiescent consumption. Therefore, we have carefully designed these auxiliary blocks, such as operational transconductance amplifiers and voltage comparators.

The main contributions of this thesis are:

- Deduction of simplified equations to compare 2 and 3-coil links with an optimized Matching Network (MN).
- Development of a 3-coil link half-duplex RFID 134.2 kHz system.
- Analysis of the influence of the titanium case in the inductive link of implantable medical devices.
- Development of a joint design flow which exploits the advantages of using both MNs and dc-dc converters in the receiver to achieve load impedance matching.
- Analysis of closed-loop postregulated systems, highlighting the effects that the additional coils, receiver resonance (series or parallel), and type of driver (voltage or current) used in the transmitter, have in the feedback control loop.
- Proposal of systematic analysis and design of charge recycling switches in step-up dc-dc converters.
- New architecture for low-power high slew-rate operational transconductance amplifier.
- Novel architecture for high-efficiency active rectifier.

The thesis is essentially based on the publications [1–9]. During the PhD program, other publications were generated [10–15] that are partially or non-included in the thesis. Additionally, some contributions presented in the text, are in process of publication.

Resumen

En los últimos años la transferencia inalámbrica de energía (WPT) ha cobrado especial atención, ya que logra aumentar la robustez, usabilidad y autonomía de los dispositivos móviles. Transferir energía inalámbricamente relaja el compromiso entre el tamaño de la batería y la disponibilidad de energía, permitiendo aplicaciones que de otro modo no serían posibles.

Esta tesis tiene como objetivo desarrollar técnicas novedosas para aumentar la eficiencia y la distancia de transmisión de sistemas de transferencia inalámbrica por acople inductivo (IPT). Se abordó el diseño del enlace inductivo y varios circuitos utilizados en el receptor de energía. Además, realizamos un cuidadoso análisis a nivel sistema, teniendo en cuenta el diseño conjunto de diferentes bloques. Todo el trabajo está orientado hacia el desarrollo de aplicaciones de bajo consumo, como dispositivos médicos implantables activos (AIMD) o sistemas de identificación por radio frecuencia (RFID).

Se consideraron principalmente tres enfoques para lograr mayor eficiencia y distancia: 1) El uso de bobinas resonantes adicionales, colocadas entre el transmisor y el receptor. 2) El uso de redes de adaptación de impedancia en el receptor. 3) El diseño de circuitos rectificadores y conversores dc-dc con alta eficiencia.

El efecto ocasionado por las bobinas resonantes adicionales en el enlace inductivo es usualmente abordado sin tener en cuenta su influencia en todas las partes del sistema. En este trabajo, analizamos teóricamente y comparamos sistemas de 2 y 3 bobinas, mostrando las ventajas que tiene la bobina adicional en conjunto con el uso de redes de adaptación. El efecto de dicha bobina, en sistemas de lazo cerrado fue también estudiado, demostrando que el diseño del lazo debe considerar el número de bobinas que utiliza el link. Se trabajó con un sistema real de RFID, analizando el uso de una bobina resonante en una aplicación práctica existente y de amplio uso en el Uruguay.

El punto de máxima eficiencia se puede alcanzar ajustando la impedancia vista por la bobina receptora hasta alcanzar su valor óptimo. En transferencia inductiva, este valor óptimo se ajusta en muchos casos mediante un conversor dc-dc de ganancia variable. Por otro lado, otros trabajos utilizan una red de adaptación para lograr el mismo objetivo. En esta tesis, proponemos un diseño combinando ambas técnicas, las redes de adaptación y los conversores dc-dc, resaltando los beneficios del uso conjunto de ambos métodos.

Circuitos de rectificación y de conversión de tension dc-dc, son usualmente incluidos en el receptor de energía. Mantener alta eficiencia en ambos circuitos es

fundamental, ya que ésta afecta no solo la potencia de salida sino también la disipación del receptor. En aplicaciones como AIMDs, aprovechar la mayor cantidad de energía recibida es crucial para reducir el calentamiento y respetar los limites de exposición. En esta tesis presentamos el diseño de un rectificador activo, y un conversor dc-dc a capacitores conmutados. En aplicaciones de bajo consumo, la potencia consumida por cualquier bloque auxiliar utilizado en el circuito, puede afectar la eficiencia considerablemente. Por lo tanto, hemos diseñado cuidadosamente estos bloques, como ser amplificadores de transconductancia y comparadores de tensión.

Las mayores contribuciones de la tesis son:

- La deducción de ecuaciones simplificadas que permiten comparar sistemas de 2 y 3 bobinas que utilizan redes de adaptación de impedancia.
- El desarrollo de un sistema de RFID de 3 bobinas.
- El análisis del efecto que tiene la caja de titanio, que habitualmente se usa para encapsular AIMDs, en el enlace inductivo.
- Un flujo de diseño que aprovecha las ventajas de utilizar redes de adaptación en conjunto con conversores dc-dc en el receptor para alcanzar la impedancia de carga óptima.
- El análisis de un sistema en lazo cerrado con postregulación, donde se muestran los efectos en el lazo de control generado por las bobinas adicionales utilizadas, el tipo de resonancia (serie o paralelo) del receptor, y el tipo de driver (voltaje o corriente) usado en el transmisor.
- El análisis de la implementación de las llaves en conversores dc-dc elevadores de tensión.
- El diseño de amplificadores de transconductancia de bajo consumo y alto slew-rate.
- Diseño de rectificadores activos de alta eficiencia.

La tesis se basa esencialmente en las publicaciones [1–9]. Durante el desarrollo del doctorado se generaron también las publicaciones [10–15] que fueron parcialmente incluidas o dejadas por fuera del presente documento. Adicionalmente, algunas de las contribuciones presentadas en el texto están en proceso de publicación.

Georgia Tech College of Engineering
School of Electrical and Computer Engineering

Nov. 12, 2018

PhD student: Pablo Perez-Nicoli, Universidad de la Republica, Uruguay

Faculty Advisor: Prof. Fernando Silveira, Universidad de la Republica, Uruguay

External Committee member: Prof. Maysam Ghovanloo, Georgia Institute of Technology

Date of oral exam: 21st November 2018

Re: Evaluation of the written PhD dissertation titled: Circuits and Systems for Inductive Power Transfer (06-10-2018)

To whom it may concern:

In his thesis, Mr. Perez-Nicoli provides a comprehensive theoretical analysis, thorough simulation construct, and step by step design and optimization procedure for the entire power flow pipeline, from the energy source to the load, in near-field wireless power transmission, with particular focus on the receiver side. He starts by laying out an in-depth foundation for theoretical analysis of two, three, and multi-coil inductive power transfer (IPT) links and compares the pros and cons of each power transfer strategy, while offering an excellent coverage and overview of the literature in this field. Then he applies this theoretical foundation and simulation toolset to the practical case of an existing radio-frequency identification (RFID) system for livestock tracking and identification, demonstrating his ability to apply a novel deign that would consider both power efficiency and data readout to extend the reading range by 2.7 times. Throughout the thesis, he also verifies his designs and optimizations with both simulation and well-constructed experimental setups. Then he focuses on the key building blocks on the receiver side of the IPT systems, and offers a few novel ideas for improving the performance of active rectifiers, DC-DC converters, and matching networks used in this application. In particular, he focuses on the optimal design of the matching networks and rectifiers, carefully evaluating effects of various design parameters, topologies, and circuit elements in the overall performance of the IPT link, all supported with simulation and measurement results. Finally he evaluates various closed-loop feedback configurations for regulating the output voltage and maintaining the high power transfer efficiency in response to various sources of perturbation, such as load or coil distance variations.

In terms of the importance of the work done, wireless power transmission is enjoying an explosive growth in a wide range of applications from RFID and implantable medical devices (IMD) to wireless charging of mobile devices and electric vehicles. Because of these applications, the number of publications in this field has grown exponentially in recent years, and Mr. Perez-Nicoli does an excellent job covering the state-of-the-art, understanding their advantages and limitations, and in a few cases offering his original contribution particularly in terms of in-depth analysis of various configurations, while considering the complex interaction between numerous design parameters, and offering a co-design strategy for two key building blocks of the IPT system, the matching network and AC-DC converter. Therefore, in terms of positioning of the topic in the frame

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of the current knowledge in the discipline, Mr. Perez-Nicoli has done an excellent job, and does not seem to have missed any important work over the last decade. I also consider the importance of the work accomplished and novel contributions commendable and sufficient for a PhD thesis.

In terms of the quality of the manuscript, despite the large amount of math and theoretical formulation, the writing is clear and appropriate as a Thesis. The order of the chapters is reasonable, considering the scope of the work that has been accomplished, and covers most of the IPT pipeline with suffient depth and details. There are some minor gramatical typos here and there, which can be easily corrected, and in certain sections, there is room for adding more explanation and clarification to help the reader better understand and follow the math. Mr. Perez-Nicoli does a good job in giving a short intro at the beginning of each section, laying out the topics to be discusses, and at the end of the section, summarizing the conclusions and the take home message. This practice helps with the reader understanding and contents of that section.

Finally based on the above summary, I consider the thesis acceptable without any reservation, and it can proceed to the next step. I look forward to seeing the final defense presentation. Please let me know if any additional details are required at this stage.

Sincerely,

Maysam Ghovanloo, PhD
Professor
Georgia Institute of Technology
School of Electrical and Computer Engineering

DIPARTIMENTO DI INGEGNERIA DELL'ENERGIA ELETTRICA
E DELL'INFORMAZIONE "GUGLIELMO MARCONI"

To the Graduate Academic Committee of the Universidad de la Republica,
Montevideo, URUGUAY
Report on the PhD Thesis of Pablo Perez-Nicoli
" Circuits and Systems for Inductive Power Transfer"

I have read Pablo Perez-Nicoli thesis document with the title "Circuits and Systems for Inductive Power Transfer".
The thesis is well written, and tackles both theoretical and experimental aspects with rigor, precision and method. The manuscript is very well organized and easy to be read. For any chapter, significant summary and conclusions are provided which facilitate the detailed reading of the manuscript.

The work proposed is significant, timely and can be exploited further in the field of medium (low) power miniaturized WPT links to enhance efficiency especially for those applications where the IPT links are non-fixed. The related work from others is widely considered.

The purpose of this work has been to analyse and provide all the elements necessary to accurately, and correctly, tackle the design of inductive wireless power transmission systems (for medium power transfer), exploring frequencies in the KHz and MHz region.

The modelling activity is described in detail and is well developed and rigorous. The candidate contribution is very relevant since it provides custom models and novel solution for all the main sub-systems of an IPT link. Particularly significant and interesting to the reader is the systematic approach to carry out a joint design of the matching network and of the ac-dc converters in the receiver to track the optimum loading conditions of the IPT.
It is important to emphasize that the work has not only studied the best configuration and topology to maximize the WPT transfer efficiency, but it has also provided solutions that are relevant to the problem of systems shielding once they operate.

All the themes addressed in this thesis are relevant and gives rigorous information to design the main building blocks for a IPT link implementation, which is now considered one of the most suitable choice for medium power miniaturized WPT system. This is definitely a very hot topic nowadays and thus I consider this work very well aligned with international interest in R&D.

A significant number of publications co-authored by the candidate also states the quality of his work results. In the following I briefly comment on each chapter and, eventually at the end I include some possible questions/remarks related to the chapter subject.

Chapter 1, contains the introduction where the motivation for the entire research work is developed. In particular, the main reference topologies of an inductive link are analytically described and the associated figure of merits for an IPT link are recalled and discussed.

In **Chapter 2**, the PhD candidate provides a detailed description of his modelling approach not only to account for the main coupling mechanism and the related network behaviour of a WPT system, but also to discuss deeply possible alternative configurations of a IPT link. The detail with which the candidate has considered all the parameters that contribute to the operation of a WPT link is remarkable, providing always good analytical solutions that are not only very fast to calculate but also allows the reader to obtain a clear explanation of all the effects that produce certain performances. These solutions are also compared with general full-wave simulations that can be considered as independent validation of the approach. The analytical discussion of an entire kHz RFID system is also Presented considering standard 2-coil system and the possible enhancements with a 3-coil solution.
Remark: it would be interesting to include a discussion about the effective implementation of the 3-coil solution and its impact on the portability of the RFID system.

Chapter 3 is dedicated to the exploration of different IPT receivers. The analytical study of each topology is remarkable as well as the critical discussion of the referenced available topologies from the state-of the-art. Then the chapter is dedicated to the development of an original architecture of a low-power high slew rate OTA used in the feedback of a dc-dc converter and its CMOS implementation is provided.
This is my favourite chapter, form which I learnt more being not directly related to my research activity. Noticeable is also the power budget provided with detailed computation of losses contributions.

In **Chapter 4** the candidate first discusses all the possible approaches to track the best operating point of the entire system, considering adjustable matching network and adjustable ac-dc converters available in the literature. The interesting solution to jointly design both.

Chapter 5 presents the full system implementation and the measurements results of the design procedure, considering the regulation techniques presented in the previous chapters. This concluding chapter also provides a general picture with a sort of design guidelines to be adopted in terms of number of coils and their connection type to reach the optimal operating conditions of the WPT link.

Chapter 6: the conclusions are consistent with the rest of the manuscript. They are very clear and state the main issues encountered during this multi-year research work. The different perspectives to continue on the subject are significant and clearly show that the area of WPT is worthy to be exploited in the next future taking advantages of both the technology advances and of the accurate modelling analyses, which the present thesis started from.

On the overall I judge the candidate activity very significant and well developed during the years and I consider he can definitely pass to the final examination. I will be happy to further discuss his work during the Viva voice examination.

Bologna, November 11th, 2018

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Chapter 1

Introduction

1.1 Wireless power transfer

In the past decade, we have witnessed a dramatic increase in the number of Mobile Devices (MDs) which are used in a wide range of applications and contexts. Batteries are often used as energy storage elements to power them. For applications such as wireless sensors, or Active Implantable Medical Device (AIMD) Fig. 1.1a, replacing the batteries may be impractical, expensive, risky, or in some cases impossible. To recharge these batteries the power can be harvested by the MDs itself, but in many applications this power may not be enough. Wireless Power Transfer (WPT) to these devices is a useful solution to recharge or even avoid using batteries. Furthermore, WPT is also used in several other applications as mentioned next.

The most popular application where WPT avoids using batteries is the Radio-Frequency Identification (RFID) Fig. 1.1b. Passive RFID tags that do not rely on a battery, are more robust, cheaper and have a longer life expectancy.

Nowadays, WPT is also used to power or recharge devices that have traditionally used a power cord such as mobile phones Fig. 1.1c, electric cars Fig. 1.1d and home appliances Fig. 1.1e. In these applications, WPT not only is a practical solution but also enables new possibilities like electric re-charging lanes among many others.

A number of studies have focused on long distance and large power WPT systems [16]. These systems will enable mind-bending applications like the proposed in [17], where solar power is collected in the space and transferred wirelessly to the earth Fig. 1.1f.

The main parameters that define the WPT link are: 1) The distance ($D_{TX\text{-}RX}$) between Transmitter (TX) and Receiver (RX), 2) The TX and RX sizes (A_{TX} and A_{RX} respectively), 3) The carrier frequency (f), 4) The power required at the load circuit (P_L) and 5) System efficiency (η_{TOT}).

Many trade-offs exist between these variables. Which variables are optimized depend on the application. For electric vehicles, there are no significant constraints on the TX and RX coils sizes, and the main focus is on achieving high power

(a) AIMDs (b) RFID (c) Phones

(d) Vehicles (e) Home appliances (f) Solar power satellite

Figure 1.1: Wireless power transfer applications. Pictures sources: Fig. 1.1a: www.impulse-dynamics.com, Fig. 1.1b: [5], Fig. 1.1c: www.apple.com, Fig. 1.1d: www.techradar.com, Fig. 1.1e: www.wirelesspowerconsortium.com, Fig. 1.1f: [16].

transmission. On the other hand, on AIMDs, the RX size is one of the main constraints, and the power levels are much lower than those for electric vehicles.

There are various classifications of WPT systems, but typically they are separated in near-field and far-field links. This classification is based on the physical working principle, in the far-field an electromagnetic wave transports the energy while near-field relies on magnetic or electric coupling.

To achieve long distances, in the range of meters, far-field is preferred because the beam can be pointed to the RX. This beam-based WPT systems can transfer large power (kilowatts) at large distances (tens of meters) with high efficiency ($>$ 50%) [16]. However, for short distances (tens of centimeters), higher efficiencies are achieved using near-field links [18] that does not require a line-of-sight operation.

The near-field can be sub-divided into magnetic or electric coupling. Most of the proposed electric coupling links are for short gap distances (millimeters) due to constraints on the developed voltage [19]. Inductive Power Transfer (IPT) is the most common and many works, transferring power in the centimeters range, have been presented. In addition, the magnetic field causes less adverse effects on the human body than the electric field, thus IPT is the best choice for biomedical systems [18].

A detailed description and comparison between different WPT mechanisms, including the ultrasound links, can be found in classical reference works, e.g., [20].

In this work, we focus on the design of IPT systems which are further introduced in Section 1.2.

1.2 Inductive power transfer systems

A general block diagram of an IPT system is presented in Fig. 1.2. A driver circuit generates an alternating current in the transmitter coil which induces an alternating voltage in the RX coil. The Receiver Circuit (RX-circuit) adapts this induced voltage to power the load (R_L).

In the driver, the voltage available in the dc power source could be adjusted before generating the alternating signal with the inverter. A Matching Network (MN) in the TX is sometimes used to optimize the inverter performance. The magnetic link can consist of one or more TX and one or more RX. Besides, additional resonant coils could be used to improve the system performance as it is explained later in this section. In the RX, a resonant capacitor or a general MN are used to adapt the load impedance of the RX coil. Then, the alternating voltage is rectified and adjusted with a dc-dc converter to power the load.

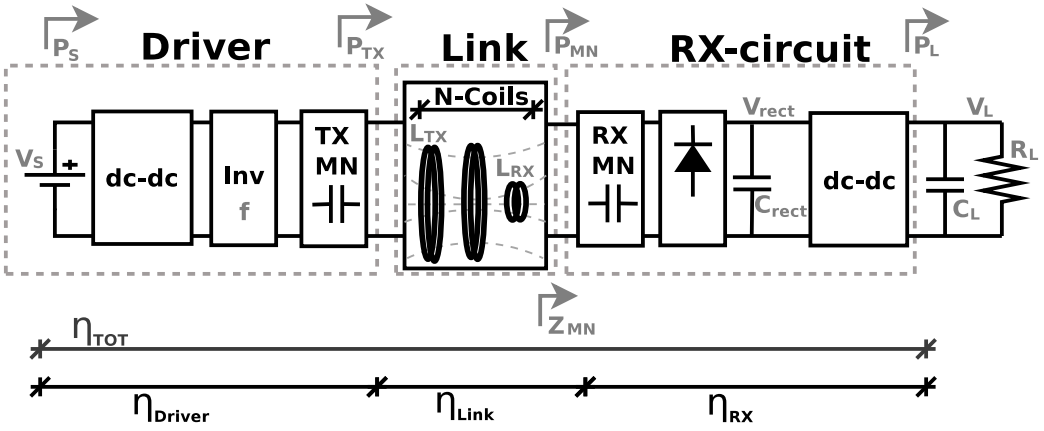

Figure 1.2: Block diagram of an Inductive Power Transfer (IPT) system. Acronyms: dc-dc: dc/dc converter, Inv: inverter (dc/ac converter), TX-MN: transmitter matching network, RX-MN: receiver matching network. L_{TX} and L_{RX} are the TX and RX selfinductances respectively. $\eta_{Driver} = P_{TX}/P_S$, $\eta_{Link} = P_{MN}/P_{TX}$ and $\eta_{RX} = P_L/P_{MN}$ are the driver, link and RX-circuit efficiencies respectively. $\eta_{TOT} = P_L/P_S$ is the total efficiency. V_S is the voltage of the power source in the TX and V_L is the load voltage in the RX. R_L models the load circuit. C_{rect} and C_L are filter capacitors. Most of these terms are widely used in the thesis, thus they are defined in the glossary.

The total system efficiency (η_{TOT}), is determined by the link efficiency (η_{Link}), the driver circuit efficiency (η_{Driver}) and the RX circuit efficiency (η_{RX}).

Recently, several papers have been published analyzing these links, trying to increase distance and efficiency. Those papers can be coarsely divided into three main categories. First, works focused on the coil design [5,21–24] to obtain high coil quality and coupling factors and increase the link efficiency [3,25]. Second, papers that propose improvements in the design of the circuits (e.g., rectifiers [6,26,27], dc-dc converters [28]). Third, studies that exploit the well-known result that there is an optimum value for Z_{MN} in Fig. 1.2 (that we will call $Z_{MN_{opt\text{-}\eta}}$) which maximizes link efficiency ($\eta_{Link} = P_{MN}/P_{TX}$). These studies propose methods to reach and automatically track this optimum $Z_{MN_{opt\text{-}\eta}}$ [29–35].

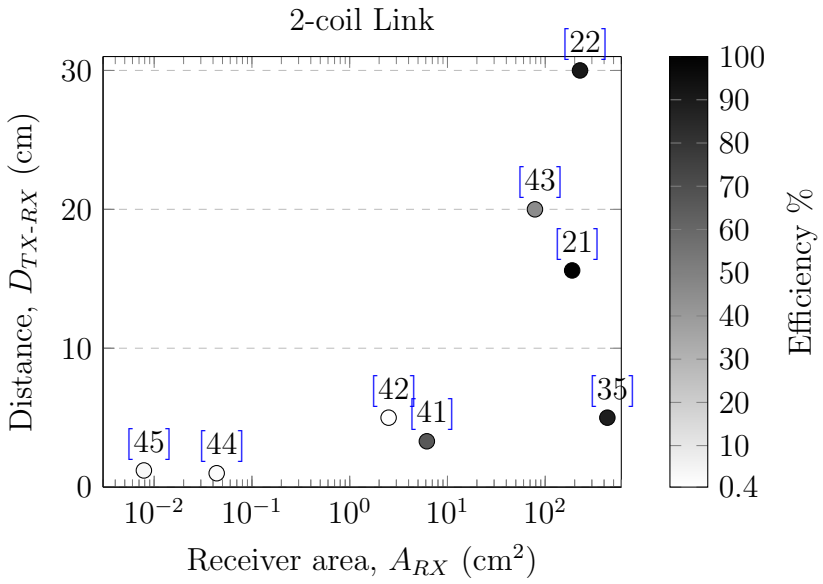

Figure 1.3: 2-coil Link state-of-the-art. Distance, RX coil size and Link efficiency η_{Link}. In this figure, we include some relevant papers of all the cited in the thesis that achieve the largest distances and efficiencies.

In systems where a large distance and small coil size are desired, the link efficiency is often the one that limits the total efficiency. The RX coil is usually the one with more size constraints, e.g., AIMDs. In Fig. 1.3 a summary of works' results is presented to highlight and quantify the difficulty in achieving long distance with small receivers. In the zone without works ($D > 10$ cm, $A_{RX} < 1$ cm^2), the efficiency would be even lower than 0.4% (the minimum presented in Fig. 1.3). To overcome this problem Kurs *et al.* [36] proposed a novel magnetic link using additional resonant coils which increases the efficiency for a given distance, or the power transfer distance for a given efficiency. Although [36] proposed a 4-coil link and it was used by many other works such as [37], the same principle can be used to build a 3-coil link [38, 39]. On the other hand, other works extend this idea to generate an N-relay coils link [40]. As shown in Fig. 1.4, systems with one additional coil (3-coil links) can achieve higher efficiencies at larger distances even with small RX coils, in comparison with the 2-coil link.

1.3 Motivation and goals

As discussed in previous sections, WPT is an important and fast-growing area. Particularly, IPT is already commercially used in various applications. However, many challenges still remain, which is indicated by the large number of papers that continue being published analyzing these links.

In this work, we address the design of IPT systems, with focus on the inductive link and RX circuits design.

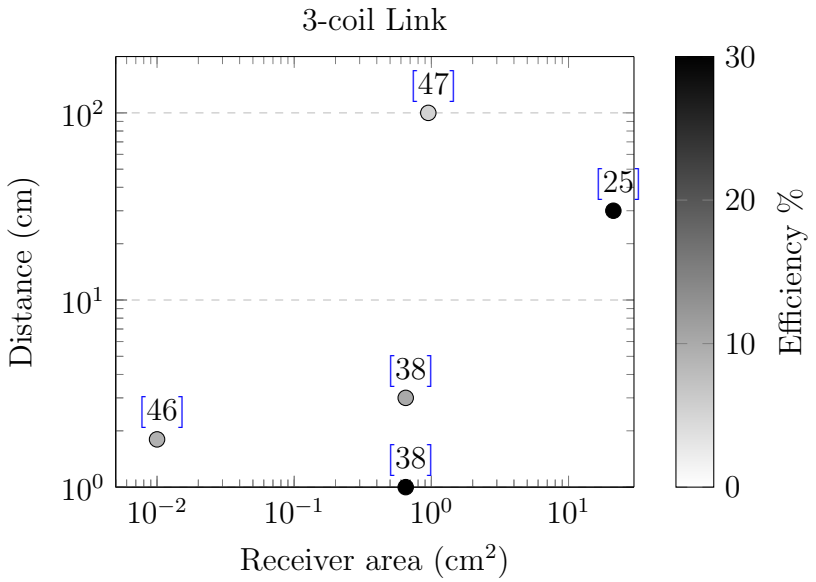

Figure 1.4: 3-coil Link state-of-the-art. Distance, RX coil size and Link efficiency η_{Link}. In this figure, we include some relevant papers of all the cited in the thesis that achieve the largest distances and efficiencies.

Most of the works in the state-of-the-art are concentrated on the design of a single block of the IPT system, without a system-level analysis that achieves a global optimum point. Therefore, we analyze the joint design of different parts of the system. Some of the research questions addressed are summarized next.

The use of additional resonant coils has been widely studied as mentioned in Section 1.2. However, it is not clear how do these coils affect the closed-loop methods of output voltage regulation and maximum efficiency point ($Z_{MN_{opt\text{-}\eta}}$) tracking. Additionally, these multiple-coil links are usually analyzed with a fixed, series or parallel, resonant capacitor in the RX [38]. On the other hand, improvements in the link efficiency by using a general Matching Network (MN) in 2-coil links (without additional coils) have been proved [42]. Thus, the comparison between the improvements of using additional resonant coils and the improvements obtained using MN is not straightforward. In [38], it is mentioned that the additional coils can play the role of an impedance-matching circuit. This opens the question if there is any advantage in adding an MN in a multiple coil system and whether it is possible to face the design of the MN and the additional resonant coils jointly.

The load transformation done by an MN is achieved in some works by means of a variable gain dc-dc converter that adapts its input resistance. Therefore, MN and dc-dc converters have been used in the literature to achieve the optimum impedance $Z_{MN_{opt\text{-}\eta}}$. However, a comparison between the MN and dc-dc converters is missing, and it is necessary to study if there is any advantage in using both methods together.

Summarizing, in this work, we not only address the design of particular blocks

as the rectifier and dc-dc converter, but also analyze and compare different approaches from a system-level design perspective. The thesis organization is presented in Section 1.4.

1.4 Thesis outline

The system block diagram of Fig. 1.5 represents a simplified outline of the thesis, which is described next.

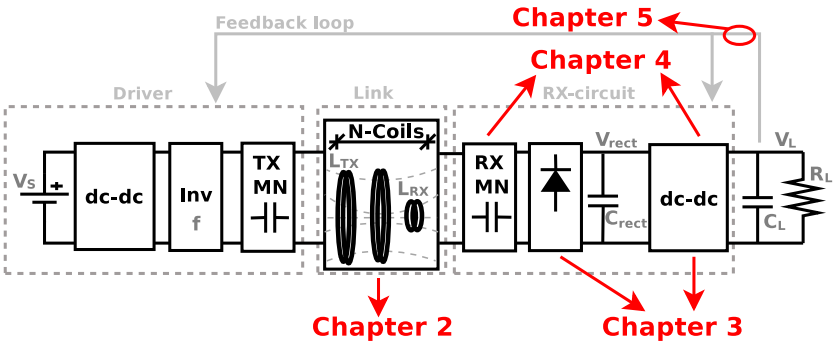

Figure 1.5: System diagram depicting the thesis organization.

First, in Chapter 2, the inductive link is studied. Section 2.1 introduces the circuit model and theoretical analysis, for 2- and 3-coil links. In this analysis, the 2- and 3-coil links are jointly considered with the use of MNs. Section 2.1 is an adapted version of [3]. The use of an additional resonant coil in an actual RFID low-frequency system is presented in Section 2.2, that is an adapted version of [5]. Finally, the presence of a foreign conductive object and its influence in the inductive link is addressed in Section 2.3, that is an adapted version of [9].

The design of the RX circuits, rectifier and dc-dc converter, is addressed in Chapter 3. First, in Section 3.1 the design of switched capacitor step-up dc-dc converters is discussed, especially focused on the switches design, this section is an adapted version of [1]. The architecture of a low-power high slew rate Operational Transconductance Amplifier (OTA), is presented in Section 3.2 that is an adapted version of [4]. This OTA was designed as a part of the feedback loop of a dc-dc converter. However, this low-power OTA can be used in various applications. Later, in Section 3.3 we address the design of an active rectifier, this section is an adapted version of [8]. Finally, in Section 3.4 a mixed block, which rectifies and increases the voltage is analyzed, this last section is an adapted version of [6].

The joint design of the MN, rectifier and dc-dc converter is presented in Chapter 4, the whole chapter is an adapted version of [7]. In this chapter, MNs and variable gain dc-dc converters are compared, and the advantages of a joint design are highlighted. A design flow for the joint design is presented and applied to a system that was fabricated and tested.

The analysis of the closed-loop control, to adjust the load voltage (V_L) and achieve optimum Z_{MN}, is discussed in Chapter 5. This chapter demonstrates how

the use of additional coils may affect the maximum efficiency point tracking. Measurements of a proof-of-concept system are presented highlighting the importance of taking into account the results of the chapter.

Finally, the main conclusions of this thesis are drawn in Chapter 6.

It is useful to note that the terms used throughout the thesis are defined in the glossary. Additionally, it is possible to click on these terms to see its definition in the glossary (e.g. η_{Link}).

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Chapter 2

Inductive link

In this chapter, we first analyze in Section 2.1 the inductive link circuit model, deducing analytical expressions for the efficiency in 2- and 3-coil links. The efficiency of each link is compared, and the improvements due to the additional coil in a system with an MN are quantified. Then, the inclusion of a third coil in an actual RFID system is presented in Section 2.2. Finally, the effect of a foreign metallic object in the link is addressed in Section 2.3.

2.1 Power transfer efficiency: circuit model and theoretical analysis in two and three-coil systems

The link efficiency (η_{Link}) can be calculated in a general N-relay coil system using Reflected Load Theory (RLT) [25]. This method consists in calculating each coil efficiency separately, then $\eta_{Link} = \prod_{i=1}^{N} \eta_i$. The efficiency of each coil is calculated as the ratio between the power transfer to the next one (or delivered to the load if $i = N$) and the total power dissipated in the coil. Section 2.1.1 presents this calculation for a 2-coil link while the 3-coil link is addressed in Section 2.1.2. In this work, for the sake of simplicity, the coupling between non-neighboring inductors has been considered negligible, as in [25].

2.1.1 2-coil link

Figure 2.1 shows the basic electrical model of a 2-coil WPT system. In this model no parasitic capacitors were considered, C_{TX} was added to achieve resonance in the TX. The mutual inductance between TX and RX is $M_{TX\text{-}RX}$. R_{TX} and R_{RX} are the parasitic ac resistance of each coil (L_{TX} and L_{RX} respectively), and R_L is the load resistor. Comparing with Fig. 1.2, we are modeling the rectifier and the followings blocks as an AC load resistance R_L, in order to simplify the link analysis. The driver output resistance could be considered embedded in R_{TX}. Figure 2.2 shows some MN alternatives. First, there are the commonly used parallel-resonator and series-resonator which are used only to achieve resonance at the desired frequency. In [43], using a 2-coil system, the authors proposed to apply a capacitive

series-parallel resonator which not only achieves resonance ($Im\{Z_{MN}\} = -w.L$) but also adjusts the real part of the load impedance ($Re\{Z_{MN}\}$) to improve efficiency. A limitation of a capacitive series-parallel MN is that not any value of $Re\{Z_{MN}\}$ can be achieved. In a more general case, any other MN topology could be used, and this is the case considered in this section.

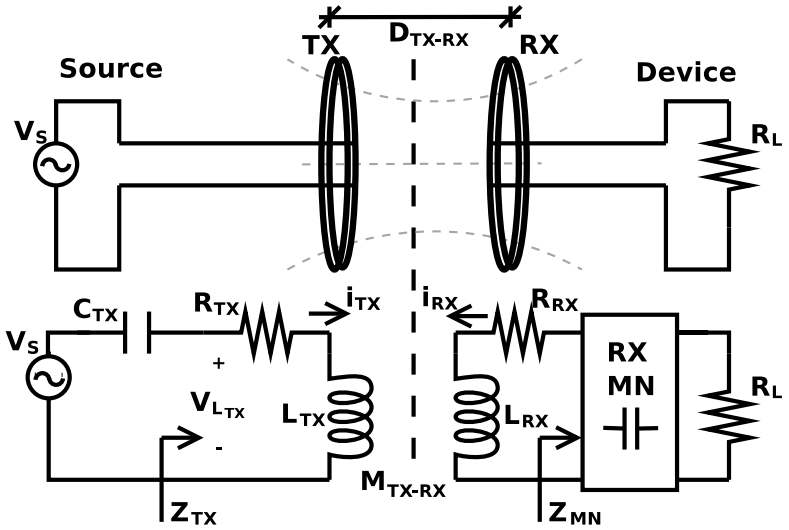


Figure 2.1: 2-coil model.

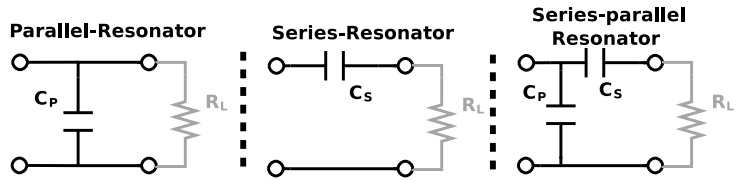


Figure 2.2: MNs used for WPT.

The efficiency of the receiver coil is the ratio between the power dissipated in Z_{MN} and the total power dissipated in R_{RX} and Z_{MN},

$$\eta_{L_{RX}} = \frac{Re\{Z_{MN}\}}{Re\{Z_{MN}\} + R_{RX}} = \frac{Q_{RX}}{Q_{RX} + Q_L} \tag{2.1}$$

where $Re\{Z_{MN}\}$ indicates the real part of Z_{MN}, $Q_{RX} = \frac{wL_{RX}}{R_{RX}}$ and

$$Q_L = \frac{wL_{RX}}{Re\{Z_{MN}\}}. \tag{2.2}$$

To determine the efficiency of the transmitter coil, Z_{TX} (see Fig. 2.1) needs to be computed.

$$\left.\begin{array}{l} V_{L_{TX}} = (R_{TX} + jwL_{TX})i_{TX} + jwM_{TX\text{-}RX}i_{RX} \\ i_{RX} = \frac{-i_{TX}jwM_{TX\text{-}RX}}{R_{RX}+jwL_{RX}+Z_{MN}} \end{array}\right\} \Longrightarrow$$
$$\Longrightarrow Z_{TX} = \frac{V_{L_{TX}}}{i_{TX}} = (R_{TX} + jwL_{TX}) + \frac{w^2 {M_{TX\text{-}RX}}^2}{R_{RX}+jwL_{RX}+Z_{MN}} \tag{2.3}$$

As can be seen, Z_{TX} is the series combination of R_{TX}, L_{TX} and a reflected impedance from the RX coil. The maximum TX coil efficiency is obtained when the real part of this reflected impedance is maximized. It occurs when w is such that the imaginary part of $jwL_{RX} + Z_{MN}$ is equal to zero. In this case, the reflected impedance is maximum and purely real, which is the advantage of having a resonant RX coil.

In the case of a resonant RX coil, an expression for this reflected resistance can be derived from (2.2) and (2.3),

$$\begin{aligned} R_{RX\text{-}TX_{ref}} = \frac{w^2 {k_{TX\text{-}RX}}^2 L_{TX} L_{RX}}{R_{RX} + Re\{Z_{MN}\}} &= \frac{{k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX} Q_L}{Q_L + Q_{RX}} R_{TX} \\ &= {k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L} R_{TX} \end{aligned} \tag{2.4}$$

where $Q_{TX} = wL_{TX}/R_{TX}$, Q_L is the one defined by (2.2), $k_{TX\text{-}RX}$ is the coupling factor between the coils ($k_{TX\text{-}RX} = M_{TX\text{-}RX}/\sqrt{L_{TX} L_{RX}}$) and $Q_{RX\text{-}L}$ was defined as

$$Q_{RX\text{-}L} = \frac{Q_{RX} Q_L}{Q_{RX} + Q_L} = \frac{wL_{RX}}{R_{RX} + Re\{Z_{MN}\}}. \tag{2.5}$$

The resulting TX coil efficiency can be calculated as the power dissipated in $R_{RX\text{-}TX_{ref}}$ (power transferred to the RX coil), divided the total power dissipated in R_{TX} and $R_{RX\text{-}TX_{ref}}$

$$\eta_{L_{TX}} = \frac{R_{RX\text{-}TX_{ref}}}{R_{RX\text{-}TX_{ref}} + R_{TX}} = \frac{{k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L}}{{k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L} + 1} \tag{2.6}$$

Finally, the total link efficiency ($\eta_{Link} = \eta_{L_{TX}} . \eta_{L_{RX}}$) is

$$\eta_{Link} = \frac{Q_{RX\text{-}L}}{Q_L} \frac{{k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L}}{{k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L} + 1}, \tag{2.7}$$

where the RX coil efficiency (2.1) was rewritten using the previously defined $Q_{RX\text{-}L}$, $\eta_{L_{RX}} = \frac{Q_{RX}}{Q_{RX} + Q_L} = \frac{Q_{RX\text{-}L}}{Q_L}$.

The reader should note that this expression (as the others presented in this section) is valid for any MN as the particular MN architecture was not considered.

If any of ${k_{TX\text{-}RX}}^2$, Q_{TX} or Q_{RX} increase, a better performance is obtained ($X_{TX\text{-}RX} = {k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX}$ should be as high as possible). On the other hand, Q_L has an optimum value which can be obtained from (2.7) as

$$Q_{L_{opt}} = \frac{Q_{RX}}{\sqrt{1 + {k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX}}}. \tag{2.8}$$

From (2.8) and the Q_L definition (2.2), the real part of the optimum Z_{MN} that maximizes η_{Link}

$$Re\{Z_{MN_{opt\text{-}\eta}}\} = R_{RX} \sqrt{1 + {k_{TX\text{-}RX}}^2 . Q_{TX} Q_{RX}}. \tag{2.9}$$

If the series MN shown in Fig. 2.2 is used, $Re\{Z_{MN}\} = R_L \Rightarrow Q_L = wL_{RX}/R_L$. In the case of the parallel MN Fig. 2.2, $Re\{Z_{MN}\} = (wL_{RX})^2/R_L \Rightarrow Q_L =$

$R_L/(wL_{RX})$ (assuming $R_L >> wL_{RX}$). Therefore, with a series or parallel MN, Q_L can only be modified by changing R_L. However, R_L is usually defined by the application. A capacitive series-parallel MN allows to modify Q_L for a given R_L, but within a limited range. Using a general MN, we are theoretically allowed to achieve any desirable Q_L (2.2), thus $Q_{L_{opt}}$ can be always set. The point where $Q_{L_{opt}}$ ($Z_{MN_{opt\text{-}\eta}}$) is achieved is referred to as Maximum Efficiency Point (MEP). In Section 4.1.1 the use of MN is further discussed.

Instead of adjusting Q_L with a MN to achieve $Q_{L_{opt}}$, another alternative is to modify $Q_{L_{opt}}$ by changing $k_{TX\text{-}RX}$ (see (2.8)) until $Q_{L_{opt}} = Q_L$. The $k_{TX\text{-}RX}$ can be adjusted modifying the coils' geometries. However, regarding the maximum achievable efficiency of the link, the higher $k_{TX\text{-}RX}$ is, the better. Therefore, $k_{TX\text{-}RX}$ is not considered as an adjustable parameter to achieve the MEP. Further discussion regarding this is presented in Section 2.1.3.1.

2.1.2 3-coil link

The 3-coil link circuit model is depicted in Fig. 2.3, where L_A and R_A are the additional coil self-inductance and parasitic resistance. The capacitors C_{TX}, C_A and C_{RX} were selected to assure that all the coils resonate at the same frequency.

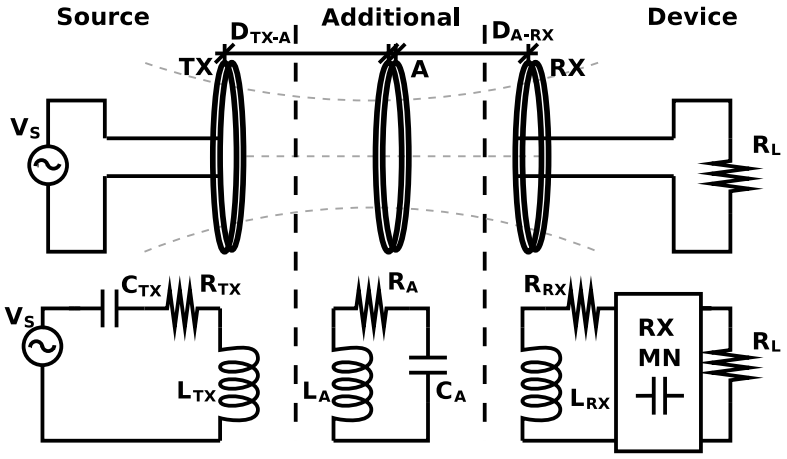


Figure 2.3: 3-coil model.

In this case, the RX efficiency is still given by (2.1). The additional coil efficiency (L_{η_A}) is calculated in the same way that the TX coil efficiency was calculated in Section 2.1.1. The reflected resistance in the additional coil from the RX is calculated analogously to (2.4), obtaining

$$\begin{aligned} R_{RX\text{-}A_{ref}} = \frac{w^2 k_{A\text{-}RX}^2 L_A L_{RX}}{R_{RX} + Re\{Z_{MN}\}} &= \frac{k_{A\text{-}RX}^2 Q_A Q_{RX} Q_L}{Q_L + Q_{RX}} R_A \\ &= k_{A\text{-}RX}^2 Q_A Q_{RX\text{-}L} R_A, \end{aligned} \tag{2.10}$$

where $k_{A\text{-}RX}$ is the coupling factor between the additional coil and the RX coil

and $Q_A = \frac{wL_A}{R_A}$. Therefore,

$$\eta_{L_A} = \frac{R_{RX\text{-}A_{ref}}}{R_{RX\text{-}A_{ref}} + R_A} = \frac{{k_{A\text{-}RX}}^2 Q_A Q_{RX\text{-}L}}{{k_{A\text{-}RX}}^2 Q_A Q_{RX\text{-}L} + 1}. \tag{2.11}$$

The reflected resistance from the additional coil to the TX coil ($R_{A\text{-}TX_{ref}}$) is computed neglecting the direct coupling between L_{TX} and L_{RX},

$$\begin{aligned} R_{A\text{-}TX_{ref}} =& \frac{w^2 {k_{TX\text{-}A}}^2 L_{TX} L_A}{R_{RX\text{-}A_{ref}} + R_A} \\ =& {k_{TX\text{-}A}}^2 Q_{TX} Q_A R_{TX} \frac{R_A}{{k_{A-RX}}^2 Q_A Q_{RX\text{-}L} R_A + R_A} \\ =& {k_{TX\text{-}A}}^2 Q_{TX} Q_A R_{TX} \frac{1}{{k_{A\text{-}RX}}^2 Q_A Q_{RX\text{-}L} + 1}. \end{aligned} \tag{2.12}$$

Finally the TX efficiency is

$$\eta_{L_{TX}} = \frac{R_{A\text{-}TX_{ref}}}{R_{A\text{-}TX_{ref}} + R_{TX}} = \frac{{k_{TX\text{-}A}}^2 Q_{TX} Q_A}{{k_{TX\text{-}A}}^2 Q_{TX} Q_A + {k_{A\text{-}RX}}^2 Q_A Q_{RX\text{-}L} + 1}. \tag{2.13}$$

And the total link efficiency ($\eta_{Link} = \eta_{L_{TX}} \eta_{L_A} \eta_{L_{RX}}$) is

$$\eta_{Link} = \frac{Q_{RX\text{-}L}}{Q_L} \frac{{k_{A\text{-}RX}}^2 Q_A Q_{RX\text{-}L}}{{k_{A\text{-}RX}}^2 Q_A Q_{RX\text{-}L} + 1} \frac{{k_{TX\text{-}A}}^2 Q_{TX} Q_A}{{k_{TX\text{-}A}}^2 Q_{TX} Q_A + {k_{A\text{-}RX}}^2 Q_A Q_{RX\text{-}L} + 1}. \tag{2.14}$$

$\eta_{Link} \to 0$ either when ${k_{A\text{-}RX}}^2 Q_A Q_{RX\text{-}L} \to 0$ or ${k_{A\text{-}RX}}^2 Q_A Q_{RX\text{-}L} \to \infty$. Therefore, an optimum value exist for ${k_{A\text{-}RX}}^2 Q_A Q_{RX\text{-}L}$,

$$({k_{A\text{-}RX}}^2 Q_A Q_{RX\text{-}L})_{opt} = \sqrt{1 + {k_{TX\text{-}A}}^2 Q_{TX} Q_A}. \tag{2.15}$$

If the position of the additional coil can be selected, (2.15) can be fulfilled adjusting the additional coil position or its geometry.

However, if $k_{TX\text{-}A}$ and $k_{A\text{-}RX}$ are given, the optimum Q_L that maximizes the efficiency in a 3-coil link (2.14) is

$$Q_{L_{opt}} = Q_{RX} \cdot \sqrt{\frac{{k_{TX\text{-}A}}^2 Q_{TX} Q_A + 1}{({k_{A\text{-}RX}}^2 Q_A Q_{RX} + 1)({k_{TX\text{-}A}}^2 Q_{TX} Q_A + {k_{A\text{-}RX}}^2 Q_A Q_{RX} + 1)}}. \tag{2.16}$$

Although having given coupling factor is an unlikely scenario, we are going to show in Section 2.1.3.2, that the coupling factors can be optimized to maximize a figure of merit, and then for that given couplings, the MN is designed. In Section 2.1.4 we show that the approach of Section 2.1.3.2 is the one that achieves higher link efficiency.

2.1.3 2-coil vs 3-coil comparison

This section summarizes a comparison between the use of a given 2-coil link, or, alternatively adding a third resonant coil (3-coil). Additionally, the role of an MN to adapt Q_L is studied in both cases.

We considered two different scenarios to compare the 2- and 3-coil links. First, the case where the RX cannot be modified and just an additional coil is included (Section 2.1.3.1). Then, the case where besides adding a coil, the receiver MN is accordingly adjusted (Section 2.1.3.2).

2.1.3.1 Comparison with the same receiver MN

If the 2-coil (2.7) and 3-coil (2.14) links efficiencies are compared, the load coil efficiency ($Q_{RX\text{-}L}/Q_L$) is present in both expressions so that it does not affect the comparison.

Defining $X_{TX\text{-}RX} = {k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L}$ and $X_{TX\text{-}A} = {k_{TX\text{-}A}}^2 Q_{TX} Q_A$ and assuming $({k_{A\text{-}RX}}^2 Q_A Q_{RX\text{-}L})_{opt}$ is selected (by selecting the optimal additional coil position), the 2-coil and 3-coil link efficiency can be expressed as,

$$\begin{aligned}\eta_{2coil} =& \frac{Q_{RX\text{-}L}}{Q_L}\frac{X_{TX\text{-}RX}}{X_{TX\text{-}RX}+1} = \frac{Q_{RX\text{-}L}}{Q_L} f_2(X_{TX\text{-}RX}) \\ \eta_{3coil} =& \frac{Q_{RX\text{-}L}}{Q_L}\frac{\sqrt{1+X_{TX\text{-}A}}.X_{TX\text{-}A}}{(1+\sqrt{1+X_{TX\text{-}A}})(1+X_{TX\text{-}A}+\sqrt{1+X_{TX\text{-}A}})} = \frac{Q_{RX\text{-}L}}{Q_L} f_3(X_{TX\text{-}A})\end{aligned} \tag{2.17}$$

If $X_{TX\text{-}A} = X_{TX\text{-}RX} = X$, $f_2(X) > f_3(X)\ \forall\ X$ and thus $\eta_{2coil} > \eta_{3coil}$, which means that the inclusion of an additional coil has reduced the link efficiency.

The larger $X_{TX\text{-}A}$ or $X_{TX\text{-}RX}$ are, the higher the efficiencies are, as f_2 and f_3 are monotonically increasing functions. Therefore, the efficiency can be improved by an additional coil if $X_{TX\text{-}A}$ is higher enough than $X_{TX\text{-}RX}$. To achieve $X_{TX\text{-}A} > X_{TX\text{-}RX}$, the additional coil should be closer to the transmitter or has a larger radius than the receiver ($k_{TX\text{-}A} > k_{TX\text{-}RX}$). Additionally, $X_{TX\text{-}A} > X_{TX\text{-}RX}$ can be achieved if $Q_A > Q_{RX\text{-}L}$, which can be done as Q_A (2.2) is only determined by the parasitic resistance of the additional coil while $Q_{RX\text{-}L}$ (2.5) has an external load resistor. This is indeed one of the most important advantage of 3-coil over 2-coil links.

The optimum Q_L is different in a 2-coil system (2.8) and in a 3-coil system (2.16). Therefore the comparison carried out in this subsection could be unfair, as the same Q_L is present in both cases. For instance, if the 2-coil system is optimized ($Q_{L_{opt}}$), the 3-coil link that requires a different Q_L is not. However, in some applications, it is not practical to modify the receiver. In Section 2.2, we design an additional coil to be included in an actual RFID system in order to increase its distance range. The selected actual RFID system is the one used in Uruguay for cattle identification. Millions of tags are already in use, therefore a design that includes a tag (RX) modification is infeasible in this case.

2.1.3.2 Comparison adjusting the receiver MN

The use of a general MN in the RX coil adds a degree of freedom that allows us to set the optimum Q_L (2.2) in both systems (2- and 3-coil link), as in (2.8) and (2.16) respectively. The following question arises: when using this general MN, does the addition of the third coil provide a benefit in terms of the total efficiency? We discuss this issue in the remainder of this section.

If the optimum Q_L of (2.8) and (2.16) are substituted in (2.7) and (2.14) respectively, it is interesting to note that the link efficiency of both systems has the same expression

$$\eta_{2,3} = \frac{A_{2,3}^2 - 1}{(A_{2,3}+1)^2}, \tag{2.18}$$

where A_2 (for 2-coil link) and A_3 (for 3-coil link) are,

$$\begin{aligned} A_2 &= \sqrt{1 + {k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX}} \\ A_3 &= \sqrt{1 + \frac{{k_{TX\text{-}A}}^2 Q_{TX} Q_A . {k_{A\text{-}RX}}^2 Q_A Q_{RX}}{{k_{TX\text{-}A}}^2 Q_{TX} Q_A + {k_{A\text{-}RX}}^2 Q_A Q_{RX} + 1}}. \end{aligned} \tag{2.19}$$

As $\eta_{2,3}$ (2.18) increases when $A_{2,3}$ increases, it is easy to see that adding a resonant coil in order to increase the link efficiency is profitable if and only if,

$${k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX} < \frac{{k_{TX\text{-}A}}^2 Q_{TX} Q_A . {k_{A\text{-}RX}}^2 Q_A Q_{RX}}{{k_{TX\text{-}A}}^2 Q_{TX} Q_A + {k_{A\text{-}RX}}^2 Q_A Q_{RX} + 1} \tag{2.20}$$

This inequality provides a very simple method to determine if an additional coil is profitable (assuming that $Q_{L_{opt}}$ is going to be set because the maximum efficiency is desired).

As mentioned, it can be seen from (2.18) and (2.19) that $A_{2,3}$ must be maximized in order to maximize the efficiency. In the 2-coil system, this leads to maximize ${k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX}$, which is a usually applied result [38].

In the 3-coil link (with optimum Q_L), we are demonstrating that the following term needs to be maximized,

$$\frac{{k_{TX\text{-}A}}^2 Q_{TX} Q_A . {k_{A\text{-}RX}}^2 Q_A Q_{RX}}{{k_{TX\text{-}A}}^2 Q_{TX} Q_A + {k_{A\text{-}RX}}^2 Q_A Q_{RX} + 1}. \tag{2.21}$$

As far as we know, this criterion has not been highlighted before and is very useful to determine if an additional coil will be profitable and also to find optimal size and position in order to maximize (2.21).

The term (2.21) can be simplified for the case of SCMR (${k_{TX\text{-}A}}^2 Q_{TX} Q_A >> 1$ or ${k_{A\text{-}RX}}^2 Q_A Q_{RX} >> 1$) and $Q_{TX} = Q_{RX}$ to obtain that the optimum values of $k_{TX\text{-}A}$ and $k_{A\text{-}RX}$ are the ones which maximize ${k_{TX\text{-}A}}^2 . {k_{A\text{-}RX}}^2 / ({k_{TX\text{-}A}}^2 + {k_{A\text{-}RX}}^2)$ (expression that only depends on the geometry of the system).

2.1.4 Simulation results – improvement of a MN in a 3-coil link –

As was shown, in a 3-coil link, the link efficiency can be increased adjusting the additional coil position or geometry until fulfilling (2.15) or adjusting Q_L to (2.16). Therefore, two approaches exist to match the system. The aim of the simulations in this section is to demonstrate that an MN is still useful in a 3-coil link. In addition, we provide a simple method to find the optimum combination of MN and additional coil position.

Two 3-coil link systems (as shown in Fig. 2.3) were simulated using series-resonant and an L-C MN (Fig. 2.5) to set an optimum Q_L. The simulation was performed in CST (Fig. 2.4). All the values used in the proof-of-concept systems are shown in Table 2.1.

Table 2.1: Proof-of-concept systems. The coils used, load value ($R_L = 500\ \Omega$) and carrier frequency are assumed as given, C_{TX} and C_A were selected to achieve resonance at 1 MHz. The values of C_{RX} and L_{RX} were optimized as described in this Section 2.1.4.

Coil	turns	Radius	Quality factor	Resonance Components
L_{TX}	200	5 cm	$Q_{TX} = 50$	$C_{TX} = 3.2$ pF
L_A	100	8 cm	$Q_A = 250$	$C_A = 6.98$ pF
L_{RX}	50	2 cm	$Q_{RX} = 35$	Series-Resonant $C_{RX} = 180$ pF L-C MN Fig. 2.5 $C_{RX} = 261$ pF $L_{RX} = 278\ \mu$H

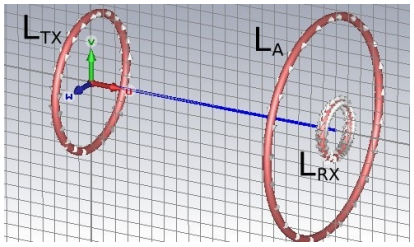


Figure 2.4: Model of 3 coupled coil system. CST simulation.

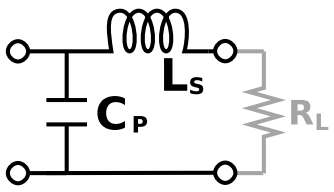


Figure 2.5: L-C MN.

The distance between the TX coil and the RX coil was kept fixed at 20 cm and the additional coil position $D_{TX\text{-}A}$ was varied ($D_{TX\text{-}A} + D_{A\text{-}RX} = 20\ cm$). Figure 2.6 shows the simulation results.

In the case of a series-resonator, (2.15) is fulfilled around $D_{TX\text{-}A} = 16$ cm achieving $\eta_{Link} = 34\%$. In this case, the additional coil position was optimized for a given Q_L.

However, if we first find the $D_{TX\text{-}A}$ that maximize A_3 and then for that position Q_L is set as $Q_{L_{opt}}$, the efficiency achieved is maximized. In this case, the optimum

pair of $D_{TX\text{-}A}$ and Q_L is found. Any other value of Q_L will not achieve such a high efficiency for all intermediate additional coil position $D_{TX\text{-}A}$. The $D_{TX\text{-}A} \simeq 14$ cm is the one that maximizes A_3. The L-C-resonator Fig. 2.6, was designed to fulfill (2.16) at $D_{TX\text{-}A} \simeq 14$ cm, achieving $\eta_{Link} = 40$ %.

In this example, (2.20) is verified for any $D_{TX\text{-}A}$ which means that the additional coil improves the link efficiency regardless of the value of $D_{TX\text{-}A}$. If the additional is removed (2-coil link), the efficiency obtained is 26 μ%.

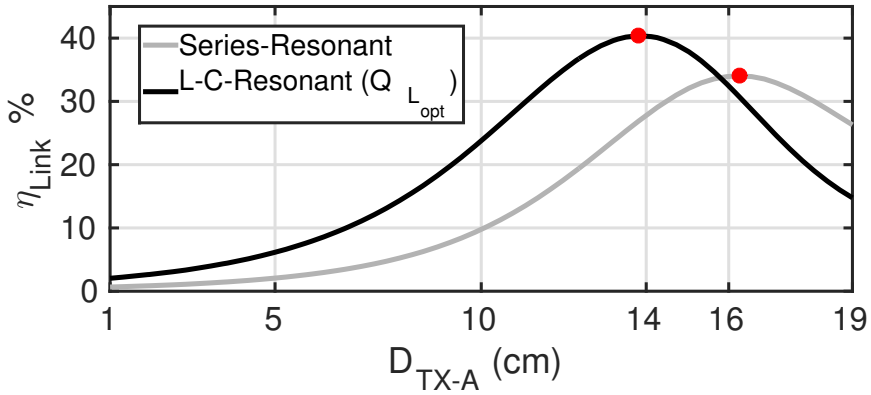


Figure 2.6: Simulation result. $D_{TX\text{-}RX} = D_{TX\text{-}A} + D_{A\text{-}RX} = 20$ cm.

2.1.5 Conclusion of Section 2.1

This section considered the use of a general load MN in 2- and 3-coil links. The commonly used (RLT) equations assume a parallel-resonator or a series-resonator in the RX. We generalized these equations for a general MN highlighting the differences between the 2- and 3-coil cases.

It was shown that the MN can be used to improve the efficiency where there are geometric constraints, e.g. coil 2 and 3 must be fixed together at a certain distance. Besides, we showed analytically and by simulation, that MNs can be used to improve the efficiency in a 3-coil link even when the additional coil can be freely positioned. This proves that, although the additional coil can be used to match the system as mentioned in previous works [38], the MN is still useful in a 3-coil link.

Moreover, a theoretical analysis shows whether the additional coil increases or not the total link efficiency. Finally, useful expressions have been deduced to compare and maximize 2 and 3 coil link efficiencies.

2.2 Third resonant coil in RFID systems

The additional resonant coils have the potential to enhance read range of near field RFID systems. In spite of this, its application in the RFID context has not been deeply analyzed yet. This section models and analyses a half-duplex, Frequency Shift Keying (FSK) RFID system with one additional coil between the reader and the tag, taking into account both phases (charging and reading) of this bidirectional operation. A 3-coil RFID system was designed using a commercial tag (RI-INL-R9QM widely used in cattle identification), reader (using a TMS3705) and designing the additional resonant coil whose radius and quality factor were optimized. Additionally, the influence of high coil quality factor is addressed for steady state and transient response. The designed system increases almost 2.7 times the original 2-coil RFID read distance (from 16 cm to 43 cm). The analytical design and measurements data are in good agreement. The design procedure can be applied not only to other RFID systems but also to other systems that use the same channel to energize and transfer data, such as some AIMDs.

2.2.1 RFID introduction

The use of RFID has dramatically increased in recent years. This technology has several applications such as track and manage inventory, access management, animal identification and helping toll collection. In this context, it is usually desirable to achieve long read ranges. In cattle identification, for instance, increasing the read distance eases the system operation.

In order to enlarge the read distance, active (battery-powered) tags are sometimes used, avoiding the need of transferring power and strengthening the tag response. Although used, this adds complexity and makes the system more expensive. Passive tags are cheaper, robust and have greater durability than the active ones. More sophisticated approaches like reconfigurable antenna architectures [48] and multisine excitation signals [49] have been presented, showing the interest in the research on technical alternatives for increasing the read distance. In applications where a large number of tags are already in use, like cattle identification, solutions that just modify the reader, being compatible with existing tags, are key for promoting adoption.

The tag data transmission can be done simultaneously with the charging phase (full duplex), e.g., by load shift keying modulation, or after the charging phase (half-duplex). If the system is half-duplex, during the charging phase a storage capacitor is charged in the tag. Then this energy is used to respond to the reader (reading phase), for example by transmitting the data modulated in FSK.

This work takes a standard RFID system used for cattle identification as a case study. This system is implemented with passive tags, operates in half-duplex with FSK modulation at low-frequency (134.2 kHz charging, 134.2 kHz and 123.2 kHz response frequencies for, respectively, the 0 and 1 bit) [50]. The system operation and equivalent schemes for the charging and reading phase are graphically depicted in Fig. 2.7. As can be seen, it consists of 50 ms charging phase followed by the tag response (reading phase) of, approximately, 15 ms.

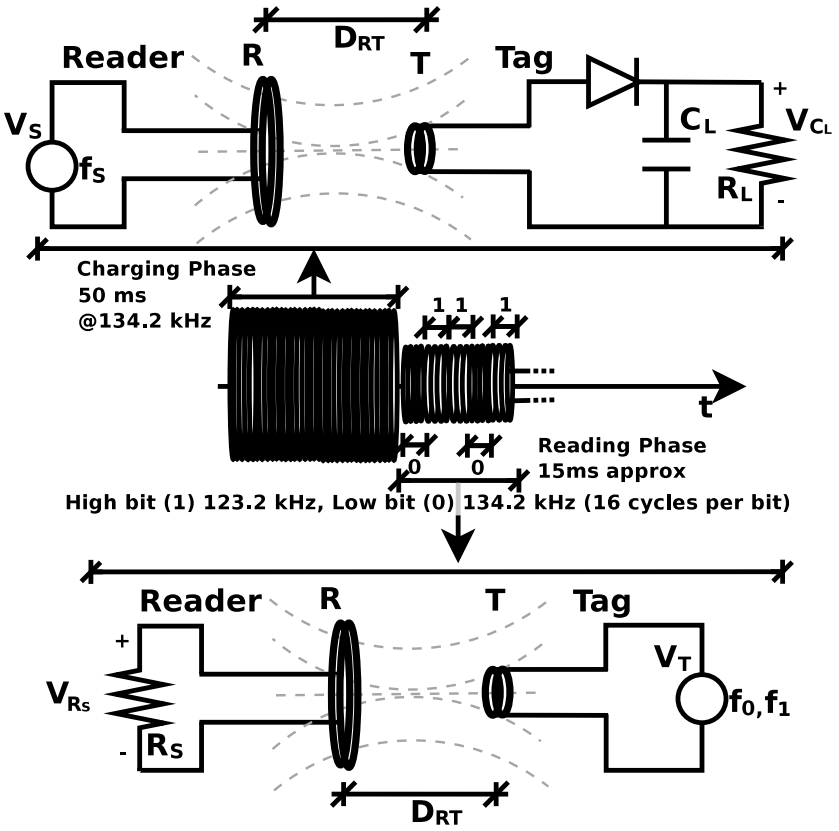
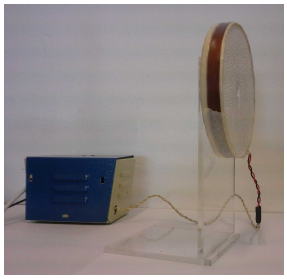


Figure 2.7: Scheme of a half-duplex RFID system with FSK response.

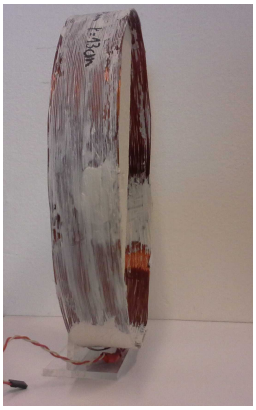
In this system, the maximum read distance can be limited either by the charging or the reading phase. If the voltage available in the storage capacitor (C_L in Fig. 2.7) after the charging phase (50 ms) is not enough for the tag to work, it will not respond. The response will also fail if the voltage in the storage capacitor, during the response time, falls below a minimum value required for data transmission by the tag. Additionally, if the reader is too far from the tag, the received response may be too weak, and thus not be correctly decoded due to noise.

As was discussed previously, an additional resonant coil can increase the efficiency for a given distance or the transfer distance for a given efficiency. Many papers have been published based on this principle, but only a few use it in the RFID context. Moreover, an in-depth study of the use of additional resonant coils in RFID applications, taking into account both charging and reading phases (bidirectional), has not been published in any work previous to our [5], as far as we know.

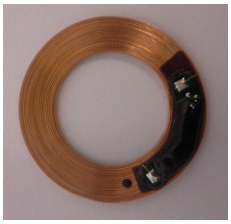
In [51], a 4-coil system to transfer power to an RFID sensor is analyzed. However, it just considers the charging phase, thus only considering a unidirectional operation with a single frequency. The study presented in [51] was further developed in [52] where the reduction in the system bandwidth due to high coil quality factors is mentioned as a drawback but its exact consequence in the link is not



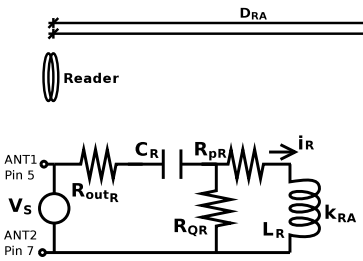
(a) Reader (TMS3705)



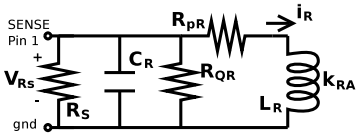
(b) Additional coil



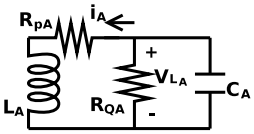
(c) Commercial tag (RI-INL-R9QM)



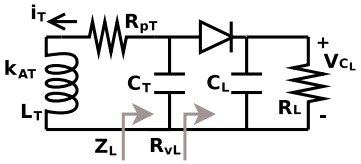
(e) Reader model during the charging phase



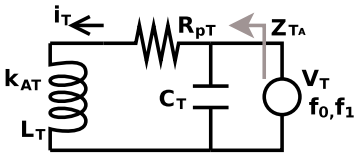
(f) Reader model during the reading phase



(g) Additional coil model



(h) Tag model during the charging phase



(i) Tag model during the reading phase

Figure 2.8: System model. The subscript R, A and T are for the reader, the additional coil and the tag components respectively. R_{p_i}, L_i and C_i are the parasitic resistance, self-inductance and resonant capacitor respectively. The subscript RA, AT and RT are going to be used to indicate that the distance (D_{ij}) or coupling factor (k_{ij}) are between reader, additional coil or tag. R_{QR} and R_{QA} are added to control the impedance seen at the reader and the additional coil circuits respectively. The half-wave rectifier (diode and C_L) and R_L models the tag load while R_S models the reader input impedance during the reading phase. V_S is the reader's driver signal and V_T the tag response signal. R_{out_R} is the reader's driver output resistance.

analyzed. As it is shown in this work, increasing the additional coil quality factor increases both the 1 and 0 bits steady state reading amplitude (V_{Rs} on Fig. 2.7). Thus, the reduction of the system bandwidth is not a problem from the point of view of attenuation of the transmission frequencies in the reading phase. Instead, we clarify that the reduced bandwidth due to high coil quality factors may limit the operation due to its impact on the transient response of the system, causing intersymbol interference between consecutive bits.

A 3-coil system applied directly to RFID is studied in [53]. That work, in contrast with [51, 52] uses a commercial tag and reader. However, the reader and tag were not deeply modeled, neither at the charging nor at the reading phase, studying the system transfer in only one direction. This results in a non-optimum design of the additional coil. Furthermore, the read range limits are measured but not theoretically analyzed.

This work analyses both the charging and the reading phase for a 3-coil RFID system. A 3-coil system was chosen instead of the more typical 4-coil system based on two main reasons. First, it allows to improve the RFID link with minimal additions to the original (2-coil) system. Secondly, it has been proved, that 4-coil links fail to achieve a high power delivered to the load compared with 3-coil links [38]. Basically, in 4-coil links, there is always a compromise between achieving high system efficiency while delivering enough power to the load for a given driver output voltage (V_S). However, 3-coil links are able to achieve both, high efficiency and high power delivered to the load [38]. Increasing V_S will improve the power delivered to the load in any system (2-, 3- or 4-coil links) but it may add complexity to the driver and it implies a further change in the system, which is not desirable. For the same reasons (i.e. to explore solutions compatible with existing tags) other alternatives, such as modifying the tag MN as discussed in Section 2.1 are not considered in this section.

Summarizing, both tag and reader, are modeled and an optimal additional coil is designed taking into account the bidirectionality of the system. The impact of the characteristics of the additional resonant coil (quality factor, radius, and resonant frequency) are addressed in both directions of the operation of the link. As two different frequencies will exist in the same system (one corresponding to charging and the 0 bit and the other one to the 1 bit), the presented analytical model takes into account the operation outside of the coil resonant frequency. In the analysis, it is considered not only the steady state response of the system but also how the transient response to changes in transmitted bits impacts the read process. The designed system increases almost 2.7 times the original 2-coil RFID read distance, from 16 cm to 43 cm.

This Section 2.2 is organized as follows. First, Section 2.2.2 introduces the reader, tag, and additional coil models which are then used to theoretically analyze and design the 3-coil system. Next, Section 2.2.3 presents the traditional 2-coil RFID system measurements in order to, later, compare them with the proposed 3-coil system. Section 2.2.4 summarizes the 3-coil link equations (derivations are presented in Appendix A). In Section 2.2.5 the additional coil design is presented, analyzing the influence of its resonant frequency, radius and quality factor

as well as reader's resonant frequency. The 3-coil link measurements are detailed in Section 2.2.6. Finally, Section 2.2.7 summarizes the main conclusions.

2.2.2 System model

In this section, the reader, the tag and the additional coil models are presented. Compared with the previous Section 2.1, the nomenclature is changed as there are no TX and RX. The Reader works as the TX in the charging phase, but it is the RX during the reading phase. Therefore, we will use Reader (R) and Tag (T) instead of Transmitter (TX) and Receiver (RX), changing the subscripts of the parameters accordingly.

The reader that we used is shown in Fig. 2.8a. It is based on a TMS3705 transponder base station IC from Texas Instruments (TI). The schematic diagrams are presented in Fig. 2.8e and Fig. 2.8f for the charging and reading phase respectively. These schematic diagrams are one of the suggested by TI.

The tag is the RI-INL-R9QM from TI and it is shown in Fig. 2.8c. The schematic diagrams shown in Fig. 2.8h and Fig. 2.8i were derived from the tag datasheet and the guidelines of the International Committee for Animal Recording (ICAR) [54].

Table 2.2 shows the component values. The value of the self-inductances (L) and their parasitic resistances (R_p) of the reader, additional coil and tag, play an important role in the link efficiency. Therefore, they were measured. R_p was measured for both frequencies (0 and 1 bit), so that the variation of the parasitic resistance with frequency is taken into account. The 0 and 1 bit frequencies were obtained from the tag datasheet. The coupling factors between coils were simulated using CST. The reader generates a 5 V_p (peak voltage) square wave. For V_S, it is only considered the 6.37 V_p fundamental of this square wave, since higher order harmonics will be filtered by the system. The reader's driver output impedance R_{out_R} was measured and is within the range estimated by the manufacturer. The peak voltage of the tag's driver (V_{T_p} in Table 2.2) was experimentally determined so that the tag equivalent circuit generates the same field strength as an actual tag. The reader resonant frequency (f_{res_R}) value, which defines the C_R value, and R_{QR} value will be discussed for the typical 2-coil system in Section 2.2.3 and for the designed 3-coil system in Section 2.2.5.

The tag charging is going to be considered successful if V_{C_L} is higher than 5 V at the end of the phase (based on ICAR guidelines [54]). The steady state amplitude received by the reader from the tag (V_{R_S} Fig. 2.8f) should be high enough in order not to be affected by noise and to be correctly demodulated. The receiver sensitivity is supposed to be high (capable of detecting signals in the few mV_p range). As it is going to be shown, this amplitude does not limit the RFID system, thus its exact value is not essential. In order to estimate the limit for a reliable detection of the signal, $V_{R_S} > 10$ mV_p was considered.

Table 2.2: Component values of Fig. 2.8. Some values (indicated as TBD) are going to be determined at the design stage. These values are then presented in Table 2.3.

Reader	Tag
$R_{pR} = 15.1\ \Omega$ @123.2 kHz	$R_{pT} = 42.75\ \Omega$ @123.2 kHz
$R_{pR} = 15.9\ \Omega$ @134.2 kHz	$R_{pT} = 44.59\ \Omega$ @134.2 kHz
$L_R = 443\ \mu$H	$L_T = 2.49$ mH
$f_{res_R} = TBD$; $C_R = TBD$	$f_{res_T} = 134.2$ kHz ; $C_T = 565$ pF
$R_S = 47\ \text{k}\Omega$	$C_L = 68$ nF
Radius $r_R = 6$ cm	$R_L = 2.2\ \text{M}\Omega$
$R_{QR} = TBD$	$f_S = f_0 = 134.2$ kHz
$V_S = 6.37\ \text{V}_p$	$f_1 = 123.2$ kHz
$R_{out_R} = 11.5\ \Omega$	Radius $r_T = 1.35$ cm
	$V_{T_p} = 9\ \text{V}_p$

2.2.3 2-coil RFID link measurements

For the typical 2-coil RFID system, the reader resonant frequency will be set equal to the tag resonant frequency 134.2 kHz.

The reader (TMS3705) requires a minimum value of load impedance at the driver (ANT1 Pin 5 and ANT2 Pin 7, see Fig. 2.8e). In order to limit the impedance seen by the driver at the minimum allowed, that we will call $Z_{R_{V\,MIN}}$, $R_{QR} = 5\ \text{k}\Omega$ is needed. This assures that when the reader is not coupled with any other circuit, the driver seen impedance is equal to its minimum allowed value $|Z_{R_V}| = Z_{R_{V\,MIN}}$, limiting its maximum output current.

The maximum read distance obtained was $D_{RT} = 16$ cm. In order to identify the no read reason, another coil was used as an antenna to sense the magnetic field between the reader and tag. Figure 2.9 shows the magnetic field strength near the tag for $D_{RT} = 16$ cm (where the tag was read) and for $D_{RT} = 17$ cm (where the tag was NOT read). As can be seen, the tag response at 17 cm is shorter than the total tag response time ($\simeq 15$ ms, as the one at 16 cm). This is because the energy stored in C_L was not enough at $D_{RT} = 17$ cm to complete the whole response, thus the tag was not read.

As a conclusion, the charging phase is limiting the read distance. Therefore, the goal of the 3-coil system should be to improve the charging phase, without neglecting the reading phase.

2.2.4 3-coil RFID system analysis

The 3-coil system is analyzed via RLT [25] as in Section 2.1. The link efficiency is computed multiplying the reader efficiency (η_R), the additional coil efficiency (η_A) and the tag efficiency (η_T), either in charging or reading phases.

The efficiency was previously calculated assuming that all the coils resonate

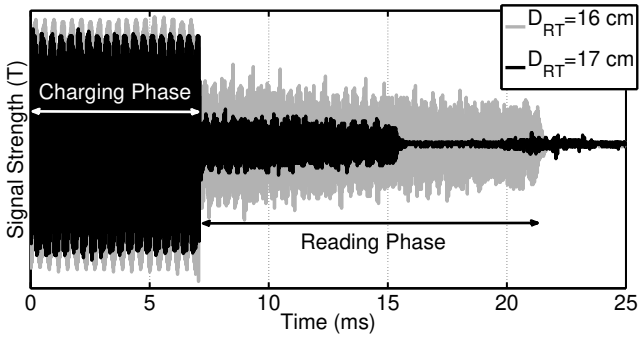
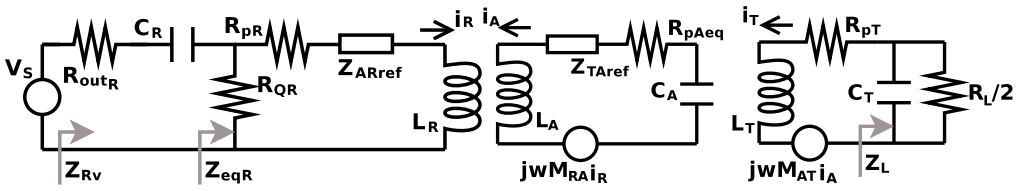


Figure 2.9: Measured magnetic field between the reader and tag for $D_{RT} = 16$ cm and $D_{RT} = 17$ cm showing why the tag was not read at 17 cm.



(a) Reader model (b) Additional coil model (c) Tag model

Figure 2.10: Reader, additional coil and tag models during the charging phase, including reflected impedance from the subsequent stage. The derivations associated with this scheme are presented in Appendix A.

at the same frequency, which is a usual assumption. However, this is not the case in this section as two different frequencies exist in the same system at the reading phase. Additionally, as it is going to be studied in Section 2.2.5, it will be profitable to change the resonant frequency of the reader. For these reasons, the analysis presented here takes into consideration that each coil has its own resonant frequency, $w_{res_i} = 2\pi.f_{res_i} = \frac{1}{\sqrt{L_i C_i}}$ with $i = R$, A or T for, respectively, the reader, additional and tag parameters.

It is worth mentioning that this analysis is for steady state. Similar considerations about the transient response, which impacts the bit transitions and decoding, will be addressed in Section 2.2.5.

The results found in this section will be useful to design and predict the performance of the 3-coil system. For instance, how the additional coil quality factor affects the steady state response for both bits, even when not all the coils are resonating.

First, the charging efficiency is presented in Section 2.2.4.1. Then, the same idea is used to calculate the reading efficiency in Section 2.2.4.2. The results or definitions that have different values depending on the phase are specified by the subscript (C) for the charging phase and (R) for the reading phase.

2.2.4.1 Charging Phase

The derivation details are presented in Appendix A. This section summarizes and analyses the results.

Tag Efficiency Assuming that the half-wave rectifier is ideal and therefore does not dissipate (in order to simplify the model), the tag efficiency (2.22), is simply calculated as the ratio between the power dissipated in R_L over the total power dissipated in R_L and R_{pT} (see Fig. 2.8h). $Q_{L_{(C)}}$ (2.23) and Q_T (2.24) are the load quality factor at charging phase and tag quality factor respectively.

$$\eta_{T_{(C)}} = \frac{Q_T}{Q_T + Q_{L_{(C)}}} \tag{2.22}$$

$$Q_{L_{(C)}} = \frac{wL_T}{Re\{Z_L\}} = \frac{R_L/2}{w.L_T}\left(\frac{w}{w_{res_T}}\right)^4 \tag{2.23}$$

$$Q_T = \frac{wL_T}{R_{pT}} \tag{2.24}$$

All these parameters are given by the model, so the tag efficiency is fixed.

Additional Coil Efficiency The total equivalent resistance in the additional coil R_{pAeq} of Fig. 2.10b, can be calculated as (2.25). R_{QA}, Fig. 2.8g, is added to adjust Q_A and its value is determined in Section 2.2.5. Z_{TAref} is the reflected impedance in the additional coil from the tag. The normalized reflected impedance in the additional coil from the tag is defined as $\overline{Z_{TAref}} = Z_{TAref}/R_{pAeq}$ (Fig. 2.10b) and it can be calculated as (2.26). Q_A (2.27) is the additional coil quality factor.

$$R_{pAeq} = \frac{(w.L_A)^2}{R_{QA}}.\left(\frac{w_{res_A}}{w}\right)^4 + R_{pA} \tag{2.25}$$

$$\overline{Z_{TAref}} = \frac{k_{AT}^2 Q_T Q_A Q_{L_{(C)}}}{Q_T + Q_{L_{(C)}} + jQ_T Q_{L_{(C)}}(1-(w_{res_T}/w)^2)} \tag{2.26}$$

$$Q_A = \frac{wL_A}{R_{pAeq}} \tag{2.27}$$

Thus, the additional coil efficiency is given by (2.28).

$$\eta_{A_{(C)}} = \frac{Re\{\overline{Z_{TAref}}\}}{1 + Re\{\overline{Z_{TAref}}\}} \tag{2.28}$$

As can be noticed, $\eta_{A_{(C)}}$ is maximum when the tag is resonating ($w_{res_T} = w$), since $Re\{\overline{Z_{TAref}}\}$ is maximum at that frequency. The tag resonant frequency is given by the tag designer and is equal to the reader charging signal ($f_{res_T} = f =$ 134.2 kHz).

It can be seen that a higher Q_A increases $\eta_{A_{(C)}}$, independently on whether the tag or additional coil operate at their resonance frequency. This is the case because (2.26) and (2.28) are valid for any w.

Reader Efficiency The normalized reflected impedance in the reader from the additional coil $\overline{Z_{ARref}} = Z_{ARref}/R_{pR}$ (Fig. 2.10a) can be obtained in a similar way

$$\overline{Z_{ARref}} = \frac{k_{RA}^2 Q_A Q_R}{1 + \overline{Z_{TAref}} + jQ_A(1 - (w_{res_A}/w)^2)} \tag{2.29}$$

$$Q_R = \frac{wL_R}{R_{pR}} \tag{2.30}$$

where Q_R (2.30) is the reader quality factor.

The reader efficiency is

$$\eta_{R_{(C)}} = \frac{Re\{\overline{Z_{ARref}}\}}{1 + Q_R^2 \frac{R_{pR}}{R_{QR}} + \frac{R_{out_R}}{R_{pR}} + Re\{\overline{Z_{ARref}}\}} \tag{2.31}$$

Likewise, $\{\eta_R \eta_A\}_{(C)}$ also rises if Q_A increases, regardless whether the reader, tag or additional coil operate at their resonance frequency.

The output voltage V_{C_L} can be calculated as

$$V_{C_L} = \sqrt{R_L \frac{1}{2} \frac{V_S^2 Re\{Z_{R_V}\}}{|Z_{R_V}|^2} . \{\eta_R \eta_A \eta_T\}_{(C)}} \tag{2.32}$$

$$\frac{Z_{R_V}}{R_{pR}} = 1 + Q_R^2 \frac{R_{pR}}{R_{QR}} + \frac{R_{out_R}}{R_{pR}} + \overline{Z_{ARref}} + jQ_R \left(1 - \left(\frac{w_{res_R}}{w}\right)^2\right) \tag{2.33}$$

where $|Z_{R_V}|$ indicates the absolute value of Z_{R_V} (Fig. 2.10a). R_{QR} adjusts the driver (V_S) load impedance.

This expression predicts the voltage V_{C_L} at the end of the charging phase (50 ms) assuming that steady state is achieved.

The absolute value $|\overline{Z_{ARref}}|$ rises when Q_A increases (2.29), thus the driver load impedance $|Z_{R_V}|$ (see (2.33) and Fig. 2.10a) will also increase which may decrease the power delivered by the reader, reducing V_{C_L} (2.32). However, $|Z_{R_V}|$ is dominated by the reader impedance (R_{pR}+R_{out_R}) in this application and therefore, $|Z_{R_V}|$ is not significantly affected by Q_A. Consequently, the power delivered by the reader can be approximated as constant.

Summarizing, $\{\eta_R \eta_A\}_{(C)}$ and thus V_{C_L}, rise if Q_A increases.

2.2.4.2 Reading Phase

Applying the same procedure, the reading efficiency and V_{R_S} voltage (Fig. 2.8f) can be obtained.

Reader efficiency

$$\eta_{R_{(R)}} = \frac{Q_R}{Q_R + Q_{L_{(R)}}} \tag{2.34}$$

$$Q_{L_{(R)}} = \frac{R_S // R_{QR}}{w.L_R} \left(\frac{w}{w_{res_R}}\right)^4 \tag{2.35}$$

Additional coil efficiency

$$\eta_{A_{(R)}} = \frac{Re\{\overline{Z_{RAref}}\}}{Re\{\overline{Z_{RAref}}\} + 1} \tag{2.36}$$

$$\overline{Z_{RAref}} = \frac{k_{RA}^2 Q_A Q_R Q_{L_{(R)}}}{Q_R + Q_{L_{(R)}} + jQ_R Q_{L_{(R)}}(1 - (w_{res_R}/w)^2)} \tag{2.37}$$

Tag efficiency

$$\eta_{T_{(R)}} = \frac{Re\{\overline{Z_{ATref}}\}}{Re\{\overline{Z_{ATref}}\} + 1} \tag{2.38}$$

$$\overline{Z_{ATref}} = \frac{k_{AT}^2 Q_A Q_T}{1 + \overline{Z_{RAref}} + jQ_A(1 - (w_{res_A}/w)^2)} \tag{2.39}$$

Finally the output voltage

$$V_{R_S} = \sqrt{R_S // R_{QR} \frac{V_T^2 Re\{Z_{T_A}\}}{|Z_{T_A}|^2} . \{\eta_R \eta_A \eta_T\}_{(R)}} \tag{2.40}$$

$$Z_{T_A}/R_{pT} = 1 + \overline{Z_{ATref}} + jQ_T \tag{2.41}$$

where Z_{T_A} is the tag's driver (V_T) load impedance (Fig. 2.8i).

The same reasoning applies in this case, V_{R_S} rises for the 0 and 1 bits if Q_A increases. Therefore, even though the system bandwidth decreases, both bit amplitudes rise when Q_A increases.

2.2.5 3-coil RFID system, additional coil design

Section 2.2.4 shows how an additional coil between the reader and the tag affects each phase. That analysis provides analytical expressions to predict the steady state amplitude on each phase. These expressions are now used to optimize the 3-coil system. Additionally, Section 2.2.3 shows that the typical 2-coil system is currently limited by the charging phase, thus the additional coil should be focused on improving this phase.

In cattle identification, for instance, millions of these tags are already in use. Consequently, solutions that do not modify the tag circuit have a higher impact. In this section, the design of the additional coil is approached, assuming that the tag is given and only the reader can be modified.

First, the performance dependence with Q_A is analyzed in Section 2.2.5.1. The analysis shows a trade-off between increasing the charging distance and improving the reading phase distance. This section also explains how this trade-off can be relaxed if the reader resonant frequency is lower than 134.2 kHz.

Then Section 2.2.5.2 optimizes the additional coil radius (r_A), quality factor (Q_A) and resonant frequency.

2.2.5.1 Q_A trade-off

As was shown in Section 2.2.4, the highest V_{C_L} and V_{R_S} steady state amplitudes are obtained when the additional coil has the highest possible quality factor. It was also highlighted that this relation between amplitude and Q_A is independent of the resonance of each coil. Thus, even when the signal frequency is different from the resonant one, the larger Q_A is, the better (as far as steady state is concerned).

However, a large value of Q_A may cause interference between consecutive bits (intersymbol interference) as it will be shown next. As was explained in Section 2.2.1, data is sent by FSK modulation and each bit has a length of 16 cycles modulated carrier. Therefore, both bits should extinguish in less than 16 cycles in order not to affect the consecutive one. An isolated series R-L-C circuit has a transient response which decays exponentially as $e^{-t\frac{R}{2L}}$. In order to estimate the bit decay time, the additional coil is modeled (as a first approximation) as an isolated coil. It means that each bit takes $\frac{2L}{R} = 2Q\frac{1}{w} = \frac{Q}{\pi}\frac{1}{f}$ seconds, i.e., $\frac{Q}{\pi}$ cycles, until decaying in value to 37% of its initial value. The higher the Q_A is, the longer each bit lasts, and the more intersymbol interference exists. Additionally, the system needs more time to reach steady state, as the transient response lasts longer.

Therefore, a trade-off exists between increasing steady state amplitudes and avoiding intersymbol interference.

Furthermore, if each coil resonates at the same frequency (134.2 kHz), the 0 bit will have much more amplitude than the 1 bit ($V_{R_{S@134.2\ kHz}} >> V_{R_{S@123.2\ kHz}}$). This issue aggravates the intersymbol interference, limiting even more the maximum Q_A acceptable. Different approaches can be made in order to match bits amplitude and thus relax this trade-off.

By choosing the additional coil resonant frequency between the 1 and 0 bit frequencies, the bit amplitudes can be even equaled. However, this approach will directly affect the charging phase as the charging and 0 bit frequencies are equal (134.2 kHz).

A smarter strategy is to remove R_{QR} (Fig. 2.8e and Fig. 2.8f), which had been added to limit the driver load impedance $|Z_{R_V}|$ (2.33), and limit this load impedance by choosing a lower reader resonant frequency. $|Z_{R_V}|$ has the same value, when the reader is not coupled with any circuit, in this two different scenarios: if $f_{res_R} = 126.7$ kHz is set and no R_{QR} is used, or if $f_{res_R} = 134.2$ kHz and $R_{QR} = 5\ \text{k}\Omega$. Therefore, the current ($V_S/|Z_{R_V}|$) delivered by the reader's driver is also the same in both scenarios. When no R_{QR} is used, all the driver's output current pass through the reader coil, therefore transmitting barely more power (for a given Z_{ARref}). Thus, this lower reader resonant frequency will increase $V_{R_{S@123.2\ kHz}}$ while lowering $V_{R_{S@134.2\ kHz}}$, reducing the difference between them without neglecting the charging phase.

If R_{QR} is removed, the bit decay time may increase. If the reader is modeled as an isolated coil, it will need Q_R/π cycles to extinguish each bit. Nevertheless, the bit decay time of the whole system will be dominated by Q_A as it is usually higher than Q_R. If this is not the case, the values of Q_R and Q_T should be taken into account to control the transient response.

Another alternative to match bit amplitudes in steady state could be to use a dual-band additional coil [55]. Dual-band coils add an extra pole to achieve resonance at two frequencies. This extra pole may affect the transient response increasing the bit decay time and adding complexity to the circuit. The analysis of this alternative is out of the scope of this work.

To conclude, a trade-off exists between achieving high steady state amplitudes (V_{C_L} and V_{R_S}) and avoiding intersymbol interference. Increasing Q_A will increase V_{C_L} and V_{R_S} for both 1 and 0 bits. On the other hand, a large Q_A value will increase the decay time generating intersymbol interference. If the steady state amplitudes of V_{R_S} for 1 and 0 bits are too different, intersymbol interference increases. Therefore, Q_A should be the minimum that achieves enough V_{C_L} and V_{R_S} steady state amplitudes to be decoded. Additionally, the bit amplitudes ($V_{R_{S@134.2\ kHz}}$ and $V_{R_{S@123.2\ kHz}}$) should be kept as equal as possible.

In order to balance the 1 and 0 bit amplitudes and fulfill the minimum driver load impedance requirement ($Z_{R_V} > Z_{R_{V\,MIN}}$), the reader resonant frequency is set to 126.7 kHz and no R_{QR} is used (Table 2.3) as explained before. The 2-coil maximum read distance using this reader is 17 cm, one cm higher than the one presented in Section 2.2.3. This is due to the fact that the reader current slightly increases because of not using R_{QR} to limit $|Z_{R_V}|$, as was explained in this section. The additional coil resonant frequency is not used to match bit amplitudes, as it jeopardizes the charging phase which is the limiting one as is going to be shown in the next Section 2.2.5.2.

2.2.5.2 Additional Coil Design

It is not easy to obtain analytic expressions for V_{C_L} and V_{R_S} as a function of the additional coil radius (r_A). Strictly, its optimum value depends on Q_A, the resonance frequencies $w_{res_{R,A,T}}$, and the distance between coils D_{RA} (reader-additional), D_{AT} (additional-tag). Additionally, the relationship between r_A and the coupling factors (k_{RA} and k_{AT}) should be known.

Figure 2.11 allows us to find the optimum r_A that requires the lowest Q_A to fulfill the steady state amplitude requirements. The first plot of Fig. 2.11 refers to the charging phase. The minimum Q_A that satisfies $V_{C_L} > 5$ V, for at least one position of the additional coil, is plotted as a function of $D_{RT} = D_{RA} + D_{AT}$ for several r_A values. The same was done for the reading phase, but satisfying $V_{R_S} > 10\ \mathrm{mV}_p$. In this section $f_{res_R} = 126.7$ kHz (as was discussed in Section 2.2.5.1) and $f_{res_A} = 134.2$ kHz were used.

This analysis determines the optimal values of r_A which requires the lowest Q_A in order to fulfill the specifications ($V_{C_L} > 5$ V and $V_{R_S} > 10\ \mathrm{mV}_p$). A higher Q_A value may cause intersymbol interference.

As can be seen, for the charging phase, slight variations exist for radius between 13 cm and 25 cm. For the 0 bit (134.2 kHz) reading phase almost no variations exist between the different radius. The 1 bit (123.2 kHz) starts presenting differences at long distances ($D_{RT} > 45$ cm). It is important to highlight that the charging phase is the one that requires higher Q_A. It should be mentioned that strictly,

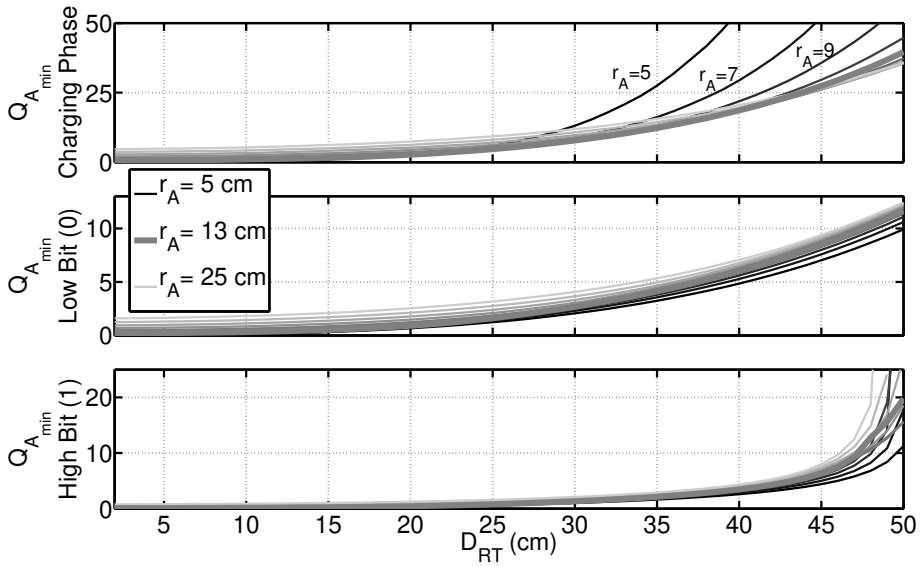


Figure 2.11: Minimum Q_A that fulfills charging phase, low (0) and high (1) bit steady state amplitude constraints, for r_A values between $r_A = 5$ cm and $r_A = 25$ cm. The coupling factors were obtained from simulations using CST.

$Q_{A_{@134.2\ kHz}}$ should fulfill the charging and 0 bit constraints and $Q_{A_{@123.2\ kHz}}$ should fulfill the 1 bit constraint.

Figure 2.11 allows different D_{RA} for charging and reading. This is useful to see the dependence of each phase with r_A, but the design must consider the same additional coil position (D_{RA}) for any phase. In Fig. 2.12 the minimum Q_A that satisfy all the specification ($V_{C_L} > 5$ V, $V_{R_{S@123.2\ kHz}} > 10$ mV$_p$ and $V_{R_{S@134.2\ kHz}} > 10$ mV$_p$) for at least one D_{RA}, is plotted as a function of D_{RT}.

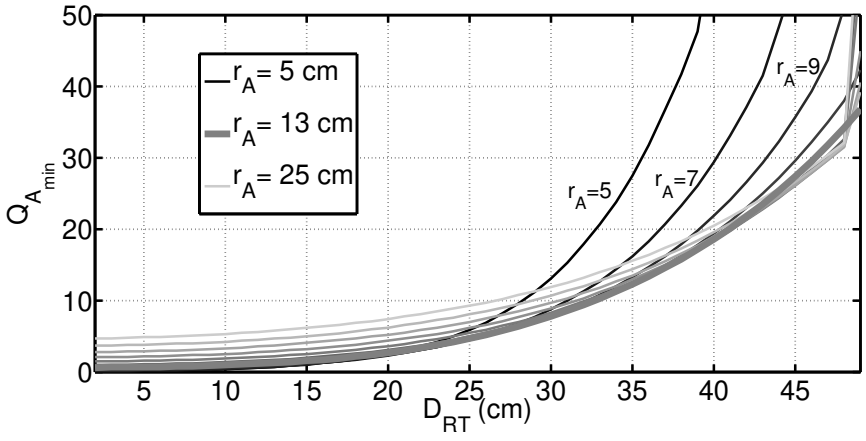


Figure 2.12: Minimum Q_A that fulfills all steady state amplitude constraints, for r_A values between $r_A = 5$ cm and $r_A = 25$ cm.

With $r_A = 13$ cm (or lower), for D_{RT} around 45 cm, the limiting phase is the charging one, as the reading phase does not need a high Q_A. For higher radius the

1 bit starts limiting at large D_{RT} (around 50 cm, see Fig. 2.11 and Fig. 2.12).

In conclusion, the best performance is obtained with $r_A = 13$ cm. This radius fulfills the steady state amplitude constraints, with the minimum possible Q_A, preventing intersymbol interference. Moreover, the best additional coil resonant frequency is $f_{res_A} = 134.2$ kHz. Changing this resonant frequency directly deteriorates the charging phase reducing the read distance, see (2.29) and (2.31). If the 1 bit had limited the read distance, a different additional coil resonant frequency would have been considered.

Achieving high D_{RT} is only possible if the $Q_{A_{min}}$ needed does not neglect the transient response.

A 3-coil system was built using the typical tag (Fig. 2.8c) and the reader without R_{QR} and $f_{res_R} = 126.7$ kHz. The additional coil has 13 cm radius, 40 turns, .9 mm wire section diameter, quality factor of $41_{@134.2\,kHz}$ ($46_{@123.2\,kHz}$) and its resonant frequency was tuned to 134.2 kHz. Initially R_{QA} is not included.

The 3-coil system was set with $D_{RA} = 40$ cm, $D_{AT} = 3$ cm ($D_{RT} = 43$ cm). At such a distance the tag was correctly charged but its response was not properly read. Figure 2.13 shows the signal received at the reader with and without the additional coil. As can be seen, the high Q_A affects the transient response. This causes that steady state is not achieved in each bit time (visible in the dashed line region of the waveform). Intersymbol interference then occurs preventing a successful reading.

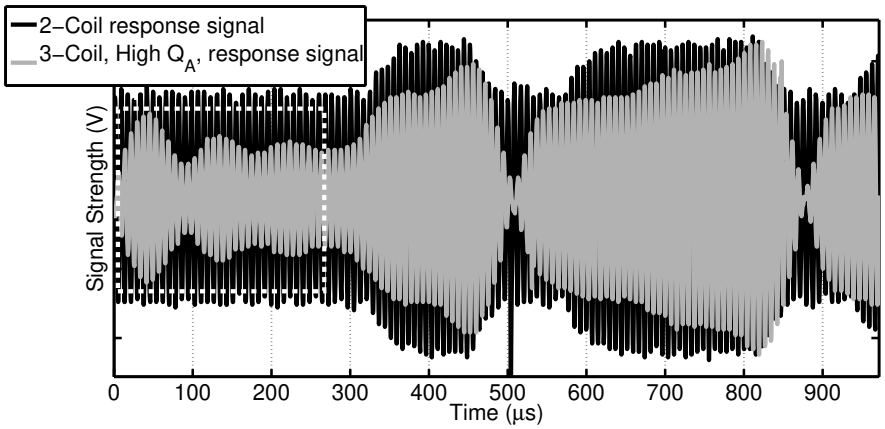


Figure 2.13: Part of the response signal (Measured) received by the reader (11101001). Without R_{QA}, no steady state is achieved and intersymbol interference occurs.

In order to solve this problem, R_{QA} was introduced. The additional coil quality factor can be reduced but not below the limit shown in Fig. 2.12. It was found that using $R_{QA} = 53$ kΩ, which results in $Q_{A_{@123.2\,kHz}} = 32$ and $Q_{A_{@134.2\,kHz}} = 29$, recovers the signal so that the reader decode the response.

Table 2.3 summarizes the design for the additional coil and the modification proposed for the reader.

At higher D_{RT} distances ($D_{RT} > 43$ cm), the minimum Q_A needed for successfully charging deteriorates the transient response and it was impossible to read the

Table 2.3: Final design.

$f_{res_R} = 126.7$ kHz ; $C_R = 3.56$ nF	no R_{QR}
$L_A = 648$ μH; $R_{QA} = 53$ kΩ	$r_A = 13$ cm
$f_{res_A} = 134.2$ kHz ; $C_A = 2.17$ nF	L_A 40 turns, .9 mm diameter
$R_{pA} = 11.0$ Ω @123.2 kHz	$R_{pA} = 13.3$ Ω @134.2 kHz

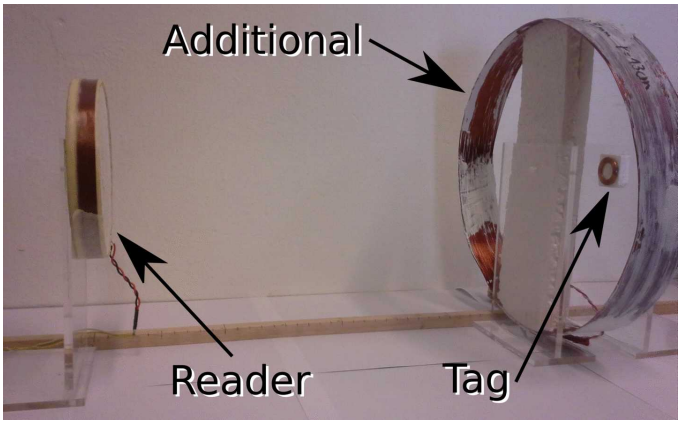


Figure 2.14: Measurement set-up. Different distances between coils (D_{RA} and D_{AT}) and the possible practical implementation are discussed in the text.

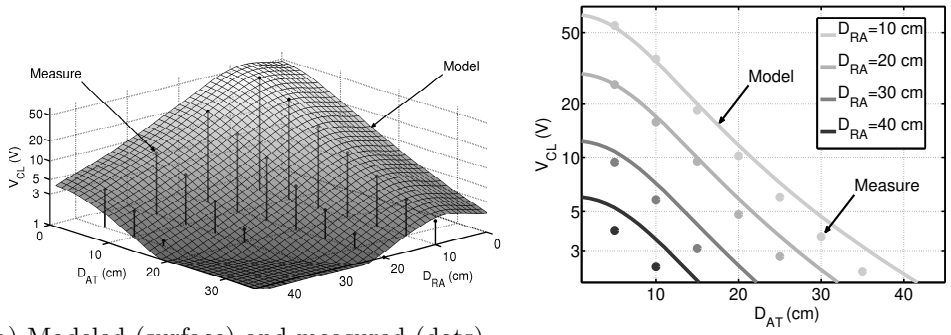
tag. The system without R_{QR} is capable of energizing the tag up to $D_{RT} = 46$ cm ($D_{RA} = 42$ cm $D_{AT} = 4$ cm), however, the tag response is not correctly decoded.

2.2.6 3-coil RFID link measurements

In this section, the measurements of the 3-coil system designed in Section 2.2.5 (Fig. 2.8, Table 2.2 and Table 2.3) are presented. The tag circuit shown in Fig. 2.8h was implemented using off the shelf discrete elements which allowed us to measure V_{C_L}. The read distance of an actual tag, Fig. 2.8c, was measured and compared with the model predictions. Figure 2.14 shows the measurement set-up.

Figure 2.15 compares V_{C_L} for the model and measurements for different distances between the coils (D_{RA}, D_{AT}). The measurements were done after the 50 ms of the charging phase. As can be seen, the analytical model and measurements are in good agreement considering the simplifications made. The model does not consider the voltage drop at the rectification diode and cross coupling between the reader and the tag k_{RT}. Additionally, inaccuracies in the value of the coil resonant frequency, quality and coupling factors directly alter V_{C_L}.

Figure 2.16 shows the regions where $V_{C_L} > 5$ V (charging limit), and the regions where the 1 and 0 bit amplitudes are higher than 10 mV_p, for different positions of the coils (D_{RA}, D_{AT}). All the points (D_{RA}, D_{AT}) that fulfill the charging limit ($V_{C_L} > 5$ V) also verify the limit for reliable detection of both bits



(a) Modeled (surface) and measured (dots).

(b) Cross-sections of (a) for four D_{RA} values.

Figure 2.15: V_{C_L} modeled and measured.

($V_{R_S} > 10\,\mathrm{mV}_p$). Thus, the read distance is limited by the charging phase. The dashed lines on Fig. 2.16 highlight the points with constant $D_{RT} = D_{RA} + D_{AT}$. Using Fig. 2.16 it is possible to identify all the different (D_{RA}, D_{AT}) configurations where the tag is read.

The maximum read distance of an actual tag for different distances between the reader and the additional coil, D_{RA}, is also presented in Fig. 2.16. The point where the highest D_{RT} distance is achieved is $D_{RA} = 40$ cm, $D_{AT} = 3$ cm.

In summary, these results show that the system was correctly modeled and verify the correctness of the proposed design approach.

The dash-dot line in Fig. 2.16 corresponds to the reading distance $D_{RT} = 16$ cm of the 2-coil system. Any point over this line corresponds to a configuration that has a larger read distance than the original 2-coil RFID system. Therefore, regarding the cattle identification application, the results show that the distance can be significantly increased both by using the additional coil closer to the reader (like an extension of the reader) or closer to the tag (either a modified tag with an extension or a fixed additional coil close to a place where the animals pass by).

2.2.7 Conclusion of Section 2.2

The enhancement of a half-duplex, FSK, RFID system through the application of an additional resonant coil was modeled taking into consideration both phases, charging and reading. It was shown that high values of the additional coil quality factor Q_A, in spite of reducing the system bandwidth, make both bit amplitudes received by the reader to increase. Therefore, we demonstrate that the reduction in bandwidth is not a problem from the point of view of attenuation of the transmission frequencies in the reading phase. However, the transient response is affected by high additional coil quality factor Q_A. The results of this study demonstrate that a trade-off exists between achieving high steady state amplitude and reducing intersymbol interference. The results of the model were applied to the design and test of a 3-coil RFID. The test system applied a commercial tag (RI-INL-R9QM widely used in cattle identification), a reader (using a TMS3705) and additional resonant coil (whose radius and quality factor were optimized). The

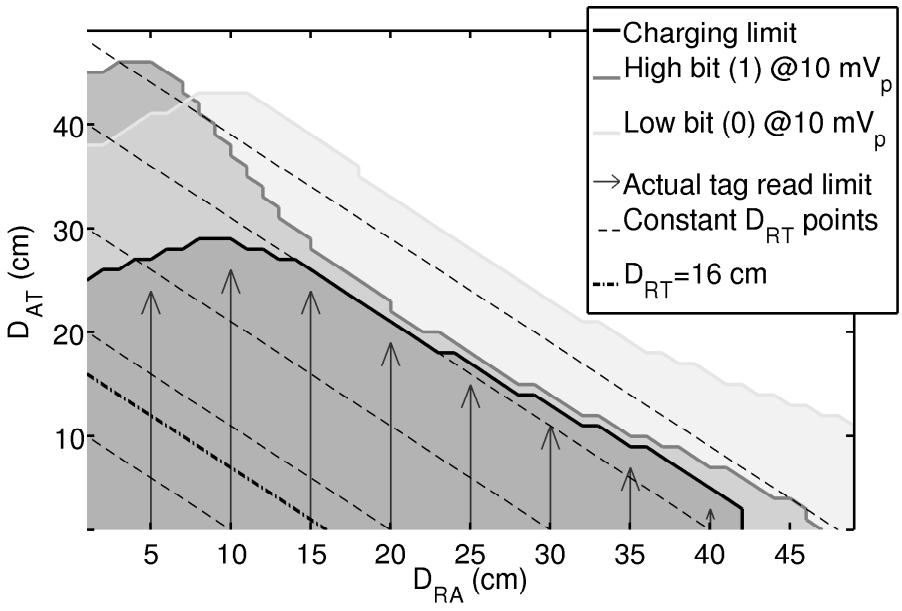


Figure 2.16: Read limits, modeled and measured with actual tag.

designed system increases almost 2.7 times the original 2-coil RFID read distance (from 16 cm to 43 cm). The analytic design predictions and measurements are in good agreement, thus validating the presented modeling approach. The design procedure can be applied not only to other RFID system but also to other systems that use the same channel to wirelessly energize and transfer data such as some implantable medical devices.

2.3 Influence of the titanium case used in AIMDs on the WPT link

Biocompatible materials are used to cover the AIMDs. Parylene or medical-grade silicone can be used to coat the device [56]. In devices that shall be implanted for long-term, titanium is widely used as the main enclosure due to its hermeticism. This material is often alloyed, and different grades exist.

When a WPT system is designed for an AIMDs, the effect that the human tissue has in the magnetic link (including the electrical characteristics of coils) should be considered as it was done in [56] and [57] among others. However, the effect that a titanium case has in this link can be much more important as shown in [58], and it has not been so widely studied. In [58], it was proposed to use a ferrite layer as a magnetic shield between the receiver coil and the titanium case. Another option is to separate the receiver coil from the titanium case, the optimal separation distance was addressed in [59]. Nonetheless, as far as we know, the influence that different titanium alloys have on the link efficiency has not been addressed in previous works.

Different titanium alloys (grades) present different electrical resistivities. In this section, we study how the titanium resistivity affects the link efficiency. It is shown that a worst resistivity exists that minimize the link efficiency. A simplified electrical model is developed to understand this effect and quantify its impact on the receiver coil quality factor. It is validated by simulations and measurements, that significant variations in the link efficiency exist when the titanium grade of the receiver case is changed. Therefore, this section provides a simple analysis to understand the effect that different titanium grades have in a WPT system used for AIMDs.

This section is organized as follows. First, in Section 2.3.1 a simplified analysis is presented modeling the effect and impact of the titanium case in the efficiency. Simulation of coils in the presence of titanium, using CST, and its corresponding measurements results are presented in Section 2.3.2. Finally, the main conclusions of this Section 2.3 are drawn in Section 2.3.3.

2.3.1 Conductive foreign object: theoretical analysis

The efficiency that can be achieved in a 2-coil WPT link [21] is

$$\eta_{Link_{MAX}} = \frac{{k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX}}{(1 + \sqrt{{k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX}})^2}. \tag{2.42}$$

This maximum efficiency ($\eta_{Link_{MAX}}$) was previously deduced in (2.18) and (2.19). An increase either in the coupling factor or the quality factors will improve the link efficiency (2.42), therefore these factors should be maximized during the design of the coils.

The coupling factor is mainly determined by the coils size, shape, orientation and separation. Additionally, the presence of the titanium case affects the magnetic field distribution also affecting $k_{TX\text{-}RX}$ and thus the link efficiency. How this titanium case affects the magnetic field depends on its size, position, working frequency, and conductivity. For instance, if the conductivity and working frequency impose a skin depth lower than the titanium case thickness, the magnetic field cannot go through the case. However, for higher values of resistivity, or a lower working frequency, it could be possible for the magnetic field to go through the case.

Regarding the coil quality factor ($Q = wL/R$), it depends on the ratio between the coil reactance and its equivalent series parasitic resistance. The presence of the titanium case, near the receiver, can be modeled as explained below.

The magnetic field surrounding the receiver induces current on the titanium case. At first approximation, this case can be modeled as a third coil (L_C) magnetically coupled with the receiver coil [60]. In order to calculate how the Q_{RX} is affected, the reflected impedance in it from the titanium case is calculated using the RLT [25]. A schematic of this model is shown in Fig. 2.17. The reflected impedance (Z_{ref}) can be calculated as

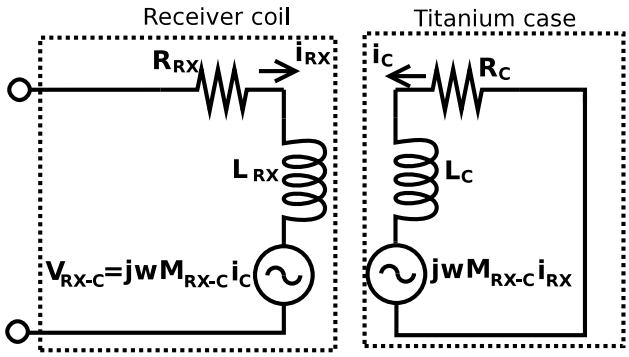


Figure 2.17: Equivalent model to estimate the effect of the titanium case on the receiver coil quality factor (Q_{RX}).

$$Z_{ref} = \frac{V_{RX\text{-}C}}{i_{RX}} = \frac{jwM_{RX\text{-}C}i_c}{i_{RX}} = \frac{M_{RX\text{-}C}^2 w^2}{jwL_C + R_C} \Rightarrow$$
$$Z_{ref} = \underbrace{\frac{M_{RX\text{-}C}^2 w^2 R_C}{(wL_C)^2 + R_C^2}}_{Re\{Z_{ref}\}} - j \underbrace{\frac{M_{RX\text{-}C}^2 w^3 L_C}{(wL_C)^2 + R_C^2}}_{Im\{Z_{ref}\}}. \tag{2.43}$$

Then, using Z_{ref}, the equivalent receiver quality factor ($Q_{RX\text{-}eq}$) can be calculated as

$$Q_{RX\text{-}eq} = \frac{wL_{RX} - Im\{Z_{ref}\}}{R_{RX} + Re\{Z_{ref}\}}. \tag{2.44}$$

It can be seen from (2.43), that in this simplified analysis, the real part of Z_{ref} ($Re\{Z_{ref}\}$) is maximum when $R_C = wL_C$ while the imaginary part ($Im\{Z_{ref}\}$) is a monotonic decreasing function of R_C. Therefore, different titanium grades, have different R_C, and thus have different effects on Q_{RX}. For instance, if we assume, to simplify the discussion, that $wL_{RX} >> Im\{Z_{ref}\}$ (low coupling between the receiver coil and the case), $Q_{RX\text{-}eq}$ is minimum when $R_C = wL_C$. This means that it may exist a material whose resistivity minimize the receiver coil quality factor and thus the link efficiency. An example of this situation is shown in Section 2.3.2.

During the previous discussion, many approximations have been done. For instance, a change in the material resistivity might also affect the self-inductance of the case L_C and its coupling with the receiver coil $M_{RX\text{-}C}$, as it might alter the current distribution through the case, depending also on the skin depth value. However, the goal of this section is not to find precise analytical relationships, as it depends on the particular situation under study. The aim of this discussion was to show that the effect that the titanium case has on the link strongly depends on its resistivity. Additionally, it was shown that it might exist a Worst Case Resistivity (WCR), which minimizes the receiver quality factor and thus the link efficiency. Note that this WCR depends on the working frequency w, even assuming constant values for the electrical parameters on the equivalent model.

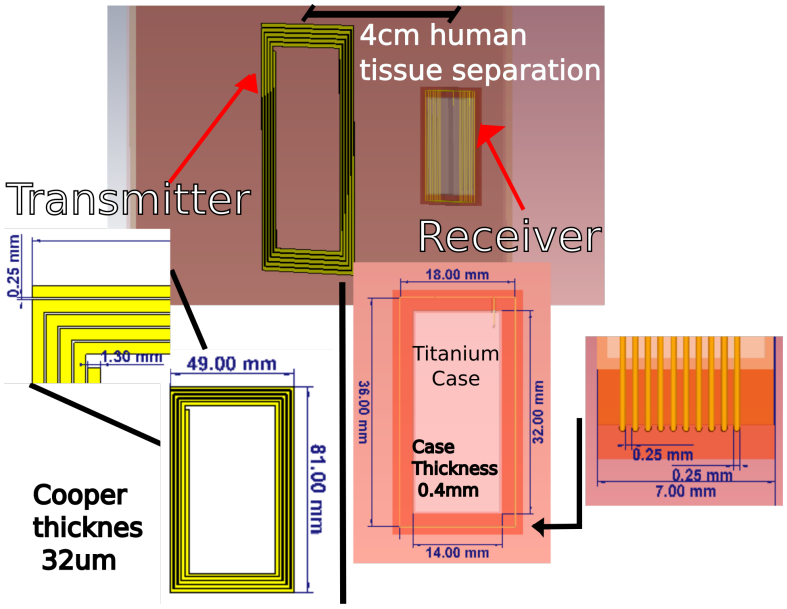


Figure 2.18: CST simulation model.

In the next Section 2.3.2, a WPT link for AIMDs working at 13.56 MHz is presented. The effect of the case resistivity on the coils coupling and quality factor is simulated using CST. Additionally, measurements with different titanium grades are presented. Therefore, the discussion of this section is validated and the existence of a WCR, which minimizes the link efficiency, is proved in an actual system.

2.3.2 Simulation and measurement results

The designed transmitter and receiver coils are presented in Fig. 2.18. The transmitter is a 5-turn printed spiral coil while the receiver is a 10-turn spring coil around the titanium case and separated 2 mm from it. The distance between the transmitter and the receiver was fixed at 4 cm, and the working frequency is 13.56 MHz. The design details of this link are not presented because it is a proof-of-concept system and our aim is to analyze how the titanium conductivity affects it.

The CST model showed in Fig. 2.18 was simulated sweeping the resistivity of the AIMD case. The coils coupling factor ($k_{TX\text{-}RX}$) between transmitting and receiving coils and the receiver quality factor Q_{RX} as a function of the case resistivity are presented in Fig. 2.19. Due to low coupling, the transmitter quality factor is almost not altered by the AIMD case resistivity and it is $Q_{TX} \simeq 80$.

For large values of case resistivity, the magnetic field can go through the AIMD case, thus increasing $k_{TX\text{-}RX}$ (Fig. 2.19).

As shown in Fig. 2.19, a WCR exists, in this case at around 100 $\mu\Omega$m, as discussed in Section 2.3.1.

The receiver coil quality factor was measured in the three cases indicated in

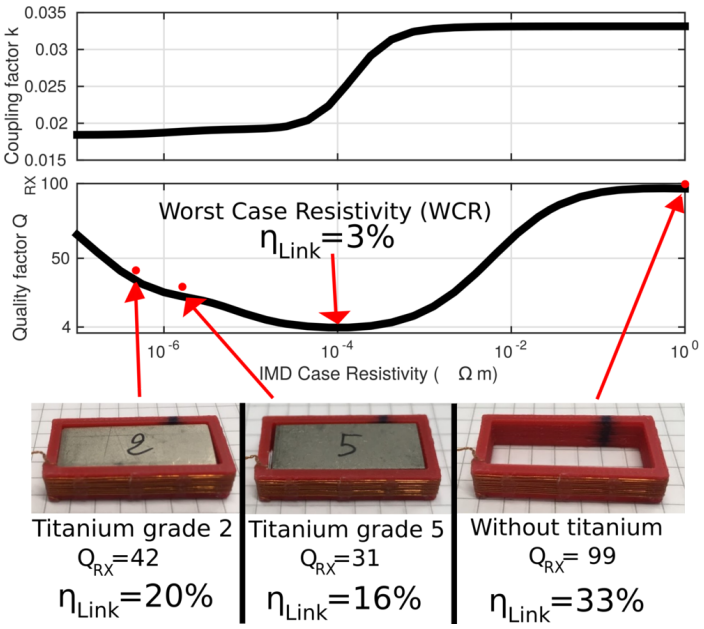


Figure 2.19: CST simulations and measurements of coupling factor ($k_{TX\text{-}RX}$) between TX and RX, and RX quality factor (Q_{RX}) as a function of the AIMD case resistivity. Working at 13.56 MHz. The RX coil pictures were taken over a 5 mm $\times$ 5 mm square grid pattern.

Fig. 2.19, using titanium grade 2, grade 5 and without titanium case. The titanium resistivities were measured obtaining 476 nΩm for grade 2 and 1.63 $\mu\Omega$m for grade 5. The case without titanium corresponds to the case with a quasi-infinite resistivity. As can be seen, both grades of titanium have lower resistivities than the WCR, and a higher quality factor is obtained in the case of titanium grade 2.

This means that, if titanium grade 5 is used for the AIMD case at this frequency (13.56 MHz), the link efficiency from (2.42) is $\eta_{Link} = 16\%$. On the other hand, if titanium grade 2 is used, the efficiency from (2.42) is $\eta_{Link} = 20\%$. Therefore, the link efficiency can be improved by 4% by changing the titanium grade of the AIMD case. If a material with the WCR is used, the efficiency from (2.42) is $\eta_{Link} = 3\%$. These results highlight the importance of carefully taking into account the case resistivity.

2.3.3 Conclusion of Section 2.3

The influence of the AIMD case resistivity on the WPT link efficiency was addressed. Since titanium is an electrical conductor, it affects both the coupling and quality factor, thus changing the electromagnetic link efficiency. The lower the link efficiency is, the higher the power dissipated is, which is totally undesired in AIMDs. The link efficiency using titanium grade 2 and grade 5 for the AIMD case was compared. It was shown that, at 13.56 MHz, the link efficiency is less affected by titanium grade 2, which is a better conductor than grade 5. This may be a non-intuitive result at first hand, and that if overlooked might lead to inappropri-

ate design decisions, thus highlighting the importance of taking into account the analysis presented in this section.

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Chapter 3

Receiver circuits analysis

The RX could be totally passive in applications where the load requires an ac voltage such as light bulbs or heating elements. However, in most applications, a dc regulated voltage is required. Therefore, as shown in Fig. 1.2, a rectifier and a dc-dc converter are included for this purpose.

The power losses in the RX not only reduce P_L but also generate heating which is totally undesired in applications such us AIMDs. For this reason, achieving high efficiency in the RX-circuits is crucial.

This chapter analyzes the design of different circuits used in the RX. First, in Section 3.1, switched capacitor step-up dc-dc converters are discussed especially focused on the switches design. The architecture of a low-power high slew rate OTA is presented in Section 3.2. This OTA was designed as a part of the feedback loop of a dc-dc converter. Later, in Section 3.3 we address the design of an active rectifier. Finally, in Section 3.4 a mixed block that rectifies and increases the voltage is analyzed. All the circuits are designed, and the OTA was fabricated, in a 130 nm CMOS technology.

The proof-of-concept circuits of each section are not directly related. However, all the circuits are oriented towards the development of high-efficiency low-power applications.

3.1 Step-up dc-dc converters

A dc-dc converter in the RX can adjust Z_{MN} and increase η_{Link} (Fig. 1.2), this usage is further studied in Chapter 4. Instead of adjusting Z_{MN}, the dc-dc converter in the RX could regulate the output voltage if a control feedback loop is included. In Chapter 5, a system that uses a dc-dc converter to regulate the output voltage is analyzed. Additionally, in Chapter 5, a dc-dc converter is used in the TX to adjust the input voltage of the inverter. Therefore, the dc-dc converter is an important block, used in both TX and RX, with different goals.

The dc-dc converters can be divided between inductor-based and switched-capacitor converters. Inductor-based converters reach good efficiencies and high output power even with low input voltages. However, most inductors cannot be

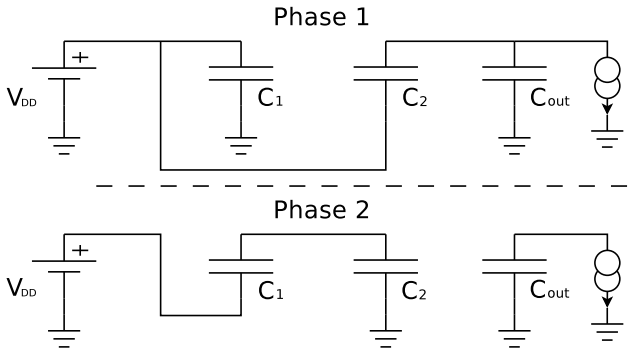


Figure 3.1: Dickson step-up dc-dc converter.

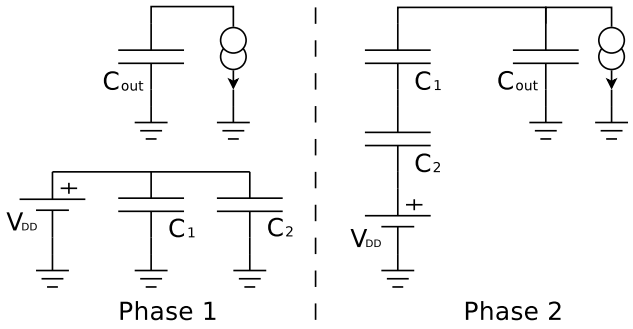


Figure 3.2: Series-parallel step-up dc-dc converter.

integrated which increases the device size [61–64]. In a switched-capacitor, only capacitors and switches are used which makes them suitable for integration. To achieve a lightweight and small size is a key requirement in many applications, so the design of a fully integrated converter has been the main goal of many works.

A switched capacitor step-up dc-dc converter is usually referred to as a Charge Pump (CP). Many different CP architectures have been proposed such as Dickson Fig. 3.1 [65–72], Series-Parallel [73, 74] (shown in Fig. 3.2 and is further discussed in Section 3.1.2), Cockcroft–Walton [75], Fibonacci [76], Doubler [77–79], among other variations. Regardless of the architecture, a CP consists in switching the capacitors and voltage source interconnections, usually between two (or more) states (or phases), with the aim of obtaining an output voltage higher than the source one. In a step-up converter, the implementation of the switches that perform the interconnections is not as simple as in a step-down one, this issue is addressed in Section 3.1.1.

Most of the implemented CPs are based on Dickson topology [65] (the first that was used in an integrated circuit as is highlighted in [80]). Although the original circuit used diodes, in modern implementation these were replaced by MOS transistors [66].

On the other hand, the series-parallel (Fig. 3.2) CP has not been so widely used. This architecture allows us to get various conversion levels [73]. [81] presents a useful comparison between different CP architectures in fast switching limit

(FSL, when the resistance of the switches dominates the output impedance of the converter) and slow switching limit (SSL, when the resistance of the switches has a negligible effect in the output impedance of the converter, which is dominated by the capacitance value). It is shown that Series-parallel CPs present the best performance in terms of output impedance, and hence conduction losses and efficiency, in SSL. Ultra-low power converters usually operate in this region as output impedance is adjusted to the load by changing the switching frequency.

Additionally, the series-parallel CP has traditionally been the main architecture for stimulation circuits in many implants, such as cardiac pacemakers [82–84], where an external, stimulation tank capacitor of some microFarads is charged to a voltage that may be higher than the battery voltage. Therefore the results presented in this work are also applicable in that context.

Independently of the converter architecture, all step-up CP converters need special solutions, as will be discussed in Section 3.1.1, for handling some of the switches that need to operate outside of the power supply rails. This section addresses this problem and presents a step-up dc-dc converter, based on the series-parallel architecture (shown in Fig. 3.2), that multiplies by three the supply voltage. A solution for the implementation of the switches in the case of this converter architecture is presented. The switches presented use the same general structure that the Dickson architecture of [85], but modified for a series-parallel converter. The proposed switches are driven from the input voltage and do not need an auxiliary charge pump. Their design improves the efficiency by recycling charge and optimizing the gate swing. The converter can start-up with the load connected without any additional mechanism.

The section is organized as follows. First, the challenges and solutions related to the implementation of over the supply rail switches in a step-up CP converter are reviewed in Section 3.1.1. Section 3.1.2 presents the series-parallel architecture studying the requirements of each switch. In Section 3.1.3 the proposed switches are presented. The circuit in charge of generating the needed control signals is analyzed in Section 3.1.4. Simulation results and comparisons with other works can be found in Section 3.1.5. Finally, Section 3.1.6 summarizes the main conclusions of this analysis.

3.1.1 Switches in a step-up converter

Either using a Dickson type charge pump architecture or a simple series-parallel converter, a key issue lies in how to design the switches, being more critical in the series-parallel converter [80]. The simplest use of an ordinary switch (Fig. 3.3) requires to have available a power supply equal to the highest voltage to be handled by the switch, i.e. it operates within the power supply rails. Otherwise, it cannot be turned off and/or it will present a high impedance when it is on. NMOS and PMOS have different behaviors. The PMOS gate has to be higher than both A and B nodes (Fig. 3.3) in order to turn it off, but can be easily turned on connecting its gate to ground. NMOS however, needs a voltage over A or B to be turned on while it is turned off just setting its gate to ground. Furthermore, the PMOS

substrate connection must be connected to a voltage higher than A and B, in order to avoid direct conduction of the drain-substrate or source-substrate junctions. As a result, ordinary switches cannot be driven from the input voltage on a step-up converter.

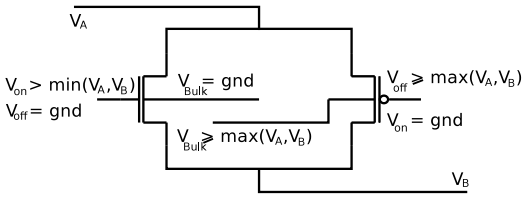


Figure 3.3: Ordinary switch voltage ranges. V_A and V_B are supposed to be above ground. Conditions consider also conduction in weak inversion (sub-threshold) regime.

The solutions reported in the literature to solve these problems can be summarized in four main different approaches, which are presented in Fig. 3.4 and are discussed in the remaining of this section. The first one, depicted in Fig. 3.4 A, powers the logic that drives the switches from the output node [70, 71]. This approach allows using standard circuits to control the gates in a step-up converter as the switches operate within the supply rails of the control signals. Additionally, in steady state, the switches are driven from a higher voltage than if they were driven from the input. This yields smaller resistance and allows to deliver more power to the output. However, an auxiliary block is necessary at start-up when no output voltage is available. [70] proposed, using this method, a converter with 120 mV input and 770 mV output with an efficiency of 38.8%. To kick start from such a low voltage an additional logic and extra switches powered from the input source are used until the output voltage reaches 300 mV.

A variant of this method (shown in Fig. 3.4 B) includes logic powered from the input and a level shifter powered from the output or an intermediate stage in order to drive the switches [72, 77, 78, 86, 87]. As the logic usually consists of a ring oscillator, by powering it from a constant supply voltage instead of powering it from the output avoids the dependency of the frequency on the output voltage value. In this approach, the correct start-up of the circuit must be checked, but it can be achieved by simpler means than in the previous case. When the output

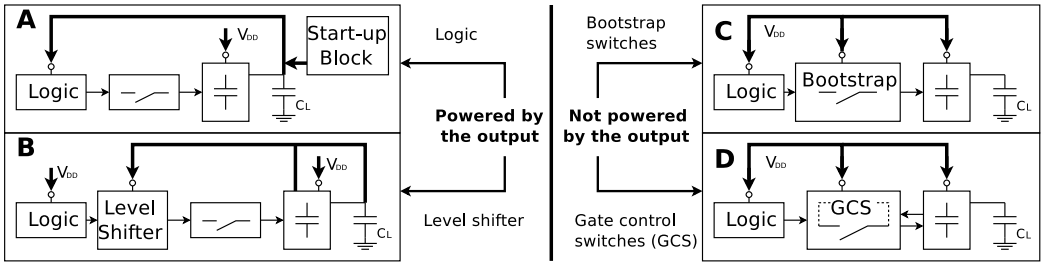


Figure 3.4: Summary of different step-up converter's switches approaches. V_{DD} is the input voltage. References: A [70, 71], B [72, 77, 78, 86, 87], C [79, 88], D [67–69, 75, 89] and this work.

voltage is used to power a block of the converter, a parasitic feedback loop is generated which has to be taken into account.

The third approach (Fig. 3.4 C) for over the supply rail switches is the bootstrap technique, know also as bootstrap-switches [79, 88] or bootstrap charge pump [80]. It elevates the voltage of the power switch gate, working as a small auxiliary CP to control each switch. The phases of these auxiliary CPs are interleaved with the main CP phases so that the switches of the auxiliary CP can rely on the output or intermediate voltage of the main CP to be driven. These architectures add several transistors and capacitors adding complexity to the converter and jeopardizing efficiency.

The fourth approach (schematically depicted in Fig. 3.4 D), refers to the case when the voltages that are supplied by auxiliary CPs in the bootstrap approach are instead opportunistically obtained from voltages available in the own converter. This approach has been applied in Dickson CPs. The original architecture proposed by Dickson in 1976 [65] used diodes instead of switches. However, the reduction in output voltage (and efficiency) generated by the use of diodes is unacceptable in low input voltage applications.

Nowadays ad-hoc connections are made using the internal charge pump nodes to turn on and off each switch avoiding diodes to be used [67–69, 75, 89]. These ad-hoc connections are all actually based on the gate control strategies described in [85]. The easiest implementation of these ad-hoc connections is achieved when an internal node of the converter (represented by V_{AUX} in Fig. 3.5 A) can be directly used to control another switch, as in [68, 75]. Nevertheless, this is possible just in some particular architectures and switches. When it is impossible, gate control switches (GCS) [67, 69] are added to control the main switch, as shown in Fig. 3.5 B. In this figure, V_L and V_H are internal nodes of the converter used to drive the switch so that their voltages have to verify that $V_L < min(V_A, V_B)$ and $V_H \geq max(V_A, V_B)$ as was explained in Fig. 3.3. V_H can be connected to the maximum between V_A and V_B as in [67] (and this work, as will be discussed in Section 3.1.3) or to other internal voltage as in [69]. V_L could be ground, but if an internal node of the converter is used to discharge the power switch gate, as proposed in this work, its charge is recycled and efficiency is improved. The V_{OFF}, Fig. 3.5 B, is usually taken from another internal node whose value is lower than V_H when the main switch must be turned off and higher in the other case. V_{ON} could also be taken from an internal node (self-controlled switch) or from the control logic.

In Fig. 3.5 B and the associated discussion focused on the GCS for a PMOS, the problem to be solved is the turn off of the switch. Nevertheless, the same reasoning can be used to turn on an NMOS using internal voltages that are higher than the supply voltage.

Section 3.1.3 presents an implementation of the GCS approach in the context of the series-parallel architecture, improving efficiency through reduced gate swing and gate charge recycling.

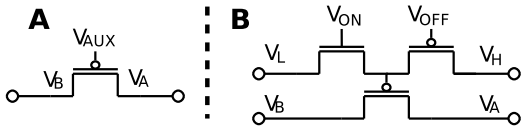


Figure 3.5: Summary of gate control switches ad-hoc connections. References: A [68, 75], B [67, 69] and this work.

3.1.2 Series-parallel architecture

Figure 3.6 shows the architecture of a series-parallel x3 step-up converter. In Phase 1 (Fig. 3.2 and Fig. 3.6), when the charge is taken from the source, $SWV_{DD}\{1,2\}$ and $SWgnd\{1,2\}$ are turned on while $SWi\{1,2\}$ and SWV_{out} are turned off. On Phase 2 (Fig. 3.2 and Fig. 3.6), the charge is being delivered to the load, $SWV_{DD}\{1,2\}$ and $SWgnd\{1,2\}$ are turned off whereas $SWi\{1,2\}$ and SWV_{out} are turned on. The status of all the switch in each phase is summarized in Table 3.1. Therefore, just two signals are needed to control the switches, one drives $SWgnd\{1,2\}$ and $SWV_{DD}\{1,2\}$ while the other drives $SWi\{1,2\}$ and SWV_{out}. These two signals must be non-overlapping so that short circuits are avoided.

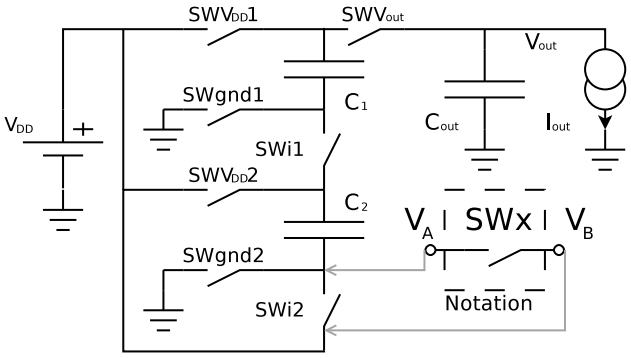


Figure 3.6: Series-Parallel step-up x3 converter.

Table 3.1: Status of switches of Fig. 3.6 in each phase.

Switch	Phase 1	Phase 2
$SWV_{DD}1$	ON	OFF
$SWV_{DD}2$	ON	OFF
$SWgnd1$	ON	OFF
$SWgnd2$	ON	OFF
$SWi1$	OFF	ON
$SWi2$	OFF	ON
SWV_{out}	OFF	ON

In order to define the requirements of the drive signal for each switch, Fig. 3.7 shows the terminal voltages of each switch in both phases. If $SWgnd1$ is implemented by an NMOS transistor, it can be easily turned off by setting its gate to gnd in any situation and is possible to turn it on charging its gate to V_{DD} since the source is at gnd (see Fig. 3.7). For the same reasons, $SWgnd2$ can be also implemented by a single NMOS transistor, therefore a special design for these switches is not necessary.

Figure 3.7 indicates that $SWi\{1,2\}$ can be implemented using just one transistor too. In this case, a PMOS fulfills the requirements as it can be turned off connecting its gate to V_{DD} ($V_A = gnd$, $V_B = V_{DD}$ see Fig. 3.7). As it was explained before, turn it on is not a problem. The substrate can be connected to the B node (the bottom node in Fig. 3.6) since this node is always at a higher voltage than A.

Consequently, the only switches whose design is tricky are $SWV_{DD}\{1,2\}$ and SWV_{out} and they are studied in Section 3.1.3.

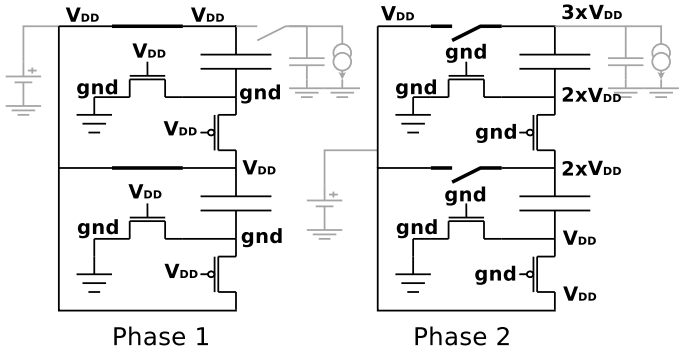


Figure 3.7: Nodes voltages in each phase.

3.1.3 Switches design

Firstly, the design of $SWV_{DD}\{1,2\}$ is detailed as it is easier to understand. Then in Section 3.1.3.2 the most challenging switch, SWV_{out}, is analyzed. The proposed architecture recycles the SWV_{out} gate charge, thus reducing losses. Losses are further decreased by minimizing the gate swing for both the $SWV_{DD}2$ and the SWV_{out} switches, as to turn them off the gate is charged to the lowest necessary voltage.

3.1.3.1 Switches to V_{DD}

The proposed switch for $SWV_{DD}\{1,2\}$ is depicted in Fig. 3.8. The power transistor is $M1$ while $M2$ and $M3$ drive the $M1$ gate. During Phase 1, Vin (Fig. 3.8) is set to V_{DD} thus $M3$ discharges the gate of $M1$, turning it on. Since in this Phase node B is lower than V_{DD}, $M2$ remains off (as indicated in Fig. 3.3). Therefore, node B is charged to V_{DD} in this cycle.

At the end of Phase 1, switches $SWV_{DD}\{1,2\}$ and $SWgnd\{1,2\}$ are turned off before $SWi\{1,2\}$ and SWV_{out} are turned on. Firstly, when Vin is set to gnd, $M2$ charges the gate of $M1$ to the voltage available in node B, thus $M1$ is now connected as a diode. Then, after $SWi\{1,2\}$ are turned on, node B rises but the diode connection of $M1$ prevents $M1$ from discharging node B. At start-up, or if the chosen working frequency is too high, node B may not be fully charged to V_{DD} during Phase 1. In that case, the charge may go through $SWV_{DD}\{1,2\}$ even during Phase 2 (from A to B). However, this behavior, instead of being a problem, makes the output node B to rise faster, as the charge is being taken from the source in both phases.

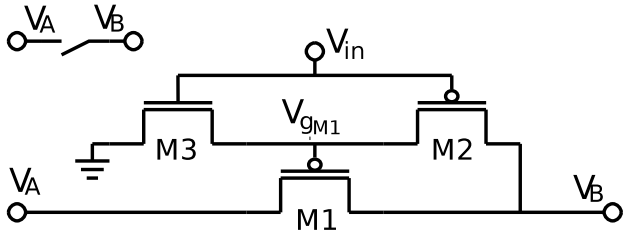


Figure 3.8: Proposed switch for $SWV_{DD}\{1,2\}$.

Transistors $M2$ and $M3$ do not change the converter efficiency as these two transistors were already included in the last stage of the inverter chain that drives the gate of $M1$. Furthermore, the gate of $M1$ is always at the minimum voltage necessary to cut $M1$ off, thus reducing its swing and improving the efficiency.

3.1.3.2 Switch to V_{out}

First, we are going to analyze why the switch designed for $SWV_{DD}\{1,2\}$ cannot be used to implement SWV_{out}. If the switch shown in Fig. 3.8 is used for SWV_{out}, $M2$ will never be off since its maximum Vg ($Vin = V_{DD}$) is always lower than node B (the output node, which goes up to $3V_{DD}$). Consequently, if the switch in Fig. 3.8 is used for SWV_{out}, in Phase 2 when SWV_{out} should be on, the output node is shorted to ground through $M2$ and $M3$ in the SWV_{out}.

In order to avoid this problem, the gate of $M2$ is connected to node A as is shown in Fig. 3.9. SWV_{out} is going to be turned on only when V_A is higher than V_B, otherwise the output node (V_B) is discharged. Therefore, when SWV_{out} is on ($Vin = V_{DD}$), $M2$ remains off as $V_A > V_B$. This avoids the direct path from the output node to ground occurring if the design of $SWV_{DD}\{1,2\}$ is used.

At the end of Phase 2, $V_A \simeq V_B$ and Vin are set to ground so $M3$ turns off, hence Vg_{M1} remains discharged but now floating. When the Phase 1 starts again, V_A of SWV_{out} decreases, turning on $M2$ ($V_A < V_B$) and charging the gate of $M1$, thus SWV_{out} is off as it is desired.

The charge used to drive the gate of $M1$ can be reused by connecting Vin and V_D as is shown in Fig. 3.10. So during Phase 1 $M3$ is off ($Vin = V_D = V_{DD} < Vg_{M1} = 3V_{DD}$) and $M2$ in on ($Vg_{M2} = V_A = V_{DD} < V_B = V_{out} = 3V_{DD}$), as a result SWV_{out} is off ($Vg_{M1} = V_{out} = 3V_{DD}$). At Phase 2, $M3$ is on ($Vg_{M3} =$

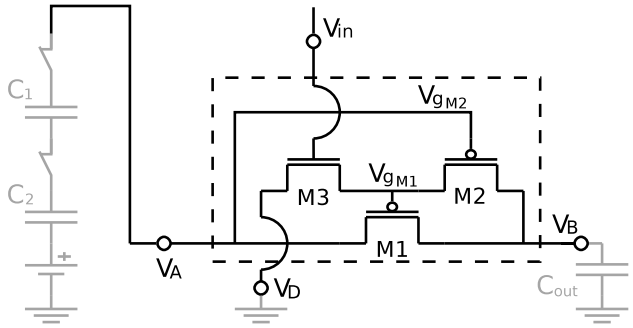


Figure 3.9: $SWVout$ without charge recycling.

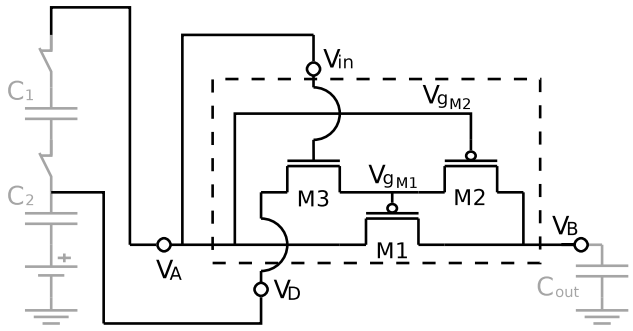


Figure 3.10: Proposed switch for SWV_{out} with charge recycling.

$3V_{DD} > V_D = 2V_{DD}$) and Vg_{M1} is discharged to $2V_{DD}$ so $M1$ is turned on since V_A and V_B are higher ($V_A = V_B = 3V_{DD}$ see Fig. 3.7). The sequence described is shown in the simulation results plotted in Fig. 3.12. Summarizing, Vg_{M1} will vary between $2V_{DD}$ and $3V_{DD}$. Instead of dumping the M1 gate charge to ground each time that Vg_{M1} changes from $3V_{DD}$ to $2V_{DD}$, this charge is used to refill C2. Therefore, SWV_{out} is self-controlled and its gate charge is recycled.

In switches $SWV_{DD}\{1, 2\}$ and SWV_{out}, the NMOS and PMOS substrates are connected to ground and the V_B node, respectively.

Using the proposed switches, in theory, any integer step-up ratio can be achieved by just changing the number of capacitors used. With extra SWV_{out} switches, a multiple output converter can also be implemented.

3.1.4 Control signal generation

Two non-overlapping signals are needed in order to control the converter. Fig. 3.11 shows a simplified schematic of the logic used to generate these signals. The switching frequency is generated with a 9-stage current-starved ring oscillator represented by the block Ring Oscillator in Fig. 3.11. The frequency of the ring oscillator is controlled through the signals $VContN$ and $VContP$. $VContP$ is generated in the block Control Voltage from the single input control signal $VContN$. Finally, a non-overlapping pulse generator followed by a buffer generates Phase1 and Phase2 signals.

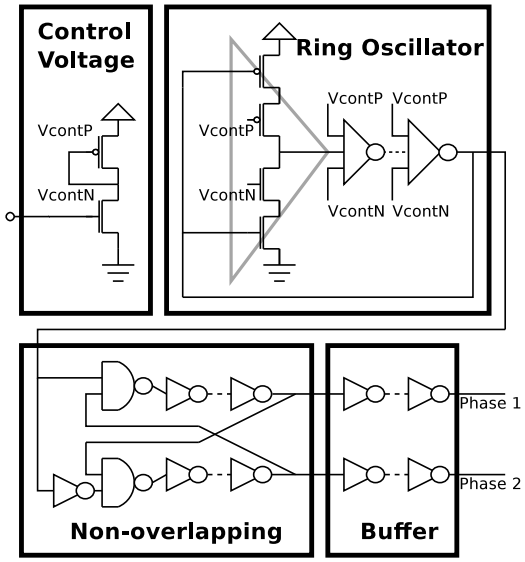


Figure 3.11: Control signal generation.

This logic block is capable of working powered from the input source even at the lowest start-up voltage of 200 mV. Its power consumption is taken into account in the reported overall efficiency.

3.1.5 Simulation results of a proof-of-concept circuit

The proposed step-up dc-dc converter was simulated in a 130 nm CMOS technology. The proof-of-concept system specifications were selected for ultra-low power (5μ A) and low input voltage (400 mV) applications.

The results prove that the switches are working as desired. The performance achieved by the converter is compared with the state of art in Table 3.2.

In order to demonstrate the behavior of SWV_{out}, Fig. 3.12 shows the simulated signals V_A, V_B, V_D and Vg_{M1} of Fig. 3.10. This simulation was done with $V_{DD} = 400$ mV, a switching frequency of 1 MHz (selected by simulation to achieve maximum efficiency) and an output current of 5 μA. The total capacitance used was 600 pF. As can be seen in Fig. 3.12 the output voltage is almost 1.1 V. The efficiency simulated was 81%, including the switching loss of the gate capacitance of all transistors and the control signal generation. The regulation feedback loop of the converter is out of the scope of this work and not considered in the predicted efficiency. Nevertheless, if the power consumption of the feedback loop components (voltage divider and comparator) reported in [66] are added the efficiency is reduced in 6% to 75%. Therefore the expected performance is very competitive with similar converters listed in Table 3.2.

To estimate the power savings by reducing the gate swing of the switches and recycling gate charge, the overall efficiency was recalculated assuming that all switches were driven with signals between gnd and $3V_{DD}$, as if the logic was powered from the output node (Fig. 3.4 A). In these conditions, the efficiency is

Table 3.2: Comparison with the state of art of the step-up dc-dc converter.

Reference	[61]	[67]	[68]	[89]	[66]	This work*	
Technology (nm)	350	130	180	250	130	130	
Start-up voltage (mV)	35	125	700	300	270	200	
External component	INDUCTOR	NO	NO	NO	NO	NO	
Input voltage (mV)	100	125	700	300	450	400	200
Output voltage (V)	1.8	$\simeq 0.35$	1.5	3.2	1.4	1.07	0.48
Output power/current	$\simeq 300$ μW	100 nA	4 μA	1 μW	5 μA	5 μA	100 nA
Switching frequency (kHz)	28.4	360	5000	1000	800	1000	50
Maximun efficiency (%)	58	62	55	68	65	81	66

* Simulation results

reduced by 3% (from 81% to 78%).

Figure 3.13 shows the simulated efficiency as a function of the output voltage for different output currents. The different output voltages are achieved by changing the switching frequency from around 100 kHz to 2 MHz.

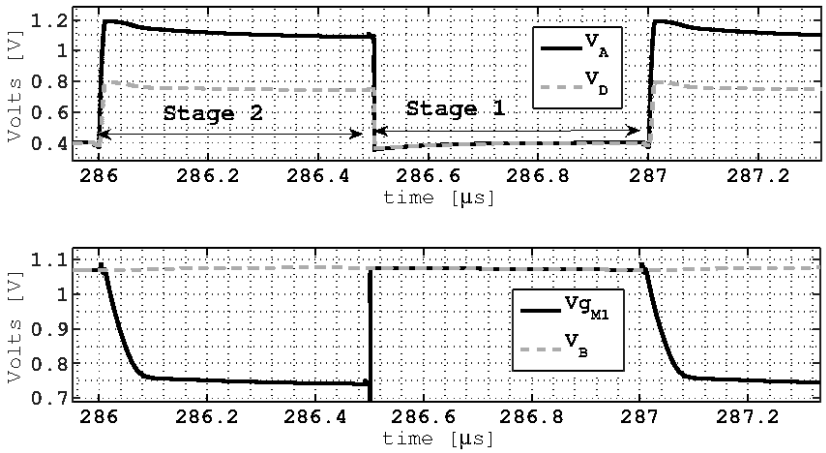


Figure 3.12: Simulated signals of SWV_{out}.

3.1.6 Conclusion of Section 3.1

The design of the gate control strategy for switches operating above the power supply rail has been presented in the particular case study of a series-parallel, 3x, ultra-low power, step-up dc-dc converter. A systematic procedure for identifying the requirements of each switch has been first presented, as well as a review of the main approaches presented in the literature for driving the switches. Then the switches that required special solutions have been addressed. It has been shown how, starting from a basic structure, the gate and drain-source terminal voltages of the auxiliary switches can be handled so that the gate swing of the main switch is minimized, thus saving energy. Additionally, the gate charge of the main transistor in one of the proposed switches is recycled, thus providing further energy saving.

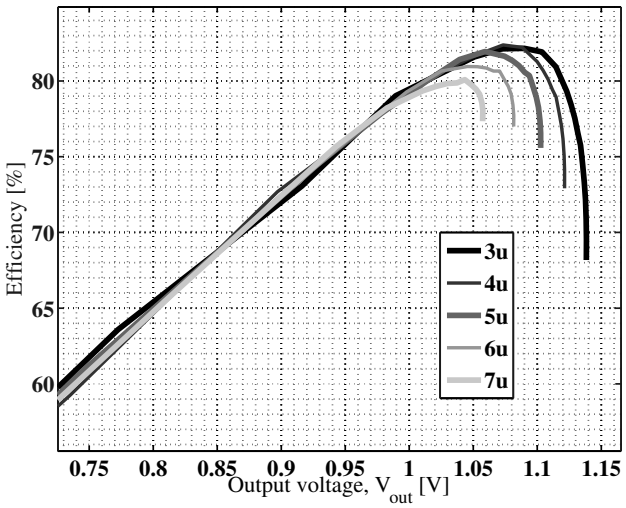


Figure 3.13: Efficiency as a function of output voltage V_{out}(changing the switching frequency) for different output currents (I_{out}).

A proof-of-concept converter was designed and simulated, achieving an efficiency of 81% (without considering the feedback loop consumption) at V_{in} = 400 mV and 5 μA load current and operating down to V_{in} = 200 mV.

3.2 Low-power operational transconductance amplifier

The OTA is probably one of the most elementary and widely used circuits. For instance, an OTA can be used in the feedback loop of a dc-dc converter to regulate its output voltage.

In this section, we address the design of an OTA for low-power applications. Additionally, we use the proposed architecture in the design of a non-symmetrical OTA which is part of the feedback loop of a switched-capacitor dc-dc converter. This circuit was fabricated in 130 nm and experimental results are presented.

This section is organized as follows. Section 3.2.1 introduces the trade-off between the OTA bias current and its slew-rate. Section 3.2.2 presents a proposed non-linear current mirror that will be applied for slew rate enhancement. Section 3.2.2 also presents two other architectures [90,91] that will be compared with the proposed one. In order to thoroughly compare the proposed architecture, we designed our circuit using the same technology (0.5 μm), bias current and output capacitance that were applied in the publications that presented the other alternative architectures. The results of this comparison are shown in Section 3.2.3. General issues regarding the stability of the proposed non-linear current mirror are addressed in Section 3.2.4. An application of the novel architecture in an OTA that is part of the feedback loop of a switched-capacitor dc-dc converter is analyzed in Section 3.2.5. Section 3.2.6 presents the measurement results of this circuit. Finally, the main conclusions of the section are drawn in Section 3.2.7.

3.2.1 Trade-off between bias current and slew-rate

The OTA is a widely used block and its power consumption has been extensively studied. A key drawback, regarding power consumption of classic (class-A) OTAs, is the direct dependence of slew-rate on quiescent consumption. As the slew-rate directly depends on the maximum output current and, in a class-A OTA this is determined by the bias current, a high slew-rate can only be achieved by increasing static power consumption.

Many architectures have been proposed with the aim of reducing quiescent current without jeopardizing slew-rate. Basically, the idea behind is to enhance the slew-rate when it is needed. These architectures can be divided into two categories. The first, known as adaptive biasing was proposed by [92] and consists in increasing the bias current when the differential pair is unbalanced. On the other hand, when a small differential input signal is applied, the bias current is maintained small in order to reduce static power consumption and preserve stability. Based on this idea, many architectures have been reported. These architectures dynamically change the bias current with the differential input signal in order to fulfill low static power consumption, and high slew-rate [92–98]. In [96, 97] comparisons between different adaptive biasing circuits, referred to as class-AB input stages, are done.

In the particular case of a symmetrical OTA, the second way of enhancing slew-rate maintaining a low static power consumption consists in dynamically changing the current mirror's copy ratio as it is shown in Fig. 3.14. In these architectures, a 1:1 copy ratio is maintained at small input signal. In contrast, when a large signal is applied, the copy ratio is increased and a high slew-rate is achieved. Therefore, this block works as a slew-rate ameliorative, increasing the output current above the bias current when it is needed. Different architectures have been proposed in order to greatly increase this ratio adding a degeneration resistance [90, 91, 99]. Some works use both techniques together (Fig. 3.14) conforming a so-called "Super Class-AB OTA" [91].

In this section, a Super Class-AB OTA which uses a novel non-linear current mirror based on a self-controlled degeneration resistance is proposed. We have originally presented the basic idea in [2] (with a later extended version in [4]), and others works have also used it like [100]. The simplicity of the proposed architecture reduces not only the quiescent current consumption but also the required area. Moreover, it simplifies the implementation of layout matching techniques in comparison with previously reported architectures, as all transistors that require matching are equally sized.

3.2.2 Non-linear current mirrors

In this section, some of the most used non-linear current mirrors are studied and compared with the proposed architecture. All the non-linear current mirrors that are shown in Fig. 3.15 are supposed to be used in the OTA of Fig. 3.14.

The first architecture, shown in Fig. 3.15a, was proposed by [90]. Considering that $R_{1,2}$ have a much lower value than $r_{o_{4,5}}$ (where $r_{o_{4,5}}$ are the small signal drain

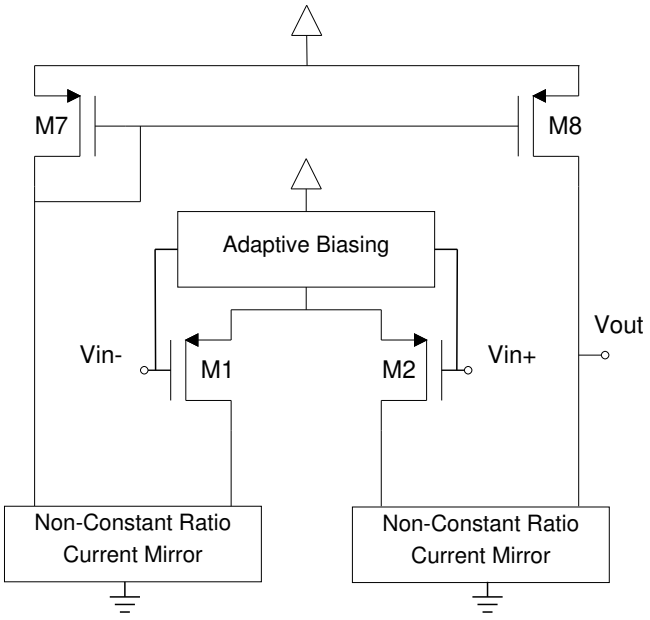


Figure 3.14: Super Class-AB OTA with non-linear copy ratio and adaptive bias.

source resistance of M4 and M5), when a differential input voltage v_d is applied, a $gm_{1,2}.v_d/2$ current flows through $R_{1,2}$ generating small signal variations at nodes V_L and V_R ($v_l = -v_r = R_{1,2}.gm_{1,2}.v_d/2$) while maintaining V_C constant (virtual ground). In consequence, $R_{1,2}$ enhance the voltage variation at nodes V_L and V_R increasing one current mirror copy ratio while reducing the other in order to rise the output current. On the other hand, when no differential input is applied, no current flows through $R_{1,2}$ and the mirror keeps a 1:1 copy ratio. The main disadvantage of this architecture is that $R_{1,2}$ need to be integrated. Moreover, if they are implemented using transistors as in [90] an extra bias voltage has to be generated.

In [91], three different non-linear current mirrors which achieve similar ac characteristics while increasing slew-rate are presented. However, all of them need additional bias currents or voltages which tend to increase quiescent power consumption. We selected the architecture depicted in Fig. 3.15b to do an in-depth comparison, due to its similarity to our proposed architecture.

In the architecture of Fig. 3.15b, M11 and V_b are designed in order to maintain M11 at the ohmic region (near to saturation) while no differential input is applied ($I_R = I_B/2$). Under this condition, approximately a 1:1 copy ratio is achieved by properly selecting M5 and M6 aspect ratios. When a differential input voltage is applied, I_R increases and M11 turns to saturation region (if it is well designed) increasing its drain source resistance dramatically and in consequence boosting the copy ratio and the output current.

The proposed architecture is shown in Fig. 3.15c [2,4]. Neither additional bias

branches nor bias voltages are needed, which is a key issue to maintain a very low quiescent current. If no differential input voltage is applied, the proposed architecture maintains a 1:1 copy ratio in the NMOS current mirrors. Transistors M9,M10,M11,M12 are designed to operate in the ohmic region (near to saturation). As the same aspect ratio is selected for, respectively, M9,M10,M11,M12 and M3,M4,M5,M6, and as $V_R = V_L$, M9,M10,M11,M12 have the same gate voltage, imposing the same resistance at the source of M3,M4,M5,M6 achieving a 1:1 copy ratio.

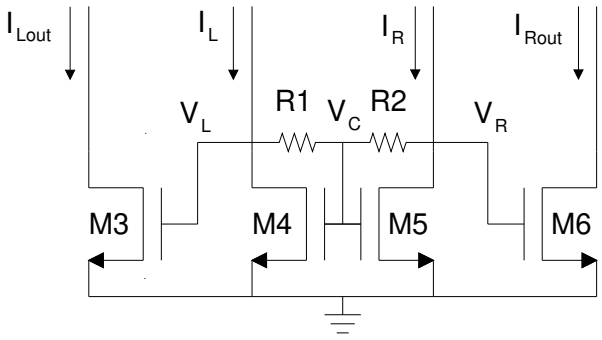
When a negative differential voltage v_d exists between the inputs of the OTA, I_R increases (noted as $\uparrow$ from now on) and I_L decreases (noted as $\downarrow$ from now on) so $V_R \uparrow$ and $V_L \downarrow$. In consequence, M11 saturates (as $I_R \uparrow$ and $V_L \downarrow$) increasing its drain source resistance while M12 decreases its drain source resistance (as $V_R \uparrow$) enhancing M5-M6 current mirror copy ratio. At the same time, the drain source resistance imposed by M10 decreases ($V_R \uparrow$) in comparison with the one imposed by M9 ($V_L \downarrow$) reducing the M3-M4 current mirror copy ratio. If the differential pair is totally unbalanced ($V_{in-} >> V_{in+}$) $I_L = 0$ A then $V_L = 0$ V turning off M11 rising V_R and giving the maximum output current I_{Rout}. As a result, the output current will be determined by the width of M6 (and M12) and it is independent of the bias current. This dramatically increases the output current of the OTA when it is totally unbalanced improving the OTA's slew-rate.

The proposed architecture has the advantage of reducing the quiescent current because it does not need any bias voltage. Additionally, as the same aspect ratio is selected for, respectively, transistors M9, M10, M11, M12 and M3, M4, M5, M6, better layout matching techniques can be implemented. In contrast to the architecture of Fig. 3.15b the unitary copy ratio is fixed by matching of equal transistors without requiring tuning of an auxiliary voltage.

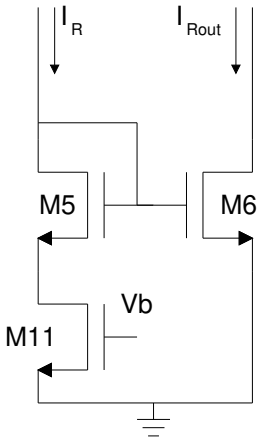
3.2.3 Comparison with previously proposed architectures

In this section, a comparison between the proposed architecture and the one presented in [91] is done. To do so, both circuits were simulated using the technology applied in [91], a 0.5 μm CMOS process. Both architectures use the same adaptive biasing block (same class-AB input stage) which was presented in [101]. In Fig. 3.16 the proposed circuit designed to be compared with [91] is shown. The comparison is done with the same OTA architecture where the non-linear current mirror used was the one depicted in Fig. 3.15b [91].

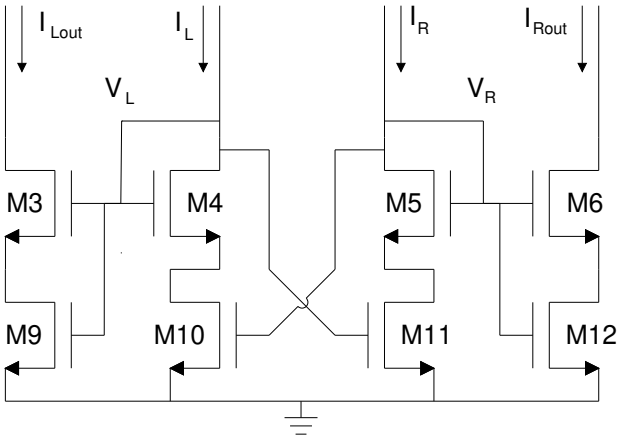
The adaptive biasing block [101] based on Flipped voltage followers (FVF's) allows the OTA to obtain a higher dc gain and less settling time. At static condition, when $Vin_+ = Vin_-$ then $V_{GS_1} = V_{GS_{1B}}$ and $V_{GS_2} = V_{GS_{1A}}$ so that M1-M1B and M2-M1A work as current mirrors setting a bias current through M1 and M2 equal to I_B. The same reasoning leads to the conclusion that the structure rejects a common mode signal. When a small differential signal v_d is applied, $Vin_+ = v_d/2$ and $Vin_- = -v_d/2$. As M1A and M1B are designed to work as voltage followers, $v_{GS_2} = v_{G_2} - v_{S_2} = v_d/2 - (-v_d/2) = v_d$ and $v_{GS_1} = v_d$. As a result, the adaptive biasing block doubles the small signal gain compared to a single differential pair.



(a) Current mirror presented in [90].



(b) Current mirror presented in [91].



(c) Proposed current mirror.

Figure 3.15: Non-linear current mirrors.

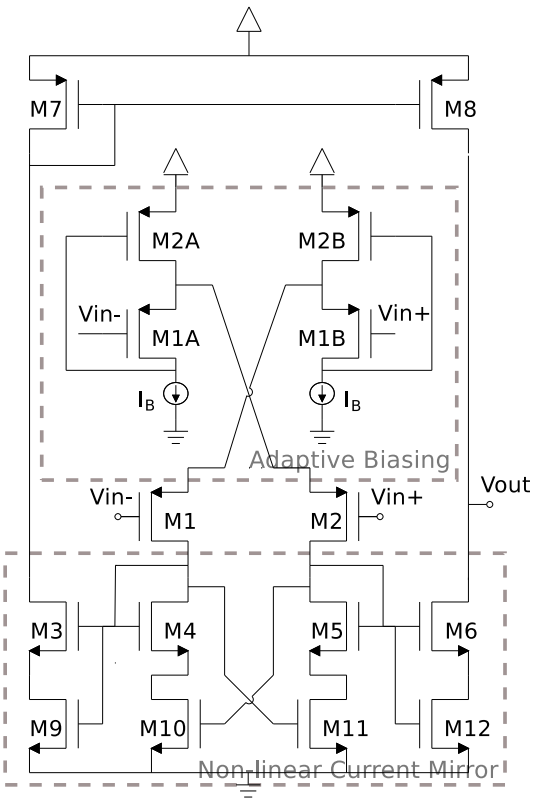


Figure 3.16: Symmetrical OTA with class-AB input and the proposed non-linear current mirror.

The main advantage of this biasing block is that the maximum current through M1 and M2 is not limited to I_B, being as large as V_{GS} and β of M1 and M2 are ($\beta = \mu C_{ox} W/L$).

The design of the circuit proposed by [91] was done following the aspect ratios, load capacitance and bias current declared by the authors. The simulations showed a very good agreement with the measurements reported in [91] validating the design (see [91]* and [91] in Table 3.4). However, some slight differences can be observed as the exact sizes and technology are not reported by the authors. The short length chosen in our design generates small variations in the quiescent currents, increasing the static power consumption. We present two different designs of the proposed architecture, the first one with high f_T while the second one prioritizes the slew-rate. Both proposed circuits were designed to fulfill similar specifications achieved by [91] while maintaining low quiescent current. All the sizes used for the circuits are presented in Table 3.3.

All the circuits were simulated with a bias current (I_B) equal to 10 μA, a load capacitance of 80 pF and a supply voltage of 2 V. Table 3.4 shows the ac characteristics for the simulated circuits. Additionally, we also include the measured results declared by [94] (which also used $C_L = 80$ pF and $I_B = 10$ μA, in a 0.5 μm

Table 3.3: Transistor's sizes for Fig. 3.16.

[W/L]	[91]*	Prop. 1	Prop. 2
M1,M2,M1A,M1B	50	50	50
M3,M6	35	20	65
M4,M5	60	20	65
M9,M12	N/C	25	160
M10,M11	60	25	160
M7,M8,M2A,M2B	240	240	240

(*) W/L for simulation of architecture of [91].

Table 3.4: Simulation Results.

	[94]	[91]*	[91]	Prop. 1	Prop. 2
DC gain [dB]	43	39.6	41	44.6	40.6
f_T [MHz]	0.725	2.2	2.3	3.59	2.45
PM [deg]	89.5	86.8	71	85.1	85.5
Static power [μW]	120	167	140	137	142
SR (+) [$V/\mu s$]	100	20	14	7	23
SR (-) [$V/\mu s$]	-78	-20	-28	-6.5	-26
ST** (+) [ns]	29	200	n/a	100	124
ST** (-) [ns]	57	180	n/a	130	105
THD*** (dB)	-56	-48	-40	-49	-47

(*) Simulated results of [91] using sizing shown in Table 3.3.
(**) Settling time (ST) (1%)
(***) THD @100 kHz, 900 mV_{pp}

All in the same technology, 0.5 μm CMOS technology.

CMOS technology). In [94] measurements for the same OTA using the non-linear current mirror presented in Section 3.2.2 and shown in Fig. 3.15a were done.

The aim of these circuits is to achieve high slew-rate while maintaining low quiescent currents so an important characteristic is the step response of the circuit. This simulation was done by configuring the circuits in unity-gain mode and applying a 500 mV, 1 MHz square wave to the input of the OTAs. The result of this simulation is presented in Fig. 3.17 for the proposed circuit (Design number 1) while Fig. 3.18 shows the result of the circuit proposed by [91]. The slew-rate and settling time of this design can be seen in Table 3.4. These could be improved by increasing the aspect ratio of transistors M3-6 and M9-12 which are the ones that determine the maximum output current as explained before, this was done on design number 2 (Prop. 2). This jeopardizes the f_T as the parasitic capacitances increase too (see Table 3.4 design number 2).

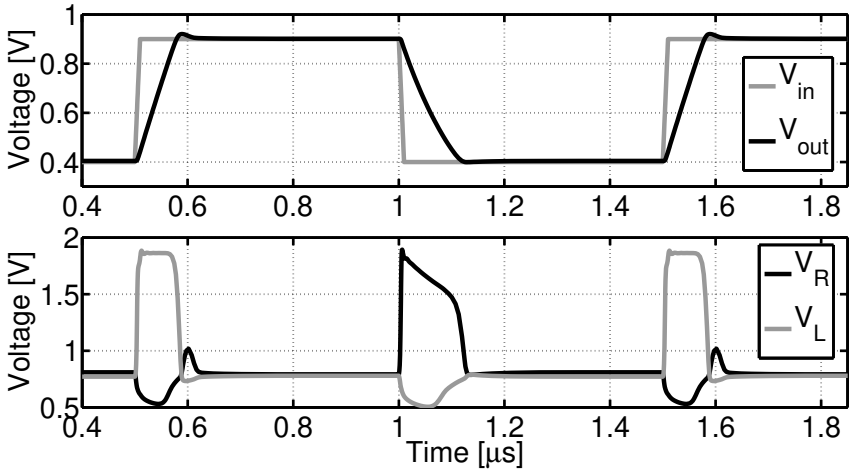


Figure 3.17: Simulation results from dimensioning shown in Table 3.3 of the proposed design number 1 (Prop. 1) OTA. V_R and V_L are the ones shown in 3.15c.

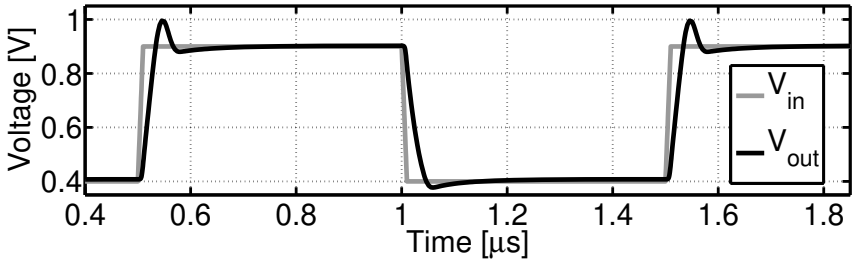


Figure 3.18: Simulation results from dimensioning shown in Table 3.3 of OTA proposed by [91].

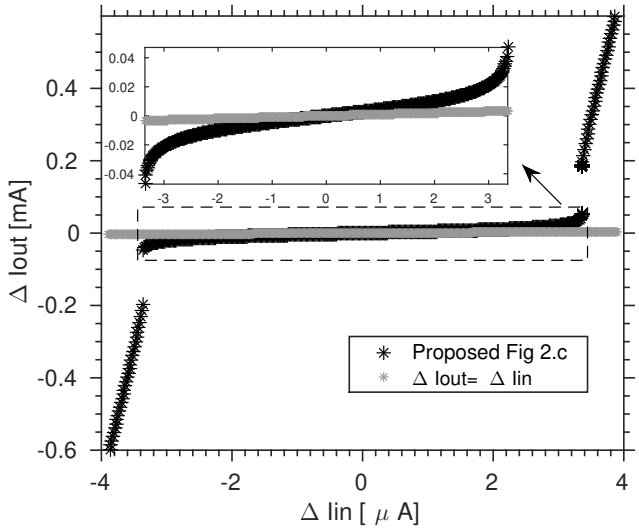
Note that if a conventional (Class-A) OTA is used, to achieve the same slew-rate as the proposed architecture (design 1), a bias current in the output branch of $i = SR.C_L = 520$ μA (instead of 10 μA) is needed, proving the advantage of using the proposed architecture.

3.2.4 Stability

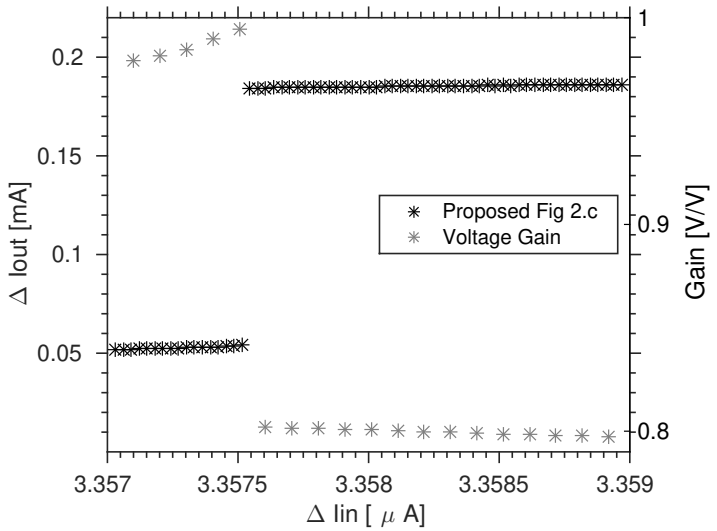
In this section, we will address the positive feedback loop that exists in our non-linear current mirror. We are going to show that this feedback loop is stable for low amplitude inputs and that the instability boosts the OTA slew-rate as is desired.

Figure 3.19a shows how the proposed mirror (Fig. 3.15c) can boost the output current. $\Delta I_{out} = I_{D_{M6}} - I_{D_{M3}}$ is plotted as a function of $\Delta I_{in} = I_{D_{M5}} - I_{D_{M4}}$ in steady state.

As can be seen in Fig. 3.15c, transistors M4,M10 and M5,M11 are biased with currents I_L and I_R respectively imposed from the differential pair. If $V_R \uparrow \Rightarrow$



(a) Output current of the mirror ($I_{D_{M6}} - I_{D_{M3}}$) as a function of the input current ($I_{D_{M5}} - I_{D_{M4}}$).



(b) Voltage gain of the open loop of Fig. 3.20 and output current of the mirror as a function of the difference in the input currents.

Figure 3.19: Steady-state output current of the proposed mirror as a function of the input current.

$R_{DS_{M10}} \downarrow \Rightarrow V_L \downarrow \Rightarrow R_{DS_{M11}} \uparrow \Rightarrow V_R \uparrow$, thus a positive feedback loop in voltage exists whose gain should be kept below one, in order to make the system stable.

Figure 3.20 shows this loop opened. If the loop gain $\frac{\partial v_o}{\partial v_i}$ is higher than one, the loop becomes unstable. This gain not only depends on the bias currents I_L and I_R but also on the dc voltages V_R and V_L. Since I_L and I_R are imposed by the differential pair, the combinations of V_L and V_R that make the loop unstable cannot be achieved in steady state.

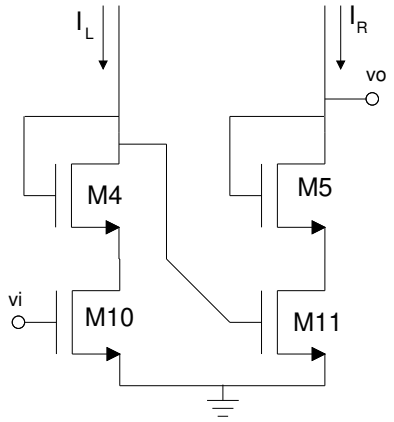


Figure 3.20: Positive feedback loop in the proposed architecture, open for open-loop gain analysis.

As can be seen in Fig. 3.19, a gap in ΔI_{out} exists since that values of output current correspond to unstable voltages (V_R ,V_L).

Figure 3.19b plots a zoom of Fig. 3.19a where the gap in ΔI_{out} occurs. Additionally, it is plotted the loop gain as a function of ΔI_{in} which shows that the loop gain reaches the unitary gain in the border of the gap.

Therefore, the proposed non-linear current mirror increases the output current based on two effects: the non-linearity (range around -3.3 μA to 3.3 μA) and the discontinuity generated by the positive feedback loop.

This unstable zone may lead to undesired overshooting in transient response, thus care must be taken while designing.

3.2.5 Application to switched-capacitor dc-dc feedback loop

In this section, we present the application of the non-linear current mirror in an OTA to be used as part of the feedback control loop of a switched-capacitor dc-dc converter [15]. This converter is different from the one presented in Section 3.1, this is intended for ultra-low power applications with $V_{in} = 1.2$V, $Vo = 1.1$ V-0.2 V, $P_{LOAD_{max}} = Vo.I_L = 2.2$ mW. Therefore, the quiescent consumption of the OTA is critical for the converter's efficiency at low output currents. First, we will see how the entire system works which will impose the requirements for the OTA, Fig. 3.21 shows a block diagram of the system.

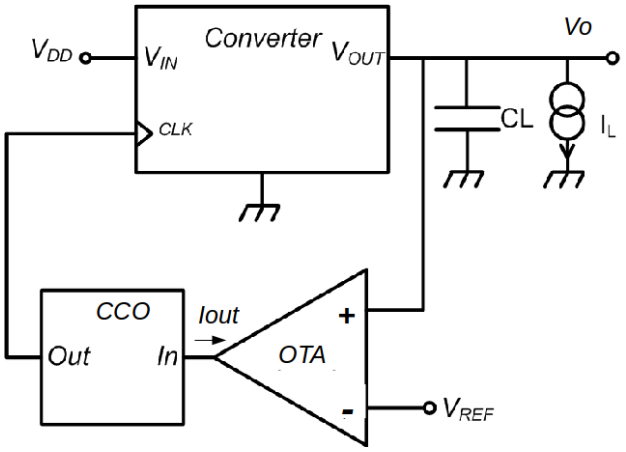


Figure 3.21: Block diagram of the switched-capacitor dc-dc converter with the feedback control loop. The CCO is a Current Controlled Oscillator and the OTA is the proposed block.

In these converters, the switching frequency depends on the current delivered to the load, a higher current implies a higher switching frequency in order to maintain the output voltage of the converter (Vo see Fig. 3.21) constant. To do this, a feedback loop is required to detect changes in Vo and adjust the switching frequency accordingly. The feedback loop consists of an OTA and a current control oscillator (CCO) (as the one that we presented in [10]). The OTA controls the input current of the CCO, which controls the switching frequency of the converter, depending on the difference between Vo and the desired output voltage (V_{REF} see Fig. 3.21). The CCO is based on a current-starved ring oscillator, the output current of the OTA is copied by a PMOS current mirror and used to control the current through the inverters of the ring oscillator. Due to this, the output frequency of the oscillator directly depends on the output current of the OTA. Since the output current of the OTA is copied through a PMOS current mirror, when the OTA wants to deliver a negative current (when $Vo = V_{in+}$ is higher than $V_{REF} = V_{in-}$, see Fig. 3.21), the input voltage of the mirror rises to VDD turning off the CCO.

One of the most challenging issues in this kind of converters is to achieve high efficiencies when the current delivered to the load is very small, for example in the order of the μA. One of the reasons why this is not trivial is that the feedback loop needs to have a consumption negligible in comparison with the current delivered to the load, if not the total efficiency of the converter will be diminished in this situation. On the other hand, when the delivered power is high, the OTA needs to deliver enough current to increase the CCO frequency and achieve the required switching frequency of the converter. Thus, the CCO has an output frequency range of three orders of magnitude while its input current changes between some pA and tens of μA [10].

The reasons stated before are why the required OTA needs to be able to deliver μA at its output when its inputs are unbalanced but cannot consume more than some tens of nA of quiescent current when the inputs are balanced. With a classic

symmetric OTA this cannot be done since the maximum output current is limited by the I_{bias} of the OTA. In order to fulfill the two specifications, high maximum output current, and low quiescent consumption, the non-linear current mirrors proposed in this work were used in a symmetric OTA.

Moreover, in this particular application, the OTA only needs to have a high output current when Vo is below the V_{REF} (Fig. 3.21) so the non-linear current mirror was used in one of the two NMOS current mirrors. It can be noticed that by doing this the positive feedback loop analyzed in the previous section is not present in this architecture. Figure 3.22 shows the architecture of the implemented non-symmetrical OTA.

It can be seen that when the output voltage of the converter ($Vo = V_{in+}$) drops below the reference voltage ($V_{REF} = V_{in-}$), the non-linear current mirror is used, increasing the output current. However, if the output voltage Vo exceeds V_{REF}, there is no need of boosting the output current of the OTA. If Vo is higher than V_{REF}, the OTA will deliver Ibias (negative) but that current cannot pass through the input of the CCO (as there is a PMOS diode at the input). Thus, the input voltage of the CCO increases until VDD and the oscillator is turned off. This is the desired operation since the converter is not capable of reducing the output voltage, therefore it stops working until the load discharges Vo below V_{REF}.

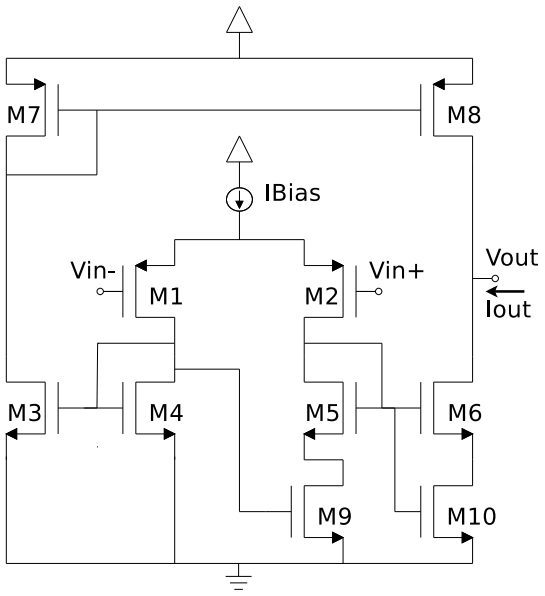


Figure 3.22: Proposed non-symmetrical high slew-rate OTA, fabricated in 130 nm. Used in the feedback loop of a switched-capacitor dc-dc converter.

The circuit was fabricated in a 130 nm technology and the sizes of each transistor are shown in Table 3.5. Figure 3.23 shows the layout and Fig. 3.24 a photo of the fabricated circuit.

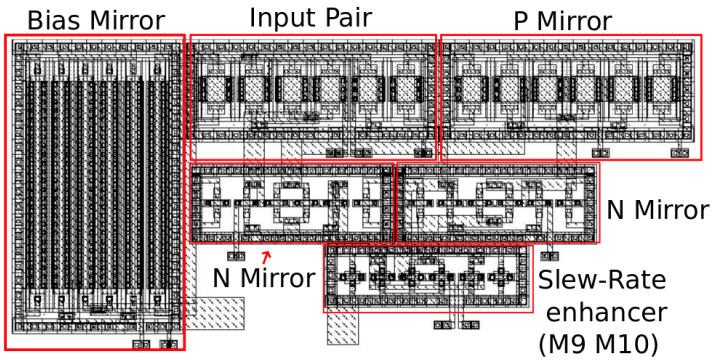


Figure 3.23: Layout of the Fabricated OTA, $420\ \mu\text{m}^2$.

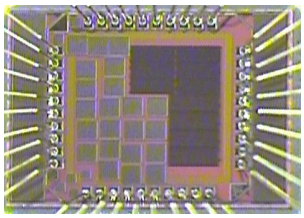


Figure 3.24: Fabricated chip photo. Auto fill blocks and dual-mim caps cover the OTA.

3.2.6 Measurement results

In this section measurements of the non-symmetrical OTA are presented. The aim of the measurements is to demonstrate that the slew-rate enhancer is working. In order to show this, two different measurements are presented. Figure 3.25 shows the OTA's output current for various differential inputs voltages ($v_d = Vo - V_{REF}$). Figure 3.26 displays the OTA's output voltage for a square wave input when the OTA is loaded with a 50 pF capacitance and biased with 50 nA.

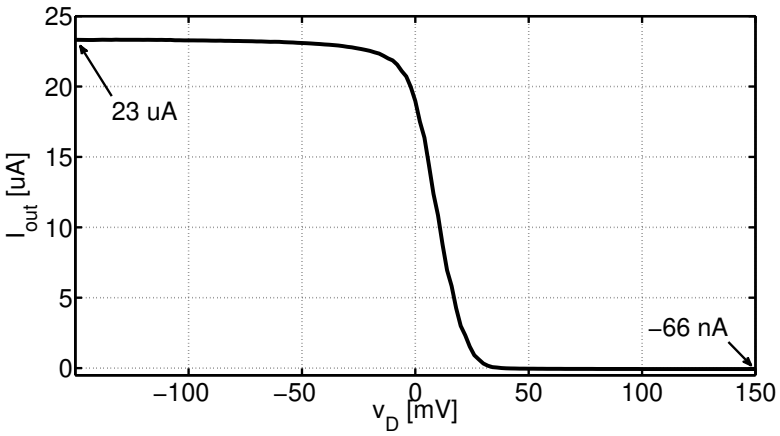


Figure 3.25: Measure of the OTA output current for different input voltages v_d. The common mode voltage is 600 mV.

Table 3.5: Transistor's sizes of the non-symmetrical fabricated OTA.

	[μm]
M1,M2,M7,M8	$W = 1.6$ $L = 1.2$
M3,M4,M5,M6	$W = 0.6$ $L = 0.24$
M9,M10	$W = 0.52$ $L = 0.12$

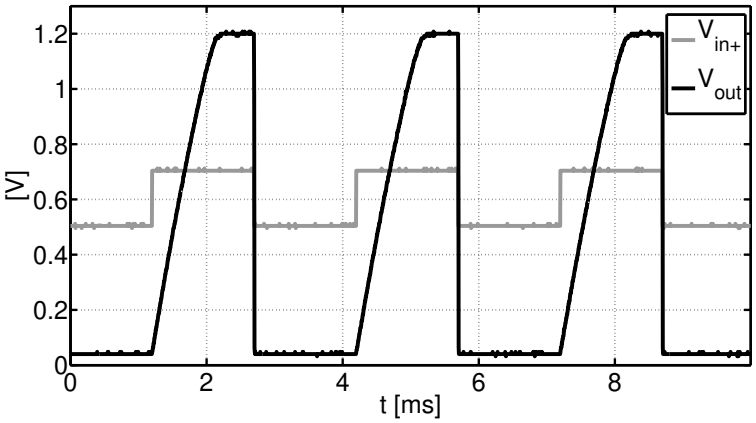


Figure 3.26: OTA output voltage measured with a square input. $V_{in-} = 600\ mV$ and $C_L = 50\ pF$.

The non-symmetrical architecture helps to understand the improvement in slew-rate achieved by the proposed non-linear current mirror. When $V_{in+} > V_{in-}$, the OTA works like a classic one since the non-linear current mirror is not activated. However, when $V_{in+} < V_{in-}$ the slew-rate enhancer block dramatically increases the output current. This allows us to easily compare the proposed circuit and a classic OTA.

Figure 3.25 shows that for a positive v_d, the output current is similar to the bias current 66 nA ($I_{bias} = 50$ nA, slight mirror copy ratio errors influence the actual result), as in a typical OTA. However, for negatives values of v_d the non-linear current mirror increases the output current achieving 23 μA, approximately 350 times higher than the typical one (66 nA).

In Fig. 3.26 the difference between the rise and fall time evidences the improvement obtained by the proposed slew-rate enhancer. The measured slew-rates are 1.5 mV/μs and 535 mV/μs at rising and falling time respectively.

3.2.7 Conclusion of Section 3.2

In this section, a new architecture for a Super Class-AB OTA was proposed based on a novel non-linear current mirror architecture. The proposed circuit has a comparable performance with the state-of-the-art Super Class-AB OTAs while re-

ducing the quiescent current consumption and improving dc gain and bandwidth. The compactness of the proposed architecture allows to use less area and is better suited for the implementation of layout matching techniques than others proposed circuits. Additionally, the copy ratio of the proposed architecture is fixed by matching of equal transistors in contrast to other previously presented architectures. The novel non-linear current mirror was also used to design a non-symmetrical OTA which is part of the feedback loop of a switched-capacitor dc-dc converter. This circuit was fabricated in 130 nm validating through measurements the proposed architecture.

3.3 Active rectifier

The design of rectifiers with high Power Conversion Efficiency (PCE) and Voltage Conversion Ratio (VCR) has been addressed in many papers [26, 27, 102–105]. Passive diodes dramatically degrade PCE and VCR in applications where the input voltage amplitude is comparable with the diode forward voltage. To solve this, in active rectifiers, the passive diodes are substituted with MOS switches and comparators, avoiding the voltage drop and increasing both PCE and VCR. A typical architecture of an active rectifier, that is used in this section, is presented in Fig. 3.27 [102–105].

The delay of the comparator causes that the switch does not turn exactly at the proper time. If a signal of 13.56 MHz is being rectified, some nanoseconds of delay in the comparator are enough to deteriorate the rectifier performance [26]. Many WPT systems are designed at this frequency (13.56 MHz) which is within the free industrial scientific and medical band. In addition, this frequency allows the implementation of high-quality factors coils with small sizes, which are required in AIMD applications. To design high-efficiency active rectifiers that work at 13.56 MHz, different techniques to overcome the comparator delay have been proposed [26, 27, 102–105]. In [26, 27], off-chip signals are needed to tune the delay compensation circuit while in [102–105] a feedback loop was implemented to automatically optimize the delay compensation.

The comparator power consumption is not directly scaled with the rectifier output power, thus it affects the efficiency especially at light loads. In order to achieve low rectifier output powers with high efficiency, low power consumption comparators are required. For instance, in low power applications, e.g., 1 mW output power, the comparator proposed in [102] that consumes 770 μW cannot be used. Such a low output power is required in biomedical systems like [106], where an EEG fabricated in a 130nm process that consumes 1.07 mW from a 1.2 V source was presented.

In this section, we present the design and simulation results, in a 130nm CMOS technology, of an active rectifier that is able to deliver 1.37 mW ($R_L = 1\ k\Omega$, $V_{rec} = 1.17\ V$) with high efficiency (PCE=95.7%). This was possible due to the proposed low power comparator, that consumes only 3.7 μW. Additionally, the proposed comparator implements a feedback loop to self-tune the delay compensation as in [102], thus none off-chip control signal is needed.

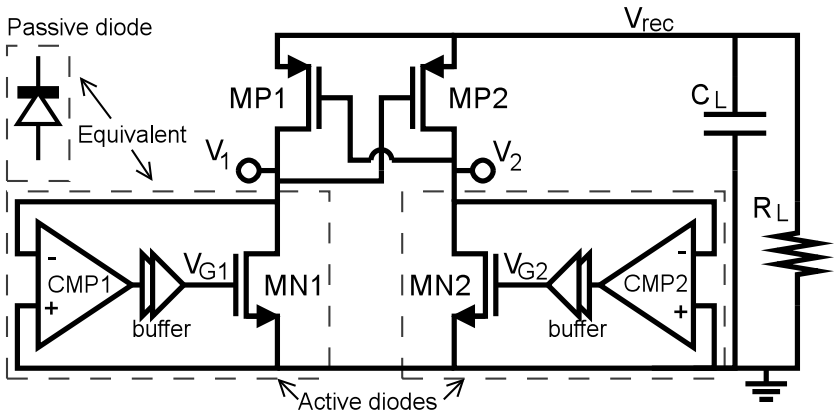


Figure 3.27: Active rectifier used. CMP1 and CMP2 are instances of the proposed comparator which schematic is presented in Fig. 3.29.

Section 3.3 is organized as follows. Section 3.3.1 presents a summary of the rectifier design. The proposed comparator is analyzed in Section 3.3.2. The simulation results are presented in Section 3.3.3 followed by concluding remarks in Section 3.3.4.

3.3.1 Active rectifier: architecture and design

The rectifier of Fig. 3.27 was designed in a 130nm technology. The transistors widths were optimized to maximize PCE for an input peak voltage $V_{in_{peak}} = (V_1 - V_2)_{peak} = 1.2$ V with a frequency of 13.56 MHz, a load resistance $R_L = 1$ kΩ and $C_L = 2$ nF. The frequency, voltage and output power were selected for low power AIMDs [106]. If MN1 and MN2 are too wide the gate drive loss dominates, while if they are too narrow the conduction loss dominates, thus an optimum width exists. The design led to a W/L=304μm/120nm for MN1 and MN2. The PMOS transistors are self-driven thus they were selected much wider, W/L=5000μm/120nm (MP1 and MP2). A further explanation regarding the active rectifier architecture and its design is presented in Appendix B.

The PCE can be expressed as PCE= $P_{out}/(P_{out} + P_{cond} + P_{gd} + P_{comp})$, where P_{out} is the power delivered to R_L, P_{cond} is the conduction loss dissipated in MN1, MN2, MP1 and MP2, P_{gd} is the gate drive loss consumed by the driver (inverter chain) that drives the gates of MN1 and MN2, and finally, P_{comp} is the power consumed by both comparators. All these powers and the VCR=$V_{rec}/V_{in_{peak}}$ are presented in the simulation results Section 3.3.3.

This design does not consider the comparator and driver delay which generates back current. Therefore, we need a comparator able to drive at 13.56 MHz with a compensated delay and a low power consumption $P_{comp} << P_{out} \simeq (1.2V)^2/1000\Omega = 1.44$ mW. This comparator was the most challenging block designed and is presented in the next Section 3.3.2.

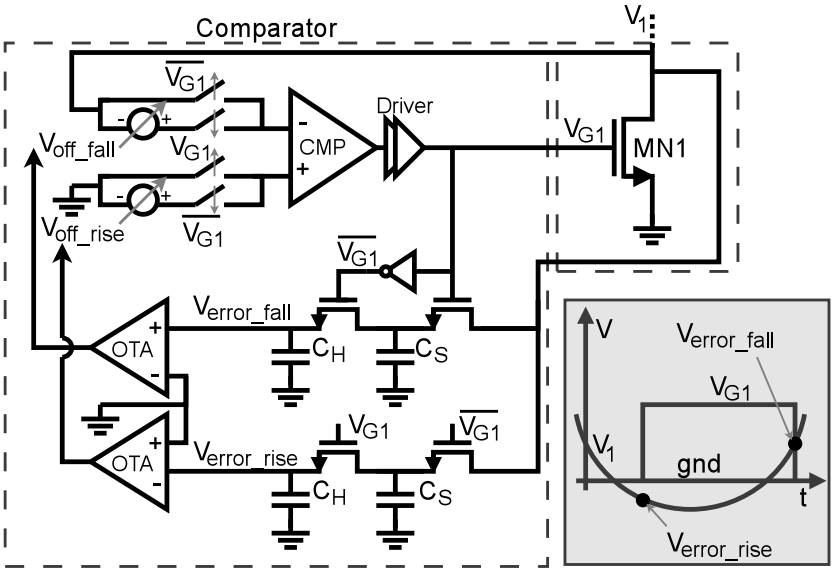


Figure 3.28: Block diagram of the delay compensated comparator.

3.3.2 Proposed comparator

In this section, we will first present a general description to understand how the delay of the comparator is compensated and then the proposed implementation.

3.3.2.1 Structure Description

A simplified description of the comparator is presented in Fig. 3.28 and explained below. The switch MN1 will be turned ON when V_1 is lower than gnd. Signals V_1 and V_{G1} are represented in Fig. 3.28 to simplify the comparator understanding. The delay compensation consists in adding the proper offset to the comparator in order to make it start turning earlier and thus compensate its delay [26]. For instance, when V_{G1} is down and the comparator is awaiting to generate a rising edge in this signal, an offset $V_{off\_rise} > 0$ is added in the positive input of the comparator as shown in Fig. 3.28. This makes that the comparator starts turning when $V_1 = V_{off\_rise}$, before V_1 gets to gnd, and thus its delay is compensated. A similar approach is applied for the falling edge of V_{G1} with the V_{off_fall} voltage. This idea has been used in [26,27,102–104]. In [26,27] off-chip signals are needed to tune the values of V_{off_rise} and V_{off_fall}, while in [102–104] the negative feedback loop shown in Fig. 3.28 and explained below was used.

The main idea of the feedback is to sample the voltage of V_1 in both edges of V_{G1}. These sampled voltages will be referred to as V_{error_fall} and V_{error_rise} for the falling and rising edges, respectively. The same signal that controls the gate of MN1, V_{G1}, is used to sample the signal V_1 in capacitor C_S thus obtaining precisely the value of V_1 in the falling and rising edges. That sampled value is then held in capacitor C_H. Since V_{G1} is supposed to switch when $V_1 = gnd$, these values (V_{error_fall} and V_{error_rise}) represent the delay that V_{G1} has in each edge. These

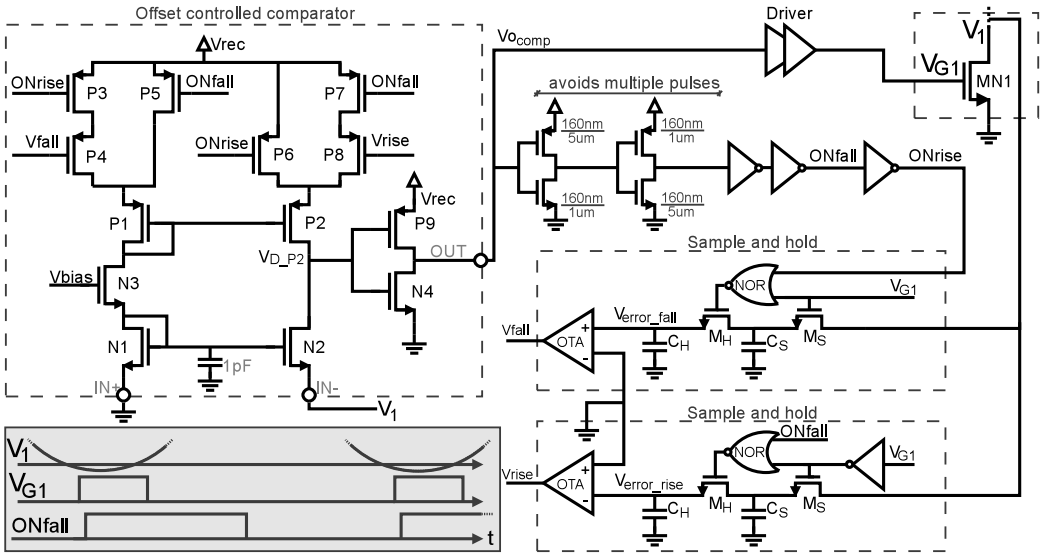


Figure 3.29: Schematic of the proposed delay compensated comparator.

errors are then amplified and used to control the offsets added to the comparator.

3.3.2.2 Proposed Circuit

In this subsection, the proposed delay compensated comparator showed in Fig. 3.29 is described for the case of CMP1 in Fig. 3.27. An offset controlled comparator, composed of transistors N1-N4 and P1-P9, compares V_1 against gnd. In this common-gate (N1 and N2) comparator [26], we propose to add source resistances to P1 and P2 in order to generate offset by changing the PMOS current mirror copy ratio. Transistors P3, P5, P6, and P7 work as switches controlled by the digital signals $ONrise$ and $ONfall$ ($ONrise = \overline{ONfall}$). P4 and P8 work as resistances that are added to the source of P1 or P2 respectively, depending on $ONrise$ and $ONfall$. The voltages $Vrise$ and $Vfall$ are the outputs of the amplifiers and control how much offset is added to the comparator in each edge. The voltage V_{bias} in the gate of N3 determines the bias current of the comparator. If there is no source resistance in P1 and P2 and $IN_- = V_1 = gnd = IN_+$, the same bias current of the left branch is copied to the right one. A difference between IN_+ and IN_- modifies the current through N2 and thus switches the comparator.

For instance, when the output voltage of the offset controlled comparator (Vo_{comp}) is low, the comparator is awaiting to generate a rising edge, thus $ONfall = gnd$ and $ONrise = V_{rec}$ as shown in Fig. 3.29. In this situation, the source resistance is added to P2, reducing the current through it. Therefore V_{D_P2} will go down even before $V_1 < gnd$, thus bringing forward the Vo_{comp} rising edge. If $Vrise = gnd$, the rising edge is almost not altered while the maximum delay compensation is applied to the rising edge if $Vrise = V_{rec}$. An analogous analysis can be done with $Vfall$.

In previous works [26, 27, 102–104] the offset of the comparator was generated

with additional current branches. These extra branches increase power consumption. The solution proposed in this section achieves lower power consumption as will be shown in Section 3.3.3.

If too much offset is added too fast after the Vo_{comp} edge, multiple pulses may occur in Vo_{comp} (and V_{G1}) which is not desired. This multiple pulse problem was discussed in previous works [102, 103, 105]. In the proposed comparator this problem was overcome with minimum power consumption by adding a delay between Vo_{comp} and the signals $ONfall$ and $ONrise$. Since in normal operation V_{G1} has a low duty cycle, the delay that we generate after the rising edge is short while the delay after the falling edge is much larger. Therefore, after the falling edge in V_{G1}, the logic maintains the same offset that caused this falling edge during a safety time, preventing the generation of another pulse before the next period. This different delay depending on the V_{G1} edge is achieved increasing the PMOS length of the first inverter and the NMOS length of the second one as can be seen in Fig. 3.29.

In the same conference where we presented this way to overcome the multiple pulse problem [8], a similar analysis was presented in [107]. Although the architecture used in [107] is different, they showed how the multiple pulse problem can be solved adding delay in the feedback as we proposed in [8].

The control signals of the sample and hold (S&H) are generated using a NOR and the signals V_{G1}, $ONrise$ and $ONfall$. This simple implementation avoids M_S and M_H to be ON at the same time, as happens if the S&H is implemented as shown in the simplified block diagram of Fig. 3.28 due to the inverter delay.

The amplifier (OTA of Fig. 3.29) architecture and design is presented in Fig. 3.30. It was designed to assure the loop stability as discussed in [102], with minimum power consumption. The S&H was designed to minimize the charge injection effect, $C_S = C_H = 40$ fF and $W/L = 320$nm/120nm for both M_S and M_H. A dummy switch, not presented in Fig. 3.29, with $W/L = 160$nm/120nm was added in V_{error_rise} and V_{error_fall}. In the offset controlled comparator, N3 has $W/L = 160$nm/2.5μm while the rest of the transistors are minimum size ($W/L = 160$nm/120nm) to minimize parasitic capacitance. Although these small sizes generate offset, it is not a problem since the feedback loop will control $Vfall$ and $Vrise$ to adjust it anyway. The gate voltage of N3, $Vbias$, imposes a bias current $I = 1.25$ μA.

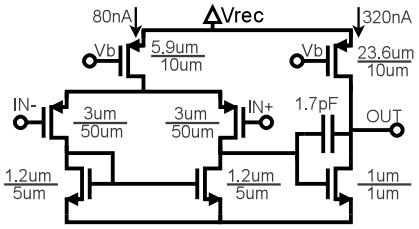


Figure 3.30: Designed OTA of Fig. 3.29.

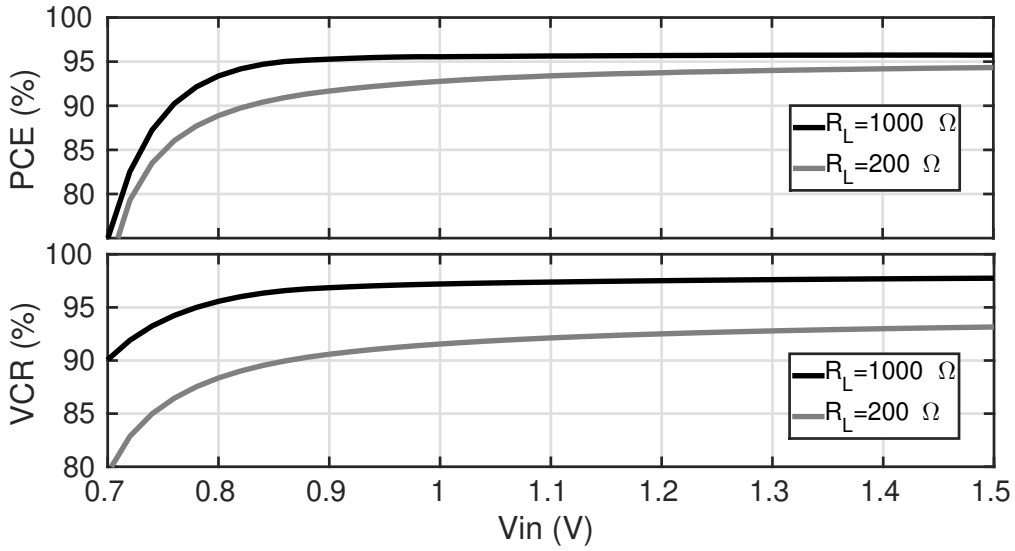


Figure 3.31: Simulated PCE and VCR for the proposed rectifier.

3.3.3 Simulation results

The rectifier presented in Section 3.3.1 was simulated, using the proposed comparator, in a 130nm technology. The simulated PCE and VCR are presented in Fig. 3.31 as a function of the rectifier input amplitude ($V_{in_{peak}}$). Although the rectifier transistors width (MN1, MN2, MP1 and MP2) were optimized for $V_{in_{peak}} = 1.2V$ and $R_L = 1$ kΩ, an efficiency higher than PCE> 93% is obtained for the range $0.8V < V_{in_{peak}} < 1.5V$. The power distribution for the case of $V_{in_{peak}} = 1.2V$ and $R_L = 1$ kΩ is presented in Fig. 3.32.

A Monte Carlo simulation was done for the case of $V_{in_{peak}} = 1.2V$ and $R_L =$ 1 kΩ. The histogram of the PCE for 200 runs is presented in Fig. 3.33. The VCR obtained in this Monte Carlo has a mean value $\text{VCR}_{mean} = 97.3\%$ and a standard deviation $\sigma = 0.30\%$. The pulses in V_{G1} for 20 of those runs are presented in Fig. 3.34a. As can be seen, the circuit is robust maintaining high PCE and VCR, this is because the feedback loop automatically adjusts $Vfall$ and $Vrise$ in each run to compensate the delay.

In order to show how the feedback loop is controlling the delay, the same rectifier was simulated without the feedback loop. The comparator used is the same common-gate showed in Fig. 3.29 without the source resistances (and without the rest of the feedback loop). This rectifier has a mean efficiency PCE= 91% and a standard deviation $\sigma = 5.3\%$, thus its performance is considerably lower than the proposed comparator. The pulses in V_{G1} for 20 of those runs are presented in Fig. 3.34b, which highlights the need of the feedback loop.

These simulation results are compared with the state-of-the-art in Table 3.6. Although we are presenting simulation results, as [104, 105], the proposed circuit presents a very promising PCE and VCR. Regarding the power consumption of the comparators (P_{comp}), this work presents the lowest one, which allows us to achieve

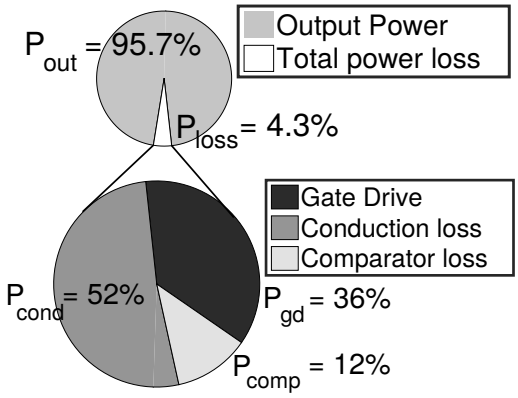


Figure 3.32: Power distribution at $V_{in_{peak}} = 1.2V$ and $R_L = 1\text{k}\Omega$.

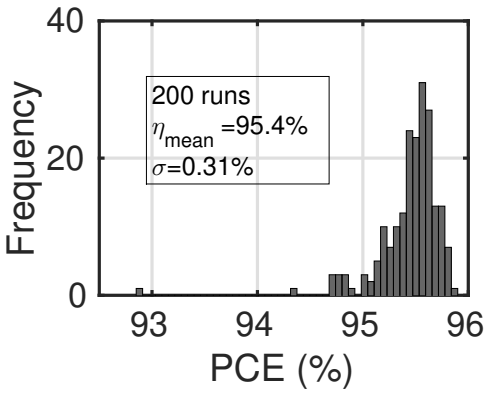
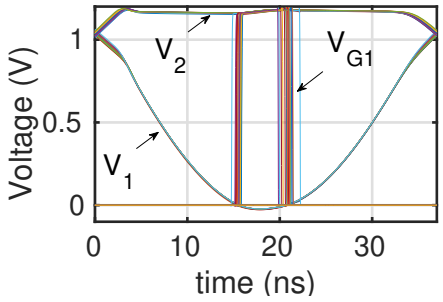
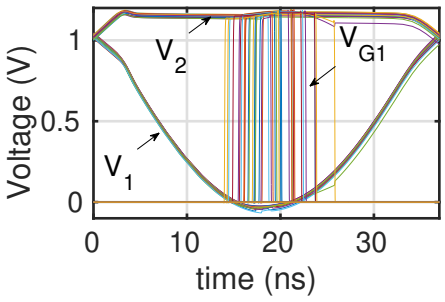


Figure 3.33: Monte Carlo simulation at $V_{in_{peak}} = 1.2V$ and $R_L = 1\text{k}\Omega$.



(a) For the proposed circuit.



(b) Without feedback loop.

Figure 3.34: Pulses in V_{G1}.

high efficiency with such a low output power. The Off-chip signals row in Table 3.6 indicates whether off-chip control signals are needed to tune the comparator delay.

3.3.4 Conclusion of Section 3.3

The proposed delay compensated comparator achieves a low power consumption of 3.7μW thanks to: 1) the proposed low-power common-gate comparator with source resistance in the PMOS current mirror, 2) the simple control logic imple-

Table 3.6: Comparison to the state-of-the-art active rectifiers.

	TCAS-I 2011 [26]	TbioCAS-2013 [27]	JSSC-2016 [102]	JSSC-2016 [103]	WPTC-2016 [104]	ISCAS-2017 [105]	This Work
Technology	0.5 μm	0.5 μm	0.35 μm	65 nm	180 nm	180 nm	130 nm
Frequency	13.56 MHz	13.56 MHz	13.56 MHz	13.56 MHz	13.56 MHz	13.56 MHz	13.56 MHz
Input voltage	3.8 V	1.46 V	3.6 V	2.5 V	4.5 V	2 V	1.2 V
P_{OUT}	19.4 mW $R_L = 500\Omega$	5.76 mW $R_L = 1\text{k}\Omega$	22 mW $R_L = 500\Omega$	57 mW $R_L = 100\Omega$	35 mW $R_L = 500\Omega$	17 mW $R_L = 200\Omega$	1.37 mW $R_L = 1\text{k}\Omega$
C_L	10μF	1μF	2nF	51.8nF	100nF	N/A	2nF
VCR	82%	82.2%	92.4%	95.2%	93%	91.5%	97.5%
PCE	80.2%	79%	91.4%	94.6%	92.2%	95.3%	95.7%
Off-chip signals	YES	YES	NO	NO	NO	NO	NO
P_{comp} Simulated	135 μW	525 μW	770 μW	N/A	N/A	44 – 120 μW	7.39 μW

mented that overcomes the multiple pulse problem, and 3) the transistor sizing which reduces power consumption. The comparator delay is self-compensated by a feedback loop and none off-chip signal is needed. This comparator was used to implement a high efficiency, 95.7%, active rectifier that is suitable for wireless power transfer systems at 13.56 MHz for low power ($Pout \simeq 1$ mW) applications.

3.4 Multiple-gain active rectifier

Instead of using an active rectifier (Section 3.3) and a dc-dc converter (Section 3.1), both blocks can be implemented together in a multiple-gain rectifier [30, 108–110].

This section presents the implementation of a novel multiple-gain x1-x2-x3 rectifier. The architecture used is the modular series-parallel presented Section 3.1 which allows multiple conversion levels. The analysis of Section 3.3 was used for the active switches implementation.

This section is organized as follows. First, the proposed architecture is introduced in Section 3.4.1. Further details regarding its design can be found in Appendix C. Simulation results of a proof-of-concept circuit are presented in Section 3.4.2. In Section 3.4.3, the converter is used to adjust Z_{MN} and maximize η_{Link}, this study is further addressed in Chapter 4. Finally, the main conclusions of Section 3.4 are drawn in Section 3.4.4.

3.4.1 Proposed ac-dc converter

The proposed series-parallel architecture is shown in Fig. 3.35. The cells x2 and x3 have the same architecture as Cellx1. We assume that the capacitors used are large enough to maintain its voltage V_C almost constant.

The rectifier works in two main non-overlapping phases: in $T1$ parallel connected capacitors are charged from the input and in phase $T2$ the charge is delivered to the load from series connected capacitors. Since in phase T1 the energy is taken from an AC source, in order to adequately charge capacitor C from this source it is necessary to distinguish the following situations. First, it must be differentiated which input terminal has the highest voltage in order to connect the input always with the same polarity. Second, it must be detected when the input voltage is higher than the capacitor voltage V_C, so that it is charged instead of discharged. These two detections are implemented as described next. The phase $T1$ is divided in $T1_A$ that is active when $V_A > V_C$ and $T1_B$ that is active when $V_B > V_C$, during this time the $T2$ switches remain OFF. In order to detect whether we must activate phase $T1_A$ or $T1_B$, the switches $T1_{A_{down}}$ and $T1_{B_{down}}$ of the first cell (Cellx1, Fig. 3.35) are in charge of referencing the input voltage to ground. Thus, $T1_{A_{down}}$ is ON when $V_A > V_B$ while $T1_{B_{down}}$ is ON when $V_A < V_B$. Phase $T2$ is activated during the lapse when the input voltage (absolute value of $(V_A - V_B)$) is lower than V_C, and therefore V_C cannot be charged during this period (see time diagram in Fig. 3.35). On phase $T2$ the cells are interconnected in series and connected to the load. Which switches are turned ON depends on the

conversion ratio selected. During this phase $T1$ switches are OFF except for the ones that reference the node A and B to ground ($T1_{A_{down}}$ and $T1_{B_{down}}$ of Cellx1).

If the conversion ration is x3, switches $T2_{out}$x2 and $T2_{out}$x1 remain OFF while the other switches operate as described before. For a x2 ratio, switches $T2_{out}$x3, $T2_{out}$x1, $T2$x3 and all the switches in Cellx3 are not used (OFF state). When a unitary ratio is needed, only the switches of Cellx1 are active. Additionally $T2_{out}$x1 can be kept ON during both phases $T1$ and $T2$, thus transmitting power to the output in both phases.

Three comparators are needed, one to compare V_A and V_B and two more to detect when V_A or V_B is higher than V_C. All the cells will have the same transistor sizes and capacitor value. Therefore, on steady-state, the voltage on each active cell's capacitor V_C will be theoretically the same. All the cells will receive the same amount of charge during $T1$ and will lose also the same charge during $T2$ (as they are connected in series). Consequently, when V_A or V_B is higher than V_C on Cellx1, where the comparators are, we can assume that it is time to refill not only Cellx1 but also the others cells.

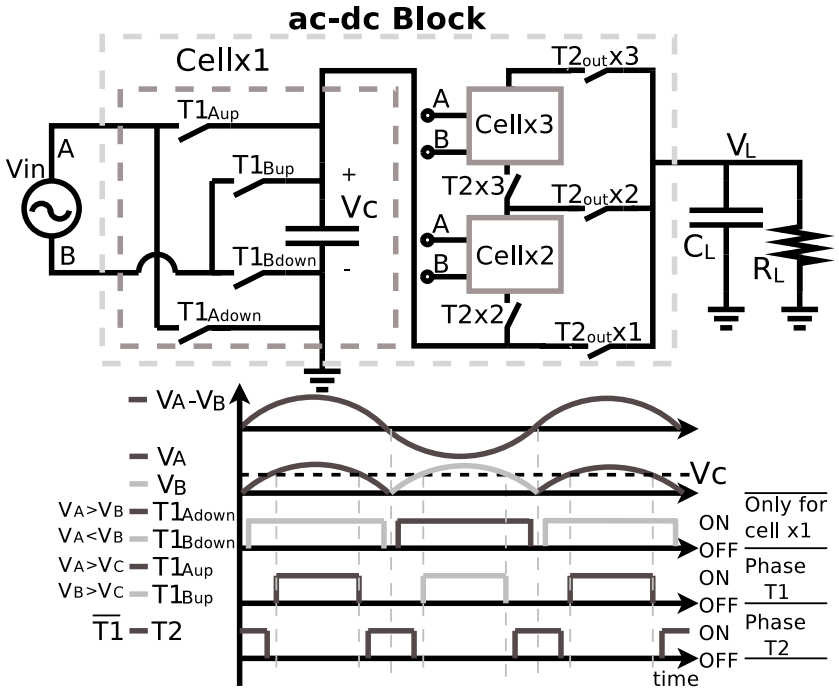


Figure 3.35: Proposed series-parallel reconfigurable multiple-gain rectifier.

The MOS switches implementation is not trivial in any step-up converter [1], as discussed in Section 3.1. Here, we decided to use the output dc voltage to drive the switches, approach A in Fig. 3.4. Since in a step-up the output voltage (V_L) is always the highest voltage (or near the highest considering the voltage drop in the switches), we can turn OFF any PMOS transistor and drive the NMOS with lower ON resistance, thus allowing more output power for a given width. All the NMOS bulks are connected to ground while the PMOS bulks are connected to V_L.

At startup, if V_L is totally discharged, the switches do not operate properly, and the converter is not able to start. Several approaches can be used to ensure startup, depending on the initial conversion ratio, load power consumption, or if a precharged capacitor or battery is available. For example, in most AIMD's with WPT capability, a battery to start the converter would be available. However, a robust system should be able to startup even if there is no energy at all in the receiver. For this reason, we add four diodes in parallel with $T1$ switches only in Cellx1 working as a full wave rectifier. It provides a dc voltage in the V_C of the first cell to enable self-startup. The converter will start in x1, and we assume that there is enough power to rise V_L. This can be achieved by reducing the distance D or temporary increasing the transmitter power until the receiver has started up.

The architecture was designed to deliver around 1.8 to 110 mW at 3V output voltage ($R_L = 80 - 5k\Omega$) and 1 MHz input frequency. It was simulated on a 130nm CMOS technology using 3.3V high-voltage transistors. Further information regarding the multiple-gain rectifier is presented in Appendix C.

3.4.2 Simulation results

The proposed converter was simulated using a 130nm CMOS technology and 200nF off-chip capacitors. Those capacitors are enough to have very low voltage variations reducing losses and ripple. As the comparators and all the logic is out of the scope of this section, it was implemented in verilog. Although the logic power consumption was not included in the efficiency, the gate-drive power was considered as it represents a non-negligible amount of power.

Figure 3.36 presents the simulated efficiency of the proposed converter and the efficiency predicted by the model used to design it, which is discussed in Appendix C.

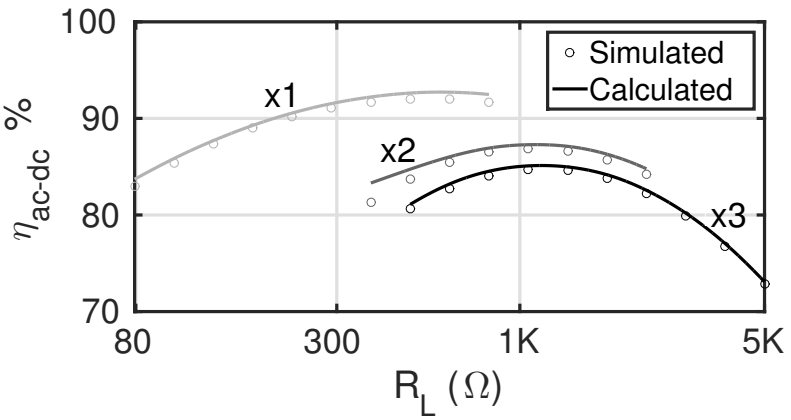


Figure 3.36: Proposed ac-dc converter efficiency. In this simulation, V_{in} was adjusted to always obtain constant output voltage ($V_{out} = 3$ V) which is the typical situation when preregulation is used (preregulation is analyzed in Chapter 5 and Appendix D). The carrier frequency was 1 MHz.

A comparison between the proposed ac-dc converter and works in the state-

of-the-art is presented in Table 3.7. It should be noted, that in this work we are presenting simulation results and that the power consumption of the logic and comparators are not considered in the efficiency. If, for example, the high-speed comparators presented in [26] that consumes 135μW had been used for the three comparators, the x1-x2-x3 rectifier maximum efficiencies would be 92%, 86.9% and 84.7% respectively. If the comparators proposed in Section 3.3 are used, the efficiency is almost not affected. Additionally, this is a worst case estimation as the comparators of Section 3.3 were designed and measured working at 13.56MHz, while the ac-dc converter designed in this section is working at 1 MHz.

Table 3.7: Comparison with state-of-the-art.

	[27]	[109]	[30]	[108]	This work
f (MHz)	13.56	13.56	40.68	1	1
Gain G	x2	x1-x2	x1-x2	x2-x4	x1-x2-x3
η_{ac-dc} %	79	77-70	$\simeq$ 90-80	92.7-88.5	95-92.2-89.7
Power mW	$\simeq 6$	20	$\simeq$ 1-13	1-20	$1.8 - 110$

The actual gain value in each conversion ratio depends on R_L. If R_L decreases more power has to be taken from V_{in}, thus V_C is reduced, phase $T1$ takes more time and the gain G decreases.

3.4.3 Application on a WPT system

It was studied in Section 2.1, that an optimum value for Z_{MN} exists, which maximizes η_{Link}. In Section 2.1, we showed that the $Z_{MN_{opt\text{-}\eta}}$ can be achieved by means of an MN. As mentioned before, Z_{MN} can also be adjusted changing the gain of the multiple-gain rectifier. This is further studied in Chapter 4 where both approaches, MN and ac-dc converters, are analyzed together.

In this section, it is shown how the multiple-gain rectifier presented in Section 3.4.1 can be used in a WPT system to adjust Z_{MN}. A simplified system diagram is presented in Fig. 3.37.

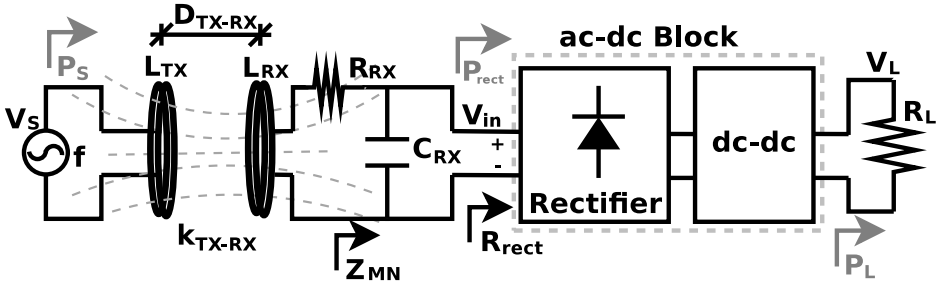


Figure 3.37: Model of wireless power transfer receiver.

Here, a parallel resonator (C_{RX}) is used in the receiver to achieve resonance, the case with a general MN is addressed in Chapter 4. It can be proved that if R_{rect} in (Fig. 3.37) verifies that $(R_{rect}/(wL_{RX}))^2 >> 1$ the value of C_{RX} that achieves resonance is $C_{RX} = 1/(w^2 L_{RX})$, and in that case, Z_{MN} is

$$Z_{MN} = \frac{(wL_{RX})^2}{R_{rect}} - jwL_{RX}. \tag{3.1}$$

$$Z_{MN_{opt}} = R_{RX}\sqrt{1 + {k_{TX\text{-}RX}}^2.Q_{TX}Q_{RX}} - jwL_{RX} \tag{3.2}$$

R_{rect} can be calculated as a function of the ac-dc efficiency $\eta_{ac\text{-}dc} = P_L/P_{rect}$, gain $G_{ac\text{-}dc}$ and the load resistance R_L,

$$P_{rect} = \frac{V_{in_p}^2}{2R_{rect}} = \frac{P_L}{\eta_{ac\text{-}dc}} = \frac{{V_L}^2}{\eta_{ac\text{-}dc}R_L} \Rightarrow R_{rect} = \frac{\eta_{ac\text{-}dc}R_L}{2G_{ac-dc}^2}. \tag{3.3}$$

An expression for the optimum gain that maximizes efficiency can be obtained from (3.1), (3.2) and (3.3)

$$G_{ac\text{-}dc_{opt}} = \sqrt{\frac{\eta_{ac\text{-}dc}\sqrt{1 + {k_{TX\text{-}RX}}^2.Q_{TX}Q_{RX}}}{2Q_{RX}}\frac{R_L}{wL_{RX}}}. \tag{3.4}$$

As can be seen, this optimum gain $G_{ac\text{-}dc}$ should be modified when the load, R_L, distance or orientation hence $k_{TX\text{-}RX}$ changes, in order to remain working near the MEP. The action of dynamically adjust the RX to achieve the MEP is referred to as Maximum Efficiency Point Tracking (MEPT).

Most of the multiple-gain rectifiers in the state of the art have only two different gains x2x4 [108] or x1x2 [30, 109, 110]. The proposed multiple-gain x1-x2-x3 rectifier provides a better regulation under a wider R_L and $k_{TX\text{-}RX}$ ranges.

In this WPT system, we used the same two-turn copper wire 50.8x72.2 mm coils for transmitter and receiver. The target distance is between 5 to 10 cm. The coil was implemented and measured at 1 MHz in order to obtain its characteristics, $L_{TX} = L_{RX} = 931$ nH, $R_{TX} = R_{RX} = 146\text{m}\Omega$ and thus $Q_{TX} = Q_{RX} \simeq 40$.

The $\eta_{ac\text{-}dc}$ for different R_L and $G_{ac\text{-}dc}$ was presented in Fig. 3.37. Using (3.1) and (3.3) to estimate Z_{MN}, the link efficiency η_{Link} was calculated from (2.7) for different ac-dc converter gains $G_{ac\text{-}dc}$, distances $D_{TX\text{-}RX}$, and load resistance R_L. We are assuming that the coils are coplanar and aligned. $k_{TX\text{-}RX}$ was derived from electromagnetic simulation using CST. Therefore, $\eta_{TOT}{=}P_L/P_S{=}\eta_{Link}{\cdot}\eta_{ac\text{-}dc}$ is presented in Fig. 3.38.

As can be seen, for the distance range of interest, a three-gain x1-x2-x3 reconfigurable rectifier allows a load variation between 80Ω and $5k\Omega$ while preserving efficiency.

3.4.4 Conclusion of Section 3.4

A novel series-parallel architecture for an active-rectifier was proposed. The architecture uses the same modular architecture presented in Section 3.1 for a dc-dc

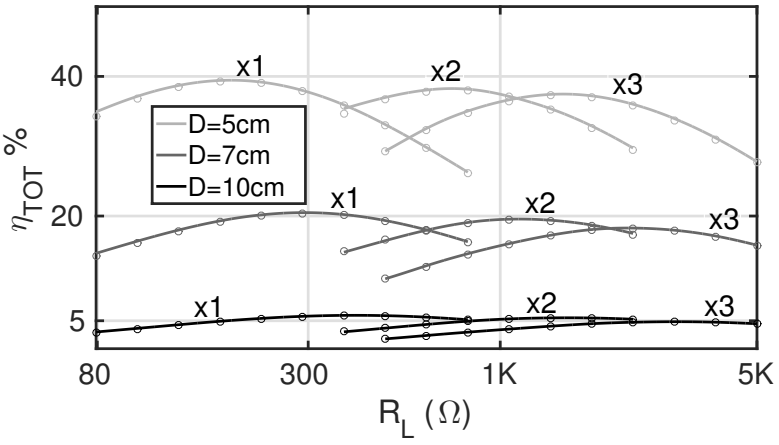


Figure 3.38: Simulated link efficiency using the proposed ac-dc converter.

converter with active switches like the ones presented in Section 3.3. This modular architecture allows multiple conversion ratios compared to others previous works.

A proof-of-concept circuit with three conversion ratios x1-x2-x3 was designed and simulated in 130nm. Additionally, its performance was assessed in a 2-coil WPT system achieving an almost constant efficiency under a wide output power variation range.

The use of converters to adjust Z_{MN} is further analyzed in Chapter 4 where both techniques, MN and ac-dc converters are jointly designed.

Chapter 4

Receiver design: matching networks vs adjustable ac-dc converters

This section addresses two approaches for adjusting Z_{MN}: MNs and adjustable ac-dc converters. The use of MNs was discussed in Section 2.1 and the use of an adjustable gain converter to adjust Z_{MN} was introduced in Section 3.4.3. In particular, in the remaining sections, it is discussed which is the optimum way to combine these two approaches. A simplification of the diagram presented in Fig. 1.2 is depicted in Fig. 4.1, focused on the two main blocks addressed in this section, the MN and the ac-dc block. Figure 4.1 outlines the notation for voltages, powers, impedances, and efficiencies.

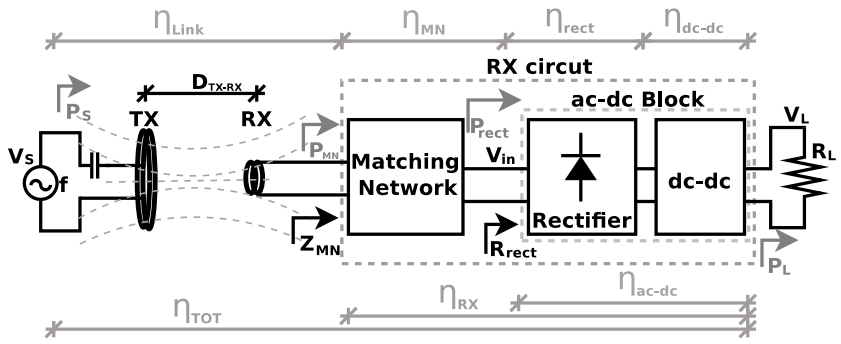


Figure 4.1: Block diagram of a WPT system. P_S, P_{MN}, P_{rect} and P_L are the transmitter's driver output power, receiver MN input power, ac-dc block input power, and output power, respectively. Z_{MN} and R_{rect}, are the MN input impedance and ac-dc block input resistance, respectively. Each intermediate efficiency is indicated, the total system efficiency is $\eta_{TOT} = P_L/P_S = \eta_{Link}.\eta_{MN}.\eta_{rect}.\eta_{dc\text{-}dc}$. To simplify the notation, $\eta_{ac\text{-}dc} = \eta_{rect}.\eta_{dc\text{-}dc}$ and $\eta_{RX} = \eta_{MN}\eta_{rect}.\eta_{dc\text{-}dc}$ were also defined.

The MNs are a straightforward method to achieve the optimum load value [3, 42]. It allows modifying both the imaginary and the real part of Z_{MN} to achieve its optimum value $Z_{MN_{opt\text{-}\eta}}$. The imaginary part of $Z_{MN_{opt\text{-}\eta}}$ should cancel the receiver coil impedance jwL_{RX}, in order to achieve resonance which maximizes

power transfer efficiency [25]. The referred optimum value for the real part that maximizes efficiency is given by

$$Re\{Z_{MN_{opt\text{-}\eta}}\} = R_{RX}\sqrt{1 + {k_{TX\text{-}RX}}^2.Q_{TX}Q_{RX}}. \tag{2.9}$$

This equation 2.9 was deduced in Section 2.1.

The commonly used series or parallel resonance capacitor [29, 30, 109, 111] can be thought of as a particular case of an MN that only adjusts the imaginary part. The series resonator modifies the imaginary part without altering the real one. Conversely, the parallel resonator modifies the real part. However, this modification cannot be selected as desired because only one degree of freedom is available and it is used to achieve resonance.

As can be seen from (2.9), the optimum real part depends on the coils' properties and the coupling factor. Additionally, the input impedance of an MN depends on its load impedance (R_{rect}). Thus, if the load power consumption varies (R_L changes), so does R_{rect}, requiring a different MN. Therefore, the MN that optimizes the system changes if the distance ($D_{TX\text{-}RX}$) or R_L change. Although it can be done, it is not easy to switch between different MNs since it requires many components and switches adding complexity to the system and, possibly, jeopardizing its performance. Therefore, fixed MNs are usually used [3, 42, 112]. In [42] maximum link efficiency was achieved in the case of 2-coil links while [3] addressed the use of MNs in 3-coil links. MNs also have been applied to fulfill other goals. In [112] the MN was included in the transmitter, to control the driver's load impedance variations due to changes in the coupling factor ($k_{TX\text{-}RX}$). MNs have losses which depend on the components used (capacitor or inductor) and their values [113]. The MN power efficiency can be defined as $\eta_{MN} = P_{rect}/P_{MN}$ (see Fig. 4.1).

An alternative to achieve $Re\{Z_{MN_{opt\text{-}\eta}}\}$, is to control the input resistance of the ac-dc block (R_{rect}, Fig. 4.1), as in Section 3.4.3 and [29–31, 33, 35]. In [29, 30] a reconfigurable gain rectifier is used, while [31, 33, 35] have a fixed rectifier followed by a dc-dc converter with variable conversion ratio. In those papers, R_{rect} is modified to dynamically control $Re\{Z_{MN}\}$, and a fixed MN (series or parallel resonant capacitor) is used to set the imaginary part ($Im\{Z_{MN}\}$) and hence achieve $Z_{MN_{opt\text{-}\eta}}$.

In this study, we model the ac-dc block input impedance (R_{rect}) in a first-order approximation as a real impedance, as in [29, 33, 35, 114]. Our measurement results and their agreement with the theoretical model further validate this approximation. Nevertheless, if the imaginary part of the input impedance of the ac-dc block cannot be neglected, it could be modeled through a parallel parasitic capacitor, as done in [30]. During the MN design, this parasitic capacitor should be considered to achieve resonance.

The converter efficiency should be taken into account as it will impact the overall efficiency ($\eta_{TOT} = \eta_{Link}.\eta_{MN}.\eta_{ac\text{-}dc}$) and the improvements in η_{Link} by achieving $Z_{MN_{opt\text{-}\eta}}$ could be lost due to low $\eta_{ac\text{-}dc}$.

Changes in the MN or the ac-dc converter gain alter the output voltage V_L if the rest of the system is not correspondingly adjusted to maintain a fixed V_L. The output voltage regulation in this context will be addressed in Section 4.3. Further details regarding closed-loop voltage regulation are presented in Chapter 5.

Low-frequency analog designers usually do not use MNs to achieve impedance matching in their designs, while an MN is often included in radio frequency (RF) circuits. This could be the reason why many works do not include a general MN in the receiver and only a resonant capacitor is used before the ac-dc block, e.g., [29, 30, 109] that work at 40.68 MHz, 1 MHz and 13.56 MHz, respectively. However, studies in the same frequency range have been published showing the improvements in efficiency and output voltage achieved by using MNs, e.g., [42,43] that work at 13.56 MHz and 4 MHz, respectively. These works [42, 43], analyze the advantages of MNs in WPT, however, they do not consider the possibility of jointly using an adjustable ac-dc converter like the one used in [29,30,109]. In [35] it was appropriately highlighted that in a high power transfer environment (tens of watts) the MN can reduce the overall efficiency. However, at lower power levels, $P_L = 10$ mW in [42] and $P_L = 2$ W in [43] the advantages of MN have been proved.

In this section we analyze, for the first time, how both methods (general MNs and adjustable ac-dc converters) can be used together to design an inductive (near-field) WPT system exploiting the advantages of each method. A general approach regarding the design of both circuits is established and a proof-of-concept system working at 13.56 MHz and delivering between 1 mW to 5.6 mW is presented. Compared to a traditional design which uses a parallel resonance capacitor, the proof-of-concept system has improvements in measured efficiencies up to 80% at the largest distances (4.5 cm-5.5 cm), thus maximizing the distance range ($\simeq 20\%$ increase). A step-up ac-dc converter is considered a direct way to increase V_L (e.g., [109] and this could also be an initial intuitive vision). However, we show that the use of a step-up may end up reducing V_L and the highest output voltage is achieved using only an MN. Measurements of a proof-of-concept system, show that the maximum output voltage achieved following the proposed design flow was 90% higher (from 1.36 V to 2.59 V) than the case where a step-up converter is used.

This chapter is organized as follows. Section 4.1 presents a theoretical analysis of achieving the optimum Z_{MN} using either an MN or an adjustable ac-dc converter. The joint design applying both an MN and adjustable ac-dc is studied in Section 4.2. Section 4.3 describes different methods to regulate V_L showing that the proposed design is compatible with V_L regulation techniques. A proof-of-concept circuit is designed in Section 4.4 and the measurement results are presented in Section 4.5. Finally, the main conclusions of this work are drawn in Section 4.6.

4.1 Optimum Z_{MN} study

In this section, we will first discuss a general analysis and the implications of achieving the optimum Z_{MN}. Then, the use of MNs (Section 4.1.1) and adjustable ac-dc converters (Section 4.1.2) are studied, while the joint design with both blocks together (MN+ac-dc) is presented in Section 4.2. Additionally, two alternative methods to achieve the desired Z_{MN} are discussed in (Section 4.1.3).

The MN and the ac-dc converter (from now on referred to as the RX-circuit, see Fig. 4.1) can be modeled as a block that sets a certain input impedance Z_{MN}

in the input ac terminal, and that provides a dc output voltage V_L with a specific efficiency $\eta_{RX} = \eta_{MN}.\eta_{ac\text{-}dc} = P_L/P_{MN}$. This simplified model is depicted in Fig. 4.2.

The link efficiency η_{Link} (2.7) was deduced in Section 2.1 [3, 38].

$$\eta_{Link} = \frac{P_{MN}}{P_S} = \frac{Q_{RX\text{-}L}}{Q_L} \frac{{k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L}}{{k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L} + 1} \tag{2.7}$$

It can be noted that, the RX-circuit only affects the η_{Link} by its input impedance Z_{MN} that affects Q_L.

Therefore, the total efficiency ($\eta_{TOT} = \eta_{Link}.\eta_{RX}$) is maximized when the RX-circuit achieves $Z_{MN_{opt\text{-}\eta}}$ (given by (2.9), maximizing η_{Link}) with the highest possible η_{RX}.

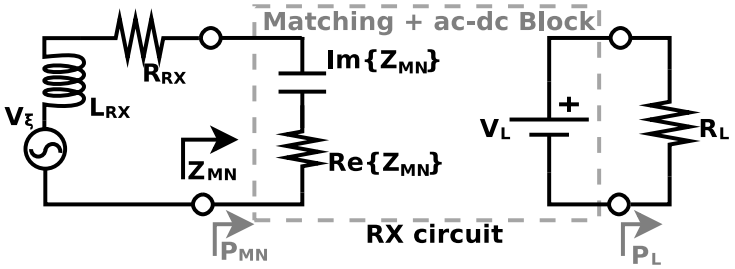


Figure 4.2: Simplified model of the MN and ac-dc converter to analyze matching at the receiver. L_{RX} and R_{RX} are the inductance and parasitic resistance of the receiver coil respectively while V_ξ is the voltage induced in it.

On the other hand, the power that reaches the MN (P_{MN}) can be calculated as (4.1) [38], where g_{Link} was defined to simplify the notation. An optimum value for Z_{MN} (which we will call $Z_{MN_{opt\text{-}V}}$) that maximizes P_{MN} for a given transmitter voltage V_S exists (4.2), and is different from (2.9).

$$P_{MN} = \frac{Q_{RX\text{-}L}}{Q_L} \frac{{k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L}}{({k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L} + 1)^2} \frac{{V_S}^2}{2R_{TX}} = g_{Link}(Re\{Z_{MN}\}).{V_S}^2 \tag{4.1}$$

$$Re\{Z_{MN_{opt\text{-}V}}\} = R_{RX}(1 + {k_{TX\text{-}RX}}^2.Q_{TX}Q_{RX}) \tag{4.2}$$

The output power P_L can be written as (4.3). Since P_L is equal to the product of P_{MN} and η_{RX}, it is maximized when (4.2) holds (thus maximizing P_{MN}) with the highest η_{RX} possible.

$$\frac{{V_L}^2}{R_L} = P_L = \eta_{RX} P_{MN} \overset{(4.1)}{\Longrightarrow} P_L = \eta_{RX} g_{Link}(Re\{Z_{MN}\}).{V_S}^2 \tag{4.3}$$

The transmitter voltage V_S can be used to regulate the output voltage V_L and thus P_L (4.3), this regulation method is used in this section and will be discussed later. Note that if the driver is able to generate the V_S required to achieve the desired value of V_L, the output power is guaranteed, and the efficiency should be

maximized by holding $Z_{MN_{opt\text{-}\eta}}$ (2.9). However, if V_S reaches its maximum possible value due to the driver limitations, it becomes reasonable to maximize the received power setting $Z_{MN_{opt\text{-}V}}$ (4.2). In the latter case, the design of a new driver could be also considered.

Summarizing, either to obtain the maximum link efficiency or maximum output power, Z_{MN} should be matched to (2.9) or (4.2), respectively; with the highest RX-circuit (MN+ac-dc) efficiency. The desired Z_{MN} can be obtained with different combinations when ac-dc converters and MN are both used. Defining the converter gain as $G_{ac-dc} = V_L/V_{in_p}$ (where V_L is the output dc voltage and V_{in_p} is the peak voltage of the sinusoidal input), different converter gains with its corresponding MN can lead to the same $Z_{MN_{opt}}$ ($Z_{MN_{opt\text{-}\eta}}$ or $Z_{MN_{opt\text{-}V}}$). However, the total efficiency of each combination of MN and ac-dc (η_{RX}) is not the same, and the maximum should be found.

From this analysis, we can conclude the following, which may be a non-intuitive result at first hand and that if overlooked might lead to inappropriate design decisions. A higher ac-dc gain does not imply a higher output voltage. For example, if we are in the optimum condition of $Z_{MN} = Z_{MN_{opt\text{-}V}}$ given by (4.2), an increase in the ac-dc gain will change Z_{MN} mismatching the input, reducing g_{Link} (4.1), decreasing P_L (4.3) and V_L.

This is validated by experimental results in Section 4.5. Additionally, the proof-of-concept system shows that the maximum V_L is achieved by an MN without the need of any ac-dc step-up (at $G_{ac-dc} = 1$). This is because in order to achieve $Z_{MN_{opt\text{-}V}}$, the MN with a unity gain ac-dc converter (rectifier) has higher efficiency (η_{RX}) than the MN with a step-up ac-dc converter.

Works like [109] have proposed and managed to increase V_L by means of increasing the ac-dc converter gain. It is impossible to reproduce the conditions of [109] as the quality factors of the coils are not given. From our analysis, we conclude that the gain variation proposed by [109] from 1 to 2, increases V_L because it improves the Z_{MN} match (thus increasing $g_{Link}(Re\{Z_{MN}\})$. However, this is not a general situation and it will be demonstrated via practical examples that higher gain may generate lower output voltages. This issue regarding the design presented in [109] was pointed out by [30] but it was not analyzed in a general way.

Section 4.2 addresses the problem of how the MN and adjustable ac-dc converter should be jointly designed in order to maximize the total efficiency η_{TOT} under different distances $D_{TX\text{-}RX}$ and load resistances R_L. In the following subsections, we present separately a brief analysis of the impedance transformations performed by an MN (Section 4.1.1) and an ac-dc converter (Section 4.1.2).

4.1.1 Matching network analysis

An MN can be implemented in very different ways. Transmission line impedance transformers are often used at high frequencies, where the wavelength is comparable to the circuit size. In near-field inductive applications (around MHz) lumped matching methods are the most appropriate ones. Many different lumped MN

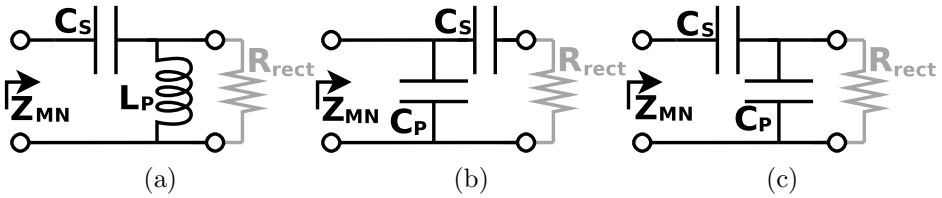


Figure 4.3: Three of the eight different L-Match MNs. (a) Was used in [42]. (b) Was used in [43]. (c) Is going to be used in the proof-of-concept circuit in Section 4.5.

architectures exist like L-Match, π-Match, T-Match, among other combinations. In the particular case of L-Match, 8 different combinations exist using inductors and capacitors, three of them are presented in Fig. 4.3.

The series or parallel capacitor, commonly used to achieve resonance at the receiver, can be considered as a particular case of L-match where one component has zero or infinite impedance. In that case, that particular MN has only one design variable that is usually set to resonate ($Im\{Z_{MN}\} = -wL_{RX}$) without purposely adjusting $Re\{Z_{MN}\}$. This series or parallel resonant capacitor, and even the series-shunt topology of Fig. 4.3b, which was applied in [43], are usually referred to as resonant structures instead of MNs.

Each MN topology has different characteristics such as frequency response, component values, efficiency and $Re\{Z_{MN}\}$ proportional or inversely proportional to R_{rect}. Additionally, they are differently affected by parasitic capacitances in its input (capacitance of the coil) and in its output (rectifier input capacitance). Which architecture can be used mainly depends on R_{rect} and $Z_{MN_{opt}}$ ($Z_{MN_{opt\text{-}\eta}}$ or $Z_{MN_{opt\text{-}V}}$) since not every impedance transformation can be achieved with each MN. A detailed analysis of MN properties can be found in classical reference works [113, 115]. In the remaining of this subsection, we present some general considerations, particularly regarding the MN used in the proof-of-concept circuit (Section 4.5).

For example, for the MN presented in Fig. 4.3c, Z_{MN} is given by

$$Z_{MN} = \frac{R_{rect}}{(R_{rect}wC_P)^2+1} - \left(\frac{1}{wCs} + \frac{{R_{rect}}^2 wC_P}{(R_{rect}wC_P)^2+1}\right)j. \tag{4.4}$$

Based on (4.4), it is evident that the MN presented in Fig. 4.3c can only be used if $Re\{Z_{MN_{opt}}\} < R_{rect}$. In this case, it is desirable to have $(R_{rect}wC_P)^2 >> 1$, hence $Im\{Z_{MN}\}$ (resonance) is not altered by R_{rect} variations. Under that condition, $Re\{Z_{MN}\}$ is inversely proportional to R_{rect}.

The efficiency of an MN depends on the quality factor of the components used, $Q_{L_{lumped}} = wL/R_{p_L}$ for an inductor and $Q_{C_{lumped}} = 1/(wCR_{p_C})$ for a capacitor (where R_{p_L} and R_{p_C} are the parasitic series resistances of the inductor and capacitor, respectively) [113]. The higher the component quality factor is, the better the resulting MN efficiency will be. MNs that only use capacitors like the ones shown in Fig. 4.3b and Fig. 4.3c are preferred as $Q_{C_{lumped}} >> Q_{L_{lumped}}$ for most practical cases [113].

4.1.2 AC-DC Converter analysis

A rectifier is usually needed since most loads require a dc supply voltage. As it was previously discussed, a dc-dc converter after the rectifier can be used to adapt Z_{MN} [31–33, 35]. In order to avoid an additional block, different variable gain rectifiers have been proposed [29, 30, 109, 110] trying to improve the ac-dc efficiency and reduce the circuit size.

Either using a rectifier and a dc-dc or a variable gain rectifier, it is easy to dynamically modify the block gain in order to approximately maintain the $Z_{MN_{opt}}$ when the distance $D_{TX\text{-}RX}$ or the R_L varies.

Different architectures have been considered to implement this ac-dc block. In [35] a rectifier followed by a buck converter in continuous conduction mode is presented. The buck converter duty cycle is used to adjust R_{rect}. In [32] it was proved that a buck converter in discontinuous conduction mode presents an input resistance that is independent of the converter input voltage and load resistance. In microwave power transfer as in [32], the optimum impedance is not affected by the transmitter to receiver distance, thus the converter that they propose can be designed to assure optimum impedance $Z_{MN_{opt}}$ under distance and power consumption variations without any dynamic adjustment. However, in the case of inductive powering, $Z_{MN_{opt}}$ also depends on the transmitter to receiver distance, so the converter proposed by [32] can be used to have a Z_{MN} independent of R_L but its duty cycle must be adjusted to withstand the distance variations.

Another approach is to use a reconfigurable structure able to change the converter gain as studied in Section 3.4 and in [29, 30, 109, 110]. Converters that do not need an additional inductor are preferred due to size constraints in the receiver that many applications have, such as AIMDs. For a converter with gain $G_{ac-dc} = V_L/V_{in_p}$ (where V_L is the output dc voltage and V_{in_p} is the peak voltage of the sinusoidal input), efficiency $\eta_{ac\text{-}dc}$ and load resistance R_L, the input resistance R_{rect} (Fig. 4.1) was calculated in (3.3) (Section 3.4.3).

$$P_{rect} = \frac{V_{in_p}^2}{2R_{rect}} = \frac{P_L}{\eta_{ac\text{-}dc}} = \frac{{V_L}^2}{\eta_{ac\text{-}dc}R_L} \Rightarrow R_{rect} = \frac{\eta_{ac\text{-}dc}R_L}{2G_{ac-dc}^2} \tag{3.3}$$

Therefore, the input resistance R_{rect} can be modified by changing G_{ac-dc}.

Regardless of the converter architecture, the possible range of R_{rect} and thus Z_{MN} is limited due to converter limitations. For instance, if a variable gain converter is used, the gain (G_{ac-dc}) is limited since very high or low gains will jeopardize efficiency. Additionally, it may also lead to very high or very low converter input voltage because $V_{in_p} = V_L/G_{ac-dc}$.

4.1.3 Other methods to achieve $Z_{MN_{opt}}$

It should be mentioned that other ways to achieve the optimum Z_{MN} also exist. This section describes in general two alternative methods that are not going to be considered in the joint design of Section 4.2 for the reasons explained here.

A relatively new method was proposed in [116, 117] which consists of shorting the load in order to modulate the receiver coil quality factor and dynamically track

$Z_{MN_{opt\text{-}\eta}}$. In [117] the proposed technique was compared on a prototype with the case where no technique is used at all to achieve $Z_{MN_{opt\text{-}\eta}}$, showing a large improvement in efficiency (from 10.5% to 32.5% in total efficiency). However, the maximum theoretical link efficiency that could be achieved in that prototype using the coils and coupling factor that the authors report ($Q_{TX} = 187$, $Q_{RX} = 93.7$ and $k = 0.044$) is around 70%. This maximum theoretical efficiency was calculated from the well-known expression (2.42). This means that although this technique improves the efficiency, it is still much lower than the theoretical limit of the link.

Another way to optimize the system is present in links with more than two coils [36], where $Z_{MN_{opt}}$ depends on the quality factor and coupling factor between all the coils. Therefore, the optimal $Z_{MN_{opt}}$ can be adapted to match Z_{MN} changing, e.g., the extra coils' position or radius [37, 38, 108]. This approach to achieve $Z_{MN_{opt}}$ was discussed in Section 2.1 where it was shown that an MN is needed anyway. In addition, the extra coil position and radius are not easy to adjust dynamically. For simplicity, we are presenting the analysis for a 2-coil inductive link. Although the value of $Z_{MN_{opt}}$ changes for systems with more than two coils, the general analysis regarding the design of MN and ac-dc converter to achieve the optimal Z_{MN} is independent of the number of coils used.

4.2 MN and AC-DC converter joint design

Section 4.1 highlighted that the RX-circuit should be designed to achieve $Z_{MN_{opt\text{-}\eta}}$ (2.9) or $Z_{MN_{opt\text{-}V}}$ (4.2) with maximum efficiency η_{RX}. It was also shown that either an MN or an ac-dc converter can be used to match Z_{MN}. In the previous sections 4.1.1 and 4.1.2, a general description of the constraints and trade-offs in the design of each circuit was presented. Summarizing these two sections (4.1.1 and 4.1.2), Table 4.1 presents the advantages and disadvantages of each approach regarding Z_{MN} matching in inductive WPT systems.

The main idea of the joint design is to exploit the advantages of each circuit (MN and ac-dc). The MN is used for a large $Re\{Z_{MN}\}/R_L$ adaptation range providing high efficiency, and the ac-dc converter is used to dynamically adjust variations in $D_{TX\text{-}RX}$ and R_L. We assume that the coils were designed to have high coupling and quality factor and their values are given as their design is out of the scope of this section. The converter efficiency $\eta_{ac\text{-}dc}$ depends on the coils distance $D_{TX\text{-}RX}$ and the load R_L since the converter will be adjusted to achieve $Z_{MN_{opt}}$ under $D_{TX\text{-}RX}$ and R_L variations, hence $\eta_{RX} = \eta_{MN}\eta_{ac\text{-}dc}$ also depends on these parameters. Therefore, the design presented in this section aims to obtain the maximum η_{RX} when η_{Link} is low (at large $D_{TX\text{-}RX}$) and the load is consuming high power (at low R_L). This situation of maximum distance and load power consumption will be referred to as the critical point, and the subscript "crit" is added in variables to indicate their value at that situation. If this design goal is achieved in this worst case scenario, when power consumption or distance is lower, additional losses can be tolerated in the RX-circuit to adapt Z_{MN}. As a result, this design maximizes the distance that can be achieved by having the highest η_{RX} when η_{Link} is the lowest.

Table 4.1: Matching Network (MN) and ac-dc converter comparison.

	MN	ac-dc
Conversion ratios $Re\{Z_{MN}\}/R_L$	Wide range	Limited range
Dynamic adaptation	Many components and switches. Complex system, jeopardizing efficiency	Easier to implement
Efficiency	Very high if only capacitors are used	High but depends on conversion ratio R_{rect}/R_L and P_L
Can be integrated ?	NO (in the few MHz or lower frequency range), but a resonant element is needed anyway	YES. However, most ac-dc blocks (e.g., @ $P_L \simeq 10$ mW) require external capacitors or inductors

In order to clarify the design procedure, Fig. 4.4 presents a simplified design flow diagram, which is described next.

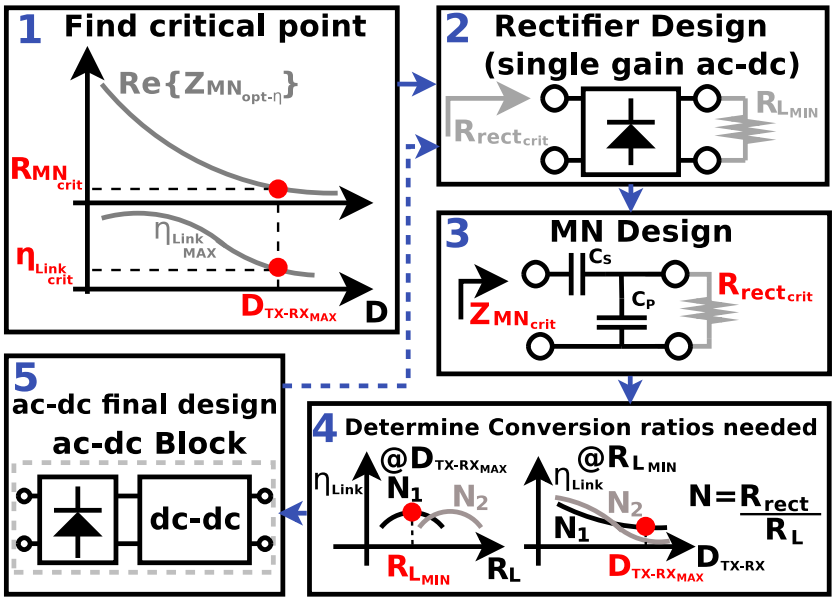


Figure 4.4: Simplified design flow diagram.

In **step 1**, the maximum $D_{TX\text{-}RX}$ (critical point) should be determined. To do so, the maximum efficiency $\eta_{Link_{MAX}}$ that can be obtained for each $D_{TX\text{-}RX}$ is plotted. As previously explained, this $\eta_{Link_{MAX}}$ is calculated from (2.7) assuming

that the $Re\{Z_{MN_{opt\text{-}\eta}}\}$ (2.9) is set, which leads to (2.42) [3, 21].

$$\eta_{Link_{MAX}} = \frac{{k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX}}{(\sqrt{1 + {k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX}} + 1)^2} \tag{2.42}$$

Since (2.42) depends solely on the coils' properties, $\eta_{Link_{MAX}}$ is determined by the coils design. The total efficiency η_{TOT} will be lower than $\eta_{Link_{MAX}}$ (2.42) due to the RX-circuit losses that define η_{RX}. Consequently, if a minimum acceptable link efficiency $\eta_{Link_{crit}}$ is set, the maximum $D_{TX\text{-}RX}$ ($D_{TX\text{-}RX_{MAX}}$, k_{crit}) can be found for the given coils, and also $Re\{Z_{MN_{opt\text{-}\eta}}\}$ from (2.9). The $Re\{Z_{MN_{opt\text{-}\eta}}\}$ in the critical situation is defined as $R_{MN_{crit}}$. From (4.1) and (4.3) using k_{crit} and $Re\{Z_{MN}\} = R_{MN_{crit}}$ the V_S needed to transmit the desired power at the critical point, $V_{S_{crit}}$, can be calculated. The transmitter should be able to impose that voltage $V_{S_{crit}}$, otherwise $Z_{MN_{opt\text{-}V}}$ could be chosen instead of $Z_{MN_{opt\text{-}\eta}}$ or the transmitter's driver should be modified.

In **step 2**, the ac-dc block is designed to rectify the signal at the working frequency and deliver up to the maximum power consumed by the load ($R_L = R_{L_{MIN}}$). Additionally, this ac-dc block should be designed to obtain maximum efficiency ($\eta_{ac\text{-}dc}$), without considering impedance matching. Therefore, a high-efficiency block with a non-optimized input impedance is obtained. At this stage, the adaptive part of the circuit that regulates R_{rect} has not been designed yet. This step can be interchanged with the first one as they are independent.

In **step 3**, the MN is designed to match the load ($Z_{MN_{opt}}$) at the critical situation. Therefore, it will convert $R_{rect_{crit}}$ (at maximum P_L, $R_{L_{MIN}}$) into $R_{MN_{crit}} - jwL_{RX} = Z_{MN_{opt-crit}}$ which is the optimum value of Z_{MN} at the critical point as it was calculated in step 1. The value of $R_{rect_{crit}}$ is obtained from step 2.

At this stage, the RX-circuit was designed to work optimally at the critical point, with an ac-dc converter ratio fixed in step 2, $R_{rect_{crit}}/R_{L_{MIN}} = N_1$. Now in **step 4**, since the MN is already designed, the link efficiency (2.7) as a function of R_L and $D_{TX\text{-}RX}$ can be found for different ac-dc impedance conversion ratios (R_{rect}/R_L). This is performed to determine the conversion ratios needed to assure high efficiency under the expected R_L and $D_{TX\text{-}RX}$ variations.

Finally in **step 5**, the converter design can be completed as the required input resistance conversion ratios R_{rect}/R_L and their load power (R_L) are known. To do this two different approaches can be taken, add a dc-dc converter after the block designed in step 2 [31, 33, 35], or modify the rectifier designed in step 2 to include multiple ac-dc gains as was proposed in [29, 30]. In the case that a dc-dc converter is added, it will be bypassed at the critical point due to the fact that the system was already optimized at that point in step 3. Therefore, the efficiency at the critical point is not reduced and the maximum distance is maintained. If any limitation occurs during this step to reach the required conversion ratios, it is necessary to go back to step 2 and modify the architecture or design selected at that step.

This design procedure is applied on an actual system in Section 4.4.

4.3 Output voltage regulation

In most practical cases, the output voltage V_L should be maintained constant under $D_{TX\text{-}RX}$ and R_L changes. Although the detailed implementation of the output regulation is out of the scope of this section, we will describe different approaches in order to show that our proposed analysis and design can be applied in conjunction with output voltage regulation methods. A further analysis of the feedback loops not only to regulate the output voltage but also to track the maximum efficiency, is presented in Chapter 5.

Figure 4.5 depicts different approaches for regulating V_L. In (B) [118] a variable capacitor is used to tune or detune the MN, while in (C) [119] the transmitter signal frequency is changed detuning both transmitter and receiver. Therefore, both methods adjust V_L by reducing the system efficiency. In these approaches, an adjustable ac-dc converter is not needed and maximum efficiency is not achieved, thus the proposed joint design is not applicable.

In approach (A) [29, 120], the output voltage is regulated by changing the transmitter voltage V_S. In this method, as in (C), back-telemetry is needed so that the value of V_L is known at the primary side. In works like [121] (D) a fedback dc-dc converter is used to regulate V_L directly in the receiver. In this case, the converter gain G_{ac-dc} depends on V_{in} (Fig. 4.5) which can be modified by changing V_S. In [121] V_S is used to adjust G_{ac-dc} until $Z_{MN_{opt}}$ is achieved. This (D) feedback loop is further analyzed in Chapter 5.

Therefore, in (A) the ac-dc converter gain is adjusted to achieve $Z_{MN_{opt}}$ and then V_S is modified in order to obtain the desired V_L. While in (D), the converter gain is set to maintain V_L constant and V_S can be adjusted to obtain $Z_{MN_{opt}}$. In both cases, the optimum final situation is the same. The only difference is the dynamic that drives each method (A, D) to its optimal situation described in Section 4.2. The general analysis presented here can be used to design the MN and ac-dc, then each method (A, D) will take different paths to find the G_{ac-dc} and V_S needed. In the proof-of-concept system of this chapter, we will take approach (A) to regulate V_L.

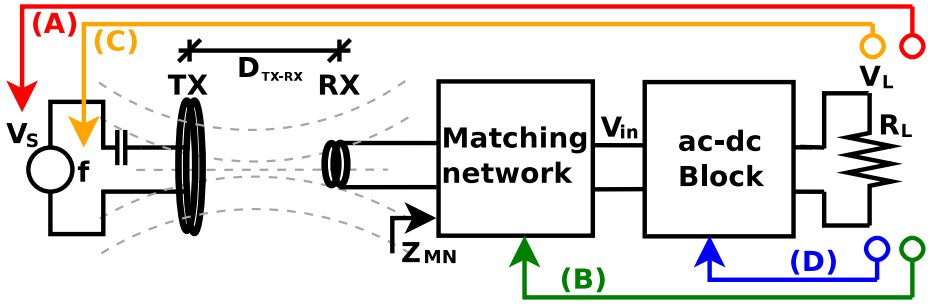


Figure 4.5: Approaches to adjust the output voltage. (A) modifing transmitter amplitude [29, 120]. (B) tuning or detuning the resonant structure [118]. (C) changing the transmitter frequency [119]. (D) adjusting the ac-dc block gain [121].

4.4 Proof-of-concept system design

In order to validate the analysis of the optimization of the WPT link through the joint use of an MN and a dc-dc converter, a proof-of-concept system was designed and measured using off-the-shelf components. The system is presented in Fig. 4.6 and Table 4.2. The carrier frequency was fixed at $f = 13.56$ MHz in the industrial, scientific and medical band. The load to be powered consumed between 1 mW to 5.6 mW at $V_L = 2.6$ V ($R_L = \{1.2 - 7\}$ kΩ) thus the system should be designed to maintain high efficiency under this load variation. In this example, we will use a rectifier followed by a dc-dc step-up converter to implement the ac-dc block.

The design presented in Section 4.2 is applied here for this proof-of-concept system.

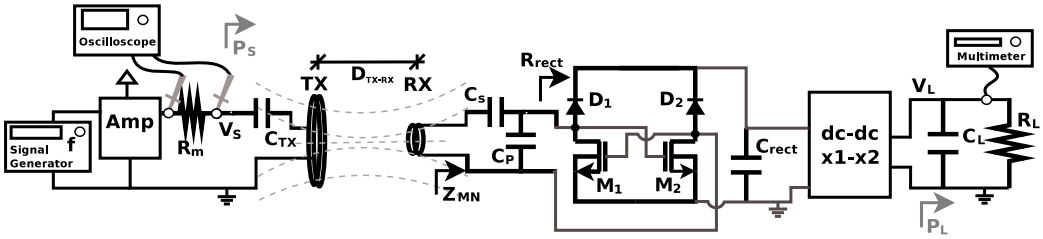


Figure 4.6: Proof-of-concept system and measurement setup.

Table 4.2: Proof-of-concept system components.

Component	Description
L_{TX}	Pulse Elec. W7002, $L_{TX} = 1.18$ μH $Q_{TX} = 95.7$ [1,2]
L_{RX}	Pulse Elec. W7001, $L_{TX} = 877$ nH $Q_{TX} = 27.2$ [1]
C_{TX}	Johanson Tech. (501S42E-JV4S) $C_{TX} = 1/(w^2 L_{TX})$
C_S, C_P	Murata (GRM15-KIT-C0G-DE) [3]
D_1 D_2	Diodes Incorporated, Schottky (SDM10U45-7)
M_1 M_2	Vishay Siliconix, MOSFET N-CH 20 V 0.63 A SC-75 A (SI1012CR-T1-GE3)
C_{rect}, C_L	Murata 3.3 μF (GRM21BR61C335KA88L)
dc-dc	x2: ON Semiconductor NCP1729 Doubler, x1: bypassed
R_L	$R_L = \{1.2 - 7\}$ kΩ $V_L = 2.6$ V $P_L \simeq \{1 - 5.6\}$ mW

NOTE 1– Measured values at 13.56 MHz, including coil's connector and PCB paths. NOTE 2– One turn of the W7002 coil was removed to increase self-resonant frequency and Q_{TX}. NOTE 3– Adjusted to comply with (4.4).

Step 1: Measuring the coils coupling ($k_{TX\text{-}RX}$) and quality factors (Q_{TX} and Q_{RX}), $\eta_{Link_{MAX}}$ can be plotted from (2.42), and it is presented in Fig. 4.7. In this example it is assumed that the minimum acceptable η_{TOT} is around 10%. Considering the RX-circuit losses (η_{RX}) and including a safety margin, the maximum

transmission distance (critical point) using these coils is 5.5 cm, and $R_{MN_{crit}} = 3.5\ \Omega$.

Step 2: Based on the working frequency and maximum output power expected, we designed an ac-dc block (rectifier) shown in Fig. 4.6 and its components described in Table 4.2. In this design, the goal was to maximize efficiency, and the converter input impedance was not considered in its optimization. The designed converter achieves an efficiency of $\eta_{ac\text{-}dc} = 85\%$ when delivering maximum power $R_L = R_{L_{MIN}} = 1.2\ \text{k}\Omega$ ($P_L = 5.6$ mW). The selected architecture for the rectifier has unitary gain since its output dc voltage is ideally equal to its peak input voltage $G_{ac-dc_{crit}} = V_L/V_{in_p} \simeq 1$. The input impedance can be approximated using (3.3), and it is presented in (4.5).

$$R_{rect_{crit}} = \frac{\eta_{ac-dc_{crit}} R_{L_{MIN}}}{2.G^2_{ac-dc_{crit}}} = \frac{0.85 \times 1200\ \Omega}{2} = 510\ \Omega \tag{4.5}$$

We selected this architecture because, in this frequency range, rectifiers with unitary gain present higher efficiency than doublers and other more complex architectures. However, in other applications, the rectifier that achieves maximum efficiency could have a different gain and the rest of the design flow is not affected.

Step 3: The MN should be designed to transform the $R_{rect_{crit}}$ calculated in (4.5) (step 2) into $Z_{MN_{opt-crit}} = R_{MN_{crit}} - jwL_{RX} = (3.5 - 74.7j)\ \Omega$ (obtained in step 1). This design assures that at the critical point ($D_{TX\text{-}RX_{MAX}}$ and $R_{L_{MIN}}$) $Z_{MN_{opt}}$ is achieved, and the ac-dc converter is working at the point where it was designed to work.

In this case, it is possible to design the MN using the configuration presented in Fig. 4.3c which only uses capacitors, obtaining a very high η_{MN}. From (4.4), the capacitors values can be calculated to achieve resonance ($Im\{Z_{MN}\} = -jwL_{RX}$) and maximize efficiency ($Re\{Z_{MN}\} = R_{MN_{crit}}$), $C_P = 277.8$ pF and $C_S = 361.6$ pF. The MN efficiency can be estimated to be $\eta_{MN} > 97\%$ from the conversion ratio $R_{rect_{crit}}/R_{MN_{crit}} = 510\ \Omega/3.5\ \Omega$, and the capacitor quality factors that are in this case higher than 1000 (using GRM15-KIT-C0G-DE) [113]. The MN efficiency will be approximated $\eta_{MN} \simeq 1$ since such a high value is difficult to measure and in many cases will be dominated by the length of the PCB paths instead of the capacitors' quality factors. The values of C_P and C_S are estimations and trimming is needed due to parasitic capacitances.

Step 4: In this design, we will use a variable gain dc-dc converter after the rectifier designed in step 2 in order to adjust Z_{MN}. Therefore, to estimate the gains needed we calculate η_{Link} for different R_L and G_{ac-dc} using (3.3) to calculate R_{rect}, (4.4) to obtain $Re\{Z_{MN}\}$ and thus Q_L, and (2.7) to get η_{Link}. From this analysis, we conclude that two gains (x1, x2) are sufficient to work near $Z_{MN_{opt\text{-}\eta}}$ for the distance range and output power consumption expected. The η_{TOT} for different G_{ac-dc} and $D_{TX\text{-}RX}$ is presented in Section 4.5.

Step 5: In this case, we are not designing a specific dc-dc converter for this application. The NCP1729 from ON semiconductor was used connected as a doubler to achieve $G_{ac-dc} \simeq 2$, and it was turned off and bypassed to obtain $G_{ac-dc} \simeq 1$.

This design is validated through measurements in the next section.

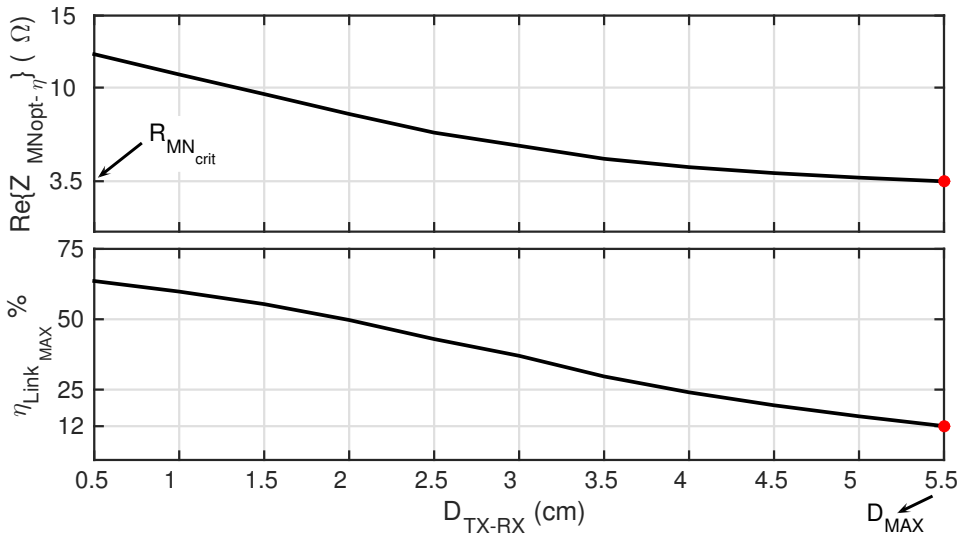


Figure 4.7: Proof-of-concept system maximum efficiency (2.42), and real part of the optimum Z_{MN} (2.9).

4.5 Measurement results

The measurement setup is presented in Fig. 4.6 and Fig. 4.8. The transmitter was accurately set to resonance, and P_S was obtained using a shunt (R_m) resistor and an oscilloscope. The dc power delivered to the load (P_L) was obtained measuring V_L and R_L. The measured total efficiency $\eta_{TOT} = P_L/P_S$, for different $D_{TX\text{-}RX}$ and R_L, is presented in Fig. 4.9 and Fig. 4.10. For all the points, $V_L = 2.6$ V was regulated adjusting V_S (method C, Section 4.3). The theoretical efficiencies, calculated using (2.7) and the measured values of $k_{TX\text{-}RX}$, Q_{TX}, Q_{RX}, η_{RX} and Z_{MN}, are also presented in Fig. 4.9 and Fig. 4.10.

As mentioned before, the feedback control is out of the scope of these chapter. Just in order to quantify the power consumption that this control loop could have, note that in [29] a load modulation signal generator was implemented to control power in closed-loop consuming only 17 μA (76.5 μW). In many systems, a back-telemetry link for communication exists (e.g. AIMDs) which could be used to implement this control loop. Therefore, we can estimate that this control loop will not significantly affect the efficiency of the proof-of-concept system, and the improvements due to the impedance adjustment will not be significantly reduced due to the consumption of the control circuit.

As shown in Fig. 4.9, η_{TOT} is higher for almost all the distances at x1 (bypassing the voltage doubler) where $Re\{Z_{MN}\} = 3.5\ \Omega$ and $\eta_{RX} = \eta_{rect} = 85\%$. When the doubler is on, $Re\{Z_{MN}\} = 9.5\ \Omega$ and $\eta_{RX} = \eta_{rect}.\eta_{dc\text{-}dc} = 85\%.82\% = 70\%$. If either the efficiency η_{TOT} is desired to be higher than 10%, or the transmitted power P_S is limited to around 60 mW, the maximum distance that can be achieved with $R_L = R_{L_{MIN}} = 1200\ \Omega$ is 5.5 cm. Note that this maximum distance is achieved bypassing the voltage doubler (at x1).

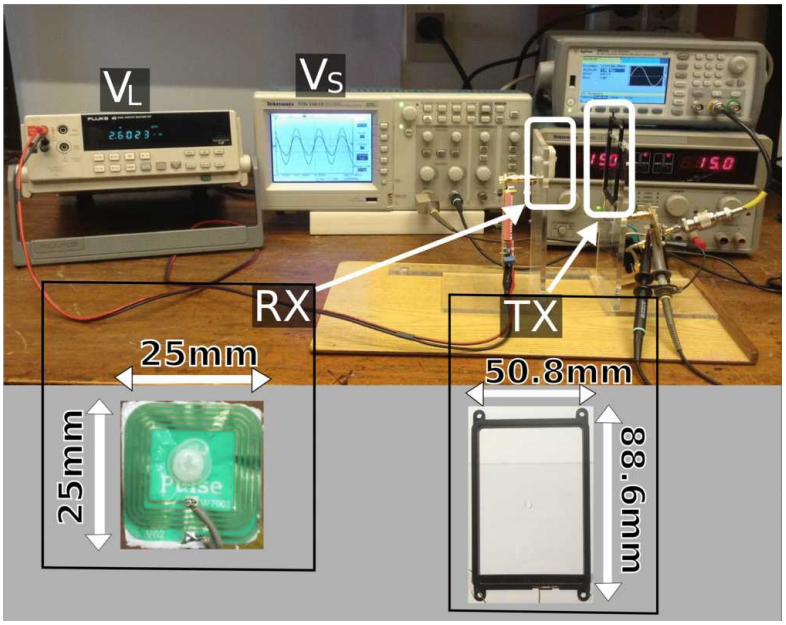


Figure 4.8: Measurement setup.

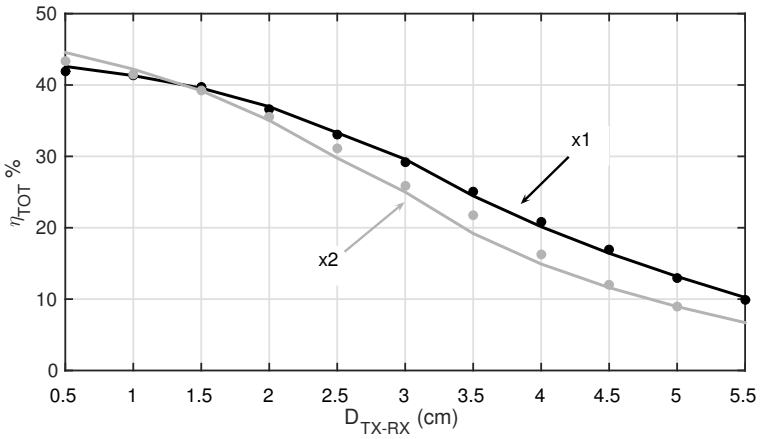


Figure 4.9: Total system efficiency η_{TOT} at $R_L = R_{L_{MIN}} = 1200\ \Omega$ ($P_L = 5.6$ mW). With the dc-dc doubler off (x1) and using the dc-dc doubler (x2). The dots represent measured values and the lines the theoretical model.

The voltage doubler is used to match the load under distances lower than $D_{TX\text{-}RX_{MAX}}$ and $R_L > R_{L_{MIN}}$ as can be seen in Fig. 4.10.

Due to the proposed design flow, the maximum η_{RX} value (85% at x1 dc-dc conversion ratio) is used at large distances, when η_{Link} is minimum, and P_L is high. This corresponds to the cases of $D_{TX\text{-}RX} = 5.5$ cm $R_L = \{1200 - 2000\}\ \Omega$ in Fig. 4.9 and Fig. 4.10. The lowest $\eta_{RX} = 70\%$ (x2) is present for less power demanding loads and lower distances (Fig. 4.10) where η_{Link} is higher. Therefore, the transmission distance was maximized.

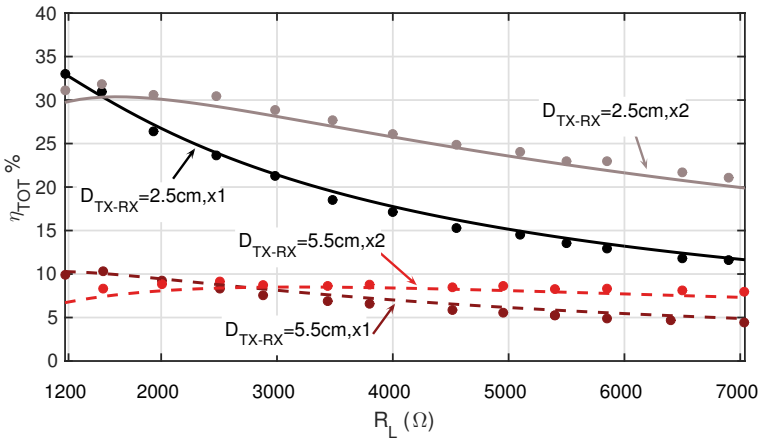


Figure 4.10: Total system efficiency η_{TOT} under the expected R_L changes. $R_L = \{1.2-7\}$ kΩ is equivalent to $P_L \simeq \{1-5.6\}$ mW ($V_L = 2.6$ V is fixed). The dots represent measured values and the lines the theoretical model.

Note that, the MN is designed in step 3 to adapt the input impedance of the ac-dc converter designed in step 2, which does not include an impedance adaption (does not include the dc-dc converter). In order to further validate and compare the proposed design flow, Fig. 4.11 presents the efficiency ($\eta_{TOT\{MN_{\text{x2}}\}\text{x2}}$) obtained when the MN is designed to transform R_{rect} into $R_{MN_{crit}} - jwL_{RX}$ with the voltage doubler on (instead of bypassed, thus without following the design flow described in Section 4.2). Additionally, Fig. 4.11 shows the efficiency obtained following the proposed design flow at x1 $\eta_{TOT\{MN_{\text{x1}}\}\text{x1}}$.

As shown in Fig. 4.11, the inclusion of a voltage doubler does not allow us to increase the maximum transmission distance @$R_{L_{MIN}}$ (critical point), even if the MN is designed to match $Z_{MN_{opt\text{-}\eta}}$ while the voltage doubler is on ($\eta_{TOT\{MN_{\text{x2}}\}\text{x2}}$). This is because η_{RX} is worsened by the inclusion of the dc-dc converter while higher efficiency can be obtained using only an MN.

A typical and straightforward approach for the receiver is to use just a parallel capacitor C_P to achieve resonance (in place of the MN) followed by a circuit that rectifies and may adjust voltage as in Section 3.4.3 and [29,30,109]. This approach was also implemented and measured in this chapter, using only a parallel resonant capacitor followed by the same rectifier and dc-dc converter used in the designed system. The results of this typical design are labeled in Fig. 4.11 as $\eta_{TOT\text{x1}}$ (when no step-up dc-dc is applied) and $\eta_{TOT\text{x2}}$ (when a x2 dc-dc is included). At low distances $\eta_{TOT\text{x1}}$ achieves the highest efficiency, because the $Re\{Z_{MN}\}$ obtained in this particular case is 20 Ω which is closer to $Re\{Z_{MN_{opt}}\}$@$D_{TX\text{-}RX} = 0.5$ cm than in the other presented cases. However, at larger distances, the $Re\{Z_{MN}\}$ is far from the optimum (20 Ω >> 3.5 Ω) decreasing efficiency, while the proposed system presents higher efficiency. Therefore, the proposed design leads to a system that presents 80% higher efficiency, from 9.2% to 16% at 4.5 cm, compared with a system that uses a parallel capacitor resonant structure and a converter to track the maximum efficiency. Figure 4.11 shows that the proposed design achieves

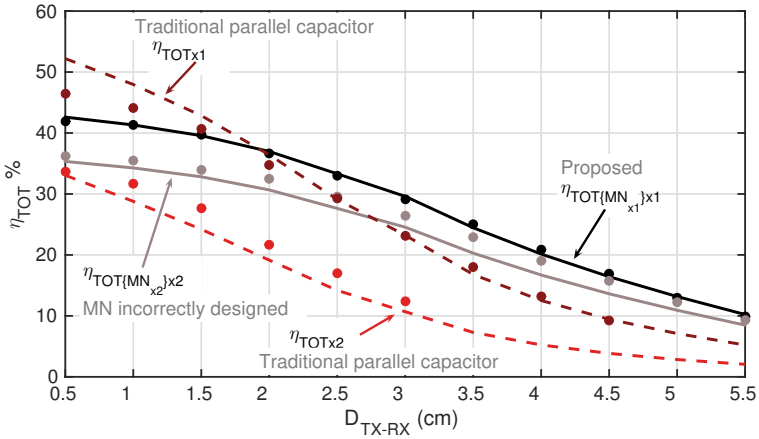


Figure 4.11: Comparison of the proposed designed system with its doubler off $\eta_{TOT\{MN_{x1}\}x1}$, with the following cases: • $\eta_{TOT\{MN_{x2}\}x2}$, doubler on and MN designed to achieve $R_{MN_{crit}}$ in this case (with doubler on) thus without following the proposed design flow. • η_{TOTx1} and • η_{TOTx2} that are traditional approaches, without C_S and setting C_P only to achieve resonance (parallel resonator), without and with doubler respectively. All cases measured at $R_L = R_{L_{MIN}} = 1200\ \Omega$ ($V_L = 2.6$ V, $P_L = 5.6$ mW). The dots represent measured values and the lines the theoretical model.

the highest efficiency at large distances ($D_{TX\text{-}RX} > 2$ cm), thus increasing the maximum transmission distance.

In this system, the performance obtained when a series resonant capacitor is used to achieve resonance is even worse than the one obtained with a parallel capacitor. The $Re\{Z_{MN}\}$ obtained with a series resonator was theoretically calculated and it is 510 Ω. This value is equal to the rectifier input impedance calculated in (4.5), as the series capacitor does not affect the real part of the impedance. This $Re\{Z_{MN}\}$ value, is much higher than the optimum value $Re\{Z_{MN_{opt\text{-}\eta}}\}$ plotted in Fig. 4.7. For this reason, the use of a parallel capacitor, which results in a value of $Re\{Z_{MN}\}$ closer to the optimum value, leads to higher efficiency than a series resonator.

Although the theoretical model fits the measured values, there are some differences, particularly in Fig. 4.11. The following approximations affect the accuracy of the model. As mentioned at the beginning of this chapter, the ac-dc block input impedance was modeled as a resistance, as in [29, 33, 35, 114]. However, the rectifier generates harmonics that are mainly (but not totally) filtered by the resonant receiver. Moreover, the proximity between coils affects their resonant frequency, which was also not considered in the model. Additionally, the rectifier and doubler efficiencies were assumed constant ($\eta_{rect} = 85\%$ and $\eta_{dc\text{-}dc} = 82\%$). This simplified model allows us to analyze and optimize the system, in spite of the small differences noticeable in Fig. 4.11.

So far, we have shown that the proposed design flow is optimum to maximize efficiency and achieve maximum distance for a given set of coils. In this proof-of-concept system, we assume that the maximum distance is limited by a minimum acceptable efficiency at the critical point. Next, we show that without voltage

regulation, the maximum V_L for a fixed V_S and $D_{TX\text{-}RX}$ is also achieved designing the MN as proposed in the design flow (step 3). To do so, V_L was measured in the six conditions depicted in Fig. 4.12, for $V_S = 300$ mV (peak voltage) and $D_{TX\text{-}RX} = 5$ cm (selected as critical point):

- Without a general MN, using only C_P (parallel resonator) to achieve resonance (traditional resonator):
  without doubler (V_{Lx1}), with doubler (V_{Lx2}).

- Designing the MN to achieve (4.2) while the doubler is bypassed (following design flow):
  without doubler ($V_{L\{MN_{x1}\}x1}$), with doubler ($V_{L\{MN_{x1}\}x2}$).

- With the MN designed to achieve (4.2) while the voltage doubler is on (without following design flow):
  without doubler ($V_{L\{MN_{x2}\}x1}$), with doubler ($V_{L\{MN_{x2}\}x2}$).

As V_L, and thus P_L, is maximized in this case, (4.2) was used instead of (2.9) to adjust $Re\{Z_{MN}\}$ in the proposed design. As shown in Fig. 4.12, the maximum V_L is achieved following the guideline described: using an MN designed as we propose without voltage doubler ($V_{L\{MN_{x1}\}x1}$). This is because the maximum V_L is achieved when (4.2) is held with the highest η_{RX}, as discussed in Section 4.1.

It can be seen that if the traditional parallel resonant capacitor is used, and a dc-dc step-up x2 is included with the aim of increasing V_L we obtain just 1.36 V, which is 90% increased (to 2.59 V) by the designed system.

Even though $Re\{Z_{MN}\}$ is closer to $Re\{Z_{MN_{opt}}\}$ in the case of $V_{L\{MN_{x2}\}x2}$, $V_{L\{MN_{x2}\}x1}$ presents a higher voltage due to its better η_{RX}. In the other cases, the doubler, in addition to mismatch $Re\{Z_{MN}\}$, jeopardizes η_{RX} reducing V_L (4.3).

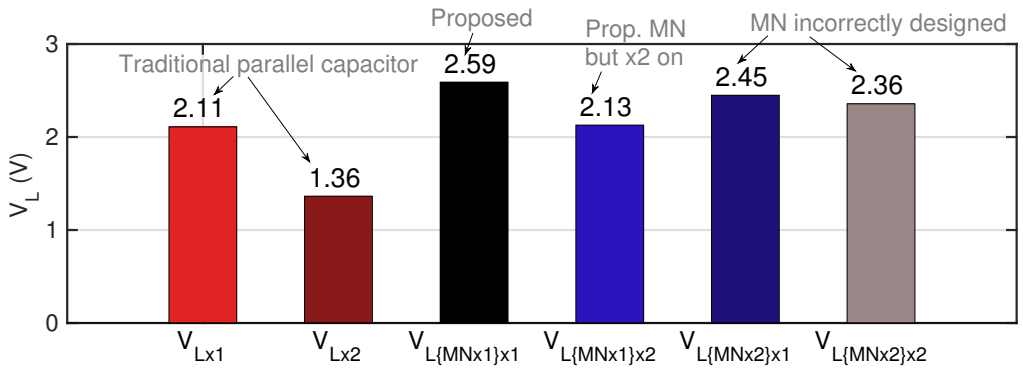


Figure 4.12: Output voltage V_L for different MN and dc-dc gain design criteria, at $V_S = 300$ mV$_p$, $D_{TX\text{-}RX} = 5$ cm and $R_L = 1200\ \Omega$. $V_{L\{MN_{x1}\}x1}$ corresponds to the criterion proposed in this chapter.

4.6 Conclusion of Chapter 4

We proposed a simple design flow to maximize efficiency and distance range of inductive WPT systems using both MNs and adjustable ac-dc converters. This maximum range is achieved by designing the receiver circuit to have its highest efficiency when the link efficiency is the lowest (at large distances). The proposed design uses the MN to match the load impedance at the largest distance (lowest link efficiency) and highest P_L, while the multiple gains of the ac-dc converter adjust the load impedance for lower distances and P_L. Output voltage regulation was studied, as both MN and ac-dc converter influence V_L, showing that the design flow is compatible with V_L regulation.

Additionally, it was proved that the use of a step-up converter is not the most appropriate way to maximize the output voltage in inductive links. We showed that in many typical cases where the MN has higher efficiency than a dc-dc or ac-dc step-up, the maximum output voltage is obtained using only an MN without a step-up converter.

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Chapter 5

Closed-loop analysis: maximum efficiency point tracking and V_L regulation

In the previous chapters, the importance of achieving $Z_{MN_{opt\text{-}\eta}}$ (MEP) was highlighted. It was shown how MNs and ac-dc converters can be used for this purpose. In Section 4.3 it was indicated that changes in the MN or the ac-dc converter gain alter the output voltage (V_L) if the rest of the system is not correspondingly adjusted to maintain a fixed V_L. In this chapter, the discussion of Section 4.3 is extended, analyzing how the MEPT and V_L regulation can be implemented together.

This chapter is organized as follows. First, in Section 5.1 the interaction between the MEPT and the V_L regulation is discussed and the concept of preregulation and postregulation are introduced. The postregulation is further studied in Section 5.2. A theoretical analysis of postregulation is carried out in Section 5.3, and the conclusions of that analysis are presented in Section 5.4. We build and test a proof-of-concept system in Section 5.5 that validates the analysis. Finally, the main conclusions of the chapter are summarized in Section 5.6.

5.1 MEPT vs V_L regulation

In Fig. 5.1, a system-level description is presented indicating different feedback loops that can be used for MEPT and V_L regulation. All the loops of Fig. 5.1 are discussed next.

Many different approaches have been proposed in order to regulate V_L and the received power. In feedback (A) Fig. 5.1, V_L is regulated adjusting the dc-dc gain in the transmitter ($G_{TX_{dc-dc}}$), thus modifying the Thévenin equivalent voltage (V_{TH}) [29, 120]. In (B) the Receiver Matching Network (RX-MN) is modified to detune the receiver, reducing the received power in order to regulate V_L [118]. In (C) the carrier frequency (f) imposed by the inverter (Inv) is used, as it not only detunes the TX but also the RX [119]. Finally, in (D) a fedback dc-dc converter is put just before the load to keep V_L constant [121].

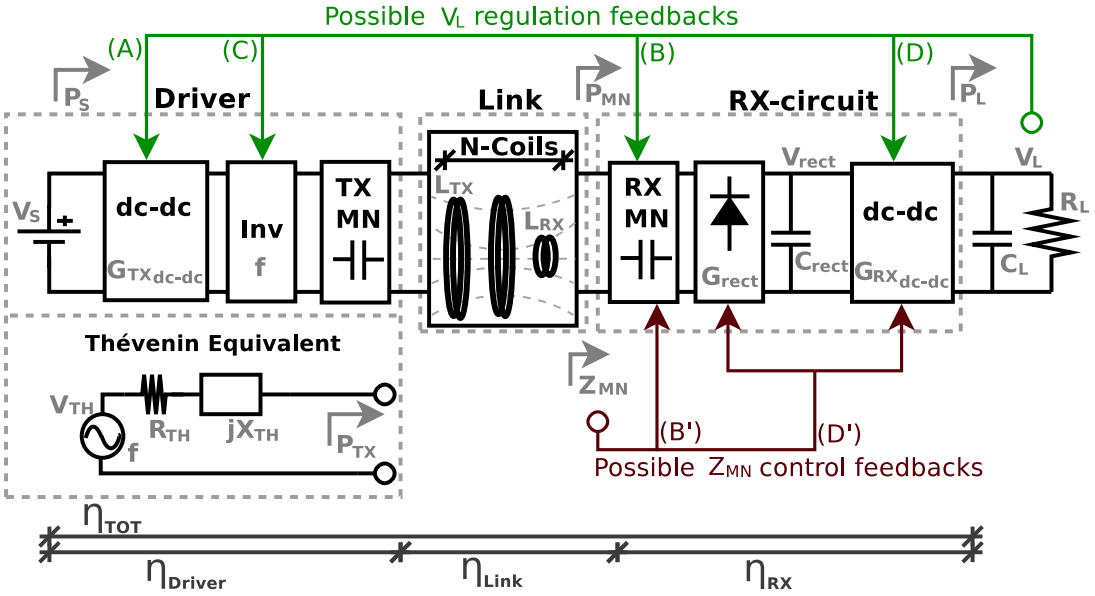


Figure 5.1: System-level description of wireless power transfer system. Acronyms: dc-dc: dc/dc converter, Inv: inverter (dc/ac converter), TX-MN: transmitter matching network, RX-MN: receiver matching network. $G_{TX_{dc-dc}}$, $G_{RX_{dc-dc}}$ and $G_{rect} = (peak\ input\ voltage/dc\ output\ voltage)$ are the transmitter dc-dc, receiver dc-dc and rectifier gains. L_{TX} and L_{RX} are the transmitter and receiver selfinductances respectively. $\eta_{Driver} = P_{TX}/P_S$, $\eta_{Link} = P_{MN}/P_{TX}$ and $\eta_{RX} = P_L/P_{MN}$ are the driver, link and RX-circuit efficiencies respectively. $\eta_{TOT} = P_L/P_S$ is the total efficiency.

On the other hand, different methods exist to achieve and automatically track the MEP $Z_{MN_{opt\text{-}\eta}}$, under coil distance ($k_{TX\text{-}RX}$) and load (R_L) variations [29–31, 42]. Papers like [42] adjust the RX-MN (Feedback B' in Fig. 5.1), while [29, 30] and [31] change the gain of the rectifier (G_{rect}) and dc-dc converter ($G_{RX_{dc-dc}}$) respectively (Feedback D' in Fig. 5.1). The value of $Z_{MN_{opt\text{-}\eta}}$ is needed to implement these feedback loops, a further analysis is addressed in Appendix D.

As can be seen, many of the proposed methods to regulate V_L are incompatible with those proposed to achieve maximum η_{Link}. Basically any change in the RX-circuit for regulating V_L like (B) and (D), also changes Z_{MN}. In addition, changes in f (C) also affect the receiver resonance modifying Z_{MN} and thus the efficiency. In the optimum situation the RX-MN, G_{rect} and $G_{RX_{dc-dc}}$ (RX-circuit) should be the ones that hold $Z_{MN_{opt\text{-}\eta}}$ while V_{TH} (Driver voltage) is the needed to achieve the desired V_L.

The straightforward way to achieve this optimum situation is to set up the RX-circuit in order to hold $Z_{MN_{opt\text{-}\eta}}$ and then control the driver based on the value of V_L to regulate it [29, 122]. If, for instance, the power consumption of the load (P_L) changes, a feedback can adapt the gain (G_{rect} or $G_{RX_{dc-dc}}$) to maintain $Z_{MN_{opt\text{-}\eta}}$. This change in the gain and P_L will affect V_L so another feedback has to control it by adjusting the driver (V_{TH}). Therefore, this method is composed of an (A) feedback to control V_L, and a (B') or (D') one to hold $Z_{MN_{opt\text{-}\eta}}$. This

approach will be referred to as preregulation, Fig. 5.2.

A not so intuitive way to achieve the same optimum situation was proposed in [33, 123]. In this approach, the output voltage is regulated by a (B) or (D) feedback and $Z_{MN_{opt\text{-}\eta}}$ is achieved by changes in the driver (V_{TH}) as explained below. This method will be referred to as postregulation (Fig. 5.2), and have been used in recent works as [33, 114, 121, 124]. It can be noted that changes in the driver alone, were not considered as a means to achieve $Z_{MN} = Z_{MN_{opt\text{-}\eta}}$ (Fig. 5.1) because actually if only V_{TH} is changed neither Z_{MN} nor $Z_{MN_{opt\text{-}\eta}}$ are altered. However, in postregulation, changes in the driver generate changes in the RX-circuit gain. For example, if a (D) feedback is used, $G_{RX_{dc-dc}}$ would change since V_{rect} depends on the driver (V_{TH}) while V_L is kept constant by the (D) feedback. Therefore, the changes in the driver (V_{TH}) are actually generating changes in the RX-circuit modifying Z_{MN}, and thus it can be used to try to achieve $Z_{MN} = Z_{MN_{opt\text{-}\eta}}$. The dynamics of postregulation is more complex to analyze and it is not easy to determine at first glance if the MEP ($Z_{MN} = Z_{MN_{opt\text{-}\eta}}$) can be actually achieved. Indeed, in [114] it was pointed out that in the particular case where a voltage source is used to drive a resonant transmitter in a 2-coil link with a series capacitor in RX-MN as a resonant element, the MEP cannot be achieved if only V_{TH} is adjusted. Additionally, it was proved that the link efficiency is limited in that case to 50% even for ideal coils ($Q \to \infty$), case when theoretically [25] the link efficiency should tend to 100%. Postregulation will be further addressed in Section 5.2.

An extended discussion comparing pre and post regulation can be found in Appendix D.

In this chapter, it is demonstrated that when postregulation is used, the MEP cannot always be achieved and in order to achieve it the following aspects should be appropriately combined: 1) the type of driver used (current or voltage), 2) the resonance or non-resonance of the transmitter, 3) the number of coils used in the link (N) and 4) the resonant structure used in the RX-MN (series or parallel). All the combinations are considered highlighting which ones are able to achieve the MEP and which ones not. These results are summarized in Table 5.5. As far as we know, this is the first time that all these cases are analyzed leading to general considerations regarding the design of these links. The analysis is validated through simulations and measurements of a proof-of-concept system. This proof-of-concept system proves that if the analysis presented here is not taken into account, the maximum possible efficiency of a system cannot always be achieved. Applying this analysis we were able to increase the achievable efficiency of a 3-coil link from 28% to 37.5%, showing the impact of following the analysis proposed here. Considering that the addition of resonant coils has been widely used since it was proposed [36], the results of this work are highly applicable.

5.2 Postregulation analysis

In Fig. 5.2 the feedback loops needed to achieve maximum efficiency and output voltage regulation are represented for the pre and post regulation approaches.

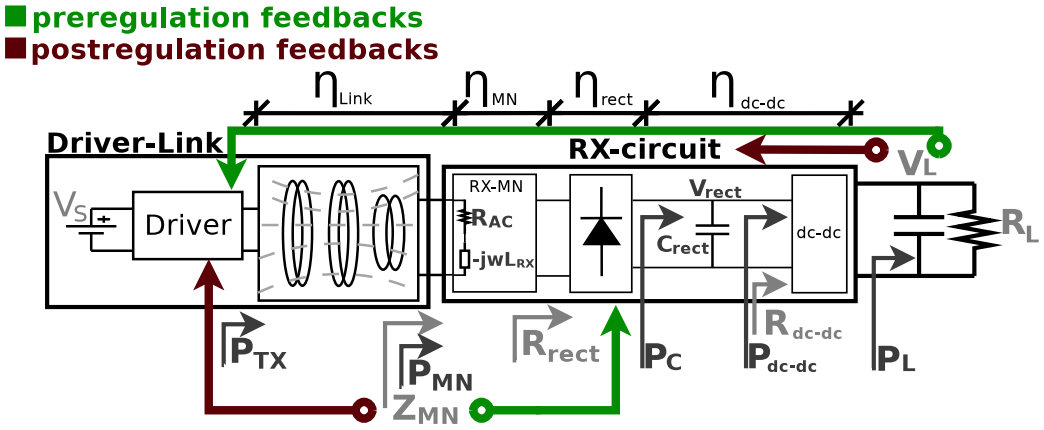


Figure 5.2: Representation of preregulation and postregulation feedbacks.

To simplify the discussion we will assume that the receiver dc-dc converter gain $G_{RX_{dc-dc}}$ is the parameter controlled to keep V_L constant in postregulation (approach D' in Fig. 5.1), and G_{rect} is fixed.

Regardless of the selected approach, if V_L is kept constant, P_L (and thus $P_{dc\text{-}dc}$) is determined by the load and independent of the previous blocks in the system.

However, the power that reaches the output capacitance of the rectifier C_{rect} (P_C), basically depends on all the parameters of the system. This power P_C is affected first by the driver: V_{TH}, R_{TH} and X_{TH} (Fig. 5.1). Second by the link: number of coils (N), coils quality factor Q_i where $i \in [1, N]$ and coupling factor (k_{ij}) where $i, j \in [1, N]$ $i \neq j$. Third, by the RX-MN (η_{MN}) and rectifier (η_{rect}) efficiencies. Finally, P_C also depends on the dc-dc input resistance $R_{dc\text{-}dc}$. This resistance can be estimated as

$$R_{dc\text{-}dc} = {V_{rect}}^2 / P_{dc\text{-}dc}. \tag{5.1}$$

In the steady-state, P_C equals $P_{dc\text{-}dc}$, this steady state condition and all the parameters that affect P_C are presented in (5.2).

$$P_C = f(V_{TH}, R_{TH}, X_{TH}, N, Q_i, k_{ij}, \eta_{MN}.\eta_{rect}, R_{dc\text{-}dc}) = P_{dc\text{-}dc} \tag{5.2}$$

The designer can directly set or determine all the parameters presented in (5.2) except for $R_{dc\text{-}dc}$ that depends on V_{rect} and is affected by the dc-dc feedback loop. In consequence, for a given set of parameters, V_{rect} and thus $R_{dc\text{-}dc}$ should converge to a value that satisfies (5.2). However, this value does not exist for all possible parameter sets. In addition, if a value of $R_{dc\text{-}dc}$ that satisfies (5.2) exists, it has to be a stable equilibrium point. These issues are further discussed in Section 5.3.2.

Once the system has reached a stable equilibrium point, the value of Z_{MN} is set. As was mentioned before, it exists an optimum value for this impedance that maximizes efficiency ($Z_{MN_{opt\text{-}\eta}}$). In order to set $Z_{MN} = Z_{MN_{opt\text{-}\eta}}$, V_{TH} can be modified in (5.2) changing the equilibrium point $R_{dc\text{-}dc}$, and thus Z_{MN} [33, 123]. The existence of that V_{TH} that achieves $Z_{MN} = Z_{MN_{opt\text{-}\eta}}$, is discussed in this chapter.

5.3 Theoretical analysis

The theoretical analysis is organized as follows. First, the method to analyze the operating point is introduced in Section 5.3.1. Section 5.3.2 shows how RX-MN structure (series or parallel) affects the operating point. The results of Section 5.3.2 are then applied in a 2-coil link in Section 5.3.3 where the influence of the type of driver (current or voltage) and the transmitter resonance are introduced. Finally, Section 5.3.4 presents the generalization to N-coil links. The results of this theoretical analysis will be summarized highlighting the conclusions in Section 5.4.

5.3.1 Introduction to the analysis

The link efficiency η_{Link}, and the power that it delivers (P_{MN}, see Fig. 5.2), is directly affected by Z_{MN}. Therefore, in order to analyze the operating point and how it affects efficiency, the steady state condition of (5.2) was rewritten in (5.3) as a function of Z_{MN} (instead of $R_{dc\text{-}dc}$). Note that all the efficiencies and powers presented in (5.3) were defined in Fig. 5.1.

$$\overbrace{\underbrace{f(V_{TH},R_{TH},X_{TH},N,Q_i,k_{ij},Z_{MN})}_{P_{MN}}.\eta_{MN}.\eta_{rect}}^{P_C} = \overbrace{\frac{P_L}{\eta_{dc\text{-}dc}}}^{P_{dc\text{-}dc}} \tag{5.3}$$

To simplify the analysis, we approximate η_{MN}, η_{rect} and $\eta_{dc\text{-}dc}$ by constants. These approximations are needed in order to analyze the system in general and will be valid in the operating range of these blocks.

In Fig. 5.3, the left side of equality (5.3) (P_C) and the right side of it ($P_{dc\text{-}dc}$) are represented as a function of the real part of Z_{MN}, $Re\{Z_{MN}\} = R_{AC}$. We are considering in this discussion that RX-MN was designed to hold resonance ($Im\{Z_{MN}\} = -jwL_{RX}$) and only R_{AC} depends on V_{rect}. This is validated during the following analysis.

As was explained before, P_L is given by the load and does not depend on R_{AC}. Therefore, $P_{dc\text{-}dc} = P_L/\eta_{dc\text{-}dc}$ is represented in Fig. 5.3 as constant.

For any set of parameters, P_C will behave as is represented in Fig. 5.3, with a maximum value at R_{opt-P}. This behavior corresponds to the well known maximum power transfer theorem, where a maximum occurs when $Z_{MN} = R_{opt-P} - jwL_{RX}$ is the conjugated of the Driver-Link output impedance.

If V_{rect} is set to a value for which the R_{AC} does not satisfy (5.3), the power that reaches C_{rect} (P_C) will be different from the one consumed ($P_{dc\text{-}dc}$). Therefore V_{rect} (and thus R_{AC}) will move to a point that does satisfy (5.3). The stability of the points that satisfy (5.3) under a perturbation in V_{rect} is addressed later in this section.

As can be seen from Fig. 5.3, if P_L is too high ($P_L > P_{C_{MAX}}.\eta_{dc\text{-}dc}$), there will be no R_{AC} that satisfies (5.3). If $P_L < P_{C_{MAX}}\eta_{dc\text{-}dc}$ two values of R_{AC} that satisfy (5.3) exist, R_{AC_L} and R_{AC_R}. One of these values is stable while the other is unstable as will be shown.

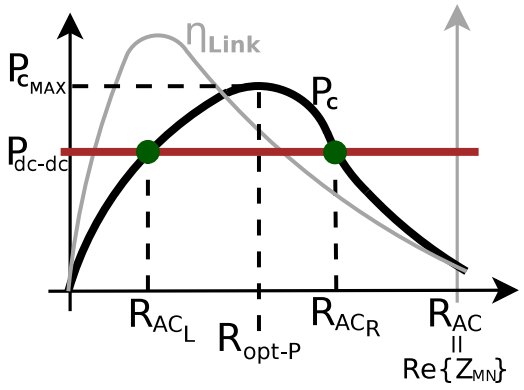


Figure 5.3: Introduction to the graph used to analyze the operating point and it dependence with the system parameters.

The graph of Fig. 5.3 is used in the remaining of the chapter. In Section 5.3.2, it is shown how the RX-MN modify which is the stable point R_{AC_L} or R_{AC_R}. Then in Section 5.3.3 we analyze the influence of the TX driver (current or voltage) and the TX resonance in the P_C curve. Finally, in Section 5.3.4 we show how both curves, P_C and η_{Link} are affected by the addition of resonant coils.

5.3.2 Influence of RX-MN in the operating point

The stability of the operation point is deduced analyzing the perturbation response. Four cases can be analyzed: perturbation from R_{AC_L} or R_{AC_R} each one with a parallel or series resonator in the RX-MN. First, in Table 5.1 we present analytical expressions for the input impedance of series RX-MN (5.4), parallel RX-MN (5.5) and rectifier (5.6) that are used in the analysis.

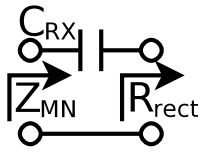
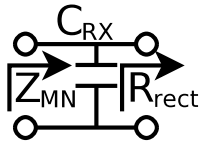
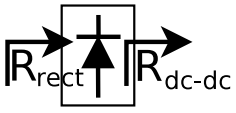
In (5.7) the system response to a perturbation in V_{rect} is analyzed for the case of $R_{AC} = R_{AC_L}$ (see Fig. 5.4) with a parallel resonator. Note that in each step the number of the equation or figure used is indicated. The up arrow (↑) and down arrow (↓) indicate an increase or decrease in the variable value respectively. The analysis of (5.7) shows that $R_{AC} = R_{AC_L}$ with a parallel resonator is stable.

The case for R_{AC_R} with parallel resonator is not presented but can be deduced from (5.7) noting that the only different step is the one that depends on Fig. 5.4. In this case, a decrease in R_{AC} (from R_{AC_R}) will generate that $P_C > P_{dc\text{-}dc}$ thus increasing V_{rect}. Therefore, R_{AC_R} results being unstable when using a parallel resonator.

The series resonator is analyzed in (5.8) for the case of R_{AC_R}. As can be seen from (5.4) and (5.5), the relationship between R_{AC} and R_{rect} is direct for (5.4) and inverse for (5.5). This difference between series and parallel resonator generates that the point (R_{AC_L} or R_{AC_R}) that was stable in parallel resonator, becomes unstable with a series resonator and vice versa. Therefore, the R_{AC_R} that was shown to be unstable with parallel resonator, is stable with series resonator (5.8).

The unstable case of R_{AC_L} with series resonator is not presented but it can

Table 5.1: Impedance transformation.

	Series RX-MN: $Z_{MN} = \overbrace{R_{rect}}^{Re\{Z_{MN}\}=R_{AC}} + \frac{1}{jwC_{RX}}$ (5.4)
	Parallel RX-MN: (if $R_{rect}/(wL_{RX})^2 >> 1$, $wL_{RX} = 1/wC_{RX}$) $Z_{MN} = \overbrace{\frac{(wL_{RX})^2}{R_{rect}}}^{Re\{Z_{MN}\}=R_{AC}} + \frac{1}{jwC_{RX}}$ (5.5)
	Rectifier: $R_{rect} \simeq \frac{\eta_{rect} R_{dc\text{-}dc}{}^1}{2}$ (5.6)

NOTE 1- Obtained form $P_{rect}.\eta_{rect} = P_C$, neglecting parasitics capacitances and diode threshold voltage.

be deduced from (5.8) noting that in this case when $R_{AC} \uparrow$ (from R_{AC_L}) $\Rightarrow P_C > P_{dc\text{-}dc}$ (Fig. 5.4), inverting the final result.

It should be mentioned that if a more complex RX-MN is used, as previously done in the thesis, this analysis is not altered. The same deduction made in (5.7) and (5.8) can be remade using the impedance transformation of the particular MN. The stable and unstable points are the same as in the series resonator (5.4) if the relationship between R_{rect} and R_{AC} is direct, and they are the same as in the parallel resonator (5.5) if the relationship between R_{rect} and R_{AC} is inverse.

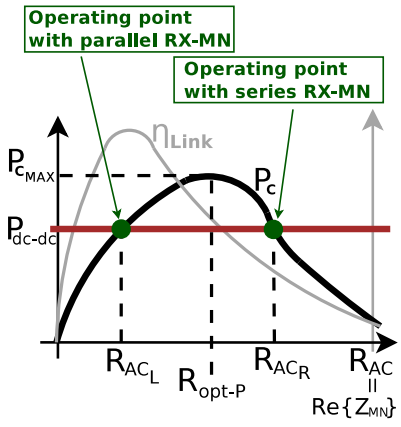


Figure 5.4: Operating point (5.3) representation. $R_{AC} = Re\{Z_{MN}\}$.

R_{AC_L} with parallel resonator

$$V_{rect} \uparrow \overset{(5.1)}{\Longrightarrow} R_{dc\text{-}dc} \uparrow \overset{(5.6)}{\Longrightarrow}$$
$$R_{rect} \uparrow \overset{(5.5)}{\Longrightarrow} R_{AC} \downarrow \overset{Fig.\ 5.4}{\Longrightarrow} \quad (5.7)$$
$$P_C < P_{dc\text{-}dc} \overset{Fig.\ 5.2}{\Longrightarrow} V_{rect} \downarrow$$

R_{AC_R} with series resonator

$$V_{rect} \uparrow \overset{(5.1)}{\Longrightarrow} R_{dc\text{-}dc} \uparrow \overset{(5.6)}{\Longrightarrow}$$
$$R_{rect} \uparrow \overset{(5.4)}{\Longrightarrow} R_{AC} \uparrow \overset{Fig.\ 5.4}{\Longrightarrow} \quad (5.8)$$
$$P_C < P_{dc\text{-}dc} \overset{Fig.\ 5.2}{\Longrightarrow} V_{rect} \downarrow$$

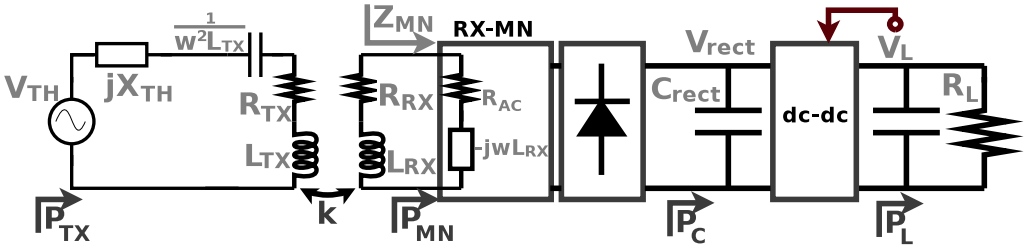


Figure 5.5: Schematic circuit for a 2-coil link with postregulation.

In [114] the existence of this stable and unstable points was analyzed in the particular case of series resonator (series RX-MN), 2-coil link, and using a voltage source to drive the transmitter. As far as we know, the dependency of this stable point with the resonant structure used in the receiver has not been analyzed before. Additionally, in this chapter, we also consider the number of coils (N), the type of driver used, and the transmitter resonance.

5.3.3 Influence of RX-MN, type of driver and transmitter resonance in a 2-coil link

The influence of transmitter resonance and driver are introduced using a 2-coil link. Analytical expressions for the main points in Fig. 5.3 are presented and evaluated for different proof-of-concept systems.

The circuit schematic is presented in Fig. 5.5. In the equations presented here, we are assuming that the receiver coil is always resonating ($Im\{Z_{MN}\} = -jwL_{RX}$) since this maximizes the link efficiency ($\eta_{Link} = P_{MN}/P_{TX}$) [25]. However, a resultant imaginary part is considered in the transmitter (jX_{TH}), since it does not jeopardize the link efficiency and its value does affect the operating point as will be shown. In order to simplify the discussion, in Fig. 5.5 the series resonant capacitor in the transmitter is assumed to be canceling the coil impedance (jwL_{TX}) thus jX_{TH} is the resultant imaginary impedance. However, this resultant imaginary part can be generated by detuning the transmitter or using a general MN as it is used in the receiver. The output resistance of the driver (R_{TH}) can be included as part of the coil parasitic resistance to simplify the equations.

The link efficiency was calculated in (2.7).

$$\eta_{Link} = \frac{P_{MN}}{P_{TX}} = \frac{Q_{RX\text{-}L}}{Q_L} \frac{{k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L}}{{k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L} + 1} \tag{2.7}$$

The power that reaches the C_{rect} (P_C) is presented in (5.13), and the value of R_{AC} that maximizes it (R_{opt-P}) in (5.10). Note that P_C and R_{opt-P} do depend on X_{TH}.

$$P_C = \frac{Q_{RX\text{-}L}}{Q_L} \frac{\eta_{MN}\eta_{rect} R_{TX} {k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L}}{(R_{TX}(1 + {k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L}))^2 + X_{TH}^2} \frac{V_{TH}^2}{2} \tag{5.13}$$

Table 5.2: 2-coil R_{AC} different optimum values, highlighted in Fig. 5.6.

$$Re\{Z_{MN_{opt\text{-}\eta}}\} = R_{opt-\eta} = R_{RX}\sqrt{1 + {k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX}} \quad (5.9)$$
$$R_{opt-P} = R_{RX}\sqrt{\frac{(1 + {k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX})^2 + (X_{TH}/R_{TX})^2}{(X_{TH}/R_{TX})^2 + 1}} \quad (5.10)$$
$$R_{opt-P}\vert_{@X_{TH}=0} = R_{opt-P_{vTXres}} = R_{RX}(1 + {k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX}) \quad (5.11)$$
$$R_{opt-P}\vert_{@X_{TH}\to\infty} = R_{opt-P_i} = R_{RX} \quad (5.12)$$

This optimum value of R_{opt-P} for the particular case of a resonant transmitter ($X_{TH} = 0$) is given in (5.11). If a current source is used to drive the same series resonant transmitter, the power that reaches C_{rect} in that case (P_{C-i}) is given in (5.14), and it is maximized for $R_{AC} = R_{opt-P_i}$ (5.12). This current source case is equivalent to consider a voltage source with an extremely large X_{TH} which corresponds to the Thévenin model of the current source driver. Thus, the limit of R_{opt-P} with X_{TH} as X_{TH} tends to infinite equals R_{opt-P_i}. As can be seen, P_C depends on the type of driver used and the transmitter resonance.

$$P_{C-i} = \frac{Q_{RX\text{-}L}}{Q_L}\eta_{MN}\eta_{rect}{k_{TX\text{-}RX}}^2 Q_{TX} Q_{RX\text{-}L}\frac{I_T^2 R_{TX}}{2} \quad (5.14)$$

The total system efficiency $\eta_{TOT} = \eta_{driver}\eta_{Link}\eta_{MN}\eta_{rect}\eta_{dc\text{-}dc}$ and P_C were evaluated as a function of R_{AC} using the values of the proof-of-concept system presented in Table 5.3. Six different cases are considered. In cases I and II a current driver is used in a series resonant transmitter with parallel and series RX-MN respectively. III and IV consider the cases of a voltage driver and a series resonant transmitter also with parallel and series RX-MN respectively. The non-resonant transmitter is considered in V for parallel RX-MN and in VI for series RX-MN.

The results are presented in Fig. 5.6 where η_{Link} was obtained from (2.7), P_C from (5.13) (Table 5.3 with $X_{TH} = 0.8\ \Omega$ cases V and VI), P_{C-res} from (5.13) with $X_{TH} = 0$ (cases III and IV) and P_{C-i} from (5.14) (cases I and II). The output power $P_L = 50$ mW is also presented. As was explained before, each case has one stable operating point that is highlighted in Fig. 5.6. Although six different cases are considered and are presented in Table 5.3, η_{Link} as a function of R_{AC} is the same for all cases since the expression (2.7) is not altered by the parameters changed between the cases analyzed. Three different cases of P_C exist as (5.13) depends on X_{TH}.

Table 5.3: 2-coil proof-of-concept cases.

Case	Components values
All	$L_{TX} = 1.18\ \mu$H ; $Q_{TX} = 146.5$ (Pulse Elec. W7002)
All	$L_{RX} = 877$ nH ; $Q_{RX} = 34.1$ (Pulse Elec. W7001)
All	$k = 0.08$ ($D = 1$ cm) ; $f = 13.56$ MHz ; $P_L = 50$ mW
All	$\eta_{driver} \simeq 90\%$; $\eta_{rect} \simeq 90\%$; $\eta_{dc\text{-}dc} \simeq 75\%$
I	$I_T = 190$ mA ; Parallel RX-MN (5.5)
II	$I_T = 190$ mA ; Series RX-MN (5.4)
III	$V_{TH} = 750$ mV ; $X_{TH} = 0\ \Omega$; Parallel RX-MN (5.5)
IV	$V_{TH} = 750$ mV ; $X_{TH} = 0\ \Omega$; Series RX-MN (5.4)
V	$V_{TH} = 750$ mV ; $X_{TH} = 0.8\ \Omega$; Parallel RX-MN (5.5)
VI	$V_{TH} = 750$ mV ; $X_{TH} = 0.8\ \Omega$; Series RX-MN (5.4)

V_{TH} and I_T are peak values. $\eta_{MN} \simeq 100\%$

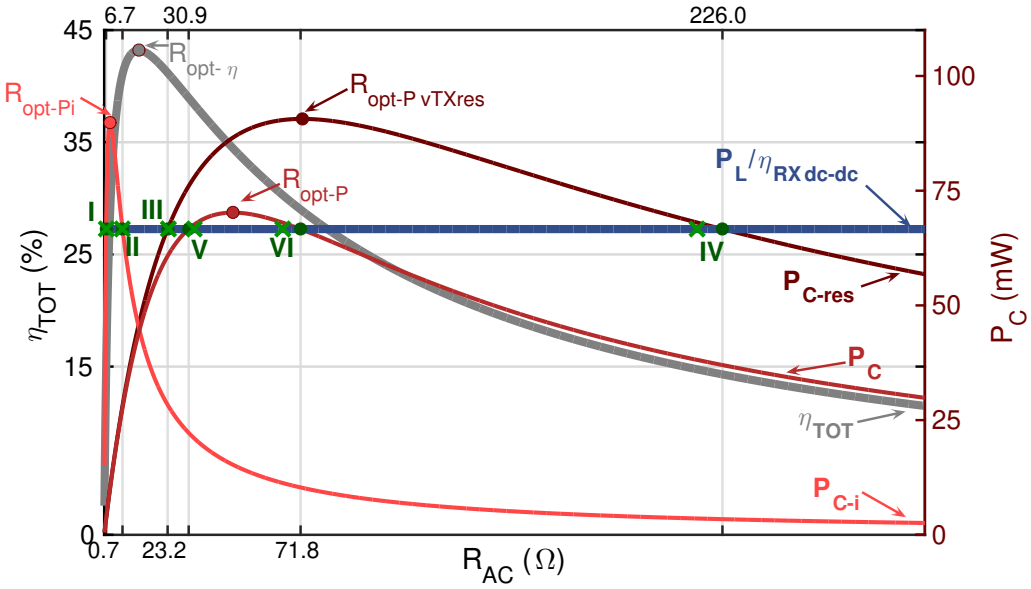


Figure 5.6: 2-coil operating point analysis. P_L is the power delivered to the load, P_{C-res} and P_C are the power that reaches C_{rect} using a voltage driver with a resonant and non-resonant transmitter respectively, and P_{C-i} is the power that reaches C_{rect} if a current source driver is used in the transmitters. These plots were generated using the proof-of-concept values presented in Table 5.3. The cross-marks are Spice simulations of each case.

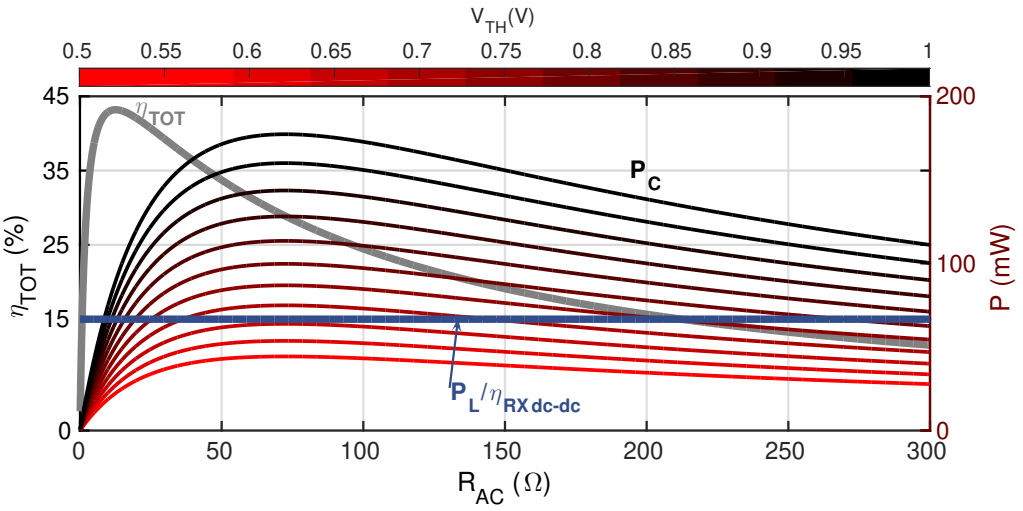


Figure 5.7: Changes in P_C under V_{TH} modifications at $X_{TH} = 0$.

In order to show how the operating point can be modified adjusting V_{TH}, Fig. 5.7 presents P_C under a sweep in V_{TH} for the case of $X_{TH} = 0$ (P_{C-res} of Fig. 5.6). With a series RX-MN, as the stable point is the one on the right of R_{opt-P} (R_{AC_R} Fig. 5.4), from Fig. 5.7 we can see that changing V_{TH} the stable R_{AC} varies between R_{opt-P} and infinity (theoretically). An analogous deduction can be done for a parallel RX-MN. This is summarized in (5.15).

$$\begin{aligned} &R_{AC} \text{ range under } V_{TH} \text{ variations:} \\ &\text{With series RX-MN } \Rightarrow [R_{opt-P}, \infty] \\ &\text{With parallel RX-MN } \Rightarrow [0, R_{opt-P}] \end{aligned} \tag{5.15}$$

The behavior of P_C under V_{TH} variations presented in Fig. 5.7 is actually independent of the number of coils and X_{TH}, as is further discussed in Section 5.3.4. Therefore, (5.15) is valid for any X_{TH} and number of coils.

Although Fig. 5.6 and Fig. 5.7 were generated using values from the proof-of-concept cases, from (5.9), (5.10), (5.11) and (5.12), it can be proved that for any set of parameters, $R_{opt-P_i} < R_{opt-P} < R_{opt-P_{vTXres}}$ and

$$\text{In 2-coil link:} \quad \underbrace{R_{opt-P_i}}_{R_{opt-P}|_{@X_{TH}\to\infty}} < R_{opt-\eta} < \underbrace{R_{opt-P_{vTXres}}}_{R_{opt-P}|_{@X_{TH}=0}} . \tag{5.16}$$

Thus, some general conclusion can be drawn as follow. In the case IV, where it was used a series RX-MN and a voltage resonant transmitter ($X_{TH} = 0$ thus $R_{opt-P}|_{@X_{TH}=0} = R_{opt-P_{vTXres}}$), from (5.15) it can be deduced that $R_{AC} \in [R_{opt-P_{vTXres}}, \infty]$. Then using (5.16) it is proved that the range obtained of R_{AC} does not include $R_{opt-\eta}$. Therefore, V_{TH} cannot be used to achieve the MEP in case IV. This discussion can be graphically seen in Fig. 5.6, observing that

the stable point of case IV is at the right of $R_{opt-P_{vTXres}}$ and thus will not reach $R_{opt-\eta}$ under changes in V_{TH}. However, in case III which uses a parallel resonator, $R_{AC} \in [0, R_{opt-P_{vTXres}}]$ thus it includes $R_{opt-\eta}$.

A similar deduction that the one made for case IV can be done to the case I where a current source and a parallel resonator was used. In that case, $R_{AC} \in [0, R_{opt-Pi}]$ which does not include $R_{opt-\eta}$ (5.16) concluding that in case I MEP cannot be achieved only modifying V_{TH}.

The six cases presented in Table 5.3 were also simulated using Spice. In the simulation, a rectifier with ideal diodes ($V_\gamma \cong 0$) and an ideal dc-dc converter were used. The power load was set to $P_L/(\eta_{MN}\eta_{rect}.\eta_{dc\text{-}dc})$ to include these losses. The dc-dc converter was turned on after V_{rect} has been stabilized, to allow start-up. The simulated R_{AC} for each case is presented in Fig. 5.6 with a cross-mark. These simulations validate the analytical expressions and analysis. The slight differences between the simulated and theoretically expected values are mainly due to the following approximation. All the analysis presented here is assuming that the RX-circuit has a linear input impedance and does not introduce harmonic distortion (first harmonic approximation). However, the rectifier generates harmonics that are mainly (but not totally) filtered by the resonant receiver.

It should be noted that the input voltage of the dc-dc regulator (V_{rect}) at the stable point could be in some cases impractical. For example, from the simulations, it can be seen that in the case of I $V_{rect} = 33.4\ V$ while in the case II $V_{rect} = 780\ mV$. This has to be considered to properly select the working case and the dc-dc regulator.

In Appendix E, the same analysis of this section is carried out for a 3-coil link. In the next section, a generalization for an N-coil link is presented.

5.3.4 Generalization to N-coil link

As was mentioned and will be further shown in Section 5.4, the relative position of $R_{opt-\eta}$, $R_{opt-P_{vTXres}}$ and R_{opt-P_i} is important when tracking the MEP. In this section, this relative position is studied in general for an N-coil link.

The power that reaches C_{rect} (P_C) can be calculated as the product of P_{TX}, η_{Link}, η_{MN} and η_{rect} (Fig. 5.2). Thus, the relative position between the maximums of P_C (R_{opt-P}) and η_{Link} ($R_{opt-\eta}$), is affected by the dependency of P_{TX} with R_{AC}. In what follows, P_{TX} as a function of R_{AC} is analyzed to conclude then how it affects R_{opt-P}.

In Fig. 5.8 the simplified schematic for an N-coil link using RLT is presented. Using the RLT, P_{TX} can be expressed as a function of R_{ref_1} which is the reflected resistance in the transmitter (5.17). The values of the reflected resistance in each coil (R_{ref_i}) is given in (5.18).

$$P_{TX} = \frac{V_{TH}^2}{2} \frac{(R_{TX} + R_{ref_1})}{X_{TH}^2 + (R_{TX} + R_{ref_1})^2} \tag{5.17}$$

$$R_{ref_i} = \frac{w^2 k_{i,i+1} L_i L_{i+1}}{R_{i+1} + R_{ref_{i+1}}} \tag{5.18}$$

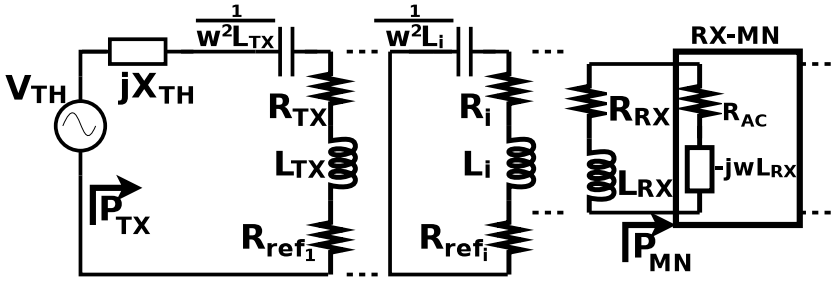


Figure 5.8: Simplified schematic using Reflected Load Theory (RLT), for an N-coil link.

From (5.17), the value of R_{ref_1} that maximizes the power delivered by the driver, P_{TX}, is $R_{ref_1} = X_{TH} - R_{TX}$ (if $R_{TX} < X_{TH}$), Fig. 5.9.

The reflected resistance is inversely proportional to the total resultant resistance in the consecutive coil (5.18). Thus, each extra coil inverts the relationship between R_{AC} and R_{ref_1}. In a link with an even number of coils, R_{ref_1} as a function of R_{AC} is monotonically decreasing while in a link with an odd number of coils, it is monotonically increasing. Using this result, Fig. 5.9 can be redone changing the horizontal axis from R_{ref_1} to R_{AC} as is presented in Fig. 5.10. The R_{AC} that maximizes P_{TX}, $R_{opt-P_{TX}}$, and its dependence with X_{TH} are represented in Fig. 5.10. For instance, an increase in X_{TH} ($X_{TH} \uparrow$) moves the maximum of P_{TX} to the right in the case of an odd number of coils and to the left in the case of an even number of coils. When $X_{TH} < R_{TX}$, P_{TX} has no relative maximum value ($\partial P_{TX}/\partial R_{AC} \neq 0 \ \forall \ R_{AC} > 0$ and $\forall \ N$) and it is a monotonically increasing function if N is even and monotonically decreasing function if N is odd.

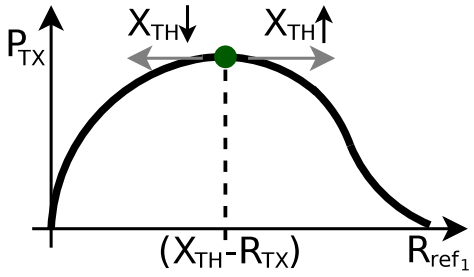


Figure 5.9: Power delivered by the driver (P_{TX}) as a function of the reflected resistance in the transmitter (R_{ref_1}).

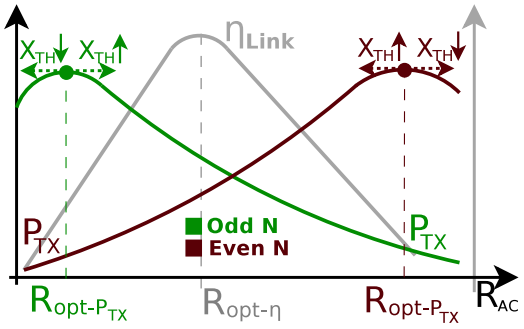


Figure 5.10: P_{TX} and η_{Link} as a function of R_{AC}.

Since P_{TX} is always positive with no relative minimum values for any X_{TH}, it can be proved that the R_{AC} that maximizes the product ($P_C = P_{TX}\eta_{Link}\eta_{MN}\eta_{rect}$), R_{opt-P}, fulfills the following properties: $R_{opt-P} < R_{opt-\eta}$ if $R_{opt-P_{TX}} < R_{opt-\eta}$ and $R_{opt-P} > R_{opt-\eta}$ if $R_{opt-P_{TX}} > R_{opt-\eta}$. Using this property, and the previous discussion of how X_{TH} affects $R_{opt-P_{TX}}$, Table 5.4 can be deduced.

Therefore, in this section (5.16) was generalized to an N-coil link in Table 5.4. This result will be used in Section 5.4.

Table 5.4: Summary of relative positions of maximums.

Case	Relative positions of maximums
N even	$\overbrace{R_{opt-P_i}}^{R_{opt-P}\|@X_{TH}\to\infty} < R_{opt-\eta} < \overbrace{R_{opt-P_{vTXres}}}^{R_{opt-P}\|@X_{TH}=0}$
N odd	$\overbrace{R_{opt-P_{vTXres}}}^{R_{opt-P}\|@X_{TH}=0} < R_{opt-\eta} < \overbrace{R_{opt-P_i}}^{R_{opt-P}\|@X_{TH}\to\infty}$

Table 5.5: Summary of different cases studied indicating whether MEPT is possible by adjusting the driver amplitude.

	Driver Type	N (number of coils)	RX-MN	MEPT possible?
i	Current ($X_{TH} \to \infty$)	Even	Parallel	NO
ii	Current ($X_{TH} \to \infty$)	Even	Series	YES
iii	Voltage ($X_{TH} = 0$)	Even	Parallel	YES
iv	Voltage ($X_{TH} = 0$)	Even	Series	NO
v	Current ($X_{TH} \to \infty$)	Odd	Parallel	YES
vi	Current ($X_{TH} \to \infty$)	Odd	Series	NO
vii	Voltage ($X_{TH} = 0$)	Odd	Parallel	NO
viii	Voltage ($X_{TH} = 0$)	Odd	Series	YES

5.4 MEP Attainability

In this section the main results obtained in the theoretical analysis Section 5.3 are highlighted and used to finally summarize in which cases the MEP can be achieved and in which ones not.

The two main results from Section 5.3 are the following. First, (5.15) where the achievable R_{AC} range under V_{TH} variations is shown. As can be seen, this range is limited by the R_{AC} that maximizes P_C (R_{opt-P}). Second, Table 5.4, where the position of the R_{AC} that maximizes efficiency ($R_{opt-\eta}$) with respect to R_{opt-P} was summarized. Finally, from (5.15) and Table 5.4 it can be determined in which situations the achievable R_{AC} range under V_{TH} variations includes $R_{opt-\eta}$. In those cases where $R_{opt-\eta}$ is included in the R_{AC} range, MEPT is possible while in the others not. This is summarized in Table 5.5.

Note that for a link with a given number of coils and resonant structure (RX-MN), MEP can always be achieved if the driver type is correctly chosen. Changing between current or voltage driver is equivalent to tune or detune enough the transmitter. In the latter case, the effect of the driver efficiency when its load is detuned should be considered.

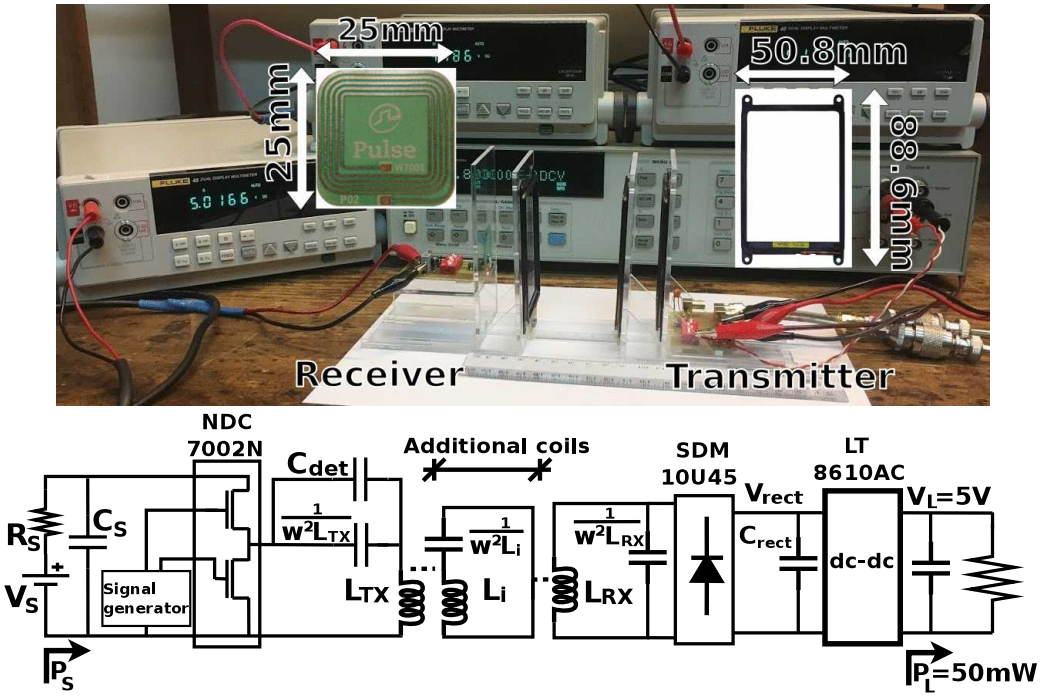


Figure 5.11: Measurement setup and schematic.

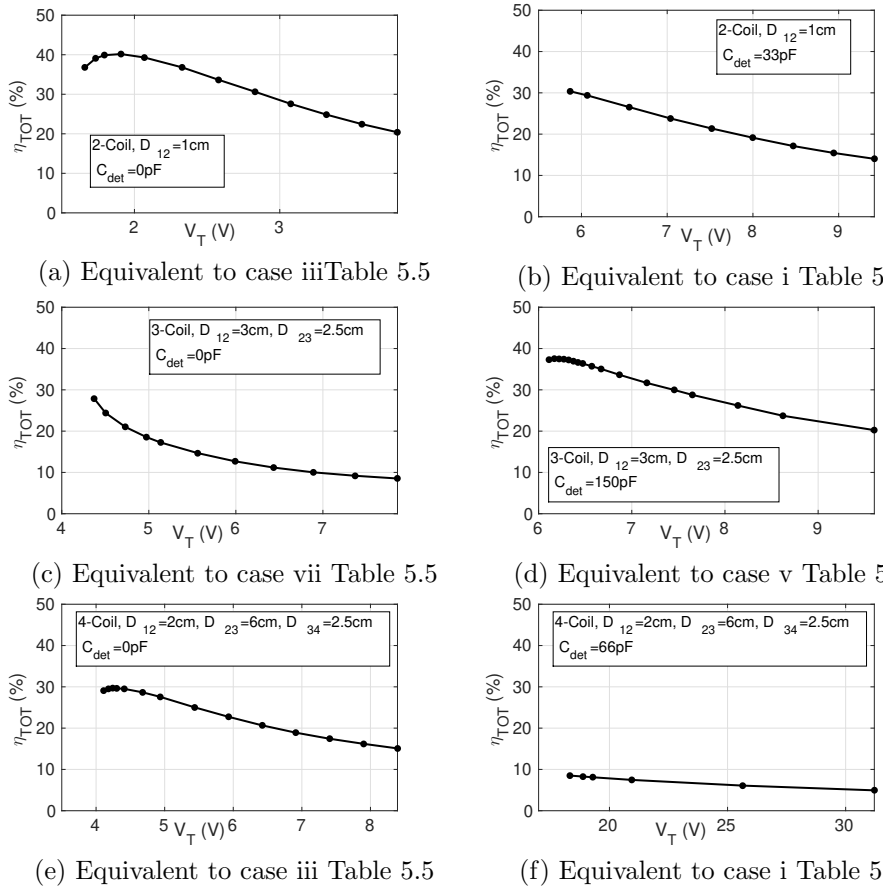
5.5 Measurement results

In this section, some of the cases presented in Table 5.5 are validated through measurements. The system used is presented in Fig. 5.11. It operates at 13.56 MHz and is intended to power a 50 mW load.

The transmitter voltage V_S was swept in order to reach the MEP. Six different cases were measured, tuning and detuning the transmitter in links with 2-, 3- and 4-coil. In all the cases a parallel capacitor in the receiver RX-MN was used. The same coil (Pulse 7002) was used for the transmitter and the additional coils, see Fig. 5.11. The receiver coil was implemented using the Pulse 7001, see Fig. 5.11. The total efficiency η_{TOT} as a function of V_S for the six cases measured are presented in Fig. 5.12. The power P_S was measured using a shunt resistor (R_S) shown in Fig. 5.11. The total system efficiency was calculated as $\eta_{TOT} = ({V_L}^2/R_L)/P_S$.

Each plot in Fig. 5.12 indicates the number of coils used in the link, the distances between coils, and the value of C_{det} used to detune the transmitter (Fig. 5.11). A $C_{det} = 0$pF means that the transmitter is in resonance. Additionally, the corresponding case of Table 5.5 is indicated in the caption.

The value of C_{det} was selected to generate an X_{TH} high enough to change the relative position of $R_{opt-\eta}$ and R_{opt-P} as was discussed in Section 5.3.4. For instance, in the case of a 2-coil link, $C_{det} = 33$ pF generates an $X_{TH} \simeq 22\ \Omega$. Evaluating (5.9) and (5.10) it is deduced that $R_{opt-P}|_{@X_{TH}=22} < R_{opt-\eta} < R_{opt-P}|_{@X_{TH}=0}$. Therefore, the relative position of R_{opt-P} and $R_{opt-\eta}$ was changed by the inclusion of C_{det}. The same change could be achieved by changing the driver from voltage to current mode as was discussed in Section 5.3.3.



(a) Equivalent to case iiiTable 5.5

(b) Equivalent to case i Table 5.5

(c) Equivalent to case vii Table 5.5

(d) Equivalent to case v Table 5.5

(e) Equivalent to case iii Table 5.5

(f) Equivalent to case i Table 5.5

Figure 5.12: Measured efficiency. Dij is the distance between coils i and j.

In all the cases, V_S was decreased until the receiver dc-dc converter stopped working. The dc-dc converter can stop working for two reasons: 1) The V_{rect} is out of the tolerated range of the dc-dc converter, 2) V_S is too low so P_C does not cross $P_L/\eta_{dc\text{-}dc}$ (see Fig. 5.7) and thus does not exist a possible operating point. The first reason can be solved just by selecting another regulator. The value of V_{rect} was measured and it was verified that V_{rect} was always in the range tolerated by the dc-dc converter and it was not limiting the experiment. In consequence, the minimum V_S in the sweep was, in all the cases, due to the second reason.

It can be seen in Fig. 5.12 that in the cases where MEPT is possible, a maximum appears. In the cases of 2-coil and 4-coil, the maximum efficiency achieved is higher when the transmitter is resonating since in these cases MEPT is possible. However, in the case of a 3-coil link, MEPT is possible with the transmitter detuned. As can be seen in Fig. 5.12c and Fig. 5.12d, by detuning the transmitter in the 3-coil link, MEPT was possible and the efficiency achieved increases from 28% to 37.5%.

5.6 Conclusion of Chapter 5

In this chapter, the advantages of postregulation as a method to control the output voltage of WPT systems were highlighted and the tracking of the MEP in this context was studied. Design guidelines were provided to assure that the MEP can be achieved. These guidelines address the driver structure, transmitter resonance and resonant structure in the receiver for any number of coils. Following these guidelines, non-obvious optimal designs can be found, such as the experimentally shown case of a 3-coil link where the MEP is achieved when the transmitter operates out of resonance. In this case, the efficiency was increased from 28% to 37.5% at a transfer distance of 5.5 cm while delivering 50 mW to the load, which is a suitable value for low power wireless devices.

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Chapter 6

Conclusion

This thesis analyzed IPT systems proposing novel architectures and design procedures to increase the efficiency and the distance range. We made contributions in the inductive link analysis (Chapter 2), integrated circuit design (Chapter 3) and system-level design (Chapter 4 and Chapter 5). Specific conclusions of each analysis where presented at the end of the corresponding section. In this chapter the main conclusions of the thesis are summarized.

We considered two approaches to achieve and track the MEP ($Z_{MN_{opt\text{-}\eta}}$), MNs and adjustable ac-dc converters. Various MNs where implemented, and the ac-dc converter design was addressed. We presented the design of a rectifier (Section 3.2.6), a dc-dc converter (Section 3.1) and a unified block that rectifies and increases the input voltage at the same time (Section 3.4). The effects of the MN and the adjustable ac-dc converters in the MEP were discussed and a joint design method was proposed. The proposed design uses the MN to match the load impedance at the largest distance (lowest link efficiency) and highest P_L, while the multiple gains of the ac-dc converter adjust the load impedance for lower distances and P_L. As both MN and ac-dc converter influence V_L, it was verified that the design flow is compatible with V_L regulation. In particular, the influence of the MN in a postregulation system was addressed showing that the MN may affect the attainability of the MEP. Furthermore, we proved that in a multi-coil link, having an odd or even number of coil affects differently the MEP attainability in a postregulated system. Additionally, it was proved that the use of a step-up converter is not the most appropriate way to maximize the output voltage in inductive links. We showed that in many typical cases where the MN has higher efficiency than a dc-dc or ac-dc step-up, the maximum output voltage is obtained using only an MN without a step-up converter.

Regarding the analysis of the inductive link, the inclusion of additional resonant coils was considered. In Section 2 we deduced analytical expressions to compare the 2- and 3- coil links. Although in [38] it is mentioned that the additional coils can play the role of an impedance-matching circuit, we proved that the MN is still needed to maximize the system efficiency. The influence of a third resonant coil in an actual RFID half-duplex system was presented. We showed that the additional coil affects both phases, charging and reading. A high additional coil

quality factor improves the charging distance, but jeopardizing the reading phase due to inter-symbol interference. The trade-off was analyzed proposing a design procedure, increasing the total read range.

Overall, the thesis addressed the topic from the system-level and block level, including the impact of the interaction between blocks.

6.1 Thesis contributions

The main contributions of this thesis are:

- Deduction of simplified equations to compare 2 and 3-coil links with optimized MNs.
- Development of a 3-coil link half-duplex RFID 134.2 kHz system.
- Analysis of the influence of the titanium case in the inductive link of implantable medical devices.
- Development of a joint design flow which exploits the advantages of using both MNs and dc-dc converters in the receiver to achieve load impedance matching.
- Analysis of closed-loop postregulated systems, highlighting the effects that the additional coils, receiver resonance (series or parallel), and type of driver (voltage or current) used in the transmitter, have in the feedback control loop.
- Proposal of systematic analysis and design of charge recycling switches in step-up dc-dc converters.
- New architecture for low-power high slew-rate operational transconductance amplifier.
- Novel architecture for high-efficiency active rectifier.

6.2 Future work

During the last years, many researchers have contributed to WPT from different perspectives which will continue in the years to come. From my point of view, it is needed to continue enhancing the system-level analysis, working in the comparison between different proposed techniques that can be used with the same purpose. Although some of these comparisons have been carried out in this thesis, further work is still needed.

For example, although many authors have proposed active rectifiers that also regulate the output voltage (ac-dc converter, Section 3.4), these architectures have not been widely compared against the use of a traditional active rectifier followed by a dc-dc converter. In a unified ac-dc architecture, as the one presented in

Section 3.4, the capacitors are interconnected at the carrier frequency. However, if a dc-dc converter is used after the rectifier, the switching frequency of the dc-dc converter can be adjusted. Nevertheless, the extra dc-dc increases the number of required switches which may increase losses. With this example, I just intend to highlight that although new architectures are proposed, sometimes they are not properly compared with previous approaches.

Another example addressed in the thesis is the comparison between the different approaches to adjust the load impedance (Z_{MN}). We have analyzed a joint design using MN and adjustable ac-dc converters. However, other approaches exist such as the ones mentioned in Section 4.1.3. Further analysis, including these and other alternatives, would be useful to help designers to decide which approach best fits their system.

The interaction between the WPT link and the target load system should be further analyzed. To efficiently use the power available in a battery, different techniques have been proposed like dynamic voltage frequency scaling. In systems that are periodically or continuously charged wirelessly, a smart power distribution can be implemented. For instance, the system can decide to store the power or increase the voltage/frequency to take advantage of power availability.

Additionally to the previously mentioned general areas, we are currently working in the followings points in order to complete some of the work presented in the thesis.

- The rectifier proposed in Section 3.3, was improved and submitted for fabrication in a 180 nm technology.
- The analysis presented in Section 2.3 will be extended considering different relative position between the receiver coil and the titanium case. In addition, the device heating and specific absorption ratio will be taken into account.
- We are working in the development of long distance WPT systems for AIMDs. In this context, the limitations due to human safety should be included in the analysis presented in the thesis.

6.3 Publications associated with the thesis

6.3.1 Journals

- P. Pérez-Nicoli and F. Silveira, "Maximum efficiency tracking in inductive power transmission using both matching networks and adjustable AC-DC converters," *IEEE Trans. Microw. Theory Techn.*, no. 99, pp. 1–11, 2018
- P. Pérez-Nicoli, A. Rodríguez-Esteva, and F. Silveira, "Bidirectional analysis and design of RFID using an additional resonant coil to enhance read range," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2357–2367, July 2016
- P. Pérez-Nicoli, F. Veirano, P. C. Lisboa, and F. Silveira, "Low-power operational transconductance amplifier with slew-rate enhancement based on

non-linear current mirror," *Analog. Integr. Circ. Sig. Process.*, vol. 89, no. 3, pp. 521–529, 2016

- P. Pérez-Nicoli, P. C. Lisboa, F. Veirano, and F. Silveira, "A series-parallel switched capacitor step-up DC-DC converter and its gate-control circuits for over the supply rail switches," *Analog. Integr. Circ. Sig. Process.*, vol. 85, no. 1, pp. 37–45, 2015

6.3.2 Conferences

- P. Pérez-Nicoli, M. Biancheri-Astier, A. Diet, Y. Le Bihan, L. Pichon, and F. Silveira, "Influence of the titanium case used in implantable medical devices on the wireless power link," in *IEEE Wireless Power Transf. Conf.* IEEE, 2018, pp. 1–3
- P. Pérez-Nicoli and F. Silveira, "Comparator with self controlled delay for active rectifiers in inductive powering," in *IEEE Wireless Power Transf. Conf.* IEEE, 2018, pp. 1–3
- F. Veirano, P. Pérez-Nicoli, P. Castro-Lisboa, and F. Silveira, "Gate drive losses reduction in switched-capacitor DC-DC converters," in *IEEE Latin Amer. Symp. Circuits Syst.* IEEE, 2018
- P. Pérez-Nicoli and F. Silveira, "Reconfigurable multiple-gain active-rectifier for maximum efficiency point tracking in WPT," in *IEEE Latin Amer. Symp. Circuits Syst.*, Feb 2017, pp. 1–4
- P. Pérez-Nicoli and F. Silveira, "Matching networks for maximum efficiency in two and three coil wireless power transfer systems," in *IEEE Latin Amer. Symp. Circuits Syst.* IEEE, Feb. 2016, pp. 215–218
- A. Rodríguez-Esteva, M. S. P. Casulo, B. S. Laborde, P. Pérez-Nicoli, and F. Silveira, "Modelling approach for low-frequency strongly coupled magnetic resonance wireless power transfer system," in *IEEE Argentine School Micro-Nanoelectron., Technol., Appl.*, Aug 2016, pp. 17–21
- P. Pérez-Nicoli, F. Silveira, X. Zhang, and A. Amara, "Uplink wireless transmission overview in bi-directional VLC systems," in *IEEE Int. Conf. Electron., Circuits Syst.*, Dec 2016, pp. 588–591
- P. Pérez-Nicoli, F. Veirano, P. C. Lisboa, and F. Silveira, "High slew-rate OTA with low quiescent current based on non-linear current mirror," in *IEEE Latin Amer. Symp. Circuits Syst.*, Feb 2015, pp. 1–4

6.4 Publications non associated with the thesis

6.4.1 Journals

- P. C. Lisboa, P. Pérez-Nicoli, F. Veirano, and F. Silveira, "General top/bottom-

plate charge recycling technique for integrated switched capacitor DC-DC converters," *IEEE Trans. Circuits Syst. I*, vol. 63, no. 4, pp. 470–481, April 2016

6.4.2 Conferences

- P. Pérez-Nicoli, F. Veirano, C. Rossi-Aicardi, and P. Aguirre, "Design method for an ultra low power, low offset, symmetric OTA," in *IEEE Argentine School Micro-Nanoelectron., Technol., Appl.*, Aug 2013, pp. 38–43
- F. Veirano, P. Pérez-Nicoli, S. Besio, P. Castro, and F. Silveira, "Ultra low power pulse generator based on a ring oscillator with direct path current avoidance," in *IEEE Latin Amer. Symp. Circuits Syst.*, Feb 2013, pp. 1–4

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Appendix A

RFID: three-coil charging phase calculations. Apendix of Section 2.2

A.1 Tag efficiency

In order to simplify the model, we make two approximations. First, we assume that the diode of the half-wave rectifier is ideal and therefore does not dissipate. Hence $V_{C_{T_p}} = V_{C_L}$ where $V_{C_{T_p}}$ is the peak voltage at C_T and V_{C_L} is the DC voltage at C_L (see Fig. 2.8h). Second, we approximate the effect of the diode and its load (C_L, R_L) by a resistor R_{vL}, making the overall model linear and, hence, easily tractable. R_{vL} is determined so that the mean power dissipated in R_{vL} ($\overline{P_{R_{vL}}}$) is equal to the power dissipated in R_L (P_{R_L}). This results in $R_{vL} = R_L/2$ as seen in the following equation (A.1).

$$\overline{P_{R_{vL}}} = \frac{V_{C_{T_p}}^2}{2.R_{vL}} = \frac{V_{C_{T_p}}^2}{R_L} = \frac{V_{C_L}^2}{R_L} = P_{R_L} \tag{A.1}$$

The tag efficiency (A.2) is calculated as the ratio between the power dissipated in R_L over the total power dissipated in R_L and R_{pT} (see Fig. 2.8h).

$$\eta_{T_{(C)}} = \frac{I_T^2 Re\{Z_L\}}{I_T^2 R_{pT} + I_T^2 Re\{Z_L\}} \tag{A.2}$$

$Re\{Z_L\}$ is simply calculated as (see Fig. 2.10c),

$$\begin{aligned} Z_L = R_{vL} // \frac{1}{jwC_T} = \frac{R_L/2}{jwC_T.R_L/2+1} \Longrightarrow \\ \left.\begin{array}{l} \Longrightarrow Re\{Z_L\} = \frac{R_L/2}{(wC_T.R_L/2)^2+1} \\ \frac{1}{\sqrt{C_T.L_T}} = w_{res_T} \rightarrow C_T = \frac{1}{w_{res_T}^2 L_T} \end{array}\right\} \Longrightarrow \\ \Longrightarrow Re\{Z_L\} = \frac{R_L/2}{\left(\frac{w.R_L/2}{w_{res_T}^2 L_T}\right)^2+1} \simeq \frac{(w.L_T)^2}{R_L/2}.\left(\frac{w_{res_T}}{w}\right)^4 \\ Im\{Z_L\} = \frac{-R_L/2.jwC_T.R_L/2}{(wC_T.R_L/2)^2+1} \simeq \frac{1}{jwC_T} \end{aligned} \tag{A.3}$$

where $(wC_T.R_L/2)^2 = \left(\frac{R_L/2}{w.L_T}\right)^2 \left(\frac{w}{w_{res_T}}\right)^4 >> 1$ was assumed. Finally from (A.2) and (A.3),

$$\eta_{T_{(C)}} = \frac{Q_T}{Q_T + Q_{L_{(C)}}} \tag{A.4}$$

$$Q_{L_{(C)}} = \frac{wL_T}{Re\{Z_L\}} = \frac{R_L/2}{w.L_T}\left(\frac{w}{w_{res_T}}\right)^4 \tag{A.5}$$

$$Q_T = \frac{wL_T}{R_{pT}} \tag{A.6}$$

A.2 Additional coil efficiency

In order to calculate $\eta_{A_{(C)}}$, The reflected impedance in the additional coil from the tag Z_{TAref} (Fig. 2.8g and Fig. A.1) should be computed first.

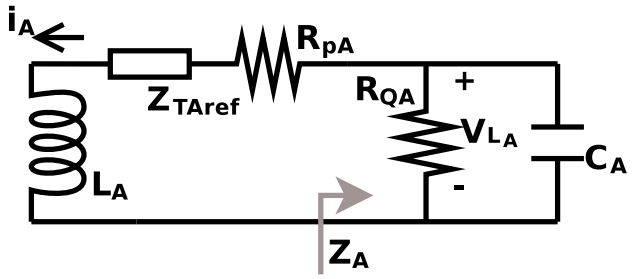

Figure A.1: Additional coil model, including the reflected inductance from the tag.

$$\left.\begin{array}{l} V_{L_A} = (R_{pA} + jwL_A)i_A + jwM_{AT}i_T \\ i_T = \frac{-i_A jwM_{AT}}{R_{pT}+jwL_T+Z_L} \end{array}\right\} \Longrightarrow$$
$$\Longrightarrow V_{L_A} = (R_{pA} + jwL_A)i_A + \frac{w^2M_{AT}^2}{R_{pT}+jwL_T+Z_L}i_A \tag{A.7}$$

where M_{AT} is the mutual inductance between the tag and the reader, $M_{AT} = k_{AT}\sqrt{L_A L_T}$. Z_L was found in (A.3), so Z_{TAref} is,

$$\begin{aligned} Z_{TAref} &= \frac{w^2k_{AT}^2L_AL_T}{R_{pT} + \frac{(w.L_T)^2}{R_L/2}.\left(\frac{w_{res_T}}{w}\right)^4 + jwL_T + 1/jwC_T} \\ &= \frac{w^2k_{AT}^2L_AL_T}{R_{pT} + \frac{(w.L_T)^2}{R_L/2}.\left(\frac{w_{res_T}}{w}\right)^4 + jwL_T(1-(w_{res_T}/w)^2)} \\ &= \frac{k_{AT}^2wL_A}{\frac{R_{pT}}{wL_T} + \frac{(w.L_T)}{R_L/2}.\left(\frac{w_{res_T}}{w}\right)^4 + j(1-(w_{res_T}/w)^2)} \\ &= \frac{k_{AT}^2wL_AQ_TQ_{L_{(C)}}}{Q_T + Q_{L_{(C)}} + jQ_TQ_{L_{(C)}}(1-(w_{res_T}/w)^2)} \end{aligned} \tag{A.8}$$

Additionally, R_{QA} can be substituted by an equivalent series resistance, in order to do that Z_A (Fig. A.1) is calculated in a way similar to the one for (A.3),

$$\begin{aligned} Z_A =& R_{QA} // \frac{1}{jwC_A} \Longrightarrow \\ Re\{Z_A\} =& \frac{R_{QA}}{\left(\frac{w.R_{QA}}{w_{res_A}^2 L_A}\right)^2 + 1} \simeq \frac{(w.L_A)^2}{R_{QA}}.\left(\frac{w_{res_A}}{w}\right)^4 \\ Im\{Z_A\} =& \frac{-R_{QA}.jwC_A.R_{QA}}{(wC_A.R_{QA})^2 + 1} \simeq \frac{1}{jwC_A} \end{aligned} \tag{A.9}$$

where $(wC_A.R_{QA})^2 = \left(\frac{R_{QA}}{w.L_A}\right)^2 \left(\frac{w}{w_{res_A}}\right)^4 >> 1$ was assumed. Thus, the circuit of Fig. A.1 can be simplified as is shown on Fig. 2.10b, where R_{pAeq} is defined as,

$$R_{pAeq} = \frac{(w.L_A)^2}{R_{QA}}.\left(\frac{w_{res_A}}{w}\right)^4 + R_{pA} \tag{A.10}$$

The normalized reflected impedance in the additional coil from the tag ($\overline{Z_{TAref}}$) is calculated from (A.8),

$$\begin{aligned} \overline{Z_{TAref}} =& Z_{TAref}/R_{pAeq} \\ =& \frac{k_{AT}^2 Q_T Q_A Q_{L_{(C)}}}{Q_T + Q_{L_{(C)}} + jQ_T Q_{L_{(C)}}(1 - (w_{res_T}/w)^2)} \end{aligned} \tag{A.11}$$

$$Q_A = \frac{wL_A}{R_{pAeq}} \tag{A.12}$$

Finally, the additional coil efficiency $\eta_{A_{(C)}}$ is calculated (see Fig. 2.10b) as the ratio between the power dissipated in R_{pAeq} over the total power dissipated in R_{pAeq} and Z_{TAref}.

$$\eta_{A_{(C)}} = \frac{Re\{\overline{Z_{TAref}}\}}{1 + Re\{\overline{Z_{TAref}}\}} \tag{A.13}$$

A.3 Reader efficiency

The Z_{ARref} (Fig. 2.10a) can be obtained in a way similar to the one applied for (A.7) and (A.8),

$$\left.\begin{array}{l} Z_{ARref} = \frac{w^2 k_{RA}^2 L_R L_A}{R_{pAeq} + Z_{TAref} + jwL_A(1-(w_{res_A}/w)^2)} \\ \overline{Z_{ARref}} = Z_{ARref}/R_{pR} \\ \overline{Z_{ARref}} = \frac{k_{RA}^2 Q_A Q_R}{1 + \overline{Z_{TAref}} + jQ_A(1-(w_{res_A}/w)^2)} \end{array}\right\} \Longrightarrow \tag{A.14}$$

$$Q_R = \frac{wL_R}{R_{pR}} \tag{A.15}$$

Appendix A. RFID: three-coil charging phase calculations. Apendix of Section 2.2

Now the effect of R_{QR} is analyzed by calculating Z_{eqR} (Fig. 2.10a). $(R_{pR} + Z_{ARref})$ is referred to as Z^*. The imaginary part of Z^* is assumed to be much lower than jwL_R. This is usually the case based on operation close to resonance of the additional coil and low coupling factor k_{RA}, see (A.14).

$$\begin{aligned} Z_{eqR} =& \frac{(Z^* + L_R jw)R_{QR}}{Z^* + R_{QR} + L_R jw} \simeq \frac{(Re\{Z^*\} + L_R jw)R_{QR}}{Re\{Z^*\} + R_{QR} + L_R jw} \Longrightarrow \\ Re\{Z_{eqR}\} =& \frac{R_{QR}[Re\{Z^*\}(Re\{Z^*\} + R_{QR}) + (L_R w)^2]}{(Re\{Z^*\} + R_{QR})^2 + (L_R w)^2} \\ \simeq& Re\{Z^*\} + \frac{(L_R w)^2}{R_{QR}} \\ Im\{Z_{eq}\} =& \frac{R_{QR} L_R w(2Re\{Z^*\} + R_{QR})}{(Re\{Z^*\} + R_{QR})^2 + (L_R w)^2} j \simeq L_R jw \end{aligned} \tag{A.16}$$

It was assumed that $R_{QR} >> Re\{Z^*\}$ and $(R_{QR})^2 >> (wL_R)^2$. These assumptions usually hold for typical designs like the one under study in this work where high R_{QR} values are used. If this were not the case the analysis presented is not fundamentally altered. As a conclusion R_{QR} increases the series resistance of L_R without altering the imaginary part.

Then, the reader efficiency $\eta_{R_{(C)}}$ is obtained as the power dissipated in Z_{ARref} divided by the total power dissipated in $R_{pR} + \frac{(L_R w)^2}{R_{QR}}$, R_{out_R} and Z_{ARref}.

$$\begin{aligned} \eta_{R_{(C)}} =& \frac{Re\{Z_{ARref}\}}{R_{pR} + \frac{(L_R w)^2}{R_{QR}} + R_{out_R} + Re\{Z_{ARref}\}} \\ =& \frac{Re\{\overline{Z_{ARref}}\}}{1 + Q_R^2 \frac{R_{pR}}{R_{QR}} + \frac{R_{out_R}}{R_{pR}} + Re\{\overline{Z_{ARref}}\}} \end{aligned} \tag{A.17}$$

Appendix B

Active rectifier design. Appendix of Section 3.3.1

This appendix presents the analysis of the active rectifier shown in Fig. 3.27 [102–105]. The design carried out to determine the width of the switches is also explained.

The main voltages of the rectifier are represented as a function of time in Fig. B.1, where four operation zones are defined. All the operation zones are depicted in Fig. B.2. While $0 < V_1 - V_2 < V_{rec}$ (Zone I), only MP1 is ON thus $V_1 = V_{rec}$. The increase in the input voltage $(V_1 - V_2)$ generates a reduction in V_2 until it reaches *gnd*, which happens when $V_1 - V_2 = V_{rect}$. When $V_1 - V_2 > V_{rec}$ (zone II) MN2 is turned on, and the charge is delivered to the output node through transistors MN2 and MP1. The zones III and IV are analogous to zones I and II respectively, but with a different polarity.

We define the duty-cycle of the rectifier as

$$D = \frac{T_{ON-II} + T_{ON-IV}}{T} \tag{B.1}$$

where T is the input signal period, T_{ON-II} and T_{ON-IV} are the lapses were MN2 and MN1 are ON, respectively. This duty-cycle is used as a design parameter, and an optimum value for it exists as shown next. In the remainder of this

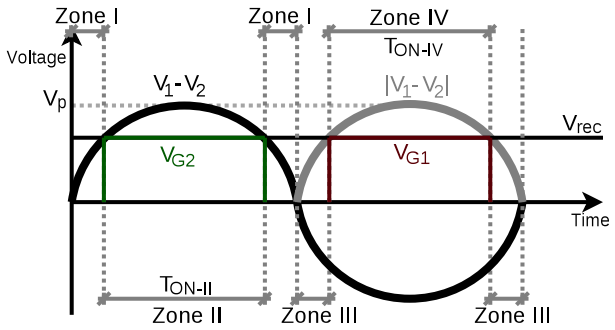

Figure B.1: Voltages representation of the circuit shown in Fig. 3.27.

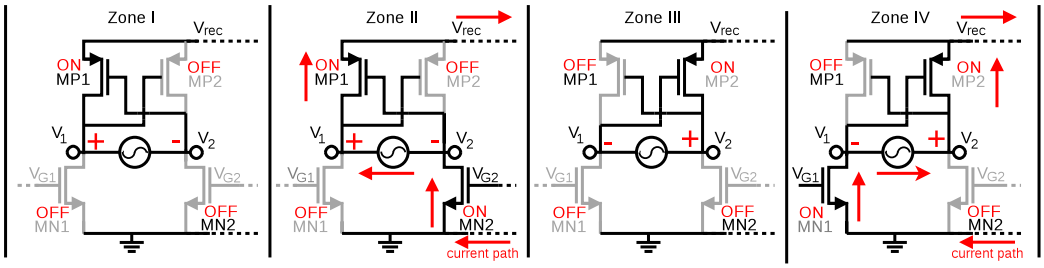

Figure B.2: Transistors states for each operation zone defined in Fig. B.1.

appendix, we calculate the rectifier efficiency for each D, to find the optimum design (transistors widths, W_{PMOS} and W_{NMOS}) that maximize the efficiency.

For each D, the output voltage V_{rec} is calculated evaluating $V_1 - V_2$ at the end of zone I, obtaining

$$V_{rec} = V_p sin(\frac{\pi}{2}(1-D)) \tag{B.2}$$

where V_p is the input peak voltage.

Then, if steady state was achieved, the charge delivered by the rectifier must be equal to the charge consumed by the load R_L

$$\frac{T.V_{rec}}{R_L} = 2\int_{t=\frac{T}{4}(1-D)}^{t=\frac{T}{4}(1+D)} \frac{(V_1 - V_2) - V_{rec}}{R_{out}} dt \tag{B.3}$$

where R_{out} is the rectifier total output resistance, determined by the series of MN2 and MP1 in zone II, or MN1 and MP2 in zone IV. The PMOS transistors are self-driven, the wider they are, the higher the input capacitance is. However, an increase in the PMOS width does not imply an increase in the power consumed to drive its gates. Therefore, the PMOS can be set much wider than the NMOS. If $W_{PMOS} >> W_{NMOS}$, R_{out} is approximately equal to the NMOS drain-source resistance. This is an advantage of this rectifier architecture, where only the NMOS transistors generate voltage drop and power losses, and the PMOS transistors practically work as ideal switches.

From R_{out}, W_{NMOS} is estimated for a minimum length transistor.

Finally, the conduction loss and gate drive loss can be calculated as (B.4) and (B.5), respectively. The gate parasitic capacitance of NMOS transistors, C_{NMOS} used in (B.5), can be obtained from simulation and depends on W_{NMOS}. In order to consider the overhead power consumption of the buffers that drive the NMOS gates, in (B.5) the gate power consumption is multiplied by 1.25 [125].

$$P_{cond} = \frac{2}{T}\int_{t=\frac{T}{4}(1-D)}^{t=\frac{T}{4}(1+D)} \frac{[(V_1 - V_2) - V_{rec}]^2}{R_{out}} dt \tag{B.4}$$

$$P_{gd} = 2C_{NMOS}V_{rec}^2\frac{1}{T} \times 1.25 \tag{B.5}$$

The power conversion efficiency (B.6), is calculated as the ratio between $P_{out} = V_{rec}^2/R_L$ and the total input power.

$$\text{PCE} = \frac{P_{out}}{P_{out} + P_{cond} + P_{gd} + P_{comp}} \tag{B.6}$$

In this design to find the optimum widths, P_{comp} was considered zero. The design procedure can be redone once P_{comp} is obtained, but this does not considerably affect the rectifier design.

Summarizing, for each D the R_{out} is calculated from (B.2) and (B.3), the W_{NMOS} that sets that R_{out} can be found from simulations of the technology used. Finally, the rectifier efficiency is calculated using (B.4), (B.5) and (B.6).

This design flow was done in a 130 nm technology. The drain-source resistivity and gate capacitance were extracted for this technology for different transistors widths. The design procedure assumes $V_p = 1.2$ V with a frequency of 13.56 MHz, a load resistance $R_L = 1$ kΩ and $C_L = 2$ nF. The design led to a W/L=304μm/120nm for MN1 and MN2. The PMOS transistors are self-driven thus they were selected much wider, W/L=5000μm/120nm (MP1 and MP2).

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Appendix C

Multiple-gain rectifier design. Appendix of Section 3.4.1

A numerical model was implemented to determine the size of the switches. A brief description of this design is done in this appendix.

In order to estimate the efficiency, conduction losses, gate-drive power, and diffusion parasitic capacitance were considered. The ON-resistance, gate and diffusion parasitic capacitance were extracted from simulations as a function of transistor width. Hence, the converter losses and output power can be estimated from the load impedance R_L and transistors sizes, to find the optimum combination.

Some switches are shared between different conversion ratios, and its optimum size depends on which ratio is prioritized. As was discussed before, usually the largest or lowest gains are the most critical ones. Therefore, based on the analysis presented in 3.4.3, the converter switches sizes were designed at x3 with $R_L = 2\,\mathrm{k}\Omega$. In x2, the switches sizes will not be optimum, but on the other hand the converter efficiency will tend to increase because fewer switches are used.

NMOS transistors are used for $T1$ switches in Cellx2 and Cellx3 and $T2$x2 switch as it presents lower resistance than PMOS for that voltage ranges. PMOS transistors are used for $T2_{out}$x1, $T2_{out}$x2, $T2_{out}$x3 and $T2$x3.

Cellx1 has the following differences. At unitary conversion ratio, more power has to be delivered to the load, and NMOS switches cannot be used for $T1_{A_{up}}$ and $T1_{B_{up}}$. Therefore, in Cellx1 CMOS switches were used in $T1_{A_{up}}$ and $T1_{B_{up}}$, switching on the NMOS when x2 and x3 and the PMOS when x1. Additionally, two NMOS transistors were used in each $T1_{A_{down}}$ and $T1_{B_{down}}$ switch to provide extra width at high output power (when x1) (switch segmentation). This extra PMOS due to the use of CMOS switches in $T1_{A_{up}}$ and $T1_{B_{up}}$ and the extra NMOS on $T1_{A_{down}}$ and $T1_{B_{down}}$ (Cellx1) where designed to maximize the efficiency of x1 at $R_L = 200\Omega$.

To reduce the number of design variables (transistor sizes), we calculate the optimum width distribution for a series of switches to achieve certain total resistance minimizing gate-drive power consumption. By doing it, all the $T1$ switches widths are included in only one design variable (their total series resistance R_{TOT}). The same is done with $T2$, where only its R_{TOT} is swept during the design, and

then all the $T2$ transistor widths are obtained from (C.1).

$$W_j = \sqrt{\frac{1}{M_j J_j}} \frac{1}{R_{TOT}} \left(\sum_{i=1}^{N} \sqrt{\frac{J_i}{M_i}} \right) \tag{C.1}$$

In (C.1), W_j is the width of transistor j, R_{TOT} is the total resistance of all the N switches in series, J_i and M_i are, respectively, the energy spent to drive the gate and the conductivity of the switch i per transistor width. In our architecture, J_i only depends on the technology used since the same voltage is used to turn ON and OFF all the switches. However, M_i is different for each switch as the conductivity also depends on the diffusion voltages. It can be noted that if all the switches are in the same conditions ($J_i = J_j$ and $M_i = M_j \; \forall \; i, j$), thus $W_j = N/(R_{TOT} M) \; \forall \; j$. This result is a generalization of the one presented in [126] where a similar result was obtained in the particular case of the series of one PMOS and one NMOS transistor.

Appendix D

Comparison between pre- and post-regulation. Appendix of Section 5.1

The Table D.1 presents a brief comparison between pre- and post- regulation method.

Since postegulation controls V_L directly in the receiver, it is more stable under $k_{TX\text{-}RX}$ and R_L changes. In previous preregulation works [29, 120], an LDO is added to improve V_L stability. However, this LDO increases losses, especially while its input voltage ($V_{LDO_{in}}$) is being adjusted. Additionally, once the LDO input voltage is regulated to $V_{LDO_{in}} \cong V_L$, a sudden decrease in $k_{TX\text{-}RX}$ affects V_L until the feedback amends the driver. This takes more time in comparison with postregulation as it depends on back telemetry throughput and inductive link response time.

In preregulation, Z_{MN} is directly controlled in the receiver which assures that $Z_{MN_{opt\text{-}\eta}}$ is quickly reached. However, the value of $Z_{MN_{opt\text{-}\eta}}$ depends on $k_{TX\text{-}RX}$ and its value is unknown in many applications. Although it is possible to measure $k_{TX\text{-}RX}$ [127], it adds complexity to the system which jeopardizes efficiency. In postregulation $Z_{MN_{opt\text{-}\eta}}$ can be achieved from the driver without any back teleme-

Table D.1: Preregulation and Postregulation comparison.

Preregulation	Postregulation
V_L regulation: • Depends on back telemetry	V_L regulation: • No back telemetry needed.
MEPT: • Fast: Z_{MN} is directly controlled in the receiver • Complex implementation: $Z_{MN_{opt\text{-}\eta}}$, which depends on the coupling ($k_{TX\text{-}RX}$), is needed	MEPT: • Slow: based on perturbation and observation, but back telemetry is not needed • Simple implementation: $Z_{MN_{opt\text{-}\eta}}$ not needed.

try, as it is explained below. Assuming that the receiver dc-dc converter is working and able to deliver the P_L demanded by the load, the MEP is tracked adjusting V_{TH} until P_{TX} is minimized which can be measured in the same transmitter [33, 123]. When P_{TX} is minimized, $Z_{MN_{opt\text{-}\eta}}$ is indirectly achieved. However, this is not possible in all systems as discussed in Chapter 5. This minimum P_{TX} is usually reached by a perturbation and observation method whose main drawback is its slow convergence since after each perturbation the driver control has to wait until the system has reached a new stable point.

Appendix E

Postregulation in 3-coil link. Appendix of Section 5.3.3

In this section, the same analysis done in Section 5.3.3 is carried out for the case of 3-coil link. The circuit schematic is presented in Fig. E.1, the same two coil used in Section 5.3.3 were used here for the TX and RX respectively, together with an additional coil with self inductance L_A and parasitic resistance R_A. In this 3-coil system, the receiver and the auxiliary coils are tuned to resonate at the carrier frequency (f) and a total resultant impedance will be considered in the transmitter (X_{TH}) as was done in Section 5.3.3.

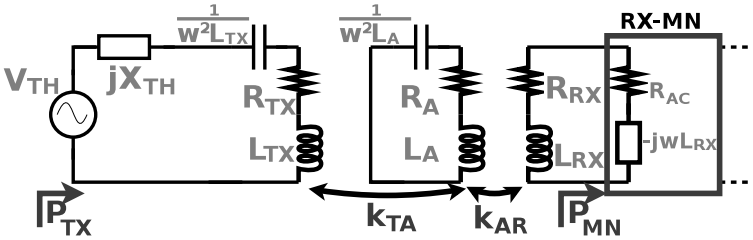

Figure E.1: Schematic circuit for a 3-coil link with postregulation.

The link efficiency (η_{Link}) in this case is (E.1) while (E.2) presents the power received by the RX-MN. In order to simplify the notation, $\alpha = k_{TA}^2 Q_{TX} Q_A$, $\beta = k_{AR}^2 Q_A Q_{RX}$ and $\gamma = k_{AR}^2 Q_A Q_{RX\text{-}L}$ were defined.

$$\eta_{Link} = \frac{P_{MN}}{P_{TX}} = \frac{Q_{RX\text{-}L}}{Q_L} \frac{\gamma}{\gamma+1} \frac{\alpha}{\alpha+\gamma+1} \tag{E.1}$$

$$P_C = \frac{Q_{RX\text{-}L}}{Q_L} \frac{\eta_{MN}\eta_{rect}\alpha\gamma}{(X_{TH}/R_{TX})^2(\gamma+1)^2 + (\alpha+\gamma+1)^2} \frac{V_{TH}^2}{2} \tag{E.2}$$

$$P_{C-i} = \frac{Q_{RX\text{-}L}}{Q_L} \frac{\eta_{MN}\eta_{rect}\gamma\alpha}{(\gamma+1)^2} \frac{I_T^2 R_{TX}}{2} \tag{E.3}$$

Appendix E. Postregulation in 3-coil link. Appendix of Section 5.3.3

Table E.1: 3-coil R_{AC} different optimum values.

$R_{opt-\eta} = R_{RX}\sqrt{\frac{(\beta+1)(\alpha+\beta+1)}{\alpha+1}}$	(E.4)
$R_{opt-P} = R_{RX}\sqrt{\frac{(X_{TH}/R_{TX})^2(1+\beta)^2+(\alpha+\beta+1)^2}{(X_{TH}/R_{TX})^2+(\alpha+1)^2}}$	(E.5)
$R_{opt-P_{vTXres}} = R_{RX}\frac{\alpha+\beta+1}{\alpha+1}$	(E.6)
$R_{opt-P_i} = R_{RX}(1+\beta)$	(E.7)

Table E.2: 3-coil proof-of-concept cases.

Case	Components values
All	$L_{TX} = 1.18\ \mu$H ; $Q_{TX} = wL_{TX}/R_{TX} = 95.7$ (Pulse Elec. W7002)
All	$L_A = 1.18\ \mu$H ; $Q_A = wL_A/R_A = 95.7$ (Pulse Elec. W7002)
All	$L_{RX} = 877$ nH ; $Q_{RX} = wL_{RX}/R_{RX} = 27.2$ (Pulse Elec. W7001)
All	$k_{TA} = 0.059$ ($D_{TA} = 5$ cm); $k_{AR} = 0.056$ ($D_{AR} = 2$ cm)
All	$f = 13.56$ MHz ; $P_L = 20$ mW
All	$\eta_{driver} \simeq 90\%$; $\eta_{MN} \simeq 100\%$; $\eta_{rect} \simeq 90\%$; $\eta_{RX_{dc-dc}} \simeq 75\%$
I	$I_T = 90$ mA ; $X_{TH} = 0\ \Omega$; Parallel RX-MN (5.5)
II	$I_T = 90$ mA ; $X_{TH} = 0\ \Omega$; Series RX-MN (5.4)
III	$V_{TH} = 1.5$ V ; $X_{TH} = 0\ \Omega$; Parallel RX-MN (5.5)
IV	$V_{TH} = 1.5$ V ; $X_{TH} = 0\ \Omega$; Series RX-MN (5.4)
V	$V_{TH} = 1.5$ V ; $X_{TH} = 10\ \Omega$; Parallel RX-MN (5.5)
VI	$V_{TH} = 1.5$ V ; $X_{TH} = 10\ \Omega$; Series RX-MN (5.4)

V_{TH} and I_T are peak values

The values that maximize η_{Link} and P_C are (E.4) and (E.5) respectively. In the particular case where a current driver is used, the power that reaches RX-MN will be (E.3). The optimum values for the particular cases of a voltage driver and a current driver with a resonant transmitter are (E.6) and (E.7) respectively.

The component values for the same six cases used in Section 5.3.3 are presented in Table E.2, and the operating point for each case is highlighted in Fig. E.2.

It is evident that the inclusion of an additional coil modifies the operating point as it affects not only η_{Link} but also P_C as a function R_{AC}. It is easy to observe that the relative positions of the six cases studied in Fig. E.2 were modified with respect to the case of Fig. 5.6. From equations (E.4), (E.5), (E.6) and (E.7) it can be proved that in this case of 3-coil link $R_{opt-P_{vTXres}} < R_{opt-P} < R_{opt-P_i}$ and $R_{opt-P_{vTXres}} < R_{opt-\eta} < R_{opt-P_i}$ always. Thus, now the R_{AC} at the operating point in II is always higher than $R_{opt-\eta}$ while the R_{AC} at the operating point in

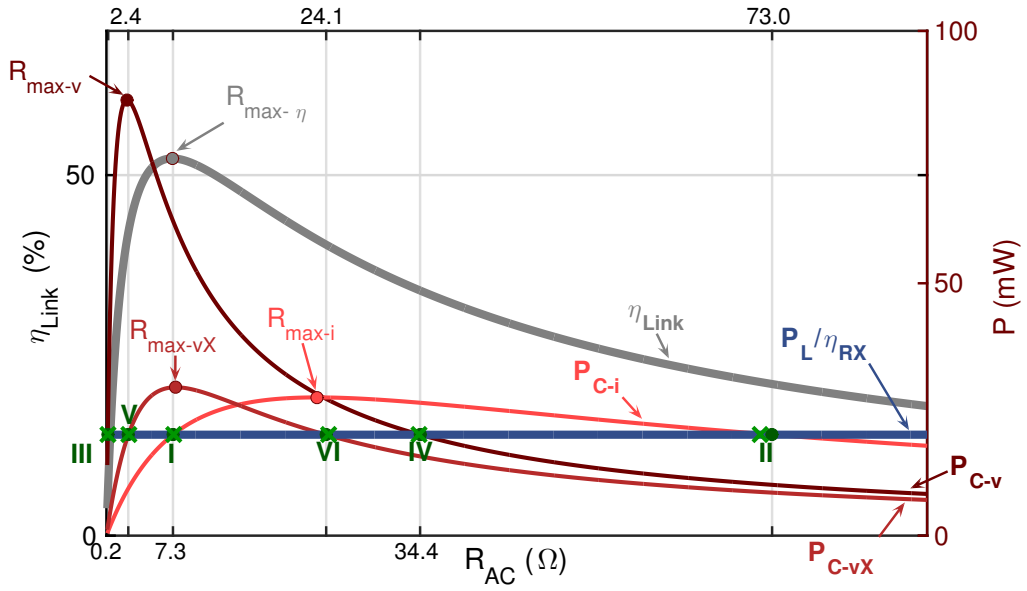

Figure E.2: 3-coil operating point Analysis. P_L is the power delivered to the load, P_{C-v} and P_C are the power that reaches the receiver (RX-MN) using a voltage driver with a resonant and non-resonant transmitter respectively, and P_{C-i} is the power that reaches the receiver (RX-MN) if a current source drives a resonant transmitter. These plots were generated using the proof-of-concept values presented in Table E.2. The cross-marks are spice simulations of each case.

III is always lower than $R_{opt-\eta}$.

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Bibliography

[1] P. Pérez-Nicoli, P. C. Lisboa, F. Veirano, and F. Silveira, "A series-parallel switched capacitor step-up DC-DC converter and its gate-control circuits for over the supply rail switches," *Analog. Integr. Circ. Sig. Process.*, vol. 85, no. 1, pp. 37–45, 2015.

[2] P. Pérez-Nicoli, F. Veirano, P. C. Lisboa, and F. Silveira, "High slew-rate OTA with low quiescent current based on non-linear current mirror," in *IEEE Latin Amer. Symp. Circuits Syst.*, Feb 2015, pp. 1–4.

[3] P. Pérez-Nicoli and F. Silveira, "Matching networks for maximum efficiency in two and three coil wireless power transfer systems," in *IEEE Latin Amer. Symp. Circuits Syst.* IEEE, Feb. 2016, pp. 215–218.

[4] P. Pérez-Nicoli, F. Veirano, P. C. Lisboa, and F. Silveira, "Low-power operational transconductance amplifier with slew-rate enhancement based on non-linear current mirror," *Analog. Integr. Circ. Sig. Process.*, vol. 89, no. 3, pp. 521–529, 2016.

[5] P. Pérez-Nicoli, A. Rodríguez-Esteva, and F. Silveira, "Bidirectional analysis and design of RFID using an additional resonant coil to enhance read range," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 7, pp. 2357–2367, July 2016.

[6] P. Pérez-Nicoli and F. Silveira, "Reconfigurable multiple-gain active-rectifier for maximum efficiency point tracking in WPT," in *IEEE Latin Amer. Symp. Circuits Syst.*, Feb 2017, pp. 1–4.

[7] P. Pérez-Nicoli and F. Silveira, "Maximum efficiency tracking in inductive power transmission using both matching networks and adjustable AC-DC converters," *IEEE Trans. Microw. Theory Techn.*, no. 99, pp. 1–11, 2018.

[8] P. Pérez-Nicoli and F. Silveira, "Comparator with self controlled delay for active rectifiers in inductive powering," in *IEEE Wireless Power Transf. Conf.* IEEE, 2018, pp. 1–3.

[9] P. Pérez-Nicoli, M. Biancheri-Astier, A. Diet, Y. Le Bihan, L. Pichon, and F. Silveira, "Influence of the titanium case used in implantable medical devices on the wireless power link," in *IEEE Wireless Power Transf. Conf.* IEEE, 2018, pp. 1–3.

[10] F. Veirano, P. Pérez-Nicoli, S. Besio, P. Castro, and F. Silveira, "Ultra low power pulse generator based on a ring oscillator with direct path current avoidance," in *IEEE Latin Amer. Symp. Circuits Syst.*, Feb 2013, pp. 1–4.

[11] P. Pérez-Nicoli, F. Veirano, C. Rossi-Aicardi, and P. Aguirre, "Design method for an ultra low power, low offset, symmetric OTA," in *IEEE Argentine School Micro-Nanoelectron., Technol., Appl.*, Aug 2013, pp. 38–43.

[12] A. Rodríguez-Esteva, M. S. P. Casulo, B. S. Laborde, P. Pérez-Nicoli, and F. Silveira, "Modelling approach for low-frequency strongly coupled magnetic resonance wireless power transfer system," in *IEEE Argentine School Micro-Nanoelectron., Technol., Appl.*, Aug 2016, pp. 17–21.

[13] P. Pérez-Nicoli, F. Silveira, X. Zhang, and A. Amara, "Uplink wireless transmission overview in bi-directional VLC systems," in *IEEE Int. Conf. Electron., Circuits Syst.*, Dec 2016, pp. 588–591.

[14] F. Veirano, P. Pérez-Nicoli, P. Castro-Lisboa, and F. Silveira, "Gate drive losses reduction in switched-capacitor DC-DC converters," in *IEEE Latin Amer. Symp. Circuits Syst.* IEEE, 2018.

[15] P. C. Lisboa, P. Pérez-Nicoli, F. Veirano, and F. Silveira, "General top/bottom-plate charge recycling technique for integrated switched capacitor DC-DC converters," *IEEE Trans. Circuits Syst. I*, vol. 63, no. 4, pp. 470–481, April 2016.

[16] N. Shinohara, "History of research and development of beam wireless power transfer," in *IEEE Wireless Power Transf. Conf.* IEEE, 2018, pp. 1–3.

[17] P. E. Glaser, "Power from the sun: Its future," *Science*, vol. 162, no. 3856, pp. 857–861, 1968.

[18] T. Sun, X. Xie, and Z. Wang, *Wireless power transfer for medical microsystems*. Springer, 2013.

[19] J. Dai and D. C. Ludois, "A survey of wireless power transfer and a critical comparison of inductive and capacitive coupling for small gap applications," *IEEE Trans. Power Electron.*, vol. 30, no. 11, pp. 6017–6029, Nov 2015.

[20] K. Van Schuylenbergh and R. Puers, *Inductive powering: basic theory and application to biomedical systems*. Springer Science & Business Media, 2009.

[21] H. Kim, C. Song, D. H. Kim, D. H. Jung, I. M. Kim, Y. I. Kim, J. Kim, S. Ahn, and J. Kim, "Coil design and measurements of automotive magnetic resonant wireless charging system for high-efficiency and low magnetic field leakage," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 383–400, Feb 2016.

[22] S. H. Lee and R. D. Lorenz, "Development and validation of model for 95%-efficiency 220-W wireless power transfer over a 30-cm air gap," *IEEE Trans. Ind. Appl.*, vol. 47, no. 6, pp. 2495–2504, Nov. 2011.

[23] D. H. Kim, J. Kim, and Y. J. Park, "Optimization and design of small circular coils in a magnetically coupled wireless power transfer system in the megahertz frequency," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 8, pp. 2652–2663, Aug 2016.

[24] M. Benamara, M. Grzeskowiak, A. Diet, G. Lissorgues, Y. L. Bihan, S. Protat, and C. Conessa, "A twisted loop antenna to enhance HF RFID detection for different tag positioning," in *Eur. Conf. Antennas Propag.*, Apr. 2016, pp. 1–5.

[25] M. Kiani and M. Ghovanloo, "The circuit theory behind coupled-mode magnetic resonance-based wireless power transmission," *IEEE Trans. Circuits Syst. I*, vol. 59, no. 9, pp. 2065–2074, Sept. 2012.

[26] H.-M. Lee and M. Ghovanloo, "An integrated power-efficient active rectifier with offset-controlled high speed comparators for inductively powered applications," *IEEE Trans. Circuits Syst. I*, vol. 58, no. 8, pp. 1749–1760, Jan. 2011.

[27] H. M. Lee and M. Ghovanloo, "A high frequency active voltage doubler in standard CMOS using offset-controlled comparators for inductive power transmission," *IEEE Trans. Biomed. Circuits Syst.*, vol. 7, no. 3, pp. 213–224, Jun. 2013.

[28] X. Zhang and H. Lee, "A reconfigurable 2x/ 2.5x/ 3x/ 4x SC DC-DC regulator for enhancing area and power efficiencies in transcutaneous power transmissions," in *IEEE Custom Integrated Circuits Conf.*, Sept. 2011, pp. 1–4.

[29] H. Lee, "An auto-reconfigurable 2x/4x AC-DC regulator for wirelessly powered biomedical implants with 28% link efficiency enhancement," *IEEE Trans. VLSI Syst.*, vol. PP, no. 99, pp. 1–1, 2015.

[30] X. Li, C. Y. Tsui, and W. H. Ki, "Power management analysis of inductively-powered implants with 1x/2x reconfigurable rectifier," *IEEE Trans. Circuits Syst. I*, vol. 62, no. 3, pp. 617–624, March 2015.

[31] M. Fu, H. Yin, X. Zhu, and C. Ma, "Analysis and tracking of optimal load in wireless power transfer systems," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3952–3963, Jul. 2015.

[32] Y. Huang, N. Shinohara, and T. Mitani, "Impedance matching in wireless power transfer," *IEEE Trans. Microw. Theory Techn.*, vol. 65, no. 2, pp. 582–590, Feb 2017.

[33] W. X. Zhong and S. Y. R. Hui, "Maximum energy efficiency tracking for wireless power transfer systems," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 4025–4034, Jul. 2015.

[34] T. C. Beh, M. Kato, T. Imura, S. Oh, and Y. Hori, "Automated impedance matching system for robust wireless power transfer via magnetic resonance coupling," *IEEE Trans. Ind. Electron.*, vol. 60, no. 9, pp. 3689–3698, Sept. 2013.

[35] C. Florian, F. Mastri, R. P. Paganelli, D. Masotti, and A. Costanzo, "Theoretical and numerical design of a wireless power transmission link with GaN-based transmitter and adaptive receiver," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 4, pp. 931–946, April 2014.

[36] A. Kurs, A. Karalis, R. Moffatt, J. D. Joannopoulos, P. Fisher, and M. Soljacic, "Wireless power transfer via strongly coupled magnetic resonances," *Science*, vol. 317, no. 5834, pp. 83–6, July 2007.

[37] K. Na, H. Jang, H. Ma, and F. Bien, "Tracking optimal efficiency of magnetic resonance wireless power transfer system for biomedical capsule endoscopy," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 1, pp. 295–304, Jan 2015.

[38] M. Kiani, U. M. Jow, and M. Ghovanloo, "Design and optimization of a 3-coil inductive link for efficient wireless power transmission," *IEEE Trans. Biomed. Circuits Syst.*, vol. 5, no. 6, pp. 579–591, Dec 2011.

[39] J. Kim, D.-H. Kim, J. Choi, K.-H. Kim, and Y.-J. Park, "Free-positioning wireless charging system for small electronic devices using a bowl-shaped transmitting coil," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 3, pp. 791–800, Mar. 2015.

[40] F. Zhang, S. A. Hackworth, W. Fu, C. Li, Z. Mao, and M. Sun, "Relay effect of wireless power transfer using strongly coupled magnetic resonances," *IEEE Trans. Magn.*, vol. 47, no. 5, pp. 1478–1481, May 2011.

[41] H. Lee, "An auto-reconfigurable 2 × /4× AC-DC regulator for wirelessly powered biomedical implants with 28% link efficiency enhancement," *IEEE Trans. Very Large Scale Integr.*, vol. 24, no. 4, pp. 1598–1602, April 2016.

[42] R. F. Xue, K. W. Cheng, and M. Je, "High-efficiency wireless power transfer for biomedical implants by optimal resonant load transformation," *IEEE Trans. Circuits Syst. I*, vol. 60, no. 4, pp. 867–874, April 2013.

[43] L. Chen, S. Liu, Y. C. Zhou, and T. J. Cui, "An optimizable circuit structure for high-efficiency wireless power transfer," *IEEE Trans. Ind. Electron.*, vol. 60, no. 1, pp. 339–349, Jan 2013.

[44] M. Zargham and P. G. Gulak, "Fully integrated on-chip coil in 0.13 *murmm* CMOS for wireless power transfer through biological media," *IEEE Trans. Biomed. Circuits Syst.*, vol. 9, no. 2, pp. 259–271, April 2015.

[45] A. Ibrahim and M. Kiani, "A figure-of-merit for design and optimization of inductive power transmission links for millimeter-sized biomedical implants," *IEEE Trans. Biomed. Circuits Syst.*, vol. 10, no. 6, pp. 1100–1111, 2016.

[46] P. Yeon, S. A. Mirbozorgi, and M. Ghovanloo, "Optimal design of a 3-coil inductive link for millimeter-sized biomedical implants," in *2016 IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Oct 2016, pp. 396–399.

[47] T. Sun, X. Xie, G. Li, Y. Gu, Y. Deng, and Z. Wang, "A two-hop wireless power transfer system with an efficiency-enhanced power receiver for motion-free capsule endoscopy inspection," *IEEE Trans. Biomed. Eng.*, vol. 59, no. 11, pp. 3247–3254, Nov 2012.

[48] M. Abbak and I. Tekin, "RFID coverage extension using microstrip-patch antenna array [wireless corner]," *IEEE Antennas Propag. Mag.*, vol. 51, no. 1, pp. 185–191, Feb. 2009.

[49] A. J. S. Boaventura and N. Carvalho, "Extending reading range of commercial RFID readers," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 1, pp. 633–640, Jan. 2013.

[50] ISO/IEC, "ISO 11785 radio frequency identification of animals – technical concept," vol. 65.040.99, 1996.

[51] S. V. Georgakopoulos and O. Jonah, "Optimized wireless power transfer to RFID sensors via magnetic resonance," in *IEEE Antennas Propag. Soc. Int. Symp.*, July 2011, pp. 1421–1424.

[52] O. Jonah, S. V. Georgakopoulos, and S. Yao, "Strongly coupled resonance magnetic for RFID applications," in *IEEE Antennas Propag. Soc. Int. Symp.*, July 2013, pp. 1110–1111.

[53] R. Goncalves, N. B. Carvalho, and P. Pinho, "Increasing the RFID readability range using wireless power transmission enhancements," in *Wireless Power Transf.*, May 2013, pp. 135–138.

[54] I. C. for Animal Recording (ICAR), "International agreement of recording practices," pp. 433–434, June 2008.

[55] M.-L. Kung and K.-H. Lin, "Enhanced analysis and design method of dual-band coil module for near-field wireless power transfer systems," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 3, pp. 821–832, Mar. 2015.

[56] U.-M. Jow and M. Ghovanloo, "Modeling and optimization of printed spiral coils in air, saline, and muscle tissue environments," *IEEE Trans. Biomed. Circuits Syst.*, vol. 3, no. 5, pp. 339–347, 2009.

[57] M. Zargham and P. G. Gulak, "Maximum achievable efficiency in near-field coupled power-transfer systems," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 3, pp. 228–245, 2012.

[58] T. Campi, S. Cruciani, F. Palandrani, V. De Santis, A. Hirata, and M. Feliziani, "Wireless power transfer charging system for AIMDs and pacemakers," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 633–642, 2016.

[59] C. Xiao, K. Wei, D. Cheng, and Y. Liu, "Wireless charging system considering eddy current in cardiac pacemaker shell: Theoretical modeling, experiments, and safety simulations," *IEEE Trans. Ind. Electron.*, vol. 64, no. 5, pp. 3978–3988, 2017.

[60] Y. Le Bihan, "Study on the transformer equivalent circuit of eddy current nondestructive evaluation," *NDT & E Int.*, vol. 36, no. 5, pp. 297–302, 2003.

[61] Y. K. Ramadass and A. P. Chandrakasan, "A battery-less thermoelectric energy harvesting interface circuit with 35 mv startup voltage," *IEEE J. Solid-State Circuits*, vol. 46, no. 1, pp. 333–341, Jan. 2011.

[62] J. Kimball, T. Flowers, and P. Chapman, "Low-input-voltage, low-power boost converter design issues," *IEEE Power Electron. Lett.*, vol. 2, no. 3, pp. 96–99, Sept. 2004.

[63] E. J. Carlson, K. Strunz, and B. P. Otis, "A 20 mV input boost converter with efficient digital control for thermoelectric energy harvesting," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 741–750, Apr. 2010.

[64] P.-H. Chen, K. Ishida, K. Ikeuchi, X. Zhang, K. Honda, Y. Okuma, Y. Ryu, M. Takamiya, and T. Sakurai, "A 95mV-startup step-up converter with v_{TH}-tuned oscillator by fixed-charge programming and capacitor pass-on scheme," in *IEEE Int. Solid-State Circuits Conf.* IEEE, Feb. 2011, pp. 216–218.

[65] J. Dickson, "On-chip high-voltage generation in MNOS integrated circuits using an improved voltage multiplier technique," *IEEE J. Solid-State Circuits*, vol. 11, no. 3, pp. 374–378, June 1976.

[66] Y.-C. Shih, T. Shen, and B. P. Otis, "A 2.3 μw wireless intraocular pressure/temperature monitor," *IEEE J. Solid-State Circuits*, vol. 46, no. 11, pp. 2592–2601, Nov. 2011.

[67] C. Ulaganathan, B. J. Blalock, J. Holleman, and C. L. Britton, "An ultra-low voltage self-startup charge pump for energy harvesting applications," in *IEEE Int. Midwest Symp. Circuits Syst.* IEEE, Aug. 2012, pp. 206–209.

[68] Jingjing Che, Chun Zhang, Zhongqi Liu, Ziqiang Wang, and Zhihua Wang, "Ultra-low-voltage low-power charge pump for solar energy harvesting systems," in *Intl. Conf. Commun., Circuits Syst.* IEEE, July 2009, pp. 674–677.

[69] Jieh-Tsorng Wu and Kuen-Long Chang, "MOS charge pumps for low-voltage operation," *IEEE J. Solid-State Circuits*, vol. 33, no. 4, pp. 592–597, Apr. 1998.

[70] P.-H. Chen, K. Ishida, Y. Okuma, Y. Ryu, M. Takamiya, and T. Sakurai, "A 120-mV input, fully integrated dual-mode charge pump in 65-nm CMOS

for thermoelectric energy harvester," in *Asia and South Pacific Design Automation Conf.* IEEE, Jan. 2012, pp. 469–470.

[71] I. Doms, P. Merken, C. Van Hoof, and R. P. Mertens, "Capacitive power management circuit for micropower thermoelectric generators with a 1.4 μa controller," *IEEE J. Solid-State Circuits*, vol. 44, no. 10, pp. 2824–2833, Oct. 2009.

[72] T. Myono, A. Uemoto, S. Kawai, E. Nishibe, S. Kikuchi, T. Iijima, and H. Kobayashi, "High-efficiency charge-pump circuits with large current output for mobile equipment applications," pp. 1602–1611, Oct. 2001.

[73] Y.-H. Chang and S.-Y. Kuo, "A gain/efficiency-improved serial-parallel switched-capacitor step-up DC–DC converter," *IEEE Trans. Circuits Syst. I*, vol. 60, no. 10, pp. 2799–2809, Oct. 2013.

[74] Y. Beck and S. Singer, "Capacitive transposed series-parallel topology with fine tuning capabilities," *IEEE Trans. Circuits Syst. I*, vol. 58, no. 1, pp. 51–61, Jan. 2011.

[75] R. Zhang, Z. Huang, and Y. Inoue, "A low breakdown-voltage charge pump based on cockcroft-walton structure," in *IEEE Int. Conf. ASIC.* IEEE, Oct. 2009, pp. 328–331.

[76] F. Ueno, T. Inoue, I. Oota, and I. Harada, "Emergency power supply for small computer systems," in *IEEE Int. Conf. Circuits Syst.* IEEE, 1991, pp. 1065–1068.

[77] J. Starzyk, "A DC-DC charge pump design based on voltage doublers," *IEEE Trans. Circuits Syst. I*, vol. 48, no. 3, pp. 350–359, Mar. 2001.

[78] P. Favrat, P. Deval, and M. Declercq, "A high-efficiency CMOS voltage doubler," *IEEE J. Solid-State Circuits*, vol. 33, no. 3, pp. 410–416, Mar. 1998.

[79] M. AbdElFattah, A. Mohieldin, A. Emira, and E. Sanchez-Sinencio, "A low-voltage charge pump for micro scale thermal energy harvesting," in *Int. Symp. Ind. Electron.* IEEE, June 2011, pp. 76–80.

[80] G. Palumbo and D. Pappalardo, "Charge pump circuits: An overview on design strategies and topologies," *IEEE Circuits Syst. Mag.*, vol. 10, no. 1, pp. 31–45, 2010.

[81] M. D. Seeman and S. R. Sanders, "Analysis and optimization of switched-capacitor DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 841–851, Mar. 2008.

[82] D. Wayne, "Low voltage low power design techniques for medical devices," in *Analog Circuit Design*, R. Plassche, W. Sansen, and J. Huijsing, Eds. Springer US, 1995, pp. 105–126.

[83] F. Silveira and D. Flandre, *Low Power Analog CMOS for Cardiac Pacemakers*. Boston, MA: Springer US, 2004.

[84] E. Klaassen, "Cardiac rhythm management ICs," in *Bio-Medical CMOS ICs*, H.-J. Yoo and C. van Hoof, Eds., 2011, pp. 421–451.

[85] Feng Su, Wing-Hung Ki, and Chi-Ying Tsui, "Gate control strategies for high efficiency charge pumps," in *IEEE Int. Symp. Circuits Syst.* IEEE, 2005, pp. 1907–1910.

[86] Chi-Chang Wang and Jiin-Chuan Wu, "Efficiency improvement in charge pump circuits," *IEEE J. Solid-State Circuits*, vol. 32, no. 6, pp. 852–860, June 1997.

[87] Feng Su and Wing-Hung Ki, "Component-efficient multiphase switched-capacitor DC–DC converter with configurable conversion ratios for LCD driver applications," *IEEE Trans. Circuits Syst. II*, vol. 55, no. 8, pp. 753–757, Aug. 2008.

[88] K. Eguchi, H. Zhu, F. Ueno, and T. Tabata, "Design of a step-up/step-down SC DC-DC converter with series-connected capacitors," in *IEEE Int. Symp. Circuits Syst.*, vol. 3. IEEE, 2003, pp. III–300–III–303.

[89] S. Abdelaziz, A. G. Radwan, A. Eladawy, A. N. Mohieldin, and A. M. Soliman, "A low start-up voltage charge pump for energy harvesting applications," in *Int. Conf. Engr. Technol.* IEEE, Oct. 2012, pp. 1–5.

[90] J. Ramirez-Angulo and M. Holmes, "Simple technique using local CMFB to enhance slew-rate and bandwidth of one-stage CMOS OP-AMPS," *Electron. Lett.*, vol. 38, no. 23, p. 1409, 2002.

[91] J. A. Galan, A. J. Lopez-Martn, R. G. Carvajal, J. Ramrez-Angulo, and C. Rubia-Marcos, "Super class-AB OTAs with adaptive biasing and dynamic output current scaling," *IEEE Trans. Circuits Syst. I*, vol. 54, no. 3, pp. 449–457, Mar. 2007.

[92] M. Degrauwe, J. Rijmenants, E. Vittoz, and H. De Man, "Adaptive biasing CMOS amplifiers," *IEEE J. Solid-State Circuits*, vol. 17, no. 3, pp. 522–528, June 1982.

[93] R. Klinke, B. Hosticka, and H. Pfleiderer, "A very-high slew-rate CMOS operational amplifier," *IEEE J. Solid-State Circuits*, vol. 24, no. 3, pp. 744–746, June 1989.

[94] A. Lopez-Martin, S. Baswa, J. Ramirez-Angulo, and R. Carvajal, "Low-voltage super class AB CMOS OTA cells with very high slew-rate and power efficiency," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1068–1077, May 2005.

[95] Ah-Reum Kim, Hyoung-Rae Kim, Yoon-Suk Park, Yoon-Kyung Choi, and Bai-Sun Kong, "Low-power class-AB CMOS OTA with high slew-rate," in *Int. SoC Design Conf.* IEEE, 2009, pp. 313–316.

[96] M. Pennisi, G. Palumbo, and R. G. Carvajal, "Analysis and comparison of class AB current mirror OTAs," *Analog. Integr. Circ. Sig. Process.*, vol. 67, no. 2, pp. 231–239, Oct. 2010.

[97] G. Palumbo, M. Pennisi, and R. G. Carvajal, "Figures of merit for class AB input stages," in *Eur. Conf. Circuit Theory Des.* IEEE, Aug. 2011, pp. 749–752.

[98] B. Huang, D. Chen, and L. Xu, "Slew-rate enhancement via excessive transient feedback," *Electron. Lett.*, vol. 49, no. 15, pp. 930–932, July 2013.

[99] Joongho Choi, Jinup Lim, and Cheng-Chew Lim, "A low-voltage operational amplifier with high slew-rate for sigma-delta modulators," in *IEEE Int. Symp. Circuits Syst.* IEEE, 2006, p. 4.

[100] S. Sutula, M. Dei, L. Terés, and F. Serra-Graells, "Class-AB single-stage opamp for low-power switched-capacitor circuits," in *IEEE Int. Symp. Circuits Syst.*, May 2015, pp. 2081–2084.

[101] R. Carvajal, J. Ramirez-Angulo, A. Lopez-Martin, A. Torralba, J. Galan, A. Carlosena, and F. Chavero, "The flipped voltage follower: a useful cell for low-voltage low-power circuit design," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 7, pp. 1276–1291, July 2005.

[102] L. Cheng, W. H. Ki, Y. Lu, and T. S. Yim, "Adaptive on/off delay-compensated active rectifiers for wireless power transfer systems," *IEEE J. Solid-State Circuits*, vol. 51, no. 3, pp. 712–723, March 2016.

[103] C. Huang, T. Kawajiri, and H. Ishikuro, "A near-optimum 13.56 MHz CMOS active rectifier with circuit-delay real-time calibrations for high-current biomedical implants," *IEEE J. Solid-State Circuits*, vol. 51, no. 8, pp. 1797–1809, 2016.

[104] J. Fuh, S. K. Hsieh, F. B. Yang, and P. H. Chen, "A 13.56MHz power-efficient active rectifier with digital offset compensation for implantable medical devices," in *IEEE Wireless Power Transf. Conf.*, 2016, pp. 1–3.

[105] Z. Xue, D. Li, W. Gou, L. Zhang, S. Fan, and L. Geng, "A delay time controlled active rectifier with 95.3% peak efficiency for wireless power transmission systems," in *IEEE Int. Symp. Circuits Syst.*, 2017, pp. 1–4.

[106] A. Bagheri, M. T. Salam, J. L. P. Velazquez, and R. Genov, "56-channel direct-coupled chopper-stabilized EEG monitoring ASIC with digitally-assisted offset correction at the folding nodes," in *IEEE Biomed. Circuits Syst. Conf.*, Oct 2014, pp. 659–662.

[107] Z. Xue, S. Fan, Z. Guo, and L. Geng, "Low power on/off control method for active-diode applied in wireless power transmission," in *IEEE Wireless Power Transf. Conf.* IEEE, 2018, pp. 1–3.

[108] G. Lee, B. H. Waters, Y. G. Shin, J. R. Smith, and W. S. Park, "A reconfigurable resonant coil for range adaptation wireless power transfer," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 2, pp. 624–632, Feb. 2016.

[109] H. M. Lee and M. Ghovanloo, "An adaptive reconfigurable active voltage doubler/rectifier for extended-range inductive power transmission," *IEEE Trans. Circuits Syst. II*, vol. 59, no. 8, pp. 481–485, Aug 2012.

[110] X. Li, C. Y. Tsui, and W. H. Ki, "A 13.56 MHz wireless power transfer system with reconfigurable resonant regulating rectifier and wireless power control for implantable medical devices," *IEEE J. Solid-State Circuits*, vol. 50, no. 4, pp. 978–989, Apr. 2015.

[111] N. Inagaki, "Theory of image impedance matching for inductively coupled power transfer systems," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 4, pp. 901–908, April 2014.

[112] M. Liu, S. Liu, and C. Ma, "A high-efficiency/output power and low-noise megahertz wireless power transfer system over a wide range of mutual inductance," *IEEE Trans. Microw. Theory Techn.*, vol. PP, no. 99, pp. 1–9, 2017.

[113] Y. Han and D. Perreault, "Analysis and design of high efficiency matching networks," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1484–1491, Sept. 2006.

[114] Y. Narusue, Y. Kawahara, and T. Asami, "Maximizing the efficiency of wireless power transfer with a receiver-side switching voltage regulator," *Wireless Power Transf.*, pp. 1–13, feb 2017.

[115] T. H. Lee, *Planar Microwave Engineering: A Practical Guide to Theory, Measurement, and Circuits.* Cambridge University Press, 2004, vol. 1.

[116] M. Kiani, B. Lee, P. Yeon, and M. Ghovanloo, "A power-management ASIC with Q-modulation capability for efficient inductive power transmission," in *IEEE Int. Solid-State Circuits Conf.*, Feb. 2015, pp. 1–3.

[117] B. Lee, P. Yeon, and M. Ghovanloo, "A multicycle Q-modulation for dynamic optimization of inductive links," *IEEE Trans. Ind. Electron.*, vol. 63, no. 8, pp. 5091–5100, Aug. 2016.

[118] J. Tian and A. P. Hu, "Stabilising the output voltage of wireless power pickup through parallel tuned dc-voltage controlled variable capacitor," *Electron. Lett.*, vol. 52, no. 9, pp. 758–759, 2016.

[119] P. Si, A. P. Hu, S. Malpas, and D. Budgett, "A frequency control method for regulating wireless power to implantable devices," *IEEE Trans. Biomed. Circuits Syst.*, vol. 2, no. 1, pp. 22–29, Mar. 2008.

[120] G. Wang, W. Liu, M. Sivaprakasam, and G. A. Kendir, "Design and analysis of an adaptive transcutaneous power telemetry for biomedical implants," *IEEE Trans. Circuits Syst. I*, vol. 52, no. 10, pp. 2109–2117, Oct. 2005.

[121] T. D. Yeo, D. Kwon, S. T. Khang, and J. W. Yu, "Design of maximum efficiency tracking control scheme for closed-loop wireless power charging system employing series resonant tank," *IEEE Trans. Power Electron.*, vol. 32, no. 1, pp. 471–478, Jan. 2017.

[122] M. Fu, H. Yin, M. Liu, and C. Ma, "Loading and power control for a high-efficiency class E PA-driven megahertz WPT system," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 6867–6876, Nov 2016.

[123] H. Li, J. Li, K. Wang, W. Chen, and X. Yang, "A maximum efficiency point tracking control scheme for wireless power transfer systems using magnetic resonant coupling," *IEEE Trans. Power Electron.*, vol. 30, no. 7, pp. 3998–4008, July 2015.

[124] H. Li, Y. Tang, K. Wang, and X. Yang, "Analysis and control of post regulation of wireless power transfer systems," in *IEEE Annu. Southern Power Electron. Conf.*, Dec 2016, pp. 1–5.

[125] J.-S. Choi and K. Lee, "Design of CMOS tapered buffer for minimum power-delay product," *IEEE J. Solid-State Circuits*, vol. 29, no. 9, pp. 1142–1145, Sep 1994.

[126] G. Bawa and M. Ghovanloo, "Analysis, design, and implementation of a high-efficiency full-wave rectifier in standard CMOS technology," *Analog. Integr. Circ. Sig. Process.*, vol. 60, no. 1, pp. 71–81, 2009.

[127] S. Stoecklin, T. Volk, A. Yousaf, and L. Reindl, "A maximum efficiency point tracking system for wireless powering of biomedical implants," *Procedia Engineering*, vol. 120, pp. 451 – 454, 2015.

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Glossary

$D_{TX\text{-}RX}$ Distance between the transmitter and the receiver.
L_{RX} Receiver self-inductance.
L_{TX} Transmitter self-inductance.
$M_{TX\text{-}RX}$ Mutual inductance between the transmitter and the receiver.
P_L Power delivered to the load (dc), see Fig. 1.2.
P_{MN} Output power of the receiver coil, see Fig. 1.2.
P_S Output power of the source in the transmitter, see Fig. 1.2.
P_{TX} Output power of the transmitter driver circuit, see Fig. 1.2.
$P_{dc\text{-}dc}$ Receiver dc-dc converter input power.
P_{rect} Receiver rectifier input power.
Q_L Load quality factor, $Q_L{=}wL_{RX}/\mathrm{Re}\{Z_{MN}\}$.
$Q_{RX\text{-}L}$ RX equivalent quality factor, $Q_{RX\text{-}L}{=}Q_{RX}Q_L/(Q_{RX}{+}Q_L){=}wL_{RX}/(R_{RX}{+}\mathrm{Re}\{Z_{MN}\})$.
Q_{RX} Receiver quality factor $= \frac{wL_{RX}}{R_{RX}}$.
Q_{TX} Transmitter quality factor $= \frac{wL_{TX}}{R_{TX}}$.
R_L Load resistance, it models the input resistance of the device being powered.
R_{RX} Receiver coil parasitic series resistance.
R_{TX} Transmitter coil parasitic series resistance.
$R_{dc\text{-}dc}$ Receiver dc-dc input resistance.
R_{rect} Rectifier input resistance, it is equal to the MN load resistance. See Fig. 3.37.
V_L Load voltage, see Fig. 1.2.
V_S Voltage of the power source in the transmitter, see Fig. 1.2.
V_{rect} Rectifier output voltage, see Fig. 1.2. It is equal to V_L if there is no dc-dc converter.
$Z_{MN_{opt\text{-}V}}$ Optimum value for Z_{MN} that maximizes the output power P_L.
$Z_{MN_{opt\text{-}\eta}}$ Optimum value for Z_{MN} that maximizes the link efficiency η_{Link}.
$Z_{MN_{opt}}$ Optimum value of Z_{MN}, it refers to both $Z_{MN_{opt\text{-}\eta}}$ and $Z_{MN_{opt\text{-}V}}$.
Z_{MN} Load impedance of the receiver coil RX, see Fig. 1.2.
η_{Driver} Transmitter driver efficiency, see Fig. 1.2.
η_{Link} Inductive link efficiency, see Fig. 1.2.
η_{MN} Receiver MN efficiency, see Fig. 4.1.
η_{RX} Receiver circuit efficiency, see Fig. 1.2 ($\eta_{RX} = \eta_{MN}.\eta_{rect}.\eta_{dc\text{-}dc}$).
η_{TOT} Total system efficiency $\eta_{TOT} = P_L/P_S$, see Fig. 1.2 ($\eta_{TOT} = \eta_{Driver}.\eta_{Link}.\eta_{RX}$).
$\eta_{ac\text{-}dc}$ Receiver ac-dc converter efficiency, see Fig. 4.1 ($\eta_{ac\text{-}dc} = \eta_{rect}.\eta_{dc\text{-}dc}$).
$\eta_{dc\text{-}dc}$ Receiver dc-dc converter efficiency, see Fig. 4.1.
η_{rect} Receiver rectifier efficiency, see Fig. 4.1.

f Carrier frequency of the power transfer.
$k_{TX\text{-}RX}$ Coupling factor between the transmitter and the receiver.
w Carrier angular frequency of the power transfer, $w = 2\pi f$.

Acronyms

AIMD Active Implantable Medical Device.

CMOS Complementary Metal Oxide Semiconductor.
CP Charge Pump.
CST Simulation software CST Studio Suite ®.

FSK Frequency Shift Keying.

IPT Inductive Power Transfer.

LDO Low-Dropout Regulator.

MDs Mobile Devices.
MEP Maximum Efficiency Point.
MEPT Maximum Efficiency Point Tracking.
MN Matching Network.

OTA Operational Transconductance Amplifier.

PCE Power Conversion Efficiency.

RFID Radio-Frequency Identification.
RLT Reflected Load Theory.
RX Receiver.
RX-circuit Receiver Circuit.
RX-MN Receiver Matching Network.

TX Transmitter.

VCR Voltage Conversion Ratio.

WCR Worst Case Resistivity.
WPT Wireless Power Transfer.

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