Estimation and Control Techniques in Power Converters

by

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Abstract

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Doctor of Philosophy in Engineering - Electrical Engineering and Computer Science

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This thesis develops estimation and control techniques in power converters. The target applications are voltage regulators for modern microprocessors (VRM) and distributed DC power systems (DPS).

A method for the on-line calibration of a circuit board trace resistance at the output of a buck converter is described. This method is applied to obtain an accurate and high-bandwidth measurement of the load current in the VRM applications, thus enabling an accurate DC load-line regulation as well as a fast transient response. Experimental results show an accuracy well within the tolerance band of this application, and exceeding all other popular methods.

A method for estimating the phase current unbalance in a multi-phase buck converter is presented. The method uses the information contained in the voltage drop at the input capacitor's ESR to estimate the average current in each phase. The method

can be implemented with a low-rate down-sampling A/D converter and is not computationally intensive. Experimental results are presented, showing good agreement between the estimates and the measured values.

An online adaptation method of the gain of an output current feedforward path in VRM applications is developed. The feedforward path can improve substantially the converter's response to load transients but it depends on parameters of the power train that are not known with precision. By analyzing the error voltage and finding its correlation with the parameter error, a gradient algorithm is derived that makes the latter vanish. Experimental results show a substantial improvement of the transient response to a load current step in a prototype VRM.

Impedance interactions between interconnected power subsystems are analyzed. Typical examples of these interconnections are a power converter with a dynamic load, a power converter with an input line filter, power converters connected in parallel or cascade, and combinations of the above. A survey of the most relevant results in this area is presented together with detailed examples. Fundamental limits on the performance of the interconnected systems are exposed and a system-level design approach is proposed and corroborated with simulations.

Professor Seth R. Sanders
Dissertation Committee Chair

To Sônia, todo o amor que houver nesta vida.

To my parents, with love and gratitude.

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Gabriel Eirea

Berkeley, August 2006

Part I

Estimation Techniques in VRM

Applications

Chapter 1

Introduction

1.1 VRM and DPS applications

For over 40 years the semiconductor industry has been evolving steadily following Moore's Law, which states that the number of transistors on a chip roughly doubles every two years [2]. The trend was first observed in 1965 and it is predicted to continue at least until 2020 [3]. The implications of this trend are striking. As the size of transistors decreases, their speed increases and more functionality can be incorporated on a single chip at a reduced cost. As a consequence, digital integrated circuits (ICs) became ubiquitous in our society and have improved dramatically our standard of living. Semiconductors have become a $200 billion industry and the foundation for the trillion-dollar electronics industry [2].

At the forefront of this revolution are the highly integrated digital processing ICs, especially general-purpose microprocessors. These devices offer a tremendous computing power at a low cost. Communication systems, data servers, desktop computers at home and the office, and portable devices are some of the applications powered by microprocessors that define the landscape of modern life.

The increasing number of transistors and speed of operation creates an increase in the power consumption of the devices. As size is also reduced, the ability to dissipate the heat generated in the IC is diminished. Consequently, temperatures inside the chip can get close to the thermal limit of silicon. This is one of the reasons why power consumption needs to be reduced. Another important reason is the growing concern on the efficient use of energy resources in the planet, with initiatives like "Energy Star" in the United States [4].

The power consumed by a digital IC can be estimated as

$$P = knCV^2f \tag{1.1}$$

where k is an utilization factor, n is the number of transistors, C is the capacitance of a transistor, V is the supply voltage, and f is the frequency of operation. The values of n and f are continuously increasing in order to offer more computing power. At the present, modern microprocessors have hundreds of millions of transistors and clock frequencies of several Gigahertz, and the trend is to increase these parameters [1]. Since C is mostly constant for a given technology, the two variables that can be

used to reduce the power consumption are k and V. Effectively, the voltage V has been gradually decreasing from $5V$ to below $1V$ over the years. Probably the biggest improvement in power reduction for microprocessors comes from power management techniques that allow turning off parts of the circuit that are not being used, therefore reducing the factor k. However, this power reduction technique creates large and fast current transients when the microprocessor sends to sleep or awakes large logic blocks. Some of these trends are shown in Fig. 1.1 [1].

The circuit that delivers the power to the microprocessor is usually called a Voltage Regulator Module (VRM). The preferred architecture for this power converter is the multiphase buck converter with synchronous rectification (Fig. 1.2). This architecture reduces the ripple both of the output voltage and the input current, allowing for smaller filter components. Since the load is shared by the different phases, the maximum rating of the semiconductors and inductors is decreased, becoming a cost-efficient solution for high-current applications such as VRM [5].

A technique called Adaptive Voltage Positioning (AVP) was adopted in order to reduce the number of output capacitors by allowing the output impedance of the converter to be different from zero [6]. This technique requires that the output voltage follow a "load-line" that depends on the output current; the slope of the load-line is typically around $1m\Omega$. The output voltage specification is completed with the definition of a tolerance band (TOB) that includes the tolerance both for
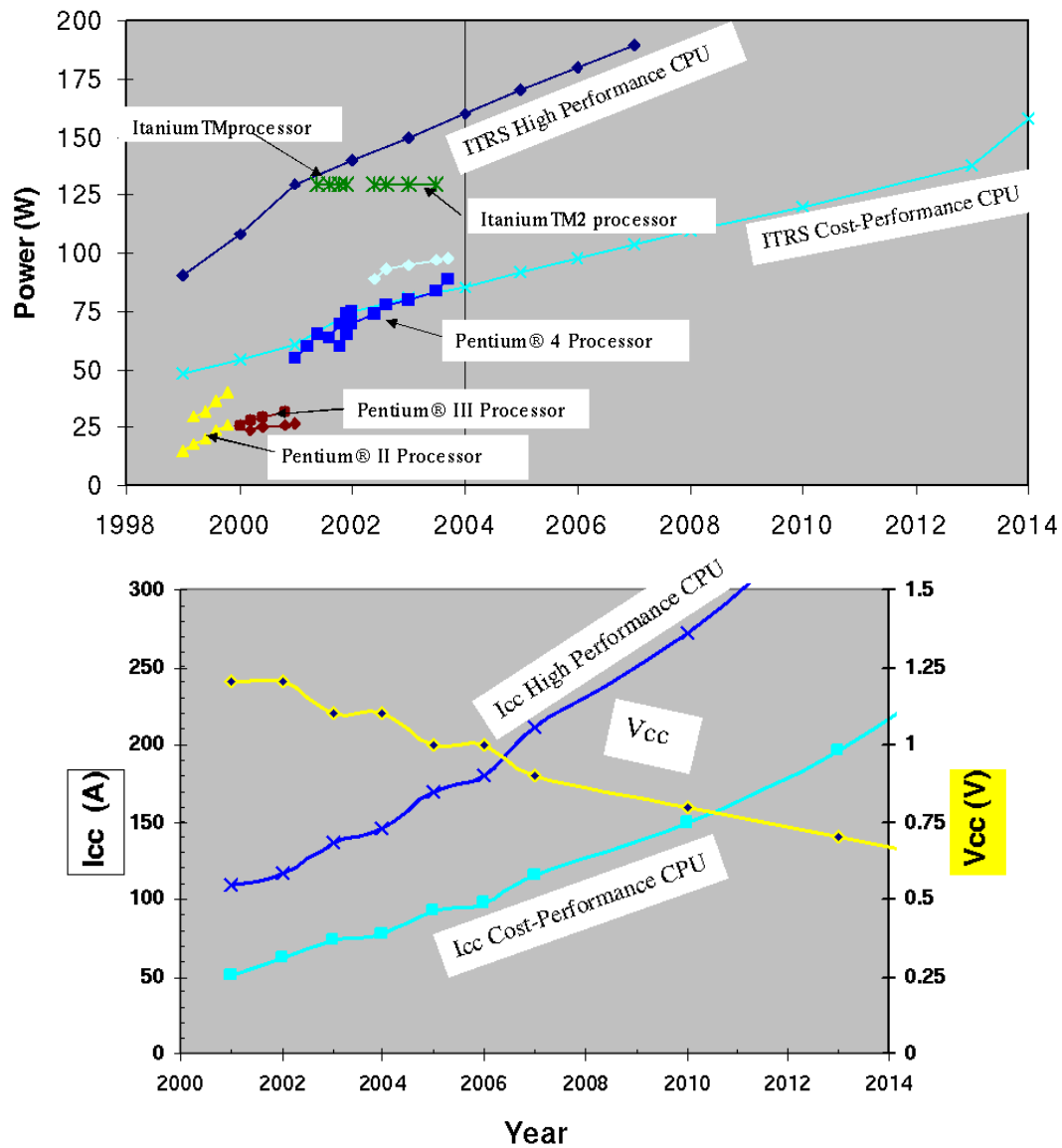
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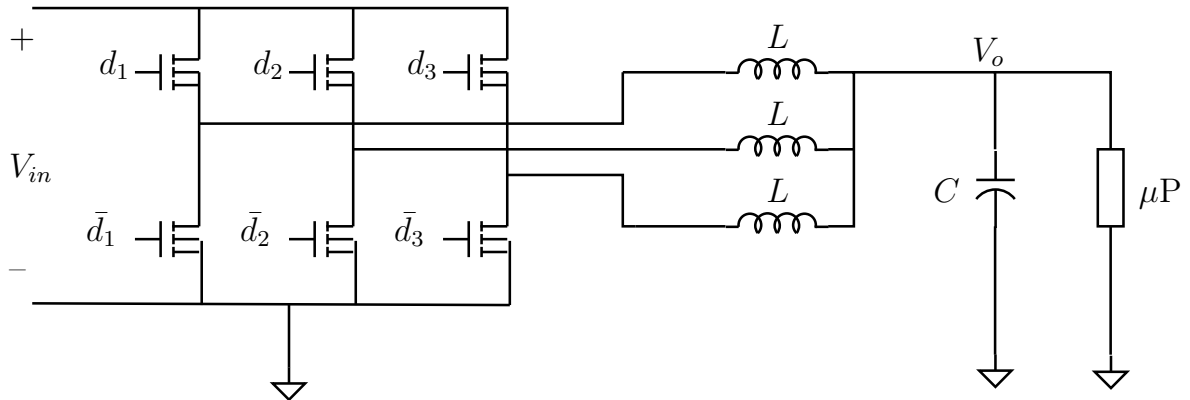
Figure 1.2: Multiphase buck converter with synchronous rectification. Three-phase example.

steady-state variations of the voltage (due to ripple or offset voltages) and dynamic variations during load current transients. This is illustrated in Fig. 1.3.

The state of the art specifications for VRM systems is summarized in Table 1.1 [7]. The trend in VRM specifications is to have larger load currents, faster and larger load transients, lower output voltage, and tighter tolerances (Fig. 1.4). The challenge is to comply with these specifications, while at the same time meeting the market requirements in terms of cost, efficiency, high power density, and low profile.

A typical motherboard is shown in Fig. 1.5 with the VRM area outlined. While most of the components in a motherboard are reduced in size and integrated, the VRM has not been able to reduce its size and uses a larger proportion of the real estate. It is estimated that up to 30% of the motherboard area is used by power delivery circuits, mostly by the VRM [8]. The same source cites the trend towards more compact form factors, making the size problem a very important one.
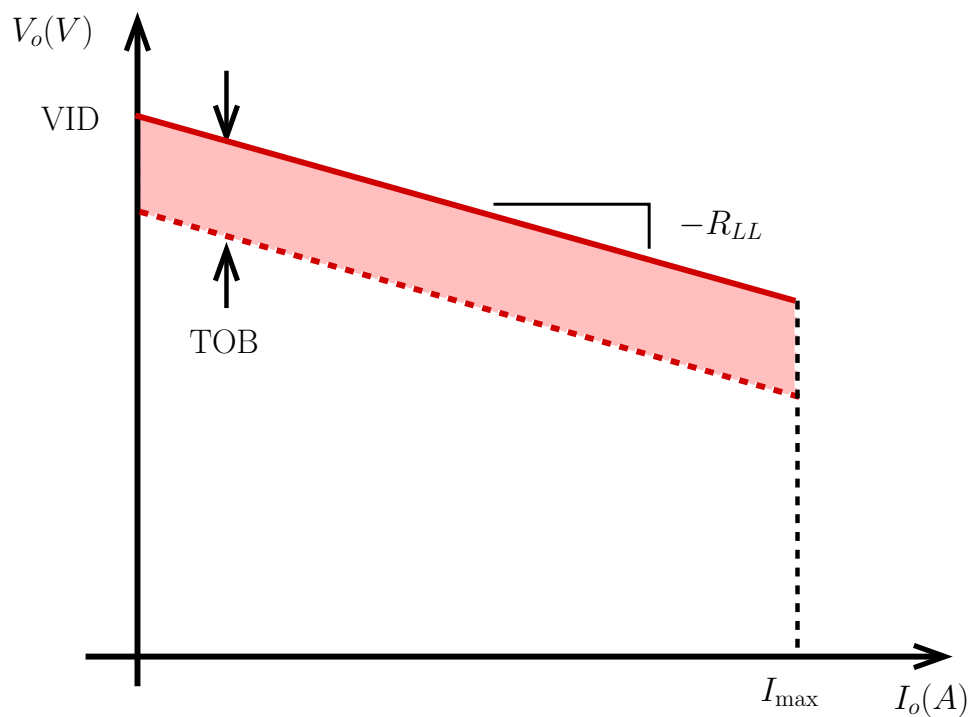
Figure 1.3: Adaptive Voltage Positioning.

Table 1.1: Summary of VRM state of the art.

Multiphase buck converter with synchronous rectification	
Automatic Voltage Positioning (load-line)	
Input voltage	$12V$
Dynamic output voltage reference	$0.8 - 1.6V$
Tolerance band	$40mV$
Output current	$1 - 120A$
Output current slew-rate	up to $900A/\mu s$
Load-line impedance	$1.25m\Omega$
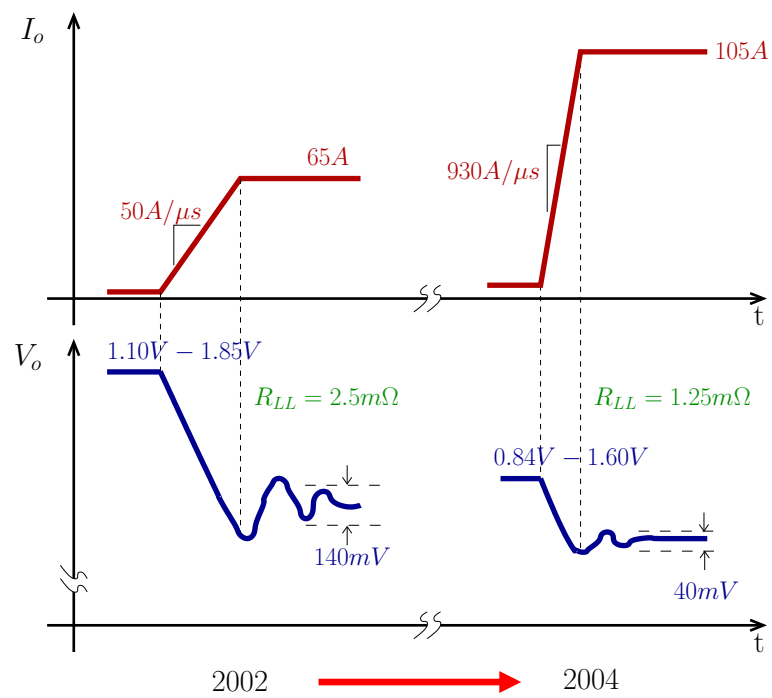
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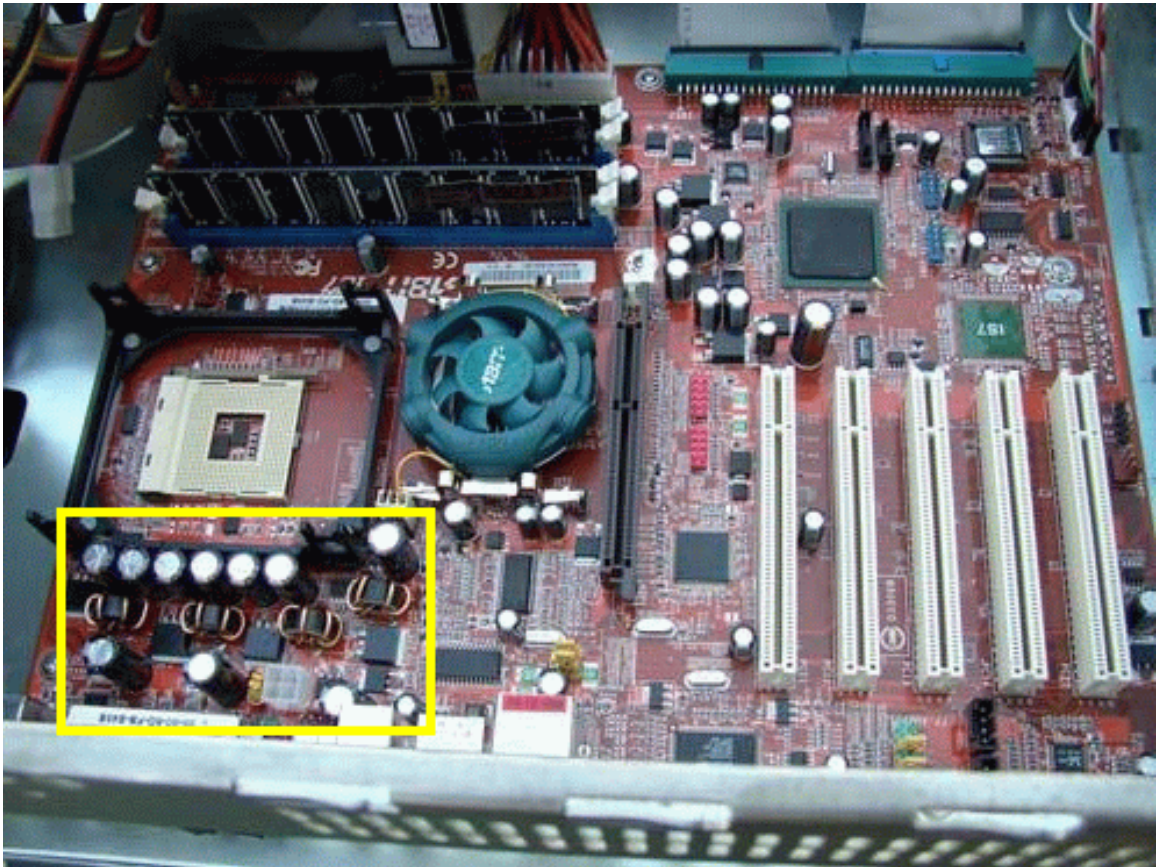
Figure 1.5: Motherboard Abit IS7 with VRM controller Intersil HIP6301CB. (Extracted from http://www.lostcircuits.com)

The output capacitors account for a large part of the cost and size of the VRM. Most of the research efforts and commercial developments target the reduction of the output capacitance. This is one of the reasons why AVP and the multiphase buck architecture were introduced, besides having other benefits. Control strategies can also help reduce the output capacitance, such as the case of output current feedforward [9] that motivates most of the work in this thesis.

Delivering power to big and complex digital ICs is becoming a challenge not only for microprocessors, but also graphic processors, memories, and others. In data centers and communication systems, power has to be delivered to racks and boards in a room. This creates the need to a careful design of the whole power delivery architecture. DC Distributed Power Systems (DPS) are increasingly common and pose new challenges in terms of stability and performance of the interconnected sources, filters, power converters, and loads [10]. The most used DPS architecture is the Intermediate Bus Architecture (IBA), in which nonisolated Point Of Load (POL) converters provide local voltage regulation from a mildly regulated intermediate voltage.

Analysts see increasing price pressures in the DC/DC market, slowing down the growth rates. Commoditization of some market segments, most notably PCs and related products, lead to this phenomenon. Although the volume of sales is expected to continue to grow steadily, the DC/DC converter market annual growth is estimated at 5.7% [11]. The power management IC segment was a $5 billion market in 2002

and is estimated to be around \$8 billion today [12].

The subject of this thesis is the improvement of control strategies for power delivery circuits in VRM and DPS applications, which lie at the base of the Information Technology revolution.

1.2   Thesis overview

This thesis is organized in two parts. In Part I, three contributions in the area of control of DC/DC converters, in particular VRM applications, are presented.

The subject of Chapter 2 is an output current sensing method based on the on-line calibration of parasitic resistance elements on the power train. This method allows for an accurate, efficient, and low cost sensing of the output current in high-current buck converters. In VRM applications, this enables not only load-line tracking but also output current feedforward for improved transient response.

In Chapter 3, a current unbalance estimation algorithm for multiphase buck converters is presented. The algorithm requires sensing a single voltage and processing the information digitally. The processing cost is low, since it involves operations that can be scheduled over a relatively long time interval.

Chapter 4 presents an adaptation method to tune the output current feedforward path in a VRM application. Transient response to fast and large current variations can be improved with output current feedforward, as long as the parameters match

those of the plant. This adaptive control method tunes the critical parameter in the feedforward path so that the voltage error during transients is minimized.

These three contributions are tightly related and together can be applied to a VRM system for improved performance. However, each technique could be applied independently on this or other applications. The methods described in Chapters 2 and 3 comprise a total current sensing solution for VRM applications, or other low voltage, high-current applications. The method described in Chapter 4 assumes that the output current information is available by some method, for example using the method described in Chapter 2, but other methods could be used.

In Part II, theoretical aspects of the interconnection of power converters are analyzed. Chapter 5 presents an overview of the problem of impedance interactions between a power converter and an input filter, or between any interconnection between power converters. This problem is relevant due to the prevailing use of DC Distributed Power Systems for power distribution at all levels: at a room level in data centers or communication systems, at a motherboard level in computing applications, and even at a chip level in complex integrated circuits. With a comprehensive literature review and numerous examples, this chapter is intended as a survey of the most relevant results in this area.

In Chapter 6 the fundamental limits of performance in interconnected power systems are explored, and an alternative solution for the specific case of a power converter

with an undamped input filter is proposed. This solution is intended to serve as an example of a design approach that is based on a system-level view of the problem. By designing properly the impedances of the various interconnected subsystems, the fundamental limits of performance can be avoided without resorting to the prevailing design method of adding capacitors and damping the filters, which adds cost, size, and weight to the system.

Finally, the main contributions of this thesis are outlined in Chapter 7, together with suggestions for future research topics.

Chapter 2

Output Current Estimation

In this chapter, a method for the on-line calibration of a circuit board trace resistance at the output of a buck converter is described. The input current is measured with a precision resistor and processed to obtain a DC reference for the output current. The voltage drop across a trace resistance at the output is amplified with a gain that is adaptively adjusted to match the DC reference. This method is applied to obtain an accurate and high-bandwidth measurement of the load current in the modern microprocessor voltage regulator application (VRM), thus enabling an accurate DC load-line regulation as well as a fast transient response. Experimental results show an accuracy well within the tolerance band of this application, and exceeding all other popular methods.

Table 2.1: Popular current sensing methods.

Method	Accuracy	Efficiency	Cost	Comments
Hall effect	high	high	very high	not used
Sense resistor at the output	high	very low	medium	not used
Sense resistor at the input	medium	medium	medium	not used
R_{DS}	low	high	low	used for balancing
Inductor sensing	medium	high	low	preferred solution
SENSEFET	medium	high	high	special MOSFETs

2.1 Introduction

Voltage regulators for modern microprocessors (VRMs) pose unprecedented de-
mands on DC-DC power converters, in terms of regulation, bandwidth, and cost [7].
Adaptive Voltage Positioning (AVP), also known as load-line regulation, was adopted
as an effective technique to reduce the amount of capacitance at the output [6]. This
technique requires the output voltage to change with the load current, as if the out-
put impedance of the power converter were a resistor of small value (around $1m\Omega$).
The controller can be designed to make the effective closed-loop output impedance
resistive, or to meet another desired specification, over a wide frequency range, by
processing the output current information [6].

For this reason, and due to the tight regulation window required by the applica-
tion, a precise and high-bandwidth measure of the output current is needed. Existing
current-sensing techniques are shown and compared in Table 2.1 [13, 14].

Other methods have been proposed but are not used commercially. An on-line

calibration method for MOSFET R_{DS} sensing that requires additional power train components, was described in [15]. An observer-based approach requiring intensive numerical processing was reported in [16].

For efficiency, cost, and relative accuracy, inductor sensing is the preferred method at the present time [7]. The method is illustrated in Fig. 2.1. The relationship between the capacitor voltage and the inductor current in the frequency domain is:

$$I_L = \frac{V_{sw} - V_o}{Ls + R_{dcr}} = \frac{1}{R_{dcr}} \cdot \frac{V_{sw} - V_o}{\frac{L}{R_{dcr}}s + 1} \tag{2.1}$$

$$V_c = \frac{V_{sw} - V_o}{RCs + 1}. \tag{2.2}$$

If $RC = \frac{L}{R_{dcr}}$, then

$$V_c = R_{dcr} I_L \tag{2.3}$$

It can be appreciated that this method has the disadvantage that both the effective series resistance R_{dcr} and the L/R time constant of the inductor need to be known and tracked as they change with temperature.

Most of the methods described above sense the inductor current, which has the same DC value as the output current, and tracks it well up to the closed-loop bandwidth of the converter. In designs with electrolytic capacitors, the output capacitor's ESR is chosen to be equal to the desired output impedance, as given by the load-line specification. This allows the converter to follow the load-line ideally at an arbitrary high bandwidth [6]. However, if ceramic capacitors are used the ESR is substantially
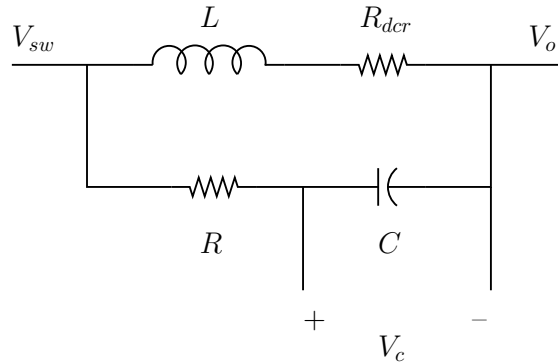
Figure 2.1: Inductor sensing.

lower than the load-line impedance rendering the previous design method impracti-

cal. The concept of generalized load-line was introduced in [9] as a practical design

objective for VRM systems with ceramic capacitors. The bandwidth in such a system

is given by the time constant $\tau = R_{LL}C_o$ where R_{LL} is the desired load-line and C_o

is the output capacitor value. In some cases it could be very difficult to follow the

load-line over this frequency range, especially as C_o is decreased to reduce costs. In

order to enhance load-line tracking without pushing the feedback bandwidth close to

instability, output current feedforward was proposed [9]. In this case, the inductor

current information is not useful and the load current must be sensed. In [9] the

authors used inductor sensing together with an analogous technique to sense the out-

put capacitor current, and combined both to obtain the output current. Thus, the

method used poses the same practical challenges as inductor sensing.

The objectives of this research is to develop a current sensing method with the

following characteristics:

1. **Output current sensing.** By sensing the output current, a high bandwidth signal is obtained that can be used in an output current feedforward scheme to improve the transient response of the system.

2. **Accuracy of 1%.** It is estimated that inductor sensing accuracy is about 8%. This means that at $100A$ in a $1m\Omega$ load-line the voltage error is $\pm 8mV$. As a consequence, the designer has to assign an inductor sensing error budget of $16mV$ out of a $40mV$ tolerance band (TOB). With a more accurate sensing method the error budget could be reduced to $2mV$, thus relaxing the constraints for other circuit components.

3. **Efficient.** In high-current applications such as in the VRM, the designer cannot afford to put additional components in the power train.

4. **Low cost.** This is always a desired objective, especially in a commoditized applications such as the VRM. In practice this means, among other things: reduced bill of materials (BOM), low pin-count, little extra IC complexity.

In this chapter, a method that approaches these ideal conditions is presented. The method senses the output current by using the output trace resistance (or any parasitic resistance at the output of the converter) as a sensing element. The value of the trace resistance is calibrated on-line by a slow estimation loop. The estimation
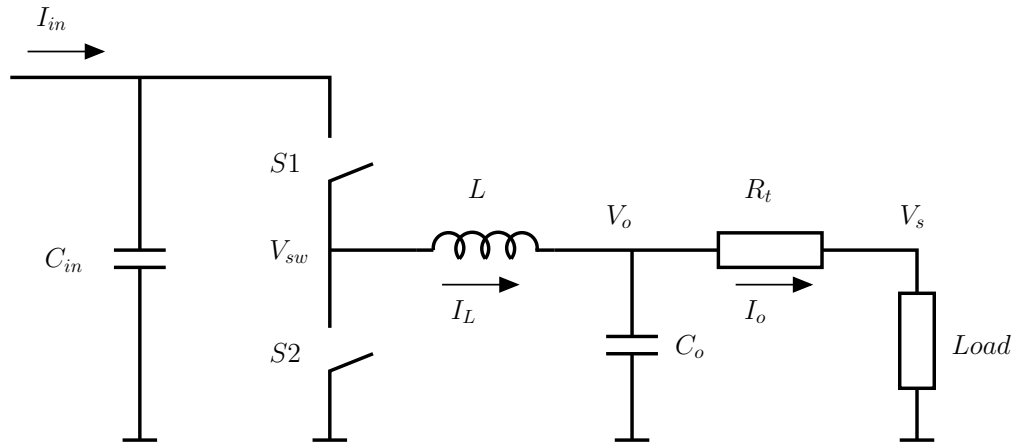
Figure 2.2: Buck converter

algorithm is based on the DC correspondence between the output current and the input current. The latter is accurately measured with a sense resistor and used as a reference. This method can achieve high-accuracy and high-bandwidth measurement of the output current with a small efficiency penalty due to the input-side resistor. Further, the measured input current may be useful for control purposes.

2.2 Method description

Fig. 2.2 shows a buck converter. The output trace resistance is shown explicitly as element R_t. The input current I_{in} is measured by placing a sense resistor before the input capacitor. Usually an inductor is located at this place as a choke, so this current is mostly DC and free of high frequency noise. In steady-state, the average current through the input capacitor is zero, so the average current through the high-

side switch is being effectively measured. This current can be ideally expressed as uI_L, where $I_L(t)$ is the inductor current, and

$$u(t) = \begin{cases} 1, & \text{if S1 is ON} \\ 0, & \text{if S1 is OFF.} \end{cases} \qquad (2.4)$$

It can also be argued that the average current through the output capacitor is zero, so the average inductor current is equal to the average output current. Then,

$$\langle I_{in} \rangle = \langle uI_L \rangle \qquad (2.5)$$

$$\langle I_L \rangle = \langle I_o \rangle \qquad (2.6)$$

where $\langle \bullet \rangle$ indicates the DC or average component of the signal. In steady-state and in continuous conduction mode (CCM), it holds that

$$\langle uI_L \rangle = \langle uI_o \rangle \qquad (2.7)$$

as illustrated in Fig. 2.3. Therefore, it can be concluded that

$$\langle I_{in} \rangle = \langle uI_o \rangle. \qquad (2.8)$$

This relationship establishes the basis of the on-line calibration algorithm. In Fig. 2.4 a block diagram of the estimation loop is shown. The current sense amplifier (CSA) measures the voltage drop on the trace resistance $(V_o - V_s)$. Its output is the estimated current $\hat{I}_o$. This value is multiplied by the function $u(t)$, simulating the operation of the top switch. The difference between this signal and the input
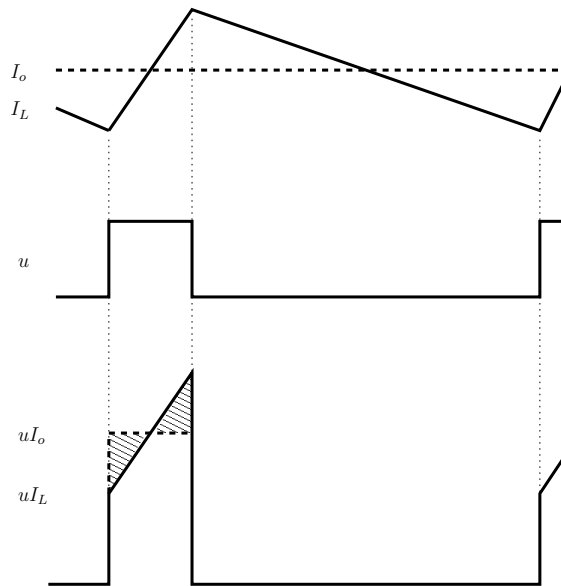
Figure 2.3: In steady-state and CCM, $\langle uI_L \rangle = \langle uI_o \rangle$ because the areas of the shaded triangles are equal.

current I_{in} is sent to the input of an integrator, whose output sets the gain of the CSA, therefore closing the loop and forcing the integrator to converge to the correct gain. If the gain is too low, the input of the integrator will be positive and the gain will increase, and *vice versa*. The loop will converge to set the gain such that the condition expressed in (2.8) is met, therefore achieving the desired result $\hat{I}_o = I_o$. The bandwidth of this adaptive tuning loop should be slow enough as to average-out the effect of switching and load transients, but fast enough to allow for tracking temperature changes. This gives a practical criteria to set the gain of the loop. A low bandwidth is also needed to guarantee the stability of the adaptive loop.

Notice that, although the adaptation loop is slow, the actual measurement of the
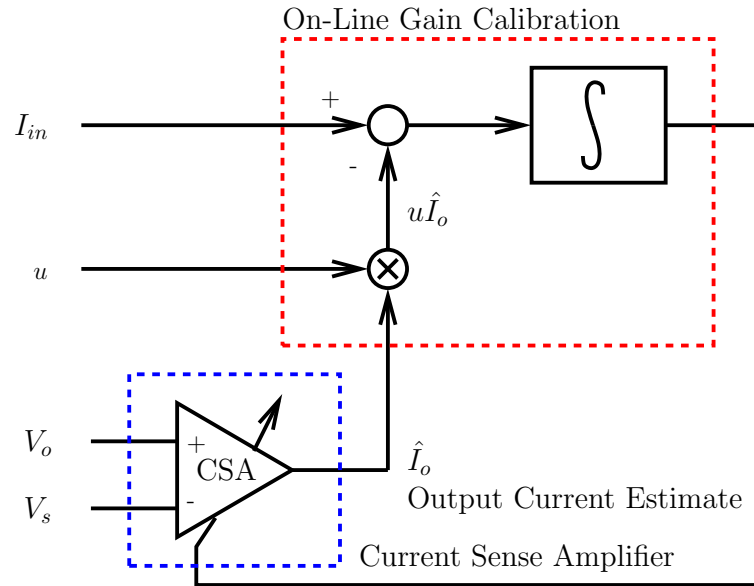
Figure 2.4: Current sense amplifier with gain estimation loop.

output current is high-bandwidth, because it is given by the voltage drop $V_o - V_s$ across the passive trace resistance amplified with a variable gain amplifier.

The magnitude of the differential voltage $V_o - V_s$ has to be such that the signal can be resolved. This means that there is a trade-off between the signal amplitude and the power loss due to the trace resistance. This trade-off results in the selection of a specific PCB layout and impacts the characteristics of the CSA.

As an example, consider a representative example of a VRM with a maximum load current equal to $100A$, an output voltage equal to $1V$, and a trace resistance of $0.2m\Omega$. At the maximum current, the voltage drop $V_o - V_s$ would be equal to $20mV$. This represents a power loss of $2W$ over the $100W$ delivered to the load.

Since the typical efficiency for this application at full load is in the range of $75 - 85\%$, the impact of the power loss due to the trace resistance is acceptable. For a 1% sensing accuracy, it is necessary to resolve $200\mu V$ out of the $20mV$ voltage drop. The bandwidth desired for this measurement is on the order of a few megahertz. A CSA with these characteristics is possible with current technology.

2.3 Method analysis

Some of the assumptions made in the previous section are valid only in ideal circuits. First, there are many factors that make (2.8) only an approximate equation. Second, the PCB trace that goes from the output capacitors to the load behaves as a two-terminal resistor only over a certain bandwidth due to parasitic elements. These issues are addressed in the following subsections.

2.3.1 Errors due to simplified switching model

In a practical implementation, (2.8) is only approximate. The sources of error are described below.

Reverse recovery

Not all the current that goes through the high-side switch flows to the inductor. A correction has to be made to the input current information in order to reflect

more accurately the inductor current. Some of the charge that flows through the high-side MOSFET ends up charging/discharging parasitic capacitances and, most importantly, are recombined in the low-side MOSFET's antiparallel diode (reverse recovery). This effect can be modeled by rewriting (2.5) as [17, pp. 244-247]

$$\langle I_{in} \rangle = \langle u I_L \rangle + Q_{rr} f_s + t_{rr} f_s \langle I_L \rangle \tag{2.9}$$

where Q_{rr} is the reverse recovery charge, t_{rr} is the reverse recovery time, and f_s is the switching frequency. This equation includes both the effect of the charge flowing to the diode and the delay in the switching node voltage due to the reverse recovery time. Rearranging terms, and introducing (2.7), it is concluded that

$$\langle I_{in} \rangle \left(1 - \frac{t_{rr} f_s}{D} \right) - Q_{rr} f_s = \langle u I_o \rangle. \tag{2.10}$$

This expression is more accurate than (2.8), and can be easily contemplated in the estimation circuit of Fig. 2.4 by introducing a gain factor slightly less than unity. In practice, the constant term $Q_{rr} f_s$ is very small (comparable to the voltage offset of the amplifiers), so it can be neglected. The gain factor is represented in Fig. 2.5 by the block with gain $k = 1 - \frac{t_{rr} f_s}{D}$.

Switching command delay

The function $u(t)$ is an idealization of the switching action. In practice, there is a delay between the gate-drive command and the effective switching. This error can be

reduced by extracting u directly from the switching node, and not from the gate-drive command. This implementation is illustrated in Fig. 2.5 by introducing a hysteretic comparator to sense the switching node voltage.

Transients

It is clear that (2.8) was derived under the assumption of steady-state operation, since it is based on the fact that the average current on the input and output capacitors is zero. Besides, the output voltage changes with the load due to Adaptive Voltage Positioning (AVP), so some of the current through the inductor goes into charging/discharging the output capacitor during load transients. However, the effect of transients on the adaptation algorithm is negligible provided that the adaptation is slow enough. The following analysis illustrates how to set bounds on the adaptation loop bandwidth.

Assume there is an output current step ΔI_o, then the average inductor current will converge exponentially to the new output current value with time constant equal to $\tau = R_{LL}C_o$, where R_{LL} is the load-line value and C_o is the output capacitor value [9]. During the transient, (2.6) is not valid, since the difference between $\langle I_o \rangle$ and $\langle I_L \rangle$ is equal to $\Delta I_o \exp^{-t/\tau}$. The integral of that difference is $A_0 \Delta I_o \tau$, where A_0 is the gain of the integrator (i.e., the transfer function of the integrator is $\frac{A_0}{s}$). If the relative

error due to this transient is bounded, then

$$\frac{A_0 \Delta I_o \tau}{1/R_t} < \epsilon \tag{2.11}$$

where $1/R_t$ is the ideal gain of the CSA and ϵ is the desired relative error. This equation gives the following upper bound in the integrator gain

$$A_0 < \frac{\epsilon}{\Delta I_o \tau R_t}. \tag{2.12}$$

For a representative VRM [7], $\Delta I_o^{\text{max}} = 100A$, $\tau = 1\mu s$, and $R_t = 0.3m\Omega$. With $\epsilon = 0.5\%$, then $A_0 = 165 \times 10^3$. The quantity of interest for this calculation is the loop bandwidth, that can be extracted from the circuit of Fig. 2.5 by linearization. The loop gain can be expressed as

$$H(s) = \frac{A_0}{s} I_o R_t D \tag{2.13}$$

therefore the loop bandwidth is

$$\omega_{BW} = A_0 I_o R_t D. \tag{2.14}$$

Notice that the bandwidth depends on the output current. The limitation in the integrator gain gives a bound in the loop bandwidth. For a typical current of $30A$, this bandwidth is

$$\omega_{BW}^{\text{max}} = 148 rad/s \tag{2.15}$$

or equivalently, a time constant of $42ms$. This is fast enough to track any thermal transient.
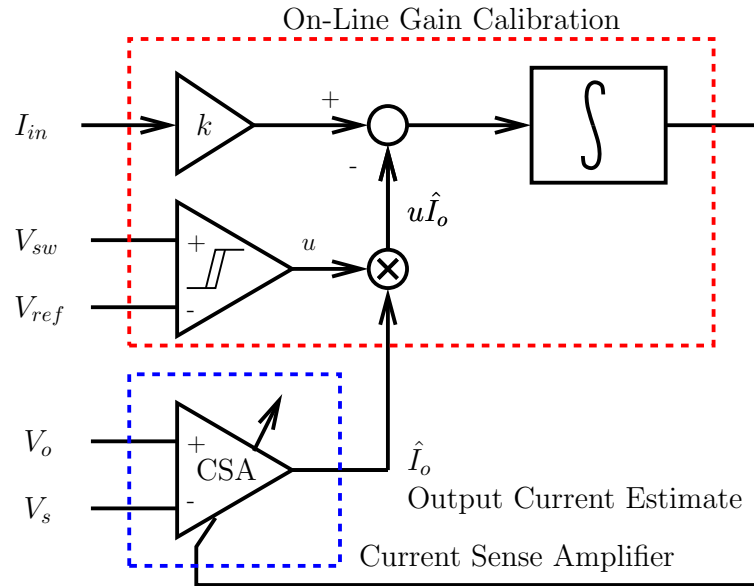
Figure 2.5: Current sense amplifier with gain estimation loop, modified to contemplate non-ideal effects.

Discontinuous Conduction Mode

The relationship (2.8) is valid only in CCM. The converter enters Discontinuous Conduction Mode (DCM) at light loads for some architectures. It is shown in Section 2.4 that the signal is so low at light loads, that the integrator needs to be stopped to prevent a drift in the estimate, so the adaptation loop should never operate in DCM.

2.3.2 Errors due to lumped resistance model

The output trace behaves resistively over a certain frequency range, but at high frequencies the parasitics of the PCB trace make the resistive model unrealistic. This

imposes a practical limit in the bandwidth of the sensing method.

A first-order estimation of the frequency response of two parallel copper plates in a PCB is derived next. Consider a stripline consisting of a pair of rectangular copper plates of length $\mathcal{L}$ and width $\mathcal{W}$, separated by a dielectric material of thickness $h \ll \mathcal{L}, \mathcal{W}$ and relative permeability $\mu_r \approx 1$. When a current I flows lengthwise through one of them and returns in the opposite direction through the other, a magnetic field $H = \frac{I}{\mathcal{W}}$ is formed in the dielectric. The magnetic flux is then

$$\Phi = \mu_0 H \mathcal{L} h = \frac{\mu_0 \mathcal{L} h}{\mathcal{W}} \times I, \tag{2.16}$$

so the inductance is

$$L = \frac{\mu_0 \mathcal{L} h}{\mathcal{W}}. \tag{2.17}$$

The capacitance, on the other hand, can be computed using the well-known equation for a parallel plate capacitor

$$C = \frac{\varepsilon_r \varepsilon_0 \mathcal{L} \mathcal{W}}{h}. \tag{2.18}$$

If the cutoff frequency is estimated as $f_c = \frac{1}{2\pi\sqrt{LC}}$ then the following result is obtained:

$$f_c = \frac{1}{2\pi\sqrt{\varepsilon_r \varepsilon_0 \mu_0}\mathcal{L}}. \tag{2.19}$$

Notice that the dependence on the width of the plate and the thickness of the dielectric cancel out, and the final result depends only on the length and the dielectric

constant. Actually, the product of the angular cutoff frequency and the stripline length $2\pi f_c \mathcal{L} = \frac{1}{\sqrt{\varepsilon_r \varepsilon_0 \mu_0}}$ is the propagation speed of light in this medium.

Therefore, the trace can be approximated by an LC low-pass filter with a cutoff frequency given by (2.19). For a representative PCB (FR4) $\varepsilon_r = 4.7$, then the cutoff frequency can be expressed in international units as

$$f_c = \frac{22 \times 10^6}{\mathcal{L}}. \tag{2.20}$$

For example, a $2cm$ trace would have a cutoff frequency of $1.1GHz$. It is safe to state that the trace will behave resistively at least up to one decade below the cutoff frequency, in our example $110MHz$. It is concluded that, for all practical purposes, the parasitic dynamic components of the PCB trace will not affect the measurement of the output current.

Another potential source of error is the fact that in a practical layout the V_o node is spread since there are many output capacitors in parallel. This is especially the case in multi-phase buck converters, where the phases are kept apart for thermal considerations. The actual output trace is a wide plate of copper. The lumped resistor model might not be adequate due to the difference in the current density in different portions of the plate, which varies during transients. This can be mitigated by measuring the voltage at V_o using the Kelvin sensing technique with a passive resistor network, so as to average out the voltage at different points in the plate. The technique is illustrated in Fig. 2.6 for a three-phase VRM.
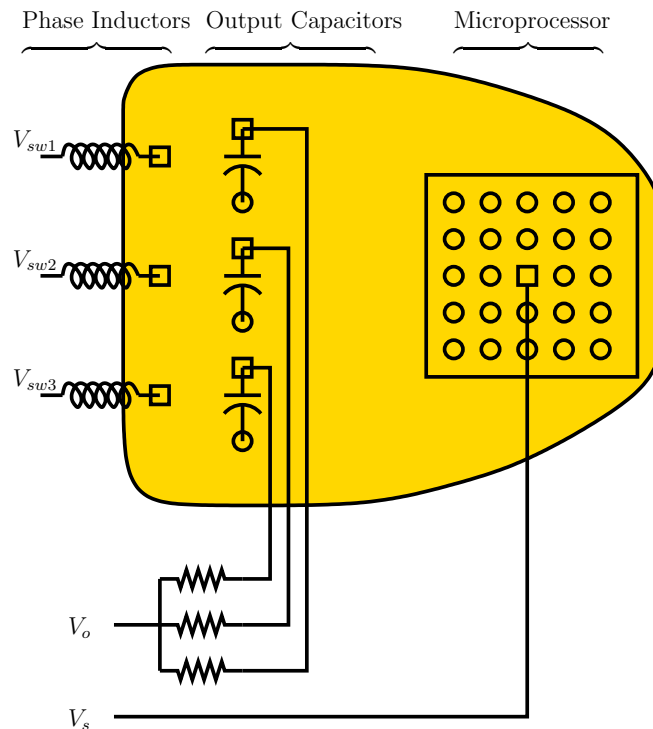
Figure 2.6: Kelvin sensing technique with resistor averaging in a 3-phase VRM.

Finally, in a multi-phase buck converter, and under the assumption that the phase currents are balanced and the adaptation is slow enough to ignore transients, the signal $u(t)$ can be obtained from the switching node of any phase.

2.4   Experimental results

A prototype breadboard implementing the circuit in Fig. 2.5 was built using standard off-the-shelf parts. A simplified schematic of the board is shown in Fig. 2.7, and the main component values are shown in Table 2.2.
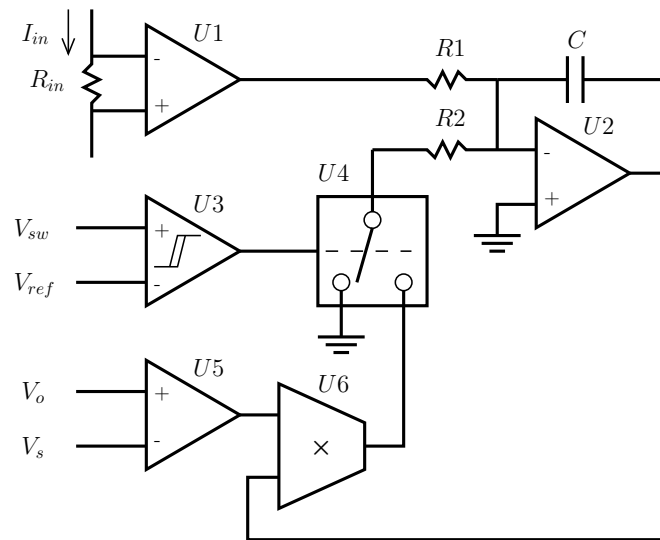
Figure 2.7: Estimation breadboard schematic (simplified).

Table 2.2: Breadboard components

Component	Value
$U1$	AD623
$U2$	TL082
$U3$	AD8611
$U4$	ADG820
$U5$	AD620
$U6$	AD835
R_{in}	$10m\Omega$
$R1$	$33K\Omega$
$R2$	$33K\Omega$
C	$10\mu F$

Table 2.3: Power train components and parameters

Component/Parameter	Value
VRM controller	FAN5019
# phases	3
f_{sw}	$257kHz$
V_{in}	$12V$
V_{out}	$1.2V$
L (per phase)	$680nH$
C	$8 \times 820\mu F$
top switch	FDD6296
bottom switch	2×FDD8896
t_{rr}	$27ns$
Q_{rr}	$12nC$
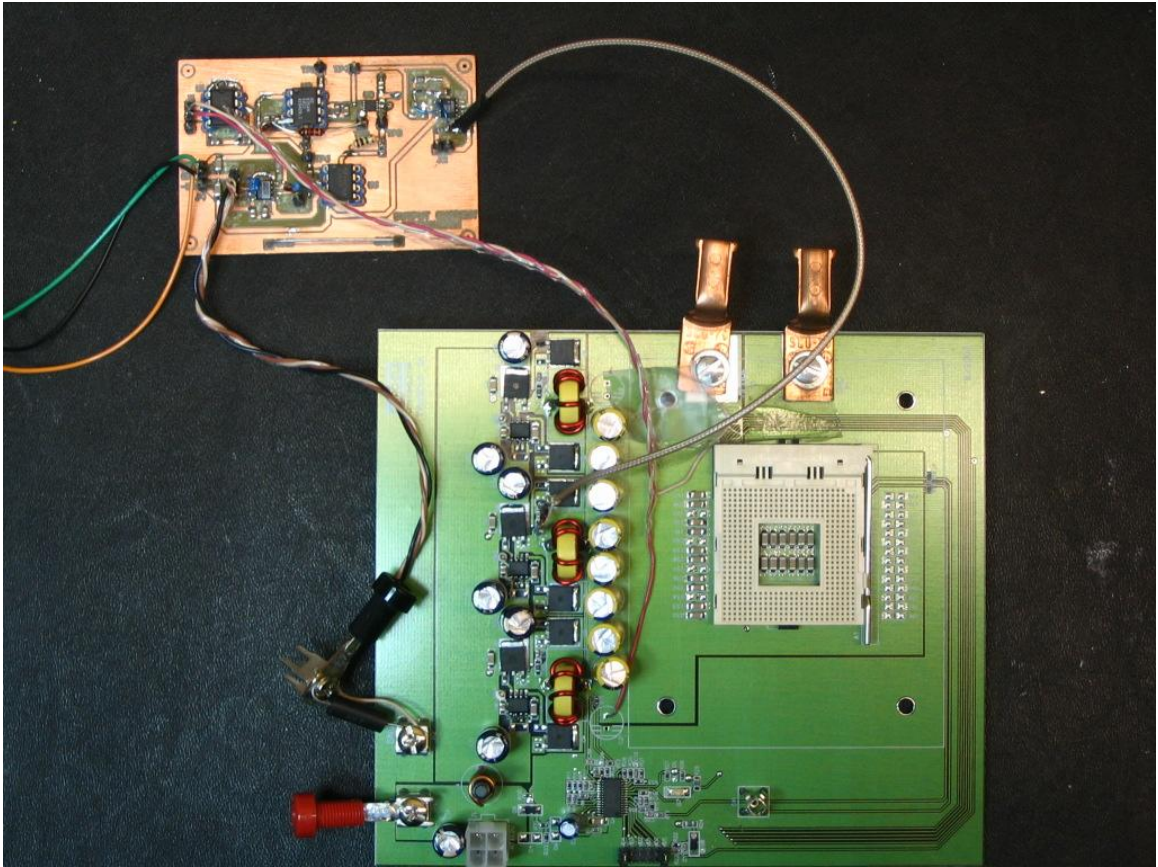
Figure 2.8: Prototype breadboard connected to the VRM evaluation board.

Notice that the factor k is implemented by changing the ratio of resistors $R1$ and $R2$. The board was connected to the 3-phase VRM evaluation board FAN5019_3A of Fairchild Semiconductor, whose main characteristics are listed in Table 2.3. The current estimation error was assessed at DC while the VRM board was running at different loads. A picture of the breadboard connected to the evaluation board is shown in Fig. 2.8.

The results are shown in Fig. 2.9. The dotted line represents the measurements
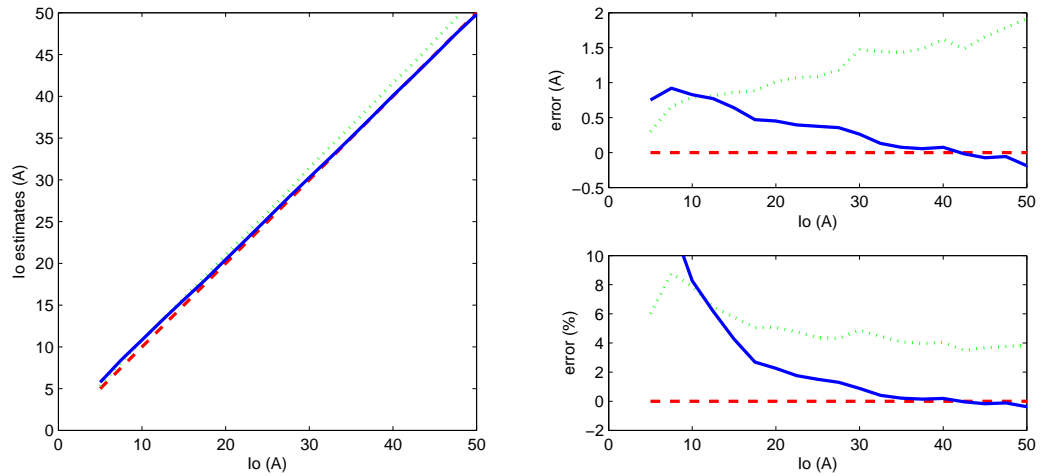
Figure 2.9: Experimental measurements of the current estimation method. Left: measured values. Right: absolute (top) and relative (bottom) errors. (Dashed line: correct value; Dotted line: measurement without trimming; Solid line: measurement after trimming.)

performed without adjusting the input current reference ($k = \frac{R2}{R1} = 1$). The solid line represents the measurements after trimming the gain in the input current path, accounting for the current loss due to reverse recovery. The trimming was done based on empirical observations; however the gain introduced agrees very well with the gain computed using (2.10) based on the MOSFET datasheet. The gain was modified by changing $R1$ to $34K\Omega$ and $R2$ to $32K\Omega$, giving $k = \frac{R2}{R1} = 0.94$. The computed value from the datasheet was $k = 0.93$.

The absolute error remains low for the whole range of load currents, but the relative error is high at light load. At load values below $5A$, the integrator in the estimation circuit starts to drift and reaches saturation. This is reasonable because

the signal level is too low to provide enough information, and the offset voltage of the amplifiers start to dominate the signal. The same situation arises if the converter enters DCM at light load. Although the absolute error in the current estimate is small, it is desirable to avoid this drift so that the integrator value is correct when the load steps up. For these reasons, the integration should be stopped at light load. From the results shown in Fig. 2.9, a threshold of $20A$ would guarantee an estimation error below 2%. To achieve this, R_t should be calibrated during operation at load currents above the threshold, and the calibration should be frozen at load currents below the threshold. Notice that, while the adaptive loop is frozen, the CSA still senses the output current with a constant gain, so the current measurement at light load is still accurate.

The architecture of the estimation circuit allows for an efficient mixed-signal implementation, in which the integration can be performed digitally, with the ability to stop the integration without drift, while the signal conditioning is performed in the analog domain.

2.5 Conclusions

This chapter describes a method that allows for an efficient, accurate, and high-bandwidth measurement of the output current in a buck converter. This enables a VRM application to follow the load-line with precision, and to use output current

feedforward for a fast transient response.

The method uses the PCB trace resistance at the output of the converter as a sensing element. A slow adaptive loop estimates the gain of the sensing amplifier based on the DC relationship between the output current and the input current, which is measured with a precision sense resistor. The effect of transients and switching non-idealities are quantified and included in the method derivation.

A breadboard was constructed and experiments show a precision better than 2% for currents above 20% of the rated maximum. The adaptation loop should never operate at low currents to avoid drifts in the estimate because of the the low signal level compared to the voltage offset of the amplifiers. The estimated current however is accurate for the whole operating range.

Although the method presented makes emphasis on tuning the resistance of the PCB trace, it could be equally used to tune any other sense resistance located in series with the output current or the inductor current, including inductor sensing.

Chapter 3

Phase Current Unbalance

Estimation

In this chapter, a method for estimating the phase current unbalance in a multi-phase buck converter is presented. The method uses the information contained in the voltage drop at the input capacitor's ESR to estimate the average current in each phase. Although the absolute estimation of the currents depends on the value of the ESR and is therefore not accurate, the relative estimates of the currents with respect to one other are shown to be very accurate. The method can be implemented with a low-rate down-sampling A/D converter and is not computationally intensive. Experimental results are presented, showing good agreement between the estimates and the measured values.

3.1 Introduction

The multi-phase synchronous buck converter is the topology of choice for low-voltage high-current DC/DC converter applications [5, 18–23]. The advantages of this topology are numerous. In a converter with N phases the ripple frequency is Nf_s, where f_s is the switching frequency of each phase, therefore both the ripple is reduced and the requirements of the input and output filters are relaxed. Each switch and inductor conducts N times less current than in an equivalent conventional buck converter. Finally, there are more opportunities of control in one clock cycle, meaning that the delay in the control loop gets reduced and a higher bandwidth can be achieved. However, the topology requires more components and a more complex controller.

Furthermore, there is a potential problem with current unbalance. The thermal constraints as well as the dimensioning of the semiconductors and inductors of each phase depend on the maximum current they deliver. If all phases are balanced, the maximum phase current is equal to the maximum load current divided by N. However, small variations in the characteristics of each phase could generate a significant current unbalance, leading to the need to over design the components. Besides that, if the currents are not balanced properly frequency components below Nf_s are present in the input current. In conclusion, most of the advantages of the multi-phase topology are lost if the currents are not balanced.

For this reason, all commercial designs have an active phase balancing circuitry. The most common methods in high-current applications use phase current measurements obtained by inductor sensing [18–20] or R_{DS} sensing [21–23]. Both methods require a priori knowledge of a parasitic series resistance (inductor DCR in the former and MOSFET R_{DS} in the latter) for each phase and need to track its variation with temperature.

In [24] and in this work a method for estimating the current unbalance based on samples of the input voltage is described. The merit of this approach is that the same sensing element (the input capacitor ESR) is used for all phases, therefore eliminating the uncertainty when comparing measurements for different phases. In [24] the input voltage is sampled directly during the conduction time of each phase, and the samples are compared to obtain the unbalance information. However, the input voltage carries a lot of undesired high-frequency content due to the switching of large currents, reducing dramatically the signal-to-noise ratio (SNR) of the sampled values, rendering the method not practical. Furthermore, if the on-times of the different phases superpose (duty-cycle greater than $1/N$), the samples are not useful.

In this chapter, a different approach for sampling the voltage input waveform is presented. Instead of relying on the instantaneous values of the waveform, a frequency analysis is performed on a filtered version of the waveform. This approach results in a much better SNR. A linear relationship between the sampled waveform and the

amplitude of the phase currents is derived. The numerical processing required is equivalent to a low-order matrix-vector multiplication or a low-order FFT, and needs to be updated at a slow rate. With the increasing popularity of digital capabilities in DC/DC controllers, this functionality is not difficult nor costly to implement.

As described above, this method uses the input capacitor ESR as a unique sensing element for all phases. Therefore, the relative relationship of the phase currents' estimates with respect to each other is accurate, although the absolute value still carries the uncertainty in the value of the sensing element. The unbalance information can be used in an active current sharing method to achieve good current sharing among all phases.

This chapter is organized as follows. The current unbalance estimation method is described in Section 3.2. Some practical considerations are addressed in Section 3.3. Finally, experimental results are reported in Section 3.4.

3.2   Method description

The main idea behind the method comes from the understanding of the waveform at the input voltage of a multi-phase buck converter. In Fig. 3.1 a buck converter with two phases is shown to illustrate the derivation of the method.

Usually the input current I_{in} has a very small AC component due to the presence of an inductor (choke). Therefore, the AC component of the current through the
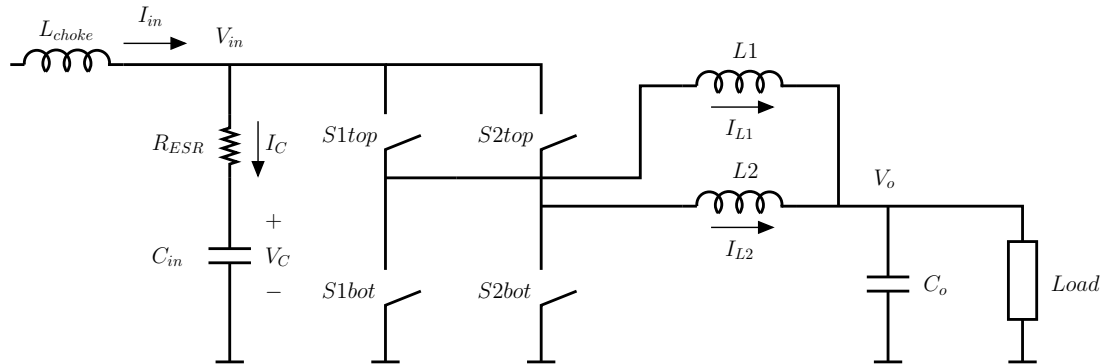
Figure 3.1: Two-phase buck converter. The input capacitor's ESR is shown explicitly.

top switch (e.g., $S1top$) is provided by the input capacitor C_{in}, creating a voltage drop on its ESR that is proportional to the inductor current during the conduction time of the corresponding phase. This creates a perturbation on the input voltage V_{in}. Since the conduction time of the phases is multiplexed in time, the resulting waveform in V_{in} contains the information of the DC amplitude of all phase currents. This is illustrated in Fig. 3.2. In this particular example, the average current in phase 2 is larger than in phase 1. Given that the difference in the phase currents can be appreciated directly from the waveform, it could be argued that sampling the input voltage during the conduction time of each phase could provide the unbalance information. Unfortunately, the samples taken of this waveform are noisy, so this approach becomes impractical. Additionally, in some cases the conduction times of different phases could overlap (for example with a duty-cycle larger than 50% in a two-phase system). For these reasons, it is more practical to analyze the harmonic content of the waveform, as will be described next.
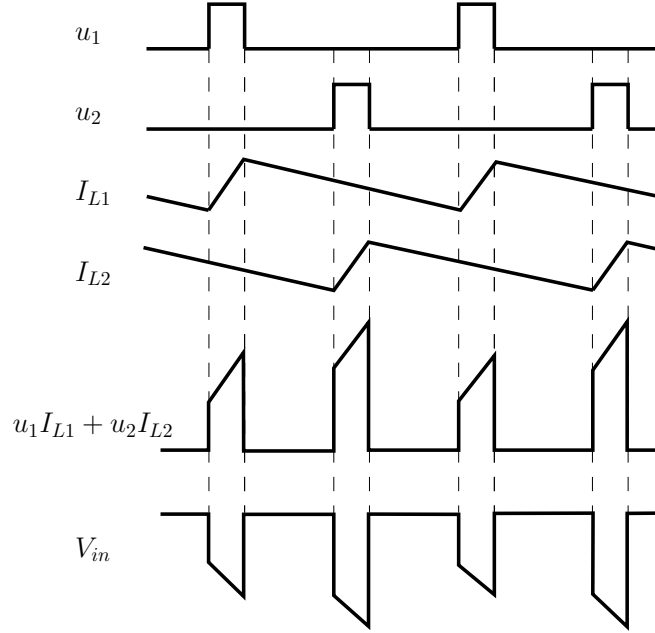
Figure 3.2: Voltage and current waveforms in a two-phase buck converter with unbalanced currents.

In general, for a buck converter with N phases

$$V_{in} = V_C + R_{ESR}I_C \tag{3.1}$$

$$I_C = I_{in} - \sum_{i=1}^{N} u_i I_{Li} \tag{3.2}$$

and then, combining (3.1) and (3.2)

$$V_{in} = V_C + R_{ESR}I_{in} - R_{ESR}\sum_{i=1}^{N} u_i I_{Li} \tag{3.3}$$

where

$$u_i(t) = \begin{cases} 1, & \text{if } Sitop \text{ is ON} \\ 0, & \text{if } Sitop \text{ is OFF} \end{cases} \quad \text{for } i = 1 \ldots N.$$

As mentioned above, in steady-state operation the input current I_{in} can be considered constant. The capacitor voltage V_C, on the other hand, can be considered

constant as long as the time constant $R_{ESR}C_{in}$ is such that the capacitor impedance behaves resistively at the switching frequency. If that is not the case, as could happen with ceramic capacitors, then an extra circuit as depicted in Fig. 3.3 can be used to eliminate the variations due to the charging/discharging of the capacitor. If the RC time constant of the two branches is equal (i.e., $R_{ESR}C_{in} = R_sC_s$), then

$$V_s(t) = R_{ESR}I_C(t). \tag{3.4}$$

Substituting I_C from (3.2), it is concluded that

$$V_s = R_{ESR}I_{in} - R_{ESR}\sum_{i=1}^{N} u_i I_{Li}. \tag{3.5}$$

Notice that this waveform is the same as the input voltage, but without the capacitor voltage. This means that not only are the variations in the capacitor charge excluded, but also that the DC component is eliminated, making the waveform voltage levels more suitable for sampling. In the following derivations, it will be assumed that the waveform to be processed is $V_s(t)$ and not $V_{in}(t)$.

The relative amplitude of the phase currents will be reflected in the harmonic content of the waveform $V_s(t)$, in particular in frequencies kf_s for $k = 1 \ldots N - 1$, where f_s is the switching frequency. For perfectly balanced operation, the V_s waveform would have zero content at these frequencies. In the case illustrated in Fig. 3.2, $V_{in}(t)$ (or equivalently, V_s) has a harmonic component at frequency f_s due to the difference in the average current in the two phases; it is easy to see that the lowest
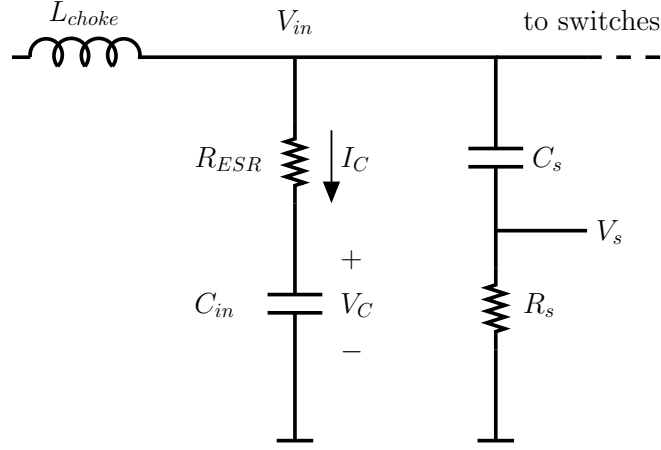
Figure 3.3: Capacitor current sensing.

harmonic frequency present in a two-phase balanced circuit would be $2f_s$. It will be shown below that frequencies above $(N-1)f_s$ can be eliminated without losing the unbalance information, allowing for the sampling of a "clean" waveform, without all the high-frequency content usually present at the input voltage node.

The harmonic content of V_s can be computed by using the Fourier series expansion of a pulse train, and applying the time-shift and superposition properties. A pulse train of amplitude one and duty cycle D (Fig. 3.4) has the following Fourier coefficients:

$$c_0^{PT} = D \tag{3.6}$$

$$c_k^{PT} = c_{-k}^{PT} = D \cdot \frac{\sin k\pi D}{k\pi D}. \tag{3.7}$$

The time origin is located at the middle of the pulse. Notice that it is sufficient to do the computation with a rectangular pulse, and not a trapezoidal one as in Fig. 3.2,
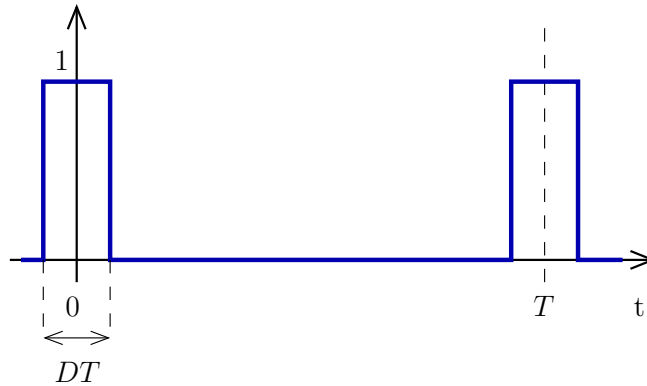
Figure 3.4: Pulse train.

because the higher frequency components are of no interest since the method relies

on lower frequency harmonics.

The waveform $V_s(t)$ can be expressed as a constant term $V_{s0} = R_{ESR}I_{in}$, minus

the sum of N pulse trains of amplitude A_m time-shifted by mT/N, $m = 0 \ldots N - 1$

(Fig. 3.5). The results are general and valid even if the pulses overlap (i.e., $D > 1/N$).

Then, the Fourier series expansion of $V_{in}(t)$ is

$$V_s(t) = \sum_{k=-\infty}^{+\infty} c_k e^{jk\omega t} \tag{3.8}$$

where the Fourier coefficients can be obtained from (3.6) and (3.7), applying the

time-shift and superposition properties

$$\begin{aligned} c_0 &= V_{s0} - c_0^{PT} \cdot \sum_{m=0}^{N-1} A_m \\ &= V_{s0} - D \cdot \sum_{m=0}^{N-1} A_m \end{aligned} \tag{3.9}$$
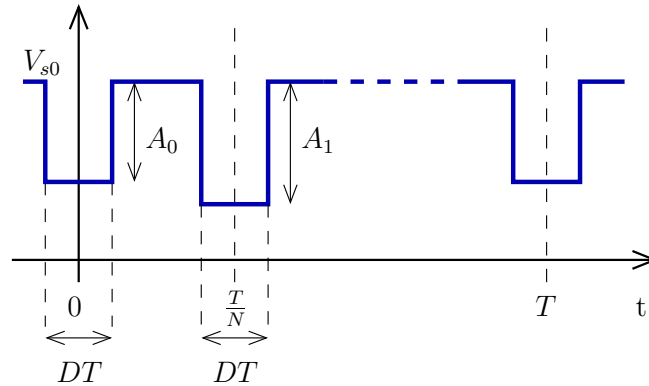
Figure 3.5: The waveform $V_s(t)$ as a superposition of pulse trains.

$$
\begin{aligned}
c_k &= -c_k^{PT} \cdot \sum_{m=0}^{N-1} A_m e^{-j\frac{2\pi km}{N}} \\
&= -D \cdot \frac{\sin k\pi D}{k\pi D} \cdot \sum_{m=0}^{N-1} A_m e^{-j\frac{2\pi km}{N}}.
\end{aligned}
\tag{3.10}
$$

The first N Fourier coefficients from (3.9) and (3.10) can be written in a more compact form as

$$
\mathbf{c} = V_{s0}\mathbf{e_1} - \mathbf{P_D}\mathbf{S_N}\mathbf{a}
\tag{3.11}
$$

where

$$
\begin{aligned}
\mathbf{c} &= \left[\begin{array}{cccc} c_0 & c_1 & \cdots & c_{N-1} \end{array}\right]^{\mathsf{T}} \\
\mathbf{e_1} &= \left[\begin{array}{cccc} 1 & 0 & \cdots & 0 \end{array}\right]^{\mathsf{T}} \\
\mathbf{P_D} &= D \cdot \mathrm{diag}\left[\begin{array}{cccc} 1 & \frac{\sin \pi D}{\pi D} & \cdots & \frac{\sin(N-1)\pi D}{(N-1)\pi D} \end{array}\right]
\end{aligned}
$$

$$\mathbf{S_N} = \begin{bmatrix} W_N^0 & W_N^0 & \cdots & W_N^0 \\ W_N^0 & W_N^1 & \cdots & W_N^{N-1} \\ W_N^0 & W_N^2 & \cdots & W_N^{2(N-1)} \\ \vdots & \vdots & & \vdots \\ W_N^0 & W_N^{N-1} & \cdots & W_N^{(N-1)(N-1)} \end{bmatrix}$$

$$W_N = e^{-j\frac{2\pi}{N}}$$

$$\mathbf{a} = \begin{bmatrix} A_0 & A_1 & \cdots & A_{N-1} \end{bmatrix}^\mathsf{T}.$$

Notice that $\mathbf{S_N}$ is the Discrete Fourier Transform matrix which is invertible, with inverse $\frac{1}{N}\mathbf{S_N}^*$ [25].

Now the problem of computing the Fourier coefficients from a sampled version of the waveform $V_s(t)$ is addressed. Let $x_k = V_s(kT_{\text{samp}})$, where $T_{\text{samp}} = 1/(2Nf_s)$, i.e., the waveform is sampled at $2N$ times the switching frequency. The waveform should be filtered with a low-pass anti-aliasing filter with a cut-off frequency equal to Nf_s for full recovery of the low frequency harmonics.

Then, the relationship between the Fourier coefficients of the continuous-time signal and the sampled values is given by the Discrete Fourier Transform [25]

$$\begin{aligned} \mathbf{c}' &= \frac{1}{2N}\mathbf{S_{2N}}(1:N, 1:2N)\mathbf{x} \\ &= \tilde{\mathbf{S}}_{\mathbf{2N}}\mathbf{x} \end{aligned} \tag{3.12}$$

where $\mathbf{x} = \begin{bmatrix} x_0 & x_1 & \cdots & x_{2N-1} \end{bmatrix}^\mathsf{T}$, and the $2N$-point DFT matrix is truncated to

ignore the negative-frequency components, generating $\tilde{\mathbf{S}}_{\mathbf{2N}}$. The prime notation is used to emphasize that these are the Fourier coefficients of the voltage waveform that is actually sampled. This waveform is different from the input voltage waveform used to derive (3.11) in two aspects: first, there is a distortion introduced by the anti-aliasing filter, and second, there is a phase shift introduced if the sampling is not performed synchronized with the time origin used to derive (3.11). These two effects are deterministic and easy to characterize as follows.

The presence of a low-pass filter before the sampling process may introduce an amplitude and phase distortion in the waveform, that can be taken into account by introducing a correction matrix $\mathbf{C}$ that includes the transfer function of the filter evaluated at the frequencies of interest

$$\mathbf{C} = \mathrm{diag} \left[\begin{array}{cccc} H(0) & H(2\pi f_s) & \cdots & H((N-1)2\pi f_s) \end{array} \right] \qquad (3.13)$$

where $H(\omega)$ is the frequency response of the low-pass filter.

In order to be consistent with the derivation of the Fourier coefficients in (3.7), the origin $t = 0$ has to be positioned at the middle of the conduction time of the phase associated with amplitude A_0. It is usually more convenient for the sampling synchronization to position the origin at the beginning of the conduction period. This would, according to the time-shift property, introduce a phase-shift of $k\pi D$ for each

Fourier coefficient c_k, that can be summarized in a correction matrix $\mathbf{R}$ defined as

$$\mathbf{R} = \text{diag} \begin{bmatrix} 1 & e^{-j\pi D} & \cdots & e^{-j(N-1)\pi D} \end{bmatrix}. \tag{3.14}$$

Then, combining both effects, the relationship between the Fourier coefficients of the sampled waveform and the ideal one is

$$\mathbf{c}' = \mathbf{RCc}. \tag{3.15}$$

Combining (3.11), (3.12), and (3.15)

$$\tilde{\mathbf{S}}_{\mathbf{2N}}\mathbf{x} = \mathbf{RC}\left(V_{s0}\mathbf{e_1} - \mathbf{P_D}\mathbf{S_N}\mathbf{a}\right) \tag{3.16}$$

yielding the vector of phase current amplitudes

$$\mathbf{a} = \mathbf{S_N}^{-1}\mathbf{P_D}^{-1}\left(V_{s0}\mathbf{e_1} - \mathbf{C}^{-1}\mathbf{R}^{-1}\tilde{\mathbf{S}}_{\mathbf{2N}}\mathbf{x}\right). \tag{3.17}$$

Since the objective is to estimate the current unbalance, the difference of each amplitude with respect to the average is derived as

$$\mathbf{a_{diff}} = \mathbf{a} - \frac{1}{N}\mathbf{1}\mathbf{1}^{\mathsf{T}}\mathbf{a} \tag{3.18}$$

where $\mathbf{1} = \begin{bmatrix} 1 & 1 & \cdots & 1 \end{bmatrix}^{\mathsf{T}}$.

Finally, combining (3.17) and (3.18) it is concluded that

$$\begin{aligned} \mathbf{a_{diff}} &= -\left(\mathbf{I} - \frac{1}{N}\mathbf{1}\mathbf{1}^{\mathsf{T}}\right)\mathbf{S_N}^{-1}\mathbf{P_D}^{-1}\mathbf{C}^{-1}\mathbf{R}^{-1}\tilde{\mathbf{S}}_{\mathbf{2N}}\mathbf{x} \\ &= \mathbf{M_{N,D}}\mathbf{x}. \end{aligned} \tag{3.19}$$

Notice that the term involving the DC component of the input voltage gets canceled, confirming that it is irrelevant for the unbalance estimation.

The current unbalance estimation problem was reduced to a linear transformation of a $2N$-dimensional vector into an N-dimensional one. This transformation can be accomplished by a matrix-vector multiplication. The matrix $\mathbf{M_{N,D}}$ only depends on the number of phases, the steady-state duty-cycle, and the characteristics of the anti-aliasing filter, so it would be constant for most applications.

The vector $\mathbf{a_{diff}}$ does not need to be computed every switching period because the current unbalance does not change very fast. Actually, it could be recomputed once every few milliseconds, every few seconds, or much less frequently depending on the application. For this reason, this estimation method does not require much computation power.

3.3   Method implementation

The implementation of this current unbalance estimation technique requires sampling the input voltage waveform and digital processing of the samples obtained. In this section, some practical aspects of the implementation are addressed.

3.3.1 Sampling the input voltage waveform

As stated above, the DC value of the input voltage is not relevant for estimation purposes. Moreover, the common-mode voltage of this waveform may be beyond the range of the controller IC technology. The sensing circuit shown in Fig. 3.3 not only eliminates the fluctuations in the capacitor charge but also suppresses the DC voltage acting as a passive high-pass filter.

Another practical issue arises when the input capacitor consists of several pieces spread on the PCB board, usually following the spread of the different phases. During the conduction time of every phase, most of the current flows through the capacitors closer to the top switch of the corresponding phase. In order to capture all capacitors in a single voltage waveform, resistive averaging is proposed as shown in Fig. 3.6 for the case of a three-phase circuit. If the resistor values are small, namely $R_1 \ll N R_s$, then this circuit is equivalent to the one in Fig. 3.3, but now the average of the voltages in all capacitors is sensed.

The waveform also needs to be filtered with a low-pass anti-aliasing filter, with a cutoff frequency equal to $N f_s$. This can be done with an active filter inside the controller chip.

There need to be $2N$ samples per switching period. The sampling rate however can be arbitrarily reduced by undersampling, as long as the converter is approximately in steady-state. For example, instead of acquiring all the samples in one switching
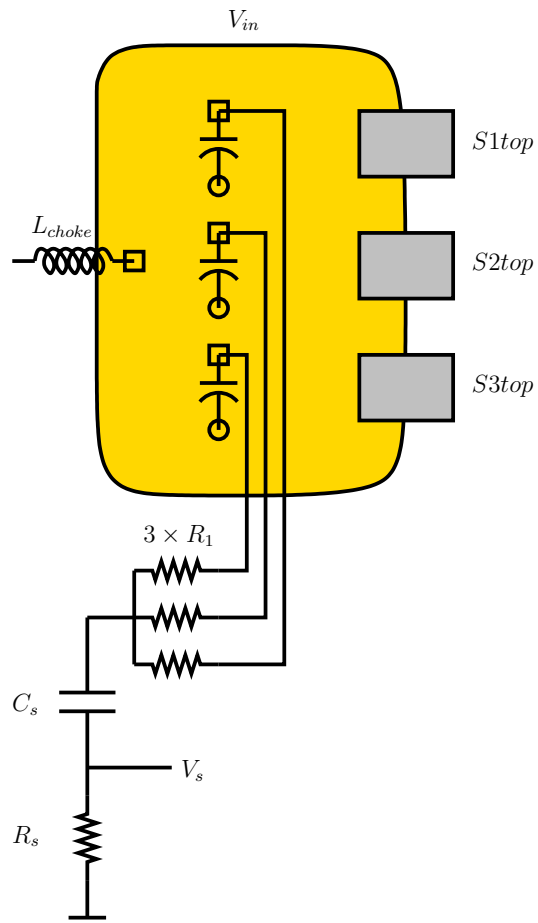
Figure 3.6: Capacitor current sensing using the resistive averaging technique. A similar arrangement can be used at the ground node if necessary. Example with three phases.

period, the first sample could be acquired in one period, the second sample in the following period, and so on. Since the waveform is stationary, the result is equivalent.

Although the derivation assumes $2N$ samples per switching period, this is the minimum needed. More samples per period can be taken, relaxing the requirements for the anti-aliasing filter at the expense of a faster sampling rate and more computation. The only change needed to contemplate more samples is to generate a new matrix $\tilde{\mathbf{S}}_{\mathbf{2N}}$ equal to $\tilde{\mathbf{S}}_{\mathbf{K}} = \frac{1}{K}\mathbf{S}_{\mathbf{K}}(1 : N, 1 : K)$, where $K > 2N$ is the number of samples.

If there is a transient between samples, the estimated unbalance information would not be correct. Given that the time constant of the changes in the current unbalance is large compared to the dynamics of the system, the output of this estimation method could be filtered digitally to smooth out the errors due to transients. This would particularly be the case if the estimated unbalance information is used to balance the circuit in a closed-loop active balancing system with low bandwidth.

3.3.2   Computation

Once the samples are available, all the computation that is needed is given by the linear transformation (3.19), that amounts to the multiplication of a complex-valued N-by-$2N$ matrix by a real-valued vector of length $2N$. Since the results are ideally real numbers (the vector of amplitudes $\mathbf{a_{diff}}$), then the imaginary parts can be ignored

because in the end they will add up to zero. The operations needed for obtaining the results are $2N^2$ multiplications and $2N^2 - N$ additions.

Alternatively, the form given in (3.19) indicates that the transformation is comprised of a $2N$-point DFT ($\tilde{\mathbf{S}}_{\mathbf{2N}}$), followed by a diagonal multiplication ($\mathbf{P_D}^{-1}\mathbf{C}^{-1}\mathbf{R}^{-1}$), an N-point IDFT ($\mathbf{S_N}^{-1}$), and the calculation of the difference of each component with the average. It could be appropriate to use FFT techniques to obtain a more efficient implementation of this transformation. The computation would have four steps. Each M-point DFT or IDFT step implemented with Radix-2 FFT algorithms requires $\frac{M}{2}\log_2 M$ complex multiplications and $M\log_2 M$ complex additions [25], where M is equal to $2N$ in one case and N in the other. The diagonal matrices add N complex multiplications. Finally, the average and difference computations contribute $2N - 2$ real additions. The total is then $N\left(\frac{3}{2}\log_2 N + 2\right)$ multiplications and $N\left(3\log_2 N + 4\right) - 2$ additions. Most of these are complex, although with some clever manipulations some could be reduced to real operations. Assuming no reduction is performed, each complex multiplication is equivalent to four real multiplications and two real additions, and each complex addition is equivalent to two real additions.

The two computation methods are compared in Table 3.1. It is evident that the FFT method is more efficient only for a large number of phases. It is concluded that the matrix-vector multiplication method should be used in most practical cases.

In some applications, the matrix $\mathbf{M_{N,D}}$ can change due to its dependence on

Table 3.1: Number of operations for two estimation methods

	Matrix Method		FFT Method	
N	additions	multiplications	additions	multiplications
4	28	32	116	80
8	120	128	308	208
16	496	512	764	512
32	2,016	2,048	1,820	1,216

the steady-state duty-cycle D. If those changes are substantial, several matrices can be precomputed and in every computation cycle the appropriate one is selected corresponding to the duty-cycle during the acquisition time.

It should be noted also that the inversion of matrix $\mathbf{P_D}$ is not possible if $kD \approx 1$ for $k \in [1, 2, \cdots N - 1]$. In this case, the algorithm should be modified to exclude the problematic harmonic and to instead include higher harmonics to the equation until the problem becomes well-conditioned.

3.4 Experimental results

A three-phase evaluation board for a commercial VRM solution (FAN5019_3A of Fairchild Semiconductor, whose main characteristics are listed in Table 3.2) was used as a test-bed for this concept. The power train was run in open loop, and different distributions of the load current among the three phases were created by inserting
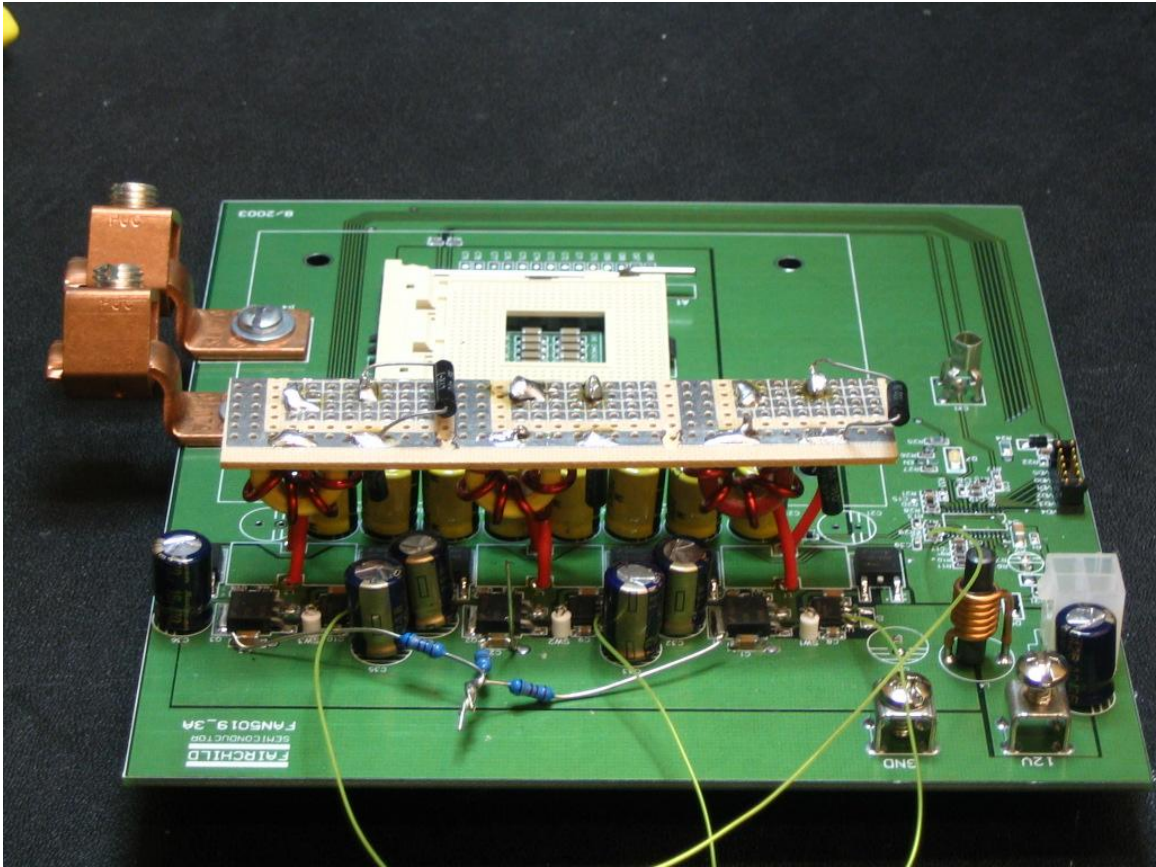
Figure 3.7: Experimental setup.

small resistors of different values in series with the inductors. Since the time constant of the input capacitor was large with respect to the switching period, no capacitor current sensing circuit was used, but the input voltage waveform was captured with a digital oscilloscope in AC-coupling mode. However, the resistor averaging technique was used to average the input voltage at the capacitors located next to each phase. It was noted that symmetry of the layout was critical to obtain good data. The evaluation board with the modifications described is shown in Fig. 3.7.

Table 3.2: VRM evaluation board characteristics

Component/Parameter	Value
# phases	3
f_{sw}	$243kHz$
D	0.11
V_{in}	$12V$
L_{choke}	$630nH$
C_{in}	$6 \times 470\mu F$
R_{ESR}	$18m\Omega/6$
top switch	FDD6296
bottom switch	$2\times$FDD8896

The data processing, including the anti-aliasing filter and sampling, was performed numerically in a PC. Eleven series of data were taken with each series corresponding to a specific distribution of the phase currents. Fig. 3.8 shows an example of the sampled input voltage waveform before and after the anti-aliasing filter, and the samples. In this figure, the benefits of filtering the signal before sampling are evident, since much of the high frequency content is eliminated. The Matlab code used to filter each series of data is presented in Appendix A.

Fig. 3.9 shows the estimation results. The estimated current unbalance for each phase is plotted against the actual current unbalance (measured during the experiment). The estimated currents were derived by dividing $\mathbf{a_{diff}}$, as derived in (3.19),
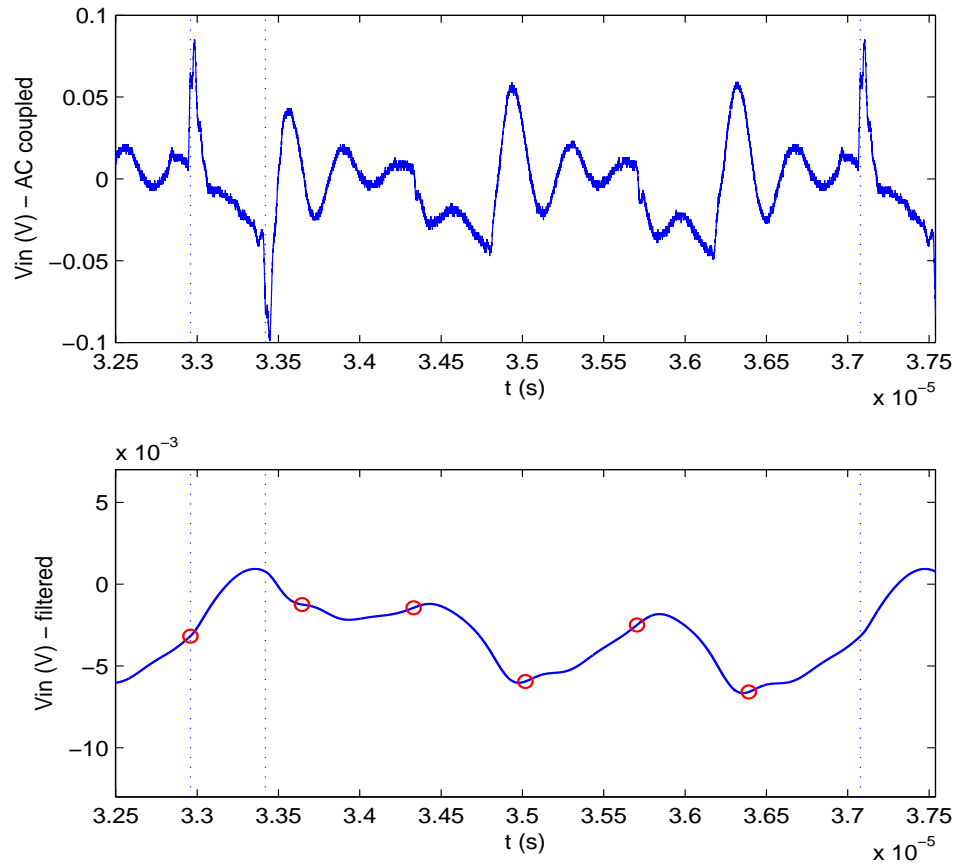
Figure 3.8: Input voltage waveform in a three-phase buck converter. Top: before filtering; Bottom: after filtering. The vertical lines indicate the timing of phase one. The circles indicate the samples.

by the nominal value of the input capacitor ESR. Since this value has a lot of un-
certainty, the points are not aligned with the diagonal $y = x$ but with a line with a
smaller slope. However, the agreement between the estimates and the actual values
is good. The estimation error is within $0.7A$. As a reference, the total current was
$12A$, averaging $4A$ per phase. The rated current per phase in this circuit is $35A$, thus
the error is on the order of 2% of full scale. Moreover, if the information is intended
to be used as part of an active current balancing system then the sign of the current
unbalance is of the most importance, therefore the uncertainty in the ESR value is a
second order effect.

3.5 Conclusions

A method for estimating the phase current unbalance in a multi-phase buck con-
verter was presented. The method is based on the frequency analysis of the input
voltage ripple. Experimental results show good agreement between measured and
estimated phase current deviations with respect to the average. The estimated values
can be used in an active balancing method to achieve good current sharing among all
phases.
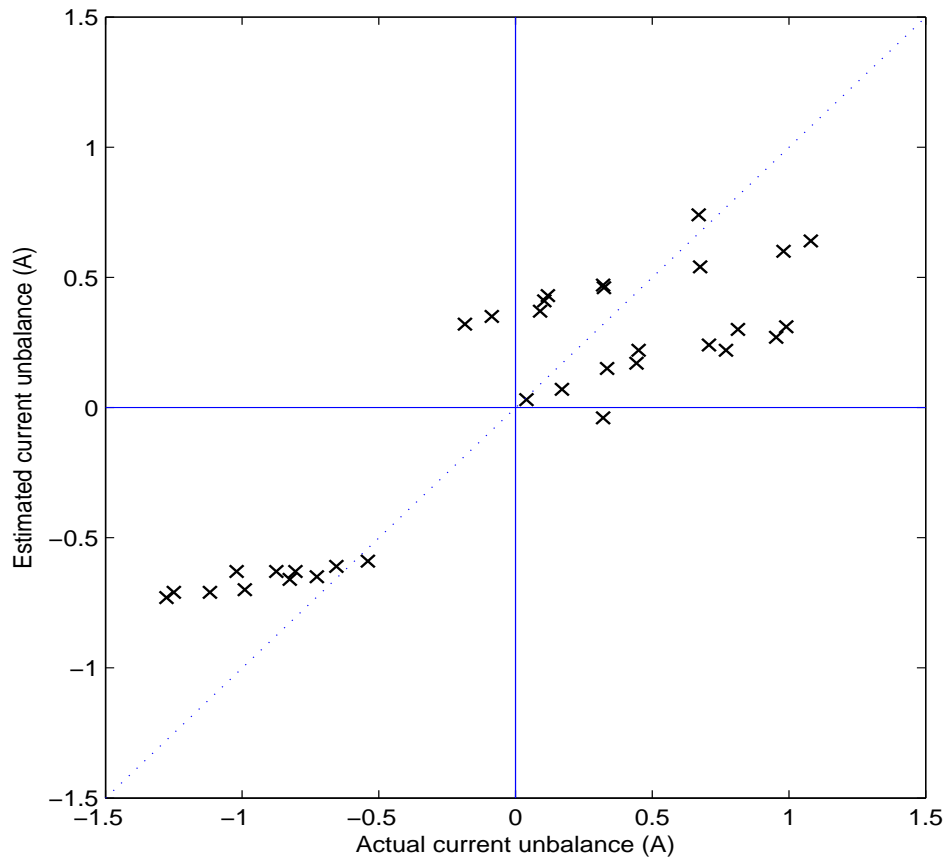
Figure 3.9: Experimental results: estimated unbalance vs. actual unbalance. Unbalance current is defined as the difference between the phase current and the average over all phases. The figure shows eleven series of data with three points each, corresponding to the three phases. Ideally, all points should be on the diagonal.

Chapter 4

Adaptive Output Current Feedforward

In this chapter, a method for adapting the gain of an output current feedforward path in VRM applications is presented. For regulators using Adaptive Voltage Positioning (AVP), output current feedforward can improve the dynamic response to fast load transients. However, the feedforward path depends on parameters of the power train that are not known with precision. By analyzing the error voltage and finding its correlation with the parameter error, a gradient algorithm is derived that makes the parameter error vanish and minimizes the voltage error.

4.1 Introduction

In VRM applications, AVP was adopted as an effective way of reducing the output capacitance [6]. Instead of regulating a fixed voltage, independent of the output current, AVP mandates that the regulator should have a small resistive output impedance. This means that the output voltage has to track the variations in the output current. The specification is valid both for static (DC) operation as well as transients (AC).

In control systems terminology, AVP imposes a tracking problem in which the reference signal becomes $V_r - R_{LL}I_o$, where V_r is the nominal reference voltage, R_{LL} is the reference output resistance (load-line), and I_o is the output current. Since the high-frequency output impedance of the buck converter is always equal to the ESR of the output capacitors, traditional designs select the ESR equal to R_{LL}. This approach works well for electrolytic capacitors. However, this is not feasible for ceramic capacitors, which have a much lower ESR. For this reason, the concept of generalized load-line was introduced [9]. The generalized load-line acknowledges the physical limitations of the system, creating a dynamic output impedance reference Z_{ref} that is equal to R_{LL} at low frequencies, and the ESR of the output capacitor at high frequencies.

In tracking control problems it is usually convenient to include a feedforward path from the reference signal to the input of the plant, in order to improve the dynamic

performance without pushing the bandwidth of the feedback loop too high. This approach is particularly useful in VRM applications, in which the output current has large and fast transients that need to be tracked, while the bandwidth of the feedback loop is limited by the switching frequency of the converter [9]. Output current feedforward had been reported earlier as a way of improving the output impedance of a DC-DC converter [26, 27].

The feedforward path is effective as long as its parameters correspond to the actual values of the plant. Unfortunately, the value of many components in the power train of a VRM converter have a wide uncertainty. For this reason, in this chapter, an adaptive mechanism is presented in order to tune the feedforward path with the objective of minimizing the voltage error.

A traditional *model reference adaptive control* (MRAC) scheme is shown in Fig. 4.1 [28]. The desired behavior of the system is specified with a Reference Model. The difference e between the output y_m of the model and the output y of the Plant is used to tune the parameters of the Controller according to some Adaptation Law. This law is defined such that the behavior of the closed-loop system converges to that of the reference model. In the figure, a typical MRAC scheme for a feedback controller is shown.

In the case of a VRM application with AVP, since the objective is regulation of the output voltage, the output of the reference model is simply the reference voltage
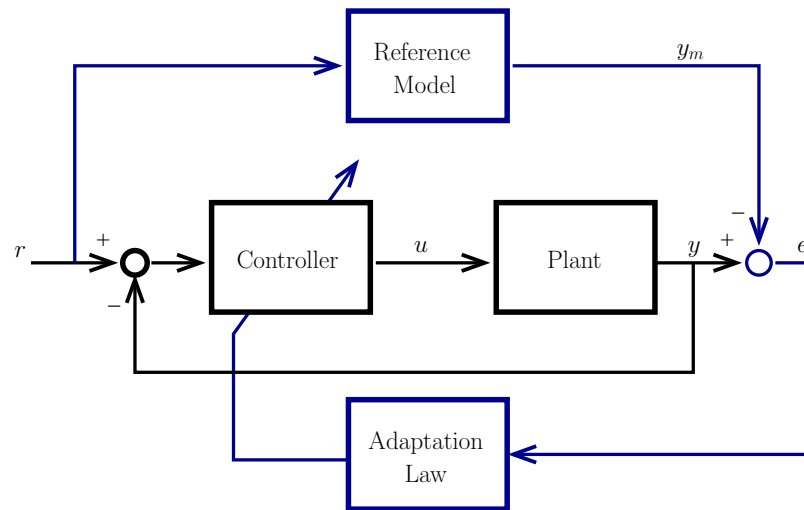
Figure 4.1: Model Reference Adaptive Control.

v_r minus the Reference Impedance times the output current i_o. Therefore, the error

signal to be observed for adaptation purposes is the same error signal v_e that is

sent to the input of the feedback Controller. This is illustrated in Fig. 4.2. In the

adaptive control scheme developed in this chapter, the parameters to be tuned by the

Adaptation Law are those of the Feedforward path.

4.2 Feedforward gain adaptation

4.2.1 Ideal feedforward

The ideal feedforward transfer function can be computed from the block diagram

shown in Fig. 4.3. Block G is the small-signal model of a buck converter, with two
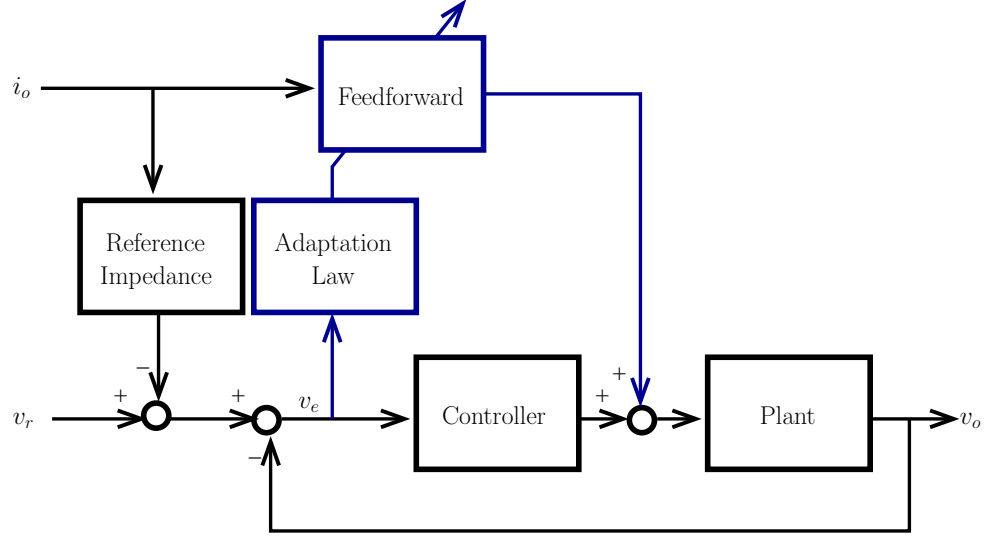
Figure 4.2: MRAC in a VRM application.

inputs corresponding to the duty cycle command d and the output current i_o, and one output corresponding to the output voltage v_o. This two-input-one-output block can be represented by two transfer functions, $G = [G_{vd} \ \ G_{vi}]^\mathsf{T}$ such that

$$v_o = G_{vd} \cdot d + G_{vi} \cdot i_o. \tag{4.1}$$

The feedback controller is represented by block K and the output current feedforward by block F. Adaptive Voltage Positioning is achieved by subtracting the reference impedance Z_{ref} times the output current from the reference voltage v_r.

The closed-loop transfer function from the output current i_o to the output voltage v_o (i.e., the output impedance) in this system is equal to

$$Z_o^{CL} = T_{i_o \to v_o} = \frac{-G_{vd}KZ_{ref} + G_{vd}F + G_{vi}}{1 + G_{vd}K} \tag{4.2}$$
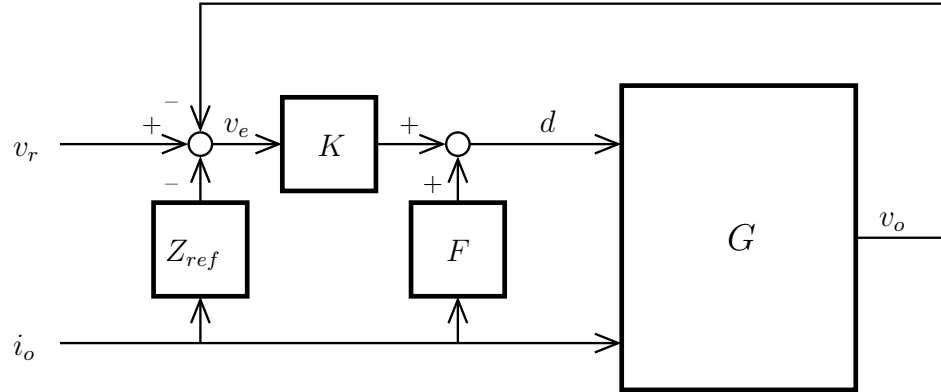
Figure 4.3: DC/DC converter model using voltage mode control and output current feedforward.

By equating the closed-loop output impedance to the desired output impedance $-Z_{ref}$, the ideal value of F can be found to be

$$F = -\frac{Z_{ref} + G_{vi}}{G_{vd}}. \tag{4.3}$$

Notice that the ideal feedforward controller is independent of the feedback controller K. One possible interpretation of this result is that the feedforward path would ideally be able to provide perfect load-line tracking, generating an error v_e equal to zero, and thus making the contribution of the feedback path to the control command d equal to zero independently of the feedback controller. In practice, of course, the feedback loop is still needed to compensate modeling errors and omissions, to reject disturbances, and to provide accurate regulation at low frequency.

The feedforward transfer function (4.3) will be evaluated as a function of the circuit parameters next by introducing the small-signal converter model and the reference impedance transfer function.
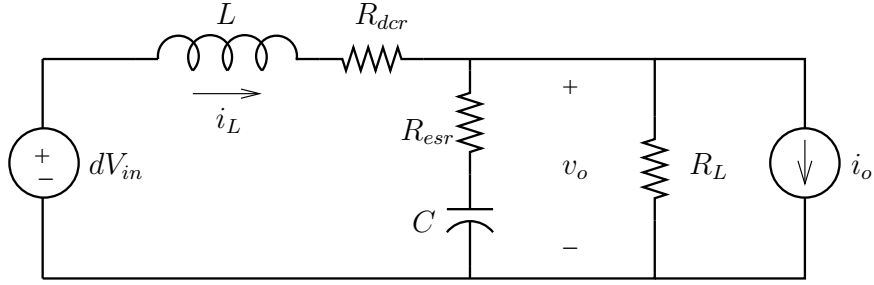
Figure 4.4: Small-signal model of the output stage of a buck converter with resistive load.

The buck converter model can be derived based on the small-signal model of Fig. 4.4. In this model, the load is represented by resistance $R_L = \frac{V_o}{I_o}$, where V_o and I_o are the steady-state output voltage and output current. Together with the steady-state input voltage V_{in}, these quantities define the operation point. The transfer functions of interest are:

$$G_{vi} = \left.\frac{v_o}{i_o}\right|_{d=0} = -\frac{R_L}{R_{dcr} + R_L} \frac{(Ls + R_{dcr})(R_{esr}Cs + 1)}{\frac{R_{esr}+R_L}{R_{dcr}+R_L}LCs^2 + \frac{(R_{dcr}R_L+R_{esr}R_L+R_{esr}R_{dcr})C+L}{R_{dcr}+R_L}s + 1} \quad (4.4)$$

$$G_{vd} = \left.\frac{v_o}{d}\right|_{i_o=0} = \frac{V_{in}R_L}{R_{dcr} + R_L} \frac{R_{esr}Cs + 1}{\frac{R_{esr}+R_L}{R_{dcr}+R_L}LCs^2 + \frac{(R_{dcr}R_L+R_{esr}R_L+R_{esr}R_{dcr})C+L}{R_{dcr}+R_L}s + 1} \quad (4.5)$$

The generalized load-line [9] is given by:

$$Z_{ref} = R_{LL} \cdot \frac{R_{esr}Cs + 1}{R_{LL}Cs + 1} \quad (4.6)$$

where R_{LL} is the desired low-frequency load-line.

After substitution of these values in (4.3) and some algebra, the following exact

result is obtained:

$$F = -\frac{\frac{R_{LL}R_{esr}}{R_L}LCs^2 + \left[R_{LL}R_{esr}\left(\frac{R_{dcr}}{R_L}+1\right)C + \left(\frac{R_{LL}}{R_L}-1\right)L\right]s + R_{LL} - R_{dcr} + \frac{R_{LL}R_{dcr}}{R_L}}{V_{in}\left(R_{LL}Cs+1\right)}$$

(4.7)

Some approximations can be made at this point. Usually, $R_L \gg R_{dcr}, R_{esr}, R_{LL}$. This can be understood in terms of the converter efficiency: if the condition is not valid, then the converter would have very poor efficiency. Under this assumption, the function can be simplified as:

$$F \approx -\frac{R_{LL}\left[\frac{R_{esr}}{R_L}LCs^2 + \left(R_{esr}C - \frac{L}{R_{LL}}\right)s + 1 - \frac{R_{dcr}}{R_{LL}}\right]}{V_{in}\left(R_{LL}Cs+1\right)}$$

(4.8)

Further approximations can be made by recognizing that typically $\frac{L}{R_{LL}} \gg R_{esr}C$ and that over the range of frequencies of interest, the numerator is dominated by the first order term in s. Finally, the expression can be written as

$$F \approx \frac{Ls}{V_{in}\left(R_{LL}Cs+1\right)}.$$

(4.9)

This is the same expression reported in [9] for voltage mode control. It can be seen that the feedforward path consists of a derivative term with a high-frequency pole. The most critical parameter is the gain or multiplying factor of the derivative term.

4.2.2   Adaptation algorithm

The feedforward transfer function (4.9) is a high-pass filter that only generates a feedforward signal during transients. The feedback controller provides accurate

regulation at low frequencies. An error in the gain of the feedforward path will be reflected in a non-zero voltage error v_e during transients. The information contained in this signal will be used to tune the gain of the feedforward path.

In order to derive the adaptation law, a gain stage is added to the feedforward path noted as parameter θ, that ideally would be unity. Since the actual values of the parameters in the circuit (most notably the inductance L) may be different from the values used to compute F, the parameter θ will be allowed to change in order to compensate this difference. Then, the feedforward path will be

$$\hat{F} = -\theta \cdot \frac{Z_{ref} + G_{vi}}{G_{vd}}. \tag{4.10}$$

From Fig. 4.3, the error voltage v_e can be computed as

$$v_e = \frac{Z_{ref} + G_{vi}}{1 + G_{vd}K} (\theta - 1) \cdot i_o. \tag{4.11}$$

Define the parameter error $\phi = \theta - 1$ and a new signal

$$h = \frac{Z_{ref} + G_{vi}}{1 + G_{vd}K} \cdot i_o, \tag{4.12}$$

then

$$v_e = h \cdot \phi. \tag{4.13}$$

A gradient algorithm [28] is implemented by defining the following estimation law:

$$\dot{\theta} = -g \cdot h \cdot v_e, \tag{4.14}$$

where $g > 0$ is a "small" value that will define the bandwidth of the adaptation algorithm.

It is simple to prove the convergence of this algorithm. Substituting (4.13) into (4.14) yields

$$\dot{\phi} = \dot{\theta} = -g \cdot h^2 \cdot \phi. \tag{4.15}$$

This equation shows that the adaptation algorithm will always change the value of the parameter θ in the direction that makes the parameter error ϕ go to zero, provided $h \neq 0$. The rate of convergence depends on the magnitude of the signal h as well as the gain g. In order to achieve an effective convergence to zero, h has to contain enough information to drive the equation ("persistence of excitation" [28]). In practice this is always achieved in VRM applications because the output current does not remain constant. Moreover, with a digital implementation of the algorithm, once the parameter error converges to zero the persistence of excitation requirement is not necessary anymore and the correct value of θ can be stored in a register.

In order to obtain the signal h, the output current i_o needs to be filtered according to (4.12) by the transfer function

$$D(s) = \frac{Z_{ref} + G_{vi}}{1 + G_{vd}K}. \tag{4.16}$$

By using (4.3), this equation can also be written as

$$D(s) = -F \cdot \frac{G_{vd}}{1 + G_{vd}K}. \tag{4.17}$$
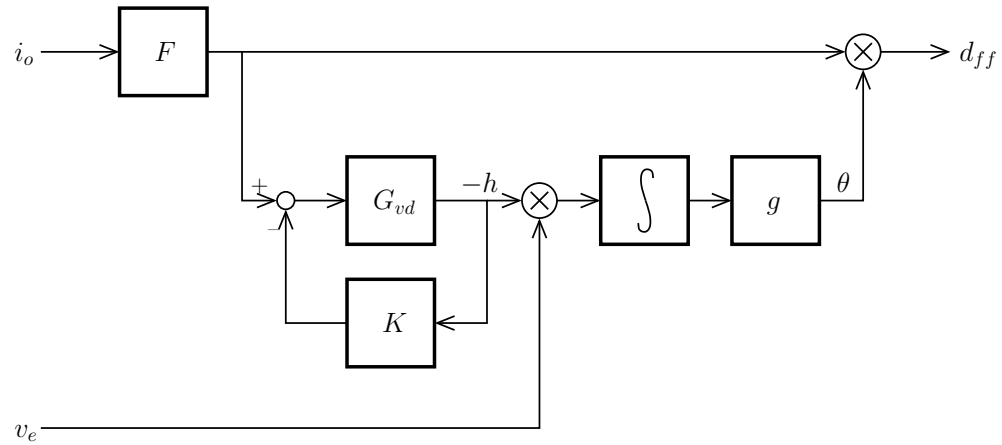
Figure 4.5: Feedforward path with gain adaptation algorithm.

The feedforward path with the gain adaptation algorithm is shown in Fig. 4.5. This implementation requires a filter consisting of a replica of the plant transfer function G_{vd} and the feedback controller K, one integrator, and two multipliers. The output d_{ff} is the duty-cycle command that is added to the output of the feedback controller as in Fig. 4.3.

The adaptation algorithm was simulated using representative values for the power train and controller. The simulations of the output current step down response are shown in Fig. 4.6 and compared to the case of fixed-gain feedforward and no feedforward. It can be seen that, while output current feedforward improves the transient response, it is not a good response due to the uncertainty in the value of the inductor. With adaptive-gain feedforward, the transient response improves considerably and remains unaffected by the uncertainty in the inductor value.
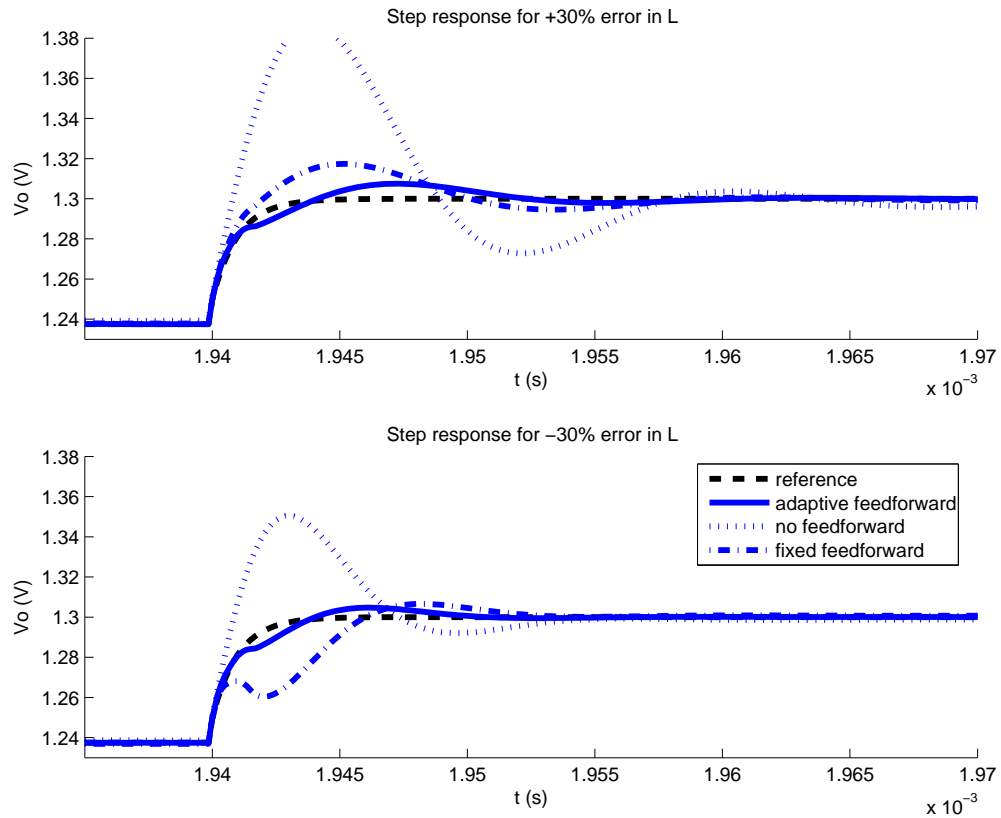
Figure 4.6: Simulation of an output current step down response under three different conditions: without feedforward (dotted), with fixed-gain feedforward (dash-dotted), and with adaptive-gain feedforward (solid). The top figure corresponds to an initial gain error of +30%, and the bottom one to an error of -30%.

4.3   Digital implementation

In Fig. 4.5 it can be seen that the transfer function $D(s)$ of (4.17) is implemented in two parts. The output current i_o is filtered with F, and then processed with the feedback connection of G_{vd} with K. The first part is shared with the actual feedforward path, so it will already be implemented. The second part has a total transfer function equal to

$$\tilde{D}(s) = \frac{G_{vd}}{1 + G_{vd}K}.$$

(4.18)

(Notice that the minus sign is carried to the output and into the gradient search (4.14).) The algebraic expression for this transfer function is of fourth order, but it will be shown that it can be simplified to a second-order expression.

The bode plots of $D(s)$ and $\tilde{D}(s)$ are shown in Fig. 4.7 for a representative set of parameters. In the figure it could be seen that the range of frequencies where the magnitude of the filter $D(s)$ is significant is around $[10^4, 10^7]$. In this frequency range, the filter can be approximated as a second order filter with a zero at the origin. Therefore, since F has a zero at the origin, $\tilde{D}(s)$ can be approximated as

$$\tilde{D}(s) \approx \frac{k}{\frac{s^2}{\omega_n^2} + \frac{2\xi}{\omega_n}s + 1},$$

(4.19)

where k, ω_n and ξ are to be determined empirically. With this approximation, and after suitable choice of parameters, the transfer functions are the ones shown in Fig. 4.7.
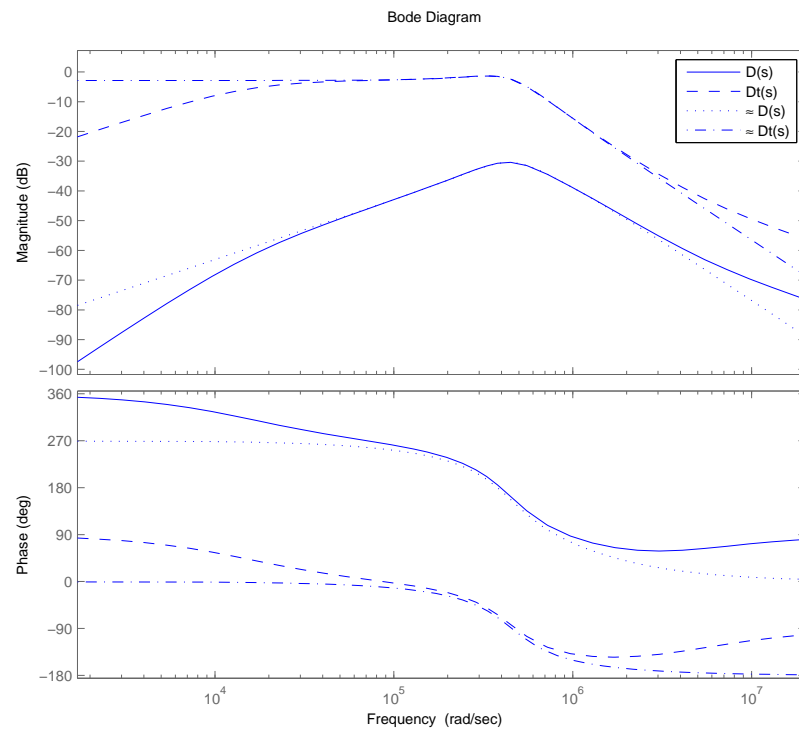
Figure 4.7: Bode plot of $D(s)$ (solid), $\tilde{D}(s)$ (dashed), and their approximations (dotted and dash-dotted respectively).
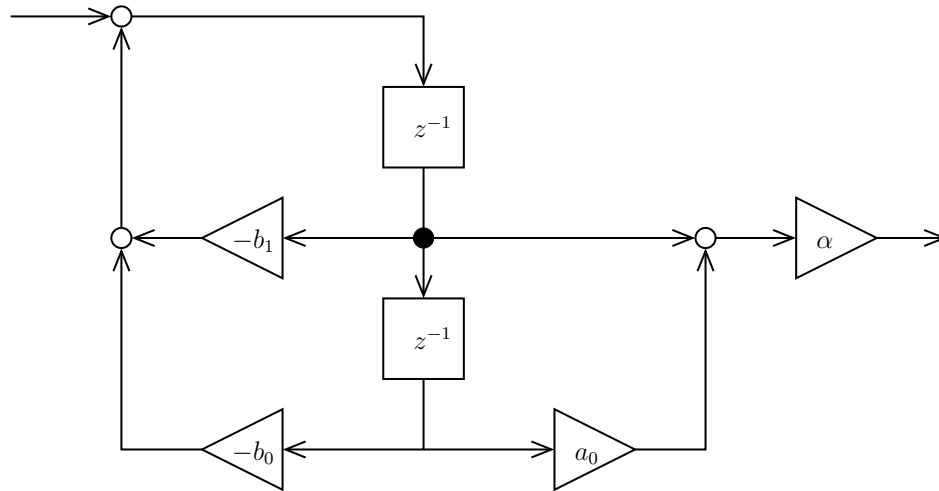
Figure 4.8: Implementation of digital filter $\tilde{D}(z)$.

An equivalent digital filter in the z-domain can be extracted from (4.19) using a bilinear transformation. The general form of such a digital filter is

$$\tilde{D}(z) = \alpha \cdot \frac{z + a_0}{z^2 + b_1 z + b_0}. \tag{4.20}$$

In Fig. 4.8 an implementation of this filter is shown. The filter coefficients can be approximated by sums or subtractions of powers of two, so the filter can be implemented efficiently using only adders and shift operations. The effect of these approximations, as well quantization effects, can be analyzed by simulation to reach a reasonable trade-off between accuracy and cost of implementation.

In the experimental setup used, filter F is implemented analogically using an operational amplifier to perform the derivative of the output current signal with an extra high-frequency pole. The output of this filter is digitized and used as the
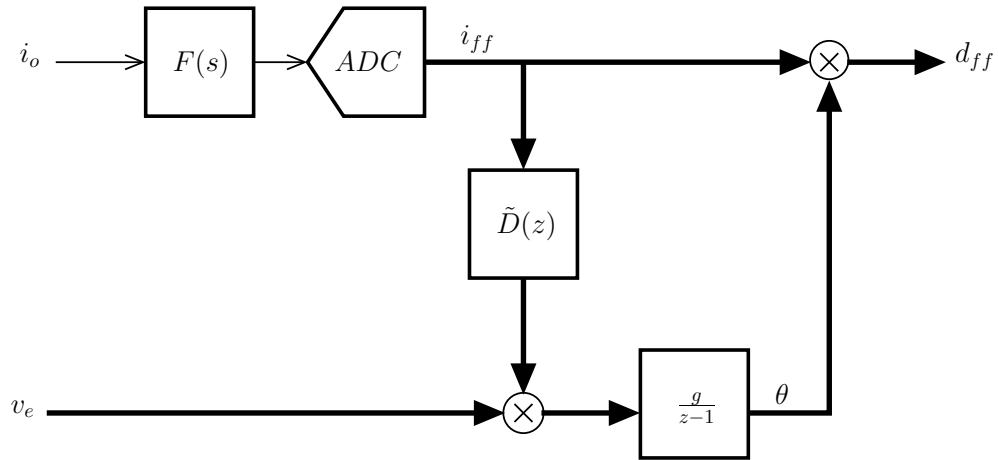
Figure 4.9: Adaptive feedforward implementation. Digital signals are shown with bold lines.

feedforward command i_{ff}. This same signal is used as an input to filter $\tilde{D}(z)$ in order to perform the gain adaptation. The value of v_e, on the other hand, is already available in digital form at the digital feedback controller. The overall circuit of the implementation is shown in Fig. 4.9.

4.4 Experimental results

The adaptive feedforward control is implemented in an FPGA board and connected to a prototype four-phase VRM power train. The FPGA board contains a Xilinx VirtexII-Pro chip and two A/D converters for sampling the error voltage and the derivative of the output current. PWM is implemented digitally in the FPGA using a combination of a counter with an external delay line and dither [29]. The feedback controller is a PID implemented in the FPGA. The output current is mea-

Table 4.1: FPGA board characteristics.

FPGA board	
FPGA	Xilinx XCV2P40-7FG676
ADC for v_e	ADC10030CIVT
	LSB $= 2mV$
ADC for i_{ff}	ADC10030CIVT
	LSB $= 71mA/\mu s$
f_{sw}	$372kHz$
f_{samp}	$4 \times f_{sw} = 1.49MHz$
sampling delay	$210ns$
computation delay	$84ns$
DPWM resolution	11 bits $= 13ns$

sured using a sense resistor. The characteristics of the two boards are presented in Tables 4.1 and 4.2, and photos are shown in Fig. 4.10 and 4.11. The two boards are connected one on top of the other, as shown in Fig. 4.12.

A high-level block diagram of the FPGA implementation is shown in Fig. 4.13, and the Verilog code for the adaptive feedforward block is presented in Appendix B. The sensing circuits are shown in Fig. 4.14. The output voltage is sensed using resistive averaging of the voltages across the output capacitors of each phase. Twisted pairs are used to connect the differential signals to the input of the differential amplifiers. The signal conditioning is shown in Fig. 4.15. There is a differential stage for each signal, followed by a conversion to a ground-referenced voltage with an adequate

Table 4.2: Power train board characteristics.

Power train board	
# phases	4
V_{in}	$12V$
V_{ref}	$1.2V$
R_{LL}	$1.5m\Omega$
R_{sense}	$1.5m\Omega$
L	$300nH$ per phase
C	$1.2mF$
R_{esr}	$1.2m\Omega$
top switch	$2\times$Si4892DY
bottom switch	$2\times$Si4362DY
drivers	LM27222
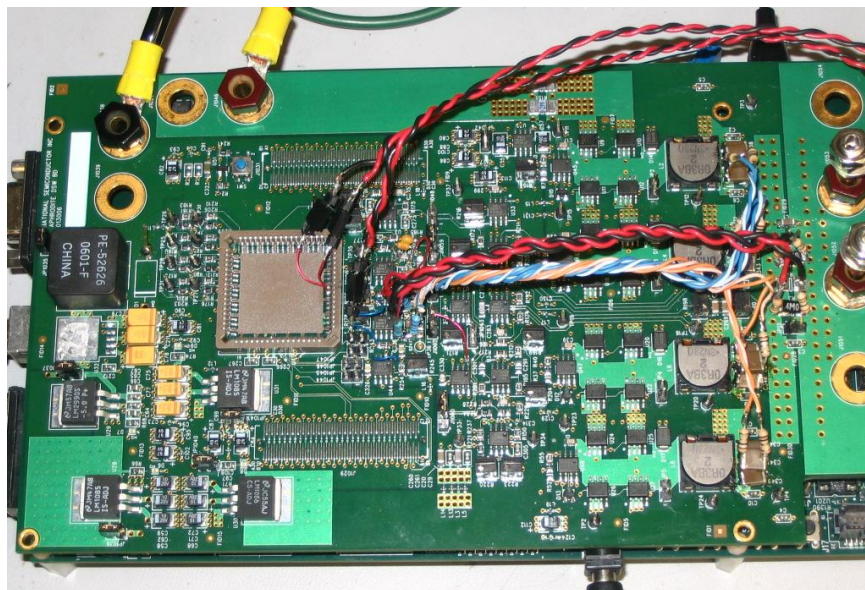
Figure 4.10: Experimental setup: power train board.
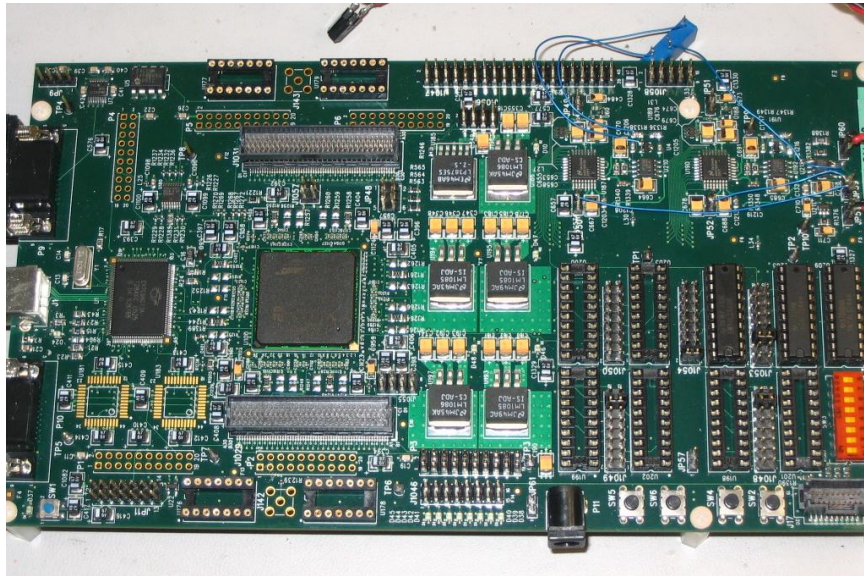
Figure 4.11: Experimental setup: FPGA board.
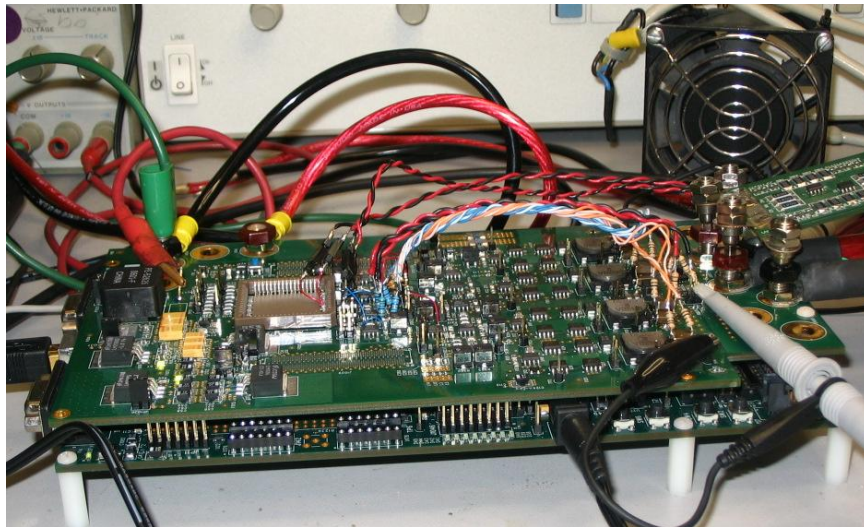
Figure 4.12: Experimental setup: boards interconnected.
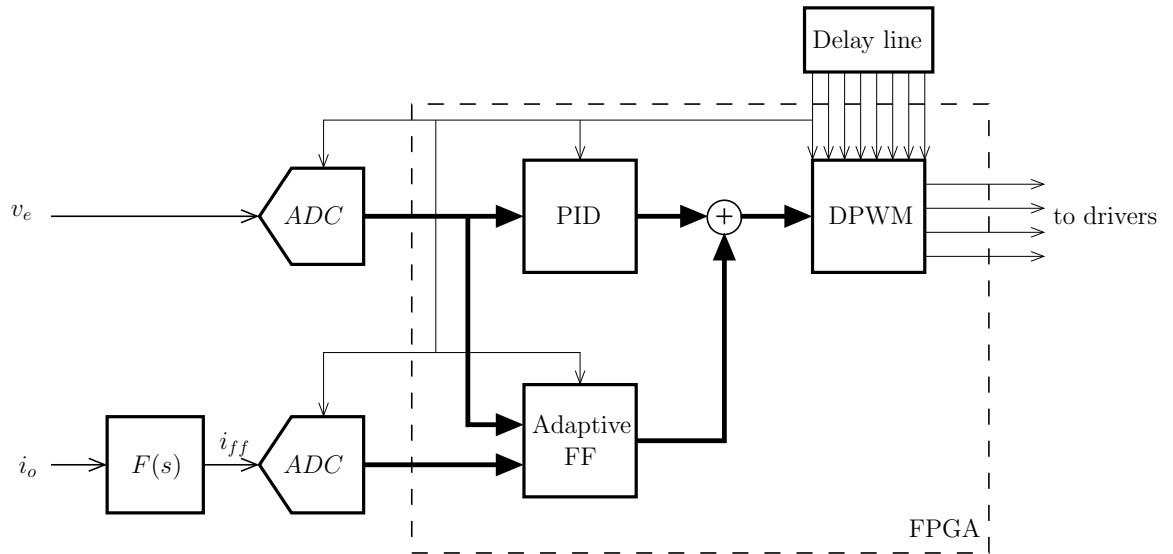
Figure 4.13: FPGA implementation block diagram.

common-mode voltage for the ADCs.

The experimental results are shown in Figs. 4.16-4.19. A $30A$ step (from $5A$ to $35A$) is generated with a resistive load fired by a fast MOSFET. In Fig. 4.16 only the feedback controller is operating and an undershoot of about $50mV$ with respect to the new steady-state value is observed in the transient response. In Fig. 4.17, the feedforward path is enabled with a fixed gain that is less than the optimal value, a situation that may occur in practice due to the uncertainty in the power train components. The transient response improves and the undershoot is reduced to around $30mV$. In Fig. 4.18 a similar situation is presented, but this time the fixed gain is greater than the optimal, resulting in an overshoot of around $10mV$ followed by an undershoot of around $25mV$. Finally, in Fig. 4.19 the adaptive feedforward method is
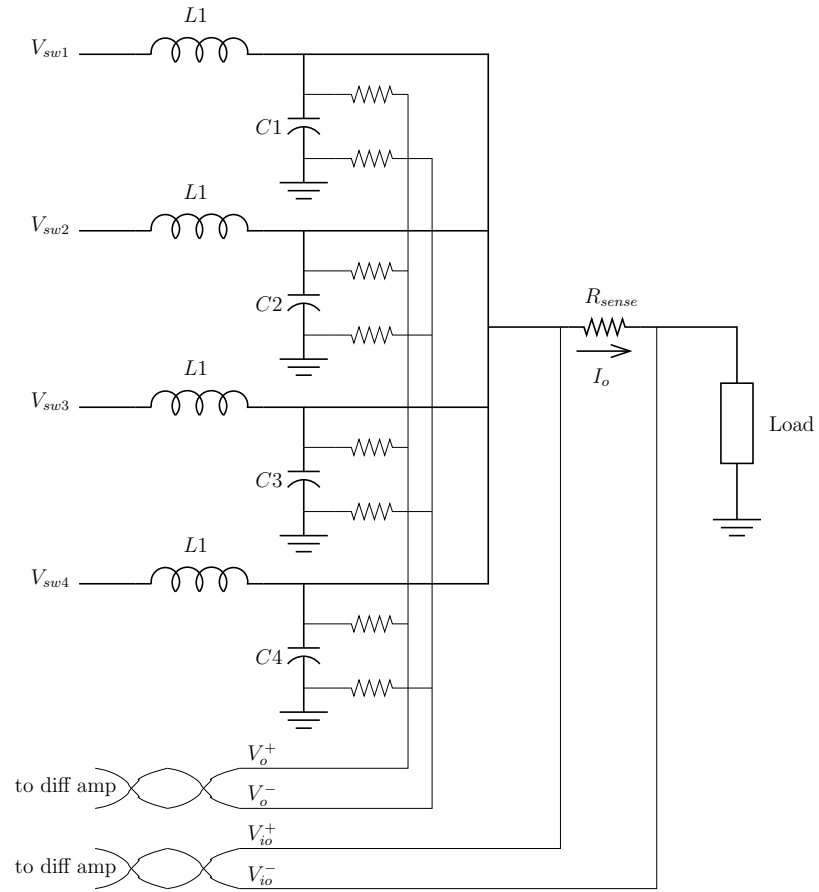
Figure 4.14: Sensing circuits.
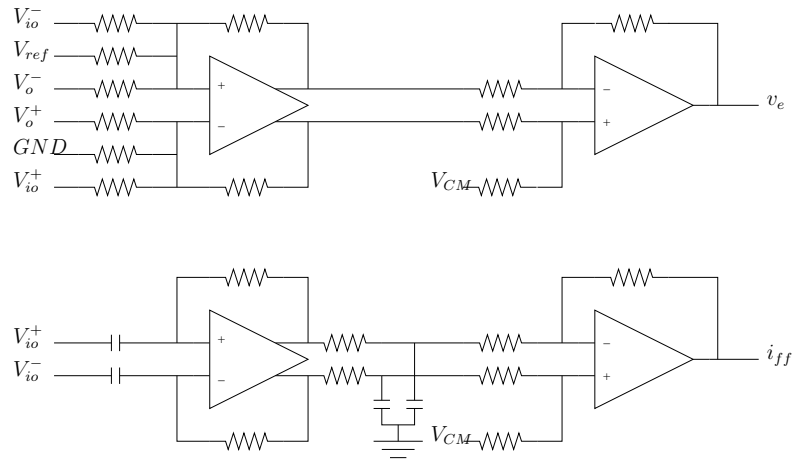
Figure 4.15: Signal conditioning circuits.

enabled, and the gain converges to a value that provides the best transient response achievable with an undershoot of around $20mV$.

In these experiments it was not possible to achieve a better performance than the one presented because there is substantial delay both in the feedforward and the feedback paths. This delay is caused mainly by the conversion time of the pipelined ADCs. In Table 4.1 it can be observed that the conversion time plus the computation time are close to $300ns$. The modulator adds an extra delay. During this time, in a positive loading transient the output capacitor discharges and it becomes very difficult to avoid the undershoot. In an unloading transient the situation is analogous, although saturation of the duty cycle is more likely to happen than in the step-up case because the steady-state duty cycle is around 0.1. If saturation occurs, the response depends mostly on the power train parameters and the controller delay [9]. For these
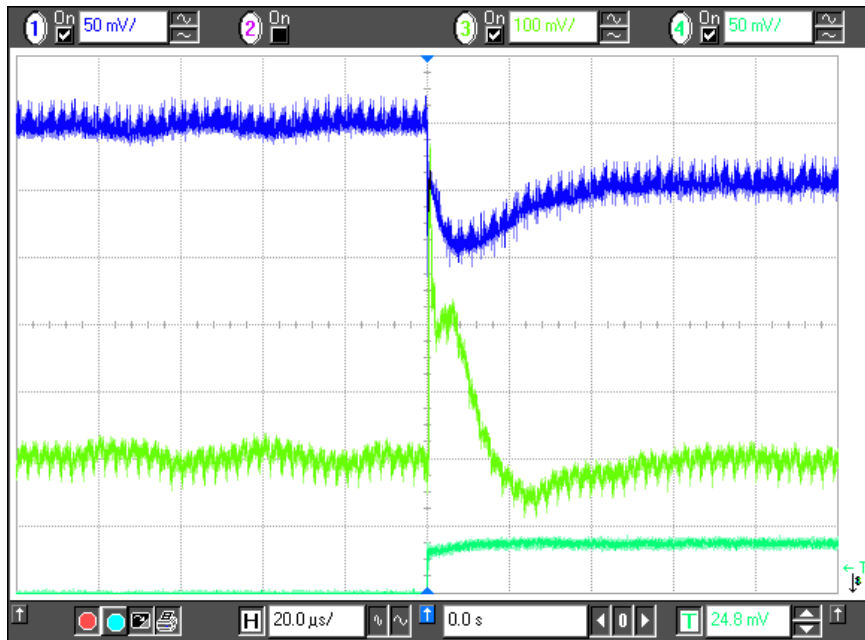
Figure 4.16: Step response with feedback only. Top: v_o, middle: i_{ff}, and bottom: i_o.
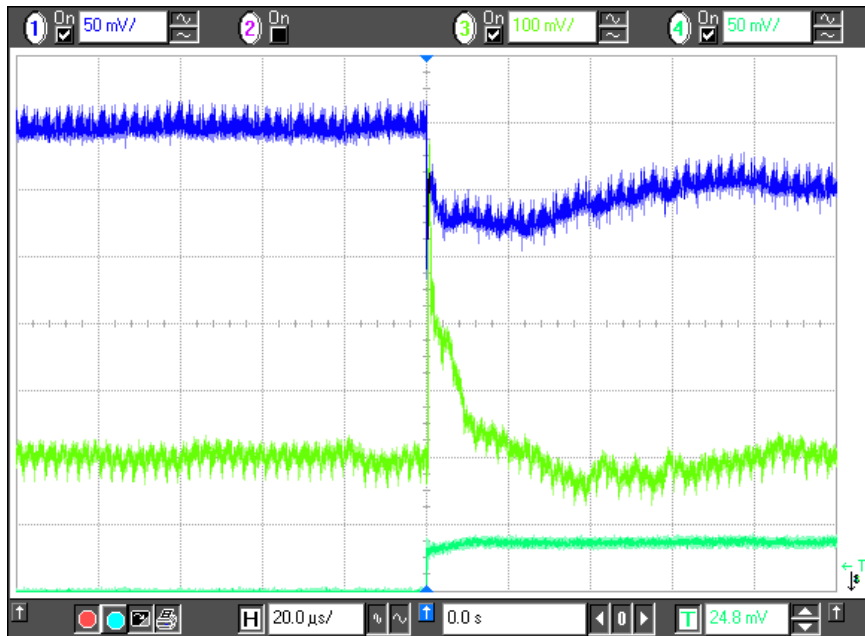
Figure 4.17: Step response with fixed-gain feedforward (small value). Top: v_o, middle: i_{ff}, and bottom: i_o.
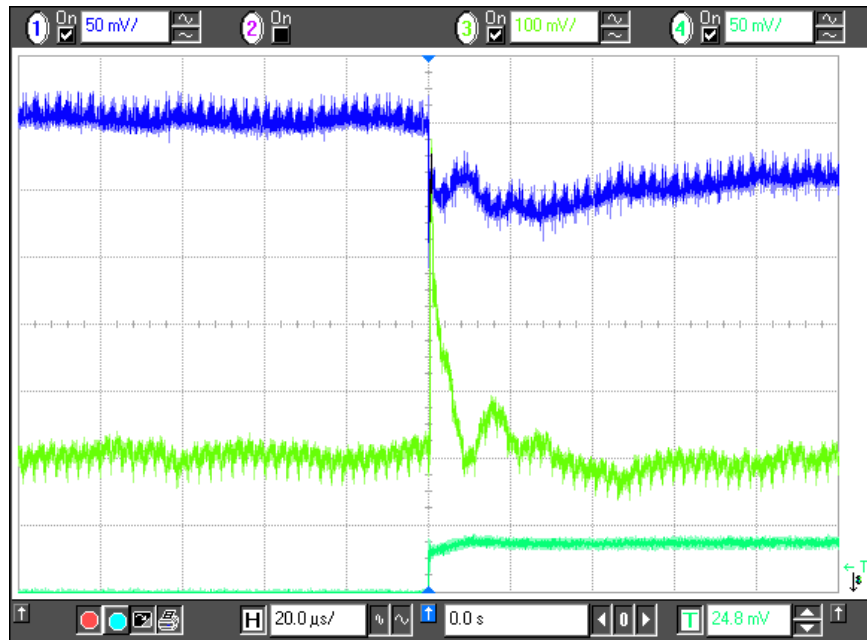
Figure 4.18: Step response with fixed-gain feedforward (large value). Top: v_o, middle: i_{ff}, and bottom: i_o.
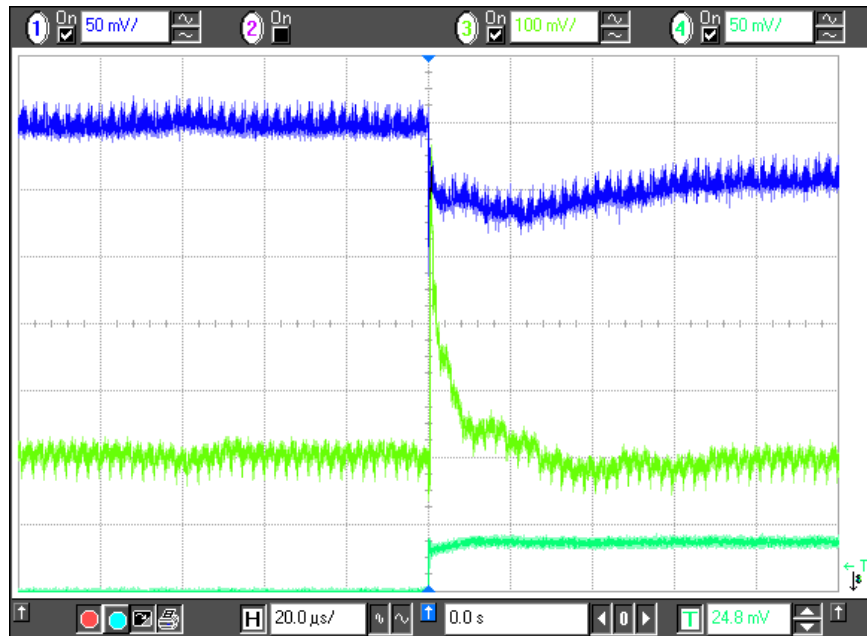
Figure 4.19: Step response with adaptive feedforward. Top: v_o, middle: i_{ff}, and bottom: i_o.

reasons, it is very important to reduce the delay to the minimum, selecting adequate ADCs and optimizing the digital computation for the lowest latency.

4.5 Conclusions

In this chapter, an adaptive control method was presented that tunes the gain of an output current feedforward path in VRM applications. The adaptation method is based on a gradient search that uses the correlation between the voltage error and the feedforward signal to minimize the parameter error. Convergence of the method is guaranteed as long as the output current changes sufficiently to excite the adaptation system. Once the parameter error converges to zero the feedforward path is tuned and no additional excitation is necessary.

The method was implemented digitally in an FPGA. Experimental results show a substantial improvement in the transient response of a VRM prototype board with respect to control systems with only feedback and with fixed but detuned feedforward.

Part II

Impedance Interactions in DC

Distributed Power Systems

Chapter 5

Impedance Interactions: An Overview

5.1 Introduction

In this chapter, interconnections among DC power distribution subsystems are analyzed, and an investigation is launched into how the performance of the global interconnection differs from that predicted by the analysis of each independent subsystem. Typical examples of these interconnections are a power converter with a dynamic load, a power converter with an input line filter, power converters connected in parallel or cascade, and combinations of the above.

Most of the literature on the subject is focused on the problem of a power con-

verter in the presence of an input filter, but more recently the same ideas are being applied in the context of DC Distributed Power Systems (DPS). Every interface in any interconnection of power converters, filters and/or loads is subject to impedance interactions. This is the case of DPS, in particular the Intermediate Bus Architecture (IBA) in which an off-line converter provides a mildly regulated DC line that is distributed among subsystems, with Point-Of-Load (POL) converters providing voltage regulation in close proximity to the loads. Typical applications for this architecture are communications systems, data centers, motherboards, and even on-chip power distribution networks.

A typical diagram for a DPS is shown in Fig. 5.1. One or more AC/DC converters with Power Factor Correction provide an intermediate DC voltage from the same or potentially different AC sources. A battery can be present for power backup. Many POL converters with their respective EMI filters feed independent or shared loads. Some loads could even be connected to the intermediate bus directly. In this diagram, it can be appreciated that interfaces marked as A, B, and C are prone to impedance interactions and potential performance degradation.

The state of the art is such that it is very simple to check the overall performance and stability of an already engineered system by simulation or experimentation. This is usually a system integrator's job. If a problem is encountered, there is little possibility of modifying the internal dynamics of the converters. As a consequence, the most
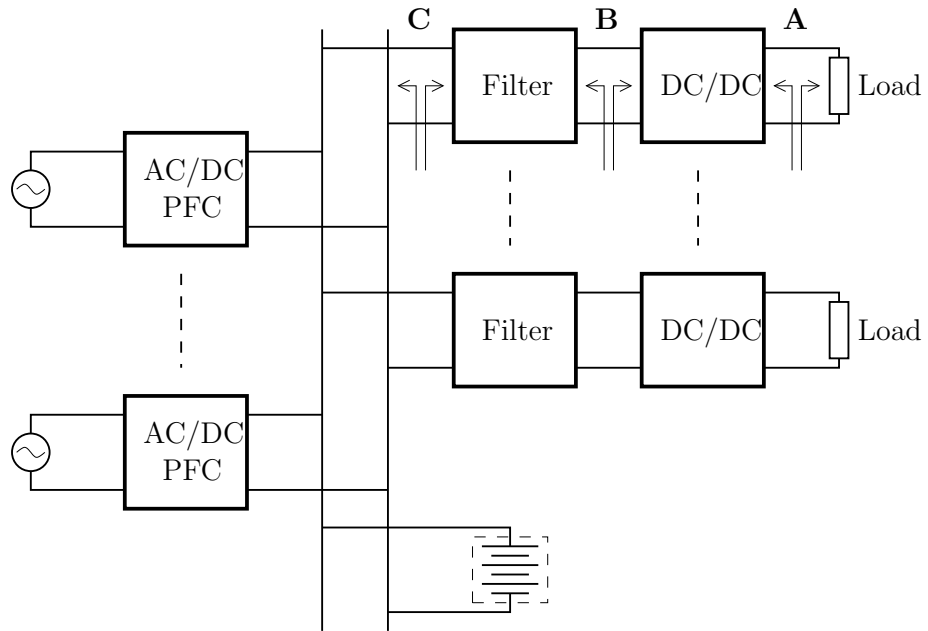
Figure 5.1: Typical DPS diagram.

likely outcome of this process is that the filters become oversized, by the addition of capacitors, inductors, damping, or some combination of these.

A literature review as well as an exposition of the most important aspects of this subject are presented first in this chapter. In the following chapter, a contribution to the understanding of this problem using fundamentals of control systems theory is developed and the feasibility of reducing impedance interactions by control methods instead of physical design is explored.

5.2   Literature review

It was observed early in the development of the discipline of Power Electronics that certain power converters showed unstable behavior in the presence of an input filter [30]. This problem was analyzed using newly derived averaged models in the mid-seventies [31]. A theoretical understanding of the phenomenon was consolidated and design guidelines were derived in order to guarantee the eradication of the problem in voltage programmed regulators [32]. This contribution is usually referred to as the "Middlebrook criterion". Results were extended for current programmed regulators in [33].

The solution proposed was based on adding damping to the input filter. Optimization procedures were derived in order to minimize the size of the filter, the power dissipation, or some other quantity of interest while still achieving the desired damping [34, 35].

In the eighties an input voltage feedforward scheme was proposed in order to mitigate the effects of the input filter [36, 37]. This method is based on a zero-pole cancellation that is difficult to achieve in practice, even using adaptive methods [38]. This was, however, the first attempt to solve the problem using control methods instead of modifying the physical design of the filter.

A practical overview of the problem of impedance interactions in the context of input filter interactions, with a timeline of key papers can be found in [39].

As scaling in IC technology increased density and speed, DPS were proposed to meet the new power demands [10]. This created new topologies of interconnected power converters and line filters in which impedance interactions at every interface could potentially degrade the performance of the system. Analysis methods were extended and new design guidelines developed for this type of system [40–44].

Recent efforts have been made to measure the impedances online for the sake of analyzing stability and performance degradation due to the interconnection of power modules [45, 46]. These methods allow users to analyze the systems and subsystems without knowledge of internal components.

It has been observed that a power converter is immune to impedance interactions at its input and output ports if it has both an output impedance and a forward-voltage transfer function equal to zero [47]. These conditions are not possible to achieve in practice. A system-level approach has to be undertaken to guarantee an overall stability and performance objective.

5.3   Problem description

Traditionally, a power converter is designed under the assumption that there exists an ideal voltage source at the input, as shown in Fig. 5.2. In this case, it is clear that variations in the input current I_{in} (due to, for example, load variations) will not affect the input voltage V_{in}. It can be said that the input and the output of the converter
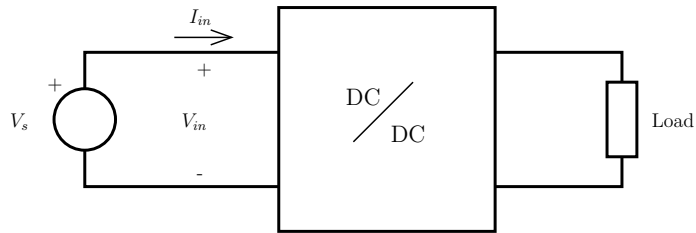
Figure 5.2: DC/DC converter without an input filter.
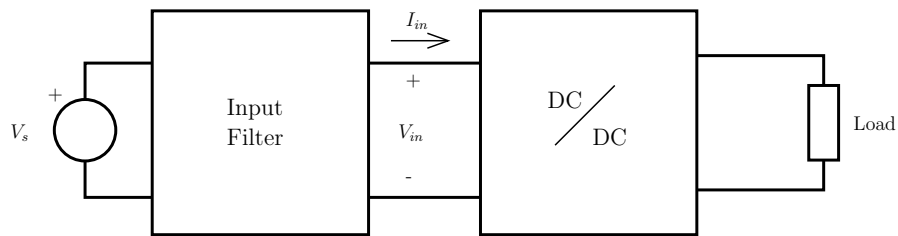
Figure 5.3: DC/DC converter with an input filter.

are "decoupled".

Now consider the system in Fig. 5.3, in which an input filter is added. This input filter can be an EMI filter or the output impedance of another power converter. When I_{in} changes, a perturbation in the input voltage V_{in} will occur due to the output impedance of the input filter. This creates a new feedback loop that can affect significantly the dynamics of the converter, in some cases degrading its performance or even resulting in instability.

The interaction between the impedances can be analyzed by using as an illustrative example the model shown in Fig. 5.4, where Z_o is the output impedance of the input filter, and Z_i is the input impedance of the power converter. The effect of a
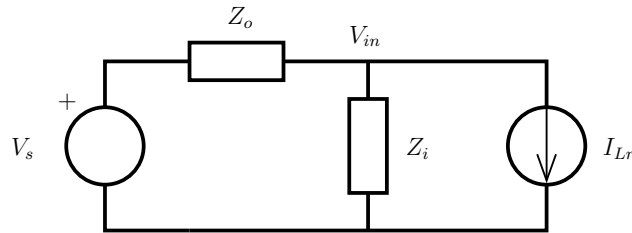
Figure 5.4: Equivalent circuit of a power converter connected to an input filter.

perturbation in the input voltage V_{in} as a function of a change in the load current (reflected to the input of the converter) I_{Lr} is

$$\frac{V_{in}}{I_{Lr}} = -(Z_o \| Z_i) \tag{5.1}$$

$$= -\frac{Z_o}{1 + Z_o Y_i}, \tag{5.2}$$

where $Y_i = \frac{1}{Z_i}$ is the input admittance. This means that a new feedback loop, sometimes called the "small loop", is established. The stability of this loop can be analyzed by applying the Nyquist criterion to $Z_o Y_i$.

In general, the feedback loop created by the connection of two n-ports systems can be analyzed as a MIMO dynamic feedback system. This interpretation is presented in [48] in the context of the small gain theorem, which gives a sufficient condition for the stability of the feedback system. Necessary and sufficient stability conditions for dynamic feedback systems are given in [49]. In the special case of the interconnection of two one-ports which are stable, the feedback system is stable if and only if the zeros of $1 + Z_1 Y_2$ have negative (or zero) real part, where Z_1 and Y_2 are the impedance and

admittance of the two one-ports respectively.

In conclusion, the Nyquist criterion applied to $Z_o Y_i$ as in (5.2) is a necessary and sufficient condition for stability of the interconnection of stable one-ports. This is a very useful result because in practice most of the circuits interconnected in a DPS are stable.

Stability of the interconnection is critical, but from an engineering perspective performance should also be analyzed. Even if the loop is stable, it can still affect significantly the dynamics of the power converter and degrade its performance. The analytical tools for analyzing the performance will be given in the next section.

Example: Buck converter with LC input filter

The ideas exposed above are illustrated here with a simple but important example. Assume a buck converter is controlled such that the output power is constant. This could be the case, for example, if the load is resistive and the converter regulates the output voltage. The closed-loop input impedance over the controller bandwidth is then computed as follows. First, the input power is expressed as a function of the output power and the efficiency:

$$V_{in} I_{in} = \frac{V_o I_o}{\eta}. \tag{5.3}$$
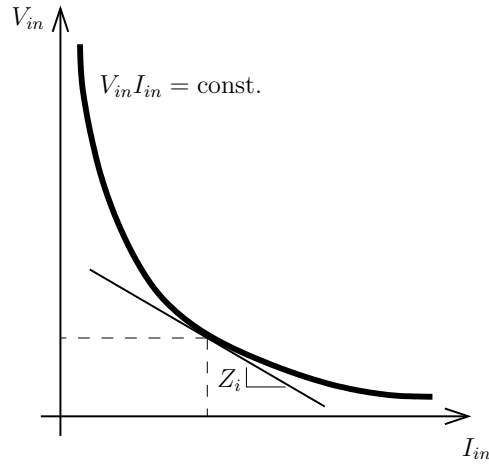
Figure 5.5: Negative input impedance of a constant-power converter.

Then, the small-signal input impedance is computed as the partial derivative of the input voltage with respect to the input current:

$$V_{in} = \frac{V_o I_o}{\eta I_{in}} \tag{5.4}$$

$$\Rightarrow \frac{\partial V_{in}}{\partial I_{in}} = -\frac{V_o I_o}{\eta I_{in}^2}. \tag{5.5}$$

Finally, by substituting $I_{in} = D I_o$ (buck converter) and $\frac{V_o}{I_o} = R_L$ (resistive load), the following result is obtained:

$$Z_i = -\frac{R_L}{\eta D^2}. \tag{5.6}$$

This negative input impedance can be seen graphically in Fig. 5.5 as the slope of the (V_{in}, I_{in}) curve. The impedance depends on the operating point.

Now assume the converter is connected with an LC input filter like the one depicted
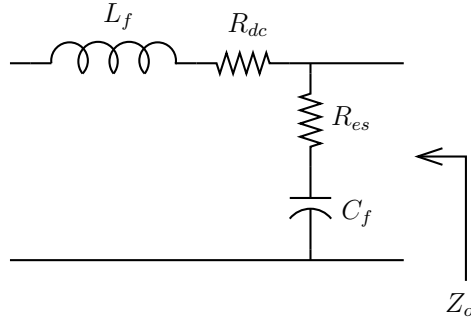
Figure 5.6: Input filter.

in Fig. 5.6. The output impedance of this filter is

$$Z_o = \frac{(L_f s + R_{dc})(R_{es} C_f + 1)}{L_f C_f s^2 + (R_{dc} + R_{es}) C_f s + 1}. \tag{5.7}$$

The stability of the system can be analyzed by computing explicitly the transfer

function (5.2). For simplicity of notation, η is assumed to be equal to unity. Then

$$\frac{V_{in}}{I_{Lr}} = -\frac{Z_o}{1 + Z_o Y_i} \tag{5.8}$$

$$= \frac{-(L_f s + R_{dc})(R_{es} C_f s + 1)}{\left(1 - \frac{D^2 R_{es}}{R_L}\right) L_f C_f s^2 + \left[\left(R_{dc} + R_{es} - \frac{D^2 R_{es} R_{dc}}{R_L}\right) C_f - \frac{D^2 L_f}{R_L}\right] s + 1 - \frac{D^2 R_{dc}}{R_L}} \tag{5.9}$$

Applying the Routh-Hurwitz criterion to the denominator of this expression, a

stability condition can be derived. Usually $\left(1 - D^2 \frac{R_{es}}{R_L}\right)$ and $\left(1 - D^2 \frac{R_{dc}}{R_L}\right)$ are positive.

Assuming the latter, the stability condition can be written as

$$\left(R_{dc} + R_{es} - D^2 \frac{R_{es} R_{dc}}{R_L}\right) C_f - D^2 \frac{L_f}{R_L} > 0 \tag{5.10}$$

$$\Leftrightarrow \quad \frac{R_L}{D^2} > (R_{es} \| R_{dc}) + \frac{Z_C^2}{R_{es} + R_{dc}} \approx Q Z_C \tag{5.11}$$

where $Z_C^2 = \frac{L_f}{C_f}$ and $Q \approx \frac{Z_C}{R_{es} + R_{dc}}$. This is equivalent to say that the magnitude of

the input impedance of the converter has to be larger than the peak of the output impedance of the LC filter at the resonance frequency. This is consistent with the Nyquist criterion, because at that frequency the term $Z_o Y_i$ has an angle of 180° and needs to have a magnitude less than unity in order not to encircle the (-1,0) point.

This example is valid as long as the controller bandwidth of the converter is high enough such that the constant-power assumption holds for the resonant frequency of the LC filter. More exact, but also more complicated results can be obtained by computing the closed-loop input impedance of the converter based on a small-signal model.

5.4   Middlebrook criterion

The Middlebrook criterion is a sufficient condition for guaranteeing the stability of two interconnected systems. Moreover, the criterion also guarantees that no performance degradation occurs due to the interconnection. Following this criterion, the designer can effectively "decouple" one module from its source or load impedance.

The derivation of the criterion can be better understood by applying the Extra Element Theorem (EET) [50]. The EET is used when a transfer function for a system is known and an additional element is connected to one port of the system, modifying the original transfer function. The setup is shown in Fig. 5.7. Suppose the transfer function $T_{u \to y}$ is known when there is no impedance Z connected to the port in system
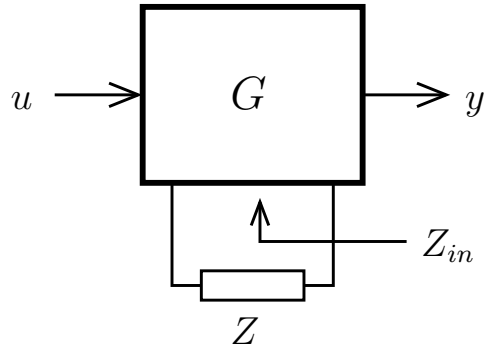
Figure 5.7: The Extra Element Theorem.

G (either $Z = \infty$ or $Z = 0$). When the impedance is connected, this will naturally affect the transfer function. The EET postulates that the new transfer function will be:

$$T_{u \to y}|_Z \quad = \quad T_{u \to y}|_{Z=\infty} \; \frac{1 + \frac{Z_n}{Z}}{1 + \frac{Z_d}{Z}} \qquad\qquad (5.12)$$

$$= \quad T_{u \to y}|_{Z=0} \; \frac{1 + \frac{Z}{Z_n}}{1 + \frac{Z}{Z_d}} \qquad\qquad (5.13)$$

$$\text{where} \qquad Z_n = Z_{in}|_{y \to 0} \qquad\qquad (5.14)$$

$$\text{and} \qquad Z_d = Z_{in}|_{u=0} \qquad\qquad (5.15)$$

The two new quantities that need to be computed are the input impedance of the port under special circumstances. For computing Z_n the input variable u has to be set such that the output variable y vanishes (notice that this is not the same as shorting the output). For computing Z_d the input variable u has to be set to zero.

In the case of a converter with an input filter, the port would be the input port of

the converter and the impedance to add would be the output impedance of the input filter Z_o. Since this impedance is usually assumed to be zero, the effect of a non-zero impedance can be analyzed by using form (5.13) of the EET. The transfer functions of interest would usually be the output impedance of the converter, the duty-cycle to output voltage, or the audio susceptibility transfer functions. The duty-cycle to output voltage transfer function $T_{d \to v_o}$ will be analyzed next as an example.

To compute Z_n the duty cycle has to be set such that the (small signal) output voltage vanishes. This is usually the control objective (voltage regulation), so it can be concluded that Z_n is the ideal closed-loop input impedance of the converter Z_i^{CL} (ideal in the sense that would achieve perfect regulation over all frequencies). To compute Z_d the duty cycle has to be set to zero, which means that the converter operates in open loop. Therefore, Z_d is the open-loop input impedance of the converter Z_i^{OL}. By substituting into (5.13) the following result is obtained:

$$T_{d \to v_o}\big|_{Z_o} = T_{d \to v_o}\big|_{Z_o=0} \frac{1 + \frac{Z_o}{Z_i^{CL}}}{1 + \frac{Z_o}{Z_i^{OL}}} \tag{5.16}$$

This result is exact and predicts the effect of the input filter in the dynamics of the converter. Based on this result, Middlebrook established the simple, although conservative, design rule that is today known as the Middlebrook criterion and can be stated as follows:

> "The dynamics of the converter will not be significantly affected by an input filter if $|Z_o| \ll |Z_i^{CL}|$ and $|Z_o| \ll |Z_i^{OL}|$."
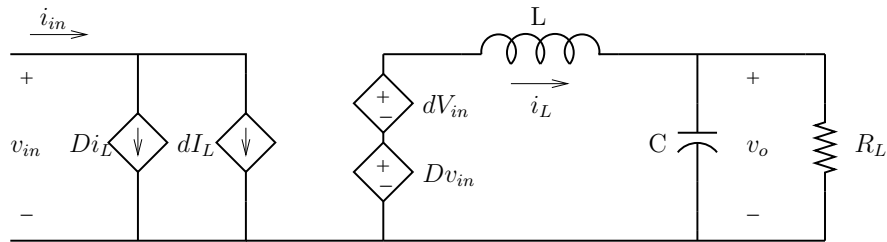
Figure 5.8: Small-signal model of a buck converter with resistive load.

This criterion can be immediately understood by looking at (5.16): the conditions imply that the multiplying term that affects the transfer function is close to unity. If the dynamics are not affected, then clearly stability and performance of the converter are preserved. It is also evident that the criterion is a sufficient condition that can potentially be very conservative.

Example: Applying the EET to a buck converter with input filter

In the case of a buck converter, whose small-signal model is shown in Fig. 5.8, the duty-cycle to output voltage transfer function is:

$$T_{d \to v_o} = \left. \frac{v_o}{d} \right|_{v_{in}=0} = V_{in} \cdot \frac{1}{LCs^2 + \frac{L}{R_L}s + 1}. \tag{5.17}$$

In order to apply the EET, it is necessary to compute the open-loop and ideal closed-loop input impedances. The former is:

$$Z_i^{OL} = \left. \frac{v_{in}}{i_{in}} \right|_{d=0} = \frac{R_L}{D^2} \cdot \frac{LCs^2 + \frac{L}{R_L}s + 1}{R_L Cs + 1}, \tag{5.18}$$

while the latter needs to be computed by setting the duty-cycle such that it cancels

the output voltage, namely $d = -\frac{D}{V_{in}}v_{in}$. Then

$$Z_i^{CL} = \left.\frac{v_{in}}{i_{in}}\right|_{d=-\frac{D}{V_{in}}v_{in}} = -\frac{R_L}{D^2}. \tag{5.19}$$

Finally, we can apply the EET as stated in (5.13) to obtain the duty-cycle to

output voltage transfer function when we connect the input filter of Fig. 5.6:

$$T_{d\to v_o} = V_{in} \cdot \frac{1}{LCs^2 + \frac{L}{R_L}s + 1} \cdot \frac{1 - \frac{D^2}{R_L} \cdot \frac{(L_f s + R_{dc})(R_{es}C_f + 1)}{L_f C_f s^2 + (R_{dc} + R_{es})C_f s + 1}}{1 + \frac{D^2}{R_L} \cdot \frac{R_L Cs + 1}{LCs^2 + \frac{L}{R_L}s + 1} \cdot \frac{(L_f s + R_{dc})(R_{es}C_f + 1)}{L_f C_f s^2 + (R_{dc} + R_{es})C_f s + 1}}. \tag{5.20}$$

After some algebra the expression can be reduced to

$$T_{d\to v_o} = V_{in} \cdot \frac{N(s)}{D(s)} \tag{5.21}$$

where

$$N(s) = \left(1 - D^2\frac{R_{es}}{R_L}\right)L_f C_f s^2 + \left[\left(R_{dc} + R_{es} - D^2\frac{R_{es}R_{dc}}{R_L}\right)C_f - D^2\frac{L_f}{R_L}\right]s + 1 - D^2\frac{R_{dc}}{R_L} \tag{5.22}$$

and

$$
\begin{aligned}
D(s) \;=\; & L_f C_f LC s^4 + \\
& \left[L_f C_f \left(\frac{L}{R_L} + D^2 R_{es}C\right) + (R_{dc} + R_{es})C_f LC\right]s^3 + \\
& \left[L_f C_f \left(1 + D^2\frac{R_{es}}{R_L}\right) + LC + LC_f\frac{R_{dc} + R_{es}}{R_L} + D^2 L_f C + D^2 R_{dc}R_{es}CC_f\right]s^2 + \\
& \left[\left(R_{es} + R_{dc} + D^2\frac{R_{dc}R_{es}}{R_L}\right)C_f + \frac{L + D^2 L_f}{R_L} + D^2 R_{dc}C\right]s + \\
& 1 + D^2\frac{R_{dc}}{R_L}.
\end{aligned} \tag{5.23}
$$

Although the denominator of the expression does not add much insight into the problem, the numerator shows an interesting fact. Comparing (5.22) with the denominator in (5.9), it can be concluded that the zeros of the duty-cycle to output voltage transfer function are equal to the poles of the closed-loop transfer function computed in the previous section under the assumption of perfect regulation. This is consistent with control theory results, namely that under the condition of infinite feedback gain the poles of the closed-loop transfer function are equal to the zeros of the plant. More importantly, this example shows that instability of the closed-loop system is related to the existence of right half-plane zeros in the plant, and that those zeros are introduced by the input filter.

An illustration of the effect of an input filter in the dynamics of a buck converter is shown in Fig. 5.9. The top two graphs show the bode plots in the case of a damped input filter. Since $|Z| \ll |Z_n|, |Z_d|$ (i.e., the Middlebrook criterion is satisfied) the plant transfer function $T_{d \to v_o}$ presents its characteristic second-order shape, unaffected by the input filter. The bottom two graphs show the case of an undamped (or lightly damped) input filter. The plant transfer function shows the effect of the input filter resonance, leading potentially to a degradation of performance and even instability.
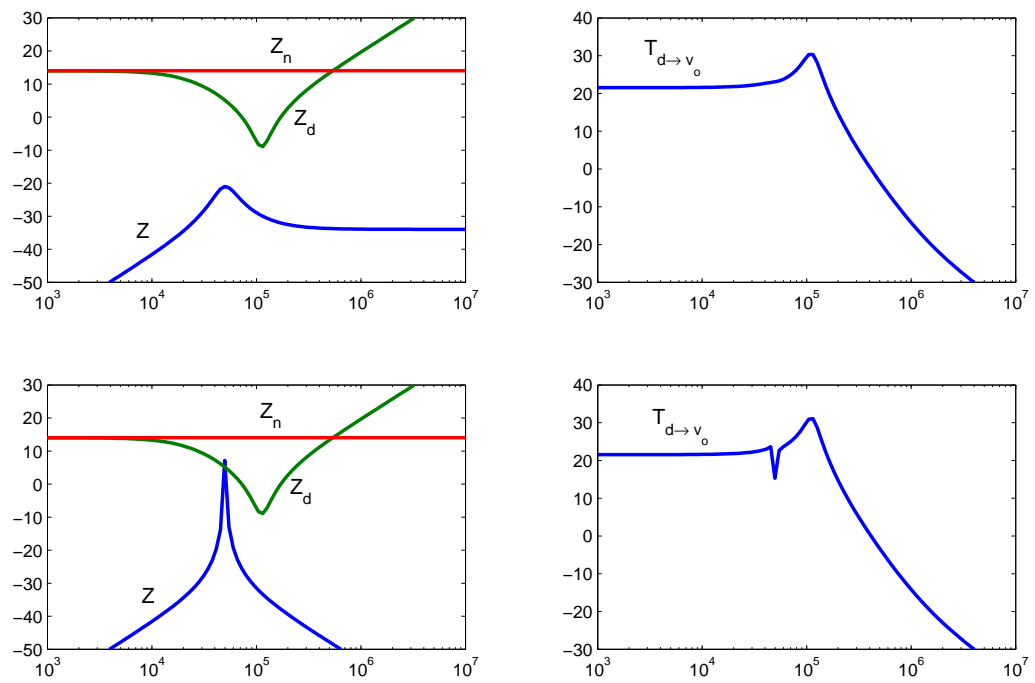
Figure 5.9: Effect of input filter in buck converter dynamics. Top: Damped input filter. Bottom: Undamped input filter.

5.5 Modeling

When designing the control system of a power converter, it is standard practice to derive a small-signal model and from there extract the transfer functions of interest, for example the duty-cycle to output voltage transfer function, duty-cycle to inductor current transfer function, output impedance, etc. If the converter is connected to a source or load impedance these transfer functions are not valid any longer, as explained in the previous sections. There are many ways to deal with this:

1. Assume the Middlebrook criterion is valid and ignore impedance interactions.

2. Derive the new transfer functions using the extra-element theorem (EET).

3. Include the impedance in the small-signal model and derive the transfer functions for the new model.

In the design process, the first option is probably the only feasible one, since the complexity of the other approaches is too high for a designer. However, if the purpose is to simulate and validate a controller design, there is no need to recompute the transfer functions. A two-port model of the converter, based on the small-signal model, can be derived and connected to the impedance for simulation.

Any type of two-port model would work, however the nature of DC/DC power converters is such that in closed loop it is more useful to see the input voltage and output current as independent variables ("inputs" to the system), while the input
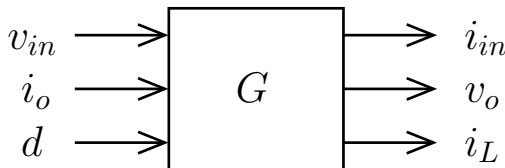
Figure 5.10: DC/DC converter model.

current and output voltage are dependent variables ("outputs" of the system). This leads naturally to a hybrid parameter model. In two-port models in which one of the ports can be naturally identified as "input" and the other as "output", some authors make the distinction between the two possible types of hybrid models that can arise. Following this convention, the so-called inverse-hybrid parameter, or G-parameter model was proposed [51, 52]. A derivation of this type of two-port model is shown next.

Suppose the converter has a small-signal (linear), multivariable model G depicted in Fig. 5.10. The inputs are the input voltage v_{in}, the output or load current i_o, and the duty-cycle d. The outputs are the input current i_{in}, the output voltage v_o, and the inductor current i_L. (The latter is useful in the context of current-mode control, otherwise it could be obviated.)

This system can be completely described by the following set of equations:

$$\begin{cases} i_{in} &=& G_{iv}v_{in} + G_{ii}i_o + G_{id}d \\ v_o &=& G_{vv}v_{in} + G_{vi}i_o + G_{vd}d \\ i_L &=& G_{Lv}v_{in} + G_{Li}i_o + G_{Ld}d \end{cases} \tag{5.24}$$
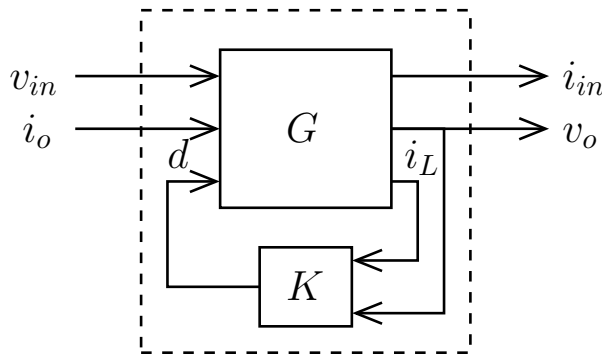
Figure 5.11: DC/DC converter model with feedback controller K.
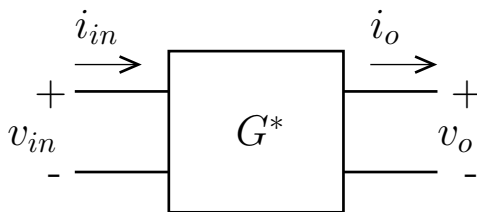
Figure 5.12: Two-port model of a closed-loop DC/DC converter.

When a feedback controller K is connected (Fig. 5.11), the closed-loop converter becomes a two-input, two-output system that can be represented as a two-port system (Fig. 5.12). Here the system G^* represents the closed-loop converter. The system can be described by the following set of equations:

$$\begin{cases} i_{in} & = & G_{iv}^* v_{in} + G_{ii}^* i_o \\ \\ v_o & = & G_{vv}^* v_{in} + G_{vi}^* i_o \end{cases} \tag{5.25}$$

For simulation purposes, however, the transfer functions of the closed-loop description do not need to be computed. An internal description like the one inside the dashed box in Fig. 5.11 can be used. A less compact, but more realistic circuit
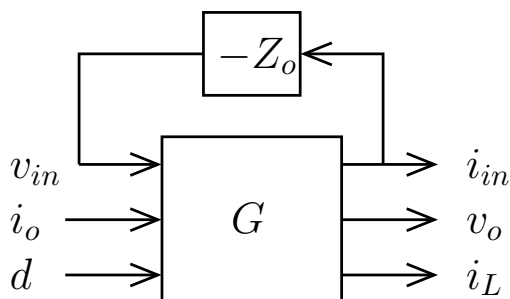
Figure 5.13: DC/DC converter with input filter. Multivariable model case.

description, like the one in Fig. 5.8 can also be used, although in some systems it could consume more computational resources.

The advantage of two-port models arises when subsystems need to be interconnected, in particular when there are many subsystems in series or parallel. For example, consider a converter with an input filter. In the multivariable model of Fig. 5.10, the filter could be accommodated by including a feedback loop with the output impedance of the filter Z_o, as depicted in Fig. 5.13. It is assumed that the only small-signal perturbation at the input of the converter is due to perturbations in the input current, interacting with the output impedance of the filter.

Now, suppose the input filter is connected to the output of another converter, for example an AC/DC converter. To include the effect of this cascaded interconnection, it would be required to compute the output impedance of the filter under the presence of the AC/DC converter, and then to substitute this value instead of Z_o in the figure. For every additional subsystem interconnected to the network, all impedances need
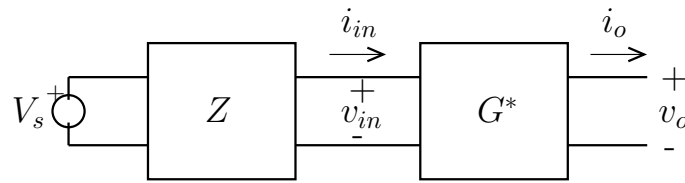
Figure 5.14: DC/DC converter with input filter. Two-port model case.

to be recomputed.

Compare this scenario with the two-port model case. The input filter can be included using its own two-port model Z as shown in Fig. 5.14, and its input port connected to a DC voltage source V_s, or equivalently a short circuit.

If a new converter is connected to the input of the filter, the voltage source can be replaced by the output port of this new converter and no modifications are needed to the filter model. No matter how complex the interconnections, the two-port model allows for a topological connection that is identical to the circuit without needing to recompute any of the models. Hence, it can be concluded that two-port models are more convenient than multivariable models for simulation and verification of interconnected systems.

It should be noted, though, that the small-signal model described so far depends on the (large-signal) operating point of the converter. Therefore, when the converter is connected to a load or a source impedance that changes the operating point, the converter model needs to be recomputed. The general form of the equations, though, does not change because only the values of some parameters are modified.
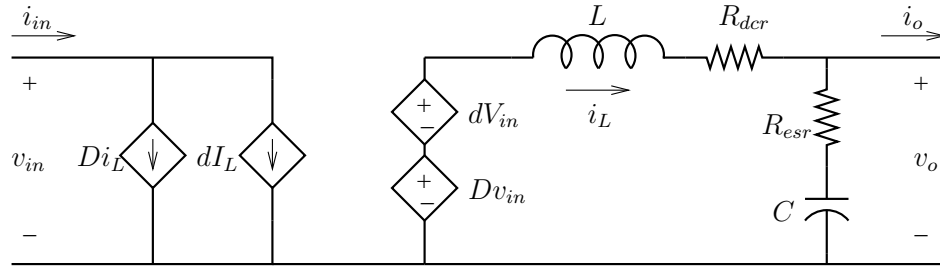
Figure 5.15: Small-signal model of buck converter with parasitic resistances.

Example: Two-port model of a buck converter

In the case of a buck converter, the traditional averaged small-signal model as shown in Fig. 5.8 (without the load resistance R_L) is simple enough to be used in simulations as a two-port model. The canonical G-parameter model is derived here for completeness. The parasitic resistances of the inductor and the switches (R_{dcr}), and the capacitor (R_{esr}) are also included in the derivation. The small-signal model of reference is shown in Fig. 5.15.

There are nine transfer functions to be derived in accordance with (5.24). These are:

$$G_{iv} = \left.\frac{i_{in}}{v_{in}}\right|_{d=i_o=0} = D^2 \cdot \frac{Cs}{LCs^2 + (R_{dcr} + R_{esr})\,Cs + 1} \tag{5.26}$$

$$G_{ii} = \left.\frac{i_{in}}{i_o}\right|_{v_{in}=d=0} = D \cdot \frac{R_{esr}Cs + 1}{LCs^2 + (R_{dcr} + R_{esr})\,Cs + 1} \tag{5.27}$$

$$G_{id} = \left.\frac{i_{in}}{d}\right|_{v_{in}=i_o=0} = I_o \cdot \frac{LCs^2 + \left(R_{dcr} + R_{esr} + \frac{V_o}{I_o}\right)Cs + 1}{LCs^2 + (R_{dcr} + R_{esr})\,Cs + 1} \tag{5.28}$$

$$G_{vv} = \left.\frac{v_o}{v_{in}}\right|_{d=i_o=0} = D \cdot \frac{R_{esr}Cs + 1}{LCs^2 + (R_{dcr} + R_{esr})\,Cs + 1} \tag{5.29}$$
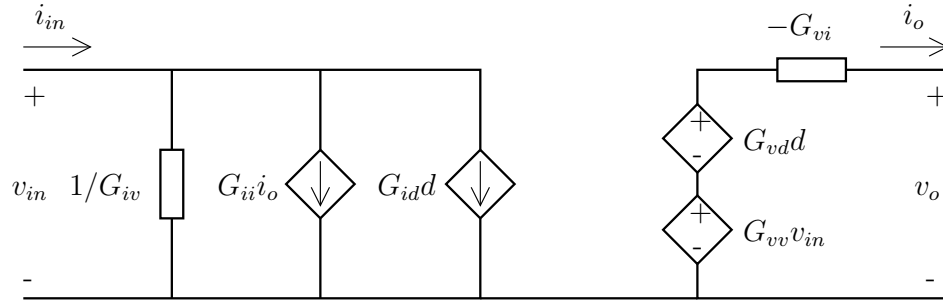
Figure 5.16: Implementation of the G-parameter two-port model. Open-loop case.

$$G_{vi} = \left.\frac{v_o}{i_o}\right|_{v_{in}=d=0} = \frac{(Ls + R_{dcr})(R_{esr}Cs + 1)}{LCs^2 + (R_{dcr} + R_{esr})Cs + 1} \tag{5.30}$$

$$G_{vd} = \left.\frac{v_o}{d}\right|_{v_{in}=i_o=0} = V_{in} \cdot \frac{R_{esr}Cs + 1}{LCs^2 + (R_{dcr} + R_{esr})Cs + 1} \tag{5.31}$$

$$G_{Lv} = \left.\frac{i_L}{v_{in}}\right|_{d=i_o=0} = D \cdot \frac{Cs}{LCs^2 + (R_{dcr} + R_{esr})Cs + 1} \tag{5.32}$$

$$G_{Li} = \left.\frac{i_L}{i_o}\right|_{v_{in}=d=0} = \frac{R_{esr}Cs + 1}{LCs^2 + (R_{dcr} + R_{esr})Cs + 1} \tag{5.33}$$

$$G_{Ld} = \left.\frac{i_L}{d}\right|_{v_{in}=i_o=0} = V_{in} \cdot \frac{Cs}{LCs^2 + (R_{dcr} + R_{esr})Cs + 1} \tag{5.34}$$

The circuit representation of this model is shown in Fig. 5.16. The feedback loop can be incorporated with an additional circuit that generates the duty-cycle d. If current-mode control is used, the current i_L can be generated using (5.32–5.34).

This example shows a method to derive a canonical two-port model for a DC/DC converter. In closed-loop operation, a canonical model can also be obtained by trivial (although complicated) algebraic manipulations. In practice, the model could also be extracted from measurements. This means that a canonical model for a converter operating in closed-loop can be obtained from measurements even when the internal
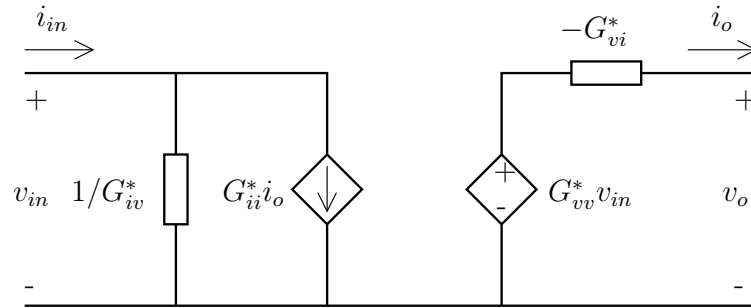
Figure 5.17: Implementation of the G-parameter two-port model. Closed-loop case.

characteristics are unknown ("black box"). The transfer functions to be obtained, according to (5.25) are only four, namely:

$$G_{iv}^* \;=\; \left.\frac{i_{in}}{v_{in}}\right|_{i_o=0} \quad \text{(input admittance)} \tag{5.35}$$

$$G_{ii}^* \;=\; \left.\frac{i_{in}}{i_o}\right|_{v_{in}=0} \quad \text{(inverse current gain)} \tag{5.36}$$

$$G_{vv}^* \;=\; \left.\frac{v_o}{v_{in}}\right|_{i_o=0} \quad \text{(voltage gain)} \tag{5.37}$$

$$G_{vi}^* \;=\; \left.\frac{v_o}{i_o}\right|_{v_{in}=0} \quad \text{(output impedance)} \tag{5.38}$$

The equivalent circuit is shown in Fig. 5.17. A system integrator could benefit from this approach when all or most of the subsystems in a DPS are modules whose internal behavior is unknown. Each one of them can be characterized by measuring these four transfer functions and the overall performance of the system can be predicted by simulation.

5.6   Conclusions

In this chapter, the problem of impedance interactions between interconnected power converters and/or passive circuits was presented. The basic results in this area were described, as well as the context in which the results were developed. A buck converter with an input filter was used as a representative example to illustrate the main ideas.

The next chapter will address this problem from a different perspective, exploring the fundamental issues that arise in this area and the feasibility of using control methods to preserve performance and stability of interconnected systems.

Chapter 6

Mitigation of Impedance

Interactions

In this chapter, the possibility of improving the performance of interconnected power converters and/or filters by using control methods instead of physical design is explored. First, some fundamental limitations are exposed. Different controller design methods are explored and compared. Finally, an example of the use of system-level design to mitigate impedance interactions is presented.

6.1 Limits of performance

It has been observed that an undamped input filter adds a pair of complex-conjugate right-half plane zeros to the duty-cycle to output transfer function of the

converter [35]. This observation is in accordance with the example shown in Section 5.4.

A RHP zero in the feedback loop is known to impose serious limits in the achievable performance of the closed-loop control system [53]. In general, the loop bandwidth should be less than half the frequency of the zero in order to preserve stability.

In many applications, the resonant frequency of the input filter is less than the resonant frequency of the output filter, which in turn is less than the desired bandwidth. As a consequence, the RHP zeros introduced by the input filter will invariably cause instability in closed-loop operation. It can be concluded that, under the presence of the RHP zeros, the performance requirements of the application (expressed, for example, as a high loop gain over the desired bandwidth) are not compatible with stable operation. It is for this reason that the most common solution to the problem is the addition of damping to the input filter, which moves the zeros from the RHP to the LHP.

When considering a power converter with an input filter, the converter's input voltage changes with its input current as described in the previous chapter. This voltage could be used as a controller input. In this case the controller would have two inputs (output voltage and input voltage) and one output (duty-cycle). In a MIMO system like this, the role of zeros is not as straightforward as in the SISO case because there is a spatial direction added to the frequency dimension. In particular, the limits

of performance imposed by RHP zeros are more difficult to analyze [54].

Therefore, the RHP zeros in traditional output voltage feedback control impose a fundamental limitation in the performance of the system, but more caution should be taken when discussing control with input voltage feedforward. In this chapter, although no definitive answer is attempted in this regard, an exploration of a large set of controllers with input voltage feedforward seems to indicate that the same limits of performance for SISO systems are valid in the MIMO case for this application.

6.2   Robust design of controllers

In this section, a robust design procedure is introduced in order to explore possible control schemes that could meet the performance and stability requirements of a representative VRM application under the presence of an input filter. It is shown that there is no stabilizing controller that can achieve high loop gain at the resonant frequency of the input filter.

The section is organized as follows. First, a model of the plant (a buck converter with an input filter) is presented in Section 6.2.1. The model includes uncertainty in the characteristics of the input filter. In Section 6.2.2, the plant is analyzed using the Middlebrook criterion (introduced in Section 5.4), revealing that for some parameter values the criterion is not satisfied and RHP zeros are introduced. A traditional PID control design is presented in Section 6.2.3 and its stability is analyzed. In

Section 6.2.4 input voltage feedforward is introduced, showing stable operation with nominal parameters but instability for some parameter values. A μ-synthesis design is presented in Section 6.2.5 that aims to find a controller that could achieve both stability and good performance under the presence of uncertain parameters in the input filter. Finally, in Section 6.2.6, conclusions are presented.

6.2.1　The plant

A diagram of the control system of a DC/DC converter using voltage mode control is shown in Fig. 6.1. The box labeled G represents the dynamics of the converter. The small-signal input voltage is generated by the presence of an input filter of output impedance Z_o. Adaptive Voltage Positioning (AVP) is achieved by subtracting the reference impedance Z_{ref} times the output current i_o from the reference voltage v_r. As an example, the generalized output impedance approach as defined in [9] is used, meaning that

$$Z_{ref} = R_{LL} \cdot \frac{R_{esr}Cs + 1}{R_{LL}Cs + 1} \tag{6.1}$$

The box labeled K corresponds to the controller that generates the duty-cycle command d based on the error voltage v_e. An input voltage feedforward path is included also in order to explore a richer set of controllers.

The converter's model can be obtained based on (5.26–5.31). However, in this chapter a resistive load R_L is also included in order to explore different operating
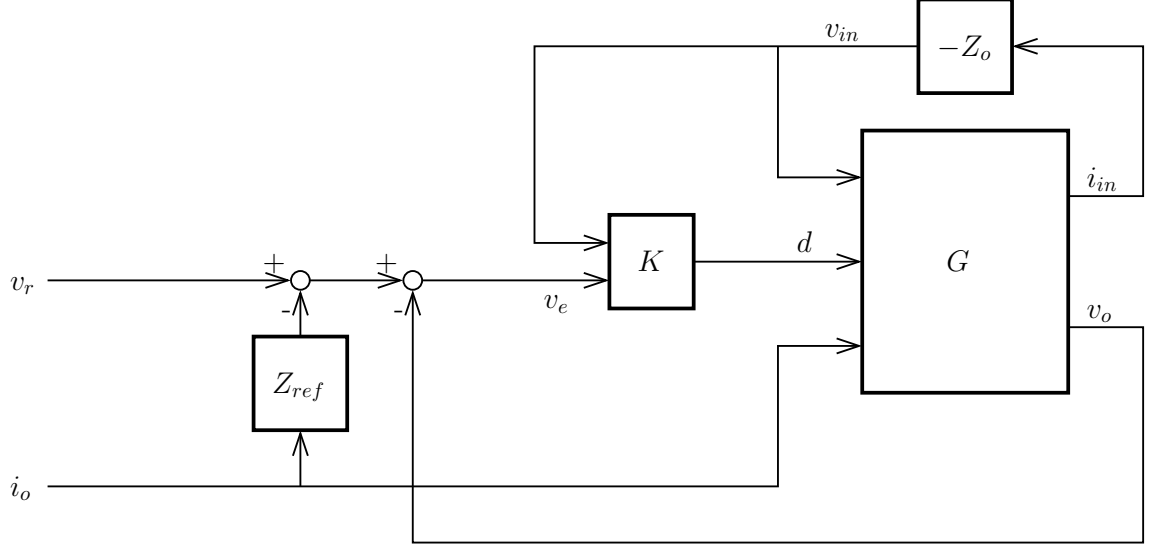
Figure 6.1: Voltage mode control of a DC/DC converter with load-line and input voltage feedforward, in the presence of an input filter.

conditions. This generates a "terminated" model, in which the following transfer functions define block G according to Fig. 6.2:

$$G_{iv} = \frac{D^2}{R_{dcr} + R_L} \cdot \frac{(R_{esr}Cs + 1)}{\frac{R_{esr}+R_L}{R_{dcr}+R_L}LCs^2 + \frac{(R_{dcr}R_L+R_{esr}R_L+R_{esr}R_{dcr})C+L}{R_{dcr}+R_L}s + 1} \tag{6.2}$$

$$G_{ii} = D \cdot \frac{R_L}{R_{dcr} + R_L} \cdot \frac{R_{esr}Cs + 1}{\frac{R_{esr}+R_L}{R_{dcr}+R_L}LCs^2 + \frac{(R_{dcr}R_L+R_{esr}R_L+R_{esr}R_{dcr})C+L}{R_{dcr}+R_L}s + 1} \tag{6.3}$$

$$G_{id} = \frac{DV_{in}}{R_{dcr} + R_L} \cdot \left(1 + \frac{(R_{esr} + R_L)Cs + 1}{\frac{R_{esr}+R_L}{R_{dcr}+R_L}LCs^2 + \frac{(R_{dcr}R_L+R_{esr}R_L+R_{esr}R_{dcr})C+L}{R_{dcr}+R_L}s + 1}\right) \tag{6.4}$$

$$G_{vv} = D \cdot \frac{R_L}{R_{dcr} + R_L} \cdot \frac{R_{esr}Cs + 1}{\frac{R_{esr}+R_L}{R_{dcr}+R_L}LCs^2 + \frac{(R_{dcr}R_L+R_{esr}R_L+R_{esr}R_{dcr})C+L}{R_{dcr}+R_L}s + 1} \tag{6.5}$$

$$G_{vi} = -\frac{R_L}{R_{dcr} + R_L} \frac{(Ls + R_{dcr})(R_{esr}Cs + 1)}{\frac{R_{esr}+R_L}{R_{dcr}+R_L}LCs^2 + \frac{(R_{dcr}R_L+R_{esr}R_L+R_{esr}R_{dcr})C+L}{R_{dcr}+R_L}s + 1} \tag{6.6}$$

$$G_{vd} = V_{in} \cdot \frac{R_L}{R_{dcr} + R_L} \cdot \frac{R_{esr}Cs + 1}{\frac{R_{esr}+R_L}{R_{dcr}+R_L}LCs^2 + \frac{(R_{dcr}R_L+R_{esr}R_L+R_{esr}R_{dcr})C+L}{R_{dcr}+R_L}s + 1} \tag{6.7}$$

For a representative VRM application, the component and parameter values are
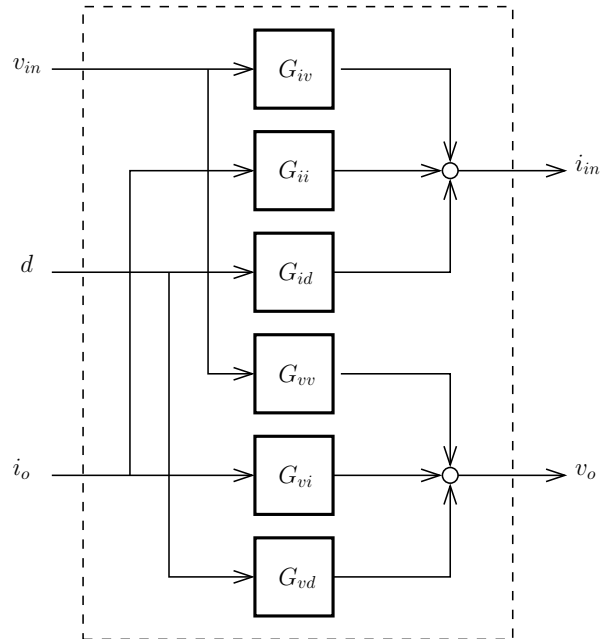
Figure 6.2: Internal structure of block G.

presented in Table 6.1. The table also includes the specification of the load-line R_{LL}

and the range of output currents. The switching frequency and the desired bandwidth

are also specified. The input filter corresponds to the one shown in Fig. 5.6. Table 6.2

shows the filter component values. In both tables, the range of variation for selected

parameters is also indicated. The purpose of this study is to analyze the effect of

the input filter on the dynamics of the converter, therefore only the filter parameters

and the operating point are allowed to change, while the converter parameters are

assumed constant. In order to simplify the formulation, the frequency and damping

of the input LC filter are changed by variations in the capacitor's parameters only.

Table 6.1: Representative VRM application values

Component/Parameter	Nominal Value	Range of Variation
V_{in}	$12V$	$10 - 13V$
V_{ref}	$1.2V$	$0.8 - 1.3V$
L	$100nH$	
R_{dcr}	$1m\Omega$	
C	$800\mu F$	
R_{esr}	$1m\Omega$	
R_{LL}	$1.25m\Omega$	
I_o	$100A$	$1 - 120A$
f_s	$1MHz$	
BW	$80kHz$	

Table 6.2: Input filter values

Component	Nominal Value	Range of Variation
L_f	$800nH$	
R_{dc}	$0.1m\Omega$	
C_f	$500\mu F$	$200 - 3,000\mu F$
R_{es}	$1m\Omega$	$.2 - 20m\Omega$

6.2.2   Preliminary analysis

Applying the Middlebrook criterion to this system, it can be seen that the stability conditions are not met for some input filter parameters in the range specified. This is illustrated in Fig. 6.3, showing the Bode plots of the input impedance of the converter G_{iv}^{-1} at a high-load condition and the output impedance of the input filter Z_o. A set of plots for Z_o are shown corresponding to a representative set of input filter parameter variations. The input filter resonance is not damped enough in some cases and the peak becomes larger than the input impedance of the converter. It is expected, from previous analysis, that the system would be unstable if the bandwidth of the loop is above the input filter resonance for those particular sets of parameters.

This problem formulation is a good candidate to explore to what extent the use of input voltage feedforward and robust design techniques could overcome the fundamental limit of performance observed in the traditional SISO controller design.

6.2.3   PID feedback design

In this design, the controller K shown in Fig.6.1 has the feedforward path from v_{in} to d equal to zero, and the feedback path from v_e to d is designed using standard control techniques. The input filter is assumed to be absent, implying that the loop to be designed is formed by the series connection of the controller K and the duty-cycle to output voltage transfer function G_{vd}, which will be referred to as "the plant". The
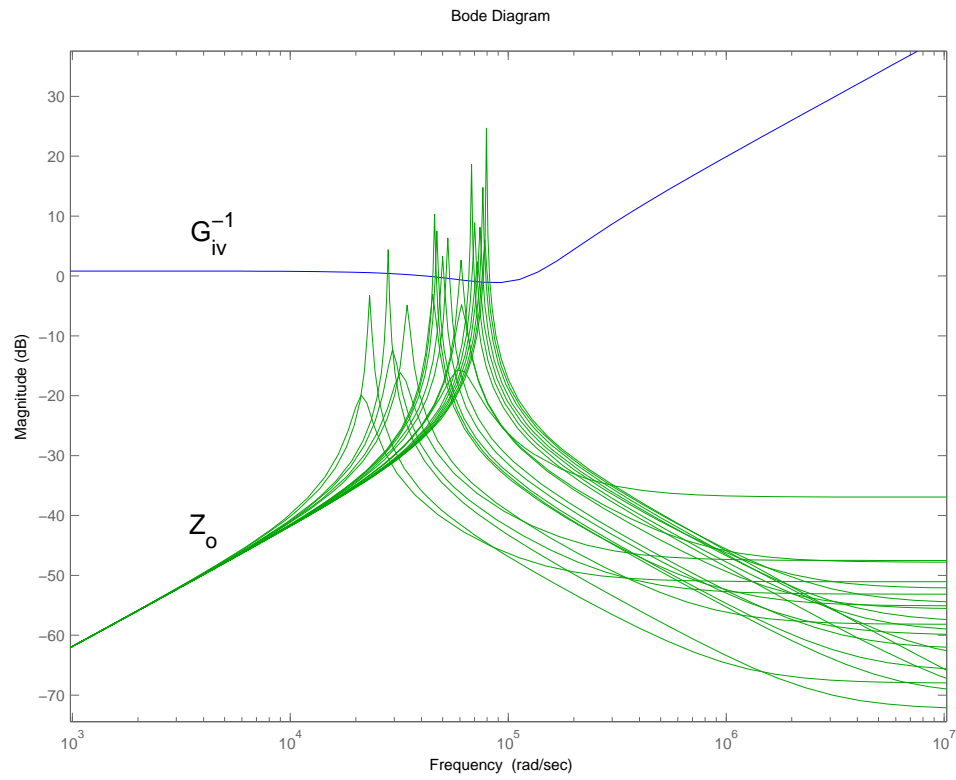
Figure 6.3: Magnitude of the input impedance of the converter G_{iv}^{-1} compared with the magnitude of the output impedance of the filter Z_o for a set of different parameter values.
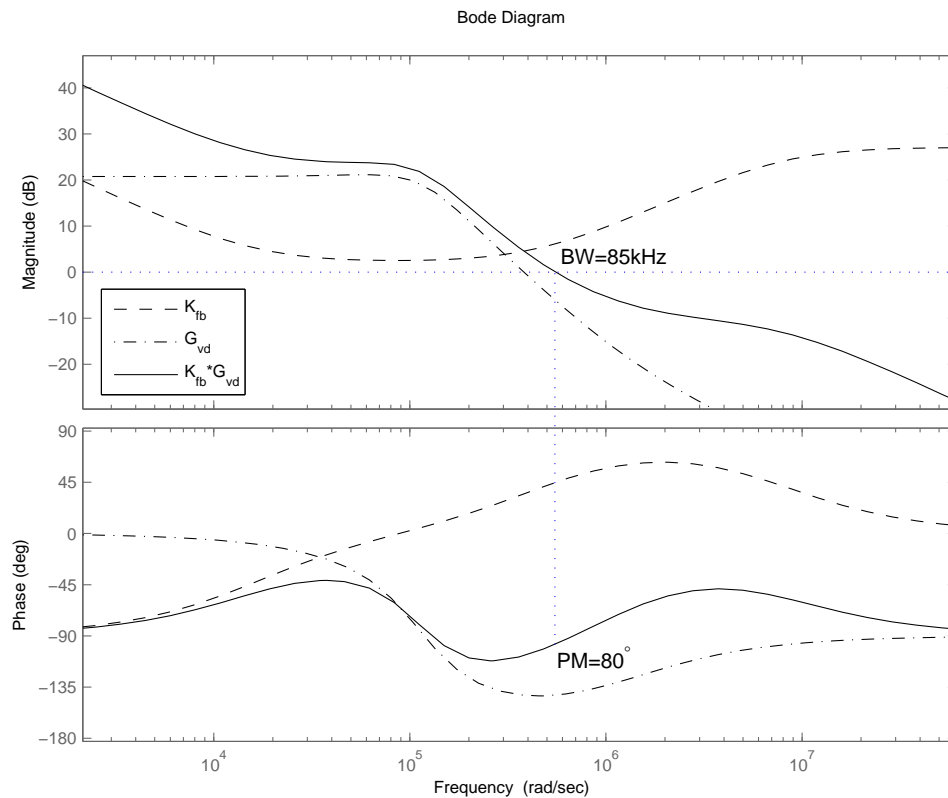
Figure 6.4: Feedback PID design. Bode plot of the controller (dashed line), the plant (dash-dotted line), and the resulting loop gain (solid line).

design is performed under the most demanding situation, which is at high load.

The PID controller has one pole at the origin, two zeros located in the proximity of the plant's double pole, and an additional pole located in proximity to the ESR zero introduced by the output capacitor. The Bode plot of the controller, the plant, and the loop are shown in Fig. 6.4. The bandwidth is around $85kHz$ and the phase margin 80°.

The design appears to be adequate, however when the input filter is connected
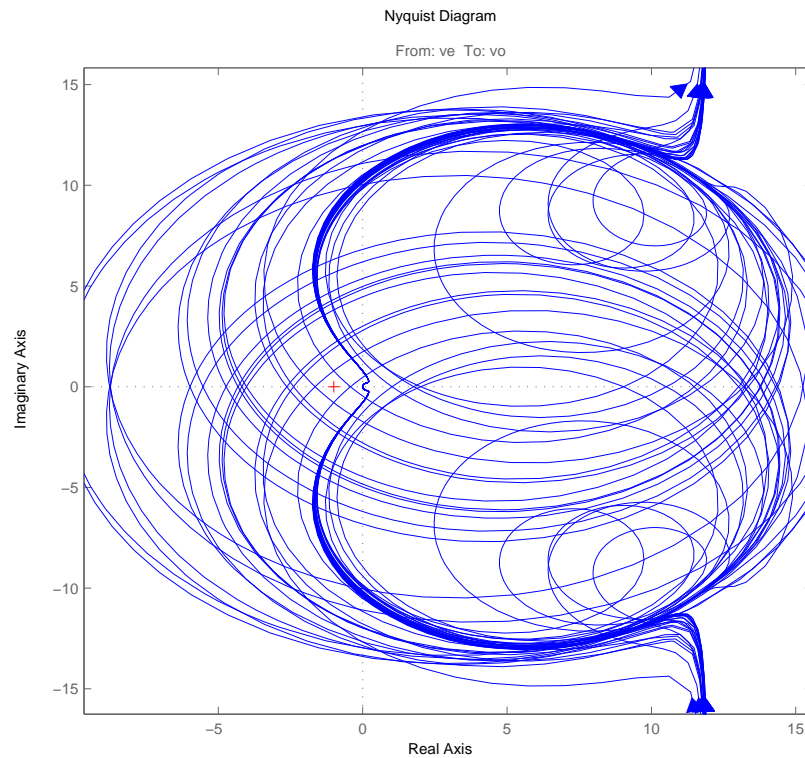
Figure 6.5: Set of Nyquist plots of the feedback PID design for different input filter parameters.

and the new loop gain computed (for example, using the extra-element theorem), instability is revealed in the set of Nyquist plots of Fig. 6.5. For each input filter parameter value set, a different Nyquist plot is shown. Some of the plots encircle the $(-1, 0)$ point, revealing instability. This is not surprising, since it was predicted in the previous section.

6.2.4   Input voltage feedforward

This design is based on that in [36]. The feedback controller is the same PID as in the previous section, but an input voltage feedforward path equal to $-\frac{D}{V_{in}}$ is added. The controller K, as shown in Fig. 6.1 has now two inputs and one output. This ideally cancels out the effect of any input filter in the loop gain. However, this is equivalent to a RHP zero-pole cancellation that hides the instability such that it is not observed at the output. A slight deviation from the ideal conditions reveals the instability in the output of the system.

The Nyquist plot of the loop under variations in the input filter is shown in Fig. 6.6. Comparing with Fig. 6.5 it can be appreciated that the feedforward term effectively cancels the effect of the input filter in the loop, which appears now to be stable. However, when the input voltage is allowed to change (in addition to the variations in the input filter), the feedforward term is not ideal anymore and the Nyquist plot of the loop becomes the set shown in Fig. 6.7. In this case it can be seen that the system is unstable for some set of parameters in the range of variation, as evidenced by the encirclement of the point $(-1, 0)$.

6.2.5 μ-synthesis design

The examples in the previous sections illustrate that the RHP zeros impose a fundamental limitation in the conventional design of controllers for DC/DC convert-
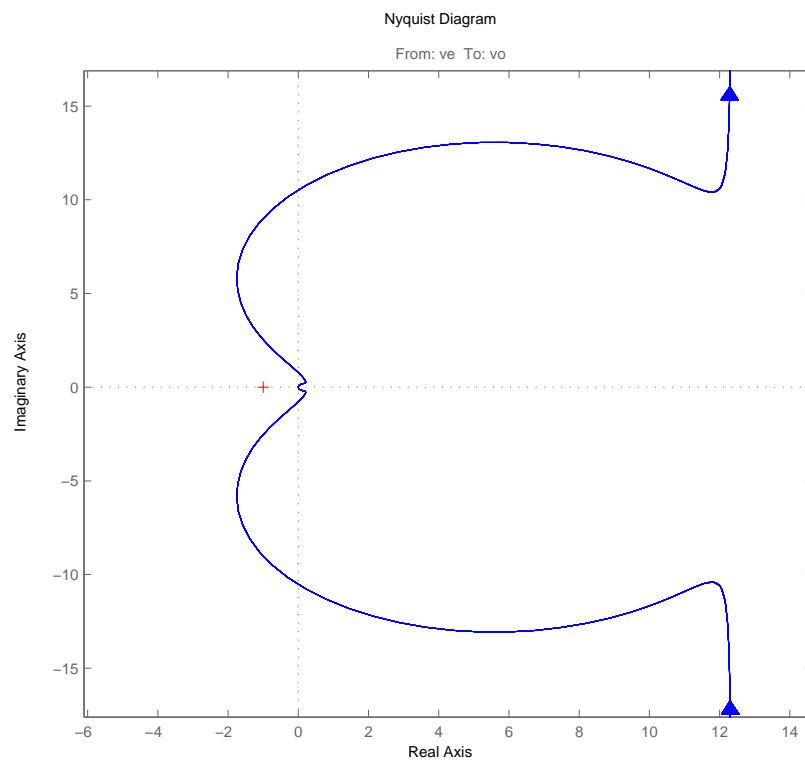
Figure 6.6: Nyquist plot of the feedforward design under ideal conditions.
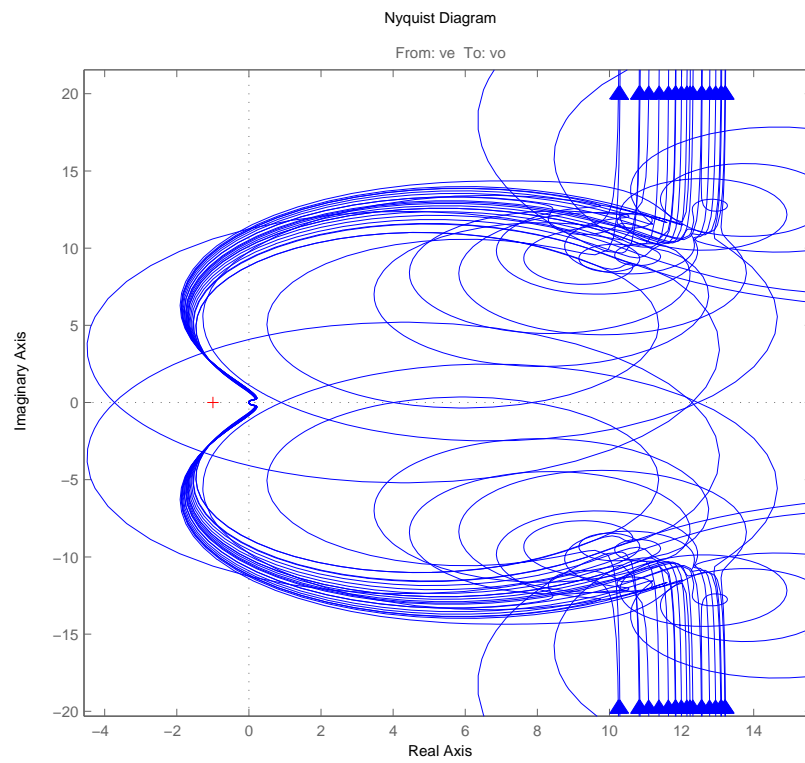
Nyquist Diagram

From: ve To: vo

Figure 6.7: Nyquist plot of the feedforward design with variations in the input voltage.

ers with an undamped input filter. To confirm this, a larger set of controllers is explored by using the μ-synthesis algorithm available in the Matlab Robust Control Toolbox [55]. The idea is to try to find out if there exists any controller K that could achieve stability and adequate performance under the constraints of the problem. In order to proceed with the controller design, the problem has to be posed as a norm minimization problem. The following setup is based on the methodology described in [56] and [55].

The system setup is shown in Fig. 6.8. The inputs to be considered are the voltage reference v_r and the output current i_o, while the main output of interest is the error voltage v_e. In order to penalize the amplitude of perturbations in the input voltage and to comply with well-posedness conditions, the input voltage v_{in} and the duty-cycle command d are also included as outputs respectively. The model is valid up to half the switching frequency, so the uncertainty due to the switching action is included by adding an extra perturbation input v_s at the output of the plant. All these signals have to be weighted in order to constrain the problem with realistic specifications. The dashed box indicates the controller location, to be synthesized by the designer or the control design algorithm.

The system, then, has the form indicated in Fig. 6.9. The controller K has two inputs and one output, and is to be designed in order to minimize the H_∞ norm of the transfer function from the inputs (v_r, i_o, v_s) to the outputs $(\tilde{v}_e, \tilde{v_{in}}, \tilde{d})$ under all
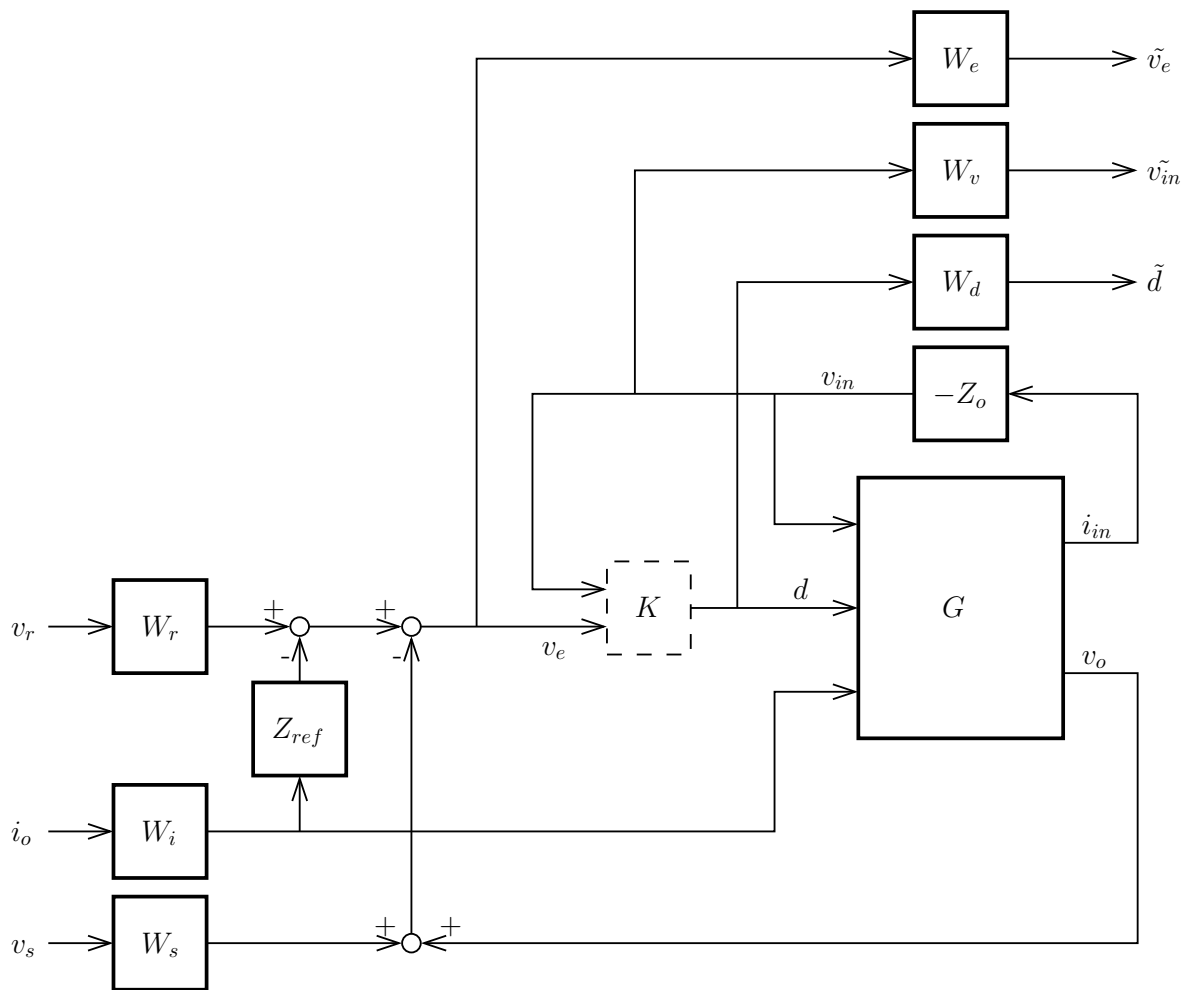
Figure 6.8: System setup for robust control design.
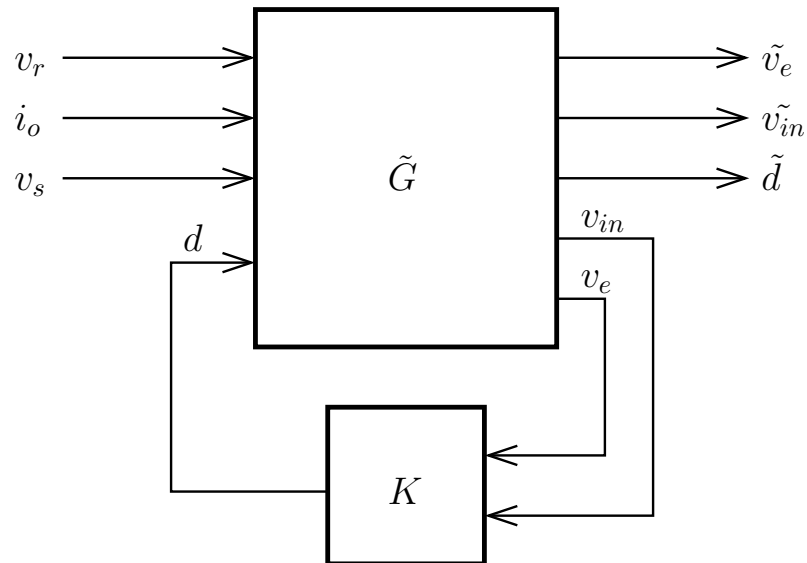
Figure 6.9: Simplified system setup for robust control design.

parameter variations, while preserving stability.

For this application, the weighting functions used to shape the system's response are shown in Figs. 6.10 and 6.11 for the inputs and outputs respectively. The weights at the reference inputs v_r and i_o represent the bandwidth of the signals to be tracked. The weight in the perturbation v_s represents the uncertainty at frequencies above half the switching frequency. On the other hand, the weights at the outputs represent the desired bandwidth of the system as well as the relative importance of the different signals.

The μ-synthesis algorithm was run on a system with uncertainties in the input filter and the input voltage. The code is presented in Appendix C. The Bode plot of the controller synthesized is shown in Fig. 6.12, compared with the controller of the
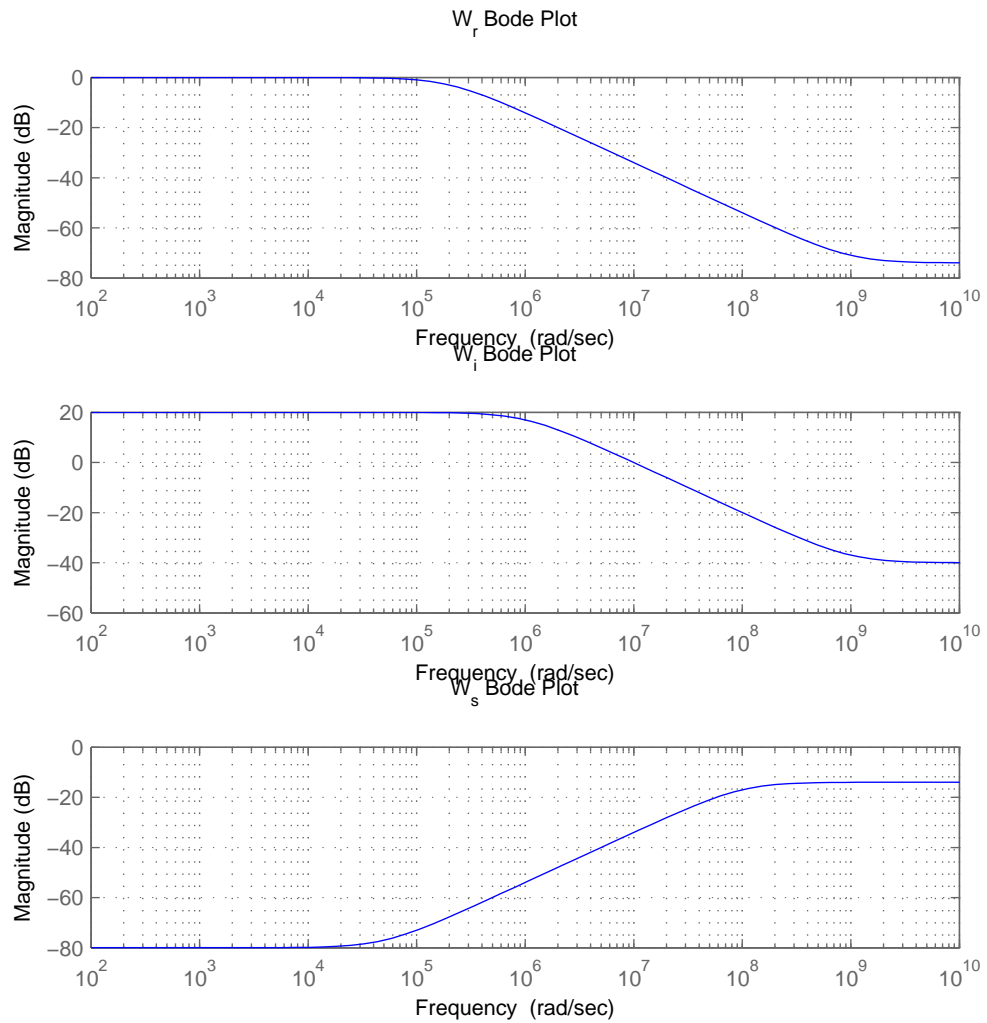
Figure 6.10: Weighting functions for the inputs.
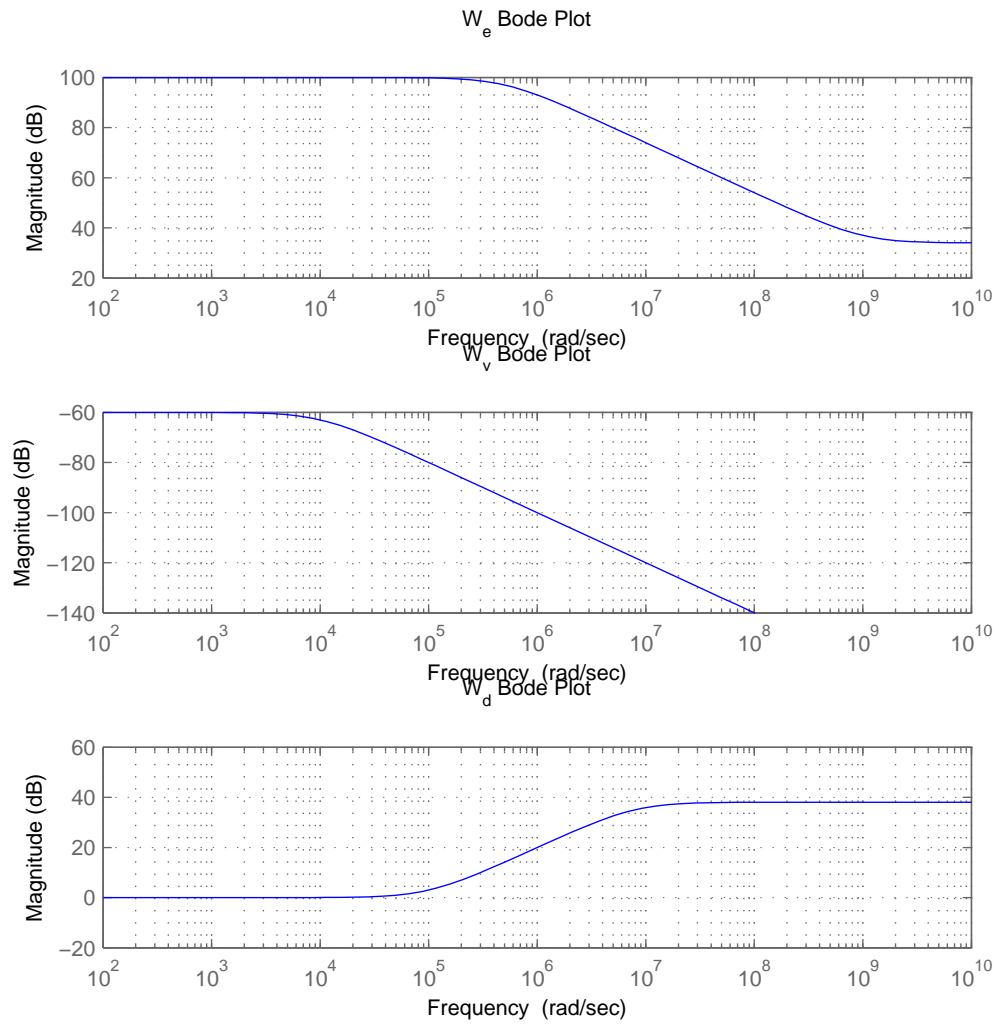
Figure 6.11: Weighting functions for the outputs.

previous section (PID feedback and input voltage feedforward). It can be seen that the μ controller has a much lower gain, especially in the region of the resonant frequency of the input filter. The loop transfer function Bode plot is shown in Fig. 6.13 and the Nyquist plot in Fig. 6.14. The loop magnitude is less than $0dB$ for all frequencies, this means that effectively the feedback loop is not present and performance of the system is very poor. As evidenced by the Nyquist plot, the system is stable. One possible interpretation of this result is that the controller tries to suppress the frequencies in which an abrupt phase change occurs due to the undamped filter. As a consequence, the Nyquist plot does not encircle the point $(-1, 0)$ because the magnitude of the loop transfer function is less than unity.

6.2.6   Conclusions

It can be concluded by the previous analysis and the examples shown that there does not seem to be a control strategy that permits a stable operation of a DC/DC converter with an undamped input filter, while achieving a bandwidth above the resonance of the filter. The strategy of damping the input filter that is standard practice at the present seems to be the only feasible solution to the problem. The next section proposes an alternative way of damping the input filter without using physical resistors.
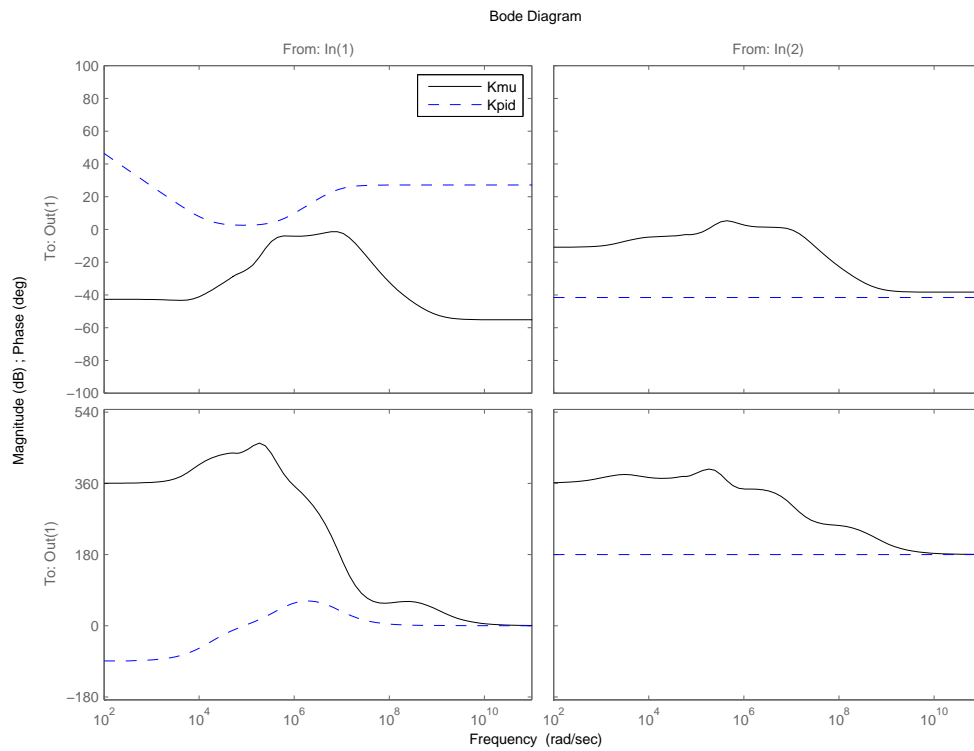
Figure 6.12: Bode plot of the μ controller (solid) compared with the PID controller (dashed). Left: error voltage to duty-cycle transfer function. Right: input voltage to duty-cycle transfer function. Top: magnitude. Bottom: phase.
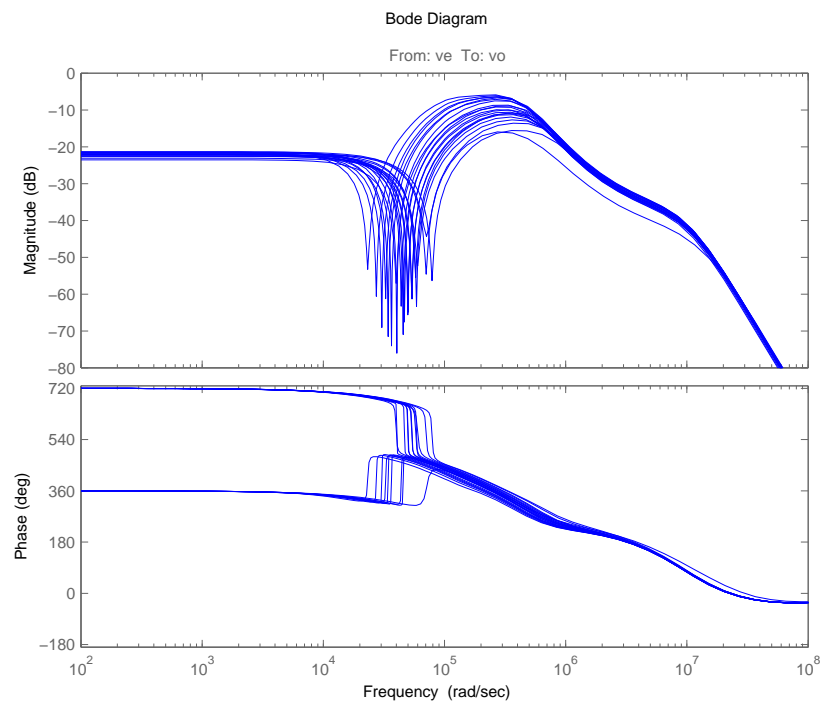
Figure 6.13: Set of Bode plots of the loop with the μ controller for different input filter parameter values.
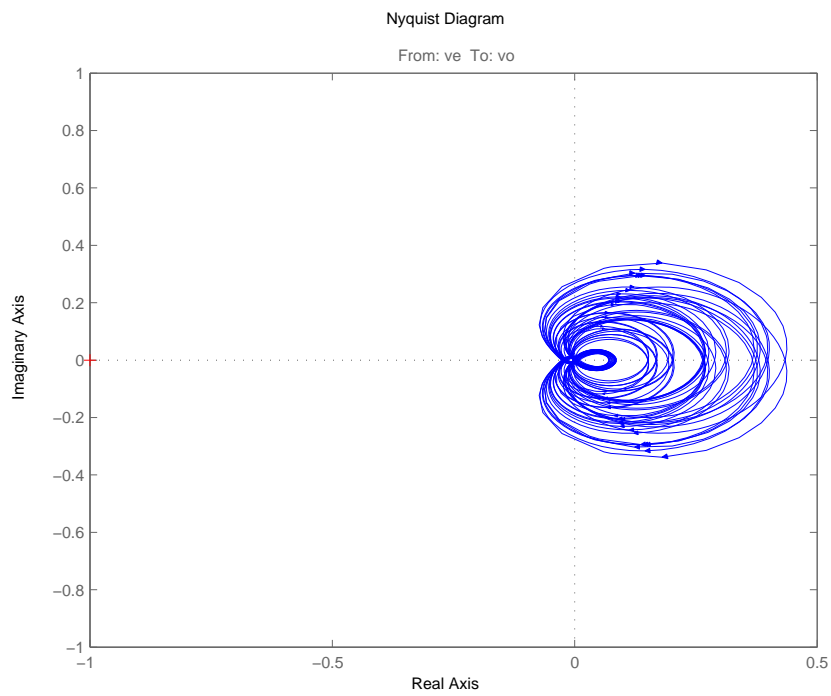
Figure 6.14: Nyquist plot of the loop with the μ controller for different input filter parameter values.
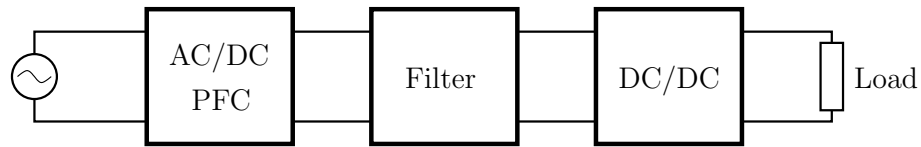
Figure 6.15: Simple DPS architecture.

6.3   Virtual damping of input filter

It has been shown in the previous sections that the presence of an input filter in a power converter under certain conditions could affect the stability of the system, and no control strategy in the converter can solve the problem. The most a control system can achieve is to stabilize the system at the expense of performance. In this section, a different approach from a systems perspective is explored.

Consider the simple DPS architecture shown in Fig. 6.15. A front-end converter performs power factor correction (PFC) and provides a mildly regulated DC bus. A point-of-load (POL) DC/DC converter provides a tightly regulated voltage to the load from this intermediate bus. An EMI filter is used at the input of the POL converter to reduce the frequency content of its input current.

It has been shown that the effects of the filter on the dynamics of the POL converter can be reduced by adding damping. Instead of adding physical damping, the output impedance of the front-end converter can be adjusted to provide the necessary damping. The idea is illustrated in Fig. 6.16. The output impedance of the front-end converter can be made resistive (R_o) over a wide frequency range in
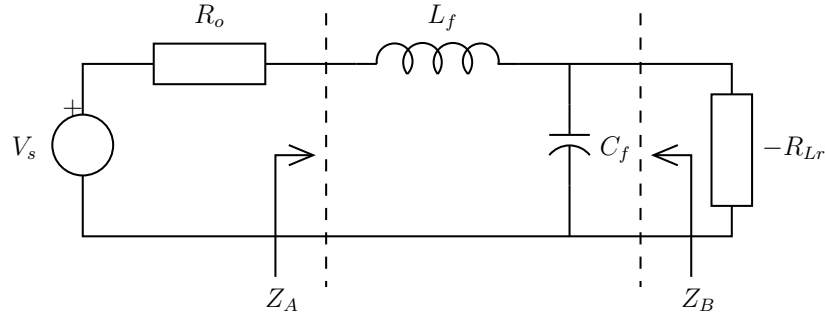
Figure 6.16: Equivalent circuit of simple DPS architecture.

order to damp the input filter and counteract the negative input resistance of the POL converter $-R_{Lr} = -\frac{R_L}{\eta D^2}$.

The system can be viewed as two two-ports interconnected: one is the filter with impedances Z_A and Z_B, and the other one is composed by the two independent resistances $-R_{Lr}$ and R_o. However, the system can also be viewed as two stable one-ports interconnected: one is the filter with resistance R_o in series, and the other is the DC/DC converter with impedance $-R_{Lr}$. This permits a simpler yet still rigurous analysis, because the special case described in Section 5.3 can be used. The location of the zeros of $1 - Z_B Y_{Lr}$ with $Y_{Lr} = \frac{1}{R_{Lr}}$ determine the stability of the interconnection.

Impedance Z_B can be computed as

$$Z_B = (L_f s + R_{dc} + R_o) \| \left(\frac{1}{C_f s} + R_{es} \right) \tag{6.8}$$

$$= \frac{(L_f s + R_{dc} + R_o) \cdot (R_{es} C_f s + 1)}{L_f C_f s^2 + (R_{dc} + R_{es} + R_o) C_f s + 1}. \tag{6.9}$$

Stability can be analyzed using the Routh-Hurwitz criterion on the numerator of

$1 - Z_B Y_{Lr}$, which is

$$\left(1 - \frac{R_{es}}{R_{Lr}}\right) L_f C_f s^2 + \left[\left(R_{dc} + R_o + R_{es} - \frac{R_{es}(R_{dc} + R_o)}{R_{Lr}}\right) C_f - \frac{L_f}{R_{Lr}}\right] s + 1 - \frac{R_{dc} + R_o}{R_{Lr}}$$

$$(6.10)$$

The coefficient $\left(1 - \frac{R_{es}}{R_{Lr}}\right)$ is positive for representative values of the parameters, but the term $\left(1 - \frac{R_{dc} + R_o}{R_{Lr}}\right)$ may not be always positive depending on the value of R_o. The stability conditions can be written as:

$$\left(1 - \frac{R_{dc} + R_o}{R_{Lr}}\right) > 0 \text{ and} \tag{6.11}$$

$$\left[\left(R_{dc} + R_o + R_{es} - \frac{R_{es}(R_{dc} + R_o)}{R_{Lr}}\right) C_f - \frac{L_f}{R_{Lr}}\right] > 0. \tag{6.12}$$

These conditions impose bounds on the values of R_o:

$$\frac{Z_C^2 - R_{es} R_{Lr}}{R_{Lr} - R_{es}} - R_{dc} < R_o < R_{Lr} - R_{dc} \tag{6.13}$$

Under the usual assumptions that $R_{Lr} \gg R_{es}, R_{dc}$, the expressions can be simplified to the following

$$\frac{Z_C^2}{R_{Lr}} - (R_{es} + R_{dc}) < R_o < R_{Lr}. \tag{6.14}$$

Notice that the most constrained case is given by the lowest value of R_{Lr}, i.e., under a high-load condition.

For the typical values reported in Tables 6.1 and 6.2, the assumptions are valid and the worst-case value for R_{Lr} is $640m\Omega$, then the bounds would be

$$1.4m\Omega < R_o < 640m\Omega. \tag{6.15}$$

The designer has a wide range of options for selecting R_o.

The circuit in Fig. 6.16 was simulated using LTspice/SwCADIII [57]. The value for R_{Lr} used was $640m\Omega$ and the input filter values were taken from 6.2. A voltage step was introduced at the input and the capacitor voltage was observed. Several values of R_o were used, spanning the range indicated in (6.15). The results are shown in Fig. 6.17 and corroborate the theoretical results. For $R_o = 1m\Omega$ the system is unstable. For $R_o = 1.4m\Omega$ it is marginally stable. For $R_o = 2, 20,$ and $500m\Omega$ the system is stable with different damping characteristics. For $R_o = 640m\Omega$ and above the system becomes unstable. These results are in agreement with the range predicted in (6.15).

6.4 Conclusions

This chapter has analyzed the input filter problem from the fundamentals of control system theory. It has been illustrated by examples that there exist fundamental limits to the performance of a DC/DC converter in the presence of an undamped input filter. The only stabilizing controller that could be found using an optimizing algorithm was shown to have poor performance due to the fact that it suppresses the frequency range in which the input filter resonance occurs.

A virtual damping technique has been proposed that allows for stable operation without compromising the performance of the system. The technique is based on
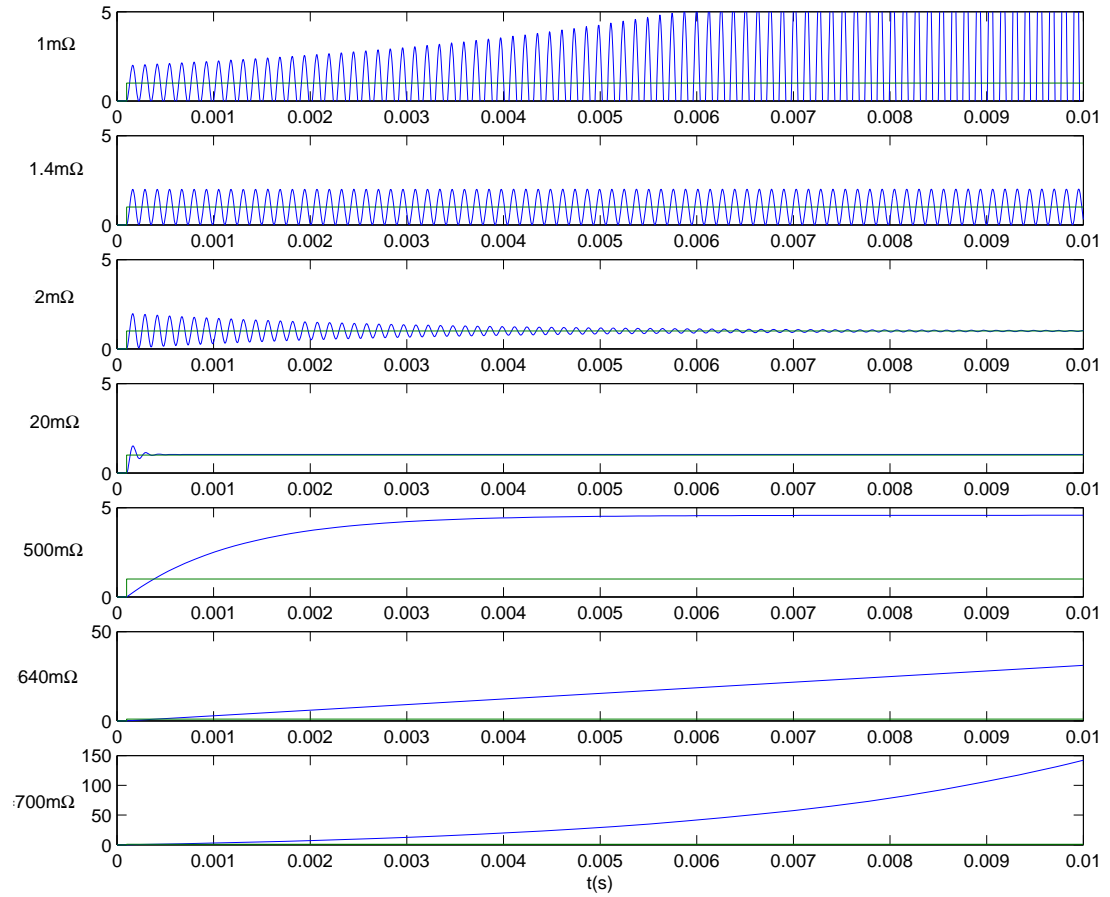
Figure 6.17: Simulation of the virtual damping example with different values of R_o. Response to an input voltage step.

a system-level design in which the system interconnected to the input of the input filter has a resistive output impedance. Simulations corroborate the design equations derived analytically.

In DPS designs, techniques like the one described above could be used to guarantee stability and performance of the interconnection without adding physical components that increment the size, weight, and cost of the system.

Chapter 7

Contributions and Future Work

7.1 Contributions of this Thesis

Output current sensing

An output current sensing methods for high-current buck converters was developed. The method uses the resistance of the PCB trace between the output capacitors and the load as a sensing element. This resistance is estimated in an on-line adaptive scheme by using the input current, which is sensed with a precision resistor, as a reference.

The method is practical, efficient and experimental results show better accuracy than other popular methods. The implementation cost is not significant. By measuring directly the output current, accurate load-line tracking as well as output current

feedforward are enabled.

Although the method described uses the PCB trace resistance, it could be used to tune any other parasitic resistance in the power train, including the series resistance of the inductor, used in the popular inductor sensing method.

Current unbalance estimation

A current unbalance estimation method for multi-phase buck converters was developed. The method is based on an analysis of the harmonic content of the input voltage waveform. The amount of computation power required is reasonable and can be performed with dedicated logic or an already existing microcontroller.

Experimental results show an error on the order of 2% of the rated current of each phase. This method can be used as part of an active phase current balancing circuit, substituting other popular methods that have less accuracy and/or require more external components.

Adaptive output current feedforward

A method for tuning the gain of the output current feedforward path in VRM applications was presented. Although output current feedforward is known to improve the transient response without affecting the stability of the system, its dependence on uncertain power train parameters makes its use difficult in practice. With this

method, the most critical parameter can be tuned adaptively on-line with few computational resources, paving the way to successful commercial application.

The method was implemented in an FPGA and experimental results show a strong performance improvement with respect to a control system without feedforward and with fixed-gain feedforward.

Fundamental performance limits in interconnected converters

The problem of interactions of a converter with its input filter, and several converters interconnected, was analyzed in detail. A survey of the most relevant results in this area was presented. The fundamental limits of performance of interconnected systems were identified by example, and illustrated with the μ-synthesis controller design method.

One possible solution to mitigate the effect of an EMI filter impedance on a POL converter was outlined and simulated. This approach shows that there are system-level design strategies that can be used to eliminate undesirable effects without overdesigning the filters.

7.2   Suggestions for future research

Mixed-signal implementation of output current estimation

The output current estimation method described in Chapter 2 is suitable for an efficient mixed-signal IC implementation. The sensing path requires a low-offset, high-bandwidth differential amplifier, while the gain estimation path can be performed digitally. The variable-gain amplifier in the sensing path can be implemented with a DAC multiplier, in which the variable gain is represented as a digital input and the sensing signal can be used as a reference voltage. Thus, the output would be proportional to both quantities, achieving effective signal multiplication. This possible implementation is illustrated in Fig. 7.1.

The multiplication of the estimated current $\hat{I}_o$ times the switching signal u was performed with a switch in the prototype breadboard. The signal u in turn was obtained from the switching node V_{sw} in order to minimize the errors due to delay. In some applications, those errors could be tolerable, thus the switching signal could be obtained from the duty-cycle command, simplifying further the circuit complexity. The trade-off between accuracy and complexity in this case, as well as the trade-off between voltage offset and bandwidth in the sensing amplifier, would depend on the overall system design and market requirements, therefore it will be application-dependent.
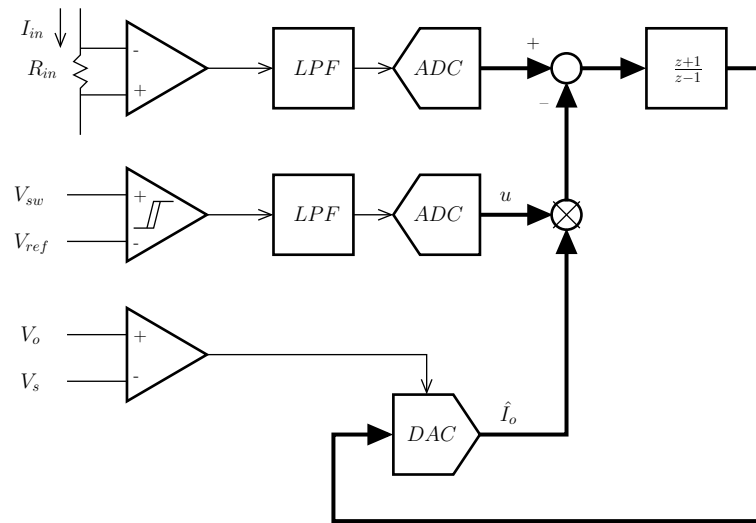
Figure 7.1: Mixed-signal implementation of the output current sensing method. Digital signals are shown with a bold line.

Active phase current balancing

An active phase current balancing (or current sharing) method can be implemented based on the unbalance estimation method described in Chapter 3. This function is usually an integrated part of the PWM controller, since its outputs would add or subtract directly from the duty-cycle command. Therefore, both the current unbalance estimation and the active phase balancing circuits should be implemented in a PWM controller IC.

Adaptive feedback control

The thesis presents an adaptive feedforward control method in Chapter 4. Similar techniques could be applied to tune the parameters of the feedback loop controller,

which are also parameter dependent. At the present, the controller (usually called the error amplifier) needs a careful design and breadboard tuning with discrete components before coming to production. Even with digital controllers, the parameters need to be tuned some way or another.

There is a vast literature on the subject of PID tuning. The methods are either on-line or off-line. During startup time, a converter usually goes thru a soft-start sequence during which an off-line type of tuning method can be attempted. Otherwise, the normal load transients specific to VRM applications generate enough perturbation as to enable an on-line type of tuning, similar to the one derived for the feedforward gain.

Control strategies for stability and performance of DPS

Stability and performance of DPS is a subject that has been addressed in Chapters 5 and 6. The technique described in the latter performs virtual damping of an EMI filter to preserve stability and performance of a POL converter. This shows that there are many possibilities in this area, regarding the use of control techniques at a system-level in order to improve the dynamics of a DPS interconnection. Excessive and unefficient use of capacitance and damping resistors can be avoided.

Similar to the presence of stabilizing and power factor correction elements in an AC interconnected system, a new generation of elements for DC interconnected sys-

tem could arise. These elements would be used to stabilize the system and preserve the dynamics of the individual components by offering adequate impedances to compensate buses shared by many other components.

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Appendix A

Unbalance estimation Matlab code

```
% Current Unbalance Estimation
% 3 phases

% read scope output files
vsw=csvread('vsw30.csv',6,3);
vin=csvread('vin30.csv',6,3);
t = vsw(:,1); % time
Vsw = vsw(:,2); % switching node voltage
Vin = vin(:,2); % input voltage (AC coupled)

% detect period and duty-cycle
Vref = 6; % trigger level
inCycle = 0;
prevDiff = -1;
finished = 0;
i = 1;
while ((finished==0) && (i<length(t))),
    currDiff = Vsw(i)-Vref;
    if ((prevDiff<0) && (currDiff>=0)),
        if (inCycle==0),
            i0 = i;
            t0 = t(i);
            inCycle = 1;
```

```
        else
            if (i-i0>8000), % rule out noise
                i2 = i;
                t2 = t(i);
                finished = 1;
            end
        end
    elseif ((prevDiff>0) && (currDiff<=-0)),
        if (i-i0>800), % rule out noise
            i1 = i;
            t1 = t(i);
        end
    end
    prevDiff = currDiff;
    i = i+1;
end
T = t2-t0;
D = (t1-t0)/T;
npoints = i2-i0+1;
nduty = i1-i0;
tp = t(i0:i2)';
Vinp = Vin(i0:i2)';

% low-pass filter
[b,a]=butter(2,2/npoints); % 2nd order, wc=2*pi/T
text = [tp tp+T tp+2*T tp+3*T tp+4*T tp+5*T tp+6*T tp+7*T tp+8*T tp+9*T];
Vinext = [Vinp Vinp Vinp Vinp  Vinp  Vinp  Vinp  Vinp  Vinp  Vinp];
Vinf = filter(b,a,Vinext);

% plot waveforms
figure(1)
clf
subplot(211)
plot(text,Vinext);
line([t0+8*T t0+8*T],[-.1 .1]);
line([t1+8*T t1+8*T],[-.1 .1]);
line([t2+8*T t2+8*T],[-.1 .1]);
axis([t0+8*T-D*T t0+9*T+D*T -.1 .1])
subplot(212)
hold
```

```
plot(text,Vinf);
line([t0+8*T t0+8*T],[-.015 .01]);
line([t1+8*T t1+8*T],[-.015 .01]);
line([t2+8*T t2+8*T],[-.015 .01]);
axis([t0+8*T-D*T t0+9*T+D*T -.013 .007])

% sample
x = [Vinf(npoints*8);
     Vinf(npoints*8+round(npoints/6));
     Vinf(npoints*8+round(2*npoints/6));
     Vinf(npoints*8+round(3*npoints/6));
     Vinf(npoints*8+round(4*npoints/6));
     Vinf(npoints*8+round(5*npoints/6))];

tx = [text(npoints*8);
     text(npoints*8+round(npoints/6));
     text(npoints*8+round(2*npoints/6));
     text(npoints*8+round(3*npoints/6));
     text(npoints*8+round(4*npoints/6));
     text(npoints*8+round(5*npoints/6))];

 plot(tx,x,'or');

% phase correction due to filter: DC, fs, and 2*fs
C = diag([1 .695*exp(-j*pi/180*90) .241*exp(-j*pi/180*136)]);

% phase correction due to time-shift
R = diag([1 exp(-j*pi*D) exp(-j*2*pi*D)]);

% compute the estimated difference wrt average
S3 = fft(eye(3));
S6 = fft(eye(6));
Pd = D*diag([1 sin(pi*D)/(pi*D) sin(2*pi*D)/(2*pi*D)]);
M = -(eye(3)-1/3*ones(3))*inv(S3)*inv(Pd)*inv(C)*inv(R)*S6(1:3,:)/6;
Vdiff = M*x;

% estimate current by using ESR
Resr = 18e-3;
Idiff = Vdiff/Resr
```

Appendix B

Adaptive feedforward Verilog code

```verilog
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////
// Adaptive feedforward module for VRM
//////////////////////////////////////////////////////////////////////
module adapt_ff(diout, verr, vff, fixed_ff, clk, rst, gain, sel, sat_dc);
    input signed [4:0] diout;   // current
    input signed [4:0] verr;    // voltage error
    output signed [4:0] vff;    // feedforward signal
    input fixed_ff;             // use fixed ff instead of adaptive
    input clk;                  // clock
    input rst;                  // reset active high
    output [7:0] gain;          // output to be displayed in the scope
    input [2:0] sel;            // output selection
    input sat_dc;               // indicates saturation of the duty-cycle

wire signed [7:0] dio; // derivative of the current (filter input)

// intermediate values of the filter
wire signed [7:0] w0;
reg signed [7:0] w1;
reg signed [7:0] w2;
wire signed [7:0] w1q;
wire signed [7:0] w2q;
```

```verilog
wire signed [7:0] w12;
wire signed [7:0] w2o;
wire signed [7:0] w12o;
wire signed [8:0] w12o_wire;

wire signed [7:0] dif; // output of the filter
wire signed [7:0] cor; // correlation between verr and dif
wire signed [12:0] cor_wire; // full multiplier result

reg [7:0] gain; // output to the scope

wire [7:0] fxg; // fixed gain
reg [20:0] adg_reg; // adaptive gain register
wire [7:0] adg; // adaptive gain
wire [7:0] seg; // selected gain

wire signed [12:0] vff_wire; // full multiplier result

reg signed [4:0] diout_reg; // register at the input of diout
reg signed [4:0] verr_reg; // register at the input of ve

// load line filter signals
reg signed [7:0] wll1; // register for load line filter
wire signed [7:0] wll0;
wire signed [7:0] dio_ll0;
wire signed [7:0] dio_ll; // input filtered for load line

// Digital filter
// input: diout; output: dif
// performing shift with sign extension and saturation when it suits
assign dio = { {3{diout_reg[4]}} , diout_reg };
assign wll0 = dio + wll1 - { {5{wll1[7]}} , wll1[6:4] };
assign dio_ll0 = wll0 - { {3{wll1[7]}} , wll1[6:2]} + \
                 { {5{wll1[7]}} , wll1[6:4]};
assign dio_ll = { {3{dio_ll0[7]}} , dio_ll0[6:2] };
assign w0 = dio_ll + w12;
assign w1q = ({ w1[7] , ((~(|(w1[7:6]))) || (&(w1[7:6]))) ? \
           w1[5:0] : (w1[7] ? 6'h00:6'h3F) , 1'b0 }) - \
           ({ {2{w1[7]}} , w1[7:2] }) - \
           ({ {4{w1[7]}} , w1[7:4] });
```

```verilog
begin
      if (rst == 1'b1) begin
            diout_reg <= 5'b0;
            verr_reg <= 5'b0;
            wll1 <= 8'b0;
            w1 <= 10'b0;
            w2 <= 10'b0;
            adg_reg <= { fxg , 13'h00 }; // initial gain
      end else begin
            diout_reg <= diout; // input register
            verr_reg <= verr; // input register
            wll1 <= wll0; // load line filter
            w1 <= w0; // digital filter
            w2 <= w1; // digital filter
            adg_reg <= adg_reg + ((sat_dc)? 8'h00 : cor); // integrator
      end
end

endmodule
```

Appendix C

Robust design Matlab code

```
% Robust design of buck converter controller with input filter

% nominal parameters
Vin_nom = 12; % input voltage
Vref_nom = 1.2; % reference voltage
N = 4; % number of phases
L_nom = 400e-9/N; % total inductance
Rdcr_nom = 4e-3/N; % inductor DC resistance
C_nom = 800e-6; % output cap
Resr_nom = 1e-3; % cap series resistance
Io_nom = 100; % output current
Rref = 1.25e-3; % droop

% actual values
Vin = ureal('Vin',Vin_nom,'Range',[10 13]);
Vref = Vref_nom;
L = L_nom;
Rdcr = Rdcr_nom;
C = C_nom;
Resr = Resr_nom;
Io = Io_nom;

% derived values
```

```
Vo = Vref;
D = Vref_nom/Vin_nom;
R = .01; % 1 for light load, .01 for high load

% input voltage feedforward
F = -D/Vin;

% input filter
Lin = 800e-9;
Rdcin = .1e-3;
Cin = ureal('Cinreal',500e-6,'Range',[200e-6 3000e-6]) + ...
      ultidyn('Cinlti',[1 1],'Bound',0.05*800e-6);
Resin = ureal('Resinreal',1e-3,'Range',[.2e-3 20e-3]) + ...
        ultidyn('Resinlti',[1 1],'Bound',0.05*3e-3);

% controller
Kp = 32; % proportional gain
Kd = 256; % derivative gain
Ki = 0.125; % integral gain
fsw = 1e6; % switching frequency
T = 1/fsw; % switching period
fsamp = fsw*N; % sampling frequency
Tsamp = 1/fsamp; % sampling period

% converter averaged continuous-time model
Gvd = Vin*R/(R+Rdcr)*tf([Resr*C 1], ...
      [(Resr+R)/(Rdcr+R)*L*C ((Resr*R+Resr*Rdcr+Rdcr*R)*C+L)/(Rdcr+R) 1]);
Gvv = D*R/(Rdcr+R)*tf([Resr*C 1], ...
      [(Resr+R)/(Rdcr+R)*L*C ((Resr*R+Resr*Rdcr+Rdcr*R)*C+L)/(Rdcr+R) 1]);
Gvi = -R*Rdcr/(R+Rdcr)*tf([Resr/Rdcr*L*C Resr*C+L/Rdcr 1], ...
      [(Resr+R)/(Rdcr+R)*L*C ((Resr*R+Resr*Rdcr+Rdcr*R)*C+L)/(Rdcr+R) 1]);
Gid = D*Vin/(R+Rdcr)*(1+tf([(Resr+R)*C 1], ...
      [(Resr+R)/(Rdcr+R)*L*C ((Resr*R+Resr*Rdcr+Rdcr*R)*C+L)/(Rdcr+R) 1]));
Giv = D^2/(R+Rdcr)*tf([(Resr+R)*C 1], ...
      [(Resr+R)/(Rdcr+R)*L*C ((Resr*R+Resr*Rdcr+Rdcr*R)*C+L)/(Rdcr+R) 1]);
Gii = D*R/(R+Rdcr)*tf([Resr*C 1], ...
      [(Resr+R)/(Rdcr+R)*L*C ((Resr*R+Resr*Rdcr+Rdcr*R)*C+L)/(Rdcr+R) 1]);

% PID controller
Ad = 1/2/Vin_nom * (tf(Kd.*[1 -1],[1 0],Tsamp) + ...
```

```
      tf(Kp,1,Tsamp)+tf(Ki.*[1 0],[1 -1],Tsamp));
A = d2c(Ad,'tustin');

% reference impedance (load-line)
Zref = Rref*tf([Resr*C 1],[Rref*C 1]);

% input filter
Zo = tf([Resin*Lin*Cin Lin+Resin*Rdcin*Cin Rdcin], ...
     [Lin*Cin (Rdcin+Resin)*Cin 1]);

% weights
We = tf(1e5*[1/1e9 1],[1/5e5 1]); % minimize error up to BW
Wr = tf([1/1e9 1],[1/2e5 1]); % reference BW around 33kHz
Wd = tf(10*[1/1e9 1],[1/1e6 1]); % more weight on output current disturbance
Wu = tf([1/1e5 1],[1/8e6 1]); % penalize actuator input for well-posedness
Wv = tf(1e-2*[1/1e9 1],[1/1e4 1]); % penalize input voltage for stability
Ws = tf(1e-2*[1/1e5],[1/1e8 1]); % disturbance due to switching

% interconnection for mu design
systemnames = 'Gvd Gvv Gvi Giv Gid Gii Zo Zref We Wr Wd Wu Wv Ws';
inputvar = '[vr;io;vs;d]';
outputvar = '[We;Wu;Wv;Wr-Zref-Gvd-Gvv-Gvi-Ws;-Zo]';
input_to_Gvd = '[d]';
input_to_Gvv = '[-Zo]';
input_to_Gvi = '[Wd]';
input_to_Gid = '[d]';
input_to_Giv = '[-Zo]';
input_to_Gii = '[Wd]';
input_to_Zo = '[Giv+Gid+Gii]';
input_to_Zref = '[Wd]';
input_to_We = '[Wr-Zref-Gvd-Gvv-Gvi-Ws]';
input_to_Wr = '[vr]';
input_to_Wd = '[io]';
input_to_Wu = '[d]';
input_to_Wv = '[-Zo]';
input_to_Ws = '[vs]';
cleanupsysic = 'yes';
P = sysic;
P.InputName={'vr' 'io' 'vs' 'd'};
P.OutputName={'vet' 'vut' 'vint' 've' 'vin'};
```

```
% interconnection for CL analysis
systemnames = 'Gvd Gvv Gvi Giv Gid Gii Zo Zref';
inputvar = '[vr;io;d]';
outputvar = '[Gvd+Gvv+Gvi;vr-Zref-Gvd-Gvv-Gvi;-Zo]';
input_to_Gvd = '[d]';
input_to_Gvv = '[-Zo]';
input_to_Gvi = '[io]';
input_to_Gid = '[d]';
input_to_Giv = '[-Zo]';
input_to_Gii = '[io]';
input_to_Zo = '[Giv+Gid+Gii]';
input_to_Zref = '[io]';
cleanupsysic = 'yes';
P2 = sysic;
P2.InputName={'vr' 'io' 'd'};
P2.OutputName={'vo' 've' 'vin'};

% traditional controllers
Kfb = [A 0]; % only feedback
Kff = [A F]; % standard controller w/feedforward

% mu design
opt = dkitopt('NumberofAutoIterations',4);
[Kmu,CLmu,bnd] = dksyn(P,2,1,opt);

% closed-loop systems
CL2fb = lft(P2,Kfb);
CL2ff = lft(P2,Kff);
CL2mu = lft(P2,Kmu);

% interconnections for OL analysis
systemnames = 'Gvd Gvv Giv Gid Zo Kfb';
inputvar = '[ve]';
outputvar = '[Gvd+Gvv]';
input_to_Gvd = '[Kfb]';
input_to_Gvv = '[-Zo]';
input_to_Gid = '[Kfb]';
input_to_Giv = '[-Zo]';
input_to_Zo = '[Giv+Gid]';
```

```
input_to_Kfb = '[ve;-Zo]';
cleanupsysic = 'yes';
Pfb = sysic;
Pfb.InputName={'ve'};
Pfb.OutputName={'vo'};

systemnames = 'Gvd Gvv Giv Gid Zo Kff';
inputvar = '[ve]';
outputvar = '[Gvd+Gvv]';
input_to_Gvd = '[Kff]';
input_to_Gvv = '[-Zo]';
input_to_Gid = '[Kff]';
input_to_Giv = '[-Zo]';
input_to_Zo = '[Giv+Gid]';
input_to_Kff = '[ve;-Zo]';
cleanupsysic = 'yes';
Pff = sysic;
Pff.InputName={'ve'};
Pff.OutputName={'vo'};

systemnames = 'Gvd Gvv Giv Gid Zo Kmu';
inputvar = '[ve]';
outputvar = '[Gvd+Gvv]';
input_to_Gvd = '[Kmu]';
input_to_Gvv = '[-Zo]';
input_to_Gid = '[Kmu]';
input_to_Giv = '[-Zo]';
input_to_Zo = '[Giv+Gid]';
input_to_Kmu = '[ve;-Zo]';
cleanupsysic = 'yes';
Pmu = sysic;
Pmu.InputName={'ve'};
Pmu.OutputName={'vo'};
```