Low Power Integrated LC Voltage Controlled Oscillator in CMOS Technology at 900MHz

Por

Rafaella Fiorelli

Tesis Presentada Ante el
Instituto de Ingeniería Eléctrica
Para Cumplir con Parte de
los Requisitos del Grado de

MAGISTER EN INGENIERíA ELÉCTRICA

En el Área de MICROELECTRÓNICA

Tutor:

Prof. Dr.Fernando Silveira

Tribunal:

Prof.Dr.Wilhelmus Van Noije, USP, Brazil
Prof. Juan Mártony, UdelaR, Uruguay
MSc.Julio Pérez Acle, UdelaR, Uruguay

Instituto de Ingeniería Eléctrica
Facultad de Ingeniería
Universidad de la República
Montevideo, Uruguay

December 2005

ISSN: 1510-7264

Typesetted in LaTeX 2_ε

Contents

List of Figures

List of Tables

Resumen

En este trabajo fue diseñado un oscilador controlado por voltaje tipo LC en la banda de 900MHz. Se usó una tecnología CMOS de $0.35\mu m$, se trabajó con inductores internos al chip y varactores MOS de inversión. Fue realizada una revisión de los modelos más importantes de ruido de fase en osciladores LC. Para optimizar el compromiso entre el ruido de fase y el consumo, el bloque de transistores cruzados fue diseñado para trabajar en la region de inversión moderada. La metodología de diseño presentada utiliza el modelo ACM y la metodología g_m/I_D. El oscilador controlado por voltaje finalmente diseñado tiene un consumo de corriente de 3mA con una fuente de voltaje de 3V y su ruido de fase medido es de -107dBc/Hz@1MHz. Estos resultados muestran que se alcanzó un buen compromiso entre el ruido de fase y el consumo del circuito.

Abstract

In this work, a low power LC voltage controlled oscillator at the 900MHz band has been designed. A $0.35\mu m$ CMOS technology, monolithic inductors and inversion MOS varactors have been used. A review of the most important models of phase noise in LC oscillators has been done. In order to optimize the trade-off between the phase noise and the consumption, the cross-coupled pair transistors were designed to work in the moderate inversion region. A design methodology using the ACM model and the g_m/I_D methodology is presented. The voltage controlled oscillator finally designed has a current consumption of 3mA with a 3V power supply and a measured phase noise of -107dBc/Hz@1Mz. Those results show that a good trade-off between phase noise and power consumption was reached.

Agradecimientos

Me gustaría expresar brevemente mi más sincera gratitud a todas aquellas personas que, de una u otra forma, me apoyaron y ayudaron durante estos dos años. Sin ellas no hubiese podido realizar satisfactoriamente este trabajo.

Primeramente, deseo agradecer a mi tutor, el Prof. Dr.Fernando Silveira, por su invaluable guía a lo largo de todo este trabajo. Las fructíferas discusiones generadas y el apoyo brindado -tanto académico como humano- durante estos años fueron indispensables para haber llevado esta tesis de maestría a buen puerto. Sinceramente, muchísimas gracias.

Por supuesto que quiero agradecer a las demás personas que integran el Grupo de Microelectrónica: MSc.Pablo Aguirre, MSc.Leonardo Barboni, Ing.Pablo Mazzara, Ing.Linder Reyes e Ing.Conrado Rossi. Son muchísimos los momentos que necesité de su ayuda y siempre la obtuve.

Deseo agradecer también a todas las personas que trabajan el en IIE. Para los profesores, investigadores y personal no docente y para las secretarias (y sus chocolates), muchísimas gracias por hacer posible que algunos de nosotros podamos realizar posgrados en Uruguay.

Me gustaría agradecer a la Facultad de Ingeniería en su conjunto por haberme otorgado la beca de maestría. También agradezco a CSIC por haber apoyado financieramente mi pasantía en Bélgica.

Deseo expresar mi sincera gratitud a los integrantes del Laboratorio de Circuitos Integrados DICE de la Universitè catolique de Louvain la Neuve, en Bélgica, muy especialmente al Dr. Denis Flandre por permitirme trabajar durante tres meses en su laboratorio y a Laurent Vancaille y Bertrand Parvais entre muchos otros, por haber sido tan hospitalarios durante mi estadía en Bélgica.

Deseo agradecer al Prof. Dr. Silva Martinez y a Alberto Valdes-García de la Universidad Texas *A&M* de Estados Unidos por habernos brindado información muy valiosa sobre software de simulación de inductores, tan necesario para este trabajo.

Agradezco a la institución MOSIS a través de su programa MEP, por habernos permitido realizar chips de prueba al comienzo de ésta maestría.

Mi pasantía en Bélgica no hubiese sido tan interesante y enriquecedora si no hubiese tenido en gusto de conocer a dos personas tan especiales como son Gonzalo Picún y Silvia Rojas. Nunca sabré como pagarles por todo lo que hicieron por mí en esos meses. Muchas gracias.

Quiero agradecer de corazón a mis amigos. Siempre me han alentado a seguir adelante y se han interesado en lo que hago a pesar que aún no he sido capaz de explicarles claramente que he estado estudiando. Quiero nombrar especialmente a dos personas. A Denise Dalva por haberme acompañado incondicionalmente durante estos años. A Claudia Fumero, porque somos tan diferentes y tan iguales.

A mi novio Alfredo Arnaud. Alfre, tengo la gran suerte que tú, mi amor, entiendas lo que yo estudio. Te doy gracias por las infinitas horas del tiempo que me brindaste y que tanto me ayudaron. Te agradezco por haber estado junto a mi todos estos años. Definitivamente no hubiese llegado hasta aquí sin ti.

Quiero agradecer por último a mi familia: a mis adorados padres, Adriana y Reynaldo y al más genial de los hermanos, Enzo. Ellos me han dado la fuerza y el cariño que necesité para llegar hasta aquí. También agradezco a Florencia, la hermana que me regalaron de grande y a Chiche, la abuela que me regalaron de grande. A mis abuelos, porque sin ellos no estaría aquí y a Teco y Neca mis segundos padres.

Le dedico este trabajo a dos personas que no están aquí hoy pero que estoy segura estarían felices de ver hasta donde he llegado. A mi querida Maestra Elena, y a Valentín.

Chapter 1
Introduction

The explosive growth in radio-frequency applications has resulted in an increasing demand of wireless devices such as transceivers, receivers and transmitters [2] [3] [4] [5] [6] [7] [8] [9] [10]. The applications where these devices are used are uncountable. They go from short to long range communications systems and from very low to very high bit rates (such as local area networks). Depending on the application is the requirements of the power consumption of the system; for example, for short range and low bit rate communications the power consumption might be low. Sometimes the application fixes the voltage source needed; if the devices must use battery power supply and must have autonomy of several years its power consumption must be of few microwatts. If the system can be supplied by the mains network the power consumption can be of the order of miliwatts or even more. From the previous discussion it is clear that the system requirements such as autonomy, range of communication or bit rates strongly condition the device design.

The work presented in this document is part of a design of a transmitter working in the band of 900MHz. It is intended that this transmitter works under most of the specifications of the IEEE 802.15.4 norm [11], whose applications are directed to very low power consumption and very low data bit-rates. These devices are usually attached to sensors of temperature, humidity, pressure, acceleration, chemical products among many others. They can log data coming from the sensors or from an external data source. They can be used in agronomy (as reporting the soil conditions or tracing the cattle), in cars (sending tires' pressure or the state of the brakes), in industry (monitoring the temperature or the humidity of a controlled process of difficult or almost impossible access) and even at home.

One of the most important blocks of the transmitter is the phase locked loop (PLL) which fixes the channel frequency. A PLL is a system with a feedback loop where an oscillator is controlled in such a way that its output signal has same phase that the reference input signal. Its key block to obtain a good PLL performance is the Voltage Controlled Oscillator (VCO). This block has an internal device that modifies its characteristics with a change in an input voltage V_{bias}. When V_{bias} changes the VCO frequency oscillation is modified. The VCO features determine the good quality of the PLL obtained. The VCO studied for this thesis was part of a PLL, which is under test. It has been used a LC VCO (L represents the inductance and C the capacitance of the VCO). It was designed in a $0.35\mu m$ standard CMOS digital technology. The oscillation is produced at the frequency at which L and C resonate. All the components of the VCO are on-chip, which means that it has monolithic inductors. We obtained a compact design with no need of external chip components. However, the standard CMOS technology used constrains the quality factor of the inductor obtained, which jeopardizes the performance of the VCO

Reference	Technology	Freq	Phase Noise	Tuning Range	Consumption	Inductors	Varactors
[12]	0.5μm CMOS	434MHz	-111dBc/Hz @600kHz	1.6%	0.23mA	off-chip	accumulation-mode
[13]	0.6μm CMOS	2.4GHz	-118dBc/Hz @1MHz	11%	9mA	on-chip	inversion-mode
[14]	0.25μm CMOS	4GHz	-117dBc/Hz @1MHz	15%	3mA	on-chip	new structure
[15]	0.7μm CMOS	1.8GHz	-116dBc/Hz @600kHz	13%	4mA	on-chip	?
[16]	0.35μm CMOS	2.4GHz	-105dBc/Hz @100kHz	14%	4.5mA	on-chip	accumulation-mode
[17]	0.18μmCMOS	5.3GHz	-124dBc/Hz @1MHz	10%	7.5mA	on-chip	p+/n-well diodes
[18]	0.65μm BiCMOS	2GHz	-125dBc/Hz @600kHz	11%	19mA	on-chip	p+/n-well diodes
[19]	0.35μm CMOS	1.3GHz	-119dBc/Hz @600kHz	28%	6mA	on-chip and bond-wire	accumulation-mode
[20]	0.35μm BiCMOS	2GHz	-117dBc/Hz @600kHz	26%	4mA	on-chip	?
[21]	0.25μm CMOS	1.8GHz	-121dBc/Hz @600kHz	?	2mA	on-chip	?

Table 1.1: Published works of LC voltage controlled oscillators' design of the last few years

[22][23][24].

This kind of VCOs has been widely studied in the last years, and several publications have shown very interesting results on this matter. To show the state-of-the-art of this subject, it is given a summary of the most important works in Table 1.1. The benchmarks used to compare these works are: the phase noise reached at a certain frequency, the tuning range of the VCO, the current consumption and construction of the inductor on-chip or off-chip. The results depend also on the technology used, the working frequency and the kind of varactors implemented. In this summary the range of frequency given goes from 433MHz to 5.3GHz. We focused particularly on designing a VCO with the lowest possible current consumption without increasing too much the phase noise.

To design the VCO transistors the g_m/I_D methodology [25] was utilized . This unifies the treatment of all regions of operation, and with this it is obtained a relation between g_m/I_D and the normalized current $I_D/(W/L)$. It is found that the g_m/I_D curve is a common characteristic of all the transistors belonging to a same process.

The ACM model [26] has been the transistor model used to do the analytical computations. This physically based model describes all the operation regions with continuous, simple and accurate expressions. This kind of model was a necessity in our work as we were interested in studing the VCO transistors in all the operation regions, specially in the moderate inversion region. Combining the ACM model and the g_m/I_D methodology it is very easy to compute the transistor dimensions.
The VCO initial specifications were the following:

- the technology must be a CMOS standard technology.
- the VCO will be used in a very low power consumption system so it must have a power consumption as low as possible.
- the supply voltage will be 3V but can drop to 2.4V (if two batteries of 1.2V are used).
- the phase noise of the PLL depends strongly on the phase noise of the VCO, so an acceptable value of the last one must be reached to fulfill as much as possible the IEEE802.15.4[11] requirements.
- the occupied area of the VCO is limited to $600\mu m$ by $600\mu m$ -it has been an arbitrary chosen value-.
- the tuning range must be at least 3.2%, because the band of 915MHz of the IEEE802.15.4[11] is 15MHz around 915MHz.
- it has to handle a load capacitance (coming from the other blocks of the PLL) of 0.6pF on each output port.

The summary of the contents of this work is as follows:

Chapter 2: Analysis and design of -Gm LC VCOs In this chapter is studied the type of VCOs used. Various architectures are presented and it is discussed why the used topology is chosen. Also it is studied the mechanism of oscillation of these devices. The design methodology proposed in this work and the choice of transistors working in moderate inversion region is explained. Finally, a discussion on the design of the layout is given.

Chapter 3: Phase Noise in LC VCOs The phase noise is a fundamental characteristic of the VCO. Two models -an empirical and a physical-based model- are described, showing the advantages of each one of them. The noise sources and the phase noise expressions of the topology used are given. A discussion of the trade-offs between the phase noise and the power consumption is presented. Finally, the values of the phase noise (calculated and simulated) are shown.

Chapter 4: Inductors Design In this chapter several types of monolithic inductors are shown as well as some models to calculate its physical characteristics. The simulation tools used during this work are proposed. Finally, the inductor design methodology is described and the parameters of the final inductor used are shown.

Chapter 5: Varactor Design In this chapter the most common topologies of varactors are presented and, specifically, the varactor topology used in this work is deeply studied. At the end, the final varactor characteristics are shown.

Chapter 6: Measurements In this chapter the measurement setup is presented as well as the measured results.

Chapter 7: Conclusions and Future Work

Chapter 2
Analysis and design of -Gm LC VCOs

2.1 Introduction

The voltage controlled oscillators (VCO) designed in CMOS technologies have become nowadays a real solution in the band of radio frequencies (from now on RF) because of having achieved low power consumption and low phase noise values.

Also the use of on-chip inductors is now acceptable in RF [15] [19] [18] [27] . In the band of 900MHz it has been also possible to design and use monolithic inductors despite its size [28]. In this frequency the size of the inductor increases because in an LC oscillator the oscillation frequency ω_0 is:

$$\omega_0^2 = \frac{1}{LC} \tag{2.1}$$

and if the frequency ω_0 decreases and the capacitor value is maintained constant the inductor value must increase.

In this chapter the principles and equations that governs the G_m LC VCO type will be studied. Various of its topologies are reviewed, putting particular attention in the complementary cross-coupled -Gm LC VCO, which is the one used throughout this work.

Also a VCO design methodology is presented using the equations that determine the VCO oscillation and the ACM CMOS transistor model [26]. This methodology is based on finding good trade-offs between power consumption and phase noise.

Another aim of this chapter is to show that at 900MHz the cross-coupled transistor block can work correctly in moderate inversion and that at this level of inversion the power consumption is improved without jeopardizing other characteristics of the VCO.

Finally the complete set of design parameters of the utilized VCO are presented.

2.2 Principles and Topologies of -Gm LC VCO

A VCO is an oscillator whose oscillation frequency -or working frequency- can be modified using an external bias voltage V_{bias}. It is very important the way the frequency of the VCO f varies when V_{bias} changes. If the curve f vs V_{bias} is as shown in Fig.2.1, some characteristics of the VCO can be defined. Firstly, there is a central zone of the curve where the frequency varies linearly with V_{bias} as shown with the straight line of Fig.2.1. The limits of the linearized zone are where the straight line begins to separate from the curve. The voltages where these limits occur are

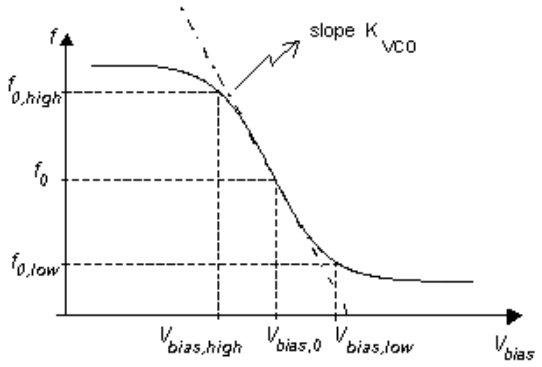


Figure 2.1: Typical curve of the VCO frequency versus V_{bias}

called $V_{bias,low}$ and $V_{bias,high}$ and correspond to the lower and higher frequency limits ($f_{0,low}$ and $f_{0,high}$). We define the VCO central frequency f_0 as the frequency f when $V_{bias} = (V_{bias,low} + V_{bias,high})/2$. Another parameter defined in the VCO is the K_{VCO}, the tuning constant. It is determined by the tuning slope [29], and it is defined as:

$$K_{VCO} = \left| \frac{d(f(V_{bias}))}{d(V_{bias})} \right| \tag{2.2}$$

This expression can be approximated as:

$$K_{VCO} \approx \left| \frac{f_{0,high} - f_{0,low}}{V_{bias,high} - V_{bias,low}} \right| \tag{2.3}$$

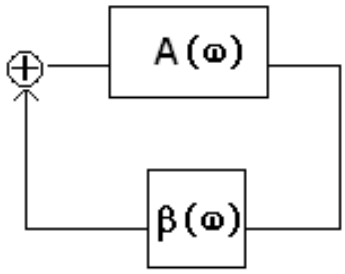
In this work the element that changes its characteristics when the bias voltage changes is a varactor (a variable capacitor); it modifies its capacitance when its drain voltage V_D is modified ($V_{bias} = V_D = V_S$). In Chap.5 a complete study of this structure will be done.

The kind of LC VCOs studied here are called Harmonic Oscillators because they are capable of produce an almost pure sinusoidal oscillation with good phase noise and spectral purity. [1].

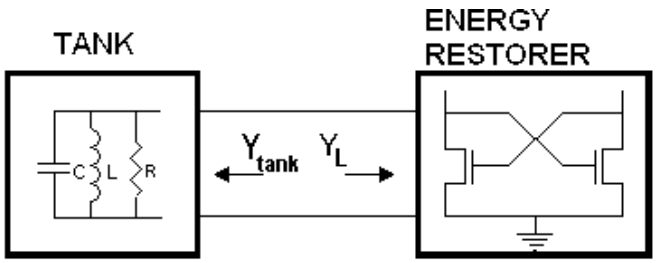
These oscillators can be modelled in two ways which are equivalent [30]: one is the feedback model and the other is the negative-resistance model. Both descriptions are equivalent and depending on the topology of the circuit is the one utilized.

The first model is shown in Fig.2.2(a) and consists of a forward block A(s) and a feedback block β(s). To work as an oscillator this circuit has to obey the Barkhausen criterion:

[1]The phase noise represents the phase and frequency fluctuations of the VCO -the VCO noise-; thus the higher the phase noise the poorer the quality of the VCO. This will be studied deeply in Chap.3.



(a) Feedback model



(b) Negative-resistance model

Figure 2.2: Types of oscillator models

$$Re(A\beta) = 1 \tag{2.4}$$
$$Im(A\beta) = 0 \tag{2.5}$$

The other model is depicted in Fig.2.2(b); it has two blocks, one determines the frequency (tank) and the other is the active circuit (also called energy restorer). For this model the equation that has to be fulfilled is:

$$Y_L + Y_{tank} = 0 \tag{2.6}$$

where Y_L is the admittance of the energy restorer and Y_{tank} is the admittance of the tank. From this expression the working frequency and the oscillation condition is obtained.

The tank filters the non-sinusoidal current signal coming from the active block and obtains in its terminals a sinusoidal voltage. As the tank has a non-zero resistance it losses energy and then the oscillation might disappear. To maintain the oscillation it is needed the active block (or energy restorer) that brings back the energy lost in the filter. Nevertheless, it also generates lot of harmonics in its out-

put current, which are filtered in the tank. This model is called negative-resistance model because the energy restorer can be seen as a negative resistance that compensates the parasitic resistance of the tank.

In this work the -Gm LC VCO is modelled as a negative-resistance oscillator. Its energy restorer comprises one or two blocks of two cross-coupled MOS transistors. They have the gate of one transistor connected to the drain of the other -and viceversa- and its sources are short-circuited. The conductance seen from the drains of the two cross-coupled transistor block is negative, as it will be shown later and its value is $-Gm = -g_m/2$ (this is why those circuits are called "-Gm" oscillators). There is a direct dependence between the biasing of these transistors and the value of the negative resistance of the energy restorer in these oscillators.

There are several topologies of -Gm oscillators, being the most common used the following ones (depicted in Fig.2.3).

1. **all-nMOS cross-coupled transistors with resistor bias.**

   The basic one consist of two nMOS cross-coupled transistors connected to the tank by its drains and biased by a resistor connected between the MOS sources and ground (GND) or between the tank and V_{DD}, as it is shown in Figs.2.3(a) and 2.3(d).A variant of this topology is the circuit without the resistance. The drawback of this topology is the direct dependence of the properties of the circuit with the voltage source's fluctuations and technology parameter variations (for example the V_{GS} voltage modifies the bias current). It can be seen specially in the non-constant value of the bias current throughout a complete cycle, which can lead to an increment in the phase noise with respect to other topologies if the resistance value is not well chosen [31].

2. **all-nMOS cross-coupled transistors structure with MOS current source.**

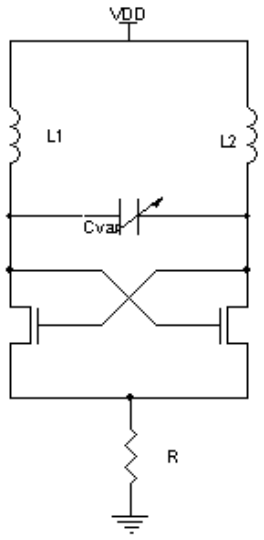
   It is a variant of the previous topology but instead of a resistor bias it uses a MOS current source. In Fig.2.3(b) it is depicted the nMOS source and in Fig.2.3(e) it is the pMOS source.

3. **Cross-coupled complementary topology.** It is composed by two blocks of cross-coupled pair transistors -pMOS and nMOS- and an MOS current source. In Fig.2.3(c) it is the one with an nMOS source and in Fig.2.3(f)it has the pMOS source.

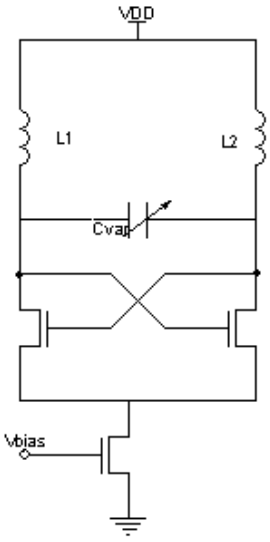
In [32] it is shown that the second topology has worse results in terms of phase noise that the third one (a brief explanation of this matter is given in App.B.1).

In the third structure both blocks are designed to have the same transconductance value, which means that each nMOS and pMOS transistor has the same transconductance ($g_{m,p} = g_{m,n} = g_m$). In this case the total negative resistance $-G_m$ of both blocks is

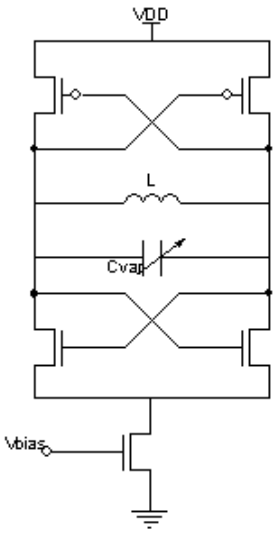
$$-G_m = -2 \cdot g_m/2 = -g_m \tag{2.7}$$



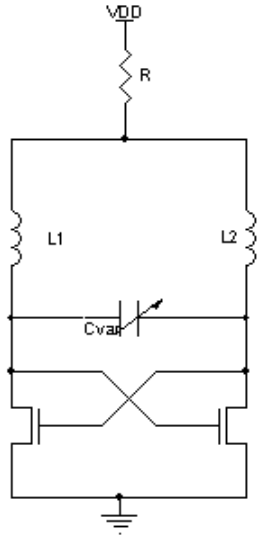
(a) Cross-coupled (resistor biased)



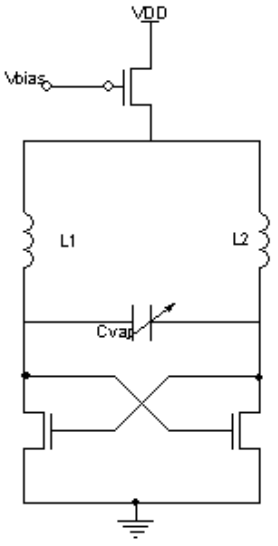
(b) Cross-coupled (n-Type MOS current source)



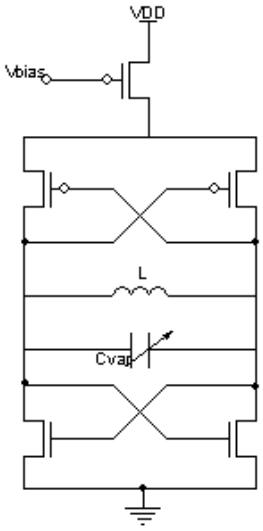
(c) Cross-coupled complementary (n-Type current source)



(d) Cross-coupled (resistor biased)



(e) Cross-coupled (p-Type MOS current source)



(f) Cross-coupled complementary (p-Type MOS current source)

Figure 2.3: Different topologies of -Gm LC VCO

However, the addition of two more transistors -specially the p-MOS ones- raises the value of the parasitic capacitance which might be a problem in the design. Also this topology cannot scale down to lower the supply voltage compared with the all-nMOS cross-coupled topology because it uses an extra V_{gs}. On the other hand as in the all-nMOS structure the dc value of the drain voltage is almost V_{DD}, the dc voltage drop across the channel is larger than in the complementary VCO, which can lead to stronger velocity saturation [21].

A topology which has not been shown in Fig.2.3 is the one that uses a cross-coupled p-MOS transistor block instead of a n-MOS one. As it is studied in [17] the all-pMOS topology with pMOS current source has a little better performance respect of the all-nMOS structure with nMOS current source.

The pMOS current source that is used in the second and third structures fixes the bias current of the VCO independent of the supply voltage. As the current source adds phase noise to the VCO and the pMOS transistors have better flicker noise figures, in this work it has been used the pMOS transistors to build the the current source.

In our design we have chosen the cross-coupled complementary topology (see Fig.2.3(f)) to design our VCO.

2.3 Cross-coupled transistors block

To study the operation of the VCO it is needed to know how the cross coupled transistors block works. To do that, we will study this block using the small-signal model for the transistors. In this study -as depicted in Fig.2.4(a), their common source has a constant voltage value because the circuit has a symmetrical structure (the transistors are considered identical) and the output voltage (the voltage between its drains) is differential. Then this point is considered *virtual ground* at small-signal.

The transistor model used is the quasi-static model five intrinsic capacitance model which considers the capacitances C_{gd}, C_{gs}, C_{db}, C_{gd}, C_{gb} [33]. It has been also considered the capacitance C_{ds}. In the used model there are not considered the channel resistance, the gate intrinsic resistance and the transconductance delay [34] [35]).[2]

The extrinsic capacitances are also considered in the study. In Fig.2.4(b) is the small-signal model of the block. The overlap and junction capacitances are included together with the intrinsic ones, despite they are not explicitly mentioned in the scheme).

As bulk and source voltages are *virtual ground*, the capacitances C_{sb} are short-circuited in the small-signal operation, being the resulting circuit the one shown in Fig.2.4(c).

Since the transistors, their bias current and their capacitances are considered identical; and as the gate of one transistor is crossed with the drain of the other; a

[2]The designed nMOs transistors work below the quasi-static limit, the pMOS are a bit over that limit.

simple differential model of the block can be obtained (see Fig.2.4(d)). The capacitance $C_{gd,1}||C_{gd,2}$ is split in two capacitances in series of value $2 \cdot (C_{gd,1}||C_{gd,2})$ and the middle point can be considered as virtual ground. Then it is possible to have all the capacitances of the circuit in parallel and to obtain the equivalent capacitance seen by the drains of the transistors, whose value is:

$$C_{eq,-Gm} = 2C_{gd} + \frac{(C_{gs} + C_{db} + C_{ds} + C_{gb})}{2} \tag{2.8}$$

To explain the transformation of the transconductance of the transistors into a negative resistance shown in Fig.2.4(d) lets take the transistor M1 of Fig.2.4(a). The gate-source voltage of M1 is the drain-source voltage of M2, then $g_{m,1}v_{gs,1} = g_{m,1}v_{ds,2}$. As $v_{ds,1} = -v_{ds,2}$ (because of the differential output voltage) then $g_{m,1}v_{gs,1} = -g_{m,1}v_{ds,1}$. Not considering the capacitances and the conductance g_{ds},$-g_{m,1}v_{ds,1}$ is the current going through $v_{ds,1}$, then $-g_{m,1}$ can be seen as a negative resistance between drain and source.

Then the total equivalent conductance of this block is:

$$G_{eq} = -\frac{g_m}{2} + g_{ds} \tag{2.9}$$

Assuming that in the bias point the transistor is in the saturation region, $g_{ds} \ll g_m$ and then:

$$G_{eq} \cong -\frac{g_m}{2} = -G_m \tag{2.10}$$

Using the ACM transistor model [26], the expression of the $C_{eq,-Gm}$ in saturation is:

$$C_{eq,-Gm} = 2{\cdot}C_{ov,gd} + \frac{C_{ov,gs} + C_{jd,db}}{2} + \frac{(n-1)C_{ox} + \left(\frac{2}{3}C_{ox}(\sqrt{1+i}-1)\frac{\sqrt{1+i}+2}{(\sqrt{1+i}+1)^2}\right)}{2n} \tag{2.11}$$

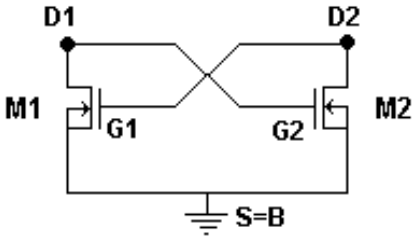
where n is the slope factor [36], slightly dependent on the gate voltage, greater than one and usually smaller than two. i is the normalized current [26]:

$$i \cong \frac{I_D}{I_S} \tag{2.12}$$

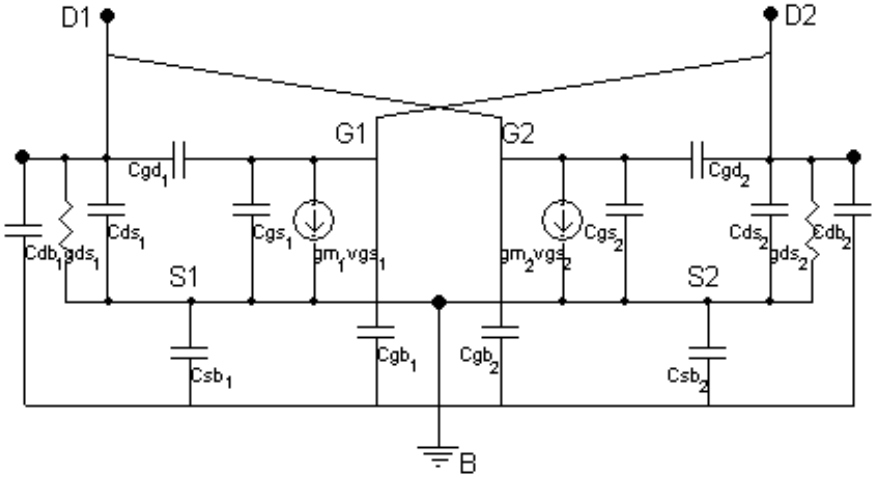
and

$$I_S = \mu n C_{ox} \frac{U_t^2}{2} \frac{W}{L} \tag{2.13}$$

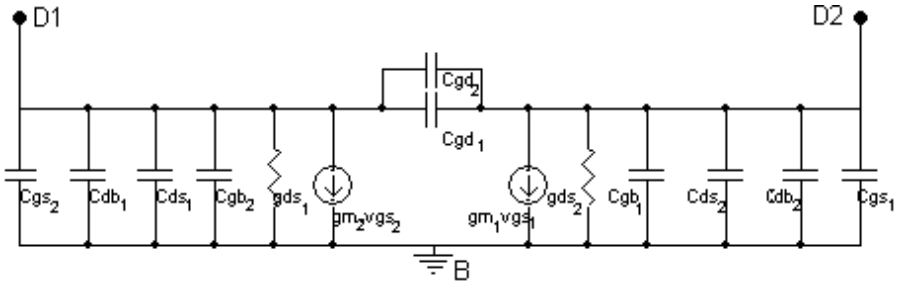
where μ is the carrier mobility, C_{ox} is the oxide capacitance per unit area, U_t is the thermal voltage and W and L are the width and length of the transistors.



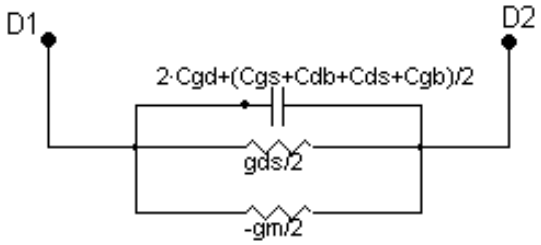
(a) Cross-coupled block



(b) Complete model



(c) Simplified model



(d) Equivalent simplified model

Figure 2.4: Small signal cross-coupled block models

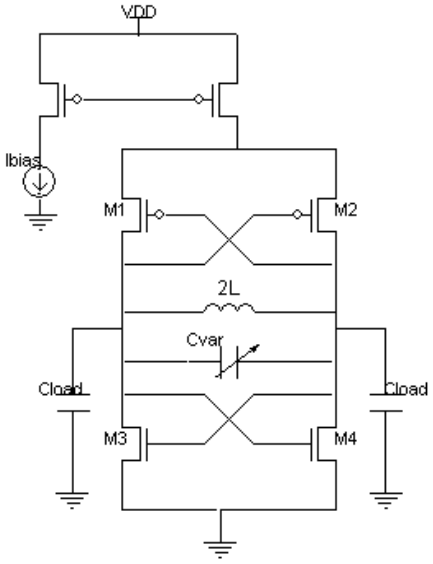


Figure 2.5: Complementary VCO topology used in this work

2.4 Complementary cross-coupled -Gm LC VCO

As it has been already said, the VCO used in this work is the complementary cross-coupled -Gm LC VCO with a pMOS current source (see Fig. 2.5). We have decided to work with a complementary topology because of its very good phase noise response with respect to the one that uses a nMOS pair. We also used a pMOS current source because the $1/f$ noise of pMOS is generally found to be less than for an nMOS one with the same dimensions (a deeper study of the phase noise subject will be done in Chap.3).

The physical model of this VCO topology considering the cross-coupled block model and the parasitics of the varactor and inductor is shown in Fig.2.6(a). The inductor value is L and it has associated a conductance $g_{L,par}$ and a capacitance C_L. The varactor's capacitance is C_{var} and its associated conductance is g_{var} (its inductance is neglected) -the parasitics of the inductor and varactor are studied in Chaps. 4 and 5-. The tank conductance is:

$$2g_{tank} = g_{L,par} + g_{var} + g_{ds,n} + g_{ds,p} \tag{2.14}$$

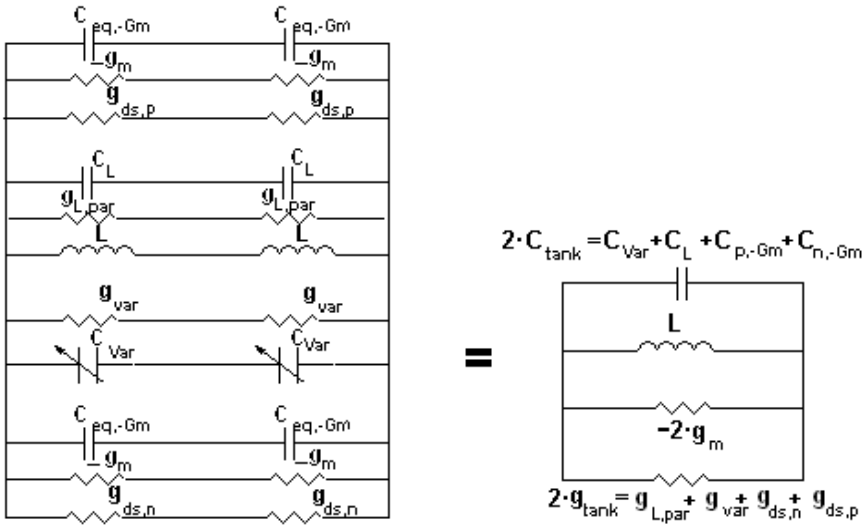
In Fig. 2.6(b) is the simplified model of this circuit.

This circuit oscillates when the Eq.2.6 is met. If this equation is separated in the imaginary and real part, are obtained the following two equations:

$$2 \cdot g_m = g_{tank} \cong g_{L,par} \tag{2.15}$$

and

$$f_0 = \frac{1}{2\pi\sqrt{L \cdot C_{tank}}} \tag{2.16}$$



(a) Complete model (b) Simplified model

Figure 2.6: Small signal quasi-static cross-coupled complementary VCO model

with

$$C_{tank} = C_{Var} + C_L + C_{n,-Gm} + C_{p,-Gm} \tag{2.17}$$

As the VCO is usually loaded with a non-negligible capacitance C_{load} (see Fig. 2.5) this must be taken into account in the C_{tank}:

$$C_{tank} = C_{var} + C_L + C_{n,-Gm} + C_{p,-Gm} + C_{load} \tag{2.18}$$

The condition of oscillation is (see Eq. 2.15)

$$g_m \geq g_{tank}/2 \tag{2.19}$$

Consequently, when a VCO is designed, it is usual to take a more conservative relation between the g_m and the tank conductance using the oscillation factor α:

$$2 \cdot g_m = \alpha \cdot g_{tank} \tag{2.20}$$

The oscillation factor has an arbitrary value, usually equal to 3 (which is considered conservative). This factor gives security to the design; if it is considered almost 1, it is probable that the current value would be lower but it is also probable that the oscillator does not start because of the spread in the value of the VCO components. In the Sec.2.6 there will be a deeper explanation on this matter.

Usually the conductances g_{ds} and g_{var} are low enough respect of the $g_{L,par}$ to be neglected.

2.5 Design Methodology

The design methodology presented here can be used in any of the VCO topologies shown previously, but it is focused on particularly the cross-coupled complementary -Gm LC VCO.

The specifications of the VCO are very related with the system in which it is part. The VCO designed here will be part of a Phase Locked Loop (PLL), whose specifications of power and phase noise are rigorous so that it can be used in communication circuits (as transmitters and receivers) which fulfill the IEEE 802.15.4 standard. The VCO can modify substantially the phase noise or power consumption values [37] of a PLL. Thus, one of the most important VCOs specifications are the maximum power consumption and the maximum phase noise (and sometimes the minimum peak output voltage).

As this VCO has on-chip inductors and these take substantial silicon area, the total VCO area is usually an important fraction of the total area of the system in which it is embedded. For this reason, the maximum VCO total area is also specified. The on-chip inductors are strongly conditioned by this requirement.

The VCO physical parameters to be found in the design flow are: the inductance value and its parasitics, the varactor's value and its characteristics, the size of the pMOS and nMOS transistors and the size of the bias current pMOS transistors. It has to be considered the parasitics of the layout in the design -usually capacitances at the working frequencies- and the load capacitance C_{load} of the load of the VCO.

One important design parameter used in this methodology is the transconductance-to-current ratio g_m/I_D [25]. This ratio can be expressed in terms of the normalized current i (Eq.2.12) [33]:

$$\frac{g_m}{I_D} = \frac{2}{nU_t(\sqrt{1+i}+1)} \tag{2.21}$$

As $i = I_D/I_S$ and $I_S \propto W/L$ then

$$i = k \cdot I_D/(W/L) \tag{2.22}$$

with

$$k = \frac{2}{\mu n C_{ox} U_t^2} \tag{2.23}$$

It means that g_m/I_D can be plotted versus $I_D/(W/L)$. This curve is a characteristic curve that depends only on the technology. Particularly this characteristic curve is very useful as it relates the transistor g_m/I_D with g_m knowing the drain current I_D (and viceversa); or relates the transistor aspect ratio W/L with g_m knowing I_D. Its typical behaviour is showed in Fig.2.7, where it is plotted the measured characteristic curve of g_m/I_D of the nMOS transistor $0.35\mu m$ technology.

The technology used also determines the characteristics of:

- the inductance: its value L, the quality factor Q, the resistive losses $R_{L,par}$.

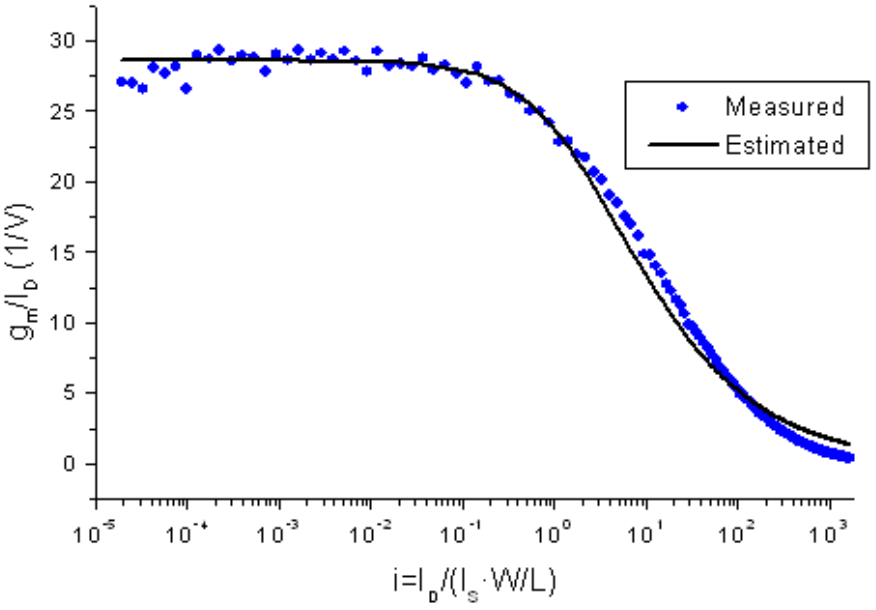


Figure 2.7: g_m/I_D **measured and estimated for a** $L = 0.35\mu m$,$W = 200\mu m$ **nMOS transistor (estimation calculated implementing the ACM model [33] in a Matlab routine, with n=1.25)**

- the varactor: its capacitive curve, the VCO gain K_{VCO}.
- the transistors: the parasitic capacitances and g_m.

From Eq.2.15 and the assumption that $g_{tank} \approx g_{L,par}$, $g_m = \alpha \cdot g_{L,par}/2$. Then, if g_m/I_D of the transistors M_i,[i=1..4] is increased while α and the inductance electrical characteristics (L, $g_{L,par}$,C_L) are fixed, g_m is set and I_D decreases (with $I_D = I_{bias}/2$). It leads to a reduction in the VCO power consumption. However, the minimum possible value of I_D is limited by the maximum oscillator phase noise value specified [38] [39], as it increases when I_D drops (the Phase Noise behaviour will be studied in Chap.3). It is also limited by the parasitic capacitances of the transistors M_i, i=1..4 (see Fig. 2.5), since an increment in g_m/I_D with g_m constant produces an increment in the transistor's width[33]:

$$W = L \cdot g_m \cdot \frac{k g_m/I_D}{\frac{4}{nU_t}\left(\frac{1}{nU_t} - g_m/I_D\right)} \tag{2.24}$$

An increment in the transistor width W also restricts the oscillation frequency and diminish the tuning range. It is because a higher W is equivalent to higher transistor parasitic capacitances -which reduces the possible varactor capacitance or makes it negative-.

Considering the previous discussion, the proposed VCO design methodology is presented in the scheme of Fig.2.8. Given an inductor value L and a oscillation frequency f_0, the inductor dimensions and its parameters are calculated ($g_{L,par}$ and

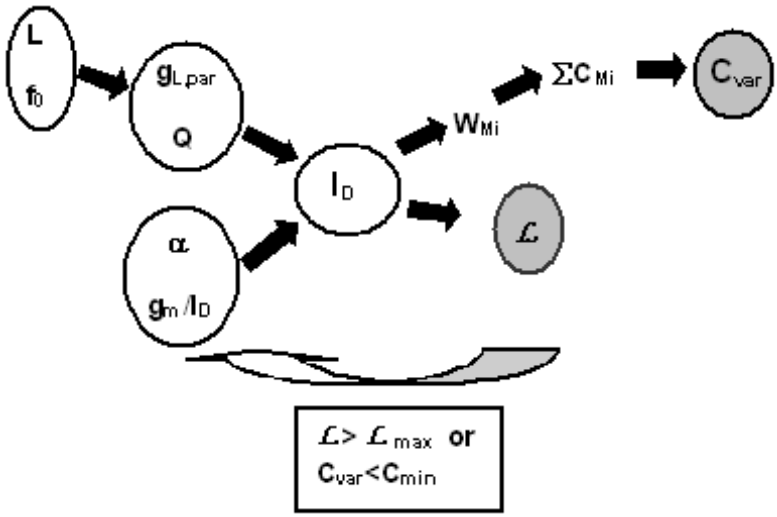


Figure 2.8: Design methodology

Q among others). With these parameters, g_m/I_D and α, it is found I_D. Using the transistor's characteristic curves of Fig.2.7 or the Eq.2.21, the width of Mi's are obtained. At last, the varactor capacitance C_{var} is calculated. If the phase noise $\mathcal{L}$ is higher than $\mathcal{L}_{max}$ or the varactor capacitance C_{var} is less than a $C_{var,min}$ then the g_m/I_D or the L chosen have to be changed.

With the previous discussion about the complementary VCO and the design methodology several possible situations can be pointed out:

- Using Eq.2.24, if g_m/I_D is fixed, when the inductor value increases the transistor width W decreases (see Fig.2.9). The reason is that the rise of the inductor also increases the inductor series resistance, decreasing $g_{L,par}$ and hence the g_m of the transistors (see Eq.2.15).

- Also from Eq.2.24 for a fixed inductor, if g_m/I_D rises then W increases because g_m is constant. This behaviour is shown in Fig.2.9.

- Usually the inductor capacitance is higher than the transistor capacitances and then if the inductor value grows, despite the transistor width falls, the varactor capacitance decreases (remember that the total VCO capacitance must fulfill the Eq. 2.16) (see Fig.2.10, C_{var} versus L).

- For a constant inductor value, the g_m is constant and if g_m/I_D increases, from Eq.2.24, the W increases and the varactor capacitance decreases. The total capacitance of the VCO can be so high that C_{var} would fall below zero (see in Fig.2.10 the plot of C_{var} versus g_m/I_D)

The VCO output voltage is a specification which has been taken into consideration in the methodology design but it has had less influence that the phase noise

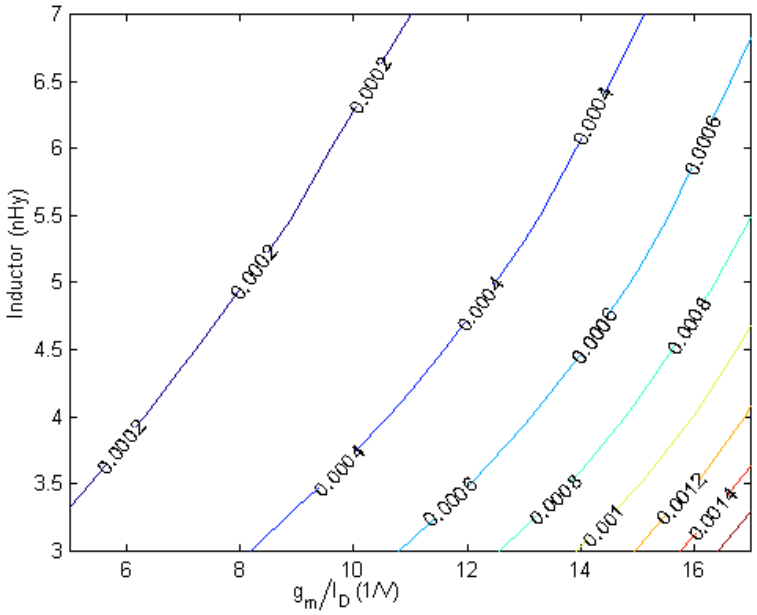


Figure 2.9: Width of nMOS cross coupled transistors vs. g_m/I_D and L

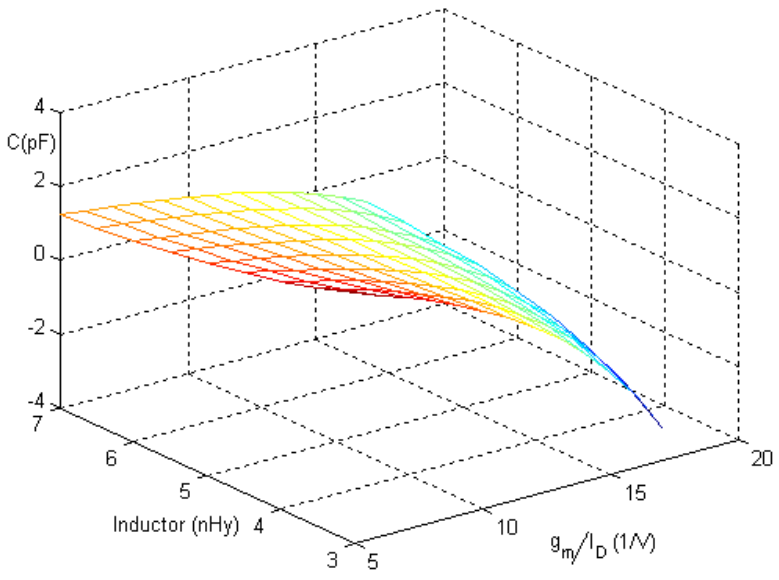


Figure 2.10: Varactor capacitance vs. g_m/I_D and L

and consumption constrain. The output voltage amplitude of the oscillation can be approximated as [21]:

$$V_{out} = \frac{4}{\pi}\frac{I_{bias}}{g_{tank}} \cong \frac{4}{\pi}\frac{I_{bias}}{g_{L,par}} \tag{2.25}$$

with $I_{bias} = 2 \cdot I_D$. The intuitive idea of this expression is that when the VCO oscillates the LC tank resonates and its impedance is equal to the tank resistance. The tank attenuates the harmonics of the current and leaves the fundamental of the input current. A differential voltage of the Eq.2.25 is generated with this current if a rectangular current waveform is considered [21].

It means that a high output voltage amplitude is reached when the current I_D grows, which goes against the reduction of the power consumption. Then, as we decided to choose the VCO with the lower possible current consumption , then its output amplitude is fixed and the output voltage constrain has not been considered. This type of oscillators usually have high current values and the equivalent inductor conductance is not small. It is expected that the designed VCO peak to peak output voltage amplitude would be around 1V.[3]

The quiescent output voltage depends on the zone in which the transistor works. In this work the transistor is biased in such a way to be in moderate inversion, then the V_{GS} is around U_t (see the chapter four of [35]).

2.6 Amplitude stabilization mechanism

Until now we have accepted that the oscillator starts but it has not been shown how the oscillator arrives to the steady-state. To give a brief and qualitative explanation it will be supposed in the following discussion that the transistors of both cross-coupled blocks are in saturation.

In the following it will be illustrated the control amplitude mechanism of the VCO. In this kind of oscillators the output voltage V_1 is sinusoidal but not the output current, which has all the possible harmonics of the working frequency f_0 as it is shown in Fig.2.12:

$$V_{out}(t) = V_1 \cdot \cos(\omega_0 t) \tag{2.26}$$

$$i_{out}(t) = \sum_{n=1}^{\infty} i_n \cos(\omega_0 t) \tag{2.27}$$

Using the scheme of Fig.2.11, and considering that i_1 is the fundamental component of the drain current,it is defined the transconductance G_{m1} as:

$$G_{m1} = \frac{i_1}{V_1} \tag{2.28}$$

[3]This amplitude was not sufficient for the PLL to work correctly, so it has been used a preamplifier to increase this value

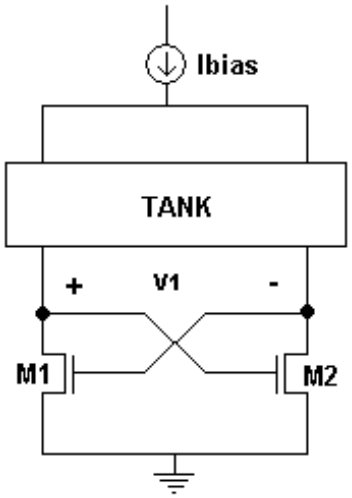


Figure 2.11: Amplitude stabilization mechanism in a -Gm block

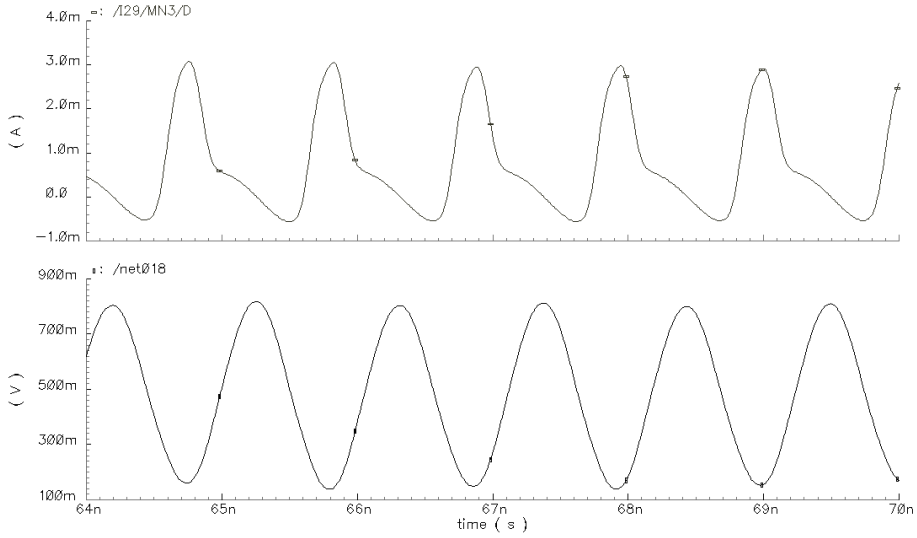


Figure 2.12: Drain current of the VCO cross-coupled transistors vs. time

where G_{m1} is the large signal transconductance at ω_0, i_1 and V_1 are the drain current and the drain voltage of the transistor M_1, respectively. When the voltage V_1 is very small we are working at small-signal and then

$$G_{m1} = g_m = \frac{2I_S}{nU_t}(\sqrt{1+i} - 1) \cong \frac{I_S}{nU_t} i = \frac{I_D}{nUt} \quad V_1 \ll U_t \tag{2.29}$$

with I_S, U_t, n and i as defined previously.

When we are working in large-signal, the output current tends to be sharp

spikes [39], whose average value is I_{bias}. Then the fundamental current i_1 is:

$$i_1 = \frac{2}{T_0}\int_0^{T_0} i_{out} cos(\omega_0 t)dt \cong \frac{2}{T_0}\int_0^{T_0} i_{out}dt = 2I_D \tag{2.30}$$

where $T_0 = 1/(2\pi f_0)$ is the signal period. The approximation is valid at large-signal because the peak of current will occur when $cos(\omega_0 t) \approx 1$, and around this point the current i_{out} is considered to be almost 0. Then

$$G_{m1} = \frac{2I_D}{V_1} \quad V_1 \gg U_t \tag{2.31}$$

Comparing Eq.2.29 with Eq.2.31, it is clear that G_{m1} in large signal is lower than G_{m1} in small signal and also that the large signal transconductance is inversely proportional to the voltage V_1. The previous discussion shows that the VCO has a negative feedback which controls the output voltage amplitude.

2.7 Moderate inversion design

This work has been focused on design a 910MHz VCO with cross-coupled transistors in moderate inversion. This choice has been done for various reasons. Firstly, we want to show that the g_m/I_D methodology [25] can be used in radio-frequency and that is is possible to work far from strong inversion with advantageous trade-offs in the VCO performance (reduction of power consumption in the VCO without jeopardizing the phase noise).

In Fig.2.7 the current consumption and the varactor capacitance C_{var} are given for different values of g_m/I_D and different inductor values, using a $0.35\mu m$ technology. To give some numeric examples, the bias current of the transistor and C_{var} are given for various combinations of g_m/I_D and L in Tables 2.1 and 2.2 respectively.

$g_m/I_D(1/V)$	**L(nHy)**	I_{bias}(mA)
5	**3**	13
5	**7**	4.2
8	**3**	8
8	**7**	2.6
11	**3**	5.8
11	**7**	1.9

Table 2.1: Bias current of each cross-coupled transistors versus g_m/I_D and inductor L

As it can be seen in these pictures and numbers, the bias current decreases more than a half when the transconductance-to-current ratio increases from 5 to 11, with a fixed inductor(for a 7nHy inductor I_{bias} is 4.2 and 1.9mA respectively). It means that working at $g_m/I_D = 11$ -at a low-moderate inversion zone-, we are

$g_m/I_D(1/V)$	**L(nHy)**	$Cvar$(pF)
5	**3**	5.8
5	**7**	2.4
8	**3**	3.6
8	**7**	1.8
11	**3**	1.4
11	**7**	1.1
12	**3**	0.4
12	**7**	0.8

Table 2.2: Capacitance of each varactor versus g_m/I_D and inductor L

reducing roughly to a half the power consumption. If we were able to work at weak inversion with $g_m/I_D = 17$, for example, the bias current would be around 1.3mA for an $L = 7nHy$, which is not so lower than the bias current of $g_m/I_D = 11$. The current consumption from moderate inversion to weak inversion does not change so much but what does increase is the width of the transistor, which rises the transistor capacitances so much that at $g_m/I_D = 17$ the varactor capacitance would be $-8pF$, a negative capacitance!.

In case of working in strong inversion the current consumption increases considerably. In Sec.3.6 it is shown that the improvement in phase noise when working in strong inversion does not compensate the increment in the power consumption.

Then it is in moderate inversion where a good trade-off between power consumption and physical constrains is observed.

In the Chap.3 it can be seen that the phase noise values in moderate inversion are acceptable to be used in real applications.

2.8 Layout design and its consequences in the design methodology

The layout design is a very delicate and difficult task in radio-frequency because lots of effects begin to appear at these bands and commonly they degrade the performance of the system, specially if a careless layout is done. Some effects are: the appearance of transmission lines, inductive, capacitive and resistive parasitics, the antenna-effect, substrate coupling and others. But which is also true is that many of these problems can be considerably reduced if a good layout is performed.

The transmission lines and antenna-effect are almost neglected if the higher dimensions of the circuit are below one tenth of the wave length (in the working band $\lambda/10 \approx 30mm$, which has never exceeded)[40]. The coupling substrate is important when more than one circuit with different signals are used, for example when a power amplifier and a VCO are used, both circuits have to be shielded using a guard ring connected to ground, to effectively fix the substrate to the ground voltage [41].

In case of the parasitics of the interconnecting wires we only considered their parasitic capacitances and not their resistance parasitics because most of the wires of the design are short and the ones that are a bit more long were made wide enough to be discarded the resistive effect. For example, the metal wire that connects the drains of the transistors nMOS and pMOS has a length of $100\mu m$ and a width of $10\mu m$ approximately, and is one of the largest traces of the circuit. The sheet resistance of the metal is $70m\Omega_{square}$, then the total resistance of this trace is around 0.7Ω. For a bias current of $1mA$ the voltage drop between the drains is around $0.7mV$, negligible respect of the signals of the VCO.

Regarding the transistors, as the width W of them is very large (hundreds of μm), the gate resistance due to the resistive poly-silicon and the contacts has a considerable value. To decrease this resistance a multi-fingered layout has been made, which means that N transistors with a width of W/N are all connected in parallel, as it is seen in Fig.2.14. As the gate resistance of each transistor is in parallel with the other gates, the result resistance is around N times smaller than the simple structure. However this kind of layout needs a lot of interconnection wires which increases the parasitic capacitances.

From what has been discussed, in the design methodology the layout parasitics have to be considered. In this work, the resistances of the multi-fingered structure transistors and of the wires are not considered in the methodology. Also the parasitic inductances are neglected. Therefore the unique parasitics considered are the capacitances. The following is a detailed discussion on this matter.

Due of the need of maintaining the symmetry of the cross-coupled complementary architecture, the layout has been disposed with an axial symmetry as it is in Fig.2.15. This disposition is of great importance specially in terms of phase noise minimization.

Parasitic capacitances

The 900MHz -Gm LC VCO designed in this work occupies an important amount of silicon area because:

1. the inductors are quite big (each one can take tenths of thousands of μm^2) because the working frequency is not too high.

2. as the varactor capacitance has been implemented with a MOS transistor, to reach the wanted capacitance the varactor width is considerable.

3. as the transistors were designed to work in moderate inversion they have widths of hundreds of μm.

The influence of these three blocks in the total parasitic capacitances are considered separately to study their influence. We took care of these parasitics in the post-layout stage by adjusting the varactor size to achieve the wanted frequency.

The inductors' parasitic capacitances will be studied in Chap.4 and these are quite well-known so they are added from the beginning in the VCO methodology design when the inductor parasitics are calculated. But it has to be mentioned that

the traces that carry the signals to the inductors have a non-negligible length which cause parasitic capacitances.

The layout of the cross-coupled transistors can be made in two different ways. One is to design interlaced transistors and the other is to design each transistor separately. In Figs.2.16(a) and 2.16(c) are depicted the complete view of the separate and interlaced nMOS cross-coupled block, respectively. In the design both have been done as it is seen in Fig.2.16(a). The former has much more parasitic capacitances than the last one because the capacitances that appear with the interconnect wires increases considerably the total parasitic capacitances. If the detail of the interlaced layout of Fig.2.16(b) is compared with the interlaced layout of Fig.2.16(d) it is visible that there is a larger quantity of interconnect wires in the former one.

However separate transistors decrease the matching of the g_m, despite the large size of the transistors diminish this effect. As it is very difficult to estimate the total parasitic capacitances added by the wires because of the need of several iterations between the algorithm results and the designed layout, in this work the separate-transistor architecture has been chosen.

To maintain the symmetry of the layout the varactor has to be divided into two parts. The same situation that appeared with the cross-coupled transistor block is repeated here: each transistor of the varactor can be drawn separately or interlaced with the other one. In this case it has been found that it is even more difficult to interlace both transistors than in the case before mentioned. Also in this situation the parasitic capacitances are very large. Then we decide to use the separate layout in our design. The complete layout and a detail of the connections of the multi-fingered transistors are shown in Figs.2.17(a) and 2.17(b), respectively.

2.9 Current Source design

The election of the current source to be used and its design has been studied in several works (for example in [17] [21]). It has been payed so much attention to this subject because a bad choice in the type of the source or in the sizing would jeopardize the phase noise of the complete VCO.

In [17] it has been shown that the best current source is a current mirror of pMOS tansistors. Also the size of these transistors has to be as large as possible to reduce the thermal and $1/f$ noise because they are inversely proportional to the width of the transistor[33][42]. The size of the current souce is $W = 2000\mu m$ and $L = 1\mu m$. The final layout view of the current source is in Fig.2.18

It can be added a capacitor in parallel with the bias current source to reduce the oscillation of the source of the cross-coupled pMOS transistors and therefore the phase noise, but its drawback is that it decreases the output impedance of the source voltage V_{DD} making the VCO more susceptible to voltage supply variations [21].

2.10 Final Design

Considering the foregoing analysis and design methodology the VCO design is given in this section. The final election of the variables involved attempted to fulfill the compromise between power consumption and phase noise by working in moderate inversion, the requirements of output voltage and the maximum area budget. The considerations of possible technology variations in passive and active devices have also been considered.

It has been created an algorithm in Matlab [43] that implements the design methodology proposed in Fig.2.8. The design has been done in a $0.35\mu m$ CMOS standard technology; the supply voltage used is $V_{DD} = 3$ Volts and the central frequency is 915MHz. The design space has been obtained varying the inductor and the g_m/I_D. This election has been done because:

- the inductor is a difficult component whose characteristics -series resistance and quality factor- modifies substantially the behaviour of the VCO;
- the transconductance-to-current ratio variation modifies the current consumption and the transistor size.

Also with the series resistance of the inductor it can be obtained the g_m of the transistors and with the g_m/I_D the drain current needed. And finally, as it has been said previously, we want to test the g_m/I_D methodology [25] in this kind of circuits.

In the design we use a limited number of these variables: L varies between 3nHy and 7nHy at steps of 1nHy, and $g_m/I_D[1/V]$ goes from 5 to 17, at steps of $1V^{-1}$. We considered that, due to the variations in the technology, a smaller simulated step would not be neither useful nor clear. The final design values of g_m/I_D and L obtained from the algorithm are given in Table 2.3.

Design Parameter	**Value**
L (nHy)	5
g_m/I_D	11

Table 2.3: Final values of L and g_m/I_D obtained from the implemented algorithm

As we would like to design the VCO transistors in moderate inversion arise the problem discussed in Sec.2.8: the value of C_{var}. In this particular design the variable that fundamentally limits is the C_{var}, as it can be seen in Table 2.2. The C_{var} decreases very rapidly after $g_m/I_D = 11$ as it is shown in Fig.2.13(b) so a good compromise has been found in this value.

The transistor length is the minimum of the technology: $0.35\mu m$ to have the maximum f_t available.

In Table2.4 there are the most important VCO variables:

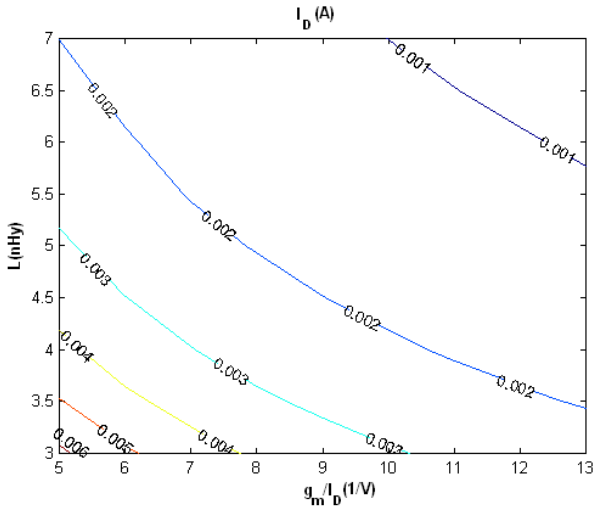
Final Layout

Design Parameter	Value	Design Parameter	Value
L	5nHy	$R_{L,par}$	90Ω
$C_{L,eq}$	$90fF$	C_{load}	600fF
I_D	$1.5mA$	g_m	$0.030S$
C_{var}	700fF	W_{var}	$1600\mu m$
W_n	$336\mu m$	W_p	$782\mu m$

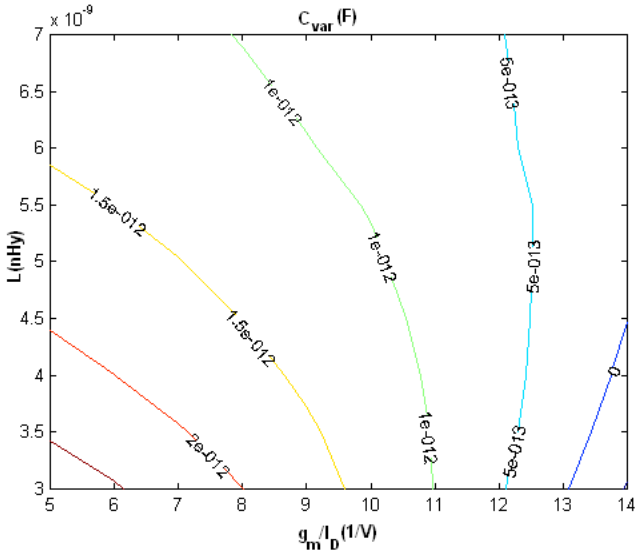
Table 2.4: Final values of several variables of the VCO design

The final layout of the VCO is depicted in Fig.2.19. All the blocks except of the inductors (see Chap.4) have been previously presented as well as a detailed view of them. The layout obeys the floorplan given in Fig.2.15. The total silicon area occupied is of $600\mu m$ by $500\mu m$ approximately (around $0.3mm^2$).

All the active blocks have been surrounded by double guards to isolate them and to avoid latch up. The inductors have been partially guarded to ground to decrease the substrate noise coupling though the inductors [44] [45].



(a) I_D vs g_m/I_D and L



(b) C_{var} vs g_m/I_D and L

Figure 2.13: Drain current of the cross-coupled transistors and varactor capacitance versus g_m/I_D and inductor value L

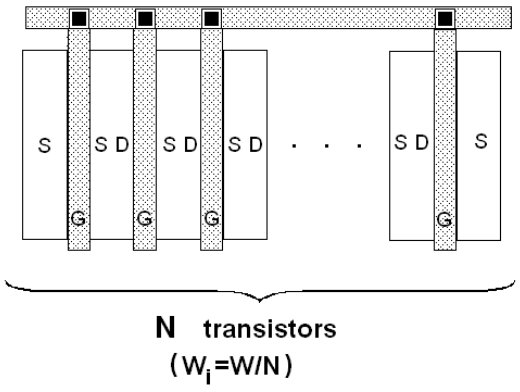


Figure 2.14: Multi-fingered layout of a transistor with width W

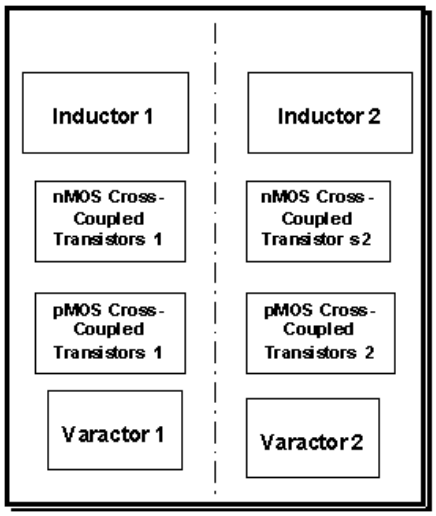
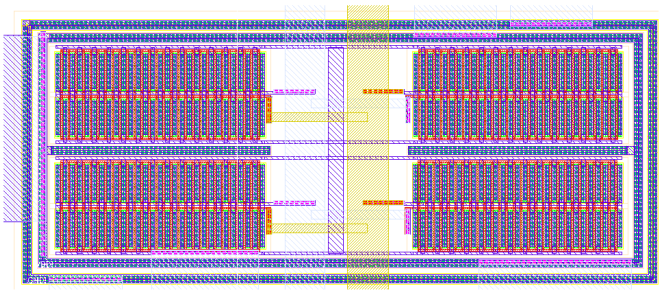
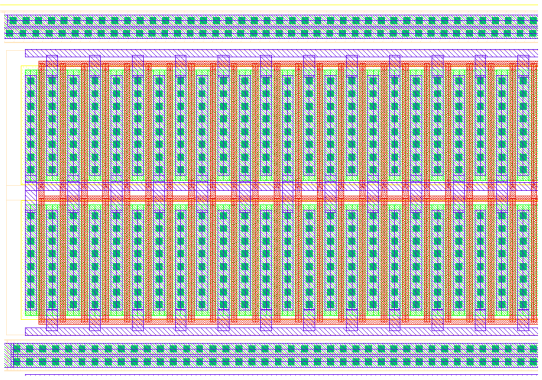


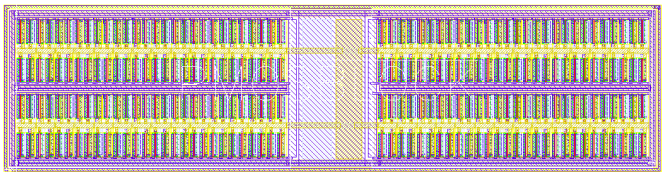
Figure 2.15: Floorplan of the cross-coupled complementary -Gm LC VCO



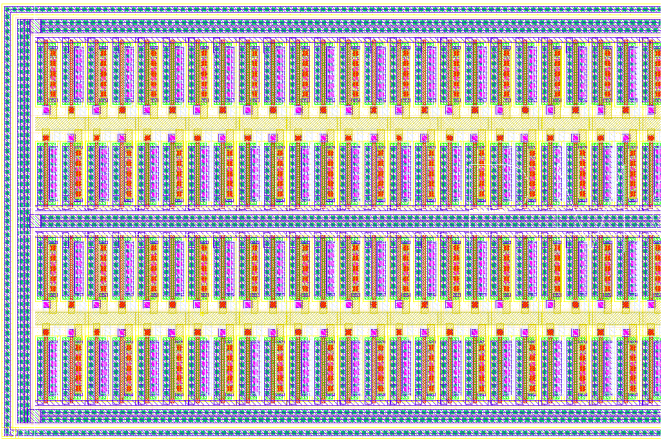
(a) Final layout of the pMOS block



(b) Detail of the structure of the final pMOS block

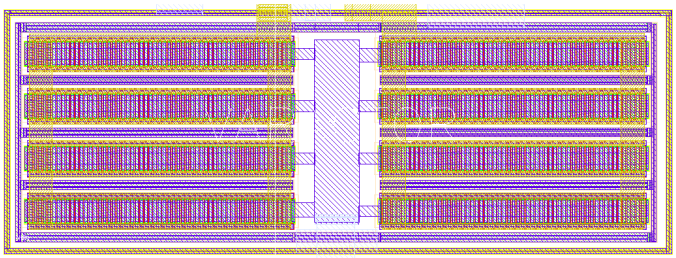


(c) Interlaced layout of the pMOS block (not used in the final VCO design)

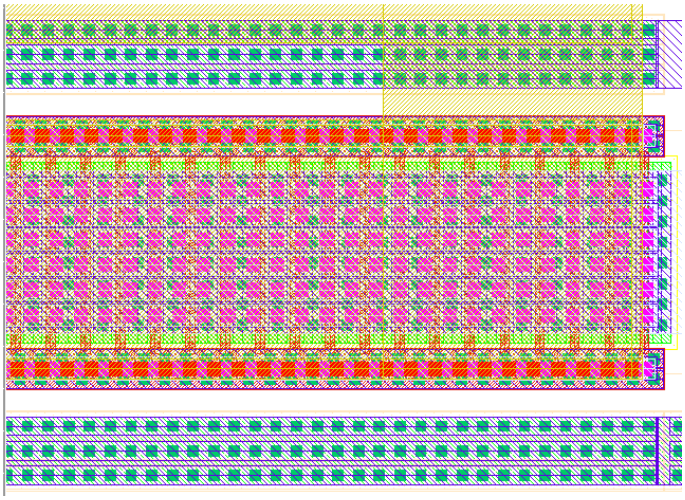


(d) Detail of the structure of the interlaced pMOS block

Figure 2.16: Separate transistor layout and interlaced layout of the pMOS cross-coupled block



(a) General view of the final varactor (the two separate group of transistors are clearly appreciated)



(b) Detail of the varactor layout showing the multi-fingered transistors interconnected

Figure 2.17: Final varactor layout

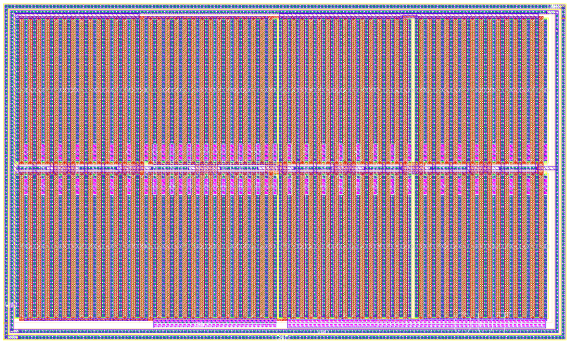


Figure 2.18: Current source layout

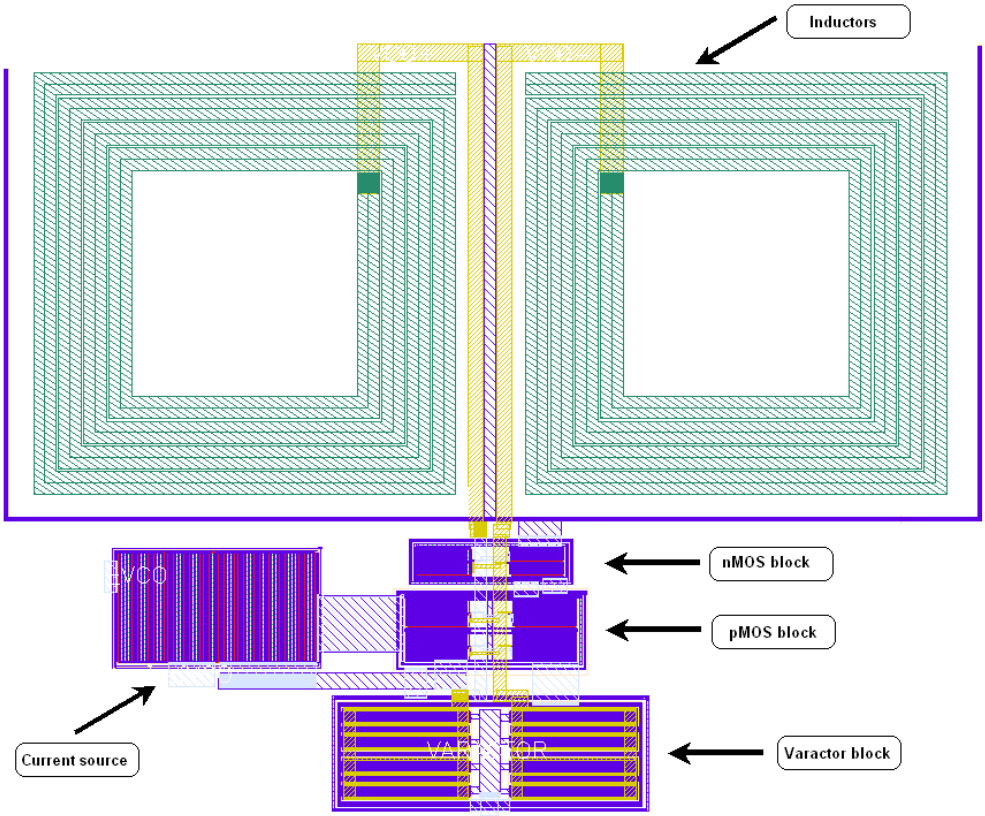


Figure 2.19: Final layout of the fabricated VCO

Chapter 3
Phase Noise in LC VCOs

3.1 Introduction

In this chapter the Phase Noise in electrical oscillators is studied. A general definition of phase noise for a typical oscillator and particulary expressions of it for LC-VCO are provided. Also, there are described their most important models, divided in Lineal Time Invariant (LTI) and Lineal Time Variant (LTV) ones. The noise sources in the complementary LC-VCO is studied, and expressions of its phase noise are derived. Finally the calculus and simulation results of the designed -Gm LC VCO are shown.

3.2 Phase Noise Definition

When an ideal oscillator is modelled, its output can be expressed as:

$$V_{out} = A\cos[\omega_0 t + \phi] \tag{3.1}$$

where amplitude A and arbitrary phase ϕ are constant values. Therefore, the spectrum of this signal are two impulses at frequencies $\pm f_0 = \frac{\omega_0}{2\pi}$, where f_0 is the frequency of oscillation [46].

However, when using a real oscillator, the amplitude and the phase are affected by noise and are time-variant, so the output is now:

$$V_{out}(t) = A(t)\cos[\omega_0 t + \phi(t)] \tag{3.2}$$

were $\phi(t)$ is called the excess phase of the output. The spectrum of this signal has sidebands close to the frequency of oscillation f_0.

These instabilities in amplitude and phase can be characterized quantifying the single sideband noise spectral density around the carrier ω_0 (see Fig.3.1). It has units of decibels below the carrier per hertz (dBc/Hz) and is defined as [32]:

$$\mathcal{L}_{total}(\Delta\omega) = 10\log\frac{P_{sideband}(\omega_0 + \Delta\omega, 1Hz)}{P_{carrier}} \tag{3.3}$$

where $P_{sideband}(\omega_0 + \Delta\omega, 1Hz)$ is the single sideband power at an offset $\Delta\omega$ from the carrier measured within a bandwidth of 1 Hz and $P_{carrier}$ is the power of the signal at ω_0. This noise characterization includes the effect of both amplitude and phase fluctuations, which is a disadvantage because it is not possible to know them separately. On the other hand, this parameter has the advantage that is easily measurable using a Spectrum Analyzer because the values of $P_{sideband}(\omega_0+\Delta\omega, 1Hz)$ and $P_{carrier}$ are easily obtained.

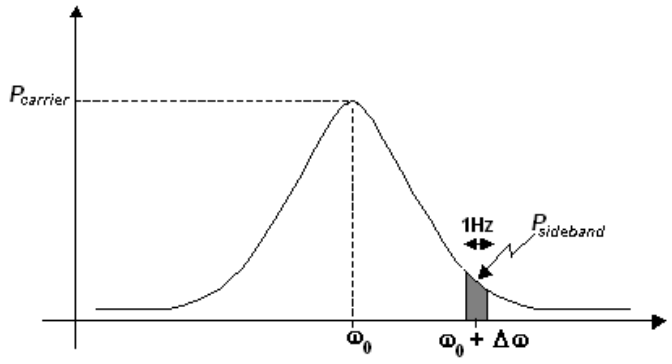


Figure 3.1: Spectrum of the signal around ω_0, showing the single sideband power at $\omega_0 + \Delta\omega$ in grey

In this work it is assumed that the amplitude noise effect is reduced -and almost eliminated- due to the amplitude-limiting oscillator's mechanism. But this mechanism does not reduce the phase noise, which is at last, the dominant noise in the oscillator. Then, $\mathcal{L}_{total}$ is almost dominated by the effect of the phase noise, and:

$$\mathcal{L}_{total}(\Delta\omega) = \mathcal{L}_{phase}(\Delta\omega) = \mathcal{L}(\Delta\omega) \tag{3.4}$$

Eq.3.3 is the usual definition of the Phase Noise.

The phase noise is an important characteristic of the VCO for various reasons. In a receiver -if it is sufficiently high- less channels can be used in the band as they interfere with each other. In transmitters and receivers when a signal is downconverted (upconverted) using the output signal of the VCO with high phase noise, the downconverted (upconverted) signal has lots of components at other unwanted frequencies around the frequency of interest. In the transmitters it generates a diffuse constellation of symbols making difficult to receive them correctly.

3.3 Review of existing Phase Noise Models

Various models have been developed to explain and describe the behaviour of the phase noise in oscillators. Two of the most important are the Leeson's model [47] and the one developed by Hajimiri and Lee [46]. The difference between them is that the former is a Linear Time Invariant empirical model (from now on LTI) while the last one is Linear Time Variant physically based model (LTV). In this section both models are briefly explained and their fundamental phase noise equations are shown.

3.3.1 Linear time invariant model

The models described in this section study the phase noise of an LC-oscillator. This circuit, visualized in Fig.3.2 is composed by a tank formed by the parallel of an

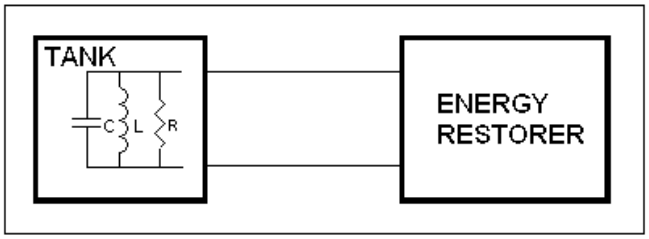


Figure 3.2: RLC oscillator

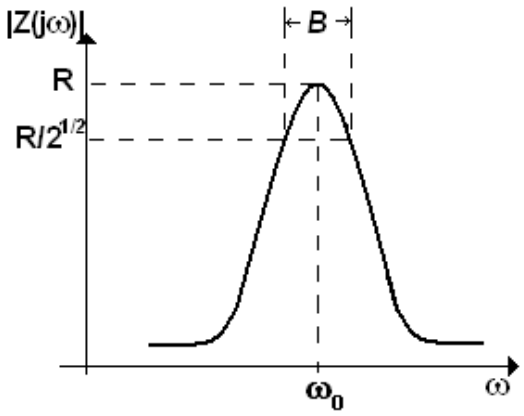


Figure 3.3: Equivalent tank impedance value.

inductor L, a capacitor C and a resistor R (the last represents the thermal losses of C and L, as they are not ideal components). It also has an energy restorer block, which brings back the energy lost in R; this element can be seen as a negative resistance of value -R. In this section this element will be considered as noiseless to simplify the study and make easy the explanation; but later on (in Sec.3.4) a detailed study of the common noise sources of this block is done.

In this simplified case and considering only the white noise, the only source of noise of this circuit is the tank resistance's white noise, which is represented as a current source with the spectral density given in Eq.(3.5).

$$\overline{i_n^2} = \frac{4kT}{R} \tag{3.5}$$

As it is shown in Fig.3.3, this circuit can be seen as a filter, then B can be defined as its pass-band bandwidth. The quality factor Q of this oscillator is defined as:

$$Q = \frac{R}{\omega_0 L} \cong \frac{\omega_0}{B} \tag{3.6}$$

The last equality is demonstrated in Sec.A.1 of Appendix A.5.

Working at offset frequencies $\Delta\omega$ with respect of the carrier, with $\Delta\omega \ll \omega_0$

($\Delta\omega \ll B/2$), and considering that the resistance of the tank is cancelled by the restorer block the equivalent impedance is approximately [32][48]:

$$Z(\omega_0 + \Delta\omega_0) \approx \jmath \frac{\omega_0 L}{2\frac{\Delta\omega}{\omega_0}} = \jmath \frac{R\omega_0}{2Q\Delta\omega} \tag{3.7}$$

This equation shows the 1/f passband characteristic around ω_0.

From Eqs.(3.6) and (3.7) it is obtained the spectral density of the noise power

$$\overline{v_n^2} = \overline{i_n^2}|Z|^2 = 4kTR\Big(\frac{\omega_0}{2Q\Delta\omega}\Big)^2 = 4kT\frac{\omega_0 L}{Q}\Big(\frac{\omega_0}{2\Delta\omega}\Big)^2 \tag{3.8}$$

Due to the $1/f$ characteristic of the oscillator around ω_0 (see Eq.3.7), the noise power spectral density expressed in Eq. 3.8 has a frequency dependency of $1/f^2$. Also, as it is expected, increasing the Q of the tank decreases the noise spectral density.

With Eqs.(3.3) and (3.8) it is possible to write the following expression of phase noise

$$\mathcal{L}(\Delta\omega) = 10\log\Big[\frac{2kT}{P_{carrier}}\Big(\frac{\omega_0}{2Q\Delta\omega}\Big)^2\Big] \tag{3.9}$$

Therefore to decrease the phase noise of the oscillator the quality factor of the tank can be improved or the power of the carrier signal must be increased.

The previous approach is useful because clarifies how phase noise appears. However, when this is compared with the experimental data, some differences arise. Firstly, the magnitude is higher because the tank loss is not the unique source of noise, e.g.: the limiter block is not ideal. Another difference is that the zone where the phase noise is proportional to $1/f^2$ does not continue indefinitely but asymptotically changes to a flat zone because of the filter characteristic of the tank at high offset frequencies. Finally, near the carrier frequency ω_0 the phase noise spectrum is not proportional to $1/f^2$ but to $1/f^3$.

To match the experimental data with the theory, Leeson [47] proposed the following empirical modifications to Eq.3.9:

$$\mathcal{L}(\Delta\omega) = 10\log\left(\frac{2FkT}{P_{carrier}}\Big(1+\Big(\frac{\omega_0}{2Q\Delta\omega}\Big)^2\Big)\Big(1+\frac{\Delta\omega_{1/f^3}}{|\Delta\omega|}\Big)\right) \tag{3.10}$$

The F parameter, also called *device excess noise factor* is an empirical fitting parameter. $\Delta\omega_{1/f^3}$ is usually taken approximately equal to the $1/f$ white noise corner $\Delta\omega_{1/f}$, but $\Delta\omega_{1/f^3}$ is not always similar to $\Delta\omega_{1/f}$ [46], this parameter is also considered an empirical parameter. The fact that these parameters cannot be determined from the geometry and architecture of the VCO makes difficult to use the Eq.3.10.

In some architectures, the value of F has an empirical expression. For example,

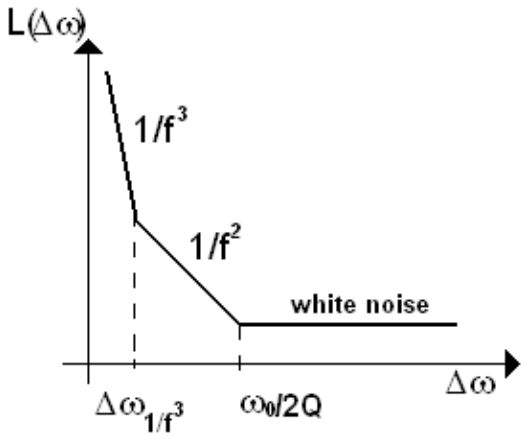


Figure 3.4: Asymptotic graphic of Phase Noise.

for a LC differential VCO it is possible to use the following expression [38]

$$F = 2 + \frac{8\gamma T I_{bias}}{\pi V_0} + \gamma \frac{8}{9} g_{mbias} R \tag{3.11}$$

where γ is called *noise factor* of a MOSFET; for a long channel MOSFET its value is typical 2/3 and for a short channel one it is approximately 2.5 [49](these values depend also on the inversion level; an interesting study of this matter is given in [35]). I_{bias} is the current given by the current source; V_0 is the VCO output voltage; R is the equivalent resistance of the VCO; and g_{mbias} is the transconductance of the bias transistor.[4]

The Leeson's model expressed in Eq.3.10 is a linear time invariant model which estimates much better the phase noise spectrum compared with Eq.3.9. However it has the drawback of being an empirical model and without any data from the VCO architecture behaviour ($\Delta\omega_{1/f^3}$ or F), this model cannot make any quantitative predictions.

It is not the case of LC-VCO's, where approximated expressions of the F parameter exist and good phase noise estimations are possible.

3.3.2 A linear time varying phase noise theory

This theory has been presented by Ali Hajimiri and Thomas Lee [32][39][46] and attempts to give a quantitative explanation of the phase noise of VCOs. It is not the idea of this section to explain deeply the complete theory but to give a brief insight into it and to show the most important results.

In the cited works there are revised two hypothesis used in the Lesson's model:

[4]The first term of F equation arise from the tank noise, the second is deduced from the differential pair noise and the last one is caused by the bias current noise. An interesting deduction of these terms is given in [38]

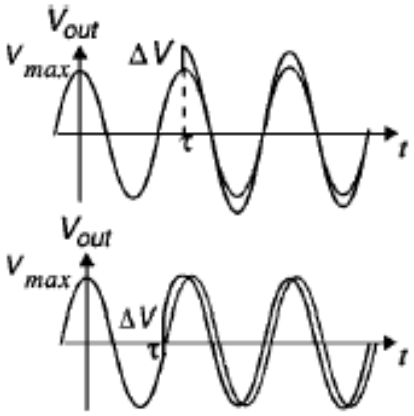


Figure 3.5: Impulse responses of LC tank. Taken from [32].

the linearity and the time-invariance.

The linearity assumption is maintained. Despite the oscillator is itself a non linear system because its signal amplitude is limited, the relation between the noise and the excess phase can be reasonably assumed to be linear if it is considered that the imposed perturbations are small compared to the main oscillation.

The time-invariance is, on the contrary, an erroneous assumption. A good example of this mistake is considering an LC lossless tank at which an impulse is added to the output signal, as it is shown in Fig.3.5. If the impulse is injected when the signal is a maximum, only the amplitude is modified; but if it is injected at zero-crossing times, only the phase changes. At other times, both amplitude and phase change. Then, depending on the time the injection occurs is the disturbance in the phase, which means that the system is time variant, and, what is more, is a *periodical* LTV system.

A current impulse at the input of the tank generates a change in the charge of the tank capacitor C without no change in the inductor current. Then a Δq in C generates a $\Delta V = \Delta q/C$.

The excess phase ϕ generated by a current impulse is directly proportional to the ΔV generated (see Fig.3.5), and can be written as:

$$\Delta\phi = \Gamma(\omega_0\tau)\frac{\Delta V}{V_{max}} = \Gamma(\omega_0\tau)\frac{\Delta q}{q_{max}} \tag{3.12}$$

where V_{max} is the maximum voltage of the capacitor, q_{max} is the maximum charge of C and $\Gamma(x)$ is a new function defined in this method, called impulse sensitivity function (ISF). It describes the sensitivity to the system to an impulse injected at a phase $\omega_0 t$. This function depends on the system and is completely different in LC VCOs and in ring VCOs, for example. The ΔV and Δq have to be normalized respect of the maximum voltage or charge of the capacitor to maintain the proportionality relation between phase and voltage, shown in Fig.3.5, without having

units.

To understand the behaviour of these kind of systems the unit impulse response for the excess phase is studied . This function will be used to show how the mechanism of the phase noise works.

Maintaining the same form as the excess phase of Eq.3.12, the impulse response can be written as follows:

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}} u(t-\tau) \tag{3.13}$$

where $u(t)$ is the unit step function.

For a input current i(t) the excess phase can be calculated as follows:

$$\phi(t) = \int_{-\infty}^{\infty} h_\phi(t,\tau) i(\tau) d\tau = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_0\tau) i(\tau) d\tau \tag{3.14}$$

As $\Gamma(x)$ is a periodical function it can be expressed by Fourier series with coefficients c_n. If its c_n coefficients are known, the excess phase is:

$$\phi(t) = \frac{1}{q_{max}} \Big[\frac{c_0}{2} \int_{-\infty}^{t} i(\tau) d\tau + \sum_{n=1}^{\infty} c_n \int_{-\infty}^{t} i(\tau) \cos(n\omega_0\tau) d\tau \Big] \tag{3.15}$$

It is known that noise at a certain frequency, injected into an oscillator, produces spectral components at other frequencies. To demonstrate this property, $i(t)$ is considered to be a sinusoidal current source with phase $(m\omega_0 + \Delta\omega)t$, where $m\omega_0$, with $m = 1..\infty$ is a frequency multiple of the oscillator frequency and, as it has been used in this chapter, $\Delta\omega << \omega_0$. All the integrals of the terms in Eq.3.15 are negligible except when n=m. Then the excess phase noise results in the following approximate expression:

$$\phi(t) \approx \frac{I_m c_m \sin(\Delta\omega t)}{2 q_{max} \Delta\omega} \tag{3.16}$$

with the coefficients c_m used previously (with n=m).

It shows that the spectrum of $\phi(t)$ are two impulses at $\pm\Delta\omega$, despite the spectrum of the imposed signal is at frequency $m\omega_0$.

With Eq. 3.15 the spectrum of $\phi(t)$ can be obtained, but what is really important is the spectrum of the output signal as a function of $\phi(t)$. This change is called phase to voltage conversion, and it is a modulation of the excess phase that appears in the output signal.

A clarifying scheme of the process is shown in Fig.3.6, considering that the output voltage of the system is sinusoidal. If no perturbation appears the output voltage is $v_{out} = \sin(\omega_0 t)$ and no phase modulation appears. But if a current perturbation i(t) exists, then an excess phase $\phi(t)$ appears in the system (the normalized i(t)is multiplied by the ISF function at $\omega_0 t$, obtaining $\psi(t)$ and then integrated to obtain $\phi(t)$). This excess phase is added to $\omega_0 t$, the initial phase of the system.

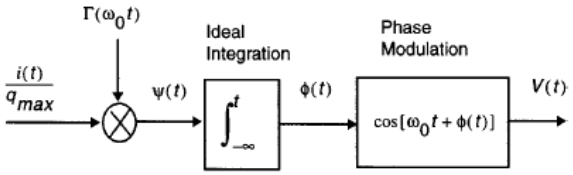


Figure 3.6: Block diagram of the process. Taken from [32].

Here appears the phase modulation because now $v_{out} = \cos(\omega_0 t + \phi(t))$. The sinusoidal function used in this example describes a typical modulation function of an oscillator response.

If the scheme of Fig.3.6 is used to obtain the voltage conversion of the excess phase of Eq.3.16, considering the sinusoidal modulation function $v_{out} = \cos(\omega_0 t + \phi(t))$, an expression of the phase noise at the output can be obtained using Eq.3.3:

$$\mathcal{L}(\Delta\omega) \approx 10log\Big(\frac{I_m^2 c_m^2}{4q_{max}^2 \Delta\omega^2 P_{carrier}}\Big) \tag{3.17}$$

This result can be extended to a white noise source:

$$\mathcal{L}(\Delta\omega) \approx 10log\Big(\frac{\overline{i_n^2}\sum_{m=0}^{\infty} c_m^2}{4q_{max}^2 \Delta\omega^2}\Big) \tag{3.18}$$

It is very interesting because it shows that the noise around the harmonics of the oscillator frequency is downconverted. This is, in fact, the spectrum of the $1/f^2$ region; and it can be rewritten using Parseval's theorem ($\sum_{n=0}^{\infty} c_m^2 = 2\Gamma_{rms}^2$) in function of Γ_{rms}^2

$$\mathcal{L}(\Delta\omega) = 10 \cdot log\Big(\frac{\overline{i_n^2}\Gamma_{rms}^2}{2q_{max}^2 \Delta\omega^2}\Big) \tag{3.19}$$

In case the current noise is flicker noise $\overline{i_{n,1/f}^2} = \overline{i_n^2}\frac{\omega_{1/f}}{\Delta\omega}$, where $\omega_{1/f}$ is the $1/f$ corner frequency, expression of phase noise is given by Eq. 3.20 where is clear the $1/f^3$ noise spectrum behaviour.

$$\mathcal{L}(\Delta\omega) = 10 \cdot log\Big(\frac{\overline{i_n^2}\Gamma_{rms}^2}{8q_{max}^2 \Delta\omega^2}\frac{\omega_{1/f}}{\Delta\omega}\Big) \tag{3.20}$$

The $1/f^3$ corner frequency is obtained making equal the Eqs.3.19 and 3.20 obtaining:

$$\Delta\omega_{1/f^3} = \omega_{1/f} \cdot \frac{c_0^2}{4\Gamma_{rms}^2} = \omega_{1/f}\Big(\frac{\Gamma_{dc}}{\Gamma_{rms}}\Big)^2 \tag{3.21}$$

In Fig.3.7 it is shown the evolution of the current noise into phase noise in the frequency domain: as an example all the bands of noise (1/f noise and white noise) are considered. Firstly all the components of noise are downconverted to the

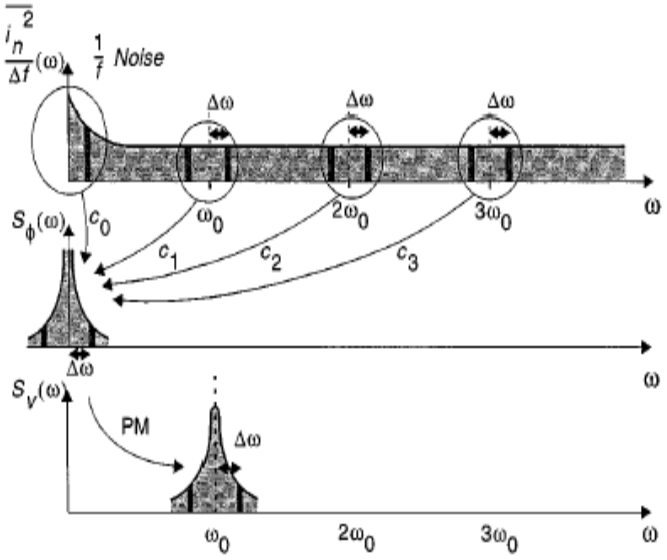


Figure 3.7: Evolution of circuit noise into phase noise. Taken from [32].

baseband as it has been explained (see Eq.3.16 and 3.18) obtaining the excess phase spectrum. Each band around ω_0 is multiplied by the correspondent c_n coefficient. Up to here it is a linear time variant system. Then, the second step is to upconvert this baseband spectrum (also called phase modulation PM). If the function is sinusoidal as in the example, with frequency ω_0, the spectrum is transferred to this frequency as it is shown in the figure. This step in a non-linear block.

The ISF function depends on the characteristics of the circuit and particulary Γ_{dc} decrease if the circuit is symmetric. So, to reduce the value of $1/f^3$ corner frequency, it is important to have as much as possible a symmetric circuit.

For example,the LC-Gm VCO differential circuit (see Fig. 3.8(a)) has a very sinusoidal function ISF and, consequently a low Γ_{dc}. But, if a complementary LC-Gm VCO circuit (Fig.3.8(b))is used, the Γ_{dc} value decreases still more -if correct values of W_n and W_p are chosen- because the symmetry is enhanced.

Another interesting approach of this model is the study of the influence of cyclostationary noise sources. It means that the model of noise sources is not really stationary, but it varies cyclically. For example, for a MOSFET of a LC oscillator, its drain current is not constant but varies periodically with time; this fact influences directly the white and flicker noise sources of the MOSFET. The LTV model proposed can accept the modification of working with a cyclostationary noise source, because this source can be described as the stationary source multiplied by a new periodic function, $\alpha(\omega_0 t)$. In the case of a cyclostatioary white noise source is the product of a white noise source and the periodic function.

$$i_n(t) = i_{n0}(t) \cdot \alpha(\omega_0 t) \tag{3.22}$$

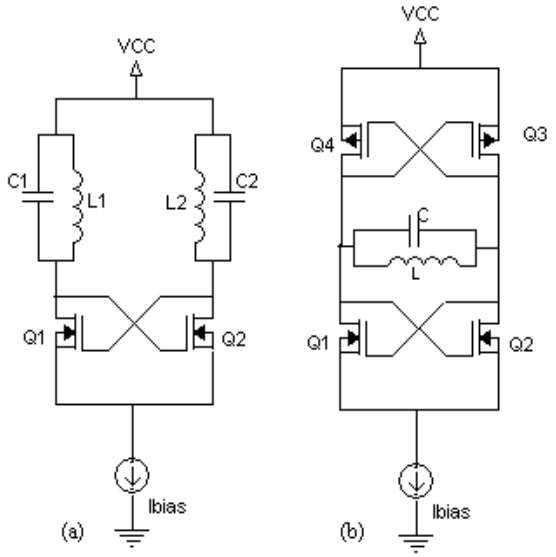


Figure 3.8: (a)Differential VCO, (b)Complementary VCO

This can be extended to the Γ function:

$$\Gamma_{eff}(x) = \Gamma(x) \cdot \alpha(x) \tag{3.23}$$

If the cyclostationary approach will be applied, all the previous discussion is valid as long as Γ_{eff} is used.

In this section the LTV model is presented and the most important results are given. It is clear that this method is better than LTI Lesson's one, specially because phase noise is described quantitatively in $1/f^2$ and $1/f^3$ regions without empirical parameters as it is shown in expressions 3.19 and 3.20. In addition, the characteristics of a good quality oscillator in terms of phase noise are briefly discussed, and the very good performance of the LC -Gm complementary VCO is pointed out.

3.4 Noise Sources

In this section the noise sources of the VCO designed in this work are studied, to obtain a qualitative expression of the total phase noise expected in this circuit [39] [50].

To visualize the different noise sources of the circuit, in Fig.3.9 it is shown the LC-VCO with the noise current sources of the MOSFETs and the noise voltage sources of the series resistance of the inductor and the varactor.

From Fig.3.9 and using the Thevenin equivalent circuit, it is obtained the four cross-coupled transistors equivalent noise power density:

$$\overline{i_{M^2_{equiv}}} = \frac{1}{4}(\overline{i^2_{n1}} + \overline{i^2_{n2}} + \overline{i^2_{p1}} + \overline{i^2_{p2}}) = \frac{1}{2}(\overline{i^2_n} + \overline{i^2_p}) \tag{3.24}$$

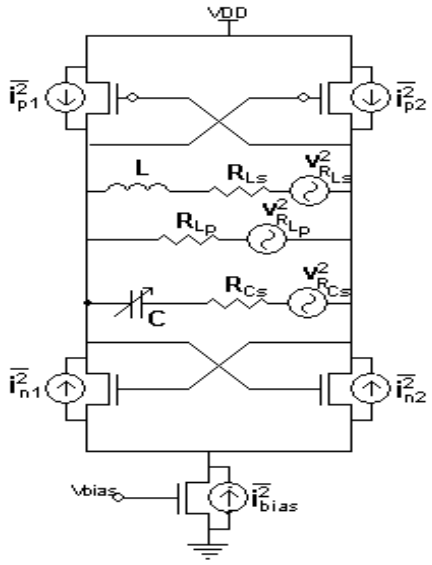


Figure 3.9: Noise sources in a complementary differential LC-VCO oscillator.

where it is considered that $\overline{i_n^2} = \overline{i_{n1}^2} = \overline{i_{n2}^2}$ and $\overline{i_p^2} = \overline{i_{p1}^2} = \overline{i_{p2}^2}$.

The thermal noise densities $\overline{i_n^2}$ and $\overline{i_p^2}$ are [35]:

$$\overline{i_n^2} = 4n_n kT\gamma \cdot g_{m,n} \tag{3.25}$$

$$\overline{i_p^2} = 4n_p kT\gamma \cdot g_{m,p} \tag{3.26}$$

where k is the Boltzmann's constant, T is the absolute temperature, $g_{m,n}$ and $g_{m,p}$ are the transconductance of the transistors nMOS and pMOS respectively,n_n and n_p are the slope factor of the nMOS and pMOS, and gamma is approximately 2/3 and 2.5 for long and short channel transistors, respectively [49].

Therefore $i^2_{M_{equiv}}$ is

$$\overline{i^2_{M_{equiv}}} = 2kT\gamma(n_n \cdot g_{m,n} + n_p \cdot g_{m,p}) \tag{3.27}$$

This noise is also named *drain current noise*.

The noise power spectral density of due to the inductor noise and the varactor noise are

$$\overline{i^2_{ind}} = 4kTg_{ind,par} \tag{3.28}$$

$$\overline{i^2_{var}} = 4kTg_{var} \tag{3.29}$$

where $g_{ind,par} = \frac{1}{R_p} + \frac{R_s}{L\omega^2}$ and $g_{var} = \frac{Cvar\omega}{Qvar}$ and usually $g_{ind,par} \ll g_{var}$

As it has been seen in Ec.2.20 $2g_m = \alpha g_{tank} \cong \alpha g_L$ then the drain current noise is $\gamma{\cdot}n{\cdot}\alpha$ times higher than the other noises generated by the inductor or the varactor (if $\gamma \approx 2.5$, $\alpha = 3$ and $n = 1.3$, $\overline{i^2_{M_{equiv}}} \approx 9$ times higher than $\overline{i^2_{ind}}$). The varactor

and inductor noises are generally neglected. Assuming this and using Eq.3.20 the phase noise can be expressed as:

$$\mathcal{L}(\Delta\omega) = 10 \cdot log\Big(\frac{kT\gamma(g_{m,n} + g_{m,p})\Gamma_{rms}^2}{2q_{max}^2 \Delta\omega^2 P_{carrier}}\Big) \tag{3.30}$$

For LC-VCOs the ISF function Γ is approximately $1/\sqrt{2}$, because the tank voltage is very sinusoidal [46]. Then the phase noise in the $1/f^2$ zone can be written as:

$$\mathcal{L}(\Delta\omega) = 10 \cdot log\Big(\frac{kT\gamma(g_{m,n} + g_{m,p})}{4q_{max}^2 \Delta\omega^2 P_{carrier}}\Big) \tag{3.31}$$

In case the current noise is flicker noise, the densities for nMOS and pMOS transistors are [51]:

$$\overline{i_{n,flicker}^2} = \frac{K_F \cdot g_{m,n}^2}{W_n L}\frac{1}{f} \tag{3.32}$$

$$\overline{i_{p,flicker}^2} = \frac{K_F \cdot g_{m,p}^2}{W_p L}\frac{1}{f} \tag{3.33}$$

with K_F a constant independent of the bias but dependent on the fabrication details.

With these equations we found that the phase noise expression in the $1/f^3$ region is:

$$\mathcal{L}(\Delta\omega) = 10 \cdot log\Big(K_F \cdot (\frac{g_{m,n}^2}{W_n L} + \frac{g_{m,p}^2}{W_p L})\frac{1}{4q_{max}^2 \Delta\omega^3 P_{carrier}}\Big) \tag{3.34}$$

3.5 Trade-offs in -Gm LC VCOs

The previous expressions using the LTV model are very useful when a very good estimation of the phase noise is needed. But to have an approximation of the circuit phase noise, it can be used the LTI model, particulary in the LC-VCOs' case. Working in the $1/f^2$ zone, the phase noise is written as in Eq. 3.9 where F is given in Eq. 3.11.

For an LC-VCO the carrier's power $P_{carrier}$ is

$$P_{carrier} = \frac{V_0^2}{2 \cdot R} \tag{3.35}$$

where V_0 is the maximum tank voltage and R is the parallel tank resistance.

With this we obtain an approximate expression of the phase noise

$$\mathcal{L}(\Delta\omega) = \frac{4kTRF}{V_0^2}\Big(\frac{\omega_0}{2Q\Delta\omega}\Big)^2 \tag{3.36}$$

which can be re-written using the g_m/I_d factor as

$$\mathcal{L}(\Delta\omega) = \frac{kT\pi^2}{32}\frac{F}{\alpha}\frac{1}{Q^2}\frac{g_m/I_d}{I_{bias}}\Big(\frac{\omega_0}{\Delta\omega}\Big)^2 \tag{3.37}$$

In Appendix A.5, Sec.A.2 is explained how to obtain the last equation.

It has been studied -using the Eq.3.37- the dependence of the VCO's phase noise with the intrinsic parameters of the inductor: Q, L and $R_{L,par}$.

- For a VCO with $L = 5nH$, $C = 6pF$, $I_{bias} = 2mA$,$V_{DD} = 3V$ and $f_0 = 910MHz$ and a $\Delta\omega = 600kHz$ [5], its phase noise is plotted using Eq.3.37(see Fig. 3.10) when varying $R_{L,par}$. As it is shown in the Eq.A.20 of Appendix A.5 the parallel resistance $R_{L,par}$ of the inductor is proportional to the quality factor Q. If increases $R_{L,par}$, increases Q, which results in a reduction of the phase noise.

- In Fig. 3.11 it is shown the behaviour of the phase noise when varying the inductance value, for a VCO with fixed $Q = 3$; $V_{DD} = 3V$, $f_0 = 910MHz$, $I_{bias} = 2mA$ and $C = 6pF$. As $Q = R_{L,par}/wL$ (refer to Eq.A.20), if Q is fixed [6]and L is raised then $R_{L,par}$ must increase. This leads to the previous discussion about the consequences of rise $R_{L,par}$ An increment in L in the mentioned conditions leads to a lower phase noise.

- Now it is considered a similar situation with identical parameters' values, but now a fixed inductor L is used and the Q of the inductor varies. The phase noise decreases as Q is raised. A plot of the phase noise as a function of Q is shown in Fig.3.12.

A general conclusion from these results is that having an inductor with a high Q improves the phase noise. If the inductor is off-chip it can be achieved easily, but it is not the case of the monolithic inductors. Also, it is true that increasing the inductor value decreases the phase noise, but this only happens when the Q is fixed; this is difficult to be done because generally increasing the size of the inductor leads to high losses, and then lower Q. These facts will be seen in Chapter 4.

The previous approach only considers the minimization of the phase noise in a VCO design. A more realistic approach is to consider not only the phase noise minimization but also the imposed specifications of the power consumption. Then, it is possible to define a figure of merit *FOM* which takes into account the power consumption P_d and the phase noise in an offset band $\Delta\omega$ from ω_0 [52]. This figure of merit has to be minimized in order to obtain high performance (low phase noise and low power consumption). It is defined as:

$$FOM = \mathcal{L}(\Delta\omega)P_d\Big(\frac{\Delta\omega}{\omega_0}\Big)^2 \tag{3.38}$$

[5]The phase noise at this $\Delta\omega$ value is usually specified in the published works and in the IEEE802.15.4 power specifications are given at this frequency

[6]It is not a typical case

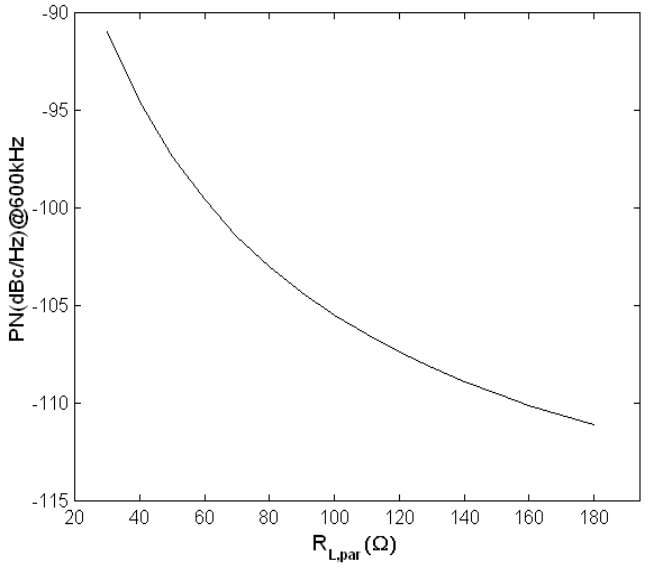


Figure 3.10: Phase noise versus parallel tank resistance @ 600kHz from the carrier, considering a constant L.

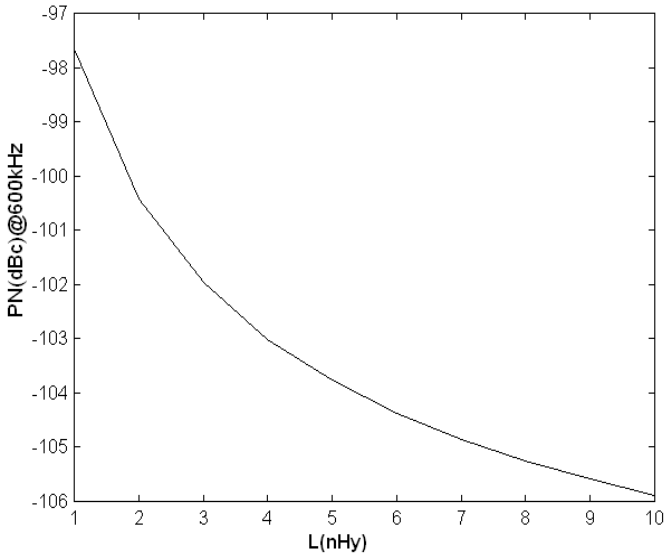


Figure 3.11: Phase noise versus Inductance @ 600kHz from the carrier, considering a constant Q.

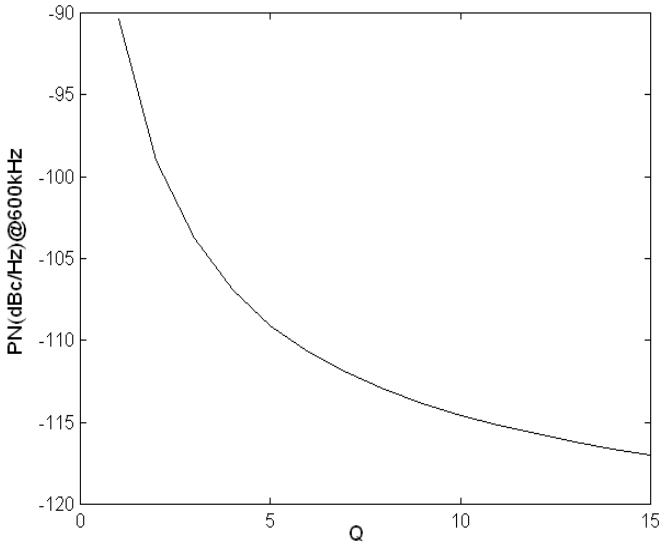


Figure 3.12: Phase noise versus inductor quality factor Q @ 600kHz from the carrier, with a fixed L.

where $P_d = I_{bias}V_{DD}$.

Substituting Eq. 3.36 into Eq. 3.38 we obtain:

$$FOM = \frac{kT\pi^2}{8}\frac{F}{\alpha}\frac{1}{Q^2}(g_m/I_d)V_{DD} = K_1 \cdot \frac{F}{\alpha}\frac{1}{Q^2}(g_m/I_d)V_{DD} \tag{3.39}$$

If the supply voltage, γ and the Q factor are constant (which is not always the case), to minimize FOM the coefficient g_m/I_d has to be as low as possible.

Another way of studding FOM is considering that the coefficient g_m/I_d, F and Q are functions of the equivalent resistance R of the tank. Therefore considering that the quality factor of the tank Q is almost equal to the quality factor of the inductor Q_L, and the tank resistance R can be approximated to the equivalent parallel resistance of the inductor $R_{L,par}$, the FOM is:

$$FOM = \frac{\frac{V_{DD}}{\alpha} \cdot \left(2 + \frac{8\gamma RL,parI_{bias}}{\pi V_0} + \gamma\frac{8}{9}g_{mbias}R_{L,par}\right)\left(\alpha/(R_{L,par}I_d)\right)}{\left(\frac{R_{L,par}}{\omega_0 L} + \sqrt{\left(\frac{R_{L,par}}{\omega_0 L}\right)^2 - 4}\right)^2} \tag{3.40}$$

Considering that (see Appendix A.5, Sec.A.3)

$$R_{L,par} = \frac{(Q_L^2 + 1)}{Q_L} \cdot \omega_0 L \tag{3.41}$$

the Eq.3.39 can be re-written as

$$FM = \frac{2V_{DD}\left(2 + \left(\frac{8\gamma I_{bias}}{\pi V_0} + \gamma\frac{8}{9}g_{mbias}\right)\cdot\frac{(Q_L^2+1)}{Q_L}\cdot\omega_0 L\right)}{\omega_0 L Q_L(Q_L^2+1)} \tag{3.42}$$

Considering only variations of the tank parameters, in Fig. 3.5 it is shown the FOM as a function of R_s (series resistance of the inductor), Q and $R_{L,par}$ for an arbitrary set of parameters: $V_{DD} = 3V$, L=5nHy, $f_0 = 910MHz$, $I_d = 9mA$, $g_{mbias} = 50mS$, $\alpha = 3$ and with Q varying between 1 and 7. According to the figures, to obtain a minimum FOM the quality factor of the tank or equivalently the inductance's parallel resistance have to be as high as possible, what is consistent with decreasing as much as possible the inductance series resistance of the tank.

If only the variation of the g_m/I_D is considered (with $Q = 3$, $L = 5nHy$ and $f_0 = 910MHz$) the FOM has the behaviour shown in Fig.3.14. In this figure it is clear that minimizing the FM being equivalent to work in strong inversion.

However, in this work it is shown that a good compromise between phase noise and power consumption is achieved when working in moderate inversion.

3.6 Phase Noise results obtained from simulation

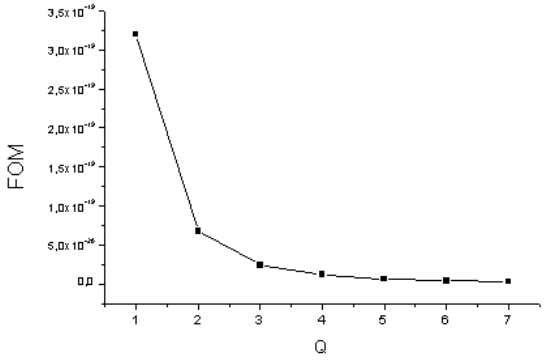
In this section the results of phase noise calculated in Matlab and simulated in RF Spectre of Cadence are shown.

A Matlab routine has been implemented to calculate the phase noise for a set of differential cross-coupled VCOs in $0.35\mu m$ technology with the following characteristics:

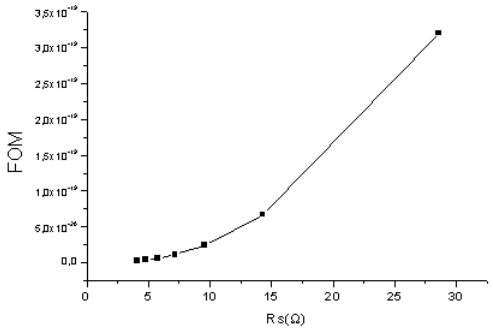
- $f_0 = 910MHz$
- $g_m/I_D = (5..17)[S\cdot A]^{-1}$
- $L = (3..7)nHy$
- $\alpha = 3$
- $C_{load} = 0.6pF$

In Fig.3.15 it is plotted the phase noise versus the inductance of the designed VCOs @600kHz from the carrier with the LTI model. It shows that increasing the g_m/I_D of the cross-coupled transistors or increasing the inductor value (considering that the Q varies accordingly) the phase noise of these VCOs is deteriorated. When the g_m/I_D rise from $5(V)^{-1}$ to $17(V)^{-1}$ the phase noise increases almost 10dBc/Hz. The reduction of this parameter due to L is not so important, being approximately 0.7dBc/Hz.

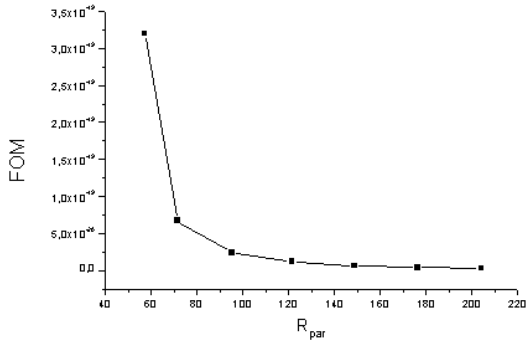
The VCO finally designed has a theoretic value of $g_m/I_D = 11$ and $L = 5nHy$. For this values the phase noise between 16kHz and 3.2MHz is calculated using two methods: (1) the LTI method with the Eqs. 3.11 and 3.37 and (2) the



(a) FOM versus Q



(b) FOM versus R_s



(c) FOM versus R_{par}

Figure 3.13: Figure of Merit (defined in 3.38) versus Q, R_s and R_{par}.

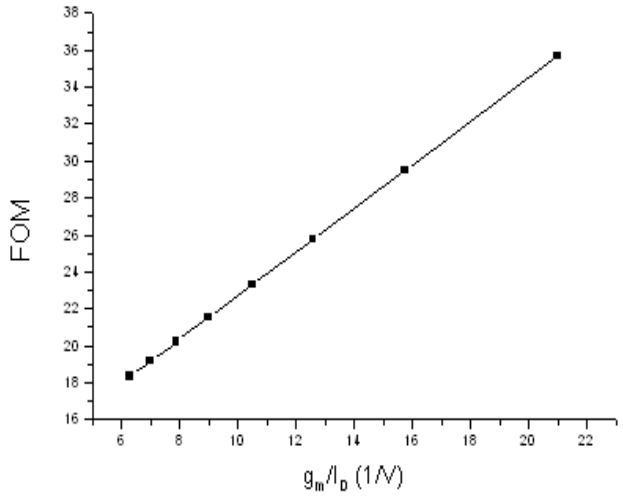


Figure 3.14: Figure of Merit versus g_m/I_D.

LTV method with Eq.3.31 and that $q_{max} = V_{max}C_{total}$ (with V_{max} the maximum voltage of each output node of the tank and C_{total} the total capacitance of the tank). Both results are plotted in 3.6 (the initial value has been chosen long enough from the $1/f^3$ zone). Both curves are very similar but there is a difference in the phase noise value. At 600kHz from the carrier the phase noise value with the LTI model is approximately -108dBc/Hz and with the LTV model is -119.7dBc/Hz. The difference can be explained with the noise factor F of the LTI model as it is an empirical value and in this work it has been obtained by an approximated expression.

With the Spectre RF tool of Cadence, the phase noise of this circuit has been simulated and the results are shown in Fig.3.17. The phase noise value at 600kHz from the carrier is -121dBc/Hz. There is a great agreement between the phase noise calculated with the LTV model as it was expected.

3.7 Conclusions

In this chapter it has been studied the two phase noise theories most utilized to model this parameter: the linear time invariant and the linear time variant. It has been shown that the last one is the most accurate theory to find the phase noise of an oscillator and that it is possible to calculate it easily for a LC VCO. It has been shown that good agreement between the simulations and the matlab analysis. It also has been shown that low values of phase noise can be achieved with the LC VCO working in moderate inversion.

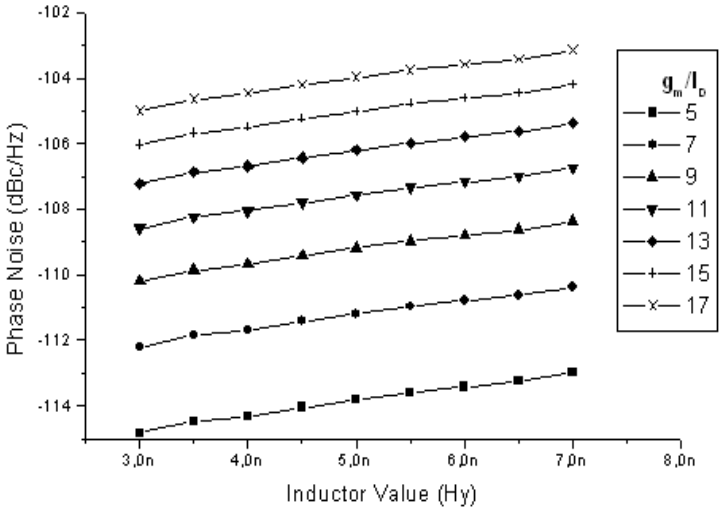


Figure 3.15: Phase Noise vs. Inductance @600kHz offset from carrier for several gm/Id.

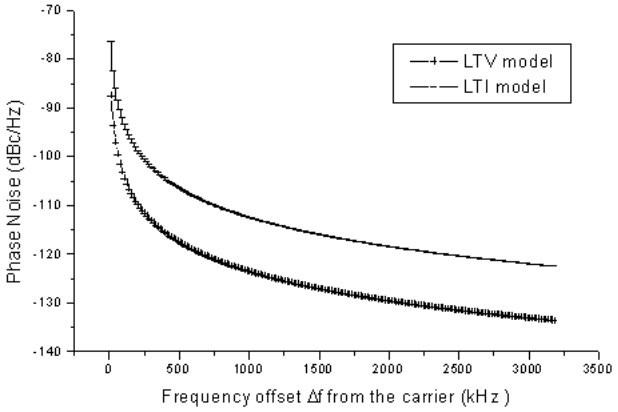


Figure 3.16: Phase noise versus the offset frequency calculated with Matlab for the designed VCO, for the LTI and LTV models.

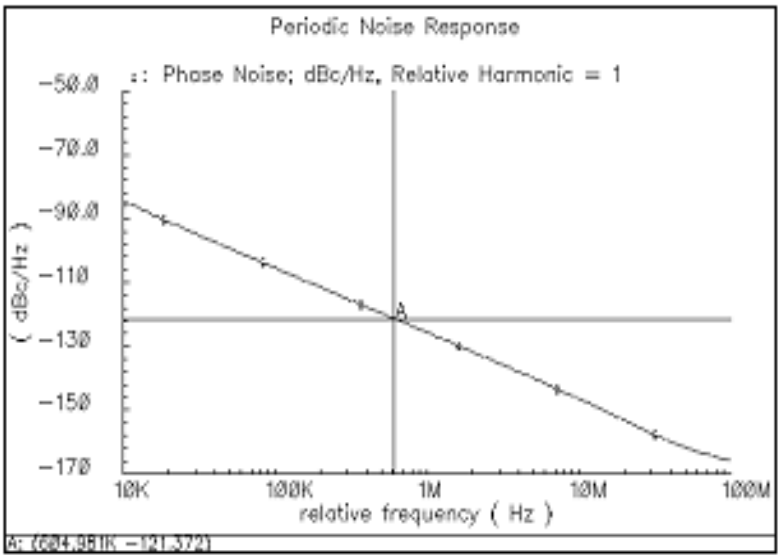


Figure 3.17: Simulated Phase Noise in Cadence.

Chapter 4
Inductors Design

4.1 Introduction

The study of on-chip inductors has increased recently due to the possibility of obtain, in standard CMOS technologies, an inductor design with acceptable performance.

The most important characteristics of a monolithic inductor are its equivalent inductance L value, its quality factor Q (which depends on the resistance of the inductor), its self resonant frequency SRF and its area. Other parameters are dependant of the mentioned characteristics, for example the series and parallel resistances. The working frequency of the inductor f_0 strongly determines some of these parameters.

The working frequency and the inductor geometry determines directly the inductance value [22].

The quality factor measures the inductor's ideality and it is a function of the magnetic and electric losses of the inductor.

In this chapter it will be described the different inductor types, its modelling (physical basis and several actual models), its losses, and the final design used.

4.2 Inductor Types

As it has been mentioned, one of the most important characteristics of an inductor is the quality factor Q. It is generally defined as:

$$Q = 2\pi \frac{maximum\, energy\, stored}{energy\, disipated\, per\, cycle} \tag{4.1}$$

This factor is proportional to the metal conductance and to the distance between the inductor and the substrate because increasing those factors makes a considerable lessening in the losses. This is the principal reason why the on-chip inductors are designed in the uppermost metal available in the process. Also, the technologies normally provide the option to fabricate this metal thicker than the other metal layers which reduces the metal resistance.

There is a wide variety of inductor forms, including transformers and baluns. The most common shapes are the square, the polygon and the spiral. Just to give an idea of the variety we list and depict in Fig.4.1 the typical ones [53]:

1. square spiral(Fig.4.1(a)),
2. tapered square spiral(Fig.4.1(b)),

3. polygon spiral(Fig.4.1(c)),
4. polygon ring,
5. polygon symmetric spiral(Fig.4.1(d)),
6. square symmetric spiral(Fig.4.1(e)),
7. multi metal series connected square spiral(Fig.4.1(f)),
8. multi metal shunt connected (stacked) square spiral
9. planar transformer(Fig.4.1(g)),
10. symmetric balun.

The polygon spirals could have six, eight or more sides or can also be circular. The ring is a circular spiral with only one turn. The multi-metal structures are formed by two or more metals, as Fig.4.1(f) attempts to show. The series multi-metal spiral are various spirals each one in a different metal interconnected in one point and put one over the other and the shunt spirals is the same structure but they are interconnected in two points. The transformer is a structure of two spirals interleaved, and the balun has the same structure of a transformer.

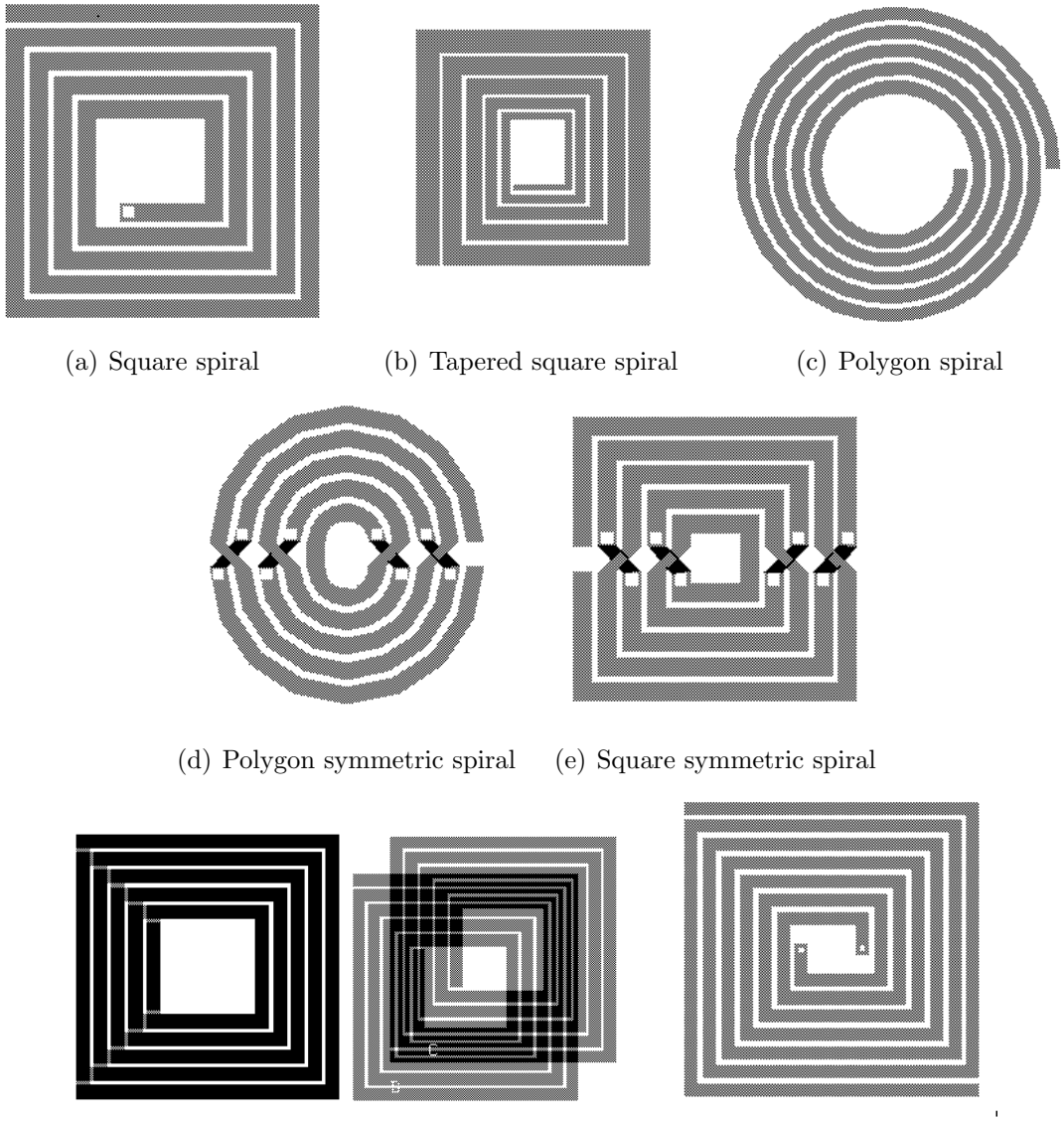
The election of the shape depends on the L value needed and the characteristics of the mask generation systems. If a large L has to be implemented, a multi layer inductor would be used. It is convenient to do circular structures because for the same inductor value they have less series resistance. The polygonal and square ones have more resistance that the spiral ones but are implemented since most mask systems only admit wires with 135 or 90 degrees angles. In this work a square inductance has been used because: it was the first time we work with on-chip inductors and there exist much more previous works which studied them [44][54][55] and also because its layout is easier to implement.

4.3 Modelling

During the last years a wide variety of models have been developed having different levels of complexity. There are some (see [1][56]) that model the inductor with discrete parameters and have a simple set of equations and constants (which depend on the geometry) that describe L, Q, and the series resistance R_s. Others [54] are more complex and use distributed parameters to describe the inductor behaviour.

The VCO's working characteristics rely strongly on the inductor features, specially the L, Q and R_s, and they must be included in the VCO design routine. Owing to this, it is necessary to have good analytical inductor models, which will be discussed here.

These characteristics depend fundamentally on the working frequency. In this case the parameters' value obtained is valid only in a narrow bandwidth around f_0



(a) Square spiral (b) Tapered square spiral (c) Polygon spiral

(d) Polygon symmetric spiral (e) Square symmetric spiral

(f) Multi-metal series connected square spiral (g) Planar transformer

Figure 4.1: Types of inductors' layout.

(as it will be shown later R_s depends on the frequency, and also Q). In this case it is specifically used a two-port π type model shown in Fig. 4.2.

In this figure are shown the lumped elements' model of the inductor: the series inductance L_s, the series resistance of the inductor R_s, the parallel capacitance between both ports C_s. Between each port and the silicon there is the capacitance C_{ox}. In series with C_{ox} is the parallel of the resistance R_{si} and the capacitance C_{si} existent between the upper and the lower sides of the silicon bulk. In Fig.4.3 it is shown the cross-section view of an inductor and its parasitics [56]. In Sec.4.4 it will be given a physical explanation of the resistive losses of the inductor.

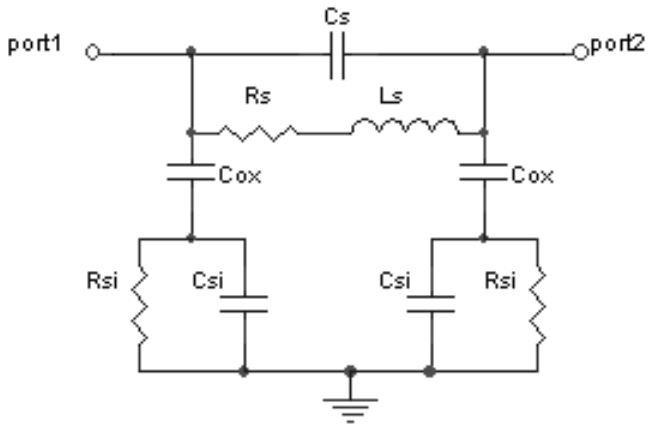


Figure 4.2: Lumped inductor model based on a π net.

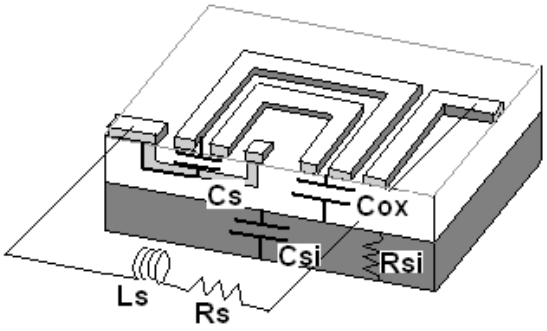


Figure 4.3: Monolithic inductor cross-section view.

Some models use the six elements of the model and others simplify them working without C_{Si}, and also without R_{Si} [23] -this case is acceptable if the resistance of the substrate right enough to be neglected-.

The Q expression, using these parameters, is [56]:

$$Q = \frac{\omega L_s}{R_s} \frac{R_p}{R_p + \left((\omega L_s/R_s)^2 + 1\right) \cdot R_s} \left(1 + \frac{R_s^2 C_p}{L_s} - \omega^2 L_s C_p\right) \tag{4.2}$$

where

$$R_p = \frac{1}{\omega^2 C_{ox}^2 R_{si}} + \frac{R_{si}(C_{ox} + C_{si})^2}{C_{ox}^2} \tag{4.3}$$

and

$$C_p = Cox \frac{1 + \omega^2 (C_{ox} + Csi) C_{si} R_{si}^2}{1 + \omega^2 (C_{ox} + Csi)^2 R_{si}^2} \tag{4.4}$$

A simplified equation can be used to obtain a rough value of Q:

$$Q = \frac{\omega L_s}{R_s} \tag{4.5}$$

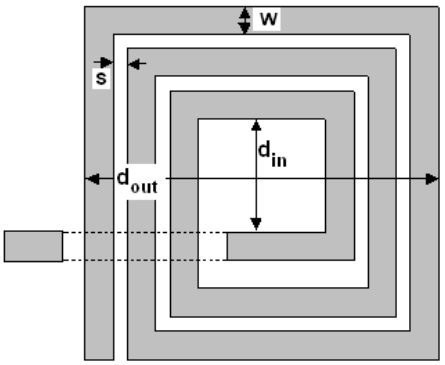


Figure 4.4: Inductor physical parameters: s is the space between wires, w is their width, d_{out} and d_{in} are the output and input diameter respectively.

In Fig.4.4 it is shown the principal physical parameters involved in the expressions of the lumped elements: the wire width w, the spaces between wires **s** and the output and input diameters d_{out} and d_{in}.

The expressions that calculate the lumped elements vary considerably from one model to the other. Here are resumed two of the most important ones.

Yue's model [57][58]

This work gives expressions of L, R_s, C_s, C_{ox}, R_{si}, C_{si} in function of the inductor's geometry. In case of the L value, it is obtained using the Greenhouse algorithm [59]. The other elements' expressions, working with a four-metal technology, are:

$$R_s = \frac{\rho.l}{w.\delta.(1 - e^{\frac{-t}{\delta}})} \tag{4.6}$$

$$C_s = n.w^2(\frac{\epsilon_{ox}}{t_{oxM4-M3}}) \tag{4.7}$$

$$C_{ox} = \frac{1}{2}.l.w(\frac{\epsilon_{ox}}{t_{ox}}) \tag{4.8}$$

$$C_{si} = \frac{1}{2}.l.w.C_{sub} \tag{4.9}$$

$$R_{si} = \frac{2}{l.w.G_{sub}} \tag{4.10}$$

where l is the overall length of the spiral, w is the track width, δ is the metal skin depth, t is the metal thickness, N is the number of turns, *n=N-1* is the number of crossovers between spiral and the center port, $t_{oxM3-M4}$ is the oxide thickness between spiral metal and center port metal, t_{ox} is the oxide thickness between spiral metal and substrate, C_{sub} is the substrate capacitance per unit area, G_{sub} is the substrate conductance per unit area.

Mohan's inductance expressions [1]

In [1] three expressions of inductance values are presented: the first based on the expression of Wheeler [60], the second obtained from the Current Sheet

Approximation and the last one based on a data fitting technique. As it is shown that the three ones are almost equivalent, only the former one is presented here:

$$L_s = K_1 \mu_O \frac{N^2.d_{avg}}{1 + K_2.\xi} \tag{4.11}$$

where ξ, the fill ratio, is defined as:

$$\xi = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \tag{4.12}$$

d_{out} is the output diameter of the spiral, d_{in} is the input diameter and $d_{avg} = 0.5(d_{out} + d_{in})$. The constants K_1 and K_2 depends on the geometry of the inductor (three geometries are defined in [1]: square, hexagonal and orthogonal). Their values are given in the following table:

Geometry	**K1**	**K2**
square	2.34	2.75
hexagonal	2.33	3.82
orthogonal	2.25	3.55

Table 4.1: Values of the constants K_1 and K_2 (defined in [1])

In [1] there is a comparison between the three inductance expressions, the results obtained from a Field Solver and the measured values. There is a good matching between all of them.

The values of R_s, C_s, C_{Si}, R_{Si} and C_{ox} can be calculated as proposed in the Yue's model.

Other models [55][54] take each segment of the spiral and model it as a two-port network consisting of lumped elements, similar as what has been seen previously.

4.4 Inductor losses

The inductor losses are studied and quantified because of its influence in the quality factor Q and the phase noise $\mathcal{L}$ of the VCO: Q is inversely proportional and as has been seen in 3.5 the $\mathcal{L}$ is directly proportional to the losses.

In this section an approach to the inductor losses subject is presented, based on the work of Craninckx and Steyaert [15], where these are divided into two categories: (1) Metal Losses and (2) Substrate Losses.

4.4.1 Metal Losses

The inductor has a intrinsic DC resistance $R_{s,DC}$ associated, whose value is equal to the resistivity ρ of the metal multiplied by the length of the winding and divided by its section. Depending on the metal used is the $R_{s,DC}$ obtained; the best situation is to have a low-resistivity metal, as Cooper [22], but in CMOS standard

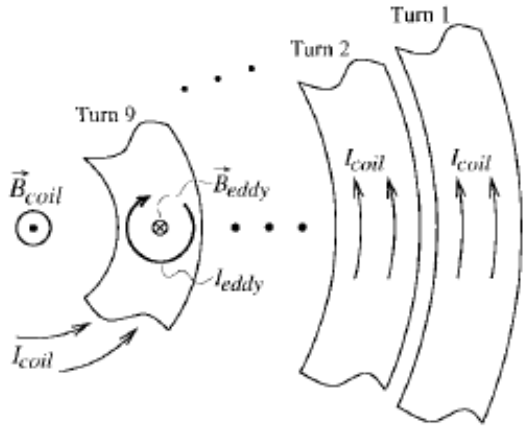


Figure 4.5: Eddy currents
Spirals' eddy currents (taken from [15])

technology the metal used is Aluminium, despite $\rho_{Al} = 2.75 \times 10^{-8}$ is higher than $\rho_{Cu} = 1.69 \times 10^{-8}$.

Also when working at high frequencies, the skin-effect begins to matter. This effect makes the resistance to increase dramatically and increasing the width of the inductance do not improve the Q value but raises the capacitances C_s. This effect is modelled in Eq.4.6 as the exponential term in the denominator.

Another effect than can be more important that the skin effect is the generation of eddy currents in the spirals (see Fig.4.5). The currents flowing through the winding generate a $\overrightarrow{B_{coil}}$ field perpendicular to the inductor, which flows not only through the middle hollow but through the metal turns, and its magnitude decrease with the distance measured from the center of the inductor. This field induces eddy currents in the inner coils, generated by an opposite field $\overrightarrow{B_{eddy}}$ -by the law or Faraday and Lenz-. But the value of these currents is higher in the inner turns, and can be larger than the current of the coil. To see this effect clearly, in Fig.4.6 it is shown the series resistance in function of the frequency for each of the turns of a 9-turn inductor (the ninth turn is the inner one).

As it is difficult to model analytically this effect it has to be prevented in order to model the losses correctly. To prevent it, the inductors have to be designed with a large center hole.

4.4.2 Substrate Losses

The $\overrightarrow{B_{coil}}$ field not only induces currents in the winding but also in the substrate of the chip as shown in Fig.4.7. These currents flow parallel to the inductor and in a sense contrary to the coil current -because of the law of Faraday and Lenz-. If the substrate is a high resistive one it is possible to neglect these losses [23] but this cannot be done in CMOS standard processes because the substrate is a semiconductor, thus these losses lead to a lower Q factor. These losses are represented

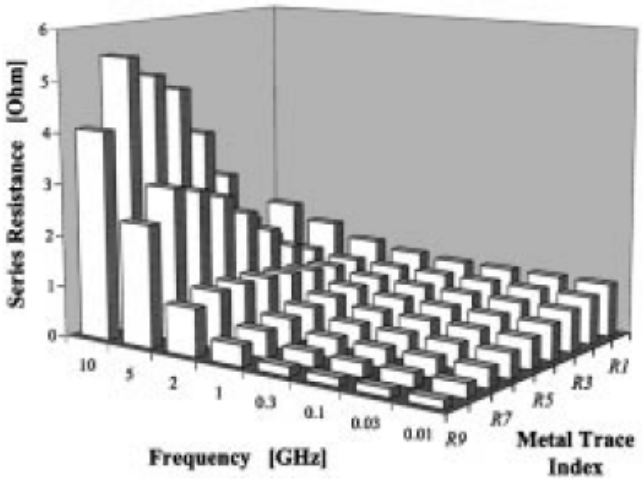


Figure 4.6: Generation of substrate current on planar inductors (taken from [15]).

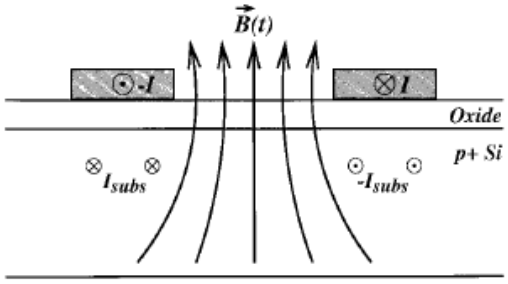


Figure 4.7: Individual series resistance per metal trace[15].

in the models in the resistance R_{si}, as in the Eq- 4.10.

4.5 VCO Phase noise and Inductor

As it has been discussed in Chapter 3 the characteristics of the inductor (equivalent parallel resistance $R_{L,par}$, Q and L) are substantial to determine the VCO's phase noise. It means that the inductor design has to be carefully studied in order to obtain good phase noise values.

Firstly a deduction of the expression of the equivalent parallel resistance of the inductor will be done, considering the model of Fig. 4.2 and a differential VCO architecture (see Fig.2.5).

Supposing that the VCO circuit is completely symmetric -no mismatch exist between each half part-, the node of union of both inductors (port2 in Fig. 4.2)has a constant value. Then, if we study the circuit with a small-signal model, this node is a *virtual ground*, hence the capacitor C_{ox}, the resistor R_{si} and capacitor C_{si} of port2 are short-circuited. Then the series of $R_{si}\|C_{si}$ and C_{ox} of port1 are in parallel

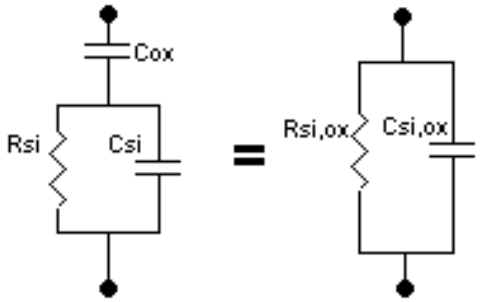


Figure 4.8: Conversion of the configuration of R_{si},C_{si} and C_{ox} into a scheme of a capacitor $C_{si,ox}$ and a resistance $R_{si,ox}$ in parallel.

with the inductor.

This series of elements can be modified to be seen as a parallel of a resistance $R_{si,ox}$ and a capacitor $C_{si,ox}$ as it is depicted in Fig.4.8. For typical values of R_{si}, C_{si} and C_{ox} the equivalent resistance $R_{si,ox}$ is higher than R_{si} (the deduction of $R_{si,ox}$ and $C_{si,ox}$ is in Sec.A.4 of App.A.5).

Moreover, the series resistance of the inductor R_s can be transformed into a parallel resistance by the following equation (see Sec.A.3):

$$R_{s,par} = (Q^2 + 1) \cdot R_s \cong Q^2 \cdot R_s \cong \frac{R_s}{(L\omega_0)^2} \tag{4.13}$$

Therefore, the equivalent parallel resistance of the inductor is:

$$R_{L,par} = R_{si,ox} \| \frac{R_s}{(L\omega)^2} \tag{4.14}$$

For the CMOS standard technologies typically used, $R_{si,ox} \gg R_{s,par}$, and then $R_{L,par} \cong R_{s_{,par}}$.

These results are used in Sec.3.5 to obtain the phase noise $\mathcal{L}$ as a function of the series resistance of the inductor (refer to Eq.3.37).

From what has been observed in this chapter, Q_L, L or $R_{L,par}$ strongly depend on the features of the technology used: the metal layers' number, the inductor's metal width and the resistance of the substrate. This dependance between the inductor characteristics and the technology result in a direct dependance between the phase noise of the VCO and the technology.

4.6 Simulation tools

The characteristics of an inductor can be obtained not only by the models previously mentioned but also utilizing specialized software for this matter.

In this work two tools have been used: the freeware ASITIC [53] and the *RF*

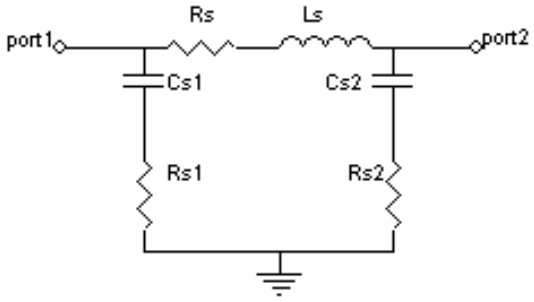


Figure 4.9: π-model used in the ASITIC program.

Spectre Inductor Modeler of Cadence [61].

The Inductor Modeler of *RF Spectre* is an extractor based on electromagnetic calculations. Given the geometry of the inductor it extracts the parameters of the lumped element model. The inputs are, among others, f_0, d_{OUT},w, s, number of turns N and inductor type. The outputs are R_s (the AC resistance including the skin-depth effect), L_s, Q (the quality factor at the working frequency), Q_{max} (maximum quality factor of the inductor within the 10 MHz to 20 GHz frequency range),f_{Qmax} (frequency at which Qmax occurs). [7].

The Analysis and Simulation of Inductors and Transformers for ICs (ASITIC) program [53] [24] is also based on electrostatic and magnetostatic calculations, a simplified approach of the electromagnetic analysis. The simplification is based in the fact that at the frequencies of interest the electromagnetic equations are replaced by static equations (the good agreement between this program's simulations and measurements has been checked up to 5GHz). This program uses the π-model of Fig.4.9.

The ASITIC and the Inductor Modeler of Cadence are used when the designer has an approximate idea of the physical parameters of the inductor and it is needed to corroborate the electrical characteristics of the inductor. For example, having the width and space of turns, its number, external diameter and the metal where the inductor will be fabricated, it is possible to obtain its π model parameters: L_s, R_s, its capacitances and Q. An iteration process can be done to adjust the physical parameters until the desired inductor characteristics are met.

In the case of ASITIC it is also possible to obtain an optimum inductor design using some physical characteristics previously fixed, as the space of turns or the maximum inductor area available (translated to the maximum output diameter),the inductance value and the minimum Q needed.

[7]This solver employs an algorithm to generate macromodels for the spiral components. Electrostatic and magneto-static EM solvers are called separately to extract the capacitive and inductive parameters of the structure. It considers skin-depth effects, and models the substrate effect by treating the lossy layers as lossy conductor planes. The meshes for inductive and capacitive extractions are inter-correlated. Because of the conductor and substrate loss, the extracted parameters are formulated as RLCG matrixes (lumped element model)[61]

Some of the advantages of ASITIC are the optimization feature and its speed. On the other hand, as it does not include the effect of substrate in the calculus of inductance; for CMOS technologies it underestimates the substrate losses of the inductor. In the case of RF Spectre modeler, it uses Fasthenry (a program for the efficient extraction of inductances and resistances of complex 3-D geometries of conductors [62]), which includes the lossy substrate effect.

In this work, there has been used firstly the ASITIC program to obtain an optimum design limiting the area; and secondly, to re-check the results from ASITIC, the RF Spectre Modeler. In the following section a deep insight of the design will be given.

Exampes of others programs which can be utilized for inductor simulation instead of the previously mentioned are: (1) Sonnet (www.sonnetusa.com); (2) SISP -for Windows- (www.elab.ntua.gr/sisp/); (3)HFSS (www.ansoft.com/products/hf/hfss) among others.

4.7 Inductor Design

The inductor design is bound to the VCO design methodology of Fig.2.8 because in the VCO's design flow, the resistance $R_{L,par}$, the capacitance $C_s \| C_{si,ox}$, Q and L values are used to obtain the phase noise, the power consumption and the transistor sizes, among other VCO's features. This is why the inductor design methodology proposed here has two stages. Firstly, using an algorithm which implements the mentioned inductor models, rough values of the inductor characteristics are obtained and these can be used in the principal routine of the VCO. Secondly, when the final VCO design is chosen, there is an approximate estimation of the L and Q values. With these values, the working frequency and specifications of geometrical constrains (spacing between tracks and maximum inductor area), the ASITIC feature called *optarea* can be used to obtain the physical dimensions of the optimum inductor that obeys these specifications. Later on, using ASITIC or Cadence RF Spectre Inductors' Modeler, an accurate π-model of the designed inductor is calculated, model that is finally re-inserted in the VCO's design routine to refine the values of the VCO's physical parameters.

The VCO finally designed is simulated in Cadence and in this instance it is used the Cadence RF Spectre Inductors' Modeler. It enables to characterize the inductor designed, being possible to use the model of this inductor in all the stages of the design in Cadence (schematic, layout and extraction).

The ASITIC program and the RF Spectre Inductors' Modeler need the physical characteristics of the technology, particularly distances between metals, the metal width, the resistivity and the dielectric constant. In our work we use a $0.35\mu m$ CMOS technology, which has one poly and 4 metals (the inductors were designed in the top metal layer for the reasons mentioned in Sec.4.4). The technology process used does not have a very thick top metal, preventing us from improving the Q factor of the inductor. In Fig.4.10 is a scheme of the layers of this technology and in Fig. 4.11 it is shown graphically data that needs both software tools.

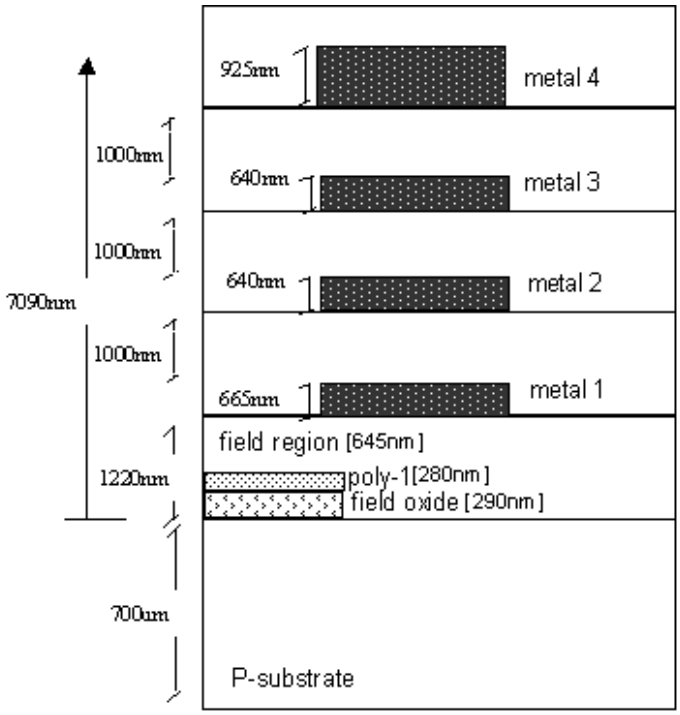


Figure 4.10: Scheme of the technology's layers

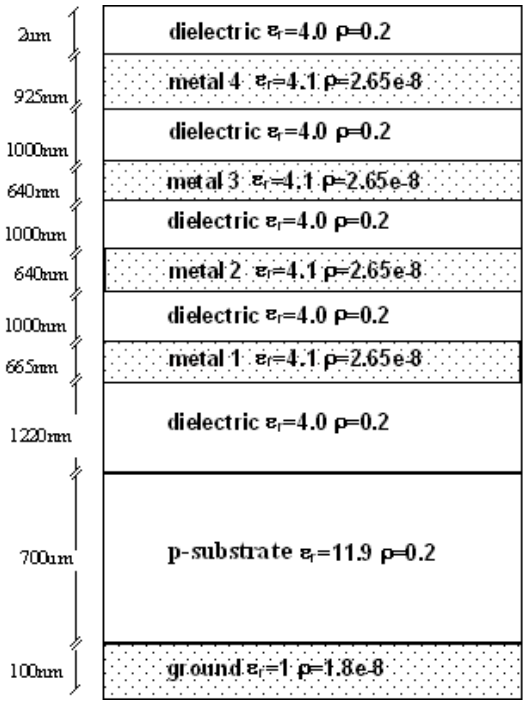


Figure 4.11: Technology data given to the RF inductor's modeler

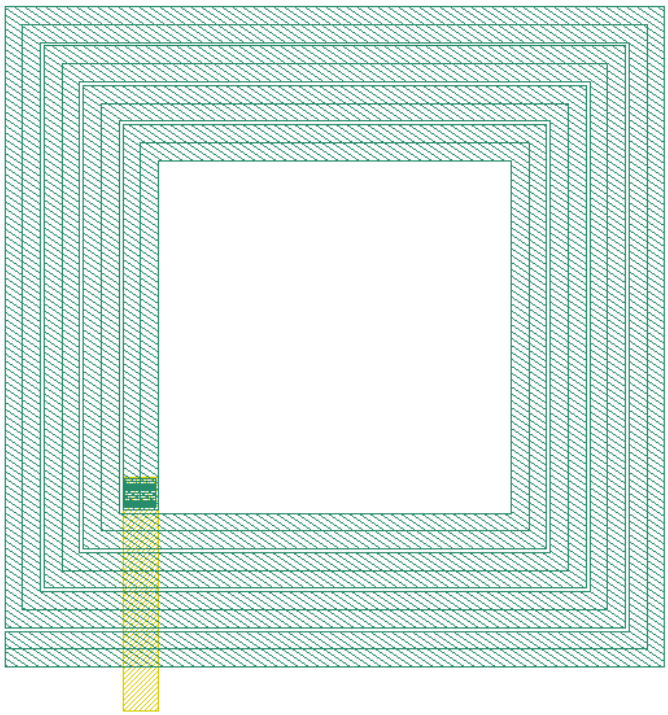


Figure 4.12: Final layout design of the inductor

The function *optarea* of ASITIC has as inputs the geometry, the working frequency, the inductor metal, a fixed spacing, the L value and its accuracy, a range of width track, a range of output diameter and a minimum Q. Its output are the trace width w, the output diameter d_{out} and the number of turns. The resulting inductor , for $L = 5nH$, $f_0 = 915MHz$, $s = 1.5\mu m$ and $Q_{min} \approx 3$ are given in Table 4.2 (see Fig.4.12):

Geometry	square
Metal	top metal
Number of turns	4
w(μ m)	14
s(μ m)	1.5
d_{out}**(μ m)**	260

Table 4.2: Geometric parameters obtained with the function *optarea* of ASITIC

With these inductor dimensions, it has been obtained the electrical parameters using various methods.

Using the equations of Yue's Model and the expression of Mohan's inductance

we have calculated L,R_s, C_s,C_{ox} and Q. The results are shown in Table 4.3.

L(nH)	5.118
Rs(Ω)	9.33
Cs(fF)	27
Cox(fF)	122
Q	3.1

Table 4.3: Parameters of the inductor calculated using the Yue's Model and the Mohan expressions.

With the ASITIC program we obtain the pi-model of this inductor whose values are shown in Table 4.4.

Q	$2.926_{differentialconection}$
	$2.929_{port2short-circuited}$
	$2.971_{port1short-circuited}$
L(nH)	5.105
Rs(Ω)	9.68
Cs1(fF)	154.7
Rs1(Ω)	12.59
Cs2(fF)	152.8
Rs2(Ω)	6.678
SRF(GHz)	5.668

Table 4.4: Parameters of the inductor calculated using ASITIC.

And finally with the RF Spectre Inductors' Modeler the data presented in Table 4.5 models the inductor designed.

L(nH)	5.014
Rs(Ω)	6.89
Q	3.9
Qmax	5.94
frequency of Qmax (GHz)	1.93
SRF(GHz)	3.87

Table 4.5: Parameters of the inductor calculated using RF Spectre Inductors' Modeler.

If the three results are compared it can be seen that the outputs of the ASITIC program are very similar to the ones obtained by using the equations of Yue and Mohan 's models. They have very similar values of Q, R_s, L, and C_{si} (for the

equivalence between the π model of ASITIC and model used in Yue's equations compare the Figs.4.2 and 4.9).

In the results obtained by Cadence tool, the inductance value is very similar to the other two models but there is a slight difference in the quality factor and in the series resistance. The difference is about 20% approximately in the Q factor an 25% in the series resistance factor.

It was expected that the Q factor obtained with the Cadence tool might be lower because it considers the losses of the substrate. But the documentation of that tool has not sufficient information to understand why this happens. Therefore we decide to use the data of the ASITIC program because it was clearly documented and we know clearly which are its problems.

Chapter 5
Varactor Design

5.1 Introduction

Towards the application of CMOS technologies in radio-frequencies, not only the attention has been put in the monolithic inductor but also in improving the varactors. They are capacitors which can tune its capacitance value by means of a bias voltage. They are not passive devices as they are made using active devices such as diodes or transistors.

In most cases the quality factor of the varactor Q_{var} is high enough compared to the quality factor of the inductor to neglect the non-idealities. Anyway these devices have to be studied in order to check this assumption. In the last years it has been an improvement in the varactor topologies to increase the Q_{var} as it is shown in [63][14].

The aim of this chapter is to show the most common varactors' topologies, to study more deeply the varactor topology utilized in the final design and to discuss the final layout.

5.2 Varactors topologies

The topologies of varactors widely used are:

- p-n reverse biased diode
- MOS varactors:
    1. Drain-Source-Bulk structure (D-S-B MOS).
    2. Inversion-mode MOS (I-MOS)
    3. Accumulation-mode MOS (A-MOS)

p-n reverse biased diode

The first topology is a basic structure used in VCOs [18]: a reverse biased diode used as a capacitor. Its simplified electrical model and symbol are shown in Fig.5.1 [64]. This simplified model does not consider the inductance in series with the capacitance. The capacitance C_j is the reverse p-n junction capacitance, $R_{Var,series}$ is the series parasitic resistance and $R_{Var,par}$ is the parallel resistance due to the substrate losses. The capacitance can be varied because C_j has a dependence on the reverse bias voltage V_{rev} of the p-n junction given by Eq.5.1:

$$C_j = C_{j0}\Big(\frac{V_0}{V_0 + V_{rev}}\Big)^m \tag{5.1}$$

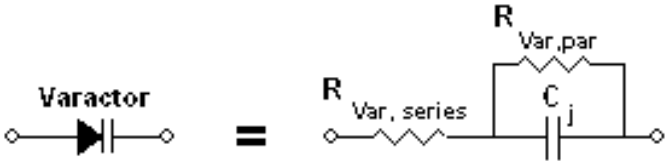
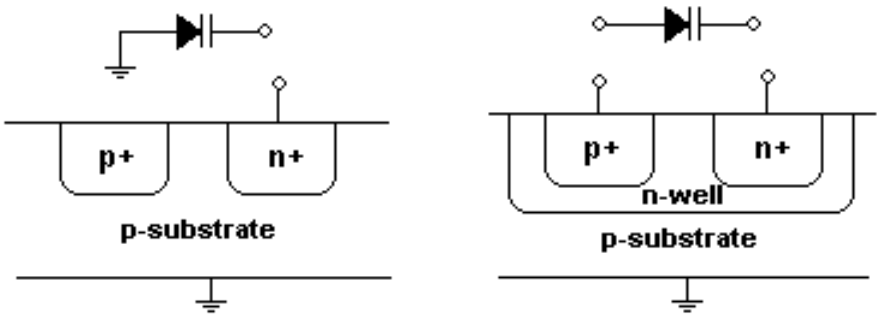


Figure 5.1: Used symbol of the p-n varactor and its simplified model.



(a) Single-ended Structure (b) Differential Structure

Figure 5.2: Typical structures of p-n reverse bias diode

with C_{j0} the junction capacitance at $V_{rev} = 0$, V_0 the contact potential and m a constant which depends on the technology and the physical structure of this varactor (usually $0 < m < 1$).

With this simplified model the quality factor of the p-n reverse varactor $Q_{var,p-n}$ can be expressed as [64]:

$$Q_{var,p-n} = \frac{\omega_0 C_j R_{Var,par}}{1 + \frac{R_{Var,series}}{R_{Var,par}} + \omega_0^2 C_j^2 R_{Var,par} R_{Var,series}} \tag{5.2}$$

For the working frequency of 900MHz this expression can be approximated as:

$$Q_{var,p-n} \approx \frac{1}{\omega_0 C_j R_{Var,series}} \tag{5.3}$$

The quality of this varactor varies with the junction capacitance which also depends on V_{rev}.

Depending on the used technology is the way this structure is built. In usual n-well CMOS processes it can be fabricated two types, shown in Fig.5.2: a single-ended and a differential structure. They can be p+/n-well on p-substrate/n+ structures.

MOS varactor

Other varactor types are those based on the MOS transistor. The MOS transis-

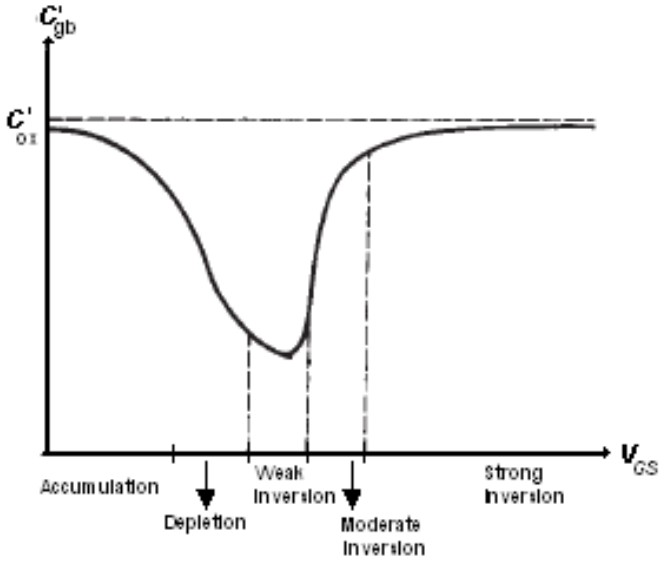


Figure 5.3: Capacitance per unit area C'_{gb} versus V_{GB} (taken from [35])

tor as a capacitor is deeply studied in [35]. The usual MOS transistor working as a capacitor has the source, drain and bulk short circuited, and the capacitor is formed between the gate and bulk plates. Depending on the voltage V_{GB} is the value of the capacitance (per unit area) C'_{gb} and the operating region in which the MOS structure is (see Fig.5.3). In an nMOS transistor if V_{GB} is lower that a certain negative voltage (called Flat Band Voltage V_{FB}), the transistor works in the accumulation region (the gate is charged negatively and the surface below the oxide accumulates holes to provide positive charge). In the accumulation zone $C'_{gb} \approx C'_{ox}$. When $V_{GB} > V_{FB}$ the transistor enters the depletion region (the gate is charged positively and the surface is depleted of holes, being charged negatively with fixed charges); here C'_{gb} begins to fall down . If $V_{GB} \gg V_{FB}$ the transistor is in inversion region: free-electrons are attracted to the surface and the channel is formed. Depending on the value of V_{GB} is the inversion region where the transistor works: weak, moderate or strong inversion. In weak inversion C'_{gb} has the lowest possible value and then it begins to grow until in strong inversion it reaches the value C'_{ox}. The capacitance characteristic of this two-terminal structure is non-monotonic and it is not desirable in a varactor. Thus other structures, like three terminal structures that do not have this behaviour can be used.

The MOS transistor as a three terminal MOS structure (source and drain connected together as shown in the nMOS depicted in Fig.5.4) can be seen also as a variable capacitor with capacitor's characteristics controlled by the drain (source) voltage. The structures used are: (1)Drain-Source-Bulk structure (2) accumulation-mode MOS and (3) inversion-mode MOS transistors [65][66].

Drain-Source-Bulk structure

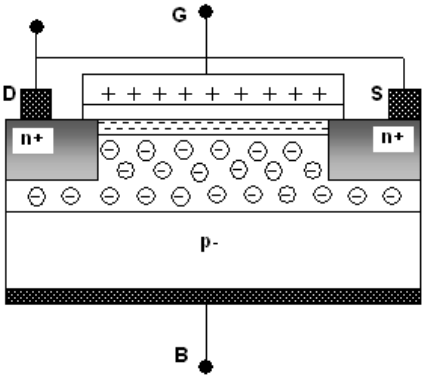


Figure 5.4: Transistor MOS seen as a three terminal structure

This structure consists in connecting together the drain and source with the bulk as it is shown in the pMOS transistor of Fig.5.5(a). This can be seen as the two terminal MOS structure already discussed.

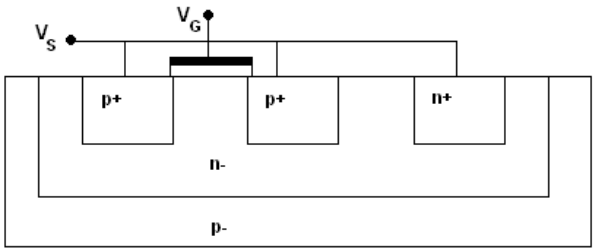
A pMOS transistor with a width of $850\mu m$ and length of $0.35\mu m$, a gate voltage $V_g = 0.6$, connected with Drain=Source=Bulk has the curve of the small-signal normalized (respect of the oxide capacitance C_{ox}) gate capacitance c_{gg} is plotted versus V_{sg} as seen in Fig.5.5(b)(simulated with the the program Smash 5.2.2 [67] using the BSIM3v3).

Inversion-mode MOS capacitor

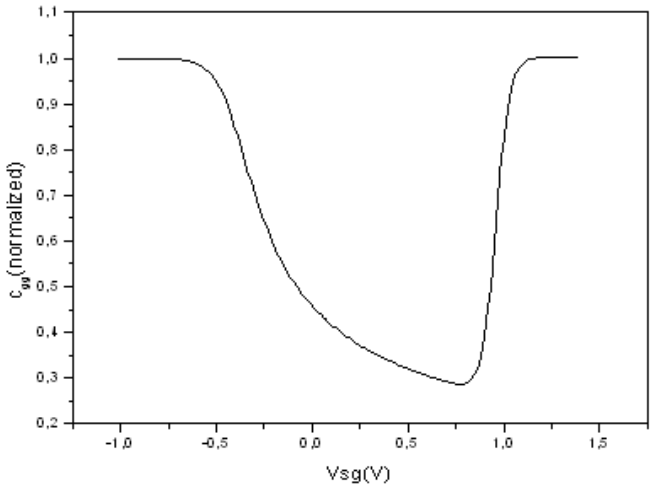
Working with a pMOS transistor structure, the bulk is connected to the highest voltage of the circuit (V_{DD}) and the capacitor is formed between the gate and the drain and source. As the n-well connection of the device is always connected to the highest possible voltage, the gate voltage shall be equal or lower to the bulk voltage and the transistor is working always in the inversion zone (I-MOS)(Fig.5.6(a)). For the usual technologies which have only one bulk, the nMOS transistors are not commonly used because the bulk voltage cannot be varied as it is connected to the substrate which is necessarily connected to ground.

The characteristic of this device is monotonic and non-linear, and the transition between the minimum possible capacitance C_{min} to the maximum one C_{max} is very sharp.

Using the same pMOS transistor that in the example of the previous structure but with the bulk connected to V_{DD} =3V, it has been plotted in Fig.5.6(b) the normalized gate capacitance c_{gg} (simulated with the the program Smash 5.2.2 [67] using the BSIM3v3). It is clearly visible the sharp slope of the curve, which means that with a small variation of the bias voltage the capacitance changes considerably (see the detail view of Fig.5.6(c)). Here the transition from C_{min} and C_{max} happens approximately in $V_{bias,high} - V_{bias,low} = \Delta V = 450mV$.



(a) Cross-section view



(b) c_{gg} vs V_{sg}

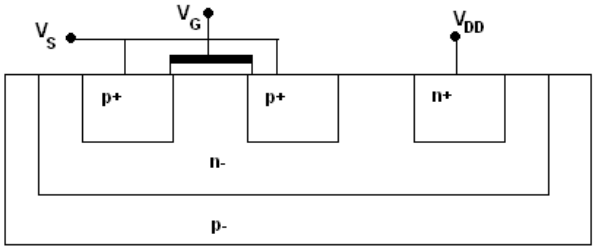
Figure 5.5: Characteristics of the D-S-B structure

Accumulation-mode MOS capacitor

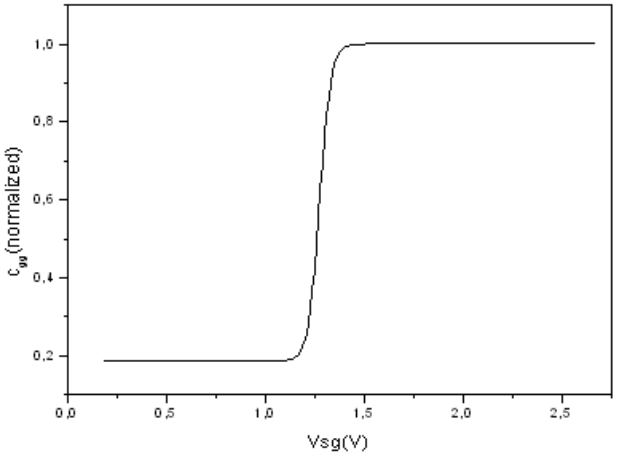
To obtain an accumulation-mode MOS capacitor (A-MOS) the inversion has to be prevented and to do so the injection of holes to the channel has to be avoided (working with a pMOS transistor). To assure this, the pMOS transistor is modified and the the p+ zones are changed for a n+ zones, as it is shown in Fig.5.7(a).

The variable capacitance characteristic is also monotonic and non linear but the transition from C_{min} to C_{max} is much softer that in the inversion-mode transistor, as it is shown in Fig.5.7(b)(simulated with the the program Smash 5.2.2 [67] using the BSIM3v3). The curve only intends to show the behaviour of this structure. The simulation has been done with a pMOS with p+ zones and to avoid the inversion region the V_g voltage has been increased up to 2.2 Volts (we do not have a model of a pMOS with the +n zones to make a simulation). It takes almost 1V to do the transition, 0.5V more than in the inversion-mode.

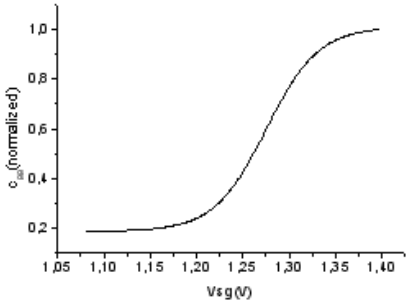
From the three MOS structures previously mentioned, the accumulation mode MOS is the best because of the smoothness of the slope, which means that the VCO



(a) Physical scheme

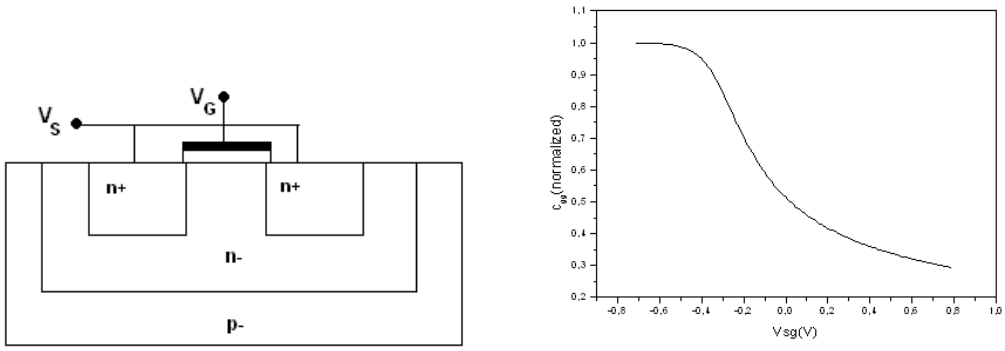


(b) Gate capacitance c_{gg} versus V_{sg}



(c) Detail of the c_{gg} versus V_{sg}

Figure 5.6: Inversion-mode MOS.



(a) Physical scheme

(b) Gate capacitance c_{gg} versus V_{sg}

Figure 5.7: Accumulation-mode MOS.

gain K_{VCO} decreases (see Eq.2.2). Its behaviour is good when a VCO containing this varactor is used in a PLL because the PLL phase noise is reduced [37].

We have decided to use the inversion-mode MOS as a varactor instead of a accumulation-mode MOS. It was because at the moment of the design we did not have models which could describe correctly the behaviour of an accumulation-mode MOS. To validate a possible design with the A-MOS several chip fabrications and physical tests might be needed and it was not possible.

5.3 Quality factor and Parasitic Resistance of the I-MOS varactor

The quality factor of the I-MOS varactor is:

$$Q_{var} = \frac{1}{R_{s,var}\omega_0 C_{gg}} \tag{5.4}$$

where $R_{s,var}$ is the series resistance of the varactor. To increase the varactor quality factor, the gate capacitance, the series resistance (directly related with the varactor capacitance, proportional to the I-MOS size) or the frequency have to be reduced. For a particular working frequency, to reduce the varactor capacitance (and resistance) the inductor value has to increase. Reducing the varactor capacitance also reduces the tuning range. Therefore a compromise between the inductor and varactor sizes have to be reached.

The parasitic resistance of the varactor is what determines the Q_{var} value. This parasitic resistance is highly determined by the layout geometry. The use of a multi-fingered structure (see Fig.2.14) is needed to reduce this resistance because generally the widths of the I-MOS are very large.

The series resistance of an inversion-mode pMOS combines the gate resistance, the contacts to polysilicon and diffusion and the resistance of the inverted channel.

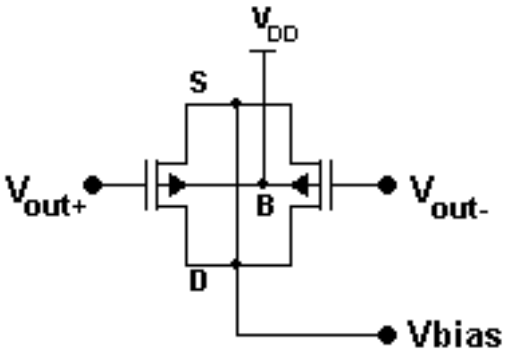


Figure 5.8: Differential structure of two I-MOS varactors.

The expression of this resistance is [66]:

$$R_{s,var} = \frac{1}{12N}\left(R_{ch,square}\frac{L}{W} + R_{poly,square}\frac{W}{L}\right) = \frac{1}{12N}\left(\frac{1}{k_p(V_{BG} - |V_{T_0,p}|)}\frac{L}{W} + R_{poly,square}\frac{W}{L}\right) \tag{5.5}$$

where N is the number of fingers, k_p is the gain factor of the pMOS transistor, $R_{ch,square}$ is the sheet resistance of the channel in triode region [65] and $R_{poly,square}$ is the poly resistance per square including the contacts. The factor 12 is due to the distributed characteristic of the channel, considering an RC model and also connections on both sides of the gate [13]. As the $R_{poly,square} \ll R_{ch,square}$ the length has to be minimized, so the process minimum length has to be used [66].

Moreover, increasing the number of fingers minimizes the series resistance but increases the varactor parasitic capacitances which, as it has been discussed in Chap.2 can limit the tuning range. It also increases the varactor area, which can limit the inductor available area (remember that one of the VCO specifications is the maximum VCO area available).

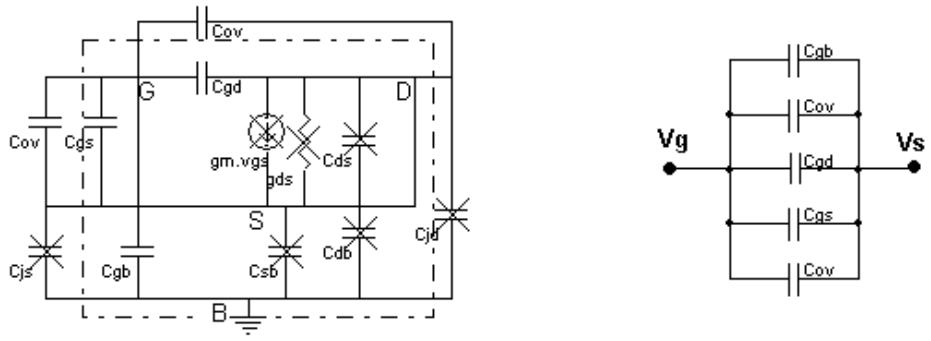
5.4 Final Varactor Design

As it has been mentioned beforehand, we use an inversion-mode varactor despite we know that the A-MOS varactor has better performance because of the lack of simulation models of these structures.

We use two I-MOS connected together by their sources, drains and bulks as in the Fig.5.8.

A matlab routine has been done to calculate the width of the varactor. To do so the varactor has been modelled with the 5-capacitances quasi-static small-signal transistor model, as it is depicted in the scheme of Fig.5.9(a). The source and drain are connected together and are, with the bulk, a "virtual ground". For this reason some elements of the model are short-circuited; they are shown in Fig.5.9(a) with a cross (X) over them.

The remained elements (only capacitances) are shown in Fig.5.9(b). As the



(a) Intrinsic and extrinsic capacitance model (the crosses show which element in short-circuited as D=S=B="virtual ground" in small-signal)

(b) Equivalent model

Figure 5.9: Inversion-mode varactor small-signal electrical model.

source width is equal to the drain width, C_{ov} is the same for both nodes. Thus, the gate capacitance is:

$$C_{gg} = 2C_{ov} + C_{gs} + C_{gd} + C_{gb} = 2\big(C_{ov} + C_{gs}\big) \tag{5.6}$$

Considering that we are working in saturation, $C_{gd} \approx 0$ and then:

$$C_{gg} = 2C_{ov} + C_{gs} + C_{gb} \tag{5.7}$$

Modelling the capacitances with the ACM model [33] as a function of the current i(see Eq.2.12), the C_{gg} is (with $i_f = i_r = i$ -see A.5 for more details-):

$$C_{gg} = 2C_{ov} + \frac{C_{ox}}{n}\left(n - \frac{1}{\sqrt{1+i}}\right) \tag{5.8}$$

To relate the current i with the voltage V_{sg} we use the following expression:

$$V_{sg} = -\left(V_{T_0} + nU_t\left(\sqrt{1+i} + ln\big(\sqrt{1+i} - 1\big) - 2\right)\right) \tag{5.9}$$

In Chap.2 it has been shown that one of the results of the proposed design methodology is the value of the varactor capacitance at the central frequency f_0.As it has been stated in Chap.2 we consider the central frequency as the frequency obtained at $(V_{bias,low} + V_{bias,high})/2$. Therefore, having the varactor capacitance at this voltage, we iterate until the width of the transistor is obtained. We use an approximate value of the varactor capacitance at the central frequency of around $0.5C_{ox}...0.55C_{ox}$

The capacitance value of both varactors at 910MHz is around $C_{gg} = 750fF$. Then the capacitance of each varactor at this frequency is approximately 1.5pF. This

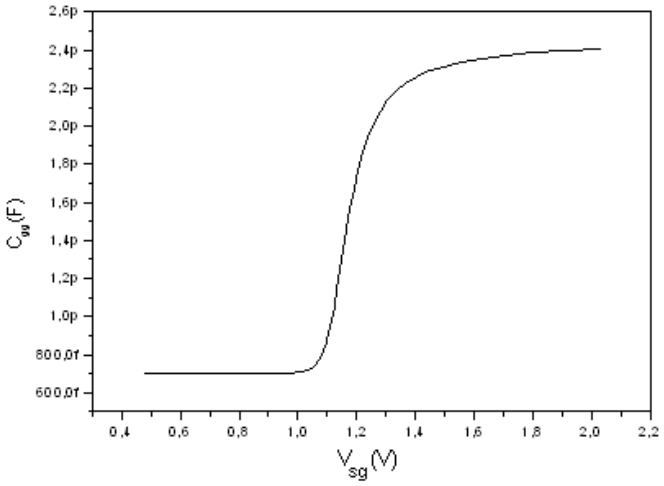


Figure 5.10: Simulated c_{gg} curve of both varactors.

is the value considering the overlapping capacitances C_{ov}. Without C_{ov} the C_{gg} value is 1.3pF. This value is approximately reached with an I-MOS of $W = 1550\mu m$. The C_{gg} vs. V_{sg} curve of both transistors -simulated with the the program Smash 5.2.2 [67] using BSIM3v3- is shown in Fig.5.10.

As we have already seen, the C_{max} tends to be C_{ox}. The value of C_{ox} is:

$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}} WL \tag{5.10}$$

being ϵ_{ox} the oxide dielectric constant ($\epsilon_{ox} = 0.345e-10F/m$) and t_{ox} is the oxide thickness ($t_{ox} \cong 7.6e-9m$ for the $0.35\mu m$ technology used). For $L = 0.35\mu m$ and $W = 1550\mu m$ the C_{ox} value is approximately 2.46pF. If we compare this value with the maximum value of C_{gg} shown in Fig.5.10 we can see that both coincide as it was expected.

The series resistance of the varactor varies as the V_{gs} voltage change through a whole period. Then, to obtain a mean value of $R_{s,var}$ we take the mean value of V_g and the value of V_s @ 910MHz, then $V_{sg} = 1.2V - 0.6V \cong 0.6V$ then $V_{sg} - V_{t,p} \cong 1.1V$. The term of R_{ch} in the $R_{s,var}$ is approximately $4m\Omega$.

The term of the $R_{poly,square}$ expression depends of this technology parameter, which in this case is $R_{poly,square} \cong 8\Omega/square$. With this value the whole term is equal to 13Ω.

It is clear that, as the transistor length is minimum and the width is very large, the most important term of the series resistance equation is the one of the poly sheet resistance. The total series resistance of each multi-fingered varactor I-MOS has a mean value of 13.5Ω.

To calculate the quality factor value, it has been considered the central frequency and its associated varactor capacitance. With a $f_0 = 910MHz$, $C_{gg} = 1.3pF$ (considering only the intrinsic capacitances) and a resistance $R_{s,var} = 13.5\Omega$ the qua-

lity factor is $Q = 10.9$. Its value is not very high but with respect of the quality factor of the inductor is sufficiently good to neglect the effect of the resistance of the varactor in the tank resistance.

To reduce more the resistance a higher number of fingers N might be chosen. But this implies higher parasitics capacitances. In this design this has been a problem because the VCO has been charged considerably with other blocks of a frequency synthesizer and it has not been possible to increase N.

Varactor Layout

The varactor layout has been done following the scheme of Fig.2.15 of Chap.2. Each I-MOS varactor was designed separately, placed symmetrically respect of a vertical axis. The interlaced layout between both varactor transistors has not been done because it increases the parasitic capacitances of the I-MOS, despite doing this could jeopardize the matching between both I-MOS transistors. The complete view of both varactors is shown in Fig.5.11(a). Fig.5.11(b) shows a partial view of the interlaced layout.

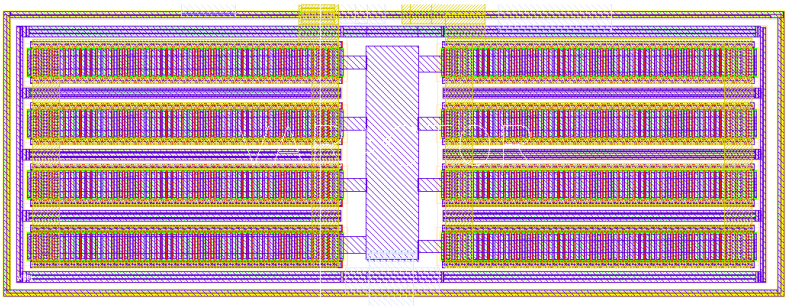
Each varactor has been divided into 4 parts, each one with 55 transistors of $W = 7\mu m$, as it is seen in Fig.5.11(a)[31]. It has been added as much contacts as possible in gate, source and drain.It is specially important in the gate to decrease as much as possible the contribution of the contact resistance in the series resistance of the varactor.

5.5 Conclusions

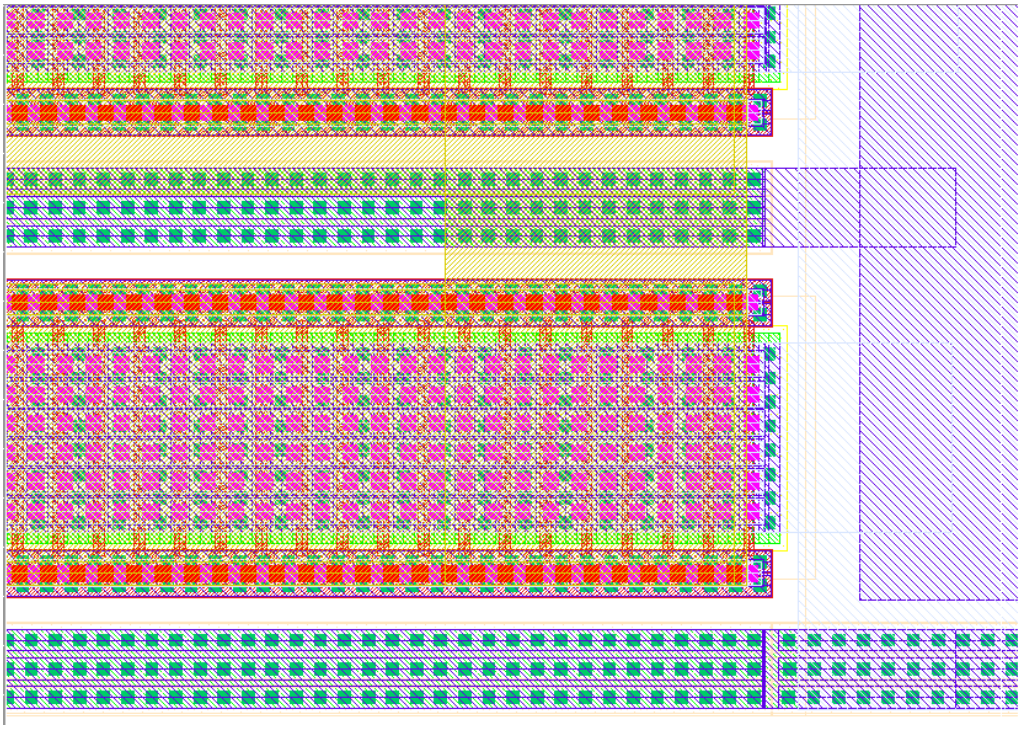
In this chapter it has been studied the different structures of varactors commonly used and the is has been shown that the A-MOS has better performance.

It has been also explained that the reason why it has been used the I-MOS varactors has been because we lack of models to simulate the A-MOS structure.

Finally it has been presented the varactor designed and its characteristics. This varactor does not have a very good quality factor because its series resistance is not too low. But a compromise was reached between the series resistance and the parasitic capacitances to obtain the frequency desired. Also the Q is sufficiently high to not consider the parasitics effects of the resistance in the whole VCO design.



(a) Complete view



(b) Partial view

Figure 5.11: Varactor Layout

Chapter 6
Measurements

6.1 Introduction

To validate the simulation results done throughout this work several measurement of different aspects of the fabricated VCO have been done. All the measurements were performed over one packaged chip. To mount the chip a PCB has been done and external components such as baluns, filter capacitors and SMA connectors has been used. An on-chip VCO buffer has been designed to test the VCO. Measurements of the current consumption, the power spectral density and the phase noise of the VCO were performed.

6.2 Measurement Setup

To do the measurements a PCB has been designed (see App.C.1 for the details of the fabricated PCB). As the fabricated chip contains a PLL (which includes a VCO), a separate VCO and other circuits, the PCB was designed to measure all of these circuits.

To measure the VCO we put an on-chip buffer at the VCO's outputs. This block has been added to have a fixed capacitive load at the VCO's outputs isolating the VCO from the external variable load (pads, bonding, outside-chip load).

The buffer is a differential pair with an off-chip current source. The buffer load is also outside of the chip. The buffer structure is seen in Fig.6.1. The size of the transistors is $W = 324\mu m$ and $L = 0.35\mu m$

The output signals of the buffer are the drains of its transistors. The buffer was designed to have a $g_m^{buff}/I_D = 3$, with g_m^{buff} the buffer transistor's transconductance.

To calculate the gain of the buffer we have to consider the DC and AC equivalent impedances seen from the drains of the transistors. The scheme of the buffer and its load is shown in Fig.6.2.

At DC, the chokes (with values of around 400nHy) filter the RF signal and the load is the only the R_{loadDC}. At AC the RF signal is decoupled from the continuous voltage using the capacitor C_{filter}.

In DC, for a buffer current I_{buff} and a DC load resistance R_{loadDC}, the drain voltage is

$$V_{D,DC} = \frac{I_{buff}}{2} R_{loadDC} \tag{6.1}$$

For $I_{buff} = 15mA$ and $R_{loadDC} = 50\Omega$, the $V_{D,DC} \cong 0.4V$.

The balun is used to generate a single signal -referenced to ground- from the differential signal of the buffer. Its input and output impedances are 50Ω. The input impedance is differential so each output pin of the buffer sees 25Ω respect of

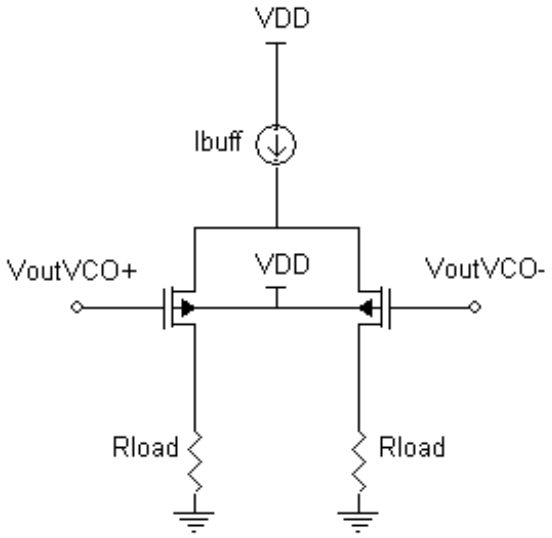


Figure 6.1: Structure of the buffer used

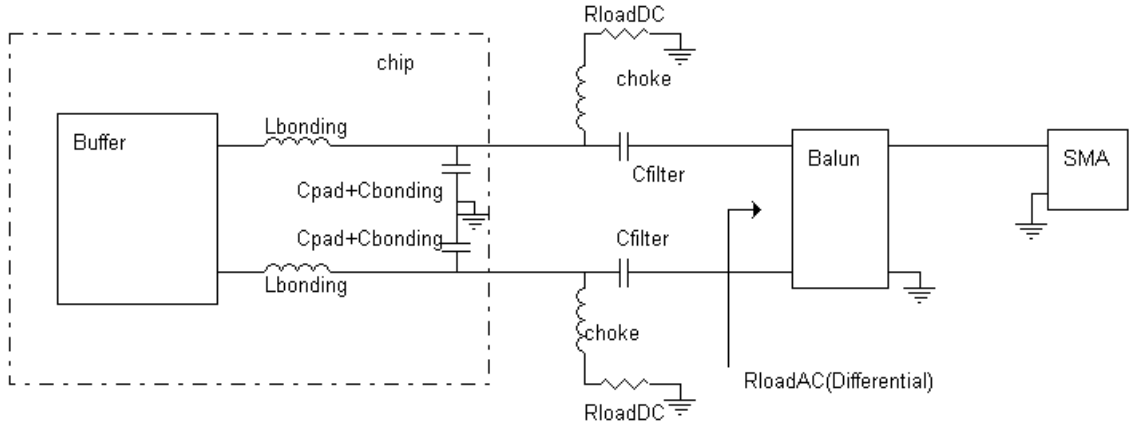


Figure 6.2: Scheme of the buffer and its load (AC and DC load) as it is implemented in the PCB

ground. The output impedance is matched with the input impedance seen to the SMA connector, which is also 50Ω

To check that the measured power at the peak frequency of the spectrum is the expected, a Cadence simulation has been done. Considering that $L_{bonding} = 5.6nHy$ and $C_{bonding} + C_{pad} = 4.8pF$ ($L_{bonding}$ and $C_{bonding}$ are typical values), the equivalent resistance at 910MHz seen from each branch of the buffer is around $R_{eq} = 22\Omega$. It means that the gain of the buffer is: $G_{buff} = R_{eq} * g_m^{buff} \cong 0.5$. With the values of $L_{bonding}$ and $C_{bonding} + C_{pad}$ used previously to calculate the gain, a VCO bias current $I_{bias} \cong 3mA$ and a varactor bias voltage $V_{bias} = 0$, it has been obtained by simulation that output voltage of the buffer is $V_{out,buffer}^{peak} \cong 0.25V$ and that the VCO output voltage is $V_{out,VCO}^{peak} \cong 0.55V$. It means that effectively the gain is $G_{buff} \cong 2$.

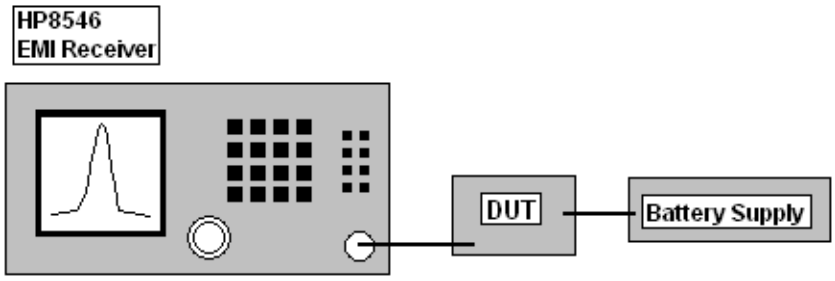


Figure 6.3: Measurement setup for PSD tests and Phase Noise tests

The measured power value at the VCO working frequency is around -1.20dBm (with $V_{bias} = 0$). Considering the losses of the measurement setup, the power at the output of the buffer is estimated at 0.3dBm. Supposing the same values of the bonding and pad parasitics considered previously, the VCO peak output voltage $V_{out,VCO}^{peak}$ is estimated around 0.6V. Thus, there is good agreement between the measurements and the simulation of the output VCO voltage.

It has alto been checked the maximum current at which the oscillation does not start. The measured current was 1.2mA and the expected current was 1mA.

The current consumption of the VCO is of 3mA, with a supply voltage of 3V, which means a power consumption of 9mW. The PSD and phase noise measurements have been done with the previous values.

6.3 PSD measurements

The measurement setup for the power spectral density (PSD) of the VCO output is shown in Fig.6.3. It has been used a HP8546A EMI receiver to sense the PSD. A set of current and voltage supplies using batteries has been done, as very bad performance has been seen when using an equipment connected to the mains network (this equipment was a Semiconductor Parameters Analyzer HP4155).

To obtain the frequency versus V_{bias}(bias voltage of the varactor), a sweep of V_{bias} has been done. The results are shown in Fig.6.4

The VCO gain for the simulated and measured VCO, the approximated linear range as well as the tuning range are given in Table 6.1.

	K_{VCO}	frequency range	tuning range
Simulated	-169MHz/V	945MHz-850MHz	11%
Measured	-214MHz/V	937MHz-810MHz	15%

Table 6.1: K_{VCO} simulated and measured.

Two VCOs have been fabricated in the chip, one isolated and the other being part of the PLL, as it is shown in Fig.6.5. The test of the oscillation frequency

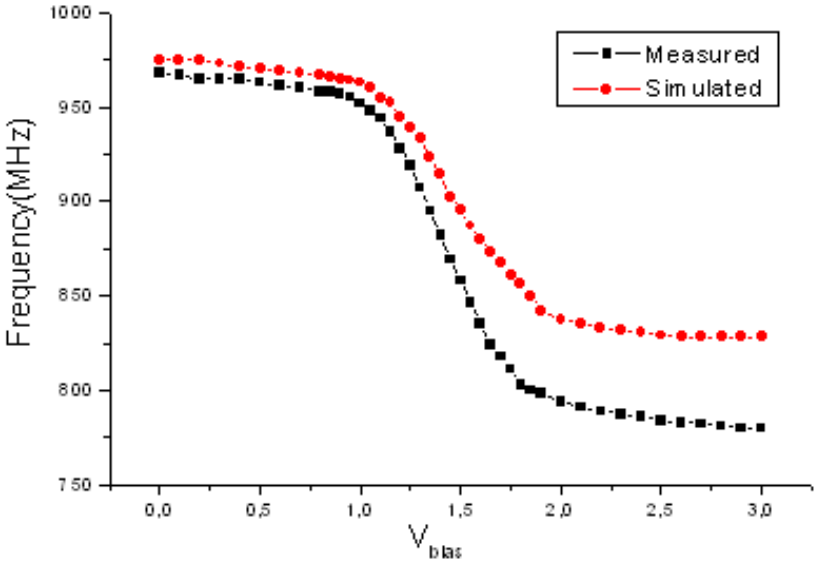


Figure 6.4: VCO oscillation frequency versus V_{bias}

versus V_{bias} was done with the isolated VCO. The study of the power spectrum of the signal has been done with the PLL's VCO. Some differences were encountered specially in the frequency range. The highest frequency of the VCO belonging to the PLL was approximately 25MHZ lower respect of the isolated one. It is expected as the former has more capacitive load.

The output spectrum of the signal with $V_{bias} = 0$ is the one shown in Fig.6.6.

6.4 Phase noise measurements

As we do not have any equipment to measure the phase noise of the signal, we use the same setup as in the PSD measurement. We apply the definition of the phase noise (refer to Eq.3.3) to obtain a set of results.

We measure it at different frequency offsets from the carrier. The bandwidth used was 30Hz instead on 1Hz as it is stated in the definition, but we considered that no appreciable difference will be measured (30Hz is the smallest bandwidth of the equipment used). At Table 6.2 the values of the phase noise measured are given.

Δf from the carrier	phase noise measured (dBc/Hz)
100kHz	-87
600kHz	-102
1MHz	-107

Table 6.2: Phase noise measured at $V_{DD} = 3V$ and $I_{bias} = 3mA$

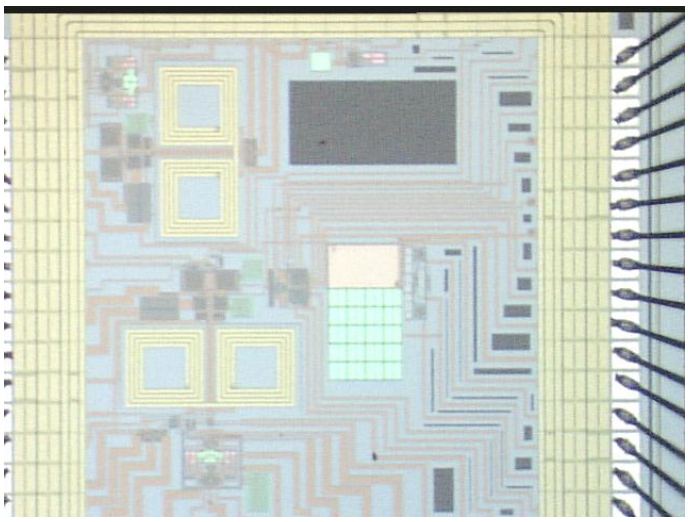


Figure 6.5: Die-photograph containing the PLL and the isolated VCO

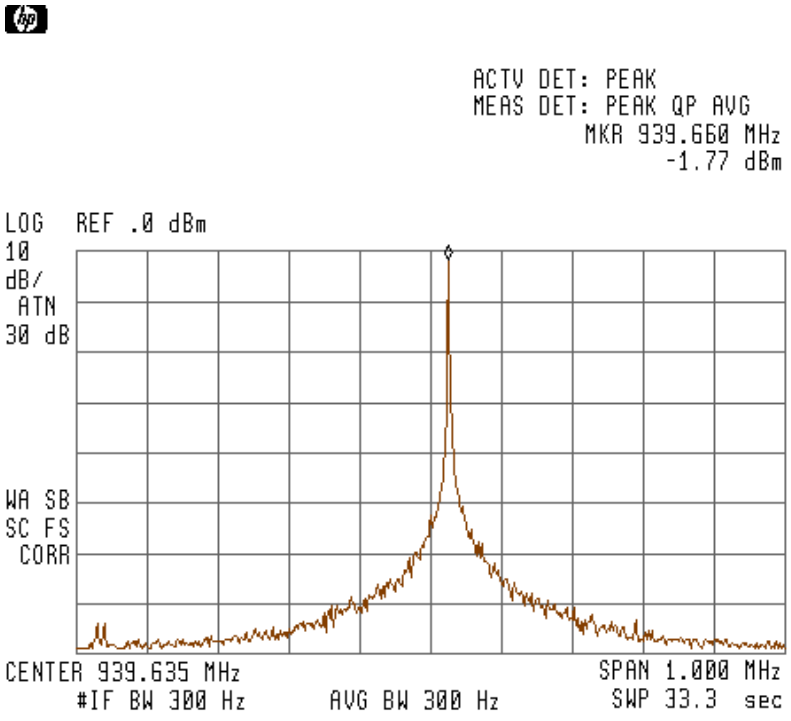


Figure 6.6: VCO oscillation frequency versus V_{bias}

6.5 Conclusions

It has been possible to test working characteristics of the VCO, its current consumption as well as its range of operation and the phase noise at the output of the packaged chip. The values of output power and consumption are as expected. The phase noise was higher than the values of the the simulations (approximately 10dbc/Hz higher). We suppose that this difference was due to the measurement setup, as it was very sensitive to external interference.

The characteristics of the inductor and the varactor were not measured as no adequate equipment (such as microprobe testing equipment or network analyzer) was available.

Chapter 7
Conclusions and Future Work

7.1 Introduction

In this chapter the challenges of designing a fully integrated VCO as well as the key features of the designed VCO and its possible improvements are discussed. A brief discussion about designing in moderate inversion is given as well as comments about the design methodology proposed. A conclusion is drawn and future work on this subject is also included.

7.2 Challenges of designing an on-chip low power VCO

There are several difficulties in designing low power on-chip VCOs with good performance. As we have already mentioned, the phase noise is a very important feature of the VCO because high phase noise jeopardizes the reception and transmission of a signal. But the way to decrease the phase noise is increasing the bias current of the circuit. So a trade-off between the consumption of the circuit and the phase noise generated must be found.

The on-chip VCO is a feature of the circuit that has pros and cons. The fact that the VCO is in a chip makes a design more compact and robust. But as monolithic inductors are used the VCO quality factor is reduced considerably. On-chip inductors in CMOS standard technology have $Q \cong 3..5$ while off-chip inductors can have quality factors of 40 [12]. However improvements have been done [15] [24][68] to increase the inductor low-quality-factor.

The inductor value also fixes the phase noise. If the quality factor of the inductor is not constant (as generally occurs) and the inductor value is raised the phase noise rises too, although this increment is small.

The inductor highly determines the VCO current consumption. In CMOS technologies the on-chip inductors have low quality factor values so the current consumption rises respect of a high quality inductor. The VCO transistors' g_m is proportional either to the bias current and to the inductor conductance(refers to Eq.2.15). It means that a low quality inductor has a higher conductance than a high quality one and then the current consumption is also higher.

The MOS varactor might modify the characteristics of the VCO, specially if the width of it is large enough to deteriorate its quality factor. In this component is specially important doing a multi-fingered layout, and choose correctly the number of fingers.

The parasitic capacitances of the layout cannot be neglected, specially working in moderate inversion region. In this region the width of the transistors can be sufficiently high so that the overlap and junction capacitances cannot be neglected.

If a careless layout is done and all the parasitics are not taken into account, the VCO working frequency shall drop dozens of megahertz below the expected frequency or even more.

The current source is also an important block of the VCO. Its noise is upconverted by the cross-coupled block and it increases the VCO phase noise. By choosing a pMOS current source with very big transistors makes decrease the injected noise to the VCO.

7.3 Key features of the proposed VCO

The VCO designed has a current consumption of 3mA, a measured phase noise of -107dBc/Hz @1MHz, a tuning range of 15% for a 3V supply and an area of $500\mu m$ by $600\mu m$. These values are under the initial specifications of the VCO.

The minimum current at which the VCO oscillates was measured to be 1.2mA, and very good correlation exists between this value and the one expected from calculation. The measured power at the working frequency was 0.3dBm (through an auxiliary output buffer), as it was expected. The buffer added at the output of the VCO works correctly.

7.4 Moderate inversion and design methodology

The design of the cross-coupled transistors of the VCO in moderate inversion region allow us to reduce as much as possible the current consumption of the circuit. In fact, it has been chosen the higher g_m/I_D at which the VCO can work -without having a varactor capacitance too small- at a central frequency of 915MHz. But there are difficulties when working in this region. Firstly the width of the transistors increases when working in moderate inversion. The width goes from $80\mu m$ to $340\mu m$ for the nMOS transistors and $200\mu m$ to $780\mu m$ for the pMOS transistors when working with $g_m/I_D = 5$ and $g_m/I_D = 11$ respectively. Then, the large width increases the parasitic capacitances of the VCO not only due to intrinsic but also due to overlap, junction and interconnect capacitances. And finally the large capacitances reduce the varactor value and the tuning range.

The design methodology using the g_m/I_D methodology [25] and the ACM MOSFET model [26] is proven as an interesting tool to design LC VCOs. The results are easily obtained and the consequences in the design features when certain parameters vary (inversion level, bias current and inductance principally) are clearly visible.

The analytical LTV model of the phase noise used [46] agrees completely with the simulations made in RF Spectre of Cadence [61]. It is very good because with a simple Matlab routine the phase noise of an LC VCO was obtained.

7.5 Measurement difficulties

During the measurement stage several problems arise. As in our laboratory we do not have microprobes to test the VCO in the waffer itself we had to test it

using a packaged chip. And to do so a PCB has to be used. All these physical stages between the VCO and the measurement system are more sensitive to electromagnetic interference which is transformed in phase noise at the output.

The 8546 EMI receiver, used to measure the output signal power spectrum, does not have any tool to measure the phase noise. Then the phase noise has to be calculated using the definition of Eq.3.3. The single side band noise spectral density was obtained with this instrument. In fact, it outputs the power at a certain frequency, which is calculated using a filter with a bandwidth not lower than 30Hz. As the phase noise definition states that it has to be calculated with a 1Hz bandwidth, it has not been possible to calculate accurately the power of the noise. Also the EMI receiver does not let us calculate simultaneously the power of the carrier and the power of the noise (the sensitivity of the instrument changes at different power values and the sweep has to be very low).

For all these reasons it was not possible to measure accurately the real phase noise of the VCO.

It would have been very interesting to measure the characteristics of the inductors or the varactor but no instruments were available to do so.

7.6 Final conclusions and future work

A $0.35\mu m$ 900MHz VCO with on-chip inductors, working in moderate inversion region was designed. It has low power consumption, acceptable phase noise and very good tuning range. Despite the problems in the measurement stage is was possible to obtain its approximated phase noise value.

Experience in designing and testing RF CMOS integrated circuits, including on-chip inductors and varactors has been acquired. The phase noise as well as the trade-off between it and the variables involved in the VCO design were deeply studied.

Two works have been presented in a workshop [69] and a symposium [70]. Another work [71] has been presented for evaluation in an international conference.

This work leaves open lots of interesting themes to research in the future. The phase noise in oscillators is a subject which can be developed even more, specially in studying and improving the circuit structures to drop it.

The on-chip inductors fabricated in CMOS standard technologies is another subject which can also be studied and linked with the phase noise of the system. With respect to the design methodology, it can be added an inductors'area optimization routine to obtain rapidly a VCO design without using other tools (as ASITIC for example [53]).

Adding to this, the topic of the interconnect parasitic capacitances has not been considered in the design methodology, so to obtain a better model of the VCO, a quantification of these capacitances might be added in the design methodology proposed.

The varactor losses were neglected in the design methodology suggested. It would be interesting to quantify the varactor quality factor in the design routine

and also to make an optimization routine to obtain the best number of fingers of the varactor transistors.

Another feature which can be improved is, instead of inversion mode MOS varactors, using accumulation mode varactors[65]. If the VCO which contains these varactors is used in a PLL, the phase noise of the PLL is lowered as those varactors generate a lower K_{VCO} [37].

From the above discussion, there is a lot of interesting work to be done from now, hoping to going on improving our knowledge in these amazing matters.

Appendix A

A.1 Relation between the bandwidth of the tank impedance and the tank quality factor

The module of the impedance of an RLC tank is:

$$|Z(\omega)|^2 = \frac{(R^2 L\omega(1 - LC\omega^2))^2 + R^2(Lw)^4}{R^2(1 - LC\omega^2)^2 + (\omega L)^2} \tag{A.1}$$

The bandwidth B of the tank is defined when $|Z(\omega)| = |Z(\omega_0)|/\sqrt{2}$ (3dB drop)(see Fig.A.1). Then:

$$\frac{(R^2 L\omega(1 - LC\omega^2))^2 + R^2(Lw)^4}{R^2(1 - LC\omega^2)^2 + (\omega L)^2} = R^2/2 \tag{A.2}$$

Lets work with this equation:

$$2(R^4)(L\omega)^2(1-LC\omega^2)^2+2R^2(L\omega)^4 = (R^6(1-LC\omega^2)^4+2R^4(\omega L)^2(1-LC\omega^2)^2+R^2(\omega L)^4) \tag{A.3}$$

Simplifying this equation we obtain:

$$\frac{L\omega}{R} = 1 - LC\omega^2 \tag{A.4}$$

If we use the equality $LC = 1/\omega_0^2$ then the previous equation is transformed into:

$$\frac{L\omega}{R} + \frac{\omega^2}{\omega_0^2} - 1 = 0 \tag{A.5}$$

Rewriting this equation:

$$\omega^2 + \omega_0^2 \frac{L}{R} - \omega_0^2 = 0 \tag{A.6}$$

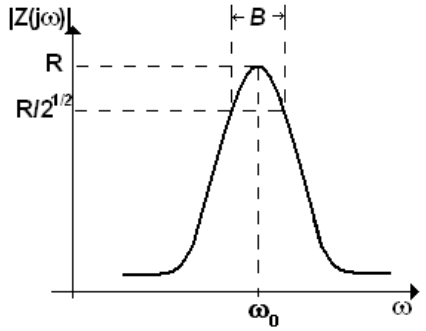


Figure A.1: Equivalent tank impedance value

As $Q = R/\omega_0 L$, the root of this equation is:

$$\omega = -\frac{\omega_0}{2Q} + \frac{1}{2}\sqrt{(\frac{\omega_0}{Q})^2 + 4\omega_0^2} = -\frac{\omega_0}{2Q} + \frac{\omega_0}{2Q}\sqrt{1+4Q^2} \tag{A.7}$$

As $Q = R/\omega_0 L$, the root of this equation is:

$$\omega = \omega_0 - \frac{\omega_0}{2Q} \tag{A.8}$$

As the root ω is $\omega_0 - B/2$ then B/2 is:

$$\frac{B}{2} = \frac{\omega_0}{2Q} \tag{A.9}$$

A.2 Phase Noise vs. the transconductance-to-current ratio

The phase noise Leeson's formula is (from Eq. 3.10):

$$\mathcal{L}(\Delta\omega) = \frac{2kTF}{P_{carrier}}\frac{\omega_0}{2Q\Delta\omega} = \frac{4kTRF}{V_0^2}\frac{\omega_0}{2Q\Delta\omega} \tag{A.10}$$

as

$$P_{carrier} = \frac{V_0^2}{2R} \tag{A.11}$$

If

$$Vo = R \cdot I_{bias} 4/\pi = R \cdot I_D \cdot 8/\pi \tag{A.12}$$

and

$$\frac{g_m}{I_D} = \frac{\alpha}{R \cdot I_D} \tag{A.13}$$

then

$$\mathcal{L}(\Delta\omega) = \frac{4kTRF}{R^2 \cdot I_D^2 \cdot 8^2/\pi^2 \cdot 4Q^2}\Big(\frac{\omega_0}{\Delta\omega}\Big)^2 = \frac{4kTF}{(\alpha/(g_m/I_D))I_{bias}/2 \cdot 8^2/\pi^2 \cdot 4Q^2}\Big(\frac{\omega_0}{\Delta\omega}\Big)^2 \tag{A.14}$$

this equation can be rewritten as

$$\mathcal{L}(\Delta\omega) = \frac{kT\pi^2}{32}\frac{F}{\alpha}\frac{1}{Q^2}\frac{g_m/I_d}{I_{bias}}\Big(\frac{\omega_0}{\Delta\omega}\Big)^2 \tag{A.15}$$

A.3 Equivalence between the inductor series resistance and the parallel resistance

In this section we would like to obtain the equivalence between the circuit with an inductance L_s and a resistance R_s in series and the circuit with an inductance $L_{par}$and a resistance R_{par} in parallel as it is shown in Fig.A.2.Both circuits must

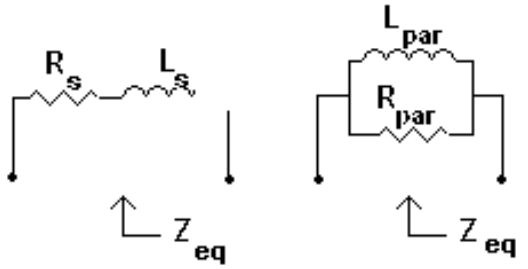


Figure A.2: Equivalence of parallel circuit and series circuit

have an equivalent impedance, then

$$Z_{eq} = R_s + jwL_s = R_{par}//jwL_{par} = \frac{R_{par}jwL_{par}}{R_{par} + jwL_{par}} \tag{A.16}$$

Then, separating the real and imaginary part of the equality

$$R_s + jwL_s = \frac{R_{par}w^2L_{par}^2}{R_{par}^2 + w^2L_{par}^2} + j\frac{wL_{par}R_{par}^2}{R_{par}^2 + w^2L_{par}^2} \tag{A.17}$$

It means that

$$R_s = \frac{R_{par}w^2L_{par}^2}{R_{par}^2 + w^2L_{par}^2} \tag{A.18}$$

$$L_s = \frac{L_{par}R_{par}^2}{R_{par}^2 + w^2L_{par}^2} \tag{A.19}$$

As the denominator of EqsA.18 and A.19 are equal and, from Eq.4.5 $Q = \frac{\omega L_S}{R_S}$

$$\frac{wL_{par}}{R_{par}} = \frac{R_s}{wL_s} = \frac{1}{Q} \tag{A.20}$$

With Eqs.A.18 and A.20 we obtain the following formula:

$$R_{par} + w^2L_{par}^2 - \frac{w^2L_{par}^2}{R_s}R_{par} = 0 \tag{A.21}$$

$$R_{par}\Big(1 + \frac{1}{Q^2} - \frac{R_{par}}{Q^2R_s}\Big) = 0 \tag{A.22}$$

$$R_{par} = (Q^2 + 1)R_s = \frac{Q^2 + 1}{Q}wL_s \tag{A.23}$$

and with Eqs.A.19 and A.20 :

$$R_{par}L_s + w^2L_{par}^2L_s - L_{par}R_{par}^2 = 0 \tag{A.24}$$

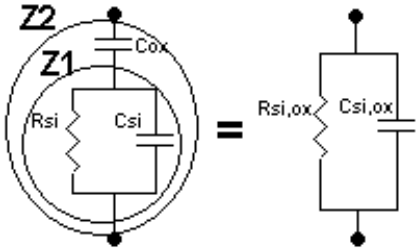


Figure A.3: Conversion of the configuration of R_{si},C_{si} and C_{ox} into a scheme of a capacitor C_si, ox and a resistance $R_{si,ox}$ in parallel.

$$w^2 L_{par}^2 (Q^2(L_s - L_{par}) + L_s) = 0 \tag{A.25}$$

$$L_{par} = \frac{Q^2 - 1}{Q^2} L_s \cong L_s \tag{A.26}$$

A.4 Deduction of the $R_{si,ox}$ and $C_{si,ox}$ values

In this section there will be deduced the values of $R_{si,ox}$ and $C_{si,ox}$ when we have a series of the C_{ox} capacitor with the impedance $C_{si}||R_{si}$ as it is shown in Fig.A.3.

From Fig.A.3, we define Z_1 as:

$$Z_1 = \frac{s}{sC_{si} + G_{si}} \tag{A.27}$$

with $G_{si} = 1/R_{si}$.

Then, the impedance Z_2 is:

$$Z_2 = \frac{1}{sC_{ox}} + Z_1 = \frac{1}{sC_{ox}} + \frac{s}{sC_{si} + G_{si}} = \frac{s(C_{si} + C_{ox}) + G_{si}}{s^2 C_{si} C_{ox} + sC_{ox} G_{si}} \tag{A.28}$$

If we want to rewrite Z_2 as a parallel of a resistance R and a capacitance C, we can study instead of Z_2, the conductance $1/Z_2 = G_2$ which will be equal to $1/R + sC = G + sC$. Then:

$$G_2 = G + sC = s\frac{sC_{ox}C_{si} + C_{ox}G_{si}}{s(C_{si} + C_{ox}) + G_{si}} \tag{A.29}$$

If $s = jw$:

$$G + jwC = jw\frac{jwC_{ox}C_{si} + C_{ox}G_{si}}{jw(C_{si} + C_{ox}) + G_{si}} \tag{A.30}$$

To obtain separately the real and the imaginary part of G_2 we multiply and divide

by the conjugate of the denominator:

$$G + \jmath wC = \jmath w \frac{(\jmath wC_{ox}C_{si} + C_{ox}G_{si})(\jmath w(C_{si} + C_{ox}) + G_{si})}{w^2(C_{si} + C_{ox})^2 + G_{si}^2} \tag{A.31}$$

Working with this equation we obtain:

$$G + \jmath wC = \jmath w \frac{C_{ox}(G_{si}^2 + w^2(C_{si} + C_{ox})C_{si}) - \jmath wG_{si}C_{ox}^2}{w^2(C_{si} + C_{ox})^2 + G_{si}^2} \tag{A.32}$$

Taking the real and the imaginary part:

$$G = \frac{w^2 G_{si} C_{ox}^2}{w^2(C_{si} + C_{ox})^2 + G_{si}^2} \tag{A.33}$$

$$C = \frac{C_{ox}(G_{si}^2 + w^2(C_{si} + C_{ox})C_{si})}{w^2(C_{si} + C_{ox})^2 + G_{si}^2} \tag{A.34}$$

We will call $R_{si,ox} = 1/G$ and $C_{si,ox} = C$ as it is shown in Fig.A.3.

As usually C_{si} is of the same order as C_{ox}, C can be considered very similar to C_{ox}. Also as the denominator of G is bigger that the part that multiplies G_{si}, then $G < G_{si}$.

To see which are the typical values of these variables, we will consider the values of C_{si}, C_{ox} and R_{si} of the technology used in this work. For 910MHz, $G_{si} \simeq 1/600\Omega = 1.6e^{-3}S$, $C_{si} \simeq 40fF$ and $C_{ox} = 160fF$:

$$R_{si,ox} = \frac{(2\pi 910e^6)^2 \cdot (200e^{-15})^2 + (1.6e^{-3})^2}{(2\pi 910e^6)^2 \cdot 1.6e^{-3} \cdot (160e^{-15})^2}\Omega = 2.8k\Omega \tag{A.35}$$

$$C = \frac{160e^{-15}((1.6e^{-3})^2 + (2\pi 910e^6)^2.(200e^{-15}).(40e^{-15}))}{(2\pi 910e^6)^2(200e^{-15})^2 + (1.6e^{-3})^2}F = 117fF \tag{A.36}$$

A.5 I-MOS varactor Gate capacitance versus i

The intrinsic capacitance of the varactor is (see 5.4):

$$C_{gg} = C_{gs} + C_{gd} + C_{gb} \tag{A.37}$$

From [33] the expressions of C_{gs} and C_{gd} are:

$$C_{gs} = \frac{2}{3}C_{ox}(\sqrt{1 + i_f} - 1)\frac{\sqrt{1 + i_f} + 2\sqrt{1 + i_r}}{(\sqrt{1 + i_f} + \sqrt{1 + i_r})^2} \tag{A.38}$$

$$C_{gd} = \frac{2}{3}C_{ox}(\sqrt{1 + i_r} - 1)\frac{\sqrt{1 + i_r} + 2\sqrt{1 + i_f}}{(\sqrt{1 + i_f} + \sqrt{1 + i_r})^2} \tag{A.39}$$

with i_f and i_r the forward and reverse normalized currents defined in [26].

As the drain source current $I_D = 0$ and $I_D = I_S(i_f - i_r)$ then $i_f = i_r = i$ and $C_{gs} = C_{gd}$.

C_{gb} is defined as:

$$C_{gb} = (1 - \frac{1}{n})(C_{ox} - C_{gs} - C_{gd}) = \frac{n-1}{n}(C_{ox} - 2C_{gs}) \tag{A.40}$$

And C_{gs} can be re-written in the following way:

$$Cgs = \frac{C_{ox}}{2}\frac{\sqrt{1+i}-1}{\sqrt{1+i}} \tag{A.41}$$

Then

$$C_{gg} = 2C_{gs} + (1 - \frac{1}{n})(C_{ox} - 2C_{gs}) = \frac{n-1}{n}C_{ox} + \frac{2}{n}C_{gs} \tag{A.42}$$

Substituting the value of C_{gs} in the previous equation we obtain:

$$C_{gg} = \frac{n-1}{n}C_{ox} + \frac{2}{n}(\frac{C_{ox}}{2}\frac{\sqrt{1+i}-1}{\sqrt{1+i}}) \tag{A.43}$$

Rearranging the equation we finally obtain:

$$C_{gg} = \frac{C_{ox}}{n}(n - \frac{1}{\sqrt{1+i}}) \tag{A.44}$$

Appendix B

B.1 Comparison of the phase noise performance of a all-nMOS LC VCO and of a complementary LC VCO

To compare the performance of the all-nMOS LC VCO (Fig.B.1(a)) and the complementary LC VCO (Fig.B.1(b)) we consider that the bias current I_{bias} of both structures are identical, that the equivalent transconductance G_m of each one are equal. We also fix the tank inductance equal to L in both cases. Finally the ISF function Γ has supposed equal in both cases.

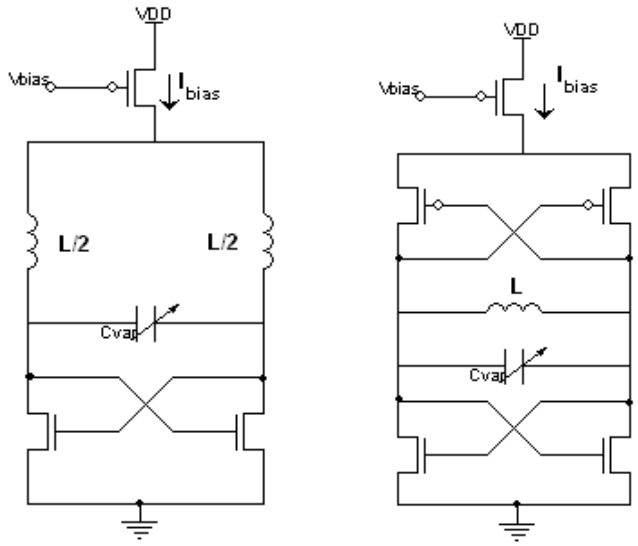
We will study some parameters of each circuit to show quantitatively that the phase noise is worse in the all-nMOS topology that in the complementary one.

All-nMOS structure

For Eq.2.25, the tank amplitude is:

$$V_{tank} = I_{bias} R_{L/2} = \frac{I_{bias} R}{2} \tag{B.1}$$

where $R_{L/2}$ is the resistance of each inductor L/2, which we made equal to a resistance R/2.



(a) Cross-coupled all-nMOS LC VCO (b) Cross-coupled differential LC VCO

Figure B.1: Comparison of phase noise performance of a all-nMOS and a differential LC VCO

As q_{max} (see Eq.3.12) is proportional to the tank voltage:

$$q_{max} \propto \frac{I_{bias}R}{2} \tag{B.2}$$

If G_m is the total transconductance, the transconductance of each nMOS transistor is $g_m = 2G_m$.

Also in this structure the total differential white noise power due to the transistors is (see Eq.3.24):

$$\overline{i_{tot}^2} = \frac{\overline{i_n^2}}{2} = 2kT\gamma(2G_m) = 4kT\gamma G_m \tag{B.3}$$

with k the Boltzmann constant, T the absolute temperature.

Re-writing the Eq.3.19 of Chap.3:

$$\mathcal{L}(\Delta\omega) = 10 \cdot log\Big(\frac{\frac{\overline{i_n^2}}{\Delta f}\Gamma_{rms}^2}{2q_{max}^2\Delta\omega^2}\Big) \tag{B.4}$$

the phase noise is

$$\mathcal{L}_{allnMOS} \propto \frac{\overline{i_n^2}}{q_{max}^2} = (4kT\gamma G_m)(R^2/4) = 16kT\gamma G_m R^2 = \mathcal{L} \tag{B.5}$$

Complementary structure

In this case the tank amplitude is:

$$V_{tank} = I_{bias}R_L = I_{bias}R \tag{B.6}$$

Here the resistance is the double than in the all-nMOS case.

q_{max} is:

$$q_{max} \propto I_{bias}R \tag{B.7}$$

Total differential white noise power due to the four transistors is:

$$\overline{i_{tot}^2} = \frac{\overline{i_n^2} + \overline{i_p^2}}{2} = 4kT\gamma G_m \tag{B.8}$$

Then the phase noise is

$$\mathcal{L}_{comp} \propto \frac{\overline{i_n^2 + i_p^2}}{q_{max}^2} = \frac{4kT\gamma G_m}{R^2} = 4\mathcal{L} \tag{B.9}$$

Therefore the complementary structure has approximately four times less phase noise that the all-nMOS one. What makes the difference is the higher value of q_{max} in the complementary structure than in the all-nMOS one (see [72]).

This discussion can be seen from another point of view: instead of comparing

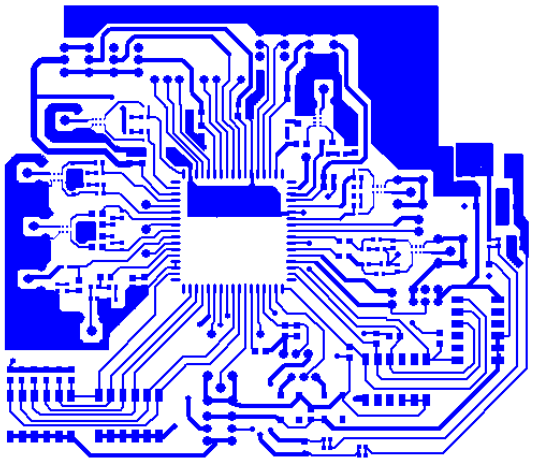
both circuits with an equal bias current, we can vary the current until both circuits have the same phase noise. It can be seen that the current of the all-nMOS structure has to be two times higher than the complementary structure.

Appendix C

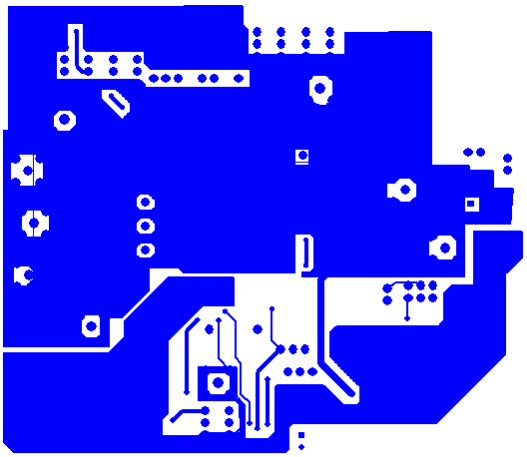
C.1 Layout of the PCB

A PCB has been fabricated to test the designed VCO, among other circuits. The top and bottom layers are depicted in Figs.C.1(a) and C.1(b). We have used decoupling ceramic capacitors of 100pF and 100nF between ground (GND) and all the supply pads (VDD). We use a ground plane to minimize the path of the signal. At the point of the external supply connection we also put a tantalum capacitor of 10mF. To fix as much as possible the various "virtual ground" of the circuit (the sources of the two cross-coupled transistor blocks and the bias varactor point) we put capacitors of 100pF between them and ground.

The fabricated PCB is shown in Figs.C.2(a) and C.2(b) (top and down layers).

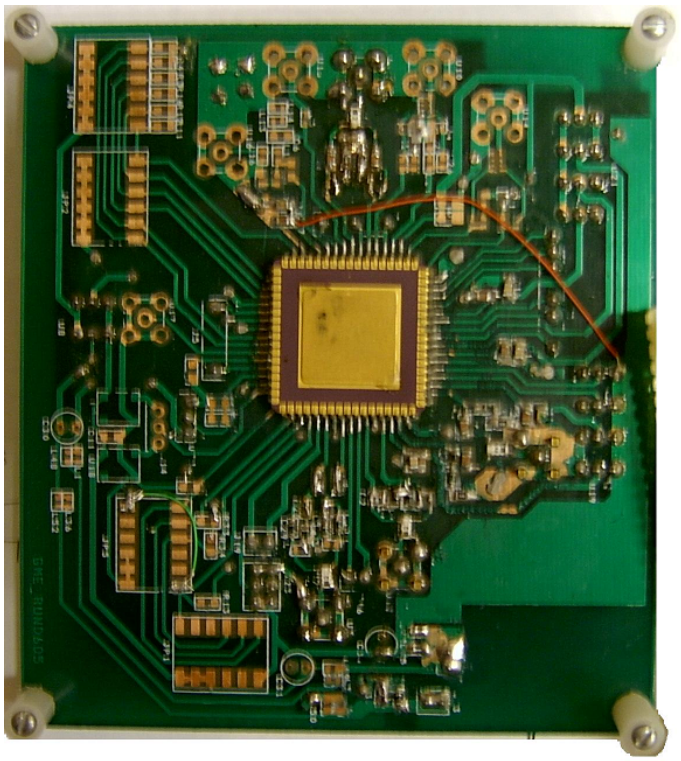


(a) Top of the PCB

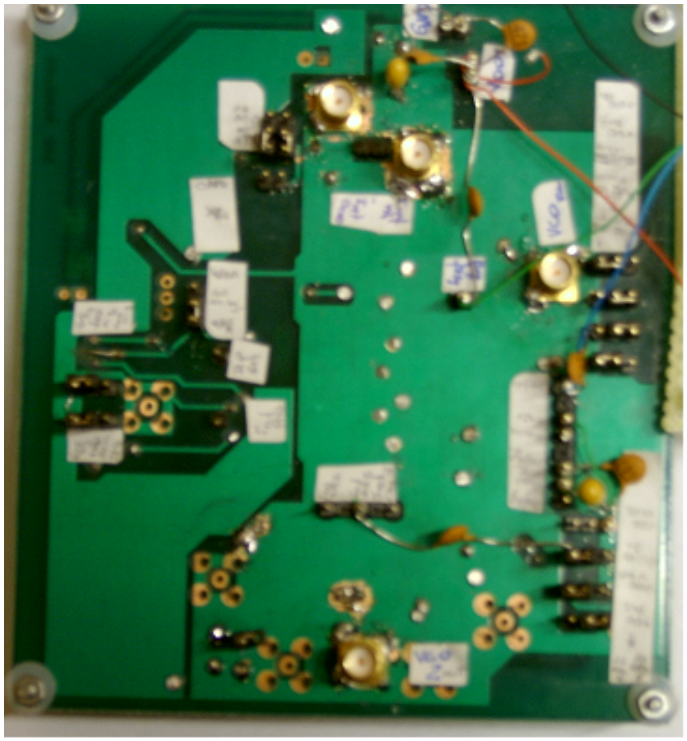


(b) Bottom of the PCB

Figure C.1: Layout of the PCB



(a) Photograph of the top layer of the final PCB



(b) Photograph of the down layer of the final PCB

Figure C.2: Final fabricated PCB

Bibliography

[1] S. Mohan, M. del Mar Hershenson, S. Boyd, and T. Lee, "Simple accurate expressions for planar spiral inductances," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 10, pp. 1419–1424, Oct. 1999.

[2] A. A. Abidi, "RF CMOS comes of age," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 4, pp. 549–561, Apr. 2004.

[3] E. Hegazi and A. A. Abidi, "A 17-mW transmitter and frequency synthesizer for 900-MHz gsm fully integrated in 0.35-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 5, pp. 782–792, May 2003.

[4] P. Quinlan, P. Crowley, M. Chanca, S. Hudson, B. Hunt, K. Mulvaney, G. Retz, C. E. OSullivan, and P. Walsh, "A multimode 0.3200-kb/s transceiver for the 433/868/915-MHz bands in 0.25-μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 12, pp. 2297–2310, Dec. 2004.

[5] E. Duvivier, G. Puccio, S. Cipriani, L. Carpineto, P. Cusinato, B. Bisanti, F. Galan, F. Chalet, F. Coppola, S. Cercelaru, N. Vallespin, J.-C. Jiguet, and G. Sirna, "A fully integrated zero-IF transceiver for GSM-GPRS quad-band application," *IEEE Journal of Solid-State Circuits*, vol. 39, no. 6, pp. 952–955, June 2004.

[6] J. A. Weldon, R. S. Narayanaswami, J. C. Rudell, L. Lin, M. Otsuka, S. Dedieu, L. Tee, K.-C. Tsai, C.-W. Lee, and P. R. Gray, "A 1.75-GHz highly integrated narrow-band CMOS transmitter with harmonic-rejection mixers," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 2003 – 2015, Dec. 2001.

[7] Y. Wu and V. Aparin, "A monolithic low phase noise 1.7ghz CMOS VCO for zero-IF cellular CDMA receivers," *IEEE International Solid-State Circuits Conference*, vol. XVII, pp. 396 – 397, Feb. 2004.

[8] C. Guo, C.-W. Lo, Y.-W. Choi, I. Hsu, T. Kan, D. Leung, A. Chan, and H. C. Luong, "A fully integrated 900-MHz CMOS wireless receiver with on-chip RF and IF filters and 79-dB image rejection," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 8, pp. 1084–1089, Aug. 2002.

[9] H. Darabi, S. Khorram, H.-M. Chien, M.-A. Pan, S. Wu, S. Moloudi, J. C. Leete, J. J. Rael, M. Syed, R. Lee, B. Ibrahim, M. Rofougaran, and A. Rofougaran, "A 2.4-GHz CMOS transceiver for Bluetooth," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 2016 – 2024, Dec. 2001.

[10] T. Lee, "CMOS RF:(still) no longer an oximoron," *IEEE Radio Frequency Integrated Circuits Symposium*, pp. 3–6, 1999.

[11] "802.15.4," IEEE, The Institute of Electrical and Electronics Engineers, Inc. 3 Park Avenue, New York, NY 10016-5997, USA, (http://standards.ieee.org/, Standard, Oct. 2003.

[12] A.-S. Porret, T. Melly, D. Python, C. C. Enz, and E. A. Vittoz, "An ultralow -power UHF transceiver integrated in a standard digital CMOS process: Arquitecture and receiver," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 3, pp. 452–464, Mar. 2001.

[13] P. Andreani and S. Mattisson, "A 2.4GHz monolithic VCO based on an MOS varactor," *Proccedings ISCAS'99*, vol. II, pp. 557–560, May-June 1999.

[14] J. Maget, M. Tiebout, and R. Kraus, "Influence of novel MOS varactors on the performance of a fully integrated UMTS VCO in standard $0.25 - \mu m$ CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 7, pp. 953–958, July 2002.

[15] J. Craninckx and M. S. J. Steyaert, "A 1.8 GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 5, pp. 736–744, May 1997.

[16] T. H. Teo, Y. Choi, H. Liao, Y.-S. Xiong, and J. S. Fu, "Characterization of symmetrical spiral inductor in 0.35μm cmos technology for RF appliction," *Solid-State Electronics*, vol. 48, pp. 1643–1650, Apr. 2004.

[17] A. Jerng and C. G. Soldini, "The impact of device type and sizing of phase noise mechanisms," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 2, pp. 360–369, Feb. 2005.

[18] B. D. Muer, M. Borremans, M. Steyaert, and G. L. Puma, "A 2-GHz low-phase-noise integrated LC-VCO set with flicker-noise upconvertion minimization," *IEEE Journal of Solid-State Circuits*, vol. 7, no. 35, pp. 1034–1038, July 2000.

[19] F. Svelto, S. Deantoni, and R. Castello, "A 1.3ghz low-phase noise fully tunablo CMOS LC VCO," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 356–361, Mar. 2000.

[20] D. Ham and A. Hajimiri, "Concepts and methods in optimization of integrated LC VCOs," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 6, pp. 896–909, June 2001.

[21] A. Hajimiri and T. H. Lee, "Design issues in CMOS differential LC oscillators," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 717–724, May 1999.

[22] J. Burghartz, D. Eldestein, M. Soyuer, H. Ainspan, and K. Jenkins, "RF circuit design aspects of spiral inductors on silicon," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 12, pp. 2028–2034, Dec. 1998.

[23] N. Nguyen and R. Meyer, "Si IC-compatible inductors and LC passive filters," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 4, pp. 1028–1031, 1990.

[24] A. M. Niknejad and R. G. Meyer, "Analysis, design, and optimization of spiral inductors and transformers for Si RF ICs," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1470–1481, Oct. 1998.

[25] F. Silveira, D. Flandre, and P. G. A. Jespers, "A gm/id based methodology for the design of CMOS analog circuis and its applications to the synthesis of a silicon-on-insulator micropower OTA," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, Sept. 1996.

[26] A. I. A. Cuhna, M. C. Schneider, and C. Galup-Montoro, "An MOS transistor model for analog circuit design," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 10, pp. 1510–1519, Oct. 1998.

[27] C.-M. Hung and K. K. O, "A packaged 1.1-GHz CMOS VCO with phase noise of -126 dBc/Hz at a 600-kHz offset," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 1, pp. 100–103, Jan. 2000.

[28] S. Tadjpour, E. Cijvat, E. Hegazi, and A. A. Abidi, "A 900-MHz dual-conversion low-IF GSM receiver in 0.35μm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 12, pp. 1992–2002, Dec. 2001.

[29] D. Leenaerts, J. van der Tang, and C. Vaucher, *Circuit Design for RF Transceivers*. Dordrecht, The Netherlands: Kluwer Academic Publishers, 2001, iSBN 0-7923-7551-3.

[30] N. M. Nguyen and R. G. Meyer, "Start-up and frequency stability in high-frequency oscillators," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 5, pp. 810–820, May 1992.

[31] R. L. Bunch, "A fully monolothic 2.5GHz LC voltage controlled oscillator in 0.35μm CMOS technology," Master Thesis, Virginia Polytechnic Institute and State University, Blacksburg,Virginia, Apr. 2001.

[32] T. Lee and A. Hajimiri, "Oscillator phase noise: a tutorial," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 326–336, Mar. 2000.

[33] C. Galup-Montoro, M. C. Schneider, and A. I. A. Cuhna, *Low-Voltage/Low-Power Integrated Circuits and Systems*, ieee press ed. E.Sanchez-Sinencio and A. Andreou, 1999, ch. A Current-based MOSFET Model for Integrated Circuit Design, pp. 7–55.

[34] T. Manku, "Microwave CMOS- device physics and design," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 3, pp. 277–285, Mar. 1999.

[35] Y.P.Tsividis, *Operation and Modelling of the MOS Transistor*, 2nd ed. Oxford University Press, 2000.

[36] C. Enz, F.Krummenacher, and E. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integrated Circuits and Signal Processing*, vol. 8, pp. 83–114, 1995.

[37] C. Vaucher, *Architectures for RF Frequency Synthesizers*, ser. Analog Circuit and Signal Processing. Dordrecht: Kluwer Academic Publishers, 2002, iSBN: 1-4020-7120-5.

[38] A. J.Rael, "Physical processes of phase noise in differential lc oscillators," *IEEE 2000 Custom integrated circuit conference*, pp. 569–571, 2000.

[39] A. Hajimiri, *Trade Offs in Analog Cirtuit Design: the Designer's Companion.* Printed in Netherlands: Kluwer Academic Publishers, 2002, ch. Trade offs in Oscillator Phase Noise, pp. 551–589, tomazou et al. (eds).

[40] H. W.Johnson and M. Graham, *High-Speed Digital Design: a Handbook of Black Magic.* New Jersey: Prentice Hall, 1993.

[41] J. Gerrits(CSEM) and D. G. Microelectronics), "RF CMOS IC design guidelines," CSEM," Design Guidelines, Feb. 2001.

[42] A. Arnaud and C. Galup-Montoro, "A compact model for flicker noise in MOS transistors for analog circuit design," *IEEE Transactions on Electron Devices*, vol. 50, no. 8, pp. 1815–1818, Aug. 2003.

[43] "Matlab," software program, 2005, www.mathworks.com.

[44] A. Pun, T. Yeung, J. Lau, F. Clément, and D. Su, "Substrate noise coupling though planar spiral inductor," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 6, pp. 877–884, June 1998.

[45] T. Blalack, Y. Lecklercq, and P. Yue, "On-chip RF isolation techniques," $http : //www.techonine.com/community/ed_resource/feature_article/21590$, Jan. 2003, searched:25/03/05.

[46] A. Hajimiri, "A general theory of phase noise in electrical oscillators," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 2, pp. 179–194, Feb. 1998.

[47] D. Leeson, "A simple model of feedback oscillator noise spectrum," *Proceedings of the IEEE*, vol. 54, pp. 329–330, Feb. 1966.

[48] L. Dai and R. Harjani, *Design of High-Performance CMOS Voltage Controlled Oscillators*, ser. analog circuit and signal processing. Boston: Kluwer academic publishers, 2003, iSBN: 1-4020-7238-4.

[49] A.A.Abidi, "High frequency noise measuremens on FET's with small dimensions," *IEEE Transactions on Electron Devices*, vol. ED-33, no. 11, pp. 1801–1805, Nov. 1986.

[50] A. Hajimiri and T. Lee, "Phase noise in differential LC oscillators," *Symposium on VLSl Circuits Digest of Technical Papers*, no. 5.1, pp. 48–51, 1998.

[51] A. Arnaud and C. G. Montoro, "Consistent noise models for analysis and design of cmos circuits," *IEEE Transactions on Circuits and Systems—Part I: Fundamental Theory and Applications*, vol. 51, no. 10, pp. 1909–1915, Oct. 2004.

[52] P. Kinget, *Analog Circuit Design*. Kluwer, 1999, ch. Integrated GHz Voltage Controlled Oscillators, pp. 353–381.

[53] A. M. Niknejad, "Analyis of Si inductors and transformers for IC's(ASITIC)," 2000, http://rfic.eecs.berkeley.edu/ niknejad/asitic.html.

[54] J. R.Long and M. A. Copeland, "The modeling, characterization and design of monolithic inductors for silicon RF IC's," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 3, pp. 357–369, Mar. 1997.

[55] Y. K. Koutsoyannopoulos and Y. Papananos, "Systematic analysis and modeling of integrated inductors and transformers in RF IC design," *IEEE Transactions on Circuits and Systems—Part II: Analog and Digital Signal Processing*, vol. 47, no. 8, pp. 699–713, Aug. 2000.

[56] P. Yue and S. Wong, "Design strategy on on-chip inductors for highly integrated RF systems," *DAC*, 1999.

[57] P. Yue, C. Ryu, JackLau, T. Lee, and S. Wong, "A physical model for planar spiral inductors on silicon," *1996 International Electron Devices Meeting Technical Digest*, pp. 155–158, Dec. 1996.

[58] P. Yue and S. Wong, "Physical modelling of spiral inductor on silicon," *IEEE Transactions on Electron Devices*, vol. 47, no. 3, pp. 560–568, Mar. 2000.

[59] H. M. Greenhouse, "Design of planar rectangular microelectronic inductors," *IEEE Transactions on Parts, Hybrids and Packaging*, vol. 10, no. 2, pp. 101–109, June 1974.

[60] H. A. Wheeler, "Simple inductance formulas for radio coils," *Proceedings IRE*, vol. 16, no. 10, pp. 1398–1400, Oct. 1928.

[61] "Cadence," 2005, www.cadence.com.

[62] C. P. Group and MIT, "Fasthenry," http://rleweb.mit.edu/vlsi/codes.htm.

[63] F.Svelto, S.Manzini, and R. Castello, "A three terminal varactor for RF IC's in Standard CMOS technologies," *IEEE Transactions on Electron Devices*, vol. 47, no. 4, pp. 893–895, Apr. 2000.

[64] A. Kiranas and Y. Papanaos, "Design issues towards the integration of passive components in silicon RF VCOs," -, vol. -, no. -, pp. 311–314, - 1998.

[65] P. Andreani and S. Mattison, "On the use of MOS varactors in RF VCO's," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 6, pp. 905–910, June 2000.

[66] R. L. Bunch and S. Raman, "Large-signal analysis of MOS Varactors in CMOS -G_m LC VCOs," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 8, pp. 1325–1332, Aug. 2003.

[67] D. Integrated, "Smash 5.2.2," *http* : *//www.dolphin* − *integration.com/medal/smash/smash*$_o$*verview.html*, 2004.

[68] S.-M. Yim, T. Chen, and K. K.O, "The effect of a ground shield on the characteristics and performance of spiral inductors," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 2, pp. 237–244, Feb. 2002.

[69] L. Barboni, R.Fiorelli, and F.Silveira, "Low power rf design blocks in weak and moderate inversion," *XI Iberchip Workshop, Baha, Brasl*, Mar 2005.

[70] ——, "Design and power optimization of cmos rf blocks operating in the moderate inversion region," *Proceedings of the 18th annual Symposium on Integrated Circuits and System Design, SBCCI, Florianolis, Brazil*, vol. I, pp. 15–20, Sept 2005.

[71] ——, "A tool for design exploration and power optimization of cmos rf circuit blocks," May 2006, work presented for evaluation for ISCAS 2006.

[72] R. Aparicio and A. Hajimiri, "A noise-shifting differential *c*olpitts VCO," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1728–1736, Dec. 2002.