CONSISTENT MODEL FOR DRAIN CURRENT MISMATCH IN MOSFETS USING THE CARRIER NUMBER FLUCTUATION THEORY

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ABSTRACT

This paper presents a new approach for accurate MOS transistor matching calculation. Our model, which is based on an accurate physics-based MOSFET model, allows the assessment of mismatch from process parameters and is valid for any operating region. Experimental results taken on a test set of transistors implemented in a 1.2 μm CMOS technology corroborate the theoretical development of this work.

Index Terms – MOSFET, analog design, matching, compact models.

1. INTRODUCTION

It is widely recognized that the performance of most analog or even digital circuits is limited by MOS transistor matching [1-4]. The shrinkage of the dimensions of MOSFETs and the reduction in the supply voltage make matching limitations even more important to such an extent that several new studies have been published in recent years [5-8]. Existing mismatch models use either simple drain current models limited to a specific operating region [1, 2, 4, 7, 8] or complex expressions [6] like that of BSIM. In general, however, the applicability of dc current models to characterize mismatch is not questioned. It is widely accepted that matching can be modeled by the random variations in geometric, process and/or device parameters. The effect of the random parameters on the drain current is quantified using the dc model of the transistor. As pointed out in [7, 8] there is a fundamental flaw in this approach that results in inconsistent modeling of matching. In effect, mismatch models implicitly assume that the actual values of the lumped model parameters can be obtained integrating the position-dependent distributed models over the areas of the channel region of the device, e.g., for the threshold voltage V_T

$$V_T = \frac{1}{WL} \iint_{channel-area} V_T(x,y)\,dxdy \qquad (1)$$

where W and L are the width and the length of the transistor, respectively.

As analyzed in [7, 8], the application of (1) to series or parallel association of transistors leads to an inconsistent model of matching owing to the nonlinear nature of MOSFETs. Consequently, the simple consideration of random fluctuations in the lumped parameters of the dc current model is not appropriate to develop matching models and new formulas must be derived from basic principles. Fortunately, the formalism needed to model matching is already available in low frequency (LF) noise modeling. In this paper, we will show that the carrier number fluctuation theory [9], employed to derive LF transistor noise, can be adapted to model current matching in MOSFETs. To obtain general results for all bias regions of the transistor we have used the Advanced Compact MOSFET (ACM) model, a physics-based one-equation all-region model [10].

2. THE ACM MODEL

According to ACM [10], the drain current in a long-channel transistor is given by,

$$I_D = \frac{\mu W}{nC'_{ox}}\left(-Q'_I + nC'_{ox}\phi_t\right)\frac{dQ'_I}{dx} \qquad (2)$$

where Q'_I is the inversion charge density, n is the slope factor, C'_{ox} is the oxide capacitance per unit area, μ is the effective mobility and ϕ_t is the thermal voltage.

The other specificity of the ACM model is the use of the unified charge control model (UCCM) [12] to link the carrier charge density with the applied voltages

$$V_P - V_X = \phi_t\left[\frac{Q'_I}{Q'_{IP}} - 1 + \ln\left(\frac{Q'_I}{Q'_{IP}}\right)\right] \qquad (3)$$

where $Q'_{IP} = -nC'_{ox}\phi_t$, $V_P = (V_{GB}-V_T)/n$ is the pinch-off voltage, and V_X is the channel potential. As shown in [13] the use of (2) in conjunction with (UCCM) (3) gives

$$I_D = -\mu\frac{W}{dx}Q'_I\,dV_X \ . \qquad (4)$$

Consequently, the ACM model is fully consistent with the quasi-Fermi potential formulation for the drain current [11].

3. CONSISTENT SMALL-SIGNAL MODEL OF THE MOSFET CHANNEL

To calculate the effect of the fluctuations on the drain current along the channel, we split the transistor into 3 series elements: the upper transistor, the lower transistor, and a small channel element of length Δx and area $\Delta A = W\Delta x$ (Fig. 1(a)).

Small-signal analysis allows one to calculate the effect of the local current fluctuation ($i_{\Delta A}$) on the drain current (ΔI_d), as shown in Fig. 1(b). The current division between the channel element and the equivalent small-signal resistance of the rest of the channel gives $\Delta I_d = (\Delta x/L)i_{\Delta A}$. This very simple result for the current division, proportional to a geometric ratio, is a consequence of the quasi-Fermi potential formulation for the drain current, i.e., the conductance of the channel element and the transconductances of the upper and lower transistors are

proportional to the local charge density. Thus, the square of the total drain current fluctuation is

$$(\Delta I_D)^2 = \sum_L (\Delta I_d)^2 = \lim_{\Delta x \to 0} \sum \left[(\Delta x / L) i_{\Delta A} \right]^2 = \frac{1}{L^2} \int_0^L \left[\Delta x (i_{\Delta A})^2 \right] dx \,. \quad (5)$$

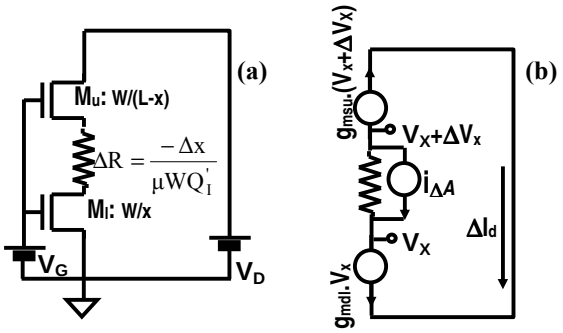

Fig. 1. Splitting of a transistor into three series elements (a) Transistor equivalent circuit (b) Small-signal equivalent circuit

4. NUMBER FLUCTUATION MISMATCH MODEL

The relationship between local fluctuation of the inversion charge density and the local current fluctuation that follows from expression (4) is

$$i_{\Delta A} = I_D \frac{\Delta Q_I'}{Q_I'} \quad (6)$$

where $\Delta Q'_I$ is the fluctuation of the inversion charge density in the channel element of area ΔA. For the sake of simplicity we will consider fluctuation in the number of carriers only, but the analysis can also be extended to include mobility fluctuation for the computation of the local current fluctuation.

From UCCM (3), one can readily derive the relation between local charge density and threshold voltage fluctuations

$$\Delta Q_I' = -C_{ox}' \frac{Q_I'}{Q_I' - nC_{ox}'\phi_t} \Delta V_T \,. \quad (7)$$

The local fluctuation of the threshold voltage ΔV_T is calculated from the conventional expression for the standard deviation [2]

$$\overline{\Delta V_T^2} = \sigma_{VT}^2 = \frac{A_{VT}^2}{W \Delta x} \,. \quad (8)$$

Using (6), (7), and (8) we calculate $(i_{\Delta A})^2$ and obtain the expression of $\overline{\Delta I_D^2}$ inserting this resultant into (5). With the aid of (2) the integration over the channel length in (5) is changed to the integration over the channel charge density given by

$$\sigma_{I_D}^2 = \overline{\Delta I_D{}^2} = \frac{\mu C_{ox}' I_D A_{VT}^2}{nL^2} \int_{Q_{IS}'}^{Q_{ID}'} \frac{1}{nC_{OX}'\phi_t - Q_I'} dQ_I' \,. \quad (9)$$

Assuming, as in [14], Poisson statistics for the depletion charge fluctuations, then

$$A_{VT}^2 = \frac{q^2}{C_{ox}'^2} (N.x_D) = \frac{q^2}{C_{ox}'^2} N_{oi} \quad (10)$$

where N is the average number of impurities per unit volume in the depletion region, x_D is the depletion deep, and $N_{oi}=Nx_D$ is the effective number of impurities per unit area.

Finally, using (10) and integrating (9) from source to drain results

$$\frac{\sigma_{I_D}^2}{I_D^2} = \frac{q^2 N_{oi} \mu}{L^2 n C_{ox}' I_D} \ln\left(\frac{nC_{ox}'\phi_t - Q_{IS}'}{nC_{ox}'\phi_t - Q_{ID}'} \right) \,. \quad (11)$$

The result in (11) is essentially the same as that derived for flicker noise in MOS transistors in [13]. This is because mismatch is a "dc noise" and the physical origin of both mismatch and flicker noise is fluctuation of either fixed charges or localized states along the channel.

5. MISMATCH MODEL IN TERMS OF INVERSION LEVELS

A useful alternative expression for (11) is obtained if the charge densities at source and drain are expressed in terms of the normalized forward and reverse currents i_f and i_r. In the ACM model [10], the drain current is expressed as the difference between forward (I_F) and reverse (I_R) components

$$I_D = I_F - I_R = I(V_G, V_S) - I(V_G, V_D) = I_S (i_f - i_r) \quad (12)$$

where $I_S = \frac{1}{2}\mu C'_{ox}\, n\phi_t^2 (W/L)$ is the specific current, which is proportional to the geometric ratio W/L of the transistor. V_G, V_S, and V_D are the gate, source, and drain voltages, respectively. i_f and i_r are the normalized forward and reverse currents or inversion levels at source and drain, respectively. Note that in the saturation region, the drain current is almost independent of V_D; therefore, $i_f >> i_r$ and $I_D \cong I_F$. On the other hand, if V_{DS} is low, then $i_f \cong i_r$. Using the relationship between inversion charge densities and currents [10], expression (11) can be rewritten as

$$\frac{\sigma_{I_D}^2}{I_D^2} = \frac{N_{oi}}{WLN^{*2}} \frac{1}{i_f - i_r} \ln\left(\frac{1 + i_f}{1 + i_r} \right) \quad (13)$$

where we define N^* as in [13, 15]

$$N^* = \frac{-Q_{IP}'}{q} = \frac{nC_{ox}'\phi_t}{q} \,. \quad (14)$$

From weak to strong inversion in the linear region, $i_f \cong i_r$ and (13) reduces to

$$\frac{\sigma_{I_D}^2}{I_D^2} = \frac{N_{oi}}{WLN^{*2}} \frac{1}{1 + i_f} \,. \quad (15)$$

In weak inversion, $i_f << 1$; thus, the first order series expansion of (13) leads to

$$\frac{\sigma_{I_D}^2}{I_D^2} = \frac{N_{oi}}{WLN^{*2}} \quad (16)$$

for either saturation or nonsaturation.

In saturation ($i_r \to 0$), expression (13) can be written as

$$\frac{\sigma_{I_D}^2}{I_D^2} = \frac{N_{oi}}{WLN^{*2}} \frac{\ln(1 + i_f)}{i_f} \,. \quad (17)$$

In weak inversion, $i_f << 1$ and (17) is almost insensitive to the current. In strong inversion, the normalized mismatch given by (17) reduces to the conventional expression if the logarithmic term is assumed to be constant.

Finally, the random errors due to edge effects can be modeled as in [1] resulting in a complete mismatch model

$$\frac{\sigma^2_{I_D}}{I_D^2} = \frac{1}{WL}\left[\frac{N_{oi}}{N^{*2}}\frac{1}{i_f - i_r}\ln\left(\frac{1+i_f}{1+i_r}\right) + \frac{B_L}{L} + \frac{B_W}{W}\right] \quad (18)$$

where B_L and B_W are the channel length and width mismatch factors due to edge effects.

6. MEASUREMENTS

Current mismatch of 24 NMOS 30µm x 1.2µm transistors was measured on a test circuit in the ES2 1.2µm CMOS DLM process, using the circuit shown in figure 2. M_{REF} was kept the same for all measurements while the remaining 23 transistors were used as M_i for data acquisition.

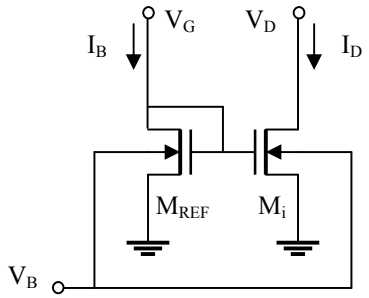

Fig. 2. Test circuit: M_{REF} is the reference transistor while M_i is the transistor under test. I_B (V_B, V_D) is a current (voltage) source.

Figure 3 presents the mismatch power normalized to the dc power ($SD^2(I_D)/I_D^2$) for drain-to-source voltage ranging from 20mV (linear region) to 1V (saturation), for different inversion levels. Simulated curves (dotted lines) have been determined from expression (13), with i_r calculated through ACM long channel model expressions [10]. The average number of impurities per unit area (N_{oi}) is estimated as 6.1×10^{12} cm^{-2}; the resulting A_{VT} calculated from (10) is about 29mV-µm. Specific current (I_S) for the devices under test is 1.2µA. It should be emphasized that drain current mismatch results from geometrical and technological fluctuations; however, for most of the cases, the dominant factor that affects current mismatch can be associated with V_T mismatch.

In weak inversion (i_f = 0.01 and 0.1), mismatch is constant from linear to saturation region and independent of the inversion level, as predicted by (16). For i_f = 1, mismatch is approximately one half of the value measured for very weak inversion, as predicted in (15). For higher inversion levels (i_f = 10 and 100) and operation in the linear region, mismatch reduces by a factor of approximately $1/(1+i_f)$, compared to weak inversion. This value increases up to a plateau when saturation is reached, presenting a good agreement with expression (17) of our model.

At this point one should compare our mismatch model with Pelgrom's model [2]. If we were to use Pelgrom's mismatch model together with the ACM model, the expression for the normalized mismatch power would be

$$\frac{\sigma^2_{I_D}}{I_D^2} = \frac{N_{oi}}{WLN^{*2}}\left(\frac{2}{1+\sqrt{1+i_f}}\right)^2 \quad (19)$$

where the dependence on i_f is that of $(g_m/I_D)^2$. Expressions (17) and (19) agree in weak inversion ($i_f << 1$), but for i_f=1000 (17) predicts a value 80% greater than (19). Explanation for this difference, arises from the distributed nature of the MOSFET. While Pelgrom's model assumes a lumped V_T for the MOSFET, our model assumes a distributed V_T along the channel. As a consequence, for strong inversion and saturation, the part of the channel closer to the drain plays a less important role in the charge fluctuation along the channel than the part of the channel closer to the source.

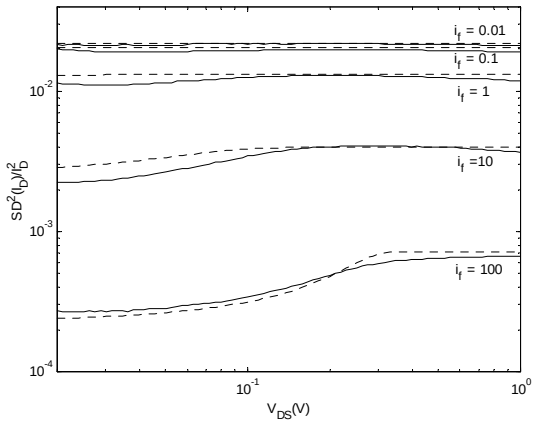

Fig. 3. Normalized current mismatch power. Bulk was kept on zero voltage. (Measurements: —; simulation: ---.)

Figure 4 shows the measured and simulated dependence of current matching on inversion level for linear (V_{DS}=50mV) and saturation (V_{DS}=1V) regions. For this measurement, transistors were paired in series for reduction of short channel effects, resulting in 12 transistor pairs per die, with 30µm x 2.4µm equivalent dimensions. N_{oi} was estimated as 7.6×10^{12} cm^{-2}, resulting in A_{VT} of 32mV-µm. In agreement with our model, measurements show that matching is identical for either linear or saturated conditions under weak inversion. For inversion levels greater than one, mismatch decreases with inversion level more intensively for linear than for saturated condition. As can be seen, expression (13) describes current mismatch accurately for any inversion condition. In the bias range from 10µA to 100µA mismatch seems to increase for the linear region. This behavior is attributed to an effective reduction of the drain-to-source voltage due to voltage drops in contact and diffusion resistances.

It is well know that bulk voltage also affects matching of MOS transistors [4]. Figure 5 shows relative mismatch for different values of bulk voltage for saturation (V_{DS}=1V). Transistors were paired in series for reduction of short channel effects. In this case, one can suppose that N_{oi} is modulated by V_{GB}. So, when bulk is more reverse biased, effective number of impurities per unit area increases under the gate, thus making N_{oi} higher. It is clear in this figure that the greater the reverse bulk voltage, the greater the mismatch. As can be observed in Fig. 5, a forward-biased bulk improves matching. When the bulk is forward biased at 0.3V, an apparent reduction of mismatch occurs for bias current lower than 10nA. Such behavior is

attributed to the action of the parasitic lateral bipolar transistor. The solid lines in figure 5 represent expression (13). Different values of N_{oi} were chosen to fit the mismatch characteristics in weak inversion.

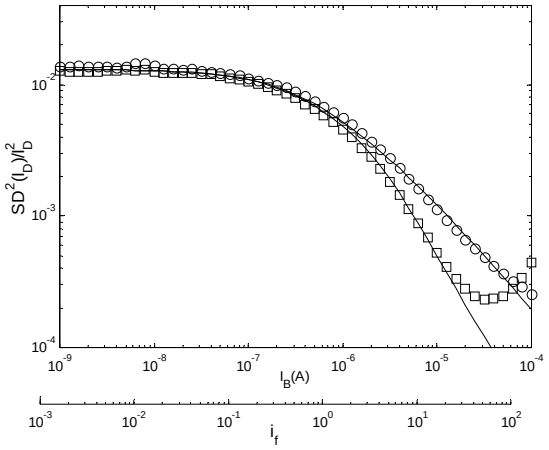

Fig. 4. Dependence of measured current matching on inversion level for linear (□ - V_{DS}=50mV) and saturation (○ - V_{DS}=1V) regions. Bulk was kept at zero volt. Solid lines show theoretical expression (13).

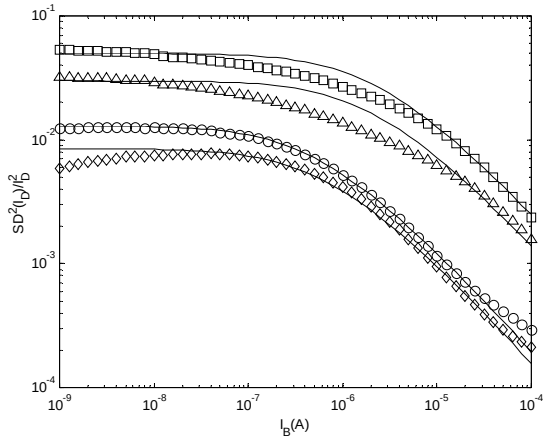

Fig. 5. Dependence of mismatch on bulk-to-source voltage in saturation (V_{DS}=*1V*). □ = -1.8V; △ = -1.2V; ○ = 0V; ◇ =+0.3V. Solid lines represent expression (13).

7. CONCLUSIONS

A mismatch model for the MOS transistor, continuous in all operation regions, has been developed. A physics based approach, based on fluctuation of carrier number, was used to integrate all the contributions of small mismatch elements along the transistor channel. This approach along with the description of the dc characteristics of MOSFET's from the ACM model resulted in a compact easy-to-use formula for mismatch that covers any operating region. Results obtained are quite similar to those derived in [13] for *1/f* noise, since the physical mechanisms at the origin of both phenomena are similar. Experimental results confirmed the accuracy of our model under various bias conditions. It is expected that this work will help designers understand and predict transistor mismatch in an accurate and easy way.

ACKNOWLEDGMENT

The authors are grateful to CNPq and CAPES, Brazilian agencies for scientific development, for their financial support.

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