Design and Power Optimization of CMOS RF Blocks Operating in the Moderate Inversion Region

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ABSTRACT

In this work the design of radiofrequency CMOS circuit blocks in the 910MHz ISM band, while biasing the MOS transistor in the moderate inversion region, is analyzed. An amplifier design tool is presented. This tool shows that it exists an optimum in the power consumption for a given gain. Different technologies are compared, using the proposed tool, regarding its performance in terms of gain and power consumption in the design space I_D-g_m/I_D. The frequency limit of the applied transistor model is discussed and comparisons with simulations using BSIM3v3 are presented. Implementation of a power amplifier and a VCO at 910 MHz in 0.35µm CMOS technology and experimental results are also shown.

Categories and Subject Descriptors:

B.7.2 [**Integrated Circuits**]: Design Aids – *simulation.*

General Terms:

Design.

Keywords:

CMOS Integrated Circuits, Radio frequency Integrated Circuits, Amplifier Design, Power optimization

1. INTRODUCTION

Nowadays, the development of low-cost, low-power radiofrequency (RF) devices grows up rapidly, specifically in personal communication equipments and networks of sensors. This kind of communications is implemented using new standards, which are characterized by short range links (usually below 100m) and reduced power consumption (since the devices are powered from batteries).

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It is known that optimum power consumption of analog circuits can be reached in the moderate inversion region [1], where is obtained a good trade-off between a high g_m/I_D and a not too large transistor size and hence reduced parasitic capacitances values. Traditionally the operation at this optimum was restricted to low frequency applications, since the transconductance values required for operation at RF implied currents that, in order to operate in moderate inversion, lead to enormous transistor sizes. This big transistor would imply high parasitic capacitances that would jeopardize the advantage of an increased g_m/I_D ratio in moderate inversion. However, what is "low" frequency and "high" frequency is technology dependent. Particularly, in current, deep sub micron technologies, the reduction of parasitic capacitances and the increase of the current drive by the increase of the gate oxide capacitance per unit area, make that RF frequencies are, in fact, "low" frequency. This idea, that this work exploits, has been also advanced in works such as [2]. In [3], this idea is applied in the design of RF low noise amplifiers. However, as far as we know, there is no published work, where a tool for analyzing the trade-offs and possible optimum solution has been presented.

In this work this improvement is applied to design power amplifiers and voltage controlled oscillators (VCO). It will be presented a software tool which can be used either to design amplifiers, obtaining an optimum design and showing the trade off between amplifier's gain and power consumption, or to evaluate the performance of a particular technology at a desired frequency. With this tool it has been checked the good performance of a 0.35µm technology at 910MHz and it has been designed a VCO and a power amplifier of 40V/V gain and 5.5mA current consumption.

2. MOS TRANSISTOR AND BUILDING BLOCK MODELING

2.1 Modeling approach

Firstly, the approach applied for modeling the MOS transistor in small signal operation and the amplifier building blocks is presented. The model used for the MOS transistor is the ACM model [4]. The basic amplifier structures considered are modeled by quadripoles, as it is shown in Fig.1, in order to represent different configurations and loads.

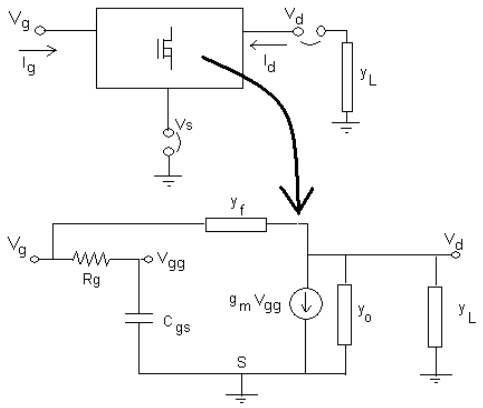

Figure 1: Transistor and basic block model

The two port relations of the quadripole in Fig. 1 can be written as:

$$i_d = y_{dd} v_{ds} + y_{dg} v_{gs}$$
$$i_g = y_{gd} v_{ds} + y_{gg} v_{gs} \quad (1)$$

Assuming that the MOS transistor operates in saturation and in the quasi-static regime:

$$y_{dd} = y_O + y_f$$
$$y_{dg} = \frac{g_m}{1 + j.2\pi.f.R_g C_{gs}} - y_f$$
$$y_{gd} = -y_f \quad (2)$$
$$y_{gg} = \frac{j.2\pi.f.C_{gs}}{1 + j.2\pi.f.R_g C_{gs}} + y_f$$

Where y_f and y_o are respectively the feedback and the output admittances, which include both parasitics of the transistor and external components, such as a drain - gate feedback resistor, as described in the next section. C_{gs} is the total gate-source capacitance equal to the sum of the gate-source and the gate-substrate capacitances, R_g is the gate resistance and f is the working frequency.

2.2 Transadmittance components

The transadmittances shown in eq.2 include both intrinsic capacitances (C_{db}, C_{gs}, C_{gb}, C_{sb}, C_{dg}) and extrinsic capacitances (gate - source and gate - drain overlap capacitances and drain - substrate and source - substrate junction capacitances). For the intrinsic capacitances, the medium frequency, five capacitor model, is deemed enough as discussed in the next section. It is interesting to note that the intrinsic capacitances C_{db} and C_{dg} have cero value, assuming the transistor in saturation.

Thus:

$$y_f = \frac{1}{R_F} + j.2.\pi.f.C_{ov}.W \quad (4)$$

where W is the transistor width, C_{ov} is the gate-drain overlap capacitance per channel width, and R_F is the drain - gate feedback resistor (some architectures have this in order to get better matching impedance and flatter frequency response at high frequency [2] [5]).

The intrinsic load is:

$$y_O = g_d + j.2.\pi.f.C_{db} \quad (5)$$

where g_d is the small signal output conductance and C_{db} is the extrinsic drain substrate parasitic capacitance given by:

$$C_{db} = X.W\,C_j + (W + 2X).C_{jsw} + W.C_{jswg} \quad (6)$$

where X is the length of the source and drain regions, C_j is the drain-substrate capacitance per area, C_{jsw} is the sidewall parasitic capacitance per unit width y C_{jswg} is the sidewall parasitic capacitance per unit width in the channel side of the drain area. The capacitances C_j, C_{jsw}, C_{jswg} are corrected as a function of the parameters MJSW (sidewall junction grading coefficient) and PB (junction potential) and the voltage applied to the junction [6].

The extrinsic load is:

$$y_L = \frac{1}{Z_{load}} + \left(gd + j.2.\pi.f.C_{db}\right)\Big|_{current\ \ source} \quad (7)$$

This expression is composed by the actual external load ($1/Z_{load}$) and the term $\left(gd + j.2.\pi.f.C_{db}\right)\Big|_{current\_source}$ models the impedance of the bias circuit (which is not shown in Fig.1).

The gate resistance R_g, is calculated as in [7] for a transistor with a non-interdigitized layout:

$$R_g \approx \frac{1}{3}\frac{W}{L} R_{SHEET} \quad (8)$$

Where L is the transistor length and R_{SHEET} is the gate resistance per square. With these expressions, the four transadmittances can be written as a set of equations suitable to work in MATLAB (eq.2). Finally, the gain of the stage A is given by:

$$A = \frac{v_{ds}}{v_{gs}} = \frac{-y_{dg}}{y_{dd} + y_L} \quad (9)$$

2.3 Non-quasistatic effects and model limit

The model that has been presented is a quasi-static model (QS), and is based on the hypothesis that the charge in the channel can reach the balance instantly after applying electrical stimulus. However, the limitation of the QS model is known at high frequency where the non-quasi-static effects (NQS) have influence. That is why it is important to have an estimation of the frequency which limits the zones of QS and NQS operation.

This limit has been fixed at $0.1 \cdot f_T$ (where f_T is the unitary gain frequency) as it is proposed in [7][8]:

$$f_{QS\max} \approx \frac{f_T}{10} = \frac{0.1\, g_m}{2\pi\left(C_{gs} + C_{gb} + C_{gd}\right)} \qquad (10)$$

Working below this limit assures also that is not necessary to use the complete model of the nine intrinsic capacitances and transcapacitances of the device [7].

Another effect that can limit the performance of the transistor MOS at high frequency is the carrier velocity saturation; an effect that is noticeable in very strong inversion. But, as in this work is shown that it is possible and convenient to work in moderate inversion, in the following this effect is not considered. In case of working in very strong inversion (gm/ID less than 3…4 1/V) it has to be taken into account that this can modify the results shown.

3. DESIGN SPACE EXPLORATION ALGORITHM

The proposed algorithm for designing RF amplifier blocks considers the design space defined by the DC bias current of the active transistor I_D and the g_m/I_D ratio of this transistor, parameters that define the transistor aspect ratio (W/L) [1]. The transistor length is taken constant equal to the minimum allowed by the technology in order to maximize the high frequency performance by decreasing parasitic capacitances. In this design space the current consumption was considered for a given voltage gain.

The algorithm is summarized as follows: the design space is covered by a grid of couples (I_D ,g_m/I_D). For each of these couples the gain A =A (I_D, g_m/I_D), width W =W (I_D, g_m/I_D) and quasi-static boundary B = B(I_D, g_m/I_D) are obtained.

Having explored this design space, as it is shown in the examples in the following sections, for a given gain, there is a g_m/I_D value that results in an optimum of consumption. This optimum lies in moderate inversion for usual gain values. The locus of the optima, which satisfies the following equation, was also determined analytically.

$$\frac{\partial A}{\partial\, g_m / I_D} = 0 \qquad (11)$$

Ongoing work on this algorithm adds the evaluation of the harmonic distortion of the stage, so that the design space can be limited to those areas that comply with a given distortion target.

4. RESULTS AND DISCUSSIONS

In the following examples, the maps of gain generated by the algorithm are shown and briefly explained.

4.1 Example #1

In this example, a one-stage amplifier with load capacitance C_L and a feedback resistance R_F is presented, as it is shown in Fig.2.

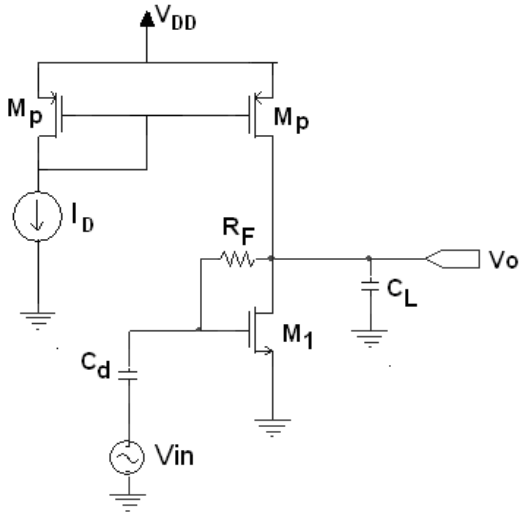

Figure 2: Circuit of the example 1

The a priori design values are: C_L=0.5pF, R_F =5kΩ,

W_{MP} =20μm, f_0 = 910MHz, $L_{MP,M1}$=0.35μm. In the first part of the example the gate resistance R_g is neglected. Later, it is studied the degradation of the previous results if the R_g corresponding to a non-interdigitized layout is considered.

Neglecting R_g and considering that the desired gain is 2V/V, the algorithm generates the gain curve of Fig.3 (circle markers), where the optimum is marked with an arrow. It is also shown the curve of optima (points of minimum consumption for a given gain, square markers); thus if it is desired to work optimally for a chosen current I_D, the gain and the g_m/I_D ratio (and therefore the transistor width) are fixed.

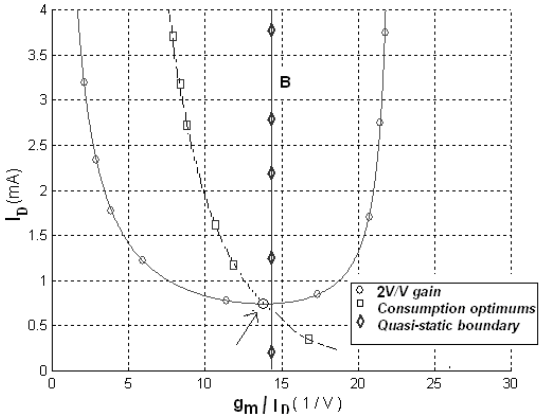

Figure 3: Result of example 1. Marked with circular markers is the 2V/V gain curve, with square markers is the optima of consumption and with rhomboid markers (B curve) is the quasi-static boundary @ 910MHz.

The last curve of this figure shows the quasi static boundary limit B for this technology (rhomboid markers), where, given a working frequency f_0, the maximum g_m/I_D is fixed independent of I_D. In the optimal point, for this example, the width of M_1 is 223um, I_D is 0.75mA, and g_m/I_D is almost 14.

The algorithm results have been contrasted with simulation results using BSIM3v3, and, as it is shown in Fig.4, a good correlation has been found.

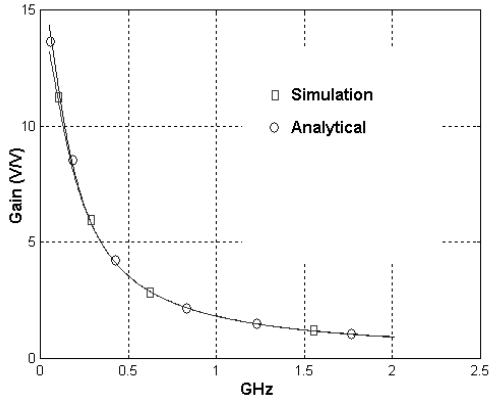

Figure 4: Frequency response calculated and simulated, neglecting Rg.

Now, as a way to show some of the potential of the proposed tool is terms of evaluating design trade-offs, it is studied how the gate resistance degrades the performance of the amplifier designed previously, if proper care is not taken at the layout. The algorithm adds $R_{geff}=R_g/3$, considering a non interdigitized layout for the transistor M1 [7], with a resistance per square of the gate material of 8.6k Ω/sq. It is clear than the new optimum occurs at a higher current consumption that the previous one (marked by an arrow in the figure). Despite the gate resistance effect is extensively known, it is interesting to see the effect on the consumption at a given gain. We can see this in the following figure:

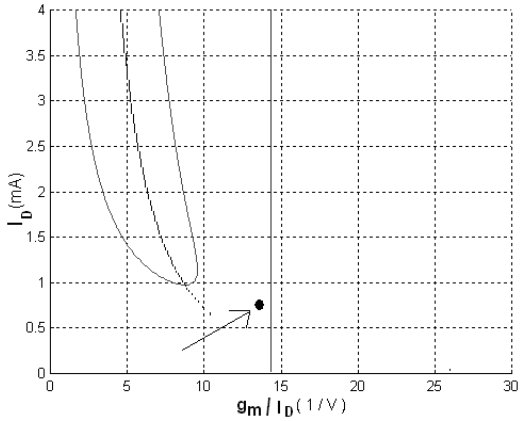

Figure 5: Gain curve of 2V/V of Example #1 when the effect of R_g of a non interdigitized layout is considered. The point marked by the arrow shows the location of the minimum consumption point determined in Fig. 3 for a negligible R_g.

4.2 Example #2

Using the architecture of Fig.2 with C_L=0.1pF, without R_F and assuming an ideal current source instead of M_p, 2V/V gain curves at 910 MHz for 0.35µm and 0.8µm technologies are obtained. Introducing the characteristics of each technology into the program, the curves of Fig. 6 are obtained.

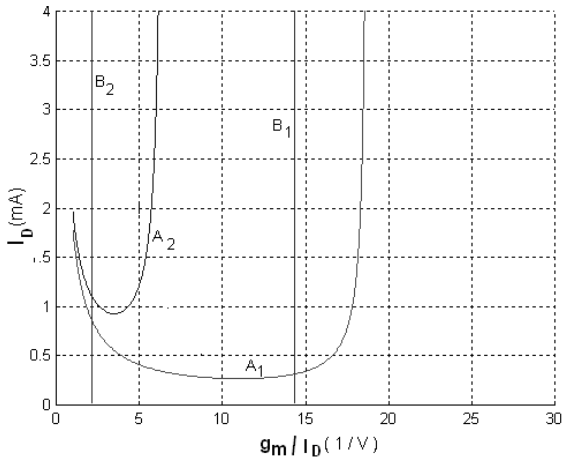

Figure 6: Comparison between 0.35µm (A1) and 0.8µm (A2) CMOS technologies for a 2V/V gain at 910MHz.

The quasi-static boundary for both technologies, working at 910MHz, are plotted (curves B1 for 0.35µm and B2 for 0.8µm). It is clearly possible to work in moderate inversion with the 0.35µm technology, and the optimum is reached in this region, while in 0.8µm it is only possible to work in strong inversion. What is more, the optimum for 0.35µm is reached with a current value 67% smaller than the one for 0.8µm. Furthermore, the optimum in the 0.8µm technology moves beyond the quasi-static boundary, meaning that the minimum required current is probably higher than the one estimated.

These advantages for a smaller feature size technology are known but our tool allows to quantify them and determine where is the actual limit for a given technology.

5. IMPLEMENTATION

Using the described methodology, the amplifier shown in Fig.7 has been designed.

The final design parameters are:

Table I: Data of the designed amplifier.

	M_1	M_2	M_3	M_P
W (um)	60	60	80	200
I_D (mA)	0.5	0.5	1.5	2.54

Current mirrors: Me_0, Me_1, Me_2: W=20µm Me_3: W=60µm

Drain inductance: L_D=3.3nH, Load: R_L=50Ω, Feedback DC bias: R1=R2=15 kΩ , C2=1pF

Series-shunt feedback: RF1=5 kΩ, RF2=15 kΩ, Supply voltage: 2.3V, Gain: 40V/V

Power given to the load R_L: 2dBm

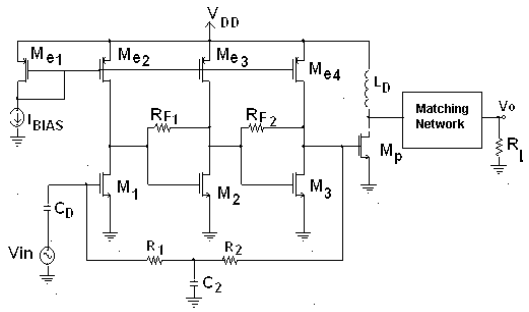

Figure 7: Amplifier implemented in 0.35µm technology with 40V/V gain at 910MHz.

6. MEASUREMENT RESULTS

A chip including this amplifier was fabricated. Unfortunately, a layout error was introduced during the final adjustments in the overall chip layout. This error made that the DC feedback, that sets the overall amplifier bias point, was non functional. In order to anyhow test the amplifier, the bias was set in open loop, which made it much more inaccurate and unstable.

Nevertheless, by testing several bias points and performing extensive simulations, it has been possible to select a bias point where it was possible to measure the performance of the circuit. In Fig.8 and in Table II are shown the results of the measurements, when V_{DD} is 2.3V, V_{bias} is 0.83V and I_D is 0.5mA

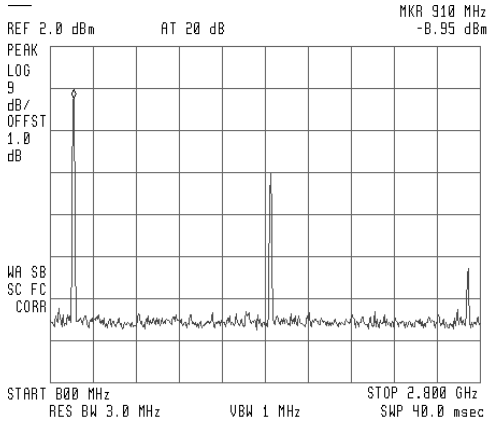

Figure 8: Power amplifier operation measurement.

Table II: Measured and simulated characteristics.

Characteristics	Measured	Simulation
I_{DD} (at 0 power delivered)	3.21 mA	3.22mA
P_{out} (*)	-8.9 dBm	-5.7 dBm
Harmonic Distortion:HD_2	-26.5 dB	-22.0 dB
Voltage gain	8.9 V/V	12.7 V/V

(*) P_{in} = -16.4 dBm (V_{in}=13.1mV) @ 910MHz, R_L=50Ω through a matching network.

These results do not show a perfect agreement between simulation or calculation and measurements. This is due to the described problem that did not allowed to precisely set the bias point for all the circuit stages, particularly the output one. Therefore, these results do not yet make it possible to fully confirm our predictions. However, it confirms operation of the preamplifier stages (M_1, M_2 and M_3 in Fig. 7) at 910MHz while biased in moderate inversion as calculated. New designs are currently under development and will be fabricated soon.

7. DESIGN OF A -GM LC VCO IN 0.35µM CMOS TECHNOLOGY

In this section it is considered the methodology and the design in CMOS standard technology of a –Gm LC VCO as it is shown in Fig.9 [9]. It has a central frequency of 910 MHz and integrated inductors [10].

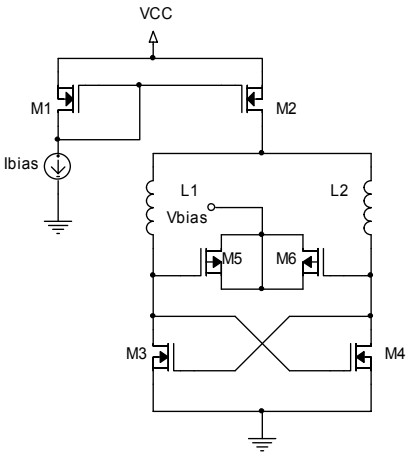

Figure 9: -Gm LC differential VCO

The VCO oscillation condition is given when

$$g_m = \alpha / R_L^{PAR} \quad (12)$$

where R_L^{PAR} is the inductor equivalent parallel resistance and α is the oscillation factor (its value is a design criterion, usually equal to 3) and g_m is the M_3 and M_4 transistors' transconductance. Therefore, given an inductance value L (that determines its associated R_L^{PAR} value according to the inductor implementation) and the oscillation factor α, g_m is obtained. As a consequence, an increment in g_m/I_D is equivalent to a drop in I_D. On the other hand, the minimum I_D value that is possible to be chosen is limited by the oscillator phase noise [11,12], because it increases when I_D drops. It is also limited by the parasitic capacitances of M_3 and M_4, because an increment in g_m/I_D is an increment in the width of those transistors, not being possible, in some cases, to reach the oscillation frequency, or leaving very diminished the tuning range.

Taking into account the previous discussion, the design methodology is the following: given the oscillation frequency and the inductor value L, the last is dimensioned and its parameters are found (parasitic equivalent capacitances and resistances and

its quality factor). The g_m/I_D ratio is determined from these parameters, α and $I_D=I_{bias}/2$. Using the transistor's characteristic curves, the inversion coefficient I, or equivalently the $I_D/(W/L)$ ratio, is obtained and from it, the width of the transistors M_3 and M_4. A brief scheme of the methodology is shown in Fig.10.

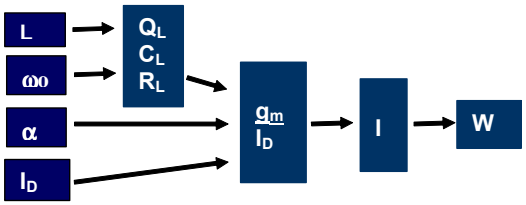

Figure 10: VCO –Gm LC design methodology

In this work the emphasis has been put in decreasing the consumption, working in moderate inversion (choosing a g_m/I_D value of 14), rather than optimizing the phase noise. For this value of g_m/I_D, the current I_{bias} is 1.6mA and the estimated phase noise is -86dBc @ 600kHz.

Using the tool described in the previous sections to obtain the quasi-static boundary of the technology, it has been checked that in the selected operating point it is possible to assume quasi-static operation of the transistors at 910MHz.

In the Fig.11 it is shown the complete layout of the fabricated circuit, including amplifiers and the VCO.

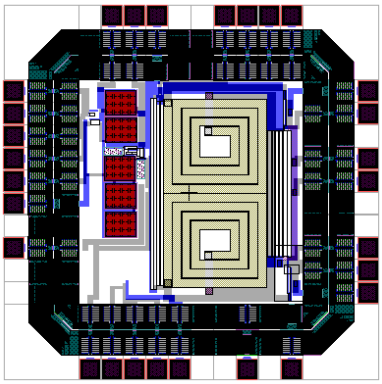

Figure 11: Complete layout: amplifier and VCO

8. CONCLUSION

In this work it has been presented a flexible tool to help in the design of low power RF blocks. It has also been shown the existence of an optimum inversion level which gives the minimum power consumption for a given gain, or equivalently, the maximum gain for a given consumption. This optimum inversion level appears in different types of amplifiers and in varied technologies. Finally it has been shown the feasibility of working, with 0.35µm technologies at 910MHz, in moderate inversion, which gives a better compromise between speed and consumption.

9. ACKNOWLEDGMENTS

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