ADVANCED SURFACE PASSIVATION OF CRYSTALLINE SILICON FOR SOLAR CELL APPLICATIONS

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DECLARATION

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in this thesis.

This thesis has also not been submitted for any degree in any university previously.

Shubham DUTTAGUPTA

Date: 15th September 2014

Take up one idea. Make that one idea your life - think of it, dream of it, and live on idea. Let the brain, muscles, nerves, every part of your body, be full of that idea, and just leave every other idea alone. This is the way to success.

– *Swami Vivekananda*

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Abstract

Photovoltaic (PV) electricity generation has the potential of becoming a major player in the global power market. Today, crystalline silicon (*c*-Si) wafer solar cells dominate the PV market (> 80 % market share), and they are likely to dominate the market for at least the next 15 years. To further reduce the cost of PV electricity, continuous technological developments are required in terms of efficiency and/or manufacturing cost ($\$/m^2$) of PV cells and modules, giving lower $/W costs. To further decrease the costs of PV electricity derived from PV cells, industry is continuously decreasing the production cost and reducing the solar cell thickness while trying to maintain - or even trying to employ technologies to further improve - the solar cells' energy conversion efficiency. An efficiency increase works as a leverage to reduce the relative cost downstream in the PV value chain (module and system cost).

Excellent passivation of the front and rear surfaces becomes imperative for achieving higher efficiency of *c*-Si wafer solar cells, especially for cells with reduced thickness. In order to continue to drive cost reduction and improvement of PV cell efficiency in mass-scale production, it is extremely important to evaluate, improve and develop 'efficient & cost-effective' surface passivation layers compatible with mass-scale production. This PhD research intends to bring surface passivating materials investigated in laboratory-scale environment into an 'industrially relevant' cost-effective environment, while continuing to further improve the surface passivation results.

There are four topics investigated in this thesis:

(1) Surface passivation of *c*-Si using industrial plasma-enhanced chemical vapour deposition (PECVD) of silicon nitride, which is one of the mainstream technologies in today's *c*-Si PV industry. Progress in the field of silicon nitride surface passivation can have significant additional impact on the PV industry, as this can enable further solar cell efficiency improvements with no additional processing cost. Improved surface passivation results with extremely low surface recombination velocities $S_{eff,max}$ of 2 and 5 cm/s on *n* and *p* type *c*-Si, respectively, and emitter saturation current densities J_{0e} of 15 fA/cm^2 on n^+ type *c*-Si are demonstrated in this thesis for plasma deposited silicon nitride films. Such results were previously only possible with 'static' depositions or by non-industrial annealing, whereas this work used an inline 'dynamic' deposition and standard industrial firing for activation of the passivation. If applied to the front of n^+p solar cells, these films are shown to improve the cell efficiency by up to 0.2% absolute.

(2) Silicon nitride generally does not provide an effective surface passivation of heavily doped *p*-type *c*-Si when applied directly on H-terminated silicon surfaces. In this PhD thesis high-quality low-temperature SiO_x layers are developed and optimised for *c*-Si surface passivation. SiO_x layers can be deposited using a low-temperature (< 300 °C) PECVD method, or formed by a chemical pre-treatment at < 100 °C. When capped with a SiN_x or AlO_x layer, the stack yields very low $S_{eff,max}$ of 7 and 8 cm/s on *n* and *p* type *c*-Si, respectively, and shows remarkably low J_{0e} of 8 fA/cm^2 on n^+ type *c*-Si surfaces and 15 fA/cm^2 on p^+ type *c*-Si surfaces. This is an important progress in the area of dielectric passivation of *c*-Si surfaces, as this dielectric stack (having very low positive charge density, whereby the surface passivation is ruled by the low density of interface states) is demonstrated in this thesis to passivate all surfaces of *c*-Si (*n* and *p* type) with arbitrary surface doping concentration. In addition, this development provides an alternative cost-effective passivation technology that can be attractive for both academia and industry.

(3) During the inception of this PhD research, aluminium oxides were shown in the literature to provide excellent surface passivation on *p*- and *n*-type Si surfaces, and also on p^+-type Si surfaces, using the atomic layer deposition (ALD) method. In this PhD, these are further studied and optimised for excellent passivation of *c*-Si using one of the industrially feasible techniques, PECVD. AlO_x (with or without a SiN_x or SiO_x capping layer) is demonstrated to provide exceptional passivation of both n^+ and p^+ type *c*-Si surfaces simultaneously (with J_{0e} of 12 and 9 fA/cm^2, respectively), for a large range of sheet resistances. This is an important step forward in the area of surface passivation in regards to the AlO_x technology, as this has specific significance for devices that need a single dielectric film to passivate both n^+ type and p^+ type *c*-Si surfaces, for example interdigitated back contact (IBC) cells.

(4) The polarity and amount of fixed charge have a profound impact on the surface recombination velocity and the solar cell's operation. In this thesis the fixed charge within a dielectric is experimentally varied, in a controlled way, by up to one order of magnitude (10^{11} - 10^{12} elementary charges/cm^2), without any impact on the density of interface states at midgap ($D_{it,midgap}$). It should be noted that this is the first time where fixed charge is 'controllably varied' over such a wide range without any impact on the functional properties and the interface defect density. Experimentally it is shown that S_{eff} scales with $1/Q^2$, which previously was investigated only by simulations or external corona charging. If the $D_{it,midgap}$ (or 'chemical passivation') is retained constant in the finished *p*-type solar cells, then charge tailoring can be an effective tool for improving the efficiency of both PERC and PERL (or LBSF) cells. All three dielectric films (SiN_x,

SiO_x/SiN_x, AlO_x/SiN_x) developed in this thesis are applied at the rear surface of full-area (239.5 cm^2) *p*-type Si Al-LBSF solar cells and their performance is investigated using quantum efficiency and 1-Sun I-V measurements. Screen-printed Al-LBSF solar cells with AlO_x/SiN_x rear surface passivation have the best PV efficiency (of up to 20.1%). Detailed analysis reveals, for example, that the fill factor of Al-LBSF solar cells with a high positively charged dielectric is strongly reduced due to a significant increase in non-ideal recombination. This non-ideal recombination is found to increase for higher positive charge densities and could be due to additional recombination in the space charge region beneath the rear Si surface.

In conclusion, this thesis presents significant progress in *c*-Si surface passivation for the most important dielectrics in the c-Si PV industry, using industrial processing conditions. Together with detailed explanations of the underlying fundamentals, the results presented in the thesis are expected to close the gap in passivation results between laboratory and industrial conditions. This can help manufacturers to reduce surface recombination losses - and thus improve the efficiency of their *c*-Si solar cells - in a cost-effective way.

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List of Symbols

Symbol	Description	Unit
τ_{eff}	Effective lifetime	s
$\tau_{eff,max}$	Maximum effective lifetime	s
τ_{SRH}	Shockley-Read-Hall lifetime	s
$\tau_{intrinsic}$	Intrinsic lifetime	s
τ_{Auger}	Auger lifetime	s
τ_{bulk}	Bulk lifetime	s
$\tau_{radiative}$	Radiative lifetime	s
$\tau_{surface}$	Surface lifetime	s
S_{eff}	Effective surface recombination velocity	cm/s
$S_{eff,max}$	Maximum effective surface recombination velocity	cm/s
$S_{eff,UL}$	Upper-limit of effective surface recombination velocity	cm/s
S	Surface recombination velocity	cm/s
J_{0e}	Emitter saturation current density	A/cm^2
J_0	Saturation current density	A/cm^2
T	Absolute temperature	K
R_s	Series resistance	Ω
R_{sh}	Shunt resistance	Ω
n	Ideality factor	-
V_T	Thermal voltage (kT/q)	V
η	Power conversion efficiency	%
J_{sc}	Short-circuit current density	A/cm^2
V_{oc}	Open-circuit voltage	V
iV_{oc}	Implied open-circuit voltage	V
$V_{oc,limit}$	Open-circuit voltage limit	V
λ	Wavelength	m
A	Absorptance	%
η_c	Carrier collection efficiency	%
R	Reflectance	%
p	Density of free holes	cm^{-3}

n	Density of free electrons	cm^{-3}
N_A	Acceptor concentration	cm^{-3}
N_D	Donor concentration	cm^{-3}
D_n	Diffusion coefficient for electrons	cm^2/s
D_p	Diffusion coefficient for holes	cm^2/s
t	Time	s
$U_{surface}$	Surface recombination rate	$cm^{-2}\ s^{-1}$
E	Energy	eV
E_C	Conduction band energy	eV
E_F	Fermi energy	eV
n_0	Electron density at thermal equilibrium	cm^{-3}
p_0	Hole density at thermal equilibrium	cm^{-3}
E_V	Valence band energy	eV
n_i	Intrinsic carrier density	cm^{-3}
E_g	Bandgap energy	eV
R_{sh}	Sheet resistance	Ω/□
x_j	Junction depth	m
Δn	Excess election density	cm^{-3}
Δp	Excess hole density	cm^{-3}
$\Phi_{AM\ 1.5G}$	Photon flux of AM1.5G spectrum	$cm^{-2}\cdot s^{-1}$
α	Absorption coefficient	cm^{-1}
n	Refractive index	-
κ	Extinction coefficient	-
W	Silicon wafer thickness	m
σ_n	Electron capture cross section	cm^2
σ_p	Hole capture cross section	cm^2
v_{th}	Thermal velocity	cm/s
D_{it}	Interface trap density	$cm^{-2}\cdot eV^{-1}$
p_s	Surface electron density	cm^{-3}
n_s	Surface hole density	cm^{-3}
S_{n0}	Electron surface recombination velocity	cm/s
S_{p0}	Hole surface recombination velocity	cm/s
A	Area	cm^2
d	Distance	cm
V_{CPD}	Contact potential difference voltage	V

Q_c	Corona charge	q cm^{-2}
J_c	Corona flux	ions/(cm^{2}s)
V_{CPD}^{light}	Contact potential difference voltage under illumination	V
V_{CPD}^{dark}	Contact potential difference voltage under dark	V
V_{DC}	Bias voltage	V
C	Capacitance	C
AC	Alternating current	A
χ_s	Electron affinity	eV
V_D	Dielectric voltage	V
V_{SB}	Surface barrier voltage	V
ϕ_{m1}	Work function of a metal	eV
ϕ_{ms}	Metal semiconductor work function	eV
Q_{total}	Total charge in the dielectric	q cm^{-2}
V_{FB}	Flatband voltage	V
ε_s	Permittivity of the semiconductor	F/m
ε_0	Permittivity of vacuum	F/m
k_s	Dielectric constant of the semiconductor	-
L_D	Debye length	cm

List of Acronyms

Acronym	Description
AlO_x	Aluminium oxide
Alneal	Post-metallisation anneal of Al-covered Si-SiO_2 interfaces
ARC	Antireflection coating
ABC	All back contact
BSF	Back surface field
C-V	Corona-voltage as used frequently in this PhD thesis
Cz	Czochralski
DC	Direct current
EQE	External quantum efficiency
FGA	Forming gas anneal
FZ	Float-zone
ISFH	Institut für Solarenergieforschung Hameln/Emmerthal
IQE	Internal quantum efficiency
I-V	Current-Voltage
PC-1D	Name of one-dimensional numerical semiconductor simulation program for personal computers
PECVD	Plasma-enhanced chemical vapour deposition
PERC	Passivated emitter rear cell
PERL	Passivated emitter rear locally diffused
PV	Photovoltaics
RCA	Radio Corporation of America
SIMS	Secondary ion mass spectrometry
SiN_x	Plasma silicon nitride
SiO_x	Plasma silicon oxide
SRH	Shockley-Read-Hall
FF	Fill factor
SR	Spectral response
WAR	Weighted average reflectance

Chapter 1: Introduction

1.1. Photovoltaic (PV) Electricity

Renewable energies are urgently needed to solve some of the biggest challenges human-kind is facing at this moment in time, such as global warming, energy shortages and energy security. Among various renewable energy resources, solar energy is a clean, climate-friendly, abundant and inexhaustible energy resource, which is relatively well-spread over the globe. Its availability is greater in warm and sunny countries – the countries that will experience most of the world's population and economic growth in the next decades. In 90 minutes it is estimated that sufficient solar energy strikes earth to provide mankind's yearly energy needs. The annual amount of energy received from the sun far surpasses the total estimated resources of all fossil and nuclear fuels combined. It is also significantly larger than yearly potential of other renewable energy sources i.e. bio-energy (biomass, photosynthesis), hydro and wind power [1]. Interestingly, the lowest estimate of the technical potential for direct solar energy is not only higher than the current global primary energy demand, but also higher than the highest estimate of any other renewable energy potential [2]. From the two basic ways of capturing the sun's energy, apart from day lighting, i.e. heat and photoreaction, four main domains of applications can be distinguished: photovoltaic (PV) electricity, heating (and cooling), solar thermal electricity, and solar fuel production [1]. In addition to enormous potential, PV electricity helps to eliminate "on-site" emissions resulting from fossil fuel consumption in buildings, industries and transport sectors contributing towards sustainability. While photovoltaic electricity from solar energy has huge potential, it still only represents a tiny fraction of the world's current energy mix. Historically, this was mainly due to the cost of PV electricity being higher than cost of bulk electricity stemming from conventional non-renewable energy driven electricity plants (for example from coal/petroleum/natural gas/nuclear). However, this is changing rapidly and is currently being driven (partly) by government policies to improve energy access, provide energy security and to mitigate climate change, which is required for sustainable future. Around the world, countries and companies are investing in solar electricity generation capacity on an unprecedented scale, and, as a consequence, costs continue to fall and technologies improve. This will allow PV residential and commercial systems to achieve parity with the distribution grid electricity

retail prices in a number of countries characterised by a good solar resource and high conventional electricity retail prices. In many countries it is argued that the cost of PV electricity has already reached 'grid parity' (a term that refers to when an alternative energy source can generate electricity at a levelised cost (LCoE) that is equal to the price of purchasing power from the electricity grid) [1]. Solar thermal electricity (STE) and solar PV electricity are now competitive against non-renewable fuelled electricity generation in sunny countries, usually used to cover demand peaks.

Photovoltaics is the direct conversion of sunlight into electricity by means of solar cells. It is one of the most promising technologies to satisfy mankind's energy demands. In 1839, the French scientist Alexandre-Edmond Becquerel discovered the photovoltaic effect, which forms the basis behind the photovoltaic technology today. In 1954, Darryl Chapin, Calvin Fuller and Gerald Pearson, associates of Bell Labs, made the first efficient silicon solar cell – initially for powering satellite applications – an extreme example of remote, off-grid electricity demand. The energy crisis of the 1970s saw the beginning of major interest in using solar cells to produce electricity for homes and businesses, but it came with prohibitive prices (nearly 30 times higher than the current price) that made large-scale applications impractical [1]. Today, a range of PV technologies, using different materials, device structures and manufacturing processes, is available on the market and is under development in laboratories.

Rapidly falling prices have made solar PV electricity more affordable than ever. In the last decade the PV sector has experienced the most significant boom to date and is expected that this is only the beginning. The average price of a completed PV system has dropped by more than 30% since the beginning of 2011. From a relatively small industry back in early 2000, the PV sector has now become a $100 billion a year business with a global reach. The major factors contributing to the growth were government subsidies, significant capacity increases, and continual innovations. Photovoltaic cells are interconnected to form PV modules with a power capacity of up to several hundred watts. Photovoltaic modules are then combined to form PV systems. Massive increase in installed PV system capacity was witnessed from 4.5 GW in 2005 to 37 GW in 2013 [3]. In parallel, the price of solar PV modules dropped from approximately \$ 4/W_p in 2008 to less than \$ 1/W_p in 2013.

1.2. Crystalline silicon wafer solar cells

Since the 1960s, crystalline silicon wafer solar cells have dominated the PV market. Silicon, being non-toxic and abundantly available, has also proven to be long-term stable when modularized. Today, crystalline silicon PV is the workhorse of the PV energy market. In the last decade the market share of *c*-Si PV has always been in the range of 80-90%, as illustrated in Figure 1.1 [4]. The cost of PV modules has dropped dramatically as the industry has scaled up manufacturing and incrementally improved the technology with improved as well as new materials. Installation costs have come down too, with more experienced and trained installers [4].

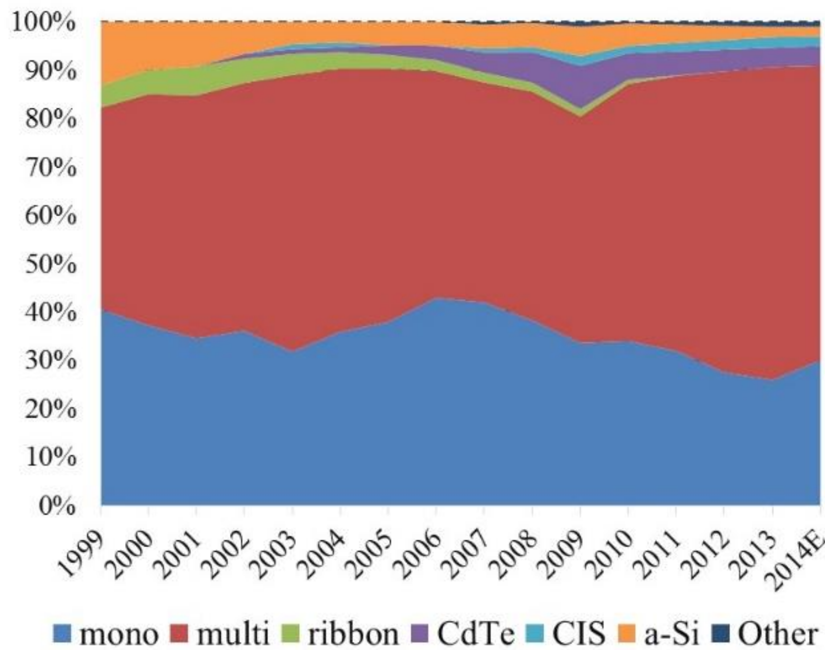

Figure 1.1: Market shares of different PV technologies. Data is based on the yearly market surveys in Photon International, IHS, SolarBuzz and in Ref. [4].

Improvements of the cell, module, or system efficiency reduce the cost in all process steps (wafer, cell, module, and balance of system), because most of the costs are area related. As suggested by Neuhaus *et al*. (and references therein), if the efficiency improves by a factor of α, the production costs per watt decrease by a factor of $\beta = 1/\alpha$ if everything else remains unchanged [5]. For a crystalline silicon wafer solar cell manufacturer, there can be three major strategies for cost reduction: (a) higher efficiencies and/or (b) reduction in manufacturing cost and/or (c) increasing throughput. The individual components for improving each strategy are mentioned in Table 1.1.

Table 1.1: Cost reduction strategies in *c*-Si PV.

1. Higher PV efficiency
1.1. Improved bulk electronic quality 1.2. Improved light trapping in the solar cell 1.3. Reduction of surface recombination losses 1.4. Improved junction formation 1.5. Reduced ohmic resistance losses 1.6. Alternative metallization concepts 1.7. Alternative high-efficiency structures 1.8. Emerging technologies (beyond silicon or multijunction technologies)
2. Reduction of cost of manufacturing and related expenditure
2.1. Reducing the cell thickness 2.2. Cheaper feedstock technologies 2.3. Development of cheaper yet efficient process technologies 2.4. Alternative metallisation technologies
3. Higher throughput and yield
3.1. Increased capacity of processing (wafers per hour) with higher yield per equipment without increasing the floor space

1.3. Thesis Motivation

Although PV electricity has a positive impact on the environment, it is required that the PV industry provides power generating products that are cost-competitive with conventional and other renewable sources of energy. Improving conversion efficiency of crystalline silicon wafer solar cells in combination with reduced production cost is imperative to reduce the costs of PV electricity. The so-called 'efficiency limit' of a crystalline silicon wafer solar cell at one-Sun irradiance is well established at approximately 29% [6-8]. This physical limitation for the efficiency mainly originates from the bandgap of silicon as well as from the diode characteristic of the solar cell. In addition to the loss mechanisms that limit the efficiency potential of a c-Si solar cell to approximately 29%, other losses which further decrease the efficiency are mentioned in Table 1.2.

Excellent passivation of the front and rear surfaces is of key importance for achieving higher conversion efficiency of silicon wafer solar cells [9]. Recently the highest conversion efficiency of a crystalline silicon solar cell has been experimentally demonstrated to be 25.6 % (cell area: 143.7 cm^2) achieved using the back contact heterojunction cell technology, HIT (Heterojunction with Intrinsic Thin layer) by Panasonic [10], which is already quite close to the theoretical limit. This cell structure is an embodiment of

excellent surface passivation. It was reported that the use of high-quality surface passivating films suppresses the surface recombination velocities at both surfaces of the HIT devices to as low as 2 cm/s, which is key for its high open-circuit voltage (V_{oc}) of up to 750 mV [10, 11]. Another commercially available high-efficiency device, the Interdigitated Back Contact (IBC) cell having high conversion efficiency of 25 % successfully maintains very low recombination in the cell with total saturation current density (J_0) loss to be as low as ~10 fA/cm^2 [12]. For 23% efficient 'passivated emitter rear locally diffused' (PERL) cells, Aberle *et al.* have calculated that approximately 50 % of the total recombination losses at the 1-sun maximum power point occur at the rear and front surfaces combined (25% at the rear side and < 25% at the front side) [13]. This explains that mitigating surface recombination losses is one of the most important strategies in the quest for higher efficiencies.

Table 1.2: Major loss mechanisms of *c*-Si solar cells.

1. Electronic recombination loss
1.1. surface recombination 1.2. recombination in the heavily-doped regions 1.3. bulk recombination 1.4. metal recombination 1.5. non-ideal recombination
2. Optical loss
2.1. front side reflection 2.2. rear-internal reflection 2.3. metal shading
3. Ohmic resistance loss
3.1. series resistance 3.2. shunt resistance

The motivation of this thesis is to further improve and develop 'industrially feasible' surface passivation layers using different dielectrics that provide a 'reduction of surface recombination losses' at moderately and heavily doped crystalline silicon surfaces. Considering the immense progress in the surface passivation using 'laboratory-type' equipment in the last three decades it is now very important to demonstrate such high-quality results using 'industrial' equipment. In addition specific attention was given to the applicability of an industrial annealing process for the activation anneal – thus, all surface passivation experiments were studied after an optimised high-temperature anneal ('fast firing') that is typically used for industrial screen-printed silicon solar cells. Development

of cheaper, improved and alternative process technologies for surface passivation of moderately and heavily-doped crystalline silicon are shown in this thesis, which can be considered highly relevant for industrial applications.

1.4. Outline of this PhD thesis

Low-temperature 'industrial' plasma-enhanced chemical vapour deposited (PECVD) silicon nitride (SiN_x), silicon oxide (SiO_x) and aluminium oxide (AlO_x) films developed in this research resulted in excellent passivation of moderately and heavily doped c-Si surfaces. Chapter 2 briefly explains the fundamentals of surface passivation and the underlying mechanisms. With the help of simulations it is shown that polarity and magnitude of fixed charge in the surface passivating dielectrics have a profound impact on surface recombination velocity. The impact of a reduced surface recombination velocity on the *c*-Si solar cell efficiency is demonstrated using simulations with the widely available PC1D computer programme. Most of the results of this PhD thesis have been published in peer-reviewed journals or in leading international conferences. Chapters 3 - 5 study the performance of various passivating layers on different surfaces and report significant progress in surface passivation results. Experimental demonstration of 'charge tailoring' is discussed in Chapter 6, which can be an effective tool for improving the PV efficiency. It should be noted that charge tailoring was performed on all the three dielectrics studied in the thesis, but only the results related to SiO_x/SiN_x are presented as this stack allowed up to one order of magnitude variation in the fixed charge density. Finally, Al-LBSF solar cells are fabricated using the three dielectrics developed in this work and results are discussed in Chapter 7.

Chapter 2: Background and literature review

2.1. Introduction

This chapter provides the basic fundamentals of surface passivation of semiconductors, a brief explanation of technological means required for reducing surface recombination, and its influence on solar cell efficiency. The surface passivation mechanism is explained to be ruled by interface defect states (represented by the parameter $D_{it,midgap}$) and fixed charge density Q_f (both in polarity and magnitude) at the *c*-Si/dielectric interface. By means of simulations it is shown that the polarity and magnitude of Q_f has a profound impact on the effective surface recombination velocity S_{eff}. The role of Q_f in passivating heavily doped silicon is also illustrated, which forms the basis for the explanation of several results in the thesis. In addition it is shown that polarity and magnitude of Q_f also can influence bulk recombination process beneath the silicon surface. It is finally emphasised that the right choice of dielectric, with suitable charge polarity and magnitude, is essential for high efficiency of *c*-Si solar cells. Using simulations with the device simulator PC1D, the impact of reduced surface recombination on the efficiency of *c*-Si solar cells is demonstrated. Finally, the state-of-the-art maximum effective surface recombination velocity $S_{eff,max}$ values and emitter saturation current density J_{0e} values reported in the literature are summarized for undiffused *n*- and *p*-type c-Si surfaces and heavily doped n^+- and p^+-type c-Si surfaces, enabling a comparison with the results achieved in this PhD thesis.

2.2. Fundamentals of surface passivation

The surface of a semiconductor represents the largest possible disturbance of the symmetry of the crystal lattice. A large density of defects (surface states) within the bandgap exists at the surface of the crystal owing to non-saturated 'dangling' bonds. Additional process-related surface states resulting from chemical residues and metallic depositions on the surface or from dislocations further increase the number of defect states, resulting in significant recombination of excess charge carriers at the surface.

In the surface recombination process an electron from the conduction band recombines with a hole in the valence band via a defect level ('surface state') within the bandgap.

Recombination via defects in semiconductors is described by the Shockley-Read-Hall (SRH) theory. The SRH theory predicts the surface recombination rate $U_{surface}$ (unit: $cm^{-2}s^{-1}$) for a single-level defect located at an energy E_t (energy level of the traps) as [14, 15]:

$$U_{surface} = \frac{(n_s p_s - n_i^2)\nu_{th} N_{st}}{\frac{n_s+n_1}{\sigma_p} + \frac{p_s+p_1}{\sigma_n}} = \frac{n_s p_s - n_i^2}{\frac{n_s+n_1}{S_{p0}} + \frac{p_s+p_1}{S_{n0}}} \quad (2.1)$$

$$n_1 \equiv n_i \exp\left(\frac{E_t - E_i}{kT}\right),\ p_1 \equiv n_i \exp\left(\frac{E_t - E_i}{kT}\right),\ n_1\, p_1 = n_i^2$$

$$S_{n0} \equiv \sigma_n \nu_{th} N_{st} \text{ and } S_{p0} \equiv \sigma_p \nu_{th} N_{st}$$

where n_s and p_s are the free electron and hole density at the surface respectively, n_i is the intrinsic carrier concentration, ν_{th} is the thermal velocity of the charge carriers (~ 10^7 cm/s in Si at 300 K), N_{st} is the number of surface states per unit area (unit: cm^{-2}), σ_n and σ_p are capture cross sections of electrons and holes respectively, and n_1 and p_1 are statistical parameters expressed as a function of E_i (the intrinsic Fermi level). S_{n0} and S_{p0} are the surface recombination velocity parameters (unit: cm/s) of electrons and holes respectively and can be written as:

In reality, the defects are distributed across the Si bandgap and, as a result, the interface defect parameters ($\sigma_{n/p}$, $n_{1/2}$, and N_{st}) are not constant. They depend on the defect's energetic location (i.e., are band gap energy dependent). Therefore $U_{surface}$ is expressed by the extended SRH formalism with an integral over the band gap [from valence band (E_V) to conduction band (E_C)] replacing N_{st} by the density of interface states D_{it} (unit: $eV^{-1}\,cm^{-2}$) [16-18]. The full expression of the multiple-level surface recombination rate is given in Equation 2.2. It is noted that, generally, the defect states near midgap (0.55 eV) tend to dominate the total surface recombination rate.

$$U_{surface} = (n_s p_s - n_i^2)\nu_{th} \int_{E_V}^{E_C} \frac{\sigma_n(E)\sigma_p(E)D_{it}(E)}{\sigma_p(E)[p_s+p_1]+\sigma_n(E)[n_s+n_1]} dE \quad (2.2)$$

Reduction in surface recombination is referred as surface passivation. Surface passivation can be measured in terms of surface recombination velocity S (unit: cm/s) at the surface of the semiconductor. In analogy to the bulk expression $U_{bulk} = \Delta n/\tau_b$ (where Δn is the excess

carrier density in the bulk and τ_{bulk} the bulk carrier lifetime), a surface recombination velocity (SRV) S can be defined as $U_{surface} \equiv S\, \Delta n_s$ where Δn_s is the excess carrier density at the surface. For the case of flatband conditions at the surface and negligible carrier trapping, the excess densities of electrons and holes are equal ($\Delta n_s = \Delta p_s$) giving [17, 19, 20]:

$$S(\Delta n_s) = \frac{n_0 + p_0 + \Delta n_s}{\frac{n_0 + n_1 + \Delta n_s}{S_{p0}} + \frac{p_0 + p_1 + \Delta n_s}{S_{n0}}} \quad \text{..........................(2.3)}$$

This shows that the SRV not only depends on the properties of the surface states [i.e. their energy level (via n_1 and p_1) their density and their capture cross sections for electrons and holes (via S_{n0} and S_{p0})], but also on the injection level Δn_s at the surface and on the wafer doping level (via n_0 and p_0) [17, 19, 20]. In practical devices there is usually a bending of the energy bands towards the surface. Hence in contrast to the flatband case of Equation 2.3 there exists no analytical expression for the SRV. Instead the surface recombination rate must be calculated from Equation 2.2, using numerically determined values for n_s and p_s. Upon calculation of $U_{surface}$ in analogy to the concept of effective recombination velocities of high-low junctions [21], an effective SRV (S_{eff}) at the surface of *p*-type semiconductors (for example) is defined as:

$$S_{eff} = \frac{U_{surface}}{\Delta n\,(x=d)} \quad \text{.................................(2.4)}$$

which can be determined at a virtual surface within the wafer positioned at the edge of the surface space charge region (located at $x = d$) [17, 19, 20]. Δn is the excess minority carrier concentration (in cm^{-3}).

If the sample features a *p-n* junction, then the electronic quality of the emitter is usually expressed via the emitter saturation current density J_{0e}. For example, for an n^+ diffused emitter on a lowly injected *p*-type wafer with acceptor density N_A, the relation between S_{eff} and J_{0e} is (for details see Refs. [17, 19, 20]):

$$S_{eff} = \frac{J_{0e}\, N_A}{q\, n_i^2} \quad \text{..............................(2.5)}$$

2.3. Characterisation of surface passivation

2.3.1. Evaluation of surface passivation of undiffused and diffused Si surfaces

Characterisation or evaluation of surface passivation requires measurement of S_{eff} (or J_{0e}). A direct measurement of S_{eff} or J_{0e} is not possible. It is, however, possible to measure the so-called effective minority carrier lifetime τ_{eff} of the sample, which takes into account the recombination mechanisms at the surfaces of the sample as well as within its bulk. The measurement of the effective lifetime τ_{eff} can, for example, be done using the photo-conductance method, which is a well-known and widely used method (see Refs. [22-25] and Appendix III). In the photoconductance method, τ_{eff} is measured as a function of the excess minority carrier concentration, which accounts for the recombination losses in the *c*-Si bulk (represented by τ_{bulk}) and the front and rear surfaces (represented by $\tau_{surface}$ for each of the two surfaces). The main assumption here is that both surfaces have a similar surface recombination velocity. It is widely accepted that this assumption is reasonable if the surface preparation is the same for both surfaces and a similar passivation scheme is applied on both the sides, although some concern can be raised regarding the cleanliness of the second surface to be deposited (when the passivation layer is deposited onto the surface). The τ_{eff} of such a symmetrical structure is expressed as:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{Bulk}} + \frac{1}{\tau_{Surface}} \qquad (2.6)$$

$$\frac{1}{\tau_{Bulk}} = \left(\frac{1}{\tau_{Radiative}} + \frac{1}{\tau_{Auger}}\right)_{intrinsic} + \frac{1}{\tau_{SRH}} \qquad (2.7)$$

As shown in Equation 2.7, bulk recombination is determined by both intrinsic (i.e. radiative and Auger recombination, for which empirical models exist [26, 27]) and extrinsic recombination (i.e. SRH recombination) though defects, which can be due to various sources such as non-saturated dangling bonds, metallic impurities, lattice faults, dangling bonds at grain boundaries (in multicrystalline Si), and boron-oxygen complexes (in monocrystalline Czochralski (Cz) grown boron-doped Si) [28-36].

The carrier lifetime due to recombination at the surface ($\tau_{surface}$) can be calculated by solving the following equation [37-39]:

$$\frac{1}{\tau_{Surface}} = \alpha_1^2 D \qquad (2.8)$$

where D (in cm^2/s) is the minority carrier diffusion constant under low injection level and the ambipolar diffusion constant under high injection level and α_1 is the solution of transcendental equation:

$$\tan\left(\frac{\alpha_1 W}{2}\right) = \frac{S_{eff}}{\alpha_1 D} \qquad (2.9)$$

Assuming low-level injection in the wafer, insertion of α_1 from Eq. 2.8 into Eq. 2.9 gives the following relation [40]:

$$S_{eff} = \sqrt{D\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}\right)} \tan\left(\frac{W}{2}\sqrt{D\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}\right)}\right) \qquad (2.10)$$

where W (in cm) is the wafer thickness and D (in cm^2/s) is the minority carrier diffusion constant, dependent on dopant type and resistivity. For a well-passivated sample, τ_{eff} is independent of D and is entirely determined by the recombination within the bulk and the two surfaces of the *c*-Si wafer. If both surfaces are passivated identically, one obtains:

$$S_{eff} = \frac{W}{2}\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{Bulk}}\right) \qquad (2.11)$$

As shown by Sproul *et al*. [22], the relative deviation of Equation 2.11 from the exact solution is below 4% for $S_{eff} < \frac{D}{4W}$. For example, for a 180 μm thick 1.5 Ωcm *p*-type Si wafer, Equation 2.11 is valid if S_{eff} is calculated to be less than ~ 400 cm/s. For an inferior surface passivation (high S_{eff}) the surface lifetime is limited by the diffusion of minority carriers to the surface. In that case Equation 2.10 needs to be used.

It should be noted that some uncertainty may exist in the model for the determination of $\tau_{intrinsic}$ of silicon [26, 27]; hence, passivation properties are preferentially evaluated on high-quality bulk materials, for example float-zoned (FZ) wafers. In this case the total recombination losses can be assumed to be dominated by recombination at the wafer

surfaces. Assuming $\tau_{bulk} = \infty$, one obtains an upper limit of the surface recombination velocity $S_{eff,max}$:

$$S_{eff,max} = \frac{W}{2\tau_{eff}} \qquad (2.12)$$

In *c*-Si solar cells, surface passivation studies of heavily doped regions are very important. They are usually characterised by the emitter saturation current density J_{0e} ('e' stands for emitter, in case of absence of an emitter one can use J_{0s} where 's' stands for surface, which can be a moderately doped *c*-Si surface or a high-low junction). This saturation current density is an important parameter which limits the open-circuit voltage and hence the efficiency of the solar cells. A better surface passivation will mean lower J_{0e}.

Kane and Swanson introduced a method [41] for extraction of J_{0e} from photoconductance measurements at high injection from specially prepared symmetrical lifetime samples [42, 43]. This method is extensively used in this thesis to investigate the level of surface passivation on heavily doped *c*-Si surfaces. Photoconductance within the heavily doped regions can be neglected because they are usually very thin (0.2 to 5 µm) compared to the substrate (~180 µm) and the heavy doping in that region strongly reduces the minority carrier lifetime. At high-injection conditions, the injection level dependence of S_{eff} can be used to separate recombination in the heavily-doped region and the bulk Si [41-43]. The effective lifetime τ_{eff} of a symmetrically diffused wafer with or without passivation can be expressed as [44]:

$$\frac{1}{\tau_{eff}} = \frac{1}{\tau_{Bulk}} + \frac{2}{\tau_{Emitter}} \qquad (2.13)$$

$$\frac{1}{\tau_{eff}} = \left(\frac{1}{\tau_{Radiative}} + \frac{1}{\tau_{Auger}}\right) + \frac{1}{\tau_{SRH}} + \frac{J_{0e}}{qW\,n_i^2}\left(2N_{doping} + \Delta n_{front} + \Delta n_{rear}\right) \qquad (2.14)$$

Subtracting $1/\tau_{intrinsic}$ from $1/\tau_{eff}$ and assuming $\Delta n_{front} = \Delta n_{rear} = 2\Delta n$, Equation 2.14 becomes:

$$\frac{1}{\tau_{eff}} - \frac{1}{\tau_{Intrinsic}} = \frac{1}{\tau_{SRH}} + \frac{2J_{0e}}{qW\,n_i^2}\left(N_{doping} + \Delta n\right) \qquad (2.15)$$

J_{0e} is thus obtained from the slope of the straight line when $\frac{1}{\tau_{eff}} - \frac{1}{\tau_{Intrinsic}}$ is plotted versus Δn (an example is shown in Figure 2.1) provided the measurement is taken at high injection where $\Delta n >> N_{doping}$ (excess carrier density being at least one order of magnitude higher than the bulk doping concentration). The analysis method also allows to extract the SRH bulk lifetime (τ_{SRH}) from the Y-intercept of Figure 2.1, which can be a useful tool for the investigation of solar cell fabrication process steps. High-injection conditions can easily be satisfied when high-resistivity (> 5 Ωcm) substrates are used. At high injection, τ_{SRH} is independent of Δn and thus J_{0e} can be determined from Equation 2.15.

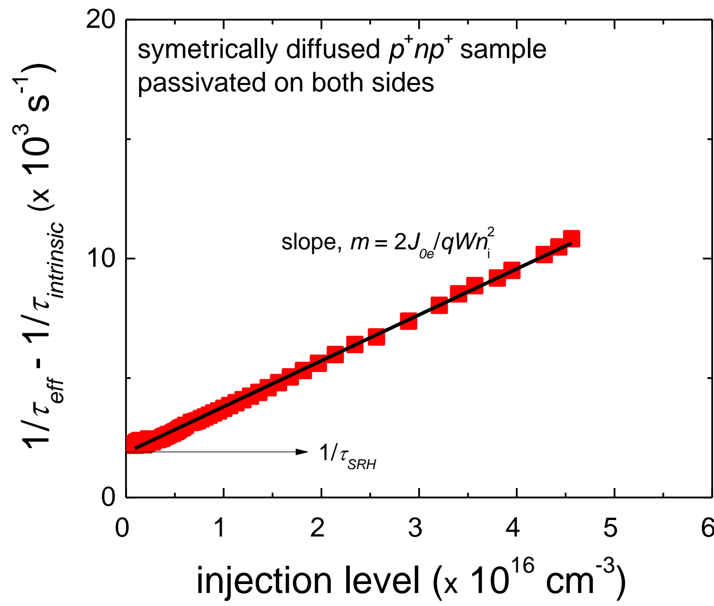

Figure 2.1: Intrinsic recombination (mainly Auger) corrected inverse effective lifetime as a function of injection level of a symmetrically diffused and passivated *c*-Si sample.

2.3.2. Evaluation of electronic interface properties by contactless corona-voltage (*C*-*V*) measurements

The surface passivation of our samples is significantly influenced by the fixed charge density (Q_f) in the SiN_x film, the density of interface defect states (D_{it}) and the capture cross section (σ) of holes and electrons at the *c*-Si/dielectric interface [14, 15, 19, 45-47]. In order to extract fixed charge density (Q_f) in the SiN_x film, the density of interface defect states (D_{it}), contactless corona-voltage measurements were carried out using a PV-2000 metrology tool from Semilab Inc., USA [48-51]. The method uses corona charging in air

to deposit an electric charge on a dielectric thus changing the electric field in the dielectric and in the semiconductor. The response is measured in a non-contact manner by using a contact potential difference (V_{CPD}) in the dark and under strong illumination. The contact potential difference (V_{CPD}) between the wafer and a vibrating reference electrode is determined by using Kelvin probe measurements in the dark and under illumination as a function of the deposited corona charge (Q_c) (a more detailed description of the measurement procedure is mentioned in Appendix IV). Corona charging changes the surface band bending in the crystalline silicon wafer. The change in surface potential due to corona charging at the Si-dielectric interface is defined as surface barrier (ΔV_{sb}). The flat-band voltage (V_{fb}) is obtained when there is no band bending observed upon corona charging (i.e. $\Delta V_{sb} = 0$).

This technique in principle measures the total charge (Q_{total}) in the dielectric. Total charge Q_{total} is defined as the amount of corona charge required to drive the initial condition (band bending due to the charge present in the PECVD layer) to a flat-band condition. It should be noted that the fixed insulator charge density Q_f is considered the main component in Q_{total} (for details see Ref. [51]). It is assumed that the charges contributing to flat-band are all located near the silicon/dielectric interface. *c*-Si samples passivated with a leaky dielectric (such as PECVD SiN_x film) can suffer from hysteresis during a corona-charging measurement, which can potentially adversely influence the measurements. In order to avoid this problem, the measurements were done using only negative corona charges. As a general procedure positive corona charge is used for negatively charged dielectrics (e.g. PECVD AlO_x) and negative corona charge is used for positively charged dielectrics (e.g. PECVD SiN_x, SiO_x).

The density of interface traps, D_{it}, be calculated as the ratio $\Delta Q_{IT}/\Delta V_{SB}$, where ΔV_{SB} is the change in the surface barrier due to the deposited quantum of corona charge and ΔQ_{it} is the interface trap charge density, which is the charge added to the interface traps when the surface barrier changes as ΔV_{sb}. Further details of the procedure of extraction of Q_{total} and D_{it} are discussed in detail by Wilson *et al*. [49, 52] or included in Appendix IV in the thesis. V_{sb} corresponds to an energy position within the Si band gap E_g. For *n*-type Si, $V_{sb} = 0$ corresponds to the Fermi energy level (E_f) below conduction band edge (E_C) (exact location is E_C - E_f, and for our sample it is located ~ 0.25 eV below conduction band). In this way, D_{it} can be extracted as a function of energetic position in the silicon bandgap. In this

technique, the D_{it} spectra starts from flat-band condition (V_{sb} = 0 corresponding to E_f) and extends until deep inversion. This is the reason for very high D_{it} near E_f (as V_{sb} = 0 in this location as flat-band is achieved). This is due to the measurement limitation and D_{it} data under accumulation is inaccessible. Here, the D_{it} is valid from the onset of flat-band condition to deep inversion. The measurements of charge density and energy-dependent interface defect density $D_{it}(E)$ were done on multiple passivated samples at different time intervals to validate repeatability and reliability of the measurement. As a uncertainty experiment few measurements were carried out comparing the contactless corona-voltage and traditional MOS (metal-oxide semiconductor) C-V (capacitance-voltage) technique confirms the $D_{it,midgap}$ values (which are indicative of interface quality) and charge density values are comparable. PECVD SiN_x films are generally "*leaky*" in nature, which often complicates the extraction of Q_{total} and D_{it} measurements. It is important to mention that in order to minimize the impact of leakage for our samples certain steps were taken during the non-contact corona-voltage D_{it} measurement of the SiN_x films. The amount of time for each corona-voltage cycle was reduced as much as possible and a voltage transient was measured after each corona dose. With this time resolved voltage measurement, a leakage correction is performed as described in Ref. [49] which allows the extraction of D_{it} across a larger portion of the bandgap.

2.4. Technological methods to improve surface passivation

The surface recombination rate at a semiconductor surface can be technologically reduced by two different strategies:

2.4.1. Reduction of the density of interface states (also referred to as 'chemical passivation')

The surface recombination rate $U_{surface}$ or the effective surface recombination velocity S_{eff} is directly proportional to the density of defects, D_{it} present at the *c*-Si surface as can also be interpreted from Eq. 2.1. Hence, reduction of the density of interface states D_{it} (see Equation 2.2) is the most obvious and straightforward strategy for achieving good surface passivation. Figure 2.2 shows that S_{eff} scales linearly with $D_{it,midgap}$ (for simplicity only defects at the mid-gap levels are selected and the impact is illustrated) – this is key as it means reducing D_{it} by two orders of magnitude will reduce the surface recombination

losses by two orders of magnitude. This is valid for an arbitrary doping concentration of the silicon (meaning irrespective of whether the silicon is undiffused or diffused).

Technologically, D_{it} can be reduced by application of appropriate surface passivating materials. These surface passivating materials effectively passivate the dangling bonds present at the *c*-Si surface by hydrogen present either in the passivating materials or by annealing in a gas containing hydrogen (e.g. forming gas with 4% hydrogen and 96% nitrogen/argon). An alternative approach is by immersion of Si in polar liquids, with or without illumination [53-55]. The most successful candidates are silicon oxides, amorphous silicon, silicon nitrides and aluminium oxides. For example, a $D_{it,midgap}$ as low as 10^9 eV^{-1} cm^{-2} was obtained for an undiffused *c*-Si wafer passivated by a thermal SiO_2 film after a post-deposition annealing in an hydrogen containing gas (forming gas) [56]. Process conditions and post-deposition annealing play a significant role in the reduction of D_{it} and the surface recombination rate. It will be shown for PECVD silicon nitride, silicon oxide and aluminium oxide used in this thesis, that an appropriate process conditions and a post-deposition anneal in an industrial fast firing furnace effectively reduces $D_{it,midgap}$ to values as low as 3×10^{10} eV^{-1} cm^{-2} (compared to $D_{it,midgap} > 5\times10^{12}$ eV^{-1} cm^{-2} in the as-deposited state).

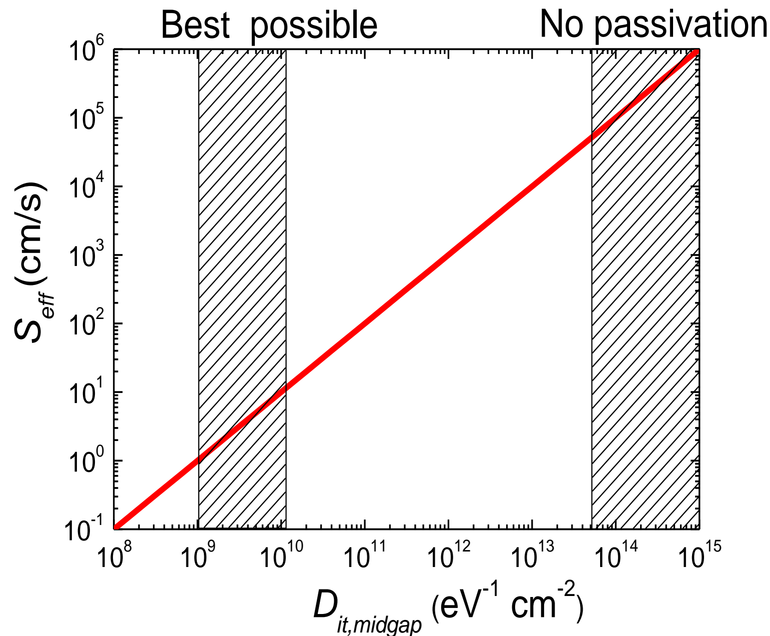

Figure 2.2: Extracted S_{eff} as a function of $D_{it,midgap}$ showing that surface recombination scales linearly with the density of interface states [57].

2.4.2. Reduction of surface concentration of electrons (n_s) or holes (p_s) ('field-effect passivation')

A SRH recombination process requires both a hole and an electron. Furthermore, the capture cross sections for electrons and holes of the dominant defects affect the recombination rate. The highest surface recombination rate is observed when the product of capture cross section and concentration of electrons equals the corresponding product for holes [17]:

$$n_s \sigma_n \approx p_s \sigma_p \, , \qquad (2.16)$$

Apart from the capture cross sections $\sigma_{n/p}$, it can be understood that if the surface concentration (or density) of one charge carrier type (hole or electron) is drastically reduced, then the recombination rate will reduce strongly. Significant reduction in surface electron or hole concentration can be achieved by an internal electric field below the semiconductor surface. Technologically, an internal 'built-in' field can be formed by either implementing a doping profile beneath the surface or by the application of an electrostatic field by means of stable electrical charges in an overlying insulator. The later can be achieved by depositing a thin dielectric layer (having a fixed charge) onto the silicon surface.

For example in PV, silicon oxides and silicon nitrides are widely used as positively charged dielectrics [19], while aluminium oxides can be used as negatively charged dielectrics [57-59]. The polarity and magnitude of the fixed charge have a profound impact on the surface passivation of moderately and heavily doped silicon. The electric field induced by a fixed charge Q_f present in the dielectric (both in terms of polarity and magnitude) impacts the carrier densities at the *c*-Si surface, creating accumulation, depletion or inversion. The influences of negative and positive Q_f on the surface electron (n_s) and hole (p_s) density of a 1.5-Ωcm *p*-type Si wafer are shown in Figures 2.3(a) and 2.3(b), respectively. Correspondingly, the influence of negative and positive Q_f on S_{eff} was extracted to further illustrate the surface passivation mechanism. Relatively small charge densities ($< 1\times10^{10}$ cm^{-2}) of either polarity have almost no impact on the surface passivation (see Figure 2.4). Moderate negative Q_f ($\sim 5\times10^{10}$ - 5×10^{11} cm^{-2}) on *p*-type Si reduces surface recombination gradually unlike the case for moderate positive Q_f where, as expected, the region of 'depletion' arises

when [n] and [p] become comparable at the surface of *c*-Si [see Figure 2.3(b)] and thus results in an increased surface recombination velocity (see Figure 2.4).

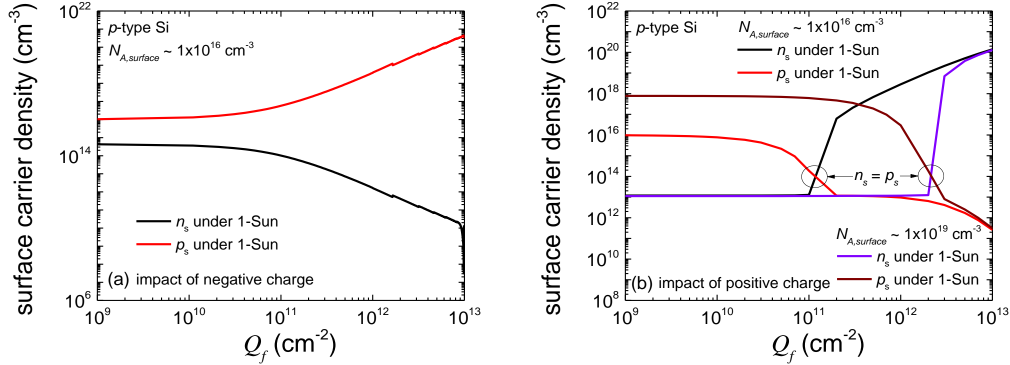

Figure 2.3: Influence of **(a)** negative Q_f and **(b)** positive Q_f on surface electron (n_s) and hole (p_s) carrier density of a 1.5 Ω.cm *p*-type Si wafer (simulation was performed in PC1D assuming 1-Sun illumination and further checked by numerical device simulator Sentaurus by Ma *et al.* [60, 61]).

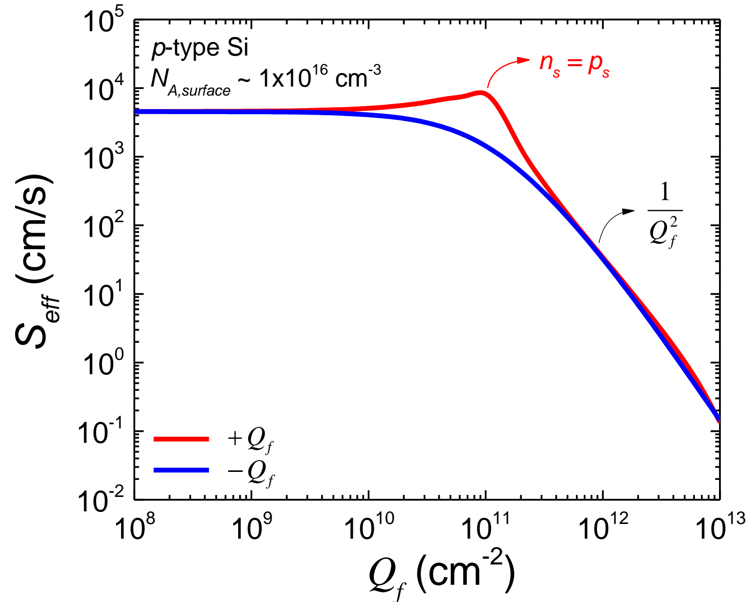

Figure 2.4: Effective surface recombination velocity (S_{eff}) extracted at $\Delta n = 1\times10^{14}$ cm^{-3} as a function of negative and positive Q_f on a 1.5 Ω.cm *p*-type Si wafer (simulation performed in the numerical device simulator Sentaurus by Ma *et al.* [60, 61]) under 1-Sun illumination, $D_{it,midgap}$ was assumed to be 10^{11} eV^{-1}cm^{-2} and $\sigma_n/\sigma_p = 1$)

Such a behaviour was reported in the literature based on theory and on corona charging experiments [17, 18, 62, 63]. Interestingly, this is experimentally observed in this thesis (see Chapter 6) where it will be shown that S_{eff} is higher under depletion conditions. As expected, a higher amount of negative and positive charge induces accumulation and inversion at the *c*-Si surface respectively [see Figures 2.3(a) and 2.3(b)], resulting in a drastic reduction of the surface recombination velocity, see Figure 2.4. For Q_f values of > 5×10^{11} cm^{-2}, the surface recombination velocity scales inversely with the square of Q_f [40].

$$U_{surface} \propto S_{eff} \propto \frac{1}{Q_f^2} \quad \text{(2.17)}$$

This relationship was established previously both in theory [64] and by corona charging experiments, see for example Refs. [46, 62, 64, 65]. Experimental verification of this relationship is shown in this thesis, whereby the fixed charge within a dielectric is experimentally varied, in a controlled way, by up to one order of magnitude (10^{11} - 10^{12} elementary charges/cm^2), without any impact on the density of interface states at midgap energies (more details in Chapter 6).

Effective surface passivation of heavily doped *c*-Si is essential for achieving higher open-circuit voltage and hence higher PV efficiency. Fixed charge in a dielectric also has a strong impact on the surface passivation of heavily doped *c*-Si. As shown in Figure 2.3(a), negative charge on a *p*-type *c*-Si surface leads to accumulation conditions. Hence, irrespective of the doping concentration, negative charge in a dielectric is considered always beneficial for surface passivation of p^+ type *c*-Si as shown by Hoex *et al.* [53] using negatively-charged atomic layer deposited Al_2O_3. This is also shown in this thesis (Chapter 5) where industrially-feasible PECVD AlO_x films are used. Figure 2.3(b) shows the impact of Q_f on the passivation of heavily doped *c*-Si under inversion conditions. When heavily doped *c*-Si (N_A ~ 1×10^{19} cm^{-3}) is used, it is shown that the depletion region shifts towards a higher charge density range +(1-5)×10^{12} cm^{-2} in the example of Figure 2.3(b). A p^+np^+ structure was used for this simulation with measured p^+ dopant profile having surface doping concentration of 1×10^{19} cm^{-3} (as used in Chapter 4). This explains (partly) the reason for inferior passivation of p^+ type *c*-Si by SiN_x, where the Q_f is in a range that drives *c*-Si surface into depletion. This phenomenon is observed several times in this thesis (Chapters

4 and 5). It is also evident from Figure 2.3(b) that, in the case of inversion, reducing Q_f can also help to significantly reduce the surface recombination rate.

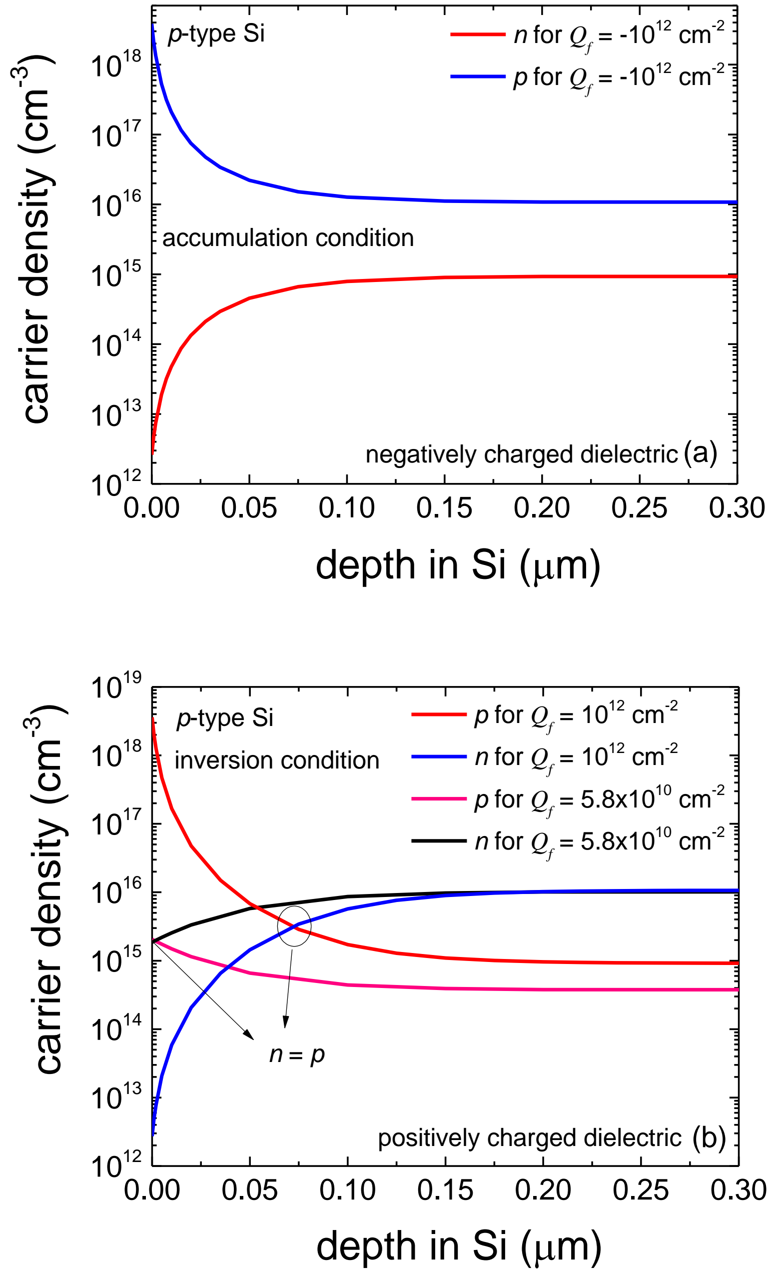

Figure 2.5: Influence of **(a)** negative (-10^{12} cm^{-2}) and **(b)** positive ($+5.8\times10^{10}$, $+10^{12}$ cm^{-2}) fixed charge density (Q_f) on electron (n) and hole (p) carrier density of 1.5 Ω.cm p-type Si wafer as a function of depth in Si (simulations performed in PC1D under 1-Sun illumination)

This forms the basis for the explanation of the surface passivation mechanism of thermal SiO_2 and PECVD SiO_x/SiN_x films on p^+ *c*-Si (see Chapter 4) and PECVD AlO_x films on n^+ *c*-Si (see Chapter 5) where a reduced Q_f is experimentally shown to not be detrimental for the surface passivation, provided the $D_{it,midgap}$ remains low. In general, Figures 2.3 and 2.4 demonstrate the enormous impact of Q_f on S_{eff}. Equation 2.16 means that increasing Q_f by two orders of magnitude will reduce the recombination rate by 4 orders of magnitude. The surface passivation mechanism where surface recombination (or S_{eff}) is ruled by Q_f is referred as 'field-effect passivation' [17, 18, 62].

In addition to its impact on surface recombination, Q_f also affects the recombination rate in a thin sub-surface region. A typical example is shown in Figure 2.5, where the electron [n] and hole [p] carrier density are simulated using PC1D [66] as a function of depth in a 1.5 Ωcm *p*-type Si wafer, for both negative and positive surface charge densities (under one-Sun illumination). As evident from Figure 2.5(a), a negative charge density of 10^{12} cm^{-2} attracts the majority charge carriers (holes) towards the surface, leading to accumulation condition. On the other hand Figure 2.5(b) shows the impact of a positive fixed charge density on *p*-type *c*-Si. A high positive charge (e.g. 10^{12} cm^{-2}) reduces the hole majority charge carrier density at the surface and attracts minority carrier electrons to the surface, leading to inversion conditions at the surface.

At a certain depth below the surface the electron and hole densities are equal ([n] = [p]), causing a local maximum in the recombination rate where $n\sigma_n = p\sigma_p$, [18] (in this case the capture cross section ratio $\frac{\sigma_n}{\sigma_p}$ was assumed to be 1) and is referred to as recombination in the space-charge region (SCR). A space charge region is considered detrimental in the presence of additional bulk defects (such as a damaged sub-surface region as proposed in Refs. [46, 61, 65]). It is speculated in the literature that the presence of a damaged sub-surface region in the space-charge region can lead to an injection-level dependent surface recombination velocity for inverted surfaces, but not for accumulated surfaces. It should be noted that the location of the cross-over point of [n] and [p] densities (region of depletion) beneath the Si surface changes with the magnitude of the positive charge density in the dielectric film. For example, in case of lower positive charge densities, 5.8×10^{10} cm^{-2} as shown here, [n] and [p] are equal at the surface (instead of at some distance below the surface), which in this case will increase the surface recombination velocity. These

artefacts are not present when the fixed surface charges produce accumulation conditions at the surface.

In practice, the surface passivation mechanism for most of the surface passivation materials is ruled by either ‘chemical’ passivation, ‘field-effect’ passivation, or both. For example, thermal SiO_2 - one of the most researched materials in the semiconductor field - relies on both ‘chemical’ and ‘field-effect’ passivation and provides an excellent *c*-Si surface passivation. Depending on the processing conditions, Q_f at the Si-SiO_2 interface can be in the range of 10^{10} - 10^{11} cm^{-2} with very high midgap D_{it} of > 10^{13} $eV^{-1}cm^{-2}$ in as-grown conditions [67, 68]. Such low Q_f and high midgap D_{it} cannot explain a high-quality surface passivation (see Figures 2.2 and 2.4) [19]. However, an optimised anneal (‘Alneal’ or forming gas anneal) significantly reduces the midgap D_{it} to the range of 10^9 - 10^{10} $eV^{-1}cm^{-2}$, explaining the outstanding surface passivation capabilities [17, 56, 67]. The surface passivation mechanism for low-temperature SiO_x/SiN_x stacks developed in this thesis (see Chapter 4) is also explained (mainly) by very good chemical passivation where $D_{it,midgap}$ as low as 3×10^{10} $eV^{-1}cm^{-2}$ and Q_f in the range of 10^{11} - 10^{12} cm^{-2} was measured, depending on processing conditions (more details in Chapters 4). Another widely used positively charged surface passivating material is SiN_x. In fact, PECVD SiN_x is presently a mainstream material in the *c*-Si PV industry and has been researched extensively (for a review see Ref. [69]). The surface passivation mechanism for PECVD SiN_x is also explained by both chemical and field-effect passivation. PECVD SiN_x shows large positive Q_f that is generally of the order of 10^{12} cm^{-2}. In the as-deposited state, PECVD SiN_x can show very large Q_f of up to +(7-8)$\times10^{12}$ cm^{-2} [19, 70, 71], however high $D_{it,midgap}$ (> 5×10^{12} eV^{-1} cm^{-2}) does not allow effective surface passivation. After an optimised anneal[1] the PECVD SiN_x still shows large Q_f up to +(2-4)$\times10^{12}$ cm^{-2} and significantly reduced $D_{it,midgap}$ (~ 3-9$\times10^{11}$ eV^{-1} cm^{-2}). The high-quality surface passivation for SiN_x is explained (mainly) by high built-in positive charge at Si-SiN_x interface (field-effect passivation) in combination with a moderately low $D_{it,midgap}$ (chemical passivation). As explained in the previous section (Figure 2.4) and also by Equation 2.16, a small increase in Q_f significantly improves the surface passivation. This is observed in this thesis (see Chapter 3), which is mainly responsible for the high-quality passivation results with SiN_x reported in this PhD research.

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[1] Industrial fast firing at 850 °C was used in the work.

From Figures 2.3, 2.4 and 2.5 the importance and significance of negatively charged dielectrics is clear. AlO_x (with or without a capping layer[1]) emerged as an interesting dielectric in the PV community [57, 63, 72]. With its negative Q_f at the Si-AlO_x interface[2], AlO_x became especially interesting for *p*-type *c*-Si surface passivation. Figures 2.3(a), 2.4 and 2.5(a) explain the ability of a negative Q_f to not only reduce surface recombination [57, 73, 74] but also avoid enhanced bulk recombination in the SCR. In the as-deposited state, PECVD AlO_x (with or without a capping layer; both cases studied in this PhD thesis) may show a positive[3] or a negative[4] charge density with very high $D_{it,midgap}$ (> 10^{12} eV^{-1} cm^{-2}), resulting in poor surface passivation. After an optimised anneal[4], Q_f in the PECVD AlO_x film reaches up to $-(2\text{-}7)\times10^{12}$ cm^{-2} and $D_{it,midgap}$ reduces to ~ 1×10^{11} eV^{-1} cm^{-2}. Both the high negative Q_f (field-effect passivation) and the comparatively low $D_{it,midgap}$ (chemical passivation) combine to yield the excellent surface passivation reported in this thesis. Table 2.1 summarizes the best reported $S_{eff,max}$ and J_{0e} values available in the literature for undiffused and diffused *c*-Si, respectively.

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[1] The capping layer can be SiN_x or SiO_x, depending on the application and design of solar cell.

[2] In fact the interface is, more precisely, Si-SiO_x-AlO_x (where < 2 nm SiO_x arises after annealing [54]).

[3] Depending on the process conditions. Investigated in this thesis.

[4] Industrial fast firing at 850 °C was used in the work.

Table 2.1: Surface passivation and electronic properties of commonly used multifunctional thin films (containing either positive or negative fixed insulator charge) for homojunction *c*-Si solar cell applications.

Films			Surface passivation results				Electronic interface properties	
			n-type *c*-Si[1]	n^+-type *c*-Si[2]	*p*-type *c*-Si[1]	p^+-type *c*-Si[2]	$D_{it,midgap}$	Q_f
			$S_{eff,max}$	J_{0e}	$S_{eff,max}$	J_{0e}		
			[cm/s]	[fA/cm^2]	[cm/s]	[fA/cm^2]	[$\times 10^{11}$ eV^{-1}cm^{-2}]	[$\times 10^{11}$cm^{-2}]
positively charged films	Thermal SiO_2	static	2.4 [75, 76]	~10 [75, 76]	11.8 [77]	20 [44]	0.01-1 [17, 19, 56, 67]	0.1-1 [19]
positively charged films	PECVD SiO_x[3]	static	2 [78, 79]	210 [80]	11 [81]	NA	0.1-1 [82, 83]	5-10 [78]
positively charged films	PECVD SiN_x	static	3.4 [84]	20 [75]	6.7 [85]	23 [84, 86]	~3-50 [19]	~1-70 [19, 70, 71]
positively charged films	PECVD SiN_x	dynamic	30 [87]	60 [88, 89]	11.8 [90]	NA	NA	NA
negatively charged films	ALD Al_2O_3	static	0.33 [91]	60 [92]	2.35 [91]	10 [74]	1 [73]	−(40-100) [73, 93, 94]
negatively charged films	PECVD AlO_x[3]	dynamic	NA	NA	10 [95]	8 [96]	0.1-10 [97]	−(10-40) [97]

NA stands for 'Not available'.[1]Results are shown for *c*-Si wafers resistivity between 1 to 5 Ωcm that are useful for solar cell fabrication. [2]It should be carefully noted that J_{0e} is partly dependent on the Auger recombination, which will vary with the doping profile and processing conditions done at different laboratories. In addition results with emitters having highest sheet resistance reported for each work is mentioned in this table. [3]Results may have been reported without or with a SiN_x capping layer.

2.5. Surface passivation for high-efficiency *c*-Si solar cells

The entire volume of a *c*-Si solar cell is electronically active. Reducing recombination at the surfaces and in the bulk Si is essential for achieving high conversion efficiency. Having discussed the fundamentals (Section 2.1) and technological methods to reduce surface recombination along with the surface passivation mechanism (Section 2.2 and 2.3), in this section the impact of reducing recombination for achieving higher conversion efficiency of *c*-Si wafer solar cells will be briefly discussed.

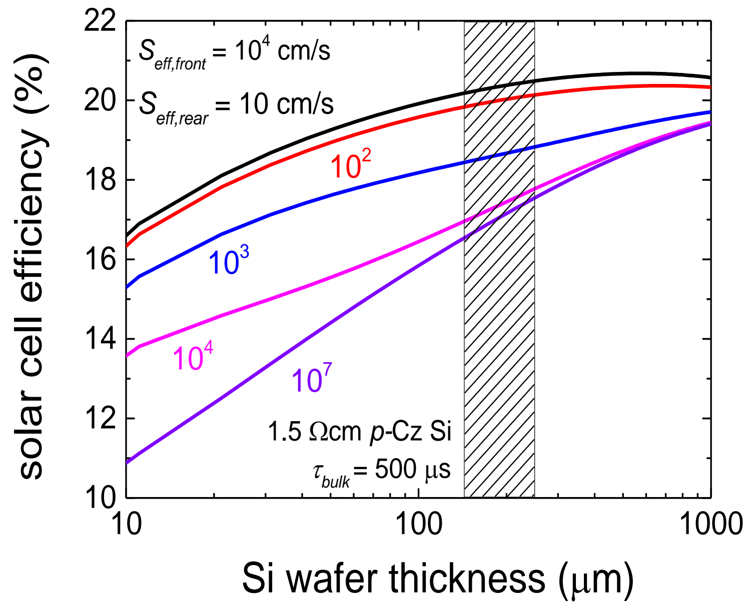

Figure 2.6: Simulated one-Sun efficiency of an n^+p *c*-Si wafer solar cell as a function of the wafer thickness, for several effective rear surface recombination velocities $S_{eff,rear}$. Note that higher cell efficiencies are possible with higher bulk lifetime, higher rear internal reflection R_b (this simulation used R_b of 70%, whereby this parameter is above 90 % for rear dielectrically passivated solar cells) and lower $S_{eff,front}$. The shaded area in the graph represents the wafer thickness range presently used in the PV industry (150 - 250 µm). The cell parameters assumed in the simulation are listed in Appendix II.

The Si wafers account for approximately half of the cost of today's *c*-Si solar cells [98]. Reducing the as-cut wafer thickness would result in a more efficient use of the silicon ingots, which would improve the $/W$_p$ cost if the PV efficiency can be maintained. Due to continuous reductions of the wafer thickness, surface passivation is becoming increasingly important. As evident from Figure 2.6, reducing surface recombination losses at the rear surface ($S_{eff,rear}$) of the Si wafer solar cell becomes imperative when the Si wafer thickness is reduced. Current industry standard is still the aluminium back

surface field (Al-BSF) solar cell with $S_{eff,rear}$ of approximately 500 - 1000 cm/s and a substrate thickness of ~180 µm. Reducing $S_{eff,rear}$ to < 100 cm/s results in an efficiency improvement without changing any other parameter [99-101]. Incorporating surface passivating dielectrics at the rear can result in a drastic reduction in $S_{eff,rear}$, see Table 2.1 for the S_{eff} values obtained after dielectric passivation (Note: in practice the $S_{eff,rear}$ will be higher than S_{eff} values reported in Table 2.1 because of recombination at the metal contacts). Application of rear dielectric also results in improved optics, by increasing the rear surface reflection [99-101].

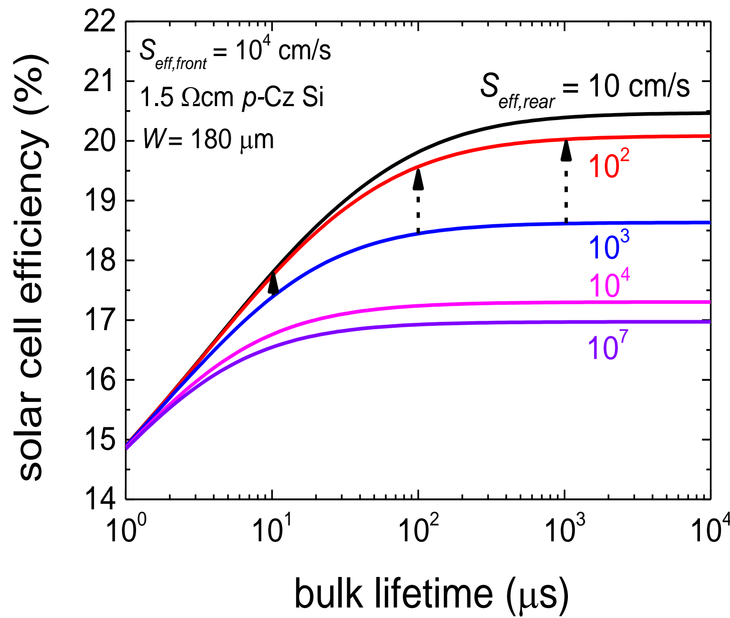

Figure 2.7: Simulated one-Sun efficiency of an $n^{+}p$ *c*-Si wafer solar cell as a function of the bulk lifetime of *c*-Si, for several $S_{eff,rear}$ values. The cell parameters assumed in the simulation are listed in Appendix II.

It is also important to understand the importance of reducing $S_{eff,rear}$ for solar cells using higher bulk lifetime *c*-Si substrates. Figure 2.7 shows that reducing $S_{eff,rear}$ is more effective in increasing the PV efficiency when the recombination losses in the bulk material are low. Even for multicrystalline Si (effective lifetimes of 10 - 150 µs), reducing $S_{eff,rear}$ appears to be effective for enabling higher conversion efficiencies, however the impact is greatly magnified when better monocrystalline Si with higher bulk lifetime is used (effective lifetime lies in the range of 100 - 5000 µs).

Improved surface passivation at both front and rear side for a c-Si solar cell have a significant impact on PV efficiency. Figure 2.8 especially shows that reduction of

$S_{eff,front}$ has a severe impact on efficiency especially when the rear is well passivated. Today for homogeneous emitters with sheet resistance of 70-100 Ohm/sq, front surface recombination velocity $S_{eff,front}$ is generally in the order of 10^4 - 10^6 cm/s [75] depending upon diffusion process conditions and passivation performance (Chapters 3-5). For high-efficiency structures $S_{eff,rear}$ is minimised by the use of passivation layer; here the requirement for reducing $S_{eff,front}$ becomes highly critical for achieving higher conversion efficiency. It is evident from Figure 2.8 that the efficiency of a c-Si solar cell with low $S_{eff,rear}$ (10-100 cm/s) can still be improved by more than 1% absolute by reducing $S_{eff,front}$ to 10^3 cm/s compared to current state-of-the-art of 10^4–10^6 cm/s. Such reduction in $S_{eff,front}$ can be achieved by the use of an optimised emitter profile together with a high-quality dielectric passivation.

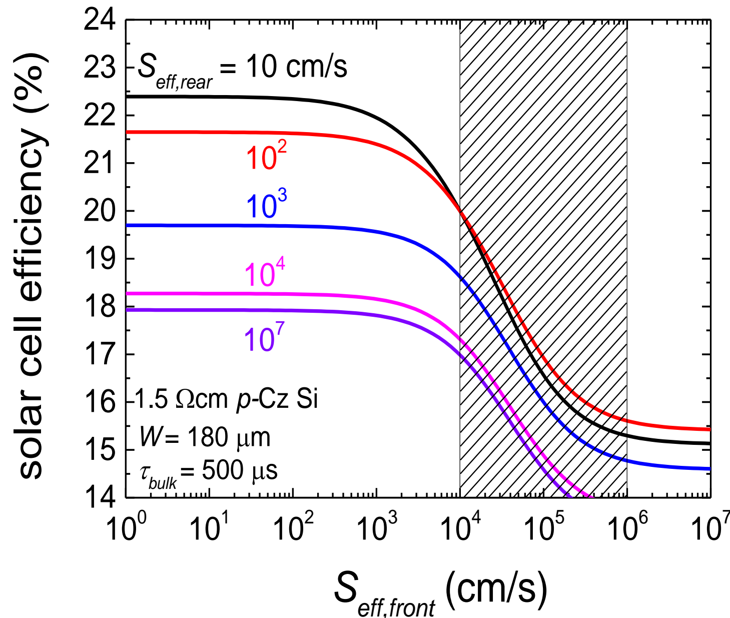

Figure 2.8: Simulated one-Sun efficiency of an n^+p *c*-Si wafer solar cell as a function of $S_{eff,front}$, for several values of $S_{eff,rear}$. The shaded area in the graph represents the current range of $S_{eff,front}$ (10^4–10^6 cm/s) [75]. The cell parameters assumed in the simulation are given in Appendix II.

This thesis mainly concerns with the development, optimisation and improvement of 'industrially-feasible' low-temperature surface passivation schemes for both undiffused *n* and *p* type Si and diffused n^+ and p^+ type Si. These developments and improvements will result in reduction of both $S_{eff,rear}$ and $S_{eff,front}$ in a solar cell devices, which will have a significant impact in improving PV conversion efficiencies.

2.6. Fabrication of test structures

Substrates: The *c*-Si wafers used in this thesis were mainly large-area (either 125x125 or 156x156 mm pseudo square) Cz grown *n* and *p*-type Si. These are mainly selected to align the PhD research relevant for industrial application where Cz silicon are mostly used. The Cz *c*-Si were in the range of 1.5-10 Ωcm (exact base resistivity is mentioned for respective experiments in the following chapters). The thickness of the Cz silicon were in the range of 180 - 220 μm. Note: this is the starting thickness, saw damage removal process as described below removes some Si (the final thickness of the wafers are mentioned in the following chapters/graphs). For certain experiments (mentioned specifically in the thesis) high-quality shiny-polished float-zone (Fz) grown (100 mm diameter circular) *n* and *p*-type Si were used. The Fz *c*-Si were in the range of 1-2 Ωcm. All Cz and Fz *c*-Si wafers used in this thesis has {100} as surface orientation.

Brief details of several processing steps done:

1. Saw damage etch (referred to as SDE hereafter)

Saw damage etch (SDE) process is required for removing microstructural damage caused during sawing and slicing of wafers. SDE was done in a potassium hydroxide (KOH)/de-ionized (DI) solution at 80 °C for 25 mins removing 10 μm of Si from each side.

2. Texturing

Texturing is the process to form random pyramids. This is done at the front side especially to maximise light trapping in Si solar cells. The wafers studied in this work received alkaline texturing in a KOH/isopropyl alcohol (IPA)/DI water solution for 30 minutes at 80 °C. This resulted in a textured surface with upright random pyramids with a size of up to 5-6 μm.

3. RCA cleaning

The purity of the surfaces of a Si wafer is key prerequisite for an effective surface passivation. Si wafer cleaning chemistry has remained essentially unchanged during the last 25 years and is based on hot alkaline and acidic hydrogen peroxide solutions, a process known as Radio Corporation of America (RCA) standard cleaning [19, 102]. All samples used in this thesis strictly follows the cleaning sequence described below unless stated otherwise.

Table 2.2: Cleaning sequence used for the Si wafers processed in this thesis.

Step	Process name	Chemicals used	Details
1	RCA1	28:7:1 H_2O:NH_4OH (25%):H_2O_2 (30%)	10 mins at 80 °C
2	Rinse	Deionised H_2O (~18 MΩcm)	1 min at 20 °C
3	HF	HF (5%)	1 min at 20 °C
4	Rinse	Deionised H_2O (~18 MΩcm)	1 min at 20 °C
5	RCA2	28:7:1 H_2O:HCl (35%):H_2O_2 (30%)	10 mins at 80 °C
6	Rinse	Deionised H_2O (~18 MΩcm)	1 min at 20 °C
7	HF	HF (5%)	1 min at 20 °C
8	Rinse	Deionised H_2O (~18 MΩcm)	1 min at 20 °C
9	Spin-Rinse-Dry	Rinse in deionised H_2O (~18 MΩcm) Dry in N_2 ambient	10 mins

4. Phosphorus diffusion

The RCA cleaned wafers (textured or planar) were diffused in an industrial tube furnace (from Tempress B.V., The Netherlands) using phosphorus oxy-chloride ($POCl_3$) as the phosphorus source. This resulted to a diffused n^+ layer on both surfaces for the Si. Mostly symmetrical phosphorus diffused n^+pn^+ structures were used (unless otherwise stated) with both textured and planar wafers were fabricated – these served as heavily-doped Si surfaces. The sheet resistance of the n^+ emitter was varied by varying the process conditions (time and temperature) during the $POCl_3$ diffusion. The phosphorus silicate glass (PSG) layer formed after diffusion was removed by dipping in 10% HF solution for 2 minutes followed by RCA cleaning process as described in Table 2.2.

5. Boron diffusion

The RCA cleaned wafers (textured or planar) were diffused in an industrial tube furnace (from Tempress B.V., The Netherlands) using boron tri-bromide (BBr_3) as the liquid boron source. The boron diffusion process consisted of two steps, a deposition step for the borosilicate glass (BSG) followed by an in-situ drive-in step at a slightly higher temperature, resulting in a symmetrical p^+np^+ structure. Different time and temperature was used in order to achieve different sheet resistance of the p^+ emitter during the deposition step and drive-in steps. The BSG was removed from the samples using a dip in hot (50 °C) diluted 15% HF solution. All the sample underwent a dry thermal oxidation process at 1050 °C for 75 minutes to produce an approximately 100 nm thick SiO_2 film. This thermal process redistributes the boron atoms in the silicon wafer, resulting in the deep (~2 μm) doping profiles.

6. Dynamic deposition of dielectrics using industrial plasma-enhanced chemical vapour deposition (PECVD) reactor

PECVD reactors can be divided in two main groups: direct plasma and remote plasma reactors. The direct plasma reactors are parallel plate reactors where the wafers are within the plasma zone and influence the plasma. This makes the plasma frequency a very important parameter, which can in turn be divided in two sub-categories: low frequency (10-500 kHz) and high frequency (> 4MHz, with a typical value of 13.56 MHz). The direct plasma reactors are, generally speaking, static deposition systems ("non-moving substrates"). The remote plasma reactors on the other hand have substrates outside the plasma zone. The advantages for remote plasma reactors are the decoupling of the plasma and substrate transportation system, which makes it possible to use substrates with arbitrary shape and size. Furthermore, the low ion energies of the process minimise surface damage and thus the method can be considered better suited for surface passivation of solar cells. The remote plasma reactors can be of static deposition or dynamic deposition ("moving substrates"). The dynamic deposition systems have capabilities of very high throughput (~2000 wafers/hr) and hence are very useful and cost-effective for mass-scale manufacturing.

Overview of the used system

The dielectric (SiN_x, AlO_x, SiO_x) depositions performed in this thesis used an industrial-type inline remote PECVD reactor (SiNA®-XS) from Roth & Rau AG, Germany. The system features an inline modular configuration with a continuous coating capabilities, particularly developed to deposit silicon nitride onto silicon wafers. The system was upgraded to deposit SiO_x and AlO_x layers. All chambers are made of stainless and acid-proof steel. The chamber covers can be swung-up to carry out maintenance and service work. The SiNA® system comprises the following main components:

- Vacuum chambers with heaters, valves, and vacuum pump combinations
- Coating sources installed in process chamber
- Automatic internal transport system
- Gas system
- Cooling system
- Compressed-air system
- Power supplies

Figure 2.9 shows the cross section of the deposition system which consists of three vacuum chambers: load module, process chamber (consisting of buffer module in,

process module and the buffer module out) and unload module. Both loadlocks (loading and unloading modules) are equipped with sliding vane rotary vacuum pump/ roots blower combinations. The entry loadlock contains an infrared lamp heater for the preheating of the carrier during pumpdown. The processing chamber is evacuated through a set of dry rotary pumps, backed up by two successive roots blowers. Inside the processing chamber, two heating plates form an isothermal tunnel as a secondary preheating stage. Then follow the three linear plasma sources. Each consists of a quartz tube which runs across the processing chamber perpendicular to the direction of transport, at a distance of approximately 12 cm above the carrier level. A microwave antenna is located in the centre of the quartz tube, the inside of which is at atmospheric pressure. Alongside the quartz tubes, two rows of magnets are installed, which stabilize the plasma in the low-pressure regime by forcing electrons on curved paths. The plasma source has two types of gas inlet. One set is located above the quartz tubes, and is used for ammonia (for nitride-type depositions, e.g. SiN_x), nitrous oxide (for oxide-type depositions, e.g. SiO_x and AlO_x) and hydrogen. Another two rows of gas inlets (per plasma source) for the introduction of silane are located below the magnets at the front and back end of the plasma source. The plasma is excited around the quartz tubes by means of two continuous-wave magnetron microwave generators with a frequency of 2.45 GHz, each of which feeds up to 4000 W of microwave power (peak power) into both antennae via a symmetrical splitter. In the deposition region (refer to process module in Fig. 2.9), the carrier is heated from the bottom by second heating plate. The deposition takes place in the central part of the deposition chamber, where the wafers underpass a linear plasma source. The carrier rests on rollers, by which it is transported linearly through the vacuum chambers. The rollers are synchronously driven by a belt drive from the outside of the chambers. The wafers cool down in the third part of the deposition chamber before entering the exit load lock chamber. The system is capable for multi-carrier (continuous) depositions with load and unload at the same time. 9 wafers can be processed simultaneously in one carrier. A typical deposition run takes about 3-6 min (depending on the process selected, thickness required and recipe chosen). For different shape and size, different carrier designs are available. The throughput of this system is 500 wafers/h (however can easily be enlarged to industrial demands of up to 2000 wafers/hr.).

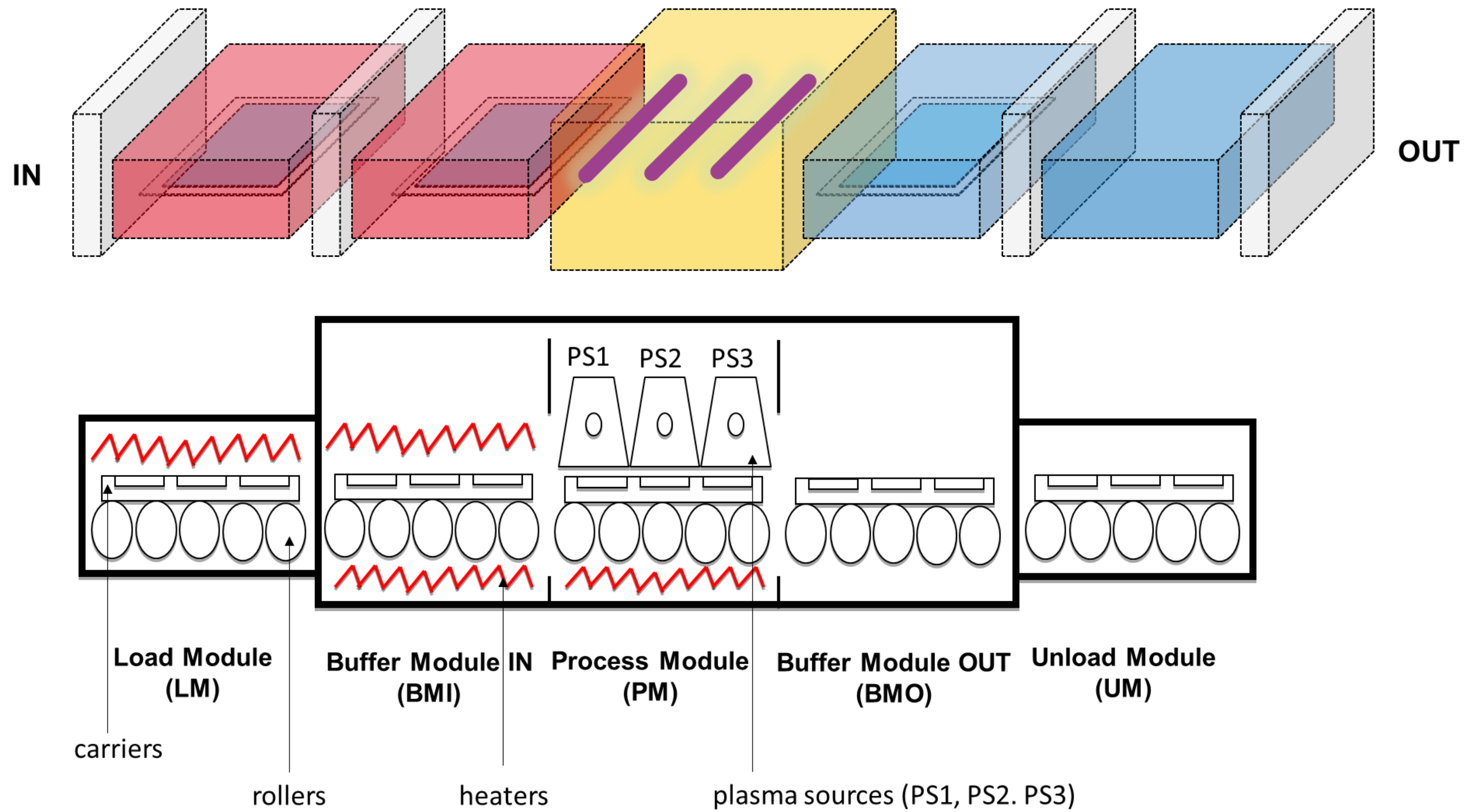

Figure 2.9: Schematic cross section of the inline PECVD system used in this work.

7. Industrial fast-firing

An industrial fast-firing furnace was used to test the high-temperature stability of the films investigated. In general, excellent dielectric passivation results are reported in the literature either in as deposited state or after an optimised post-deposition treatment, e.g. forming gas annealing (FGA), rapid thermal processing (RTP) or the so called *alnealing* process whereby a sacrificial Al layer is deposited onto the dielectric film prior to annealing. In order to validate the excellent passivation results at the solar cell device level, it is extremely important to align the research in accordance to industrial processing conditions by investigating thermal treatments that are actually used for solar cell manufacturing. A typical industrial silicon wafer solar cell fabrication sequence includes a high-temperature firing process (spike anneal with a peak temperature of around 750 - 850 °C for 3-5 seconds) where the front Ag paste is fired through the front dielectric film to contact the emitter of the solar cell. Since the scope of this thesis is mainly to investigate passivation films for industrial application, it was important to investigate the surface passivation performance after an industrial firing process. There were two furnaces used in this thesis a) Ultraflex from Dispatch Industries, USA (typical peak temperature used is 750 °C) and b) Camini from Roth and Rau AG, Germany (typical peak temperature of 880 °C).

Chapter 3: Low-temperature plasma-deposited silicon nitride (SiN_x)

3.1. Introduction

Amorphous hydrogenated silicon nitride (a-SiN_x:H or, briefly, SiN_x) films deposited by plasma-enhanced chemical vapour deposition (PECVD) have become the state-of-the-art antireflection coating for industrial silicon wafer solar cells, as this coating not only reduces reflection losses but simultaneously provides surface passivation for n^+ diffused emitters and hydrogen passivation of bulk defects [9, 103-105]. SiN_x films provide an excellent surface passivation for lowly and moderately doped *p*-type and *n*-type crystalline silicon (*c*-Si), as well as heavily doped *n*-type *c*-Si surfaces (such as n^+ emitters) [9, 19]. With respect to *c*-Si surface passivation, a significant amount of work has been done since last three decades showing the ability of SiN_x films. The best surface passivation results reported to date were obtained using statically (i.e., non-moving substrate) deposited SiN_x films [84, 85, 106-109]. In 2002, Kerr *et al.* demonstrated upper-limit effective surface recombination velocity ($S_{eff.max}$) values of 7.2 and 13.2 cm/s, respectively, on planar *n*-type and *p*-type 1.5 Ωcm *c*-Si wafers passivated by SiN_x films deposited statically at high frequency (13.56 MHz) in a laboratory-type "direct" PECVD reactor. SiN_x films having a refractive index in the 1.9-2.1 range (at λ = 633 nm) were found to perform best [106]. In contrast, for SiN_x films deposited statically with the "remote" PECVD method (using 2.45 GHz microwaves for plasma excitation), the best surface passivation was obtained for Si-rich SiN_x films [107]. For example, in 1996 Lauinger *et al.* achieved $S_{eff.max}$ of 35 and 15 cm/s, respectively, on planar 1-2 Ωcm *p*-type *c*-Si passivated with silicon nitride films having a refractive index of 2.0 and 2.4 [107, 108]. In 2008, using planar 1-Ωcm *n*-type Si wafers, Chen *et al.* demonstrated $S_{eff.max}$ of 7.5 and 3.5 cm/s, respectively, with silicon nitride films having a refractive index of 2.0 and 2.75 [84]. Recently, in 2010, Hameiri *et al.* reported $S_{eff,\,max}$ of 25 cm/s and 7.1 cm/s on 1 Ωcm *p*-type *c*-Si with refractive index of 2.0 and 2.4, respectively [109]. Recently in 2013, Wan *et al.* [85] achieved very low $S_{eff.max}$ of 6.7 and 4.7 cm/s on *p*- and *n*-type Si respectively using statically deposited SiN_x films using lab-type reactor in as deposited state. While all these results involving laboratory-scale static deposition reactors are undoubtedly excellent, more research and progress is needed for industrial application where dynamically deposited (i.e. moving substrate) plasma SiN_x films are of key interest. This is because of its very high throughputs

(> 2000 wafers/hour) that is essential for continuous cost saving strategies. However, dynamically deposited plasma SiN_x films have so far only achieved a modest level of surface passivation, although such SiN_x films are widely used in silicon wafer solar cell manufacturing [88, 90, 110, 111]. Further reduction of surface recombination velocities using SiN_x deposited in an industrial inline PECVD reactor that are industrially firing stable is becoming very important for realizing industrial high-efficiency silicon wafer solar cells as the industry adapts increasingly thinner substrates.

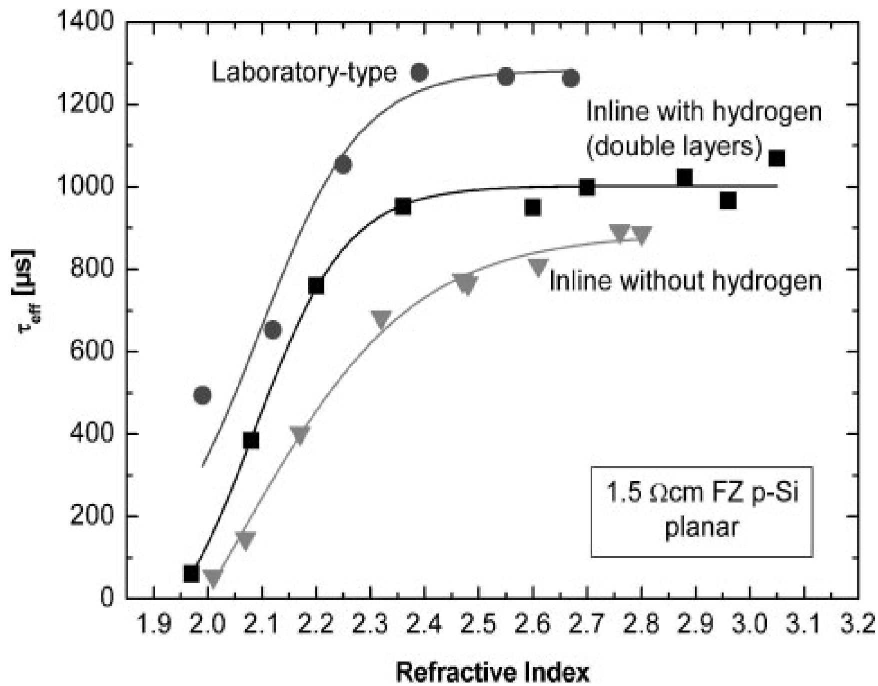

Figure 3.1: Effective minority carrier lifetime (τ_{eff}) of a symmetrical SiN_x passivated *p*-type Si wafer as a function of refractive index at wavelength of 633 nm. The graph is taken from Ref. [110] for their optimised static and dynamic deposition of plasma SiN_x.

During early 2000 due to this specific interest of industrial application, development and optimisation of dynamically deposited plasma SiN_x layers for solar cell application were performed. In fact, Moschner *et al.* compared the passivation performance for their optimised laboratory-type (static deposition) and inline PECVD reactors (dynamic deposition) [110]. A clear difference in surface passivation was observed between static and dynamic deposition systems (see Figure 3.1 taken from Ref. [110]). SiN_x films with lower refractive index films ($n < 2.2$), which are useful for solar cell application [112] showed a relatively poor surface passivation when deposited in the inline reactor (although little improvement was observed with addition of hydrogen). Using these industrial PECVD reactor, as-deposited SiN_x films on 1.5 Ωcm *p*-type Si wafers provided $S_{eff.max}$ of 200 ± 50 cm/s for a refractive index of 1.9-2.1 and $S_{eff.max}$ of

20 cm/s for a refractive index of > 2.4 [110, 111]. However, in 2004 Winderbaum *et al.* demonstrated very low $S_{eff.max}$ values of 11.8 cm/s (S_{eff} ~ 7.5 cm/s assuming a bulk lifetime of 3.38 ms) on 1.4 Ωcm *p*-type Si wafers passivated by inline silicon nitride films with a refractive index of 1.9-2.0 after a rapid thermal anneal (RTA) in forming gas at 650 °C. However, it was reported that this was one-off occurrence, several samples repeatedly reached $S_{eff.max}$ of 18.8 cm/s after a 10-second anneal at 700 °C. Similar films gave $S_{eff.max}$ of 75 cm/s after annealing in an industrial fast firing furnace [90]. These results indicate that industrial PECVD reactors are actually capable of producing excellent surface passivation quality that matches that of laboratory size machines, after an optimised annealing is performed. Although dynamically deposited plasma SiN_x were studied to some extent during the 2000s, excellent silicon surface passivation results matching laboratory-type static deposition systems was still lacking. It is important to note that given the industrial relevance and application of dynamically deposited plasma PECVD SiN_x for mass-production of crystalline silicon solar cells, a further improvement is imperative. In 2010, when SERIS cleanroom was ready for operation; development and progress in high-quality surface passivation using plasma SiN_x film was identified as a crucial step. Firstly, it is of high importance close the gap in surface passivation performance between the static and dynamic depositions required to improve solar cell efficiency in industries. Secondly, it is equally important to have high-levels of surface passivation after high temperature industrial firing process instead of after as-deposited conditions or optimised annealing. These two points serves as the motivation towards working on dynamically deposited plasma SiN_x in this chapter for the thesis.

3.2. Process optimisation

In order to achieve optimum surface passivation properties, a rigorous process optimisation is essential. Some researchers have examined an extensive process parameter variation, analysing their response using statistical software like Minitab or Jump. For example for PECVD SiN_x, this was already studied extensively in Refs. [107, 108, 113-115]. In this thesis, the best known method (BKM) – the recipe recommended by the equipment manufacturer - served as the starting point process recipe for the PECVD SiN_x. This process recipe was considered the most optimised recipe for the SiN_x deposition in this type of PECVD system, which is outlined in Table 3.1. As can be seen from Table 3.1, the main process parameters that can be varied are: 1) deposition temperature, 2) chamber pressure, 3) plasma power, 4) gas ratio and

5) total gas flow. Out of these five process parameters, the plasma power and the deposition temperature were identified to be the most significant process parameters responsible for optimisation of surface passivation. Shiny polished {100} *n*-type (~1-2 Ωcm) float-zoned *c*-Si wafers with a thickness of ~280 µm and a diameter of 100 mm were used for initial optimisation.

Table 3.1. Inline PECVD deposition parameters and film properties of SiN_x that served as baseline recipe. This film yields refractive index of 2.03 and thickness of 70 nm.

Process gas	Total gas flow (sccm)	Gas ratio (NH_3/SiH_4)	Deposition temperature (°C)	Reactor pressure (mbar)	Plasma power (W)
$SiH_4 + NH_3$	1035	3.5	400	0.25	2500

Prior to the SiN_x deposition, the samples received a standard RCA cleaning procedure. The SiN_x films were dynamically deposited onto each side of the Si wafer (in two separate runs), using a commercial inline microwave-powered PECVD reactor (Roth & Rau, SiNA-XS). The deposition temperature was varied from 300 to 550 °C with an interval of 50 °C and $S_{eff,max}$ was calculated as shown in Figure 3.2 (a). It was observed that 450 °C resulted in the best surface passivation ($S_{eff,max}$ ~16 cm/s), improving the surface passivation by almost a factor of two compared to the baseline 400 °C process ($S_{eff,max}$ ~40 cm/s). It should be noted that a variation of temperature changes the optical properties of the films (i.e. increasing temperature reduces thickness, with a minor increase in refractive index). The carrier speed was adjusted to keep the thickness almost constant at 70 nm. The second important parameter was the plasma power. This was varied from 1500 to 3500 W (in 500 W steps) and the $S_{eff,max}$ was calculated as shown in Figure 3.2 (b). The trend indicates that higher plasma power yields better surface passivation. A plasma power of 3500 W gave the best surface passivation ($S_{eff,max}$ ~14 cm/s) compared to the baseline 2500 W process ($S_{eff,max}$ ~20 cm/s). It should be noted that variation of the plasma power significantly changes the films' optical properties (thickness increases and refractive index reduces with increasing plasma power). The carrier speed was adjusted to keep the thickness almost contact at 70 nm and the gas ratio was adjusted to keep the refractive index at around 2.05. The optimised recipe (same as Table 3.1, but with a temperature of 450 °C and a plasma power of 3500 W) was investigated on both *p*- and *n*-type silicon as a function of refractive index (at wavelength 633 nm). The $S_{eff,max}$ values are presented in Figure 3.3. As evident, for the relevant refractive index (n) for PV application i.e. $n < 2.3$ the $S_{eff,max}$ is higher than

90 cm/s for *p*-type Si (whereas $S_{eff,max}$ < 10 cm/s was reported for static deposition system) [84, 85, 108, 116]. Similarly higher $S_{eff,max}$ was observed even for *n*-type Si for $n < 2.3$.

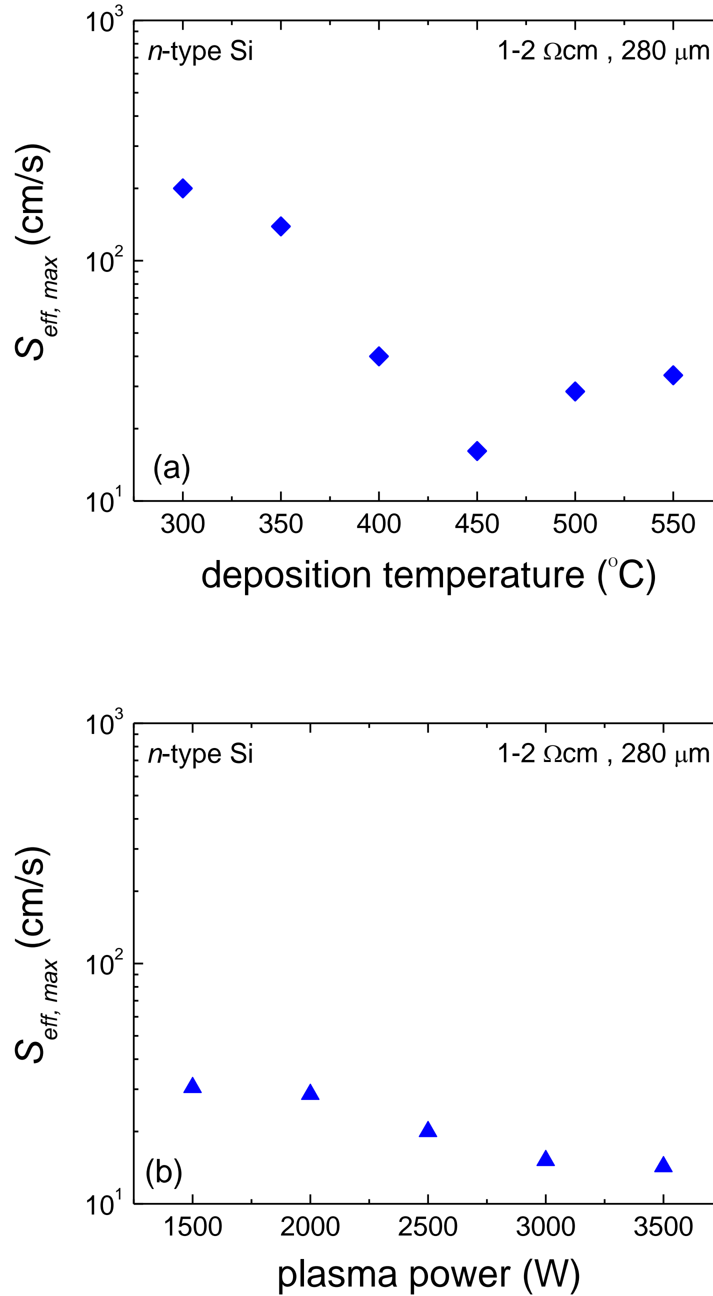

Figure 3.2: $S_{eff.max}$ at $\Delta n = 1\times10^{15}$ cm^{-3} as a function of the most important process parameters **(a)** deposition temperature and **(b)** plasma power of the SiN_x films obtained on low-resistivity undiffused *n*-type FZ *c*-Si.

These optimised results (presented in Fig 3.2) were inferior to the best published results available in the literature that are specifically developed in lab-type reactors.

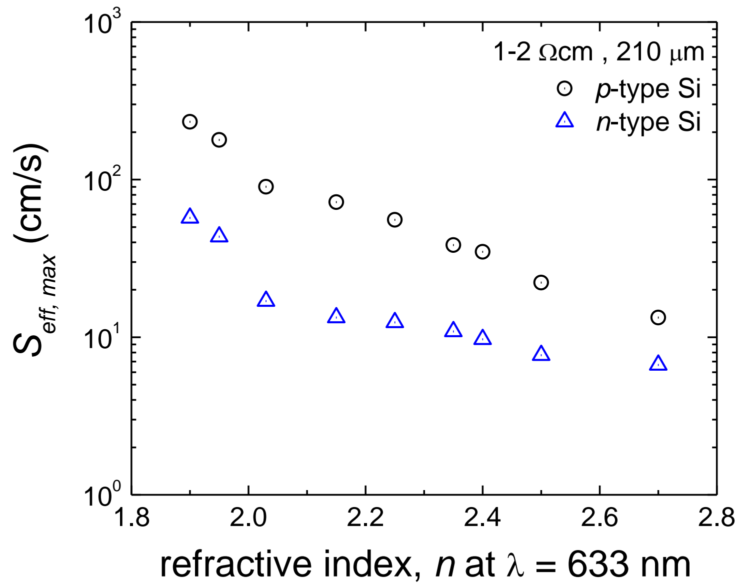

Figure 3.3: $S_{eff.max}$ at $\Delta n = 1\times10^{15}$ cm^{-3} as a function of refractive index of the SiN_x films obtained on low-resistivity undiffused *p*- and *n*-type *c*-Si. Note: The $S_{eff.max}$ data of this work are the average values from five samples.

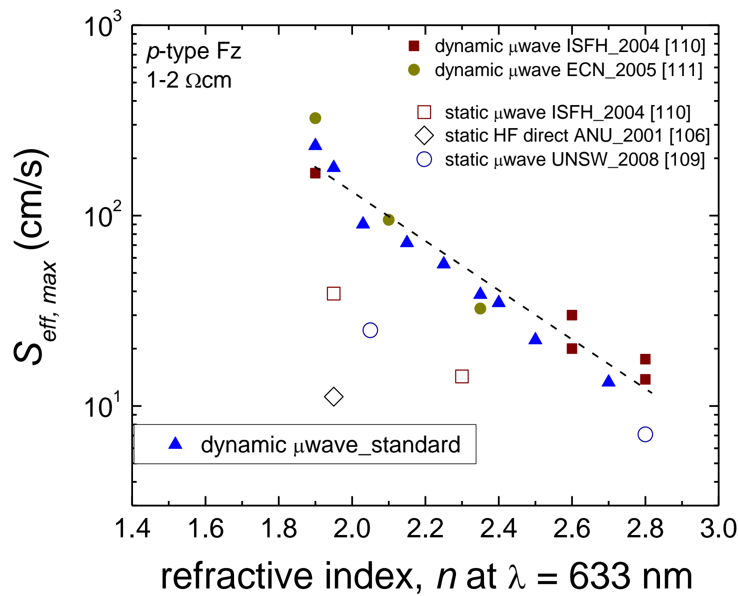

Figure 3.4: $S_{eff.max}$ at $\Delta n = 1\times10^{15}$ cm^{-3} as a function of refractive index of the as-deposited SiN_x films for 1.5 Ω.cm *p*-type FZ wafers. The dotted line represents the trend observed for the results from the inline reactors (solid symbols). The open symbols represent the results obtained in the lab-type reactors.

Figure 3.4 summarises the crystalline silicon surface passivation performance for the best reported results on 1-2 Ωcm *p*-type Si using inline reactors (dotted line) in as-deposited conditions compared to best results reported till date by static deposition systems (again for as-deposited conditions). All optimised surface passivation results using inline reactors (including results from Fig 3.2) so far showed similar results for inline reactors in agreement with other authors [110, 111] however as discussed earlier the results from lab-type reactors [106, 109, 110]) were superior. This clearly indicated further improvement was needed in regards to surface passivation using inline deposition systems.

3.2.1. Impact of spatial separation of plasma sources

As an exercise towards process optimisation, the study of the impact of neighbouring plasma sources was never done or specifically reported in the literature. After having optimised the main deposition parameters, it was now required to study the so-called parameter "impact of plasma source configuration". The different plasma source configurations are illustrated in Fig 3.5(a) (also refer to Fig. 2.9 for more details). The surface passivation results for different plasma source configurations are shown in Figure 3.5(b). Interestingly, this turned out to be the most important parameter as is evident from Fig 3.5: SiN_x deposition with the first plasma source (PS1) resulted in the lowest $S_{eff,max}$ of 10.6 cm/s (i.e., about 9 times lower surface recombination velocity compared to the standard three plasma source configuration (PS1+2+3) giving $S_{eff,max}$ of 90 cm/s. The use of two plasma sources either sequential (PS1+2 or PS2+3) or separated (PS1+3) also resulted in significantly improved silicon surface passivation compared to results obtained when all three plasma sources (PS1+2+3) were used together. Especially PS1+3 resulted in passivation results almost as good as PS1 with $S_{eff,max}$ of 12.8 cm/s. The superior results with PS1 can be understood from the fact that the film growth is continuous beneath a particular plasma source (the influence of segmented plasma as is the case for multiple plasma source is absent in this case). However, there is small difference in results between the use of PS1 or PS2 or PS3. For PS2 and PS3 the substrate travels a longer distance in the reactor to reach the respective plasma source compared to PS1, and hence can be subjected to (unintentional) surface contamination that affects the silicon surface passivation results. Although the best result is reported for PS1, it should be noted that the throughput for such a process is very low, which is unacceptable for industrial application. The surface passivation quality of a SiN_x film depends significantly on the initial 20-30 nm of film thickness,

as this part of the film determines both the interface quality as well as the amount of fixed charge in the film [117-119].

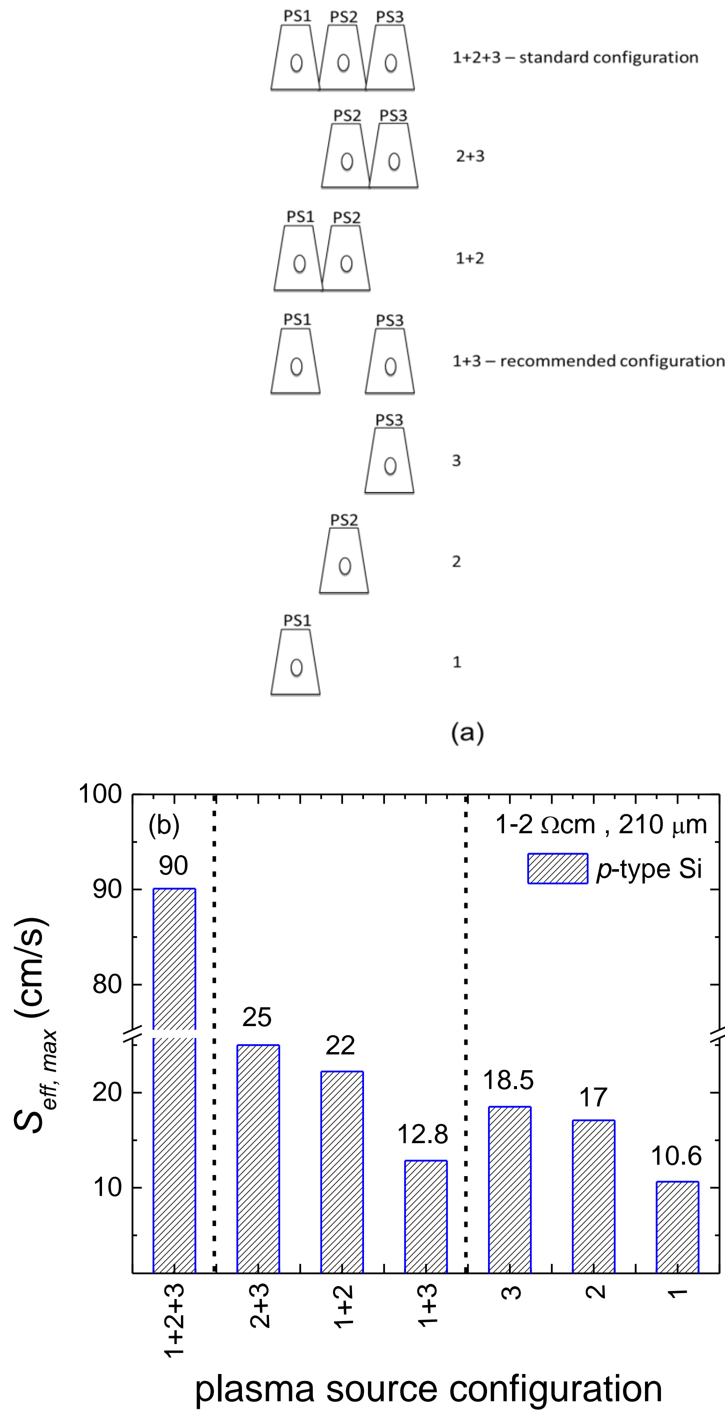

Figure 3.5: **(a)** Plasma source configurations investigated in this thesis. **(b)** Measured $S_{eff.max}$ at Δn = 1×10^{15} cm^{-3} as a function of the plasma source configuration, for SiN_x films deposited on *p*-type *c*-Si wafers. Note: The $S_{eff.max}$ data are the average values from five samples.

Thus the use of the first plasma source is crucial as it provides better interface quality and less potential contamination. It was shown experimentally before that the positive charge density in PECVD SiN_x film saturates after a so-called threshold thickness of 20-30 nm [118]. Hence, it was understood that the growth of first 20-30 nm should be uninterrupted for maximum positive charge density in the film. Since the target film thickness was 70 nm (because of its optimum optical performance [112]), the use of two plasma sources seemed appropriate as this means the thickness of each SiN_x film (from each plasma source) is ~35 nm. Considering that the use of PS1 is essential, PS1+2 and PS1+3 were the two choices left. The PS1+3 plasma source configuration resulted in better surface passivation, as can be seen in Fig 3.5. The results of Fig. 3.5 are among the key results obtained in this thesis in regards to surface passivation using a dynamically deposited PECVD SiN_x film. Remarkably, optimising the plasma source configuration (especially with PS1+3) led to a dramatic 9-fold improvement of the surface passivation quality compared to the standard reactor configuration. This is a proprietary work, which lead to a patent that is converted to PCT and is published as Ref. [120].

Figure 3.6 shows the $S_{eff.max}$ values obtained in this work on *p*-type wafers as a function of the refractive index of the as-deposited SiN_x films. For comparison, the best results published by other groups for such samples are also shown in the graph. The lower dashed line represents the trend achieved in this study, whereas the upper dashed line represents the trend previously reported by other groups for industrial SiN_x films deposited dynamically onto *p*-type Si wafers. As a matter of fact, for a large refractive index range, our $S_{eff.max}$ values are as good as, or even better than, the best values reported to date for statically deposited SiN_x films. Static deposition systems generally give better surface passivation results when compared to the dynamic deposition systems simply because the plasma conditions at the sample surface are constant and laterally uniform during the film deposition process. During a dynamic process, as a result of the moving substrate, the plasma conditions at the sample's surface change as it moves into, goes through, and then out of the plasma region. As a consequence of these changing plasma conditions, the resulting surface passivation quality is usually lower than for optimised static depositions. However, the main advantage of dynamic systems is that they can be used for inline processing, which is capable of very high throughputs. This is obviously beneficial from a manufacturing point of view.

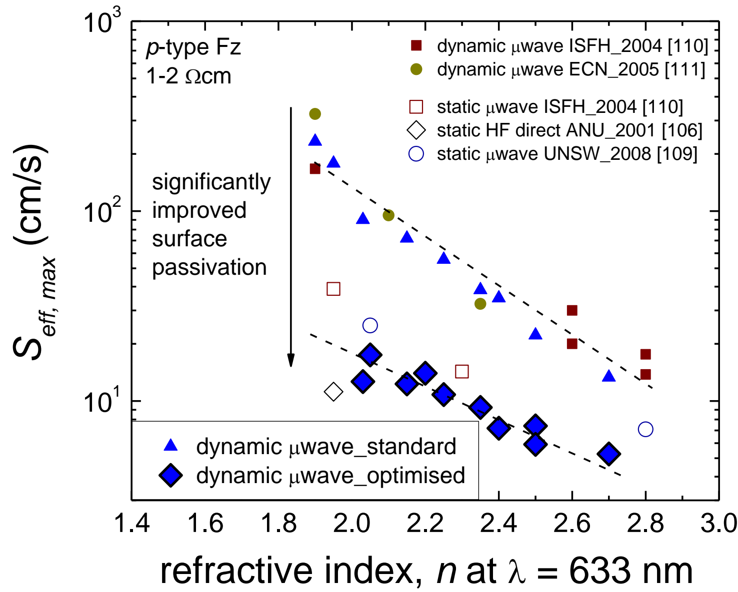

Figure. 3.6: $S_{eff.max}$ at Δn = $1{\times}10^{15}$ cm^{-3} as a function of refractive index of the as-deposited SiN_x films for *p*-type *c*-Si wafers. The results obtained in this work (triangles) are compared to the best published results for as-deposited inline remote plasma SiN_x films (solid symbols) [110, 111]. Also shown, for comparison, are the best reported laboratory results for statically deposited SiN_x films (open symbols) [106-109]. However, it should be noted that an optimised post-deposition annealing can result in even better surface passivation for all studies presented here. Note: The $S_{eff.max}$ data of this work are the average values from five samples.

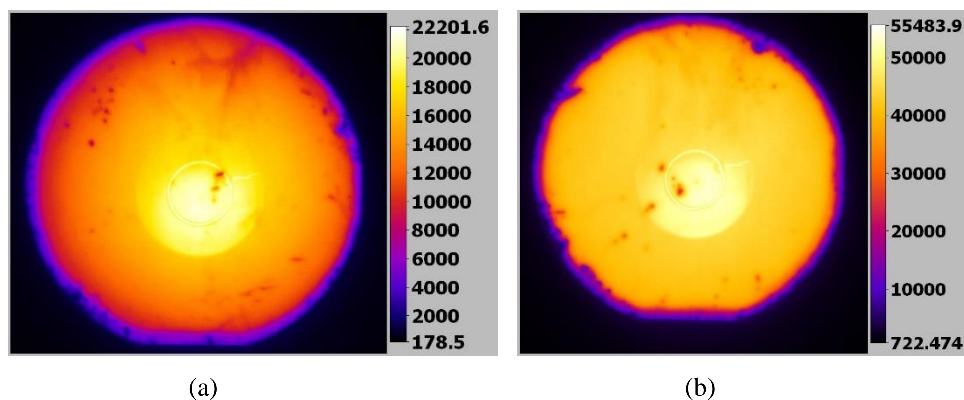

Figure 3.7.: Spatially resolved photoluminescence (PL) images of the SiN_x deposited on 1-2 *p*-type Fz Si as used in Fig. 3.6, **(a)** SiN_x deposited using 'standard' plasma source configuration, **(b)** SiN_x deposited using 'optimised' plasma source configuration. Refractive index of 2.03 was selected for this.

Furthermore the level of surface passivation was verified by spatially resolved photoluminescence (PL) imaging, in addition to carrier lifetime measurements. SiN_x deposited using optimised plasma configuration [Fig. 3.7 (b)] clearly shows significantly improved surface passivation as evident from very high PL counts (with brighter contrast) compared to SiN_x deposited using standard plasma source configuration [Fig. 3.7 (a)].

3.2.2. Surface passivation mechanism

The Si-SiN_x interface generally exhibits a midgap interface state density ($D_{it,midgap}$) in the range of 10^{11} to 5×10^{12} $eV^{-1}cm^{-2}$, which is normally one order of magnitude higher than the Si-SiO_2 interface [117-119, 121, 122]. Interestingly, no D_{it} results are so far reported in the literature for inline PECVD SiN_x. In order to understand the significant improvement in surface passivation as shown in Figs. 3.5, 3.6 and 3.7, it was important to measure the electronic interface properties. Contactless corona-voltage measurement were performed to extract positive charge density and interface state density and shown in Fig. 3.8 (technique explained in Chapter 2).

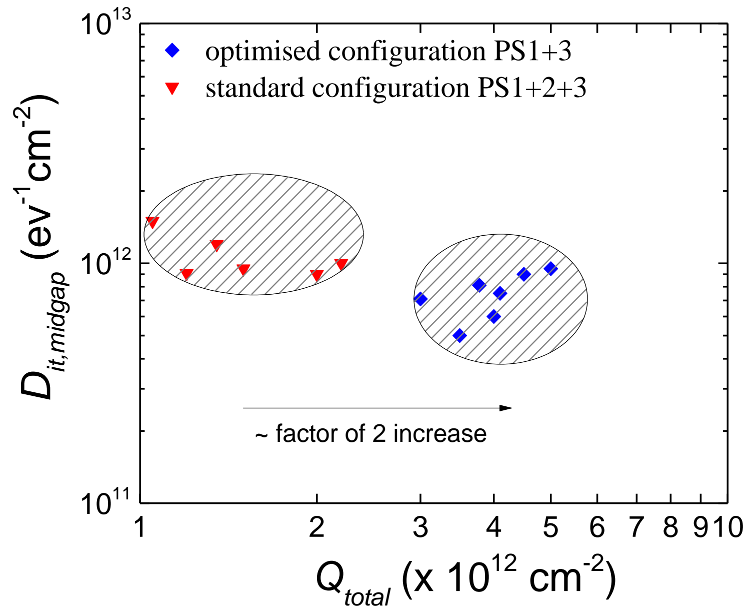

Figure 3.8: Measured $D_{it,midgap}$ as a function of positive charge density for standard (PS1+2+3) and optimised (PS1+3) plasma source configuration.

Using standard configuration, the midgap D_{it} was found to be relatively higher in the range of $8\text{-}10 \times 10^{11}$ $eV^{-1}cm^{-2}$ compared to other reported values in the literature (static

depositions) i.e. ~ 3×10^{11} $eV^{-1}cm^{-2}$ [85, 116]. This forms (partly) the reason for inferior passivation results using dynamic depositions in standard plasma source configuration. It should be noted that $D_{it,midgap}$ a critical parameter as it indicates the interface quality and is highly sensitive to deposition conditions. It can be possible to further improve D_{it} by process optimisation. With the optimised plasma source configuration, PS1+3 (after Fig. 3.5), the $D_{it,midgap}$ values are measured to be as low as 5-6×10^{11} $eV^{-1}cm^{-2}$, which is a clear improvement compared to standard configuration. This is considered one of the reasons for improved surface passivation.

The surface passivation mechanism of PECVD SiN_x strongly depend on the field-effect passivation provided by the high positive charge density near the interface (> 10^{12} cm^{-2}) [20, 123, 124]. A high positive charge density is very beneficial for surface passivation particularly for *n*-type Si that drives the surface under accumulation. Such high positive charge density drives moderately-doped *p*-type Si surface under inversion, which also helps for reducing recombination at the surface (see Figs. 2.3 and 2.4). Remarkably, the measurement revealed that for the SiN_x film deposited using PS1+3 (optimised configuration) has a significantly higher (~2 times) positive charge density compared to PS1+2+3 (standard configuration) as evident from Fig 3.8. In addition to the improved interface state density, this explains and confirms that the significantly improved surface passivation is predominantly due to an improved field-effect passivation and, to a lesser degree, to an improved chemical passivation.

3.3. Surface passivation of moderately-doped *c*-Si

Figure 3.9 shows the injection level dependent τ_{eff} and $S_{eff.max}$ values for moderately doped *p*-type and *n*-type Si wafer passivated by either a nearly-stoichiometric SiN_x film (n = 2.05) or a Si-rich SiN_x film (n = 2.5). In the as-deposited condition, nearly-stoichiometric SiN_x films exhibit $S_{eff.max}$ of 17.5 cm/s and 14.7 cm/s for *p*- and *n*-type FZ Si, respectively. After an industrial firing process (peak temperature > 800 °C) the $S_{eff.max}$ values reduced to 11.7 cm/s and 9.5 cm/s for *p*- and *n*-type FZ Si, respectively, indicating that the surface passivation provided by the SiN_x film is firing stable (or even improved due to the firing process). This is an important result as it demonstrates that excellent surface passivation can be achieved using an inline plasma silicon nitride film on large-area Si wafers after an industrial firing process, a result that is rarely found in the literature.

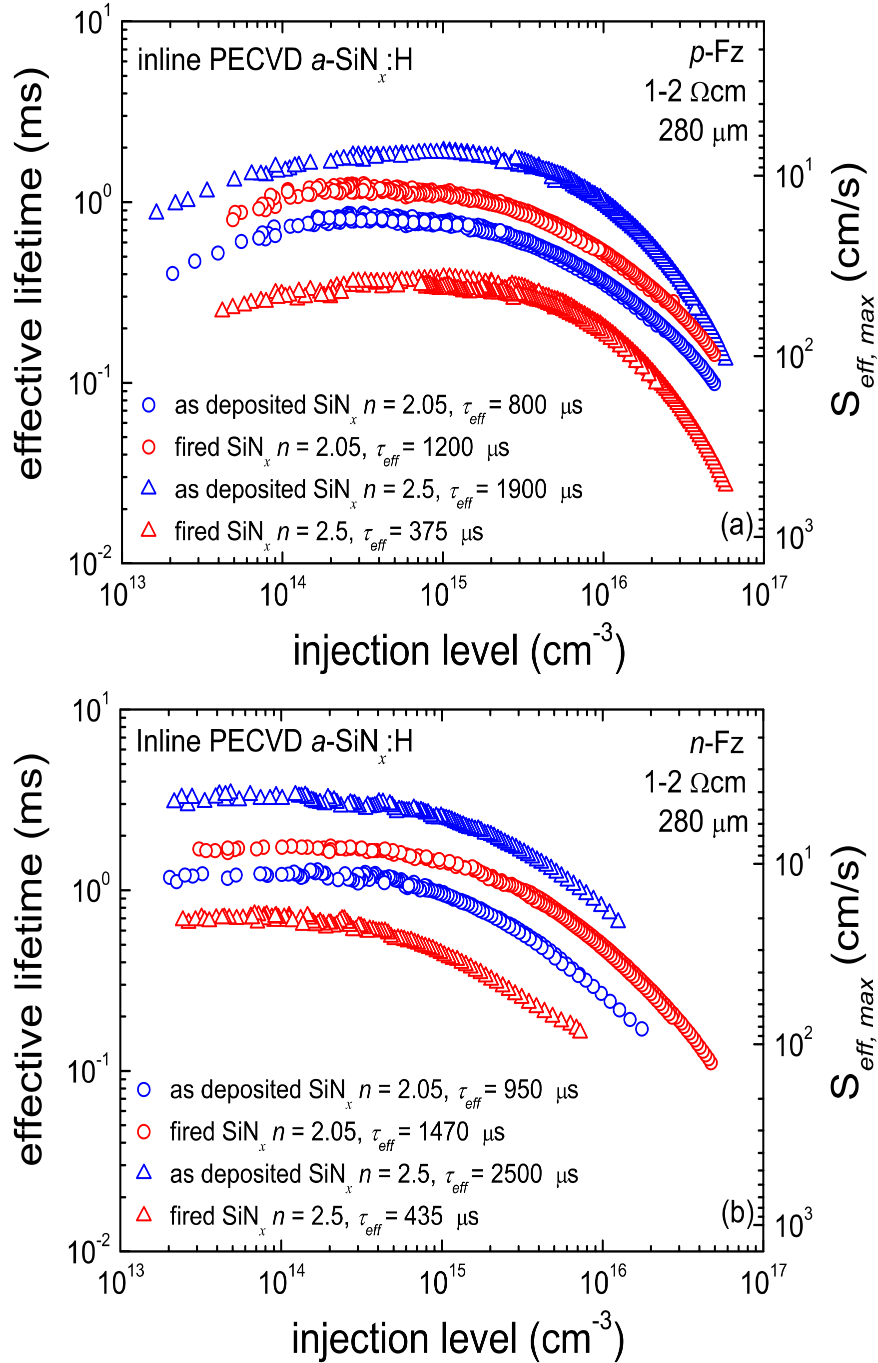

Figure. 3.9: Injection level dependent effective carrier lifetime and maximum effective surface recombination velocity for **(a)** *p*-type and **(b)** *n*-type c-Si wafers passivated on both sides with either a nearly-stoichiometric SiN_x film (n = 2.05) and Si-rich SiN_x film (n = 2.5). The results are shown for as-deposited state and after industrial-firing. The τ_{eff} values corresponds to an injection level of $\Delta n = 10^{15}$ cm^{-3} shown in the legend.

In one of the previous studies similar high-quality results ($S_{eff.max}$ of 18.8 cm/s on *p*-type FZ Si of similar resistivity) were achieved using nearly-stoichiometric dynamically deposited SiN_x films after a 10-second rapid thermal anneal (RTA) in forming gas at

700 °C. However, after industrial firing at this value increased to $S_{eff.max}$ of 75 cm/s [90]. It is evident from Figs. 3.6 and 3.9 that the $S_{eff.max}$ values reported in this work demonstrate a significant improvement over the previously published results for dynamically deposited SiN_x films, both for the as-deposited condition and after industrial firing, which is of relevance for industrial screen-printed high-efficiency silicon wafer solar cells.

Table 3.2: Measured τ_{eff} and $S_{eff.max}$ obtained for {100} *p*-type and *n*-type (~1-2 Ωcm) *c*-Si wafers with a thickness of ~280 μm passivated on both sides by as-deposited and after industrially-fired inline PECVD SiN_x films. Max. τ_{eff} is the maximum measured effective lifetime value of Fig. 3.9, followed by its corresponding S_{eff} and $S_{eff.max}$ values.

Doping type	*n* at λ = 633 nm	Condition	τ_{eff} at 10^{15} cm^{-3} (μs)	S_{eff} (cm/s)	$S_{eff.max}$ (cm/s)	Max. τ_{eff} (μs)	S_{eff} (cm/s)	$S_{eff.max}$ (cm/s)
p	2.05	As-deposited	800	13.4	17.5	900	11.4	15.6
p	2.05	Fired	1200	7.5	11.7	1260	7.0	11.1
p	2.50	As-deposited	1900	3.2	7.4	1900	3.2	7.4
p	2.50	Fired	375	33.2	37.3	375	33.2	37.3
n	2.05	As-deposited	950	12.8	14.7	1200	9.7	11.7
n	2.05	Fired	1470	7.6	9.5	1700	6.3	8.2
n	2.50	As-deposited	2500	3.7	5.6	3300	2.3	4.2
n	2.50	Fired	435	30.2	32.2	735	17.1	19.0

In this case Si-rich SiN_x film showed outstanding surface passivation results in as-deposited conditions with $S_{eff.max}$ values of 7.4 cm/s and 5.6 cm/s for *p*- and *n*-type FZ Si, respectively. Unlike the nearly-stoichiometric SiN_x film, the surface passivation provided by the Si-rich SiN_x film degraded significantly due to the firing process, as $S_{eff.max}$ increased to 37.3cm/s and 32.2 cm/s, indicating thermal instability. This is very important result as these are rarely found in literature especially for dynamically-deposited SiN_x film. A higher Si-N bond density in nearly-stoichiometric SiN_x is believed to be responsible for its higher thermal stability [125, 126]. Table 3.2 summarizes the measured τ_{eff}, S_{eff} and $S_{eff.max}$ obtained for both *p*-type and *n*-type *c*-Si wafers with a thickness of ~280 μm passivated on both sides by as-deposited and after industrially-fired inline PECVD SiN_x films. The S_{eff} values assume only intrinsic recombination in the bulk under low-injection (τ_{bulk} of 3.38 ms for 1.5 Ωcm *p*-type Si and 7.2 ms for 1.5 Ωcm *n*-type Si, after Kerr *et al.* [106]), while the $S_{eff.max}$ values

assume $\tau_{bulk} = \infty$, which corresponds to upper-limit effective surface recombination velocities.

The long-term stability of the fabricated samples was also investigated, by measuring the effective lifetime after storage of the samples for more than two years under indoor ambient conditions. These tests confirmed that the effective lifetimes of the samples remained constant over a period of two years. The uniformity of the SiN_x thickness over the entire area of the wafers was confirmed to be better than ± 3% (as measured by spectroscopic ellipsometer). Furthermore, using photoluminescence imaging, the surface passivation quality was also confirmed to be relatively uniform across the wafer [see Fig. 3.7(b)].

In order to understand the improvement is surface passivation after firing, contactless corona-voltage measurements were carried out. SiN_x films after firing revealed a large negative V_{fb} (-14 V), indicating a high positive charge density in the SiN_x film near the interface. Table 3.3 summarizes the Q_{total} and $S_{eff.max}$ data obtained for SiN_x in this work compared to other remote plasma SiN_x films. The Q_{total} of $+8\times10^{12}$ cm^{-2} found in this work for nearly stoichiometric SiN_x films is significantly higher than previously published values obtained for as-deposited SiN_x films using a similar remote-plasma PECVD [127, 128] technique. Theoretically it was shown that, for high charge densities (> 5×10^{11} cm^{-2}), the surface recombination rate (U) is inversely proportional to the square of the fixed charge density (Q_f) i.e. $U \approx 1/|Q_f|^2$ [64]. Therefore, a slight increase or decrease in charge is expected to have a strong influence on the recombination rate. Hence, improved surface passivation obtained in this work can be attributed to a relatively higher density of positive charge, thereby enhancing the field-effect passivation by the SiN_x films. However, some experimental studies indicate that other effects also play an important role for the recombination rate when an electric field is applied externally (e.g. via a gate voltage or corona charging) [53, 62].

A decrease of Q_{total} to about 4.3×10^{12} cm^{-2} is observed after a standard industrial firing at ~800 °C. Such decrease in charge density was also observed by other authors [127]. This can be due to re-construction of the bonding network in the nitrides (incorporation of oxygen or removal of hydrogen while annealing) or/and growth of an interfacial silicon oxynitride (SiO_xN_y) film between the *c*-Si wafer and the SiN_x film. Both effects can modify one of the charged states (K^+ or K^-) of the amphoteric K centres (a dominant defect when consisting of a Si atom back bonded to three N atoms) [19, 70, 124, 129-131] that can explain the decrease in fixed charge. Another possible mechanism can be

due to de-trapping of holes from the K^+ centres and charge carrier transport across the interface. A similar concept was shown by Weber *et al.* for annealed negatively charged SiN_x, whereby the negative charge resulted from corona charging [132]. This is probably one of the reasons behind the improved passivation of SiN_x-passivated boron emitters upon prolonged annealing of the samples [86].

Table 3.3: Q_{total} and $S_{eff.max}$ values of SiN_x passivated *n*-type *c*-Si surfaces as derived from contactless corona-voltage and photoconductance decay measurements. N.A. means that the data is not available from the reference.

Remote plasma SiN_x films	Q_{total} (10^{12} cm^{-2})	$S_{eff.max}$ (cm/s)
Dynamic SiN_x (n = 2.0), as deposited	+ 8.4	14.7
Dynamic SiN_x (n = 2.0), industrially fired	+ 4.3	9.8
Static SiN_x (n = 1.94), as deposited [127]	+ 2.3	30
Static SiN_x (n = 1.94), industrially fired [127]	+ 1.5	25
Static SiN_x (n = 2.0), as deposited [128]	+ 0.65	N.A.
Static SiN_x (n = 2.0), as deposited [128]	+ 0.58	N.A.

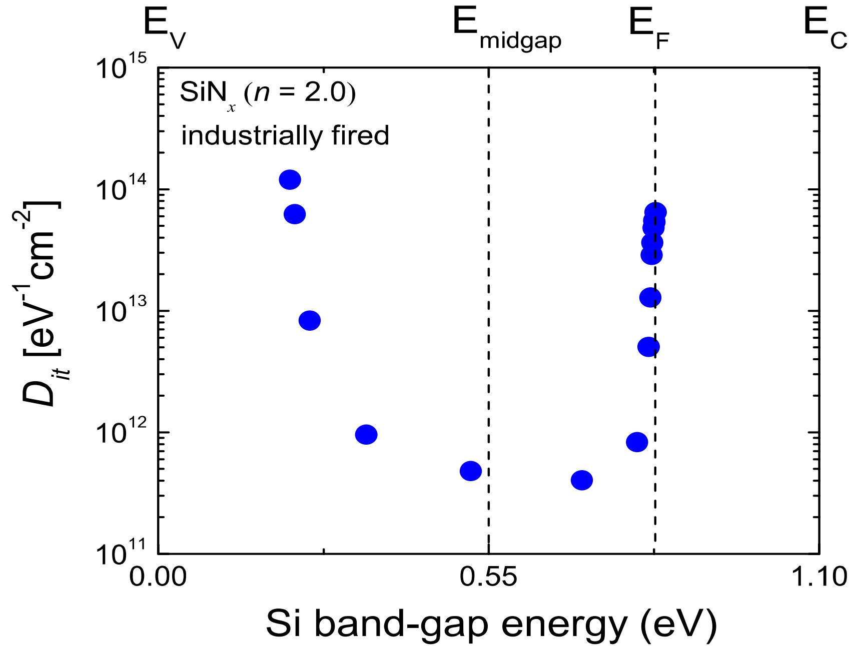

Figure 3.10: Measured *c*-Si/SiN_x interface state density (D_{it}) as a function of the bandgap energy for an industrially-fired PECVD SiN_x (n = 2.05) on *n*-type doped *c*-Si wafer.

The improved surface passivation of the industrially fired samples, despite their reduced positive charge density, can be attributed to a reduced interface state density (D_{it}) at the Si/SiN_x interface. This may be caused by hydrogen diffusion towards the

interface and thus saturation of dangling bonds ("*chemical passivation*"). The as-deposited nitrides (both nearly-stoichiometric and Si-rich) suffered from high leakage current densities. As a result, these nitrides could not hold sufficient corona charge to probe the midgap energy levels during the corona charging experiments, which is required for the extraction of D_{it}. However, the industrially fired samples had significantly lower leakage current densities, which enabled the extraction of their D_{it} to be less than 5×10^{11} eV^{-1}cm^{-2} at midgap energies, as shown in Figure 3.10.

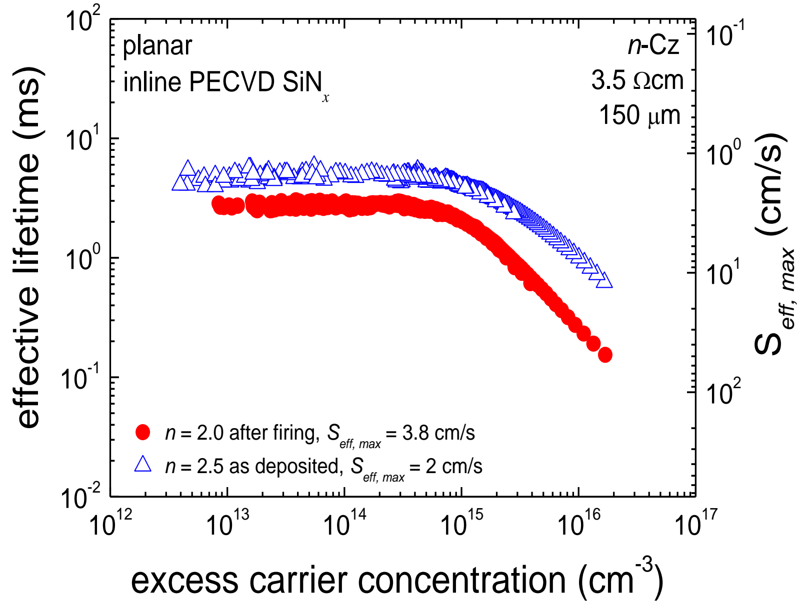

Figure 3.11: Injection level dependent effective carrier lifetime and maximum effective surface recombination velocity for *n*-type Cz wafers passivated on both sides with either a nearly-stoichiometric SiN$_x$ film (n = 2.05) and Si-rich SiN$_x$ film (n = 2.5). The $S_{eff,\,max}$ values correspond to an injection level of $\Delta n = 10^{15}$ cm^{-3} as shown in the legend. $S_{eff,\,max}$ values assume $\tau_{bulk} = \infty$, which corresponds to upper-limit effective surface recombination velocities.

Several *n*-type Cz Si of high resistivity (3.5 Ωcm) wafers with a thickness of ~150 μm were also used to study surface passivation. Figure 3.11 shows the injection level dependent effective carrier lifetime and $S_{eff,max}$ results for *n*-type Cz Si wafers passivated by either a industrially-fired nearly-stoichiometric SiN$_x$ film (n = 2.05) or a Si-rich SiN$_x$ film (n = 2.5). Ultra-low $S_{eff,max}$ values of 3.8 cm/s and 2.0 cm/s are obtained for a nearly-stoichiometric SiN$_x$ film (n = 2.05) or a Si-rich SiN$_x$ film (n = 2.5), respectively. Previously in Fig. 3.9, high quality surface passivation results on 1.5 Ωcm float-zoned silicon was demonstrated [133]. The results in Fig 3.11 serves as an extension of the previous work demonstrating that remarkable surface passivation can be achieved

using an inline plasma silicon nitride film most importantly on large-area Cz Si wafers after an industrial firing process.

3.4. Surface passivation of heavily-doped *n*-type *c*-Si

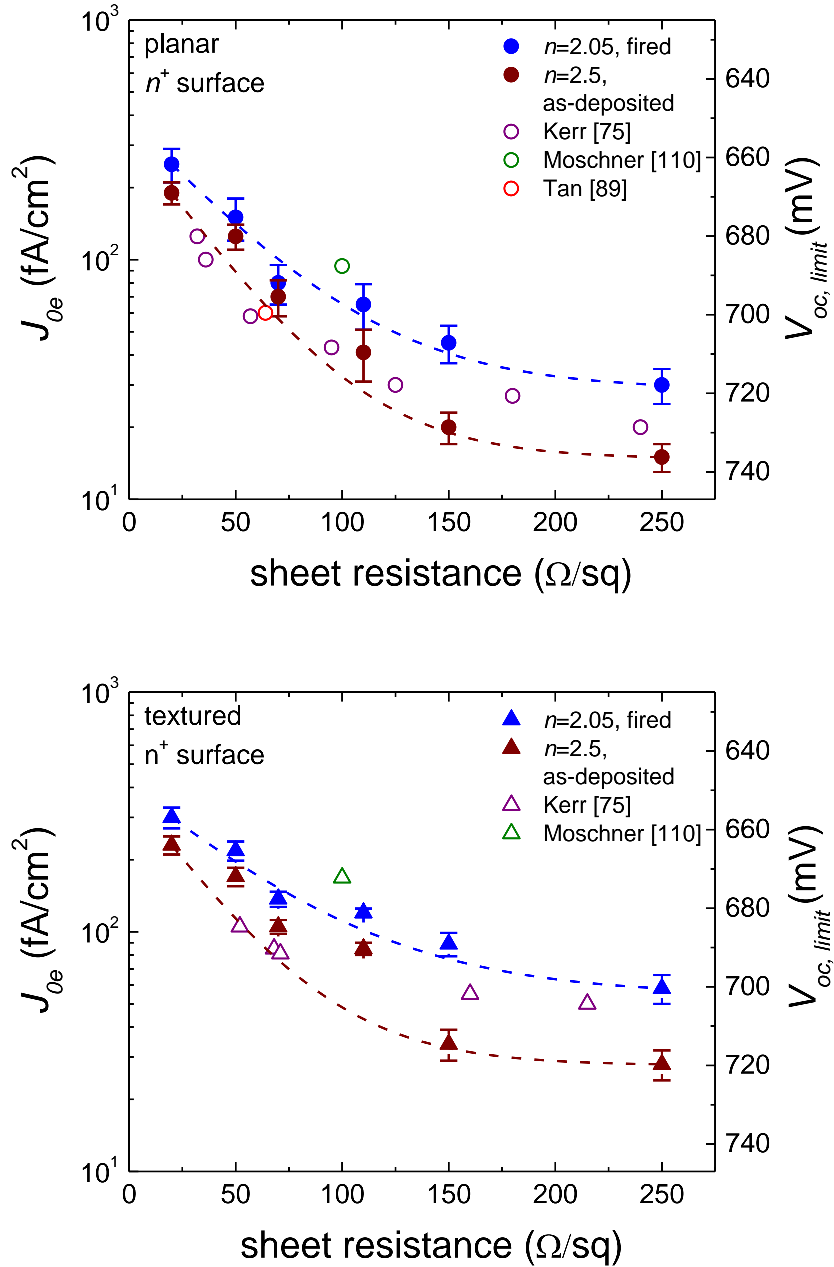

Figure 3.12 (a): Measured J_{0e} as a function of the sheet resistance of planar phosphorus-diffused n^+ layers. The emitters were passivated either by an industrially-fired nearly-stoichiometric SiN_x film (n = 2.05) or Si-rich SiN_x film (n = 2.5). Some of the best published results are also included [75, 89, 110], **(b)**: Same as above, but for textured samples.

Saw damage etched planar (100) as well as random-pyramid textured (111) *p*-type (~5 Ωcm) Cz Si wafers with a thickness of ~150 µm were used as substrates. Symmetrical phosphorus diffused n^+pn^+ structures (for process details see section 2.6) with both textured and planar wafers were fabricated – these served as heavily-doped Si surfaces. After a Radio Corporation of America (RCA) cleaning process [102], the optimised PECVD SiN_x films were deposited on both the sides of undiffused (planar) and diffused (planar and textured) silicon. From the τ_{eff} measurement, the emitter saturation current density J_{0e} of the n^+ layers was extracted at high injection (1×10^{16} cm^{-3}) using the relation proposed by Kane and Swanson (see Equation 2.15 and Fig. 2.1 in Chapter 2) [41]. Figure 3.12 shows the extracted J_{0e} (left Y-axis) and $V_{oc,limit}$ (right Y-axis) for SiN_x passivated (a) planar and (b) textured n^+ surfaces as a function of the phosphorus diffused n^+ sheet resistance. $V_{oc,limit}$ was calculated from the extracted J_{0e} using the following relation:

$$V_{oc,limit} = \frac{nkT}{q}\ln\left(\frac{J_{sc}}{J_{0e}} + 1\right), \quad (3.1)$$

where n is the diode ideality factor (assumed as 1 here). kT/q is the thermal voltage (25.6 mV), k is the Boltzmann constant, T is the temperature, J_{sc} is the short-circuit current (40 mA/cm^2 was used here).

The best published results till date for surface passivation of planar and textured n^+ surfaces are also shown in the Figure 3.12 for single-layer SiN_x passivation deposited using lab-type and industrial-type reactors [44, 75, 88, 89, 110]. SiN_x films with optimum antireflective properties under air (n = 2.05) showed J_{0e} values as low as 25 fA/cm^2 on 150 Ω/sq planar n^+ diffusions after industrial firing.

Even lower J_{0e} values of 14 fA/cm^2 were obtained using Si-rich SiN_x (n = 2.5) on similar planar n^+ diffusions. As a matter of fact, these results are quite remarkable as they demonstrate the lowest J_{0e} measured to date using single-layer SiN_x. Assuming a short-circuit current density of 40 mA/cm^2, such a low J_{0e} value would limit the open-circuit voltage ($V_{oc.limit}$) of a *c*-Si wafer solar cell to 737 mV. The surface passivation of the industrial phosphorus diffusions with inline PECVD SiN_x films is thus clearly outstanding.

Figure 3.13 inspects the ratio of $J_{0e,textured}$ and $J_{0e,planar}$ for the n^+ Si as a function of n^+ sheet resistance. Clearly J_{0e} increases by a factor of 1.2-2.4 for a textured surface when

compared to a planar surface, depending on the sheet resistance. Experiments furthermore show that:

(i) the textured wafers exhibit a 5 ± 3 Ω/sq higher sheet resistance than the planar wafers (this has been observed and confirmed from several experiments, whereby we measured the sheet resistance separately for each of the planar and textured wafers). This might be caused by a) larger surface area of textured samples, b) the tops and bases of the random pyramids having different doping concentration (also observed in Ref. [75] and highlighted in Ref. [134]).

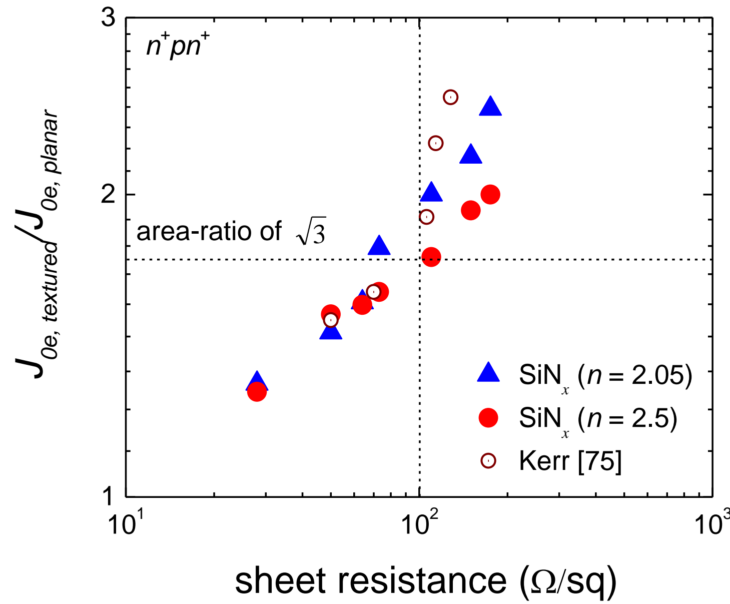

Figure 3.13: The ratio of J_{0e} of textured and planar n^+ silicon vs. the n^+ sheet resistance.

(ii) the lightly diffused surface (150 Ω/sq) resulted in a J_{0e} ratio ($J_{0e,\text{textured}}/J_{0e,\text{planar}}$) of 2.5, whereas the heavy diffusion (20 Ω/sq) resulted in a J_{0e} ratio of 1.2. For lighter diffusions (> 100 Ω/sq.) the sensitivity of surface passivation becomes more important. Higher J_{0e} (more than 1.73) for textured surface with lighter diffusions is likely to be due to a) a higher density of interface states (D_{it}) at the (111) exposed surface in textured Si compared to (100) surface in planar Si [135-137], b) the presence of pyramid edges and vertices on textured surfaces [138-140].

PECVD deposited hydrogenated *a*-Si:H or *a*-SiN$_x$:H was reported to passivate both (111) and (100) surfaces effectively [140-142]. As observed here for lighter diffusions (> 100 Ω/sq.), Si-rich SiN$_x$ (n = 2.5) yields reduced J_{0e} ratio, which implies better H passivation of (111) surface by high refractive index SiN$_x$ compared to nearly-stoichiometric SiN$_x$ (n = 2.05) in this work and the SiN$_x$ (n = 1.9) used in the work of

Kerr *et al.* [75]. For heavy diffusions (< 100 Ω/sq.) it appears likely the surface is less relevant as the diffusions are deeper. And for deeper n^+ layers the junction depletion region is not conformal with the surface texture (tends to become planar) [134]. It can be the fact that the recombination at the heavily-doped n^+ layers is limited by recombination in the bulk of n^+ layers (Auger recombination or precipitate formation/ incomplete ionization). As expected, Si-rich SiN_x cannot anymore provide better passivation on textured (111) oriented surfaces.

3.5. Conclusions

A significantly improved level of *c*-Si surface passivation is demonstrated using SiN_x films deposited in a commercially available inline PECVD reactor. The results are as good as obtained by lab-type static deposition reactors. This improvement is mainly attributed the change in plasma source configuration that resulted to a high positive charge density in SiN_x in combination with lower interface defect density at the *c*-Si/SiN_x interface. Remarkably low $S_{eff,max}$ values of 2 and 5 cm/s is obtained on moderately-doped undiffused *n*-type and *p*-type Cz silicon, respectively. Similar high-quality results are also obtained on phosphorus-doped n^+ silicon for a wide range of sheet resistances. J_{0e} as low as 15 fA/cm^2 was achieved. Surface recombination of the textured n^+ layer was investigated to be limited by the surface for lightly-doped n^+ surfaces and limited by the bulk for heavily-doped n^+ layers. In addition the impact of the surface texture on J_{0e} disappears for heavily-doped layers. SiN_x films are shown to stable after an industrial firing process that is widely used in the photovoltaic industry, whereas in earlier work an optimised annealing was required for excellent results. The present work thus demonstrates that a standard industrial fast firing process is sufficient for obtaining outstanding surface passivation results with inline deposited SiN_x. These excellent were achieved using an industrial inline reactor on large-area Si wafers, and thus could be beneficial for industrially fabricated high-efficiency silicon wafer solar cells.

3.6. Publications arising from this Chapter

1. **S. Duttagupta**, L. Fen, M. Wilson, B. Hoex, A.G. Aberle, Extremely low surface recombination velocities on low-resistivity *n*-type and *p*-type crystalline silicon using dynamically deposited remote plasma silicon nitride

films, *Progress in Photovoltaics: Research and Applications*, 22, 641-647, 2014.

2. **S. Duttagupta**, B. Hoex, F. Lin, T. Mueller and A. G. Aberle, High-quality surface passivation of low-resistivity *p*-type *c*-Si by hydrogenated amorphous silicon nitride deposited by industrial-scale microwave PECVD, Proc. of 37th IEEE Photovoltaic Specialists Conference, Seattle, p. 001421 – 001423 (2011). ***Best Poster Award*** in the conference area "Crystalline Silicon: Cell Structures and Processes".
3. **S. Duttagupta**, B. Hoex, and A.G. Aberle, "Progress in surface passivation of heavily-doped crystalline silicon using PECVD silicon nitride" In preparation for submission to a Journal
4. **S. Duttagupta**, B. Hoex, A. G. Aberle, "Progress with industrially feasible passivation of lightly and heavily doped n-type silicon surfaces using inline PECVD silicon nitride", **[Oral presentation]**, Tech Digest of 22nd PVSEC, China, (2012).
5. **S. Duttagupta**, F. Ma, B. Hoex, T. Mueller, and A. G. Aberle, Optimised antireflection coatings using silicon nitride on textured silicon surfaces based on measurements and multidimensional modelling, Proc. of International Conference on Materials for Advanced Technologies 2011 (ICMAT 2011), Symposium O, Singapore (2011); Energy Procedia 15, p. 78-83 (2012). **Best Poster Award.**

Chapter 4: Low-temperature plasma-deposited and chemically-grown silicon oxide (SiO_x) and stacks

4.1. Introduction

Thermally grown silicon dioxide (SiO_2) has been extensively studied in the past few decades for the passivation of (un) diffused silicon surfaces [19, 45, 143, 144]. A high-quality Si-SiO_2 interface was extremely crucial for the success in microelectronics application [143, 144]. After an optimised anneal, the Si-SiO_2 interface can result to very low interface defect density, for example $D_{it,midgap}$ in the order of 10^9 $eV^{-1}cm^{-2}$ [17, 56, 67, 143]. Such low $D_{it,midgap}$ is a pre-requisite for excellent surface passivation of *c*-Si [20, 145], which is evident by extremely low surface recombination velocity S_{eff} (2.4 cm/s) [77]. These thermal SiO_2 was used for high efficiency solar cell devices that resulted to (then) world-record efficiencies up to 24.7% [146, 147]. However, higher processing temperature (800 - 1100°C) for thermal SiO_2 can be detrimental for less pure Cz-grown or multicrystalline Si. Moreover, a high temperature process can significantly add up fabrication cost.

The most widely used alternative approach for low-temperature SiO_2 is the PECVD method, which can allow low-temperature (< 400 °C) processing along with significantly higher deposition rates. Single-layer SiO_x generally does not provide a high-quality passivation with $S_{eff,max}$ ~500-1000 cm/s in the as-deposited state [148-151]. A forming gas anneal (FGA) can improve passivation thereby lowering $S_{eff,max}$ to 100 cm/s, but these values are insufficient for high-performance silicon wafer solar cells [148, 150]. Important to mention that in fact some results in the literature indicated unstable surface passivation [148, 152]. However, use of a capping layer (for example SiN_x) with optimised annealing significantly improved the surface passivation capability with $S_{eff,max}$ of 2 and 11 cm/s on *n*- and *p*-type silicon [78, 81]. The reason was attributed to effective hydrogen passivation (where hydrogen comes from capping SiN_x). This resulted $D_{it,midgap}$ as low as 10^{11} $eV^{-1}cm^{-2}$ and in addition a very low Q_f of 10^{11} cm^{-2} were measured [81]. Such low Q_f can be utilised for surface passivation of heavily-doped p^+ *c*-Si, which is otherwise seems not possible by dielectrics with high Q_f [see Section 2.3 (b)]. PECVD SiO_x with a capping layer was shown to provide very good surface

passivation on moderately-doped undiffused silicon (after optimised anneal). However, results after high-temperature annealing is seldom found in the literature. Thus, it is interesting to investigate this considering the relevance for industrial screen-printed solar cell applications. For heavily-doped n^+ and p^+ *c*-Si excellent passivation was obtained with J_{0e} ~ 20 fA/cm^{-2} for thermal SiO_2 (with and without a SiN_x capping layer) after optimised annealing or an alneal process [44, 75, 153-158]. However, it is surprising that very limited data is available on PECVD SiO_x for high-quality surface passivation of heavily-doped *c*-Si. Hence, considering the economic and technological advantages it's very important to develop PECVD SiO_x layers for effective surface passivation of all the relevant *c*-Si surfaces for solar cells.

Among many other low-temperature techniques to form SiO_x layers especially using chemical solutions [54], an alternative technique (using RCA-2 chemical) is used as explained in section 4.3.2. The results for passivation of p^+ *c*-Si is reported therein.

4.2. Surface passivation of moderately-doped *c*-Si

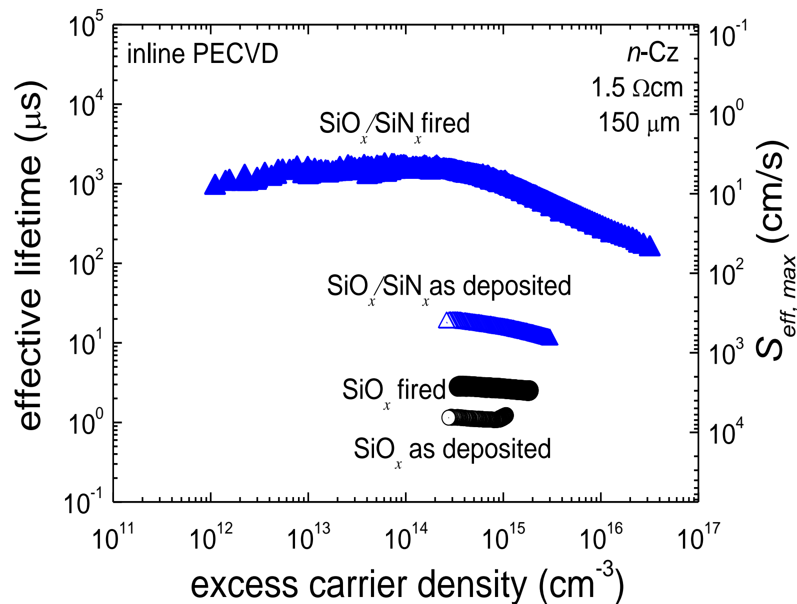

Figure 4.1: Measured injection-level dependent τ_{eff} (left Y axis) and corresponding $S_{eff,max}$ (right Y axis) for *n*-type Cz wafers passivated by dielectrics (mentioned in the graph) on both sides, before and after industrial firing at 880 °C.

Dynamically-deposited PECVD SiO_x films are extensively investigated. The layers are deposited using the inline PECVD reactor described in Section 2.6. The deposition conditions and film properties (such as refractive index and thickness) are summarized in Table 4.1. Figure 4.1 shows injection level dependent effective lifetime curve for dynamically-deposited PECVD SiO_x films on *n*-type Cz silicon. In as deposited state the film doesn't provide any level of surface passivation (τ_{eff} ~ 1 µs at 10^{15} cm^{-3}). After industrial fast firing with peak temperature ~ 880 °C, the surface passivation results didn't improve at all (τ_{eff} ~ 2.6 µs at 10^{15} cm^{-3}). Deposition of a SiN_x capping layer resulted in a minor improvement in passivation (τ_{eff} ~ 15 µs at 10^{15} cm^{-3}). However, a drastic improvement in surface passivation with $S_{eff,max}$ ~ 7.6 cm/s was obtained with the dielectric stack of SiO_x/SiN_x films after industrial firing. Moreover, it is important to note that τ_{eff} was observed to be flat for lower injection-levels. This is very important as Si solar cells often operate in low light conditions and low injection-level independent τ_{eff} is thus an important observation.

Table 4.1. Inline PECVD deposition parameters and film properties for the PECVD dielectrics used in this work.

Dielectric	Process gas	Heater set temperature (°C)	Reactor pressure (mbar)	Plasma power (W)	Refractive index	Thickness (nm)
SiO_x	SiH_4 + N_2O	200	0.15	700	1.47	15
SiN_x	SiH_4 + NH_3	350	0.20	2200	2.0	70

4.2.1. Surface passivation mechanism

In order to explain the surface passivation behaviour in Figure 4.1, it was required to investigate the electronic interface properties. Using contactless *C-V* measurements, total charge density (Q_{total}), energy-dependent $D_{it}(E)$ was measured. As observed in Figure 4.2 below, the inferior surface passivation of single-layer SiO_x (both in as-deposited and fired) can be explained by very high $D_{it,midgap}$ ~10^{13} $eV^{-1}cm^{-2}$. Incorporation of capping SiN_x layer improved the $D_{it,midgap}$ to ~ 10^{12} $eV^{-1}cm^{-2}$. However, the surface passivation is still inferior with S_{eff} ~ 500 cm/s. The drastic improvement in

surface passivation ($S_{eff,max}$ ~ 7.6 cm/s) after industrial firing the SiO_x/SiN_x stack layer is attributed to a reduction in $D_{it,midgap}$ of ~ 3×10^{10} $eV^{-1}cm^{-2}$.

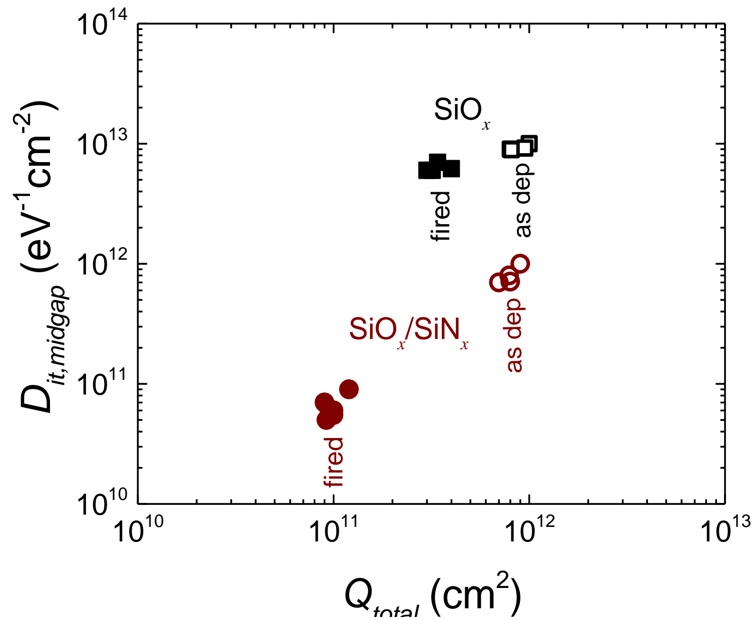

Figure 4.2: Measured $D_{it,midgap}$ as a function of Q_{total} for the investigated PECVD SiO_x with or without a capping layer.

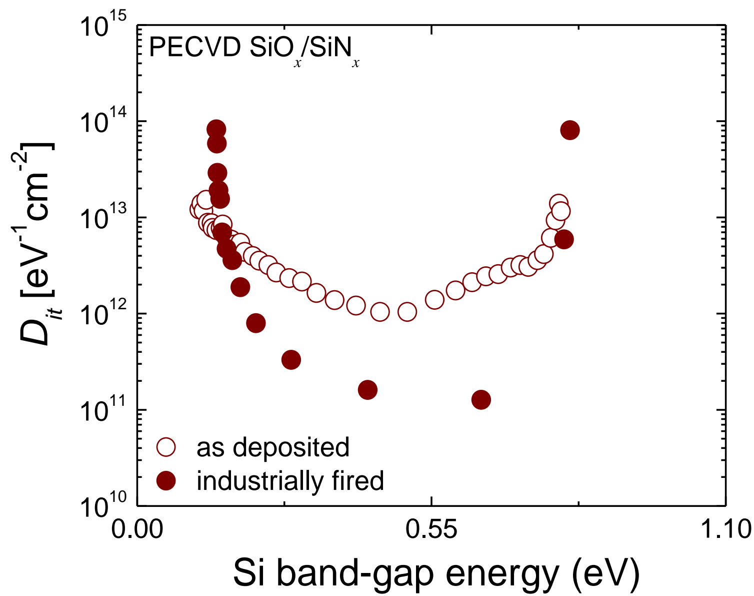

Figure 4.3.: Measured interface state density (D_{it}) at the c-Si/SiO_x interface as a function of the bandgap energy for an as-deposited and industrially-fired PECVD SiO_x/SiN_x stack on an undiffused n-type c-Si wafer.

Figure 4.3 shows the Si bandgap energy dependent interface defect density $D_{it}(E)$. As can be seen, the anneal (fast-firing) improved the $D_{it\ midgap}$ of the sample by one order of magnitude to ~3×10^{10} $eV^{-1}cm^{-2}$, indicating a very good interface quality after the industrial firing process. This can be attributed to the transport of hydrogen atoms from the SiN_x film to the *c*-Si/SiO_x interface, leading to the passivation of dangling bonds and thus a reduced interface state density (D_{it}) ("chemical passivation"). The measurements revealed a small negative V_{fb} (-0.05 V), indicating a very low Q_{total} of about $+10^{11}$ cm^{-2} in the PECVD SiO_x/SiN_x stack near the *c*-Si/SiO_x interface. Low positive charge density has some advantages, which will be explained in the later part of the chapter. The surface passivation mechanism is dominated by high-quality interface thus a 'chemical passivation'.

4.3. Surface passivation of heavily-doped *p*-type *c*-Si

The electronic passivation of heavily doped p^+ type crystalline silicon (*c*-Si) surfaces has proven to be very challenging in the past, especially with positively charged dielectrics. The most commonly used positively charged dielectrics in the photovoltaic (PV) community - thermal oxide (SiO_2) and amorphous hydrogenated silicon nitride (*a*-SiN_x:H or briefly SiN_x) - are typically found to be an unsuitable choice for p^+ silicon surface passivation due to their intrinsic positive fixed charge (Q_f) and asymmetric capture cross sections for electrons and holes ($\sigma_{n/p}$) [44, 74, 159-161]. During the 1980s, King and Swanson performed a detailed study on p^+ silicon surface passivation by thermal SiO_2 [162]. In 2002, Kerr *et al.* reported one of the best results for SiO_2 passivated (after *alneal* or forming gas anneal) p^+ silicon surfaces, with emitter saturation current density (J_{0e}) values ~20 fA/cm^2 [44]. In fact, Kerr *et al.* were also one of the first to study surface passivation of p^+ silicon by plasma-enhanced chemical vapour deposition (PECVD) SiN_x (in the as-deposited state). It was found that SiN_x can only provide a modest level of surface passivation on passivated p^+ silicon surfaces, which was later confirmed by other authors [44, 159, 160]. On the other hand, Chen *et al.* reported an excellent p^+ silicon surface passivation (with J_{0e} < 13 fA/cm^2) by Si-rich SiN_x films after a prolonged anneal at 450 ºC, and also after an industrial firing process [86, 141]. Recently, it was also shown that SiO_2 and SiO_2/SiN_x stacks provided modest level of surface passivation on p^+ silicon surfaces, whereas negatively-charged aluminium oxide (Al_2O_3) films grown by atomic layer deposition (ALD) give outstanding surface passivation on similar p^+ silicon surfaces [161]. The latter was also demonstrated at the solar cell device level, with efficiencies of up to 23.9% for *n*-type

PERL (passivated emitter rear locally diffused) *c*-Si wafer solar cells [74, 163, 164]. In 2008 Mihailetchi *et al*. reported excellent J_{0e} values of 23 fA/cm^2 for p^+ silicon surfaces passivated by a stack consisting of an ultrathin oxide grown wet-chemically by HNO_3 and then capped with a SiN_x film [165]. Thus in general (except for the work of Chen *et al.*), it was observed that a single PECVD SiN_x film is not suitable for p^+ silicon surface passivation [44, 159, 160]. One of the reasons is the very high fixed positive charge density of > 10^{12} cm^{-2} in PECVD SiN_x films on *c*-Si. Very recently it was observed that the fixed charge density in the SiN_x film can be reduced by adding a thin silicon oxide layer between the *c*-Si wafer and the SiN_x film, and this resulted in good surface passivation on low-resistivity undiffused *p*-type *c*-Si wafers, with effective surface recombination velocities (S_{eff}) of < 11 cm/s [81]. Given this promising result on undiffused *c*-Si wafers, it is of interest to explore the passivation performance of SiO_x/SiN_x stacks on p^+ diffused *n*-type *c*-Si wafers, which are becoming an important substrate in the *c*-Si PV industry. There are two methods that are examined in this thesis to form SiO_x films, 1) PECVD method 2) wet-oxide 'chemical' method. Both of them will be discussed in the following section.

4.3.1. PECVD SiO_x

In this work it will be shown that PECVD SiO_x/SiN_x stacks can provide state-of-the-art surface passivation on p^+ silicon surfaces. Symmetrical p^+np^+ structures were fabricated by a standard BBr_3 diffusion of planar and textured *n*-type Cz silicon wafers with a dimension of 125 mm × 125 mm, bulk resistivity of 5-8 Ωcm. The details of fabrication process is mentioned in section 2.6 of the thesis. In this work the initial p^+ diffusion had a sheet resistance of 55 Ω/sq. Subsequently the borosilicate glass was stripped in a diluted (10%) HF solution until the surface was hydrophobic and the samples underwent a thermal oxidation which also altered the B doping profile resulting in a final sheet resistance of 75 Ω/sq, which were used for surface passivation studies in this work. The p^+ diffusions (both 55 Ω/sq and 75 Ω/sq) were characterized by four-point probe measurements (Cresbox, Napson) and secondary ion mass spectrometry (SIMS, Evans Analytical) and the results are shown in Figure 4.4. Prior to the deposition of the PECVD dielectric films, the samples were again RCA cleaned with a final HF dip followed by water rinsing and drying, to ensure a H-terminated surface. Three different PECVD dielectric films was investigated in this study: a) a single 70 nm SiO_x film, b) a 15 nm SiO_x film capped with a 70 nm SiN_x film, and c) a

single 70 nm SiN_x film. The deposition conditions and film properties (such as refractive index and thickness) are summarized in Table 4.1. The transport speed of the sample carrier was adjusted to yield the desired thickness of the dielectric films. After deposition of the dielectric films onto both surfaces of the p^+np^+ structure (using two separate deposition runs), the samples received a post-deposition anneal in an industrial fast firing furnace (Ultraflex, Despatch) for a few seconds at a heater set temperature of ~800 ºC.

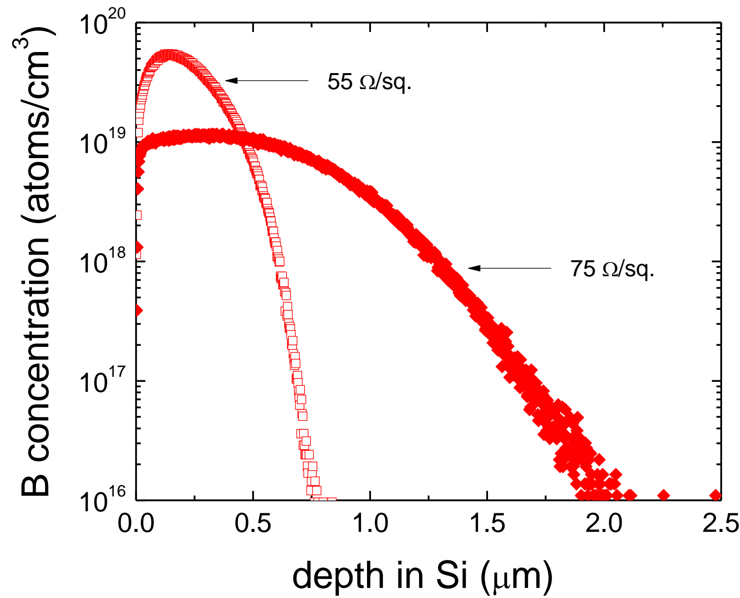

Figure. 4.4: Boron depth profile of selected p^+ diffusions as measured by SIMS. The sheet resistance determined by 4-point probe measurements is also shown.

From the effective lifetime measurement, the emitter saturation current density J_{0e} of the p^+ surface was then extracted from the slope of the inverse lifetime vs. injection level curve at high-injection conditions (in the range of 5×10^{15} - 1.5×10^{16} cm^{-3}), using the relation proposed by Kane and Swanson (see Equation 2.15 and Fig. 2.1 in Chapter 2) [41].

Figure 4.5 shows the measured Auger-corrected inverse effective carrier lifetimes as a function of injection level for 75 Ω/sq planar p^+ silicon layers passivated by PECVD SiO_x, SiO_x/SiN_x dielectric stacks, and a single layer of SiN_x. A single PECVD SiO_x film provides poor surface passivation, both in the as-deposited state (J_{0e} ~ 500-600 fA/cm^2) as well as after an industrial firing process (~ 350 - 400 fA/cm^2), as is evident from the higher slope. However, it is expected that these results can be improved by a forming gas anneal (FGA), but this is beyond the scope of this work. In the as-deposited state,

the SiO_x/SiN_x stack resulted in a J_{0e} value of ~450 fA/cm^2. A significant improvement was observed after industrial firing with set temperatures of > 800 °C, resulting in an excellent level of p^+ surface passivation with J_{0e} values of ~25 fA/cm^2.

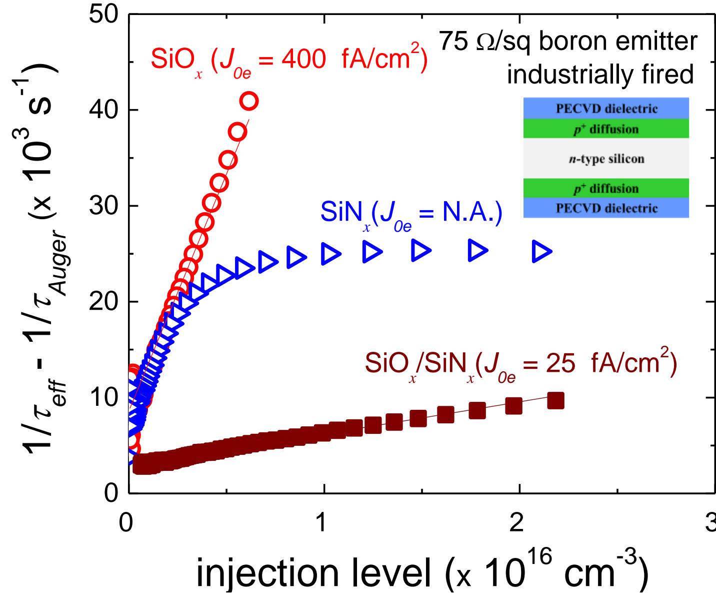

Figure 4.5.: Measured injection level dependence of the Auger-corrected inverse effective lifetime of symmetrical p^+np^+ samples symmetrically passivated by SiO_x, SiO_x/SiN_x and SiN_x films. All layers were deposited by PECVD and the samples received a post-deposition anneal in an industrial firing furnace.

This can most likely be attributed to a significantly improved chemical passivation by a reduction of the interface defect density between at the SiO_x/*c*-Si interface by hydrogen released from the SiN_x films during the high-temperature step. Experiments on pyramid-textured samples showed an increase in J_{0e} by a factor of ~1.8 compared to planar samples, which can be understood by the increased surface area (factor 1.73). Assuming a short-circuit current density of 40 mA/cm^2 and using the ideal one-diode model, it can be calculated that a J_{0e} of 25 fA/cm^2 would limit the one-Sun open-circuit voltage to 726 mV at 25 °C for an *n*-type c-Si solar cell. One of the key results here is the linear behaviour of Auger-corrected effective lifetime curves for the lifetime samples passivated with positively charged PECVD SiO_x/SiN_x dielectrics stacks, allowing the extraction of J_{0e} values using Eq. 2.15, which is clearly not the case in Figure 4.5 for industrially fired 70 nm PECVD SiN_x (n = 2.05) films.

A similar non-linearity has also been reported by other authors [44, 92, 160]. This non-linearity is a deviation from the standard theory, which can be attributed to increased

surface recombination at the interface either due to a) high positive fixed charge density ($> 10^{12}$ cm^{-2}) or b) higher asymmetry of the capture cross sections (σ) for electrons and holes at the c-Si/SiN_x interface. Therefore, in order to quantify the level of surface passivation by PECVD SiN_x, $V_{oc,implied}$ of these symmetrically passivated p^+np^+ samples was reported as also mentioned by others [24, 44, 160, 166]. A $V_{oc,implied}$ of about 630 ± 10 mV was measured, which implies an inferior surface passivation compared to the p^+np^+ samples passivated by PECVD SiO_x/SiN_x stacks, which showed a $V_{oc,implied}$ of ~690 ± 5 mV after an industrial firing process. Please note that $V_{oc,\ implied}$ also depends on factors such as the bulk doping level and the bulk carrier lifetime of the used c-Si wafers, as well as the optical properties of the passivation coating; hence, care must be taken when comparing experimental values between different works.

Modelling: Role of fixed charge density and extraction of S_{n0} at p^+ c-Si surfaces

The electron surface recombination velocity parameter S_{n0} at the p^+ type c-Si surface is a critical parameter for the interface quality, as it quantifies the recombination activity of that interface. From the Shockley-Read-Hall (SRH) theory [14, 15], extended by Girish *et al.* and Aberle *et al*. to include the effects of interface charges and illumination [16, 17]; S_{n0} is proportional to the product of the N_{st} (the number of surface states per unit area) and the electron capture cross section (σ_n):

$$S_{n0} \equiv v_{th}\sigma_n N_{st}, \qquad (5.2)$$

where v_{th} is the thermal velocity of the charge carriers. Taking both the measured boron diffusion profile and the Q_f (as measured above) into account, the S_{n0} values were extracted for the passivated p^+ silicon surface by matching the experimental and simulated effective lifetime curves using Sentaurus TCAD [167]and using the physical models from Refs. [168, 169].

Figure 4.6 shows the simulated J_{0e} of a 75 Ω/sq. p^+np^+ sample symmetrically passivated with a PECVD SiO_x/SiN_x stack as a function of S_{n0}. This figure also shows the role of considering the amount and polarity of charge for extraction of S_{n0}. A J_{0e} of 25 fA/cm^2 (from Fig. 2) and Q_f of $+10^{11}$ cm^{-2} as determined in this work for industrially-fired PECVD SiO_x/SiN_x stacks corresponds to a S_{n0} of about 400 cm/s. Such low surface recombination velocity is comparable to values reported earlier for ALD grown Al_2O_3 films [74]. The J_{0e} vs. S_{n0} curve for an insulator charge of $+10^{11}$ cm^{-2} is almost the same

as that for zero charge. It is also clear that the surface passivation mechanism for the SiO_x/SiN_x stack completely relies on “chemical passivation”. The role of charge (both in terms of polarity and magnitude) in surface passivation of p^+ silicon is illustrated.

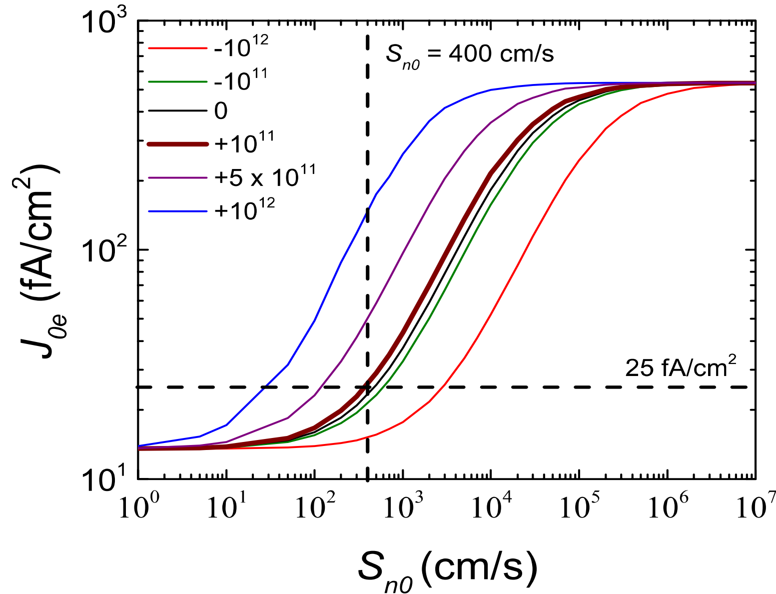

Figure 4.6.: Simulated J_{0e} values of a 75 Ω/sq. p^+np^+ sample symmetrically passivated with a PECVD SiO_x/SiN_x stack, as a function of the S_{n0} and the fixed insulator charge density.

Obviously a negative fixed charge is more beneficial as it repels the minority carrier electrons from the interface. As shown in the Figure 4.6, a film with negative insulator charge of -1×10^{12} cm^{-2} with a similar S_{n0} value of 400 cm/s results to lower J_{0e} of < 18 fA/cm^2. On the other hand, films with Q_f of > +1×12 cm^{-2} (such as for SiN_x) show poor surface passivation with J_{0e} > 100 fA/cm^2 (considering a similar S_{n0}). This explains (at least partly) the detrimental effect of a very high positive fixed charge in the case of passivating p^+ silicon surfaces. However, experimentally it is often found that the J_{0e} values are much higher than 100 fA/cm^2, which is likely to be due to higher S_{n0} at these c-Si/SiN_x interfaces. This could either be due to asymmetric capture cross sections or higher interface defect densities at these interfaces. Interestingly, it was observed that J_{0e} can be below 150 fA/cm^2 when D_{it} is low (10^{11} eV^{-1} cm^{-2}) and Q_f is below 10^{12} cm^{-2}. In addition to this simulation study, it is further corroborated from field effect measurements that a positively charged dielectric can effectively passivate p^+ silicon surfaces, provided the fixed charge Q_f is < $+1\times10^{12}$ cm^{-2} and D_{it} remains low.

4.3.2. Chemically-grown SiO_x

Although Mihailetchi *et al*. reported excellent emitter saturation current density J_{0e} values of 23 fA/cm^2 for p^+ surfaces passivated by a dielectric stack consisting of an ultrathin oxide grown by HNO_3 and a SiN_x capping layer [165]. Unfortunately, the underlying surface passivation mechanism was not discussed in detail. As explained in the previous section, PECVD SiO_x/SiN_x stacks (SiO_x thickness ~25 nm) can provide an excellent surface passivation of heavily-doped p^+ silicon surfaces, with J_{0e} values of ~25 fA/cm^2 after an industrial firing process [151]. It would be interesting to investigate if this thin PECVD grown SiO_x film can be replaced by an ultrathin chemically grown SiO_x layer.

Pseudo-square (125 mm × 125 mm) Cz *n*-type Si wafers with a bulk resistivity of 5-8 Ωcm, a thickness of 150 μm, and a (100) surface orientation were used in this experiment. The wafers were saw damage etched and some received alkaline texturing. The 75-Ω/sq p^+np^+ structures were fabricated. The samples were cleaned using the RCA (Radio Corporation of America) process [102] with a final HF dip to ensure H-terminated hydrophobic surface. Some of these samples were kept separately (Set 1), while the other samples (Set 2) underwent chemical pre-treatment using HCl (40 %): H_2O_2 (40 %): DI water solution at a temperature of 90 ºC for 15 minutes. This resulted in surface oxidation with many Si-OH bonds ('hydroxylated SiO_x' also sometimes referred as OH-terminated Si in this text). The resulting *c*-Si surface is hydrophilic in nature. The thickness of the ultrathin chemical oxide film was determined by transmission electron microscopy (FEI Tecnai, operated at 200 kV) and was found to be ~0.6 nm as shown in Fig. 4.7, which agrees well with results reported in literature [170, 171]. A PECVD SiN_x (~70 nm) layer was deposited in a commercial inline microwave-powered remote PECVD reactor (SiNA-XS, Roth & Rau AG, Germany) for both sample sets (Set 1 and 2). The PECVD SiN_x (refractive index n = 2.05 and thickness of 70 nm) was deposited on both sides of the wafer resulting in a symmetrically passivated lifetime structure. After deposition of the PECVD SiN_x onto both surfaces of the p^+np^+ structure all samples received a post-deposition anneal in an industrial fast firing furnace (Ultraflex, Despatch) for a few seconds at a set temperature of ~ 800 ºC. From the effective lifetime measurement using a contactless flash-based photoconductance decay tester (WCT-120, Sinton Instruments, USA), the emitter saturation current density J_{0e} of the boron emitter was then extracted at high-injection

conditions (~10^{16} cm^{-3}) as shown in Fig. 4.8, using the relation proposed by Kane and Swanson (see Equation 2.15 and Fig. 2.1 in Chapter 2 for details) [24, 41]

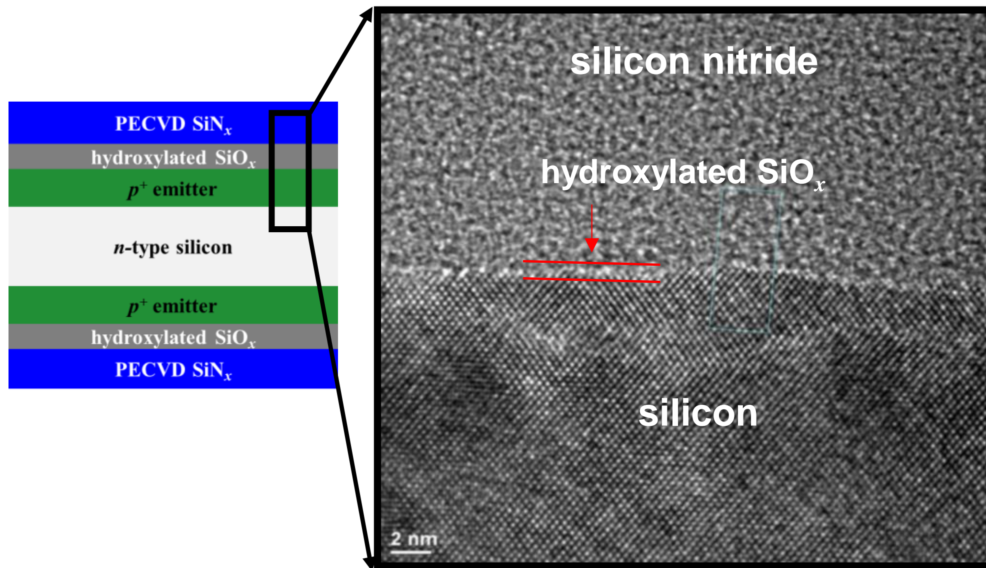

Figure 4.7.: Schematic diagram and TEM micrograph of a p^+np^+ sample passivated with a PECVD SiN_x film deposited onto an ultrathin chemical oxide.

Figure 4.8 shows the measured Auger-corrected inverse effective carrier lifetimes as a function of injection level for 75-Ω/sq planar p^+ silicon layers passivated by a) PECVD SiO_x, b) SiN_x deposited on H-terminated surface, and c) SiN_x deposited on ultrathin chemical oxide. For comparison, results of PECVD AlO_x/SiN_x stacks from our previous are also included (details of this is presented in the next chapter). Single-layer PECVD SiO_x and SiN_x deposited on H-terminated surface provide poor surface passivation. Interestingly, the SiN_x deposited on ultrathin chemical oxide surface resulted in a drastic improvement in surface passivation, with J_{0e} values of ~26 fA/cm^2 on planar p^+ surfaces after an industrial firing step (set temperature ~ 800 ºC). It is very important to mention here that a linear relationship was observed for the lifetime samples passivated with SiN_x deposited on ultrathin chemical oxide, thus allowing the reliable extraction of J_{0e} values using Eq. 1. This linear relationship is not observed in the case of SiN_x deposited onto an H-terminated surface, as reported by others as well [44, 160]. The textured surface roughly shows increase in J_{0e} by a factor of 1.7 - 2.2, which can mainly attributed to increase in surface area.

In order to further verify the level of surface passivation, in addition to carrier lifetime measurements, spatially resolved photoluminescence (PL) imaging was performed. PL

images were taken for $p^{+}np^{+}$ samples passivated with SiN_x deposited on ultrathin chemical oxide [Fig. 4.9 (a)] and SiN_x deposited on H-terminated surface [Fig 4.9 (b)]. The PL intensity images were taken with the same exposure time (0.1 s) and are shown in a similar scale to depict the difference in the surface passivation quality. It is clear that the SiN_x deposited on ultrathin chemical oxide exhibits very high PL counts (with brighter contrast) compared to SiN_x deposited on H-terminated surface, proving better surface passivation.

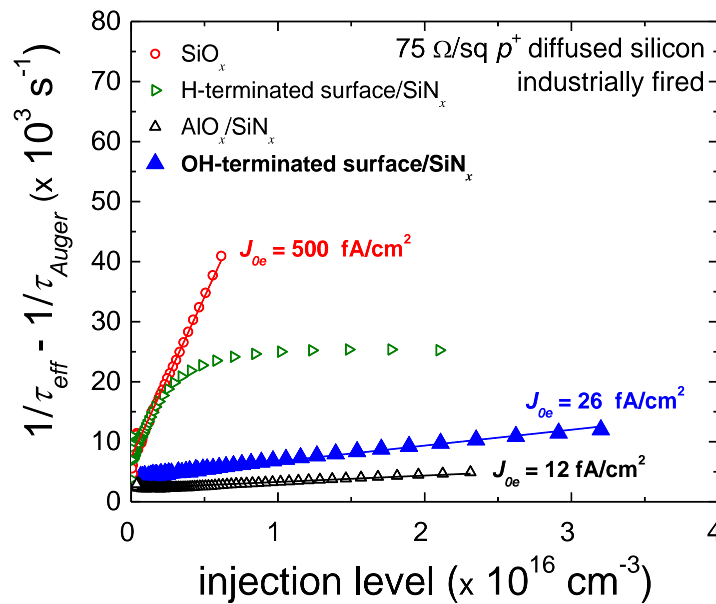

Figure 4.8.: Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially fired dielectric passivated 75-Ohm/sq $p^{+}np^{+}$ samples.

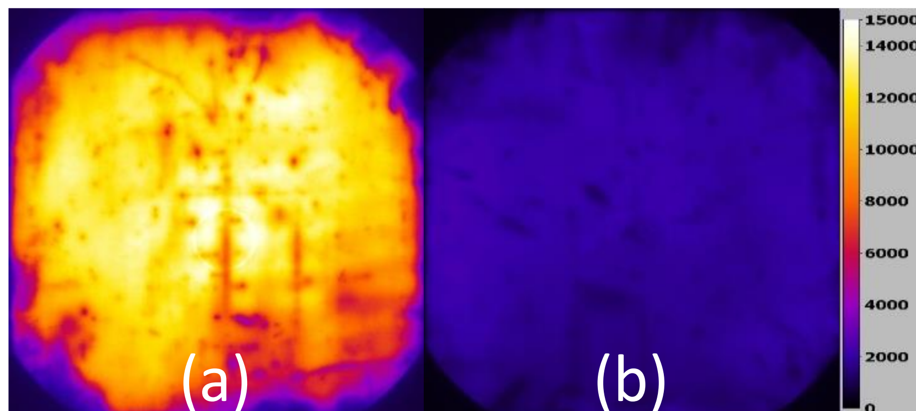

Figure 4.9.: Spatially resolved photoluminescence (PL) images of 75-Ohm/sq $p^{+}np^{+}$ samples passivated with **(a)** SiN_x deposited on ultrathin chemical oxide film, **(b)** SiN_x deposited on H-terminated surface. Both the samples were industrially fired at ~ 800 °C.

A deeper understanding of the surface passivation mechanism of the SiN_x deposited on ultrathin chemical oxide requires the evaluation of the interface properties (for example, density of interface states D_{it} and amount of total charge Q_{total}). Contactless corona-voltage measurements were carried out on undiffused silicon samples both before and after industrial firing.

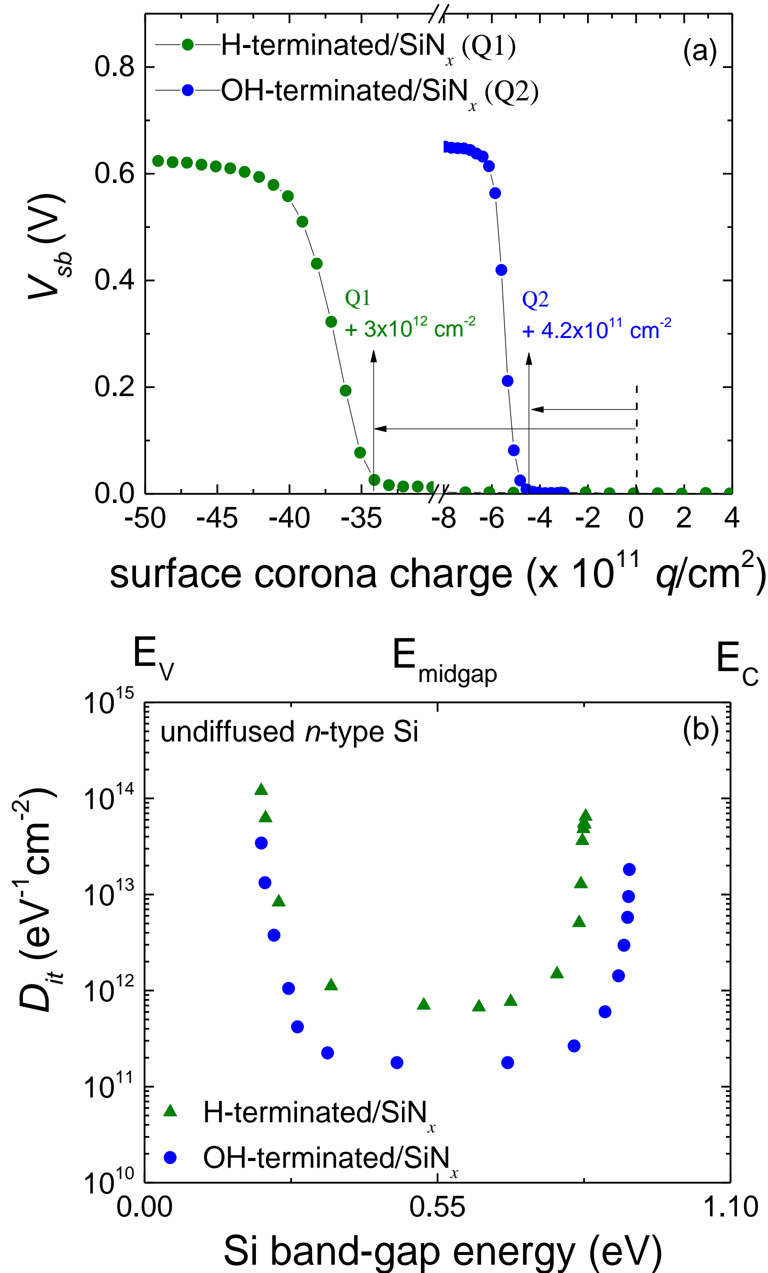

Figure 4.10: **(a)** Measured surface barrier voltage (V_{sb}) as a function of surface corona charging and **(b)** Measured interface defect density (D_{it}) as a function of the bandgap energy for SiN_x deposited on ultrathin chemical oxide (OH-terminated) and on H-terminated surface. Results are shown for industrially fired samples.

The measurements revealed a small negative flat-band voltage V_{fb} -1.8 V, indicating a lower charge density near the interface. Q_{total} of about ~ +4.2×10^{11} cm^{-2} in the case of SiN_x deposited on ultrathin chemical oxide was measured. On the other hand, SiN_x deposited on H-terminated surface features high negative flat-band voltage V_{fb} -5.09 V resulting very high positive Q_{total} of about +3×10^{12} cm^{-2}, which is in good agreement with literature. A comparison is shown in Fig. 4.10(a), which indicates the drastic reduction of the positive charge density for SiN_x deposited on ultrathin chemical oxide. Understanding the drastic reduction of the insulator charge density requires further experiments and more study. The high positive Q_{total} in SiN_x films deposited on H-terminated surface drives the p^+ surface into depletion, thereby increasing the surface recombination rate. This recombination is significantly reduced by inserting an ultrathin silicon oxide, which reduces the positive Q_{total} by almost one order of magnitude.

The role of reduced Q_{total} on effective surface passivation of p^+ surface is well explained in previous section (Fig. 4.6). In Fig. 4.10(b) the energy dependent interface defect density D_{it} *(E)* for both cases (SiN_x deposited on ultrathin chemical oxide and on H-terminated surface) has been shown. As can be seen, the insertion of the ultrathin chemical oxide improved the $D_{it\ midgap}$ to ~2×10^{11} eV^{-1}cm^{-2} (compared to ~7×10^{11} eV^{-1}cm^{-2} for the H-terminated surface). The origin for such improvement requires more study on a) growth mechanism of PECVD SiN_x on H-terminated surface and ultrathin chemical oxide, b) influence of plasma damage. The insertion of ultrathin oxide can potentially reduce the *c*-Si surface damage from the bombardment of ammonia radicals formed in the plasma. It is recently reported that the penetration of nitrogen (N) atoms into *c*-Si, which can occur during SiN_x deposition, degrades the *c*-Si bulk quality [172], c) surface roughness and d) role of ultrathin chemical oxide in hydrogen transport process.

It should be noted that the optical performance of both types of sample (SiN_x deposited on ultrathin chemical oxide and on H-terminated surface) is similar, hence can be used as an efficient antireflection coating (ARC). Using advanced computer modelling (Sentaurus TCAD), the electron surface recombination velocity (S_{n0}) for 75-Ω/sq planar boron diffused surfaces was calculated to be as low as 450 cm/s.

4.4. Surface passivation of heavily-doped *n*- and *p*-type *c*-Si

Passivation of heavily doped n^+ and p^+ silicon surfaces is very important for high-efficiency Si wafer solar cells. Double-side contacted Si wafer solar cells (n^+np^+ or n^+pp^+) and all-back-contact (ABC) solar cells require passivation of both dopant polarities. The most commonly used positively-charged dielectrics in the photovoltaic (PV) community - thermal silicon oxide (SiO_2) and amorphous hydrogenated silicon nitride (a-SiN_x:H or briefly SiN_x) - are typically found to be an excellent candidate for n^+ silicon surface passivation but show moderate performance for p^+ Si surface passivation [44, 159] Similarly, Al_2O_3 films grown by plasma-assisted atomic layer deposition (PA-ALD) - which have a high negative charge density of up to 1×10^{13} elementary charges/cm^2 - can passivate p^+ Si surfaces with an arbitrary sheet resistance very well, however, they provide only a moderate passivation on n^+ Si surfaces for a particular range of sheet resistance [74, 92]. On the other hand, recently, Duttagupta *et al.* reported outstanding surface passivation of both n^+ and p^+ silicon surfaces using PECVD AlO_x/SiN_x stacks [173]. Generally, thick (~100 nm) thermal silicon oxide (SiO_2) films or stacks consisting of a thin (5-30 nm) SiO_2 film capped by a 50-100 nm thick silicon nitride (SiN_x) film are used due to their ability to passivate both n^+ and p^+ silicon surfaces [174, 175]. In 2008, Mihailetchi *et al.* reported excellent J_{0e} values of 23 fA/cm^2 for p^+ Si surfaces passivated by a stack consisting of an ultrathin oxide grown in a HNO_3 solution capped by a SiN_x film [165]. It is expected that this is a good method for simultaneously passivating both n^+ and p^+ silicon surfaces, however, no data are available yet in regards to its capability of passivating n^+ silicon surfaces. This stack was used to passivate the rear surface of ABC solar cells and this resulted in only moderate open-circuit voltages (< 650 mV) [176-179]. The implied V_{oc} of these devices were limited to the range of 660 to 680 mV. Thus it's important to investigate the possibility to improve the surface passivation with other dielectrics that are low-temperature deposited, industrially feasible and cost-effective, which can result in excellent passivation of both n^+ and p^+ silicon surfaces.

In this work, it is shown that SiO_x/SiN_x stacks deposited by PECVD in a fully industrial process can provide excellent surface passivation on both p^+ and n^+ emitters with various sheet resistance values. Symmetrical n^+pn^+ structures were fabricated using a standard $POCl_3$ diffusion on planar and textured p-type Cz silicon wafers with a dimension of 125 mm × 125 mm and a bulk resistivity of ~5 Ωcm. The sheet resistance of the n^+ emitter was varied by varying the process conditions (time and temperature) during the $POCl_3$ diffusion. Symmetrical p^+np^+ structures were fabricated by a standard

BBr_3 diffusion of planar and textured n-type Cz silicon wafers with a dimension of 125 mm × 125 mm, bulk resistivity of 5-8 Ωcm. The p^+ sheet resistance was varied by varying the process conditions (time and temperature) during the BBr_3 diffusion and by a post-diffusion oxidation (more details can be found in section 2.6). After the diffusion, the phosphorus and borosilicate glass was removed and the samples received a Radio Corporation of America (RCA) cleaning with a final HF dip to ensure an H-terminated surface. Subsequently, a stack of 15 nm SiO_x and 55 nm SiN_x was deposited on both sides of the samples in an industrial inline plasma-enhanced chemical vapour deposition (PECVD) reactor (SiNA XS, Roth & Rau, Germany). The deposition parameters are listed in Table 4.1.

After the PECVD deposition, the lifetime samples received a standard industrial firing process with a peak temperature of > 800 °C in an industrial firing furnace (Ultraflex, Despatch, USA). From the effective lifetime τ_{eff} of a symmetrical n^+pn^+ or p^+np^+ sample, the emitter saturation current density J_{0e} of the p^+ and n^+ surface was then extracted from the slope of the inverse lifetime vs. injection level curve at high-injection conditions (in the range of 5×10^{15} – 1.5×10^{16} cm^{-3}), using the relation proposed by Kane and Swanson (see Equation 2.15 and Fig. 2.1 in Chapter 2) [41].

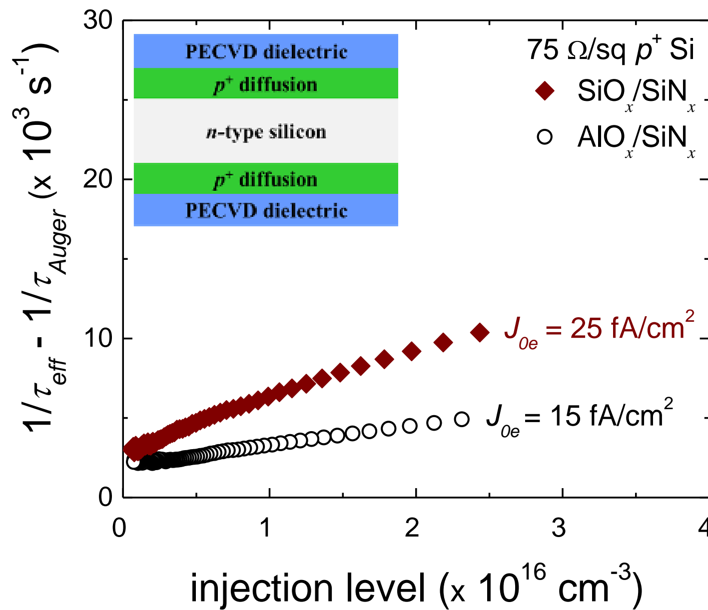

Figure 4.11: Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially-fired dielectrically passivated planar p^+np^+ samples. The p^+ sheet resistance is 75 Ω/square.

Figure 4.11 shows the measured Auger-corrected inverse effective carrier lifetimes as a function of injection level for 75 Ω/sq planar p^+ silicon passivated by industrially-fired PECVD SiO_x/SiN_x. For comparison, results obtained for p^+ silicon surfaces passivated by PECVD AlO_x/SiN_x are also included (more details in next chapter). It should be noted that a linear relationship was observed for the Auger-corrected effective lifetime curves with positively charged PECVD SiO_x/SiN_x dielectric stacks (allowing the extraction of J_{0e} values using Kane-Swanson relation), which is not the case for other positively charged dielectrics such as PECVD SiN_x [44, 160, 180].

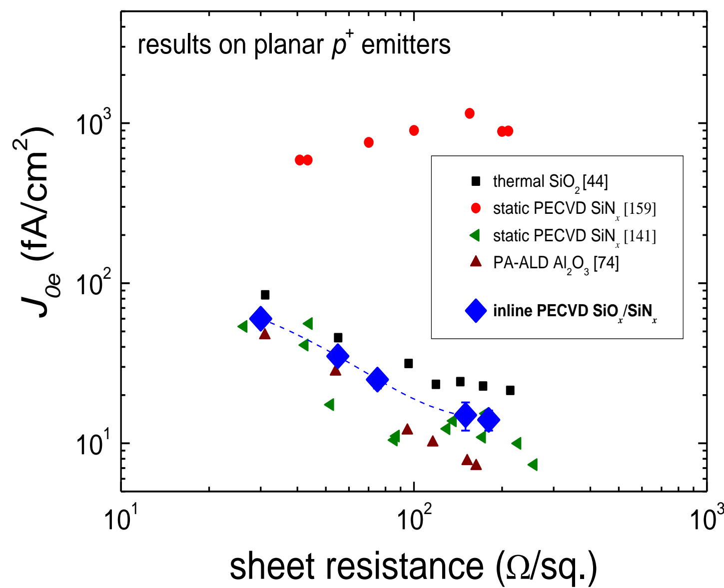

Figure 4.12.: J_{0e} values of p^+ emitters passivated by industrially-fired PECVD SiO_x/SiN_x stacks (large blue diamonds) as a function of p^+ sheet resistance. The dashed line is a guide to the eye. For comparison, other published results for passivated p^+ Si are also included from references [44, 74, 141, 159, 180].

Figure 4.12 shows J_{0e} results as a function of the sheet resistance. PECVD SiO_x/SiN_x stacks show excellent passivation results that are very close to the best published results on p^+ silicon [44, 74, 141, 159, 180]. It is important to emphasise that such high-quality passivation for a wide range of p^+ sheet resistance was achieved using a low-temperature positively-charged dielectric deposited in an industrial reactor and fired in an industrial firing furnace. Figure 4.13 shows the measured Auger-corrected inverse effective carrier lifetimes as a function of injection level for 70 Ω/sq planar n^+ silicon passivated by industrially-fired PECVD SiO_x/SiN_x. For comparison results obtained for n^+ silicon passivated by PECVD SiN_x were shown, which are considered to be the state-of-the-art technology for passivating phosphorus-diffused n^+ silicon. Figure 4.14

shows J_{0e} results as a function of the sheet resistance. Clearly these PECVD SiO_x/SiN_x stacks show excellent passivation on phosphorus-diffused n^+ silicon.

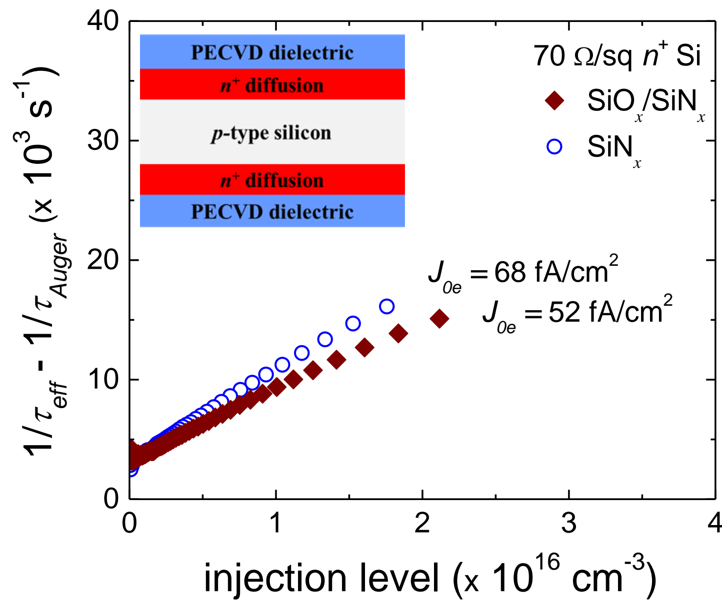

Figure 4.13.: Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially fired dielectrically passivated planar n^+pn^+ samples. The n^+ sheet resistance is 70 Ω/square.

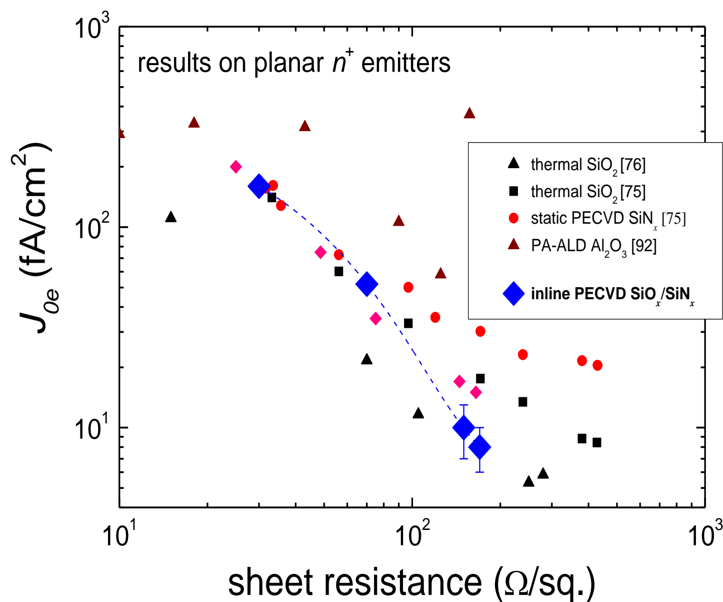

Figure 4.14.: J_{0e} values for p^+ emitters passivated by industrially-fired PECVD SiO_x/SiN_x stacks (large blue diamonds) as a function of n^+ sheet resistance. The dotted line is a guide to the eye. For comparison, other published results for passivated n^+ emitters are also included from references [75, 76, 92, 173].

In order to show good performance at the solar cell device level, it is important to have good optical properties (especially for front-side applications) in combination with excellent surface passivation results on textured surfaces. J_{0e} values for textured p^+ and n^+ silicon passivated with PECVD SiO_x/SiN_x stacks increases by a factor of 1.5 - 2.2, for a wide range of sheet resistances, a behaviour which is similar to that observed for other dielectrics [134, 180]. Reflection measurements show less than 2% weighted average reflection (weighted over the 300-1000 nm wavelength range of the solar spectrum) measured on random pyramid-textured Si surfaces passivated by SiO_x/SiN_x dielectric stacks. The hemispherical reflection (as a function of wavelength) of the samples was measured using spectrophotometry (Lambda 950, PerkinElmer, USA) in the 300-1000 nm range. Excellent surface passivation quality for both dopant polarities enables the use of these layers for back-side applications (e.g. for all-back-contact cells), while the good anti-reflective properties add value as this stack can also be used for front-side applications in *n*-type Si wafer solar cells (with good optical and passivation properties).

The surface passivation quality of our samples is mainly ruled by field-effect passivation (due to the built-in fixed charge density) and chemical passivation (due to a low interface defect density). In order to explain the surface passivation mechanisms, contactless corona-voltage (*C-V*) measurements were performed on three inline PECVD dielectrics (SiN_x, AlO_x/SiN_x and SiO_x/SiN_x) deposited on both surfaces of *n*-type undiffused Cz Si wafers. Figures 4.15 and 4.16 show the midgap interface defect density ($D_{it,midgap}$) and the fixed charge density (Q_f) for samples passivated by PECVD SiN_x, AlO_x/SiN_x and SiO_x/SiN_x, before and after firing. A decent interface defect density for both PECVD SiN_x and AlO_x/SiN_x stacks was measured, while PECVD SiO_x/SiN_x stacks exhibit excellent interface defect density with $D_{it,midgap}$ values of as low as ~3×10^{10} $eV^{-1}cm^{-2}$, see Fig. 4.15. PECVD SiO_x/SiN_x stacks also feature very low Q_f of about $+10^{11}$ cm^{-2} near the *c*-Si/SiO_x interface, which is much lower than the Q_f of the other dielectrics (see Fig. 4.16). Such a low charge in the dielectric is not effective for field-effect passivation. Therefore, the main mechanism behind the excellent passivation provided by our PECVD SiO_x/SiN_x stacks is the excellent interface quality.

The excellent results of PECVD SiO_x/SiN_x stacks on n^+ silicon can be explained by a better interface quality compared to the state-of-the-art PECVD SiN_x film, as observed in Figure 4.15. The excellent results by PECVD SiO_x/SiN_x stacks on p^+ silicon are mainly explained by the excellent interface quality compared to the other PECVD films used in this work. In addition, the very low positive fixed charge density in these stacks

was found to be not detrimental for p^+ silicon passivation, as it was insufficient to significantly increase the minority carrier (i.e. electron) concentration at the surface.

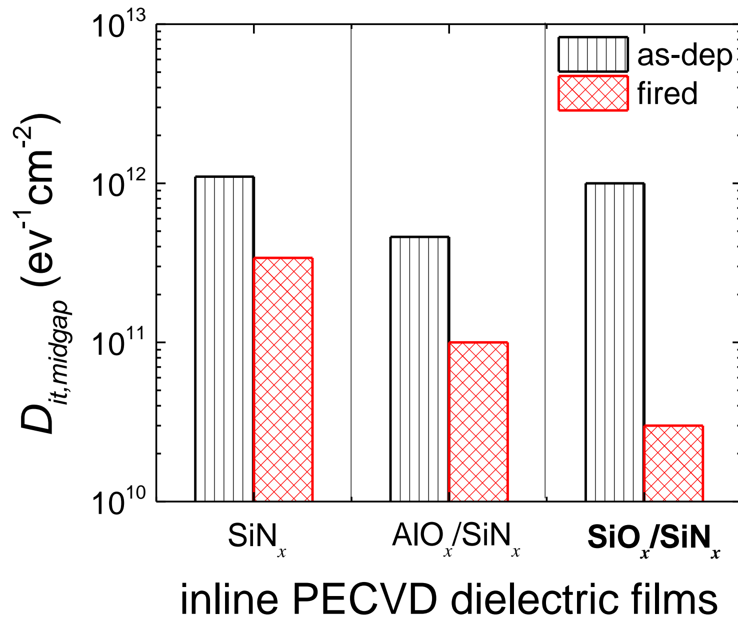

Figure 4.15.: Midgap interface defect density ($D_{it,midgap}$) for PECVD SiN_x, AlO_x/SiN_x and SiO_x/SiN_x passivated samples, before and after industrial firing.

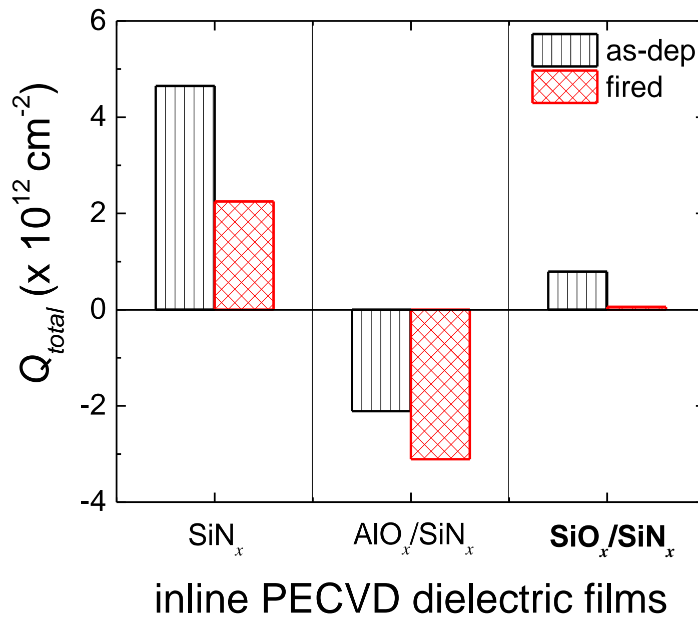

Figure 4.16.: Total charge density (Q_{total}) for PECVD SiN_x, AlO_x/SiN_x and SiO_x/SiN_x passivated samples, before and after industrial firing.

It is further corroborated from field effect measurements and device modelling that positively charged dielectrics can effectively passivate p^+ silicon surfaces, provided the

fixed charge Q_f is < $+1\times10^{12}$ cm^{-2} as long as the D_{it} remains low as shown in our previous work [181]. p^+nn^+ structures (textured on both sides) were also fabricated with homogeneous full-area n^+ and p^+ diffusions on n-type Cz Si wafers. After passivation with PECVD SiO_x/SiN_x stacks on both sides, implied V_{oc} values of > 700 mV (no metal contacts) were measured after industrial firing. This shows the potential for improved PV efficiency of these devices (double-side contacted solar cells) when passivated with the PECVD SiO_x/SiN_x stacks developed in this work.

Evaluation of optical properties of the PECVD SiO_x film

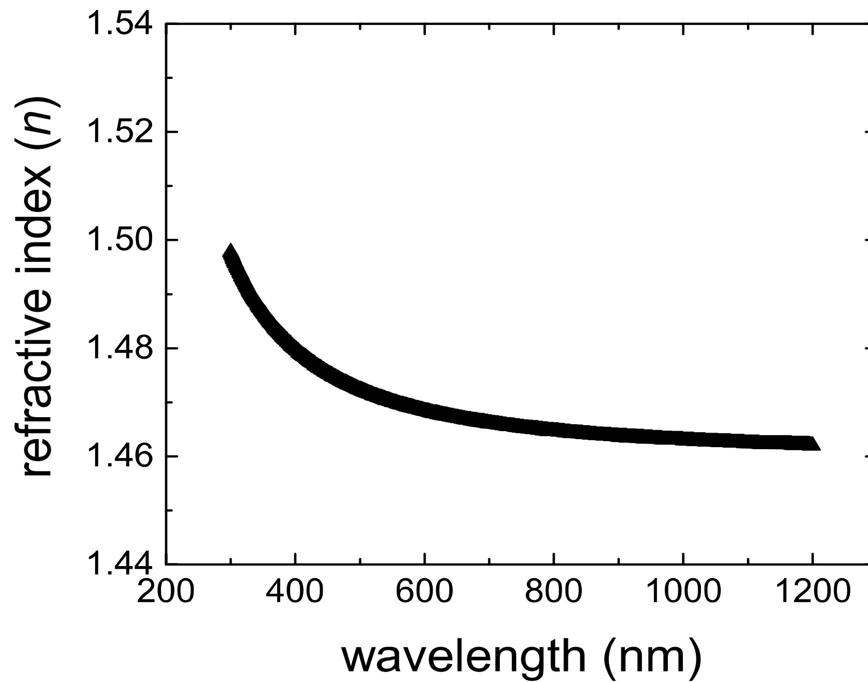

Figure 4.17.: Refractive index (n) of PECVD SiO_x film as a function of wavelength, as obtained from spectroscopic ellipsometry measurements. The extinction coefficient (k) was found to be below detection limit.

The optical constants (refractive index n and extinction coefficient k) were measured by spectroscopic ellipsometry (GES5, Sopralab, France). Figure 4.17 shows the refractive index of the single PECVD SiO_x film used in this work. The refractive index at $\lambda = 633$ nm is measured as 1.47, while the photon absorption was below the detection limit. This indicates that a thin PECVD SiO_x layer is optically transparent and has a similar behaviour as thermal SiO_2, and thus can be used in combination with a SiN_x film to serve as an effective antireflection coating on silicon. Reflection measurements showed less than 2% solar spectrum weighted average reflection (weighted over the 300-1000 nm wavelength range) measured on pyramid-textured Si surfaces passivated by 15 nm SiO_x film capped with a 70 nm SiN_x film dielectric stack, which confirms

that these stacks are suitable for application on the p^+ diffused front surface of textured n-type c-Si wafer solar cells.

4.5 Conclusions

In this work excellent surface passivation results are reported on all industrially relevant n and p-type silicon (i.e. n, p, n^+ and p^+) having both planar and textured surfaces by SiO_x/SiN_x stack. SiO_x were shown to deposit in low-temperature using PECVD and chemical process. Based on contactless corona-voltage measurements, the mechanism of surface passivation of SiO_x/SiN_x dielectric stacks was explained to be completely dominated by chemical passivation rather than field-effect passivation. As only a standard industrial firing process was used for activation of the surface passivation, this surface passivation scheme is fully industrially compatible. Good antireflective performance combined with excellent surface passivation capabilities makes these stacks a strong candidate for application in high-efficiency industrial n-type and p-type silicon wafer solar cells.

4.6. Publications arising from this Chapter

1. **S. Duttagupta**, F.-J. Ma, B. Hoex and A.G. Aberle, Excellent surface passivation of heavily doped p^+ silicon by low-temperature plasma-deposited SiO_x/ SiN_y dielectric stacks with optimised antireflective performance for solar cell application, *Solar Energy Materials and Solar Cells*, 120, pp. 204-208, 2014
2. **S. Duttagupta**, F.-J. Ma, B. Hoex, A.G. Aberle, Extremely Low Surface Recombination Velocities on Heavily Doped Planar and Textured p^+ Silicon using Low-Temperature Positively-Charged PECVD SiO_x/SiN_x Dielectric Stacks with Optimised Antireflective properties, **[Oral presentation]**, Proc. 39th IEEE PV Specialists Conference, Tampa, Florida, USA, June 2013.
3. S. Duttagupta, B. Hoex, A.G. Aberle, "Progress with industrially-feasible surface passivation of heavily-doped p-type and n-type crystalline silicon by PECVD SiO_x/SiN_x with optimised antireflective performance", **[Oral presentation]**, Proc. of 28th European Photovoltaic Solar Energy Conference, Paris, France, September 2013.
4. **S. Duttagupta**, P. K. Basu, F.-J. Ma, B. Hoex, A.G. Aberle, "Progress with Cost-Effective Surface Passivation of p^+ Silicon by PECVD SiN_x" **[Oral**

presentation], Proc. of 29th European Photovoltaic Solar Energy Conference, Amsterdam, The Netherlands, September 2014.

Chapter 5: Low-temperature plasma-deposited aluminium oxide (AlO_x) and stacks

5.1. Introduction

Research within the crystalline silicon (*c*-Si) wafer based photovoltaic (PV) community is driven by the necessity to decrease the costs per watt peak ($/$W_p$) of the solar cells and PV modules. As a consequence, the thickness of the Si wafers is being reduced and alternative *c*-Si material and production processes are being investigated. Presently, most wafer-based Si solar cells are fabricated from *p*-type wafers. A high-efficiency solar cell structure based on *p*-type wafers requires effective passivation of the undiffused *p*-type Si at the rear-side. Such is the case for *p*-type passivated emitter and rear cell (PERC) cells, *p*-type aluminium local back surface field (Al-LBSF) cells.

Although majority of the solar cells are based on *p*-type Si wafers, the relative insensitivity of *n*-type *c*-Si material to various impurities and recombination active defects (such as the B-O complex) could well result in a switch in the future to predominantly *n*-type wafers [33, 182]. These advantages are already exploited in today's highest-efficiency commercial silicon wafer solar cells produced by Panasonic and SunPower [10, 12]. The emitter of an *n*-type silicon wafer solar cell is either a heterojunction or a p^+-type *c*-Si layer formed by diffusion or ion implantation. The electronic passivation of the surface of the p^+ emitter has proven to be very challenging in past [159].

Considering the practical importance of *p*-type Si surface i.e. a moderately doped (undiffused) Si surface and a heavily-doped p^+-type Si surface; it is important to study negatively-charged dielectrics. This would be fundamentally a suitable choice because (a) negative charge repels the minority carriers (electrons) at the surface thereby reducing surface recombination rate (accumulation conditions are beneficial, see Fig 2.3 in Chapter 2 for more details), (b) accumulation conditions does not introduce artefacts originating increased bulk recombination (also briefly explained in Chapter 2, see Fig. 2.5).

In recent years, amorphous aluminium oxide (AlO_x) has received tremendous interest in the photovoltaic community for its application as a surface passivation film for

crystalline silicon wafer solar cells. Although the passivation properties were reported by Hezel and Jaeger back in 1989 [121], sadly the technology was dormant for ~15 years until Agostinelli *et. al.* used Al_2O_3 for rear surface passivation of *p*-type Si solar cells with spin-on sol-gel and atomic-layer-deposition (ALD) method [72, 183]. Soon after, series of outstanding surface passivation results were reported by Hoex *et al.*, Dingemans *et al.* using atomic-layer-deposition (ALD) method [57, 73, 74, 93, 184-186] and excellent solar cell results were demonstrated on *p*-type (>20%) and *n*-type silicon (~24%) [163, 187]. Several other techniques were evaluated like PECVD [95, 188], sputtering [189] and spatial ALD [190].

More precisely, AlO_x films provide excellent surface passivation on lightly doped *n*-type and *p*-type silicon as well as on heavy-doped p^+ silicon [57, 73, 74, 95, 184]. In addition to a low interface defect density (~10^{11} $eV^{-1}cm^{-2}$), a distinguishing property of AlO_x is the presence of a high negative charge density (10^{12} - 10^{13} cm^{-2}, in units of elementary charges) in the film. This is especially beneficial on *p*-type *c*-Si surfaces as the minority carriers (electrons) are effectively shielded from the *c*-Si surface. Due to its excellent surface passivation properties on *p*-type surfaces, AlO_x has mainly been considered for the application in *p*-type passivated emitter and rear cell (PERC) cells, *p*-type aluminium local back surface field (Al-LBSF) cells, and *n*-type passivated emitter and rear locally diffused (PERL) cells [99, 163].

Owing to the advantages of inline PECVD i.e. high-rate deposition (100 nm/min) and industrial applicability, this technology was established and high-quality films for surface passivation were developed in this thesis. As the inline PECVD process was relatively new (in 2009), a detailed process optimisation was required for optimum surface passivation results. In addition, more work was required for the development of high-quality surface passivation results especially after industrial high-temperature firing (instead of typical lab-type activation anneal i.e. forming gas anneal). Although passivation results on *p*-type silicon using inline PECVD AlO_x was already demonstrated in 2009 [95], it was required to obtain such high-quality passivation results on p^+-type Si, which is vital for *n*-type solar cells. Furthermore, ALD Al_2O_3 films provided excellent surface passivation on p^+ silicon for an arbitrary sheet resistance [74]. However, results are compromised for n^+ doped Si passivated by Al_2O_3 films grown by plasma-assisted and O_3-based atomic layer deposition (ALD) [92]. This can be a problem for application in solar cells where simultaneous passivation of Si surface is required for example, certain solar cell structures such as interdigitated back-contact (IBC) solar cells require simultaneous passivation of both dopant polarities [174].

Progress in research is essential in order to enable excellent passivation on both n^+-type and p^+-type c-Si surfaces using single AlO_x or a stack.

5.2. Surface passivation of moderately-doped *c*-Si

It is important to evaluate surface passivation performance on moderately-doped undiffused Si as this represents rear surface of some high-efficiency solar cell structure (e.g. PERC cell concepts). Figure 5.1 shows measured injection-level dependent τ_{eff} (left Y axis) of the passivated p- and n-type Si wafer and corresponding $S_{eff,max}$ (right Y axis) before and after industrial firing at peak temperature of 800 °C. Result are shown for both p-type *Cz* silicon [Fig. 5.1 (a)] and n-type *Cz* silicon [Fig. (b)]. The PECVD AlO_x are deposited using optimised conditions.

Table 5.1: Inline PECVD deposition parameters and film properties for the PECVD AlO_x used here (unless otherwise stated). The optimised heater set temperature (T), reactor pressure (p), plasma power (P), refractive index (n) and thickness (d).

Dielectric	Process gas	T (°C)	p (mbar)	P (W)	n at 633 nm	d (nm)
AlO_x	TMA [$Al(CH_3)_3$] + N_2O + Ar	350	0.10	1500	1.61	25

In as-deposited state the PECVD AlO_x shows inferior surface passivation with τ_{eff} of merely 10 µs ($S_{eff,max}$ = ~1000 cm/s) at $\Delta n = 10^{15}$ cm^{-3} for p-type *Cz* Si and τ_{eff} of 81 µs ($S_{eff,max}$ = ~70 cm/s) at $\Delta n = 10^{15}$ cm^{-3} for n-type *Cz* Si. Drastic improvement in surface passivation was observed after industrial firing with τ_{eff} of 560 µs ($S_{eff,max}$ = ~14 cm/s) at $\Delta n = 10^{15}$ cm^{-3} for p-type *Cz* Si and τ_{eff} of 4242 µs ($S_{eff,max}$ = ~1.5 cm/s) at $\Delta n = 10^{15}$ cm^{-3} for n-type *Cz* Si. Such an ultra-low $S_{eff,max}$ is an exceptional result that ensures outstanding surface passivation provided by the PECVD AlO_x. Importantly these results are obtained after industrial firing. It should be mentioned that AlO_x layer up to 100 nm can provide very good surface passivation after industrial firing process.

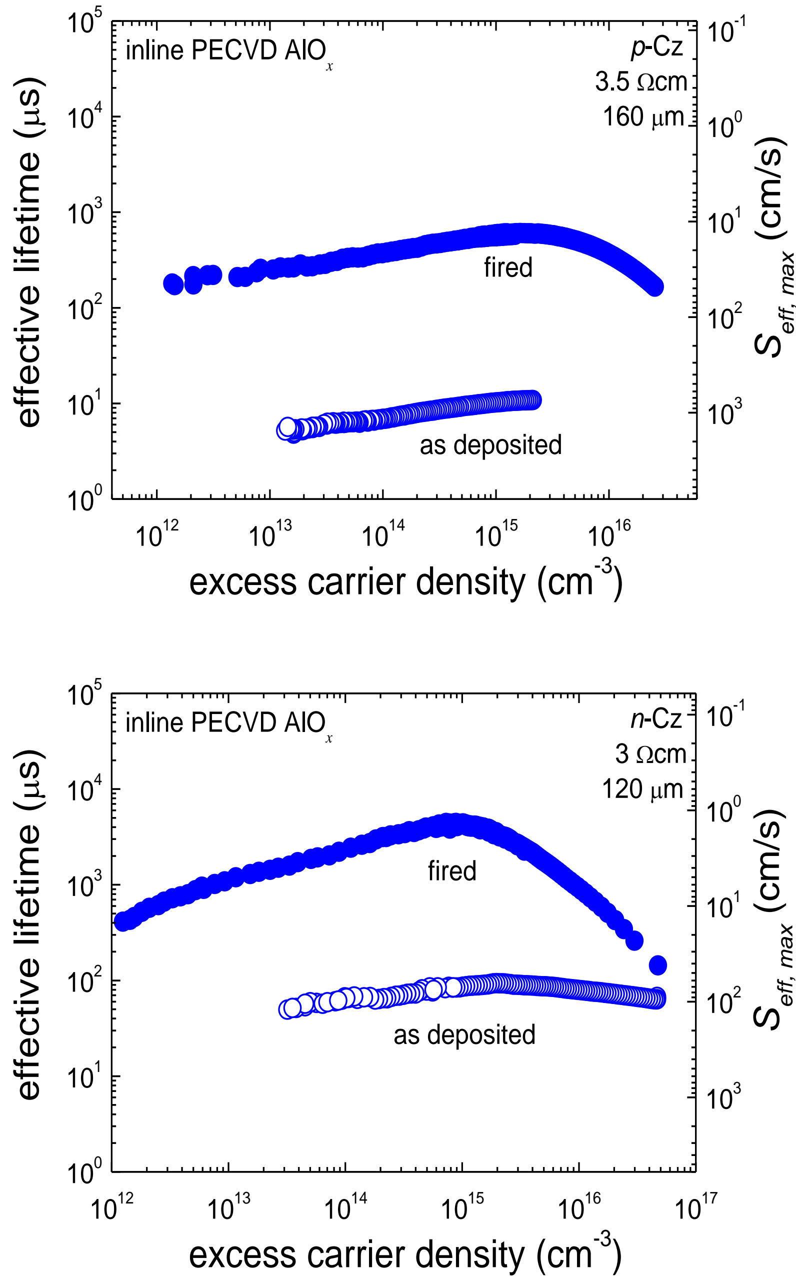

Figure 5.1: Measured injection-level dependent τ_{eff} (left Y axis) and corresponding $S_{eff,max}$ (right Y axis) before and after industrial firing at 800 °C for symmetrically PECVD AlO_x passivated **(a)** *p*-type *Cz* silicon **(b)** *n*-type Cz silicon.

5.2.1. Importance of capping layers

Although a thin PECVD AlO_x layer (without a capping layer) industrial firing is capable of providing excellent surface passivation results both on *p*-type and *n*-type silicon, however there are few reasons why capping layers are beneficial: (a) cost: TMA (tetra-methyl aluminium), is an expensive chemical. Reducing the usage with thinner

layer will ensure lower cost in the fabrication, (b) application perspective: when AlO_x is used for front-side application e.g. passivating the front p^+ layer of *n*-type solar cells, an effective antireflection coating is required. A SiN_x capping layer can serve this appropriately. Such a capping layer is also beneficial for rear-side application as well. A SiO_x capping layer is optically more suitable for rear-side application due to its lower refractive index than AlO_x. Thus it's important to study the surface passivation and performance of these stack layers, (c) improved stability: application of capping layer provides wider process window, a capping SiN_x also gives improved chemical stability. In addition when applied at the rear-side of the industrial screen-printed cells, a capping SiN_x or SiO_x protects the underlying AlO_x from metal paste interaction that can potential destroy or disintegrate the stability of the AlO_x if not capped suitably. Moreover, the use of a capping layers SiN_x or SiO_x ensures an effective hydrogenation of the surface defect states enhancing surface passivation results significantly.

Table 5.2: Inline PECVD deposition parameters and film properties for the PECVD dielectrics used as a capping layer in this work (unless mentioned otherwise). The optimised heater set temperature (*T*), reactor pressure (*p*), plasma power (P), refractive index (*n*) and thickness (*d*).

Dielectric	Process gas	*T* (°C)	*p* (mbar)	P (W)	*n* at 633 nm	*d* (nm)
SiO_x	$SiH_4 + N_2O$	200	0.15	700	1.47	70
SiN_x	$SiH_4 + NH_3$	300	0.20	2200	2.05	70

The surface passivation results of 25 nm AlO_x without a capping layer, AlO_x with a 70 nm SiN_x as a capping layer and AlO_x with a 70 nm SiO_x as a capping layer is shown in Fig. 5.2. In as-deposited state as expected the surface passivation is inferior, although minor improvements was observed for as deposited SiN_x and SiO_x capping layers. This is attributed to *in-situ* annealing of the PECVD AlO_x layer during deposition of the capping layers. After firing, the surface passivation capability is drastically improved irrespective of the use of any capping layers. It should be noted that the SiN_x capping layer resulted the best values with $S_{eff,max}$ of ~8.8 cm/s and as low as < 2 cm/s for *p*-type and *n*-type silicon, respectively. SiO_x capping layer resulted $S_{eff,max}$ of ~9.7 cm/s and < 2 cm/s for *p*-type and *n*-type silicon respectively. Thus application of both the capping layers yielded remarkable surface passivation.

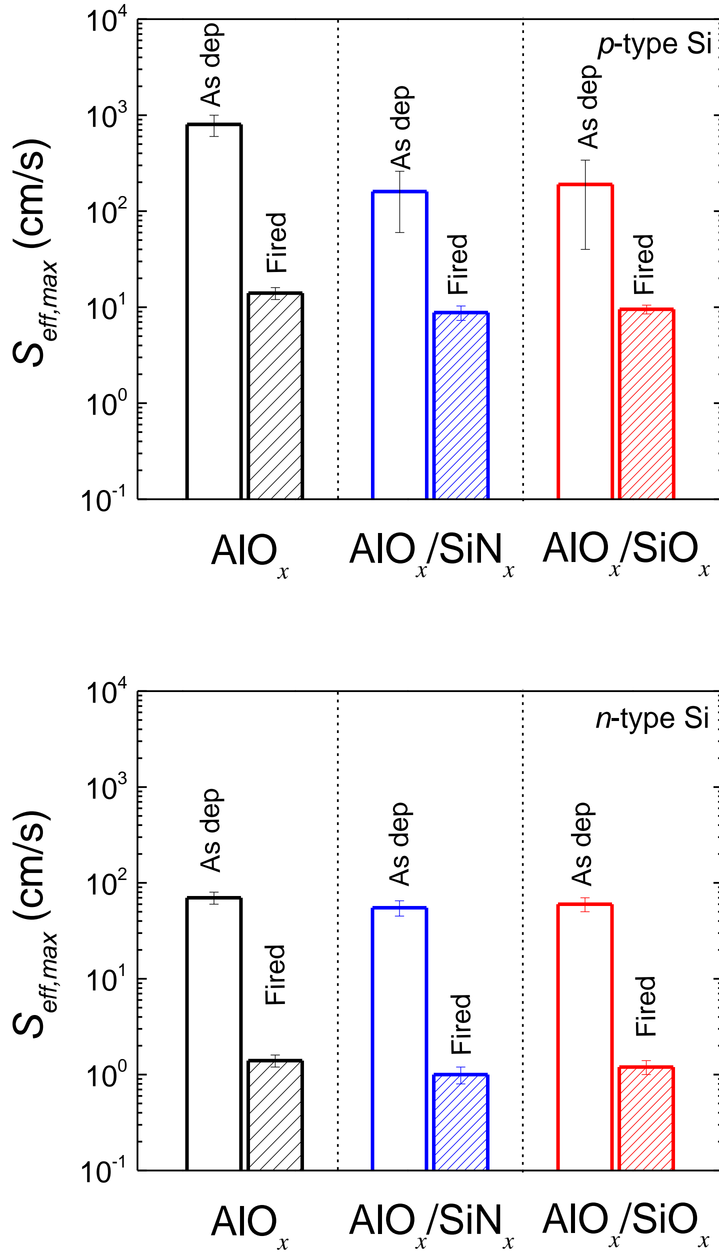

Figure 5.2: $S_{eff,max}$ at 10^{15} cm^{-3} as a function of AlO_x, AlO_x/SiN_x or AlO_x/SiO_x before and after industrial firing at 800 °C for **(a)** *p*-type *Cz* silicon **(b)** *n*-type *Cz* silicon.

5.2.2. Surface passivation mechanism

Contactless corona-voltage measurements was used for measuring total charge density (Q_{total}) and energy-dependent $D_{it}(E)$ required to investigate the electronic interface properties of these films. Figure 5.3 shows $D_{it,midgap}$ as a function of Q_{total} for the investigated AlO_x with or without capping layer SiN_x or SiO_x. As observed the as deposited films shows very high $D_{it,midgap}$, which explains the inferior passivation showed by

as-deposited films. After industrial firing the exceptionally improved passivation results are explained by drastic reduction in $D_{it,midgap}$ (9×10^{10} – 2.5×10^{11} $eV^{-1}cm^{-2}$) combined with significant increase in negative charge density (2.5×10^{12} – 7×10^{12} cm^{-2}). Based on these results the surface passivation mechanism for all the films investigated here is ruled by effective chemical as well as field-effect passivation.

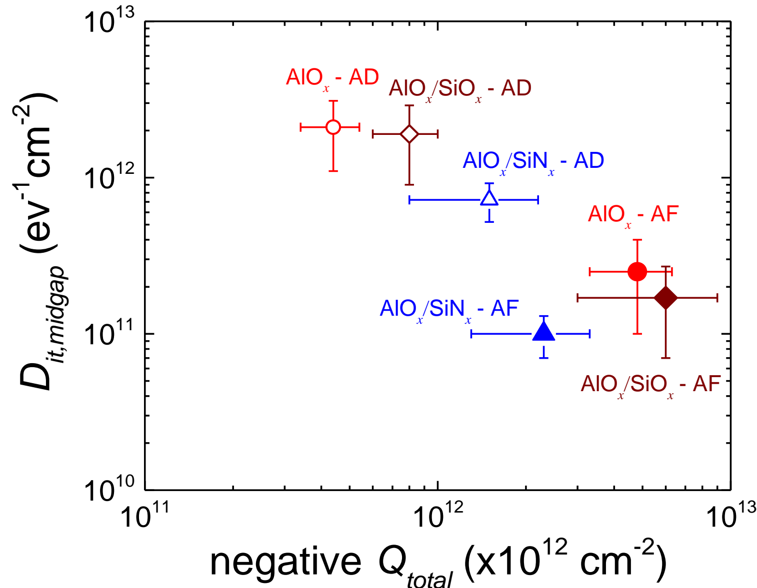

Figure 5.3: Measured $D_{it,midgap}$ as a function of negative Q_{total} for the investigated AlO_x with or without capping layer SiN_x or SiO_x. The results before and after industrial firing is presented.

5.3. Surface passivation of heavily-doped *p*-type *c*-Si

The p^+np^+ structures were fabricated as explained section 2.5. The boron dopant profiles of the p^+np^+ samples used in this work were measured by the ECV method, as shown in Figure 5.4. The *n*-type Si wafers were monocrystalline (Cz, phosphorus-doped, 6-8 Ωcm), about 150 μm thick, pseudo-square (125 mm × 125 mm), and with a (100) surface orientation. After the diffusion process, borosilicate glass layers were removed by dipping in HF solution, followed by rinsing in de-ionised water. Prior to the deposition of the PECVD dielectric films, the samples were cleaned using the RCA (Radio Corporation of America) clean with a final HF dip followed by water rinsing and drying to ensure an H-terminated surface. The sheet resistance of the p^+ diffusions was unaffected by the pre-deposition cleaning as confirmed by 4-point probe measurements. p^+np^+ samples with various sheet resistances were coated on both sides with 30 nm AlO_x capped with 70 nm SiN_x.

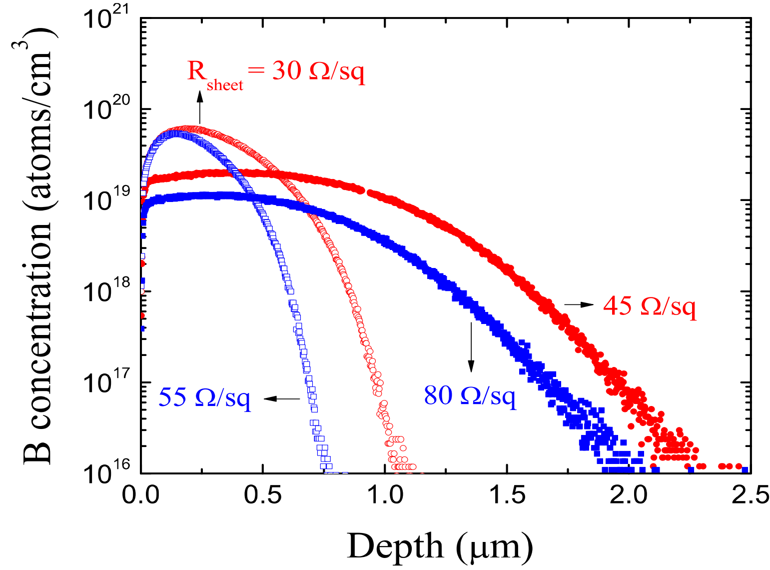

Figure 5.4: SIMS measurements of the boron profile of two boron-diffused Si wafers, before and after a high-temperature thermal oxidation process. Also shown are the sheet resistances measured with a 4-point probe instrument.

After the PECVD processes, the samples received an activation anneal in an industrial fast firing furnace (Ultraflex, Despatch, USA) for a few seconds at a set peak temperature of > 800 °C, similar to the co-firing step applied to the screen-printed metallization of industrial silicon wafer solar cells. The effective minority carrier lifetime (τ_{eff}) of the lifetime samples was measured using a contactless flash-based photoconductance decay tester (WCT-120, Sinton Instruments), in both the quasi-steady-state and the transient mode [24]. From the τ_{eff} measurement, the emitter saturation current density (J_{0e}) per side of the n^+pn^+ and p^+np^+ samples was extracted from the slope of the Auger-corrected inverse lifetime vs. injection level curve at high-injection conditions (Δn ~ 10^{15} - 10^{16} cm^{-3} in our case), using the relation proposed by Kane and Swanson [41].

Figure 5.5 shows the measured Auger-corrected inverse effective carrier lifetimes of a typical annealed p^+np^+ samples passivated on both sides with identical AlO_x/SiN_x dielectric stacks. The p^+ sheet resistances of these planar samples cover the range from 30 to 180 Ω/square, as shown in the figure. A linear relation between the Auger-corrected inverse lifetime and the injection level is observed at high-injection conditions (> 1×10^{16} cm^{-3}), enabling the extraction of J_{0e} values from these measurements. It should be noted that a linear behaviour is, for example, not observed if such

p^+ emitters are passivated by a SiN_x or SiC_x film [44, 191]. In the as-deposited state, the AlO_x/SiN_x stacks gave higher J_{0e} values of more than 700 fA/cm^2 for 180 Ω/sq B emitters, which indicate almost no passivation. However, as shown in Fig. 5.5, excellent passivation is obtained after the fast firing, resulting in very low J_{0e} values of 10-45 fA/cm^2. These results are comparable to the best values ever reported for passivated planar p^+ silicon emitters [74]. Assuming a short-circuit current density of 40 mA/cm^2 and an ideal diode law, the J_{0e} result for the 80 Ω/sq emitter represents a 1-sun open-circuit voltage limit of the solar cell of 736 mV at 25 ºC.

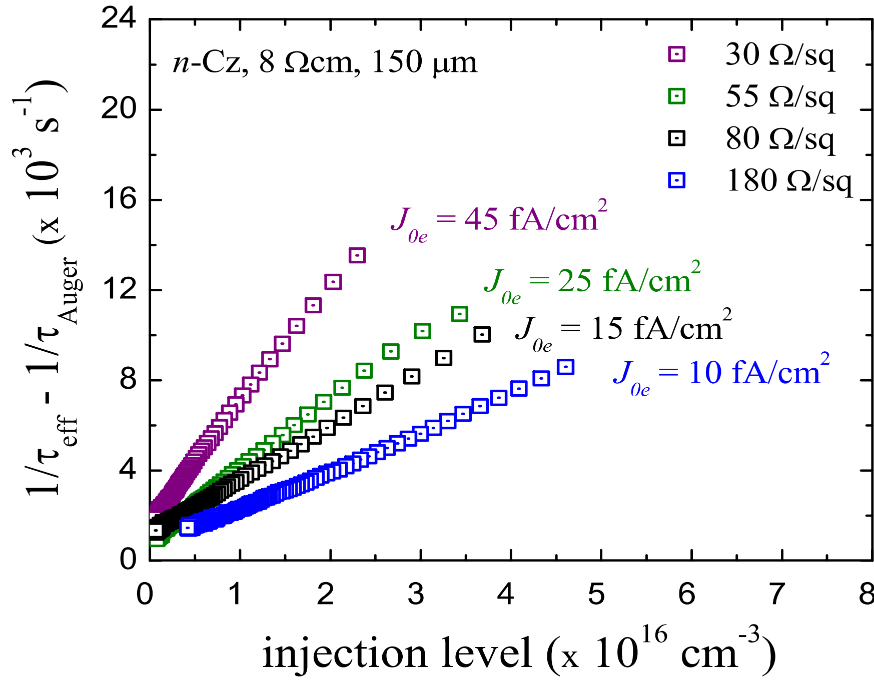

Figure 5.5: Measured Auger-corrected inverse effective lifetime as a function of the injection level, for four symmetrically passivated planar p^+np^+ samples. The passivation stack on each surface is 35 nm AlO_x/70 nm SiN_x. Prior to these measurements, the samples were annealed at ~750 ºC in an industrial fast firing furnace.

The J_{0e} improvement via the fast firing process is primarily due to hydrogenation, whereby atomic H present in the SiN_x film diffuses to the Si/AlO_x interface and reduces the interface state density ("chemical passivation"), thereby reducing the interface recombination rate. Another possible reason can be an increase of the built-in negative charge density in the AlO_x film due to the annealing step ("field-effect passivation"), as observed by Saint-Cast *et al.* for similar PECVD AlO_x films [95]. It is emphasised that in the present work the thermal activation of the AlO_x film was done using a process that is widely used in the PV industry, whereas in earlier work with ALD-grown Al_2O_3 films the thermal activation was done by a 30 minute anneal at 425 ºC in a N_2 environment. These results thus demonstrates that a standard industrial fast firing

process is sufficient for obtaining excellent passivation of p^+ silicon emitters with an AlO_x/SiN_x dielectric stack. This is an important result with respect to the industrial application of such stacks for silicon wafer solar cell application. It should also be noted that 25 nm PECVD AlO_x films without a capping SiN_x could also effectively be activated by a standard industrial firing process and resulted in similarly low J_{0e} values as obtained for the AlO_x/SiN_x stacks. A single AlO_x film, however, cannot simultaneously act as an efficient anti-reflection coating on the front surface of a high-efficiency *n*-type solar cell due to its low refractive index; thus, the focus in this work is on AlO_x/SiN_x stacks.

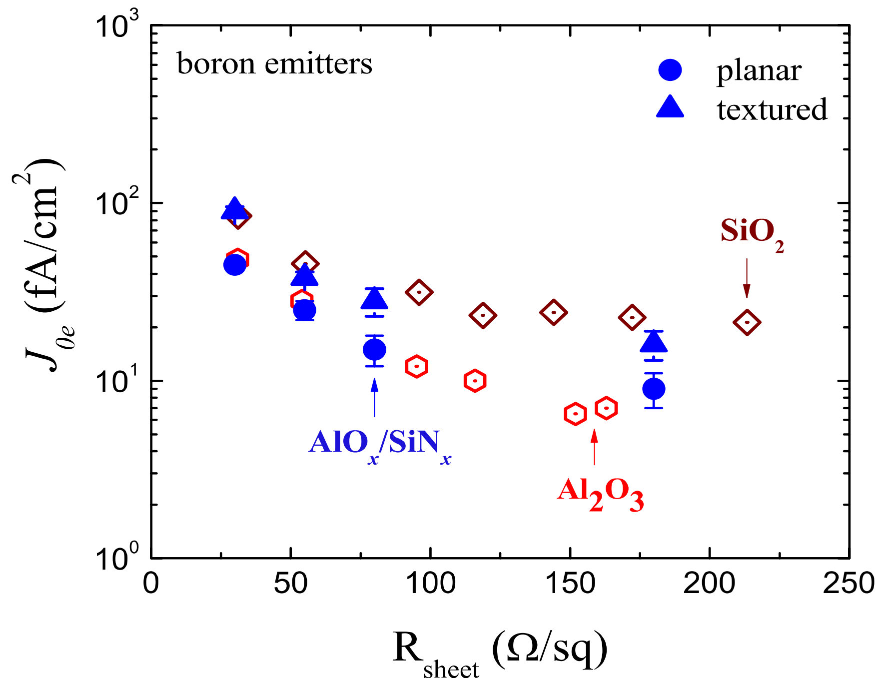

Figure 5.6: Measured J_{0e} values as a function of boron emitter sheet resistance passivated with AlO_x/SiN_x dielectric stack (this work) and compared with ALD-grown Al_2O_3 [7] and thermal SiO_2 [16]. For AlO_x/SiN_x dielectric stack, both planar and random-pyramid textured boron emitter passivation results are shown.

Figure 5.6 shows the extracted J_{0e} values as a function of the p^+-Si (boron emitter) sheet resistance (R_{sheet}). The passivation of planar p^+ emitters by AlO_x/SiN_x stacks in this work is compared with earlier published results for p^+ emitters passivated by ALD-grown Al_2O_3 [74] and thermal SiO_2 [44]. The AlO_x/SiN_x passivated p^+-Si samples, after industrial firing, show excellent passivation similar to that of annealed ALD-grown Al_2O_3 films. Several authors have reported J_{0e} values as a function of the boron emitter sheet resistance (see Fig. 5.6), however, only limited experimental data can be found in the literature for the passivation of pyramid-textured boron emitters for a range of

sheet resistances. We show that the passivated textured boron emitters demonstrate an increase in J_{0e} by merely a factor of 1.5-2 when compared to planar boron emitters. This increase is attributed to the larger surface area of the textured samples, giving a higher surface recombination rate. Another contributor could be differences in the boron concentration at the tops and bases of the Si pyramids. For a given sheet resistance, our J_{0e} values for AlO_x/SiN_x passivated pyramid-textured p^+ emitters are lower than those obtained on pyramid-textured n^+ emitters passivated by aluminium-annealed thermal SiO_2 or as-deposited a-SiN_x:H [75].

TMA is an expensive chemical; hence, it is important to investigate the minimal AlO_x thickness that is required in the AlO_x/SiN_x stack to obtain a good surface passivation for the p^+ emitter. Figure 5.7 shows the measured J_{0e} values (left axis) and corresponding implied V_{oc} values (right axis) as a function of the AlO_x thickness in the stack, for 80 Ω/sq planar boron emitters. It can be seen that the lowest J_{0e} values (and thus highest implied V_{oc}) are obtained for an intermediate AlO_x thickness of about 25 nm and that the J_{0e} increases (and implied V_{oc} decreases) for both thinner and thicker AlO_x films in the stack. The implied V_{oc} was extracted by a relation proposed by Sinton [13, 19, [24, 166]:

$$implied\ V_{oc} = \frac{kT}{q} ln \frac{(N_d + \Delta n)\Delta n}{n_i^2}, \qquad (5.1)$$

Figure 5.7 also shows that an AlO_x thickness of merely 5 nm in the stack still gives an excellent J_{0e} of 18 fA/cm^2 and an implied V_{oc} of 692 mV. For an AlO_x film thickness of above 75 nm blistering was observed after the fast firing furnace anneal, resulting in a strongly reduced level of surface passivation. This could be related to either a difference in thermal expansion coefficient between AlO_x and *c*-Si or the (violent) release of molecular hydrogen from the aluminium film during the high temperature firing step. Industrial Si wafer solar cells are textured in-order to minimise reflection losses, and hence the application of the developed AlO_x/SiN_x stack to industrial Si wafer cells requires optimisation with respect to its optical and electronic performance on textured surfaces. For example, a stack with 5 nm AlO_x capped with 65 nm SiN_x on textured (random pyramids) 55 Ω/sq boron emitters showed J_{0e} values of < 38 fA/cm^2 and good antireflection properties (2.3 % solar spectrum weighted average reflectance).

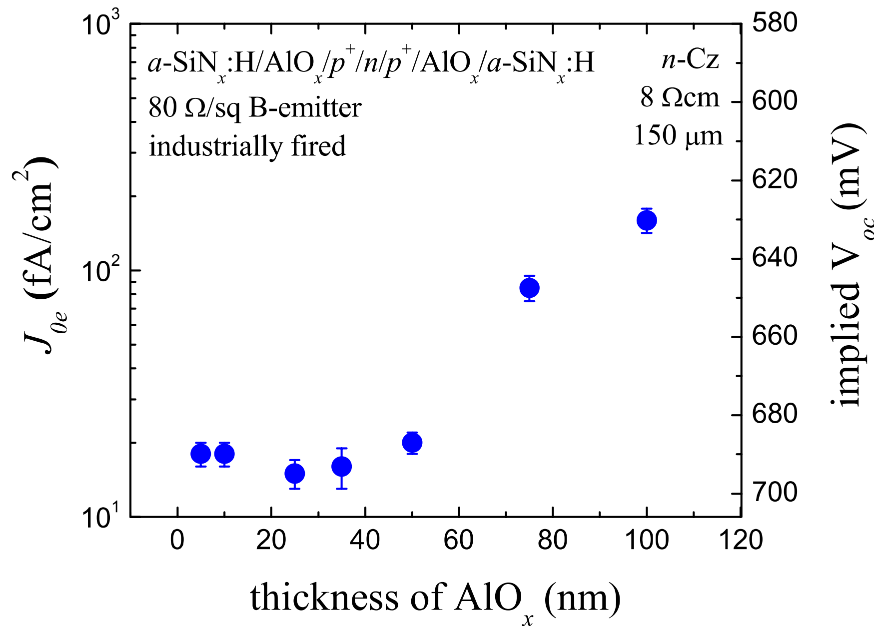

Figure 5.7: Measured J_{0e} values (left axis) and corresponding implied V_{oc} values (right axis) of planar 80 Ω/sq boron emitters as a function of the AlO_x thickness in the AlO_x/ SiN_x stack.

5.4. Surface passivation of heavily-doped *n*- and *p*-type *c*-Si

Excellent passivation of heavily-doped n^+ and p^+ silicon surfaces is very important for high-efficiency Si wafer solar cells. Some solar cell structures such as interdigitated back-contact (IBC) solar cells require simultaneous passivation of both dopant polarities [174, 192]. For this application preferentially a suitable dielectric is needed that can passivate both n^+ and p^+ silicon surfaces simultaneously. Thick (~100 nm) thermal silicon oxide (SiO_2) films or stacks consisting of a thin (5-30 nm) SiO_2 film capped by a 50-100 nm thick silicon nitride (SiN_x) film are often used due to their ability to passivate both n^+ and p^+ silicon surfaces [44, 160, 174, 175, 192]. However, low-temperature (< 400°C) surface passivation is typically preferred for the fabrication of industrial high-efficiency silicon wafer solar cells, due to its potential cost effectiveness, lower thermal budget and the possibility for inline processing. Recently, Mihailetchi *et al*. reported excellent results for p^+ surfaces passivated by a stack consisting of an ultrathin oxide grown by hot HNO_3 and then capped with a SiN_x film [165]. Although no specific results are available in regards to its capability of passivating n^+ silicon surfaces, it can be considered a good method for passivating both n^+ and p^+ silicon surfaces simultaneously as these layers have already been used for large-area screen-printed interdigitated back-contact (IBC) solar cells showing good efficiencies [176-179]. However, it should be noted that these devices showed

moderate implied V_{oc} (iV_{oc}) in the range of 660 - 680 mV and also resulted in moderate solar cell open-circuit voltages of $V_{oc} < 650$ mV [176-179]. It is also suggested in these publications that still an optimised dielectric is needed that can passivate both n^+ and p^+ silicon surfaces simultaneously in order to achieve higher open-circuit voltage and therefore higher solar cell efficiency.

AlO_x films provide excellent surface passivation on p^+ silicon for an arbitrary sheet resistance [74, 96, 180]. Recently it has been shown that n^+ doped Si in a certain sheet resistance range can also be passivated by Al_2O_3 films grown by plasma-assisted and O_3-based atomic layer deposition (ALD), however the results are not yet competitive [92, 193]. In addition, PA-ALD not yet an industrially feasible technique. Thus, it is of great interest to investigate if negatively-charged AlO_x films deposited by industrial PECVD can provide excellent passivation on both n^+ and p^+ silicon surfaces.

Symmetrical n^+pn^+ carrier lifetime structures were fabricated as explained section 2.5. The phosphorus dopant profiles of the n^+pn^+ samples used in this work were measured with the electrochemical voltage (ECV) method, as shown in Figure 5.8. The *p*-type Si wafers were monocrystalline (Cz method, boron-doped, 5-8 Ωcm), about 150 μm thick, pseudo-square (125 mm × 125 mm), and with a (100) surface orientation. The p^+np^+ structures were fabricated as explained section 2.5. The boron dopant profiles of the p^+np^+ samples used in this work were measured by the ECV method, as shown in Figure 5.9. The *n*-type Si wafers were monocrystalline (Cz, phosphorus-doped, 6-8 Ωcm), about 150 μm thick, pseudo-square (125 mm × 125 mm), and with a (100) surface orientation. After the diffusion process, the phosphorus or borosilicate glass layers were removed by dipping in HF solution, followed by rinsing in de-ionised water. Prior to the deposition of the PECVD dielectric films, the samples were cleaned using the RCA (Radio Corporation of America) clean with a final HF dip followed by water rinsing and drying to ensure an H-terminated surface. The sheet resistance of the p^+ and n^+ diffusions was unaffected by the pre-deposition cleaning as confirmed by 4-point probe measurements.

The n^+pn^+ and p^+np^+ samples with various sheet resistances were coated on both sides with 30 nm AlO_x capped with 70 nm SiN_x, using an industrial inline microwave-powered remote PECVD reactor (SiNA-XS, Roth & Rau, Germany). We emphasise that all samples (n^+pn^+ and p^+np^+) were processed without any change in the PECVD process conditions. The deposition conditions are summarized in Table I.

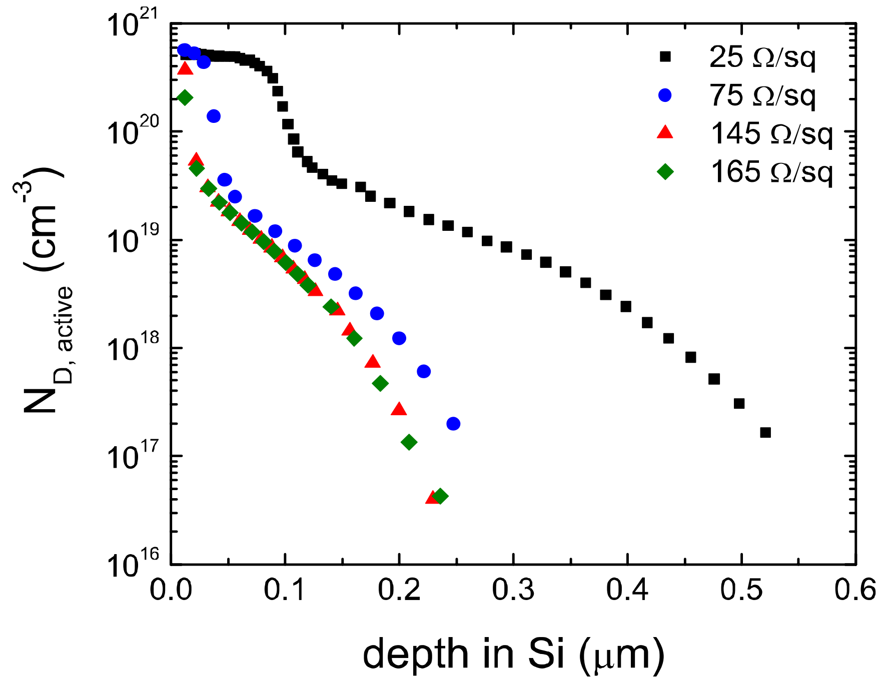

Figure 5.8.: Phosphorus dopant profile of $n^{+}pn^{+}$ samples measured by ECV profiling. The sheet resistance values determined by 4-point probe measurements are shown in the graph.

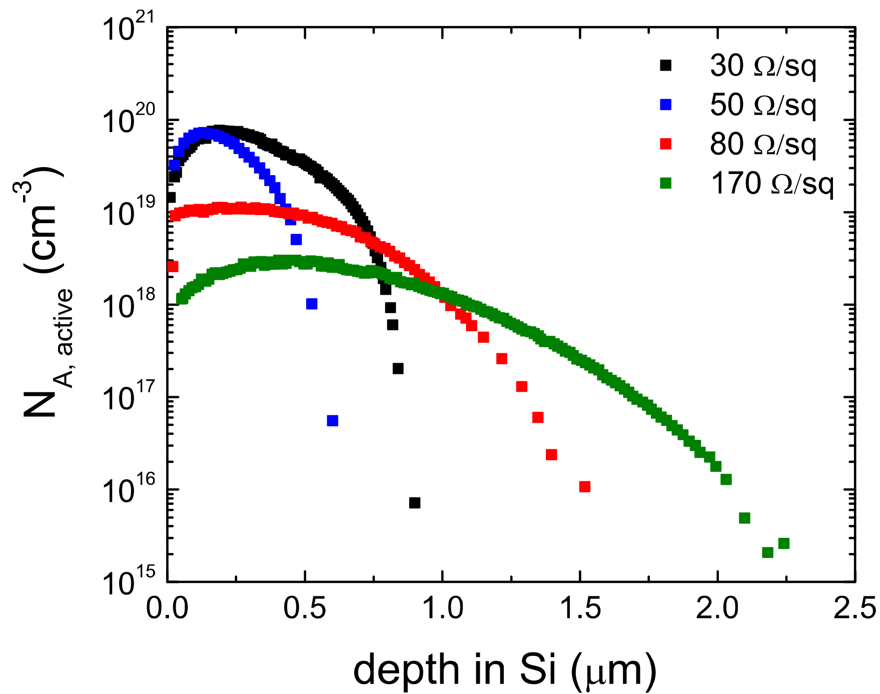

Figure 5.9.: Boron dopant profile of $p^{+}np^{+}$ samples measured by ECV profiling. The sheet resistance values determined by 4-point probe measurements are shown in the graph.

Table 5.3: Experimental details used for the deposition of the dielectric films in this study.

Dielectric	Process gas	Deposition temperature (°C)	Reactor pressure (mbar)	Plasma power (W)
AlO_x	$Al(CH_3)_3 + N_2O + Ar$	450	0.10	1500
SiN_x	$SiH_4 + NH_3$	200	0.20	3000

After the PECVD processes, the samples received an activation anneal in an industrial fast firing furnace (Ultraflex, Despatch, USA) for a few seconds at a set peak temperature of > 800 °C, similar to the co-firing step applied to the screen-printed metallization of industrial silicon wafer solar cells. The effective minority carrier lifetime (τ_{eff}) of the lifetime samples was measured using a contactless flash-based photoconductance decay tester (WCT-120, Sinton Instruments), in both the quasi-steady-state and the transient mode [24]. From the τ_{eff} measurement, the emitter saturation current density (J_{0e}) per side of the n^+pn^+ and p^+np^+ samples was extracted from the slope of the Auger-corrected inverse lifetime vs. injection level curve at high-injection conditions (Δn ~ 10^{15} - 10^{16} cm^{-3} in our case), using the relation proposed by Kane and Swanson [41].

Figure 5.10 shows the measured injection level dependence of the Auger-corrected inverse effective carrier lifetime of industrially fired n^+pn^+ samples passivated on both sides by a PECVD AlO_x/SiN_x dielectric stack. The results cover a wide range of industry-relevant sheet resistances (25-165 Ω/sq). It is emphasized that we observe a linear relationship for all lifetime samples, allowing the extraction of J_{0e} values using Kane-Swanson relation. This was not always the case in the work of Hoex *et al.* where it was mentioned that the relationship was not linear for 100-200 Ω/sq n^+ emitters passivated by PA-ALD Al_2O_3 [92]. This was attributed to the very high negative fixed charge density (up to 10^{13} cm^{-2}) of PA-ALD Al_2O_3 films, which strongly increased the minority carrier (hole) density at the n^+ surface in their work and thereby caused an injection level dependent J_{0e}. In the present work, we show an excellent level of surface passivation with extremely low J_{0e} values of 12 fA/cm^2 for 165 Ω/sq planar n^+ emitters passivated by PECVD AlO_x/SiN_x dielectric stacks after an industrial firing process. As a matter of fact, the J_{0e} values obtained in this study are similar to, or even better than, the best values reported in the literature for n^+ emitters passivated by PECVD SiN_x [75]. These results are also significantly better than those obtained for n^+ emitters passivated

by Al_2O_3 grown by ALD techniques reported so far [92, 193]. Identical PECVD stacks were also used to passivate p^+ emitters.

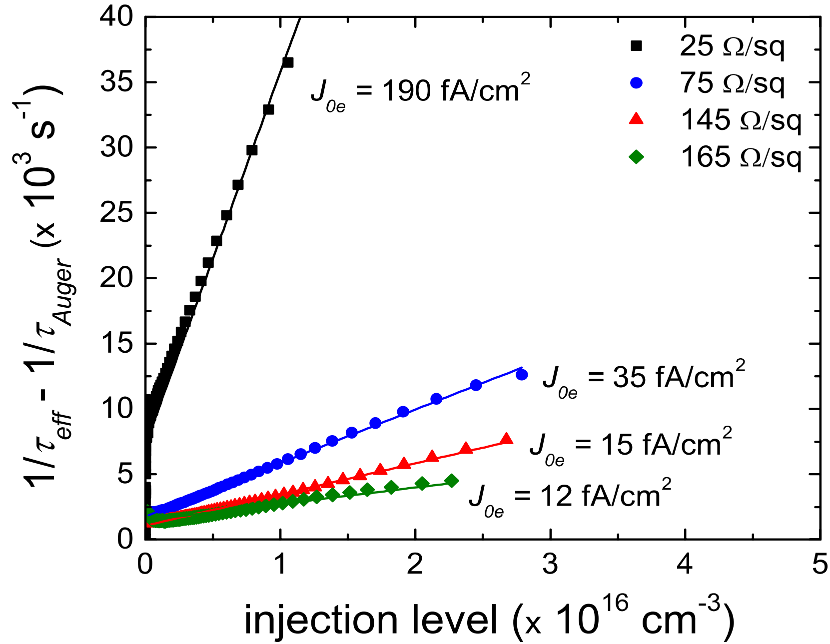

Figure 5.10.: Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially fired n^+pn^+ samples symmetrically passivated by PECVD AlO_x/SiN_x dielectric stacks (symbols). The sheet resistance of the n^+ emitters determined by four point probe measurements is shown in the legend. The J_{0e} values obtained from the straight-line fits (solid lines) are also shown.

Figure 5.11 shows the measured injection level dependence of the Auger-corrected inverse effective carrier lifetimes of industrially fired p^+np^+ samples passivated on both sides with an AlO_x/SiN_x dielectric stack. The lifetime samples show a clear linear relationship, indicating again that Kane-Swanson can be used to extract the J_{0e} value of this emitter. An extremely low J_{0e} value of 8 fA/cm^2 was obtained for a 170 Ω/sq emitter, which is comparable to the values obtained for p^+ emitters passivated by Al_2O_3 films grown by PA-ALD [74].

It should be noted that in the previous section (5.2), p^+np^+ samples were passivated on both sides with an AlO_x/SiN_x dielectric stack deposited in slightly different processing conditions. Here both n^+pn^+ and p^+np^+ samples were processed simultaneously with 100 °C higher deposition temperature for AlO_x and ~100 °C lower deposition temperature for capping SiN_x layer. This resulted in better interface quality and more importantly, slightly reduced fixed charge density. These stacks also provide excellent

results on p^+ Si surfaces for a wide range of sheet resistance with similar J_{0e} values as reported in previous section. Table 5.4 summarizes the experimentally measured effective lifetime (τ_{eff} at Δn = 10^{15} cm^{-3}), emitter saturation current density (J_{0e}), and implied V_{oc} (iV_{oc}) for n^+pn^+ and p^+np^+ samples symmetrically passivated by an industrially fired AlO_x/SiN_x dielectric stack. Note that effective lifetime and implied V_{oc} also depends on factors such as bulk doping level and bulk effective minority carrier lifetime of the silicon wafer used and the optical properties of the passivation coating, hence, care must be taken when comparing experimental values between different experiments.

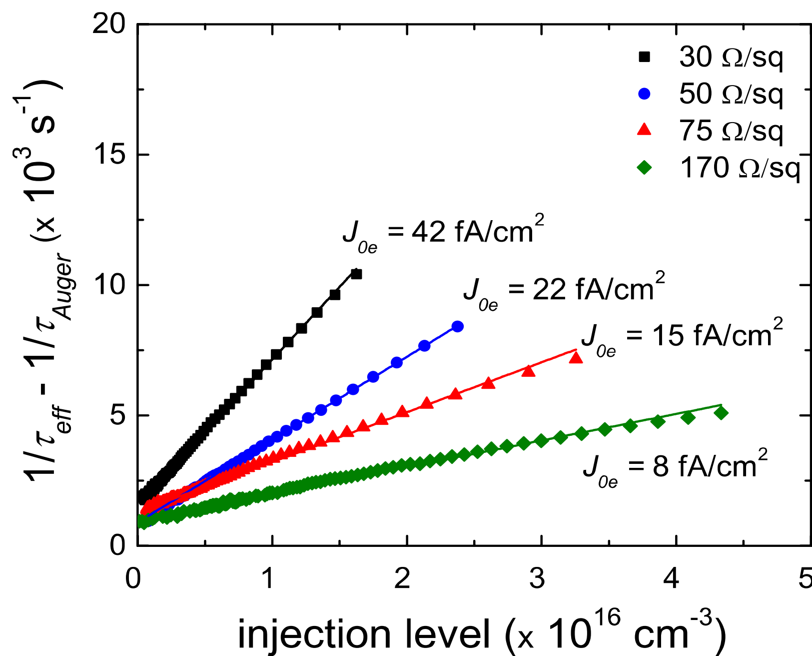

Figure 5.11.: Measured injection level dependence of the Auger-corrected inverse effective lifetime of industrially fired p^+np^+ samples symmetrically passivated by PECVD AlO_x/SiN_x dielectric stacks (symbols). The sheet resistance of the p^+ emitters determined by four point probe measurements is shown in the legend. The J_{0e} values obtained from the straight-line fits (solid lines) are also shown.

$V_{oc,limit}$ represents the one-Sun open-circuit voltage limit of a solar cell at 25 ºC calculated from the experimentally measured J_{0e} and assuming a short-circuit current density (J_{sc}) of 40 mA/cm^2 with an ideal diode law (n =1) by [24, 166]:

$$V_{oc,limit} = n\frac{kT}{q}\ln(\frac{J_{sc}}{J_{oe}} + 1),\dots\dots\dots\dots\dots(5.2)$$

where n is the diode ideality factor, which is considered one in this calculation. kT/q is 25.9 mV at 25 °C with k, T, q being the Boltzmann constant, absolute temperature in Kelvin and the elementary charge, respectively.

Table 5.4.: Experimentally determined effective lifetime (τ_{eff}) at Δn = 10^{15} cm^{-3}, saturation current density (J_{0e}) per side and implied V_{oc} (iV_{oc}) for n^+pn^+ and p^+np^+ samples symmetrically passivated by an AlO_x/SiN_x stack. The $V_{oc,limit}$ was calculated by Eq. 5.2 using the measured J_{0e} values.

	Sheet resistance for phosphorus-diffused n^+ surface on p-type Si (Ω/sq.)				Sheet resistance for boron-diffused p^+ surface on n-type Si (Ω/sq.)			
	25	**75**	**145**	**165**	**30**	**50**	**80**	**170**
τ_{eff} (µs)	94	465	770	700	484	841	700	930
J_{0e} (fA/cm^2)	190	35	15	12	45	22	15	8
iV_{oc} (mV)	640	688	706	703	670	690	700	712
$V_{oc, limit}$ (mV)	670	713	735	741	707	725	735	751

Figure 5.12 shows the experimentally obtained J_{0e} values for n^+ and p^+ emitters passivated by industrially fired PECVD AlO_x/SiN_x stacks. For comparison, the best published results from the literature are included as well. It should be noted that the preparation of the n^+ and p^+ emitters in the various studies were different and most likely resulted in different dopant profiles for a comparable sheet resistance. This potentially affects the Auger recombination losses in these emitters. However, the general trend can be used for comparison. It is evident from Figure 5.12 that thermal SiO_2 is a good candidate for both dopant polarities, showing excellent surface passivation of n^+ emitters and a decent surface passivation for p^+ emitters after either *alneal* (aluminium-annealing) or forming gas anneal (FGA) [44, 75, 76, 169].

PECVD SiN_x provides excellent passivation of n^+ emitters after forming gas anneal (FGA) [75]. Generally these SiN_x films provide a compromised level of surface passivation on p^+ emitters [44, 159]. Only limited reports are available where PECVD SiN_x provides a good level of surface passivation on p^+ emitters, however, the underlying mechanism is not yet properly understood [86, 141].

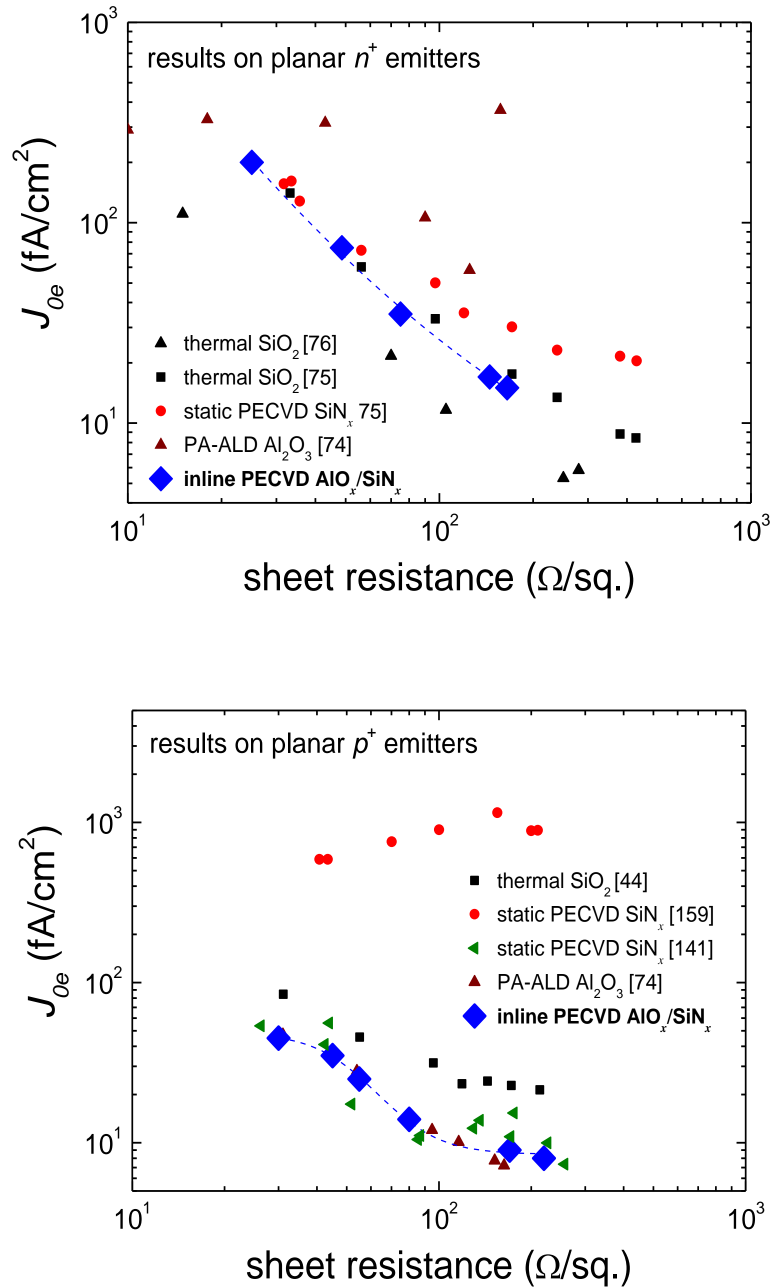

Figure 5.12: Experimentally obtained J_{0e} values (diamonds; this work) for **(a)** n^+ emitters and **(b)** p^+ emitters passivated by industrially fired PECVD AlO_x/SiN_x stacks (the dotted lines are guides to the eye). Each of our J_{0e} values is the average result of a batch of 10 samples. Also shown, for comparison, are state-of-the-art J_{0e} values reported in the literature for planar n^+ and p^+ emitters passivated by thermal SiO_2, PECVD SiN_x and ALD-grown Al_2O_3.

Similarly PA-ALD Al_2O_3 films provide only a moderate passivation on n^+ emitters [see Fig. 5.12(a)], however, p^+ surfaces with an arbitrary sheet resistance can be well

passivated with PA-ALD Al_2O_3 films [74, 92]. Based on the experimental results presented in this work it is clear that our industrially fired PECVD AlO_x/SiN_x stacks provide an excellent level of surface passivation on both n^+ and p^+ emitters, for the entire investigated sheet resistance range. Hence, our work demonstrates that these PECVD AlO_x/SiN_x stacks can be used to simultaneously passivate all *c*-Si surfaces that are of relevance in today's PV industry.

To obtain more insight into the interface properties such as fixed charge density (Q_f) and interface defect density (D_{it}) of our industrially fired AlO_x/SiN_x stacks, contactless corona-voltage (*C-V*) measurements were performed on undiffused Si samples. These measurements revealed that the industrially-fired AlO_x/SiN_x dielectric stacks on *c*-Si used in this work have a comparatively low mid-gap interface defect density of $< 10^{11}$ eV^{-1} cm^{-2} in combination with a moderate negative fixed charge density in the range of $(1\text{-}2)\times10^{12}$ cm^{-2}.

Understanding the surface passivation of p^+ Si surfaces by negatively-charged dielectrics is relatively straightforward. A low interface defect density provides excellent chemical passivation. In addition, the negative fixed charge density reduces the minority carrier concentration at p^+ Si surfaces (for the B surface concentrations investigated in this work) providing field-effect passivation. Understanding the passivation of n^+ Si surfaces by negatively-charged dielectrics is, however, not straight-forward. For this purpose we used advanced computer modelling (TCAD, Sentaurus) to study the role of field-effect passivation for heavily doped n^+ surfaces. In these simulations we take both the fundamental hole surface recombination velocity parameter (S_{p0}) and the interface fixed charge (Q_f) into account, similar to the approach presented by Girish *et al.* and Aberle *et al*. [16, 17] and furthermore using the physical models from Refs. [168, 169] S_{p0} is the surface recombination velocity parameter for holes assuming flat band conditions and can be expressed by:

$$S_{p0} \equiv v_{th}\sigma_p N_{st}, \quad (5.3)$$

where v_{th} is the thermal velocity, σ_p is the capture cross-section for holes and N_{st} is the number of surface states per unit area [19]. Using the measured n^+ dopant profile of the 75 Ω/sq diffusion from Fig. 5.8, J_{0e} vs. S_{n0} curves for various fixed charge densities were determined. The results are shown in Fig. 5.13. From Fig. 5.13 it is clear that positive fixed charge densities are beneficial for the passivation of the 75 Ω/sq n^+ Si

diffusion, resulting in significantly lower J_{0e} values for similar S_{p0} values. On the other hand a very high negative fixed charge density of 10^{13} cm^{-2} is found to be detrimental and results in higher J_{oe} values, in good agreement with the experimental results reported by Hoex *et al.* for n^+ Si passivated by Al_2O_3 films grown by PA-ALD [92].

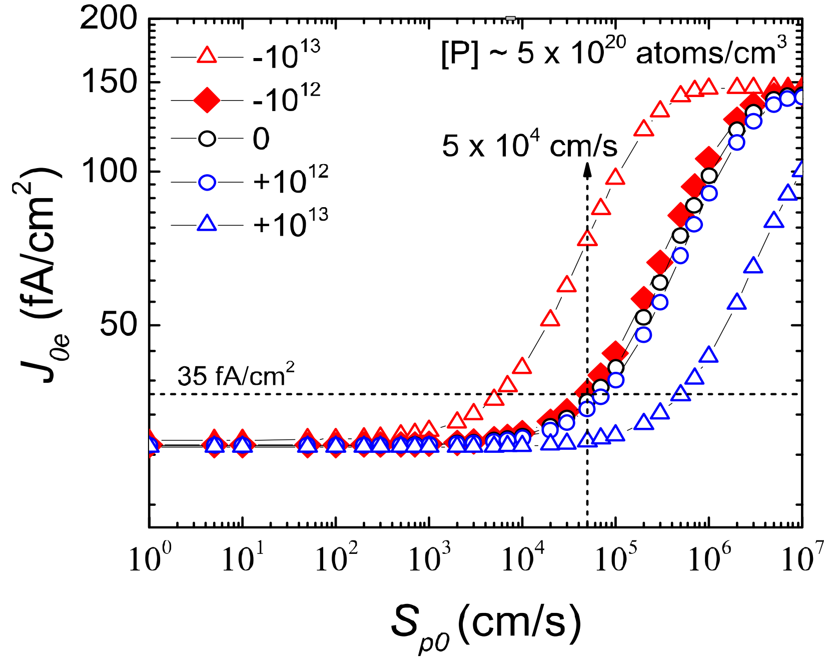

Figure 5.13: Simulated J_{0e} as a function of the S_{p0} at the *c*-Si/dielectric interface for high (10^{13} cm^{-2}) and moderate (10^{12} cm^{-2}) fixed charge densities of both polarities in the dielectric film. A symmetrical n^+pn^+ sample was used with a 75 Ω/sq diffusion per side (the experimental measured diffusion profile from Fig. 5.8 was used in the simulation).

For moderate fixed interface charge densities in the range of -10^{12} cm^{-2} to $+10^{12}$ cm^{-2} it can be seen that the fixed charge is hardly affecting the J_{0e} over the whole investigated S_{p0} range, and hence the passivation is predominantly ruled by chemical passivation in this case. It should be noted that a similar trend (effect of fixed charge) was observed on other n^+ diffusions used in this work; however the fixed charge range will depend on the surface dopant concentration. The results in Fig. 5.13 also allow us to extract the S_{p0} value at the interface between the *c*-Si wafer and the AlO_x/SiN_x stack. Taking the measured J_{0e} value of 35 fA/cm^2 and the measured Q_f of -10^{12} cm^{-2} we can see that this results in a S_{p0} value of ~5×10^4 cm/s. This value is in the similar order to the S_{n0} (electron surface recombination velocity parameter) value obtained by our PECVD AlO_x/SiN_x stack on heavily-doped p^+ Si surfaces, which is in the range of 10^4 cm/s [194]. It is observed that the S_{p0} value obtained in this work is slightly better than the S_{p0} reported by Altermatt *et al.* (> 10^5 cm/s) for n^+ Si having a surface dopant density of ~2×10^{20} atoms/cm^3 passivated by forming gas annealed thermal SiO_2 [169]. Hence,

these results indicate that heavily doped n^+ Si surfaces can be passivated as effectively as heavily doped p^+ Si surfaces using a negatively-charged PECVD AlO_x/SiN_x stack.

5.5 Conclusions

In conclusion, it was shown that moderately and heavily-doped *n*-type and *p*-type *c*-Si surfaces are well passivated by an industrially fired PECVD AlO_x/SiN_x dielectric stack. The obtained $S_{eff,max}$ and J_{0e} values are similar to the values reported in the literature for state-of-the-art Al_2O_3 films grown by plasma-assisted ALD. The thermal activation of the stack was performed in a commercial fast firing furnace, resulting in an overall process that is well suited for industrial production. Simultaneous passivation of heavily-doped *n*-type and *p*-type *c*-Si surfaces is an important step forward in surface passivation with AlO_x/SiN_x dielectric stacks, as some high-efficiency *c*-Si solar cell designs (for example all-back-contact and bifacial Si solar cells) require passivation of both dopant polarities. Based on contactless corona-voltage measurements and device simulations we show that a negatively-charged AlO_x/SiN_x stack with lower charge density can provide excellent passivation on both n^+ and p^+ *c*-Si surfaces, provided the interface defect density remains low. In combination with the excellent results obtained on undiffused *c*-Si surfaces, our work demonstrates that all *c*-Si surfaces of relevance in today's PV industry can be well passivated by a firing-stable, low-temperature deposited and industrially feasible dielectric stack.

5.6 Publications arising from this Chapter

1. **S. Duttagupta**, F. Lin, K. Devappa Shetty, A. G. Aberle and B. Hoex, Excellent boron emitter passivation for high-efficiency Si wafer solar cells using AlO_x/SiN_x dielectric stacks deposited in an industrial inline plasma reactor, *Progress in Photovoltaics: Research and Applications*, 21, 760-764, 2013.
2. **S. Duttagupta**, F. Lin, K.D. Shetty, M. Wilson, F.M. Ma, J. Lin, A.G. Aberle, B. Hoex, "State-of-the-art Surface Passivation of Boron Emitters on *n*-Type c-Si using Inline PECVD AlO_x/SiN_x Stacks for Industrial High-Efficiency Solar Cells", Proc. of 38th IEEE PV Specialists Conference (PVSC), Austin, Texas, USA, 3-8 Jun 2012
3. **S. Duttagupta**, F. Lin, T. Mueller, A. G. Aberle and B. Hoex, Progress in passivation of heavily *n*-type and *p*-type doped silicon surfaces by plasma-

deposited AlO_x/SiN_x dielectric stacks, *IEEE Journal of Photovoltaics*, 3, 1163-1169, 2013.

4. F. Lin, **S. Duttagupta**, K. Devappa Shetty, M. Boreland, A. G. Aberle and B. Hoex, Excellent passivation of p^+ silicon surfaces by inline PECVD SiO_x/AlOx stacks, *Japanese Journal of Applied Physics*, 51:10NA17, 2012.
5. F. Lin, **S. Duttagupta**, A.G. Aberle, B. Hoex, "Excellent passivation of n^+ and p^+ silicon by PECVD SiO_x/AlO_x Stacks", Proc. of 27th European Photovoltaic Solar Energy Conference, Frankfurt, Germany, September 2012.

Chapter 6: Dielectric charge tailoring in PECVD SiO_x/SiN_x stack and its impact on rear-side surface passivation of large-area *p*-type Al local back surface field solar cells

6.1. Introduction

The alloyed aluminium local back surface field (Al-LBSF) solar cell structure developed in the 1980s at Fraunhofer ISE [195-197] on *p*-type crystalline silicon (*c*-Si) wafers provides higher conversion efficiency compared to the conventional full-area alloyed Al-BSF solar cell. Using evaporated (and alloyed) Al rear contacts and positively charged thermal silicon dioxide (SiO_2) for rear passivation, cell efficiencies of up to 20.6% were realized in 1990 [195, 197]. In the 1990s, Aberle *et al*. at ISFH (Institut für Solarenergieforschung in Hamelin/Emmerthal) replaced the high-temperature grown thermal oxide by low-temperature plasma-deposited silicon nitride (hereafter SiN_x), which was shown to provide an excellent level of surface passivation on both *p* and *n*-type *c*-Si surfaces [108, 198]. High efficiencies of up to 20% were realized for rear SiN_x passivated Al-LBSF cells [198].

Hence, it was demonstrated back then that the positive charge in the rear dielectric film does not detrimentally affect the Al-LBSF solar cell efficiency when a local BSF exists underneath the metal contacts. In fact, from 2D simulation and experiments it seems that a higher positive insulator charge density can even improve the efficiency of Al-LBSF cells, by improving the short-circuit current density J_{sc} [199, 200]. In contrast, it is often mentioned that SiN_x can lead to compromised solar cell efficiency when applied on the rear of *p*-type Si solar cells with local rear contacts, see for example Ref. [201]. It should be noted that this is correct for the 'passivated emitter and rear contacted' (PERC) solar cell structure [202], which features a standard ohmic contact between the metal and the silicon wafer. This is attributed to the presence of an inversion layer induced by the high positive charge density in nearly stoichiometric SiN_x (N-rich) that causes a current flow between the inversion layer and the rear metal contacts. This leads to an effect called 'parasitic shunting' and particularly reduces J_{sc} [201]. Dauwe *et al.* showed that the use of Si-rich SiN_x reduced the effect of parasitic shunting [116].

Si-rich SiN_x generally exhibits lower positive charge density compared to nearly-stoichiometric SiN_x [124]. Consequently, Si-rich SiN_x leads to a poorly conductive inversion layer (or none at all), as explained in Ref. [116]. Thus, from both 2D simulations and the reviewed experiments, it can be understood that charge tailoring (both in terms of polarity and amount) within a dielectric is an interesting approach for improving both PERC and LBSF designs using the same dielectric film (or stack).

Past research has shown that plasma-enhanced chemical vapour deposition (PECVD) SiO_x/SiN_x stacks provide very good surface passivation on undiffused *n*-type and *p*-type *c*-Si wafers, with surface recombination velocity S_{eff} values < 2 and 11 cm/s, respectively on float-zoned (FZ) silicon [78, 81]. In 2012, Muenzer *et al.* reported the use of positively-charged PECVD silicon oxynitride (SiO_xN_y) and SiN_x stacks for rear passivation of Al-LBSF cells, resulting in full-area Cz cell efficiencies of close to 20% (with front selective emitter) [203].

Despite the clear importance of the fixed charge density in the dielectric film for the efficiency of Si solar cells, studies of tailoring the charge density in a dielectric (without changing its thickness or refractive index) are seldom found in the literature. The polarity and amount of fixed charge have a profound impact on the solar cell's operation. From a fundamental and technological point of view, it is important to further explore the possibility of tailoring the fixed charge density in dielectrics and to study its impact on the injection-level dependent surface recombination and solar cell efficiency.

6.2. Fabrication

6.2.1. Fabrication of symmetrical test structures for evaluation of surface passivation and electrical interface properties

Saw damage etched large-area (239.5 cm^2) *p*-type (~1.5 Ωcm) Cz Si wafers with (100) orientation and a thickness of ~160 µm were used for the fabrication of the test structure. Prior to the deposition of the PECVD dielectric stack, the samples were cleaned using the RCA (Radio Corporation of America) procedure [102] with a final HF dip to ensure an H-terminated surface followed by water rinsing and drying. A PECVD SiO_x layer (~30 nm) was deposited (using a N_2O and SiH_4 gas mixture) onto both surfaces at various deposition temperatures, followed by SiN_x (~70 nm) deposition at 400 ºC

(using a NH_3 and SiH_4 gas mix) on both sides of the wafer resulting in a symmetrically passivated lifetime structure. The experiment was carefully designed to maintain the SiO_x thickness constant at 30±2 nm. All PECVD films were deposited in a commercial inline microwave-powered remote PECVD reactor (MAiA, Roth & Rau AG). After the PECVD deposition, the samples received a post-deposition anneal in an industrial fast firing furnace (Camini, Roth & Rau AG) for a few seconds at a set peak temperature of 880 ºC. The S_{eff} were extracted from the effective lifetime τ_{eff} measurement using a contactless flash-based photoconductance lifetime tester (WCT-120, Sinton Instruments) [24], using the following relation:

$$S_{eff} = \frac{W}{2}\left(\frac{1}{\tau_{eff}} - \frac{1}{\tau_{bulk}}\right), \qquad (6.1)$$

where τ_{bulk} is the intrinsic bulk lifetime of the 1.5 Ωcm *p*-type Si wafers (using the model for FZ wafers of Ref. [26]) and W the wafer thickness. As all the samples assumed to have the same bulk quality and underwent the same process, iV_{oc} can be used to evaluate the impact of surface passivation on the performance of solar cells. Contactless corona-voltage measurements were carried out on a PV-2000 tool (Semilab) in order to extract $D_{it,midgap}$ and Q_{total} in the SiO_x/SiN_x stack. Total charge Q_{total} is defined as the amount of corona charge required to drive the initial condition (band bending due to the charge present in the PECVD layer) to a flat-band condition. It should be noted that the fixed insulator charge density Q_f is considered the main component in Q_{total} (for details see Ref. [51]). The procedure for extraction of these parameters is described in detail in Refs. [49, 51].

6.2.2. Fabrication of large-area Al-LBSF *p*-type Si solar cells

For fabrication of solar cells the saw damage etched wafers underwent alkaline texturing in a KOH/isopropyl alcohol (IPA)/DI water solution, resulting in a textured surface with upright random pyramids with a size of up to ~6 µm on both sides of the wafer. After a wet-chemical cleaning (RCA), all wafers underwent an inline phosphorus (n^+) diffusion ('homogeneous emitter') in a commercial in-line furnace (CALiPSO, Roth & Rau AG, Germany), resulting in a sheet resistance of 70 Ω/sq on both sides of the wafers. The phosphorus silicate glass (PSG) formed during the diffusion process was chemically etched. In the same process the rear n^+ layer was removed ('edge isolation') and the rear surface was smoothened. A SiO_x/SiN_x dielectric

stack was used for rear surface passivation. The wafers were then divided into two groups (each group containing 16 wafers) in order to investigate the impact of the SiO_x deposition temperature on the cell performance. For Group 1 a 30-nm SiO_x film was deposited at 200 ℃ and capped with a 70-nm SiN_x film. For Group 2 a 30-nm SiO_x film was deposited at 400 ℃ and capped with a 70-nm SiN_x film. The rear dielectric stacks were locally opened by laser ablation (line openings with 50 μm width with 1 mm pitch). Finally the metal contacts were formed by industrial screen printing. Four screen-printing steps were performed: In the first two steps the rear busbars and the front busbars – both used silver (Ag) paste – were printed. The full-area rear electrode was then printed using Al paste (whereby Al fills the ablated regions in the dielectric); lastly the front fingers were printed using Ag paste. Industrial co-firing was performed to form front and rear contacts, using a peak set temperature of ~880 ℃. This firing process ensures the formation of good ohmic contact at the front and rear surfaces and forms localized BSF regions (for Al-LBSF cells) and, in addition, it activates the surface passivation.

6.3. Results and Discussion

6.3.1. Evaluation of surface passivation and electronic interface properties

Figure 6.1(a) presents S_{eff} values measured at an excess carrier concentration of 1×10^{15} cm^{-3}, using Eq. 6.1 (shown in the left *y*-axis and assuming a bulk lifetime of 1.9 ms [26]) and the measured 1-Sun iV_{oc} (shown in the right *y*-axis) as a function of the deposition temperature of the PECVD SiO_x film. Note that the capping SiN_x film was deposited at a fixed deposition temperature of 400 ℃. We observe a strong dependence of the surface passivation quality on the SiO_x deposition temperature. As is evident from Fig. 6.1, the surface passivation quality varies by more than one order of magnitude when the SiO_x deposition temperature changes from 100 to 400 °C. An optimum passivation with $S_{eff} < 8$ cm/s was obtained for a SiO_x deposition temperature of 200 ℃, corresponding to an iV_{oc} of 715 mV. It should be noted that the reported S_{eff} can be considered as an upper limit, as commercial-grade low-resistivity *p*-type Cz wafers were used; the bulk lifetimes of these wafers are known to be lower than the intrinsic lifetime that was used to calculate S_{eff}.

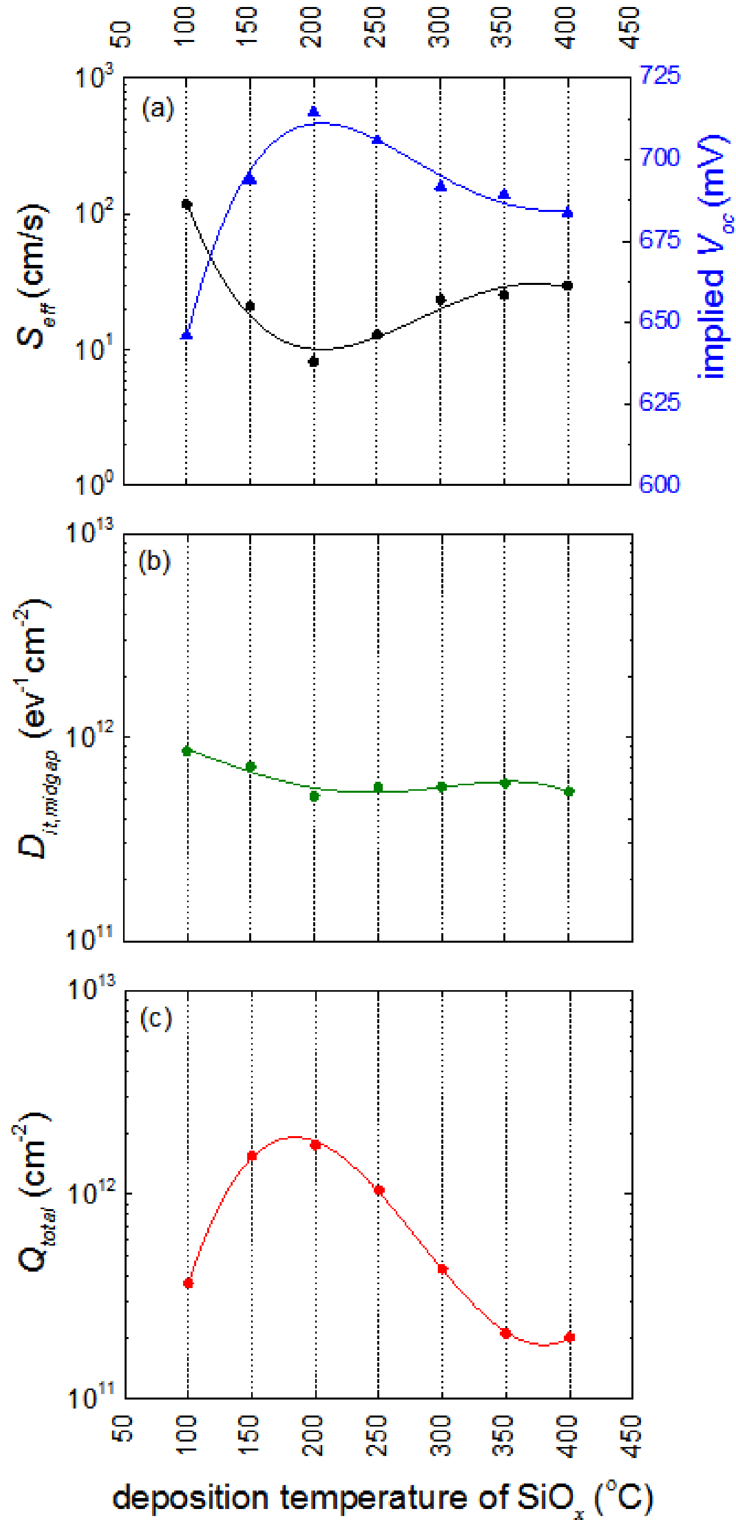

Figure 6.1: (a) Effective surface recombination velocity measured at an excess carrier concentration of 1×10^{15} cm^{-3} and iV_{oc} measured at 1-Sun as a function of the deposition temperature of the SiO_x film. **(b)** $D_{it,midgap}$ as a function of SiO_x deposition temperature. **(c)** Q_{total} as a function of SiO_x deposition temperature. Note: The capping SiN_x film was deposited at a fixed temperature of 400 °C and all lifetime samples were fired for a few seconds at a set peak temperature of 880 °C

In order to better understand the impact of Q_{total} and $D_{it,midgap}$ on the surface passivation, Figure 6.1 also presents each of them as a function of the SiO_x deposition temperature. It seems that $D_{it,midgap}$ is independent of the deposition temperature with a relatively low mid-gap value in the order of (5–6)×10^{11} $eV^{-1}cm^{-2}$ for deposition temperatures of ≥ 200 ºC [Fig. 6.1(b)]. This suggests that, regardless of the SiO_x deposition temperature, most of the defects at the Si/SiO_x interface are passivated by hydrogen from the overlying SiN_x film during the industrial firing process (i.e. reducing the dangling bond density at the Si surface). It is interesting to observe the behaviour of Q_{total} as a function of deposition temperature [Fig. 6.1(c)]. This trend mimics the trend of S_{eff}. It thus seems that the surface passivation quality of this set of samples is mainly ruled by Q_{total}, i.e. by field-effect passivation. The optimum surface passivation was achieved for a deposition temperature of 200 ºC, with Q_{total} = 1.75×10^{12} cm^{-2} and $D_{it,midgap}$ = 5×10^{11} $eV^{-1}cm^{-2}$.

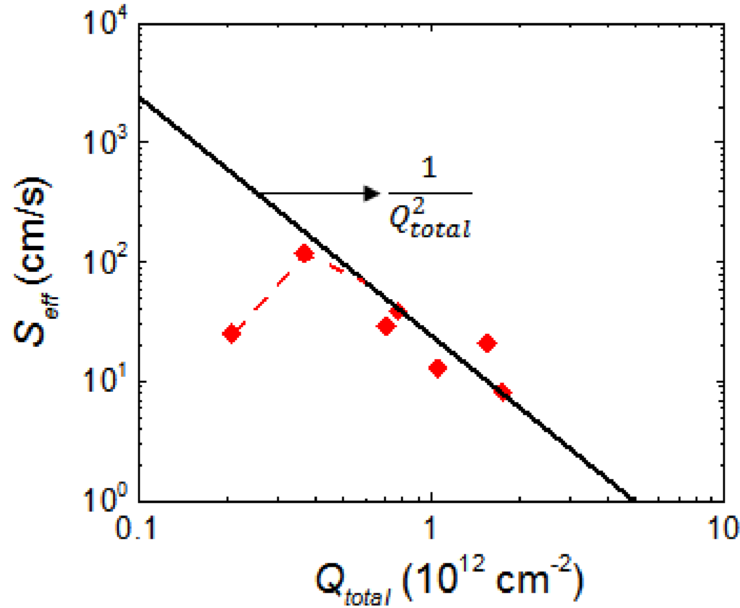

Figure 6.2: Effective surface recombination velocity S_{eff} for *p*-type 1.5-Ωcm Si surfaces as a function of experimentally measured positive Q_{total}. The black straight line represents the theoretically predicted S_{eff} vs. $1/Q^2_{total}$, behaviour for inversion conditions at the surface of the *p*-type Si wafer [46, 64, 65].

Figure 6.2 shows the relationship between measured S_{eff} and measured Q_{total}. For the investigated *p*-type Si wafers (1.5 Ωcm), the surface becomes inverted for an insulator charge density of about +3×10^{11} cm^{-2} [17]. As can be seen from Fig. 6.2, for inversion conditions, S_{eff} is proportional to the inverse square of the total positive charge density, in accordance to theory [64]. On the other hand, for charge values up to 3×10^{11} cm^{-2},

the surface remains under depletion conditions. These are known from theory to cause a maximum in the surface recombination rate at a particular surface band bending (i.e., insulator charge) [17]. This is also observed in our experiments, see the red dashed line in Fig. 6.2. This set of data also allows investigation of the impact of Q_{total} on the injection-level dependence of τ_{eff} thereby showing difference in the 1-Sun V_{oc} and maximum power point (*MPP*) voltage conditions (V_{mpp}).

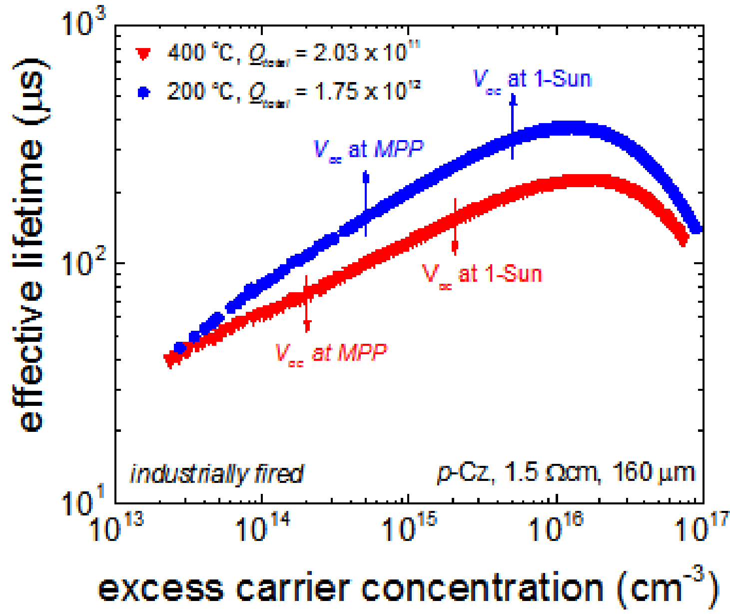

Figure 6.3. Measured τ_{eff} as a function of excess carrier concentration for symmetrically passivated *p*-type Cz Si wafers with PECVD SiO_x/SiN_x stacks, for two SiO_x deposition temperatures (200 and 400 °C).

Figure 6.3 presents the injection-level dependent τ_{eff} for two SiO_x deposition temperatures: a) 200 ºC, b) 400 ºC. As the measured $D_{it,midgap}$ values of these samples are similar [see Fig. 6.1(b)], the difference in the passivation quality can be totally attributed to the Q_{total} within the film. This is a unique set of experimental data since it demonstrates the impact of a one order of magnitude variation in insulator charge (with a constant $D_{it,midgap}$) on τ_{eff}. Normally, such experimental data and the modification of Q_{total} are studied by external corona charging, which often creates interface damage [62]. In Fig. 6.3, both the curves demonstrate a similar injection level dependence. It is possible that this injection level dependence results from an asymmetric bulk lifetime τ_{bulk} (since commercial-grade *p*-type Cz Si wafers were used, which are known to contain impurities with asymmetric capture cross sections, causing an injection-level dependent τ_{bulk} [204]). Note that, based on the studies by Aberle *et al*. [17], the surface lifetime $\tau_{surface}$ will not suffer from an injection-level dependence since the Q_{total} is high

enough ($Q > 5\times10^{11}$ cm^{-2}) to cause inversion. This is especially the case for the 200 ºC sample where the charge is 1.75×10^{12} cm^{-2}. Based on the results from Fig. 6.3, it appears that the τ_{eff} curve for the higher positive charge density shows higher 1-sun V_{oc} and V_{mpp} potential.

6.3.2. Al-LBSF solar cell results

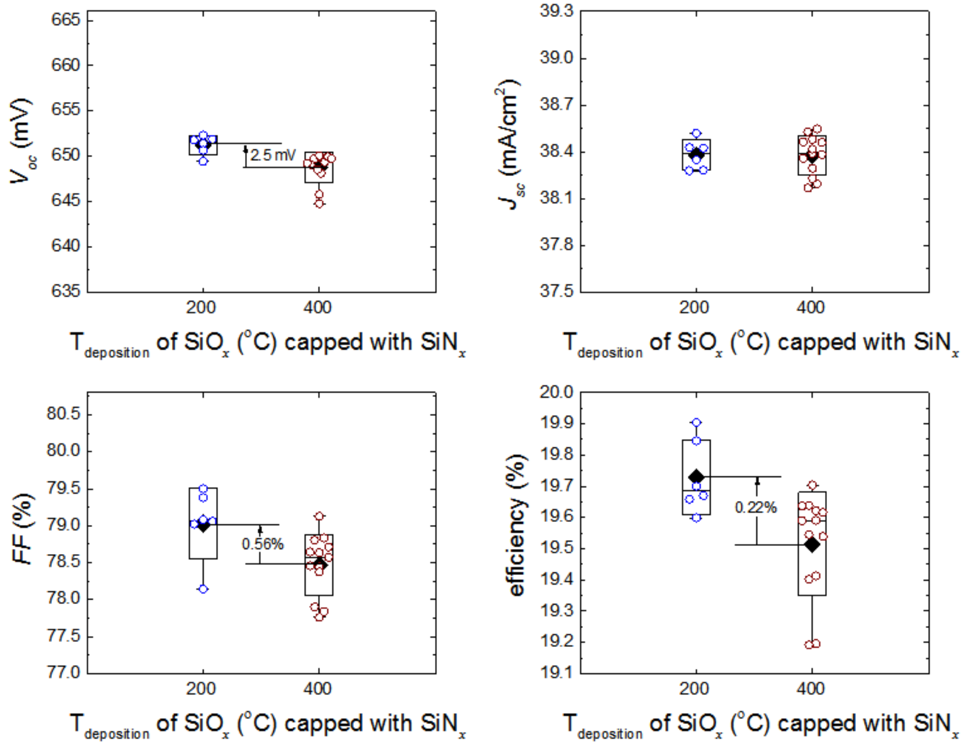

Figure 6.4: One-Sun current-voltage (*I-V*) parameters (V_{oc}, J_{sc}, *FF*, *Eff*) measured under standard testing conditions (25 °C, 100 mW/cm^2, AM 1.5 G) for Al-LBSF silicon solar cells with SiO_x/SiN_x rear passivating dielectric stacks, for two different deposition temperatures ($T_{deposition}$) of the SiO_x film. The solid diamonds are the mean value of the corresponding solar cell parameter. For the ease of comparison of the four graphs, the Y-axis of each graph was scaled such that the top value of each Y-axis is about 5% larger than its bottom value.

Owing to the results discussed in the previous section, two deposition temperatures were selected (200 and 400 ºC) for the SiO_x process and Al-LBSF solar cells were fabricated. The measured 1-Sun current-voltage (*I-V*) parameters are shown in Fig. 6.4. The SiO_x film deposited at 200 ºC provided an almost 10 times higher Q_{total} compared to the one deposited at 400 ºC. As expected from the results shown above, the Al-LBSF

cells with SiO_x deposited at 200 ºC showed an enhanced efficiency (0.22% average absolute improvement) compared to the batch of cells with SiO_x deposited at 400 ºC. This is mainly due to improvements in the cell V_{oc} by 2.5 mV (average) and FF by 0.56% absolute (average). This is in agreement with Fig. 6.3, as higher 1-Sun V_{oc} and V_{mpp} were measured on the lifetime test wafers. The reason for the FF improvement is still under investigation, however a possible explanation to this increase is the impact of the injection dependence of ideality factor in the voltage range between *MPP* and open circuit conditions. It was suggested in 2D simulations [199] that a higher positive insulator charge density (for example using our 200 ºC deposited SiO_x film) in combination with a LBSF (instead of a standard ohmic contact) can improve the cell J_{sc} by ~1.7 mA/cm^2. However, this was not observed in this study, as no change in J_{sc} was observed. A better understanding of the impact of charge tailoring on the solar cell's operation is critical. More experimental work along with multidimensional modelling is needed to further investigate the impact of the polarity and the magnitude of Q_{total} on Al-LBSF and PERC cells, which is beyond the scope of this paper. As a proof of concept, these initial results are quite promising, indicating the significant potential of charge tailoring on industrial Al-LBSF silicon solar cells.

6.4. Conclusions

Excellent surface passivation results were reported with industrially fired PECVD SiO_x/SiN_x stacks on undiffused *p*-type commercial-grade Cz silicon surfaces with S_{eff} of ~8 cm/s and very high implied V_{oc} of up to 715 mV. Experimentally the charge density in SiO_x/SiN_x dielectric stacks deposited by an industrial low-temperature PECVD method was varied by up to one order of magnitude ($10^{11} – 10^{12}$ cm^{-2}), without any impact on $D_{it,midgap}$. These films feature good interface quality ($D_{it,midgap}$ ~5×10^{11} eV^{-1}cm^{-2} after industrial firing), which is independent of the SiO_x deposition temperature. The fundamental relationship between Q_{total} and S_{eff} was verified, which previously was investigated only by simulations or external corona charging. Injection-level dependent effective carrier lifetime curves and measured charge densities showed higher cell V_{oc} and FF potential achievable with higher positive fixed insulator charge (under the assumption that the $D_{it,midgap}$ remains constant in the finished solar cells). As a proof-of-concept, Al-LBSF cells were fabricated with films having either relatively high or low positive insulator charge density. The films with higher positive charge density used as the rear passivating layer showed improved conversion efficiency by 0.2% (absolute), which came mainly from an improvement in V_{oc} and FF. The results indicate

that dielectric charge tailoring is a very effective and promising approach for silicon solar cells, and has both fundamental and technological relevance.

6.5. Publications arising from this Chapter

1. **S. Duttagupta**, Z. Hameiri, T. Grosse, D. Landgraf, B. Hoex, and A.G. Aberle Submitted to IEEE Journal of Photovoltaics (J-PV), 2014.
2. **S. Duttagupta**, Z. Hameiri, B. Hoex, and A.G. Aberle, "Dielectric charge tailoring in PECVD SiO_x/SiN_x stacks and its impact on industrial *p*-type silicon wafer solar cell efficiency," **[Oral presentation]**, Proc. of 40th IEEE PV Specialists Conference (PVSC), Denver, Colorado, USA, 7 - 13 Jun 2014.

Chapter 7: Investigation of rear surface passivation schemes for large-area *p*-type Al local back surface field solar cells

7.1. Introduction

Due to the continuous decrease in wafer thickness and desire for higher energy conversion efficiency of *c*-Si wafer solar cells, electronic and optical losses at the rear surface are becoming increasingly important [20]. Thin films deposited at low temperature (< 450 °C) such as silicon oxide (SiO_x), silicon nitride (SiN_x), amorphous silicon (*a*-Si:H), and more recently, aluminium oxide (AlO_x) and their stacks are constantly being evaluated for this purpose and have been successfully applied for efficiency improvements [11, 57, 79, 99, 116, 163, 205-208]. Rear surface passivation is especially important for high-efficiency solar cells (> 20 % efficiency) where it is important to reduce the effective surface recombination velocity at the rear to values below ~ 100 cm/s after metallization [20, 145]. High-efficiency solar cell structures based on *p*-type silicon substrates such as 'aluminium local back surface field' (Al-LBSF), 'passivated emitter rear contacted' (PERC) and 'passivated emitter rear locally diffused' (PERL) silicon wafer solar cells are widely expected (see the ITRPV roadmap [98]) to be the next "mainstream" industrial solar cell structures. These structures have the rear surface passivated by a thin film that improves the performance of the solar cells both electronically and optically. Thus it is important to evaluate and understand the impact of different rear surface passivating dielectrics on the performance of solar cells.

The operation of high-efficiency Si solar cells is significantly influenced by the surface recombination behaviour of rear-passivating dielectrics, for example an injection-level dependent surface recombination velocity (giving a 'non-linear' cell behaviour) [13, 19, 209-211]. The polarity and magnitude of the fixed charge in the rear dielectric may have a significant impact on the efficiency of *p*-type Si solar cells. For example, Dauwe *et al.* showed that SiN_x can lead to reduced solar cell efficiency when applied on the rear of *p*-type Si wafer solar cells with local rear contacts [201]. It was explained that this is the case for the PERC solar cell structure, which features a standard ohmic

contact between the metal and the silicon wafer. This is attributed to the presence of an inversion layer induced by the high positive charge density in nearly-stoichiometric SiN_x that allows a current flow ('short circuit') between the inversion layer and the rear metal contacts. This leads to an effect called 'parasitic shunting' and particularly reduces the short-circuit current density J_{sc} [201]. Later it was shown that the use of Si-rich SiN_x reduced the effect of parasitic shunting [116]. Si-rich SiN_x generally has a lower positive charge density compared to nearly-stoichiometric SiN_x films [124]. Consequently, Si-rich SiN_x leads to a poorly conductive inversion layer (or none at all), as shown in Ref. [116]. For Al-LBSF solar cells, however, parasitic shunting is typically not observed as the inversion layer is interrupted by the local back surface field [116, 145, 195-197, 199, 212-214]. However, Schultz *et al.* evaluated the impact of different rear dielectric films on Al-LBSF cells (Al-LBSF cells were prepared by laser-fired contacts) [207, 215]. It was demonstrated that application of a thin thermal SiO_2 beneath the SiN_x improved their cell performance significantly (compared to the cells with SiN_x rear passivation only) showing higher J_{sc} and improved IQE performance at longer wavelengths. Due to increased industrial applicability of Al-LBSF cells, it is important to understand the performance of *p*-type Al-LBSF Si wafer solar cells with different rear surface passivation layers.

In this chapter three low-temperature deposited dielectrics (AlO_x/SiN_x, SiO_x/SiN_x, and SiN_x) are investigated for rear surface passivation of *p*-type Al-LBSF Si wafer solar cells. From one-Sun current-voltage (I-V), external quantum efficiency, reflection measurements and device simulation using PC-1D, the impacts of the rear-surface passivating dielectrics on the performance of the Al-LBSF solar cells are analysed. Furthermore, the polarity and magnitude of the fixed charge in the rear passivating dielectric is correlated to the fill factor loss for Al-LBSF solar cells.

7.2. Fabrication

Large-area (156 mm × 156 mm) pseudo-square monocrystalline *p*-type Cz Si wafers with bulk resistivity ρ of 1.5 Ωcm, thickness W of 160 µm and having (100) surface orientation were used. The wafers were saw damage etched (SDE) in a potassium hydroxide (KOH)/de-ionized (DI) solution removing 10 µm of Si from each side. The wafers received alkaline texturing in a KOH/isopropyl alcohol (IPA)/DI water solution, resulting in a textured surface with upright random pyramids with a size of up to ~6 µm on both sides of the wafer. After a wet-chemical cleaning (RCA) [102], all wafers

underwent an inline phosphorus (n^+) diffusion ('homogeneous emitter') in a commercial in-line furnace (CALiPSO, Meyer Burger, Germany), giving a sheet resistance of 70 Ω/sq on both sides of the wafers. The phosphorus silicate glass (PSG) formed during the diffusion process was removed by wet chemical etching. In the same process the rear n^+ layer was removed ('edge isolation' process) and the rear surface was also smoothened. The wafers were then divided into four groups, each group containing 16 wafers (see Figure 7.1). Three different PECVD dielectric films/ stacks were investigated in this study: Group 1: 25 nm AlO_x film capped with a 70 nm SiN_x film; Group 2: 30 nm SiO_x film capped with a 70 nm SiN_x film; Group 3: single 95 nm SiN_x film. This thickness of each dielectric stack was chosen so that the optical thickness (refractive index, n multiplied by the thickness, d) was similar for all the groups. Some reference Al-BSF cells were fabricated under Group 4. All dielectric films were deposited in a commercial inline microwave-powered remote PECVD reactor (MAiA, Meyer Burger, Germany).

<table>
<tr><th>STEPS</th><th colspan="4">PROCESS DETAILS</th></tr>
<tr><td></td><td>Group 1</td><td>Group 2</td><td>Group 3</td><td>Group 4</td></tr>
<tr><td></td><td colspan="3">Al-LBSF</td><td>Al-BSF</td></tr>
<tr><td>0</td><td colspan="4">p-type Cz Si (100), ρ = 1.5 Ω.cm, W = 160 µm, area = 239.5 cm^2</td></tr>
<tr><td>1</td><td colspan="4">Saw damage etch and random pyramid texturing</td></tr>
<tr><td>2</td><td colspan="4">Cleaning</td></tr>
<tr><td>3</td><td colspan="4">Inline phosphorus diffusion on both sides (70 Ω/sq.)</td></tr>
<tr><td>4</td><td colspan="4">Cleaning (PSG removal and rear side edge isolation & smoothing)</td></tr>
<tr><td rowspan="2">5</td><td colspan="3">Rear Passivation Dielectric</td><td rowspan="3">N.A.</td></tr>
<tr><td>25 nm AlO_x</td><td>30 nm SiO_x</td><td rowspan="2">95 nm SiN_x</td></tr>
<tr><td>6</td><td colspan="2">70 nm capping SiN_x</td></tr>
<tr><td>7</td><td colspan="4">Front ARC SiN_x</td></tr>
<tr><td>8</td><td colspan="4">Rear dielectric ablation</td></tr>
<tr><td>9</td><td colspan="4">Screen-printing of front-side bus bars (Ag)</td></tr>
<tr><td>10</td><td colspan="4">Screen-printing of rear-side full-area (Al)</td></tr>
<tr><td>11</td><td colspan="4">Screen-printing of front-side finger (Ag)</td></tr>
<tr><td>12</td><td colspan="4">Industrial firing at a set-temperature of 880 °C</td></tr>
</table>

Figure 7.1: Fabrication process to study impact of different rear surface passivating layers on p-type Si solar cells.

It is important to mention here that symmetrical test structures were prepared using samples after step 4 that were junction removed and smoothened on both sides – this surface is similar to the rear of the solar cells. These samples were passivated on both sides with AlO_x/SiN_x, SiO_x/SiN_x and SiN_x, representing the rear surface of the solar cells fabricated in this work. This is required to analyse the surface passivation quality with the photoconductance method [24] and interface properties by contactless corona-voltage measurements [48, 49, 51]. Prior to the deposition of the PECVD dielectric films, all samples were RCA (Radio Corporation of America) [102] cleaned with a final HF dip followed by water rinsing and drying, to ensure a H-terminated surface. The deposition conditions and film properties (such as refractive index and thickness) are summarized in Table 7.1. Aluminium full-area back surface field (Al-BSF) cells were also fabricated (see Group 4 in Figure 7.1 with no rear dielectric) as reference. After rear-surface passivating layer or stack depositions, a SiN_x (n = 2.0 and d = 70 nm) was deposited at the front to serve as anti-reflection coating (ARC).

Table 7.1: Inline PECVD deposition parameters and film properties for the PECVD dielectrics used in this work. Heater set temperature (T), reactor pressure (p), plasma power (P), refractive index (n) and thickness (d).

Dielectric	Process gas	T (°C)	p (mbar)	P (W)	n at 633 nm	d (nm)
AlO_x	TMA [$Al(CH_3)_3$] + N_2O + Ar	350	0.10	1500	1.61	25
SiO_x	$SiH_4 + N_2O$	200	0.15	700	1.47	30
SiN_x	$SiH_4 + NH_3$	400	0.20	2200	2.05	90
Capping SiN_x	$SiH_4 + NH_3$	400	0.20	2200	2.03	70

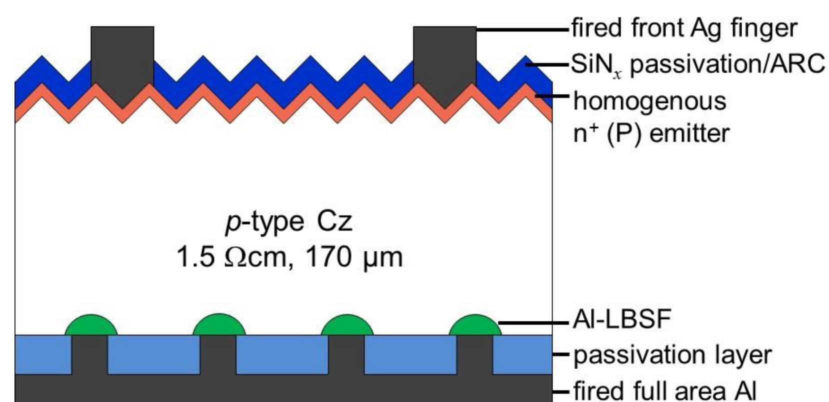

Figure 7.2: Schematic of the Al-LBSF cell fabricated in this work.

For Groups 1, 2 and 3, the rear dielectrics were locally opened by laser ablation. UV lasers were used for dielectric ablation with conditions for example pitch of 1 mm and the size of opening as 50 um (line opening). Finally the metal contacts were formed by industrial screen printing. Three screen-printing steps were performed: First, the front busbars were printed using silver (Ag) paste; second, a full-area rear electrode was printed using aluminium (Al) paste (whereby Al fills the ablated regions in the dielectric); third, the front fingers were printed using Ag paste. Rear busbars were not printed, as the focus in this work was to analyse the impact of the passivation layers at the solar cell level. Finally industrial co-firing was performed to form front and rear contacts, using a peak set temperature of ~ 880 ºC. This firing process firstly ensures good contact formation at the front and rear, secondly, at the rear, it forms a localized BSF (for Al-LBSF cells) or a full-area BSF (for the reference cells in group 4, Al-BSF cells), and thirdly it activates the passivation performance. The cells were fabricated at Roth & Rau AG in Hohenstein, Germany, using surface passivation recipes provided by the present author.

7.3. Results and discussion

The measured one-Sun I-V parameters of the four groups of cells are summarized in Table 7.2. A clear increase in efficiency in the range of 0.7 - 1.3 % absolute for the Al-LBSF structure (with AlO_x/SiN_x or SiO_x/SiN_x as rear dielectrics) is observed compared to the Al-BSF reference cells.

This is mainly because of improvements in the open-circuit voltage (V_{oc}) and, particularly, the short-circuit current density (J_{sc}). The fill factor (FF) of the Al-BSF cells is slightly higher, mainly because of lower series resistance due to full-area metal coverage at the rear. The V_{oc} increase of about 13 mV was observed for the Al-LBSF cells with AlO_x/SiN_x or SiO_x/SiN_x rear dielectric indicating reduced rear surface recombination losses due to the dielectrics. J_{sc} improvement of up to 1-2 mA/cm^2 was obtained for the same Al-LBSF cells compared to the Al-BSF counterparts, indicating increased rear internal reflection in combination with reduced recombination losses due to the rear dielectrics. The focus of this work was on the investigation of rear surface passivation schemes for large-area *p*-type Al local back surface field solar cells – hence, additional investigations and analysis will only be provided for Groups 1, 2 and 3.

Table 7.2: One-sun I-V parameters measured under standard testing conditions (25 °C cell temperature, 100 mW/cm^2, AM 1.5 G) for the Al-LBSF silicon solar cells with three different rear passivating dielectrics (AlO_x/SiN_x, SiO_x/SiN_x and SiN_x). For comparison, results of standard Al-BSF cells are also included. Average values with standard deviation of 16 cells processed under each batch is also mentioned.

	Group 1 AlO_x/SiN_x		Group 2 SiO_x/SiN_x		Group 3 SiN_x		Group 4 Al-BSF	
	Best	Ave.	Best	Ave.	Best	Ave.	Best	Ave.
V_{oc} (mV)	648.9	647.7 ± 0.86	648.7	647 ± 1.08	641.1	638.6 ± 1.95	634.6	634.4 ± 0.58
J_{sc} (mA/cm^2)	38.1	37.8 ± 0.11	37.5	37.2 ± 0.22	37.0	36.5 ± 0.31	36.2	36.0 ± 0.05
R_s (Ω -cm^2)	0.72	0.67 ± 0.03	0.64	0.59 ± 0.03	0.65	0.57 ± 0.04	0.57	0.56 ± 0.02
R_{sh} (kΩ-cm^2)	40.28	39.75 ± 1.31	65.37	46.44 ± 0.66	41.74	39.35 ± 0.35	77.55	65.88 ± 12.24
FF (%)	78.9	79.1 ± 0.24	78.5	78.1 ± 0.41	77.3	77.7 ± 0.22	79.2	79.3 ± 0.12
*Eff** (%)	19.5	19.4 ± 0.09	19.1	18.8 ± 0.17	18.4	18.2 ± 0.17	18.2	18.1 ± 0.04

*As-fabricated efficiency.

In order to illustrate a clear trend, Figure 7.3 shows the box plots of the one-Sun current-voltage (I-V) measurement results for the Al-LBSF cells with different rear dielectrics. Among the three groups fabricated in this experiment, Al-LBSF cells with AlO_x/SiN_x rear dielectric passivation resulted in the highest conversion efficiency of 19.5 %. This is followed by cells with SiO_x/SiN_x rear dielectric passivation (19.1 %) and then cells with SiN_x rear dielectric passivation (18.4 %), as shown in Figure 7.3(d). [Remark: In a separate experiment, efficiencies of up to 20.1 % were obtained for Al-LBSF Si wafer solar cells with an AlO_x/SiN_x rear surface passivation. The results are not shown/explained in this chapter, as they requires further characterisation.]

The one-Sun V_{oc} appears to be similar for both AlO_x/SiN_x and SiO_x/SiN_x and lower for SiN_x group (Figure 7.3(a)). Cell V_{oc} is indicative of recombination at the surfaces and in the bulk of the Si at the measured light intensity (one-Sun in this case). It should be noted that all three dielectrics showed very good surface passivation results and similar

injection level dependence on the undiffused p-Cz wafers used in this work. The results are published elsewhere, see Refs. [216, 217]. Contactless corona-voltage measurement reveals high negative Q_{total} of 2×10^{12} cm^{-2} for AlO_x/SiN_x and positive Q_{total} of 7×10^{11} cm^{-2} and 4×10^{12} cm^{-2} for SiO_x/SiN_x and SiN_x, respectively, as measured in this work. However, the difference lies in mid-gap interface defect density $D_{it,midgap}$. For the AlO_x/SiN_x and SiO_x/SiN_x stacks $D_{it,midgap}$ is similar (in the range of 10^{11} eV^{-1}cm^{-2}), while the SiN_x exhibits a higher interface defect density with $D_{it,midgap}$ values of ~8×10^{11} eV^{-1}cm^{-2}, which is related to the differences in surface passivation among these dielectrics in this case. If in the finished solar cells the surface recombination at the rear is ruled by $D_{it,midgap}$, then the difference in surface passivation results among these dielectrics can be partially correlated to the differences in the cells' V_{oc}.

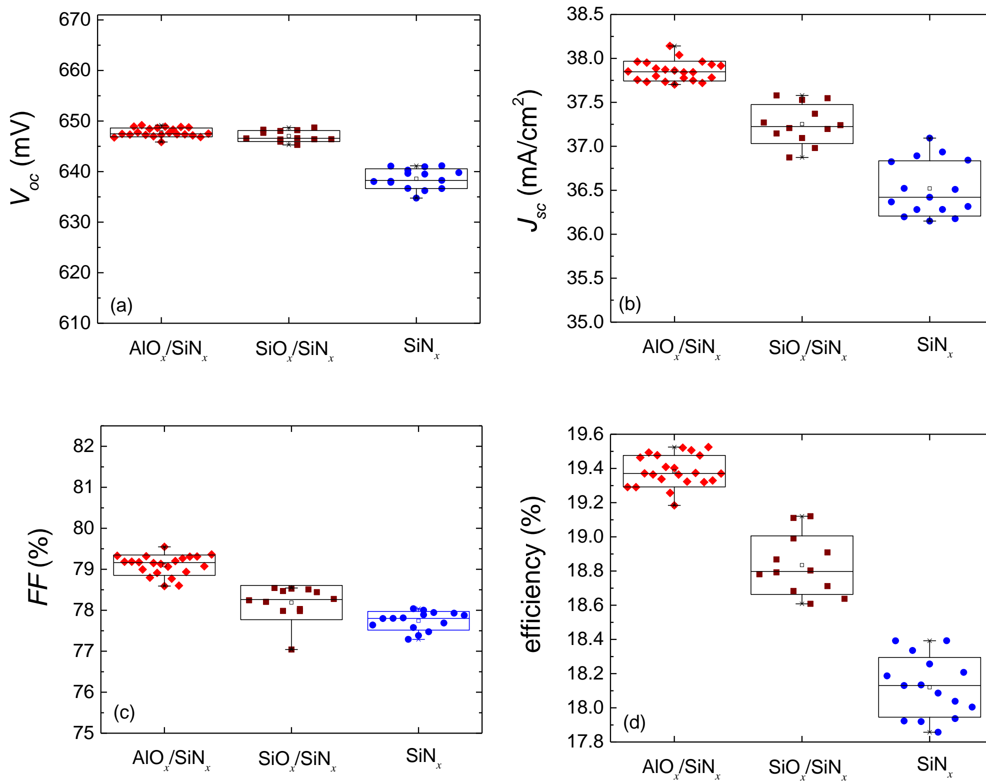

Figure 7.3: Box plots of the one-Sun I-V parameters (V_{oc}, J_{sc}, FF, Eff) measured under standard testing conditions (25 °C, 100 mW/cm^2, AM 1.5 G) for the Al-LBSF silicon solar cells with three different rear passivating dielectrics. For the ease of comparison of the four graphs, the Y-axis of each graph was scaled such that the top value of each Y-axis is about 10% larger than its bottom value.

In order to better understand the differences in the solar cell performances, the external quantum efficiencies (EQE) and reflectances (R) were measured. Furthermore, the

internal quantum efficiencies (IQE) were extracted from these measurements. The EQE measurements were performed under a bias light intensity of 0.3 suns ('differential' spectral response). Figure 7.4 shows the measured differential EQE and the measured R for the champion solar cell from each of the three groups, along with the corresponding IQEs. Interestingly, the quantum efficiencies of the 3 types of cells clearly differ at longer wavelengths (> 750 nm), where the carrier collection efficiency is sensitive to the passivation quality of the rear surface. In the 1000-1200 nm range where the penetration depth exceeds the wafer thickness, the IQE is also affected by the degree of parasitic absorption and reflection of light reaching the rear surface. In order to understand the large differences, firstly J_{sc} was calculated from the measured EQE data, using the following equation:

$$J_{sc} = q \int_{\lambda=300}^{\lambda=1200} \phi_{AM1.5G}(\lambda) * EQE\ (\lambda)\ d\lambda \qquad (7.1)$$

where $\phi_{AM1.5G}(\lambda)$ is the photon flux of the AM 1.5G solar spectrum. The J_{sc} values extracted from EQE measured at 0.3 suns (using Eq. 7.1) and values from Table 7.2 are summarised in Table 7.3.

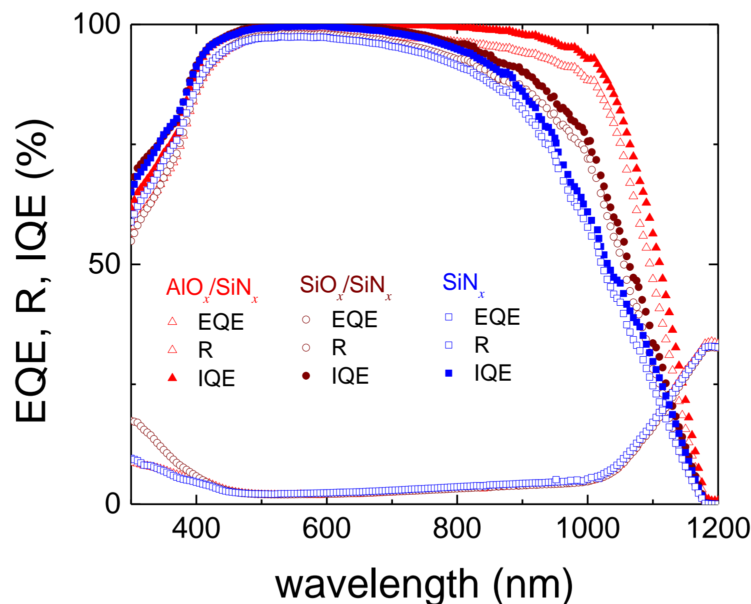

Figure 7.4: Measured external quantum efficiency (EQE), measured reflectance (R), and calculated internal quantum efficiency (IQE) in the 300 - 1200 nm wavelength range of Al-LBSF cells with three different rear-passivating dielectrics (AlO_x/SiN_x, SiO_x/SiN_x and SiN_x). The EQE measurements used a bias light intensity of 0.3 suns.

Table 7.3: Summary of J_{sc} values from one-sun I-V measurements and EQE measurements at 0.3 suns.

Rear dielectric scheme	J_{sc} values measured at 1 Sun (mA/cm^2)	J_{sc} values extracted from EQE (mA/cm^2)	Difference (mA/cm^2)	Cell behaviour
AlO_x/SiN_x	38.1	38.09	--	Linear
SiO_x/SiN_x	37.5	36.02	1.5	Non-linear
SiN_x	37.0	34.60	2.4	Non-linear

The analysis (results shown in Table 7.3) shows large differences in J_{sc} extracted under 1 Sun and 0.3 Suns for Al-LBSF cells having SiO_x/SiN_x (difference of 1.5 mA/cm^2) and SiN_x (difference of 2.5 mA/cm^2) as rear surface passivation schemes, whereas almost no difference was observed for the Al-LBSF cells with AlO_x/SiN_x rear passivation. This indicates that a severe non-linearity is present in the Al-LBSF cells having a SiO_x/SiN_x and, particularly, a SiN_x rear surface passivation.

A detailed analysis of the IQE at longer wavelengths gives information on the electronic and optical quality of the rear surface [19, 218]. The following analysis was performed for the Al-LBSF cells fabricated with an AlO_x/SiN_x rear passivation as it shows linear spectral response where the characterisation results can be accurate unlike the cell having non-linear behaviour.

Evaluation of near-infrared region (750 - 950 nm):

Photons with a wavelength in the 750 - 950 nm range do not penetrate deep enough into the *c*-Si wafer to reach its rear surface. The IQE in this wavelength region is thus not affected by the optical properties of the rear surface, enabling a relatively straightforward determination of the effective diffusion length (L_{eff}) and the collection efficiency of the solar cell [218]. As proposed by Basore *et al.,* the IQE in this wavelength range can be written as [218]:

$$\frac{1}{IQE\ (\lambda)} = 1 + \frac{\cos\theta_1}{\alpha\ (\lambda) L_{eff}} \quad \text{(7.2)}$$

where θ_1= 41.8° is the angle of refraction (in the case of a front surface textured with upright pyramids), and $\alpha(\lambda)$ is the wavelength dependent absorption coefficient of c-Si.

Equation 7.2 was used to fit the measured IQE spectra shown in Fig. 7.5 in order to determine L_{eff}. From L_{eff}, the base and cell rear component of dark saturation current density (J_{0b}) and the average collection efficiency (η_c) can be extracted using the following equations [218]:

$$J_{0b} = \frac{qD_n n_i^2}{N_A L_{eff}} \quad \text{(7.3)}$$

$$\eta_c = \frac{L_{eff}}{W}\left(1 - e^{-\frac{W}{L_{eff}}}\right) \quad \text{(7.4)}$$

where q is the elementary charge (1.602×10^{-19} cm^{-2}), D_n the minority carrier diffusion coefficient (~ 30 cm^2/s for a 1.5 Ohm.cm p-type Si), n_i the intrinsic carrier concentration (8.6×10^9 cm^{-3} [219]), and N_A the bulk acceptor concentration (9.7×10^{15} cm^{-3} in this work). The extracted L_{eff}, J_{0b}, η_c values are summarized in Table 7.4.

L_{eff} is influenced by recombination in the bulk and at the rear surface, which in this case consists of dielectrically passivated regions and localized rear metal contacts. Such high L_{eff} (1800 µm) and η_c (94%) indicate a good electronic quality of the bulk and the rear surface, as well as a high optical quality of the rear surface. With a short-circuit current density of 38.1 mA/cm^2 (measured, see Table 7.2) and using the ideal one-diode model, it can be calculated that the J_{0b} of 200 fA/cm^2 (from Eq. 7.3, see Table 7.4) limits the one-Sun open-circuit voltage ($V_{oc,limit}$) to 671 mV at 300 K. This is considered a high value for an industrial large-area solar cell fabricated on a p-type Cz substrate. Further reduction in recombination at the dielectrically passivated regions, beneath the localised metal contacts and in the bulk Si will further improve $V_{oc,limit}$ and hence the cell efficiency.

Table 7.4: Parameters extracted from the measured IQE describing the recombination in the base and at the rear surface of the Al-LBSF cells fabricated with AlO_x/SiN_x rear surface passivation.

Rear dielectric scheme	L_{eff} (µm)	J_{0b} (fA/cm^2)	η_c (%)
AlO_x/SiN_x	1800 ± 100	200 ± 30	94 ± 2

Evaluation of near-bandgap region (1000 - 1200 nm):

Photons with wavelengths longer than 1000 nm are weakly absorbed in *c*-Si wafers and thus some of them will reach the wafer's rear surface. The IQE in this wavelength range can be expressed as [218]:

$$IQE\ (\lambda) = \eta_c \frac{A}{1-R} \quad (7.5)$$

where η_c is the average collection efficiency as defined in Eq. 7.4, A is the absorption in the silicon wafer, and R_b is the cell's rear internal reflectance, where one can insert the value of η_c estimated from the analysis of the 750-950 nm range into Eq. 7.5 to obtain A. IQE can be simulated in PC1D [66, 218] by selecting right combination of bulk diffusion length L_{bulk}, rear surface recombination velocity S_{rear} and rear internal reflectance R_b to the experimentally measured data. The individual components of L_{eff} i.e. L_{bulk} and S_{rear} was attempted to resolve from the IQE data using PC1D fitting, by carefully looking at the 750 - 950 nm range. The simulated IQE was found to be in good agreement with the measured IQE, as shown in Figure 7.5, and the extracted values of L_{bulk}, S_{rear} and R_b are summarised in Table 7.5. It should be noted that the accuracy in determining a unique combination of L_{bulk} and S_{rear} merely from IQE data is limited [218]. Assuming L_{bulk} to be 1000 μm PC1D fit resulted in S_{rear} of 100 cm/s and R_b of 90 %, which is similar to the values achieved in Ref. [99].

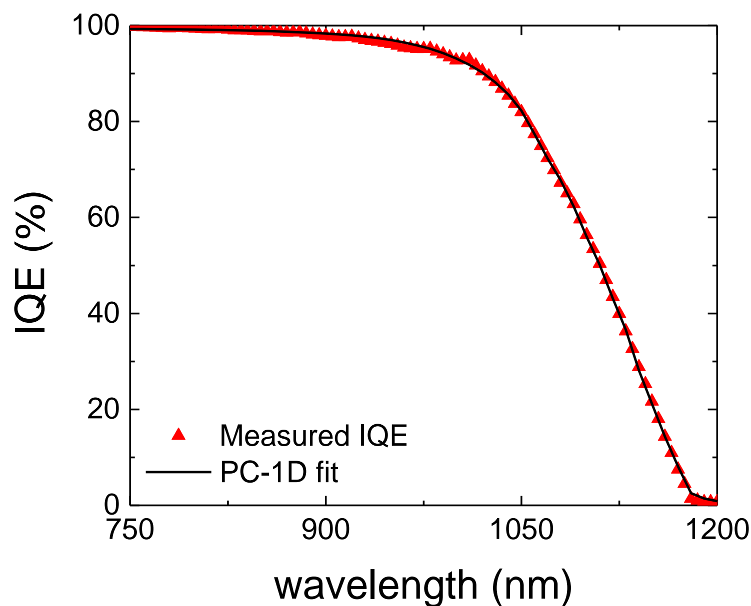

Figure 7.5: Measured IQE (symbols) and PC1D simulated IQE (line) in the 750 - 1200 nm wavelength range of Al-LBSF cells with AlO_x/SiN_x as rear surface passivation.

Table 7.5: Rear surface recombination velocity S_{rear} and rear internal reflectance R_b calculated using PC1D fitting.

Rear dielectric scheme	L_{bulk} (µm)	S_{rear} (cm/s)	R_b (%)
AlO_x/SiN_x	1000	100 ± 20	90 ± 2

Even at one-Sun conditions, large differences in J_{sc} were observed (see Table 7.2). Due to a lack of time, the reasons for this behaviour could not be investigated in detail. Schultz *et al.* [207, 215] also showed that Al-LBSF cells (LBSF from laser fired contacts) with SiN_x (having high positive charge in the range of 10^{12} cm^{-2})* as rear passivation had reduced J_{sc} compared to cells with thin thermal SiO_2/SiN_x (having low positive charge in the range of 10^{11} cm^{-2})* as rear passivation. The observed J_{sc} effect was ascribed to parasitic shunting. On the other hand, in a recent study by Dullweber *et al.* on screen-printed Al-LBSF cells, AlO_x/SiN_x (having high negative charge in the range of 10^{12} cm^{-2})* and thin thermal SiO_2/SiN_x (having low positive charge in the range of 10^{11} cm^{-2})* did not show any difference in J_{sc}. This confirms that Al-LBSF cells having a rear dielectric with a small positive fixed charge or a negative fixed charge can both result in very good cell efficiency.

It should be noted that it was suggested via 2D simulations that a higher positive insulator charge in combination with a local back surface field (instead of a standard ohmic contact) can improve the cell J_{sc} and consequently the cell efficiency [199, 213, 214]. Unfortunately, this was not observed neither in the work of Schultz *et al.* nor in the present work for Al-LBSF cells passivated with SiN_x (having high positive charge of > 10^{12} cm^{-2}). It is important to mention that - due to the industrial screen-printed Al-alloyed LBSF used in this work - there is always a possibility of voids or imperfect LBSF formation [220, 221], which can give a short-circuit current path leading to parasitic shunting [116, 201]. Considering the data available in the literature and from the present work, understanding the impact of charge in the rear dielectric on the IQE behaviour and J_{sc} of Al-LBSF cells is not yet totally clear. More experimental work, along with multidimensional modelling, is needed to further investigate the impact of the polarity and the magnitude of the fixed charge density on Al-LBSF cells.

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* Value estimated by the present author (no value was mentioned in the publications).

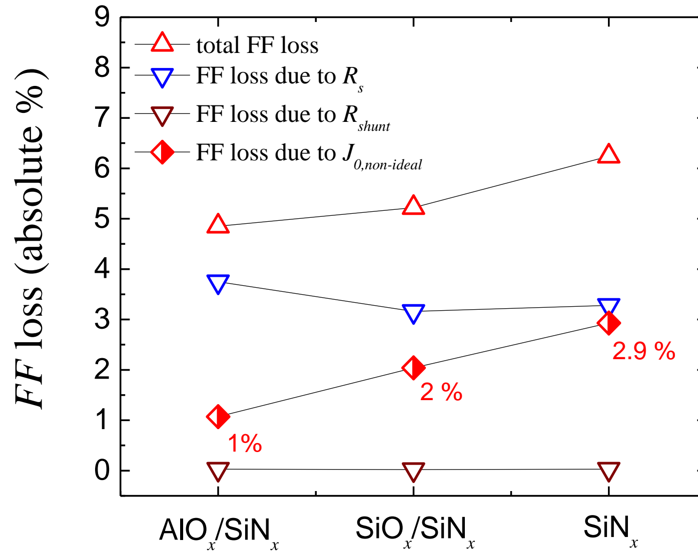

Figure 7.6: Fill factor (*FF*) loss analysis for Al-LBSF cells with three different rear-passivating dielectrics (AlO_x/SiN_x, SiO_x/SiN_x, SiN_x).

Significant differences in the fill factor (FF) of the Al-LBSF cells were observed for different rear-passivating dielectrics (AlO_x/SiN_x, SiO_x/SiN_x and SiN_x), see Table 7.2. A FF loss analysis was performed for these cells using the method described in Ref. [222]. The method is based on the two-diode model of solar cells [223] and attributes losses in FF due to ohmic resistances (series resistance R_s and shunt resistance R_{shunt}) and recombination processes with ideality factors not equal to one, which are referred to as 'non-ideal recombination' ($J_{0,non\text{-}ideal}$) in this work. The FF loss analysis results for the best cell in each group are shown in Figure 7.6. A striking correlation between the FF loss and the $J_{0,non\text{-}ideal}$ of the Al-LBSF cells passivated with different rear-passivating dielectrics was observed. The *FF* loss due to $J_{0,non\text{-}ideal}$ is 1.1, 2.0 and 2.9 % absolute for the Al-LBSF solar cells with a AlO_x/SiN_x, SiO_x/SiN_x and SiN_x rear surface passivation, respectively, see Figure 7.6.

As the cell processing was identical apart from the rear surface dielectrics, the differences in the FF loss due to $J_{0,non\text{-}ideal}$ can be attributed to the different rear surfaces. AlO_x/SiN_x with its negative fixed charge density generates accumulation conditions at the rear Si surface. On the other hand, SiO_x/SiN_x and SiN_x have low and high positive fixed charge density, respectively, which depletes or even inverts the rear surface. The

inverted condition can result in additional bulk recombination, due to the formation of a space charge region beneath the Si surface (more explanations in Ref. [46, 60, 61, 65]). This space charge region may well be the source of $J_{0,non\text{-}ideal}$. As evident from Figure 7.6, this effect is more pronounced for the dielectric with the higher positive charge density (SiN_x), leading to a higher FF loss due to $J_{0,non\text{-}ideal}$. Additionally, as mentioned by Aberle *et al.* [19, 210], if an injection level dependent recombination mechanism is present in a solar cell, then the FF loss due to $J_{0,non\text{-}ideal}$ determined by the FF loss analysis include the influence of this injection level dependence (or 'non-linearity' of the cell). Thus, a detailed loss analysis of the Al-LBSF cells fabricated in this work needs to take their non-linearity into account.

7.4. Conclusions

Three different rear surface passivation schemes such as AlO_x/SiN_x, SiO_x/SiN_x and SiN_x were investigated in this chapter for application on large-area (239.5 cm^2) *p*-type Si Al local back surface field (Al-LBSF) silicon wafer solar cells. The Al-LBSF solar cells were fabricated and analysed by one-Sun current-voltage (I-V), external quantum efficiency and reflection measurements in combination with PC1D device simulations. A champion solar cell efficiency of 20.1% was obtained for Al-LBSF solar cells with an AlO_x/SiN_x rear surface passivation, while the solar cells with SiO_x/SiN_x and SiN_x rear surface passivation showed lower efficiencies. The analysis revealed a severe non-linearity in the Al-LBSF cells fabricated with SiO_x/SiN_x and SiN_x as rear surface passivation, which was not the case for Al-LBSF cells fabricated with AlO_x/SiN_x rear passivation. Despite the fact that these dielectrics showed a very similar level of surface passivation on dedicated lifetime samples, significant differences in the quantum efficiency and short-circuit current density were observed. It was hypothesized that this difference originates either from the non-linearity of the cells or/and from differences in polarity and amount of fixed charge density in the rear surface passivating dielectric. Analysis with PC1D estimated that Al-LBSF cells with an AlO_x/SiN_x rear surface passivation have very low rear surface recombination velocity of 100 cm/s and high rear internal reflection of 90 %. A detailed analysis revealed that the fill factor of Al-LBSF solar cells with a positively charged dielectric is strongly reduced due to a significant increase in non-ideal recombination. This non-ideal recombination is found to increase for higher positive charge densities and could be due to additional recombination in the space charge region beneath the Si surface.

Chapter 8: Summary and Future work

This PhD thesis reports several important advancements with industrially feasible surface passivation methods on both moderately and heavily doped *c*-Si using positively and negatively charged dielectrics for application in crystalline silicon solar cells (updated results in Table 8.1). This PhD thesis has been divided broadly into four sections. In the following, the original contributions and possible future work for the respective sections are summarised.

8.1. Low-temperature plasma-deposited silicon nitride (SiN_x)

In **Chapters 3**, outstanding surface passivation results were obtained using *dynamically* deposited plasma SiN_x with surface recombination velocities $S_{eff,max}$ of 2 and 5 cm/s on *n* and *p* type *c*-Si. For a phosphorus diffused emitter (n^+ *c*-Si), an exceptionally low emitter saturation current density J_{0e} of 15 fA/cm^2 was reported. Such high-quality passivation was previously only achievable with static depositions (using lab-type reactors) or by non-industrial annealing, whereas this work used a commercially available inline reactor and standard industrial firing. The surface passivation mechanism was explained to be due to an increased fixed charge density in the *dynamically* deposited plasma SiN_x films developed in this work. Because dynamically deposited plasma SiN_x is one of the mainstream technologies in today's *c*-Si PV industry, this progress could have significant impact on the PV industry as this enables solar cell efficiency improvements of more than 0.2% absolute with no additional processing cost.

Although SiN_x is an extensively researched material, it is recommended for future work to continue to investigate especially the origin of positive charge in the interface and the microscopic location of charge in the dielectric. This is particularly important for further improvements of the surface passivation quality. The presence of a nanoscale interfacial layer between Si and SiN_x has to be studied in detail, as it will have an impact on the electronic properties of plasma SiN_x. There has been some speculation in the literature on the presence of plasma damage in PECVD SiN_x – further studies will enable to understand this properly. In addition, it is imperative to investigate and establish methods for altering the fixed charge in SiN_x, as this could have a big impact on crystalline silicon solar cells.

8.2. Low-temperature plasma-deposited and chemically-grown silicon oxide (SiO_x) and stacks

High-quality SiN_x (as developed in Chapters 3 and 4) did not provide good surface passivation of p^+ type *c*-Si when applied directly on H-terminated *c*-Si surfaces. The primary reason is the high positive fixed charge in SiN_x. It was experimentally shown and fundamentally understood that a good surface passivation of p^+ type *c*-Si requires a reduced fixed positive charge density (in combination with a low interface defect density). In **Chapters 4**, it was shown that inserting a thin PECVD SiO_x (10-30 nm) between the *c*-Si and the SiN_x reduced positive fixed charge density significantly (by almost one order of magnitude) with a drastic reduction of the interface defect density (measured to be as low as 3×10^{10} $eV^{-1}cm^{-2}$). This stack layer yields low $S_{eff,max}$ of 7 and 8 cm/s on *n* and *p* type *c*-Si, respectively, and shows remarkably low J_{0e} of 8 fA/cm^2 on n^+ *c*-Si surfaces and 15 fA/cm^2 on p^+ *c*-Si surfaces. Further research was carried out in this thesis to see if this thin PECVD deposited SiO_x film can be replaced by a chemically grown SiO_x layer resulting in similar surface passivation results, which can be considered as an even more cost-effective process (as it does not involve any hazardous gases). Furthermore, it was shown that a 0.6 nm thick chemically-grown ultrathin SiO_x layer between *c*-Si and SiN_x is sufficient to reduce both the fixed charge density and the interface defect density sufficiently to obtain excellent surface passivation of p^+ *c*-Si (25 fA/cm^2), which is a pre-requisite for well performing *n*-type solar cells. This work again used industrial firing for passivation activation. These results are comparable to the best results reported in the literature using other dielectrics. The work on PECVD and chemical SiO_x can be considered a major progress in the area of dielectric passivation of c-Si surfaces, as this dielectric stack was demonstrated in this thesis to passivate *all* c-Si surfaces (*n* and *p* type) with arbitrary surface doping concentration. In addition, this technology provides a cost-effective and environmentally friendly passivation solution that can be attractive for both academia and industry.

It is recommended for future work to especially investigate the UV stability of the passivation, and then to demonstrate higher solar cell efficiency with the developed SiO_x/SiN_x stacks. More research is required to explain the reason for the reduced positive charge and density of interface states by using the stack layer.

8.3. Low-temperature plasma-deposited aluminium oxide (AlO_x) and stacks

In order to further reduce surface recombination at p^+ *c*-Si surfaces and allow a better process, the use of high negatively charged films was shown to be beneficial, whereby both field-effect and chemical passivation can be utilised. In this thesis, significantly improved surface passivation results using *dynamically* deposited plasma AlO_x (with or without a SiN_x or SiO_x capping layer) were demonstrated with ultra-low $S_{eff,max}$ of 1 and 8 cm/s on *n* and *p* type *c*-Si, respectively, after industrial firing. In **Chapter 5**, AlO_x was demonstrated to provide exceptional surface passivation of both phosphorus emitters (n^+ *c*-Si) and boron emitters (p^+ *c*-Si), with J_{0e} of 15 and 9 fA/cm^2, respectively, for a large range of sheet resistances. This is an important progress in surface passivation in regards to the AlO_x technology, as this has specific significance for devices that need a single dielectric film for passivating both n^+ and p^+ *c*-Si surfaces, for example interdigitated back contact (IBC) solar cells.

In the future, improved efficiencies of IBC solar cells can be expected with this low-temperature passivation scheme. It is recommended that more research is carried out to investigate the origin of the negative charge, and its exact location in the film. Further studies should also elucidate the role of the interfacial 'SiO_x' layer for the enhancement of the negative charge and the reduction of density of interface states after annealing. This will continue to improve the fundamental knowledge regarding this dielectric film on c-Si. For PV application, as mentioned in this thesis, it is important to further investigate the 'tailoring/engineering' of interface properties, with the aim to improve the device performance.

8.4. Towards efficiency enhancement of *c*-Si solar cells

The polarity and amount of fixed charge has a profound impact on the surface recombination velocity and the solar cell's operation. Charge tailoring (both in terms of polarity and amount) within a dielectric without changing important film properties (e.g., composition, refractive index, thickness) can be an interesting path towards improved Si solar cell performance. From a fundamental and technological point of view, it is important to delve into this topic of research. In **Chapter 6**, the fixed charge within a dielectric was experimentally varied, in a controlled way, by up to one order of magnitude (10^{11} - 10^{12} elementary charges/cm^2), without any impact on the density of interface states at midgap level ($D_{it,midgap}$). Experimentally it was shown that, for inversion conditions, S_{eff} scales with $1/Q^2$, which previously was investigated only by

simulations or external corona charging. It should be shown in future work that, if the $D_{it,midgap}$ (or 'chemical passivation') is retained constant in the finished *p*-type solar cells, then charge tailoring can be an effective tool for improving the solar cell efficiency, especially for 'aluminium local back surface field' (Al-LBSF), 'passivated emitter rear locally diffused' (PERL) and 'passivated emitter rear contacted' (PERC) solar cells. In an initial study, large-area Al-LBSF cells were investigated with different rear surface passivating films, as shown in **Chapter 7**. All three dielectric films (SiN_x, SiO_x/SiN_x, AlO_x/SiN_x) developed in this thesis were applied on the rear surface of full-area (239.5 cm^2) *p*-type Si Al-LBSF solar cells and their performance was investigated using spectral response and one-Sun I-V measurements. Screen-printed Al-LBSF solar cells with AlO_x/SiN_x rear surface passivation had the best PV efficiency of up to 20.1%. Detailed analysis revealed, for example, that the fill factor of Al-LBSF solar cells with a high positively charged dielectric is strongly reduced due to a significant increase in non-ideal recombination. This non-ideal recombination was found to increase for higher positive charge densities and could be due to additional recombination in the space charge region beneath the Si surface.

As a future work, development of a rigorous model for 'charge tailoring in dielectrics' should be established, to advance the understanding of this important topic in the PV community. With advanced 2D computer modelling and advanced characterisation methods, it should be possible to identify the origin of the reduced (or improved) short-circuit current density and fill factor of Al-LBSF cells.

Table 8.1: Surface passivation and electronic properties of commonly used multifunctional thin films summarised in Table 2.1 with the results obtained in this PhD thesis.

Films			Surface passivation results				Electronic interface properties	
			n-type *c*-Si[1]	n^+-type *c*-Si[2]	*p*-type *c*-Si[1]	p^+-type *c*-Si[2]	$D_{it,midgap}$	Q_f
			$S_{eff,max}$	J_{0e}	$S_{eff,max}$	J_{0e}		
			[cm/s]	[fA/cm^2]	[cm/s]	[fA/cm^2]	[$\times 10^{11}$ eV^{-1}cm^{-2}]	[$\times 10^{11}$ cm^{-2}]
positively charged films	Thermal SiO_2	static	2.4 [75, 76]	~10 [75, 76]	11.8 [77]	20 [44]	0.01-1 [17, 19, 56, 67]	0.1-1 [19]
	PECVD SiO_x[3]	static	2 [78, 79]	210 [80]	11 [81]	NA	0.1-1 [82, 83]	5-10 [78]
		dynamic	7	8	8	15	0.3-2	~0.8-10
	PECVD SiN_x	static	3.4 [84]	20 [75]	6.7 [85]	23 [84, 86]	~3-50 [19]	~1-70 [19, 70, 71]
		dynamic	30 [87]	60 [88, 89]	11.8 [90]	NA	NA	NA
			2	15	5	25	5-9	40-80
negatively charged films	ALD Al_2O_3	static	0.33 [91]	60 [92]	2.35 [91]	10 [74]	1 [73]	−(40-100) [73, 93, 94]
	PECVD AlO_x[3]	dynamic	NA	NA	10 [95]	8 [96]	0.1-10 [97]	−(10-40) [97]
			1.6	12	8	9	1	−(10-70)

NA stands for 'Not available'. [1]Results are shown for *c*-Si wafers resistivity between 1 to 5 Ωcm that are useful for solar cell fabrication. [2]It should be carefully noted that J_{0e} is partly dependent on the Auger recombination, which will vary with the doping profile and processing conditions done at different laboratories. In addition results with emitters having highest sheet resistance reported for each work is mentioned in this table. [3]Results may have been reported without or with a SiN_x capping layer.

Appendices

Appendix I: List of Publications arising from this PhD research

PCT patent applications

1. **S. Duttagupta**, B. Hoex, M. B. Boreland, "A System and Method of Depositing a Layer on a Substrate", patent application PCT/SG2012/000310
2. **S. Duttagupta**, B. Hoex, M. B. Boreland, J. Wong, T. Mueller, "A Method of Manufacturing a Photovoltaic Cell", patent application PCT/SG2013/000527
3. F. Zheng, J. Wong, M. B. Boreland, B. Hoex, A. Karpour, A. G. Aberle, **S. Duttagupta**, T. Mueller, "Method of Fabricating a Solar Cell", patent application PCT (ID6 – NUS ILO Ref 12316N)

Published journal papers

1. **S. Duttagupta**, F. Lin, K. Devappa Shetty, A. G. Aberle and B. Hoex, Excellent boron emitter passivation for high-efficiency Si wafer solar cells using AlO_x/SiN_x dielectric stacks deposited in an industrial inline plasma reactor, *Progress in Photovoltaics: Research and Applications*, 21, 760-764, 2013.
2. F. Lin, **S. Duttagupta**, K. Devappa Shetty, M. Boreland, A. G. Aberle and B. Hoex, Excellent passivation of p^+ silicon surfaces by inline PECVD SiO_x/AlO_x stacks, *Japanese Journal of Applied Physics*, 51:10NA17, 2012.
3. **S. Duttagupta**, L. Fen, M. Wilson, B. Hoex, A.G. Aberle, Extremely low surface recombination velocities on low-resistivity *n*-type and *p*-type crystalline silicon using dynamically deposited remote plasma silicon nitride films, *Progress in Photovoltaics: Research and Applications*, 22, 641-647, 2014.
4. **S. Duttagupta**, F. Lin, T. Mueller, A. G. Aberle and B. Hoex, Progress in passivation of heavily *n*-type and *p*-type doped silicon surfaces by plasma-deposited AlO_x/SiN_x dielectric stacks, *IEEE Journal of Photovoltaics*, 3, 1163-1169, 2013.
5. **S. Duttagupta**, Fa-Jun Ma, B. Hoex and A. G. Aberle, Excellent surface passivation of heavily doped p^+ silicon by low-temperature plasma-deposited SiO_x/SiN_y dielectric stacks with optimised antireflective performance for solar cell application, *Solar Energy Materials and Solar Cells*, 120, pp. 204-208, 2014.

In preparation for journal submission

6. **S. Duttagupta**, B. Hoex, and A.G. Aberle, "Progress in surface passivation of heavily-doped crystalline silicon using PECVD silicon nitride" In preparation for submission to a Journal (partly mentioned in Chapter 3 of the thesis).
7. **S. Duttagupta**, Z. Hameiri, B. Hoex, and A.G. Aberle, "Dielectric charge tailoring in PECVD SiO_x/SiN_x stacks and its impact on industrial *p*-type silicon wafer solar cell efficiency," Submitted to IEEE Journal of Photovoltaics **(Invited)**, 2014. (Presented in Chapter 6 of the thesis).
8. **S. Duttagupta**, B. Hoex, and A.G. Aberle, "On the mechanism of surface passivation of heavily doped *p*-type Si using PECVD SiN_x deposited on ultrathin SiO_x" In preparation for submission to a Journal (partly mentioned in Chapter 4 of the thesis).
9. **S. Duttagupta**, J. Wong, B. Hoex, and A.G. Aberle, "Impact of rear surface passivation schemes on the performance of large-area *p*-type silicon Aluminium-local back surface field solar cells" In preparation for submission to a Journal (partly mentioned in Chapter 7 of the thesis).
10. **S. Duttagupta**, R. A. Stangl, B. Hoex, A.G. Aberle and T. Mueller, "Application of charged dielectrics for industrial locally-contacted high-efficiency Si wafer solar cells" In preparation for submission to a Journal.
11. **S. Duttagupta**, Z. Hameiri, B. Hoex, and A.G. Aberle, "Analysis of surface recombination at the Si-SiN_x and Si-AlO_x interface" In preparation for submission to a Journal.

Conference papers

1. **S. Duttagupta**, B. Hoex, F. Lin, T. Mueller and A. G. Aberle, High-quality surface passivation of low-resistivity *p*-type *c*-Si by hydrogenated amorphous silicon nitride deposited by industrial-scale microwave PECVD, Proc. of 37th IEEE Photovoltaic Specialists Conference, Seattle, p. 001421 – 001423 (2011). ***Best Poster Award*** in the conference area "Crystalline Silicon: Cell Structures and Processes".
2. F. Lin, B. Hoex, **S. Duttagupta**, and A. G. Aberle, Excellent passivation of p^+ silicon surfaces by inline PECVD SiO_x/AlO_x stacks, Technical Digest of the 21st International Photovoltaic Science and Engineering Conference, paper 4D-1P-16, Fukuoka, Japan, (2011).

3. **S. Duttagupta**, F. Ma, B. Hoex, T. Mueller, and A. G. Aberle, Optimised anti-reflection coatings using silicon nitride on textured silicon surfaces based on measurements and multidimensional modelling, Proc. of International Conference on Materials for Advanced Technologies 2011 (ICMAT 2011), Symposium O, Singapore (2011); Energy Procedia 15, p. 78-83 (2012). ***Best Poster Award.***
4. Prabir K. Basu, Kishan Devappa Shetty, Shanmugam Vinodh, Debajyoti Sarangi, Natalia Palina, **Shubham Duttagupta**, Fen Lin, Zheren Du, Jia Chen, Bram Hoex, Matthew B. Boreland and Armin G. Aberle "19% efficient inline-diffused large-area screen-printed Al-LBSF silicon wafer solar cells", Proc. of 2nd International Conference on Silicon Crystalline Photovoltaics, Energy Procedia 27, pp. 444-448 (2012).
5. **S. Duttagupta**, F. Lin, K.D. Shetty, M. Wilson, F.M. Ma, J. Lin, A.G. Aberle, B. Hoex, "State-of-the-art Surface Passivation of Boron Emitters on *n*-Type c-Si using Inline PECVD AlO_x/SiN_x Stacks for Industrial High-Efficiency Solar Cells", Proc. of 38th IEEE PV Specialists Conference (PVSC), Austin, Texas, USA, 3-8 Jun 2012
6. F. Lin, **S. Duttagupta**, A.G. Aberle, B. Hoex, "Excellent passivation of n^+ and p^+ silicon by PECVD SiO_x/AlO_x Stacks", Proc. of 27th European Photovoltaic Solar Energy Conference, Frankfurt, Germany, Sep 2012.
7. F-J Ma, **S. Duttagupta**, M. Peters, G. S. Samudra, A. G. Aberle, B. Hoex, "Numerical modelling of silicon p^+ emitters passivated by a PECVD AlO_x/SiN_x stack" Proc. of PV Asia Pacific Conference 2012 (PVAP 2012), Singapore (2012); Energy Procedia vol. 33, (2013) p. 104.
8. **S. Duttagupta**, Z. Hameiri, B. Hoex, A. G. Aberle, "Crystalline silicon surface passivation with industrial plasma silicon nitride and aluminium oxide", **[Oral presentation]**, Tech. Digest of 22nd PVSEC, China, (2012).
9. Z. Hameiri, **S. Duttagupta**, B. Hoex, A. G. Aberle, "The impact of deposition temperature on the passivation quality of industrial plasma deposited aluminium-oxide stack layers", **[Oral presentation]**, Tech. Digest of 22nd PVSEC, China, (2012).
10. **S. Duttagupta**, B. Hoex, A. G. Aberle, "Progress with industrially feasible passivation of lightly and heavily doped n-type silicon surfaces using inline PECVD silicon nitride", **[Oral presentation]**, Tech Digest of 22nd PVSEC, China, (2012).
11. F-J Ma, **S. Duttagupta**, M. Peters, G. S. Samudra, A. G. Aberle, B. Hoex, "Numerical analysis of p^+ emitters passivated by a PECVD AlO_x/SiN_x stack" Proc. of 3rd International Conference on Crystalline Silicon Photovoltaics (SiliconPV),

[Oral presentation], Hamelin, Germany, 2013; Energy Procedia, vol. 38, (2013) p. 124.

12. **S. Duttagupta**, Fa-Jun Ma, Bram Hoex, Armin G. Aberle, Extremely Low Surface Recombination Velocities on Heavily Doped Planar and Textured p^+ Silicon using Low-Temperature Positively-Charged PECVD SiO_x/SiN_x Dielectric Stacks with Optimised Antireflective properties, **[Oral presentation]**, Proc. of 39th IEEE PV Specialists Conference (PVSC), Tampa, Florida, USA, 16 - 21 Jun 2013.
13. **S. Duttagupta**, B. Hoex, A.G. Aberle, "Progress with industrially-feasible surface passivation of heavily-doped *p*-type and *n*-type crystalline silicon by PECVD SiO_x/SiN_x with optimised antireflective performance", **[Oral presentation]**, Proc. of 28th European Photovoltaic Solar Energy Conference, Paris, France, Sep 2013.
14. N. Nandakumar, F. Lin, B. Dielissen, F. Souren, X. Gay, R. Gortzen, **S. Duttagupta**, A. G. Aberle, B. Hoex, "Silicon surface passivation by Al_2O_3 films grown by spatial atomic layer depositions using low-cost precursors, Proc. of 28th European Photovoltaic Solar Energy Conference, Paris, France, Sep 2013.
15. Z. P. Ling, F-J Ma, **S. Duttagupta**, M. Tang, J. Ge, A. Khanna, R. Stangl, A.G. Aberle, T. Mueller, "Three-dimensional numerical analysis of hybrid hetero-junction silicon wafer solar cells with front-side locally diffused emitter and rear-side heterojunction BSF point contacts", **[Oral presentation]**, Proc. of 28th European Photovoltaic Solar Energy Conference, Paris, France, September 2013.
16. **S. Duttagupta**, Z. Hameiri, B. Hoex, and A.G. Aberle, "Dielectric charge tailoring in PECVD SiO_x/SiN_x stacks and its impact on industrial *p*-type silicon wafer solar cell efficiency," **[Oral presentation]**, Proc. of 40th IEEE PV Specialists Conference (PVSC), Denver, Colorado, USA, 7 - 13 Jun 2014. *Nominated for the* ***Best Student Contribution Award*** *in the Area 4 "Crystalline Silicon Photovoltaics"*
17. M. Wilson, Z. Hameiri, N. Nandakumar and **S. Duttagupta**, "Application of non-contact corona kelvin metrology for characterization of PV dielectrics on textured surfaces, Proc. of 40th IEEE PV Specialists Conference (PVSC), Denver, Colorado, USA, 7 - 13 Jun 2014.
18. **S. Duttagupta**, B. Hoex, and A.G. Aberle, "Progress with Cost-Effective Surface Passivation of p^+ Silicon by PECVD SiN_x" **[Oral presentation]**, Proc. of 29th European Photovoltaic Solar Energy Conference, Amsterdam, The Netherlands, Sep 2014. ***Best Student Contribution Award*** *for the most outstanding student research work in the field of "Wafer-Based Silicon Solar Cells and Materials Technology"*

Appendix II: PC1D simulation parameters

Summary of PC1D simulated parameters (Figures 2.6, 2.7 and 2.8).

Parameter	**Values**
Wafer thickness	180 µm
	Varied between 1 to 1000 µm for Figure 2.6
Wafer dopant type	*p*-type Si
Resistivity	1.5 Ω.cm
Bulk lifetime	500 µs
	Varied between 1 to 10 ms for Figure 2.7
Phosphorus emitter sheet resistance	60 Ω/sq.
Fill factor	80 %
Reflectance	2%
Front surface recombination velocity (S_{front})	10^4 cm/s
	Varied between 1 to 10^7 cm/s for Figure 2.8
Rear surface recombination velocity (S_{rear})	Varied between 1 to 10^7 cm/s for Figure 2.8

Appendix III: Contactless effective lifetime measurement

The standard procedure for measuring effective lifetime τ_{eff} of minority carrier in *c*-Si is the 'photoconductance' technique developed at Stanford University and commercialised by Sinton Consulting Inc. [Ref. 11 of Chapter 2]. In this thesis the effective lifetime of the passivated or unpassivated sample was measured using the photoconductance tool WTC-120 from Sinton Consulting Inc.

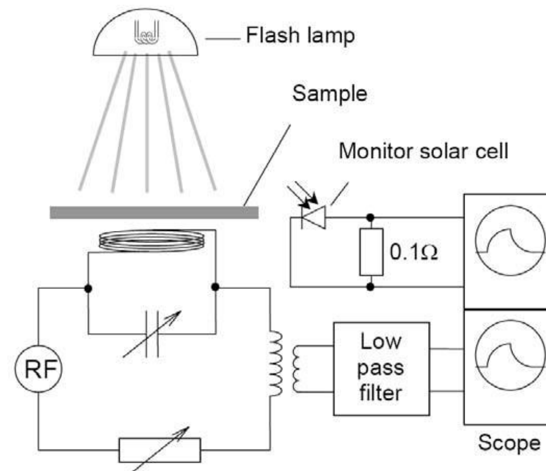

Figure AIII.1: Schematic sketch of the photoconductance measurement setup.

In this experimental setup, the measured silicon wafer is illuminated by a Xenon flash lamp, which has its spectrum distributed mainly at the wavelengths of 900 to 1000 nm. This near infrared light source allows fairly uniform profile of the excess carrier density Δn along the wafer thickness. During the lamp flash, the photoconductance of the measured wafer $\Delta\sigma$ is measured non-contact manner by using inductive coupling. At the same time, the light intensity is measured using a reference solar cell, which is placed very close to the measured sample. The excess carrier density Δn in the sample is calculated from the measured $\Delta\sigma$. Knowing the optical properties of the measured sample allows for the determination of the photogeneration rate within the sample measuring the illumination intensity with a monitor solar cell. After determination of both Δn and photogeneration, τ_{eff} can be calculated as a function of Δn (for more details see Ref. 28 of Chapter 2). Although a brief explanation in given in Chapter 2.

Appendix IV: Contactless corona-voltage measurements

[Taken from the manual of PV-2000, Semilab, Inc., USA]

The contactless corona-voltage (C-V) measurement is implemented in the Semilab's PV-2000 is an adaptation of corona-voltage metrology extensively used in the field of semiconductors for monitoring dielectrics and interfaces. The technique provides fast, preparation free measurement of electrical parameters that affect the passivation quality dielectrics for PV applications. The technique uses incremental corona-charging of dielectrics and measurement of the surface potential with a vibrating capacitive electrode i.e., a Kelvin-probe. The principle of noncontact corona-voltage technique is illustrated in Fig. AIV.1. A corona gun deposits an electric charge, ΔQ_c on the dielectric surface. The charged site is transferred to a position under a vibrating voltage probe to determine a change of the surface voltage. Sequential charging-measuring gives the *V-Q* characteristics that forms the basis for determining electrical parameters.

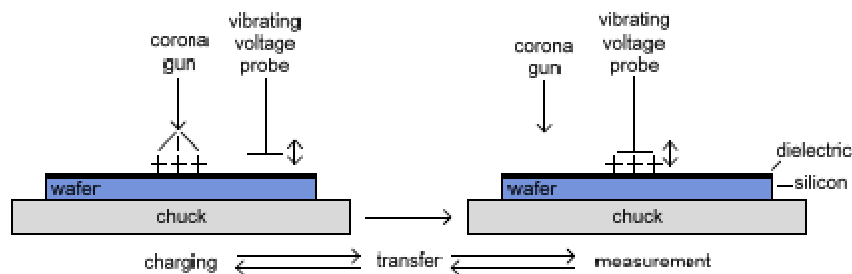

Figure AIV.1: Corona charging and voltage measuring used in noncontact corona-voltage metrology.

Corona charging

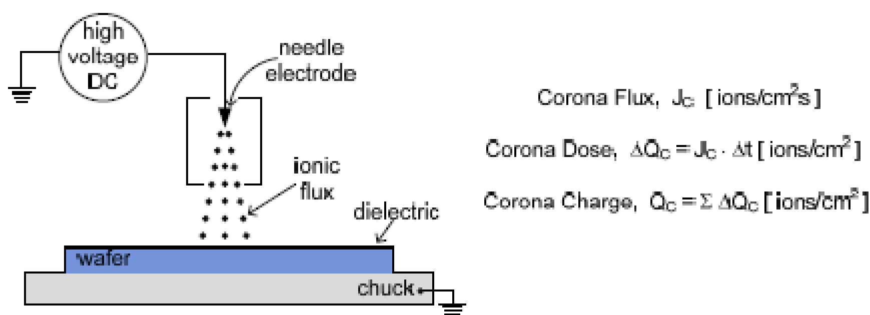

Figure AIV.2: Point-source corona gun used in noncontact C-V

Noncontact C-V uses a point source corona gun shown schematically in Fig. AIV.2, to deposit an ionic charge uniformly over an area 6 mm in diameter. Corona discharge in air is initiated by a high DC voltage applied to a needle electrode. Discharge current controls the corona flux. The flux and charging time, Δt, define the corona dose, ΔQ_c.

Charge polarity is determined by the polarity of high voltage. Positive corona in air deposits predominantly $(H_2O)_n\ H^+$ ions while negative corona deposits predominantly CO_3^- ions. The ions are thermalized and their deposition causes no damage to dielectrics. Corona charge can be removed by rinsing in water. The corona dose is calibrated using oxidized Si wafer of known thickness.

Kelvin probe voltage measurement

A vibrating Kelvin probe shown in Fig. AIV.3 is used to measure the contact potential difference, V_{CPD}, between the wafer and the reference electrode. Corona induced change of surface voltage ΔV, is then determined from ΔV_{CPD}. LED's are used to provide light pulses in order to measure V_{CPD} under strong illumination, V_{CPD}^{light}. In the Kelvin probe method a reference electrode vibrates above the wafer modulating the wafer-probe capacitance C. A bias V_{DC} is applied in series with V_{CPD} inducing an electric charge on the capacitor $Q(t) = (V_{CPD} + V_{DC})\ C(t)$. Periodic capacitance modulation $C(t) = C_0 + \Delta C \cos \omega t$ generates a corresponding AC current:

$$J = dQ/dt = \omega \Delta C(V_{CPD} + V_{DC}) \sin(\omega t) \ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

By nulling the ac current with V_{DC} bias, one obtains

$$V_{DC} = -V_{CPD}\ at\ J = 0 \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

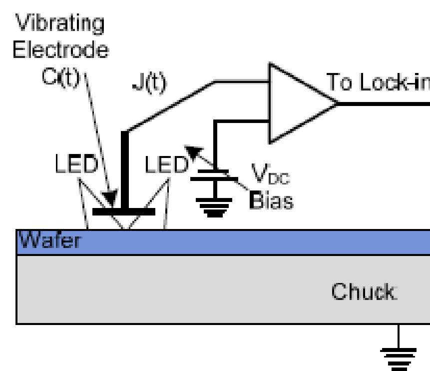

Figure AIV.3: The vibrating Kelvin Probe for measurement of surface voltage.

The 2 mm diameter probe is used in the PV-2000. It vibrates with frequency of about 1100 Hz enabling fast measurements of V_{CPD} ± 60 V with 0.2 mV precision at 10 ms time constant. The contact potential difference between two metals is given by a difference in metal work functions $V_{CPD} = \phi_{m1} - \phi_{m2}$. In the case of a semiconductor

substrate with a dielectric film on the top, the V_{CPD} contains not only the work function difference ϕ_{ms} between the metal reference electrode and the silicon substrate, but also two additional terms, i.e. the surface barrier, V_{SB} and the dielectric voltage, V_D. The corresponding V_{CPD} expression is:

$$V_{CPD} = \phi_{ms} + V_{SB} + V_D \quad (3)$$

A corresponding diagram of Si with a dielectric film is shown in Fig. AIV.4. The ϕ_{ms} contains the semiconductor work function that depends on the electron affinity χ_s value, and on the Fermi energy $E_C - E_F$. These quantities are shown in Fig. AIV.4.

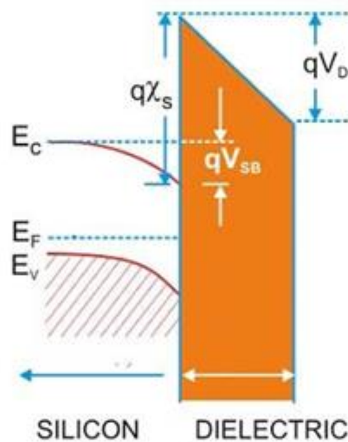

Figure AIV.4. The surface band diagram of *p*-type silicon with dielectric film

Effects of corona charging

The change of the contact potential difference (ΔV_{CPD}) caused by an increment of corona charge is equal to the change in the voltage drop across the dielectric (ΔV_D) plus the change in the surface barrier (ΔV_{SB}) (voltage drop across the space charge region):

$$\Delta V_{CPD} = \Delta V_D + \Delta V_{SB} \quad (4)$$

Strong illumination of the Si underneath the CPD probe flattens the surface barrier giving approximately V_{SB} = 0. Illumination does not affect V_D. Accordingly, CPD measurements in the dark and under illumination are used to determine ΔV_{SB} induced by corona charge:

$$V_{CPD}^{dark} - V_{CPD}^{light} = \Delta V_{SB} \quad (5)$$

$$V_{CPD}^{dark} - \Delta V_{SB} = \Delta V_D \text{ or } V_{CPD}^{light} = \Delta V_D \text{ ....(6)}$$

The determination of the ΔV_D and ΔV_{SB} due to an incremental corona charge allows the simple calculation of important dielectric parameters.

In the initial state *p*-Si with SiO_2 is under inversion, application of negative corona charge will first drive it to towards flat-band the amount of corona charge equals charge in the dielectric, Q_{total}. The corona charging, ΔQ_c, induces a mirror-charge in silicon, part of which appears in the space charge as ΔQ_{sc} and part in the interface traps as ΔQ_{it}, (Q_{OT} oxide trapped charge does not change).

Flat band voltage (V_{FB}) and Total charge in the dielectric (Q_{TOTAL})

The V_{CPD} in the dark and under illumination is systematically measured after incremental corona charging and a V_{CPD} versus corona charge (Q_c) plot is generated as shown in Fig AIV.5.

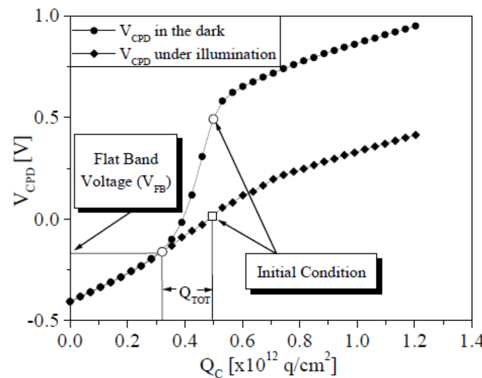

Figure AIV.5. Contact potential difference versus corona charge plot illustrating the determination of flat band voltage and Q_{TOT}.

The measurement sweeps the bands at the interface from accumulation through flat band and depletion to inversion. The flatband voltage (V_{FB}) is one of the important dielectric parameters providing information on process (such as gate oxide growth) stability. In the COCOS method the flat band voltage is considered to be the V_{CPD} value when the difference between the V_{CPD} curves in the dark and under illumination is zero (V_{SB}~0), as illustrated in Fig AIV.5. It is important to note that the V_{FB} determined using the COCOS method will differ from the V_{FB} determined using MOS capacitors primarily due to work function differences between the gate and CPD electrode. In the fabrication of MOS capacitors, a forming gas anneal is typically performed which is

not necessarily the case with the COCOS method in which oxides can be measured directly after oxide growth. This difference in the process history of the oxide will also cause a difference between corona-based diagnostics and the MOS technique.

Another very important dielectric parameter determined by the COCOS technique is Q_{TOT}. Q_{TOT} is the total charge from the initial charge state of the oxide/semiconductor system necessary to achieve the flat band condition. An example of the determination of Q_{TOT} with an initial state in depletion is shown in Fig AIV.5. In the COCOS technique Q_{TOT} is precisely determined from the V_{SB} vs. Q_C data as the Q_C difference between the initial V_{SB} value and flat band.

Interface state density

Fig AIV.6 illustrates an energy band diagram of the Si/SiO_2 system with a CPD reference electrode. In this diagram it is shown that the net effective dielectric charge, Q_D, including the deposited corona charge, must be imaged in the space charge region in order to fulfil the condition of electrical neutrality:

$$Q_D = Q_{IT} + Q_F + Q_{OT} + Q_M + Q_C = -Q_{SC} \qquad (7)$$

Therefore, a quantum of corona charge, ΔQ_C, deposited on the surface of the oxidized silicon can be imaged in the space charge region, ΔQ_{SC}, but can also be imaged in any oxide traps that can exchange charge with the bulk silicon, i.e., interface traps ΔQ_{IT}, Q_F is the fixed charge, Q_{OT} being oxide trapped charge, Q_M mobile charge.

$$\Delta Q_C = -(\Delta Q_{SC} + \Delta Q_{IT}) \qquad (8)$$

The surface space charge, Q_{SC}, can be determined from the surface barrier, V_{SB}

$$Q_{SC} = \pm \frac{\sqrt{2}\varepsilon_s kT}{qL_D} F\left(V_{sb}, \frac{n_0}{p_0}\right), \qquad (9)$$

$$F\left(V_{sb}, \frac{n_0}{p_0}\right) = \pm[\left(e^{-\beta V_{sb}} + \beta V_{sb} - 1\right) + \frac{n_0}{p_0}\left(e^{-\beta V_{sb}} + \beta V_{sb} - 1\right)]^{1/2}, \qquad (10)$$

F is the space charge function, which relates V_{SB} (band bending) to corresponding semiconductor space charge, Q_{SC} using well-known electrostatic relations, $\varepsilon_s = \varepsilon_0 k_s$ is

the permittivity of the semiconductor, where ε_0 is permittivity of vacuum and k_s is the dielectric constant of the semiconductor. kT is the thermal energy and q is the elementary charge.

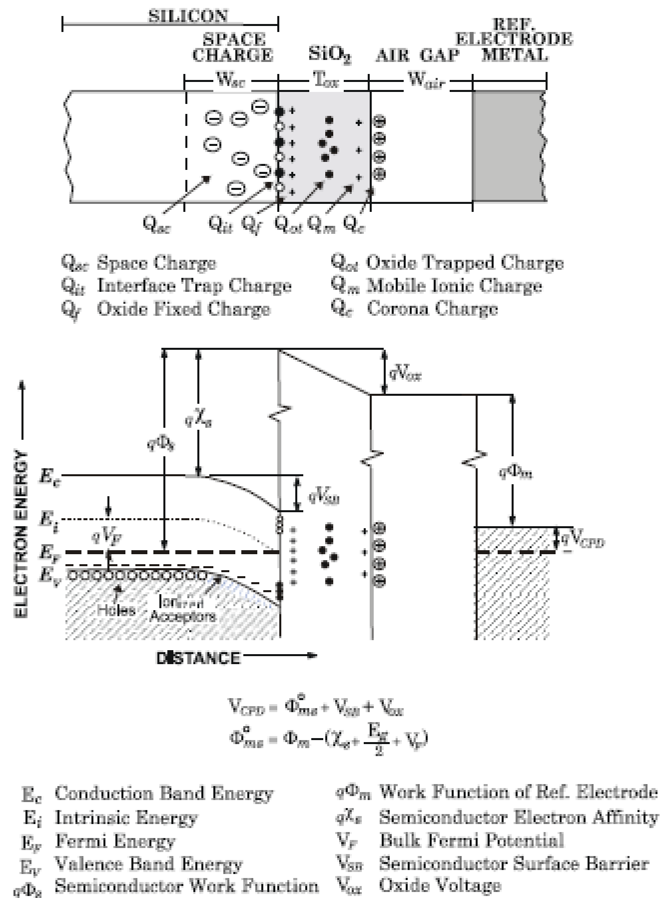

Figure AIV.6. Si/SiO_2 energy band diagram with a CPD reference electrode.

L_D is extrinsic Debye length for holes where $L_D = [\frac{\varepsilon_s}{qp_0\beta}]^{1/2}$. n_0, p_0 are the concentrations of free electrons and holes respectively in semiconductor bulk. $\beta = \frac{q}{kT}$. The interface trap charge, ΔQ_{IT}, corresponding to a given quantum of corona charge is determined from the following relation:

$$|\Delta Q_{IT}| = |\Delta Q_C| - |\Delta Q_{SC}| \qquad (11)$$

The density of interface traps, D_{it}, be calculated as the ratio $\Delta Q_{IT}/\Delta V_{SB}$, where ΔV_{SB} is the change in the surface barrier due to the deposited quantum of corona charge. A *Dit* spectrum can then be obtained by plotting D_{it} versus V_{SB}. The spectrum of D_{it} starts from the flatband condition, V_{SB}=0, and extends up to deep inversion. V_{SB} is actually analogous to position in energy band gap of silicon. For example, for a *p*-type Si (1.5

Ω.cm), V_{SB} close to 0 corresponds to energy about 0.2 eV above the valence band (the exact position is $E_v + E_F$ and it depends on the Fermi energy E_F above the valence band). Increasing V_{SB} corresponds to moving upward in energy toward the conduction band E_C. Thus a silicon band gap energy level dependent density of interface states can be extracted as shown in Fig AIV.7.

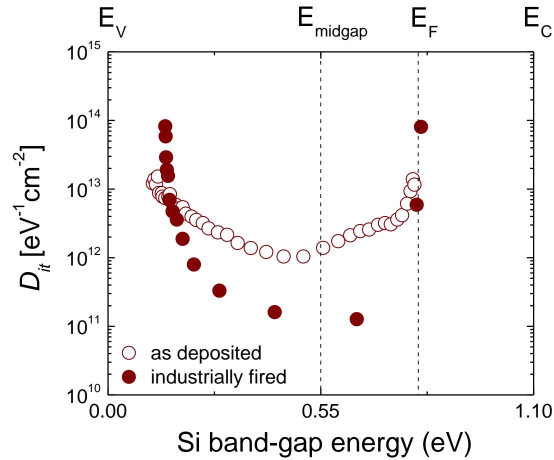

Figure AIV.7: Density of interface states as a function of silicon energy band gap. In this example the substrate used was *n*-type (4.5 Ω.cm), hence measurement starts from 0.27 eV below conduction band. The D_{it} at mid-gap level is below 10^{11} eV^{-1}cm^{-2}.

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