RF TRANSCEIVER DESIGN FOR WIRELESS SENSOR NETWORKS

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Declaration

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

CHUA DINGJUAN

31ST DECEMBER 2013

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Contents

Summary

Transceivers for wireless sensor networks (WSNs) and wireless body area networks (WBAN) are expected to consume low power for long battery life or to operate from other power supplies such as solar cells. Hence, techniques such as duty cycling and variable data rates are often adopted to reduce the overhead power consumption and increase the effective throughput per energy consumed. To satisfy these requirements without compromising on the throughput requirements of the application layer, high data rates and low power consumption are the main priorities of transceivers in WSNs and WBANs.

For WSNs or WBANs, the most commonly used frequencies are the 433.92-MHz band and the 2.4-GHz band in the license-free Industrial, Scientific and Medical (ISM) bands. At a lower frequency, the 433.92-MHz band consumes less power for the same propagation distance, however, the allowable emission bandwidth is limited at 1.085MHz and there are more stringent limitations on maximum output power. Therefore, in high data rate scenarios, the modulated power spectrum of the transmitter will be close to the bounds of the emission mask requirements. Any small frequency deviation from process variations and frequency drifts could cause transmission to fall out of band easily. Therefore, to maximize the data rate in the allocated channel bandwidth, the use of frequency calibration is necessary.

To reduce timing overhead without sacrificing on frequency calibration resolution, a coarse-fine frequency calibration technique is proposed. The

coarse calibration is based on time-to-voltage conversion (TVC) and successive-approximation-register based (SAR) architecture. The fine calibration employs the cyclic vernier time-to-digital-conversion (TDC) technique to overcome limitations of TVC technique at fine resolution. Achieving a frequency resolution of 120-kHz across the ISM band with a tuning range of 54-MHz, the calibration process only takes less than 18.5-μs. Implemented in 0.18-μm CMOS process, the OOK transmitter achieves a maximum data rate of 1-Mbps with -13.5-dBm output power while dissipating 1.7-mA from a 1.8-V power supply.

The 2.4-GHz operating frequency has a smaller propagation distance and higher power consumption. However it is a worldwide unlicensed band and has an emission bandwidth that is 11 times that of the 433.92-MHz band, allowing much higher data rates. Therefore, an energy-efficient transceiver by employing low power circuit design techniques is proposed. Operated at a voltage supply of 1.2-V, The on-off-keying (OOK) transmitter achieves an overall efficiency of 23% and a figure of merit of 0.1nJ/bit.mW operating at 10-Mbps at an output power of 0-dBm.

In OOK communication, the receiver needs to asynchronously oversample the incoming signal which increases the power consumption in the receiver. This design presents a low power and energy efficient 2.4-GHz OOK self-aligning super-regenerative receiver (SRR) for high data rate applications. A simple preamble-based digital quench self-alignment scheme is proposed to achieve synchronous recovery of the payload. The proposed self-alignment scheme oversamples the preamble to find the optimal phase to synchronize the incoming data. The quench frequency can be reduced to the data rate after the synchronization and hence improve the energy efficiency of the receiver. The SRR consumes 0.16-nJ/bit for a sensitivity of -65-dBm at a data rate of up to 10-Mbps.

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Chapter 1

Introduction

1.1 Background

Wireless Sensor Networks (WSNs) consist of many tiny nodes (called sensor nodes, SN) connected together wirelessly. In a typical star network topology, these SNs are controlled by a central node and communicate only with the central node. Each node senses the parameter of interest, converts it to digital data, does limited processing on the data, and communicates through the transceiver. The parameter measured by the sensor can be environmental parameters such as temperature, humidity, human health parameters like heart rate, blood glucose, cardiac activity, brain activity etc., or for identifying objects and their movement. Wireless Body Area Networks (WBAN) also belong to the family of WSN with specific attention to health care or monitoring physiological parameters on, in or around the body. WBAN applications include e-health services like ECG, EEG, temperature, blood pressure, heart rate, movement/acceleration, camera on a pill (PillCam), implanted medical devices, etc.

The typical scenario of WBAN is as shown in Figure 1.1 [3]. Sensor Nodes (SN) shown at the bottom of the figure communicate information to the Personal Servers

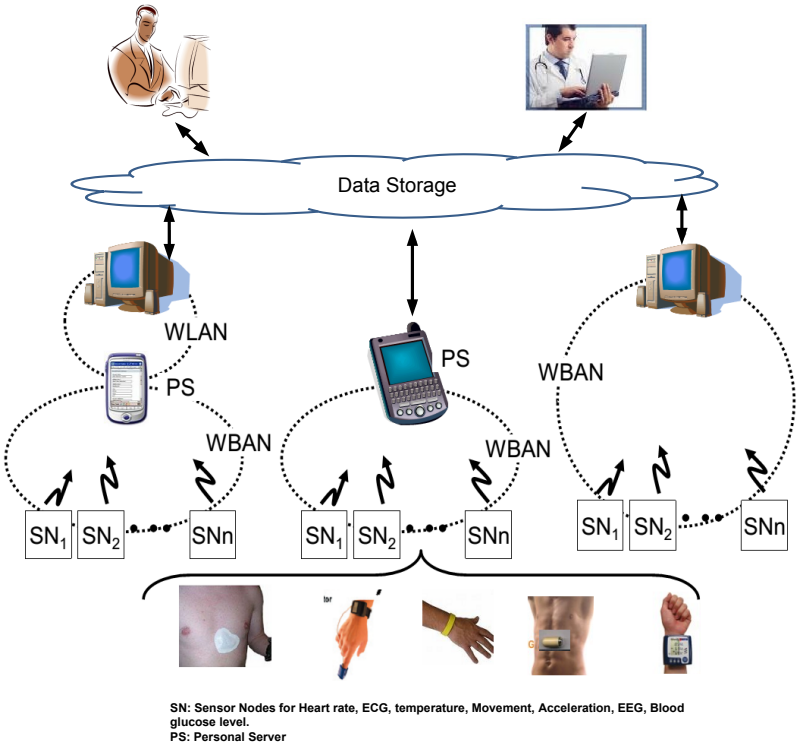


Figure 1.1: Typical Scenario of Wireless Body Area Network (WBN).

(PS) which is typically situated a short distance (<10m) away. The PS may be a dedicated smart phone or personal digital assistant (PDA) with a WBAN transceiver. SNs are typically either worn by the patient or implanted while the PS may be carried by the locations or located in a central place, such as in the room/ward. Healthcare professionals then access the data through the Internet or WBAN network as shown.

To achieve portability and long-term wear, each SN should be small in form factor and should work for long periods of time powered by a single battery and/or by energy harvested from the environment. Since the transceiver typically consumes the most power in a SN, low power consumption is essential. Considering the short transmission distance and long battery life requirements of the WBAN nodes, the main requirements on the physical layer are as listed [4].

1. Duty Cycling

   To reduce power consumption in transmission overheads, the transceiver

should be employed under high duty cycling between active and standby modes. The transceiver should also be switched on only if necessary and should consume minimal power during sleep or standby modes.

2. Low Complexity Modulation Schemes

   Typically covering a wireless range of less than 10m, spectral efficiency can be traded off for power efficiency such that low complexity modulation schemes such as on-off keying (OOK) or frequency-shift keying (FSK) can be adopted.

3. Flexible Data Rate

   With a graceful trade off between power consumption and data rate in low complexity modulation schemes, a flexible or adaptive data rate enables the Medium Access Control (MAC) layer to determine the most appropriate data rate to achieve energy savings.

4. Low cost, light weight and small size

To achieve high duty cycling while fulfilling the minimum throughput requirements of the application layer, the transceiver requires high data rates to transmit more data in a single packet. In addition, this data rate should be flexible and easily adjusted to allow the MAC layer to adaptively change the data rate to achieve optimum energy savings. To achieve low power consumption, the OOK modulation scheme is preferred as during the transmission of a '0' bit, little or no power is consumed. The complexity and power consumption of OOK receivers can also be greatly reduced as they can be simplified to only detect the presence and absence of a carrier in the bit period. However, this is at the expense of interference or noise rejection. Since any intentional or unintentional energy present in the frequency band may be mistaken as a signal, OOK transceivers are also typically more subjective to interference or noise and maybe be more suitable for less crowded frequency bands. Last, to achieve low cost and a small form factor, the use of bulky off-chip passives

should be reduced.

Standard compliant transceivers such as Zigbee and WirelessHART based on IEEE 802.15.4 among other standards such as Bluetooth are also popular for WBAN and WPAN applications. Although these transceivers provide compliance to standards, the power consumption is typically very high. For example, the commercial IEEE 802.15.4 compliant 2.4-GHz zigbee RF transceiver, CC2520 [5] from Texas Instruments consumes a current of 77.4-mW and 55.5-mW in transmit and receive modes respectively, which is 10 times more than the proposed transceiver specifications. In late 2010, the Bluetooth Low-Energy (LE) standard was introduced for low data rate and infrequent communication from nodes where the critical low power requirement is needed. State-of-the-art implementations [6] consume powers of 8.9-mW and 4.8-mW at 1-Mbps in transmit and receive modes respectively. Though the power consumption is an order lower than Bluetooth, it is only able to support a maximum payload of 216-bits and the energy efficiency is still larger than $>$1-nJ/bit for each operation.

1.2 Design Considerations

For WSNs or WBANs, the most commonly used frequencies of operation lie in the license-free frequency bands where the user of these products do not need an individual license from the telecommunication regulatory authorities. This frequency range is between 300-MHz and 2.5-GHz and is often referred to as the Industrial, Scientific and Medical (ISM) band. Governed by the regulatory bodies of the Federal Communications Commission (FCC) in the United States and the European Telecommunications Standards Institute (ETSI) in the European Union, there are limitations placed on the operating frequencies, output power and emission bandwidth on the wireless transceivers.

Amongst the ISM band of frequencies, two of the most commonly used bands in WSNs and WBANs are the 433.92-MHz band and the 2.4-GHz band. The 433.92-MHz band spans from 433.05-MHz to 434.79-MHz over a channel bandwidth of 1.74-MHz. This frequency band is frequently adopted for biomedical applications as signals in the 400-MHz range can propagate through human body tissues. Its proximity to the MedRadio band [7] and overlap with the 420-MHz to 450-MHz narrowband frequency channel designated in the IEEE 802.15.6 standard [8] for WBAN applications is also another reason for its popularity. With a lower carrier frequency and path loss, the propagation distance of the 433.92-MHz carrier is approximately 6 times larger than a 2.4-GHz carrier when at the same output power. However, due to the lower operating frequency, there are more stringent limitations on maximum output power emissions. The smaller allocated bandwidth also limit the maximum data rate.

The 2.4-GHz band spans from 2.4-GHz to 2.4835-GHz over a channel bandwidth of 83.5-MHz. Despite a smaller propagation distance, the 2.4-GHz frequency band is a unlicensed band worldwide [9] (US, Europe, Japan, China, etc), which maximizes the portability of the wireless sensor nodes. The much wider channels allow much higher data rates that cannot be matched by the lower frequencies. The 2.4-GHz band is also used by common commercial wireless technologies such as WiFi, Bluetooth and Zigbee. Consequently, components for this frequency band are more readily available and hence are likely to be at much lower cost than the other bands. However, the higher operating frequency typically means higher power consumption for transmission and reception. In addition, one downside of operating in this band is the susceptibility to interference from other wireless technologies that are also occupying this band.

From the design perspective of the transceiver, the two main important parameters

Table 1.1: Emission Power and Bandwidth Limits

	FCC		ETSI	
Freq (MHz)	EIRP (dBm)	Bandwidth (MHz)	EIRP (dBm)	Bandwidth (MHz)
433.92	< -13.3	<1.085	$< +12.15$	No Limits
2400	< -0.23	<12	$< +10$	No Limits

are the output power and allowable bandwidth of the transmitter. The FCC regulatory limits specify the maximum electrical field strength, E, at a distance, r, from a transmitting antenna for various frequency bands. However, the parameter of interest is the maximum power that can be supplied to the antenna in order to satisfy the limits of E. To calculate this, (1.1) can be used to convert the maximum electrical field strength to an equivalent output power (dBm). This is defined as the Effective Isotropic Radiated Power (EIRP) and represents the transmission power limits in the frequency bands [9].

$$EIRP = 10log\left(\frac{4\pi \times E^2 \times r^2}{0.377}\right) \tag{1.1}$$

The emission bandwidth limits are specified in FCC Section 15.231(c) [10]. The regulations state that the emission bandwidth shall be no wider than 0.25% of the center frequency for devices operating above 70-MHz and below 900-MHz. For devices operating above 900-MHz, the emission shall be no wider than 0.5% of the center frequency. The emission bandwidth is determined by the points in the radiated spectrum that are 20-dB below the modulated carrier.

Based on the above discussion, Table 1.1 summarizes the maximum emission power and maximum emission bandwidth limits meted by the FCC and ETSI for the two respective bands. As can be seen, comparing between the FCC and ETSI, the FCC imposes stricter limitations on the emission power and emission bandwidth of transceivers operating within the ISM bands. For the course of this dissertation, the

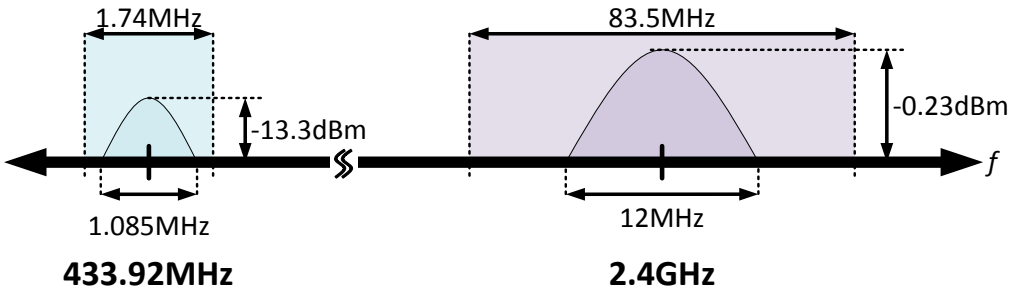


Figure 1.2: Comparison of Power and Bandwidth limits between 433.92-MHz and 2.4-GHz Band.

requirements will largely reference the FCC regulations.

Fig. 1.2 illustrates the frequency channel bandwidth, FCC output emission bandwidth and output power limits of the 433.92-MHz and 2.4-GHz band for comparison. It can be observed that the allowable emission bandwidth in the 433.92-MHz band is about 11 times smaller at 1.085-MHz and is limited to a maximum output power of -13.3-dBm. In addition, when the emission bandwidth is fully occupied, the output spectrum of the transmitter will occupy about 62% of the available frequency channel bandwidth of 1.74-MHz, causing it to be near the bounds of the emission mask. This is in comparison to the 2.4GHz frequency, where the fully occupied emission bandwidth only occupies 14% of the frequency channel bandwidth. The much larger allowable emission bandwidth also makes it more suitable for high data rate (>2Mbps) transmissions.

1.3 Research Objectives

As discussed in Section 1.2, by virtue of the operating frequency, transceiver design in the 433.92-MHz and 2.4-GHz frequency bands have vastly different specifications and design requirements. Therefore, this dissertation is partitioned into two sections, where in each section we seek to address the unique concerns respective to each frequency band.

As mentioned in Section 1.1, high data rates and low power consumption is a priority of transceivers in WSNs and WBANS. Based on previous works [11], low power consumption and high data rates were previously achieved at 433.92-MHz. In such high data rate scenarios, the modulated power spectrum of the transmitter will be close to the bounds of the emission mask requirements. Any small frequency deviation from process variations and frequency drifts could cause transmission to fall out of band easily. With limited quality factors that can be achieved for on-chip inductors, these short-term frequency drifts are further amplified in decreasing technology nodes. Therefore, to maximize the data rate in the allocated channel bandwidth, the use of frequency calibration is necessary, which is also the focus of the first half of this dissertation.

Frequency calibration allows us to adjust the frequency of the carrier back to the desired value and therefore, finer frequency steps would allow the modulated spectrum to be better fitted into the emission mask. However, a smaller frequency resolution leads to a longer calibration time as typically more time is required to measure smaller frequency steps. Therefore a coarse-fine frequency calibration technique is proposed. The coarse calibration based on the TVC technique with a binary capacitor array for frequency tuning, controlled by the successive-approximation logic. To achieve better frequency resolution and avoid the mismatch limitation in TVC technique, an additional fine calibration is performed based on the time-to-digital conversion (TDC) technique is proposed, which enables us to achieve $<$140-kHz resolution.

Different from the 433.92-MHz frequency band, transceiver operation with high data rates and low power consumption in the 2.4-GHz frequency band face much lesser bandwidth limitations as the emission bandwidth is 11 times larger and can accommodate much higher data rates. In addition, as the fully occupied emission

bandwidth only takes up 14% of the available frequency channel bandwidth, the issue of frequency drifts is less pronounced. However, due to the higher operating frequency, the power consumption is much larger. Intended as the physical layer implementation of an energy-efficient scalable health-care system-on-chip (SoC) for WBANs in collaboration with two fellow researchers working on the MAC, baseband and front-end application layers, the second half of this dissertation focuses on energy-efficient transceiver design by employing low power circuit design techniques.

For the design of the transmitter, an energy-efficient 2.4-GHz transmitter design is demonstrated. The transmitter includes a LC-based VCO with an on-chip inductor and a class-AB differential power amplifier. To achieve optimum energy efficiency, the oscillator and power amplifier are designed and optimized in tandem. Operated at a voltage supply of 1.2-V, The transmitter achieves a normalized figure of merit [12] of 0.1nJ/bit.mW at a data rate of 10-Mbps while providing an output power of 0-dBm.

On the receiver side, two architectures of receivers are explored to achieve low power consumption and small chip area. In the first architecture, the envelope detection receiver architecture is implemented to achieve low power consumption and small chip area. Due to area limitations, an inductorless design is adopted. Demonstrating a worse case bit error rate (BER) of 10^{-2} for a sensitivity of -65-dBm and a high data rate of 5-Mbps, the receiver consumes 2.9-mA from a 1.2-V voltage supply, achieving a FOM of 0.7-nJ/bit.

To further reduce power consumption, the super regenerative architecture is adopted in the second version. Super regenerative receivers (SRRs) achieve large RF front end gain while consuming very low power by making use of the high regeneration gain from an oscillator. The oscillator is controlled periodically by the quench signal and samples the incoming OOK signal at the quench signal's

frequency. However, in non-coherent OOK communication, as the incoming signal is asynchronous, the receiver needs to oversample the incoming signal in order to recover the input data reliably. This increases the power consumption in the receiver. In addition, as a high quenching frequency increases the noise bandwidth of the SRR receiver, high oversampling ratios are not preferred. Therefore, this work presents a simple preamble-based digital quench self-alignment scheme to achieve synchronous sampling. The proposed self-alignment scheme oversamples the preamble to find the optimal phase to synchronize the incoming data. The quench frequency can be reduced to the data rate after the synchronization and hence improve the energy efficiency of the receiver. The proposed SRR achieves a FOM of 0.16-nJ/bit for a sensitivity of -65-dBm at a data rate of up to 10-Mbps.

1.4 Organization of the Dissertation

The rest of this dissertation is organized as follows.

Chapter 2 presents the 433.92-MHz frequency calibrated transmitter. System level considerations for 433.92-MHz ISM transceivers will be discussed to arrive at the frequency calibration and transmitter specifications. The design of the frequency calibration system and transmitter will be discussed in detail. A review and comparison with relevant published research work is also presented.

Chapter 3 begins with the system level considerations for WSN and WBAN transceivers operating at 2.4-GHz. The link budget is considered to derive the transmitter and receiver specifications. A review of relevant published research work is also presented. Subsequently, the design of the OOK transmitter is presented. To achieve high energy efficiency, the low power circuit topologies and techniques that have been used are discussed. Detailed measurement results are also presented to demonstrate the favourable FOM and high efficiency achieved. Lastly, the design

of two OOK receivers will be described. The first design discusses a compact and low power envelope detection receiver. Measurement results and comparison with recent works in literature will also be discussed. The second design presents the low power super regenerative architecture with digital quench self-alignment for high data rates. Measurement results will be presented and comparisons with recent works in literature will also be discussed.

Chapter 4 concludes the dissertation and discusses possible areas of future work.

Chapter 2

433.92-MHz Frequency Calibrated Transmitter Design

As mentioned in Section 1.1, high data rates and low power consumption is a priority of transceivers in WSNs and WBANS. However, in such high data rate scenarios, the modulated power spectrum of the transmitter will be close to the bounds of the emission mask requirements. Any small frequency deviation could cause transmission to fall out of band easily. In practical situations, process variations often cause the frequency of the oscillator to deviate from the designed value. In addition, variations in environmental conditions such as temperature changes cause frequency drift in the oscillator with time. With limited quality factors that can be achieved for on-chip inductors, these frequency drifts are further amplified in decreasing technology nodes. Even though these frequency drifts are relatively small in magnitude, they cannot be neglected. Therefore, frequency calibration is required.

During frequency calibration, the carrier frequency of the transmitter needs to be accurately set so that the data rate can be maximized within the allowable emission bandwidth limits while ensuring that the output spectrum is well under the required

spectral mask. In addition, the carrier frequency of the transmitter needs to be set such that it is aligned within the input bandwidth of the receiver for proper reception.

In this chapter, a frequency calibrated 433.92-MHz transmitter with a tuning range of 54-MHz and a frequency resolution of $\leq$140-kHz over the ISM band of 433.05-MHz to 434.79-MHz is described. To compensate for frequency drifts due to process variation, a coarse SAR and fine TDC calibration architecture is proposed. The choice of TDC for fine calibration avoids the limitations in TVC based frequency tuning technique. The frequency calibration process can be completed in less than 18.5-µs or 8.5-µs and 10-µs for coarse and fine calibration respectively. With a simple speed-up circuit for the oscillator, the transmitter achieves a data rate of 1-Mbps at an output power of -13.5dBm.

2.1 Frequency Accuracy

To calibrate an out-of-band carrier frequency into the ISM band spanning 433.05-MHZ to 434.79-MHz with a channel bandwidth of 1.74-MHz, theoretically a frequency resolution of 1.74-MHz is sufficient. However, in high data rate scenarios where the modulated spectrum occupies a relatively large proportion of the available channel bandwidth, finer frequency control will allow better fit of the modulated spectrum into the emission mask.

As described in section 1.1, FCC section 15.231(c) [10] states that the emission bandwidth of the modulated spectrum must be smaller than 0.25% of the centre frequency, where the emission bandwidth is determined by the points in the radiated spectrum that are 20-dB below the modulated carrier. Therefore, the maximum allowable emission bandwidth at the centre of the ISM band at 433.92-MHz is 1.085-MHz. Assuming a fully occupied emission bandwidth of 1.085-MHz, the frequency resolution required to fit this occupied bandwidth into the ISM channel

bandwidth of 1.74-MHz is approximately 330-kHz. In addition to the occupied bandwidth, the frequency stability of the transmitter needs to be considered. To achieve a typical frequency stability of $\pm$100-ppm, the frequency resolution should be accurate to $<$86-kHz.

Since these frequency requirements are independent, they can be fulfilled through coarse and fine calibration processes. For example, when the transmitter is first switched on, coarse calibration can be carried out to set the carrier frequency to be within the frequency channel bandwidth. Subsequently, during operation, the fine calibration process can be periodically enabled to calibrate the carrier frequency for frequency drifts before packet transmission. Defining them as independent processes can help to reduce unnecessary power consumption as the respective calibration processes are only executed when needed. Based on the frequency bandwidth and stability requirements, the coarse and fine frequency resolution requirements of the transmitter are defined to be 330-kHz and 86-kHz respectively.

One main source of frequency deviation in oscillators is due to process variations in the passive components and transistors. Therefore, to accommodate these process variations, a 10% margin of frequency tuning range is incorporated into this design. This allows the digitally controlled oscillator (DCO) to be tuned 44-MHz from 412-MHz to 456-MHz. To achieve the desired fine frequency resolution of 86-kHz, the frequency tuning range is designed to be tuned across approximately 9 bits of resolution.

2.2 Background

Frequency calibrated transmitters can generally be categorized into open-loop and closed-loop architectures. Closed-loop OOK/FSK transmitters based on phase-locked or frequency-locked loops automatically lock its frequency to the

reference frequency and therefore no additional frequency calibration is needed. While providing high frequency accuracy, it requires continuous loop operation. Furthermore, the constraint on the loop bandwidth limit the maximum achievable data rate [13]. Open-loop OOK/FSK transmitters are subject to the PVT variations and the carrier frequency needs to be calibrated.

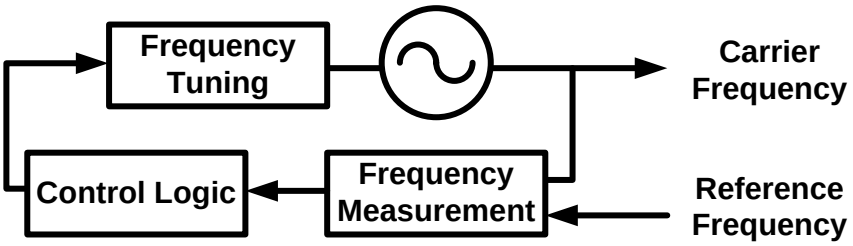


Figure 2.1: Block Diagram of Generic Frequency Calibration System

Typical frequency calibration techniques for open-loop transmitters, as shown in Figure 2.1, consist of frequency measurement and tuning circuits. It monitors the difference between the carrier and reference frequencies, and calibrates the carrier frequency back to the desired value through a feedback loop. Frequency measurement is often one of the most time consuming operations in the calibration process as typically more time is required to achieve finer resolution in the time or frequency measurements.

A straightforward method to measure the carrier frequency is by simply counting the number of cycles over a fixed time window [14]. Though lower in implementation complexity, the calibration time increases exponentially with respect to frequency resolution. For example, to achieve 10-bit resolution, at least 1024 cycles need to be counted. A period-based frequency comparison technique is proposed in [1], where time-to-voltage conversion (TVC) is used to convert the time difference between two signal periods into an equivalent voltage through a charge pump. This voltage is then evaluated successively by the SAR control

logic. The TVC method achieves a similar frequency resolution as the previous method but only requires n cycles for n-bit resolution, therefore reducing calibration time significantly. However, inherent mismatches in the charging and discharging currents of the charge pump limit the frequency resolution that can be achieved. Although this resolution can be increased by reducing the reference frequency, or by accumulating multiple T-to-V conversions, both result in longer calibration time. Last, the time-to-digital conversion (TDC) architecture based on the inherent delay of logic gates can also been used to measure the frequency with very high timing resolutions. However, depending on the resolution, the TDC approach may also take a long time to measure the frequency. In addition, despite the high resolution, accumulative jitter limits the range of the TDC.

Frequency tuning is the next block in the frequency calibration system and can be performed as part of the VCO or DCO. The tuning can be either continuous or in discrete levels, depending on the architecture of the oscillator. For continuous tuning, varactors are usually involved where the control voltage to the varactor determines the equivalent capacitance. For discrete tuning, a capacitor array is usually employed where the digital code to the capacitor array determines the equivalent capacitance.

It can be observed that the choice of the frequency measurement technique is a compromise between frequency resolution and calibration time. Therefore, an appropriate choice can be made based on the required frequency resolution which will be discussed in the following section.

2.3 System Architecture

To achieve 9 bits of frequency resolution over a tuning range of 44-MHz with a minimum amount of calibration time, a coarse-fine frequency calibration technique is proposed. The coarse calibration is performed based on the TVC

technique with a binary capacitor array for frequency tuning, controlled by the successive-approximation logic. This leverages on the short calibration time of the TVC technique. However, to achieve better frequency resolution and avoid the mismatch limitation in TVC technique, an additional fine calibration is performed based on the TDC technique, which enables us to achieve $<$140-kHz resolution.

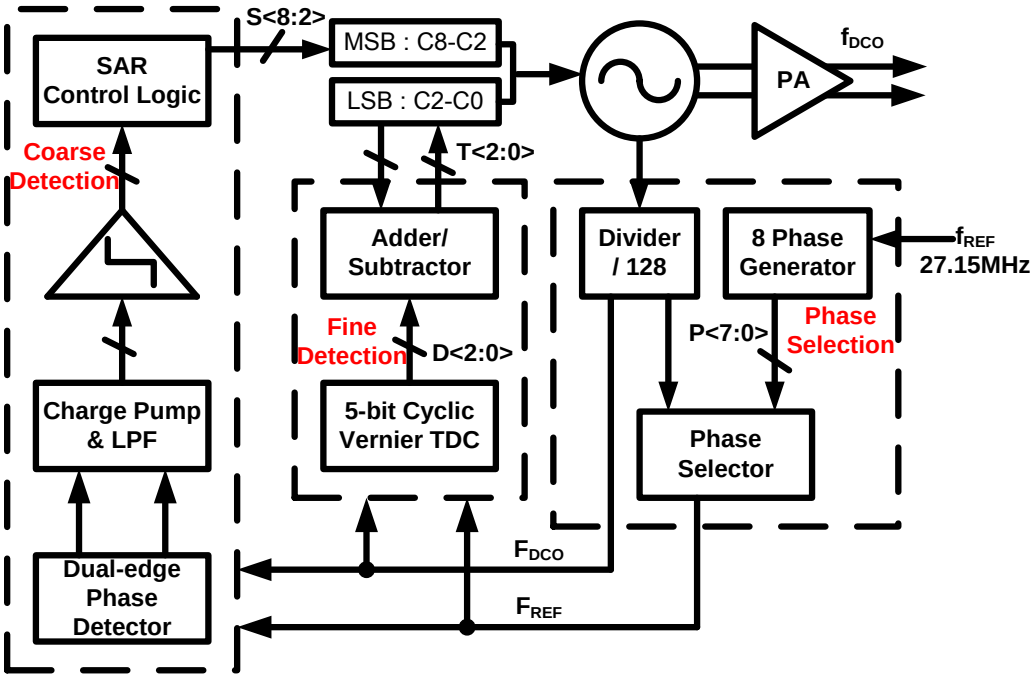


Figure 2.2: System Block Diagram

Figure 2.2 shows a block diagram of the proposed transmitter with frequency calibration. The transmitter mainly consists of four function blocks: the phase selector, the SAR coarse calibration, the TDC fine calibration and the transmitter blocks. The system includes two modes of frequency calibration, coarse and fine, that can be carried out independently. This allows the coarse and fine calibration processes to be carried out as independent foreground and background processes respectively. For example, when the system is first powered up, coarse calibration can first be executed to align the transmission frequency to the desired frequency channel as a foreground process. Subsequently, during the operation

of the transmitter, fine calibration can be carried out periodically prior to packet transmissions as a background process to calibrate for gradual frequency drifts. For example, during TDMA transmissions, the MAC layer would wake-up the transceiver some margin time before its allocated time slot. This timing margin can be increased and the extra time can be used to carry out frequency calibration. Alternatively, a series of 1 bits can be padded before the actual preamble which can be used for the calibration phase.

The coarse frequency calibration block tunes the main coarse capacitor array, which consists of 7-bit binary weighted capacitors, C_{8C} to C_{2C}. The conventional incremental search algorithm converges in a worst case 2^N number of cycles while the binary search algorithm converges in a fixed $(N+1)$ number of cycles, where N is the resolution. Therefore, the binary search algorithm with a fixed calibration time is preferred. Since the SAR clock frequency is derived from the oscillator frequency, it will run at a varying frequency of $f_{DCO}/4N$, where N is 128 in this design. Assuming the lowest , the maximum or worse case coarse calibration time is 8.5-µs. When coarse calibration is completed, the digital output is latched in the registers.

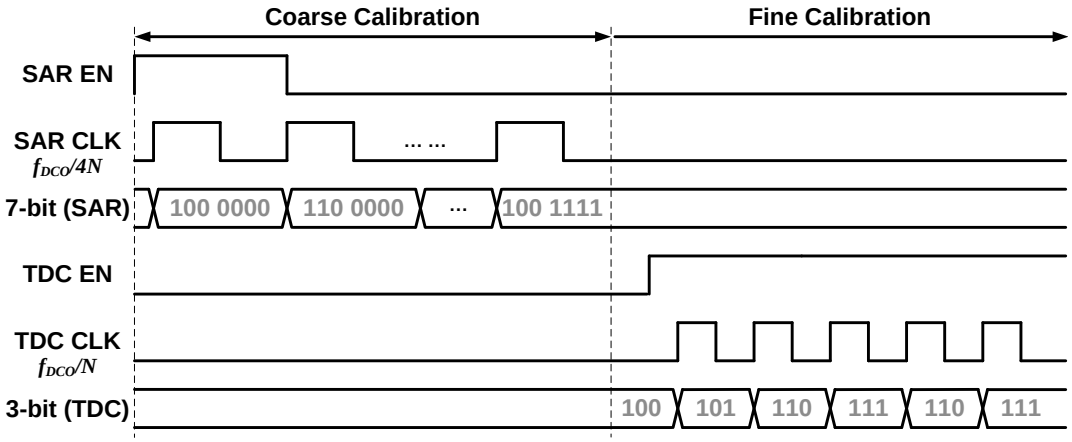


Figure 2.3: Timing Diagram of Calibration Scheme

To further increase the frequency accuracy, the fine frequency calibration block

can be enabled. The fine tuning is performed through a 3-bit fine capacitor array, C_{2F} to C_{0F}, where the most significant bit (MSB) C_{2F}, overlaps with the least significant bit (LSB) C_{2C} of the coarse array. The overlap of the tuning curves allows the fine calibration scheme to correct possible frequency misalignment of ± 1 LSB at the end of the coarse calibration scheme. The cyclic vernier TDC is employed to measure the frequency in the fine calibration. The TDC clock frequency runs at a varying frequency of f_{DCO}/N and is expected to achieve a stable output in less than 10-µs.

These calibration times can be quantitatively measured as a contribution to timing overhead during data transmission. Coarse calibration can be assumed to be a foreground process that is used to select the appropriate frequency channel upon powering up of the system. In such initialization modes, a calibration time in the order of microseconds is negligible. However, as fine frequency calibration may need to be repeated periodically as a form of background calibration, this calibration time is significant and can be measured as an overhead during the transmission of a data packet. Assuming that the calibration needs to be done prior to every transmission, a 10us calibration would correspond to an overhead of 10-bits for a 1-Mbps data rate. For packet lengths of 32 byes and above, this contributes an overhead of less than 4%.

2.3.1 Phase Selection

The time to voltage (TVC) block is a key building block to the proposed frequency calibration scheme as it converts the frequency difference between the reference and DCO signal to a time difference for quantification.

The phase selection block consists of a frequency divider, a 8-phase generator and a phase selector [1]. The choice of the external frequency reference is a tradeoff between calibration time and power consumption of the calibration process. As this

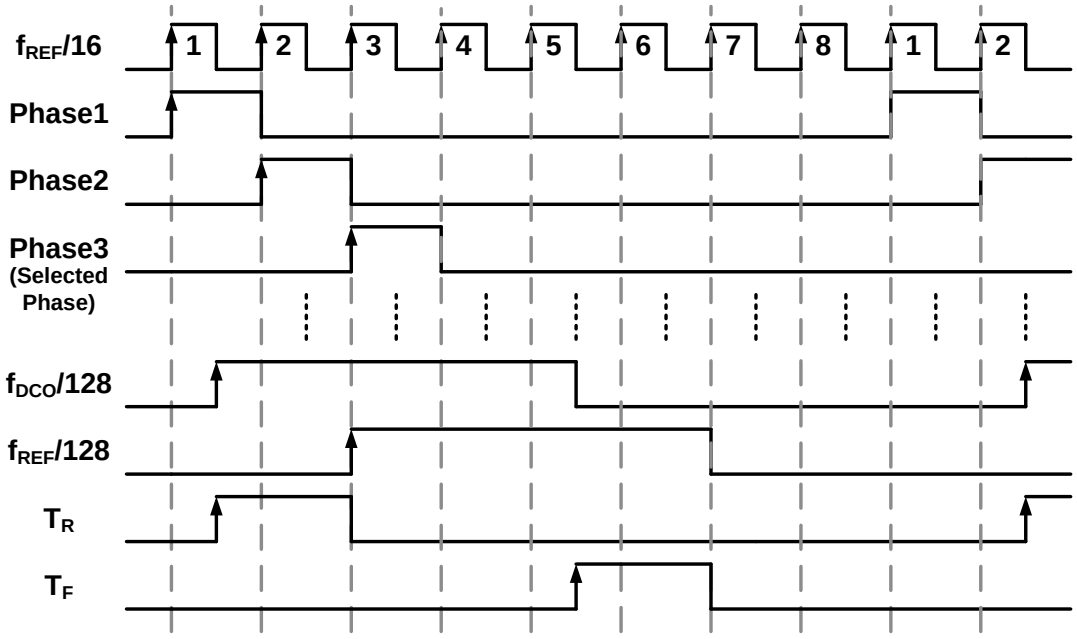


Figure 2.4: Timing Diagram of Phase Selection Block.

frequency reference is externally provided, a division ratio of 16 selected so that the commercially available crystals at 27.12-MHz can be directly used. Thus the external reference signal is at a frequency of $f_{REF}/16$ where f_{REF} is the targeted calibration frequency. For ease of calculation throughout this chapter, f_{REF} is taken to be 434-MHz and the corresponding external reference signal is calculated to be 27.125-MHz.

The phase selection block begins the time-to-voltage conversion by producing two signals for phase comparison. The timing diagram of the phase selection block is shown in Figure 2.4. The external reference signal $f_{REF}/16$ is further divided by 8 on chip to generate eight non-overlapping reference phases while the DCO frequency is divided down by 128. By using the rising edge of the DCO signal as the trigger signal, the *r-th* reference phase with the smallest phase difference with respect to the rising edge of the DCO can be identified. By subsequently obtaining the phase differences between the rising edges of the DCO and reference signals and using them to control the charging and discharging of a charge pump, the time difference

can be converted into an equivalent voltage.

However, since the reference and DCO signals are not synchronized, the time difference between the $(r+1)$-th reference phase and the DCO signal will range from 0 to $16/f_{REF}$-µs, falling in the dead zone of the charge pump. Therefore to avoid the dead-zone region of the charge pump, the phase selector selects the third reference phase $(r+2)$-th as the reference signal instead. In the example shown in Figure 2.4, the rising edge of $f_{DCO}/128$ falls within the signal Phase 1. Therefore, to avoid the dead zone region, Phase 3 will be selected instead, which corresponds to the phase of $f_{REF}/128$ in the figure.

The dual-edge phase detector then generates the pulse signals T_R and T_F which are equivalent to the time differences between the rising and falling edges of the DCO and reference phase signal. Effectively, $|T_R - T_F|$ represents the difference between the periods of the DCO and reference signal. Both coarse and fine calibrations use this phase information to tune the frequency of the DCO.

2.3.2 Coarse Calibration

The coarse calibration block, as indicated in Figure 2.2, consists of the dual-edge phase detector, charge pump, comparator and SAR control logic blocks. The dual-edge phase detector and charge pump in combination with the phase selector block effectively converts the phase difference between the DCO and reference into a voltage and tunes the DCO frequency through the SAR logic.

Pulses T_R and T_F represent the time difference between the periods of the DCO and reference signal. Therefore, by using these pulses to control the charging and discharging of a charge pump, this period difference can be converted into a net voltage value. The magnitude and polarity of this voltage values indicate the frequency difference and whether f_{DCO} is higher or lower than f_{REF}. To improve

the accuracy of the charge pump and enlarge the time-to-voltage ratio, the charging and discharging of the charge pump is carried out twice with two sets of pulses. The final net voltage value is compared with a reference voltage by the comparator. The comparator output is then provided to the SAR control block.

The SAR conversion phase consists of $(N+1)$ cycles where N is the number of bits. In the first phase, the MSB is first set to 1 while all the remaining bits are set to 0. The time difference between the DCO and reference frequency is then measured through the TVC block. If the comparator output is '1', it indicates that $f_{DCO} > f_{REF}$, the current bit remains at '1', else the current bit will be switched to '0'. This is repeated successively until all 7 bits have been updated, providing a final digital output of $S<8:2>$. This corresponds to a final frequency of

$$f_{REF} - \Delta f_C < f_{DCO} < f_{REF} + \Delta f_C$$

where Δf_C is the frequency resolution of the coarse tuning array in the ISM band at 330-kHz. For a fixed frequency step, the corresponding time resolution required differs for different frequencies as the period is different for each frequency. Therefore, the time resolutions for all frequencies within the ISM band are considered and the smallest resolution is taken. The formula used and the final time resolution calculated are as shown below.

$$\frac{1}{f_U} - \frac{1}{f_U + \Delta f_C} < \frac{\Delta t_C}{128} < \frac{1}{f_L} - \frac{1}{f_L + \Delta f_C}$$

$$223\text{-ps} < \Delta t_C < 225\text{-ps}$$

where Δf_C is 330-kHz, f_L is the lower bound of the ISM band at 433.05-MHz and f_U is the upper bound of the ISM band at 434.79-MHz. Therefore, the minimum time resolution that must be discerned by the coarse calibration scheme is 223-ps.

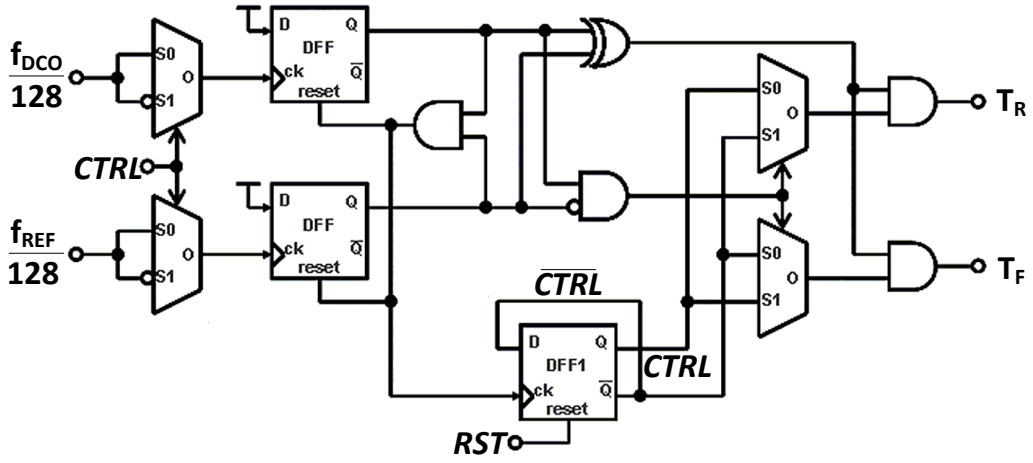


Figure 2.5: Schematic of Dual-Edge Phase Detector. [1]

Based on the required time resolution, the specifications of each of the block can be derived accordingly. The achievable frequency or time resolution of the TVC coarse calibration topology is dependent on a few factors. The mismatch in the phase detector and mismatch in the charge pump contributes error in the output voltage to the comparator. Along with the comparator offset voltage they affect the voltage comparison precision. They will be discussed in the following sub-block sections.

2.3.2.1 Dual-Edge Phase Detector

The dual-edge phase detector generates the pulses T_R and T_F, which represent the time difference between the rising and falling edges of $\frac{f_{DCO}}{128}$ and $\frac{f_{REF}}{128}$. The time difference between is ideally equal to the period difference between the signals $\frac{f_{DCO}}{128}$ and $\frac{f_{REF}}{128}$. However, any mismatch between the generation of the T_R and T_F signals will contribute errors to the frequency resolution.

The schematic dual-edge phase detector implemented is shown in Figure 2.5. This circuit avoids mismatch between the generation of T_R and T_F by reusing the phase detector circuit for both the rising edges and falling edges. This is achieved by using the phase detector to first find the time difference between the rising edges.

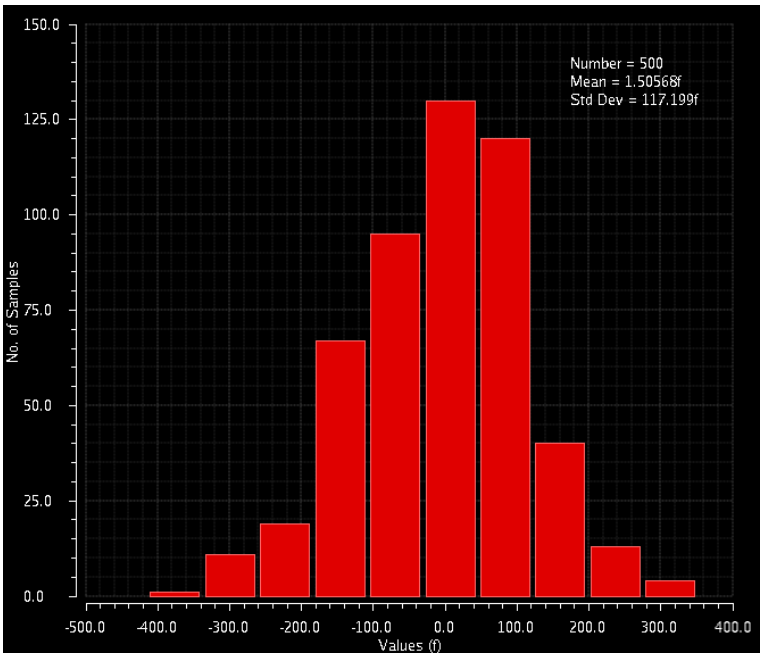


Figure 2.6: Histogram of 500 Monte Carlos simulations for mismatch between propagation delays.

Subsequently, by toggling the *CTRL* signal, both the input signals are inverted during the falling edges such that the same circuit can be reused to find the time difference again between the falling edges. By using only one phase detector instead of two parallel phase detectors, area is reduced and the mismatch is reduced to the mismatch between the propagation delays between the two inverters used to invert the signals.

To evaluate this, 500 Monte Carlos simulations were ran for the mismatch in propagation delays on the rising edge and the falling edge of the two inverters. As shown in Figure 2.6, the worst-case mismatch between the two inverters is $<$400-fs. As established in 2.3.2, the time resolution that must be discerned by the coarse calibration scheme is 223-ps. Therefore, the worst-case mismatch in the propagation delay between the inverters used is considered to be negligible in reference to the time resolution.

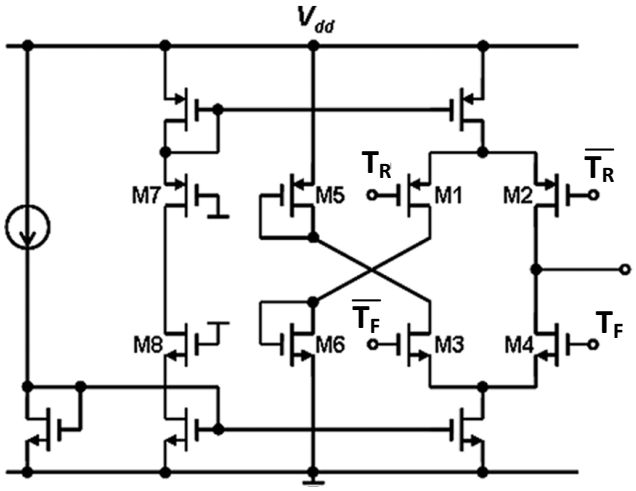


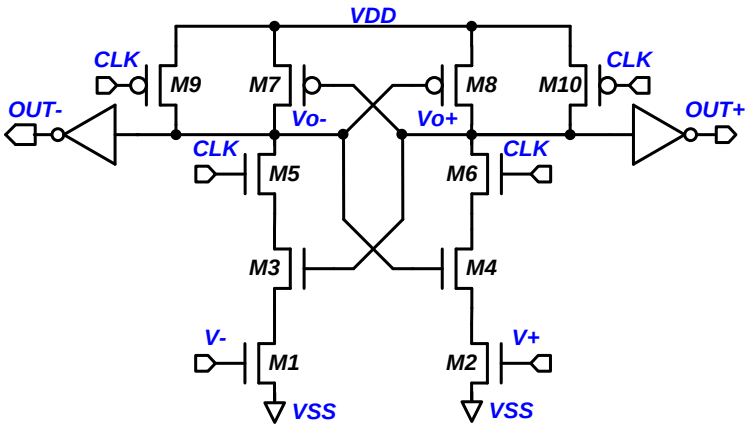
Figure 2.7: Schematic of Charge Pump. [1]

2.3.2.2 Charge Pump

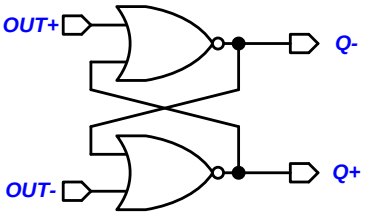
The time difference between T_R and T_F pulses will be converted in an equivalent voltage through the charge pump. However, various factors can cause current mismatch in the charge pump which contributes error to to the conversion from the time to voltage domain. The different considerations in the charge pump design are discussed in the following.

The schematic of the charge pump implemented is as shown in Figure 2.7. As the process used is not a sub-micron technology node, channel length modulation is not pronounced and a doubling of transistor length only reduces channel modulation effect by about 8%. Therefore, minimum size devices are used in the design of this charge pump.

In this implementation, the time-to-voltage conversion is also performed twice before voltage comparison. This doubles the voltage difference at the comparator input and relaxes the comparator design requirements. It can also be interpreted to improve the calibration precision and reliability for a given comparator design. Even though accumulating more time-to-voltage conversions can further improve the voltage comparison precision, it is at the cost of increased calibration time.



(a) Regenerative comparator.



(b) SR Latch.

Figure 2.8: Circuit diagram of the dynamic comparator.

For a time resolution of ±223-ps, simulation results show that the voltage difference produced at the output of the charge pump for a charge pump current of 100-uA is about ±5-mV. This determines the minimum allowable offset of the comparator which is the succeeding stage of the charge pump. Based on simulation results, similarly for a time resolution of ±223-ps, the allowable charge pump mismatch is 0.5% due to the small time resolution.

2.3.2.3 Comparator

As developed in the previous point, the comparator must be required to discern voltage differences of at least ±5-mV and the required resolution of the comparator should be at least 5-mV. However, the input offset voltage of the comparator will also play a part in determining the overall resolution of the comparator.

A dynamic comparator based on the Lewis-Gray topology [15] which has low

static power consumption is adopted. The schematic of the comparator is shown in Figure 2.8. During the reset phase, when the CLK is VSS, $Vo+$ and $Vo-$ nodes of the regenerative latch are reset to VDD. During the comparison phase, when CLK changes to VDD, the transistors M5 and M6 are turned on. The input transistor pair (M1 and M2) starts to charge the output nodes, $Vo+$ and $Vo-$, at different rates which is proportional to the applied input voltage ranging from VDD to VSS. The cross-coupled P-type transistors (M4 and M5) are turned on and this initiates the positive feedback process enabling the regeneration of a small differential voltage $\triangle V_{in} = V+ - V-$ to a full swing differential output. A pair of inverters is added to the differential output stage of the comparator so that it improves the driving capability for the next SR latch stage. After the regenerative latch stage, the SR latch performs a conversion from return-to-zero to non-return-to-zero. The circuit of the SR latch is as shown in Figure 2.8b.

To reduce the input offset voltage this, reasonably large device sizes are used and careful layout is done in the comparator design. To evaluate the input offset voltage of the comparator, 500 Monte Carlos simulations were carried out and the simulation results are shown below.

The Monte Carlos simulations were executed for a capacitive load of 100-fF at a mid-rail voltage of 0.9-V. The simulation results show that the comparator achieves a mean offset of 0.35-mV which is below the $\pm$5mV resolution requirement. The offset exhibits a standard deviation of 4.75-mV which is also still below the 5-mV requirement.

2.3.3 Fine Calibration

Due to inherent matching limitations in the charge pump, the time resolution that can be converted to an equivalent voltage through the TVC process is limited. As

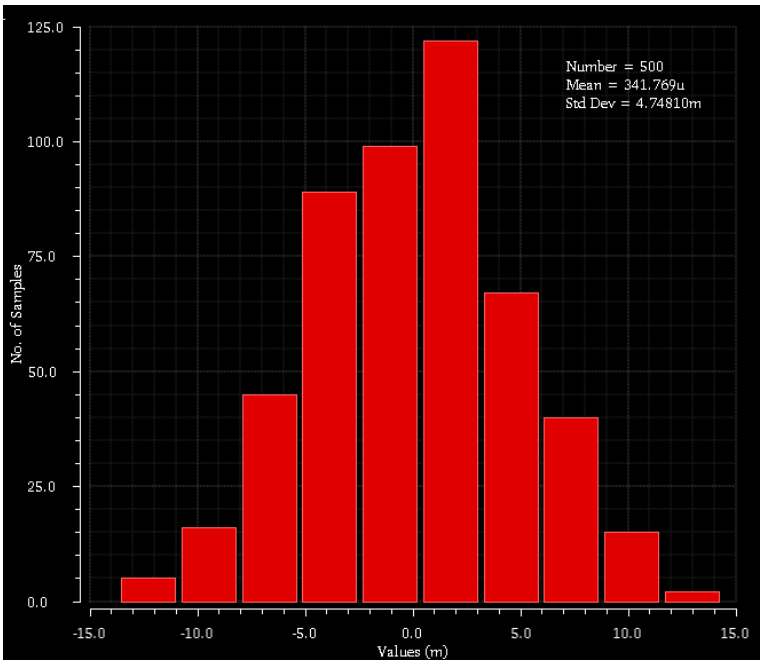


Figure 2.9: Histogram of 500 Monte Carlos Simulations for Comparator Input Offset Voltage.

discussed in Section 2.1, the required frequency resolution step is 86-kHz across the ISM band. This means that the TDC must be able to resolve the time differences in periods between signals at frequencies $f/128$ and $(f+\Delta f_F)/128$ where Δf_F is 86-kHz. For a fixed frequency step, the equivalent period differences can be calculated to find out the time resolution required. The time resolution of the TDC is calculated as shown in (2.1),

$$\frac{1}{f_U} - \frac{1}{(f_U+\Delta f_F)} < \frac{t_{LSB}}{128} < \frac{1}{f_L} - \frac{1}{(f_L+\Delta f_F)}$$
$$57.5ps < t_{LSB} < 58ps \tag{2.1}$$

where f_L is the lower bound of the ISM band at 433.05-MHz and f_U is the upper bound of the ISM band at 434.79-MHz.

To quantify time delays in an order of hundreds of picoseconds and below, the direct time digitization in the TDC architecture is chosen as it avoids the stringent

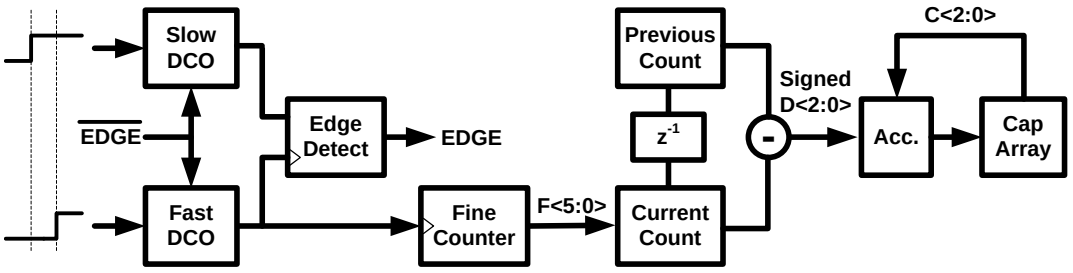


Figure 2.10: TDC Block Diagram

requirements on the accuracies of the comparator and charge pump in the TVC process. In TDC, the conventional vernier delay line architecture is commonly used for its simplicity and low power consumption. It is able to quantify time pulses with a time resolution equivalent to the delay of a unit buffer cell. However, as the nominal fanout-of-4 (FO4) delay of an inverter in 0.18-µm process is 75.6-ps [16] and approximated to be 150-ps for a unit buffer cell, such delay line TDC schemes are insufficient. In addition, such architectures are prone to process variation and mismatches in the delay cells. Therefore, a TDC architecture that can achieve a resolution better than the delay of a single buffer or in other words, sub-inverter delay resolution is necessary and the cyclic Vernier TDC architecture is adopted [17].

Figures 2.10 and 2.11 shows the block diagram and timing diagram of the cyclic Vernier TDC respectively. When the first rising edge is detected, denoted as F_{DCO} in Figure 2.11, the slow DCO starts to oscillate with a period of T_S, and the number of cycles is counted by the coarse counter. After an input delay of T_{INPUT}, the second rising edge occurs, denoted as F_{REF} in Figure 2.11, which triggers the faster DCO to oscillate with a period of T_F. At this time, the coarse counter is disabled, and the output of the counter represents a coarse measurement of the time between F_{DCO} and F_{REF}. The residue of the input delay (T_{FINE}) is measured by the vernier structure.

As T_F is slightly smaller than T_S, the time difference between rising edges of the

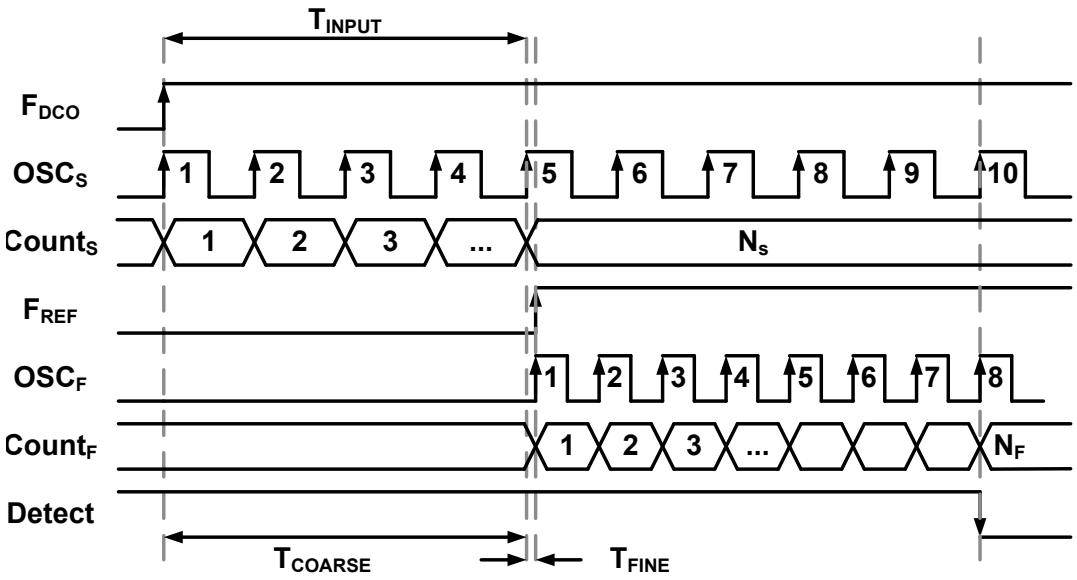


Figure 2.11: TDC Timing Diagram

two oscillations is reduced every cycle by the difference in periods (T_S - T_F), and the edge of the fast DCO eventually catches up with the slow DCO. By counting the number of cycles it takes for the fast DCO to catch up with the slow DCO, T_{FINE} is measured. The overall measurement of the time difference can be expressed as

$$\Delta T = T_{COARSE} + T_{FINE} = N_S T_S + N_F (T_S - T_F) \tag{2.2}$$

It can be observed that the fine resolution of the TDC does not depend on the absolute frequencies of the DCOs but only their difference in periods. While the delay of a unit buffer cell is prone to process variations and mismatches, the difference in periods of the DCOs is repetitive and consistent, allowing the TDC to achieve the required timing resolution consistently. Therefore, to achieve the required time resolution as calculated in (2.1), $T_S - T_F$ is designed to be 45-ps to provide a safe margin.

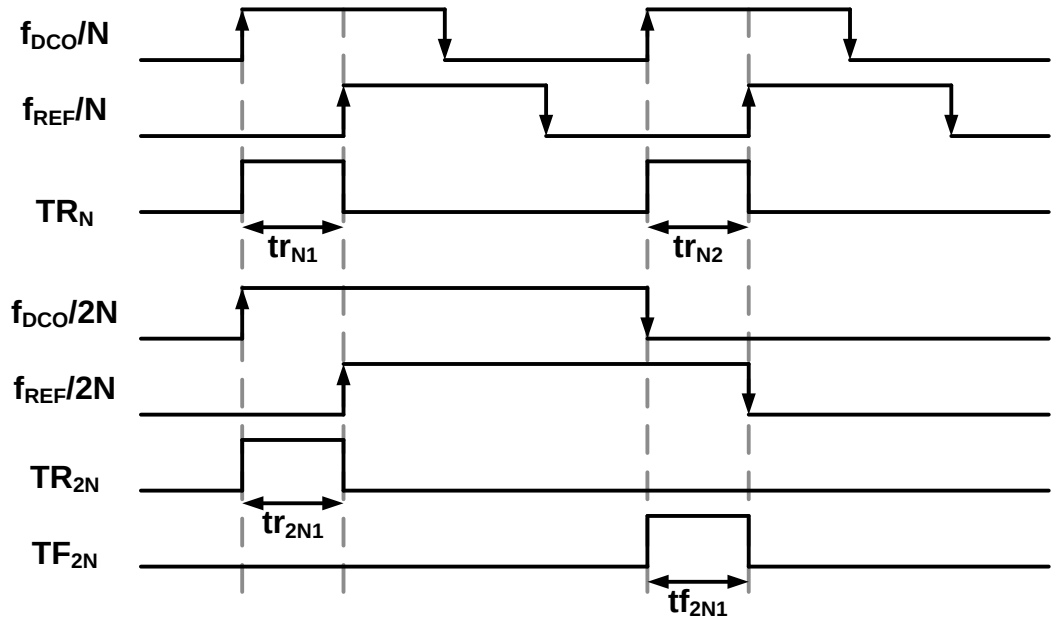


Figure 2.12: Comparing successive rising pulses in TDC.

2.3.3.1 TDC Control Logic

Similar to the operation of the TVC in the SAR calibration process, the rising and falling edges corresponding to the pulse widths of T_R and T_F can be utilized to obtain the period differences between F_{DCO} and F_{REF}. However, the inversion of the F_{DCO} and F_{REF} signals for operation during the falling edges require additional control logic and risk delay mismatches that would affect the accuracy of the conversion process. Therefore, trading off calibration time for implementation accuracy and complexity, only successive rising edges are utilized. Similar to the operation of the TVC in the SAR calibration process, when the pulse widths of T_R and T_F in a period are exactly equal, it indicates that the DCO frequency is exactly equal to the reference frequency. This understanding can similarly be extended to comparing successive T_R pulses as it is equivalent to comparing T_R and T_F at half the current operating frequency. This is illustrated in Figure 2.12 where the pulse width of tr_{N2} is the same as that of tf_{2N1}. Thus, the input signals F_{DCO} and F_{REF} for coarse

calibration block are reused here to avoid the mismatches in delays between the different phases in the phase selection process.

Preset to a mid rail value of '100' when it is not under operation, the TDC is assumed to be enabled only after the SAR calibration has been completed where the DCO frequency is accurate to a resolution of Δf_C. Therefore, the input frequency to the TDC $F_{DCO} \varepsilon \{(f_{REF} - \Delta f_C)/128, (f_{REF} + \Delta f_C)/128\}$ where Δf_C is 330-kHz, the frequency resolution of the coarse tuning array. The range of period differences expected for 433.05-MHz$\leq f_{REF} \leq$434.79-MHz is calculated to be $\pm$232-ps, corresponding to approximately $\pm 5 \times t_{LSB}$. Due to the phase selection process, the reference signal has a minimum delay of one clock pulse with respect to the DCO signal creating a large coarse count which does not carry necessary information and can be neglected. Therefore, only the fine count N_F is utilized in the calibration logic. To accomodate $\pm 5 \times t_{LSB}$, N_F is designed to be a 5-bit counter.

The difference between successive fine counts are accumulated and updated as the digital code of the fine capacitor array as shown in Figure 2.10. Based on this, the TDC calibration logic is as follows.

1. The previous fine count is subtracted from the current count :
   $\Delta N_F = N_F(t = N) - N_F(t = N-1)$ where $\Delta N_F \varepsilon \{-3, 3\}$
2. $\Delta N_F > 0 \Rightarrow f_{DCO} > f_{REF}$, $\Delta N_F < 0 \Rightarrow f_{DCO} < f_{REF}$
3. Fine capacitor array code is updated with the value of ΔN_F :
   $C_F(t = N) = C_F(t = N-1) + \Delta N_F$

Theoretically, ΔN_F converges to zero where the frequency of the DCO remains equal and locked to the reference frequency. However, in the presence of noise, the digital code stabilizes to two most stable values and oscillates between these two values as demonstrated in Figure 2.13.

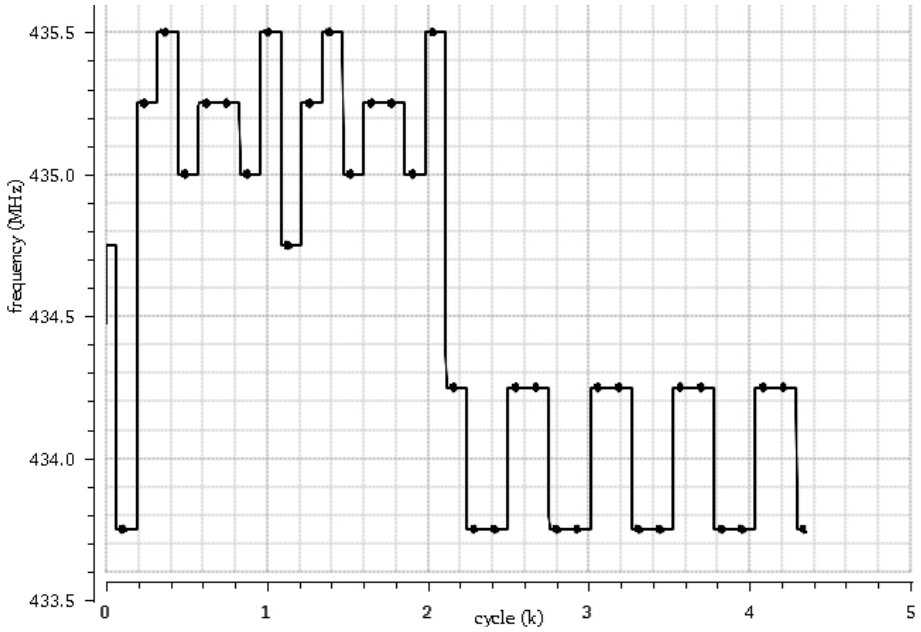
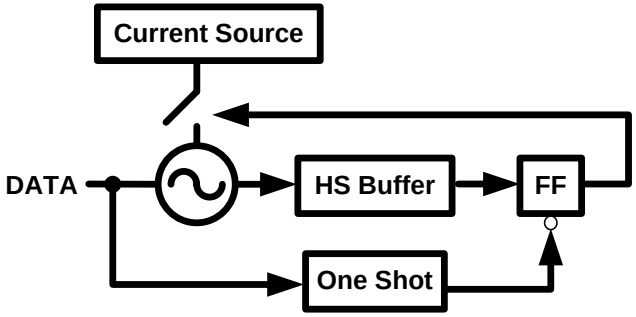


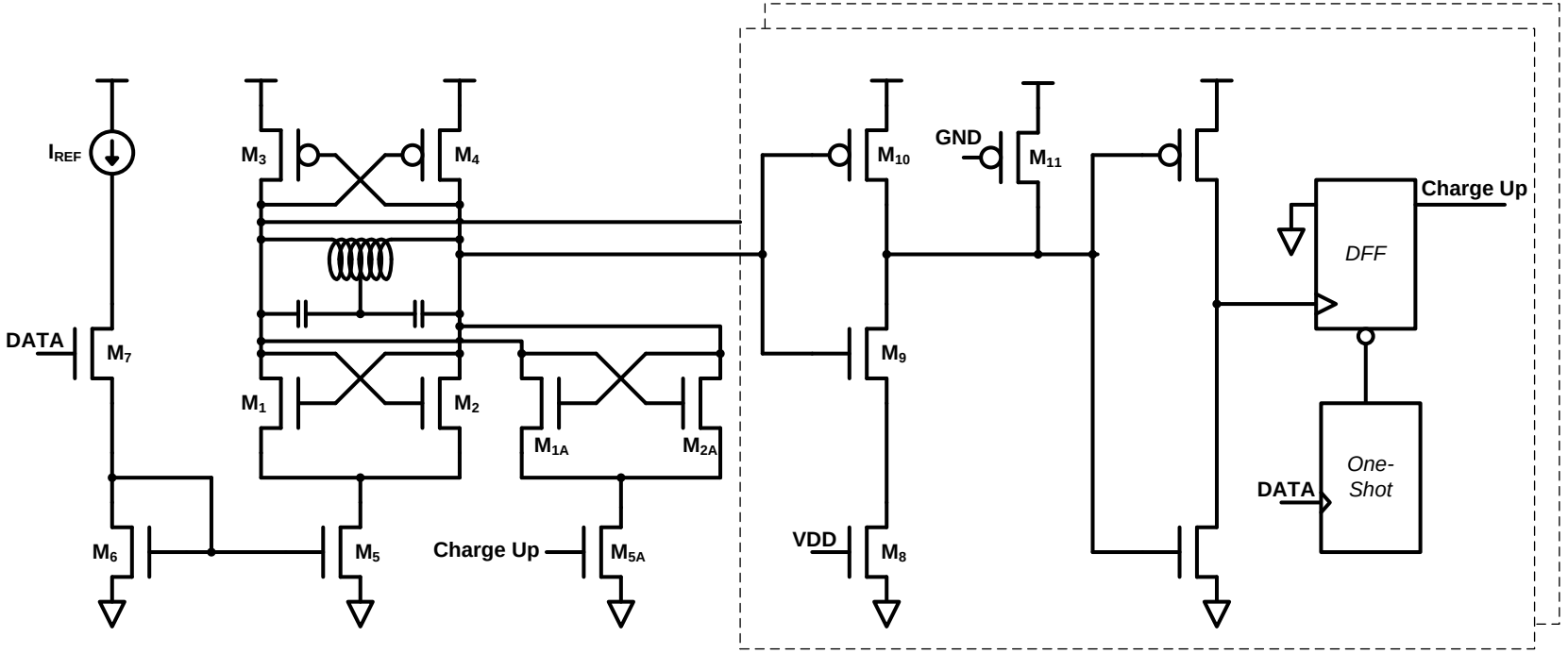
Figure 2.13: Convergence of TDC Digital Output Code.

2.4 Transmitter Architecture

Due to the range of frequencies and varying capacitor loads from tuning the capacitor array, the rise time and settling time of the DCO can vary greatly for a constant drain current. This increases the calibration time required and decreases the achievable data rate of the transmitter. Therefore, to achieve the required data rate and reduce the calibration time, the rise time and settling time of the oscillator must be minimized. However, designing for the worst-case conditions results in a waste of power at nominal conditions. Therefore, an automatic charge-up circuit that reuses the digital interface circuits between the DCO and the digital control logic is proposed.



(a) DCO Block diagram.



(b) Schematic of DCO with Automatic Charge-up Circuit

Figure 2.14: Schematic of DCO circuit.

Figure 2.14 shows the proposed mixed-signal DCO with the automatic charge-up circuit. It consists of an LC-tank DCO and an automatic charge up block that includes a secondary NMOS transconductance pair, a high-speed buffer, a D Flip-flop and a one-shot pulse generator. When DATA input is high, the one-shot pulse generator resets the D flip-flop to output a high signal, enabling the secondary transconductance pair M1A and M2A. Once the oscillations attain sufficient amplitude to drive the buffer stage, the flip-flop is triggered and the Charge-Up signal disables the secondary transconductance pair automatically.

The schematic of the circuit is shown in Figure 2.14b, for simplicity, only half of the fully differential circuit is illustrated. The LC-tank DCO adopts complementary-type PMOS and NMOS pairs. Compared with a NMOS or PMOS only cross-coupled topology, using a complementary cross-coupled structure has two main advantages. First, the additional complementary transistor pair results in twice the negative resistance offered to the LC-tank for a given current consumption to compensate for losses. Second, when the PMOS and NMOS transistors are matched in terms of transconductance and parasitic capacitances, the oscillating wave form of the complementary topology is more symmetrical, which significantly decreases the upconversion of $1/f$ device noise to the $1/f^3$ phase noise region around the carrier [18]. In order to reduce power consumption, a large inductor value of 20-nH was selected to increase the loop gain of the DCO. The on-chip inductor is a symmetric center-tapped octagonal inductor with a patterned ground shield with a quality factor of 6. The high-speed buffer makes use of a level-shifted inverter M9 and M10 to operate in the common-mode range of the DCO with M11 acting as a pull-up transistor.

To achieve high output efficiency, a push-pull class AB amplifier is used at the output stage of the transmitter to drive the off-chip matching network and balun for

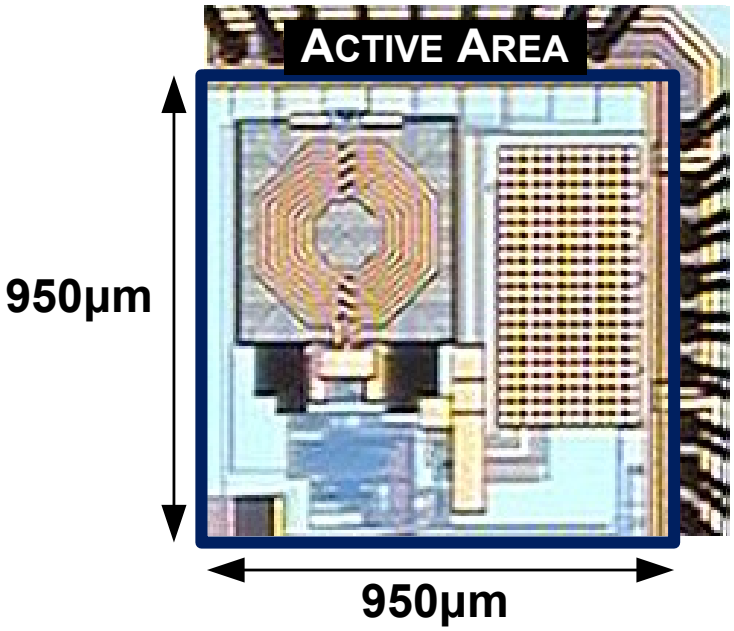


Figure 2.15: Die micrograph of the chip.

differential to single-ended conversion.

2.5 Measurement Results

The proposed transmitter is implemented in 0.18-µm CMOS process with a 1.8-V power supply. The chip micrograph is presented in Figure 2.15. The chip measures 950-µm by 950-µm, occupying an active area of 0.9-mm^2.

Figure 2.16 shows the measured frequency tuning characteristics of the DCO with respect to the digital code of the coarse capacitor array. Due to process variations, the frequency band has shifted upwards to span 428-MHz to 480-MHz. Despite the shift, the ISM band remains within the frequency tuning range of the DCO. The measured coarse and fine frequency steps of the DCO is 400-kHz and 140-kHz respectively, in the ISM band. The coarse and fine frequency steps measured were much larger than the designed parameters. The explanations for these deviations are summarized as follows :

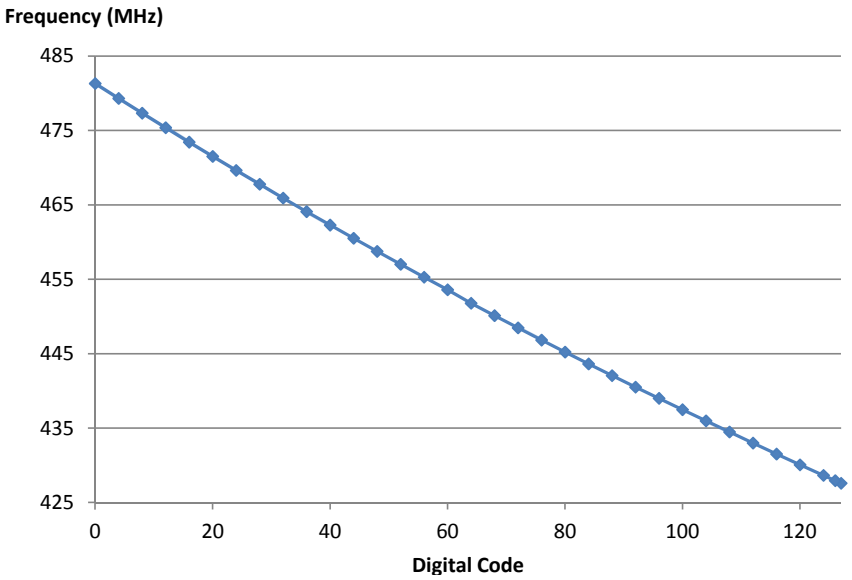


Figure 2.16: Measured DCO tuning characteristics.

1. To achieve a total tuning range of 44-MHz from 412-MHz to 456-MHz with a centre frequency of 433.92-MHz, the centre frequency and tuning range of the oscillator were both overdesigned. However, based on the measurement results, it seems the margin was overestimated and the tuning range measured was 52-MHz which is 20% larger than the desired tuning range. Similarly, as the frequency resolution is designed over a fixed number of bits, the frequency resolution is tied to the tuning range. Due to the fact that the tuning range is larger than expected, the frequency resolution is also larger than expected.

2. The tank capacitance uses two 5.5-pF capacitors or an equivalent capacitance of 11-pF. To achieve the required frequency resolution, the tuning capacitor array requires a unit capacitance in the order of 5-fF. However, the smallest unit MIM capacitor provided by the 0.18-um process was in the order of 50-fF. Therefore, a custom Metal-Insulator-Metal (MIM) capacitor with reduced dimensions from the minimum recommended capacitor size was used for the unit capacitor in the coarse capacitor array. However, that was still insufficient

to achieve the required resolution for the fine capacitor array. Therefore two unit capacitors were connected in series to halve the effective capacitance. Based on the measurement results, it seems that the effective capacitance was larger than expected value, further increasing the fine frequency resolution.

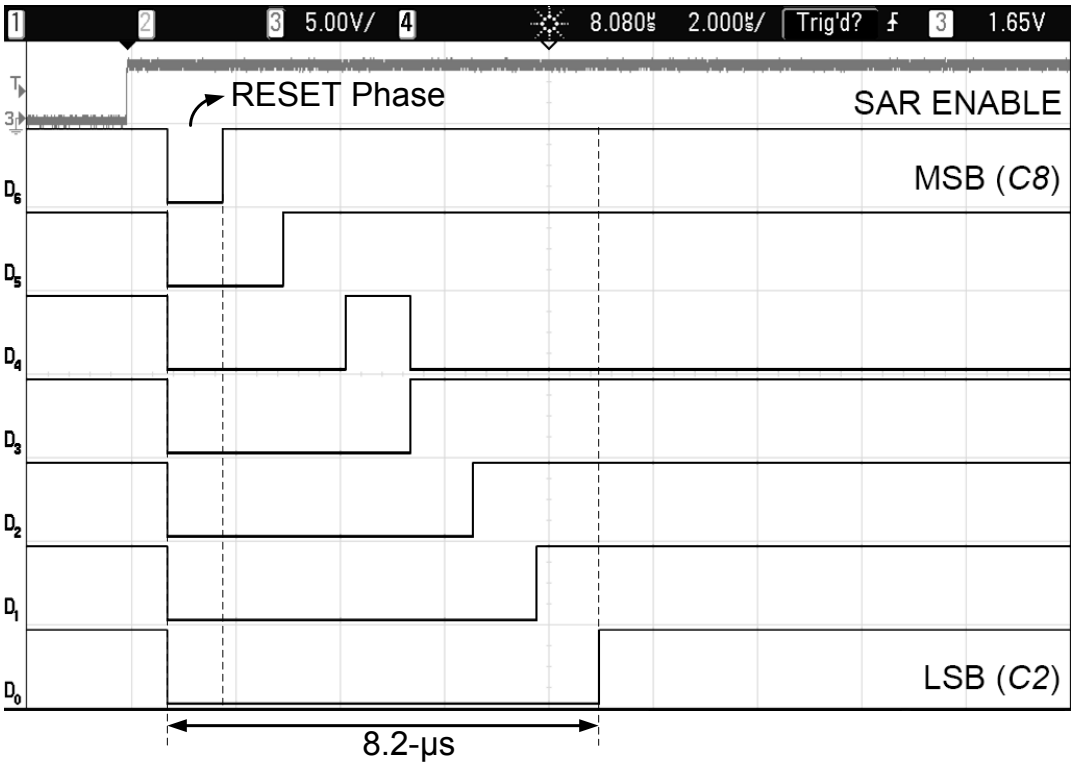


Figure 2.17: Digital code for DCO array during SAR calibration operation.

Figure 2.17 illustrates the measured digital code of the coarse capacitor array during the SAR calibration process on a mixed-signal oscilloscope. After the rising edge of the SAR ENABLE signal, the digital output is reset on the next rising edge of the SAR CLK signal, pulling all signals to a low. The coarse calibration process then begins with setting each successive bit to high before switching it to the final result based on the comparison result. The digital code converges to a value of '1101111' which corresponds to a frequency of 434-MHz. The total coarse calibration time is 8.2-µs.

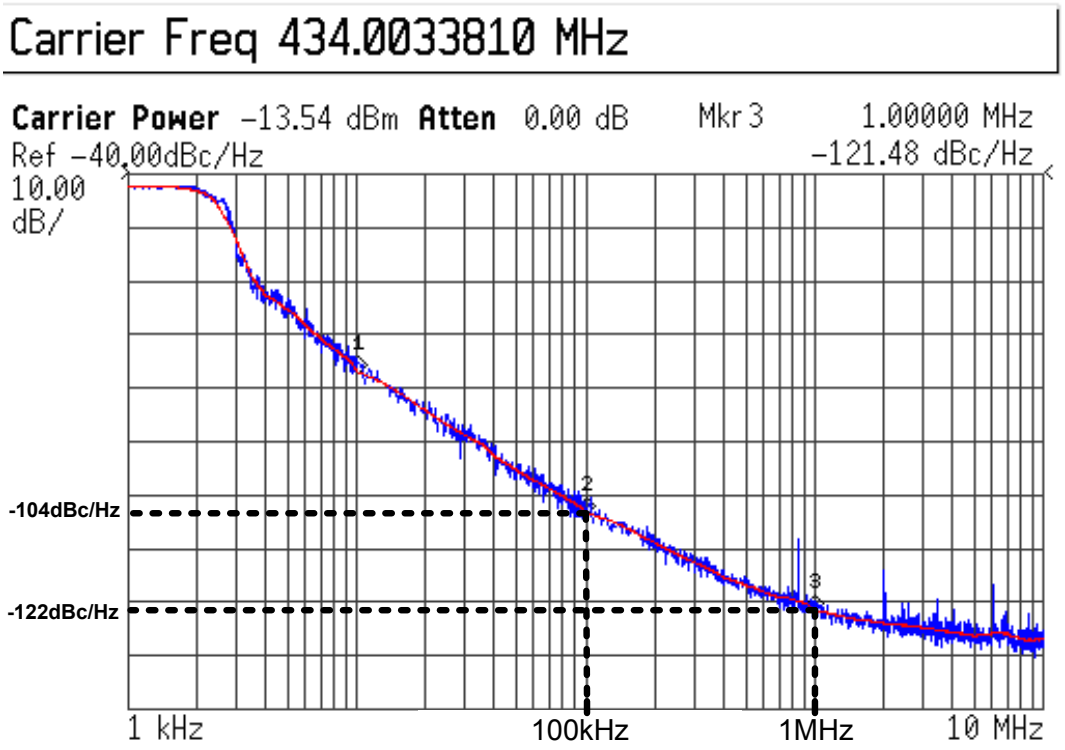


Figure 2.18: Measured phase noise of transmitter in all ON state.

The measured phase noise of the calibrated transmitter is shown in Figure 2.18. The measured phase noise is -100dBc/Hz and -118dBc/Hz at an offset of 100-kHz and 1-MHz respectively.

The maximum data rate for the OOK modulation is limited to the rise time of the DCO and PA. As demonstrated in Figure 2.19, the measured oscillator rise time is 200-ns. By rule-of-thumb, the bit period should not be less than 5 times the oscillator rise time, limiting the maximum data rate to 1-Mbps. The modulated OOK spectrum using a pseudo-random binary sequence of 65536 bits at 1-Mbps is shown in Figure 2.20. The modulated spectrum occupies a 20-dB emission bandwidth of 0.97-MHz at 1-Mbps, satisfying the bandwidth requirements of the ISM band. With a 50% OOK modulated input signal, the measured current consumption of the DCO is 1.7-mA at an output power of -13.5-dBm that satisfies FCC emission power limits.

As the calibration process is completed in a single conversion cycle, the power

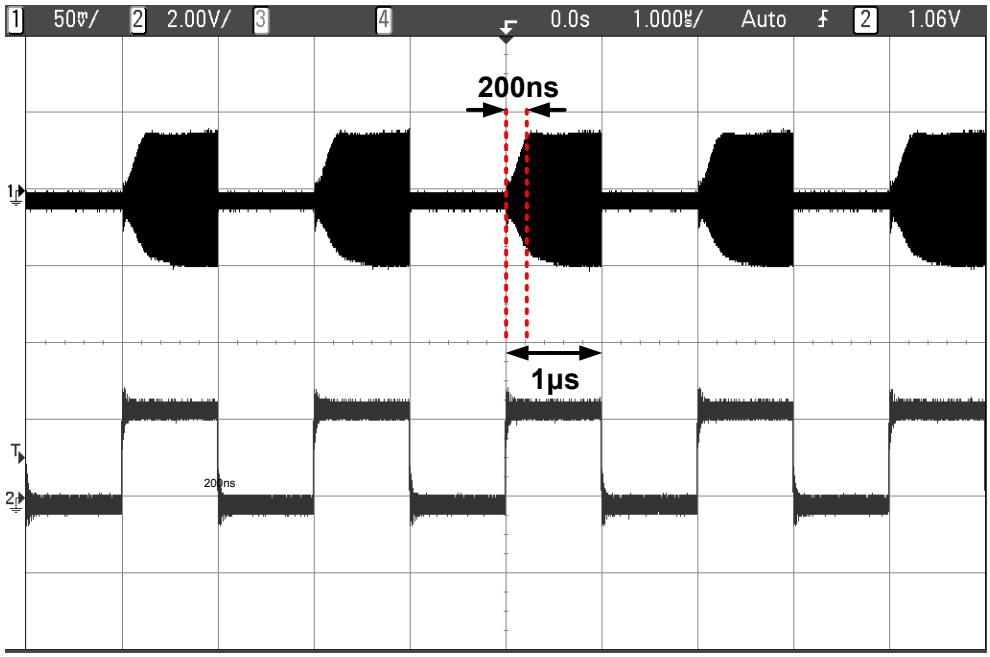


Figure 2.19: Measured output of transmitter in '1010' state.

consumption measured is not accurate and tends to be lower. Therefore, a conservative estimate of the current consumption is obtained from simulations. During the coarse calibration process, the digital and analog circuit blocks consume 280-µA and 800-µA respectively. Therefore, a single coarse calibration cycle is estimated to consume 16.6-nJ in energy. During the fine calibration process, the digital circuit blocks consume 340-µA. Therefore, a single fine calibration cycle of 10-µs is estimated to consume 6.1-nJ in energy.

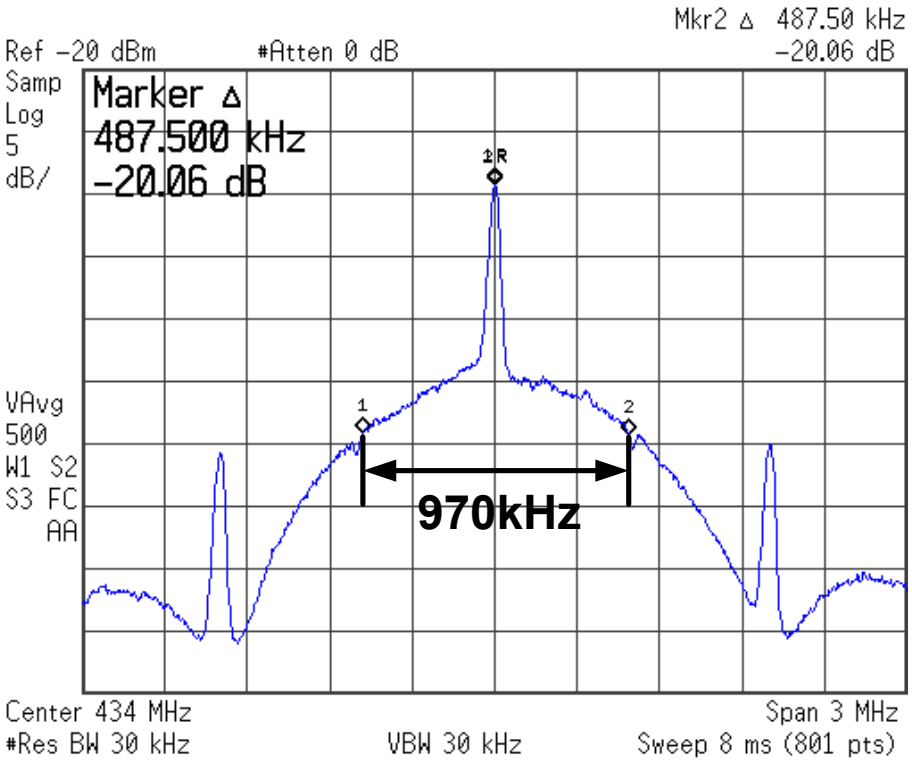


Figure 2.20: Measured output power spectrum of transmitter with pseudo random binary sequence input.

Table 2.1: Measured Chip Performance

Process	0.18-μm CMOS
Power Supply	1.8-V
SAR Calibration Time	<8.5-μs
TDC Calibration Time	<10-μs
Modulation Scheme	OOK
Maximum Data Rate	1-Mbps
PA Output Power	-13.5-dBm
FOM	3.1-nJ/bit
Current Consumption	
DCO	1.7-mA
SAR Calibration∗	16.6-nJ/Conversion Cycle
TDC Calibration∗	6.1-nJ/Conversion Cycle
Chip Core Area	0.95-μm × 0.95-μm

Table 2.2: Performance Comparison

	[19]	[20]	[14]	This Work
Process	90nm	65nm	180 nm	180 nm
Oscillator Architecture	LC	Ring	LC (Off-chip L)	LC
Tuning Range	319-415MHz	0.8GHz to 2GHz	864MHz-1.06GHz	420-480MHz, 480-600MHz
Tuning Resolution	14-bit	10-bit	-	8.5-bit
Frequency Resolution	$\leq$ 1.4kHz	-	-	$\leq$140-kHz
Calibration Architecture	Off-chip	TVC (R Trimming)	Counter	SAR & TDC
Calibration Time	-	250-600ns	36μs	8.5µs & 10µs
Transmitter Performance				
Data Rate	120kbps	-	1Mbps	1Mbps
Output Power	-	-	-2.9dBm	-13.5dBm
FOM	2.9nJ/bit	-	1.94nJ/bit	3.1nJ/bit

Table 2.1 summarizes the measured performance of the proposed design. The performance comparison with other designs for frequency calibration is as shown in Table 2.2. Although some other designs achieve much higher tuning resolutions and smaller frequency steps [19], they make use of off-chip equipment such as the spectrum analyzer to accurately measure the frequency. Zhang et. al [20] achieve calibration in less than 1-μs but require external resistor trimming to accurately define the reference. Compared with the counter based approach [14], the proposed calibration architecture is able to achieve higher resolution in a shorter amount of time.

The transmitter figure-of-merit is bigger compared to other due to the very low quality factor (<6) of the on-chip inductor and can be substantially reduced with an off-chip inductor or by implementation in a process with increased metallization layers.

2.6 Conclusion

A 433.92-MHz ISM band frequency calibrated transmitter is proposed. Based on the TVC technique, the SAR is adopted for coarse calibration while the cyclic vernier TDC technique is adopted for fine calibration. Achieving a frequency resolution of 140-kHz across the ISM band with a tuning range of 54-MHz, the calibration process only takes less than 18.5-μs. Implemented in 0.18-μm CMOS process, the OOK transmitter achieves a maximum data rate of 1-Mbps with -13.5-dBm output power while dissipating 1.7-mA from a 1.8-V power supply.

Chapter 3

2.4-GHz Transceiver Design for WSNs

Intended to fulfill the unique requirements of an energy-efficient scalable health-care system-on-chip (SoC) for WSNs / WBANs, custom PHY layer specifications and a custom transceiver architecture is proposed. The requirements of this transceiver are low cost, small size, low power consumption and energy efficiency. Cost is perhaps one of the most important design requirements. This indicates that the SoC should be a compact, fully integrated node using standard silicon CMOS process. Hence, the size of the integrated circuit and the number of off-chip components should be minimized.

3.1 Background

3.1.1 Physical Layer Specifications

3.1.1.1 Modulation

Owing to the growing market for WSNs, there has been extensive research on WSN/WBAN transceivers in recent years. In contrast to many high-performance systems, WSNs sensor networks have drastically reduced communication range and duty cycle, implying little need for optimal use of bandwidth. Therefore simple modulation schemes that trade off spectral efficiency for power efficiency is often used [4].

OOK and FSK modulation schemes are two commonly used modulation schemes due to their low complexity and low power consumption. OOK modulation employs simpler circuits and can potentially achieve better energy efficiency as the entire transmitter can be switched off when transmitting a '0'. The complexity and power consumption of OOK receivers can also potentially be greatly reduced as they effectively only need to detect the presence and absence of a carrier in the bit period. The FSK modulation scheme is more robust against interference and jamming when compared to OOK, but this comes at the cost of increased power consumption due to the presence of a constant carrier and increased complexity in the demodulation process.

3.1.1.2 Data Rate and Frequency

WSNs typically have a low average data rate, on the order of hundreds to thousands of bits per second. However, WBANs expect slightly higher data rates in the order of 10kbps and also a possibility of up to 10-Mbps in raw data rates in some applications [21].

Typically, low data rate radios have a strong correlation with low power consumption, due to simplified architectures and reduced bandwidths. However, this does not necessarily indicate energy efficiency. A key metric for measuring the energy efficiency of wireless transceivers is energy per bit, representing the amount of energy required by a transceiver to transmit or receive a single bit of data. To maximize energy efficiency, this ratio should be minimized. The energy per bit ratios tend to decrease with increasing data rate, particularly for wireless transmitters. Therefore, increased energy efficiency can be achieved by using Mbps data rates and duty cycling the transceiver rather than using kbps data rates. By using high duty cycling between active and standby modes, energy efficient operation can be achieved at a much lower average power level even though active mode power consumption is higher.

Hence, a data rate of up to 10-Mbps is proposed. Such a data rate allows for increased energy efficiency while not placing excessive demands on the transmitter. As summarized in Table 1.1, the 433.92-MHz frequency band has an emission bandwidth of 1.085-MHz which is insufficient for band compliance. Therefore, the frequency band of 2.4-GHz is selected.

3.1.1.3 Output Power and Sensitivity

Based on the guidelines in [21], a transmission range between two nodes in a WBAN network of at least 3 meters should be supported. Taking this into account, the link budget analysis can be used to finalize the target specifications of our transceiver for health applications. The receiver sensitivity could be computed using the Friis formula [22], where the received power at a distance from a transmitter varies inversely with the square of the distance as shown:

$$P_r = P_t G_t G_r \left(\frac{\lambda}{4\pi d} \right)^2 \tag{3.1}$$

where P_r and P_t represent the power received and transmitted, respectively, G_r and G_t represent the antenna gains, λ represents the wavelength of the transmission carrier and d represents the distance between the two antennae. As a conservative estimate, both antenna gains are assumed to be 1. The Friis free space equation assumes that the transmitter and receiver have a clear, unobstructed line of sight between each other. The ratio of the transmitted power to the received power represents the path loss, therefore by rearranging (3.1), the path loss for free space can be calculated to be 49.6-dB for a distance of 3 metres using (3.2).

$$\begin{aligned} \text{Path loss} &= 10log_{10}\left(\frac{P_t}{P_r}\right) \\ &= 10log_{10}\left(\frac{4\pi d}{\lambda}\right)^2 \\ &= 20log_{10}d\ (\text{km}) + 20log_{10}f\ (\text{MHz}) + 32.44\ (\text{dB}) \end{aligned} \tag{3.2}$$

However, in practical scenarios, there is additional path loss between the transmitter and receiver due to multipath propagation that causes fading. In addition, for nodes positioned on the human body there may be possible shadowing due to the human body or obstacles near the human body and postures of human body which further increases the path loss. For example, in the proposed channel models for WBAN, the modified path loss equation for operation at 2.4-GHz is as follows :

$$\text{Path loss} = 7.84log_{10}d\ (\text{mm}) + 34.1\ (\text{dB}) \tag{3.3}$$

where the scaling coefficients and constants of 7.84 and 34.1 respectively were parameters derived by a least square fitting to the measured average path loss over the frequency range in the setting of a hospital room [23]. Based on (3.3), the path loss for a distance of 1 to 3 metres will range from 57-dB to 61-dB.

Since the maximum output power allowable in the 2.4-GHz ISM band is -0.23-dBm, a design target of 0-dBm is chosen. Based on the path loss calculations

as above, a target receiver sensitivity of -65-dBm is selected.

3.1.1.4 Literature Review

To measure the energy efficiency of wireless transceivers, the FOM of energy per bit, denoted as FOM in (3.4), is commonly used. However, in transmitter characterization, this FOM does not take into account differences in output power. Therefore, for transmitter characterization, an alternative FOM_{TX} as proposed in [12] which normalizes for output power is adopted for the transmitter characterization. As the FOM also does not take into account differences in modulation efficiency, comparison should be restricted to OOK modulation transmitters.

$$\text{FOM}_{\text{TX}} = \frac{\text{DC Power}}{\text{Data Rate} \times \text{Output Power}} \, (nJ/bit.mW) \tag{3.4}$$

$$\text{FOM}_{\text{RX}} = \frac{\text{DC Power}}{\text{Data Rate}} \, (nJ/bit) \tag{3.5}$$

Similarly, for the characterization of the performance of receivers, the typical energy per bit FOM is insufficient for receiver characterization as it does not take into account sensitivity variation. However, due to the lack of alternative figure of merits, FOM as defined in (3.4) will be used for benchmarking.

However, despite these efforts in benchmarking the designs, it has to be borne in mind that no FOM can be fool proof when both the transmitter and receiver power consumption (energy efficiency) have to be considered together. This is because these FOMs are one-sided characterizations, which do not take the other transmitting or receiving end into account. For example, heavily duty-cycled transmitters with high data rates may yield better figure of merits in the transmitter. However, these high data rates make the receiver much more difficult to design with good sensitivity, due to the increased noise bandwidth.

Table 3.1: Table of comparison for recent OOK Transmitters

Parameter	[24]	[25]	[26]	[27]	[28]	[29]	[30]	[31]
Output Power (dBm)	-5	-14	0	-12.5	0	-23.2	-20	-12.5
Power Consumption (mW)	55	3	2.3	0.44	4.86	7.93	0.191	0.38
Voltage Supply (V)	2.5	1.5	1	0.7	1.8	2.5	0.8	1
Bit Rate (Mb/s)	100	136	10	1	4	1	5	5
FOM_{TX} (nJ/bit.mW)	0.16	0.55	0.23	7.82	1.22	1662	3.82	1.35
Technology (nm)	250	180	90	65	180	250	180	90
Frequency (GHz)	5.73	2.46	2.4	2.4	2.4	2.4	2.4	2.45
Year	2005	2010	2010	2012	2011	2007	2013	2014

Table 3.2: Table of comparison for recent OOK receivers.

Parameter	[32]	[33]	[34]	[35]	[36]	[37]	[38]
Sensitivity (dBm)	-100.5	-60	-81	-60	-67	-67	-90
Power Consumption (mW)	0.4	2.8	2.1	6.6	0.5	0.18	9.5
Voltage Supply (V)	1	1.2	1.2	1.2	1.2	0.7	1
Bit Rate (Mb/s)	0.005	1	11	1.2	5	1	1
FOM_{RX} (nJ/bit)	80	2.8	0.191	5.5	0.1	0.18	9.5
Technology (nm)	-	130	Discrete	130	90	65	130
Frequency (GHz)	1.9	2.4	2.4	5	2.4	2.4	2.2-2.488
Year	2005	2007	2007	2008	2010	2012	2014

Tables 3.1 and 3.2 show the comprehensive comparison of the recently published OOK transmitters and receivers at frequencies around 2.4-GHz. All of the works are for OOK transmission and detection and FOM_{TX} and FOM_{RX} will be used to benchmark our research work.

3.1.2 Specifications for Transmitter and Receiver

Table 3.3: Specifications of the Transceiver

Parameter	Symbol	Specification	Units
Modulation Scheme	-	OOK	-
CMOS Technology	-	65-nm	-
Frequency	f_0	2.4	GHz
Supply Voltage	V_{DD}	1.2	V
Transmitter			
Transmitter Output Power	P_O	0	dBm
Data Rate	DR	1-10	Mb/s
Normalized Energy Efficiency	FOM_{TX}	<0.2	nJ/bit.mW
Receiver			
Receiver Sensitivity	P_{MDS}	-65	dBm
Data Rate	DR	1-10	Mb/s
Energy Efficiency	FOM_{RX}	<0.2	nJ/bit

Table 3.3 summarizes the desired specifications of the transceiver. Adopting the OOK modulation scheme, the transmitter targets an output power P_O of 0-dBm in the 2.4-GHz frequency band at a data rate of 10-Mbps. The receiver targets a sensitivity level of -65-dBm. The specifications not only target a comparable FOM to the published work but also optimally distributes the DC power consumption at the transmitter and receiver.

3.2 Transmitter Design

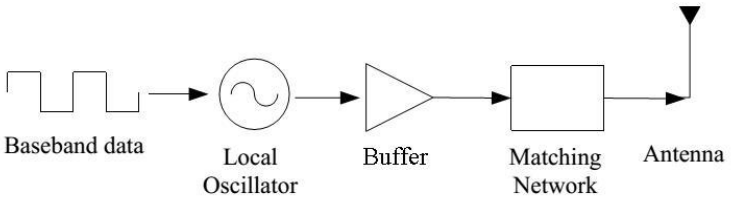


Figure 3.1: Block Diagram of the Direct Modulation Transmitter

An OOK transmitter can be implemented through the direct modulation transmitter architecture as shown in Figure 3.1. It consists of an oscillator and an output buffer that drives the 2.4-GHz carrier to the antenna through a matching network. In the direct modulation transmitter, the baseband data directly modulates the local oscillator and/or buffer. This eliminates the power hungry digital modulator, DACs, I/Q mixers and I/Q generation circuit in a typical direct conversion transmitter architecture and results in higher transmitter efficiency. In addition, when the input data is '0', the oscillator and buffer are both switched off and no DC power is consumed, further reducing the power consumption.

3.2.1 Architecture

To optimize the transmitter for energy-efficient operation, power consumption is of first and utmost consideration in the selection of oscillator and buffer topology. To achieve low phase noise, single transistor RF oscillator topologies may be preferred due to reduced noise sources. However, supply noise is gradually becoming a major contributor in sub-micron technologies due to reduced power supply voltages, a higher order of digital integration and an increased number of circuits on the same IC. The proposed transceiver is intended as the physical layer realization for an SoC including a front-end acquisition system and a MAC network controller. For

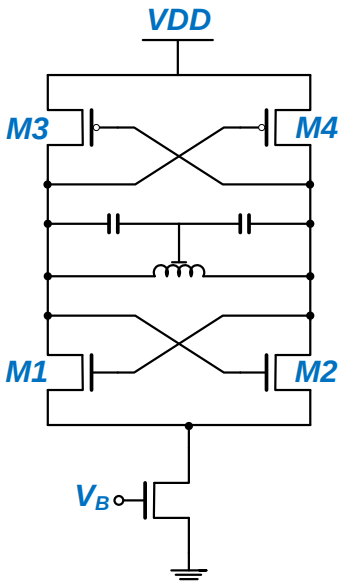
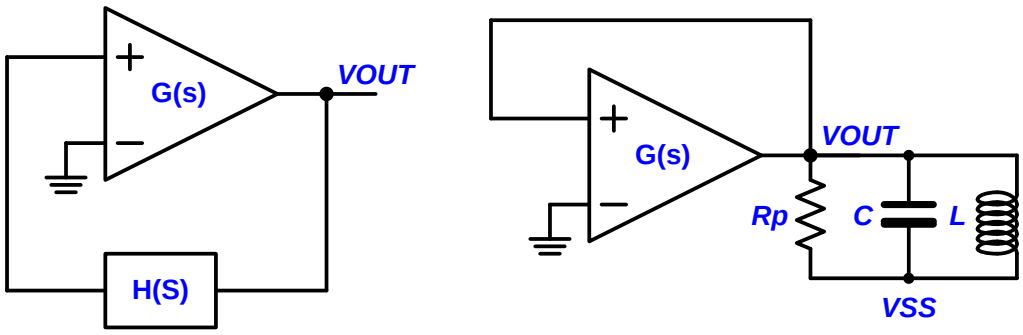


Figure 3.2: Circuit Diagram of complementary cross coupled LC oscillator.

integration with both digital and analog subsystems on a single chip, differential topologies that provide common-mode noise rejection is preferred.

The cross-coupled LC oscillator topology as shown in Figure 3.2 is selected in comparison with topologies utilizing only a single cross-coupled pair. The complementary cross-coupled VCO has two main advantages. First, with the additional transistor pair, the complementary topology offers higher transconductance to compensate for the loss of the tank. Due to the current reuse, less current consumption is required for the same transconductance. This topology is hence more power efficient. Second, by matching the PMOS and NMOS transistors, the complementary topology can provide better symmetry properties in the oscillating waveform, which decreases the upconversion of $1/f$ noise of devices to the $1/f^3$ phase noise region [18].

To provide compatibility with the rest of the sub-systems in the chip, a fixed voltage supply of 1.2-V is used. Therefore, to fix the bias current of the VCO



(a) Feedback Loop Model. (b) Transconductance Model.

Figure 3.3: Oscillator Feedback Loop Models.

such that it is independent of the supply voltage, a tail current transistor is used. This allows optimum control of power consumption versus the output swing of the oscillator. Even though a PMOS tail transistor has lower flicker noise contribution than an NMOS transistor, the NMOS transistor occupies less headroom. As only the amplitude or energy level is detected in OOK modulation, phase noise is not a major consideration and a tail NMOS transistor with smaller area has been selected for use.

3.2.2 Circuit Design

3.2.2.1 Oscillator Design

All oscillators can be represented as a simple feedback network as shown in Figure 3.3a. In an ideal system, the Barkhausen criterion requires the gain around the feedback loop to equal unity and the total phase shift around the loop to equal zero (or some multiple of 360°) such that the input signal will be amplified and added back to the input in phase, resulting in self-sustained oscillations. An alternate way to describe the operation of oscillators involves the concept of negative resistance. Figure 3.3b shows a model of a simple negative resistance LC oscillator. In this figure the active device is a transconductance (G_M) amplifier connected in positive

feedback to an LC tank circuit where the resistance R_P is a lumped equivalent model of the non-idealities of the inductor and capacitor. It can be shown that the tank circuit sees a negative resistance of $-1/G_M$ looking back into the transconductor output. When the negative resistance cancels the equivalent parallel resistance of the tank circuit, the Barkhausen criterion is satisfied.

Each cross-coupled pair generates a negative resistance of $-2/g_m$ to the LC-tank, therefore, the total negative resistance provided by the two complementary cross-coupled pairs is given by

$$R_{COMP,PAIR} = R_{N,PAIR}//R_{P,PAIR} = \frac{-2}{g_{mN} + g_{mP}} \tag{3.6}$$

where g_{mN} and g_{mP} is the transconductance of a single NMOS and PMOS transistor respectively. In order for the circuit to oscillate, the magnitude of this negative resistance must be smaller than the equivalent parallel resistance, R_P, of the tank circuit by a certain ratio, α as shown below:

$$\frac{R_P}{R_{COMP,PAIR}} = \alpha$$

This ratio is a safety factor that gives the design some margin so that oscillation is guaranteed, even when PVT is considered.

3.2.2.2 Custom Inductor Design

As can be seen from the previous section, the minimum transconductance and current required in the oscillator is primarily dominated by the losses in the tank, R_P. Therefore, it is essential to design and optimize the tank with minimal combined inductance and capacitance loss. This leads to maximum L/R and L/C ratios [39]. To maximize the L/R ratio, the quality factor of the on-chip inductor should be

maximized. However, this is highly limited by the available process layers in the given technology. To maximize the L/C ratio, the inductance value L should also be maximized, however, this leads to increasingly large areas. Therefore, a compromise between these various factors has to be achieved.

In the technology adopted, a proprietary inductor library with four different types of inductor topologies is provided. They are :

- Single and Differential Spiral Inductor
- Single and Differential Stacked Inductor
- Single and Differential Symmetric Inductor
- Differential Symmetric Inductor with Center Tap

The square stacked inductors achieve higher inductance for a much smaller area, but due to its tight windings, they possess low Q. The spiral and symmetric inductors have better Qs at the expense of much larger areas. As the architecture of the oscillator is differential, the tank can be considered to be made up of two equal inductors in series. Therefore, due to this differential structure, the Differential Symmetric Inductor with Center Tap is preferred.

The differential symmetric inductor effectively represents two individual spiral inductors connected in series. However, due to the nested structure where each inductor takes up effectively half the coil length, it occupies a much smaller area. In addition, due to its symmetrical structure between the two inductors, good symmetry is provided between the differential branches of the cross-coupled oscillator, reducing the non-linearities in the oscillating output. Through the use of a center tap, routing length and parasitic capacitance is reduced. The structure of the inductor is as shown in Figure 3.4.

Utilizing the OIF tool from the foundry, for a given inductance value, the minimum area or maximum quality factor at the desired operating frequency can be found. Using this tool, the maximum Q values at various inductances are found and

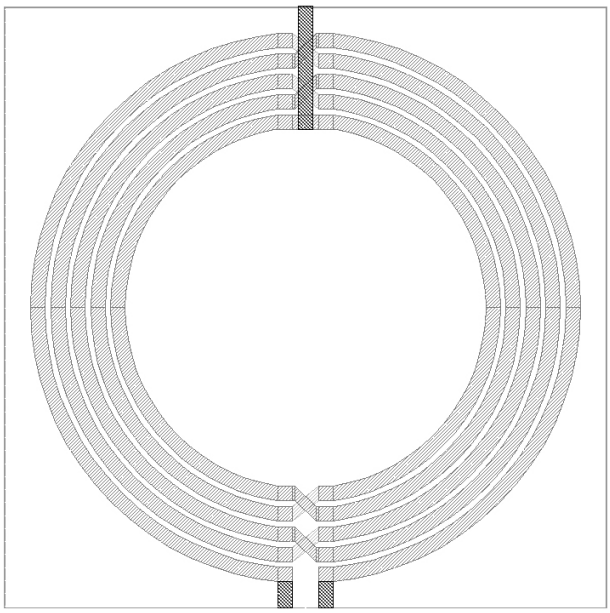


Figure 3.4: Layout of a differential symmetric inductor with center tap.

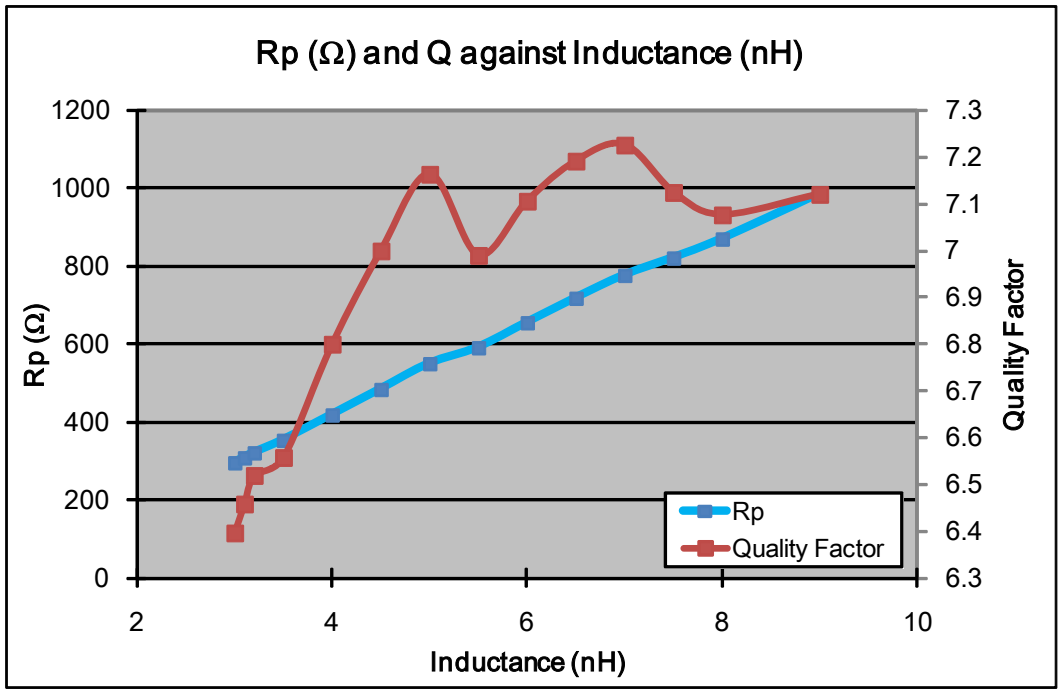


Figure 3.5: Rp and Q against Inductance at 2.4GHz.

plotted in Figure 3.5. It can be seen in Figure 3.5 that increasing the inductance value leads to small increases in quality factor, though this increase plateaus at quality factors above 7. Similarly, an increased inductance value will lead to a higher equivalent parallel resistance of the inductor, therefore lowering the required transconductance of the cross-coupled transistor pairs. In consequence, the required bias current and power are decreased. However, this leads to increasingly large areas. Based on these considerations, at a compromise between area, Q and R_P, an inductance value of 4.5-nH is selected. At 4.5-nH with an operating frequency of 2.4-GHz, the Q is 7 with a self-resonating frequency of 10-GHz, occupying an area of 255μm by 255μm.

Despite the optimized Q, it can be seen that the Q of the inductor is still below 10. To reduce inductor loss and improve the Q, the metallization layer with the lowest loss must be chosen for the inductor. To reduce eddy current losses in the substrate and to reduce the capacitive coupling to the substrate, this metallization layer should be as far as possible from the silicon substrate. The top metal available in this process is a low resistivity aluminum metal layer that is 32-kA thick. However, the metal used in the foundry provided inductors are all limited to METAL5, one layer below the top aluminium metal layer available. Therefore, to achieve an inductor with a higher Q, a custom inductor utilizing the top aluminum metal layer is designed.

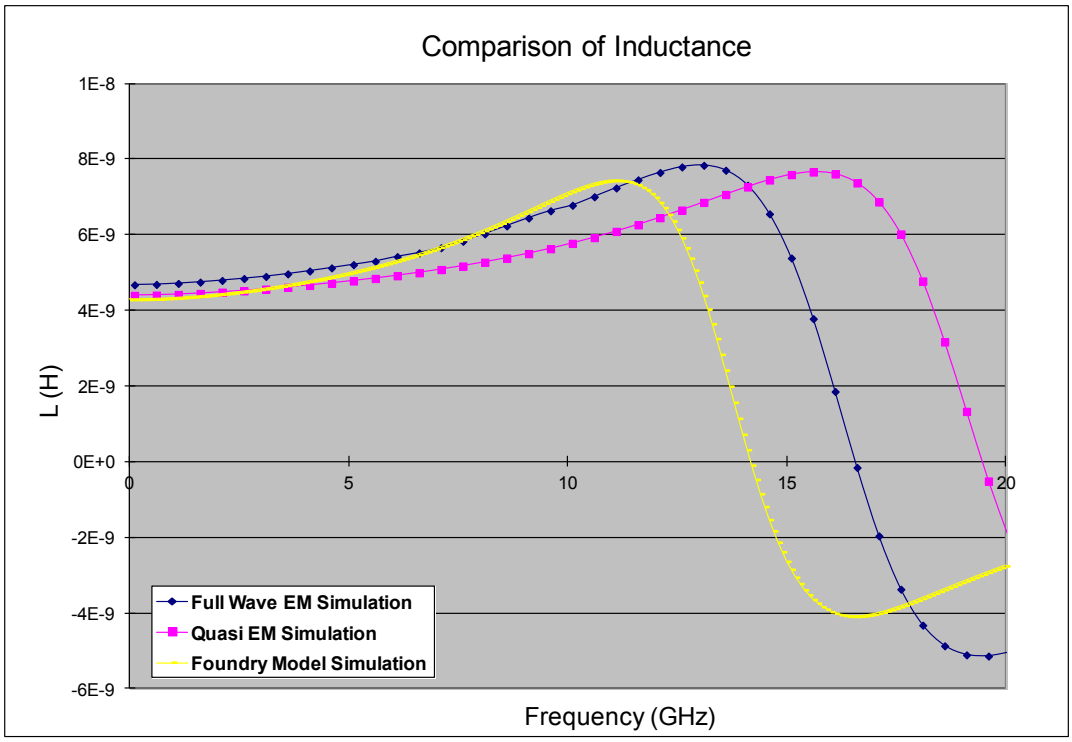
To design the custom inductor, the Virtuoso Passive Component Modeler (VPCM) program from Cadence is used. Allowing the synthesis and verification of inductors, the VPCM tool includes three different synthesis algorithms, 1) Full Wave Electromagnetic (EM) solution, 2) Quasi Static EM Solution and 3) Scalable Equivalent Circuits. The Quasi-Static EM Solver provides the best performance with reasonable accuracy, while the Full Wave EM Solver provides the best accuracy. The inputs to the synthesis module are the inductor design targets, including L, Q, SRF

(Self-Resonant Frequency), area and operating frequency. The inductor geometry parameters that can be optimized include track width, track space, track turn and radius.

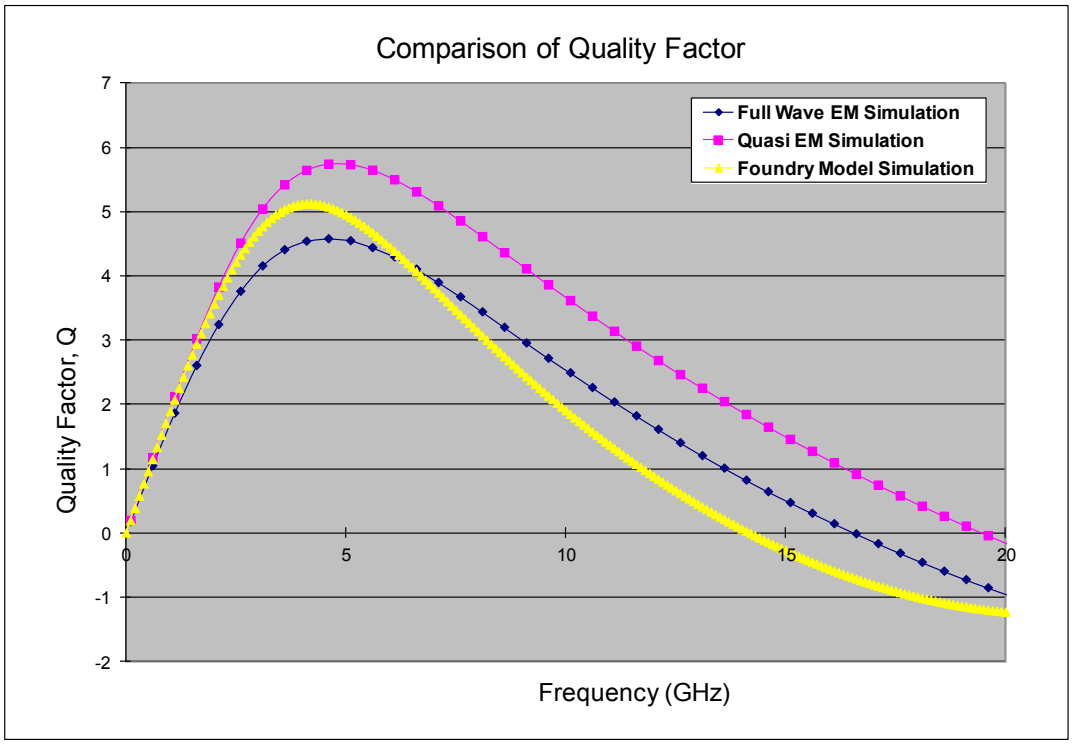
To evaluate the accuracy of the synthesis algorithms provided by VPCM, the L and Q of the VPCM generated models are evaluated against the provided foundry models. The L and Q simulation values are plotted in Figure 3.6a and Figure 3.6b, respectively, for an inductor of 4.5-nH to be operated at 2.4-GHz. As can be seen in Figure 3.6a, at frequencies above 5-GHz, the synthesis algorithms provided by VPCM start to deviate from the foundry model with big differences in the self-resonance values. Similarly for Q, there are clearly discrepancies between the various models. However, despite these discrepancies, it can be seen that the VPCM quasi-static EM model presents close agreement with the foundry model in the frequency band of interest (2.4-GHz).

Table 3.4: Parameters of Custom Inductor

Performance Metrics	
Operating Frequency	2.4-GHz
Inductance	4.40555-nH
Quality Factor	19.4039
Self Resonance Frequency	4.60815-GHz
Structure and Dimensions	
Type	Differential Center-Tapped Symmetric
Winding Width	8.9-μm
Winding Space	2-μm
Winding Turns	5
Winding Radius	89.8-μm
Maximum Size	284.6-μm

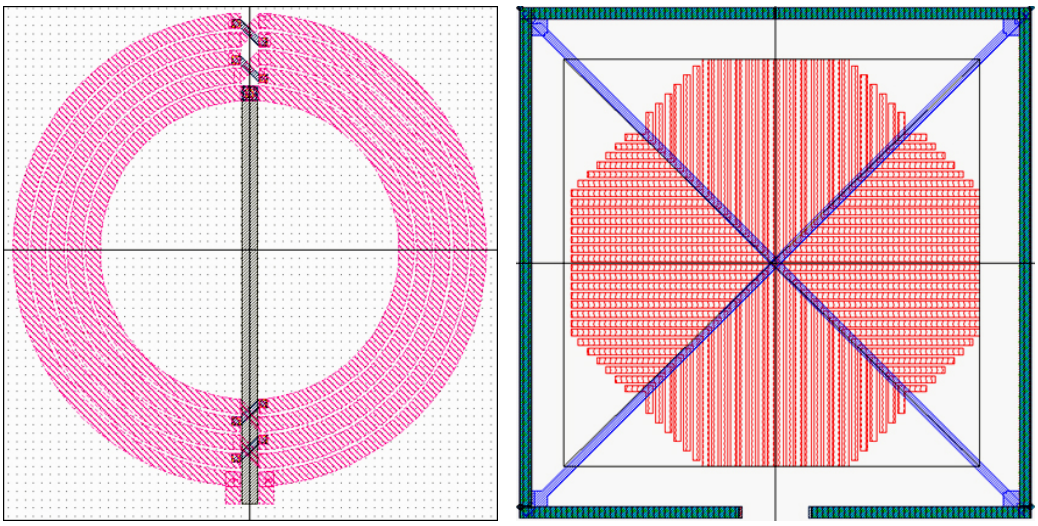


(a) Simulated Inductance Values using VPCM and Foundry models.



(b) Simulated Quality Factors using VPCM and Foundry models.

Figure 3.6: Comparison between VPCM and Foundry models.



(a) Inductor layout. (b) Patterned ground shield layout.

Figure 3.7: Layout of Custom Center-Tapped Symmetric Inductor.

Using the Quasi Static EM solver, the custom designed center-tapped symmetric inductor is as shown in Figure 3.7 and the inductor's parameters are summarized in Table 3.4. To decouple the inductors characteristics from substrate variation and to further enhance the Q of the inductor by isolating the inductor from the substrate and thus reducing the substrate parasitics [40], a patterned ground shield is used as demonstrated in Fig 3.7b. Similar to above, a characterization of the inductor is conducted to decide on an optimum balance between inductance, quality factor and R_P . The custom inductor has an inductance value of 4.4-nH and a Q of 19.4 which is a 280% improvement over the foundry provided inductor. Including the patterned ground shield, the inductor occupies a total area of 390µm by 390µm.

3.2.2.3 Output Buffer

The output buffer needs to deliver an output power of around 0-dBm to the antenna, whose impedance is 50Ω. The main considerations for the buffer design are its efficiency and low voltage operation. In OOK modulation and during the

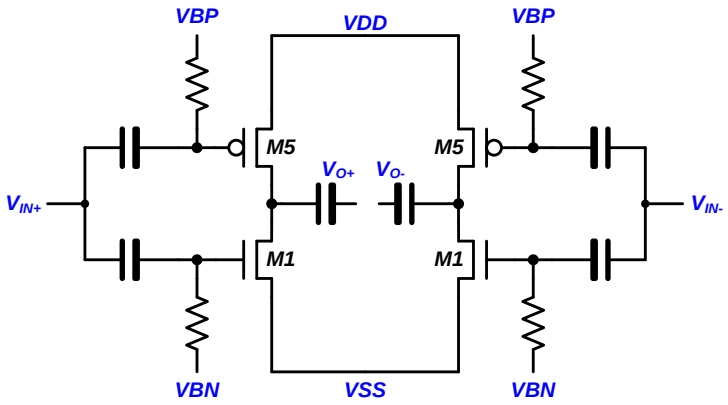


Figure 3.8: Schematic of Buffer Circuit

transmission of a '1', the carrier amplitude is largely constant for the duration of the bit period. This constant carrier amplitude means that more efficient nonlinear power amplification can be used and thus the linearity of the buffer is not a concern. In situations where there is pulse shaping at the baseband, a linear PA would be preferred to preserve envelope or amplitude information [41]. In a non-linear PA, as it is operated largely in the saturation region with large gain, the rise time may be slightly improved with a non-linear PA [42]. However, there may be weak harmonic components at $3f_O$ and $5f_O$ that are generated by the non-linearities in the PA. As these components tend to get attenuated by the band-pass nature of the matching networks, baluns and antennas, they are tolerable as long as they are below the regulatory limits.

To provide an output power of 0-dBm to the antenna, the peak-to-peak differential voltage swing will need to be approximately 630-mV with an output impedance of 50-ohms. At 2.4-GHz, a tuned power amplifier with inductor loading would potentially provide greater gain and better matching. However, due to area limitations, the buffer is restricted to an un-tuned amplifier topology.

Figure 3.8 illustrates the buffer circuit topology selected. The inverter-type buffer

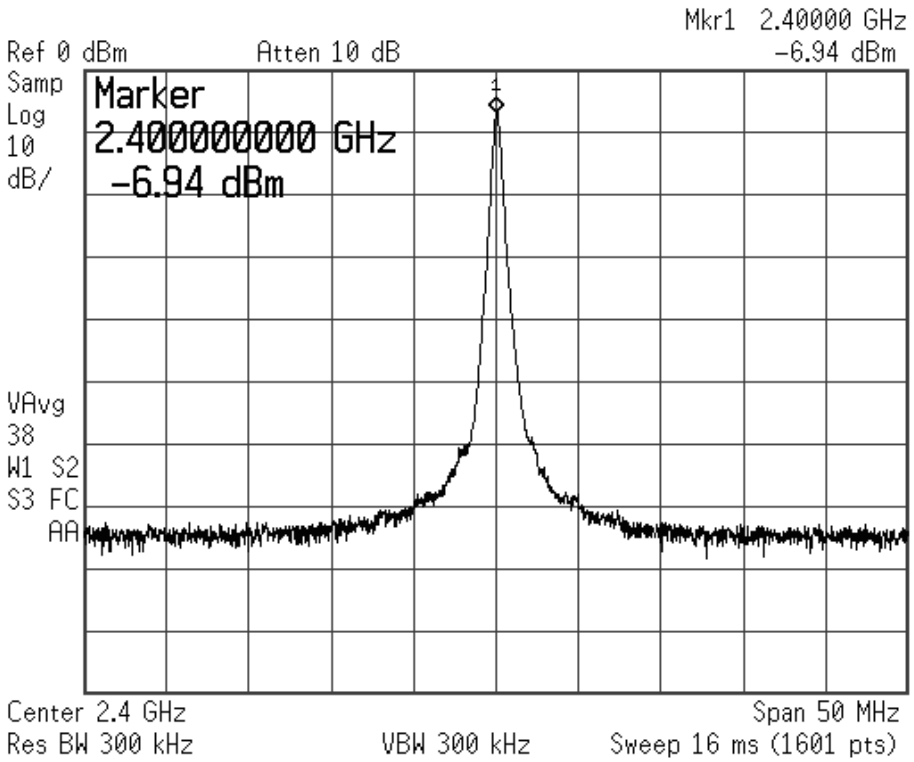


Figure 3.9: Frequency spectrum of carrier with all '1' input.

utilizes current-reuse between the NMOS and PMOS transistors to improve power efficiency. In addition, it is controlled through the baseband data such that during a '0' bit, the biasing current is switched off. Since the output of the VCO is AC-coupled with DC blocking capacitors, the buffer ideally does not consume any power during the transmission of a '0'.

3.2.3 Measurement Results

The proposed OOK transmitter is fabricated in a 1-Poly, 7-Metal 65-nm CMOS process at UMC. It is operated under a nominal supply voltage of 1.2-V. The transmitter occupies an area of 490-µm by 390-µm. The chip was bonded in a commercial QFN40 package and tested.

Figure 3.9 shows the single-ended carrier measured in a 50-MHz span with a resolution bandwidth of 300-kHz. The noise within this span is 70-dB lower than

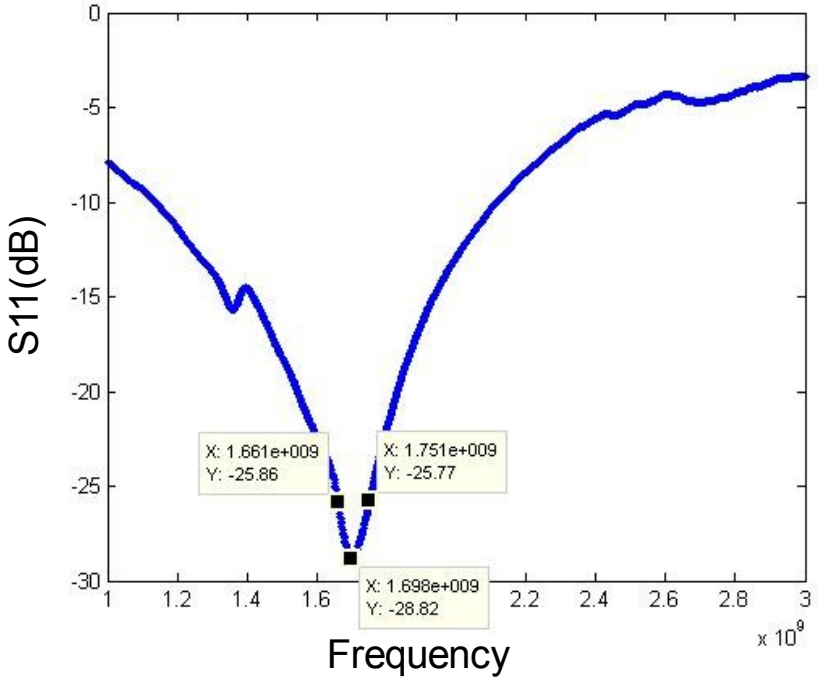


Figure 3.10: S_{11} at transmitter output with all '0' input.

the carrier.

As mentioned in section 3.2.2.3, the designed unloaded Q of the on-chip custom inductor is 19.4. Due to insufficient area and package pins, the LC oscillator was not individually fabricated. Therefore, the measurement of the actual Q cannot be found directly. However, a rough estimate of the loaded Q can be found by measuring the reflection coefficient at the output of the transmitter when the DATA input is '0'. By disabling the oscillator and the buffer, the transistors are effectively switched off. The reflection coefficient S_{11} at the output of the transmitter provides an approximation to the impedance of the tank. The measured S_{11} is as shown in Figure 3.10 and the loaded Q of the on-chip inductor can be found by using the formula, $Q = \frac{f_C}{\Delta f_C}$, where f_C is the frequency at the point of lowest reflection and Δf_C is the 3-dB bandwidth from f_C. The Q from the S_{11} measurement is 19 which agrees closely to the designed value.

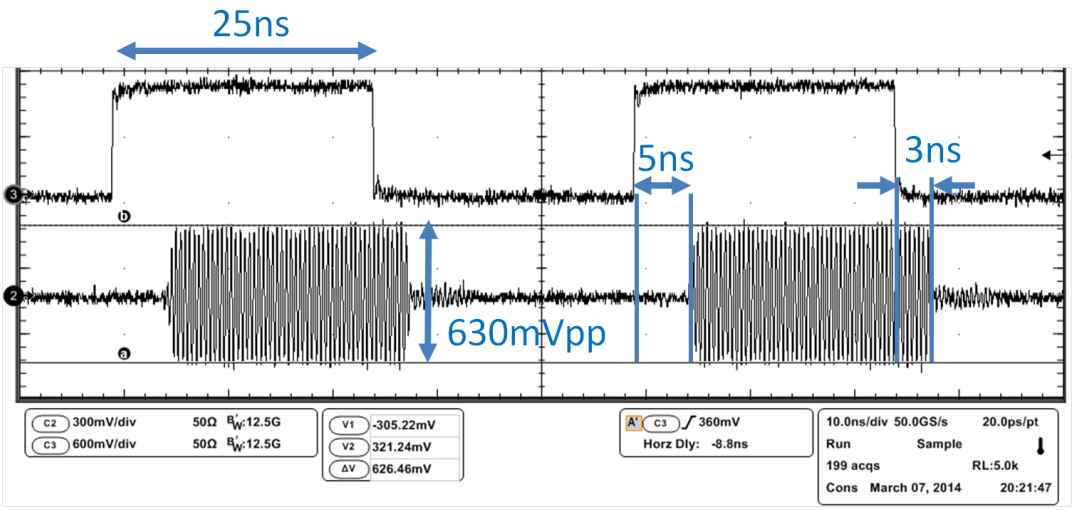
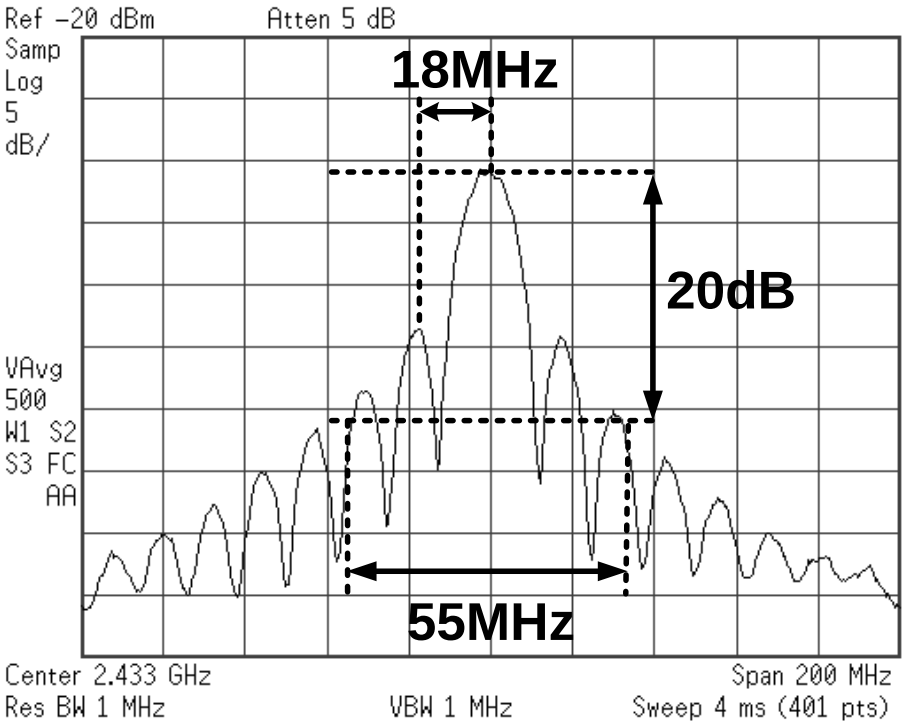


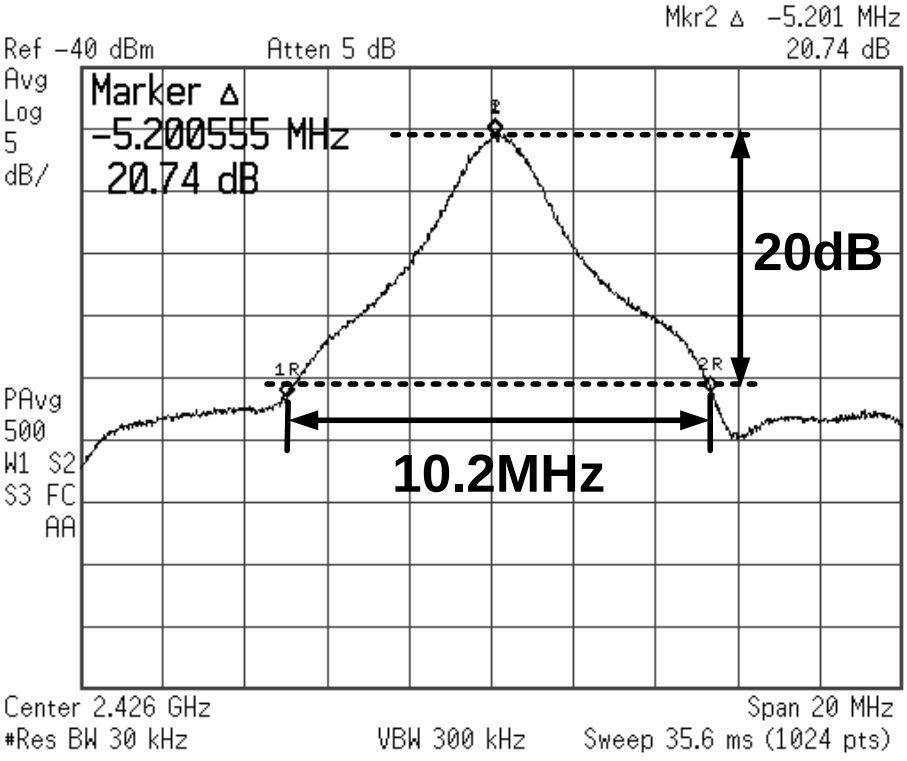
Figure 3.11: Modulated transmitter output with '1010' input.

The minimum bias current to start up oscillation was also evaluated to obtain an approximation for the quality factor of the fabricated inductor. The minimum current to start up oscillations is approximately 7.5-μA compared with 6-μA in schematic simulations. Assuming that the start-up current is inversely and linearly proportional to the Q of the inductor, it can be approximated that the measured Q is 15.5.

The performance during data transmission is first tested by applying a '1010' pattern to the transmitter. The oscilloscope screenshot of the modulated transmitter transient is shown in Figure 3.11. As can be seen, the differential output of the transmitter rises to a peak-to-peak voltage of approximately 630-mV, corresponding to an output power of 0-dBm. This is approximately close to the maximum power that can be transmitted in the 2.4-GHz ISM band under the FCC regulations. To show the rise time and fall time clearly within the span of the oscilloscope, a bit period of 25-ns was used. As can be seen, the transmitter requires a rise time of 5-ns and a fall time of 3-ns. Applying a general rule of thumb which specifies the minimum bit period to be at least 5 times the sum of the rise and fall time, the transmitter satisfies the bit period requirements of a data rate of 10-Mbps.



(a) '1010' Data Input.



(b) PRBS Data Input.

Figure 3.12: Modulated transmitter output spectrum.

The transmitter output spectrum at 10-Mbps with an input pattern of '1010' is shown in Figure 3.12a. Theoretically, based on the spectrum of an ideal square wave, the first lobe is at 1.5 times the data rate away while the 20-dB emission bandwidth is approximately 7 times the data rate. From the measurements, it can be seen that the first lobe is at 18-MHz which is close to the theoretical 15-MHz while the measured 20-dB emission bandwidth is 55-MHz. The slight increase in measured values may be due to phase noise from the oscillator which adds power to the sidelobes. In addition, OOK modulation pulls the VCO slightly which may create transient frequency components that show up during the measurements.

To better approximate the behaviour of true random data in a practical scenario, a pseudo-random binary sequence (PRBS) is applied to the transmitter. The modulated OOK spectrum using a pseudo-random binary sequence of 65536 bits at 5-Mbps is as shown in Figure 3.12b. The modulated spectrum occupies a 20-dB emission bandwidth of 10.2-MHz, satisfying the 12-MHz emission bandwidth requirement of the FCC regulations. Data rates above 5-Mbps may require data shaping to achieve compliance with the emission bandwidth requirements.

While transmitting an output power of 0-dBm at 10-Mbps, the transmitter consumes a current of only 0.8-mA. This is because both the oscillator and buffer are switched off during the transmission of a '0' bit, reducing power consumption. In addition, at such high data rates, with the duration of a bit period reducing to just 100-ns at 10-Mbps, the amount of time in which static DC current is consumed at steady state oscillations is greatly reduced. Even though it is usually assumed that the power consumption during 50% OOK modulation is half of the power consumption when the transmitter is fully switched on, the measurements suggest that greater savings are observed at much higher data rates. This is illustrated in Figure 3.13. At low data rates, current consumption approximates half the DC current consumption

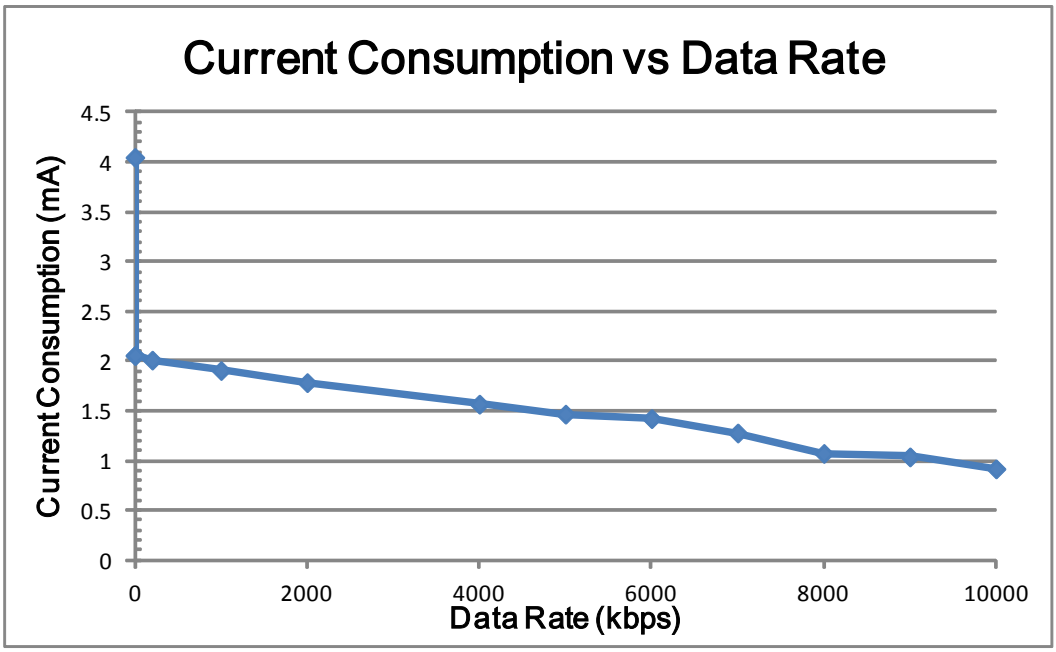


Figure 3.13: Current consumption against data rate.

when the transmitter is transmitting all '1's, equivalent to an OOK data rate of zero. At higher data rates, current savings of up to 75% is observed.

Therefore, as a measure of its energy efficiency, the FOM_{TX} (normalized energy efficiency) is calculated to be 0.1nJ/bit.mW which is better than recent works. The overall power efficiency of the transmitter is also measured and shown in Figure 3.14. The transmitter achieves a best efficiency of 23% at a differential output power of 0-dBm.

Table 3.5 summarizes the measured results and the transmitter has achieved its target performance specifications.

Table 3.6 presents the performance comparison with recently published state-of-the-art 2.4-GHz OOK transmitters. The proposed transmitter performs favourably compared with the others and offers the best FOM_{TX}. Although [24] shows a comparable FOM_{TX}, it operates at 100-Mbps. Such a high data rate degrades the noise bandwidth, making it difficult to design a low power receiver

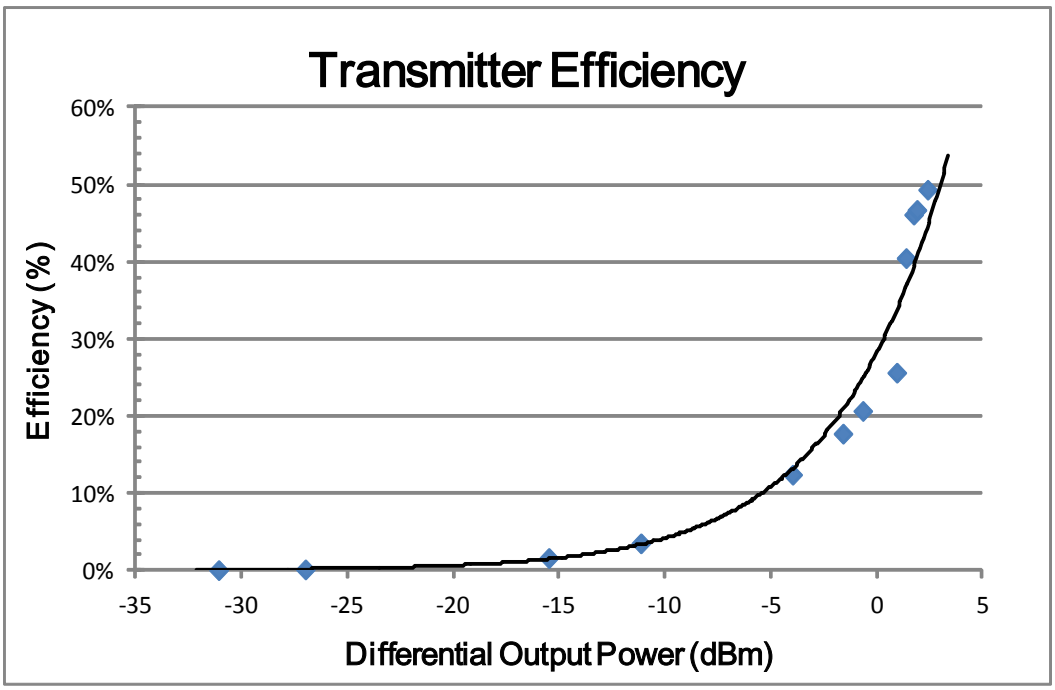


Figure 3.14: Measured transmitter efficiency.

Table 3.5: Performance Summary of 2.4-GHz Transmitter

Parameter	Symbol	Specification	Units
Modulation Scheme	-	OOK	-
CMOS Technology	-	65	nm
Frequency	f_0	2.4	GHz
Supply Voltage	V_{DD}	1.2	V
Transmitter Single-Ended Output Power	P_O	0	dBm
Transmitter DC Power Consumption	P_{DC}	0.96	mW
Data Rate	DR	$<$10	Mb/s
Normalized Energy Efficiency	FOM_{TX}	0.1	nJ/bit.mW

with reasonable sensitivity.

Table 3.6: Table of comparison with recent OOK Transmitters

Parameter	[24]	[25]	[26]	[27]	[28]	[29]	[30]	[31]	This Work
Output Power (dBm)	-5	-14	0	-12.5	0	-23.217	-20	-12.5	0
Power Consumption (mW)	5	3	2.3	0.44	4.86	7.925	0.191	0.38	0.96
Voltage Supply (V)	2.5	1.5	1	0.7	1.8	2.5	0.8	1	1.2
Bit Rate (Mb/s)	100	136	10	1	4	1	5	5	10
FOM_{TX} (nJ/bit)	0.05	0.02	0.23	0.44	1.22	7.9	0.04	0.08	0.1
FOM_{TX} (nJ/bit.mW)	0.16	0.55	0.23	7.82	1.22	1662.26	3.82	1.35	0.1
Technology (nm)	250	180	90	65	180	250	180	90	65
Frequency (GHz)	5.73	2.46	2.4	2.4	2.4	2.4	2.4	2.45	2.4
Year	2005	2010	2010	2012	2011	2007	2013	2014	2013

3.2.4 Conclusion

In this section, a low power proprietary OOK transmitter that is able to support data rates up to 10-Mbps is described. The energy efficiency of the transmitter is enhanced significantly at high data rates and the transmitter achieves performance better than recently published OOK transmitters. Fulfilling the regulations of the FCC and ETSI, the transmitter satisfies the emission spectrum mask limits for transmission in the 2.4-GHz ISM band with a PSRB data input of up to 5-Mbps.

3.3 Receiver Design

As OOK receivers only need to detect the presence and absence of a carrier in the bit period, the architecture of the receiver can be greatly simplified. With baseband information modulated on its amplitude rather than its phase or frequency, there is no need to extract either the phase or frequency information. This avoids the use of frequency conversion blocks such as phase-locked loops (PLL), mixers and oscillators which reduces power consumption and saves area. Since only the envelope information needs to be recovered, they are therefore also generally non-coherent. Amongst the various architectures, the envelope detection and super-regenerative architectures are two commonly used architectures for their simplicity, low power consumption and small area. In this section, an envelope detection receiver achieving a FOM_{RX} of 0.7-nJ/bit at 5-Mbps and a super-regenerative receiver achieving a FOM_{RX} of 0.16nJ/bit at 10-Mbps is presented.

3.3.1 Envelope Detection Receiver

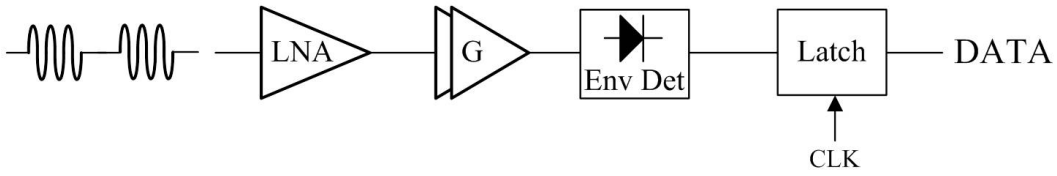


Figure 3.15: Block Diagram of generic envelope detection receiver.

To achieve low power consumption, wideband non-linear envelope detectors as shown in Figure 3.15 are a popular choice as they do not need a local oscillator. In such architectures, the incoming OOK signal is amplified at the received RF frequency. Once the signal reaches a sufficient magnitude, a non-linear squarer or

envelope detector is employed to preserve the base band information in the envelope. To provide compatibility to the baseband block, the information can be further converted to an equivalent digital signal.

3.3.1.1 Noise Analysis

Based on the output power provided by the transmitter and the required transmission range, the target sensitivity of the OOK receiver is defined in Section 3.1.2 to be -65-dBm. This can also be expressed as the minimum detectable signal that the receiver must be able to recover.

However, since channel noise and circuit noise is always present in all communications systems, the required noise performance of the communication link and transceiver can be quantified using the link budget. The link budget can be used to estimate the required signal-to-noise ratio (SNR) and noise figure (NF) of the receiver such the signal can be recovered with sufficient accuracy by the receiver.

The link budget is expressed as :

$$P_{RX,MIN} = 10log_{10}(kT) + 10log_{10}(BW) + SNR_{MIN} + NF \tag{3.7}$$

where $P_{RX,MIN}$ (in dBm) is the minimum signal power that should be accurately recovered by the receiver or the required sensitivity. The first term $10log_{10}(kT)$ is the effective noise power available in 1-Hz bandwidth at a system temperature of 290K and is equivalent to -174-dBm, which is also the white noise level. BW represents the input noise bandwidth of the receiver in units of Hz, which can be approximated to be twice the data rate. The SNR_{MIN} represents the minimum SNR required at the output of the receiver, and NF represents the noise figure of the receiver.

The minimum required SNR of the non-coherent OOK modulation scheme is dependent on the required level of reliability of the receiver as well as the the ratio

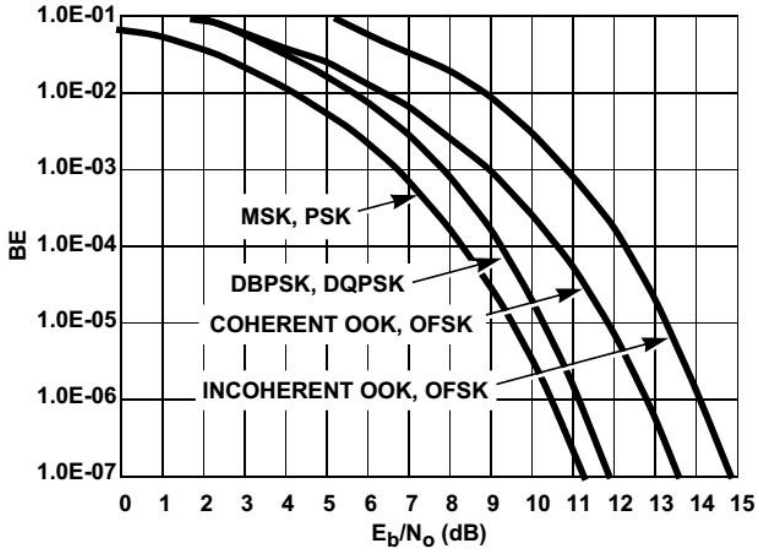


Figure 3.16: Probability of bit error for common modulation methods [2].

of energy per bit (E_b) to the spectral noise density (N_o) [43]. Figure 3.16 graphs the E_b/N_o for varying levels of BER. For the OOK modulated signal at a bit error rate of 10^{-3}, the ratio of energy per bit to spectral noise density(E_b/N_o) is approximately 11dB. Using the ratio of 11-dB, the required signal-to-noise ratio (SNR) can be calculated with the following equation:

$$SNR = \frac{E_b}{N_o}\frac{R}{BW} \tag{3.8}$$

where R represents the data rate and BW represents the bandwidth of the signal.

Since the bandwidth of an OOK signal can be approximated to be twice the data rate, $R/BW = 0.5$ and this gives an SNR of 8-dB. With all the parameters available, the maximum NF of the receiver can be calculated using (3.7) to be 30-dB.

The overall noise figure of receivers are often estimated using the Friis formula for noise figure which expresses the total noise factor (F) of a series of cascaded devices as a function of the noise factor and gain of each device. The noise contributed by the first amplification block has the most significant effect on the

total overall noise figure. However, gambini et. al suggests this analysis cannot be directly applied to an envelope detection receiver. This is due to the non-linear signal gain of the envelope detector and the noise downconversion by intermodulation with the incoming signal and by self mixing, and the DC noise leakage to the output [44].

Due to the nonlinear operation of envelope detectors, it is difficult to analyze the noise transformation in the envelope detector and predict the sensitivity of the receiver accurately. However, since the gain of the envelope detector is input-dependent, a decrease in input signal amplitudes lead to decreasing envelope detector gain. Therefore, the most efficient means to improve the sensitivity of such receivers is to increase the amount of gain preceding the envelope detector [44]. These results were similarly augmented in [45], where simulation results indicate that greater payoffs in sensitivity can be achieved by increasing gain in the front-end amplifier of an envelope detection receiver, even if the increase in gain results in degraded front-end noise performance.

Therefore, based on envelope detection to utilize the benefits of the OOK modulation scheme, the proposed receiver architecture is as shown in Figure 3.15. With an expected input of -65-dBm, the equivalent peak voltage into the receiver is 175-μV. As a conservative estimate, the envelope detector can be approximated to have a low conversion gain of 0.1 for an input with a peak voltage of 20-mV as the input voltage is small [45]. Therefore, to achieve an input of at least 5-mV to the comparator would require a peak input of approximately 50-mV to the envelope detector, necessitating a gain of 50-dB from the gain blocks. However, due to expected losses in the input matching network from the antenna, process variations and to provide a degree of design margin, a target gain of 60-dB is set for this design with a front-end noise figure of $<$5-dB.

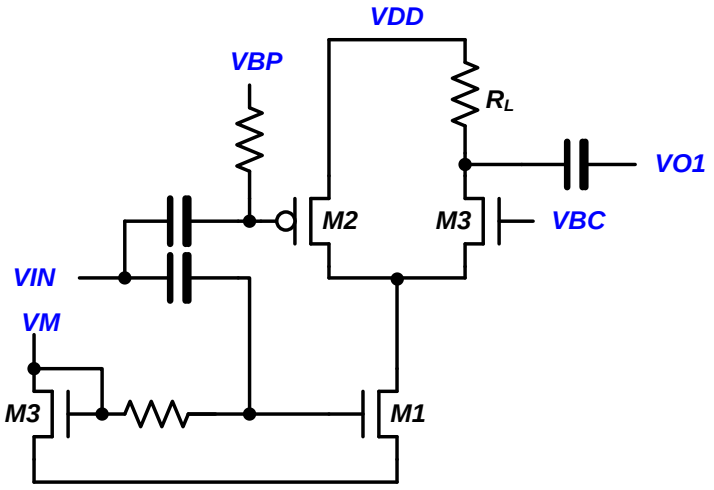


Figure 3.17: Circuit Diagram of LNA.

3.3.1.2 Circuit Design

Low Noise Amplifier To allow for good receiver sensitivity, the input signal is first amplified by a LNA. As mentioned in Section 3.3.2, there are greater payoffs in sensitivity when gain instead of noise is improved. Therefore, the gain of the LNA will be of priority. Figure 3.17 shows the adopted modified cascode-type LNA topology [46]. The classic common source cascode architecture is one of the most popular topology due to its wide bandwidth, high gain, and high reverse isolation and reasonable noise figure. It is made of an input common source stage and a cascode common gate stage. The common-gate stage has inherently wide-bandwidth characteristics. This in conjunction with the cascode topology increases the output impedance and extends the overall bandwidth of the LNA, which allows the LNA to operate at high gains at high frequencies. The increased gain, also leads to better isolation between the input and output ports. The common gate stage provides a low input impedance, suppressing the Miller effect of the common source stage, improving the reverse isolation and bandwidth.

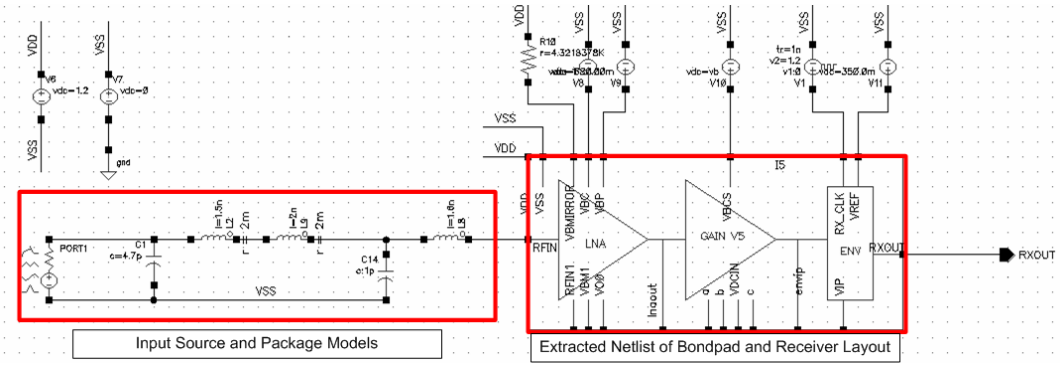
However, due to the low operating supply voltage, device M2 has been added

to modify the classic cascode configuration. Device M2 acts as a current-steering transistor which diverts a fraction of the bias current from the common-gate stage for improved headroom. At the same time, M2 acts as a common-source amplification stage and contributes a portion gain, therefore improving the gain of the LNA. The loading resistor (R_L) is directly proportional to gain. By increasing the value of the resistance, a higher low frequency gain and generally lower power is achieved. However, due to the pole contributed by the capacitive load and the loading resistor (assuming sufficiently large and negligible drain resistance), increasing the resistance will decrease the bandwidth which will affect the gain at 2.4-GHz range. Therefore, there is an optimum value for the resistance of R_L and it can be optimized for sufficient gain within the power budget.

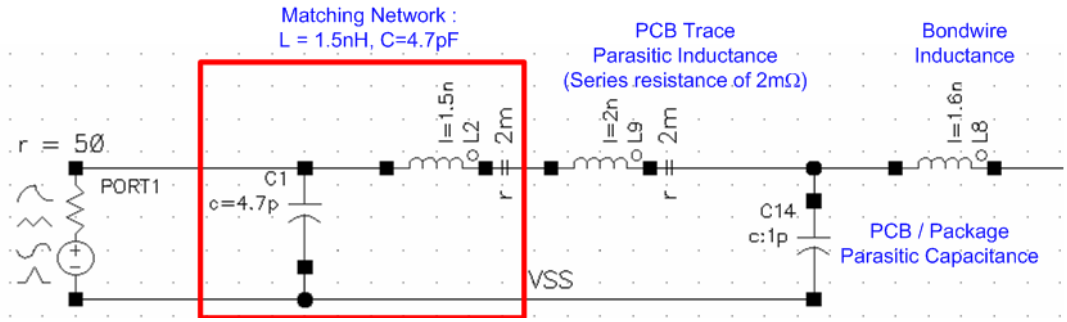
Even though inductive degeneration at the NMOS common source stage is typically adopted to achieve source matching, S-parameter simulations with the extracted pad parameters, a matching network and a simple package model representing package and trace parasitics indicate that an S11 lower than 10-dB is attainable.

As shown in Figure 3.18. the LNA is simulated with a combination of estimated package parasitics and the extracted bondpad netlist. In addition, a matching network is also included in the test bench to provide a more realistic prediction of the S11 and to ensure that L and C values can be kept within realistic boundaries during measurement. In the presence of PVT variations, model deviations, PCB parasitics, the matching network may need to be adjusted to compensate for such variations and ensure that a S11 better than -10-dB can be obtained. The simulation schematic and values used in the package model are also shown in the schematic figure.

The simulated gain, NF and S11 of the LNA stage using the above testbench is shown in Figure 3.19. Matched to 50-Ω through the extracted bondpad model and a package model including bond-wire inductance and packages parasitic capacitances

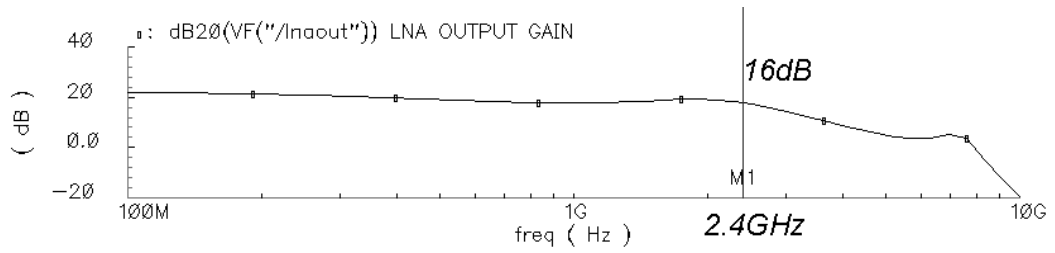


(a) Testbench Schematic.

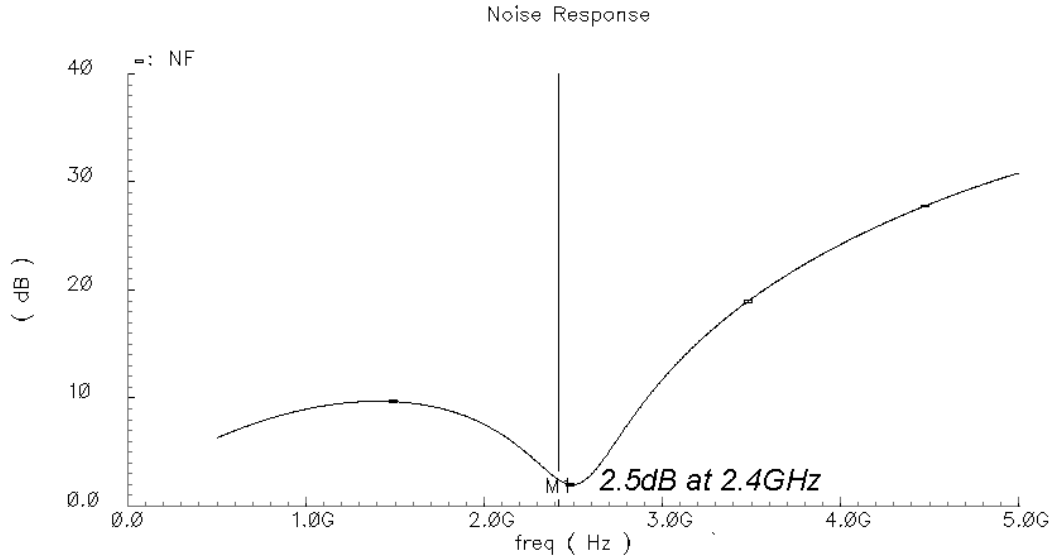


(b) Input Source and Package Models.

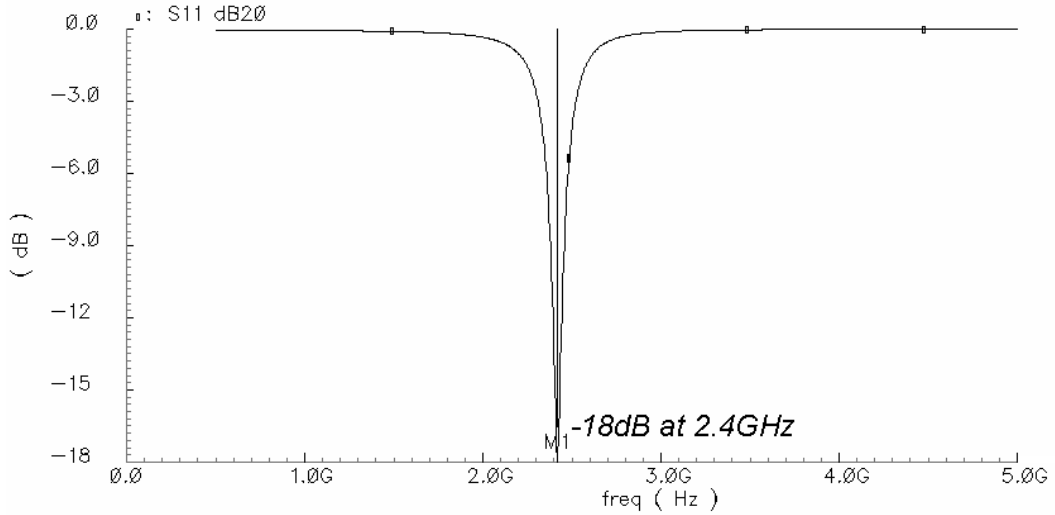
Figure 3.18: Testbench of LNA Simulation.



(a) Gain of LNA.



(b) Noise figure of LNA.



(c) Input reflection coefficient, S11, of LNA.

Figure 3.19: Postlayout simulations of LNA gain, noise figure and S11.

and inductaces, the LNA achieves a gain of 16-dB, an input NF of 2.5-dB and a S11 of -20-dB.

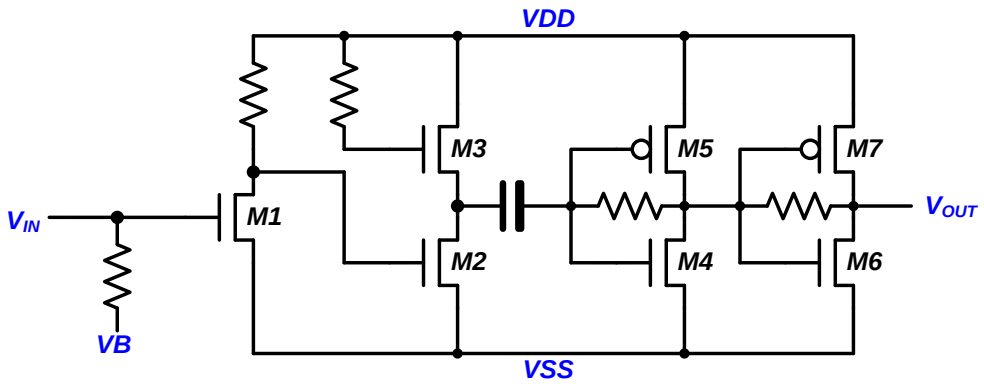


Figure 3.20: Circuit Diagram of gain block.

Gain Amplifier To achieve an overall gain of 60-dB, the subsequent gain blocks need to achieve an overall gain of approximately 44-dB. However, due to the high frequency and low voltage supply, cascode topologies are avoided and instead, four cascaded stages contributing approximately 10-dB each are used. The schematic of the four-stage gain amplifier is as shown in Figure 3.20.

Due to the high output impedance of the LNA, the input common source stage is sized small to provide approximately 8-dB of gain without overloading the LNA output stage. The resistance of the loading resistor is directly proportional to gain but trades off gain due to the pole contributed by the capacitive load and can be optimized accordingly.

It is followed by a second common source stage with active inductor peaking is used to further extend the bandwidth and achieve higher gain. The active inductor load is implemented through an NMOS transistor that is resistor gated. Looking into the source of the transistor presents an inductive impedance that partially tunes out the capacitive load at that point and increases the bandwidth of the stage. However, the drawbacks of active inductors are the additional noise contribution and the large voltage drop caused by the NMOS threshold voltage which is further increased by body effect. Due to the fact this is the third stage of amplification and does not

contribute much to the overall noise figure, the additional noise contribution can be tolerated To reduce the VDS voltage drop across the active inductor load, a low threshold voltage NMOS device is used. To further reduce the body effect, the bulk is tied to the source of the NMOS. A gate resistance of 14-kΩ is used in the active inductor load to to extend the bandwidth of the amplifier by approximately 20%.

To reduce power consumption, the last two stages of amplification make use of current reuse. Compared to the conventional common-source stage, the current-reuse topology amplifies using both the NMOS and PMOS. It therefore doubles the transconductance and gain for the same bias current. The last two stages are self-biased using a large feedback resistor between the input and output. This design is adopted to prevent runaway of the DC operating points due to the cascaded stages. The choice of the feedback resistance is an important parameter that affects the output resistance and gain. First, to prevent the loading of the self-biased inverter on the second amplification stage, an AC coupling capacitor is inserted between the second and third stages. The gain of the second stage is thus shielded from the resistive loading of the subsequent stages. The coupling capacitor and input resistance effectively form a high pass pole and contribute negligible effect. However, the series combination of the coupling capacitor and the input C_{GS} of the subsequent stage increase the capacitive load slightly and thus the coupling capacitor needs to be selected carefully.

Second, the expressions for the gain and bandwidth of the self-biased inverter need to be analyzed. The schematic of a generic self-biased inverter is shown in Figure 3.21. With current reuse, the overall transconductance is increased to $(g_{mN} + g_{mP})$ for the same biasing current as compared to a single-transistor topology. The gain is therefore approximately

$$A_V \approx (g_{mN} + g_{mP}) \,.\, (Z_L) \tag{3.9}$$

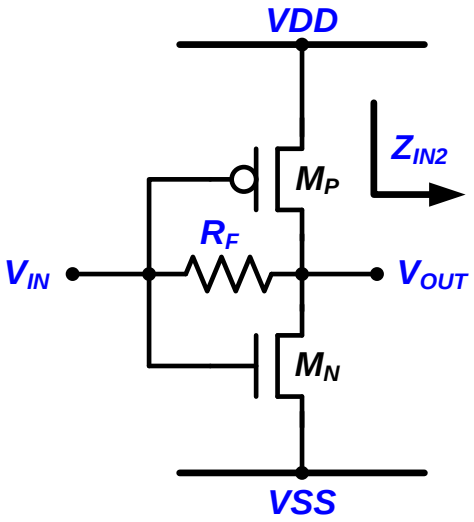


Figure 3.21: Schematic of generic self-biased inverter stage.

where the output resistance is represented by Z_L and is shown in equation 3.10.

$$Z_L = R_F//r_{dsN}//r_{dsP}//Z_{IN2} \tag{3.10}$$

As the input resistance sees R_F in series with Z_L, it can be assumed that the dominant pole is at the input of the amplifier. The bandwidth of the amplifier can thus be estimated to be as shown in 3.11. [47]

$$BW_{-3dB} \approx \frac{1+A_V}{2\pi \cdot R_F \cdot (C_{gsN}+C_{gsP})} \tag{3.11}$$

As first look from 3.9 and 3.10, increasing R_F increases gain while trading off bandwidth. However, since r_{dsN} and r_{dsP} can be assumed to be much larger, the gain is primarily determined by $R_F//Z_{IN2}$. Even though increasing R_F may help to increase the gain, the increase is expected to be small as Z_{IN2} is expected to be small and dominate. In addition, due to the DC blocking from the coupling capacitor, there is no need to increase the value of R_F for reducing loading. Therefore, the value of R_F can be chosen small to achieve the necessary bandwidth and achieve reasonable

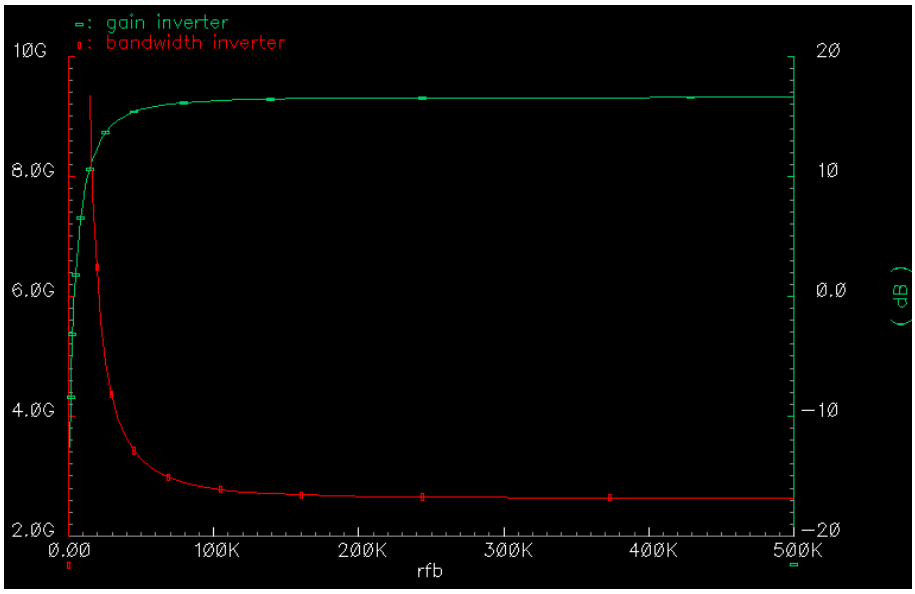


Figure 3.22: Simulation of 3-dB Bandwidth and Gain of Self-biased Inverter against R_F.

gain.

A simple simulation of the gain versus the 3dB bandwidth of the amplifier (inclusive of the coupling capacitor) with respect to the value of the feedback resistor is shown in Figure 3.22. As can be seen, R_F values above 200-kΩ provide no further increases in gain. Therefore, a R_F value of about 100-kΩ is chosen which gives a gain of about 17-dB and a 3-dB bandwidth of about 2.8-GHz.

The simulation results of the 4-stage gain block is shown in Figure 3.23 and the gain block contributes a gain of approximately 45-dB bringing the overall front-end receiver gain to about 60-dB.

Envelope Detector A important block of this receiver is the envelope detector. Envelope detectors are typically implemented with a rectifier followed by a peak detector. The rectifier uses a non-linear response to extract a DC signal from the amplitude of an AC signal. In a standard silicon process, PN and MOS diodes are often used to implement a rectifier. Even though a PN diode is ideally able to provide

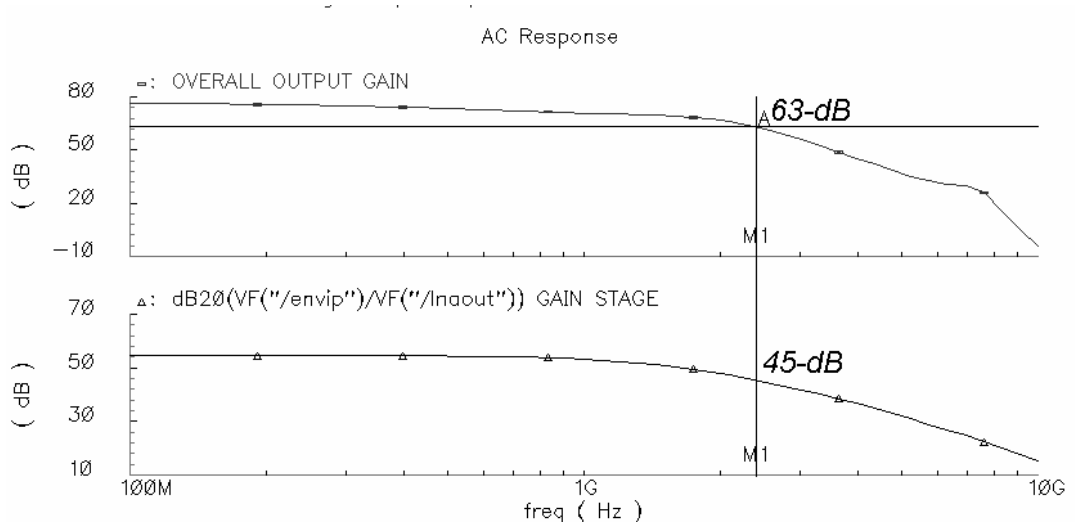


Figure 3.23: Postlayout simulation of gain amplifier.

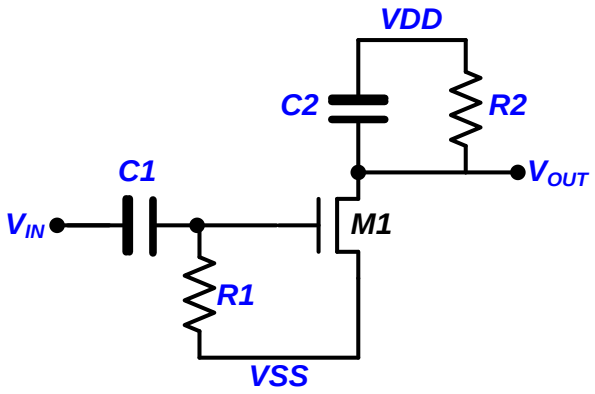


Figure 3.24: Circuit Diagram of envelope detector.

larger conversion gain, it requires a DC voltage drop of at least 0.8-V across it. At a voltage supply of 1.2-V, this will result in very tight headroom requirements for subsequent stages. Therefore, the MOS diode is preferred.

The schematic of the first-order RC high pass filter and the envelope detector used is shown in Figure 3.24. To help to reduce the glitches and reduce low frequency noise, a high pass filter precedes the envelope detector. As the input signal is a 2.4GHz carrier modulated at 5-Mbps (equivalent to 2.5-MHz square signal), the high pass pole is selected to be about 5 times smaller at 500-kHz which determines the

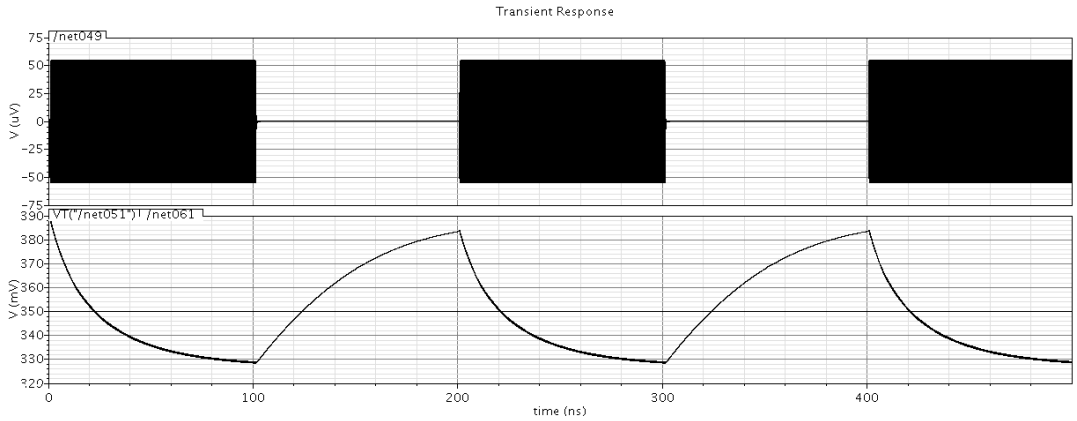
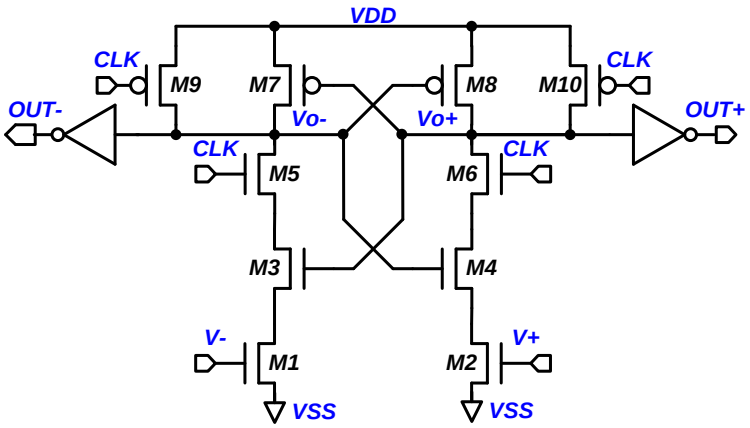


Figure 3.25: Simulated operation of envelope detector.

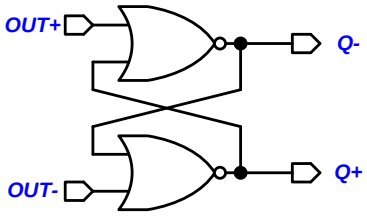
values of R1 and C1 to be 600-kΩ and 500-fF respectively.

The envelope detector is based on the common source pair operating in sub-threshold region and is effectively equivalent to a source-follower with a slow time constant at the output, where this time constant is determined by (R2 $\times$ C2). With a bit period of 200-ns, the time constant should be sufficiently small compared to the bit period such that the envelope output voltage is able to reach steady state before 200-ns while providing the largest possible output envelope for a given input. Since the transistor behaves as a common-drain amplifier, R2 can first be chosen to be relatively large such that it does not load the output and bring down the gain further. Capacitor C2 can then subsequently be optimized such that the time constant is approximately 50-ns as it takes about 5 time constants to approximate steady state. The final values of R2 and C2 are 600-kΩ and 1-pF.

With a larger R2 value which gives a longer rise time, even though output loading can be reduced and the conversion gain is improved, the duration for which the pulse is above the reference voltage is reduced. This is detrimental to the latch as it requires faster switching and convergence times at the expense of higher current consumption. For a data rate of 10-Mbps, Figure 3.25 presents simulated operation of the envelope detector for a '1010' RF input.



(a) Regenerative comparator.



(b) SR Latch.

Figure 3.26: Circuit diagram of the dynamic comparator.

Comparator As seen in the previous section, the input data signal is recovered through the recovery of the envelope information. As the envelope detector provides a signal output in the order of 20-mV, this signal has to be buffered rail-to-rail to convert it into a digital signal. This will ease digital integration with the baseband block. Since the input into the comparators is in the order of tens of millivolts, the resolution of the comparator is relaxed and resolution can be traded for power savings. Therefore, a dynamic comparator based on the Lewis-Gray topology [15] which has low static power consumption is adopted.

Figure 3.26 shows the circuit of the dynamic comparator. After the envelope detector, the clocked, regenerative latch regenerates the voltage difference using the positive feedback mechanism in the cross-coupled inverter. During the reset phase, when the CLK is VSS, $Vo+$ and $Vo-$ nodes of the regenerative latch are reset to

VDD. During the comparison phase, when CLK changes to VDD, the transistors M5 and M6 are turned on. The input transistor pair (M1 and M2) starts to charge the output nodes, $Vo+$ and $Vo-$, at different rates which is proportional to the applied input voltage ranging from VDD to VSS. The cross-coupled P-type transistors (M4 and M5) are turned on and this initiates the positive feedback process enabling the regeneration of a small differential voltage $\triangle V_{in} = V+ - V-$ to a full swing differential output. A pair of inverters is added to the differential output stage of the comparator so that it improves the driving capability for the next SR latch stage.

After the regenerative latch stage, the SR latch performs a conversion from return-to-zero to non-return-to-zero. The circuit of the SR latch is as shown in Figure 3.26b.

To evaluate the input offset of the comparator, 165 monte carlos simulations were executed. The mean offset of the comparator is 88uV. This is sufficient as postlayout simulations measure the peak-to-peak voltage produced by the envelope detector to be about 70mV for an input signal of -65dBm. The reference voltage of the comparator can be adjusted externally to compensate for the offset voltage.

3.3.1.3 Overall Receiver Performance

The overall layout of the receiver is shown as in Figure 3.27. Due to its inductorless structure, the receiver is very compact, occupying a core area of only 300-μm by 100-μm.

Figure 3.28 demonstrates the post-layout simulated operation of the entire receiver. Operating at 1.2-V supply, the input signal is at an input power of -75-dBm referenced to a characteristic impedance of 50-Ω, modulated by a '1010' data stream at 10-Mbps. The clock to the latch samples at a frequency of 10-MHz. Consuming an average current of 2.58-mA, the energy efficiency of the envelope detection receiver is 0.31-nJ/bit.

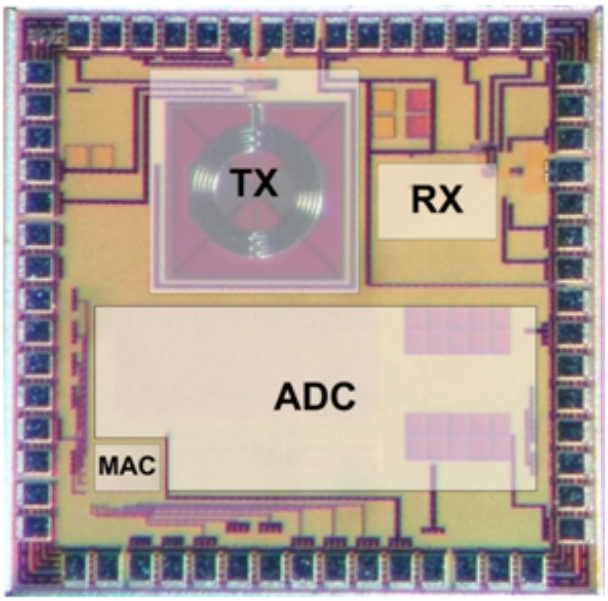


Figure 3.27: Chip Photo.

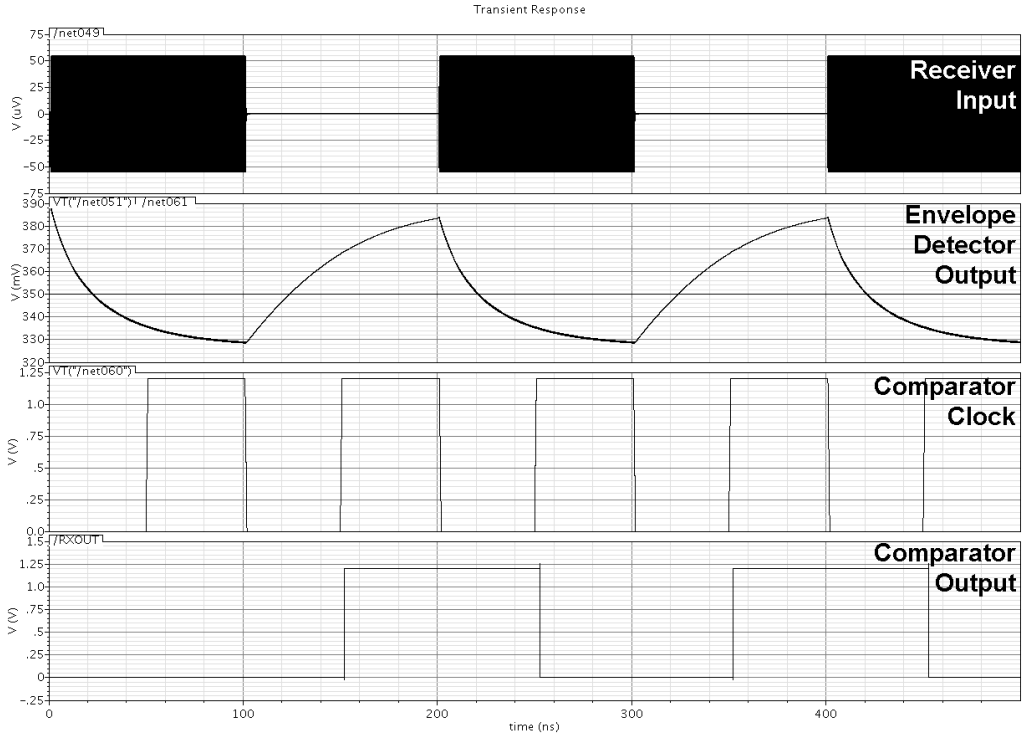


Figure 3.28: Post-Layout Simulated operation of overall receiver performance.

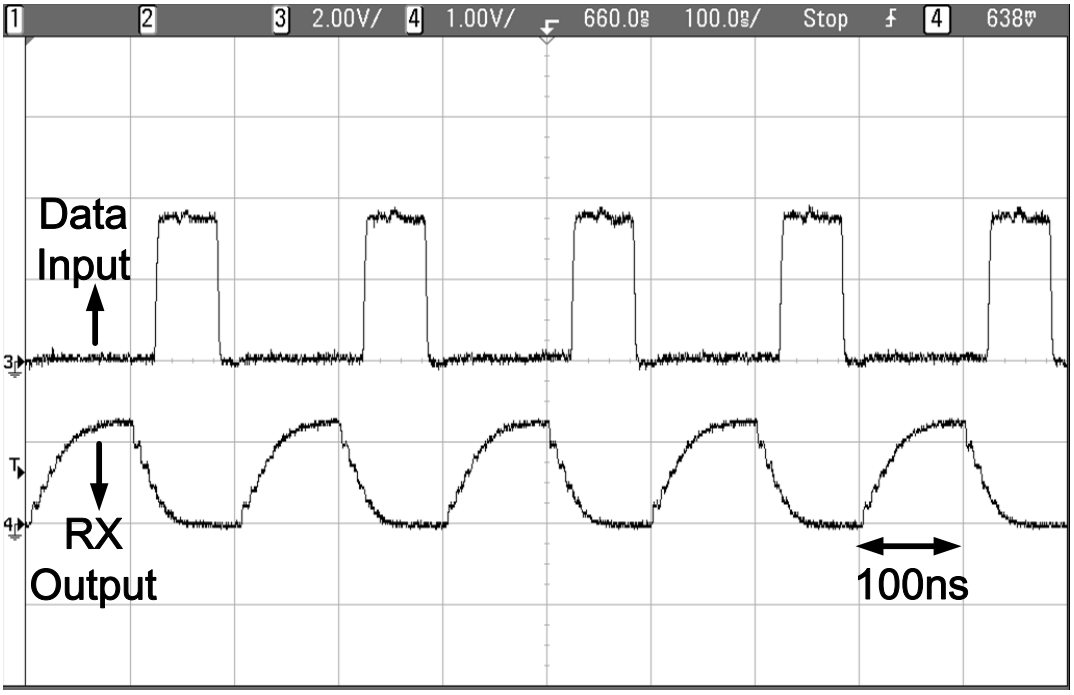


Figure 3.29: Oscilloscope screenshot of receiver operation at 10-Mbps.

3.3.1.4 Measurement Results

To evaluate the functionality of the receiver, a '1010' data stream input was applied to the RF signal generator. The modulated RF signal at an output power of -60-dBm at 2.4-GHz is supplied to the receiver and the output is monitored on the oscilloscope in the time domain. Figure 3.29 shows the oscilloscope screenshot of receiver operation. A '1010' data sequence is applied to the RF signal generator, modulating the 2.4-GHz signal input at 10-Mbps. It can be seen that the receiver is able to demodulate and recover the '1010' input data correctly at 10-Mbps.

In the figure, it can also be observed that the comparator output waveform does not exhibit a duty cycle of 50%. This is due to a few factors. First, as the envelope detector output is being compared to a reference voltage, non-50% duty cycles will be generated when the reference voltage is not exactly in the middle of the envelope detector output. In addition, as the regeneration or latch time (of the comparator

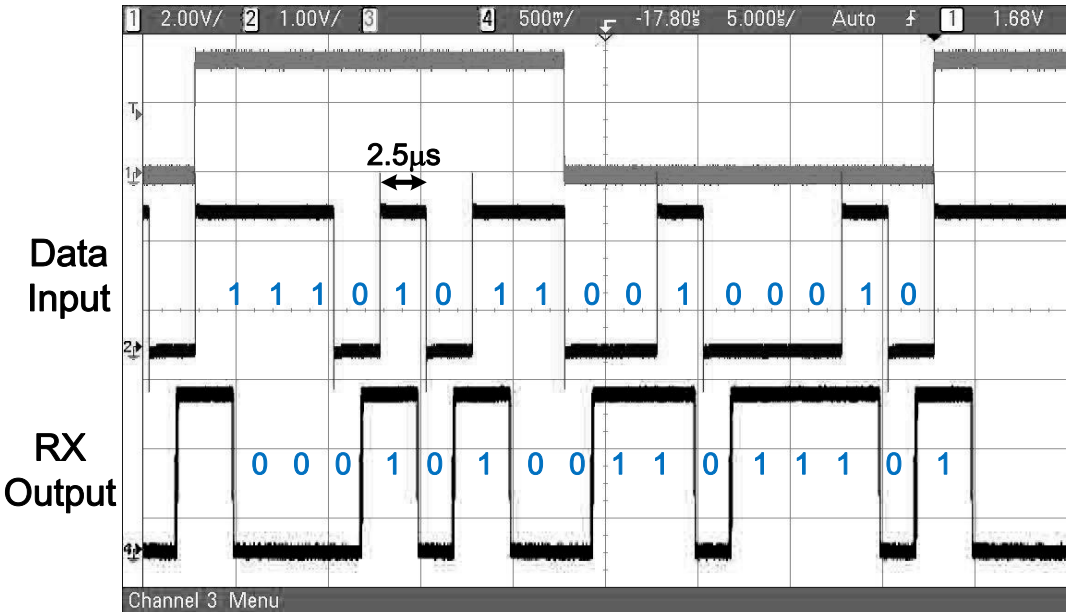


Figure 3.30: Oscilloscope screenshot of receiver operation with PRBS data input.

is dependent on the differential input voltage to the regenerative pair, the rising edge of the comparator output will occur at varying times. This may also lead to non-50% duty cycles. This can be corrected by re-sampling the comparator output with reference to a clock signal at the same frequency.

Figure 3.30 further demonstrates the performance of the receiver with a 16-bit pseudo-random data sequence at 400-kbps, indicating proper operation with random inputs.

To characterise the reliability of the receiver, the BER of the receiver is calculated over a continuous set of 10,000 bit samples. A repeated '1010' input data sequence is used for post-processing simplicity. The measured BER performance of the receiver is 10^{-2} for an input signal strength of -60-dBm at 5-Mbps. The BER does not meet the target specifications of 10^{-3}.

Investigations through post-layout simulations suggest that this is largely due to digital noise and clock coupling through the common pad ring. Due to insufficient pads, the digital and analog supply rings were connected together, resulting in a

common power supply for the pads. By simulating the core together with the pad frame, the simulation results suggest that the glitches coupling from the transitions of the digital clock travel into the analog power supply though the pad ring and severely affect the performance of the envelope detector at small signal amplitudes. This therefore degrades the sensitivity of the receiver. This problem can be easily rectified by separation of the analog and digital pad rings in future work.

The receiver consumes a current of 2.9-mA from a 1.2-V voltage supply, achieving an FOM_{RX} of 0.7-nJ/bit at 5-Mbps. This FOM_{RX} is higher than the targeted specification as well due to the lowered data rate. Therefore, in order to further lower down the current consumption and achieve the desired sensitivity at 10-Mbps, a second generation design is implemented that will be elaborated in the next section.

3.3.2 Super-Regenerative Receiver

The super-regenerative architecture is based on the super-regeneration principle invented by Armstrong in 1922 [48]. In the past, this architecture was meant for use in vacuum tube circuits, but it has seen a renewed interest due to their excellent sensitivity for small amounts of DC power consumption. Compared with the envelope detection architecture, the high gain and power consuming RF gain blocks are replaced with the high gain oscillator, reducing the power consumption greatly. However, this is at the expense of much larger area due to the on-chip inductor required. In addition, a major disadvantage of this architecture is the poor selectivity and component variations due to changes in environment and process.

3.3.2.1 Introduction

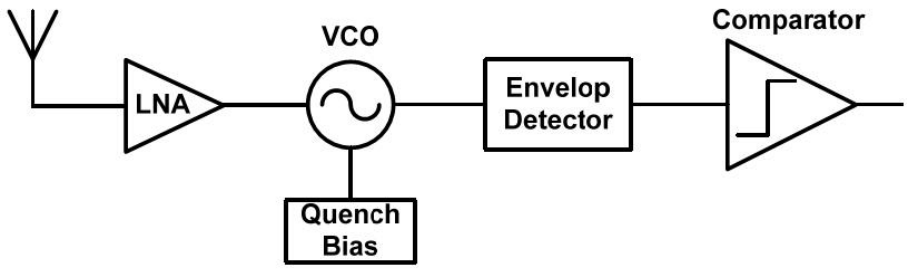


Figure 3.31: Block diagram of a generic super-regenerative receiver.

A basic block diagram of the super-regenerative receiver (SRR) is presented in Figure 3.31. The SRR consists of a tuned amplification block, an oscillator, an envelope detector and a comparator. The principle of super-regeneration is simply put, based on the variation of the start-up time of the oscillator. Normally, an oscillator starts oscillations due to the presence of thermal noise in the circuit, which can be a relatively slow process. In the presence of an external injected RF signal, such as a carrier at the resonance frequency, the startup becomes much

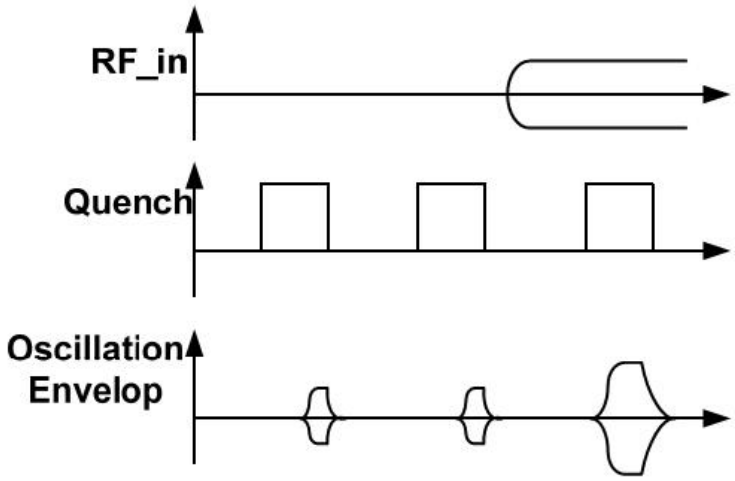


Figure 3.32: Operation of a generic super-regenerative receiver.

faster. Therefore, in OOK modulation where the amplitude is 100% modulated, the modulated signal is easily detected with this architecture.

The main signals are illustrated in Figure 3.32. The oscillator is periodically enabled and disabled through the quench signal. In receive mode, the oscillator is enabled and held at the edge of oscillation. If a '1' is transmitted, the oscillations quickly build up due to the incoming signal. When a '0' is transmitted, the oscillations in the receiver take much more time to build up. Therefore, by tracking the envelope information using the envelope detector circuit and setting an appropriate threshold voltage for the comparator, the oscillations in each quench cycle can be used to determine whether the transmitted signal is a '0' or a '1'. However, since the oscillations eventually saturates, the oscillator needs to be reset and quenched to repeat the start-up cycle again. Therefore, the oscillator is quenched periodically by the quench signal.

There are two general modes of operation as shown in Figure 3.33. In the linear mode, the self sustained oscillations are quenched before they reach their maximum amplitude. Therefore, the height of the SRO output has a linear relationship with the RF input power and the envelope of the oscillations is detected at an appropriate time

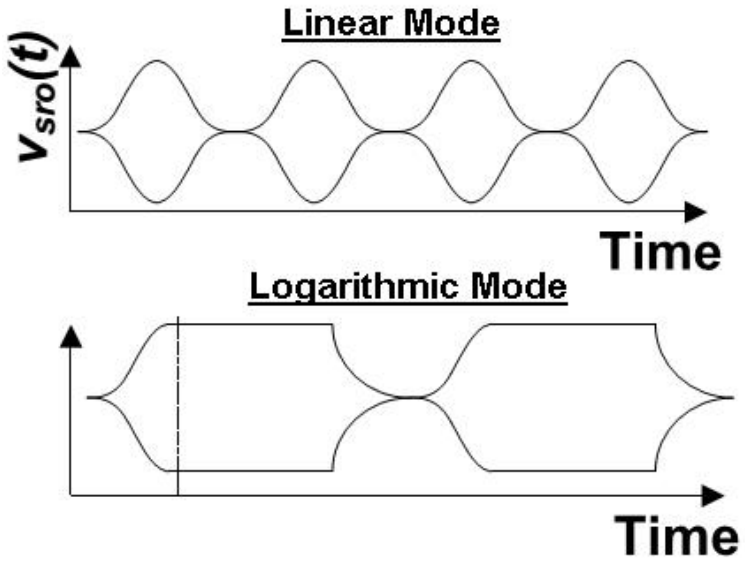


Figure 3.33: Linear and logarithmic modes of operation for SRR.

before oscillations saturate. In the logarithmic mode, the self sustained oscillations are allowed to reach their maximum amplitude at steady state such that the area enclosed by the envelope of the SRO output has a logarithmic relationship with the RF input power. In this mode, the circuit counts the duration for which the envelope stays above a certain threshold value. Since this mode of operation needs a longer time for the oscillator output to reach steady state, it effectively limits the achievable data rate. In this work, the linear mode of operation is chosen to maximize the data rate.

3.3.2.2 Theory of Operation

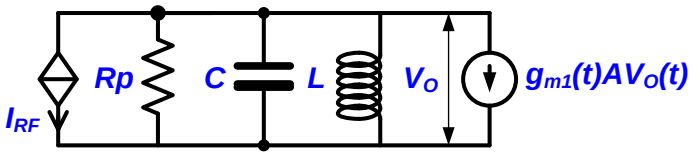


Figure 3.34: Resonant Tank Model.

The parallel resonant tank which forms the core of a resonant oscillator is as

shown in Figure 3.34. The resonant tank consists of an inductor L, a capacitor C, and R_P represents the dissipative losses in the inductor due to finite Q. The time varying transconductance provided by active devices is represented by $g_{m1}(t)AV_o(t)$ while the injected input signal is modeled by a current source I_{RF}. Applying KCL to Figure 3.34, the transfer function can be expressed as :

$$\frac{V_O}{I_{RF}} = \frac{Z_O \omega_O s}{s^2 + \left[\frac{Z_O \omega_O s}{R_P} - g_m A Z_O \omega_O\right] s + \omega_O^2} \tag{3.12a}$$

$$Z_O = \sqrt{\frac{L}{C}} \tag{3.12b}$$

$$\omega_O = \sqrt{\frac{1}{LC}} \tag{3.12c}$$

The quench signal with the corresponding movement of poles is shown in Figure 3.35 [42]. As can be seen from (3.12a), the real parts of the poles varies from a negative value determined by the passive components to a positive value as g_m increases from zero to beyond the minimum transconductance required for oscillation (g_m, min). The bias current at which this happens is typically called the critical current ($I_{CRITICAL}$). The damping factor, which is the coefficient of the s term in (3.12a), determines whether oscillations will be self-sustainable.

For oscillator currents below $I_{CRITICAL}$, the poles remain in the left half plane and the output oscillations are overdamped. The SRO behaves like a band pass filter with high Q and this is also termed the regeneration mode. As currents increase above $I_{CRITICAL}$, the poles move to the right half plane. The resonant system is now underdamped and this is termed the super-regeneration mode. With the loaded Q decreasing, the SRO starts to oscillates with a start up time inversely proportional to the current in excess of $I_{CRITICAL}$.

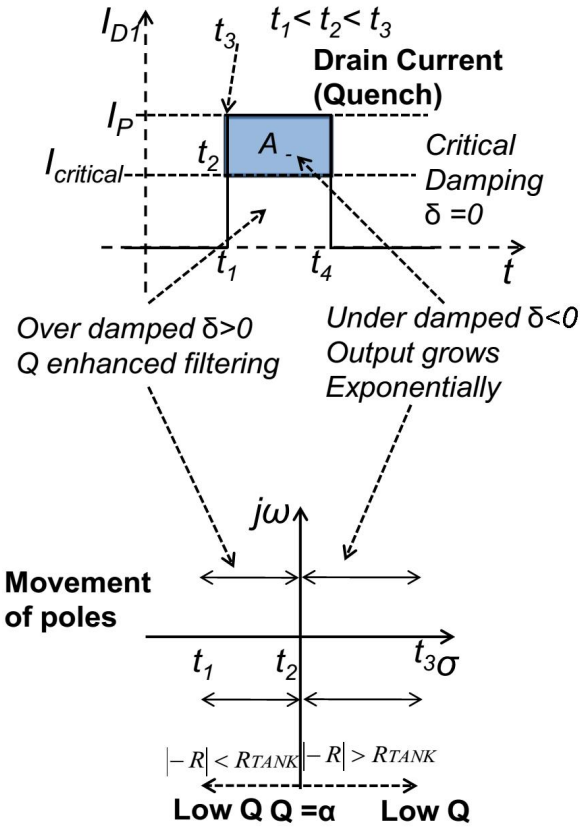


Figure 3.35: Quench Signal and Movement of poles.

The super-regenerative gain and selectivity of the receiver has been derived for various commonly used types of quench signals, such as the sawtooth, sinusoidal and triangular waveforms [49]. It has been proven that selectivity is mainly controlled by the slope at the point where current transits beyond $I_{CRITICAL}$. Therefore, selectivity can be slightly improved with quench signals that transit gradually in the region of $I_{CRITICAL}$ [50]. Therefore, amongst the three commonly used quench signal waveform shapes, the sawtooth quench waveform provides the best selectivity.

This is however at the expense of reduced data rates as more time is now required to allow these slower transitions and for oscillations to build up. In addition, to generate such accurate current values, current DACs are typically required to accurately control the value and slope of the drain current. However, for an on-chip

resonant tank, the exact value of loss is difficult to determine and furthermore, $I_{CRITICAL}$ varies with temperature, resulting in inconsistent receiver selectivity and sensitivity [33]. For precise operation, calibration may be required which further reduces the achievable data rates. Though the selectivity is enhanced, power consumption is also considerably increased.

Trading off selectivity for data rate and low power consumption, the square wave quench has been adopted. It offers the best super regenerative gain and also allows the possibility of direct integration with the baseband and MAC block as there is no need for DACs. However, it has the worst selectivity and sensitivity due to the fast rising edges. The next section examines the noise performance of the SRO using a square wave quench and shows that it is sufficient to attain the required sensitivity.

3.3.2.3 Noise Analysis

In the super-regeration mode, the SRO starts to oscillates with a start up time inversely proportional to the current in excess of $I_{CRITICAL}$. The amplitude of the envelope is proportional to the current in excess of $I_{CRITICAL}$ and is also proportional to the time duration for which the oscillation has been allowed to build up, labelled as $(t_4 - t_1)$ in Figure 3.35. For a square quench signal, this shaded area $A-$ is thus known as the superregenerative gain, G_S, and can be expressed as :

$$G_S = \frac{\Delta\Omega^{0.4}}{\Delta\Omega - 1}\left[\frac{1}{\pi}\frac{\Delta\Omega * \Omega_q}{\Delta\Omega^2 - 1}\left(e^{A-} - 1\right) - \frac{1}{2}\right] \tag{3.13}$$

where $\Delta\Omega$ is the difference between the minimum damping factor and the mean damping factor; $A-$ is the shaded area; Ω_q is normalized quench frequency and they are given by,

$$\Delta\Omega = \frac{I_P - I_{CRITICAL}}{I_{CRITICAL}}$$

$$A_- = (I_P - I_{CRITICAL})(t_4 - t_2)$$

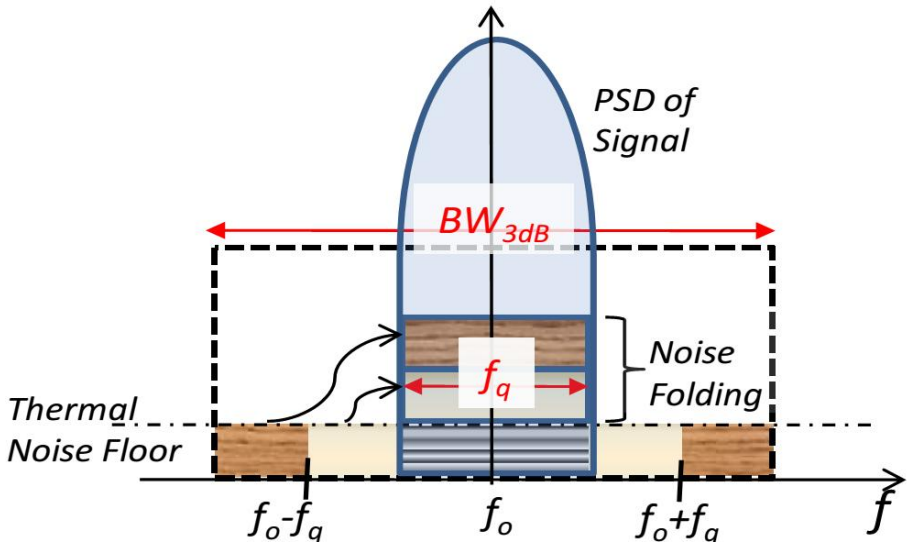


Figure 3.36: Noise Folding of the SRO's thermal noise assuming that BW_{3dB} is 3 times of quench frequency.

$$\Omega_q = \frac{w_q}{\bar{\omega}}$$

The noise contribution from SRO is not restricted to the thermal noise contribution from the occupied bandwidth of the signal alone. The SRO produces a sizable output signal even when there is no incoming RF input due to the periodic enabling through the quench signal. This noise response therefore depends on the quench frequency and the SRO gain G_S. In order to reduce this noise response, the SRO gain G_S can be traded off by reducing the g_m or the bias current $(I_P - I_{CRITICAL})$. However, this reduction of SRO gain reduces the output amplitude of the envelope, increasing the baseband gain required to distinguish between a '0' and '1'. Keeping G_S at a reasonable value by reducing the time constant widens the noise bandwidth.

In order to ensure that the SRO output signal rises to a reasonable level for a '1', the modulation bandwidth (BW_{-3dB}) or noise bandwidth needs to be much larger than the quench frequency. As the SRR is effectively a data-sampled system, the receiver input signal is discretely sampled by the SRO and this causes noise aliasing. This noise bandwidth folds itself due to the sampling by the quench signal as shown

in Figure 3.36. This noise can be defined by the excess noise ratio γ, and for large SRO gains is defined as [49]

$$\gamma = \frac{BW_{-3dB}}{f_Q} \tag{3.14}$$

where

$$BW_{-3dB} = \frac{2f_q}{\Omega_q}\sqrt{\sqrt{2\left(\Delta\Omega^4+1\right)}-\Delta\Omega^2-1} \tag{3.15}$$

The BW_{-3dB} is typically about two to four times the quench frequency and increases when the super-regenerative gain increases. Therefore, from (3.15), it can be seen that minimizing the quench frequency also reduces the bandwidth and improves the selectivity.

However, to satisfy the Nyquist criterion, the quench frequency must be greater than twice the bandwidth of the incoming signal because the timing of the incoming RF signal is unknown. This leads to increased noise bandwidths and degrades the selectivity of the receiver. Therefore, a particular contribution of this design is a simple quench alignment circuit which reduces the quench frequency to the data rate, optimizing the sensitivity and selectivity performance.

Assuming the quench frequency to be equal to that of the data rate and for a conservative estimate, the 3-dB bandwidth is taken to be 10 times that of the quench frequency, an excess noise factor of approximately 10-dB is obtained. This excess noise factor component modifies the link budget equation and the link budget for the super regenerative receiver can be expressed as

$$P_{RX,MIN} = 10log_{10}\left(kT\right) + 10log_{10}\left(BW_{-3dB}\right) + SNR_{MIN} + 10log\gamma \tag{3.16}$$

As mentioned in section 3.3.1.1, the minimum SNR is 8-dB. For a data rate of 10-Mbps, the sensitivity of the receiver is estimated to be -76-dBm and is sufficient

for our design.

3.3.2.4 Proposed Quench Alignment

The targeted sensitivity of the receiver is -65-dBm at a data rate of 10-Mbps and with an energy efficiency of <0.2nJ/bit. As mentioned previously, due to the non-coherent nature of OOK modulation, the receiver needs to oversample the incoming signal at least at twice the input data rate to recover the data reliably [51]. This doubles the oscillator power for a given data rate and reduces the energy efficiency of the receiver. Alternatively, it reduces the data rate to half the maximum bit rate and reduces the effective throughput of the communication link. In addition, as the input noise bandwidth of a SRR is proportional to the quench rate, oversampling increases the input noise bandwidth and reduces the sensitivity of the SRR. Therefore, one method to improve the energy efficiency of the SRR is to adjust the phase of the quench sampling signal such that it synchronously samples the incoming RF signal.

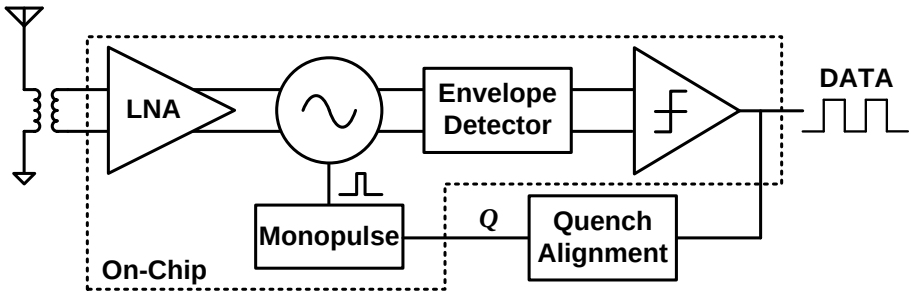
However, to do that, the quench signal must first be aligned to the incoming data signal. In [51], the quench is manually aligned externally. In [50], a closed loop scheme is employed for this alignment. Such non-data aided closed loop schemes trade off the exact timing and hence sensitivity to consecutively identical digits. In addition, the loop requires a certain settling time during which the phase of the quench is not accurate. This means that the initial portion of the data in a packet cannot be detected, which is a disadvantage for small packets.

Quench alignment techniques were also proposed to achieve higher data rates [34] or reduce power consumption [52]. The method in [34] locks an additional oscillator operating at baseband frequency to a Gaussian modulated RF signal through a phase-locked loop (PLL) and achieves good sensitivity and energy efficiency. However, the closed loop feedback system increases the complexity due to stability

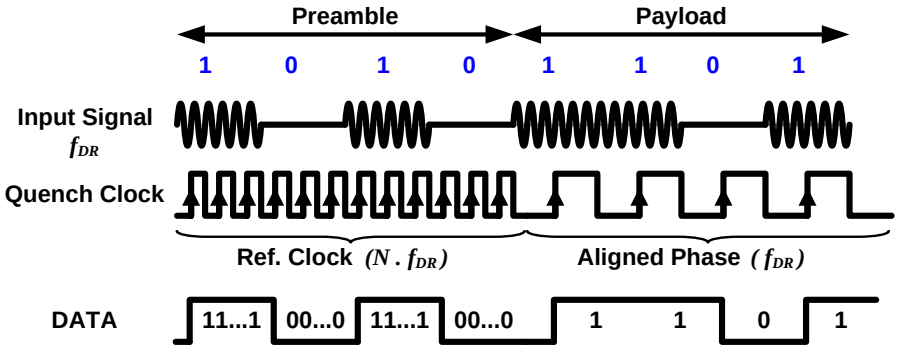
and locking considerations. It may also be difficult to implement the design on-chip due to the large component values required in the PLL's low frequency loop filter. The synchronous self-aligning quench technique in [52] utilizes the oscillator's startup time to control the quench frequency. As the quench frequency is fixed at a multiple of the maximum data rate, power consumption is fixed and this is not energy-efficient when the data rate is low.

This work proposes a SRR with a digital quench alignment scheme that generates the quench signal for synchronous sampling based on oversampling the preamble of a data packet. Figure 3.37b illustrates the proposed automatic quench alignment scheme. In most wireless transmission protocols, data packets begin with a preamble that consists of a known and fixed pattern of bits such as '1010'. The preamble is used to delimit the start of packet transmission, provide clock synchronization or facilitate DC compensation. For example, the Zigbee standard uses a preamble of 4 bytes or 32 bits at the beginning of the data packet while Bluetooth makes use of a '1010' or '0101' standard preamble code. Therefore, making use of the preamble is a convenient approach and does not require any additional hardware or changes to be made to the baseband layer.

The proposed scheme takes advantage of this and oversamples the preamble of the incoming data packet by N times and selects the optimum phase out of N phases for synchronous sampling of the remaining payload or information bits of the packet. Once the correct phase is selected, the quench frequency can be reduced to a frequency equal to the data rate. Due to the simplicity of the proposed scheme, no special bit shapes are required and the alignment can be applied across all data rates, achieving power savings even at low bit rates. This alignment scheme can also be easily integrated into the baseband block.



(a) Block diagram.



(b) Timing diagram.

Figure 3.37: Super regenerative receiver architecture.

3.3.2.5 Receiver Architecture

Figures 3.37a and 3.37b illustrate the block diagram and timing diagram of the proposed SRR. It consists of a low-noise amplifier (LNA), super-regenerative oscillator (SRO), envelope detector, baseband amplifier and comparator in the forward path. The feedback path includes a monopulse generator and a quench alignment circuit.

Two single-ended LNAs provide 50-Ω matching to the antenna and amplify the modulated 2.4-GHz incoming carrier. The output is directly injected into the oscillatory nodes of the SRO. The SRO is controlled by the quench signal that causes the oscillations to start-up and die out periodically. In the presence of an injected signal, the oscillations start up much faster. By utilizing the variation in start-up time of the oscillator, the oscillator is able to detect the presence of a signal. The envelope

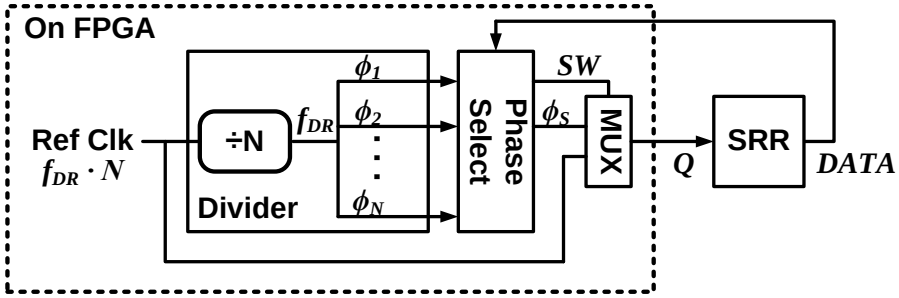
detector extracts the baseband information in the envelope of the oscillations and the baseband amplifier amplifies it before feeding it to the comparator. The comparator digitizes it to a binary output. The oscillator acts as a sampling system where the quench signal is the sampling control signal. To achieve synchronous sampling, the quench signal must be aligned to the incoming data.

As illustrated in Fig. 3.37b, the proposed preamble-based self-alignment quench works as follows. During the preamble phase of the packet, the digital quench alignment block first sets the quench clock to the reference clock signal that has a frequency that is N times of the incoming data rate f_{DR}. Thus, the SRR oversamples the input data and generates N digital output bits in the output DATA signal for each input data bit. These N sets of the preamble output can be collated. Based on the sets of digital output, the phase selector block identifies an optimal phase to synchronously recover the subsequent payload of the packet. Once the optimal phase is selected, the switch control block switches to the selected clock signal of frequency f_{DR}, which is equal to the data rate. This alignment is repeated for each incoming packet.

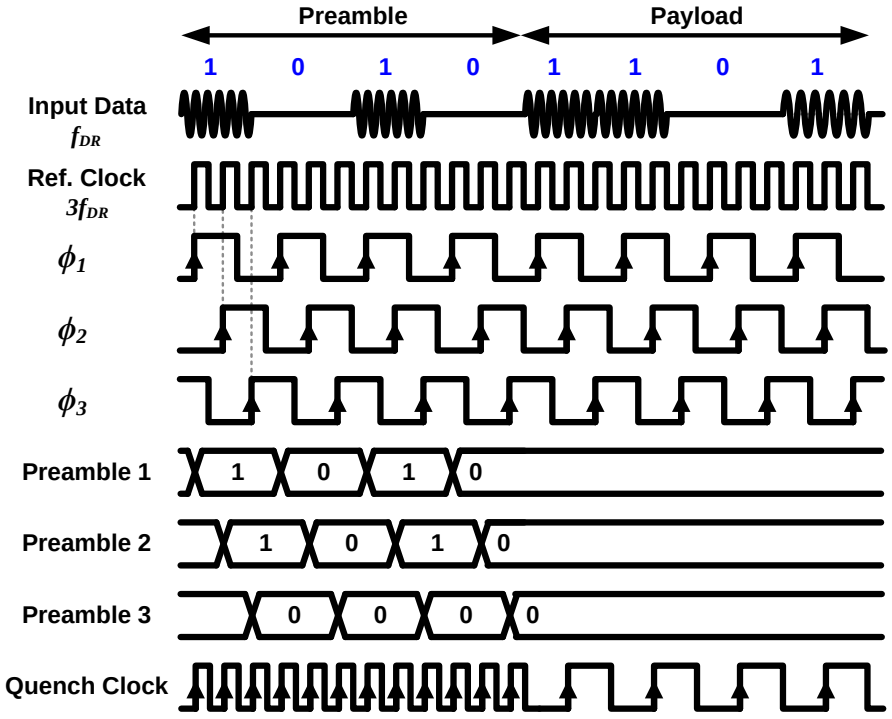
This reduces power consumption as the SRO is only quenched at a frequency equal to the data rate for the remaining of the packet. In addition, additional clock recovery circuits are rendered unnecessary as the quench signal can be used as a bit-synchronous reference clock in subsequent circuits. In this work, for proof-of-concept and flexibility, the quench alignment block is implemented on FPGA. However, it is not difficult to implement it on chip. The detail of the quench alignment process and circuit implementation will be discussed in the next section.

3.3.2.6 Quench Alignment Circuits

Quench Alignment Controller The block diagram of the quench alignment circuit is shown in Figure 3.38a. The quench alignment block consists of a divider, a



(a) Block diagram.



(b) Timing diagram.

Figure 3.38: Quench alignment scheme.

phase selector and a multiplexer. The divider generates N clock signals at frequency f_{DR} where the $i\text{-}th$ clock signal is $360^{\circ}/N \times i$ out of phase with respect to ϕ_1. Based on ϕ_1 to ϕ_N, N sets of the preamble can be recovered from the output $DATA$ from the SRO. The phase selector blocks selects the optimum phase ϕ_S based on the collated preamble sets. After $N \times p_{bits}$ clock cycles, where p_{bits} is the number of bits in the preamble, the multiplexer switches the quench clock to ϕ_S. Based on measurements, a minimum oversampling ratio of 3 is required for reliable operation.

Figure 3.38b shows the timing diagram of the quench alignment process. The preamble pattern of '1010' and the oversampling factor of $N = 3$ are used in this example. The quench clock to the SRO is first obtained from the reference clock source at a frequency of $3f_{DR}$. This generates 3 sets of digital outputs and are labelled Preamble 1 to 3. As the input and the clock signals are asynchronous, the first or third set of the digital output may be not recovered correctly as the quench signal is too close to the edge of the bit period. In this example, Preamble 3 is wrong and indicates that the corresponding clock phase ϕ_3 is unsuitable for use. Therefore ϕ_2 is selected. In the event that Preambles 2 and 3 recover the correct pattern, ϕ_2 will also be selected as that would align the clock signal closest to the middle of the bit period. After 12 clock cycles, the quench clock will transition to the optimum phase selected. The rest of the payload is then sampled at a quench frequency equal to the data rate.

Since the quench clock is recovered based on a limited number of bits, the frequency drift of the sampling clock and input signal will limit the maximum payload length of this alignment circuit. Assuming a clock drift of $\pm$100-ppm for both the input data stream and the quench clock, a worse case relative drift of $\pm$200-ppm is assumed. Therefore, based on the duration of a bit period, a worst-case drift of $\pm$200-ppm would allow a maximum payload length of 500 bits or 62 bytes

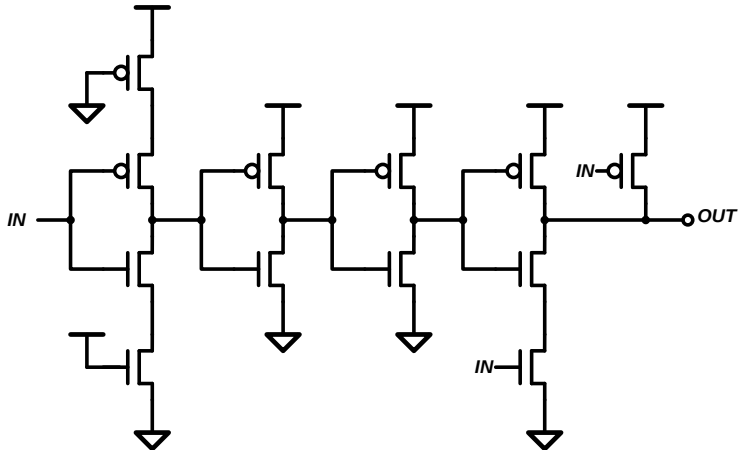


Figure 3.39: Quench generator circuit.

to be recovered correctly.

This quench alignment circuit is implemented off-chip on Microsemi's IGLOO nano FPGA [53] for flexibility to cater to varying preamble lengths and patterns. Due to the simplicity of the circuit alignment scheme, it can be easily integrated on-chip. Synopsys simulations of the implementation in the same technology running at a clock frequency of 30-MHz occupies an area of 44-μm by 44-μm and consumes an average DC power of 30.8-μW. This power consumption contributes an additional 0.03-nJ/bit to the energy efficiency of the receiver.

Quench Generator Circuit The alignment scheme requires the use of two different quench frequencies within a single packet. Since the sensitivity and operation of the SRO is extremely sensitive to the pulse width of the quench signal, any inconsistencies in the pulse width will degrade the performance of the SRO. Furthermore, as quench signals are typically obtained directly from the clock signal or by dividing down the clock signal, this makes it difficult to ensure a consistently exact pulse width across various clock frequencies. Therefore, to overcome this challenge, a pulse-invariant signal can be realized by a mono-pulse circuit as shown in Fig. 3.39. The post-layout simulation results achieve a consistent pulse width of

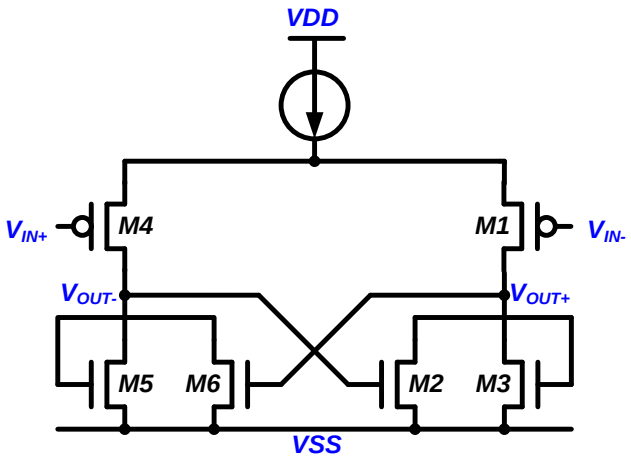


Figure 3.40: Schematic of pre-amplifier.

15-ns across different operating frequencies.

3.3.2.7 Circuit Design

The oscillator, envelope detector and comparator circuit blocks adopted in this receiver have been covered in detail in Sections 3.2.2.1 and 3.3.1.2 respectively and therefore will not be repeated in this section. The pre-amplifier will be covered in the following.

Pre-Amplifier At high quench and clock frequencies, clock kickback and feedthrough from the comparator can cause glitches during the operation of the envelope detector. Due to the small input and output signal amplitudes, these glitches can corrupt the output of the envelope detector. To reduce this effect, the digital supply is separated from the analog supply and a pre-amplifier is inserted between the comparator and the envelope detector. Figure 3.40 illustrates the circuit of the pre-amplifier. The gain of the base band amplifier is boosted by the cross coupled pair across the diode connected loads. To ensure stability, the aspect ratio of the cross connected device is made only 0.75 times that of the diode connected loads. The pre-amplifier provides about 21-dB of gain while consuming 16-μA of current.

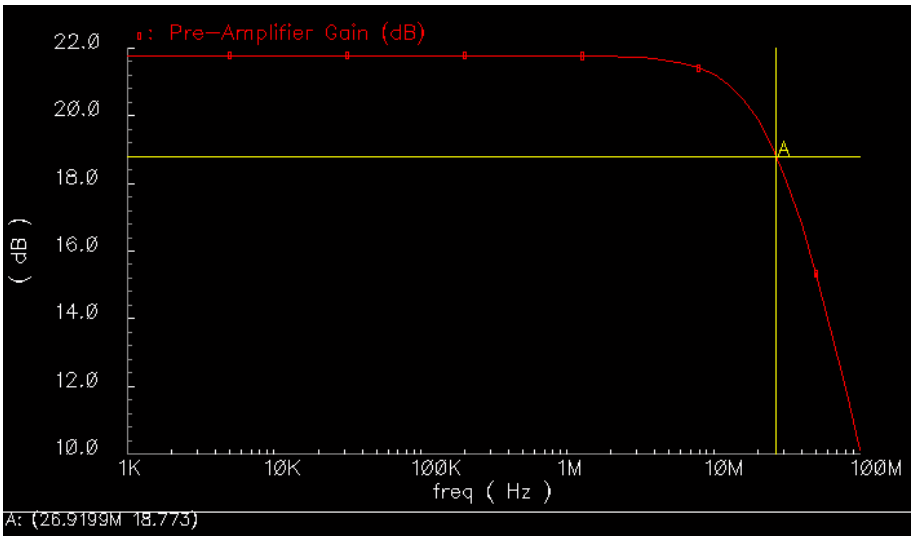
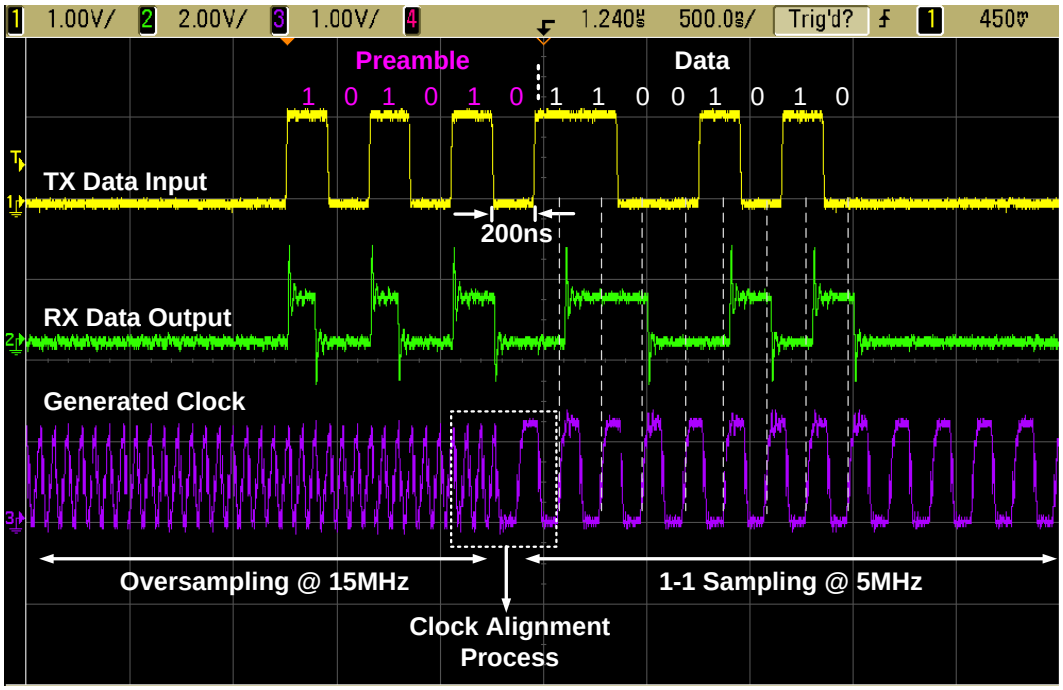


Figure 3.41: Simulation Results of Gain(dB) of Pre-amplifier.

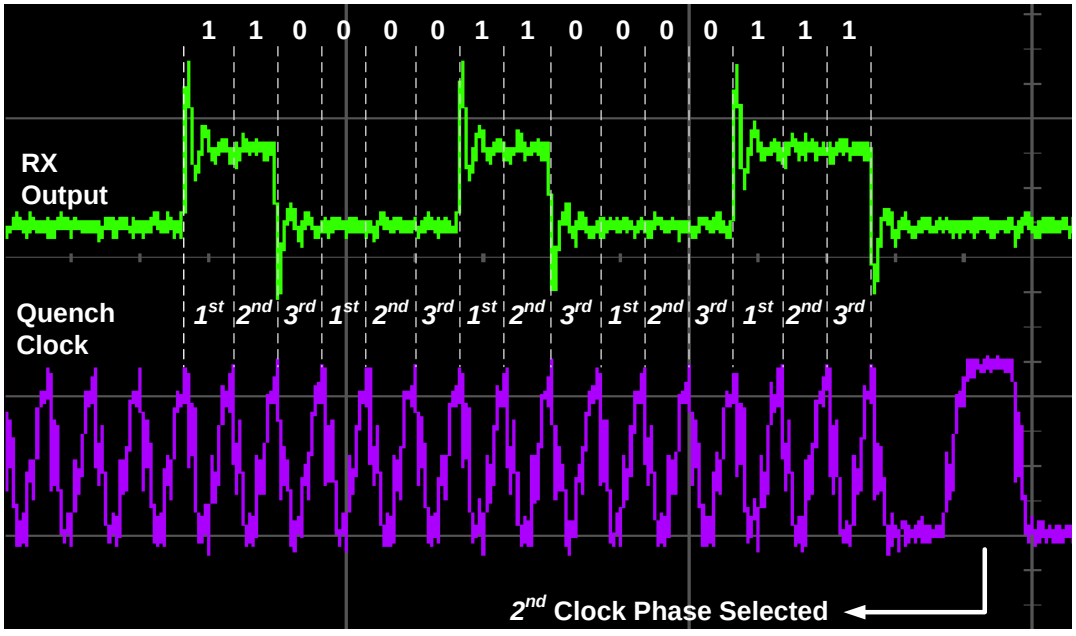
The simulated gain of the pre-amplifier (with capacitive loading from the next stage) is shown in Figure 3.41. As the input data rate is 10-Mbps, the input signal can be approximated to have a bandwidth of 5-MHz signal. The pre-amplifier has a 3-dB gain of about 27-MHz which is sufficient for this data rate.

3.3.2.8 Measurement Results

Quench Alignment Process Fig. 3.42a and 3.43 illustrate the quench alignment process for a 5-Mbps and 10-Mbps input data stream respectively. In the first 5-Mbps test example, 6 preamble bits '101010' and a payload of '11001010' is used. As shown in the zoom in figure of Fig. 3.42b, the preamble is oversampled 3 times. The first and second set of preambles recovered is '1010' which is correct while the third set is incorrect at '0001'. This indicates that the 5-MHz quench clock phases corresponding to the first and second sets are more stable. Therefore, the second 5-MHz quench phase should be selected to recover the payload. This can also be seen in Fig. 3.42a where the rising edges of the 5-MHz quench clock is aligned approximately to the middle of the bit period. A second test example at 10-Mbps



(a) Quench alignment process.



(b) Preamble zoom-in.

Figure 3.42: Quench alignment measurement at 5-Mbps.

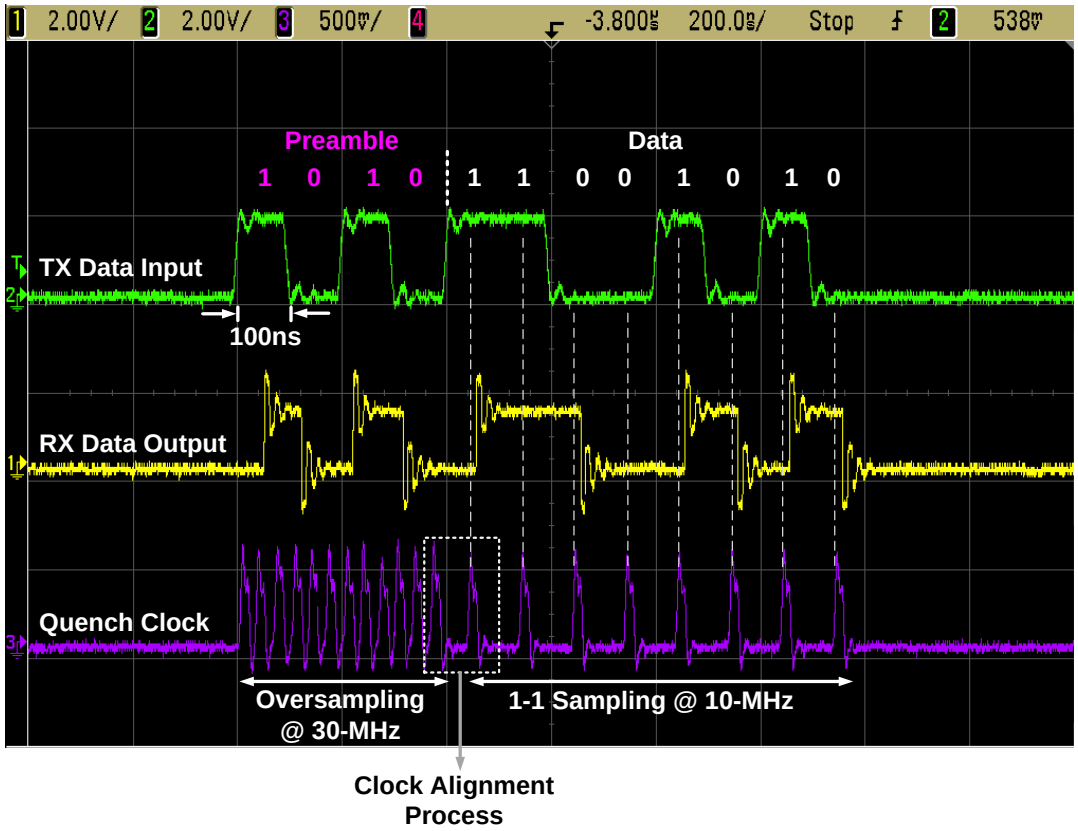


Figure 3.43: Quench alignment process at 10-Mbps.

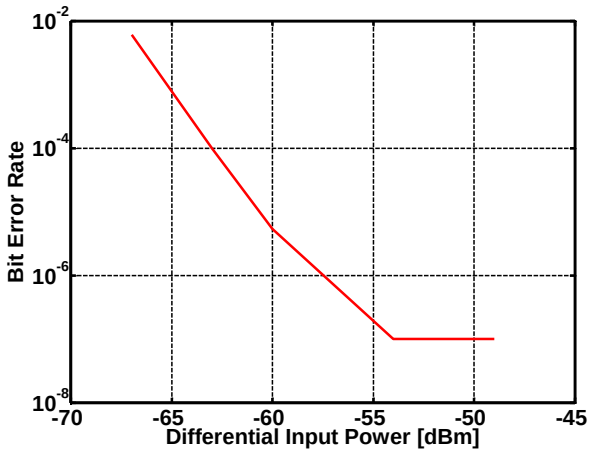


Figure 3.44: Bit error rate measurements of the SRR at 10-Mbps.

with 4 preamble bits of '1010' with correct and synchronous payload recovery is also demonstrated in Fig. 3.43, indicating that the auto-alignment works across various data rates. When the oversampling ratio is reduced from 3 to 1, simulation results show a 66% and 14% reduction in SRO and SRR power consumption, respectively. The order of reduction observed during measurement is in agreement.

Measurements with modulated carrier Fig. 3.44 shows the measurements of the BER of the super-regenerative receiver with a modulated 2.4-GHz carrier. At an input data rate of 10-Mbps, the receiver achieves a bit error rate of 0.1% with a differential input power of -65-dBm.

3.3.3 Conclusion

In this section, we have proposed two low power proprietary OOK receivers that are able to support data rates up to 10-Mbps. The envelope detection receiver is compact and does not require an oscillator, therefore occupying an area of only 0.03-mm^2. It consumes a current of 2.9-mA from a 1.2-V voltage supply, achieving an FOM_{RX} of 0.7-nJ/bit at 5-Mbps.

Table 3.7: Performance Summary of 2.4-GHz Super-Regenerative Receiver

Parameter	Symbol	Specification	Units
Modulation Scheme	-	OOK	-
CMOS Technology	-	65	nm
Frequency	f_0	2.4	GHz
Supply Voltage	V_{DD}	1.2	V
Sensitivity	$P_{RX,MIN}$	-65	dBm
Data Rate	DR	10	Mb/s
DC Power Consumption	P_{DC}	1.7	mW
Energy Efficiency	FOM_{RX}	0.160	nJ/bit

To further improve the energy efficiency, a super regenerative receiver is proposed. The super-regenerative receiver consumes 1.42-mA from a 1.2-V supply at 10-Mbps, achieving a energy efficiency FOM_{RX} of 0.16-nJ/bit. With a fully integrated LC-VCO, the receiver occupies an area of 0.22-mm^2. The super regenerative receiver meets the target specifications meted out.

Table 3.8 summarizes key parameters of receiver performance metrics of recent works. The proposed super-regenerative receiver achieves better or comparable performance with recent works at similar sensitivities at a nominal bit error rate of 10^{-3}.

Table 3.8: Table of comparison for recent OOK receivers.

Parameter	[32]	[33]	[34]	[35]	[36]	[37]	[38]	This Work (1)	This Work (2)
Sensitivity (dBm)	-100.5	-60	-81	-60	-67	-67	-90	-60	-65
Power Consumption (mW)	0.4	2.8	2.1	6.6	*0.5	0.18	9.5	3.48	1.7
Voltage Supply (V)	1	1.2	1.2	1.2	1.2	0.7	1	1.2	1.2
Bit Rate (Mb/s)	0.005	1	11	1.2	5	1	1	5	10
FOM_{RX} (nJ/bit)	80	2.8	0.191	5.5	0.1	0.180	9.5	0.7	0.16
Technology (nm)	-	130	Discrete	130	90	65	130	65	65
Frequency (GHz)	1.9	2.4	2.4	5	2.4	2.4	2.2-2.488	2.4	2.4
Year	2005	2007	2007	2008	2010	2012	2014	2013	2013

∗Only includes RF Front-end

Chapter 4

Conclusion

High data rates and low power consumption is a priority of transceivers in WSNs and WBANS. However, by virtue of the operating frequency, transceiver design in the 433.92-MHz and 2.4-GHz frequency bands have vastly different band regulations and specifications. Power consumption in the 433.92-MHz ISM band is typically lower but emission bandwidth restrictions limit the data rate. On the other hand, operation in the higher frequency 2.4-GHz band require higher power consumption but face less bandwidth limitations. The following sections summarizes the key results of this dissertation and suggests opportunities for future work.

4.1 433.92-MHz Frequency Band

To maximize the data rate in the limited channel bandwidth, a transmitter with frequency calibration is proposed. Frequency calibration allows us to adjust the frequency of the carrier back to the desired value and finer frequency steps would allow the modulated spectrum to be better fitted into the emission mask. To achieve high resolution with reasonable calibration time is the aim of this work.

4.1.1 Original Contributions

- A coarse calibration scheme based on the TVC technique and controlled by the successive-approximation logic is implemented to achieve calibration in less than $<$8.5-µs.
- The proposed frequency calibration scheme overcomes frequency resolution limitations in TVC technique without significantly increasing calibration time by implementing a coarse-fine frequency calibration architecture.
- A fine resolution of $<$140-kHz is achieved by adopting the time-to-digital conversion (TDC) technique, which has not been achieved in previous open-loop frequency calibration systems.
- The calibration scheme achieves a locking range of 54-MHz in $<$18.5-us while consuming only 22.7-nJ.

4.1.2 Future Work

To further improve the data rate that can be fitted into the emission mask, there are several techniques that can be further implemented. First, by pulse-shaping the output transmission pulses through gaussian or commonly used triangular shaping at the oscillator or power amplifier, the occupied emission bandwidth can be reduced [26, 54]. This may allow a higher data rate for the same emission bandwidth. In addition, more bandwidth efficient modulation schemes such as QAM can be adopted such that more information can be transmitted in the same amount of bandwidth.

In addition, to complete the transmitter, a compatible receiver can be designed. Leveraging on the stable and calibrated frequency of the transmitter, the receiver can be allowed to have a smaller input bandwidth. This can potentially be traded off for power savings or improved sensitivities in the receiver.

4.2 2.4-GHz Frequency Band

To achieve low power consumption, low power circuit design techniques are employed to design an energy-efficient transceiver.

4.2.1 Original Contributions

Transmitter :

- An energy-efficient proprietary 2.4-GHz OOK transmitter with an on-chip inductor is designed and implemented.
- It supports data rates up to 10-Mbps with a single-ended output power of -2.2-dBm.
- It achieves energy efficiency of 0.1-nJ/bit.mW that is better than recently published OOK transmitters.
- the transmitter satisfies the emission spectrum mask limits for transmission in the 2.4-GHz ISM band with a PSRB data input of up to 5-Mbps.

Receiver:

- A low power super-regenerative receiver with an automatic timing alignment scheme is proposed. The alignment scheme maximizes the sensitivity and reduces power consumption of the receiver.
- The super-regenerative receiver supports up to 10-Mbps.
- The receiver achieves an energy efficiency of 0.16-nJ/bit, comparable or better with recent works at similar sensitivites.

4.2.2 Future Work

To further achieve better energy efficiency in the transmitter, off-chip inductors or bondwire inductances with much higher quality factors can be used. By

implementing speed-up circuit techniques to increase the data rate much beyond 10-Mbps, the effective energy per bit can also be potentially reduced. Similarly, the energy efficiency of the super-regenerative receiver potentially can be improved by increasing the data rate. At the same time, automatic gain calibration can also be implemented to achieve robust operation and also potentially lower power consumption in the face of unstable channel conditions.

Last, to complete the proprietary 2.4-GHz transceiver, a baseband layer with the necessary channel encoding and receiver alignment circuit can be designed and implemented on chip to achieve a truly system-on-chip solution.

List of Publications

[1] M. Kumarasamy Raja, D. Chua, and Y. Xu, ”A 52-pJ/bit 433-MHz low power OOK transmitter,” *Analog Integrated Circuits and Signal Processing*, vol. 70, no. 1, pp. 57C67, 2012. [Online]. Available: http://dx.doi.org/10.1007/s10470-011-9637-2

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[3] D. Chua, R. Pan and Y. P. Xu, ”A 1-Mbps 433.92-MHz ISM Transmitter with SAR-TDC Frequency Calibration”, Journal recommended for resubmission to TCAS-I and under revision.

[4] D. Chua, R. Pan and Y. P. Xu, ”A 2.4-GHz 0.2-nJ/bit Super-Regenerative Receiver with Automatic Quench Alignment”, Journal submitted to TCAS-II.

[5] R. Pan, D. Chua and Y. P. Xu, ”A QoS-Aware Real-Time Scalable Network Controller IC for Multi-Patient Wireless Vital Signs Monitoring”, Journal submitted to TBCAS.

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