INFLUENCE OF SILICON NANOSTRUCTURES ON THE GROWTH OF GAN ON SILICON

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NATIONAL UNIVERSITY OF SINGAPORE

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DECLARATION

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which has been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Wee Qixun

14 November 2013

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Summary

GaN has several applications, such as light-emitting diodes (LEDs), laser diodes (LDs) and high-electron mobility transistors (HEMTs). Silicon, as a cheaper substrate than sapphire and SiC, is becoming a more common substrate for GaN, but the intrinsic differences between the two materials created integration problems. It is known that forming nanostructures on the substrate can induce better crystal quality through nanoheteroepitaxy; hence, an investigation on how silicon nanostructures can influence the subsequently grown GaN was done.

One-step metal-assisted chemical etching (MACE), was used to create the silicon nanostructures. The etching conditions were varied in order to investigate on the nanostructure formation process. It was found that the activation energy of the one-step MACE reaction is 0.33 ± 0.02 eV, and evidences were found that the rate limiting reaction of one-step MACE resembles that of etching SiO_2 in HF.

Two distinct regimes, with different etch rates, were found for the etching of silicon by one-step MACE, namely short etching time regime (1.51 nm/s) and long etching time regime (2.70 nm/s). Size variation was also found with etching duration. A suitable etching condition (5.0 M HF and 0.02 M $AgNO_3$ at 25 ℃ with no stirring) was chosen for subsequent GaN growths, for its reliability in producing nanostructures up to about 1.5 μm.

AlN deposition was performed on the nanopatterned substrates. It was found that a single large AlN crystal (> 100 nm) can be grown on the tip of a silicon nanostructure (with diameter < 40 nm) when growth rate was reduced to 180 nm/h. It was also found that the AlN nucleation layer on nanopatterned substrate cannot be thick (about 200 nm), or subsequent GaN film coalescence is difficult. GaN film coalescence was possible with 60 nm of AlN nucleation layer (with an additional 200 nm of AlGaN

layer to avoid meltback etching). In addition, GaN film coalescence could not be obtained when grown on substrates with nanostructures taller than 300 nm.

Three different MOCVD growth sequences were implemented on silicon substrates patterned with 100 nm tall nanostructures, and their GaN quality were compared. Among the samples, Sample III (one with graded AlGaN buffer layers) was found to have the lowest biaxial tensile strains and lowest dislocation density among the nanopatterned substrates. The large air voids observed in between the nanostructures of Sample III was deduced to have aid in the strain reduction. However, the overall GaN quality (based on dislocation density) on nanopatterned silicon substrates was worse than that on flat silicon substrates.

GaN growth was then done on 50 nm tall nanostructures. GaN on 50 nm nanostructures was found to also have an overall tensile strain reduction and dislocation density reduction, when compared to that on a flat silicon. However, screw dislocation density of GaN on 50 nm nanostructures was found to be higher than GaN on flat silicon. The RMS roughness of the GaN film on 50 nm nanostructures is also found to be worse than GaN films on flat silicon (1.70 nm compared to 0.364 nm).

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List of Symbols

a_{GaN}: lattice parameter of wurtzite GaN, parallel to the basal plane

a_{Si}: lattice parameter of Si

b: magnitude of the dislocation's Burger's vector

c_{GaN}: lattice parameter of wurtzite GaN, normal to the basal place

D: diffusivity

d: inter-planar spacing,

E_a: activation energy

E_D: areal energy density of a screw dislocation

E_{epi}: maximum strain energy density per unit area of epilayer

ΔE_g: change in band gap

$\boldsymbol{g}$: diffraction vector

h: Planck's constant

h: thickness

k: Boltzmann's constant,

k_{epi}: interfacial compliance parameter, from reference [51]

$\boldsymbol{k_i}$: wave vector of incident beam

$\boldsymbol{k_d}$: wave vector of diffracted beam

l: mean free path

m_e: mass of electron

N: concentration

P: pressure

P_b: bubbler pressure (in Pa)

Q_b: volume flow rate of carrier gas into the bubbler (in sccm)

q: elementary charge

R: ideal gas constant (=8.314 J mol^{-1} K^{-1})

R: closest distance from the dislocation to a free surface

$\dot{R}$: growth rate

r: radius

$\boldsymbol{S}$: vector representing a reciprocal lattice point

T: temperature

U: gas velocity

V: accelerating voltage

v: velocity

w_D: effective interfacial width of the dislocation

Y: Young's modulus

δ: boundary layer thickness

ε: strain

θ: angle between the incident beam and the planes of atoms

λ: wavelength

λ_e: electron wavelength

ν: Poisson ratio

ρ: molar ratio defined as [HF]/([HF]+[H_2O_2]) by reference [175]

σ: biaxial stress

σ_f: fracture strength

ϕ: rotation angle of the sample, where its axis normal to sample surface

χ: tilt angle of the sample, where its axis is the interception of diffraction plane and sample surface

ω: angle between the incident beam and sample surface

$\Delta\omega$: Raman shift

Chapter 1. Introduction

1.1 Introduction and motivations for growing GaN on silicon

GaN was touted to be a very promising compound semiconductor, when, almost half a century ago, it was discovered to have a large direct bandgap of 3.42 eV [1, 2]. Eventually, the scientific community realized that alloys of GaN with AlN and/or InN would provide a material system with direct bandgap ranging from 0.7 eV to 6 eV [3, 4] (it should be pointed out that the bandgap of InN was realized to be at about 0.7 eV only a decade ago [5]). Such a material system allows the realization of optical devices which operates in the infra-red, to visible and to ultraviolet wavelengths. The large bandgap and high electron mobility of GaN [6] also led to the development of field-effect transistors and high electron mobility transistors [7, 8] capable of operating at high temperatures [9].

Native GaN substrates are still not widely available as it is difficult to grow large single crystal of GaN, due to its requirement to grow at high temperatures because of its strong atomic bonding and high melting point [10]. A high nitrogen pressure is required at the growth temperatures to suppress decomposition of GaN [3, 4, 11], which makes it difficult to grow GaN substrates. Hope for GaN's future was ignited after Amano and his co-workers [12] managed to grow high quality GaN on sapphire by using metalorganic chemical vapor deposition (MOCVD). Subsequently, a plethora of researches were focused on GaN growth [13-18] on foreign substrates. The ideal substrate should be as similar as possible to the target material, GaN (or more specifically wurtzite structure GaN). The material properties important for substrate consideration include crystal structure, lattice constants, coefficient of

thermal expansion and thermal stability. So far, the best results are attained on silicon carbide (SiC), sapphire and, more recently, silicon.

Silicon carbide crystals are comprised of covalently bonded silicon and carbon atoms, of which their unit cell consists of one carbon atom attached to 4 silicon atoms in a tetrahedral structure. SiC has many polytypes, differentiated by the stacking order of atoms in the c-direction. The more common SiC polytypes available are 6H-SiC and 4H-SiC. As both polytypes' c-planes have hexagonal atomic arrangement, they are both suitable substrates for the wurtzite GaN. The lattice mismatch is about 3.5%, and the thermal expansion strain is about 0.01% for 6H-SiC and 0.03% for 4H-SiC [4], sustained by cooling from growth temperatures (about 1000 ℃) to room temperature (about 25 ℃). This means that GaN will sustain a residual tensile strain upon cooling from growth temperatures.

Sapphire (chemical formula Al_2O_3) assumes a trigonal lattice structure where its hexagonal cell has 12 aluminum atoms and 18 oxygen atoms, held together by ionic bonds (see Figure 1-1). The O atoms form an approximate simple hexagonal close packed arrangement, whereas the Al atoms occupy two-thirds of the octahedron sites in between the O atoms. The apparent lattice mismatch between the sapphire's unit cell and GaN unit cell is at more than 30%. However, growth of GaN on sapphire is aligned to its Al atoms, which is rotated 30 ° from the sapphire unit cell. Therefore, the actual lattice mismatch is at around 16%. The thermal expansion strain is about −0.18% [4], sustained by cooling from growth temperatures (about 1000 ℃) to room temperature (about 25 ℃). The minus sign of the strain indicates the GaN is subjected to residual compressive strain.

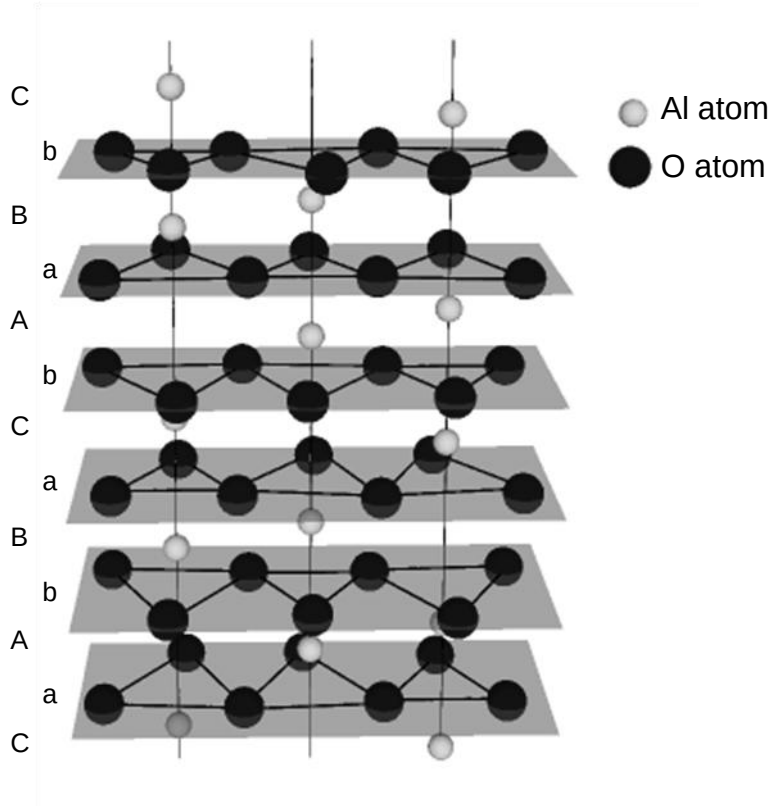

Figure 1-1. A schematic of the atomic arrangement of sapphire, where the oxygen atoms forms an approximate simple hexagonal close packed arrangement, and the aluminum atoms occupies two-thirds of the octahedron sites in between the O atoms. Figures adapted from reference [19].

Silicon has a diamond lattice structure with a cubic unit cell. Each unit cell contains 8 silicon atoms, where they are covalently bonded in a tetrahedron fashion. For GaN growth, Si(111) substrates are widely used, instead of the more common Si(001) substrates. This is because Si(111) plane contains hexagonally arranged atoms, similar to the c-plane of GaN and GaN is predominantly grown in the c-direction. The lattice mismatch is about −16.8% and thermal expansion strain is about 0.19%, sustained by cooling from growth temperature (about 1000 ℃) to room temperature (about 25 ℃). The positive sign of the thermal expansion strain shows that GaN will contracts more than silicon during cooling down, sustaining residual tensile strains.

The importance of GaN is explained in the following sections followed by the reasons for using Si as a substrate and the challenges that have to be overcome to grow GaN

on silicon. Nanopatterning the silicon substrate is then introduced as a topic of research, to investigate its influence on the subsequently grown GaN.

1.1.1 Benefits of GaN

GaN has several intrinsic characteristics which encourage its usage. It is both chemically and thermally stable. Its related alloys ($(Al_xGa_{1-x})_yIn_{1-y}N$) can be tuned to have direct bandgap from 0.7 eV all the way to 6 eV. This is a very large range for any single material system. In addition, it can achieve reasonably high optical emission efficiencies even with high dislocation density [20].

GaN is a III-V compound semiconductor made up of two elements, group III gallium and group V nitrogen. GaN has several properties that are ideal for making optoelectronic devices [21]. It has direct bandgap (giving rise to high radiative recombination efficiency), a large bandgap (capable of emitting ultraviolet and blue emission), high thermal conductivity (improved device reliability for high power devices) and chemical stability (suitable for operation in harsh environment).

1.1.1.1 Chemically and thermally stable

GaN is a very stable material which can endure relatively harsh chemical conditions, even at high temperatures. The thermal stability of GaN allows high temperature processing as well. However, the chemical stability of GaN also makes wet etching unsuitable. Hence, dry etching is usually used for processing of GaN material.

1.1.1.2 Adjustable direct bandgap when alloyed with InN and AlN

GaN and its associated alloys, like AlGaN and InGaN, have direct bandgaps. Direct bandgap material can have carriers recombine directly, with no loss of momentum. The energy loss from the recombination, which is equal to the bandgap energy, will be emitted in the form of a photon. This is called radiative recombination. In the case of indirect bandgaps, recombination is usually non-radiative. Although radiative

recombination is possible for indirect bandgap material through mediation of defects [22], for example, it is not preferred as this mechanism is comparatively inefficient. Hence, having direct bandgap is a prerequisite for building efficient light-emitting diodes (LEDs).

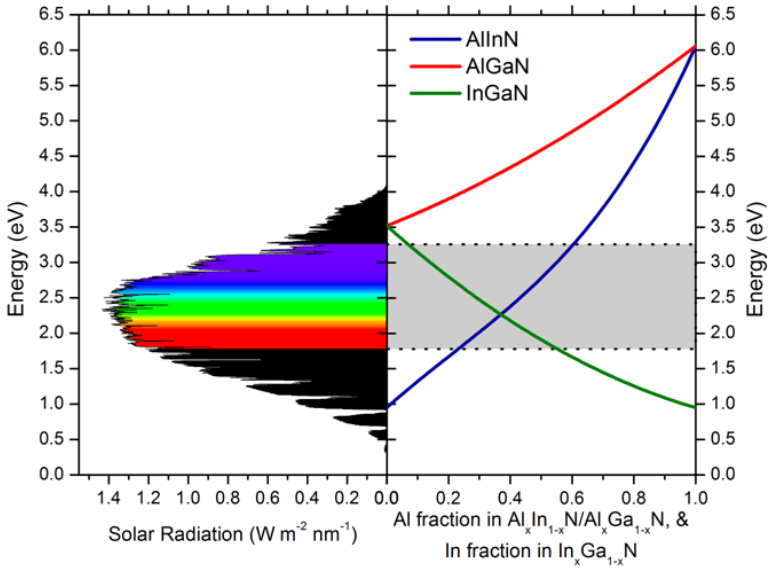

Figure 1-2. A plot of ASTM G-173-03 direct beam AM1.5 solar spectrum flux [23] (left) compared with a plot of bandgap energies of $Al_xIn_{1-x}N$, $Al_xGa_{1-x}N$ and $In_xGa_{1-x}N$ alloys (right), determined by reference [24]. The two adjacent graphs show complete coverage of the visible light spectrum and almost complete coverage of the solar spectrum. The corresponding visible light colors are added into the solar spectrum flux for illustration. Graph presentation adapted from reference [25].

GaN has a bandgap of 3.4 eV and it can form a ternary alloy with another III-V compound such as indium nitride (InN) and aluminum nitride (AlN), which has a bandgap of 0.7 eV and 6.2 eV respectively [26]. $In_xGa_{1-x}N$ (and $Al_xIn_{1-x}N$) bandgap spans the whole of the visible light spectrum (see Figure 1-2). This makes this alloy suitable for light production, as any of the visible light could be achieved by simply adjusting gallium, aluminum and indium content in the material. However, there is still the miscibility gap problem in InGaN alloy, where InGaN phase separates into

two phases (high indium content InGaN and low indium content InGaN). It still posed as a challenge to achieve InGaN with high indium content.

1.1.1.3 High efficiency even with high dislocation density

One remarkable characteristic of the III-nitrides is the material's ability to produce light at high efficiency, even though it has a high dislocation density [27]. Lester and his co-workers found out that the early LEDs fabricated by Nichia had very high dislocation densities [20]. They estimated the dislocation density to be between 2 and 10×10^{10} cm^{-2}. This was a pleasant surprise to the LED research field. For comparison, a dislocation density of more than 10^6 cm^{-2} in AlGaAs LEDs would have caused external quantum efficiency to drop to less than 1% [28]. On this aspect, a comparatively highly defective III-nitride material had been shown to produce light at about 40% efficiency [29].

1.1.2 Benefits of silicon as a substrate

The reason for silicon's involvement is cost reduction. GaN is typically grown on sapphire or silicon carbide substrates, which are expensive and only come in small wafer sizes (up to 4 inch for SiC wafers and 6 inch for sapphire wafers). Conversely, silicon is comparatively cheap and the technology to produce large silicon wafers is available (400 mm for Si(100) wafers). The maturity of the silicon industry enables varied kinds of silicon wafers to be fabricated: highly doped, conductive or insulating. Silicon is also relatively easy to do post-deposition processing for, due to the mature processing techniques in the silicon industry. In addition, having compound semiconductors grown on silicon would advance us towards integrating III-V materials and silicon, providing the possibility in harnessing the advantages of both types of materials in a single device.

As cost reduction is an important factor when developing device improvements, silicon is portrayed as a very promising replacement substrate for sapphire for nitride-based devices.

1.1.2.1 Low cost material

The conventional substrates for III-nitrides, like sapphire and SiC, cannot be made into large wafer sizes, due to technological limitations. The largest wafer size available for sapphire is 6 inches and for SiC is only 4 inches. In contrast, silicon substrates can be produced at sizes up to 400 mm. The availability of such large-area substrates would bring about savings in terms of economies of scale.

Table 1-1. Prices of various wafers. Prices were obtained from University Wafer's website [30].

Wafer sizes	Silicon (100)	Silicon (111)	Sapphire c-plane	6H-SiC (0001)
2 inch	US$4.90	US$6.90	US$19.90	US$327.80
4 inch	US$9.90	US$16.90	US$109.00	N.A.
6 inch	US$13.90	US$18.90	N.A.	N.A.
Cheapest price per area (per inch^2)	US$0.49	US$0.67	US$6.33	US$104.34

In addition to having large wafer sizes, the abundance of silicon and highly developed silicon growth technology also makes silicon a cheaper choice. Comparing the prices per unit area (see Table 1-1), silicon is cheaper by about 10 times than sapphire and more than 100 times than SiC substrates. This is attributed to the mature silicon industry, which enabled highly optimized and cost-efficient fabrication of high quality silicon substrates.

Other than just the raw production cost, processing with silicon is also easier and cheaper than with other competing substrates. Once again, the lower cost of processing is partly because of the matured silicon industry.

1.1.2.2 Flexibility in conductivity control

Another benefit of using silicon as a substrate is that its conductivity is customizable. Silicon's conductivity could be changed easily by adjusting its doping level. This versatility allows conductivity to be modified according to the needs of the final device. For example, a high electron mobility transistor (HEMT) would require a substrate with low conductivity to minimize leakage current, and a LED might benefit from a high conductivity substrate for the possibility having the back of the substrate as an anode.

1.1.2.3 Good thermal conductivity

Other than the cost factor, silicon also possesses good thermal conductivity at about 150 W m^{-1} K^{-1}, as compared to sapphire's 23 W m^{-1} K^{-1}. This property promotes heat dissipation for GaN devices, ensuring the devices' longevity. However, it should be noted that 6H-SiC (another suitable substrate for GaN) has a much larger thermal conductivity at 490 W m^{-1} K^{-1}. For reference and comparison, GaN's thermal conductivity is between 200 and 230 W m^{-1} K^{-1} [31, 32].

1.2 Problems with integrating the two materials

However, due to the intrinsic differences between the two materials, integration of GaN and silicon is not easy. There are many problems associated from growing GaN-based material on silicon substrates. Material property differences such as the coefficient of thermal expansion, lattice constants and crystallographic structure pose a huge challenge to integrating the two materials. Such incompatibilities lead to highly defective GaN films [4], causing problems for devices, such as current leakage and depletion of two-dimensional electron gas (2DEG) channel of HEMTs [33-36]. These incompatibilities will be described in the following sections.

1.2.1 Meltback etching

Ga and Si react with each other at high temperatures (observed at around 1000 ℃) resulting in meltback etching of silicon [27, 37], forming deep voids in the substrate. Low-temperature GaN (LT-GaN) growth is commonly used for sapphire substrates to obtain high quality GaN, but that would not work for silicon substrates [37, 38]. Ishikawa et al. [37] reported that when a LT-GaN buffer layer grown on silicon is heated to the GaN's MOCVD growth temperatures, the surface became rough due to meltback etching. They deposited a low temperature GaN layer as a nucleation layer, the method used for GaN on sapphire, and found out that the silicon surface degraded and roughened upon heating up to growth temperatures. They argued that the LT-GaN decomposed at high temperatures and the resultant gallium metal caused the deterioration of the substrate. However, the exact mechanism for this meltback etching is unclear.

1.2.2 Lattice mismatch

A heteroepitaxial film is formed when the film and substrate are of different materials. Usually a lattice mismatch exists between the film material and the substrate's material, but it is also possible to get a lattice-matched heteroepitaxial films. One such material system is $Ga_{0.5}In_{0.5}P$ on GaAs [39]. However, the choice of materials will be very limited if we constrained ourselves to use only lattice-matched material systems. For lattice-mismatched material systems, strains and defects will inevitably be introduced in the deposited films. GaN on silicon is such a case.

Silicon and GaN do not only have lattice mismatch, they are also of different crystal structure type. Silicon atoms are arranged in a cubic diamond lattice structure whereas GaN atoms are arranged in a hexagonal wurtzite lattice structure. Despite the intrinsic differences, the atomic arrangement in the Si(111) plane is in a 2D triangular lattice, which is compatible with the GaN(0001) plane or c-plane (see Figure 1-3).

Hence, Si(111) substrates are usually utilized for growing GaN. If Si(100) substrates are used, deposition results in mixed phases (containing both wurtzite and zinc blende phases [40]) and/or mixed orientations [41] of GaN. However, aligning Si(111) plane and GaN c-plane still does not solve the large lattice mismatch between silicon and GaN.

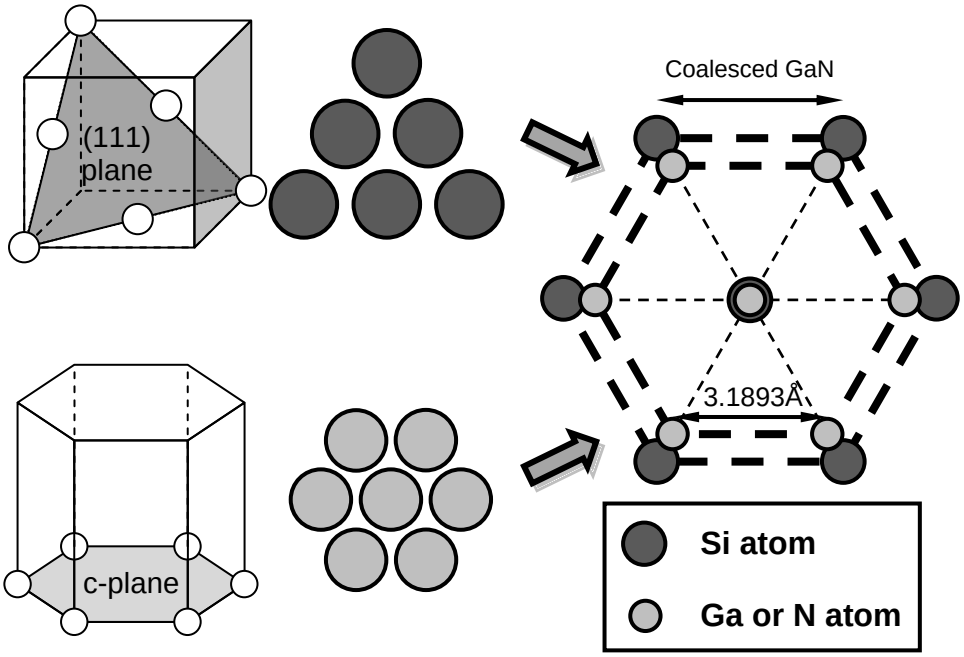

Figure 1-3. Schematic comparing the lattice distance between silicon atoms on its (111) plane and GaN atoms on its c-plane.

From the literature, the lattice constants for GaN are a_{GaN} = 3.1893 Å and c_{GaN} = 5.1851 Å, and for silicon is a_{Si} = 5.4309 Å [4]. As the crystal structures of both materials are different (one hexagonal and one cubic), the lattice constants have to be converted to calculate the effective lattice mismatch. The new lattice constant a_{Si}' = $(\sqrt{2}/2)$ a_{Si} = 3.8402 Å. The lattice mismatch is about 17%. Such a high lattice mismatch causes a high density of defects [42, 43], which will be detrimental for any devices built upon it.

1.2.3 Coefficient of thermal expansion mismatch between silicon and GaN

Thermal mismatch is a major problem because of the high GaN growth temperature (~1000 ℃) in MOCVD. The mismatch in coefficient of thermal expansion will result in residual strains. Films can be deposited in a relaxed state at high growth temperatures, but strain will build up during cooling to room temperature. Since the coefficient of thermal expansion of silicon (2.616×10^{6} K^{-1}) is smaller than that of GaN (5.59×10^{6} K^{-1}), GaN shrinks more than silicon during cooling, creating high tensile stress in GaN. It is estimated to create a thermal strain of 0.19% [4]. Such a large thermal strain will result in extensive cracking of GaN film grown on silicon, if the film is grown beyond 1 μm in thickness [44, 45].

1.2.4 Nitridation of silicon

In MOCVD growth of GaN, ammonia is used as the source gas. A problem arises when silicon is exposed to ammonia at the typical growth temperatures. Silicon and ammonia will react to form silicon nitride at elevated temperatures [46, 47].The silicon nitride, usually amorphous, does not allow GaN to form an epitaxial relationship with the silicon beneath [27]. Hence, nitridation of silicon is detrimental to the subsequent growth of single crystal GaN.

1.3 Scope of work and thesis organization

The objective of this thesis is to investigate the effectiveness of using simple-to-fabricate nanopatterned silicon as a substrate for III-nitride materials. However simple methods are required to establish optimized etching conditions to suit the needs for III-nitride epitaxy growth. Therefore, despite the plethora of research in literature dedicated to nanopatterning, there is still a need to investigate silicon nanostructures fabrication, specifically geared toward the aim of making it a suitable substrate.

Similarly, although research on growth of GaN (or III-nitrides in general) on silicon has been extensive and the process has matured into mass production industrially, a limited GaN research has been dedicated toward nanopatterned silicon substrates.

Research on growth GaN (or III-nitrides in general) on silicon has been extensive and the process has matured into mass production industrially; however the dislocation density of GaN on silicon is still high (typically above 10^8 cm^{-2} [48]) and thick buffer layers are required to provide strain reduction [49]. Hence, it is important to dedicate time and effort to investigate on other methods to reduce dislocations and strains. As nanopatterned substrates are known to aid in stress relaxation and defects reduction in deposited films [50-54], it is worth exploring the formation of III-nitrides on nanopatterned silicon substrates. There will be a more detailed discussion on stress and defects reduction in the later part of this thesis (in Section 2.4, Chapter 2).

In Chapter 2, a broad-based review of the existing methods and techniques for GaN growth on silicon will be presented. There will be a strong emphasis on MOCVD growth, because this is the deposition technique used in industry. Due to the intrinsic incompatibilities between GaN and silicon, special efforts in deposition are mandatory. In addition, an introduction to the benefits of nanostructured substrates, together with a literature review on research which leverages the advantages of

nanostructuring for III-nitride growth is also given. Chapter 3 includes the relevant basic theories and working principles for MOCVD growth and several characterization tools. In Chapter 4, a systematic investigation of electroless etching of silicon will be presented and discussed. In Chapter 5, results for GaN deposition on the prepared silicon nanostructures will be presented, with corresponding material characterizations and explanations. Finally, Chapter 6 summarizes the significance of this study and proposes suggestions for future work.

Chapter 2. Techniques to grow GaN on silicon and introducing nanostructures strategies

2.1 Existing growth techniques and solutions for GaN-on-Si

Although there are several difficulties involved in growing GaN on silicon (as discussed in the previous chapter), the cost benefit of using silicon as a substrate is still very attractive. Hence, the research community for GaN on silicon has continued working on this material system and found solutions (or partial solutions) to the problems stated in the previous chapter. The solutions include the use of thermally stable nucleation layers, in-situ silicon nitride masking, strain engineering and epitaxial lateral overgrowth (ELO). The development of GaN on silicon has progressed greatly such that some devices based on this material system, such as LEDs and HEMTs, are already commercially available.

In this chapter, existing growth techniques are presented and it is explained how they overcome the problems of growing GaN on silicon. Nanostructured silicon surfaces are then presented as a promising technique to overcome some of the problems which GaN growth on silicon faces. A brief literature review is presented on what has been done by researchers who have used nanostructured surfaces for GaN growth on silicon.

2.1.1 Nucleation layer or protection layer

As stated in the previous chapter, it is unsuitable to grow GaN directly on silicon due to meltback etching and formation of amorphous silicon nitride. In addition, GaN is

found to be unable to wet silicon surfaces [55]. Hence, another material is required as the nucleation layer. The material must be able to avoid the meltback and silicon nitridation problems, while also aid in accommodating lattice mismatch and alignment of crystal orientation [27]. Therefore, the material needs to be able to completely cover silicon's surface while maintaining stability at the growth temperature (about 1000 ℃). The most common material of choice is AlN.

2.1.1.1 Utilization and optimization of AlN as nucleation layer

Amano et al. were the first to report the use of AlN as a nucleation layer for growth of GaN on sapphire in 1986 [12]. Subsequently, Watanabe et al. [56] reported the first use of an AlN nucleation layer for GaN growth on silicon in 1993, after which AlN nucleation layers were widely used for GaN growth on silicon [55, 57-67]. AlN is a suitable nucleation layer for silicon, as it forms a continuous film on silicon [67] and maintains stability at high growth temperatures [3, 68]. It can protect the silicon underneath from meltback etching and provide a suitable seeding layer for GaN films. Growing AlN requires ammonia, which could cause nitridation of silicon [64]. Hence, the silicon substrate is often exposed to the aluminum source for a short time before starting the AlN deposition [38, 62, 65]. This preflow of the aluminum source is to deposit an aluminum layer on the silicon surface, which prevents nitridation of the silicon.

Optimization of AlN nucleation has been reported in several works. It was found that the growth temperature which produced the best quality AlN deposited on silicon is 1150 ℃, yet the best quality GaN was obtained on AlN grown at 1060 ℃ [59]. The duration of the preflow of the aluminum source has to be optimized, as too short a period might not prevent silicon nitride formation and too long a period would roughen the subsequent AlN deposited [62]. It was reported that the optimal preflow duration for trimethylaluminum (TMAl) is 5 s [62]. However, some reports the

optimum AlN growth temperature to be as low as 850 ℃ [55] instead. Hence, there appears to be two possible ranges of AlN growth temperatures, where good GaN quality can be obtained from either a low growth temperature (between 720 to 850 ℃) [38, 45, 55, 60, 65, 69-71] or a high growth temperature (between 1010 to 1100 ℃) [44, 61-63, 72-76], but not at intermediate growth temperatures [59].

The optimum thickness of AlN is not consistently reported in the literature. Some literature reports the optimum AlN thickness to be as thin as 10 nm (grown at 850 ℃) [55], yet some reports the optimum AlN thickness to be 160 nm [66]. While the AlN thickness for a high temperature AlN (HT-AlN) nucleation layer is not consistent, the AlN thickness for a low temperature AlN (LT-AlN) nucleation layer is reported to be in a tight range of 10 and 30 nm.

2.1.1.2 Other materials as nucleation layers

Other researchers also have found success without using nitrides as nucleation layers. The usage of AlAs as a nucleation layer was first reported by Kobayashi et al. [77] However, they did not directly deposit GaN on AlAs; they oxidized the layer into aluminum oxide prior to GaN growth. Unfortunately, oxygen impurities were found to exist in the GaN layer using cathodoluminescence measurements. Subsequently, Strittmatter et al. [78, 79] reported using 20 to 30 nm of AlAs as a nucleation layer by depositing GaN directly on this layer. The resultant GaN grown had a full width at half maximum (FWHM) of 2700 arcsec for an X-ray rocking curve of the GaN(0002) reflection. Although AlAs is found to be thermally stable and promising, the adoption of AlAs as nucleation layer has not continued.

As silicon carbide is known to be a suitable substrate for GaN growth, research efforts were done to form silicon carbide as a nucleation layer on silicon [80-83]. The first reported use of silicon carbide as a nucleation layer for GaN on silicon was by Takeuchi et al. [80], where they deposited 200 nm of silicon carbide as a nucleation

layer. Subsequently, carbonization was introduced to convert the silicon surface to silicon carbide, prior to deposition of the silicon carbide nucleation layer [81, 82, 84-86]. It should be noted that the researchers still utilized an AlN seeding layer on top of the silicon carbide, until in 2009 where low temperature GaN was used instead [83]. Nucleation layers are required on silicon carbide because direct deposition of high temperature GaN on silicon carbide results in high surface roughness [87]. However, strangely, Takeuchi et al. [80], who pioneered the use of silicon carbide as a nucleation layer, reported success in depositing GaN directly on a silicon carbide nucleation layer without AlN nor any other techniques to improve surface morphology.

2.1.2 In-situ silicon nitride masking

In-situ silicon nitride masking is a method pioneered by Gibart's group in France [88, 89], although this term was coined by Dadgar et al. [70] in 2002. In-situ silicon nitride masking is a simple technique to improve the quality of GaN, where no lithographic step is required [90]. In this technique, the growth is interrupted with a short duration silicon nitride deposition. This deposition is designed to form a thin, discontinuous silicon nitride layer on the surface. GaN growth is then carried out on areas not covered by silicon nitride, forming isolated GaN islands. Hence, the modification to the surface forced GaN to deviate from 2D film growth into 3D island growth [90]. These isolated islands grow laterally and coalesce to form a continuous GaN film. Similar to ELO [91-93], in-situ silicon nitride masking reduces dislocations by allowing GaN to grow without constraints from the underlying highly mismatch substrate.

Hageman et al. [55] found out that the insertion of a silicon nitride layer reduced the FWHM of D^0X (donor bound exciton) photoluminescence peak from 17.6 meV to 10 meV, and the photoluminescence intensity increased by a factor of 2.5. The FWHM

of the omega-scans for (0002) and ($10\bar{1}5$) rocking curves also decreased by about 20%. Improvement in LED performance of about a factor of 5 was shown when a silicon nitride mask was used [70].

Contreras et al. [94] convincingly showed the effect of silicon nitride masking through cross-sectional transmission electron microscope (TEM) images. While threading dislocations with edge components were not affected, the silicon nitride masking layer was shown to reduce threading dislocations with screw components by about 70%. It was proposed that silicon nitride preferentially deposits on the step edges and threading dislocation sites (which extend to the surface), as it is energetically favorable [95] to do so. The presence of the silicon atoms pinned the dislocation to the silicon nitride layer and, if possible, combined with another screw dislocation (of the opposite Burgers vector) to create a dislocation loop. This reduced the threading screw dislocation density.

On top of dislocation density reduction, it was also found that a silicon nitride masking layer also reduced the tensile stress of the GaN by up to 0.53 GPa [69]. It was expected to reduce tensile stresses because silicon nitride masking encouraged the formation of larger islands. As island coalescence contributes to the tensile stresses [96, 97], larger islands translate to fewer coalescence boundaries, which in turn reduces coalescence-induced tensile stresses. The incorporation of a silicon nitride masking layer after deposition of AlN nucleation layer was also observed to reduce tensile stresses [69].

However, the disadvantage of silicon nitride masking was that a thicker GaN is then necessary for GaN to coalesce to form a continuous film. Nevertheless, a thinner silicon nitride masking layer [69] and an adjustment to the V/III ratio [94] could reduce the thickness necessary for GaN to coalesce. As reduction of the masking layer results in smaller island size at coalescence, which in turn reduces its effect on

strain and dislocation reduction, a suitable duration for silicon nitride deposition should be chosen to achieve the required balance between strain and dislocation reduction and coalescence time reduction.

2.1.3 Superlattice

Superlattices are periodic structures consisting of thin layers made of different materials. Since a critical thickness is required before a dislocation nucleates [98], having thin layers will avoid nucleation of dislocations, as long as they are below the critical thickness. Such a structure could be grown indefinitely for materials with lattice mismatch, in theory [99], even if the strains exist in the layers. Therefore, a superlattice of GaN and AlN could provide compressive strain to compensate for the tensile strain in the nitride film on silicon [76]. Feltin et al. reported that a superlattice consisting of 10 periods of AlN/GaN contributed 215 MPa of compressive stress [76]. Jang et al. [75] reported that their optimized superlattice was 20 periods of $Al_{0.3}Ga_{0.7}N$/GaN with a total thickness of 60 nm. Superlattices have also been observed to decrease dislocation densities by 2 to 3 orders of magnitude (from greater than 10^{12} to 10^{9}-10^{10} cm^{-2}) [100, 101].

2.1.4 Compressive LT-AlN interlayer

To avoid cracking of deposited films due to residual thermal strain, strain engineering is employed [27, 38]. Tensile stress is prevalent in GaN films on silicon due to its formation from coalescence of islands [102], GaN's larger coefficient of thermal expansion, and also from n-type doping with silicon [103]. The tensile stress arises from silicon doping because silicon atoms block the movement of dislocation, preventing dislocation movement [104, 105] to relieve coalescence stress. The residual tensile stress causes cracking of GaN films, which is a problem for device fabrication.

Strain engineering is applied by inserting low temperature AlN (LT-AlN) interlayers. The LT-AlN interlayer ingeniously compensates for the residual tensile stress [71]. Blasing et al. explained that the LT-AlN interlayer is relaxed at the deposition and subsequent high temperature GaN grown would be compressively strained due to the smaller lattice of AlN. The LT-AlN interlayer serves as a buffer between the bottom and top GaN layers, avoiding the translation of any strains from the underlying layers to subsequent top layers. AlN deposited at lower temperature can induce higher compressive strains to compensate for the tensile residual thermal stresses in GaN grown on top. The inclusion of this interlayer can thus avoid cracking in GaN films. Dadgar et al. [45] obtained a crack-free GaN film by incorporating a 15 nm thick LT-AlN interlayer, where a sample without the LT-AlN had a crack density of 240 mm^{-2}.

The introduction of LT-AlN can also result in higher crystal quality, where the FWHM of GaN(0002)'s X-ray rocking curve was reported to decrease to near that of GaN on sapphire (about 400 arcsec or 0.111 °) [38].

2.1.5 Graded AlGaN buffer layers

A graded intermediate buffer layer is frequently used in mismatched heteroepitaxy [106], for example in the Ge/silicon system. However, unlike the Ge/silicon system, a compositionally graded buffer layer cannot be applied to the GaN/silicon system. Instead, the compositional grading uses AlGaN, where the Ga content increases step-wise (or continuously) from AlN to GaN. Even though GaN could be deposited on AlN/Si, insertion of AlGaN intermediate layers improved the quality of the resultant GaN [61, 107]. Kim et al. showed that the insertion of AlGaN intermediate layers reduced both GaN's dislocation density and surface roughness, which translated to better optical properties [107]. The presence of AlGaN intermediate layers provided compressive stresses [61, 73], like LT-AlN, which compensated for the intrinsic tensile stresses in GaN on silicon. Able et al. [108] showed that a graded AlGaN

buffer layer thickness of about 400 nm is sufficient to reduce the tensile stress to avoid cracking. The reason for this compressive stress is that the AlGaN lattice constant is smaller than that of GaN, thus GaN will sustain compressive stresses when grown on AlGaN. Although AlN's lattice constant is also smaller than GaN, the critical thickness for pseudomorphic growth of GaN on AlN is too thin to be useful; hence, compressive stress can be introduced without generation of more dislocations by using an AlGaN intermediate layer [108].

2.1.6 Epitaxial lateral overgrowth

To mediate the high dislocation density resulting from the large lattice mismatch, several growth techniques have been introduced. Epitaxial lateral overgrowth (ELO) techniques are useful in achieving high quality GaN in MOCVD. ELO is a technique where GaN grows laterally across either a void or a growth mask, starting from a nucleated island on the substrate. The laterally grown GaN would eventually coalesce to form a continuous film. The ELO technique has been used with success in several other heteroepitaxy systems such as GaAs on Si [91], InGaAs on GaAs [92], and InP on Si [109].

As the portion of GaN that was laterally grown is not constrained by any lattice structure underneath it, it tends to grow into very high quality GaN with low dislocation density. It had been demonstrated that dislocation lines, which began propagating vertically, started to change direction and ran parallel to the surface (see Figure 2-1) as the material grew laterally [93, 110]. ELO is known to reduce dislocation densities from 10^8-10^{10} cm^{-2} to 10^6 cm^{-2} [4].

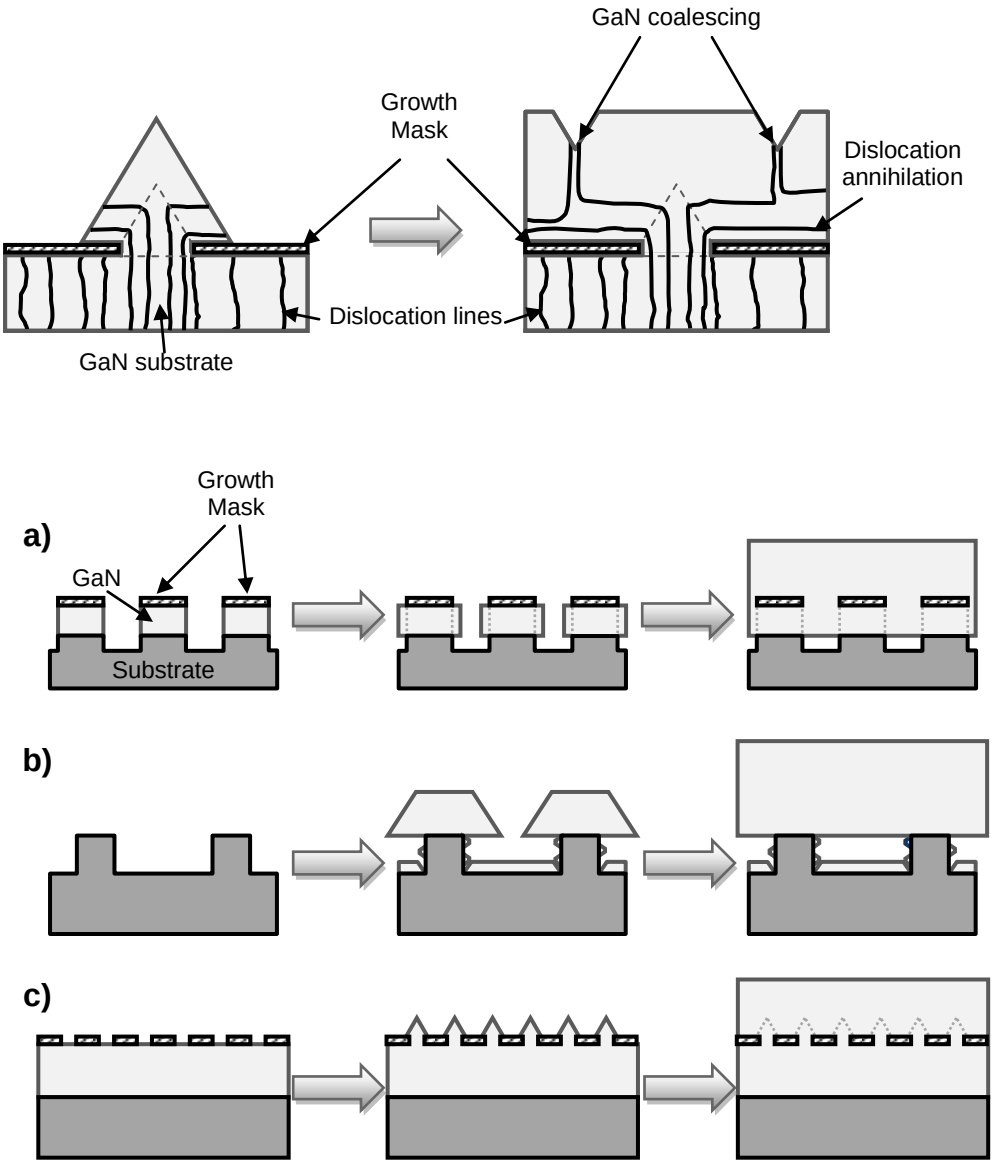

Figure 2-1. Schematic of the ELO process showing the reduction of dislocation lines mechanism as GaN coalesces (top), as derived from reference [111], with variants of ELO, such as pendeo-ELO (a), maskless ELO (b) and nano-ELO (c).

There are several variants of ELOs, including pendeo-ELO [112], maskless ELO [113] and nano-ELO [114-116], which all improve the GaN quality with the same concept. The fabrication steps for the variants of ELO are given in Figure 2-1.

2.2 Silicon substrates with nanostructured surfaces

As ELO is shown to dramatically reduce defects in GaN-on-silicon heteroepitaxy [117], incorporating this idea with nanoheteroepitaxy was especially intriguing [50]. This is because nanoheteroepitaxy can accommodate mismatch as high as 4.2% without generating defects for any thickness grown [50]. Combining both techniques gives nanoheteroepitaxy lateral overgrowth (NELO), first described by Zubia and Hersee [50]. With NELO, crystals are grown on areas small enough such that the critical thickness [118] is increased substantially, and in certain cases the critical thickness ceases to exist [51]. This makes it possible to grow high mismatched heteroepitaxy without creating dislocations.

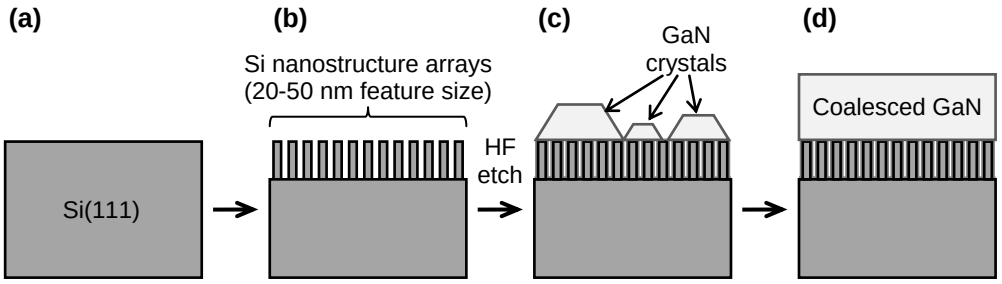

Figure 2-2. Schematic of the fabrication sequence for this work. The Si(111) substrate (a) is etched to form nanostructure arrays (b). A short immersion in dilute HF is done to remove native oxide before GaN growth is performed on the substrate by MOCVD, with AlN deposited as a nucleation layer (c). The GaN eventually coalesces into a film.

Therefore, we aim to leverage on this and use a silicon substrate with nanostructured surface for GaN film growth (see Figure 2-2). First, silicon (111) is used to produce silicon nanostructures by top-down etching (described in Chapter 4). One-step metal-assisted chemical etching (1-step MACE) is proposed to fabricate the nanostructures, and optimization of this nanofabrication is presented in a later part of this thesis. Then silicon is briefly etched using dilute HF to remove the native oxide before it is placed in the MOCVD reactor. An AlN nucleation layer is first grown, followed by any

required buffer layers, and then finally GaN. In Chapter 5, this thesis will discuss the effects the nanostructured surface has on the GaN film grown over it. Before presenting the results of the growth, the benefits of using such a nanostructured substrate are explained.

2.3 Benefits of nanostructures

We described the role of nanostructures in dislocation reduction to be due to three main mechanisms: forcing existing dislocations out of nanostructures through dislocation annihilation, preventing new dislocation by accommodating mismatch coherently, and reduced stiffness of nanopatterned substrate.

Due to the mismatch in lattice constant, GaN films grown on sapphire or silicon carbide contain a high density of threading dislocations and defects. The presence of dislocations and defects is detrimental to the performance of devices fabricated out of these materials. For example, LEDs will have less photons generated as the defects act as non-radiative recombination centers; HEMT devices will suffer a reduced electron mobility as the threading dislocations cut into the path of the electron channel [119]. Since there is no commercially viable native substrates available (either too small or too expensive), researchers explored various approaches to reduce the threading dislocations.

2.3.1 Threading dislocation annihilation

The idea of threading dislocation annihilation in nanostructures was explained in a simple concept by Eshelby [120]. The effect of free surfaces on a screw dislocation located at a distance far enough from the center of a nanorod ($0.54r$ away, as predicted by Eshelby's calculations) would provide a force to bring the dislocation out

of the nanorod. Colby et al. [121] carried out a numerical study to investigate this dislocation annihilation effect in nanorods. They modeled 100 nm tall GaN nanorods with a pyramidal top (see Figure 2-3), with diameters ranging between 10 to 80 nm. They concluded that dislocations located at more than $0.25r$ from the center will always have a lateral force greater than the Peierls-Nabarro force (the force that pins dislocations), for nanorods with diameter between 20 to 80 nm. In other words, dislocations present in the nanorod's cross-sectional area have a 93% chance of being forced out.

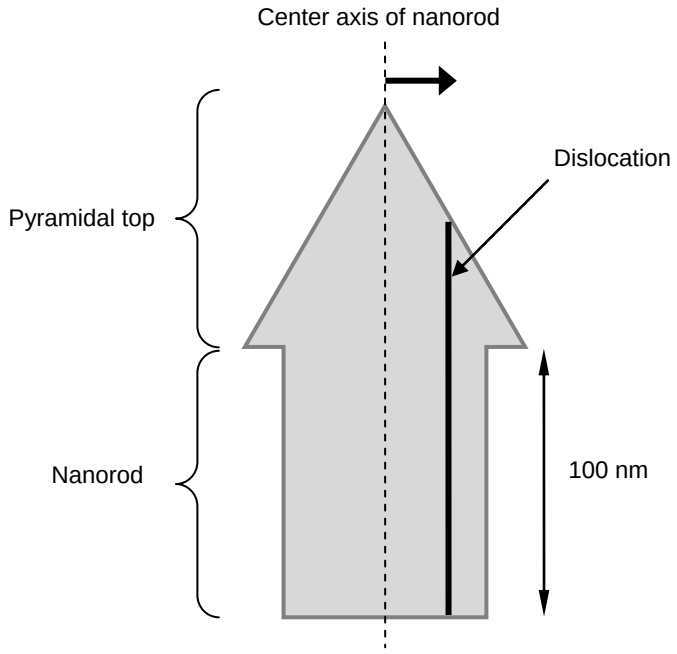

Figure 2-3. Shape of modeled GaN nanorod by Colby et al. [121], where the 100 nm tall nanorod has a pyramidal top.

2.3.2 Defects and strain reduction by nanoscale growth area

The small diameter of a nanorod makes it difficult for dislocations to nucleate within the rod. Matthews [122] showed that nucleation of half-loops requires a critical radius. If the nanorod cannot accommodate half-loop of at least the critical radius, it is

reasonable to think that half-loop nucleation would not be possible according to Matthews's theory.

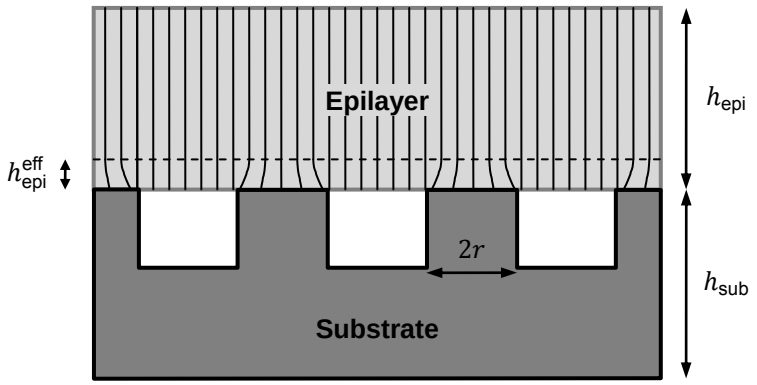

Figure 2-4. Schematic showing the various dimensions to calculation strain energy per unit area in nanoheteroepitaxy. Adapted from reference [50].

The reduced dimension of a vertical nanorod also means only a small area is in contact with the substrate. Hence, only a small base area of the grown material is forced to align itself to the lattice constant of the substrate. The rest of the rod will be able to elastically relax in radial directions [50]. A small base area will also mean a great reduction of misfit dislocations occurring at the interface, thus minimizing the formation of threading dislocations [51, 123]. A detailed explanation, in the energy point of view, is known as the nanoheteroepitaxy theory, developed by Zubia and Hersee [50] (based on Luryi and Suhir's report [51]). The theory is described in the following paragraphs.

When the lateral dimension of the area to deposit is finite, the total strain energy per unit area of a coherent film will be less than that of an infinitely large area [51]. This total strain energy varies linearly with the lateral dimensions of the deposited area. Zubia and Hersee [50] argued that the total strain energy should be even lower than suggested by Luryi and Suhir, as substrate compliance was ignored in their calculations. The structure considered is represented in Figure 2-4. The substrate is

patterned with an array of vertically standing rods of radius r. Target material is then grown on top of the rods, and subsequently coalesced to form a continuous epilayer of thickness h_{epi}. Hence, the rigid contact between the epilayer and the substrate is confined to the top of the rods. The epilayer is assumed to have no rigid contact with the substrate in the area between the rods. The maximum strain energy density per unit area in the epitaxially grown material (E_{epi}) is given as [51]:

$$E_{\text{epi}} = \frac{Y_{\text{epi}}}{1-\nu_{\text{epi}}} \varepsilon_{\text{epi}_0}^2 h_{\text{epi}}^{\text{eff}} \tag{2-1}$$

where Y_{epi} is the Young's modulus, ν_{epi} is the Poisson ratio, $\varepsilon_{\text{epi}_0}$ is the maximum strain at the interface and $h_{\text{epi}}^{\text{eff}}$ is the effective layer thickness [51]. Please note that the portion of epilayer beyond $h_{\text{epi}}^{\text{eff}}$ would contribute negligible strain increase on the epitaxial layer [51]. The effective layer thickness arises because of the small contact area between the epilayer and the substrate, when compared to the epilayer thickness. The maximum interfacial strain of the epitaxial layer is defined by [50]:

$$\varepsilon_{\text{epi}_0} = \frac{\varepsilon_T}{1+\left(K\dfrac{1-\exp\left(-\pi h_{\text{epi}}/2r\right)}{1-\exp\left(-\pi h_{\text{sub}}/2r\right)}\right)}, \tag{2-2}$$

$$\text{where } K = \frac{Y_{\text{epi}}}{1-\nu_{\text{epi}}}\frac{1-\nu_{\text{sub}}}{Y_{\text{sub}}}.$$

and where ε_T is the total lattice mismatch strain, h_{epi} is the thickness of the epitaxial layer, h_{sub} is the height of the substrate, r is the radius of the growth area, Y_{sub} is the Young's modulus of the substrate and ν_{sub} is the Poisson ratio of the substrate. Assuming both epilayer and substrate thicknesses are much larger than the radius of the rods (h_{epi}, $h_{\text{sub}} \gg$ r), we can approximate that:

$$\varepsilon_{\text{epi}_0} \approx \frac{\varepsilon_T}{1+K}, \tag{2-3}$$

For the GaN-on-silicon system, $\varepsilon_{\text{epi}_0}$ is estimated to be about $0.32\varepsilon_T$ or (6.5%), from Equation (2-3). The rest of the 68% of the mismatch is accommodated by the substrate (silicon). This estimate is relatively accurate if $h_{\text{epi}}, h_{\text{sub}} > 4r$.

The effective layer thickness is defined as [51]:

$$h_{\text{epi}}^{\text{eff}} = \frac{r}{\pi}\left[1 - \text{sech}\left(k_{\text{epi}} r\right)\right]^2 \left[1 - e^{-\pi h_{\text{epi}}/r}\right] \tag{2-4}$$

where k_{epi} is the interfacial compliance parameter of the epitaxial layer [51]. The interfacial compliance parameter is estimated by:

$$k_{\text{epi}} = \frac{1}{h_{\text{epi}}^{\text{eff}}}\sqrt{\frac{3}{2}\left(\frac{1-\nu_{\text{epi}}}{1+\nu_{\text{epi}}}\right)} \tag{2-5}$$

$$k_{\text{epi}} \approx \frac{0.88}{h_{\text{epi}}^{\text{eff}}}, \tag{2-6}$$

taking $\nu_{\text{epi}} = 0.319$, from reference [124]. Assuming $h_{\text{epi}} \gg r$, we get:

$$h_{\text{epi}}^{\text{eff}} \approx \frac{r}{\pi}\left[1 - \text{sech}\left(\frac{0.88r}{h_{\text{epi}}^{\text{eff}}}\right)\right]^2 \tag{2-7}$$

Solving Equation (2-7) gives $h_{\text{epi}}^{\text{eff}} \approx 0.27r$. Note that this estimate does not depend on epilayer thickness, as long as the epilayer is thick enough ($h_{\text{epi}} > 4r$). The effective layer thickness ceases to depend on epilayer thickness because of strain decay [125]. With the values of $\varepsilon_{\text{epi}_0}$ and $h_{\text{epi}}^{\text{eff}}$ (estimated from Equation (2-3) and (2-7), respectively), the maximum strain energy density per unit area in the epilayer can be calculated by Equation (2-1), we get:

$$E_{\text{epi}}\ (\text{J/m}^2) \approx 0.51r\ (\text{nm}) \tag{2-8}$$

Note that E_{epi} only varies with the radius of the rods. In the case of a planar substrate, the areal strain energy density of the epilayer ($E_{\text{epi, planar}}$) is given by [126]:

$$E_{\text{epi, planar}} = \frac{Y_{\text{epi}}}{1-\nu_{\text{epi}}} h_{\text{epi}} {\varepsilon_T}^2 \tag{2-9}$$

For the case of GaN-on-silicon:

$$E_{\text{epi, planar}}\ (\text{J/m}^2) \approx 18.7 h_{\text{epi}}\ (\text{nm}) \tag{2-10}$$

For comparison, an array of rods with 40 nm in diameter would have maximum areal strain energy density of about 10 J/m^2 (regardless of epilayer thickness, as long as epilayer thickness is large), whereas the areal strain energy density of just 1 nm of GaN epilayer on a flat silicon substrate would have exceeded that.

In order to consider the case where dislocation formation is not energetically favorable, the strain energy of a dislocation needs to be calculated. According to People and Bean, the areal energy density of a screw dislocation (E_{D}) is estimated to be [126]:

$$E_{\text{D}} \approx \frac{Y_{\text{epi}}}{2\left(1+\nu_{\text{epi}}\right)} \frac{b^2}{4\pi w_D} \ln\left(\frac{R}{b}\right) \tag{2-11}$$

where w_D is the effective interfacial width of the dislocation (based on People and Bean [126], we assumed it to be 5 atomic spacing in the $\langle 11\bar{2}0 \rangle$ direction), R is the closest distance from the dislocation to a free surface and b is the magnitude of the dislocation's Burger's vector. Since epilayer and substrate thickness are large, we take $R = r$ [50].

$$E_{\text{D}}\ (\text{J/m}^2) \approx 1.56 \ln\left(\frac{r\ (\text{nm})}{0.51851}\right) \tag{2-12}$$

It is not energetically favorable for the dislocation to form if E_{D} is larger than E_{epi}. Solving Equations (2-8) and (2-12), dislocation should not form when r is smaller than 8.5 nm (for GaN-on-silicon system). However, it should be noted that it would only be useful if such a system can be applied over a large area. Creating an array of nanorods smaller than 17 nm in diameter over a large area would be technologically challenging to achieve.

2.3.3 Reduced stiffness of nanopatterned substrate

In Zubia and Hersee's work (described above), it was assumed that lattice mismatch was the only strain involved. However, in the GaN-on-silicon system, there is also thermal mismatch, where the thermal strain occurs after the deposition was completed. Such residual strain was not accounted for, hence it is prudent to explain the strain reduction mechanism for such case.

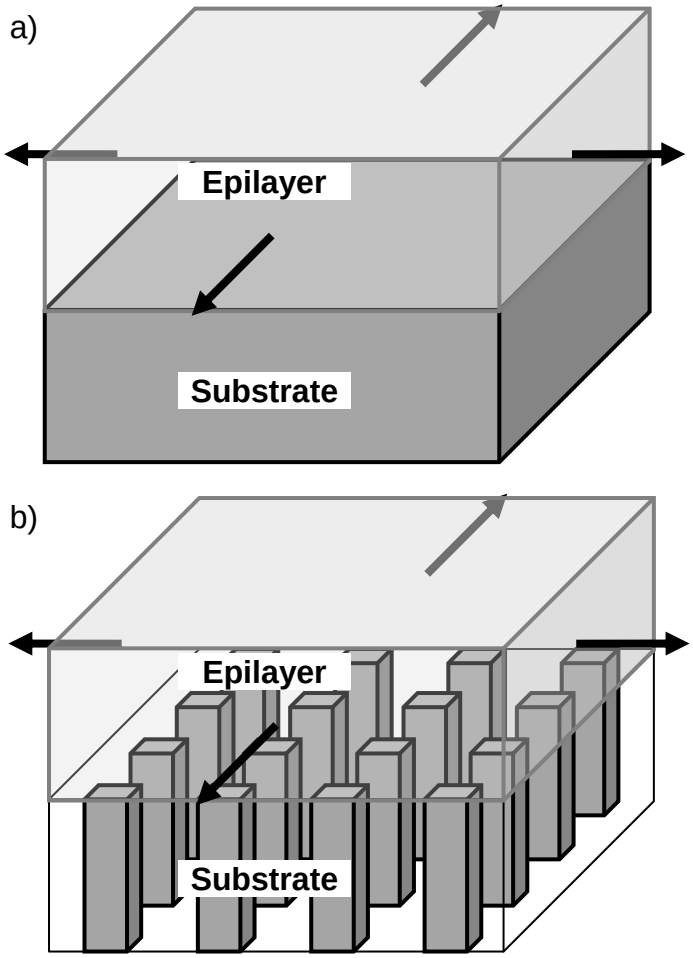

Figure 2-5. Schematic of epilayer grown on planar substrate and on an array of rods.

Figure 2-5 compares a schematic of an epilayer grown on top of a planar substrate to that of an epilayer grown on top of an array of rods. As there is an air matrix

surrounding the array of rods, the overall effective Young's modulus of the layer of rods is less than that of a planar substrate. The lower stiffness of the array of rods would allow the epilayer to expand or contract with less biaxial stress than if it is on a planar substrate. However, it is important to point out that such a system is unlikely to fully accommodate all thermal strains. [4].

In the GaN-on-silicon system, GaN film on a 50 mm wafer has to contract by about 100 μm (thermal expansion strain of 0.19%) to eliminate the thermal strain. This is possible if the rods are long enough to accommodate by bending. However, as high quality III-nitride requires rods of nanosize diameters (explained in sections 2.3.2 and 5.2.2), the rods cannot be too tall or they will have very high aspect ratio (in the range of 1000s). Such nanorods will be susceptible to breakage and bending, rendering it near impossible to fabricate. Hence, the rods' height has to reduced, but at the expense of a reduced thermal strain accommodation effect.

Taking the simplified assumption that the maximum lateral distance for a rod to bend is equal to half its height, a 100 nm tall rod could only relieve about 0.1% of the thermal strain on a 50 mm wafer. This is only possible if the nanorod is thin enough to accommodate bending without failure. Taking the fracture strength (σ_f) to be about 10 GPa and Young's Modulus (Y) to be about 100 GPa, for silicon nanorods with $2r_{\max}$ less than 20 nm [127], we can estimate the maximum diameter ($2r_{\max}$) of the nanorod for this to be possible using simple beam theory [128]:

$$r_{\max} = \frac{1}{3}\frac{\sigma_f}{E} \times \frac{H^2}{w}$$

where H is the height of the rod and w is the lateral bending distance. The maximum diameter for the case described above is about 13 nm.

2.4 Literature review on GaN on nanostructured surfaces

After the discussion on the mechanisms through which nanostructures can accommodate lattice and thermal mismatch, it can be seen that it is certainly promising and attractive to leverage nanostructures to grow high quality material.

2.4.1 Nanoporous silicon

According to the recommendations of International Union of Pure and Applied Chemistry (IUPAC), there are three subcategories of nanoporous silicon depending on pore sizes, namely microporous (less than 2 nm), mesoporous (2 to 50 nm) and macroporous (50 to 1000 nm) [129]. The brief review that follows will include nanoporous silicon of all subcategories.

The first successful GaN growth on nanoporous silicon was reported in 2001 [130]. The nanoporous silicon used was formed by a vapor etching technique, where the silicon substrate was exposed to HF and HNO_3 vapors, forming nanoporous silicon with size features less than 100nm [131]. Unfortunately, the GaN produced was not only polycrystalline, but with both wurtzite and zinc blende phases. This could be because the substrate used was Si(100) instead of Si(111).

It was only 5 years later when GaN growth on a nanoporous Si(111) substrate was reported [52]. In this work, nanoporous silicon was fabricated by drying etching a Si(111) substrate with anodized aluminum oxide (AAO) as an etch mask. An array of vertically straight nanopores was formed, with a pore diameter of about 60 nm. The authors claimed that the nanoporous substrates were found to reduce the dislocation density in the GaN on it. Unfortunately, the amount of reduction was not given. Threading dislocations were observed to bend 90° and not propagate to the top surface, much like as observed in epitaxial lateral overgrowth [132]. A stress reduction of about 0.82 GPa was found for GaN on nanoporous Si, when compared

with GaN on flat Si. In addition, the authors found that the optical properties were also improved for GaN on nanoporous Si.

Nanoporous silicon fabricated by anodization was also used for GaN growth [53]. The nanoporous silicon has sponge and rod-like structures on the order of 10 nm. Similar to the work by Zang et al. [52], improvements were found in GaN films grown on nanoporous silicon. Tensile stress was found to be reduced as well (reduction of between 0.32 and 0.53 GPa), but not as much as reported by Zang et al. However, interesting results were reported on the characterization using X-ray diffraction. It was found that the FHWM of the X-ray rocking curve for GaN(0002) was wider on nanoporous silicon than that on flat silicon; conversely, the FWHM of the X-ray rocking curve for GaN($10\bar{1}2$) was narrower on nanoporous silicon than that on flat silicon.

2.4.2 Patterned silicon-on-insulator

Silicon-on-insulator (SOI) substrates are considered as compliant substrates as the thin silicon can accommodate strains from misfit by deformation [133]. The presence of the oxide provided a additional possible defect reduction mechanism, where oxide become "fluid" at high temperatures [133]. At the same time, such nanoscale islands on oxide is less thermally stable [114], which can be detrimental to the quality of GaN grown on it. Although there were growths done on SOI [134-137], Zubia et al. further improved on the usage of SOI by patterning it into separated islands of silicon (see Figure 2-6), with sizes ranging from 80 to 300 nm, before depositing III-nitrides [114]. However, due to the nanosize of the silicon islands, the annealing step prior to growth had to be lowered to prevent deformation, probably due to increased surface diffusion [138].

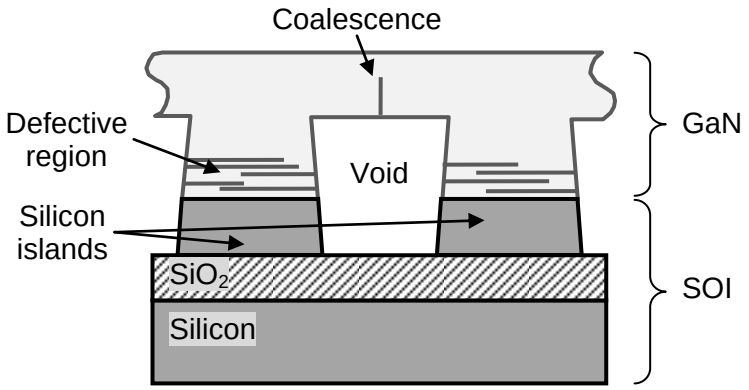

Figure 2-6. Schematic of the patterned SOI substrate with silicon islands, fabricated by Zubia et al. [114]. Diagram adapted from reference [114].

2.4.3 Silicon nanopillar arrays

It had been theorized that a pillar-like interfacial layer is able to reduce residual thermal strain, effectively becoming a universal substrate for systems with high thermal mismatch [4]. The pillars would be able to avoid cracking or dislocation formation by deformation. Hence, it is an attractive approach for mismatched system like GaN on silicon.

To the best of our knowledge, GaN films grown on silicon nanopillar arrays was first reported in 2005, by Hersee et al. [139] The nanopillar arrays were fabricated using AAO, forming pillars between 20 to 60 nm in diameter while their center to center spacing was about 110 nm. GaN grown on these substrates was found to have dislocation densities of less than 10^8 cm^{-2}. However, no other reports on GaN growth on silicon nanopillar arrays could be found, although there was a report in 2007 for GaN growth on silicon micropillar arrays [140].

2.5 Summary

Existing techniques for GaN growth on silicon are explained and presented. The techniques include implementing nucleation layers, in-situ silicon nitride masking, superlattices, LT-AlN interlayers, graded AlGaN buffer layers, and ELO. Subsequently, a nanostructured substrate, fabricated using one-step metal-assisted chemical etching, was proposed for our investigation. Benefits deriving from the nanostructures are explained. Previous works done by other researchers, based on nanostructured silicon, were reviewed.

Chapter 3. GaN growth by MOCVD and its characterizations

3.1 Introduction

This chapter describes and explains the features of MOCVD, and the characterization tools used in this thesis. The characterization tools includes atomic force microscope (AFM), scanning electron microscope (SEM), transmission electron microscope (TEM), X-ray diffraction (XRD), photoluminescence (PL) and Raman spectroscopies.

3.2 Metalorganic chemical vapor deposition of GaN

It should be noted that there exist several synonyms in literature for this growth technique, such as metalorganic vapor phase epitaxy (MOVPE), organometallic chemical vapor deposition (OMCVD) and organometallic vapor phase epitaxy (OMVPE). All the mentioned terms referred to the same growth technique, but, for consistency, this thesis will only refer it as MOCVD.

3.2.1 Introduction

MOCVD is a deposition method based on chemical vapor deposition (CVD), where the gaseous precursors react to form a film on a heated substrate (see Figure 3-1 for schematic diagram of MOCVD). This deposition method differs from physical vapor deposition (PVD) such as evaporation, sputtering and molecular beam epitaxy. The main difference is that deposition depends on chemical reactions of the gaseous precursor(s) and the use of carrier gas. MOCVD also deviates from CVD due to the

use of metalorganics (MO) compounds. The use of MO sources demands additional steps in transporting the precursors to the target substrate, which will be explained later in this chapter. In addition, very high quality grown layers with high throughput could be obtained using MOCVD.

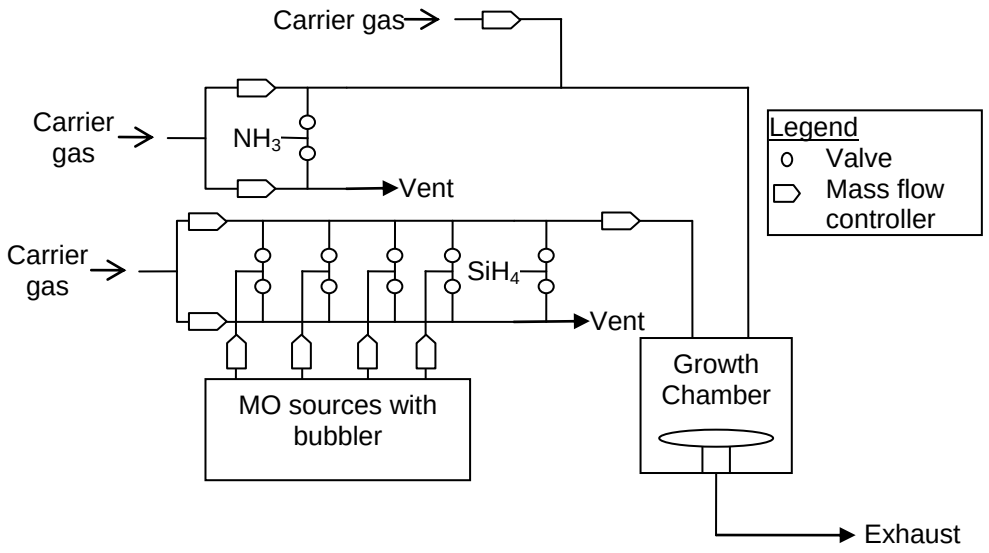

Figure 3-1. Schematic of the gas handling system of MOCVD

MOCVD is considered to be pioneered by Manasevit and his co-workers [141-143] in the 1960s, where his group worked extensively on material system based on arsenide. Subsequently, his group also reported work on nitride growth using MOCVD in 1971 [144]. However, MOCVD work on high quality III-nitrides was only kick started after Amano and his co-workers succeeded in MOCVD growth of GaN film on sapphire substrates in 1986 [12]. Another notable significant milestone was when Nakamura and his co-workers managed to fabricate successfully GaN-based LED in 1993 [145]. Since then, MOCVD on GaN was intensively researched into to obtain quality capable of device operation, whereby light emitting diodes (LEDs), laser diodes (LDs), transistors and photodetectors are demonstrated and produced commercially [146, 147]. The successful commercial implementation of MOCVD

growth of GaN over other techniques is because of its suitability in large scale production, promoting favorable economic benefits [143].

MOCVD is a complex deposition technique operating at high temperatures. There are two sections which are characteristic of MOCVD system: a special gas handling system involving bubblers and dilution by carrier gas (usually hydrogen and/or nitrogen), and the reaction chamber modified for high temperature operation. The carrier gas serves to transport the precursors from the source to the growth chamber.

3.2.2 Precursors for GaN growth in MOCVD

The group III precursors for MOCVD growth of III-nitrides consist of metalorganics (or group III alkyls), which include trimethylaluminum (TMAl), triethylaluminum (TEAl), trimethylgallium (TMGa), triethylgallium (TEGa) and trimethylindium (TMIn). The group V precursor for nitrides used is dominantly ammonia (NH_3). The precursors used for doping are usually silane (SiH_4) for n-type, and biscyclopentadienyl magnesium (Cp_2Mg) for p-type. It should be mentioned that trialkyl compounds are pyrophoric and highly reactive with water and oxygen, while ammonia gas is highly corrosive [4], hence extreme care should be taken. The hydride sources are in gaseous form, contained in pressurized cylinders, which can be introduced into the reactor through the gas lines. However, the MO sources are in liquid (or in the case for TMIn and Cp_2Mg, solution) form, which require a bubbler system (Figure 3-2) to transport.

The liquid precursors (or solution for TMIn and Cp_2Mg) are contained in a sealed stainless steel bubbler, where carrier gas is introduced into the inlet pipe and exit from the outlet pipe. The bubbler is designed such that the inlet pipe introduces the carrier gas into the liquid precursor and the carrier gas bubbles and exit through the outlet pipe. In this manner, the carrier gas will carry along the precursors in the form of vapor. The bubbler is placed in a thermal bath (usually between -20 ℃ and 40 ℃)

for a consistent vapor pressure. For our case, we use -10 °C, 20 °C, 30 °C and 40 °C for TMGa, TMAl, TMIn and CP_2Mg, respectively. The flow rate of carrier gas is controlled by a mass flow controller (MFC), and the pressure in the bubbler is maintained by a pressure controller fixed at outlet pipe. This pressure is to be higher than the growth chamber's pressure.

The vapor pressure of the MO is a critical parameter as it determines the concentration of the MO that is transported by the carrier gas, into the growth chamber. The vapor pressure can be calculated in terms of the following expression:

$$Log(p_{\mathrm{MO}}) = A - \frac{B}{T} \tag{3-1}$$

where p_{MO} is the equilibrium vapor pressure in Torr, and T is temperature in Kelvins. A and B are the coefficients determined from experimental results [148], usually provided by the manufacturer. The vapor pressure could be easily changed from Torr to the standard Pa by:

$$P_{\mathrm{MO}}(\mathrm{Pa}) = p_{\mathrm{MO}}(\mathrm{Torr}) \times \frac{101325}{760} \tag{3-2}$$

where P_{MO} is partial pressure of MO in Pa. Table 3-1 showed the coefficients for some of the MO precursors, provided by SAFC [149]. Usually, the flow rate input into the MOCVD system is in standard cubic centimeters per minute (sccm). In order to convert this flow rate into a more standardized molar flow rate (in mol/min), we use the following:

$$\text{Molar flow rate} = \frac{P_{\mathrm{std}}}{\mathrm{R}T_{\mathrm{std}}} \times \frac{Q_{\mathrm{b}}P_{\mathrm{MO}}}{P_{\mathrm{b}}} \tag{3-3}$$

where P_{std} is pressure at standard conditions (in Pa), R (=8.314 J mol^{-1} K^{-1}) is ideal gas constant, T_{std} is temperature (in kelvins) at standard conditions, Q_{b} is the volume flow rate of carrier gas into the bubbler (in sccm), and P_{b} is bubbler pressure (in

pascals). Note that the standard conditions are taken at P_{std} =101325 Pa, and T_{std}=273.15 K.

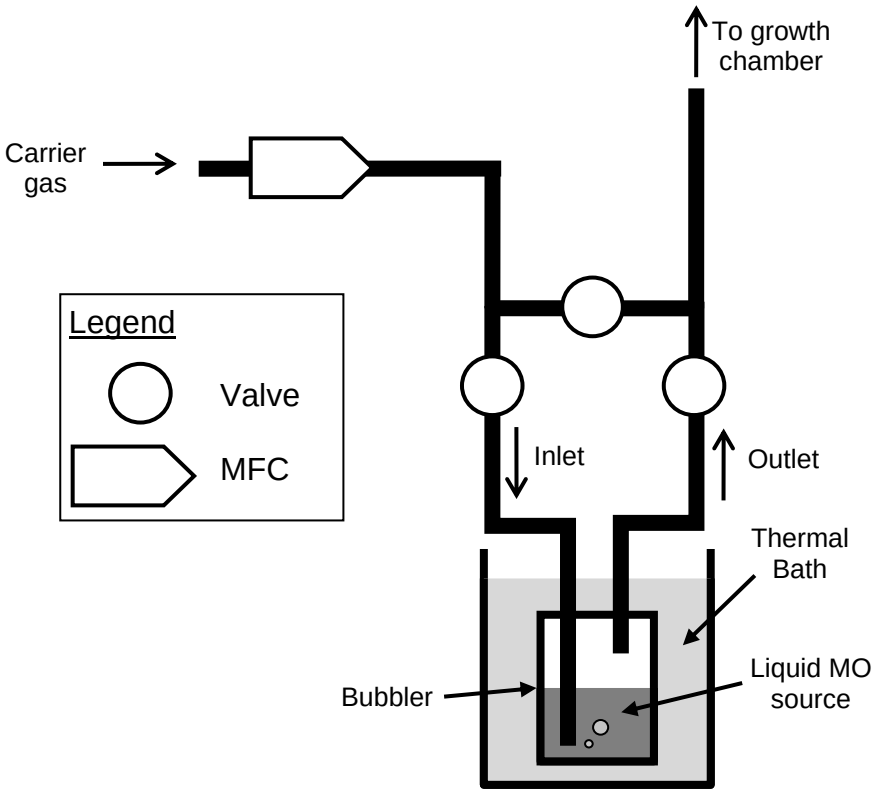

Figure 3-2. Schematic of a bubbler system to transport precursor using carrier gas.

From Equation (3-3), there are several parameters which could be changed to modify the MO molar flow rate. The straightforward parameter to change is the volume flow rate of carrier gas into the bubbler, where a change in the volume flow rate of carrier gas has a direct influence on the MO molar flow rate. However, as every MFC has a specified upper and lower limit, changing volume flow rate might not be possible if a large change in molar flow rate is required. The next parameter to change would be the bubbler pressure, where molar flow rate is inversely proportional to the bubbler pressure. Another parameter to change would be the bubbler temperature. This should be last choice among the stated methods, as thermal bath requires an extended period

of time to stabilize at a target temperature. Nevertheless, if large change to the molar flow rate is required, this should be the parameter to change.

Table 3-1. A and B coefficients of selected MO precursors. Melting points are also provided for reference. Obtained from reference [149].

MO precursors	A	B	Melting point (^{o}C)
TMAl	8.220	2134	15.4
TMGa	8.070	1703	-15.8
TEGa	8.080	2162	-82.3
TMIn	10.52	3014	88.4
Cp_2Mg	10.00	3372	176
DEZn	8.280	2109	-28

3.2.3 Growth chamber

The MOCVD used in this research is the EMCORE D125 MOCVD system. It is a vertical rotating-disk reactor, where the source gases are introduced into the growth chamber from above onto the substrates. The substrates are placed on a circular horizontal disk, called wafer carrier, which rotates at a high speed of up to 1000 revolutions per minute (rpm) during growth, to promote uniformity of the deposited films. The rotation is applied from a motor, outside the growth chamber, to a spindle which sticks into the center of the growth chamber. The wafer carrier is placed directly on this spindle inside the growth chamber, hence the wafer carrier's rotation speed is directly determined by the rotation speed of the spindle. The wafer carrier is heated by a two-zone resistive heater which is controlled by a feedback system for each zone, consisting of a proportion-integral-differential (PID) controller and a thermocouple. The thermocouples are installed beneath the heating filaments. The growth chamber is made of stainless steel and cooled with water (cold wall reactor).

MOCVD is a complex process where a number of homogeneous and heterogeneous reactions happen between the group III and group V precursors. Growth related processes on the substrate surface such as adsorption, desorption and surface diffusion are also important in MOCVD. The carrier gas will transport the precursors to the heated region of the growth chamber, where they will undergo gas phase reactions, typically decomposition and adduct formation reactions [150], and also surface reactions, which we shall not discuss in great details. The reactions happening in the growth chamber is multi-steps and complex, but it can be represented by a simple formula:

$$A_3M + NH_3 \rightarrow MN + \text{by-products}$$

where A is the alkyl group and M is the group III metal.

In CVD, there are two growth regimes to consider: mass transport limited (or diffusion limited) regime and surface-reaction-limited regime [143]. In the mass transport limited regime, the growth rate is limited by gas phase diffusion; whereas in surface-reaction-limited regime, the growth rate is limited by the reaction rates at the substrate surface. The different regimes can be identified by observing how growth rate varies with temperature. If the logarithm of the growth rate has a linear relationship with the inverse of the absolute temperature, then the growth is in the surface-reaction-limited regime. If the logarithm of the growth rate has a sublinear dependence on temperature, then the growth is in the mass transport limited regime. In a less commonly discussed case where the growth rate decreases with increasing temperature, the growth could be caused by either reactant desorption [151], parasitic reactions [151-153] or etching [154].

In the mass transport limited growth regime, an increase in chamber pressure should not affect the growth rate [143].[1] Since the reactor is in a steady-state condition, the growth rate is directly related to the flux of reactants to the substrate. We shall only consider the flux of group III reactants (i.e. metalorganics). This is because MOCVD always operates in ammonia-rich condition (V/III ratio more than 100). When in the mass transport limited regime, taking the boundary layer model, the flux of group III reactants to the substrate surface is determined by the following equation:

$$\text{Flux} = \frac{D}{\delta} N_{\text{GrpIII}} \tag{3-4}$$

where D is the diffusivity, δ is the boundary layer thickness, and N_{GrpIII} is the concentration of group III reactant in bulk gas. From Ghandhi and Field [155], they demonstrated the following relationship for boundary layer thickness:

$$\delta \propto \sqrt{\frac{D}{U}} \tag{3-5}$$

where U is the gas velocity. From Moffat and Jensen [156] estimation, the diffusivity of TMGa in hydrogen is given as:

$$D = \frac{2.26 \times {T_{\text{gas}}}^{1.73}}{P} \text{cm}^2/\text{s} \tag{3-6}$$

where T_{gas} is the bulk gas temperature in Kelvin and P is pressure in Pa. From equations (3-4), (3-5) and (3-6), the following could be derived for the growth rate (assuming reaction is not desorption limited and there is negligible parasitic reactions):

[1] From Equation (3-7), the growth rate is seen to have an inverse square root dependence on the chamber pressure. However, in practice, when we change the chamber pressure without changing other settings, two other important parameters, namely gas velocity and reactant partial pressures, are affected as well. As the gas flows are mass-controlled, increasing chamber pressure will reduce the volume of the gas flows, making gas velocity *inversely proportional* to the chamber pressure. Mass-controlled gas flows will also fix the mass ratio of the reactants and carrier gas. Hence, the reactant partial pressure will be *directly proportional* to the chamber pressure. Looking back at Equation (3-7), increasing P will decrease U and increase P_{GrpIII} proportionally, and vice versa. This cancels the effect of changing P.

$$\text{Growth rate} \propto \sqrt{\frac{U}{P}} P_{\text{GrpIII}} T_{\text{gas}}{}^{0.865} \tag{3-7}$$

where P_{GrpIII} is the partial pressure of group III reactant in bulk gas. Note that concentration has been replaced with partial pressure, since partial pressure is directly proportional to its concentration. Equation (3-7) shows that the growth rate for mass transport limited regime has sublinear relationship with gas temperature.

In the surface-reaction-limited growth regime, the growth rate should be governed by the following equation (by stagnant film approximation) [143],

$$\text{Growth Rate} \propto e^{\frac{-E_a}{kT_{\text{sub}}}} \times \frac{P_{\text{GrpIII}}}{\text{R}T_{\text{gas}}} \tag{3-8}$$

where E_a is the activation energy to the surface reaction, k is the Boltzmann's constant, T_{sub} is the substrate temperature, and R is the ideal gas constant. Equation (3-8) shows that the growth rate has an exponential relationship with substrate temperature.

3.3 Atomic force microscopy

Atomic force microscopy (AFM) is a characterization tool that allows us to see and measure surface topography at high resolution and accuracy. AFM is very different from other forms of microscopes as it does not form an image using focused photons or electrons. AFM creates images by physically "feeling" the surface with a sharp tip; together with an x-y sweeping scan, the three dimensional topography of the surface can be determined. It should be noted that there exists special variants of AFM, such as magnetic force microscopy (MFM), electric force microscopy (EFM) and scanning Kelvin probe microscopy which leverage on AFM techniques to obtain information

other than just the topography. We shall not go into depth and skip discussion on such variants.

The tapping mode AFM (see Figure 3-3) is one of the more popular forms of contact mode AFM. This is the mode which is used in our characterization, using Bruker's Dimension® Icon™ AFM. The AFM cantilever tip is forced to oscillate at its resonant frequency by a piezoelectric. As the oscillating tip is brought near to the specimen surface, the interaction between the tip and the surface result in dampening of the oscillation. This in turn affects the frequency and amplitude of the tip. The photodetector will pick up this difference and feed it back to the system, causing adjustment to be made to the height such that the tip maintained a fixed distance away from the specimen's surface.

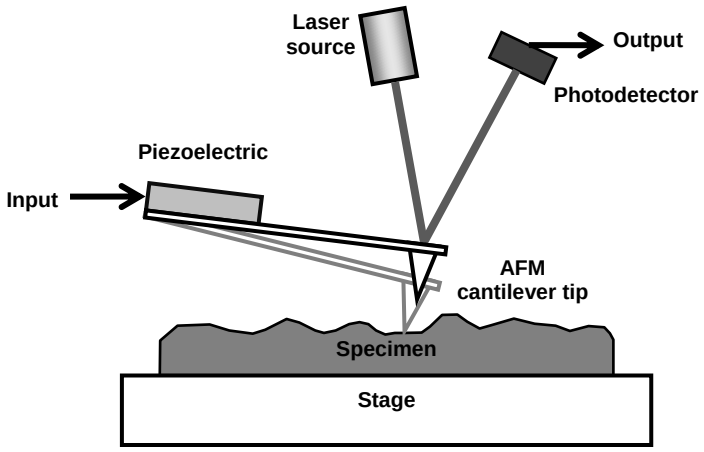

Figure 3-3. A simplified schematic of the operation of a tapping mode AFM.

AFM have a high resolution of 0.1 nm in the z-direction (vertical), which is better than SEM, and it could operate in air at atmospheric pressure. However, the imaging speed of AFM is very slow, typically a few minutes to tens of minutes for an image, depending on the size of the area imaged. The slow speed is due to the need to physically move the tip or sample stage in a raster scan fashion. Although SEM also

operates by raster scan, it is the electron beam that is moving; hence, it can be scanned much faster. The AFM is also prone to thermal drift, which could be reduced significantly if the specimen is left to stabilize in the system. Nevertheless, that would render the AFM as even more time consuming.

There are several precautions required in order to produce good AFM images. One common cause of artifacts is due to contaminated AFM tips. Such artifacts appear as streaks in the AFM images. When this happens, it should be replaced with a new AFM tip. Another common artifact could arise from moving samples, which is when the sample moved while the scanning is taking place. As Bruker's Dimension® Icon™ AFM uses vacuum suction to hold the sample, the back of the sample must be flat and clean for the suction to work properly. If that is not possible, the sample should be affixed to the sample stage by adhesive tape.

3.4 Scanning electron microscopy

A scanning electron microscope (SEM) uses an electron beam, rather than visible light, to produce a magnified image of the sample. Since electron wavelengths are much smaller than visible light wavelengths, much larger magnifications are possible. The electron wavelength depends on its velocity v, or accelerating voltage V, and can be calculated using de Broglie equation:

$$\lambda_e = \frac{\mathrm{h}}{m_e v} = \frac{\mathrm{h}}{\sqrt{2qm_e V}} = \frac{1.2264}{\sqrt{V}} \text{ [nm]} \tag{3-9}$$

where λ_e is the electron wavelength, h is Planck's constant, m_e is mass of electron, and q is the elementary charge. From Equation (3-9), an electron with an accelerating voltage of 5 kV has wavelength of 0.017 nm (much smaller than visible light, which

is between 400 to 700 nm), thus allowing much better resolution than an optical microscope.

An electron source with a maximum accelerating voltage of 30 kV is used for SEM purposes. Imaging is formed by a scanning mode, where electrons are focused into a small spot and they are swept across an area of interest sequentially. The focused spot first moves horizontally from left to right (in the x direction) rapidly, forming a single line scan. Then the spot is deflected back to the left where it started for the horizontal scan, but it is also deflected downwards slightly. The next line scan will then be slightly displaced downwards when compared with the previous scan. This is repeated until the whole area of interest is covered. The signals collected then form the image.

The most common signal collected for imaging is the secondary electrons. Secondary electrons are electrons that are ejected from the outer-shell of the target specimen, where energy is gained from the primary source electrons. Most of the secondary electrons are created close to the specimen surface (typically less than 2 nm) [157]. Hence, this mode of signal collection shows the topography of the specimen. This would be the operating mode for all of the SEM images used in this thesis, using a JEOL JSM 6700F.

A good focus of the electron spot will correspond to a good image resolution. Focusing is done by moving to a small feature on the specimen and obtaining a sharp image of the feature, by adjusting the objective-lens current. Astigmatism also has to be corrected in order to obtain a focused image. Ideally, astigmatism is corrected when the electron probe spot on the specimen corresponds to a perfectly round shape. Hence, astigmatism should be corrected from specimen to specimen because different specimens might not be mounted exactly flat on the sample holder.

No special sample preparation is required for SEM imaging, unless the specimen is insulating. Insulating specimen may result in electrostatic charging, in which the image will suffer serious degradation if the specimen becomes negatively charged. Approaching electrons from the probe would be deflected by the negatively charged specimen, resulting in distortions and fluctuations. If the specimen is not mounted properly to the sample holder, image degradation may also occur as extra charges could not be conducted away from the specimen. A thin coating of conductive material, usually 10 nm of gold, can be sputtered on the insulating specimen to prevent image distortion from charging effects. However, it should be noted that the signal received from a gold coated specimen might show grains of the sputtered gold at high enough magnifications. In addition, signal contrasts from different materials in the specimen would be masked by the conductive coating.

The resolution of SEM is typically between 1 and 10 nm [157], which is about 2 orders of magnitude better than light-optical microscope. The resolution for the JEOL JSM 6700F is 1 nm and 2.2 nm, for an accelerating voltage of 15 kV and 1 kV, respectively. It is worth commenting that this resolution is much larger than the electron wavelength (calculated using Equation (3-9)), as the beam diameter in SEM can only be focused to 0.1 nm at best. In addition, due to scattering of electrons, the secondary electrons detected come from a much broader area than the beam diameter. This results in reduced resolution.

3.5 Transmission electron microscopy

Similar to SEM, a transmission electron microscope (TEM) also utilizes an electron beam to produce a magnified image of the sample. Therefore, TEM can obtain high resolution because of the shorter de Broglie wavelength of electrons (as explained above). The difference between TEM and SEM is that TEM makes use of transmitted

electrons for imaging. Hence, a certain amount of preparation is required to thin the sample to become electron transparent. The imaging optics then use appropriate lenses to form a high resolution image (resolution of about 0.2 nm for modern TEM [157]). The resolution of the TEM (JEOL 2100 LaB_6 TEM) used for the results in this thesis is 0.14 nm.

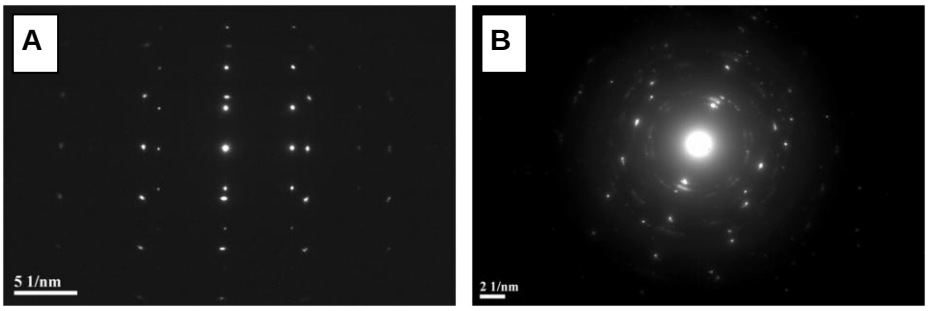

Figure 3-4. SADP of (A) a single crystalline GaN film on AlN, with [01$\bar{1}$0] as the zone axis, and a polycrystalline AlN film (B). Note that single crystalline samples result in sharp spots, while polycrystalline samples result in concentric rings of spots.

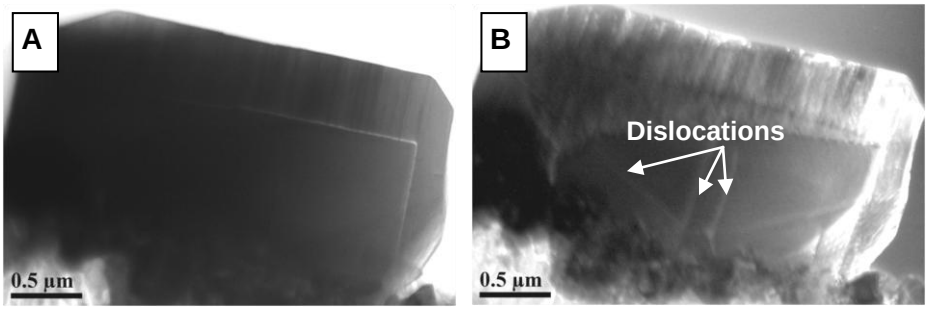

Figure 3-5. (A) Bright-field and (B) dark-field TEM images ($\boldsymbol{g}$=[0002]) of a GaN island. Note that some of the dislocations become visible in the dark-field image.

In addition to the ability to achieve high resolution, a very useful function of TEM is to obtain selected area diffraction patterns or SADP (see Figure 3-4). When electrons pass through the sample, the sample's planes of atoms act like a diffraction grating for the wave-like electrons. If the sample is single crystalline, the resulting image will be a series of spots, where each spot corresponds to a satisfied diffraction condition of

the sample's crystal structure. From the spots position, the crystal structure and the zone axis can be determined. If the sample is polycrystalline, the diffraction pattern will form concentric rings. This is useful in confirming the crystallinity and the crystal structure of the sample.

TEM can also be adjusted to obtain dark-field images, where the user can choose the targeted diffracted spot to form the image. Dislocations with Burgers vector containing a non-zero component in that direction will be visible. From Figure 3-5B, the chosen diffracted vector (***g***) is [0002], hence dislocations with Burgers vectors having a non-zero [0002] component will be visible.

3.6 X-ray diffraction

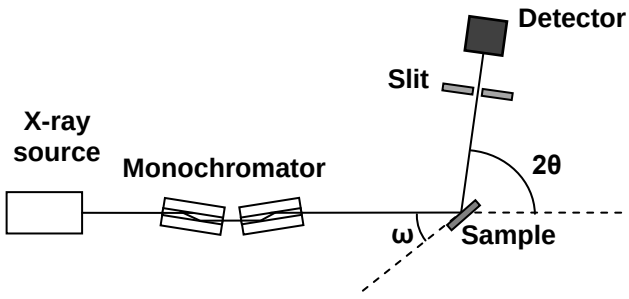

Figure 3-6. Schematic optics of double-crystal XRD.

X-ray diffraction (XRD) is a non-destructive characterization technique which involves probing a target sample with X-ray radiation, in order to find out its thickness, lattice parameters, strain, composition, defect densities and crystal structure if unknown. The X-ray is typically produced by bombarding copper with electrons. In Figure 3-6, the X-ray radiation is made monochromatic after passing it through a monochromator, before directing it at the sample. This arrangement is

known as the double-crystal XRD, which is used for high resolution scans. For even higher resolution, the slit can be replaced by an analyzer crystal. According to Bragg's law, the inter-atomic spacing (between planes of atoms) produces constructive interference according to the following:

$$n\lambda = 2d \sin\theta \tag{3-10}$$

where n is an integer (usually unity in XRD analysis), λ is the wavelength of the X-ray, d is the inter-planar spacing, θ is the angle between the incident beam and the planes of atoms.

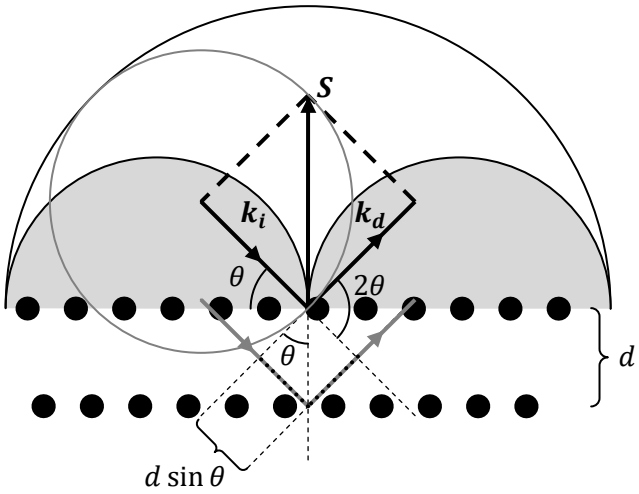

Figure 3-7. A representation of the reciprocal space of a sample scanned using XRD, where the path difference between the 2 planes of atoms is marked by dotted line. The total path difference is $2d \sin\theta$. Vectors $\boldsymbol{k_i}$ (incident beam) and $\boldsymbol{k_d}$ (diffracted beam) have a length of $1/\lambda$ each, and $\boldsymbol{S} = \boldsymbol{k_d} - \boldsymbol{k_i}$ where $\boldsymbol{S}$ is the reciprocal lattice spot probed by XRD in this arrangement. If the Bragg diffraction condition is satisfied, vector $\boldsymbol{S}$ will have a length of $1/d$. Regions of reciprocal space where the sample blocks the x-ray beam are shaded in grey (inaccessible). The Ewald sphere is shown here as a circle with blue outline, cutting the origin of the reciprocal space and the reciprocal lattice spot of vector $\boldsymbol{S}$.

Figure 3-7 shows a representation of the reciprocal space of a probed crystal. Bragg diffraction occurs when Equation (3-10) is satisfied (usually $n = 1$). Then vector $\boldsymbol{S}$ is a reciprocal lattice point of the sample with a length of $1/d$. The regions of reciprocal

space where the sample blocks the X-ray beam are shaded in grey (inaccessible). In other words, this lattice points in the shaded reciprocal space define planes where the diffracted beam does not appear above the crystal surface. The Ewald sphere is shown here as a circle with blue outline, cutting the origin of the reciprocal space and the reciprocal lattice spot of vector $\boldsymbol{S}$. The significance of the Ewald sphere is that all lattice points that lie on the surface of the Ewald sphere define the crystal planes where diffracted beams can emerge for that particular incident beam $\boldsymbol{k_i}$. When comparing the angles in Figure 3-6 and Figure 3-7, it might appear that ω equals to θ. Note that this is only true if the probed crystallographic planes are parallel to the sample surface.

Hence, by obtaining the angles, we can obtain the inter-atomic spacing using Bragg's equation. It should be noted that there are areas in the reciprocal space which cannot be accessed by the XRD (see shaded regions in Figure 3-7), as either the incident beam or the diffracted beam is obstructed by the sample. An example of such an obstructed reciprocal spot is the $(10\bar{1}2)$ plane of GaN. Another arrangement can be used to probe reciprocal space in this region, where the sample is rotated $90\,°$ in ϕ direction and tilt in χ direction (see Figure 3-8). This arrangement is known as skew symmetric.

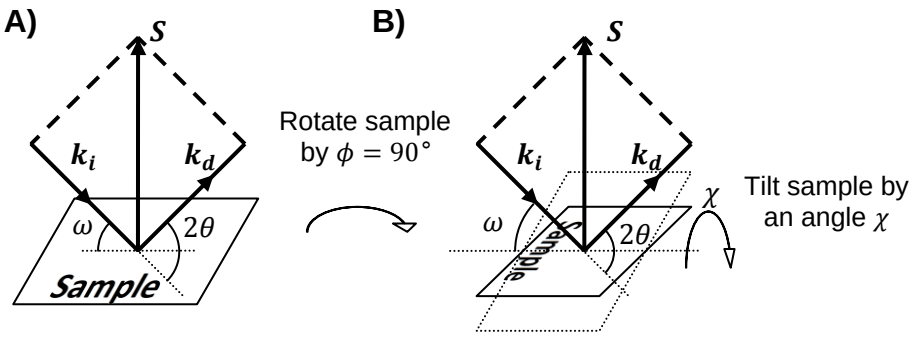

Figure 3-8. Schematic showing how to change from (A) a symmetrical scan arrangement to (B) a skew symmetrical scan arrangement.

Most reported values for XRD in the literature were acquired by either ω scans or 2θ-ω scans (or ω-2θ scans which is the same as 2θ-ω as but ω is on the x-axis, instead of 2θ). In ω scans, the X-ray source and detector both remain stationary while the sample is rotated about the ω axis. In reciprocal space, $\boldsymbol{S}$ vector traces an arc centered on the origin. The length of $\boldsymbol{S}$ stays the same, but its direction changes. In 2θ-ω scans, the sample is rotated by ω and the detector is rotated by 2θ with an angular ratio of 1 : 2, respectively. In reciprocal space, $\boldsymbol{S}$ vector moves outwards from the origin radially, while maintaining the direction. Hence, the length of $\boldsymbol{S}$ changes, but its direction remains the same. If the arrangement is such that $\omega = \theta$, it is known as the symmetrical scan.

The spots in the reciprocal space will be broadened by the presence of microstructural defects. This broadening is often represented in the form of FWHM of the XRD scans. A broadening in the ω scan is caused by an increased amount of dislocation-induced tilt or twist (it could be also caused by wafer curvature). A broadening in the 2θ-ω scan is caused by a variation in the interplanar spacing, which could be due to strain or composition gradients (it could be also caused by X-ray wavelength variations).

The FWHM of the ω scan is useful in estimating the threading dislocation density of a sample, especially in the highly defective III-nitrides [158]. For the wurtzite III-nitrides, ω scans of the $000l$ reflections (obtained by symmetrical scans) are distorted by threading dislocations with screw components [159]; whereas ω scans of the off-axis reflections (obtained by skew symmetrical scans) are sensitive to all threading dislocations. A simple estimate of the total dislocation density can be obtained from the FWHM of 0002 reflection [158]:

$$\text{Total dislocation density} = \frac{\text{FWHM}^2}{4.35b^2} \tag{3-11}$$

where b is the burgers vector (taken as lattice constant c). Note that the FWHM is in radians. If the FWHM of both 0002 ($FWHM_{0002}$) and $10\bar{1}2$ ($FWHM_{10\bar{1}2}$) reflections are obtained, the screw and edge dislocations can be estimated by [160]:

$$\text{Screw dislocation density} = \frac{FWHM_{0002}{}^2}{9b^2} \tag{3-12}$$

$$\text{Edge dislocation density} = \frac{FWHM_{10\bar{1}2}{}^2}{9b^2} \tag{3-13}$$

Hence, it is common to use the FWHM of ω scan as a measure of the quality of crystals.

3.7 Optical characterization

Optical characterization is a non-destructive characterization technique from which we can extract important physical properties, such as the quality of a film and stress/strain in the film. The two main optical characterization techniques used for this study were photoluminescence (PL) and Raman spectroscopy.

3.7.1 Photoluminescence

Luminescence is the process of emitting light upon an external excitation. Photoluminescence (PL) refers to luminescence excited by an external optical source. PL allows us to find out band edge emission and defect optical transitions of the probed sample.

To measure PL for GaN-based materials, a He-Cd laser (325 nm) is used as an excitation source. Sometimes a neutral density filter is placed between the laser and the sample to reduce the intensity of the laser beam incident on the sample (see Figure 3-9). The laser is directed at the sample and the luminescence collected from the sample into a detector. Before the detector, the collected luminescence is directed

at a monochromator, which can reflect different wavelengths of light into the detector. The monochromator is adjusted by a computer automatically, so that a spectrum of the collected PL signal can be detected and saved. The PL spectra obtained for the results in this thesis were collected from Renishaw's 2000 micro-PL setup, using the 325 nm (maximum power: 50 mW) line from a Kimmon He-Cd laser as excitation source. A microscope is incorporated with the equipment, where a spatial resolution of 1 μm or better can be achieved with a 40× objective lens. Variable temperature measurements, ranging from 15 to 300 K, could be made using a helium closed cycle cryostat.

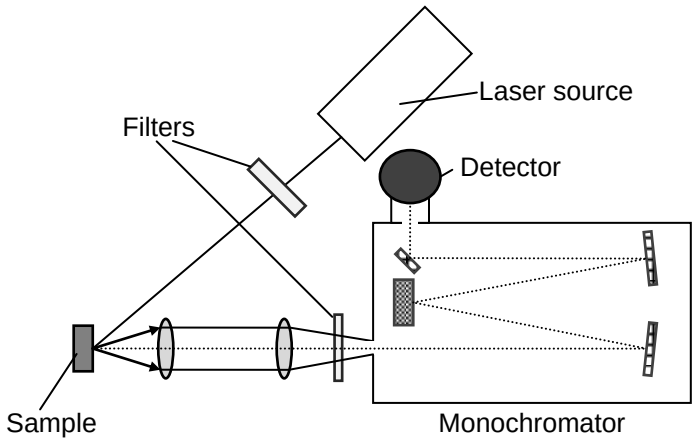

Figure 3-9. A simple schematic of a PL setup.

Band edge emission, impurity transitions and defect transitions can be revealed by PL. For excitonic transitions, the PL emissions can be fitted into a Lorentzian line shape; whereas the temperature dependence can be fitted into a Varshni equation [161, 162]. A GaN film with biaxial compressive strain will express a blueshift in its PL, while a GaN film with biaxial tensile strain will express a redshift in its PL [4]. The PL shift happens in the free excitons and bound excitons [161]. A simple relationship between band gap change and biaxial strain in wurtzite GaN can be estimated by [163]:

$$\varepsilon_{xx} = \varepsilon_{yy} \approx -\frac{\Delta E_g}{9.4\ \text{eV}} \tag{3-14}$$

where ε_{xx} and ε_{yy} are the biaxial strains and ΔE_g is the change in band gap. Similarly, a simple relationship between band gap change and biaxial stress can be estimated by [163]:

$$\sigma_{xx} = \sigma_{yy} \approx -\frac{\Delta E_g}{20 \pm 3\ \text{meV}}\,(\text{GPa}) \tag{3-15}$$

where σ_{xx} and σ_{yy} are the biaxial stress, in GPa.

3.7.2 Raman spectroscopy

A simple schematic of a Raman spectrometer is shown in Figure 3-10. The monochromatic laser beam is directed towards a holographic notch filter. This filter strongly reflects the photons of the laser wavelength, while allowing other wavelengths to transmit through. The laser beam is then directed at the sample through a conventional optical microscope setup. The scattered light is collected and dispersed by a diffraction grating. The CCD detector then captures the dispersed light and converts into recorded spectrum in a computer.

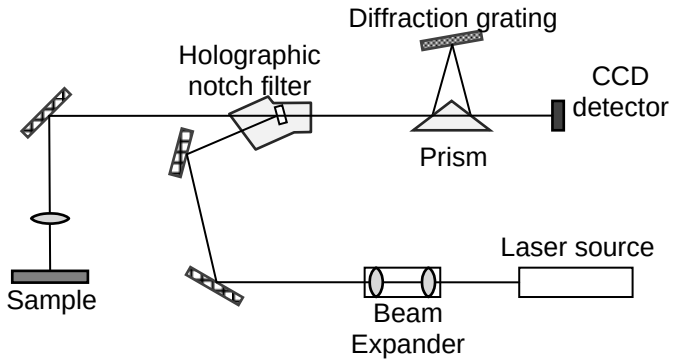

Figure 3-10. Schematic of a Raman spectrometer

Raman scattering occurs when there is inelastic scattering of light on the sample. Inelastic scattering happens when the incident light interacts with the molecules of

the sample and results in shifts in the energy of the laser. This happens because the photons transfer momentum to the molecules (resulting in phonons) and the scattered photons lose energy equivalent to the phonons' energy. This shifting provides vibrational information of the sample. The shifting is known as Raman shift. Raman shifts is calculated by:

$$\Delta\omega = \left(\frac{1}{\lambda_0} - \frac{1}{\lambda}\right) \tag{3-16}$$

where $\Delta\omega$ is the Raman shift, λ_0 is the excitation wavelength, and λ is the collected Raman spectrum wavelength. As the Raman shift is commonly expressed in cm^{-1}, the Raman shift can be calculated using:

$$\Delta\omega\ (\mathrm{cm}^{-1}) = \left(\frac{1}{\lambda_0\ (\mathrm{nm})} - \frac{1}{\lambda\ (\mathrm{nm})}\right) \times \frac{10^7\ (\mathrm{nm})}{(\mathrm{cm})} \tag{3-17}$$

For wurtzite GaN, there are several phonon modes characteristic of GaN.

Table 3-2 shows the list of phonon modes (for unstrained GaN) which can be retrieved using a Raman spectrometer. E_2(high) mode is found to be more sensitive to biaxial stress than other modes [163], and the biaxial stress can be conveniently calculated by [164]:

$$\sigma_{xx} = \sigma_{yy} = -\frac{\Delta\omega}{4.3}\ \mathrm{GPa\ cm} \tag{3-18}$$

where σ_{xx} and σ_{yy} are the biaxial stresses. This means that if the E_2(high) peak shifts to a larger value, it signifies a biaxial compressive stress, and vice versa. The Raman spectroscopy results in this thesis were obtained from Renishaw's inVia Raman system, with 532 nm laser.

Table 3-2. Phonon modes of wurtzite GaN measured by Raman spectroscopy. Figures retrieved from reference [165].

Modes	**Raman peaks (cm^{-1})**
E_2(low)	144.0
A_1(TO)	531.8
E_1(TO)	558.8
E_2(high)	567.6
A_1(LO)	734.0
E_1(LO)	741.0

Chapter 4. Nanostructured silicon by metal-assisted chemical etching

4.1 Introduction

This chapter provides a brief review of metal-assisted chemical etching (MACE). The procedures to fabricate silicon nanostructures by MACE are then presented. The physics and chemistry of MACE are explained briefly. Several experimental parameters were varied to investigate their effects on the resultant silicon nanostructures. From the results, the optimum etching conditions are then determined for controllable and reliable etching of silicon.

4.2 Introduction and basic phenomenon of metal-assisted chemical etching

In the field of semiconductors, no other material is as well researched as silicon. Hence, when great scientific attention began on nanotechnology in the 2000's, various fabrication methods were formulated to form silicon nanostructures. The methods could be broadly categorized into bottom-up and top-down approaches. Bottom-up approaches include vapor-liquid-solid (VLS) growth; top-down approaches include reactive ion etching (RIE), electrochemical etching and metal-assisted chemical etching (MACE).

MACE has garnered much scientific interest because of its several strengths [166]. First of all, it is a simple and low cost technique. After deposition of a noble metal (between 2 to 20 nm thick) on a silicon substrate, an immersion of the substrate in the

prepared etchant is all that is required to form nanostructures. Patterning can be done by using a template mask [167-171], by dewetting the metal film through annealing [172, 173], or by simply taking advantage of the spontaneously formed patterns of deposited discontinuous films [174]. No other special equipment is required. Second, crystallinity of nanostructures is generally maintained as they are etched out of high quality single crystalline silicon substrates. Third, structures of nano-size features with high aspect ratios can be formed rapidly with this technique. This is because the etch rate is fast, with reported etch rates of up to 4.5 μm/min [175], and there is no apparent limit to how small the features of fabricated nanostructures can get [166]. These are some of the reasons why metal-assisted chemical etching stands out among other nanofabrication techniques.

However, the disadvantage to using this technique is the increased probability of metal contamination. As noble metals are used to cover a large area of the substrate, there is always a chance of incomplete removal of the catalytic metal.

4.3 Literature review of silicon nanostructures formed by metal-assisted chemical etching

One of the earliest reports on MACE of silicon came from Dimova-Malinovska et al. [176]. They reported the preferential etching of silicon when aluminum is in contact with silicon. This opened a new avenue in silicon patterning. Subsequently, it was discovered that several other metals such as gold [177], silver [178] and platinum [177, 178] were also suitable as catalyst.

In MACE, a noble metal is first deposited on the silicon substrate. The noble metals found to be suitable include gold, silver and platinum, but gold is more widely used. Then a solution containing HF and an oxidizing agent is used to etch the prepared sample. The noble metal catalytically enhances etching of silicon beneath it,

compared to areas with no metal coverage. Due to downwards etching, the metal sinks into the silicon substrate. The metal coverage determines the area where preferential etching occurs, hence nanostructures of various shapes and sizes can be fabricated by controlling the metal coverage pattern.

While it is sufficient to etch silicon by using just HF mixed with an oxidizing agent, the reaction is usually very slow (at less than 10 nm/h [166]) without catalytic metal on it. The dominant explanation provided in the literature on the role of catalytic metal is that it catalyzes the reduction of the oxidant (e.g. H_2O_2 or $AgNO_3$) to produce holes in the catalyst which then migrate to the silicon to promote its oxidation. The catalytic behavior of the metal is commonly attributed to its negatively charged surface which attracts the positively charged oxidizing ions to it. Some researchers attribute this effect to the higher electronegativity of the catalytic metal, when compared to silicon [175, 179, 180]. Some researchers reasoned that it is a natural occurrence for the metal nanoparticles to gain a negatively charged surface at the solution's pH level [170]. Unfortunately, most publications merely state that the deposited metals function as catalysts without much elaboration [177, 178, 181-183]. This is because it is difficult to experimentally observe the microscopic behavior of the etching process [173].

In a particular case where the etchant consists of a mixture of HF and $AgNO_3$ [184], silicon nanostructures can be formed without prior deposition of noble metals on the substrate. The concentration of $AgNO_3$ used is usually small as too high concentrations (> 0.3 M) will not result in formation of nanostructures [185]. When silicon is immersed in the etchant, silver nanoparticles precipitate out on the substrate. The newly precipitated silver now acts as a catalyst to etch silicon. As more silver precipitates out, it naturally forms an incomplete film on the silicon surface with nanoscale patterning (size features of less than 50 nm) and dendrites eventually form. This nanoscale patterning is transferred onto silicon, thus forming an array of silicon

nanostructures. We refer this nanofabrication method as one-step MACE [186]. Due to its simplicity in creating nanopatterning, we make use of such nanopatterned substrates to investigate III-nitride growth on silicon nanostructures.

Masks formed by various techniques such as nanosphere lithography [167, 168, 187, 188], soft lithography [169], interference lithography [189], optical lithography [170], and anodic aluminum oxide [171, 190, 191] are used to form patterned metal on silicon substrate. The masks are utilized together with deposition of the catalytic metal to form the desired pattern of the required size features. The patterned metal can be fabricated either by forming the mask template before depositing the catalytic metal (negative mask pattern), or by depositing a continuous film of the catalytic metal and then subsequently patterning it with the mask template (positive mask pattern). In this way, a desired pattern can be achieved with the mask, thus attaining the required arrangement and shape of nanostructures. However, the inclusion of the mask template complicates the procedures. Even when no pre-patterning is done, a separate step is still required to deposit the catalytic metal. The additional step required prior to the chemical etching could be evaporation [187], sputtering [191], electrodeposition [181], or spin-coating [169]. Therefore, one-step etching is attractive because of the simplicity that it provides for the experimentalists. However, the simplicity comes at a cost: there is no direct control over the shape and sizes of the etched nanostructures. As an investigative research on how GaN film growth is influenced by silicon nanostructures, it is logical to use a simple nanofabrication technique. Hence, the combination of electroless deposition with MACE is attractive for our studies.

4.3.1 Effects of substrate doping and porosity

The doping level is also found to affect the roughness and the porosity of each nanostructure. The porosity here is referring to the nanostructure being microporous

or mesoporous. MACE of higher doping level silicon is found to produce rougher [192] and porous [188] silicon nanostructures, for both p-type [193] and n-type [186] silicon. In addition, a porous layer of silicon is sometimes observed to be underneath the resultant nanostructures [188] as well. Since porous silicon can form from highly doped silicon without catalytic metal in the etching solution, it was hypothesized that the etching occurs preferentially at the impurities' sites [188, 193]. The more generally accepted explanation of porous silicon formation with highly doped silicon is that diffusion of excess injected holes from the oxidant [166, 170, 194]. As it is more energetically favorable to inject holes to highly doped silicon than lowly doped silicon [193], highly doped silicon is more likely to have excess holes. These excess holes can diffuse in the silicon to sites away from the metal-silicon interface, and then subsequently oxidize silicon to form porous silicon.

The etch rate of MACE is known to be affected by the substrate doping type [166]. It was found that MACE has a slower etch rate on p-type substrates than on n-type substrates [166, 188, 195]. However, reports on the effect on the etch rate for different doping levels is not consistent in the literature. For instance, Li et al. reported similar etch rates between p^- and p^+ silicon etched by MACE [177]; whereas Cruz et al. reported that the etch rate on p^- silicon was 1.5 times faster than that on p^+ silicon [196]. It is currently unclear why the doping levels affect the etch rate [166], but it has been hypothesized that the competition between non-catalytic chemical etching of highly doped silicon and the MACE process reduces the etch rate of MACE [188].

4.3.2 Effects of the ratio of HF and oxidant

The concentration of HF and the oxidant was found to affect both the etching rate and also the morphologies of the etched nanostructures. Chartier et al. systematically studied the influence of the HF/H_2O_2 ratio on the etching rate and on the etched

morphologies of Si substrates (p-type (100) silicon wafers, 1-2 Ω cm were used), with silver as the catalytic metal [175]. They concluded that the morphologies were determined by the molar ratio ρ, which is defined as [HF]/([HF]+[H_2O_2]) [175]. When ρ is greater than 70%, Ag particles caused formation of straight vertical pores. When ρ is less than 70% but greater than 20%, cone-shaped pores were formed. For ρ less than 20%, the etching is deemed to transit into the polishing regime, hence the useful range for ρ is greater than 20%. Qu et al. found that if the H_2O_2 concentration is low at 0.1 M (or ρ ≈ 98%), the resultant nanostructures (etched from a highly doped n-type Si(100) wafer) will be solid and non-porous [186].

The reason for the increase in porosity with higher concentration of oxidizing agent is because a higher concentration will inject excessive holes to silicon [166, 170, 188]. The holes are injected through the catalytic metal into silicon. If the concentration of the oxidizing agent is low, injected holes are expected to stay within the proximity of the injected site, oxidizing silicon only at the catalytic metal. If the oxidizing agent concentration is high, there will be excessive holes injected. The excessive holes will transport away and oxidize silicon away from the catalytic metal, causing formation of microporous silicon on areas with no metal coverage.

4.3.3 Effects of substrate crystallography

The etching direction of MACE is known to be preferentially in the ⟨100⟩ crystallographic directions. For silicon (100) substrates, the etching direction is vertically downwards [184, 197]. For (110) substrates, it is observed that the etching direction is in the [100] direction, forming slanting silicon nanostructures [197]. For silicon (111) substrates, it has been reported that etching silicon with a 10-50 nm thick Ag nanoparticles using 4.6 M HF and 0.44 M H_2O_2 resulted in slanted nanostructures in [100] directions [198], with a minority in the vertical [111] direction [197]. Subsequently, Huang et al. [199] found that the etching direction on

silicon (111) substrates could be controlled between [100] and [111], by changing the concentration of the oxidant. It was found that lower oxidant concentration leads to etching in the [100] direction, while higher oxidant concentration leads to etching in the [111] direction. Huang et al. suggested that this occurs because there exist two competing dissolution processes of silicon, namely Model I and Model II [199]. In Model I, direct dissolution of silicon occurs, as in Equation (4-1) [199]:

$$\mathrm{Si(s)} + 4\mathrm{HF_2^-} \rightarrow \mathrm{SiF_6^{2-}} + 2\mathrm{HF} + \mathrm{H_2} + 2\mathrm{e^-} \quad (4\text{-}1)$$

In Model II, silicon oxide forms first before dissolution of oxide, as given in Equation (4-2) and (4-3) [199]:

$$\mathrm{Si(s)} + 2\mathrm{H_2O} \rightarrow \mathrm{SiO_2(s)} + 4\mathrm{H^+} + 4\mathrm{e^-} \quad (4\text{-}2)$$

$$\mathrm{SiO_2(s)} + 6\mathrm{HF} \rightarrow \mathrm{H_2SiF_6} + 2\mathrm{H_2O} \quad (4\text{-}3)$$

Huang et al. argued that when the oxidant concentration is low, the etching is limited by the transfer of electrons, causing it to proceed by Model I. As silicon undergoes direct dissolution, the prevailing etching direction is in the [100] direction due to the lower back-bond strength of the (100) planes when compared to (111) [200]. When oxidant concentration is high, it is suggested that the oxide formation is fast, thus oxide is formed first before it is subsequently dissolved by HF in the solution [199]. As formation of oxide occurs preferentially underneath the catalytic metal, the etching direction is vertically downwards. Note that as oxide etching is isotropic, the difference in back-bond strengths between different planes does not matter.

4.4 Silicon nanostructures preparations

The fabrication of Si nanostructure arrays closely follows that of Peng et al., Tan et al. and Cheng et al. [184, 201, 202]. Prior to etching, Si(111) wafers (n-type, phosphorus doped with resistivity of 1-10 Ω cm) were cleaned in acetone, isopropyl alcohol (IPA)

and deionized water (DI H_2O) sequentially in ultrasonic bath for 5 min each. This was to ensure the wafers were free of organic grease. The wafers were then immersed in piranha solution, heated on a hotplate set to 200 ℃, for 20 min. The piranha solution is prepared by mixing sulfuric acid (97%) and hydrogen peroxide (33%) in 3:1 volume ratio. This piranha solution acts as an aggressive oxidant to remove organic contaminants. After piranha cleaning, the back surfaces of the silicon wafers were spincoated with photoresist. This protects the back surfaces from the etching solution. As the silicon wafers were left with a thin layer of silicon oxide after piranha cleaning, the wafers were etched in diluted HF solution for 1 min to remove the oxide. The hydrophobic surface of silicon wafers indicates the oxide was removed. The silicon wafers were then rinsed with running deionized water for about a minute.

For the etching of silicon, a water bath of the required temperature (ranging from 10 to 65 °C) was prepared and a Teflon beaker containing HF and $AgNO_3$ of the required concentration (ranging from 1.0 to 7.0 M for HF concentration and 0.01 to 0.04 M for $AgNO_3$ concentration) was placed in the bath. To ensure that the temperature of the etching solution was as close as possible to the required temperature, the beaker was placed inside the temperature bath for 10 min before commencement of the etching. The wafer was then immersed into the beaker for etching. After immersion for the required duration, the wafer was transferred quickly into a beaker of deionized water to halt etching. The substrate was then rinsed with copious deionized water to remove any etching solution.

The etched wafers were covered by a thick coating of silver dendrites (Figure 4-4). To remove the silver dendrites deposit, the wafers were placed in a solution of nitric acid, hydrochloric acid and deionized water (where HNO_3:HCl:DI H_2O had a volume ratio of 1:1:1). After 30 min, the wafer was retrieved and then rinsed with deionized water. The etched wafers were then immersed in acetone then IPA to remove the

protective photoresist on the back surface. After rinsing in deionized water, the substrates were blown dry with nitrogen.

TEM analysis was done on the silicon nanostructures to verify their crystallinity. From Figure 4-1, we can observe that the nanostructures retained their single crystal nature, with their longitudinal axes parallel to the ⟨111⟩ direction, which is normal to the wafer surface. The substrates used were Si(111), so this also showed that the etching direction of this process is generally vertical and perpendicular to the substrate surface. Microporous silicon [175] was not observed, as lightly doped silicon wafers were used [203].

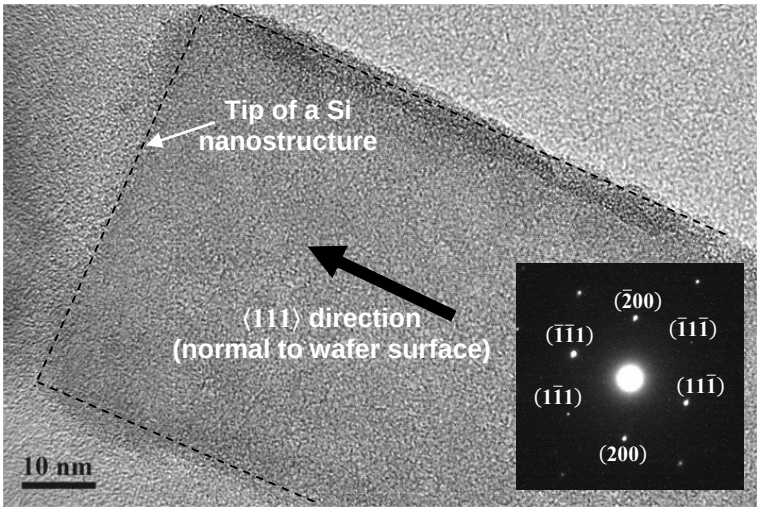

Figure 4-1. TEM image of the tip of a typical silicon nanostructure etched by one-step MACE from a Si(111) wafer. Inset shows the SADP, where the sharp defined spots indicated that the nanostructure maintained its high crystallinity. It can be seen that the longitudinal axis of the nanostructure lies along the ⟨111⟩ direction, which is also the normal of the wafer. The broken black lines are visual aids which outline the silicon nanostructure.

4.5 Chemistry and thermodynamics of one-step metal-assisted chemical etching

Before etching occurs, a reduction of the silver ions happens on the silicon surface, where the reduction half-reaction is [180]:

$$\mathrm{Ag^+} \rightleftharpoons \mathrm{Ag(s)} + \mathrm{h^+} \tag{4-4}$$

As a redox reaction, there is a corresponding oxidation reaction where silicon is oxidized, following the chemical half-reaction [175, 180]:

$$\mathrm{Si(s)} + 2\mathrm{H_2O} + 4\mathrm{h^+} \rightleftharpoons \mathrm{SiO_2(s)} + 4\mathrm{H^+} \tag{4-5}$$

The presence of HF will then subsequently etch away the silicon oxide, where:

$$\mathrm{SiO_2(s)} + 6\mathrm{HF} \rightarrow \mathrm{H_2SiF_6} + 2\mathrm{H_2O} \tag{4-6}$$

After the initial silver deposition, the reaction then proceeds through the mechanism of MACE, described earlier in this Chapter. The reaction can be separated into cathode (at the liquid-silver interface) and anode (at the silver-silicon interface) reactions. The cathode reaction is given by Equation (4-4), and the anode reaction is given by [175]:

$$\mathrm{Si(s)} + 6\mathrm{HF} + n\mathrm{h^+} \rightarrow \mathrm{H_2SiF_6} + n\mathrm{H^+} + \frac{4-n}{2}\mathrm{H_2}\uparrow \tag{4-7}$$

Hence, the overall reaction is described as:

$$n\mathrm{Ag^+} + \mathrm{Si(s)} + 6\mathrm{HF} \rightarrow n\mathrm{Ag(s)} + \mathrm{H_2SiF_6} + n\mathrm{H^+} + \frac{4-n}{2}\mathrm{H_2}\uparrow \tag{4-8}$$

The chemical reaction can be understood by the schematic shown in Figure 4-2. In the first part of the reaction, silver ions are reduced to solid silver and nucleate on the silicon surface (A in Figure 4-2). The nucleation of silver will inject holes into silicon, causing oxidation to form silicon oxide. This nucleation is a process which will occur at energetically favorable sites. Since the silicon wafer is atomically flat, nucleation happens randomly (see Figure 4-3). Note that the density of the nanoparticles is much less than the density of the nanostructures (see Figure 4-5). This is because as there is

no HF in the solution, oxidizing silicon will form silicon oxide. The reaction will rapidly proceed until the silicon surface is coated completely with a thin protective layer of silicon oxide. Since only a limited amount of silicon is oxidized, only a limited amount of silver is precipitate out before the reaction halts completely.

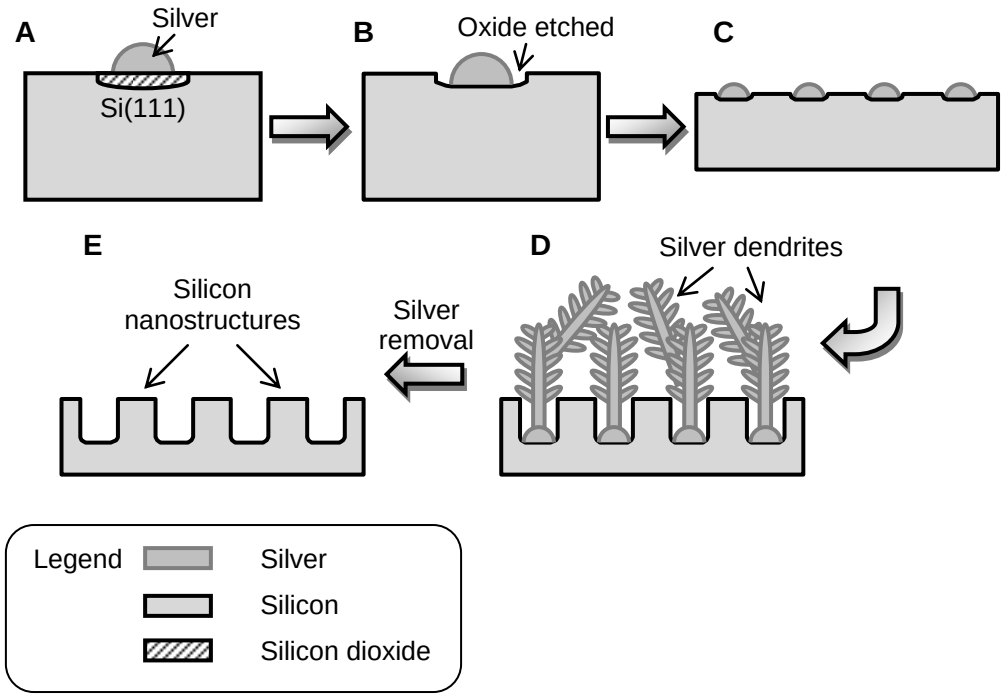

Figure 4-2. Schematic of the formation of silver dendrites and silicon nanostructures.

Next, the presence of HF in the solution will etch away the silicon oxide and cause the silver nanoparticles to be in direct contact with the silicon substrate (B in Figure 4-2). The randomly nucleated silver will decorate the whole silicon wafer (C in Figure 4-2). Once silver is in direct contact with silicon, the process proceeds through the mechanism of MACE. Silver ions preferentially precipitate on existing silver rather than on silicon, while a simultaneous silicon etching occurs beneath the silver which is in direct contact with silicon. As the etching proceeds, more and more silver will be precipitated. The precipitated silver will eventually form a network of silver dendrites, and sink into the silicon substrate to form nanostructures (D in Figure 4-2).

The difference between this one-step MACE and other forms of MACE is that catalytic metal (silver in this case) is precipitated out simultaneously with etching. After the required duration for etching is done, silver can be etched away by using a mixture of HCl, HNO_3 and deionized water, leaving behind silicon nanostructures (E in Figure 4-2). This method is simple as only one step is required (other than the cleaning steps), but the disadvantage is that there is no control over the deposition of silver.

The typical appearance of the final silicon nanostructures can be represented by Figure 4-5. The widths of the nanostructures are between 20 to 60 nm, and they compose about 30-40% of the silicon surface area (or about 60-70% of the surface was etched down).

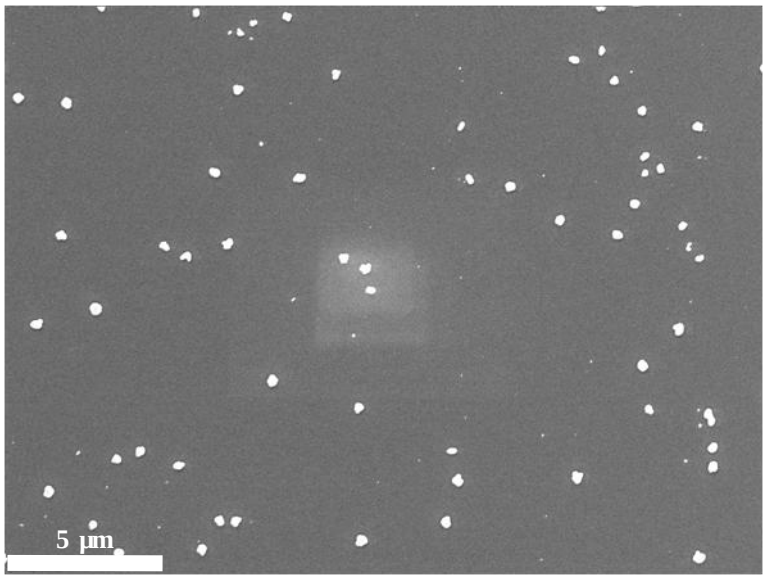

Figure 4-3. SEM micrograph of silver nanoparticles (in white) nucleated on silicon in a solution with 0.02 M $AgNO_3$ (with no HF). It can be observed that the silver nanoparticles nucleate randomly over the silicon surface.

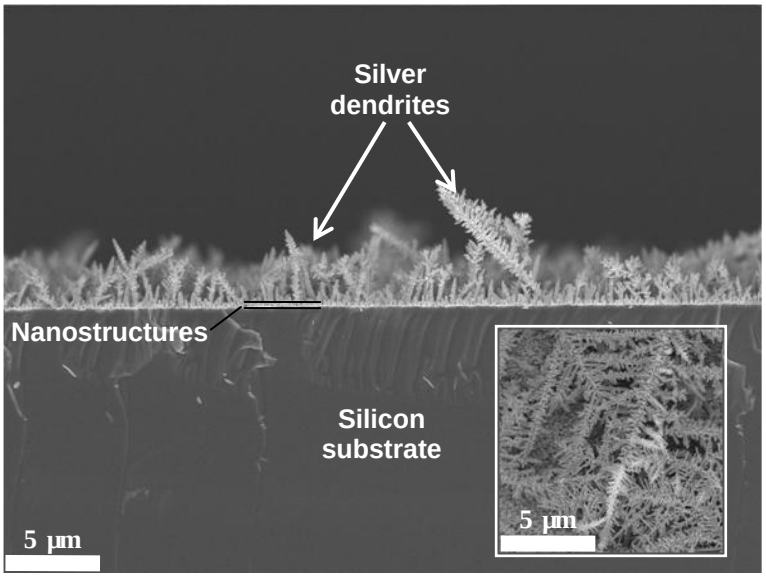

Figure 4-4. Cross-sectional SEM image of silicon wafer after etching in the $AgNO_3$ and HF solution. The thick film of silver dendrites reached about 5 μm in height after one minute of etching. Inset shows the plan view of the silver dendrites.

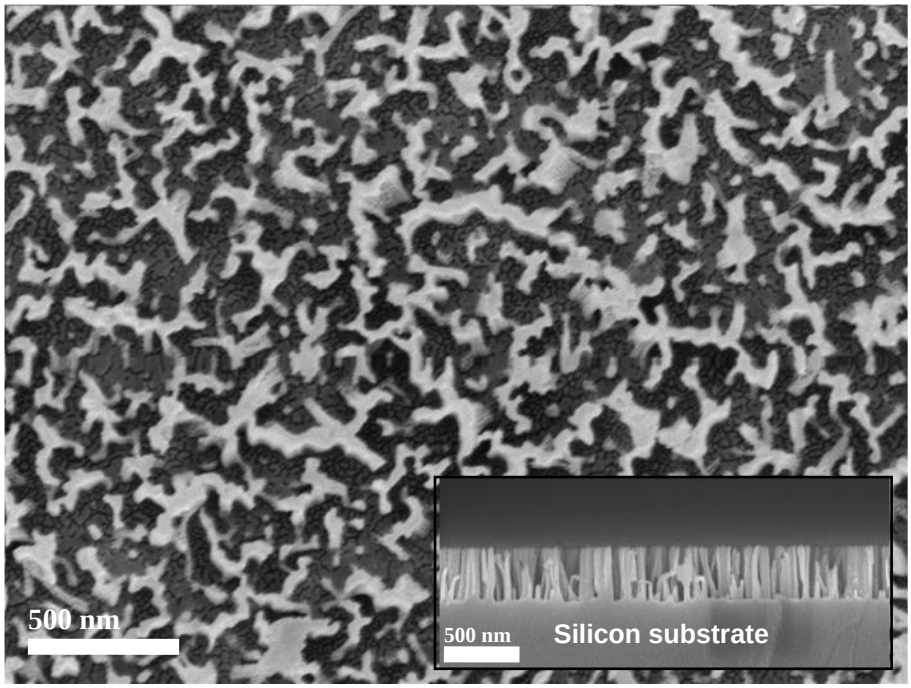

Figure 4-5. SEM image of a typical silicon nanostructured substrate etched by the one-step MACE process. The nanostructures have widths from 20 to 60 nm and occupy about 30-40% of the substrate's surface area. Darkened areas denote where etching has taken place. Inset shows a cross-sectional SEM of the silicon nanostructure array.

4.6 Experimental factors affecting results

The etching conditions given by Peng et al. [184] were followed (5.0 M HF and 0.02 M $AgNO_3$ at 50 ℃). However, after just 1 min of etching, it was found that the "skyline" (collective outline of the nanostructures' tips) was not flat (see Figure 4-6). This suggested that some form of damage was inflicted on the nanostructures' tips, where the tips were removed partially forming recessed tips. Such recession of the nanostructures' tips had been reported elsewhere but at a much lower HF concentration and for longer etching duration [204]. Unfortunately, the authors did not identify nor suggest any reasons for such recession. This is undesired because the top surface of the nanostructure should be Si(111) plane, which is the silicon's most ideal crystallographic face for III-nitride growth. Subsequently, it was found that stirring the solution while etching provided a better morphology (flat "skyline").

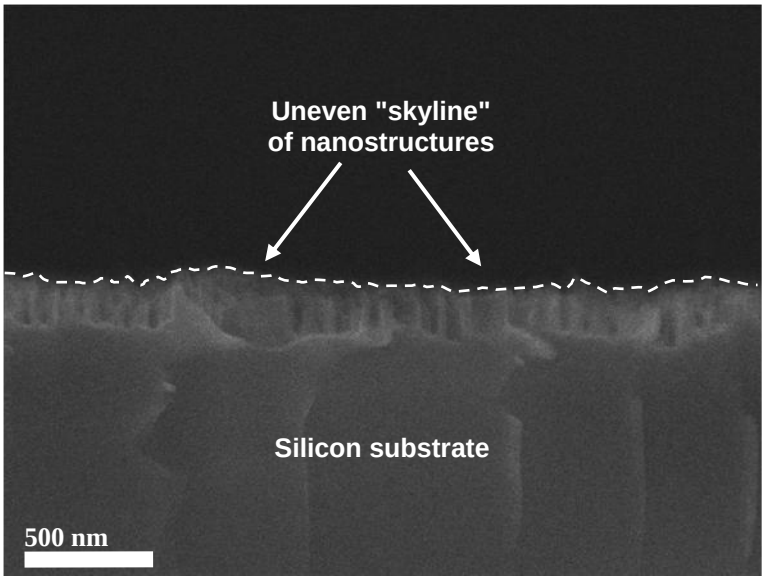

Figure 4-6. Silicon nanostructures etched for 1 min in solution containing 5.0 M HF and 0.02 M $AgNO_3$ at 50 ℃. The broken white line outlines the uneven "skyline" across the nanostructures, indicating that some form of damage was inflicted on the top surface.

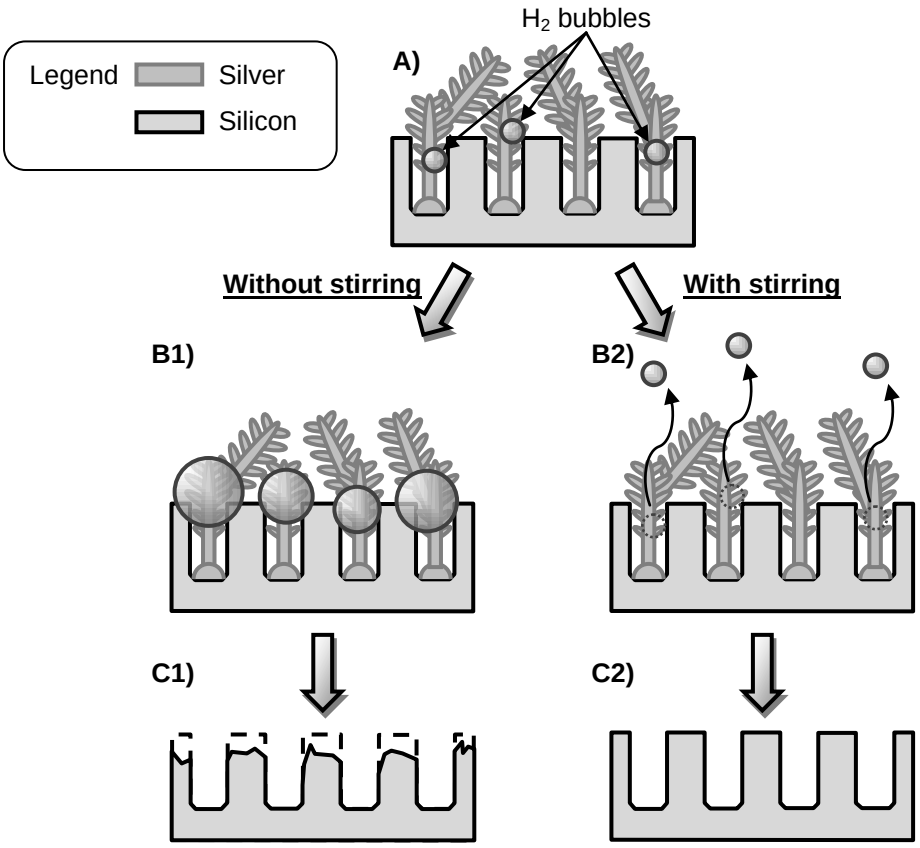

Figure 4-7. Schematic of a proposed mechanism on how stirring of the etching solution reduced (or eliminated) the damage observed on the tip of silicon nanostructures. (A) When etching is done at higher temperatures, hydrogen bubbles evolve at a significant rate. When stirring is not implemented, (B1) the bubbles are attached to the nanostructures long enough to grow to a size, (C1) which can significantly damage the tip of the nanostructures. When stirring is implemented, (B2) the agitation allows the hydrogen bubbles to detach from the nanostructures while they are still small. Thus, (C2) avoiding mechanical damage to the silicon nanostructures' tips.

The following explanation is suggested. As etching at higher temperatures has a higher etch rate, hence hydrogen will be generated, according to Equation (4-8), at a higher rate. Escaping hydrogen bubbles impose strains on the silicon nanostructures as they escape out of the etching solution, and this got worse with higher hydrogen generation. The evolution of the hydrogen bubbles is sufficiently violent to damage the top regions of the fragile nanostructures, by breaking them mechanically. Stirring agitates the solution and allows the hydrogen bubbles to escape at a higher rate, allowing the hydrogen to escape as small bubbles. This effectively reduced the strain from escaping hydrogen bubbles. An illustration of both mechanisms can be

represented by Figure 4-7. Etching at lower temperatures (i.e. 25 ℃) does not have such undesirable recessions because the hydrogen gas did not evolve violently as the etch rates are slower. However, stirring would increase the likelihood of silver removal from the silicon surface, and etching would be stopped. Therefore, it is frequent to observe shiny swirl marks on the surface after etching, as etching halts in those areas due to silver removal. It should also be noted that stirring of the solution also results in faster etching. Hence, both stirring and no stirring were implemented for this investigation, depending on which was necessary.

4.6.1 Silver nitrate concentration

The silver nitrate concentration was varied to find out its effect on the etching reaction. The etching was done at 50 ℃ for 1 min with the etching solution containing 5.0 M HF, and stirring was implemented. Only the silver nitrate concentration was varied. Three different concentrations were used for comparison: 0.01 M, 0.02 M and 0.04 M. The concentration of silver nitrate was not varied too much, as large deviations were known to be unable to form nanostructures [185]. As etched nanostructures were significantly recessed [204] when etched with one of the etching condition (5.0 M HF, 0.04 M $AgNO_3$ 50 ℃, with stirring), another set of specially prepared substrates was used to determine the recessed depth.

For this set of experiments, the Si(111) substrates were coated with lines of photoresist (MicroChemicals AZ 5214E), which covers about 20% of the substrate's surface. The area covered by the photoresist will be protected against the etching solution [204]. The substrates underwent a descum process using a reactive ion etching (RIE) system before MACE was done. This is to ensure the exposed surface is free of organic contaminants.

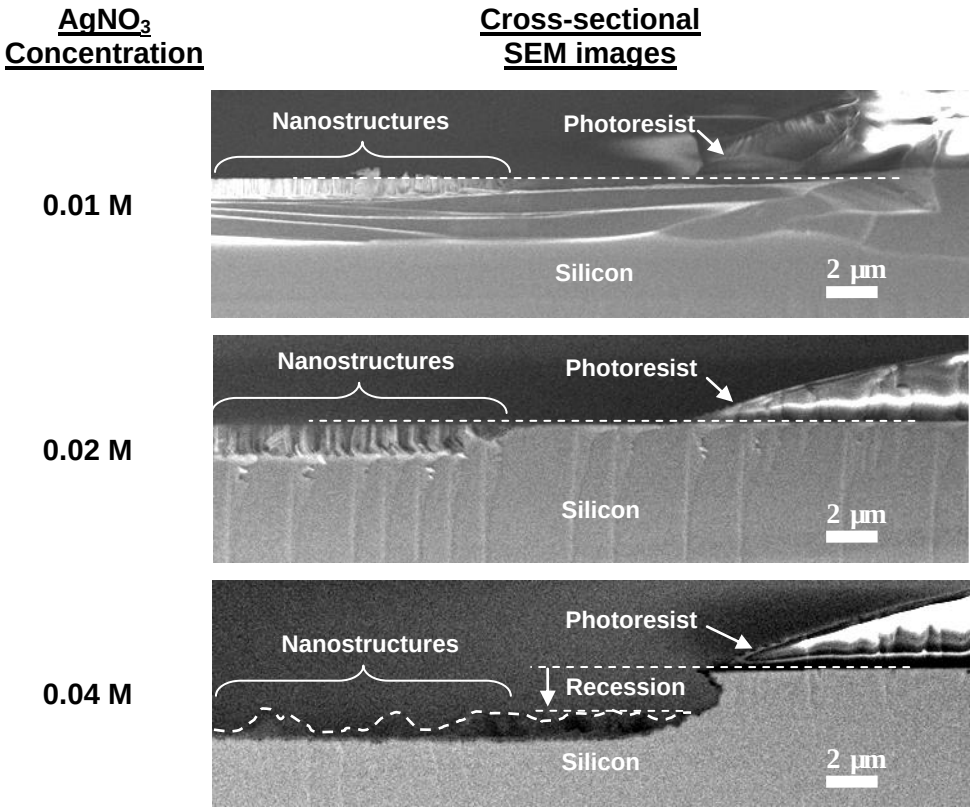

Figure 4-8. Cross-sectional SEM images of nanostructures after 1 min of chemical etching at 50 ℃ in a solution containing 5.0 M HF and different $AgNO_3$ concentrations (0.01, 0.02 and 0.04 M). Stirring was implemented. Recession of the nanostructures is only observed for substrates etched using the etching solution with 0.04 M $AgNO_3$. The "skyline" of the nanostructures etched using the etching solution with 0.04 M $AgNO_3$ is outlined by the jagged broken line.

After etching, the recessed depth can then be determined by comparing the regions protected by the photoresist and the exposed regions. From Figure 4-8, it can be seen that only the nanostructures etched out using the solution with 0.04 M $AgNO_3$ have recessed nanostructures, while nanostructures etched out using 0.01 and 0.02 M $AgNO_3$ have their tips level with the protected silicon surface. It is interesting to note that for etching using the solution containing 0.01 and 0.02 M $AgNO_3$, the etched out nanostructures did not form on regions just next to the boundary of the photoresist, but only after about 6 μm away from the boundary. The etch rates of both 0.01 M and 0.02 M was found to be about 700 nm/min and 1300 nm/min, respectively. The height of the nanostructures formed using the solution with 0.04 M $AgNO_3$ was found

to be about 730 nm tall; but a significant recession of the nanostructures was observed to be about 1200 nm deep. Hence, the total etch rate for the 0.04 M $AgNO_3$ solution was almost 2000 nm/min.

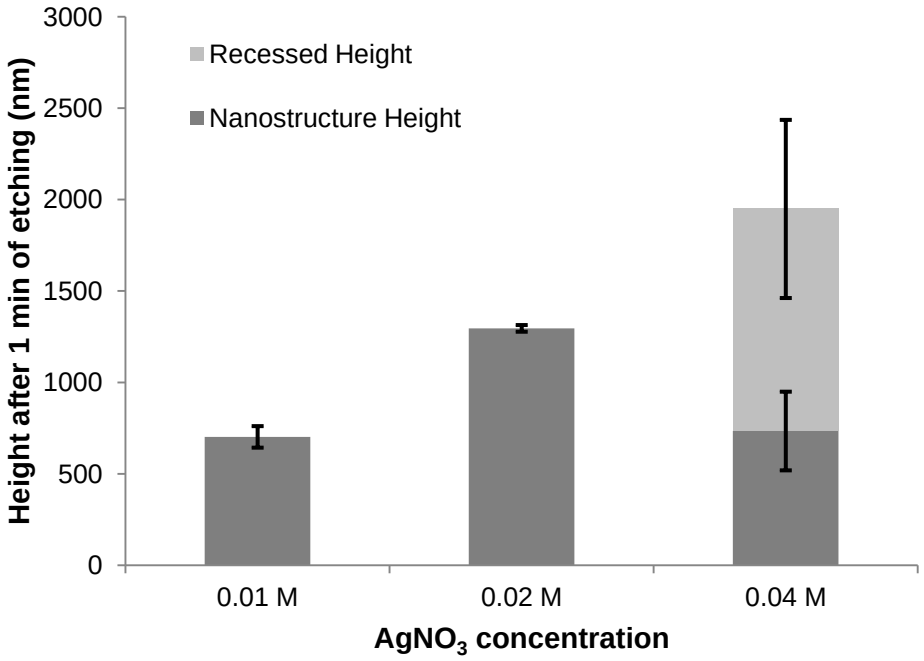

Figure 4-9. Graph comparing the nanostructures' height after 1 min of chemical etching at 50 ℃ in a solution containing 5.0 M HF and varying $AgNO_3$ concentrations. Stirring was implemented. Cross-sectional SEM images of the different $AgNO_3$ concentrations are given in Figure 4-10.

From the cross-sectional SEM image (see Figure 4-8), it was observed that the "skyline" was not flat as well. This seems to suggest that the higher $AgNO_3$ concentration provided too high a driving force toward silver nanoparticle precipitation, such that a very compact film of coagulated silver nanoparticles formed. The highly compact silver agglomerate does not allow very tall nanostructures to be formed. As the silver sinks into silicon, a film of the silver nanoparticles will eventually be in direct contact with the nanostructures' tips. Etching of the tips would then occur through metal-assisted chemical etching. A schematic of this excessive etching mechanism is illustrated in Figure 4-10. In order to avoid the excessive tip

etching, the substrate we prepared for MOCVD growth was etched with a solution containing 0.02 M silver nitrate.

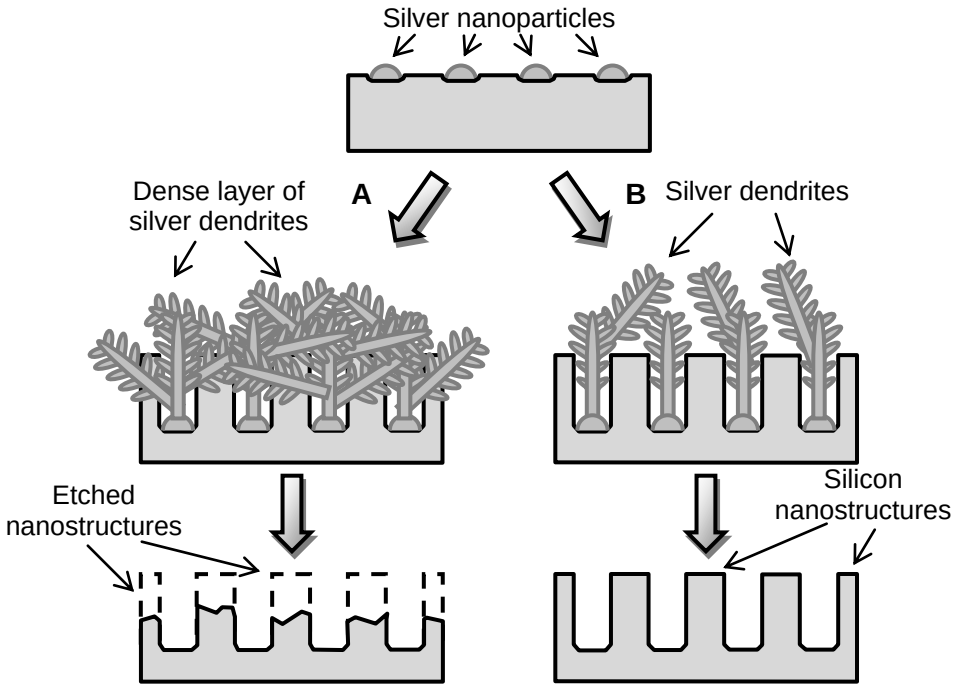

Figure 4-10. Schematic showing how a dense layer of silver dendrites (A) results in etching of the silicon nanostructures' tips and a less dense layer of silver dendrites (B) leaves the silicon nanostructures' tips intact.

4.6.2 Temperature

A temperature variation of between 10 to 65 ℃ of the etching solution was done. The rest of the etching conditions remained constant (i.e. immersion for 1 min in etching solution containing 5.0 M HF and 0.02 M $AgNO_3$ was done). Stirring was implemented in this study. We confirmed that the etching rate increases with temperature. To be specific, the etch rates increases in the form of Arrhenius equation, in the form of etch rate = A $\exp(-E_a/kT)$, where A is a constant, E_a is an activation energy, k is Boltzmann's constant and T is temperature in kelvins. We fit the Arrhenius equation to our experimental values and found the activation energy to be 0.33±0.02 eV. This value is close to the 0.36 eV determined by Cheng et al. [202] and

the 0.37 eV determined by Nassiopoulou et al. [205], which they had determined for Si(100) substrates. In addition, this activation energy is similar to that for etching SiO_2 with HF, as determined by Judge (between 0.35 to 0.40 eV) [206]. This suggests that the rate limiting reaction is likely to be the same as that of etching SiO_2 in HF; however, stronger evidence is necessary to confirm this.

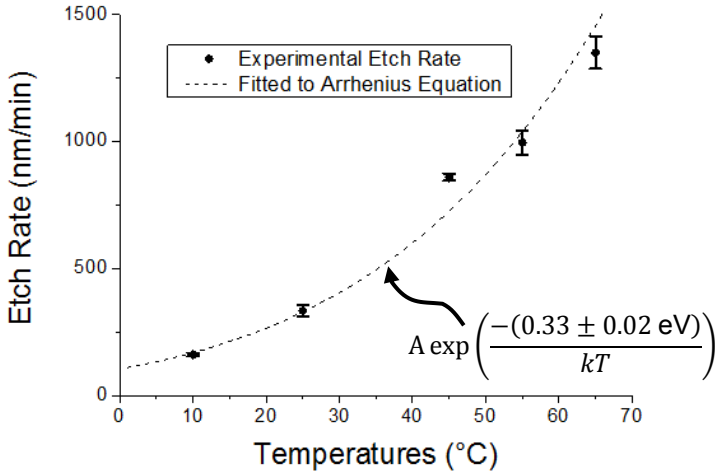

Figure 4-11. Graph of etch rate against temperature of the etching solution (5.0 M HF, 0.02 M $AgNO_3$). The etching duration was fixed at 1 min. The broken line plot is fitted to an Arrhenius equation, based on the experimental data.

Upon closer inspection, the arrays of nanostructures did not have their tips aligned to a flat plane for etching done at 55 ℃, and this is even worse at 65 ℃. This indicates that although a higher temperature would provide a faster etch rate, it tends to damage tips of nanostructures. This signified that tips will still be damaged even with stirring (possibly by more violent hydrogen bubble evolution), at elevated temperatures. Since the purpose of stirring is to avoid tip etching, yet they still occur at elevated temperatures, it is favorable to etch at lower temperatures. Since the etch rates were determined by measuring the height of the resultant nanostructures, the etch rates at higher temperatures will be underestimated. With this in mind, it should be noted that

the calculated activation energy is an underestimated value. This is consistent with the lower calculated activation energy (0.33 eV) when compared with the literature.

When etched without stirring at 25 ℃, it was found that the "skyline" of the etched substrate is still flat after 1 min of etching. The etch rate for 25 ℃ was found to be about 90 nm/min, which is almost 4 times slower than with stirring (330 nm/min).

4.6.3 Hydrofluric acid concentration

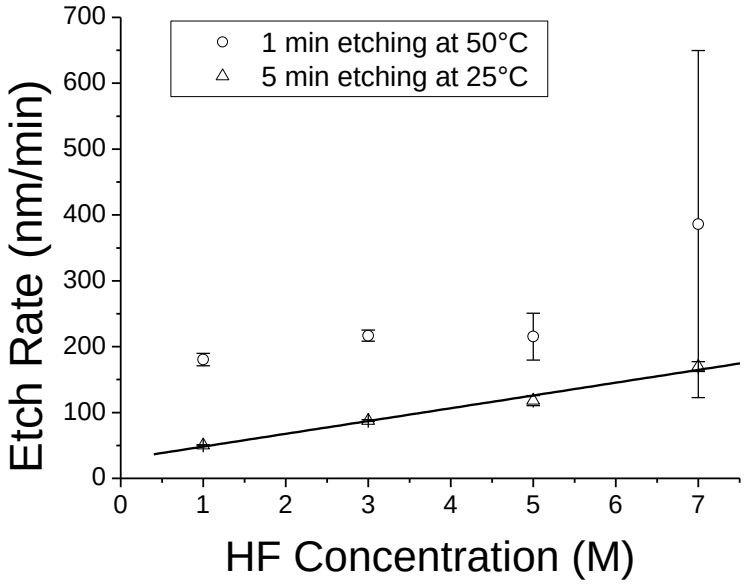

Figure 4-12. Graph of etch rate against HF concentration. Data points in circles were obtained from 1 min etching at 50 ℃, and data points in triangles were obtained from 5 min etching at 25 ℃. The $AgNO_3$ concentration was fixed at 0.02 M. No stirring was implemented. The higher errors for etching at 50 ℃ at higher HF concentrations are derived from the uneven etching from the etching conditions. The black line serves as a visual aid to mark the linear relationship between etch rate and HF concentration for 25 ℃.

The HF concentration was varied to investigate how it would affect the nanostructure formation. Initially, the etching conditions were fixed at 50 ℃, 0.02 M $AgNO_3$ for 1-minute etching, with only HF concentration being varied from 1.0 to 7.0 M. No stirring was implemented. It was found that the etch rate increased with increasing

HF concentration; at the same time, increasing HF concentration also increased the damage done to the tips of the nanostructures, and serious uneven etching occurs at 7.0 M HF. This makes such etching conditions very undesirable.

In the next series of experiments, the etching temperature was reduced to 25 ℃ and the etching time was increased to 5 min. The etching time was increased to 5 min as it is easier to measure the height of taller nanostructures. From Figure 4-12, it can be seen that the etching rate of experiments at 25 ℃ closely followed a linear relationship with HF concentration. This supports that HF is involved in the process and that its consumption is part of the rate limiting process. However, it should be noted that this does not verify the existence of an intermediate oxide. HF will be part of the rate limiting process, whether silicon forms an intermediate oxide first or silicon oxidizes directly to H_2SiF_6.

4.6.4 Etching duration

A series of experiments were done to determine how the height of the nanostructures varies with the etching duration. The etching solution used was fixed at 0.02 M $AgNO_3$ and 5.0 M HF at 25 ℃. No stirring of the solution was used. It was found that the etching follows an approximately linear relationship with the etching duration (see Figure 4-13).

It was reported by several researchers that the etching rate has a linear relationship with etching duration [202, 207]. However, we found that there are two distinct regimes, a short etching time regime and a long etching time regime. The short etching time regime was found to have an etching rate of 1.51 nm/sec, which after 100 s it increased to 2.70 nm/sec. This seemingly contradicts Ozdemir et al.'s observations [208] where they reported a decrease of the etching rate after some time. This is because their observation was for much longer etching periods (up to 600 min)

than our experiments (up to 600 s). Hence, we suspect that the etch rate for our setup would decrease after a few hours as well.

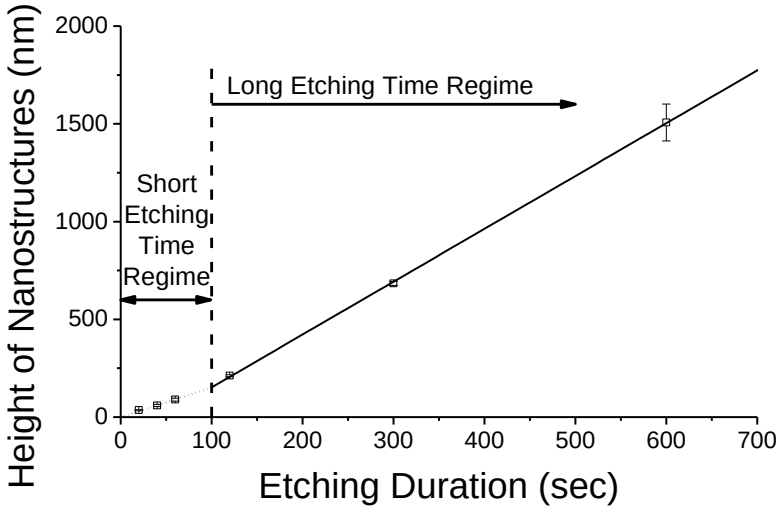

Figure 4-13. Graph of height of etched nanostructures against etching time. Etching conditions were 25 ℃, 0.02 M $AgNO_3$ and 5.0 M HF, and no stirring was used. The lines serve as visual aids for the linear relationships, where the dotted line is for the short etching time regime and solid line is for the long etching time regime.

We attribute this change of etching rate to the catalytic characteristics of the dendritic silver film. In the short etching time regime (less than 100 s), silver precipitated to form discontinuous film over the whole wafer with formation of few silver dendrites (see Figure 4-14a-c). When the dendrites have sufficient coverage over the sample (see Figure 4-14d-e), the etching changed into the long etching time regime (more than 100 s) with faster etching. A possible reason is that the large surface area of silver dendrites, which are efficient in capturing silver ions for the redox reaction. It should be noted that the 100-second transition time is expected to vary with etching conditions. The time over which etching transforms to the next regime should strongly depend on how fast silver dendrites are formed.

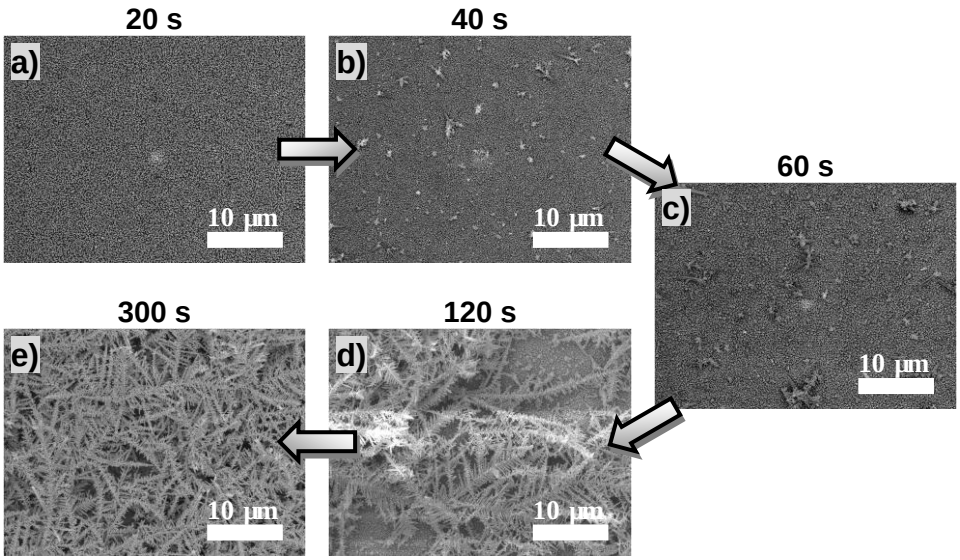

Figure 4-14. Plan view SEM images showing the evolution of the dendritic silver film coverage with etching duration by one-step MACE in 5.0 M HF and 0.02 M $AgNO_3$ at 25 ℃. The etching duration is indicated above the corresponding SEM image. After 20 s of etching (a), a negligible amount of silver dendrites were formed (only silver nanoparticles formed, which are not distinguishable at this magnification). After 40 s of etching (b), small clusters of silver dendrites (about 1 to 2 µm in size) started appearing over the surface. After 60 s of etching (c), the clusters of silver dendrites grew, with some reaching 10 µm in size. However, the silver dendrites only occupied less than 10% of the total substrate's surface. Beyond 120 s of etching (d and e), silver dendrites covered more than half of the total substrate's surface.

For etching times of 5 min or less, there existed only small variations in the height of nanostructures. In addition, the height of nanostructures can be controlled easily by varying the etching duration, as it follows very closely the linear relationship with 2 regimes: short etching time regime (below 100 s) and long etching time regime (100 to 600 s). This shows that this selected etching condition (25 ℃, 5.0 M HF, 0.02 M $AgNO_3$, and no stirring) is both reliable and controllable (by adjusting the etching time) to obtain the desired nanostructure height.

4.6.5 Size variation of nanostructures with etching duration

The feature size of the nanostructures was found to change with etching duration. The feature sizes were obtained by taking the average nanostructure size, based on measurements done on plan-view SEM images. As seen from Figure 4-15, size

features of the silicon nanostructures remained generally the same until after 60 s of etching. When the etching duration reached 120 s, the trenches appeared to have widened from about 80 nm to 100 nm. When the etching duration reached 300 s, the widths of the trenches seemed to increase to about 120 nm. The apparent increase in nanostructure size after 300 s of etching is because of capillary-induced agglomeration [209] between nearby nanostructures, making them look like larger nanostructures. This is probably due to the high aspect ratio of nanostructures (about 10) after 300 s of etching, which caused them to bend easily [210]. Capillary forces act on the nanostructures during drying, which pull the nanostructures together and pin them together [209].

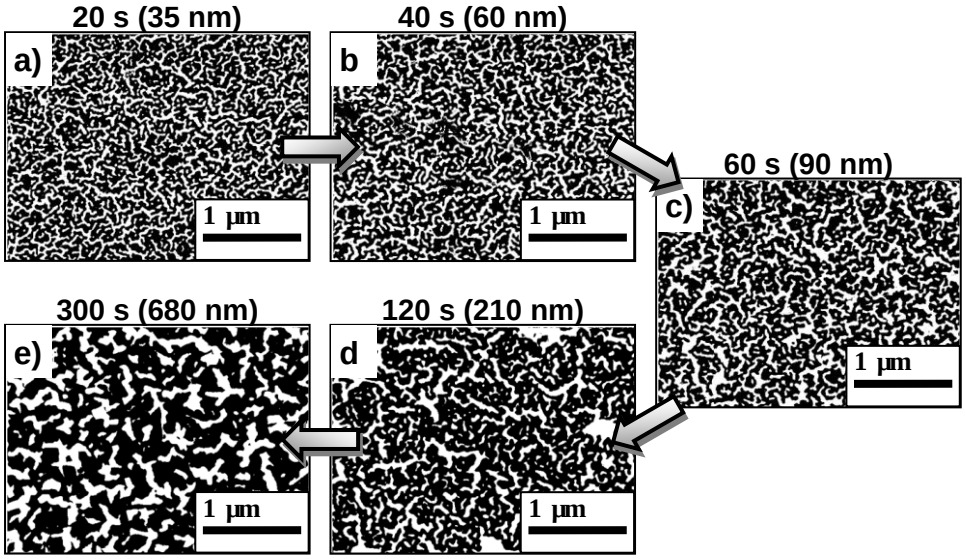

Figure 4-15. Plan-view SEM images of silicon nanostructures etched for various durations by one-step MACE in 5.0 M HF and 0.02 M $AgNO_3$ at 25 ℃. The etching duration is indicated above the corresponding SEM image. The images are converted to black and white so that it is easier to compare the SEM images visually. The white areas are the standing silicon nanostructures and the black areas are the etched trenches.

4.7 Conclusion

We have characterized the formation of silicon nanostructures using a simple and low cost 1-step electroless etching technique, where crystallinity of the substrate is maintained. However, the disadvantages of this technique are that there could be contamination due to the presence of the catalytic metal and there is little control over the position, size and shape of the nanostructures. The mechanism of electroless etching was discussed and we investigated the effects of varying several etching conditions, such as the $AgNO_3$ concentration, temperature, HF concentration, and etching duration, systematically. It was found that several etching conditions would damage the nanostructures' tips, either by violent evolution of hydrogen bubbles or excessive tip etching by a dense layer of silver dendrites. Such conditions include a silver nitrate concentration of 0.04 M, temperature at 55 ℃ or higher, and HF concentration of 7.0 M. We have also obtained the activation energy of this reaction as 0.33 ± 0.02 eV by fitting to an Arrhenius equation, which is close to the activation energy of SiO_2 etching with HF. This suggested that the rate limiting reaction of one-step MACE resembles that of etching SiO_2 in HF. Finally, we found a suitable etching condition (25 ℃, 5.0 M HF, 0.02 M $AgNO_3$, and no stirring) which produces desirable structures with little nanostructure tips etching, up to 600 s. The height can be controlled by adjusting the etching duration. 2 distinct regimes are also observed: short etching time regime and long etching time regime.

Chapter 5. III-nitride growth on nanopatterned silicon substrates

5.1 Introduction

The aim of MOCVD growth on nanopatterned silicon substrates is to obtain III-nitride films on top of the silicon substrates. This is to reap the benefits as described in earlier chapters of a compliant substrate. We found out that it is critical to have a thin AlN nucleation layer and short enough silicon nanostructures in order to form a smooth GaN layer. We have also compared various different growth structures as buffer layers for comparison of their effectiveness in producing a good quality GaN layer. The GaN grown on flat silicon was placed against GaN grown on nanopatterned silicon, indicating some material improvements compared to using nanopatterned silicon.

To start off the discussion of growth of GaN on silicon, we should investigate the nucleation aspect as that is the first layer deposited on silicon. Due to several intrinsic material differences described in Chapter 1, direct deposition of GaN is incompatible with silicon [48]. One serious problem is meltback etching, which can be avoided by using a thermally stable AlN as the first layer (as described in Chapter 2). Therefore, AlN nucleation is important as it is the first step towards forming a good III-nitride material on silicon. Some growth parameters, such as the chamber pressure and growth rates, were varied in the investigation of AlN nucleation on silicon nanostructures.

In this chapter, the growth of GaN on nanostructured silicon will be examined. As an AlN nucleation layer is required before the growth of GaN, studies were done on AlN

deposition on silicon nanostructures. The chamber pressure and growth rates were varied, and effects of such variations in parameters are discussed. The height of nanostructures was also varied to observe the height effect on subsequent GaN growth. Different growth structures were then implemented on nanostructured silicon and compared. The quality of GaN layers was also compared between those grown on nanostructured silicon and flat silicon.

5.2 AlN nucleation on silicon nanostructures

Growth was performed in an EMCORE D125 MOCVD system, with TMAl and ammonia as source gases. Hydrogen was used as the carrier gas. Before growth, the samples consisting of nanostructured silicon were etched in dilute HF for 1 min to remove the native oxide. The samples were then rinsed in deionized water and blown dry with nitrogen, before they were loaded into the reactor. An AlN nucleation layer was deposited by flowing TMAl and NH_3 at 1070 ℃. The TMAl flowrate and chamber pressure were varied to observe the effects on the deposition. A pre-flow of TMAl was carried out for 12 s at 1070 ℃, prior to introducing NH_3, to avoid nitridation of the silicon.

5.2.1 Effects of pressure

Figure 5-1 shows the growth rates of AlN as a function of reactor pressure (averaged over a duration of 30 min), on both nanostructured silicon and flat silicon. A TMAl flow rate of 51.9 μmol/min was used for Figure 5-1 whereas the TMAl flow rate was reduced to 25.9 μmol/min in Figure 5-2. The lines are the best fitted graphs of Chen et al.'s equation for parasitic reactions [152], which will be explained later.

From Figure 5-1, it can be seen that the growth rate decreases with increasing chamber pressure, i.e. growth efficiency decreases as chamber pressure increases. Neither reaction limited nor mass transport limited regimes can explain this phenomenon. The reason behind this decreasing growth efficiency with increasing chamber pressure is parasitic reactions or gas phase depletion [152].

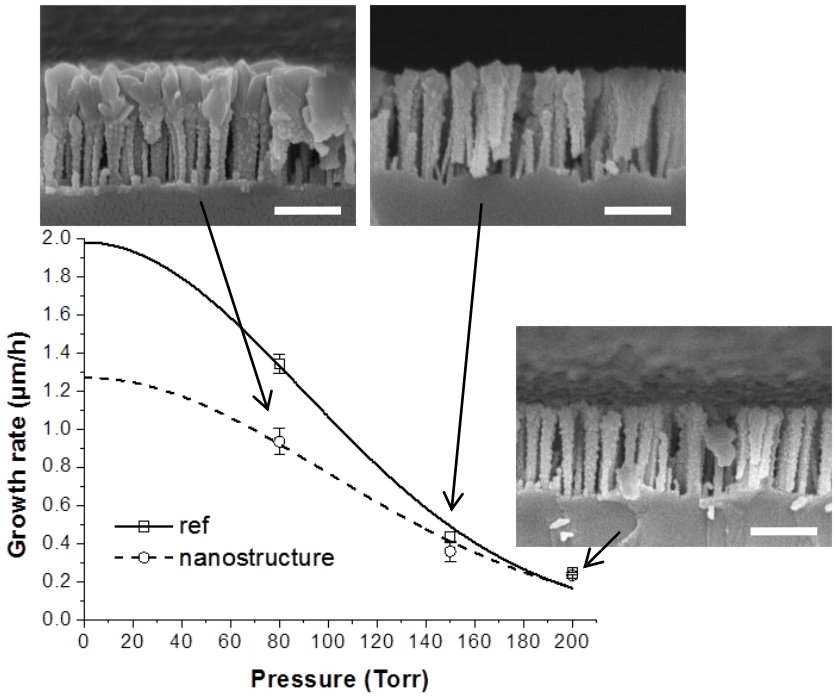

Figure 5-1. Graph of growth rates of deposited AlN versus reactor pressure. Deposition duration is 30 min. TMAl flow rate is 51.9 μmol/min. The growth rates of AlN deposited on flat silicon (labeled as 'ref') are presented together with growth rates of AlN deposited on silicon nanostructures (labeled as 'nanostructure'). The AlN growth rates on nanostructures were obtained by measuring AlN thicknesses from the tip of the silicon nanostructures. The line is the best fitted graphs of Chen et al.'s equation (see Equation (5-6)) for parasitic reactions [152]. The insets are the cross-sectional SEM images of AlN deposited on nanostructures, with varying pressures. The scale bars are 500 nm.

Parasitic reactions are homogeneous reactions which consume the gaseous precursors before they can be used for the heterogeneous deposition. According to several references [152, 153], the parasitic reaction of TMAl and NH_3 is a second order

bimolecular reaction. These homogeneous reactions are governed by the following equations [211],

$$\text{Parasitic Reaction Rate} \propto [\text{TMAl}] \times [\text{NH}_3] \times e^{\frac{-E_a}{kT_{\text{gas}}}}, \text{ or} \tag{5-1}$$

$$\text{Parasitic Reaction Rate} \propto \frac{P_{\text{TMAl}} P_{\text{NH}_3}}{\left(kT_{\text{gas}}\right)^2} \times e^{\frac{-E_a}{kT_{\text{gas}}}} \tag{5-2}$$

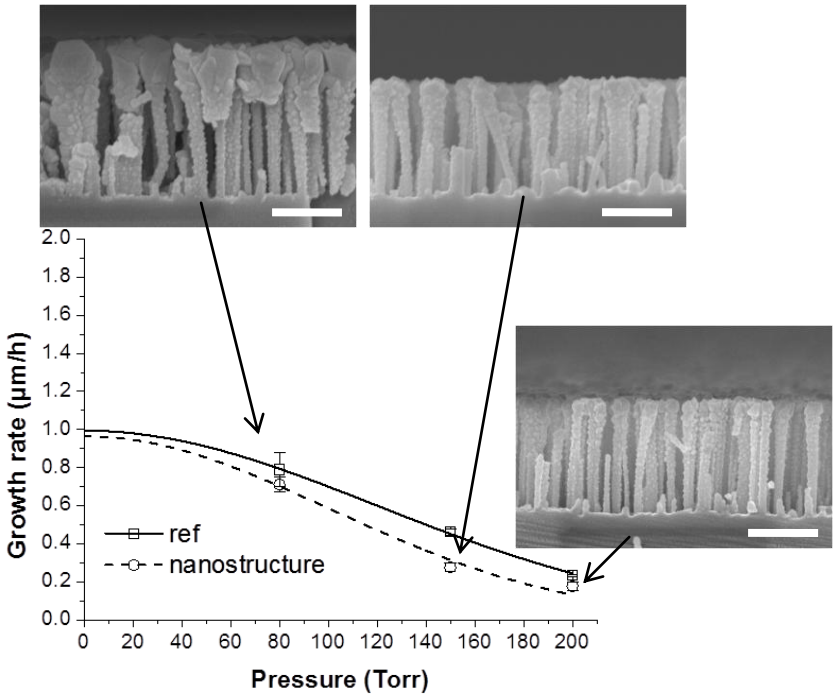

Figure 5-2. Graph of growth rates of deposited AlN versus reactor pressure. Deposition duration is 30 min. TMAl flow rate is 25.9 µmol/min. The growth rates of AlN deposited on flat silicon (labeled as 'ref') are presented together with growth rates of AlN deposited on silicon nanostructures (labeled as 'nanostructure'). The AlN growth rates on nanostructures were obtained by measuring AlN thicknesses from the tip of the silicon nanostructures. The line is the best fitted graphs of Chen et al.'s equation (see Equation (5-6)) for parasitic reactions [152]. The insets are cross-sectional SEM images of AlN deposited on nanostructures, with varying pressures. The scale bars are 500 nm.

where T_{gas} is the gas temperature and E_a is the activation energy. Assuming no change in gas temperature:

$$\Rightarrow \text{Parasitic Reaction Rate} = \text{A} \times [\text{TMAl}] \times [\text{NH}_3], \tag{5-3}$$

where A is a constant. From this, we can calculate the concentration of TMAl when the flow reaches the substrate, then derive the growth rate dependence on reactor pressure (similar to Chen et al.'s derivation [152]). For simplicity, the concentration of ammonia is assumed to be constant (this is reasonable because the growth is operated at high V/III ratio, where even with full depletion of TMAl, the NH_3 concentration will decrease by less than 1%). Solving the parasitic reaction rate equation, we get the concentration of TMAl reaching the substrate to be

$$[\mathrm{TMAl}] = [\mathrm{TMAl}]_0 \times e^{-B[\mathrm{NH_3}]t} \tag{5-4}$$

where $[\mathrm{TMAl}]_0$ is the concentration of TMAl when it enters the reactor, t is the time it takes for the reactants to reach the substrate, and B is a constant. Since both the concentration of a gaseous species and the time for reactant gases to travel is directly proportional to the pressure, we can rewrite Equation (5-4) as:

$$[\mathrm{TMAl}] = [\mathrm{TMAl}]_0 \times \exp(-C\mathrm{P}^2) \tag{5-5}$$

where C is a constant. As the growth is operating in mass transport limited regime, the growth rate is directly proportional to the group III precursor concentration. Translating this relationship to growth rate, we obtain

$$\text{Growth Rate of AlN} = \dot{\mathrm{R}}_0 \times \exp\left(-\left(\frac{\mathrm{P}}{\mathrm{P}_0}\right)^2\right) \tag{5-6}$$

where $\dot{\mathrm{R}}_0$ is the growth rate of AlN if the parasitic reaction is completely inhibited and P_0 is the reactor pressure where parasitic reactions become significant. From this equation, it is obvious that the growth rate is affected by pressure and is very much dependent on the constant P_0; the lower the value of P_0, the more sensitive the growth rate will be to a change in pressure. According to Chen et al. [152], they found that the constant P_0 is about 100 times higher for TMGa than for TMAl. Note that this implies that if a certain pressure caused a drop in GaN growth rate to 95% of its

maximum due to parasitic reaction, that same pressure would have caused the AlN growth rate to drop to less than 1%.

The growth rates of the samples were fitted to Equation (5-6) and listed out in Table 5-1, with the best fit parameters. It can be seen that the P_0 for all samples are around the same value (about 150 Torr). This suggests that the reduction in TMAl flow rate does not reduce the effect of parasitic reactions. An interesting observation is that at higher TMAl flow rate (51.9 μmol/min), the AlN growth rate on nanostructures drops to a larger extent (when compared to on flat silicon) than at lower a TMAl flow rate (25.9 μmol/min).

Table 5-1. Equations relating growth rate ($\dot{R}$) and reactor pressure (P) with best fitted parameters (according to Equation (5-6)) for nanostructured and flat silicon, with different TMAl flow rates. The units for growth rates and reactor pressures are μm/h and Torr, respectively.

TMAl flow rate (μmol/min)	**Growth rate (from Equation (5-6)) with the best fit parameters**	
	Nanostructured	**Reference (Flat)**
51.9	$1.3 \pm 0.2 \exp\left[-\left(\frac{P}{140 \pm 20}\right)^2\right]$	$2.0 \pm 0.2 \exp\left[-\left(\frac{P}{130 \pm 10}\right)^2\right]$
25.9	$1.0 \pm 0.1 \exp\left[-\left(\frac{P}{140 \pm 20}\right)^2\right]$	$0.99 \pm 0.02 \exp\left[-\left(\frac{P}{169 \pm 4}\right)^2\right]$

Metalorganics can easily form adducts with ammonia, which is the reason why the reactants are kept separated until they are introduced into the reaction chamber [152]. As the parasitic reaction is severe between TMAl and ammonia [150, 152, 153], it is important to keep the pressure low to reduce parasitic reaction in AlN growth.

From both Figure 5-1 and Figure 5-2, the growth rates of AlN on nanostructures are observed to be always lower than the growth rates of AlN on flat silicon. This is because the presence of nanostructures increased the surface area available for deposition to occur. This resulted in reduction in AlN deposition on the tip of the nanostructures, as precursors are consumed by deposition on the sidewalls. Another

observation is that the difference in AlN growth rates between a nanostructured surface and a flat surface becomes larger (smaller) when growth rates are higher (lower). An explanation for this phenomenon is suggested. At lower growth rates, the reactant (TMAl) concentration reaching the surface is low, so that there is lower driving force to growth. The lower driving force encourages growth to occur more readily at sites which are more energetically favorable (i.e. on the Si(111) surface of nanostructures' tips) than other sites (i.e. on nanostructures' sidewalls). The increased preference to deposit on the nanostructures' tips reduced the reactant depletion effects from the sidewalls.

5.2.2 Effects of growth rate on AlN nucleation

A few different AlN films were deposited at different growth rates on the nanostructures to observe how that would affect the deposited AlN. In order to observe the AlN-coated silicon nanostructures, the nanostructures were scratched off for TEM analysis. From TEM images, it was found that growth rates affect the quality of the grown AlN. Only growth runs with slow AlN growth rates would produce a high quality single crystal AlN on the tips of the nanostructure (see Figure 5-3c).

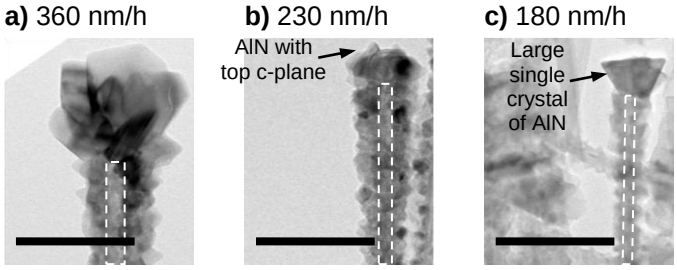

Figure 5-3. TEM images of AlN grown on silicon nanostructures with growth rates of (a) 360 nm/h, (b) 230 nm/h and (c) 180 nm/h. The dotted line serves to outline the position of the buried silicon nanostructure. The scale bars are 200 nm.

We observe that the AlN crystals on the sidewalls (see Figure 5-3) are polycrystalline and have no specific orientation. The crystals are about 20 to 50 nm in size. Polycrystallinity arose from the lack of crystallographic similarities between silicon and the wurtzite structure AlN. However, aligned AlN crystals could be still grown on the tip of the nanostructures. This is because the tips of the nanostructures are hexagonally packed Si(111) planes. Note that the c-planes of AlN (and all III-nitrides) are also hexagonally packed. It is well-known that III-nitride materials can be grown aligned to the silicon crystal structure, when grown on the Si(111) plane [70, 76, 79]. The epitaxial relationship between AlN (and GaN) and silicon is that AlN c-plane is parallel to Si(111) plane, and AlN($1\bar{1}00$) plane is parallel to Si($11\bar{2}$) plane (see Figure 5-4).

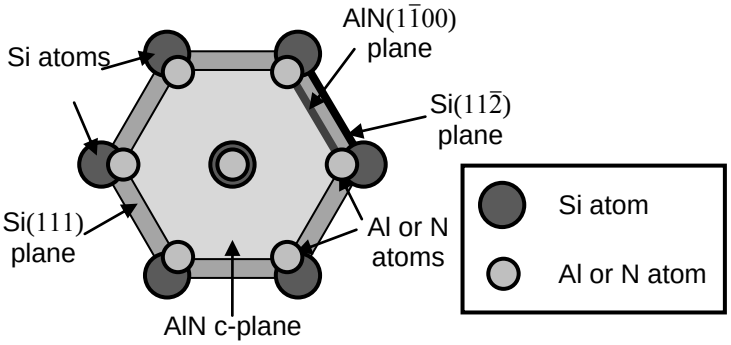

Figure 5-4. Atomic arrangement the epitaxial growth relationship of silicon and AlN, where Si(111) plane (shaded light orange) and AlN c-plane (shaded light blue) are parallel. The Si($11\bar{2}$) plane (black line) parallel to the AlN($1\bar{1}00$) plane (dark grey line). Note that both planes appeared as lines as both are perpendicular to the Si(111) plane and AlN c-plane.

However, when the growth rate of AlN is fast (at 360 nm/h), deposited AlN on the top of the nanostructures does not form this epitaxial relationship with the silicon substrate (see Figure 5-3a). The overall appearance of AlN crystals deposited at fast growth rates on silicon nanostructures is random and very polycrystalline. When the growth rate was reduced to 230 nm/h, crystallographically aligned AlN crystals were

observed on the tips of the nanostructures. A c-plane AlN can be seen forming on the tip of the nanostructure (see Figure 5-3b), but crystals of other crystallographic orientation also formed at the tip. It was only at a slow growth rate of 180 nm/h that a single large AlN crystal can be observed on the tip of a nanostructure (see Figure 5-3c). A magnified TEM image, together with SADP, confirmed that epitaxial relationship is observed between the deposited AlN and silicon nanostructure (see Figure 5-5).

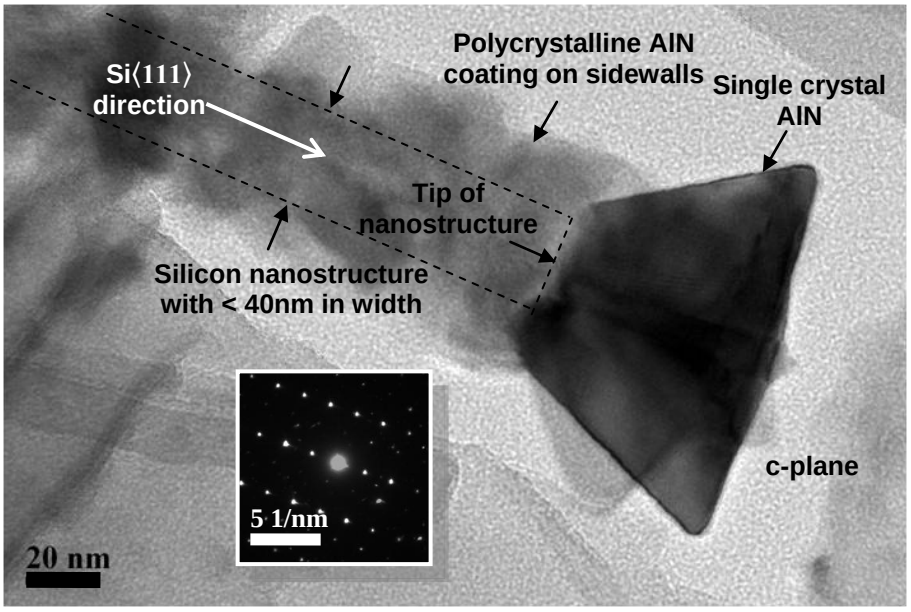

Figure 5-5. TEM image of a silicon nanostructure with a single crystal AlN grown on its tip, which was scratched off the substrate. The AlN crystal has an inverse- pyramid shape. Such single crystal of AlN was only observed on nanostructures with width less than 40 nm and where AlN was grown at a slow rate of 180 nm/h. Inset shows the SADP of the AlN crystal with clear diffraction spots (view from $[2\bar{1}\bar{1}0]$ zone axis), indicating that it is a single crystal. The diffraction pattern for the AlN crystal is enhanced visually by darkening other spots by image processing. Other scattered spots originated from the polycrystalline AlN on the sidewalls of the nanostructure.

Slower growth rate tends to produce higher quality crystals [10], and this was exemplified in our AlN deposition on nanostructures. Large AlN single crystals (more than 100 nm) were found on the tips of several nanostructures observed in TEM, which AlN was deposited at a slow rate of 180 nm/h (see Figure 5-5). The

large crystals are aligned crystallographically with the silicon substrate, according to the epitaxial relationship described in Figure 5-4. The large AlN crystals are more than 100 nm in size, with some more than 200 nm. These are much larger than the AlN crystallites grown on flat silicon, which are usually about 50 nm in size. However, having slow growth rates is not the only pre-requisite of obtaining such large single crystals of AlN. Such large AlN crystals are only found on nanostructures which are 40 nm or smaller in size.

The large AlN crystals were found to grow in an inverse-pyramid shape (see Figure 5-5). This is in contrast with GaN crystals because GaN crystals are grown revealing their (0001) and $(1\bar{1}01)$ facets [111, 117] (in a positive pyramid shape) whereas the AlN crystals are grown revealing (0001) and $(1\bar{1}0\bar{1})$ facets. Such a feature was also observed in AlGaN crystals [212].

5.2.3 Non-conformality of AlN deposition

It was found that all nanostructures exhibited variations in AlN growth rates along their sidewalls. AlN coating was thinner at the bottom of the nanostructures; in other words, non-conformal AlN deposition. This occurs because of depletion of the precursor, TMAl in this case, down the nanostructures' trenches.

The deposition on sidewalls decreases with depth into the nanostructures, forming conical shapes (see Figure 5-6). This is because the high aspect ratio of the nanostructures (more than 10) together with the nano-sized trenches between the nanostructures (less than 100 nm) prevented convective transport of reactants to the sidewalls. The prevailing transport mechanism of reactants to the sidewalls was by free molecular flow. As reactants transport down the trenches through free molecular flow, they become depleted due to sidewall deposition. Free molecular flow happens when the mean free path of molecules (mean free path at 200 Torr is estimated to be 592 nm at 1000 ℃) is larger than the lateral dimension of the trench (< 100 nm).

The mean free path, l, can be estimated by:

$$l = \frac{1}{\sqrt{2}\pi a^2 N} \tag{5-7}$$

where a is the molecules' diameter (≈ 5Å) and N is the molecule concentration. N can be estimated by:

$$N = \frac{pN_A}{RT} \tag{5-8}$$

$$N_{200\text{Torr}} = \frac{(200 \times 133.3)(6.02 \times 10^{23})}{8.31 \times 1273} = 1.52 \times 10^{24} \text{ molecules/m}^3$$

assuming ideal gas and T = 1273 K. Similarly, we get:

$$N_{80\text{Torr}} = \frac{(80 \times 133.3)(6.02 \times 10^{23})}{8.31 \times 1273} = 6.07 \times 10^{23} \text{ molecules/m}^3$$

From Equation (5-7), we get:

$$l_{200\text{Torr}} = \frac{1}{\sqrt{2}\pi(5 \times 10^{-10})^2(1.52 \times 10^{24})} = 592 \text{ nm}$$

$$l_{80\text{Torr}} = \frac{1}{\sqrt{2}\pi(5 \times 10^{-10})^2(6.07 \times 10^{23})} = 1.483 \text{ μm}$$

As both the heights of the nanostructures and the gaps between the nanostructures are smaller than, or about the same order as, the free mean path of molecules, molecular diffusion is the prevailing transport mechanism for the reactants.

In addition, the poor surface diffusion length of Al [213, 214] also discourages AlN from attaining a conformal coating. This non-conformal deposition causes "necking" of the trenches [211], which makes it harder for reactants to reach the bottom of the trenches.

In fact, this non-conformality is advantageous in our case. Higher deposition rate on the nanostructures' tips, than at the trenches' bottom, encourages deposited materials to coalesce to form a film while leaving air gaps between the nanostructures. This causes subsequent deposited nitride to bridge across gaps between nanostructures,

forming a film supported by standing nanostructures, with air voids in between. Such a structure can relieve thermal stresses that arise from the coefficient of thermal expansion mismatch between the substrate and the film [52, 115].

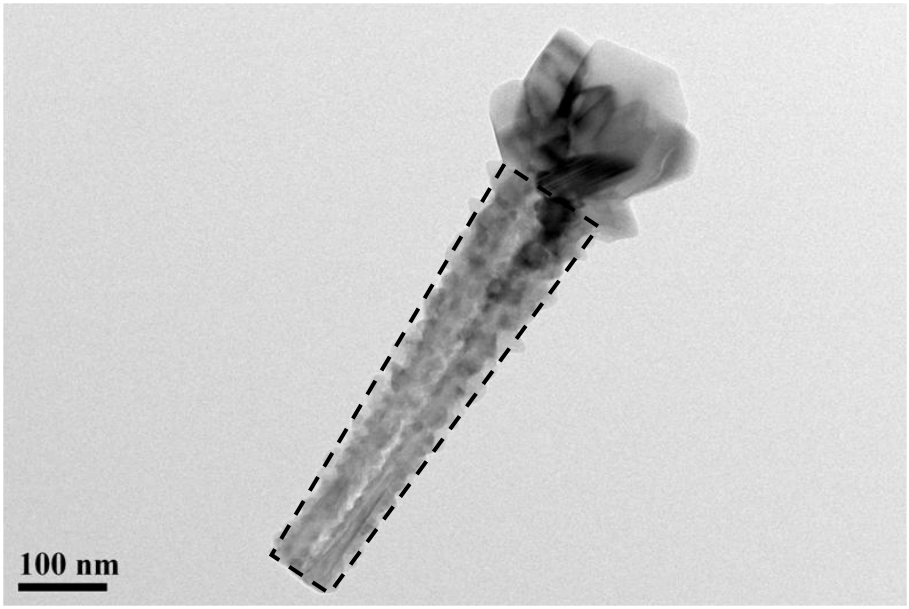

Figure 5-6. TEM image of a typical silicon nanostructure coated with AlN. The AlN layer forms an inverse-conical shape (outlined by the broken line), due to non-conformal deposition.

5.2.4 Summary

It was found that the growth rate has an inverse relationship with reactor pressure due to significant parasitic reactions. The relationship can be described by Equation (5-6). Slow growth rate of 180 nm/h was shown to produce high quality AlN crystals, in which a single crystal AlN can form on the tips of silicon nanostructures. The nanostructured surface results in non-conformal coating of AlN. This is advantageous to our aim of achieving a compliant substrate, as voids between the nanostructures can relieve strains in the subsequently deposited continuous film.

5.3 AlN nucleation layer

To grow GaN on flat silicon using our system, about 200 nm of HT-AlN is required to be deposited as nucleation layer. However, for nanostructured silicon, it was found that the AlN nucleation layer cannot be at such thickness, or proper GaN film coalescence cannot occur subsequently (see Figure 5-7).

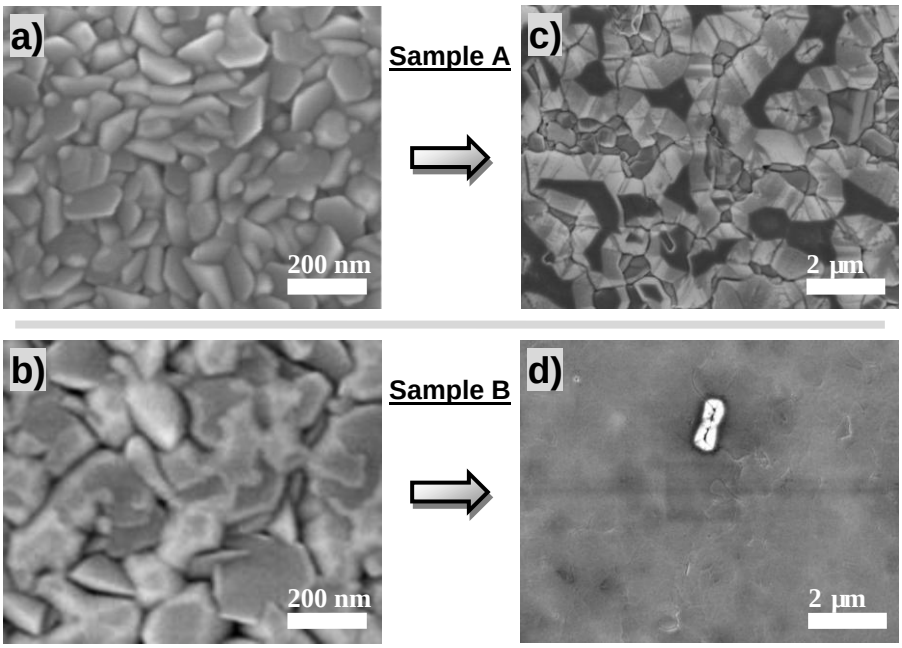

Figure 5-7. Plan view SEM images of (a) 200 nm AlN nucleation layer (sample A) and (b) 200 nm AlGaN on 60 nm AlN nucleation layer (sample B). After 1 µm of GaN was grown on sample A and B, it was found that a GaN film did not coalesce on sample A (c); while GaN film coalesced on sample B (d).

The reason for the difference is because of the good coverage of AlN. AlN deposition provides good coverage, even for nanostructured silicon, hence an appreciable amount of AlN is deposited on the sidewalls of the silicon nanostructures. As AlN deposited on the sidewalls is polycrystalline (see Figure 5-5), any AlN growth extended from the sidewalls will be polycrystalline as well. If AlN is deposited thick enough, this polycrystalline AlN on the sidewalls will compete with the single crystalline AlN on the tips for growth, and for overall dominance in the texture. As

polycrystalline AlN results in misoriented GaN, coalescence in the subsequent GaN layer is difficult (see Figure 5-7c).

To promote coalescence, thinner AlN nucleation layer (60 nm) was grown, with an additional 200 nm AlGaN layer deposited subsequently to avoid meltback etching. The texture is dominantly c-plane oriented with the thinner AlN nucleation layer (see Figure 5-7b). Coalescence then occurred with the subsequently deposited GaN layer, resulting in a flat and continuous film (see Figure 5-7d).

5.4 GaN morphologies with varied heights of nanostructures

GaN growth was performed on substrates of various nanostructure heights to examine the effects of nanostructures height on the GaN morphologies. First, a 60 nm AlN nucleation layer was grown, followed by a 190 nm thick $Al_{0.6}Ga_{0.4}N$, both at 1070 ℃. Then a 280 nm GaN layer was grown, followed by a LT-AlN interlayer grown at 750 ℃. Finally, another 280 nm GaN layer was grown. All GaN layers were grown at 1000 ℃.

Three different heights of the nanostructures were used in this growth: 100 nm (short), 300 nm (medium) and 700 nm (long). It can be seen that GaN on the short nanostructures had fully coalesced to form a continuous film. GaN on the medium height nanostructures had not yet fully coalesced. For the long nanostructures, GaN only managed to form isolated islands of various sizes, ranging from 1 to 7 μm (see Figure 5-8c). From the cross-sectional SEM images, it can be seen that that the nanostructures were almost completely buried by III-nitride in both the short and medium nanostructures (see Figure 5-8d and e); whereas III-nitride only grew partially into the nanostructures for the long nanostructures (see Figure 5-8f). Looking more closely, it can be seen that the GaN crystals grown on long

nanostructures extended to about 2 μm in height, which is much more than the thickness of the GaN films on short and medium nanostructures. This shows that the GaN crystals on long nanostructures were growing more vertically rather than laterally. Hence, the isolated GaN crystals were unlikely to coalesce with longer growth duration.

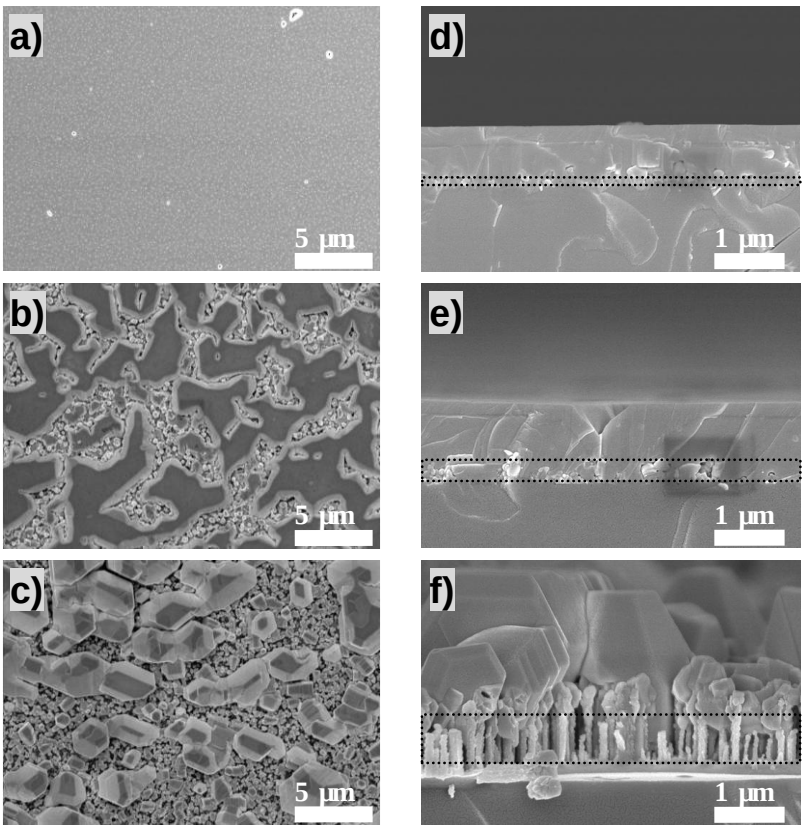

Figure 5-8. Plan view (left: (a), (b) and (c)) and cross-sectional view (right: (d), (e) and (f)) SEM images of GaN grown on substrates with various nanostructure heights. The heights used were about 100 nm ((a) and (d)), 300 nm ((b) and (e)) and 700 nm ((c) and (f)), and they are referred to as short, medium and long nanostructures, respectively. The broken black line serves as a visual aid to the position of the nanostructures.

As it is difficult to attain continuous GaN film on medium and long nanostructures, we will investigate on how having short nanostructures (about 100 nm tall) affects the GaN film.

5.5 Influence of growth structures on GaN film

Buffer layers are often required for mismatched material systems [215-217], as they serve to improve the quality of the desired film [218]. There exist several techniques and growth structures which could be implemented on GaN growth on silicon (as explained in Chapter 2) to reduce dislocations and defects, such as in-situ silicon nitride masking [70], superlattice [75, 100] and multi-step-graded AlGaN buffer layers [73].

We had implemented the three above-mentioned techniques on the nanostructured substrates. All samples have about 100 nm tall nanostructures, etched using one-step MACE with optimized conditions described in Chapter 4. From now on, we will refer the different samples according to Table 5-2 for easy referencing.

Table 5-2. Sample naming with respect to the growth techniques applied on them.

Name	**Techniques applied to Si etched using one-step MACE**
Sample I	In-situ silicon nitride masking
Sample II	Superlattice
Sample III	Multi-step-graded AlGaN buffer layers

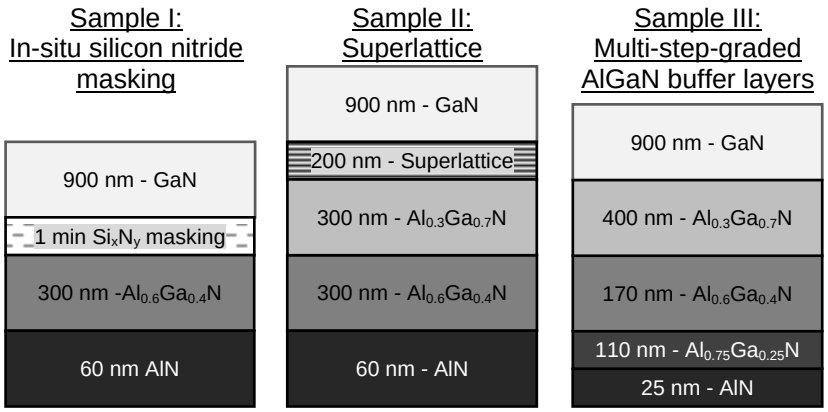

Figure 5-9. Three different growth structures were grown on nanostructured silicon substrates for comparison. Note that the structures are not drawn to scale.

5.5.1 In-situ silicon nitride masking

The structure of our Sample I is schematically presented in Figure 5-9. A 60 nm thick AlN nucleation layer was deposited, followed by a 300 nm $Al_{0.6}Ga_{0.4}N$ layer. Both layers were deposited at 1070 ℃. The temperature was then reduced to 1000 ℃. Silicon nitride masking was then deposited for 1 min, before a final 900 nm of GaN was grown.

A 60 nm of AlN nucleation layer was chosen due to reasons given earlier in this Chapter. A high Al content AlGaN ($Al_{0.6}Ga_{0.4}N$) was deposited to avoid meltback etching, as the 60 nm AlN might not be sufficient in protecting the silicon substrate. 1 min of silicon nitride deposition formed a discontinuous mask on the AlGaN layer. A longer deposition (4 min) was attempted, but this resulted in misaligned polycrystalline GaN (see Figure 5-10). This is likely to be because 4 min of silicon nitride deposition completely (or almost completely) masked the AlGaN beneath, preventing any epitaxial relationship to be transferred to the GaN grown on it.

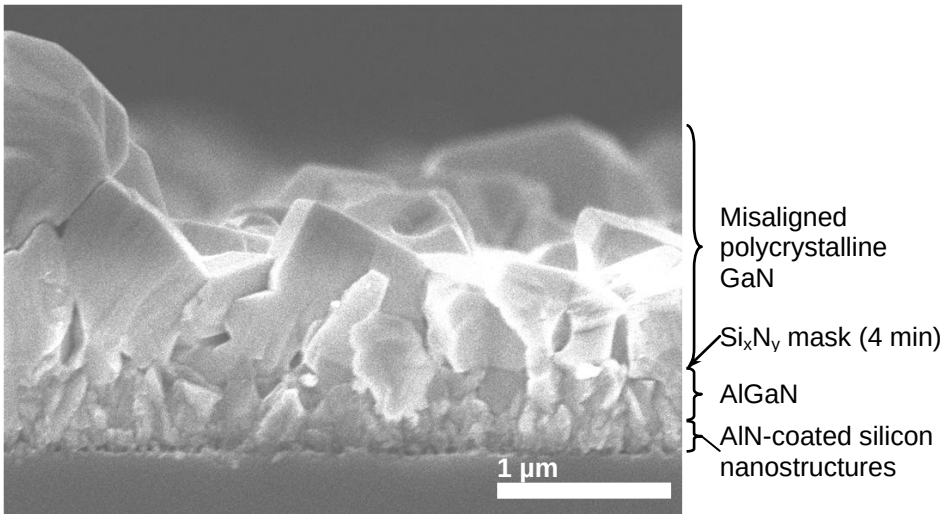

Figure 5-10. Cross-sectional SEM image of GaN grown on 4-minute silicon nitride mask. The growth structure is given on the right of the image. The thick silicon nitride mask prevented subsequent GaN from forming an epitaxial relationship with the AlGaN beneath.

5.5.2 Superlattice

The structure of our Sample II is schematically presented in Figure 5-9. A 60 nm of AlN nucleation layer was chosen due to reasons given earlier in this Chapter. A 300 nm high Al content AlGaN ($Al_{0.6}Ga_{0.4}N$) was deposited to avoid meltback etching, as the 60 nm AlN might not be sufficient in protecting the silicon substrate. Another 300 nm AlGaN ($Al_{0.3}Ga_{0.7}N$) buffer layer was included before introducing the superlattice as we had difficulty in forming a flat smooth surface if this layer was not included. This is probably due to the uneven surface after the high Al content AlGaN layer. The above-mentioned layers were deposited at 1070 ℃. A superlattice consisting of 20 periods of 6 nm GaN and 4 nm AlN were then deposited at 1040 ℃. The temperature was then reduced to 1000 ℃ to grow a final 900 nm of GaN.

5.5.3 Stepped AlGaN buffer layers

The structure of our Sample III is schematically presented in Figure 5-9. A 25 nm thick AlN nucleation layer was deposited, followed by 3 AlGaN layers of different compositional content. The deposition was done in this order: 110 nm $Al_{0.75}Ga_{0.25}N$ layer, 170 nm $Al_{0.6}Ga_{0.4}N$ layer and 400 nm $Al_{0.3}Ga_{0.7}N$ layer. The layers were deposited at 1070 ℃. The temperature was then reduced to 1000 ℃ to grow a final 900 nm of GaN.

For this growth structure, we proposed to grow a thinner AlN and high Al content AlGaN so as to achieve flat continuous layer as soon as possible. As higher Ga content AlGaN layer would enhance lateral growth [212], this growth structure aimed to reduce the thickness of AlN and high Al content AlGaN as much as possible. This is deemed to be important because the presence of nanostructures makes it difficult for film to coalesce [219], resulting in rough and poor quality film. Hence, a thinner 25 nm of AlN was deposited, followed by a 110 nm thick high Al content AlGaN ($Al_{0.75}Ga_{0.25}N$). The relatively thick $Al_{0.75}Ga_{0.25}N$ was deposited to avoid meltback

etching, as the 25 nm AlN might not be sufficient in protecting the silicon substrate. Subsequently, 2 layers of AlGaN of different composition (170 nm of $Al_{0.6}Ga_{0.4}N$ and 400 nm of $Al_{0.3}Ga_{0.7}N$) were included before GaN growth.

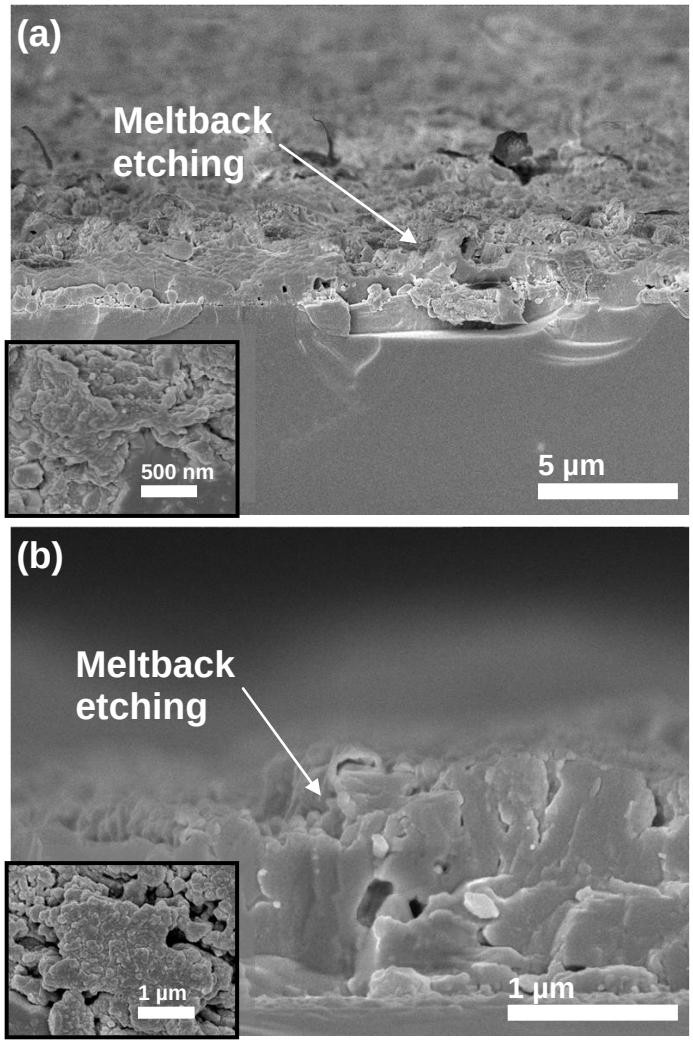

Figure 5-11. Cross sectional SEM images showing meltback etching occurring on substrate with 100 nm tall nanostructures, grown with the following structures: (a) 25 nm AlN/30 nm $Al_{0.75}Ga_{0.25}N$/60 nm $Al_{0.6}Ga_{0.4}N$/200 nm $Al_{0.3}Ga_{0.7}N$/900 nm GaN and (b) 25 nm AlN/35 nm $Al_{0.75}Ga_{0.25}N$/110 nm $Al_{0.6}Ga_{0.4}N$/250 nm $Al_{0.3}Ga_{0.7}N$/900 nm GaN. The inset in each cross sectional SEM image shows the corresponding plan view SEM images.

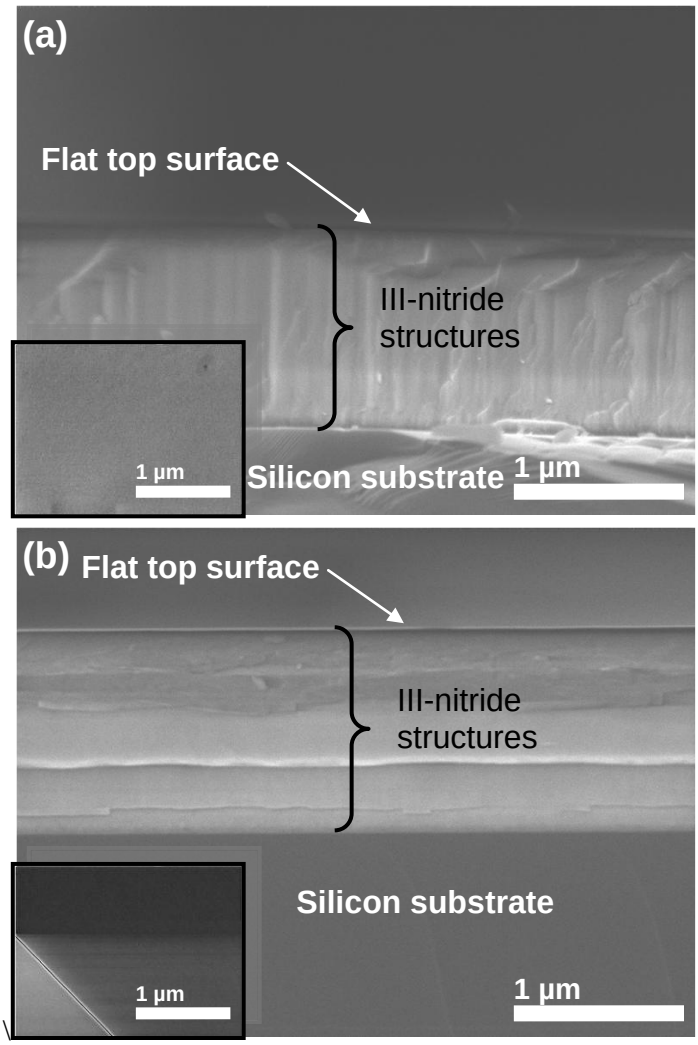

Figure 5-12. Cross sectional SEM images showing the smooth, flat GaN grown on flat silicon. The structures grown are exactly the same as those in Figure 5-11, where (a) has 25 nm AlN/30 nm $Al_{0.75}Ga_{0.25}N$/60 nm $Al_{0.6}Ga_{0.4}N$/200 nm $Al_{0.3}Ga_{0.7}N$/900 nm GaN and (b) has 25 nm AlN/35 nm $Al_{0.75}Ga_{0.25}N$/110 nm $Al_{0.6}Ga_{0.4}N$/250 nm $Al_{0.3}Ga_{0.7}N$/900 nm GaN. The inset in each cross sectional SEM image shows the corresponding plan view SEM images.

Initially, even thinner AlGaN layers were attempted on top the 25 nm AlN nucleation layer, but poor results followed. Figure 5-11 shows the results of GaN deposition on nanostructured silicon with thinner AlGaN layers (growth structure stated in description). Such thin AlGaN layers resulted in a very rough surface due to meltback etching. However, it is important to note that if the same growth structures were implemented on a flat silicon substrate, meltback etching did not occur (see Figure 5-12). Therefore, the thicknesses of thermally resistant layers (AlN and AlGaN layers)

are critical to grow GaN film on top of nanostructured silicon successfully. This is because the presence of nanostructures makes it difficult to form complete coverage of thermally resistant layers over silicon. Hence, the growth structure of Sample III (see Figure 5-9) contained the thinnest high Al content AlGaN layers implemented, which can successfully grow GaN film on nanostructured silicon with just 25 nm of AlN nucleation layer.

5.5.4 Comparison of quality

The three different samples (Sample I, II and III) were characterized using several characterization tools, such as SEM, TEM, XRD and PL.

5.5.4.1 SEM

From Figure 5-13, it can be seen that the top surfaces are relatively smooth. The reference samples (Sample I - Ref, Sample II - Ref and Sample III - Ref) refer to the simultaneous growths on a flat silicon surface. Looking more closely, it can be seen that the coalescence is not yet complete for Sample II. Grain boundaries could still be seen clearly under SEM. The faint boundaries of coalescing islands could be still observed in Sample I, whereas such boundaries could not be observed on Sample III. All reference samples have flat surfaces, with no distinguishable boundaries.

This signified the effect of having thinner layers of AlN (and high Al content AlGaN) and transition to high Ga content AlGaN in Sample III. As high Ga content AlGaN enhances the lateral growth of III-nitrides, earlier coalescence is shown to be necessary for a good surface morphology. Sample I fared better than Sample II as the thin silicon nitride covered misaligned AlGaN crystal, which later on GaN might grow on it and compete for growth with the c-plane aligned GaN.

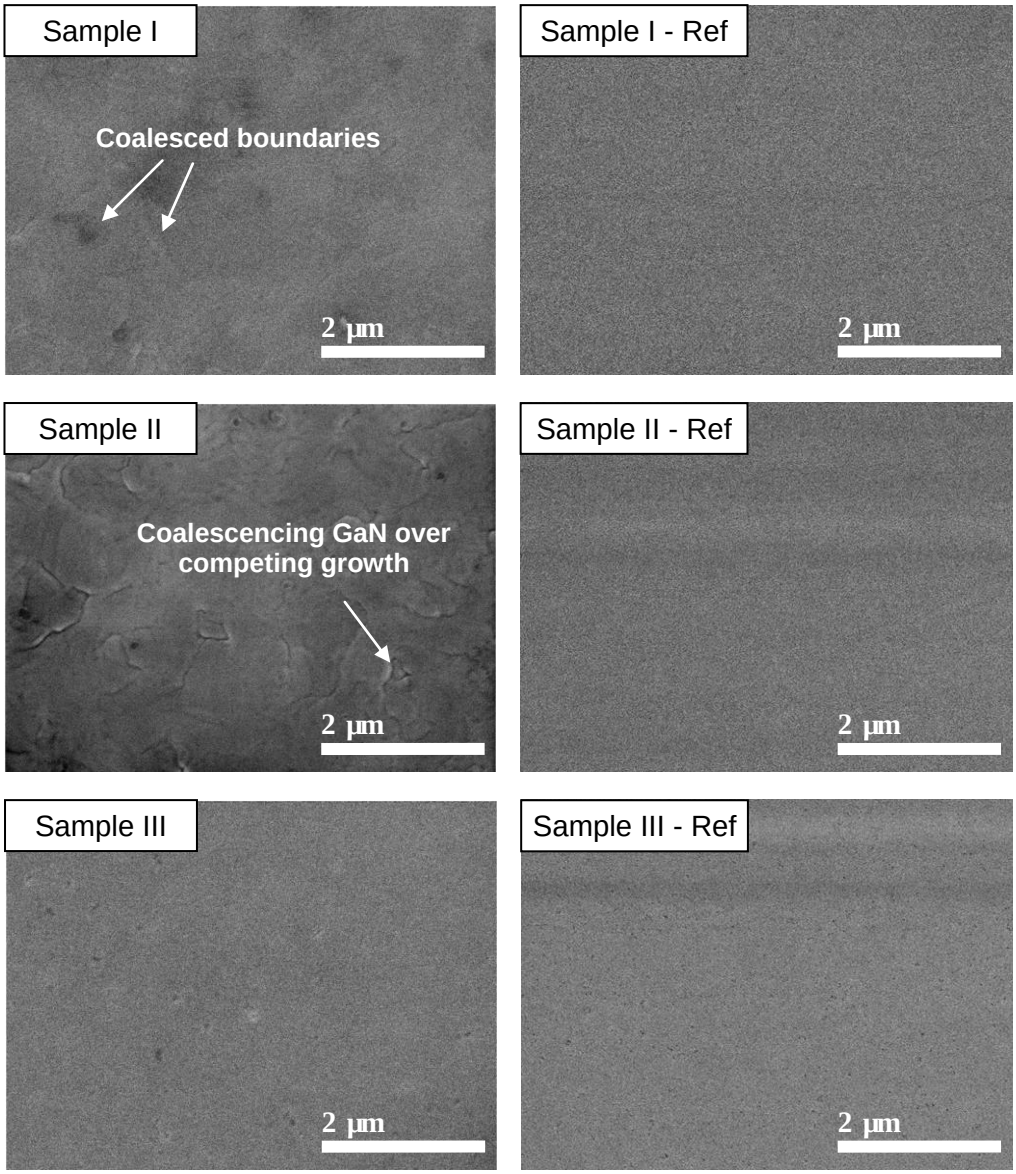

Figure 5-13. Plan view SEM images of three different growth structures grown on nanostructures: Sample I, II and III (left). Details of the growth structures are described earlier in Figure 5-9. The plan view SEM images of the corresponding reference samples (grown on flat silicon) of the growth structures are positioned on the right.

5.5.4.2 Photoluminescence

The low temperature PL spectra of the three samples are shown in Figure 5-14. The PL measurement was done at 15 K. The peaks of the PL were at 3.443, 3.451 and 3.453 eV for Sample I, II and III, respectively. The FWHMs of the peaks for the three samples were similar, at about 50 meV.

As shifting of PL spectra are associated with strains in the lattice [220], we can estimate the stresses and strains present in the three samples. Assuming there are only in-plane biaxial stresses, the stresses could be estimated by using Equation (3-15). Taking 3.474 eV as strain-free (from reference [76]), the stresses are 1.6 ± 0.3 GPa, 1.2 ± 0.3 GPa and 1.1 ± 0.3 GPa for Samples I, II and III, respectively. The biaxial strains are found to be $(3.3 \pm 0.2) \times 10^{-3}$, $(2.5 \pm 0.2) \times 10^{-3}$ and $(2.2 \pm 0.2) \times 10^{-3}$ for Samples I, II and III, respectively (from Equation (3-14)). The stresses in the GaN films on the three samples are all tensile. Note that although values in reference [76] were measured at 10 K, the band gap is shifted by less than 1 meV when temperature is increased to 15 K, according to the Varshni's equation, taking parameters from reference [162]. Therefore, it is reasonable to apply the relationship for measurements at 15 K.

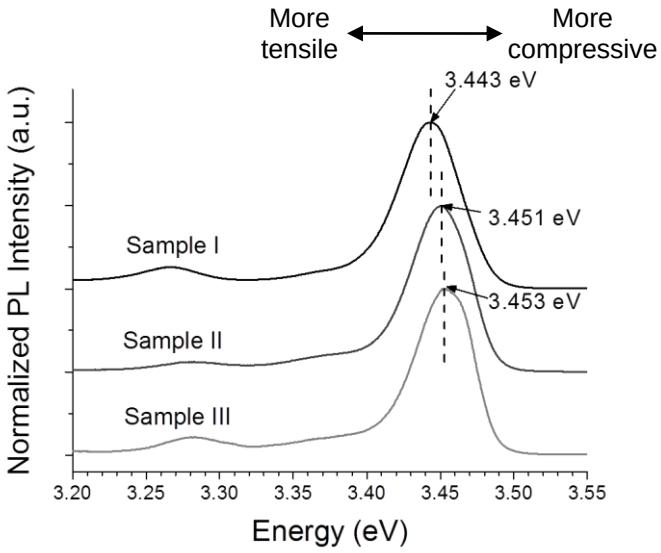

Figure 5-14. Comparison of normalized low temperature (15 K) PL of Sample I, II and III. The peaks coincide with the bound exciton lines.

The biaxial stresses and strains were also derived for reference samples (same growth structure as Sample I, II and III but grown on flat silicon) and the values are given in

Table 5-3. It can be seen that only in Sample III that a reduction in stress is observed when compared to their corresponding reference sample.

Table 5-3. Biaxial stresses and strains derived from shift in PL.

Sample	Biaxial stress (GPa)		Biaxial strain ($\times 10^{-3}$)	
	Nanostructured silicon	Reference	Nanostructured silicon	Reference
I	1.6 ±0.3	1.1 ±0.3	3.3 ±0.2	2.3 ±0.2
II	1.2 ±0.3	1.1 ±0.3	2.5 ±0.2	2.3 ±0.2
III	1.1 ±0.3	1.8 ±0.4	2.2 ±0.2	3.8 ±0.3

It should be noted that even though the measurements were done at low temperatures, the estimated biaxial stresses and strains are for the samples at room temperature. This is because given relationship has been calibrated to use low temperature PL measurements for stresses and strains estimation at room temperature [76].

5.5.4.3 XRD

Values of θ were obtained from the peak positions of GaN(0002) and GaN($10\bar{1}2$) for Samples I, II and III to determine the lattice parameters, c and a. c parameter could be calculated using Bragg's Law (note that $c = 2\times d_{0002}$); a parameter could be calculated by first obtaining $d_{10\bar{1}2}$ using Bragg's Law, and then applying following relationship:

$$a = \frac{2d_{10\bar{1}2} \times c}{\sqrt{3c^2 - 12{d_{10\bar{1}2}}^2}} \tag{5-9}$$

After obtaining the lattice parameters, the corresponding strains (ε_c and ε_a) were calculated by using c_0=5.1851 Å and a_0=3.1893 Å as strain-free parameters [4] for GaN. The strains are calculated from the following formulae:

$$\varepsilon_c = \frac{c - c_0}{c_0} \tag{5-10}$$

$$\varepsilon_a = \frac{a - a_0}{a_0} \tag{5-11}$$

Note that ε_a is the biaxial strain. The strain of a was also estimated from ε_c, using elastic constants C_{13} and C_{33}. The relationship is:

$$\varepsilon_a = -\frac{C_{33}}{2C_{13}}\varepsilon_c \tag{5-12}$$

where C_{13} was taken as 106±20 GPa and C_{33} was taken as 398±20 GPa from reference [221]. The biaxial strains for reference samples (same growth structure grown on flat silicon) are also estimated (see Table 5-4) for comparison.

Note that the error provided was large (strains were reduced to just one significant number), because of the rather wide peaks of GaN(0002) and GaN($10\bar{1}2$) in 2θ-ω scans were taken into consideration (FWHM between 0.2 °to 0.3 °). Although the step size of XRD could be as small as 0.0001°, a step size of 0.0025 ° was more than sufficient to identify the peak position. Hence, step size of 0.0025 ° was used to calculate the error, using the following equation [158, 222]:

$$\frac{\Delta d}{d} \approx \cot\theta \times \Delta\theta \tag{5-13}$$

where Δd is the error in determining the lattice spacing, and $\Delta\theta$ is the step size or error in θ (in radians). The error for determining c is estimated to be ±0.0005 Å. However, as the intensity for GaN($10\bar{1}2$) is much lower resulting in a low signal-noise-ratio (see Figure 5-15), $\Delta\theta$ is taken as 0.005 ° instead. Thus, the error for determining $d_{10\bar{1}2}$ is estimated to be ±0.0005 Å. The error given in Table 5-4 was estimated from the error estimated above and Equations (5-9), (5-10), (5-11) and (5-12).

Table 5-4. Strains ε_c and ε_a are calculated from XRD measurements and by assuming c=5.1851 Å and a=3.1893 Å as strain-free parameters [4] for GaN.

The ε_a in the last column is calculated using elastic constants C_{13} and C_{33} given by reference [221].

Sample	**ε_a calculated from c and a parameters ($\times 10^{-3}$)**		**ε_a calculated from c parameters and elastic constants ($\times 10^{-3}$)**	
	Nanostructured silicon	**Flat silicon**	**Nanostructured silicon**	**Flat silicon**
I	2.6 ± 0.9	2.1 ± 0.9	0.3 ± 0.1	0.1 ± 0.1
II	-0.2 ± 0.9	0.4 ± 0.9	-0.1 ± 0.1	0.2 ± 0.1
III	6.8 ± 0.9	1.2 ± 0.9	0.1 ± 0.1	0.1 ± 0.1

It was observed that Sample II had the most reduction in biaxial tensile strain effect. In fact, it exhibited biaxial compressive strain instead. This is most probably due to the multiple compressive layers in the superlattice of Sample II. Another observation was that the growth sequence of Sample II seemed to have a much greater strain reduction effect on nanostructured substrate than on flat silicon. This is likely due to the improper coalescence of GaN film on Sample II (see Figure 5-13 for the discontinuity). This results in a reduction of thermal strain on GaN film. Samples I and III both have tensile biaxial strain, but it is uncertain which has a higher strain (see Table 5-4).

From the XRD results, the crystal quality of the GaN could also be derived. Table 5-5 presents the screw dislocation density and edge dislocation density, estimated from the FWHMs of omega rocking curves of the GaN(0002) peak and GaN($10\bar{1}2$) peaks, respectively, based on reference [158]. It can be seen that Sample III has the lowest dislocation density, followed by Sample I and then Sample II.

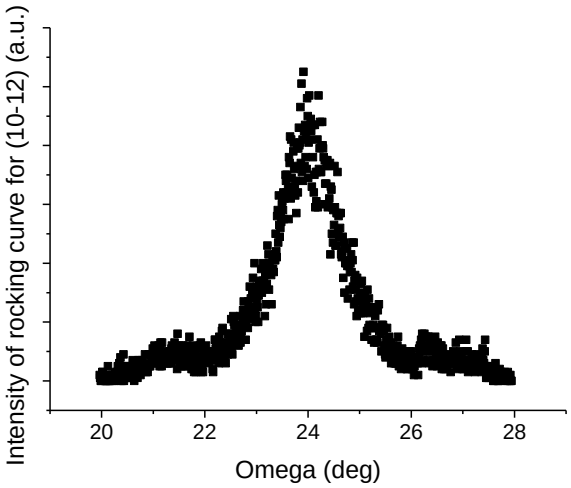

Figure 5-15. Omega rocking curve of GaN($10\bar{1}2$) peak for Sample III. It is difficult to pinpoint the exact peak position due to the low signal-noise-ratio and broad peak. Error in identifying peak position is as high as 0.01°.

Table 5-5. Estimated dislocation density from FWHMs of XRD omega rocking curves.

Sample	**Screw dislocation density**		**Edge dislocation density**	
	Nanostructured	**Reference**	**Nanostructured**	**Reference**
I	2.3×10^{10} cm^{-2}	1.0×10^{9} cm^{-2}	7.8×10^{10} cm^{-2}	1.0×10^{10} cm^{-2}
II	1.3×10^{10} cm^{-2}	5.3×10^{8} cm^{-2}	1.1×10^{11} cm^{-2}	7.2×10^{9} cm^{-2}
III	7.6×10^{9} cm^{-2}	1.1×10^{9} cm^{-2}	6.6×10^{10} cm^{-2}	1.4×10^{10} cm^{-2}

5.5.4.4 TEM

Figure 5-16 shows the cross-sectional dark-field TEM images of Samples I, II and III. Note that the dark-field images for $\boldsymbol{g}$ =[0002] reveal dislocations with screw component and $\boldsymbol{g}$=[$1\bar{1}00$] reveal dislocations with edge component. From Figure 5-16**,** the dislocations in the GaN layer of Sample I are observed to be concentrated at the boundary of a grain (see Figure 5-16A and B); while the dislocations in the GaN layer of Samples II and III are about evenly distributed (see Figure 5-16C to F). In addition, in Sample I, dislocations are also reduced in the GaN layer when compared to the layers beneath. This is due to the effect of in-situ silicon nitride masking, where

GaN grows over areas masked by silicon nitride (see Figure 5-17). With this masking, dislocations in GaN can bend laterally as the GaN layer grows laterally over the mask, and dislocations under the masked areas are prevented from extending to the top GaN layer.

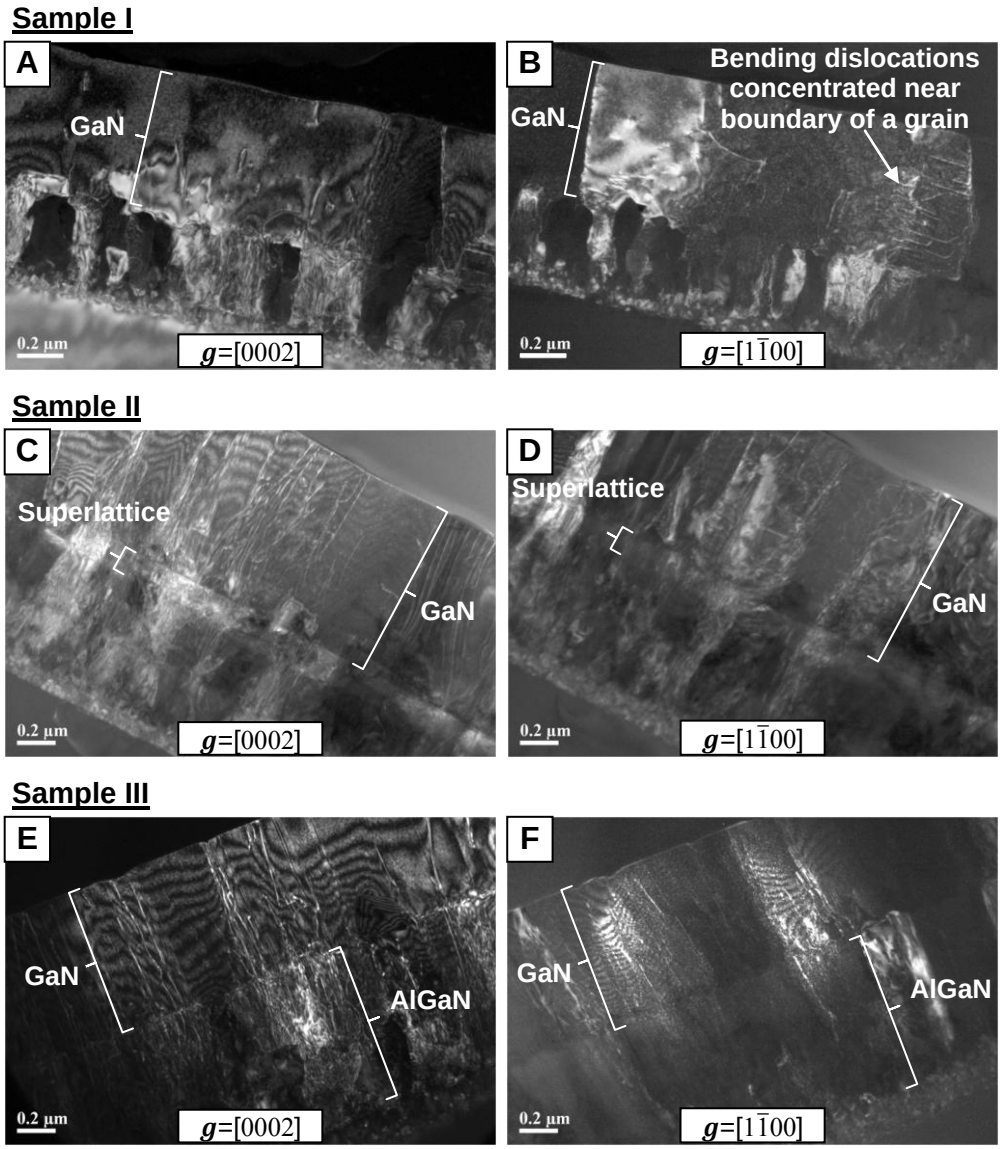

Figure 5-16. Cross-sectional dark-field TEM images of Sample I (A and B), II (C and D) and III (E and F), with $\boldsymbol{g}$=[0002] (left) and $\boldsymbol{g}$=[1$\bar{1}$00] (right).

Sample II contained superlattice structure which could help to reduce the dislocation density [223]. Figure 5-18 shows that a dislocation loop is generated by the

superlattice structure, preventing the dislocation from threading up the surface. However, not all dislocations are prevented from reaching the top layer as threading dislocations are still able to thread up to the surface.

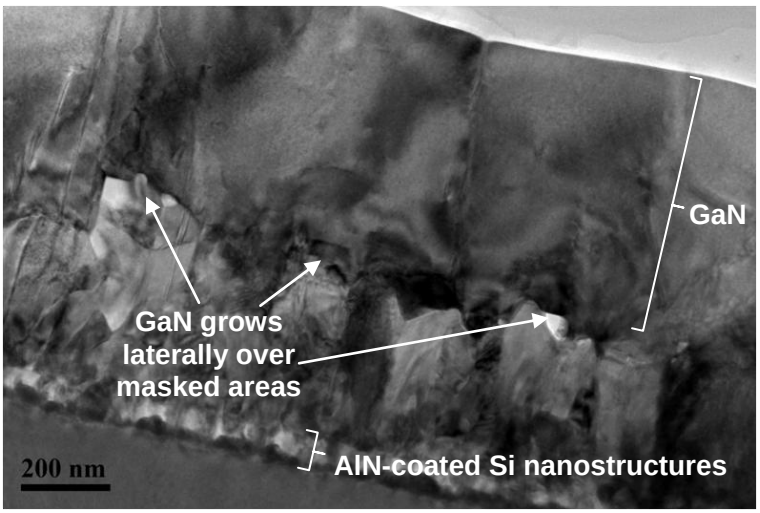

Figure 5-17. TEM image of Sample I, showing GaN crystal grew over masked regions and coalesce to form a continuous film.

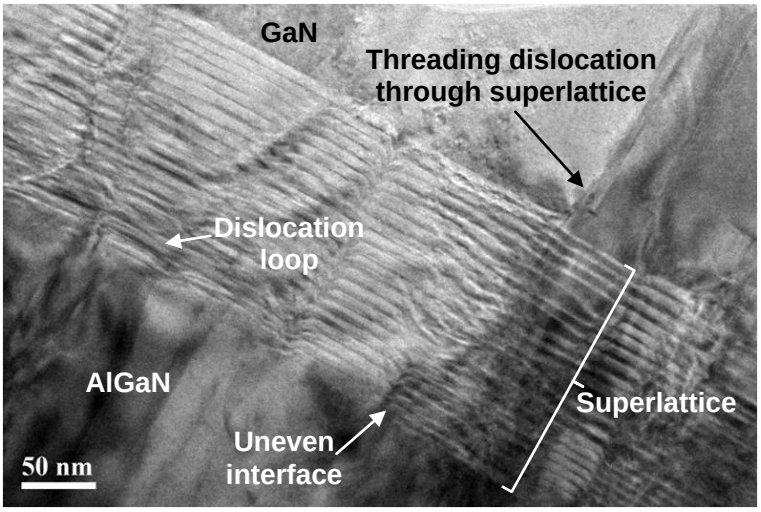

Figure 5-18. Cross-sectional TEM image of Sample II, showing the superlattice structure. A dislocation loop is observed in the superlattice and a threading dislocation is observed to pass through the superlattice structure.

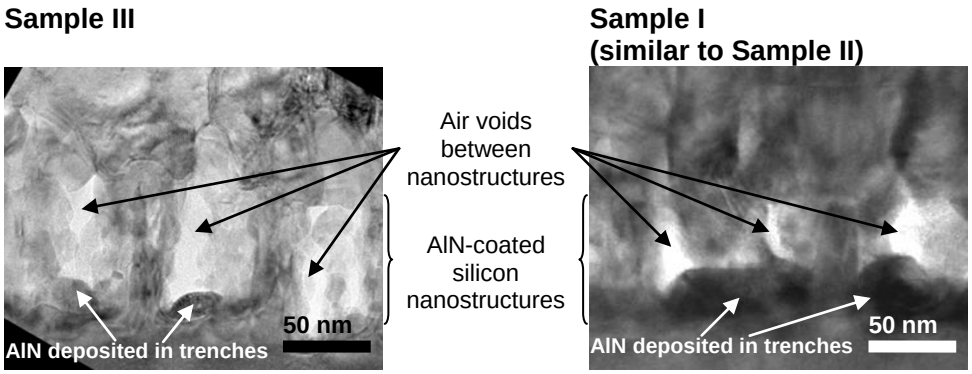

Figure 5-19. Cross-sectional TEM images of Sample III (left) and Sample I (right) of the silicon nanostructures. Due to thinner AlN deposition (about 25 nm thick) in Sample III, it has larger air voids between the nanostructures than Sample I and Sample II.

The thinner AlN nucleation layer deposited on Sample III is intended to allow lateral coalescence earlier in the growth. A side effect which came along with this thinner AlN layer is that larger air voids between the nanostructures result (see Figure 5-19). As AlGaN (and GaN) does not provide good coverage as AlN, thinner AlN would have reduced fillings of the trenches between the nanostructures. This larger air voids is believed to provide stress relaxation [52] for the residual thermal stresses.

5.5.5 Discussions

The strains estimated from PL and XRD are presented in Figure 5-20 for comparison. The strains estimated using c and a parameters are not included due to the large errors involved. The strain values derived using XRD conflicted with the values derived using PL. This is probably because of the different probe depth due to difference in absorption of the two different beams. As the absorption coefficient of the 325 nm UV laser is much higher than the X-ray (about 10^5 cm^{-1} for 325 nm UV [224] compared to 429 cm^{-1} for X-ray [158]), the PL spectra is more sensitive to the material near the surface due to a lower penetration depth [225]. Hence, the reason why compressive strain in Sample II was only detected by XRD but not PL could be due to that compressive strain is only found deep in the GaN layer. Therefore, the

generally lower strains for all samples measured by XRD (compared to as derived from PL) were probably due to stress gradient in the GaN layer.

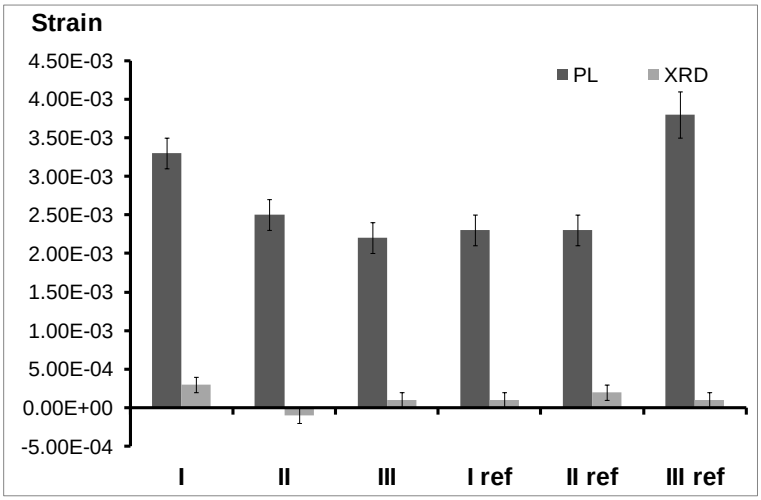

Figure 5-20. Graphical representation of the different strains estimated from various methods (by PL and XRD). Note that tensile strains are positive and compressive strains are negative.

From the strains estimated by XRD results, the reduced strains in Sample II, when compared to its reference, suggested that the growth structure of Sample II does not impede the stress reduction capability of nanostructures on the final GaN layer. Unfortunately, the PL results do not indicate a reduction in strain. This could be probably due to the presence of more dislocations in Sample II (than its reference), which allowed relaxation of the compressive strains generated by the superlattice as growth proceeds.

Silane burst is not as effective on Sample I, considering that its effect on flat silicon has the best results among the three, in terms of reducing biaxial tensile strains. Superlattice structure is shown to produce compressive components well to oppose the residual tensile strains on flat silicon, but it did not work as well when applied on nanostructured substrate. The early coalescence strategy had the best effect on nanostructured substrates (Sample III has the least strains when compared Sample I

and Sample II), but the same technique did not provide much strain relief on a flat substrate. This is because this growth structure does not provide strain relief by itself, but facilitated the nanostructures' ability to provide strain relief.

It can be seen that only Sample III has a reduction in biaxial strain over its reference (from 3.2×10^{-3} to 1.6×10^{-3}). This is likely to be the effect of its larger air voids present in between the nanostructures. It suggested that the voids allowed strain relaxation. This could be understood as the voids reduced the stiffness and rigidity of the substrate, till the depth of the nanostructures. Although the nanostructures are only 100 nm in height, the strain relaxation provided is still substantial for Sample III. As for Samples I and II, the biaxial strain either worsen or remained the same, compared to their respective reference. This shows that the 100 nm nanostructures did not provide additional strain relief if either in-situ silicon nitride masking or superlattice is incorporated in the growth structure.

Overall, the GaN quality on nanostructured silicon is worse than GaN on flat silicon (see Table 5-5). GaN films on nanostructured silicon all have higher dislocation density than GaN films on flat silicon (reference), regardless of the growth structure applied. This, unfortunately, showed that the nanostructured silicon generated higher dislocation density, instead of reducing it. This is probably because of the difficulty in attaining a flat layer on nanostructured silicon. As rougher interface is known to generate dislocations [226], the dislocation density increased when growth is done on the nanostructured surface.

Although all three samples have increased dislocation density, compared to their respective reference, the increase was not the same. It is worth mentioning that Sample III has the least increase in dislocation density among the three growth structures. Table 5-6 shows the ratio of dislocation density of the samples to their respective references. It can be seen that Sample III has the least increase in

dislocation density, among the three. It is likely that inducing faster film coalescence in Sample III contributed to the lower increase in dislocation density.

Table 5-6. Ratio of dislocation density of Sample I, II and III to their respective references, as estimated by XRD (see Table 5-5)

Sample	$\frac{\text{Screw dislocation density of Sample}}{\text{Screw dislocation density of Reference}}$	$\frac{\text{Edge dislocation density of Sample}}{\text{Edge dislocation density of Reference}}$
I	23	7.8
II	25	15
III	7	5

5.6 GaN film improvement with 50 nm tall nanostructures

From the above results, the quality of III-nitride films on 100 nm tall silicon nanostructures did not improve over III-nitride films on flat silicon, after considering dislocation density and biaxial stress. It could be said that the inclusion of 100 nm tall silicon nanostructures were not suitable for the growth structures in Samples I, II and III. The problem seems to be the difficulty in forming a smooth surface.

Another set of growths were done on shorter silicon nanostructures (50 nm). First, a 60 nm AlN nucleation layer was grown at 1070 ℃, followed by a 190 nm thick $Al_{0.6}Ga_{0.4}N$. Then a 280 nm GaN layer was grown followed by a LT-AlN interlayer grown at 750 ℃. Finally, another 280 nm GaN layer was grown. All layers were grown at 1000 ℃, unless otherwise stated. The same growth structure was also grown on a flat silicon substrate in the same growth run as reference.

Continuous GaN film was formed on the 50 nm tall nanostructures. It should be noted that III-nitride material completely filled in between the gaps of the nanostructures

(see Figure 5-21). This is due to the lower aspect ratio of the silicon nanostructures, which allowed the better coverage of AlN layer.

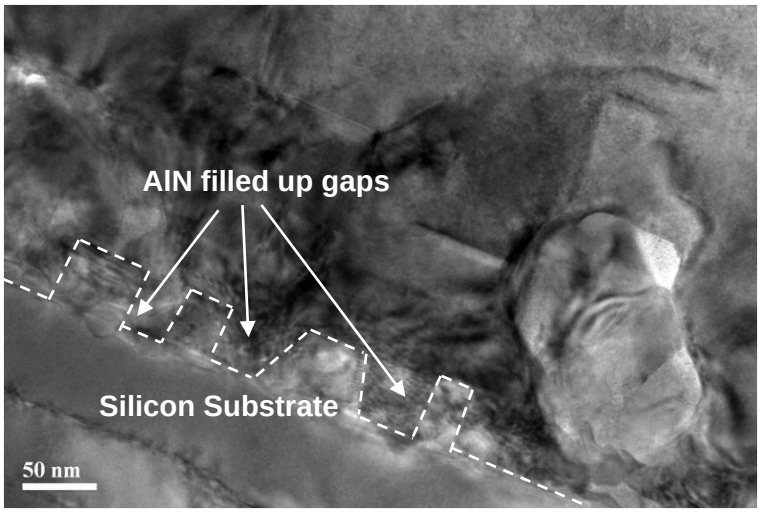

Figure 5-21. Cross-sectional TEM image of III-nitride grown on 50 nm tall nanostructures. The broken line is a guide to the position of the silicon nanostructures.

5.6.1 Stress in film

Strain in the film is estimated using XRD, by first finding c parameter (using θ value from GaN(0002) peaks) and using Equation (5-12). The biaxial strains in GaN film were calculated to be $(-0.2\pm0.1)\times10^{-3}$ and $(0.4\pm0.1)\times10^{-3}$ on the 50 nm nanostructures and reference sample, respectively (note that a positive strain indicates tensile strain). The corresponding biaxial stress were −0.1±0.1 GPa and 0.1±0.1 GPa in GaN on 50 nm nanostructures and reference sample (grown on flat silicon), respectively. A compressive biaxial strain was detected in GaN on 50 nm nanostructures, and more importantly, the strain was less tensile than GaN on flat silicon.

Phonons of the grown GaN were measured using Raman spectroscopy (see Figure 5-22). According to Tripathy et al. [164], Raman shift of E_2(TO) phonons of GaN can be used to determine the biaxial stress, where the shift $\Delta\omega = 4.3\ \sigma_{xx}$ cm^{-1} GPa^{-1}, and

a red shift is related to tensile stress. Taking the E_2(TO) value of 567.5 cm^{-1} as stress-free (taken from 400 μm thick free standing GaN [164]), the biaxial stresses were found to be 0.47±0.08 GPa and 0.58±0.08 GPa in GaN on 50 nm nanostructures and reference sample, respectively. As the errors for the values provided by literature were not provided, they were estimated based on the values' given significant figures (i.e. 4.3±0.1 σ_{xx} cm^{-1} GPa^{-1} and 567.5±0.1 cm^{-1}). The biaxial strains could be calculated using:

$$\frac{\text{Biaxial stress}}{\text{Biaxial strain}} = \left(C_{11} + C_{12} - \frac{2C_{13}^{\,2}}{C_{33}}\right)\varepsilon_a \qquad (5\text{-}14)$$

where C_{11}, C_{12}, C_{13} and C_{33} are elastic constants from reference [221]. The biaxial strains were $(1.0\pm0.3)\times10^{-3}$ and $(1.2\pm0.3)\times10^{-3}$ in GaN on 50 nm nanostructures and the reference sample, respectively.

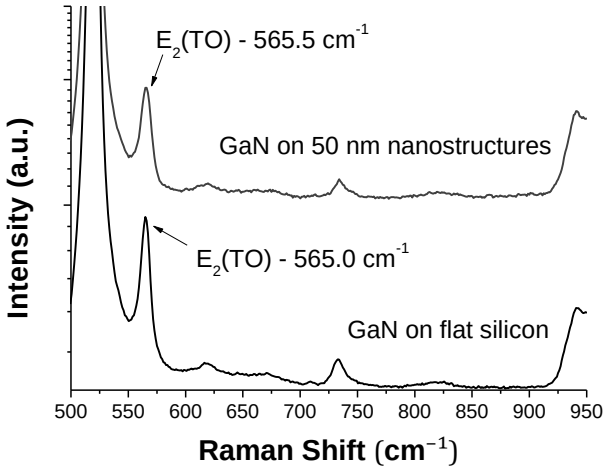

Figure 5-22. Raman shift of GaN film on 50 nm tall nanostructures and GaN film on flat silicon.

PL measurements were also taken to estimate the biaxial strains (see Figure 5-23). The peaks for the bound exciton were position at 3.465 eV and 3.459 eV for GaN on 50 nm nanostructures and the reference sample, respectively. The calculated biaxial

strains from the PL peak position are tabulated in Table 5-7. Strains by XRD and Raman measurements are also consolidated in Table 5-7.

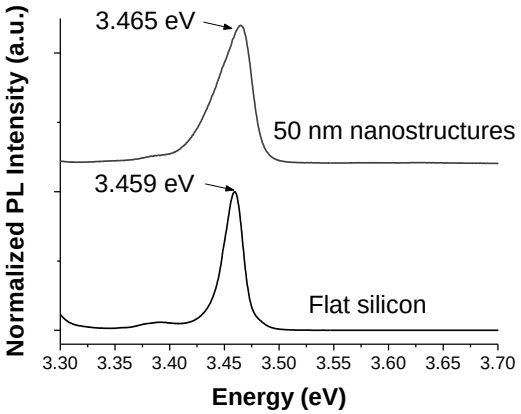

Figure 5-23. Comparison of normalized low temperature photoluminescence of GaN film on 50 nm tall nanostructures and GaN film on flat silicon.

Table 5-7. Consolidated biaxial strains from various characterizations.

Samples	**Estimated biaxial strains ($\times 10^{-3}$) from**		
	XRD	**Raman**	**PL**
GaN on 50 nm nanostructures	-0.2 ± 0.1	1.0 ± 0.3	1.0 ± 0.2
GaN on flat silicon	0.4 ± 0.1	1.2 ± 0.3	1.6 ± 0.2

The estimated strains based on the various methods described above, other than XRD, agree reasonably well with each other. The general trend is that GaN on 50 nm nanostructures still have lower tensile strains (Raman: 17% reduction, PL: 38% reduction) than GaN on flat silicon. From the results, it is demonstrated that stress can be alleviated by inclusion of Si nanostructures in between the GaN film. Some of the thermal stresses created from the high temperature growth can be relieved by composite of Si nanostructures within GaN layer.

5.6.2 Dislocation density

The dislocation densities were estimated by using hot acid etch method [227-229], where etch pits are counted and divided by the area examined. Figure 5-24 shows the top view SEM images of both GaN on 50 nm nanostructures and its reference, after hot phosphoric etch. The estimated etch pit density for GaN on 50 nm nanostructures and on flat Si were 6×10^{8} cm^{-2} and 1×10^{9} cm^{-2}, respectively.

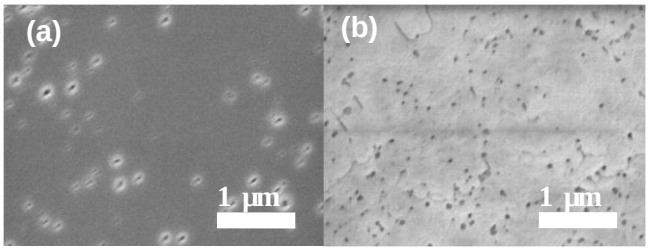

Figure 5-24. SEM image of top view of GaN on (a) 50 nm nanostructures and on (b) flat reference silicon, after hot phosphoric etch. The etch pit density of GaN on nanostructures and flat silicon were estimated to be 6×10^{8} cm^{-2} and 1×10^{9} cm^{-2}, respectively.

The dislocation densities of the samples were also estimated by the FWHM of rocking curves of GaN(0002) and GaN($10\bar{1}2$). The results are tabulated in Table 5-8. The total dislocation density is obtained by adding the values of screw and edge dislocation density together. Note that this value is likely to overestimate the total dislocation density as it assumed all dislocations are either pure screw or pure edge dislocations. Values of the etch pit density were also included in the table for easier referencing.

The XRD results suggested that the nanostructures induced more screw dislocations in the GaN grown on it, but reduced the overall total dislocations, by 20% (or by 40%, from etch pit density results). The overall dislocation density reduction is believed to be assisted by the coalescence of III-nitrides. During coalescence, dislocations which bend as the crystal grows laterally have a chance to interact with other dislocations

and annihilate each other [111]. The increased in screw dislocations could be explained by Figure 5-25. Before coalescence, the III-nitride crystals are supported by separated silicon nanostructures. If the crystal is tilted by an angle α, there will be a mismatch in height d, where $d \approx L \sin \alpha$, where L is the size of the crystal. Taking that the typical value of L is about 100 nm, a tilt angle of 0.3° is sufficient to cause the height mismatch d to be more than the c parameter (about 0.5 nm) of III-nitride crystal. This will induce screw dislocations to be generated.

Table 5-8. Estimated dislocation density and etch pit density of GaN on 50 nm nanostructures and flat silicon. The total dislocation density is calculated by adding the estimated screw and edge density. The lower value between the two samples in each column is underlined.

Sample	**Dislocation density estimated by FWHMs of XRD rocking curves**			**Etch pit density**
	Screw dislocation density	**Edge dislocation density**	**Total dislocation density**	
GaN on 50 nm nanostructures	4.2×10^{9} cm^{-2}	$\underline{1.5\times10^{10}}$ cm^{-2}	$\underline{1.9\times10^{10}}$ cm^{-2}	$\underline{6\times10^{8}}$ cm^{-2}
GaN on flat silicon	$\underline{3.0\times10^{9}}$ cm^{-2}	2.1×10^{10} cm^{-2}	2.4×10^{10} cm^{-2}	1×10^{9} cm^{-2}

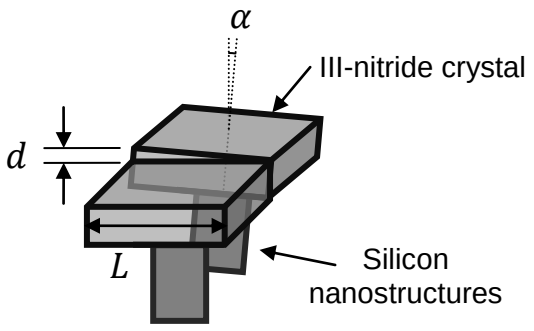

Figure 5-25. Schematic on the possible explanation on the increased screw dislocation density for GaN grown on silicon nanostructure.

5.6.3 Roughness of film

The roughness of the film can be measured by using AFM. Figure 5-26 shows the AFM images obtained from GaN on 50 nm nanostructures and on flat silicon. The root-mean-square (RMS) values of the roughness are found to be 1.70 nm and 0.364 nm for GaN on 50 nm nanostructures and on flat silicon, respectively. The increased roughness is expected because the substrate did not start off as a flat surface, but rather as a substrate with roughness of 50 nm.

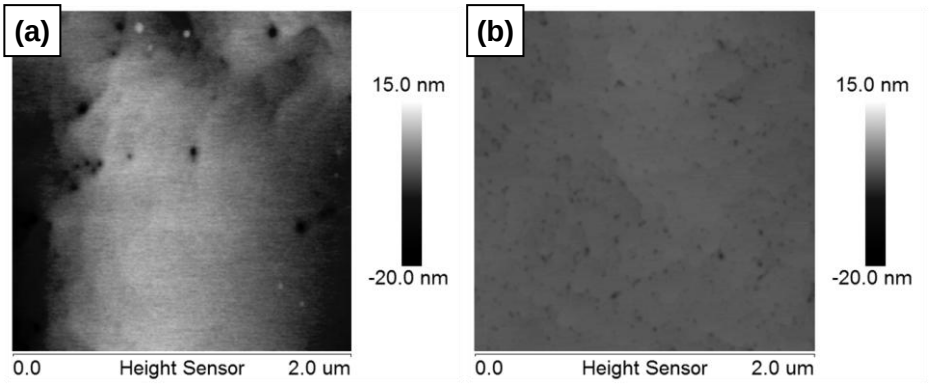

Figure 5-26. AFM images of the surface of GaN on (a) 50 nm nanostructures and on (b) flat silicon. The RMS values of the roughness are 1.70 nm and 0.364 nm for GaN on 50 nm nanostructures and on flat silicon, respectively. Both AFM images are adjusted to have the same scale for the color bar.

5.7 Summary

The nucleation of AlN on silicon nanostructures was investigated and explained. It was found that deposition of AlN on silicon nanostructures is also affected by parasitic reaction, which is also observed for deposition on flat silicon. It was found that high quality AlN crystals results from slow growth rates and they are crystallographically aligned to the silicon nanostructures that they grew on, where the relationship is AlN(0001)//Si(111) and AlN($1\bar{1}00$)//Si($11\bar{2}$). The large crystals are

found to be larger than 100 nm and are only found growing on tips of silicon nanostructures with size smaller than 40 nm. Conversely, AlN grown on the sidewalls of the silicon nanostructures are polycrystalline. The non-conformal deposition of AlN on the high aspect ratio nanostructures should encourage formation of air voids in between the nanostructures, which should relieve thermal residual stresses.

AlN thickness must be less than 200 nm for the subsequent GaN film to coalesce. Thinner AlN nucleation layers (60 nm or less) were found to aid in film coalescence. Nanostructures height was found to have a large effect on the quality of the GaN film, and continuous GaN film is difficult to form on nanostructures taller than 100 nm. Various growth structures to attain GaN on 100 nm tall silicon nanostructures were applied and compared. Sample III (with air voids) was found to have reduced biaxial strains over its reference. However, the general GaN quality was found to be worse off on 100 nm tall nanostructures than on flat silicon.

GaN growth was done on 50 nm tall nanostructures to compare with GaN growth on flat silicon. GaN growth on 50 nm tall nanostructures showed a reduction in stress and total dislocation density when compared to GaN on flat silicon. However, the screw dislocation density in GaN on the 50 nm nanostructures was found to be higher than GaN on flat silicon, as very slight tilting (0.3°) of the nanostructures would be sufficient to induce screw dislocations. The RMS roughness of the GaN film on 50 nm nanostructures is also found to be worse than GaN film on flat silicon (1.70 nm compared to 0.364 nm). Hence, an improvement in GaN quality, in terms of stress relaxation and total dislocation density, was observed when 50 nm nanostructures was incorporated, when compared to GaN on flat silicon. Nevertheless, the smoothness of the GaN surface suffered when growth was performed on the 50 nm nanostructures.

Chapter 6. Conclusions and future work

6.1 Conclusions

In this thesis, GaN was grown on nanopatterned silicon using MOCVD. Vertically standing nanostructures, with irregular shapes, were etched out of silicon (111) wafers by using one-step metal-assisted chemical etching (MACE). The nanostructures are separated from one another, having widths between 20 and 60 nm, and trenches between 80 nm and 120 nm wide. The nanostructures compose about 30-40% of the substrate area.

We have investigated the effects of varying etching conditions in one-step MACE for the formation of the silicon nanostructures. The etching conditions varied include silver nitrate concentration, temperature, hydrofluric acid concentration and etching duration. Several etching conditions were found to result in excessive tip etching. Such conditions include silver concentration of 0.04 M, temperature at 55 ℃ or higher, and HF concentration 7.0 M. From our results, it is established that 5.0 M HF and 0.02 M $AgNO_3$ at 25 ℃ with no stirring is a suitable etching condition, up to a duration of 600 s.

Based on the etch rate, we are able to determine that the reaction could be fitted to an Arrhenius equation. The activation energy is then found to be 0.33 ± 0.02 eV. Evidence was found that the rate limiting reaction resembles that of etching SiO_2 in HF. Evidence includes: similar value for activation energy as HF etching SiO_2 (between 0.35 and 0.40 eV, as determined by Judge [206]); etch rate's linear relationship with HF concentration between 1.0 to 7.0 M at 25 ℃.

Certain etching conditions promote damages to the tips of nanostructures, either by mechanical stresses due to hydrogen bubbles evolution or by tips etching due to the dense catalytic silver dendrites above the nanostructures. The mechanical stresses by hydrogen bubbles evolution are made worse by higher etching rate (i.e. higher temperatures and higher HF concentrations); and the tips etching are worsen by higher $AgNO_3$ concentrations. Other than changing etching conditions, implementation of stirring could reduce the tips damages by hydrogen bubbles.

Two distinct regimes were found for the etching of silicon by 1-step MACE, namely the short etching time regime and long etching time regime. The short etching time regime was found to have an etch rate of 1.51 nm/s, for etching duration of up to 100 s. After which the etch rate increased to 2.70 nm/s, in the long etching time regime. The change in the etch rate is attributed to the silver dendrite coverage on the surface, which is unique to the one-step MACE process. Note that the stated rates are pertinent to the use of 5.0 M HF and 0.02 M $AgNO_3$ at 25 ℃, with no stirring. This etching condition is also found to be reliable (minimal nanostructure tip etching) and controllable (by adjusting the etching duration) to obtain the desired nanostructure height, up to about 1.5 μm.

Size variation was also found to change with etching duration. For etching duration of 60 s and below, the trench widths are about 80 nm. When etching duration reached 120 s, the trenches widened to 100 nm; and when etching duration reached 300 s, the trenches widened to 120 nm. It was also found that the tall nanostructures (more than 600 nm) tend to bend and stick to one another, due to high aspect ratio (above 10).

It was found that deposition of AlN on silicon nanostructures is also affected by parasitic reactions, which is also observed for deposition on flat silicon. It was found that high quality AlN crystals result from slow growth rates, and large (more than 100 nm in diameter) single crystals of AlN were observed on tips of silicon nanostructures

of width less than 40 nm. The large AlN crystals are crystallographically aligned to the silicon nanostructures that they grew on, where the relationship is AlN(0001)//Si(111) and AlN($1\bar{1}00$)//Si($11\bar{2}$). Conversely, AlN layers grown on the sidewalls of the silicon nanostructures are polycrystalline. The non-conformal deposition of AlN on the high aspect ratio nanostructures was observed to encourage formation of air voids in between the nanostructures. This feature was found to correlate with lower thermal residual stresses.

The AlN thickness must not be too large (200 nm or more) or the subsequent GaN film grown would have difficulty coalescing. Thinner AlN nucleation layers (60 nm or less) were found to aid in subsequent film coalescence. Nanostructure height was found to have a large effect on the quality of the GaN film. Our experimental results had shown that continuous layer of GaN film can be grown on substrates with 100 nm tall nanostructures. When the height of nanostructures were increased to 300 nm, GaN coalescence did not occur even after a nominal thickness of about 500 nm of GaN layer was grown. When the height of nanostructures were increased further to 700 nm, only isolated GaN islands, of size ranging from 1 to 7 um, were formed.

Three different growth sequences were implemented on silicon substrates patterned with 100 nm tall nanostructures, and their GaN quality were compared. The different growth sequences each contained a main technique in improving GaN's quality, which are in-situ silicon nitride masking (Sample I), superlattice (Sample II) and graded AlGaN buffer layers (Sample III). For each growth sequence grown on the nanostructured substrate, the same growth sequence was also done on flat silicon as reference samples for comparison.

Using PL measurements to estimate, Sample III was found to have the lowest biaxial tensile strains among the nanopatterned substrates, and only it was the only sample to have lower strain than its reference sample (grown on flat silicon). Sample III was

also found to have the lowest dislocation density (estimated using XRD) among the nanopatterned substrates. Large air voids were observed to exist between the nanostructures of Sample III, and it was deduced that this reduced the stiffness and rigidity of the layer of nanostructures. Thus, reduction of strain was observed for Sample III. However, the overall GaN quality (based on dislocation density) on nanopatterned silicon substrates were worse than that on flat silicon substrates.

As GaN quality was found to be worse on 100 nm tall nanostructures than on flat silicon, GaN growth was done on 50 nm tall nanostructures. It was determined that there was an overall tensile strain reduction (from Raman: 17% reduction, and from PL: 38% reduction) for GaN on 50 nm tall nanostructures than on flat silicon. The GaN on 50 nm tall nanostructures also showed a reduction in the total dislocation density (estimated as a 20% reduction, based on XRD results, or at 40% reduction, based on etch pit density results), when compared to GaN on flat silicon. However, the screw dislocation density in GaN on the 50 nm nanostructures was found to be higher than GaN on flat silicon, as very slight tilting (0.3°) of the nanostructures would be sufficient to induce screw dislocations. The RMS roughness of the GaN film on 50 nm nanostructures is also found to be worse than GaN films on flat silicon (1.70 nm compared to 0.364 nm).

6.2 Recommendations for future work

Although the benefit of using one-step MACE is its simple fabrication of nanostructures, there is basically no control over the feature size and shape of the nanopattern. Much better control in the nanopattern could be created by using techniques like nanoimprinting and interference lithography. Hence, it will be very interesting to investigate the effects of different size features and nanostructure arrangement. It should be noted that the technique used must be able to create

nanopattern with small enough feature size as nanostructures with diameter less than 40 nm (see Chapter 5) are required for high quality AlN single crystals to form on silicon nanostructure tips. Both nanoimprint lithography [230] and interference lithography [231] have been used to achieve feature sizes smaller than 50 nm, which makes them suitable nanofabrication techniques.

It was found that GaN coalescence is difficult with taller silicon nanostructures. However, GaN coalescence might not necessarily be impossible. As the presence of 50 nm tall nanostructures are sufficient to induce a stress relaxation in the GaN layer, taller nanostructures are expected to improve the relaxation effect. Hence, it is worth exploring different growth techniques which could achieve GaN film coalescence with taller silicon nanostructures.

Finally, devices have yet to be fabricated out of GaN grown on nanopatterned substrates. As GaN could be used to fabricate several types of devices, such as LEDs and HEMTs, future work should include device fabrication as well. This will provide an actual and practical indication of the device improvement that such nanopatterned substrate might provide.

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