STUDY ON $IN_{0.53}GA_{0.47}As$ MOS DEVICES WITH PLASMA-PH_3/N_2 TREATMENT AND DEVICE STRUCTURE OPTIMIZATION

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Declaration

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

25th may 2014

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Summary

As the semiconductor industry approaches the limits of traditional silicon CMOS scaling, introduction of performance boosters like novel materials is becoming necessary. Nevertheless, several critical problems still need to be addressed.

First part of the thesis focuses on the issue with high-*k*/$In_{0.53}Ga_{0.47}As$ gate stack which is the high interface trap density resulting in gate stacks with low mobility, low I_{on}, poor gate stack thermal stability and large gate leakage making it unsuitable for gate stack scalability. A passivation layer involving plasma-PH_3/N_2 treatment on HfAlO $In_{0.53}Ga_{0.47}As$ MOSFET has been used to address these issues. Plasma-PH_3/N_2 passivated HfAlO/$In_{0.53}Ga_{0.47}As$ gate stack reveals good thermal stability up till 800°C with much lower gate leakage due to the absence of Frenkel Poole emission associated with trap energy levels of ~0.95-1.3eV. The improvements of peak mobility and hence on-state performance of this passivated device can be attributed to the reduced trap states in the upper half of the bandgap, possibly due to reduced free As, resulting in reduced Coulombic scattering compared to non-passivated device. Also the existence of a thicker passivation layer giving a thickness of ~0.6nm for passivated device compared to the interfacial layer of ~0.35nm for non-passivated device reduces the soft optical phonon scattering contributed by the HfAlO. In addition, its robust passivation layer is effective in preventing the interdiffusion of elements between the oxide and $In_{0.53}Ga_{0.47}As$ substrate, therefore reducing interface dipole scattering at high E-field and hence increases the mobility at high E-field compared to non-passivated device.

Further studies through TCAD simulations show that not only the concentration, but also the nature of the interface traps (acceptor-like vs donor-like) at upper half of the bandgap of the high-*k*/$In_{0.53}Ga_{0.47}As$ interface, can contribute to SS, V_{th} and hence I_{on}. It is shown that reduced acceptor-like traps at the interface of

high-*k*/$In_{0.53}Ga_{0.47}As$ plasma-PH_3/N_2 pasivated device is responsible for reduced V_{th} of the passivated device.

Second part of the thesis focuses on the issues with bulk-planar short channel implanted S/D $In_{0.53}Ga_{0.47}As$ MOSFETs which include the large S/D parasitic series resistance due to low active carrier doping concentration resulting in source starvation and poor device electrostatic integrity. Therefore device optimization through TCAD simulation has been performed through reduced gate-to-S/D spacing with addition of 15nm wide spacer, halo doping and junction engineering through raised S/D structure. Raised S/D is effective in improving device performance relative to implanted S/D due to its ability to reduce source starvation and improve electrostatic integrity. Further optimization, suitable for 22nm and 14nm gate length plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ MOSFETs, have also been predicted with channel engineering through RSD structure with thin channel of 3nm thickness, high-*k* spacers and R_c of 93Ω.µm. This structure, without heterostructure for L_g=14nm, is effective in achieving SS of 88.4mV/dec, DIBL=147mV/V with $I_{d,sat}$=1775µA/µm at V_g-$V_{t,sat}$=0.7V, V_d=0.7V. On the other hand device with heterostructure gives SS of 95.2mV/dec, DIBL=188.8mV/V and $I_{d,sat}$=2090µA/µm at V_g-$V_{t,sat}$=0.7V, V_d=0.7V.

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List of Symbols and Acronyms

Symbol /Acronym	Description
ALD	Atomic Layer Deposition
B	Ballistic coefficient
BTBT	Band to band tunneling
CBM	Conduction band minima
CD	Depletion capacitance
C_g	Gate capacitance
C_{gc}	Gate-to-channel capacitance
C_{it}	Interface trap capacitance
C_{lf}	Low frequency capacitance
CNL	Charge Neutrality Level
C_{ox}	Gate oxide capacitance
CP	Charge pumping
Cs	Semiconductor capacitance
DIBL	Drain Induced Barrier Lowering
D_{it}	Interface trap density
DOS	Density of states
E_a	Activation energy
ε_r	Dynamic dielectric constant
EBL	Electron beam lithography
E_c	Conduction band minima
EDT SCLC	Exponentially distributed trap SCLC
EDX	Energy Dispersion X-Ray
E_F	Fermi energy level
E_i	Intrinsic fermi level
EOT	Equivalent oxide thickness
E_t	Trap energy level
FN	Fowler-Nordheim
FP	Frenkel Poole
GGO	Gallium-Gadolinium Oxide
G_m	Maximum transconductance
HCl	Hydrochloric
$I_{d,sat}$	Saturation drive current
I_{on}	On-current
ISD	Implanted Source/Drain

k	Permittivity
J_g	Gate leakage current density
λ	Correlation length
L_g	Gate length
LO	Longitudinal optical phonons
m*	Effective mass
MBE	Molecular beam epitaxy
MLD	Mono-layer Doping
MOCVD	Metal-Organic-Chemical-Vapor-Deposition
μ_{eff}	Effective mobility
μ_{coul}	Mobility limited by coulombic scattering
μ_{ph}	Mobility limited by phonon scattering
μ_{sr}	Mobility limited by surface roughness scattering
$(NH_4)_2S$	Wet sulfide
N_{inv}	Inversion electron concentration
N_t	Average trap concentration
PECVD	Plasma enhanced chemical vapour deposition
PVD	Physical vapour deposition
P_xN_y	Phosphorus nitride
Q_{inv}	Inversion charge density
r	Backscattering rate
R_c	Contact resistance
RMS	Root mean square
RSD	Raised Source/Drain
R_{sh}	Sheet resistance
SCLC	Space Charge Limited Conduction
SCE	Short channel effect
S/D	Source/Drain
SE	Schottky Emission
SO	Soft optical
SS	Subthreshold Slope
TMA	trimethyl aluminum
CV/I	Gate delay
τ_c	Carrier transit time
τ_d	Dielectric relaxation time
T_{ch}	Channel thickness
t_f	Pulse fall time

TFL	Trap filled limited
TO	Transverse optical phonons
t_r	Pulse rise time
UTB	Ultra thin body
V_d	Drain voltage
V_g	Gate voltage
V_{inj}	Injection velocity
V_T	Thermal injection velocity
V_{th}	Threshold voltage at V_d=0.05V
$V_{t,sat}$	Threshold voltage at V_d=0.7V or 1V
W	Gate width
W_{eff}	Effective gate width

Chapter 1: Introduction and Motivation

1.1. Silicon transistor scaling: Benefits and Issues

Moore‘s Law predicted that the number of transistors placed on an integrated circuit (IC) would double every two years [1] and has been known to guide the progress. The device scaling is the key attribute for planar MOSFET circuitry in order to achieve significantly higher packing density per unit chip area, reduction of cost per function and improvement in circuit speed performance.

The key concept of the MOSFET scaling proposed by Dennard in 1974 [2] is that various structure and electrical parameters of MOSFET should be scaled simultaneously, which guarantees the reduction in device dimensions without compromising the current-voltage characteristics. However, as MOSFET continues to scale down to sub-100nm, the conventional device scaling is confronted with several limitations, which provide the trade-off relationships among on-current, power consumption and short channel effects as shown in Fig.1.1. One such example is that to maintain the on-current scaling with reduced gate length (L_g), oxide thickness has to be reduced, but this will cause greater power consumption in terms of high gate leakage current. Also, as L_g is scaled, significant control of channel by the gate is lost and the drain field begins to influence the channel formation, resulting in short channel effect (SCE). Hence, new device engineering methods to overcome these difficulties are much needed to mitigate the trade-offs.

These new device technologies, shown as possible solutions in Fig.1.1 [3] are known as the technology boosters, and they include technologies or

structures such as high-*k*/metal-gate for gate stack engineering, high carrier mobility or high carrier velocity channels, ultrathin-body (UTB) structures and multigate structures for channel engineering and metal source/drain (S/D) for S/D engineering. The principle of these technology boosters is to improve the device parameters such as gate leakage current, mobility, saturation velocity and short channel effects. For instance a 45nm process technology based on high-*k*, metal gate, and strained silicon was introduced in 2000 [4] while scaling of this technology continued to the 32nm technology node in 2009 [5]. More recently in 2011, FINFET structure was introduced to enable further scaling to the 22nm technology node [6]. As technology node progresses towards sub-20nm, fundamental limits of Si properties and gate pitch will impose limitations to the continuous scaling of device dimensions in terms of challenges to the conventional techniques and materials used for CMOS strain engineering. Therefore, future advancement of CMOS scaling would require novel channel materials, processes and device architectures.

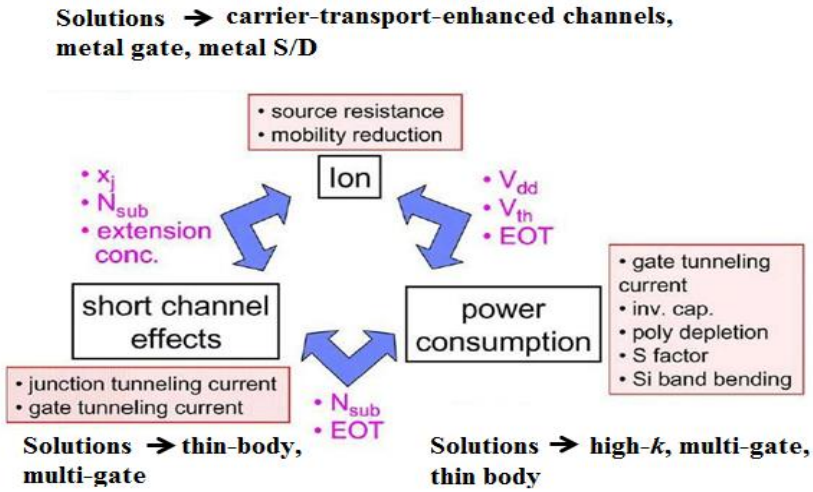

Fig.1.1. Trade-off factors among on-current, power consumption/leakage current and short channel effects under simple device scaling and possible solutions [3].

1.2. Motivation of III-V Channel Materials for Future CMOS applications

When MOSFET is scaled to deep sub-100nm technology node, carrier transport in the scaled device becomes quasi-ballistic. It has been shown through simulation and experiments that injection velocity, instead of saturation velocity, is still a reliable performance indicator for the drive current [7-10].

Lundstrom's theory [11] initially pointed out based on scattering theory that the drain current at the saturation condition is dominated by thermal injection velocity, V_T, at the source side instead of the saturation velocity, in short channel devices. The saturation current of a short channel device can be expressed as:

$$I_{d,sat}=C_{ox}W_{eff}V_T((1-r)/(1+r))(V_g-V_{th}) \qquad \text{Equation (1.1)}$$

where C_{ox} is the gate oxide capacitance, W_{eff} is the effective gate width, r is the backscattering coefficient which indicates the number of carriers backscattered to the source, V_g is the voltage between the gate and the source, V_{th} is the threshold voltage, and V_T is the thermal injection velocity. V_T is dependent on low field mobility and r is inversely proportional to low field mobility [9-10]. For extremely scaled devices operating in the ballistic regime i.e. r=0, where the ballistic coefficient, B=((1-r)/(1+r))=1, the maximum current would be controlled by the injection velocity near the source region of the transistor.

Therefore, by incorporating new channel materials with higher low field mobility and higher injection velocity near the source region, the performance of $In_{0.53}Ga_{0.47}As$ in quasi-ballistic regime is expected to be better than Si. Based on Table 1.1, III-V compound semiconductors have

significantly smaller electron effective mass compared to silicon which leads to high electron mobility that can translate into enhanced device performance at low supply voltage [12].

Table 1.1. Physical parameters of the commonly used semiconductors as channel materials [12].

	Si	Ge	GaAs	$In_{0.53}Ga_{0.47}As$	InAs	InSb
Electron mobility (cm^2/Vs)	1350	3900	8500	14000	33000	77000
Hole mobility (cm^2/Vs)	460	1900	400	400	460	850
Electron effective mass ($/m_0$)	0.19	0.082	0.067	0.05	0.027	0.013
Bandgap (eV)	1.12	0.66	1.42	0.74	0.36	0.17
Permitivity	11.8	16	12.4	13.9	14.8	17.7

1.3. Challenges of III-V CMOS Technology

In order to reap the advantages of the intrinsic properties of III-V materials, a lot of challenges still have to be overcome before the manufacturing of III-V logic transistors becomes viable [12]. Such challenges include cost effective heterogeneous integration of III-V on Si, formation of thermally stable gate dielectric with low interface state density and leakage and realization of S/D with low resistance. Fig.1.2 summarizes the challenges faced by III-V CMOS [13] and some will be briefly discussed in the subsequent sections.

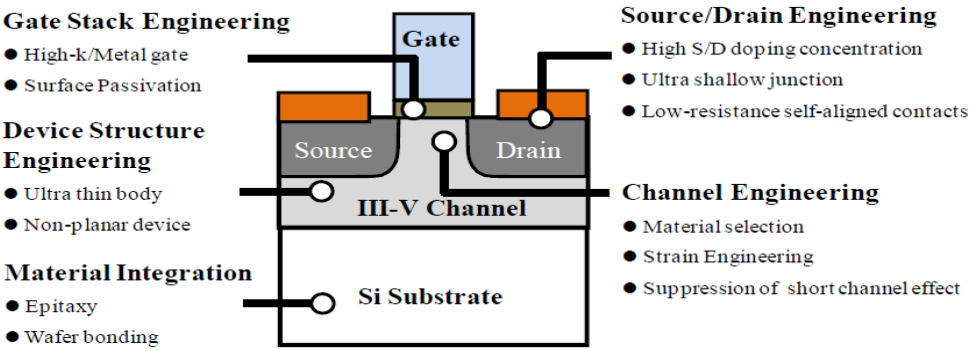

Fig.1.2. Schematic illustration showing the technical challenges faced by high mobility III-V CMOS on Si substrates for future logic applications [13].

1.3.1. Formation of High Quality and Thermodynamically Stable Gate Stack for $In_xGa_{1-x}As$ N-MOSFETs

As disussed in previous sections, significant increase in carrier injection velocity is crucial in order to maintain the commensurate performance scaling of MOSFETs to the gate length. Hence, to take advantage of the electronic transport properties of III-V NMOS, in particular $In_{0.53}Ga_{0.47}As$ MOSFET in this work, researchers are exploring for thermodynamically stable gate dielectrics which can form unpinned Fermi level at the $In_{0.53}Ga_{0.47}As$ oxide interface [14-28] since a decade ago.

In order to realize high performance $In_{0.53}Ga_{0.47}As$ N-MOSFET a high quality and thermodynamically stable high-*k* gate stack on $In_{0.53}Ga_{0.47}As$ is needed. However, when the surface is oxidized during high-*k* oxide deposition, a high density of interface states which include different native surface species caused by oxygen related reaction (Ga–O bonds, As–O bonds), interfacial lattice defects and stoichiometry perturbation such as As-As, elemental As, and As and Ga anti-sites can be formed [29-30]. Unlike SiO_2 on Si, the native oxides of $In_{0.53}Ga_{0.47}As$ can generate high density of interface states which can cause Fermi level

pinning, resulting in an increased subthreshold swing, frequency dispersion of capacitance, electron mobility degradation and creating reliability issues.

In order to reduce interface trap density (D_{it}) and unpin the $In_{0.53}Ga_{0.47}As$ interface, various techniques have been studied which include in-situ molecular beam epitaxy (MBE) growth of gallium-gadolinium oxide (GGO) [31], metal organic chemical vapour deposition (MOCVD) of HfAlO and HfO_2 with SiH_4, NH_3 or plasma-PH_3/N_2 treatment [26-27], atomic layer deposition (ALD) of Al_2O_3, HfO_2, ZrO_2, $La(AlO_x)/ZrO_2$ and $TaSiO_x$ [32-39] using silicon or InP capping layer [40-42]. Note that most methods employed do not involve high-*k* dielectric forming directly on $In_{0.53}Ga_{0.47}As$, which has the disadvantage of high D_{it} formation between the high-*k* dielectric and $In_{0.53}Ga_{0.47}As$, and thus can result in significant carrier scattering and mobility degradation. Nevertheless, all the reported D_{it} values on various MOS devices are still higher than $1x10^{11}cm^{-2}eV^{-1}$ [12] resulting in low electron mobility observed in inversion layer of $In_{0.53}Ga_{0.47}As$ N-MOSFET. Further reduction of D_{it} is still desirable.

One technique employed, other than passivation technique, to improve the mobility and hence device performance of $In_{0.53}Ga_{0.47}As$ MOSFET is to bury the channel beneath a wide bandgap material (known as capping layer), thus separating the charged interface states from the channel causing reduced Coulombic scattering and remote phonon scattering from oxide phonons. However, one disadvantage of this technique is the electron spillover from the channel to the capping layer, thus reducing the mobility in the high E-field. In addition, this technique may not provide good scalability as device scales due to its larger capacitance equivalent thickness (CET) caused by the presence of low-*k* capping layer. Also, the mobility of

the device would not only be dependent on the capping layer/$In_xGa_{1-x}As$ channel interface but also on the high-*k*/capping layer interface [43] which requires sufficiently low D_{it} and hence surface channel MOSFET studies involving such high-*k*/capping layer interface are still necessary.

Not only reduced D_{it} is important, thermally stable high-*k* dielectric is also required to ensure that the interface between high-*k* and $In_{0.53}Ga_{0.47}As$ maintains its high quality even after subsequent thermal process steps which include S/D dopant activation anneal of between 600°C-800°C.

1.3.2. Channel Engineering

Due to their significant transport advantage which allows high performance even at low supply voltage, high mobility materials are being very actively researched as channel materials for future highly scaled CMOS. However the device design considerations for $In_{0.53}Ga_{0.47}As$ MOSFET differ from that of a Si MOSFET. This is due to the fact that most explored high mobility materials have a significantly smaller bandgap compared to Si, leading to very high band-to-band tunneling (BTBT) leakage currents, which may limit their scalability. In addition, since most high mobility materials also typically have a higher permittivity (*k*), they also suffer from worse short channel effects (SCEs). Thus the off-state leakage and SCE of $In_{0.53}Ga_{0.47}As$ MOSFETs is expected to be of worse performance compared to Si MOSFETs. In addition, the driving capability of $In_{0.53}Ga_{0.47}As$ MOSFETs may also be adversely affected because of their much smaller density of states (DOS) due to its small effective mass

compared to silicon. Small DOS affects the device performance in terms of the loss of inversion capacitance which limits the transconductance and the reduction in scattering rate in the source of the MOSFET which limits the ability of the source to sustain a sufficiently large flow of carriers into the channel. The latter phenomenon is known as source starvation. In addition, when large gate electric field is applied, electrons filling up the Γ valley would tend to move to the L valley as well where the effective mass increases and mobility drops [44-45]. Hence, the preferred $In_xGa_{1-x}As$ alloy is one with larger energy level difference between different Γ-L valleys but also with acceptable conduction band DOS [46-47].

1.3.3. Formation of Ultrashallow Junctions With Low S/D Resistance

In addition to the gate stack, selection of the best ohmic contact and junction technology is also important. Implanted junctions that have served silicon well may not be suitable for compound semiconductors due to the compound nature of $In_{0.53}Ga_{0.47}As$ which can result in lower maximum activated doping density, loss of stoichiometry due to preferential group V evaporation and difficulty in recovering from implant amorphization.

A number of alternatives are being studied to replace implantation as the junction technology of source. One example of a promising approach is selective regrowth, where either MBE or MOCVD is used to selectively regrow very heavily doped S/D regions [48-49]. Advantages of such approach over implantation include 1) abrupt doping profile 2) reduced drain junction leakage current, which controls the device off-state leakage, caused by the absence of implantation damage and 3) high doping density.

This can provide low access resistance (in addition to low contact resistance) and reduces the junction leakage which tends to become significant due to its smaller bandgap than silicon, hence addressing the issues related to device scalability as device approaches deep sub-100nm technology node.

Other techniques pursued to create a potentially defect-free S/D is the use of silicide like process involving selective epitaxy of GeSi on N+ $In_{0.53}Ga_{0.47}As$ with two step metallization process [50-51] and monolayer doping (MLD) through the use of sulphur [52].

1.4. Thesis outline

The focus of this thesis would be addressing the three challenges of $In_xGa_{1-x}As$ MOSFETs described in previous sections. The issues in Sections 1.3.1 is addressed in Chapters 3-6. The issues in Sections 1.3.2-1.3.3 will be addressed in TCAD simulation Chapter 7. The main technical contributions would be documented into 6 chapters as shown below.

Chapter 2 consists of an overview of passivation techniques on $In_{0.53}Ga_{0.47}As$ and description on charge pumping technique for interface trap characterization. In addition, an overview of the gate leakage mechanisms used in this work as well as insights on new mobility scattering mechanisms, more specific to $In_{0.53}Ga_{0.47}As$ MOSFETs obtained from this work, are summarized. Also, process flows for the long channel and short channel device fabrication have been included.

In Chapter 3, the robustness of the high-*k*/$In_{0.53}Ga_{0.47}As$ with plasma-PH_3/N_2 treatment with high temperature annealing has been studied by varying annealing temperature from 600°C to 800°C after completion of

device fabrication and quantifying the effects on D_{it}, J_g, and EOT. This is needed to study the thermodynamic stability of the plasma-PH_3/N_2 passivated/HfAlO gate stack on $In_{0.53}Ga_{0.47}As$ MOSFET. Plasma-PH_3/N_2 treated planar devices have also been fabricated with submicron gate lengths up to 0.6μm to investigate the potential device scaling of plasma-PH_3/N_2 treated devices and benchmarked to show results comparable to that of other passivation techniques in terms of $I_{d,sat}$, mobility, D_{it} and J_g.

In Chapter 4, the quality of the gate oxide formed has been studied through the gate leakage conduction mechanism. It is found that non-passivated gate oxide leakage mechanism is dominated by bulk limited conduction mechanism such as exponentially distributed Space Charge Limited Conduction (EDT-SCLC) mechanism while passivated device is dominated by Trap Free SCLC mechanism implying that the trap states in the bulk oxide do not dominate the transport. In addition, the off-state leakage of the long channel $In_{0.53}Ga_{0.47}As$ MOSFETs are dominated by reverse biased drain-substrate leakage, due to the Shockley Read Hall mechanism caused by unoptimized S/D implant and annealing conditions.

Chapter 5 is dedicated to understand the reason for the channel mobility enhancement of plasma-PH_3/N_2 passivated MOSFET in the low to high vertical E-field region by plotting out temperature dependence measurements of mobility. The positive temperature dependence of mobility in the low field region for both non-passivated and passivated devices given by < 0.2MV/cm shows that Coulombic scattering is present. However, the reason for higher peak mobility of plasma-PH_3/N_2 passivated device is due to reduced D_{it} causing reduced Coulombic scattering. In addition, its reduced soft optical phonon scattering from the HfAlO is attributed to the

thicker ~0.6nm thick and robust passivation layer, known as P_xN_y layer, of the passivated device compared to the ~0.35nm thick interfacial layer of non-passivated device. In addition to reduced surface roughness scattering, the reduced interface dipole scattering is attributed to the ~0.6nm thick robust passivation layer which prevents interdiffusion of In/Ga across the interface resulting in less randomly oriented dipoles. Thus these reduced soft optical phonon scattering and reduced surface roughness and interface dipole scattering contributed to the higher mobility in mid to high E-field region respectively.

Chapter 6 involves TCAD simulation with calibration parameters being carried out to match data from previous IEDM 2008 published works from our group. The aim of this TCAD study is to: 1) confirm that the larger V_{th} for non- passivated device is caused by larger concentration of acceptor-like traps as observed from our experimental results in Chapter 4 2) confirm the reason for larger I_{off} is due to its larger concentration of donor-like traps, as explained from the energy band-diagram and its relation to the D_{it} which affect the I_d-V_g plots and 3) investigate the performance scalability of $In_{0.53}Ga_{0.47}As$ MOSFET with and without passivation for L_g up till 60nm for the current process flow used by our group.

Chapter 7 also involves TCAD simulation, with similar calibration parameters used in Chapter 6, but with device optimization of plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ MOSFET by changing the original process flow or device dimension. This is done through (a) reduced gate to S/D contact spacing to 15nm, by adding spacer of width 15nm, from 2μm in the original process flow (b) reduced contact resistance to 400Ω.μm achievable in implanted S/D $In_{0.53}Ga_{0.47}As$ MOSFET, compared to 1200Ω.μm in the

original process flow (c) Addition of halo implant. To counteract the trade-off between electrostatic integrity and drive current, performance scalability of raised S/D (RSD) MOSFET is studied and it is found to be beneficial due to reduced source starvation effect. In order to sustain low SCE up till 14nm technology node, thin channel with RSD MOSFET, high-*k* spacer and structures both with and without heterostructure, has also been studied and benchmarked with results from other simulation groups.

Chapter 8 would show the general conclusions and suggestions for future work.

A flow chart of the outline of the thesis which is divided into two branches dealing with research issues addressed through experimental work as well as partly TCAD work as shown in Fig.1.3 and TCAD work involving optimization of device structures as shown in Fig.1.4.

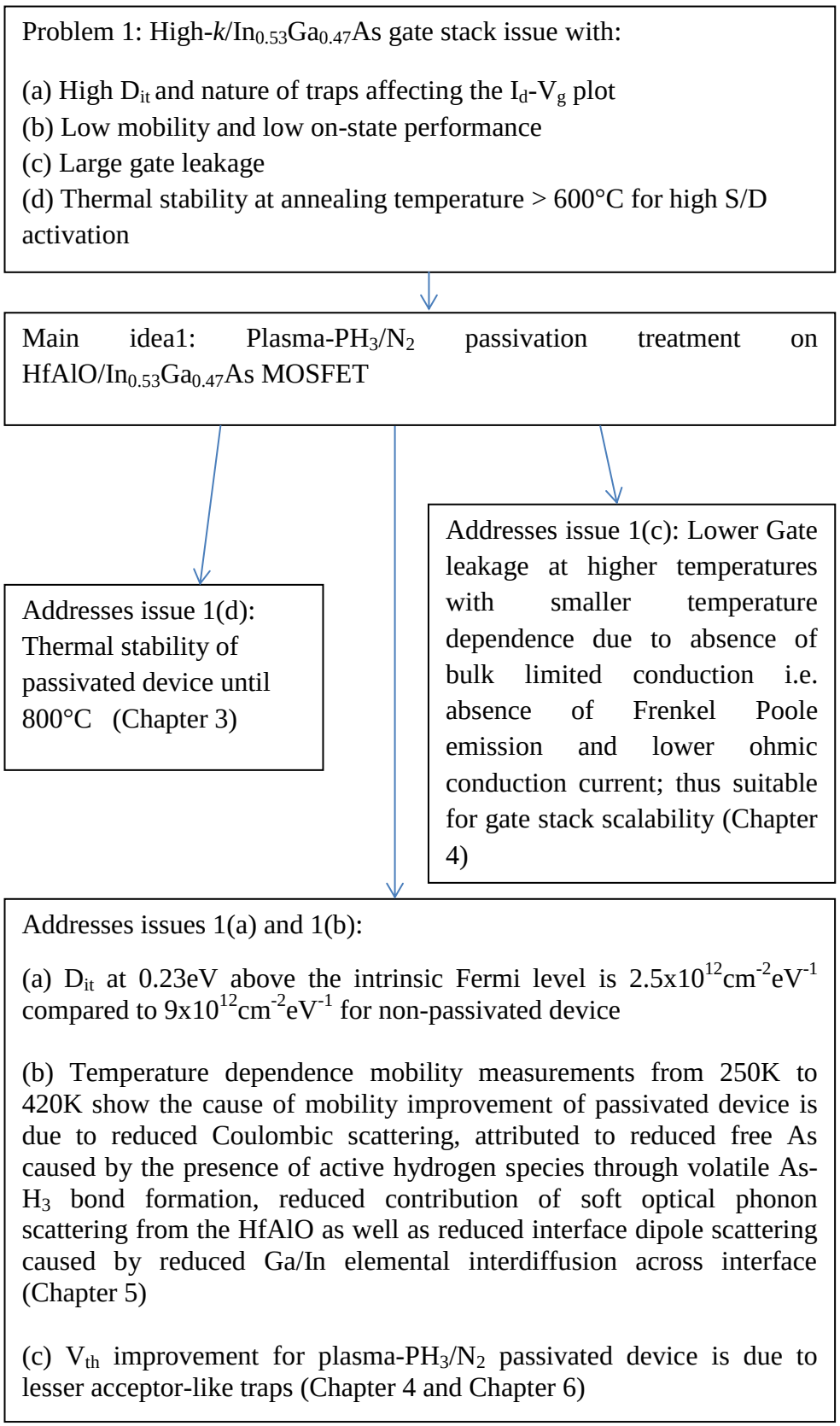

Fig.1.3. Flowchart of the issues addressed in high-*k*/$In_{0.53}Ga_{0.47}As$ MOSFETs in the first part of the thesis found in Chapters 3-6.

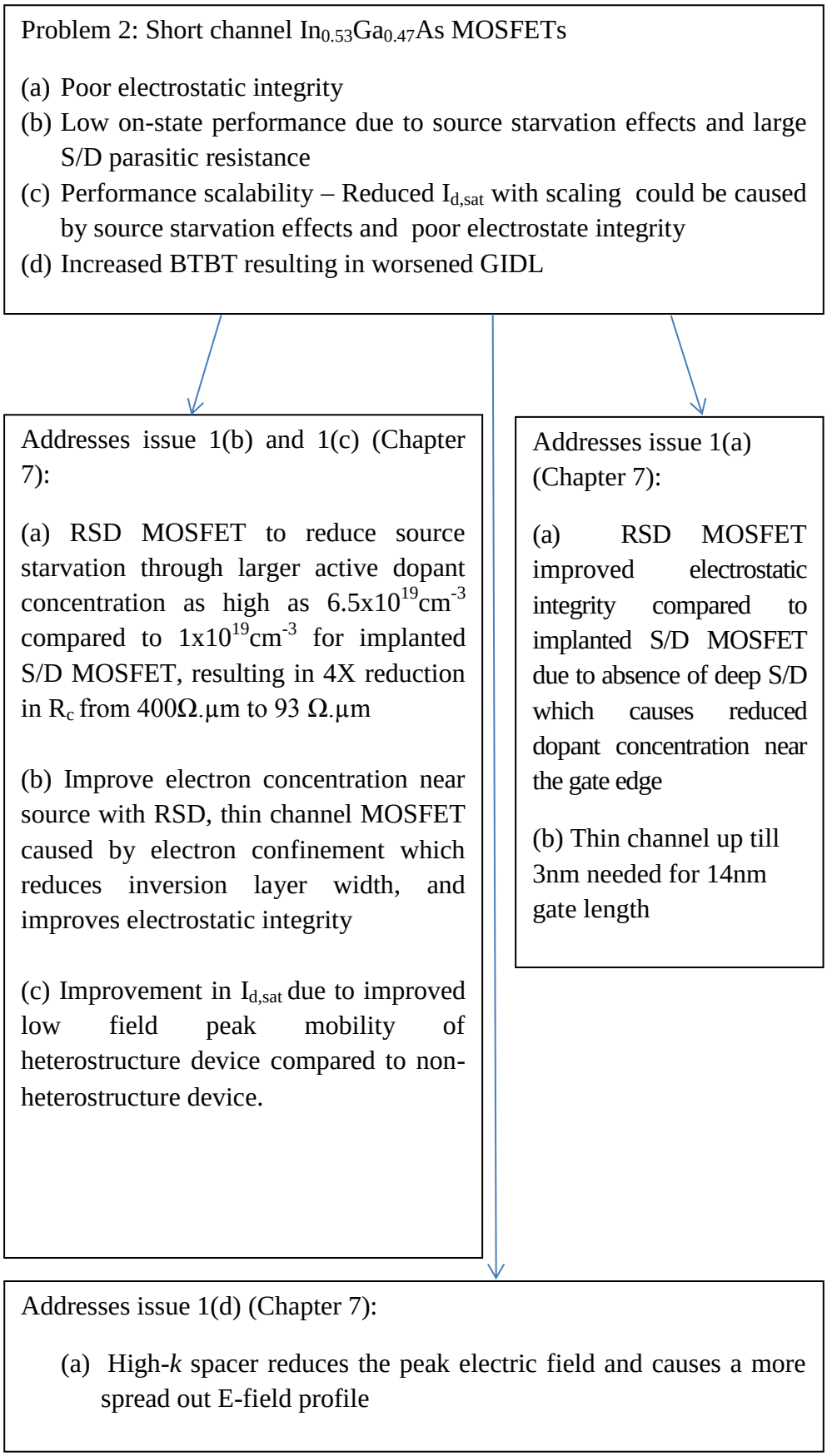

Fig.1.4. Flowchart of the issues addressed in high-*k*/$In_{0.53}Ga_{0.47}As$ MOSFETs in the second part of the thesis found in Chapter 7.

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Chapter 2: Literature Review and Fabrication Process

2.1. Overview of $In_xGa_{1-x}As$ Passivation Techniques

Sulfur-passivation by wet chemical treatment has been adopted in the E-mode MOSFET demonstrations as a practical and effective passivation of GaAs-based III-V surface after the native oxide removal by wet etching [1-3]. It is believed that the wet sulfide ($(NH_4)_2S$) treatment leaves the cleaned $In_xGa_{1-x}As$ surface sulfur-terminated with a weak bonding of chemisorbed sulfur over the surface like in the case of GaAs [4]. Thus, the formation of native oxides of $In_xGa_{1-x}As$ may be much suppressed during air exposure before loading the samples into the dielectric deposition chamber. However, the wet chemical treatment alone is not sufficient to accomplish a well-ordered surface passivation mainly due to the poor thermal stability of the sulfur bonds on surface [5]. The use of Si interfacial passivation layer (IPL), through the use of ex-situ amorphous Si deposition using physical vapor deposition (PVD) or molecular beam epitaxy (MBE) tools, atomic layer deposition (ALD) technique or plasma enhanced chemical vapor deposition (PECVD), is found to improve subthreshold characteristics, drive current and channel mobility of $In_xGa_{1-x}As$ N-MOSFETs with ALD Al_2O_3, PVD HfO_2 and MBE $LaAlO_3$ gate oxides [6-7]. With the use of ALD Al_2O_3/PECVD Si interlayer/$In_xGa_{1-x}As$, a much better transport characteristic (higher transconductance (G_m), $I_{d,sat}$ and mobility) was reported compared to without Si interlayer [8]. The species mentioned to be responsible for the poor device performance for device without Si IPL is the higher oxidation state of Ga, Ga_2O_3 [9], or formation of undimerized As when Ga_2O_3 is present [10]. However, one of the problems associated with this method is that Si IPL is fully or partially

oxidized prior to or during high-*k* oxide deposition, and thus becomes a part of the gate stack contributing to EOT. In addition, if a portion of Si deposited to the $In_xGa_{1-x}As$ surface is not oxidized or bonded, the issue of Si in-diffusion at elevated temperatures may occur. However, this diffusion can be suppressed with reduced Si IPL thickness and controlling its bonding status with oxygen and arsenic at the interface [11].

Despite several types of high-*k* deposited such as ZrO_2 [12-13], Al_2O_3 [14-15], HfO_2 [16-19] and $AlLaO_3$ [20] on N-$In_xGa_{1-x}As$ using ALD, high D_{it} exist at lower half part of the bandgap [21]. It has been found that atomic hydrogen is more effective than molecular hydrogen in passivating bulk defects of GaAs and much less likely to harm interface of the substrate unlike those from energetic hydrogen ions of plasma [22]. Papers have reported the benefits of hydrogen passivation treatment, one of which is that D_{it} of GaAs/Ga_2O_3 interface can be reduced to ~$10^{11}cm^{-2}eV^{-1}$ after the hydrogen (H_2) plasma clean of GaAs surface prior to the e-beam deposition of Ga_2O_3 [23]. Brammertz and Lin [24-26] have also shown that using hydrogen anneal, similar benefits can be obtained for $In_xGa_{1-x}As/Al_2O_3$ interface. However, the effectiveness of H_2 treatment on D_{it} distribution is still unclear. Taken from Ref [25], where studies have been performed on $(NH_4)_2S$ treated ALD Al_2O_3 on p-$In_xGa_{1-x}As$ capacitor, H_2 anneal is found to be effective in reducing D_{it} in the upper half of bandgap only but less on the lower half of bandgap. On the other hand, it is found that the combined use of HCl, $(NH_4)_2S$ and trimethyl aluminum (TMA) treatment along with PDA in pure H_2 annealing is effective in reducing D_{it} in the lower half of the bandgap compared to the results obtained from the use of hydrochloric acid (HCl) and $(NH_4)_2S$ treatment together with dry TMA surface treatment for

the ALD process with PDA in N_2 gas [21]. Hence, based on these passivation treatments method used, no specific technique has been found to effectively suppress the D_{it} throughout the entire bandgap. Thus, further advances in reducing D_{it} across the entire bandgap, using H_2 or with other novel methods, are still required before replacing silicon channel with high indium content $In_xGa_{1-x}As$.

Note that exposing hydrogen passivated $In_{0.53}Ga_{0.47}As$ to high temperature anneal can result in breaking of In-H or Ga-H bonds. This is because breaking of Si-H bonds in Si/SiO_2 has been observed at high temperature anneal or during hot carrier injection caused by high electric field due to its low Si-H binding energy (3.04eV) and thus reactivate the interface states. Since Ga-H and In-H bonds have bond strengths given by 2.76eV and 2.52eV respectively [27] which are even lower than Si-H bond, the likelihood of Ga-H/In-H bond breaking is even more than Si-H bond. Hence, even though using hydrogen passivation (such as forming gas anneal) for $In_{0.53}Ga_{0.47}As$ is beneficial in reducing the interface trap density through removal of occupied dangling bond, it is appealing for process steps after the final device fabrication step or for those gate first processes which use low temperature in-situ epitaxially grown raised S/D. This may be one of the reasons why most work which performed hydrogen anneal on $In_{0.53}Ga_{0.47}As$ devices are carried out on $In_{0.53}Ga_{0.47}As$ MOSCAPS or MOSFETs with gate last processes [28-30].

In addition, other passivation techniques like ammonia passivation and phosphorus passivation has been carried out on $In_{0.53}Ga_{0.47}As$ by several groups to reduce the D_{it} [31-32]. Formation of Ga-N from ammonia passivation has been found to improve D_{it} and is expected to be more

thermally stable than Ga-P due to its larger bond strength of 3.2eV for Ga-N compared to 2.38eV for Ga-P bond [27]. However, plasma-PH_3/N_2 treatment used in this work has the additional advantage of the presence of a P_xN_y layer on top of the Ga-P bond and with a bond strength which is even larger at 6.39eV than Ga-N. The significance of this is the higher chemical stability of P_xN_y which only disintegrates at 850°C onwards allowing $HfAlO/P_xN_y/In_{0.53}Ga_{0.47}As$ device to achieve a thermally stable gate stack suitable for gate-first self-aligned device.

Thus this motivated the study of plasma-PH_3/N_2 passivation which is investigated in this work, as well as investigation on whether the D_{it} within the whole or part of the bandgap or only part of it that can be effectively suppressed. As will be shown in Section 5.2.3.1 Fig.5.3, plasma-PH_3/N_2 passivation is effective in reducing interface trap density in the upper half of the bandgap, to comparable levels with other passivation techniques as shown in Fig.3.10 in Section 3.4.2.

2.1.1. Overview of the Mechanism of plasma-PH_3/N_2 Treatment

Mechanism of plasma-PH_3/N_2 treatment, which refers to how the plasma-PH_3/N_2 reacts with the substrate and form the passivation materials of P_xN_y and P-for-As exchange layer, has already been explained and analysed in thesis reference from a fellow team member from our group [33]. Hence, to summarize the mechanism, PH_3 at over 430°C has been suggested to react with $In_{0.53}Ga_{0.47}As$ substrate, thus producing P-for-As exchange layer first. This is then followed by the deposition of a stable atomically thin P_xN_y layer on the P-for-As exchange layer through the reaction mechanism of the activated species of PH_3 and N_2 in a suitable

plasma condition. In addition, hydrogen from the PH_3 is also beneficial to interact with the displaced free As to form volatile As-H_3 species that is easily desorbed through evaporation. The thermal stability of the P_xN_y material, in which the atoms are bonded by covalent bonds, might be the main reason why the gate stack with this passivation shows the improved electrical characteristics compared to non-passivated gate stack at even high temperature.

2.2. Overview of Charge Pumping Technique

The charge pumping method, proposed by Brugler and Jespers [34], requires fully functional MOSFETs as test structures and useful for determining the interface trap density distributed across the bandgap of the high-k/semiconductor MOSFET interface. The setup is as shown in Fig.2.1. The MOSFET source and drain are tied together and reverse biased with voltage V_R. A time varying gate voltage is applied to drive the surface under the gate into inversion and accumulation. The charge pumping current is measured at the substrate.

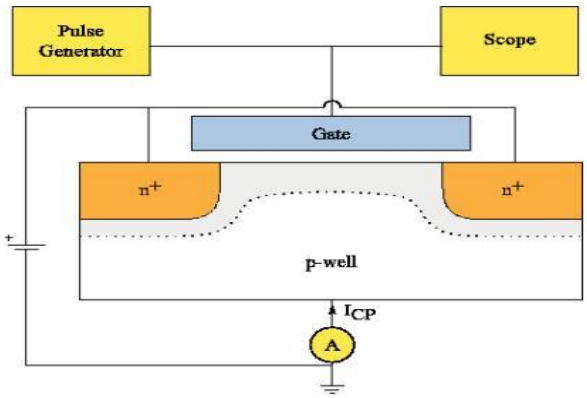


Fig.2.1. Basic experimental set-up for charge pumping measurement [35].

When the transistor is pulsed into inversion, surface becomes deeply depleted and electrons will flow from S/D to channel region. Some of these electrons would be captured by the surface traps as shown in Fig.2.2(a). When the gate pulse drives back into accumulation, the trapped electrons captured by traps located at shallow energy levels would drift back to S/D, while the remaining trapped electrons at deeper energy levels will recombine with the majority carriers from the substrate. This recombination will give rise to a net flow of charges into the substrate as shown in Fig.2.2(b), which is proportional to D_{it} [36].

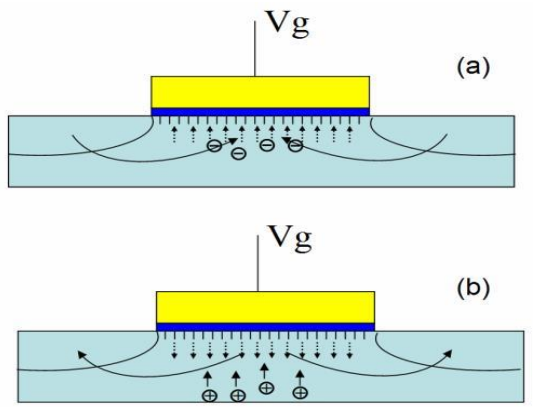


Fig.2.2. Illustration of charge pumping effects by varying the V_g (a) in inversion (b) in accumulation on a MOSFET [36].

One of the advantages of charge pumping is that it may be a better tool to probe the interface, rather than C-V and G-V characteristics, since it is a direct measurement [37-38]. In addition, the interpretation of data does not require sophisticated modeling unlike in the case of C-V and G-C characteristics. The charge pumping signal directly reflects the amount of D_{it} without being affected by the weak inversion. Moreover, the energy dependence of D_{it} in the band gap can be derived from the charge pumping analysis.

One of the disadvantages of this technique is that at 300K, only a small portion of the traps within the $In_xGa_{1-x}As$ bandgap is scanned and hence resulting in underestimation of the true value of the D_{it}. By measuring at lower temperature, the D_{it} distribution can be characterized across a wider portion of the bandgap since the electron and hole emission levels move closer to the band edges. Thus a monotonous increase in charge pumping current is expected when lowering the temperature. Another way to characterize the D_{it} distribution across a wider portion of the bandgap is to measure with shorter transition times. According to emission level theory, lowering the transition times below 100ns at 300K will enable D_{it} to be scanned further into the energy band gap.

In this work, as shown in Fig.5.3 in Section 5.2.3.1, we have used this method to evaluate the trap density across the $HfAlO/In_{0.53}Ga_{0.47}As$ plasma-PH_3/N_2 and non-passivated devices. However, due to lack of equipment for measurement with varying temperature, data from charge pumping measurement carried out only at room temperature will be studied. Nevertheless, it is sufficient to show that interface trap density is effectively reduced at areas near the upper half of the bandgap with plasma-PH_3/N_2 treatment.

2.3. Overview of Gate Leakage Mechanisms

Several mechanisms contribute to gate leakage current. Conduction mechanisms can be grouped into electrode limited conduction mechanisms (injection limited conduction mechanisms) or bulk limited condution mechanisms, which depend only on the properties of the dielectric itself. Measuring the temperature dependent conduction currents helps to

determine the constitution of the conduction currents. Electrode limited conduction mechanisms include Schottky emission (SE), Fowler Nordheim (FN) tunnelling, direct tunnelling and thermionic field emission. Bulk limited conduction mechanisms include Frenkel Poole emission, hopping conduction, ohmic conduction and Space Charge limited conduction. In this section, space charge limited conduction and Frenkel Pool emission would be explained since these mechanisms are found to exist in our non-passivated HfAlO/$In_{0.53}Ga_{0.47}As$ MOSFET which could be responsible for its higher leakage current compared to the plasma-PH_3/N_2 passivated HfAlO/$In_{0.53}Ga_{0.47}As$ MOSFET.

2.3.1. Space Charge Limited Conduction

Mott and Gurney stated that under applied bias, the free carrier concentration can be increased due to the injection of free carriers in the vicinity of a junction formed by different materials [39]. The space charge effect is said to occur when the injected free-carrier concentration is larger than the thermal equilibrium value. The injected carriers influence the space charge and the electric field profile which drives the current. The current produced due to the presence of a space charge effect is called the Space-Charge-Limited (SCL) current [40].

When electrons are thermally excited to energy sufficient to overcome the barrier, Φ, at the emission surface, electrons would be injected into the conduction band of the material, in this case gate oxide. The frequent collisions with the phonons of the oxide and the structural imperfections in the oxide are the dominant factors of electron flow in the conduction band of the oxide [41]. Mott and Gurney observed that the

presence of localized electron traps located in the forbidden gap could drastically interfere with the passage of injected current [42]. Rose then gave a detailed description of the form and magnitude of the reduction in injected current due to localized trapping of the injected carriers [39].

2.3.1.1 Trap Free Insulator and Insulator with Shallow Traps

A possible source of these electrons leading to gate leakage might be a set of donor-like traps so shallow that they are not effective as electron traps Here, once the injected free electron concentration becomes comparable to the thermally generated electrons, the current voltage characteristics will depart from Ohm's law and follow the Trap-Free square law. The onset of SCL current injection will place at the crossover voltage V_x (Trap Free) defined in Fig.2.3. This current voltage characteristic is true for trap-free insulators or when trap states do not dominate the transport. For such insulators, the J-V characteristics within the Trap-free Square Law regime in Fig.2.3 is described with slope given by ~2 [43].

On the other hand, insulators containing shallow traps have different current-voltage characteristics. The current voltage curve follows Ohm's law and transitions to the given crossover voltage V_x (shallow traps) is determined as Equation (2.1):

$$V_X = \frac{8qn_o d^2}{9\varepsilon_r \varepsilon_o \theta} \qquad \text{Equation (2.1)}$$

As long as the Fermi level lies below the trap level E_t, the traps are shallow and the current voltage characteristics follows the "Shallow Trap I-V Characteristics" regime after it transitions from Ohm's law. In this regime,

the slope would be given by ~3 due to presence of trap states that are exponentially distributed in energy [43] i.e. known as EDT-SCLC mechanism. Following this, the Fermi level keeps rising as electrons are being injected. Thus, at $V=V_{TFL}$, the Fermi level crosses E_t and the current voltage curve merges with the Trap Filled Limited (TFL) law. After Fermi level crosses E_t, these traps become deep traps and current increases sharply for small change in voltage at V_{TFL} [39]. A typical current-voltage characteristic for the case of trap free insulator and insulator with shallow traps is shown in Fig.2.3 [44].

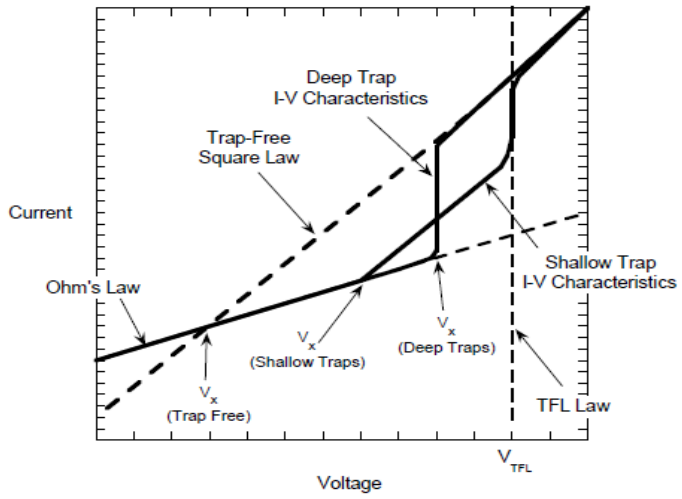


Fig.2.3. Space Charge limited current voltage characteristics for insulators containing trap free and shallow traps [44].

Hence, based on the explanation above, the SCLC mechanism is identified to be present as Trap-Free SCLC mechanism for plasma-PH_3/N_2 passivated device and EDT-SCLC mechanism for non-passivated device as shown in Section 4.2.2.2. Despite the Trap-Free Square Law showing larger gate leakage current than regime "Shallow Trap I-V Characteristics" regime in Fig.2.3, the experimental results obtained in this work shows non-

passivated device giving larger gate leakage current than passivated device in Fig.4.6 from Section 4.2.2.1. This is due to the larger ohmic conduction current for non-passivated device compared to plasma-PH_3/N_2 passivated device.

2.3.2. Frenkel Poole (FP) Emission

FP emission results from the lowering of Coulombic potential barrier by an applied electric field. The FP effect is associated with barrier at the trap well in the bulk of the insulator film i.e. the coulomb potential energy of the electrons in a trapping center can be reduced by an applied field across the dielectric film shown in Fig.2.4. Hence, this reduction in potential energy can increase the probability of an electron being thermally excited out of the trap into the conduction band of the dielectric. The leakage current associated with FP emission can be determined by utilizing the following Equation (2.2).

$$J = (qN_C\mu)E\exp\left[\frac{-q(\varphi_t - \sqrt{qE/\pi\varepsilon_r})}{kT}\right] \qquad \text{Equation (2.2)}$$

where N_c is the density of states in the conduction band, μ is the mobility, $q\varphi_t$ is the trap energy level, E is the electric field and ε_r is the dynamic dielectric constant. For FP emission the plot of ln(J/E) vs $E^{1/2}$ should be linear with the inverse of the slope corresponding to reported ε_r of the high-*k* oxide [45]. Since FP emission is owing to the thermal activation under an electric field, this conduction mechansim is often observed at high temperature and high electric field. This mechanism is identified in the high field region of non-passivated device given in Section 4.2.2.2 in Fig.4.9.

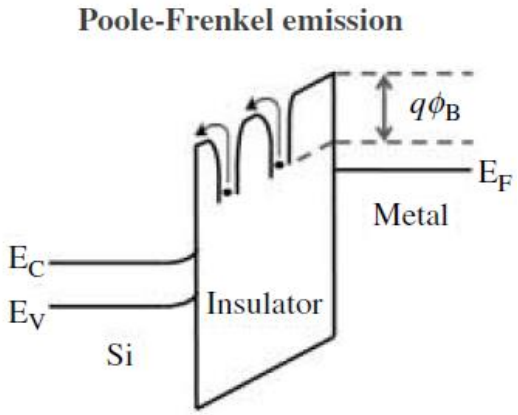


Fig.2.4. Schematic energy band diagram of Frenkel Poole emission [45].

2.4. Overview of Mobility Scattering Mechanisms on high-*k*/$In_xGa_{1-x}As$ MOS Devices

So far, several scattering mechanisms on high-*k*/$In_xGa_{1-x}As$ devices have been observed, and they include mechanisms such as interface roughness [46], interface dipole scattering [47] and remote Coulombic scattering due to charges in the oxide and/or at the interface as well as phonon scattering [48]. These scattering mechanisms would be shown in this section.

2.4.1. Coulombic Scattering and Phonon Scattering

At low E_{eff}, Coulombic scattering dominates and the mobility increases with higher inversion carrier density due to the screening effect. This is observed in $LaAlO_3$/$In_xGa_{1-x}As$ MOSFET [48]. The Coulombic scattering at low inversion charge could be attributed to the net positively charged donor states present at the interface between the $In_xGa_{1-x}As$ channel and the high-*k*/$LaAlO_3$ dielectric. The phonon limited mobility, μ_{Phonon}, dominates across a wide range of carrier density as indicated by the strong temperature dependence, in particular those caused by substrate/bulk phonons. It is proposed that the phonons could originate remotely from the

high-*k* dielectric or could be associated with the polar nature of the $In_xGa_{1-x}As$ semiconductor or an interaction between the two [48-49].

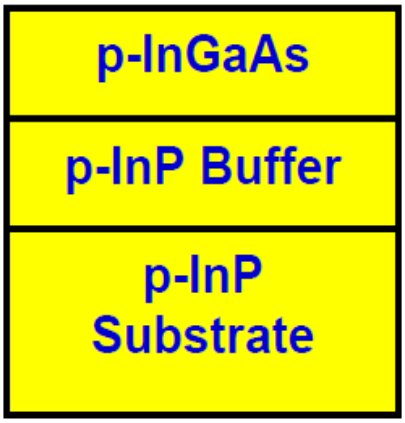
Hence, mobility data in Chapter 5 of this work given in Sections 5.2.2 and 5.2.3 will be analysed in the light of this discussion to identify dominant scattering mechanism and suppression of certain mechanisms due to passivation.

2.4.2. Interface Dipole Scattering

One of the reasons proposed for the improved mobility of ALD Al_2O_3 on $In_xGa_{1-x}As$ (111) A MOSFET compared to $In_xGa_{1-x}As$ (100) A MOSFET is interface dipole scattering based on the fact that μ_{eff} improvements under high E_{eff} is associated with V_{th} shift to the negative direction [47]. The cause of this V_{th} shift is due to the interface dipoles at $Al_2O_3/In_xGa_{1-x}As$ as deduced from the y intercept of V_{fb} vs EOT which indicates a large interface dipole strength for $In_xGa_{1-x}As$ (111) A compared to $In_xGa_{1-x}As$ (100) A.

Hence in our work, we have made use of similar technique to identify the presence of larger interface dipole scattering for non-passivated device compared to passivated device as shown in Fig.5.9 from Section 5.2.3.3.

2.5. Process Flow of $In_{0.53}Ga_{0.47}As$ MOSFETs Fabricated



$In_{0.53}Ga_{0.47}As$ (500nm, Zn doped)

InP buffer (Zn p+)

InP substrate (Zn p+)

Fig.2.5. MBE growth of p-$In_{0.53}Ga_{0.47}As$ on InP with the specifications provided. $In_{0.53}Ga_{0.47}As$ is 500nm thick, lattice matched with InP.

The process flow for device fabrication has been performed on the heterostructure substrate, which has been provided from commercial growth services, given in Fig.2.5. MBE method was used to grow the 2-inch p+ InP substrate (doping level is $3x10^{18}cm^{-3}$), 200nm p-doped (doping level is $1x10^{18}cm^{-3}$) InP buffer and 500nm p-doped $In_{0.53}Ga_{0.47}As$. The dopants used for p-type formation is Zn and doping level has been extracted from the electrochemical capacitance-voltage (ECV) method.

Similar to the fabrication of silicon MOS device, the surface preparation is an important step before growth or deposition of dielectric. The $In_{0.53}Ga_{0.47}As$ surface was first cleaned using 1% dilute HF for 2min to remove the native oxide originating from the surface. HF cleaning for 2min does not significantly attack the surface resulting in surface roughness to only increase slightly, measured from the Atomic Force Microscopy (AFM). Since surface passivation by Chalcogen atoms such as sulphur and selenium has been widely adopted in $In_{0.53}Ga_{0.47}As$ devices for surface passivation,

$(NH_4)_2S$ cleaning has been carried out for 5min at room temperature to prevent oxidation caused by exposure to the ambient. This is followed by 3min de-ionized water rinse, as the standard pre-gate cleaning procedure.

Subsequently, the p-type $In_{0.53}Ga_{0.47}As$ devices needed for plasma-PH_3/N_2 passivation were loaded into the holder of the multichamber chemical vapor deposition system with substrate temperature being maintained at 430°C and they were treated with plasma-PH_3/N_2 treatment for 1min. Thus devices which undergo plasma-PH_3/N_2 passivation treatment is termed as passivated device while devices which do not undergo plasma-PH_3/N_2 passivation treatment is termed as non-passivated device. Without breaking vacuum, both passivated and non-passivated devices then immediately underwent metalorganic CVD (MOCVD) of HfAlO using $[HfAl(MMP)_2(OiPr)_5]$ as precursor, at 450°C and post-deposition anneal at 400°C for 30s in N_2 ambient. It is comprised of 10% Al_2O_3 and 90% HfO_2. The advantage of HfAlO over HfO_2 is that the crystallization temperature is higher for HfAlO, causing it to have better thermal stability than HfO_2 and also easier removal by HF to form the S/D contact opening after a high temperature process. Chapter 3 studies involves 8nm thick high-*k* HfAlO, while Chapter 4-Chapter 5 involves 5nm thick HfAlO. For long channel devices fabricated from both runs, the channel doping concentration of p-type $In_{0.53}Ga_{0.47}As$ is $1x10^{16}cm^{-3}$.

2.5.1. Long Channel MOSFET Fabrication Process

After gate oxide deposition process, device fabrication for the MOSFETs followed the conventional self-aligned process where a 150nm

TaN film was first deposited by sputtering Ta using Ar/N_2 gas as a gate electrode. Next, gate area was defined by Cl_2 based reactive ion etching.

Silicon is then implanted through 10nm of sacrificial SiO_2, deposited using e-beam evaporator, into the $In_{0.53}Ga_{0.47}As$ with dose of $1x10^{14}cm^{-2}$ and energy of 50keV. This is then followed by a 100nm SiO_2 capping layer deposition before sample undergoes various activation conditions, in this case 600°C 1min in N_2 ambient. The RTA system uses a standard setup for 8-inch silicon wafer, and the $In_{0.53}Ga_{0.47}As$ sample is placed on top of a dummy 8-inch silicon wafer where temperature is then monitored by a Pyrometer. After RTA, SiO_2 capping layer is then removed. The implant and annealing condition are chosen since good rectifying junction with forward and reverse current ratio as 6 orders of magnitude can be achieved, with low sheet resistance of the Si implanted region being 65-80Ω/sq and contact resistance determined to be about 600Ω.μm [1].

The ohmic S/D contacts were then made by photolithography and electron beam evaporation of AuGe 50nm/Ni 25nm /Au 50nm alloy. This is then followed by lift off process, using acetone/ultrasonic bath and subsequently IPA and DI rinse. Metal alloying RTA was carried out at 360°C-400°C for 1min in N_2. As a back contact, Ti/Pt/Au alloying was used. Final step involved forming gas anneal (FGA) performed at 10% H_2/90% N_2 concentration at 400°C for 10min. Hence, the process flow for fabrication of $In_{0.53}Ga_{0.47}As$ MOSFET is shown in Fig.2.6.

- MBE grown $In_{0.53}Ga_{0.47}As$
- HF and $(NH_4)_2S$ surface treatment
- Plasma-PH_3/N_2 treatment (optional)
- HfAlO deposition
- In-situ PDA 400°C 30s
- Sputter TaN deposition
- Gate etch and high-*k* etching
- Si implantation ($50keV/1x10^{14}cm^{-2}$)
- S/D activation RTA 600°C 60s
- S/D and back contact formation
- Forming Gas Anneal (FGA) 10% H_2/90% N_2 concentration at 400°C for 10min

Fig.2.6. Process flow of long channel $In_{0.53}Ga_{0.47}As$ N-MOSFET fabrication.

Note that the processes described is for the fabrication of long channel MOSFETs (≥ 2μm devices) fabricated in the form of a ring-shape gate $In_{0.53}Ga_{0.47}As$ MOSFET as shown in Fig.2.7.

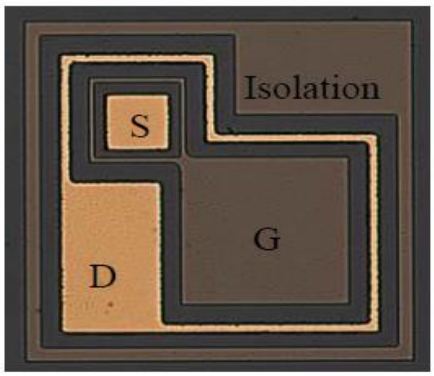


Fig.2.7. Top view of a ring shape $In_{0.53}Ga_{0.47}As$ MOSFET, fabricated using a two-mask step.

This is known as a two-mask transistor process since one mask is for ring-shape gate pattern and device isolation. Another mask is for the source and drain contact pattern. Typical gate lengths fabricated using this process is 2μm-20μm with the width being 200μm-400μm an additional square area of $100x100\mu m^2$ for probing. Fig.2.8 is the schematic of the MOSFET formed using above process and is used for Chapter 3-5 long channel MOSFET studies. However, devices fabricated in Chapter 4-5 does not

include FGA step.

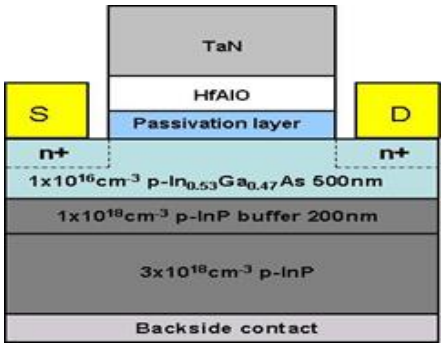


Fig.2.8. Schematic cross section of the self-aligned $In_{0.53}Ga_{0.47}As$ N-MOSFET integrated with CVD HfAlO gate dielectric and TaN metal gate.

2.5.2. Short Channel sub-2µm Channel Length MOSFET Fabrication Process

The process flow to fabricate a sub-2µm scale channel length MOSFET is similar to the self-aligned fabrication process given in Fig.2.6 but several changes are made from the long channel device fabrication. They are highlighted in bold in Fig.2.9, and includes procedures such as Electron Beam Lithography (EBL), Pt hardmask for gate patterning and implant conditions.

- MBE grown $In_{0.53}Ga_{0.47}As$
- HF and $(NH_4)_2S$ surface treatment
- Plasma-PH_3/N_2 treatment (optional)
- HfAlO deposition
- In-situ PDA 400°C 30s
- Sputter TaN deposition
- **Electron beam lithography for gate patterning**
- **Pt deposition and lift-off as RIE hard mask**
- Gate etch and high-*k* etching
- **Si implantation (20keV/1x10^{14}cm^{-2})**
- S/D activation RTA 600°C 60s
- S/D and back contact formation

Fig.2.9. Process flow of sub-2µm short channel $In_{0.53}Ga_{0.47}As$ N-MOSFET fabrication. Words in bold highlight the steps that differ from long channel $In_{0.53}Ga_{0.47}As$ N-MOSFET fabrication process.

Sub-2µm HfAlO $In_{0.53}Ga_{0.47}As$ NMOSFET has been fabrication with plasma-PH_3/N_2 treatment. Pt is used since it is resistive to RIE etching. After drawing the gate using electron beam lithography, Pt is deposited followed by Pt lift-off. This is then followed by positive resist being spin coated onto the wafer before optical lithography step consisting of exposure and development is carried out. Next involves the RIE and ashing process for photoresist removal. Hence, now only gate line region consists of Pt remaining on top of TaN. The SD contact is then formed after implantation and RTA activation using a second masking layer for pattern formation and lift off. Note that the process flow described in this section is used for the device fabrication of sub-2µm devices in Chapter 3 (Section 3.3-3.4), as well as device taken from our group's IEDM 2008 data which is used for TCAD calibration parameters from Chapter 6. In addition, the p-type doping concentration for $In_{0.53}Ga_{0.47}As$ channel fabricated for the short channel devices in this work in Chapter 3 is given by $1x10^{16}cm^{-3}$.

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Chapter 3: Thermal stability and Electrical Performance of plasma-PH_3/N_2 Passivated HfAlO/$In_{0.53}Ga_{0.47}As$ MOSFET

3.1. Introduction and Motivation

Plasma-PH_3/N_2 passivation treatment has been previously shown to result in better $HfO_2/In_{0.53}Ga_{0.47}As$ interfacial properties as well as device transfer characteristics compared to the device without the passivation [1-2]. It is shown from XPS and AFM, based on our previous studies [2-3], that a low pressure plasma-PH_3/N_2 treatment of $In_{0.53}Ga_{0.47}As$ results in a smooth and atomically thin P_xN_y film as the main product, with P-for-As anion exchange layer found beneath the P_xN_y layer in a wide range of process window. This P-for-As exchanged layer together with the P_xN_y layer formation is responsible for the prevention of the evolution of undesired As species such as free As.

However, these studies lack in thermodynamic evaluation. This chapter thus focuses on thermodynamic stability study of the $In_{0.53}Ga_{0.47}As$ MOSFET, which is essential for devices fabricated using gate-first technique. The key issue in demonstrating self-aligned $In_{0.53}Ga_{0.47}As$ MOSFETs is to maintain the electrical quality of the high-*k*/$In_{0.53}Ga_{0.47}As$ interface while achieving high dopant activation in the S/D. Hence, the thermal stability of the $In_{0.53}Ga_{0.47}As$ MOSFETs passivated with plasma-PH_3/N_2 treatment is studied by examining the properties of the high-*k*/$In_{0.53}Ga_{0.47}As$ interface using transmission electron microscopy (TEM), energy dispersion X-ray (EDX), capacitance–voltage (C-V), and charge pumping techniques. It will be shown that plasma-PH_3/N_2 passivation treatment has excellent thermal

stability up to 800°C based on the negligible changes in the equivalent oxide thickness (EOT), D_{it} and subthreshold slope. Despite the increase in gate leakage current density (J_g) by 2 orders of magnitude after 800°C anneal, it is still considerably low compared with the J_g of a non-passivated device which increases by 5 orders of magnitude from before anneal to after 700°C anneal.

In addition to the improvement in thermal stability, plasma-PH_3/N_2 passivated device also showed suppressed D_{it} at the upper half of the bandgap, which is favorable for N-MOSFET operation. Also, electrical results obtained from plasma-PH_3/N_2 passivation treatment, which includes mobility, D_{it}, drive current and J_g, would be benchmarked with other passivation techniques.

3.2. Thermal Stability Analysis of plasma-PH_3/N_2 Passivated $In_{0.53}Ga_{0.47}As$ MOSFET

After completion of device fabrication described in Section 2.5.1, the stability studies involved plasma-PH_3/N_2 passivated and non-passivated $In_{0.53}Ga_{0.47}As$ MOSFETs going through RTA processes at varying temperature steps i.e. 600°C for 1min, 700°C for 1min, and 800°C for 5s (for plasma-PH_3/N_2 passivated device only) to simulate S/D activation temperatures. The electrical results have been obtained on the same set of devices with the devices measured after each temperature anneal. Note that no anneal/before anneal data shown in the figures in this chapter corresponds to device electrical results before the devices undergo FGA and any additional RTA processes after device fabrication.

Inversion C-V curves, which refers to the gate-to-channel capacitance (C_{gc}), obtained using the split C-V measurement technique has been illustrated in Fig.3.1. Split C-V technique based measurements are performed by

grounding the substrate and measuring the capacitance between gate and S/D connected together. The curves measured at 100kHz show sharp transitions from accumulation to inversion after annealing the plasma-PH_3/N_2 passivated MOSFETs until 800°C in Fig.3.1. As seen in the figure, no presence of kinks and C-V stretch out at 800°C anneal can be observed. The EOT shows negligible changes up to 800°C anneal, with EOT~2.7nm before anneal and EOT~2.8nm after 800°C anneal. This shows the robustness of the P_xN_y gate stack and the gate stack/$In_{0.53}Ga_{0.47}As$ heterostructures after RTA, which can be attributed both to the superior thermal [4-7] and chemical stability [2,4,8] of the P_xN_y barrier layer against oxidation caused by the strong P–N bond that can suppress the formation of a defective low-*k* interfacial layer. The thermal stability of P_xN_y is helpful here since its decomposition temperature is higher than 850°C [5-6, 9].

The J_g extracted after each annealing step which are plotted in the inset of Fig.3.1, shows that at 600°C N_2 anneal, there are no significant changes in J_g compared to the result before anneal. However, the leakage current in these devices increased by 2 orders of magnitude after 800°C 5s anneal i.e. from $2x10^{-7}A/cm^2$ for no anneal to $1.95x10^{-5}A/cm^2$ at V_g=1V. Nevertheless, this J_g of ~$1.95x10^{-5}A/cm^2$, is still considerably low compared with the J_g of a non-passivated device, which significantly increases by 5 orders of magnitude from $9.44x10^{-7}A/cm^2$ for no anneal to $5.16x10^{-1}A/cm^2$ at V_g=1V after 700°C 1min anneal. This low electrical gate leakage demonstrates that the HfAlO/P_xN_y gate stack has good thermodynamic stability and integrity even after high temperature anneal.

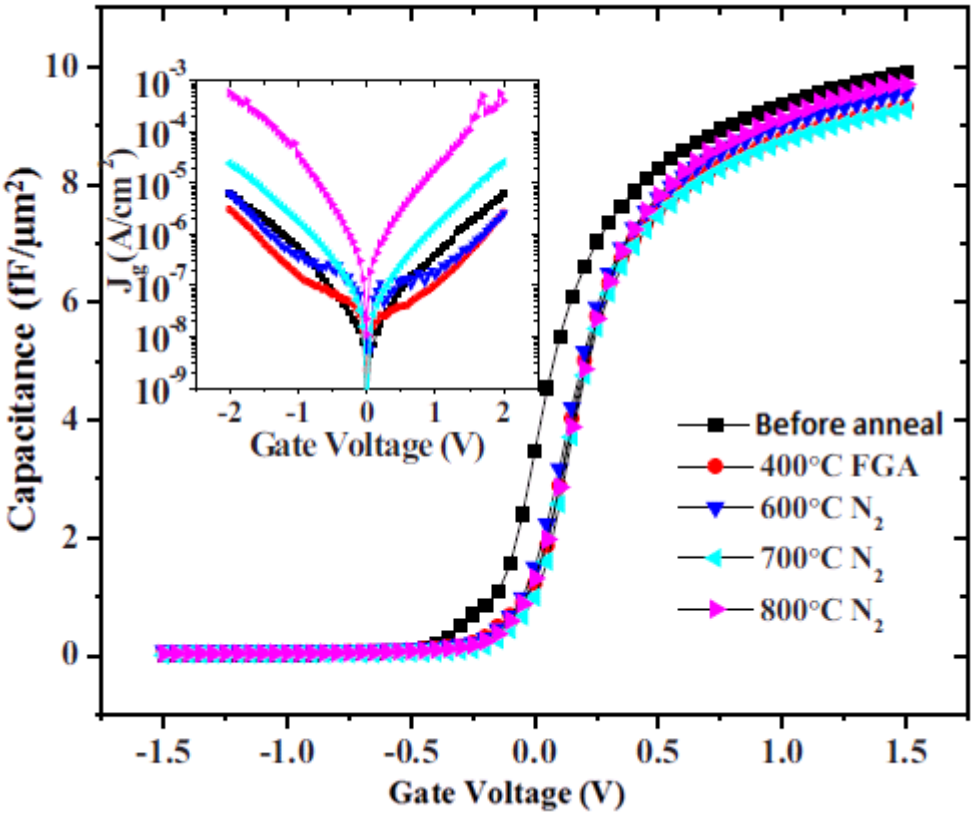

Fig.3.1. C_{gc} curves, generated from split C-V measurement technique, measured at 100kHz of plasma-PH_3/N_2 passivated devices as a function of temperatures at 600°C N_2 1min, 700°C N_2 1min and 800°C N_2 5s. Note the 2 order increase in J_g after high temperature anneal.

Fig.3.2(a) to Fig.3.2(d) shows the TEM images of the HfAlO/P_xN_y/$In_{0.53}Ga_{0.47}As$ gate stack used in above measurements. Alloying the HfO_2 film with Al_2O_3, it is known that the crystallization temperature of HfO_2 film will be increased [10] as seen in Figs.3.2(a)-(d) where the HfAlO remains amorphous up to 800°C anneal. It can be observed that the interface between $In_{0.53}Ga_{0.47}As$ and the passivation layer is smooth until 600°C anneal. However, the sharp transition from the crystalline $In_{0.53}Ga_{0.47}As$ substrate to the P_xN_y layer can no longer be observed at 800°C in Fig.3.2(c) due to the structural changes seen at the localized rough $In_{0.53}Ga_{0.47}As$ interface caused

by the poor thermal stability of $In_{0.53}Ga_{0.47}As$ that starts to show Ga/As out-diffusion at 800°C [11]. The localized rough interface in Fig.3.2(c) and the EDX data (as shown in Fig.3.3(a)) could suggest the migration of Ga/As upward [12]. The interface roughness is found only in localized regions and not seen throughout, as shown in Fig.3.3(b) where the EDX data show no Ga/As outdiffusion. This results in a uniform HfAlO/$In_{0.53}Ga_{0.47}As$ interface seen from the TEM image in Fig.3.2(d)). However, the relatively unchanged C-V curves in Fig.3.1, the consistent D_{it} in Fig.3.4, relatively consistent transconductance in the linear region in Fig.3.5 and consistent subthreshold slope in Fig.3.6 suggest that such roughness is confined to a small region of total width. Nevertheless, the localized interface roughness observed suggests the need to find the optimum condition for the PH_3/N_2 passivation process. The localized thinning of HfAlO and the outdiffusion of Ga/As could be responsible for the increase in J_g for the plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ device due to strong exponential dependence on oxide weak spots. The frequency dispersion ($C_{10kHz\text{-}1MHz}/C_{10kHz}$) and hysteresis (difference in flatband voltage for 100kHz C-V curves obtained from forward and reverse sweeps) in inversion C-V of the plasma-PH_3/N_2 passivated devices are not significantly altered. They are ranging between 2.3% and 2.9% and 48mV and 52mV for frequency dispersion and hysteresis, respectively, with varying annealing temperature before anneal to 800°C.

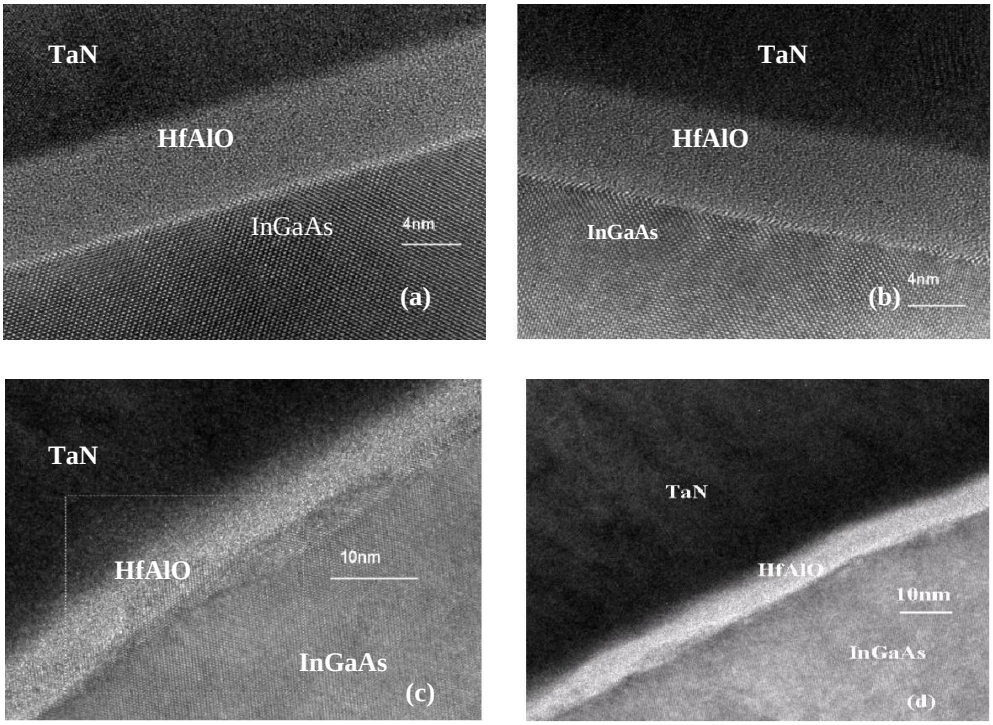

Fig.3.2. TEM images of HfAlO/plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ gate stack with (a) no activation anneal but with FGA 400°C (b) 600°C 1min activation anneal with FGA 400°C and (c) 600°C 1min activation anneal with FGA 400°C followed by 800°C anneal 5s. (d) Same annealing condition as (c) but showing the good even HfAlO layer on even $In_{0.53}Ga_{0.47}As$ surface. Note that oxide thickness measured from TEM is given by ~8nm.

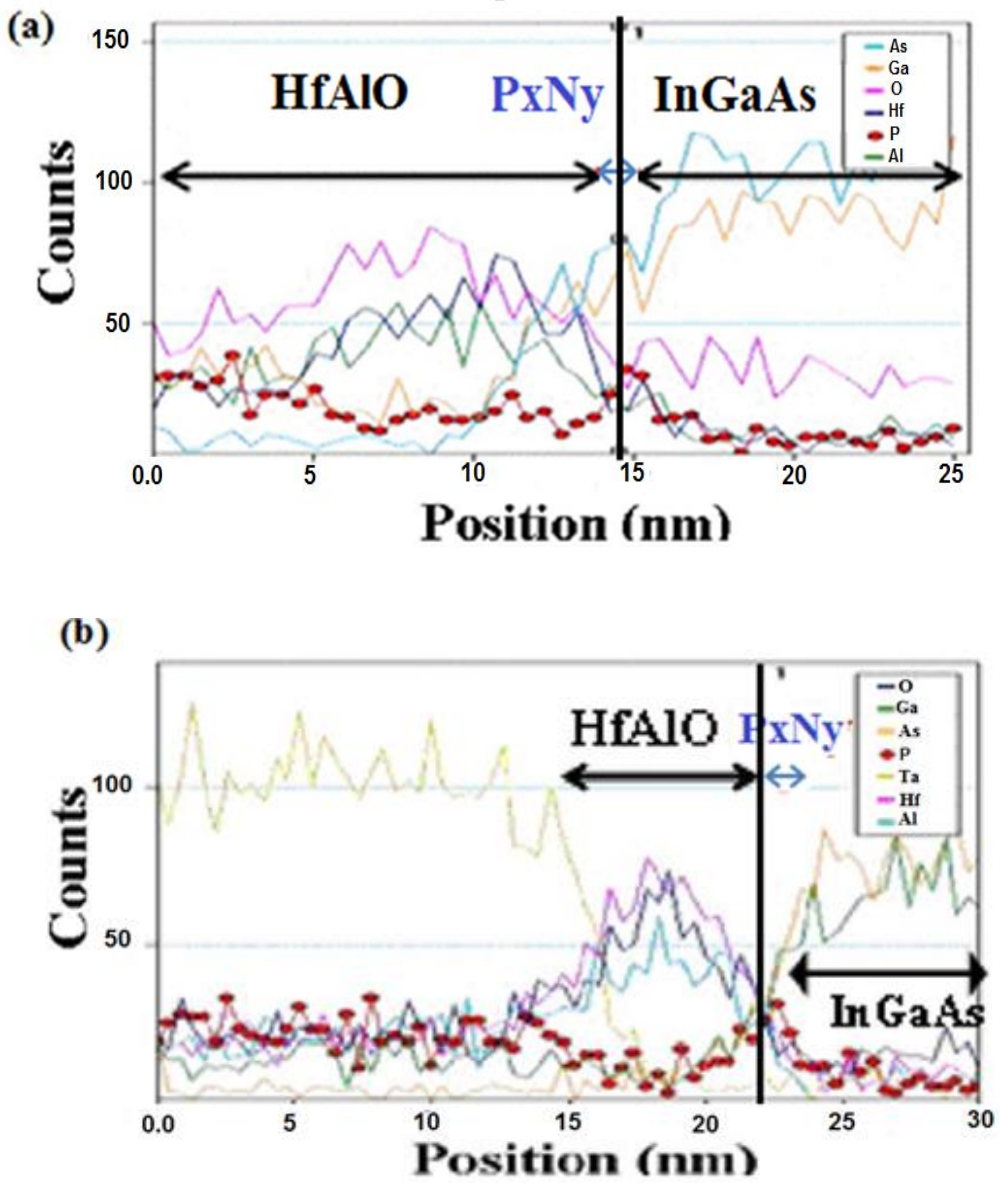

Fig.3.3. EDX results of HfAlO/P_xN_y/$In_{0.53}Ga_{0.47}As$ gate stack with 600°C activation anneal FGA 400°C followed by 800°C anneal at (a) localized rough interface taken from Fig.3.2(c) of TEM image and (b) uniform smooth interface taken from Fig.3.2(d) of TEM image.

The D_{it} at the upper and lower halves of the bandgap of the $In_{0.53}Ga_{0.47}As$ N-MOSFETs is measured using the variable rise/fall time of the charge pumping technique [13-14], with constant amplitude gate pulse at a frequency of 100kHz and gate pulse amplitude of 1.2V. The fall time (rise

time) is varied between 100ns and 1000ns while keeping the rise time (fall time) constant at 100ns to find the electron emission energy level above the midgap (hole emission energy level below the midgap) of the bandgap. In Fig.3.4, the D_{it} above the midgap is smaller than below midgap for plasma-PH_3/N_2 passivated device. This means that either donor-like traps or acceptor-like traps or both in the upper half of the bandgap for passivated device exist in lesser concentration than in lower half of bandgap. Since subthreshold slope alone cannot distinguish between acceptor/donor-like traps, the lower on-current (I_{on}) and lower transconductance can be used to deduce that there is greater acceptor-like traps for non-passivated compared to plasma-PH_3/N_2 passivated N-MOSFET as seen in Fig.3.5. Greater concentration of acceptor-like traps causes larger amounts of electrons being captured by the acceptor-like traps when the Fermi level sweeps to the conduction band minima E_c. Thus, lesser electrons are available for inversion, exhibiting lower on-state currents and increase in V_{th} for non-passivated devices compared to plasma-PH_3/N_2 passivated devices.

The consistency of the mean D_{it} about the midgap between $7.6x10^{12}cm^{-2}eV^{-1}$ at 800°C and $9.7x10^{12}cm^{-2}eV^{-1}$ at 600°C implies good thermal stability of the HfAlO/P_xN_y/$In_{0.53}Ga_{0.47}As$ withstanding RTA up to 800°C. This is also evidenced from the insignificant change in the subthreshold slope (105–120mV/dec) with various annealing conditions, compared to the larger magnitude and greater change in subthreshold slope (210-250mV/dec) with various annealing conditions for the non-passivated device as shown in Fig.3.6. This shows the poorer thermal stability of the HfAlO/$In_{0.53}Ga_{0.47}As$ interface of the non-passivated device. The peak transconductance of the 3μm gate length device plotted in Fig.3.5 shows that

the transconductance for V_d=0.05V at 800°C has slightly improved value due to lesser Coulombic scattering by the interface states, suggesting a slight improvement in the interface quality compared to 600°C, thus agreeing with the subthreshold swing results and the mean D_{it} about the midgap. On the other hand, transconductance for non-passivated device does not improve significantly with increase in annealing temperature, possibly due to worsened interface quality. In addition, the increment observed in the transconductance in V_d=1V region is also probably due to the reduction in oxide thickness deduced from the decrease in EOT after the 800°C anneal, as also observed for the non-passivated device. However, the magnitude of the transconductance is smaller for non-passivated device due to the poorer interface quality.

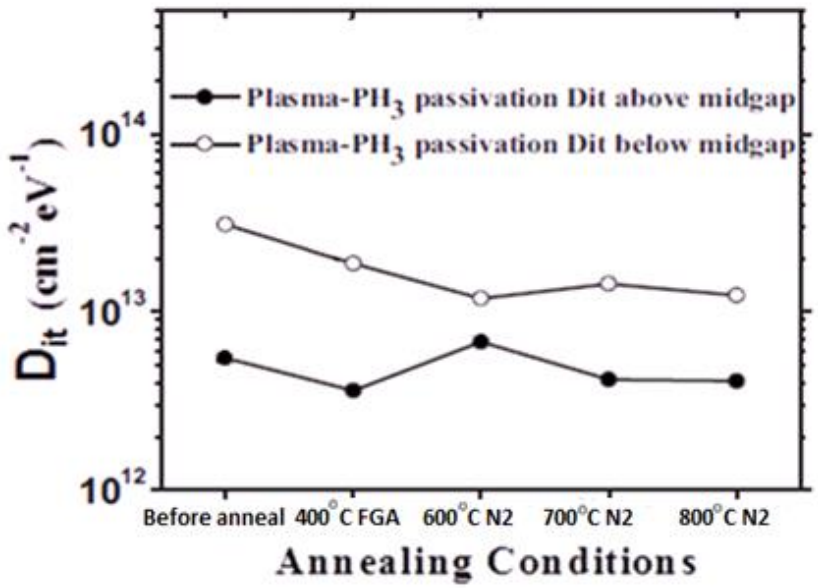

Fig.3.4. Comparison of the D_{it} of plasma-PH_3/N_2 passivated devices which have undergone annealing conditions at 600°C N_2 1min, 700°C N_2 1min and 800°C N_2 5s.

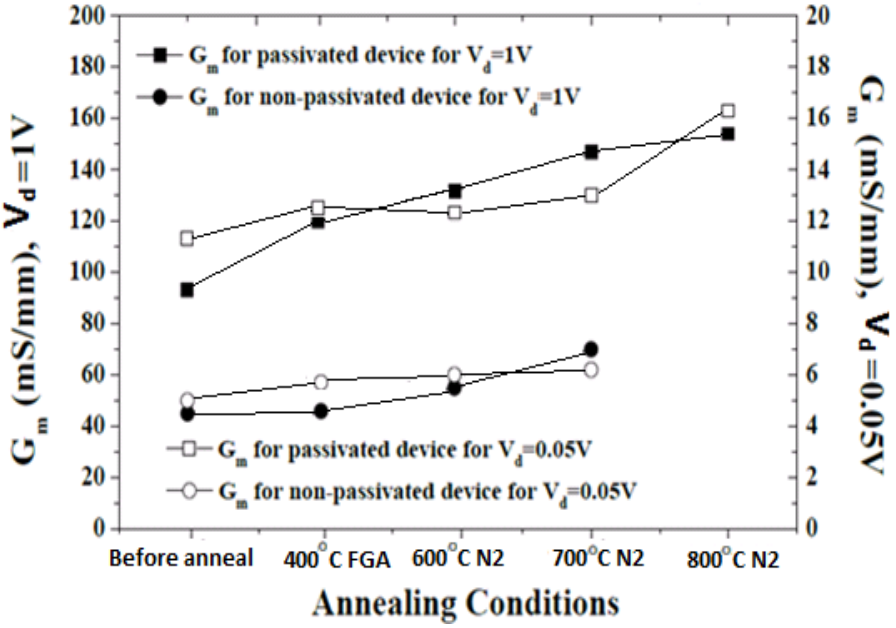

Fig.3.5. Maximum transconductance (G_m) which is normalized with gate width of 65µm, for plasma-PH_3/N_2 passivated and non-passivated devices, which have undergone annealing conditions at 600°C N_2 1min, 700°C N_2 1min and 800°C N_2 5s (only for plasma-PH_3/N_2 passivated devices).

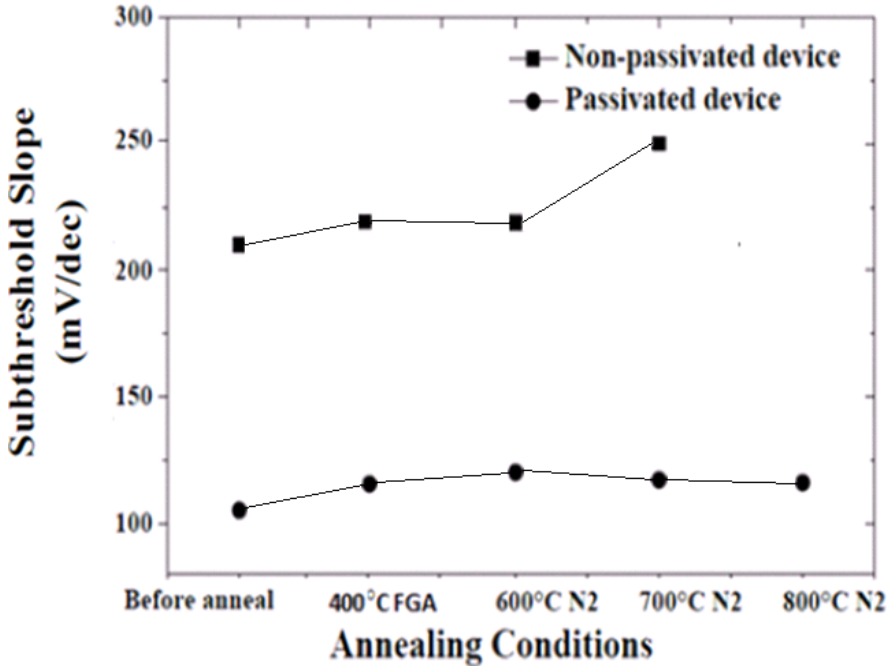

Fig.3.6. Subthreshold slope taken at V_d=0.05V which is normalized with gate width of 65µm, for plasma-PH_3/N_2 passivated and non-passivated devices, which have undergone annealing conditions at 600°C N_2 1min, 700°C N_2 1min and 800°C N_2 5s (only for plasma-PH_3/N_2 passivated devices).

3.3. Electrical characterization of plasma-PH_3/N_2 Passivated HfAlO/$In_{0.53}Ga_{0.47}As$ MOSFET

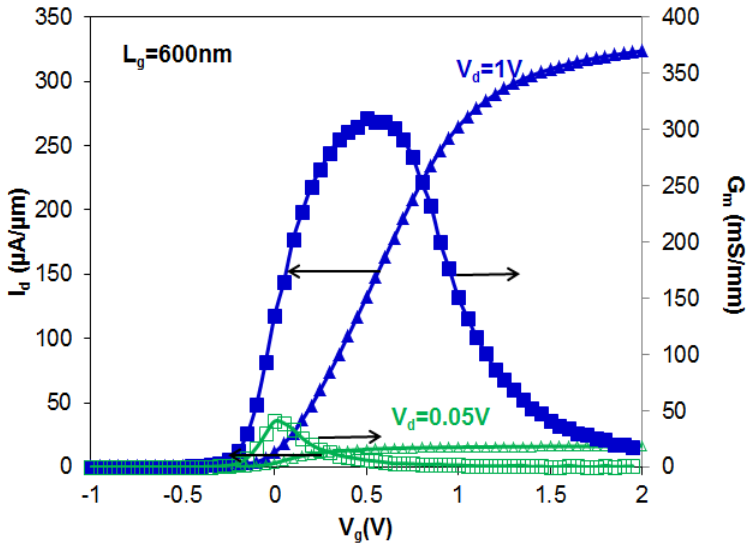

Fig.3.7. I_d-V_g characteristics of the P_xN_y-passivated TaN/HfAlO/$In_{0.53}Ga_{0.47}As$ MOSFET with L_g=600nm, showing maximum G_m of 310mS/mm.

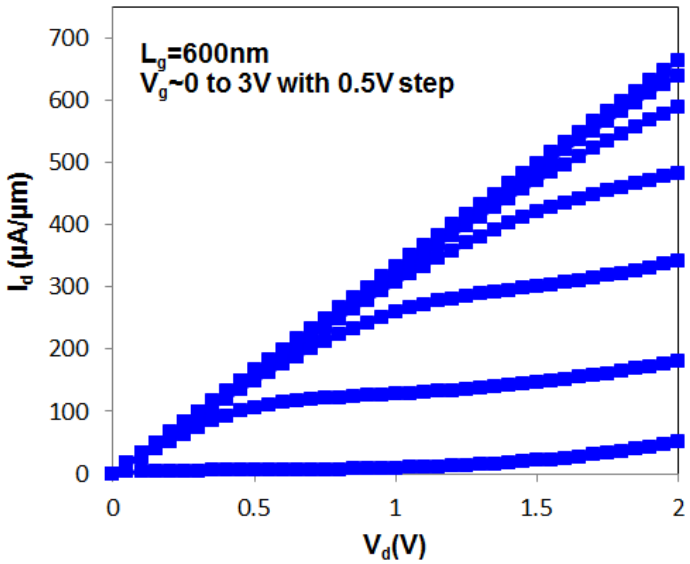

Fig.3.8. I_d-V_d of 600nm gate length $In_{0.53}Ga_{0.47}As$ MOSFET with plasma-PH_3/N_2 passivation.

Fig.3.7 shows the I_d-V_g characteristics of $In_{0.53}Ga_{0.47}As/P_xN_y$/HfAlO MOSFET with L_g=0.6μm at V_d=1 and V_d=0.05 V for device without FGA and additional RTA processes after device fabrication. The HfAlO has physical thickness of 8nm. SS at V_d=1V is 221mV/dec with DIBL given by

139mV/V. A high peak transconductance, G_m of 310 mS/mm was recorded at V_d=1V with drive current at V_g=2V, V_d=1V being given as 324µA/µm. The I_d-V_d characteristics are shown in Fig.3.8. Gate voltage is from 0V to 3V in 0.5V step. The drain bias ranges from 0 to 2V. Slight SCE is observed due to channel doping concentration being lightly doped at p-type $1x10^{16}cm^{-3}$. It is clearly seen that when V_g > 2V, the MOSFET current is very close to each other for increasing V_g. This means the limiting factor for further current/transconductance increase is mainly the series resistance. Maximum current for this device is 664µA/µm at gate and drain bias of 3V and 2 V respectively.

3.4. Benchmarking of $In_{0.53}Ga_{0.47}As$ MOSFETs

3.4.1. Mobility benchmark for high-*k*/$In_{0.53}Ga_{0.47}As$ Interface

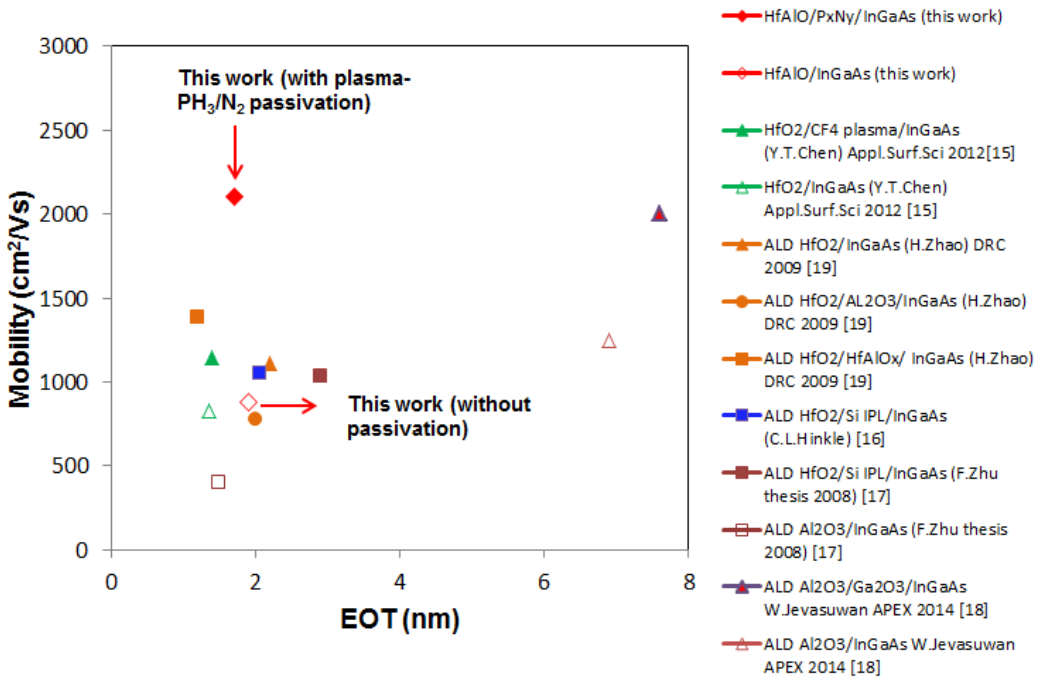

Fig.3.9. Mobility benchmarking with various passivation techniques including this work.

The mobility value obtained for this work has been benchmarked against several passivation techniques which include CF_4 plasma [15], Si [16-17], Ga_2O_3 [18] and HfO_2/HfAlO bi-layer gate stack [19] shown in Fig.3.9. Mobility obtained for this work is similar to the best reported surface-channel mobility, and highest compared to the rest for an aggressively scaled EOT. This is attributed to better passivation and the smaller channel doping concentration of $1x10^{16}cm^{-3}$ for this work, while the rest corresponds to larger channel doping concentration of $3x10^{16}cm^{-3}$ [18], $5x10^{16}cm^{-3}$ [15], $1x10^{17}cm^{-3}$ [16], $3x10^{17}cm^{-3}$ [17]. In addition, mobility benchmarking shows that passivation layers or bi-layer gate oxide would result in larger mobility due to reduced trap density.

3.4.2. D_{it} benchmark for high-*k*/$In_{0.53}Ga_{0.47}As$ Interface

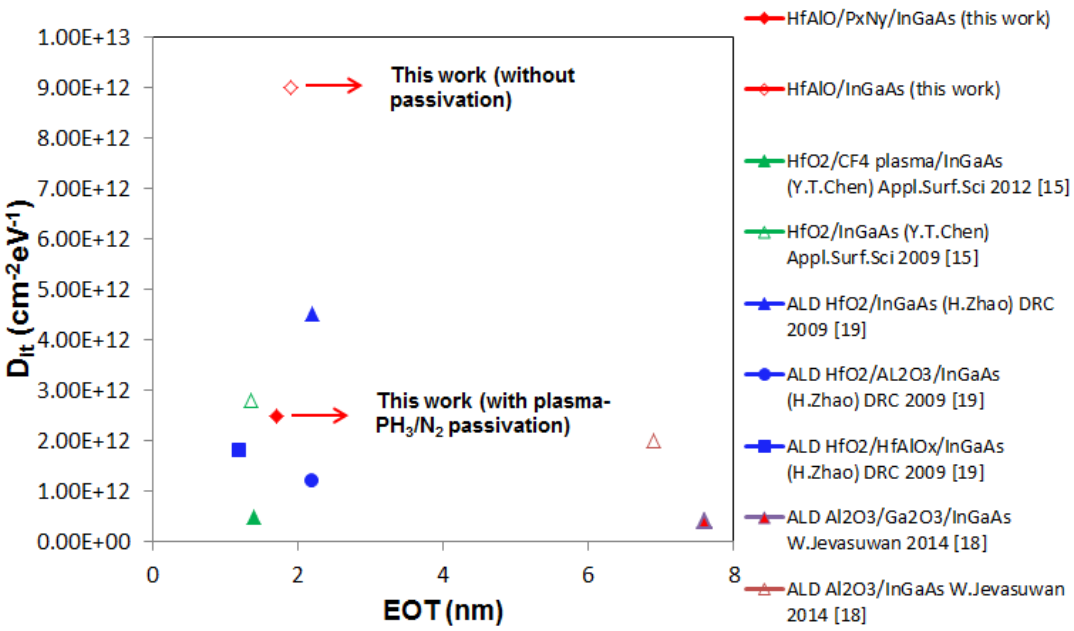

Fig.3.10. D_{it} (taken at $E-E_i=0.25eV$) as a function of EOT for devices with different passivation or bi-layer gate oxide.

The benchmark of D_{it} taken at trap energy levels of 0.25eV away from intrinsic Fermi level vs EOT, depicted in Fig.3.10, shows that for all references including this work, bi-layer gate oxide or gate oxide with interfacial layers are needed for reduced D_{it} required for device enhancement. Energy levels close to the conduction band is taken for comparison because mobility and hence device performance in on-state is mainly attributed to D_{it} in this range [21-22]. In addition, figure shows that even at scaled EOT of 1.7nm, small D_{it} in the low $2.5x10^{12}cm^{-2}eV^{-1}$ is achievable in our work, which is comparable to those best few reported in literature. Ref [15] and Ref [19] both gives lower D_{it} compared to this work due to gate last process being adopted for their work, in order to protect gate stack from S/D annealing. Note that for Ref [18], the D_{it} is significantly smaller but yet in the mobility results, it is comparable to that obtained as this work. This is likely due to the D_{it} measured taken from MOSCAP instead of MOSFET, which excludes the effect from the high temperature S/D annealing thus underestimating the D_{it}. This implies the concept of plasma-PH_3/N_2 is appealing for future gate-first self-aligned $In_{0.53}Ga_{0.47}As$ MOS device due to its D_{it} being of comparable values to that of gate-last processes.

3.4.3. $I_{d,sat}$ benchmark for high-*k*/$In_{0.53}Ga_{0.47}As$ Interface

$I_{d,sat}$ for comparison has been taken at gate overdrive of V_g-$V_{t,sat}$=1.5V, V_d=1V to remove the effects of SCE for fair benchmarking as shown in Fig.3.11. The drain current achieved in our self-aligned gate-first 3µm plasma-PH_3/N_2 passivated HfAlO/$In_{0.53}Ga_{0.47}As$ MOSFET is higher than that of a 1µm ALD Al_2O_3/$In_{0.53}Ga_{0.47}As$ MOSFET from Ref [23]. This is due to the smaller channel doping concentration used in our work given by

$1x10^{16}cm^{-3}$ compared to $5x10^{16}cm^{-3}$ used in Ref [23]. In addition, the 0.8μm and 0.6μm plasma-PH_3/N_2 passivated devices fabricated in this work also both show larger $I_{d,sat}$ than the 0.5μm device fabricated in Ref [25], which makes use of gate-last process in Ref [25]. The fact that this work shows comparable results with gate last ALD-Al_2O_3 process further confirms the good thermal stability of device fabricated with plasma-PH_3/N_2 passivation technique.

On the other hand, it is observed that gate first self-aligned process using in-situ ultrahigh vacuum MBE deposition technique to deposit the Al_2O_3/GGO i.e. Ga_2O_3 (Gd_2O_3) in Ref [23] gives larger $I_{d,sat}$ than ALD deposited $Al_2O_3/In_{0.53}Ga_{0.47}As$ [23] and also our work. This is due to the clean GGO/$In_{0.53}Ga_{0.47}As$ interface, free of In_2O_3, In $(OH)_3$, and Ga_2O_3 but still observed in the ALD approach [28-29]. For our work, as will be mentioned in Section 5.2.3.3, due to their smaller binding energy separation between the peaks and the XPS lines of Ga3d and In4d being strongly overlapped with Hf4f (since our gate dielectric is HfAlO), it is difficult to deconvolute the peaks from oxides of Ga and In. However, as shown in Fig.5.9, we compare the change in Ga/In ratio using angle-resolved XPS (ARXPS), with respect to with and without RTP to deduce the passivation effect on the chemical composition disturbance at the oxide/$In_{0.53}Ga_{0.47}As$ interface. Although we could not indicate what species were formed exactly at the HfAlO/$In_{0.53}Ga_{0.47}As$ interface, we found that the chemical disturbance in relative Ga/In ratios of $In_{0.53}Ga_{0.47}As$ by the RTP is still present, though significantly reduced at the interface with the plasma-PH_3/N_2 passivation. Therefore this disturbance of the Ga/In ratio, which signifies a chemical reaction occurring at the HfAlO/$In_{0.53}Ga_{0.47}As$ interface, explains the reason

why our plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ MOSFET has lower $I_{d,sat}$ than that of MBE $Al_2O_3/In_{0.53}Ga_{0.47}As$ in Ref [23].

Therefore, this benchmarking shows that the method of gate oxide deposition is critical to realize higher $I_{d,sat}$ by engineering the high-k/$In_{0.53}Ga_{0.47}As$ interface to remove further interfacial reactions.

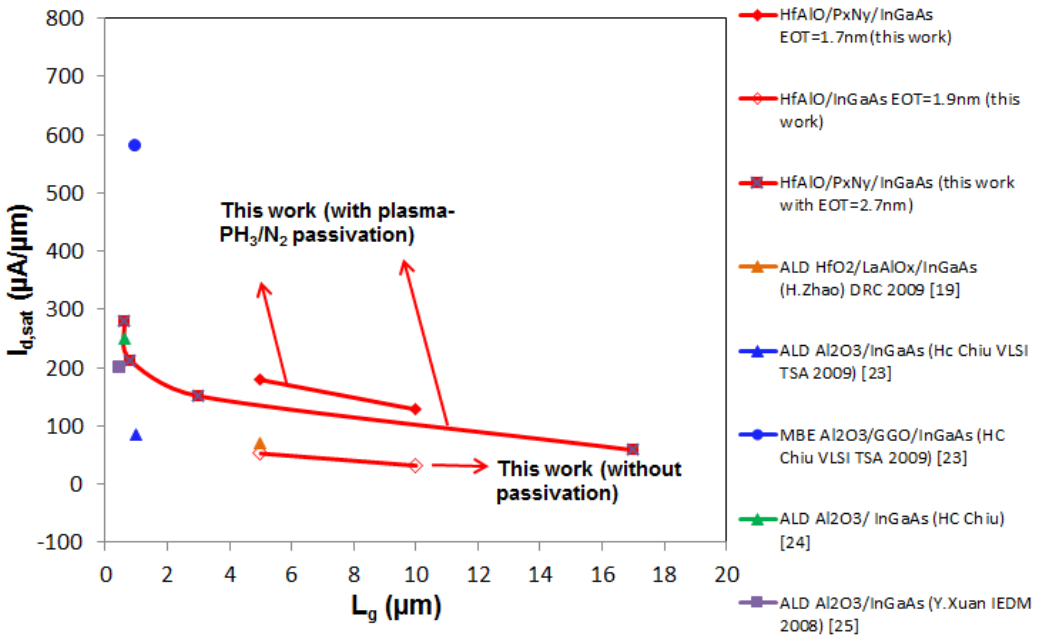

Fig.3.11. Summary of drain current of representative work on $In_{0.53}Ga_{0.47}As$ MOSFETs, taken at V_d=1V, V_g–$V_{t,sat}$=1.5V.

3.4.4. J_g benchmark for high-k/$In_{0.53}Ga_{0.47}As$ Interface

Fig.3.12 shows that P_xN_y passivated gate stack with 5nm thick HfAlO exhibits good gate leakage behaviour at EOT of sub-2nm while non-passivated gate stack exhibits about one-order of magnitude larger gate leakage at the same oxide thickness. Gate leakage density compared with works from different gate stacks shows comparable J_g implying good scalability of passivated gate stack.

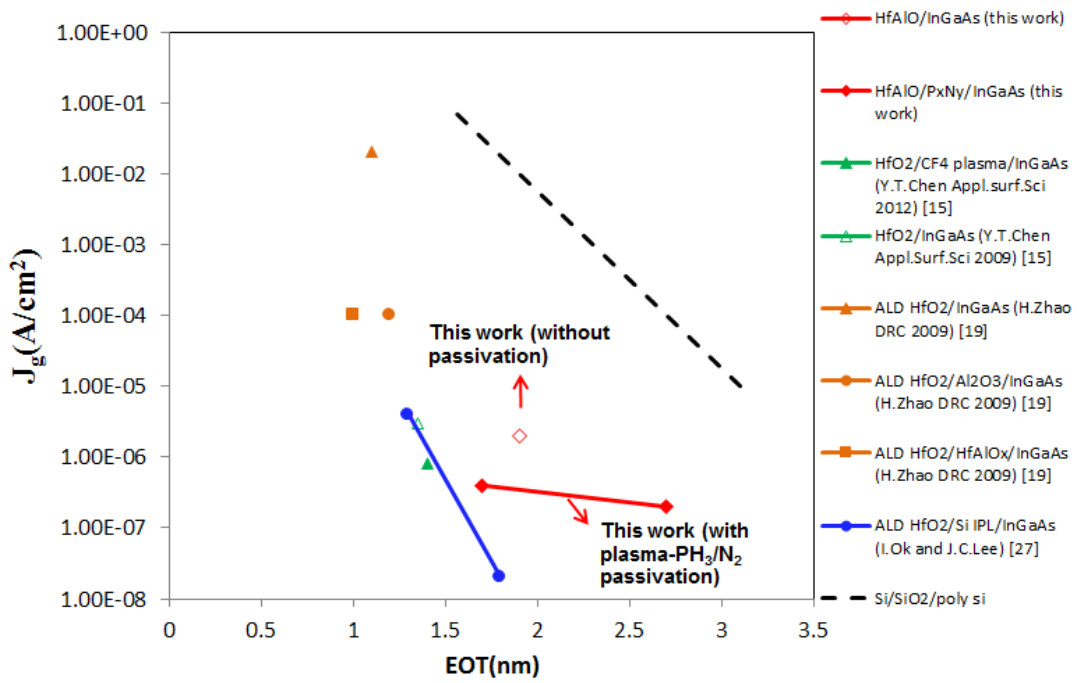

Fig.3.12. Benchmarking of gate leakage current density, J_g, at V_{fb}+1V for MOSFETs for this work and other passivation techniques from literature.

3.5. Conclusion

In summary, a new technique to electrically passivate the interface of $In_{0.53}Ga_{0.47}As$ using plasma-PH_3/N_2 passivation treatment prior to dielectric deposition has been used to improve CMOS performance. The thermal stability of the plasma-PH_3/N_2 passivated HfAlO/$In_{0.53}Ga_{0.47}As$ gate stack up to 800°C 5s anneal has been studied and is found to have good thermal stability as proven from the negligible changes in the EOT, frequency dispersion, hysteresis and D_{it}. However, a 2 order of magnitude increase in J_g exists at 1V with J_g being $1.95x10^{-5}A/cm^2$ after 800°C anneal compared to $2x10^{-7}A/cm^2$ before anneal. This can be attributed to the localized thinning of the gate dielectric and the rough interface caused by the out-diffusion of Ga/As, as observed by TEM images. However, 5 order magnitude of increment in J_g is observed for non-passivated device at V_g=1V, implying its

worse thermal stability than passivated device. D_{it} measurement by the charge-pumping method and SS results revealed consistent values with increase in temperature for plasma-PH_3/N_2 passivated devices, implying good thermal stability. Device characteristics of L_g=600nm for $HfAlO/P_xN_y/In_{0.53}Ga_{0.47}As$ MOSFET has been reported, in addition to benchmarking of D_{it}, mobility, $I_{d,sat}$ and J_g with respect to other passivation techniques.

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Chapter 4: Leakage Current and Carrier Transport Mechanisms of plasma-PH_3/N_2 Passivated HfAlO/ $In_{0.53}Ga_{0.47}As$ MOSFET

4.1. Introduction and Motivation

From the previous chapter, we have studied the thermal stability performance of the HfAlO/$In_{0.53}Ga_{0.47}As$ MOSFET and shown the improvements made in the device characteristics with plasma-PH_3/N_2 passivation treatment. However, understanding of how this treatment is effective in improving the device performance in terms of the various mechanisms such as gate leakage, off-state leakage and carrier transport mechanism have yet to be investigated systematically. Detailed knowledge of gate leakage and carrier transport can give insight to defects that are present in the high-*k* oxide or at the high-*k*/$In_{0.53}Ga_{0.47}As$ interface, and thus allows targeted improvement to be made to the gate stack.

The aim of this chapter is to investigate the physical origins of the gate leakage improvement and improvement in off-state leakage and carrier-transport mechanism in the subthreshold and on-state of plasma-PH_3/N_2 passivated TaN/HfAlO/$In_{0.53}Ga_{0.47}As$ MOSFETs compared to non-passivated TaN/HfAlO/$In_{0.53}Ga_{0.47}As$ MOSFETs, for temperatures between 250K and 420K. This is needed in order to investigate material parameters such as activation energy of the traps and average bulk trap concentration as well as distinguish the conduction mechanisms that contribute to the conduction current through the dielectric film. Note that Chapter 4 and Chapter 5 have results taken from the same device samples. Hence, discussions on them are inter-related.

4.2. Carrier Transport and Leakage Mechanism of $In_{0.53}Ga_{0.47}As$ MOSFETs

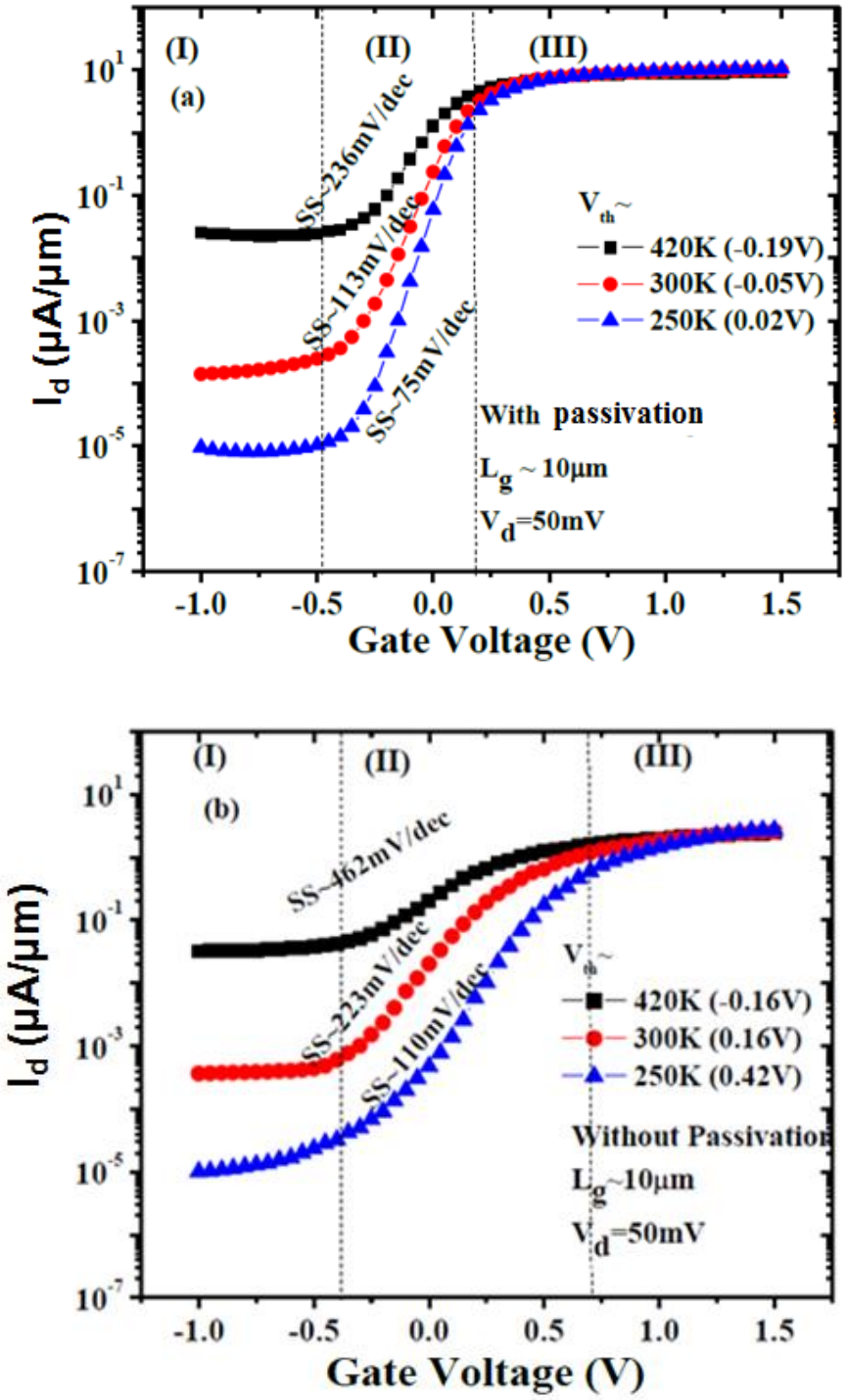

Fig.4.1. I_d-V_g characteristics of (a) plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ N-MOSFET as a function of temperature. Ideal V_{th} at 300 K is -0.098 V and (b) non-passivated $In_{0.53}Ga_{0.47}As$ N-MOSFET as a function of temperature. Ideal V_{th} at 300 K is -0.096 V.

4.2.1. Carrier Transport and Off-state Leakage Mechanism

In this chapter as well as Chapter 5, after completion of device fabrication, gate leakage and I_d-V_g measurements between 250K and 420K have been performed on the devices to carry out the temperature dependence studies. The temperature dependent drain current vs gate voltage (I_d-V_g) characteristics of the device with varying temperature from 250K to 420K have been plotted out as shown in Fig.4.1(a) and 4.1(b). The temperature dependence of the transfer characteristics is a strong function of gate bias, indicating onset of various conduction mechanisms.

Figs.4.1(a)-(b) are divided into three regions. Region (I) will be used to explain the I_{off} contributors in the passivated and non-passivated MOSFETs. Region (II) which corresponds to the subthreshold characteristics will be used to analyse the impact of D_{it} present at the high-*k* dielectric/$In_{0.53}Ga_{0.47}As$ interface of passivated and non-passivated $In_{0.53}Ga_{0.47}As$ N-MOSFETs. Finally Region (III) will be used to explain the carrier transport mechanism for both non-passivated and passivated devices.

The I_{off} contributors in the N-MOSFETs shown from Region (I) in Figs.4.1(a)-(b) have been evaluated as shown in Fig.4.2. The reverse biased drain-substrate p-n junction current, $I_{bulk,}$ is the significant contributor to I_{off} for both passivated and non-passivated devices. This reverse biased junction leakage current is a summation of the diffusion current, generation current and band-to-band tunnelling current [1].

To understand the mechanism of this reverse biased p-n junction leakage which is strongly dependent on temperature, the readings taken at V_g=-0.7V within Region (I) of Figs.4.1(a)-(b), have been plotted as I_{bulk} in the Arrhenius plot of the I_{off} shown in Fig.4.3. Only temperatures between 250K

and 300K were investigated for this analysis in order to prevent I_g from dominating I_{off}. This figure reveals a thermionic component with an activation energy barrier E_a of 0.4eV for non-passivated and 0.38eV for passivated N-MOSFETs, which is consistent with half the bandgap $E_g/2$ of $In_{0.53}Ga_{0.47}As$. This strong temperature dependence indicates that band–to-band tunneling (BTBT) component is negligible here. This E_a being equal to $E_g/2$ indicates that the main contribution to the temperature dependence of leakage floor is attributed to Shockley Read Hall generation-recombination which is proportional to $\exp(-E_g/2kT)$, where E_g is the bandgap, k is the Boltzmann constant and T is temperature.

SRH generation-recombination mechanism relies on the presence of deep levels in the depletion region. It occurs when an electron trapped in a deep level, gains energy, and climbs out of the Coulombic well. Hence, this means that the junction leakage could come from the bulk defects caused by the elements from the relatively volatile V group which is dependent on the activation and implant condition. This is found to be the limitations of implanted S/D $In_{0.53}Ga_{0.47}As$ long channel MOSFETs observed by other groups as well [2-3]. Hence, optimization has to be carried out on the implant condition and activation anneal in order to further reduce the reverse biased drain-substrate leakage but this component still has leakage floor contributions. Thus, it is beneficial to study on non-implanted S/D $In_{0.53}Ga_{0.47}As$ MOSFET such as epitaxially grown S/D $In_{0.53}Ga_{0.47}As$ MOSFET or Implant Free MOSFET structures.

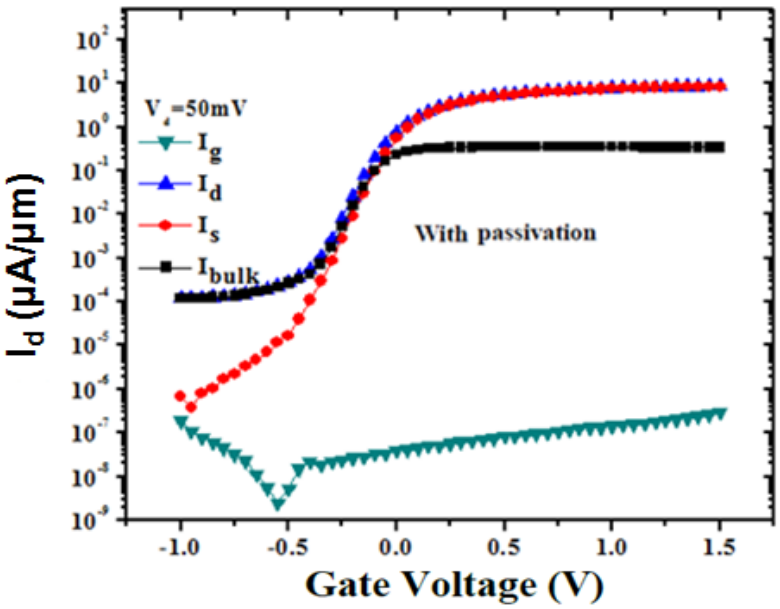

Fig.4.2. Four-terminal I_d-V_g measurements on plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ N-MOSFET showing I_{off} dominated by I_{bulk}, known as reverse biased drain-substrate junction leakage.

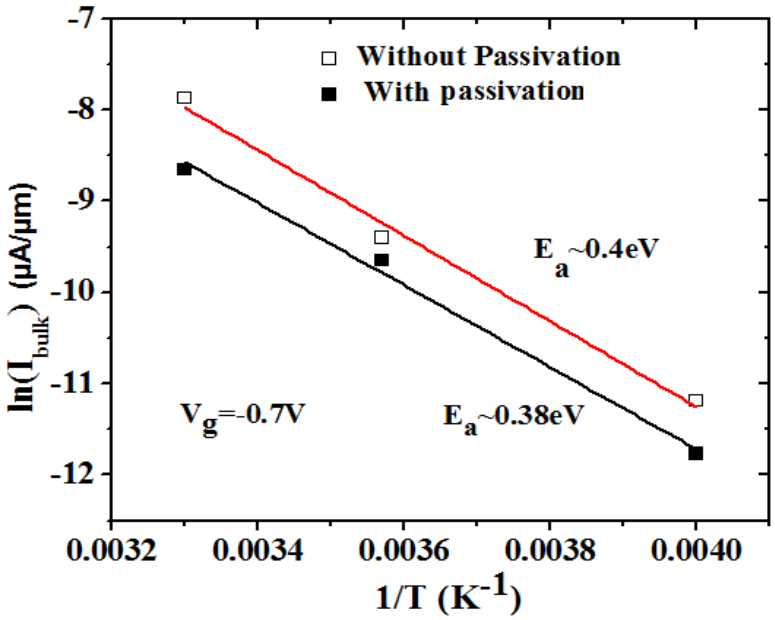

Fig.4.3. Temperature dependence of substrate current (I_{bulk}) of both plasma-PH_3/N_2 passivated and non-passivated $In_{0.53}Ga_{0.47}As$ N-MOSFET taken from temperatures between 300K to 250K. The I_{bulk} values have been taken at I_{off} values at V_g=-0.7V from Fig.4.1(a) and 4.1(b). An activation energy of $E_g/2$ extracted in Region (I) confirms SRH generation-recombination current.

The impact of D_{it} present at the high-*k* dielectric/$In_{0.53}Ga_{0.47}As$ interface on the subthreshold characteristics [Region (II)] from Figs.4.1(a)-(b), of passivated and non-passivated $In_{0.53}Ga_{0.47}As$ N-MOSFETs will be analysed here. It is seen that the average SS increases from 75mV/dec to 236mV/dec for plasma-PH_3/N_2 passivated device, while it increases from 110mV/dec to 462mV/dec for non-passivated device as temperature increases. The expression for the SS is given by $SS=[2.3kT/q]*[1+(C_d+C_{it})/C_{ox}]$ where C_{ox} is the oxide capacitance and C_d is the semiconductor depletion layer capacitance and C_{it} is the capacitance due to interface states. The D_{it} (taken from C_{it}/q) obtained from experimental SS for 300K is around $4.3x10^{12}cm^{-2}eV^{-1}$ for plasma-PH_3/N_2 passivated device and $1.5x10^{13}cm^{-2}eV^{-1}$ for non-passivated device. This means that plasma-PH_3/N_2 is also effective in improving the midgap D_{it} as seen from the improvements in SS. In addition, from Fig.4.1(a), the V_{th} shift w.r.t. ideal V_{th} is not as significant compared to the V_{th} shift w.r.t. ideal V_{th} of the non-passivated device shown in Fig.4.1(b). This means that the passivated device consists of smaller amounts of acceptor-like traps within the bandgap, while non-passivated device consists of higher concentration of acceptor-like traps which increases the V_{th} due to negative charging of these acceptor states [4].

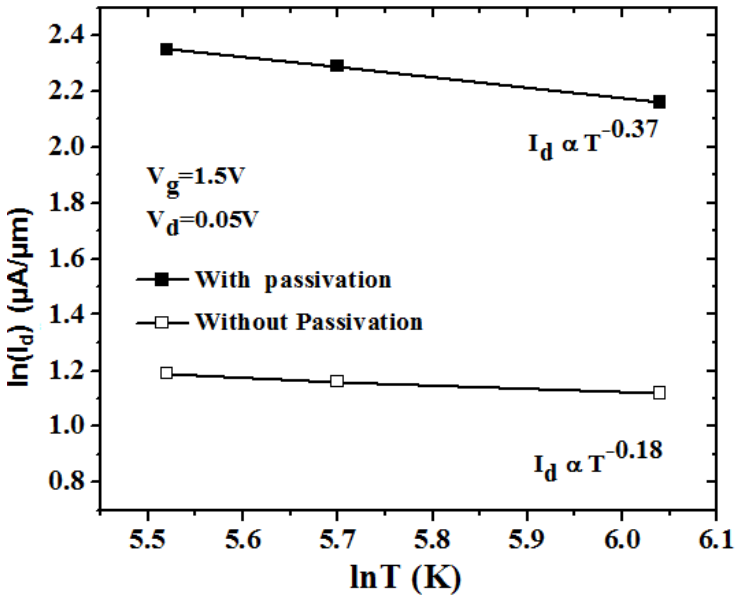

Fig.4.4. ln|I_d| vs ln|T| plot of both plasma-PH_3/N_2 passivated and non-passivated $In_{0.53}Ga_{0.47}As$ N-MOSFET showing a negative temperature dependence of the on-current.

In Region (III) of Figs.4.1(a)-4.1(b), I_{on} is seen to be larger in the passivated than non-passivated device caused by the lesser contribution from acceptor-like traps in the upper half of the bandgap which causing lesser amount of negative trapped charges to be built in when E_F sweeps to the E_c [5] This further confirms the larger concentration of acceptor-like traps in non-passivated device compared to passivated device.

In addition, discussing the carrier transport mechanism of the non-passivated and plasma-PH_3/N_2 passvated device, it is observed that I_d increases as temperature decreases for both passivated and non-passivated device, with I_d having temperature dependence of $T^{-0.37}$ for passivated device, which is stronger than that of non-passivated device having temperature dependence given by $T^{-0.18}$ as shown in Fig.4.4. The weaker temperature dependence for non-passivated device implies its mobility degradation mechanism is being dominated by interface dipole or surface roughness

scattering. The fact that there is non-uniformity or waviness in the HfAlO/$In_{0.53}Ga_{0.47}As$ interface as seen from transmission electron microscopy (TEM) image for non-passivated device as shown in Fig.4.5(a) in comparison to the more abrupt interface for passivated device as seen in Fig.4.5(b) implies that the effects of surface roughness scattering on the mobility at high electric field as observed for non-passivated device should not be dismissed.

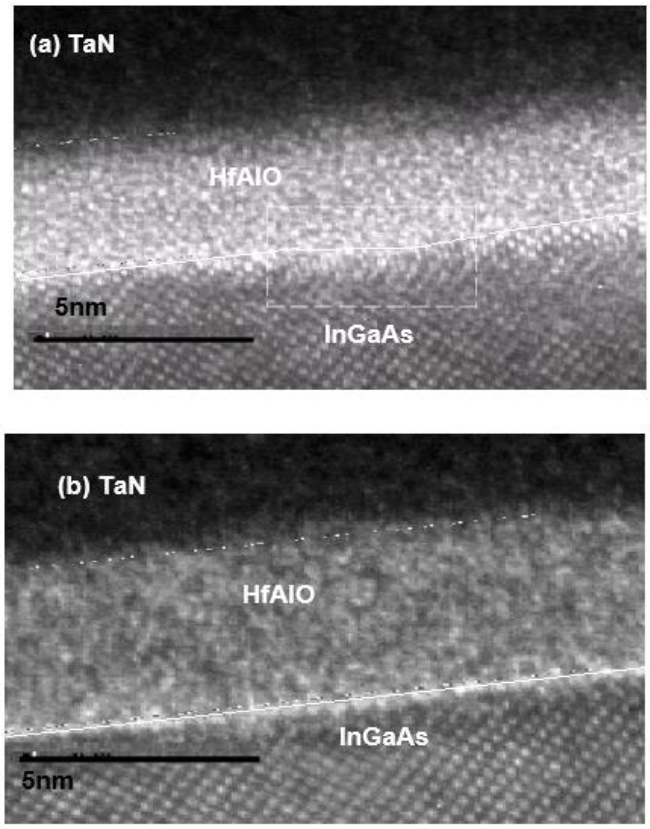

Fig.4.5 (a) HR-TEM image of non-passivated N-MOSFET and (b) HR-TEM image of plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ N-MOSFET.

4.2.2. Gate-leakage mechanism

4.2.2.1. J_g-V_g Characteristics at 300 K

Fig.4.6 illustrates the J_g of non-passivated and passivated HfAlO/$In_{0.53}Ga_{0.47}As$ N-MOSFETs described as a function of applied gate voltage (V_g) in the substrate injection region at 300K. It is seen that passivated device has lower J_g in the inversion region of N-MOSFET compared to non-passivated device, especially in the V_g region greater than 1V. This could be due to the lower interface states and bulk traps in the oxides of the passivated devices. It is seen from intercept of the EOT vs physical oxide thickness shown in Fig.4.7 and high-resolution TEM (HR-TEM) images of non-passivated and passivated device as shown in Fig.4.5(a) and 4.5(b) respectively that the interfacial layer is thicker (~0.6nm) in passivated than non-passivated (~0.35nm) device. However, the thicker interfacial layer of passivated device compared to non-passivated device is believed to be contributed mostly by the passivation layer which consists of P_xN_y and P-for-As exchange layer [6]. On the other hand non-passivated device interfacial layer is made up of the interdiffusion of elemental In/Ga across the high-*k*/$In_{0.53}Ga_{0.47}As$ interface and thus has low *k* values. Hence, this also explains the larger EOT of 1.9nm for non-passivated compared to 1.7nm for passivated device despite the thicker interfacial layer of passivated device.

The inset of Fig.4.6, which shows the $\ln|J_g|$ vs $\ln|E|$ plots for the two types of device at positive gate bias and where E is the Electric field applied, are investigated to analyze the conduction mechanism at 300 K. In low electric field region (in the Ohmic regime i.e. $V < V_{TR}$), J_g-V_g characteristics followed the Ohm's law where both passivated and non-passivated devices

show similar trends in leakage current i.e. $J \propto V^{s}$, where s refers to the slope of the graph. The curves are linear with s~1 indicating an Ohmic behaviour, with non-passivated device having s~0.92 while passivated device has s~0.76. Ohm's law implies that the density of thermally generated free carriers inside the films is larger than the injected carriers due to the carrier transit time (τ_c) being larger than the dielectric relaxation time (τ_d). Clearly, this mechanism dominates behaviour of passivated devices throughout at room temperature.

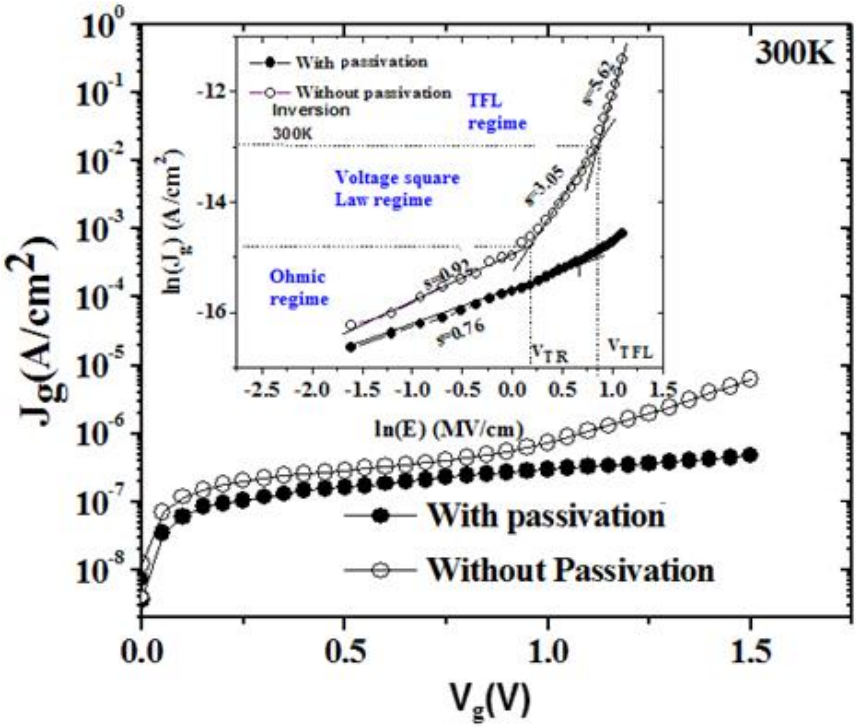

Fig.4.6. J_g characteristics of plasma-PH_3/N_2 passivated and non-passivated $In_{0.53}Ga_{0.47}As$ N-MOSFET at 300 K. Inset shows the ln|J_g| vs ln|E| plot. EOT value of non-passivated $In_{0.53}Ga_{0.47}As$ N-MOSFET is 1.9 nm and EOT value of passivated $In_{0.53}Ga_{0.47}As$ N-MOSFET is 1.7 nm. The voltage boundaries and s values of $J \propto V^{s}$ fits are also shown.

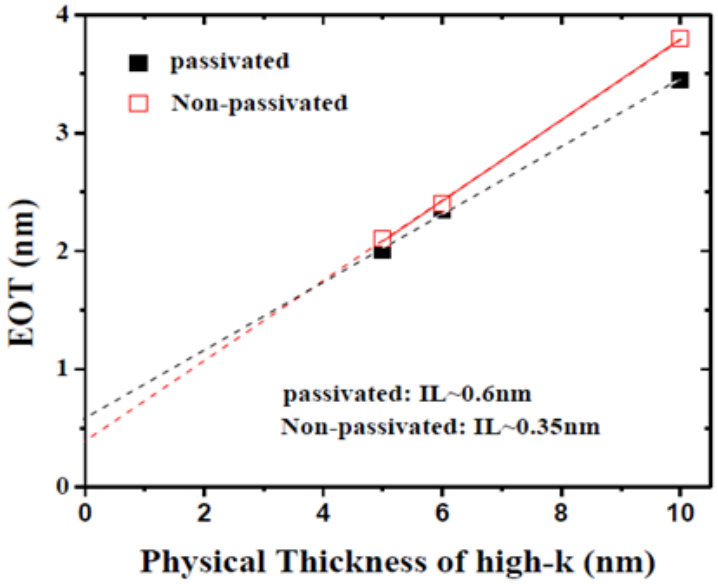

Fig.4.7. EOT vs physical oxide thickness of both passivated and non-passivated devices.

The non-passivated device shows Voltage Square Law and Trap Filled Limited Regimes (TFL) [7-8] determined by higher s due to space charge limited conduction (SCLC) mechanism. In the inset of Fig.4.6, the region between V_{TR} and V_{TFL} is referred to as the Voltage Square Law regime. The onset voltage V_{TR} can be expressed as Equation (4.1) [7]:

$$V_{TR} = \frac{8qn_o d^2}{9\varepsilon_r \varepsilon_o \theta} \qquad \text{Equation (4.1)}$$

where n_o is the concentration of free charge carriers in equilibrium, d is the thickness of the HfAlO film, ε_r is the dynamic dielectric constant of the HfAlO film, ε_o is the permittivity of free space and θ refers to the ratio of free-carrier density to total carrier (free and trapped) density. In this region where $V > V_{TR}$, τ_c becomes equal or less than τ_d. This means that the τ_c is too short for dielectric relaxation to take place. Hence, the amount of injected carriers will exceed the thermally generated carriers [9]. Thus, with increasing V_g, more injected electrons would be supplied and then captured in

trap centers located in the HfAlO bulk. It is found that s=3.05 which is ~3, implying the presence of trap states in the bulk oxide that are exponentially distributed in energy. Such value of s signifies exponentially distributed trap space charge limited conduction (EDT-SCLC) mechanism [10]. An exponential distribution of trap in energies is expected for traps originating from surface defects and structural disorders [11].

When $V > V_{TR}$, the increase of applied voltage may increase the density of free carriers resulting from injection to such a value that E_F moves up above the electron trapping level. When V reaches V_{TFL}, strong injection occurs and all traps are filled up, and subsequently injected carriers will be free to move in the oxide so that at V_{TFL}, the current will rapidly jump from its low trap limited value to a high trap-free SCL current [12]. Hence, V_{TFL} corresponds to the voltage at which quasi Fermi level passes through electron trap level [13]. The average bulk trap concentration, N_t, can be estimated from V_{TFL} as shown in Equation (4.2):

$$V_{TFL} = \frac{qN_t d^2}{2\varepsilon_o \varepsilon_r} \qquad \text{Equation (4.2)}$$

Here, d is the thickness of the film and ε_r is given by 3.42, derived from the refractive index of HfAlO which is reported to be 1.85. Thus the average trap concentration N_t was estimated to be $1.3 \times 10^{19} cm^{-3}$, which is well within the expected values of high-*k* obtained in the range of $\sim 10^{19}$-$10^{20} cm^{-3}$ [14-15].

4.2.2.2. Temperature Dependence of J_g-V_g Characteristic

The temperature dependencies on J_g are also explored in order to analyze the gate leakage mechanisms of HfAlO gate oxide in the positively gate biased region. Fig.4.8 shows a plot of $\ln|J_g|$ vs $\ln|E|$ as a function of temperature for non- passivated device. As temperature increases from 300K to 420K, electrons located at deeper trap centers are much easier to be excited. Hence, more injected electrons are required to achieve the same density as the thermally generated electrons. Thus, the s values as seen from 0.86 to 1.67 deviate from the ideal slope of ~1 with increasing temperature. This also causes the increase in V_{TR} with increasing temperature. The activation energy of the shallow traps (traps distributed closer to the E_c of the HfAlO oxide) can be determined from the plot of $\ln|J_g|$ as a function of 1/T in the Voltage square law regime as shown in the inset of Fig.4.8, where the slope represents the activation energy values of the shallow traps. These activation energy values are given as ~0.22 to 0.27 eV. It is seen that the leakage current in the TFL regime is sensitive to temperature, because these shallow traps liberate free electrons to the E_c, which is a thermally activated process following Arrhenius law. These shallow trap levels could be related to dangling bonds [16]. In addition, it is observed that V_{TFL} decreases with increasing temperature. This is due to the relatively lower voltage required to fill up all the trap levels at higher temperatures, since the thermal generation of the carriers increases with temperature.

Further analysis shows that FP emission also exists at the region in the TFL regime (at regions of $\ln|E| > 0.66$ MV/cm) for temperatures between 370K and 420K as shown in Fig.4.8. Gate leakage current associated with FP emission can be determined by utilizing the following Equation (4.3):

$$J = (qN_C\mu)E\exp\left[\frac{-q(\varphi_t - \sqrt{qE/\pi\varepsilon_r})}{kT}\right] \qquad \text{Equation (4.3)}$$

Where N_c is the density of states in the conduction band, μ is the mobility, $q\varphi_t$ is the trap energy level, E is the electric field and ε_r is the dynamic dielectric constant. For FP emission the plot of $\ln(J_g/E)$ vs $E^{1/2}$ should be linear, with the slope corresponding to the inverse of the ε_r of the gate dielectric. From the slopes of the two linear plots in Fig.4.9, the ε_r values at temperatures of 370K and 420K are found to be 5.2 and 2.4 respectively. These values correspond to the same order of magnitude of ε_r of HfAlO given by 3.42 reported in literature [17]. Hence, this means that FP emission also exists in non-passivated device at high temperature and high field region.

The Arrhenius plot of ln (J_g/E) vs 1/T shown in the inset of Fig.4.9 reveals that the ionization energy of the traps (also means the energy barrier of the traps with respect to E_c) within the HfAlO is given as ~0.95 to 1.3 eV below E_c. The fact that the activation energy obtained from the Arrhenius plot of voltage square law regime in the given temperature range is significantly smaller than the trap energy estimated from FP Arrhenius plot indicates that the traps responsible for these two mechanisms are different. FP conduction should originate from the deeper trap levels in the oxide, such as interstitial defects [18-20] or vacancies. On the other hand, SCLC mechanism is due to the shallow trap levels, attributed to defects with energy levels close to E_c, such as dangling bonds. As will be seen in Chapter 5, the existence of these defect levels can be attributed to the interdiffusion of In/Ga elements across the HfAlO/$In_{0.53}Ga_{0.47}As$ interface as analyzed from XPS analysis.

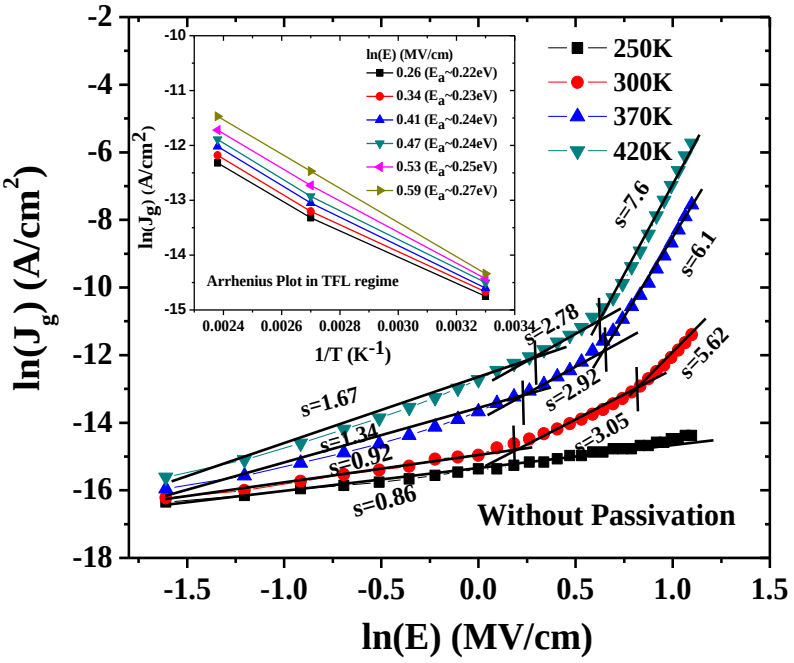

Fig.4.8. ln|J_g| vs ln|E| plot of non-passivated device at temperatures between 250K and 420K.Inset shows the Arrhenius plot in the TFL regime.

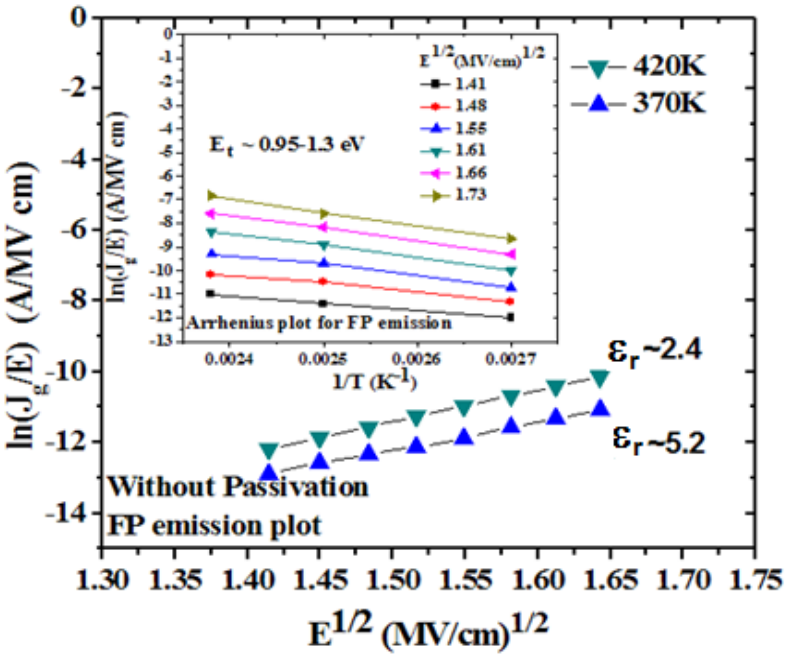

Fig.4.9. ln(J_g/E) vs $E^{½}$ plots (FP fitting) observed in non-passivated $In_{0.53}Ga_{0.47}As$ N-MOSFET. Inset shows the Arrhenius plot in the FP emission regime.

On the other hand, Fig.4.10 which shows a plot for the passivated device, depicts that the s values in the voltage square law regime are given as ~2 for 370K and 420K, suggesting a trap free SCLC mechanism, instead of EDT-SCLC mechanism. This happens when the trap level is so shallow i.e. having small ionization energy that they are not effective as electron traps. The dominance of such mechanism means that there are less bulk oxide defects present in the passivated device and that injection of carriers may also be limited by the interface properties of the high-*k*/$In_{0.53}Ga_{0.47}As$, further implying the existence of a well-formed interface between the HfAlO and $In_{0.53}Ga_{0.47}As$ which is in good agreement with the HRTEM image shown in Fig.4.5(b), compared to non-passivated device. Also, in contrast to non-passivated device, passivated device also does not experience TFL regime and FP emission, further suggesting the advantages that plasma-PH_3/N_2 passivation has on reducing these defects caused by interstitial defects or vacancies.

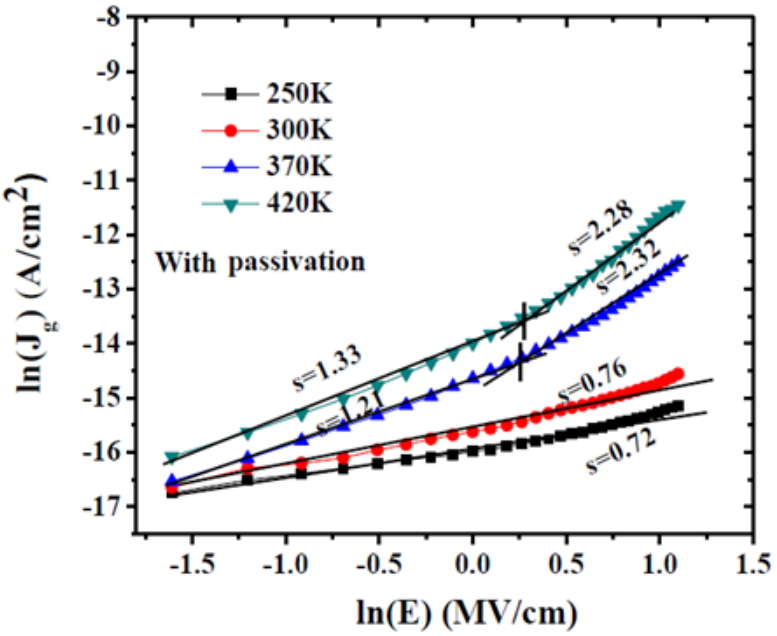

Fig.4.10. ln|J_g| vs ln|E| plot of plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ N-MOSFET at temperatures between 250K and 420K.

4.3. Conclusion

As a conclusion, in Section 4.2.2, gate leakage mechanism of the HfAlO plasma-PH_3/N_2 passivated and non-passivated $In_{0.53}Ga_{0.47}As$ MOSFETs have been evaluated, in order to correlate the quality of the oxide deposited with the gate leakage mechanisms observed. It is found that at temperatures higher than 300K, trap free SCLC mechanism dominates the gate leakage of passivated device but non-passivated device consists of exponentially distributed SCLC mechanism as well as Frenkel-Poole emission at high electric field. This Frenkel-Poole emission is associated with energy trap levels of ~0.95eV to 1.3eV and is responsible for the increased gate leakage of non-passivated device. In addition, the electrical properties of the non-passivated device has also been extracted from the SCLC mechanism, with the average trap concentration of the shallow traps of $1.3x10^{19}cm^{-3}$ and their average activation energy of ~0.22 to 0.27eV. The existence of these defect levels in non-passivated device can be attributed to the interdiffusion of In/Ga/As elements across the HfAlO/$In_{0.53}Ga_{0.47}As$ interface, thus also affecting the trap densities within the HfAlO. On the other hand, passivated device does not contain Frenkel-Poole emission nor exponentially distributed SCLC mechanism, indicating the absence of such defects in the bulk of the oxide. In addition, the temperature dependent characteristics of off-state leakage have also been evaluated to provide insight into the off-state mechanism shown in Section 4.2.1. The off-state leakage of both passivated and non-passivated device is determined by I_{bulk} where its terminology is described by reverse biased drain-substrate junction leakage, with Shockley-Read-Hall mechanism being its main contributor, and has activation energy of 0.38eV for passivated

device and 0.4eV for non-passivated device.

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Chapter 5: Effects of plasma-PH_3/N_2 Passivation on Mobility Degradation Mechanisms of $In_{0.53}Ga_{0.47}As$ MOSFETs

5.1. Introduction and Motivation

Demonstration of $In_{0.53}Ga_{0.47}As$ based MOSFETs fabricated with various in-situ and ex-situ deposited high-*k* dielectrics, with and without passivation layer, has been reported [1-4]. However, its channel mobility has still been lower than the expected bulk mobility achievable in $In_{0.53}Ga_{0.47}As$ which shows research potential of further improvement in device interface to maximize mobility.

In order to realize mobility enhancement, the scattering mechanisms responsible for the mobility degradation must be understood. In this chapter, we will take a closer look at the influence of plasma-PH_3/N_2 passivation on the mobility characteristics of $In_{0.53}Ga_{0.47}As$ MOSFETs. Firstly, mobility extraction and correction technique used would be discussed in Section 5.2.1. The evaluation of the temperature dependence study of the mobility on the mobility degradation mechanisms present in plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ MOSFETs as well as non-passivated MOSFETs would be investigated and discussed in Section 5.2.2. Section 5.2.3 would involve analysis on the factors causing the improvement in the mobility of the plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ MOSFETs compared to the non-passivated.

5.2. Mobility of plasma-PH_3/N_2 Passivated $In_{0.53}Ga_{0.47}As$ MOSFETs

5.2.1. Mobility Extraction and Correction Technique

In this work, we extracted the effective mobility from the drain conductance in the linear regime i.e. V_g-V_{th} >> V_d. For our case, the effective mobility (μ_{eff}) is extracted using the Equation (5.1):

$$\mu_{eff} = L_g * I_d / (W Q_{inv} * V_d) \qquad \text{Equation (5.1)}$$

where Q_{inv} is the inversion charge density (Ccm^{-2}). In order to obtain Q_{inv}, C-V measurements given by Equation (5.2) was used:

$$Q_{inv} = \int C_{inv} . dV_g \qquad \text{Equation (5.2)}$$

where C_{inv} is obtained using split C-V measurement. The effective field is obtained from Equation (5.3) [5]:

$$E_{eff} = (Q_{dep} + \eta\, Q_{inv}) / \varepsilon_s \qquad \text{Equation (5.3)}$$

where Q_{dep} is the depletion charge density and η is taken as ½ for electrons [6]. Q_{dep} can also be obtained from split C-V measurement.

For $In_{0.53}Ga_{0.47}As$ MOSFETs, presence of interface traps is an important issue which needs to be taken into account. The interface trap induced stretch out can lead to an overestimation of Q_{inv} when integrating the measured capacitance using the split C-V method resulting in underestimation of mobility. Hence, in this work, we have made use of the method by Zhu [7], where a C-V model is used to obtain Q_{inv} by fitting the model to the measured C-V.

Since one of our objectives in studying the temperature dependence of the mobility is to confirm the presence of the additional source of phonon scattering in the non-passivated device, we are interested in the difference between phonon scattering rates of both passivated and non-passivated device

at each temperature. This is very much affected by exponent α from $\mu \propto T^{\alpha}$. From Ref [8], even if the method used to obtain the corrected C-V is less accurate, the C-V stretch out approximately results in the scaling of the extracted inversion charge density and hence mobility with a constant factor, which thus should not affect the value of exponent α.

Thus, based on method of extraction, the mobility with interface trap correction attributed to C-V stretch out, has been plotted in Fig.5.2. However, it is important to note that Zhu's method only accounts for the stretch-out in C-V but assumes that the experimental inversion response of the carriers is free from frequency dispersion due to interface states, which may not be applicable for Ge and III–V systems where the interface states are generally high [9]. Hence, to minimize this effect of D_{it} contributing to this additional capacitance associated with traps charging (C_{it}), the split C-V curve used to extract mobility has been taken at high frequency of 100kHz. Nevertheless, a direct measurement procedure such as Hall mobility measurements, where impact of large D_{it} densities will be excluded [8, 10], will still be desirable. Another method may include measuring split C-V at temperatures as low as 77K to be free from dispersion due to D_{it} [11].

5.2.2. Measurement of Temperature Dependence of Mobility

The μ_{eff} curves is extracted from the measured gate-to-channel capacitance at 100kHz for a range of temperatures between 250K and 420K, as shown in Fig.5.1(a) and Fig.5.1(b), which corresponds to that of passivated and non-passivated devices, respectively. In addition, as shown in Fig.5.1(a), there is little variation in capacitance at V_g=1.2V with either temperature or frequency (inset). On the other hand, the non-passivated device C-V in

Fig.5.1(b) has a much larger capacitance dispersion in the inversion region with temperature and frequency (inset). This signifies the presence of larger interface defects in the non-passivated device within the upper half of the band gap than the passivated device. In addition, the presence of D_{it} causes a significant frequency-dependent threshold voltage shift in the C–V characteristics, as shown in the inset. In addition, such C-V characteristics of non-passivated device may also be due to a dispersion phenomenon involving a disordered (stoichometric defects existing within the disordered surface region) $In_{0.53}Ga_{0.47}As$ layer at the interface between the substrate and the dielectric [12], which has been proposed as one of causes of interface dipole scattering in this work as shown in Section 5.2.3.3. This disordered layer can be seen from the TEM image of Fig.4.5(a) and can also be confirmed from the XPS analysis which shows greater Ga/In diffusion for non-passivated device after anneal as shown in Section 5.2.3.3.

Fig.5.2 displays the μ_{eff}, with interface trap correction, of HfAlO/$In_{0.53}Ga_{0.47}As$ passivated and non-passivated devices at various temperatures from 250K to 420K as a function of transverse electric field (E_{eff}). It is seen that the μ_{eff} values are much higher than that for Si. Clearly μ_{eff}, in the low field region, defined as region between 0 to ~0.2MV/cm, has positive temperature dependence for non-passivated and passivated device where mobility increases with temperature. This implies the presence of Coulombic scattering due to charges near the HfAlO/$In_{0.53}Ga_{0.47}As$ interface for both devices.

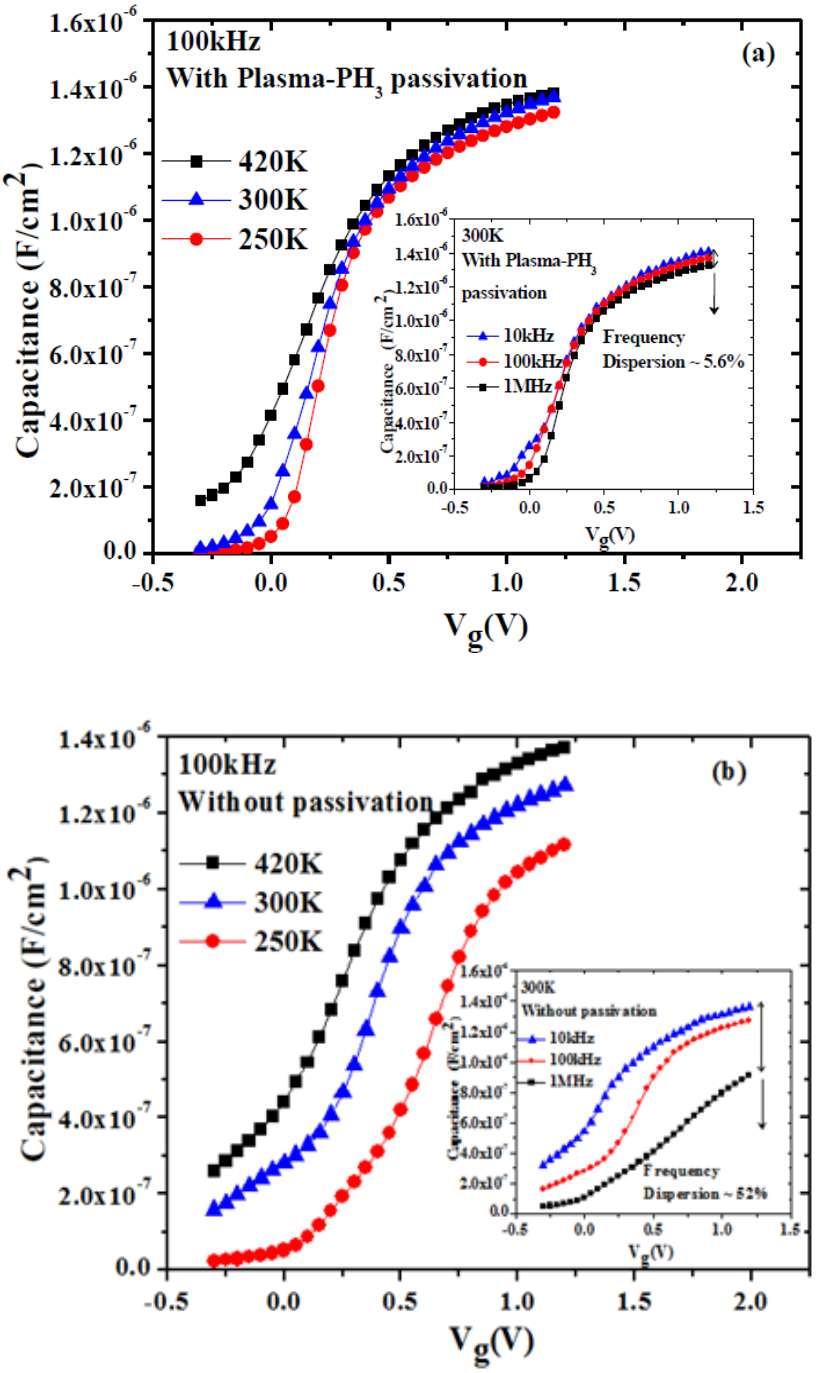

Fig.5.1 (a) C–V response at 100kHz with varying temperature of 250K to 420K of plasma-PH_3/N_2 passivated HfAlO/$In_{0.53}Ga_{0.47}As$ N-MOSFET. Inset (a) shows corresponding room-temperature *C–V* variation between 10kHz to 1MHz in passivated $In_{0.53}Ga_{0.47}As$ devices and (b) C–V response at 100kHz with varying temperature of 250K to 420K of non-passivated HfAlO/$In_{0.53}Ga_{0.47}As$ N-MOSFET. Inset (b) shows corresponding room-temperature C–V variation between 10kHz to 1MHz in non-passivated $In_{0.53}Ga_{0.47}As$ devices.

In the mid E_{eff} region (~0.3 to 0.5MV/cm) of Fig.5.2, μ_{eff} of passivated devices increase with decreasing temperature, implying phonon scattering is dominant in this region, in particular substrate/bulk phonon scattering. On the other hand, the temperature dependence of mobility for non-passivated device is weaker than that of passivated device. This is reasonable because Coulombic scattering could still play a significant role, such that it partially hides the effect of phonon scattering or that the weaker temperature dependence of mobility for non-passivated device may imply dominance of soft optical phonon scattering (SO) contributed by the HfAlO which has a weak temperature dependence [13].

In the high E_{eff} region (~0.6 to 0.7MV/cm), phonon scattering still persists in passivated device. For non-passivated device, the weak temperature dependence of mobility suggests the presence of surface roughness scattering or interface dipole scattering [14]. Similar mechanism has also been reported from simulation results in Ref [15] where experimental results obtained from atomic layer deposited Al_2O_3 on non-passivated $In_{0.53}Ga_{0.47}As$ consists of Coulombic scattering mechanism dominating at low E_{eff} and surface roughness scattering mechanism at high E_{eff}.

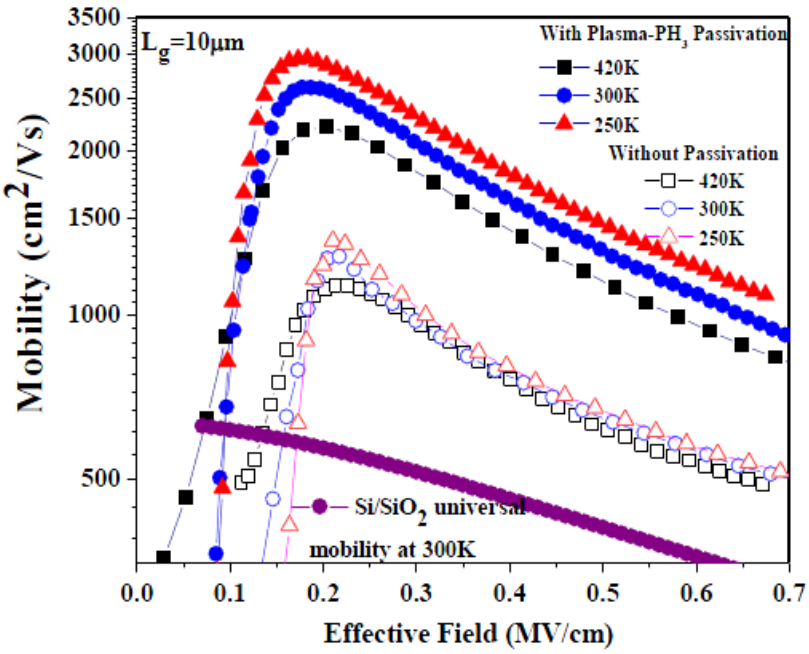

Fig.5.2. Effective electron mobility in non-passivated and plasma-PH_3/N_2 passivated HfAlO/$In_{0.53}Ga_{0.47}As$ N-MOSFET at various temperatures from 250K to 420K, using the C-V correction method.

5.2.3. Factors Causing Improvement in Mobility of plasma-PH_3/N_2 Passivated $In_{0.53}Ga_{0.47}As$ MOSFETs

5.2.3.1. Effect of Interface States

In order to understand what contributed to the reduction in Coulombic scattering in passivated device and hence to explain its higher μ_{eff} compared to non-passivated device in the low to mid-E_{eff} region, we have investigated the energy distributions of the D_{it} shown in Fig.5.3. D_{it} is strongly reduced in the upper half of the bandgap for passivated device, due to its ability in reducing As-As bonds which have their energy states in the upper half of the bandgap [16-20]. This is expected because based on the plasma-PH_3/N_2 treatment mechanism as shown in added Section 2.1.1, hydrogen from the PH_3 can enhance the removal of As element segregation by forming volatile As-H_3 that can be desorbed through evaporation.

The lesser amounts of As-As bonds in plasma-PH_3/N_2 passivated device relative to non-passivated device can be seen from Table 5.1 which has been taken from the deconvolution of XPS As3d shown in Fig.5.4 [21]. The suppression of As-As bonds observed with the use of passivation treatment can be attributed to the presence of P_xN_y layer which allows a more bulk-like $In_{0.53}Ga_{0.47}As$ interface. The existence of this P_xN_y layer can be evidenced from the analysis of the XPS peak shifts of N1s and P2p, which matches the XPS characteristics of P_3N_5 [22-23]. This suppression of free As is supported by reported active hydrogen species promoting free As desorption by forming volatile AsH_x species [23]. In addition, the improvement in midgap D_{it} at energy levels $E\text{-}E_i$~0.15eV with passivation treatment explains the reduction in SS, as mentioned in Chapter 4.

The mean D_{it} for passivated and non-passivated device as shown in Fig.5.3 is given by $6.02x10^{12}cm^{-2}eV^{-1}$ and $1.24x10^{13}cm^{-2}eV^{-1}$ respectively, measured from Charge Pumping technique with constant amplitude gate pulse at frequency of 200kHz and gate pulse amplitude of 1.2V. It is important to note that fixed charges deduced from the V_{fb} vs EOT results shown in Fig.5.5 gives values $3.1x10^{11}cm^{-2}$ and $5.1x10^{11}cm^{-2}$ for passivated and non-passivated device respectively. The density of oxide traps calculated from the C-V hysteresis for non-passivated (passivated) at 100kHz is given by $8.1x10^{11}cm^{-2}$ ($3.4x10^{11}cm^{-2}$). Since these values of oxide traps and fixed charges are smaller than D_{it}, this means that a significant amount of Coulombic scattering may be attributed to the D_{it} rather than by fixed charges or the oxide traps.

Nevertheless, while these results may provide a suggestion as to the origin of some interface defects responsible for the interface trap density

distribution, a definitive statement still cannot be made as to the real significance of the role of As surface states. This is because the presence of Ga and In surface states still need to be identified, but due to their smaller binding energy separation between the peaks, identification of these defect states using XPS are difficult. Hence more analysis in areas such as electronic spin resonance would be helpful toward atomic identification of the interface defects.

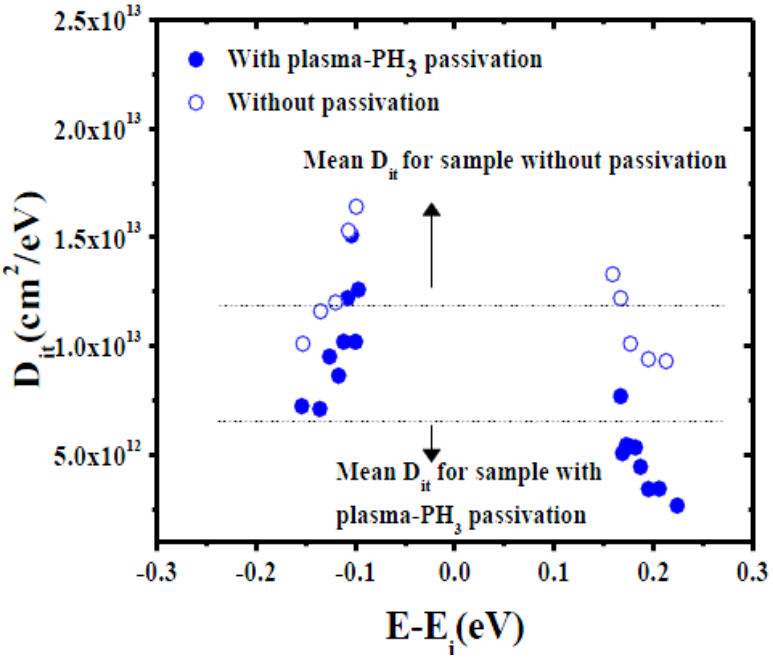

Fig.5.3. Energy distribution of D_{it} as determined by the t_r and t_f dependence of charge pumping currents. The horizontal lines represent the mean D_{it} of the entire bandgap, for non-passivated and plasma-PH_3/N_2 passivated device.

In addition, the mean D_{it} values shown suggest that ideal interface quality cannot be achieved by simple pre-gate or post-gate treatment alone. Several groups have shown that with post-gate treatment only, the D_{it} values of ALD $Al_2O_3/In_{0.53}Ga_{0.47}As$ [24-27] are still undesirably high. Hence, further advances in reducing D_{it} across the whole bandgap, most likely using both pre-gate and post-gate treatment, are still required before replacing Si channel by high indium content $In_xGa_{1-x}As$. Such methods may include the use of

combined plasma-PH_3/N_2 passivation treatment with optimized pre-gate treatment i.e. $(NH_4)_2S$ treatment, which with optimized concentration of 10% compared to 22% is effective in suppressing significant reoxidation without introducing the detrimental effects of high $In_{0.53}Ga_{0.47}As$ surface roughness [28]. For the use of post-gate treatment, forming gas anneal in H_2 can also be effective in passivating D_{it} in the lower half of bandgap in some cases while in other cases it is effective in passivating D_{it} in the upper half of the bandgap. A systematic study of the effects of this forming gas anneal should also be studied.

Table 5.1. Summary of relative intensities of As-As chemical states at the $In_{0.53}Ga_{0.47}As$ surfaces, obtained from the chemical shifts in As 3d core level emission. As a reference, the bulk $In_{0.53}Ga_{0.47}As$ sample is prepared by in-situ Ar sputter etching about 10Å of the non-treated sample and the XPS spectra is analyzed [23].

	composition of As 3d
	As-As
No Passivation	0.46
Plasma-PH_3/N_2 passivation	0.4
Bulk	0.3

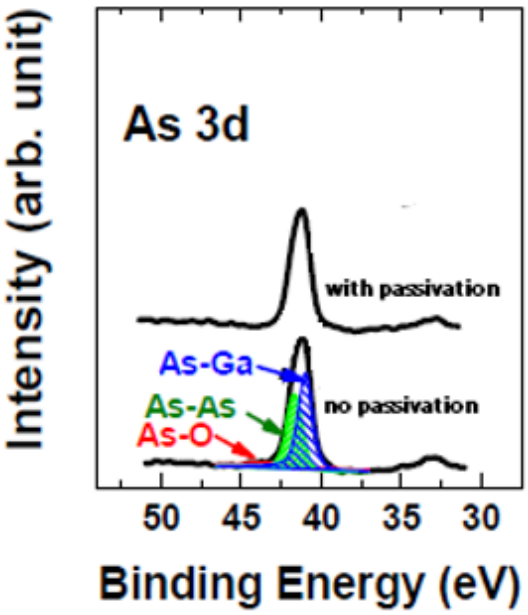

Fig.5.4. XPS spectra for the $In_{0.53}Ga_{0.47}As$ surfaces with and without plasma-PH_3/N_2 passivation treatment are shown for (a) As 3d. Typical results of deconvolution analysis are illustrated with the corresponding chemical bonds indicated [21].

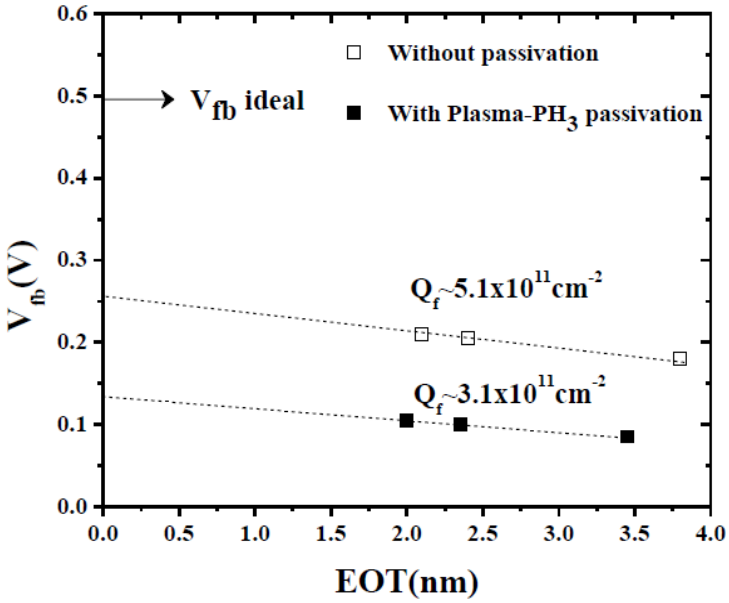

Fig.5.5. V_{fb} vs EOT plots of passivated and non-passivated $In_{0.53}Ga_{0.47}As$ devices.

Another treatment involved can also be through the use of Fluorine (F) incorporation into high-*k* gate dielectric using CF_4/O_2 plasma treatment. F is effective in reducing the D_{it} by 4X at high-*k*/substrate interface [29]. This is

attributed to the termination of oxygen vacancies by the incorporated F atoms to form stronger Hf-F bonds with higher binding energy. F tends to pile up at the $HfO_2/In_{0.53}Ga_{0.47}As$ interface passivating interface traps, thus resulting in a better quality interface [29-31]. However, the effect of F incorporation on the D_{it} distribution is not investigated yet. One of the disadvantages of plasma-PH_3/N_2 passivation technique is the use of plasma which could result in plasma damage occurring if excessive plasma is applied (such as plasma wattage or treatment time) as seen in Ref [21]. This plasma damage could result in disordering, such as dangling bonds and broken bonds, as well as surface roughening. However, in this work, comparison of the AFM results for sample after plasma-PH_3/N_2 passivation treatment shows relatively unchanged values at 0.15nm compared to 0.16nm for non-passivated sample. This implies that no plasma damage is observed for this passivation treatment condition. This shows the importance of optimizing the plasma power and treatment time in ensuring that plasma damage is minimized.

5.2.3.2. Effect of Phonon Scattering

In addition to Coulombic scattering caused by high densities of D_{it}, scattering due to coupling of electrons with the surface optical modes and substrate longitudinal-optical (LO) phonons, could contribute to the difference in μ_{eff} in both devices [32]. Fig.5.6 shows the $\mu_{eff,}$ mobility limited by Coulombic scattering, μ_{coul}, mobility limited by phonon scattering, $\mu_{ph,}$ and mobility limited by surface roughness scattering, $\mu_{sr,}$ as a function of E_{eff} at 300K for N-MOSFETs with and without passivation. To obtain the μ_{ph} values, we made use of the Mathiessen's rule: $1/\mu_{ph} = 1/\mu_{eff} - 1/\mu_{coul} - 1/\mu_{sr.,}$ where μ_{coul} is extracted from the μ_{eff} at low fields by linear fitting and

extrapolated to high $E_{eff,}$. This dependency is linear due to the increasing carrier screening effects of the electrons with increase in electric field, which causes the attractive potential of the electrons with the charged centers to weaken. In order to obtain $\mu_{sr,}$ it is best to measure the device at temperatures as low as 77K in order to limit the contribution of phonon scattering to the $\mu_{eff.}$ However, we were unable to perform such measurements due to the lack of resources.

Hence μ_{sr} plotted in Fig.5.6 is obtained from the simulated μ_{sr} results of $HfO_2/In_{0.53}Ga_{0.47}As$ device with p-type doping concentration of $3x10^{17}cm^{-3}$ taken from Ref [32]. The μ_{sr} have been obtained from Ando's model, with an exponential correlation spectrum, as well as degenerate-static-multisubband screening included.

The μ_{sr} simulated [32] is given by RMS asperity height (Δ) ~0.48nm and correlation length (λ) ~1.2nm. AFM measurements reveal that Δ for our device is given by ~0.15nm and ~0.16nm for passivated and non-passivated device respectively, for devices without 600°C S/D anneal. However since the step height for non-passivated device seen from TEM image taken with 600°C S/D anneal in Fig.4.5(a) is small/insignificant and this occurs only in localized regions, we can assume that Δ is still almost the same as without S/D anneal. Hence using the μ_{sr} obtained from simulation to assume the lower limit for the expected μ_{sr} is reliable.

Similarly for passivated device, the TEM step height seen in Fig.4.5(b) is negligible and hence no significant deviation from Δ RMS height obtained from AFM for without S/D anneal is expected. Thus, given that the Δ RMS height is similar for both non-passivated and passivated devices, the use of the same μ_{sr} values to extract μ_{ph} of both devices is reliable since the expected

increase in μ_{sr} for passivated device compared to non-passivated is only 1.14X due to μ_{sr} being proportional to λ/Δ^2 [33].

μ_{sr} starts to become a significant factor at E_{eff} > 0.7MV/cm from Fig.5.6 but this value of E_{eff} where μ_{sr} starts to play a significant role depends on the exponent of E_{eff}. The exponent of E_{eff} is dependent on the value of λ[34]. Following the approach that was used in Ref [33], we also assumed that λ is the same for both non-passivated and passivated devices and hence the exponent of E_{eff} would be the same [33]. Thus, the μ_{sr} would only become a significant factor at high E_{eff} of 0.7MV/cm for both non-passivated and passivated devices which is not within the region where μ_{ph} is extracted from. This means the μ_{ph} extraction is reliable.

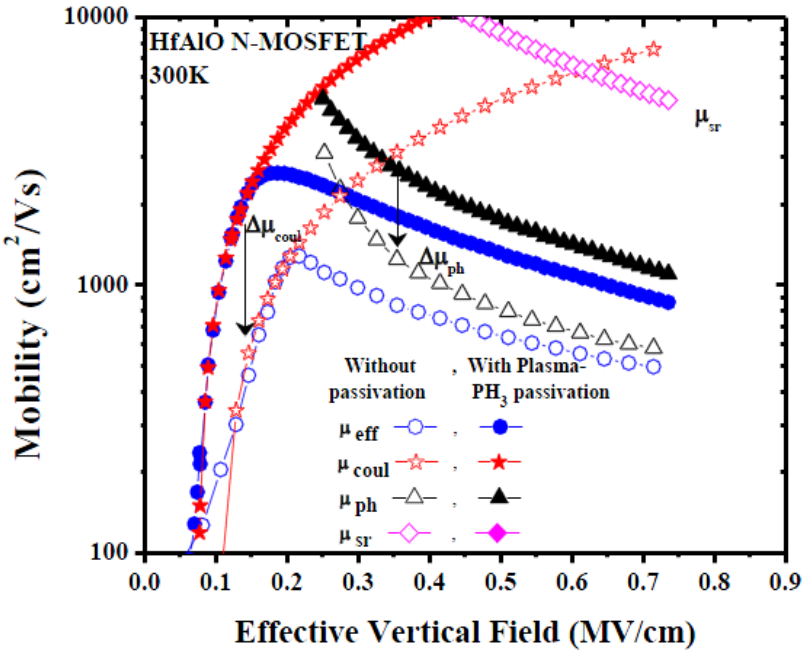

Fig.5.6. μ_{eff}, μ_{coul}, μ_{ph}, μ_{sr}, for passivated and non-passivated device obtained using Matthiessen's rule.

Fig.5.6 shows that the mobility limited by phonon scattering for the non-passivated device is significantly lower than the passivated device,

indicating a more severe phonon scattering for the non-passivated device. Assuming no significant difference in bulk $In_{0.53}Ga_{0.47}As$ of both non-passivated and passivated device, the phonon scattering contribution from the substrate is expected to be similar for both samples. Thus, this suggests that the reason for the additional source of phonon scattering in non-passivated device could be due to the effects from HfAlO gate dielectric. To investigate the reason for this source of additional phonon scattering, we studied the phonon scattering rate as a function of temperature as shown in Fig.5.7. Phonon scattering rate is taken from the equation (q/(μm*)) [13], where m* is the effective mass of the carrier in $In_{0.53}Ga_{0.47}As$ inversion channel taken as $0.041m_o$ with m_o as the free electron mass. By taking the difference between the two sets of phonon scattering rate curves in Fig.5.7, we can get the scattering rate caused by this additional phonon source in the HfAlO of the non-passivated device, and this curve is also plotted in Fig.5.7. From the two dimensional deformation potential theory of surface phonon scattering, the scattering rate due to optical phonon may be expressed as [13,35] Equation (5.4):

$$1/\tau_{op} \propto [N_R + (N_R + 1)\, u(E - \hbar\omega)] \qquad \text{Equation (5.4)}$$

where $N_R = (1/(e^{\hbar\omega/kT} - 1))$ is the phonon occupation number, E is the carrier energy, ω is the phonon frequency, and $u(x)$ is the unit step function, $u(x < 0)=0$ and $u(x > 0)=1$. Assuming that the phonon energy is smaller than thermal carrier energy i.e. $\hbar\omega < E$, then Equation (5.5) shows that:

$$1/\tau_{op} \propto (2N_R + 1) = ((e^{\chi} + 1)/(e^{\chi} - 1)) \text{ where } \chi = \hbar\omega/kT \qquad \text{Equation (5.5)}$$

Equation (5.5) indicates that when $\hbar\omega << kT$, $(1/\tau_{op}) \propto T$, and when

$\hbar\omega > kT$, $(1/\tau_{op})$ approaches a constant i.e. independent of temperature [13]. In order to investigate the characteristics of the phonon scattering contributed by the high-*k*, its two transverse optical (TO) phonons with energies $\hbar\omega$ would be used. For HfAlO, the values of TO1 and TO2 for HfAlO are assumed to be those between HfO_2 and Al_2O_3. TO1 for HfO_2 is given as 12.40meV and its TO2 is 48.35meV, while TO1 for Al_2O_3 is given as 48.18meV and its TO2 is 71.4meV [36]. Comparison of the above values with kT of 21.5meV-36meV (for our measurement temperatures of 250K to 420K), a temperature independent scattering rate for TO2 phonons is expected since $\hbar\omega >$ kT where $\hbar\omega$ is between 48.35meV to 71.4meV and kT is 21.5meV-36meV. On the other hand, TO1 phonons scattering rate can have a linear temperature dependence if $\hbar\omega <$ 36meV, where $\hbar\omega$ is between 12.4meV to 48.18meV. It can also have a temperature independent scattering rate if $\hbar\omega >$ 21.5meV. Thus, from the results where a temperature independent scattering rate for the TO2 phonons, and a temperature independent to linear temperature dependence for the TO1 phonons is observed, this explains the weak temperature dependence of the scattering rate of non-passivated device seen in Fig.5.7.

Weak temperature dependence is a characteristic of SO phonon scattering, in contrast to phonon scattering contributed by the bulk phonons from the substrate which has stronger temperature dependence [13]. This implies the reason for the additional source of phonon scattering rate in non-passivated device is due to the HfAlO.

The reason for this is likely due to the thinner interfacial layer thickness given by ~0.35nm for the non-passivated device, while it is given by ~0.6nm for the passivated device, as deduced from the intercept of the EOT vs physical oxide thickness in Fig.4.7. Even though the difference in interfacial layer

thickness is small, based on high-k/SiO_2/Si system, even a slight increment (~0.1nm) in SiO_2 interfacial layer thickness can result in an exponential improvement in μ_{ph} [37-38]. This is based on the physical mechanism where the scattering amplitude matrix element decreases away from the dielectric interface as e^{-Qt}, where Q represents the in-plane momentum transfer and t is the distance from the interface [37]. Thus, this SiO_2 interfacial layer between the channel and the HfO_2 reduces the detrimental effect of the soft optical phonon scattering on the mobility through decoupling between the motion of electrons in the inversion layer and those SO phonons in the high-*k* dielectric. Therefore, similar methodology or reason can be applied to our high-*k*/$In_{0.53}Ga_{0.47}As$ system where a ~0.25nm smaller interfacial layer thickness than the passivation layer of P_xN_y can result in the significant reduction to μ_{ph} of non-passivated device, contributed by the significant SO phonon scattering in the HfAlO.

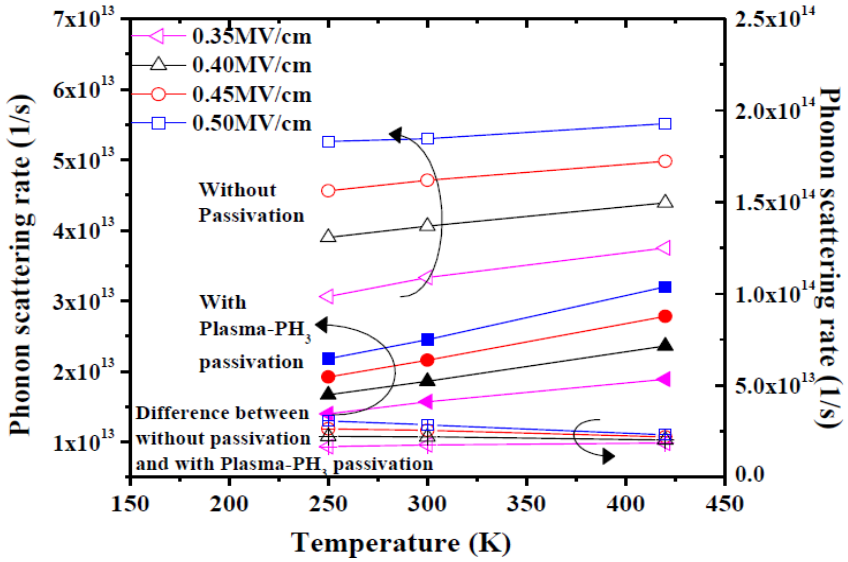

Fig.5.7. Phonon scattering rate vs Temperature for passivated and non-passivated devices, with difference between both phonon scattering rates being contributed by the SO phonon scattering caused by HfAlO in the non-passivated device.

5.2.3.3. Effect of Interface Dipole Scattering

It is seen that the temperature dependences of μ_{eff} in the non-passivated device in the high E_{eff} regime is weak (from Fig.5.2). Based on the TEM image in Fig.4.5(a), non-uniform interfacial layer with unclear high-*k*/$In_{0.53}Ga_{0.47}As$ interface and some non-uniform transition regions is observed while clear transitions and atomically sharp and smooth interface between HfAlO and $In_{0.53}Ga_{0.47}As$ can be observed for passivated device in Fig.4.5(b). Thus the possibility of surface roughness scattering as one of the causes of weak temperature dependence of mobility for non-passivated device cannot be ignored. However, this effect may not be significant due to localized areas of the non-passivated device where the step height is higher than passivated device.

Nevertheless, the correlation between the mobility at high E-field and shift in V_{fb} in the negative direction (given by difference between y-axis intercept and V_{fb} ideal of Fig.5.5 which corresponds to the dipole strength) shows there is another mechanism that possibly contributes to the weak temperature dependence of the non-passivated device at high E-field. It is seen that with stronger interface dipole strength, μ_{eff} increases. The stronger interface dipole strength observed in passivated device could be due to the ordering of the interface dipoles i.e. more ideally aligned dipoles contributing to smaller interface dipole scattering. On the other hand, non-passivated device experience smaller interface dipole strength possibly caused by randomly oriented dipoles which scatter the carriers i.e. more interface dipole scattering. This can occur due to the interdiffusion of elements of high-*k* and

$In_{0.53}Ga_{0.47}As$ substrate across the interface which induces dipole fluctuation, thus contributing to carrier scattering which results in lower μ_{eff} [39-40].

Fig.5.8 shows the Ga 3d and In 4d XPS spectra obtained from 2nm HfAlO deposited on $In_{0.53}Ga_{0.47}As$ at take-off angle (TOA) of 30° and 90° for both passivated and non-passivated devices with and without PDA. P1/P2 ratio from Fig.5.9 shows the deconvoluted area ratio of the peaks present in the Ga3d and In4d spectra taken from Fig.5.8. P1 (spectra at ~19eV) includes the area of $Hf4f_{5/2}$ and Ga3d peaks while P2 (spectra at ~17eV) includes the area at $Hf4f_{7/2}$ and In4d peaks. Fig.5.9 depicts that non-passivated device has a larger change in Ga/In ratio than passivated device.

Obtaining accurate values of Ga/In ratio is difficult due to the XPS lines of Ga and In being strongly overlapped with Hf. Therefore, we are comparing the change in P1/P2 ratio (comparing P1/P2 ratio for conditions without and with PDA), to deduce that there is larger intermixing/interdiffusion of Ga/In near the high-*k*/$In_{0.53}Ga_{0.47}As$ interface for non-passivated device, which may be responsible for the existence of larger amounts of randomly oriented dipoles in non-passivated device.

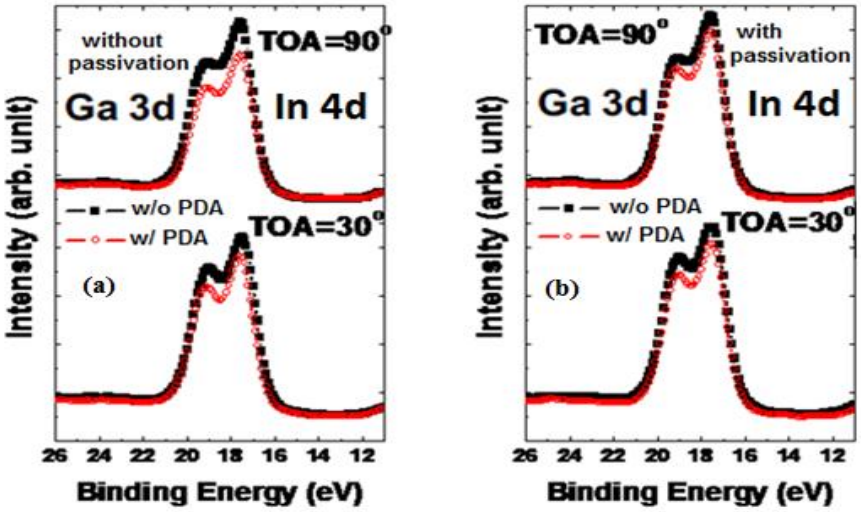

Fig.5.8. Ga 3d and In 4d (a) XPS spectra for the $In_{0.53}Ga_{0.47}As$ surfaces without and (b) with plasma-PH_3/N_2 passivation treatment are shown.

Change in P1/P2 ratio can be correlated with change in Ga/In ratio since the ideal ratio of $Hf4f_{5/2}/Hf4f_{7/2}$ is found to be ¾, and is not expected to change regardless of the thickness and the measurement condition. Passivated device shows smaller change in P1/P2 ratio, which implies that the passivated device is more robust to interdiffusion of Ga/In elements across the high-*k*/$In_{0.53}Ga_{0.47}As$ interface.

Plasma-PH_3/N_2 passivation results in reduced amount of interdiffusion of elements within the HfAlO/$In_{0.53}Ga_{0.47}As$interface and hence effective in reducing the degree of interface dipole scattering. This is because of the formation of a thin P_xN_y passivating layer over the P terminated surface, caused by P-for-As reaction, before high-*k* deposition. This P_xN_y interlayer has strong mechanical properties and is a chemically and thermodynamically stable material, with the presence of stable and strong covalent bond due to its cross-linked structure [41-42]. In addition, the presence of P-for-As exchange reaction, which is also present in our plasma-PH_3/N_2 passivation treatment process, causes Ga-P bond to be present in passivated device [23], which is

stronger than that of Ga-As bond, due to its larger heat of formation. Hence, the chances of breaking the Ga-P bonds, to result in interdiffusion of elements across the interface, at high temperature processing (for instance during PDA or S/D activation annealing) would be reduced in the passivated device. However, too excessive In/Ga-P bond formation may result in formation of artifacts that can further worsen device performance [23].

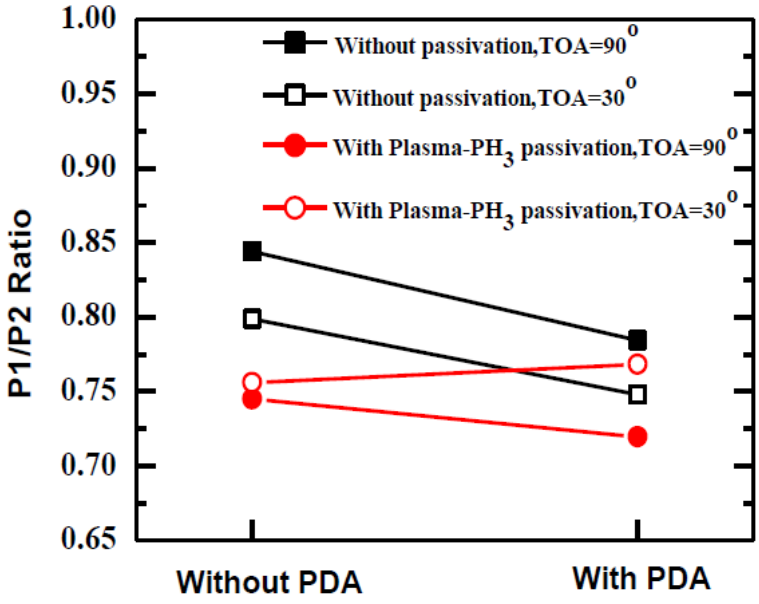

Fig.5.9. XPS analysis showing P1/P2 ratio as a function of conditions (with and without PDA) applied to the samples. The P1/P2 ratio has been taken from the deconvolution of the peaks from XPS Ga 3d and In 4d of Fig 5.8.

Hence, as seen from the chemical analysis from XPS data, it is believed that the small amount of crystalline disorders/defects present in the substrate of the non-passivated device below the HfAlO/$In_{0.53}Ga_{0.47}As$ interface as shown in the highlighted box of the high resolution-TEM (HR-TEM) image as seen in Fig.4.5(a) could possibly be due to the effects of the interdiffusion of the high-*k* and $In_{0.53}Ga_{0.47}As$ elements [39-40]. Such defects are not obvious from the HR-TEM image of the passivated device seen in Fig.4.5(b). Nevertheless, it is important to note that surface roughness scattering may also play a part in

this regime due to the HR-TEM image seen in Fig.4.5(a) which reveals a slight waviness at the high-*k*/$In_{0.53}Ga_{0.47}As$ interface for non-passivated device, suggesting that its poorer interface roughness could also be responsible for the lower μ_{eff} observed.

5.3. Conclusion

As a conclusion, this chapter investigated the inversion layer scattering mechanisms of HfAlO/$In_{0.53}Ga_{0.47}As$ N-MOSFETs with plasma-PH_3/N_2 passivation layer to understand the physical origins of mobility enhancement compared to non-passivated device. The mobility extraction technique used for interface trap correction used for this work has been discussed in Section 5.2.1 and followed by the evaluation of a temperature dependence study of the mobility on the mobility degradation mechanisms present in plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ MOSFETs as well as non-passivated MOSFETs in Section 5.2.2. Section 5.2.3 investigated the physical origins of mobility enhancement of HfAlO/$In_{0.53}Ga_{0.47}As$ N-MOSFETs with plasma-PH_3/N_2 passivation layer. It is found that the mobility enhancement of plasma-PH_3/N_2 passivated device is caused by the reduction in Coulombic scattering caused by the reduced As-As bond formation, as well reduced soft optical phonon scattering associated with reduced interactions of the surface optical phonons in the high-*k* oxide. In the high E_{eff}, the reduction in the interface dipole scattering is caused by the decrease in the interdiffusion of elements from HfAlO and $In_{0.53}Ga_{0.47}As$ substrate, which prevents formation of randomly oriented dipoles.

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Chapter 6: TCAD Simulation of Non-passivated and plasma-PH_3/N_2 Passivated $In_{0.53}Ga_{0.47}As$ MOSFET for Scalability Evaluation

6.1. Introduction and Motivation

The goal of this chapter is to evaluate effectiveness of plasma-PH_3/N_2 passivation in achieving and improving scalability in $In_{0.53}Ga_{0.47}As$ MOSFETs through TCAD simulations. For realistic study on this aspect, TCAD simulation model parameters must be tuned so that they are able to predict measured data of reported devices reasonably accurately. Hence it is important to identify a good measurement results set that can be used for model parameter tuning purpose. The device performance of the fabricated sub-100nm plasma-PH_3/N_2 HfAlO/$In_{0.53}Ga_{0.47}As$ MOSFETs fabricated in this work has high contact resistance and increased gate to source-drain spacing compared to another lot fabricated in our group, and hence these data are not best suited to calibrate model parameters. Hence, the device model calibration parameters and optimization for scalability studies in this thesis has been based on our group's IEDM 2008 long channel (4μm) non-passivated and plasma-PH_3/N_2 passivated $HfO_2/In_{0.53}Ga_{0.47}As$ MOSFETs as well as the short channel (95nm) plasma-PH_3/N_2 passivated HfO_2 $In_{0.53}Ga_{0.47}As$ MOSFET electrical data performance. The device models and the parameters used for calibration to fit the electrical data from the long channel and short channel gate length MOSFETs will be described in Section 6.2. This section will also explore, based on the energy diagram, the effect of D_{it} at different energy trap location on the I_d-V_g results. In addition, through simulation, it can be further confirmed that the smaller V_{th} and SS of plasma-PH_3/N_2 passivated device is caused by

the smaller concentration of acceptor-like traps while its smaller I_{off} and SS is due to its smaller concentration of donor-like traps as also mentioned in Chapter 4. Using the same device calibration model parameters, Section 6.3 shows the expected performance scalability of non-passivated vs plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ MOSFETs using the existing process flow.

6.2. Calibration of Simulation Parameters for 95nm Gate Length Fabricated $In_{0.53}Ga_{0.47}As$ MOSFET with Implanted S/D

The experimental data for fitting simulation parameters to realistic values has been taken from the 4µm and 95nm gate length TaN/ 10nm HfO_2/ $1x10^{17}cm^{-3}$ p-type $In_{0.53}Ga_{0.47}As$/ $1x10^{18}cm^{-3}$ p-type InP buffer/ $3x10^{18}cm^{-3}$ p-type substrate MOS devices [1]. Two types of 4µm devices i.e. one with plasma-PH_3/N_2 passivation and another one without plasma-PH_3/N_2 passivation, have been used for the calibration purposes. Good match between the simulated and the experimental device characteristics have been obtained by calibrating the simulation parameters as seen in Fig.6.1. The simulations have been performed using 2D device simulator, MEDICI [2].

First step involved in the fitting of the 4µm non-passivated and passivated device characteristics to the experimental device characteristics is by varying the TaN gate work function between 4.44eV to 4.53eV in order to fit the V_{th}. Next step is performing a curve fit focused on the subthreshold region by varying the D_{it} distribution as well as the HfO_2 dielectric constant. The fitting of the I_d-V_g curves for both devices have been pursued by adopting the D_{it} distributions as shown in Fig.6.2, which is in agreement with the interface trap distribution of $HfO_2/In_{0.53}Ga_{0.47}As$ MOSFET reported in [3]. The acceptor-like traps exist at energy levels above the CNL, while donor-like traps

exist at energy levels below the CNL. CNL in Fig.6.2 is at 0.24eV above intrinsic Fermi level (E_i), a value chosen which is between 0.104eV above E_i [4] and also within E_c [5] reported in literature. HfO_2 permittivity values of 13 for passivated device and 12 for non-passivated device has been used, based on the EOT values given as 3nm and 3.2nm respectively taken from the published C-V results [1], for which I-V data is shown in Figs.6.1(a)-(b).

Next step involved the fitting of the linear and saturation region currents of the long channel devices. Mobility models used include Lombardi's model for low lateral field mobility and high-*k* mobility model (both to model the mobility degradation at semiconductor-insulator interface due to perpendicular field and remote phonon scattering prevalent with use of high-*k* dielectrics) and the high lateral field GaAs like mobility model with velocity overshoot. These models were used to reproduce the inversion mobility measured using the split C-V method. Different mobility input parameters for low field mobility model, but same high field mobility model input parameters, were used for 4µm non-passivated and plasma-PH_3/N_2 passivated devices. The values used for bandgap and electron affinity have been based on literature which determines the band alignment [6-7]. In addition, band-to-band tunnelling and quantum mechanical models were included. Three valley band related models were turned on in order to capture the effects of intervalley transfer by varying the electron effective mass at different satellite states which will impact the drive current. This is important especially at high lateral fields where the possibility of electron transfer to the upper satellite valley will be higher.

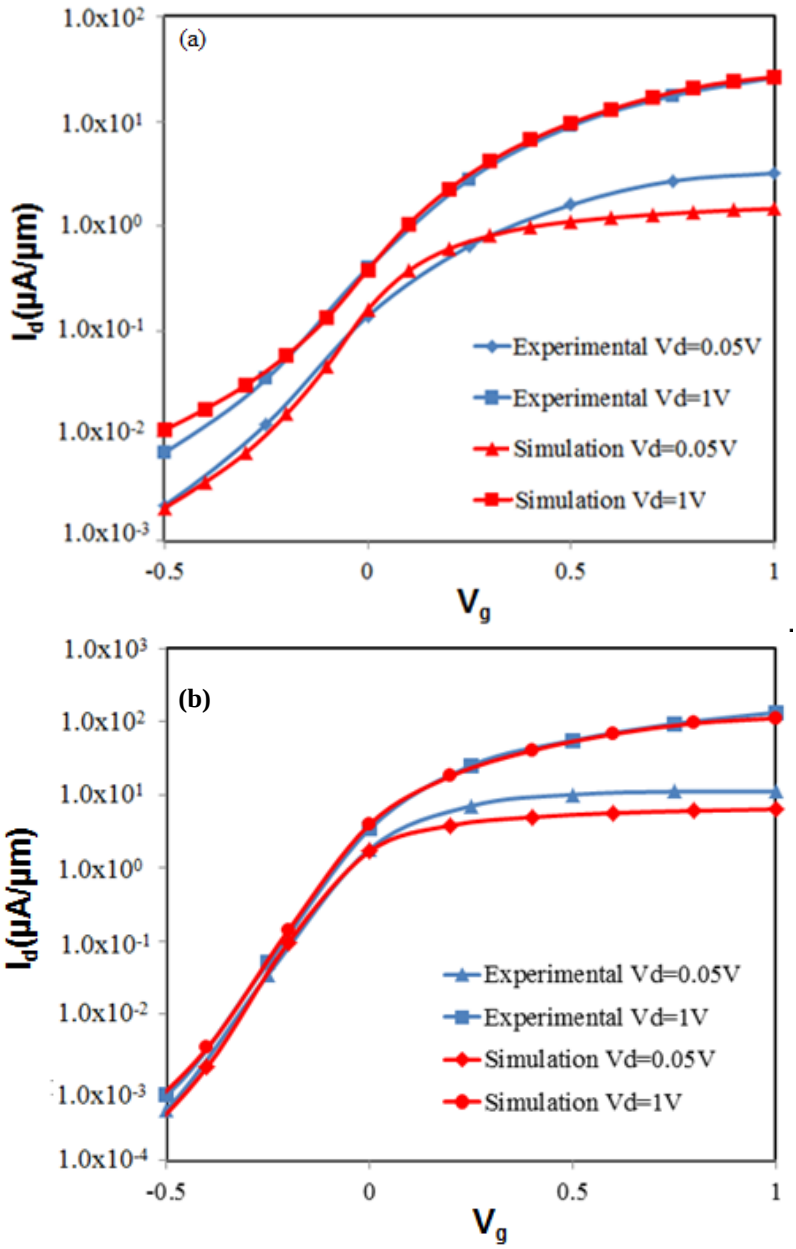

Fig.6.1 (a) Comparison between the experimental and simulated I_d-V_g characteristics of 4μm gate length non-passivated $In_{0.53}Ga_{0.47}As$ MOSFET and (b) Comparison between the experimental and simulated I_d-V_g characteristics of 4μm gate length plasma-PH_3/N_2 $In_{0.53}Ga_{0.47}As$ MOSFET.

The S/D doping has been modelled by Gaussian profiles with adjustments to reproduce the S/D sheet resistance taken from the reported transmission line method (TLM) measurement as 80Ω/sq with junction depth given by 100nm [8]. The peak carrier concentration $3.5x10^{18}cm^{-3}$ located at the surface of semiconductor is used, which is similar to the experimental peak carrier

concentration obtained with the similar implant and annealing conditions given by $2.3x10^{18}cm^{-3}$ [9]. The contact resistance 600Ω.µm of the long channel devices is taken from the reported TLM measurements [8]. The TCAD calibration parameters including the band alignment parameters have been included in Table 6.1. The simulation results with calibrated model parameters for the 4µm non-passivated and passivated devices to the experimental results are shown in Fig.6.1(a) and Fig.6.1(b) respectively. This set of parameters is sufficiently accurate for predicting I_{on}, I_{off}, DIBL and SS which are vital for device performance evaluation for scalability.

Table 6.1. Parameters used in the calibration of the device models.

	HfO_2			1nm P_xN_y			$In_{0.53}Ga_{0.47}As$			InP		
	k value	bandgap	affinity	*k* value	bandgap	affinity	*k* value	bandgap	affinity	*k* value	bandgap	affinity
Non-passivated	12	5.6	2.5	Nil	Nil	Nil	13.9	0.744	4.51	12.5	1.34	4.38
Plasma-PH_3/N_2 passivated	13	5.6	2.5	5.2	8	2.52						

For the calibration of the simulation parameters of the short channel (95nm L_g) non-passivated device, similar mobility model input parameters, as well as other model parameters, to the 4µm non-passivated device have been used. The only difference is in terms of the higher work function used at 4.81eV, S/D peak doping concentration at $5.5x10^{18}cm^{-3}$, junction depth of 32nm due to different implant conditions at $20keV/1x10^{14}cm^{-2}$ resulting in matched measured sheet resistance of ~250Ω/sq [10]. The S/D contact to gate has a spacing of 2µm, with contact resistances set at 1200Ω.µm reported from TLM measurements [8]. The results are shown in Fig.6.3. $I_{d,sat}$ and subthreshold region of the non-passivated device is fitted well except the on-

state current at low V_d. This set of parameters is sufficiently accurate for predicting I_{on}, I_{off} , DIBL and SS which are vital for device performance evaluation for scalability. We also show the predicted performance enhancement, using the same D_{it} distribution and mobility input parameters for low field and high field obtained from the long channel 4µm plasma-PH_3/N_2 passivated device, for the plasma-PH_3/N_2 passivated 95nm L_g device. Similar to the long channel device, the expected I_d-V_g for passivated device also shows V_{th} shifted to the left and reduced DIBL caused by lesser amount of interface traps. The DIBL is given by 100mV/V for the predicted plasma-PH_3/N_2 passivated device while non-passivated device has DIBL 127mV/V. The SS for plasma-PH_3/N_2 passivated device is 169mV/dec compared to 233mV/dec for non-passivated device at V_d=1V, corresponding to the increasing contribution of the SCE to the SS and DIBL of the 95nm L_g device. $I_{d,sat}$ is given by 273µA/µm for plasma-PH_3/N_2 passivated device, which is more than 2X increase compared to the $I_{d,sat}$ of non-passivated device at 120µA/µm. This is attributed to the larger mobility caused by reduced interface scattering at the HfAlO/$In_{0.53}Ga_{0.47}As$ interface.

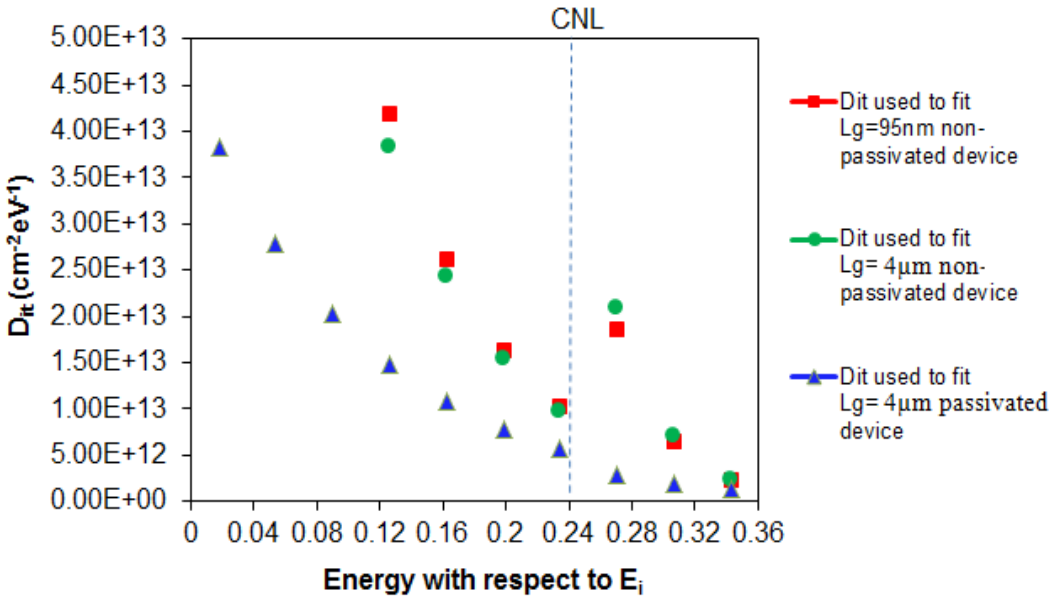

Fig.6.2. D_{it} distribution, with trap energy level with respect to the intrinsic Fermi level, of $HfO_2/In_{0.53}Ga_{0.47}As$ MOSFET with and without plasma-PH_3/N_2 passivation simulated for I_d-V_g fitting. Only the upper half of the bandgap is shown for fitting since the simulation results for surface channel architecture MOSFETs are sensitive to this part of the bandgap only [11]. Note that traps above the CNL are defined as acceptor-like traps while traps below this level are defined as donor-like traps.

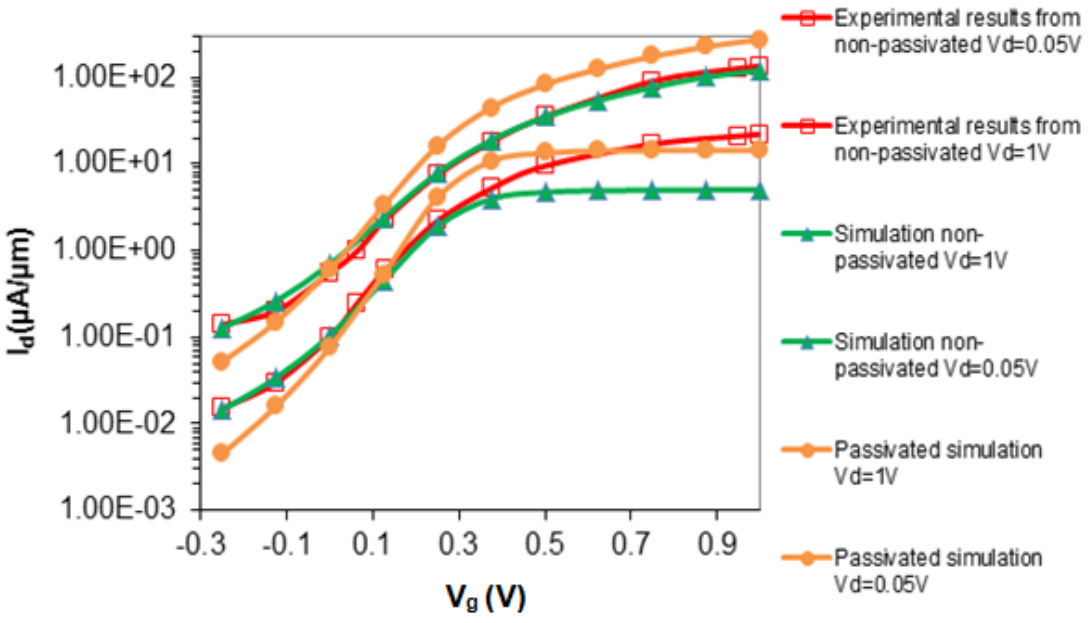

Fig.6.3. Calibration of non-passivated L_g=95nm with 10nm thick HfO_2 device showing matching to the experimental results. Expected performance enhancement prediction through plasma-PH_3/N_2 passivation using simulation is also shown.

6.3. Effect of Interface Trap Density on Threshold Voltage of Non-passivated and plasma-PH_3/N_2 Passivated MOSFET

As mentioned in Chapter 4, the smaller concentration of acceptor-like traps for plasma-PH_3/N_2 device was identified to be responsible for reduced V_{th}. The D_{it} distribution used in the simulations as a function of energy from the intrinsic Fermi level E_i is concentrated in the upper half of the bandgap as seen in Fig.6.2, due to its surface channel architecture [11]. Note that E_i has been calculated as 0.416eV based on standard Equation (6.1):

$$E_i = \frac{E_C + E_V}{2} + \frac{1}{2}kT\ln\left(\frac{N_V}{N_C}\right) \qquad \text{Equation (6.1)}$$

It will be shown here which D_{it} energy location corresponds to which point of the I_d-V_g curves taken from Figs.6.1(a)-(b). Looking at Fig.6.4(a) and Fig.6.4(b), taken at V_g=-0.5V and V_d=0.05V which corresponds to the off-state of non-passivated and plasma-PH_3/N_2 passivated device shown in Fig.6.1(a) and Fig.6.1(b) respectively, non-passivated device has E_F at 0.17eV below E_c while passivated device has E_F at 0.22eV below E_c. Thus V_g for non-passivated device will sweep at 0.154eV above E_i. Since E_c energy level with respect to E_v is given as 0.74eV and E_i energy level with respect to E_v is given as 0.416eV, E_F at 0.17eV below E_c corresponds to energy level of 0.57eV with respect to E_v. Hence, 0.57eV-0.416eV=0.154eV would mean E_F is 0.154eV above E_i at off-state. Similarly, passivated device will sweep at 0.104eV above E_i. At these two locations, which are given by 0.154eV and 0.104eV above E_i for non-passivated and plasma-PH_3/N_2 passivated device respectively, the density of donor-like traps is higher for non-passivated compared to passivated device as seen from Fig.6.2 D_{it} distribution. Hence, this explains the larger subthreshold slope and leakage for non-passivated than passivated case as seen

from Fig.6.1(a) and Fig.6.1(b) at V_g=-0.5V, V_d=0.05V.

As I_d from Fig.6.1(a) and Fig.6.1(b) continues to increase to 0.1μA/μm, E_F will sweep through much smaller range on magnitude of D_{it}. Before achieving strong inversion, Fig.6.5(a) below shows E_F at 0.059eV away from E_c for non-passivated device and 0.0988 away from E_c for passivated device. This corresponds to 0.265eV away from E_i for non-passivated device and 0.225eV away from E_i for passivated device, based on similar calculations mentioned earlier. The fact that energy level is currently at 0.265eV away from E_i for non-passivated device, this means it is beyond the CNL. Hence, acceptor-like traps residing at this energy level for non-passivated device would start to play a part in affecting device performance, while plasma-PH_3/N_2 treated device which has energy level at 0.225eV away from E_i still has donor-like traps controlling the device performance. Thus the acceptor-like traps given by trap concentration of ~$2x10^{13}cm^{-2}eV^{-1}$ at energy level of 0.265eV seen in Fig.6.2 would contribute to a positive shift in V_g to the right at I_d=0.1μA/μm in Fig.6.1(a) for non-passivated device. On the other hand, the donor-like traps given by trap concentration of ~$5x10^{12}cm^{-2}eV^{-1}$ at energy level of 0.225eV away from E_i for passivated device seen in Fig.6.2 would contribute to V_g shift to the left at I_d=0.1μA/μm in Fig.6.1(b). This explains the V_g shift to the right to V_g=-0.036V for non-passivated and V_g shift to the left to V_g=-0.2V for passivated device, when taken at I_d =0.1μA/μm.

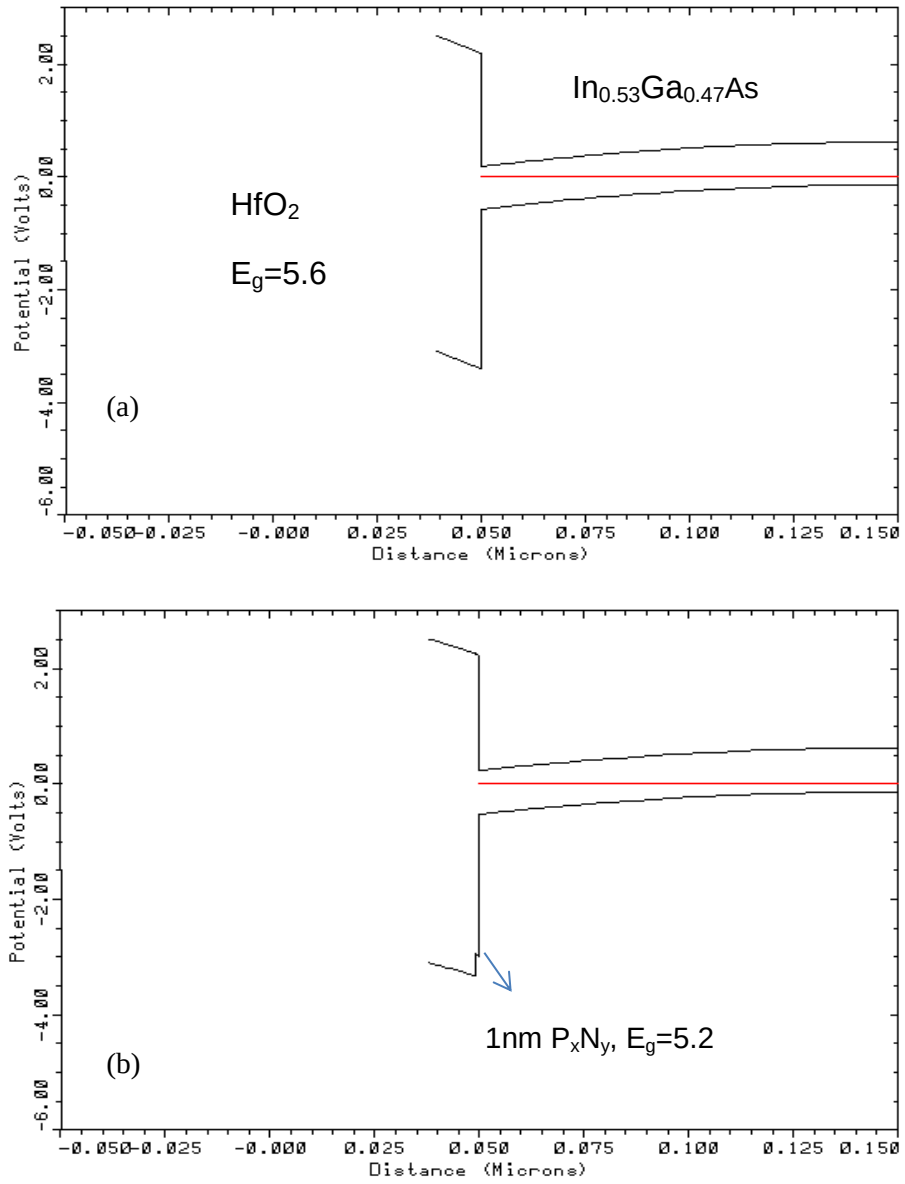

Fig.6.4 (a) Energy band diagram showing the conduction band energy, Fermi level energy and valence band of non-passivated and (b) plasma-PH_3/N_2 passivated device taken at V_g=-0.5V, V_d=0.05V. The upper and lower black lines correspond to E_c and E_v respectively while horizontal line between E_c and E_v corresponds to E_F.

The energy band diagram for the respective threshold voltage states taken at 0.5µA/µm from Fig.6.1(a) and Fig.6.1(b), which corresponds to $V_g=V_{th}$=0.1V for non-passivated and $V_g=V_{th}$=-0.12V for passivated devices respectively, is given in Fig.6.6(a) and Fig.6.6(b). At this state, E_F is already close to the E_c for both devices, implying that the energy states for both devices are already above the CNL which means there will be contribution of

acceptor-like traps to the V_{th}. As seen from Fig.6.2, non-passivated device is seen to contain more acceptor-like traps than non-passivated device. Hence, this explains the larger shift in V_{th} to the right for the non-passivated device compared to plasma-PH_3/N_2 passivated device.

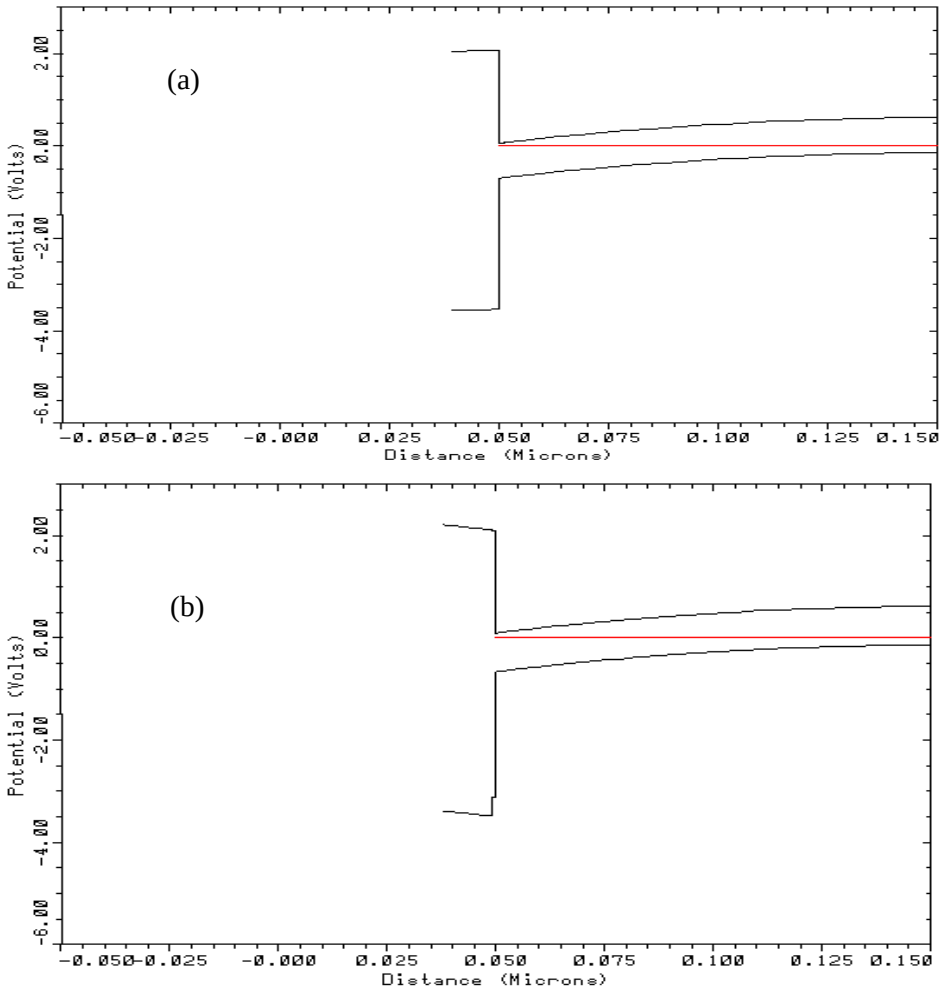

Fig.6.5 (a) Energy band diagram of non-passivated and (b) plasma-PH_3/N_2 passivated device before reaching strong inversion. Note that V_g is taken at -0.036V for non-passivated corresponding to I_d=0.1μA/μm from Fig.6.1(a) and V_g at taken at -0.2V for passivated corresponding to I_d=0.1μA/μm from Fig.6.1(b).

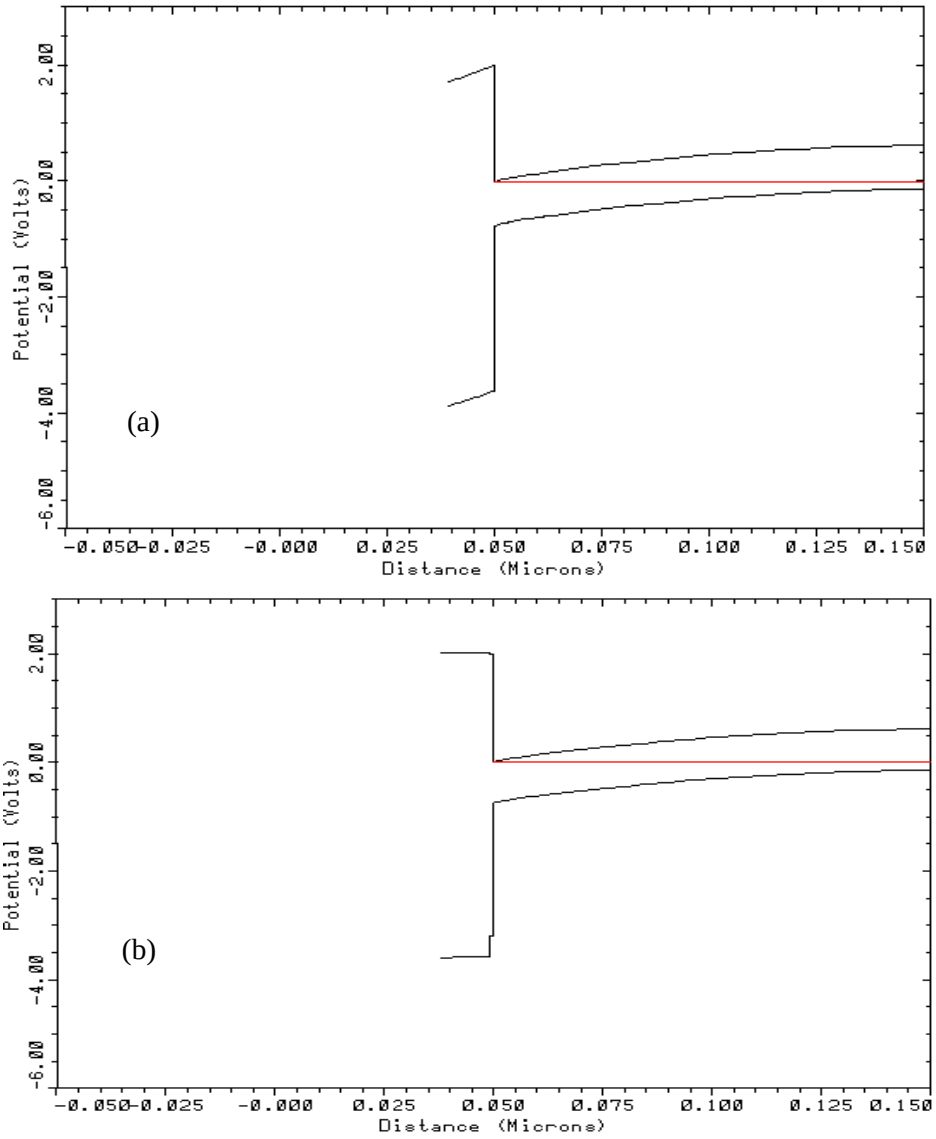

Fig.6.6 (a) Energy band diagram of non-passivated and (b) plasma-PH_3/N_2 passivated device at the respective V_{th}. Note that V_g is taken at 0.1V for non-passivated device and V_g is taken at -0.12V for passivated device.

6.4. Effect of Interface Trap Density on I_d-V_g Characteristics of Non-passivated and plasma-PH_3/N_2 Passivated MOSFET

Fig.6.7(a) shows the distribution of acceptor-like trap density simulated and their effects on the I_d-V_g characteristics at V_d=0.05V on the 4μm MOSFET is shown in Fig.6.7(b). Increasing acceptor-like traps will shift the V_{th} to the right making inversion operation difficult, resulting in reduced on-state current. On the other hand, Fig.6.7(c) shows the distribution of donor-like trap density

simulated and their effects on the I_d-V_g plot of the MOSFET shown in Fig.6.7(d). Significant contribution of donor-like traps in the semiconductor bandgap makes it difficult to move the E_F towards the valence band edge, thus making it difficult to turn the transistor off. Therefore, the SS and off currents, taken at V_g=-0.3V of the device with higher donor-like interface traps are relatively high. This has also been observed from the data reported by other groups [12-13].

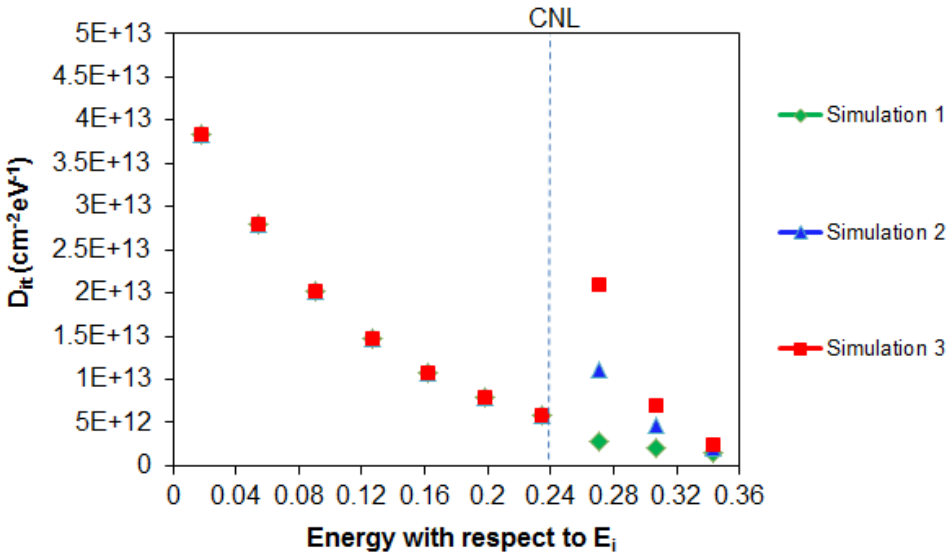

Fig.6.7 (a) Distribution of acceptor-like trap density used in three simulations of Fig.6.7(b). The simulations have been varied such that acceptor-like traps, which correspond to energy trap levels beyond CNL, are increasing while the donor-like traps corresponding to energy trap levels below CNL are fixed.

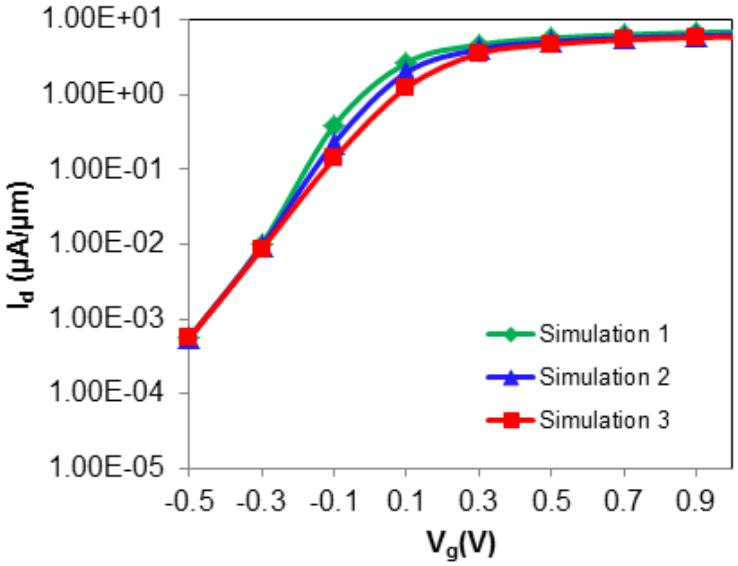

Fig.6.7 (b) MEDICI simulation of $In_{0.53}Ga_{0.47}As$ MOSFET with varying acceptor-like interface traps and fixing donor-like traps, with D_{it} distribution shown in Fig.6.7(a). Acceptor-like traps increase V_{th} and on-current. On current is degraded from 112 µA/µm to 105µA/µm and 97µA/µm, and V_{th} increases from 0, 0.02V to 0.1V, for D_{it} distribution given as simulation 1,2,3 respectively shown in Fig.6.7(a).

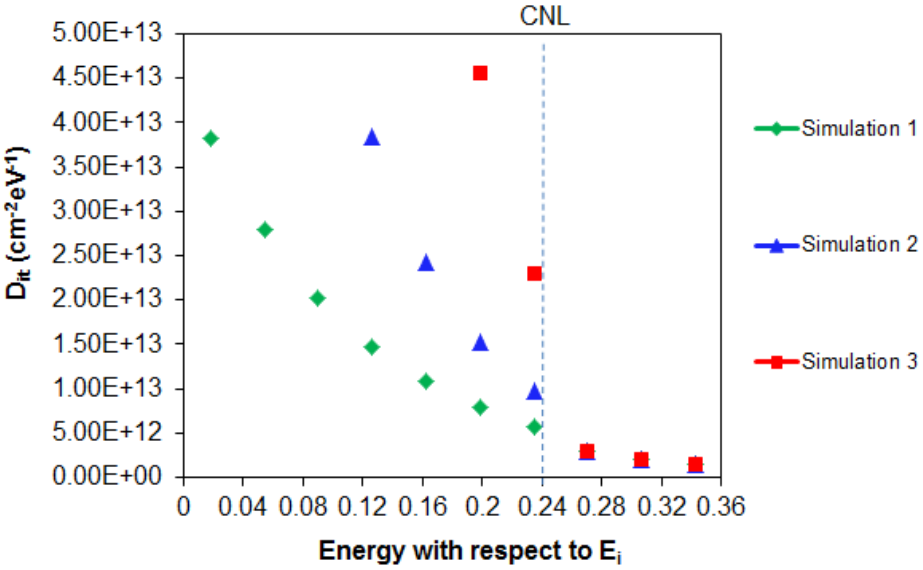

Fig.6.7 (c) Distribution of donor-like trap density in three simulations of Fig.6.7(d) variation. The simulations have been varied such that donor-like traps, which correspond to energy trap levels below CNL, are increasing while the acceptor-like traps corresponding to energy trap levels above CNL are fixed.

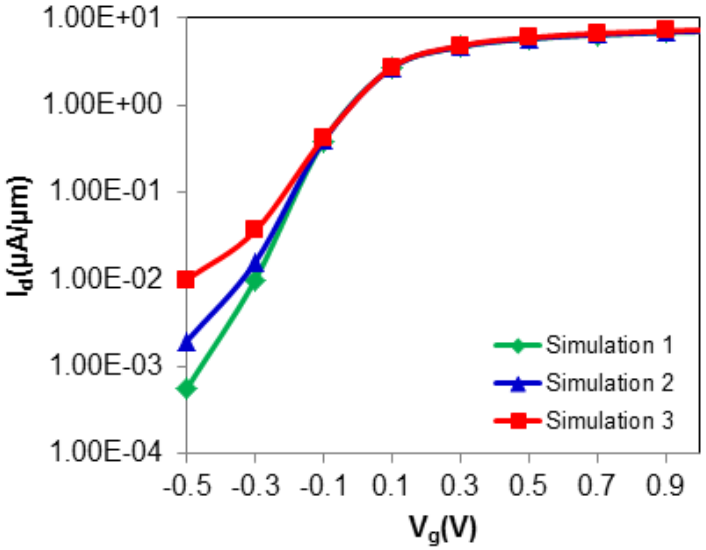

Fig.6.7 (d) MEDICI simulation of $In_{0.53}Ga_{0.47}As$ MOSFET with varying donor-like interface traps and fixing acceptor-like traps with D_{it} distribution shown in Fig.6.7(c). Donor-like traps change SS and off current of the device, keeping on-current unchanged.

6.5. Performance Scalability of Implanted S/D $In_{0.53}Ga_{0.47}As$ MOSFET Without and With plasma-PH_3/N_2 Passivation Treatment

Performance scaling of HfO_2 non-passivated vs plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ MOSFET using the same process flow as the original fabricated device conditions, and hence same EOT values given as 3nm and 3.2nm for plasma-PH_3/N_2 and non-passivated devices respectively, is studied in this section. Fig.6.8 summarizes the improved subthreshold characteristics in sub-100nm regime with plasma-PH_3/N_2 passivation. We found that SS, taken at V_d=1V, and DIBL of passivated devices is better due to multiple effects of reduced interface trap capacitance, thinner EOT as well as the effect of different interfacial layer thickness and composition. The results are shown only until L_g=60nm as the device at 50nm can no longer shut down with the existing process flow.

Fig.6.9 shows the $V_{t,sat}$ roll off at V_d=1V, showing the plasma-PH_3/N_2 treated device has better roll off than non-passivated device. The on-state performance comparison between these two devices with scaling is summarized in Fig.6.10 below. Plasma-PH_3/N_2 treated device has a better on-state performance attributed to the improved gate stack/$In_{0.53}Ga_{0.47}As$ interface more specifically due to its reduced acceptor-like trap density. Channel length scaling is an effective way to improve the on-current in long channel devices since the saturation current is inversely proportional to the channel length. However, when the channel length is scaled to the sub-100nm regime, it is observed in this figure that $I_{d,sat}$ scaling saturates. The reasons could be due to intervalley transfer of electrons from the Γ to the L valley where the effective mass of electrons is larger which contributes to large density of states but reduced injection velocity as well as increasing contribution of the parasitic series resistance. In addition, the increasing SCE from worsened electrostatic integrity, as shown in later section (Chapter 7 Fig.7.37), can also be the main reason for $I_{d,sat}$ to saturate and even have reduced performance as device scales into sub-50nm regime.

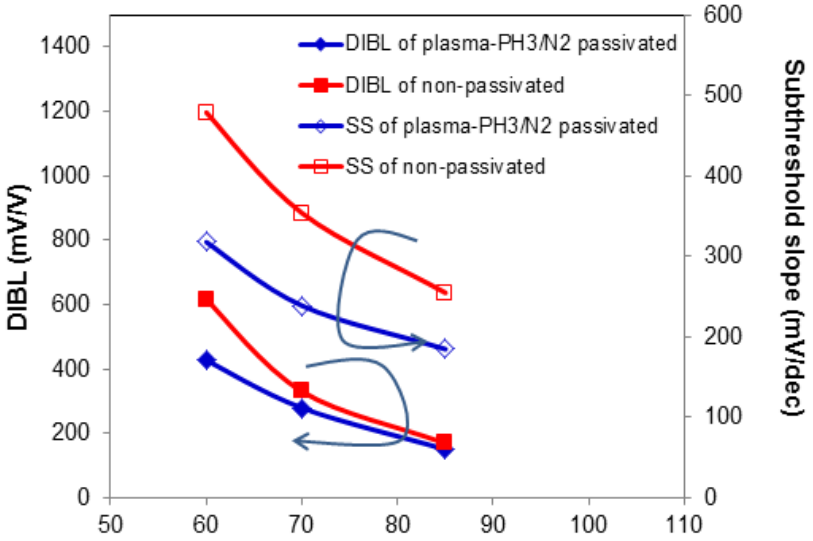

Fig.6.8. Comparison of DIBL and subthreshold slope as a function of gate length for non-passivated vs plasma-PH_3/N_2 passivated, where EOT of non-passivated device is 3.2nm and passivated device is 3nm taken from the reported data [1]. The SS has been taken at V_d=1V.

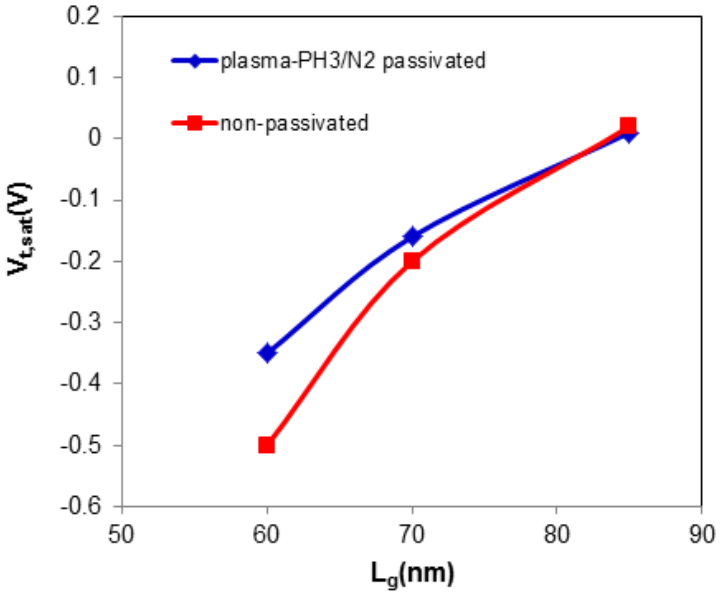

Fig.6.9. Comparison of $V_{t,sat}$ vs L_g for the two types of devices with scaling metrics at 1µA/µm.

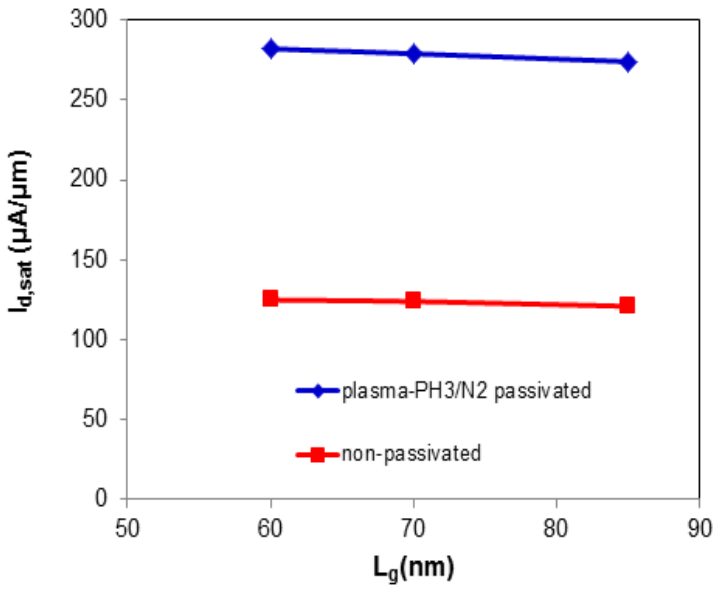

Fig.6.10. Comparison of $I_{d,sat}$ vs L_g for the two types of devices at V_d=1V, V_g=1V, where EOT of non-passivated device is 3.2nm and passivated device is 3nm taken from the reported data [1].

6.6. Conclusion

As a conclusion, this chapter has shown the calibration methodology and parameters used to match the simulation I_d-V_g data to the experimental data of $HfO_2/In_{0.53}Ga_{0.47}As$ MOSFETs with and without passivation obtained from IEDM 2008 paper by our group [1]. From TCAD simulation, the cause of the shift in V_{th} to the left for plasma-PH_3/N_2 passivated structure has been explained to be due to its smaller acceptor-like concentration relative to non-passivated device, while its smaller off-leakage can be attributed to its smaller donor-like trap density. The effect of varying the acceptor-like trap concentration as well as donor-like trap concentration on the plasma-PH_3/N_2 passivated device has also been studied, revealing the poorer on-state performance with larger acceptor-like concentration as well as larger off-state leakage with larger donor-like concentration, in agreement with several

reported papers. With the current process flow, the on-state performance scalability of plasma-PH_3/N_2 passivated device vs non-passivated device has been simulated. On-state performance of passivated devices are higher than corresponding non-passivated devices, with improvements to the SCE charateristics attributed to reduced EOT and also reduced D_{it}. Nevertheless, even at L_g=80nm the DIBL of plasma-PH_3/N_2 device is already 200mV/V but with $I_{d,sat}$ of only 275µA/µm at V_g=1V, V_d=1V. This implies further improvement to the device structure and process flow is necessary for further improved device performance. These modifications will be explored in Chapter 7 through simulation using calibrated models presented in this chapter.

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Chapter 7: Optimization Studies of plasma-PH_3/N_2 Passivated $In_{0.53}Ga_{0.47}As$ MOSFET for Sub-22nm Device Performance

7.1. Introduction and Motivation-Issues and Challenges

As transistors continue to scale aggressively in accordance with Moore‘s Law to sub-22-nm dimensions, it is important to explore novel channel materials and device structures that would lead to high performance nanoscale MOSFETs that are reasonably energy-efficient. Due to their significant transport advantage which allows high performance even at low supply voltage, high mobility materials are being very actively researched as channel materials for future highly scaled CMOS [1-8]. Thus, the idea of introducing III-V material, in our work $In_{0.53}Ga_{0.47}As$, as channel material is appealing.

However the device design considerations for $In_{0.53}Ga_{0.47}As$ MOSFET differ from that of a Si MOSFET for reasons explained here. The off-state leakage and SCE of $In_{0.53}Ga_{0.47}As$ MOSFET is expected to be worse than Si due to its smaller bandgap, high band-to-band tunnelling leakage, and also larger permittivity. In addition, the driving capability of $In_{0.53}Ga_{0.47}As$ MOSFETs may also be adversely affected because of their smaller density of states (DOS) due to its small effective mass compared to Si. One effect of small DOS is its reduction in scattering rate through having less final states for carriers to scatter to, which slows down the replenishment process and leads to a phenomenon seen in $In_{0.53}Ga_{0.47}As$ MOSFET known as source starvation [9]. This effect can limit the sheet charge density at a given gate bias.

This chapter will make use of the same calibrated plasma-PH_3/N_2 $In_{0.53}Ga_{0.47}As$ MOSFET presented in Chapter 6 for device optimization studies using TCAD simulations. Section 7.2 would involve optimizing implanted S/D

(ISD) $In_{0.53}Ga_{0.47}As$ MOSFET drive current capability by reducing access resistance through the use of spacer and best case contact resistance achievable in ISD $In_{0.53}Ga_{0.47}As$ MOSFET. The device scalability of these ISD would be further optimized through the use of source drain extension (SDE) as well as halo doping in order to reduce the SCE. One of the limitations of ISD is the low activation levels of silicon implanted in S/D (maximum $1x10^{19}cm^{-3}$) which further worsens the source starvation effects. Thus, Section 7.3 aims to reduce these effects by using epitaxial-grown S/D (known as raised S/D i.e. RSD) MOSFET which has the ability to incorporate high in-situ active doping densities ($4\text{-}10x10^{19}cm^{-3}$) in $In_{0.53}Ga_{0.47}As$ without high temperature anneals [10-11]. It will be shown in Section 7.3.1 that by comparison of the RSD with the optimized ISD, the reduction in source starvation helps in further improving the drive current performance of the RSD $In_{0.53}Ga_{0.47}As$ MOSFET. In addition, RSD MOSFET has the benefit of improving the SCE compared to optimized ISD and thus more potential for device scalability improvement. From the RSD structure, further improvement to device performance has been obtained with the use of thin channel (10nm) presented in Section 7.4. This is due to the reduced inversion layer width caused by increased quantum confinement which allows more electron carrier concentration to exist at the channel.

However, for sub-22nm technology node, such RSD thin channel structure at channel thickness (T_{ch}) of 10nm is insufficient to maintain high electrostatic integrity. This is based on the rule of thumb based on FDSOI MOSFETs, that to maintain good SCE the channel thickness should be no thicker than $L_g/3$ [12]. Hence, further channel thickness reduction is simulated with additional simulations performed on heterostructure device and varying

spacer materials to enhance device performance with low SCE and low GIDL shown in Section 7.5 down to L_g=14.nm.

7.2. Device Optimization of Implanted S/D $In_{0.53}Ga_{0.47}As$ MOSFET

Two techniques were used to optimize the drive current capability of the implanted S/D structure for this section. The first is reducing the R_c from 1200Ω.μm to 400Ω.μm. This value has been chosen based on the best achievable contact resistance measured on implanted S/D $In_{0.53}Ga_{0.47}As$ MOSFET [13]. The second is including a spacer of 15nm width, achieved through self-aligned technique, to reduce series access resistance by reducing the gate–S/D contact spacing from 2μm in the original process flow. Also, EOT has been reduced to 2nm for plasma-PH_3/N_2 device compared to 3nm in the existing process flow in Chapter 6 to further increase the device performance. In addition to these changes, ISD structure consists of halo implant, S/D extension and deep S/D to obtain acceptable electrostatic integrity with acceptable $I_{d,sat}$ compared to without halo. The halo implant is located between the deep S/D and SDE as shown from the 1D plot taken at the S/D, which is shown in Fig.7.1.

The realistic peak deep S/D concentration is chosen as $9x10^{18}cm^{-3}$ [14-15]. Improvement in electrostatic integrity with halo implant can be observed as shown in Fig.7.2(a) for L_g=70nm, giving DIBL of 226mV/V, 164mV/V and 103mV/V for devices without halo, with halo concentration of $7.2x10^{17}cm^{-3}$ and halo concentration of $2x10^{18}cm^{-3}$ respectively, implying that implementing an even higher halo doping concentration of $2x10^{18}cm^{-3}$ would further improve the DIBL. However, the drawback is the greater reduction in I_{on} as shown in Fig.7.2(b) given as 979μA/μm, 914μA/μm and 643μA/μm at V_d=0.7V, V_g=1V

for devices without halo, with halo concentration of $7.2x10^{17}cm^{-3}$ and halo concentration of $2x10^{18}cm^{-3}$ respectively. The improvements in electrostatic integrity with larger halo implant concentration can be explained from the potential contours plot (Figs.7.3(a)-(c)) and the conduction band energy plot taken at 1nm below the $P_xN_y/In_{0.53}Ga_{0.47}As$ interface (Fig.7.4). There are lesser potential lines contributed by the S/D into the channel for Fig.7.3(a) and Fig.7.3(b) compared to Fig.7.3(c), showing that control of S/D over the channel is effectively improved by halo doping. The conduction band energy profiles taken at 1nm below the interface show that the potential barrier faced by source electrons is lower for the device without halo compared to that with halo shown in Fig.7.4.

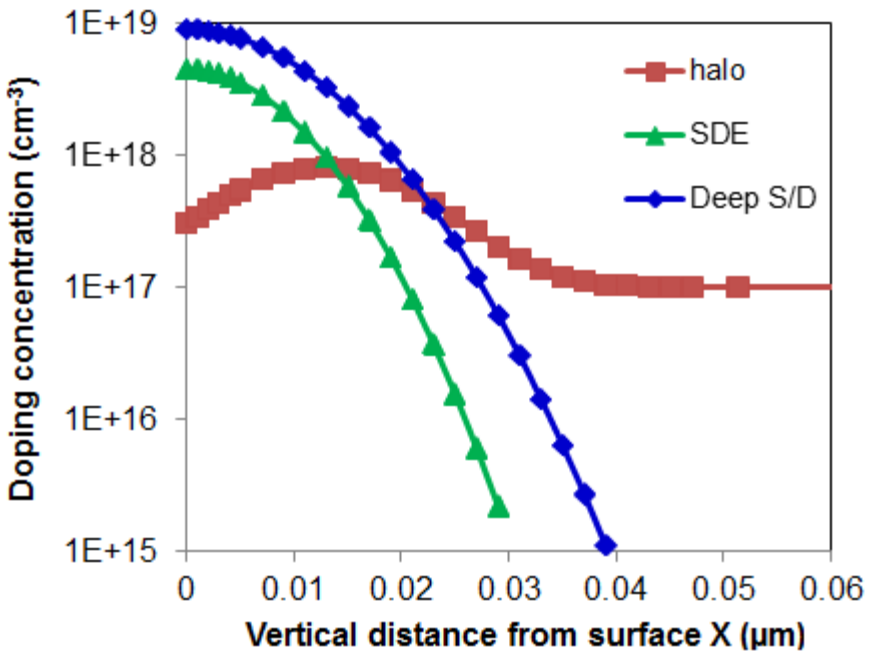

Fig.7.1. 1D Doping profile for the extension, SD and halo implants by taking a vertical cut at the S/D.

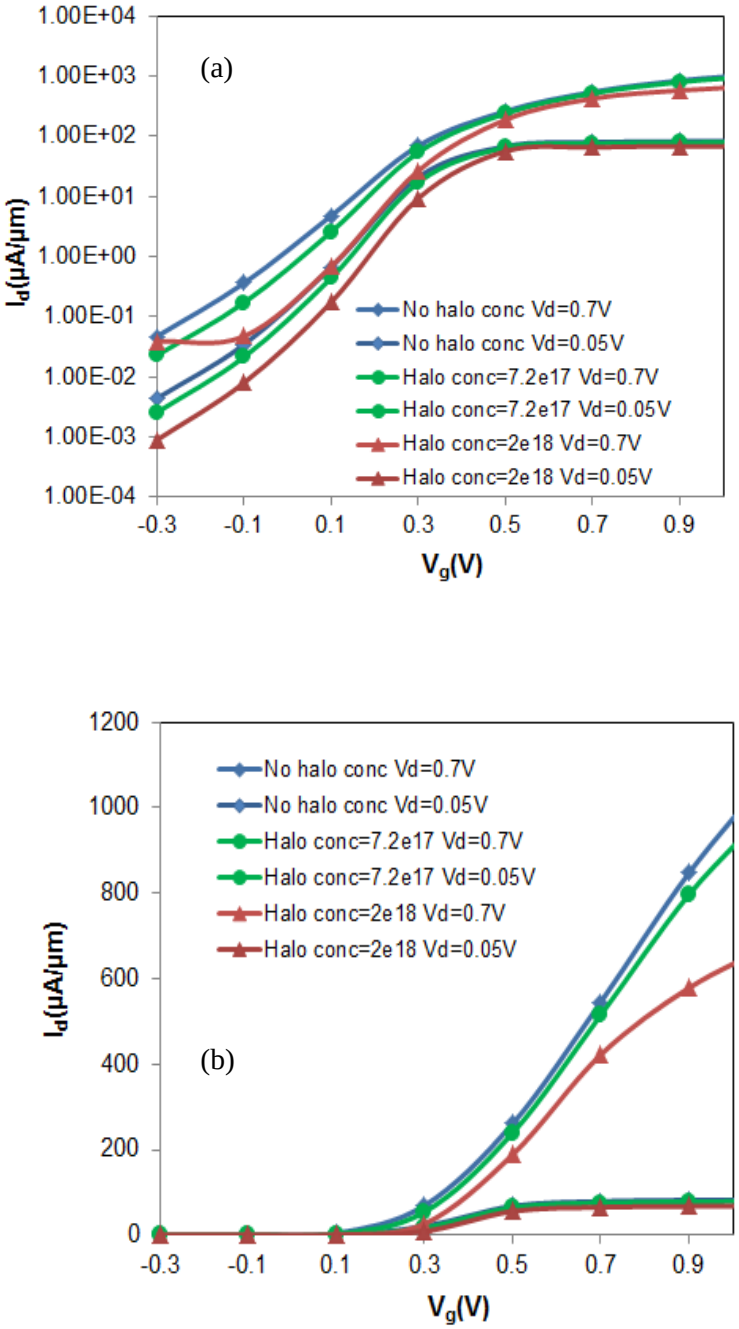

Fig.7.2 (a) I_d-V_g plot for plasma-PH_3/N_2 passivated L_g=70nm device with and without halo implant and (b) I_d-V_g plot in linear scale for plasma-PH_3/N_2 passivated device with and without halo implant. For devices with halo implant, the peak concentration is given by $7.2x10^{17}cm^{-3}$ and $2x10^{18}cm^{-3}$.

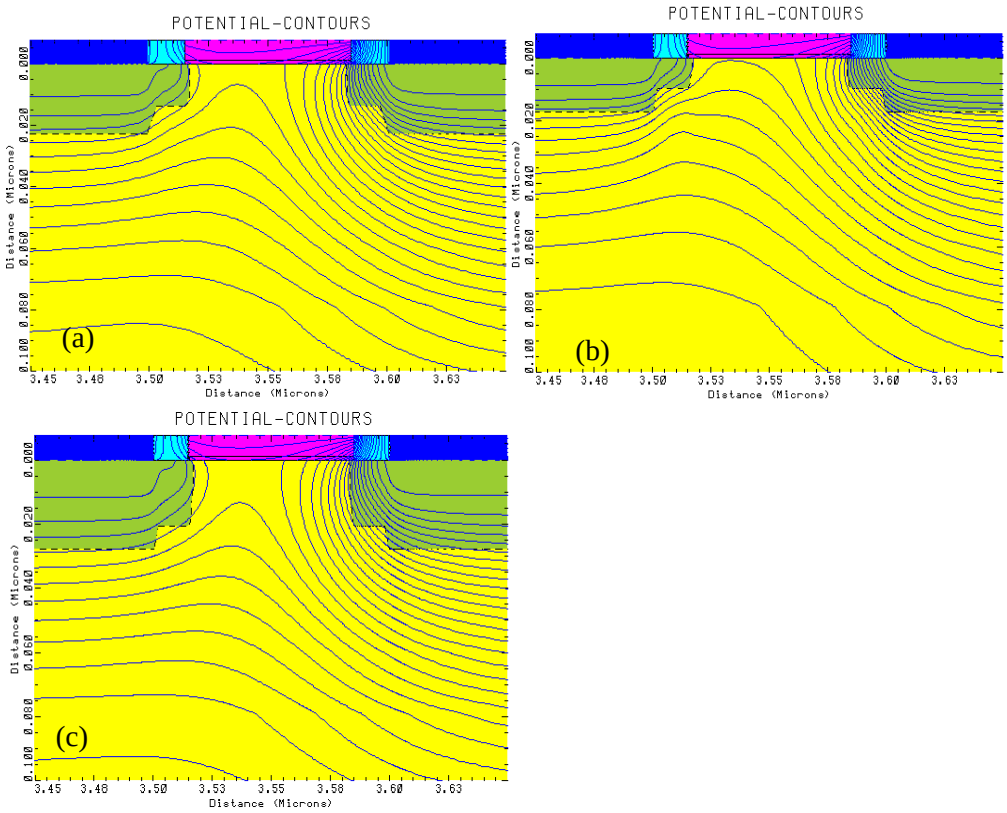

Fig.7.3. 2D potential contours at V_g=0V and V_d=0.7V, for L_g=70nm (a) with halo implant ($7.2x10^{17}cm^{-3}$) and (b) with halo implant ($2x10^{18}cm^{-3}$) and (c) without halo implant.

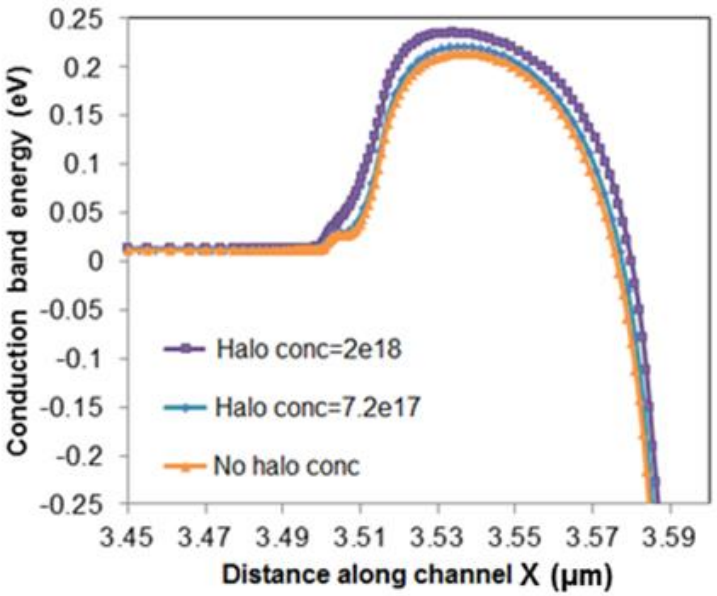

Fig.7.4. Conduction band energy profile as a function of distance along the channel taken at 1nm below the $P_xN_y/In_{0.53}Ga_{0.47}As$ interface for V_d=0.7V at V_g=0V.

However, as halo doping increases, GIDL current increases which can be clearly seen from the increased generation rate contours from the 2D plot in Fig.7.5, attributed to higher halo doping concentration near the edge of the channel. The min to max generation rate is defined as $1x10^{25}cm^3/s$ to $1x10^{29}cm^3/s$ with 5 contour lines, with a lateral mesh spacing of 0.2nm at regions close to the S/D to channel edge so that the energy band diagram would represent the true effects caused by GIDL. From Fig.7.6 it is found that the minimum tunnelling width between channel and drain regions for halo implant of $2x10^{18}cm^{-3}$ is 22.7nm while it is 29nm for halo implant of $7.2x10^{17}cm^{-3}$. The smaller tunnelling width of device with halo implant of $2x10^{18}cm^{-3}$ initiates more tunnelling of electrons from the valence band of the channel to the conduction band of the drain, resulting in greater GIDL. Hence, this shows that despite improvement in electrostatic integrity with higher halo doping concentration, this increase in drain leakage may present a difficulty for planar $In_{0.53}Ga_{0.47}As$.

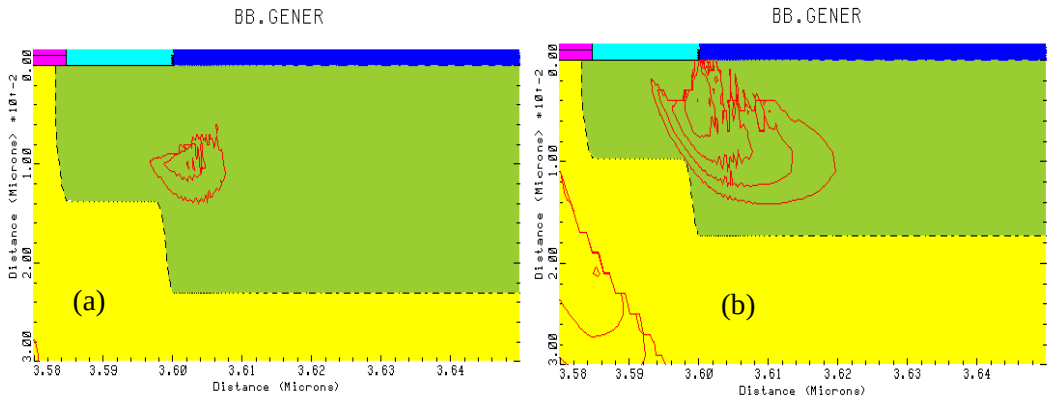

Fig.7.5. Simulation 2D BTBT generation contours at V_g=-0.3V and V_d=0.7V, for L_g=70nm (a) with halo implant ($7.2x10^{17}cm^{-3}$) and (b) with halo implant ($2x10^{18}cm^{-3}$).

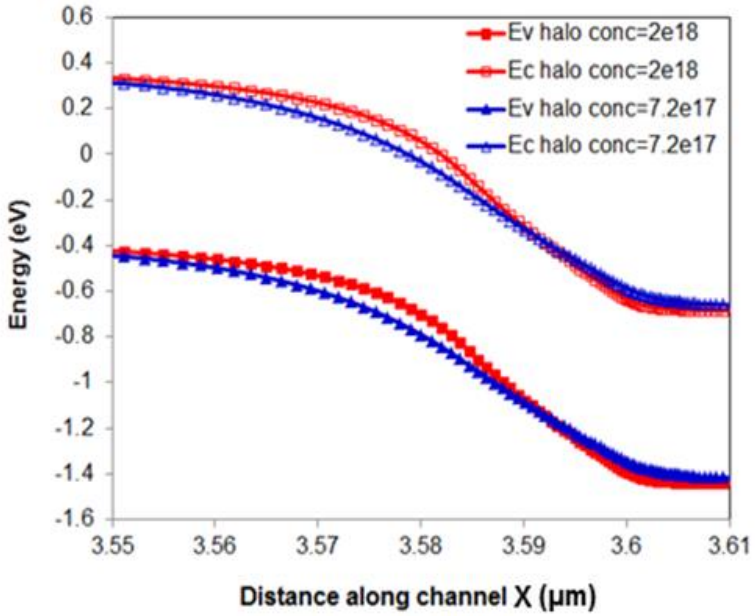

Fig.7.6. Band diagram in the lateral direction for plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$ MOSFETs with two different halo implant conditions, taken at V_g=-0.3V, V_d=0.7V at maximum BTBT generation point. From 1D profile, maximum BTBT generation occurs at x=3.6µm, y=0.01µm for Fig.7.5(a) and at x=3.6µm, y=0.004µm for Fig.7.5(b).

7.3. Raised S/D $In_{0.53}Ga_{0.47}As$ MOSFET

High mobility $In_{0.53}Ga_{0.47}As$ N-MOSFETs require shallow, abrupt and highly doped N+ S/D. Most $In_{0.53}Ga_{0.47}As$ transistors use S/D implantation through the use of Si as the n-type dopant because of its negligible diffusivity which allows the realization of very abrupt junctions. However, the maximum n-type carrier concentration in $In_{0.53}Ga_{0.47}As$ with Si as dopants can only reach ~$1x10^{19}cm^{-3}$ by direct Si implantation due to the low solid solubility limitation [14-15]. This doping level is far from the state-of-art doping concentration (in the order of 10^{20} cm^{-3}) achieved for Si and thus $In_{0.53}Ga_{0.47}As$ transistors will suffer more from S/D series resistance as compared with Si transistors. Thus, one of the motivations of studying regrown S/D MOSFET is to reduce the contact resistance through heavy in-situ doping during the selective epitaxy growth to obtain lower R_c. In addition, the higher

source doping concentration, together with its enlarged volume over which scattering can redirect carriers into longitudinal *k*-states, is expected to solve the source starvation issue, which is one of the results of DOS bottleneck present in $In_{0.53}Ga_{0.47}As$ devices.

The aim of this section is to investigate the effectiveness of RSD in reducing the source starvation issue through comparison with optimized halo-ISD MOSFET. In addition, the logic technology figures of merit (SS, $V_{t,sat}$, DIBL, I_{on}/I_{off} ratio, injection velocity (V_{inj}) and switching delay) would also be studied to show significant improvement on device scalability with RSD.

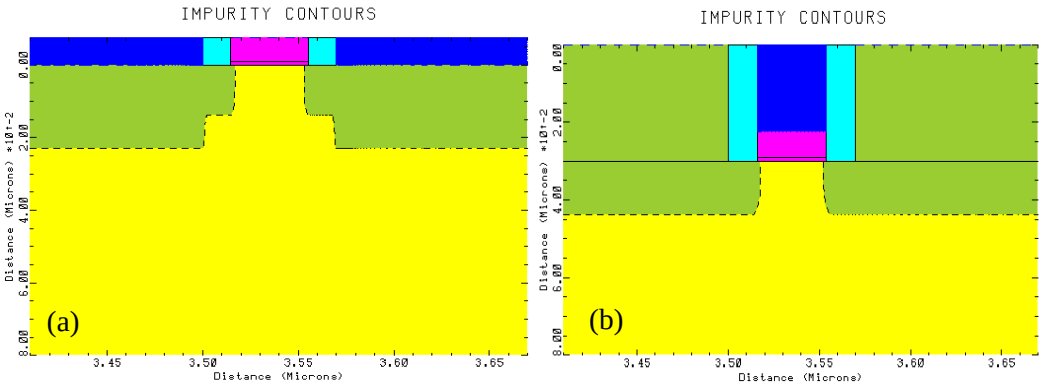

Fig.7.7. 2D plots of the (a) Implanted S/D MOSFET and (b) Raised S/D MOSFET used in the simulation

The ISD and RSD device structures both use a 15nm wide Si_3N_4 spacer, with contact resistance of 400Ω.μm [13], as well as halo and SDE. Also RSD structure here uses 30nm thick $6.5x10^{19}cm^{-3}$ doped S/D and with InP material to benefit from its band discontinuity which can result in higher carrier concentration in the channel [16]. RSD MOSFET does not include the deep S/D because of the RSD structure already present. Both structures are shown in Fig.7.7(a) and Fig.7.7(b). SDE is still needed for RSD because extensions of undoped $In_{0.53}Ga_{0.47}As$ below the sidewall spacers might

introduce extra series resistance to the MOSFET. Comparison with and without SDE at V_g-$V_{t,sat}$=0.5V, V_d=0.7V (recommended by ITRS) at EOT=0.6nm for L_g=50nm device taken at 1nm below the $P_xN_y/In_{0.53}Ga_{0.47}As$ interface showing the amount of carrier concentration along the channel direction is shown in Fig.7.8. V_d value between 0.5V to 0.8V is acceptable based on the ITRS 2011 recommendation for III-V devices [17-18] because high applied voltage (V_d=1.0V) can cause the energy of carriers to be larger than the energy separation between Γ and *L* valley (due to the low density of states in the $In_{0.53}Ga_{0.47}As$ and is given as 0.46eV) which increases the contribution of *L* valley's electrons in the electron transport. This can reduce the device performance due to low mobility of the electrons in the *L* valley [19].

It is seen from Fig.7.8 that without SDE, electron spill over from the N+ source layer which provides the necessary carriers under the sidewall spacer is insufficient to provide sufficiently large on-state performance of the device. The amount of electron concentration under the spacer is only $1.2x10^{18}cm^{-3}$, at the lowest point between the beginning and end of spacer for without SDE, compared to $3.6x10^{18}cm^{-3}$ with SDE added, thus resulting in larger access resistance. The amount of inversion electron concentration (N_{inv}) inside the channel is also larger with presence of SDE, implying that source starvation, can be reduced. This reduction in electron concentration below the spacer is also not completely compensated by the increase of the velocity shown in Fig.7.9. The average velocity inside the channel is almost the same for both SDE and without SDE, possibly due to the enhanced channel field being offset by a reduction in the injection velocity from the source due to increased impurity scattering for the structure with SDE [20]. Hence, due mainly to lesser effect of source starvation in structure with SDE, the drive

current with SDE is increased from 177.6μA/μm to 586.8μA/μm for with SDE over that without SDE.

Other than the use of SDE and reducing the spacer width to increase the electron concentration below the spacer, the use of pulse doping in the back barrier or recessed/undercut regrowth of SD below the sidewall can provide more electrons in this region to reduce the source access resistance [11,21].

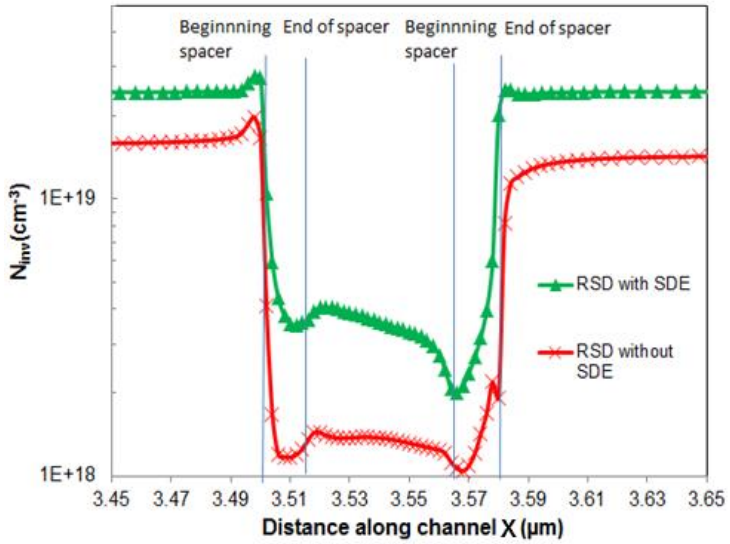

Fig.7.8. Inversion electron concentration at 1nm below $P_xN_y/In_{0.53}Ga_{0.47}As$ interface taken along the channel direction at V_g-$V_{t,sat}$=0.5V, V_d=0.7V for L_g=50nm for EOT=0.6nm.

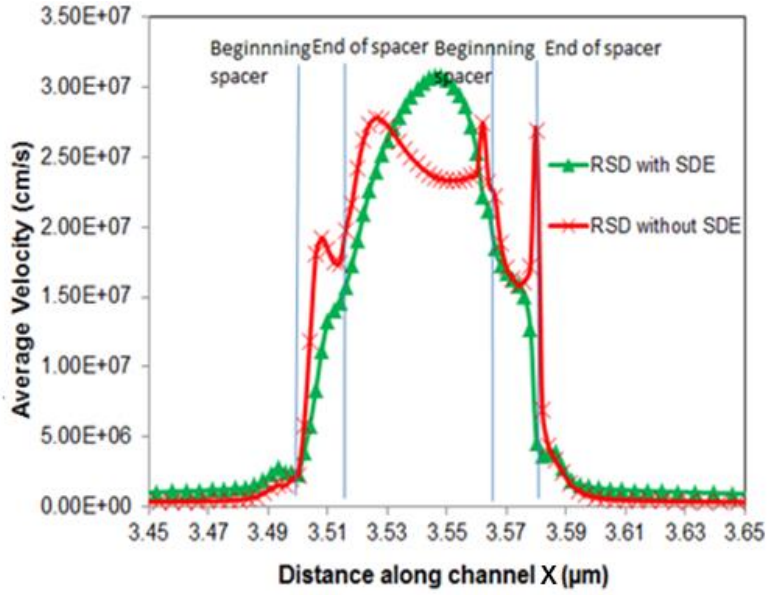

Fig.7.9. Average electron velocity along the channel of the $In_{0.53}Ga_{0.47}As$ MOSFET taken at 1nm below $P_xN_y/In_{0.53}Ga_{0.47}As$ interface and at V_g-$V_{t,sat}$=0.5V, V_d=0.7V for L_g=50nm, EOT=0.6nm.

7.3.1. Source starvation and Performance Scalability of RSD vs ISD Devices

Fig.7.10 plots the performance of both ISD and RSD devices with scaling, as a function of different EOT to show the improvement to the device performance brought about by improved gate control. ISD shows smaller drive current compared to RSD for the same device gate length, reflecting the source starvation effects more dominant in ISD MOSFETs. RSD has higher potential of mitigating this source starvation effect and this can be seen from Fig.7.11(a) which plots N_{inv} vs distance along channel comparing ISD and RSD for L_g=50nm at EOT=0.6nm showing that the inversion electron carrier concentration inside the channel is larger for RSD. This is because RSD has higher doped source which supplies more carriers which can be scattered and redistributed into the channel direction [20]. In addition, the geometry of the RSD structure itself increases the acceptance cone which thus effectively enlarges the volume over which scattering can redirect carriers into the longitudinal states [9]. On the other hand, the average velocity inside the channel is almost unchanged for RSD and ISD devices described in Fig.7.11(b). Thus, due to the smaller source starvation effect in RSD, the drive current of RSD MOSFET significantly increased compared to ISD MOSFET. In addition from Fig.7.10, ISD shows larger drive current degradation with scaling, reflecting the poorer SCE relative to RSD MOSFET.

Despite the $I_{d,sat}$ degradation with device scaling, the intrinsic gate delay given as CV/I improves with scaling, where it is calculated using C_{ox}*L*V_d/$I_{d,sat}$. However, the values are still considerably larger compared to ITRS of only 0.13ps for L_g=22nm at V_d=0.7V. Hence, to further improve driving capability, the use of lower contact resistance achievable in InP RSD

[16], compared to ISD, and also thinner channel thus with increased quantum confinement, will be useful to be studied as shown in the next section.

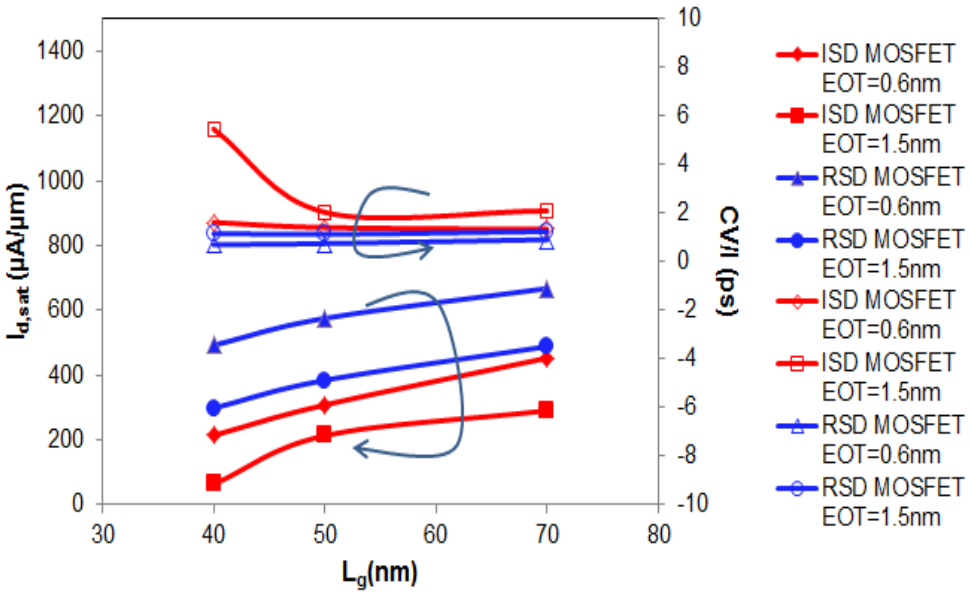

Fig.7.10. Channel length and EOT dependences of $I_{d,sat}$ and CV/I shows far better performance of RSD over conventional ISD. $I_{d,sat}$ taken at V_d=0.7V, V_g-$V_{t,sat}$=0.5V.

The improvement in threshold voltage roll off and DIBL (difference in threshold voltage measured at V_d=0.7V and V_d=0.05V) of RSD is also shown in Fig.7.12. The addition of RSD prevents the need for the deep S/D, thus reducing the total donor doping concentration near the channel. The potential contours plot, seen in Fig.7.13 which is taken at L_g=50nm for V_d=0.7V and V_g=0V, shows that there are less potential contour lines contributed by the S/D into channel, hence improving the DIBL. Further analysis of the conduction band energy plot in Fig.7.14 reveals the larger barrier height that needs to be overcome by the electrons as it enters the channel, in the RSD MOSFET compared to the ISD MOSFET, thus explaining the better short channel effect behaviour of the RSD MOSFET. In addition, due the contribution of deep SD concentration, the total donor concentration near the edge of the spacer is

larger for ISD MOSFET resulting in the electron flow lines to exist at the region close to the spacer while RSD MOSFET has electron flow lines starting and ending at the region only beyond the spacer shown in Fig.7.15, hence further explaining the DIBL improvement. The relationship between I_{on} and I_{off} was also investigated in Fig.7.16 showing the benefits of RSD structure. SS is improved by the addition of RSD due to the better gate control on the channel potential.

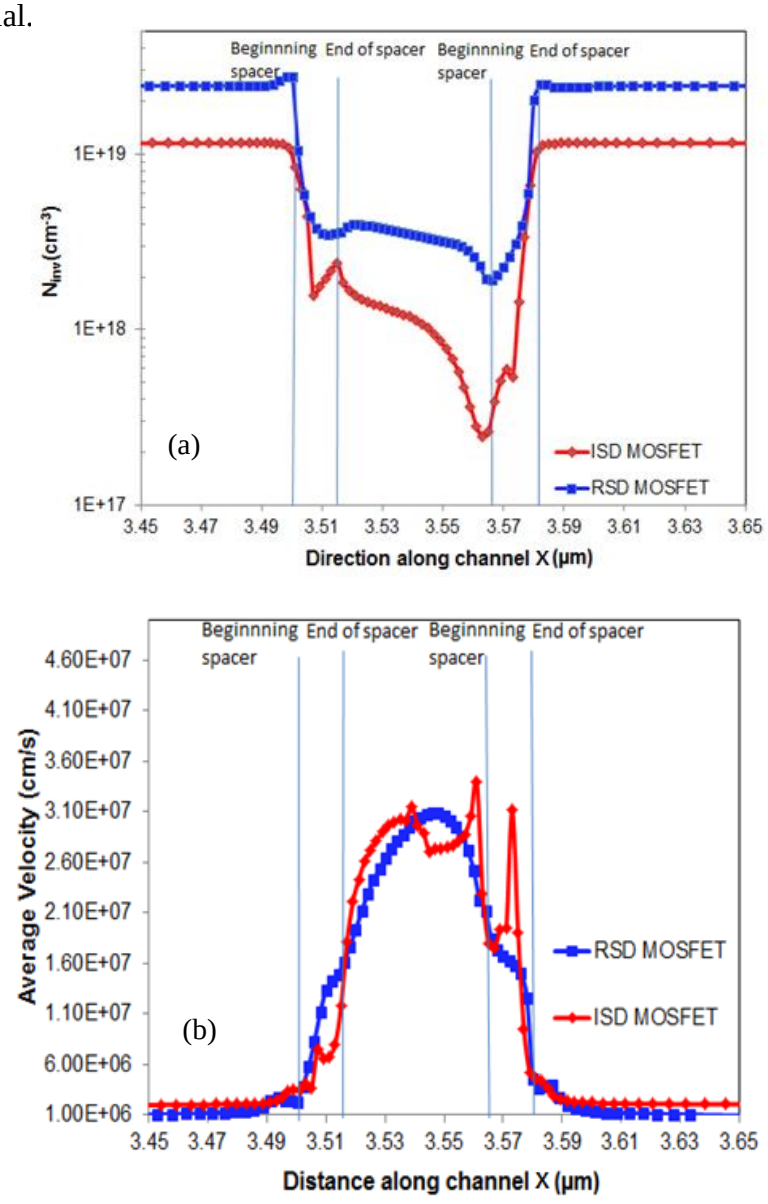

Fig.7.11 (a) Comparison of inversion electron concentration between RSD and ISD MOSFETs, where L_g=50nm, V_g-$V_{t,sat}$=0.5V and V_d=0.7V and (b) Comparison of average electron velocity between RSD and ISD MOSFETs, where L_g=50nm, V_g-$V_{t,sat}$=0.5V and V_d=0.7V.

Hence, simulation of $In_{0.53}Ga_{0.47}As$ MOSFETs have shown the potential of RSD in reducing source starvation in comparison to ISD implant structure, which results in improvement of drive current performance down to 40nm. In addition the use of RSD also allows improvement in short channel characteristics due to absence of deep S/D and improved gate control. In the next two sections, we will then focus on how thin channel can help in further reducing the source starvation issue and improving the electrostatic integrity

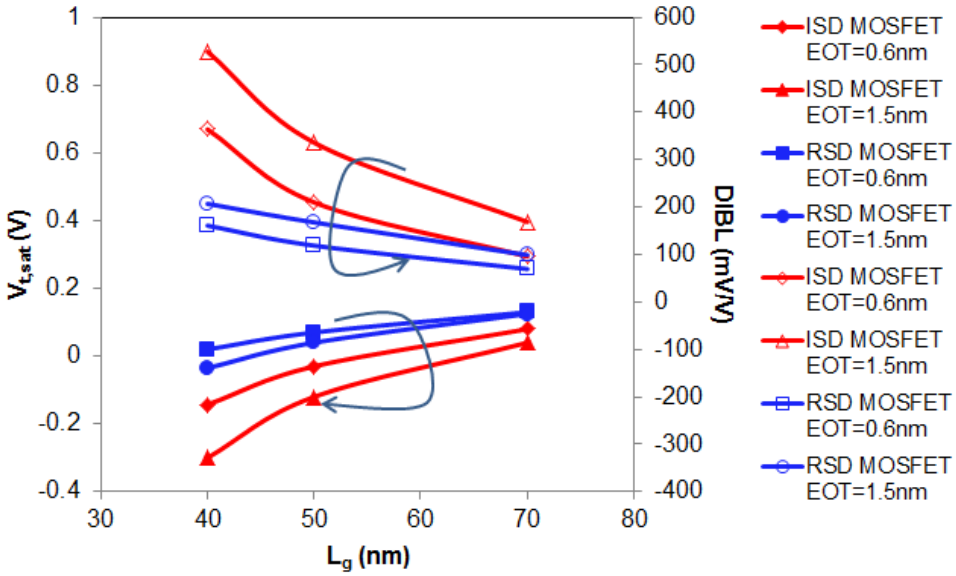

Fig.7.12. Plot of $V_{t,sat}$ and DIBL vs L_g for RSD and conventional ISD structures showing reasonable DIBL for RSD at 50nm.

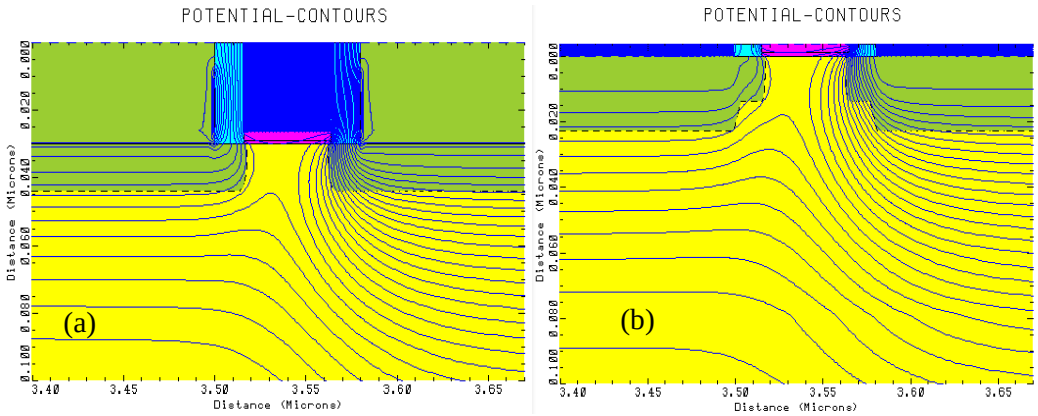

Fig.7.13. 2D potential contour plot of (a) RSD $In_{0.53}Ga_{0.47}As$ MOSFET and (b) ISD $In_{0.53}Ga_{0.47}As$ MOSFET for L_g=50nm taken at V_g=0V, V_d=0.7V.

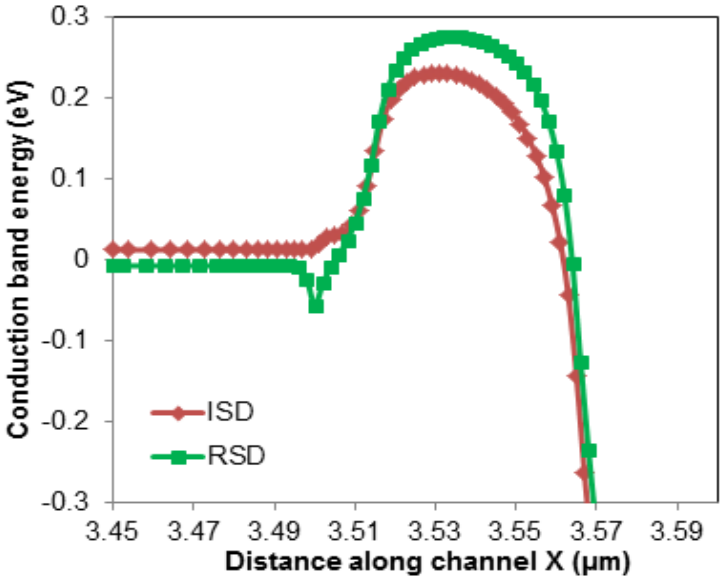

Fig.7.14. Conduction band energy profiles for RSD $In_{0.53}Ga_{0.47}As$ MOSFET and ISD $In_{0.53}Ga_{0.47}As$ MOSFET for L_g=50nm taken at V_g=0V, V_d=0.7V and taken at 1nm below the $P_xN_y/In_{0.53}Ga_{0.47}As$ interface.

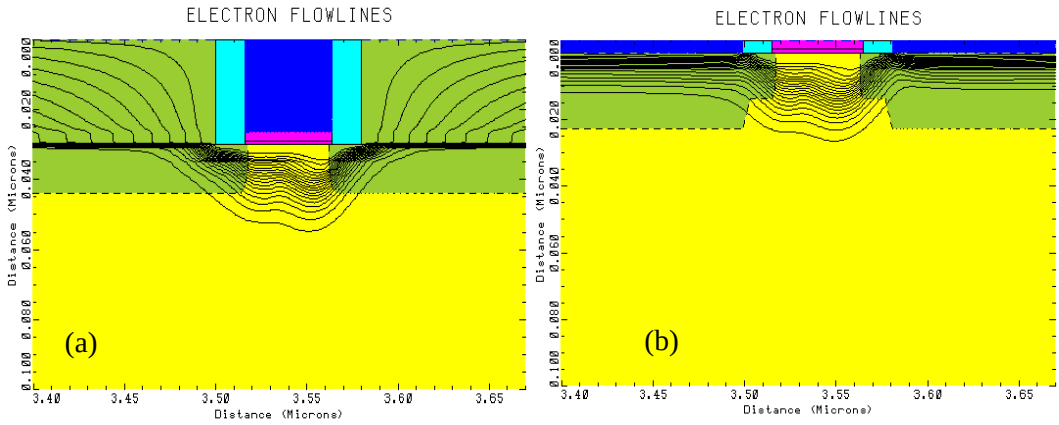

Fig.7.15. Electron flowlines for (a) RSD $In_{0.53}Ga_{0.47}As$ MOSFET and (b) ISD $In_{0.53}Ga_{0.47}As$ MOSFET for L_g=50nm taken at V_g=0V, V_d=0.7V. Electron flowlines in (a) do not start from within the spacer at the source unlike in (b).

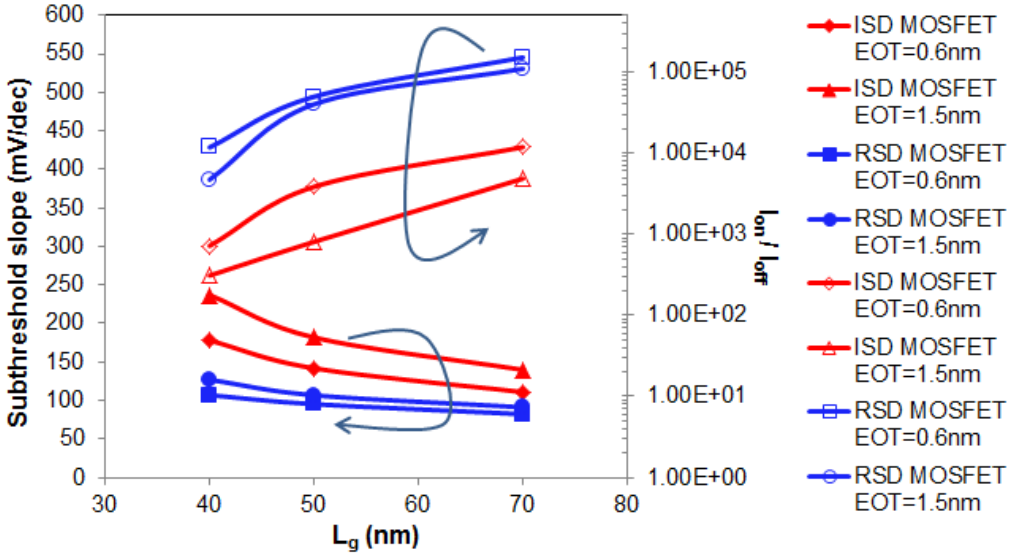

Fig.7.16. Plot of SS and I_{on} /I_{off} ratio vs L_g for RSD and ISD N-MOSFETs.

7.4. Performance Scaling with Raised S/D and $In_{0.53}Ga_{0.47}As$ Thin Channel MOSFET

Previous sections have shown that SCE in $In_{0.53}Ga_{0.47}As$ is one of the most important effects limiting MOSFET scalability, and to achieve sub-50nm gate length, very high body doping is required. However, high doping in the channel region is harmful to the device performance in both thick and thin body substrates due to mobility degradation [22-23]. Besides significant

mobility degradation, the high body doping also leads to the issue of band-to-band tunneling which is dependent on electric field and also energy bandgap. Therefore, with the limitations imposed on the doping levels on thin channel MOSFETs, lightly doped (p-type $5x10^{15}cm^{-3}$) $In_{0.53}Ga_{0.47}As$ thin channel MOSFET with lightly doped buffer layer (p-type $5x10^{15}cm^{-3}$) and without halo doping would be studied.

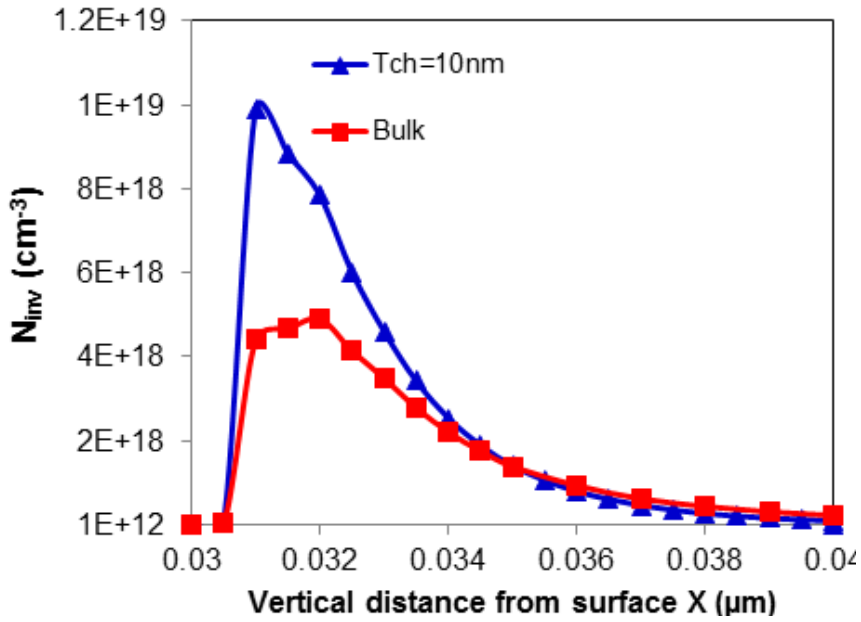

Fig.7.17. Electron density distribution in the inversion layers for $In_{0.53}Ga_{0.47}As$ bulk and thin channel MOSFET for L_g=40nm at EOT=0.6nm. Note that 0.03µm corresponds to the $P_xN_y/In_{0.53}Ga_{0.47}As$ interface and vertical distance from surface refers to distance away from $P_xN_y/In_{0.53}Ga_{0.47}As$ interface. Plot has been taken at the center of the channel.

A 10nm $In_{0.53}Ga_{0.47}As$ thin channel MOSFET up till L_g=40nm has been studied with contact resistance of 93Ω.µm achievable for raised S/D structure [2]. Fig.7.17 shows larger peak electron concentration in the inversion layer with thin channel, due to reduced width of inversion layer caused by larger quantum confinement, compared to bulk device.

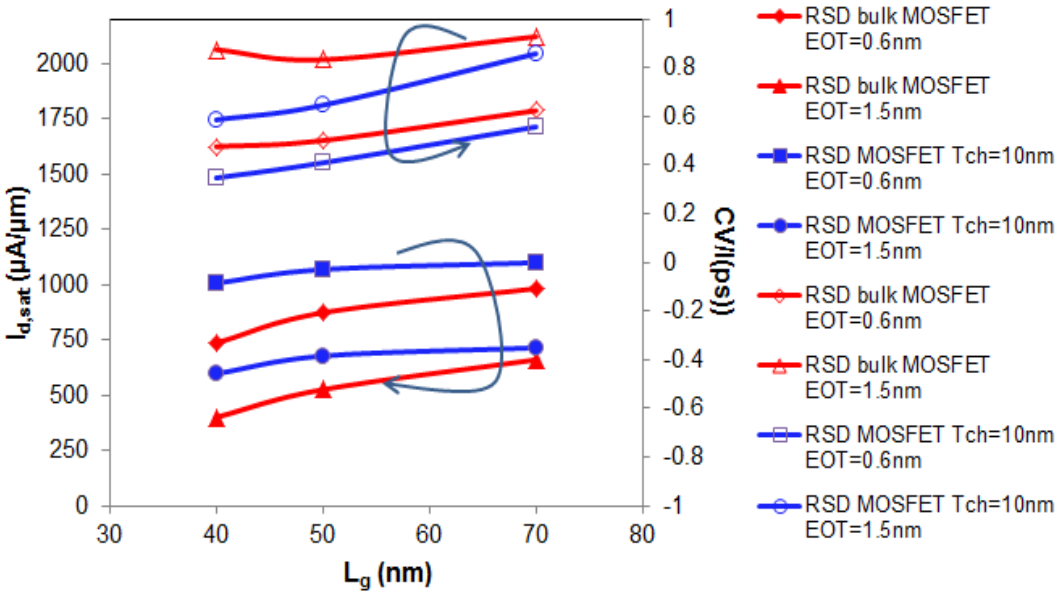

Fig.7.18. Channel length and EOT dependences of $I_{d,sat}$ shows better performance of thin channel $In_{0.53}Ga_{0.47}As$ MOSFET over bulk channel.

The device scaling capability of the thin channel structure in comparison to that of bulk MOSFET is studied in Fig.7.18. From this investigation, it is found that MOSFET with T_{ch}=10nm is effective in improving device performance compared to that of bulk MOSFET due to its potential of mitigating the source starvation effect. The fact that the inversion layer being closer to the gate as well as reduced inversion layer width in thin channel seen in Fig.7.17, could contribute to the increase in C_{inv} and hence C_g. Thus this results in the higher N_{inv} for the thin channel structure. This can be seen in Figs.7.19(a)-(b) and Figs.7.20(a)-(b) where it summarizes the method used to extract the N_{inv} and injection velocity metric respectively [24]. It is seen that a decrease in V_{inj} is observed for thin channel at the top of barrier (ToB), shown in circle in Fig.7.20(a) compared to bulk device in Fig.7.20(b). However under the same bias condition, a larger N_{inv} is observed for thin channel shown in Fig.7.19(a) compared to Fig.7.19(b). This increase of N_{inv} at the ToB overwhelms the effects of the lower injection velocity since the drain

current can be expressed as $I_d=q*V_{inj}*N_{inv}$ where q is the elementary charge. Hence, $I_{d,sat}$ performance of thin channel device is still higher despite the reduction in injection velocity. This reduced V_{inj} in thin channel may be due to the increased quantum confinement in the channel layer that increases the back-scattering rate which further reduces the velocity along the channel [19]. In addition, it is seen that the decrease of $I_{d,sat}$ with device scaling is significantly reduced with thin channel structures as seen in Fig.7.18. This implies the importance of increased N_{inv} near the source in addition to improved SCE to ensure increase in $I_{d,sat}$ with device scaling.

In addition, the $V_{t,sat}$ roll off and DIBL characteristics of the thin channel vs bulk structure as a function of EOT is shown in Fig.7.21. MOSFETs with thin channel exhibit lower $V_{t,sat}$ roll off and DIBL compared to bulk structure, and that EOT scaling is still effective to achieve good electrostatic characteristics. The reason for the larger $V_{t,sat}$ for thin channel compared to bulk is caused by the presence of quantum mechanical confinement of carriers in the thin channel layer which increases the sub-band energy level. Also, the lower SS in Fig.7.22 further shows the improvement in the electrostatic integrity of the thin channel MOSFET compared to bulk MOSFET. Fig.7.22 also shows the improvement in I_{on}/I_{off} caused by the improved on-current of thin channel MOSFET.

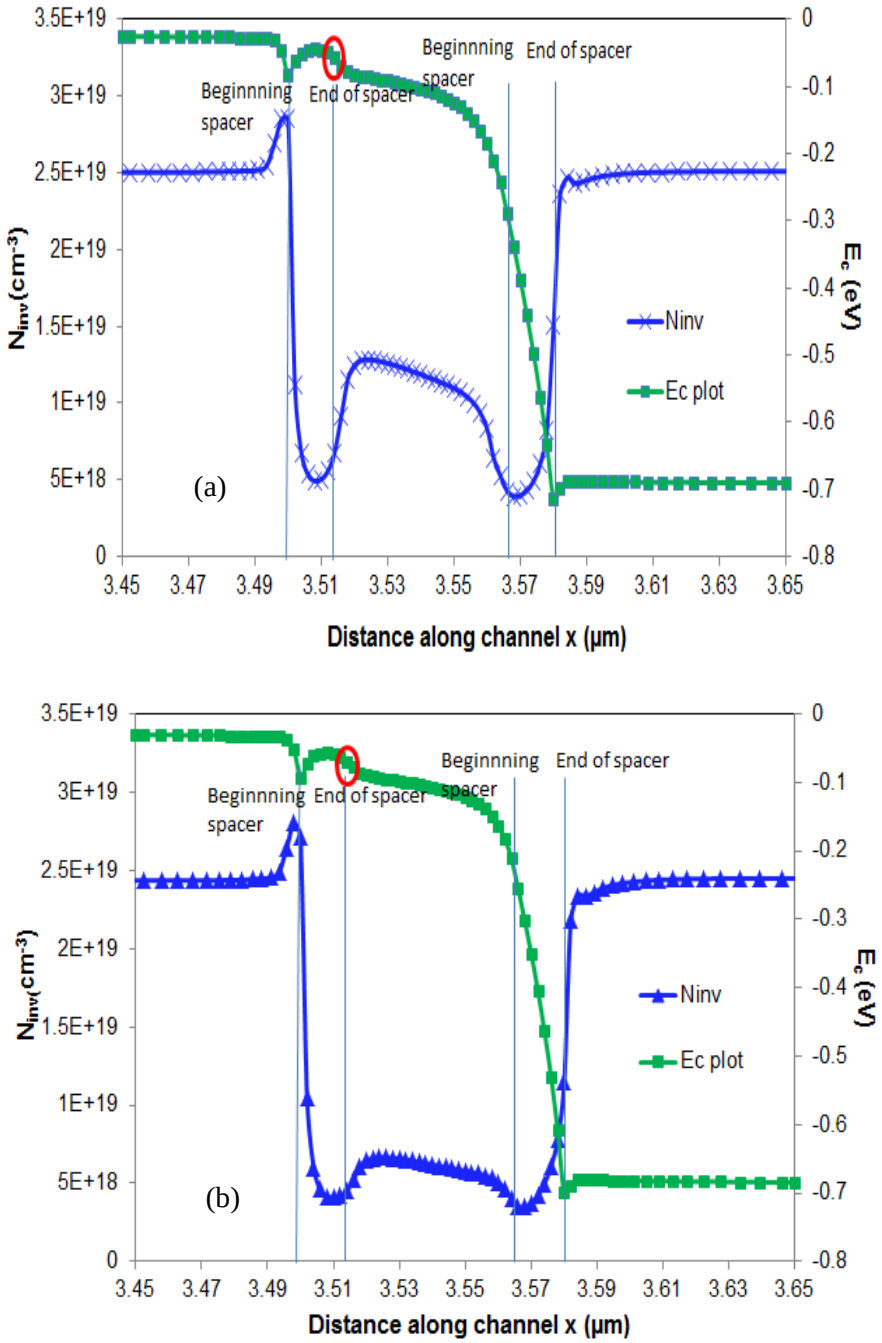

Fig.7.19 (a) Inversion electron concentration along the channel for T_{ch}=10nm structure for L_g=50nm, V_g-$V_{t,sat}$=0.5V and V_d=0.7V at EOT=0.6nm and (b) Inversion electron concentration along the channel for bulk structure for L_g=50nm, V_g-$V_{t,sat}$=0.5V and V_d=0.7V at EOT=0.6nm.

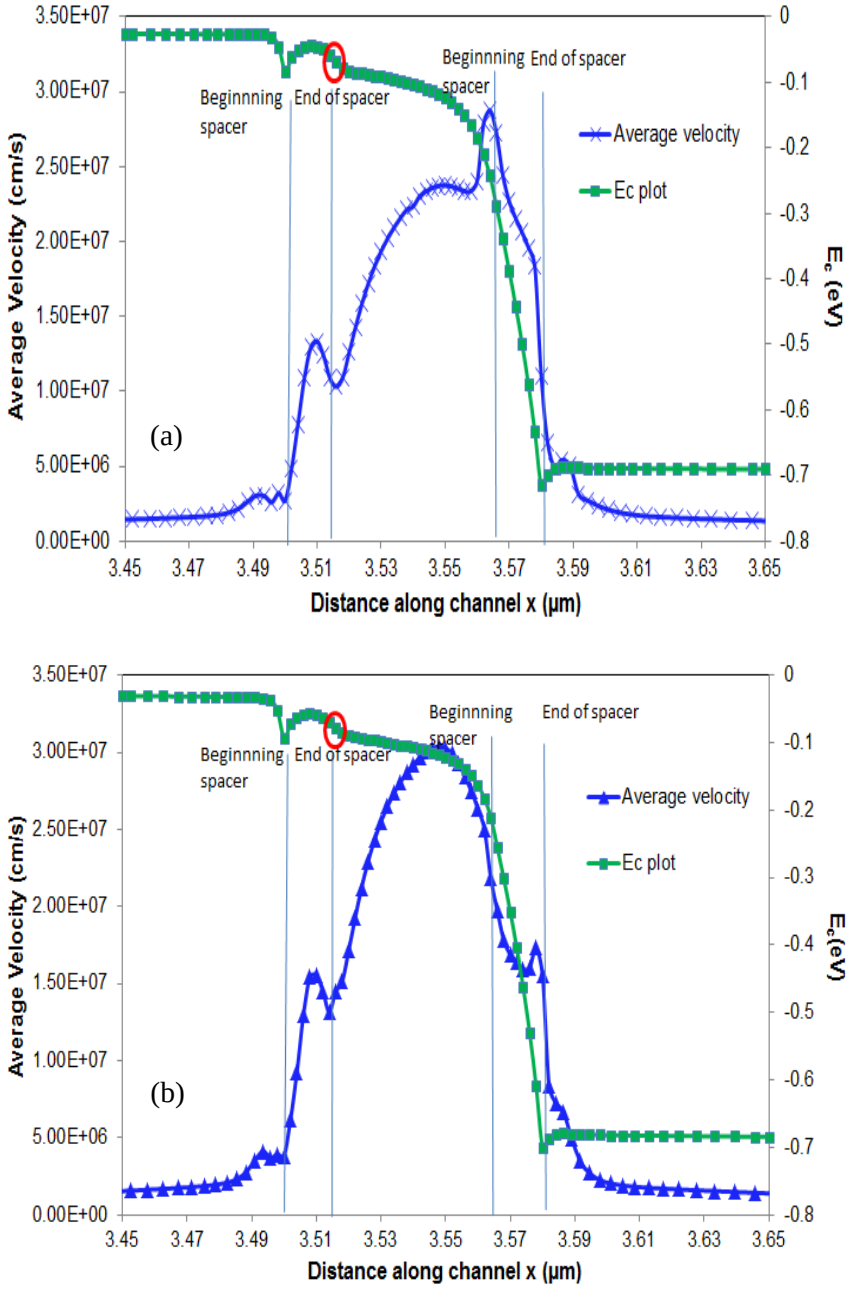

Fig.7.20 (a) Average electron velocity along the channel for T_{ch}=10nm structure for L_g=50nm, V_g–$V_{t,sat}$=0.5V and V_d=0.7V at EOT=0.6nm and (b) Average electron velocity along the channel for bulk structure for L_g=50nm, V_g-$V_{t,sat}$=0.5V and V_d=0.7V at EOT=0.6nm.

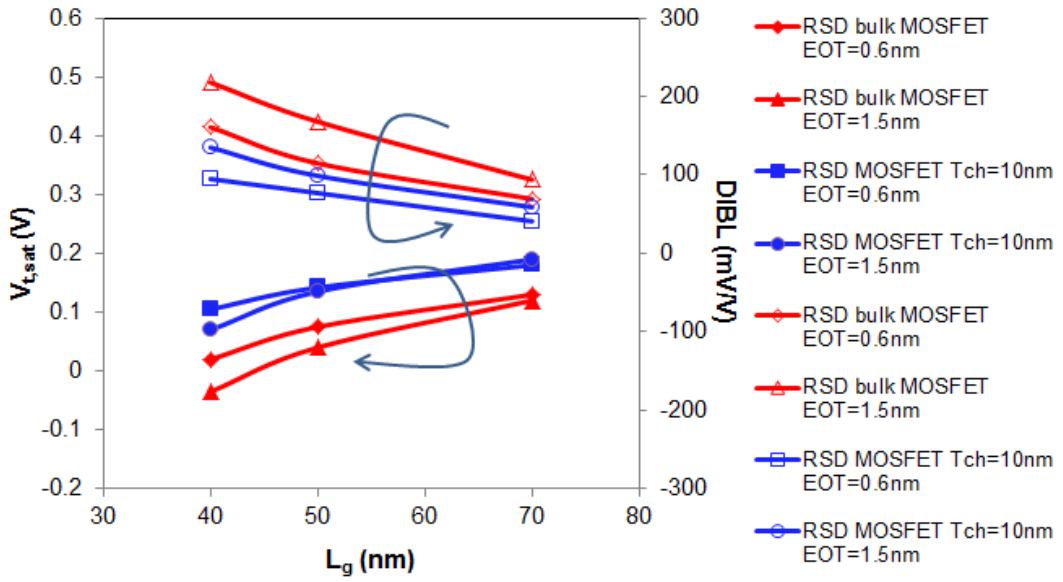

Fig.7.21. Plot of $V_{t,sat}$ and DIBL vs L_g for thin channel and bulk $In_{0.53}Ga_{0.47}As$ MOSFET.

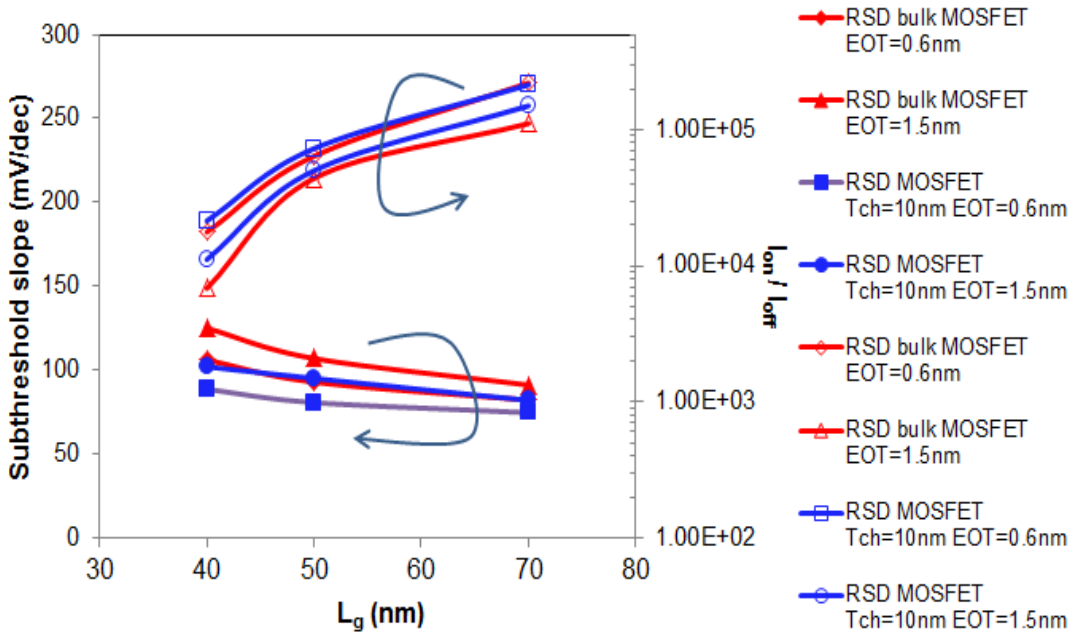

Fig.7.22. Plot of SS and I_{on} /I_{off} ratio vs L_g for RSD bulk and thin channel MOSFETs.

7.5. Optimization of $In_{0.53}Ga_{0.47}As$ MOSFET Device Structures for Performance Scalability up till Sub-22nm Technology Node

Despite the improvement in electrostatic integrity and device performance with the use of thin channel=10nm as shown in the previous section, the DIBL of L_g=40nm is already large at ~95mV/V even with EOT=0.6nm shown in Fig.7.21. In order for future scaling to sub-22nm to continue with acceptable electrostatic integrity given by leakage of 0.1μA/μm at V_g=0V, and $I_{d,sat}$=2A/mm at V_d=0.7V and V_g-$V_{t,sat}$=0.5V as predicted by ITRS 2011, further device engineering is needed. This includes studies on further scaling of channel thickness, the addition of heterostructure layer for acceptable $I_{d,sat}$ as well as spacer material for GIDL reduction. All these changes are made with the aim of predicting the $In_{0.53}Ga_{0.47}As$ performance of 22nm to 14nm gate length device.

The design of the device needed for sub-22nm is mentioned based on the device architecture for each part of the device which has been explained in the first few sections. First, raised S/D is necessary to help alleviate source starvation effects by increasing the chance of electrons to occupy the longitudinal *k*-states near the channel. Second, unintentionally doped thin channel with unintentionally doped InP buffer layer, is required to improve the SCE without affecting the mobility and hence I_{on} of the device. Hence, based on these, a cross section of the baseline structure is shown in Fig.7.23, with the gate dielectric chosen as EOT=0.6nm. The top $In_{0.53}Ga_{0.47}As$ channel layer will be varied from 12nm to 3nm as shown in Section 7.5.1 as well as addition of top and bottom $In_{0.52}Al_{0.48}As$ capping layer to form heterostructure device as shown in Section 7.5.3.

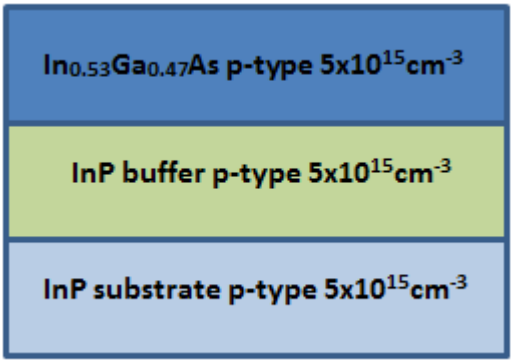

Fig.7.23. Device design of the structure simulated.

The performance of the device which includes $I_{d,sat}$, DIBL and SS have been systematically studied based on the different variations from the baseline structure. The variations are with 1) Effects of reduced T_{ch} 2) Spacer material to improve GIDL and 3) Addition of $In_{0.52}Al_{0.48}As$ top and bottom capping layer (Heterostructure Device). Finally, the structure would be compared and benchmarked to the structures simulated by other groups. Based on the ITRS roadmap, III-V technology devices have V_d of between 0.5 to 0.8V and hence, V_d=0.7V has been studied for this section.

7.5.1. Effect of Thinner channel

As T_{ch} reduces to 3nm, the $I_{d,sat}$ at the same I_{off} of 0.1µA/µm increases as seen in Fig.7.24. The performance enhancement is due to the smaller inversion layer thickness owing to the physical confinement of the electron wave function within the quantum channel. To demonstrate this, Fig.7.25 shows the electron distributions in the inversion layers computed for each device structure with the gate bias voltages given as 0.7V and drain voltage set at 0.7V. The electrons are seen to be confined in the ultrathin channel region by the InP buffer layer, thus causing the inversion layer width to decrease

leading to increase of inversion layer capacitance and hence gate capacitance. Therefore the drive current in the thin channel MOSFET increases as T_{ch} reduces. The improvement of DIBL and SS as a function of T_{ch} is shown in Fig.7.26. DIBL and SS is smaller as T_{ch} reduces due to minimum electric field from the drain penetration contributing to reduction of potential contours from the S/D to the channel shown in Fig.7.27(a) and Fig.7.27(b) and higher potential barrier from the source to the channel in Fig.7.28 for T_{ch}=3nm compared to T_{ch}=12nm. The SS improves with reduced T_{ch} due to the stronger quantum confinement which moves the peak of the inversion layer width towards the high-*k*/$In_{0.53}Ga_{0.47}As$ interface which improves the gate control [25].

The channel thickness of 3nm is chosen because severe SCE is observed with T_{ch} of 5nm especially at L_g=14nm. The SS and DIBL of T_{ch}=3nm $In_{0.53}Ga_{0.47}As$ MOSFET does not significantly degrade as the L_g reduces, while the SS characteristics of T_{ch}=5nm and 12nm start to degrade significantly when L_g drops below 22nm and 28nm respectively. This is due to improved SCE control with thinner channel.

However, one expected issue with scaling of channel thickness is the excessive quantization effect in thinner body (especially less than 5nm) that can cause carriers to travel in the higher mass L valley, where the % contribution of electrons in the drive current from the L valley can be as high as 18% for T_{ch}=3nm for V_d =1V, at gate overdrive=0.7V [26]. This effect can result in degradation in device performance. However, due to the lower supply voltage of 0.7V used in this work, it is expected that insignificant contribution of L valley electrons to the operation of the $In_{0.53}Ga_{0.47}As$ device. In order to reduce this quantization effect, other device structures that can achieve high I_{on}

and acceptable SCE without using channel thickness below 5nm is needed in order for $In_{0.53}Ga_{0.47}As$ to be competitive over Si. They include structures like double gate MOSFET and FINFET.

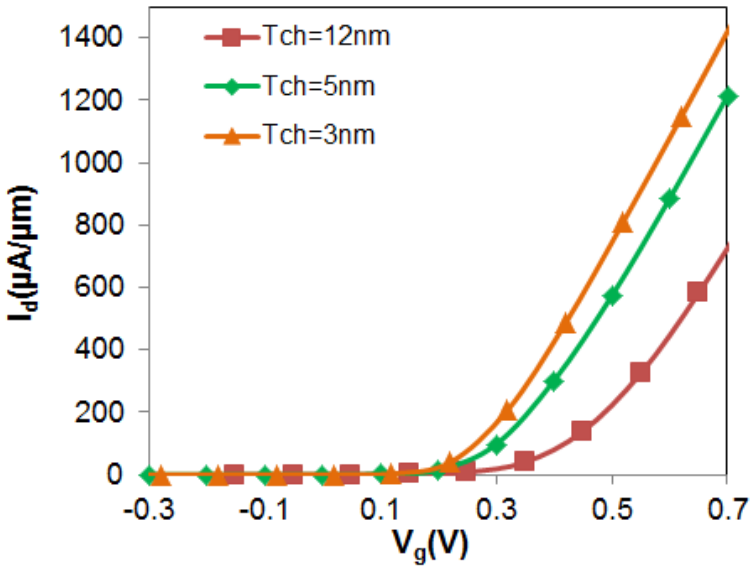

Fig.7.24. I_d-V_g plot as a function of channel thickness for V_d=0.7V at fixed I_{off} of 0.1μA/μm.

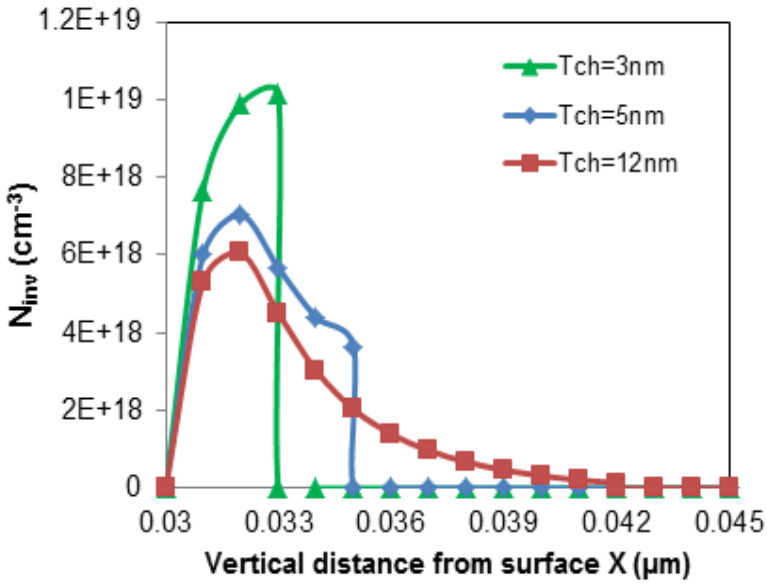

Fig.7.25. Electron density distributions in the inversion layers computed for thin channel MOSFETs as a function of channel thickness at V_d=0.7V, V_g=0.7V. These profiles have been extracted at the middle of the channel region.

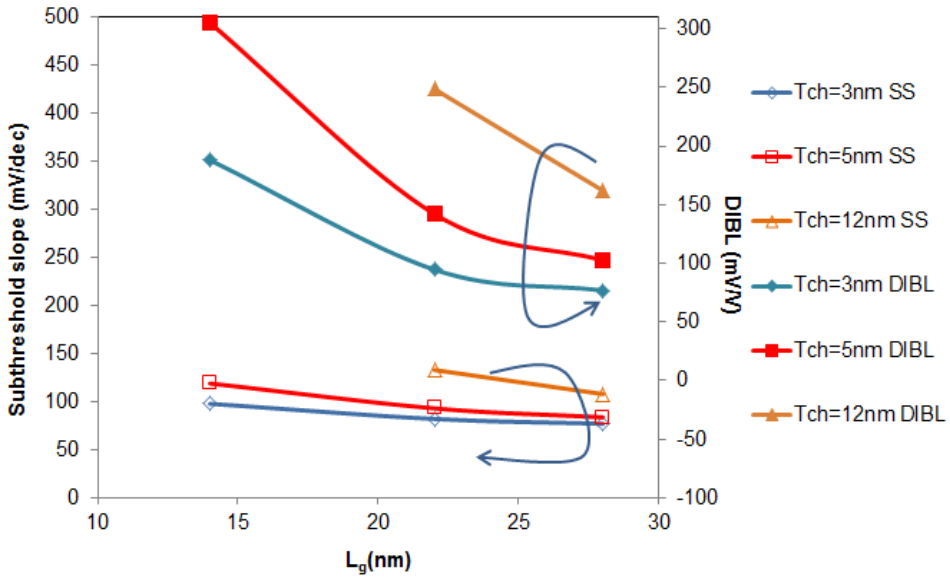

Fig.7.26. SS and DIBL vs L_g characteristics as a function of channel thickness.

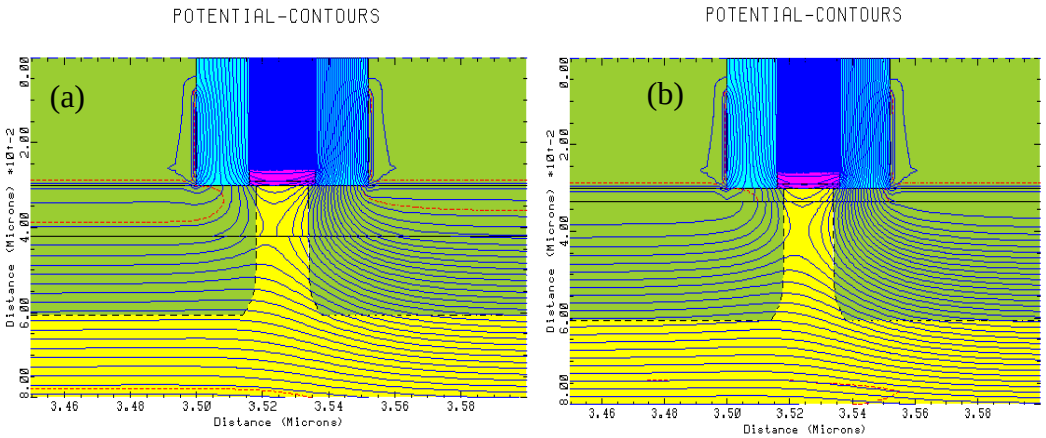

Fig.7.27. Potential contours for L_g=22nm with (a) T_{ch}=12nm and (b) T_{ch}=3nm taken at V_d=0.7V, V_g=0V.

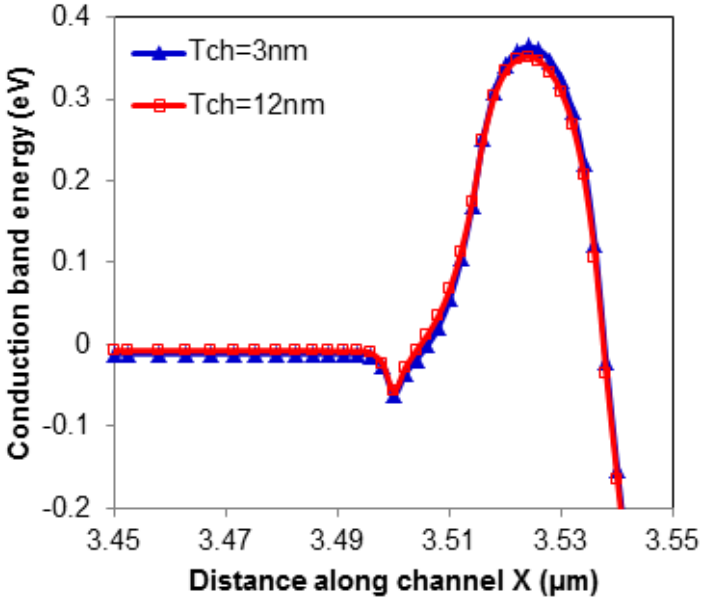

Fig.7.28. Conduction band energy vs distance along the channel comparing T_{ch}=12nm and T_{ch}=3nm for L_g=22nm device taken at V_d=0.7V, V_g=0V.

7.5.2. Effect of Spacer Material

Figs.7.29(a)-(c) shows the three different MOSFET structures used for the analysis of the GIDL characteristics. The structure in Fig.7.29(a) has a high-*k* dielectric and Si_3N_4 spacers used in the simulations studied so far, while Fig.7.29(b) has high-*k* gate dielectric extended to the bottom of the spacers and in Fig.7.29(c) both the gate oxide and spacer are of high-*k* HfO_2 material. In this section of the simulation work, the physical gate length is fixed at 22nm.

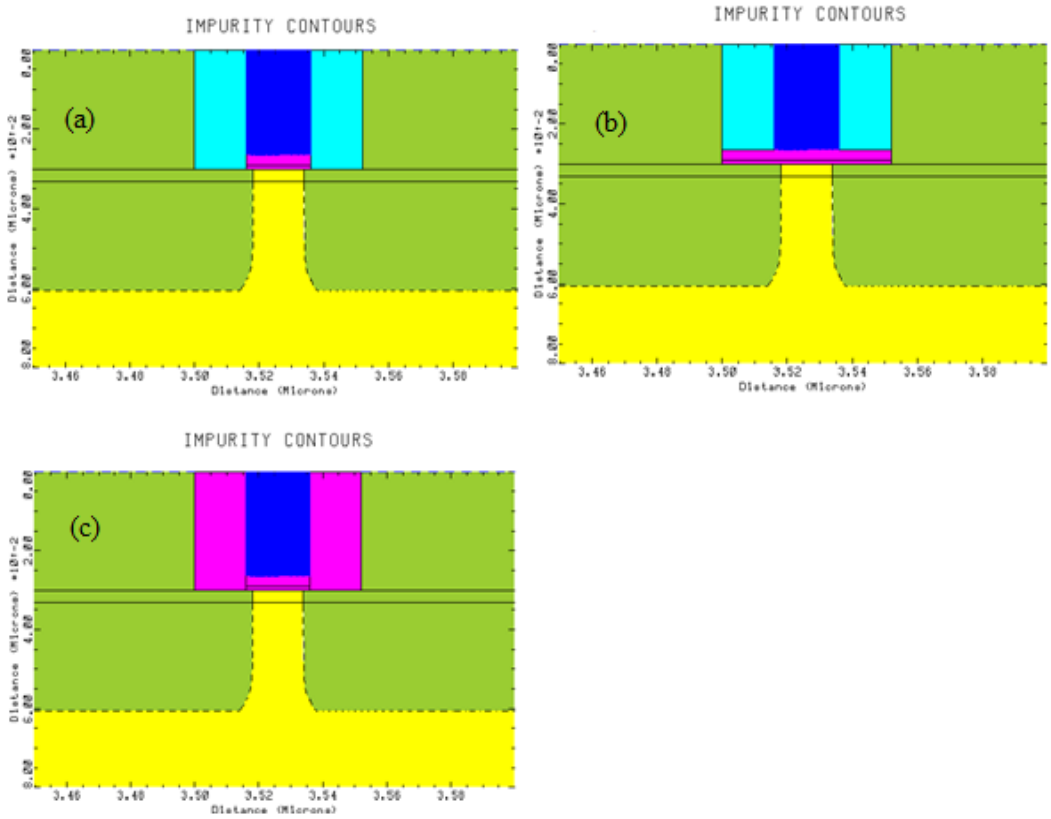

Fig.7.29 Three different spacer material used on the $In_{0.53}Ga_{0.47}As$ MOSFET structures with T_{ch}=3nm simulated with (a) Si_3N_4 spacer (b) HfO_2 extended to regions below spacer (c) HfO_2 spacer.

Effect of spacer material will affect GIDL as shown in Fig.7.30. Comparison has been made in terms of spacer material on off-state leakage and DIBL. The device structure in which the spacer is made up of high-*k* HfO_2 material, shown in Fig.7.29(c), showed the smallest GIDL current while the device structure with the spacer being made up of Si_3N_4 shown in Fig.7.29(a) showed the worst GIDL. This can be explained from the E-field contour plot in Fig.7.31. Fig.7.32 shows that the lateral electric field taken from the structure of Fig.7.31(a) gives the largest peak field with the least spread-out field profile unlike electric field plot of structure taken from Fig.7.31(c). Hence, GIDL for device HfO_2 spacer gives the least GIDL.

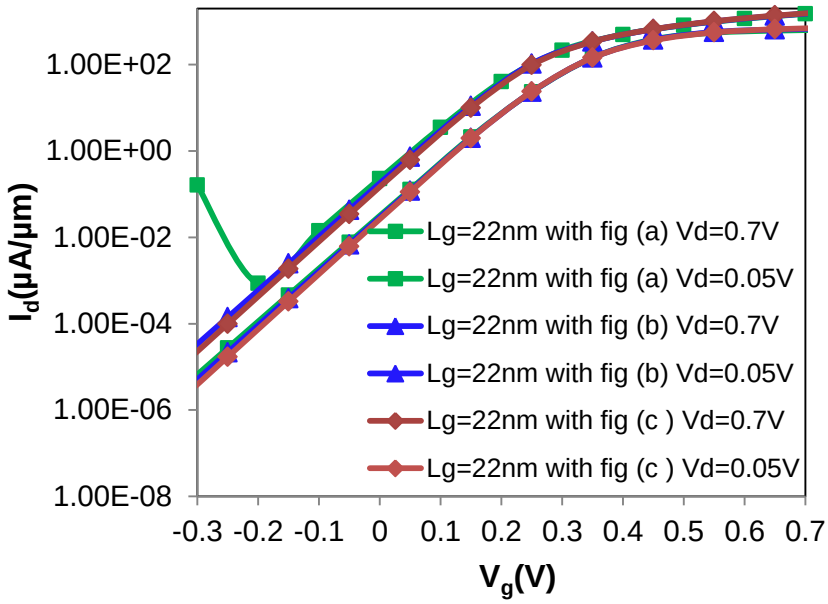

Fig.7.30. I_d-V_g characteristics showing DIBL and GIDL with comparison with the three types of spacer material.

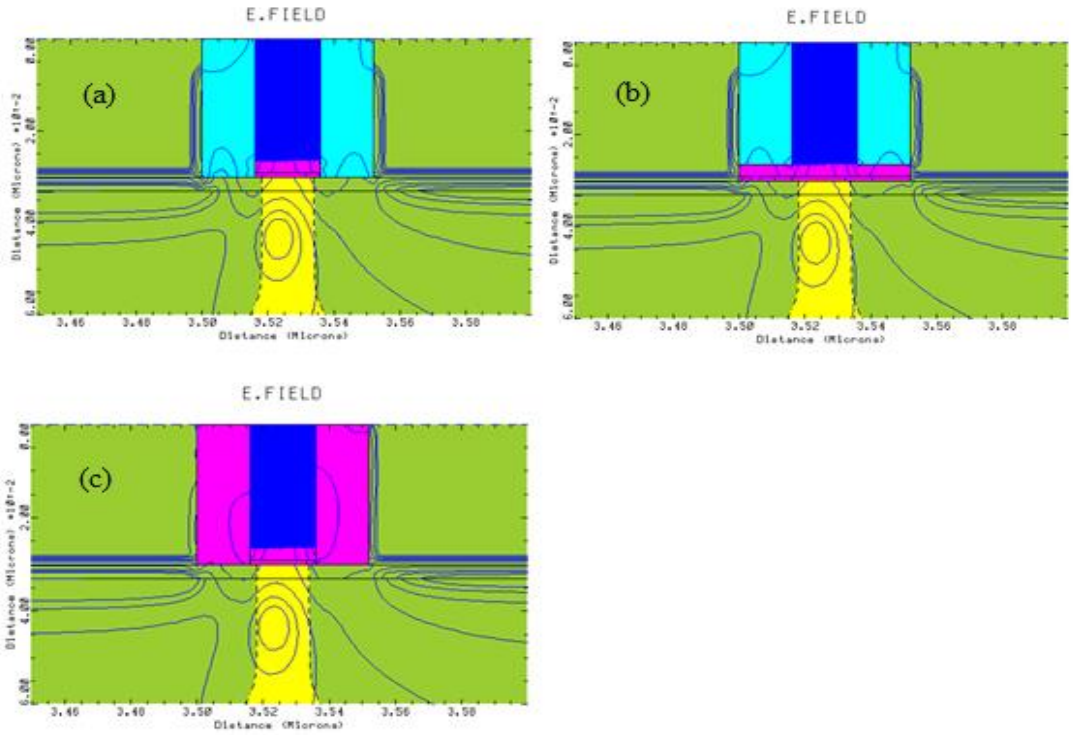

Fig.7.31. 2D electric field plot taken at V_g=-0.3V, V_d=0.7V comparing the structure with three different spacer materials with (a) Si_3N_4 spacer (b) HfO_2 extended to regions below spacer (c) HfO_2 spacer.

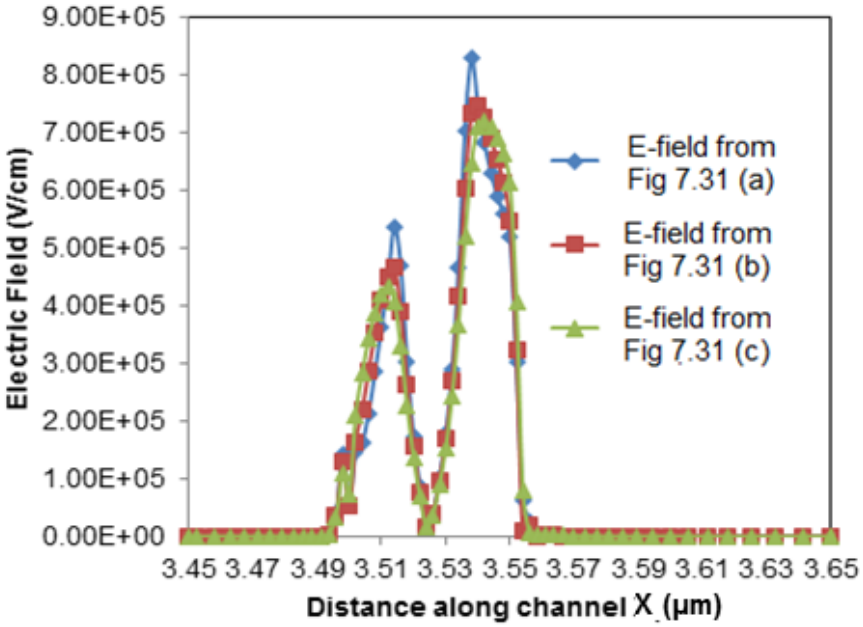

Fig.7.32. Electric field contours taken at 1nm below the $P_xN_y/In_{0.53}Ga_{0.47}As$ interface at the region along the channel with V_g=-0.3V and V_d=0.7V. Here the electric field taken from Fig.7.31(a), especially at the region of the channel/drain interface, shows the most focused and abrupt field while the electric field taken from Fig.7.31(c) shows a laterally spread field which is responsible for its smaller GIDL.

7.5.3. Effect of Heterostructure Device

In this structure, narrow bandgap $In_{0.53}Ga_{0.47}As$ material is sandwiched between the two wide-bandgap barrier layers with the channel confined at the heterostructure interface. The barrier layer used is $In_{0.52}Al_{0.48}As$ which has a conduction band offset of 0.48eV with the $In_{0.53}Ga_{0.47}As$. The III-V barrier layers are needed to provide (i) carrier confinement in the quantum well and (ii) minimized off-state leakage current. The heterostructure design with $In_{0.53}Ga_{0.47}As$ channel on wide bandgap $In_{0.52}Al_{0.48}As$ is used to cut down drain to body leakage to reduce I_{off} and to induce strong confinement to result in higher mobility. The wide bandgap top capping layer i.e. $In_{0.52}Al_{0.48}As$ layer between channel and dielectric, is used to insulate the channel charge from the effect of traps and scattering in the dielectric/III-V interface. It was kept

intentionally thin for this work at 1nm so as to avoid any spillover of charge from the channel layer with high mobility into the wide bandgap low mobility layer. Note that device with heterostructure would consist of top and bottom $In_{0.52}Al_{0.48}As$ capping layers i.e. layer 1 (a 1nm thick $In_{0.52}Al_{0.48}As$ capping layer between P_xN_y and $In_{0.53}Ga_{0.47}As$ channel layer) and layer 2 (1nm thick $In_{0.52}Al_{0.48}As$ barrier layer between $In_{0.53}Ga_{0.47}As$ channel layer and InP). This has been based on the design of III-V heterostructure double gate MOSFET [27] except that a single gate MOSFET has been simulated in this work. In addition, high-*k* spacers are used based on Section 7.5.2 where GIDL is reduced.

Reported from various groups which carried out experiments on heterostructure $In_xGa_{1-x}As$ MOSFETs, increment in mobility of the structures with capping layer is between 35% to 60% for 2nm InP/$In_{0.7}Ga_{0.3}As$ [28] and 1nm InP/$In_{0.7}Ga_{0.3}As$ [29] respectively caused by the reduced effect of D_{it} at the high-*k*/$In_xGa_{1-x}As$ interface. Thus we have chosen a 50% higher mobility in heterostructure than no heterostructure device for this work. This has been based on the reported 1nm InP/$In_{0.7}Ga_{0.3}As$ with CBO of 0.411eV [30]. Hence, $In_{0.52}Al_{0.48}As$/$In_{0.53}Ga_{0.47}As$ used in our work should have CBO of 0.48eV based on $In_{0.53}Ga_{0.47}As$ affinity of 4.51eV and $In_{0.52}Al_{0.48}As$ affinity of 4.03eV [30]. Since 1nm InP/$In_{0.7}Ga_{0.3}As$ with CBO of 0.411eV has an increase in mobility of 60%, our $In_{0.52}Al_{0.48}As$/$In_{0.53}Ga_{0.47}As$ with CBO of 0.479eV should have at least similar if not larger increase in mobility. However, this is assuming that $In_{0.52}Al_{0.48}As$ is not reactive with the high-*k* oxide, since it has been reported that $In_xAl_{1-x}As$ usually has the problem of excessive aluminium oxidation for ex-situ process [30]. Nevertheless, since P_xN_y capping layer

would be used as a barrier layer between high-*k* oxide and $In_{0.52}Al_{0.48}As$, this excessive reaction of $In_{0.52}Al_{0.48}As$ with the high-*k* oxide may be minimal.

The tradeoff of heterostructure device is that the gate to channel distance is increased leading to a reduced gate control over the channel, potentially degrading the short channel device performance. Subthreshold slope for 22nm device at V_d=0.7V is seen to increase from 78.6mV/dec to 82.7mv/dec while DIBL increases from 89.7mV/V to 115mV/V from Fig.7.33(a) for no heterostructure and heterostructure device respectively. However, the $I_{d,sat}$ at V_g-V_{th}=0.7V seen in Fig.7.33(b) linear scale is 2400μA/μm for heterostructure device and is given by 1950μA/μm for non-heterostructure device, which represents a 23% increase in $I_{d,sat}$ with the use of heterostructure.

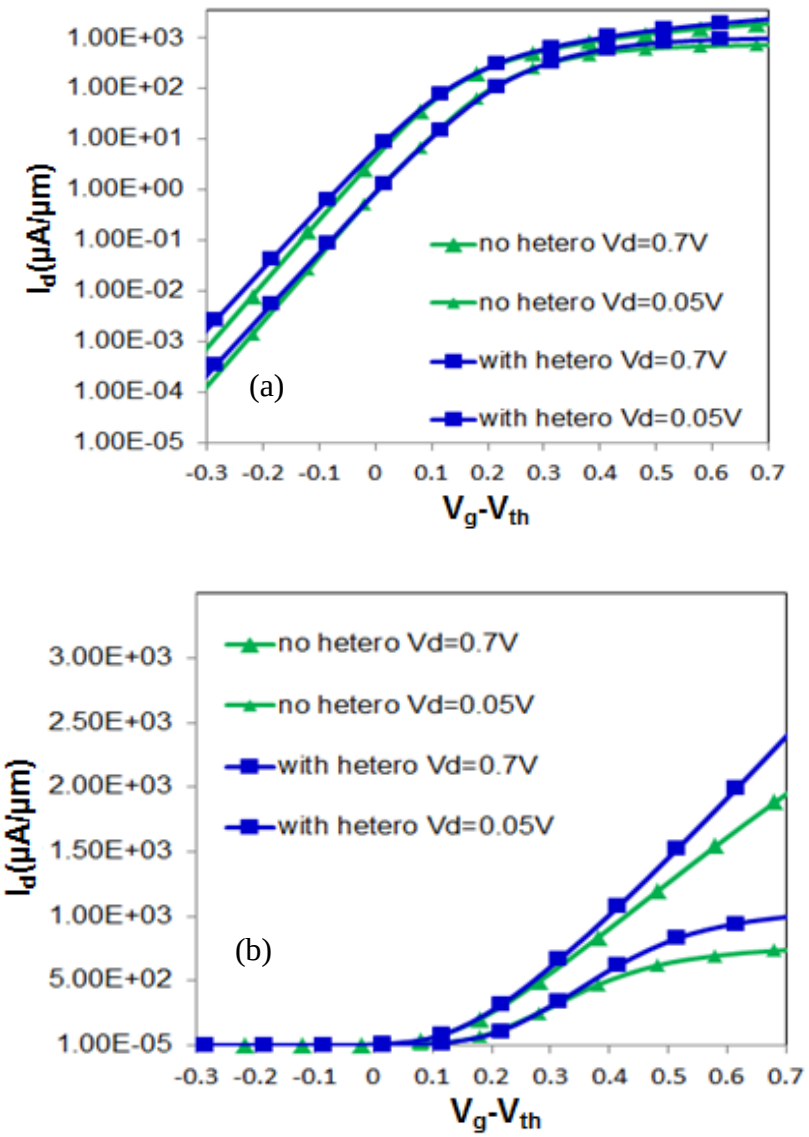

Fig.7.33. I_d–(V_g-V_{th}) plot for (a) V_d=0.7V and V_d=0.05V, for L_g=22nm devices with and without heterostructure in log scale and (b) V_d=0.7V and V_d=0.05V, for L_g=22nm devices with and without heterostructure in linear scale.

7.5.4. Performance Scalability of Device With and Without Heterostructure and Benchmarking

Thus based on the device advantages of optimizing certain parts of the device architecture discussed in previous sections, this section would make use of optimized structure with high-*k* spacer, at EOT=0.6nm, T_{ch}=3nm, with and without heterostructure for benchmarking with simulation works performed by other groups. The studies would involve gate lengths between 28nm to 14nm.

SCE is significantly suppressed in terms of $V_{t,sat}$ roll off and DIBL for devices without heterostructure seen in Fig.7.34. It can be observed for L_g=14nm, the DIBL of device without heterostructure is 147mV/V while heterostructure device has DIBL of 188.8mV/V. Fig.7.35 shows an increase of SS of device with heterostructure from 95.2mV/dec compared to 88.4mV/dec for device without heterostructure. The worsened electrostatic integrity of the device with capping layer is likely due to the increased CET caused by the presence of the lower *k* value of $In_{0.52}Al_{0.48}As$ capping layer between the P_xN_y and $In_{0.53}Ga_{0.47}As$ channel. The I_{on}/I_{off} for no heterostructure device shows a sufficiently large value of $5.94x10^5$ for L_g=14nm and $9.25x10^5$ for L_g=22nm implying the good electrostatic control with sufficiently large I_{on}. On the other hand, I_{on}/I_{off} of heterostructure device is smaller at $1.25x10^5$ for L_g=14nm and $5.18x10^5$ for L_g=22nm due to the worse electrostatic integrity compared to device without heterostructure.

Fig.7.36 shows $I_{d,sat}$ at V_d=0.7V, V_g-$V_{t,sat}$=0.5V is given by 945µA/µm and 1067µA/µm, and at V_g-$V_{t,sat}$=0.7V is given by 1600µA/µm and 1775µA/µm, for L_g=14nm and L_g=22nm respectively of device without heterostructure. On the other hand, device with heterostructure has $I_{d,sat}$ at V_d=0.7V, V_g-$V_{t,sat}$=0.5V given by 875µA/µm and 1160µA/µm, and at V_g-$V_{t,sat}$=0.7V given by 1670µA/µm and 2090µA/µm, for L_g=14nm and L_g=22nm respectively. These values are still smaller than ITRS which requires 2,200 µA/µm at supply voltage of 0.7V and gate overdrive of V_g-$V_{t,sat}$=0.5V for III-V NMOSFET. Hence, more improvements are still required such as increasing Indium concentration and changing device architecture to obtain the requirements set by ITRS. Despite the reduction in $I_{d,sat}$ with scaling, the CV/I intrinsic delay improves with scaling. The reduction in $I_{d,sat}$ with scaling is

likely contributed by the worsened electrostatic integrity (causing the significant $V_{t,sat}$ roll off) as seen in Fig.7.37. Here at longer channels where roll off is not significant i.e. from 160nm to 50nm, the $I_{d,sat}$ increases with smaller channel lengths. This shows the increasing need for improved device architecture to minimize SCE especially as L_g approaches the sub-22nm technology node in order to ensure continuous improvement in $I_{d,sat}$ with gate length scaling and hence improve device scalability. Such architectures may include FINFET, triple gate or double gate structures. Note that the Figs.7.34-7.37 have been taken from the plots of Figs.7.38(a)-(b) and Figs.7.39(a)-(b).

Table 7.1 benchmarking of this work performed with other simulation works in Ref [26] shows that this work has poorer electrostatic integrity due to lower p-type channel doping concentration of $5x10^{15}cm^{-3}$ compared to $2x10^{18}cm^{-3}$ in Ref [26] and also larger EOT of 0.6nm compared to 0.44nm in Ref [26]. Nevertheless, the electrostatic integrity obtained in this work is still acceptable, with higher $I_{d,sat}$ which has been reduced in Ref [26] caused by its higher channel doping concentration. This lower $I_{d,sat}$ is despite its larger RSD doping concentration of $1x10^{20}cm^{-3}$ and idealized contact resistance.

Comparison of this work with single gate $In_{0.75}Ga_{0.25}As$ UTB structure in Table 7.1 shows that Ref [24] has lower $I_{d,sat}$ despite its higher Indium concentration. This is likely due to the smaller RSD doping concentration used at $5x10^{19}cm^{-3}$ [24] compared to $6.5x10^{19}cm^{-3}$ in addition to larger spacer width of 20nm [24] in comparison to 15nm for this work. In addition, poorer electrostatic integrity is observed due to the higher Indium concentration used as the channel and slightly smaller L_g of 12nm. Nevertheless, Ref [24] shows the potential of double gate UTB in improving on-state current and electrostatic integrity despite increased channel thickness to 5nm compared to

3nm for the single gate devices.

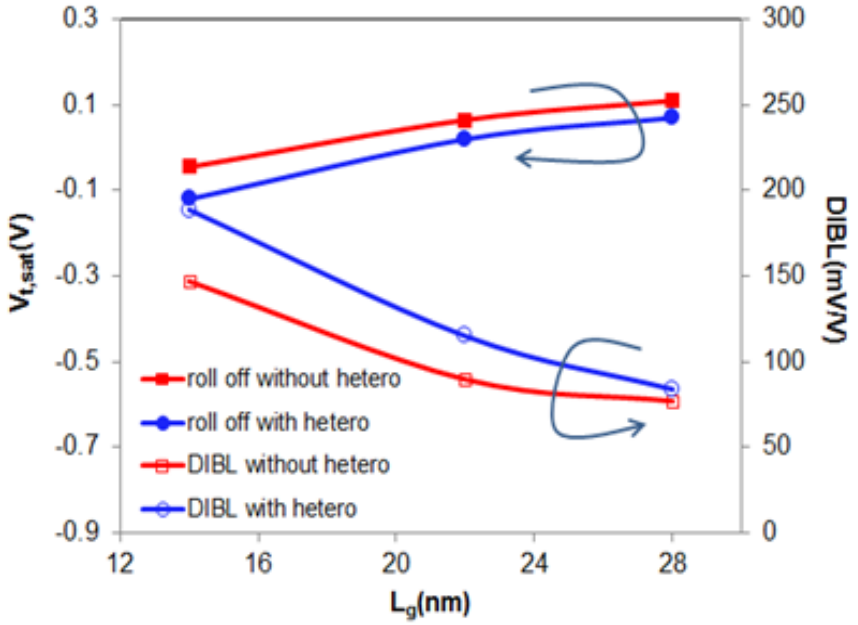

Fig.7.34. Electrostatic integrity as a function of gate length for device with and without heterostructure. Heterostructure device shows slightly worse SCE compared to without heterostructure.

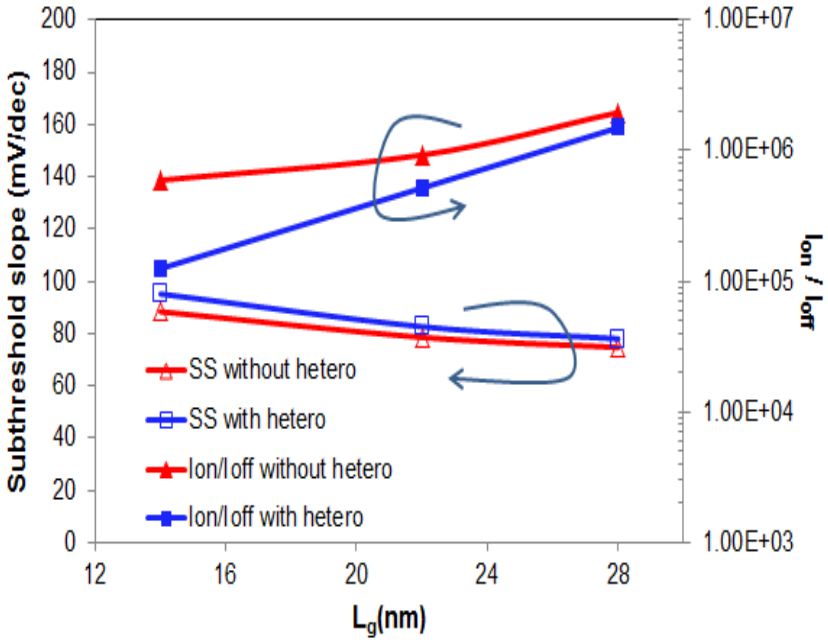

Fig.7.35. SS and I_{on}/I_{off} a function of gate length for device with and without heterostructure.

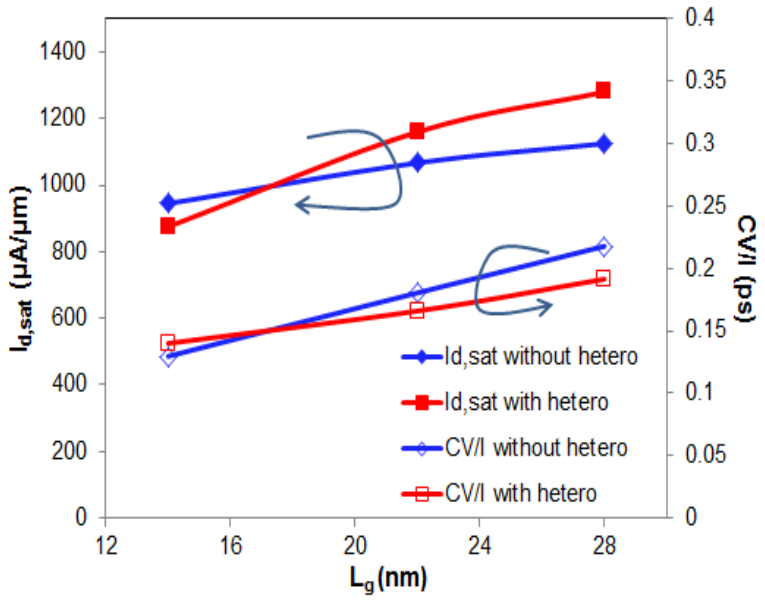

Fig.7.36. $I_{d,sat}$ and CV/I plots for device without heterostructure as a function of L_g with $I_{d,sat}$ taken at V_d=0.7V, V_g-$V_{t,sat}$=0.5V.

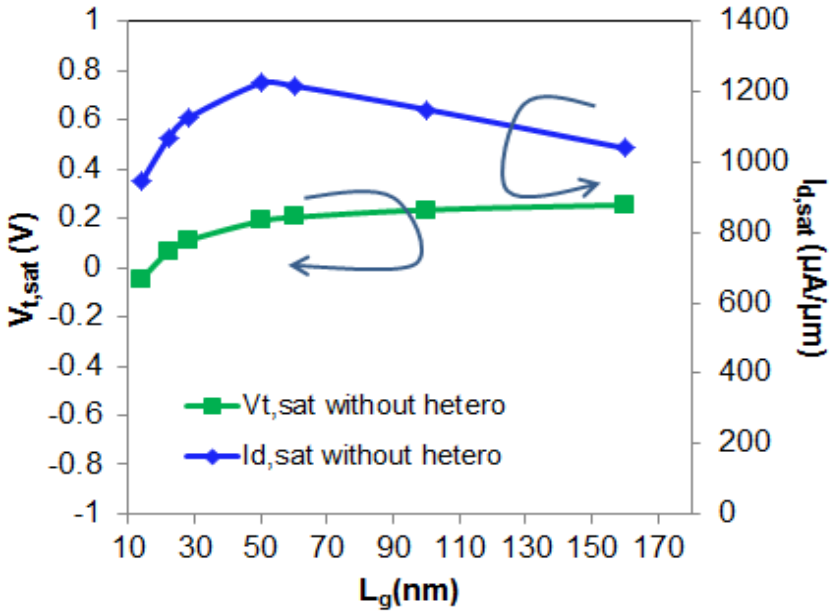

Fig.7.37. Plot of $V_{t,sat}$ and $I_{d,sat}$ as a function of L_g for V_d=0.7V, V_g-$V_{t,sat}$=0.5V. L_g below 50nm shows the region where the electrostatic effect from the drain becomes significant, resulting in significant roll off as well as causing reduced drive current with scaling.

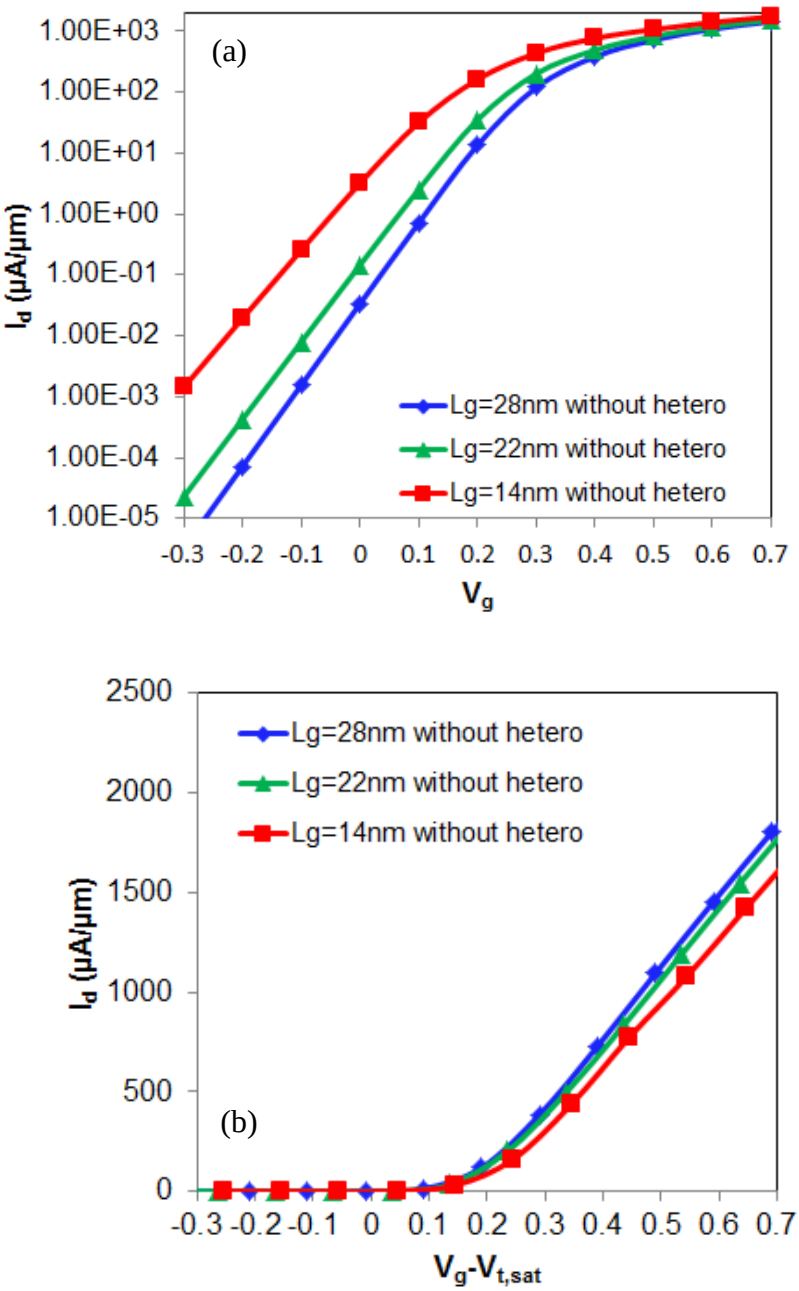

Fig.7.38 (a) I_d-V_g plot of device without heterostructure for L_g=14nm, 22nm and 28nm taken at V_d=0.7V and (b) Linear scale plot of I_d-(V_g-$V_{t,sat}$) for device without heterostructure for L_g=14nm, 22nm and 28nm taken at V_d=0.7V.

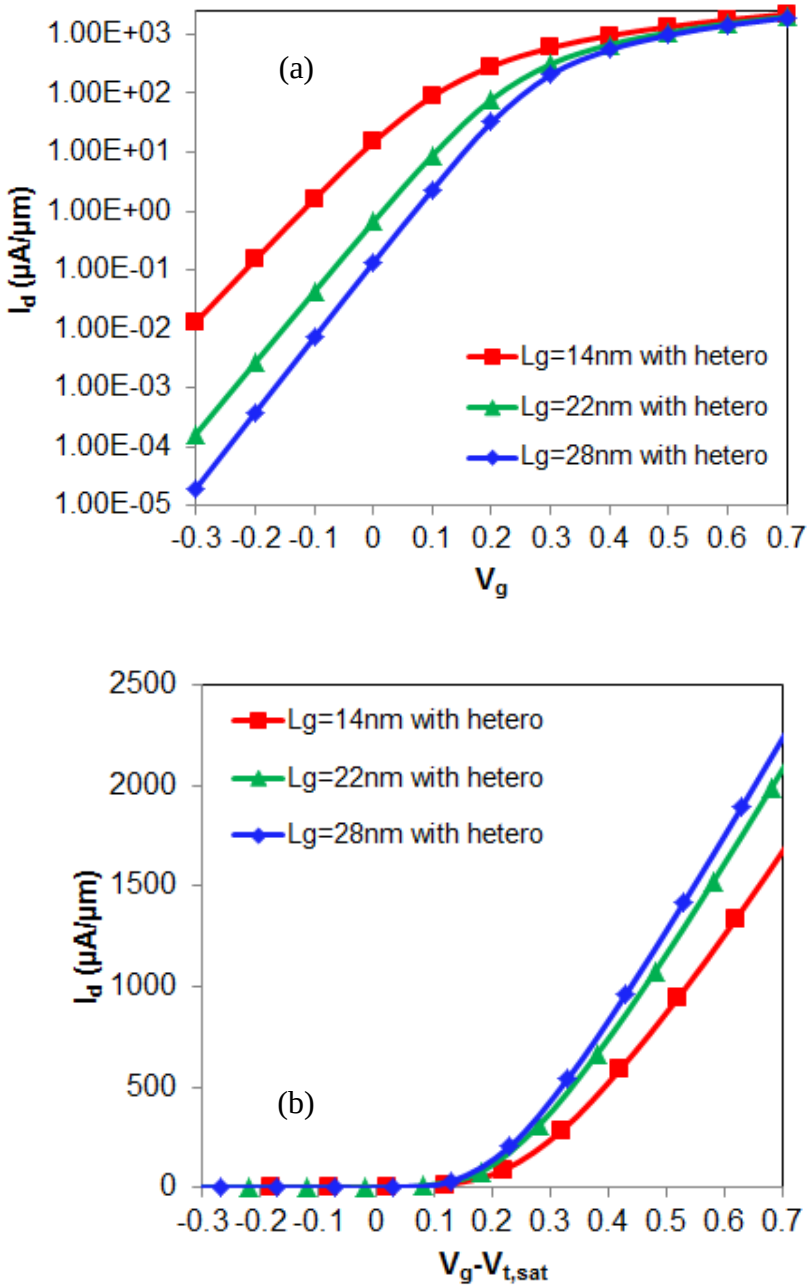

Fig.7.39 (a) I_d-V_g plot of device with heterostructure for L_g=14nm, 22nm and 28nm taken at V_d=0.7V and (b) I_d-(V_g-$V_{t,sat}$) plot of device with heterostructure for L_g=14nm, 22nm and 28nm taken at V_d=0.7V.

Table 7.1 The electrical data benchmarked against the simulation work performed by other groups [24,26] for L_g~15nm. $I_{d,sat}$ is referring to V_g-V_{th}=0.7V when comparison is made to Ref [26] and $I_{d,sat}$ is referring to V_g=0.7V at fixed I_{off} of 0.1μA/μm when comparison is made to Ref [24].

	$In_{0.75}Ga_{0.25}As$ double gate UTB MOSFET [24]	$In_{0.75}Ga_{0.25}As$ single gate UTB MOSFET [24]	this work without hetero $In_{0.53}Ga_{0.47}As$	this work with hetero $In_{0.53}Ga_{0.47}As$	IF-QWFET $In_{0.53}Ga_{0.47}As$ [26]
	V_d =0.7V	V_d =0.7V	V_d =0.7V	V_d =0.7V	V_d =1V
	L_g=12nm/ T_{ch}=5nm/EOT =0.6nm	L_g=12nm/ T_{ch}=3nm/EOT =0.6nm	L_g=14nm/ T_{ch}=3nm/EOT= 0.6nm	L_g=14nm/ T_{ch}=3nm/EOT= 0.6nm	L_g=13nm/ T_{ch}=3.25nm/EOT =0.44nm
SS	84	97	88.4	95.2	74
DIBL	91	234	147	188.8	34
$I_{d,sat}$ at fixed I_{off}=0.1 μA/μm	1747	1033	1300	1305	Nil
$I_{d,sat}$ at V_g-V_{th}=0.7V	Nil	Nil	1910	2290	1600

7.6. Conclusion

As a conclusion for this chapter, we have optimized the self-aligned surface channel plasma-PH_3/N_2 passivated $In_{0.53}Ga_{0.47}As$-based MOSFETs with implanted S/D. Further optimization through the use of raised S/D resulted in improvement to the electrostatic integrity as well as higher ability to prevent carrier starvation compared to device with implanted S/D. We have also investigated the effects of reducing the contact resistance, addition of spacer and reduced channel thickness of 10nm on device performance. It is found that with thin channel, $I_{d,sat}$ for thin channel is found to be larger than that of bulk structure, due to its higher carrier concentration brought about by stronger quantum confinement. Finally further device optimization has been carried out for prediction of 22nm and 14nm gate length $In_{0.53}Ga_{0.47}As$ MOSFETs which includes further thinning down of device channel to 3nm, varying spacer material and implementation of heterostructure device (compared to without heterostructure device). Results benchmarked with other groups' simulation works show results simulated are comparable and further improvement is expected with improved device architecture and higher Indium

concentration. In addition, to ensure continuous current increase with scaling, it is necessary for non-planar device structures or IF-QWFET capable of limiting the SCE be implemented.

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Chapter 8: Conclusion and Future Researches

8.1. Conclusion

This research work looks at III-V materials for MOSFET application, aims at advancing their device performance through novel plasma-PH_3/N_2 passivation technique and further device enhancement that can obtained based on the studies performed on the mobility scattering mechanisms and gate leakage mechanisms of such surface channel MOSFET.

In the first half of the thesis (Chapter 3 and 4), surface passivation technique for high-*k*/$In_{0.53}Ga_{0.47}As$ stack is studied in detail. It was found that device with plasma-PH_3/N_2 passivation treatment shows good thermal stability at high-*k*/$In_{0.53}Ga_{0.47}As$ interface, as confirmed from the small variation in the subthreshold slope, D_{it}, EOT and J_g results comparing before annealing and after 800°C annealing. This is believed to be due to lesser elemental Ga/As interdiffusion/intermixing across the high-*k*/$In_{0.53}Ga_{0.47}As$ interface, as confirmed by EDX analysis and TEM image, due to the presence of the thermally stable phosphorus nitride layer as well as the P-for-As exchanged layer. Gate leakage is also improved with this passivation technique attributed to the lack of traps given by trap energy levels at 0.95-1.3eV. The origins of these traps are not confirmed but likely to be due to defects, attributed to the interdiffusion of the Ga/As or In/Ga elements.

In Chapter 5, the carrier scattering mechanisms were studied through temperature dependent mobility measurements in order to understand the mechanisms responsible for improved device performance of device with plasma-PH_3/N_2 treatment relative to device without treatment. Larger Coulombic scattering, presence of soft optical phonon scattering from the

HfAlO and the interface dipole scattering present in the high transverse field were found to be primarily responsible for the lower $In_{0.53}Ga_{0.47}As$ NMOS mobility for the non-passivated device relative to device with passivation treatment. The smaller Coulombic scattering for the passivated device is attributed to the lower D_{it} in upper half of bandgap relative to the device without passivation, possibly due to the reduction in As-As bond formation as observed from XPS analysis. Further improvement to the mobility in the mid field region can be observed in passivated device relative to non-passivated device due to the reduction in soft optical phonon scattering dominating the high-*k* oxide. This is likely due to the thicker passivation layer present between the high-*k* and the substrate, which distances the high-*k* soft phonons from the interface, for passivated device. High field mobility is also improved for passivated device due to reduced interface dipole scattering brought about by aligned interface dipoles caused by reduced intermixing of Ga/In across the high-*k*/$In_{0.53}Ga_{0.47}As$ interface.

In Chapters 6-7, in order to investigate the performance scalability of implanted S/D $In_{0.53}Ga_{0.47}As$ NMOS with the current process flow, the device model calibration parameters and optimization for scalability studies in this thesis has been based on our group's IEDM 2008 long channel (4μm) non-passivated and plasma-PH_3/N_2 passivated $HfO_2/In_{0.53}Ga_{0.47}As$ MOSFETs as well as the short channel (95nm) plasma-PH_3/N_2 passivated HfO_2 $In_{0.53}Ga_{0.47}As$ MOSFET electrical data performance. Through TCAD device simulations, performance of the current device structure have been optimized through reduction in contact resistance, addition of spacer and halo implantations as well as S/D extension. Further optimization involved raised S/D structure where the results show improvement in device scalability in

terms of better electrostatic integrity with improved drive current than optimized implanted S/D attributed to its ability in reducing source starvation effects. Even further improvement to device performance and electrostatic integrity can be achieved with the use of thin channel. Further optimization to device structure, from L_g=28nm to 14nm, has also been simulated and benchmarked against simulation works performed on the same structure or different structure from this work. With raised S/D structures as well as T_{ch} =3nm and high-*k* spacers used, L_g=14nm for device without heterostructure gives SS of 88.4mV/dec, DIBL=147mV/V with $I_{d,sat}$=1775μA/μm at V_g-$V_{t,sat}$=0.7, V_d=0.7V. On the other hand for device with heterostructure SS is given by 95.2mV/dec, DIBL=188.8mV/V and $I_{d,sat}$=2090μA/μm at V_g-$V_{t,sat}$=0.7, V_d=0.7V.

In summary, this thesis has analysed and addressed several key technical challenges of $In_{0.53}Ga_{0.47}As$ MOSFET for advanced CMOS applications which include the issue of thermal stability of the high-*k*/$In_{0.53}Ga_{0.47}As$ gate stack, interface traps reduction at high-*k*/$In_{0.53}Ga_{0.47}As$ in order to reduce Fermi level pinning through the use of plasma-PH_3/N_2 passivation as well as simulating the device performance of sub-22nm technology node devices with this passivation treatment. This thesis has shown that plasma-PH_3/N_2 treatment is effective as a passivation technique to improve thermal stability which is essential for gate first self-aligned $In_{0.53}Ga_{0.47}As$ device (Chapter 3) as well as reducing traps in the gate oxide which is essential for gate oxide scaling (Chapter 4). It has also been shown that this technique is not only effective in reducing interface traps but also reducing soft optical phonon scattering and interface dipole scattering which are essential to improve device performance operating at low to higher

transverse field (Chapter 5). Further studies through TCAD simulation, studied in Chapter 6, also shows that not only the concentration, but also the nature of the interface traps (acceptor-like vs donor-like) at upper half of the bandgap of the high-*k*/$In_{0.53}Ga_{0.47}As$ interface, can contribute to SS, V_{th} and hence I_{on}. It is shown that reduced acceptor-like traps at the interface of high-*k*/$In_{0.53}Ga_{0.47}As$ plasma-PH_3/N_2 pasivated device is responsible for its reduced V_{th}. In addition, the device performance of $In_{0.53}Ga_{0.47}As$ device up till sub-22nm has been improved through the use of raised S/D structure, thin channel layer, and implementation of heterostructure (Chapter 7).

8.2. Future Works

Several issues have been opened up in this thesis which deserves further investigation. Some of the suggestions for future directions in the field of $In_{0.53}Ga_{0.47}As$ MOSFETs are highlighted in this section.

(i) Further optimization of plasma-PH_3/N_2 technique to reduce interface trap density throughout the bandgap and also surface roughness improvement

It has been found that the reduction in As-As bond present in the upper half of the bandgap is one of the possible reasons responsible for the improved device performance of the plasma-PH_3/N_2 passivation treatment. However, further reduction in As-As is still necessary to further improve the device performance. Since this As-As bond formation at the high-*k*/$In_{0.53}Ga_{0.47}As$ interface is attributed to the interaction between the P_xN_y layer formation and P-for-As exchange layer reaction, the effects of how varying the phosphorus concentration in the P-for-As exchanged layer or how varying the phosphorus/nitrogen concentration in the P_xN_y layer can help

reduce the As-As bond formation or other types of defects would be useful in further improving device performance of device with this passivation treatment. In addition, studies on how the bond formation contribute to reduction in soft optical phonon scattering from the high-*k* and also improvement in surface roughness, which has been found to contribute to device performance at higher transverse field, is also important for further device enhancement of plasma-PH_3/N_2 passivation technique. Further improvement in trap density can be obtained with pre-gate or post gate anneal. Post gate anneal include studying the effect of varying forming gas annealing (FGA) at various temperature or at various gas annealing types such as N_2 or fluorine post-gate treatment (through CF_4 plasma-treatment). These treatments can help to further reduce interface traps in the lower half of the bandgap.

(ii) Fabrication of Plasma-PH_3/N_2 with other high-*k* materials other than Hf based.

Future improvement would still be required for implementation of $In_{0.53}Ga_{0.47}As$ surface channel MOSFETs with high mobility. Novel high-*k* materials such as $LaLuO_3$ and Gd_2O_3 might have better passivation of $In_{0.53}Ga_{0.47}As$ interface and their high-*k* value (eg. *k* value of $LaLuO_3$ is 32 [1]) is also good for future EOT scaling. Fabricating surface channel $In_{0.53}Ga_{0.47}As$ MOSFETs with such high-*k* materials might be able to provide both high mobility and extremely small EOT.

(iii) Implementation of plasma-PH_3/N_2 technique with barrier layer structure

Thin channel for future device is a necessity for further device scaling as mentioned Chapter 7, but it has the tradeoff of reduced mobility due to

increased interactions from channel/high-*k* and channel/buffer interface. In order to further reduce the Coulombic scattering effects from the interface traps as well as reduce the surface roughness scattering, wide bandgap barrier layer in between the channel and high-*k* is crucial. Nevertheless, the interface quality in terms of low D_{it} and smooth high-*k*/barrier layer still remains essential to be of high quality [2] since it will still have an effect on the channel mobility especially if barrier layer is thin. Thus different passivation techniques on structures with barrier layer would still give different performance enhancement. Hence, it would be essential to perform experimental studies on plasma-PH_3/N_2 passivation on barrier layer, such as InP or $In_{0.52}Al_{0.48}As$, important for device scalability studies of plasma-PH_3/N_2 passivated with heterostructure.

(iv) Implementation of double gate heterostructure

It is seen in Chapter 7 that even with 1nm capping layer added, the DIBL increased quite significantly. In order to further benefit from even larger mobility which can be obtained from capping layer thicker than 1nm [3], without observing the tradeoff in the SCE performance, structures with even greater gate control is essential. Such structures may include double gate heterostructure where the disadvantage of the heterostructure larger SCE can be balanced off with the presence of additional gate.

(v) Heterostructure with large Indium concentration channel material

Maintaining the same body thickness given by $T_{body}=T_{ch}+T_{cap}$, by reducing the channel thickness and increasing the capping layer thickness, DIBL can be further reduced. This means the possibility of benefiting from the

high mobility of materials with high Indium concentration or even InAs without sacrificing the electrostatic integrity of the device, if the right combination of channel thickness and capping layer thickness is used. Even though mobility degradation is expected with even thinner channel, we expect the mobility enhancement with the use of higher Indium materials to offset this effect.

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List of Publications

Authors name is underlined in the list

1. Sumarlina A.B.S, H.J.Oh, A.Du, C.M.Ng, and S.J.Lee, "Study on Thermal Stability of Plasma-PH_3 Passivated HfAlO/$In_{0.53}Ga_{0.47}As$ Gate Stack for Advanced Metal-Oxide-Semiconductor Field Effect Transistor", *Electrochem.Solid-State Lett.,*Vol.13, pp. H336-H338, 2010.

2. Sumarlina A.B.S. and S.J.Lee, "Gate-Leakage and Carrier-Transport Mechanisms for Plasma-PH_3 Passivated InGaAs N-Channel Metal– Oxide–Semiconductor Field-Effect Transistors", *Jap.J.App.Phys.,* Vol.51, pp. 02BF02, 2012

3. Sumarlina A.B.S., H.J.Oh, and S.J.Lee ,"Effects of plasma-PH_3 passivation on Mobility Degradation Mechanisms of $In_{0.53}Ga_{0.47}As$ N-MOSFETs", *IEEE Trans. Elec. Dev.*, Vol.59, pp.1377, 2012

4. Sumarlina A.B.S, Oh.H.J, S.J.Lee, "Effects of plasma-PH_3 passivation on Mobility Degradation Mechanisms and Current Conduction Mechanisms of $In_{0.53}Ga_{0.47}As$ N-MOSFETs", *Solid State Devices and Materials conference*, 2011

5. Sumarlina A.B.S, G.S.Samudra, "Performance scalability studies by TCAD simulation of raised SD vs implanted SD plasma-PH_3 passivated InGaAs MOSFET", *Solid State Devices and Materials conference*, 2013

6. H. J. Oh, Sumarlina A.B.S., and S.J.Lee, "Interface enginnering for InGaAs N-MOSFET application using plasma PH_3-N_2 passivation", *J. Electrochem. Soc*., Vol.157, pp. H1051-H1060, 2010.

7. H.J.Oh, J.Q.Lin, Sumarlina A.B.S., G.Q.Lo, D.L.Kwong, D.Z.Chi, and S. J.Lee, "Thermally robust phosphorous nitride interface passivation for InGaAs selfaligned gate-first N-MOSFET integrated with high-*k* dielectric", *Tech. Dig. – Int. Electron Devices Meet,* pp.339, 2009