IEEE Access
Multidisciplinary | Rapid Review | Open Access Journal

Received April 2, 2017, accepted April 26, 2017, date of current version June 7, 2017.

Digital Object Identifier 10.1109/ACCESS.2017.2700439

Improving the Hardware Complexity by Exploiting the Reduced Dynamics-Based Fractional Order Systems

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This work was supported by University Jorge Tadeo Lozano under Grant 644-11-14. The work of A. Ibeas was supported in part by the Spanish Ministry of Economy and Competitiveness under Grant DPI2016-77271-R and in part by the University of the Basque Country (UPV/EHU) under Grant PPG17/33.

ABSTRACT Fractional calculus is finding increased usage in the modeling and control of nonlinear systems with the enhanced robustness. However, from the implementation perspectives, the simultaneous modeling of the systems and the design of controllers with fractional-order operators can bring additional advantages. In this paper, a fractional order model of a nonlinear system along with its controller design and its implementation on a field programmable gate array (FPGA) is undertaken as a case study. Overall, three variants of the controllers are designed, including classical sliding mode controller, fractional controller for an integer model of the plant, and a fractional controller for a fractional model of the plant (FCFP). A high-level synthesis approach is used to map all the variants of the controllers on FPGA. The integro-differential fractional operators are realized with infinite impulse response filters architecturally implemented as cascaded second-order sections to withstand quantization effects introduced by fixed-point computations necessary for FPGA implementations. The experimental results demonstrate that the fractional order sliding mode controller-based on fractional order plant (FCFP) exhibits reduced dynamics in sense of fractional integration and differentials. It is further verified that the FCFP is as robust as the classical sliding mode with comparable performance and computational resources.

INDEX TERMS Fractional order control, computational resources, nonlinear system, chattering.

I. INTRODUCTION

Fractional calculus is an emerging mathematical field which finds interesting applications in system models and control. The combination of the fractional operators with the integer order systems are advantageous due to the enhanced closed loop performance and robustness [1], [2].

The fractional order controllers are proven to have the ability in outperforming the integer order controllers in all aspect. With more degree of freedom, the fractional order controllers exhibit better transient response and enhanced robustness to the uncertainties. [3], [4] Moreover fractional order controllers are more robust to the measurement noise and with minimum chattering in the control signal [4]. It is a common practice to derive fractional order controllers based on integer order system models. The authors in the references [4], [5], [29] have proposed fractional order controllers based on integer order nonlinear system models and showed that the fractional order controllers outperform the conventional integer order control system.

The physical phenomena can be realistically modeled with fractional order dynamics [6], [7]. The authors of [6], [7] proved that the dynamic response of the approximated fractional order models representing a physical phenomenon is nearly equivalent to their integer order models. Similarly the anomalous diffusion phenomenon in nonhomogeneous media is modeled using fractional calculus [8]. Some other examples of fractional order modeling applications include fractance, fractional impedance [9], heat conduction [10], biology [11], [12], fractional transforms [30]–[32], fractional RC circuits [12], [33], [34] and non-integer finance

systems [13]. Some researchers have utilized fractional order models for the formulation of fractional order controllers. The authors of [14]–[19] proposed fractional order controllers based on the fractional order system models that include the industrial process, servos and physical phenomena. It has been proved in the above cited work that the control performance of the fractional controllers that are derived based on the fractional models are comparable to the fractional controllers that are formulated based on the conventional integer order systems.

However, from the implementation point of view the fractional controllers utilize more resources as compared to the integer order controllers [20]–[23]. This overhead is introduced by the inclusion of fractional operators in the controller implementation. Minimizing the number of the fractional operators required for controller realization will not only reduce the hardware complexity but also the power consumption due to reduced system dynamics. This paper leverages the degree of freedom offered by the fractional modeling of the plant to optimize the hardware resources by deriving a novel reduced order fractional controller. A model based high level synthesis methodology is used to implement the fractional order controllers using FPGA in the loop. Three variants of the controllers are designed for a well-known nonlinear system [25]. It includes a classical sliding mode control (ICIP), fractional order controller based on integer plant (FCIP) and fractional order controller based on fractional plant (FCFP). The experimental results demonstrate that the FCFP controller has reduced area overhead, power and chattering with comparable robustness to FCIP and classical sliding mode.

II. CONTROLLER's FORMULATIONS

The formulation of the high performance control for nonlinear dynamic system is always a challenging task. This section is devoted to the integer and fractional order mathematical modeling aspect and fractional order controller's formulation.

A. FRACTIONAL ORDER CONTROLLER BASED ON INTEGER MODEL

Consider the nonlinear dynamic system of Eq. 1 [24]–[26]

$$\begin{cases} \dot{x}_1(t) = -ux_1(t) + wx_4(t) - \varphi(t) \\ \qquad\quad + vx_5(t) - x_5(t)V(t) + d_1 \\ \dot{x}_2(t) = \varphi(t) - (u+\sigma)x_2(t) + d_2 \\ \dot{x}_3(t) = -(u+\gamma)x_3(t) + \sigma x_2(t) + d_3 \\ \dot{x}_4(t) = -(u+w)x_4(t) + \gamma x_3(t) + x_5(t)V(t) + d_4 \end{cases} \tag{1}$$

The nominal parameters of the above nonlinear system are defined as

$$\begin{cases} u : \textit{Death rates due to other causes}, \quad v : \textit{Natality rate} \\ w : \textit{Rate of immunity loss}, \quad \gamma^{-1} : \textit{Infective period} \\ \sigma^{-1} : \textit{Latent period} \end{cases}$$

Generally the 5th state is represented as: $x_5(t) = x_1(t) + x_2(t)+x_3(t)+x_4(t)$ [24]–[26]. By utilizing Eq.1, the dynamics of $x_5(t)$ are formulated as: $\dot{x}_5(t) = (v-u)x_5(t) + d_1 + d_2 + d_3 + d_4$. Here the terms $[d_1\ d_2\ d_3\ d_4]$ represent the parametric uncertainty which can be expressed as

$$\begin{cases} d_1 = -\Delta u x_1(t) + \Delta w x_4(t) + \Delta v x_5(t) \\ d_2 = (-\Delta u - \Delta\sigma)x_2(t) \\ d_3 = (-\Delta u - \Delta\gamma)x_3(t) + \Delta\sigma x_2(t) \\ d_4 = (-\Delta u - \Delta w)x_4(t) + \Delta\gamma x_3(t) \end{cases} \tag{2}$$

In Eq. 2 the terms involving represent the uncertainty in the parameter. The sum of all uncertainty terms is represented as $d_1 + d_2 + d_3 + d_4 = D = (\Delta v - \Delta u)x_5(t)$. Using Eq. (2), $x_5(t)$ is represented as $\dot{x}_5(t) = (v-u)x_5(t) + (v-u)x_5(t)$. In Eq. (1) $[x_1(t)\ x_2(t)\ x_3(t)\ x_4(t)]$ represent the state vector, $\varphi(t)$ is a nonlinear function expressed as $\varphi(t) = \beta x_1(t)x_3(t)/x_5(t)$ [26].

Assumption 1: System uncertainty is bounded such that

$$\begin{aligned} d_1 &\in \Omega_1 : \{d_{1\,\min} \le d_1 \le d_{1\,\max}\}, \\ d_2 &\in \Omega_2 : \{d_{2\,\min} \le d_2 \le d_{2\,\max}\} \\ d_3 &\in \Omega_3 : \{d_{3\,\min} \le d_3 \le d_{3\,\max}\}, \\ d_4 &\in \Omega_4 : \{d_{4\,\min} \le d_4 \le d_{4\,\max}\} \end{aligned}$$

Here d_{imin} and d_{imax} represent the upper and lower bounds of the uncertainty with $i = [1, 2, 3, 4]$. It is assumed that the upper bounds of the uncertainty terms are known.

Assumption 2: The Sum of the system uncertainty is upper bounded such that $D \in \Omega(d_1, d_2, d_3, d_4) : \{D_{\min} \le D \le D_{\max}\}$.

Here D_{min} and D_{max} represent the upper and lower bounds of the sum term. The control objective of this article is to design a robust controller with bounded control signal $V(t)$ such that the three states $x_1(t), x_2(t), x_3(t)$ are asymptotically zero i.e. $x_1(t) \to 0$; $x_2(t) \to 0$; $x_3(t) \to 0$ while the remaining two states arrive the respective equilibrium points such that $x_4(t) \to x_{4ref}(t)$; $x_5(t) \to x_{5ref}(t)$. Here $x_{5ref}(t)$ represents a reference command input. To achieve the above goal, a fractional order sliding manifold is utilized to derive a fractional order controller. The proposed fractional order sliding manifold is given by

$$S(t) = e(t) + c_1 D^{\alpha} \dot{e}(t) \tag{3}$$

In Eq. (3) the error dynamics are expressed as: $e = x_4(t) - x_5(t)_{ref}$; $\dot{e} = \dot{x}_4(t) - \dot{x}_5(t)_{ref}$, c_1 is a constant and D^{α} represents the fractional operator. By applying D^{α} to Eq. 3 one obtains

$$D^{\alpha} S(t) = D^{\alpha} e(t) + c_1 D^{2\alpha} \dot{e}(t) \tag{4}$$

Using the error signals dynamics $e(t) = x_4(t) - x_5(t)_{ref}$, $\dot{e}(t) = \dot{x}_4(t) - \dot{x}_5(t)_{ref}$ and by combining the dynamics of Eqs. (1) with Eq. (4), one obtains

$$\begin{aligned} D^{\alpha} S(t) = D^{\alpha}\{x_4(t) - x_5(t)_{ref}\} + c_1 D^{2\alpha}\{-(u+w)x_4(t) \\ + \gamma x_3(t) + x_5(t)V(t) + d_4 - \dot{x}_5(t)_{ref}\} \end{aligned} \tag{5}$$

From Eq. (5), the proposed control law is expressed as

$$\begin{cases} V(t) = V_{eq} + V_d \\ V_{eq} = x_5(t)^{-1}\{(u+w)x_4(t) - \gamma x_3(t) + \dot{x}_5(t)_{ref} \\ \qquad\qquad - c_1^{-1}D^{-\alpha}(x_4(t) - x_5(t)_{ref})\} \\ V_d = -x_5(t)^{-1}c_1^{-1}k_d D^{-2\alpha}\text{sgn}\{S(t)\} \end{cases} \tag{6}$$

In Eq. (6) the term k_d represents the discontinuous control gain. All other parameters of Eq. (6) have been defined in section IIA.

Remark 1: The discontinuous control V_d contains a fractional integrator applied to the signum function. This concept is already verified by the authors of reference [17].

Introduction to Theorem 1: Satisfying Assumption 1 and 2, the proposed fractional order controller given in Eq. (6) will asymptotically converge all the states of Eq. (1) to their respective equilibrium points regardless of the uncertainties in the model. i.e. $x_1 \to 0$, $x_2 \to 0$, $x_3 \to 0 x_4(t) \to x_5(t)x_4(t) \to x_5(t)$, $t \to \infty$,

Proof 1: To prove the stability of the proposed controller, the Lyapunov candidate function is $V_L = 0.5S(t)^2$. Moreover, the following inequality holds [27]

$$\left|\sum_{j=1}^{\infty} \frac{\Gamma(1+\alpha)}{\Gamma(1-j+\alpha)\Gamma(1+j)} D^j S(t) D^{\alpha-j} S(t)\right| \leq \tau |S(t)| \tag{7}$$

Here τ is a positive constant. By applying the fractional operator D^α to the Lyapunov function V_L one obtains

$$\begin{aligned} D^\alpha V_L &= S(t)D^\alpha S(t) \\ &\quad + \left|\sum_{j=1}^{\infty} \frac{\Gamma(1+\alpha)}{\Gamma(1-j+\alpha)\Gamma(1+j)} D^j S(t) D^{\alpha-j} S(t)\right| \end{aligned} \tag{8}$$

Using Eq. (7), the Eq. (8) is upper bounded as;

$$D^\alpha V_L \leq S(t)D^\alpha S(t) + \tau |S(t)| \tag{9}$$

$D^\alpha S(t)$ is explicitly calculated by using Eqs. (5), (6) and (9) as following

$$\begin{aligned} D^\alpha V_L &\leq S(t)[D^\alpha\{x_4(t) - x_5(t)_{ref}\} + c_1 D^{2\alpha}\{-(u+w)x_4(t) \\ &\quad + \gamma x_3(t) + x_5(t)V(t) + d_4 - \dot{x}_5(t)_{ref}\}] + \tau|S(t)| \\ &\leq S(t)[D^\alpha\{x_4(t) - x_5(t)_{ref}\} + c_1 D^{2\alpha}\{-(u+w)x_4(t) \\ &\quad + \gamma x_3(t) + d_4 - \dot{x}_5(t)_{ref} + \dot{x}_5(t)_{ref} + (u+w)x_4(t) \\ &\quad - \gamma x_3(t) - c_1^{-1}D^{-\alpha}(x_4(t) - x_5(t)_{ref}) \\ &\quad - c_1^{-1}k_d D^{-2\alpha}\text{sgn}\{S(t)\})\}] + \tau|S(t)| \\ &\leq S(t)c_1 D^{2\alpha}[-c_1^{-1}k_d D^{-2\alpha}\text{sgn}\{S(t)\} + d_4] + \tau|S(t)| \\ &\leq -k_d|S(t)| + \tau|S(t)| + S(t)D^{2\alpha}d_4 \end{aligned} \tag{10}$$

The discontinuous gain k_d is chosen such that the following criterion is satisfied: $k_d > |\tau + D^{2\alpha}d_{4\max}|$. The single loop controller will only cancel the uncertain terms of $\dot{x}_4(t)$. Based on **Assumption 2**, the remaining uncertain dynamics of the states $\dot{x}_1(t)$, $\dot{x}_2(t)$, $\dot{x}_3(t)$ can degrade control performance of the closed loop system. To guarantee the reaching condition of the sliding surface and to preserve the robustness of the single loop controller, the discontinuous gain is chosen as $k_d > |\tau + D_{\max}|$. Then expression (10) can be simplified as

$$\begin{aligned} D^\alpha V_L \leq &-k_d|x_1(t)| + \tau|S(t)| - S(t)D^{2\alpha}d_1 \\ &- S(t)D^{2\alpha}d_2 - S(t)D^{2\alpha}d_3. \end{aligned} \tag{11}$$

Since the last three terms of Eq. (11) are already negative, so the discontinuous gain $k_d > |\tau|$. Hence, then it is shown using the Eq. (11) that the fractional derivative of Lyapunov function is still less than zero, i.e. $D^\alpha V_L \leq 0$, which means that reaching condition of sliding surface is satisfied and $S(t) = 0$.

B. FRACTIONAL ORDER CONTROLLERS BASED ON FRACTIONAL ORDER MODEL

The nonlinear model presented in Eq. (1) is integer order. After replacing the integer order derivative with the fractional order the resultant system is represented as:

$$\begin{cases} D^\alpha \dot{x}_1(t) = -ux_1(t) + wx_4(t) - \varphi(t) \\ \qquad\qquad + vx_5(t) - x_5(t)V(t) + d_1 \\ D^\alpha x_2(t) = \varphi(t) - (u+\sigma)x_2(t) + d_2 \\ D^\alpha x_3(t) = -(u+\gamma)x_3(t) + \sigma x_2(t) + d_3 \\ D^\alpha x_4(t) = -(u+w)x_4(t) + \gamma x_3(t) + x_5(t)V(t) \\ \qquad\qquad + d_4 \end{cases} \tag{12}$$

Remark 2: Assumption 1 and 2 also hold for Eq. (12)

Here the error dynamics are expressed as $e(t) = x_4(t) - x_{5ref}(t)$, $\dot{e}(t) = \dot{x}_4(t) - \dot{x}_{5ref}(t)$. The analogous fractional order sliding manifold of Eq. (3) is given as

$$S(t) = e(t) + c_1 D^\alpha D^\alpha e(t) \tag{13}$$

Eq. (13) is analogous to Eq. (3) in the fractional order sense. Applying D^α to Eq. 13 one obtains

$$\begin{aligned} D^\alpha S(t) &= D^\alpha\{x_4(t) - x_5(t)_{ref}\} + c_1 D^{2\alpha} D^\alpha\{x_4(t) - x_5(t)_{ref}\} \\ &= D^\alpha\{x_4(t) - x_5(t)_{ref}\} + c_1 D^{2\alpha}\underline{D^\alpha\{x_4(t)\}} \\ &\quad - c_1 D^{3\alpha} x_5(t)_{ref}\} \\ &= D^\alpha\{x_4(t) - x_5(t)_{ref}\} + c_1 D^{2\alpha}\{-(u+w)x_4(t) \\ &\quad + \gamma x_3(t) + x_5(t)V(t) + d_4\} - c_1 D^{3\alpha} x_5(t)_{ref}\} \end{aligned} \tag{14}$$

The proposed control law is derived from Eq. 14 as;

$$\begin{cases} V(t) = V_{eq} + V_d \\ V_{eq} = x_5(t)_{ref}^{-1}\{(u+w)x_4(t) - \gamma x_3(t) + D^\alpha\{x_5(t)_{ref}\} \\ \qquad\qquad - c_1^{-1}D^{-\alpha}\{x_4(t) - x_5(t)_{ref}\}\} \\ V_d = -x_5(t)_{ref}^{-1}c_1^{-1}k_d D^{-2\alpha}\text{sgn}\{S(t)\} \end{cases} \tag{15}$$

The control law given in Eq. (15) is analogous to the expression (6) but in the fractional order sense. Here k_d represents the discontinuous control gain and c_1 is the sliding surface constant. The rest of the parameters are already defined in the previous section. A disadvantage of the control law presented in Eq. (15) is in the form of large fractional order dynamics i.e. in the form of $D^{-2\alpha}$ and $D^{2\alpha}$. Since the controller is

formulated based on the fractional order model of the system, so the large fractional order dynamics in the model will lead to large fractional orders in the control law correspondingly. In contrast to the above the control law of expression (6) is derived based on the integer order model so the selection of lower fractional orders for the controller is not restricted. To deal with the above mentioned problem, an analogous reduced dynamics based fractional order sliding mode manifold is proposed as

$$S(t) = e(t) + c_1 D^{\alpha} e(t) \tag{16}$$

After applying D^{α} to Eq. 16 one obtains

$$\begin{aligned} &D^{\alpha} S(t) \\ &= D^{\alpha}\{x_4(t) - x_5(t)_{ref}\} + c_1 D^{\alpha} D^{\alpha}\{x_4(t) - x_5(t)_{ref}\} \\ &= D^{\alpha}\{x_4(t) - x_5(t)_{ref}\} + c_1 D^{\alpha} \underline{D^{\alpha}\{x_4(t)\}} - c_1 D^{2\alpha} x_5(t)_{ref} \\ &= D^{\alpha}\{x_4(t) - x_5(t)_{ref}\} + c_1 D^{\alpha}\{\{-(u+w)x_4(t) + \gamma x_3(t) \\ &\quad + x_5(t)V(t) + d_4 - \dot{x}_5(t)_{ref}\}\} - c_1 D^{2\alpha} x_5(t)_{ref}\} \end{aligned} \tag{17}$$

The new control law with reduced dynamics is derived as;

$$\begin{cases} V(t) = V_{eq} + V_d \\ V_{eq} = x_5(t)^{-1}\{(u+w)x_4(t) - \gamma x_3(t) + D^{\alpha}\{x_{5ref}(t)\} \\ \qquad\qquad - c_1^{-1}\{x_4(t) - x_{5ref}(t)\}\} \\ V_d = -x_5(t)^{-1} c_1^{-1} k_d D^{-\alpha} \mathrm{sgn}\{S(t)\} \end{cases} \tag{18}$$

Remark 3: The fractional order control law given in Eq. (18) is of the reduced fractional order dynamics as compared to that given in expression (15). The control law of Eq. (18) with reduced dynamics contains only a fractional derivative and an integral while the control law of Eq. (15) consists of a fractional derivative, fractional integral and a fractional integral of double fractional order. From practical implementations point of view, the control law of Eq. (18) will require fewer computations as compared to the one given in expression (15). The fractional order dynamics of the control law given in the expression (15) is always the same as to that of the fractional order model. Another disadvantage of the control law given in the expression (15) is the increase of its fractional order beyond 1 when the fractional order dynamics of the model is greater than 0.5.

Introduction to Theorem 2: Satisfying Assumption 1 and 2, the proposed fractional order controller of Eq. (18) will asymptotically converge all the states of Eq. (12) regardless of the uncertainties in the model. i.e. $x_4(t) \to x_5(t)$; $x_3(t) \to 0$; $x_2(t) \to 0$; $x_1(t) \to 0$ *at* $t \to \infty$,

Proof 2: To prove the stability of the proposed controller given in Eq. (18), the Lyapunov candidate function is $V_L = 0.5S(t)^2$. By solving Eqs (17), (18) and (12) one obtains

$$\begin{aligned} D^{\alpha} V_L &\le S(t)[D^{\alpha}\{x_4(t) - x_{5ref}(t)\} \\ &\quad + c_1 D^{\alpha}\{\underline{-(u+w)x_4(t) + \gamma x_3(t) + x_5(t)V(t) + d_4}\} \\ &\quad - c_1 D^{2\alpha} x_{5ref}(t)] + \tau |S(t)| \\ &\le S(t)[D^{\alpha}\{-k_d D^{-\alpha}\mathrm{sgn}\{S(t)\} + d_4\}] + \tau |S(t)| \\ &\le -k_d \mathrm{sgn}|S(t)| + \tau |S(t)| + S(t) D^{\alpha} d_4 \end{aligned} \tag{19}$$

To choose the discontinuous gain we use the similar concepts to that presented in Theorem 1. The discontinuous gain must satisfy $k_d > |\tau + D_{\max}|$, which implies that $D^{\alpha} V_L \le 0$. With $D^{\alpha} V_L \le 0$, this meaning that reaching condition of the sliding surface is satisfied and $S(t) = 0$. The discontinuous control V_d of the expression (18) contains a fractional integrator. Since the fractional integrator acts as a low pass filter so the chattering phenomena will minimize. Chattering phenomena can be eliminated by using $sat(.)$ function instead of the signum function.

III. DIGITAL IMPLEMENTATION OF FRACTIONAL OPERATORS

The digital realization of the fractional order integrals and differential operators requires careful considerations in the discretization and numerical representation phases. First, the fractional order operators are derived using the Oustaloup method [28] for a specified bandwidth. This method is used to design the fractional order differential and integrals by controlling the α-parameter bounded in the range 0 to 1. The positive values of alpha are used for differentials while negative values for the integrals. The corresponding fractional order operator is a continuous domain transfer function represented in s-terms. For digital implementation of these operators on FPGA, it should be discretized from continuous domain and then converted to fixed point representation. This can be accomplished with a number of well-established discretization methods widely available in commercial software's. However, the discretized version of the transfer function in z-domain representing the fractional operator is not really amenable to digital implementation, as it is in form of improper polynomial fractions. As an example for $\alpha = -0.99$, designed in bandwidth of [0.001, 1500], with filter order of 2, the s-domain numerator and denominator polynomials of the filter are calculated as

$$N = [0.0007172 \quad 1.126 \quad 97.23 \quad 486.7 \quad 141.3 \quad 2.255]$$

$$D = [1 \quad 93.98 \quad 485.7 \quad 145.5 \quad 2.529 \quad 0.002416]$$

Here N represents the numerator coefficient and D represents the denominator coefficients. Applying Tustin's approximation for discretization on the above transfer function yields the following z-domain co-efficient

$$N = [0.0060 \ -0.0154 \ 0.0091 \ 0.0060 \ -0.0073 \ 0.0017]$$

$$D = [1.0000 \ -4.3330 \ 7.3651 \ -6.0969 \ 2.4307 \ -0.3659]$$

The z-domain transfer function is an improper polynomial fraction, in order to reduce it to the proper fraction; we can proceed in the following manner. $Q = N_1/D_1 = 0.0060$, $R = N - QD$. Here Q is the quotient, R represents the remainder and N_1, D_1 are the first elements of numerator and denominator. The polynomial division process can be re-written as $Q(R/D) \to Q + (R/D)$. As a result of the above process numerically the following results are achieved

TABLE 1. IIR filter coefficient.

SOS	Numerator Coefficients			Denominator coefficients			scale
	b_0	b_1	b_2	a_0	a_1	a_2	
Sos1	0	1	0	1	-0.38643	0	0.010427
Sos2	1	-1.3454	0.37496	1	-1.9468	0.94694	1
Sos3	1	-1.9969	0.99692	1	-1.9998	0.99982	1

as following

$$Q = 0.0060$$
$$R = [0 \quad 0.0104 \quad -0.0349 \quad 0.0423 \quad -0.0218 \quad 0.0039]$$
$$D = [1 \quad -4.3330 \quad 7.3651 \quad -6.0969 \quad 2.4307 \quad -0.3659]$$

The reduced z-domain polynomial form is a summation of a constant and a proper fraction representation of the transfer function which does not cause any numerical issues for the solvers. Then, the z-domain coefficients are used for realization of a discrete infinite impulse response filter that has similar behavior in the corresponding band to that of the fractional operator discussed above. To reduce the sensitivity of the filter to numerical representation and quantization perturbations, the cascaded direct form I second-order sections of biquad filter is adopted as hardware architecture. Table 1 shows the corresponding coefficients for the IIR filter. It can be noted that the range is now limited from -2 to $+2$ compared to the wide variation in range and the precision of numerators and denominator coefficients in the s/z-domains. The results of passing a sinusoid through the fractional operator implemented in continuous, discrete and digital domain are shown in Fig. 1.

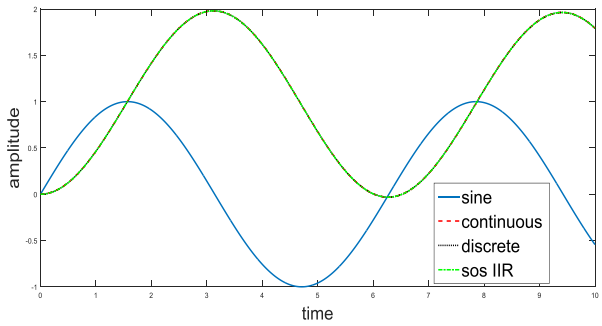
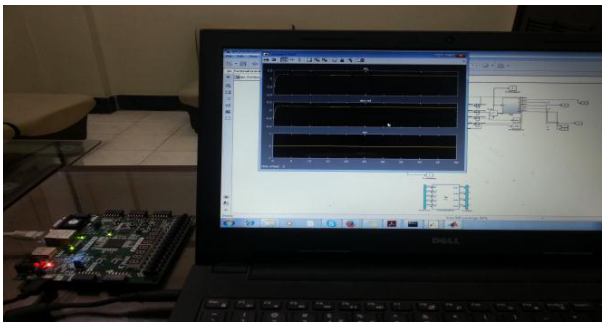


FIGURE 1. Continuous and discrete implementation of fractional operator.

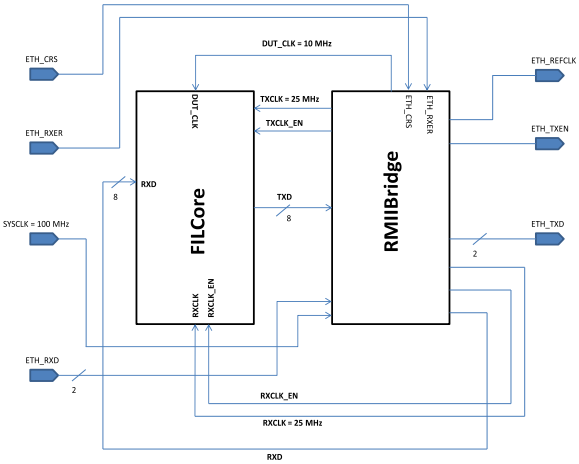
IV. EXPERIMENTAL SETUP AND RESULTS

This section presents the details of the software and hardware implementations of the proposed controllers. The overall model is first designed in software using MATLAB's Simulink using the floating point arithmetic. After the software verification, the design is mapped onto FPGA for hardware validation.

The employed FPGA platform is based on the latest 28 nm 7 series Artix-7 FPGA embedded in a Nexus 4 development board. For hardware validation, the plant model runs in the



(a)



(b)

FIGURE 2. (a) Experimental setup and (b) block diagram.

Simulink environment while the controllers run on the FPGA platform connected with the host PC through 10/100 Mbps Ethernet cable for bi-directional communication. On the PC side, the Simulink environment is responsible for controlling the simulation parameters and data transfer mechanism while on the FPGA side the Ethernet PHY chip is connected through a Reduced Media Independent Interface (RMII) to Medium Access Layer (MAC). The MAC layer in our case is our controller logic wrapped into communication layers confirming to RMII interface as shown in Fig 2. Several signals of interest are shown in this figure including the ETH_TXD and ETH_RXD representing the transmit data and receive data signals each two bit wide. The host PC sends and receives two-bit data through the PHY layer which operates on a 50 MHz while the RMII Bridge accumulates this data and communicates back and forth with 8-bit data to the design represented by FPGA in the Loop (FIL) core both operating at 25 MHz The actual controller design embedded inside the FILcore operates on a clock of 10 MHz Thus, the overall design is a multi-clock system imposing strict constraints on timing and synchronization.

From design and implementation standpoint, first a continuous time s-domain model is developed and then discretized

to z-domain. The discrete model uses the fractional operators realized with infinite impulse response filters as discussed in section III. As the controllers are to be mapped onto FPGA, they are converted to fixed-point numeric format using the built in fixed point tool leaving out the plant to operate on the default floating point numeric format. The resultant fixed-point model is simulated and compared with the floating point simulations to calculate the error due to the quantization effects. This process is iterated several times to have an error within acceptable margins. The trade-off here is between the precision and accuracy of the results against the hardware complexity. Increasing the number of bits increases the accuracy and precision but also increases FPGA resource consumption. The fixed-point model is further adapted to adhere to the hardware mapping and HDL code generation by using HDL supported Simulink blocks. The HDL coder has built-in options for several optimizations during code generation process and has the capabilities to auto-annotate critical paths in the Simulink model, which then, can be manually optimized for timings. Similarly, area optimization can be accomplished with macro blocks like DSP48s or by sharing operators.

After a synthesizable code is generated, the HDL verifier tool is used which generates the corresponding wrappers and communication commands processing cores. This high-level synthesis and rapid prototyping approach allows quick design modifications and design-space explorations seamlessly relieving the designer from the painful process of manual HDL design. Instead, the critical design parts can be manually implemented and optimized for the desired goals. Following this methodology, several controllers are mapped onto the FPGA platform and their behavior, resources, execution times control and signal errors are compared which are presented in the following sub-sections.

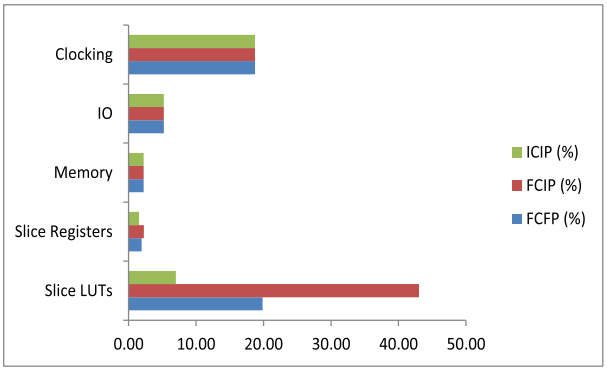


FIGURE 3. Device Utilization chart.

The resource variation is evident in the slice registers and slice LUTs which are the main resources for logic implementation. The number of slice LUTs and FFs utilized by each controller is good matrix for comparison and is the one that is applicable across a range of different device families as state-of-the-art FPGAs are widely based on 6-LUT slice architecture. From the device utilization chart given in Fig 3,

TABLE 2. Utilized resources by controllers.

Resource type	FCFP-22bits	FCIP-33bits	ICIP-22bits
Slice LUTs	12593.00	27279.00	4450.00
Slice Registers	2447.00	2862.00	1965.00
Memory	3.00	3.00	3.00
IO	11.00	11.00	11.00
Clocking	6.00	6.00	6.00

it is evident that the fractional controller integer plant (FCIP) is the most resource consuming design taking 44% LUTs and almost 3% slice flip-flops using 33 bits fixed point representation. The Integer Controller and Integer Plant (ICIP) are considered as the baseline for comparison and it is realized in 22-bit fixed point numeric format. The integer controller integer plant takes the least resources almost 7% LUTs and 2% flip-flops while the fractional controller fractional plant takes 20% LUTs and 2% flip-flops using 22-bit fixed point representation. Further details and comparsion about the utilized resources for each variant of the controller are tabulated in Table 2. The degree of freedom offered by the fractional modeling of plant to the controller reflects in the area consumption due to the reduced computational complexity. It is worth mentioning that the results are obtained without any manual or automatic optimization procedure employed which can in term result in resource savings further.

Remark 1: To have acceptable results in case of FCIP controller, the minimum fixed point bits' representation is chosen as 33. Below 33 bits the results of the FCIP controller are not realistic.

A. POWER CONSUMPTION

The post-implementation power consumption statistics generated with Vivado power estimator of the three controllers are presented in Figure 4 and Table 3. These results are obtained with the switching activity settings of 12.5 as toggling rate and 0.5 as the static probability. The percentage breakdown of the power consumption on the axis of its internal hardware components and into static and dynamic components is shown in Figure 4.

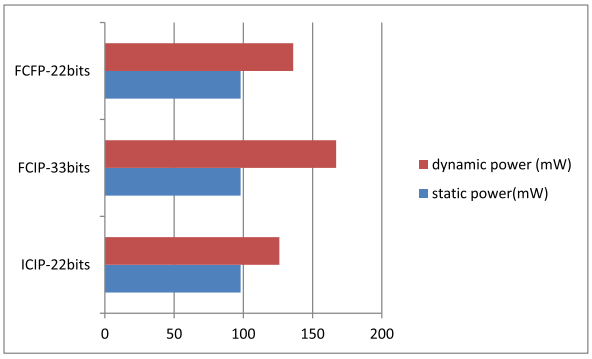


FIGURE 4. Static and dynamic power consumption.

TABLE 3. Power consumption of implemented controllers.

Resource type	FCFP -22bits (mW)	FCIP -33bits (mW)	ICIP-22bits (mW)
Clocks	4	5	4
signals	9	28	4
logic	9	20	4
BRAM	1	1	1
MMCM	106	106	106
I/O	7	7	7

TABLE 4. Model parameters and parametric uncertainty.

Model Nominal Parameters		Parametric Uncertainty	
u^{-1}	$255days^{-1}$	Δu^{-1}	$20days^{-1}$
$\gamma^{-1} = \sigma^{-1}$	$1.2days^{-1}$	$\Delta\gamma^{-1} = \Delta\sigma^{-1}$	$1days^{-1}$
w^{-1}	$12days^{-1}$	Δw^{-1}	$2.5days^{-1}$
v^{-1}	$115days^{-1}$	Δv^{-1}	$15days^{-1}$
β	$1.66days^{-1}$	β	$1.66days^{-1}$

TABLE 5. Controllers parameters.

ICIP		FCIP		FCFP	
c_1	0.5	c_1	0.5	c_1	0.5
k_d	200	k_d	200	k_d	0.01
ε	$0.5days^{-1}$	ε	$0.5days^{-1}$	ε	$0.5days^{-1}$
α	1	α	0.4	α	0.99

The device static power consumption remains the same for all the three controllers; however, the dynamic power consumption varies according to the complexities on the controllers. It can be noted that the MMCM, Block RAMs, and I/Os are consuming the same amount of power as these resource is unchanged. However, the signals and logic power consumption greatly varies following the same trends as that of the area resource consumption. From Figure 7, it is clear that the FCIP design is consuming almost double the power consumption of FCFP design which is consuming two times the power consumption of ICIP design. These figures are based on the signal and logic power consumption components of each controller. Thus the FCFP controller has a reduced the power consumption as well as the areas resources by half while maintaining the same system dynamics as will be shown in the control and signal errors section.

B. CONTROL AND SIGNAL ERRORS

This section is devoted to the comparison of the control performance and robustness property for all the three variants. The parameters of the pant and controllers are tabulated in Table 4 and 5. From the experimental results presented in section 1V, it is concluded that the fractional order controller with 22 bits' realization (FCFP) utilize less resources

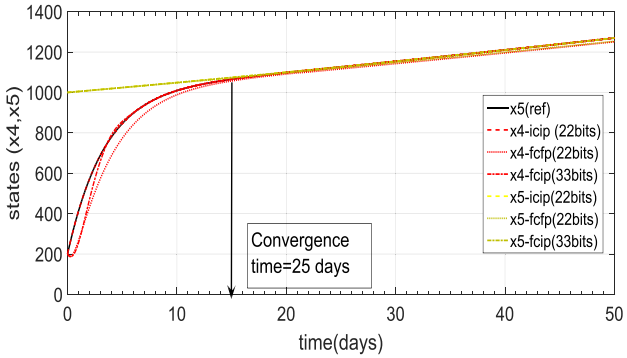


FIGURE 5. States x4 and x5 convergence and response comparison.

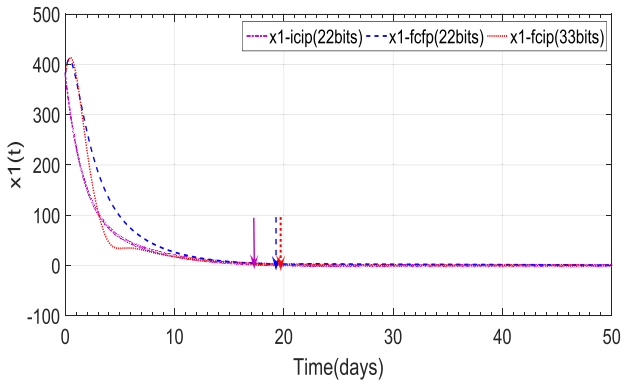


FIGURE 6. State x1 convergence and response comparison.

as compared to the first case i.e. fractional controller with 33 bits (FCIP). As it is proved from the literature survey that the classical sliding mode controller is robust to the matched uncertainties but its major disadvantage is the high frequency chattering. So the classical sliding mode controller is treated as benchmark case for comparing the robustness property for the other two cases. Fig 5 compares the convergence of the states x4 and x5 to the reference command i.e. x5(ref). The experimental results of the classical sliding mode controller (ICIP) are compared with fractional controller (FCFP-22 bits) and (FCIP-33 bits). From Fig. 5 it is obvious that for all the three cases, the average convergence time is comparable i.e. 23˜25 days. Moreover, the steady state error is negligible. The convergence times of the remaining three states x1, x2 and x3 are compared in Fig. 6, 7 and 10. To show the convergence time more precisely arrows of the same colors as original states are marked on time axis. The convergence time of state x1 with classical sliding mode controller (ICIP) is 17.5 days, with fractional order controller (FCIP-33 bits) 19 days and fractional order controller (FCFP-22 bits) is 19.8 days.

Similarly, the state x2 converges to zero at t = 14 days using classical sliding mode control (ICIP), at t = 15 days using fractional order control (FCIP-33 bits) and at t = 17.5 days using fractional order controller implemented with FCFP-22 bits.

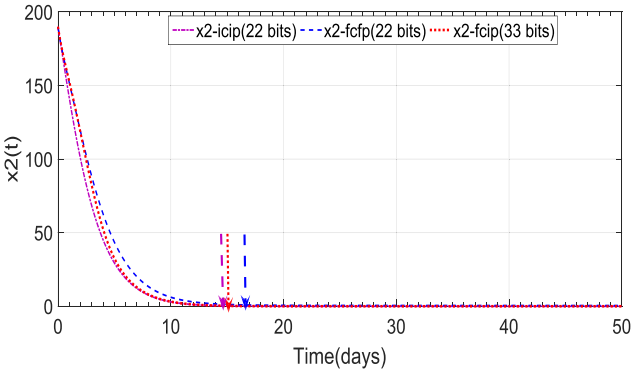


FIGURE 7. State x2 convergence and response comparison.

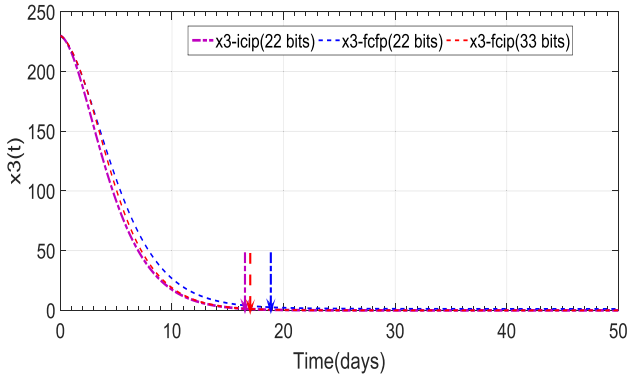


FIGURE 8. State x3 convergence and response comparison.

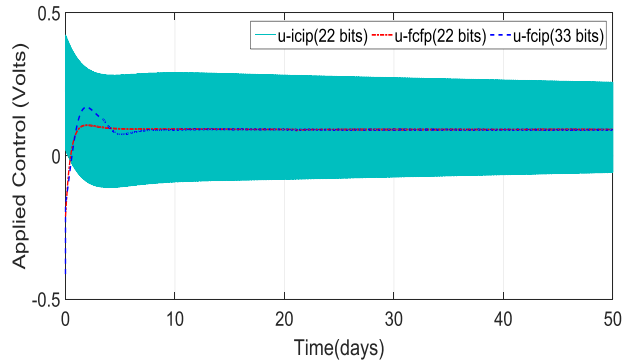


FIGURE 9. Control signal comparison.

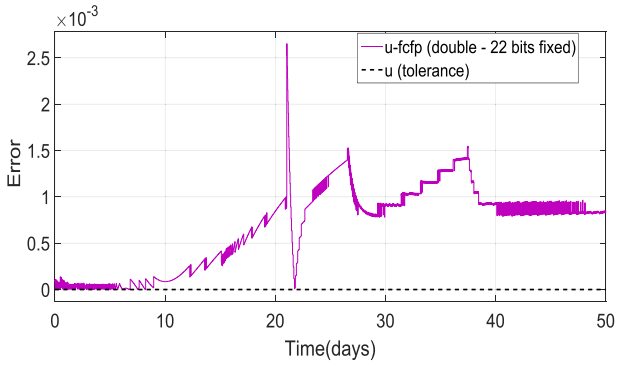


FIGURE 10. Floating point–fixed point error plot of control signal (fractional controller fractional plant).

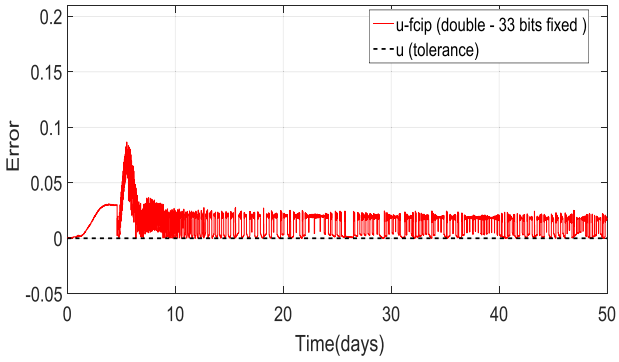


FIGURE 11. Floating point–fixed point error plot of control signal (fractional controller integer plant).

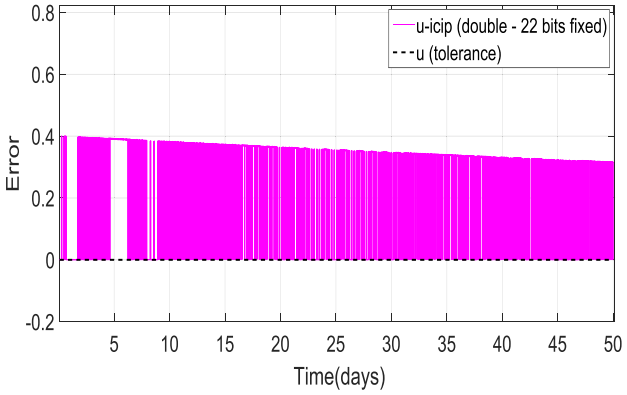


FIGURE 12. Floating point–fixed point error plot of control signal (classical sliding mode control- integer plant).

Near similar behavior can be observed from Fig. 8 showing the convergence time of state x3. The convergence times of the states using fractional order controller implemented with FCFP-22 bits are comparable with the classical sliding mode control (ICIP) which is a benchmark to evaluate the convergence property. Fig 9 compares the experimental results of the control signals for all the three variants of the controllers. It is noticeable that the classical sliding mode control (ICIP) offers maximum chattering while the fractional order controllers exhibits chattering with smaller magnitude. The main reason of the reduced chattering in the fractional order controllers of expression (15) and (18) is the existence of the fractional integrator across the discontinuous signum function. For digital implementations of the algorithms an important aspect is to analysis the errors generated due to fixed point representation of the signals.

A comparative analysis of the fixed point implementation errors generated in the control signals is shown in Fig. 10, 11 and 12. The error signals represent the amplitude difference of the control signal between floating point and fixed point representation. From the comparative results presented in Fig. 10, 11 and 12, it is noted that fractional order controller with 22 bits (FCFP) implementation have small error as compared to the other two cases. Another important aspect of the performance measurement for the implanted

controllers is the chattering phenomenon. The experimental results presented in Fig. 10, 11 and 12 show that the fractional order controller with 22 bits (FCFP) implementation offers the least amount of chattering as compared to the other variants.

V. CONCLUSION

This article is focused on the implementation and computational resources study of the fractional order controllers. Three variants of the controllers are under consideration namely classical sliding mode controller (ICIP), fractional order controller-integer plant (FCIP) and fractional order controller-fractional plant (FCFP). From the results it has been explored that the fractional controller-fractional plant (FCFP) is computationally less expensive as compared to FCIP. Moreover, it is as robust as classical sliding mode controller with additional advantage of having reduced chattering. The future work will be focused on using high-level synthesis based design-space exploration techniques for improving performance, area and power consumption along with minimizing quantization errors further.

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