A Reconfigurable Acoustic Telemetry Transmitter Employing Crystal-Less Temperature-Independent Frequency Reference for Oil Drilling Applications

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Declaration

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Zhou Lianhong

2 Jan 2014

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First of all, I would like to thank my supervisor, A/Professor Heng Chun Huat, for his relentless support and valuable guidance. His expertise in circuit design greatly helped me overcome the obstacles to accomplish this work. Thanks for all his patience and effort in teaching and guiding me in the progress of this project.

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Summary

High data rate communication is desired in oil drilling industry to transmit information such as temperature and pressure. However, typical operation temperature in oil drilling is more than 200℃ and thus such high temperature operation environment makes the circuit design challenging. Moreover, in the drilling strings, the acoustic channel exhibits comb shape characteristics which provides very limited available passband bandwidth for transmission, which limits the achievable data rate.

This work presents a multi-channel acoustic telemetry transmitter which can be configured to generate either OOK modulated signal or chirp modulated signal. The reconfigurability provides the flexibility to deal with the variation in acoustic channel characteristics. With 6-channel OOK modulated signal, a total data rate of 120bps is achieved, which is at least 3 times faster than the current reported discrete acoustic transmitter. While with 3-channel chirp modulated signal, a total data rate of 60bps is achieved.

A crystal-less temperature-independent frequency reference is employed to generate the carriers for the acoustic telemetry modulator. Two different approaches have been proposed to achieve frequency independence at such high temperature range. They consist of a frequency-locked loop (FLL), but differ in frequency deviation measurement. The first approach adopts RC phase shifter to measure the frequency deviation whereas the second approach employs frequency-to-voltage converter (FVC). Both approaches use highly digital

intensive FLL and resistor temperature coefficient (TC) compensation technique to achieve the temperature independence.

The frequency reference using RC phase shifter achieves frequency stability of ±1.94% over temperature range of 175℃ to 275℃. The frequency reference using FVC achieves frequency stability of ±2.85% over temperature range of 25℃ to 300℃ with digital trimming. Implemented in 1μm SOI CMOS technology, both chips occupy an active area of 25mm^2 and consume power of 9mW and 11mW at 25℃, respectively. To demonstrate the transmitter performance, the measured modulated output was successfully demodulated through a software receiver with proper channel and noise modeling.

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Chapter 1 Introduction

1.1 Background

Oil industry has been constantly searching for faster wireless data link for down-hole data communication. Crucial information, such as geo-steering, wellbore pressure, and temperature provide the opportunity of tight control over the bore-hole trajectories and enhancement of the wellbore stability. Conventional mud pulse and electromagnetic (EM) telemetry are rate limited (<10bps) due to low carrier frequency of 100Hz and 30Hz, respectively [1]. The operation frequency range of wireless acoustic telemetry is from 400Hz to 2kHz, and thus can offer potentially higher data rate transmission. Theoretical foundation of propagating acoustic energy in drilling strings was developed by Barnes and Kirkwood [2]. Drumheller accomplished the first successful theoretical explanation of acoustic wave propagation for telemetry purpose in real-time drilling environment [3]. Lee and Ramarao provided further understanding of acoustic attenuation in drilling string by analyzing wave propagation in fluid loaded drilling string [4-5]. However, we have yet to see a fully integrated wireless acoustic telemetry transmitter up to date. All reported wireless acoustic telemetry systems are currently discrete solutions with very little system performance information [6].

There are a few challenges in designing acoustic transmitter for oil drilling application. First, the temperature in drilling pipes is extremely high, which is a function of the underground depth of the well. Worldwide, the typical geothermal gradient is 25 ℃/km. However, in some area, it can reach to 40 ℃/km [7]. Now oil

companies have already developed the geothermal wells where the operation temperature is around 250 ℃. If deeper wells are exploited, the temperature will further increase. Moreover, in the oil companies, the qualification temperature of testing is usually 50~60 ℃ higher than the operation temperature. Second, the acoustic channel in drilling pipes exhibits comb shape characteristic, which makes the available frequency range of acoustic passband very limited. Therefore, the carriers of acoustic transmitter have to be placed accurately within the acoustic passband.

In this work, a fully integrated acoustic transmitter is proposed based on crystal-less temperature-independent frequency reference. The frequency reference is realized through digital-intensive frequency-locked loop (FLL) and can help to generate temperature-stable carriers for acoustic transmitter. Multi-channel solution is also employed to boost the achievable data rate with the reconfigurability of OOK/chirp modulation.

1.2 Transmitter Review

1.2.1 Acoustic Channel

The drilling string consists of many drill pipes which comprise a pin and box tool joint separated by a thinner section of pipe. At each joint/pipe junction, the transmission signal is partially reflected and partially transmitted, which results in a very complicated set of interfering waves. Some waves within certain frequency ranges are able to propagate along the drill string, while some are blocked. Due to the repetitive nature of the drill pipe in the drill string, the acoustic channel

exhibits typical comb shape characteristic with pipe-dependent passband channel frequencies and bandwidth as shown in Figure 1-1 [8]. Typically, the first acoustic channel is not used as they are swarmed by drilling noise. Higher frequency channels are undesirable due to much narrower bandwidth and higher attenuation. In this work, we only make use of the second to fourth channel to achieve the desired acoustic transmission. The detailed modeling of the acoustic channel is beyond the scope of this thesis. However, through our collaborators' studies, a Matlab acoustic channel model for such application has been built. This helps us determine the desired transmitter characteristic, such as transmission channel, modulation bandwidth, and etc. It also allows us to evaluate the transmitter performance through software demodulation.

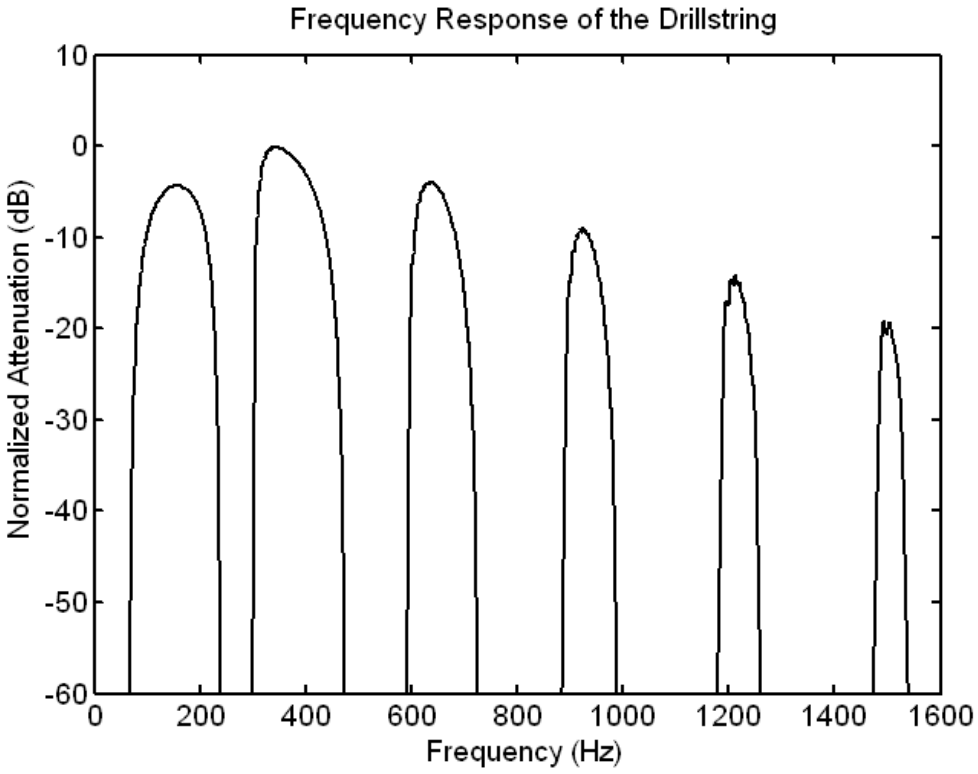

Figure 1-1 Typical comb shape acoustic channel characteristics of drill pipe.

1.2.2 Current Acoustic Transmitter

A lot of research effort is devoted to develop wireless acoustic telemetry system for oil drilling application. However, these reported designs include very little information about the circuits and are not integrated. A basic acoustic telemetry system consists of a downhole transmitter and a surface receiver [1]. The transmitter interfaces with the Measurement-While-Drilling (MWD)/Logging-While-Drilling (LWD) data bus to access tool information and generates the acoustic signal which propagates along the drill string. The receiver is positioned at the end of the drill string to receive and decode the data. An optional repeater can be placed between the downhole transmitter and the surface receiver to boost the signal so that the depth of the transmission and the data rate will be increased.

Ref [1] describes an acoustic telemetry system which can transmit 2-channel OOK modulated signals and achieves an effective data rate of 40bps. To mitigate the drill shock related damage, the downhole transmitter is positioned to be above all LWD tools. An acoustic attenuator is placed between the drill bit and the transmitter to provide the additional acoustic isolation from the drilling noise. Ref [6] energizes a stack of piezoelectric discs at a frequency of about 640Hz. The stack elastically stretches a short section and produces about 25 watts of power into wave energy. A 40Hz sweep of chirp modulated signal which spreads acoustic energy over significant sections of the passband is generated to minimize the energy loss at generally unknown frequencies due to frequency notches and other distortions. The chirp lasts for somewhat less than 1/20 second, thereby defining normal 20 baud data rate per channel.

1.2.3 Crystal-Less Temperature-Independent Frequency Reference

As discussed before, temperature-independent frequency reference is a critical building block for acoustic transmitter. Although crystal reference can provide very stable output, it has bulky size and cannot be integrated with standard CMOS process. Therefore, on chip frequency reference becomes an attractive solution. In the subsequent sections, we will examine various on chip frequency references and their limitations.

1.2.3.1 LC Oscillator

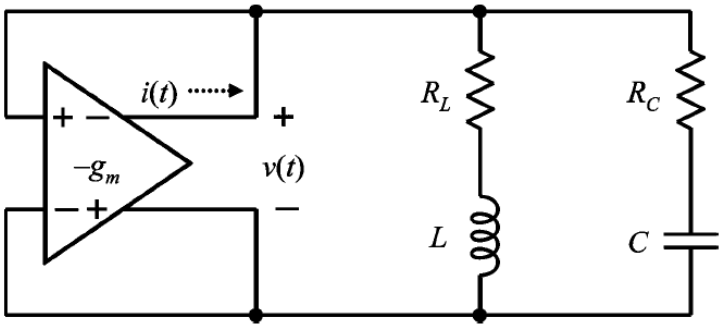

Figure 1-2 Schematic of a generalized LCO including the transconductor and the coil and capacitor losses, RL and RS, respectively [9].

The ideal resonant frequency of an LC tank, as shown in Figure 1-2, is

$$w_0 = \sqrt{LC}^{-1} \tag{1.1}$$

where L is the tank inductance and C is the tank capacitance. However, both the coil and the capacitor suffer from finite losses, R_L and R_S, respectively. Considering these losses, the actual oscillation frequency is

$$w_1 = w_0\sqrt{\frac{L-CR_L^2}{L-CR_C^2}} \tag{1.2}$$

The transconductance amplifier injects a current i(t) into the LC tank with high harmonics, the majority of which are absorbed by the capacitor instead of the inductor. This harmonic work imbalance (HWI) is reconciled by reducing the oscillation frequency.

Several techniques have been introduced to trim frequency drift due to process variation and temperature effect [10-12]. A 25MHz self-referenced solid-state frequency source which is referenced to a frequency-trimmed temperature-compensated 800MHz free-running LC oscillator (LCO) is presented in [9]. The mechanisms which result in frequency drift in LCO were first discussed. The tank inductor L is determined nearly exclusively by the coil and exhibits a low temperature coefficient (TC). The tank capacitor C consists of the designed capacitor, the transconductor and fringing capacitance from interconnect. Integrated thin-film capacitors have low TCs. However, in CMOS circuits, the transconductor presents an inversion-mode MOS (I-MOS) capacitor to the tank with a non-negligible TC. The I-MOS capacitor can be properly biased to decrease the TC. Moreover, the coil loss R_L is substantially larger than the capacitor loss R_C. Ignoring the TC due to the I-MOS capacitance from the transconductor, the temperature-dependent can be expressed as

$$w_1(T) \approx w_0\sqrt{1 - CR_L^2(T)/L} \tag{1.3}$$

where T is the temperature and $R_L(T)$ has a nearly linear positive TC for any metal interconnect.

The harmonic content of i(t) is subject to changes in the transconductor, which is proportional to carrier mobility $\mu^{1/2}$. The mobility μ has a temperature dependency

of $T^{-3/2}$. Thus HWI exhibits a positive TC. However, this effect is relatively small, and cannot cancel the negative TC from the coil loss.

The reference oscillator is shown in Figure 1-3. A 14-bit binary-weighted programmable array of p-type I-MOS varactors are employed to trim the nominal frequency. Temperature compensation is realized through a programmable 4-bit binary-weighted array of accumulation-mode pMOS (A-MOS) varactors. Temperature-dependent compensation voltage $v_{ctrl}(T)$, which is proportional to absolute temperature, is used to bias the varactor. When $v_{ctrl}(T)$ increases, the varactor capacitance decreases, which leads to a larger oscillation frequency and thus compensates for the negative TC.

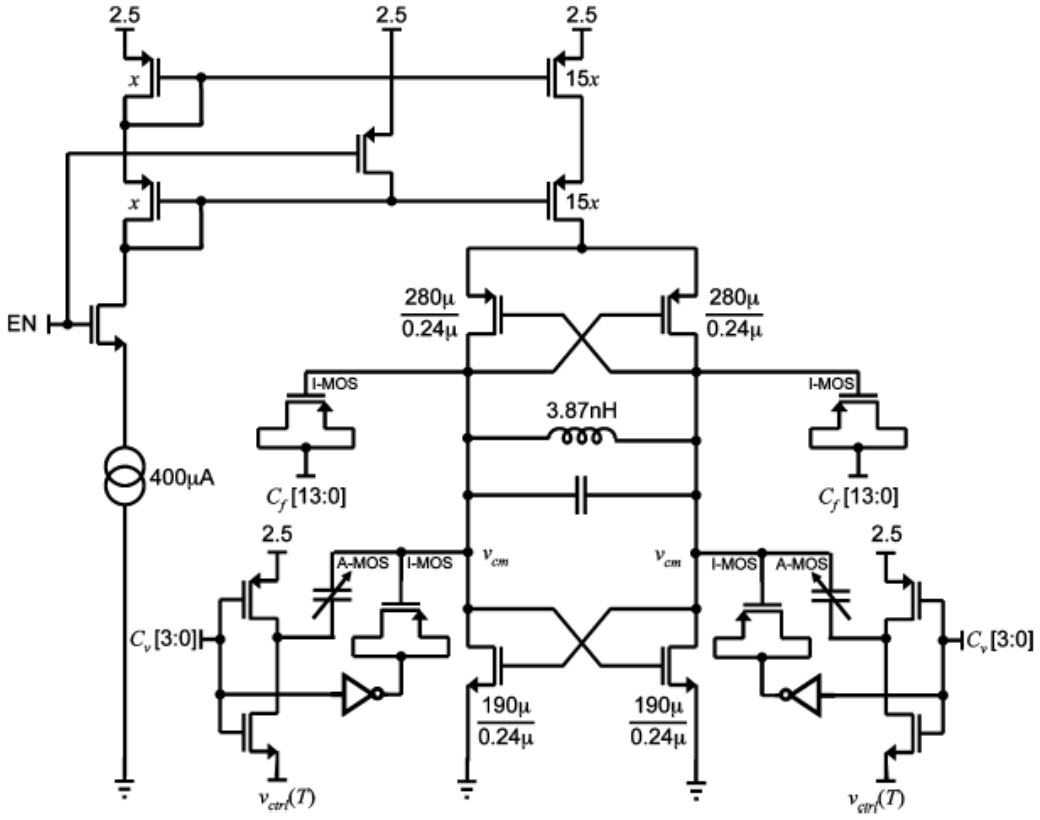

Figure 1-3 800MHz reference oscillator [9].

The system architecture is shown in Figure 1-4. Fabricated in a 0.25μm CMOS process, the chip achieves a frequency inaccuracy of ±1.4% over ±10% variation in power supply and from -10 ℃ to 80 ℃.

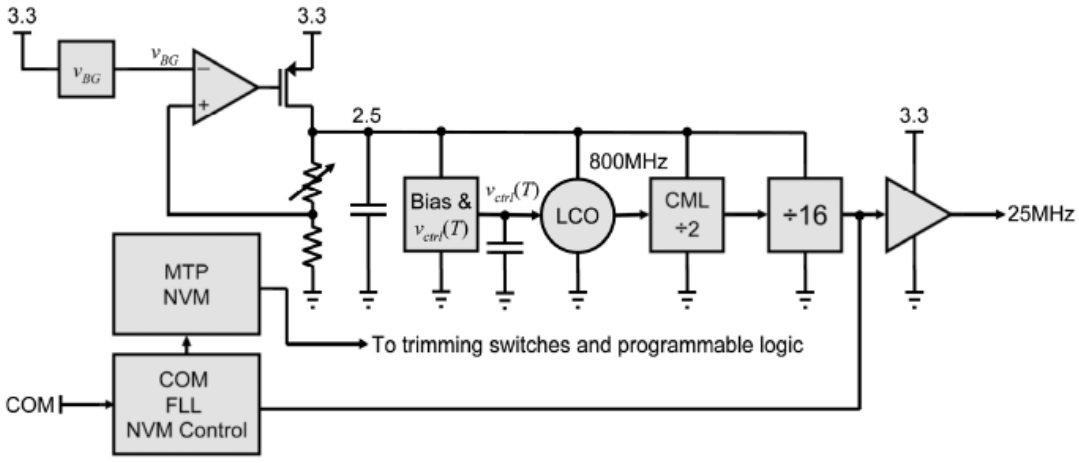

Figure 1-4 System architecture of 25MHz self-referenced frequency source [9].

Although LC oscillators have very good frequency stability, they usually occupy large chip area and dissipate more power. Also, the operation frequency of LC oscillators is not suitable for our work, because in acoustic telemetry the carrier's frequency is only a few hundred Hertz. Furthermore, the operation temperature range of LC oscillators is limited to 70~80 ℃. The targeted temperature range of our work is up to 300 ℃ and LC oscillators cannot support such high temperature operation.

1.2.3.2 RC Oscillator

Oscillator can be built based on different passive components [13-15]. A typical architecture of RC-based oscillator is Wienbrige oscillator as shown in Figure 1-5. The Wienbridge oscillator consists of an amplifier and a passive RC-feedback network. The amplifier should satisfy the condition that the gain equals to 3 and

zero phase delay is introduced. The oscillation frequency f is 1/(2•π•R•C) where R and C are the values of the resistors and capacitors in the feedback network.

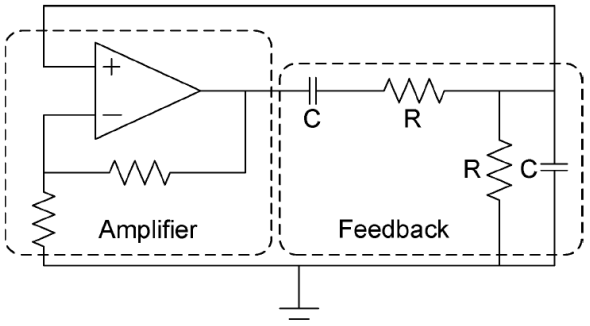

Figure 1-5 Conventional Wienbrige topology [16].

Ref [16] presents a new Wienbridge topology which achieves low phase noise, low temperature dependency and low power consumption. The oscillation frequency is determined by the passive RC network, and N-/P-poly resistors together with MIM-capacitors are employed. The temperature dependency of the capacitor is considered negligible. The N- and P-poly resistors have a positive and a negative 1st-order temperature coefficient (TC), respectively. A combined resistor with residual 2nd-order TC is thus obtained.

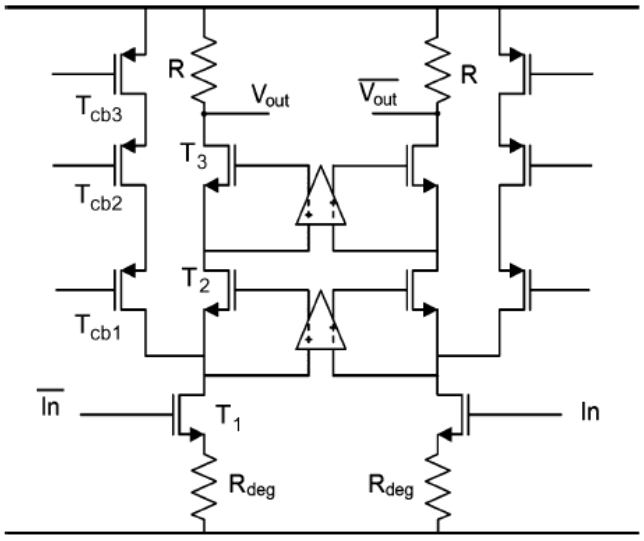

Figure 1-6 Completed amplifier used in the Wienbridge oscillator [16].

The opamp introduces the finite output impedance and phase shift to the RC network, thus affecting the oscillation frequency. To minimize the impact of the finite output impedance of the amplifier, the output impedance is enhanced by adding two cascode transistors, as shown in Figure 1-6. The transconductance g_m of the amplifier is also temperature-dependent, which leads to a gain variation due to temperature. In order to stabilize the gain, source degeneration is utilized.

$$g_{m,deg} = \frac{g_m}{1+g_m \cdot R_{deg}} \approx \frac{1}{R_{deg}} \tag{1.4}$$

Therefore, the transconductance g_m is mostly determined by the source resistor R_{deg}. The source degeneration also increase the output impedance by a factor of $(1+g_m \bullet R_{deg})$. Moreover, the current bleeding technique is used to increase the transconductance without sacrificing the output impedance. To increase the output impedance furthermore, gain boosting is applied to the cascode transistors. The pole-frequencies of the amplifier are strictly controlled to minimize the phase shift.

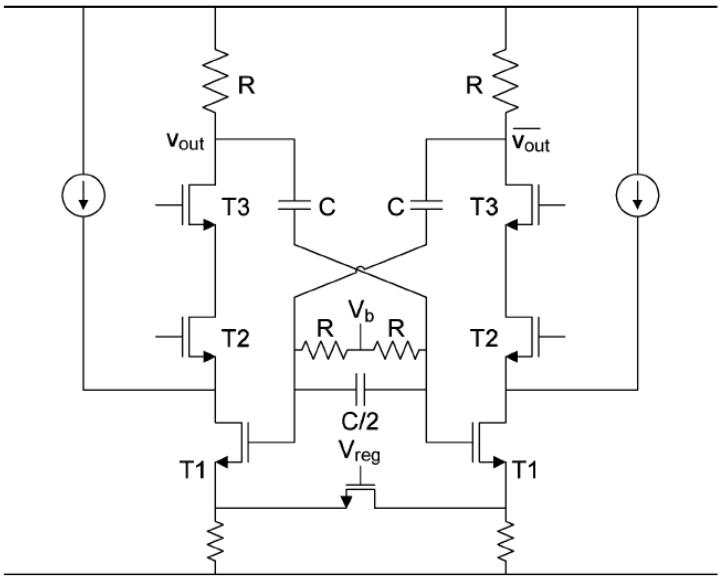

Figure 1-7 Complete schematic of the Wienbridge oscillator. The gain boost amplifiers are omitted for clarity reasons [16].

Cascading two (inverting) amplifiers with feedback network can provide the non-inverting gain required by the Wienbridge topology, as shown in Figure 1-7. A differential signal can be generated between the output nodes of the two amplifiers.

The oscillation frequencies are measured from 0℃ to 120℃ with the nominal frequency of 5.998MHz. The achieved temperature dependency is ±0.9%.

The RC oscillator is an analog approach, which may not maintain robust under extremely high temperature operation environment in oil drilling application. The temperature in the drilling pipes is as high as 250℃. Standard CMOS technology cannot support such high temperature. In our design, SOI CMOS technology is adopted. It is the only available process which can support up to 225℃. The acoustic transmission demands even higher temperature. However, the model beyond 225℃ is not available in SOI CMOS technology. Therefore, the analog approach is not a good choice for our application. Due to the lack of the accurate model for high temperature, it is difficult to design and ensure all the analog blocks which can work fine. As an alternative, digital intensive implementation with minimized analog blocks are preferred.

1.2.3.3 Ring Oscillator

A three-stage ring oscillator circuit is shown in Figure 1-8. A comparator is needed at the output of the final stage. To eliminate the asymmetric loading of the delay stages caused by the comparator, buffer and dummy delay stages are employed. Each delay stage consists of a source coupled pair and a symmetric load as shown in Figure 1-9. The oscillation frequency is expressed as:

$$f = \frac{1}{N \cdot t_d} = \frac{\mu_4 C_{ox4}(W_4/L_4)(V_{ref} - V_{T4} - V_{ctrl})^2}{N \cdot C_O \cdot (V_{ref} - V_{ctrl})} \quad (1.5)$$

where C_O is the total capacitance seen at the output of each stage. Temperature and process variation may affect the mobility of the charge carriers and the threshold. Also, the capacitor C_{ox} and C_O will change due to the temperature variation. Therefore, the oscillation frequency varies with temperature and process.

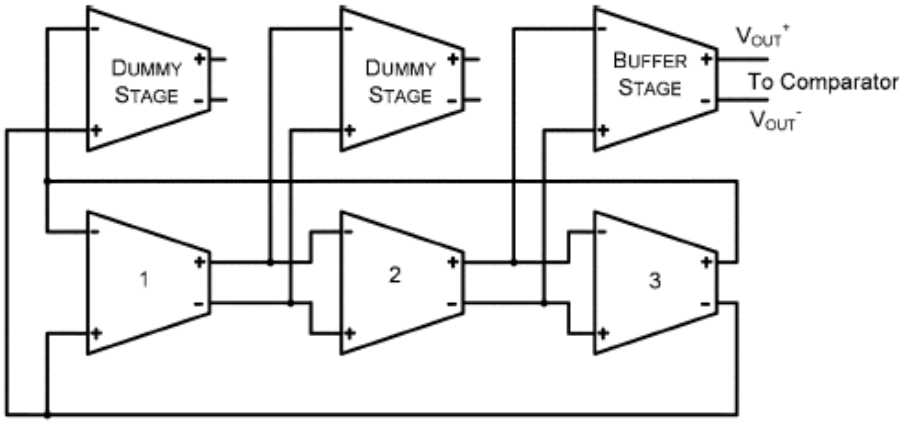

Figure 1-8 Schematic of three-stage ring oscillator [17].

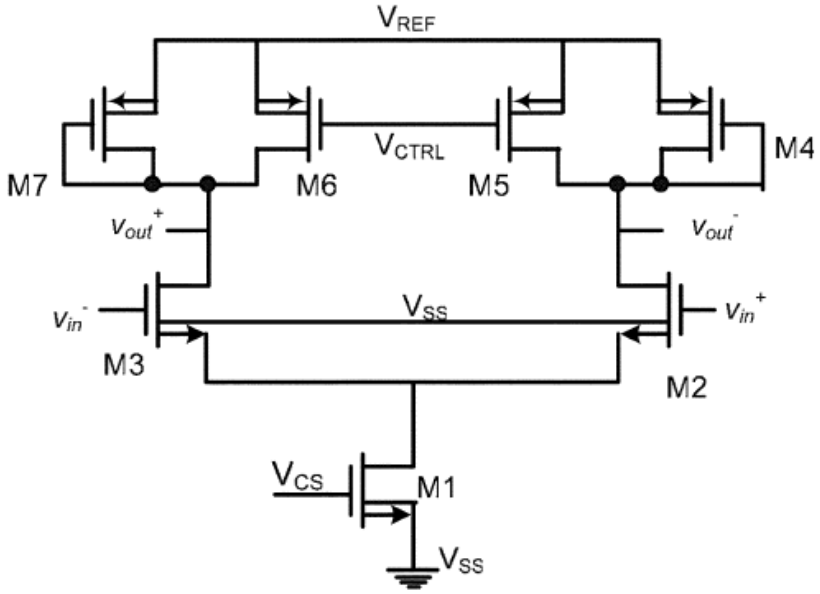

Figure 1-9 Schematic of the symmetric load delay stage [17].

Different temperature compensation techniques are proposed in ring oscillator [18-20]. A 7MHz clock oscillator realized in 0.25μm CMOS process is introduced in [17]. It incorporates a combined temperature and process compensation circuit. A bandgap referenced voltage regulator is used to generate a supply and temperature independent reference voltage, which serves as a stable temperature independent supply voltage for the oscillator and the supporting circuits. To compensate for temperature and process variations, V_{CTRL} is tuned to generate stable frequency. By analyzing the relationship between V_{CTRL} and f, in order to compensate for temperature variation, V_{CTRL} should satisfy the following equation:

$$V_{CTRL} \approx A - C \cdot T \tag{1.6}$$

where $$A \approx V_{ref} - V_{Tpo}, C \approx -\left(\frac{1}{2} \cdot \frac{f \cdot N \cdot C_{x0}}{\mu_{p0} \cdot C_{oxo} \cdot (W/L)_4}\right) \tag{1.7}$$

Process variation is compensated by sensing the threshold voltage and generating a process-dependent voltage reference for the temperature compensation circuit. Figure 1-10 shows the schematic of the complete compensation circuit. The measured frequency variation is ±1.84% over the temperature range of -40℃ to 125℃.

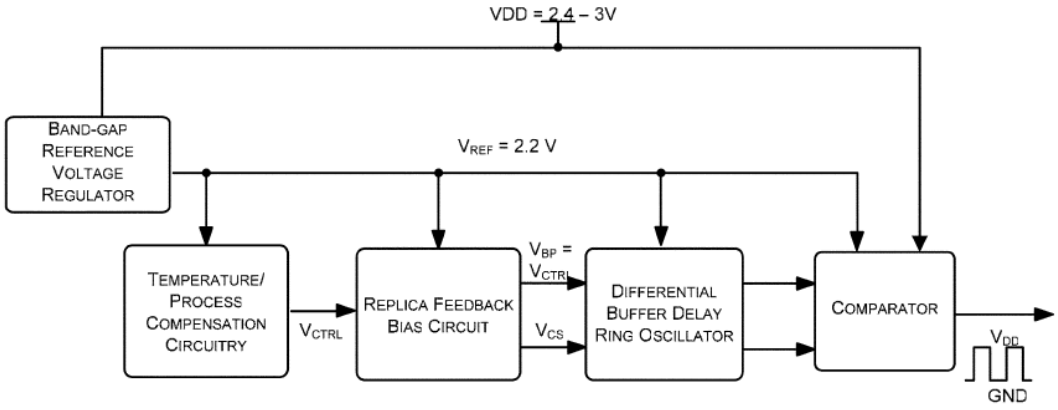

Figure 1-10 Block diagram of the temperature and process compensated ring oscillator [17].

As discussed in Section 1.2.3.2, analog implementation is not desired in our design because there is no available model beyond 225℃ for the selected SOI CMOS technology. Therefore, ring oscillator is not a good option for our application.

1.2.3.4 Thermal-Diffusivity-Based Frequency Reference

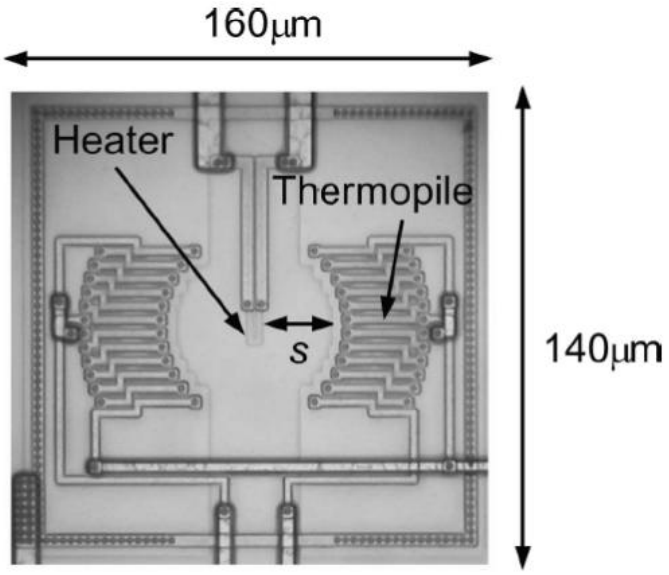

Figure 1-11 Photomicrograph of the ETF in 0.7μm CMOS [21].

An on-chip frequency reference exploiting the well-defined thermal-diffusivity (TD) of IC-grade silicon is proposed in [21]. A frequency-locked loop (FLL) is employed to lock the frequency of a digital controlled oscillator (DCO) to the process-insensitive phase shift of an electrothermal filter (ETF), which consists of a heater implemented in close proximity to a relative temperature sensor in the same silicon substrate. The photomicrograph of the ETF is shown in Figure 1-11. The heater is a thermopile made of p^+/Al thermocouples. The ETF behaves like a low-pass filter. The phase shift Φ_{ETF} introduced by the ETF is determined by its geometry, which is fixed by its layout, and by the temperature-dependent thermal-

diffusivity of bulk silicon, D [22]. At typical substrate doping levels, D is essentially process independent and therefore the phase delay is mainly determined by the accuracy of the lithography. The temperature dependence of D leads to a temperature dependent frequency reference, which is compensated by measuring the die temperature and injecting the temperature information into the FLL digitally.

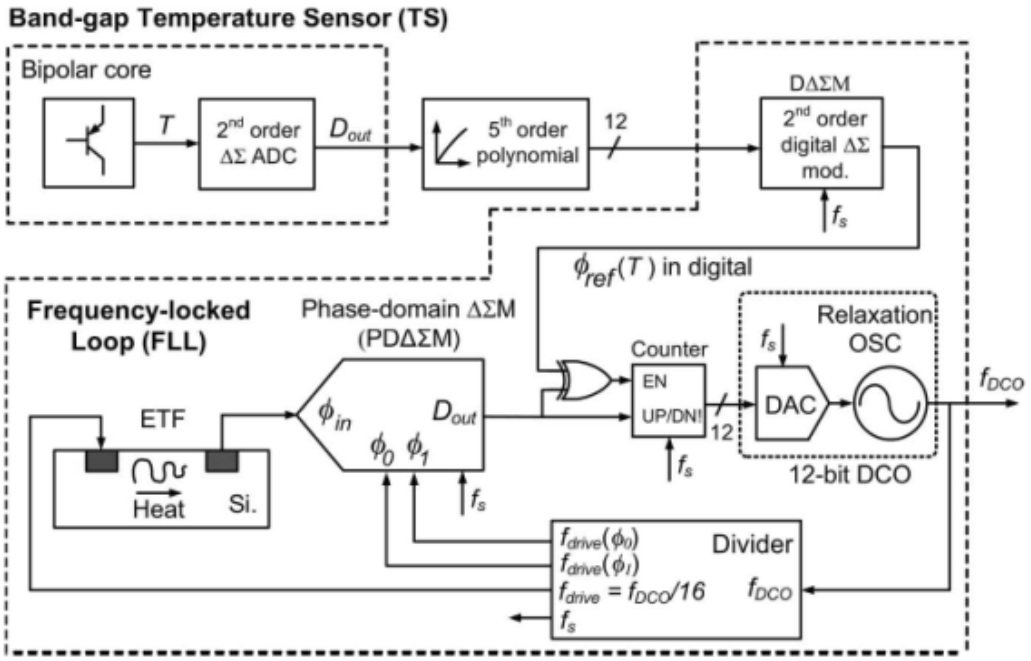

Figure 1-12 System-level block diagram of the TD frequency reference [21].

In the electrothermal FLL, Φ_{ETF} is extracted and digitized by a phase domain ΔΣ modulator (PDΔΣM). The phase reference Φ_{ref} is produced by the digital ΔΣM (DΔΣM). The bitstream is substracted from that of PDΔΣM and the resulting error signal is fed to a digital integrator, whose output drives the DCO. Feedback forces the DCO to oscillate at a frequency f_{VCO}, where $\Phi_{ETF}=\Phi_{ref}$. The temperature sensor (TS) provides a digital output which is proportional to the die temperature. It is then translated by means of a fifth-order polynomial into a 12-bit digital

number which represents the $\Phi_{ref}(T)$ and as a result the DCO generates a constant frequency of 1.6MHz. The frequency reference achieves an absolute inaccuracy of ±0.1% over the military temperature range (-55℃ to 125℃) with a single room-temperature trim. A scaled version implemented in 0.16μm process is presented in [23] with the same level of accuracy while achieving higher frequency, consuming less power and occupying smaller area.

The digital intensive architecture is suitable for high temperature operation. However, this design requires complicated calibration and accurate TS. Due to the complex digital signal processing, the up/down counter, frequency divider, the DΔΣM, the digital ΔΣ modulator producing the fine trimming word for the TS, and the decimation filter of the TS were realized off-chip, which leads to a non-fully integrated solution.

1.3 Design Consideration

Based on the operation condition in oil drilling pipes, the system specifications for acoustic transmitter are addressed here. This work does not include the power amplifier design, so the output power is not our concern. The majority of the power consumed by the acoustic telemetry system should be dominated by the power amplifier, and therefore the requirement for the dc power consumption of acoustic transmitter is relaxed and will not affect the system specification.

First, according to the high temperature operation condition in the downhole drilling pipes and the requirement of qualification temperature as introduced in section 1.1, the acoustic transmitter should be able to work at a temperature up to 300℃.

Second, as the acoustic channel exhibits comb shape characteristics shown in Figure 1-1, acoustic carrier should locate accurately within the frequency range of the acoustic passband. A temperature-independent frequency reference is needed to generate the required acoustic carrier. The frequency range of acoustic carrier is between 310Hz to 980Hz, because the 2^{nd}, 3^{rd} and 4^{th} acoustic passbands are selected for transmission in this work. The bandwidths of employed acoustic passbands are around 100Hz. Therefore, the frequency variation of acoustic carrier should be less than ±30Hz to guarantee that the acoustic carrier will not fall out of the acoustic passband range for all the temperatures, which leads to the frequency inaccuracy requirement of ±30/980(≈±3%) for the frequency reference.

Third, the data rate per channel is limited by the inter-symbol interference (ISI). According to the study of acoustic channel modeling, the impulse response has significant echoes. Hence the acoustic receiver needs to operate at lower data rate to minimize transmission errors due to the ISI. The data rate per channel is mainly determined by the acoustic channel characteristic unless more complicated and spectral-efficient modulation is employed. In this work, the total data rate is improved by employing multi-channel scheme despite ISI. Thanks to the SoC integration, it simplifies the ways of creating multi-channel signal and help attaining higher data rate. Therefore, the same data rate per channel of 20bps is adopted in our design, the same as in Ref [1] and [6].

Fourth, the signal-to-noise ratio (SNR) requirement for acoustic transmitter needs to be studied. The noise sources consist of the acoustic transmitter's noise and the drilling noise existing in the acoustic channel. According to the acoustic telemetry

system in Ref [1], the data can be robustly recovered at 20bps per channel at the drilling noise's SNR level above 10dB, as shown in Figure 1-13. Due to the lack of field test, the same assumption is applied to our design. The signal generated by the acoustic transmitter is verified under the condition that the drilling noise's SNR is 10dB. In the complete acoustic telemetry system, there are several methods to alleviate the drilling noise, such as optimizing the acoustic transmitter and receiver's positioning, adding an acoustic attenuator before the acoustic transmitter and placing the repeaters between the acoustic transmitter and receiver, which may result in a better drilling noise's SNR. In order to make the drilling noise dominant, the SNR of the transmitter's noise is required to be at least 20dB. Therefore, the noise from acoustic transmitter is ten times smaller than the drilling noise. In this case, the effect of the acoustic transmitter's noise can be neglected. Table I shows the summary of the system specifications for acoustic transmitter.

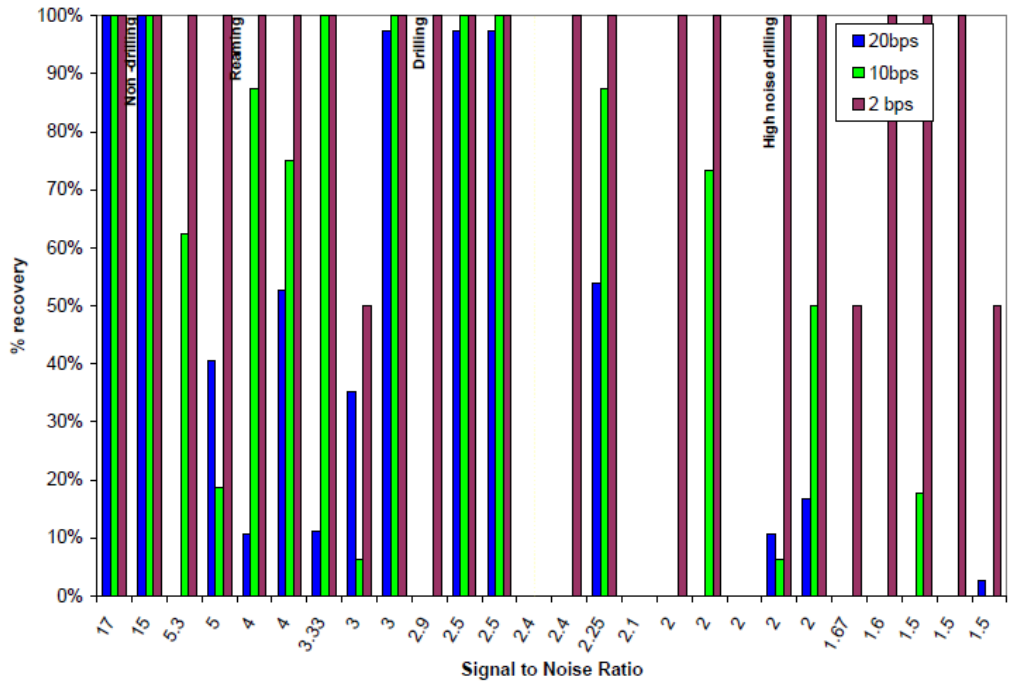

Figure 1-13 Data recovery at various rates for various noise conditions [1].

Table 1-1 SUMMARY OF SYSTEM SPECIFICATIONS FOR ACOUSTIC TRANSMITTER

	Specification
Temperature	Up to 300° C
Carrier Frequency	310Hz ~ 980Hz
Frequency Inaccuracy	±3%
Data Rate per Channel	20bps
SNR	20dB

1.4 Thesis Organization

As motivated by the above mentioned demand of acoustic telemetry system, this work presents a reconfigurable acoustic telemetry transmitter employing crystal-less temperature-independent frequency reference. Chapter 2 introduced the realization of crystal-less temperature-independent frequency reference based on RC phase shifter. Temperature compensation technique was also studied to resolve the high temperature operation issues. Chapter 3 presented another approach of crystal-less temperature-independent frequency reference, which employs a frequency-to-voltage converter (FVC). Chapter 4 firstly analyzed OOK and chirp modulation. Subsequently, the architecture of reconfigurable acoustic telemetry transmitter was presented and the advantages of such architecture were discussed. Chapter 5 summarized the major achievements of this work. Some suggestions on future improvement also have been discussed.

1.5 Publication

Lianhong Zhou, Muthukumaraswamy Annamalai, Jeongwook Koh, Minkyu Je, Libin Yao, Chun-Huat Heng, "A crystal-less temperature-independent reconfigurable transmitter targeting for high temperature wireless acoustic telemetry applications," IEEE Transactions on Circuits and Systems II, vol. 60, no. 9, pp. 542-546, Sep. 2013.

Lianhong Zhou, Wei Kwang Han, Lakshmi Sutha Kumar, Muthukumaraswamy Annamalai, Minkyu Je, Yong Liang Guan, Libin Yao, Chun-Huat Heng, "25 to 300 degree Celsius 80bps acoustic transmitter based on crystal-less temperature-independent frequency reference with differential modulation for drilling noise power cancellation," IEEE Asian Solid-State Circuits Conference, 23-6, pp. 453-456, Singapore, Nov. 2013.

Lianhong Zhou, Muthukumaraswamy Annamalai, Minkyu Je, Libin Yao, Chun-Huat Heng, "A fully integrated temperature-independent reconfigurable acoustic transmitter with resistor temperature coefficient calibration for oil drilling application," IEEE Transactions on Circuits and Systems II, pending submission.

1.6 Conclusion

From the above discussion, it is not trivial to achieve a high data rate acoustic transmitter operating in the temperature range up to 300℃. Due the comb shape characteristic of acoustic channel, the transmitter frequency needs to be tunable and stable to ensure maximum passband utilization for optimum performance. On chip reference is preferred due to its compactness and ease of packaging. However, to date, there is still no reported on chip reference operating at such

high temperature with sufficient accuracy. Finally, a fully integrated acoustic transmitter solution with reconfigurability will be attractive in terms of ease of packaging and on the field programming. In the subsequent chapter, we will elaborate on our approach to tackle the issues mentioned in this chapter.

Chapter 2 Crystal-Less Temperature-Independent Frequency Reference Based on RC Phase Shifter

2.1 System Architecture

2.1.1 Operation Principle

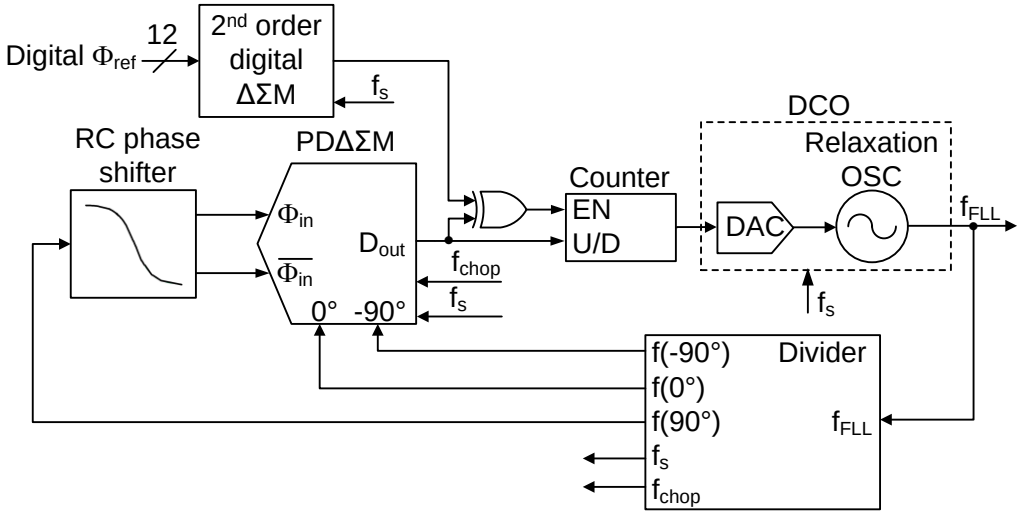

Figure 2-1 Proposed crystal-less temperature-independent frequency reference.

Due to the pipe-dependent channel characteristic mentioned earlier with ~100Hz channel bandwidth, the transmitter must have good frequency stability (±3%) and be tunable with fine frequency resolution (<1Hz). We propose crystal-less temperature-independent frequency reference as shown in Figure 2-1 to achieve the desired frequency stability. The architecture is similar to [21] where frequency locked-loop (FLL) and phase shifter are employed to create temperature-insensitive frequency reference. However, in [21], electro-thermal filter (ETF) combined with pre-measurement and calibration are needed to perform 5th-order polynomial mapping for temperature coefficient (TC) compensation. In addition,

due to the extensive digital signal processing, all digital circuitries are implemented through external FPGA.

In this implementation, we eliminate unnecessary blocks such as ETF, temperature sensor and polynomial mapping to simplify the design and provide fully integrated solution. This is possible due to the relaxed frequency stability requirement for the targeted application (±3% versus ±0.1% in [21]). In the proposed solution, we employ temperature-independent RC phase shifter instead of ETF. This eliminates the need for polynomial mapping to compensate the TC of ETF.

The digitally controlled oscillator (DCO) output first goes through a digital frequency divider to reduce the frequency by sixteen times. The divider output is then sent to the temperature-independent RC phase shifter. The resulting output is digitized through a phase domain ΔΣ modulator (PDΔΣM) and compared with a digital phase reference. The comparison is done after the digital phase reference has been converted to an equivalent bit stream through a 2^{nd} order digital ΔΣM. The resulting error is then integrated through a digital counter. The filtered output will adjust 12-bit DCO. The FLL is updated at frequency $f_s=f_{FLL}/512$. As the temperature-independent RC phase shifter provides one-to-one relationship between frequency and phase, the FLL will ensure that the DCO generates temperature-independent frequency output under equilibrium for a given fixed digital phase reference. The digital phase reference can be tuned to give the desired output frequency and is set to ~1.22MHz in this implementation. To ensure the robustness of the architecture under high temperature operation, we

have adopted a digitally intensive architecture. The DCO, the frequency divider, the loop filter, the input phase reference and the phase comparison are all implemented in digital domain to minimize the impact of analog circuit variations at high temperature.

2.1.2 Matlab model

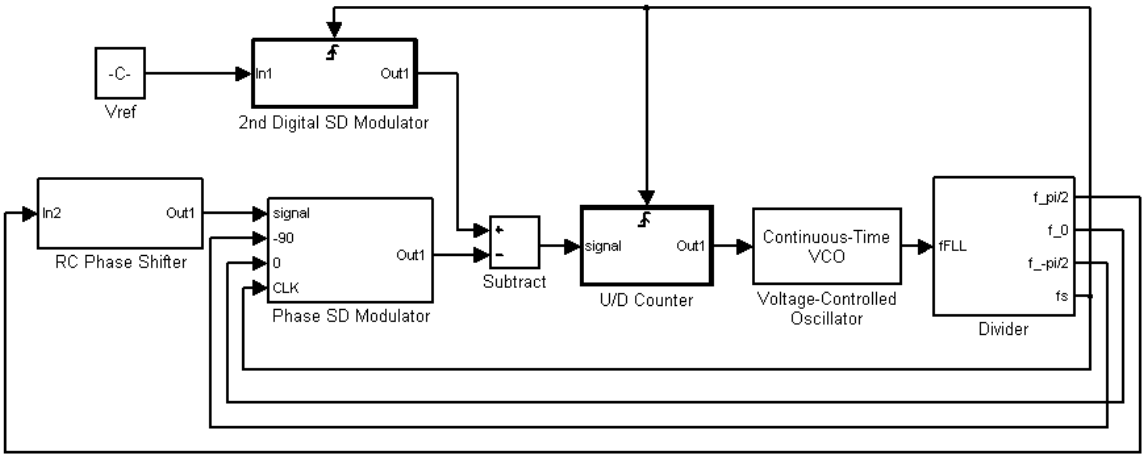

Figure 2-2 Matlab model of proposed frequency reference.

A Matlab model is built to verify the proposed architecture in system-level, as shown in Figure 2-2. Some blocks are the standard blocks provided by Matlab, such as the constant block of Vref, the Subtract block and the Voltage-Controlled Oscillator (VCO). The rest blocks are self-built. The RC phase shifter is basically a low pass filter, which is realized by a continuous transfer function block. Figure 2-3 shows the block diagram of the divider, which provides the operation clock fs of the loop and different phase versions of the signal f. The different phases are realized by setting different initial states for the Counter block. Both 2nd Digital SD Modulator and U/D counter are triggered subsystems, whose operation frequency is fs generated by the Divider. The block diagram of U/D counter is

shown in Figure 2-4. The block diagram of 2nd Digital SD Modulator is shown in Figure 2-5. In order to model the digital signal operation, the signal attribute is set to be fixed-point data type. The coefficients of the 2nd Digital SD Modulator are designed using the functions provided by Matlab Delta-Sigma Toolbox. Figure 2-6 shows the block diagram of Phase SD Modulator, and the operation principle will be explained in section 2.2.3.

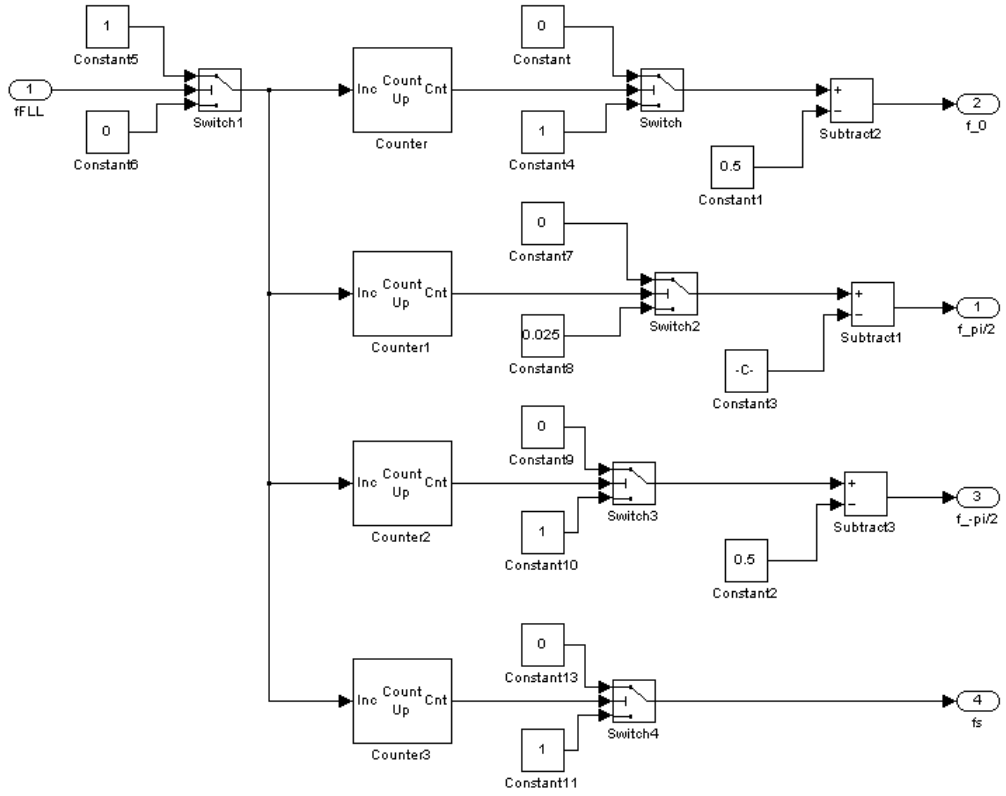

Figure 2-3 Block diagram of Divider.

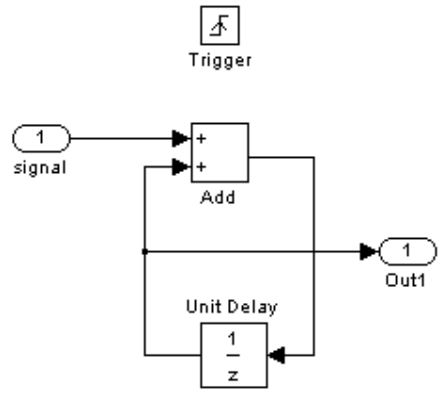

Figure 2-4 Block diagram of U/D counter.

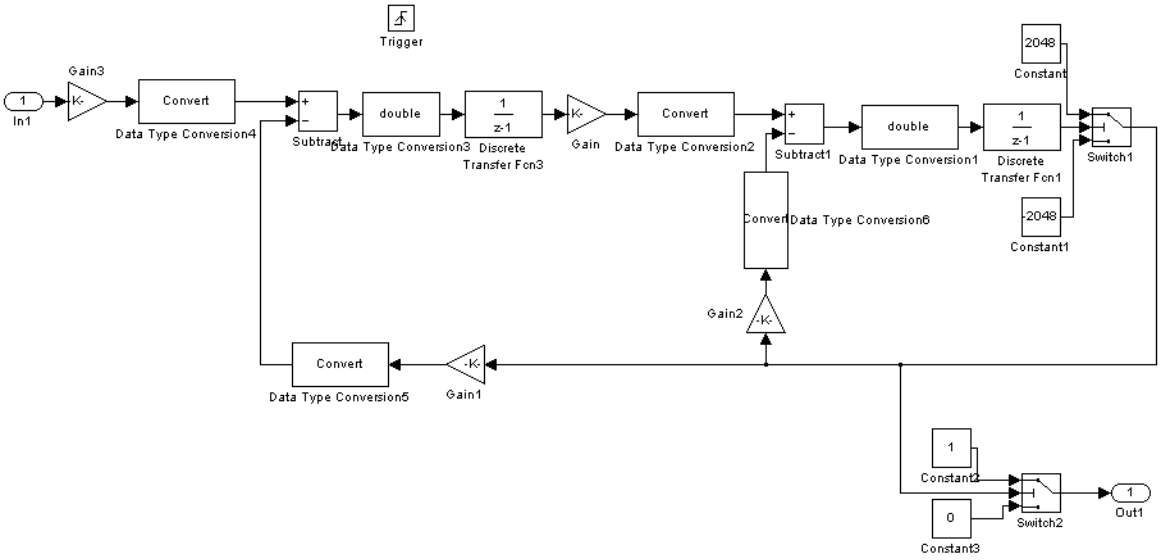

Figure 2-5 Block diagram of 2nd Digital SD Modulator.

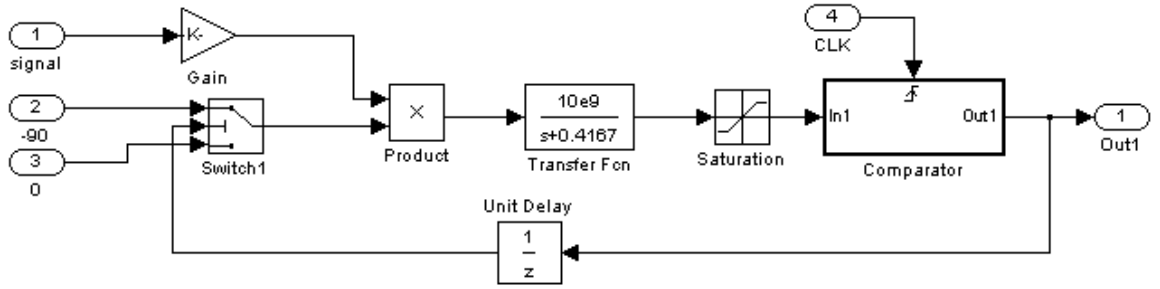

Figure 2-6 Block diagram of Phase SD Modulator.

The nominal frequency of VCO is set to be 1.22MHz and the input sensitivity is 800Hz/bit. RC phase shifter is assumed to be temperature-independent and all the

digital blocks are considered to be temperature-stable. Therefore, the most temperature-sensitive block is the VCO. Suppose the actual operating frequency of VCO drifts to different values due to the temperature variation. The FLL should tune the VCO's frequency back to 1.22MHz with a proper fixed Vref. The following figures show the simulation results with the actual free-running frequency of VCO set to be 1.25MHz and 1.2MHz, respectively. As shown in Figure 2-7(a), the average value of VCO input settles o -38.68, which adjusts the VCO to operate at the frequency of 1.22MHz. While in Figure 2-7(b), the average value of VCO input becomes stable at 23.24 with the resulting VCO frequency of 1.22MHz.

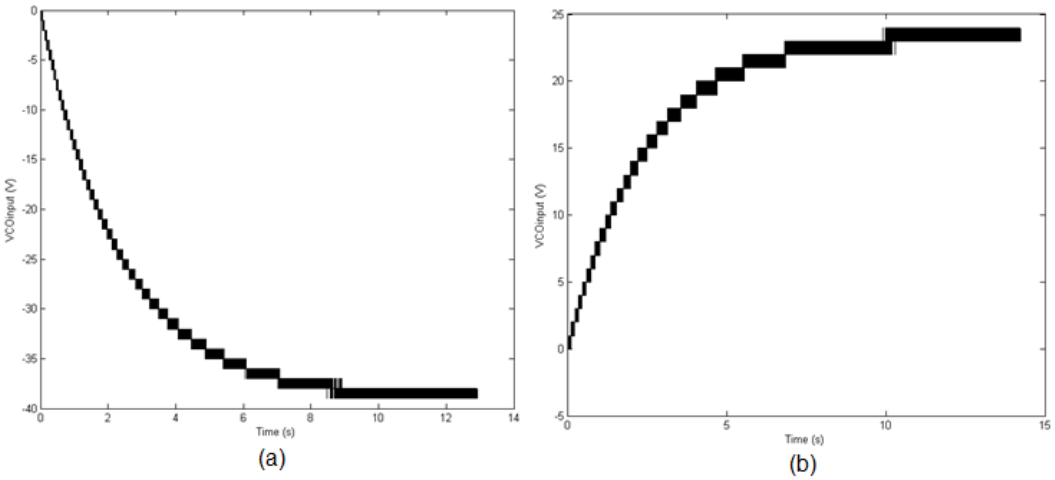

Figure 2-7 Simulation results of VCO free-running frequency (a) 1.25MHz and (b) 1.2MHz.

2.2 Circuit Implementation

2.2.1 SOI process

This work is supported by IME A*STAR Singapore, and part of the rugged electronic project where 1µm SOI CMOS technology is chosen for high temperature operation application. This work is subjected to the constraint of

using this process to ensure consistencies throughout the entire rugged electronic project because there are also other research groups involved, such as modeling. Compared to the conventional CMOS process, a layer of electrical insulator is introduced between the substrate and the silicon device in SOI CMOS process as shown in Figure 2-8(b), which brings several advantages [25]. First, the junction capacitance is gradually reduced as well as the leakage current. Therefore, the leakage power dissipation can be relieved for high temperature operation. Meanwhile, the SOI structure not only isolates the device from substrate, but also from each other. The latch up problem in conventional CMOS process is resolved in SOI process since the bottom of the device is fully covered by insulator, which eliminates the substrate noise and crosstalk. Although the SOI CMOS technology can only support to 225℃, in order to satisfy the requirement of the oil drilling application, we have to further push the temperature limitation higher, and the digital intensive architecture can provide the opportunity of doing this.

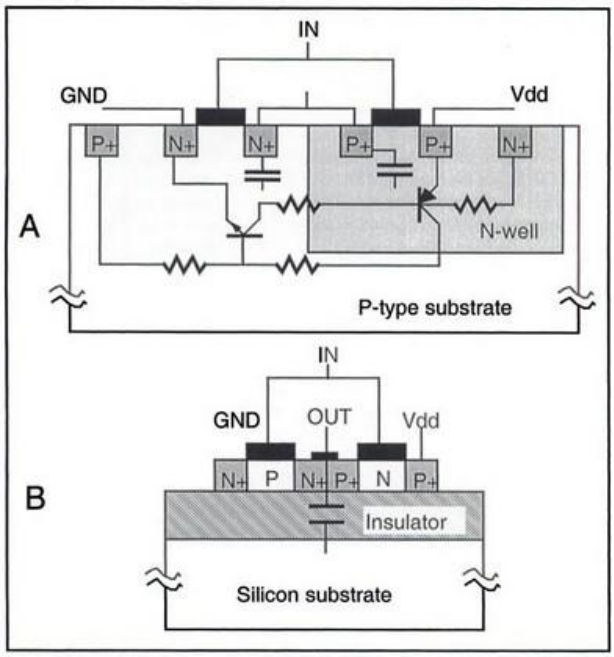

Figure 2-8 Cross section of (a) a bulk CMOS inverter (b) a SOI CMOS converter [24].

2.2.2 Temperature-Independent RC Phase Shifter

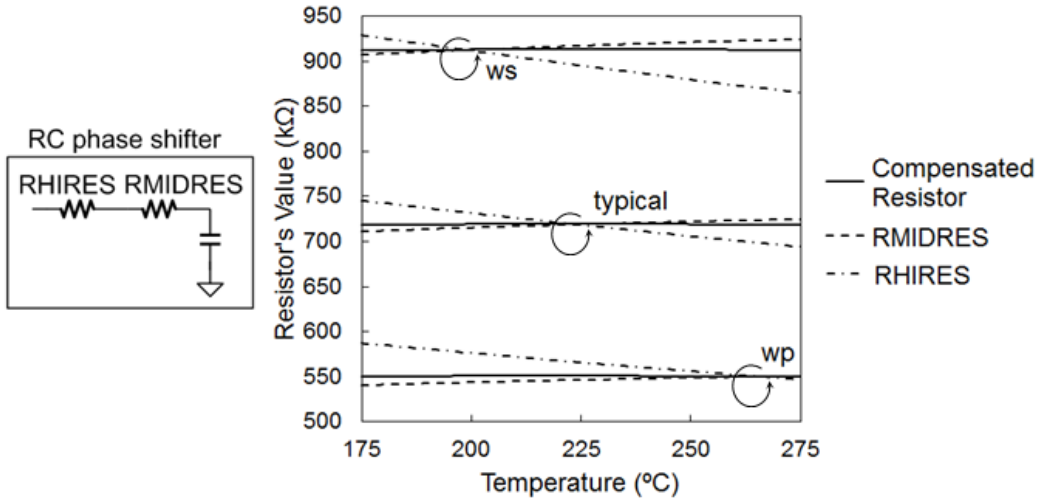

Figure 2-9 Circuits of RC phase shifter and simulation result of resistor TC compensation.

The temperature-independent RC phase shifter is basically an RC low pass filter employing resistor TC compensation technique, as shown in Figure 2-9. In RC phase shifter, the main error caused by temperature variation comes from the resistor, considering the TC of the capacitor is relatively small, which is 0.023×10^{-3}/K in 1μm SOI CMOS technology, and thus can be ignored. The temperature dependence of passive resistor can be modeled as a linear equation with TC.

$$RHIRES(T) = R_1(T_0) \times [1 + TC_1 \times (T - T_0)] \tag{2.1}$$

$$RMIDRES(T) = R_2(T_0) \times [1 + TC_2 \times (T - T_0)] \tag{2.2}$$

$$R_{total} = R_1(T_0) + R_2(T_0) + (T - T_0)[R_1(T_0)TC_1 + R_2(T_0)TC_2] \tag{2.3}$$

$$\frac{R_1(T_0)}{R_2(T_0)} = -\frac{TC_2}{TC_1} \tag{2.4}$$

The series combination of the two types of resistors with positive and negative TCs, respectively, and proper sizing can provide temperature-independent overall resistance. In equation 2.3, in order to make the TC of R_{total} be zero, the ratio of

two resistors has to satisfy the relationship shown in equation 2.4. In this work, two different types of resistors RHIRES and RMIDRES with opposite TC of -0.86×10^{-3}/K and 0.48×10^{-3}/K, respectively, are chosen. The values of these two resistors are set with proper ratio such that the combined resistors exhibit near zero TC at the desired high temperature range. As the actual resistor value fabricated is expected to vary with process corner, this will affect the effectiveness of TC compensation technique. To investigate the impact, the temperature effect of combined resistor is studied under different corner. As illustrated, the obtained combined resistance exhibit very small temperature dependency of 0.03×10^{-3}/K, which should lead to temperature-independent phase versus frequency characteristic. Nevertheless, the ultimate accuracy of process model will determine the effectiveness of this method. Normally, resistor calibration is adopted to tune the process variation in order to improve the accuracy of the resistor's value. But it is not used in our design for the following reasons. The common way of tuning a resistor's value is to implement it as a resistor array. However, the ratio of two resistors in TC compensation technique is a fractional number. It is difficult to realize an accurate fractional value through the resistor array. The accuracy of the ratio is determined by the resolution of the resistor array. If we want to improve the accuracy, we have to increase the size of the resistor array and reduce the value of the unit resistor. A large resistor array will make the design complex. Besides, if the unit resistor is too small, then the resistance of the switch will become comparable. The temperature characteristic of the switch resistance is hard to predict and cannot be compensated. Therefore,

resistor calibration using resistor array is not employed here. In chapter 5, a novel method of resistor calibration is proposed.

2.2.3 Phase Domain ΔΣ Modulator

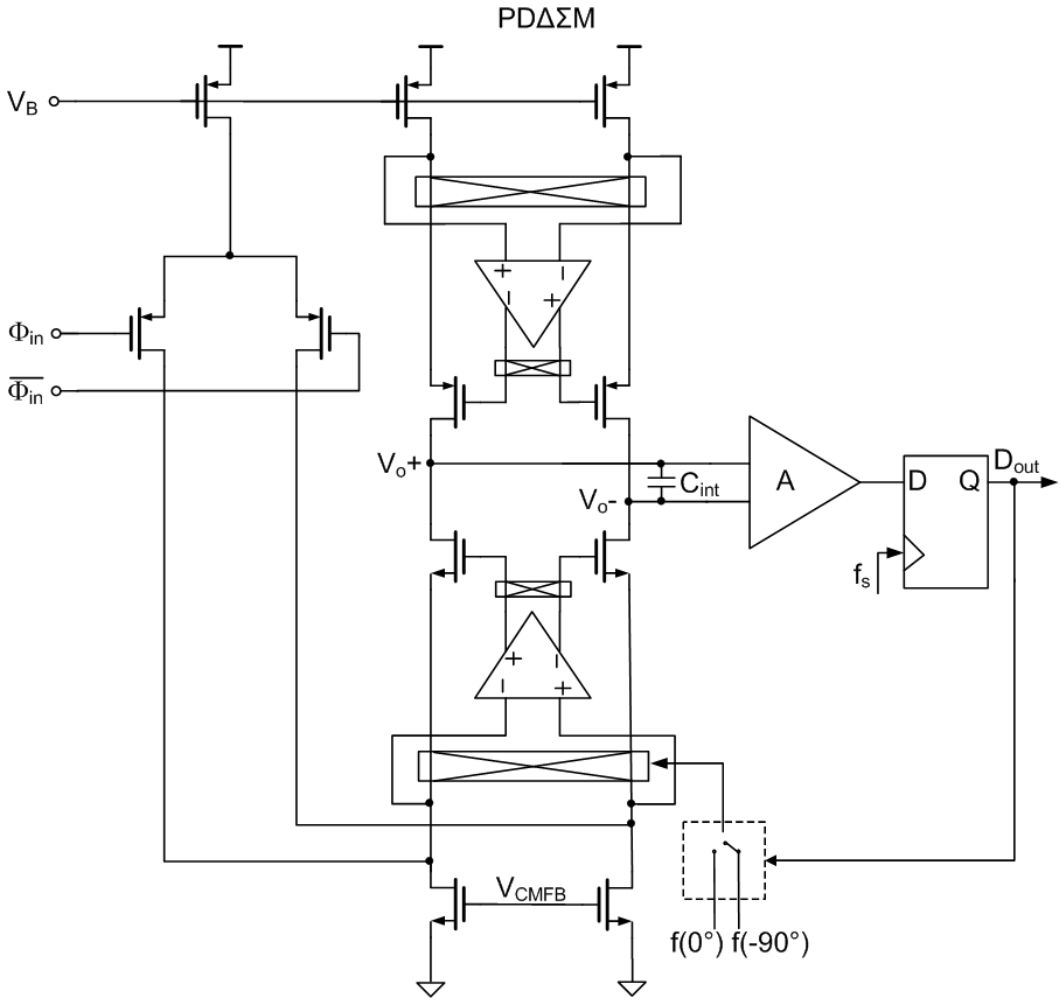

Figure 2-10 Block diagram of the PDΔΣM.

The circuit of PDΔΣM is shown in Figure 2-10, whose output bit stream is the digital representation of the phase shift introduced by RC phase shifter. Here, a transconductor with embedded chopper demodulator similar to [26] is employed. The PDΔΣM consists of a demodulator, an integrator, a quantizer and a 1-bit phase DAC. Depending on the output of D-latch, either f(0°) or f(-90°), which are

generated from a digital frequency divider, is selected to multiply with the phase shifted version of f(90°) through the demodulator. The demodulator output contains a DC current term that is proportional to $\cos(\Phi_{in}-\Phi_{FB})$, where Φ_{FB} is either 0° or -90° depending on the PDΔΣM's output bitstream. This DC term is extracted out through the C_{int}, which also filters out the harmonics of f(90°) existing at the output of the demodulator. The voltage across C_{int} is amplified by an operational transconductor amplifier (OTA) and fed to a D-latch, which acts as the PDΔΣM's quantizer.

The input signal and feedback signal of the PDΔΣM can be expressed as:

$$V_{in} = A_1 \cos(2\pi f t + \varphi_{in}) \tag{2.5}$$

$$V_{FB} = A_2 \cos(2\pi f t + \varphi_{FB}) \tag{2.6}$$

where A_1 and A_2 are the amplitudes for the PDΔΣM's input signal and feedback signal, respectively. The transconductor g_m converts V_{in} into a current, which is then multiplied with V_{FB}. Therefore, the demodulator's output I_{out} is

$$I_{out} = A_1 \cos(2\pi f t + \varphi_{in}) \cdot g_m \cdot A_2 \cos(2\pi f t + \varphi_{FB}) \tag{2.7}$$

I_{out} is filtered by C_{int}, and the DC term is

$$I_{out,DC} = 0.5 A_1 A_2 g_m \cos(\varphi_{in} - \varphi_{FB}) \tag{2.8}$$

The feedback loop of the PDΔΣM tries to balance the accumulated charge on C_{int} to be zero, which means

$$\mu \cdot 0.5 A_1 A_2 g_m \cos(\varphi_{in} - 0°) + (1-\mu) \cdot 0.5 A_1 A_2 g_m \cos(\varphi_{in} + 90°) \approx 0 \tag{2.9}$$

where μ is the weighted average value of the PDΔΣM's output bitstream. From the above equation, we can get

$$\mu \approx \frac{\cos(\varphi_{in}+90°)}{\cos(\varphi_{in}+90°) - \cos(\varphi_{in}-0°)} \tag{2.10}$$

C_{int} of 200pF is implemented as poly-p+-diffusion capacitor, which exhibits negligible leakage behavior. Hence, the PDΔΣM's resolution is mainly limited by the charge leakage from C_{int} due to transconductor output path. To minimize this charge leakage, large output resistance of the transconducor is needed. Therefore, a gain boosted folded cascode architecture is selected to achieve an output resistance of 23GΩ [26].

In addition, the additional phase shift introduced by the input transconductor pair will affect the temperature independence of the FLL. Hence, they should also have sufficiently large gain-bandwidth product (GBW) (~64MHz). Although this will incur higher power penalty, it only poses a small fraction of power compared to the Class-D power amplifier (a few watts) and should not impact the operation of the transmitter.

As the input signal will mix with f(0°) or f(-90°) to obtain the DC phase error, any DC offset of the input transconductor pair will be transformed to high frequency component and filtered by the integrator. Hence, the matching of input transconductor pair is not important. However, the output DC offset current after the demodulator due to transistor mismatch will directly manifest itself as DC phase error and induce frequency inaccuracy. Therefore, the embedded chopper demodulator will shift any DC offset current to high frequency regime and thus can be removed easily by the integrator [26]. In addition, the gain boosted opamp input is connected to the demodulator input to present low impedance path to minimize the effect of offset current [26].

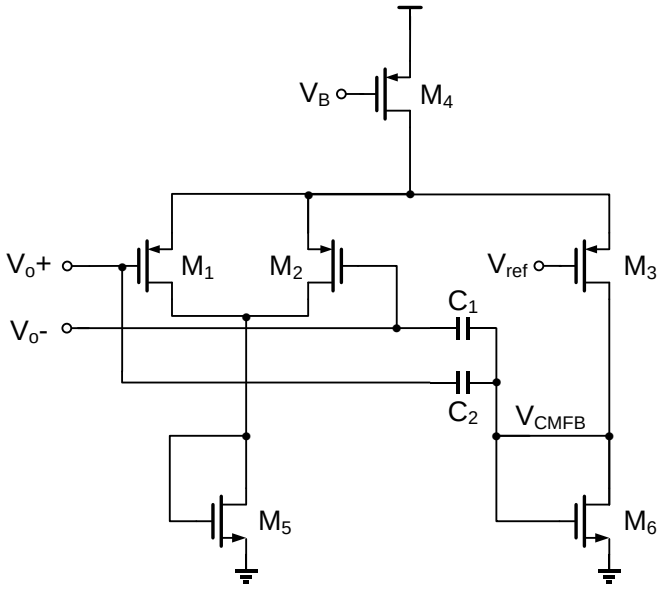

Figure 2-11 Circuit of CMFB.

For the fully differential transconductor, a common-mode feedback (CMFB) circuit is required in order to control the output common-mode voltage. The CMFB circuit can be implemented using continuous-time approach, where two large resistors are applied in order to obtain the output common-mode voltage. However, in our work, the transconductor has very large output impedance, which requires even larger sensing resistors in CMFB and thus occupies too much area. Switched capacitor based CMFB circuit can resolve such problem, but it will introduce the voltage droop issue and switch spikes [27]. Therefore, the CMFB is implemented as shown in Figure 2-11. However, this circuit suffers from limited input range. C_1 and C_2 are added to compensate the phase margin of CMFB loop. The CMFB loop can be considered as a two stage op amp which consists of the CMFB circuit (the first stage) and the differential transconductor (the second stage). Therefore, miller compensation technique can be employed here as C_1 and C_2 are placed between the output of the first stage (V_{CMFB}) and the output of the second stage (V_O+ and V_O-). As a result, the phase margin is improved from -53 °

to 39 ° at 25 ℃, as shown in Figure 2-12. Simulations are also run at different temperatures, and the compensated phase margin is 38 ° and 37 ° at 125 ℃ and 225 ℃, respectively.

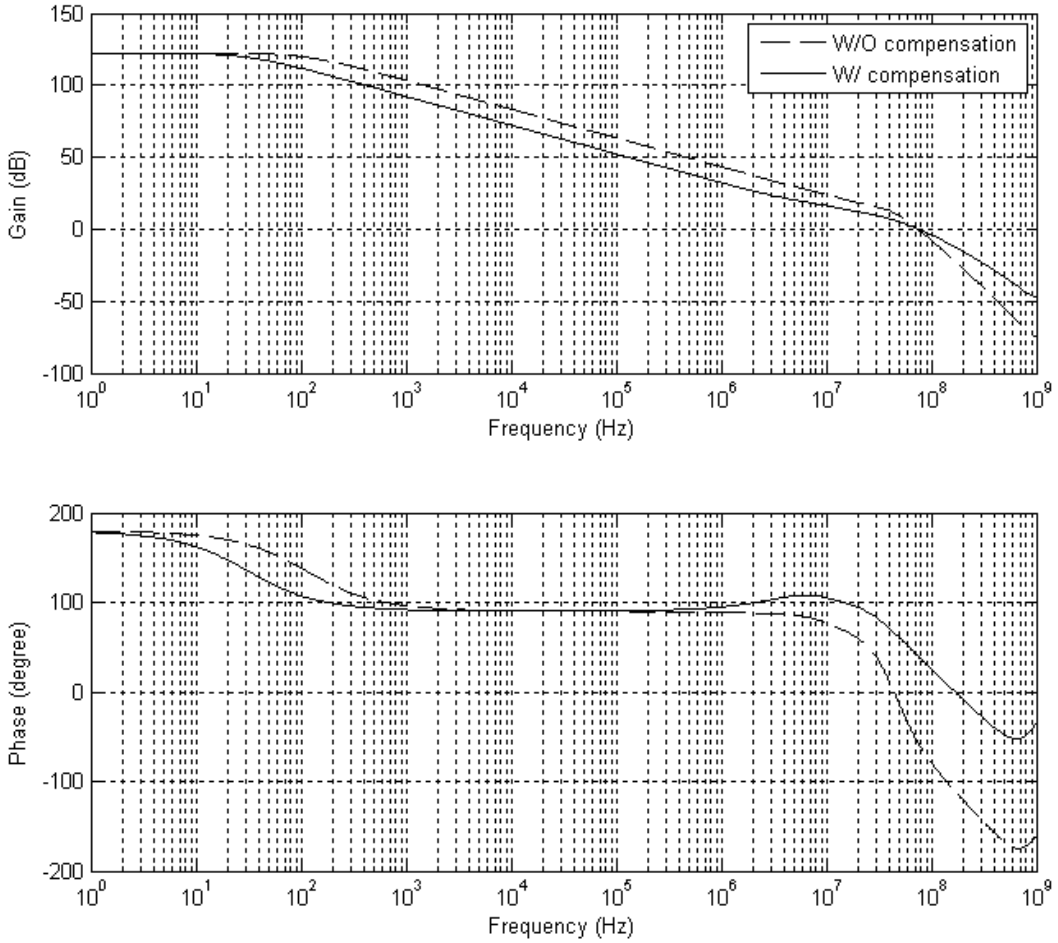

Figure 2-12 Simulation results of CMFB phase margin compensation.

The upper gain boosting amplifier of the transconductor is implemented as fully differential folded cascode amplifier with PMOS input, as shown in Figure 2-13 [26]. The common-mode level of the gain boosting amplifier is set by additional input pair whose gates are biased with an input common-mode voltage V_{incm}. The feedback loop between the input and output of the gain boosting amplifier via the main amplifier can regulate the output common-mode voltage of the gain

boosting amplifier such that the input common-mode voltage equals to V_{incm}. The bottom gain boosting amplifier is realized similarly with NMOS input.

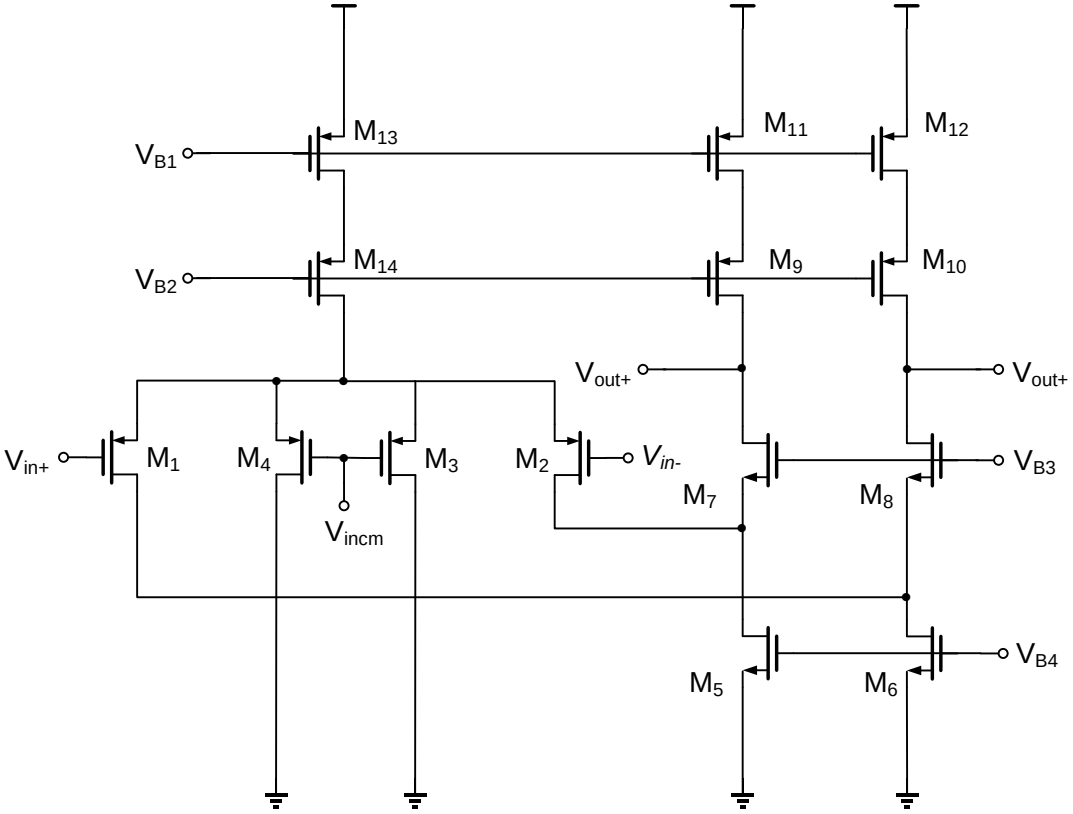

Figure 2-13 Circuit of upper gain booster amplifier.

The simulation results of the transconductor under different temperatures are presented in Figure 2-14. The achieved gain is 126dB which leads to an output impedance of 23GΩ.

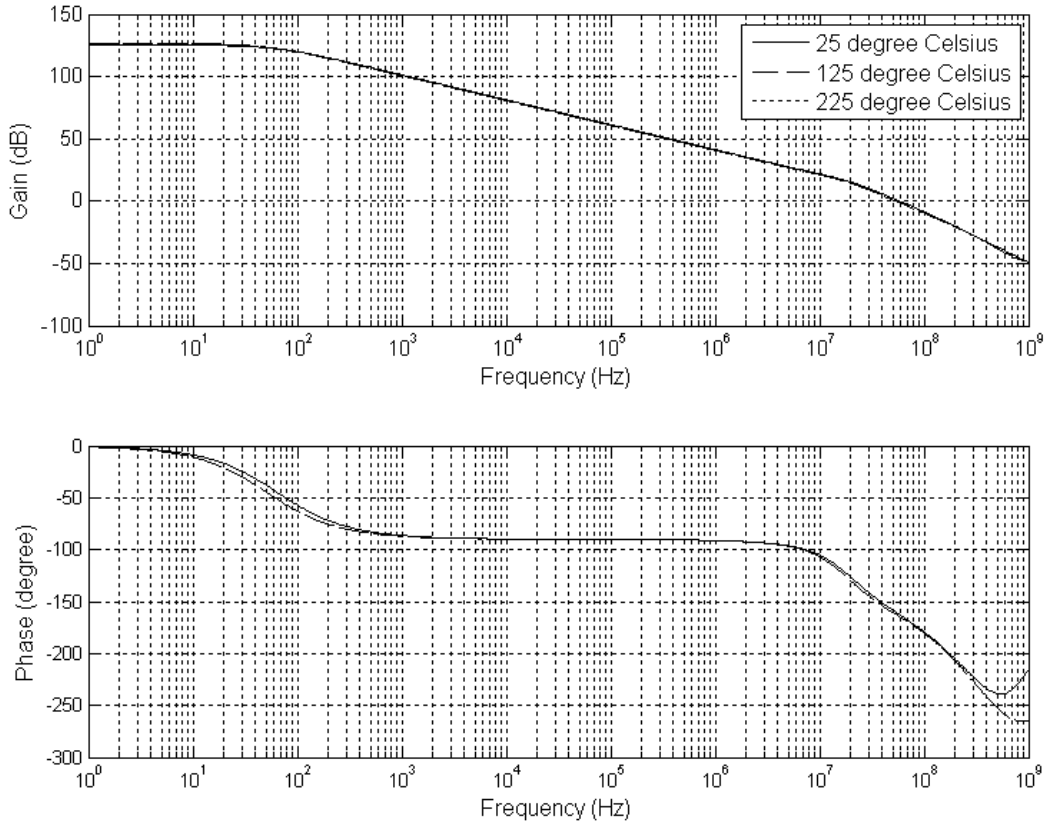

Figure 2-14 Simulation results of the transconductor's gain and phase at 25 ℃, 125 ℃ and 225 ℃, respectively.

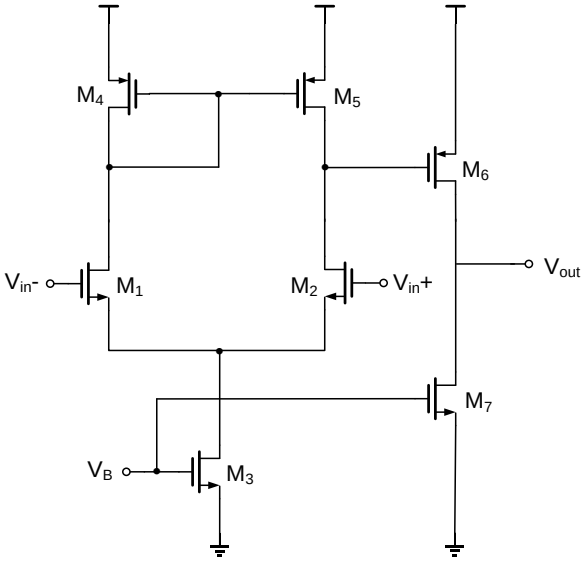

Figure 2-15 Circuit of differential-to-single-end amplifier.

The signal across C_{int} is buffered by an OTA before applied to the D-latch. The circuit is shown in Figure 2-15. The amplifier has a gain of 67dB and a rail-to-rail output.

The operation principle of PDΔΣM suggests that the output bitstream be temperature-independent because it is only determined by the two phase references and the input phase. The two phase references are generated by digital frequency divider, which is temperature-stable. However, there is leakage existing in C_{int} due to the finite output impedance of gain-boosted folded cascode amplifier which may vary under different temperature. The PDΔΣM is verified with the same phase input for different temperatures. Then the average value of the output bitstream is calculated and the inaccuracy is ±0.47% from 25 ℃ to 225 ℃.

2.2.4 12-bit DCO

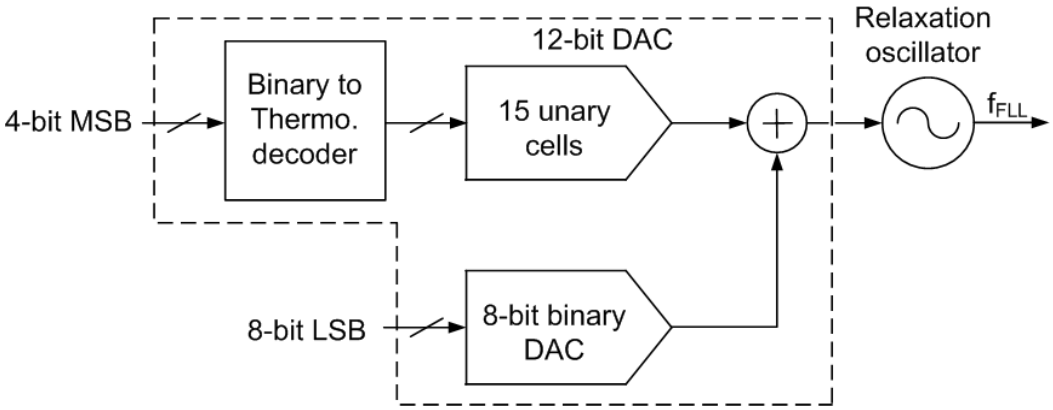

Figure 2-16 Block diagram of 12-bit DCO.

The DCO consists of a 12-bit segmented current steering DAC and a relaxation oscillator, as shown in Figure 2-16. The DAC is segmented into 4-bit MSB unary cells and 8-bit LSB binary cells, which can relax the matching requirement of current unit cell. The 4 MSBs are applied to a binary-to-thermometer decoder, and then drive 15 unary current cells. The 8 LSBs are fed to a binary-weighted DAC.

The block diagram of 12-bit current steering DAC is shown in Figure 2-17. DAC current unit sizing is chosen based on DAC resolution. Common-centroid layout is adopted to minimize the effect of process gradient. The output currents from

two segments are added and the summing current I_{DAC} directly controls the frequency tuning of the DCO with frequency resolution of 800Hz.

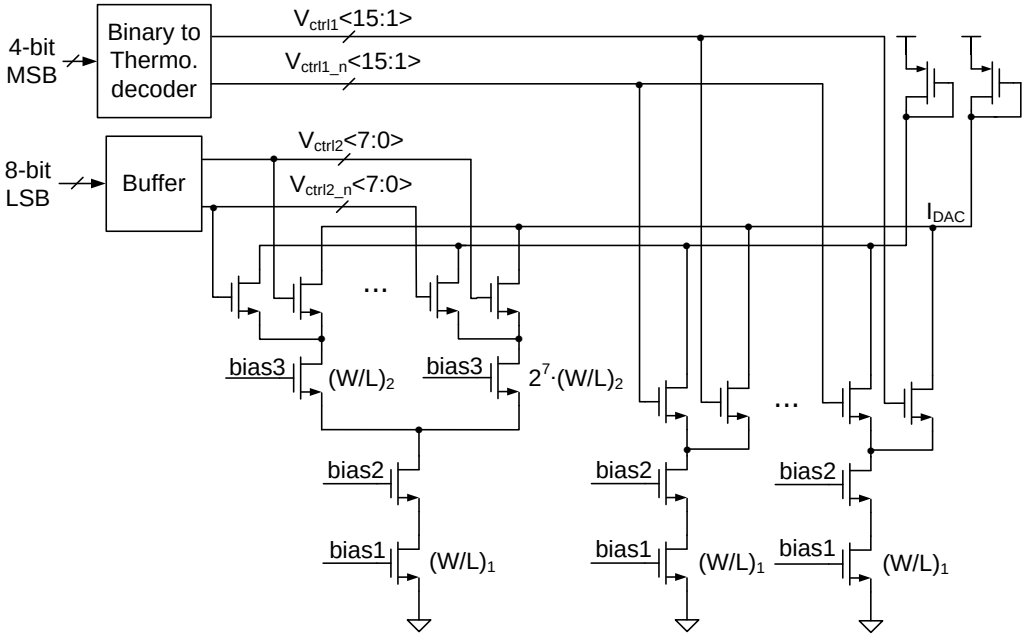

Figure 2-17 Block diagram of 12-bit current steering DAC.

In relaxation oscillator, based on the output of the latch, either C_1 or C_2 is charged to V_{dd} through M_1 or M_3, respectively, while the other capacitor is discharged by I_{DAC} via M_2 or M_4, as shown in Figure 2-18. When the voltage across the capacitors reduces to V_{ref}, the comparator's output will change the state of the SR latch. After a delay t_d, the latch toggles to the new state. Therefore, the period of relaxation oscillator is

$$T_{OSC} = \frac{2C(V_{dd}-V_{ref})}{I_{DAC}} + t_d \tag{2.11}$$

where $C=C_1=C_2$. In our work, C_1=1pF, V_{dd}=5V, and V_{ref}=2V. The kT/C noise of C_1 and C_2 is 64 μV at 300 ℃, which is much smaller than V_{dd} or V_{ref}. The cascode transistors M_5 and M_6 are gain boosted by the amplifier A, which ensures that the

current ratio is well defined despite the voltage excursion on C_1 and C_2 and the variation of I_{DAC}.

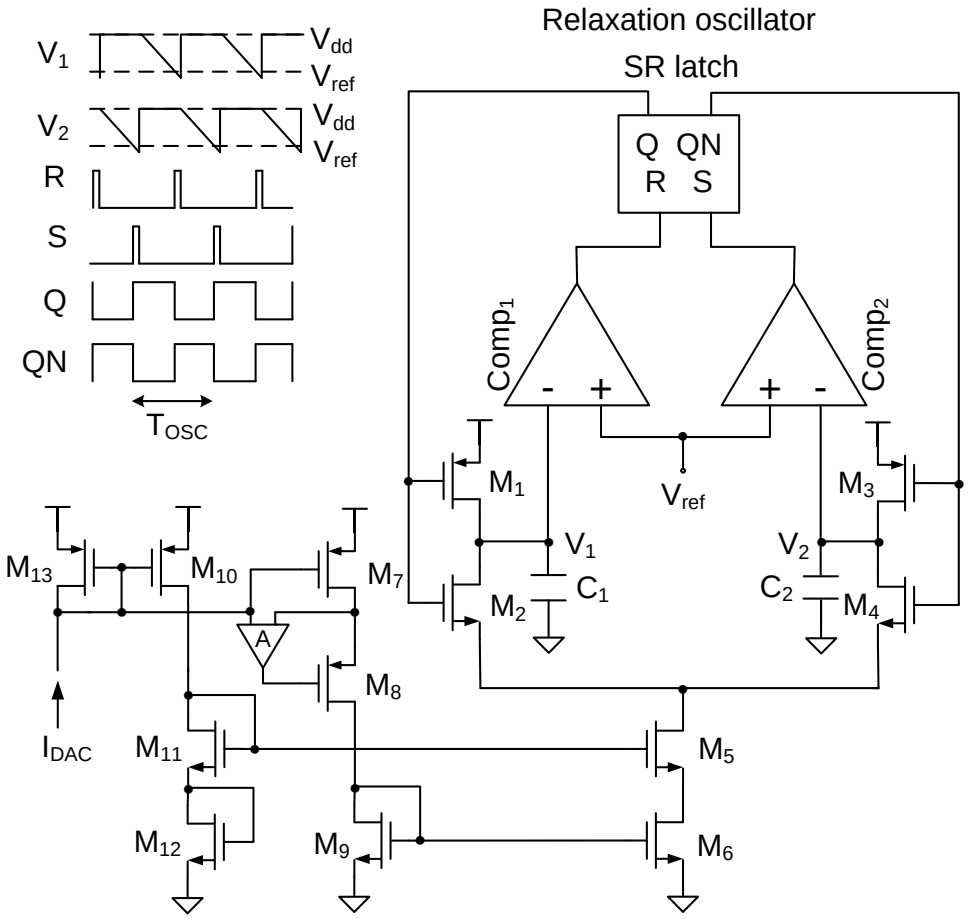

Figure 2-18 Block diagram of relaxation oscillator.

In the comparator, the switching activity can cause the kickback noise problem. The large voltage variation may be coupled through the parasitic capacitor of the input transistor to the input node. The input voltage is distorted because the circuit before the comparator does not have zero output impedance, which degrades the accuracy of the comparator. Therefore, the comparator is implemented with built-in 50mV hysteresis to minimize the kickback noise effect, as shown in Figure 2-19 [28]. Although this will affect the DCO output frequency accuracy, this inaccuracy will be tuned out by the feedback loop action of FLL.

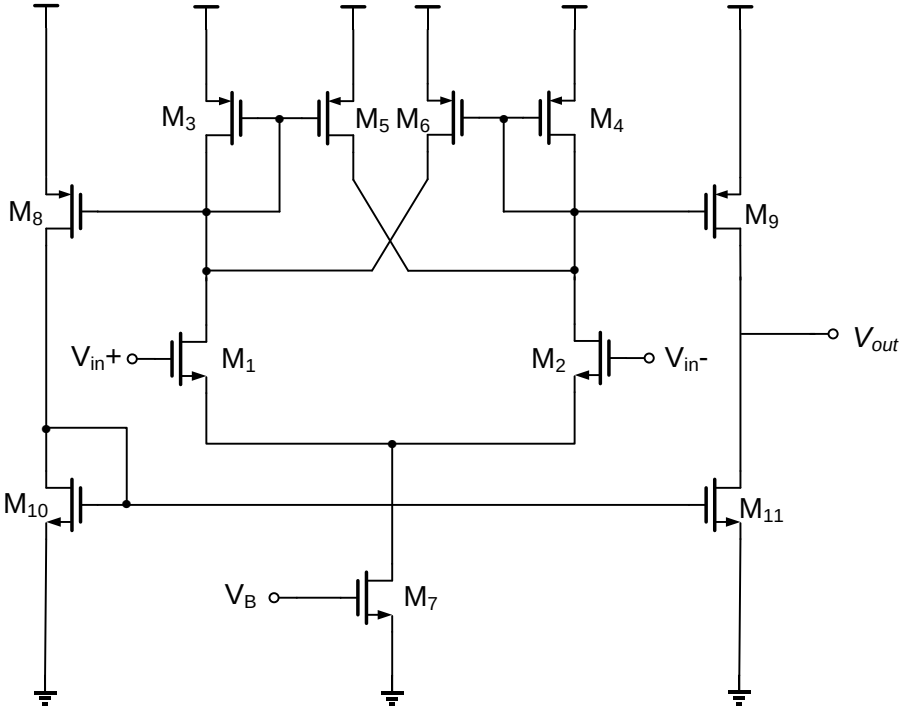

Figure 2-19 Circuit of comparator with hysteresis.

The simulation results of the comparator with hysteresis are shown in Figure 2-20. The comparator is designed such that under different temperatures the hysteresis range is wide enough to cancel the kickback noise.

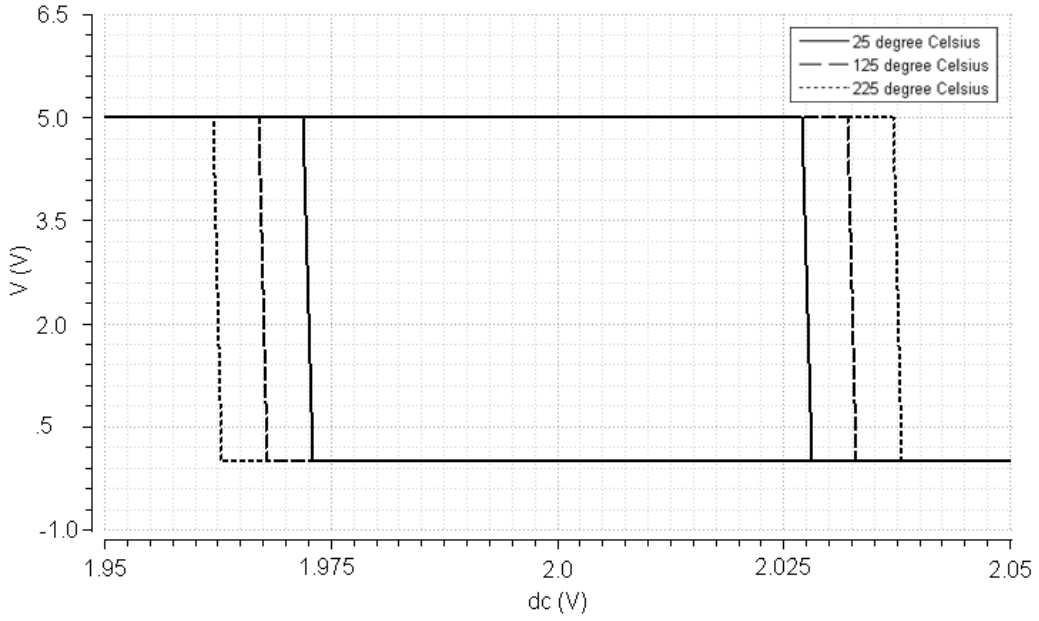

Figure 2-20 Simulation result of the comparator with hysteresis at 25 ℃, 125 ℃ and 225 ℃, respectively.

2.2.5 Digital ΔΣ Modulator

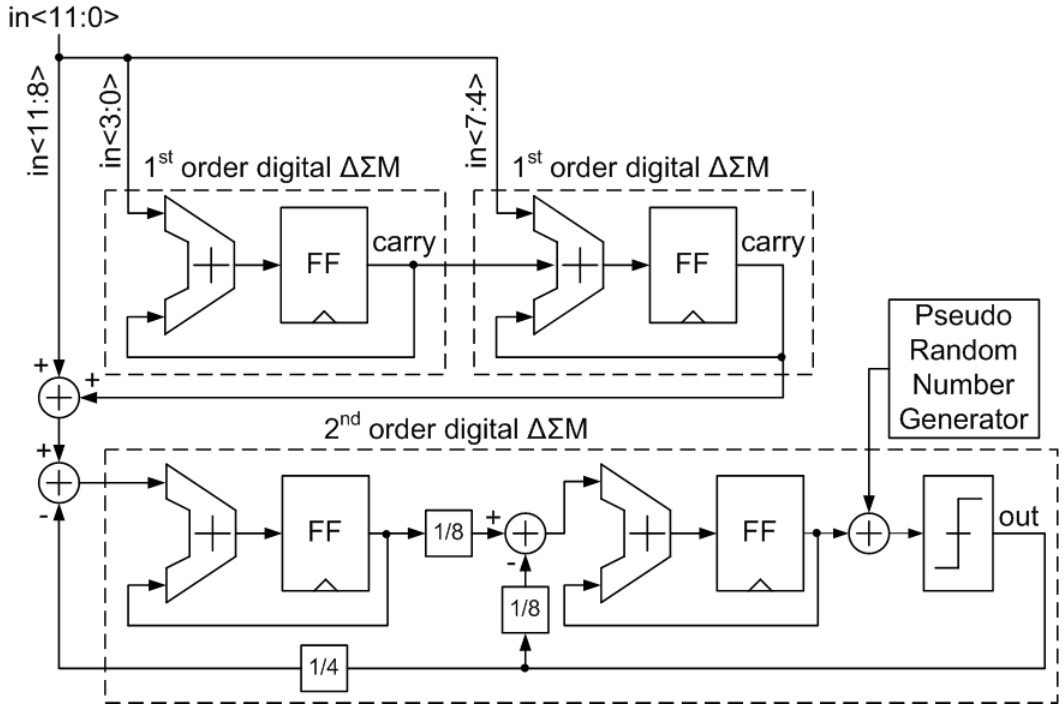

Figure 2-21 Block diagram of 12-bit 2nd order digital ΔΣ modulator.

The 12-bit 2nd order digital ΔΣ modulator converts the digital phase reference Φ_{ref} to a digital bitstream for FLL's loop comparison. In order to decrease the power consumption and the area, the digital ΔΣ modulator is implemented with reduced bit-width accumulator [31]. The 2nd order digital ΔΣ modulator consists of two 4-bit 1st order digital ΔΣ modulators and a 4-bit 2nd order digital ΔΣ modulator. The 1st order digital ΔΣ modulators converts the 8 LSBs of 12-bit input to 1-bit output which is used to dither the input of the 2nd order digital ΔΣ modulator. The architecture is shown in Figure 2-21. The coefficients of the 2nd order digital ΔΣ modulator are selected to minimize the circuit complexity. The digital ΔΣ modulator is realized through Verilog. The simulation result is shown in Figure 2-22 with a constant input. Due to the periodic action in digital circuits, the FFT results exhibits these spurious tones. Therefore, a pseudo-random number

generator is introduced and the 1-bit output is added with the second accumulator's result of the 2nd order digital ΔΣ modulator.

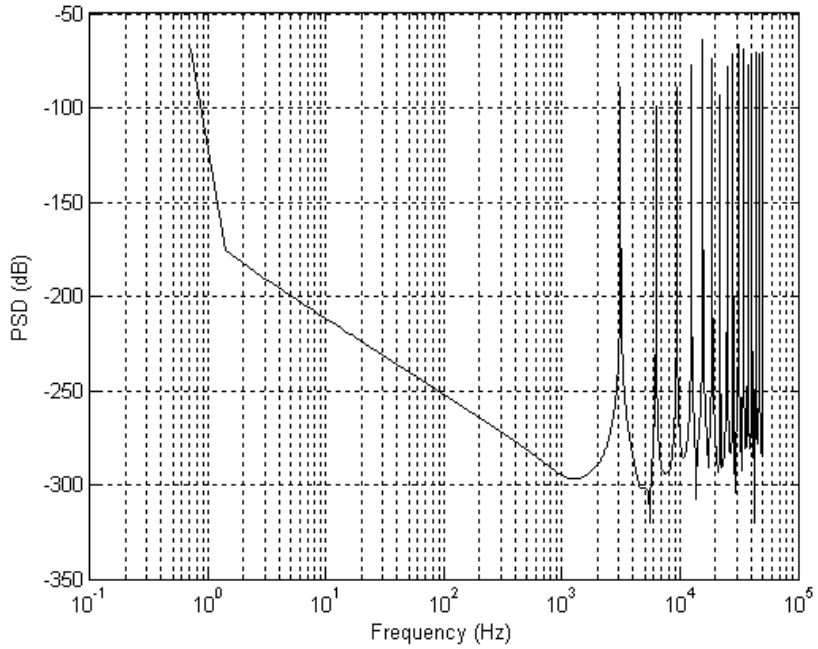

Figure 2-22 FFT of 12-bit 2nd order digital ΔΣ modulator.

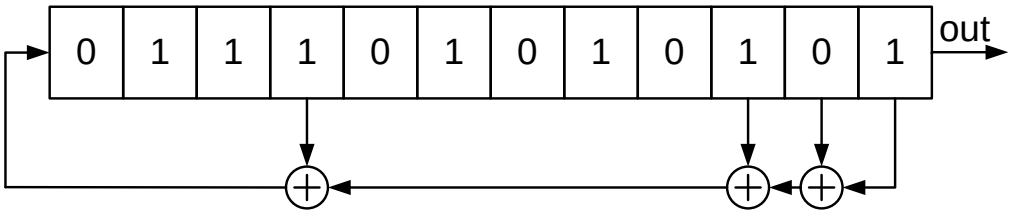

Figure 2-23 Block diagram of pseudo random number generator.

The pseudo random number generator is realized by linear feedback shift register (LFSR) [32]. An LFSR is a shift register whose input bit is a linear function of its previous state, and with a well-chosen feedback function the LFSR can produce a sequence of bits which appears random and has a very long cycle. The LFSR is implemented using 12-bit register with feedback to its input and the algorithm is shown in Figure 2-23. The feedback is formed by XORing the outputs of selected

stages of the shift register and then applying to the first stage. Each stage has a common clock.

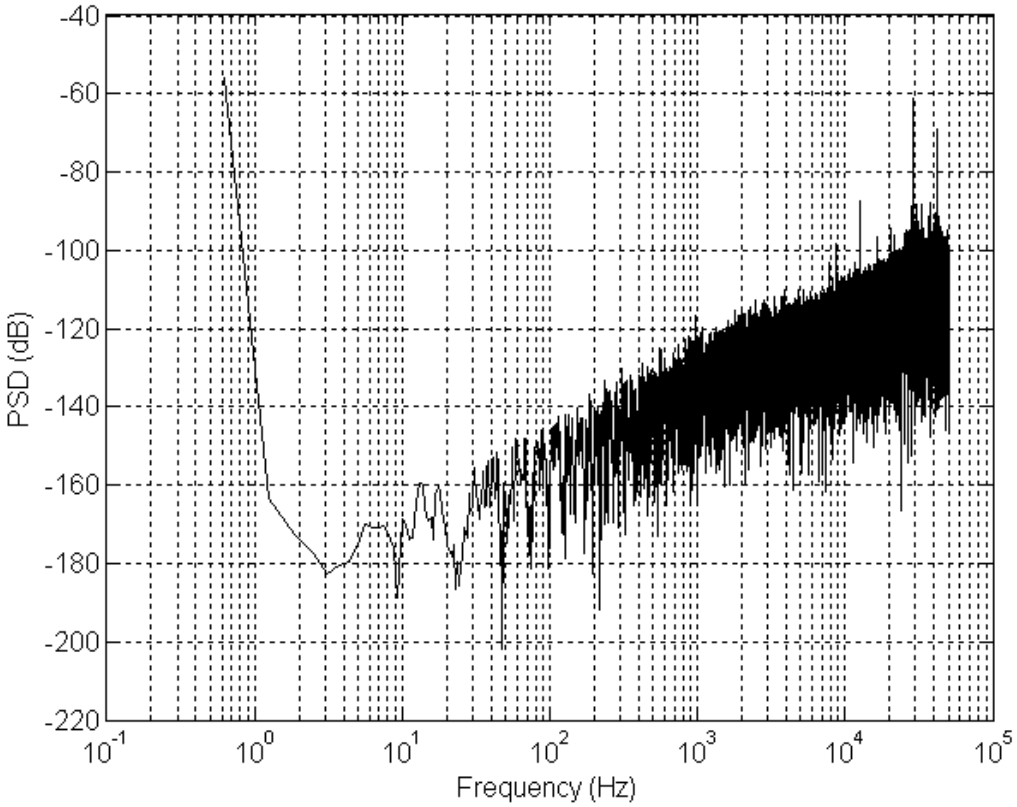

Figure 2-24 FFT of 12-bit 2nd order digital ΔΣ modulator with random signal generator.

The pseudo random number generator in the digital ΔΣ modulator introduces random noise to the output of the digital ΔΣ modulator. With the same constant input, the output of the digital ΔΣ modulator is analyzed. The FFT result exhibits clear noise shaping, and the idle tones at low frequency disappear as shown in Figure 2-24. The idle tones at high frequency can be further filtered by the following digital integrator.

2.2.6 Up/Down Counter

The 12-bit up/down counter acts as an integrator in FLL, whose output drives the 12-bit DCO. The bitstream from the digital ΔΣ modulator is substracted from the

output of the PDΔΣM and the result is applied to the digital integrator. Each bitstream toggles between 0 and 1, and thus the result is a three-level signal which is 0 when two bitstreams are equal and ±1 when they are different. The subtraction is implemented by an XOR gate and the digital integration is by means of a 12-bit up/down counter. The output of XOR gate is used as EN signal. When two bitstream equals to each other, the XOR gate disables the up/down counter. Otherwise, depending on the PDΔΣM's bitstream, noted as U/$\overline{D}$ signal, the counter increases or decreases accordingly. The block diagram of the up/down counter is shown is Figure 2-25.

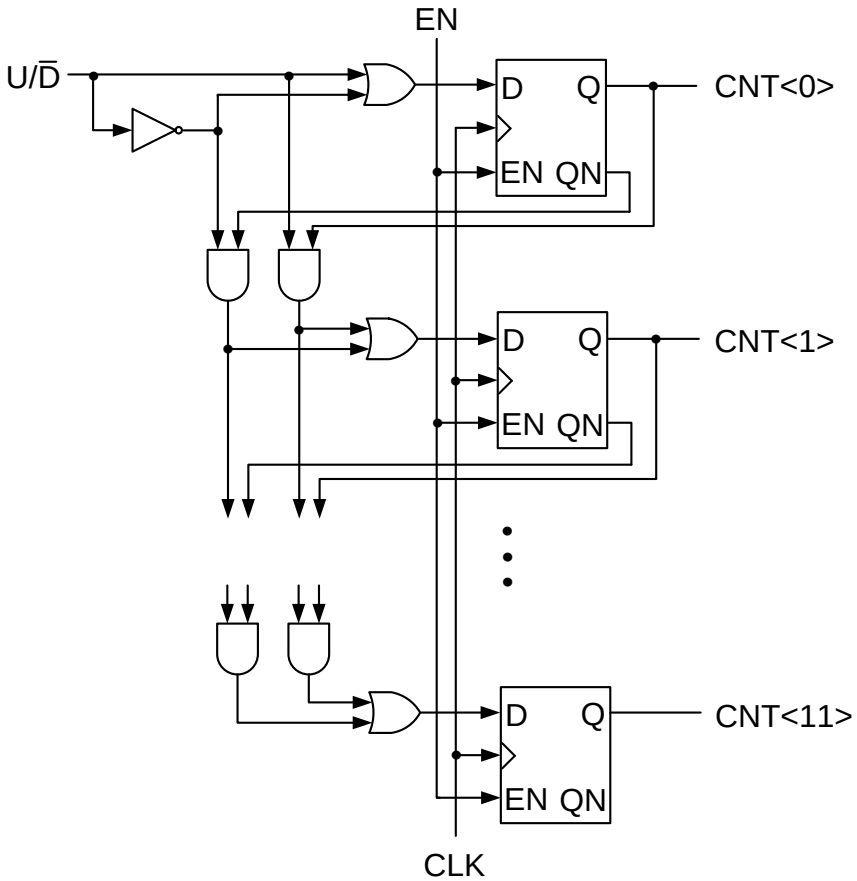

Figure 2-25 Block diagram of 4-bit up/down counter.

3.2.7 Digital Frequency Divider

Digital frequency divider is adopted to obtain various frequency outputs [33]. In FLL, the input of RC phase shifter and the clocks of the digital ΔΣ modulator, the up/down counter and the PDΔΣM are generated by frequency divider. The frequency divider is realized through a counter. The output of the frequency divider toggles between 0 and 1 based on the state of the counter.

2.3 Measurement

2.3.1 High temperature measurement setup

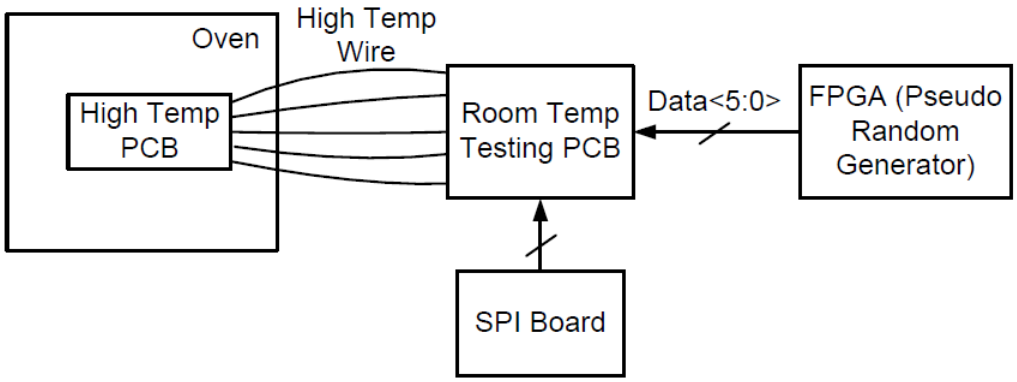

Figure 2-26 High temperature measurement setup.

High temperature measurement is conducted to test the frequency inaccuracy of the crystal-less temperature-independent frequency reference. Such high temperature testing poses several problems. Special high temperature PCB is used for the chip bonding. However, no commercially available components can support such high temperature. Therefore, a room temperature testing PCB is fabricated, and high temperature wires are used to connect the high temperature PCB and normal room temperature testing PCB. The long high temperature wires introduce large parasitic inductance. Without any decoupling capacitors near the

chips, the power supply for the chips is quite noisy which would affect the performance. Figure 2-26 shows the high temperature measurement setup. The high temperature PCB is put into the oven while the room temperature testing PCB is placed outside. These two PCBs are connected using high temperature wires. FPGA board includes the code of pseudo random generator which provides the input data for the acoustic transmitter. SPI board is used to generate the signals needed in SPI block of the chip to modify the configurations.

2.3.2 Measurement Results

The reconfigurable acoustic transmitter fabricated in 1μm SOI CMOS process has a die size of 25mm^2, 60% of which is occupied by crystal-less temperature-independent frequency reference, as shown in Figure 2-27. SOI technology is adopted to facilitate the targeted high temperature. The chip consumes 9mW and 18mW at 25°C and 225°C respectively, under 5V supply.

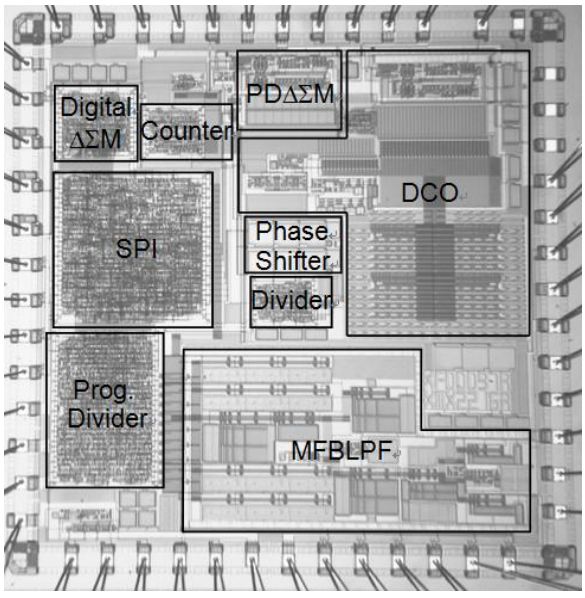

Figure 2-27 Die photo of acoustic telemetry transmitter which employs FLL with RC phase shifter.

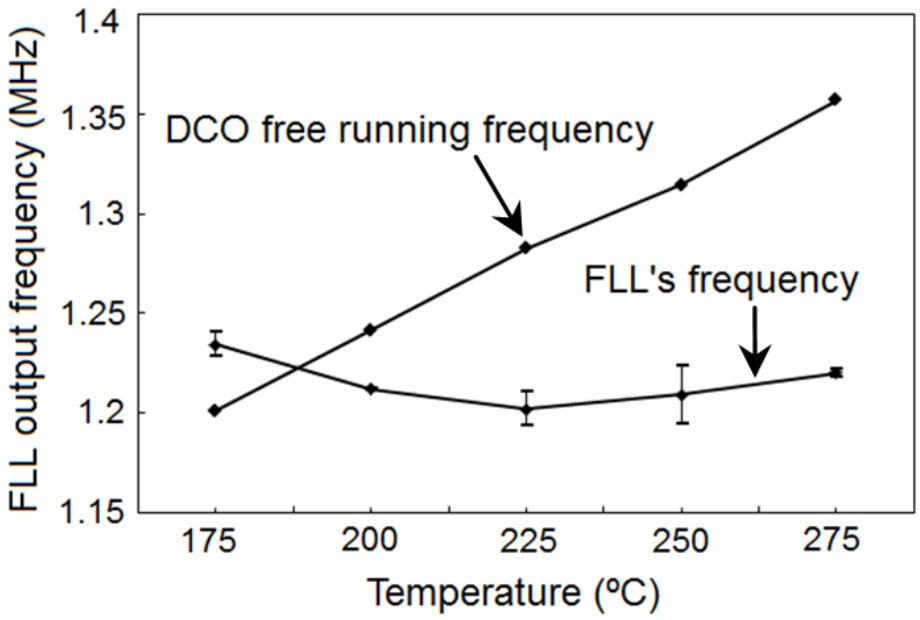

Figure 2-28 Measured frequency stability of FLL with RC phase shifter.

Figure 2-28 shows the measured frequency stability over temperature range of 175°C to 275°C. The measured frequency inaccuracy is ±1.94%, which is sufficient for the targeted application. For comparison, the measured free running frequency of the DCO without temperature compensation varies by ±6.11% over the same temperature range. We also compare our achieved performance with others in Table 2-1. As shown, ours is the only reported frequency reference with comparable stability performance operates beyond 125°C due to the SOI CMOS technology and digital intensive architecture. Although the accuracy is poorer than [21], we provide fully integrated solution by eliminating ETF, TS, external FPGA and polynomial coefficients extraction and mapping. It should be pointed out that ETF alone without any polynomial coefficients extraction and mapping will result in ±49% frequency variation due to the temperature dependency of ETF's phase delay ($\propto T^{-1.8}$) and would not be suitable for our targeted application.

Table 2-1 PERFORMANCE COMPARISON OF CRYSTAL-LESS TEMPERATURE-INDEPENDENT FREQUENCY REFERENCE

Reference	[9]	[16]	[17]	[21]	This work
Technology	0.25um	65nm	0.25um	0.7um	1um SOI
Supply (V)	3.3	1.2	2.5	5	5
Power (mW)	59.4	0.066	1.5	7.8	9/25°C 18/225°C
Area (mm^2)	NA	0.03	1.6	6.751+	25*
Reference Frequency (MHz)	25	6	7.03	1.6	1.22
Temp. Range (°C)	-10~80	0~120	-40~125	-55~125	175~275
Frequency Inaccuracy	±1.4%	±0.9%	±1.84%	±0.1%	±1.94%

+All digital circuits are realized in off-chip FPGA.

*Besides temperature compensated frequency reference, it includes full reconfigurable multi-channel OOK/chirp acoustic transmitter.

2.3.3 Discussion

From section 2.3.2, we noticed that the power at high temperature is twice of the power at room temperature. SOI CMOS technology is supposed to have a good leakage power performance at high temperature. During the simulation, the current only increases about 30% from 25℃ to 225℃. Therefore, it is difficult to identify the source where the additional current comes from. The leakage current from the pad is most suspicious reason but we cannot verify this through the measurement. In addition, there could be undesirable effect on the circuit performance due to the high power observed at high temperature.

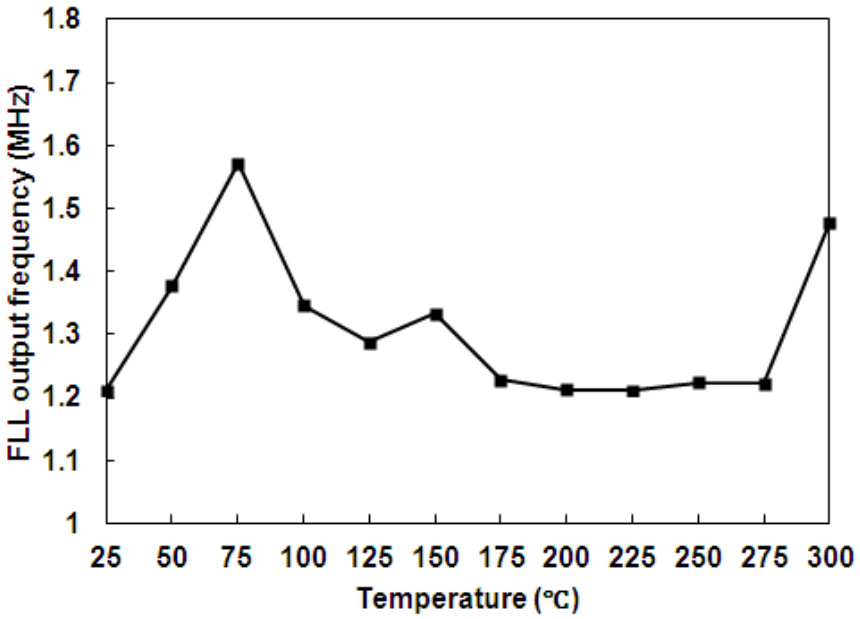

Figure 2-29 Measured frequency stability of FLL with RC phase shifter from 25°C to 300°C.

Another issue in the measurement results is that the measured frequency stability is not as good as expected. Figure 2-29 shows the measurement result within temperature range of 25℃ to 300℃. The reported temperature range is from 175℃ to 275℃, where the frequency inaccuracy can satisfy the acoustic telemetry transmission requirement. All digital blocks, such as 2nd order digital ΔΣM, U/D counter and frequency divider, within the FLL are unlikely to cause such impact as the malfunction of digital block will cause the FLL fail to acquire lock. Analog blocks are more sensitive to temperature variation. The non-linear relationship between the input frequency and the output phase in the RC phase shifter and the complicated architecture in PDΔΣM may contribute to such poor performance. The corner simulations of analog blocks, such as the RC phase shifter and the PDΔΣM, have indicated temperature variations smaller than what we measured. Moreover, another plausible reason that causes such discrepancies between the simulation and measurement could be the inaccuracy in the device model which

results in poor resistor TC compensation. Unfortunately, due to the limitation of chip area and IO pin, we do not incorporate test and characterization circuit for the RC phase shifter. In the second tapeout, some measures are included to minimize the impact of model inaccuracy.

Finally, the test setup is hardly ideal for the measurement. Although the device under test is housed in high temperature PCB to facilitate oven testing, the control and supply connections are done through long high temperature wires. Hence, the supply to the chip is far from ideal which might exhibit significant impedance at the supply and ground node. Unfortunately, due to the lack of high temperature passive resistor and capacitor components, we cannot build a complete high temperature PCB for the testing. Nevertheless, the obtained result is still sufficed for the intended applications.

Chapter 3 Crystal-Less Temperature-Independent Frequency Reference Based on Frequency-to-Voltage Converter

3.1 System Architecture

3.1.1 Operation Principle

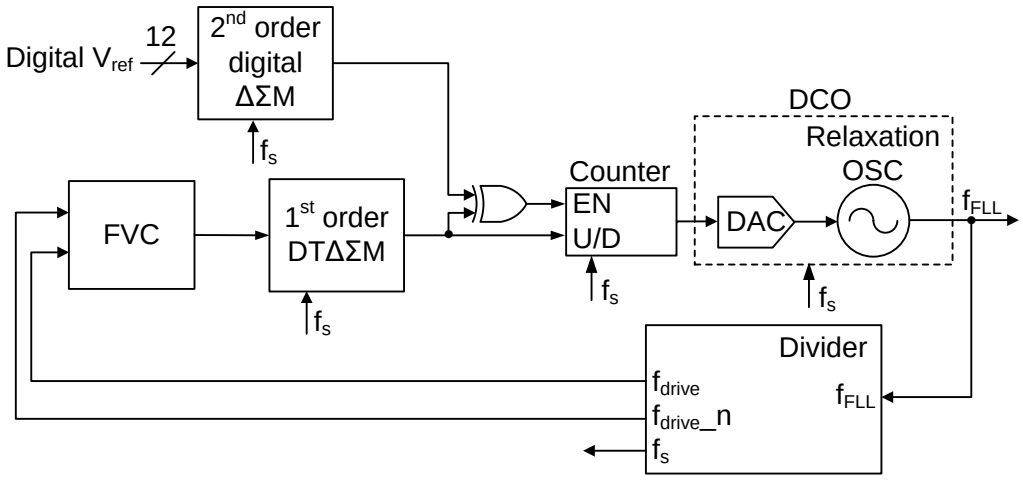

Figure 3-1 Proposed frequency reference based on frequency to voltage converter.

A new approach to realize temperature-independent frequency reference is introduced here, as shown in Figure 3-1. In the previous chapter, FLL employing an RC phase shifter and a PDΔΣM is discussed. The RC phase shifter basically translates the frequency information into a phase domain signal which is then converted to a bit stream by the PDΔΣM for the FLL's comparison.

Although we did not have sufficient information to isolate the reason for the discrepancies between measurement and simulation in the last tapeout, we did isolate a few critical blocks that could be further improved. Firstly, the RC phase shifter is not entirely linear. This might result in varying loop characteristic depending on the region of the RC phase shifter is working on. Secondly, the use

of PDΔΣM requires high output resistance. Due to the lack of accurate model at high temperature up to 300 ℃, it is difficult to foresee whether such complicated PDΔΣM will function properly at such high temperature. Hence, it is of our interest to propose an alternative FLL architecture that eliminates the use of these two blocks.

The operation principle of the new FLL is described as follows. The DCO output will be first divided down to ease the design of subsequent blocks. Following that, a temperature-independent frequency-to-voltage converter (FVC) is employed to generate an accurate voltage representation of the frequency [35]. This implies that the voltage versus frequency characteristic of FVC will not change much over the desired temperature range. The FVC output will then be converted to digital bitstream through a 1^{st} order discrete time ΔΣ modulator (DTΔΣM). Meanwhile, a digital reference input (V_{ref}) is converted to a digital bit stream through a 2^{nd} order digital ΔΣM. These two bit streams are then compared through an XOR gate to capture any frequency error. Its high frequency component is then filtered by a digital up/down counter before sending to DCO. Since both the digital representations of input reference frequency (V_{ref}) and the FVC's characteristic are temperature-independent, any DCO frequency deviation arises due to temperature variation will be captured by the FVC. The resulting negative feedback action of FLL will then eliminate this variation and give rise to a temperature-independent frequency reference (f_{FLL}).

3.1.2 Matlab Model

A Matlab model of proposed new frequency reference is studied first, as shown in Figure 3-2. The nominal frequency of VCO is set to be 3.3MHz and the input sensitivity is 800Hz/bit. The reason we increased the frequency of FLL compared to the previous work is that it can help improve the phase noise of the acoustic carriers as the divider ratio is larger. However, it also requires more bit width for the programmable divider. Considering the tradeoff between better phase noise and large programmable divider, 3.3MHz is selected.

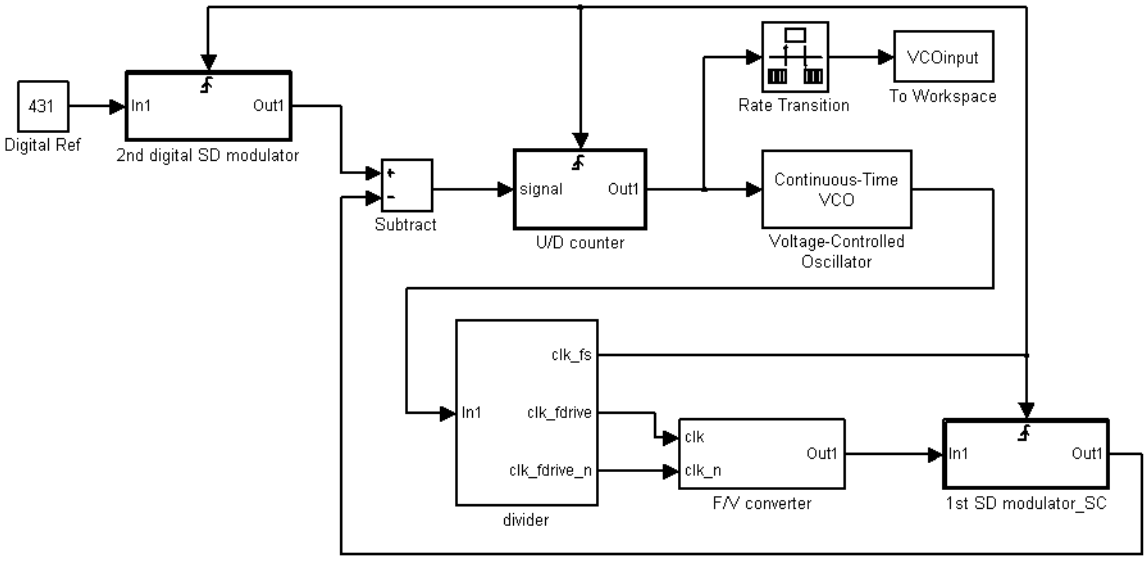

Figure 3-2 Matlab model of proposed frequency reference.

The new blocks are FVC and 1st order DTΔΣM, compared with the previous design. All the remaining blocks from previous Simulink model are reused, except for F/V converter and 1st SD modulator_SC. Figure 3-3 and Figure 3-4 show the block diagram of F/V converter and 1st SD modulator_SC, and the operation principle will be explained in section 3.2 and 3.3, respectively. F/V converter is assumed to be temperature-independent. Suppose the actual operating frequency of VCO drifts to different values due to the temperature variation. The

FLL still can tune the VCO's frequency back to 3.3MHz with a proper fixed V_{ref}. The following figures show the simulation results with the actual free-running frequency of VCO set to be 3.314MHz and 3.284MHz, respectively. As shown in Figure 3-5 (a), the average value of VCO input settles to -18.62, which adjusts the VCO to operate at the frequency of 3.3MHz. While in Figure 3-5 (b), the average value of VCO input becomes stable at 19.31 with the resulting frequency of 3.3MHz.

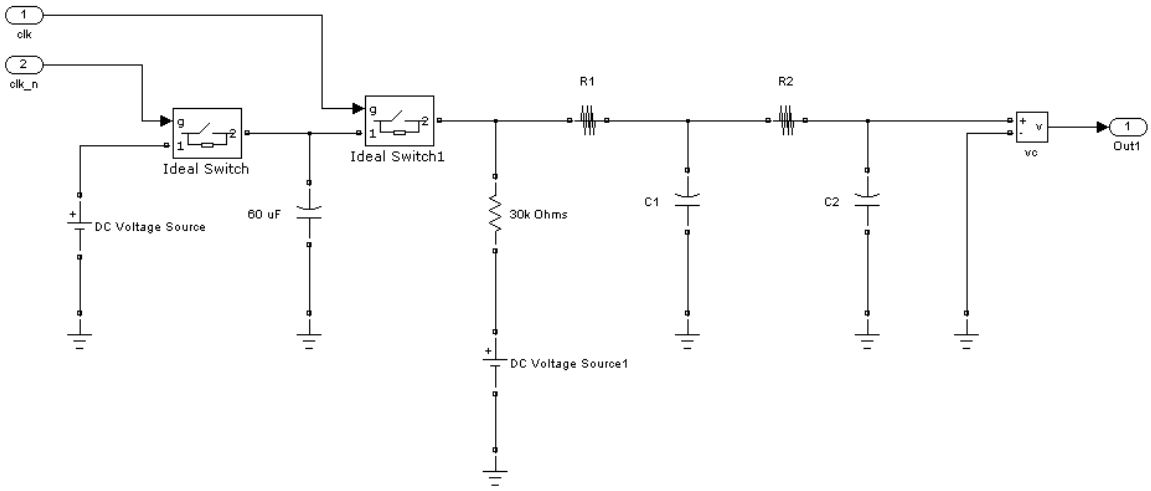

Figure 3-3 Block diagram of FVC.

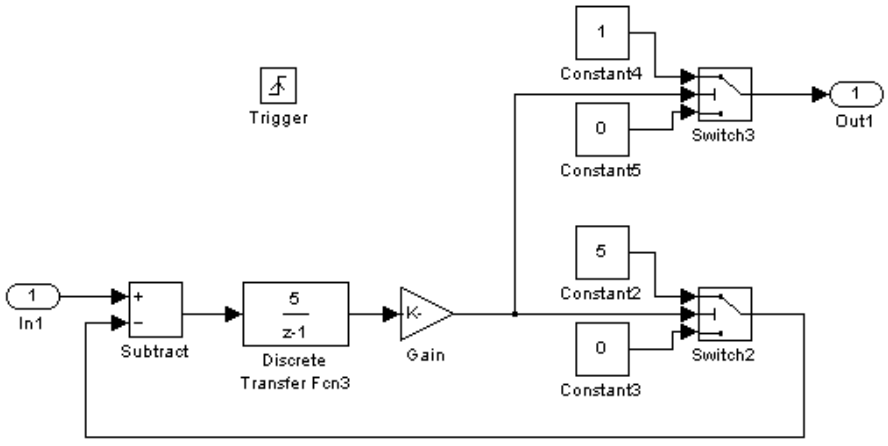

Figure 3-4 Block diagram of 1st SD modulator_SC.

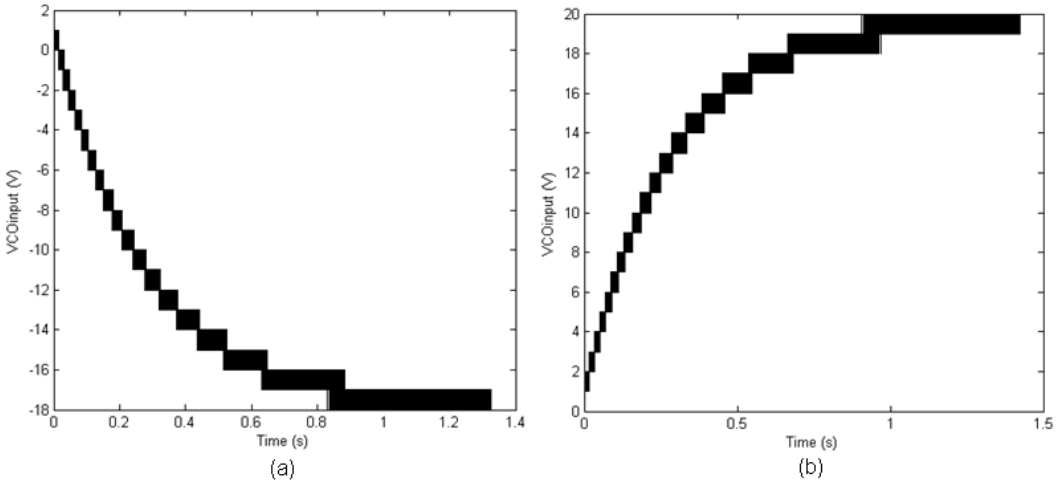

Figure 3-5 Simulation results of VCO initial frequency of (a) 3.314MHz and (b) 3.284MHz.

3.2 Frequency-to-Voltage Converter

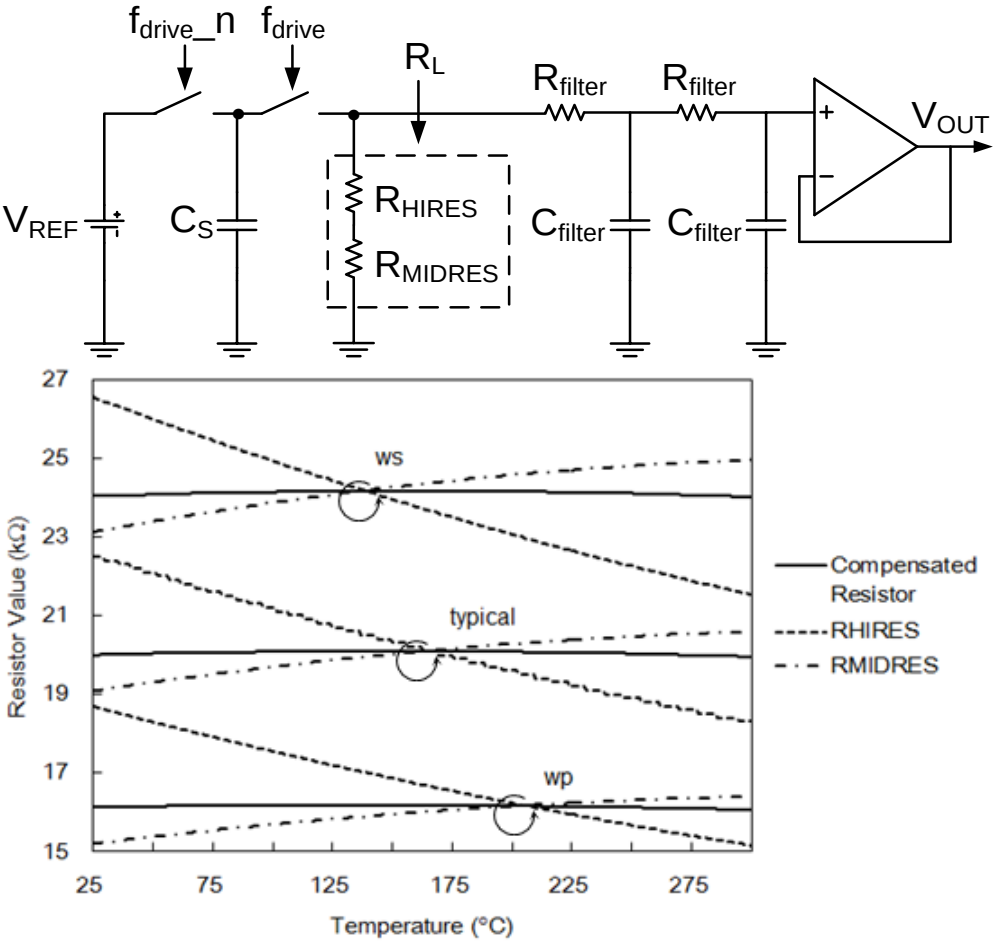

Figure 3-6 Block diagram of FVC with resistor TC compensation technique.

A differential switched capacitor based FVC is adopted in this design. For simplicity, only single ended version is shown in Figure 3-6. A switched capacitor has an equivalent resistance of $R_S=1/(f_{drive}C_S)$. Hence, the circuit represents a simple resistor divider consists of R_S and R_L. If $R_L << R_S$ is chosen, the average output voltage can be expressed as [35]:

$$V_{OUT} = V_{REF}\frac{R_L}{R_S} = V_{REF}R_L C_S f_{drive} \quad (3.1)$$

Hence, V_{OUT} will be a direct representation of f_{drive}.

If R_L and C_S are chosen to be temperature-independent, the FVC will exhibit a temperature-independent characteristic. In the proposed design, two resistors (RHIRES and RMIDRES) with opposite TCs are employed to form the R_L whereas poly-p+-diffusion capacitor with low TC is chosen for C_S. The ratio of two resistors is carefully selected to match the ratio of the TCs. The details about the resistor TC compensation technique has been discussed in section 2.2.2. The output has high frequency component (f_{drive}), and two RC filters are cascaded to extract the average voltage and suppress this high frequency component. A unity gain buffer is inserted between FVC and 1st order DTΔΣM to avoid the loading effect.

3.3 1st order Discrete Time ΔΣ Modulator

3.3.1 Operation Principle

In Figure 3-7, the 1st order DTΔΣM is used to digitize the FVC's output. Switched capacitor filter is employed as its filter coefficients can be accurately determined and is temperature-independent. A closed examination of FVC output

reveals that it consists of the desired signal around DC and high frequency components at f_{drive} as shown in Figure 3-8. Nyquist theorem requires the sampling clock (f_s) to be at least twice larger than the signal frequency of FVC. Due to the oversampling requirement of ΔΣM, it will limit the choice of f_{drive} used in FVC to a very small value as shown in Figure 3-8 (a) and (b). This will limit the suppression of f_{drive} component and require very large resistor and capacitor for the RC filters. As f_{drive} component is narrow band, subsampling concept is adopted here to push f_{drive} to higher value as shown in Figure 3-8 (c) and (d). Here, $f_{drive}=5/4f_s$ is chosen without any aliasing. The high f_{drive} will ease the design of RC filter and result in higher f_{drive} component suppression as shown.

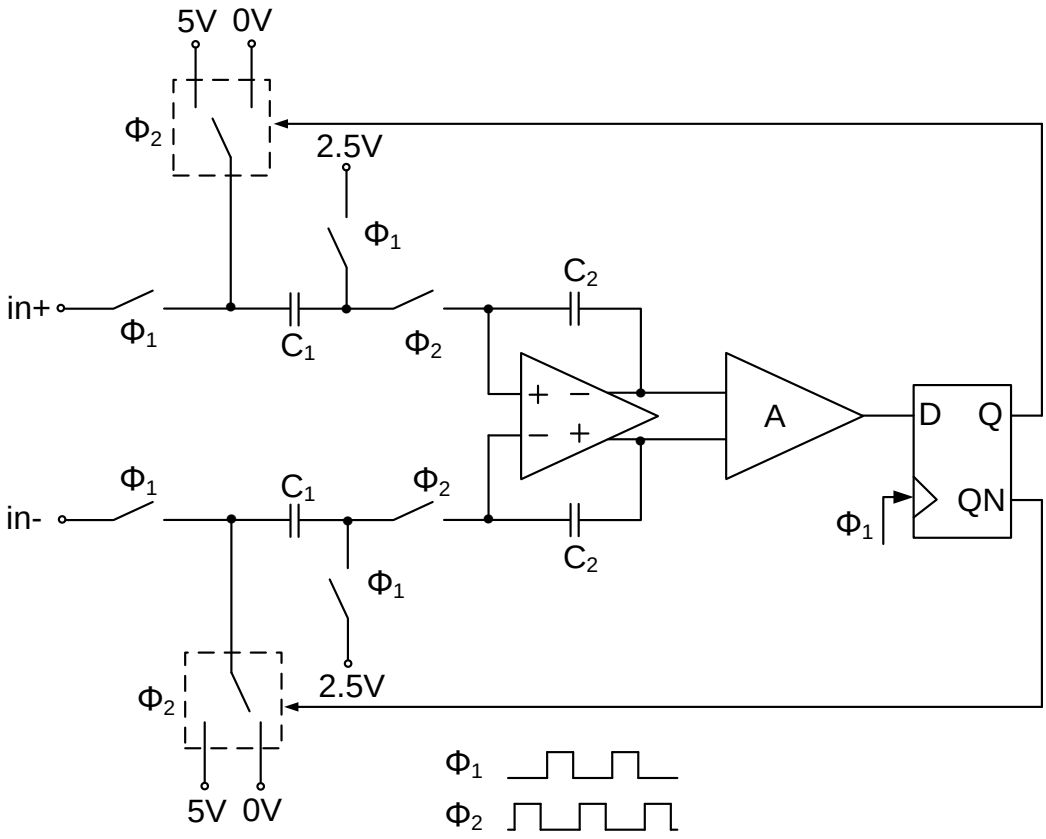

Figure 3-7 Block diagram of 1st order discrete time sigma delta modulator.

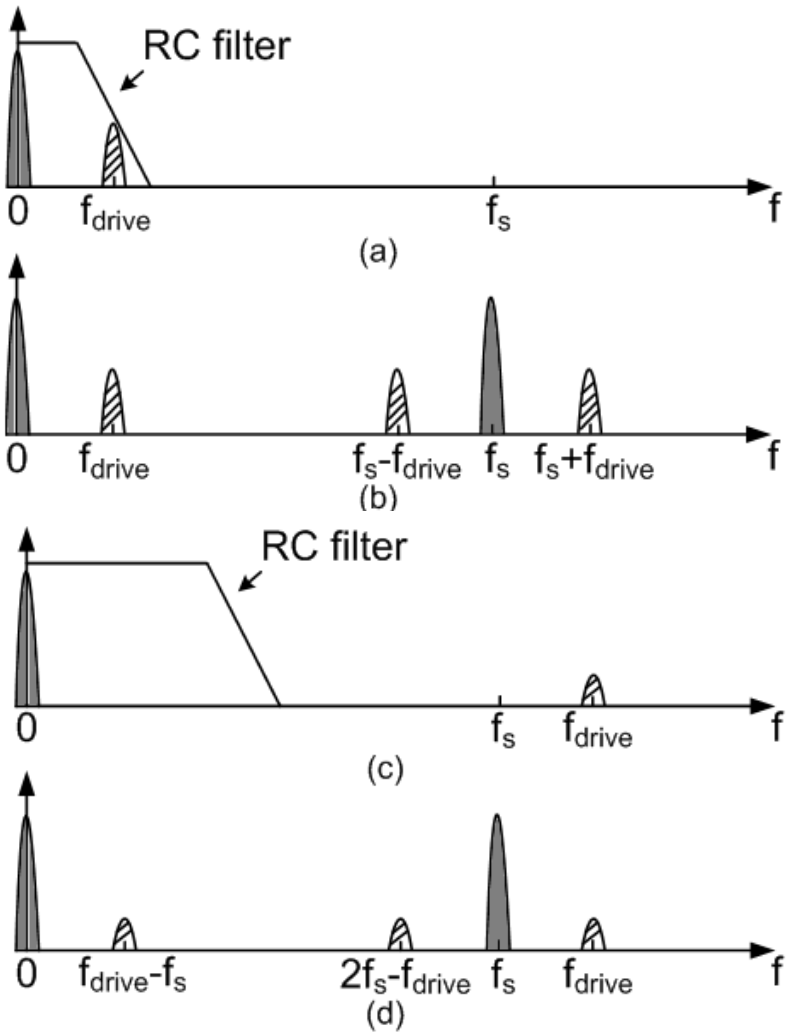

Figure 3-8 Comparison of oversampling and subsampling: oversampling (a) before sampling, (b) after sampling, subsampling (c) before sampling, (d) after sampling.

3.3.2 Implementation

Charge injection is one of the major error sources in switched capacitor circuits, which introduces an offset to the sampled output voltage [36]. In our circuit, the switch is implemented as a transmission gate. Charge injection effect can be reduced as the positive charges and the negative charges can neutralize with each other. But there are still some charges which will inject to the output node. Dummy transistors can be used to absorb the injected charges. However, the amount of the injected charges is difficult to estimate because it is determined by

many parameters such as process variation, threshold, voltage and clock transition time. Normally, the size of dummy transistor is designed as half of the switch under the assumption that the charges may evenly go to the source and the drain of the switch. The circuit of the switch used in this design is shown in Figure 3-9.

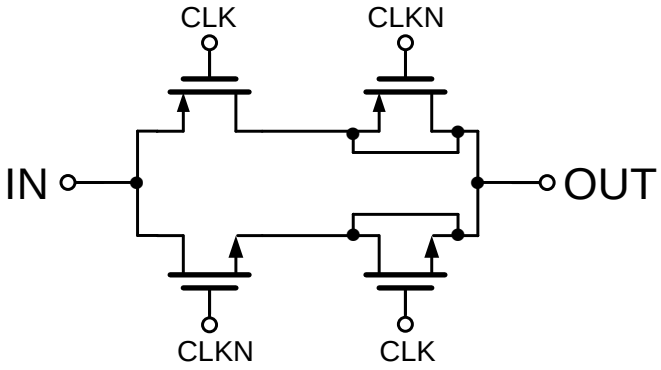

Figure 3-9 Block diagram of the switch with dummy transistor.

The effect of dummy transistor is simulated in Cadence schematic and the simulation results are demonstrated in Figure 3-10. An offset voltage can be observed after the switch is turned off. The solid line is the result with dummy transistor and the dotted line is the result without dummy transistor. From the comparison of the two lines, we can see that the charge injection is reduced but cannot be cancelled perfectly.

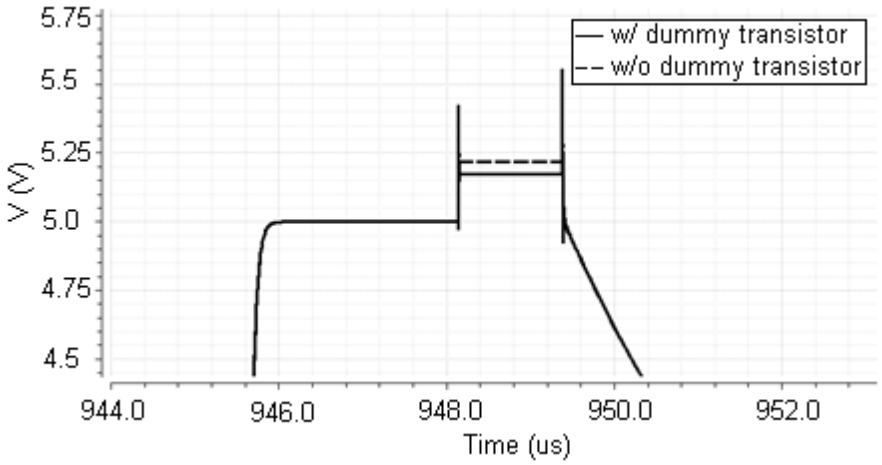

Figure 3-10 Simulation result of the switch W/O dummy transistor.

Bottom plate sampling technique is an effective method to reduce the charge injection effect [37]. The technique is shown in Figure 3-11, where two switches S1 and S2 are placed at the plates of the sampling capacitor. During the sampling phase, both S1 and S2 are turned on. However, at the transition time to hold phase, there is a delay between S1 and S2. S2 is switched off first. Then after a small delay, S1 is switched off. Since the bottom plate of the sampling capacitor is already disconnected from the ground, no more charge will inject to the sampling capacitor.

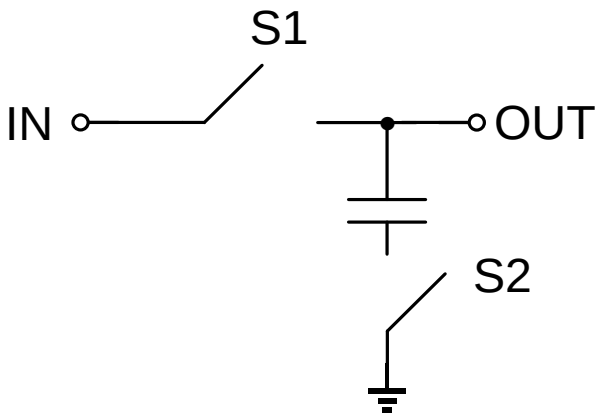

Figure 3-11 Bottom plate sampling technique.

Another error source in switched capacitor circuit is the clock feedthrough effect. As shown in Figure 3-12, the clock signal is coupled with the sampling capacitor though the gate-source capacitor. The clock feedthrough effect also introduces offset to the output voltage. Increasing the sampling capacitor can reduce the clock feedthrough effect. Besides, in order to minimize the clock feedthrough effect, the switch should use smaller size which results in smaller parasitic capacitor. However, the resistance of the switch will increase if smaller size is adopted. Therefore, there is a tradeoff when choosing the size of the switch.

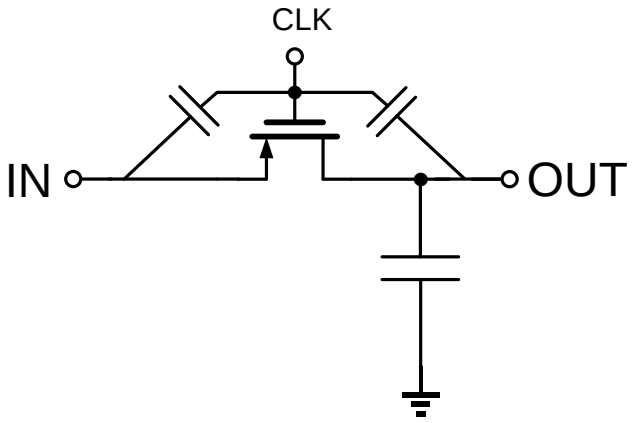

Figure 3-12 Clock feedthrough effect of the switch.

In the switched capacitor circuit, another concern is the clock scheme. For the circuit in Figure 3-7, if Φ_1 and Φ_2 are switched simultaneously, during the transient time, the input and output may be shorted, which can cause the error in charge redistribution between C_1 and C_2. To avoid such problem, a non-overlapping clock scheme is applied as shown in the bottom of Figure 3-7, which ensures that Φ_1 and Φ_2 will not be switched on at the same time. The realization of the non-overlapping clock scheme is easy in this work. The clock is generated by a digital divider from a frequency reference, and therefore it is very convenient to generate a clock with different phase. Figure 3-13 shows the simulation result of the non-overlapping clocks provided by the digital divider, together with the bottom plate sampling technique.

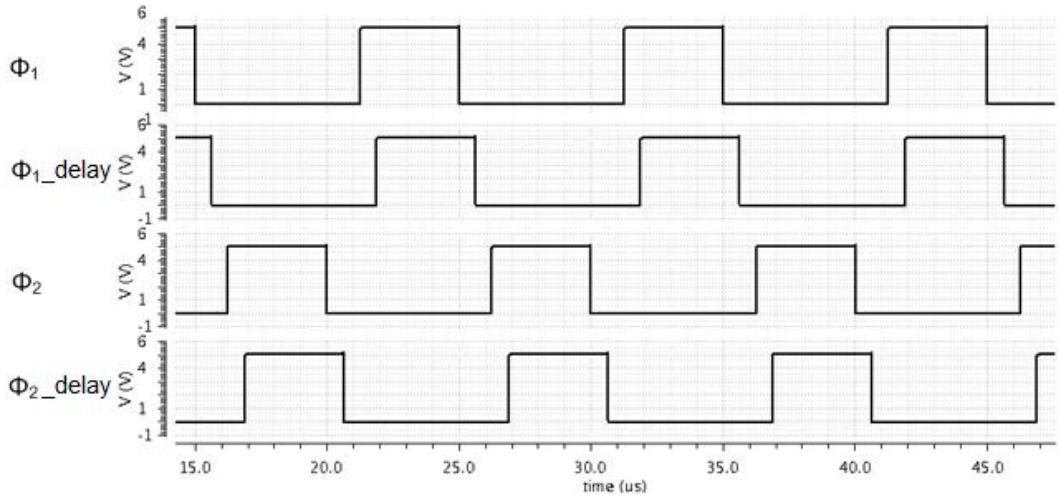

Figure 3-13 Simulation result of non-overlap clocks for 1st order DTΔΣM.

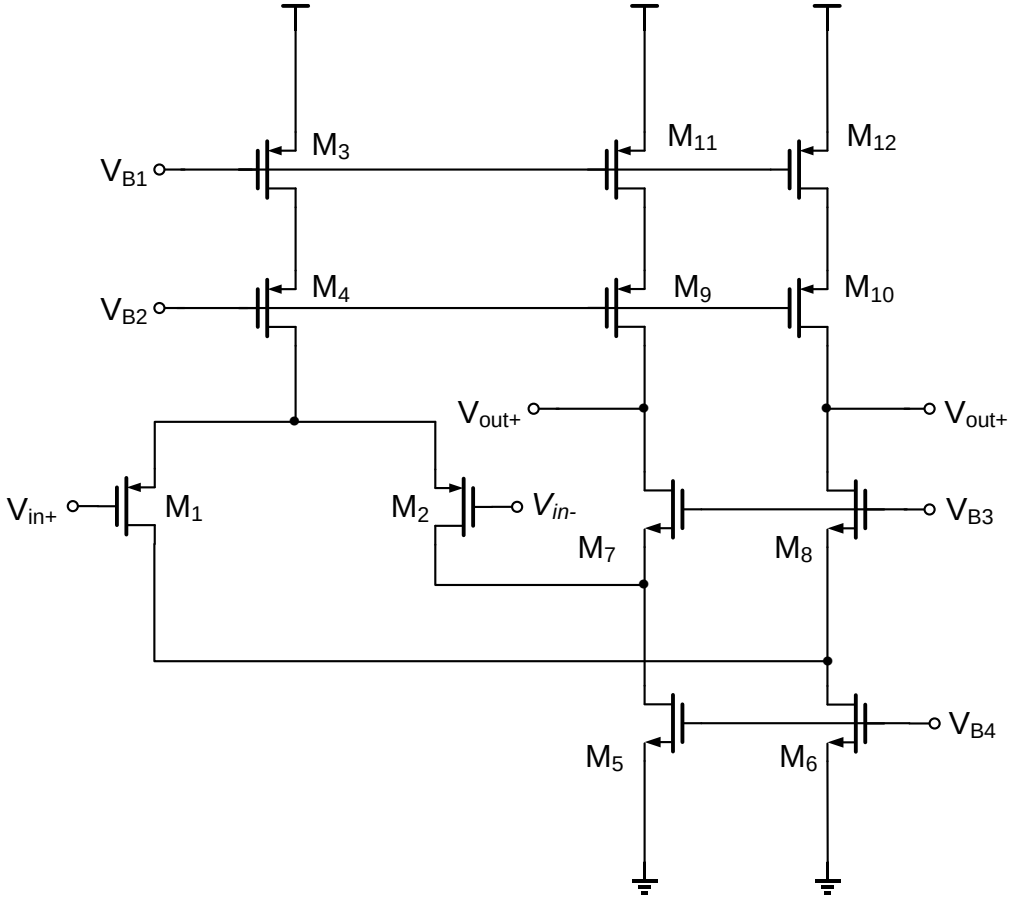

Figure 3-14 Circuit of folded cascode amplifier.

The amplifier used to build the switched capacitor integrator is realized in folded cascode architecture as shown in Figure 3-14. A typical folded cascode amplifier can provide high DC gain and bandwidth [38]. In this work, only 1st order

DTΔΣM is implemented and the output of the switched capacitor integrator is directly fed to a comparator. Therefore, the output swing is not an issue in this work. In order to guarantee the achieved output swing, the resistor sensing common mode feedback (CMFB) circuit is adopted as shown in Figure 3-15. The resistance of R_1 and R_2 is required to be large enough in order not to affect the amplifier gain.

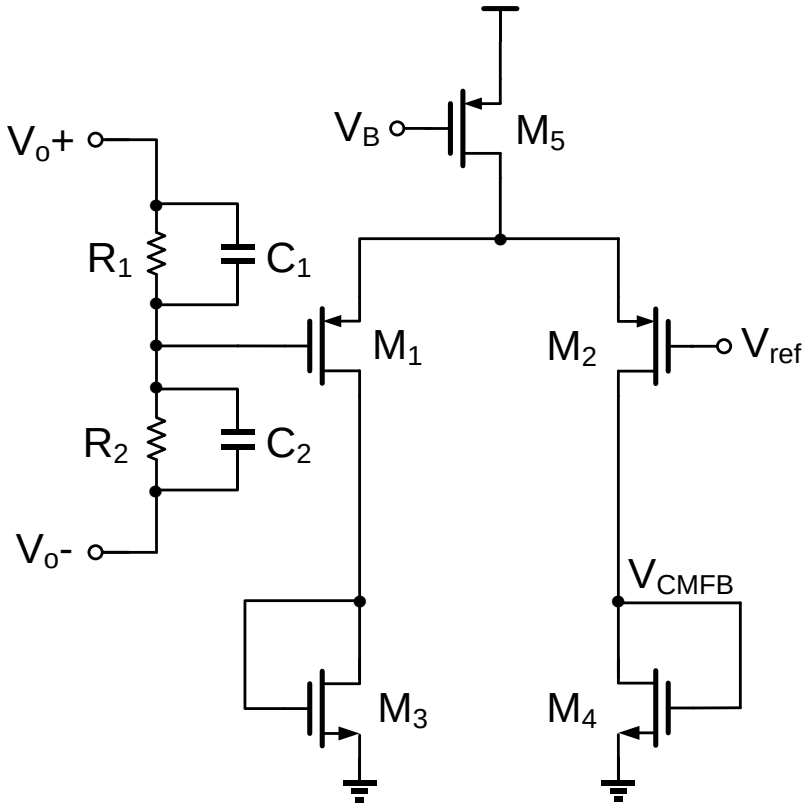

Figure 3-15 Resistor sensing CMFB circuit.

The CMFB loop is compensated by placing the capacitors C_1 and C_2 in parallel to the common mode voltage sensing resistor, which introduces phase lead and ensures the stability of the CMFB loop by adding a zero at $\omega=1/R_1C_1(R_2C_2)$. The phase margin is improved from -54 ° to 63 ° at 25 ℃ as shown in Figure 3-16. Simulations are also run at different temperatures. The compensated phase margin is 63 °and 62 °at 125 ℃ and 225 ℃, respectively.

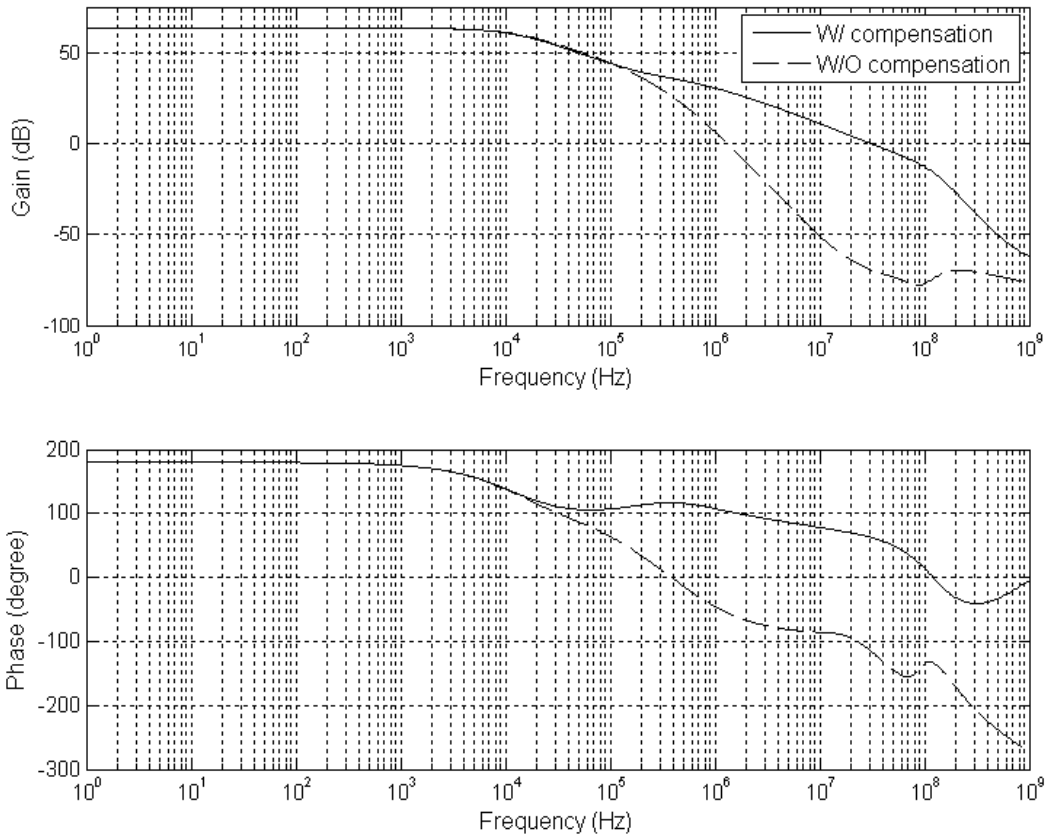

Figure 3-16 Simulation result of amplifier's CMFB phase margin compensation at 25°C.

The simulation of the folded cascade amplifier is shown in Figure 3-17. The achieved gain is 57dB, 56dB and 55dB at 25℃, 125℃ and 225℃, respectively. The phase margin is also measured, which is 81°, 81°and 81°at 25℃, 125℃ and 225℃, respectively.

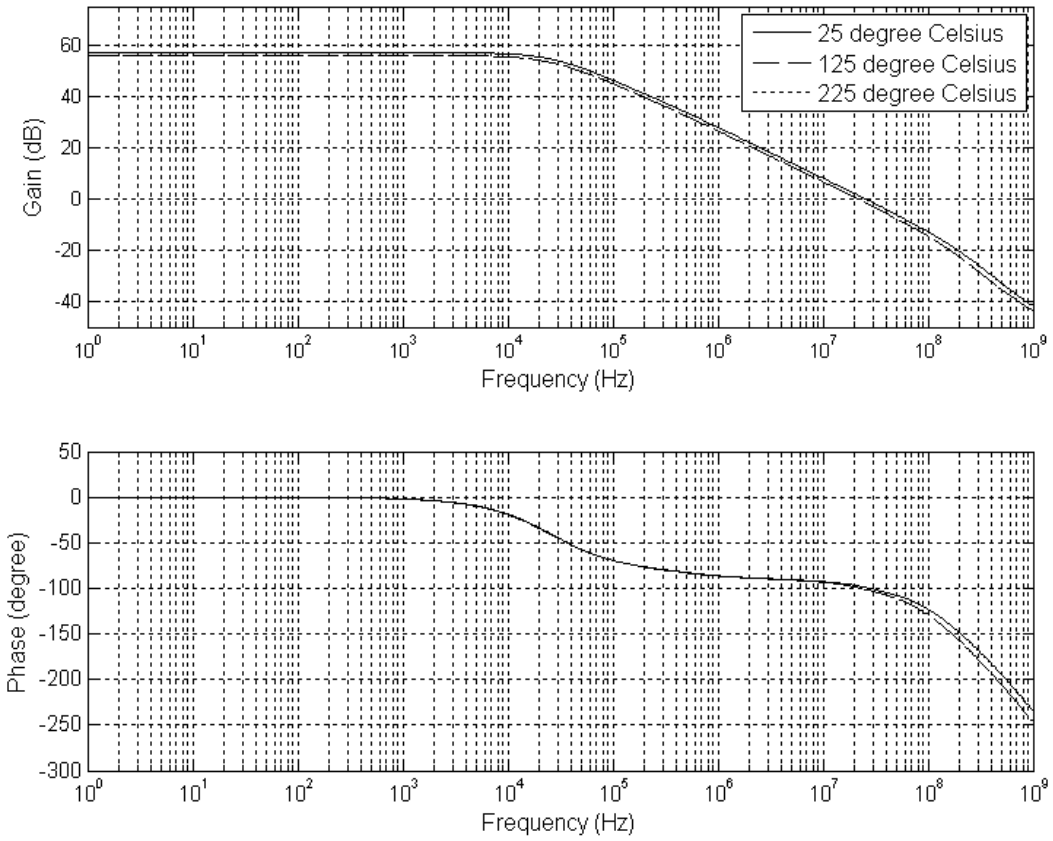

Figure 3-17 Simulation result of the folded cascade amplifier at 25°C, 125°C and 225°C, respectively.

The performance of 1st order DTΔΣM is verified by a sinusoid input with frequency of 59Hz and amplitude of 1V. The actual input of 1st order ΔΣM in this design is the output of FVC, which is a DC signal. Therefore, a low frequency input is chosen for simulation. A 32768-point FFT is presented here. Simulation results under different temperature are shown in Figure 3-18.

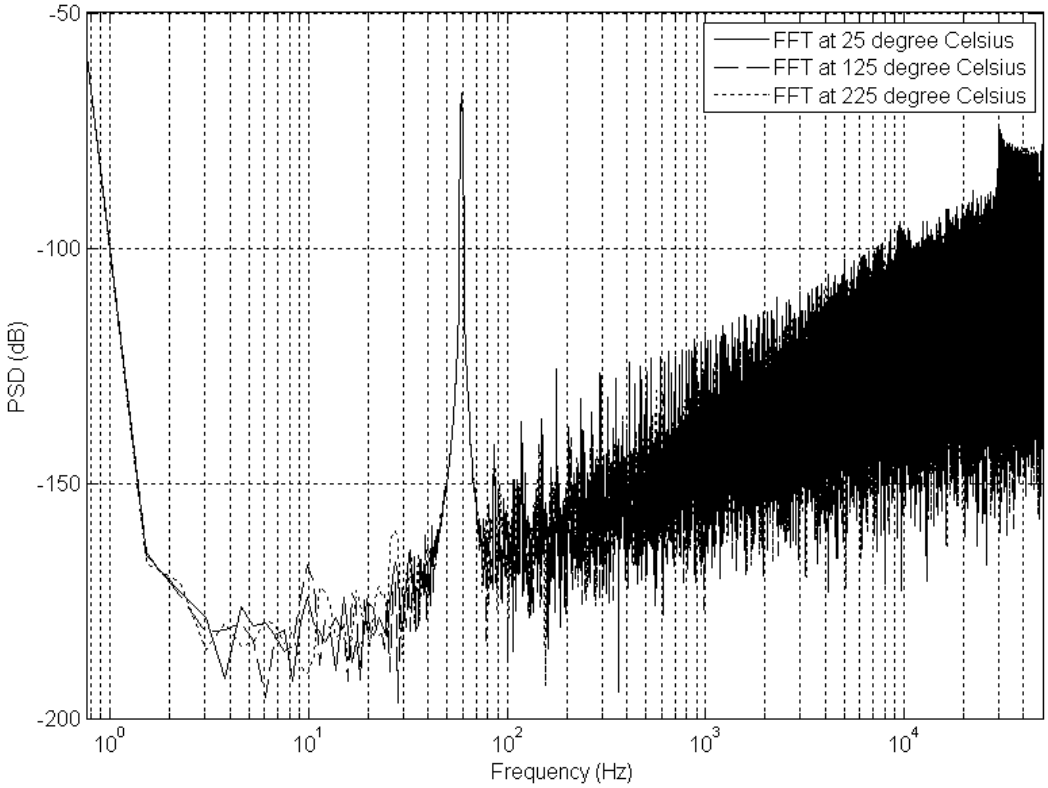

Figure 3-18 FFT of 1st order DTΔΣM at 25 ℃, 125 ℃ and 225 ℃, respectively.

3.4 Measurement

3.4.1 Measurement Results

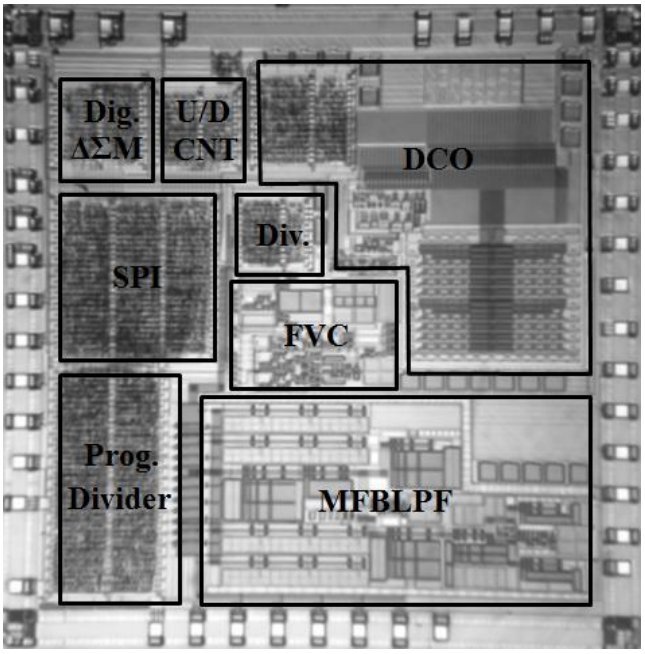

Figure 3-19 Die photo of acoustic telemetry transmitter which employs FLL with FVC.

The acoustic transmitter fabricated in 1μm SOI CMOS process has a die size of 25mm^2, with FLL occupying 60%, as shown in Figure 3-19. The chip consumes 11mW and 21mW at 25°C and 300°C respectively, under 5V supply.

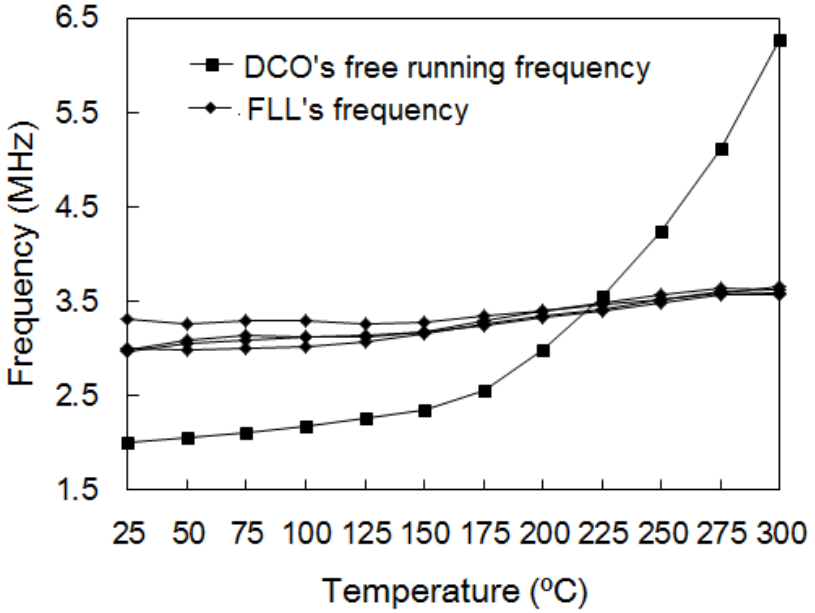

Figure 3-20 Measured frequency stability of FLL with FVC before trimming.

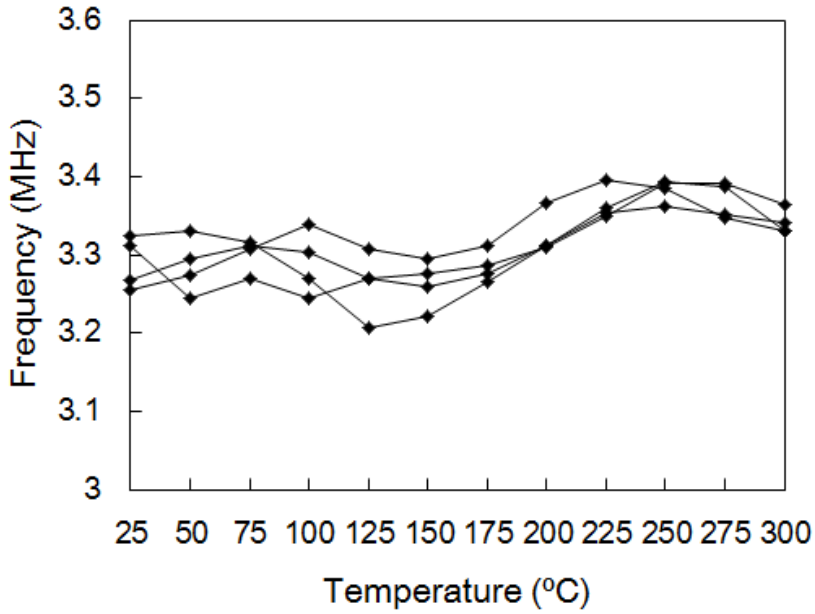

Figure 3-21 Measured frequency stability of FLL with FVC after trimming.

Figure 3-20 shows the measured frequency stability over temperature range of 25°C to 300°C. Without FLL, the free running DCO has frequency variation of

±51.5%. With FLL, the variation reduced to ±10.05%. We suspect the temperature dependent offset voltage of buffer between FVC and 1st order DTΔΣM is accountable for the degraded performance, as well as the inaccurate resistor TC compensation. Nevertheless, digital trimming can be easily applied once the FLL frequency versus temperature characteristic is known. As illustrated in Figure 3-21, by applying digital trimming to V_{REF} input, the temperature variation can be further improved down to ±2.85% which is sufficed for transmitter. Table 3-1 summarizes the performance comparison with other on-chip frequency references.

Table 3-1 PERFORMANCE COMPARISONS OF CRYSTAL-LESS TEMPERATURE-INDEPENDENT FREQUENCY REFERENCE

Reference	[9]	[16]	[17]	[21]	Chapter 2	This work
Technology	0.25um	65nm	0.25um	0.7um	1um SOI	1um SOI
Supply (V)	3.3	1.2	2.5	5	5	5
Power (mW)	59.4	0.066	1.5	7.8	9/25℃ 18/225℃	11/25°C 21/300°C
Area (mm^2)	NA	0.03	1.6	6.751+	25*	25*
Reference Frequency (MHz)	25	6	7.03	1.6	1.22	3.3
Temp. Range (°C)	-10~80	0~120	-40~125	-55~125	175~275	25~300
Frequency Inaccuracy	±1.4%	±0.9%	±1.84%	±0.1%	±1.94%	±2.85%

+All digital circuits are realized in off-chip FPGA.

*Besides temperature compensated frequency reference, it includes full reconfigurable multi-channel OOK/chirp TX and MFBLPF.

3.4.2 Discussion

From the Table 3-1, we can notice that FLL with FVC has improved frequency stability performance compared to FLL with RC phase shifter. One possible reason is that this method uses a more direct way to convert the frequency information into a voltage signal for the FLL loop's comparison. Also the relationship between the voltage and the frequency is linear. However, in RC phase shifter, the relationship between the phase delay and the input frequency is not linear. Moreover, the 1st order DTΔΣM is more robust for high temperature applications compared with the PDΔΣM, because the 1st order DTΔΣM mainly relies on the switched capacitor circuit.

Unfortunately the measured frequency stability before digital trimming is still quite large. As analyzed before, the resistor TC compensation technique is most suspicious reason. However, the design is highly digital intensive. Therefore, it is easy to apply digital trimming to it, and we can see that the frequency stability is significantly enhanced after digital trimming.

Chapter 4 Reconfigurable Multi-Channel Acoustic Telemetry Transmitter

4.1 Reconfigurable Modulation

4.1.1 On-Off Keying Modulation

On-off keying (OOK) modulation is the simplest form of amplitude-shift keying (ASK) modulation, where digital data is represented by the presence or absence of a carrier wave. Although complex modulation can help boost the data rate, considering the severe acoustic channel attenuation and the narrow passband frequency range, OOK modulation is adopted in our acoustic telemetry transmitter. With a well-defined channel characteristic, 6-channel OOK (OOK 1~6) modulated signal can be used to achieve higher data rate with the channel frequencies located at Band 2 (350Hz and 410Hz), Band 3 (620Hz and 680Hz), and Band 4 (920Hz and 960Hz), respectively. The architecture can be easily extended by using the band 5 (1170Hz to 1265Hz) but is not implemented in this work. It is not necessary as the achieved data rate without employing band 5 has well exceeded the conventional architecture. In addition, the last band also suffers from larger attenuation and smaller bandwidth. It should be noted that band below 300Hz is generally not used due to higher noise whereas band above 1.3kHz suffers higher loss and smaller bandwidth.

4.1.2 Chirp Modulation

The acoustic telemetry transmitter can also generate chirp modulated signal to provide flexible modulation based on channel characteristic. If the acoustic

channel has significant variations due to uncertainty in pipe length and section, we would not be able to place the wave energy in the "sweet spot" at the computed center of passband [6]. The 3-channel chirp (Chirp 1~3) can thus be used to spread the acoustic energy across the band, whose frequency ranges are 310~450Hz (Band 2), 600~700Hz (Band 3) and 890~980Hz (Band 4). The chirp modulation makes use of wider frequency range, and therefore it can ensure a more robust transmission.

4.2 Acoustic Telemetry Transmitter

4.2.1 Proposed Reconfigurable Acoustic Telemetry Transmitter

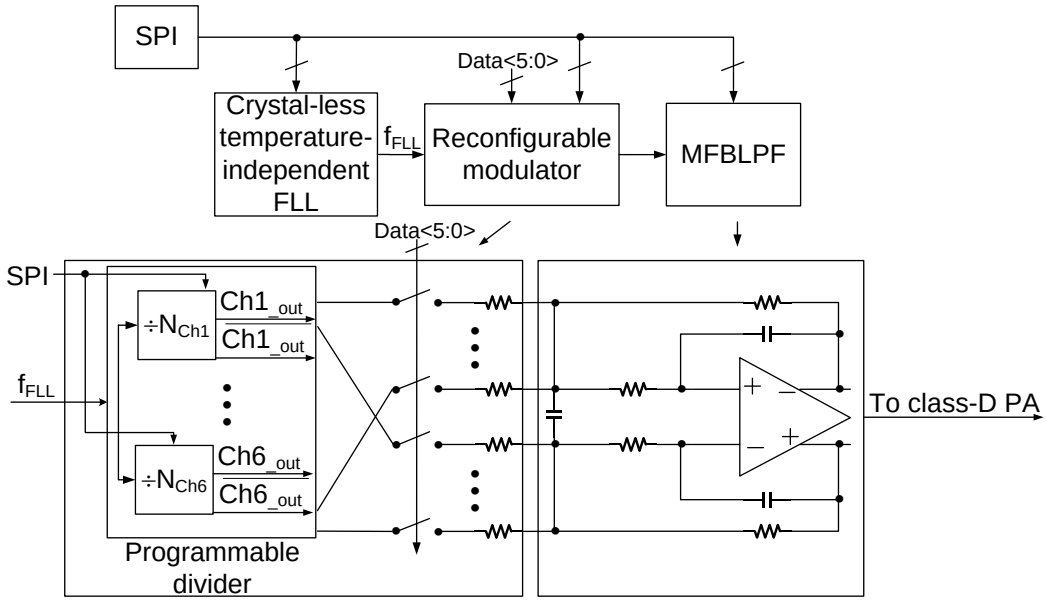

Figure 4-1 Proposed reconfigurable multi-channel acoustic telemetry transmitter.

The proposed architecture is shown in Figure 4-1, which consists of a crystal-less temperature-independent frequency reference, a reconfigurable modulator, a multiple feedback low-pass filter (MFBLPF) and a serial-to-peripheral interface (SPI). The frequency reference generates a stable frequency output over the

desired high temperature range. This output is then sent to a reconfigurable acoustic modulator. Based on the chosen modulation and incoming data, the modulator will produce either 6-channel OOK signals or 3-channel chirp signals centered at the allocated bands. The resulting signals are then combined through MFBLPF before sending to an off-chip class-D power amplifier (PA). The MFBLPF will help suppressing the unwanted harmonics and thus simplifying the frequency reference design.

Conventionally, multi-channel OOK and chirp are not used for modulation as they pose stringent requirement on the linearity of PA due to large amplitude variation. This often leads to highly inefficient PA. However, for wireless acoustic telemetry, due to its close proximity to audio range, highly efficient class-D PA can be employed, which makes multi-channel OOK and chirp a feasible choice for modulation [40, 41]. The class-D PA is beyond the scope of this work and would not be discussed in details.

As shown in Figure 4-1, six programmable dividers are employed to generate acoustic carriers with achieved output frequency resolution of <1Hz. The division ratio N_{Ch1}~N_{Ch6} can be tuned though SPI. With OOK, all six programmable dividers are utilized. N_{Ch1}~N_{Ch6} are initialized by SPI and fixed during the transmission to produce six frequency channels located within the acoustic passbands. With chirp, only three programmable dividers are used. N_{Ch1}~N_{Ch3} are employed, and their values are changed through SPI continuously across the symbol period to cover the whole acoustic passband.

4.2.2 Circuit Implementation

The signal f_{FLL} is divided by a programmable divider to generate different channel carriers. The ratios of the division can be set through SPI, which provides the flexibility of accommodating different acoustic channel characteristics. The acoustic channel exhibits comb shape and the bandwidth of each passband is narrow, thus the carriers need to be placed perfectly in the passband range. Otherwise, the carriers will be filtered by the nulls in the acoustic channels, which causes unsuccessful transmission. The OOK/chirp modulation is realized by controlling a switch with the input data.

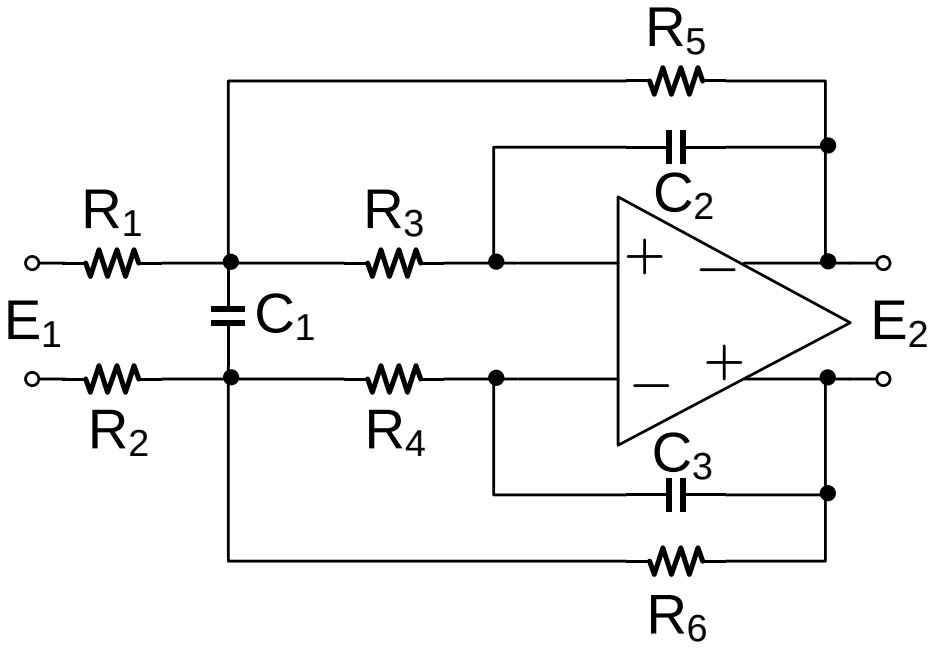

Figure 4-2 Basic architecture of MFBLPF.

The basic architecture of MFBLPF is shown in Figure 4-2 [42]. The transfer function can be expressed as

$$\frac{E_2}{E_1} = \frac{-1/R_1R_3}{2s^2C_1C_2+sC_2\left(\frac{1}{R_1}+\frac{1}{R_3}+\frac{1}{R_5}\right)+1/R_3R_5} \tag{4.1}$$

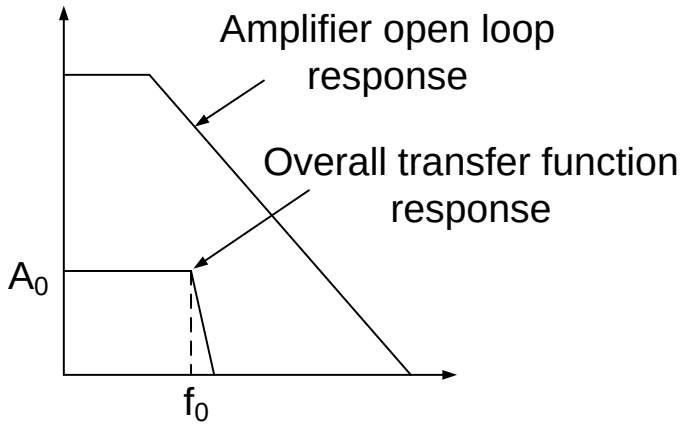

Figure 4-3 Frequency response of amplifier and MFBLPF.

The response is shown in Figure 4-3. If the following parameters are defined as

$$\mathrm{C} = \frac{k}{2\pi f_0} \tag{4.2}$$

$$\mathrm{H} = |A_0| \tag{4.3}$$

$\alpha = \sqrt{2}$ (for maximally flat response, 40dB/decade rolloff) (4.4)

Then the values of each component in MFBLPF are

$$C_1 = \frac{4}{\alpha^2}(H+1)\frac{k}{2\pi f_0} \tag{4.5}$$

$$C_2 = C_3 = C = \frac{k}{2\pi f_0} \tag{4.6}$$

$$R_1 = R_2 = \frac{\alpha}{2Hk} \tag{4.7}$$

$$R_3 = R_4 = \frac{\alpha}{2(H+1)k} \tag{4.8}$$

$$R_5 = R_6 = \frac{\alpha}{2k} = \mathrm{H}R_1 \tag{4.9}$$

The carrier's amplitude generated by the programmable divider is 5V. Therefore, before combining multiple channels together, the MFBLPF should reduce the input signal's amplitude. Considering total 6 channels for OOK modulation and the amplifier's output swing in the MFBLPF, the gain of the MFBLPF is selected

to be 0.1, which is realized by setting the ratio of R_1, R_3 and R_5 in MFBLPF. The MFBLPF also filters out the harmonics from each carrier frequency. Hence, the cutoff frequency of MFBLPF is set to be 1.3kHz. The resistor's value can change up to ±20% due to the process variation. If the cutoff frequency increases, the attenuation to the harmonics becomes smaller. If the cutoff frequency decreases, the transmission signal will be affected. Hence C_1 and C_2 are designed as a capacitor array, whose value can be set through SPI to adjust the cutoff frequency. The amplifier in the MFBLFP is implemented as a folded cascade amplifier. The combination of multi-channel carriers requires large output swing, which can maximize the power of each channel. Therefore, the CMFB circuit is realized by resistor sensing. The amplifier is realized using the same amplifier in 1st order DTΔΣM. The details of this amplifier have been discussed in chapter 3. The simulation of the MFBLPF and the amplifier under different temperatures are provided in Figure 4-4.

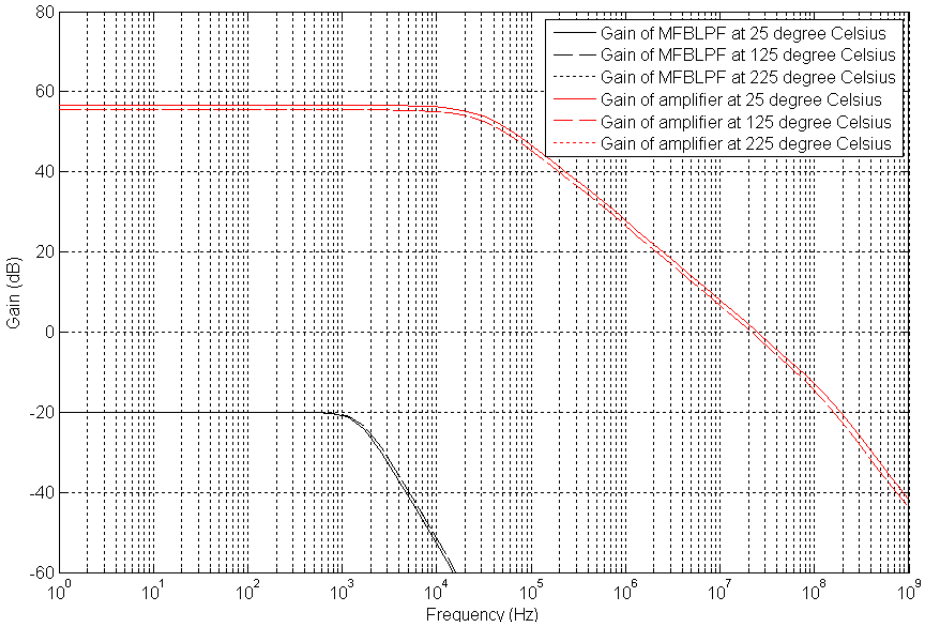

Figure 4-4 Simulation results of frequency response of amplifier and acoustic modulator at 25 ℃, 125 ℃ and 225 ℃, respectively.

Another MFBLPF is added after the acoustic modulator to provide further attenuation to the harmonics. This MFBLPF use the same architecture as discussed before except that the gain is set to 1. The simulation of this MFBLPF and the amplifier under different temperatures are shown in Figure 4-5.

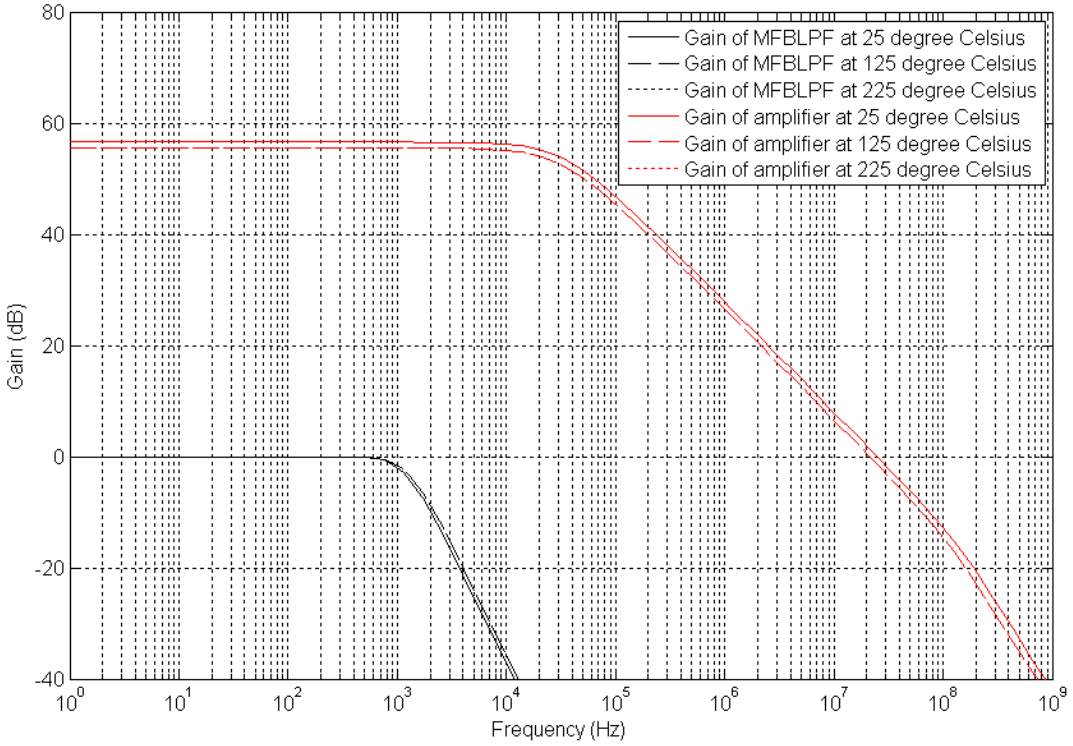

Figure 4-5 Simulation results of frequency response of amplifier and unity gain MFBLPF at 25 ℃, 125 ℃ and 225 ℃, respectively.

The SNR of acoustic transmitter is then studied. The acoustic carriers generated by the programmable divider go through the acoustic modulator. The amplitude of each acoustic carrier is 0.5V and hence the RMS power is $0.125V^2$. The noise generated by the acoustic modulator is simulated in Cadence. The frequency range of interest is from DC to 1kHz and the total noise power is 4.1e-10 V^2. Therefore, the transmitter's SNR is 85dB, which far exceeds the requirement of 20dB as discussed in section 1.3.

4.3 Measurement

4.3.1 Configuration and Demodulation

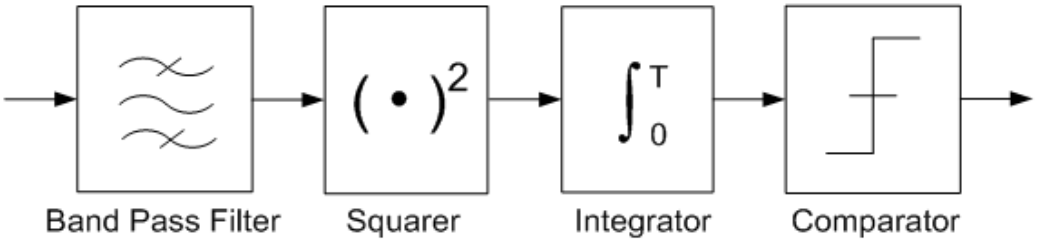

Figure 4-6 Block diagram of software demodulator.

Figure 4-6 presents the block diagram of software demodulator for one channel (OOK/chirp) only. The incoming signal first goes through a bandpass filter to extract the signal within the channel. After that, it will be fed to a squarer for energy detection. An integrator is employed to suppressed high frequency carriers and in-band high frequency noise. Finally, digital output data can be obtained through a slicer. The collected transmitter output from oscilloscope is first sent through the comb shape acoustic channel model using MATLAB [8]. The resulting output is then demodulated through software demodulator. It should be pointed out that same software demodulation approach has been adopted in [1].

4.3.2 OOK

Figures 4-7 and 4-8 show the time-domain 6-channel OOK modulation signal measured at 25℃ and demodulated data generated by acoustic telemetry transmitter which employs FLL with RC phase shifter, respectively. The signal is collected from oscilloscope and sent to the Matlab model of acoustic channel. Then it is demodulated by the software demodulator shown in Figure 4-6. The total data rate of 6-channel OOK modulation is 120bps with SNR of 10dB.

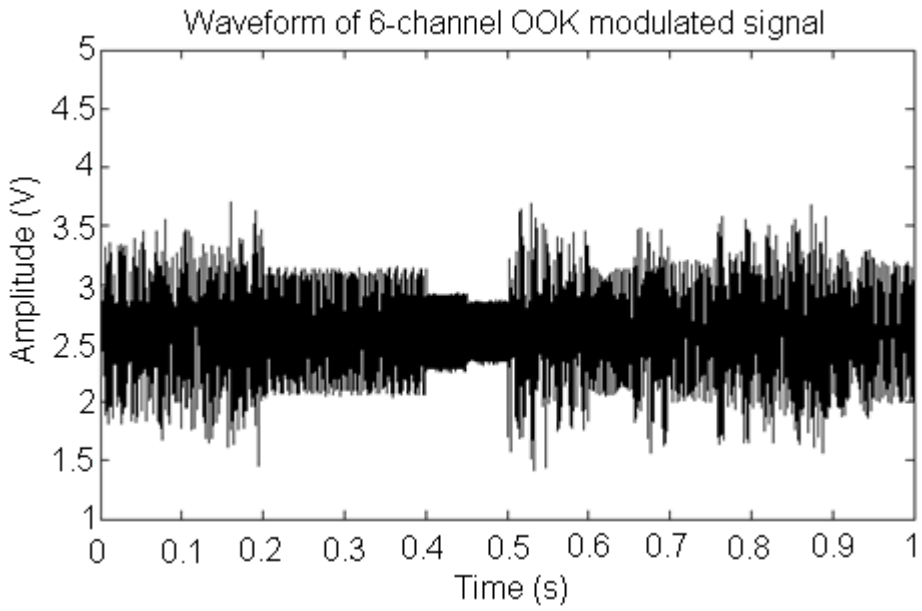

Figure 4-7 Time domain wave form of 6-channel OOK modulated signal generated by acoustic telemetry transmitter which employs FLL with RC phase shifter at 25°C.

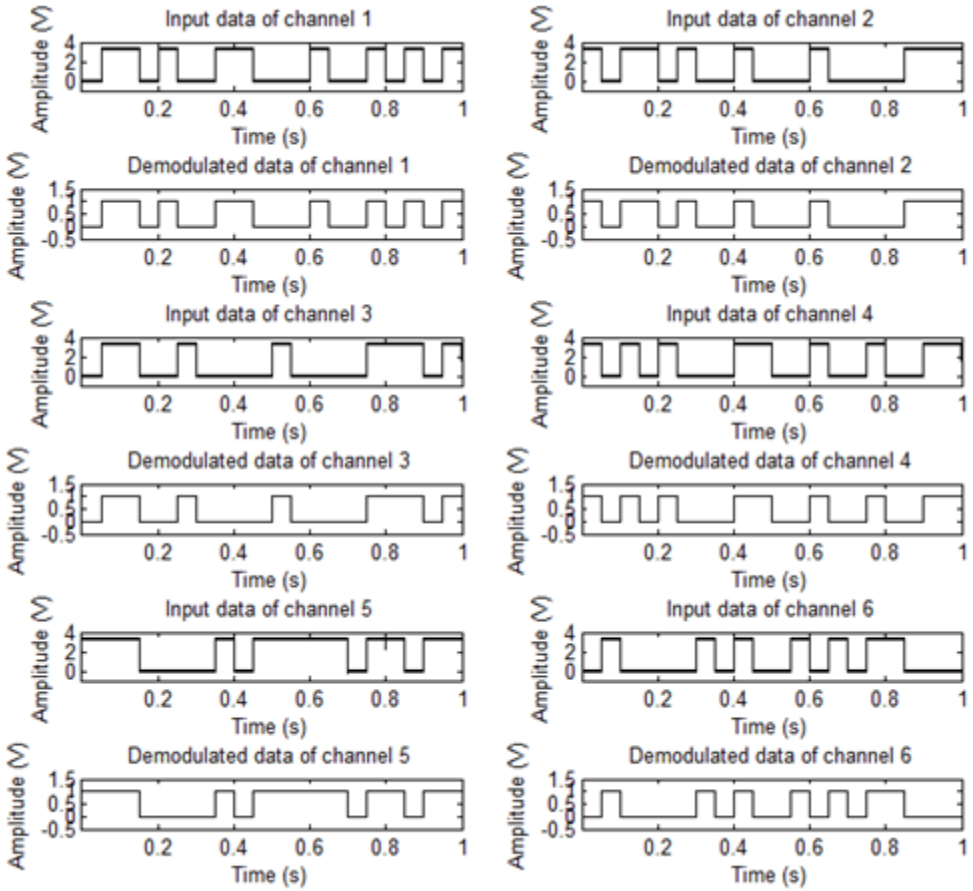

Figure 4-8 Input data and demodulated OOK data of acoustic telemetry transmitter which employs FLL with RC phase shifter at 25°C.

Figures 4-9 and 4-10 show the time-domain 6-channel OOK modulation signal measured at 25℃ and demodulated data generated by acoustic telemetry transmitter which employs FLL with FVC, respectively. The similar data processing procedure is applied. The total data rate of 6-channel OOK modulation is 120bps with SNR of 10dB.

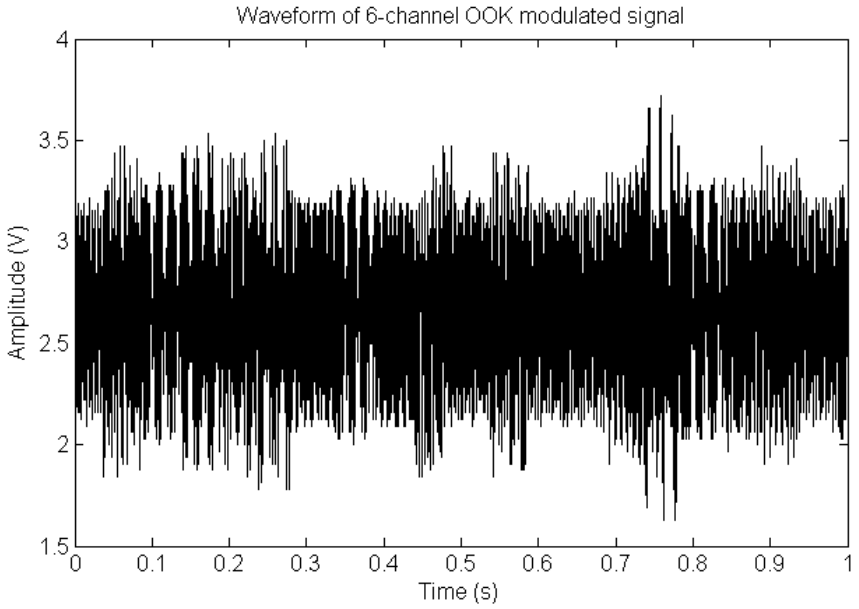

Figure 4-9 Time domain wave form of 6-channel OOK modulated signal generated by acoustic telemetry transmitter which employs FLL with FVC at 25°C.

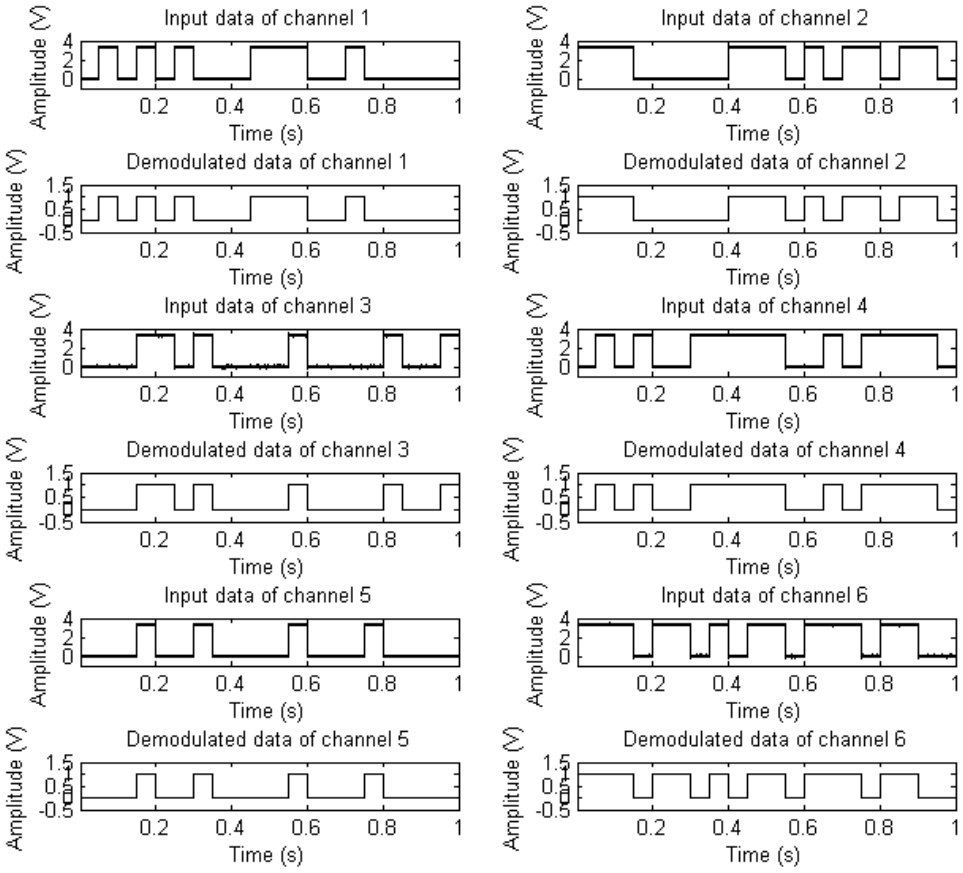

Figure 4-10 Input data and demodulated OOK data of acoustic telemetry transmitter which employs FLL with FVC at 25°C.

The acoustic telemetry transmitter is further verified at 225℃. The circuit of acoustic telemetry transmitter remains unchanged for two tapeouts, thus the high temperature measurement is only executed here to prove the functionality of this block. Figures 4-11 and 4-12 show the time-domain 6-channel OOK modulation signal measured at 225℃ and demodulated data generated by acoustic telemetry transmitter which employs FLL with FVC, respectively. The total data rate of 6-channel OOK modulation is 120bps with SNR of 10dB.

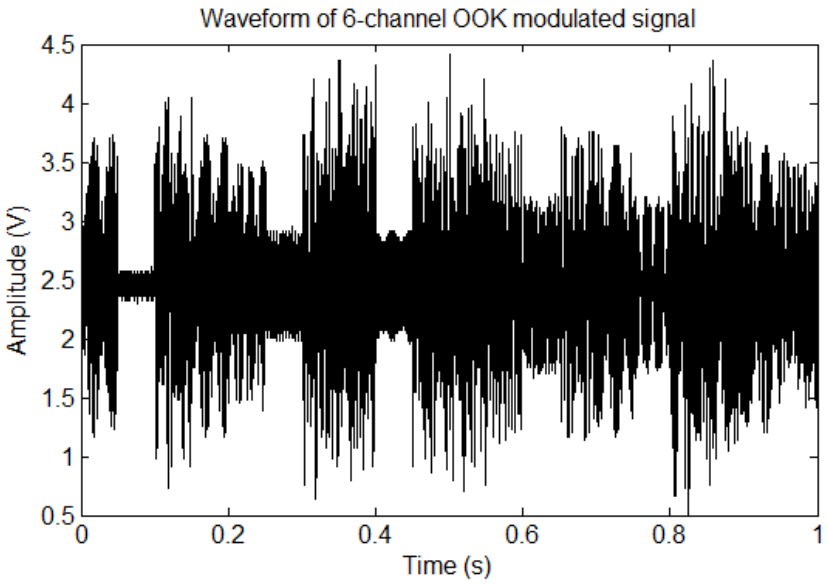

Figure 4-11 Time domain wave form of 6-channel OOK modulated signal generated by acoustic telemetry transmitter which employs FLL with FVC at 225°C.

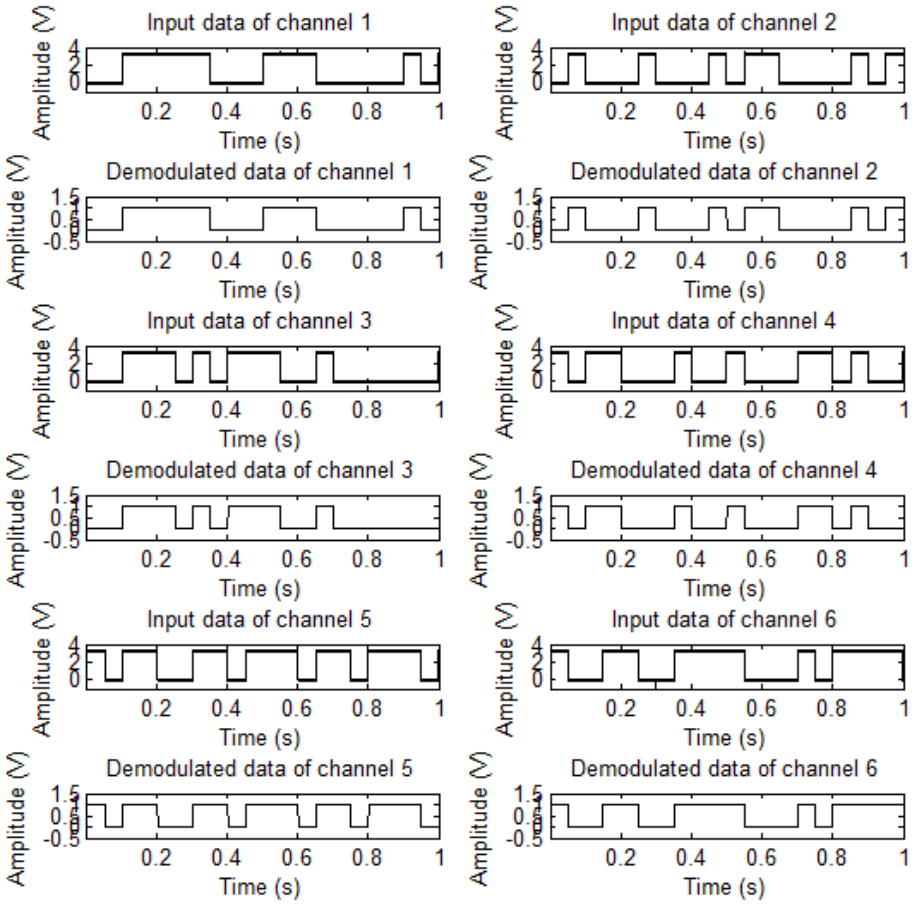

Figure 4-12 Input data and demodulated OOK data of acoustic telemetry transmitter which employs FLL with FVC at 225°C.

4.3.3 Chirp

Figures 4-13 and 4-14 show the time-domain 3-channel chirp modulation signal measured at 25℃ and demodulated data from acoustic telemetry transmitter which employs FLL with RC phase shifter, respectively. For chirp demodulation, the bandpass filter should use a wider passband than OOK demodulation. The total data rate of 3-channel chirp modulation is 60bps with SNR of 10dB.

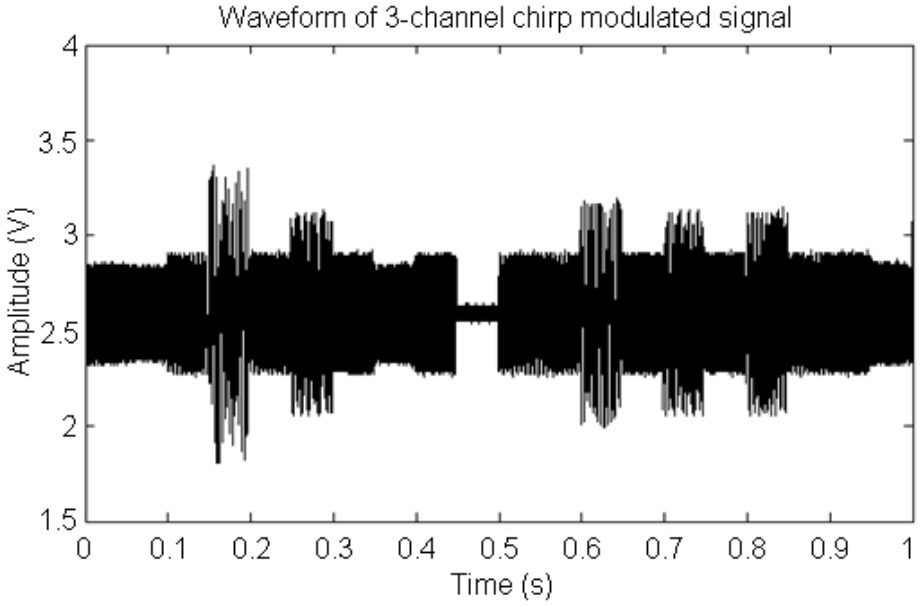

Figure 4-13 Time domain wave form of 3-channel chirp modulated signal generated by acoustic telemetry transmitter which employs FLL with RC phase shifter at 25°C.

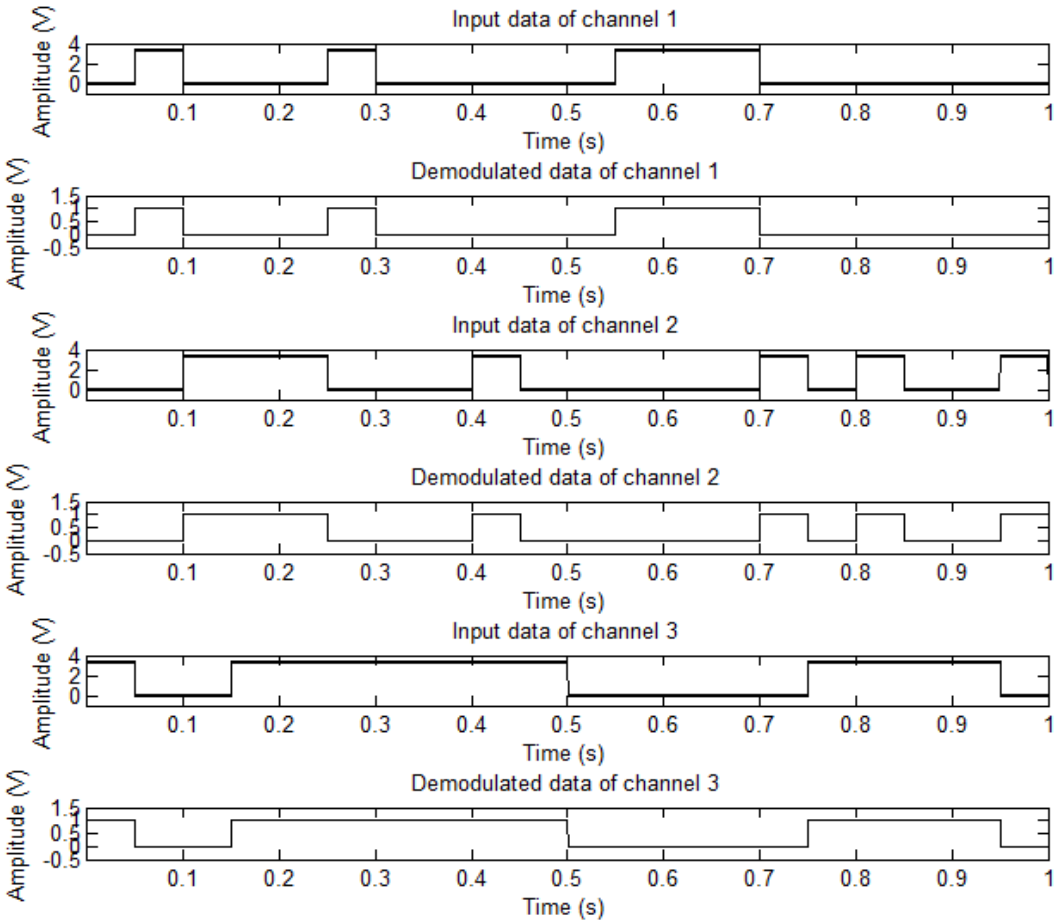

Figure 4-14 Input data and demodulated chirp data of acoustic telemetry transmitter which employs FLL with RC phase shifter at 25°C.

Figures 4-15 and 4-16 show the time-domain 3-channel chirp modulation signal measured at 25℃ and demodulated data from acoustic telemetry transmitter which employs FLL with FVC, respectively. The total data rate of 3-channel chirp modulation is 60bps with SNR of 10dB.

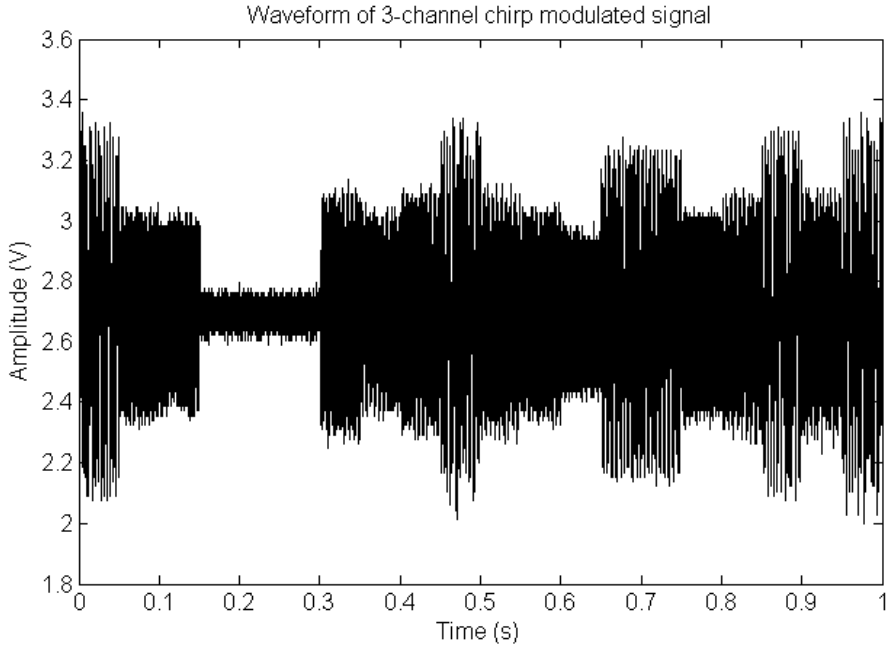

Figure 4-15 Time domain wave form of 3-channel chirp modulated signal generated by acoustic telemetry transmitter which employs FLL with FVC at 25°C.

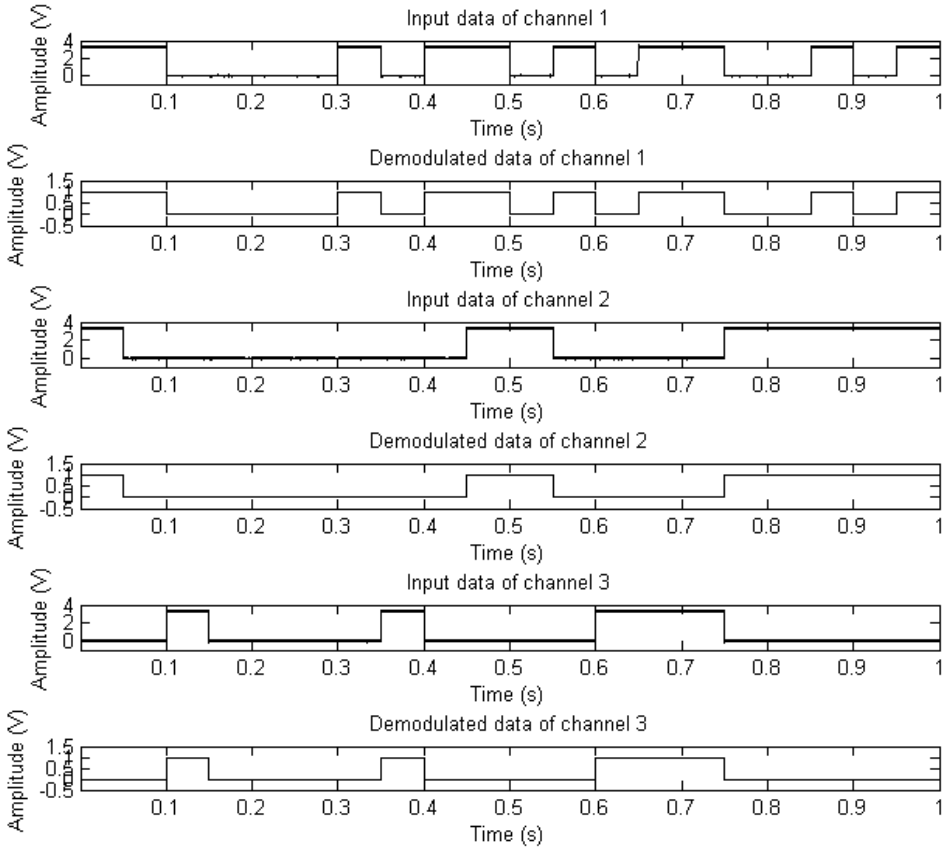

Figure 4-16 Input data and demodulated chirp data of acoustic telemetry transmitter which employs FLL with FVC at 25°C.

The acoustic telemetry transmitter is further verified at 225℃. Figures 4-17 and 4-18 show the time-domain 3-channel chirp modulation signal measured at 225℃ and demodulated data generated by acoustic telemetry transmitter which employs FLL with FVC, respectively. The total data rate of 3-channel chirp modulation is 60bps with SNR of 10dB.

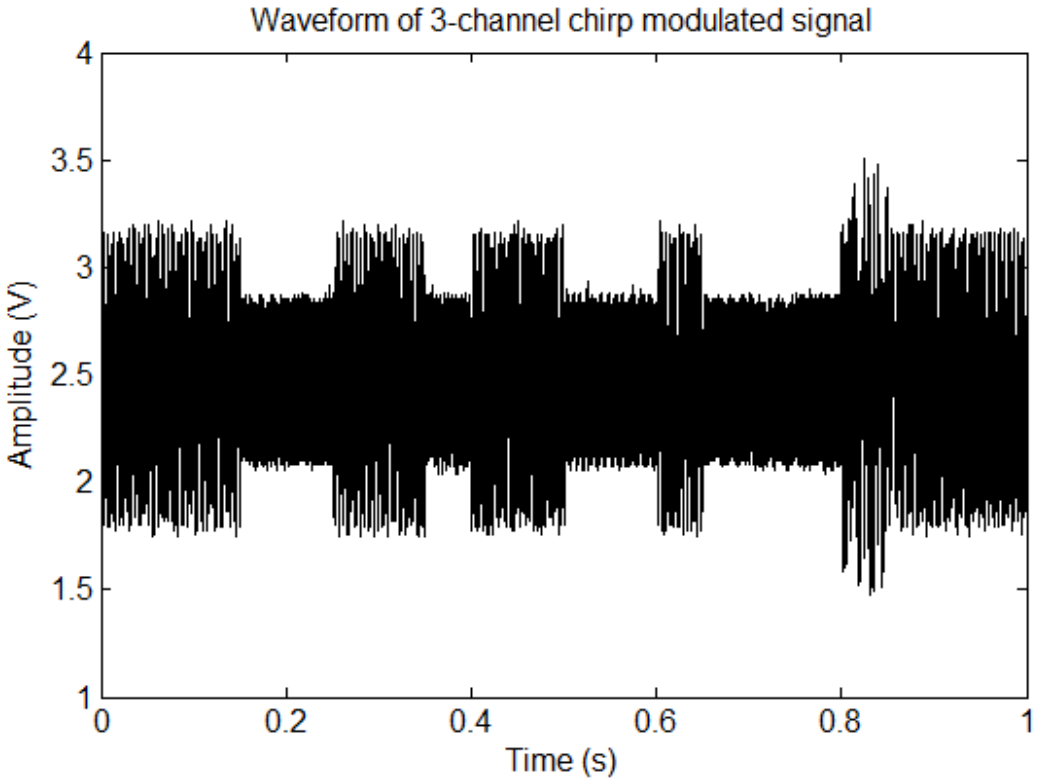

Figure 4-17 Time domain wave form of 3-channel chirp modulated signal generated by acoustic telemetry transmitter which employs FLL with FVC at 225°C.

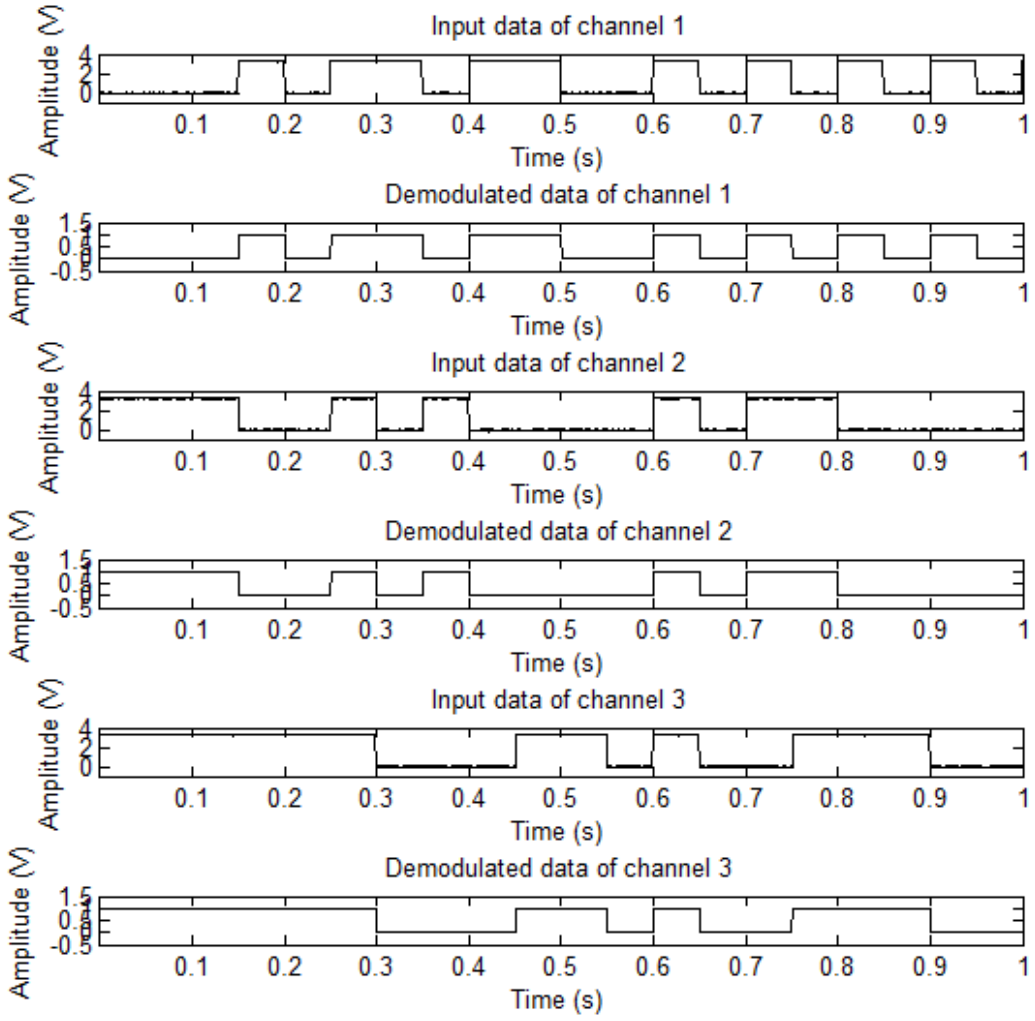

Figure 4-18 Input data and demodulated chirp data of acoustic telemetry transmitter which employs FLL with FVC at 225°C.

4.3.4 Acoustic Transmitter performance comparison

The transmitter performance is also compared in Table 4-1. All reported wireless acoustic telemetry systems are currently discrete solutions with very little system performance information. They also do not support more than two channels and can only provide single modulation. In contrast, our transmitter can provide multi-channel support with reconfigurable modulation. Our achieved data rate of 120bps is also the highest reported data rate to date.

Table 4-1 PERFORMANCE COMPARISON OF ACOUSTIC TRANSMITTERS

	[1]	[6]	This work
Number of channels	2	1	6/3
Modulation	OOK	Chirp	OOK/Chirp
Total data rate (bps)	40	20	120/60
Frequency resolution	NA	NA	0.1~0.8Hz

Chapter 5 Conclusion

5.1 Conclusion

In this work, a reconfigurable multi-channel acoustic telemetry transmitter is presented. Based on the acoustic channel characteristics, either OOK modulated signal or chirp modulated signal is generated. If the acoustic channel characteristic is well-defined, 6-channel OOK modulated signal is employed to achieve a total data rate of 120bps. If the acoustic channel characteristic is uncertain, the acoustic transmitter is configured to generate 3-channel chirp modulated signal to guarantee a successful transmission. The total data rate of chirp modulation is 60bps.

Two crystal-less temperature-independent frequency references are exploited to generate the carriers for acoustic transmitter. An FLL which employs RC phase shifter and resistor TC compensation technique is used and the achieved frequency inaccuracy is ±1.94% over the temperature range of 175℃ to 275℃. Another approach which utilizes a FLL with FVC is also studied. The measured frequency inaccuracy is ±2.85% over the temperature range of 25℃ to 300℃.

5.2 Future work

The crucial part in this work is the crystal-less temperature-independent frequency reference. Although two architectures use different methods to convert the frequency information into a signal for FLL's comparison, the temperature compensation are both implemented using resistor TC compensation technique.

However, due to the process variation, the actual values of the resistors may vary up to ±20%. Moreover, the TCs of the two different types of resistors also change due to process variation. As a result, the resistor TC compensation technique may not work as well as simulation. If the RC phase shifter and the FVC can exhibit a better temperature characteristic, the frequency inaccuracy of FLL can be further improved. Resistor calibration can be adopted to improve the accuracy of the resistor TC compensation technique. Based on the real TCs of two types of resistors, the values of the resistor are adjusted to minimize the combined TC. Resistor calibration is usually implemented using switched resistor array and the accuracy of the calibration is limited by the size of the resistor array. A new resistor calibration is exploited using digital ΔΣM. Two FVCs are implemented using different resistors RHIRES and RMIDRES, respectively. Hence the outputs of each FVC can be expressed as

$$V_{FVC\_RHIRES} = V_{REF} R_{HIRES} C_S f_{drive} \tag{5.1}$$

$$V_{FVC\_RMIDRES} = V_{REF} R_{MIDRES} C_S f_{drive} \tag{5.2}$$

V_{FVC_RHIRES} and $V_{FVC\_RMIDRES}$ have opposite TCs. A digital ΔΣM is employed to control which output of V_{FVC_RHIRES} and $V_{FVC\_RMIDRES}$ is fed to the 1st order DT ΔΣM. Assume the average value of the output bitstream from the digital ΔΣM is α. Then, the actual value V_{FVC_ACTL} seen by the 1st order DT ΔΣM is

$$V_{FVC\_ACTL} = \alpha \cdot V_{REF} R_{HIRES} C_S f_{drive} + (1-\alpha) \cdot V_{REF} R_{MIDRES} C_S f_{drive} \tag{5.3}$$

By properly setting the input of the digital ΔΣM, we can satisfy the following equation:

$$\frac{\alpha}{\alpha - 1} = \frac{TC_{RMIDRES}}{TC_{RHIRES}} \tag{5.4}$$

In this way, we can compensate the temperature dependency of the resistors in FVC. This method has been designed and sent for fabrication.

Bibliography

[1] V. Shah et al., "Design consideration for a new high data rate LWD acoustic telemetry system," SPE88636, Proc. of the Asia Pacific Oil and Gas Conf. and Exhib., Oct. 2004.

[2] Barnes et al., "Passband for acoustic transmission," JASA, vol. 51(5), pp. 1606-1608, 1972.

[3] Drumheller D. S., "Acoustic properties of drill strings," JASA, vol. 85(3), pp. 1048-1064, 1989.

[4] Lee H. Y., "Drillstring axial vibration and wave propagation in boreholes," Ph. D thesis, MIT, 1991.

[5] Ramarao N. V., "Radiation and vibration of drilling tubular in fluid-filled boreholes," Ph. D thesis, MIT, 1996.

[6] P. L. Camwell, J. G. McRory, and J. M. Neff, "Acoustic telemetry, with multiple nodes in drillstring, used to achieve distributed MWD," Drilling Contractor, pp. 30-35, Mar. 2009.

[7] Jeff Watson and Gustavo Castro, "High-temperature electronics pose design and reliability chanlleges," Analog Dialogue, vol. 46, no. 4, pp. 3-9, Apr. 2012.

[8] L. S. Kumar et al., "Downhole pipe selection and arrangement for acoustic drillstring telemetry," IEEE Industrial Electronics and Applications, pp. 1539-1542, Jul. 2012.

[9] M. S. McCorquodale et al., “A 25-MHz self-referenced solid-state frequency source suitable for XO replacement,” IEEE Trans. on Circuits and Systems-I, vol. 56, no. 5, pp. 943-956, May 2009.

[10] Erdogan Ozgur Ates, Devrim Yilmaz Aksin and Pinar Basak Basyurt, “CMOS Colpitts LC reference oscillator with 70ppm absolute frequency accuracy within 0-80°C,” in IEEE Int. Midwest Symp., Aug. 2009, pp. 1002-1005.

[11] M. S. McCorquodale et al., “A silicon die as a frequency source,” in Proc. IEEE Int. Frequency Control Symp., Jun. 2010, pp. 103-108.

[12] Erdogan Ozgur Ates, Atilim Ergul, and Devrim Yilmaz Aksin, “Fully integrated frequency reference with 1.7 ppm temperature accuracy within 0-80°C,” IEEE J. Solid-State Circuits, vol. 48, no. 11, pp. 2850-2859, Nov. 2013.

[13] Y. Tokunaga et al., “An on-chip CMOS relaxation oscillator with voltage averaging feedback,” IEEE J. Solid-State Circuits, vol. 45, no. 6, pp. 1150-1158, Jun, 2010.

[14] P. F. J. Geraedts et al., “A 90µW 12MHz relaxation oscillator with a -162dB FOM,” in IEEE ISSCC Dig. Tech. Papers, 2008, pp. 348-349.

[15] Arun Paidimarri et al., “A 120nW 18.5kHz RC oscillator with comparator offset cancellation for ±0.25% temperature stability,” in IEEE ISSCC Dig. Tech. Papers, 2013, pp. 184-185.

[16] V. D. Smedt et al., "A 66 μW 86ppm/ºC fully integrated 6MHz Wienbridge oscillator with a 172 dB phase noise FOM," IEEE J. Solid-State Circuits, vol. 44, no. 7, pp. 1990-2001, Jul. 2009.

[17] K. Sundaresan, P. E. Allen, and F. Ayazi, "Process and temperature compensation in a 7-MHz CMOS clock oscillator," IEEE J. Solid-State Circuits, vol. 41, no. 2, pp. 433-442, Feb. 2006.

[18] Chien-Ying Yu, and Chen Yi Lee, "A 0.6V 200kHz silicon oscillator with temperature compensation for wireless sensing applications," in Proc. 54th IEEE MWSCAS, 2011, pp. 1-4.

[19] J. Lee and S. Cho, "A 10MHz 80μW 67ppm/°C CMOS reference clock oscillator with a temperature compensated feedback loop in 0.18μm CMOS," in Proc. Symp. VLSI Circuits, Jun. 2009, pp. 226-227.

[20] K. Ueno, T. Asai, and Y. Amemiya, "A 30 MHz, 90-ppm/℃ fully-integrated clock reference generator with frequency-locked loop," in Proc. European Solid-State Circuits Conf. Sep. 2009, pp. 392-395.

[21] S. M. Kashmiri, M. Pertijs, and K. Makinwa, "A thermal-diffusivity-based frequency reference in standard CMOS with an absolute inaccuracy of ±0.1% from 55°C to 125°C," IEEE J. Solid-State Circuits, vol. 45, no. 12, pp. 2510-2520, Dec. 2010.

[22] K. A. A. Makinwa and M. F. Snoeij, "A CMOS temperature-to-frequency converter with an inaccuracy of less than ±0.5°C (3σ) from -40°C to 105°C," IEEE J. Solid-State Circuits, vol. 41, no. 12, pp. 2992-2997, Dec. 2006.

[23] S. Mahdi Kashmiri, Kamran Souri, and K. A. A. Makinwa, "A scaled thermal-diffusivity-based 16 MHz frequency reference in 0.16µm CMOS," IEEE J. Solid-State Circuits, vol. 47, no. 7, pp. 1535-1545, Jul. 2012.

[24] Peter Y. Yu, Manuel Cardona, *Fundamentals of Semiconductors: Physics and Materials Properties*, Springer, 2010.

[25] Colinge, Jean-Pierre, *Silicon-on-insulator technology: materials to VLSI*, Birkhäuser, pp.3, 2004.

[26] S. M. Kashmiri, Sha Xia and K. Makinwa, "A temperature-to-digital converter based on an optimized electrothermal filter," IEEE J. Solid-State Circuits, vol. 44, no. 7, pp. 2026-2035, Jul. 2009.

[27] Cailin Davis and Ivars Finvers, "A 14-bit high-temperature ΣΔ modulator in standard CMOS," IEEE J. Solid-State Circuits, vol. 38, no. 6, pp. 976-986, Jun. 2003.

[28] Phillip. E. Allen and Douglas R. Holberg, *CMOS Analog Circuit Design*, Oxford University Press, 2002.

[29] Behzad Razavi, *Design of Analog CMOS Integrated Circuit*, McGraw-Hill, 2001.

[30] R. Jacob Baker, *CMOS: Circuit Design, Layout and Simulation*, Willey, 1998.

[31] Dongmin Park, SeongHwan Cho, "A 14.2mW 2.55-to-3GHz cascaded PLL with reference injection, 800MHz delta-sigma modulator and 255fs_{rms} integrated jitter in 0.13µm CMOS," ISSCC 2012.

[32] Steven A. Tretter, Communication System Design Using DSP Algorithms, *Springer*, 2003.

[33] Bram De Muer and Michiel Steyaert. CMOS fractional-N synthesizers: Design for high spectral purity and monolithic integration. Boston: Kluwer Academic Publishers, 2003, pp. 36-38.

[34] Todd K. Moon, *Error Correction Coding: Mathematical Methods and Algorithms*, John Wiley & Sons, 2005.

[35] Michael Youssef, Alireza Zolfaghari, Behnam Mohammadi, Hooman Darabi and Asad A. Abidi, "A low-power GSM/EDGE/WCDMA polar transmitter in 65-nm CMOS," IEEE J. Solid-State Circuits, vol. 46, no. 12, pp. 3061-3074, Dec. 2011.

[36] R. Gregorian, K.W. Martin, G. C. Temes, "Switched Capacitor Circuit Design", Proceedings of the IEEE, vol.71 pp.941-966, 1983.

[37] R. Gregorian, G.C. Temes, Analog MOS Integrated Circuits for Signal Processing, John Willey & Sons, 1986.

[38] Mikko E. Waltari, Kari A. I. Halonen, Circuit Techniques for Low-Voltage *and High-Speed A/D Converters*, Springer, pp.75-76, 2002

[39] Sadeghi, N., Mirabbasi, S., Bennington, C.P.J., "A 2.5V 0.13µm CMOS Amplifier for A High Temperature Sensor System", *NEWCAS-TAISA' 09*, 2009.

[40] Joselyn Torres et al., "A low-power high-PSRR clock-free current-controlled class-D audio amplifier," IEEE J. Solid-State Circuits, vol. 46, no. 7, pp. 1553-1561, Jul. 2011.

[41] Rojas-Gonzalez M. A. and Sanchez-Sinencio, E., "Low-power high-efficiency class D audio power amplifiers," IEEE J. Solid-State Circuits, vol. 44, no. 12, pp. 3272-3284, Dec. 2009.

[42] Michael Steffes. "Design Methodology for MFB filters in ADC interface applications." Internet: http://www.ti.com/lit/an/sboa114/sboa114.pdf, Feb. 2006, [Jan. 2012].