STRAIN ENGINEERING FOR ADVANCED SILICON TRANSISTORS

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NATIONAL UNIVERSITY OF SINGAPORE

2013

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(B.Eng.(Hons.)), NUS

A THESIS SUBMITTED
FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL AND
COMPUTER ENGINEERING
NATIONAL UNIVERSITY OF SINGAPORE

2013

Declaration

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Ding Yinjie

26 March 2014

Acknowledgements

First and foremost, I would like to express my sincere gratitude to my PhD supervisor, Prof. Yeo Yee-Chia for his patience and support throughout my time here at National University of Singapore (NUS). His technical guidance and insights from our countless discussions has been invaluable. He is instrumental in instilling a strong work ethic and shaping my career goals. I am also very thankful for his time and efforts in guiding this dissertation.

I would like to thank GLOBALFOUNDRIES Singapore and Economic Development Board of Singapore for funding my graduate studies through a graduate scholarship award. I am grateful to Dr. Lap Chan from Singapore University of Technology and Design, Dr. Ng Chee Mang, and Mr. Leong Kam Chew from GLOBALFOUNDRIES Singapore for their discussions. Their personal and professional advice has been invaluable. I have benefited greatly from their vast experience in the field of semiconductor technologies. I would also like to thank Prof. Zhu Chun Xiang and Prof. Tan Leng Seow for serving on my qualifying examination committee, both of whom have provided valuable feedback.

I would like to acknowledge the technical staffs in Silicon Nano Device Laboratory (SNDL) specifically Mr Patrick Tang, Mr O Yan, and Ms. Yu Yi in providing technical and administrative support and keeping the cleanroom and lab running smoothly. Besides SNDL, a large portion of my research and experiments were also conducted over at Institute of Materials Research and Engineering (IMRE) and Singapore Institute of Manufacturing Technology (SIMTech). I appreciate the support extended by the staffs at IMRE and SIMTech. I would particularly like to thank Dr. Wang Xincai from SIMTech for all his support and assistance in laser annealing.

Thanks also go out to Dr. Deng Jie, Mr. Chum Chan Choy, Ms. Hui Hui Kim, and Ms. Teo Siew Lang from IMRE for their help in EBL patterning and TEM analysis. Additionally, I would like to extend my appreciation to Dr. Du Anyan from GLOBALFOUNDRIES Singapore for his timely discussions and NBD analysis, without which some of the work entailed in this thesis would not have been possible. I would also like to thank Nicolas Daval, Bich-Yen Nguyen, and Konstantin Bourdelle from SOITEC for their valuable discussions and UTBB-SOI wafer support.

I am grateful for the guidance and discussions from the many outstanding graduate students from SNDL. I would like specially thank Dr. Koh Shao Ming for mentoring me in the initial phase of my research, and the effort in fabricating FinFETs that used in this research work, without which many of the work entailed in this thesis would not have been possible. Special thanks also go out to Dr. Liu Bin, Dr. Gong Xiao, Dr. Zhou Qian, Cheng Ran, Eugene, Dr. Yang Yue, Tong Yi, Dr. Guo Pengfei, Dr. Zhang Xingui, Wang Lanxiang, Dr. Ashvini Gyanathan, Tong Xin, Zhu Zhu, and Dr. Han Genquan for their discussions and support in experiments and measurements during the critical submission deadlines. I would also like to extend an enormous thanks to Goh Kian Hui, Ivana, Low Kain Lu, Dr. Samuel Owen, Sujith Subramanian, Dr. Wang Wei, Zhan Chunlei, Dr. Liu Xinke, Dong Yuan, Xu Xin, and many more for their friendship, support and lively and simulating discussions over a wide range of topics. They have made my time at NUS truly enjoyable.

I would also like to express my deepest gratitude to my family for their continuous support and encourage since I embarked on my graduate studies. Lastly, but certainly not least, I would like to thank my wife, Zha Jie for her endless support and love through my candidature. A thank to my lovely son, Ruizhe, for bringing so much joy to my life.

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Abstract

Strain engineering for advanced silicon transistors

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While the aggressive geometrical scaling of transistors increases the performance-to-cost ratio for integrated-circuit-based products, it has met immense challenges as the transistor enters the deep-submicrometer regime (with gate length smaller than 250 nm), limited by phenomena such as short-channel effects (SCEs), high leakage current (subthreshold leakage or gate leakage), and dielectric breakdown. Alternative means of transistor performance enhancement have been explored recently, such as novel transistor structures, new materials, and strain engineering. To further scale down the transistor dimensions while maintaining good performance, advanced device structures such as ultra-thin-body field-effect transistors (UTB-FETs) and multiple-gate or fin field-effect transistors (FinFETs) are required at sub-20 nm technology nodes. To enhance the performance of such structures, strain technologies have to be developed for integration in UTB-FETs and FinFETs.

In this thesis, novel strain engineering techniques were explored and demonstrated in advanced Si transistors, such as nanoscale UTB-FETs and FinFETs.

This thesis work provides options of strain engineering for enhancing the performance of advanced transistors at the 20-nm technology node and beyond.

A novel way of introducing strain in ultra-thin body and buried-oxide (UTBB) SOI structures by implantation of Ge ions (Ge^+) followed by crystallization to form localized SiGe regions underneath the buried oxide (BOX) was demonstrated. The localized SiGe regions result in local deformation of the ultra-thin Si. Compressive strain of up to -0.55% and -1.2% were detected by Nano-Beam Diffraction (NBD) at the center and the edge, respectively, of a 50 nm wide ultra-thin Si region located between two local SiGe regions. The under-the-BOX SiGe technique was integrated in n-channel UTB-FETs (nUTB-FETs). The localized SiGe regions was found by finite-element simulation to induce a longitudinal (source-to-drain direction) tensile stress up to ~3000 MPa in the channel region. Significant drive current enhancement of ~18% was observed for the nUTB-FET with under-the-BOX SiGe compared to the control device. The under-the-BOX SiGe regions may be useful for strain engineering of ultra-thin body transistors formed on UTBB-SOI substrates.

A novel $Ge_2Sb_2Te_5$ (GST) liner stressor for enhancing the drive current in p-channel FinFETs (p-FinFETs) was explored. When amorphous GST (α-GST) changes phase to crystalline GST (c-GST), the GST material contracts. This phenomenon is exploited for strain engineering of p- FinFETs. A GST liner stressor wrapping a p-FinFET can be shrunk or contracted to generate very high channel stress for drive current enhancement. Saturation drain current I_{Dsat} enhancement of ~30% is observed for the FinFETs with α-GST liner over unstrained control FinFETs, due to the intrinsic compressive stress in α-GST. When phase-changed to crystalline state, I_{Dsat} enhancement of ~88% was observed for FinFETs with c-GST liner stressor over the control or unstrained FinFETs. The drain current enhancement increases with

decreasing gate length. The drain current enhancements for different fin rotations were also investigated, where the rotated FinFETs with c-GST stressor were compared with control FinFETs of the same rotation. Significant I_{Dsat} enhancement was observed for strained FinFETs with various fin rotations, with the highest enhancement observed for 0°-rotated FinFETs due to the directional dependence of the piezoresistance coefficients. GST liner stressor could be a strain engineering option in sub-20 nm technology nodes.

The local strain components in the source/drain (S/D) and channel regions of Si FinFET structures wrapped around by a GST liner stressor were investigated for the first time using NBD. When the GST layer changes phase from amorphous to crystalline, it contracts and exerts a large stress on the Si fins. This results in large compressive strain in the S/D region of <$\bar{1}$10>-oriented Si FinFETs of up to -1.15% and -1.57% in the <110> (horizontal) and <001> (vertical) directions, respectively. In the channel region of the FinFETs under the metal gate, the GST contraction results in up to -1.47% and -0.61% compressive strain in the <110> and <001> directions, respectively. In the channel region, the <110> compressive strain is higher at the fin sidewalls and lower near the fin center, while the <001> compressive strain is lower at the sidewalls and higher near the center. The effects of the Si fin and GST profiles on the stress distribution were studied using simulation. It was found that having a slanted fin structure would increase the stress at the centre of the fin.

Another novel ZnS-SiO$_2$ liner stressor was reported to enhance drive current in Si n-channel FinFETs (n-FinFETs). ZnS-SiO$_2$ expands during thermal anneal due to an increase in crystallite size. A ZnS-SiO$_2$ liner stressor wrapping around an n-FinFET can be expanded and exerts high tensile stress in the n-FinFET channel for drive current enhancement. Significant drive current enhancement was observed for n-FinFETs with as-deposited ZnS-SiO$_2$ liner over the control FinFETs without liner, due to the intrinsic

tensile stress in ZnS-SiO_2. After ZnS-SiO_2 expansion, the expanded ZnS-SiO_2 liner induces a higher tensile stress in the channel region and enhances the Si n-FinFET drive current further. Saturation drain current enhancement of ~26% and linear drain current enhancement of ~48% were observed for FinFETs with expanded ZnS-SiO_2 liner stressor compared to control FinFETs without liner, with no compromise on short channel effects. This technology was realized on FinFETs with Si:C S/D stressors and Al-incorporated NiSi contacts. ZnS-SiO_2 liner stressor could be a strain engineering option for n-FinFETs at sub-20 nm technology nodes.

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List of Symbols

a	Lattice constant
a^*, b^*, c^*	Reciprocal lattice vectors
C	Capacitance
C_{OX}	Gate oxide capacitance
d_i	Separation between the center 0 and a diffraction peak in NBD
D_{it}	Interface trap density
E_{sat}	Saturation electrical field
f	Atomic scattering factor
F	Elastic stiffness matrix
g	Reciprocal lattice vector
G_M	Transconductance
$G_{MLinMax}$	Linear saturation transconductance
G_{MSat}	Saturation transconductance
$G_{MSatMax}$	Peak saturation transconductance
h	Number of atoms in an assembly
H_{fin}	Fin height
i	Integer
I	Current
I_{Dlin}	Linear drain current
I_{Dsat}	Saturation drain current
I_G	Gate leakage current
I_{off}	Off-state current
I_{on}	On-state current
I_{SD} or I_D	Drain current
J	Scattering vector

l	Integer
L_G	Gate length
m	Integer
m^*	Hole effective mass
n	Integer
N	Doping concentration
N_{Ref}	Number of reference points in NBD
P	Thermal factor
Q_{IT}	Interface trap
Q_{OX}	Fixed oxide charge
Q_{inv}	Inversion charge density
r	Vector in 3D space
R_{CH}	Channel resistance
R_h	Atomic position
R_{Ext}	External series resistance
R_{SD}	S/D resistance
R_{Total}	Total resistance
R_p	Projected range
s	Standard deviation of the strain values in NBD
S	Inverse compliance matrix
σ_{yy}	The stress along the current flow direction
T	Temperature
T_{BOX}	Buried oxide thickness
T_{HM}	Hardmask thickness
T_{OX}	Oxide thickness
V	Voltage
V_{DD}	Supply voltage
V_{DS}	Drain voltage

V_{GS}	Gate voltage
V_{sub}	Substrate bias
V_{TH}	Threshold voltage
$V_{TH,lin}$	Linear threshold voltage
$V_{TH,sat}$	Saturation threshold voltage
w	Incident electron wave vector
w_0	Diffracted electron wave vector
W	Channel width
W_{Eff}	Effective gate width
W_{fin}	Fin width
W_G	Gate width
ΔV_{TH}	Threshold voltage shift
Y	Young's modulus
μ	Carrier mobility
μ_e	Effective electron mobility
π	Piezoresistance coefficients
ρ	Resistivity
$\sigma_{//}$	Longitudinal stresses
$\sigma_{\perp}$	Transverse stresses
$\varepsilon_{//}$	Longitudinal strain
$\varepsilon_{\perp}$	Transverse strain
υ_{inj}	Thermal injection velocity
Φ_B^N	Effective eletron barrier height
$\mathcal{F}$	Fourier transfer
$\Phi_s(r)$	Electron source wave function
ψ_S	Surface potential
$\Delta\mu$	Strain induced mobility change
μ_{eff}	Effective mobility

δ	Delta function
κ	Relative dielectric constant

List of Abbreviations

ALD	Atomic layer deposition
As	Arsenic
B	Boron
BOX	Buried oxide
CD	Critical dimension
CCD	Charge-coupled device
CESL	Contact etch stop layer
CET	Capacitance equivalent thickness
CMOS	Complementary metal-oxide-semiconductor
CVD	Chemical vapour deposition
DHF	Dilute hydrofluoric acid
DIBL	Drain induced barrier lowering
DIW	Deionized water
DLC	Diamond-like carbon
DSS	Dopant segregation Schottky
EBL	Electron beam lithography
EOT	Equivalent oxide thickness
FIB	Focused ion beam
FinFET	Fin-type field effect transistor
GAA	Gate-All-Around
GaAs	Gallium arsenide
Ge	Germanium
GeSn	Germanium-tin
HRTEM	High resolution transmission electron microscopy
IV	Current-voltage
InAs	Indium arsenide

InGaAs	Indium gallium arsenide
InSb	Indium antimonide
MOSFET	Metal-oxide-semiconductor field-effect transistor
MuGFET	Multiple-gate field-effect transistors
NBD	Nano beam diffration
NiGe	Nickel germanide
P	Phosphorus
PAI	Pre-amorphization implant
P-FET	P-channel field-effect transistor
PR	Photoresist
PECVD	Plasma enhanced chemical vapour deposition
RDF	Random dopant fluctuation
RIE	Reactive ion etcher
RSD	Raised source/drain
RTP	Rapid thermal processing
S/D	Source/drain
SB	Schottky barrier
SCE	Short channel effect
SEM	Scanning electron microscopy
Si	Silicon
SiC	Silicon carbon
SiGe	Silicon germanium
SiN	Silicon nitride
SIMS	Secondary Ion Mass Spectrometry
SOI	Silicon on insulator
SS	Subthreshold swing
TEM	Transmission electron microscopy

TOF-SIMS	Time-of-Flight Secondary Ion Mass Spectrometry
UT	Ultra-thin
UTB-FET	Ultra-thin body field-effect transistor
UTBB-SOI	Ultra-thin body and buried oxide silicon-on-insulator
UT-BOX	Ultra-thin buried-oxide

Chapter 1

Introduction

1.1 Background

Transistor scaling in the past five decades has doubled the logic device density every two to three years. While smaller transistor dimensions enable better device performance and lower cost per logic function [1],[2], conventional scaling has become more challenging as the transistor enters the deep-submicrometer (with gate length smaller than 250 nm) regime [3]-[6], limited by phenomena such as short-channel effects (SCEs), high leakage current, and dielectric breakdown. The semiconductor industry has explored alternative means of transistor performance enhancement, such as novel transistor structures, new materials, and strain engineering. Among these new technologies, strain engineering, being a cost-effective and simple option, has been the major technique for continuous improvement of the transistor performance since the 90 nm technology node.

As an important transistor performance parameter, the saturation drain current (I_{Dsat}) affects circuit speed more than any other transistor parameters and is given by [2]:

$$I_{Dsat}= \frac{\mu_{eff}C_{ox}W}{2L_G}\frac{(V_G-V_{TH})^2}{1+\frac{(V_G-V_{TH})}{E_{sat}L_G}}, \tag{1.1}$$

where μ_{eff} is the carrier effective mobility, C_{ox} is the gate oxide capacitance, W is the transistor width, L_G is the gate length, V_G is the gate voltage, V_{TH} is the threshold voltage, and E_{sat} is the saturation electrical field.

I_{Dsat} can be increased by scaling down the gate oxide thickness, which increases C_{ox}. However, as the thickness of the gate oxide approaches 1 nm, the gate leakage current increases due to direct tunnelling [7]. Implementing high-κ (κ is the relative dielectric constant) gate dielectric materials allows a thicker gate dielectric to be used while maintaining the same or smaller equivalent SiO_2 thickness (EOT). This helps to suppress gate leakage current while maintaining or enhancing I_{Dsat}.

On the other hand, enhancing μ_{eff} by channel strain engineering is a promising solution for improving I_{Dsat} or I_{on}. Increased μ_{eff} allows a higher I_{on} to be achieved for a given I_{off}, as shown in Fig. 1.1. Increased I_{on} also results in shorter gate delay CV_{DD}/I_{on}, where C is the gate capacitance and V_{DD} is the supply voltage.

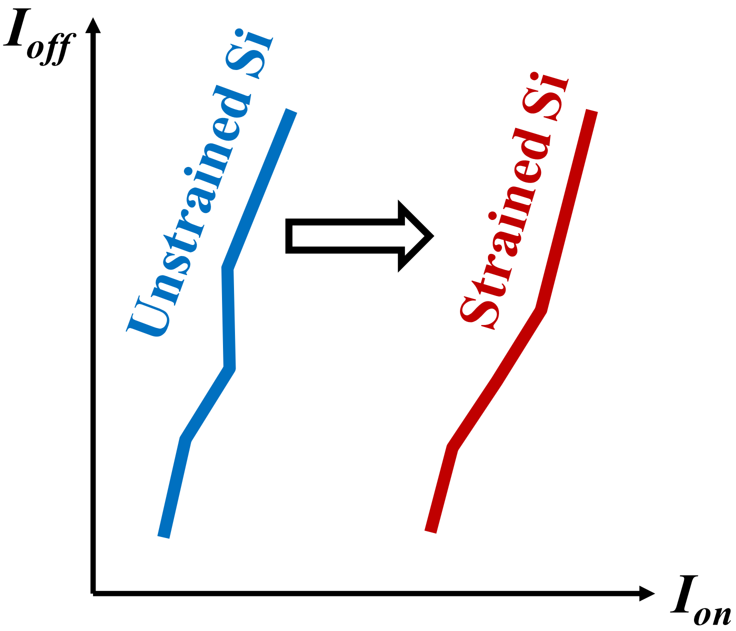


Fig. 1.1. A typical I_{off}-I_{on} plot showing that μ_{eff} enhancement through strain engineering increases I_{on} for a given I_{off}. I_{on} is the drain current when $V_{DS} = V_{GS} = V_{DD}$ (with source grounded) and I_{off} is the drain current when $V_{DS} = V_{DD}$ and $V_{GS} = 0$ V.

1.2 Strained Si Transistor Technology

Strain has been a topic of interest in semiconductor research since the 1950s. The integration of strain technology into Si transistors started in the 1990s, with biaxial stress the main focus of the industry [8]. 2.2 times electron mobility enhancement and 1.5 times hole mobility enhancement were reported by Wesler *et al.* [9] in 1992 and by Nayak *et al.* [10] in 1993, respectively. A review of the history and progress of high-mobility biaxially strained Si channel transistors was given by Lee *et al.* [8].

On the other hand, uniaxial stress is preferred and has become the current focus of the industry [3],[11]. First, compared to biaxial stress, uniaxial stress provides significantly larger mobility enhancement even at high vertical electric field due to larger warping of the conduction and valence bands [12]. Hence, the in-plane effective mass is smaller under uniaxial stress than under biaxial stress [11],[12]. Second, uniaxial stress causes smaller threshold voltage shift than biaxial stress [12]. As shown in Fig. 1.2, uniaxial stress can be incorporated into metal-oxide-semiconductor field-effect transistors (MOSFETs) for performance enhancement using a contact etch stop layer (CESL), as first demonstrated by Ito *et al.* [13] in *Int. Elec. Dev. Meet.* (IEDM) 2000. Silicon nitride (SiN) as a CESL, which can be configured to be tensile or compressive, induces tensile or compressive stress in the channel region and enhances the electron or hole mobility, respectively [14]-[16]. In general, performance enhancement increases linearly with SiN liner thickness. However, for a given SiN intrinsic stress, the drive current improvement saturates when the thickness of the SiN liner reaches a critical thickness [14]. A more effective liner stressor, diamond-like carbon (DLC), has been demonstrated for strain engineering in p-channel MOSFETs (pMOSFETs) [17],[18].

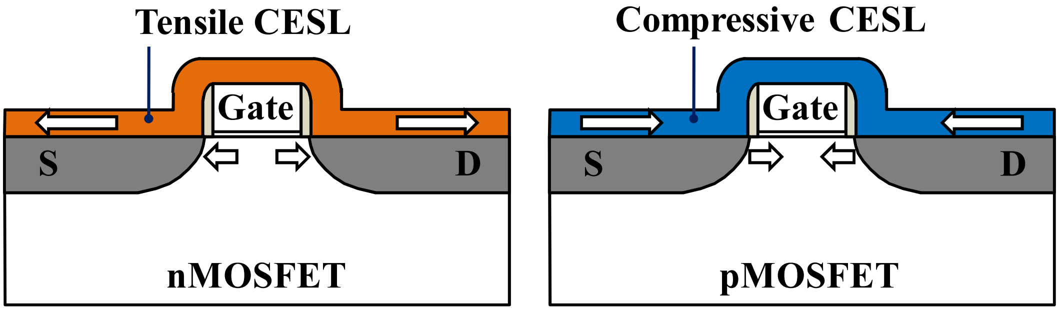


Fig. 1.2. MOSFETs with SiN CESL, which adheres to the source/drain (S/D) regions of the MOSFET. The SiN CESL has tensile or compressive intrinsic stress, which transfers to the MOSFET channel and results in electron or hole mobility enhancement, respectively.

DLC has an intrinsic compressive stress of up to 10 GPa, significantly greater than that of compressive SiN, and allows higher channel stress to be induced for a given liner thickness. DLC liner stressor thus gives significant I_{Dsat} enhancement for pMOSFETs [17],[18].

Another viable scheme for introducing uniaxial stress in the MOSFET channel is to incorporate stressors in the source/drain (S/D) regions of the MOSFET. Beneficial strain can be locally introduced in the transistor channel by embedding a material that is lattice-mismatched with respect to the Si channel in the S/D regions [19]-[36]. SiGe and silicon-carbon (Si:C) S/D stressors, induce compressive and tensile stress to enhance hole and electron mobility, respectively, were first demonstrated by P. Ranade *et al.* [19],[20] and K. W. Ang *et al.* [22].

As illustrated in Fig. 1.3(a), the introduction of SiGe, which has a larger lattice constant than Si, in the S/D regions of a p-channel transistor induces lateral compressive stress in the transistor channel [23]-[24] for hole mobility enhancement. The n-channel MOSFET (nMOSFET) counterpart of SiGe S/D stressors is Si:C, which has a lattice constant smaller than that of Si. When incorporated in the S/D regions of the transistor, Si:C stressors induce longitudinal tensile stress and vertical

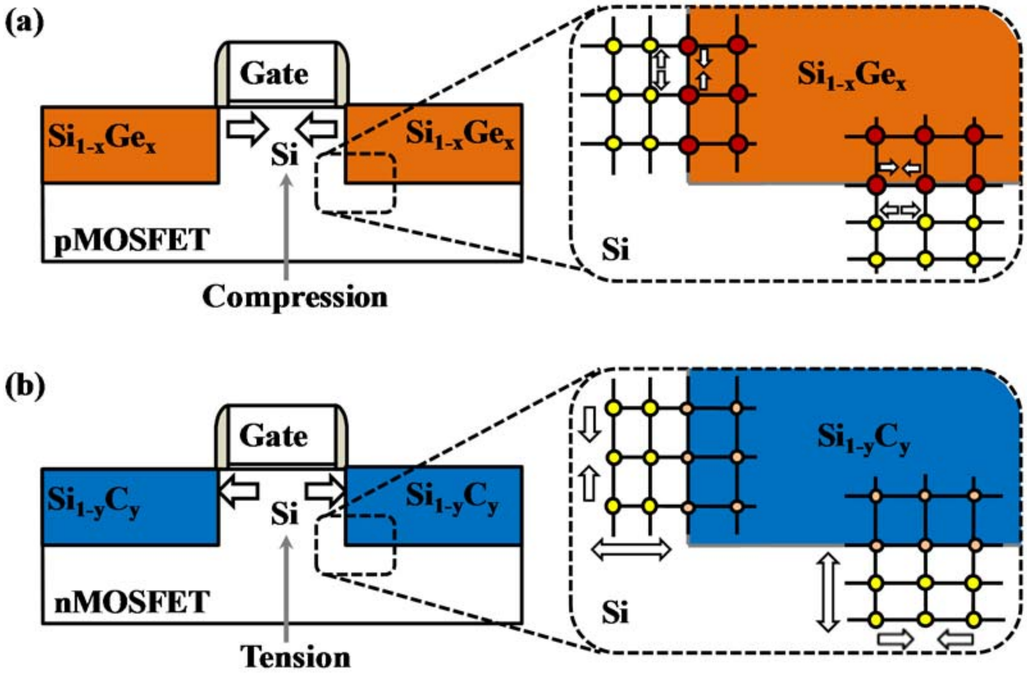


Fig. 1.3. Schematics of (a) SiGe and (b) Si:C lattice–mismatched S/D stressors in p- and nMOSFETs, respectively. The interactions of the SiGe and Si:C S/D stressors with the Si lattice at the heterojunctions are shown in the insets. SiGe in (a) has a larger lattice constant than Si, and induces longitudinal compressive stress in the transistor channel. Si:C in (b) has a lattice constant smaller than that of Si. When incorporated into the S/D regions of a nMOSFET, Si:C induces longitudinal tensile stress and vertical compressive stress in the channel.

compressive stress in the Si channel [Fig. 1.3(b)]. Both types of stress enhance electron mobility, leading to very significant drive current enhancement in Si nMOSFETs.

Besides CESL and S/D stressors, other strain engineering techniques have also been explored to enhance the drive current of MOSFETs, such as fully silicided gate-induced stress [38], stress memorization techniques [39], shallow trench isolation-induced stress [40], S/D silicide-induced stress [41], and combination of multiple stressors [42],[43]. Starting at the 90 nm technology node, uniaxial stress was successfully integrated into the mainstream MOSFET process flow to enhance transistor performance [44]-[47].

1.3 Strain Effects on Carrier Mobility

To define the stress for a unit element in Fig. 1.4, nine stress tensor components, σ_{ij}, must be specified [48]:

$$\sigma = \begin{bmatrix} \sigma_{11} & \sigma_{12} & \sigma_{13} \\ \sigma_{21} & \sigma_{22} & \sigma_{23} \\ \sigma_{31} & \sigma_{32} & \sigma_{33} \end{bmatrix}, \tag{1.2}$$

where the first index i denotes the face that the stress is applied on, while j indicates the direction of the applied stress. If $i = j$, the stress is normal to the specified surface (the blue arrows in Fig. 1.4), while $i \neq j$, σ_{ij} indicates a shear stress on face i (the orange arrows in Fig. 1.4). As the forces and moments sum to zero at static equilibrium, a stress tensor is always symmetric, that is, $\sigma_{ij} = \sigma_{ji}$. Hence, the tensor matrix above contains only six independent components [48].

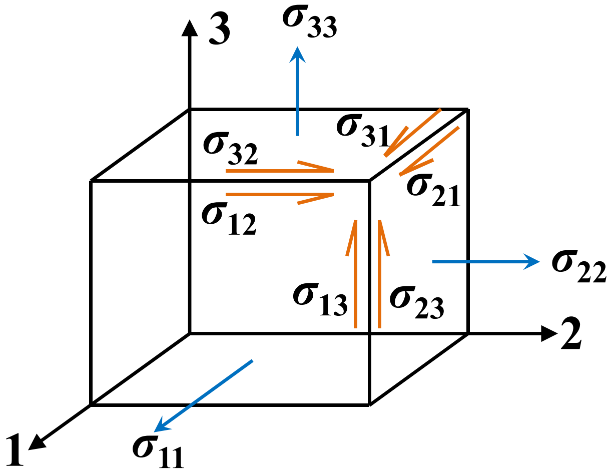


Fig. 1.4. Illustration of nine components, σ_{ij}, of stress on a unit element. If $i = j$, the stress is normal to the specified surface (the blue arrows), while $i \neq j$, σ_{ij} indicates a shear stress on face i (the orange arrows).

The strain, ε_{ij}, is also directional. For an isotropic material, stress is related to strain by Hooke's Law [49]:

$$\sigma = \varepsilon \cdot Y, \tag{1.3}$$

where Y is the Young's modulus of the material. For an anisotropic material such as Si, the Young's modulus depends on the crystal direction in which the material is being stretched, and a tensor matrix is required to fully describe the stiffness [50]. The stress and strain are related by the elastic stiffness matrix F:

$$\sigma_{ij} = \sum_{k=1}^{3} \sum_{l=1}^{3} F_{ijkl} \cdot \varepsilon_{kl} \,, \tag{1.4}$$

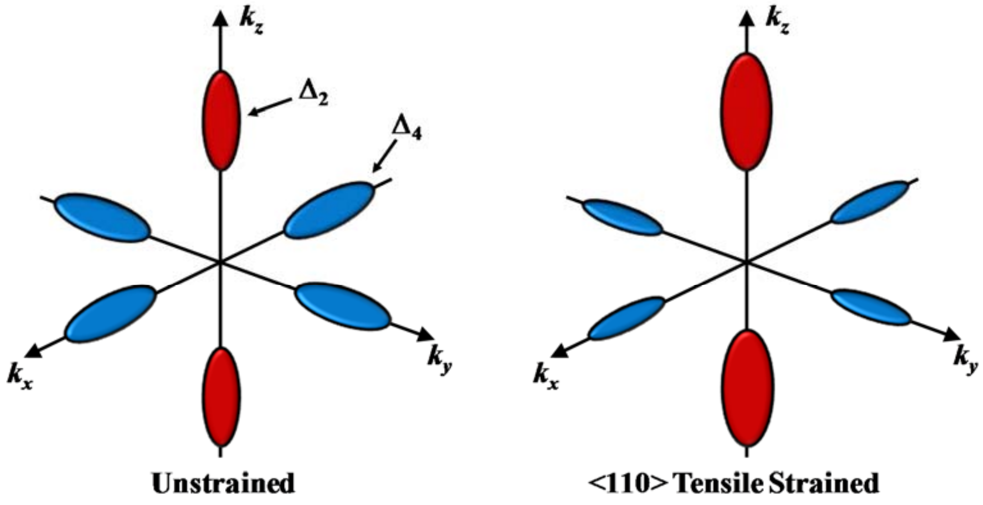
or, equivalently by the inverse compliance matrix S:

$$\varepsilon_{ij} = \sum_{k=1}^{3} \sum_{l=1}^{3} S_{ijkl} \cdot \sigma_{kl} \,, \tag{1.5}$$

where k and l are integers from 1 to 3.

Strain is introduced into the device channel preferably by applying uniaxial stress, as mentioned in Section 1.2. In Si, there are six degenerate valleys in the conduction band, with the minimum energy located near the X point in the Brillouin zone, and these valleys can be shifted and split by applied external stress [3], [51], as shown in Fig. 1.5(a). For example, <110> longitudinal tensile stress shifts the two-fold degenerate Δ_2 valleys down and four-fold degenerate Δ_4 valleys up, resulting in electrons repopulating from the Δ_4 valleys to the Δ_2 valleys. As the conductivity effective mass in the Δ_2 valleys is smaller as compared to that in the Δ_4 valleys, the repopulation of electrons into the Δ_2 valleys causes the electron mobility to increase [3]. Moreover, in a strained Si MOSFET channel, the dominant scattering mechanisms are inter-valley phonon scattering [52] and surface roughness scattering [53]. Due to the splitting of the six-fold degenerate conduction band valleys, the inter-valley scattering rate becomes lower due to the smaller density of states [51], which also results in higher mobility.

(a) Si Conduction Band Valleys in *k* Space



(b) Si Valence Band Structure

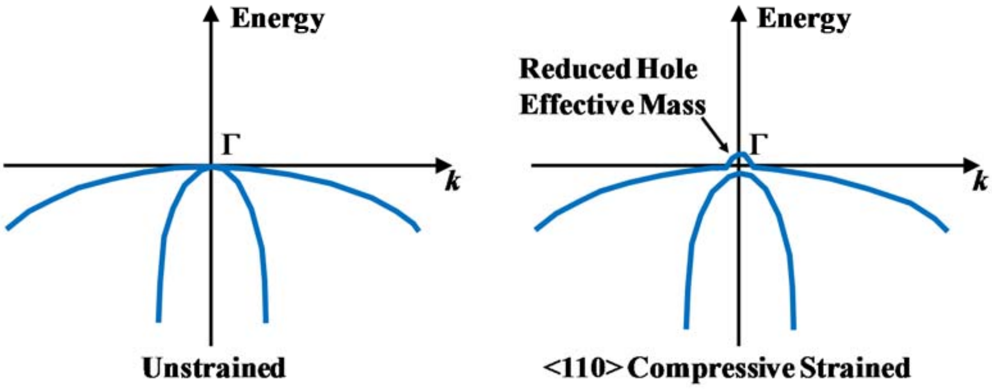


Fig. 1.5. (a) Si conduction band valleys in *k* space change under <110> tensile stress for nMOSFETs, leading to preferential electron population in the Δ_2 valleys. (b) Schematics showing how the simplified valence band structure of Si changes under <110> compressive stress. The energy dispersion at the valence band maxima is modified by the stress, leading to a reduced hole effective mass.

Fig. 1.6 shows the enhancement in effective electron mobility (μ_e) versus strain obtained by simulation [54] for (001) nMOSFETs with various channel orientations (i.e. source-to-drain direction) and tensile strains: <110> channel direction with uniaxial <110> longitudinal strain ($\varepsilon_{//}$), <100> channel direction with uniaxial <100> $\varepsilon_{//}$, and <110> channel direction with biaxial strain. Under low strain (< 0.5%), biaxial strain causes the largest enhancement [54]. However, when the strain is larger than

0.5%, the enhancements for <110>-oriented nMOSFETs under biaxial strain and <100>-oriented nMOSFETs under <100> uniaxial $\varepsilon_{//}$ saturate, as most of the electrons are already located in the lower-energy Δ_2 valleys at moderate strain levels and additional strain does not further reduce the average effective mass [3]. In contrast, the enhancement for <110>-oriented nMOSFETs under <110> uniaxial $\varepsilon_{//}$ increases significantly up to 1% strain. This is due to smaller subband splitting under <110> uniaxial strain than that under <100> uniaxial strain and biaxial strain of the same magnitude, resulting in electron repopulation up to higher levels of strain [54]. In addition, the Δ_2 subband warping under <110> uniaxial strain allows further decrease in average effective mass [3]. The experimental data reported by Suthram *et al.* [55] confirm this trend of electron mobility enhancement for <110> uniaxial strain.

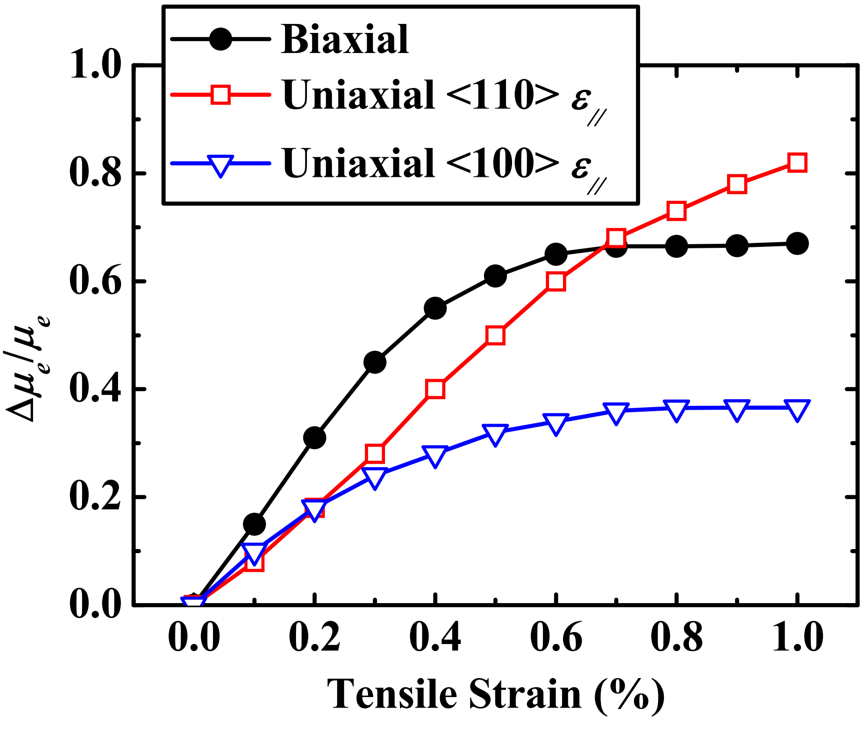


Fig. 1.6. Simulated effective electron mobility (μ_e) enhancements for (001) nMOSFETs with various channel orientations and tensile strains: <110> channel direction with uniaxial <110> longitudinal strain ($\varepsilon_{//}$), <100> channel direction with uniaxial <100> $\varepsilon_{//}$, and <110> channel direction with biaxial strain.[54].

For pMOSFETs, the valence band maxima in Si is located at the Γ point, where the heavy hole and light hole bands are degenerate [3],[49]. When applying <110> uniaxial compressive stress, which was calculated theoretically to have the largest hole mobility enhancement, the degeneracy is lifted and band warping occurs, as shown in Fig. 1.5(b). The band warping induces a reduction in hole effective mass, which is the dominant factor for hole mobility enhancement in Si pMOSFETs under uniaxial stress [3],[56]. Fig. 1.7 [12] shows effective hole mobility enhancement versus stress for pMOSFETs with various surface and channel orientations and stresses: (001) surface and <110> channel orientation with uniaxial compressive <110> longitudinal stress ($\sigma_{//}$), (110) surface and <$\bar{1}$10> channel orientation with uniaxial compressive <$\bar{1}$10> $\sigma_{//}$, and (001) surface and <110> channel orientation with tensile biaxial stress. The schematics in Fig. 1.7(a) illustrate the orientations of the surface, channel, and stress. Experimental data for uniaxial compressive stress from Wang *et al.* [57] and Thompson *et al.* [11] and biaxial tensile stress from Rim *et al.* [58] are also shown. For a wafer with (001) surface orientation, uniaxial compressive <110> $\sigma_{//}$ is more effective than tensile biaxial stress in enhancing effective hole mobility in <110>-oriented pMOSFETs. The maximum predicted Si effective hole mobility enhancement from stress is ~2 times for pMOSFETs with (001) surface, <110> channel, and biaxial tensile stress. For uniaxial stress, the maximum Si effective hole mobility enhancement is larger (~4 times) for pMOSFETs with (001) surface, <110> channel, and uniaxial compressive <110> $\sigma_{//}$ than for pMOSFETs with (110) surface, <$\bar{1}$10> channel, and uniaxial compressive <$\bar{1}$10> $\sigma_{//}$ (~2 times), due to the higher density of states in the top band for wafer with (001) surface under <110> compressive stress [12].

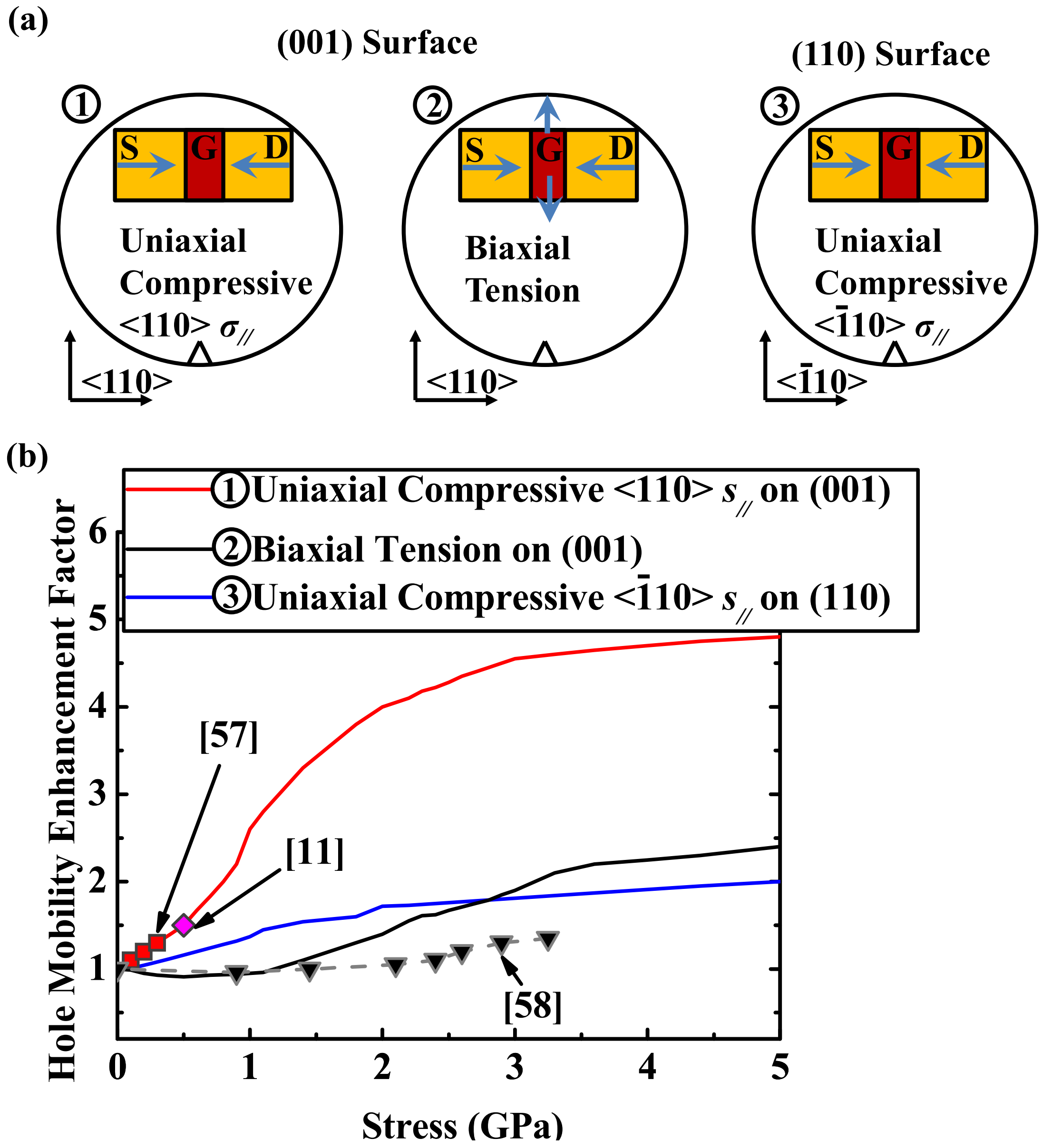


Fig. 1.7. (a) Schematics illustrate the orientations of the surface, channel, and stress of the strained pMOSFETs. (b) Calculated and experimental data for hole mobility enhancement versus stress, under uniaxial longitudinal compressive and biaxial tensile stress. The maximum predicted hole mobility enhancement is ~4 times for <110>-oriented pMOSFETs with uniaxial compressive <110> $\sigma_{//}$ on (001) surface wafer, and ~2 times for <110>-oriented pMOSFETs under biaxial tensile stress on (001) surface wafer and for <$\bar{1}$10>-oriented pMOSFETs under uniaxial compressive <$\bar{1}$10> $\sigma_{//}$ on (110) surface wafer [12].

On the other hand, piezoresistance relates the stress and electronic properties directly [59]:

$$\frac{\Delta\rho_m}{\rho}=\sum_{n=1}^{6}\pi_{mn}\cdot\sigma_n\ , \tag{1.6}$$

where ρ is the resistivity, π_{mn} is the component of the piezoresistance tensor, and σ_n is the component of the stress tensor. m and n are integers. Smith [60] reported the first measurement of piezoresistance coefficients of Si in 1954, in which Bridgman's tensor notation [61] was applied in defining the piezoresistance coefficients and geometry of the test configurations, as shown in Fig. 1.8. In Si, the stress is expected to change the number of charge carriers, which leads to a change in resistivity [60].

By considering the crystal symmetry, the piezoresistive tensor of p-type Si is characterized by Smith [60]:

$$\begin{pmatrix} \Delta\rho_{11}/\rho \\ \Delta\rho_{22}/\rho \\ \Delta\rho_{33}/\rho \\ \Delta\rho_{23}/\rho \\ \Delta\rho_{13}/\rho \\ \Delta\rho_{12}/\rho \end{pmatrix} = \begin{pmatrix} \pi_{11} & \pi_{12} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{11} & \pi_{12} & 0 & 0 & 0 \\ \pi_{12} & \pi_{12} & \pi_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & \pi_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & \pi_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & \pi_{44} \end{pmatrix} \begin{pmatrix} \sigma_{11} \\ \sigma_{22} \\ \sigma_{33} \\ \sigma_{23} \\ \sigma_{13} \\ \sigma_{12} \end{pmatrix}$$

$$= \begin{pmatrix} 6.6 & -1.1 & -1.1 & 0 & 0 & 0 \\ -1.1 & 6.6 & -1.1 & 0 & 0 & 0 \\ -1.1 & -1.1 & 6.6 & 0 & 0 & 0 \\ 0 & 0 & 0 & 138.1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 138.1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 138.1 \end{pmatrix} \begin{pmatrix} \sigma_{11} \\ \sigma_{22} \\ \sigma_{33} \\ \sigma_{23} \\ \sigma_{13} \\ \sigma_{12} \end{pmatrix} \times 10^{-11}\ \mathrm{Pa}^{-1}. \tag{1.7}$$

The piezoresistance coefficients for n- and p-type Si are summarized and compared in Table 1.1, which results in different beneficial stress for n- and p-channel MOSFETs, as shown in Fig. 1.9.

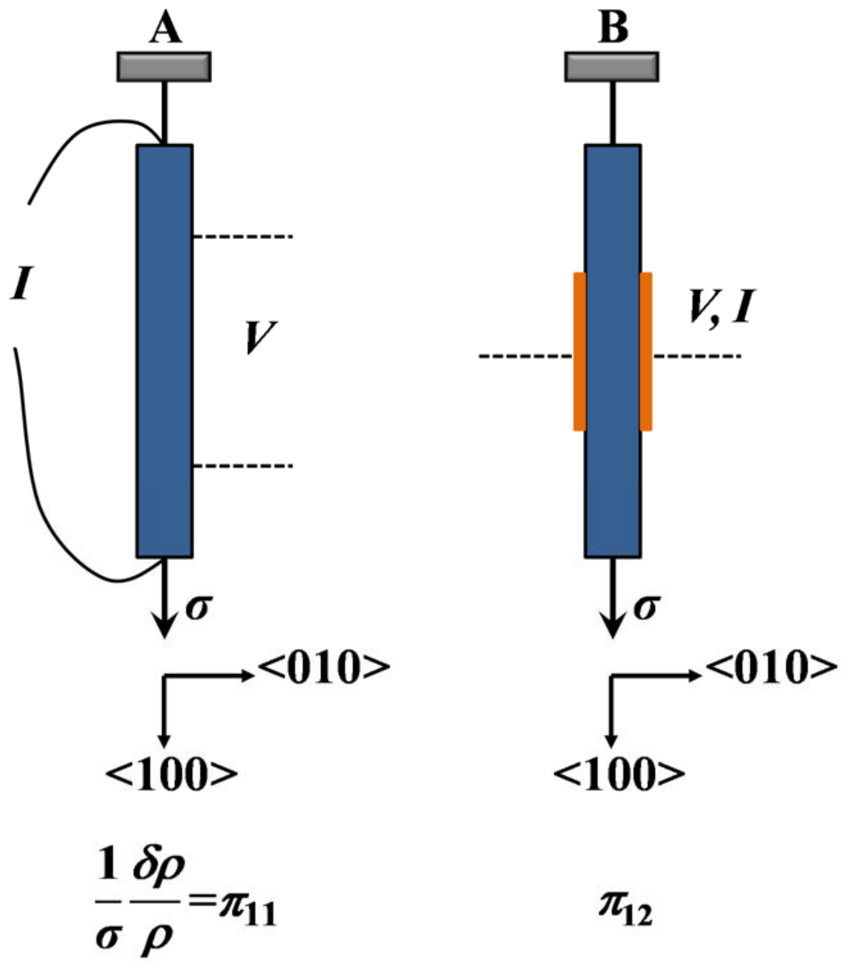


Fig. 1.8. Schematics for Smith's test configurations. Configuration A measured longitudinal piezoresistance coefficient, while configuration B provided transverse piezoresistance coefficient. Voltage drops between the electrodes (dotted lines) were measured while uniaxial tensile stress, σ, was applied to the test sample by hanging a weight [60].

Table 1.1. Piezoresistance coefficients of Si at room temperature [60].

Material	**n-type Si**	**p-type Si**
ρ (Ω-cm)	**11.7**	**7.8**
π_{11} (10^{-11} Pa^{-1})	**-102.2**	**6.6**
π_{12} (10^{-11} Pa^{-1})	**53.4**	**-1.1**
π_{44} (10^{-11} Pa^{-1})	**-13.6**	**138.1**

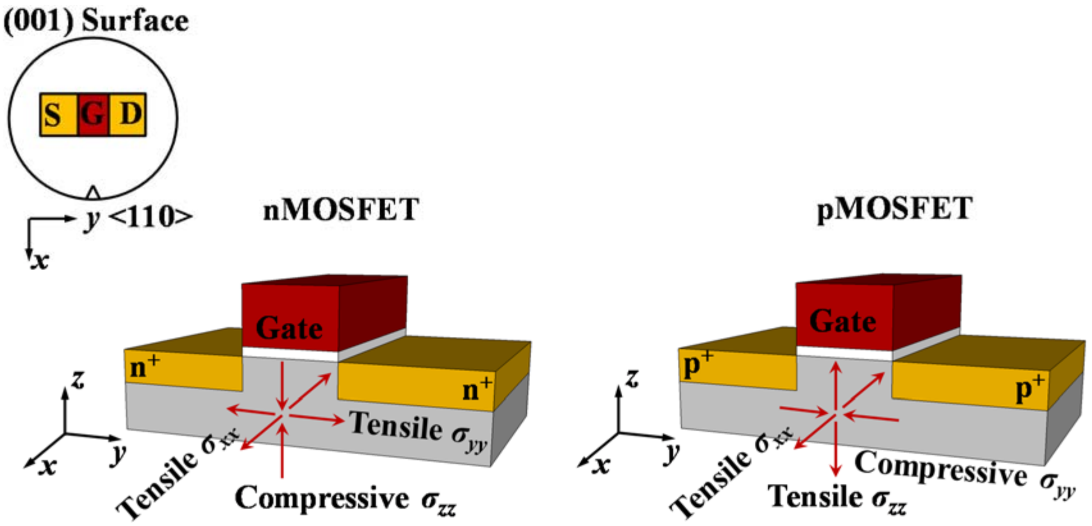


Fig. 1.9. Beneficial stress for n- and p-channel MOSFETs, with (001) surface and <110> channel orientation. In the source-to-drain direction, tensile stress is beneficial for nMOSFET while compressive stress is beneficial for pMOSFET.

The piezoresistance coefficients determined by Smith was for relatively lightly doped Si with resistivity ranging from 1.5 to 22.7 Ω-cm [60]. For wafers with doping levels several orders of magnitude higher than those in Smith's measurement, lower piezoresistance coefficients would be obtained [48].

Nevertheless, the piezoresistance coefficients give us a straightforward idea about how much drive current enhancement can be achieved under a particular stress. Therefore, it has been used to predict and understand strain-enhanced electron and hole mobilities [12],[50].

The measured piezoresistance coefficients for longitudinal compression in different channel directions are shown in Fig. 1.10 for Si pMOSFETs on (110) and (001) wafers. For both surface orientations, the piezoresistance coefficient is larger for pMOSFETs with <110> channel than for pMOSFETs with <100> channel, as the top subband that the holes repopulate into when under <110> or <100> compression has a smaller hole effective mass for <110> compression than for <100> compression [12]. Thus, longitudinal compressive stress is more effective for enhancing hole mobility in

<110>-oriented pMOSFETs than in <100>-oriented pMOSFETs. Therefore, a <110> channel direction is primarily used in strained Si pMOSFETs [62],[63]. On the other hand, a higher piezoresistance coefficient for longitudinal compression is observed for <110>-oriented pMOSFETs on a (001) wafer than for <$\bar{1}$10>-oriented pMOSFETs on a (110) wafer. This matches the larger predicted maximum hole mobility enhancement for <110>-oriented pMOSFETs under longitudinal <110> compression on (001) wafer compared to that for <$\bar{1}$10>-oriented pMOSFETs under longitudinal <$\bar{1}$10> compression on (110) wafer, as shown in Fig. 1.7.

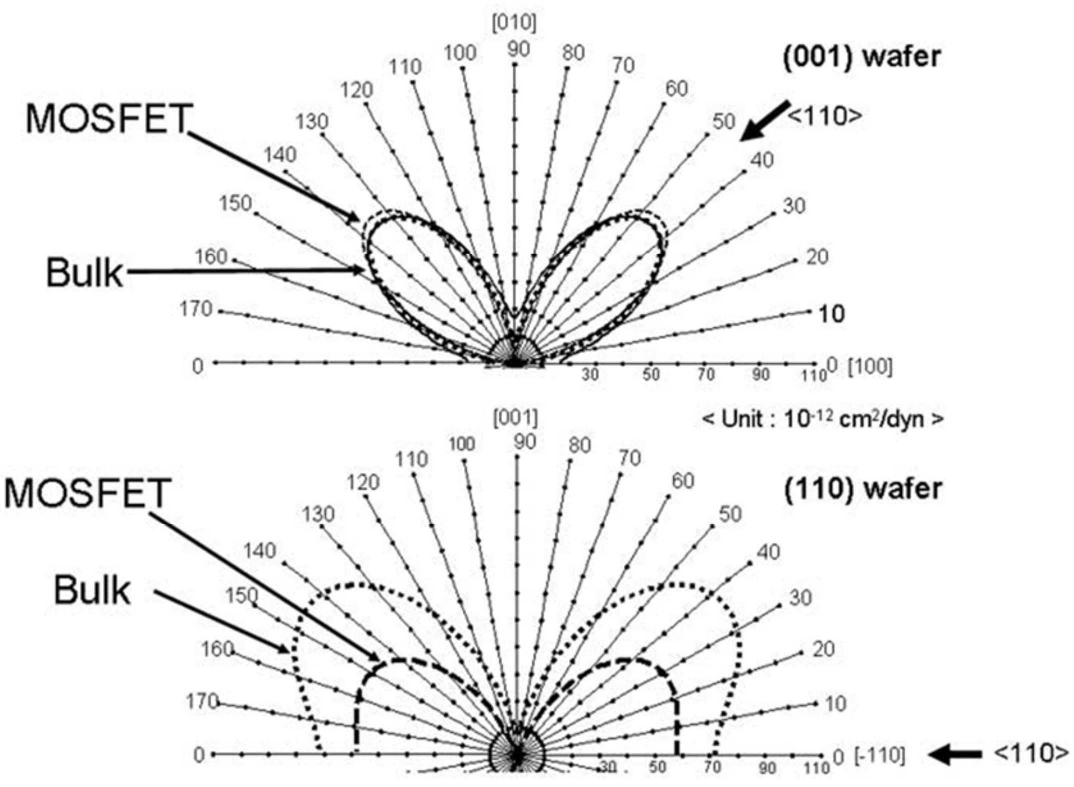


Fig. 1.10. Measured longitudinal piezoresistance coefficients of bulk p-type Si and Si pMOSFET versus channel direction for (100) and (110) wafers [12].

1.4 Strain Engineering for Advanced Transistor Architectures

In order to aggressively scale L_G of MOSFETs, SCEs need to be effectively suppressed. With the introduction of high-κ dielectrics and a novel doping profile (e.g. lightly doped drain and halo doping), the scaling limit for planar MOSFETs has been extended to ~20 nm [3],[64]. To further scale down the transistor dimensions while maintaining good performance, advanced device structures such as ultra-thin-body field-effect transistors (UTB-FETs) [Fig. 1.11(a)] and multiple-gate or fin field-effect transistors (FinFETs) [Fig. 1.11(b)] are required at sub-20 nm technology nodes. To enhance the performance of such structures, methods for introducing strain in the channel have to be developed for UTB-FETs and FinFETs.

1.4.1 Strain Engineering for UTB-FET

The UTB-FET structure relies on an ultra-thin body that is typically less than a third of L_G to suppress SCEs [65]-[68]. A lightly doped channel can be used in UTB-FETs to achieve higher mobility, and to alleviate the issue of variability of device parameters such as threshold voltage due to random dopant fluctuation [68]-[73]. UTB-FETs can be fabricated on ultra-thin (UT) silicon-on-insulator (SOI) substrates [74]-[75]. To combine their scaling advantages with strain-induced mobility enhancements, stress has recently been applied to SOI devices [76]-[81] and UTB-FETs [82]-[86]. Carrier mobility enhancement for n- and p-channel UTB-FETs under small uniaxial and biaxial stress was reported by Uchida *et al.* in 2004 [80]. Similar enhancement factors were observed between UTB-FETs and planar MOSFETs under low uniaxial stress [80].

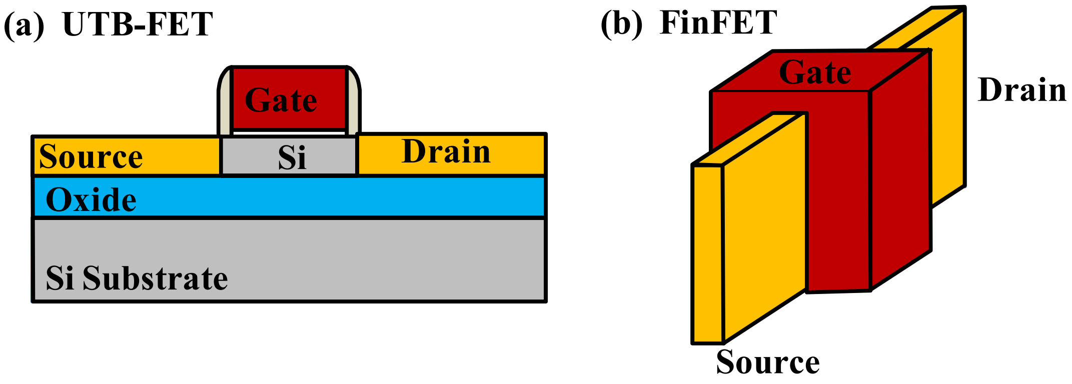


Fig. 1.11. Schematics of (a) an ultra-thin-body field-effect transistor (UTB-FET) and (b) a fin field-effect transistor (FinFET).

Under large uniaxial stress, higher enhancement was observed for p-channel UTB-FETs than for p-channel planar MOSFETs by simulation [87]. At low stress, the hole mobility in (100)-oriented pMOSFETs is enhanced mainly by band warping-induced effective mass lowering, and the effect is the same for UTB-FETs and planar MOSFETs [87]. However, at high stress, subband splitting, which induces the phonon-scattering rate reduction, plays the main role [3]. Due to the extra subband splitting resulting from the additional geometrical confinement in UTB-FETs, hole mobility enhancement at high stress is larger compared to that of planar MOSFETs [3],[87].

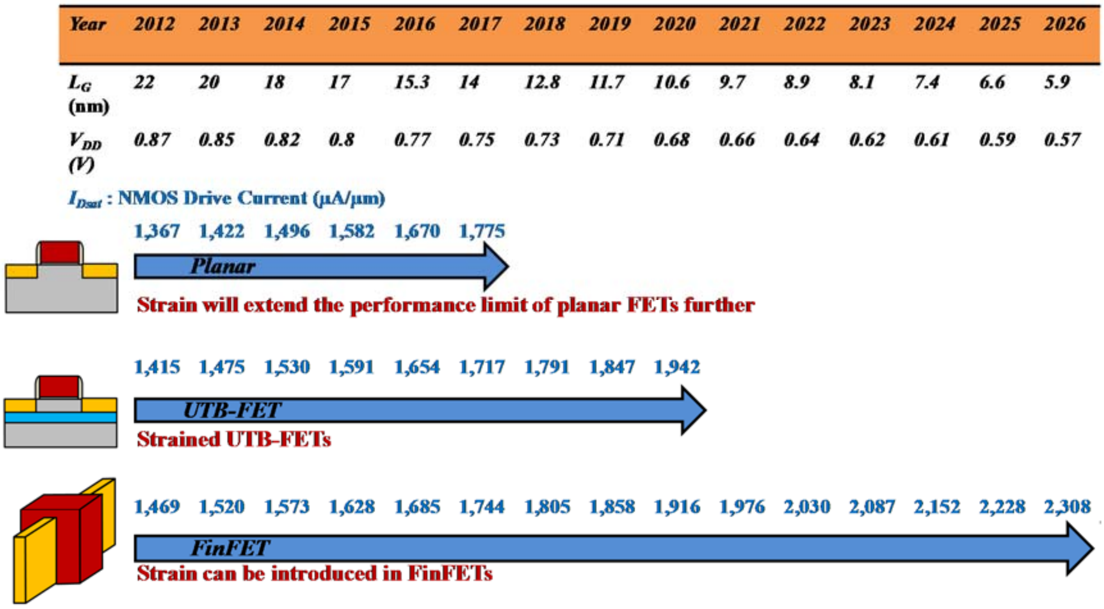
1.4.2 Strain Engineering for FinFET

Due to lateral penetration of the electric field from the drain into the channel, it is impractical to scale UTB-FETs to the sub-10-nm regime [3],[88],[89]. To improve gate control, FinFETs or multi-gate transistors which exhibit excellent control of SCEs, have been adopted by the semiconductor industry starting at the 22 nm technology node [90]-[104]. High-stress SiN liner stressor has been adopted in the manufacturing of integrated circuits based on planar transistors. In FinFETs, significant I_{Dsat} enhancement can also be achieved using SiN liner stressor [99]-[101]. In p-channel

FinFETs, DLC liner stressor has been demonstrated to significantly increase I_{Dsat} [102],[105]. S/D stressors have also been extensively studied for strain engineering in FinFETs. SiGe [106],[107] and Si:C [98],[100],[108],[109] S/D stressors have been reported to significantly enhance the drive currents of p- and n-channel FinFETs, respectively.

The difference between top and side-wall transport in FinFETs was studied by Irisawa *et al.* [110]-[112], who also proposed the optimal strain configurations for both n- and p-channel FinFETs. For FinFETs with large fin width W_{fin} (> 20 nm), the mobility enhancement from strain is similar to that for planar transistors with the same orientation, whereas for narrow FinFETs with $W_{fin} < 20$ nm, carrier confinement due to scaled device geometry becomes significant, resulting in a strong subband modulation and an increase in the density of states (DOS) in the ground-state subband [3],[87],[113]. As a result, the amount of carriers that can be affected by the strain increases, which leads to a higher enhancement factor in FinFETs with narrow W_{fin} [3],[87].

Strained Si technology could provide performance improvement even for MOSFETs operating in the ballistic regime, as shown by a theoretical study [114]. The strain-induced reduction of carrier effective mass leads to higher source carrier injection velocity, resulting in higher drive current in ballistic transistors [3],[114]. This ensures the scalability of strain technology. Although planar MOSFETs will eventually be phased out from the most advanced logic technology nodes, strain will push the performance limit further, as shown in Fig. 1.12. By combining strain-



Year	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
L_G (nm)	22	20	18	17	15.3	14	12.8	11.7	10.6	9.7	8.9	8.1	7.4	6.6	5.9
V_{DD} (V)	0.87	0.85	0.82	0.8	0.77	0.75	0.73	0.71	0.68	0.66	0.64	0.62	0.61	0.59	0.57

I_{Dsat} : NMOS Drive Current (µA/µm)

	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
Planar	1,367	1,422	1,496	1,582	1,670	1,775									
UTB-FET	1,415	1,475	1,530	1,591	1,654	1,717	1,791	1,847	1,942						
FinFET	1,469	1,520	1,573	1,628	1,685	1,744	1,805	1,858	1,916	1,976	2,030	2,087	2,152	2,228	2,308

Fig. 1.12. The 2012 update for the International Technology Roadmap for Semiconductors (ITRS) [115] projected the values of I_{Dsat} for various transistor structures from years 2012 through 2026. Strain engineering is applicable to non-classical MOSFETs such as UTB-FETs and FinFETs.

induced mobility enhancement and scaling advantages, UTB-FETs and FinFETs will continue the trend of aggressive scaling beyond year 2026, while maintaining and improving circuit performance.

1.5 Objective of Dissertation

The objective of this research is to develop and demonstrate novel strain engineering techniques in advanced Si transistors, such as nanoscale UTB-FETs and FinFETs. The need for improved transistor performance with different strain engineering technologies motivates this research effort. This thesis work provides options of strain engineering for enhancing the performance of advanced transistors at the 20-nm technology node and beyond.

1.6 Thesis Organization

The key results of this thesis are documented in the following 5 chapters.

In Chapter 2, we report a novel way of introducing strain in ultra-thin body and buried-oxide (UTBB) SOI structures by implantation of Ge ions (Ge^+) followed by crystallization to form localized SiGe regions underneath the buried oxide (BOX). Traditional means of inducing strain in the transistor channel, such as lattice-mismatched S/D stressors, would have reduced impact in ultra-thin-body transistors compared to bulk planar transistors [86],[116],[117]. New ways of strain engineering are therefore needed. Localized SiGe regions under the BOX result in local deformation and very high compressive stress in the ultra-thin Si layer. Detailed transmission electron microscopy (TEM) characterization and nano-beam diffraction (NBD) were used to analyze the strain distribution in the ultra-thin Si layer. By measuring the shifts of the peaks in the diffraction pattern in the strained region relative to those acquired in a reference unstrained region, the lattice strain in the strained region in the two directions perpendicular to the electron beam can be obtained [118]-[121]. Details of the process development for fabricating n-channel UTB-FETs (nUTB-FETs) with the under-the-BOX SiGe technique, as well as the drive current enhancement for the nUTB-FET with under-the-BOX SiGe as compared to the control nUTB-FET, will be discussed.

Chapter 3 explores a new concept for strain engineering, where a liner material is formed over a transistor and then configured to change volume post-deposition, so as to induce mechanical stress in the channel. Phase change chalcogenide materials, such as $Ge_2Sb_2Te_5$ (GST), may be used as such a liner material. When GST undergoes crystallization [i.e. phase change from the amorphous state (α-GST) to the crystalline state (c-GST)], its mass density increases and its volume is reduced. Unlike conventional liner stressors such as SiN or DLC, which rely on mechanical coupling of the intrinsic stress in the liner to the transistor channel, the mechanical stress induced by the GST contraction is exploited for strain engineering of p-channel FinFETs (p-FinFETs) in this research. Details of the process development and integration of GST liner stressor for p-FinFETs, as well as the performance enhancement induced by the GST liner stressor, will be discussed. The drain current enhancements for different fin rotations are also investigated, where the rotated FinFETs with c-GST stressor are compared with control FinFETs (without c-GST) of the same rotation.

Chapter 4 investigates (through NBD) the local strain components in the S/D and channel regions of Si FinFET structures wrapped around by a GST liner stressor. In this research work, Si FinFETs with various W_{fin} wrapped around by c-GST were fabricated, and the local strain distributions in the Si fins in the S/D regions and in the channel under the metal gate were examined using NBD. In the first part of this chapter, the physics of NBD from an assembly of atoms is discussed. In the second part of this chapter, the strain values in the <110> and <001> directions in the S/D and channel regions of the Si FinFET structures with c-GST stressor are examined. In addition, three-dimensional (3D) numerical simulations were performed to investigate the stress in the FinFET channel. The measured local strain values are also compared with the simulation results.

In Chapter 5, a new volume-change liner stressor material, ZnS-SiO_2, for strain engineering of Si n-channel FinFETs (n-FinFETs) is demonstrated. Extensive details of the process development and integration of ZnS-SiO_2 liner stressor for n-FinFETs, as well as analysis of the electrical characteristics, are presented. ZnS-SiO_2 expands during thermal anneal, and is the counterpart of GST volume-change liner stressor for strain engineering in n-FinFETs, exploiting expansion of the liner material to create large tensile stress in the channel. ZnS-SiO_2 liner was integrated on n-FinFETs with Si:C S/D stressors and Al-incorporated NiSi contacts. Incorporating Al within NiSi reduces the Schottky barrier height between NiSi and n-Si:C contact [122],[123]. The performance enhancements of n-FinFETs induced by as-deposited and expanded ZnS-SiO_2 liner stressors are compared. In addition, the performance enhancements of n-FinFETs with expanded ZnS-SiO_2 stressor at different L_G are compared, and the strain effect on carrier mobility enhancement is examined.

The contributions of this thesis and possible future directions pertaining to strained Si technology are summarized in Chapter 6.

Chapter 2

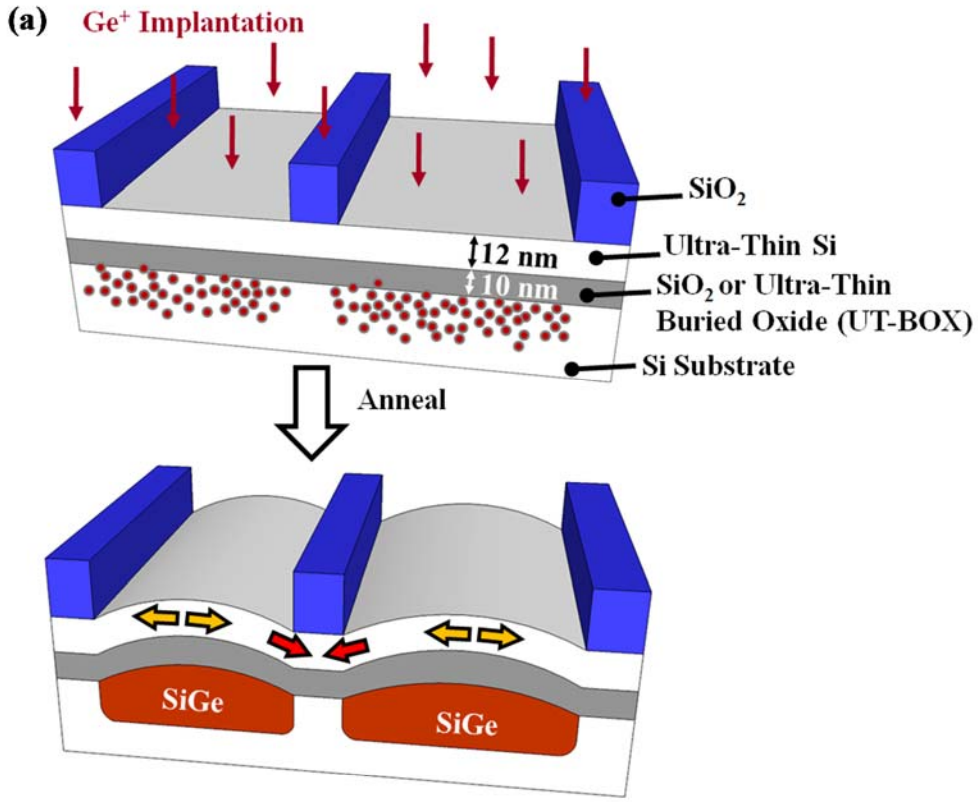
Strain Engineering of Ultra-Thin Silicon-on-Insulator Structures using Through-Buried-Oxide Ion Implantation and Crystallization

2.1 Introduction

In order to aggressively scale the gate length L_G of metal-oxide-semiconductor field-effect transistors (MOSFETs), short-channel effects (SCE) need to be effectively suppressed. Advanced device structures such as multiple-gate or fin-type field-effect transistor (FinFET) and ultra-thin body field-effect transistor (UTB-FET) are therefore required in sub-20 nm technology nodes. The UTB-FET structure relies on an ultra-thin body that is typically less than a third of L_G to suppress SCE [65]-[68]. A lightly doped channel could be used in UTB-FETs to achieve higher mobility, and to alleviate the issue of variability of device parameters such as threshold voltage due to random dopant fluctuation [68]-[73]. UTB-FETs could be fabricated on Ultra-Thin (UT) Silicon-on-Insulator (SOI) substrates [74],[75]. To realize high performance UTB-FETs, strain engineering techniques need to be used, as introduced in Chapter 1 [82]-[86]. However, traditional means of inducing strain in the transistor channel, such as lattice-mismatched source/drain (S/D) stressors, were reported to have reduced impact in ultra-thin body transistors as compared to bulk planar transistors [86],[116],[117]. Coupling between the embedded S/D stressors to the device channel is reduced as the gate pitch becomes smaller, which lowers the device mobility enhancement [116]. By optimizing structure of the stressor, such as Σ-shape S/D stressors, the channel stress could be compensated for bulk transistors. However, for UTB-FETs, as the body thickness is much thinner as compared to that of the bulk transistors, the stress loss due to the scaling of pitch would have more severe impact on UTB-FETs as compared to the bulk transistors. New ways of strain engineering are therefore needed.

In this Chapter, a novel way of introducing strain in Ultra-Thin Body and Buried Oxide (UTBB) SOI structures by implantation of germanium ions (Ge^+) followed by crystallization to form localized SiGe regions underneath the UT-buried oxide (UT-BOX) is developed. Fig. 2.1(a) illustrates the key concept of this research work. Implantation of Ge^+ into a Si substrate followed by crystallization has been reported [124]-[129], but implantation of Ge^+ through UTBB structures followed by crystallization has not been explored. Localized SiGe regions under the buried oxide (BOX) can result in local deformation of the ultra-thin Si layer.

The process development for forming localized SiGe regions underneath the UT-BOX in UTBB-SOI and numerical simulation for evaluating the stress introduced by the SiGe regions under the UT-BOX are documented in Section 2.2. In Section 2.3, Transmission Electron Microscopy (TEM) and Nano-Beam Diffraction (NBD) were used to analyze the strain distribution in the ultra-thin Si layer. Section 2.4 describes the device fabrication process flow for forming n-channel UTB-FETs (nUTB-FETs) integrated with SiGe regions under the UT-BOX developed in this work. The electrical characteristics of the fabricated devices are discussed in Section 2.5, and Section 2.6 summarizes the key results in this technology demonstration.



(b) Process flow

- **PECVD SiO_2 Hardmask Deposition**
- **Patterning using Electron-Beam Lithography**
- **Hardmask Etching and Photoresist Removal**
- **Ge^+ Implantation Through UT-BOX: Energy = 55 keV, Dose = 2×10^{16} /cm^2**
- **RTP Anneal: 900 °C for 60 s**

Fig. 2.1. (a) Three-dimensional (3D) schematic illustrating a SiO2-masked implantation of Ge ions through the UT-BOX into the Si substrate. After an anneal, SiGe regions were formed underneath the UT-BOX. The SiGe region causes localized bulging up of the UT-BOX and the overlying Si layer, leading to stress in the ultra-thin Si layer. The ultra-thin Si layer under the SiO2 hardmask is under compressive strain in the lateral direction, as indicated by the red arrows. (b) Process flow for inducing local strain in UTBB SOI by localized SiGe regions. All process steps were performed by the author except the Ge+ implantation step which was outsourced.

2.2 Fabrication Process and Stress Simulation

UTBB-SOI wafers with 12 nm of Si on 10 nm of UT-BOX were used. The process flow to form localized SiGe regions underneath the UT-BOX is depicted in Fig. 2.1(b). The UT-BOX was kept thin in order to maximize the mechanical coupling of the stress from the SiGe regions below the BOX to the ultra-thin Si layer. For the patterned samples, SiO_2 with a thickness of 50 nm was deposited using plasma-enhanced chemical vapor deposition (PECVD), and patterned using electron beam lithography (EBL). The EBL was performed as an outsourced service at the Institute of Materials Research and Engineering (IMRE). The SiO_2 layer was then etched using CHF_3-based plasma to form narrow SiO_2 lines with a line width of 50 nm, as shown in Fig. 2.2. Unpatterned samples are pieces of UTBB-SOI wafers with no SiO_2 capping. Ge^+ was then implanted with an energy of 55 keV and a dose of 2×10^{16} cm^{-2} into patterned and unpatterned samples. The Ge^+ implant energy was selected such that the projected range R_p is located underneath the ultra-thin BOX. The ion dose of 2×10^{16}

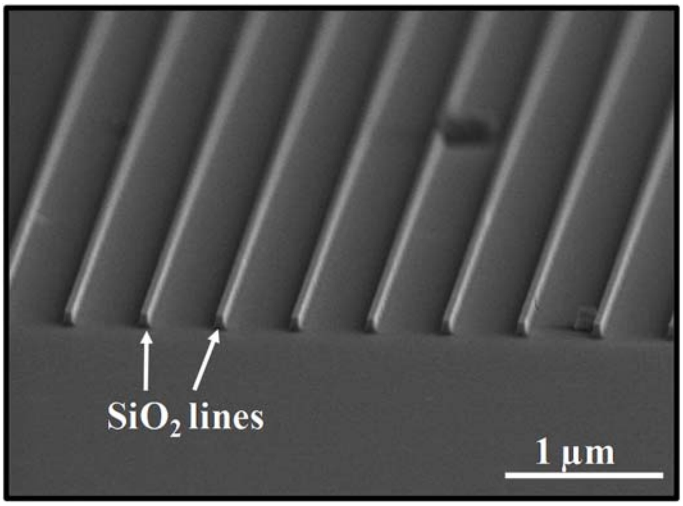


Fig. 2.2. Scanning electron microscopy (SEM) image of narrow SiO_2 lines with a line width of ~50 nm formed on UTBB-SOI wafer.

cm^{-2} leads to a Ge peak concentration of ~ 4.5 × 10^{21} cm^{-3}, as shown by the time-of-flight secondary ion mass spectrometry (TOF-SIMS) profile of Ge in UTBB-SOI [Fig. 2.3]. This corresponds to a Ge content of ~9 atomic percent (at. %). TOF-SIMS was done using positive cesium ions with an energy of 3 keV for examining the distribution of Ge. The quantification of the Ge concentration was performed with a calibration sample that received Ge^{+} implantation at a dose of 2 × 10^{16} cm^{-2} and an energy 55 keV. The sputtering time on the horizontal axis was converted to depth by measuring the crater depth and assuming a uniform sputter rate. Following Ge^{+} implant, a 900 ˚C 60 s anneal in a rapid thermal processing (RTP) tool was performed for crystallization [127]-[132]. Anneals at 850˚C for 1 or 4 hours

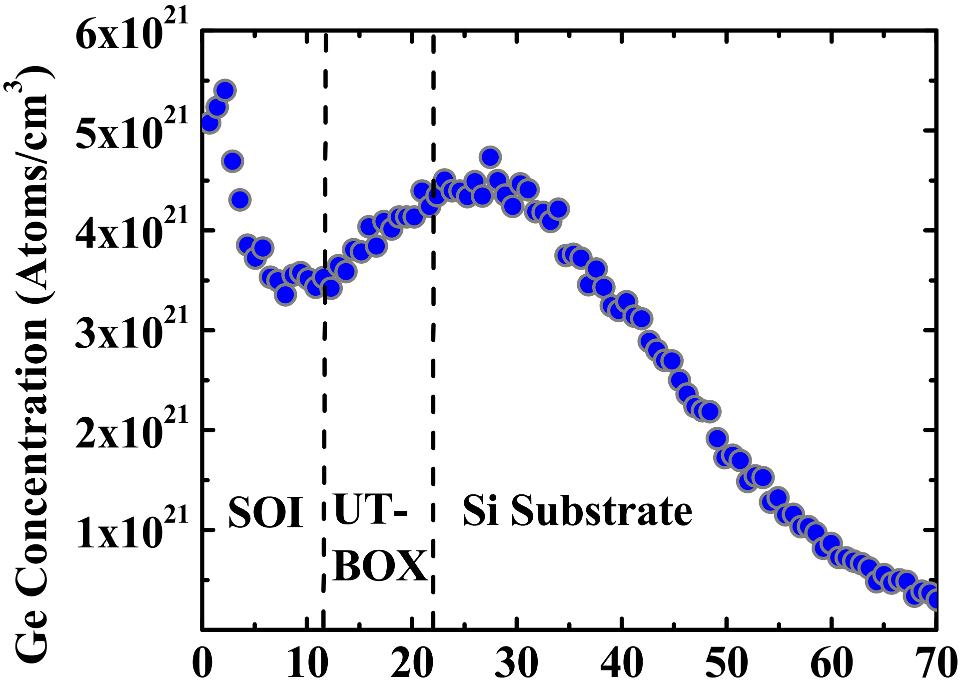


Fig. 2.3. SIMS profile shows the Ge distribution in Ge implanted UTBB-SOI, with a peak concentration of ~4.5×10^{21} cm^{-3} near the UT-BOX/Si substrate interface. The SIMS was performed as an external service job at the IMRE.

were also attempted. The anneal at 900 ˚C for 60 s was picked as it has the shortest anneal time, while being sufficient for SiGe formation.

A two-dimensional (2D) numerical simulation was performed using a simulation tool named COMSOL to investigate stress in the UTBB-SOI structure having localized under-the-BOX SiGe regions. The simulation structure and its dimensions are shown in Fig. 2.4(a). The thickness and width of the under-the-BOX SiGe regions are 30 nm and 200 nm, respectively. The distance between two adjacent SiGe regions is 50 nm, as defined by the line width of the SiO_2 pattern. Other properties of SiGe, such as a Young's modulus of 160 GPa and a Poisson's ratio of 0.279, are obtained from those of Si and Ge by linear interpolation [133]. A non-uniform finite element grid was used, with smaller grid size at regions where the stress gradient is large, such as the ultra-thin Si layer and SiGe regions. An example

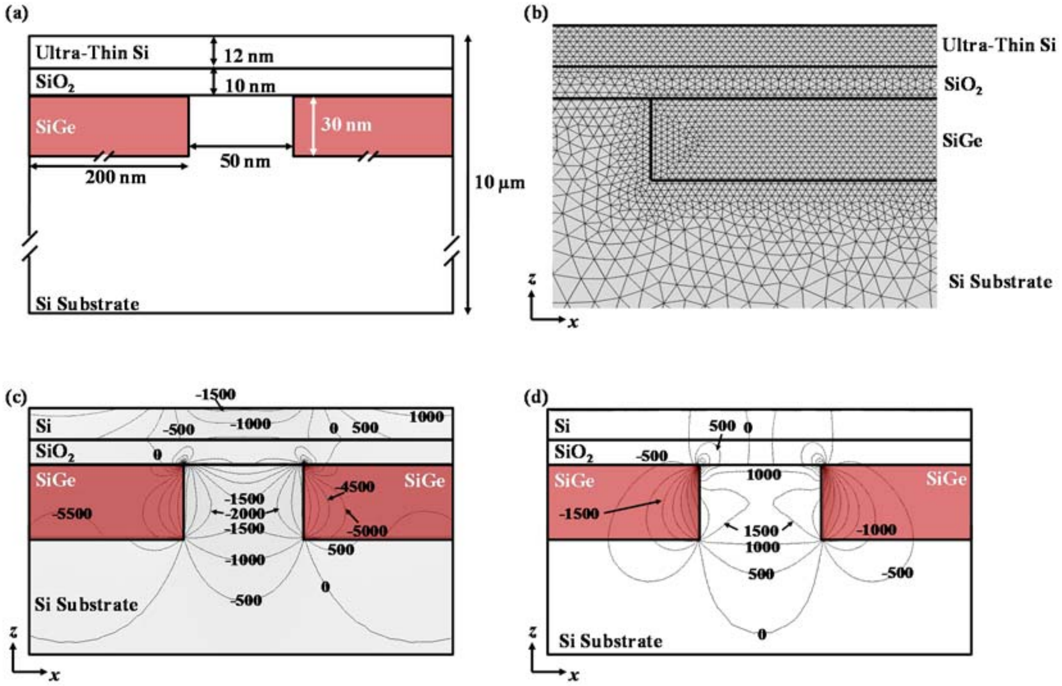


Fig. 2.4. (a) UTBB-SOI structure showing the dimensions of the ultra-thin Si layer, BOX layer, and the under-the-BOX SiGe regions. (b) Two-dimensional mesh used in a numerical simulation, showing half of the simulated structure. (c) Simulated lateral stress σ_{xx} (in MPa). The ultra-thin Si layer located above and between the SiGe regions is under lateral compressive stress. (d) Simulated vertical stress σ_{zz} (in MPa), showing that the ultra-thin Si layer is under vertical tensile stress.

of the mesh grid is shown in Fig. 2.4(b). The boundary conditions are such that the bottom and sides of the substrate, and the sides of the ultra-thin Si layer and the BOX, are rigid. The sides of the domain are assumed to have zero horizontal displacements since they are bounded by huge adjacent volumes.

Due to the introduction of additional material by the implantation process, the volume of material in the implanted region (~30 nm deep) is estimated to expand by 0.043 or 4.3%. The average Ge concentration introduced in the implanted region is ~2.15×10^{21} cm^{-3}, which is 4.3% of the atomic concentration of Si. In the simulation, the deformation of the local SiGe regions was therefore set to be 4.3% throughout the implanted region. The deformation or volume expansion of the local SiGe regions was simulated using the framework of thermoelasticity [133],[134], by setting the "thermal expansion coefficient" of the SiGe regions and the rest of the regions to be 0.043 K^{-1} and 0 K^{-1}, respectively, and increasing the temperature of the whole simulation domain by 1 K. Fig. 2.4(c) shows the simulated lateral stress σ_{xx} (in MPa) in the UTBB-SOI structure with local SiGe regions. A high compressive σ_{xx} of up to ~1.5 GPa was found in the ultra-thin Si layer with a width of 50 nm. Fig. 2.4(d) shows the simulated vertical stress σ_{zz} (in MPa). A smaller tensile stress was observed in the ultra-thin Si in the vertical direction.

2.3 TEM Characteristics and NBD Strain Anlysis

Fig. 2.5 shows the cross-sectional TEM image of an unpatterned UTBB-SOI with SiGe region underneath the BOX after anneal. A zoomed-in view of the SiGe region is shown in the inset. End of range (EOR) defect clusters were found underneath the SiGe region, at the original amorphous/crystal interface region. EOR defects were

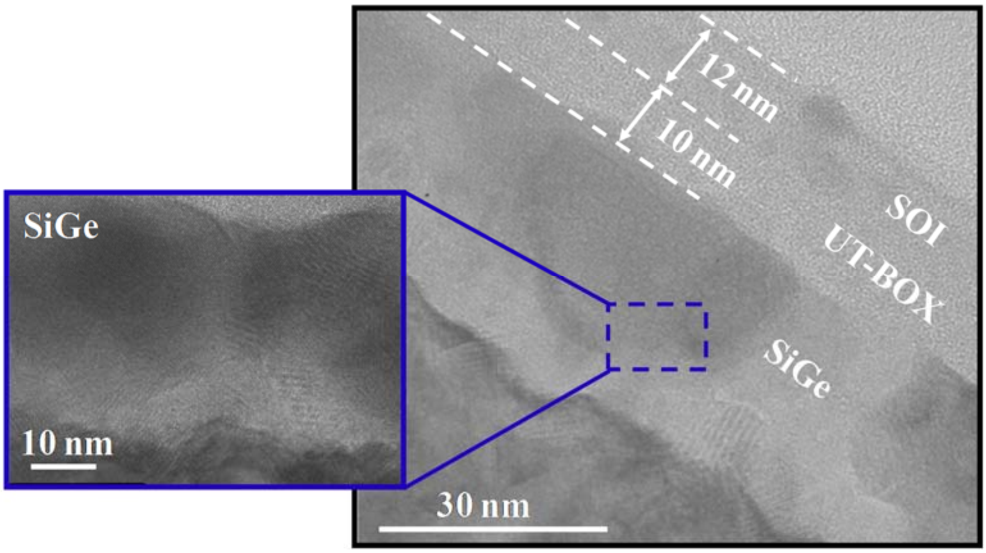


Fig. 2.5. TEM cross-section of unpatterned UTBB-SOI with SiGe regions underneath the UT-BOX. High resolution TEM shows that the SiGe region appears to be poly-crystalline. The TEM analysis was performed by Dr. ZHOU Qian of our research group.

formed during implantation, and it is very difficult to eliminate them after a high dose implantation [127]. The inset of Fig. 2.5 also shows the defective portions of the SiGe region. These defects may be misfit dislocations formed during the relief of strain in the SiGe region, which results from the re-arrangement of atoms in the amorphous/crystalline interfacial region during the re-crystallization process [126],[135].

The patterned UTBB-SOI with narrow SiO_2 lines after Ge implantation through the ultra-thin Si and UT-BOX and after anneal is shown in Fig. 2.6(a). SiGe was selectively formed underneath the UT-BOX. This results in an obvious curvature in the ultra-thin Si and UT-BOX above it. The EOR defects were observed underneath the local SiGe alloy region. The masked region and exposed region of the ultra-thin Si layer, as well as the under-the-UT-BOX SiGe region, are shown in Fig. 2.6 (b)-(d), respectively. The masked ultra-thin Si region was single crystalline [Fig. 2.6 (b)], even

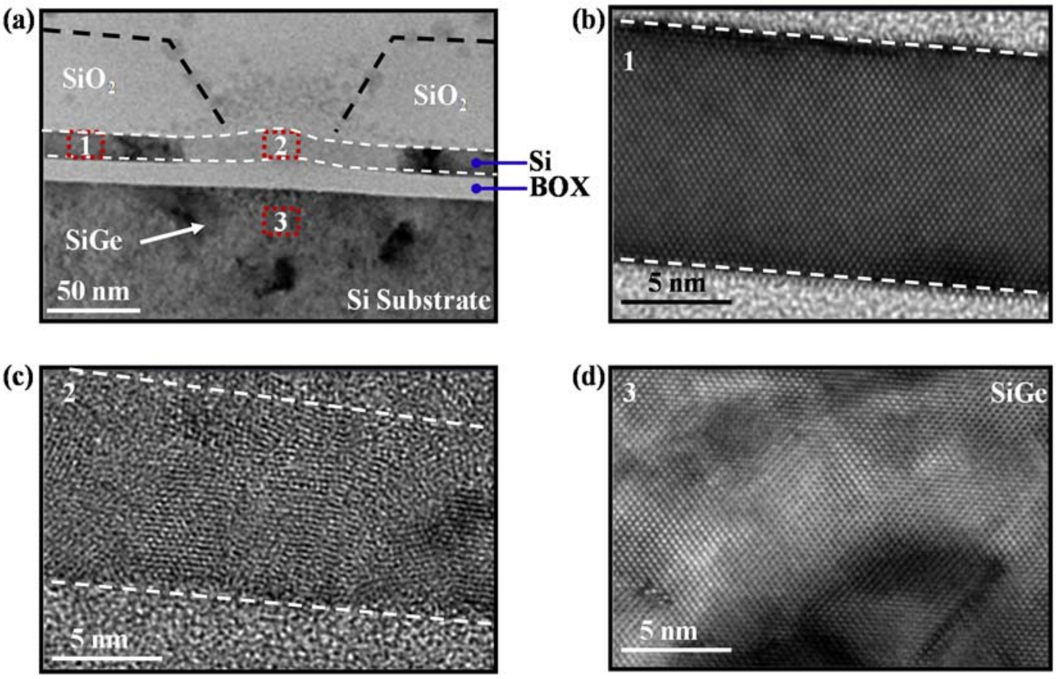


Fig. 2.6. (a) Cross-sectional TEM shows the patterned UTBB-SOI after Ge implantation through the body and UT-BOX and after 900 °C 60 s anneal. The selectively formed SiGe causes obvious curvature in the ultra-thin Si layer. High resolution TEM images show the (b) masked and (c) exposed/unmasked regions of the ultra-thin Si layer and (d) the local under-the-BOX SiGe region after Ge implant and anneal. The TEM in (c) shows that the exposed Si layer was damaged by the high-dose Ge implantation, and the Si layer is polycrystalline after the anneal. The TEM was performed as an outsourced service at the IMRE.

though the exposed or unmasked Si region was damaged by the high-dose Ge implantation. After the anneal, the exposed ultra-thin Si region became polycrystalline [Fig. 2.6 (c)].

Localized strain in the nanometer scale could be quantified by TEM based techniques, such as the NBD [118], [136]-[140]. NBD illuminates a TEM sample with a small (nanometer-sized) quasi-parallel electron beam. The small beam size selects a localized region, forming a diffraction pattern with sharp peaks at the back focal plane of an objective lens which may be used for strain analysis.

Fig. 2.7 (a) shows a TEM image of patterned UTBB-SOI with localized SiGe regions. Diffraction patterns were recorded by a 2048 × 2048 pixels CCD camera at a series of ten reference points in the Si substrate far (~1 μm) from the strained regions. The location of points 1-10 is assumed to be strain-free, i.e. the average of the <110> strain is zero. A diffraction pattern from one of the reference points or strain-free region is shown in Fig. 2.7 (b). The separation between the center *0* and a diffraction peak is directly proportional to the reciprocal of the atomic spacing in the direction from *0* to that peak. The separation between the center *0* and the (220) peak contains information on the horizontal <110> atomic spacing [141]. Fig. 2.7(c) shows the strain in the <110> direction from the ten reference points. The standard deviation of the strain values in the ten reference points can be used to estimate the accuracy of NBD. In this study, a high NBD measurement accuracy of 1.2×10^{-3} in the <110> direction was obtained [Fig. 2.7 (c)].

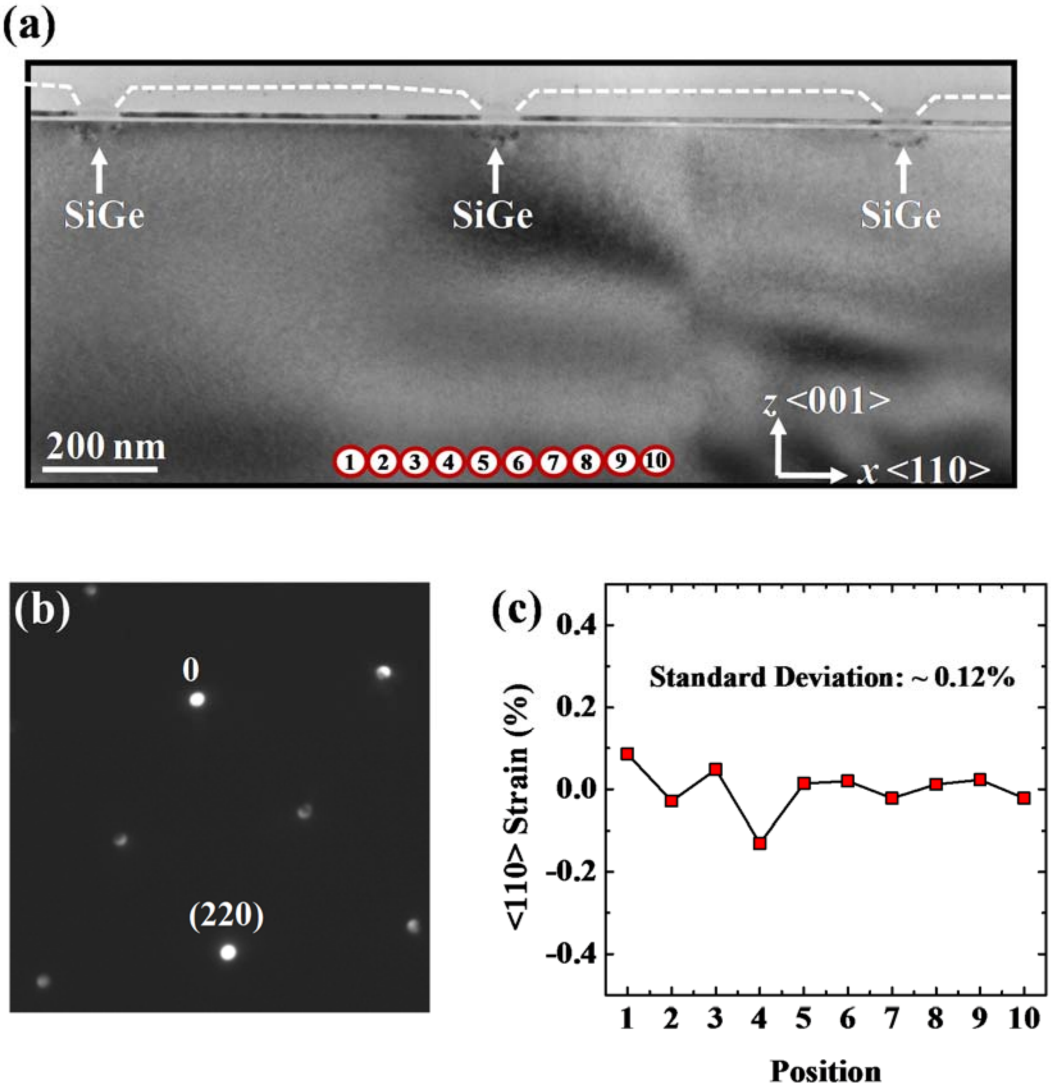


Fig. 2.7. (a) A TEM image showing a cross-sectional view of the localized SiGe regions in patterned UTBB-SOI. A series of points (labeled 1 to 10) far from the strained regions is selected to generate (b) diffraction patterns as reference using NBD. (c) Strain values at the reference points show a standard deviation of 0.12% in the <110> direction. The TEM analysis was outsourced.

NBD line scans were performed in the masked ultra-thin Si region and in the Si between two local under-the-BOX SiGe regions, as shown in the high-angle annular dark-field (HAADF) image [Fig. 2.8 (a)]. The real-time HAADF image allows accurate positioning of the electron beam. The strain values in the <110> direction at the ultra-thin Si region, which has a width of 50 nm, are shown in Fig. 2.8 (b). For strained crystals, to calculate the percentage change in the lattice constants, we employ:

$$\varepsilon_{<110>} = \frac{a_{<110>} - a_{<110>,Ref}}{a_{<110>,Ref}}, \tag{2.1}$$

where $a_{<110>}$ is the lattice constant of the strained crystal in the <110> direction. $a_{<110>,Ref}$ is the averaged lattice constants of the unstrained reference crystal [the ten reference points in Fig. 2.7(a)] in the <110> direction. Generally, the ultra-thin Si region is compressively strained, as benchmarked against the unstrained reference region deeper in the Si substrate. High average compressive strain values of -0.55% ± 0.12% and -1.2% ± 0.12% were observed at the center and edge of the ultra-thin Si region, respectively. Fig. 2.8 (c) shows a profile of the strain in the <110> direction along a vertical line in the Si substrate between the local SiGe regions.

The measured strain can be converted to stress by multiplying the Young's modulus in the <110> direction (~170 GPa) [142]. Compressive stress values of up to ~935 ± 200 MPa and ~2040 ± 200 MPa were obtained, at the center and edge of the ultra-thin Si region, respectively. The <110> stress values calculated from the NBD results are consistent with the simulated stress values σ_{xx} in Fig. 2.4 (c).

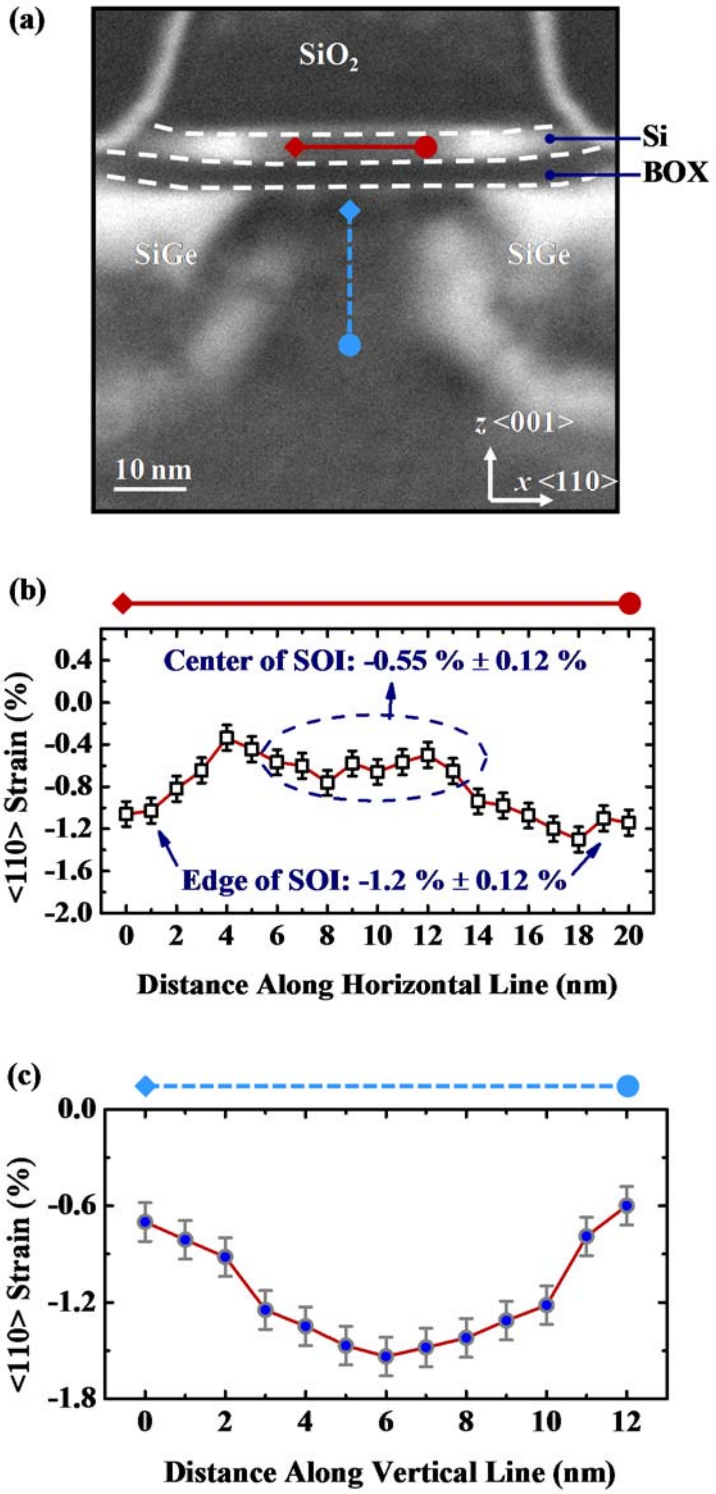


Fig. 2.8. (a) High-angle annular dark-field (HAADF) image allows accurate positioning of the electron beam. NBD line scans were performed on the ultra-thin Si layer horizontally, and on the Si substrate vertically, and the respective strain distributions in the <110> direction are shown in (b) and (c). Compressive strain of up to -0.55% and -1.2% were detected by NBD at the center and edge of an ultra-thin Si region with 50 nm width between two localized SiGe regions. The NBD analysis by Dr. DU Anyan of GLOBALFOUNDRIES is acknowledged.

2.4 Fabrication of N-Channel UTB-FET with Under-The-BOX SiGe

Un-doped UTBB-SOI substrates with 12 nm of Si on 10 nm of BOX were used for nUTB-FET fabrication. After depositing a SiO_2 hardmask with a thickness of ~50 nm, active regions were patterned using electron beam lithography (EBL). The hardmask and the ultra-thin Si layer were then etched using CHF_3-based plasma. The key process steps are summarized in Fig. 2.9, with a schematic illustrating the final device structure.

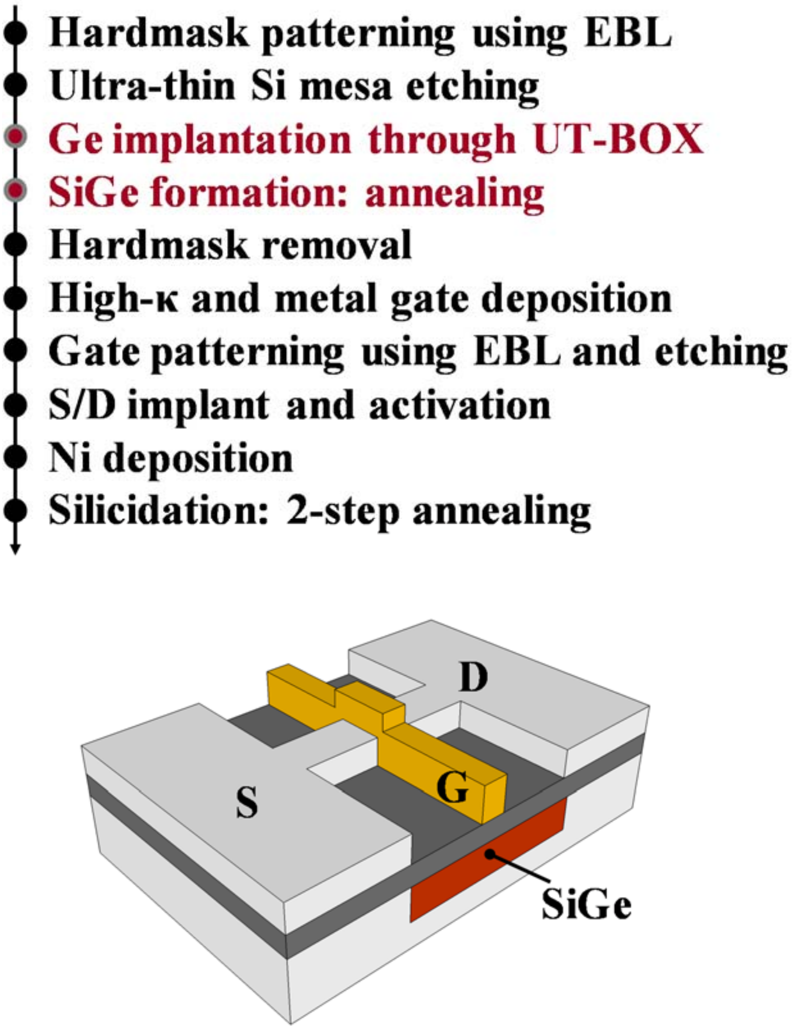


Fig. 2.9. The process flow for fabricating n-channel UTB-FETs with under-the-BOX SiGe regions. The schematic shows the final device structure.

Experimental splits were introduced after hardmask and ultra-thin Si patterning. For the strained devices, Ge^+ implantation was performed with an energy of 55 keV and a dose of 2×10^{16} cm^{-2} [Fig. 2.10 (a)], followed by thermal annealing at 900 °C for 60 s to form the SiGe regions under the UT-BOX. The SiO_2 hardmask that blocked the Ge^+ implant was then removed, as shown in Fig. 2.10 (b). Fig. 2.10(c) shows SEM image of the nUTB-FET after the under-the-BOX SiGe formation. The control nUTB-FETs did not undergo the Ge implantation.

The channel region was designed to be very narrow, with channel width W down to 20 nm [Fig. 2.11 (a)]. This maximizes the deformation caused by the under-the-BOX SiGe regions, which results in large stress in the channel. 3D simulations were performed to investigate the stress in the narrow channel with under-the-BOX SiGe. Fig. 2.11 (b) shows the distribution of simulated stress in the source-to-drain direction (σ_{yy}) in the A-A' plane, cutting along the channel from source to drain. Ultra-thin Si layer thickness of 12 nm, BOX thickness of 10 nm, W of 20 nm, and SiGe depth of 30 nm were used in the simulation. The simulation conditions are identical to those in Fig. 2.4. The zoomed-in view of the simulated σ_{yy} in the A-A' plane is shown in Fig. 2.11 (c). Very high tensile stress up to 3000 MPa in the source-to-drain direction in the channel region is observed. The simulated stress at the center of the channel as a function of the channel width is shown in Fig. 2.12. The under-the-BOX SiGe induces higher channel stress for the UTB-FETs with narrow channel width.

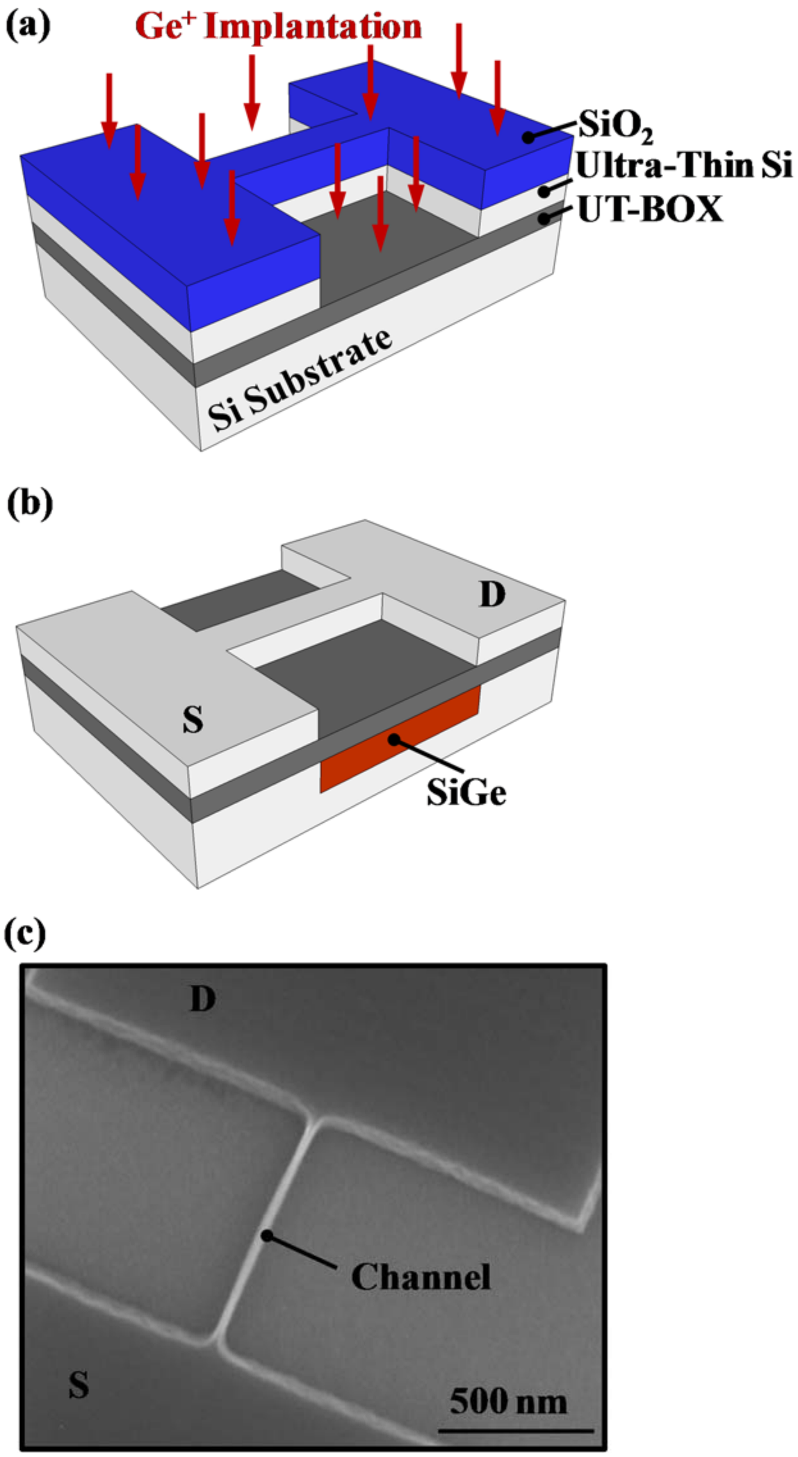


Fig. 2.10. Schematics of the UTB-FET after (a) SiO_2 hardmask patterning and ultra-thin Si etching, and (b) formation of SiGe regions under the UT-BOX. (c) SEM image of the nUTB-FET after the under-the-BOX SiGe formation.

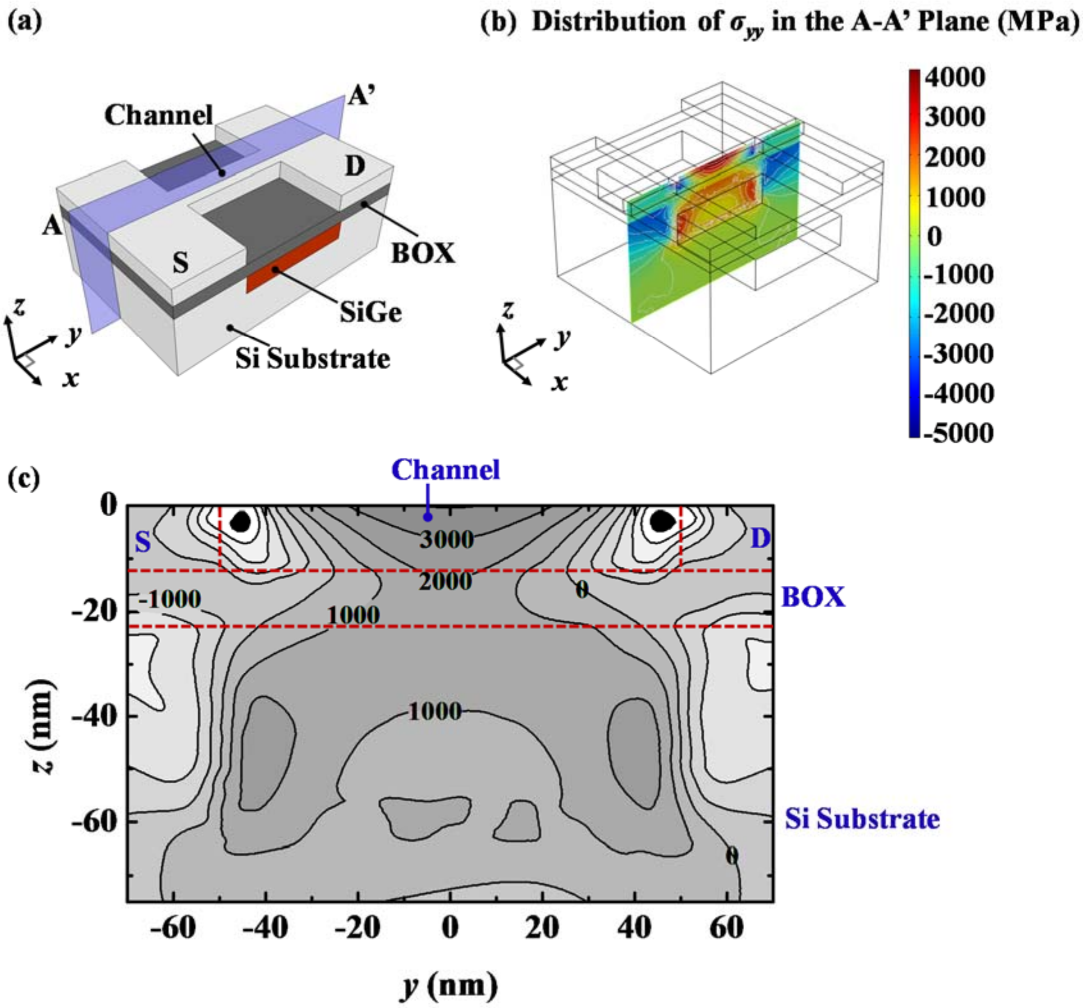


Fig. 2.11. (a) 3D schematic of a UTB-FET prior to gate stack formation, with under-the-BOX SiGe regions and narrow channel width. The source-to-drain direction is along the *y*-axis. The A-A' plane cuts along the channel from source to drain. (b) 3D finite-element simulation of stress in the *y* direction (σ_{yy}) for a UTB-FET with under-the-BOX SiGe. The scale bar for stress is shown on the right. Ultra-thin Si layer thickness of 12 nm, BOX thickness of 10 nm, channel width of 20 nm, and SiGe depth of 30 nm were used in the simulation. (c) The zoomed-in view of the simulated σ_{yy} distribution in the A-A' plane, showing that the under-the-BOX SiGe regions induce very high tensile stress in the channel.

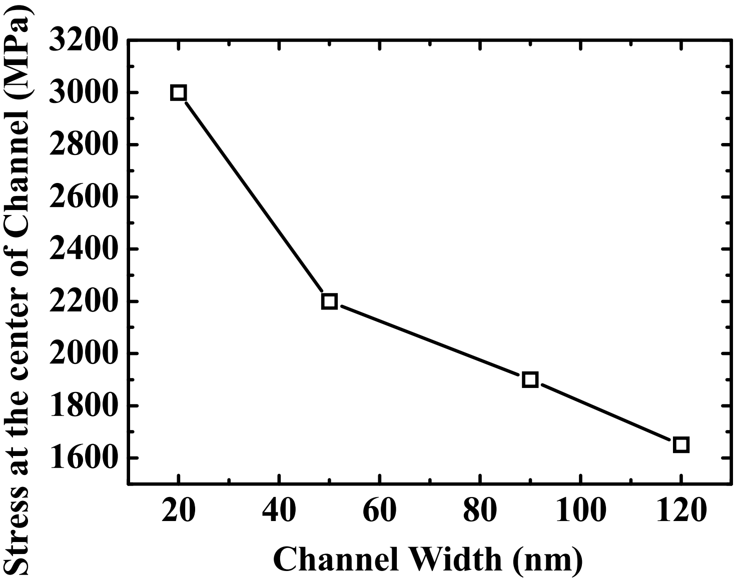


Fig. 2.12. The simulated stress at the center of the channel in UTB-FETs with under-the-BOX SiGe regions, as a function of the channel width. For narrower channel width, higher channel stress is induced by the under-the-BOX SiGe regions.

Al_2O_3 gate dielectric was deposited using atomic layer deposition (ALD), and TaN gate was deposited by sputtering. The ALD step was done by Dr. GONG Xiao of our research group. EBL (outsourced service) was used for gate patterning, followed by gate etching using chlorine-based plasma. The SEM picture in Fig. 2.13(a) shows a device with L_G of 23 nm after the gate patterning. The S/D regions were implanted

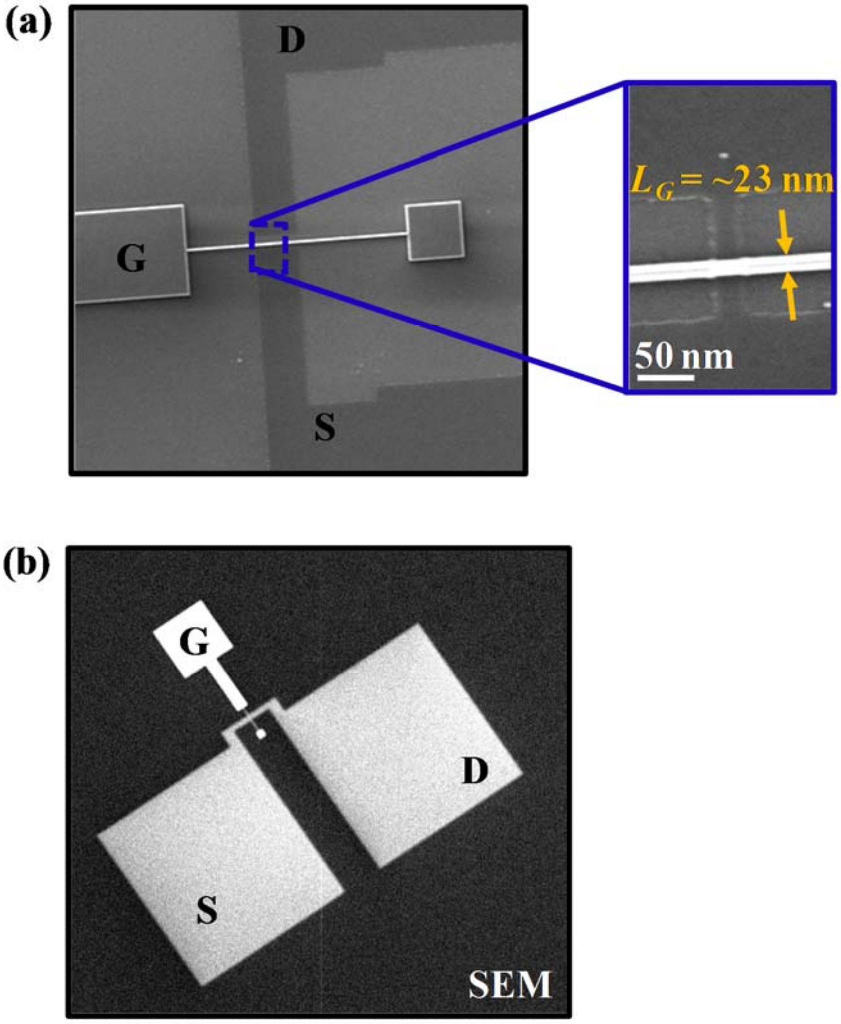


Fig. 2.13. SEM pictures of (a) a UTB-FET after gate patterning, with a zoomed-in view of the channel region (inset), and (b) a completed UTB-FET after NiSi contact formation.

with arsenic at an energy of 10 keV and a dose of 2×10^{15} cm^{-2}, followed by dopant activation. Prior to nickel (Ni) deposition, the devices underwent a standard cleaning step by dipping in hydrofluoric acid solution (HF:H_2O = 1:100) for 60 s to remove native oxide. The deposited Ni film (~7 nm thick) was annealed at 250 °C for 1 s in nitrogen ambient to form di-nickel silicide (Ni_2Si) S/D contacts. After stripping off the unreacted Ni by dipping in a sulfuric acide-peroxide solution (H_2SO_4 : H_2O_2 = 4:1) at 120 °C for 120 s, a second anneal was done at 400 °C for 10 s to form mono-nickel silicide (NiSi) S/D contacts. The two-step anneal for forming the S/D contacts is essential to prevent the in-diffusion of Ni into the channel region of the UTB-FET [143],[144]. Electrical characterization was performed by probing the gate, and NiSi S/D contacts. The SEM picture in Fig. 2.13(b) shows the completed device.

2.5 Electrical Characteristics and Discussion

Fig. 2.14(a) shows the I_D-V_G characteristics of nUTB-FETs with and without under-the-BOX SiGe regions, with L_G = 80 nm and W = 50 nm. Although both devices have similar drain-induced barrier lower (DIBL) and subthreshold swing (SS), the nUTB-FET with under-the-BOX SiGe shows a significantly higher leakage current. Comparison of the transconductance of these two devices as a function of gate voltage is shown in Fig. 2.14(b). The nUTB-FET with under-the-BOX SiGe has ~30% peak saturation transconductance enhancement over the control nUTB-FET. The I_D-V_D characteristics for the same pair of nUTB-FETs with and without under-the-BOX SiGe in Fig. 2.14, measured at a gate overdrive (V_G - V_{TH}) of 0 to 1.2 V in steps of 0.2 V, are shown in Fig. 2.15. The nUTB-FET with under-the-BOX SiGe exhibits ~18% saturation drain current (I_{Dsat}) enhancement over the control nUTB-FET at gate overdrive of 1.2 V. As the process flow is the same for these two devices except for the Ge implant and SiGe formation, the difference in I_{Dsat} is due to the stress induced by the under-the-BOX SiGe regions. Considering the high channel stress induced by the under-the-BOX SiGe regions obtained by simulation [Fig. 2.11(c)], the experimental I_{Dsat} enhancement is relatively low. By optimizing the fabrication process flow, a higher I_{Dsat} enhancement is expected.

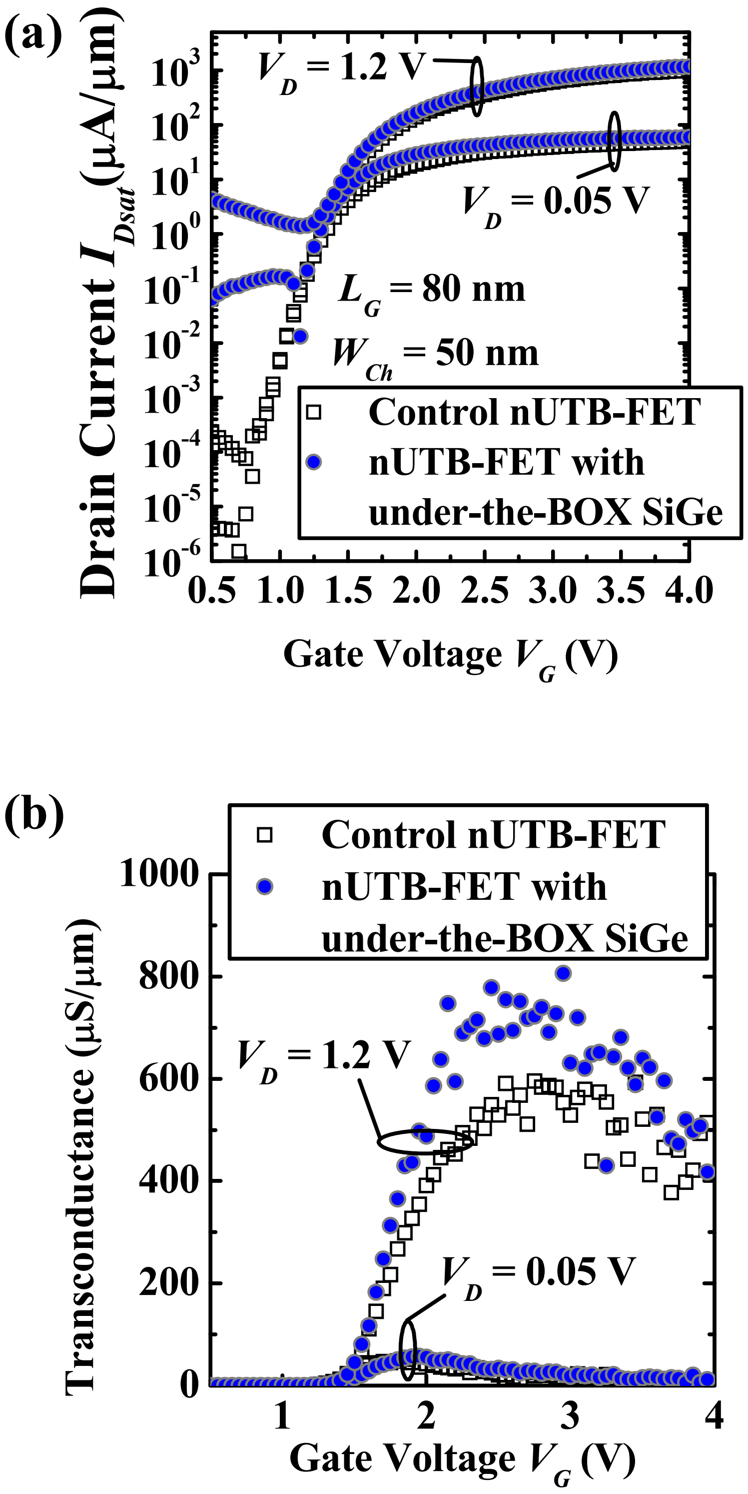


Fig. 2.14. (a) I_D-V_G and (b) transconductance characteristics of a pair of nUTB-FETs with and without under-the-BOX SiGe regions. The nUTB-FET with under-the-BOX SiGe shows a higher leakage current, and a peak transconductance improvement of ~30% as compared to the control nUTB-FET.

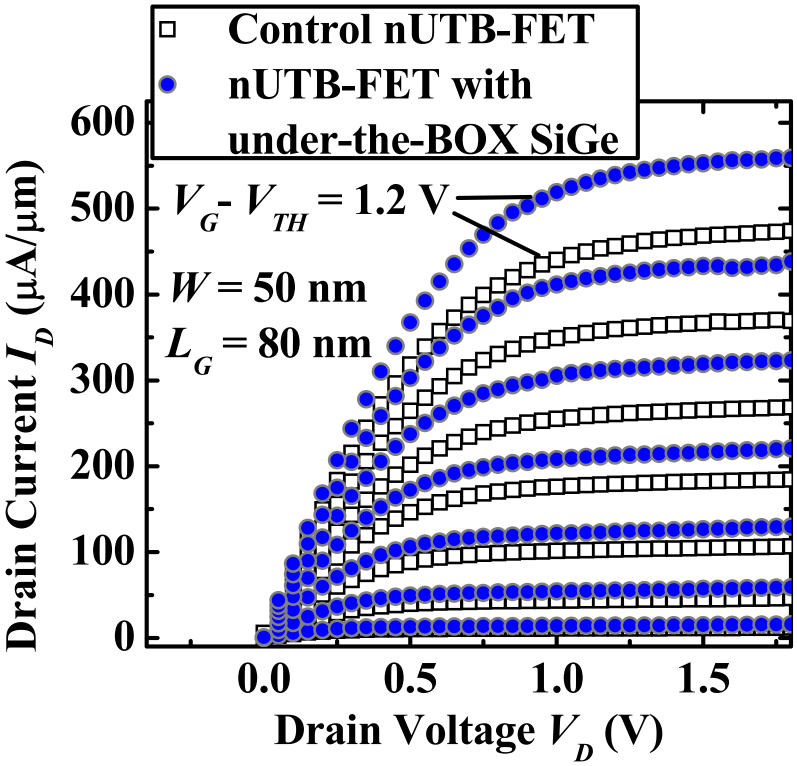


Fig. 2.15. I_D-V_D characteristics of the same pair of nUTB-FETs with and without under-the-BOX SiGe regions in Fig. 2.14, with gate length of 80 nm and channel width of 50 nm. The nUTB-FET with under-the-BOX SiGe shows ~18% drain current enhancement over the control at gate overdrive of 1.2 V.

The reason for the high leakage current in the strained nUTB-FET with under-the-BOX SiGe is examined next. As discussed above, the high-dose Ge implant introduced a high concentration of Ge near the interface between the BOX and the Si substrate, as shown in Fig. 2.3. During the high-temperature anneal, at 900 °C for 60 s for SiGe formation, Ge could diffuse into the ultra-thin BOX and Si layers and introduce traps there, which results in an increase in leakage current due to trap-assisted tunneling. In fact, this mechanism caused electrical shorting of most nUTB-FETs with under-the-BOX SiGe, and only very few devices were found to be working. When the BOX layer is probed as shown in Fig. 2.16(a), the sample annealed at 900 °C for 60 s shows a very high leakage current, as seen in Fig. 2.16(b). Annealing at a lower temperature but for a longer duration for SiGe formation can reduce the leakage current

[Fig. 2.16(b)] and improve the yield of nUTB-FETs with under-the-BOX SiGe. Further work to optimize the under-the-BOX SiGe technique in UTB-FETs is discussed in Chapter 6.

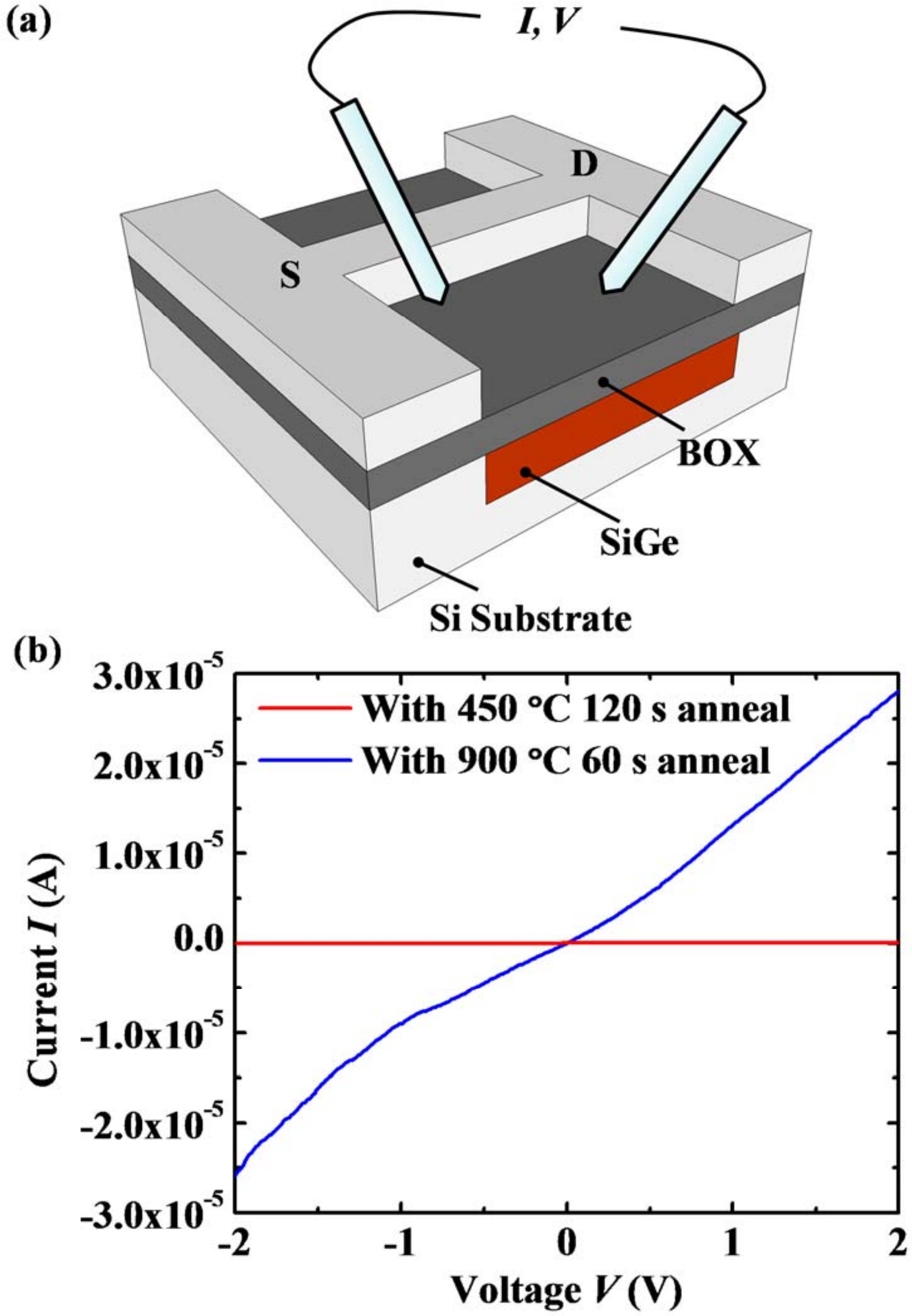


Fig. 2.16. (a) Current was measured by probing on BOX layer, after Ge implantation and thermal anneal for SiGe formation. (b) *I*-*V* characteristics for samples with 900°C, 60 s anneal, and 450°C, 120 s anneal. Annealing at a lower temperature but for a longer duration for SiGe formation could reduce the leakage current.

2.6 Conclusion

A new strain engineering technique for UTBB-SOI structures was demonstrated. Ge ion implantation through the ultra-thin Si and UT-BOX followed by crystallization forms localized SiGe regions under the UT-BOX. A high compressive lateral stress σ_{xx} of up to ~1.5 GPa was found in the ultra-thin Si region with under-the-BOX SiGe using numerical simulation. Strain analysis was performed using NBD technique. Compressive strain of up to -0.55% and -1.2% in the <110> direction (x-direction) were detected by NBD at the center and the edge, respectively, of an ultra-thin 50-nm-wide Si region between two localized SiGe regions.

Next, the under-the-BOX SiGe technique was integrated in n-channel UTB-FETs. The channel width was designed to be very narrow, and the localized SiGe regions was found by finite-element simulation to induce a longitudinal (source-to-drain direction) tensile stress up to ~3000 MPa in the channel region. Significant drive current enhancement of ~18% was observed for the nUTB-FET with under-the-BOX SiGe compared to the control device. However, the process flow for fabricating nUTB-FETs with under-the-BOX SiGe technique needs to be optimized in order to achieve a reasonable device yield.

Chapter 3

Phase-Change Liner Stressor for Strain Engineering of P-Channel FinFETs

3.1 Introduction

FinFETs or multi-gate transistors exhibit excellent control of short channel effects (SCE), and have been adopted by the semiconductor industry at the 22 nm technology node and beyond [90]-[104]. Various strain engineering or mobility enhancement techniques were reported to enhance the transistor drive current I_{Dsat}. High-stress silicon nitride (SiN) liner stressor or contact etch stop layer has been adopted in the manufacturing of integrated circuits based on planar transistors. In FinFETs, significant I_{Dsat} enhancement can also be achieved using the SiN liner stressor [97]-[101]. In p-channel FinFETs (p-FinFETs), diamond-like carbon (DLC) liner stressor has been demonstrated for strain engineering [102],[105]. DLC has an intrinsic compressive stress of up to 10 GPa, significantly greater than that of SiN, and allows a higher channel stress to be induced for a given liner thickness. DLC liner stressor has been reported to give significant I_{Dsat} enhancement for p-FinFETs [102],[105]. The key concept of the abovementioned SiN or DLC liner stressors is the mechanical coupling of the intrinsic stress from the liner to the FinFET channel.

In this Chapter, we demonstrate a new concept for strain engineering, where a liner material is formed over a transistor and then configured to change volume post-deposition, so as to induce mechanical stress in the channel. Phase change chalcogenide materials may be used as a liner material where such volume change may be effected post-deposition. For example, the liner material may be $Ge_2Sb_2Te_5$, denoted as GST. When GST undergoes crystallization or phase change from the amorphous state (α-GST) to the crystalline state (c-GST), its mass density increases and its volume is reduced. The mechanical stress induced by the GST contraction could be exploited for strain engineering of p-FinFETs.

Section 3.2 explains the key concept of using GST as a shrinkable liner stressor for FinFET. In Section 3.3, details of the process development and integration of GST liner stressor for p- FinFETs are described. In Section 3.4, extensive electrical characterization is performed for FinFETs with and without the GST liner stressor, and the performance enhancement induced by the GST liner stressor is discussed. Section 3.5 summarizes the key results achieved in this technology demonstration.

3.2 Key Concept: GST as a Shrinkable Liner Stressor

In this Section, the volume reduction or contraction due to the change of phase of GST from amorphous to crystalline is discussed. The contraction or shrinkage of the as-deposited α-GST is a physical phenomenon that is exploited in this work for transistor strain engineering.

An experiment was carried out to investigate the amount of volume change during the GST phase conversion. A 70-nm-thick α-GST was deposited on a Si substrate by sputtering at room temperature using 100 W DC power and at a pressure of 3 mTorr, followed by a 200 °C anneal for 10 minutes. The anneal crystallized the α-GST, forming c-GST with a reduced thickness. It is well-known that the amorphous and crystalline phases of GST can be reversibly changed. After crystallization of GST, we converted a selected region of the c-GST back into α-GST by a rapid laser-induced melt-quench process. A KrF excimer laser with a wavelength of 248 nm and a pulse duration of 23 ns was used to irradiate c-GST in a 2 mm by 2 mm area in N_2 ambient. All process steps were performed by the author excepted for the laser irradiation step which was done by Dr. WANG Xincai of the Singapore Institute of Manufacturing Technology (SIMTECH). The c-GST in this area was melted during the ultra-short laser irradiation, and the rapid cooling after the laser pulse converted it to the amorphous phase.

A Scanning Electron Microscopy (SEM) image [Fig. 3.1(a)] shows the top view of a sample having α-GST and c-GST regions adjacent to each other [Fig. 3.1(b)]. Examination of the cross-sectional SEM image in Fig. 3.1(c) reveals that the thicknesses of the α-GST and c-GST are 70 nm and 65 nm, respectively. Atomic Force Microscopy (AFM) was also used to scan the boundary region between the α-GST and the c-GST regions [Fig. 3.1(d)]. The thickness difference between the α-GST and c-GST layers is ~5 nm, which is consistent with the SEM observation in Fig. 3.1(c). We therefore deduced that the c-GST has a 7% volume reduction as compared with the α-GST. This is consistent with reported values (5.4 to 7.0%) in the literature [145],[146].

Fig. 3.2(a) depicts a GST liner stressor wrapped around a FinFET. Coordinate axes are also shown. Fig. 3.2(b) illustrates the key concept of this work using cross-section schematics of the transistor in the A-A' plane (*x*-*z* plane cutting through gate line and perpendicular to fin) and B-B' plane (*y*-*z* plane cutting through fin and perpendicular to gate line). The liner is amorphous when first formed over the FinFET.

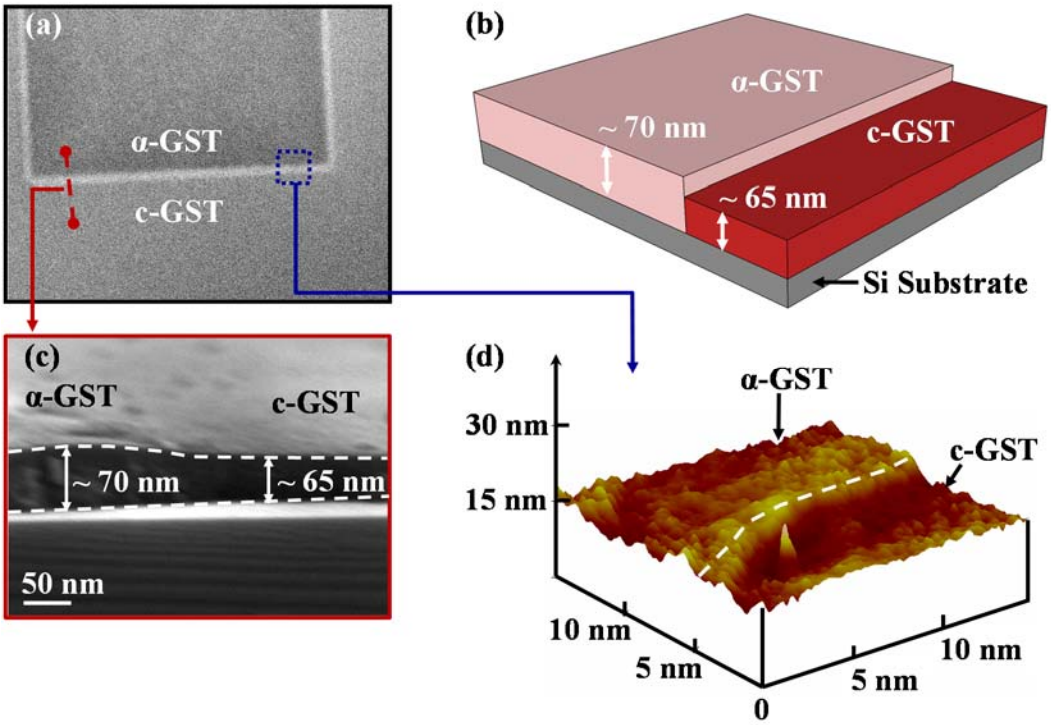


Fig. 3.1. (a) A Scanning Electron Microscopy (SEM) image showing the top view of a crystalline $Ge_2Sb_2Te_5$ (c-GST) sample with a part of it being selectively converted to amorphous $Ge_2Sb_2Te_5$ (α-GST) using a shaped excimer laser beam. A single pulse of homogenized laser beam with a fluence of 150 mJ/cm^2 was used. (b) Illustration of α-GST and c-GST regions adjacent to each other. (c) Cross-sectional SEM image shows that the thicknesses of the α-GST and c-GST regions are 70 nm and 65 nm, respectively. (d) An Atomic Force Microscopy (AFM) scan across the boundary between the α-GST and c-GST regions obtained a thickness difference of ~5 nm.

When GST undergoes phase change or crystallization from α-GST to c-GST, the volume contraction causes it to constrict or tighten its grip on the FinFET structure. In the A-A' plane, a large compressive strain ε_{xx} and ε_{zz} can result from the GST contraction. The B-B' plane view shows that the contracted c-GST increases the lateral compression ε_{yy} (source-to-drain direction) in the channel. The strain induced by GST in the FinFET channel was studied using Nano Beam Diffraction (NBD) and is documented in Chapter 4.

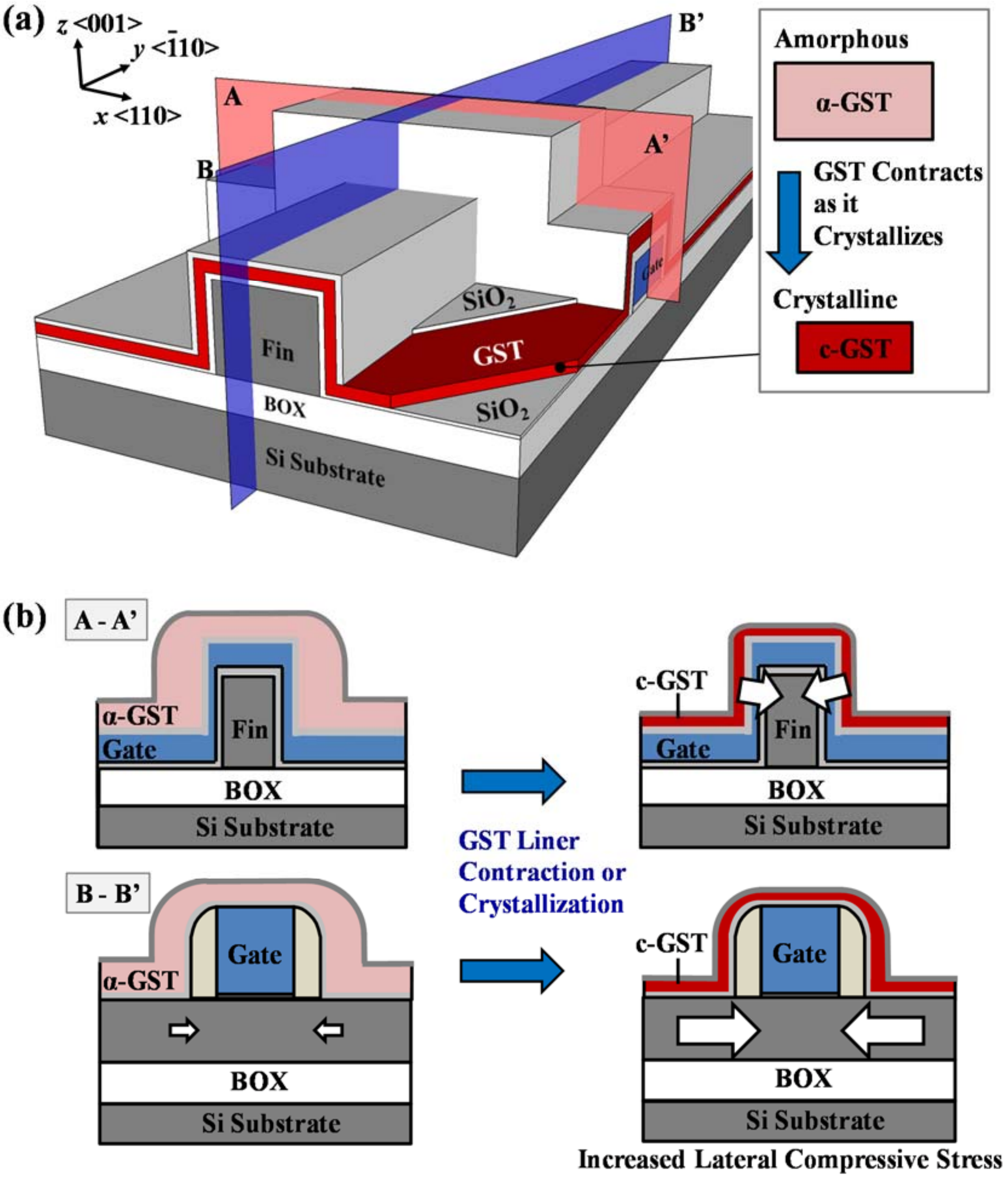


Fig. 3.2. (a) Three-dimensional schematic of a FinFET wrapped around by GST liner stressor. Coordinate axes are also shown. When GST crystallizes, its volume is reduced by ~7%. (b) Cross-section obtained in the A-A' plane illustrating the large compressive strain ε_{xx} and ε_{zz} that can result from GST contraction. The B-B' plane view shows that the contracted c-GST liner increases the compressive strain ε_{yy} in the channel in the source-to-drain direction.

3.3 Fabrication of Strained P-FinFETs with GST Liner Stressor

Eight-inch silicon-on-insulator (SOI) wafers with Si thickness of 35 nm were used for FinFET fabrication. 248-nm Deep Ultra-Violet (DUV) lithography was used for active patterning, followed by dry etching to define the fins. The fin height H_{fin} is 35 nm and fins with width W_{fin} down to 40 nm were formed. SiO_2 gate dielectric of 3 nm was thermally grown. This was followed by poly-Si gate deposition and ion implantation of boron. SiO_2 hardmask was formed on the poly-Si gate, followed by gate definition using 248-nm lithography. Photoresist and hardmask trimming were sequentially performed. Poly-Si gate etch was performed using chlorine-based plasma dry etch. After the gate etch, p^+ source/drain (S/D) extension implant was performed and SiN spacers were formed by chemical vapor deposition of SiN followed by dry etch. The p-FinFET fabrication process steps mentioned above were done by Dr. KOH Shao Ming of our research group. The following steps were performed by the author.

After deep S/D implantation and dopant activation, the SiO_2 hardmask on the poly-Si gate was removed. 10 nm of Ni was sputter-deposited and annealed to form NiSi on the gate and S/D regions. Excess Ni was selectively removed with a sulphuric acid-peroxide solution H_2SO_4:H_2O_2 [4:1] at a temperature of 120 ˚C for 120 s.

13 nm of SiO_2 was deposited on the FinFETs by plasma-enhanced chemical vapor deposition, which provides electrical isolation between the device and the to-be-deposited GST layer. A thinner SiO_2 layer is expected to improve the mechanical stress coupling between the GST stressor and the transistor channel.

70 nm of α-GST was deposited by sputtering at room temperature using 100 W DC power and at a pressure of 3 mTorr. ~10 nm of SiO_2 cap layer was deposited on top of the GST without breaking vacuum. Contact patterning and dry etching using inductively coupled fluorine-based plasma were done on control and active devices, to

remove SiO_2 layer and SiO_2/α-GST/SiO_2 layers in the contact regions, respectively. This completed the FinFETs with α-GST split.

A 200 ˚C 10 minute anneal was then performed for GST liner contraction, converting the α-GST to c-GST for the FinFETs with c-GST split. The process flow is depicted in Fig. 3.3(a). Fig. 3.3(b) and (c) show the SEM images of the control or unstrained FinFET and the strained FinFET with c-GST liner stressor, respectively. Electrical characterization was performed by probing the NiSi source, drain, and gate contacts. In this work, the probes on the NiSi in the S/D regions are ~50 µm from the gate edge. To ensure a fair comparison, only the α-GST deposition step was skipped for the control or unstrained FinFETs.

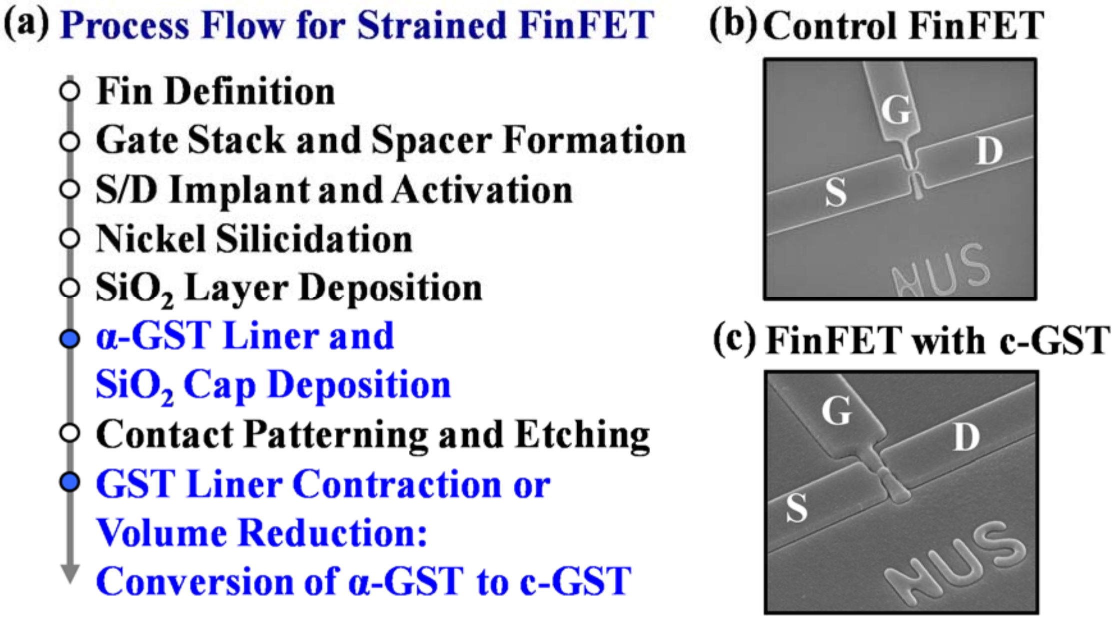


Fig. 3.3. (a) Process flow for fabricating p-FinFETs with GST liner stressor. GST deposition and liner contraction steps were skipped for the control FinFETs. The SiO_2 layer insulates the GST layer from the fin or the gate. (b) SEM image of control or unstrained p-channel FinFET. (c) SEM image of p-channel strained FinFET with c-GST liner stressor.

A cross-sectional Transmission Electron Microscopy (TEM) image of a FinFET with ~70-nm-thick c-GST liner stressor is shown in Fig. 3.4(a). To obtain the

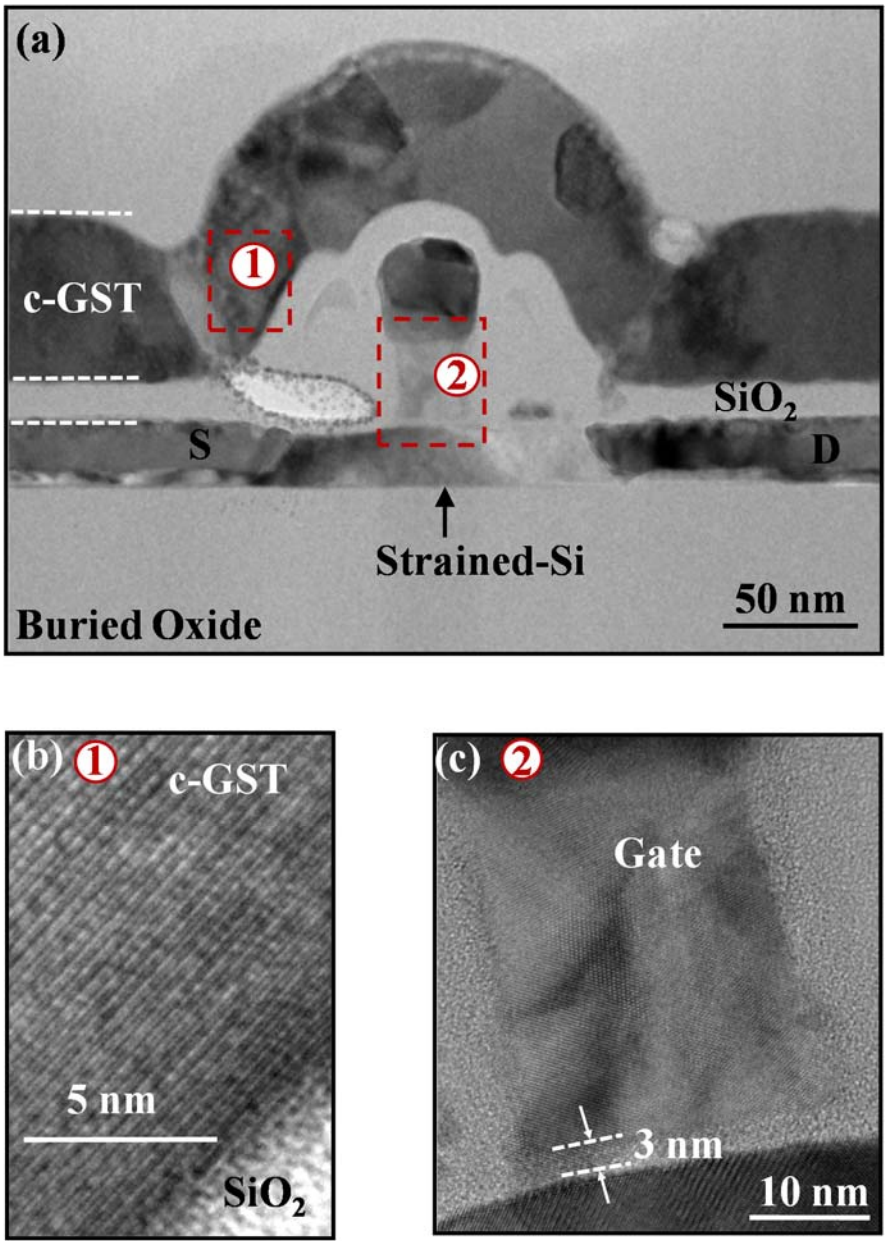


Fig. 3.4. (a) Cross-sectional Transmission Electron Microscopy (TEM) image of a p-FinFET with c-GST stressor showing a gate length of ~30 nm. A Focused Ion Beam (FIB) cut was performed in the source-to-drain direction across the gate. (b) Higher resolution TEM image showing the crystalline GST at region 1. Clear lattice fringes could be observed. GST crystallization or contraction increases the compressive stress in the channel in the source-to-drain direction. (c) Higher resolution TEM image of the gate stack (region 2). The TEM was performed as an external service job at the Institute of Materials Research and Engineering (IMRE).

TEM images in Fig. 3.4, Focused Ion Beam (FIB) cut was performed in the channel region across the gate along the source-to-drain direction. High resolution TEM images show that the GST is crystallized [Fig. 3.4(b)]. The FinFET gate length is ~30 nm as shown in Fig. 3.4(c). It is noted that the channel stress is not only introduced by the intrinsic stress in the GST liner, but also by the GST liner contraction during the phase conversion process.

To minimize the differences in electrical performance caused by process variation across wafers or between dies, the control and strained FinFETs compared were processed on the same die. All devices were processed to the step before GST deposition, before each die was broken into pieces for the experimental splits.

3.4 Electrical Characterization and Discussion

Fig. 3.5(a) shows the I_D-V_G characteristics of FinFETs (L_G = 55 nm and W_{fin} = 45 nm) with and without α-GST liner stressor. Both devices have similar drain induced barrier lowering (DIBL) and subthreshold swing. Fig. 3.5(b) shows the I_{off} - I_{Dlin} characteristics of control FinFETs and FinFETs with α-GST stressor. At I_{off} = 10 nA/μm, FinFETs with α-GST stressor show about 66% I_{Dlin} enhancement over the control FinFETs. This drain current enhancement is due to the intrinsic compressive stress of α-GST [-332 MPa, as determined by wafer-curvature measurement (outsourced)], similar to the effect of SiN or DLC liner stressors with intrinsic compressive stress.

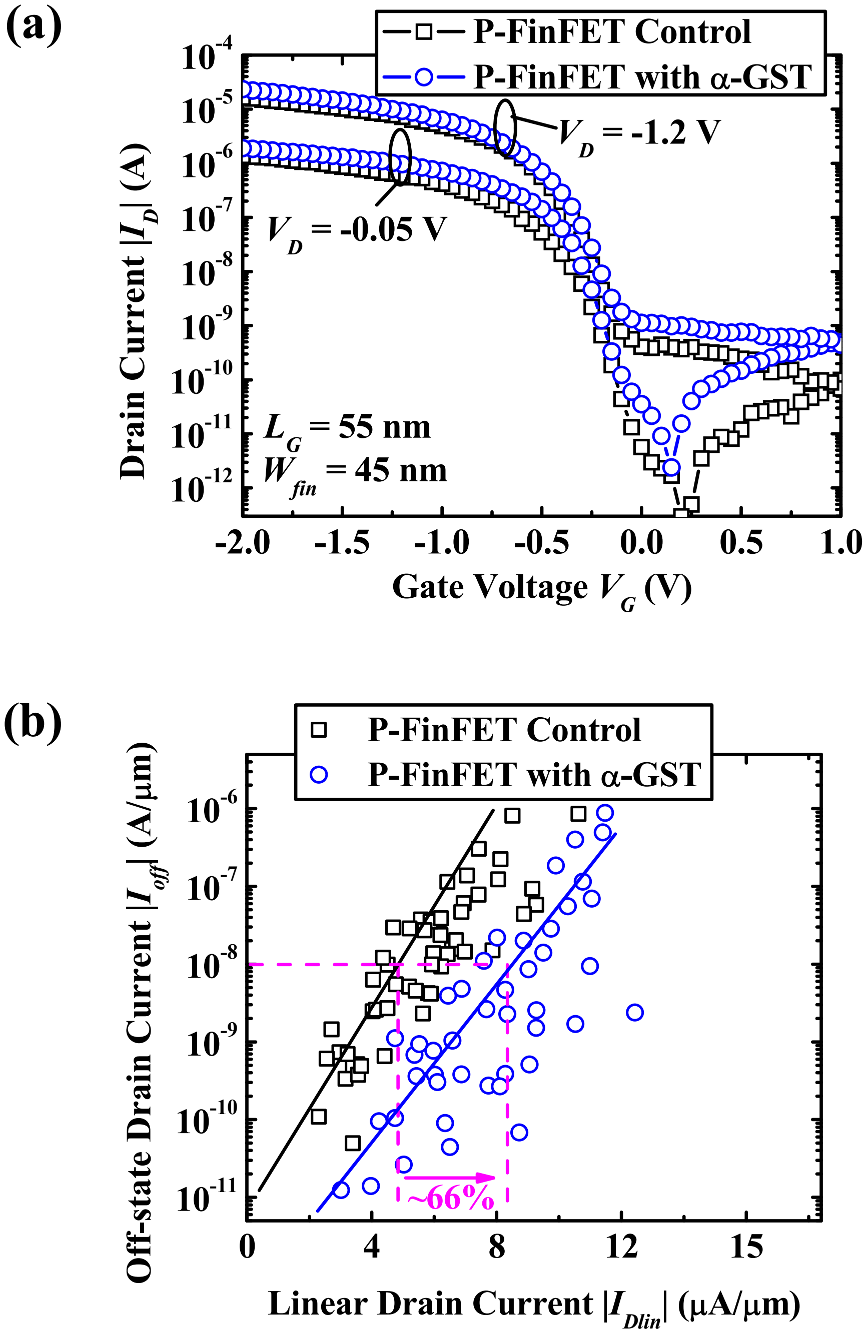


Fig. 3.5. (a) I_D-V_G characteristics of p-FinFETs with and without α-GST liner stressor, showing comparable DIBL and subthreshold swing. Gate length is 55 nm and fin width is 45 nm. (b) Plot of off-state current $|I_{off}|$ ($V_G = V_{TH,lin} + 0.2$ V, $V_D = -1.2$ V) versus $|I_{Dlin}|$ ($V_G = V_{TH,lin} - 1.1$ V, $V_D = -0.05$ V). W_{fin} = 35 nm to 115 nm, and L_G = 15 nm to 80 nm. At an off-state current $|I_{off}|$ of 10 nA/μm, FinFETs with α-GST liner stressor show ~66% I_{Dlin} enhancement over the control FinFETs. For each device split, ~50 FinFETs were measured.

The I_{Dsat} enhancement for FinFETs with as-deposited α-GST and c-GST stressor, as compared to that for the unstrained FinFET is illustrated in Fig. 3.6. The

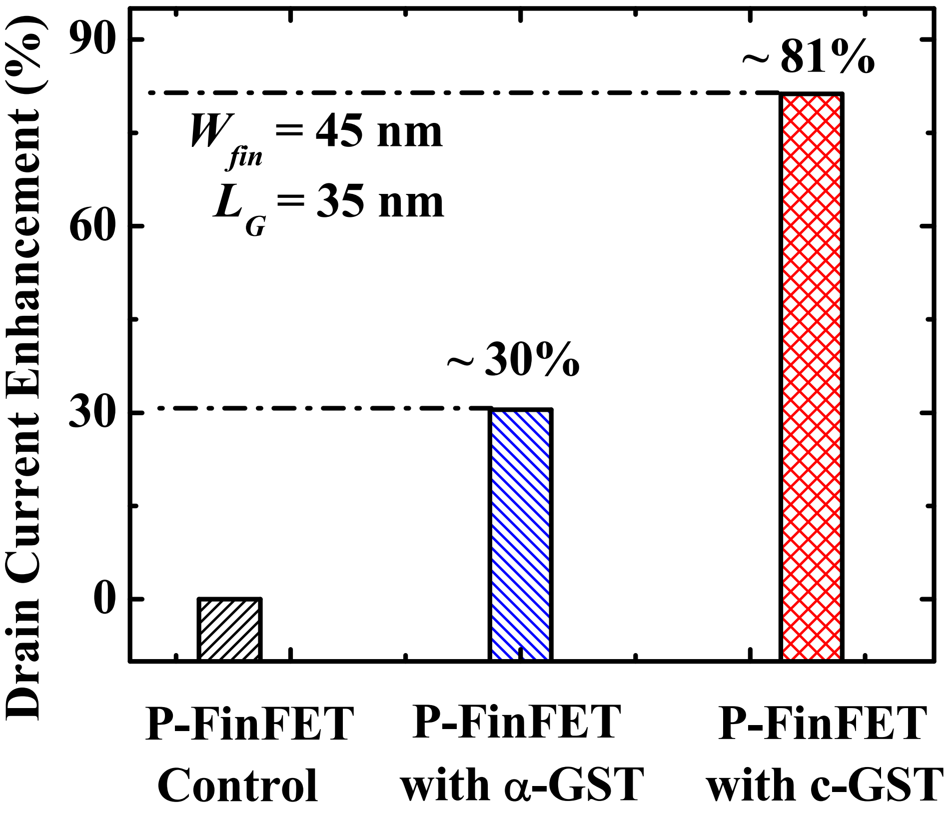


Fig. 3.6. ~30% and ~81% I_{Dsat} ($V_G = V_{TH,sat} - 1.1$ V, $V_D = -1.2$ V) enhancement were observed for p-FinFETs with α-GST and c-GST liner stressor, respectively, over the control FinFET. GST contraction during amorphous-to-crystalline phase conversion induces stress that leads to further I_{Dsat} enhancement.

intrinsic compressive stress in α-GST enhances hole mobility in p- FinFETs, resulting in ~30% I_{Dsat} enhancement over the control.

When the GST is crystallized, the GST liner contraction or volume reduction increases the strain level in the channel further, leading to higher I_{Dsat} enhancement of ~81% with respect to the control. All the devices in Fig. 3.6 have the same L_G of 35 nm and W_{fin} of 45 nm.

FinFETs with c-GST stressor will be discussed next. Fig. 3.7(a) shows the I_D-V_G characteristics of FinFETs (L_G = 45 nm and W_{fin} = 75 nm) with and without c-GST stressor. At a comparable SCE control such as DIBL, the FinFET with c-GST stressor has a slightly smaller threshold voltage than the unstrained FinFET. The band structure modification by strain results in a narrowed energy bandgap and leads to a ~10 mV reduction in the magnitude of the threshold voltage and higher leakage current [147]-[151]. Comparison of the saturation transconductance of these two devices as a function of gate voltage is also shown in Fig. 3.7(a). The FinFET with c-GST stressor has over 98% peak transconductance enhancement over the control FinFET. Fig. 3.7(b) compares the I_D-V_D characteristics of the devices in Fig. 3.7(a). I_D is normalized by the device width ($2H_{fin} + W_{fin}$). I_{Dsat} enhancement of ~78% was observed for the FinFET with c-GST stressor over the control FinFET at gate overdrive of -1.2 V. As the process flow is the same for these two devices except for the GST deposition and liner contraction, the difference in I_{Dsat} is due to the c-GST stressor. The drive current enhancement is consistent with the transconductance enhancement shown in Fig. 3.7(a).

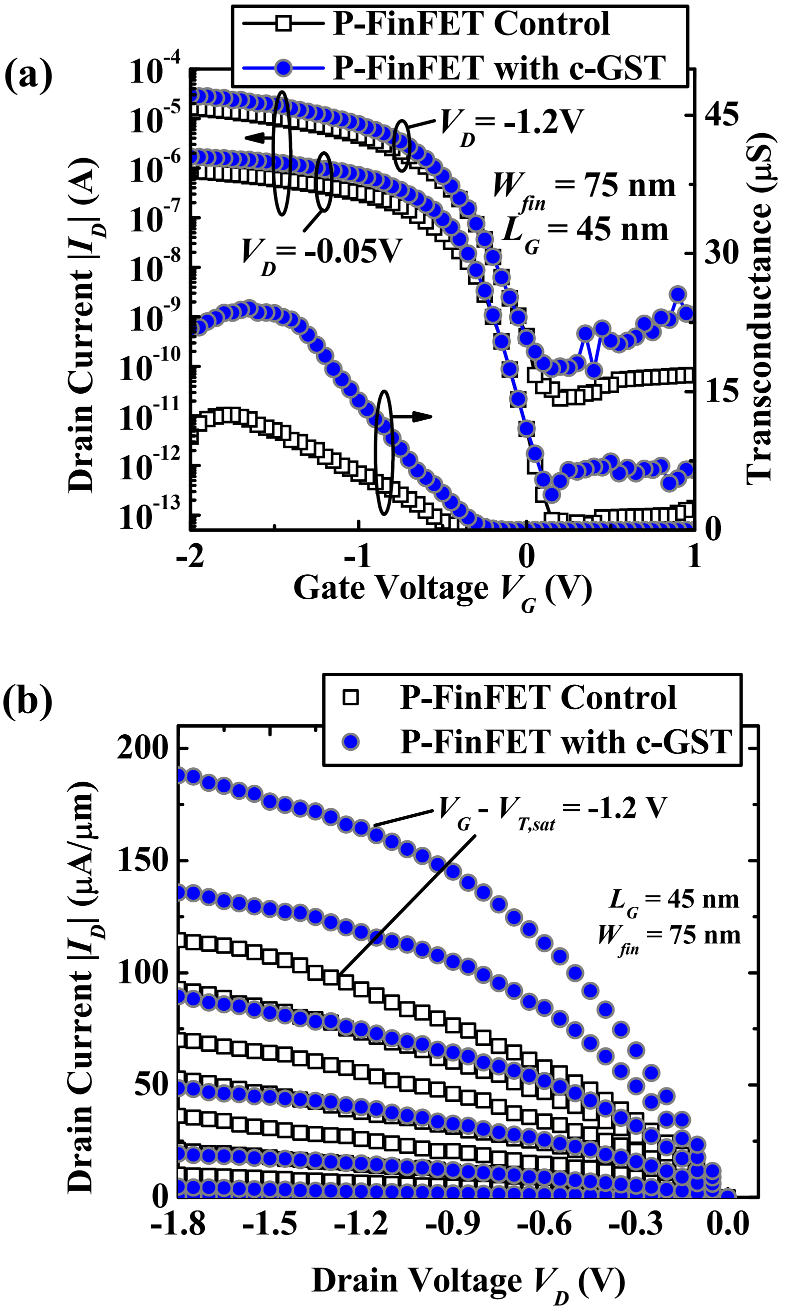


Fig. 3.7. (a) I_D-V_G characteristics of p-FinFETs with and without c-GST liner stressor, showing similar DIBL and subthreshold swing. The FinFET with c-GST has a $|V_{TH,sat}|$ that is slightly smaller (~10 mV) than that of the control. Gate length is 45 nm and fin width is 75 nm. Transconductance as a function of gate voltage is also shown. The FinFET with c-GST liner stressor has a peak transconductance improvement of ~98% over the control FinFET. (b) I_D-V_D characteristics of the p-FinFET with c-GST liner stressor and the control, with gate length of 45 nm and fin width of 75 nm. The FinFET with c-GST liner stressor shows ~78% drain current enhancement over the control at gate over-drive of -1.2 V.

The I_{off} - I_{Dsat} and I_{off} - I_{Dlin} characteristics of FinFETs with and without c-GST stressor are shown in Figs. 3.8 and 3.9, respectively. At a fixed I_{off} of 10 nA/μm, we observe an enhancement in I_{Dsat} and I_{Dlin} of ~88% and ~117%, respectively. For each device split in Figs. 3.8 and 3.9, ~60 devices were measured. The observed I_{Dsat} enhancement induced by the c-GST liner stressor is higher than those induced by SiN and DLC stressors [101],[105].

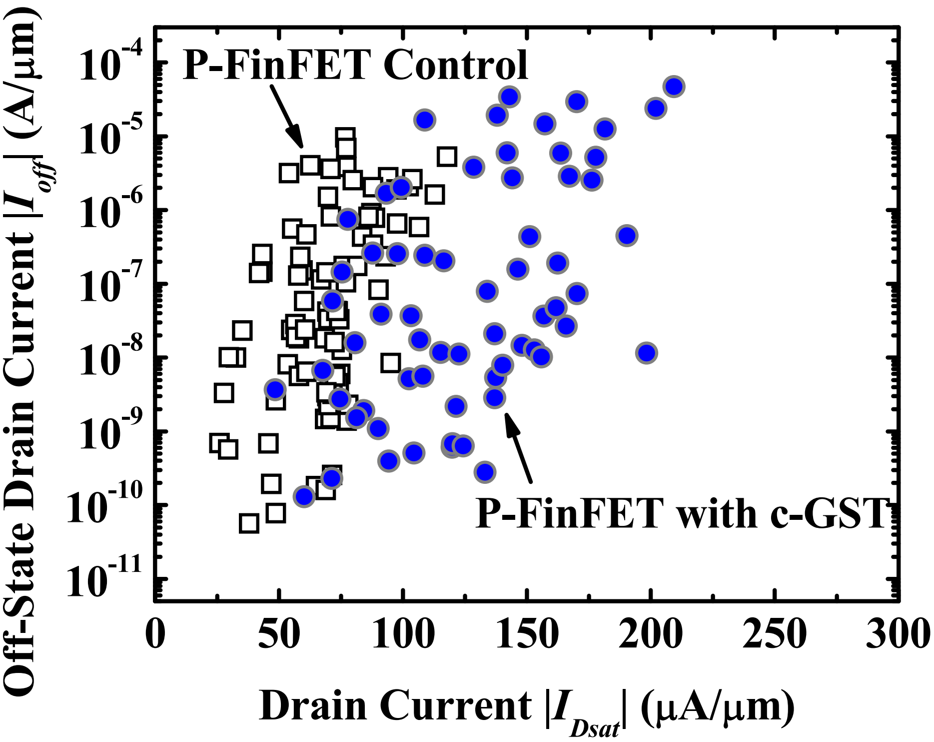


Fig. 3.8. Comparison of off-sate current |I_{off}| (obtained at $V_G = V_{TH,sat} + 0.2$ V, V_D= -1.2 V) versus |I_{Dsat}| (obtained at $V_G = V_{TH,sat} - 1.1$ V, V_D = -1.2 V) showing ~88% I_{Dsat} enhancement for FinFETs with c-GST liner stressor over the control FinFETs at |I_{off}| = 10 nA/μm. For each device split, ~60 FinFETs or data points were measured.

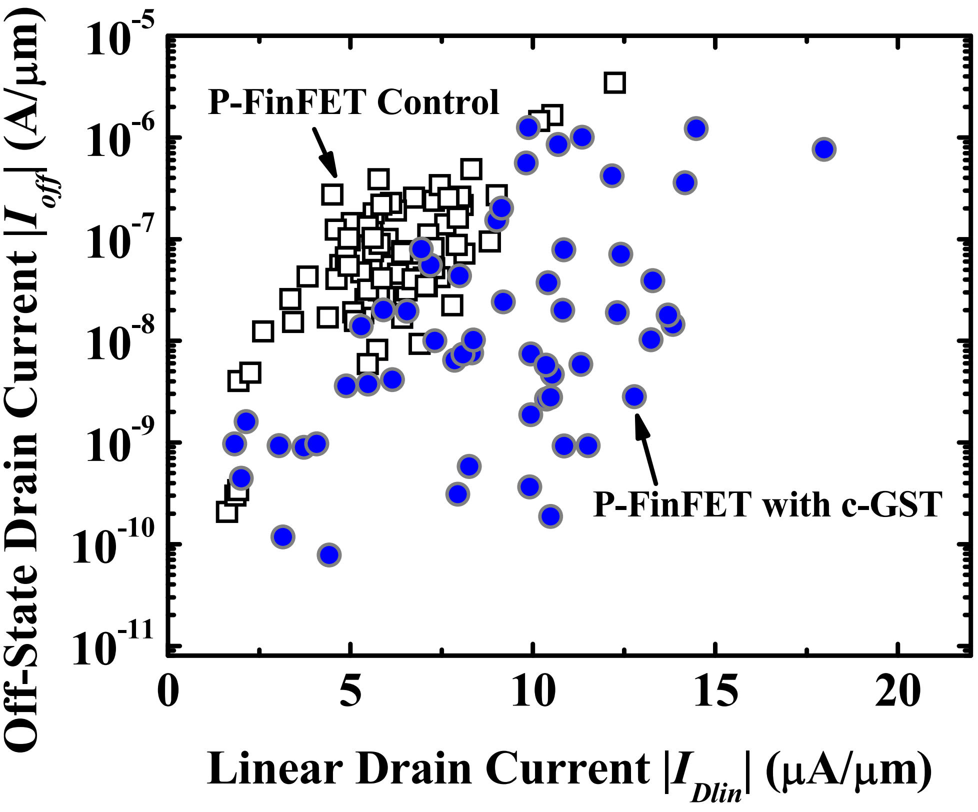


Fig. 3.9. Plot of off-state current |I_{off}| (obtained at $V_G = V_{TH,lin} + 0.2$ V, $V_D = -1.2$ V) versus |I_{Dlin}| (obtained at $V_G = V_{TH,lin} - 1.1$ V, $V_D = -0.05$ V). At |I_{off}| = 10 nA/μm, ~117% I_{Dlin} enhancement for FinFETs with c-GST liner stressor over the control FinFETs is observed. For each device split, ~60 FinFETs were measured.

The I_{Dsat} of FinFETs with and without c-GST stressor are compared at different L_G (from 15 nm to 55 nm) with a fixed W_{fin} of 40 nm in Fig. 3.10. When gate length is reduced, I_{Dsat} generally increases. The I_{Dsat} of FinFETs with c-GST stressor is higher than that of the control FinFETs without stressor for all L_G. In addition, the current enhancement is higher for smaller L_G, which is attributed to higher strain induced by the c-GST stressor at smaller L_G. This trend is consistent with simulation results of FinFETs with SiN and GST liners [153],[154].

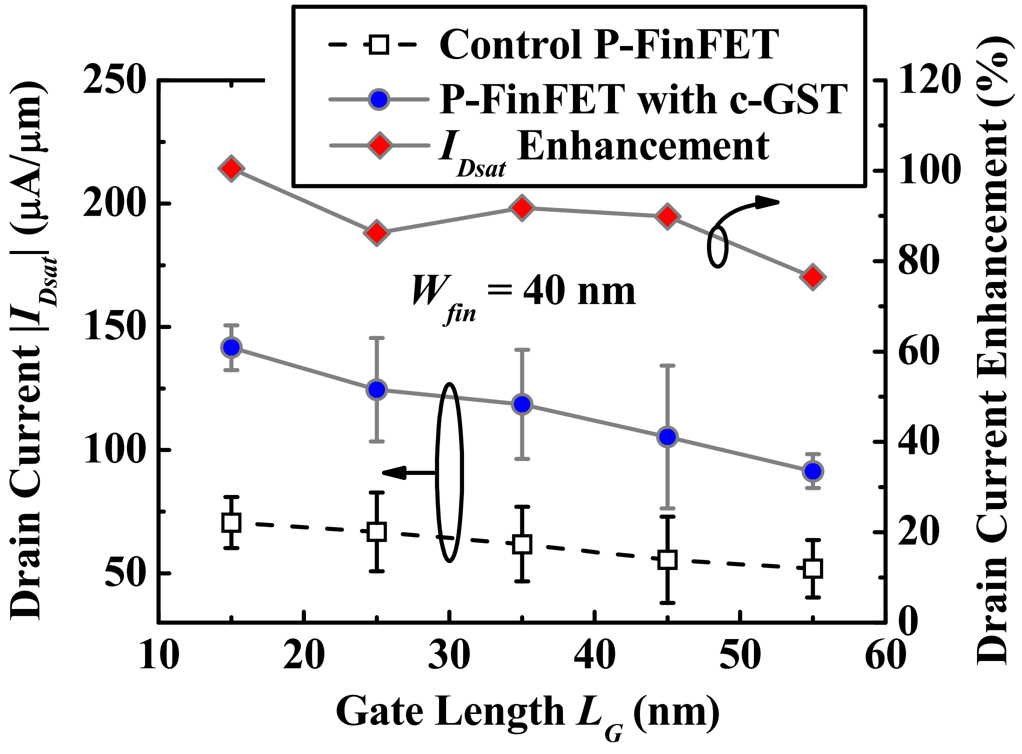


Fig. 3.10. Comparison of I_{Dsat} (obtained at $V_G = V_{TH,sat} - 1.1$ V, $V_D = -1.2$ V) for p-FinFETs with and without c-GST liner stressor at different gate lengths. As gate length is reduced, the I_{Dsat} of FinFETs both with and without c-GST stressor increases. I_{Dsat} enhancement as a function of gate length is also plotted. I_{Dsat} enhancement increases with decreasing gate length. The standard deviation of I_{Dsat} for a given W_{fin} and L_G is shown as error bars. Enhancement values were calculated using the mean I_{Dsat}.

To illustrate the effect of fin width on I_{Dsat} enhancement, the I_{Dsat} of p-FinFETs with and without c-GST stressor and I_{Dsat} enhancement as a function of W_{fin} for a fixed L_G are shown in Fig. 3.11. I_{Dsat} enhancement increases with decreasing fin width.

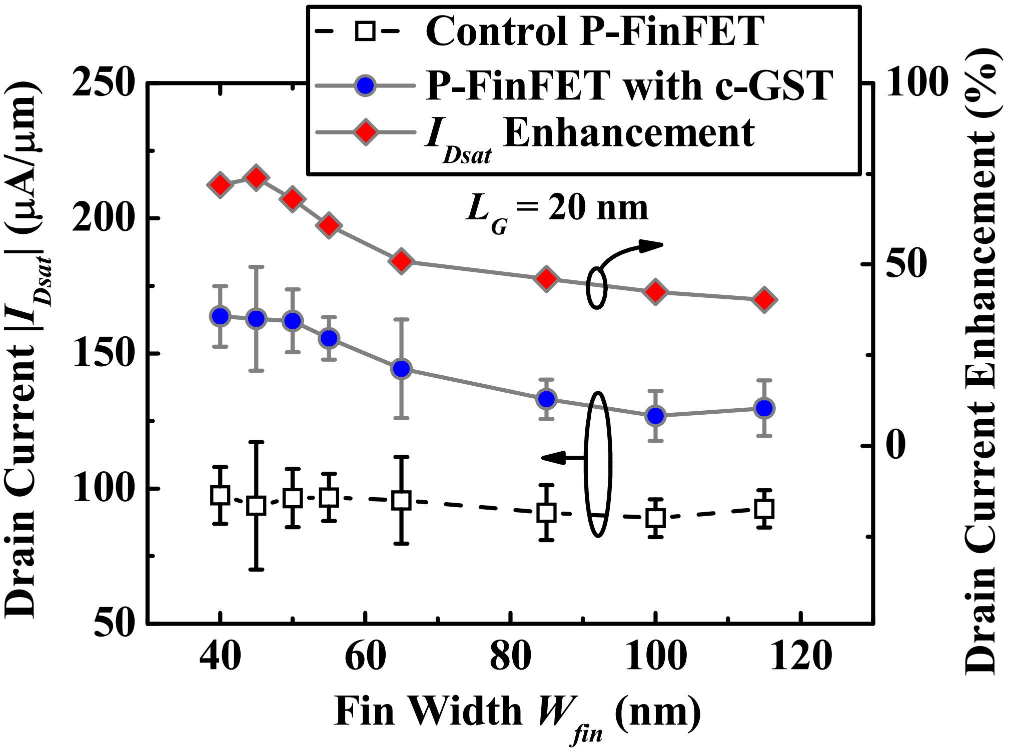


Fig. 3.11. Comparison of I_{Dsat} (obtained at $V_G = V_{TH,sat} - 1.1$ V, $V_D = -1.2$ V) for p-FinFETs with and without c-GST liner stressor at different W_{fin} and fixed L_G of 20 nm. I_{Dsat} percentage enhancement (right) increases with decreasing W_{fin}. The standard deviation of I_{Dsat} for a given W_{fin} and L_G is shown as an error bar. Enhancement values were calculated using the mean I_{Dsat}.

Drive current as a function of indicators of SCEs, such as subthreshold swing and DIBL, is plotted in Fig. 3.12 and Fig. 3.13, respectively. The I_{Dsat} of FinFETs with c-GST stressor is 67% higher than that of FinFETs without stressor at a fixed SS of 90 mV/decade (Fig. 3.12). At a fixed DIBL of 0.25 V/V, I_{Dsat} enhancement for FinFETs with c-GST stressor over control FinFETs is ~60% (Fig. 3.13).

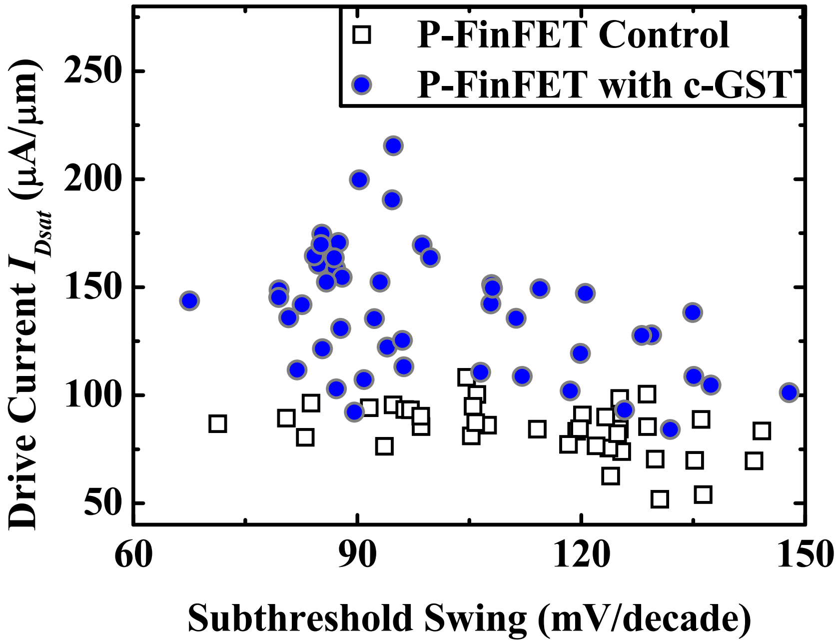


Fig. 3.12. Plot of drive current versus subthreshold swing for FinFETs with and without c-GST liner stressor. At a fixed subthreshold swing of 90 mV/decade, ~67% I_{Dsat} enhancement can be observed for FinFETs with c-GST liner stressor over the control FinFETs. I_{Dsat} was measured at gate overdrive (V_G - $V_{TH,sat}$)= -1.1 V and V_D= -1.2 V.

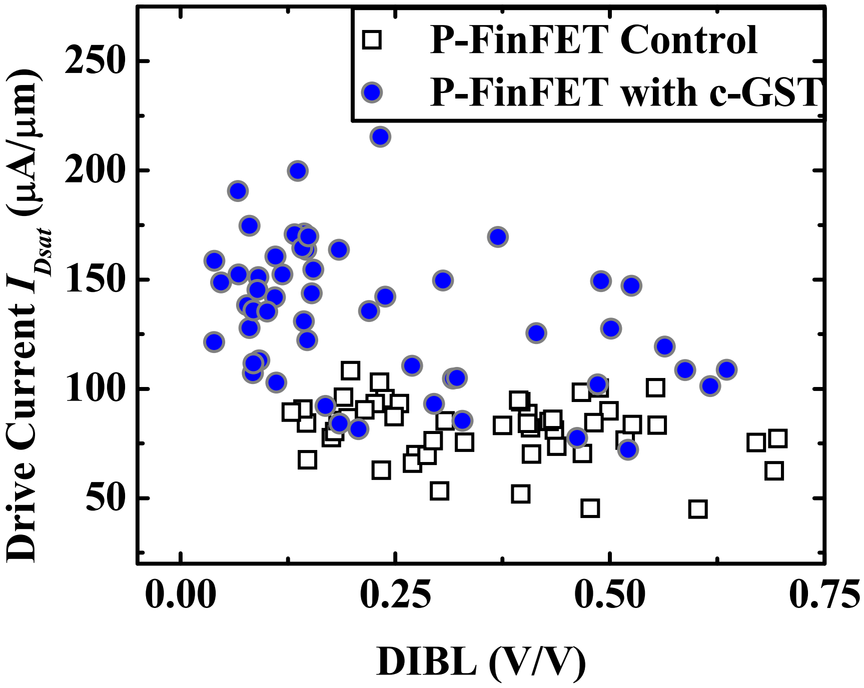


Fig. 3.13. At a fixed DIBL of 0.25 V/V, I_{Dsat} enhancement of ~60% over the control FinFETs is observed for devices with c-GST liner stressor. I_{Dsat} was measured at gate overdrive (V_G - $V_{TH,sat}$)= -1.1 V and V_D= -1.2 V.

To verify the strain effect on carrier mobility enhancement, an approach based on the slope of a plot of total resistance R_{Total} vs. L_G was employed for devices with short L_G. Fig. 3.14 shows the R_{Total}-L_G plot for FinFETs with c-GST stressor and control FinFETs. The effective carrier mobility μ can be estimated using equation below:

$$\mu = \frac{1}{WQ_{inv}\frac{dR_{Total}}{dL_G}} \ , \qquad (3.1)$$

where W is the channel width and Q_{inv} is the inversion charge density. The smaller slope for FinFETs with c-GST stressor as compared to the control translates to a mobility enhancement of up to ~130%.

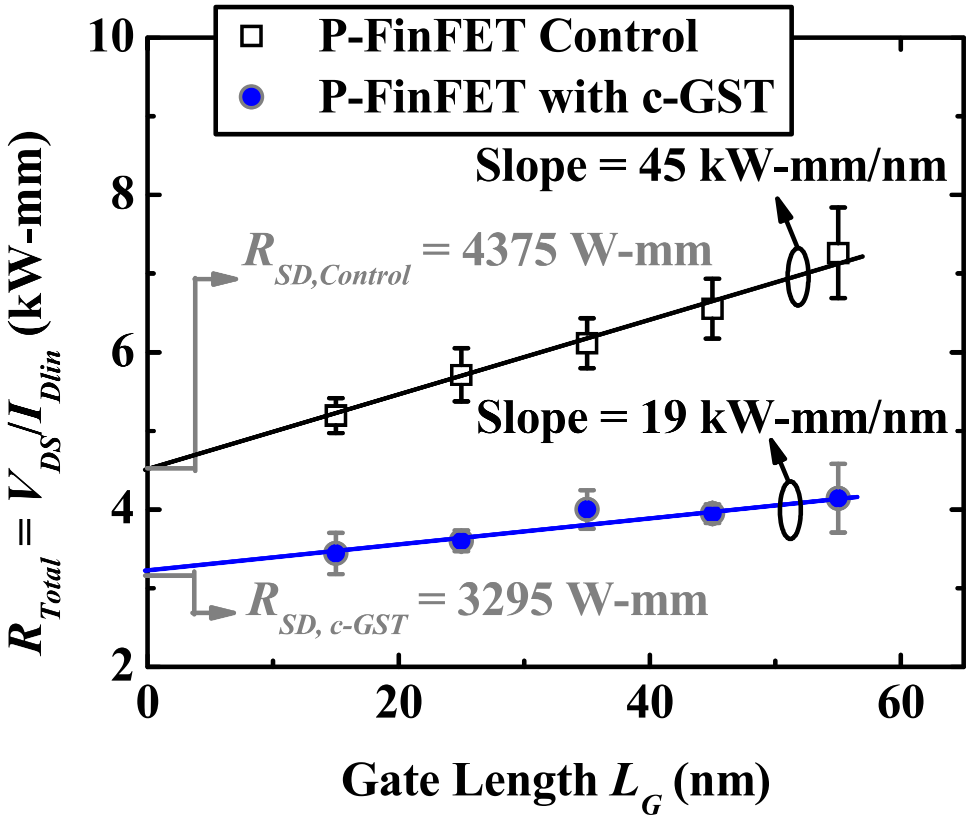


Fig. 3.14. $R_{Total} = V_{DS}/I_{Dlin}$ as a function of L_G (I_{Dlin} was taken at $V_{GS} - V_{TH,lin}$ = -1.1 V, V_{DS} = -50 mV). FinFETs with c-GST liner have a smaller dR_{Total}/dL_G, and exhibit mobility enhancement of ~130%. The standard deviation of R_{Total} is shown as error bars. FinFETs with c-GST also show ~25% R_{SD} reduction as compared to the control FinFETs.

In addition, Fig. 3.14 shows ~25% S/D series resistance (R_{SD}) reduction for the FinFETs with c-GST stressor as compared to the control FinFETs. This is likely to be due to the stress-induced mobility enhancement in S/D regions. A finite-element simulation was performed to investigate the stress in the FinFET with GST liner stressor after contraction. In the simulation, the boundary conditions are such that the bottom and sides of the Si substrate and sides of c-GST layer are rigid. The sides of the domain are assumed to have zero horizontal displacements since they are bounded by huge adjacent volumes. The contraction of the c-GST layer was simulated using the framework of thermoelasticity [133],[134]. Fig. 3.15 shows the distribution of longitudinal stress σ_{yy} in the channel and S/D regions of a FinFET with c-GST liner stressor, indicating a high compressive stress of up to -1500 MPa in the S/D regions induced by the GST liner stressor.

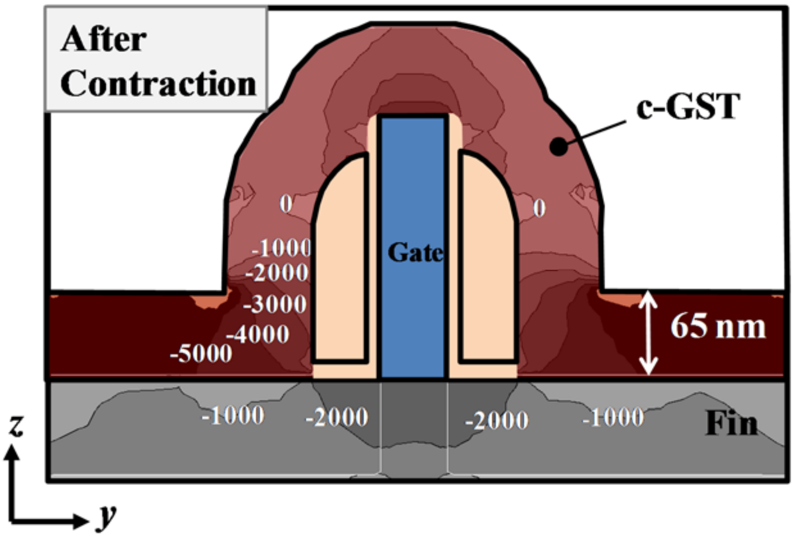
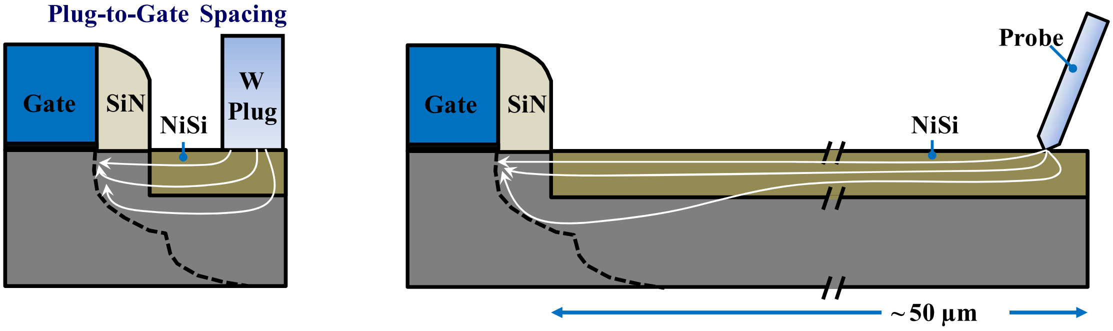


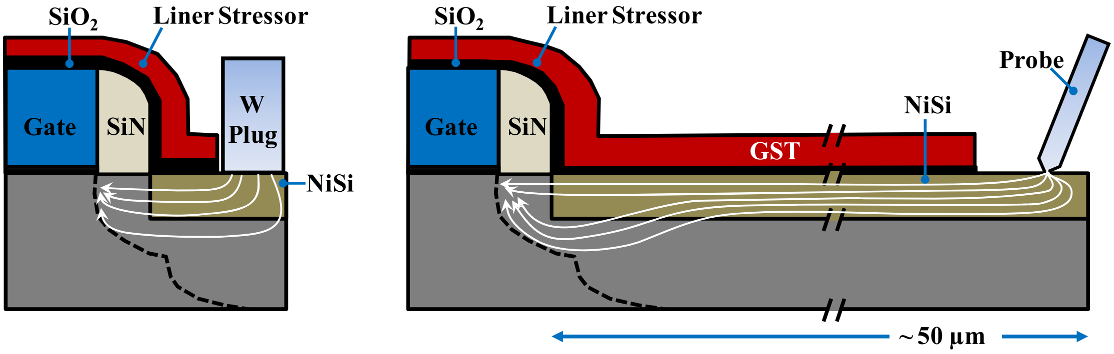
Fig. 3.15. Simulated stress σ_{yy} (in MPa) for FinFET with c-GST liner stressor after contraction. $L_G = 50$ nm. The GST liner contraction induces a larger compressive stress in the channel and S/D regions.

Fig. 3.16 shows a transistor with W plug placed very close to the channel (as is the case in industry) and a transistor in this work where the probe tip contacts the NiSi far (~50 µm) from the channel. As illustrated in Fig. 3.16 (a), the path of current flow from the W plug to the channel is much shorter compared to that in the transistor in this work [Fig. 3.16 (b)], where the current in the S/D region can spread from the NiSi into the un-silicided region under the NiSi over the long distance from probe to channel. The large compressive stress induced by the GST in the S/D regions can lead



(a) Transistor with Small Plug-to-Gate Spacing

(b) Control Transistor in This Work



(c) Transistor with Small Plug-to-Gate Spacing and Liner Stressor

(d) Transistor in This Work with GST Stressor

Fig. 3.16. Schematics of (a) a transistor with very short plug-to-channel distance used in industry, and (b) the transistor in this work, where the probe tip contacts the NiSi far (~50 µm) from the channel. The schematics in (c) and (d) are similar to those in (a) and (b) respectively, except that they have a liner stressor.

to resistivity reduction in the S/D regions. As shown in Fig. 3.16 (c) and (d), the series resistance reduction can be more significant in the transistor in this work than in a typical transistor with short plug-to-channel distance, due to the long current path between the probe and the channel. On the other hand, the thick spacer [~40 nm, as shown in Fig. 3.4(a)], under which the NiSi was not formed, might leads to the observed high $R_{S/D}$ of the FinFET in this work. This could be optimized by using a thinner spacer and will be discussed in the future work in Chapter 6.

As observed in some of the figures [e.g. Figs. 3.5 (b), 3.8 and 3.9], the data points from FinFETs with GST stressor are more widely scattered compared to those of the control. Some of this scatter could be explained by FinFETs with different W_{fin} having different amounts of drain current enhancement as observed in Fig. 3.11. In addition, the immature process flow for integrating the GST stressor could also contribute to the device-to-device variation. Thickness non-uniformity of the GST and the SiO_2 insulating layer below it, incomplete crystallization of the GST in some regions, and lateral etching of GST during the dilute HF etching of residual SiO_2 can all result in variability of the stress levels, leading to device-to-device variations in I_{Dsat} enhancement and S/D series resistance reduction.

We next explore the physical mechanisms in the strained p-channel FinFET. In this work, the top channel of the FinFET is (001)-oriented and the sidewall channels are (110)-oriented [Fig. 3.2(a)]. In an unstrained MOSFET, the degeneracy of the conduction and valence bands is lifted owing to quantum confinement due to the vertical electric field [3]. Under strain, the band edges can be shifted either additively or subtractively to the confinement-induced splitting, and only the additive splitting induced by strain will lead to mobility enhancement in the MOSFET. As the splitting due to $<\bar{1}10>$ uniaxial compression is additive to the confinement effect for valence bands [3], the longitudinal compressive strain in the <$\bar{1}$10> direction induced by c-GST enhances the hole mobility in the p-FinFET. However, the mobility enhancement due to the c-GST stressor is different for the top channel and the sidewall channels due to the different surface orientations. Besides causing the band edge to shift, strain breaks crystal symmetry and alters the band structure away from the energy minimum. Applying stress along a lower symmetrical axis causes more destructive of crystal symmetry and results in a greater band warping [51]. Ground-state sub-band warping is the major reason for the different enhancement in the (001)-oriented top channel and the (110)-oriented sidewall channels. The larger quantum confinement-induced band splitting for the (110)-oriented sidewall channels results in more holes occupying the ground-state [3]. Thus, stress does not cause as much hole re-population as in the (001)-oriented top channel. At the same time, the density of states (DOS) at the Γ point increases significantly with stress for the (001)-oriented top channel, but does not change much for the (110)-oriented sidewall channels [3]. As a result, <$\bar{1}$10> compression induced by c-GST has a more pronounced effect on the top channel in terms of hole mobility enhancement.

The drain current enhancements for different fin rotations are shown in Fig. 3.17, where the rotated FinFETs with c-GST stressor are compared to control FinFETs of the same rotation. For each fin rotation, about 8-10 devices with L_G = 45 nm and W_{fin} = 40 nm are compared. The standard deviation of the enhancements is shown as error bars. The highest current enhancement (~75%) is seen in 0°-rotated FinFETs (<$\bar{1}$10> channel orientation). 45°-rotated (<010>-oriented) FinFETs with c-GST stressor show ~37% I_{Dsat} enhancement as compared to the control FinFETs of the same orientation. It has been theoretically and experimentally proven that <$\bar{1}$10> uniaxial compressive stress is more effective than stresses in other directions for enhancing hole mobility [11], leading

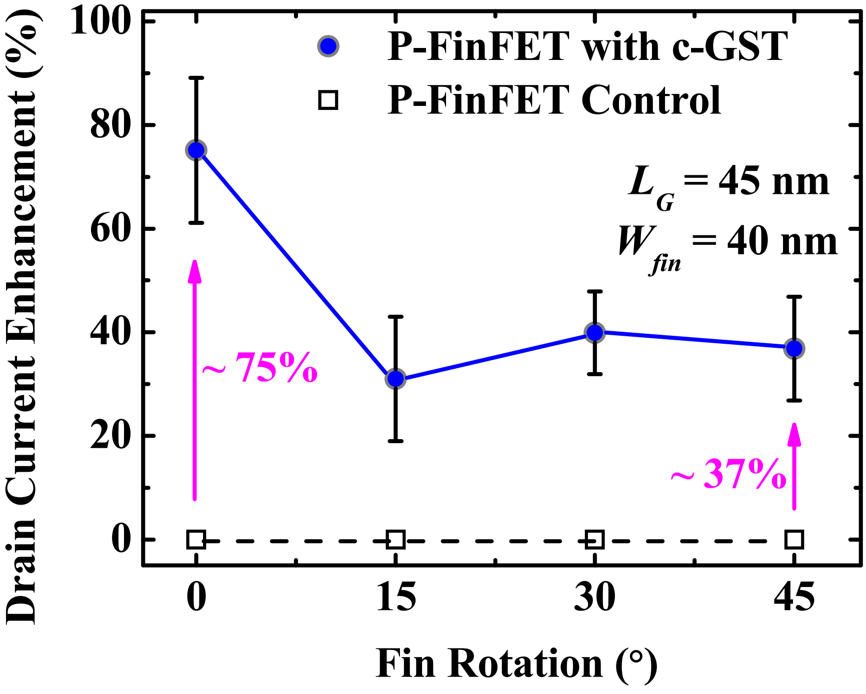


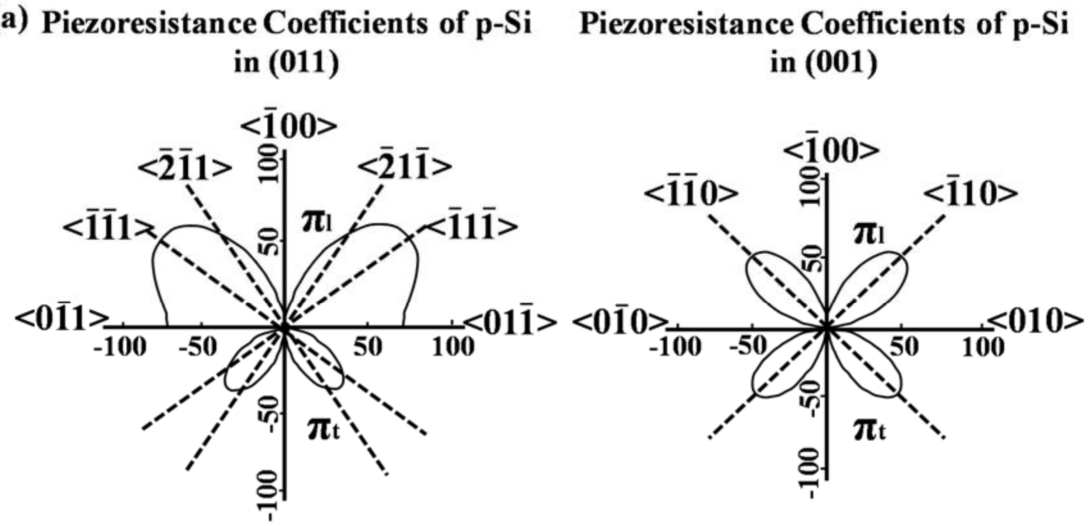
Fig. 3.17. Drain current enhancements at different fin rotations for p-FinFETs with L_G = 45 nm and W_{fin} = 40 nm. Significant I_{Dsat} (V_G = $V_{TH,sat}$ – 1.1 V, V_D = -1.2 V) enhancement induced by c-GST liner stressor is observed for different fin rotations, with the highest improvement observed for FinFETs with 0° fin rotation, i.e. fins oriented along $<\bar{1}10>$direction.

to the observed higher enhancement in the un-rotated FinFETs with $<\bar{1}10>$ orientation as compared to the rotated FinFETs.

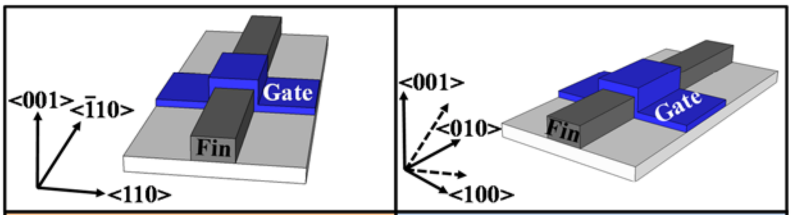
The difference in I_{Dsat} enhancement between 0°- and 45°-rotated FinFETs can also be explained by the directional dependence of the piezoresistance coefficients, as illustrated in Fig. 3.18(a), where the room temperature piezoresistance coefficients in the (011) and (001) planes of p-type bulk Si are shown, in units of 10^{-12} cm^2/dyne [59]. The relationship between resistivity ρ and stress σ is described by $\frac{\Delta\rho}{\rho} = \pi_l\sigma_l + \pi_t\sigma_t$, where

π_l and π_t are the piezoresistance coefficients in the longitudinal and transverse directions, respectively. σ_l and σ_t are the longitudinal and transverse stresses, respectively. For a given amount of compressive stress, a larger piezoresistance coefficient results in higher resistivity reduction in p-type Si.

(a)



(b)



0° Rotation				45° Rotation			
Sidewall Channels		Top Channel		Sidewall Channels		Top Channel	
π_l	π_t	π_l	π_t	π_l	π_t	π_l	π_t
72	0	70	0	9	0	9	0

Fig. 3.18. (a) Piezoresistance coefficients of p-type Si in the (011) and (001) planes, in units of 10^{-12} cm^2/dyne. (b) Piezoresistance coefficients of 0°- and 45°-rotated FinFETs, for both sidewall and top channels. Directional dependence of the piezoresistance coefficients is qualitatively consistent with the experimentally observed I_{Dsat} enhancement for FinFETs.

The piezoresistance coefficients of FinFETs with 0° and 45° fin rotations are summarized in Fig. 3.18(b). For FinFETs with 0° fin rotation, the sidewall channels have (110) surfaces and are <$\bar{1}$10>-oriented, with $\pi_l \approx 72$ and $\pi_t \approx 0$, while the top channel has a (001) surface and <$\bar{1}$10> orientation, with $\pi_l \approx 70$ and $\pi_t \approx 0$. On the other hand, in 45˚-rotated FinFETs, the piezoresistance coefficients are ~9 in the longitudinal direction and ~0 in the transverse direction for sidewall and top channels. The piezoresistance coefficients of the sidewall and top channels in 0˚-rotated FinFETs are higher than those in FinFETs with 45˚ fin rotation. Using the piezoresistance coefficients, we now quantitatively compare the mobility enhancement due to GST-induced stress (assuming -1.3 GPa compressive longitudinal stress). For simplicity, we use the bulk values for π_l and π_t, though technically piezoresistance coefficients should take into account the two-dimensional (2D) nature of transport in MOSFETs and depend on temperature and doping [62],[155]. The calculated hole mobility enhancement for the un-rotated FinFET is ~94% and that for the 45°-rotated FinFET is ~12%. Thus, with the same amount of compressive strain in the channels (in the source-to-drain direction) induced by the c-GST stressor, FinFETs with a 0˚-rotated fin have higher resistivity reduction or mobility enhancement compared to 45˚-rotated FinFETs, which in turn explains the differences in current enhancement for FinFETs with different fin rotations in Fig. 3.17.

3.5 Conclusion

In this Chapter, a new GST liner stressor for performance enhancement of p-FinFETs, featuring stress enhancement by changing the phase of as-deposited amorphous GST to the crystalline state was demonstrated. I_{Dsat} enhancement of ~30% is observed for the FinFETs with α-GST liner over unstrained control FinFETs, due to the intrinsic compressive stress in α-GST. When phase-changed to crystalline state, the c-GST contracts and exerts additional stress on the channel region, increasing the hole mobility further and giving a higher I_{Dsat} enhancement of up to ~88% over the control. I_{Dsat} enhancement is higher for smaller L_G. The drain current enhancements for different fin rotations were also investigated, where the rotated FinFETs with c-GST stressor were compared with control FinFETs (without c-GST) of the same rotation. Significant I_{Dsat} enhancement was observed for strained FinFETs with various fin rotations, with the highest enhancement observed for 0°-rotated FinFETs due to the directional dependence of the piezoresistance coefficients.

Chapter 4

Lattice Strain Analysis of Silicon Fin Field-Effect Transistor Structures Wrapped by $Ge_2Sb_2Te_5$ Liner Stressor

4.1 Introduction

With scaling of the silicon metal-oxide-semiconductor field-effect transistor (MOSFET) into sub-20 nm technology nodes, the conventional planar device structure would be replaced by the multi-gate or fin field-effect transistor (FinFET) device structure, which has excellent control of short-channel effects (SCEs) [92]-[103]. To boost the switching speed or drive current of FinFETs, carrier mobilities may be enhanced by channel strain engineering [97]-[103],[156]-[157]. In Chapter 3, a new liner stressor comprising $Ge_2Sb_2Te_5$ (GST) was demonstrated for inducing strain in p-channel FinFETs, significantly increasing the hole mobility and drive current. Phase transformation of a GST layer which wraps around a Si fin can induce very high strain levels in the Si fin. In this Chapter, the strain distributions in such Si FinFETs in the source/drain (S/D) regions and in the channel under the metal gate are investigated. Localized strain at the nanometer scale can be quantified by techniques based on transmission electron microscopy (TEM), such as nano-beam diffraction (NBD) [118],[136]-[140]. NBD illuminates a TEM sample perpendicularly with a small (nanometer-sized) quasi-parallel electron beam. The small beam size focuses on a localized region, forming a diffraction pattern with sharp peaks at the back focal plane of an objective lens which may be used for strain analysis. The small beam size reduces background noise which might be contributed by the surrounding materials.

In this Chapter, Si FinFETs with various fin widths W_{fin} wrapped around by crystalline GST (c-GST) were fabricated on (001) Si wafers. The local strain distributions in the Si fins in the S/D regions and in the channel under the metal gate were examined using NBD, and compared with finite element simulation results. By measuring the shifts of the peaks in the diffraction pattern as compared to the diffraction pattern acquired in a reference unstrained region, the lattice strain in the fin can be obtained in <110> and <001> directions perpendicular to the electron beam [118]-[121].

Fabrication of strained FinFET structures with c-GST liner stressor is described in Section 4.2. In Section 4.3, the background knowledge of NBD is introduced, and physics of NBD from an assembly of atoms is explained. Section 4.4 discusses the details of numerical simulation for investigating the stress in the FinFET with GST liner stressor. The strain values in the <110> and <001> directions in the S/D and channel regions of the Si FinFET structures with GST stressor were examined by NBD, the results are documented in Section 4.5. Comparisons of the measured and the simulated strain values are also performed in Section 4.5. Section 4.6 summarizes the key results of this Chapter.

4.2 Fabrication of Strained FinFET Structure

Si FinFET structures were fabricated on bulk (001) Si substrate. Fins with width W_{fin} from 70 nm to 130 nm were patterned using electron beam lithography (EBL) followed by plasma etching to produce a fin height H_{fin} of 60 nm. EBL step was outsourced. The Si fins run along the $<\bar{1}10>$ direction. A FEI Quanta focused ion-beam (FIB) system was used to deposit a thin, 200 nm wide strip of Pt running perpendicular to and crossing the midpoint of each fin line. This Pt strip wraps around the fins in the same way a metal gate does. 70 nm of amorphous GST (α-GST) was deposited by sputtering, as shown in Fig. 4.1(a). A 200 °C low-temperature anneal was then performed to convert the α-GST to c-GST. As shown in Fig. 4.1(b), when the GST undergoes a phase change from α-GST to c-GST, its volume reduces by ~7.0% as shown in Chapter 3, causing it to tighten its grip on the fin structure and thus exerting a compressive stress on the fin. Two-dimensional (2D) schematics of the fin cross-section in the A-A' and B-B' planes illustrate the large compressive <110> strain in the fin S/D regions and in the channel region under the metal gate, respectively, that can result from contraction of the GST. A cross-sectional SEM image in the A-A' plane and a TEM image in the B-B' plane are also shown in Fig. 4.1(b). The FinFET-like structure with a Pt strip wrapping around the fin as a gate was used for NBD strain analysis only, in order to have a quick assessment of the GST induced strain in the FinFET-like structure. The stress induced by Poly-Si gate in the FinFET and Pt gate in the FinFET-like test structure would be different. However, as large stress is induced by GST liner contraction, the gate-induced stress would not significantly affect the channel stress.

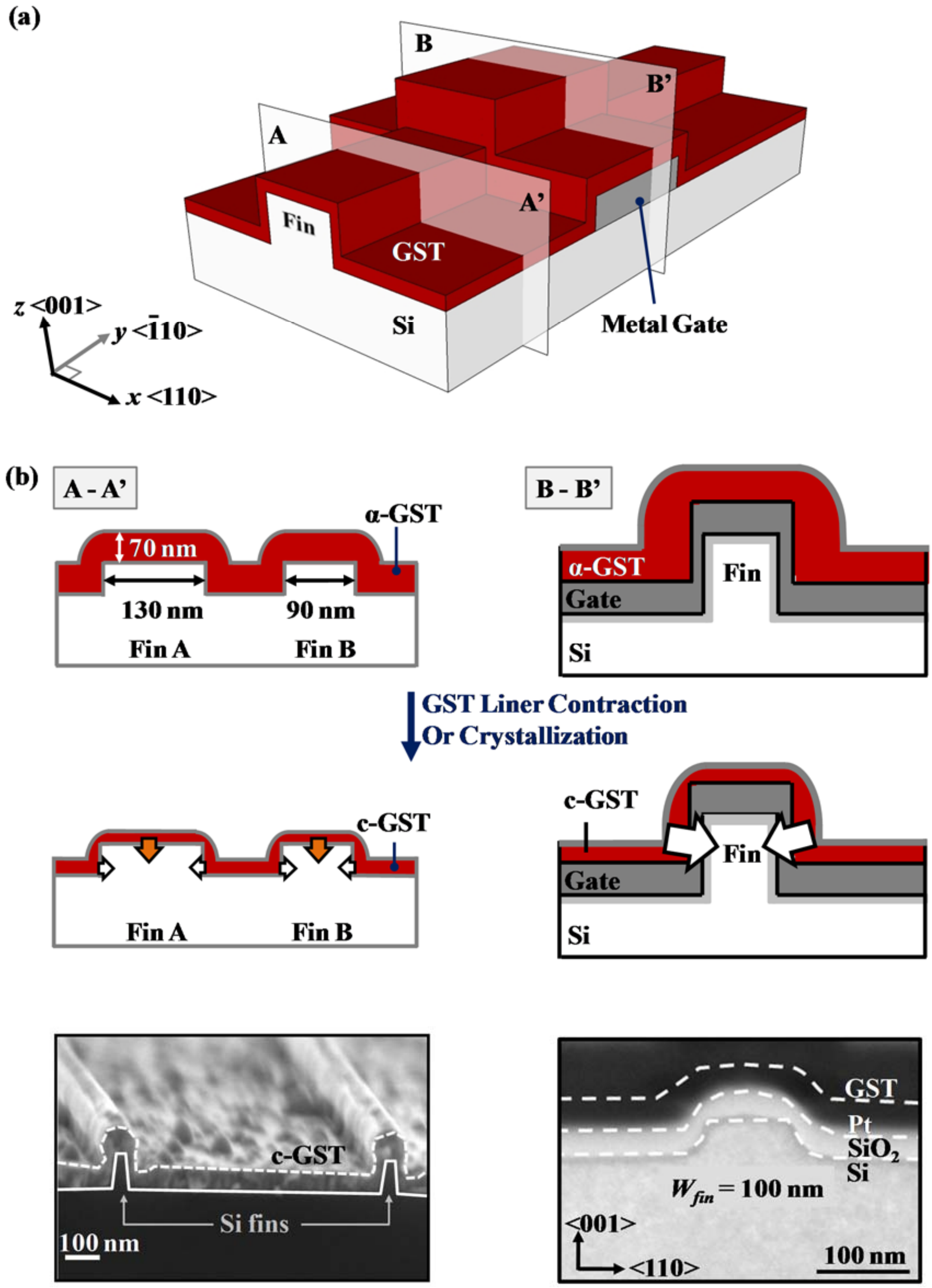


Fig. 4.1. (a) 3D schematic of a FinFET wrapped around by a GST liner stressor. Coordinate axes are also shown. When GST crystallizes, its volume is reduced by ~7%. (b) 2D schematics of the fin cross-section in the A-A’ and B-B’ planes illustrate the large compressive <110> strain in the S/D regions and in the channel region under the metal gate, respectively, that can result from contraction of the GST. A cross-sectional SEM image in the A-A’ plane and a TEM image in the B-B’ plane are also shown. TEM service was outsourced.

4.3 Strain Measurement Using Nano-Beam Diffraction

A FEI Titan microscope was used for strain measurement using TEM scan mode operated at 300 kV. The small quasi-parallel beam illumination for NBD was achieved using the microscope's three condenser lens system [118],[121]. In this study, a gun lens was used to reduce the beam current. A condenser with an aperture of 20 μm was used and a convergence angle of ~0.2 mrad was obtained, resulting in a probe size of ~0.5 nm. A larger convergence angle can be used to obtain a smaller probe size using the current setting, but a larger convergence angle gives larger diffraction spots which will complicate the peak localization [119].

Fig. 4.2(a) shows a TEM image of Si fin structures wrapped around by the c-GST stressor. The image allows accurate positioning of the electron beam. The specimen used here was relatively thick (~500 nanometers) to prevent strain relaxation. However, a thick specimen leads to blurred diffraction patterns which result from a combination of inelastic scattering and chromatic aberration of the TEM optics [119],[120]. Therefore, in order for the peaks to be localized accurately, energy filtering of the diffraction pattern was used to eliminate the blurring effect. Diffraction patterns were recorded by a 2048 × 2048 pixels charge-coupled device (CCD) camera at a series of ten reference points in the Si substrate far (~1 μm) from the strained fins. The silicon region where these ten reference points are located should be relaxed. In the nanoscale regime, diffraction patterns are more easily affected by the surrounding materials, which leads to a higher noise level in the diffraction pattern formed. To enhance the signal, we performed the NBD scan on a point basis for a prolonged period instead of line scanning. However, the risk of sample drift increases due to the prolonged acquisition time, which may affect the measurement accuracy of NBD [136]. In this study, the average exposure time for each acquired diffraction pattern is ~1 s.

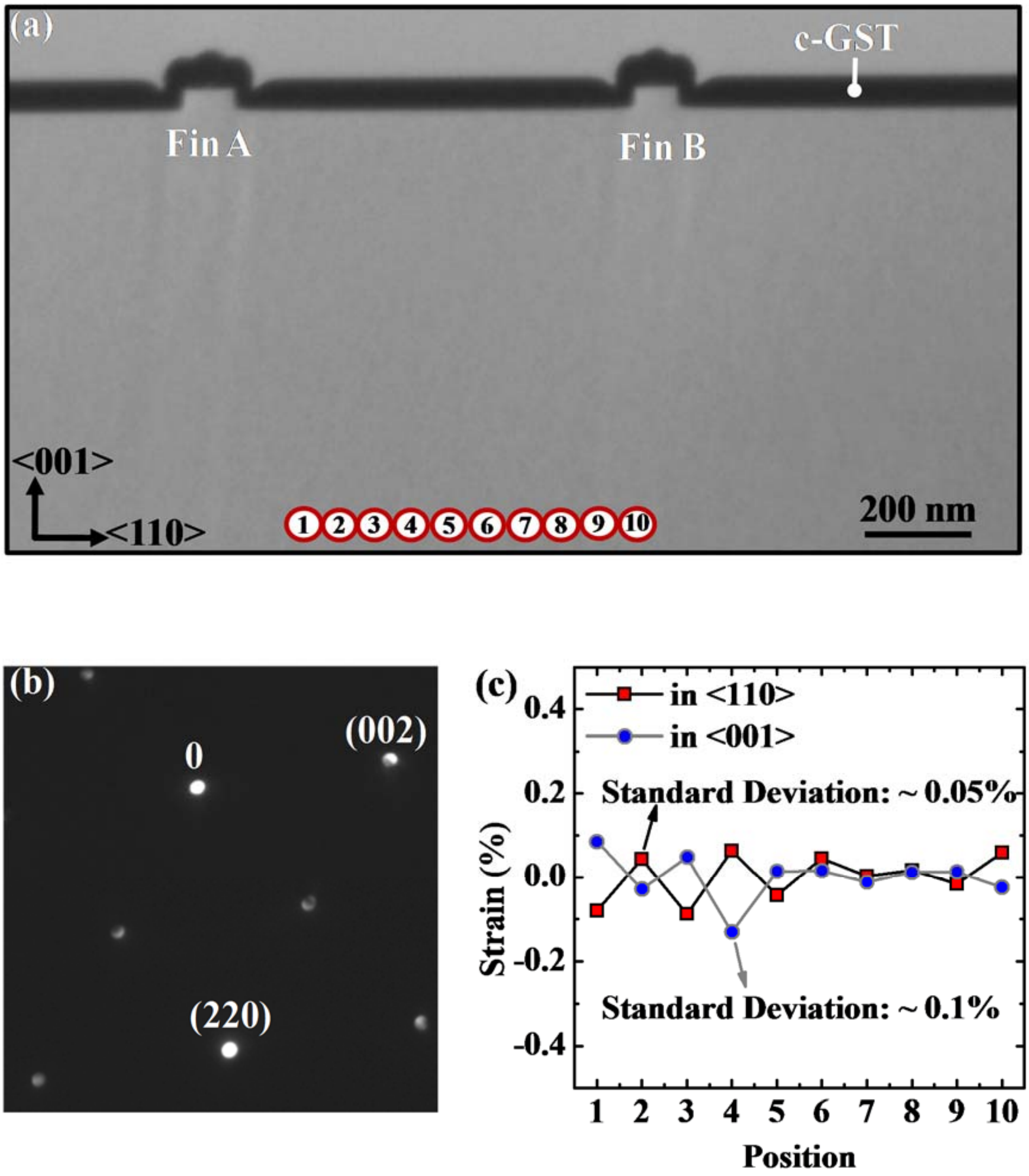


Fig. 4.2. (a) A TEM image showing a cross-sectional view of the Si fin structures with different W_{fin} wrapped around by c-GST stressor. A series of points (labeled 1 to 10) far from the strained Si fins is selected to generate (b) diffraction patterns as reference. Silicon is expected to be unstrained at the positions of points 1 to 10. (c) Strain values at the reference points show a standard deviation of 0.05% in the <110> direction and 0.1% in the <001> direction. TEM was outsourced.

The TEM tool used has outstanding mechanical and electrical stabilities which contribute to negligible sample drift. In addition, the small convergence angle achieved and the energy filtering used help to ensure high NBD measurement accuracy. NBD measurements were repeated at the same spot or location to confirm the measurement accuracy. The NBD analysis by Dr. DU Anyan of GLOBALFOUNDRIES is acknowledged.

The physics of nano-beam diffraction from an assembly of atoms will be discussed next. The potential $V(r)$ of an assembly of atoms can be written as a convolution of the potential of an individual atom $V^a(r)$ and the positions of atoms described by the delta function $\delta(r - R_h)$ [121]:

$$V(r) = V^a(r) \otimes \sum_h \delta(r - R_h)\ , \tag{4.1}$$

where r is a vector in 3D space, and R_h determines the atomic positions. The summation is used to include h number of atoms in an assembly [121]. The Fourier transform of $V(r)$ is known as the structure factor and is given by [121]:

$$\mathcal{F}[V(r)] = f(J)P(S)\sum_h e^{(-2\pi i S\cdot r_h)}. \tag{4.2}$$

Here f is the atomic scattering factor, P is the thermal factor which accounts for the effect of thermal vibrations and static disorder on atomic scattering, and J is the scattering vector. For crystals, the term $\sum_h e^{(-2\pi i S\cdot r_h)}$ in Equation (4.2) defines an array of diffraction peaks, which depends on the atomic position in real space. The structure factor also determines the intensity of the diffraction peaks. The diffraction peak position is defined by the crystal's reciprocal lattice:

$$g = w - w_0 = la^* + mb^* + nc^*\ , \tag{4.3}$$

where g is a reciprocal lattice vector, w and w_0 are the incident and diffracted electron wave vectors, respectively, and a^*, b^*, and c^* are the reciprocal lattice vectors of the crystal. l, m, and n are integers. The shape of the diffraction peak is determined by the electron probe in reciprocal space:

$$\mathcal{F}[\Phi_s(r)] \otimes \mathcal{F}[V(r)] = \mathcal{F}[V(r)]\{\mathcal{F}[\Phi_s(r)] \otimes \textstyle\sum_{l,m,n}\delta(J - la^* - mb^* - nc^*)\}, \qquad (4.4)$$

where $\mathcal{F}[\Phi_s(r)]$ is the Fourier transform of the electron source wave function [121]. The term $\sum_{l,m,n}\delta(S - la^* - mb^* - nc^*)$ defines the geometry of the diffraction pattern.

For example, a diffraction pattern from one of the relaxed Si reference points is shown in Fig. 4.2(b). The shape of the diffraction peak is defined by the electron probe in reciprocal space, as in Equation (4.4). The intensity and the position of the peaks are determined by the structure factor [Equation (4.2)] and the crystal reciprocal lattice [Equation (4.3)], respectively. The separation between the center *0* (the dc component of the image intensity) and a diffraction peak is directly proportional to the reciprocal of the atomic spacing in the direction from *0* to that peak. Thus, the (220) and (002) peaks contain information on atomic spacing in the horizontal <110> and vertical <001> directions, respectively [141]. Fig. 4.2(c) shows the strain in the <110> and <001> directions from the ten reference points indicated in Fig. 4.2(a). The standard deviation s of the strain values at the ten reference points can be used to estimate the accuracy of NBD [158], as below:

$$s = \sqrt{\frac{\sum_{i=1}^{N_{Ref}} d_i^2}{N_{Ref}} - \left(\frac{\sum_{i=1}^{N_{Ref}} d_i}{N_{Ref}}\right)^2}\ , \qquad (4.5)$$

where i is an integer, N_{Ref} is the number of reference points taken, and d_i is the separation between the center 0 and a diffraction peak in a particular direction of the i^{th} reference point measured. In this study, very high NBD measurement accuracy of 5×10^{-4} in the <110> direction and 1×10^{-3} in the <001> direction were achieved [Fig. 4.2(c)].

For strained crystals, to calculate the percentage change in the lattice constants (i.e. the strain components), we employ:

$$\varepsilon_{<110>} = \frac{a_{<110>} - a_{<110>,Ref}}{a_{<110>,Ref}}, \tag{4.6a}$$

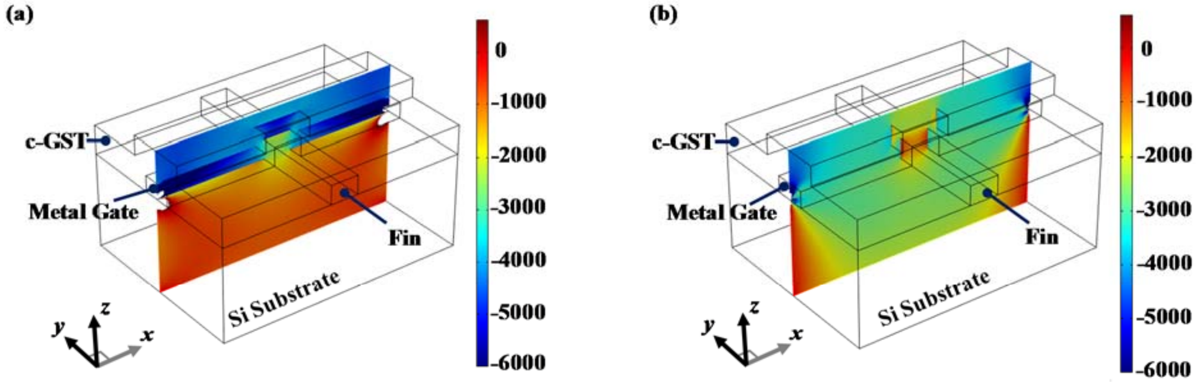
$$\varepsilon_{<001>} = \frac{a_{<001>} - a_{<001>,Ref}}{a_{<001>,Ref}}, \tag{4.6b}$$

where $a_{<110>}$ and $a_{<001>}$ are the lattice constants of the strained crystal in the <110> and <001> directions, respectively. $a_{<110>,Ref}$ and $a_{<001>,Ref}$ are the averaged lattice constants of the unstrained reference crystal (the ten reference points in Fig. 4.2) in the <110> and <001> directions, respectively.

4. 4 Simulation Details

Three-dimensional (3D) numerical simulations were performed to investigate the stress in the FinFET channel under the metal gate by a simulation tool named COMSOL. A non-uniform finite element grid was used, with smaller grid size at regions where the stress gradient is larger. The boundary conditions are such that the bottom and sides of the Si substrate and sides of c-GST layer are rigid. The sides of the domain are assumed to have zero horizontal displacements since they are bounded by huge adjacent volumes. The contraction of the c-GST layer was simulated using the framework of thermoelasticity [133],[134].

Fig. 4.3 shows the 3D numerical simulation results for a FinFET (W_{fin} = 130 nm) with 60-nm-thick GST liner stressor. Fig. 4.3 (a) and (b) are the distributions of the horizontal stress σ_{xx} and vertical stress σ_{zz}, respectively, on the x-z plane along the center of the gate. Fig. 4.3 (c) and (d) are the zoomed-in views of the fin area for σ_{xx} and σ_{zz}, respectively, showing very high compressive σ_{xx} and σ_{zz} in the FinFET channel under the metal gate, induced by the contraction of the GST.



(c) Distribution of σ_{xx}

(d) Distribution of σ_{zz}

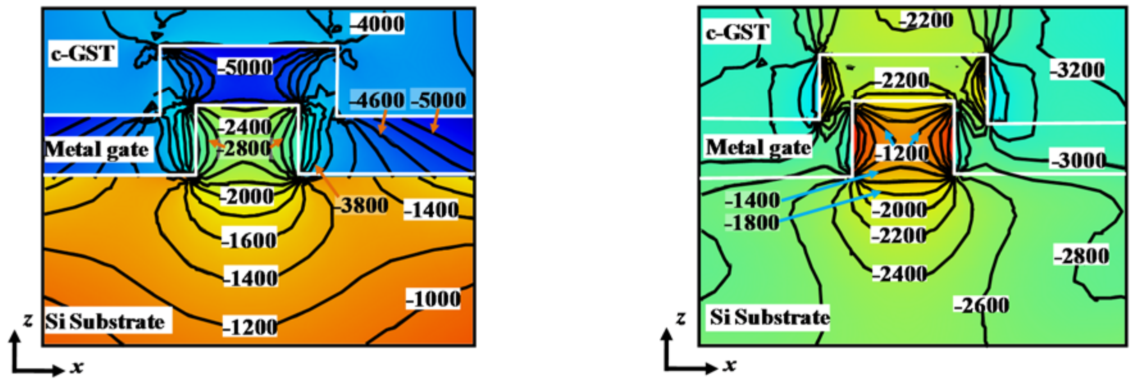


Fig. 4.3. 3D numerical simulation of a FinFET (W_{fin} = 130 nm) with GST liner stressor. (a) and (b) are the distributions of the horizontal stress (σ_{xx}) and vertical stress (σ_{zz}), respectively, on the x-z plane along the center of the gate. (c) and (d) are the zoomed-in view of the fin area for σ_{xx} and σ_{zz}, respectively.

Elasticity defines the relationship between stress σ and strain ε. For small deformations, this relationship is described by Hooke's law in terms of stiffness F or compliance S [159]:

$$\sigma = F \cdot \varepsilon\,, \tag{4.7a}$$

$$\varepsilon = S \cdot \sigma. \tag{4.7b}$$

For isotropic uniaxial cases, stiffness F can be represented by a single value of Young's modulus Y. In an anisotropic material like Si, a tensor written in 6×6 matrix notation is required to describe the elasticity. In the simulation, by providing the compliance matrix of a standard (001) Si wafer [i.e. x, y and z axes are in the <110>, <$\bar{1}$10> and <001> directions, as shown in Fig. 4.1 (a)], the simulated strain values can be converted from the associated simulated stress values by the simulator [159]:

$$\begin{pmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{yz} \\ \varepsilon_{zx} \\ \varepsilon_{xy} \end{pmatrix} = \begin{pmatrix} 5.92 & -0.38 & -2.14 & 0 & 0 & 0 \\ -0.38 & 5.92 & -2.14 & 0 & 0 & 0 \\ -2.14 & -2.14 & 7.69 & 0 & 0 & 0 \\ 0 & 0 & 0 & 12.56 & 0 & 0 \\ 0 & 0 & 0 & 0 & 12.56 & 0 \\ 0 & 0 & 0 & 0 & 0 & 19.65 \end{pmatrix} \begin{pmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{yz} \\ \sigma_{zx} \\ \sigma_{xy} \end{pmatrix} .$$

$$(\text{in } 1\times10^{-12}\ \text{Pa}^{-1}) \tag{4.8}$$

4.5 Strain Measurement Results and Discussions

The strain values in the <110> and <001> directions in the S/D and channel regions of the Si FinFET structures with c-GST stressor were examined by NBD. Fig. 4.4(a) shows the S/D region of Si fin A (W_{fin} = 130 nm), which is wrapped by 66-nm-thick c-GST stressor. Five points A_1-A_5 were selected for NBD strain analysis.

Generally, fin *A* is compressively strained by the c-GST stressor in the horizontal <110> direction [Fig. 4.4(b)]. For example, horizontal <110> compressive (negative) strain $\varepsilon_{<110>}$ of -0.88% is observed at point A_4. Therefore, the atomic spacing in the <110> direction at point A_4 is 0.88% smaller than that in the reference region. Fig. 4.4(c) shows the vertical <001> compressive strain observed at points A_1 to A_5. Similar to the <110> direction, the highest <001> strain $\varepsilon_{<001>}$ of -1.41% is observed at point A_4. Numerical simulation was performed to check the consistency of the NBD strain results for fin *A*. Fin *A* has a slightly slanted fin profile and a slightly asymmetrical GST profile, which have been considered in the simulation. The magnitude of $\varepsilon_{<110>}$ and $\varepsilon_{<001>}$ not being the highest in the middle of the fin (point A_3) could be due to the slight asymmetry of the structure. Fig. 4.4 (b) and (c) also compare the simulated horizontal strain ε_{xx} and vertical strain ε_{zz} with the measured ones using NBD for points A_1-A_5. The simulated strain values were converted from the simulated stress values by the simulator using the compliance matrix [Equation (4.8)]. Generally, the simulated strain values are comparable with the measured ones in fin *A*. However, a large difference was observed for point A_1 between the simulated and measured strain value. During the preparation of the TEM sample for NBD strain analysis, the sample thickness will affect the stress in the sample as mentioned above. Moreover, considering the nanometer scale fin structures in the NBD analysis, diffraction patterns could be easily affected by the surrounding materials and leads to noises in the diffraction pattern and inaccuracy of localizing the peaks. Although we have done the NBD scan on a point basis to compensate for the effects, high level of noises are expected in the diffraction pattern for certain points. Point A_1 might have encountered some stress loss due to the facts mentioned above. On the other hand, the strain values from the simulation did not take the noises or stress loss into account. Difference in the simulated and measured strain values is expected at certain points. Nevertheless, both simulated and measured strain shown that point A_1 is compressively strained.

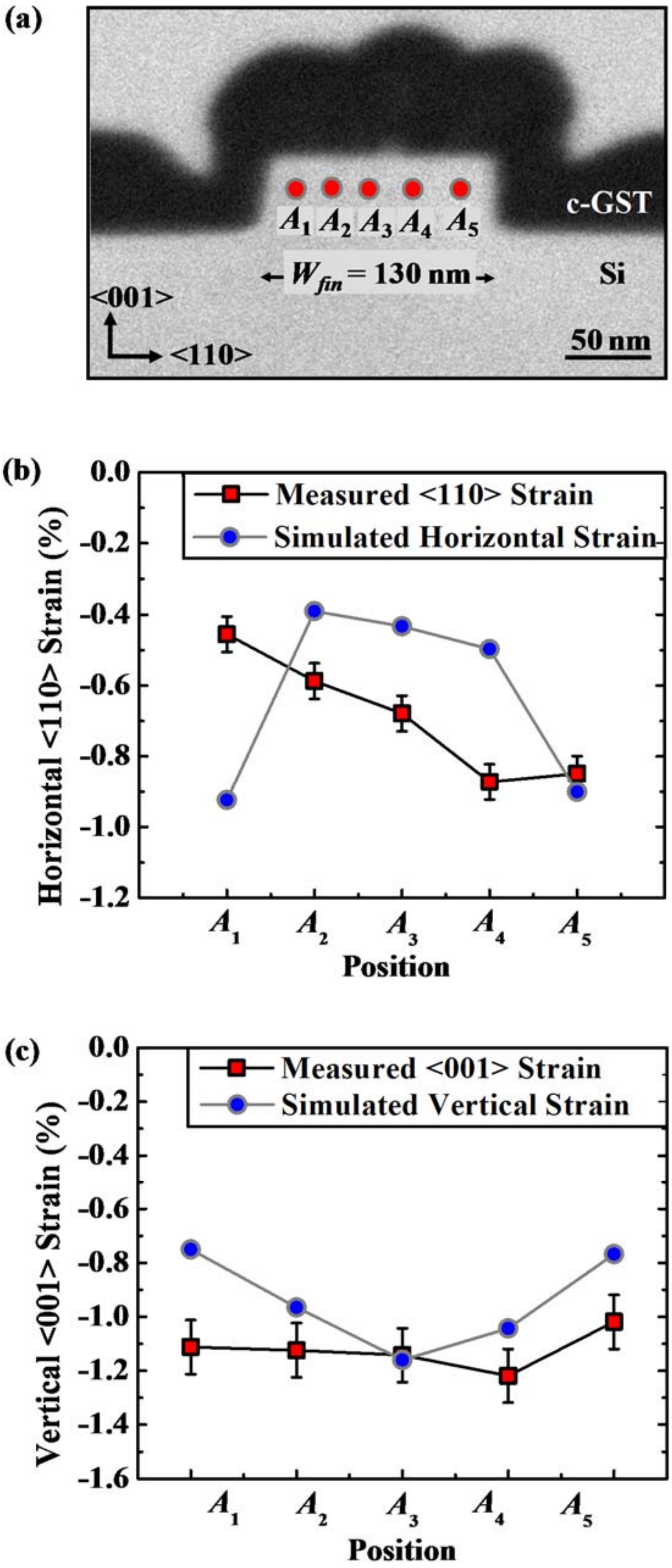


Fig. 4.4. (a) TEM image of Si fin A (W_{fin} = 130 nm) with 66-nm-thick c-GST stressor. Five points A_1-A_5 were selected for NBD strain measurements. The measured and simulated strain values in fin A in the (b) horizontal <110> and (c) vertical <001> directions are plotted.

Fig. 4.5(a) shows a TEM image of the S/D region of Si fin *B* with W_{fin} = 90 nm, wrapped by a 66-nm-thick c-GST stressor. Eight points were selected for NBD strain analysis as shown. Fig. 4.5(b) reveals that the horizontal <110> strain at all eight points is compressive, as compared to the reference region. The highest <110> compressive strain of -1.15% is observed at point B_5 near the sidewall of Si fin *B*. A comparable <110> compressive strain is observed at point B_8 near the other sidewall of Si fin *B*. However, the magnitudes of the <110> compressive strain are smaller at point B_1, and at points B_2, B_3, B_6, and B_7 at the center of fin *B*. NBD measurements were performed only at points B_5-B_8 for vertical <001> strain in fin *B*, as shown in Fig. 4.5(c). Large compressive <001> strain at points B_5-B_8 were observed. Also, in Fig. 4.5 (b) and (c), the simulated horizontal strain ε_{xx} and vertical strain ε_{zz} for points B_1- B_8 are shown. The slanted fin profile and asymmetrical GST profile with uneven GST on top of the fin have been considered in the simulation. As shown in Fig. 4.5 (b) and (c), we see that the measured strain distribution in fin B is very consistent with the simulation result.

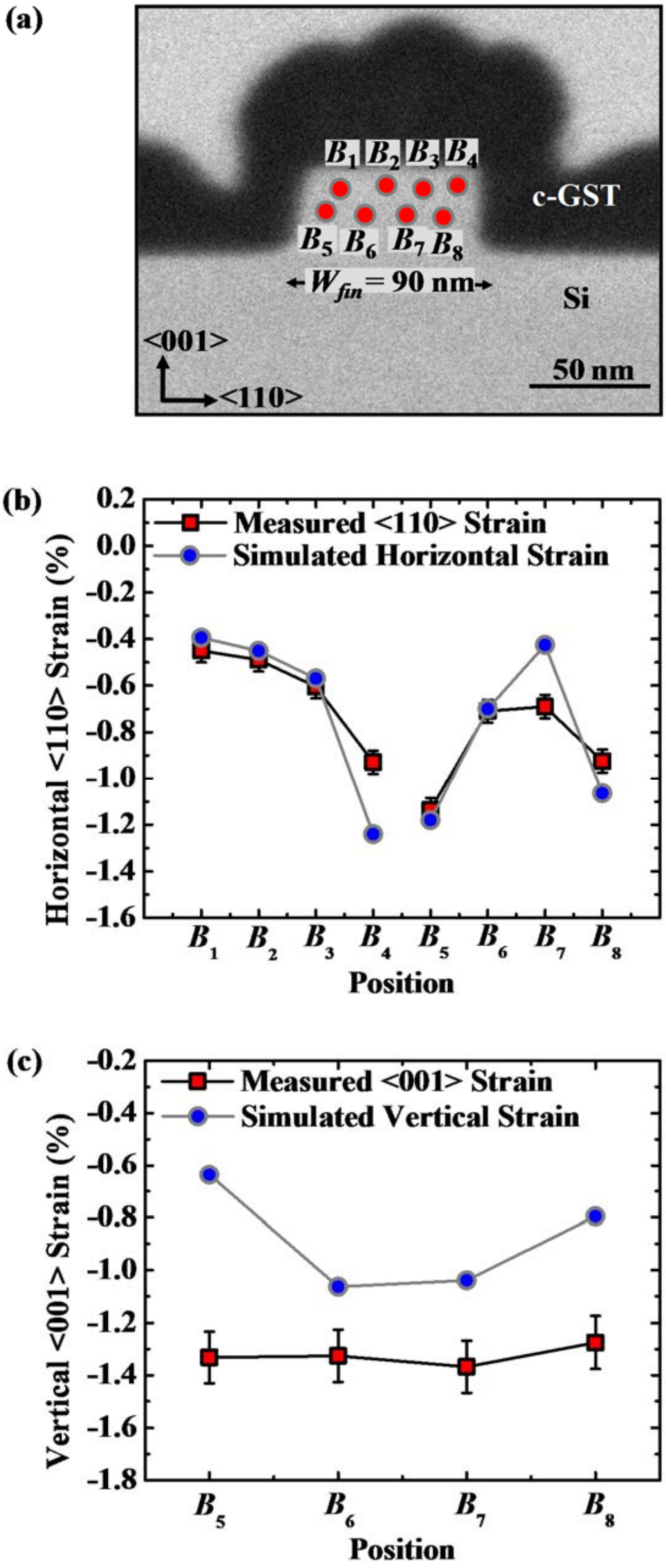
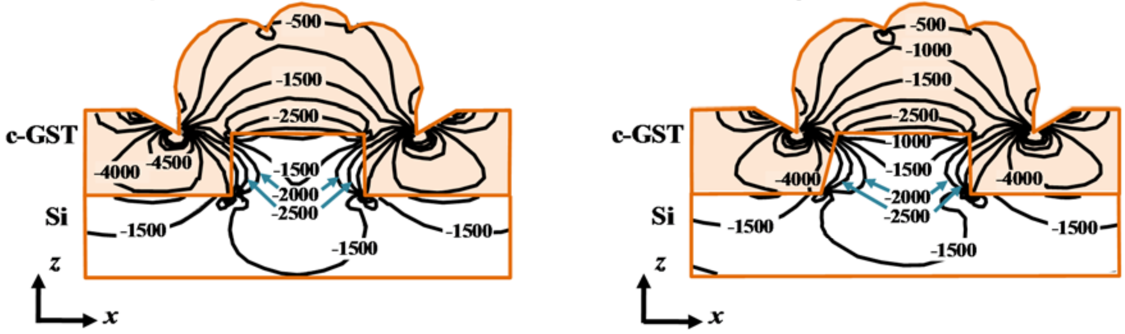


Fig. 4.5. (a) TEM image of Si fin *B* (W_{fin} = 90 nm) with 66-nm-thick c-GST stressor. Eight points B_1-B_8 were selected for NBD strain measurements. (b) Measured and simulated strain values in fin *B* in the horizontal <110> direction. (c) Measured and simulated strain values at points B_5-B_8 in the vertical <001> direction.

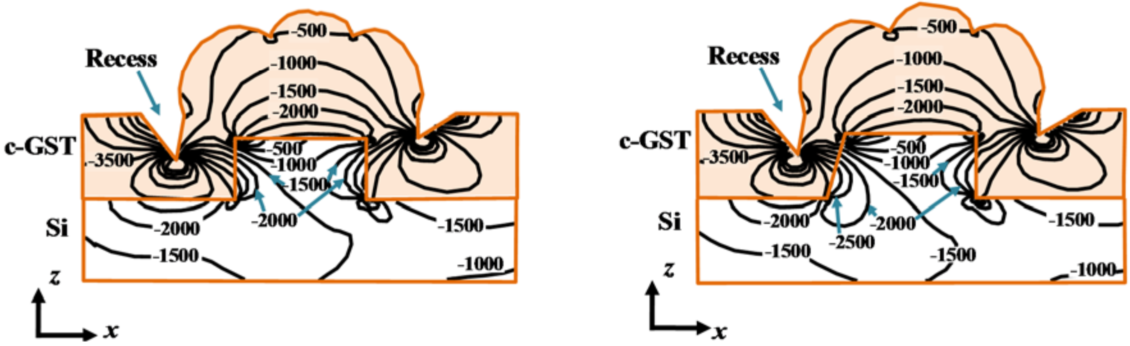
To study the effects of the Si fin and GST profiles on the stress distribution, 2D structures with different fin and GST profiles were simulated to investigate the stress in the S/D regions of Si fins (W_{fin} = 90 nm) wrapped around by 60-nm-thick c-GST stressor, as shown in Fig. 4.6. While a 3D simulation is needed to simulate the stress in the FinFET channel under the metal gate due to the short gate length, which cannot be taken as infinite, a 2D simulation is sufficient for the S/D regions of Si fins. The 2D simulation conditions are the same as those used in the 3D simulation in Fig. 4.3. Simulation results show that high compressive horizontal stress σ_{xx} is observed for all the various fin and GST profiles, but with different σ_{xx} distributions in fins with different fin and GST profiles.

Fig. 4.6 (a) and (c) have a vertical fin profile, while Fig. 4.6 (b) and (d) have a fin profile that is slanted on the left side. Fig. 4.6 (a) and (b) have a symmetric GST profile, while Fig. 4.6 (c) and (d) have an asymmetric GST profile (i.e. the GST recess on the left of the fin is deeper as compared to that on the right of the fin). Uneven GST profile on the fins [as observed in Fig. 4.5(a)] has been considered in the simulation. For fins with a vertical fin profile, symmetric GST profiles induce symmetric σ_{xx} distributions in the Si fins, while asymmetric GST profiles lead to asymmetric σ_{xx} distributions due to the deeper GST recess on the left of the fin causing the -1500 MPa contour lines to shift more towards the centre of the fin [Fig. 4.6 (a) and (c)]. Fins with a slanted fin profile on the left side result in asymmetric σ_{xx} distributions, regardless of the symmetry of the GST profile [Fig. 4.6 (b) and (d)]. Comparing the σ_{xx} distributions in Fig. 4.6 (a) and (c) to those in Fig. 4.6 (b) and (d), the -2000 MPa contour lines at the slanted side of the fin extend towards the centre of the fin, indicating that having a slanted fin structure would increase the stress at the centre of the fin. Thus, the asymmetrical NBD-measured strain distribution on fin *B* [Fig. 4.5(b)] can be well explained by the asymmetrical stress distribution (or contours) resulting from the slanted fin profile and asymmetrical GST profile, as shown in Fig. 4.6(d).

The strain in the FinFET channel region is examined next. Fig. 4.7(a) shows the TEM image of Si fin *A'* (W_{fin} = 130 nm) in the FinFET channel region covered by metal gate, and with 66-nm-thick c-GST stressor. Ten points *A'*$_1$-*A'*$_{10}$ were selected for NBD strain measurements. The strain values in fin *A'* in the <110> and <001>



(a) Vertical fin, symmetric GST **(b) Slanted fin, symmetric GST**



(c) Vertical fin, asymmetric GST **(d) Slanted fin, asymmetric GST**

Fig. 4.6. 2D numerical simulation results showing the different horizontal stress σ_{xx} distributions in Si fins (W_{fin} = 90 nm) wrapped around by 60-nm-thick GST liner stressor with different fin and GST profiles. (a) and (c) have a vertical fin profile while (b) and (d) have a fin profile that is slanted on the left side. (a) and (b) have a symmetric GST profile, while (c) and (d) have an asymmetric GST profile (i.e. the GST recess on the left of the fin is deeper and sharper as compared to that on the right of the fin). Uneven GST profile on the fins [as observed in Fig. 4.5(a)] has been considered in the simulation.

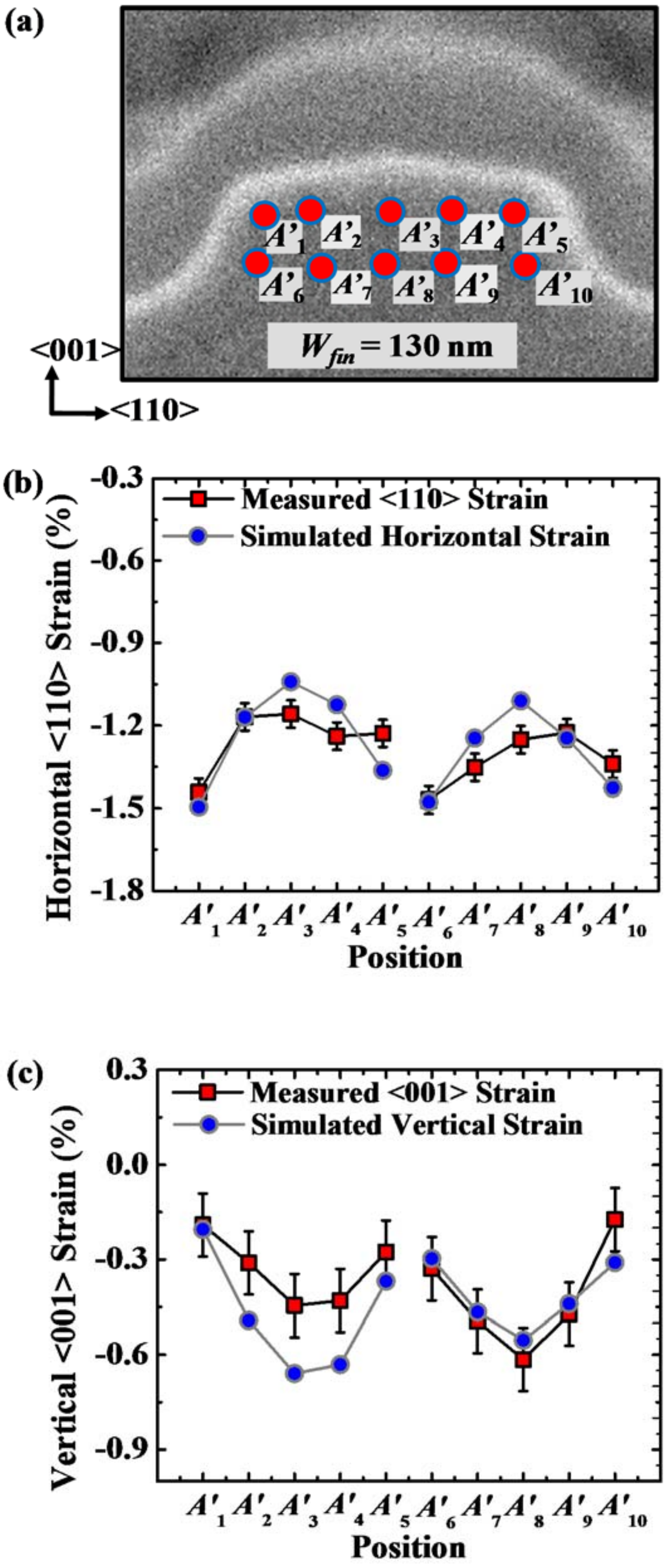


Fig. 4.7. (a) TEM image of Si fin *A'* (W_{fin} = 130 nm) covered by metal gate, and with 66-nm-thick c-GST stressor. Ten points *A'*$_1$-*A'*$_{10}$ were selected for NBD strain measurements. The measured and simulated strain values in fin *A'* in the (b) horizontal <110> and (c) vertical <001> directions are plotted.

directions are plotted in Fig. 4.7 (b) and (c), respectively. The horizontal <110> compressive strain is higher at the sidewalls of fin *A'* (e.g. -1.47% at point A'_6) and lower near the centre of fin *A'* (e.g. -1.15% at point A'_3) [Fig. 4.7(b)], while the vertical <001> compressive strain is lower at the sidewalls (e.g. -0.32% at point A'_6) and higher near the center (e.g. -0.61% at point A'_8) [Fig. 4.7(c)]. The trends observed in the NBD measurements are shown to be consistent with the 3D numerical simulation results [Fig. 4.3] for points A'_1-A'_{10} plotted in Fig. 4.7 (b) and (c) for the simulated horizontal strain ε_{xx} and vertical strain ε_{zz}, converted by the simulator using the compliance matrix from the simulated stress σ_{xx} and σ_{zz} shown in Fig. 4.3 (c) and (d), respectively.

A TEM image of Si fin *B'* (W_{fin} = 90 nm) in the FinFET channel region covered by metal gate, and with 66-nm-thick c-GST stressor, is shown in Fig. 4.8(a). Six points B'_1-B'_6 were selected for NBD strain analysis. Fig. 4.8 (b) and (c) show the horizontal <110> and vertical <001> strain values at points B'_1-B'_6, respectively. A 3D simulation was performed for fin *B*' (FinFET with W_{fin} = 90 nm) covered by 60-nm-thick c-GST stressor, to investigate the strain distributions. The simulation conditions were similar to those in Fig. 4.3. Also, the simulated horizontal strain ε_{xx} and vertical strain ε_{zz} for points B'_1-B'_6 are plotted in Fig. 4.8 (b) and (c), respectively. Similar to what was observed in fin *A'*, the horizontal <110> compressive strain is higher at the sidewalls of fin *B'* (e.g. -1.44% at point B'_6) and lower near the centre of fin *B'* (e.g. -0.81% at point A'_2) [Fig. 4.8(b)], while the vertical <001> compressive strain is lower at the sidewalls (e.g. -0.25% at point B'_1) and higher near the center (e.g. -0.51% at point B'_5) [Fig. 4.8(c)]. The simulated strain at points B'_1-B'_6 are consistent with the trends observed in the measured strain.

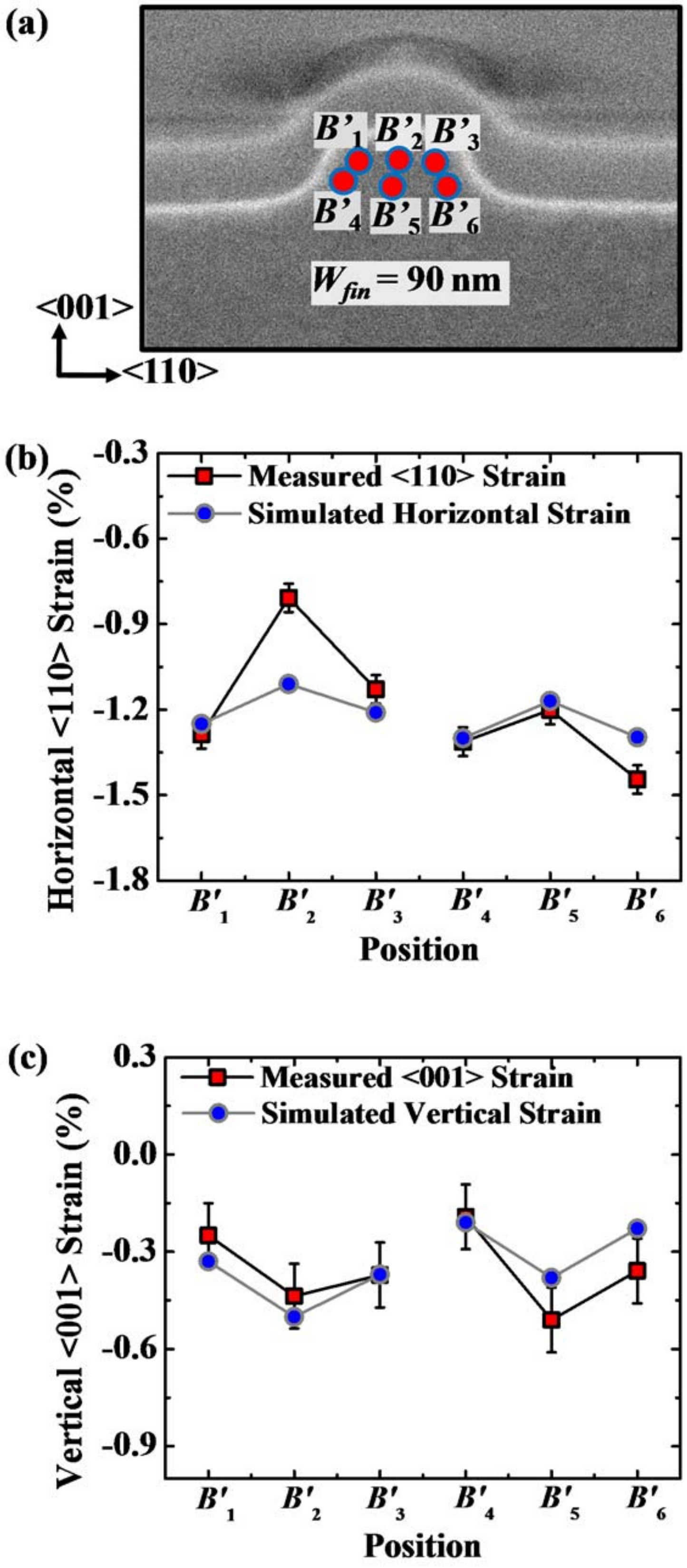


Fig. 4.8. (a) TEM image of Si fin *B'* (W_{fin} = 90 nm) covered by metal gate, and with 66-nm-thick c-GST stressor. Six points B'_1-B'_6 were selected for NBD strain measurements. The measured and simulated strain values in fin *B'* in the (b) horizontal <110> and (c) vertical <001> directions are plotted.

A point worth noting is that the c-GST stressor induces larger horizontal <110> compressive strain but lower vertical <001> compressive strain in the FinFET channel region under the metal gate (fins *A'* and *B'*) than in the S/D region (fins *A* and *B*). This could be attributed to the compressive stress in the <110> direction induced in the FinFET channel region by the metal gate [160]. Consequently, the increased compressive <110> strain results in reduction of the <001> compressive strain in the channel region.

4.6 Conclusion

In summary, the local strain components in the <110> and <001> directions in Si fins in the S/D (fins *A* and *B*) and channel (fins *A'* and *B'*) regions of <$\bar{1}10$>-oriented FinFET structures wrapped around by a c-GST stressor were investigated using NBD technique for the first time. Crystallization of as-deposited α-GST causes it to contract and induce large <110> and <001> compressive strain components in the Si fins in the S/D and channel regions. In the channel region, the <110> compressive strain is higher at the fin sidewalls and lower near the centre of the fin, while the <001> compressive strain is lower at the sidewalls and higher near the center. In addition, the c-GST stressor induces higher horizontal <110> compressive strain but lower vertical <001> compressive strain in the FinFET channel region under the metal gate (fins *A'* and *B'*) than in the S/D region (fins *A* and *B*). Moreover, the effects of the Si fin geometry and GST profile on the stress distribution were studied using simulation. It was found that having a slanted fin structure would increase the stress at the centre of the fin.

Chapter 5

An Expandable ZnS-SiO$_2$ Liner Stressor for N-Channel FinFETs

5.1 Introduction

FinFETs have excellent control of short-channel effects (SCE) [90]-[95],[97],[103] and have been adopted at the 22 nm technology node [96],[104]. To enhance the drive current I_{Dsat} of n-channel FinFETs (n-FinFETs), silicon:carbon (Si:C) source/drain stressors [98],[100],[108],[109] have been reported. The concept of Si:C source/drain stressors was first demonstrated in year 2004 [22]. Conventional high tensile-stress silicon nitride (SiN) liner stressor or contact etch stop layer has been studied extensively for strain engineering in n-FinFETs [99]-[101]. In preceding Chapters, a new class of stressor using phase-change material $Ge_2Sb_2Te_5$ (GST) was demonstrated as volume-change liner stressor in contraction mode for p-channel FinFETs. Unlike the conventional liner stressor which exploits intrinsic stress, GST was formed to wrap around the FinFET and then configured to change volume post-deposition, so as to induce mechanical compressive stress in the FinFET channel, leading to very high I_{Dsat} enhancement. However, this volume-change liner stressor material was only developed for p-channel FinFETs.

In this Chapter, we report a new volume-change liner stressor material, ZnS-SiO$_2$, for strain engineering of Si n-FinFETs. ZnS-SiO$_2$ expands during thermal anneal, and is the counterpart of GST and GeTe [161] volume-change liner stressors for strain engineering in n-FinFETs, exploiting expansion of the liner material to create large tensile stress in the channel. ZnS-SiO_2 liner was integrated on n-FinFETs with Si:C S/D stressors and Al-incorporated NiSi contacts, and a low-temperature anneal was performed to induce expansion of the ZnS-SiO_2.

In Section 5.2, the key concept of using ZnS-SiO_2 as an expandable liner stressor is discussed. Finite-element simulations were performed to investigate the stress in FinFET channels after the expansion of ZnS-SiO_2. The details of the process development and integration of ZnS-SiO_2 liner stressor for n-FinFETs are documented in Section 5.3. Extensive electrical characterization was performed for n-FinFETs with ZnS-SiO_2 liner stressor. Analysis of the electrical characteristics and the n-FinFET performance enhancement induced by the ZnS-SiO_2 liner stressor are discussed in Section 5.4. In addition, the strain effect on carrier mobility is also analyzed in Section 5.4. Section 5.5 summarizes the key results achieved in this technology demonstration.

5.2 Key Concept: ZnS-SiO_2 as an Expandable Liner Stressor

ZnS, which is a direct band gap semiconductor, is a promising material for optoelectronic applications. The band gap of ZnS crystallites is dependent of their size, with a grain size of 1.5 nm giving a band gap of 5.2 eV in comparison to a band gap of 3.65 eV for a grain size of 10 nm [162],[163]. For pure ZnS, the mean grain diameter of ZnS crystallites was determined to be between 10 and 15 nm for films thicker than ~100 nm [164]. The addition of SiO_2 to ZnS seems to be effective in reducing the grain size of the ZnS. For example, a partially crystalline structure with average ZnS crystallite size of ~2 nm was detected in the ZnS-SiO_2 composite film with high ZnS composition (97%) [164]. Annealing of the composite film initiates the formation of nanocrstallites, with the crystallite size (or volume) increasing with longer anneal times, as shown in Fig. 5.1. The average crystallite size of ZnS-SiO_2 (97% ZnS) increases to 5 nm after annealing for 1 hour [164]. Further annealing leads to more crystalline films with grains in the <111> and <220> directions and a mean size of about 10 nm after annealing for 8 hours, and with a resistivity of ~1×10^{13} Ω·m [164].

ZnS-SiO_2 is exploited for strain engineering of n-FinFETs. Fig. 5.2(a) shows a ZnS-SiO_2 liner stressor wrapping around a FinFET. Coordinate axes are also shown. Three-dimensional (3D) finite-element simulations were performed to investigate the stress in FinFET channels after a 10% expansion in the volume of ZnS-SiO_2 (with 20% ZnS and 80% SiO_2). Considering the large crystallite size change (~120%) in ZnS-SiO_2 with high ZnS composition (Fig. 5.1), the 10% expansion applied in the simulation for ZnS-SiO_2 with 20% ZnS is conservative. In the simulation, a FinFET with fin width W_{fin} of 50 nm, fin height H_{fin} of 60 nm, and gate length L_G of 100 nm

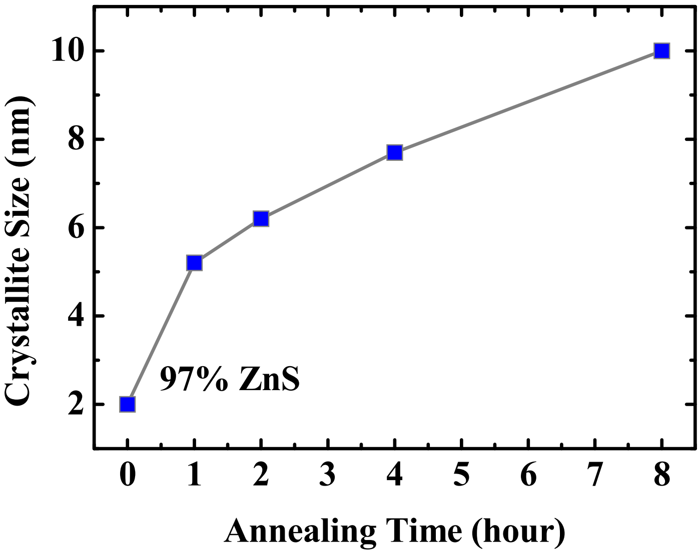


Fig. 5.1. Crystallite size of ZnS-SiO_2 (with 97% ZnS) as a function of annealing time [164].

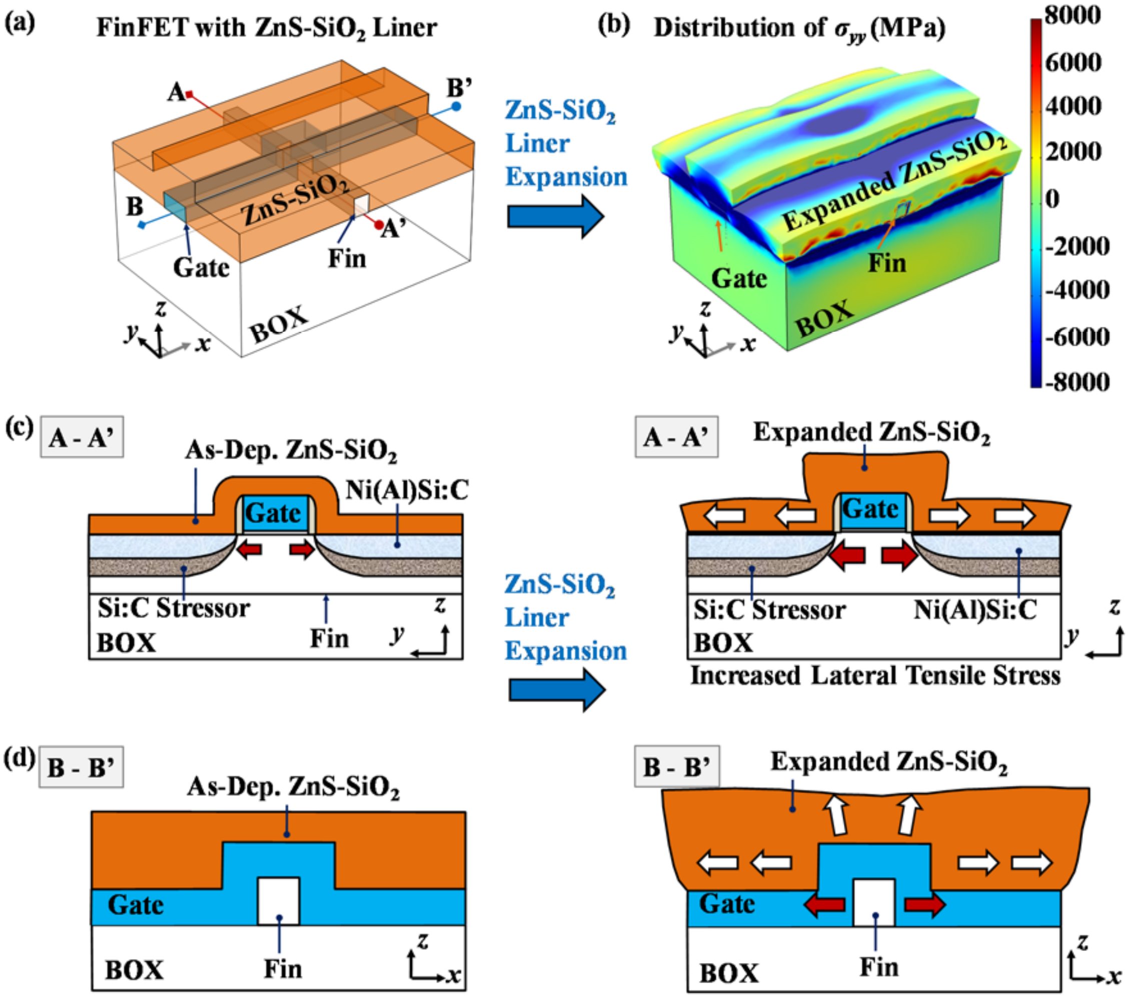
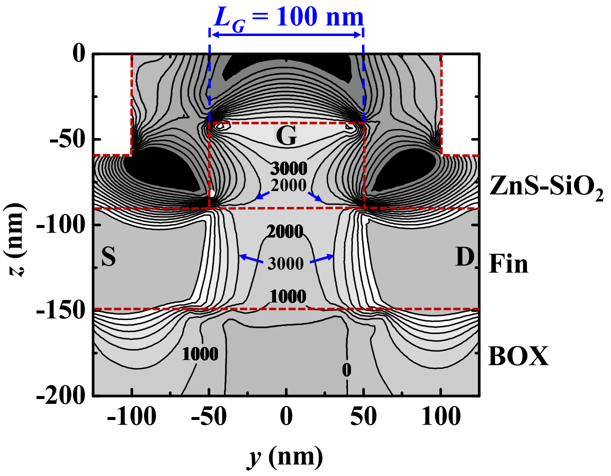


Fig. 5.2. (a) 3D schematic of a FinFET wrapped by ZnS-SiO$_2$ liner stressor. ZnS-SiO$_2$ expands when it is thermally annealed. Source-to-drain direction is along the *y*-axis. (b) 3D finite-element simulation of stress in the *y* direction (σ_{yy}) for a FinFET with expanded ZnS-SiO$_2$ liner stressor. The scale bar for stress σ_{yy} is shown on the right. Fin height of 60 nm, fin width of 50 nm, and gate length of 100 nm were used in the simulation. As ZnS-SiO$_2$ expands under the constraint that it adheres to the device structure, there is large compressive stress within the ZnS-SiO$_2$ liner. 2D schematics in the (c) A-A' and (d) B-B' planes illustrate the large tensile stress in the Si channel that can result from ZnS-SiO$_2$ expansion, which adds to the tensile stress induced by Si:C S/D stressors. The red arrows at channel and gate indicate the stress, while the white arrows at ZnS-SiO$_2$ regions indicate the expansion of ZnS-SiO$_2$ liner.

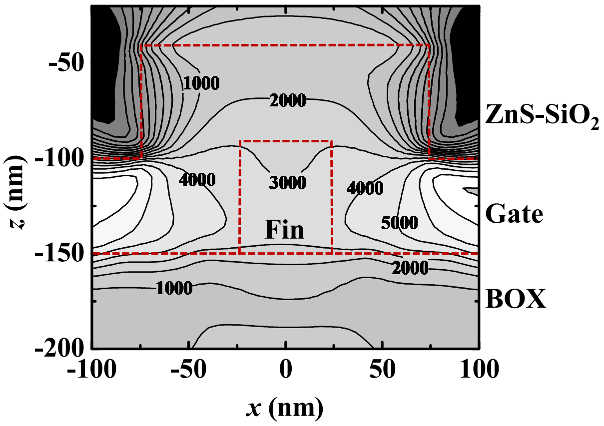
was used. A non-uniform finite element grid was used, with smaller grid size at regions where the stress gradient is larger. The boundary conditions are such that the bottom and sides of the Si substrate are rigid. The top and sides of the ZnS-SiO$_2$ layer are free. The expansion of the ZnS-SiO$_2$ layer was simulated using the framework of thermoelasticity [133]: **Error! Reference source not found.**: the 10% expansion of ZnS-SiO_2 is modeled by setting the thermal expansion coefficient of the ZnS-SiO_2 liner and the FinFET to 0.10 K^{-1} and 0 K^{-1}, respectively, and raising the temperature by 1 K. Other material properties of ZnS-SiO_2, such as the Young's modulus and Poisson's ratio, are similarly obtained from those of ZnS and SiO_2 by linear interpolation. For ZnS and SiO_2, the Young's moduli are 74.5 and 75 GPa, and the Poisson's ratios are 0.27 and 0.17, respectively. Fig. 5.2(b) shows the 3D distribution of the simulated stress in the source-to-drain direction (y direction), denoted by σ_{yy}, for the FinFET with an expanded ZnS-SiO_2 liner. The expanded ZnS-SiO_2 liner induces deformation, leading to very high mechanical tensile stress in the fin and channel. As ZnS-SiO_2 expands under the constraint that it adheres to the device structure, there is large compressive stress within the ZnS-SiO_2 liner. However, the constraint is negligible at the edges or corners of the ZnS-SiO_2 liner, where the expansion is not confined and a tensile stress is shown [Fig. 5.2(b)].

The key concept of this work is illustrated using two-dimensional or cross-section schematics in the A-A' plane [*yz* plane cutting through fin and perpendicular to gate line, Fig. 5.2(c)] and B-B' plane [*xz* plane cutting through gate line and perpendicular to fin, Fig. 5.2(d)]. The ZnS-SiO_2 liner adheres to the source/drain (S/D) regions of the FinFET. The as-deposited ZnS-SiO_2 liner has an intrinsic tensile stress, which transfers to the FinFET channel and results in electron mobility enhancement. Expansion of the ZnS-SiO_2 liner stretches the S/D regions and increases the tensile stress in the fin and channel, leading to further electron mobility enhancement. The distributions of the simulated σ_{yy} in the A-A' plane, simulated stress in the x direction (σ_{xx}) in the B-B' plane, and simulated σ_{zz} in the A-A' plane in the channel region are shown in Fig. 5.3, for a FinFET with expanded ZnS-SiO_2 liner. Very high tensile stress

(a) A - A' Distribution of σ_{yy} (MPa)



(b) B - B' Distribution of σ_{xx} (MPa)



(c) A - A' Distribution of σ_{zz} (MPa)

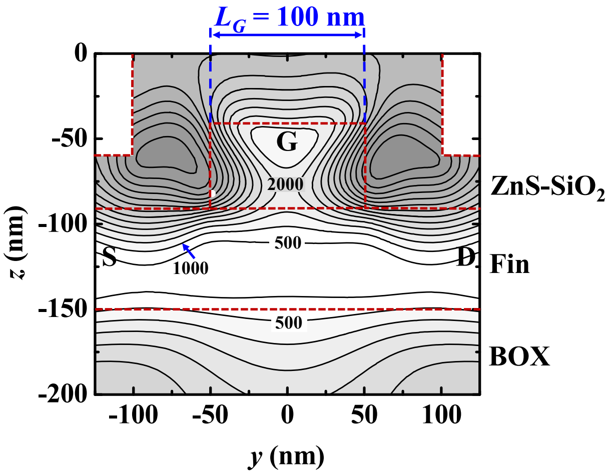


Fig. 5.3. Simulated (a) σ_{yy} distribution in the A-A' plane along the source-to-drain direction, (b) σ_{xx} distribution in the B-B' plane across the fin along the gate, and (c) σ_{zz} distribution in the A-A' plane, showing that the expansion of the ZnS-SiO$_2$ liner induces very high tensile stress in the channel and fin at all directions. The planes A-A' and B-B' are indicated in Fig. 5.2.

of up to 3000 MPa is observed in the channel and fin, induced by the expansion of the ZnS-SiO_2 liner stressor.

5.3 Fabrication of N-FinFETs with ZnS-SiO_2 Liner Stressor

Silicon-on-insulator wafers were used for N-FinFET fabrication with (001) wafer surface and <110> channel orientation. Buried oxide thickness is 140 nm. The process flow is depicted in Fig. 5.4(a). Fins with H_{fin} of 50 nm and W_{fin} down to 25 nm were formed. Thermal SiO_2 gate dielectric of ~3 nm was grown, followed by poly-Si gate deposition. Gates with L_G down to 35 nm were formed. This was followed by germanium ion (Ge^+) pre-amorphization implant (PAI) at an energy of 50 keV and a dose of 5×10^{14} cm^{-2}. Multi-energy carbon ion (C^+) implant was then performed with targeted peak C concentration of 1.5%. The C implant conditions were 3.6×10^{15} cm^{-2} at 12 keV, 7.2×10^{14} cm^{-2} at 5.5 keV, and 4.7×10^{14} cm^{-2} at 2.5 keV [122],[165]. After the deep S/D implant, Si:C stressor formation and S/D dopant activation using solid phase epitaxial re-growth were performed using a two-step rapid thermal anneal [166]. The smaller lattice constant of Si:C S/D induces uniaxial tensile strain in the Si channel for electron mobility enhancement [22],[165].

To reduce the effective electron Schottky barrier height ($\Phi_B{}^N$), shallow Ge^+ PAI (5×10^{14} cm^{-2} at 5 keV) followed by aluminum ion (Al^+) implant at a dose of 1×10^{16} cm^{-2} and energy of 1 keV were performed, as illustrated in Fig. 5.4(b) [122],[123]. The FinFET fabrication process steps mentioned above were done by Dr. KOH Shao Ming of our research group. The following steps were performed by the author.

Ni film with a thickness of ~8 nm was deposited using sputtering, followed by silicidation using a 450 °C anneal for 30 s to form the Ni(Al)Si:C S/D contacts. Unreacted Ni on the isolation and spacers was removed by sulfuric acid-peroxide

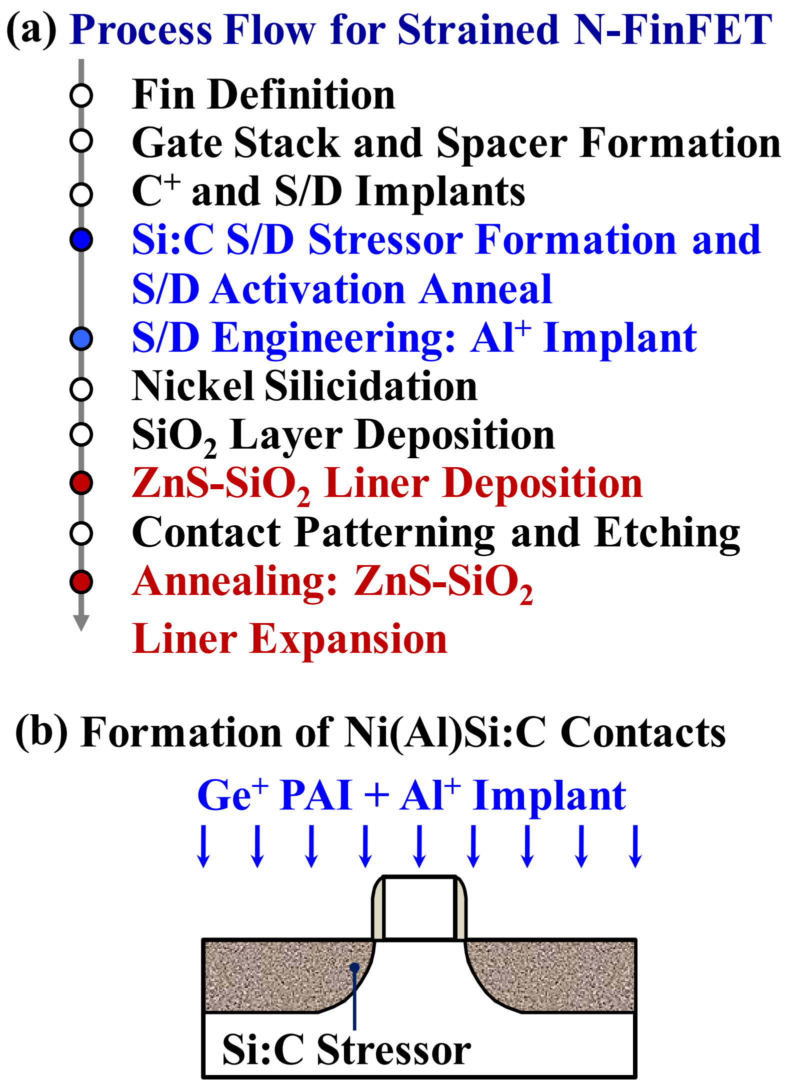


Fig. 5.4. (a) Process flow for fabricating n-FinFETs with $ZnS\text{-}SiO_2$ liner stressor. (b) Illustration of the $\Phi_B{}^N$ reduction technique applied in this work for n-FinFET, where Ni(Al)Si:C contacts were formed on Si:C S/D stressor with shallow Ge^+ PAI and Al^+ implant. The FinFET fabrication steps before Ni silicidation were performed by Dr. KOH Shao Ming of our research group. $ZnS\text{-}SiO_2$ deposition was done by Dr. Ashvini GYANATHAN of our research group.

solution [H_2SO_4:H_2O_2 (4:1)] at 120 °C for 120 s. The Al profile was controlled or engineered by C, which suppresses Al diffusion during silicidation, thus retaining a high concentration of Al within the NiSi. Incorporating Al within NiSi reduces the Schottky barrier height for n-Si:C contact [122],[123]. 15 nm of SiO_2 was deposited to complete the control n-FinFETs with Si:C S/D stressors.

Experimental splits were introduced after forming the Si:C S/D stressors and Ni(Al)Si:C S/D contacts. For n-FinFETs with dual stressors, which have an additional ZnS-SiO$_2$ liner to further enhance the tensile stress in the fin and channel, ~25 nm of ZnS-SiO$_2$ liner was deposited by sputtering a ZnS-SiO$_2$ composite target (with 20% ZnS and 80% SiO$_2$) at room temperature, using a DC power of 1000 W and a chamber pressure of 3 mTorr. ZnS-SiO$_2$ is used as a liner stressor for the first time in the experiment. The ZnS-SiO$_2$ deposition was skipped for the control n-FinFETs.

To minimize the differences in electrical performance caused by process variation across wafers or between dies, the FinFETs with and without ZnS-SiO$_2$ liner stressor were processed on the same die. All devices on the same die were processed together to the step before ZnS-SiO$_2$ deposition, before each die was broken into pieces for the experimental splits. Fig. 5.5 shows the photo of an n-FinFET die.

After contact patterning, CF$_4$-based plasma etching was done to expose the S/D and gate probe pads. Furnace anneal, which induces ZnS-SiO$_2$ liner expansion, was then performed at 350 °C for 1 hour in N$_2$ ambient for n-FinFETs with and without ZnS-SiO$_2$ liner. Electrical characterization was performed by probing the NiSi source, drain, and gate contacts. In this work, the probes on the NiSi in the S/D regions are ~50 μm from the gate edge.

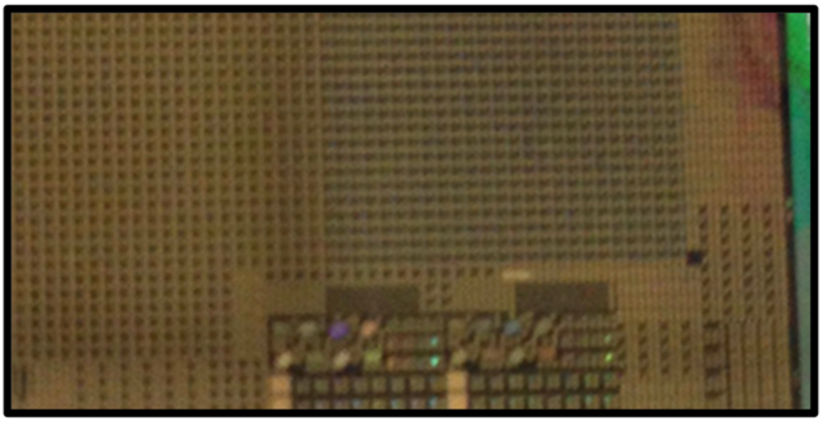


Fig. 5.5. Photo of an n-FinFET die. The FinFETs with and without ZnS-SiO_2 liner stressor were processed on the same die.

Fig. 5.6(a) shows the cross-sectional schematic of an n-FinFET with Ni(Al)Si:C S/D contacts and ZnS-SiO_2 liner stressor along the source-to-drain direction. Fig. 5.6(b) shows an SEM image of an n-FinFET featuring ZnS-SiO_2 liner stressor. To obtain the Transmission Electron Microscopy (TEM) images, a Focused Ion Beam (FIB) cut was performed in the channel region across the gate in the source-to-drain direction as shown in Fig. 5.6(b). High resolution TEM images of the S/D region [i.e. region 1 in Fig. 5.6(a)] and the expanded ZnS-SiO_2 [i.e. region 2 in Fig. 5.6(a)] of an n-FinFET with Ni(Al)Si:C contact and ZnS-SiO_2 liner are shown in Fig. 5.6(c) and (d), respectively. The expanded ZnS-SiO_2 is polycrystalline, and its thickness is ~28 nm [Fig. 5.6(d)]. Therefore, the volume expansion of the ZnS-SiO_2 line stressor in this work is estimated to be ~12%.

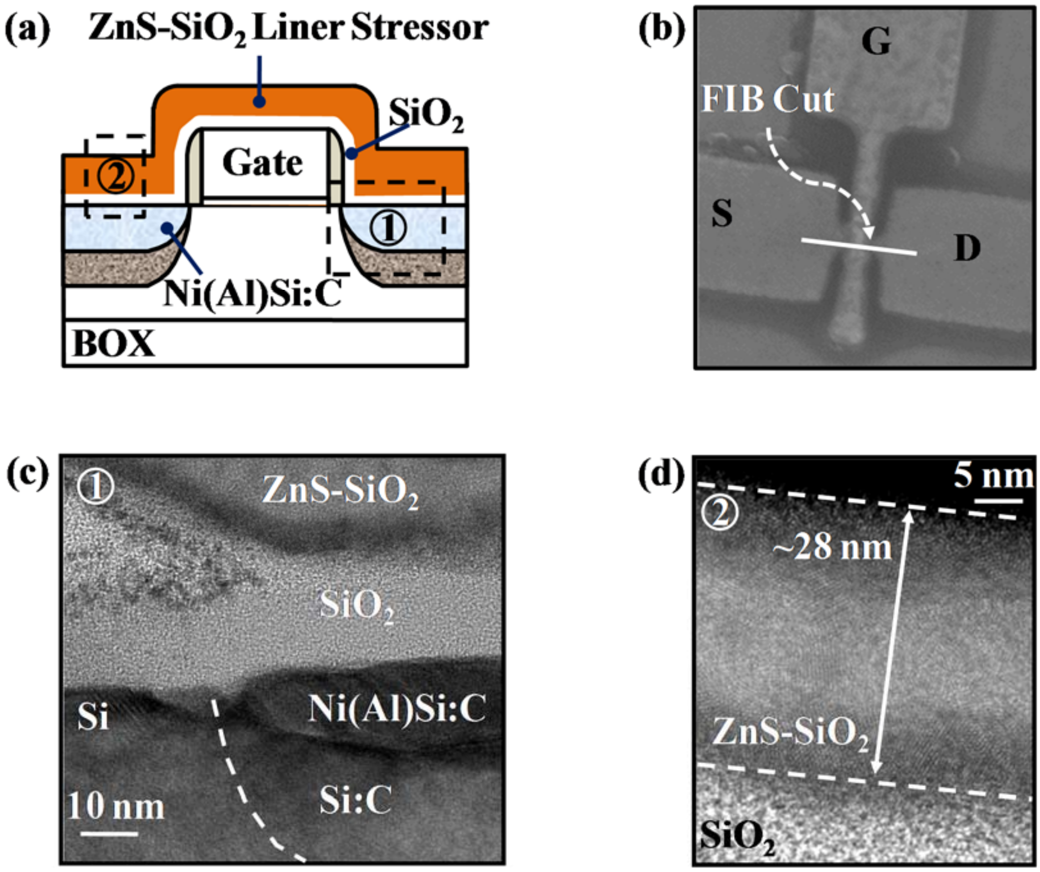


Fig. 5.6. (a) Cross-sectional schematic along the source-to-drain direction of an n-FinFET with $ZnS-SiO_2$ liner stressor. (b) SEM of n-FinFET featuring $ZnS-SiO_2$ liner stressor. High resolution TEM images showing (c) the silicided S/D region of an n-FinFET with Ni(Al)Si:C, and (d) the zoomed-in view of the $ZnS-SiO_2$ liner stressor on an n-FinFET. C suppresses Al diffusion during silicidation, thus retaining a high concentration of Al within the silicided contact material. The TEM was performed as an external service job at the Institute of Materials Research and Engineering (IMRE).

5.4 Electrical Characteristics and Discussion

To evaluate the impact of as-deposited $ZnS-SiO_2$ liner stressor on the drain current of n-FinFETs, the off-state current I_{off} versus linear drain current I_{Dlin} characteristics of control FinFETs and FinFETs with as-deposited $ZnS-SiO_2$ liner stressor are plotted in Fig. 5.7. For each device split, ~50 devices were measured. At

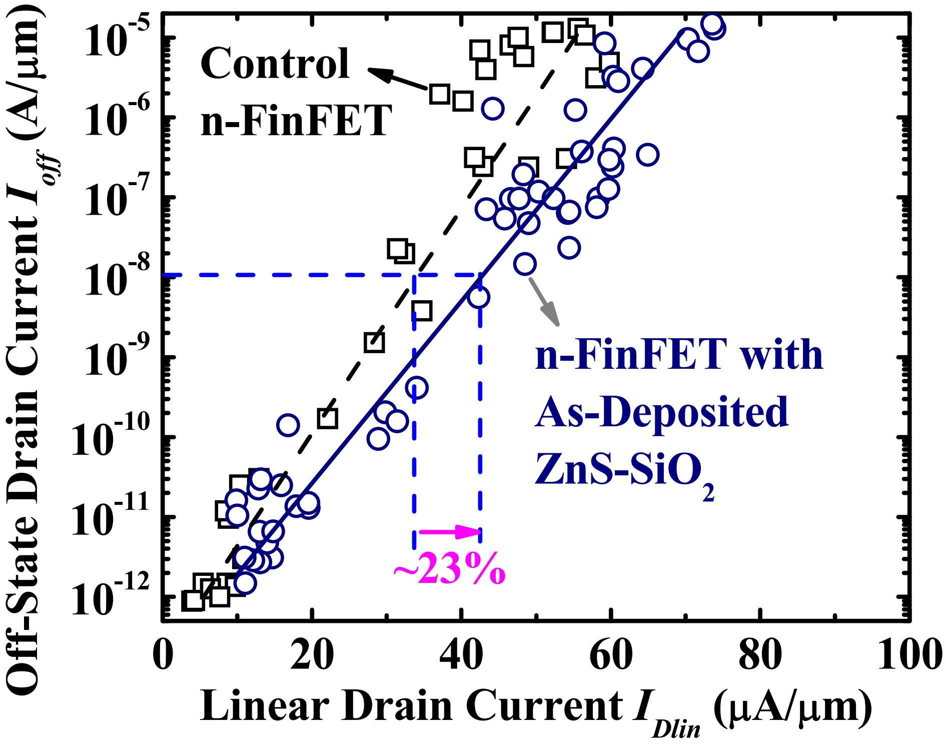


Fig. 5.7. Plot of I_{off} ($V_G = V_{TH,lin}$ - 0.1 V, V_D = 1.2 V) versus I_{Dlin} ($V_G = V_{TH,lin}$ + 1.1 V, V_D = 0.05 V) for FinFETs with and without as-deposited ZnS-SiO2 liner. W_{fin} = 25 nm to 55 nm, and L_G = 35 nm to 200 nm. At an I_{off} of 10 nA/μm, n-FinFETs with as-deposited ZnS-SiO2 liner stressor show ~23% I_{Dlin} enhancement over the control n-FinFETs. For each device split, ~50 FinFETs were measured.

I_{off} = 10 nA/μm, FinFETs with as-deposited ZnS-SiO2 stressor show ~23% I_{Dlin} enhancement over the control FinFETs. This drain current enhancement is due to the intrinsic stress of as-deposited ZnS-SiO2, similar to the effect of SiN with intrinsic tensile stress.

When ZnS-SiO2 expands after anneal, the tensile stress in the FinFET channel is expected to increase as discussed above. N-FinFETs with expanded ZnS-SiO2 liner stressor will be discussed next. Fig. 5.8(a) shows the I_D-V_G curves of n-FinFETs (W_{fin} = 45 nm and L_G = 55 nm) with and without expanded ZnS-SiO2 stressor. The two FinFETs show comparable SCE control, while the FinFET with expanded ZnS-SiO2 stressor has a slightly smaller threshold voltage than the control FinFET. The band structure modification by strain results in a narrowed energy bandgap and leads to ~15 mV reduction in the magnitude of the threshold voltage and a slightly higher leakage current [147]-[151], similar to the cases reported for n-FinFETs with other liner stressors such as SiN [167]. Comparison of the transconductance (G_m) of these two devices as a function of gate voltage is shown in Fig. 5.8(b). The n-FinFET with expanded ZnS-SiO_2 stressor has ~68% enhancement of peak saturation G_m over the control. Fig. 5.9 compares the I_D-V_G characteristics in linear scale of the devices in Fig. 5.8, where I_D is normalized by the total effective device width of ($2H_{fin}$ + W_{fin}). Saturation drain current I_{Dsat} enhancement of 29% was observed for the n-FinFET with ZnS-SiO_2 stressor over the control at gate overdrive and V_D of 1.2 V. As the process flow is the same for these two devices except for the ZnS-SiO_2 deposition, the difference in I_{Dsat} performance is due to the stress induced by the expanded ZnS-SiO_2 stressor.

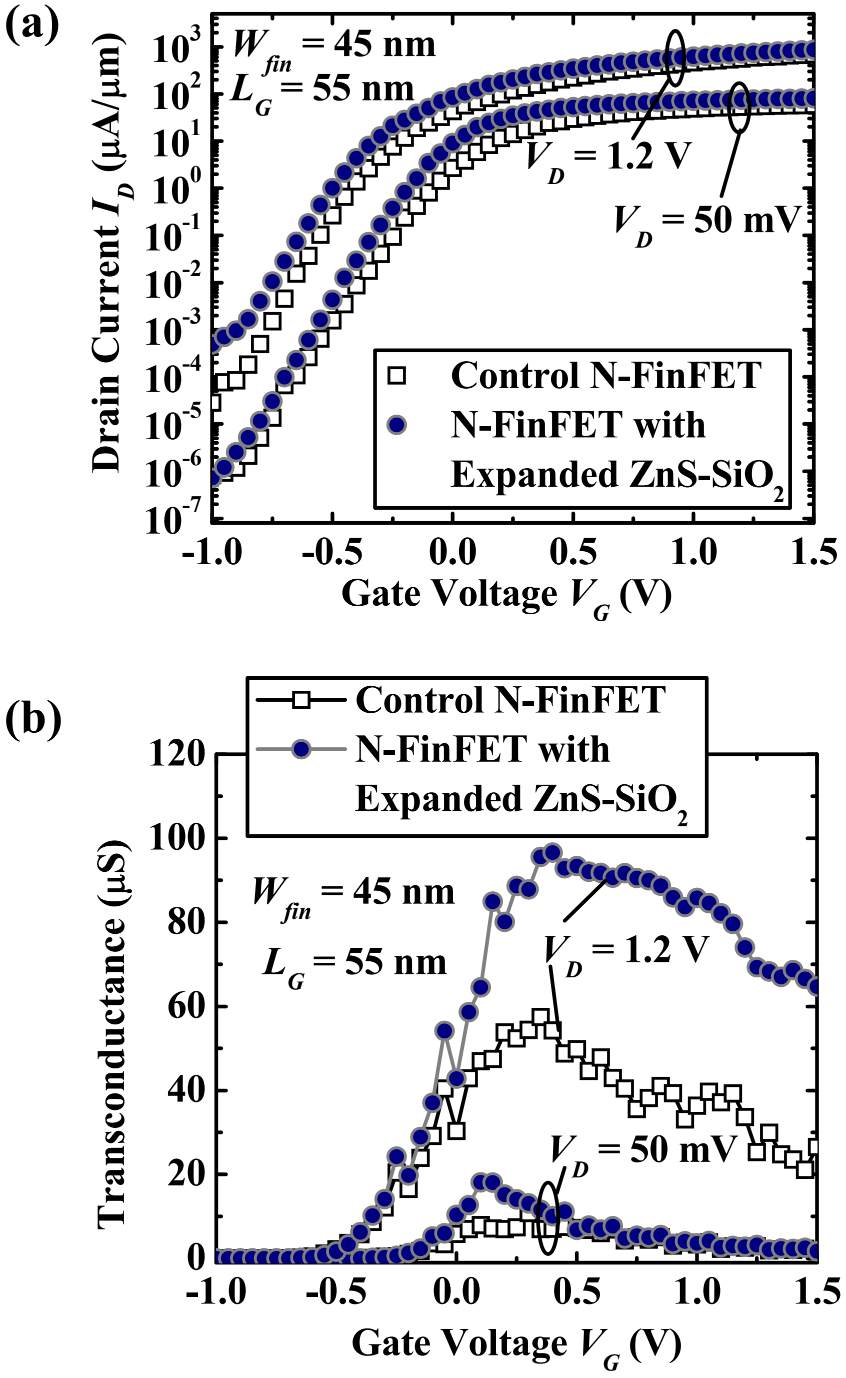


Fig. 5.8. (a) I_D-V_G characteristics of n-FinFETs with and without expanded ZnS-SiO$_2$ liner stressor, showing similar DIBL and subthreshold swing. The n-FinFET with expanded ZnS-SiO$_2$ liner has slightly smaller V_{TH} than that of the control n-FinFET. L_G is 55 nm and W_{fin} is 45 nm. (b) The n-FinFET with expanded ZnS-SiO$_2$ liner stressor has ~68% saturation G_m improvement over the control n-FinFET.

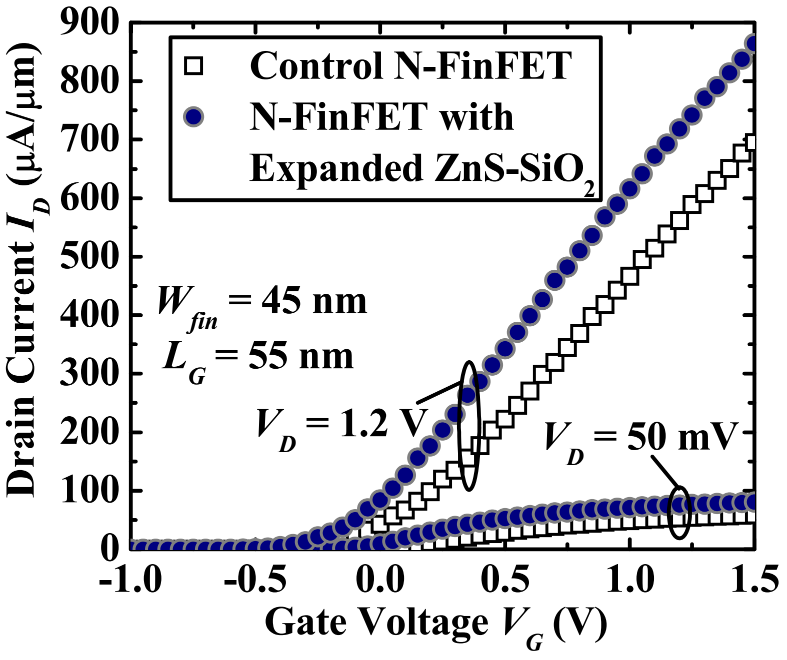


Fig. 5.9. I_D-V_G characteristics in linear scale of an N-FinFET with expanded ZnS-SiO$_2$ liner stressor and a control, with L_G of 55 nm and W_{fin} of 45 nm. The FinFET with expanded ZnS-SiO$_2$ liner stressor shows ~29% drain current enhancement over the control, at gate overdrive and V_D of 1.2 V.

In the strained FinFET channel, the stress induced by expanded ZnS-SiO$_2$ stressor splits the six-fold degenerate conduction band valleys into two groups: 1) lower energy two-fold (Δ_2) degenerate valleys that have low in-plane longitudinal effective mass, and 2) higher energy four-fold (Δ_4) degenerate valleys, causing electrons to repopulate from the Δ_4 valleys to the Δ_2 valleys [167]. With smaller conductivity effective mass in the Δ_2 valleys, the repopulation into the Δ_2 valleys causes the average effective mass to decrease and carrier mobility to increase [3]. Moreover, the band splitting also leads to a change of the scattering rate. In a strained FinFET channel, the dominant scattering mechanisms are inter-valley phonon scattering [52] and surface roughness scattering [53]. Due to the splitting of the six-fold degenerate conduction band, the inter-valley scattering rate becomes lower due to the smaller density of states [51], which results in higher mobility.

The I_{Dsat}-I_{off} and I_{Dlin}-I_{off} characteristics of n-FinFETs with and without expanded ZnS-SiO$_2$ stressor are shown in Figs. 5.10 and 5.11, respectively. For each device split in Figs. 5.10 and 5.11, ~30 devices were measured. At a fixed I_{off} of 10 nA/µm, we observe enhancements in I_{Dsat} and I_{Dlin} of ~26% and ~48%, respectively, with larger enhancement for shorter gate lengths due to enhanced strain effect, which will be discussed below. Unlike in the GST work where FinFETs with a wide range of W_{fin} (35 nm to 115 nm) were compared in the I_{Dsat}-I_{off} and I_{Dlin}-I_{off} plots, FinFETs with a smaller range of W_{fin} (25 nm to 55 nm) were plotted for FinFETs with and without ZnS stressor, which leads to a tighter distributions of the strained FinFETs in the I_{Dsat}-I_{off} and I_{Dlin}-I_{off} plots as compared to those in the GST work in Chapter 3.

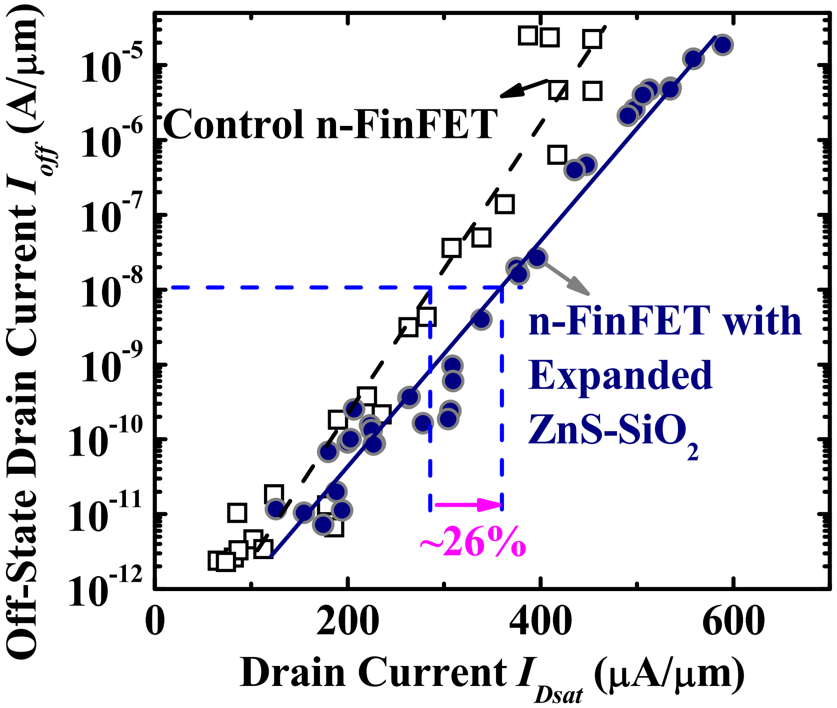


Fig. 5.10. Comparison of I_{off} ($V_G = V_{TH,sat} - 0.1$V, $V_D = 1.2$ V) versus I_{Dsat}, showing ~26% I_{Dsat} enhancement for n-FinFETs with expanded ZnS-SiO$_2$ liner stressor over the control at $I_{off} = 10$ nA/µm. $W_{fin} = 25$ nm to 55 nm, and $L_G = 35$ nm to 200 nm. I_{Dsat} is taken at $V_G = V_{TH,sat} + 1.1$ V and $V_D = 1.2$ V.

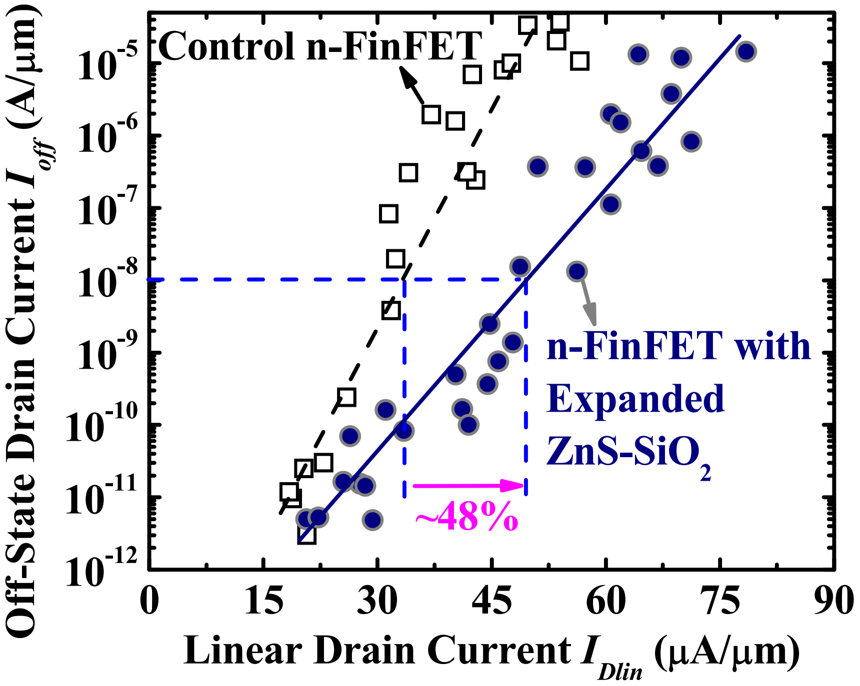


Fig. 5.11. Comparison of I_{off} ($V_G = V_{TH,lin} - 0.1$V, $V_D = 1.2$ V) versus I_{Dlin} ($V_G = V_{TH,lin} + 1.1$ V, $V_D = 0.05$ V), showing ~48% I_{Dlin} enhancement for n-FinFETs with expanded $ZnS-SiO_2$ liner stressor over the control at I_{off} = 10 nA/μm (W_{fin} = 25 nm to 55 nm, and L_G = 35 nm to 200 nm).

Next, we compare the drain current enhancements induced by the as-deposited and expanded $ZnS-SiO_2$ stressors. Fig. 5.12 shows the I_{Dlin} enhancement for n-FinFETs with as-deposited $ZnS-SiO_2$ and expanded $ZnS-SiO_2$ stressor, as compared to the control n-FinFET. All the devices in Fig. 5.12 have the same L_G of 70 nm and W_{fin} of 45 nm. $ZnS-SiO_2$ liner expansion increases the stress level in the channel significantly, doubling the I_{Dlin} enhancement in n-FinFETs. Therefore, n-FinFETs with expanded $ZnS-SiO_2$ stressor will be the focus in the following discussion.

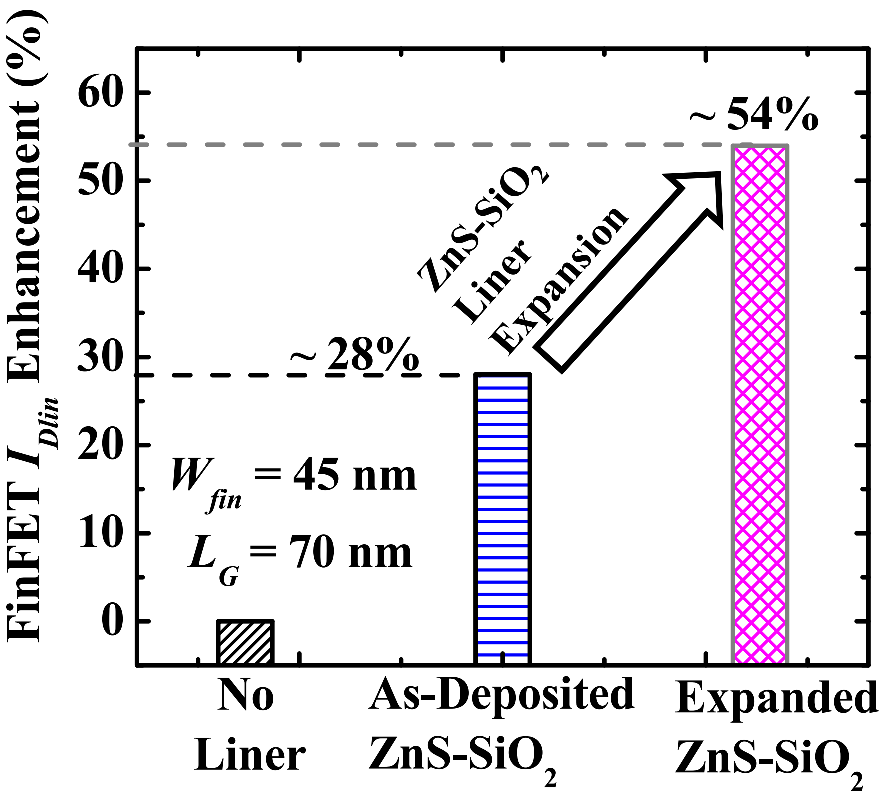


Fig. 5.12. ~28% and ~54% I_{Dlin} enhancement were observed for n-FinFETs with as-deposited and expanded ZnS-SiO$_2$ liner stressors, respectively, over n-FinFETs with no liner. ZnS-SiO$_2$ expansion induces higher stress that leads to further I_{Dlin} enhancement. I_{Dlin} is taken at $V_G = V_{TH,lin} + 1.1$ V and $V_D = 0.05$ V.

Fig. 5.13 compares the I_{Dsat} of n-FinFETs with and without expanded ZnS-SiO$_2$ stressor at different L_G (from 35 nm to 205 nm), with fixed W_{fin} of 25 nm. When L_G is reduced, I_{Dsat} generally increases, with the I_{Dsat} of FinFETs with expanded ZnS-SiO$_2$ stressor being higher than that of the control FinFETs without ZnS-SiO$_2$ stressor

for all L_G. Moreover, the current enhancement is higher for smaller L_G, which is attributed to higher stress induced in the channel by the expanded ZnS-SiO$_2$ stressor at smaller L_G. To investigate the channel stress of FinFETs with smaller L_G, 3D finite element simulation was performed for FinFETs with expanded ZnS-SiO$_2$ stressor with L_G of 20 nm. The simulation conditions are identical to those in Figs. 5.2(b) and 5.3, except that L_G is 20 nm. Fig. 5.14 shows the simulated stress σ_{yy}, σ_{xx}, and σ_{zz} at the center

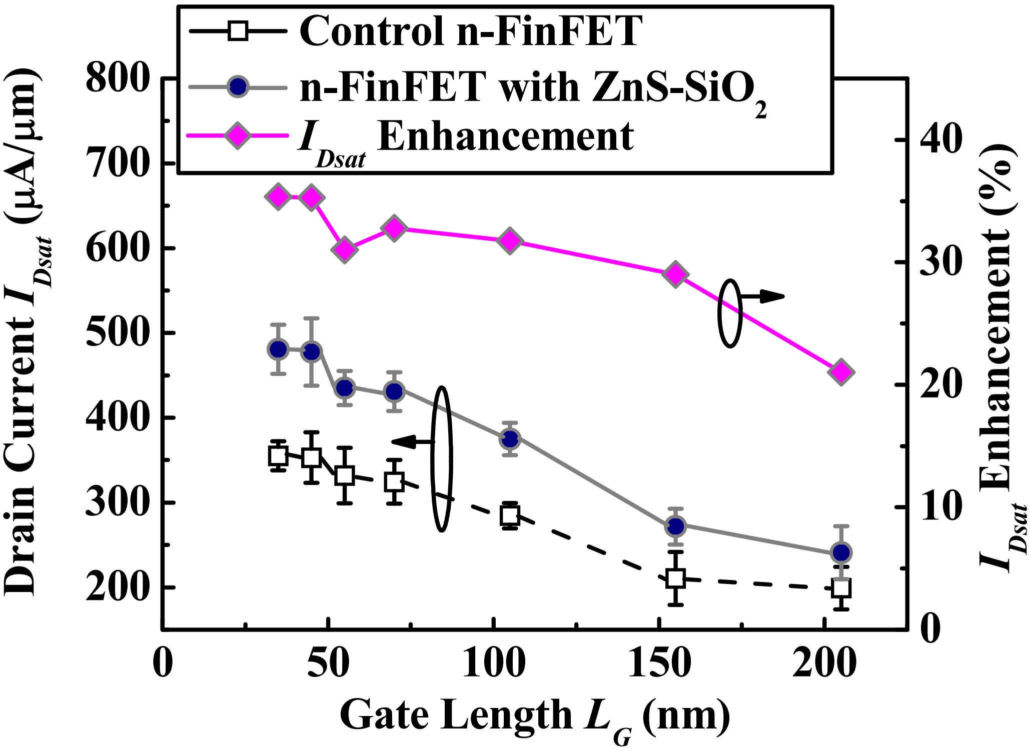


Fig. 5.13. Comparison of I_{Dsat} (obtained at $V_G = V_{TH,sat} + 1.1$ V, $V_D = 1.2$ V) for n-FinFETs with and without expanded ZnS-SiO$_2$ liner stressor at different gate lengths. As gate length is reduced, the I_{Dsat} of FinFETs both with and without expanded ZnS-SiO$_2$ stressor increases. I_{Dsat} enhancement as a function of gate length is also plotted. Generally, I_{Dsat} enhancement increases with decreasing gate length. The standard deviation of I_{Dsat} for a given W_{fin} and L_G is shown as error bars. Enhancement values were calculated using the mean I_{Dsat}. Mean I_{Dsat} values are plotted as circle or square symbols.

of the FinFET channel as a function of L_G.When L_G reduces, the channel stress induced by the expanded ZnS-SiO$_2$ liner increases, which leads to higher electron mobility enhancement for smaller L_G. This is consistent with the experimental results in Fig. 5.13, as well as the simulation results of FinFETs with SiN and GST liner stressors [153],[154].

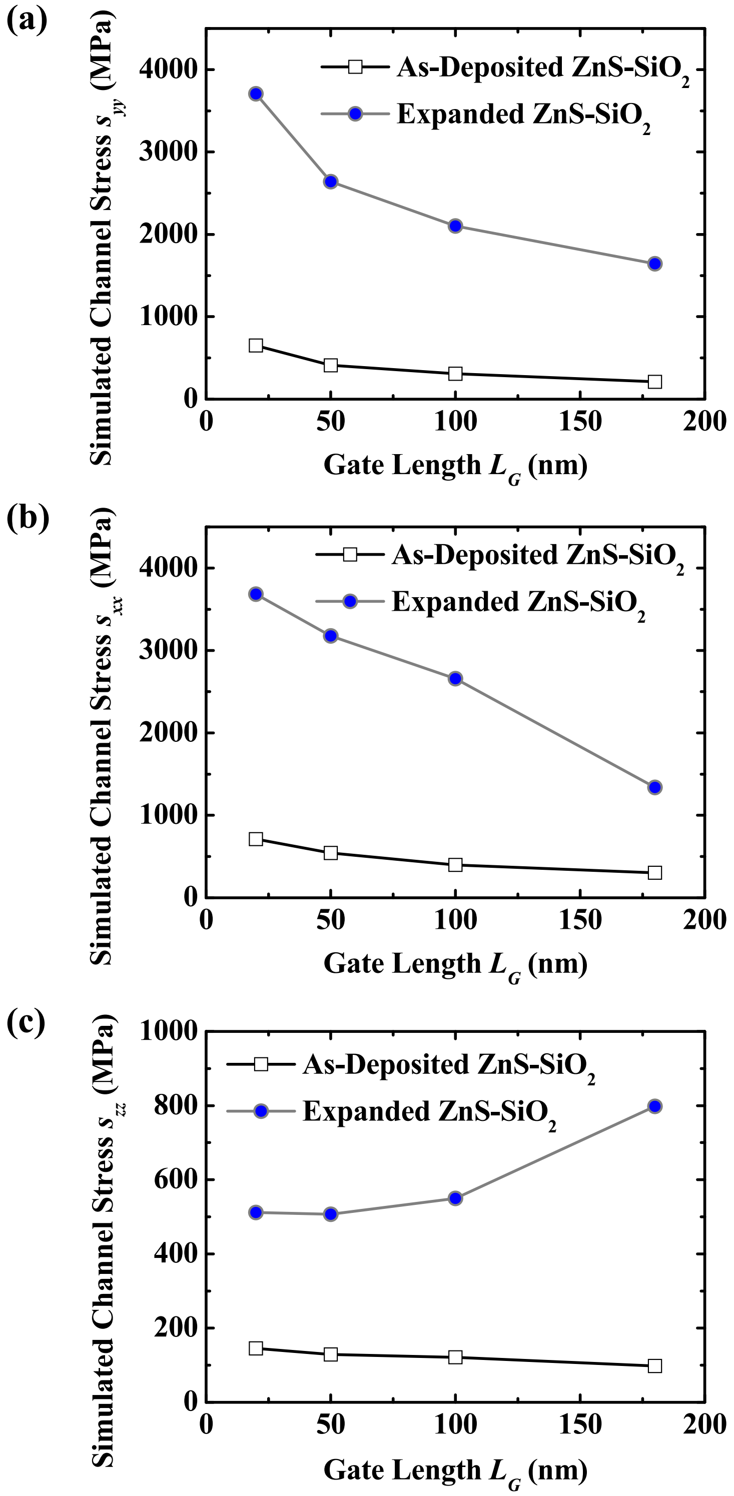


Fig. 5.14. Simulated (a) σ_{yy}, (b) σ_{xx}, and (c) σ_{zz} (at center of the channel) as a function of L_G, for FinFETs with the as-deposited and expanded ZnS-SiO$_2$ liner. The stresses induced by the expanded ZnS-SiO$_2$ liner are higher than those by the as-deposited ZnS-SiO$_2$ liner at all directions.

Comparisons of device performance as a function of drain-induced barrier lowering DIBL and subthreshold swing SS are shown in Figs. 5.15 and 5.16, respectively. At a fixed DIBL of 40 mV/V and fixed SS of 120 mV/decade, I_{Dsat} enhancement for n-FinFETs with expanded ZnS-SiO$_2$ stressor over the control is 51% and 46%, respectively.

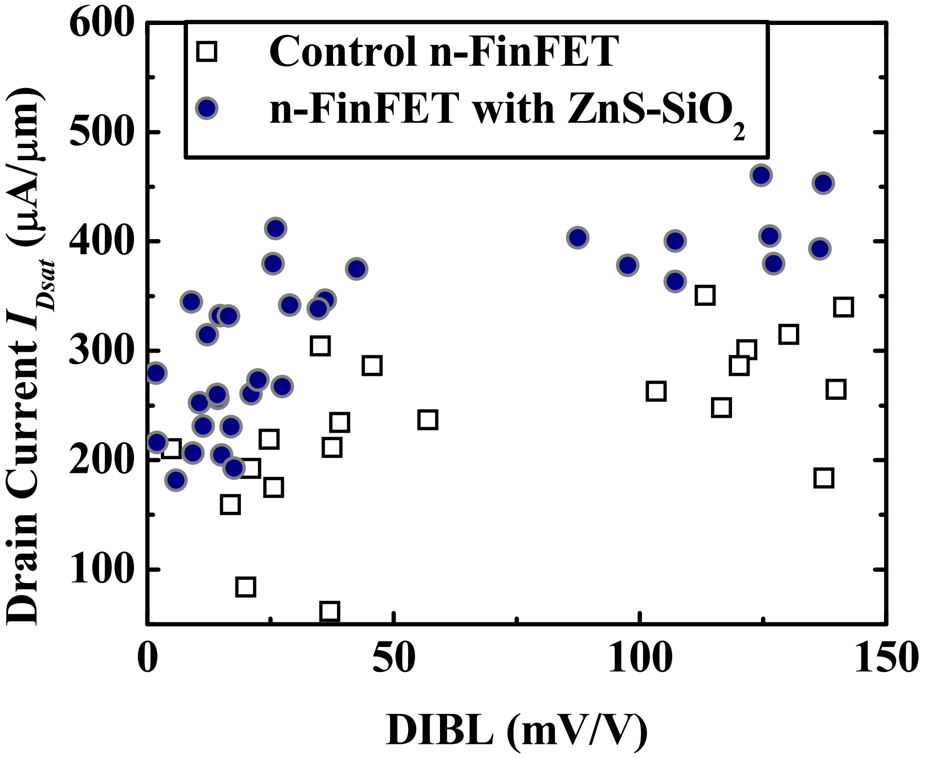


Fig. 5.15. Plot of I_{Dsat} versus DIBL for FinFETs with and without expanded ZnS-SiO$_2$ liner stressor. At a fixed DIBL of 40 mV/V, ~51% I_{Dsat} enhancement can be observed for FinFETs with expanded ZnS-SiO$_2$ liner stressor over the control FinFETs. I_{Dsat} was measured at gate overdrive V_G - $V_{TH,sat}$ = 1.1 V and V_D = 1.2 V.

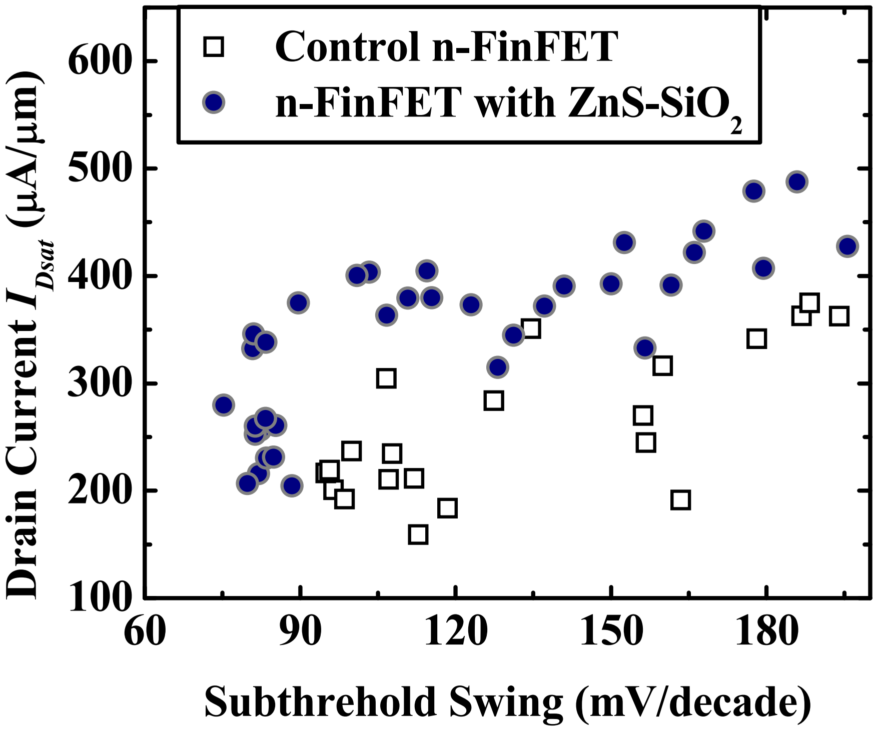


Fig. 5.16. At a fixed subthreshold swing of 120 mV/decade, ~46% I_{Dsat} enhancement can be observed for n-FinFETs with expanded ZnS-SiO$_2$ liner stressor over the control.

To verify the strain effect on carrier mobility enhancement, total resistance R_{Total} *vs.* L_G was plotted in Fig. 5.17 for both n-FinFETs with expanded ZnS-SiO$_2$ stressor and control n-FinFETs. The effective carrier mobility can be calculated using

$$\mu = \frac{1}{WQ_{inv}\frac{dR_{Total}}{dL_G}} , \tag{5.1}$$

where W is the channel width and Q_{inv} is the inversion charge density. The smaller slope for n-FinFETs with expanded ZnS-SiO$_2$ stressor as compared to the control indicates mobility enhancement of up to ~53%. The mobility enhancement is consistent with the I_{Dsat} and I_{Dlin} enhancements as shown in Figs. 5.10 and 5.11, respectively. Using the piezoresistance coefficients, we now quantitatively calculate the mobility enhancement using the simulated ZnS-induced stress in Fig. 5.3 (taking average simulated stress at center of the channel: σ_{yy} = 2 GPa, σ_{xx} = 2.5 GPa, and σ_{zz} = 500 MPa). The relationship between resistivity ρ and stress σ is described by $\Delta\rho/\rho=\pi_l\sigma_l+\pi_t\sigma_t$, where π_l and π_t are the piezoresistance coefficients in the longitudinal and transverse directions, respectively. σ_l and σ_t are the longitudinal and transverse stresses, respectively. For simplicity, we use the bulk values for π_l and π_t with channel doping considered [59], though technically piezoresistance coefficients should take the 2-D nature of transport in MOSFETs and dependence on temperature into account [62],[155]. Fig. 5.18 shows the values of π_l and π_t for top and side-wall channels of the FinFET in this work. The calculated resistivity reduction or electron mobility enhancement is ~78%, which is higher than the estimated mobility enhancement as shown in Fig. 5.17. Many factors such as immature process flow for integrating ZnS stressor could lead to the stress relaxation. Thickness non-uniformity of the ZnS and the SiO_2 insulating layer below it, incomplete crystallization of the ZnS in some regions, and lateral etching of ZnS during the dilute HF etching of residual SiO_2 can all result in stress reduction and therefore lower electron mobility enhancement.

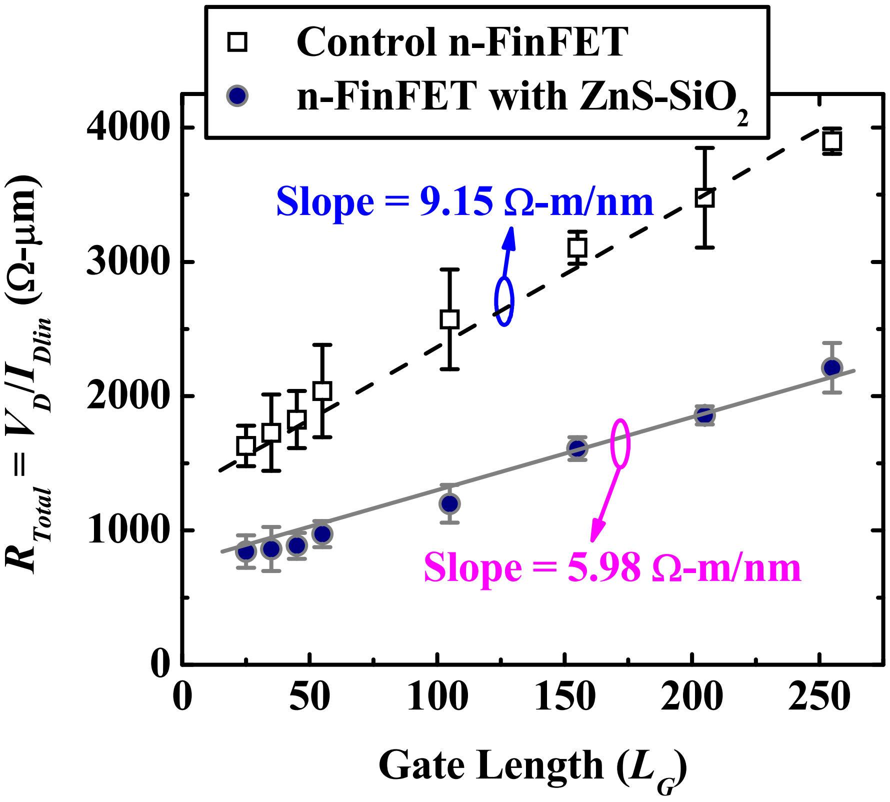
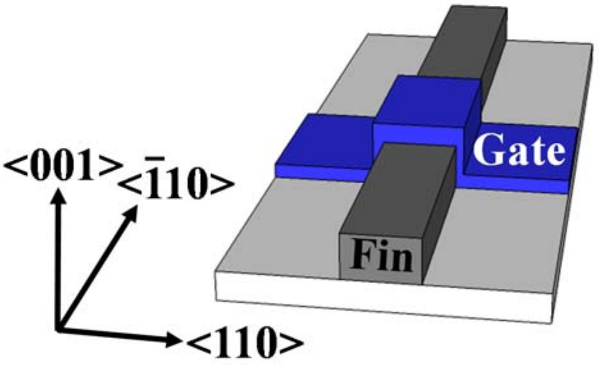


Fig. 5.17. $R_{Total} = V_{DS}/I_{Dlin}$ as a function of L_G (I_{Dlin} taken at $V_{GS} - V_{TH,lin} = 1.1$ V, $V_{DS} = 50$ mV). FinFETs with expanded ZnS-SiO$_2$ liner have a smaller dR_{Total}/dL_G, and exhibit mobility enhancement of ~53%. The standard deviation of R_{Total} is shown as error bars.



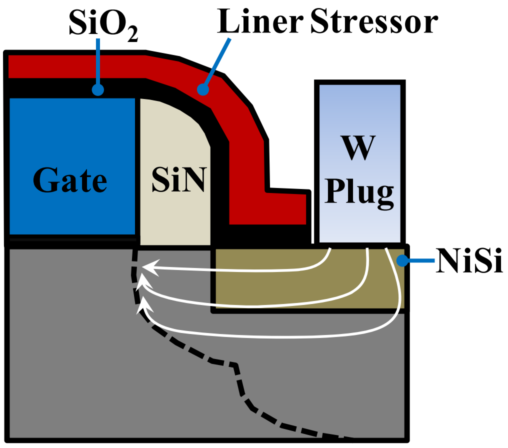
Side wall Channels		Top Channel	
π_l	π_t	π_l	π_t
-31	52	-31	-20

Fig. 5.18. Room temperature piezoresistance coefficients of <110>-oriented n-channel FinFETs, for both sidewall and top channels (in units of 10^{-12} cm^2/dyne).

In addition, Fig. 5.17 shows significant S/D series resistance (R_{SD}) reduction for the FinFETs with expanded ZnS-SiO$_2$ stressor as compared with the control FinFETs. This could be due to the stress-induced mobility enhancement in S/D regions. Fig. 5.19 shows a transistor with W plug placed very close to the channel (as is the case in industry) and a transistor in this work where the probe tip contacts the NiSi far (~50 μm) from the channel. As shown in Fig. 5.19(a), the path of current flow from the W plug to the channel is much shorter as compared with that in the transistor in this work [Fig. 5.19(b)], where the current in the S/D region can spread from the NiSi into the unsilicided region under the NiSi over the long distance from probe to channel. The large tensile stress induced by the ZnS-SiO$_2$ stressor in the S/D regions can lead to resistivity reduction in the S/D regions, though the reduction would be lower as compared to that in the channel. Hence, the series resistance reduction can be more significant in the transistor in this work than in a typical transistor with short plug-to-channel distance, due to the long current path between the probe and the channel. Besides, NiSi/Si Schottky barrier height reduction due to the stress-induced bandgap narrowing [168],[169] also play a role in the R_{SD} reduction.

Unlike the conventional liner stressor which exploits the intrinsic stress, the key concept for the new ZnS liner stressor is the expansion of the ZnS material. As mentioned above, ZnS was formed to wrap around the FinFET and then configured to expand in volume post-deposition, so as to induce huge mechanical stress in the FinFET channel. Therefore, when the thickness of ZnS liner is reduced and the space for ZnS to be filled in is extremely shrunk, significant channel stress could still be expected.

(a) Transistor with Small Plug-to-Gate Spacing and Liner Stressor



(b) Transistor in This Work with ZnS-SiO_2 Stressor

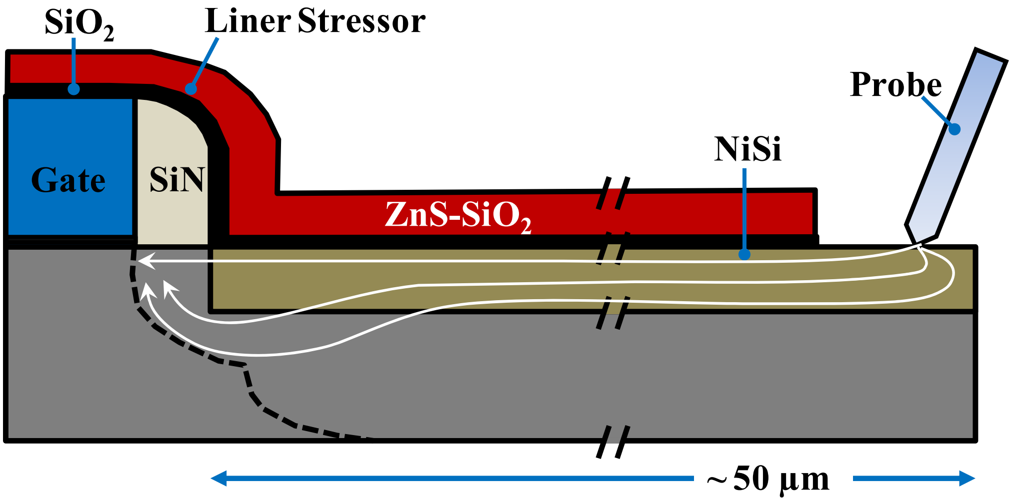


Fig. 5.19. Schematics of (a) typical transistor with very short plug-to-channel distance used in industry with liner stressor and (b) transistor in this work with expanded ZnS-SiO_2 liner, where the probe tip contacts the NiSi far (~50 µm) from the channel.

5.5 Conclusion

A new ZnS-SiO_2 liner stressor that can be made to expand during anneal in front-end processing was introduced in this Chapter. The ZnS-SiO_2 liner was integrated on n-FinFETs with Si:C S/D stressor and Al-incorporated NiSi contacts to reduce the effective electron Schottky barrier height. Significant drive current enhancement was observed for n-FinFETs with as-deposited ZnS-SiO_2 liner over the control FinFETs without liner, due to the intrinsic tensile stress in ZnS-SiO_2. After ZnS-SiO_2 expansion, the expanded ZnS-SiO_2 liner induces a higher tensile stress in the channel region and enhances the Si n-FinFET drive current further. At fixed I_{off} of 10 nA/µm, I_{Dsat} enhancement of ~26% was observed for n-FinFETs with expanded ZnS-SiO_2 liner over the control. I_{Dsat} enhancement is higher for smaller L_G. Electron mobility enhancement induced by ZnS-SiO_2 liner stressor was estimated to be ~53%. This new liner stressor is applicable to both bulk and SOI n-FinFETs. ZnS-SiO_2 liner stressor shows promise for application in n-FinFETs at advanced technology nodes.

Chapter 6

Summary and Future Directions

6.1 Contributions of This Thesis

While the aggressive geometrical scaling of transistors increases the performance-to-cost ratio for integrated-circuit-based products, it has met immense challenges as the transistor enters the deep-submicrometer regime (with gate length smaller than 250 nm), limited by phenomena such as short-channel effects (SCEs), high leakage current (subthreshold leakage or gate leakage), and dielectric breakdown. Alternative means of transistor performance enhancement have been explored recently, such as novel transistor structures, new materials, and strain engineering. To further scale down the transistor dimensions while maintaining good performance, advanced device structures such as ultra-thin-body field-effect transistors (UTB-FETs) and multiple-gate or fin field-effect transistors (FinFETs) are required at sub-20 nm technology nodes. To enhance the performance of such structures, strain technologies have to be developed for integration in UTB-FETs and FinFETs.

It is the main objective of this thesis to explore and demonstrate novel strain engineering techniques in advanced Si transistors, such as nanoscale UTB-FETs and FinFETs.

6.1.1 Strain Engineering of Ultra-Thin Silicon-on-Insulator using Through-Buried-Oxide Ion Implantation and Crystallization

In Chapter 2, we explored a novel way of introducing strain in Ultra-Thin (UT) Body and Buried-Oxide (UTBB) SOI structures by Ge^+ implant into the underlying Si substrate and the formation of localized SiGe regions underneath the UT-buried oxide (BOX) by Crystallization. The localized SiGe regions result in local deformation of the ultra-thin Si. Compressive strain of up to -0.55% and -1.2% were detected by Nano-Beam Diffraction (NBD) at the center and the edge, respectively, of a 50 nm wide ultra-thin Si region located between two local SiGe regions.

The under-the-BOX SiGe technique was integrated in n-channel UTB-FETs (nUTB-FETs). The channel width was designed to be very narrow, and the localized SiGe regions was found by finite-element simulation to induce a longitudinal (source-to-drain direction) tensile stress up to ~3000 MPa in the channel region. Significant drive current enhancement of ~18% was observed for the nUTB-FET with under-the-BOX SiGe compared to the control device. The under-the-BOX SiGe regions may be useful for strain engineering of ultra-thin body transistors formed on UTBB-SOI substrates.

6.1.2 Phase-Change Liner Stressor for Strain Engineering of P-Channel FinFETs

In Chapter 3, a novel $Ge_2Sb_2Te_5$ (GST) liner stressor for enhancing the drive current in p-channel FinFETs (p-FinFETs) was explored. When amorphous GST (α-GST) changes phase to crystalline GST (c-GST), the GST material contracts. This phenomenon is exploited for strain engineering of p- FinFETs. A GST liner stressor wrapping a p-FinFET can be shrunk or contracted to generate very high channel stress for drive current enhancement. Saturation drain current I_{Dsat} enhancement of ~30% is observed for the FinFETs with α-GST liner over unstrained control FinFETs, due to the intrinsic compressive stress in α-GST. When phase-changed to crystalline state, I_{Dsat} enhancement of ~88% was observed for FinFETs with c-GST liner stressor over the control or unstrained FinFETs. The drain current enhancement increases with decreasing gate length. The drain current enhancements for different fin rotations were also investigated, where the rotated FinFETs with c-GST stressor were compared with control FinFETs of the same rotation. Significant I_{Dsat} enhancement was observed for strained FinFETs with various fin rotations, with the highest enhancement observed for 0°-rotated FinFETs due to the directional dependence of the piezoresistance coefficients. GST liner stressor could be a strain engineering option in sub-20 nm technology nodes.

6.1.3 Lattice Strain Analysis of Silicon FinFET Structures wrapped by $Ge_2Sb_2Te_5$ Liner Stressor

In Chapter 4, the local strain components in the source/drain (S/D) and channel regions of Si FinFET structures wrapped around by a GST liner stressor were investigated for the first time using NBD. When the GST layer changes phase from amorphous to crystalline, it contracts and exerts a large stress on the Si fins. This results in large compressive strain in the S/D region of $<\bar{1}10>$-oriented Si FinFETs of up to -1.15% and -1.57% in the <110> (horizontal) and <001> (vertical) directions, respectively. In the channel region of the FinFETs under the metal gate, the GST contraction results in up to -1.47% and -0.61% compressive strain in the <110> and <001> directions, respectively. In the channel region, the <110> compressive strain is higher at the fin sidewalls and lower near the fin center, while the <001> compressive strain is lower at the sidewalls and higher near the center. The effects of the Si fin and GST profiles on the stress distribution were studied using simulation. It was found that having a slanted fin structure would increase the stress at the centre of the fin.

6.1.4 An Expandable ZnS-SiO_2 Liner Stressor for N-Channel FinFETs

In Chapter 5, we reported a novel ZnS-SiO_2 liner stressor to enhance drive current in Si n-channel FinFETs (n-FinFETs). ZnS-SiO_2 expands during thermal anneal due to an increase in crystallite size. A ZnS-SiO_2 liner stressor wrapping around an n-FinFET can be expanded and exerts high tensile stress in the n-FinFET channel for drive current enhancement. Significant drive current enhancement was observed for n-FinFETs with as-deposited ZnS-SiO_2 liner over the control FinFETs without liner, due to the intrinsic tensile stress in ZnS-SiO_2. After ZnS-SiO_2 expansion, the expanded ZnS-SiO_2 liner induces a higher tensile stress in the channel region and enhances the Si n-FinFET drive current further. Saturation drain current enhancement of ~26% and linear drain current enhancement of ~48% were observed for FinFETs with expanded ZnS-SiO_2 liner stressor compared to control FinFETs without liner, with no compromise on short channel effects. The drain current enhancement increases with decreasing gate length. This technology was realized on FinFETs with Si:C S/D stressors and Al-incorporated NiSi contacts. ZnS-SiO_2 liner stressor could be a strain engineering option for n-FinFETs at sub-20 nm technology nodes.

6.2 Future Directions

In summary, this thesis has developed and demonstrated several exploratory concepts and technology options for strain engineering in advanced Si channel transistors, such as UTB-FETs and FinFETs. Promising device performance enhancement results were observed in the preliminary assessment of these technology options. Further exploration and analysis of the proposed concepts have to be done for possible adoption in future CMOS technology nodes. Moreover, the possible adoption of alternative substrate materials will open up new research and development opportunities for the concepts developed in this thesis.

For the under-the-BOX SiGe study, a high leakage current in the strained nUTB-FET with under-the-BOX SiGe was observed. As discussed in Chapter 2, the leakage current may be due to trap-assisted tunneling resulting from Ge diffusing into the UT-BOX and Si layers during the high-temperature anneal and introducing traps there. Annealing at a lower temperature but for a longer duration for SiGe formation could reduce the leakage current, thus improving the yield of nUTB-FETs with under-the-BOX SiGe. Secondly, the channel region has to be covered during the high-dose Ge implant through the UT-BOX to prevent amorphization of the ultra-thin Si layer in the channel. Hence, the localized SiGe regions could only be formed under the BOX adjacent to the channel region, instead of forming directly under the channel region, as illustrated in Chapter 2. In this situation, the device width was designed to be very narrow in order to maximize the stress coupling from the surrounding under-the-BOX SiGe regions to the channel. Having an elevated substrate temperature (e.g. 450 °C) during the Ge implant might help to prevent amorphization of the ultra-thin Si layer, eliminating the need to cover the channel during the implant. This allows under-the-BOX SiGe regions to be formed under the channel and removes the constraint on device geometry design. In addition, integrating raised Si:C S/D stressors and the new under-the-BOX SiGe technique in nUTB-FETs would also be an interesting prospect for further study.

For the GST liner stressor study, the data points from FinFETs with GST stressor are more widely scattered compared to those of the control, as observed in Chapter 3. The immature process flow for integrating the GST stressor could contribute to the device-to-device variation. As discussed in Chapter 3, thickness non-uniformity of the GST and the SiO_2 insulating layer below it and incomplete crystallization of the GST in some regions can all lead to variability in the stress levels, leading to variations in I_{Dsat} enhancement and S/D series resistance reduction from device to device. For future works, the process for integrating a GST liner on FinFETs could be optimized in order to reduce the variation in I_{Dsat} enhancement. For example, the thickness non-uniformity of the GST and the SiO_2 insulating layer below it could be reduced by using CVD deposition. The annealing process for GST crystallization also needs to be optimized to completely crystallize the GST in order to maximize the stress. In addition, the FinFETs in this study have relatively thick spacers (~50 nm), which may reduce the channel stress induced by the GST liner. By reducing the spacer thickness, higher performance enhancement is expected for FinFETs with GST liner stressor. Realizing p-FinFETs with SiGe S/D stressors and GST liner stressor would be another interesting work to explore. Moreover, similar to GST, other phase-change materials such as SbTe and AgInSbTe (AIST) exhibit a comparable volume change rate during crystallization [170],[171]. Further development work can explore the integration of these novel phase-change materials on devices for performance enhancement.

In the ZnS-SiO_2 liner stressor work, a ZnS-SiO_2 liner was deposited by sputtering a ZnS-SiO_2 composite target with 20% ZnS and 80% SiO_2. Firstly, similar to the GST liner, the deposition of $ZnS-SiO_2$ liner could be optimized to achieve better thickness uniformity. Secondly, as shown in Chapter 5, a $ZnS-SiO_2$ liner with higher ZnS composition would have higher volume expansion after anneal (e.g. ~120% crystallite size increase for $ZnS-SiO_2$ with 97% ZnS after 1 hour anneal), which might be able to induce higher stress and therefore larger performance enhancement for n-FinFETs. In addition, to further improve the stress coupling from the $ZnS-SiO_2$ liner to the channel, the $ZnS-SiO_2$ liner should be placed closer to the channel, and it may be worthwhile to study this by using a thinner spacer or removing the spacer before depositing the $ZnS-SiO_2$ liner.

In this thesis, the GST and $ZnS-SiO_2$ liner stressors were explored to enhance the drive current in SOI FinFETs, but the new liner stressors are also applicable to other transistor structures, such as planar MOSFETs, UTB-FETs, bulk FinFETs, and nanowire MOSFETs.

Recently, there has been growing interest in transistors with germanium (Ge), germanium-tin (GeSn), and III-V [e.g. gallium arsenide (GaAs), indium gallium arsenide (InGaAs), indium arsenide (InAs), indium antimonide (InSb), etc.] as higher carrier mobility channel materials. The concepts developed in the preceding chapters could be extended to these alternative substrate platforms and evaluated in terms of device performance enhancement.

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Journal Publications

1. **Y. Ding**, R. Cheng, A. Du, and Y.-C. Yeo, "Lattice strain analysis of silicon fin field-effect transistor structures wrapped by $Ge_2Sb_2Te_5$ liner stressor," *J. Applied Physics*, vol. 113, no. 7, 073708, Feb. 2013.

2. **Y. Ding**, R. Cheng, Q. Zhou, A. Du, N. Daval, B.-Y. Nguyen, and Y.-C. Yeo, "Strain engineering of ultra-thin silicon-on-insulator structures using through-buried-oxide ion implantation and crystallization," *Solid-State Electronics*, vol. 83c, pp. 37-41, 2013.

3. **Y. Ding**, R. Cheng, S.-M. Koh, B. Liu, and Y.-C. Yeo, "Phase-Change Liner Stressor for Strain Engineering of P-Channel FinFETs," *IEEE Trans. Electron Devices.* Vol. 60*,* no. 9, pp. 2703-2711, 2013.

4. **Y. Ding**, Q. Zhou, B. Liu, A. Gyanathan, and Y.-C. Yeo, "An expandable ZnS-SiO_2 liner stressor for n-channel FinFETs," submitted to *IEEE Trans. Electron Devices.* 2013.

Conference Publications

1. **Y. Ding**, R. Cheng, S.-M. Koh, B. Liu, A. Gyanathan, Q. Zhou, Y. Tong, P. S.-Y. Lim, G. Han, and Y.-C. Yeo, "A new $Ge_2Sb_2Te_5$ (GST) liner stressor featuring stress enhancement due to amorphous-crystalline phase change for sub-20 nm p-channel FinFETs," *IEEE International Electron Device Meeting (IEDM)2011*, Washington, DC, USA, Dec. 5 - 7, 2011, pp. 833 - 836.

2. **Y. Ding**, R. Cheng, Q. Zhou, A. Du, N. Daval, B.-Y. Nguyen, and Y.-C. Yeo, "Strain engineering of ultra-thin silicon-on-insulator structures using ion implant," *6th International SiGe Technology and Device Meeting* (*ISTDM*), Berkeley, CA, USA, June 4-6, 2012.

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