THERMAL MODELING AND CHARACTERIZATION OF HIGH-POWER DEVICES

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(B.Eng. (Hons.), NUS)

A THESIS SUBMITTED

FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

DEPARTMENT OF MECHANICAL ENGINEERING

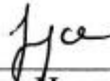
NATIONAL UNIVERSITY OF SINGAPORE

2014

DECLARATION

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.



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14/3/2014

ACKNOWLEDGEMENTS

Firstly, I would like to thank my supervisor Prof. Andrew A.O. Tay for his valuable advices, guidance and motivation throughout my entire PhD candidature.

I would like to thank Mr. Choo Kok Fah (from Temasek Lab @NTU) for his constant strong support towards my research work.

I would like to thank Dr. Teo Jin Wah Ronnie (from SIMTech) for providing his assistance and guidance towards my work on thermal characterization of LEDs.

Finally, I would like to thank Mr Dustin Kendig (from Microsanj) for his advices on the usage of the Thermoreflectance system.

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LIST OF SYMBOLS

A	Area under the Lorentz curve bounded by T_L
C_{TR}	thermoreflectance coefficient
CF_{IR}	Infrared correction factor
ΣC_{th}	Cumulative thermal capacitance
$F(w,L_b)$	Ratio between ($T_{o,max}$-T_∞) over ($T_{o,avg}$-T_∞)
$G(\vec{x},\vec{x'})$	Temperature green function at the field point $\vec{x}$ due to a unit source point $\vec{x'}$
H	Heaviside step function
I_{drive}	Drive current
I_{sense}	Sense current
K	Arbitrary constant
L	Length of a square pixel
L_b	Length of the base
L_g	Length of gate
P_g	Gate pitch
P_{opt}	Optical power
P_T	Total electrical power
ΔP_{opt}	Change in optical power
ΔP_T	Change in total electrical power input
Q	Internal heat generation rate per unit volume
$Q(\vec{x})$	Internal heat generation rate per unit volume at $\vec{x}$
Q_T	Total heat generation inside a sphere
R	Reflectivity
R_o	Initial reflectivity

ΔR	Change in reflectivity
R_{int}	Thermal interface resistance
R_{ja}	Thermal resistance
$R_{ja,real}$	Real thermal resistance
ΣR_{th}	Cumulative thermal resistance
S	Surface that encloses a region V
T	Temperature
$T(\vec{x},\overrightarrow{x'})$	Steady state temperature at any position vector $\vec{x}$ due to a source point at $\overrightarrow{x'}$
ΔT	Change in temperature
T_g	Gate temperature
T_j	Junction temperature
T_L	Curve-fitting constant of Lorentz function
T_o	Base temperature
$T_{o,avg}$	Average temperature at the base of the substrate
$T_{o,max}$	Maximum temperature at the base of the substrate
$T_{o,x}$	Temperature distribution at the base of the substrate along the x axis
T_∞	Temperature at the base of the jig
T_{ref}	Reference temperature
TSP	Temperature sensitive parameter
U	Transformed dependent variable for the Green's function
V	Volume
V_F	Forward Voltage
ΔV	Change in the forward voltage of a diode

W_g	Gate width
a	Height of the heat source from the base of the substrate
b	Thickness of substrate
d	Distance of the heat source from the center of the substrate
$k(T)$	Temperature dependent thermal conductivity
$k(T_o)$	Temperature dependent thermal conductivity at T_o
l	Length of the heat source
l_s	Overall length of the heat sources
n	Number of gates
n'	Outward unit vector normal to S
q_r	Heat flux at the boundary of a sphere
r	Radius of the sphere
r_1	Distance between a specified point to a point heat source
r_2	Distance between a specified point to a sink heat source
w	Width of the Lorentz curve where $T_{o,x} - T_L = (T_{o,max} - T_L)/2$
x	x coordinate of field point
x'	x coordinate of source point
x_c	Center of Lorentz curve
$\vec{x}$	vector of field point
$\overrightarrow{x'}$	vector of source point
y	y coordinate of field point
y'	y coordinate of source point
z	z coordinate of field point
z'	z coordinate of source point

α	Arbitrary constant
β	Angle
β_o	Optimum angle
δ	Dirac delta function
ε	Emissivity
λ	Heat dissipation per unit length
λ_{area}	Heat dissipation per unit length
θ	Transformed dependent variable in terms of T

CHAPTER 1

INTRODUCTION

The operating temperature of any semiconductor devices has an important influence on both its reliability and electrical performance. Excessive channel temperature found in Field Effect Transistors (FETs) can lead to immediate burnout or degrade in performance of devices. Many commercial wireless communication products for telecommunications and military applications are developed based on Monolithic Microwave Integrated Circuit (MMIC) technologies. With increasing demand on the level of miniaturization and integration, the increase in higher power density found on a device has led to a higher operating junction temperature. The maximum operating junction temperature for reliable operation of a device will have a direct influence on the design of the package and the thermal management requirements. Therefore, an accurate knowledge of the operating junction temperature is important to ensure the long-term reliability of a device.

The typical structure of an MMIC transistor consists of air-bridges, metal layers, source, drain and gate (Fig. 1.1). An active layer is formed in the GaAs substrate layer under the mesa layer by doping. The gate is fabricated on top of the mesa layer using optical lithography techniques. The ohmic contacts provide good connection between the interconnect metal and the active junction of the GaAs substrate surface. The first metal layer (Metal 1) deposited acts as an interconnect (e.g. source and drain). The second metal layer (Metal 2) forms the air bridge (Fig. 1.3). The via hole that is etched

through the GaAs substrate connects the device to the backside metal which is grounded.

A top view of a multi-finger MMIC device consisting of 10 gates is shown in Fig. 1.2. The gate geometry is defined as shown in Fig. 1.3, where the gate length refers to the short dimension, gate width refers to the long dimension, and the gate pitch refers to the distance between each gate for a multi-finger device. During operation, the current flows from the source to the drain, resulting in heat generation in the depleted region under the gate (Fig. 1.3). Hence, the maximum temperature of the device occurs under the gate where the actual heat dissipation occurs. This maximum temperature is often defined as the junction or the channel temperature. This junction temperature is different from and higher than the gate temperature, T_g, which refers to the temperature of the gate on the surface. Therefore, the maximum temperature measured by experimental techniques which measure surface temperatures is actually the gate temperature. In this work, the maximum temperature of a device will be defined as the junction temperature, T_j, while the measured maximum surface temperature will be defined as the gate temperature, T_g.

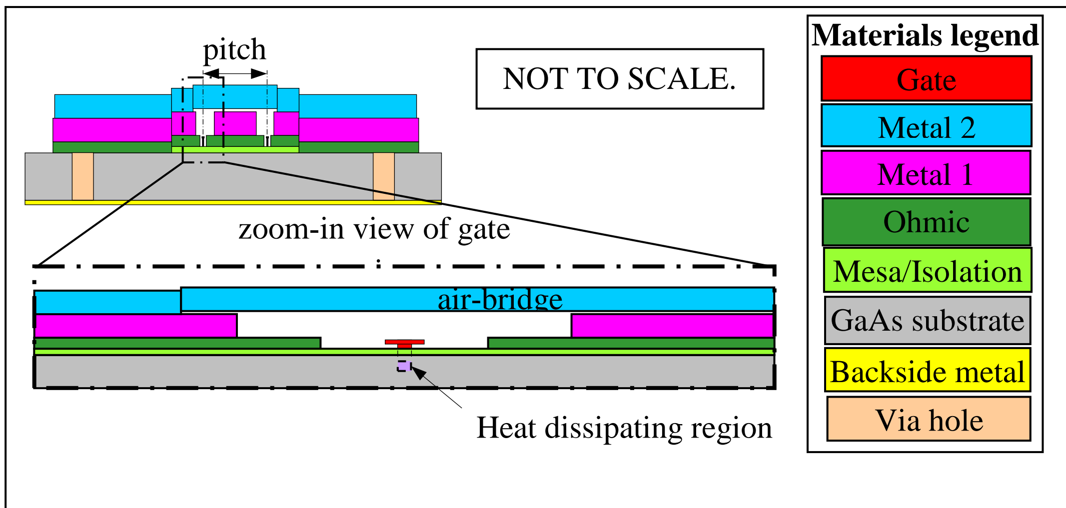


Fig. 1.1. Cross-sectional view of metal layer build-up for one of the transistors in a typical MMIC device

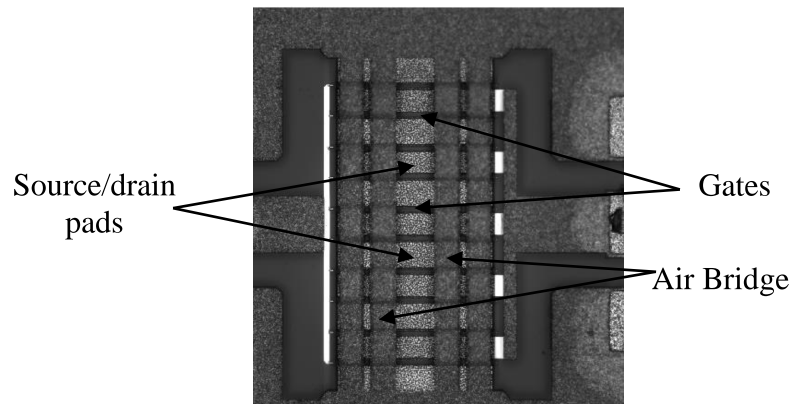


Fig. 1.2. Top view of a multi-finger MMIC device

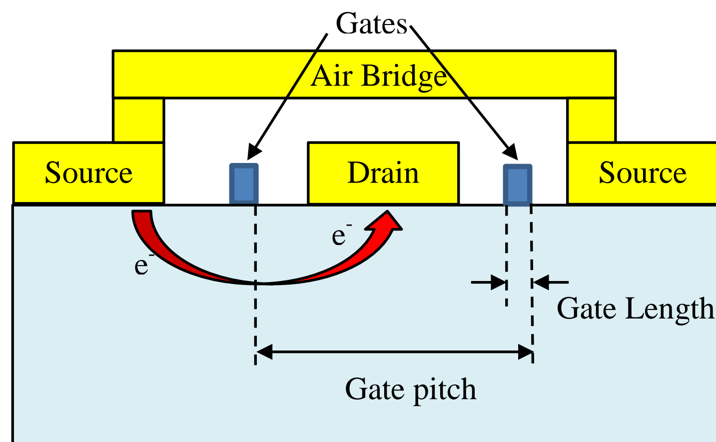


Fig.1.3. Current flows from the source to the drain within the MMIC transistor

1.1. Motivation

A heavy reliance has always been placed on using numerical methods to estimate the peak operating junction temperature of MMIC devices. Finite Element Analysis (FEA) has now been established as an accurate numerical tool for determining temperatures provided the thermal properties, heat loads, device geometry and layout are accurately known. Various models of the heat dissipation region under the gates have been proposed. However, no work has yet been done to study the effects of different models of heat dissipation region on the maximum junction temperature. As a different heat dissipation region will result in a different junction temperature, it is essential to carry out a parametric analysis to understand the effect and sensitivity of the sizes of the heat dissipation region on the maximum junction temperature of an MMIC device.

Analytical methods have also been developed to estimate the peak operating junction temperature. However, long computing time is required when the solution consists of summations of double infinite series. The analytical expression also becomes cumbersome to handle. In addition, the analytical solutions are often limited to simple geometries and boundary conditions. For example, a surface planar heat source was often used to represent the heat dissipation region, whereas the actual heat dissipation takes place in the depletion region found in the active layer below the gate. Therefore in this work, a new closed-form analytical solution has been developed where the location of the heat dissipation region is assumed to be embedded under the gate, which is more realistic. Since it is a closed-form solution, the junction

temperature as well as the temperature distribution around the gate can be easily calculated. This will greatly help to reduce the effort and time required to determine the junction temperature, especially in the early design stages.

The most direct method to determine the peak operating junction temperature is by experimental techniques. Thermal characterization of devices plays an important role in determining their performance and reliability. An accurate temperature measurement can be used to validate a numerical model as well as to verify the accuracy of an analytical solution. There are several techniques for measuring temperature of MMIC devices. The challenges in using the existing characterization techniques for temperature measurement on MMIC chips are insufficient spatial resolution, presence of reflective surfaces and submicron size features present in the MMIC structures. Insufficient spatial resolution in a characterization technique will result in the measured temperature being lower than the actual temperature. Low emissivity surfaces present on most MMIC devices have made Infrared thermography (the most common technique used) unsuitable for thermal characterization. To overcome the problems of previous characterization techniques, a recently developed technique, Thermoreflectance thermography (TRT), will be used to measure the gate temperature of MMIC devices. This work will show that TRT is a good technique for temperature measurement of semiconductor devices.

1.2. Outline of the Work

There are many variations in modelling the heat dissipation region under the gate of MMIC devices. The modelling methodology for power amplifier (PA)

MMIC devices will be studied to investigate the effect and the sensitivity of the heat dissipation region sizes on the maximum junction temperature. A baseline thermal model will be adopted and verified by measured temperatures.

Work will also be undertaken to develop a new and accurate closed-form analytical solution to determine the junction temperature and the temperature distribution around the gate region. This new analytical solution is easier to implement and requires shorter computation time as compared to previous works. In addition, the exact location of the heat dissipation region can be easily taken into account for an accurate estimation of the junction temperature. To account for the correct boundary condition at the base of the substrate in a packaged device, another new analytical method will be developed to obtain the correct temperature distribution at the base of the substrate. It can be used in conjunction with the newly developed closed-form analytical solution to give a more accurate estimate of the junction temperature in a packaged device.

To validate both the thermal model and the developed closed-form analytical solutions, calculated temperatures will be compared with those obtained numerically and experimentally. Infrared thermography (IRT) and Thermoreflectance thermography (TRT) will be employed to measure the gate temperatures of both gallium arsenide (GaAs) and gallium nitride (GaN) PA MMIC. This work will highlight the difficulties and challenges faced in obtaining accurate temperature measurements when using either IRT or TRT.

1.3. Structure of the Thesis

Chapter 1 describes the motivation and outlines the work.

Chapter 2 contains a review of the published works on modelling methodology, analytical methods and experimental techniques for assessing the gate/junction temperature of high power electronic devices.

Chapter 3 describes the work undertaken to study the modelling methodology used to accurately simulate the thermal characteristics of the MMIC.

Chapter 4 describes the formulation of a new accurate closed-form analytical solution for predicting the junction temperatures of FETs and MMICs. For validation, this analytical method will be compared with previous analytical methods and FEA solutions.

Chapter 5 describes the development of a new analytical method to accurately determine the temperature distribution at the base of the substrate in a packaged device. This method, when used together with the new closed-form analytical solution for the temperature distribution within the substrate developed in Chapter 4, helps to estimate more accurately, the peak operating junction temperature of packaged devices using the analytical approach.

Chapter 6 describes the measurement of PA MMIC junction/gate temperatures using two experimental techniques, namely the IRT and TRT.

Chapter 7 describes work done on thermal characterization of Light Emitting Diodes (LEDs). Measurement of junction/surface temperatures was made using the forward voltage method, IRT and TRT. The measurement of the junction to ambient thermal resistance of LEDs using a thermal transient

technique is also described. An analytical solution for the LED junction temperature was also formulated based on the analytical method developed earlier in Chapter 4. To establish its accuracy, the calculated junction temperatures will be compared and validated with experimental results and numerical solutions.

Chapter 8 concludes the main findings of this work.

CHAPTER 2

LITERATURE REVIEW

2.1. Thermal Measurement Techniques

Thermal characterization of devices is important for reliable circuit design. Accurate measurement techniques are important for obtaining an accurate temperature measurement for reliability assessment of devices and validation of analytical and numerical solutions. The types of thermal characterization techniques for temperature measurement range from micro-scale to nano-scale resolution and each has its own advantages and disadvantages [1-3]. For example, micro-Raman spectroscopy has an excellent spatial resolution of 0.5µm. It has been used to determine channel temperatures in AlGaN/GaN device structures [4-6]. The principle of measuring temperature using Raman spectroscopy is based on the dependency of phonon frequency on temperature. Any change in the temperature will lead to a change in the phonon frequency. Therefore, there is a need to determine the initial phonon frequency at a known temperature before biasing the device. The initial phonon frequency is used as a reference for determination of the relative phonon shift due to self-heating. Calibration is required to determine material-dependent fitting parameters before the change in phonon frequency can be calculated. The relative intensities of the Stokes and Antistokes processes measured are related to temperature. Theoretically, the ratio between the two relative intensities is material independent. However in practise, differences in the light absorption and detector sensitivities at different wavelength or frequency have to be taken

into account. To measure temperature using Raman spectroscopy, a probing laser beam needs to dwell at each spot to acquire the Raman spectrum and then move on to the next position. The measurement of both Stokes and Antistokes modes requires long integration times, which makes Raman spectroscopy a slow technique for acquiring temperature fields in devices.

Another temperature measurement technique is Liquid Crystal thermography (LCT) which has a spatial resolution of 2 μm to 5 μm. LCT has been used to measure the peak temperature of GaN-based HFET devices [7-9]. This technique requires a deposition of a thin layer of liquid crystal on the device under test. As the temperature change takes place during the phase transition of the crystal, the colour change of the light reflected from the crystal is related to the temperature. Disadvantages of using LCT include requirement of prior knowledge of the range of temperature to be measured and uncertainties arising from the alteration of the original temperature distribution due to the deposition of a liquid crystal layer on the surface of the device.

Infrared thermography (IRT) is the most common technique used for direct and non-invasive temperature measurement. It has a spatial resolution of 5 to 10 μm which is insufficient for temperature measurement of a submicron size gate. As a result, the measured temperature is an average value over the pixel area. To infer peak gate temperatures from measured temperature, Darwish et. al. [10] had proposed a model for the channel temperature prediction based on IR techniques by reversing the spatial averaging inherent in IR microscopy. The heat source was assumed to be centered within a circular pixel (Fig. 2.1) and the average temperature over the pixel was then found to be related to the peak junction temperature by an infrared averaging ratio, R_{IR}. However, an

inaccurate assumption on the temperature at the base of the substrate was made during the derivation for ease of analysis. In addition, a constant thermal conductivity was assumed for the substrate, which is usually not the case for semiconductor devices.

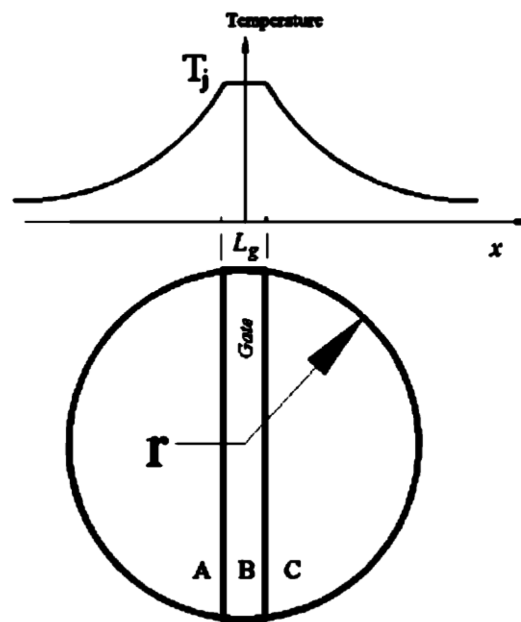


Fig. 2.1. Top view of FET. The IR microscope field of view is a circle of radius *r* centered on the heat source (gate strip). The temperature distribution inside the circle is shown on the curve [10]

The reliability of thermal imaging using IRT is dependent on the properties of the measured sample in question. These include surface emissivity of materials and the measurement environment. A theoretical blackbody has an emissivity value equal to 1. Unfortunately, surfaces of MMIC devices have non-uniform surface emissivities ranging from 0.1 to 0.5. Pixel by pixel emissivity correction is often required in order to obtain a correct temperature measurement [11, 12]. To improve the emissivity value and uniformity of the surface, a thin layer of black paint has been used to coat on the surface [12]. It has been demonstrated that the temperature measured for a coated surface is

higher than that measured for an uncoated surface [13]. For the uncoated surface, the lower temperature recorded is due to reflected infrared radiation from the highly reflective metalized surface (and subsequent error when calibrating a low emissivity surface). Infrared thermography has been used to measure the gate temperature of a GaAs power amplifier MMIC [1, 14-19], AlGaN/GaN transistor structures [5] and FET devices [9].

Despite being an established method for thermal characterization, the inability of IRT to provide sufficient spatial resolution for accurate temperature measurement of current electronic devices with submicron feature sizes, and the presence of low-emissivity reflective surfaces on most semiconductor devices drive the need to look for other alternative methods for thermal characterization. Thermoreflectance thermography (TRT), with a spatial resolution of 0.15μm to 0.5μm depending on the magnification of the objective lens, presents an attractive alternative method for measurement of the temperature of semiconductor devices [2, 20]. The principle behind TRT is the dependence of surface optical reflectivity on temperature. The relation between the change in reflectivity and temperature can be described by the thermoreflectance coefficient which has a small dependence on temperature [21]. However, the thermoreflectance coefficient for most materials is in the order of 10^{-2}/K to 10^{-5}/K. Therefore, the magnitude of the resulting thermoreflectance signal is quite low and poses a challenge in obtaining high quality thermal images. To capture the thermoreflectance signal with reasonable signal-to-noise ratio, an active device needs to be thermally cycled at a known frequency, and a lock-in technique used as well.

TRT recently has been used for thermal characterization of high power transistor arrays [22]. The temperature of MOSFET devices has also been measured using TRT and the random uncertainty of the results has been estimated to be less than 13% [23]. TRT has also been used to study the heat transfer along a silicon nanowire (0.115μm wide and 3.9μm long) suspended between two thin-film heaters [24]. It was demonstrated that the simulated thermal map matches well with the experimental thermoreflectance results. Hence, TRT shows a huge potential for thermal characterization of semiconductor devices.

Another thermal characterization technique is the electrical method [4]. Similar to IRT, the electrical method is non-invasive, fast, and can be performed using widely-available standard equipment. It derives the device temperature from a relationship between self-heating and the reduction in the saturated current of the junction. The accuracy of this method depends on the calibration techniques and assumptions made. One limitation is that the temperature measured by the electrical method averages over the whole active region of the device. In contrast, micro-Raman spectroscopy is able to provide high spatial resolution for thermal device characterization, resolving temperatures that are significantly higher than average channel temperatures.

There are other thermal characterization techniques such as scanning thermal microscopy (SThM) and micro-thermocouple thermometry [2] but they are invasive in nature and not suitable for thermal characterization of MMIC devices.

2.2. Modelling of Heat Dissipation Region Under the Gates

The need to predict the junction temperature of FETs and MMICs has led to many works related to MMIC thermal modelling and analysis using numerical methods [9, 14-16, 25-31]. Some examples of numerical methods include finite elements [16, 29], finite differences [14] and boundary elements [9]. These works presented their heat dissipation region modelling schemes, their rationales for adopting such schemes, as well as the "accuracy" of such schemes when compared with available measured data. The types of heat dissipation region modelled were typically volumetric heat source and planar heat source or thin heat source. A volumetric heat source (VHS) model represents the heat dissipation region as a parallelepiped with finite thickness, while a planar heat source (PHS) represents the heat dissipation region as an infinitely thin rectangle.

The VHS model [14-16, 25-29] has been used extensively in many publications to represent the actual power heat dissipation region in the depleted region under the gate. These VHS models presented in the publications vary in size and depth under the gate. For example, Decker and Rosato [15, 26] had conducted a comparative investigation between numerical thermal analysis and infrared microscopy of TriQuint's TGA9083 GaAs FETs. They had adopted a VHS to model the heat dissipation under the gates. The VHS was modelled to be at a depth of 0.1 µm below the surface of the substrate, and had a thickness of 0.6 µm with gate length of 0.25 µm.

On the other hand, Wilson [14] had adopted another modelling methodology to represent the heat dissipation region under the gates for his GaAs two-stage

power amplifier MMIC for validation of his reliability life test results. In his model, Wilson had included temperature dependent material properties, surface metallization layers, thermal interface resistances at the chip-to-substrate and substrate-to-housing interfaces, and a volumetric heat generation in the depletion region directly below the channels. The VHS model assumed has a height of half the gate height and at a depth equal to the gate height.

Webb and Russell [27] had assumed a non-uniform power distribution within the channel of the device. The VHS dimension and percentage amount of power distribution adopted are shown in Fig. 2.2. Instead of a rectangular VHS under the gate, the heat dissipation regions were modelled as three rectangular VHSs with different geometries at different amount of heat dissipation. Webb and Russell felt that it was not realistic to assume the power distribution to be located at the gate interface in the thermal model. However, they concluded that the precise power distribution was not important as the difference between non-uniform power distribution versus uniform power distribution was very small when assuming the depth of the heat source to be within 0.2 μm to 0.5 μm from the surface. Therefore in his later paper [31], Webb had assumed the heat dissipation region to be directly under the gate within the 0.3 μm channel with each channel dissipating an equal amount of heat. Webb also commented that there was inaccuracy in this assumption as the principal dissipation will be in a volume that is nearer to the drain region in a MESFET and was mainly confined to the collector depletion region in the HBT.

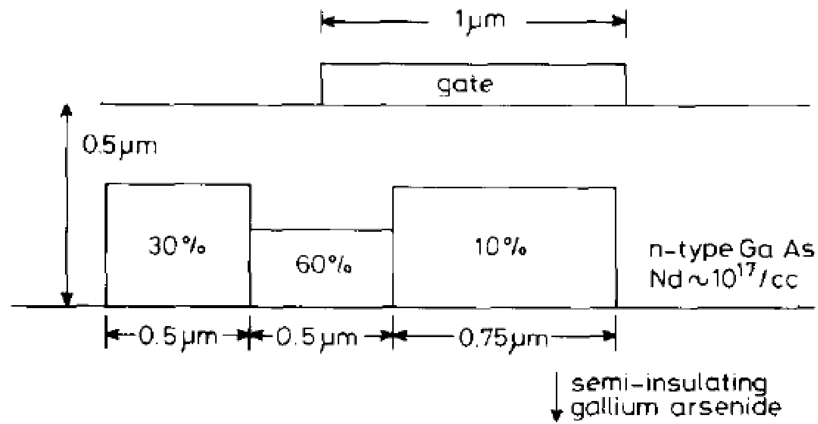


Fig. 2.2. Distribution of the total power dissipated near the gate [27].

Florian et. al. [28] had also assumed volumetric heat sources in his three dimensional thermal model which was solved using a finite difference method. Volumetric heat sources were placed at a depth of 0.1 μm in the GaAs substrate under the gates. The VHS assumed has the same dimension as the gate. The basis for this was that it was "provided by the foundry". It was noted that the modelling methodology for the heat dissipation region under the gates used by Florian et. al. closely resembles the one that had been adopted by Decker and Rosato [15, 26], and Wilson [14]. Other papers by Li et. al. [16] and Chang et. al. [29] had also assumed a similar VHS model under the gates with the same depth to represent the heat dissipation region.

In an earlier paper by Wright et. al. [9], a PHS model had been assumed as the heat dissipation region and was modelled in two ways. In the first model, a PHS was modelled directly under the gate. In the second model, the PHS was modelled to spread over the source and drain spacing. It was suggested that these two models will help to "bracket" the expected maximum junction temperature as the actual power distribution across the FET junction is dependent on the bias conditions applied.

In [30], Ferrara et. al. had used a series of finite element models and sub-models to accurately determine GaAs MMIC junction temperatures. The results had been correlated with temperatures measured using IRT. There was no discussion on how the heat dissipation regions were modelled. However from the rectangular mesh, it was apparent that a surface PHS heat dissipation region had been adopted.

2.3. Analytical Methods

Analytical methods have also been used to estimate the peak junction temperature of MMIC devices. Fourier series techniques had been used in [32-34] to solve for temperature distributions due to a planar rectangular heat source. Lindsted and Surty [32] had developed an analytical solution for a rectangular heat source placed on the top surface of a substrate with constant thermal conductivity, where the solution can be written in a product form by the customary method of separation of variables. To include the effects of temperature dependent thermal conductivity, Gao et. al. [33] had applied the Kirchhoff transformation. Ditri [34] had distinguished his work from the other previous works by including the effects of both the orthotropic and temperature dependent thermal conductivity. The main advantage of using the Fourier series technique is that boundary conditions such as the substrate thickness and the finite finger length are conveniently inherent to the solution. However, the convergence of the resulting double Fourier series can be extremely slow, resulting in very long computation times.

Fourier transformation techniques are also used to develop solutions for planar heat sources at the top surface of substrates. Kokkas [35] had derived an

analytical solution for a three-dimensional problem of heat flow in multilayer structures where power inputs can either be a direct current (dc) or a steady-state alternating current (ac). Although Fourier transformation is supposed to speed up the computation time, a double infinite series consisting of a double integral expression presented in [35], required a long computation time which is similar to a Fourier series solution.

Another approach for developing analytical solutions is by using Green's function. There are already several works, for example [36-40], using Green's function to develop analytical solutions for calculating the temperature distribution in devices such as VLSI, ULSI and Multi-Chip-Module (MCM) with spiral inductors. Oh et. al. [36] had derived a three dimensional analytical solution for temperature distribution in VLSI chips based on the FFT Green function method. It is applicable to multilayer substrates where adiabatic boundary conditions were assumed at the sidewalls of the substrate, and convective boundary conditions assumed at the top and bottom surfaces of the substrate. Constant thermal conductivity was assumed and ambient temperature was taken to be zero for convenience of the computation. The resulting solution consisted of integrals of double infinite series. The temperature distribution due to an interconnect wire with the size of 0.5x2x0.5mm on a 10x10x5mm substrate was calculated and compared with numerical results. It was found to have an error of less than 0.5%. However, the wire size considered was much bigger than that in real integrated circuits.

Wang and Mazumder [37] had derived analytical formulas for multilayer heat conduction Green function with Neumann's sidewall boundary conditions imposed and heat transfer from the top and bottom surfaces by convection to

ambient temperature set at zero. An eigen-expansion technique was used to solve the required heat conduction Green's function equation. Each layer was assumed to have the same dimensions, therefore the heat spreading effect was not considered. In addition, surface heat dissipation regions were assumed in the model. The analytical method was developed for ultra-large-scale integrated (ULSI) circuits consisting of multiple-layer materials.

Crampagne et. al. [38] had tried to generalize the studies done on micro-strip lines with two or three layers of dielectric and determined Green's function for multilayer micro-strip lines having the same geometry. Transverse transmission line technique was used together with the Green's function such that the number of dielectric layers will not be considered as an obstacle in determining Green's functions. The resulting solution consists of summations of infinite series.

Zhao et al. [39] had derived and solved the multi-layered three dimensional problem. The analytical method was developed for the Multi-Chip-Module (MCM) with spiral inductor structures. The Green's function for the three dimensional Poisson's equation was derived under the assumption that the chip horizontal dimensions were infinite. A generalized image method for an arbitrary number of layers was presented. The implementation was based on a heap data structure which dynamically sorts the images for the rapid computation of the near field. However, this method was not efficient for the far field due to slow convergence. Instead, Fast Hankel Transform was used. The combination of the two methods had led to an extremely efficient implementation.

Niknejad et. al. [40] had derived the Green's function over a multilayer substrate by solving Poisson's equation analytically in the z coordinate and numerically in the x and y coordinates. A general Green's function over a multilayer substrate was derived by considering zero temperature and heat flux at the top and bottom surfaces of a chip. Similarly, spiral inductors were considered on the surface of the substrate.

To calculate the junction temperature analytically for devices such as MMIC power amplifiers, the Green's function method was used in [41-44]. Smith [41] had derived an analytical solution for a two dimensional case with constant thermal conductivity. However, temperatures obtained from a two dimensional calculation will be higher than the experiments since the longitudinal heat flow is ignored. On the other hand, Dawson [42] had derived a solution for the three dimensional problem. However, the solution involves solving for three different conditions and constant thermal conductivity was assumed which will result in inaccurate temperature calculated since the materials properties of most if not all semiconductors are temperature dependent. On the other hand, Haji-Sheikh [43] and Islam [44] did eigenfunction expansion of the Green function to obtain a solution in terms of an infinite series and had included the effect of temperature-dependent thermal conductivity. Compared to the Fourier series and Fourier transformation techniques, the Green's function method has obvious advantages. Firstly, the solution is much simpler and the computation time is greatly reduced. In addition, the Green's function integral method is able to yield closed-form solutions as compared to the infinite series solutions obtained using Fourier series and Fourier transformation techniques.

To obtain the junction temperature in FETs and MMICs, the concept of thermal resistance was demonstrated in many works to calculate the corresponding temperature rise over the isothermal surface at the bottom of the substrate. For example, Darwish et al. [45] had approximated the thermal resistance of a FET with a constant line heat source on the substrate to be half that of a cylindrical heat source of diameter equal to the gate length located at the centre of two isothermal planes which were at a distance apart equal to twice the thickness of the substrate (Fig. 2.3). However, such an assumption was not accurate. This was pointed out by Darwish et al.[46] that the isotherms were elliptical in nature towards the bottom of the substrate. Base on this nature, Darwish et al. had accounted for it by considering two regions, i.e. thermal resistance between two half-plane confocal ellipsoids and two half-plane confocal elliptical cylinders (Fig. 2.4). Kirchhoff's transformation was carried out to account for the temperature dependent thermal conductivity. Compared to previous works, the closed-form solution of Darwish et al. [46] allowed for quick estimation of the gate temperature. However, it only allowed for calculation of the gate temperature but not the temperature distribution across the surface. In addition, it was not able to take into account the exact number of gates present in the device, and only gives the gate temperature rather than the junction temperature.

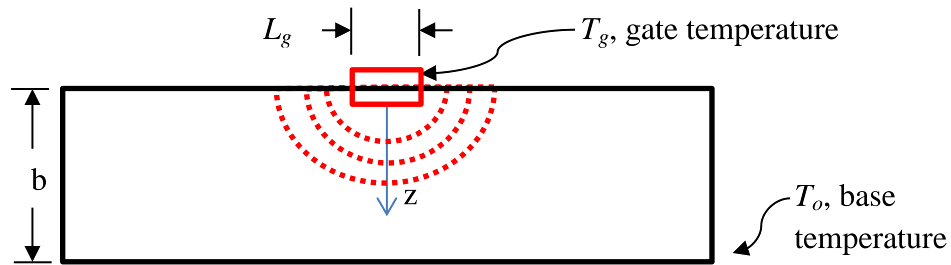


Fig. 2.3. Constant temperature contours represented by red dotted lines are shown in this cross-sectional view of gate finger and substrate [45]

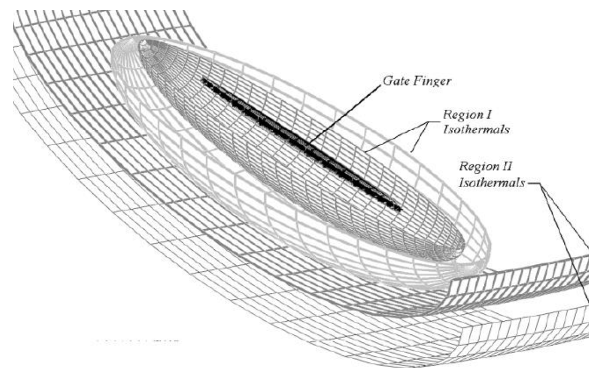


Fig. 2.4. 3-D view of isothermal surfaces for one gate finger in Dawish et. al. [46]. The ellipsoids and the two lower cylinders represent region I and II isothermals, respectively

In [45] and [46], Darwish et al. had considered the thermal resistance of the substrate only. However in the actual application, the substrate is usually soldered attached onto a carrier, which then may or may not be mounted onto some other component [16, 18, 26, 47]. Therefore, there is a spreading resistance to be considered in a packaged device as heat flows from one region to another with a very different cross sectional area. Masana had considered a heat spreading model in [48] and [49]. In [48], two different spreading situations were considered (Fig. 2.5). Both of the chip and substrate dimensions were taken into account. The boundary of the volume was assumed to be sufficiently far from the heat source such that the edge effect can be neglected and spreading will not be constricted by the boundary

surfaces. For small heat sources present in the substrate, a constant spreading angle of 45° was assumed. For multilayer structures, Masana had derived an analytical model in [49] with variable spreading angle for multilayer structures. The analytical model calculates the corresponding thermal resistance value for each layer present in the package structure.

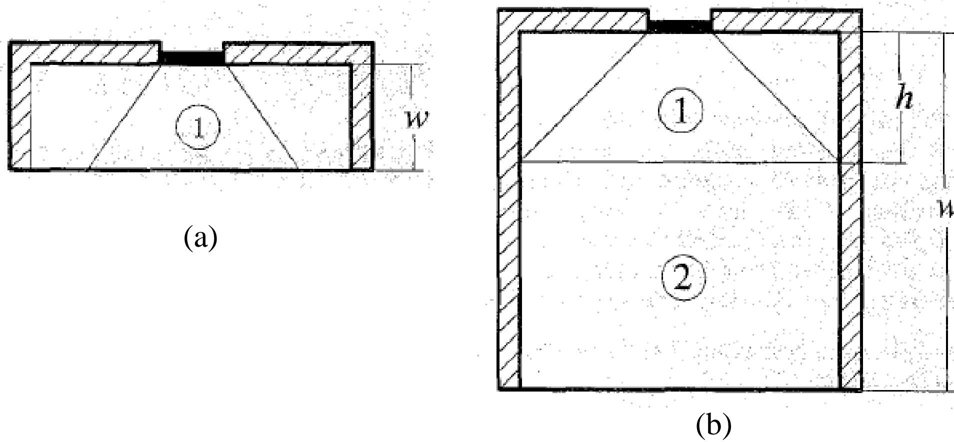


Fig. 2.5. Two different spreading situations: (a) $w_n = \frac{w}{b} \leq 1$ and (b) $w_n = \frac{w}{b} > 1$ [48]

Similarly, Lee et. al. [50] had derived an analytical model for predicting constriction and spreading resistances associated with the heat transfer from various electronic components under different modes of cooling including an isothermal surface at the base. The model assumed a heat source in contact with a large cold plate cooled with a convective heat transfer coefficient specified over the sink surface (Fig. 2.6). Dimensionless expressions in the form of infinite series were provided for computing the average and maximum spreading resistances as a function of relative contact size, plate thickness and the Biot number. The analytical solution was further simplified to become a closed-form solution with accuracy well within 10% and is simple to use.

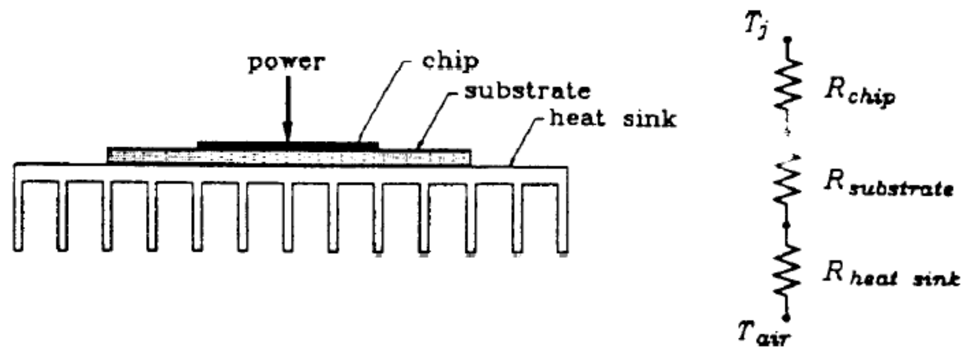


Fig. 2.6. A device is mounted on a substrate which is attached to a heat sink. The thermal resistance network is shown on the right [50]

Qi [51] has also used the concept of thermal resistance by considering a center surface heat source applied at the top layer surface of a tightly spaced array. All surfaces were assumed to be insulated. The thermal resistance solution consists of several infinite series of summation for the stacked structure. In addition, constant thermal conductivity is assumed in the solution.

Other analytical models for determining the spreading resistance in power electronics are also found in [52] and [53]. Arbitrary shape of heat sources on arbitrary shape of substrates were considered in [52] by assuming one dimensional heat flow condition in a single substrate layer. The results have an error of more than 10%. In [53], an analytical solution consisting of summation of infinite series was developed for the determination of thermal spreading resistance with a heat source placed on a three layer substrate with different footprint assumed. To calculate the spreading resistance between the heat source and the spreader layer, the substrate was assumed to have three layers of equal sizes (Fig. 2.7). This may result in an over prediction of the spreading resistance. However, it was stated that the error will become less significant with an increase in the spreading length.

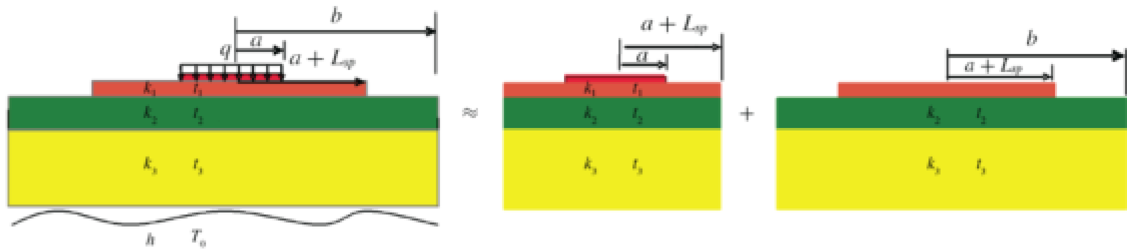


Fig. 2.7. Thermal spreading resistance for a pyramidal structure [53]

2.4. Conclusion

A wide variety of thermal characterization techniques is available for measuring the peak operating junction temperature of semiconductor devices [54]. A summary of the thermal measurement techniques that were described in this chapter is shown in Table 2.1. The ultimate choice of experimental techniques for characterization of the peak operating junction temperature is dependent on several factors such as the spatial resolution of the technique, invasive or non-invasive measurement, the scale of the measured feature, the property of the material and acquisition time of imaging.

IRT is a convenient technique for temperature measurement on features with tens of microns in size. However, limitation on spatial resolution, low emissivity, transparency of various materials and issues related to background radiation pose a challenge in obtaining an accurate temperature measurement. In addition, insufficient spatial resolution of the IR camera causes temperatures measured on a submicron size feature to be lower than its actual peak temperature. Micro-Raman spectroscopy has high spatial resolution. However, a long acquisition time is required for obtaining a temperature distribution over the device surface as the laser takes time to scan across the surface. TRT is based on the change of surface reflectivity as a function of

change in the temperature. Therefore, it is a good substitution for IRT for temperature measurement of semiconductor devices where reflective surfaces are usually present. TRT has a much better spatial resolution as compared to IRT thermography and is also able to provide real time imaging of the surface temperature of the device. Electrical methods result in an average temperature measured. Other invasive techniques such as liquid crystal thermography (LCT), scanning thermal microscopy (SThM) and micro-thermocouple thermometry are not suitable for obtaining the peak operating junction temperature of a MMIC power amplifier device. Invasive techniques will affect the actual performance of devices and poses uncertainties on the measurement results.

Besides obtaining the peak junction temperature by experimental methods, numerical methods can also be used to create an accurate thermal model to represent the actual device. From the literature, we can see that there are uncertainties in defining precisely where the heat is generated under the gates. Volumetric heat source (VHS) and thin heat source (THS) models have been used to model the heat dissipation regions under the gates. The size and depth of the heat sources vary across all papers discussed here. The actual heat dissipation regions modelled in the depletion region are dependent on the bias condition applied [55, 56]. Depletion regions change when the bias condition applied changes. As the heat is highly localised under the gates, the temperature gradient around the gate is large [57]. Hence, the need for consistent definition of the heat dissipation region is of paramount importance as a small change in size and depth of heat dissipation regions and power distribution in the depletion region may cause significant effects on the

predicted junction temperature. Due to insufficient spatial resolution of present temperature measurement techniques, it is challenging to obtain an accurate temperature measurement around the gate region. An accurate thermal model with consistent definition of heat dissipation regions will be helpful in relating the temperature predictions made for a design to an actual application and for optimization studies.

Table 2.1. Summary of Thermal Measurement Techniques

Method	Principle	Advantages	Disadvantages	Spatial Resolution (μm)
Micro-Raman	Shift in Raman frequency or ratio of Stokes/anti-Stokes amplitudes	High spatial resolution	Slow technique for acquiring temperature fields in device	0.5
Liquid Crystal Thermography (LCT)	Crystal phase transition (Color change)	Provides thermal imaging	Requires prior knowledge of the range of temperature to be measured	2 to 5
Infrared Thermography (IRT)	Planck blackbody emission	Provides thermal imaging	Emissivity dependent	5 to 10
Thermoreflectance thermography (TRT)	Temperature dependence of surface reflectivity	Provides thermal imaging, not emissivity dependent	Requires transient conditions	0.15 to 0.5
Electrical method	Relationship between temperature and saturated current of the junction	Non-invasive, fast	Measured temperature is averaged over the whole active region	-
Scanning thermal microscopy (SThM)	Atomic force microscope with thermocouple or Pt thermistor tip	Excellent spatial resolution on smooth surfaces	Contact method	0.05
Micro-thermocouple	Seebeck effect	Easy to use	Contact method	50

To model submicron size features in structures that are few millimetres in dimension, numerical analysis becomes computationally expensive and time consuming as very fine mesh is required around the gate and the junction region in order to obtain an accurate estimation of the junction temperature. Compared to numerical methods, analytical methods require shorter computational time. Although analytical methods have disadvantages in terms of flexibility of the boundary conditions compared to numerical methods, it is still beneficial to use analytical methods to calculate the junction temperature in the early stages of design. A closed-form analytical solution allows for a quick estimation of the peak operating junction temperature when the base temperature of the substrate is known. In addition, the influence of design parameters such as the gate length, gate pitch, location of heat sources and material properties on the peak junction temperature can be easily studied without having to go through the tedious meshing required for numerical analysis.

Unfortunately, all current analytical methods for calculating the junction temperature of an MMIC device have assumed a constant uniform temperature at the base of the substrate. In a packaged device, however, where the substrate is attached to a carrier, thermal finite element analysis (FEA) have shown that the temperature distribution along the base of the substrate is not uniform but has a bell-shaped distribution with a maximum directly below the heat source. Consequently, the current analytical methods which assume a constant uniform temperature at the base of the substrate have been found to be inaccurate. Therefore, a new closed-form analytical method that is able to determine the peak operating junction temperature easily and accurately by

accounting for the temperature distribution at the base of the substrate in a packaged device is desirable.

CHAPTER 3

THERMAL MODELLING OF GAAS POWER AMPLIFIER MMIC

3.1. Problem Statement

Accurate thermal simulations of Monolithic Microwave Integrated Circuit (MMIC) devices to obtain its peak operating junction temperature are often desired. The difficulty in measuring the temperature near the gate makes the numerical approach an attractive one to use. The accuracy of a thermal model is ultimately dependent on having a good understanding of the device parameters. However, there are many uncertainties present in the boundary conditions, how well the model represents the actual system, and in material properties. In addition, precisely defining where the heat is generated is difficult as the heat dissipation region is dependent on the bias voltage applied to the gate which creates a depletion region and locally changes the resistivity of the semiconductor. Different bias conditions applied to the gate will result in different depletion regions and, subsequently, slightly different distributions of heat generation.

There have been publications on MMIC thermal modelling studying various models of the heat dissipation region under the gates [9, 14-16, 25-31]. The heat dissipation region was represented by either a planar or volumetric heat source. The accuracy of each thermal model has been verified by comparing with measured temperatures. However, no work has yet been done to study the effects of the different models of heat dissipation region on the junction temperature. As different models of the heat dissipation region will result in

different junction temperatures calculated, it is essential to carry out a parametric analysis that varies the shape, size and location of the heat dissipation region. Thereafter, a baseline model for modelling the power heat dissipation region under the gate can be adopted so as to effectively relate temperature predictions made for a design to the actual application. It is especially so for higher power density semiconductors such as Gallium Nitride (GaN) as the local temperature gradients become greater.

In this work, the effect and sensitivity of the size and location of the heat dissipation region on the maximum junction temperature of a power amplifier (PA) MMIC will be studied. A detailed metal-layer stack up configuration for an accurate representation of an actual PA MMIC will be presented and compared with its simplified model which helps to reduce the effort required to represent the detailed geometry of the PA MMIC in the numerical analysis. A baseline model will be adopted and compared with the gate temperatures of a PA MMIC measured using Thermoreflectance thermography (TRT) and those calculated using FEA [58]. The baseline model will also be further verified by comparing with previous works [46, 59] and measured temperatures using photoluminescence spectroscopy [60].

3.2. Detailed Thermal Modelling of a PA MMIC

In this section, the detailed thermal modelling of a PA MMIC will be presented. The actual dimensions of the carrier and the aluminium jig have been modelled (Fig. 3.1). The thermal conductivity values used in the thermal model are tabulated in Table 3.1. All thermal conductivities were assumed to be constant except for that of GaAs which is temperature dependent. The

thermal contact/interface resistance between the Cu-Mo carrier and the aluminium jig was set at 193K-mm^2/W [15, 26]. The thermal analyses of this detailed model were conducted with the aluminium jig base (or bottom surface) temperature set at some specified temperature depending on the experimental conditions. The material stack up configuration modelled in the thermal model of the PA MMIC chip is shown in Fig. 3.2. A volumetric heat source (VHS) is used to represent the heat dissipation region under the gates. The dimensions of the VHS are assumed to be equal to the geometry of the gate and at a depth below the mesa layer that is equal to the gate height. The gate has a gate length of 0.25 μm, gate width of 100 μm and gate height of 0.28 μm. This definition of the heat dissipation region will be used as a baseline model for studying the sensitivity and effects of the geometrical parameters of the heat dissipation region on the maximum junction temperature of the device in the later sections.

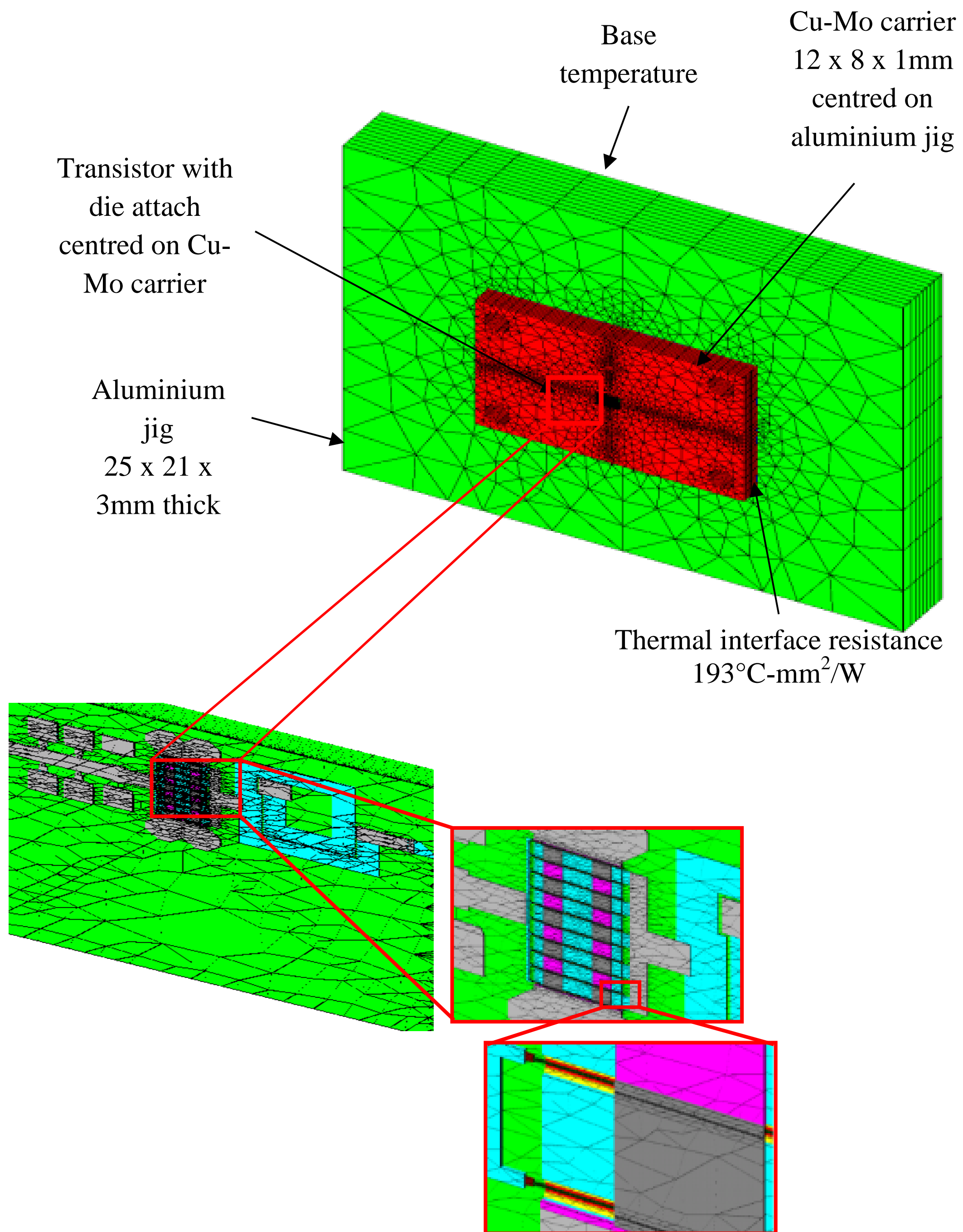


Fig. 3.1. Three dimensional detailed thermal model of PA MMIC

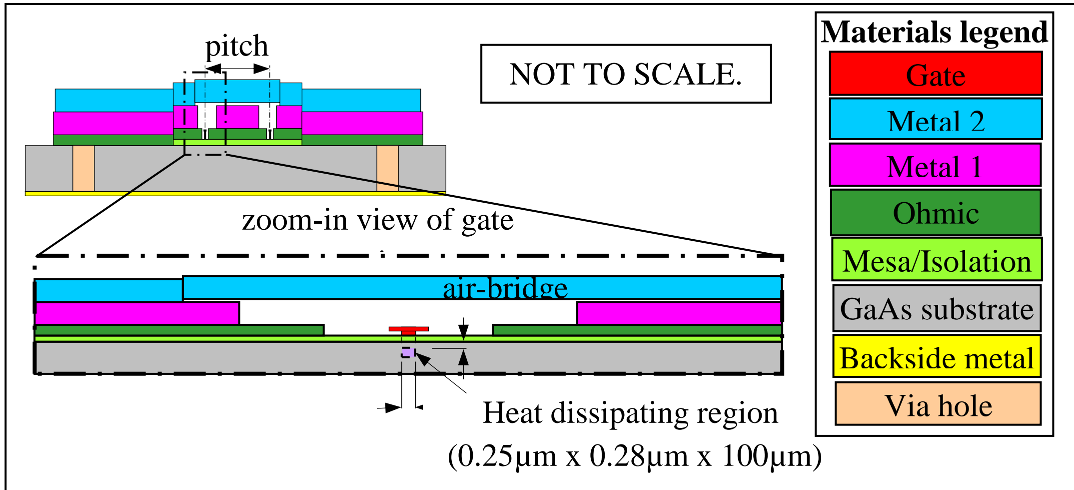


Fig. 3.2. Cross-sectional view of metal layer build-up for one of the transistors in the GaAs PA MMIC

Table 3.1. Thermal conductivity of materials in the GaAs PA MMIC

Materials/Features	Thermal conductivity (W/m-K)		Thickness (µm)
	in-plane	through-thickness	
Gate stem, cap and pad	252.0	90.6	0.28
Metal 2 or top metal	315.0		0.75
Air-bridge and pillar	315.0		0.75
Metal 1 or 1st metal	259.8	110.2	0.85
Ohmic metal	279.5	192.9	0.35
Isolation/Mesa – GaAs	$56968.5 * T^{-1.23}$		0.175
Substrate – GaAs	$56968.5 * T^{-1.23}$		100
Backside metallization	315.0		5
Via Hole – filled gold	315.0		NA
Die Attach – 80/20 AuSn	57.12		40
Carrier - 85/15 Cu-Mo	166.2		1000
Aluminium – 6061-T6	167.5		3000

3.3. Simplified Thermal Modelling of a PA MMIC

The detailed thermal model should yield more accurate results since it is more closely resembles the actual device. However, it requires a great deal of effort and time to mesh the metal layers and air bridges of complex geometries around the gate region for the FE simulation. On the other hand, a simplified model will be much easier to mesh although it will be less precise since the metal layers are ignored. However, a simplified model will be much more useful for carrying out a parametric analysis that investigates the effects of gate pitch, gate width and heat dissipation region on the junction temperature. Hence, a simplified model will be developed and its accuracy will be compared with the detailed model in the later part of this chapter.

In the simplified model, the metal-layer stack-up configuration has been ignored. Only five component parts and the thermal contact/interface resistance between the Cu-Mo carrier and the aluminium jig were modelled. These components include the gate, GaAs substrate, Au-Sn solder, Cu-Mo carrier and the aluminium jig (Fig. 3.3). The exclusion of the metal layers in the thermal model will result in a higher junction temperature calculated since the metal layers aid in the heat spreading from the junction. The effects of the metal layers on the junction temperature will be studied in section 3.4.1.

The actual dimensions and material properties of each component are the same as the detailed model shown in Fig. 3.1. The heat dissipation region modelled is similar to the baseline model adopted for the detailed model, where the VHS is at a depth of 0.28 μm below the substrate surface.

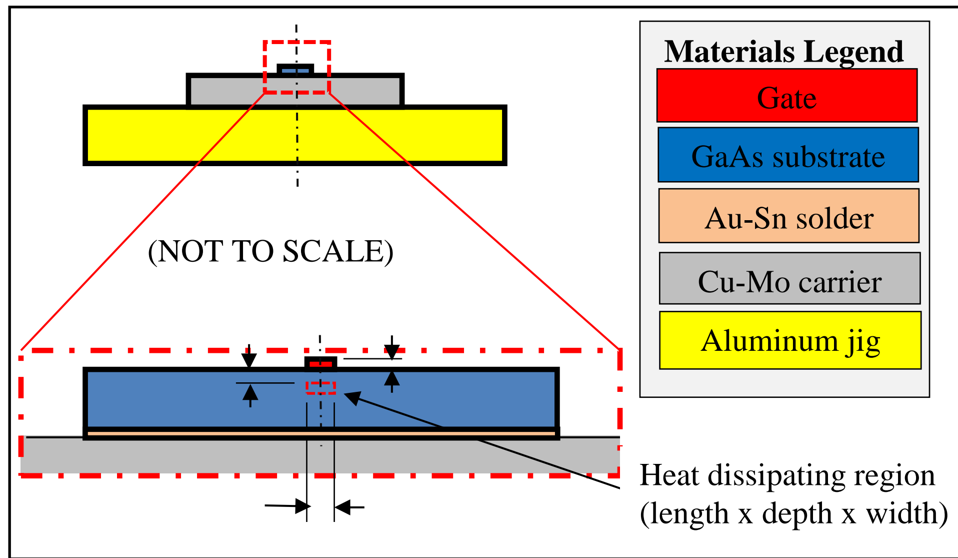


Fig. 3.3. Cross-sectional view of a simplified thermal model of the PA MMIC

3.4. Modelling of the Heat Dissipation Region Under the Gates

In this section, the effects of heat dissipation region shapes and sizes on the maximum junction temperature of a thermal test transistor will be studied using both the detailed and the simplified thermal model. The thermal test transistor is a 10 fingers device with gate width of 100 µm, gate pitch of 32 µm and substrate thickness of 100 µm. A total of ten heat dissipation shapes and sizes have been applied on the thermal models to study the sensitivity and effects of heat source geometric parameters on the junction temperature of the device.

From VHS1 to VHS3, volumetric heat sources (VHSs) are modeled to be embedded in the substrate under the gate with a certain depth as shown in Fig. 3.4. The height of the VHS is varied from 0.14 µm to 0.28 µm. It is noted that the baseline model adopted in this work corresponds to VHS1.

In Fig. 3.5, planar heat sources (PHS) are modeled to be embedded in the substrate except for PHS7 where the heat source is modeled to be on the

surface of the substrate directly under the gate. The depth of the PHS is varied from 0.28 µm to 0.56 µm. The length of the PHS is varied accordingly from the size of the gate length (i.e. 0.28 µm) to the size of the source to drain gap (i.e. 3 µm) since heating due to electrical resistance occurs when current flows from the source (S) to the drain (D).

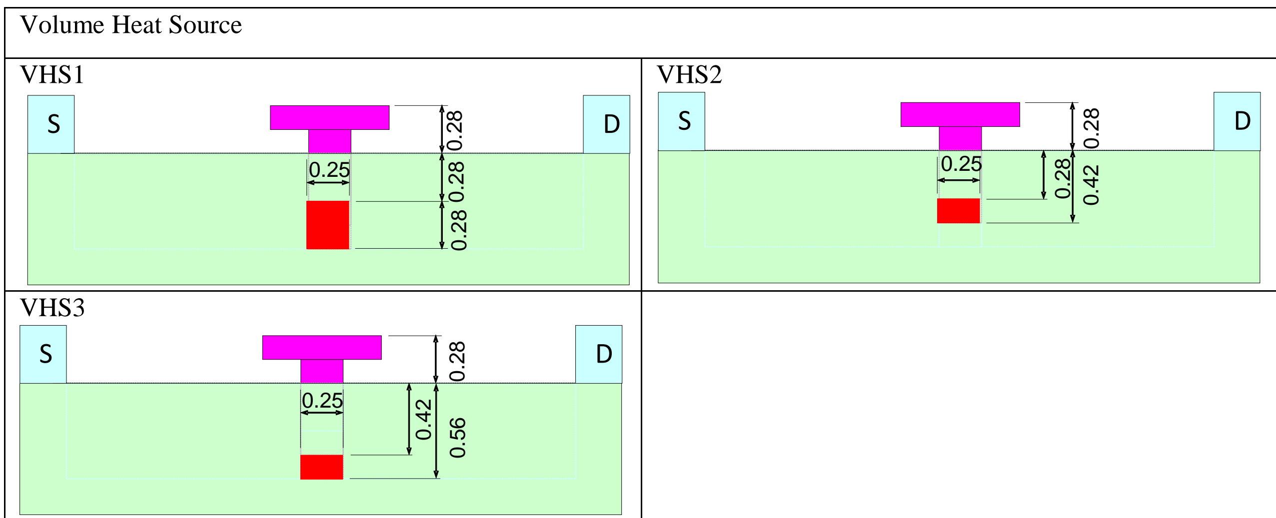


Fig. 3.4. Geometric parameters of volumetric heat source (VHS)

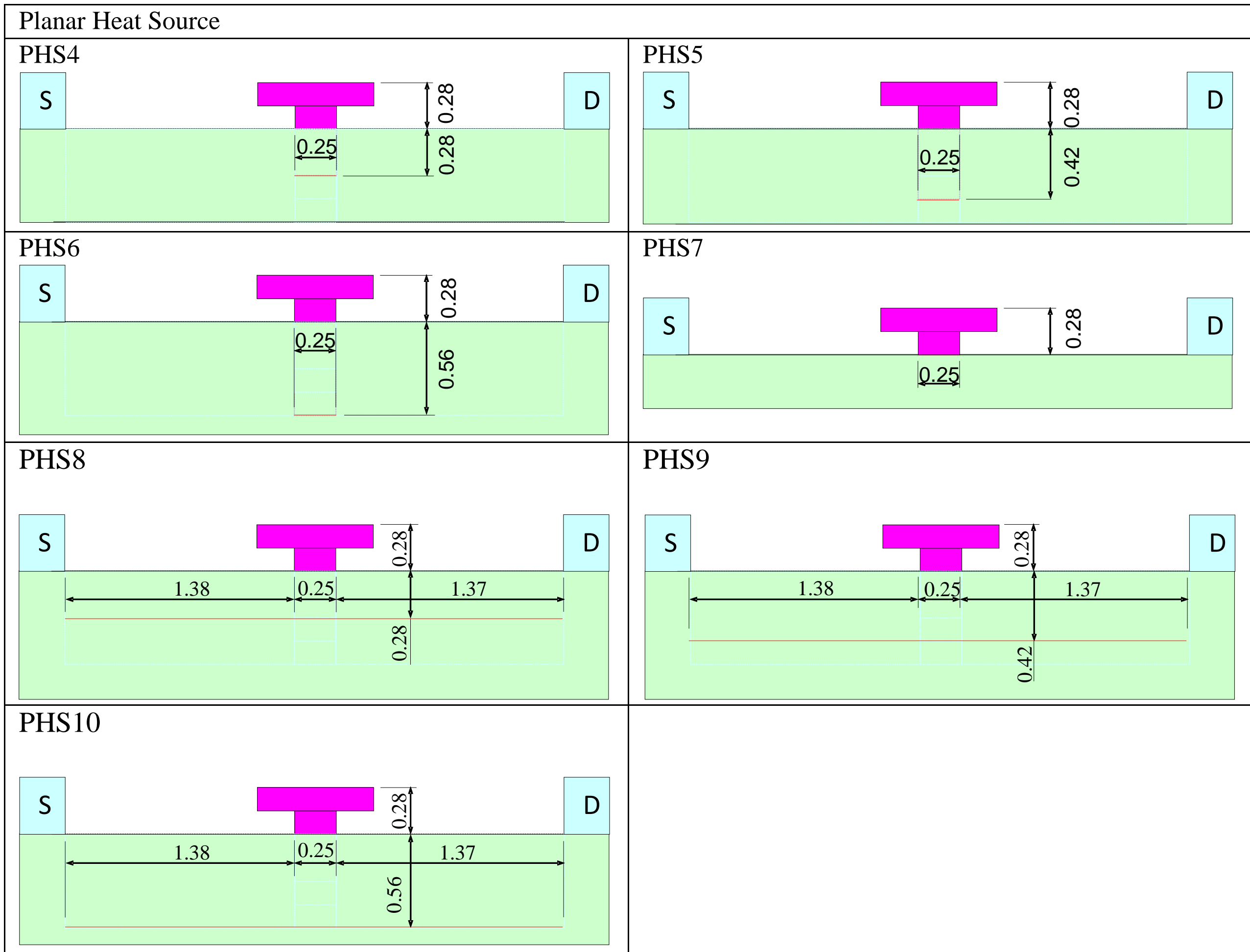


Fig. 3.5. Geometric parameters of planar heat source (PHS)

3.4.1. Sensitivity Analyses Results

In this section, the effects of heat dissipation region shapes and sizes on the maximum junction temperature calculated using both the detailed and simplified model are investigated and summarized in Table 3.2. The power heat dissipation level has been fixed at 1 W/mm. All analyses were conducted with the base temperature of the aluminium jig at 0°C.

Table 3.2. Effects of heat dissipation shapes and sizes on the maximum junction temperature

Heat source and position (µm)					Detailed Model		Simplified Model		Temperature difference between the detailed and simplified model
Type	Length	Width	Height	Depth	T_{max}	% diff	T_{max}	% diff	
VHS1	0.25	100	0.28	0.28	60.3°C	Baseline	65.2°C	Baseline	4.9°C
VHS2	0.25	100	0.14	0.28	61.1°C	1.33%	67.8°C	3.99%	6.7°C
VHS3	0.25	100	0.14	0.42	60.0°C	0.50%	65.0°C	-4.13%	5.0°C
PHS4	0.25	100	-	0.28	62.6°C	3.81%	67.8°C	4.31%	5.2°C
PHS5	0.25	100	-	0.42	61.6°C	2.16%	66.7°C	-1.62%	5.1°C
PHS6	0.25	100	-	0.56	60.8°C	0.83%	66.1°C	-0.90%	5.3°C
PHS7	0.25	100	-	0.00	68.4°C	13.43%	78.7°C	19.06%	10.3°C
PHS8	3	100	-	0.28	55.4°C	-8.13%	62.1°C	-21.09%	6.7°C
PHS9	3	100	-	0.42	55.0°C	-8.79%	60.9°C	-1.93%	5.9°C
PHS10	3	100	-	0.56	54.5°C	-9.62%	60.3°C	-0.99%	5.8°C
Average Maximum Junction Temperature					60.0°C	0.50%	66.1°C	1.63%	6.1°C

From Table 3.2, analysis of the results has shown that:

- The absolute maximum junction temperature tends to decrease when the depth of the heat dissipation region is increased. This tendency is due to the presence of more materials for heat spreading when the heat dissipation region is embedded deeper into the mesa/active region of the transistor.
- The maximum junction temperature calculated for the detailed model (excluding PHS7 to PHS10) can be reduced by 1 to 1.8°C and 0.3 to 1.1°C for every 0.28 µm increase in the depth of the PHS and VHS, respectively. Similarly, the maximum junction temperature calculated for the simplified model can be reduced by 1.1 to 1.7°C and 0.2 to 2.8°C, respectively.

- The largest variation from the baseline model occurs from the PHS7 model where the heat dissipation is modelled by a plane heat source on the surface directly under the gate.
- Similarly for heat dissipation region modelled in the source to drain spacing, PHS8 to PHS10 models showed large variation from the baseline model.
- Therefore, it is shown that a VHS model is less sensitive to changes in size and depth of the heat dissipation region as compared to a PHS model.
- It is noted that PHS7 modelled directly under the gate will tend to overestimate the maximum junction temperature by 13.43% and 21.08% in both detailed and simplified thermal models, respectively, when compared to the baseline model. The accuracy of the PHS model can be improved by modelling the heat dissipation region to be embedded in the substrate.
- It is noted that the VHS2 model shown in Fig. 3.4 closely resembled the heat dissipation region used by Wilson [14].
- The maximum junction temperatures obtained from the PHS7 and PHS8 models in both the detailed and simplified models form the upper and lower limit for the expected maximum junction temperature obtained from the baseline model. This observation is in agreement with that of Wright et al. [9], i.e. by assuming both the heat dissipation region to be directly under the gate (e.g. PHS7) and spreading over the source to drain spacing (e.g. PHS8), it will help to bind and bracket the junction temperature of the actual power profile.
- Therefore, these studies have verified that the baseline model provides a reasonable accurate simulation of the heat dissipation under the gates.

3.4.2. Temperature distribution around the hottest gate

In this section, the effects of the geometric parameters of the heat dissipation region on the heat flow under the gate are investigated. The temperature distribution around the hottest gate is shown in Fig. 3.6 and Fig. 3.7. Only the temperature contours from 45°C to 69°C are plotted.

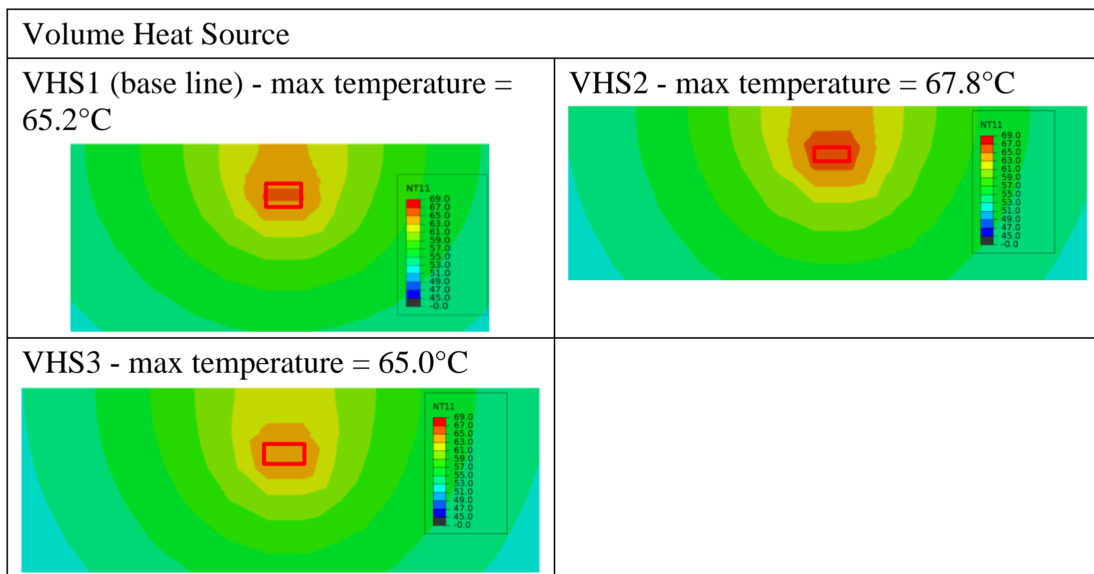


Fig. 3.6. Temperature distribution around the hottest gate for VHS simplified models

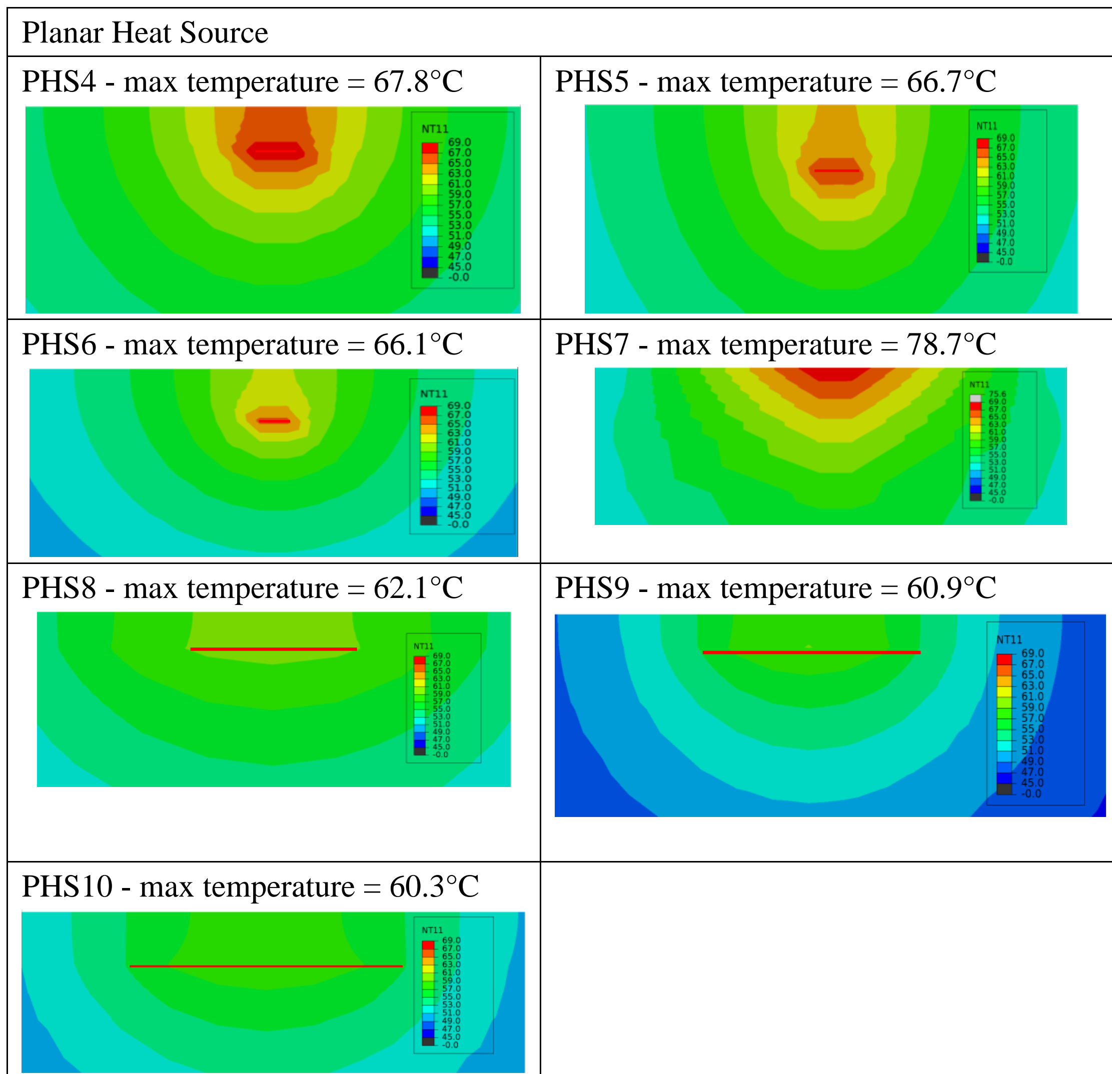


Fig. 3.7. Temperature distribution around the hottest gate for PHS simplified models

3.5. Comparison with Experimental Results

In this section, the temperatures calculated using FEA will be compared with experimental values obtained using thermoreflectance thermography (TRT) and photoluminescence spectroscopy. Since these two experimental techniques measure surface temperatures, we can only obtain the temperature of the gate which is at the surface, and not the junction temperature which is higher in magnitude and located a small distance below the gate. In Table 3.2, the peak junction temperatures, i.e. the maximum temperature in the device,

calculated from the FE thermal model occurs at where the heat dissipation region is. Since the temperatures measured by the two experimental techniques mentioned above correspond to the gate temperature, i.e. the surface temperature above the actual heat dissipation region, the gate temperatures obtained from the FE thermal models will be used to compare with the measured temperatures.

3.5.1. Thermoreflectance Thermography Results

In this section, the peak gate temperatures calculated using both detailed and simplified models based on the baseline model VHS1 are compared with the maximum gate temperatures of both GaAs and GaN PA MMIC measured using Thermoreflectance thermography (TRT). Details of the measurement of temperature using TRT are given later in Chapter 6.

a. GaAs PA MMIC

The test chip of the GaAs PA MMIC is attached onto a Cu-Mo carrier with AuSn solder and assembled into an aluminium jig for thermal characterization. The test jig consists of two clusters of 10 transistors with a gate length of 0.25 μm, gate width of 150 μm and gate pitch of 24 μm. The metal-layer stack-up configurations for both detailed and simplified thermal model are shown in Fig. 3.2 and Fig. 3.3. The base of the aluminium was maintained at 25 ^{o}C by a thermal chuck. The Thermoreflectance Image Analyzer used has a spatial resolution of 0.232 μm when coupled with a 50X objective lens. The results are plotted in Fig. 3.8. It should be noted here that since the measurements of

temperature are those of the surface of the device, the gate temperatures from the FEA results are used for comparison and not the junction temperatures.

From Fig. 3.8, it can be seen that the maximum gate temperatures obtained using the simplified thermal model is higher than that obtained using the detailed model by about 3°C and 8°C at 1W/mm and 1.5W/mm, respectively. This result is expected due to the presence of metal-layers in the detailed model which helped to facilitate metal heat spreading and lead to lower surface temperatures. The error between the simplified model and the detailed model is also on the conservative side. Hence, for design purposes, the simplified thermal model can be used with confidence. In addition, it can also be seen that the measured temperatures using TRT agree very well with the finite element results. Therefore, these results provide justification for adopting VHS1 model as the baseline model.

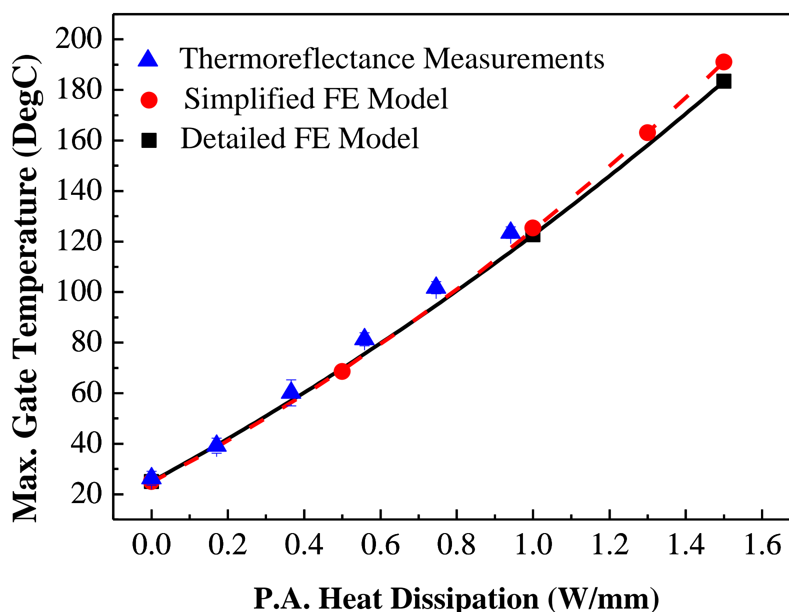


Fig. 3.8. Numerical and TRT measured temperatures for the PA MMIC

b. GaN PA MMIC

Similar to the GaAs PA MMICs, the test chip of the GaN PA MMIC was soldered onto a Cu-Mo carrier with silver epoxy adhesive and assembled into an aluminium jig for thermal characterisation. The test jig consists of 2x150 μm transistors with a gate length of 0.3 μm and gate pitch of 48 μm.

The actual dimensions of the carrier and the aluminium jig are similar to the GaAs PA MMIC shown in Fig. 3.1. The thermal conductivities of materials present in the GaN PA MMIC are tabulated in Table 3.3. The metal-layer stack-up configuration used during the fabrication of the GaN PA MMIC is shown in Fig. 3.9. The detailed thermal model of the GaN PA stack-up configuration is shown in Fig. 3.9. The interface thermal resistances between (i) Cu-Mo carrier and the aluminium jig (ii) and between GaN and silicon substrate are 193°C mm^{2}/W and 3.3 x 10^{-8} m^{2} K/W, respectively. A simplified model, consisting of only the gate, GaN substrate, Si substrate, die attach, carrier, aluminium jig and interface thermal resistances, was also modelled for comparison with the measured gate temperatures.

Table 3.3. Thermal Conductivity of materials in GaN PA MMIC

Materials/Features	Thermal conductivity (W/m-K)		Thickness (µm)
	in-plane	through-thickness	
Gate stem, cap and pad	252.0	90.6	0.3
Metal 2 or top metal – gold	315.0		5
Metal 1 or 1st metal	259.8	110.2	1.05
Ohmic metal	279.5	192.9	0.23
Isolation/Mesa – GaN	$141.39\ (298 / T)^{1.2112}$		0.15
GaN layer	$141.39\ (298 / T)^{1.2112}$		2.2205
Substrate – Si	$152.59\ (298 / T)^{1.334}$		200
Die Attach – Silver base epoxy	75.0		75
Carrier – 85/15 Cu-Mo	166.2		1000
Aluminium – 6061 – T6	167.5		3000

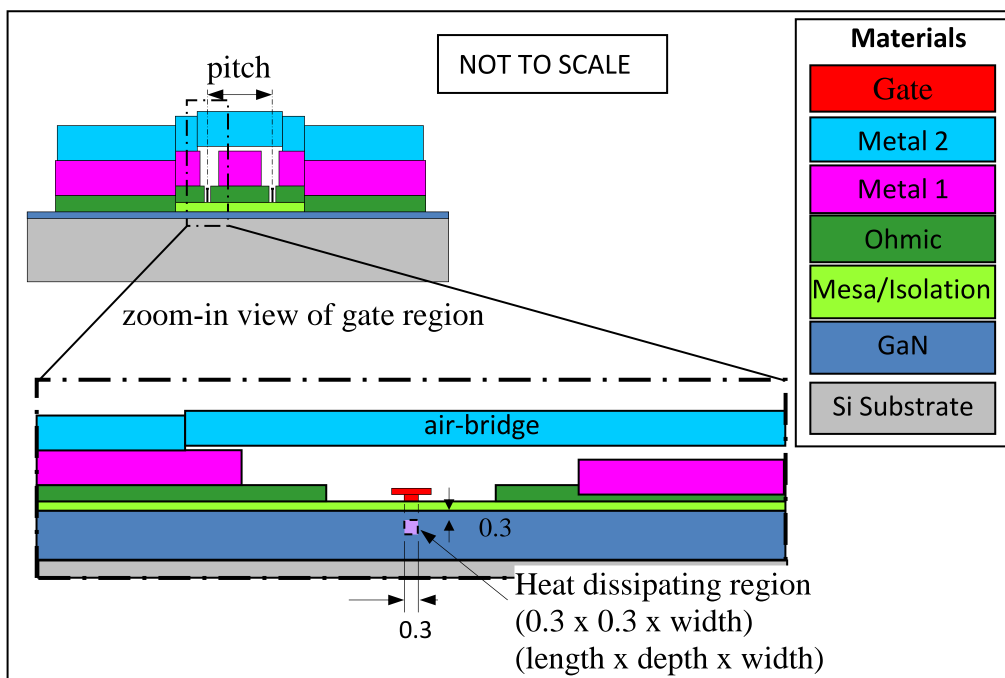


Fig. 3.9. Cross-sectional view of metal layer build-up for one of the transistors in the GaN PA MMIC

During testing, the base temperature of the test jig has been kept at a constant temperature of 25 °C and at an elevated base temperature of 70 °C by a thermal chuck. The Thermoreflectance Image Analyzer used has a spatial

resolution of 0.15 μm when coupled with a 100X objective lens. Values of the maximum gate temperature measured using TRT at each heat dissipation level and aluminium jig base temperature of 25°C and 70°C are plotted in Fig. 3.10 and Fig. 3.11, respectively. Similarly, the calculated gate temperatures obtained from FE solutions are also plotted in Fig. 3.10 and Fig. 3.11 for comparison.

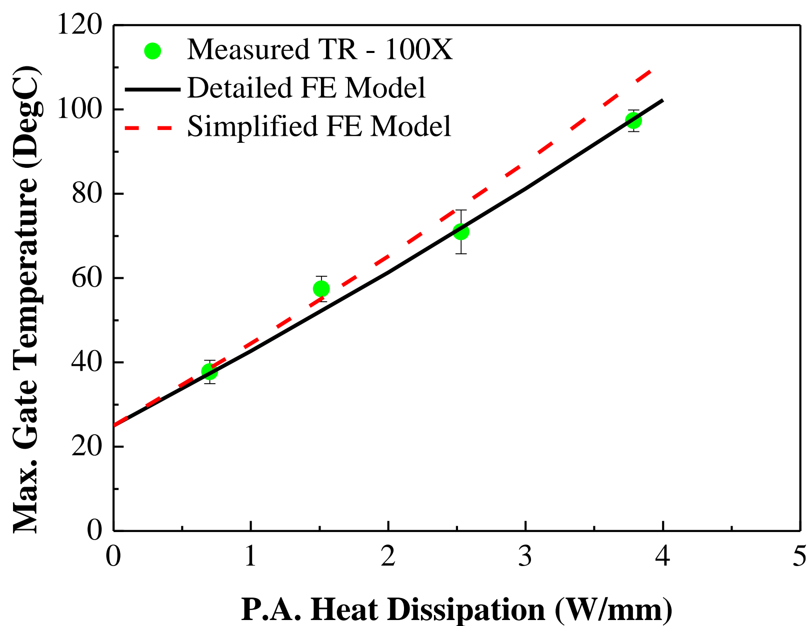


Fig. 3.10. Comparison of maximum gate temperatures for the PA MMIC with aluminium jig base temperature of 25°C measured using TR and IR thermography with those calculated using FEA

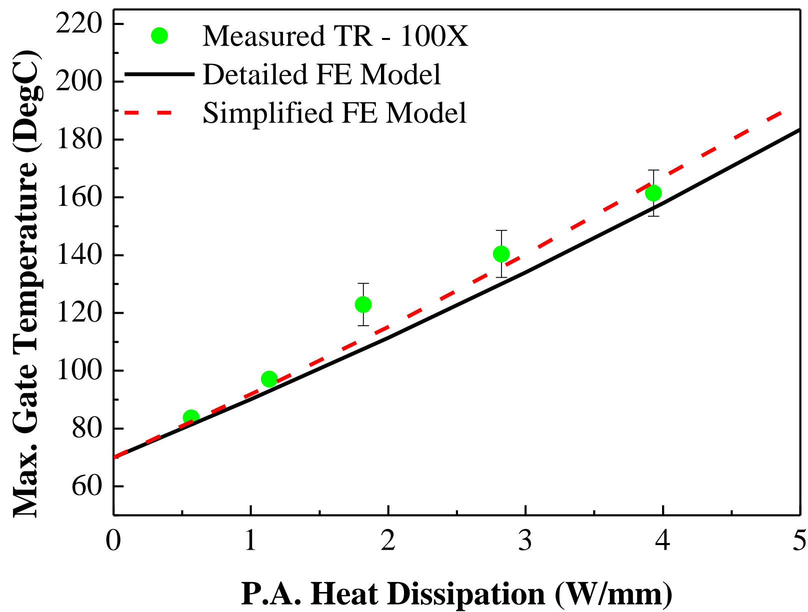


Fig. 3.11. Comparison of maximum gate temperatures for the PA MMIC with aluminium jig base temperature of 70°C measured using TRT and IRT with those calculated using FEA

From Fig. 3.10 and Fig. 3.11, it can be seen that the maximum gate temperatures obtained using the simplified thermal model is higher than that obtained using the detailed model by about 8°C and 10°C at 4W/mm for jig base temperature at 25 °C and 70 °C, respectively. This result is again expected due to the presence of metal-layers in the detailed model which helped to facilitate metal heat spreading and lead to lower surface temperatures.

From Fig. 3.10 and Fig. 3.11, it can be seen clearly that the measured gate temperatures using TRT agree very well with the finite element results. Therefore, these results provide another justification for adopting VHS1 model as the baseline model.

3.5.2. Photoluminescence Spectroscopy Results

In this section, the gate temperature rises calculated by using the baseline FE thermal model VHS1 are compared with the measured gate temperature rises using photoluminescence spectroscopy [60] on a 4x50µm, 0.25µm gate length GaAs pHEMT device and plotted in Fig. 3.12. In the thermal model, the metal thickness of drain and source has been ignored in the model and the base of the substrate was maintained at 30 ^{o}C. As shown in Fig. 3.12, the close agreement between FEA results with the measured temperatures has verified the adopted baseline VHS1 model. The calculated gate temperature rises using Darwish [46] and Cooke [59] models are also plotted in Fig. 3.12 where it can be seen that Darwish's model agrees well with our present model while Cooke's model gave temperatures which are too high.

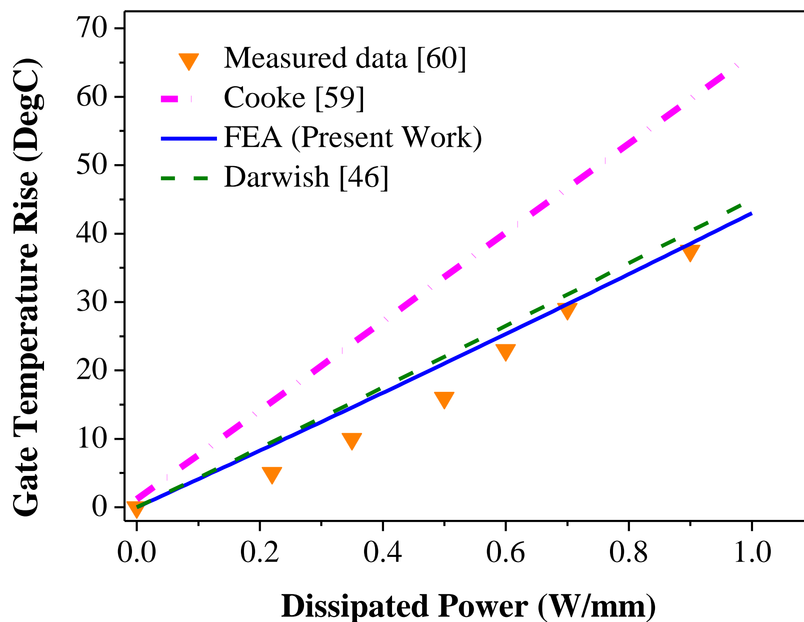


Fig. 3.12. Comparison between calculated and measured gate temperature rise for the 4x50µm, 0.25µm gate length GaAs pHEMT device

3.6. Conclusion

In this work, the effects of geometrical parameters of the heat dissipation region on the maximum junction temperature of a PA MMIC have been studied. The maximum junction temperature modelled by a volumetric heat source (VHS) model is less sensitive to changes in size and depth of the heat dissipation region as compared to a planar heat source (PHS) model. The accuracy of a PHS model can be improved when an appropriate depth of the heat source is included.

From the sensitivity analysis study, a baseline model has been adopted to represent the heat dissipation region and has been experimentally verified using Thermoreflectance thermography on a power amplifier (PA) MMIC. The calculated temperatures using the baseline model were also compared with (i) analytically calculated temperatures from other work and (ii) measured temperatures using photoluminescence. The close agreement between finite element results with measured temperatures and Darwish's results [46] has indicated that the thermal modelling methodology can be used to simulate the thermal characteristics of MMIC devices accurately.

CHAPTER 4

A NEW ACCURATE CLOSED-FORM ANALYTICAL SOLUTION FOR JUNCTION TEMPERATURE OF HIGH-POWERED DEVICES

4.1. Problem Statement

Understanding the thermal issues associated with power amplifier FETs and MMICs is important for determining the performance and reliability of these devices. The reliability of many integrated circuit packaging failure mechanisms has been found to be dependent upon the temperature gradients, magnitude of the temperature cycles, rate of temperature change, or the absolute temperature. Therefore, the junction temperature must be controlled to meet both the performance and reliability requirements.

Numerical approaches are commonly used to estimate the peak operating junction temperature. The accuracy of this method is dependent on the accuracy of the device geometry and the layout being modelled. In addition, it can be computationally expensive and time consuming when investigating the effect of the design parameters such as the gate length, gate pitch, location of heat sources, and material properties on the performance of the device. On the other hand, analytical methods will allow for quick estimation of the junction temperature without having to go through the tedious meshing required for numerical analysis.

Several works have been done to develop analytical solutions to solve for the temperature distribution in field effect transistor (FET) devices. These analytical methods are based on the Fourier series solution [32-34, 61],

Fourier transformation techniques [35], Green's function method [41-43] and even the thermal resistance method [46, 51, 52]. However, the convergence of the resulting double infinite series present in most of the previous analytical methods is extremely slow, resulting in very long computation time. Furthermore, the heat dissipation region in a high-power microwave device is often represented by a surface planar heat source in past analytical models which is inaccurate. As illustrate in This is because the actual heat dissipation takes place in the depletion region found in the active layer below the gate. Although the use of a thermal resistance network allows for quick estimation of the junction temperature, it is not able to account for the exact number of gates present in the device. In addition, it only allows for calculation of the junction temperature but not the temperature distribution across the surface.

In this section, a new accurate closed-form analytical solution for the junction temperature of power amplifier FETs or Monolithic Microwave Integrated Circuits (MMICs) will be developed. Unlike most previous works, the location of the heat dissipation region will be assumed to be embedded in the substrate some distance under the gate. As illustrated in Fig. 3.4, the actual heat dissipation region is a cuboid of square cross-section (where the length of the square is approximately equal to the length of the gate) and length equal to the width of the gate. Since the length of the gate (typically 0.25 μm) is very much smaller than the width of the gate (typically 100 μm), the heat dissipation region will be modelled by a finite line heat source which closely resembles the actual situation. The derivation for this closed-form steady-state three-dimensional analytical solution will be based on the Green's function integral method for a point heat source developed through the method of images. Since

it is a closed-form solution, the junction temperature as well as the temperature distribution around the gate can be easily determined. Consequently, the effects of various design parameters and material properties affecting the junction temperature of the device can be easily investigated. This analytical solution will also be applicable to multi-finger devices by employing superposition techniques. The accuracy of this present analytical method will be established in this section by first assuming a constant temperature at the base of the substrate. It will be shown that the common assumption of a surface planar heat source will lead to an overestimation of the junction temperature. For predicting the peak operating junction temperature in a packaged device, this analytical method can be used in conjunction with a novel analytical method developed in Chapter 5 for determining an accurate temperature distribution at the base of the substrate in a packaged device.

4.2. Derivation of Temperature Distribution due to a Finite Line Heat Source Embedded in a Substrate with Temperature Dependent Thermal Conductivity

4.2.1. Problem Description

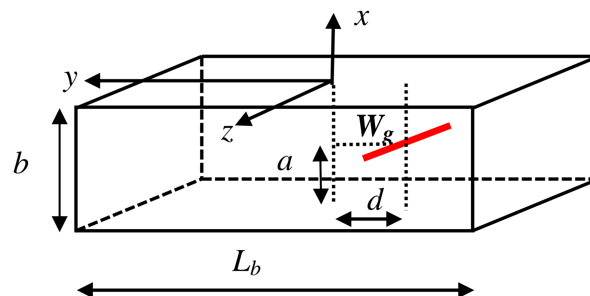


Fig. 4.1. Substrate subjected to an embedded constant line heat source of finite length W_g, and a base at a constant temperature. The remaining surfaces are assumed adiabatic.

Consider a line heat source of length $l = W_g$ embedded in a substrate of thickness b as shown in Fig. 4.1. The heat source is located at a distance a from the base of the substrate and at a distance d from the center of the substrate. The thermal conductivity k is assumed to be temperature dependent. The following assumptions are made:

1) The sides and the top surfaces of the substrate are adiabatic. Convection and radiation heat losses at these surfaces are assumed to be negligible.
2) The bottom of the substrate is an isothermal surface at constant temperature T_o.
3) A finite line heat source of constant strength and of length l equal to the gate width, W_g, can be used to represent the heat dissipation region since the gate length is very small (~0.25μm).
4) Furthermore, this line heat source is embedded some distance below the surface of the substrate. This is justified, as the actual heat dissipation in FETs and MMICs occurs in the depletion region of the active layer which is some distance below the gate [14, 55].
5) The lateral dimension of the substrate, L_b, is assumed to be large enough that it has no effect on the temperature distribution around the heat source.
6) The substrate has a temperature dependent thermal conductivity (which is often the case for almost all semiconductor materials).

4.2.2. Formulation

In this section, the steady-state three-dimensional temperature distribution due to a finite line heat source embedded in a solid of temperature dependent

thermal conductivity will be developed. The Green's function integral method for a point heat source will be employed.

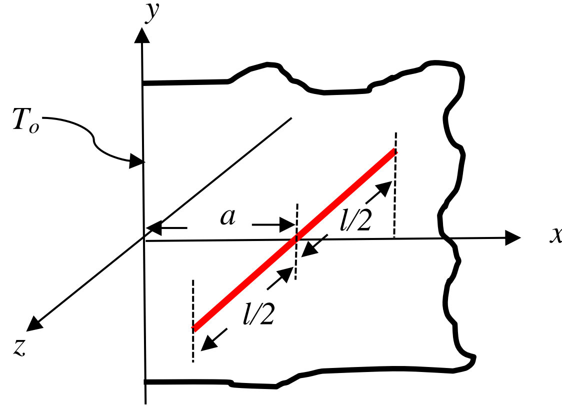


Fig. 4.2. Line heat source of finite length l in a semi-infinite solid

Consider a line heat source of finite length $l=W_g$, embedded in a semi-infinite three dimensional solid $x > 0$, $-\infty < y < \infty$ and $-\infty < z < \infty$ with temperature dependent thermal conductivity (Fig. 4.2). The heat generation per unit length of the line heat source is assumed to be constant, with the boundary condition at $x = 0$ maintained at constant temperature, T_o. Transformation of coordinates will be carried out in section 4.2.4 to transform the solution derived here to match the problem described in Fig. 4.1.

The equation governing steady heat conduction in a substrate with an internal heat generation rate of $Q(\vec{x})$ per unit volume (W/m^3) is expressed as:

$$\nabla^2 T(\vec{x}, \vec{x'}) = -\frac{Q(\vec{x})}{k(T)} \tag{4.1}$$

where $T(\vec{x}, \vec{x'})$ is the steady state temperature at any position vector $\vec{x}$ due to a point source at $\vec{x'}$ in a substrate of temperature dependent thermal conductivity $k(T)$.

The temperature dependent thermal conductivity $k(T)$ is assumed to have the general form

$$k(T) = K\left(\frac{T_{ref}}{T}\right)^{\alpha} \tag{4.2}$$

where K and α are arbitrary constants. For GaAs, $K = 51\, W/mK$, $T_{ref} = 300K$ and $\alpha = 1.23$ [34].

By use of Kirchhoff's Transformation on (4.2), let

$$\theta(T) = \int_{T_o}^{T} \frac{k(\varepsilon)}{k(T_o)} d\varepsilon = \frac{1}{k(T_o)} \int_{T_o}^{T} K\left(\frac{T_{ref}}{\varepsilon}\right)^{\alpha} d\varepsilon \tag{4.3}$$

$$\therefore \theta(T) = \frac{1}{1-\alpha} {T_o}^{\alpha}\left[T^{1-\alpha} - {T_o}^{1-\alpha}\right] \tag{4.4}$$

The inverse of (4.4) will give the actual temperature in terms of the transformed dependent variable θ:

$$T = \left[{T_o}^{1-\alpha} + \frac{1-\alpha}{{T_o}^{\alpha}}\theta\right]^{\frac{1}{1-\alpha}} \tag{4.5}$$

Utilizing (4.2) and (4.3), equation (4.1) can be expressed as:

$$\left\{\frac{\partial^2\theta}{\partial x^2} + \frac{\partial^2\theta}{\partial y^2} + \frac{\partial^2\theta}{\partial z^2}\right\} = -\frac{Q(\vec{x})}{k(T_o)} \tag{4.6}$$

$$\nabla^2\theta\left(\vec{x}, \overrightarrow{x'}\right) = -\frac{Q(\vec{x})}{k(T_o)} \tag{4.7}$$

where the source point is situated at $\overrightarrow{x'}$.

The temperature Green function $G(\vec{x}, \vec{x'})$ is defined as the temperature at field point $\vec{x}$ due to an unit heat source (W) at source point $\vec{x'}$. Therefore, $G(\vec{x}, \vec{x'})$ must satisfy the heat conduction equation in the form:

$$\nabla^2 G(\vec{x}, \vec{x'}) = -\frac{Q(\vec{x})}{k(T)} \tag{4.8}$$

The heat generation rate $Q(\vec{x})$ due to a unit strength heat source in a three-dimensional volume can be expressed as:

$$Q(\vec{x}) = \delta(\vec{x} - \vec{x'}) \tag{4.9}$$

So that:

$$\iiint_V Q(\vec{x})\, dV = 1 \tag{4.10}$$

where $\delta(\vec{x} - \vec{x'})$ is the Dirac delta function.

Substituting (4.9) into (4.8), the temperature Green's function now satisfies the heat conduction equation in the form of:

$$\nabla^2 G(\vec{x}, \vec{x'}) = -\frac{\delta(\vec{x} - \vec{x'})}{k(T)} \tag{4.11}$$

Applying Kirchhoff's transformation on (4.8),

$$U(G) = \frac{1}{1-\alpha} {G_o}^{\alpha} \left[G^{1-\alpha} - {G_o}^{1-\alpha}\right] \tag{4.12}$$

where U is the transformed dependent variable for the Green's function. Therefore,

$$\nabla^2 U(\vec{x}, \overrightarrow{x'}) = -\frac{Q(\vec{x})}{k(T_o)} \quad (4.13)$$

Substituting (4.9) into (4.13),

$$\nabla^2 U(\vec{x}, \overrightarrow{x'}) = -\frac{\delta(\vec{x} - \overrightarrow{x'})}{k(T_o)} \quad (4.14)$$

The Green second's identity is expressed as:

$$\iiint_V (\phi \nabla^2 \psi - \psi \nabla^2 \phi) dV = \iint_S \left(\phi \frac{\partial \psi}{\partial n} - \psi \frac{\partial \phi}{\partial n}\right) dS \quad (4.15)$$

Setting $\phi = U$ and $\psi = \theta$ into (4.15), where x is the observation point and x' is the integration variable,

$$\iiint_{V'} \left(U(\vec{x}, \overrightarrow{x'}) \nabla^2 \theta(\vec{x}, \overrightarrow{x'}) - \theta(\vec{x}, \overrightarrow{x'}) \nabla^2 U(\vec{x}, \overrightarrow{x'})\right) dV' = \iint_{S'} \left(U(\vec{x}, \overrightarrow{x'}) \frac{\partial \theta(\vec{x}, \overrightarrow{x'})}{\partial n'} - \theta(\vec{x}, \overrightarrow{x'}) \frac{\partial U(\vec{x}, \overrightarrow{x'})}{\partial n'}\right) dS' \quad (4.16)$$

where dV' is the volume element and n' is the outward normal on the surface element dS'.

Substituting (4.7) and (4.13) into (4.16),

$$-\iiint_{V'} U(\vec{x}, \overrightarrow{x'}) \frac{Q(\vec{x})}{k(T_o)} dV' + \iiint_V \theta(\vec{x}, \overrightarrow{x'}) \frac{\delta\left(\vec{x} - \overrightarrow{x'}\right)}{k(T_o)} dV' = \iint_{S'} \left(U(\vec{x}, \overrightarrow{x'}) \frac{\partial \theta(\vec{x}, \overrightarrow{x'})}{\partial n'} - \theta(\vec{x}, \overrightarrow{x'}) \frac{\partial U(\vec{x}, \overrightarrow{x'})}{\partial n'}\right) dS' \quad (4.17)$$

Applying the first property for Dirac delta function on the second term on the left hand side of (4.17):

$$- \iiint_{V'} U(\vec{x},\overrightarrow{x'}) \frac{Q(\vec{x})}{k(T_o)} dV' + \frac{\theta(\vec{x},\overrightarrow{x'})}{k(T_o)} = \iint_{S'} \left(U(\vec{x},\overrightarrow{x'}) \frac{\partial \theta(\vec{x},\overrightarrow{x'})}{\partial n'} - \theta(\vec{x},\overrightarrow{x'}) \frac{\partial U(\vec{x},\overrightarrow{x'})}{\partial n'} \right) dS' \quad (4.18)$$

Solving for the transformed dependent variable $\theta(\vec{x},\overrightarrow{x'})$ for temperature $T(\vec{x},\vec{x}')$:

$$\theta(\vec{x},\overrightarrow{x'}) = \iiint_{V'} U(\vec{x},\overrightarrow{x'}) Q(\vec{x}) dV' + k(T_o) \iint_{S'} \left(U(\vec{x},\overrightarrow{x'}) \frac{\partial \theta(\vec{x},\overrightarrow{x'})}{\partial n'} - \theta(\vec{x},\overrightarrow{x'}) \frac{\partial U(\vec{x},\overrightarrow{x'})}{\partial n'} \right) dS' \quad (4.19)$$

In (4.19), the prime indicates that the integration is done over the source point $\overrightarrow{x'}$. The first term on the right represents the contribution from the source while the remaining two terms represent the contributions from the boundary terms.

The objective of the formulation is to solve for the Dirichlet boundary condition where the temperature is specified on the surface. In order to solve (4.19), the Green's function, *G*, needs to be specified on the boundary before a Green's function solution can be uniquely determined.

Referring to Fig. 4.2, without any loss of generality and for convenience only, the boundary surface temperature, T_o, is assumed to be at zero Degree Celsius. Therefore, $G(\vec{x},\overrightarrow{x'}) = 0$ at the boundary and $U(\vec{x},\overrightarrow{x'}) = 0$ as calculated from (4.12), such that the first term in the surface integral (4.19) is eliminated and simplified as:

$$\theta(\vec{x},\overrightarrow{x'}) = \iiint_{V} U(\vec{x},\overrightarrow{x'}) Q(\vec{x}) dV' - k(T_o) \iint_{S'} \theta(\vec{x},\overrightarrow{x'}) \frac{\partial U(\vec{x},\overrightarrow{x'})}{\partial n'} dS' \quad (4.20)$$

From (4.4), $\theta(T_o) = 0$ as the boundary temperature $T_o = 0$. Therefore, (4.20) can be further simplified as:

$$\theta(\vec{x}, \overrightarrow{x'}) = \iiint_V U(\vec{x}, \overrightarrow{x'}) Q(\vec{x}) dV' \quad (4.21)$$

It is noted that once the transformed dependent variable for the Green's function U in (4.21) is determined, the temperature distribution due to a finite line heat source with temperature dependent thermal conductivity can be easily calculated.

4.2.3. Green's Function Solution for a Three-Dimensional Semi-inifinite Solid

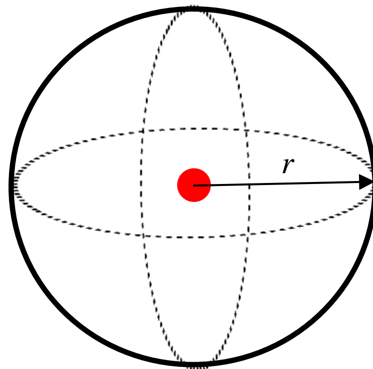


Fig. 4.3. A sphere of radius, *r,* with internal heat generation

In order to solve (4.21), a unique Green's function solution needs to be determined first. Consider a sphere of radius *r* with constant heat generation per unit volume Q (W/m^3) inside the sphere for a three-dimensional case (Fig. 4.3), the total heat generation Q_T inside the sphere is expressed as:

$$Q_T = \frac{4}{3}\pi r^3 Q \quad (4.22)$$

The heat flux, q_r, at the boundary of the sphere is related to the total heat generated Q_T by:

$$q_r(4\pi r^2) = Q_T \tag{4.23}$$

Using Kirchhoff Transformation on (4.23),

$$\frac{d\theta}{dr} = \frac{k(T)}{k(T_o)}\frac{dT}{dr} \implies \frac{dT}{dr} = \frac{k(T_o)}{k(T)}\frac{d\theta}{dr} \tag{4.24}$$

Recall that Fourier's law is expressed as:

$$q_r = -k(T)\frac{dT(r)}{dr} \tag{4.25}$$

where $T(r)$ is the temperature profile as a function of radial distance r.

Substituting (4.25) into (4.23),

$$\frac{dT(r)}{dr} = \frac{-1}{k(T)}\frac{Q_T}{4\pi r^2} \tag{4.26}$$

Substituting (4.26) into (4.24),

$$\begin{gathered} \frac{Q_T}{4\pi r^2} = -k(T_o)\frac{d\theta}{dr} \\ \theta(r) = \frac{Q_T}{4\pi k(T_o) r} \end{gathered} \tag{4.27}$$

where $\theta(r)$ is the transformed dependent variable of temperature profile $T(r)$ as a function of radial distance r.

For an unit strength point heat source, substitute $Q_T = 1$ into (4.27),

$$\nabla^2\theta = \frac{1}{4\pi k(T_o)}\nabla^2\left(\frac{1}{r}\right) \tag{4.28}$$

Now, consider a unit strength point heat source placed in an infinite space with temperature dependent thermal conductivity. To achieve the boundary

condition $T_o = 0$ at $x = 0$ (Fig. 4.2), the method of images is carried out at $x = 0$ as shown in Fig. 4.4.

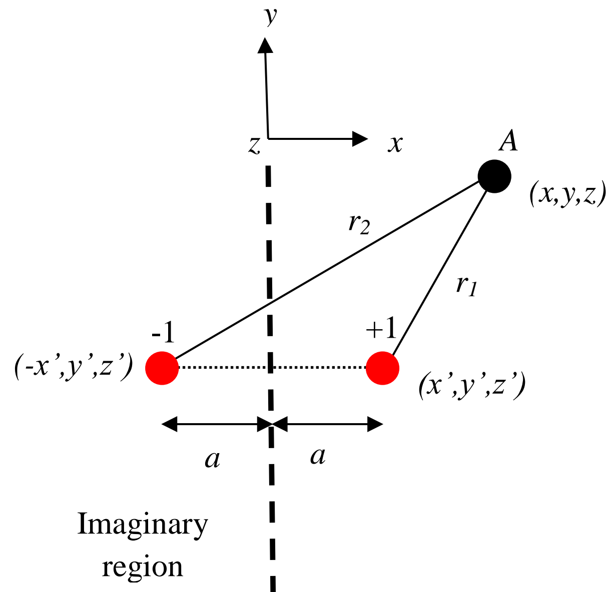


Fig. 4.4. Image for a unit point heat source along $x=0$ in a three dimensional space

In Fig. 4.4, the point heat source (+1) is reflected along $x = 0$ to get a sink source (-1) in the imaginary region. The temperature contribution towards point A due to the reflected sink source (-1) will be equal to the source (+1) but with opposite sign. Therefore, the temperature distribution at point A in a semi-infinite space with temperature dependent thermal conductivity can be expressed in terms of the transformed dependent variable θ as:

$$\theta = \frac{1}{4\pi k(\mathrm{T_o})}\left[\frac{1}{r_1} - \frac{1}{r_2}\right]$$
$$\nabla^2\theta = \frac{1}{4\pi k(\mathrm{T_o})}\left[\nabla^2\frac{1}{r_1} - \nabla^2\frac{1}{r_2}\right] \tag{4.29}$$

where r_1 is the distance between the point A and the point heat source, while r_2 is the distance between the point A and the sink source in the imaginary region. r_1 and r_2 are expressed as:

$$r_1 = \sqrt{(x - x')^2 + (y - y')^2 + (z - z')^2}$$

$$r_2 = \sqrt{(x + x')^2 + (y - y')^2 + (z - z')^2} \tag{4.30}$$

Since the transformed dependent variable U for the Green's function satisfies (4.7) in the form of (4.13) and (4.12) for a unit strength heat source, the general equation for U can also be expressed as:

$$U = \frac{1}{4\pi k(T_o)}\left[\frac{1}{r_1} - \frac{1}{r_2}\right]$$

$$\nabla^2 U = \frac{1}{4\pi k(\mathrm{T_o})}\left[\nabla^2 \frac{1}{r_1} - \nabla^2 \frac{1}{r_2}\right] \tag{4.31}$$

Substituting (4.31) into (4.21), $\theta\left(\vec{x}, \overrightarrow{x'}\right)$ can be solved:

$$\theta\left(\vec{x}, \overrightarrow{x'}\right) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\int_{0}^{\infty} \frac{1}{4\pi k(T_o)}\left[\frac{1}{r_1} - \frac{1}{r_2}\right] Q(\vec{x})\, dx'dy'dz' \tag{4.32}$$

where $H\left[z' - \frac{l}{2}\right]$ and $H\left[z' + \frac{l}{2}\right]$ are the Heaviside step function, $Q\left(\overrightarrow{x'}\right) = \lambda\delta(x' - a)\delta(y')\left\{H\left[z' + \frac{l}{2}\right] - H\left[z' - \frac{l}{2}\right]\right\}$ for a finite line heat source of length l at distance a from the boundary and heat dissipation λ per unit length (W/m) as shown in Fig. 4.2.

Therefore,

$$\theta(\vec{x},\overrightarrow{x'}) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\int_{0}^{\infty} \frac{1}{4\pi k(T_o)}\left[\frac{1}{r_1} - \frac{1}{r_2}\right] \lambda\delta(x'-a)\delta(y')\left\{H\left[z' + \frac{l}{2}\right] - H\left[z' - \frac{l}{2}\right]\right\} dx'dy'dz' \tag{4.33}$$

From the properties of the Dirac delta function:

$$\int_{-\infty}^{\infty} \delta(x-a)dx = \int_{\gamma_1}^{\gamma_2} \delta(x-a)dx = 1 \tag{4.34}$$

where $\gamma_1 < a < \gamma_2$.

The Heaviside step function is defined as:

$$H(x-a) = \begin{Bmatrix} 0 & \text{if } x < a \\ 1 & \text{if } x > a \end{Bmatrix} \tag{4.35}$$

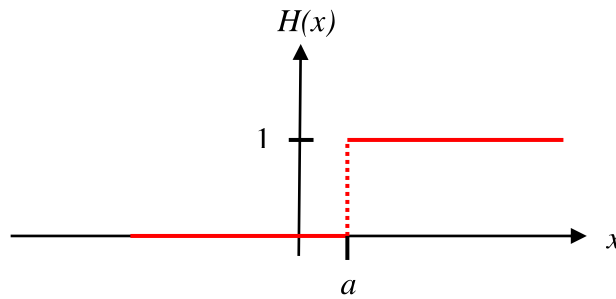


Fig. 4.5. Heaviside step function

The property that relates the Heaviside step function to the Dirac Delta function is:

$$\frac{dH(x)}{dx} = \delta(x) \tag{4.36}$$

Applying the properties of Dirac Delta function and Heavside step function (4.34) to (4.36):

$$\int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\int_{0}^{\infty} \lambda\delta(x'-a)\delta(y')\left\{H\left[z'+\frac{l}{2}\right]-H\left[z'-\frac{l}{2}\right]\right\} dx'dy'dz' \tag{4.37}$$

$$= \lambda\int_{-l/2}^{l/2} dz' \int_{-\infty}^{\infty}\delta(y')dy' \int_{0}^{\infty}\delta(x'-a)dx' = \lambda l$$

Therefore, (4.33) can be reduced to:

$$\theta(\vec{x},\overrightarrow{x'}) = \frac{\lambda}{4\pi k(T_o)}\int_{-\frac{l}{2}}^{\frac{l}{2}}\left[\frac{1}{r_1}-\frac{1}{r_2}\right]dz' \tag{4.38}$$

Substituting (4.30) into (4.38),

$$\theta(\vec{x},\overrightarrow{x'}) = \frac{\lambda}{4\pi k(T_o)}\int_{-\frac{l}{2}}^{\frac{l}{2}}\left[\frac{1}{\sqrt{(x-x')^2+(y-y')^2+(z-z')^2}}-\frac{1}{\sqrt{(x+x')^2+(y-y')^2+(z-z')^2}}\right]dz' \tag{4.39}$$

$$\theta(\vec{x},\overrightarrow{x'}) = \frac{\lambda}{4\pi k(T_o)} ln\left\{\frac{\left[(z+0.5l)+\sqrt{(x-a)^2+y^2+(z+0.5l)^2}\right]}{\left[(z-0.5l)+\sqrt{(x-a)^2+y^2+(z-0.5l)^2}\right]}\cdot \frac{\left[(z-0.5l)+\sqrt{(x+a)^2+y^2+(z-0.5l)^2}\right]}{\left[(z+0.5l)+\sqrt{(x+a)^2+y^2+(z+0.5l)^2}\right]}\right\} \tag{4.40}$$

Substituting (4.40) into (4.5), the three-dimensional temperature distribution due to a finite line heat source embedded in a semi-infinite solid can be calculated as:

$$T_1 = \left[T_o^{1-\alpha} + \frac{(1-\alpha)}{T_o^{\alpha}} \frac{\lambda}{4\pi k(T_o)} ln \left\{ \frac{\left[(z+0.5l)+\sqrt{(x-a)^2+y^2+(z+0.5l)^2}\right]}{\left[(z-0.5l)+\sqrt{(x-a)^2+y^2+(z-0.5l)^2}\right]} \cdot \frac{\left[(z-0.5l)+\sqrt{(x+a)^2+y^2+(z-0.5l)^2}\right]}{\left[(z+0.5l)+\sqrt{(x+a)^2+y^2+(z+0.5l)^2}\right]} \right\} \right]^{\frac{1}{1-\alpha}} \quad (4.41)$$

4.2.4. Transformation of Coordinates and Method of Images

To relate the derived solution (4.41) with the problem described in Fig. 4.1, the method of images is applied at *z=0* with respect to the coordinate system in Fig. 4.1 by transformation of coordinates, so that the temperature distribution in Fig. 4.1 can be calculated by (4.42). Such an approach has been well established in [62, 63].

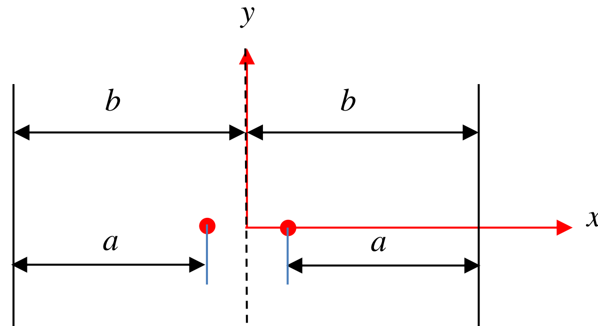


Fig. 4.6. Image of finite length (W_g) heat source along *z=0* to obtain adiabatic boundary condition at the top surface

$$T(x,y,z) = T_1(b+x, y-d, z) + T_1(b-x, y-d, z) - T_o \quad (4.42)$$

where

$$T_1(b+z,x-d,y) = \left[T_o{}^{1-\alpha} + \frac{(1-\alpha)}{T_o{}^{\alpha}} \frac{\lambda}{4\pi\bar{\mathrm{k}}(\mathrm{T_o})} \ln \left\{ \frac{\left[(y+0.5)+\sqrt{(b+z-a)^2+(x-d)^2+(y+0.5)^2}\right]}{\left[(y-0.5)+\sqrt{(b+z-a)^2+(x-d)^2+(y-0.5)^2}\right]} \cdot \frac{\left[(y-0.5)+\sqrt{(b+z+a)^2+(x-d)^2+(y-0.5)^2}\right]}{\left[(y+0.5)+\sqrt{(b+z+a)^2+(x-d)^2+(y+0.5)^2}\right]} \right\} \right]^{\frac{1}{1-\alpha}} \quad (4.43)$$

$$T_1(b-z,x-d,y) = \left[T_o{}^{1-\alpha} + \frac{(1-\alpha)}{T_o{}^{\alpha}} \frac{\lambda}{4\pi\bar{\mathrm{k}}(\mathrm{T_o})} \ln \left\{ \frac{\left[(y+0.5)+\sqrt{(b-z-a)^2+(x-d)^2+(y+0.5)^2}\right]}{\left[(y-0.5)+\sqrt{(b-z-a)^2+(x-d)^2+(y-0.5)^2}\right]} \cdot \frac{\left[(y-0.5)+\sqrt{(b-z+a)^2+(x-d)^2+(y-0.5)^2}\right]}{\left[(y+0.5)+\sqrt{(b-z+a)^2+(x-d)^2+(y+0.5)^2}\right]} \right\} \right]^{\frac{1}{1-\alpha}} \quad (4.44)$$

The peak operating junction temperature can be determined by using (4.42) once the temperature at the base (T_o) of the substrate is known. Although this temperature distribution is derived for a single line heat source, it can also be used for calculating temperature distributions due to *n* multiple line heat sources embedded in the substrate by using superposition techniques.

4.3. Comparatives Studies with Various Analytical Solutions and FEA

This section aims to compare the present analytical solution with those of other analytical methods and FEA. The problem to be used for this comparison is a one-gate MMIC chip where the length of the gate is L_g = 0.25µm and it width W_g = 100µm. The substrate dimensions are 2.235 x 2.235

x 0.1 mm^3. The surfaces are all assumed to be adiabatic except for the bottom of the substrate which is assumed to be at 25°C.

- Total heat generation, Q = 1 W, T_o = 25°C.
- L_g = 0.25 μm, W_g = 250 μm, b = 100μm.
- k = 52 W/mK for [45] or $k(T) = 51(300/T)^{\alpha}$ W/mK.

4.3.1. Comparison with Selected Past Analytical Methods

i. Ditri [34] had derived an analytical solution for calculating the temperature distribution in a microwave chip that incorporated the effects of both orthotropic values of thermal conductivity and temperature-dependent thermal conductivity. He had assumed a surface heat flux as the heat dissipation region (Fig. 4.7). The sides and the top surfaces of the substrate are assumed to be adiabatic while the bottom is an isothermal surface at constant temperature, T_o. By making use of Kirchhoff Transformation, Ditri obtained an analytical solution for the temperature solution as:

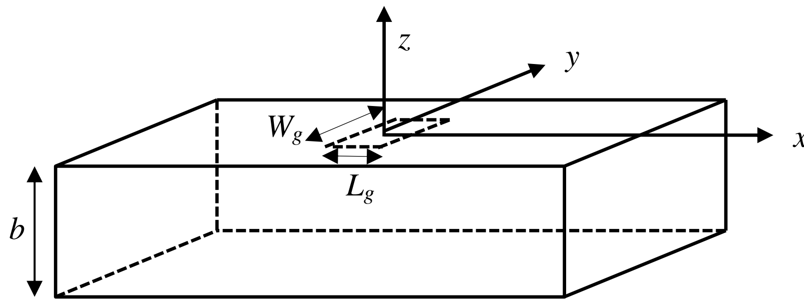


Fig. 4.7. Rectangular surface heat flux on the top surface of the substrate

$$T(x,y,z) = \left[{T_o}^{1-\alpha} + \frac{(1-\alpha)}{{T_o}^{\alpha}}\sum_{n=0}^{\infty}\sum_{m=0}^{\infty}\Theta_{mn} \times \sinh\left(\frac{\beta_{mn}z}{\sqrt{\kappa_{zz}}}\right)\cos\left(\frac{n\pi x}{a}\right)\cos\left(\frac{m\pi y}{b}\right)\right]^{\frac{1}{1-\alpha}} \quad (4.45)$$

where

$$\beta_{mn} = \sqrt{\kappa_{xx}\left(\frac{n\pi}{a}\right)^2 + \kappa_{yy}\left(\frac{m\pi}{b}\right)^2} \tag{4.46}$$

$$\Theta_{mn} = \frac{4\gamma_{mn}h}{\sqrt{\kappa_{zz}}k_o\pi^2\beta_{mn}\cosh\left(\frac{\beta_{mn}c}{\sqrt{\kappa_{zz}}}\right)nm}\cos\left(\frac{n\pi x_o}{a}\right)\sin\left(\frac{n\pi L_x}{2a}\right)\cos\left(\frac{m\pi y_o}{b}\right)\sin\left(\frac{m\pi L_y}{2b}\right) \tag{4.47}$$

$$\gamma_{mn} = \frac{4}{(1+\delta_{n0})(1+\delta_{m0})} \tag{4.48}$$

and δ_{n0} represents the Kronecker delta, which equals 1 if $m = n$ and 0 otherwise.

Ditri's work was chosen for comparison with the present analytical method as his solution is similar to that of previous analytical methods and is the most recent work where the solution consists of summations of double infinite series. It should be noted that in the problem that Ditri solved, the heat source was a planar heat source at the surface. Hence, in order to compare with Ditri's solution, a surface line heat source is used in the present analytical solution instead of the more usual embedded one.

ii. Darwish et al. [45] had expressed the temperature distribution around the gate in terms of the difference in the thermal resistance at different depth from the base of the substrate of constant thermal conductivity. The thermal resistance is derived by considering a cylinder between two infinite planes. The isotherms around the gate were assumed to be cylindrical (Fig. 2.4). The thermal resistance and the temperature profile

due to a constant highly localized heat source on a substrate of thickness *t* are calculated using (4.49) and (4.50), respectively.

$$\theta = \frac{1}{\pi W_g k} \ln\left(\frac{8t}{\pi L_g}\right) \quad (4.49)$$

$$T(z) = \theta_t - \theta_z = \frac{1}{\pi W_g k} \ln\left(\frac{t}{z}\right) \quad (4.50)$$

For an FET with multiple heat sources, Darwish et al. has taken into account the interaction of heat sources and presented a closed-form expression for calculating the junction temperature [46]:

$$T_j = [T_o^{-0.23} - 0.23(\theta_{total}^s P) T_o^{-1.23}]^{-\frac{1}{0.23}} \quad (4.51)$$

where T_j is the junction temperature, T_o is the base plate temperature in degree Kelvin, *P* is the power input per gate and θ_{total}^s is expressed as:

$$\theta_{total}^s = \frac{1}{\pi W_g k(T_o)} \ln\left(\frac{V[f(g[\sqrt{2}s] + 1)]}{V[f(g[L_g])]}\right) + \frac{1}{2\pi s k(T_o)} \ln\left(\frac{h(2.3t)}{h(s)}\right) \quad (4.52)$$

where

$$h(x) = \frac{\sqrt{1 + g(\sqrt{2}x)} + 1}{\sqrt{1 + g(\sqrt{2}x)} - 1}$$
$$V(z) = \frac{z - 1}{z + 1} \quad (4.53)$$
$$f(w) = \sqrt{\frac{\sqrt{w} + 1}{\sqrt{w} - 1}}$$
$$g(y) = \left(\frac{W_g}{y}\right)^2$$

Darwish et al. work was chosen for comparison with the present analytical method as it is a closed-form solution with a fixed surface heat source. The

present analytical can be used to compare with Darwish et al. work by using a surface line heat source instead of an embedded one.

4.3.2. Finite Element Analysis (FEA)

For the FEA, a substrate with a volumetric heat source (L_g x W_g x $0.28\mu m$) is modelled to compare with the analytical solutions (Fig. 4.8). As the actual heat dissipation occurs in a region below the gate, the volumetric heat source is modelled to be at a depth of 0.28μm below the surface of the substrate. Temperature dependency of the thermal conductivity k of the substrate is taken into account.

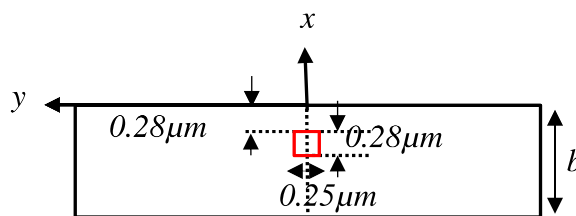


Fig. 4.8. Volumetric heat source (L_g x W_g x $0.28\mu m$) embedded in a substrate

4.3.3. Present Analytical Method

The present analytical method has been used to calculate the temperature distribution for both the surface and the embedded line heat source as illustrated in Fig. 4.9. The depth of the embedded line heat source is obtained by considering the distance of the center of the volumetric heat source from the top surface of the substrate shown in Fig. 4.8, i.e. (0.28 + 0.28/2) μm = 0.42 μm.

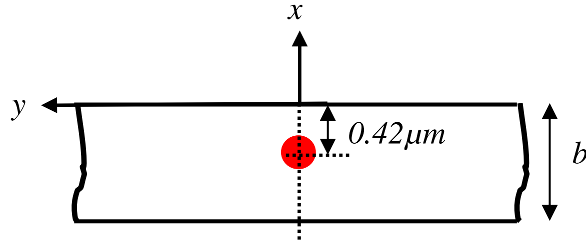


Fig. 4.9. Finite line heat source (W_g) embedded in the substrate

4.4. Comparison of Results

4.4.1. Distinction between junction temperature, T_j, and gate temperature, T_g

In this and other analytical methods where the heat sources are assumed to be embedded in the substrate under the gate, the location of the maximum junction temperature, T_j, of the MMIC device is found in the heat dissipation region that occurs in the depleted region under the gate. This junction temperature is different from and higher than the gate temperature, T_g, which refers to the temperature of the gate on the surface. For analytical models which assumed a planar heat source at the surface of the substrate where the gate is located, it will be found that the maximum junction temperature is located at the centre of the planar heat source and hence the same as the gate temperature.

In Fig. 4.10, the calculated T_j and T_g using FEA with embedded heat source, and calculated $T_{j,surface}$ using FEA with a surface planar heat source are plotted. The calculated T_j and T_g obtained using the present analytical method are also plotted in Fig. 4.10 for comparison. From the FEA results, the difference between calculated T_j and T_g increases as the power increases. At 2

W/mm and 4 W/mm, the differences between T_j and T_g are 3.07°C and 27.8°C, respectively. When a surface planar heat source is modelled, the calculated $T_{j,surface}$ differs greatly from T_j and T_g , confirming that modelling of heat dissipation using a planar heat source will lead to huge overestimation of junction temperatures.

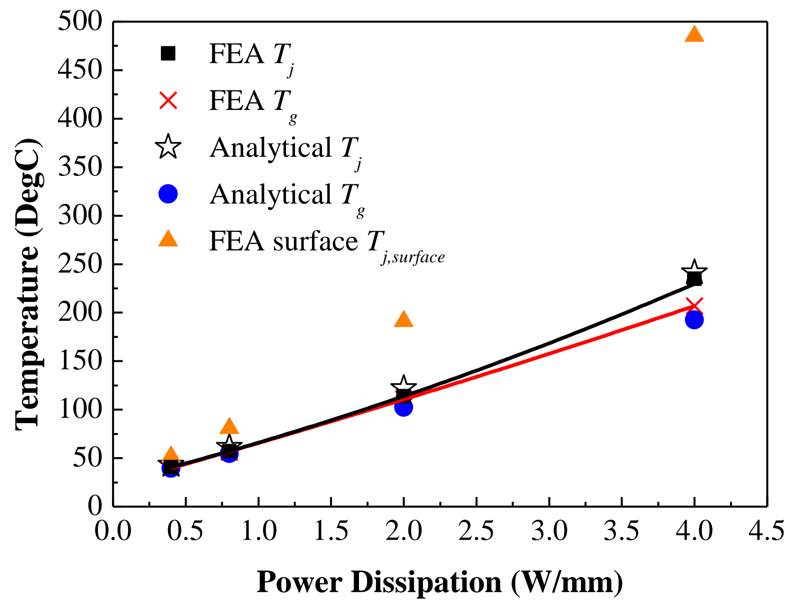


Fig. 4.10. Comparison of junction temperatures T_j and gate temperatures T_g calculated using FEA and the present analytical method

4.4.2. Comparison of Present Analytical Method with Previous Works and FEA

In this section, the calculated temperature distributions using various analytical methods and FEA based on the following listed parameters are compared. FEA results will be used as the baseline for comparison as it is more close to the actual problem. The actual temperature dependent thermal conductivity and the geometry of the heat source can be accounted for accurately without any simplification.

The temperature distribution on the surface of the substrate obtained from the various methods is plotted and compared in Fig. 4.11:

From this comparison, it is observed that:

- The present work (embedded heat source) produces results that agree much better (within 10%) with the FEA results as compared to previous works. Since the FEA results are considered the most accurate, this shows that the present method is more accurate than all the previous works studied.
- The large differences between the present work (embedded and surface heat source) and Darwish et. al. [45] reflect the importance of the effect of temperature-dependent thermal conductivity on the junction temperature and the temperature distribution around the gate.
- The location of the heat source is also an important parameter for predicting the gate temperature. The Fourier series solution [34] with a surface planar heat source leads to an overestimation of the gate temperature compared to the FEA. A similar result was obtained using the

present method when a surface line heat source was assumed. Therefore, it is important to model the heat source at the appropriate location in order to predict the gate and junction temperatures accurately.

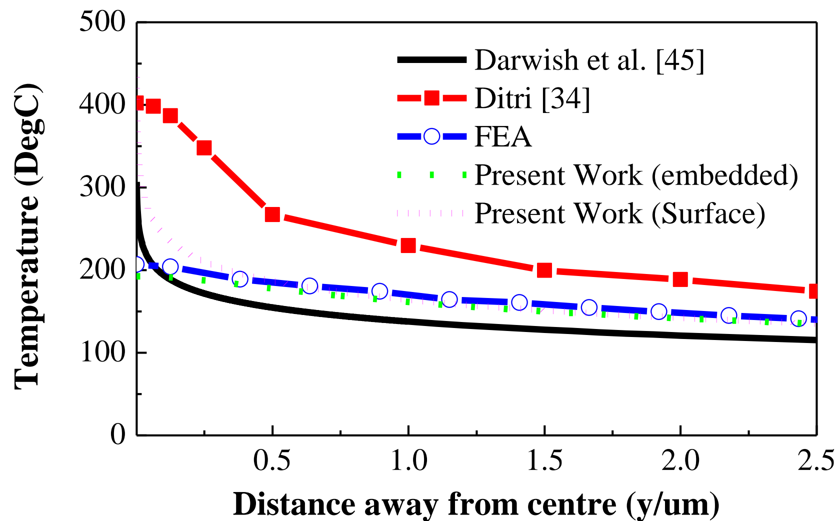


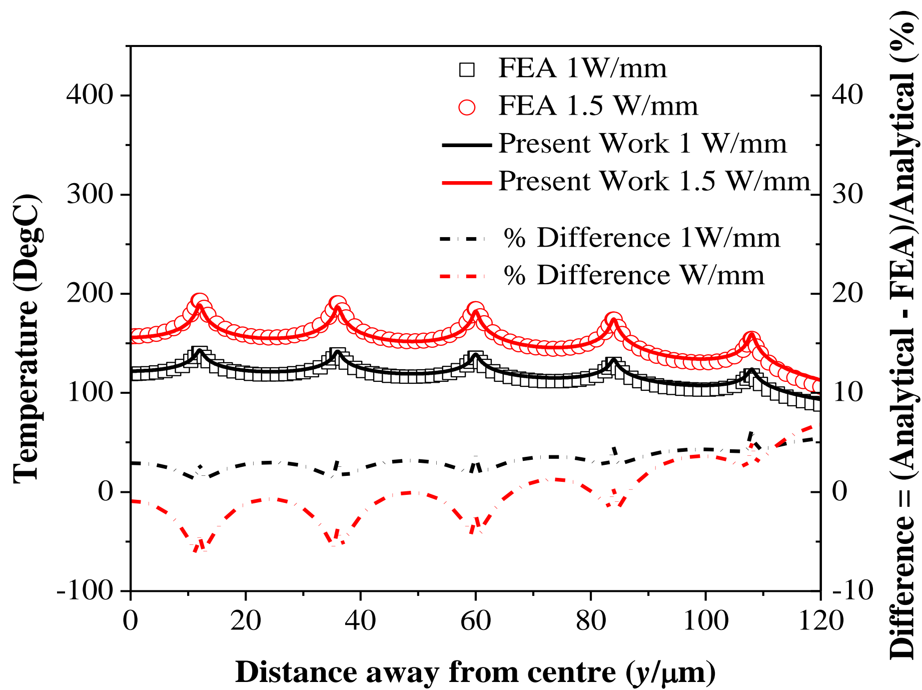
Fig. 4.11. Comparison of substrate surface temperature distribution calculated using the present work with Ditri [34], Darwish [45] and FEA results

The present method can also be applied to multiple heat sources by employing superposition technique. Below is a comparison of the results obtained for a 10-gate device using the present method and the FEA.

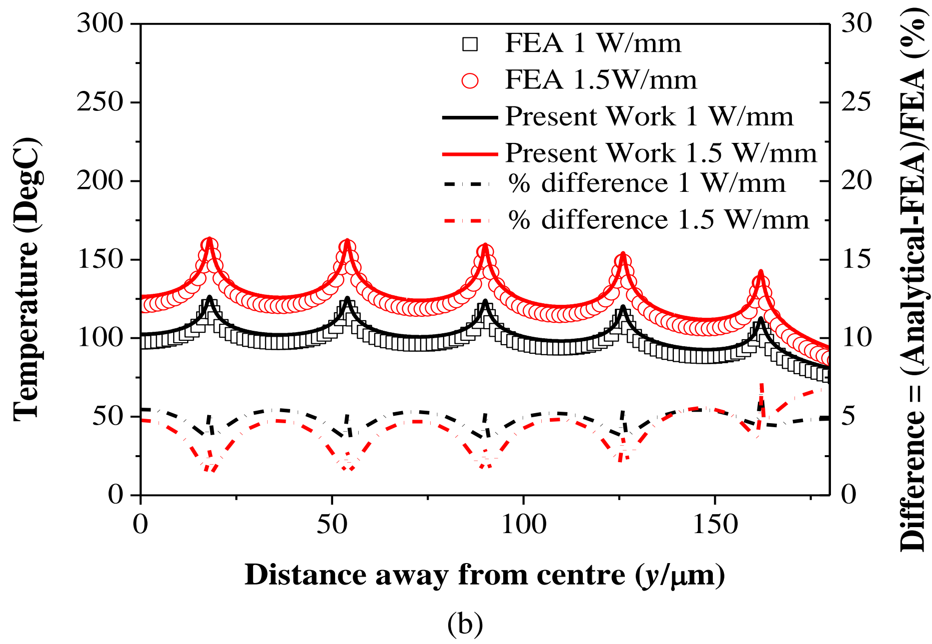
Consider the following parameters:

- gate pitch = 24 µm or 36 µm
- W_g = 150 µm, L_g = 0.25 µm, b = 100µm
- Number of gates = 10
- b = 100µm
- $T_o = 55^{o}$C
- power input = 1W/mm and 1.5W/mm

The temperature distributions on the surface of the substrate due to the ten gates are plotted in Fig. 4.12. Only half of the temperature distribution is plotted since there is symmetry along the *y*-axis. The temperature peaks are expected at location of the heat dissipation region under the gates. As can be seen, the excellent agreement between the FEA and the present work for different gate pitch of 24 µm and 36 µm shows that the present analytical method yields accurate temperature distributions for multiple heat sources using the present analytical method and the superposition technique. Furthermore, it also verifies that it is accurate to use a line heat source to represent the volumetric heat source present in FETs or MMICs since the gate length is very small compared to the gate width.



(a)



(b)

Fig. 4.12. Comparison between present work and FEA at power input of 1W/mm and 1.5W/mm with T_o =55°C for gate pitch of (a) 24µm and (b) 36µm

4.5. Comparison of Present Work with Experimental Measurements

In this section, the gate temperature calculated using the present analytical method will be compared with Darwish et. al. [46] and experimental results measured using liquid-crystal thermography (LCT) [9] and photoluminescence spectroscopy [60].

Example 1:

For the GaAs MESFET power amplifier with 80 gates, the substrate base temperature was at 125°C.

- Measured gate temperature = 228°C.
- Using [46], the calculated gate temperature = 226°C.
- Using the present work, the calculated gate temperature = 223°C.

From this comparison, close agreement is observed. This shows that the present work is able to predict the gate temperature with good accuracy.

Example 2:

For the GaAs "dense array" amplifier with 10 gates, the substrate base temperature was at 130°C.

- Measured gate temperature = 172°C.
- Using [46], the calculated gate temperature = 184°C.
- Using the present work, the calculated gate temperature = 178°C.

From this comparison, close agreement between the measured temperature and the predicted temperature from the present work is again observed. The agreement with the present work is also better than with [46]. This could be due to the assumptions made in [46], i.e. the thermal model assumes an infinite number of gates to the right and left hand side to achieve adiabatic surfaces between each gate. On the other hand, the present work is not limited by this assumption and is able to take into account the actual number of gates.

Example 3:

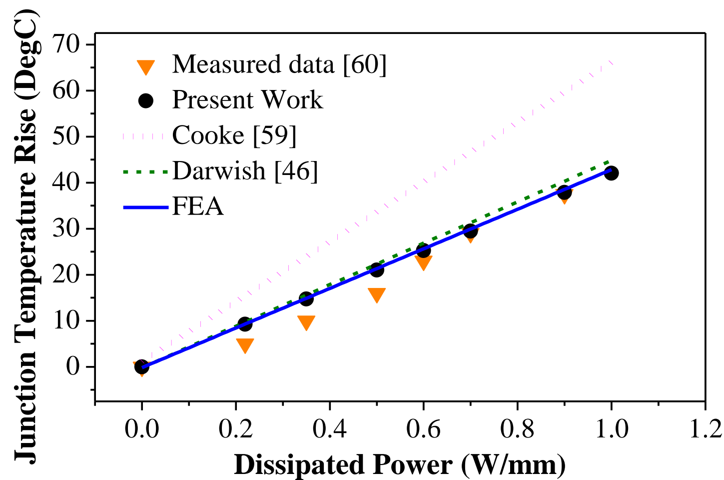


Fig. 4.13. Comparison between calculated and measured junction temperature rise for the 4x50µm, 0.25µm gate length GaAs pHEMT device

Photoluminescence spectroscopy [60] was used to measure the gate temperature rise of a 4x50µm, 0.25µm gate length GaAs pHEMT device. The gate temperature rise calculated using the present analytical method is plotted in Fig. 4.13 and compared with measured temperatures, Darwish [46], Cooke [59] and FEA results. Close agreement between the present work with measured temperatures and the FEA can be observed in Fig. 4.13.

4.6. Discussion on Convergence Rate of Solution

From the above derivation of the analytical solution, it is noted that the effect of adiabatic boundary conditions at the lateral faces is ignored, thereby yielding a closed-form analytical solution. The adiabatic boundary condition can be taken into account easily by carrying out method of images as shown in Fig. 4.14. Theoretically, an infinite number of images are required, at increasing distances from both sides of the symmetry plane and therefore with

diminishing contribution, producing a converging series. This is necessary when the heat sources are located near to the lateral faces. However, this is not needed for our case since heat sources are assumed to be located in a substrate with large width, L_b. If needed, however, it is sufficient to just include one row of image sources to achieve reasonable accuracy as shown in Fig. 4.14. It can be seen from Fig. 4.15, that the percentage difference in the calculated temperature profile, at power dissipations of 1W/mm and 1.5W/mm and gate pitches of 24 µm and 36 µm, with and without one row of image sources is less than 1%.

To illustrate further, the effects of increasing the number of row of images on the converging rate of the maximum gate temperature calculated for gate pitches of 24 µm and 36 µm are shown in Fig. 4.16(a) and Fig. 4.16(b), respectively. An increase of 0.06°C on the maximum gate temperature was observed for both gate pitches when 50 rows of images were included. This justifies the truncation of the first term, i.e. ignoring the adiabatic boundary condition at lateral faces, and therefore resulting in a closed-form analytical solution.

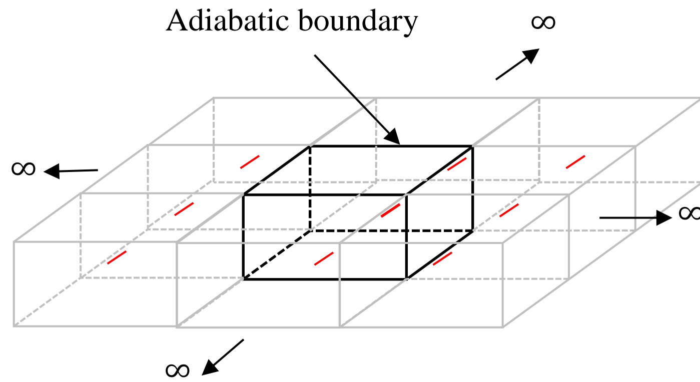
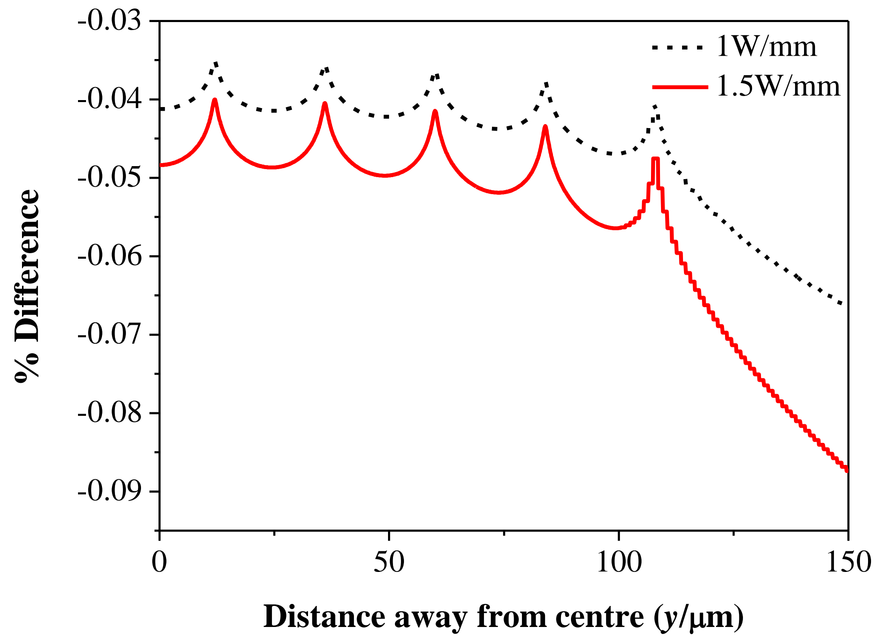
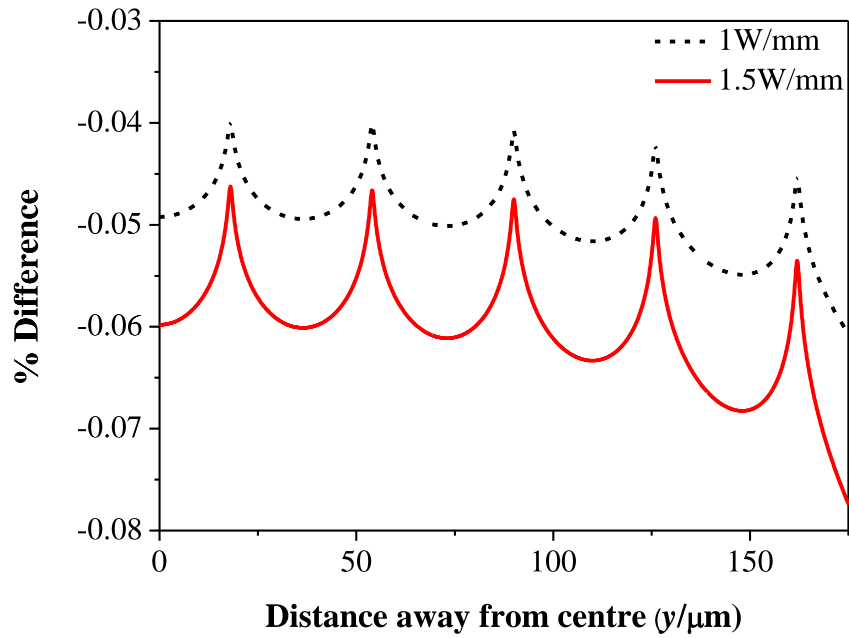


Fig. 4.14. Adiabatic boundary conditions at the lateral faces can be imposed by applying the method of images in both directions. Only one row of images (grey) is shown in this figure

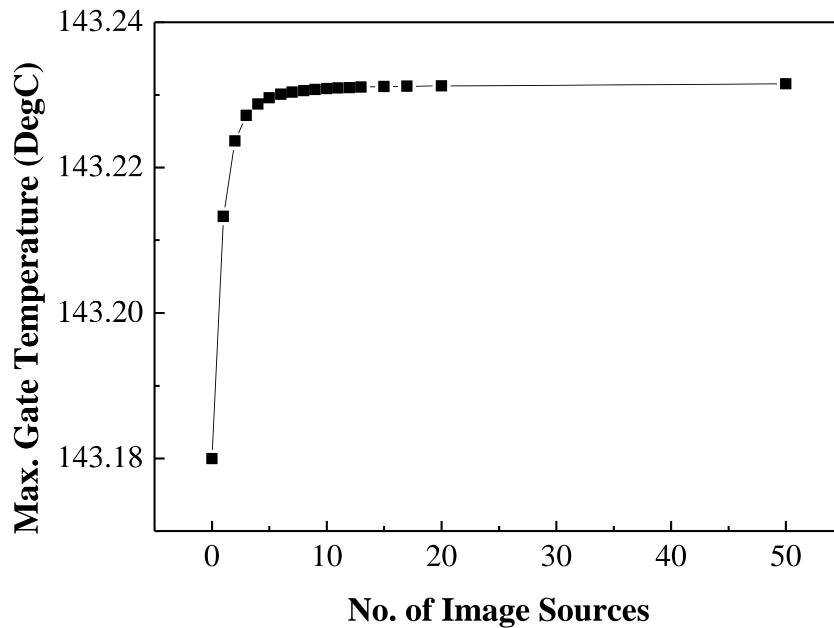


(a)

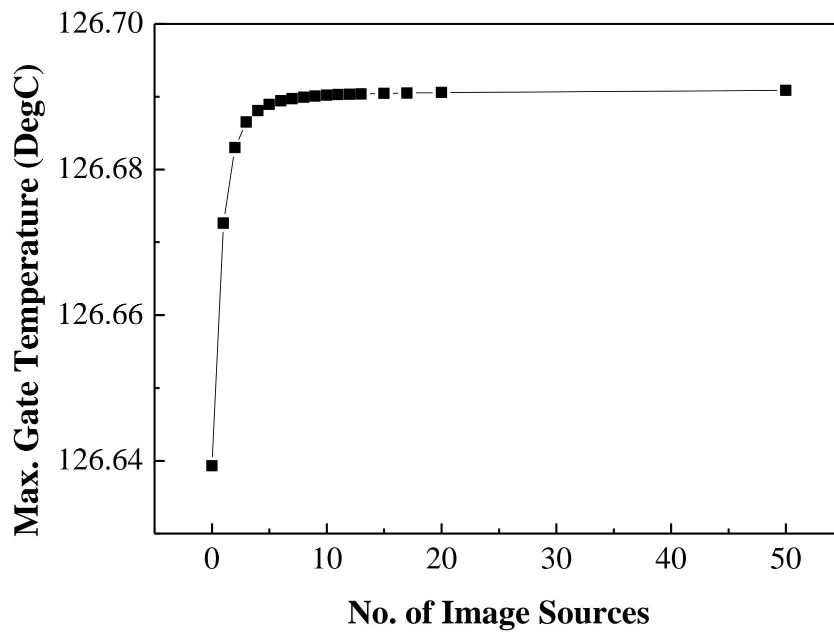


(b)

Fig. 4.15. Percentage difference in the calculated temperature profile at power dissipation of 1W/mm and 1.5W/mm with and without one row of image sources at lateral face for gate pitch of (a) 24µm and (b) 36 µm



(a)



(b)

Fig. 4.16. Converging rate for the maximum gate temperature for gate pitch of (a) 24 μm and (b) 36 μm at power dissipation of 1W/mm

4.7. Conclusion

An accurate closed-form analytical solution for predicting the temperature field in the integrated circuits due to embedded heat sources has been presented. It is based on the Green's function integral method on a point heat source developed through the method of images. Comparisons between temperatures calculated using the present analytical method, past analytical methods and FEA has shown that the present analytical method is more accurate than the previous analytical methods. Comparison with temperatures measured using liquid-crystal thermography and photoluminescence spectroscopy further confirms that the present analytical method produces results that are accurate.

Compared to previous works, the present analytical method is easier to implement and reduces the computation time significantly. In addition, the exact location of the heat dissipation region can be easily taken into account for accurate estimation of the junction temperature. The effect of the temperature dependent thermal conductivity, location of the heat source and the gate geometry on the temperature distribution around the junction can be easily investigated by simply modifying the parameter values. Although a numerical approach will provide a more accurate prediction of the peak operating junction temperature if the actual geometric details of surface features such as metal layers and air bridges are modelled, it can be time consuming and computationally expensive to investigate the effect of the design parameters on the peak junction temperature in the early design stages. Furthermore, it has been shown that the present analytical method is applicable for multi-finger devices by employing superposition techniques and has been shown to agree well with FEA results.

CHAPTER 5

A NEW ANALYTICAL METHOD FOR CALCULATING JUNCTION TEMPERATURE OF PACKAGED DEVICES INCORPORATING THE TEMPERATURE DISTRIBUTION AT THE BASE OF THE SUBSTRATE

5.1. Problem Statement

Many analytical solutions have been developed to solve for the temperature distribution in FETs. These analytical methods are based on the Fourier series solution [32-34, 61], Fourier transformation techniques [35], Green's function method [41-43] and the thermal resistance method [46, 51, 52]. Although analytical methods are limited to simple geometries and boundary conditions, they provide straightforward relations between the design parameters and the peak junction temperature. In addition, it provides a quick estimation of the peak operating junction temperature which is very useful during the initial design stage.

Currently, all analytical methods for calculating the junction temperature of an MMIC device have assumed a constant uniform temperature at the base of the substrate. In a packaged device, however, where the substrate is attached to a carrier, thermal finite element analysis (FEA) has shown that the temperature distribution along the base of the substrate is not uniform but has a bell-shaped distribution with a maximum directly below the location of the heat source. Consequently, the current analytical methods which assume a constant uniform temperature at the base of the substrate have been found to be inaccurate. Although a few spreading resistance techniques exist [49, 50]

which can be used to predict the temperature distribution at the base of the substrate, the results are not so accurate.

In the following section, a novel analytical method will be developed to determine an accurate temperature distribution at the base of the substrate in a packaged device. This method, together with the new closed-form analytical solution developed in Chapter 4 for the temperature distribution within the substrate, will allow the peak operating junction temperature to be determined easily and accurately using the analytical approach. The accuracy of the calculated base temperatures will be compared with the finite element results. In addition, the peak operating junction temperature determined using the calculated maximum base temperature and the new closed-form solution in Chapter 4, will also be compared with those measured using thermoreflectance thermography and those calculated using FEA, as well as reported numerical results in [31].

After establishing the accuracy of this novel method, it will be further establish to be applicable to the typical range of substrate thickness, i.e. 100 μm to 300 μm [64, 65]. A general formulation for the maximum substrate base temperature as a function of substrate thickness, gate length, gate pitch and total number of gates will be derived. The peak operating junction temperature calculated using the calculated maximum substrate base temperature in conjunction with the new closed-form solution in Chapter 4 will be compared with that calculated using FEA.

5.2. Determination of the Temperature T_o at the Base of the Substrate

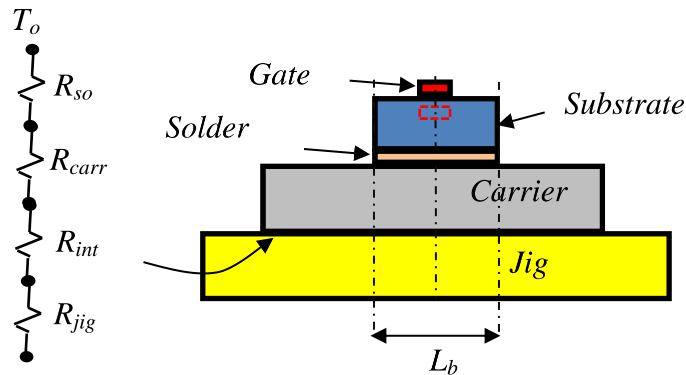


Fig. 5.1. Schematic cross-section of a PA MMIC package and the equivalent thermal resistance network

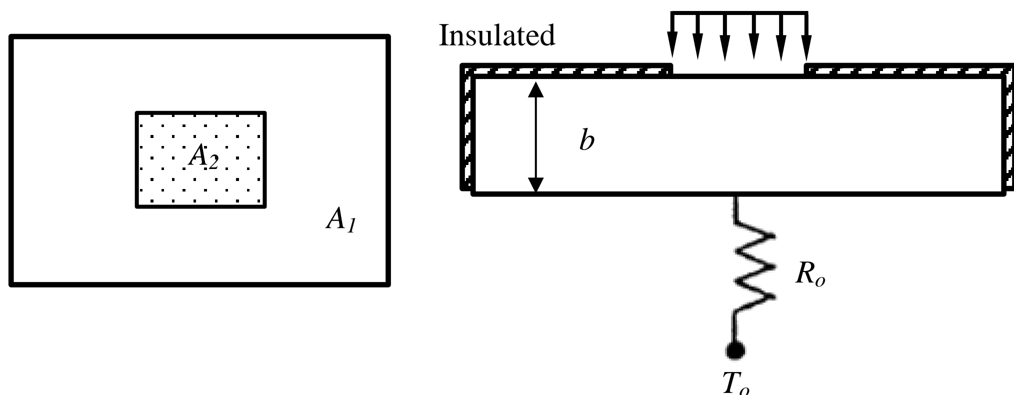


Fig. 5.2. Substrate surface area A_1 is subjected to a uniform heat source of area A_1 with insulated boundaries everywhere except at the heat source and at the bottom of the substrate

In a typical device, such as a power amplifier (PA) MMIC shown in Fig. 5.1, the substrate is solder-attached onto a carrier which is mounted onto a jig. Hence, instead of the base of the substrate being maintained at a constant temperature T_o, the base of the jig is usually the one maintained at a constant temperature T_∞. To determine T_o to be used in (4.42), the concept of spreading thermal resistance can be used. The thermal resistance network (Fig. 5.1)

consists of the spreading thermal resistance due to the jig (R_{jig}), the carrier (R_{carr}), the solder-attach layer (R_{so}) and the interface resistance (R_{int}) between the carrier and the jig. From [50], the thermal spreading resistance, R, of a plate with surface area of A_1 subjected to a uniform heat source of area A_2 with insulated boundary conditions everywhere except the heat source and the bottom of the substrate (Fig. 5.2) is expressed as:

$$R = \frac{\varepsilon\tau}{\sqrt{\pi}} + \frac{1}{2}(1-\varepsilon)^{\frac{3}{2}}\Phi_c \tag{5.1}$$

where

$$\Phi_c = \frac{\tanh(\lambda_c\tau) + \frac{\lambda_c}{Bi}}{1 + \frac{\lambda_c}{Bi}\tanh(\lambda_c\tau)} \tag{5.2}$$

with

$$\lambda_c = \pi + \frac{1}{\sqrt{\pi}\varepsilon} \tag{5.3}$$

$$\varepsilon = \frac{l_2}{l_1} \tag{5.4}$$

$$\tau = \frac{b}{l_1} \tag{5.5}$$

$$Bi = \frac{1}{\pi k t R_o} \tag{5.6}$$

$$l_1 = \sqrt{\frac{A_1}{\pi}} \tag{5.7}$$

$$l_2 = \sqrt{\frac{A_2}{\pi}} \tag{5.8}$$

External resistance, R_o, approaches zero when the boundary condition at the base of the substrate approaches an isothermal condition.

Using (5.1), the thermal resistance values due to subsequent layers with known thermal conductivity were easily determined to be: R_{jig} = 0.1365 K/W, R_{carr} = 1.1154 K/W and R_{so} = 0.1183 K/W. R_{int} has been empirically determined by Decker and Rosata in [15, 26] to be 193 K-mm^2/W.

The following parameters listed in Table 5.1 will be employed in this section unless specified otherwise:

Table 5.1. Parameters of a PA MMIC

Number of gates, n	10
Gate Width, W_g	150 µm
Gate Length, L_g	0.25 µm
Gate Pitch, P_g	24 µm
Substrate thickness, b	0.1 mm
Substrate Length, L_b	2.235 mm
Power dissipation, λ	2 W/mm
Temperature at the base of the jig, T_∞	25 ^{o}C
Temperature dependent thermal conductivity	(4.2)

From the thermal resistance network shown in Fig. 5.1, the average substrate base temperature, $T_{o,avg}$, is calculated to be 35.1 ^{o}C.

A three-dimensional finite element analysis (FEA) of the PA MMIC with the above mentioned parameters was carried out using the mesh shown in Fig. 5.3. The dimensions and material properties were adopted from Table 3.1. From the FEA, the temperature distribution along the base of the substrate is plotted in Fig. 5.4. The average substrate base temperature, $T_{o,avg}$, is calculated to be 35.5^{o}C, which is very close to the value calculated using the thermal resistance

network described above. This indicates that the thermal resistance network provides a good estimation of $T_{o,avg}$.

However from the FEA results (Fig. 5.4), it can be seen that the temperature distribution along the base of the substrate is not constant but has a maximum temperature, $T_{o,max}$ of 67.3°C. Hence, it is clear that the assumption of a constant substrate base temperature will result in an underestimation of the gate temperature T_g when used in (4.42). Therefore, it is necessary to obtain an analytical expression for the maximum temperature at the base of the substrate, $T_{o,max}$, and use this value in place of T_o in (4.42), in order to obtain a more accurate estimate of the maximum junction temperature.

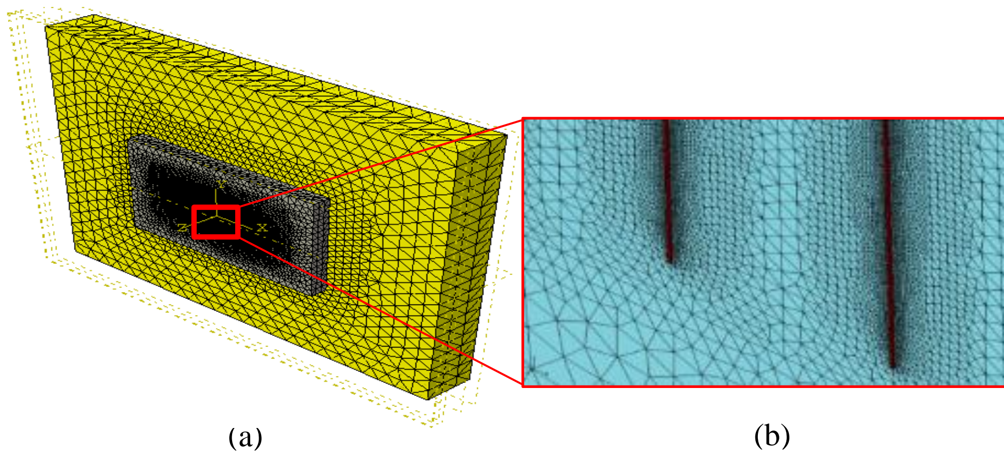


Fig. 5.3. Details of the 3D finite element mesh: (a) in the carrier and jig, and (b) around the gates

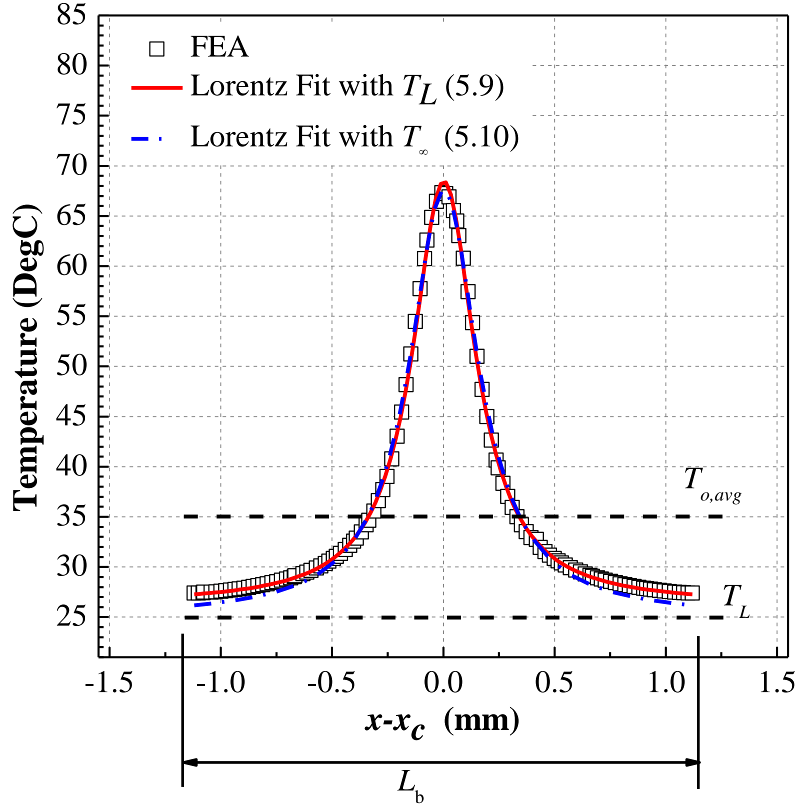


Fig. 5.4. A typical temperature distribution at the base of a substrate of a packaged PA MMIC computed from FEA and fitted with a Lorentz function

5.2.1. Lorentz Function

In the following section, an analytical method of calculating $T_{o,max}$ will be developed. It was found that the distribution of temperature, $T_{o,x}$, at the base of the substrate of a MMIC with parameters listed in Table 5.1, can be approximated by a Lorentz function (5.9) shown in Fig. 5.4:

$$T_{o,x} = T_L + 2Aw/\pi[4(x - x_c)^2 + w^2] \qquad (5.9)$$

where T_L is a curve-fitting constant, x_c is the location of the center of the curve, w is the width of the curve (in units mm) where $T_{o,x} - T_L = (T_{o,max} - T_L)/2$, and A is the area under the curve (in units mm^2) bounded by $T_{o,x} = T_L$.

The values of T_L for a typical range of values of overall length of the heat sources, l_s, and λ are shown in Fig. 5.5, where it can be observed that T_L is very close (within 1.3°C) to the ultimate heat sink temperature, T_∞. Hence, it is proposed to replace T_L in (5.9) with T_∞, since T_∞ is a known constant parameter. Therefore, the temperature distribution along the base of the substrate can be expressed by the following Lorentz function:

$$T_{o,x} = T_\infty + 2Aw/\pi[4(x-x_c)^2 + w^2] \tag{5.10}$$

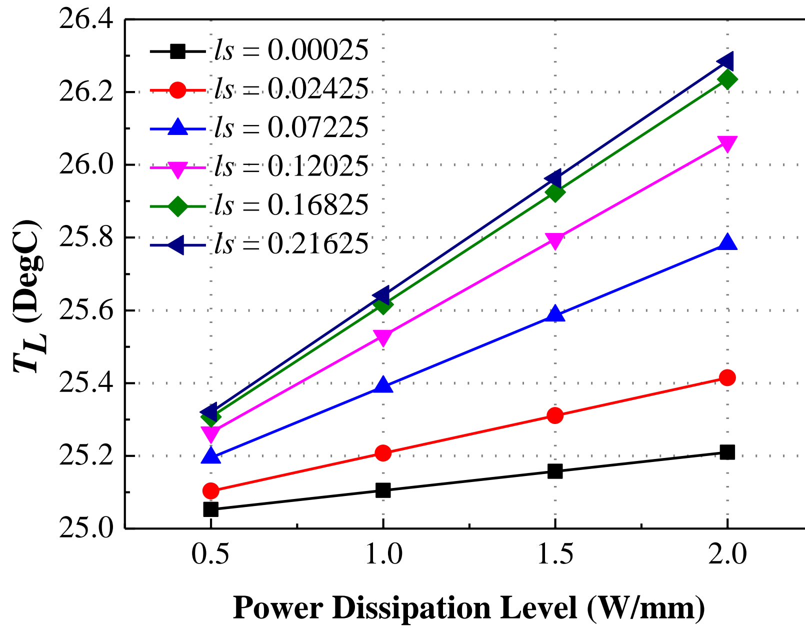


Fig. 5.5. Values of T_L for varying l_s and λ, with b = 100 μm

From (5.10), the maximum base temperature, $T_{o,max}$, is given by

$$T_{o,max} = T_\infty + 2A/\pi w \tag{5.11}$$

and the average temperature of the base of the substrate, $T_{o,avg}$, is expressed as:

$$\begin{aligned} T_{o,avg} &= \frac{1}{L_b}\int_{-\frac{L_b}{2}}^{\frac{L_b}{2}}\left[T_\infty + \frac{2A}{\pi}\frac{w}{4x'^2+w^2}\right]dx' \\ &= T_\infty + \frac{2A}{\pi L_b}\tan^{-1}(L_b/w) \end{aligned} \tag{5.12}$$

From (5.10) to (5.12), it can be shown easily that

$$\frac{T_{o,max} - T_{\infty}}{T_{o,avg} - T_{\infty}} = \frac{L_b}{w tan^{-1}\left(\frac{L_b}{w}\right)} = F(w, L_b) \tag{5.13}$$

For the MMIC with parameters listed in Table 5.1, it was found that w = 0.37806 mm and A = 25.35311 mm^2. The average and maximum temperatures at the base of the substrate calculated using (5.12) and (5.11) are 35.1^{o}C and 67.7^{o}C, respectively, which agree very well with the values of 35.5^{o}C and 67.3^{o}C computed using FEA. For the range of typical values of l_s and λ shown in Fig. 5.5, it has been found that the difference in the values of $T_{o,avg}$ calculated using (5.12) differed from those computed using FEA by less than 1.3% while the corresponding difference in $T_{o,max}$ is less than 1.5%. Moreover, the difference in the values of $T_{o,avg}$ calculated using (5.12) differed from those calculated using the spreading resistance technique [50] by 0.7%. Therefore, the Lorentz function has been shown to be able to approximate the temperature distribution at the base of the substrate in a MMIC with good accuracy.

5.2.2. Analytical Solution for $T_{o,max}$

In order to obtain an analytical solution for $T_{o,max}$ using (5.13), we need to first obtain an analytical solution for w and hence $F(w,L_b)$ in (5.13). With reference to Fig. 5.6, it is proposed that w can be approximated by:

$$w = 2b\tan(\beta) + l_s \tag{5.14}$$

where the overall length of the heat source, l_s due to n gates can be calculated from:

$$l_s = (n-1)p_g + L_g \tag{5.15}$$

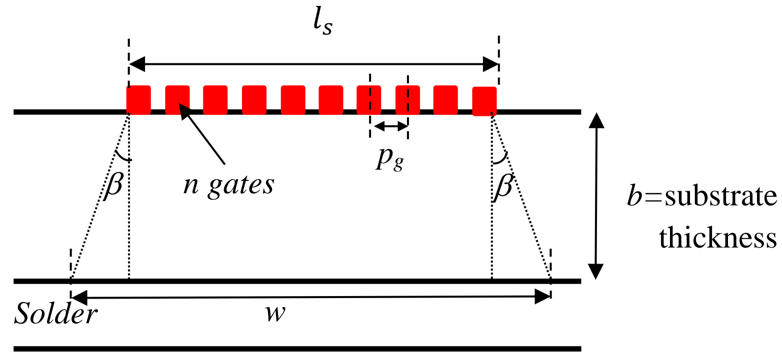


Fig. 5.6. Determination of w from thickness of substrate, b, length of heat source, l_s, and angle β

Then, the correct maximum base temperature ($T_{o,max}$) to be used in (4.42) can be found from (5.13) by:

$$T_{o.max} = \left(T_{o,avg} - T_\infty\right) \times F(w, L_b) + T_\infty \tag{5.16}$$

where $T_{o,avg}$ can be determined from the concept of spreading thermal resistance network [50].

The above solution for $T_{o,max}$ requires an appropriate value of β in equation (5.14), which we shall call β_o. This can be done, as described in the following section, by obtaining an expression for β_o in terms of the basic device parameters such as gate length, gate pitch and number of gates, with the aid of finite element analysis.

5.2.3. Determination of β_o

The number of gates, n, is varied from 1 to 10 with its corresponding l_s calculated using (5.15). The angle, β, is varied from 32.5° to 55°. The power dissipation level, λ, is also varied from 0.5 W/mm to 2 W/mm. For each analysis, the power dissipation λ is fixed while l_s and β are varied. The percentage difference between the value of $T_{o,max}$ calculated using (5.16) and that calculated using FEA for different power dissipation levels is plotted in Fig. 5.7 to Fig. 5.10.

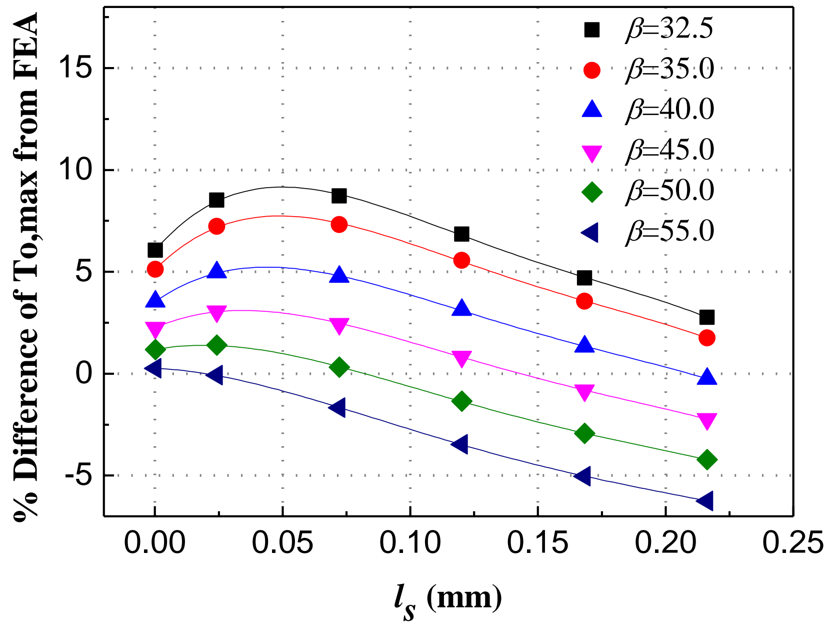


Fig. 5.7. Effect of l_s and β on $T_{o,max}$ for $\lambda = 0.5$W/mm

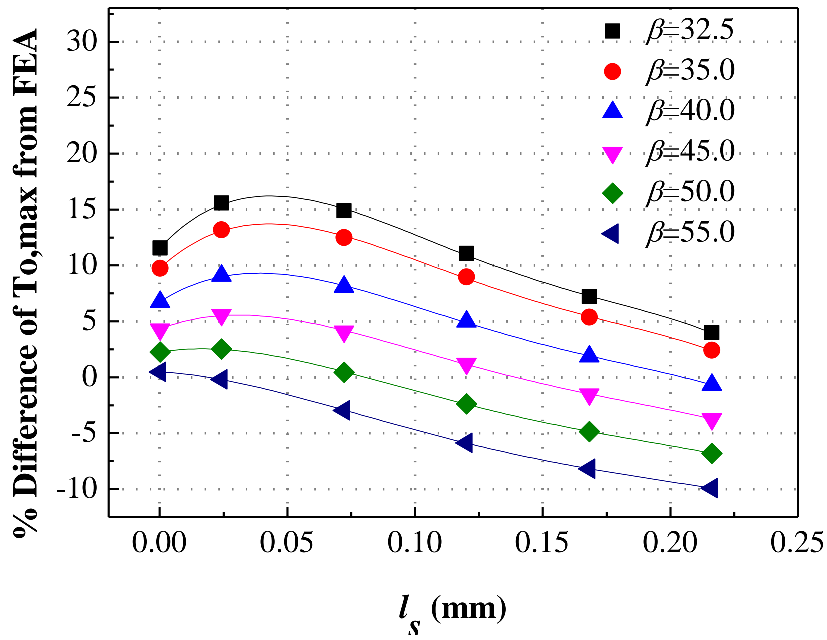


Fig. 5.8. Effect of l_s and β on $T_{o,max}$ for λ = 1.0 W/mm

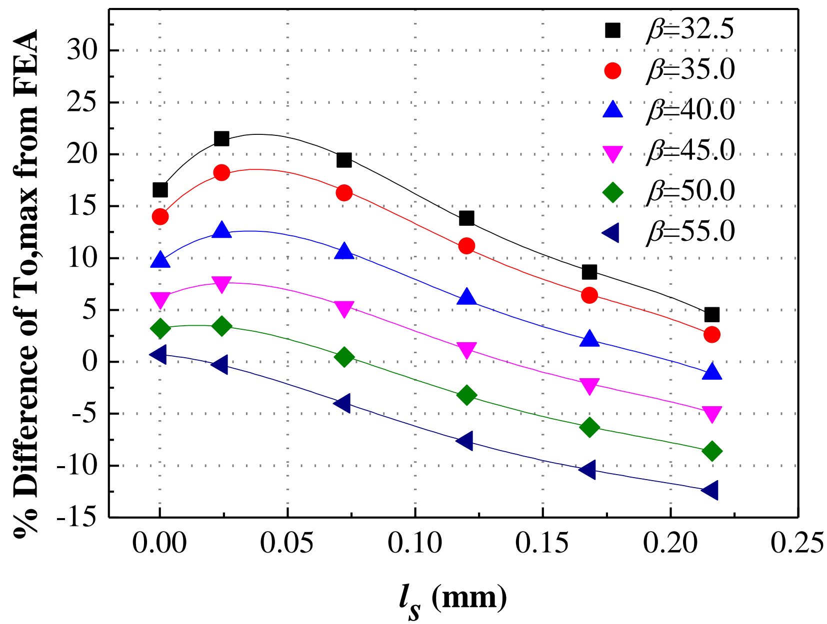


Fig. 5.9. Effect of l_s and β on $T_{o,max}$ for λ = 1.5 W/mm

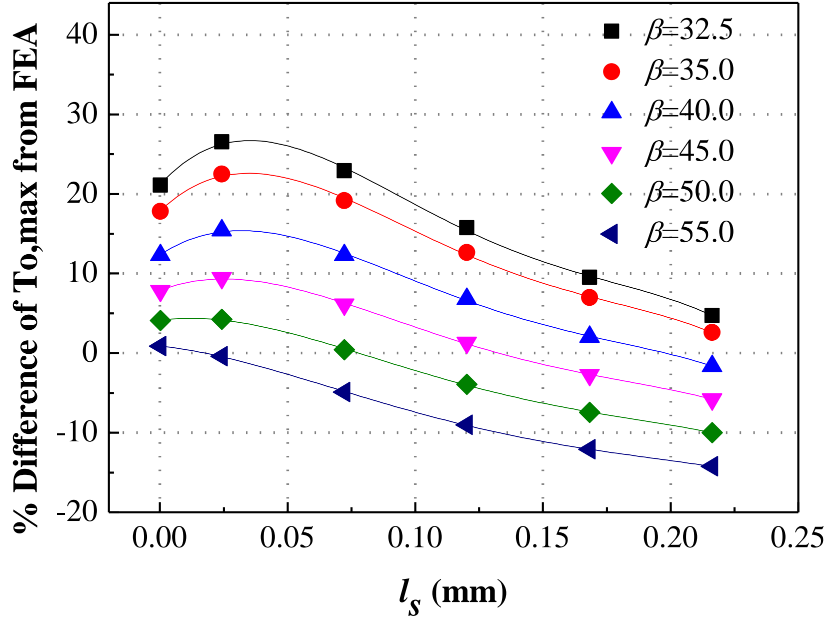


Fig. 5.10. Effect of l_s and β on $T_{o,max}$ for λ = 2.0 W/mm

From Fig. 5.7 to Fig. 5.10, the optimum values of the angle β, called β_o, which gives zero difference between $T_{o,max}$ calculated from (5.13) and that calculated from FEA can be determined graphically. However, they can also be determined more accurately by iteration of equations (5.11), (5.13) and (5.14). Values of β_o thus obtained, are plotted in Fig. 5.11. From the results, it can be seen that β_o varies linearly with l_s and this linear relationship is independent of the power dissipation level for the range studied, which covers most current GaAs MMIC devices. A linear relationship between β_o and l_s can be expressed as:

$$\beta_o = -82.70 \times l_s + 56.54 \qquad (5.17)$$

within an accuracy of better than 2%.

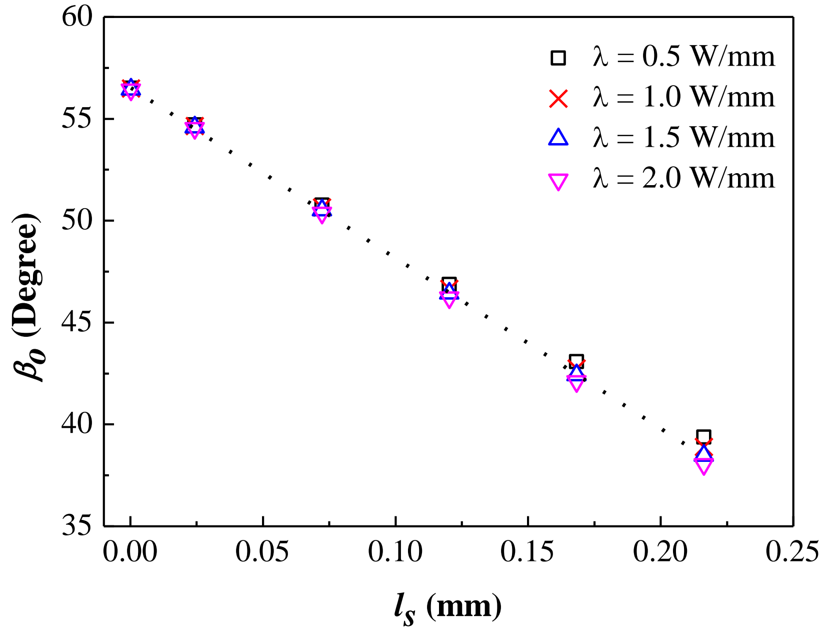


Fig. 5.11. Variation of β_o with l_s

5.3. Comparison of Junction Temperature Calculated using the Present Analytical Method with Measured Values and FEA

In this section, the peak operating gate temperatures of a GaAs power amplifier (PA) MMIC consisting of two 10 x 150 μm transistors, are measured using thermoreflectance thermography (TRT) [58, 66] and plotted in Fig. 5.12. Also plotted in Fig. 5.12 for comparison are the maximum gate temperatures calculated using (a) the present analytical method incorporating the *maximum* substrate base temperature $T_{o,max}$ obtained from (5.16); (b) the present analytical method using the *average* substrate base temperature $T_{o,avg}$ obtained from the spreading thermal resistance method [50]; (c) Darwish's method [46]; and (d) FEA [58]. As can be seen in Fig. 5.12, the maximum gate temperature calculated using the present analytical method with $T_{o,max}$ agrees

extremely well with the measured values and very well with the FEA-calculated values. On the other hand, maximum gate temperatures calculated using Darwish [46] with $T_{o,max}$ as the base temperature, are much higher. This is because in Darwish's model [46], a surface planar heat source is assumed which has been shown to lead to higher than actual gate temperatures (Fig. 4.11).

It can be noted in Fig. 5.12 that when the present method is used with $T_{o,avg}$, the gate temperatures calculated are significantly below the measured temperatures. This demonstrates very clearly that the maximum temperature at the base of the substrate should be taken into account as has been done in this work. It should be noted that the maximum gate temperature, and not the maximum junction temperature, has been used for comparison in Fig. 5.12 since the temperature measured using TRT is that at the surface of the MMIC device. With the more realistic model of an embedded heat source used in the present work, the junction temperature is different from the gate temperature and can be calculated from (4.42).

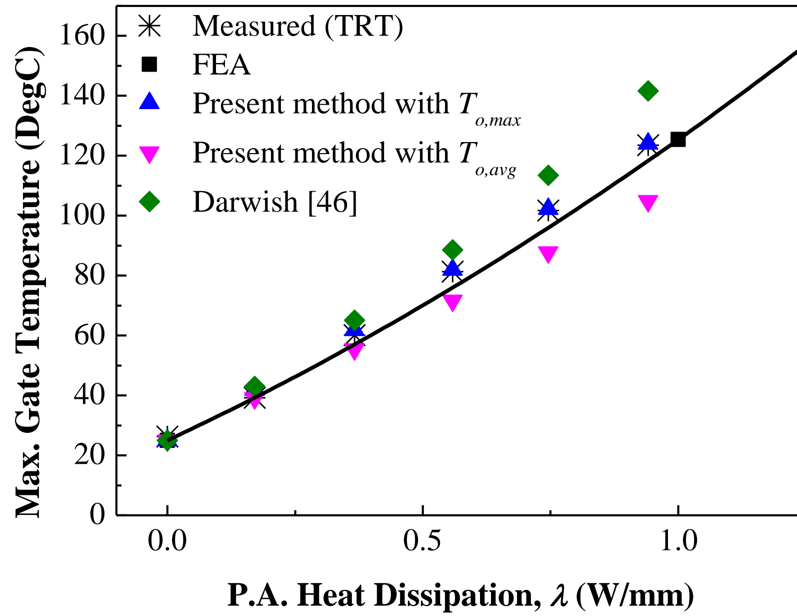


Fig. 5.12. Comparison between analytical, FEA and TRT measured temperatures for the PA MMIC

5.4. Extending Formulation of β_o to all Typical Range of Substrate Thickness

As the substrate thickness typically ranges from 100 µm to 300 µm [64, 65], the linear relationship found between β_o and l_s for substrate thickness of 100 µm (5.17) may not be applicable for other substrate thicknesses. Therefore, this sections will aim to formulate β_o as a function of both l_s and substrate thickness, b, i.e. β_o (l_s, b).

The following parameters listed in Table 5.2 will be considered in this section unless specified otherwise:

Table 5.2. Parameters of a PA MMIC

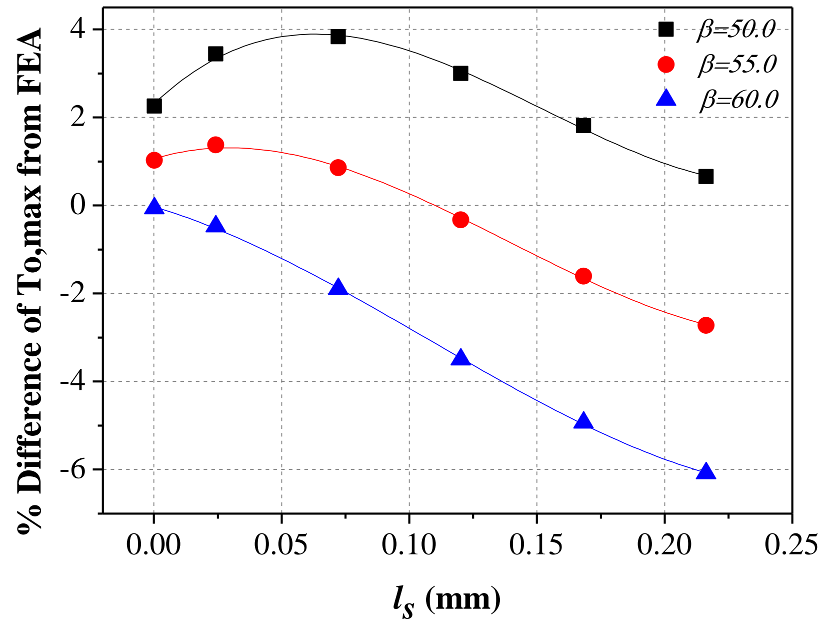
Parameter	Value
Number of gates, n	1 to 10
Gate Width, W_g	150 µm
Gate Length, L_g	0.25 µm
Gate Pitch, P_g	24 µm
Substrate thickness, b	0.1 to 0.3 mm
Substrate Length, L_b	2.235 mm
Power dissipation, λ	1 to 2 W/mm
Temperature at the base of the jig, T_∞	25 ^{o}C
Temperature dependent thermal conductivity	(4.2)

Similar three-dimensional finite element analyses (FEA) of the PA MMIC adopted in section 5.2 with the above-mentioned parameters were performed to calculate the base temperature of the substrate and the junction temperature. The thickness of the substrate was varied from 0.1 mm to 0.3 mm. The numerical results obtained will be used to compare with the analytically calculated base temperatures and the junction temperatures.

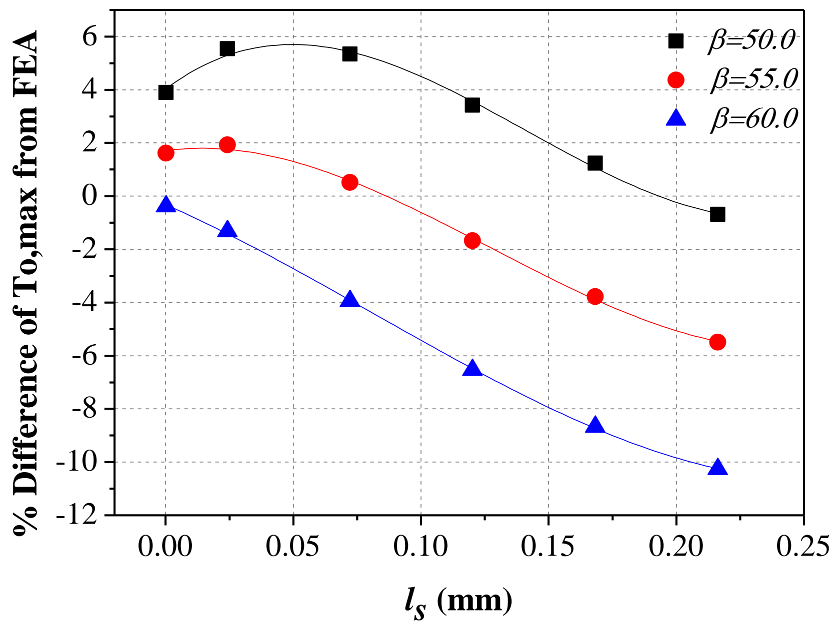
5.4.1. Determination of $\beta_o(l_s,b)$

The number of gates, n, was varied from 1 to 10 with its corresponding l_s calculated using (5.15). The power dissipation level, λ, was also varied between 1.0 W/mm and 2 W/mm. The results for substrate thickness b = 0.1 mm are shown in Fig. 5.8 and Fig. 5.10. Thus, the substrate thickness will be varied from 0.15mm to 0.3mm to investigate its effect on β_o. For each analysis of various substrate thickness, the power dissipation λ is fixed while l_s and β are varied. The angle β will be varied accordingly in order to determine the minimum percentage difference between the calculated $T_{o,max}$ using (5.16) and

those calculated using FEA for different power dissipation level and substrate thickness. The results are compared and plotted in Fig. 5.13 to Fig. 5.15.

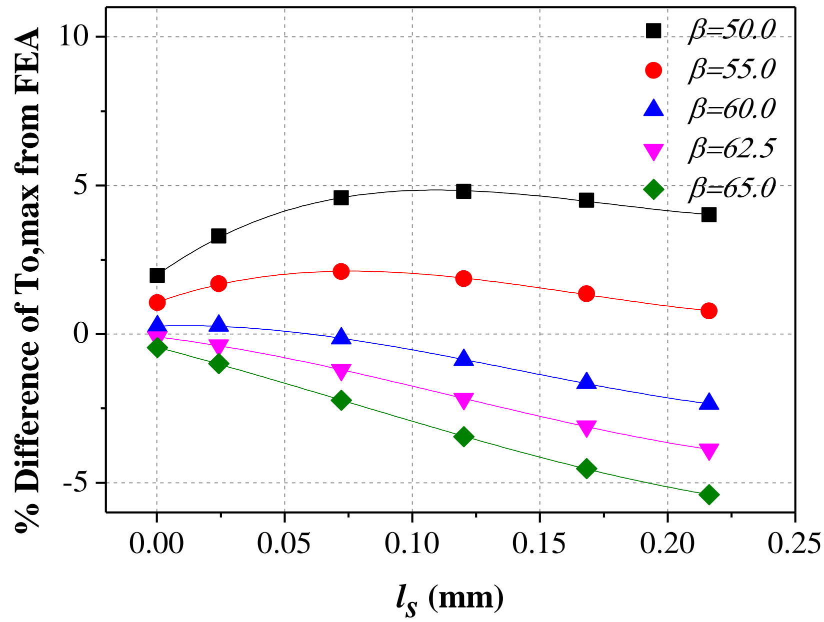


(a)

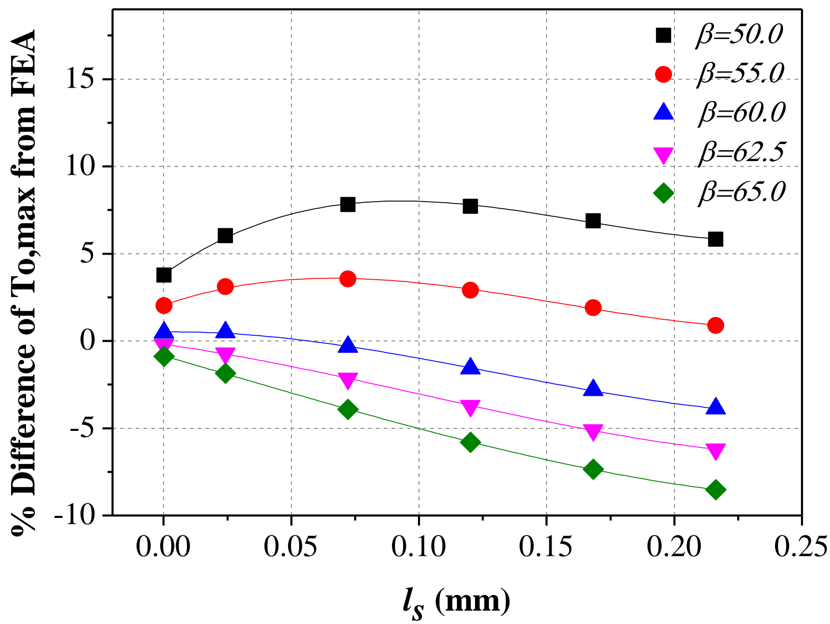


(b)

Fig. 5.13. Effect of l_s and β on $T_{o,max}$ for b=150 μm with (a) λ = 1.0 W/mm and (b) λ = 2.0 W/mm

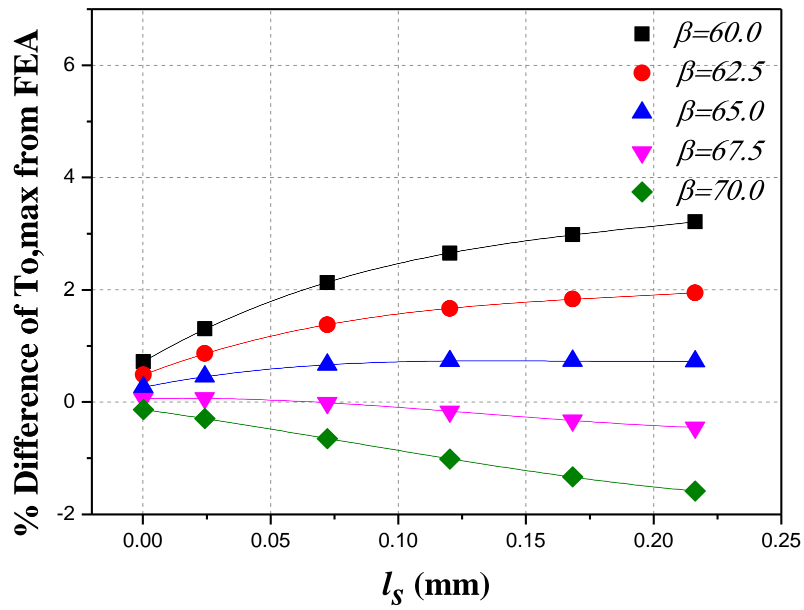


(a)

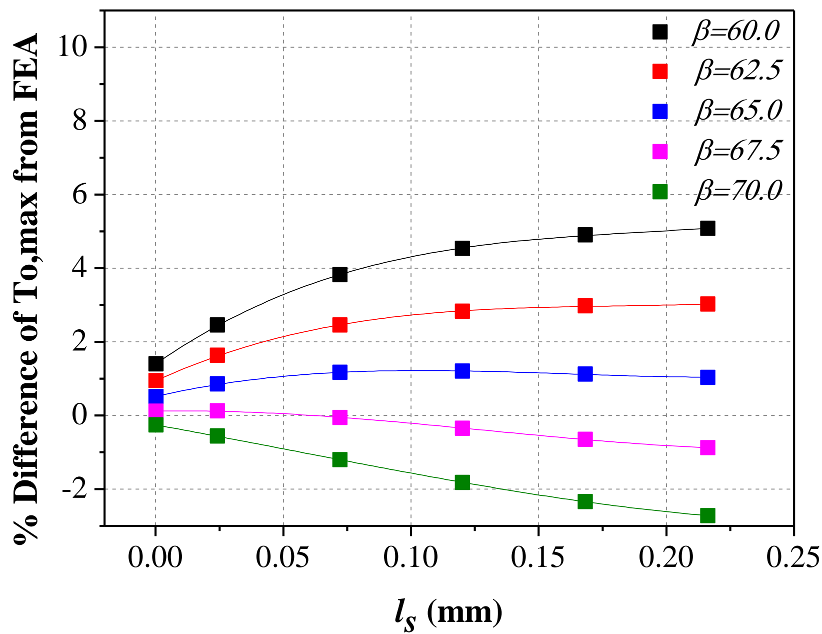


(b)

Fig. 5.14. Effect of l_s and β on $T_{o,max}$ for b=200 μm with (a) λ = 1.0 W/mm and (b) λ = 2.0 W/mm



(a)



(b)

Fig. 5.15. . Effect of l_s and β on $T_{o,max}$ for b=300 μm with (a) $\lambda = 1.0$ W/mm and (b) $\lambda = 2.0$ W/mm

From Fig. 5.8, Fig. 5.10, and Fig. 5.13 to Fig. 5.15, the optimum values of angle β, called β_o, which give zero difference between $T_{o,max}$ calculated from (5.13) and that calculated from FEA for substrate thickness of 100 μm to 300 μm are determined and plotted in Fig. 5.16. From the results, it can be seen that β_o varies linearly with l_s for all substrate thicknesses studied. This linear relationship is again independent of the power dissipation level for the range studied. The power dissipation level has a minimum effect on β_o even when the substrate thickness was varied.

From Fig. 5.16, β_o (l_s, b) can be expressed as:

$$\beta_o(l_s, b) = \left[-203.06e^{\left(\frac{-b}{0.267}\right)} + 65.30\right] l_s + \left[-32.03e^{\left(\frac{-b}{0.259}\right)} + 77.47\right] \quad (5.18)$$

within an accuracy of better than 2%.

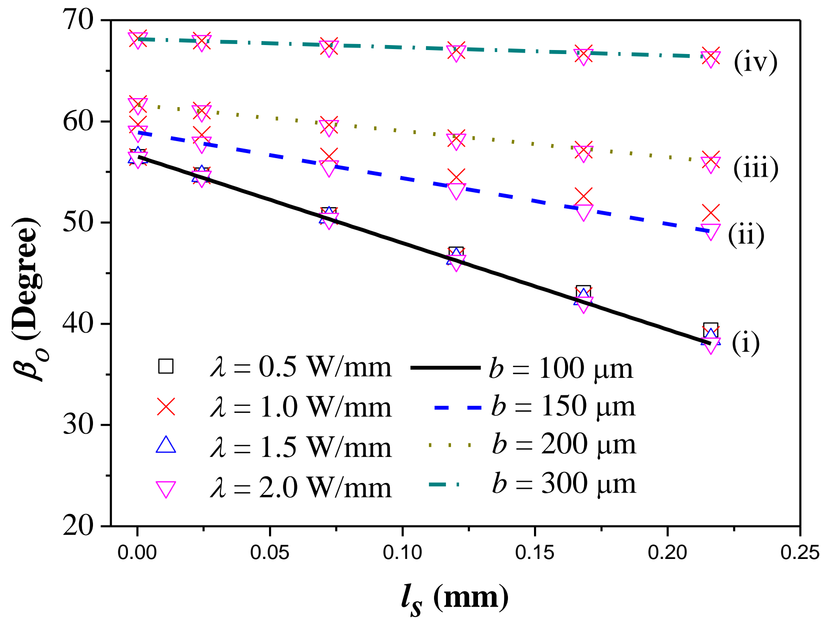


Fig. 5.16. Variation of β_o with l_s for substrate thickness of (i) b=100µm, (ii) b=150µm, (iii) b=200µm and (iv) b=300µm

5.4.2. Comparison of Junction Temperature Calculated using the Present Analytical Method with FEA

In this section, the peak operating junction temperatures calculated using (4.42) for substrate thickness of 0.1 mm to 0.3 mm was compared with those calculated using FEA. The total number of gates was varied from 1 to 10. The power dissipation level was also varied from 1W/mm to 2W/mm. The maximum base temperature, $T_{o,max}$, at the base of the substrate was calculated using (5.16) and was used in place of T_o in (4.42). The results are plotted in Fig. 5.17 to Fig. 5.20 for comparison.

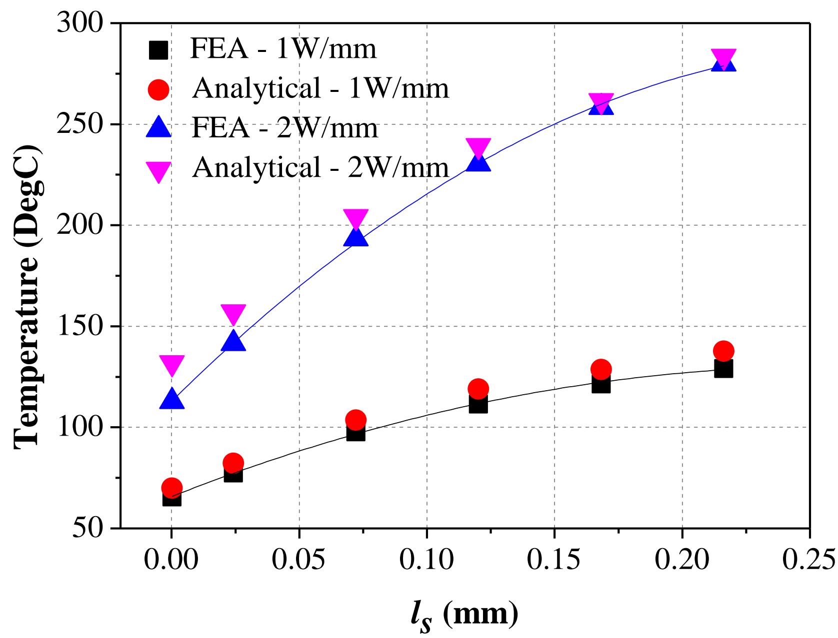


Fig. 5.17. Comparison between analytical and FEA calculated temperatures for the PA MMIC for b=0.1 mm

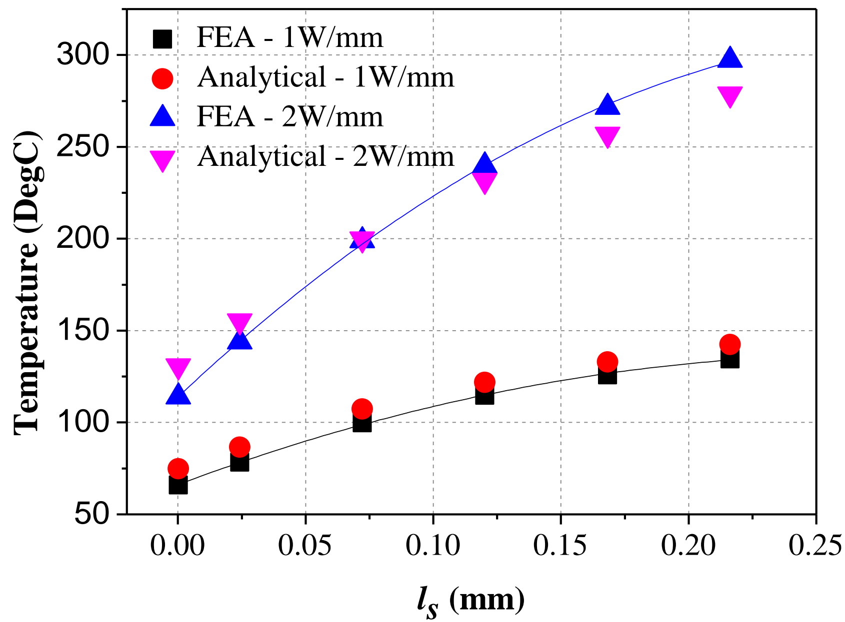


Fig. 5.18. Comparison between analytical and FEA calculated temperatures for the PA MMIC for b=0.15 mm

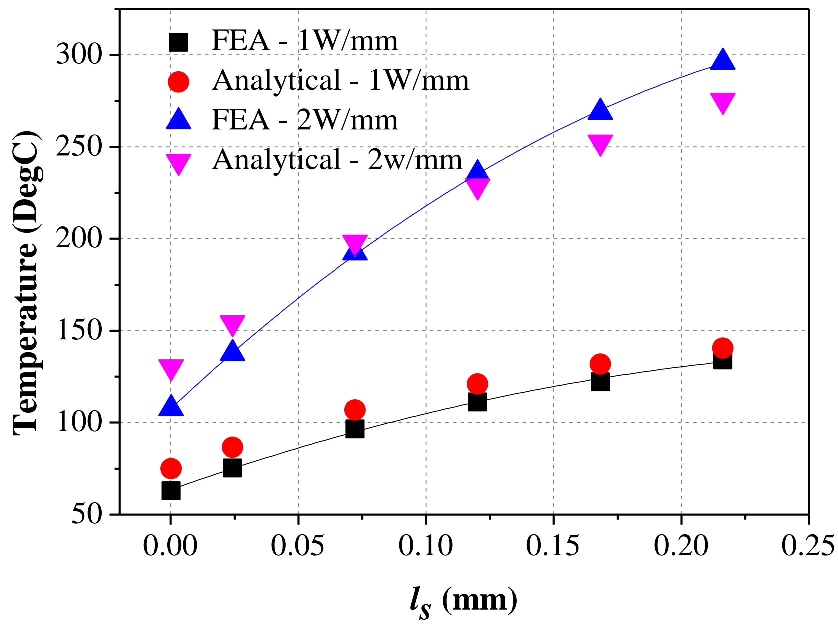


Fig. 5.19. Comparison between analytical and FEA calculated temperatures for the PA MMIC for b=0.2 mm

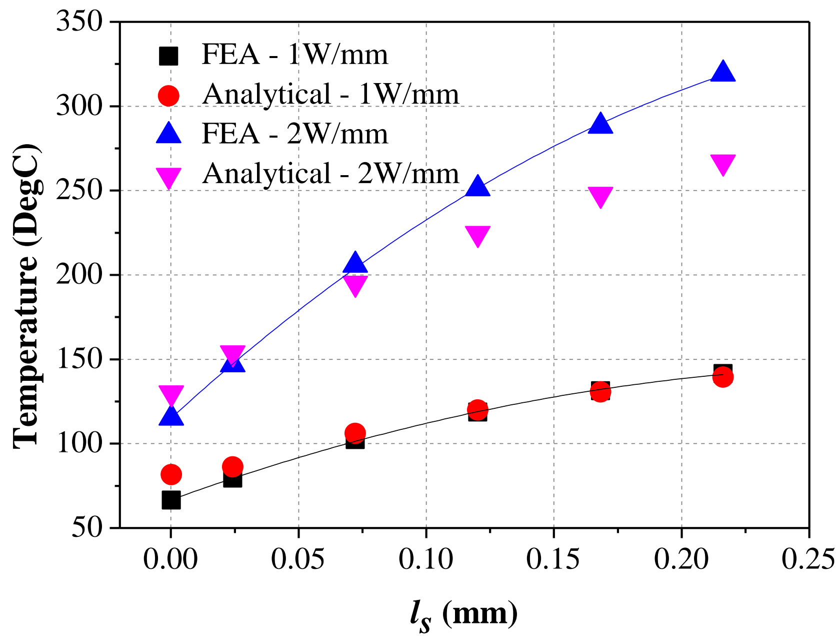


Fig. 5.20. Comparison between analytical and FEA calculated temperatures for the PA MMIC for b=0.3 mm

From the results, it can be seen that the junction temperatures calculated analytically agree very well with those calculated using FEA for power dissipation $\lambda = 1$ W/mm across the range of substrate thickness studied. On the other hand for $\lambda = 2$ W/mm, the difference between the analytically calculated and FEA junction temperatures is more than 10% when the substrate thickness becomes greater than 200 μm. Typically, power dissipating devices such as FETs require thinner substrate in order to achieve low thermal resistance. A substrate thickness of 100 μm is an optimum value for power applications in the GHz range while a substrate thickness of more than 200 μm is for low power applications in the same frequency range [64]. Therefore, one can conclude that this novel analytical method developed for calculating the junction temperature by incorporating the correct temperature at the base of the substrate is able to give an accurate quick insight in the early design stage for the current optimum substrate thickness requirement.

5.5. Conclusion

In this work, it has been shown that the temperature distribution at the base of the substrate of a packaged MMIC power amplifier can be expressed in terms of a Lorentz distribution. From this distribution, a relationship between the maximum base temperature $T_{o,max}$ and the average base temperature $T_{o,avg}$ can be obtained as a function $F(w,L_b)$ of the basic parameters of the device such as gate length, gate pitch, number of gates and substrate base length. The average base temperature can be calculated using the concept of spreading thermal resistance network, which together with $F(w,L_b)$ allows for the determination of an accurate maximum substrate base temperature, $T_{o,max}$.

This, in conjunction with the novel closed-form analytical solution for the temperature distribution within the substrate described earlier in Chapter 4, has been shown to predict maximum gate temperatures which agree very well with those calculated using FEA and those measured using thermoreflectance thermography.

This work has also been established to be applicable a typical range of substrate thickness by deriving a general formulation as a function of substrate thickness and total number of gates for estimating the temperature at the base of the substrate in a packaged MMIC device. This formulation gives an estimation of the base temperature of the substrate within an accuracy of 2%. This work will be very useful for predicting the maximum junction temperature of a power device with current optimum substrate thickness requirement by incorporating the correct maximum base temperature in analytical solutions. In addition, the present analytical method is much easier to implement unlike past analytical methods.

CHAPTER 6

THERMAL CHARACTERIZATION OF HIGH POWER DEVICES

6.1. Introduction

Thermal characterization of devices is important for reliable circuit design. Like all electronic devices, the lifetime of MMIC chips is highly dependent on its peak operating junction temperature. The predicted peak junction temperature can be used to study its effect on the reliability and failure mechanisms of MMIC devices. With increasing demand for improved performance on these devices, they are expected to handle higher power densities. As a result, the reliability of devices decreases with increasing junction temperature. Therefore, it is important to prevent the junction temperature from exceeding its safe limit. An accurate prediction of the peak junction temperature will provide useful information on the reliability and lifetime of these devices.

To predict the peak operating junction temperature of a power amplifier (PA) MMIC, experimental techniques can be used to measure the gate temperature. Accurate temperature measurement techniques are important for reliability assessment of devices and validation of analytical and numerical solutions. Temperature measurement techniques range from micro-scale to nano-scale resolution and each has its own advantages and disadvantages [1, 2, 66]. For example, the micro-Raman and Scanning Thermal Microscopy (SthM) have excellent spatial resolution of 0.5µm and 0.05µm (on smooth surface), respectively. However, both techniques require long acquisition time to obtain

a thermal image. Liquid Crystal thermography (LCT) has a spatial resolution of 2 to 5µm. However, this technique requires a deposition of a thin layer of liquid crystal on the device under test, which may pose some uncertainties as the extraneous LCT layer may alter the original temperature of the surface and the actual performance of the device. Infrared thermography (IRT) is the most common technique used for direct and non-invasive temperature measurement. It has a spatial resolution of 3 to 10 µm. However, this is not enough for an accurate measurement of the gate temperature as the typical gate length found in the current PA MMIC devices is 0.25 µm. In addition, presence of metallic surfaces in semiconductor devices requires proper calibration of emissivity before correct temperatures can be inferred from the measured apparent temperature.

As can be seen, the challenges in using these characterization techniques for temperature measurement of MMIC chips are insufficient spatial resolution, presence of reflective surfaces and submicron size features in the structures. On the other hand, Thermoreflectance thermography (TRT) is suitable for measuring temperature of low emissivity surfaces. It has a spatial resolution of 0.15 µm to 0.5 µm which is adequate for thermal characterization of current MMIC devices. It also has a fast acquisition rate. However, it requires transient conditions as well as the employment of a lock-in technique.

Therefore in this work,, thermal characterization of the gate temperature of power amplifier (PA) MMIC devices will be carried out using TRT. IRT, a popular technique often used for characterizing MMIC devices, will also be used and the results obtained will be compared with TRT. An overview of the principles and the methodology for both characterization techniques will be

presented. In addition, the challenges faced in attempting to measure the gate temperature with either IRT or TRT will be discussed. Both techniques allow for real time field imaging of the surface temperature of the device.

6.2. Thermoreflectance Thermography

6.2.1. An Overview

TRT has a fast acquisition time and is suitable for temperature characterization of reflective surfaces present on devices such as PA MMICs. It is based on the relative change in reflectivity, $\Delta R/R$, of a sample surface as a function of change in temperature, ΔT, which are related by the thermoreflectance coefficient, C_{TR}, of the material according to (6.1) [30]:

$$\frac{\Delta R}{R} = \left(\frac{1}{R}\frac{\partial R}{\partial T}\right)\Delta T = C_{TR}\Delta T \tag{6.1}$$

Unlike IRT which requires emissivity to be calibrated for each experimental set-up, TRT requires C_{TR} to be characterized once for a given material. To do so, the system measures the relative change in reflectivity $\Delta R/R$ of a material surface due to a change in the temperature ΔT by illuminating an LED source on the sample. As the value of C_{TR} does vary sharply within the spectral region of interest (e.g. the visible spectrum), the choice of illumination wavelength determines not only the spatial resolution of the technique but also the sensitivity [21]. For most metals and semiconductor materials, the value of C_{TR} is typically of the order of 10^{-5} K^{-1} to 10^{-2} K^{-1}. Therefore, a highly

sensitivity measurement is required to obtain quantitative information about the temperature of the device under test.

In this work, a Microsanj Thermoreflectance Image Analyzer was used (Fig. 6.1). This system when coupled with a 50X objective lens provides a spatial resolution of 0.232µm. A thermal chuck is used to maintain the base of the device at a constant temperature.

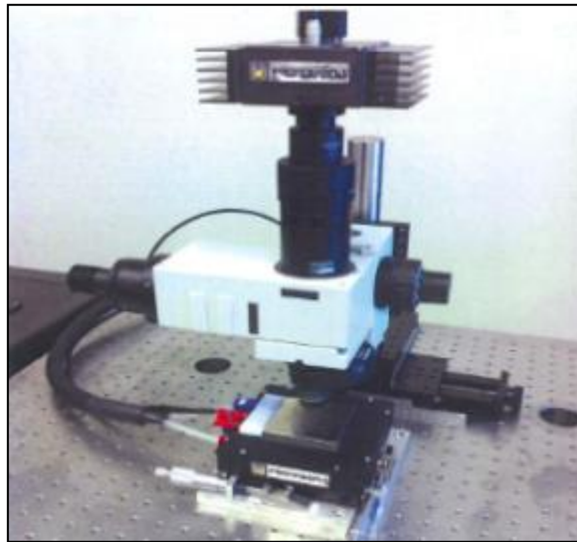


Fig. 6.1. Thermoreflectance Image Analyzer

In the following sections, the experimental methodology for characterization of thermoreflectance coefficient and temperature measurement using TRT will be discussed. The measured gate temperatures of both gallium arsenide (GaAs) and gallium nitride (GaN) PA MMIC devices obtained using TRT will be presented.

6.2.2. Theromoreflectance Coefficient Characterization

Before any quantitative deduction can be made on the measured temperature, it is necessary to characterize the material for its thermoreflectance coefficient,

C_{TR}. In this section, the experimental set-up for C_{TR} characterization will be presented.

a. Experimental Set-up

The experimental set-up used for characterizing the thermoreflectance coefficient, C_{TR}, is shown in Fig. 6.2 and Fig. 6.3. As shown in Fig. 6.2, the sample is placed on a thermoelectric module (TEM) for characterization of C_{TR}. A thermocouple probe is placed on the top surface of the sample to monitor the change in the temperature ΔT as the TEM heats up the sample. High temperature thermal glue is used to ensure that the thermocouple tip is in good contact with the surface of the sample.

The simultaneous timing graph of the characterization process is shown in Fig. 6.4. An LED illumination source is focused onto the sample surface by a microscope objective throughout the whole measurement. The CCD camera is triggered at a frequency f. The amount of light intensity that is reflected to the CCD camera from the surface in response to the change in sample temperature is measured by the system and analysed by a computer. To determine the relative change in reflectivity, $\Delta R/R$, with respect to change in temperature, ΔT, the system measures the reflectivity at two time intervals, i.e.:

i. Before a power step input is supplied to the TEM, the system measures the initial reflectivity R_i at initial temperature T_i measured by a thermocouple.

ii. A power step input in supplied to the TEM to heat up the sample to a steady state temperature of T_1. Upon reaching steady state, the system measures the reflectivity R_1 of the sample surface.

The relative change in reflectivity $\Delta R/R = (R_1 - R_i)/R_i$ with respect to the change in temperature $\Delta T = (T_1 - T_i)$ is determinined. By repeating the measurement at different amplitudes of ΔT, a linear relation between $\Delta R/R$ and ΔT can be obtained, for which the slope determines the thermoreflectance coefficient, C_{TR}.

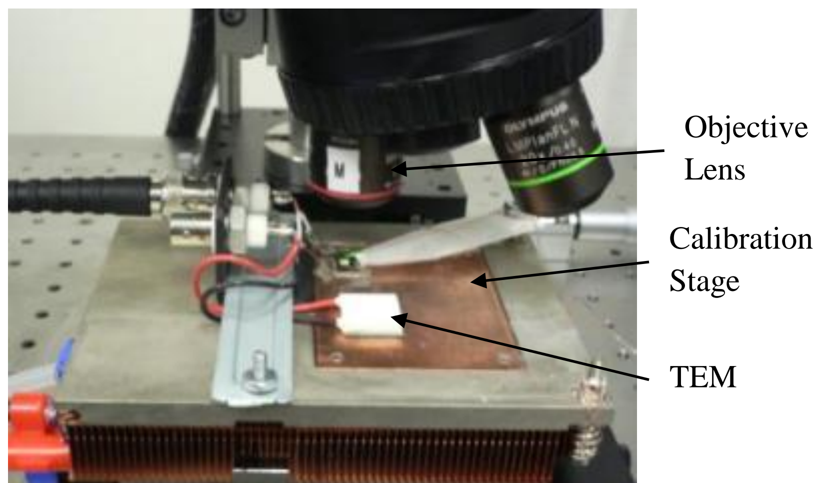


Fig. 6.2. Experimental set-up for C_{TR} characterization

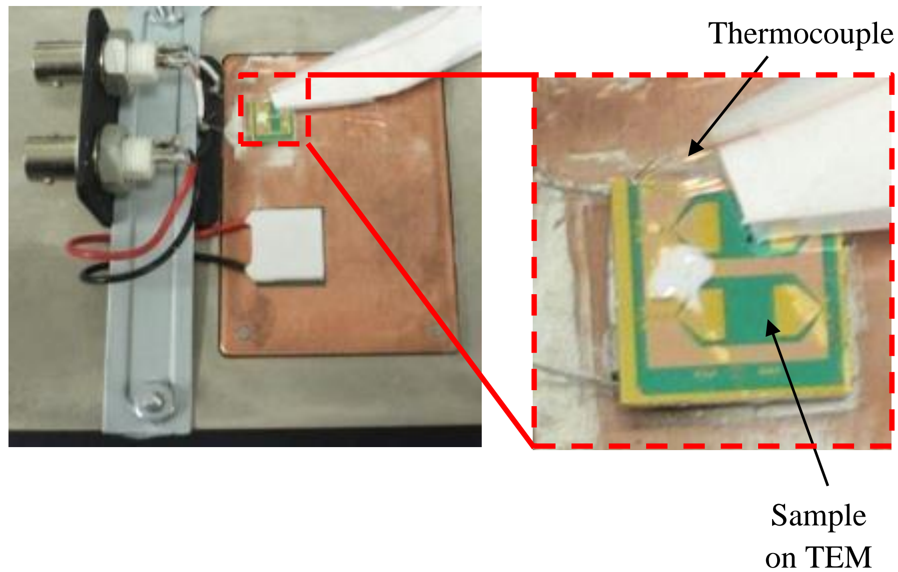
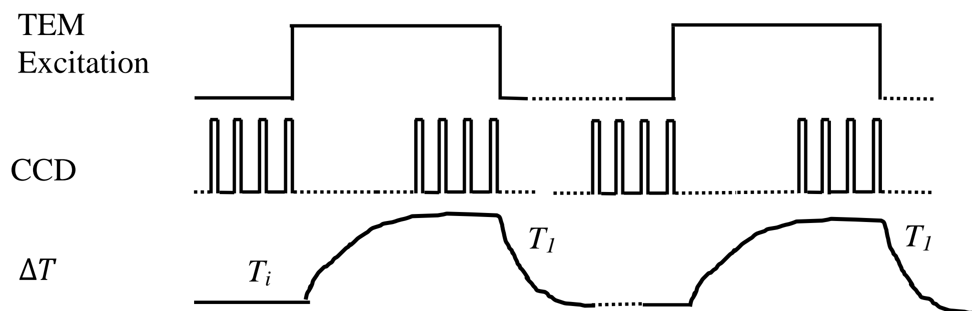


Fig. 6.3. Top view of Fig. 6.2: the sample is placed on the TEM for C_{TR} characterization. Thermocouple is used to measure $\Delta \boldsymbol{T}$ of the sample



Light always on (without pulse illumination)

Fig. 6.4. Simultaneous timing graph of the TEM excitation, CCD, LED and variation of temperature, $\Delta \boldsymbol{T}$.

b. Measurement of Thermoreflectance Coefficient of GaAs

In this section, the C_{TR} value for the GaAs gate will be measured. The following objective lens are used:

i. 5X objective lens

ii. 20X objective lens

iii. 100X objective lens

The field of view of a die consisting of GaAs transistors obtained using a 5x, 20x and 100x objective lens is shown in Fig. 6.5. A yellow box is drawn at the source-drain (S-D) pad region and a yellow line is drawn at the gate region. The following C_{TR} results presented are measured using an LED source of wavelength 530 *nm*.

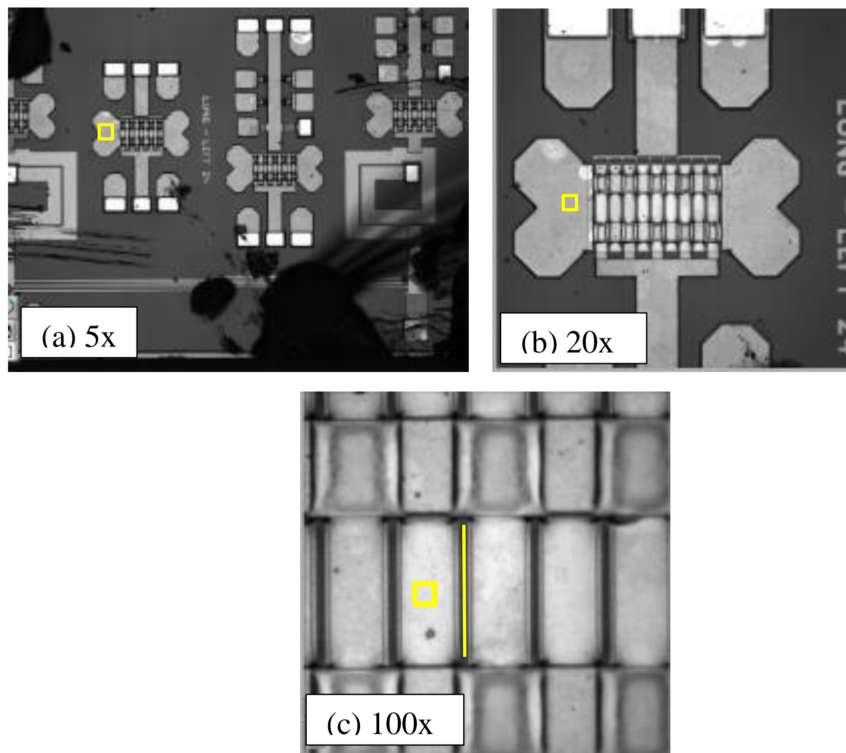


Fig. 6.5. Field of view of the GaAs chip obtained using (a) a 5X objective lens, (b) a 20X objective lens and (c) a 100X objective lens

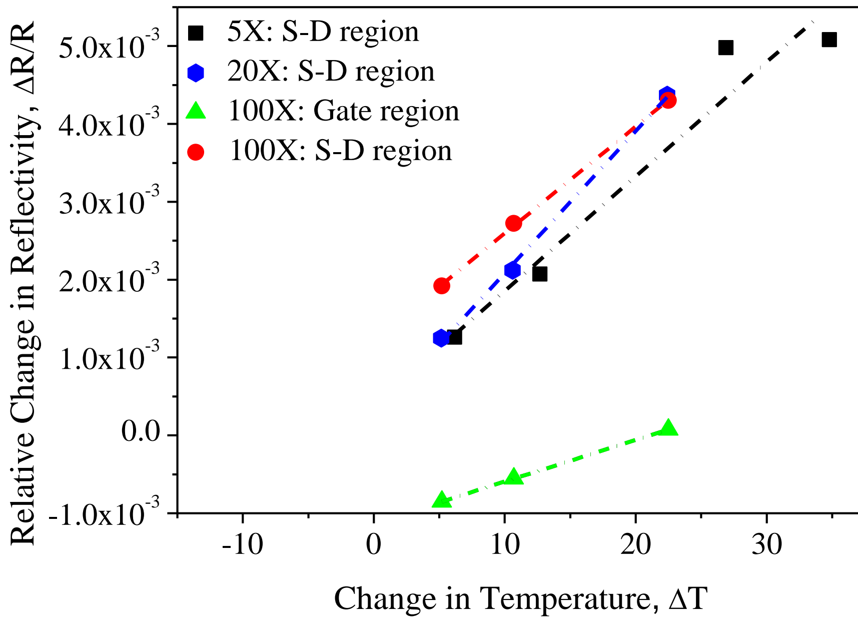


Fig. 6.6. A plot of $\Delta R/R$ versus ΔT obtained using an illuminating light source of wavelength 530nm with objective lens of 5X, 20X and 100X

In Fig. 6.6, the relative changes in the reflectivity, $\Delta R/R$, in response to the changes in temperature, ΔT, obtained using different objective lenses for different regions of interest are plotted. A linear fit has been made for each set of measured data where the slope corresponds to the C_{TR} value. The results are summarized in Table 6.1 to Table 6.3.

Table 6.1. Tabulated C_{TR} values for GaAs chip measured using a 5X objective lens with a 530 nm illuminating light source.

Objective Lens	ΔT	C_{TR}	$\Delta R/R$
5X	6.17	2.05E-04	1.26E-03
	12.7	1.63E-04	2.07E-03
	26.9	1.85E-04	4.98E-03
	34.8	1.46E-04	5.08E-03
Average C_{TR} (slope)		1.47E-04	

Table 6.2. Tabulated C_{TR} values for GaAs chip measured using a 20X objective lens with a 530 nm illuminating light source

Objective Lens	ΔT	C_{TR}	$\Delta R/R$
20X	5.15	2.42E-04	1.25E-03
	10.6	2.00E-04	2.12E-03
	22.4	1.95E-04	4.37E-03
Average C_{TR} (slope)		1.60E-04	

Table 6.3. Tabulated C_{TR} values for GaAs chip measured using a 100X objective lens with a 530 nm illuminating light source

Objective Lens	gate			S-D Region	
	ΔT	C_{TR}	$\Delta R/R$	C_{TR}	$\Delta R/R$
100X	5.19	-1.64E-04	-8.51E-04	3.70E-04	1.92E-03
	10.7	-5.20E-05	-5.56E-04	2.54E-04	2.72E-03
	22.5	5.36E-05	7.50E-05	1.39E-04	4.30E-03
Average C_{TR} (slope)		5.35E-05		1.45E-04	

From the results, the C_{TR} values for the S-D region measured using objective lens of 5X, 20X and 100X are 1.47E-04 K^{-1}, 1.60E-04 K^{-1} and 1.45E-04 K^{-1}, respectively. The GaAs gate has a C_{TR} value of 5.35E-05. It is noted that the gate length is 0.25 µm. Due to insufficient spatial resolution of objective lens of 5X and 20X, objective lens of 100X with spatial resolution of 0.15 µm was used to measure the C_{TR} value.

From these measurements, it is noted that the objective lens used has some influence on the C_{TR} value. Therefore, it is important to perform the C_{TR} characterization and thermoreflectance measurement with the same objective lens.

c. Measurement of Thermoreflectance Coefficient of GaN

In this section, the C_{TR} value for the GaN gate will be measured. The field of views of a die consisting of GaN transistors obtained using objective lens of 20X and 100X are shown in Fig. 6.7. A yellow line is drawn along the GaN gate to indicate its location more clearly. A white illumination light source has been used to measure the C_{TR} value of the GaN gate.

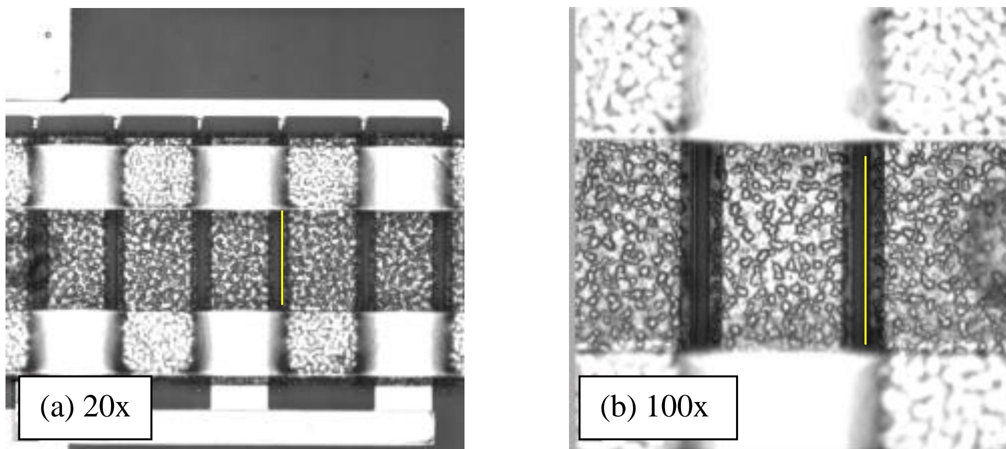
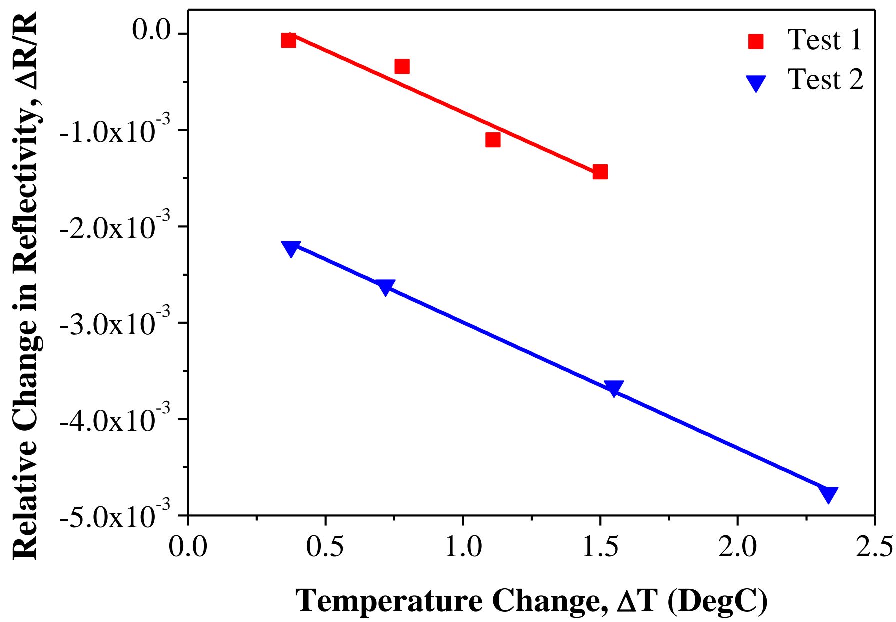
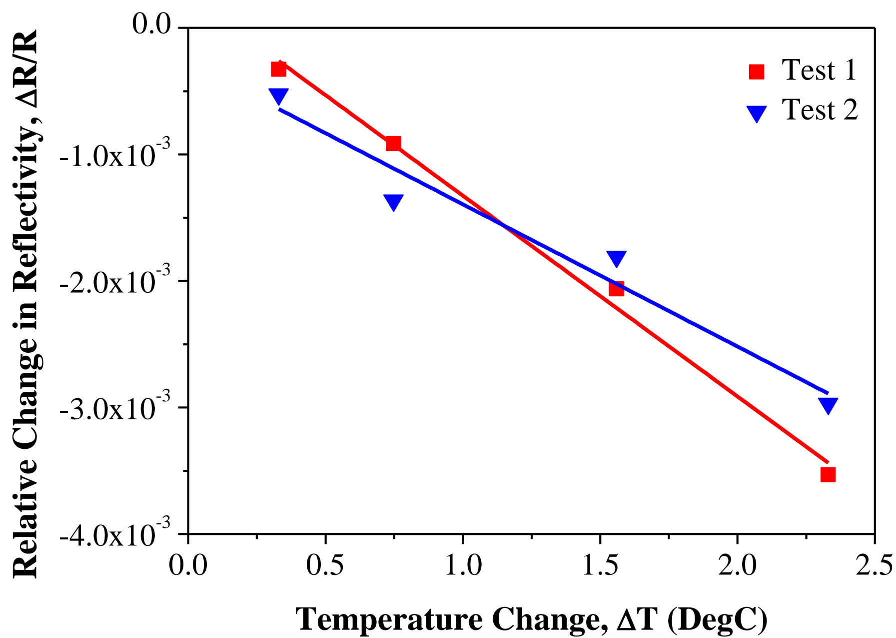


Fig. 6.7. Field of view of the GaN sample obtained using (a) a 20X objective lens and (b) a 100X objective lens.



(a)



(b)

Fig. 6.8. A plot of $\Delta R/R$ versus ΔT obtained using a white illuminating light source with (a) a 20X and (b) a 100X objective lens

The relative change in the reflectivity, $\Delta R/R$, in response to the change in temperature, ΔT, obtained using 20X and 100X objectives are plotted in Fig.

6.8(a) and Fig. 6.8(b), respectively. A linear fit has been made for each set of measured data where the slope corresponds to the C_{TR} value. The results are summarized in Table 6.4 and Table 6.5.

From the results, the measured C_{TR} values on the gate using 20X and 100X lenses are approximately 1.30E-3 K^{-1} and 1.36E-3 K^{-1}, respectively. Again, it is noted that the objective lens used has some influence on the C_{TR} value.

Table 6.4. Tabulated C_{TR} values for GaN sample measured using a 20X objective lens with a white illuminating light source

Objective Lens	Test 1			Test 2	
	ΔT	C_{TR}	$\Delta R/R$	C_{TR}	$\Delta R/R$
20X	0.366	-1.93E-04	-7.06E-05	-5.90E-03	-2.21E-03
	0.779	-4.36E-04	-3.40E-04	-3.63E-03	-2.61E-03
	1.11	-9.94E-04	-1.10E-03	-	-
	1.50	-9.56E-04	-1.43E-03	-2.36E-03	-3.66E-03
	2.33	-	-	-2.05E-03	-4.77E-03
Average C_{TR} (slope)		-1.29E-3		-1.31E-3	

Table 6.5. Tabulated C_{TR} values for GaN sample measured using a 100X objective lens with a white illuminating light source

Objective Lens	Test 1			Test 2	
	ΔT	C_{TR}	$\Delta R/R$	C_{TR}	$\Delta R/R$
100X	0.330	-9.97E-04	-3.29E-04	-1.59E-03	-5.25E-04
	0.748	-1.22E-03	-9.16E-04	-1.82E-03	-1.36E-03
	1.56	-1.32E-03	-2.06E-03	-1.16E-03	-1.81E-03
	2.33	-1.52E-03	-3.53E-03	-1.07E-03	-2.97E-03
Average C_{TR} (slope)		-1.59E-3		-1.12E-3	

d. Challenges in C_{TR} Characterization

During the C_{TR} characterization process, there are several factors that need to be considered:

1. Objective lens

The objective lens used has some influence on the C_{TR} value. Therefore, it is important to perform the characterization and temperature measurements on the device under test with the same objective lens.

Besides the variation in the C_{TR} values measured, the choice of objective lens also affects the amount of light intensity illuminating the sample surface. At higher magnification, the light intensity illuminating on the sample surface is reduced. The signal to noise ratio (SNR) decreases when the region of interest is poorly illuminated.

Although higher magnification level will provide better spatial resolution, any small vertical movement due to thermal expansion or contraction of the sample can cause defocusing of image. On the other hand, such issues are less significant at lower magnification levels.

2. Choice of illuminating light source

The choice of illuminating light source affects the amount of optical fringe type interference patterns formed. These fringes affect the accuracy of the C_{TR} value measured and also the thermoreflectance measurements. As shown in Fig. 6.9, images obtained using an LED source of wavelength 530nm have optical fringe type interference distinctly observed around the edges. On the

other hand, the optical fringe type interference patterns were significantly reduced when a white illuminating light source was used (Fig. 6.10).

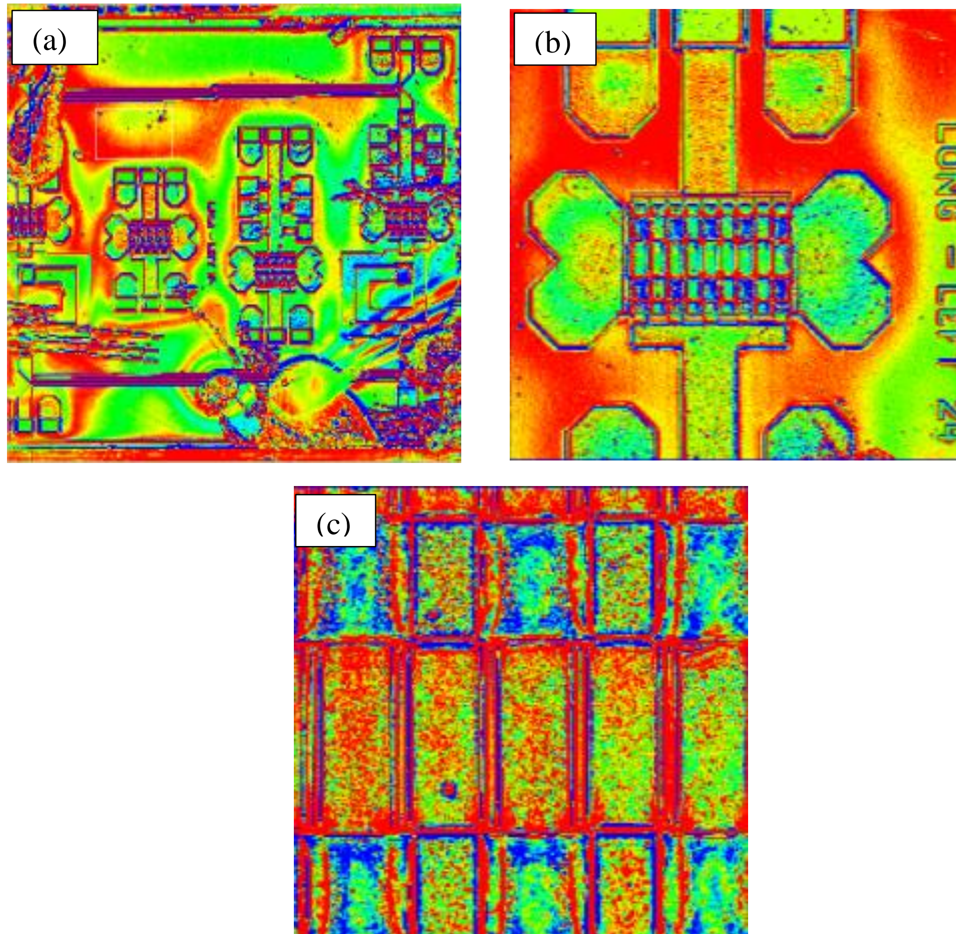


Fig. 6.9. Optical fringe type interference observed when a 530nm illuminating light source was used with (a) 5X, (b) 20X and (c) 100X objective lens

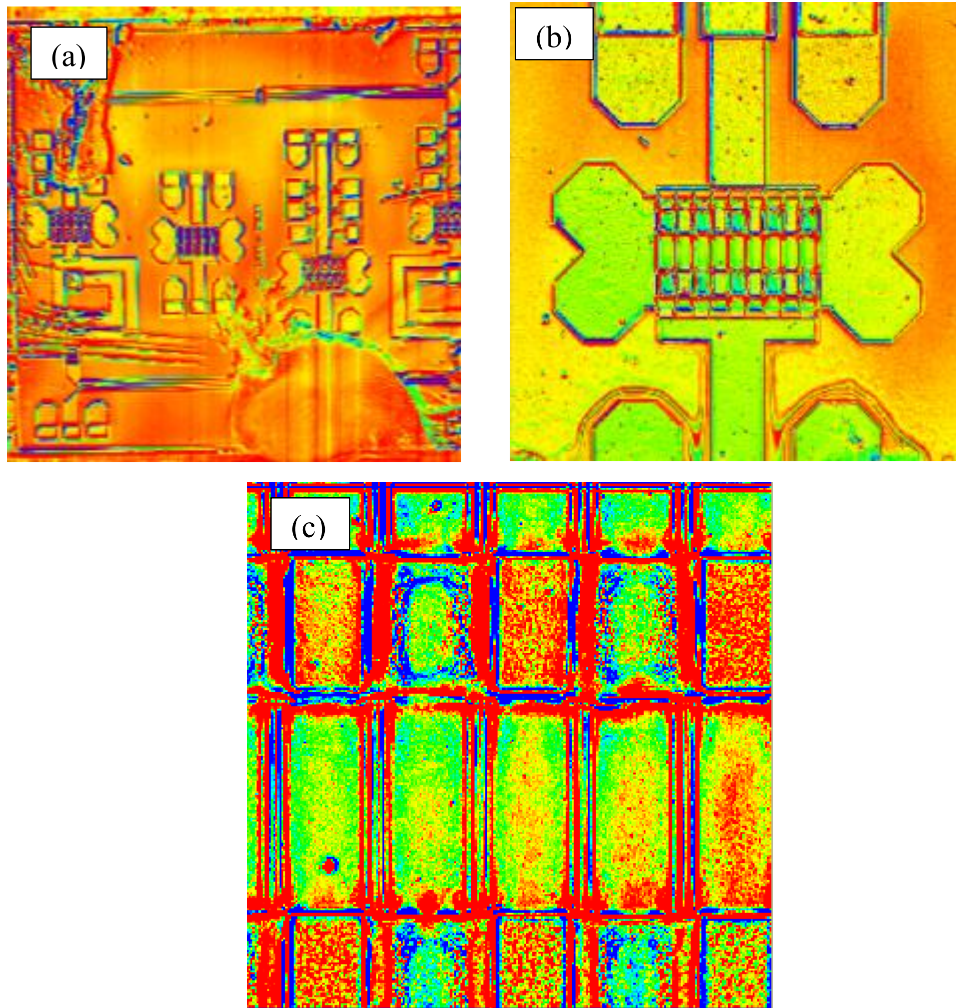


Fig. 6.10. Reduced optical fringe type interference is observed when a white illuminating light source is used with (a) 5X, (b) 20X and (c) 100X objective lens

3. Thermal expansion and contraction of Thermoelectric Module (TEM) and sample during C_{TR} characterization

The heating and cooling of the TEM often result in shifting of the sample due to thermal expansion and contraction of both the TEM and the sample under study. Significant movement in the sample will lead to inaccurate C_{TR} measured as pixel to pixel matching is required during cumulative averaging of the measured $\Delta R/R$.

Non-uniform heating of the TEM will also result in inaccuracy in the measured C_{TR} value. Thermoreflectance measurements are performed with normal light incidence. During uniform heating, the incident light onto the sample surface will be reflected and measured by the CCD camera via the objective lens (Fig. 6.11 (a)). On the other hand, when non-uniform heating of sample is present, some of the reflected light is not captured by the CCD camera (Fig. 6.11(b)). As a result, there is ambiguity on the measured C_{TR} values as different C_{TR} value may be measured across the sample surface.

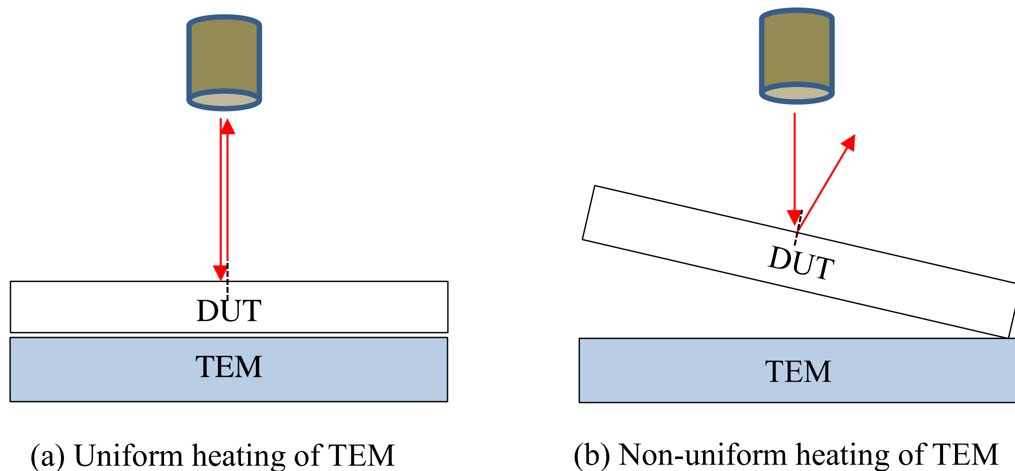


Fig. 6.11. (a) Uniform and (b) Non-uniform heat of TEM

To reduce the effect of the thermal expansion, one can reduce the change in the sample temperature to help minimize shifting of the sample due to thermal expansion.

4. Levelling of the sample

For all material characterization and temperature measurements, it is important to ensure that the sample is levelled horizontally as shown in Fig. 6.11(a). An

unlevelled sample placed on the TEM will result in similar issues faced when there is non-uniform heating of the sample.

5. Thermocouple

A thermocouple is used to measure the change in the sample surface temperature during C_{TR} characterization. The tip of the thermocouple should be in proper contact with the sample surface. Imperfect contact between the thermocouple junction and the sample surface could lead to errors in the measured surface temperature which in turn lead to inaccuracy in the C_{TR} value obtained.

6. Thermal time constant for heating the sample

Sufficient time should be given to allow the sample under test to be uniformly heated up to a steady state temperature before measurement of its reflectivity. This can be achieved by observing the temperature change measured by the thermocouple.

7. Size of the sample

The use of a smaller sample (e.g. 1 cm x 1 cm to 1 mm x 1 mm) for C_{TR} characterization will help to reduce the time required for achieving uniform heating of the sample. It will also help to reduce the problem caused by non-uniform thermal expansion and contraction of the sample during the C_{TR} characterization process.

6.2.3. Experimental Set-up for Thermal Characterization of PA MMICs

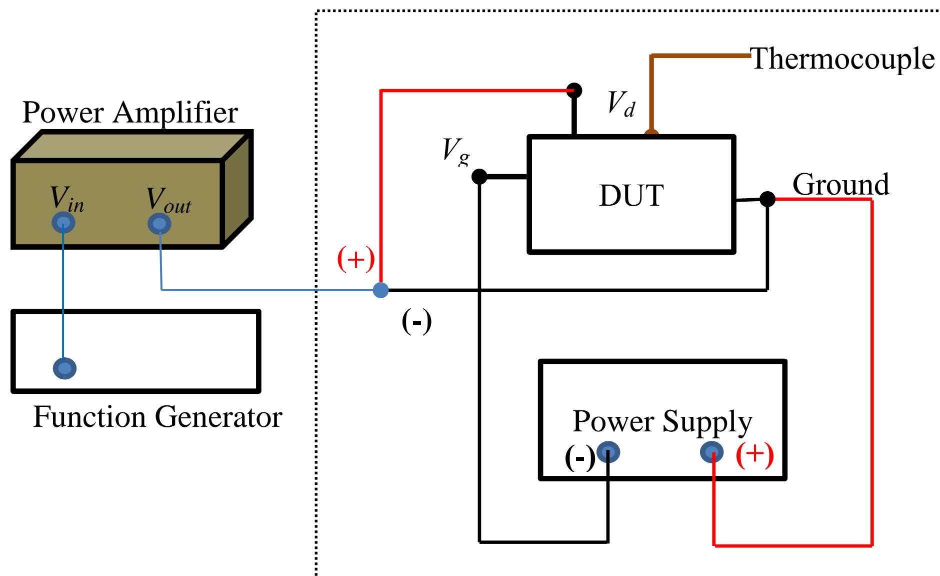


Fig. 6.12. Schematic diagram of the experimental set-up for thermal characterization of PA MMICs

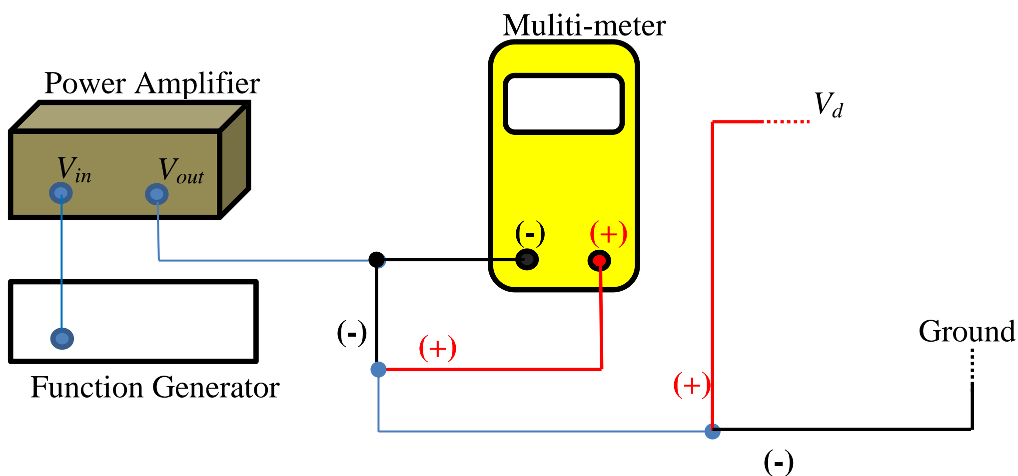


Fig. 6.13. Connect the multi-meter in series to the V_{out} to measure the drain current, I_d

The experimental set-up for thermal characterization of PA MMICs is shown in Fig. 6.12 and Fig. 6.13. In Fig. 6.12, a power amplifier is used to provide sufficient voltage supply to the device under test (DUT). The function generator is connected to the V_{in} of the power amplifier for lock-in. The V_{out} of the power amplifier is connected to the drain of the device, where the positive terminal is connected to the drain (V_d) and the negative terminal to the ground.

A power supply is used to provide a steady output power to the gain, where the positive terminal is connected to the ground and the negative terminal is connected to the gain (V_g). The DUT is securely placed onto a thermal chuck using a high temperature thermal glue to maintain a constant temperature at the base of the DUT.

To determine the total power input into the device, it is necessary to measure the drain current (I_d) prior to the testing. To do so, a multi-meter, with an accuracy of 1.5% and a resolution of 0.001A, is connected in series to the V_{out} as shown in Fig. 6.13.

6.2.4. Thermoreflectance Timing for Thermal Characterization of PA MMICs

During temperature measurement, a thermal chuck was used to maintain a constant base temperature of the device under test, in this case 25°C. In addition, transient conditions as well as the employment of a lock-in technique was carried out. To do so, the following pulse timing graph was used (Fig. 6.14):

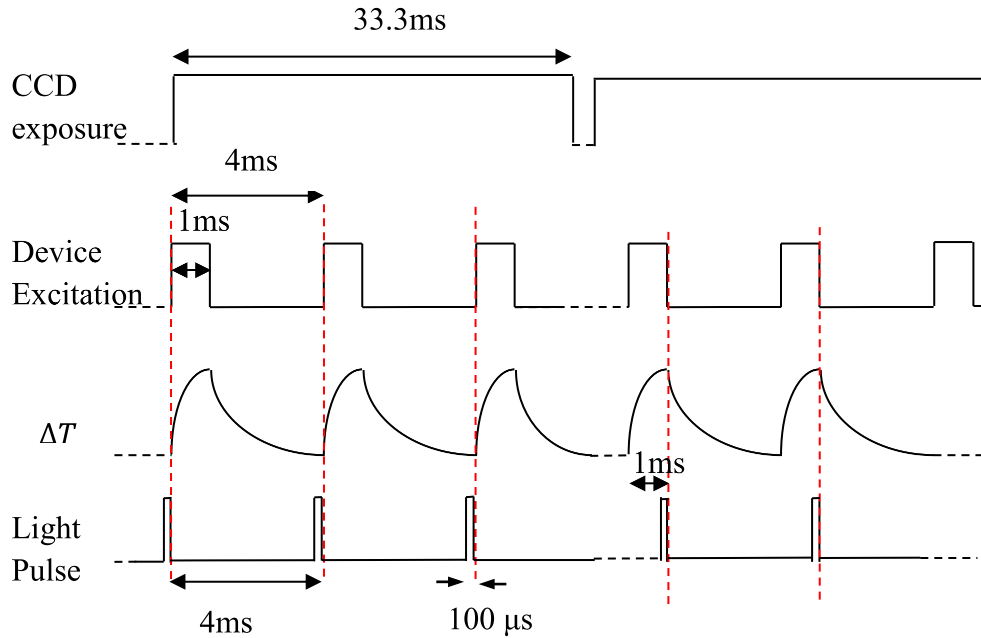


Fig. 6.14. Transient thermoreflectance timing graph

- The CCD camera exposure rate shown in Fig. 6.14 is set to 30Hz. As the camera runs at almost 100% duty cycle, the camera is on for 33.3ms and off for 0.1ms then on again.
- The device heating pulse is 1ms. For a device duty cycle of 25%, the device is on for 1ms and off for 3ms. The period for the whole cycle is 4ms.
- The temperature rise curve due to heating of the device is shown in Fig. 6.14.
- The maximum temperature rise of the device occurs between 0.9ms and 1ms of the device pulse. Therefore, an image delay of 1ms can be set to measure the maximum temperature rise.
- Pulses of light of 100 µs pulse width are strategically triggered at the start and end of the temperature rise curves as shown in Fig. 6.14 An image is captured each time a pulse of light is triggered. In this way, one set of

images of reflectance R_i at the beginning of the temperature rise, and another set of images of reflectance R_1 at the maximum temperature rise point are captured. The system then averages the sets of R_i and R_1 and the relative change in thermoreflectance, $(\Delta R/R_i)$, is computed as $(\Delta R/Ri) = (R_1-R_i)/R_i$ [3].

- ΔT of the device can then be obtained from (6.1).

6.2.5. Thermoreflectance Results for a GaAs PA MMICs

a. Description of the GaAs PA MMICs

In this section, the gate temperatures of a GaAs PA MMIC will be measured using TR thermography. The GaAs PA MMIC is a single stage power amplifier consisting of 20 transistors in two clusters (Fig. 6.15) and is capable of providing a total of 1W of output power. It has a gate length of 0.25 µm, gate width of 150 µm and gate pitch of 24 µm. The PA MMIC has been soldered onto a Cu-Mo carrier with Au-Sn solder and assembled into an aluminium jig (Fig. 6.16) for thermal characterization using TR thermography. The detailed dimensions, metal layer build-up and material properties of the GaAs PA MMIC have been described in Chapter 3.

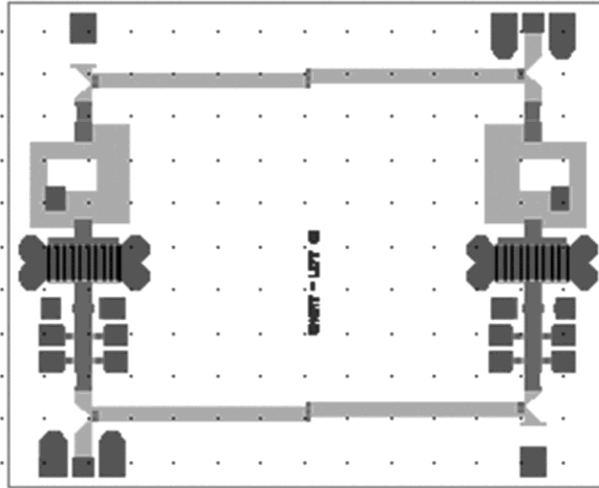


Fig. 6.15. Layout of the PA MMIC with two 10 x 150µm gates

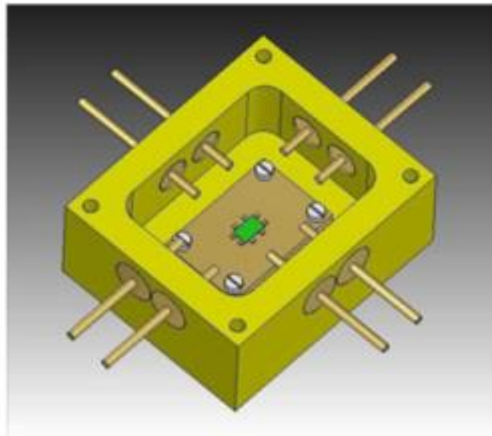


Fig. 6.16. Assembly of PA MMIC into the aluminium jig

b. Results

The base temperature of the test jig has been kept at a constant temperature of 25 ^{o}C. A 50X objective lens providing a spatial resolution of 0.232 µm has been used to measure the gate temperature. The maximum gate temperature of the transistor is measured along the gate indicated by a yellow line in Fig. 6.17. The C_{TR} value of the gate measured using a white illuminating light source is -1.64E-4 K^{-1}.

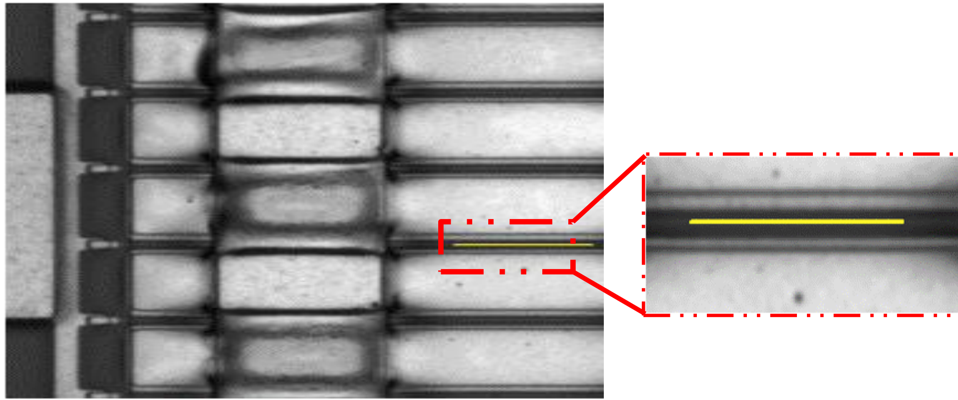
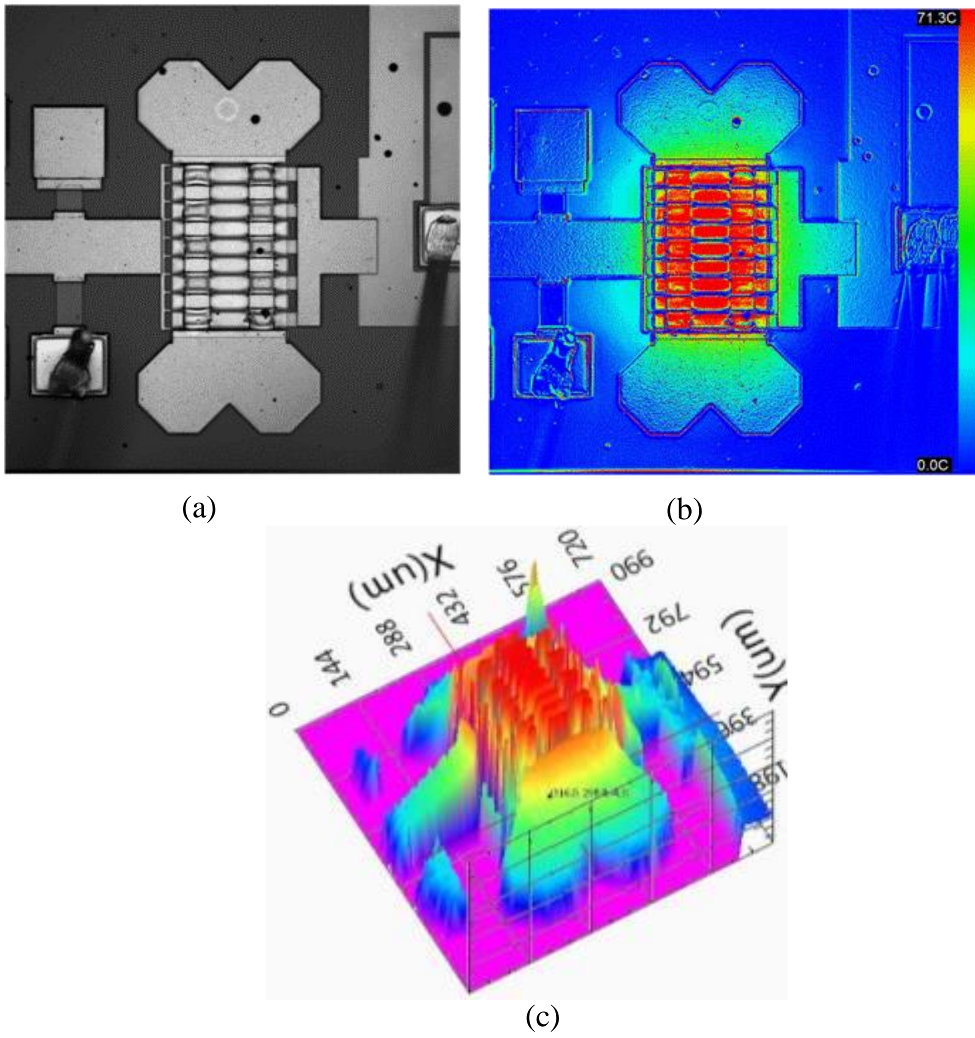


Fig. 6.17. The yellow line is drawn along the gate in this field of view obtained using a 50X objective lens

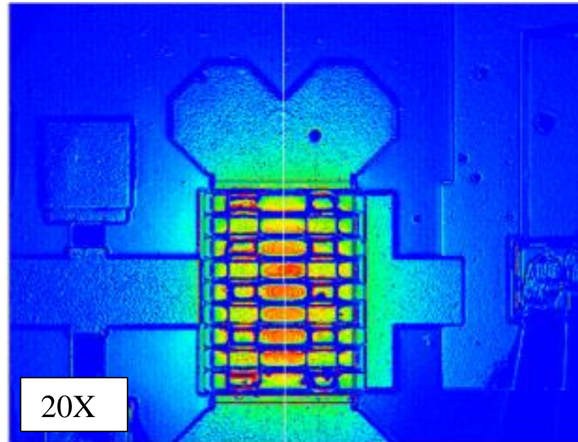
Fig. 6.18 shows a typical distribution of temperature (rises) over an MMIC during a TR measurement. It should be noted that since only the surfaces of the gates have been characterized for C_{TR}, only the temperature over the gates are correct while that over the other regions are not. The distribution of temperature (rises) along the line drawn across the gates obtained using a 20X objective lens is shown in Fig. 6.19. Each point in Fig. 6.19(b) represents a pixel of 0.58 μm. There appear to be some low temperatures measured in the regions between the gates. In reality, the temperature in the regions between the gates is unknown, since the C_{TR} value for these regions has not been characterized.



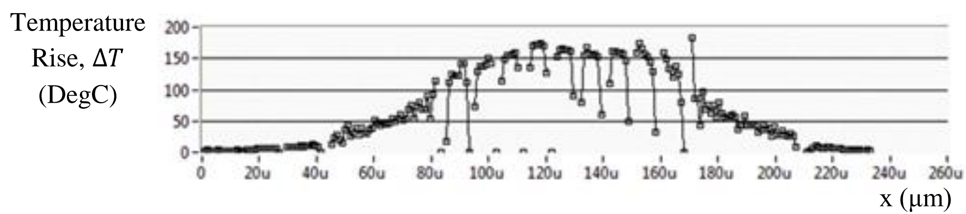
(a) (b)

(c)

Fig. 6.18. (a) Typical field of view obtained using a 20X objective lens. (b) 2-D temperature distribution on the MMIC during TR measurement. (c) 3-D temperature distribution on the MMIC during TR measurement



(a)



(b)

Fig. 6.19. (a) A center line is drawn across the transistor and (b) the distribution of temperature rises, $\Delta \boldsymbol{T}$, is plotted

The distribution of temperature rises across the cluster of gates obtained using a 50X objective lens is shown in Fig. 6.20. In Fig. 6.20(a), a line is drawn across the gates and the distribution of temperature rises along the line is plotted in Fig. 6.20(b). Each point in Fig. 6.20(b) represents a pixel of 0.232 µm. The centre point corresponds to the measured gate temperature.

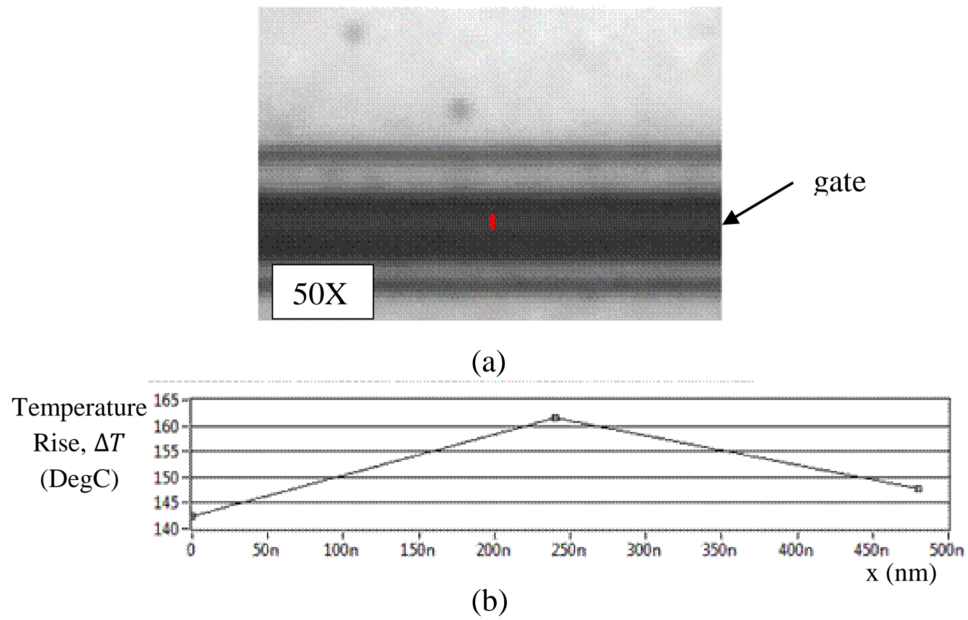


Fig. 6.20. (a) A line is drawn across the cross-section of the gate and (b) the distribution of temperature rises, ΔT, is plotted

The heat dissipation in the MMICs was increased and the values of the maximum gate temperature were measured and plotted in Fig. 6.21. Except for the first point which corresponds to zero power input, the maximum gate temperature increases linearly with the power input.

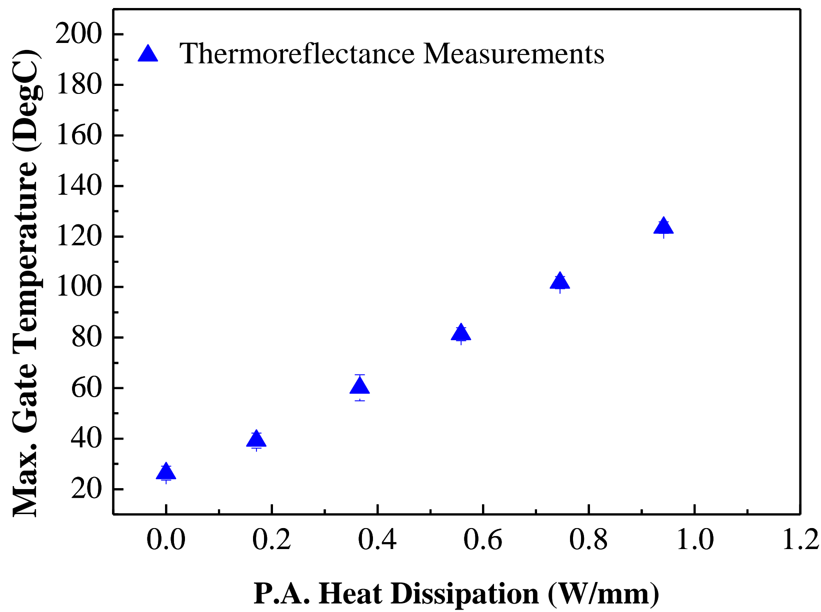


Fig. 6.21. Maximum gate temperatures of a GaAs PA MMIC measured using TR thermography

6.2.6. Thermoreflectance Results for the GaN PA MMICs

a. Description of the GaN PA MMICs

In this section, the measurement of the gate temperature of a GaN PA MMICs using TRT will be described. Similar to the GaAs PA MMICs, the test chip was soldered onto a Cu-Mo carrier with silver epoxy adhesive and assembled into an aluminium jig for thermal characterisation. The base temperature of the test jig has been kept at a constant temperature of 25 ^{o}C and at an elevated base temperature of 70 ^{o}C by a thermal chuck. The device under test has two transistors of gate length of 0.3 μm, gate width 150 μm and gate pitch of 48 μm.

b. Results

Using TRT, the gate temperatures have been measured using 20X and 100X objective lenses. The spatial resolutions resulting from using 20X and 100X objective lenses are 0.58 μm and 0.15 μm, respectively. The optical images obtained using TRT are shown in Fig. 6.22. The maximum gate temperature of the transistors was measured along the gate shown in Fig. 6.22. The C_{TR} value of the gate measured using a white illuminating light source is -1.3E-3 K^{-1}.

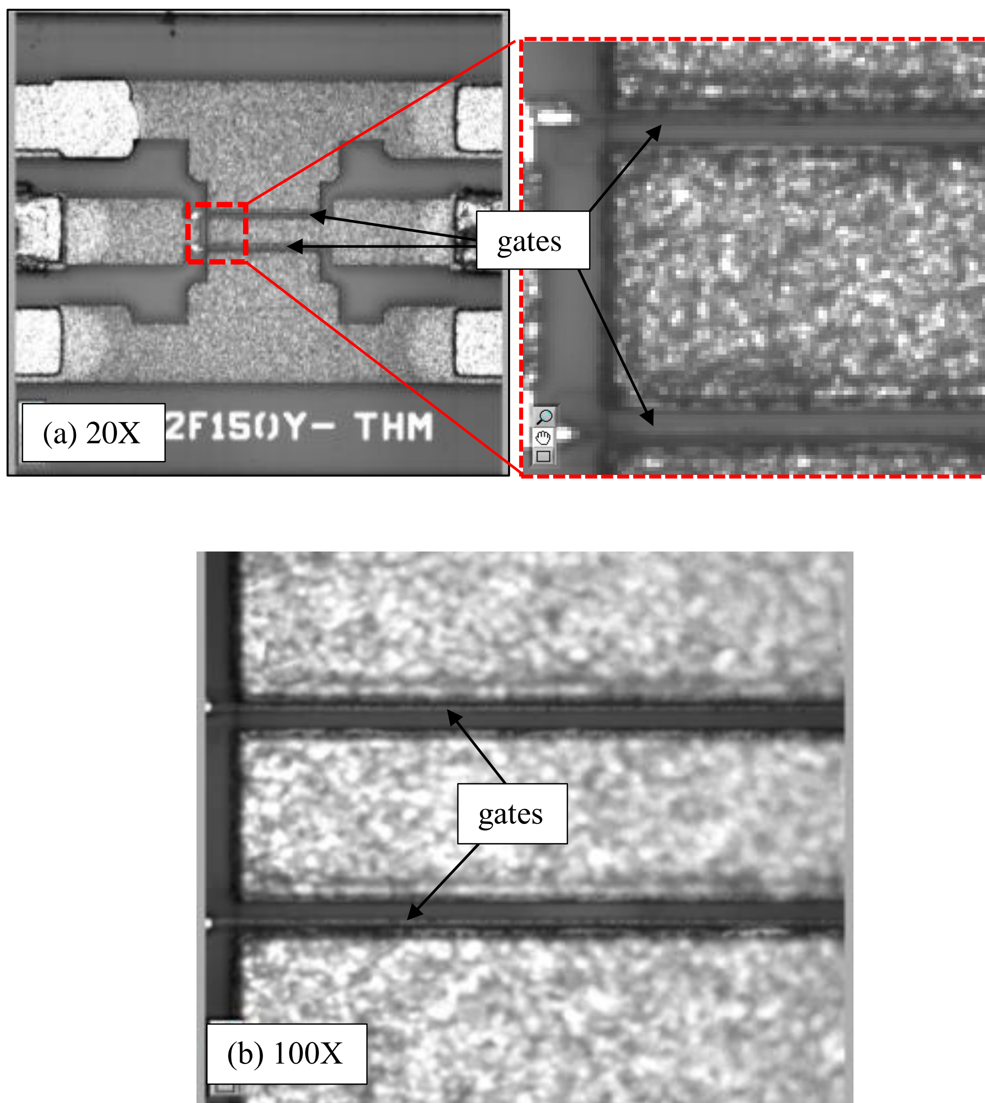


Fig. 6.22. Optical images obtained using (a) 20X and (b) 100X objective lens

The thermal image obtained using a 100X objective lens is shown in Fig. 6.23. As only the gates were characterized for its thermoreflectance coefficient value, the temperature in regions around the gates is actually unknown. Therefore in the thermal image on the right, the regions around the gates are colored dark blue so as to show clearly the heating of gates. The red color region indicated in the zoomed-in image on the right corresponds to the gate surface.

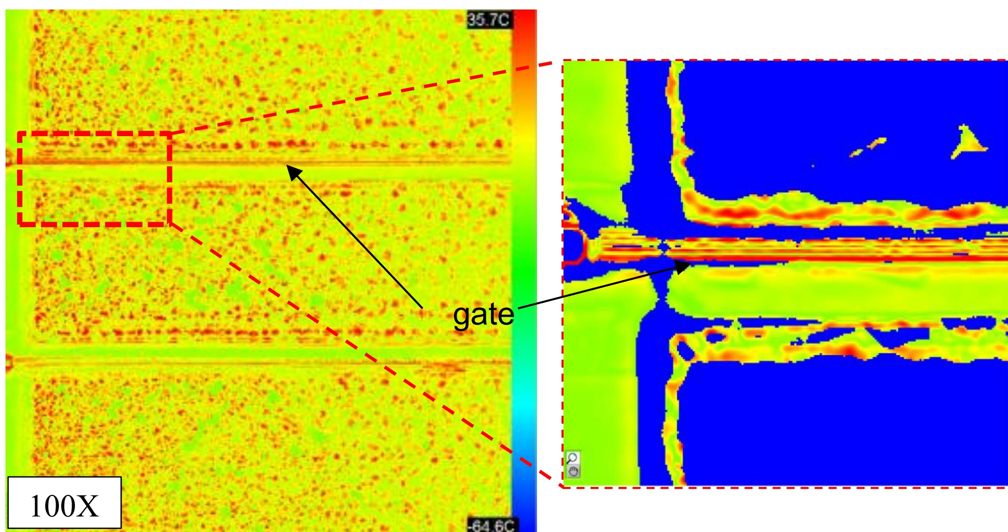


Fig. 6.23. Thermal image obtained using a 100X objective lens (LEFT). To show clearly the heating of the gates, the regions around the gates has been coloured blue (RIGHT).

The values of the maximum gate temperature measured using TRT at increasing heat dissipation levels and at aluminum jig base temperatures of 25°C and 70°C, are plotted in Fig. 6.24 and Fig. 6.25, respectively. As can be seen, the gate temperatures measured using a 20X objective lens are lower than temperatures measured using a 100X objective lens. The difference in the measured gate temperatures can be attributed to insufficient spatial resolution of 0.58 μm when using a 20X objective lens for temperature measurement of

gates with length of 0.3 µm. In this case, only about 0.3/0.58 or approximately half the pixel area is receiving reflected light from the gate surface and the rest from the region on both sides of the gate which value of C_{TR} have not been characterized. Thus, we should expect the temperature measured to be significantly in error. On the other hand, a 100X objective lens provide a spatial resolution of 0.15 µm which would allow the entire pixel to receive light reflected from the gate surface only.

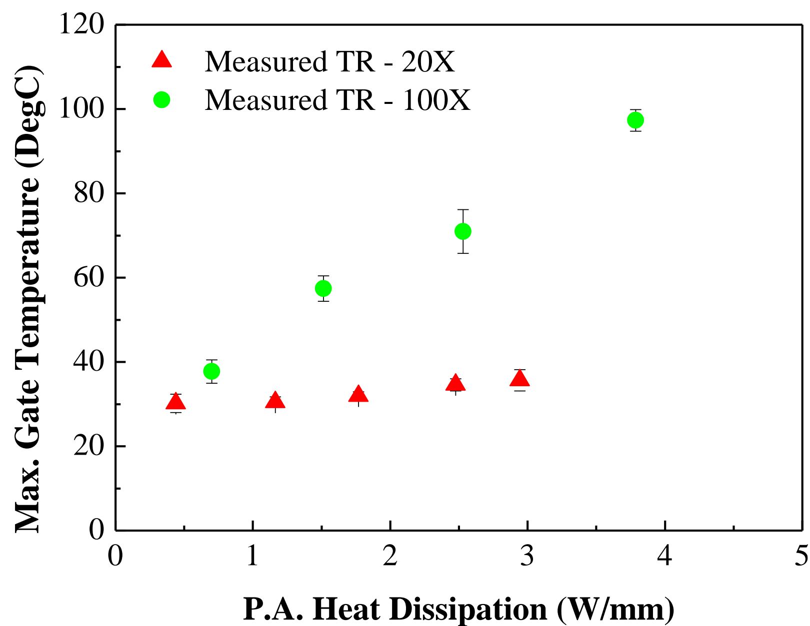


Fig. 6.24. Maximum gate temperatures of the GaN PA MMIC with aluminium jig base temperature of 25°C measured using TR thermography

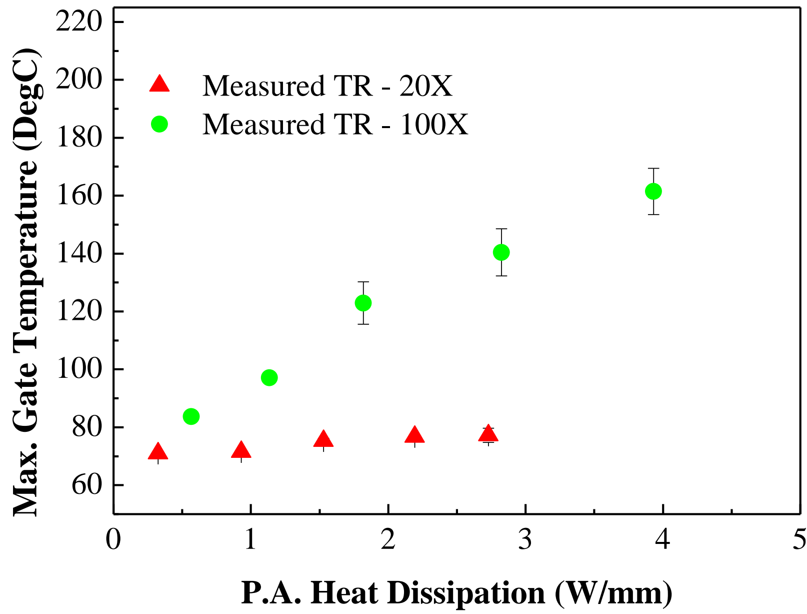


Fig. 6.25. Maximum gate temperatures of the GaN PA MMIC with aluminium jig base temperature of 70°C measured using TR thermography

6.3. Infrared Thermography

6.3.1. An Overview

The principle behind Infrared (IR) Thermography is related to the relationship between the surface temperature and the emitted electromagnetic radiation. The power emitted by a black body per unit area of the emitting surface can be defined as a function of wavelength λ and temperature T by Planck's law:

$$I(\lambda,T) = \frac{2hc^2}{\lambda^5}\frac{1}{e^{\frac{hv}{\lambda kT}}-1} \tag{6.2}$$

where h is the Planck's constant, c is the speed of light and k is the Boltzman's constant. Most Infrared detectors are designed to operate in the range of 2 μm to 10 μm wavelength band. This can be easily understood when looking at the plot of blackbody spectrum against wavelength in

Fig. 6.26. The highest amount of emitted radiance is found to fall in the range of 2 μm to 10 μm wavelength band. It is noted that the radiation intensity increases as temperature increases, with the radiation intensity peak tends towards shorter wavelength. This phenomenon has been quantified by Wien's Law:

$$(\lambda T)_{e_{\lambda=max}} = 2898\ \mu m.K \qquad (6.3)$$

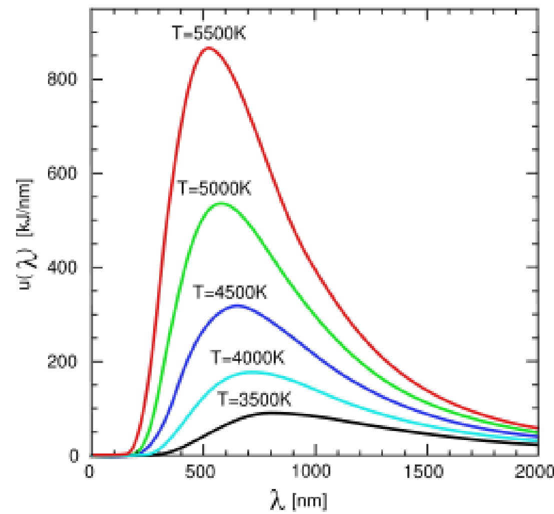


Fig. 6.26. A plot of the radiation intensity as a function of the wavelength and temperature for a black body ($\varepsilon = 1$)

For a mid-wave infrared camera, its operating wavelength band falls in the range of 2 μm to 5 μm. The amount of infrared radiation detected by infrared detectors is dependent on the material property, i.e. emissivity. It is defined as the ratio of the radiation emitted by a real body W_{RB}, compared to the radiation emitted by a blackbody W_{BB}, both at the same temperature and wavelength:

$$\varepsilon = \frac{W_{RB}}{W_{BB}} \qquad (6.4)$$

By Stefan-Boltzman's Law, the total radiated power for a real body can be expressed as:

$$W_{RB} = \varepsilon\sigma T^4 \tag{6.5}$$

where σ is the Stefan-Boltzmann constant. From this relation, the true temperature can then be computed, provided that the emissivity of surface is known.

In this work, a mid-wave (3 µm to 5 µm) CEDIP Infrared camera with a spatial resolution of 5 µm will be used. The radiance of an object is measured by the detector and is converted to temperature readings by the camera software.

6.3.2. Emissivity Calibration

a. Methodology

Due to presence of different metal layers on the surface, the emissivity value over the surface is not uniform. An emissivity map has to be measured prior to the measurement of the actual temperature distribution using an IR camera.

A commonly used technique to obtain emissivity of a surface is pixel by pixel emissivity correction [11]. Due to the presence of different materials on microcircuits, the emissivity across the surface varies. Therefore, it is more accurate to measure emissivity at each pixel location. This technique has been described as a double heat method in [12, 14, 67].

Integrating the Planck's law (6.2) over detector's sensitive wavelengths, the radiation R_{t1} emitted by a surface at some temperature $t_1{}^oC$ is given by:

$$R_{t1} = \varepsilon R_{b1} + R_o(1 - \varepsilon) \tag{6.6}$$

where R_{b1} is the radiation which would be produced by a black body at temperature t_1, ε is the surface emissivity, and R_o is the background radiation corresponding to room temperature. Similarly at a different temperature t_2, the radiation R_{t2} emitted by a surface at some temperature $t_2{}^oC$ is given by:

$$R_{t2} = \varepsilon R_{b2} + R_o(1 - \varepsilon) \tag{6.7}$$

Eliminating R_o from (6.6) and (6.7), the emissivity of the surface can be calculated by:

$$\varepsilon = \frac{(R_{t1} - R_{t2})}{(R_{b1} - R_{b2})} \tag{6.8}$$

Hence, by measuring the radiance of the unpowered device at two temperatures, we can calculate the emissivity of the sample to a high accuracy for each pixel of the image.

To create an emissivity map, the following steps were used:

- Attach a thermocouple at the base of the measured sample to monitor the change in the temperature.
- Heat up the sample to temperature t_1 (read from thermocouple). Capture the first image with the IR camera.
- Heat up the sample to a higher temperature t_2 (read from thermocouple). Capture the second image with the IR camera.
- An emissivity map is created using IR camera software.

It should be noted that the first temperature t_1 should be at least 5 degree C higher than the ambient temperature. This is to ensure that the IR camera is not measuring the radiance from the ambient, but the radiance from the heated sample. Also, it would be good to have a prior knowledge of the expected range of temperature that a powered device will reach, so that the expected measured temperature will fall within the range of temperature used for creating the emissivity.

b. Emissivity Measurement of GaAs and GaN PA MMICs

The emissivity maps of surfaces for both GaAs PA MMIC and GaN PA MMIC test chips were measured. The results are shown below:

i. GaAs Sample

Fig. 6.27 shows a typical emissivity map of the GaAs PA MMIC under study. The positions of the ten gates, spaced at 24μm apart can be clearly discerned from the line-scan that shows the emissivity distribution along a line drawn through the mid-width of the gates. The emissivity value at the gate has an average value of 0.25.

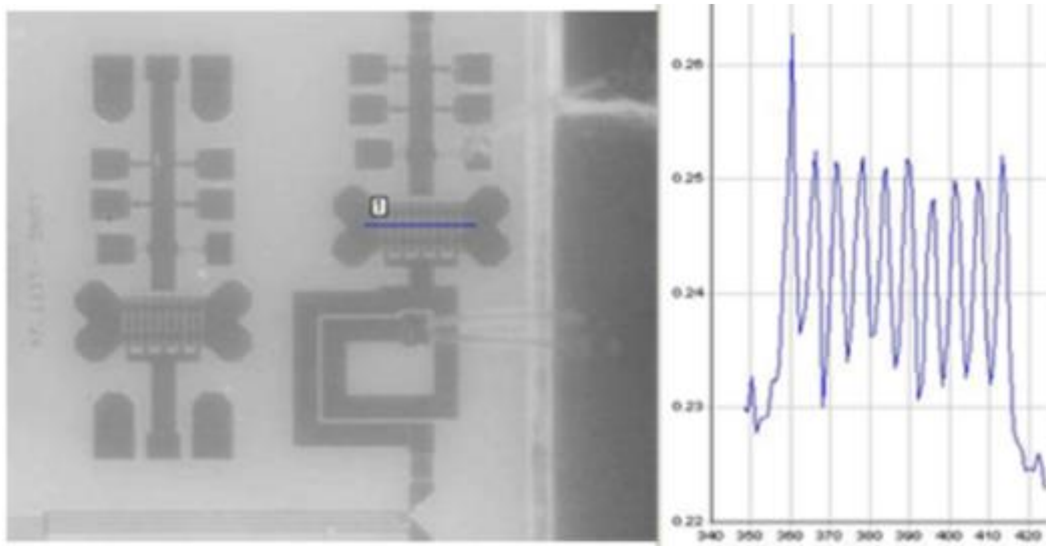


Fig. 6.27. Emissivity map of the DC biased GaAs PA MMIC.

ii. GaN Sample

A typical emissivity map of the GaN PA MMIC under study is shown in Fig. 6.28. The gates are spaced at 48 μm apart and can be clearly discerned from the line-scan that shows the emissivity distribution along a line drawn through the mid-width of the gates. The test chips consist of 2 gates. The emissivity value at the gates measured has an average value of 0.29.

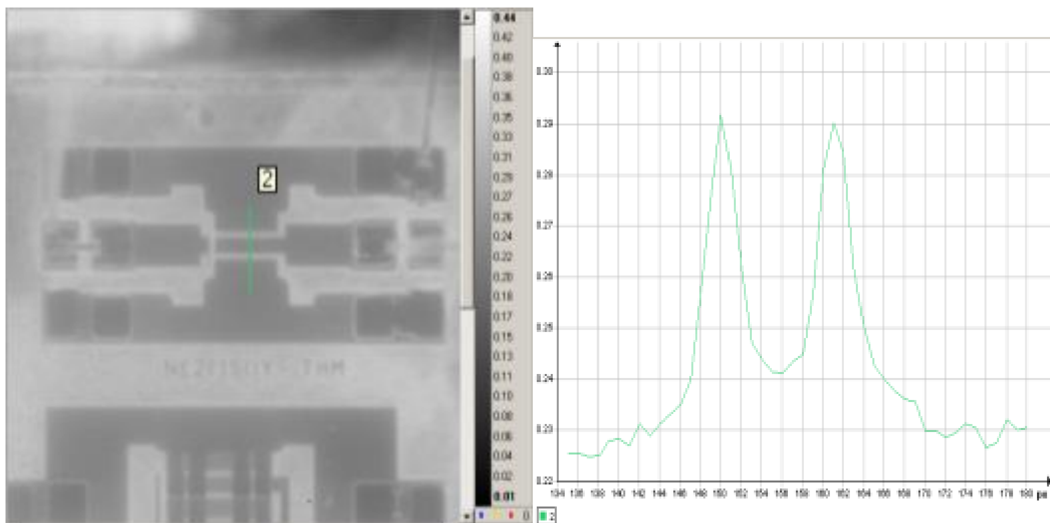


Fig. 6.28. Emissivity map of the DC biased GaN PA

c. Challenges in Emissivity Measurement

IR thermography allows for easy qualitative analysis. It gives a quick overview of where the defects or hot spots are in an electronic device. Similarly, it is also able to provide quantitative analysis, provided that the emissivity value of the measured surface is high. Unfortunately, the surfaces of most electronic devices have low emissivity values. To carry out quantitative analysis for low emissivity surfaces, emissivity correction has to be carried out. However, doing so does not guarantee that the measured temperature is the true temperature of the surface. This is because:

i. A low emissivity surface often implies that the surface is also highly reflective. The temperature of the detector (approximately 90K) may be reflected onto the measured surface. The measured temperature could actually be the temperature of the detector instead of the targeted area.

ii. The spatial resolution of the IR camera is 5µm while the measured gate length is 0.25 µm and 0.3 µm for GaAs and GaN PA MMIC, respectively. Insufficient spatial resolution of the IR camera results in an average temperature measured that is lower than the actual peak gate temperature.

iii. The device under test may become misaligned due to thermal expansion or contraction. Mechanical realignment has to be made for pixel matching during measurement of emissivity which may add on to the uncertainty.

6.3.3. Calibration of Infrared Camera using a Copper Block

The objective of this test is to investigate the accuracy of IR camera reading. This was done by measuring the surface temperature of a heated copper block from 30°C to 95°C and comparing it with the thermocouple attached to the top surface of the copper block. The experimental set-up is shown in Fig. 6.29.

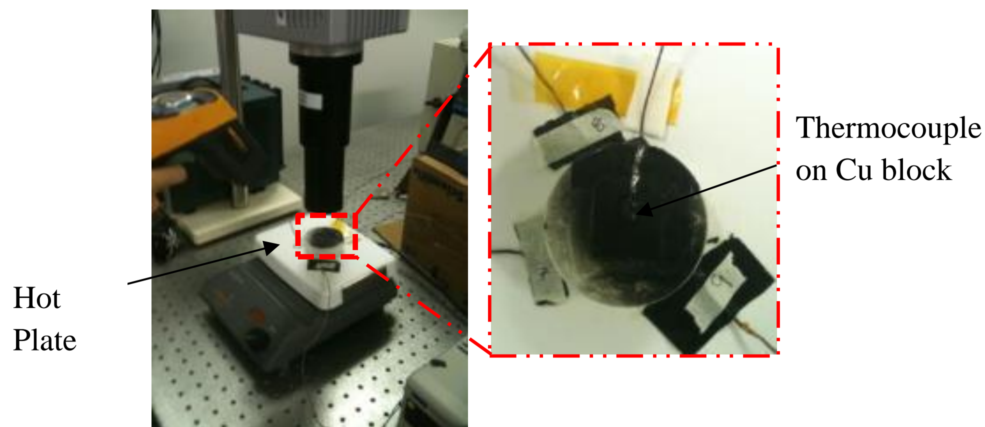


Fig. 6.29. Experimental set-up for calibration of Infrared camera

The copper block was sprayed with high emissivity paint. Two sprays had been administered at an interval of 10 minutes. Each spray was done by pressing the nozzle for only one second, releasing a 'burst' of paint. The paint created a black body surface with emissivity approximately equal to one. The copper block was placed on the hot plate for heating and under the objective lens for temperature measurement. A thermocouple was soldered onto the top surface of the copper block to measure the surface temperature. The thermocouple had earlier been calibrated against a master mercury-in-glass thermometer of accuracy 0.1 °C placed in a hot water bath (Fig. 6.30). The measured temperatures using the IR camera, and the thermocouple are plotted in Fig. 6.31.

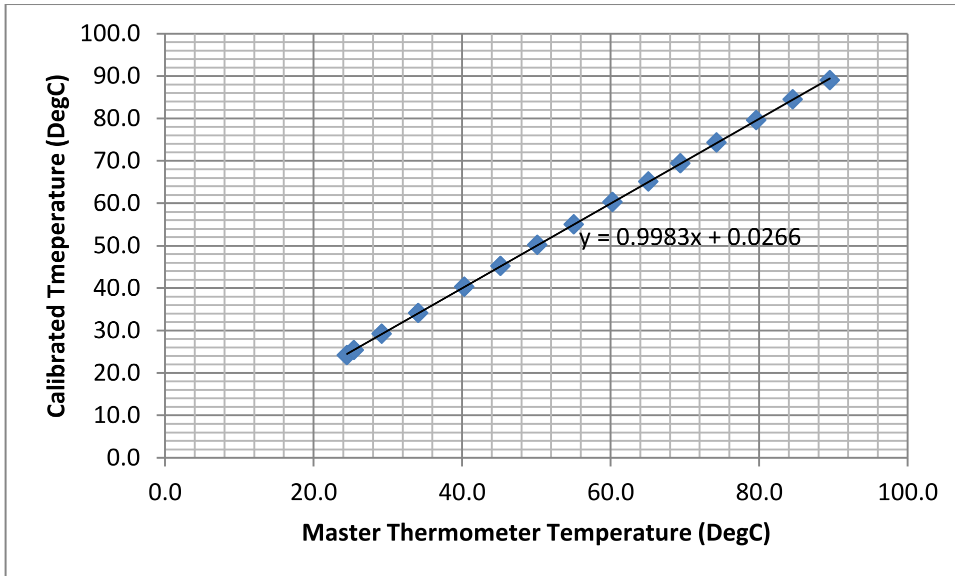


Fig. 6.30. Thermocouple calibration with respect to a master thermometer

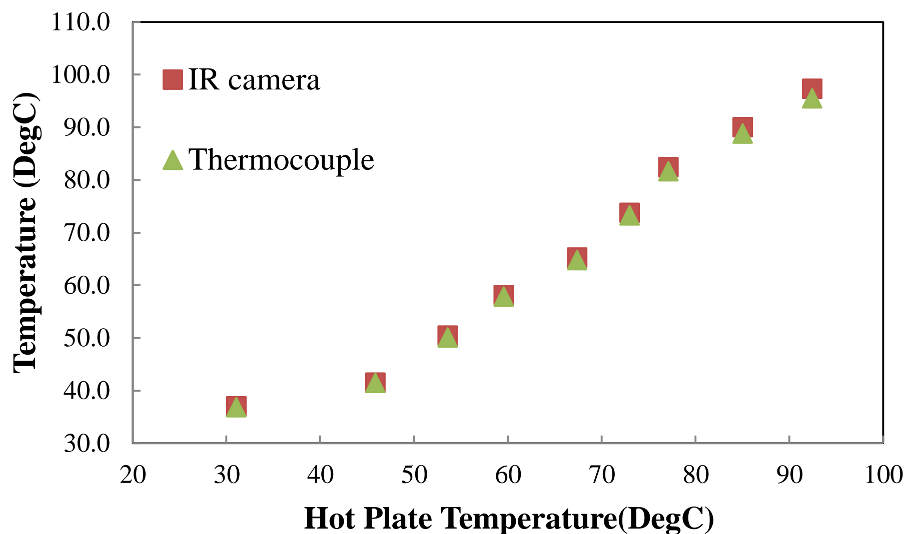


Fig. 6.31. Results for IR camera calibration test using a copper block.

As shown in Fig. 6.31, the temperature differences between the thermocouple readings versus the IR measured temperatures are very small. For temperature less than 70°C, the difference between measurements is in the range of 0.2^{o}C to 0.45^{o}C. For temperature greater than 70°C, the difference is in the range of 0.78^{o}C to 1.8^{o}C.

This calibration test has shown that the IR camera is able to provide accurate temperature measurement on a high emissivity surface with a maximum difference of 1.8°C at 95 °C or 1.9%.

6.3.4. Inferring Gate Temperature from IR Thermal Map

The spatial resolution of the IR camera used was 5 μm which is much larger than the 0.25 μm gate length of the MMIC device tested. Hence, the measured apparent temperature of a pixel of the thermal map is actually an average value, T_{avg}, of the temperature distribution over the pixel (Fig. 6.32). The peak gate temperature within a pixel can be inferred if the profile of the temperature distribution over the pixel is known.

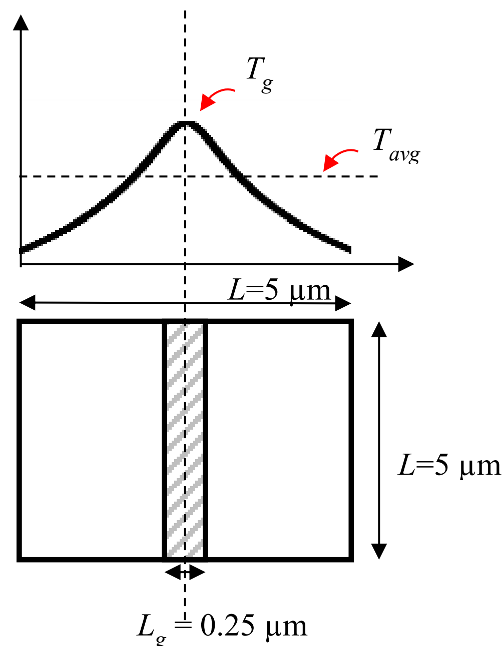


Fig. 6.32. Temperature profile across a gate within a pixel (5 μm x 5 μm)

a. Darwish's method

Darwish et. al. [10] had proposed a method for inferring the peak gate temperature from the temperature measured using IR thermography by reversing the spatial averaging inherent in IR microscopy. A constant highly localised heat source with gate length of L_g and gate width W_g on a substrate of thickness b was considered (Fig. 6.33). The substrate width, W_s, was assumed to be large enough that it has no effect on the temperature profile. A constant heat flux Q over the gate surface was assumed. All surfaces were assumed to be at adiabatic condition except for the bottom of the substrate which was assumed to be at a constant temperature. The substrate was assumed to have a constant thermal conductivity, k.

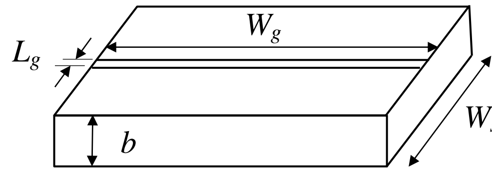


Fig. 6.33. A constant highly localised heat source of dimension Lg x Wg on a very large substrate of thickness b

To obtain the temperature profile due to a localised heat source on a substrate, Darwish et. al. had considered the thermal resistance from the gate to the base of the substrate by making an analogy to the heat transfer problem of a concentric cylinder between two infinite planes , such that:

$$\frac{T_g - T_o}{Q} = \frac{1}{\pi W_g k} \ln\left(\frac{8b}{\pi L_g}\right) \tag{6.9}$$

where T_g is the gate temperature and T_o is the substrate base temperature.

Similarly, the thermal resistance from the gate to a distance z away from the gate is expressed as:

$$\frac{T_g - T_z}{Q} = \frac{1}{\pi W_g k} \ln\left(\frac{8z}{\pi L_g}\right) \tag{6.10}$$

To obtain the temperature profile, $T(z)$, due to the localised heat source as a function of radial distance (away from the gate),

$$\frac{T_g - T_o}{Q} - \frac{T_g - T(z)}{Q} = \frac{1}{\pi W_g k} \ln\left(\frac{8b}{\pi L_g}\right) - \frac{1}{\pi W_g k} \ln\left(\frac{8z}{\pi L_g}\right) \tag{6.11}$$

$$\frac{T(z) - T_o}{Q} = \frac{1}{\pi W_g k} \ln\left(\frac{b}{z}\right) \tag{6.12}$$

Equation (6.12) was further simplified by assuming $T_o = 0$ and $Q = 1\text{W}$:

$$T(z) = \frac{1}{\pi W_g k} \ln\left(\frac{b}{z}\right) \tag{6.13}$$

To determine T_{avg} over a pixel, a circular pixel with radius r was considered:

$$T_{avg} = \frac{1}{Area}\left(T_J Area_B + \int_{A,C} T(x,y)dxdy\right)$$
$$T_{avg} = R_{IR} T_g \tag{6.14}$$

where T_g can be inferred easily from T_{avg} by the infrared averaging ratio, R_{IR}, since R_{IR} is a closed-form solution in terms of the pixel radius, gate length and thickness of the substrate.

Although the application of R_{IR} is a straightforward method, some inaccurate assumptions were made during the formulation of R_{IR}:

- The temperature at the substrate base was assumed to be constant. However, this is often not true for a packaged device that has been soldered onto a carrier.
- A single heat source was assumed to be present on the substrate. However in multi-finger devices, the neighbouring heat sources do contribute to the overall temperature profile.
- A surface heat flux had been assumed as the heat dissipation region in a FETs device. However in the actual application, the heat dissipation region takes place under the gate in the depletion region. Furthermore, it has been shown in section 4.4 that modelling of the heat dissipation region using a surface heat source will lead to a huge overestimation of the gate temperature.
- The heat flux, Q, over the gate surface was assumed to be equal to 1W.
- The thermal conductivity of the substrate was assumed to be constant, whereas the thermal conductivity of most semiconductor materials is strongly temperature dependent.

b. Present method

To obtain the profile of the temperature distribution over the pixel, it is proposed that the analytical solution (4.42) derived in Chapter 4 can be used to determine the temperature distribution due to multiple heat sources by applying the superposition technique.

To obtain the true gate temperature, T_g, from the pixel-averaged temperature, T_{avg}, measured by the IR camera (Fig. 6.32), an Infrared Correction Factor, CF_{IR}, is used where:

$$CF_{IR} = T_g/T_{avg} \tag{6.15}$$

T_g can be calculated by using (4.42) and T_{avg} in a pixel can be calculated from (6.16) below:

$$T_{avg} = \frac{1}{pixel\ area}\left[T_g \times 2 \times \frac{L}{2} \times L_g + 4r\int_{\frac{L_g}{2}}^{L/2} T dx\right] \tag{6.16}$$

This proposed method of inferring gate temperature from the measured apparent temperature resembles the actual situation of a FET much better than the method of Darwish et. al., due to the following reasons:

- In the present method, the heat dissipation region is considered to be under the gate which is more realistic.
- The actual temperature distribution at the substrate base can be more accurately determined by using (5.16) from Chapter 5.
- Temperature dependent thermal conductivity has been taken into account during the formulation of the analytical solution (4.42).
- Unlike the method of Darwish et. al. method where Q = 1W was assumed, in the present method, the actual amount of heat flux into the device can be taken into account (refer to equation (4.42)).

6.3.5. IR Measurements on a GaAs PA MMICs

In this section, the gate temperature of the GaAs PA MMICs described in section 6.2.4 will be measured using IRT. The experimental set-up will be described. As the resolution of the IR camera used was 5 µm which is much

larger than the 0.25 μm gate length of the MMIC device tested, an IR Correction Factor, CF_{IR}, will be used to infer the peak gate temperature from the measured apparent temperature.

a. Experimental Set-up for IR Thermography

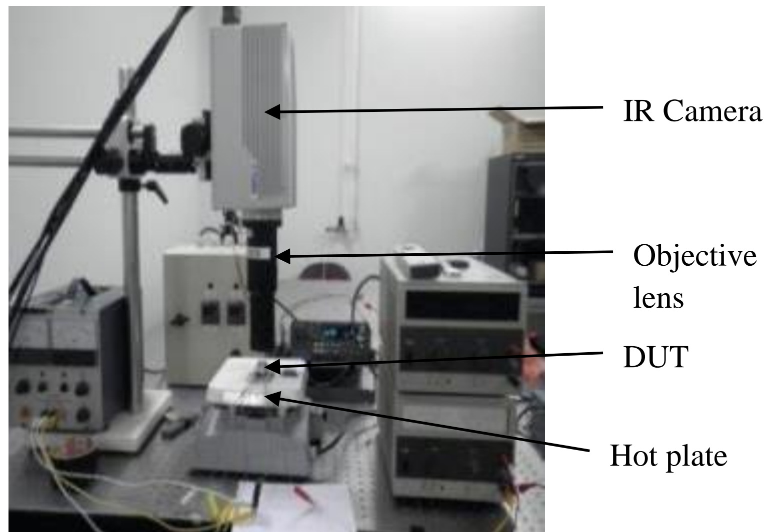


Fig. 6.34. Experimental set-up for IR thermography on a GaAs PA MMIC

The experimental set-up for measuring the gate temperature of a GaAs sample using IR thermography is shown in Fig. 6.34. The device is placed on a hot plate and under the objective lens. A thermocouple has been attached to the base of the jig to monitor its base temperature.

b. Results

Fig. 6.35 shows a typical "live" IR image of the PA MMIC after emissivity correction. The temperatures and positions of the ten gates can be discerned from the line-scan that shows the temperature distribution along a line drawn through the mid-width of the gates. The measured gate temperatures at

different heat dissipation levels before and after applying the Infrared Correction Factor, CF_{IR}, are plotted in Fig. 6.36.

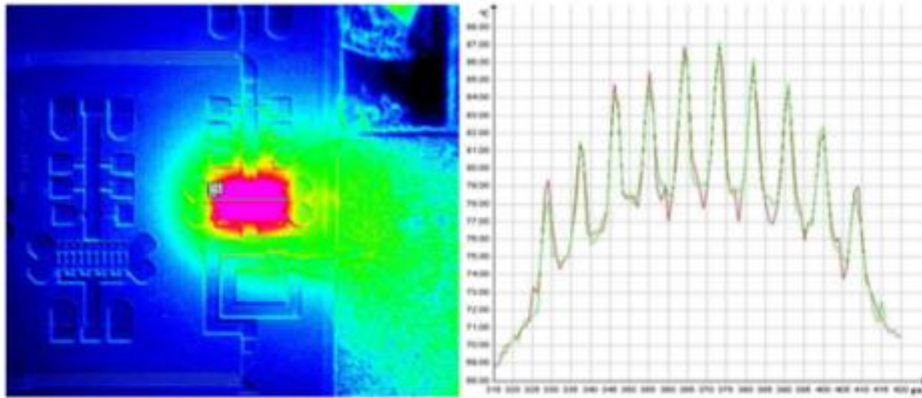


Fig. 6.35. “Live” IR image of the DC biased GaAs PA MMIC.

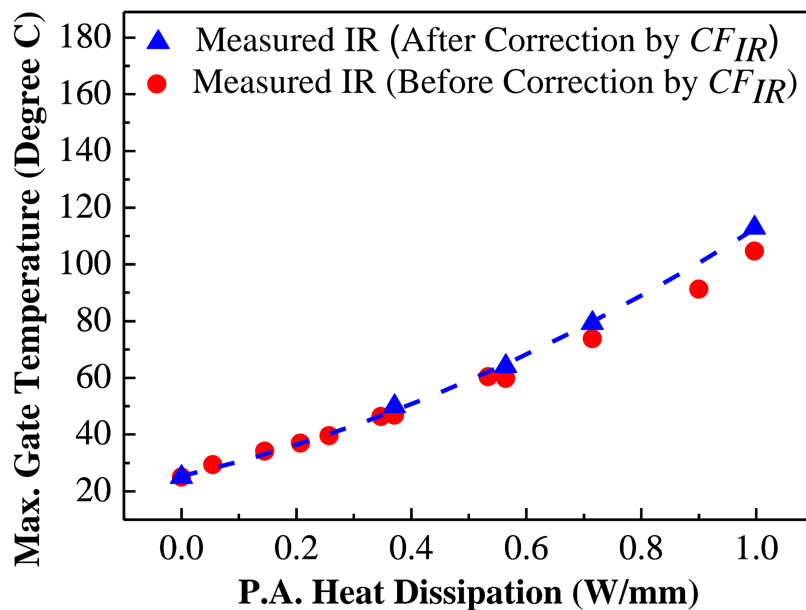


Fig. 6.36. Measured gate temperatures obtained using IRT before and after applying CF_{IR} for the GaAs PA MMIC

6.3.6. IR Measurements on a GaN PA MMIC

In this section, the gate temperature of the GaN PA MMIC described in section 6.2.5 will be measured using IRT.

a. Experimental Set-up

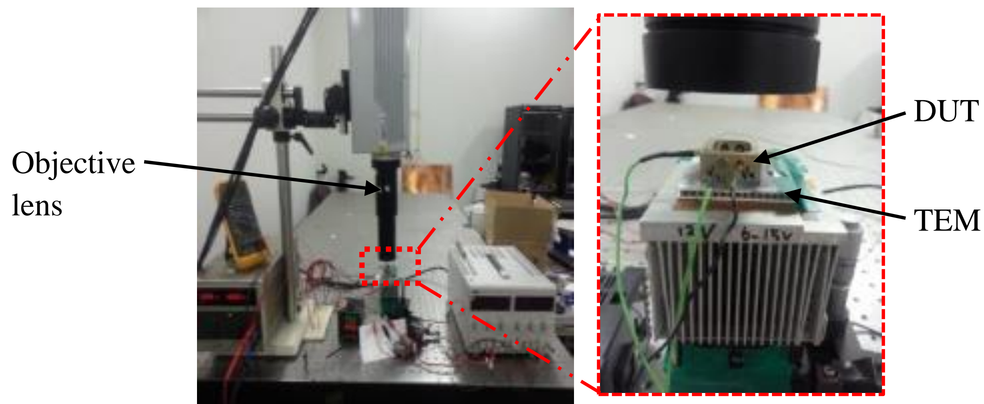


Fig. 6.37. Experimental set-up for IR thermography on a GaN PA MMIC

The experimental set-up for measuring the gate temperatures of a GaN PA MMIC using IRT is shown in Fig. 6.37. The device under test (DUT) is placed under the objective lens and on a thermoelectric module (TEM) to maintain a constant base temperature of 25 ^{o}C and later at an elevated base temperature of 70 ^{o}C.

b. Results

Fig. 6.38 shows a typical "live" IR image of the PA MMIC after emissivity correction. In Fig. 6.39, temperatures and positions of the two gates can be discerned from the line-scan that shows the temperature distribution along a line drawn through the mid-width of the gates.

Fig. 6.38. “Live” IR image of the DC biased GaN PA MMIC.

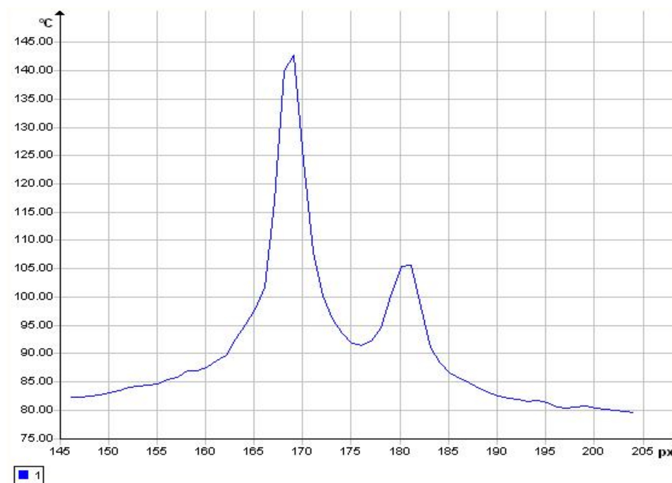


Fig. 6.39. Temperature distribution along a scan line across the gates

The measured gate temperatures at different heat dissipation level with aluminium jig base temperature at 25 ^{o}C and 70 ^{o}C are plotted in Fig. 6.40 and Fig. 6.41, respectively.

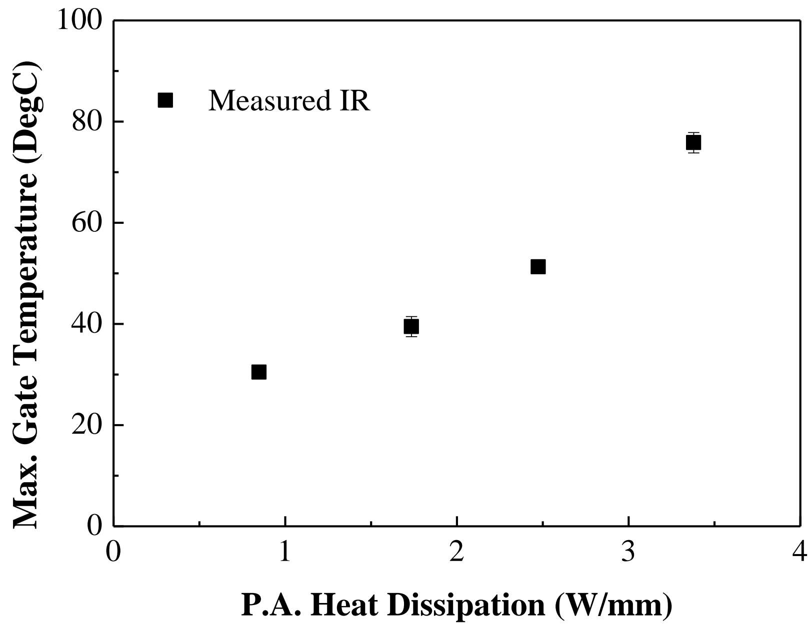


Fig. 6.40. Maximum gate temperatures for the GaN PA MMIC measured using IRT with aluminium jig base temperature of 25 ^{o}C

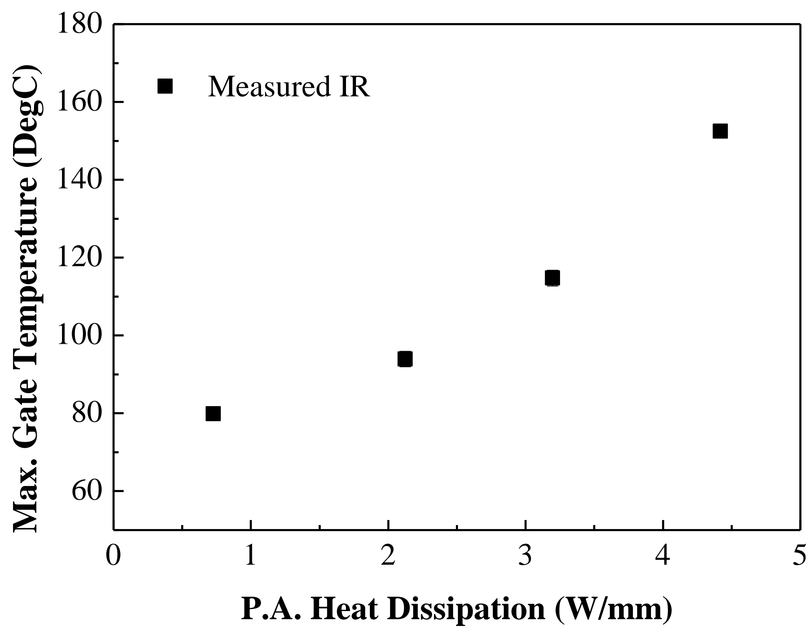


Fig. 6.41. Maximum gate temperatures for the GaN PA MMIC measured using IRT with aluminium jig base temperature of 70 ^{o}C

6.4. Comparison of Measured Gate Temperatures of GaAs PA MMIC with Numerical and Analytical Results

In this section, the measured gate temperatures obtained using IRT and TRT for GaAs PA MMIC are compared with (i) the calculated temperatures using both detailed and simplified thermal FE models presented in Chapter 3 and (ii) the calculated temperatures using the present analytical method presented in Chapter 5. As IRT and TRT measure the gate temperature on the surface and not the junction temperature, the gate temperatures calculated using the numerical and analytical methods are used for comparison with the measured gate temperatures in the sections below.

a. Comparison between TR results, Numerical and Analytical Solutions

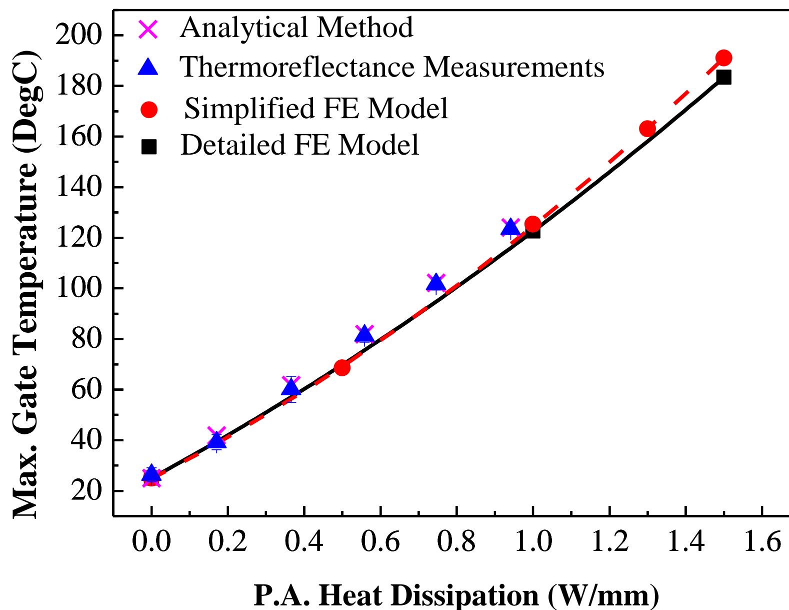


Fig. 6.42. Numerical and TR thermography measured temperatures for the PA MMIC

In Fig. 6.42, the maximum gate temperatures measured using TRT have been plotted and compared with the FE solutions calculated from the thermal models as well as the gate temperatures calculated using the present analytical method. As shown in Fig. 6.42, the analytical solutions agree very well with the FE solutions and TR temperature measurements, thus confirming the accuracy of the present analytical method and the TR measurements.

b. Comparison between IR results, Numerical and Analytical Solutions

In this section, the measured gate temperatures obtained using IRT are compared with both numerical and analytical solutions. To do so, the Infrared Correction Factor (CF_{IR}) is applied on the measured temperature to obtain the true gate temperature:

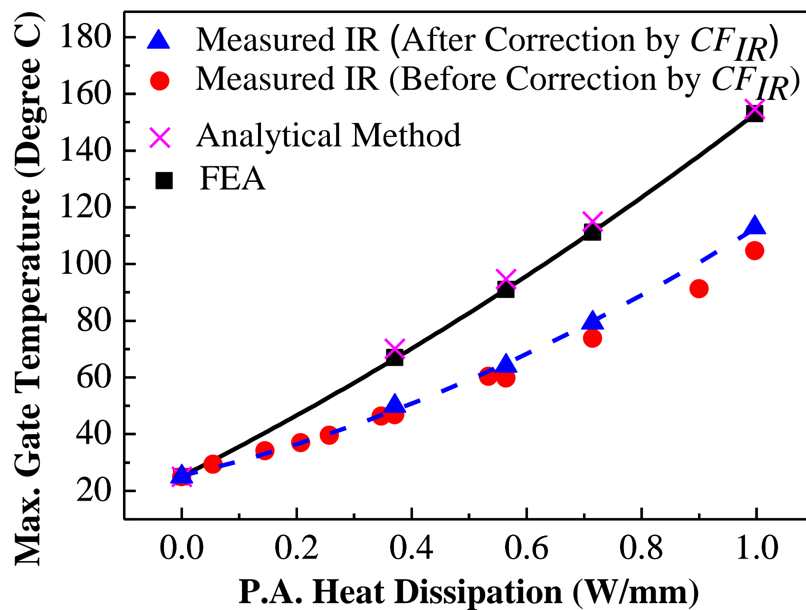


Fig. 6.43. Numerical and corrected IR measured temperatures for the PA MMIC

In Fig. 6.43, temperatures measured using IRT and "corrected" using CF_{IR} to obtain the true operating gate temperatures are plotted. The analytical solutions and FE solutions obtained from the simplified model are also plotted in Fig. 6.43 for comparison. Due to heating from the transistors, the base temperature of the aluminium jig increased as power input increased. The temperature of the base of the aluminium jig measured using a thermocouple was used as a boundary condition in the FEA.

As shown in Fig. 6.43, the analytical solutions correlate well with the FE solutions but most of the IR-measured temperatures are much lower than those calculated using FEA. The differences between the FEA and measured IR results could be due to several factors, including:

- Errors in the IR temperature measurements may have caused some discrepancy. For example, reflected background radiation from surrounding parts of the structure may have introduced errors into the measurements.
- Low emissivity surfaces pose a challenge to obtaining accurate IR measurements. The emissivity values of the gate region are less than 0.3.
- The 5μm spatial resolution of the IR camera is actually very good as the theoretical limit for IRT is about 3μm. However, for this application, the resolution is still too coarse for the 0.25μm-size gates of the PA MMIC. Although applying the CF_{IR} correction factor should help here, it is not good enough.

6.5. Comparison of Measured Gate Temperatures of GaN PA MMIC with Numerical Results

In this section, the measured gate temperatures obtained using IRT and TRT for the GaN PA MMIC are compared with the calculated gate temperatures using FEA. The detailed thermal model of the GaN PA MMIC has the same material stack-up configuration as shown in Fig. 3.9. A simplified model, consisting of only the gate, GaN substrate, Si substrate, die attach, carrier, aluminium jig and interface thermal resistances, was also modelled for comparison with the measured gate temperatures.

Values of the maximum gate temperature measured using TRT at each heat dissipation level and aluminum jig base temperature of 25°C and 70°C are plotted in Fig. 6.44 and Fig. 6.45, respectively. Similarly, the measured gate temperatures obtained using IRT and FE solutions are also plotted in Fig. 6.44 and Fig. 6.45 for comparison.

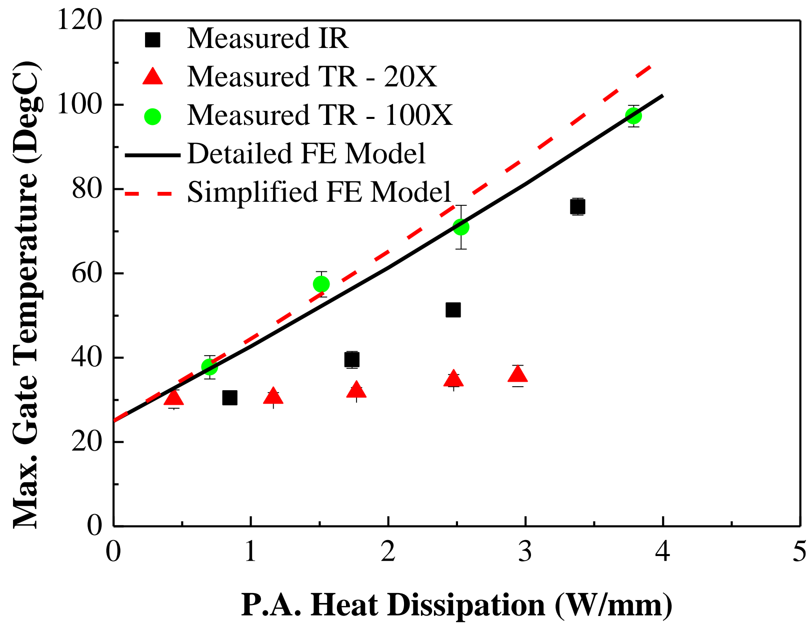


Fig. 6.44. Comparison of maximum gate temperatures for the PA MMIC with aluminium jig base temperature of 25°C measured using TRT and IRT with those calculated using FEA

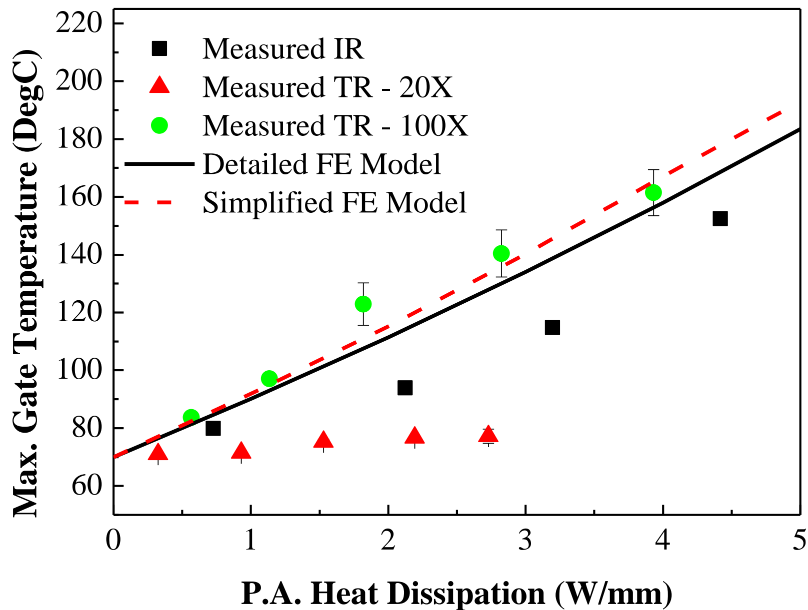


Fig. 6.45. Comparison of maximum gate temperatures for the PA MMIC with aluminium jig base temperature of 70°C measured using TRT and IRT with those calculated using FEA

From Fig. 6.44 and Fig. 6.45, it can be seen clearly that the measured temperatures using TRT with sufficient spatial resolution correlate well with the FEA results. On the other hand, measured temperatures obtained using TRT with a 20X objective lens (spatial resolution 0.58 μm) and IRT (spatial resolution 5 μm) are much lower than those calculated using FEA. This study has demonstrated the importance of having sufficient spatial resolution for accurate temperature measurements. The discrepancy between the IR measurements and the FEA results can be further attributed to the presence of low emissivity surfaces of less than 0.3 on the device.

6.6. Conclusion

In this Chapter, Infrared (IRT) and Thermoreflectance thermography (TRT) have been used to measure the peak gate temperature of both GaAs and GaN power amplifier (PA) MMICs device. An overview of the principle and the methodology for both characterization techniques has been presented. In addition, the challenges faced when using either technique to measure the gate temperature have also been discussed.

IRT has been the most common technique used for direct and non-invasive temperature measurement. The technique used for temperature measurement has been well established in the literature. As most semiconductor devices have reflective surfaces, emissivity correction is required to obtain an accurate thermal mapping. However, IRT has insufficient spatial resolution for temperature measurement on submicron size gate. In addition, any presence of sample movement will lead to inaccuracy in the measured temperature due to the mismatch of pixels.

On the other hand, TRT is a better technique for measuring temperature on reflective surfaces present in most semiconductor devices. It has sufficient spatial resolution for measuring temperature of submicron size gates. However due to its weak magnitude of the thermoreflectance coefficient, there is a challenge in obtaining high quality thermal images. As a result, a lock-in technique has to be used in order to obtain a high signal-to-noise ratio.

Both IRT and TRT have been used to measure the gate temperatures of a PA MMIC. The maximum gate temperatures obtained from FEA correlate well with those measured using thermoreflecance thermography. Due to insufficient spatial resolution, measured temperatures using IRT were "corrected" using an Infrared Correction Factor CF_{IR} and compared with results obtained using the simplified FEA model. The numerical and "corrected" measurement results show large discrepancies which could be attributed to errors in IR measurements due to reflections and the low emissivity of PA MMIC surfaces.

CHAPTER 7

THERMAL CHARACTERIZATION OF LIGHT EMITTING DIODES

7.1. Introduction

The first visible light emitting diode (LED) was created in 1962. These LEDs were red and were used primarily in decorative, display, signalling and signage applications due to its low luminous efficiency. Since then, the luminous efficiencies of LEDs have improved over the years with the development of high performance device structures such as GaN LED technology. It has exceeded the performance of conventional light sources such as incandescent and fluorescent [68, 69]. In addition, it requires lower energy consumption and maintenance [70]. Thus, the high luminous efficiencies of high power LEDs are making them an attractive option for general lighting applications. If solid-state lighting is able to replace all existing lights, it will help customers to save $115 billion by 2025 and a 10% reduction in greenhouse emission gases [71].

Despite its various advantages such as longer lifetime, energy saving, vivid colors, compact profile and reduced maintenance [72], there are still many challenges ahead for using LEDs in terms of thermal issues and cost competiveness. The increasing demand for higher performance LEDs has spurred the need for improving brightness of LEDs through driving higher current into it. However, this does not increase the optical output power significantly and causes self-heating in the device [68, 73-75]. This leads to an increase in the junction temperature of LEDs which in turn leads to

degradation in the LED optical performance in the form of a spectrum shift. The degradation of the plastic lens due to high temperature reached by the devices further degrades the luminous flux [76-80]. In addition, the phosphor material in the encapsulant undergoes browning. Extended exposure of LED devices to high junction temperatures will ultimately lead to catastrophic failure in the device due to localized heating [81].

Therefore, the efficiency and reliability of high-brightness LEDs strongly depend on the effectiveness of the thermal management of LEDs as the junction temperature of LEDs is the prime driver for effective operation.

Over the years, various techniques have been used to measure the junction temperature of LEDs including the forward voltage method, wave length shift method, liquid crystal thermography, infrared thermography (IRT) and thermoreflectance thermography (TRT). TRT is a potentially great technique for measuring LED junction temperature since the encapsulation layer is usually transparent to the TR measurement wavelength. However, to date, it has only been used for characterizing laser diodes [82] and no work has yet been done on using TRT to characterize the junction temperature of a packaged LED in the visible range.

There have also been attempts to characterize the junction-to-ambient thermal resistance of LED packages, similar to that of IC packages. In an IC package, the measured thermal resistance is a parameter which is inherent to the package. When the thermal resistance of an IC package is known, its junction temperature can be calculated under any operating condition. Likewise for an LED package, its junction temperature can be calculated once the junction-to-

ambient thermal resistance is known. Unfortunately, unlike the case of IC packages, not all of the electrical power that is supplied to the LED is dissipated as heat. It has been shown that about 85-95% of the LED power is typically dissipated as heat in the chip [83, 84] while the rest is converted into optical power. Therefore in order to accurately determine the thermal resistance of an LED package, the optical power of an LED needs to be measured and this is usually done using an integrating sphere.

In this chapter, work on thermal characterization of LEDs will be described with a special emphasis on the use of the latest novel technique called thermoreflectance thermography. Firstly, the principle of the LED will be described, followed by a literature review of the experimental methods that have been used to measure the junction temperature of LEDs. Next, the measurement of the junction temperature of some LEDs using various methods such as the forward voltage method, infrared thermography (IRT) and thermoreflectance thermography (TRT) will be described. After that, the measurement of the junction-to-ambient thermal resistance of LEDs using a transient thermal tester (T3ster) will be described. Finally, an analytical solution for the LED junction temperature will be formulated based on the analytical method developed earlier in Chapter 4. To establish its accuracy, the calculated junction temperatures will be compared and validated with experimental results and numerical solutions.

7.2. Principle of the LED

An LED is a p-n junction diode, where the p-type semiconductor is doped with holes and the n-type semiconductor is doped with electrons. When a forward

voltage is applied across the diode, generation and recombination processes of electron-hole pairs take place [85, 86]. There are three different types of recombination processes:

7.2.1. Radiative Recombination

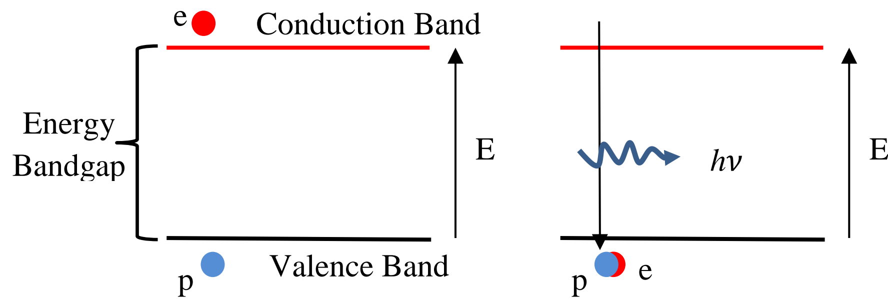


Fig. 7.1. Radiative recombination of an electron-hole pair

When a forward bias condition is applied across the diode, electrons in the conduction band recombine with holes in the valence band giving off energy as photons of light. The wavelength of the emitted light is dependent on the bandgap energy, E, of the materials forming the p-n junction, which is expressed as:

$$E = h\nu \quad (7.1)$$

where h is the Plank's Constant and ν is the frequency of the emitted photon.

7.2.2. Non-Radiative Recombination

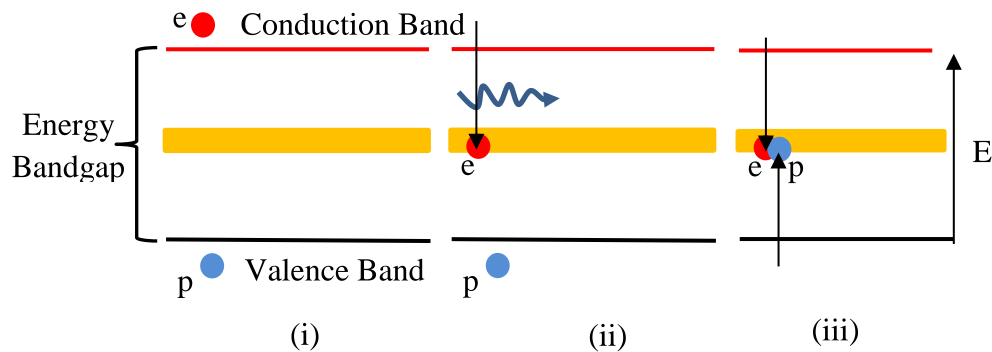


Fig. 7.2. (i) Extra energy level present in the forbidden region of the bandgap due to the presence of defects in the crystal lattice. (ii) Photons or phonons are released when electrons move to the recombination centers in the forbidden region. (iii) Carriers are annihilated when the holes move up to the same energy state before the electrons are excited back to the conduction band

Non-radiative recombination, also called Shockley-Read-Hall or SRH recombination, takes place when charge carriers recombine without releasing photons. Instead, the released energy is converted to vibrational energy of the lattice atoms, i.e. phonons. It is an unwanted process in optoelectronics that lowers the light generation and increases the heat loss. The cause for this process is due to the presence of defects in the crystal lattice. The defects produce several extra energy levels within the forbidden region of the bandgap and act as recombination centers. When electrons move to the recombination centers in the forbidden region, they may release either photons or phonons of lower energy levels. If a hole moves up to the same energy state before the electron is excited back to the conduction band, recombination takes place and the carrier is annihilated.

7.2.3. Auger Recombination

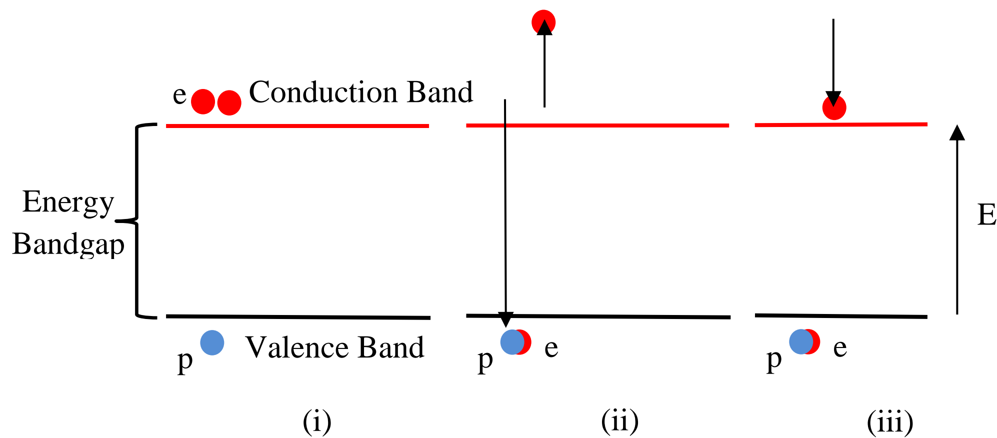


Fig. 7.3. (i) Electrons and holes are present in the conduction band and valence band, respectively. (ii) When an electron recombines with a hole, the energy released results in an increase of kinetic energy of another electron, causing it to move to a higher energy level. (iii) The kinetic energy is lost when the second electron relaxes back to the band edge

Three carriers are involved during this recombination process: an electron and a hole, and another electron in the conduction band. When an electron recombines on a band-to-band transition with a hole and gives off the resulting energy to another electron, the electron gets an increase in the kinetic energy which is lost when it relaxes to the band edge. This phenomenon may take place in the presence of high current that leads to high carrier concentration [87, 88]. This mechanism could be the reason why LEDs are less efficient at high drive currents and is still under research.

7.3. Structure of LEDs

The first LED lamp was a 5mm standard LED (Fig. 7.4) with its chip placed onto one of the leads of the lamp, typically in a small reflector cup [68]. A clear epoxy dome-shaped encapsulant is present to serve two purposes: (i) to

enhance the light extraction efficiency [85], and (ii) acts as a mechanical element of the package to hold the leads in position in the final device. The LED chip is connected to the other lead of the lamp by a thin Au wire. Such epoxy based LED is limited to an input power of less than 0.1W to maintain its operating temperature 10 to 20°C below the glass transition temperature (between 100 to 150°C) of the epoxy used. Exceeding the optimum operating temperature will induce stress on the thin Au wire and cause the LED to fail immediately. In addition, the thermal resistance of these LEDs is typically greater than 200°C/W, therefore limiting its application to low power devices only.

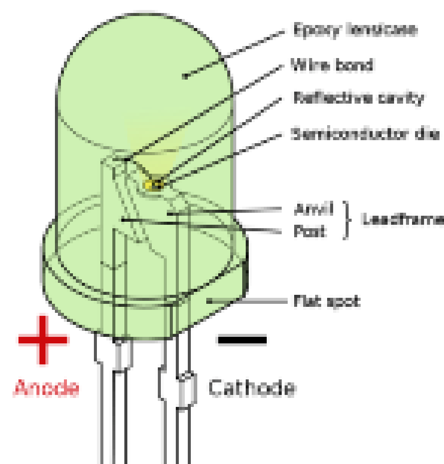


Fig. 7.4. Parts of an epoxy dome LED [89]

Therefore, the maximum thermal power that can be dissipated in the LED package is dependent on its overall thermal resistance and its operating junction temperature. A heat slug made of either aluminium or copper can be used to dissipate the heat from the LED chip to the printed circuit board (PCB), thus providing a low thermal resistance path for heat conduction and reducing the overall thermal resistance of an LED package to less than 5 K/W

[85, 90]. The typical structure of such LED packages is shown in Fig. 7.5. The LED chip is soldered to a silicon submount which is mounted on a heat slug. The cavity is filled with soft silicone and a plastic lens is attached to the package body to obtain the desired optical radiation pattern.

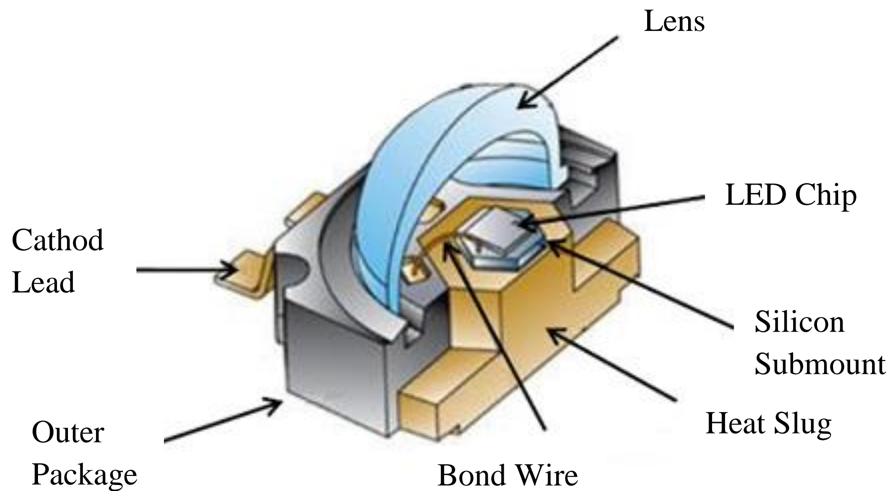


Fig. 7.5. Typical structure of high-power LED packaging [91]

The most common method to obtain a white LED is by coating a blue LED chip with yellow emitting phosphor such as Ce : YAG [92]. The phosphor coating causes a fraction of the shorter wavelength from the blue LED chip to undergo Stoke shift and is converted into longer wavelength, resulting in white light illuminating from the chip. The phosphor coating is either mixed with the epoxy or the silicone encapsulant that surrounds the LED chip or by employing a conformal phosphor coating over the LED chip [68, 92, 93].

Major improvement in LED packages, including advances in materials and materials growth and processing technologies, have increased the maximum allowable input power and thus provided a significant increase in the light output performance. Some potential applications of LEDs include general

illumination, mobile appliances, backlighting and automotive [94]. Therefore, there is a huge potential market for high-brightness LEDs as solid-state lighting fixtures with longer lifetimes require lesser maintenance as compared to conventional light fixtures.

7.4. Literature Review on LED Thermal Characterization Techniques

To ensure optimum operating junction temperature, thermal characterization of LED devices often plays an important role in designing an effective cooling solution. Several methods are available to measure the junction temperature of LED devices.

7.4.1. Forward Voltage Method

The forward voltage method [78, 84, 95-100] is a well-known technique for measuring the junction temperature of an LED. It is based on the linear dependence between the temperature rise in the p-n junction, ΔT, and the forward voltage drop, ΔV, across the p-n junction at some operating condition:

$$\Delta V = K\Delta T \tag{7.2}$$

where K refers to the temperature coefficient obtained from the linear relationship between the forward voltage drop and the junction temperature. During calibration, the LED is placed in a chamber where a controller will maintain the ambient temperature of the chamber at a desired value. Thermal equilibrium is ensured so that the LED’s junction temperature will be equal to the chamber temperature.

There are two methods that make use of forward voltage characteristics for temperature sensing:

a. Single Current Method (SCM)

In this method, a fixed current to the LED is supplied and the forward voltage is measured. When the junction temperature of the LED has reached the ambient temperature of the controlled environment, short pulses of current at a low duty cycle are supplied and the corresponding forward voltage is measured. Short pulses of current at a low duty cycle are used to minimise the occurrence of self-heating in the LED junction that will lead to a higher junction temperature than the temperature of the controlled environment. To obtain a relation between the LED forward voltage versus the junction temperature, the forward voltage measurement is repeated for a range of junction temperature controlled by external means. The relation between the forward voltage and the junction temperature is typically linear.

The SCM is theoretically the easiest method to implement. However, there are disadvantages associated with using SCM. The calibration has to be done at a pulsed-current equal to the actual current that the LED is going to be used at, and the calibration has to be repeated each time the current value changes.

b. Dual Current Method (DCM)

In this method, two separate currents are used for temperature sensing and heating of the LED junction. The sensing current, I_{sense}, must be large enough to turn the junction on over the measured temperature range and not cause any

significant self-heating of the junction. Hence, there is no need for I_{sense} to be pulsed. The typical value used for I_{sense} is 1 mA. The electrical connection for DCM is shown in Fig. 7.6. There are three steps involved in using DCM:

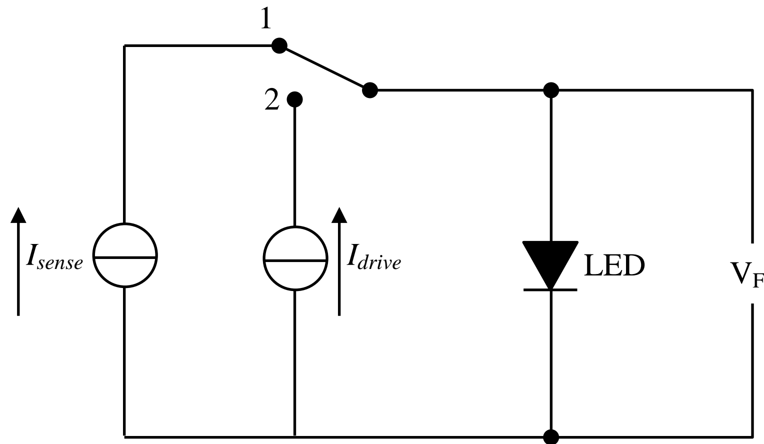


Fig. 7.6. DCM setup for junction temperature measurement

1. Firstly, the forward voltage, V_F, at varying junction temperature is measured when a constant I_{sense} = 1 mA is supplied. A linear relation between the forward voltage versus the junction temperature under I_{sense} can be obtained.
2. Next, I_{sense} is replaced with a desired amount of driving current, I_{drive}, to heat up the junction to a steady state temperature. When steady state is reached, the forward voltage is measured for determining the amount of power that is dissipated in the diode.
3. Lastly, I_{drive} is replaced by I_{sense} and the change in forward voltage as a function of time is measured, which can be relate to the change in temperature, ΔT, by using the linear relation obtained in step 1. The junction temperature, T_j, is determined by:

$$T_j = \Delta T + T_a \tag{7.3}$$

where T_a is the ambient temperature.

The DCM has advantages over the SCM. There is no need for recalibration when the driving current changes. As only a constant current source and voltage measurement capability are required, multiple units can be calibrated at the same time. However, DCM will require a more complicated electronic switch than SCM for measurement.

The forward voltage method is theoretically the easiest method to implement [95]. However, this method is not suitable for measuring the junction temperature in actual lighting equipment under operating conditions. In addition, it does not provide temperature mapping of the chip surface [101].

7.4.2. Wavelength shift method

The wavelength shift method has also been used to determine the junction temperature of an LED [95, 102]. The peak wavelength shift of LEDs is found to be proportional to the junction temperature regardless of how the temperature is created at the junction. Therefore, this linear relationship can be used as a direct measurement of the junction temperature. To do so, the peak wavelength shift is measured at various drive currents at certain case temperatures. A linear relationship between the peak wavelength shift, $\Delta\lambda$, and the change in temperature, ΔT, or power input, ΔP, can be obtained as shown in (7.4) and (7.5) respectively:

$$\Delta\lambda = K_1 \Delta T \qquad (7.4)$$

$$\Delta\lambda = K_2 \Delta P \qquad (7.5)$$

where K_1 and K_2 are constants. The wavelength shift method can be a useful method for measuring the junction temperature of LEDs when access to the

pins of LEDs is difficult. However, the shift in the peak wavelength can be very small in some LEDs and thus difficulties may arise in using this method [95].

7.4.3. Liquid Crystal Thermography

A neumatic liquid crystal thermographic technique (LCT) has been demonstrated as a direct temperature measurement technique to determine the junction temperature of GaN-based LEDs [101]. When a region coated with a liquid crystal layer on the device surface is locally heated, either due to device failure or power consumption, above the transition temperature of the liquid crystal, the liquid crystal layer within that region will change from anisotropic to isotropic. This method is reported to be non-destructive and has a high spatial resolution that is limited only by the resolution of the microscope. However, the realistic junction temperature of an LED chip after packaging could differ from the data obtained using LCT due to absence of the encapsulant. The effect of the encapsulant on the junction temperature of LEDs has been presented in [101]. Temperature measurements made using a micro thermocouple placed on an area that was very near to the inside of the chip (less than 0.1mm) was simultaneously performed during the operation of LEDs and the effect of epoxy thickness on the thermal behaviour was investigated. From the results, it was noted that the junction temperature is dependent on the thickness of the epoxy encapsulant. It was shown that the low epoxy dome samples yielded higher junction temperatures as compared to the high epoxy dome samples. The junction temperature of the chip was assumed to be equivalent to the temperature of the epoxy with a thickness less

than 0.1 mm from the chip. This assumption was validated using Finite Element Analysis (FEA).

7.4.4. Infrared thermography

Infrared thermography is a popular method for thermal imaging and temperature mapping of an object's surface. It has been used to measure LED junction temperatures in [75, 103-106]. Critical parameters such as emissivity and reflectivity of various materials present on the LED surface, and ambient temperature have to be accounted for before accurate temperature distributions can be obtained. Due to presence of the encapsulant in an LED package which is opaque to IR radiation, the measured temperature may actually be the surface temperature of the encapsulant rather than the junction temperature. A further complication arises when the LED die material is transparent to a mid-wave IR camera [79] which offers a better spatial resolution of 2.5 μm to 5 μm.

7.4.5. Thermoreflectance thermography

Thermoreflectance thermography (TRT) has been used to measure the surface temperature of both encapsulated LEDs [107] and decapsulated LEDs [108, 109]. Optical band-pass filters were used to attenuate the strong signal from the DUT and to prevent camera saturation. Uncalibrated thermal images can be used to observe temperature uniformity and to detect defective devices with hotspots. TRT presented in [107] allows for simultaneous electroluminescence and transient thermal imaging. An uncalibrated thermal image of measured LEDs was presented to show the temperature distribution uniformity across

the die surface. TRT is suitable for measuring the surface temperature of an LED die since the encapsulation materials are often transparent to visible light.

TRT has also been used to characterize the thermal behaviour of semiconductor devices that emit strong light, such as lasers [82]. A low pass filter was placed in the optical path to minimize the primary laser irradiation on the TR imaging. It has been demonstrated that the TR measurements performed at the optimal light wavelength successfully provided a submicron-resolution map of the active area of sample lasers.

7.5. Measurement of Junction Temperature of LEDs

This section describes the measurement of the surface temperatures of three LED packages using thermoreflectance thermography (TRT), infrared thermography (IRT) and the forward voltage method based on SCM (Section 7.4.1(a)). The three LED packages studied are:

(i) White phosphor-converted LED package with phosphor incorporated in the encapsulant, which we shall refer to as the PIE LED package;

(ii) White phosphor-converted LED package with chip-level-conversion which we shall refer to as the CLC LED package; and

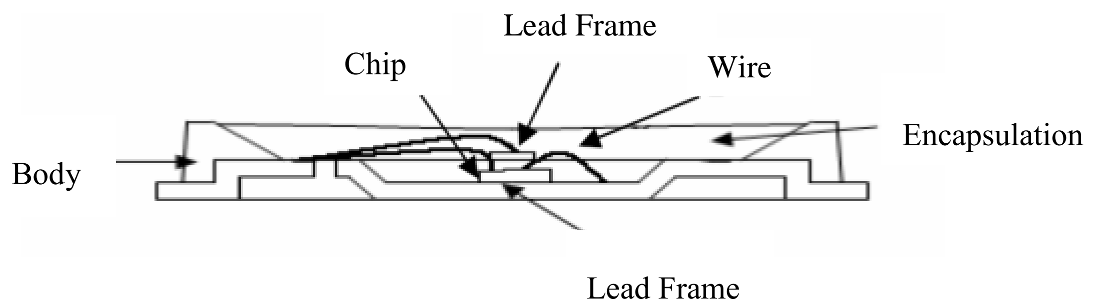
(iii) Unpackaged blue LED die which we shall refer to simply as the blue LED die.

7.5.1. White LED with phosphor incorporated in the encapsulant

a. Description

This white LED package with phosphor incorporated in the encapsulant is shown in Fig. 7.7 and shall be referred to hereafter as the PIE LED package. It is a surface mounted LED with its substrate made up of a molded plastic reflector sitting on top of a lead frame. The chip source found in this LED package is a blue LED, made up of GaN on sapphire. The die is attached within the reflector cavity and the cavity is encapsulated with silicone.

(a)



(b)

Fig. 7.7. (a) Top view and (b) internal structure of the PIE LED package

b. Characteristic Diagrams

i. Spectrum data

The spectrum data of the PIE LED is shown in Fig. 7.8. As can be seen, the relative emission intensity peaked at wavelength of 450 nm and around 600 nm. The lowest relative emission intensity happens before wavelength of 400 nm and after 780 nm.

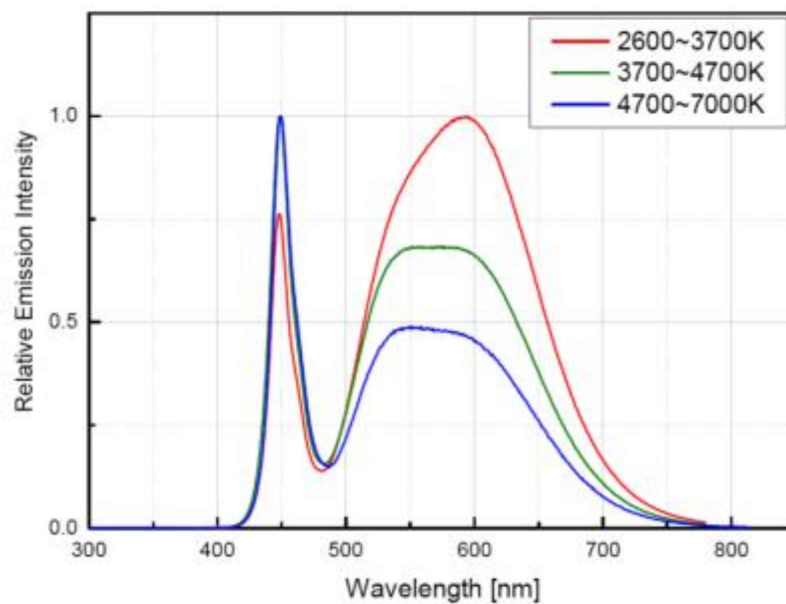


Fig. 7.8. Spectrum data of the PIE LED.

ii. Forward Voltage vs Forward Current

The current-voltage (IV) characteristics of the PIE LED is shown in Fig. 7.9. The reverse region is not shown in Fig. 7.9. It is noted that applying a reasonable reverse voltage will lead to a small amount of reverse current flowing from the negative terminal to the positive terminal, while applying a large reverse voltage will lead to failure of the LED device. The turn-on voltage was found to be 2V. As the forward voltage increases beyond the turn-

on voltage, the current increases greatly. The typical operating current for this LED is 100mA.

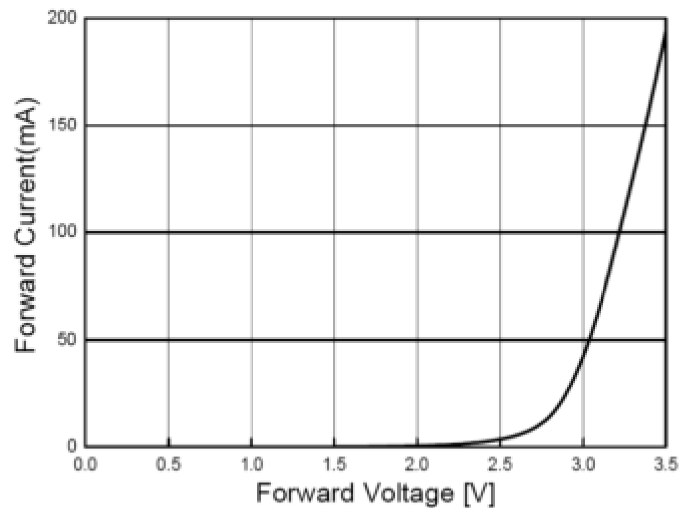


Fig. 7.9. Current-voltage (IV) curve of the PIE LED

c. Thermoreflectance Thermography Results

Thermoreflectance thermography (TRT) was used to measure the surface temperature of the LED. During the temperature measurement, a thermal chuck was used to maintain a constant base temperature of the device under test, in this case 25°C. The following pulse timing parameters were used (with reference to Fig. 6.14):

- The CCD camera exposure rate shown in Fig. 6.14 was set to 20Hz. As the camera runs at almost 100% duty cycle, the camera was on for 50ms and off for 0.1ms then on again.
- The device heating pulse was 5ms. For a device duty cycle of 25%, the device was on for 5ms and off for 15ms. The period for the whole cycle was 20ms.

- The maximum temperature rise of the device occurs between 4ms and 5ms of the introduction of the device pulse. Therefore, an image delay of 5ms was set to measure the maximum temperature rise.
- A light source of 1ms pulse width are strategically triggered at the start and end of the temperature rise curves as shown in Fig. 6.14.

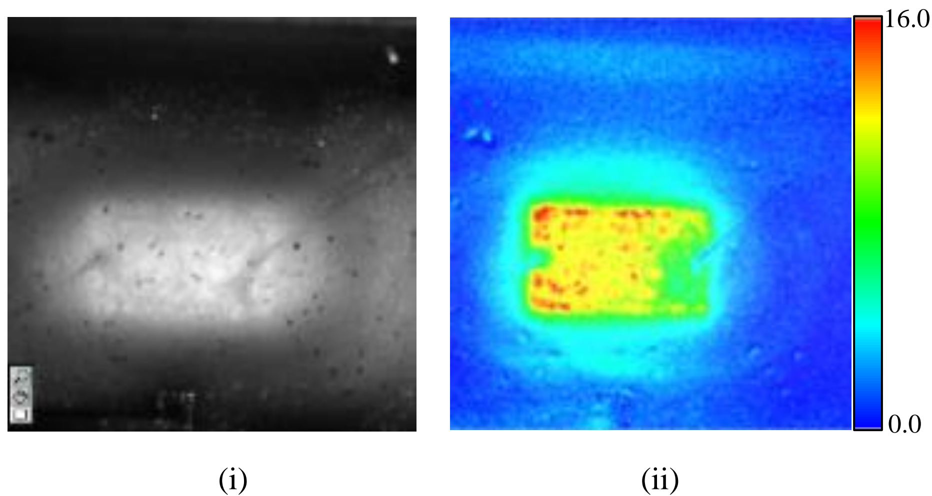


Fig. 7.10. (i) Optical and (ii) TR thermal (uncalibrated) images of the PIE LED package at 100mA

In Fig. 7.10, the optical and thermal images of the white PIE LED package at 100mA obtained using TRT are shown. It is noted in Fig. 7.10(i) that the encapsulation material used for this white LED is not very transparent, which leads to difficulty in measuring the temperature of the LED die using TRT as the temperature measured is likely to be that of the surface of the encapsulant. Hence, the thermoreflectance coefficient, C_{TR}, for the LED die was not measured. Therefore in Fig. 7.10(ii), the TR thermal image is showing the apparent change in temperature (in arbitrary units) across the top surface of the LED package. A relatively uniform temperature distribution across the surface of the LED package can be observed.

7.5.2. White LED with phosphor on the chip

a. Description

Fig. 7.11. White surface mount diode package with a clear silicone lens

The surface mounted white LED package with a clear silicone lens is shown in Fig. 7.11. The chip source found in this LED package is a blue LED, made of GaN on sapphire. This is a chip level conversion (CLC) LED package where a layer of phosphor is coated onto the surface of the emitting chip to convert the emitted blue light into white light.

b. Characteristic Diagrams

i. Spectrum Data

The spectrum data of the white CLC LED is shown in Fig. 7.12. As can be seen, the emission intensity peaked at wavelength of 450 nm and around 600 nm. The lowest relative emission intensity happens before wavelength of 400 nm and after 900 nm.

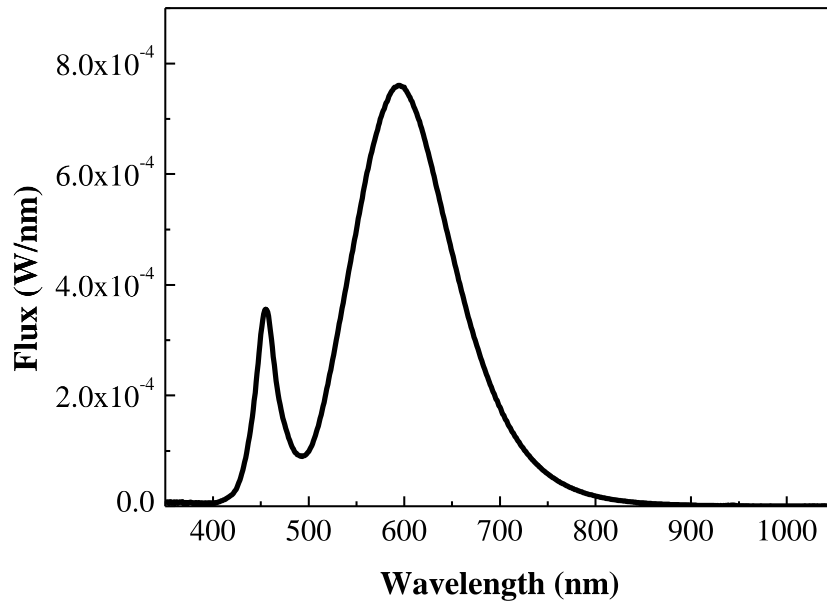


Fig. 7.12. Spectral flux of a white CLC LED

ii. Forward Voltage vs Forward Current

The current-voltage (IV) curve characteristic of the CLC LED is shown in Fig. 7.13. The reverse region is not shown in Fig. 7.13. The turn-on voltage is shown to be 2.7V. As the forward voltage increases beyond the turn-on voltage, the current increases greatly. The typical operating condition for this LED is 350mA.

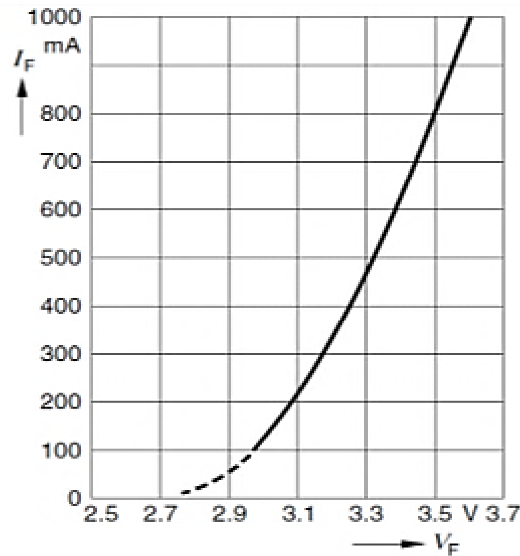


Fig. 7.13. Current-voltage (IV) curve of a white phosphors-converted LED on the chip level.

c. Experimental Results

i. Forward Voltage Measurement Results

The experimental setup is shown in Fig. 7.14. The LED was placed on the cold plate. A thermocouple with an accuracy of ±0.1 °C was attached onto the PCB near to the LED package. This was to ensure that the temperature measured by the thermocouple would be close to the junction temperature. A thermal tape was used to secure the thermocouple onto the PCB and thermal paste was used to ensure good contact between the thermocouple and the PCB. An insulated cover was used to maintain a temperature-controlled environment by preventing heat loss from the LED package to the ambient.

The forward voltage characteristic of the LED was calibrated by placing it a temperature-controlled environment set initially at25 °C. A dwell time of 10 minutes was allowed for the LED junction to reach thermal equilibrium. After the LED junction had reached thermal equilibrium, a current source of 350

mA with a short pulse width of 5 μs and a low duty cycle of 0.5% was supplied to the LED. The forward voltage was measured using an oscilloscope with an accuracy of 0.4% and a resolution of 0.01V. The forward voltage measurement was repeated for a temperature range of 25°C to 65°C in steps of 10°C. The forward voltage of the LED versus the junction temperature is plotted in Fig. 7.15.

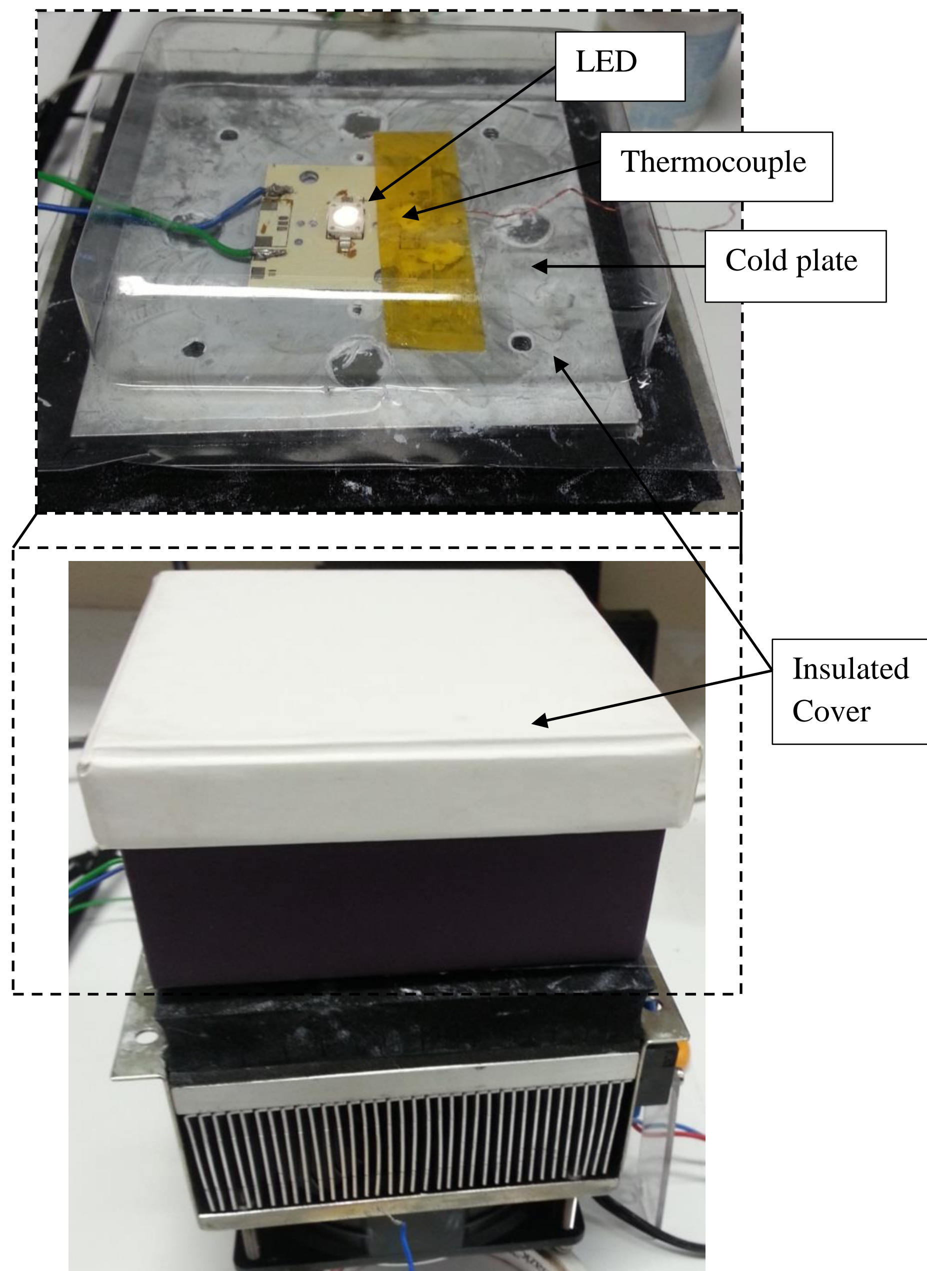


Fig. 7.14. Experimental setup for forward voltage measurement

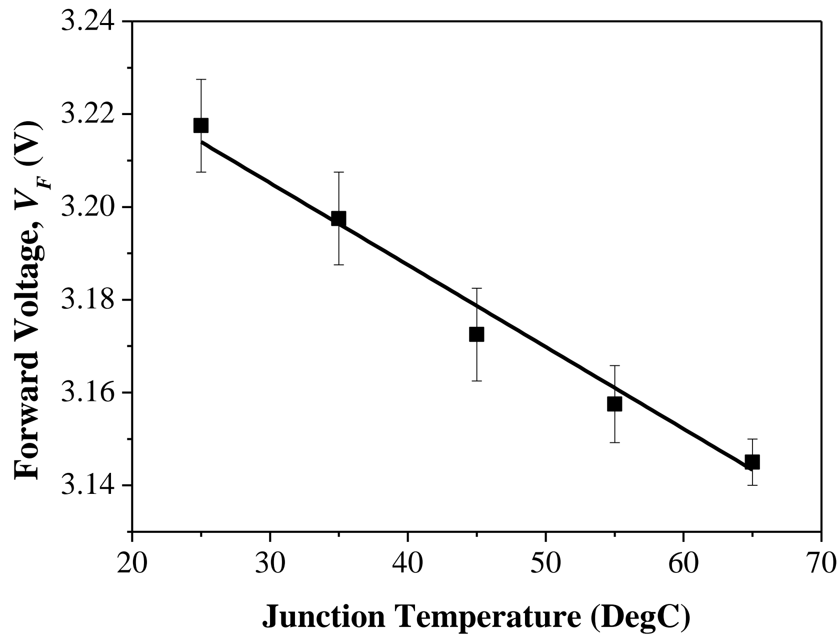


Fig. 7.15. Forward voltage versus the LED junction temperature

From Fig. 7.15, the linear relation between the forward voltage, V_F, and the junction temperature, T_j, is expressed as:

$$V_F = -1.77 \times 10^{-3} \times T_j + 3.26 \tag{7.6}$$

where the slope of the line is -1.77×10^{-3}V/°C.

At constant current source of 350 mA, the measured V_F of the LED is 3.16V. Using (7.6), the T_j of the LED is 56°C.

ii. Thermoreflectance Thermography Results

The relative change in reflectivity, $\Delta R/R$ of the surface of the CLC LED die versus the change in temperature ΔT was measured and plotted in Fig. 7.16. A linear relationship between $\Delta R/R$ and ΔT was obtained:

$$\Delta R/R = 1.71 \times 10^{-5} \times \Delta T \tag{7.7}$$

where the thermoreflectance coefficient, C_{TR}, of the LED die surface is seen to be 1.71×10^{-5} K^{-1}.

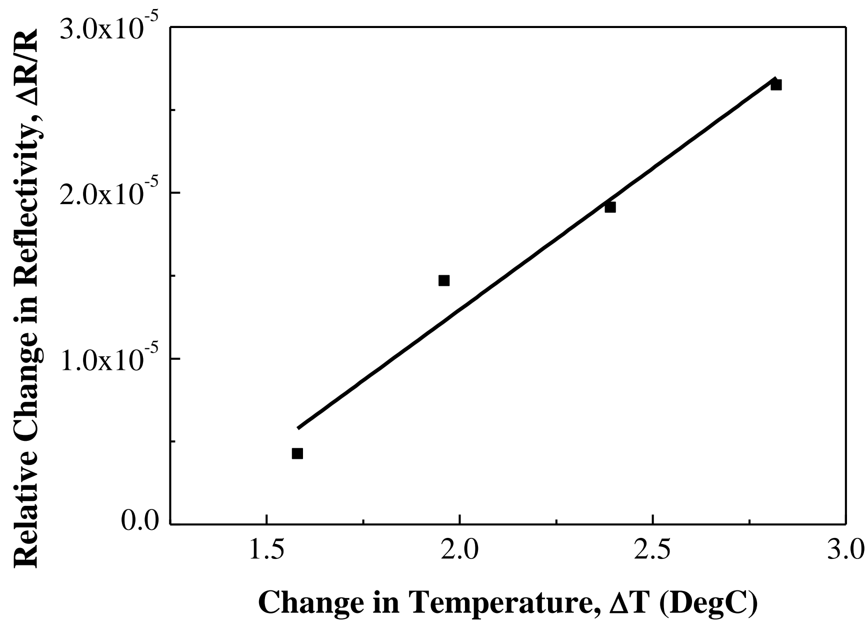


Fig. 7.16. A plot of change in relative reflectivity, $\Delta R/R$, versus change in temperature, ΔT, for the CLC LED die surface

In Fig. 7.17, the optical and thermal images of the CLC LED package at 350mA and base temperature of 25°C obtained using TRT are shown. From Fig. 7.17(i), the encapsulant for this white LED package is transparent to visible light, thus TRT is able to measure the surface temperature of the LED die. It is noted that TRT only measures the surface temperature of the LED die instead of the junction temperature since TRT is measuring the relative change in reflectivity of the die surface. The temperature rise, ΔT, across the top surface of the LED package is shown in Fig. 7.17(ii). As C_{TR} is measured only for the LED die surface, the thermal image shown in Fig. 7.17(ii) is calibrated only for the LED die surface. The thermal image shows that the temperature distribution of the LED die is non-uniform, with ΔT at the center at 25°C. Therefore, the measured surface temperature of the LED die is:

$$T = \Delta T + 25 = 50^oC \quad (7.8)$$

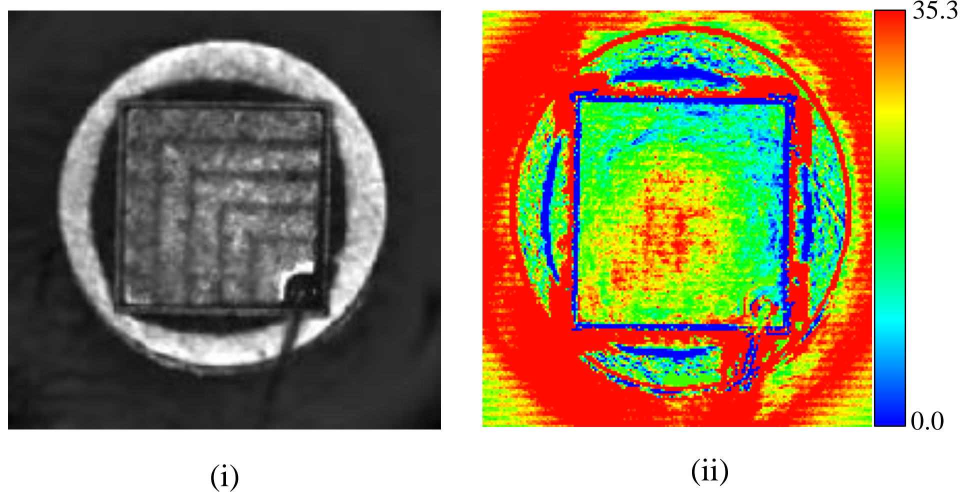
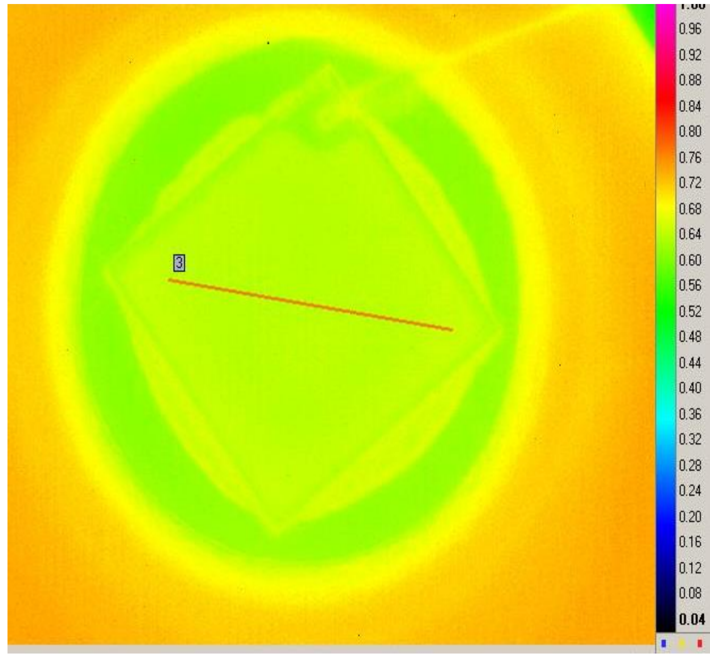


Fig. 7.17. (i) Optical and (ii) TR thermal (only die surface is calibrated) images of a white phosphor CLC LED package at 350mA

iii. Infrared Thermography Results

Infrared thermography (IRT) was used to measure the surface temperature of the LED package. The emissivity map of the LED package is presented in Fig. 7.18. A line scan is drawn across the LED die and the emissivity value, ε, measured is approximately 0.64. The thermal image obtained after emissivity correction using an IR camera is shown in Fig. 7.19. The maximum temperature of the CLC LED package determined from the line scan in the IR image across the centre is 49.0^{o}C, which is close to temperature values obtained from both thermal transient measurement and TRT. However, due to uncertainty on the transmittance and reflectance of the silicone encapsulant towards infrared radiation, there is some ambiguity on the IRT results.



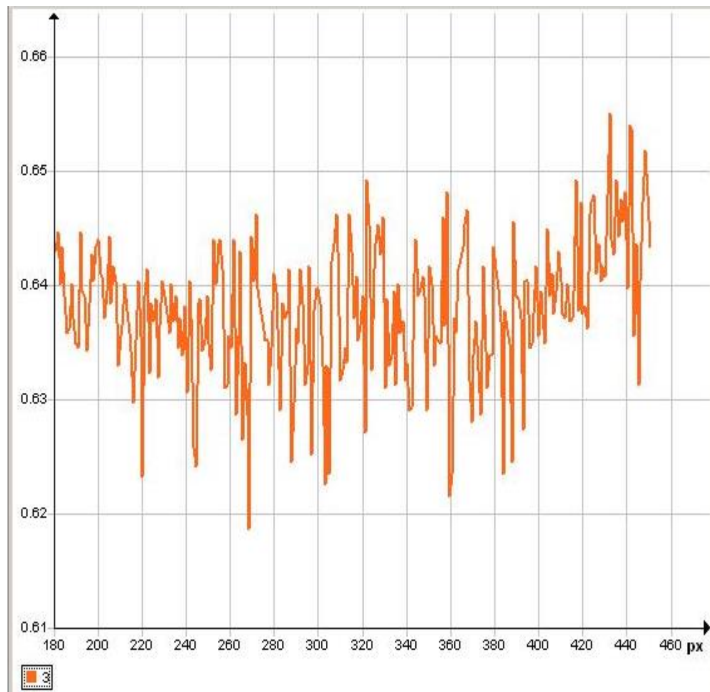


Fig. 7.18. Emissivity map of the CLC LED package

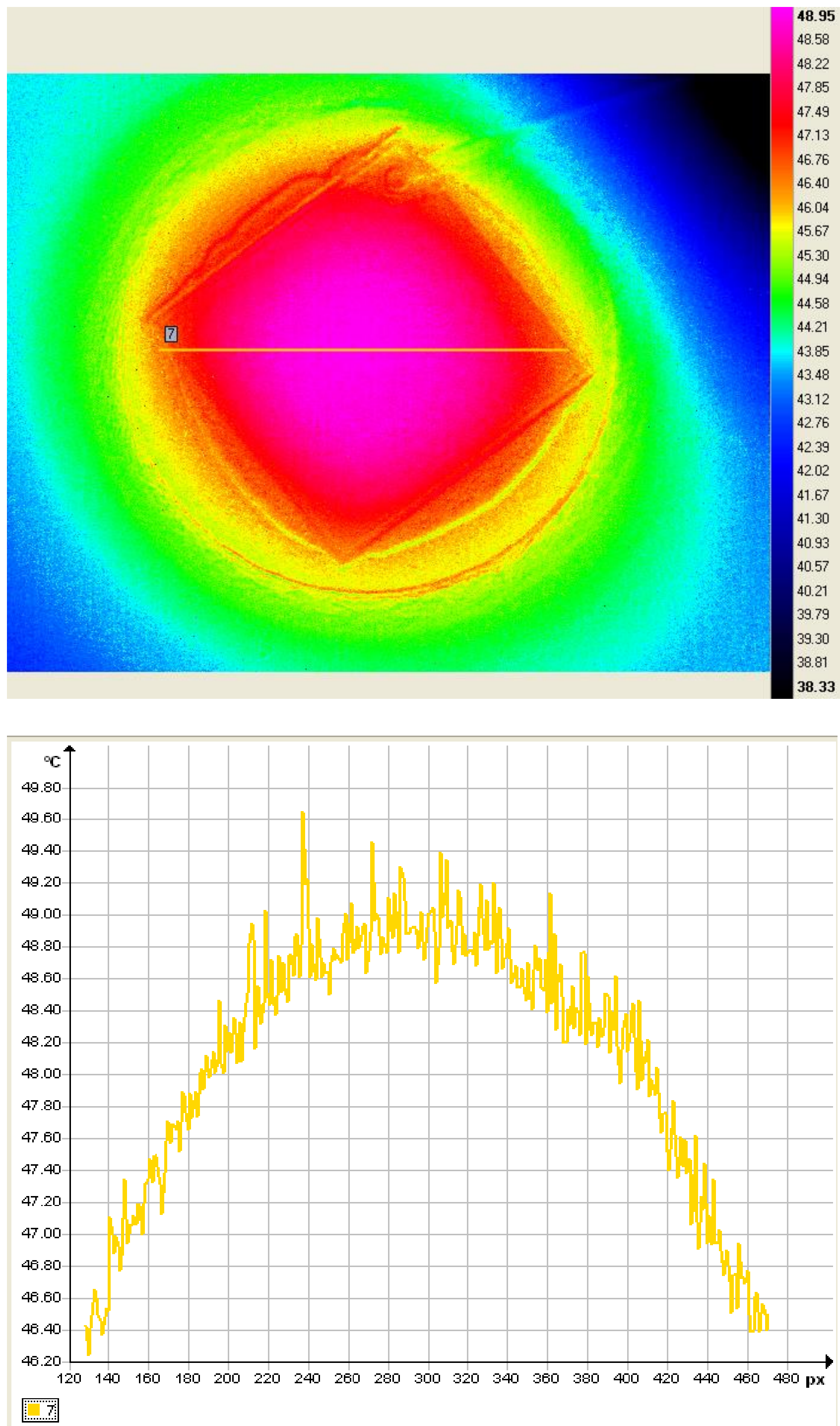


Fig. 7.19. Temperature distribution along a line scan across the CLC LED package shown in the IR image

7.5.3. Unpackaged Blue LED Die

a. Description

In this work, the measurement of junction and surface temperature of an unpackaged gallium nitride (GaN) LED die was carried out. The dimension of the LED die is approximately 4mm x 4mm.

b. Characteristic Diagrams

i. Spectrum data

The spectrum data of the LED die is shown in Fig. 7.20. As can be seen, the emission intensity peaked at wavelength of 450. The lowest relative emission intensity happens at before wavelength of 400 nm and after 550 nm.

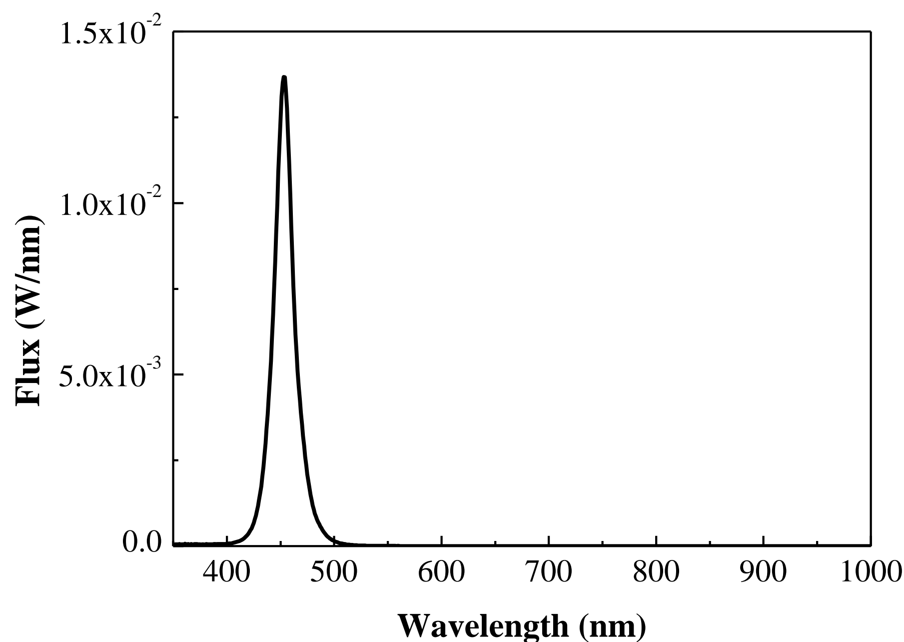


Fig. 7.20. Spectral flux of a blue LED die

c. Experimental Results

i. Thermoreflectance Thermography Results

The relative change in reflectivity, $\Delta R/R$ of the surface of the LED die versus the change in temperature ΔT was measured and plotted in Fig. 7.21. A linear relationship between $\Delta R/R$ and ΔT was obtained:

$$\Delta R/R = 7.12 \times 10^{-5} \times \Delta T \qquad (7.9)$$

where the thermoreflectance coefficient, C_{TR}, of the LED die surface is 7.12×10^{-5} K^{-1}.

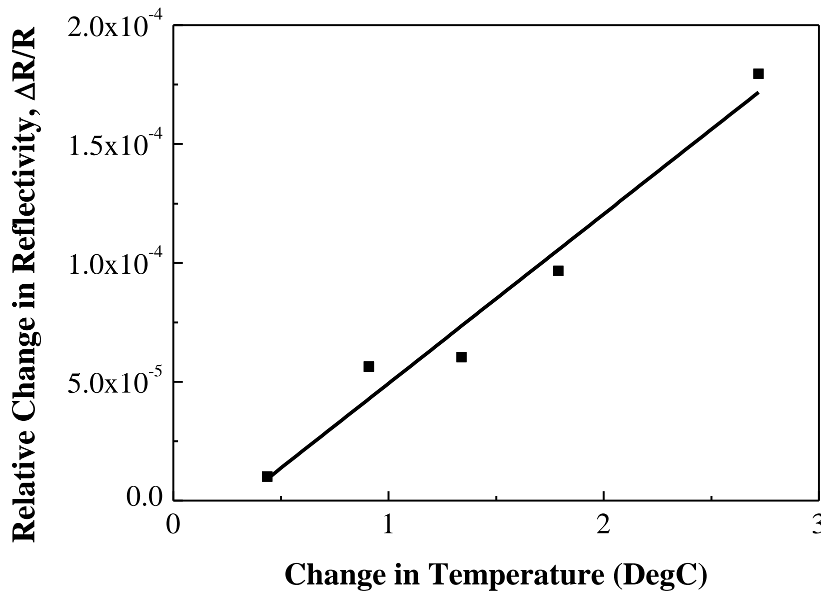


Fig. 7.21. A plot of change in relative reflectivity, $\Delta R/R$, versus change in temperature, ΔT, for blue LED die surface

In Fig. 7.22, the optical and thermal images of an unpackaged blue LED die at 350mA and base temperature of 25°C obtained using TRT are presented. The temperature rise of the LED die across the surface is presented in Fig. 7.22(ii). As only the LED die surface was calibrated for C_{TR}, the thermal image shown in Fig. 7.22(ii) is calibrated only for the LED die surface. The contact regions

shown in Fig. 7.22(ii) have a different C_{TR} value than the surface of the die, so the thermal image shows these areas as colder in this case. The maximum temperature rise, ΔT, at the center of the die is 11.7°C. Therefore, the measured surface temperature of the LED die is:

$$T = \Delta T + 25 = 37^{o}C \tag{7.10}$$

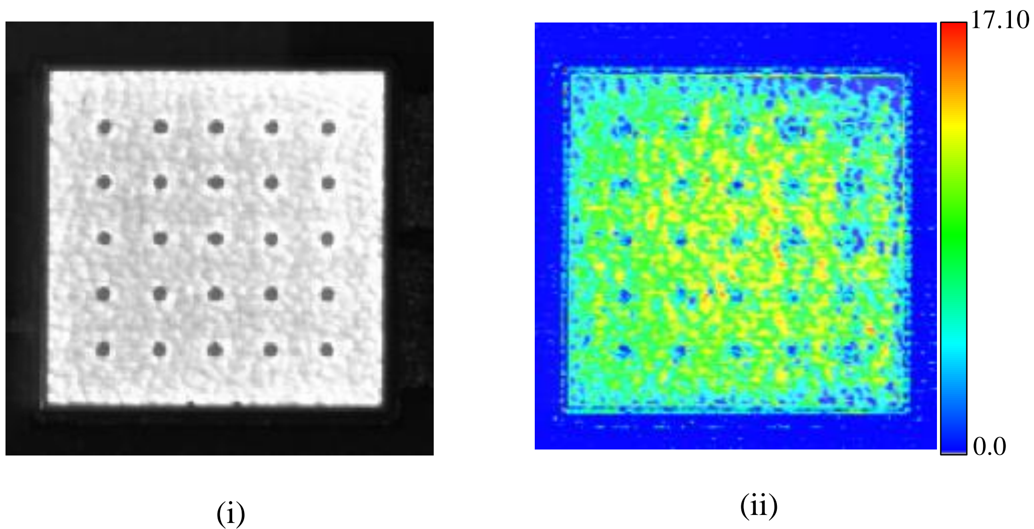


Fig. 7.22. (i) Optical and (ii) TR thermal (only die surface is calibrated) images for an unpackaged blue LED die at 350mA

ii. Infrared Thermography Results

Infrared thermography was used to measure the surface temperature of the LED die. The emissivity map across the LED die surface is presented in Fig. 7.23. A line scan is drawn across the LED die and the emissivity value, ε, measured across it is approximately 0.18. The thermal image obtained after emissivity correction using an IR camera is shown in Fig. 7.24. The maximum temperature of the LED die determined from the line scan in the IR image across the center is approximately 48.0°C. The large discrepancy between measured temperatures using IRT, TRT and transient thermal measurement

could be due to low emissivity surfaces present on the LED die that poses a challenge in obtaining accurate IR measurements.

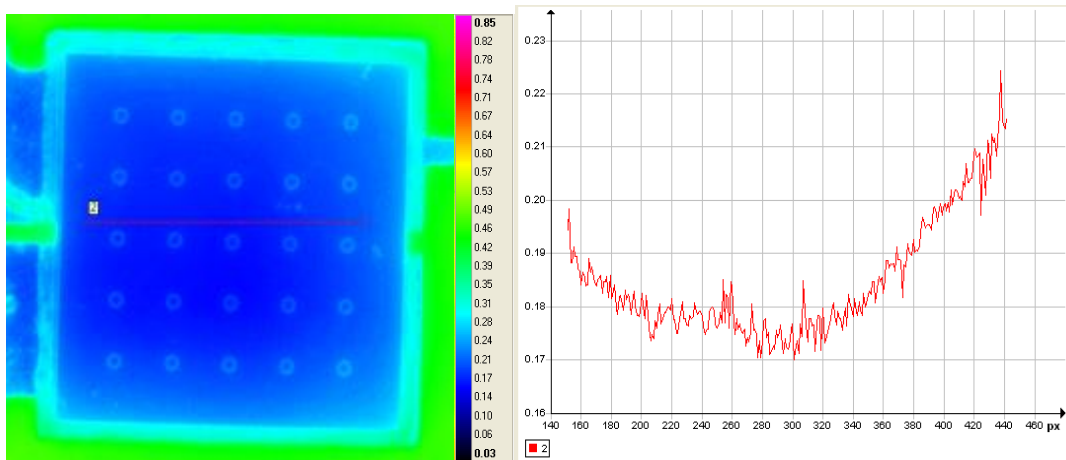


Fig. 7.23. Emissivity map of an unpackaged blue LED die

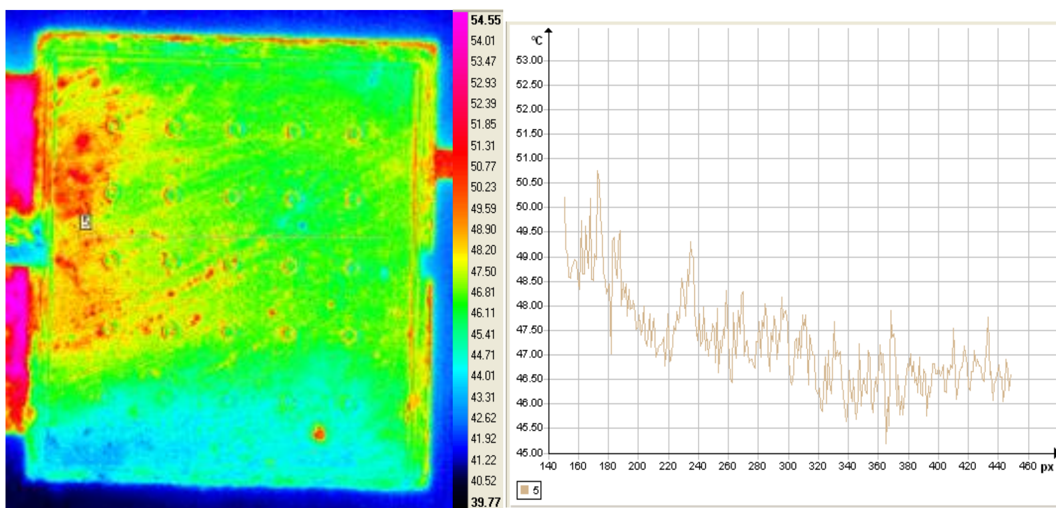


Fig. 7.24. Temperature distribution along a line scan across the unpackaged blue LED die in the IR image

7.6. Characteriztion of Junction to Ambient Thermal Resistance of LEDs

In this section, the measurement of the junction to ambient thermal resistance, R_{ja}, of both packaged and unpackaged LEDs will be described. To do this, two instruments are used, i.e. the integrating hemisphere and the transient thermal

tester (T3ster) system. The integrating hemisphere measures the optical power of the LED while the T3ster measures the thermal resistance of material layers and the thermal resistance of the interface between each pair of material layers [83, 110-114].

7.6.1. Thermal Resistance Measurement

a. Theory

During transient thermal testing of a semiconductor device, a step-wise power excitation is supplied and the corresponding change in the temperature is measured by electrical means. This is possible as every semiconductor device has a temperature sensitive parameter (TSP), which is the forward voltage of a diode. The relation between the change in the forward voltage of a diode, ΔV, and the change in the temperature, ΔT, is expressed as:

$$TSP = \Delta V / \Delta T \quad (7.11)$$

The temperature rise function, $a(t)$, is a unique characteristic of the thermal R-C network of the device under test (DUT) which can be expressed as:

$$a(t) = R\left[1 - e^{-\frac{t}{\tau}}\right] \quad (7.12)$$

where R is the resistance value, t is the time, and τ is the time constant. The response of more complex thermal structures can be considered as the sum of many such individual exponential terms with different τ time constants of different magnitudes [115]. To characterize a thermal system, the response function (7.12) is transformed into a logarithmic time variable such that the temperature rise curve is known as the thermal impedance curve. The

measured thermal impedance is converted into a cumulative structure function, i.e. a plot of the cumulative thermal capacitance versus the cumulative thermal resistance along the heat-flow path. The cumulative structure function is directly constructed from the Cauer-network equivalent R-C model of the thermal system (Fig. 7.25). A one-dimensional heat flow model needs to be assumed for a given structure so that the Cauer network will correspond well to the different parts of the physical structure [116].

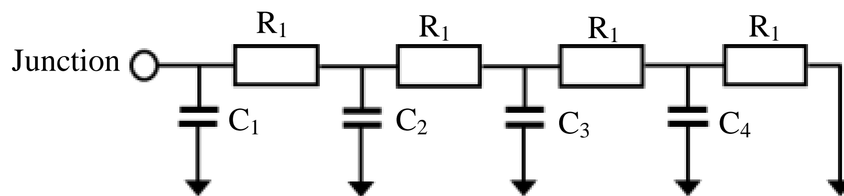


Fig. 7.25. Cauer-network model of the thermal impedance.

To carry out the transient measurement using T3ster, the device under test (DUT) is first placed on a cold plate at a constant temperature to ensure a one-dimensional heat flow from the junction towards the cold plate. A driving current, I_{drive}, is supplied to heat up the device to a steady state temperature (Fig. 7.26). When steady state has been reached, the driving current is switched off and the transient cooling response of the DUT is recorded by sending a very small sensing current, I_{sense}, of 1mA to the diode of the DUT and recording the forward voltage drop of the diode from which the temperature of the diode can be deduced using (7.11).

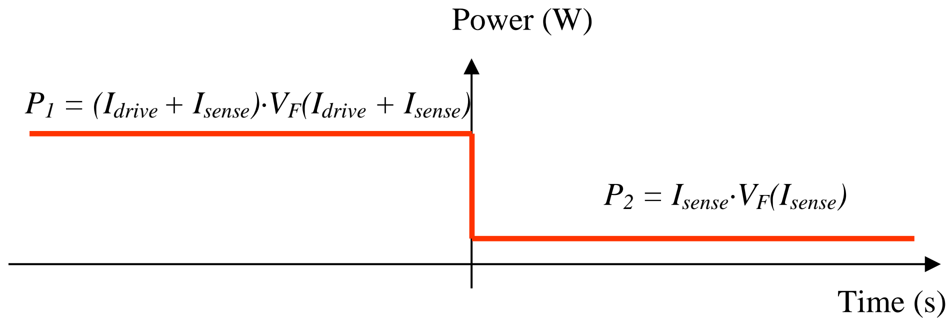


Fig. 7.26. Power step respond with respect to time for measurement of diode

Therefore, the apparent junction to ambient thermal resistance of a diode can be calculated as:

$$R_{ja} = \Delta T/\Delta P_T \quad (7.13)$$

where ΔP_T is the change in the total electrical power input into DUT:

$$\Delta P_T = P_1 - P_2 \quad (7.14)$$

As part of the supplied electrical power is converted into optical power in light emitting diodes, the real junction to ambient thermal resistance of the LED should be calculated as:

$$R_{ja,real} = \Delta T/(\Delta P_T - \Delta P_{opt}) \quad (7.15)$$

where ΔP_{opt} is the change in the optical power when I_{drive} is changed to I_{sense}.

Using T3ster, the heat-flow path of the LED can be analysed and the thermal resistance of any thermal interfaces can be derived.

b. Experimental Set-up

The experimental setup is similar to Fig. 7.14, except that the thermocouple is now placed on the cold plate for measurement of thermal resistance from the junction to the base of the LED die, or base of the PCB in the case of a

packaged LED. The DUT is connected to a diode fixture shown in Fig. 7.28. The sensing current, I_{sense}, and driving current, I_{drive}, are supplied to the DUT by the T3ster. A digital voltmeter (DVM) connecting the DUT to the T3ster is used to monitor the change in the forward voltage during measurement. To obtain the real thermal resistance of LEDs (7.15), the optical power, P_{opt}, of the LED is measured using an integrating hemisphere shown in Fig. 7.29.

Fig. 7.27. Thermal Transient Tester (T3ster)

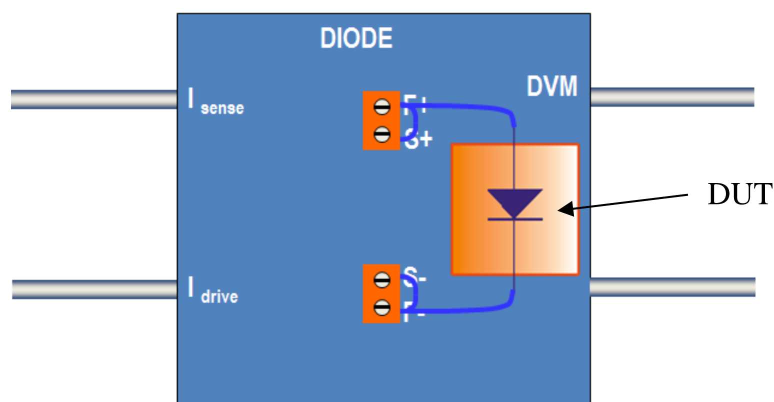


Fig. 7.28. Diode fixture with a DUT connected

7.6.2. Optical Measurement of LEDs

An integrating sphere can be used to measure the radiant flux of lamps placed in their geometric centre. It has a hollow spherical cavity with its interior covered with a diffuse white reflective coating. In this work, an integrating hemisphere system was used to determine the radiant flux (W/nm) of LEDs (Fig. 7.29). A schematic diagram of the integrating hemisphere system is shown in Fig. 7.30.

Fig. 7.29. Integrating hemisphere system

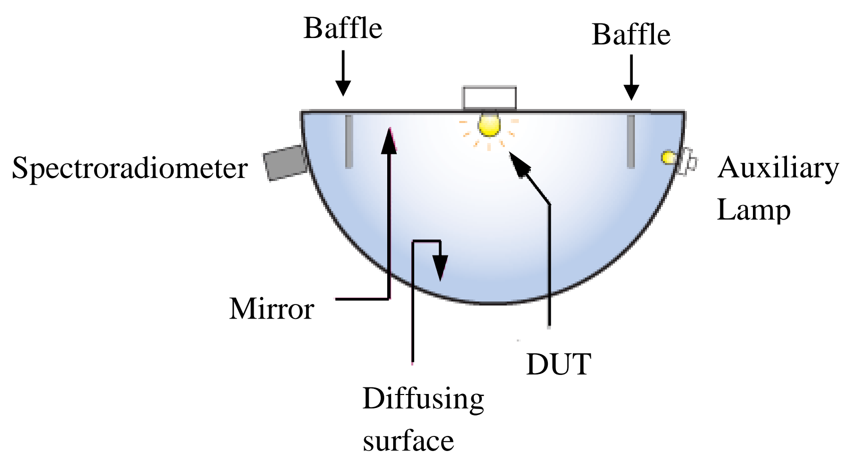


Fig. 7.30. Schematic diagram of an integrating hemisphere system

As shown in Fig. 7.30, the device under test (DUT) is placed at a port in the centre of the plane mirror. The body of the luminaire, the heat sink and any driving electronics remain outside of the chamber and do not absorb any light. The internal mirrored surface allows for symmetrical light distribution by the specular image that is akin to a full sphere. A thermoelectric cooler (TEC) is used to maintain the base temperature of the DUT. Before measuring the radiant flux of the DUT, absorption correction is first carried out. The presence of items in the testing environment, such as the metallic surface of a packaged LED or the auxiliary lamp, causes light to be self-absorbed. The absorption error is corrected by using an auxiliary lamp of known luminous flux placed in the hemisphere to calibrate the spectroradiometer. The function of the spectroradiometer is to measure the spectral power distributions of light sources. Baffles are located at appropriate positions to prevent the spectroradiometer from directly viewing the irradiated DUT or the auxiliary lamp during measurement or calibration. Light rays from the DUT that are incident on any point of the inner surface of the hemisphere are, by multiple scattering reflections, distributed equally to all other points. The radiant flux as a function of wavelength is measured (Fig. 7.31). The optical power of the DUT is determined from the area under the curve shown in Fig. 7.31.

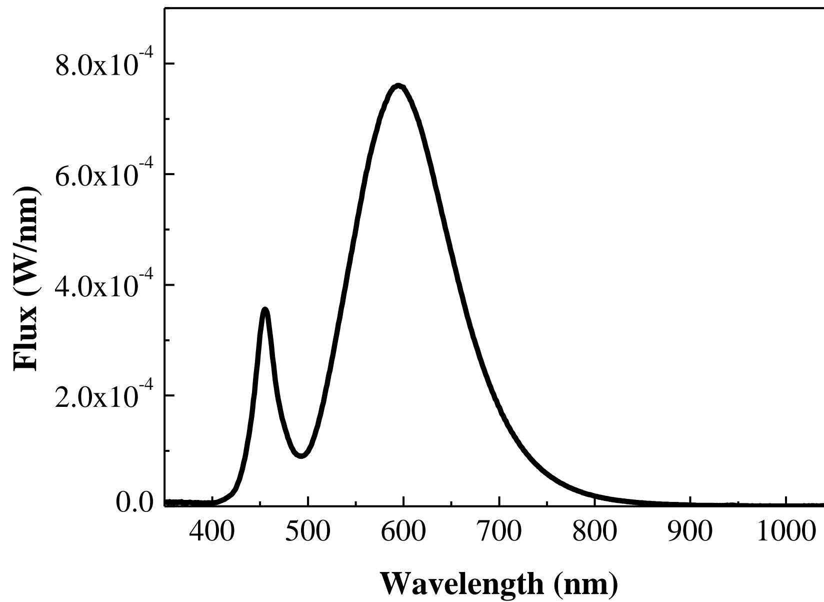


Fig. 7.31. Spectra of a white LED

7.6.3. White CLC LED with phosphor on the chip

The temperature sensitivity parameter (TSP) curve for the white CLC LED (Fig. 7.11) is obtained and plotted in Fig. 7.32. The measurement was carried out using a constant sensor current of 1 mA in the temperature range of 25°C to 55°C to avoid self-heating. From the curve, the TSP is found to be:

$$TSP = \frac{\Delta V}{\Delta T} = -1.47\ mV/K \tag{7.16}$$

For thermal resistance measurement, the CLC LED package was placed on a cold plate set at 25°C. Transient thermal measurement was carried out to record the cooling curve with a sensor current of 1 mA after driving the sample at its operating current of 350 mA for 5 minutes to reach thermal stabilization. During measurement, the heated LED was allowed to cool for 100s. The smoothed response of the cooling curve for the CLC LED is plotted

in Fig. 7.33. As can be seen, the steady state for thermal resistance measurement is observed to be reached in about 30s.

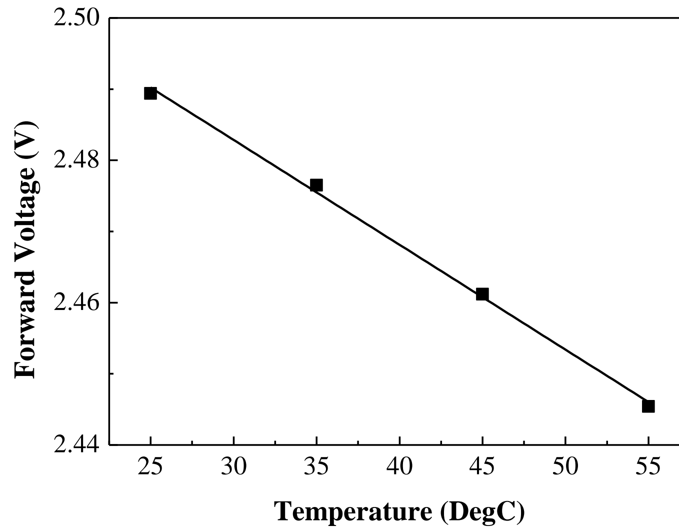


Fig. 7.32. Forward voltage versus temperature plot of the CLC LED

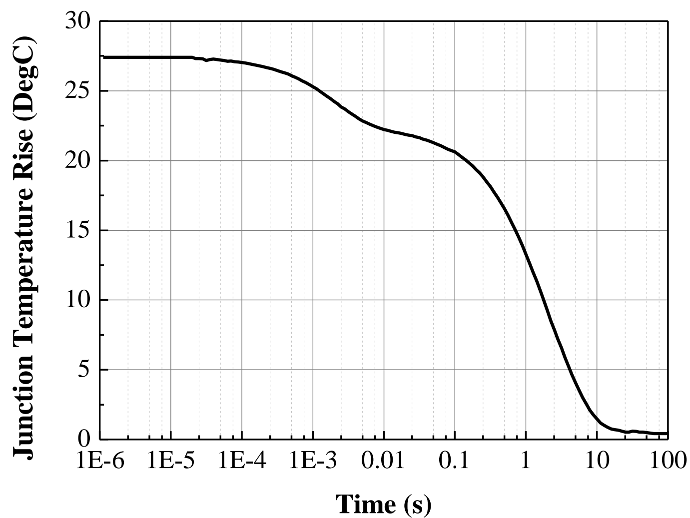


Fig. 7.33. Smoothed response of a cooling curve of the CLC LED package

The cumulative structure function that describes the thermal resistance of the LED package is presented in Fig. 7.34. The cumulative structure function is a plot of the cumulative thermal capacitance, ΣC_{th}, versus the cumulative

thermal resistance, ΣR_{th}, measured from the junction towards the heat sink. The emitted optical power is obtained from the spectral flux (Fig. 7.12) measured using the integrating hemisphere. Using (7.14), the ΔP_T = 1.105W and ΔP_{opt} = 0.116W for a driving current of 350mA.

From Fig. 7.34, the apparent total thermal resistance, R_{ja}, of the CLC LED package by assuming all electrical power input P_T is converted into heat, is evaluated to be 25.8 K/W.

By taking into consideration of P_{opt}, the real thermal resistance $R_{ja,real}$ is evaluated to be 28.8K/W which is an increase of approximately 12%.

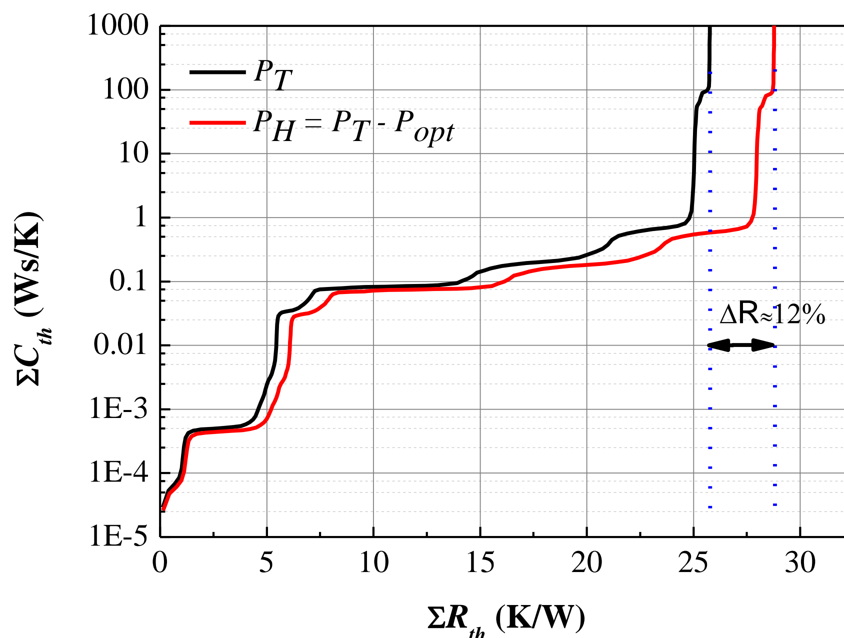


Fig. 7.34. Cumulative structure function for the CLC LED package with driving current of 350mA at heat sink temperature of 25°C

From the cumulative structure function, the thermal resistance value for different layers of the LED package can be determined. The LED package structure shown in Fig. 7.35 consists of:

- LED chip + 1st die attach + submount
- 2nd die attach
- Heat slug
- 3rd die attach between the heat slug and printed circuit board (PCB)
- Thermal interface material (TIM) between the PCB and the cold plate

The thermal resistances of the different layers present in the LED package identified by different colour segments are shown in the cumulative structure function (Fig. 7.35). Each coloured segment in Fig. 7.35 corresponds to the respective layer in the LED package structure with the same colour.

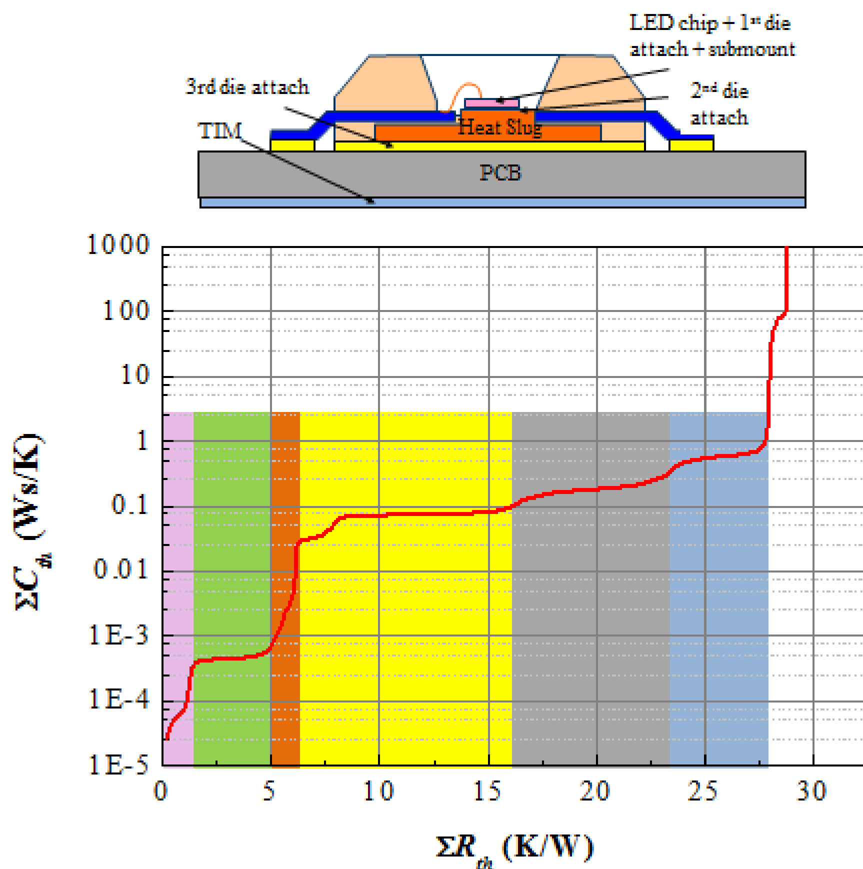


Fig. 7.35. Structure of an LED package

From the thermal resistance measurement, the junction temperature of the white LED package at 350mA is:

$$T_j = R_{ja,real}(\Delta P_T - \Delta P_{opt}) + T_a = 53.5^oC \qquad (7.17)$$

7.6.4. Unpackaged Blue LED Die

The thermal resistance of an unpackaged blue LED die was measured using the T3ster. The experimental setup shown in Fig. 7.36 is similar to Fig. 7.14. The thermocouple was placed on the cold plate using thermal tape and thermal glue. Probes were used to supply current sources to the LED die.

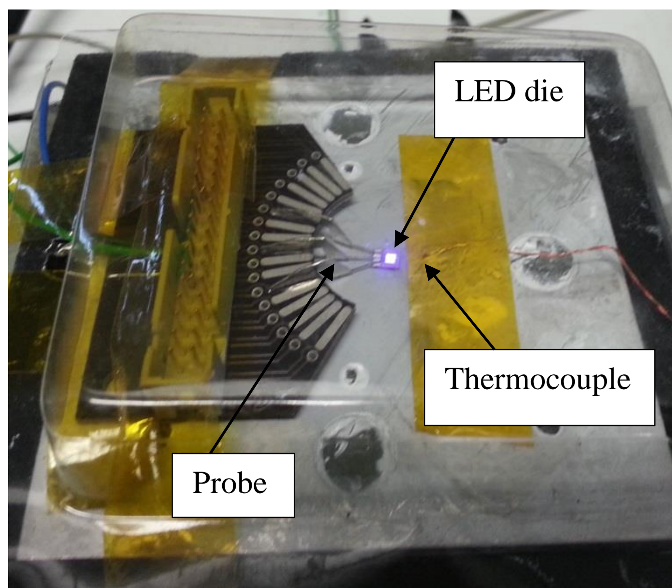


Fig. 7.36. Experimental setup for thermal resistance measurement of an unpackaged blue LED die

The temperature sensitivity parameter (TSP) curve for blue LED die is obtained and plotted in Fig. 7.37. The measurement was carried out using a sensor current of 1mA in a temperature range of 25°C to 65°C to avoid self-heating. From the curve, the TSP is found to be:

$$TSP = \frac{\Delta V}{\Delta T} = -2.55\ mV/K \quad (7.18)$$

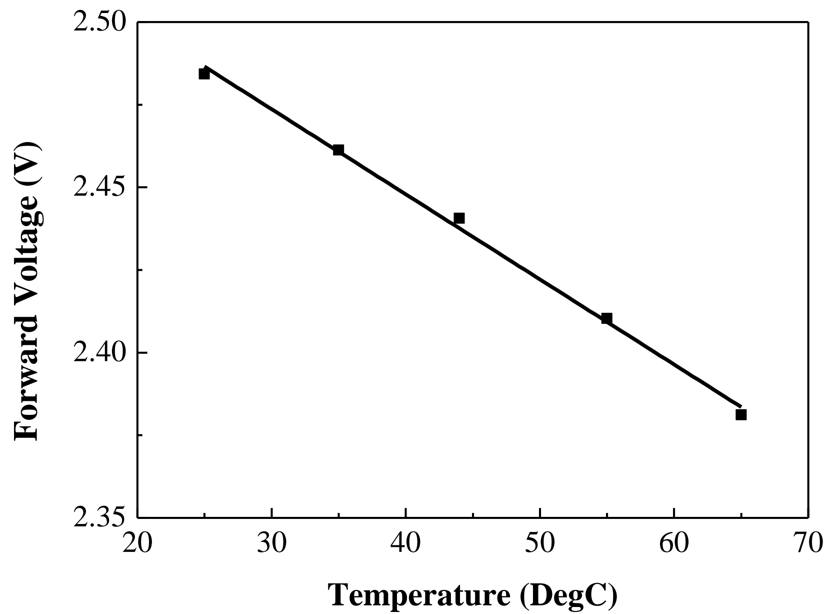


Fig. 7.37. Forward voltage versus temperature plot of the unpackaged LED die

The unpackaged blue LED die was placed on a cold plate at a set temperature of 25°C. Transient thermal measurement was carried out to record the cooling curve with a sensor current of 1 mA after driving the sample at its operating current of 350 mA for 5 minutes to reach thermal stabilization. The heated LED die was allowed to cool for 20s and its temperature during cooling recorded. The smoothed response of the cooling curve for the LED die is plotted in Fig. 7.38. The temperature of the die is observed to reach the steady state cold plate temperature in about 10s.

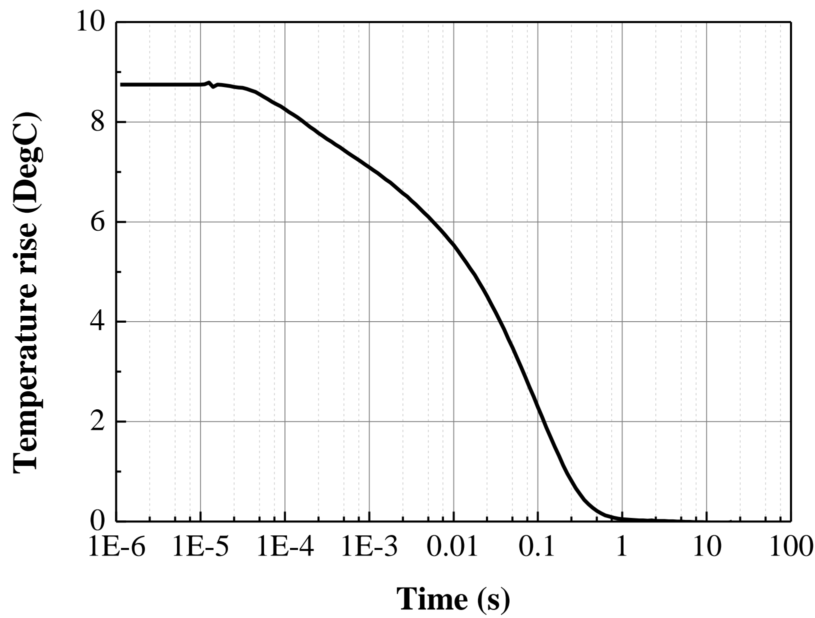


Fig. 7.38. Smoothed response of a cooling curve of the blue LED die

The cumulative structure function that describes the thermal resistance of an unpackaged blue LED die is presented in Fig. 7.39. The emitted optical power, P_{opt}, is obtained from the spectral flux Fig. 7.20 measured using an integrating hemisphere, and found to be 0.343W. Using (7.14), ΔP_T = 1.003W at the driving current of 350 mA.

In Fig. 7.39, the apparent total thermal resistance, R_{ja}, of the unpackaged LED die assuming all electrical power input P_T is converted into heat, is evaluated to be 8.87 K/W. By taking into consideration P_{opt}, the real total thermal resistance, $R_{ja,real}$, is evaluated to be 13.5K/W which is an increase of approximately 52%.

Therefore, the junction temperature of the unpackaged LED die at 350mA is:

$$T_j = R_{ja,real}(\Delta P_T - \Delta P_{opt}) + T_a = 33.9^oC \qquad (7.19)$$

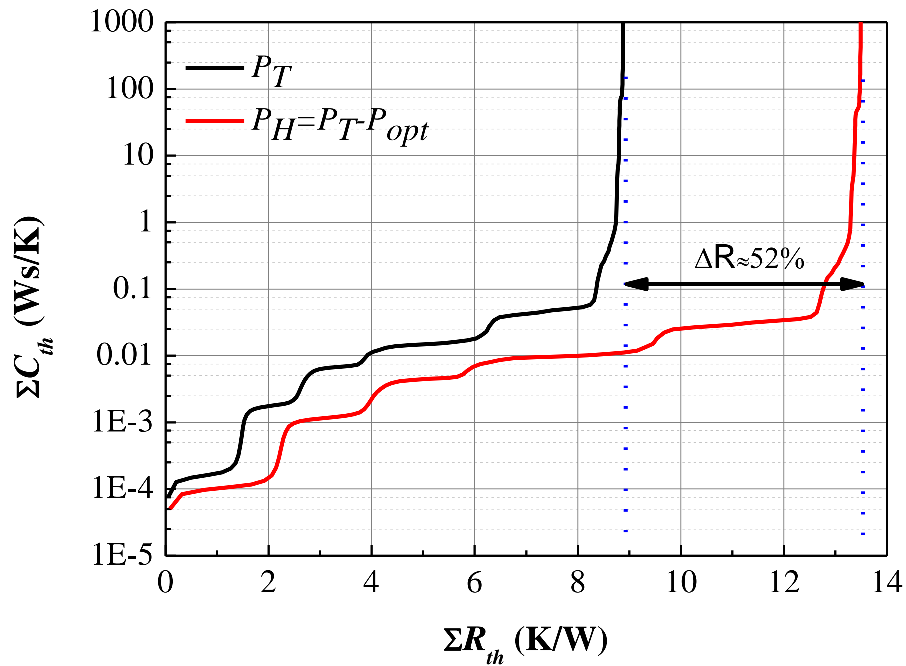


Fig. 7.39. Cumulative structure function for an unpackaged LED die with driving current of 350mA at ambient temperature of 25°C

From the cumulative structure function, it can be seen that there are at least 11 layers present in the LED die. A line scan across the cross-section of the LED die using SEM/EDX was carried out to identify the materials within the LED die. The SEM/EDX has a spot size of 3 μm. The materials and thicknesses identified from the line scan are shown in Fig. 7.40.

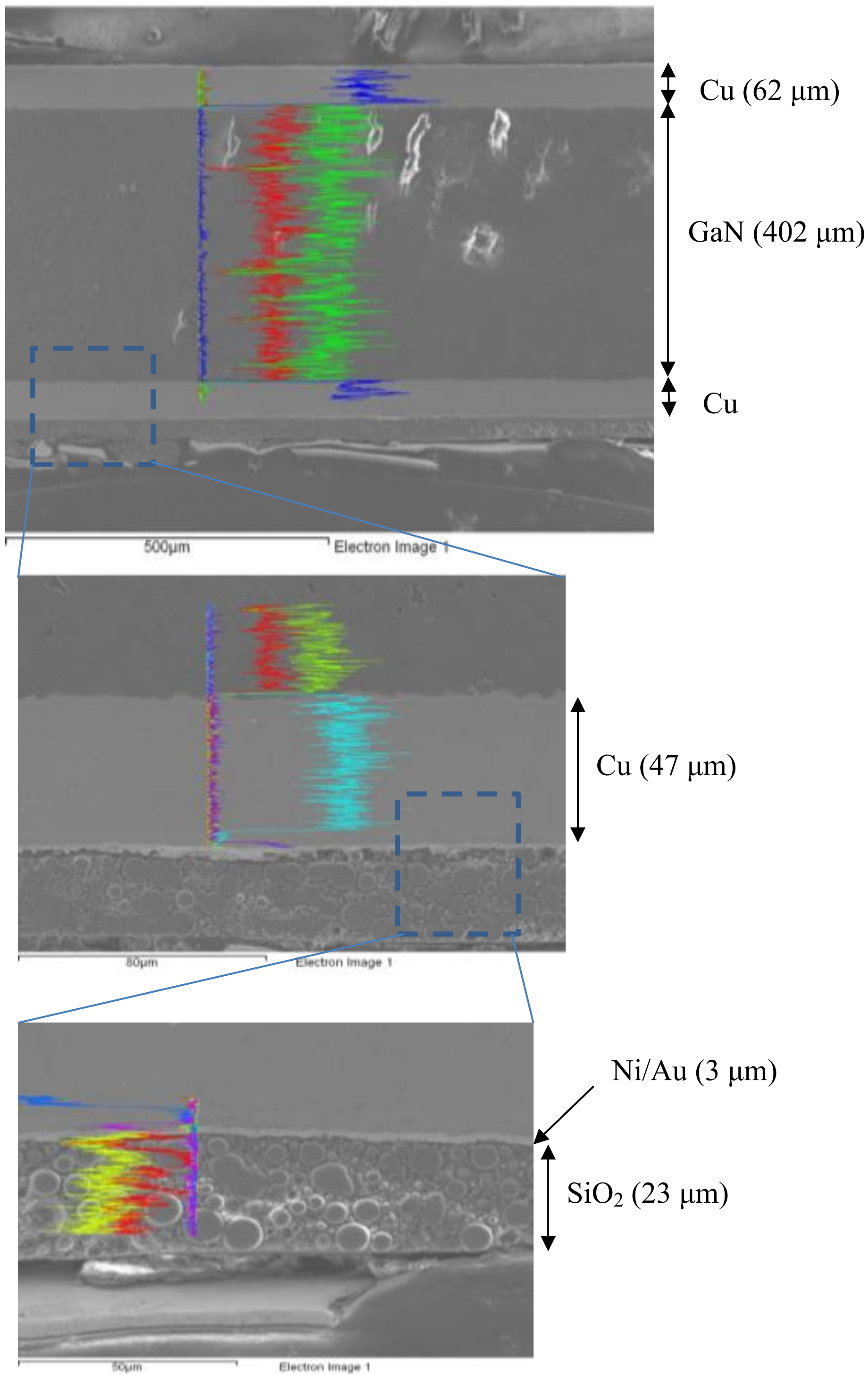


Fig. 7.40. Material stack-up configuration of the unpackaged blue LED die obtained using SEM/EDX

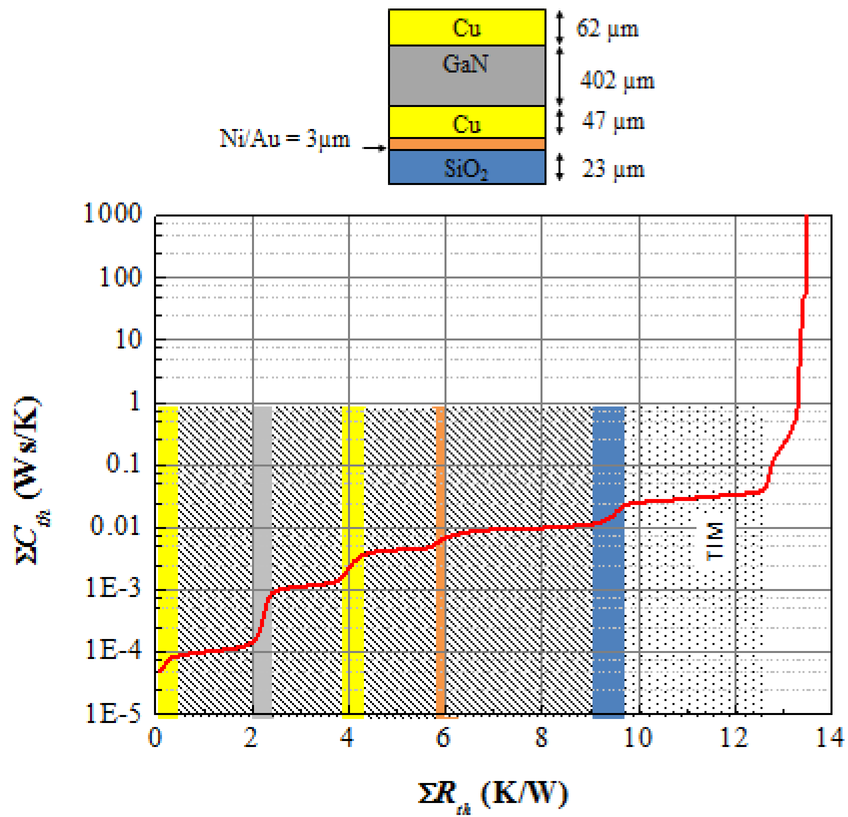


Fig. 7.41. A schematic cross-sectional side view of an unpackaged blue LED die

A schematic cross-sectional view of the material stack-up configuration of the LED is shown in Fig. 7.41. The following materials are present in the LED die:

- Top layer = 1st copper layer of thickness 62 µm
- 2nd layer = GaN of thickness 402 µm
- 3rd layer = 2nd copper layer of thickness 47 µm
- 4th layer = Ni/Au of thickness 3 µm
- 5th layer = SiO of thickness 23 µm
- Thermal interface material (TIM) between the LED die and the cold plate

The thermal resistance of the different layers present in the LED die identified by the different colours segments are shown in the cumulative structure function (Fig. 7.41). Each coloured segment in Fig. 7.41 corresponds to the respective layers in the picture of the LED die with the same colour.

The contact between each layer was found to be imperfect. From the cumulative structure function (Fig. 7.41), the thermal interface resistance values between each layer of material can be determined.

7.7. Summary of Experimental Measurement of LED Temperatures

IRT and TRT have been used to measure the surface temperatures of three types of LEDs. The forward voltage method has been used to measure the junction temperature of LEDs. Similarly, junction temperatures of LEDs were also determined from the thermal resistance of LEDs measured using T3ster. The three LEDs are:

(i) White phosphor-converted LED package with phosphor incorporated in the encapsulant (PIE LED package);

(ii) White phosphor-converted LED package with chip-level-conversion (CLC LED package); and

(iii) Unpackaged blue LED die

There was difficulty in measuring the LED die temperature of (i) using TRT due to phosphor incorporated in the encapsulating material making it opaque to visible light. On other hand, the encapsulating material of (ii) was transparent to visible light and TRT could be used. The temperature values measured for LED (ii) and (iii) are summarized in Table 7.1 and Table 7.2.

Table 7.1. Junction/surface temperature of white phosphor chip level converted LED package using different thermal characterization techniques

Thermal Characterization Technique	Measured Parameter	Junction/Surface Temperature
Forward voltage method	Slope = -1.77×10^{-3}V/^{o}C	56.5^{o}C
Thermal resistance measurement	$R_{ja,real}$ = 28.8K/W	53.5^{o}C
TR thermography	C_{TR}=7.12x10^{-5} K^{-1}, ΔT=25.4degC	50.4^{o}C
IR thermography	ε = 0.64	49.0^{o}C

Table 7.2. Junction/surface temperature of an unpackaged LED die using different thermal characterization technique

Thermal Characterization Technique	Measured Parameter	Junction/Surface Temperature
Thermal resistance measurement	$R_{ja,real}$ = 13.5K/W	33.9^{o}C
TR thermography	C_{TR}=1.71x10^{-5} K^{-1}, ΔT=11.7^{o}C	36.7^{o}C
IR thermography	ε = 0.18	48.0^{o}C

Taking results obtained from the T3ster as a reference, it is observed that the measured temperatures obtained using TRT gave close agreement with those obtained from thermal resistance measurement. Similarly, measured temperature using the forward voltage method gave close agreement with the temperature measured using the T3ster. Due to low emissivity of LED die surface, doubts on transmittance and reflectance of the encapsulation material present in a LED package, there is uncertainty on the accuracy of the measured temperatures obtained using IR thermography.

7.8. Comparison of Measured Temperature of Unpackaged LED die with Numerical and Analytical Methods

In this section, the measured temperature of the unpackaged LED die in section 7.5.3 using TRT and T3ster will be compared with calculated temperatures using both the FE method and the analytical method.

7.8.1. Thermal Modelling of the Unpackaged LED die

a. Description of the Thermal Model

In this section, the thermal model of the unpackaged LED die will be presented. The LED die has a dimension of 4mm x 4mm (Fig. 7.42). The material stack-up configuration is shown in Fig. 7.43. The thickness for each layer measured using SEM/EDX (Fig. 7.40) was modelled. From the measured thermal resistance values obtained using the T3ster (Fig. 7.41), the actual thermal conductivity values for each layer is tabulated in Table 7.3 and used in the thermal model (Fig. 7.44). In Fig. 7.44, only half of the geometry of the LED die was modelled due to the symmetry of the problem. As the thermal conductivity of GaN is usually temperature dependent, another thermal model that has incorporated the temperature dependent thermal conductivity of GaN (Table 3.3) was also modelled. The thermal interface resistance values between each layer measured by the T3ster (Table 7.4) were included in both the thermal models.

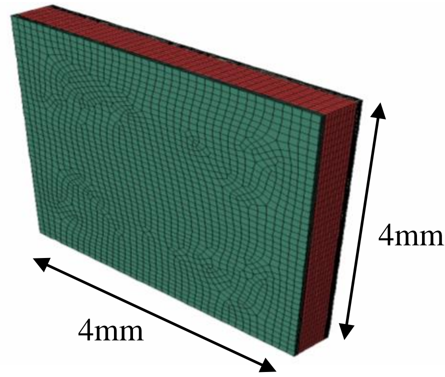


Fig. 7.42. Three-dimensional thermal model of the unpackaged LED die

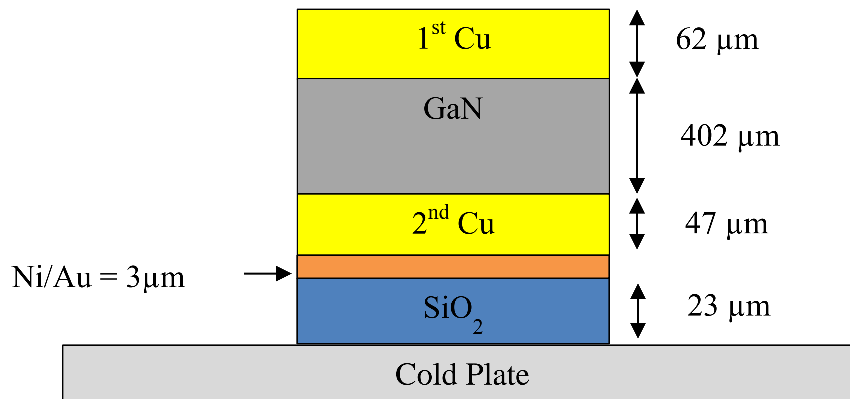


Fig. 7.43. A schematic diagram of the material stack-up configuration of the unpackaged LED die on a cold plate

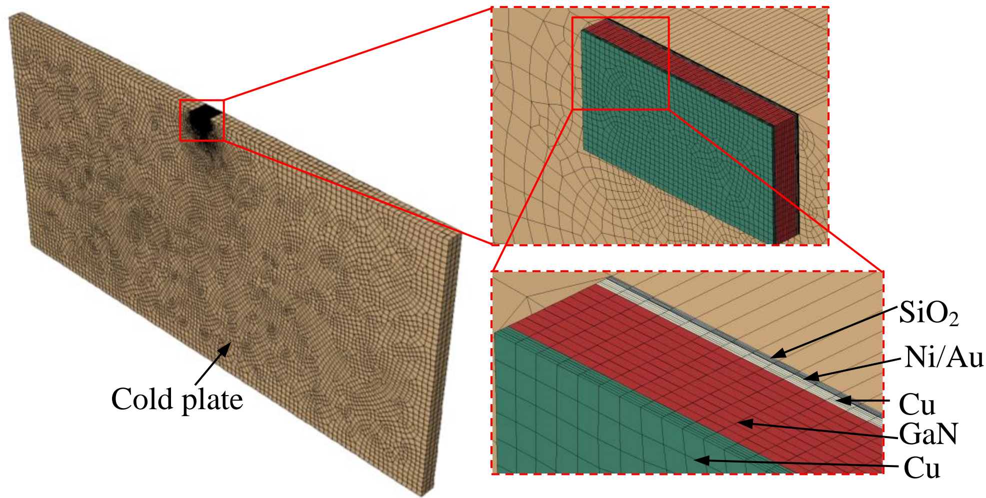


Fig. 7.44. Three-dimensional half thermal model of the unpackaged LED die on a cold plate

Table 7.3. Calculated thermal conductivities of materials present in the unpackaged blue LED die

Material	Measured Thermal Resistance (K/W)	Calculated Thermal Conductivity (W/mK)
1st Copper layer	0.31	12.38
2nd Copper layer	0.39	7.59
GaN	0.38	66.82
Ni/Au	0.24	0.79
SiO_2	0.84	1.71

Table 7.4. Thermal interface resistance between each layer measured using the T3ster

Interfaces	Measured Thermal Interface Resistance (K/W)
Between GaN and 1st Cu layer	1.60
Between GaN and 2nd Cu layer	1.50
Between 2nd Cu and Ni/Au	1.51
Between SiO2 and Ni/Au	3.10

Due to non-radiative recombination and resistive losses, heat is generated in the active region of an LED. A uniform surface heat flux is modelled on the

top surface of the GaN layer. From section 7.6.4, the total heat flux at driving current of 350mA is measured to be 0.66W. Therefore, the surface heat flux modelled is $0.66/(4mm)^2 = 0.04125W/mm^2$. Due to high thermal resistance between the active region and the air, heat is mostly transferred from the active region to the substrate. Therefore, heat conduction from the active region to the air was neglected [100, 117]. All other surfaces of the LED die were assumed to be at adiabatic condition except for the base of the LED die. The LED die was placed on a cold plate at 25°C (Fig. 7.36). From the cumulative structure function (Fig. 7.41), the thermal interface resistance between the cold plate and the base of the LED die was measured to be 2.80K/W.

b. Numerical Results

The temperature distribution of the unpackaged LED die on a cold plate is shown in Fig. 7.45. From the FE solution, the junction temperatures obtained by considering GaN with constant thermal conductivity and temperature dependent thermal conductivity are 32.0 ^{o}C and 32.1 ^{o}C, respectively. It is noted that the top surface of the LED die, i.e. the top surface of the 1st Cu layer, has the same temperature as the active region of the GaN substrate, i.e. the top surface of the GaN substrate. Neglecting the 1st Cu layer in the thermal model, it was found that the 1st Cu layer has negligible effect on the junction temperature of the LED die due to its small thickness.

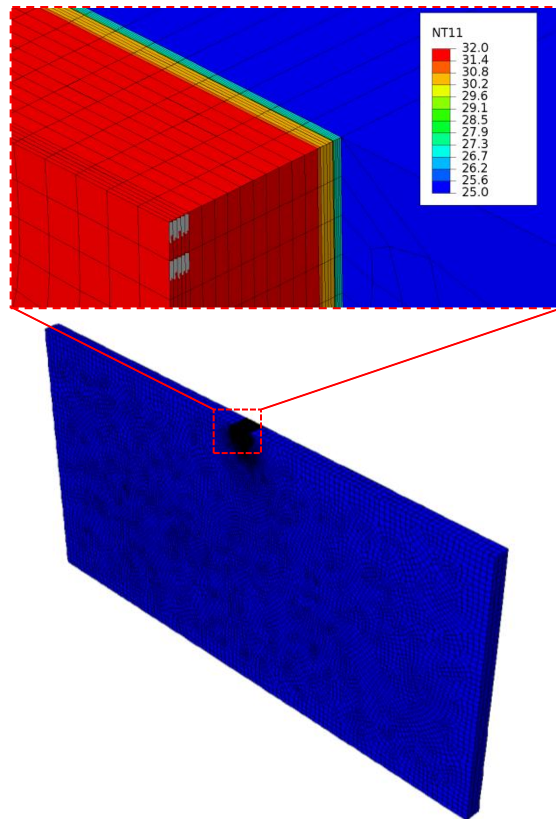


Fig. 7.45. Temperature distribution of the three-dimension unpackaged LED die

7.8.2. Analytical Method for Calculating the Junction Temperature of the Unpackaged LED die

In this section, the junction temperature of the unpackaged LED die will be calculated using the analytical method. To begin with, an analytical solution for calculating the temperature distribution due to a surface planar heat source with temperature dependent thermal conductivity will be formulated. From (4.32), the problem is solved for a planar heat source by changing the limits of the integration. Using the derived analytical solution, the junction temperature of the unpackaged LED die will be calculated.

a. Problem Description

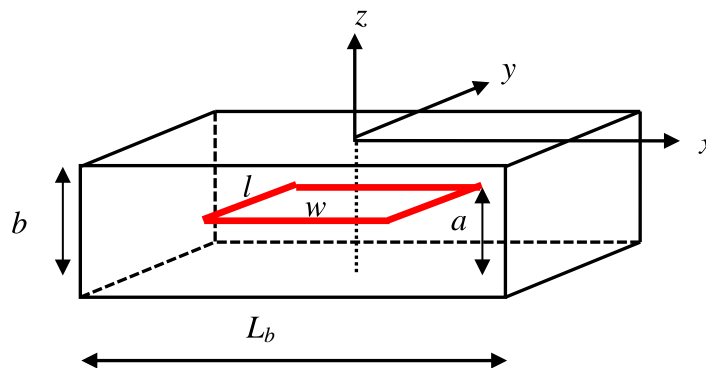


Fig. 7.46. Substrate subjected to an embedded surface planar heat source and a base at a constant temperature. The remaining surfaces are assumed adiabatic

Consider a planar heat source of dimension l x w embedded in a substrate of thickness b as shown in Fig. 7.46. The heat source is located at a distance a from the base of the substrate with its center coinciding with the center of the substrate. The thermal conductivity k is assumed to be temperature dependent. The following assumptions are made:

7) The sides and the top surfaces of the substrate are adiabatic. Due to high thermal resistance between the active region of the LED die and the air, heat is mostly transferred from the active region to the substrate [100]. Therefore, heat transfer from the active region to the air is neglected.
8) The bottom of the substrate is an isothermal surface at constant temperature T_o.
9) An embedded planar heat source of uniform heat flux λ_{area} and of dimension l x w is assumed.
10) The substrate has a temperature dependent thermal conductivity (which is often the case for almost all semiconductor materials).

b. Formulation

In this section, the steady-state three-dimensional temperature due to a planar heat source embedded in a solid of temperature dependent thermal conductivity will be developed. The Green's function integral method for a point heat source will be employed.

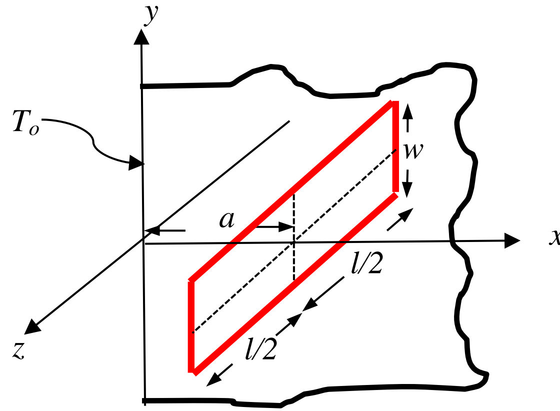


Fig. 7.47. Temperature distribution of the three-dimension unpackaged LED die

Consider a planar heat source of finite length *l* and width *w*, embedded in a semi-infinite three dimensional solid $x > 0$, $-\infty < y < \infty$ and $-\infty < z < \infty$ with temperature dependent thermal conductivity (Fig. 7.47). The heat generation per unit area of the planar heat source is assumed to be constant, with the boundary at $x = 0$ maintained at constant temperature, T_o.

From (4.32),

$$\theta(\vec{x},\vec{x'}) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\int_{0}^{\infty}\frac{1}{4\pi k(T_O)}\left[\frac{1}{r_1}-\frac{1}{r_2}\right]Q(\vec{x})\,dx'dy'dz' \qquad (7.20)$$

where $\theta(\vec{x},\vec{x'})$ is the transformed dependent variable in terms of *T*.

From the Heaviside step function, $H\left[y' - \frac{w}{2}\right]$ and $H\left[y' + \frac{w}{2}\right]$, $H\left[z' - \frac{l}{2}\right]$ and $H\left[z' + \frac{l}{2}\right]$, the total heat generation, Q, due to a planar heat source of area l x w at distance a from the boundary (Fig. 7.47) is expressed as:

$$Q\left(\overrightarrow{x'}\right) = \lambda_{area}\delta(x'-a)\left\{H\left[y'+\frac{w}{2}\right] - H\left[y'-\frac{w}{2}\right]\right\}\left\{H\left[z'+\frac{l}{2}\right] - H\left[z'-\frac{l}{2}\right]\right\} \tag{7.21}$$

where λ_{area} is the heat dissipation per unit area (W/m^2).

Therefore,

$$\theta\left(\vec{x},\overrightarrow{x'}\right) = \int_{-\infty}^{\infty}\int_{-\infty}^{\infty}\int_{0}^{\infty}\frac{1}{4\pi k(T_o)}\left[\frac{1}{r_1} - \frac{1}{r_2}\right]\lambda_{area}\delta(x'-a)\left\{H\left[y'+\frac{w}{2}\right] - H\left[y'-\frac{w}{2}\right]\right\}\left\{H\left[z'+\frac{l}{2}\right] - H\left[z'-\frac{l}{2}\right]\right\}dx'dy'dz' \tag{7.22}$$

From the properties of the Dirac delta function and substituting (4.30) into (7.22):

$$\theta\left(\vec{x},\overrightarrow{x'}\right) = \frac{\lambda_{area}}{4\pi k(T_o)}\int_{-\frac{l}{2}}^{\frac{l}{2}}\int_{-\frac{w}{2}}^{\frac{w}{2}}\left[\frac{1}{\sqrt{(x-a)^2+(y-y')^2+(z-z')^2}} - \frac{1}{\sqrt{(x+a)^2+(y-y')^2+(z-z')^2}}\right]dy'dz' \tag{7.23}$$

$$\theta\left(\vec{x},\overrightarrow{x'}\right) = \frac{\lambda_{area}}{4\pi k(T_o)}\int_{-\frac{l}{2}}^{\frac{l}{2}}\left[\ln\left[(y-y') + \sqrt{(x+a)^2+(y-y')^2+(z-z')^2}\right] - \ln\left[(y-y') + \sqrt{(x-a)^2+(y-y')^2+(z-z')^2}\right]\right]_{-\frac{w}{2}}^{\frac{w}{2}}dz' \tag{7.24}$$

Equation (7.24) can be integrated easily to obtain a closed-form solution (Appendix A):

$$\theta(\vec{x},\vec{x'}) = \frac{\lambda_{area}}{4\pi k(T_o)}(I_1 - I_2 - I_3 + I_4) \tag{7.25}$$

Substituting (7.25) into (4.5), the three-dimensional temperature distribution due to a planar heat source embedded in a semi-infinite solid can be calculated:

$$T = \left[{T_o}^{1-\alpha} + \frac{1-\alpha}{{T_o}^{\alpha}}\frac{\lambda_{area}}{4\pi k(T_o)}(I_1 - I_2 - I_3 + I_4)\right]^{\frac{1}{1-\alpha}} \tag{7.26}$$

To relate the analytical solution (7.26) with the problem described in Fig. 7.46, transformation of coordinates and method of images can be carried out (refer to section 4.2.4 for more detail). Therefore, the temperature distribution in Fig. 7.46 can be calculated by:

$$T(x,y,z) = T_1(b+z, x-d, y) + T_1(b-z, x-d, y) - T_o \tag{7.27}$$

From (7.27), it can be seen that the analytical solution is based on the design parameters such as the substrate thickness, size of substrate and material properties. Therefore, it is possible to understand the impact of design parameters on the operating junction temperature without having to go through numerical simulations.

c. Junction Temperature of the Unpackaged LED die calculated using the Analytical Method

In this section, the junction temperature of the unpackaged LED die in section 7.5.3 will be calculated using the analytical method (7.27). The active region of an LED occurs on the top surface of the GaN substrate and is approximately

the same area as the LED die (Fig. 7.48). Therefore, the substrate of the LED die conducts the heat but does not act as a heat spreader [100].

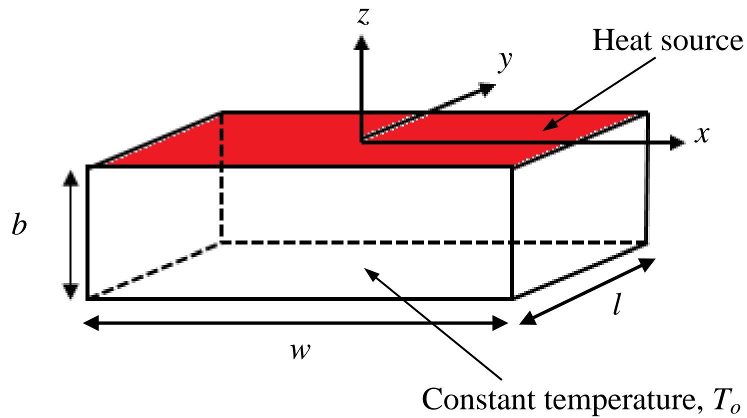


Fig. 7.48. A surface planar heat source in an LED at chip level

As shown in Fig. 7.43, the LED die consists of several layers with different thermal conductivity values and thermal interface resistance between each layer. From the thermal resistance measurement, the LED die can be represented by the thermal resistance network shown in Fig. 7.49.

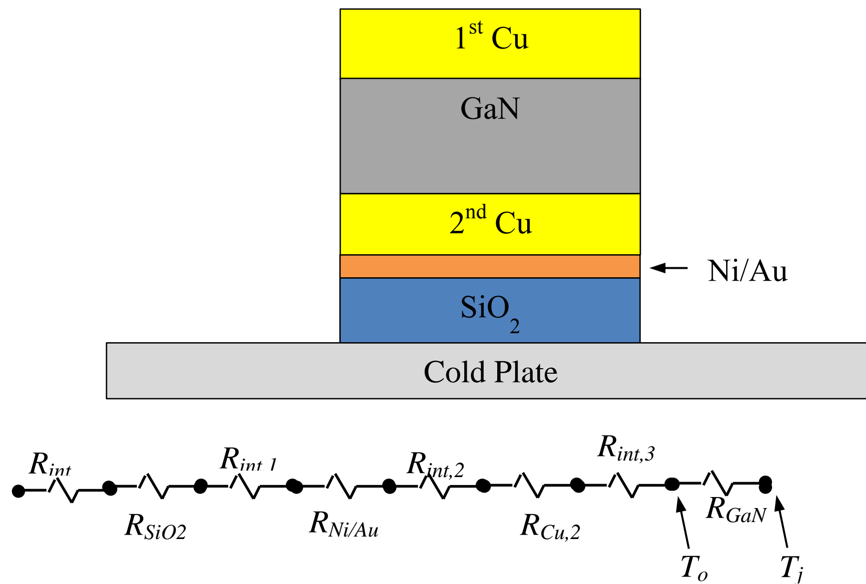


Fig. 7.49. A schematic cross-section of the LED die and the equivalent thermal resistance network

From the numerical solution, it was found that the 1st Cu layer has negligible effects on the junction temperature due to its small thickness. Therefore, the thermal resistance network (Fig. 7.49) consists of:

- thermal interface resistance between the SiO_2 layer and the cold plate (R_{int} = 2.7957K/W)
- thermal resistance of the SiO_2 layer (R_{SiO2})
- thermal interface resistance between the SiO2 and Ni/Au layer ($R_{int,1}$)
- thermal resistance of the Ni/Au layer ($R_{Ni/Au}$)
- thermal interface resistance between the Ni/Au layer and the 2nd Cu layer ($R_{int,2}$)
- thermal resistance of the 2nd Cu layer ($R_{Cu,2}$)
- thermal interface resistance between the 2nd Cu layer and the GaN layer ($R_{int,3}$)
- thermal resistance of the GaN layer (R_{GaN})

The thermal resistance and thermal interface resistance values due to subsequent layers are shown in Table 7.3 and Table 7.4. From the thermal resistance network shown in Fig. 7.49, the base temperature, T_o, of the GaN substrate is found to be 31.8 ^{o}C. To calculate the junction temperature of the LED die, the temperature dependent thermal conductivity (Table 3.3) for GaN was used. Substituting T_o into (7.27) and by considering one row of image sources at the lateral face to account for the adiabatic boundary condition at the edge (Fig. 4.14), the junction temperature of the LED die was calculated to be 32.1 ^{o}C.

7.8.3. Comparison of Results

In this section, the measured temperatures of the unpackaged LED die obtained by using the TRT and the thermal resistance measurement will be compared with temperatures calculated using the FE method and the present analytical method. The results are tabulated in Table 7.5 where it can be seen that the junction temperature calculated using the present analytical method and numerical results agree better correlates well with the FE solution, and both analytical and numerical results agree better with the thermal resistance result than the TRT result.

Table 7.5. Comparison of measured and calculated junction temperatures

	Junction Temperature
Thermal resistance measurement	33.9^{o}C
TR thermography	36.7^{o}C
FE method	32.0^{o}C
Analytical method	32.1^{o}C

7.9. Comparison of Numerical Solution with Analytical Solution for a Single Chip LED Package [117]

In this section, the junction temperature of the single chip LED package shown in [117] is calculated using the derived analytical method (7.27) and compared with the numerical solution presented in [117].

a. Description of the single chip LED package

In Fig. 7.50, the GaN LED chip is attached to a Si die using Au-Sn eutectic bonding. The Si die is solder attached using Au-Sn to a printed circuit board (PCB) that consists of 3 layers, i.e. copper circuit layer, ceramic layer (AlN) and the copper base layer. The packaged LED is attached to a heat sink using thermal grease as the thermal interface material (TIM). The structure and dimensions of the heat sink is shown in Fig. 7.51. The dimensions and thermal conductivities of materials are summarized in Table 7.6 [117].

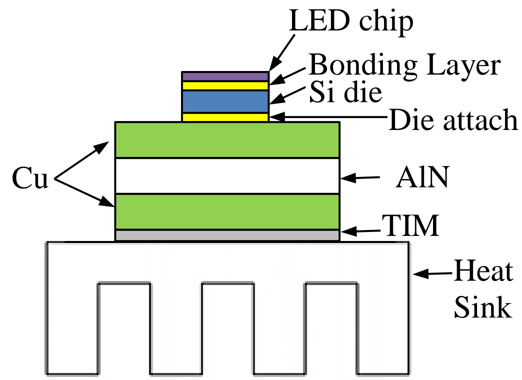


Fig. 7.50. A schematic cross-section of the single chip LED package on a heat sink

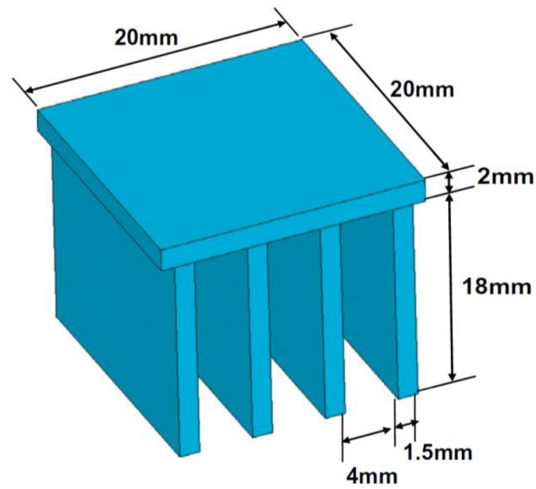


Fig. 7.51. The structure and dimensions of the heat sink [117]

Table 7.6. Dimensions and thermal conductivity values of materials

Material	Thickness (μm)	Dimension (mm)	Thermal Conductivity (W/mK)
GaN LED chip	4	1 x 1	130
Si die	375	1 x 1	124
Copper	127	10 x 10	385
Ceramic layer (AlN)	381	10 x 10	180
Au-Sn	50	1 x 1	57
TIM	50	10 x 10	3

b. Calculation of the junction temperature using the present analytical method

In this section, the junction temperature of the single chip LED package will be calculated using the present analytical method (7.27). In [117], the LED chip and the Au-Sn eutectic bonding have been excluded from the thermal model due to the very small thickness of these layers and thus have negligible effects on the overall thermal resistance of the LED package. Hence, a uniform heat flux of $1W/mm^2$ was applied on the top surface of the Si die (Fig. 7.52). All surfaces of the LED package were assumed to be adiabatic except for the top surface of the Si die and fins of the heat sink (Fig. 7.52). A uniform connective heat transfer coefficient, h = $10W/m^2K$, at 25^oC ambient

temperature was assumed at the fins of the heat sink. The equivalent thermal resistance network of the LED package shown in Fig. 7.52 consists of:

- Thermal resistance between the fins of the heat sink and ambient (R_{fin})
- Spreading thermal resistance of the base of the heat sink (R_{hs})
- Thermal resistance of the TIM (R_{TIM})
- Thermal resistance of the copper base layer ($R_{Cu,2}$)
- Thermal resistance of the ceramic layer (R_{AlN})
- Spreading thermal resistance of the copper circuit layer ($R_{Cu,1}$)
- Thermal resistance of the die attach (R_{attach})
- Thermal resistance of the Si die (R_{Si})

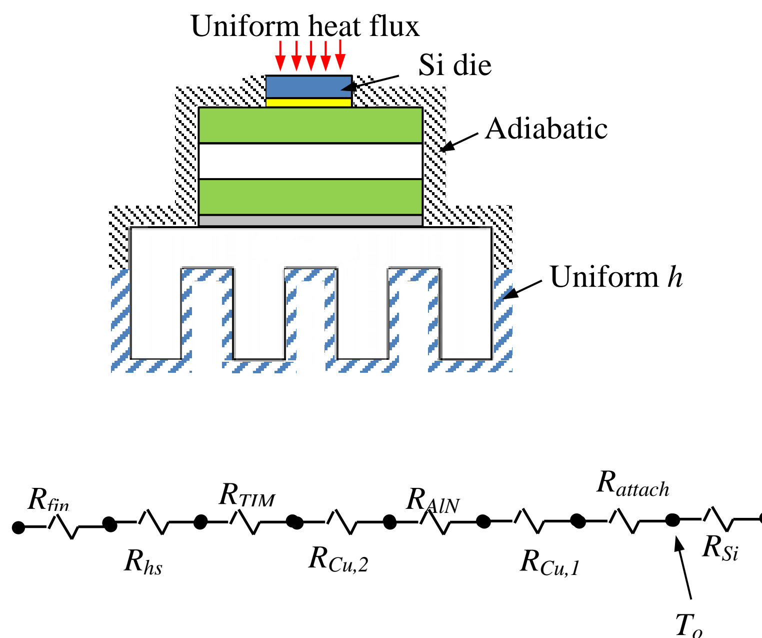


Fig. 7.52. Boundary conditions of the single chip LED package and the equivalent thermal resistance network

The thermal resistance of the heat sink consists of two components, i.e. the spreading thermal resistance of the base of the heat sink, R_{hs}, and the thermal resistance between the fins of the heat sink and ambient, R_{fin}.

The thermal resistance between the fins of the heat sink and ambient, R_{fin}, can be determined by [50]:

$$R_{fin} = \frac{1}{hA_{fin}} \tag{7.28}$$

where A_{fin} is the total surface area of the fin.

From Fig. 7.51, A_{fin} is calculated to be 3.496x10^{-3}m^2. Therefore, R_{fin} = 28.6K/W.

To determine the spreading thermal resistance of the base of the heat sink, R_{hs}, we first consider a uniform heat flux on a same cross-sectional area as the TIM, i.e. 10mm x 10mm, on the top surface of the heat sink (Fig. 7.53).

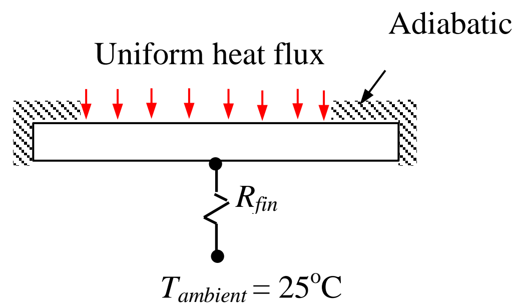


Fig. 7.53. Spreading resistance model of the heat sink

Using (5.1), R_{hs} = 0.3271K/W.

From R_{TIM} to R_{AlN}, the thermal resistance values can be calculated using the one-dimensional thermal resistance model:

$$R = \frac{L}{kA} \tag{7.29}$$

where R is the thermal resistance across the thickness, L, of the material and A is the cross-section area. Therefore, R_{TIM} = 0.166K/W, $R_{Cu,2} = 3.299\text{x}10^{-3}$, R_{AlN} = 0.021 K/W.

To determine the spreading thermal resistance of the copper circuit layer, $R_{Cu,1}$, consider a uniform heat flux of on a same cross-sectional area as the Si die, i.e. 1mm x 1mm, on the top of the heat sink. Using (5.1), $R_{Cu,1}$ is calculated to be 0.261 K/W.

To determine R_{attach}, (7.29) can be used. Therefore, R_{attach} = 0.877K/W. The base temperature of the Si die, T_o, can be determined from the thermal resistance network, i.e. $T_o = R_{total} \text{ x } Q + T_{ambient} = (R_{fin} + R_{hs} + R_{TIM} + R_{Cu,2} + R_{AlN} + R_{Cu,1} + R_{attach}) \text{ x (1W)} + 25^{o}\text{C} = 55.3^{o}\text{C}$.

For materials with constant thermal conductivity, the temperature distribution due to a planar heat source can also be calculated by substituting $\alpha = 0$ into (7.27). Substituting $T_o = 55.3^{o}$C and $\alpha = 0$ into (7.27), the calculated junction temperature by considering one row of image sources at the lateral face to account for the adiabatic boundary condition at the edge (Fig. 4.14) is 60.1^{o}C. From the numerical solution [117], the junction temperature calculated is 60.3^{o}C. From this comparison, the junction temperature obtained by using (7.27) has shown very good correlation with the calculated junction temperature obtained from the numerical solution.

7.10. Conclusion

In this work, the peak surface temperatures of LEDs die have been measured using IR and TR thermography. The junction temperatures of LED dies were measured using the forward voltage method and inferred from the thermal resistance measurements make using a T3ster. Thermoreflectance coefficient value of the measured LED die surface needs to be characterized before any quantitative deduction can be made on the measured temperature. The measured temperatures using TR thermography have been verified with thermal resistance measurement. It has been shown that thermoreflectance (TR) thermography is able to thermally characterize both unpackaged and packaged LED. The only limitation with using TR thermography is that the encapsulating material of a packaged LED has to be transparent to the light source used in the TR Analyser.

An analytical method for predicting the junction temperature due a planar heat source embedded in a substrate has been presented. This analytical method was formulated from (4.32) developed in Chapter 4 by changing the limits of integration. The calculated junction temperature obtained using the derived analytical solution by considering a surface planar heat source has shown good agreement with the measured temperatures and the numerical solution. Since the analytical solution is based on design parameters such as the substrate thickness, size of substrate and material properties, it is possible to understand the impact of design parameters on the operating junction temperature without having to go through numerical simulations.

CHAPTER 8

CONCLUSION

8.1. Conclusion

Understanding the thermal issues associated with high power electronic devices is important for improving the performance and reliability of these devices. The failure mechanisms in many integrated circuit packages have been found to be dependent upon temperature gradients, magnitude of temperature cycles, rate of temperature change, and absolute temperature. Therefore, the device operating temperature must be controlled to meet both the performance and reliability requirements.

There are several ways to obtain the peak operating junction temperature in these devices. The numerical approach is commonly used to predict the peak operating junction temperature and the temperature gradients in a device. This requires a knowledge of the die attach and packaging techniques as well as the device geometry and layout. Numerical methods include finite elements, finite differences and boundary elements. Thermal models of power amplifier FETs and MMICs involve modelling of sub-micron geometric features as well as the heat dissipation region generated due to biasing of the device. Precisely defining where the heat is generated in the channel is difficult as the heat dissipation region is dependent on the bias voltage applied to the gate which creates a depletion region and locally changes the resistivity of the semiconductor materials. The accuracy of a thermal model is ultimately

dependent on how well the model represents the actual system and the accuracy of the modelled heat dissipation region.

There has been many works done on MMIC thermal modelling and the accuracy of some thermal models had been verified by measured temperatures. Heat dissipation were typically modelled as a volumetric heat source or a planar heat source. A volumetric heat source (VHS) was usually modelled to be embedded in the substrate under the gate. From the literature, the depth of the VHS embedded in the substrate and the size of the VHS differ across all publications. Similarly, a planar heat source (PHS) was modelled either on the surface or embedded in the substrate.

There are several publications which study modelling of the heat dissipation region in high power electronic devices. However, the differences between all the various models proposed have not yet been studied. In this work, the effects of geometric parameters of the heat dissipation region on the maximum junction temperature of a PA MMIC are studied. The maximum junction temperatures obtained from both VHS and PHS models calculated using the finite element method were compared. From this study, it was shown that a small change in the size and depth of the heat dissipation region and power distribution in the depletion region has a significant effect on the predicted junction temperature. Through this sensitivity study, a baseline model was adopted to represent the heat dissipation region. The accuracy of this baseline model was verified by comparing the temperatures measured using thermoreflectance thermography.

Besides numerical methods, much work has also been done on developing analytical methods to calculate the junction temperature. Compared to numerical methods, analytical methods require much shorter computational time. Since analytical methods give closed-form expressions of the junction temperature in terms of the device geometry and material properties, they enable one to determine the effect of device geometry and material properties easily and more directly. Although analytical methods have disadvantages in terms of flexibility of the boundary conditions compared to numerical methods, it is still beneficial to use analytical methods to calculate the junction temperature in the early design stage.

Several techniques had been used in previous works to develop analytical solutions to solve for the temperature distribution in FETs and MMICs devices. They are Fourier series, Fourier transformation and Green's Function method evolved from eigenfunction expansions. However, the resulting double infinite series which appear in the solutions in most of the previous works often present convergence problems and can be extremely slow, resulting in very long computation times. Furthermore, inaccurate representation of the heat dissipation region in high-power microwave devices by a surface planar heat source was often assumed in the past analytical models for simplicity.

In addition, many analytical solutions developed to solve for the temperature distribution in FETs had assumed a constant uniform temperature at the base of the substrate. Unfortunately, the base temperature of the substrate is often unknown in a packaged device and is not uniform at all but has a bell-shaped

distribution. The substrate of the MMIC device is usually attached to a carrier and a jig, where the base of the jig instead of the substrate is maintained at a constant temperature by a thermal chuck. A standard thermal resistance network can be used to calculate the temperature at the base of the substrate. However, it has been shown in this work that such a calculation is not very accurate.

In this work, a new closed-form analytical solution that is capable of calculating the junction temperature easily and accurately without the issue of convergence and long computation time has been developed. Fundamentally, it is based on the Green's function integral method on a point heat source developed through the method of images. Compared to previous works, the present analytical method is easier to implement, more accurate and reduces the computation time significantly. In addition, the exact location of the heat dissipation region can be easily taken into account for accurate estimation of the junction temperature. This work is also applicable to multi-finger devices by employing the superposition technique. The present method has been shown to be more accurate than previous analytical methods. The calculated junction temperatures agreed well with both the FEA results and experimental measurements. Therefore, this work will allow design parameters such as the gate length, gate pitch, location of heat sources and material property to be easily studied to investigate its effect on the peak junction temperature without having to go through the tedious modelling required by numerical methods.

To determine the peak operating junction temperature in a packaged device, a novel analytical method has also been developed to determine an accurate temperature distribution at the base of the substrate in a packaged device. It

was found that the temperature distribution at the base of the substrate of a packaged MMIC power amplifier can be well represented by a Lorentz distribution. From this distribution, a relationship between the maximum base temperature $T_{o,max}$ and the average base temperature $T_{o,avg}$ can be obtained as a function of the basic parameters of the device such as gate length, gate pitch, number of gates and substrate base dimensions. This method, together with the new closed-form solution developed earlier on for the temperature distribution within the substrate, has allowed the peak operating junction temperature to be determined easily and accurately by using the analytical approach. Furthermore, it has been shown that the predicted maximum gate temperatures agree very well with those calculated using FEA and those measured using thermoreflectance thermography.

The most direct method to determine the peak operating junction temperature in FETs and MMICs is by experimental techniques. Thermal characterization of devices plays an important role in determining their performance and reliability. An accurate temperature measurement can be used to validate a numerical model as well as to verify the accuracy of an analytical solution. There are several techniques available for measuring the temperature of MMIC devices. However, due to its submicron size gates, it is often challenging to obtain an accurate measurement of the gate temperature. When there is insufficient spatial resolution, the measured temperature will be lower than the actual peak gate temperature.

In this work, infrared thermography (IRT) and thermoreflectance thermography (TRT) have been used to measure the peak gate temperature of both GaAs and GaN power amplifier (PA) MMIC devices. An overview of the

principle and the methodology for both characterization techniques were presented. In addition, the challenges faced when using either technique to measure the gate temperature have also been discussed. The spatial resolutions for IRT and TRT used were 5 μm and 0.15 μm, respectively. Comparing with the gate size of 0.25 μm of the MMIC devices studied, it can be seen that the spatial resolution of IRT is grossly inadequate while that of TRT is adequate. The maximum gate temperatures calculated from the finite element analyses have correlated well with the temperatures measured using TRT. On the other hand, large discrepancies between IR measured gate temperatures and finite element solutions were observed which can be attributed to errors due to the inadequate spatial resolution or IRT as well as the presence of reflective and low emissivity surfaces in a PA MMIC. This work has demonstrated the potential of using TRT as an effective tool for thermal characterization of semiconductor devices which often have sub-micron size gates and reflective (low emissivity) surfaces that will pose difficulties in obtaining an accurate temperature measurement using IR thermography.

Lastly, thermal characterization of Light Emitting diodes (LEDs) was also carried out in this study. LEDs are a strong candidate for the next-generation general illumination applications due to its continuously improving eco-economic benefits over conventional lighting sources. End-users are tapping onto these benefits by further pushing the LED performance to its limits, with increased drive currents and thus, higher heat generation. The efficiency and reliability of high-brightness LEDs strongly depend on the successful thermal management of the junction temperature of the LED as it is the prime driver for its effective operation.

There are several methods available to predict the junction temperature of LEDs. TRT is a potential technique for measuring the surface temperature of the LED die since the encapsulation layer is transparent to the TR measurement wavelength. However, to date, no work has been done on using TRT to characterize the absolute junction temperature of a packaged LED in the visible range except for laser diodes.

Therefore in this work, the surface temperatures of both packaged and unpackaged LEDs die have been measured using IR and TR thermography. The junction temperature of LEDs was measured using the forward voltage method. Using a T3ster, the junction to ambient thermal resistance of LEDs was measured. From the thermal resistance measurement, the junction temperatures of LEDs were calculated and compared with the measured temperatures obtained using IRT, TRT and the forward voltage method. Through these comparisons, the TRT results were validated with the measured junction temperature obtained using the forward voltage measurement. Similarly, the TRT results correlate well with the inferred junction temperature from the thermal resistance measurement. This work has demonstrated the potential of using TRT as an alternative technique to measure the surface temperature of a packaged LED die. The only limitation with using TRT is that the encapsulating material of a packaged LED has to be transparent to light.

The principle used to derive a closed-form analytical solution for calculating the junction temperature of MMIC devices has also been used to derive an analytical solution for determining the junction temperature of an LED. It is applicable to materials with either constant or temperature dependent

conductivity. Using the derived analytical solution, the calculated junction temperature has shown good agreement with the measured temperatures, FE solutions and previous works. Since the analytical solution is based on design parameters such as the substrate thickness, size of substrate and material properties, it is possible to understand the impact of design parameters on the operating junction temperature without having to go through many tedious numerical simulations.

8.2. Recommendations for Future Work

In this work, analytical solutions have been developed for calculating the junction temperature of MMIC devices where heat sources are embedded in a substrate with large lateral dimensions. This work can be further extended to cases where heat sources are located near to the edge of the substrate by using the method of images to obtain adiabatic boundary condition at the edge.

In thermal characterization of LEDs, thermoreflectance (TR) thermography has been used to measure the surface temperature of both packaged and unpackaged LEDs. The measured temperatures were validated using the thermal resistance measurements and the forward voltage method. To further demonstrate that the TR thermography is a potential technique for measuring the surface temperature of LEDs in a packaged device, more testing on different samples of LEDs can be carried out.

8.3 Publications

In the course of this research work, the following conference proceedings have been published and two papers submitted for publication in journals:

Journals:

1. J.H.L. Ling and A.A.O. Tay, “A new analytical method for calculating maximum junction temperature of packaged devices incorporating the temperature distribution at the base of the substrate,” Accepted for publication in ASME Journal of Electronic Packaging, 2014.

2. J.H.L. Ling and A.A.O. Tay, “A new accurate closed-form analytical solution for junction temperature of high-powered devices,” Submitted to *Journal of Electronic Packaging*, 2013.

Conferences:

1. J.H.L. Ling, A.A.O. Tay, K.F. Choo and W. Chen, "Thermal characterization and modelling of a gallium arsenide power amplifier MMIC," *13th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm),* pp.440-445, 2012.
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4. J.H.L. Ling, A.A.O. Tay and K.F. Choo, "Accurate thermal characterization of a GaN PA MMIC using Thermoreflectance thermography," *14th International Conference on Electronic Packaging Technology and High Density Packaging (ICEPT-HDP),* 2013. **[Awarded Cisco Best Student Paper Award.]**

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APPENDIX A

EVALUATION OF $\boldsymbol{\theta(\vec{x}, \overrightarrow{x'})}$

From (7.25)

$$\theta(\vec{x}, \overrightarrow{x'}) = \frac{\lambda_{area}}{4\pi k(T_o)} \int_{-\frac{l}{2}}^{\frac{l}{2}} \ln\left[\left(y-\frac{w}{2}\right)+\sqrt{(x+a)^2+\left(y-\frac{w}{2}\right)^2+(z-z')^2}\right] - \ln\left[\left(y-\frac{w}{2}\right)+\sqrt{(x-a)^2+\left(y-\frac{w}{2}\right)^2+(z-z')^2}\right] - \ln\left[\left(y+\frac{w}{2}\right)+\sqrt{(x+a)^2+\left(y+\frac{w}{2}\right)^2+(z-z')^2}\right] + \ln\left[\left(y+\frac{w}{2}\right)+\sqrt{(x-a)^2+\left(y+\frac{w}{2}\right)^2+(z-z')^2}\right] dz' \tag{A1}$$

Let I_1 equal to

$$I_1 = \int_{-\frac{l}{2}}^{\frac{l}{2}} \ln\left[\left(y-\frac{w}{2}\right)+\sqrt{(x+a)^2+\left(y-\frac{w}{2}\right)^2+(z-z')^2}\right] dz' \tag{A2}$$

$$I_1 = \left[-(z-z')\ln\left[\left(y-\frac{w}{2}\right)+\sqrt{(x+a)^2+\left(y-\frac{w}{2}\right)^2+(z-z')^2}\right] - \left(y-\frac{w}{2}\right)\ln\left[(z-z')+\sqrt{(x+a)^2+\left(y-\frac{w}{2}\right)^2+(z-z')^2}\right] + (x+a)\tan^{-1}\left[\frac{\left(y-\frac{w}{2}\right)(z-z')}{(x+a)\sqrt{(x+a)^2+\left(y-\frac{w}{2}\right)^2+(z-z')^2}}\right] - (x+a)\tan^{-1}\left(\frac{z-z'}{x+x'}\right) - z'\right]_{-\frac{l}{2}}^{\frac{l}{2}} \tag{A3}$$

Let I_2 equal to

$$I_2 = \int_{-\frac{l}{2}}^{\frac{l}{2}} \ln\left[\left(y - \frac{w}{2}\right) + \sqrt{(x-a)^2 + \left(y - \frac{w}{2}\right)^2 + (z-z')^2}\right] dz' \quad \text{(A4)}$$

$$I_2 = \Bigg[-(z-z')\ln\left[\left(y - \frac{w}{2}\right) + \sqrt{(x-a)^2 + \left(y - \frac{w}{2}\right)^2 + (z-z')^2}\right] - \left(y - \frac{w}{2}\right)\ln\left[(z-z') + \sqrt{(x-a)^2 + \left(y - \frac{w}{2}\right)^2 + (z-z')^2}\right] + (x-a)\tan^{-1}\left[\frac{\left(y-\frac{w}{2}\right)(z-z')}{(x-a)\sqrt{(x-a)^2+\left(y-\frac{w}{2}\right)^2+(z-z')^2}}\right] - (x-a)\tan^{-1}\left(\frac{z-z'}{x-a}\right) - z'\Bigg]_{-\frac{l}{2}}^{\frac{l}{2}} \quad \text{(A5)}$$

Let I_3 equal to

$$I_3 = \int_{-\frac{l}{2}}^{\frac{l}{2}} \ln\left[\left(y + \frac{w}{2}\right) + \sqrt{(x+a)^2 + \left(y + \frac{w}{2}\right)^2 + (z-z')^2}\right] dz' \quad \text{(A6)}$$

$$I_3 = \left[-(z-z')\ln\left[\left(y+\frac{w}{2}\right)+\sqrt{(x+a)^2+\left(y+\frac{w}{2}\right)^2+(z-z')^2}\right] - \left(y+\frac{w}{2}\right)\ln\left[(z-z')+\sqrt{(x+a)^2+\left(y+\frac{w}{2}\right)^2+(z-z')^2}\right] + (x+a)\tan^{-1}\left[\frac{\left(y-\frac{w}{2}\right)(z-z')}{(x+a)\sqrt{(x+a)^2+\left(y-\frac{w}{2}\right)^2+(z-z')^2}}\right] - (x+a)\tan^{-1}\left(\frac{z-z'}{x+a}\right) - z'\right]_{-\frac{l}{2}}^{\frac{l}{2}} \quad \text{(A7)}$$

Let I_4 equal to

$$I_4 = \int_{-\frac{l}{2}}^{\frac{l}{2}} \ln\left[\left(y+\frac{w}{2}\right)+\sqrt{(x-a)^2+\left(y+\frac{w}{2}\right)^2+(z-z')^2}\right]dz' \quad \text{(A8)}$$

$$I_3 = \left[-(z-z')\ln\left[\left(y+\frac{w}{2}\right)+\sqrt{(x-a)^2+\left(y+\frac{w}{2}\right)^2+(z-z')^2}\right] - \left(y+\frac{w}{2}\right)\ln\left[(z-z')+\sqrt{(x-a)^2+\left(y+\frac{w}{2}\right)^2+(z-z')^2}\right] + (x-a)\tan^{-1}\left[\frac{\left(y-\frac{w}{2}\right)(z-z')}{(x-a)\sqrt{(x-a)^2+\left(y-\frac{w}{2}\right)^2+(z-z')^2}}\right] - (x-a)\tan^{-1}\left(\frac{z-z'}{x-a}\right) - z'\right]_{-\frac{l}{2}}^{\frac{l}{2}} \quad \text{(A9)}$$

Therefore,

$$\theta\left(\vec{x},\overrightarrow{x'}\right) = \frac{\lambda_{area}}{4\pi k(T_o)}\left[I_1 - I_2 - I_3 + I_4\right] \tag{A10}$$

APPENDIX B

UNCERTAINTY ANALYSIS OF MEASUREMENT DATA IN CHAPTER 6

For a sample population of n readings e.g. $X_1, X_2, X_3, \ldots, X_n$, the total error in measurements, σ, can be calculated by:

$$\sigma = \sqrt{\frac{\sum_{i=1}^{n}(X_i - X_{mean})^2}{n}} \quad \text{(B1)}$$

where X_i is the measured data, and X_{mean} is the mean of all measured data where

$$X_{mean} = \frac{\sum_{i=1}^{n} X_i}{n} \quad \text{(B2)}$$

1. Uncertainty Analysis on Measured $\Delta R/R$ for GaAs chip at Gate and S-D Regions

Table B.1. Uncertainty analysis on measured $\boldsymbol{\Delta R/R}$ for GaAs chip S-D region measured using a 5X objective lens with a 530nm illuminating light source (with reference to Table 6.1)

ΔT (°C)	Test 1	Test 2	Test 3	Test 4	Uncertainty in $\Delta R/R$	Mean $\Delta R/R$
	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$		
6.17	1.25E-03	1.25E-03	1.26E-03	1.25E-03	4.33E-06	1.26E-03
12.7	2.08E-03	2.06E-03	2.08E-03	2.07E-03	8.29E-06	2.07E-03
26.9	4.92E-03	4.90E-03	5.02E-03	5.06E-03	6.69E-05	4.98E-03
34.8	5.08E-03	5.12E-03	5.11E-03	5.02E-03	3.90E-05	5.08E-03

Table B.2. Uncertainty analysis on measured $\Delta R/R$ for GaAs chip S-D region measured using a 20X objective lens with a 530nm illuminating light source (with reference to Table 6.2)

ΔT (°C)	Test 1	Test 2	Test 3	Test 4	Uncertainty in $\Delta R/R$	Mean $\Delta R/R$
	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$		
5.15	1.24E-03	1.25E-03	1.24E-03	1.26E-03	8.29E-06	1.25E-03
10.6	2.12E-03	2.13E-03	2.15E-03	2.13E-03	1.09E-05	2.12E-03
22.4	4.38E-03	4.38E-03	4.36E-03	4.37E-03	8.29E-06	4.37E-03

Table B.3. Uncertainty analysis on measured $\Delta R/R$ for GaAs chip S-D region measured using a 100X objective lens with a 530nm illuminating light source (with reference to Table 6.3)

ΔT (°C)	Test 1	Test 2	Test 3	Test 4	Uncertainty in $\Delta R/R$	Mean $\Delta R/R$
	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$		
5.19	1.90E-03	1.91E-03	1.93E-03	1.92E-03	1.12E-05	1.92E-03
10.7	2.70E-03	2.73E-03	2.74E-03	2.72E-03	1.48E-05	2.72E-03
22.5	4.30E-03	4.31E-03	4.29E-03	4.28E-03	1.12E-05	4.30E-03

Table B.4. Uncertainty analysis on measured $\Delta R/R$ for GaAs chip gate region measured using a 100X objective lens with a 530nm illuminating light source (with reference to Table 6.3)

ΔT (°C)	Test 1	Test 2	Test 3	Test 4	Uncertainty in $\Delta R/R$	Mean $\Delta R/R$
	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$		
5.19	-8.51E-04	-8.50E-04	-8.50E-04	-8.51E-04	5.00E-07	-8.51E-04
10.7	-5.54E-04	-5.60E-04	-5.53E-04	-5.56E-04	2.68E-06	-5.56E-04
22.5	7.48E-04	7.50E-04	7.52E-04	7.49E-04	1.48E-06	7.50E-04

2. Uncertainty Analysis on Measured $\Delta R/R$ for GaN chip at Gate Region

Table B.5. Uncertainty analysis on 1st set of measured $\Delta R/R$ for GaN chip gate region measured using a 20X objective lens with a white illuminating light source (with reference to Table 6.4)

ΔT (°C)	Test 1	Test 2	Test 3	Test 4	Uncertainty in $\Delta R/R$	Mean $\Delta R/R$
	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$		
0.366	-7.06E-05	-7.05E-05	-7.06E-05	-7.05E-05	4.72E-08	-7.06E-05
0.779	-3.40E-04	-3.41E-04	-3.40E-04	-3.40E-04	4.33E-07	-3.40E-04
1.11	-1.10E-03	-1.11E-03	-1.09E-03	-1.11E-03	8.29E-06	-1.10E-03
1.50	-1.43E-03	-1.43E-03	-1.44E-03	-1.44E-03	6.20E-06	-1.43E-03

Table B.6. Uncertainty analysis on 2nd set of measured $\Delta R/R$ for GaN chip gate region measured using a 20X objective lens with a white illuminating light source (with reference to Table 6.4)

ΔT (°C)	Test 1	Test 2	Test 3	Test 4	Uncertainty in $\Delta R/R$	Mean $\Delta R/R$
	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$		
0.375	-2.21E-03	-2.21E-03	-2.20E-03	-2.23E-03	1.11E-05	-2.21E-03
0.719	-2.59E-03	-2.61E-03	-2.62E-03	-2.62E-03	1.24E-05	-2.61E-03
1.55	-3.67E-03	-3.64E-03	-3.65E-03	-3.66E-03	1.01E-05	-3.66E-03
2.33	-4.77E-03	-4.78E-03	-4.78E-03	-4.77E-03	6.02E-06	-4.77E-03

Table B.7. Uncertainty analysis on 1st set of measured $\Delta R/R$ for GaN chip gate region measured using a 100X objective lens with a white illuminating light source (with reference to Table 6.5)

ΔT (°C)	Test 1	Test 2	Test 3	Test 4	Uncertainty in $\Delta R/R$	Mean $\Delta R/R$
	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$		
0.330	-3.29E-04	-3.29E-04	-3.28E-04	-3.28E-04	3.11E-07	-3.29E-04
0.748	-9.16E-04	-9.16E-04	-9.18E-04	-9.16E-04	9.27E-07	-9.16E-04
1.56	-2.05E-03	-2.06E-03	-2.06E-03	-2.05E-03	2.27E-06	-2.06E-03
2.33	-3.53E-03	-3.55E-03	-3.54E-03	-3.50E-03	1.91E-05	-3.53E-03

Table B.8. Uncertainty analysis on 2nd set of measured $\Delta R/R$ for GaN chip gate region measured using a 100X objective lens with a white illuminating light source (with reference to Table 6.5)

ΔT (°C)	Test 1	Test 2	Test 3	Test 4	Uncertainty in $\Delta R/R$	Mean $\Delta R/R$
	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$		
0.330	-5.24E-04	-5.25E-04	-5.25E-04	-5.26E-04	7.07E-07	-5.25E-04
0.748	-1.35E-03	-1.35E-03	-1.36E-03	-1.36E-03	4.36E-06	-1.36E-03
1.56	-1.80E-03	-1.80E-03	-1.82E-03	-1.82E-03	8.57E-06	-1.81E-03
2.33	-2.98E-03	-2.95E-03	-2.97E-03	-2.97E-03	1.13E-05	-2.97E-03

3. Uncertainty Analysis on Measured Gate Temperatures of a GaAs PA MMIC obtained using TRT and IRT

Table B.9. Uncertainty analysis on measured gate temperatures of a GaAs PA MMIC obtained using TRT (with reference to Fig. 6.21)

W/mm	Test 1	Test 2	Test 3	Test 4	Uncertainty in T (°C)	Mean T (°C)
	T (°C)	T (°C)	T (°C)	T (°C)		
9.33E-05	26.3	25.9	26	25.8	0.19	26.0
0.171	37.4	43.2	36.9	42.1	2.78	40.0
0.366	59.2	55.1	61.1	64.4	3.36	60.0
0.558	80.5	77.7	83.9	82.4	2.32	81.1
0.746	100.2	99.3	103.7	103.5	1.95	101.7
0.941	124.5	122.4	120.9	119.1	1.98	121.7

Table B.10. Uncertainty analysis on measured gate temperatures of a GaAs PA MMIC obtained using IRT (with reference to Fig. 6.36)

W/mm	Test 1	Test 2	Test 3	Test 4	Uncertainty in *T* (°C)	Mean *T* (°C)
	T (°C)	*T* (°C)	*T* (°C)	*T* (°C)		
0.371	45.9	46.7	47.3	46.7	1.30	58.3
0.564	58.7	59.5	58.9	56.1	0.47	73.6
0.715	73.8	72.9	73.5	74.2	0.63	104.3
0.997	104.7	103.5	105.1	103.9	0.50	46.7

4. Uncertainty Analysis on Measured Gate Temperatures of a GaN PA MMIC obtained using TRT

Table B.11. Uncertainty analysis on measured gate temperatures of a GaN PA MMIC obtained using TRT with a 20X objective lens with aluminium jig base temperature of 25°C (with reference to Fig. 6.24)

W/mm	Test 1	Test 2	Test 3	Test 4	Uncertainty in *T* (°C)	Mean *T* (°C)
	T (°C)	*T* (°C)	*T* (°C)	*T* (°C)		
0.440	29.7	27.9	32.8	28.3	1.92	29.7
1.163	30.6	30.1	32.2	30.5	0.80	30.9
1.770	31.1	32.5	32.0	30.8	0.68	31.6
2.476	33.4	35.4	34.1	35.0	0.78	34.5
2.944	34.5	36.8	35.6	36.3	0.86	35.8

Table B.12. Uncertainty analysis on measured gate temperatures of a GaN PA MMIC obtained using TRT with a 100X objective lens with aluminium jig base temperature of 25°C (with reference to Fig. 6.24)

W/mm	Test 1	Test 2	Test 3	Test 4	Uncertainty in *T* (°C)	Mean *T* (°C)
	T (°C)	*T* (°C)	*T* (°C)	*T* (°C)		
0.700	36.5	35.1	40.1	37.4	1.83	37.3
1.514	58.0	60.1	55.0	61.0	2.31	58.5
2.530	69.9	65.9	75.1	73.6	3.56	71.1
3.788	96.9	100.9	95.0	96.4	2.19	97.3

Table B.13. Uncertainty analysis on measured gate temperatures of a GaN PA MMIC obtained using TRT with a 20X objective lens with aluminium jig base temperature of 70°C (with reference to Fig. 6.25)

W/mm	Test 1	Test 2	Test 3	Test 4	Uncertainty in *T* (°C)	Mean *T* (°C)
	T (°C)	*T* (°C)	*T* (°C)	*T* (°C)		
0.324	71.1	70.9	71.3	71.1	0.14	71.1
0.931	71.3	71.7	71.3	71.1	0.22	71.4
1.530	74.9	75.4	75.9	75.1	0.38	75.3
2.192	76.6	76.7	76.5	76.8	0.11	76.7
2.729	78.9	77.5	77.1	76.9	0.78	77.6

Table B.14. Uncertainty analysis on measured gate temperatures of a GaN PA MMIC obtained using TRT with a 100X objective lens with aluminium jig base temperature of 70°C (with reference to Fig. 6.25)

W/mm	Test 1	Test 2	Test 3	Test 4	Uncertainty in *T* (°C)	Mean *T* (°C)
	T (°C)	*T* (°C)	*T* (°C)	*T* (°C)		
0.567	83.2	82.9	84.2	84.5	0.67	83.7
1.136	96.6	97.5	97.9	98.0	0.55	97.5
1.818	121.3	116.9	129.1	120.9	4.42	122.1
2.824	130.6	145.1	138.4	148.3	6.79	140.6

5. Uncertainty Analysis on Measured Gate Temperatures of a GaN PA MMIC obtained using IRT

Table B.15. Uncertainty analysis on measured gate temperatures of a GaN PA MMIC obtained using IRT with aluminium jig base temperature of 25°C (with reference to Fig. 6.40)

W/mm	Test 1	Test 2	Test 3	Test 4	Uncertainty in *T* (°C)	Mean *T* (°C)
	T (°C)	*T* (°C)	*T* (°C)	*T* (°C)		
0.847	30.3	29.5	28.8	31.2	0.90	30.0
1.736	39.0	37.5	40.1	40.2	1.09	39.2
2.474	50.3	50.5	52.0	51.3	0.68	51.0
3.379	75.2	76.0	74.9	75.4	0.40	75.4

Table B.16. Uncertainty analysis on measured gate temperatures of a GaN PA MMIC obtained using IRT with aluminium jig base temperature of 70°C (with reference to Fig. 6.41)

W/mm	Test 1	Test 2	Test 3	Test 4	Uncertainty in *T* (^{o}C)	Mean *T* (^{o}C)
	T (^{o}C)	*T* (^{o}C)	*T* (^{o}C)	*T* (^{o}C)		
0.728	79.6	79.9	79.6	79.8	0.13	79.7
2.124	93.8	93.6	93.8	93.9	0.11	93.8
3.197	115.1	114.9	115.3	115.4	0.19	115.2
4.419	153.0	152.8	152.4	152.4	0.26	152.7

APPENDIX C
UNCERTAINTY ANALYSIS OF MEASUREMENT DATA IN CHAPTER 7

To determine errors in measurement data, equations (B1) and (B2) from Appendix B were used.

6. Uncertainty Analysis on Measured Data for White CLC LED Package

Table C.1. Uncertainty analysis on measured forward voltages for the white CLC LED Package at 350 mA (with reference to Fig. 7.15)

T (°C)	Test 1	Test 2	Test 3	Test 4	Uncertainty in V (V)	Mean V (V)
	V (V)	V (V)	V (V)	V (V)		
25.0	3.20	3.24	3.22	3.21	1.48E-02	3.22
35.0	3.18	3.22	3.20	3.19	1.48E-02	3.20
44.0	3.16	3.19	3.17	3.17	1.09E-02	3.17
55.0	3.15	3.17	3.16	3.15	8.29E-03	3.16
65.0	3.14	3.15	3.15	3.14	5.00E-03	3.15

Table C.2. Uncertainty analysis on measured $\Delta R/R$ for the white CLC LED die surface (with reference to Fig. 7.16)

ΔT (°C)	Test 1	Test 2	Test 3	Test 4	Uncertainty in $\Delta R/R$	Mean $\Delta R/R$
	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$		
1.58	4.27E-06	4.26E-06	4.26E-06	4.26E-06	3.61E-09	4.26E-06
1.96	1.46E-05	1.47E-05	1.47E-05	1.47E-05	4.12E-08	1.47E-05
2.39	1.91E-05	1.91E-05	1.91E-05	1.91E-05	2.06E-08	1.91E-05
2.82	2.65E-05	2.65E-05	2.65E-05	2.65E-05	2.06E-08	2.65E-05

Table C.3. Uncertainty analysis on measured ΔT for the white CLC LED die surface (with reference to Fig. 7.17)

Test No.	ΔT
1	25.2
2	24.6
3	25.4
Mean ΔT	25.1
Uncertainty in ΔT	0.34

Table C.4. Uncertainty analysis on measured forward voltages for the white CLC LED Package at 1 mA (with reference to Fig. 7.32)

T (°C)	Test 1	Test 2	Test 3	Test 4	Uncertainty in V (V)	Mean V (V)
	V (V)	V (V)	V (V)	V (V)		
25.0	2.4900	2.4892	2.4903	2.4881	8.51E-04	2.4894
35.0	2.4763	2.4760	2.4768	2.4770	3.96E-04	2.4765
45.0	2.4611	2.4622	2.4609	2.4604	6.58E-04	2.4612
55.0	2.4449	2.4461	2.4444	2.4463	7.98E-04	2.4454

Table C.5. Uncertainty analysis on measured $R_{ja,real}$ for the white CLC LED package (with reference to Fig. 7.34)

Test No.	$R_{ja,real}$
1	28.8
2	28.7
3	28.8
Mean $R_{ja,real}$	28.8
Uncertainty in $R_{ja,real}$	4.71E-02

7. Uncertainty Analysis on Measured Data for the Blue LED Die

Table C.6. Uncertainty analysis on measured $\Delta R/R$ for the blue LED die surface (with reference to Fig. 7.21)

ΔT (°C)	Test 1	Test 2	Test 3	Test 4	Uncertainty in $\Delta R/R$	Mean $\Delta R/R$
	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$	$\Delta R/R$		
0.44	1.00E-05	1.01E-05	1.01E-05	1.00E-05	3.32E-08	1.01E-05
0.91	5.60E-05	5.64E-05	5.62E-05	5.68E-05	2.73E-07	5.64E-05
2.72	1.79E-04	1.79E-04	1.80E-04	1.80E-04	5.33E-07	1.80E-04
1.34	5.99E-05	6.05E-05	6.07E-05	6.01E-05	3.17E-07	6.03E-05

Table C.7. Uncertainty analysis on measured ΔT for the blue LED die surface (with reference to Fig. 7.22)

Test No.	ΔT
1	11.0
2	12.4
3	11.7
Mean $\Delta \boldsymbol{T}$	11.7
Uncertainty in $\Delta \boldsymbol{T}$	0.61

Table C.8. Uncertainty analysis on measured $R_{ja,real}$ for the blue LED package (with reference to Fig. 7.39)

Test No.	$R_{ja,real}$
1	13.5
2	13.5
3	13.5
Mean $R_{ja,real}$	13.5
Uncertainty in $R_{ja,real}$	3.09E-02

APPENDIX D
MESH CONVERGENCE STUDIES

1. Mesh Convergence Study for Chapter 3:

In Chapter 3, various types of heat dissipation regions were modelled (Fig. 3.4 and Fig. 3.5). Since the highest temperature gradient occurs at the region near the heat source, mesh convergence studies were carried out at the substrate level only (without the carrier and jig) to ensure that the maximum junction temperature calculated has converged. The mesh density near the heat dissipation region was varied in the x, y and z directions. In the xy plane, meshes near the heat source regions are denser as compared to regions away from the heat source. Similarly in the z direction, the number of layers of mesh near the heat source regions was deliberately increased to be denser as compared to regions away from the heat source. The following shows the results of the mesh convergence study and the final mesh used for the thermal modeling.

a. Heat dissipation regions:VHS1 to VHS3 and PHS4 to PHS7

The same thermal model was created for heat dissipation regions VHS1 to VHS3 and PHS4 to PHS7. The variation of the maximum junction temperature due to variation of the mesh density is shown in Table D.1 and plotted in Fig. D.1. The final mesh shown in Fig. D.2 corresponds to the finest mesh in Table D.1.

Table D.1. Variation of the maximum junction temperature due to variation of the number of nodes in the thermal model for VHS1 to VHS3 and PHS4 to PHS7

No. of Nodes	Max. Junction Temperature (^{o}C)
79995	53.6
83420	53.62
107395	54.19
121095	54.32
127945	54.4

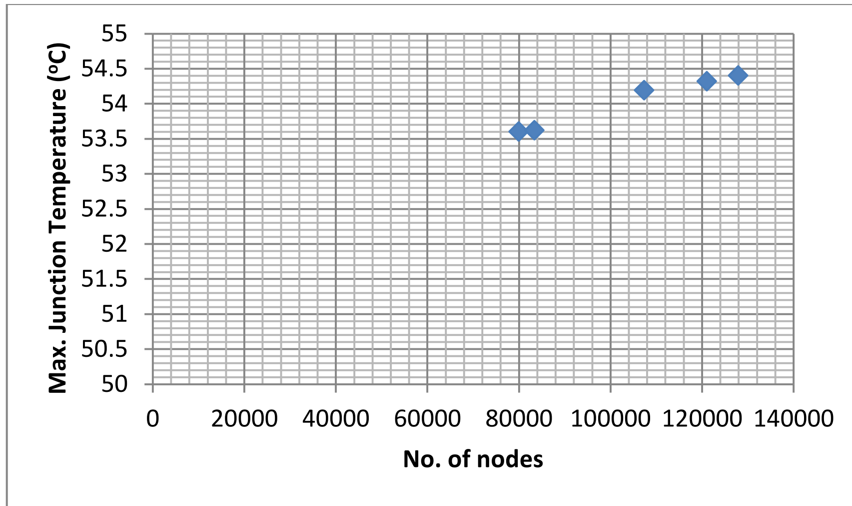

Fig. D.1. A plot of the maximum junction temperature versus the total number of nodes in the mesh used

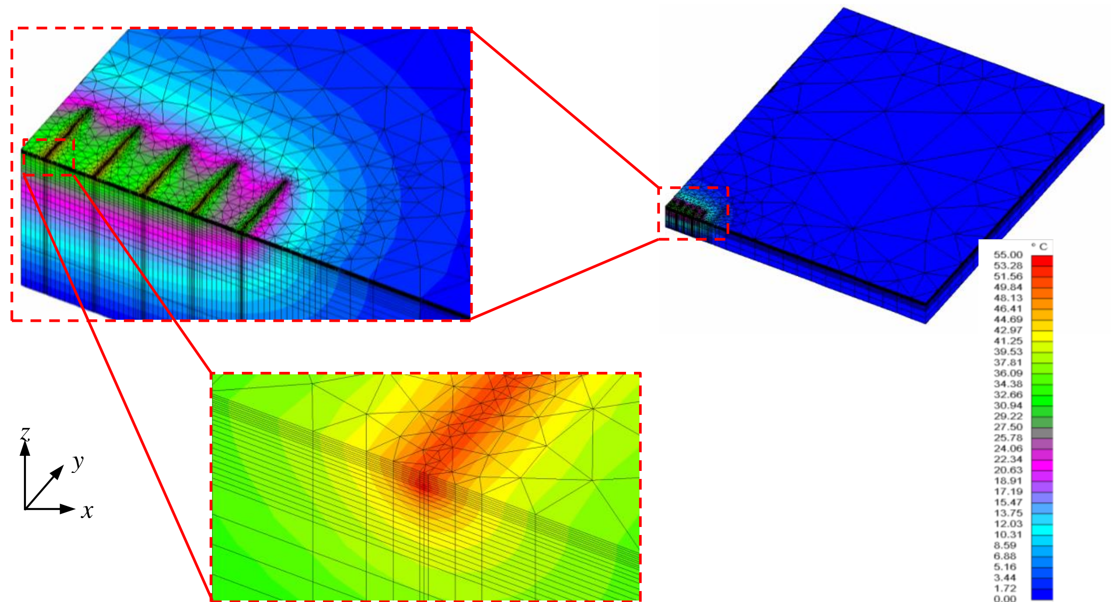

Fig. D.2. Mesh distribution in the thermal model for VHS1 to VHS3 and PHS4 to PHS7

b. Heat dissipation regions: PHS8 to PHS10

The same thermal model was created for heat dissipation regions PHS8 to PHS10. The variation of the maximum junction temperature due to variation of the mesh density is shown in Table D.2 and plotted in Fig. D.3. The final mesh shown in Fig. D.4 corresponds to the finest mesh in Table D.2.

Table D.2. Variation of the maximum junction temperature due to variation of the number of nodes in the thermal model for VHS1 to VHS3 and PHS4 to PHS7

No. of Nodes	Temperature (^{o}C)
130420	48.00
178934	48.69
257187	49.09
306285	49.18

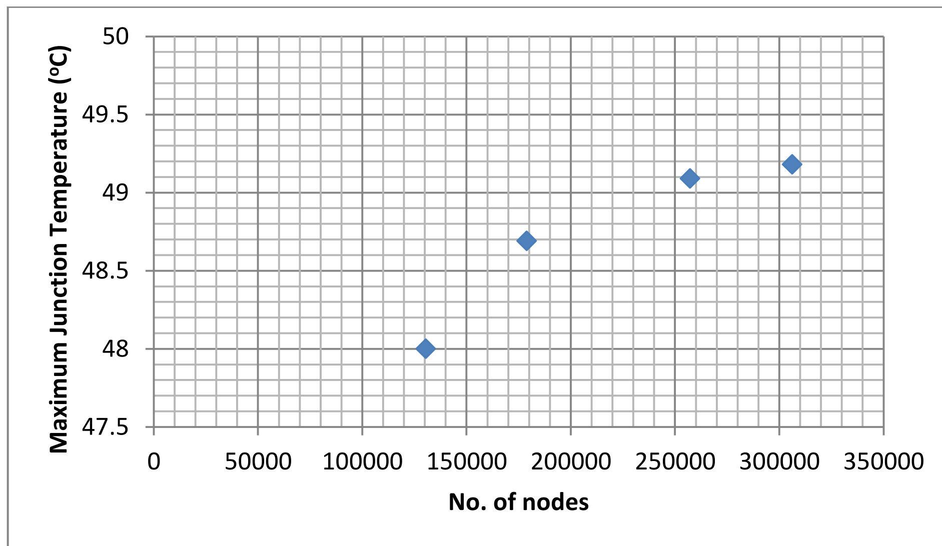

Fig. D.3. A plot of the maximum junction temperature versus the total number of nodes in the mesh used

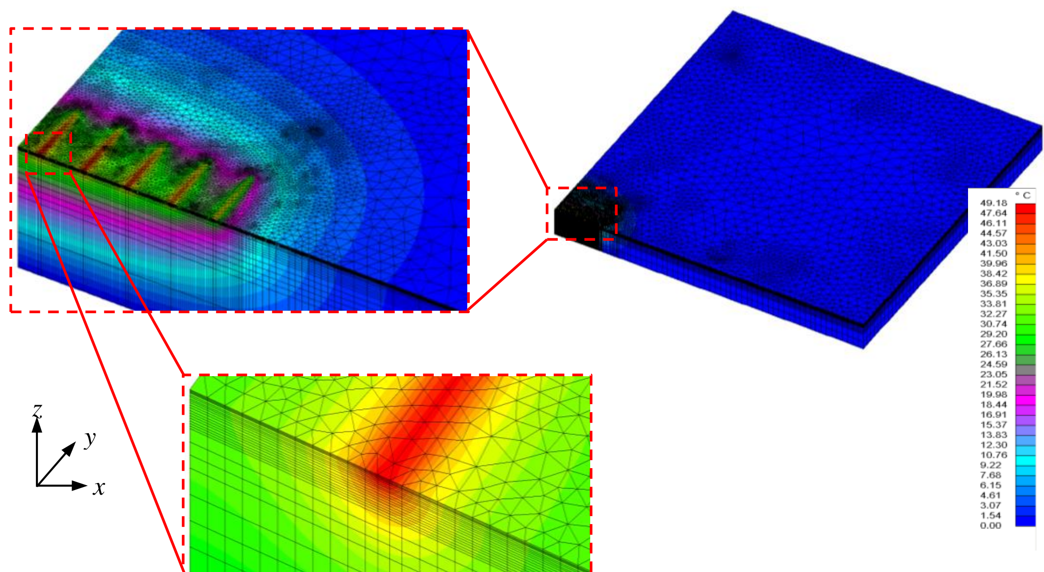

Fig. D.4. Mesh distribution in the thermal model for PHS8 to PHS10

2. Mesh Convergence Study for Chapter 4:

In Chapter 4, the temperature solutions calculated using the present analytical method for single line heat source, multiple line heat sources with gate pitch of 24 µm and 36 µm were compared with the FEA results. The following shows the results of the mesh convergence study and the final mesh used for the thermal modeling.

a. Single line heat source

In the thermal model consisting of a single line heat source, the variation of the maximum junction temperature due to variation of the mesh density is shown in Table D.3 and plotted in Fig. D.5. The final mesh shown in Fig. D.6 corresponds to the finest mesh in Table D.3.

Table D.3. Variation of the maximum junction temperature due to variation of the number of nodes in the thermal model for single line heat source

no. of nodes	Temperature (^{o}C)
99657	224.03
127543	228.3
146242	228.5
158648	229.5

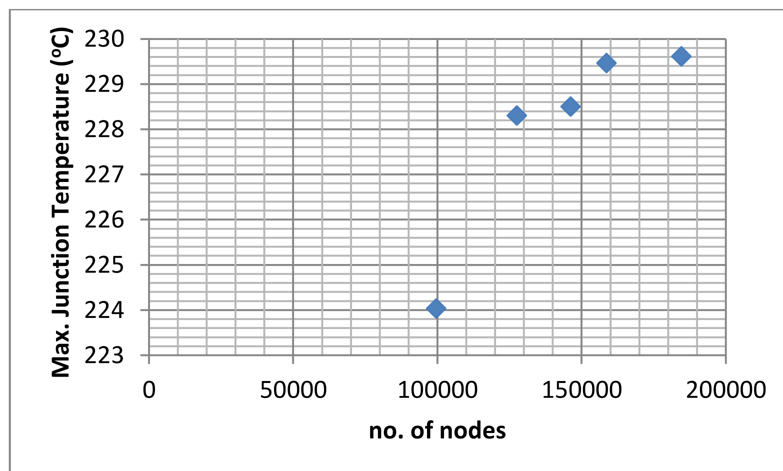

Fig. D.5. A plot of the maximum junction temperature versus the total number of nodes in the mesh used

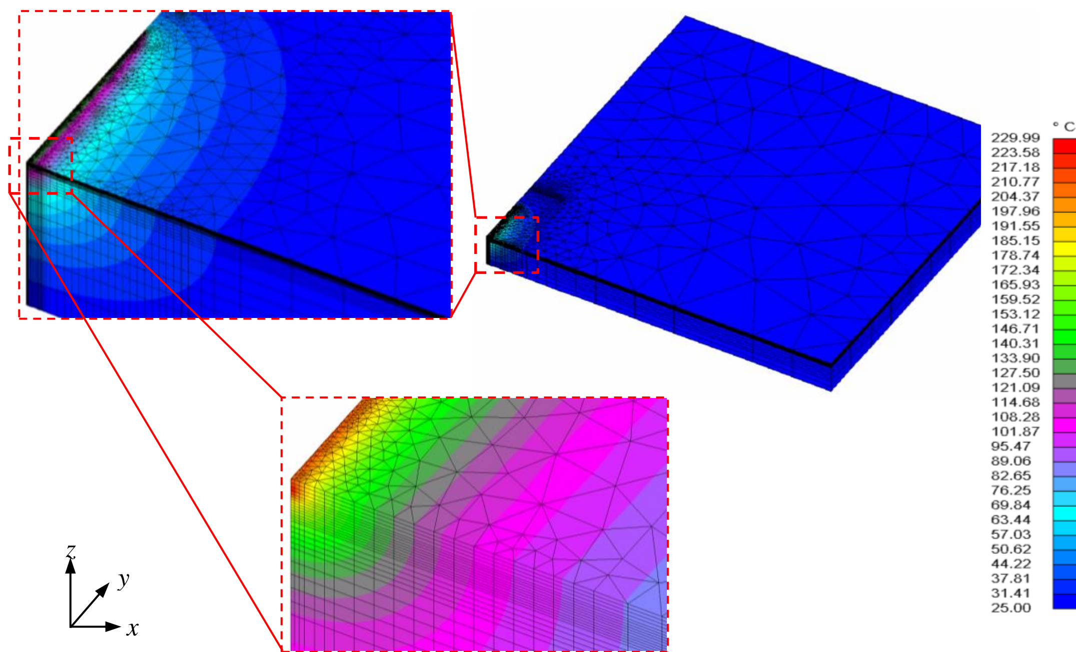

Fig. D.6. Mesh distribution in the thermal model for single line heat source

b. Multiple line heat sources for gate pitch of 24 µm

In the thermal model consisting of multiple line heat sources with gate pitch of 24 µm, the variation of the maximum junction temperature due to variation of the mesh density is shown in Table D.4 and plotted in Fig. D.7. The final mesh shown in Fig. D.8 corresponds to the finest mesh in Table D.4.

Table D.4. Variation of the maximum junction temperature due to variation of the number of nodes in the thermal model for multiple line heat sources for gate pitch of 24 µm

no. of nodes	Temperature (°C)
194752	146.8
234561	147.1
274939	147.9
319284	148.0

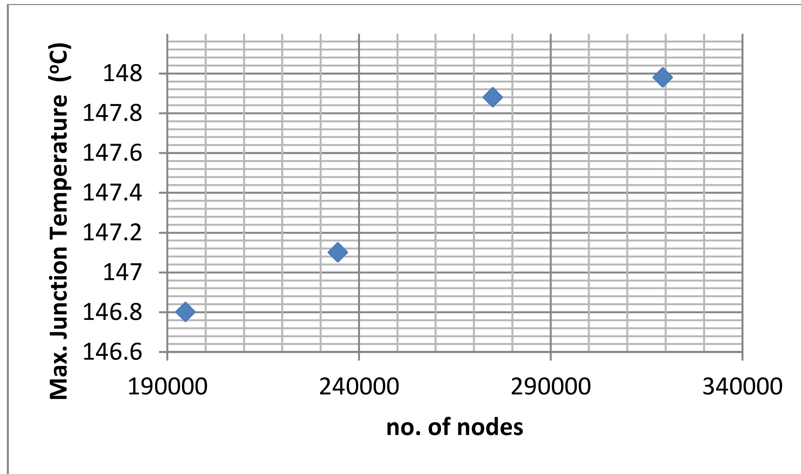

Fig. D.7. A plot of the maximum junction temperature versus the total number of nodes in the mesh used

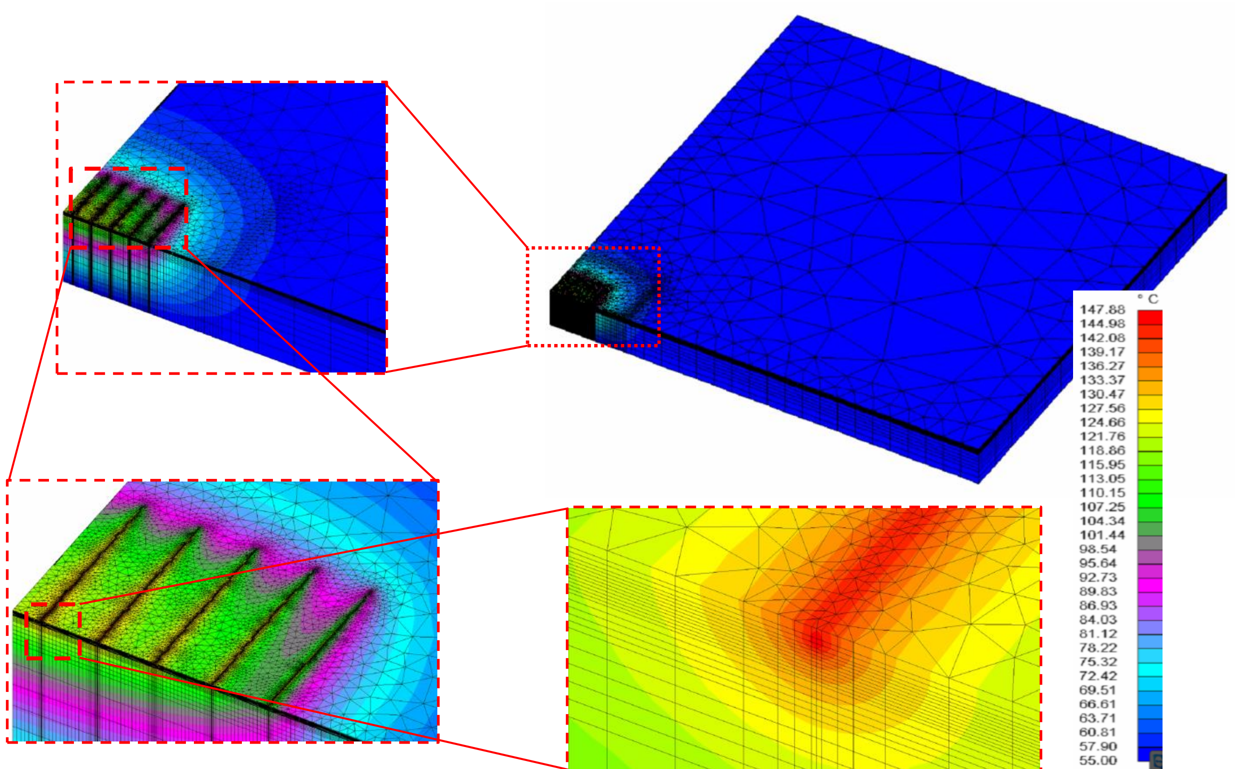

Fig. D.8. Mesh distribution in the thermal model for multiple line heat sources

c. Multiple line heat sources for gate pitch of 36 µm

In the thermal model consisting of multiple line heat sources with gate pitch of 36 µm, the variation of the maximum junction temperature due to variation of the mesh density is shown in Table D.5 and plotted in Fig. D.9. The final mesh shown in Fig. D.10 corresponds to the finest mesh in Table D.5.

Table D.5. Variation of the maximum junction temperature due to variation of the number of nodes in the thermal model for multiple line heat sources for gate pitch of 36 μm

no. of nodes	Temperature (^{o}C)
125056	126.3
172580	127
210353	127.6
277920	127.6

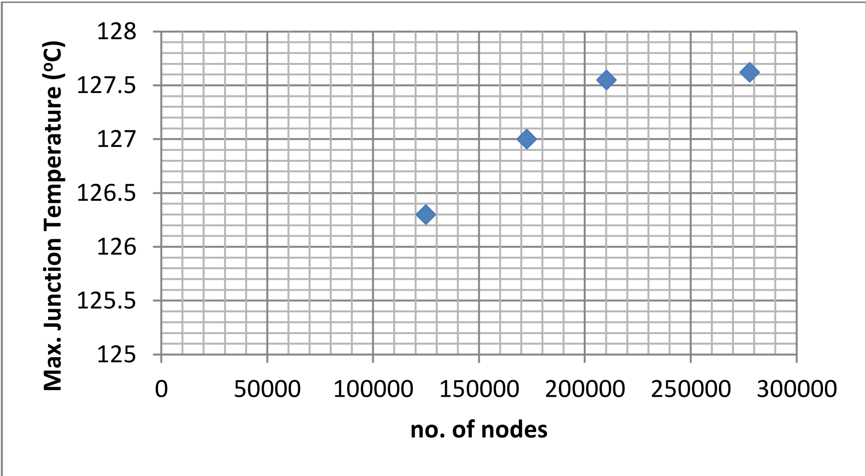

Fig. D.9. A plot of number of nodes versus the maximum junction temperature

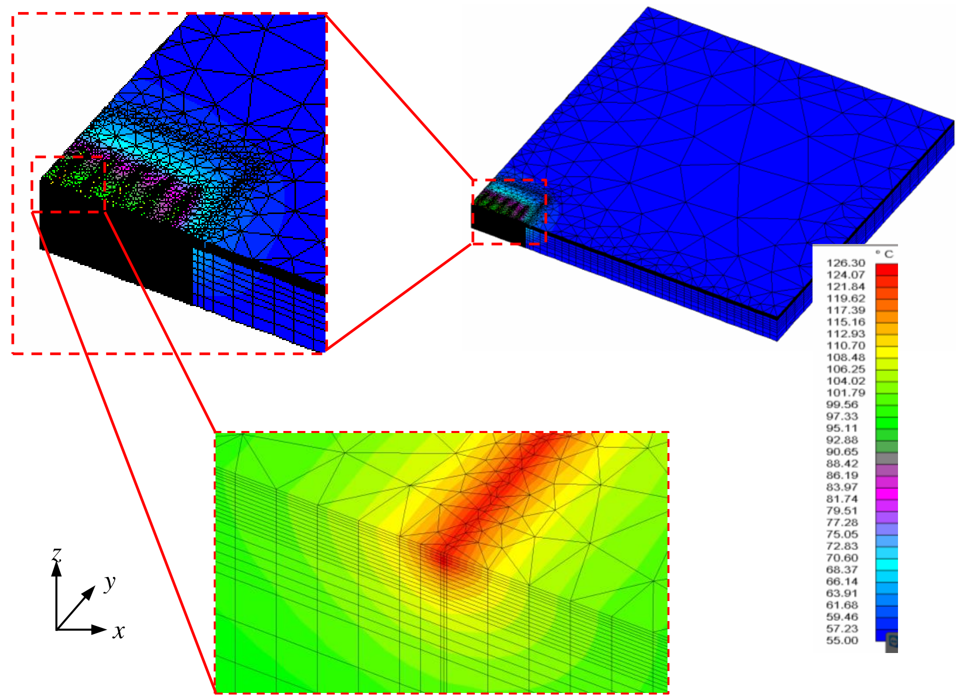

Fig. D.10. Mesh distribution in the thermal model for multiple line heat sources