PORTABLE DIFFUSE OPTICAL TOMOGRAPHY SYSTEM

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DECLARATION

I hereby declare that this thesis is my original work and it has been written by me in its entirely. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

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Thet Naing Kyaw

(30 April 2013)

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Contents

Summary

The objective of this project is to produce a low noise PRBS signal generator, to be used in a portable time-domain diffuse optical system. Due to ultra-low noise requirement at very high frequency (GHz range), circuit performance is needed to fully investigate before the actual board is fabricated. This project is to establish a frame work on systematically fabricating a RF PCB. The frame work is covered for both analog and digital circuits.

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1 Introduction

The objective of this project is to produce a low noise high frequency PRBS generator to be used in portable diffuse optical tomography system. The report will be presented in the following manner. The motivation of the design will be presented first. The explanation of the fundamental of the circuit will be followed. Since the circuit is a mixed signal design, it is separated into two portions, analog and digital. Analog circuit design involves designing a phase lock loop circuit which is responsible for generating the clock signal needed for digital circuit and a clock distribution network. The digital circuit design involves designing a 11 bit linear feedback shift register. A step by step approach to design both analog and high speed digital circuit design will be presented. It is followed by a designing procedure for the circuit layout. The functionality and performance of the circuit will be investigated with the simulations.

1.1 Background of main circuit

In the bio-medical field, optical imaging tools are important instruments such as non-invasive cancer detection device. Those tools employ various imaging technologies to detect the abnormal cells.

One of the rapidly developing imaging technologies is diffusive optical tomography (DOT). Diffusive light can penetrate turbid media such as human tissues for several centimeters. By measuring the temporal point spread function (TPSF) of diffusive light, DOT retrieves as much information as possible from the diffusive photon. The commonly used time resolved method used in DOT is the time correlated single photon counting (TCSPC) method.

The principle of single photon counting requires that no more than one photon be detected in each cycle. That requirement called for superior low noise environment. One of the ideas to achieve superior SNR comes for spread-spectrum communication system. In that system, a broadband

pseudorandom code is transmitted over the medium. The code has only a weak cross correlation with other codes and an autocorrelation function that is analogues to a delta function. So the receiving system can pick up the correct code sequence from environment noise and interference. By utilizing that property, a time resolved method has been developed which offers reduced data-acquisition time and improve overall signal-to-noise ratio. One of the popular ways to generate a broadband pseudorandom code is by using PRBS generator.

A prototype of the system using TCSPC has been reported [4]. In the prototype, a function generator is used to generate the PRBS. In this project, a PRBS generator to be used in that TCSPC system is designed. The circuit specification is as followed.

1) Low noise
2) The PRBS signal is 2.488GHz

1.2 PRBS generator

A PRBS generator is a circuit that produces pseudo random bit sequence. The name Pseudo random is called because the sequence of the code is random but it is predictable if the circuit design is known. The sequence also repeats over a certain period.

Both software and hardware PRBS generator implementation exit. One of hardware implementation of PRBS is in the form of Linear Feedback Shift Registers (LFSR). Basically the circuit can be divided into two parts, digital circuit and analog circuit. Digital circuit consists of a series of D-type flip-flops and some other logic gates to form the core of LFSR. Analog circuit design consists of a Phase lock loop circuit that produces clock signal to drive LFSR flip flop.

1.3 LFSR circuit

The current output of the Linear Feedback Shift Register is the linear function of the previous states of circuit. Typically, the designing of the LFSR circuit includes arranging a set of D-type shift registers. Depending on the required sequence length, also known as period, the number of D-type register varied. The relationship between sequence length and number of D-type register as following equation 1-1.

$$\boldsymbol{S = 2^d - 1}$$

1-1

Where, S = sequence length

d = number of D-type register

The period is determined by the number of flip-flops involved. For a given number of flip-flop, a number of different polynomial series can be generated. Only primitive polynomial series for a given number of flip-flops can produce maximal sequence. Table 1-1 shows some of the primitive polynomial series with their respective number of registers involved.

number of D-type register involved	primitive polynomial equation
2	x^2+x+1
3	x^3+x^2+1
4	x^4+x^3+1
5	x^5+x^3+1
6	x^6+x^5+1
7	x^7+x^6+1
8	$x^8+x^6+x^5+x^4+1$
9	x^9+x^5+1

10	$x^{10}+x^{7}+1$
11	$x^{11}+x^{9}+1$
12	$x^{12}+x^{11}+x^{10}+x^{4}+1$

Table 1-1 Primitive polynomial equation chart

Initial state of the LFSR circuit is called seed state. Depending on the default output state, XOR or XNOR are employed as feedback gate to avoid the dead state. The dead state is the where all the flip-flop outputs are locked into certain state until the device is reset.

Figure 1-1 shows 3 Bit shift register. It is formed with the combination of D-type flip-flops and a combinational logic. Table 1-2 shows a typical bit sequence using 3 bit shift register.

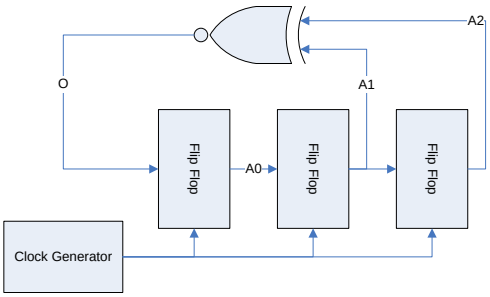


Figure 1-1 A 3 bit LFSR deisgn

state	A0	A1	A2	O
1	0	0	0	1
2	1	0	0	1
3	1	1	0	0
4	0	1	1	1
5	1	0	1	0
6	0	1	0	0
7	0	0	1	0

8	0	0	0	1
9	1	0	0	1
10	1	1	0	0

Table 1-2 3 Bit LFSR bit sequence

As it can be seen from the table, the bit sequence looks random. All the bit sequence appears except dead sequence. The series of flip-flop can be mathematically described with polynomial series as following equation 1-2.

$$O = x^3 + x^2 + 1 \tag{1-2}$$

A1 and A2 is called tap because the feedback signals are taken from those locations. The dead state of this circuit is 7 so XNOR gate is employed. Since it is a primitive polynomial sequence, all the possible bit sequence but one of 3bits flip flop is appeared once within a period. In this project, 11 flip flops are used and they operate on the same principle.

1.4 Phase lock loop circuit

A phase lock loop (PLL) can be designed to synthesize a high frequency using relatively low frequency stable oscillator. Basically, it is a negative feedback loop control system. Figure 1-2 shows a typical PLL frequency synthesizer design.

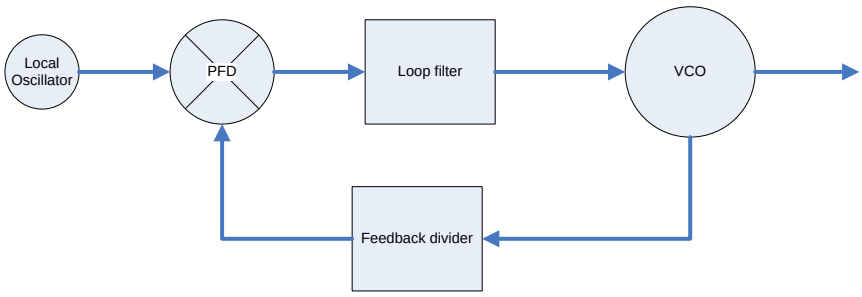


Figure 1-2 A Phase Lock Loop diagram

The circuit consists of a phase comparator, a loop filter, a low frequency crystal, a voltage control oscillator (VCO) and feedback frequency scalar. The phase comparator detects the differences between the phase of the reference clock and the feedback clock and produces the error signal. That error signal is low pass filtered and used to drive the voltage control oscillator. The voltage control oscillator will produce the frequency which is commensurate with input voltage. One portion is routed to output pin and another portion is scaled down and fed back to the phase detector for control via feedback frequency scalar.

The mathematical representation of PLL circuit and the theory of operation are well documented. This report will focus on the steps designing 2.488GHz frequency synthesizer PLL circuit. The circuit is responsible for generating clock signal that determine the bit rate of the sequence. The main consideration of this circuit is to achieve low noise performance. In order to achieve low steady state frequency error and phase noise, an active loop filter is utilized.

Two main noise sources are considered, reference transferred noise source and VCO noise. Reference transferred noise includes jitter noise from local oscillator, power supply noise. The VCO noise is induced by VCO itself and surrounding PCB noise. The higher the frequency offset is, the more prominent the VCO noise is. The noise sources can be modeled as in the Figure 1-3.

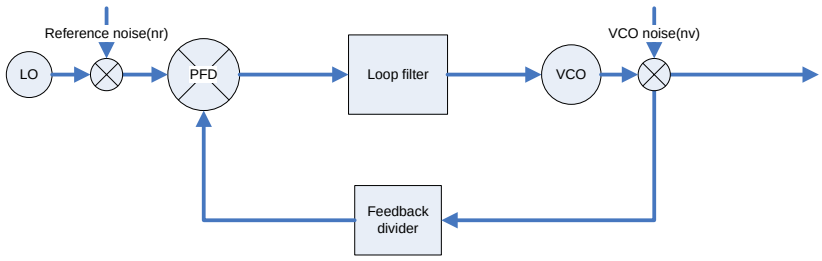


Figure 1-3 PLL with noise model

From the control theory, the output noise due to reference noise can be described as below equation 1-3.

$$S_{nr}{}^2 = N_r{}^2 * \left(\frac{G}{1+GH}\right)^2 \quad \text{1-3}$$

Where S_{nr}=Output noise due to N_r

N_r = reference noise

G = forward loop gain

H = feedback divider

G, the forward loop gain has frequency dependent response, which exhibits low pass filter response with a gain. H is simple a constant feedback divider. Hence, from that equation, it can be shown that lowering loop bandwidth will reduce N_r. The output noise due to VCO noise can be described as below equation 1-4.

$$S_{nv}{}^2 = N_v{}^2 * \left(\frac{1}{1+GH}\right)^2 \quad \text{1-4}$$

Where S_{nv}=Output noise due to N_v

N_v = VCO noise

G = forward loop gain

H = feedback divider

It is shown that the VCO noise is passing through high pass filter. The higher is the loop bandwidth, the better for VCO noise rejection. It becomes obvious that there is a trade-off to be made. Higher loop bandwidth is good for VCO noise while lower loop bandwidth is good for reference transferred noise. More detailed on this topic can be found in [8][11].

The current PLL system is a fix synthesizer frequency taking the reference clock from relatively clean frequency and driving very high VCO frequency. So the higher loop bandwidth filter is chosen.

However, there is another draw-back choosing high loop bandwidth. Designing higher bandwidth usually requires for lower pole capacitance values. The variation of their value will greatly impact the performance of the circuit because the circuit pols will be varied accordingly. If the capacitance is small enough, the PCB parasitic capacitance will contribute to that variation. So it is made sure that the values are chosen to be well above the parasitic capacitance. Phase margin is set at 60degree to grantee the PLL stability. The formula to calculate the parasitic capacitance is described in 1-5. The parasitic value of a trace with 12 mm length in the project is found to be around 0.03pf.

$$C = K * E_O * A / D$$

1-5

C= parasitic capacitance

K = the dielectric constant of the material

D=the distance between the plates

Eo = 8.854 x 10^{-12}

A = the overlapping surface area of the plates

Although it is well known that passive filter offers lower noise, based on the simulation result, the value of the capacitors needed in this very high frequency design is in fF range which is well beyond parasitic capacitance of F4 board. So the active loop filter design is chosen.

2 Circuit Design

The functional block diagram of the overall circuit is shown in Figure 2-1. It consists of main five blocks, LFSR circuit, clock distribution network, PLL circuit, Reset circuit and Output driver. PLL circuit which is responsible for generating 2.488GHz stable frequency and clock distribution network are considered analog circuits and the rest of the blocks are consider digital circuits. The system will accept reset and set signal and will output LFSR data together with 2.488GHz clock for the reference. The reset and set signal are provided so that the user can control the PRBS output without switching off the power supply.

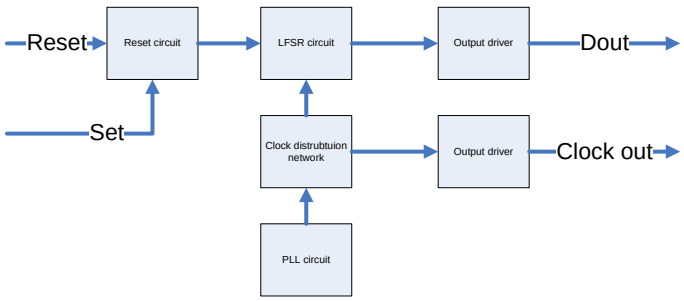


Figure 2-1 Functional block diagram

The design flow to produce that circuit is illustrated in Figure 2-2. The process is started by collecting design requirement. Some of the circuit parameters might not be known, so the assumptions have to be made. The goal is to check whether the circuit design is feasible and all the components involved are commercially available.

Once the circuit design is confirmed, it is captured into the schematic. The functionality of the circuit is checked with ideal components or behavioral component models. The output is saved which is to be benched mark against the result from non-ideal components level simulations.

A component library is built which is necessary for components level simulation. At the components level simulation, all the ideal component models are replaced with the components with realistic models, such as S-

parameters and IBIS based models. If the components level simulation doesn't produce desired result, adjust the design parameters and the circuits design are adjusted accordingly. The circuit design is fined tuned until the desired output meet with the requirement. The goal of the component level simulation is to make sure all the components parameters satisfy the requirement of the circuit design.

After that we will perform layout capture. Layout level simulation is done to capture the parasitic effect. The design process is iterative.

The circuit is relatively simple, just a series of D-type flip flop and well-understood VCO design. The main challenge comes from low noise requirement with relatively high frequency. It involves both analog circuit design in the form of PLL and digital circuit design in the form of LFSR.

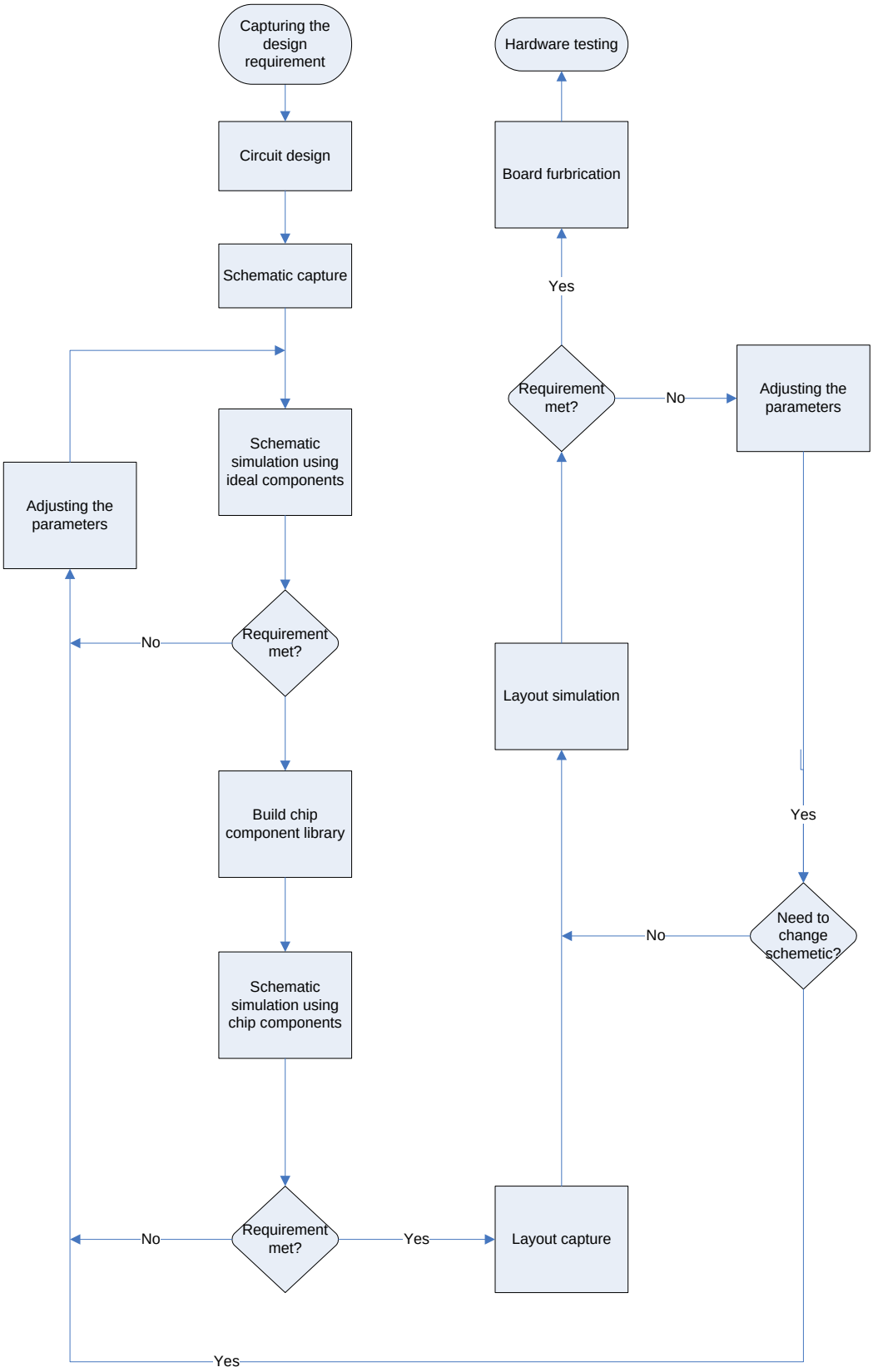


Figure 2-2 Design flow

2.1 Analog circuit

The main objective when designing the circuit is to produce a stable 2.488GHz with as low noise level as possible. The specification of the circuit is listed in the Table 2-1.

PLL requirement	parameters	unit
Frequency	2.488G	Hz
Component specifications		
ADF 4007		
N Divider	64	
N Divider to reference clock	2	
PLL IC charg pump current	5m	A
VCO		
VCO sensitivity	105M	Hz/V
Input capacitance	22p	F
Reference crystal	77.750M	Hz
Loop Filter		
OP AMP	AD8651	
C1	15.1p	F
R1	1.07k	Ohm
C2	688p	F

R2	390	Ohm
C3	65.8p	F
R3	1.00k	Ohm
R4	220	Ohm
Phase Margin	60	degree
Loop Bandwidth	1.00M	Hz
zero location	215k	Hz
pole location(R2C3)	4.65M	Hz
pole location(R1C1)	10.0M	Hz

Table 2-1 PLL Specification

Figure 2-3 shows the circuit diagram, the product of ADSim PLL design tools. In this project, ADF4007 is used as PLL synthesizer. The chip utilizes a type two phase comparator, also known as charge-pump phase comparator as its phase-frequency detector. The chip takes the reference frequency of 77.75MHz from a crystal and divided by 2 internally. The resulted frequency of 38.875MHz will be fed to PFD. The chip also takes in 2.488GHz which is divided by 64 internally. PLL charge pump current is designed to produce 5mA.

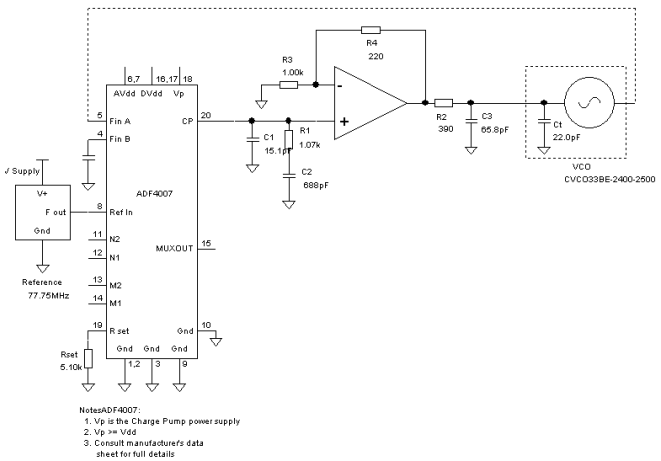


Figure 2-3 PLL schematic from ADIsimPLL

The charge pump of the chip will drive a loop filter formed by an active filter. Zero location of the active filter is set by the value of R1 and C2. The first pole location is set by the value of R2 and C3. The second pole location is set by the value of R1 and C1. Notice that the lowest capacitance value (C1) is well above the stray capacitance (1pf) found in a typical FR4 PCB board. The loop filter output is amplified with the amplifier circuit formed by AD8651, R3 and R4. The resistance values are chosen to be as low as possible so that the resistor thermal noise is kept to minimum. Loop filter = phase noise contributed by loop filter

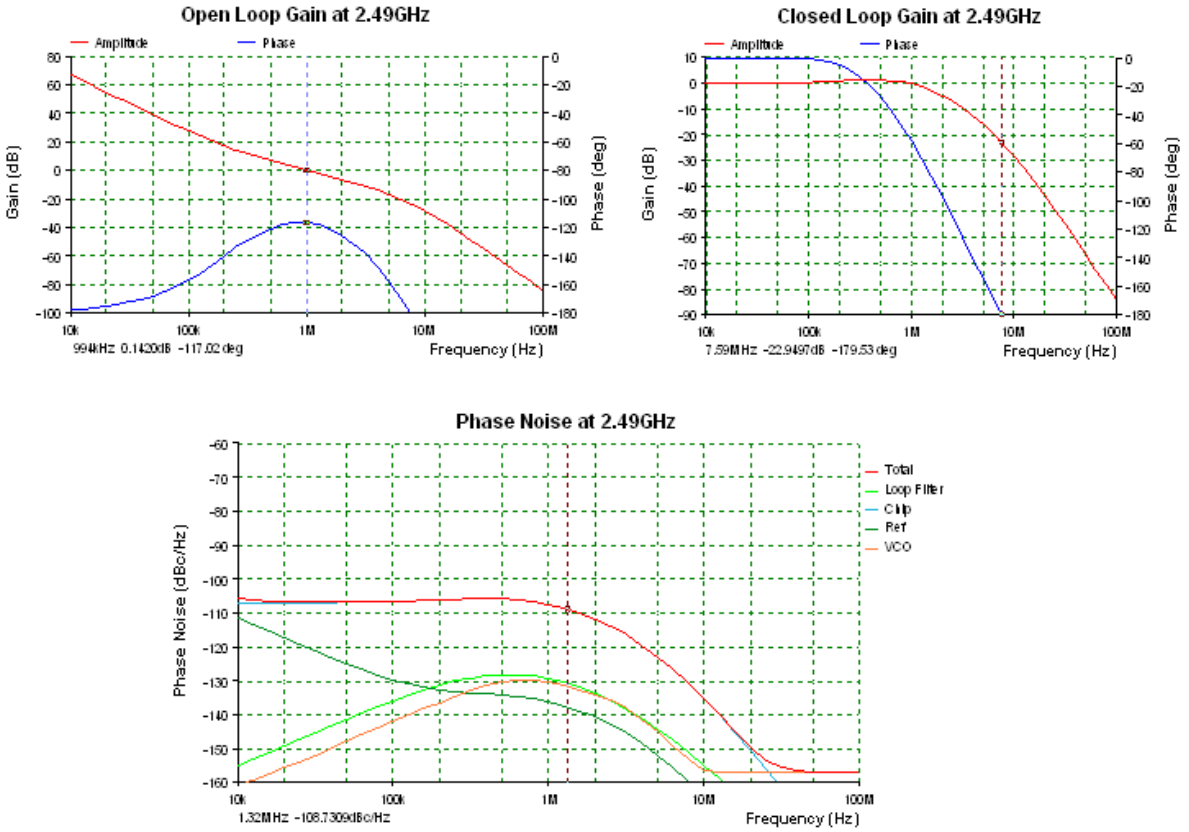
Chip = phase noise contributed by PFD

Ref = phase noise contributed by reference crystal

VCO = phase noise contributed by VCO

Total = total phase noise

Figure 2-4 shows the open loop and close sloop response of the loop filter. The noise due to loop filter is very similar to the noise introduced by VCO.



Loop filter = phase noise contributed by loop filter

Chip = phase noise contributed by PFD

Ref = phase noise contributed by reference crystal

VCO = phase noise contributed by VCO

Total = total phase noise

Figure 2-4 Performance of the loop filter

The main consideration during designing loop filter is low noise performance. Together with VCO input capacitance of 22pf, the loop filter formed as a third order system. It can be seen that the phase margin is around 60 degree and gain margin is around 22dB. The maximum noise amplitude is well below 105dBc/Hz.

The loop filter will drive the voltage control oscillator (VCO) from Crystek microwave. The VCO has the capability of producing 2.488GHz. It drives two outputs; one of them drives LFSR circuit clock distribution circuit. The other one is routed back to ADF4007. Figure 2-5 shows the simulation result of PLL circuit from ADIsimPLL. The absolute frequency error is reduced to 100 kHz within 4us. The steady state frequency error is 10m Hz. Although tracking time can be shorten with higher loop bandwidth, it is not necessary for this project because the circuit is only tracking a clean single frequency from the crystal clock.

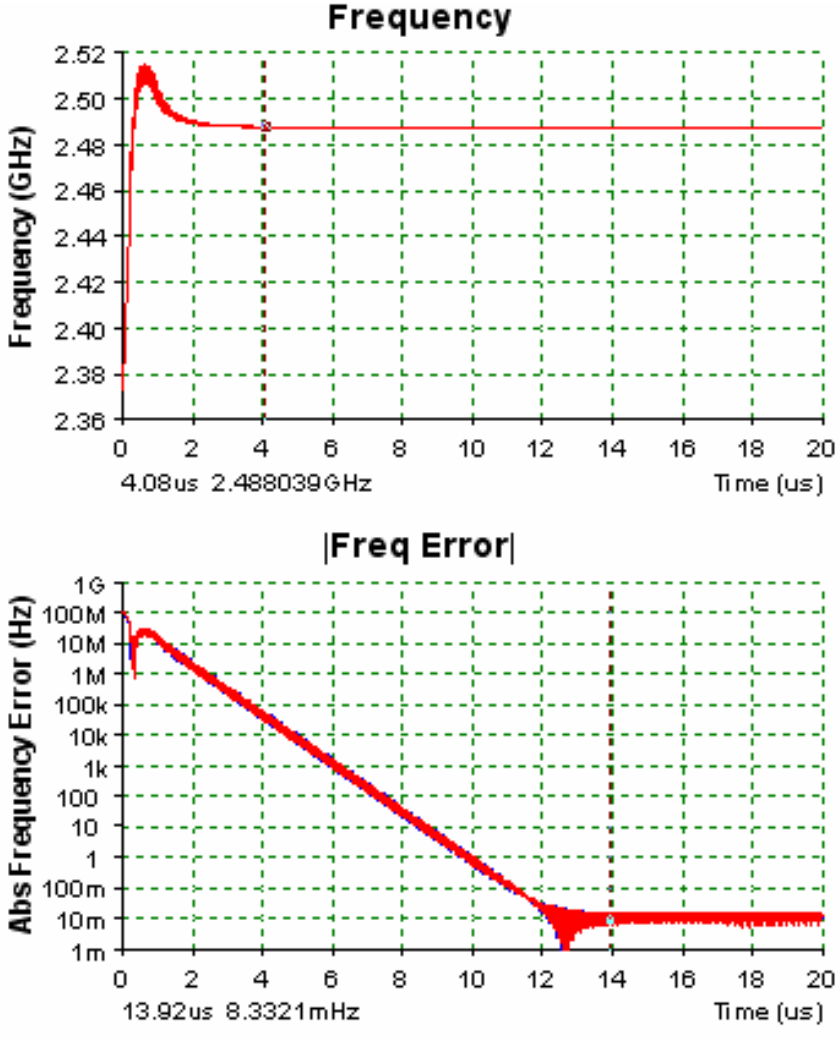


Figure 2-5 PLL Time domain performance

2.2 Digital circuit

In this project, in order to fulfill the timing requirement, 11 bits LFSR is chosen. The goal is to design and simulate a LFSR circuit at very high frequency (2.488GHz) with the best noise performance.

2.2.1 LFSR circuit

In the project, XNOR is employed because the reset state of the circuit is logic one. The running sequence and the length of the LFSR depend on the number of bits involved in LFSR circuits. In this circuit, 11 bit shift register is

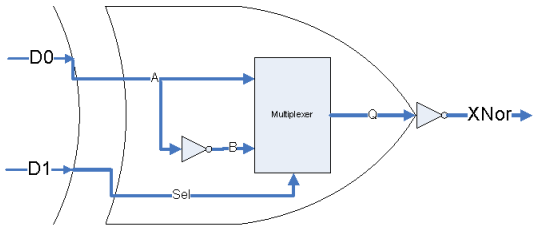
employed. In the polynomial form, it can be described as following equation 2-1.

$$y = x^{11} + x^{9} + 1 \quad \text{2-1}$$

So it will have 2^11 -1 = 2047 sequence. Each bit has 401ps. So the whole sequence will last for 822.75ns.The project uses NB7V52M which is a D type flip flop from ON Semiconductor; it has a maximum operating frequency of 10GHz. Since its interface is CML interface, clock distribution buffers are needed for every distribution. Due to high speed nature of the circuit, the propagation delay time of the chip has to be considered. Although the circuit design is 11 bit LFSR, only 9 D-type flip flops are needed due to the propagation delay time of PCB traces. The detail will be explained in Chapter 3.

2.2.2 Multiplexer

A multiplexer is considered as a smart gate that can be configured as various basic logic gate such as AND, OR and XOR GATE. All the combinational logic circuits in the project are built with the multiplexers. One of the reason, the multiplexers are used in this project is it is easily available in the market with CML interface at the required speed. Figure 2-6 shows how the multiplexer is configured as a XNOR. If the multiplexer is with differential logic, the additional physical NOT gate is not necessary in the actual circuit.



D0	D1	A	B	SEL	Q	XNOR
0	0	0	1	0	0	1
0	1	0	1	1	1	0
1	0	1	0	0	1	0
1	1	1	0	1	0	1

Figure 2-6 Multiplexer as XNOR

2.2.3 Reset circuit

The initial seed value of LFSR output is very important in synchronizing the signals. NB7V52M has differential input reset pin. The reset pins of all but the first flip-flops are connected to ground plane. The first flip flop will be connected to a S-R latch. The other function of the latch circuit is to serve as a mechanical de-bouncing circuit. Two inputs are accepted, set and reset to control the determinism of the circuit. Figure 2-7 shows NOR-gate S-R latch.

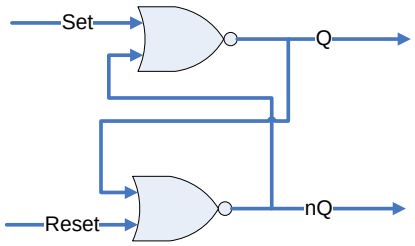


Figure 2-7 SR-Latch for reset circuit

2.2.4 Single to differential ended converter

The output from the PLL circuit is single ended with very low voltage level. So a convertor which transforms the signal that is suitable to drive CML input is designed. Figure 2-8 shows the circuit design. It employed a RF transformer to convert the single-ended signal to differential. ADL5565 is used to boost the signal to the voltage level that drives CML load.

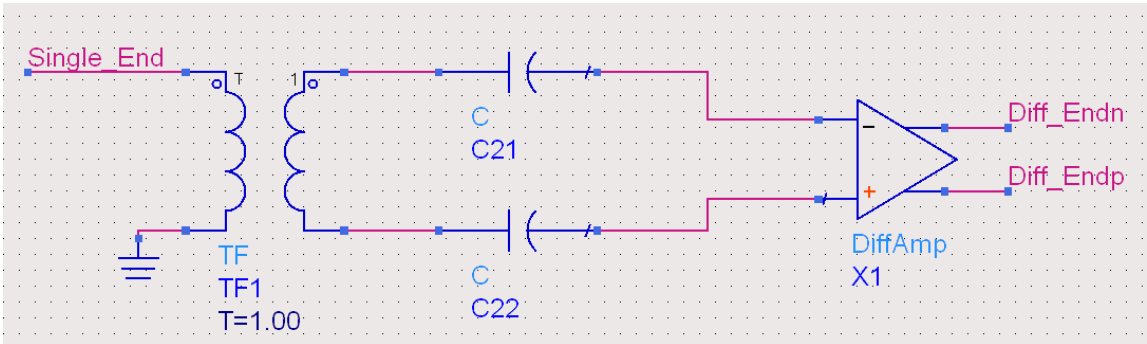


Figure 2-8 Single to Differential Output

2.2.5 Differential to single ended converter

The output from LFSR circuit is differential. To drive the single-ended input, a RF transformer is used to convert it to single-ended output.

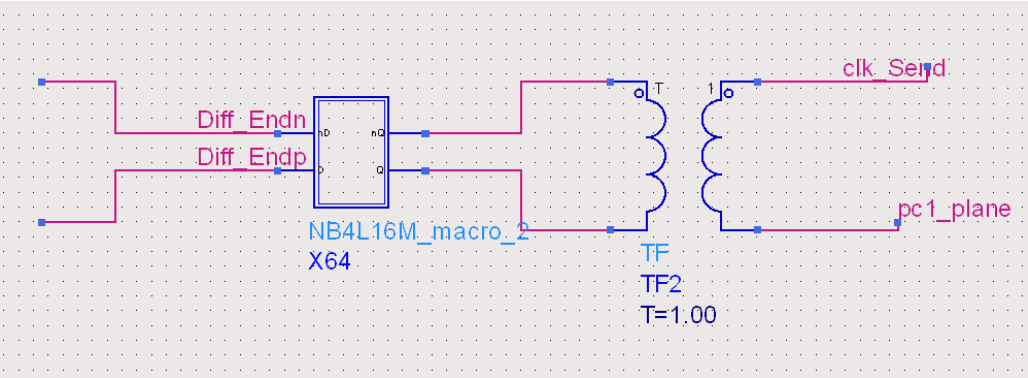


Figure 2-9 Differential to single output

2.3 Simulation of the circuit using ADS software

ADS simulator enable the PCB board level simulation. Two simulators are employed in this project, the transient simulator and the envelope simulator.

2.3.1 Transient simulation

Transient simulator of ADS software allows time domain digital circuit simulation with analog signals. The main parameter to look out for is the maximum time step. The maximum time step can't be larger than the reciprocal of signal bandwidth. Too small the time step will also result in long simulation time. So there has to be a balance to adjust the time step. Currently, the simulation time step is set to ten times the signal frequency. Another parameter is passivity of s-parameter. It needs to be enforced to make simulation more robust.

2.3.2 Envelope simulation

Envelope simulator allows simulation at a particular frequency. Although it doesn't provide as much detail information as transient simulation, it can give circuit information at a particular frequency at relatively faster speed than transient simulator. It is particularly useful for the PLL's circuit functional simulation.

2.3.3 Passivity of S-parameter

In a casual system, the S-parameter of all the passive components should have passivity. Intuitively, it means all the passive components should not amplify the signal and has the value of the gain less than unity. Due to some numerical handling error, the simulator sometimes does produce S-parameter of passive component, which has some gain at certain frequency range. It violates the causality and will cause the divergence at the simulation result. One of the solutions is to make sure that at the offending frequency point, the gain is scaled not more than unity via its Eigen value calculation. It is called enforcing passivity. When performing transient simulation, passivity of s-parameters has to be enforced to avoid divergence problem. Figure 2-10 demonstrates the point. It is taken from [18]. The red color line has the gain larger than unity gain at low frequencies. After enforcing passivity, the resultant gain (blue color line) is less than one at those low frequencies. More detail can be referenced to [19].

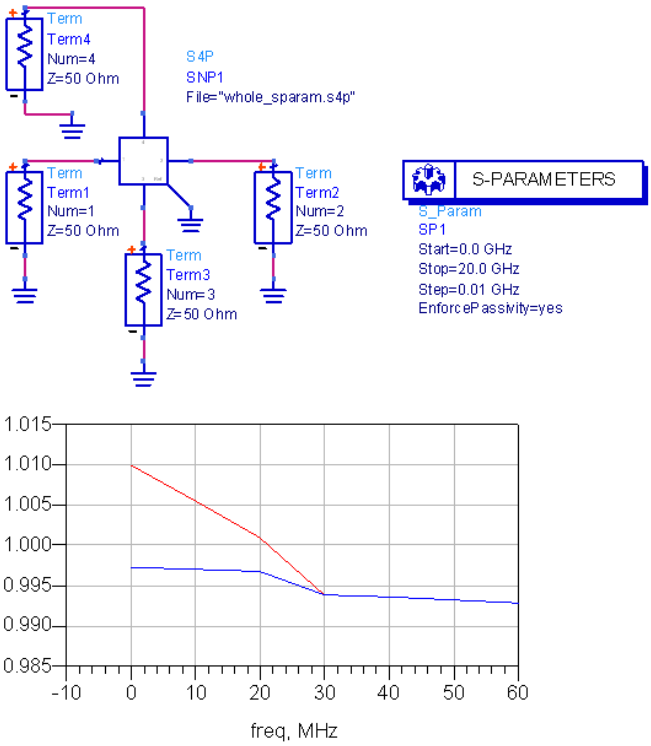


Figure 2-10 Demonstration of Enforcing Passivity

3 Schematic design

The circuit components need to be simulation-ready in order to perform functional simulation. So it is started by building a component library needed for both layout and simulation. Although ADS has a built-in simulation ready component library, it may not contain the components that are needed for the circuits. So customize simulation-ready components library is needed. Some simulation model can be obtained from component vendors in the form of spice model and S-parameter model. Most of the time, the vendors don't provide those models for various reasons such as IP concern especially for digital chips. To realistically model the I/O port of the chip, two models are used; S-parameters model and IBIS model from component vendors.

S-parameters model are vendors measurement data from the chip, consists of input and output reflection parameters, gain and insertion loss. Most of the time, S-parameters models are available for analog design components such as amplifiers. The S-parameter model can be easily implemented in ADS environment. Simply import the file to ADS circuit system and it is ready to be connected to related circuit for simulation.

For digital chip design, normally only IBIS model is available. If the simulation ready model is not available, the following three steps are followed to get a simulation ready component.

1) Chip behavior modeling
2) Propagation delay characterization
3) I/O specification (IBIS model)

Figure 3-1 show how the simulation ready chip level component looks like.

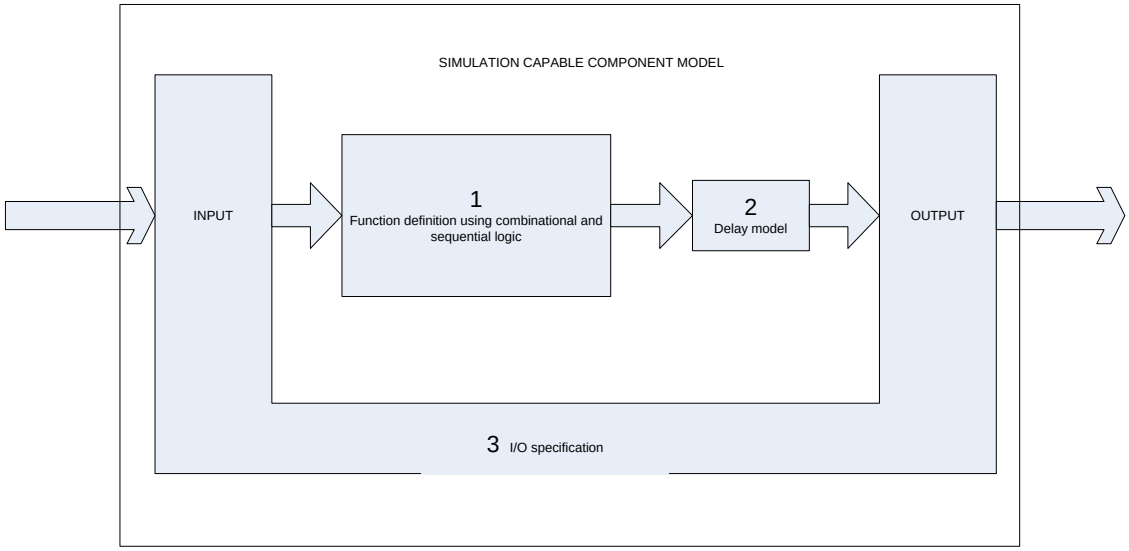


Figure 3-1 Simulation ready component model

3.1 Functional capability

For the functional simulation capability, a component library consisting of basic logic gates such as NOT gate, NAND gate, NOR gate and multiplexers is needed. Although the circuits of such components are well defined, modeling them for very high frequency (2.488GHz) is a challenge. Various transistor models are considered and it is found that idealized switch coupled with simulated parasitic capacitance is the most suitable.

An example of invertor gate model is shown in Figure 3-2. The capacitors, C1, C2 and C3 represent junction capacitance as well as load capacitance. The resistor R1 allows current return path for the capacitor C3 to aid circuit simulator. SWITCHVM2 models P-switch and SWITCHVM1models N-switch. P-switch will have low resistance when input voltage is less 0.3V and have high resistance when the input voltage is more than 0.7V. Vdh is the 1V internal digital supply voltage.

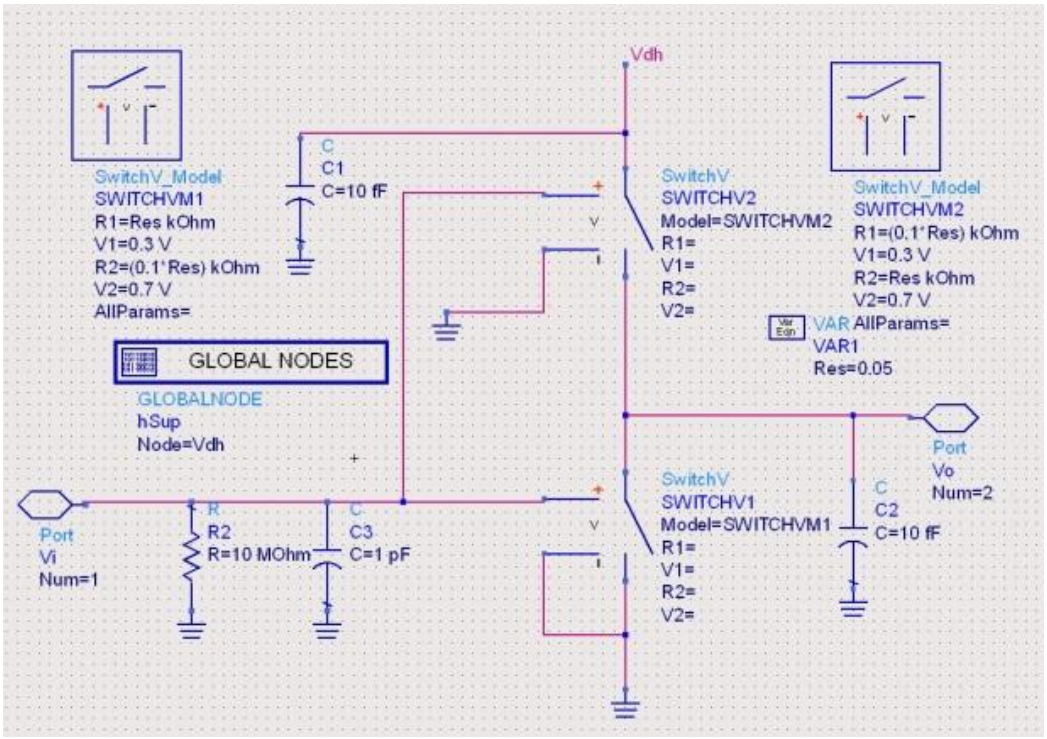


Figure 3-2 Invertor model

Figure 3-3 shows test bench of invertor and simulation output. The test bench is simulated with 5GHz, double the circuit operating frequency. The rising time and falling time of the test frequency is set to 1ps. The maximum time step of transient simulator is set to 0.1ps. All others necessary functional blocks are built in the same way.

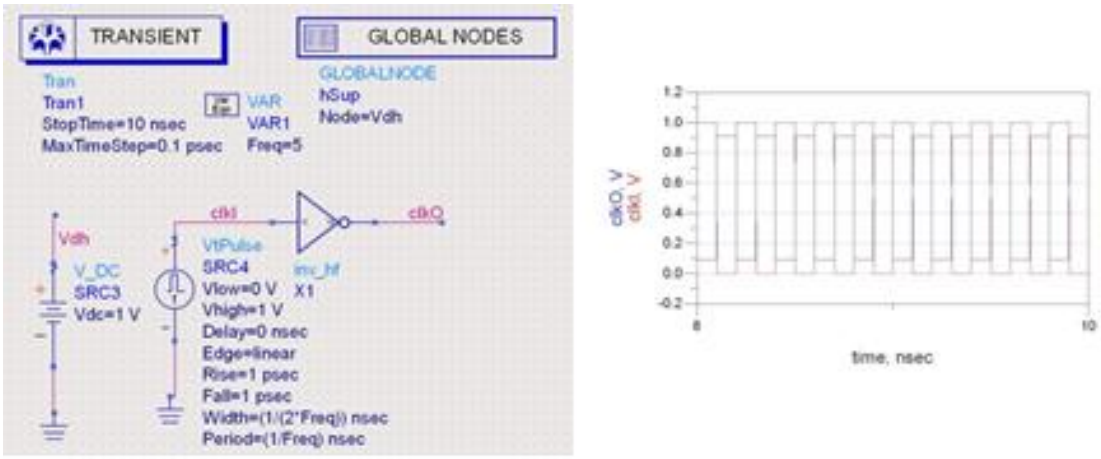


Figure 3-3 Invertor test bench with simulation result

3.2 Propagation delay characterization

After building the library, all the components go through functional validation and characterization. The characterization involved propagation delay measurement at 2.488GHz. It allows fine tuning of the model specification to match the component's data sheet to get better simulation result accuracy. Since LFSR is basically a shift register, the propagation delay time is very important. The circuit consists of an array of D-type flip flops.

Delay model is built to simulate propagation delay time. 10ps, 50ps and 100ps delay models are built to get flexible delay with optimum simulation time.

The following shows how to model 10ps delay, Figure 3-4. It is modeled as two invertors connecting back to back with a RC network at that output. With 1ohm resistance R1, the capacitance value of C1and C2 (circled in Figure 3-4) is adjusted to reach 10ps delay. Time adjusting RC network can be put at circuit input, but the propagation delay will be affected by driving load.

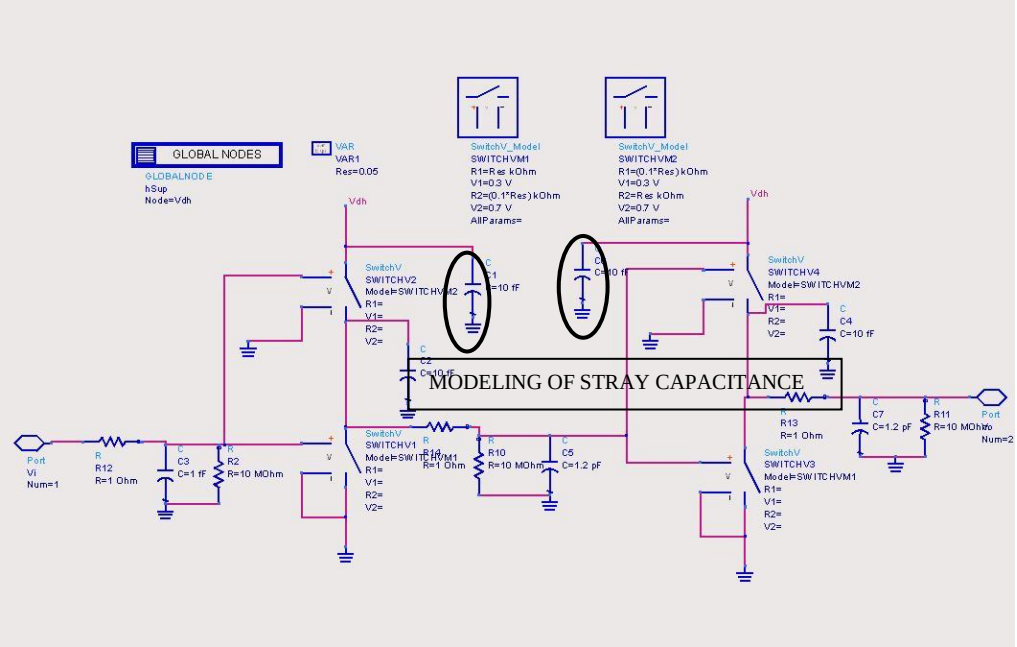


Figure 3-4 Circuit for 10ps delay modeling

Transient simulator is used to validate the result. Because the parameter that is needed to monitor is in ps, the maximum allowable time step of the transient simulator is set to 0.5 ps to get necessary timing resolution. Figure 3-5 shows the test bench for delay time characterization. The constant frequency of 2.488GHz is fed to the single to differential ended convertor. The output signal will be amplified and fed to the IBIS model. The output of the test circuit also drives another IBIS load. The purpose is to simulate the actual working condition as close as possible. The simulating devices are circled. It is cascaded to make sure that the propagating delay of the chip is not affected by the loading.

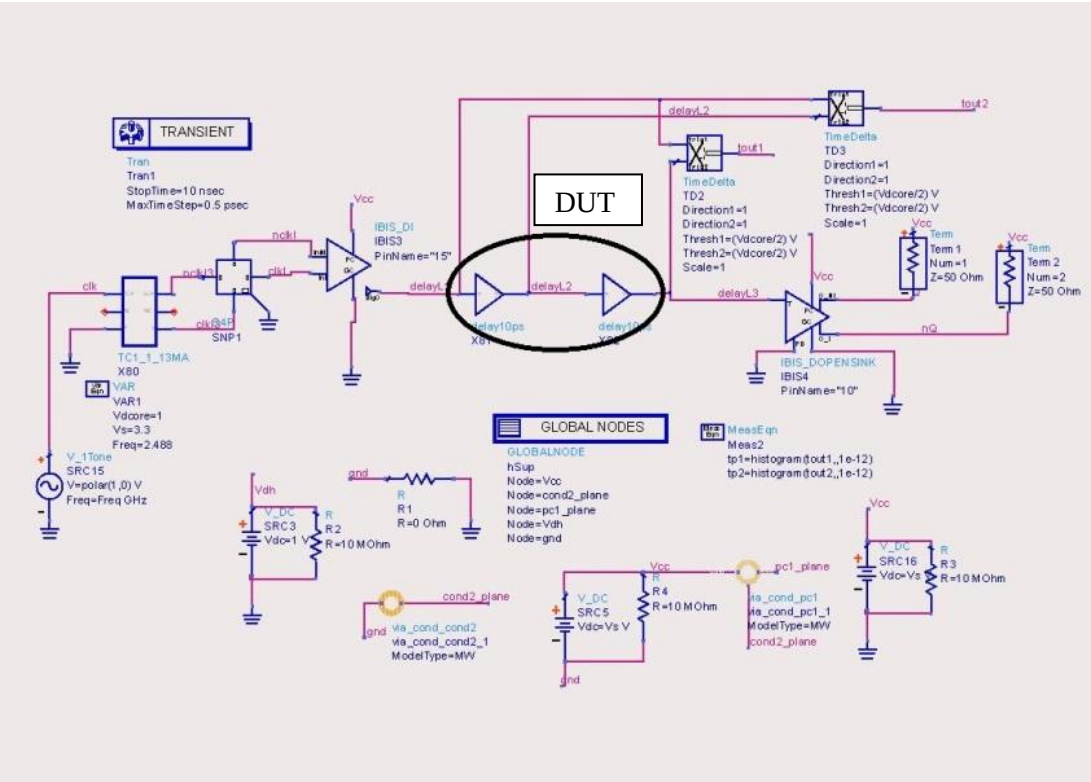


Figure 3-5 Test Bench for delay circuit

TimeDelta component is used to measure propagation delay time. It simply takes the differences of triggering instance between output and input of device. The result will be shown in histogram to investigate the worst case propagating delay. Figure 3-6 shows the simulation results for 10ps. The cursor m4 shows the cursor measurement of propagating delay time of a single delay. The cursor m2 shows worst case delay from the histogram. The cursor

m1 shows the same parameter of cascaded delay line output which is double of m2. 50ps and 100ps model are built following the same procedure.

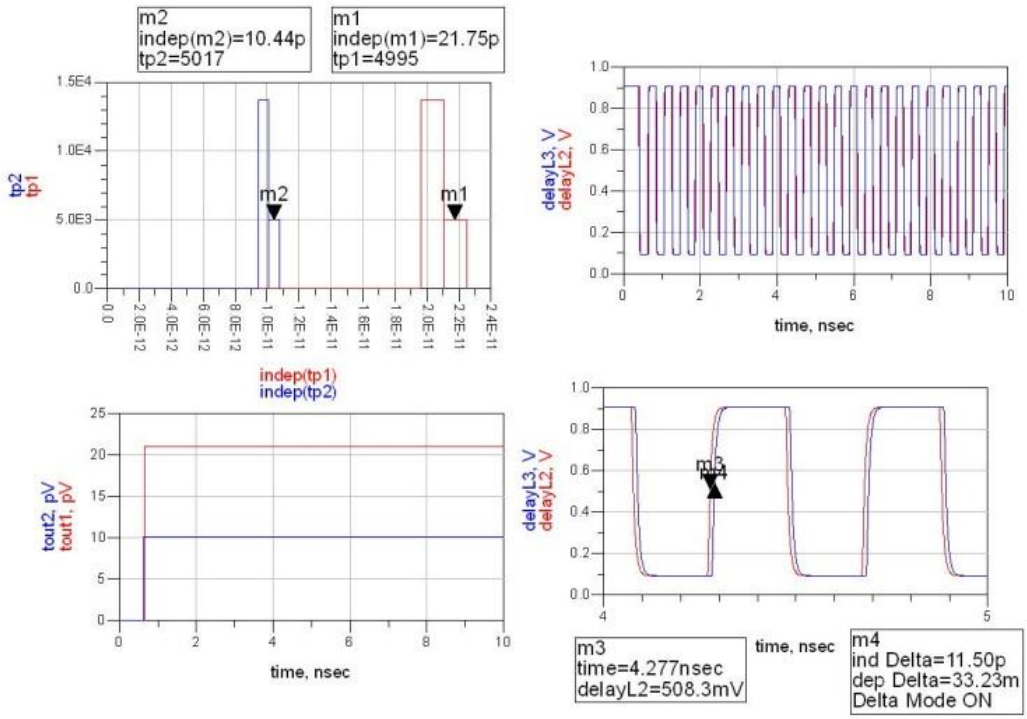


Figure 3-6 Simulation result for 10ps delay line

3.3 I/O specification

The I/O buffer interface specification (IBIS), also known as ANSI/EIA-656 allows the vendors to provide the chip performance without giving valuable IP information. Traditionally, spice models or s-parameters are given to help customers simulating the circuits, which also reveal some of the vendors' IP. IBIS models circumvents that issue by only providing the input/output performance and abstract level functional block diagram, without necessarily giving away detailed circuit level implementation.

Figure 3-7 shows the typical IBIS input and output symbols together with their representative circuit diagrams. In that diagram, L_Pkg, C_Pkg and R_Pkg represent packaging parameters, diodes represent ESD parameters,

C_Comp represents the die capacitance. The two transistors from output IBIS model represent the chip driving capability.

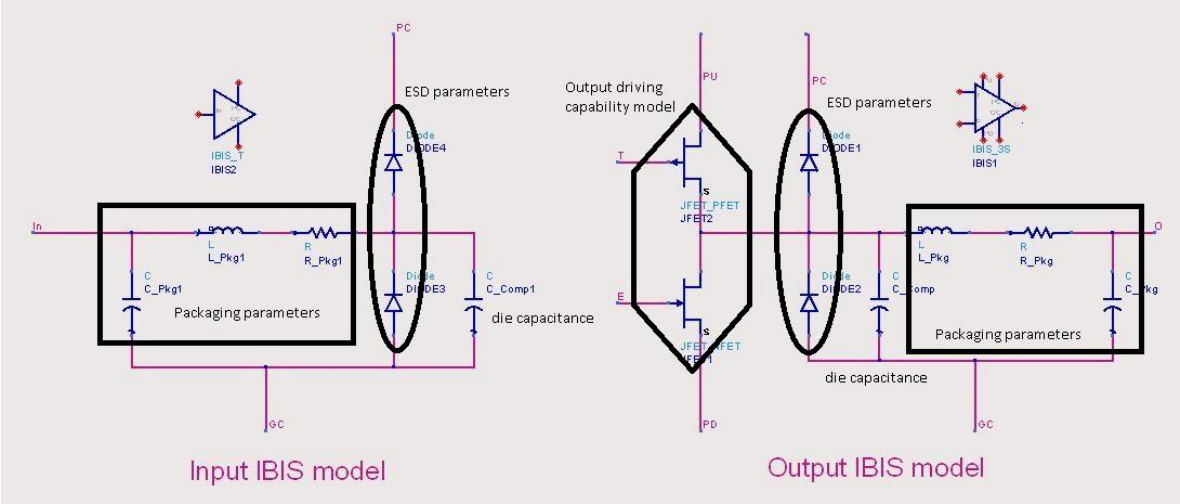


Figure 3-7 IBIS model

3.4 Chip modeling

After building all the necessary library components, individual chips are built. Below is the list of the chips that are modeled.

1) NB4L16M
2) NB7L86M
3) NB7V54M
4) NB6L16M

3.4.1 NB4L16M

NB4L16M is a clock buffer and its data sheet can be found in Appendix. Figure 3-8 shows the functional block diagram. The blocks, X1, X2, X3 and X4 have dual function of delay line and buffer. The two IBIS model is responsible for functioning as chip I/O.

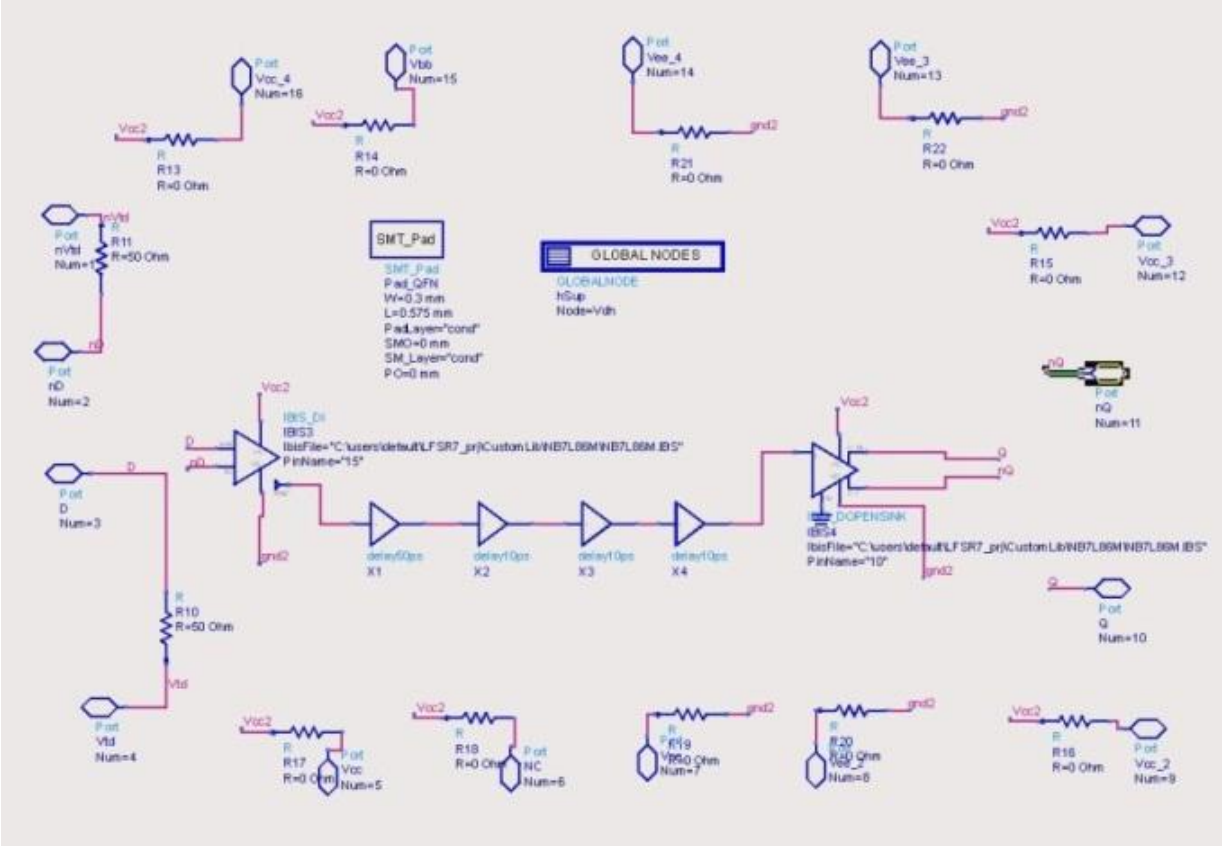


Figure 3-8 NB4L16M internal chip model

After building the modeling the functionality, the footprint for PCB integration is designed. It is done through AEL script. It is a powerful ADS feature allowing the parameters customization through the script. A sample of the script is shown in appendix. The customized script is put under local directory which is C:\users\default\hpeesof\circuit\ael. And the path is defined in C:\users\default\hpeesof\config\de_sim.cfg under USER_AEL field. SMT_Pad definition is defined in test bench. Figure 3-9 shows the schematic and layout foot print of the chip.

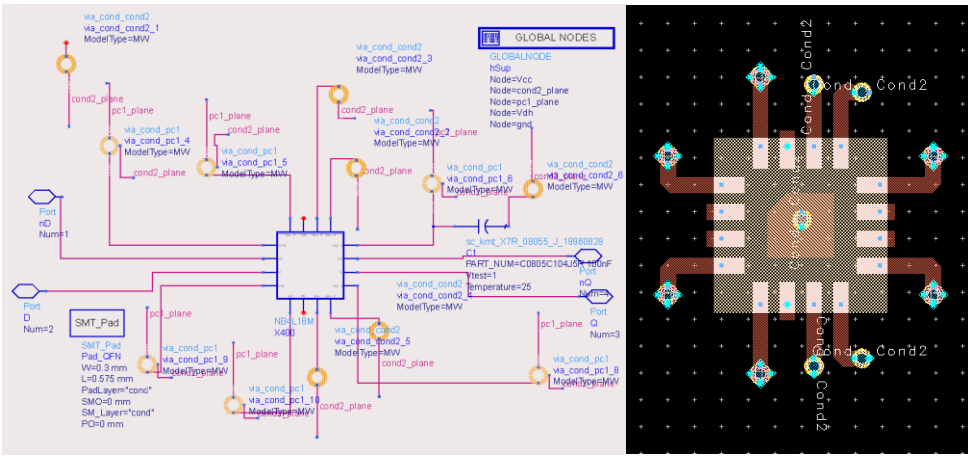


Figure 3-9 NB4L16M power supply connection

In order to simulate the actual operating environment, it is connected to the power supply and ground from via hole. Figure 3-9 show how the chip is connected. The test bench is created to test the chip whether its functionality is matched with the spec provided from the spec.

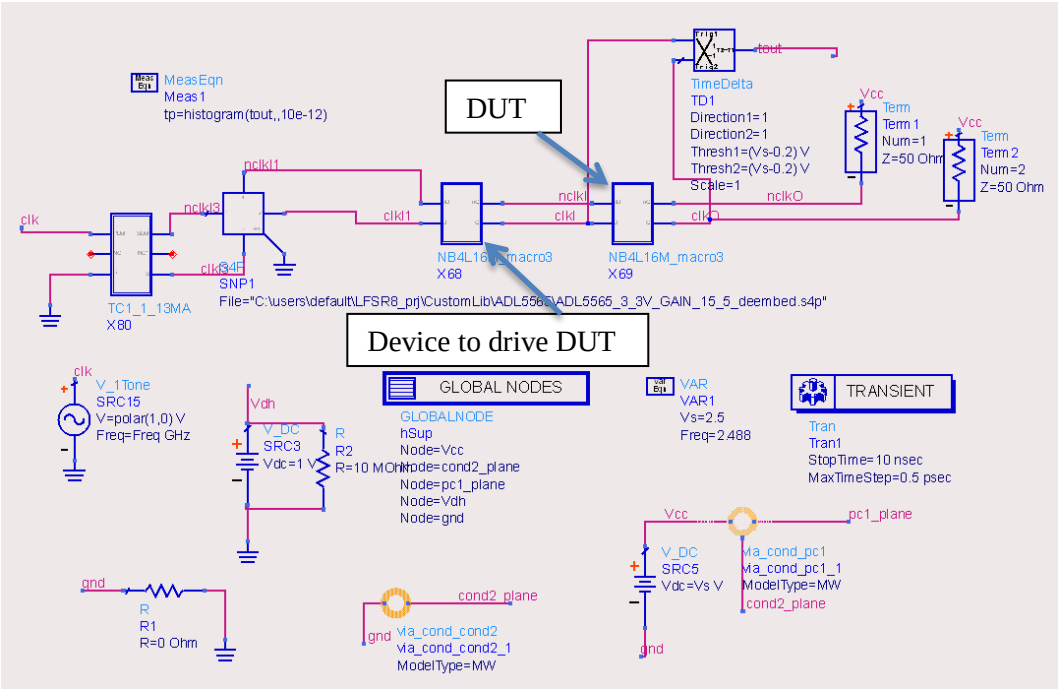


Figure 3-10 Test bench for NB4L16M

Figure 3-11 shows the simulation result from the test bench. The picture from upper left hand corner shows the histogram of propagating delay

time. It shows that worst case delay is 227.5ps which matches the data sheet value of 220ps. The lower left hand corner shows the propagating delay time in time domain form. The upper right hand corner picture shows the time domain signal waveform. The lower right hand corner picture depicts a typical propagating time delay.

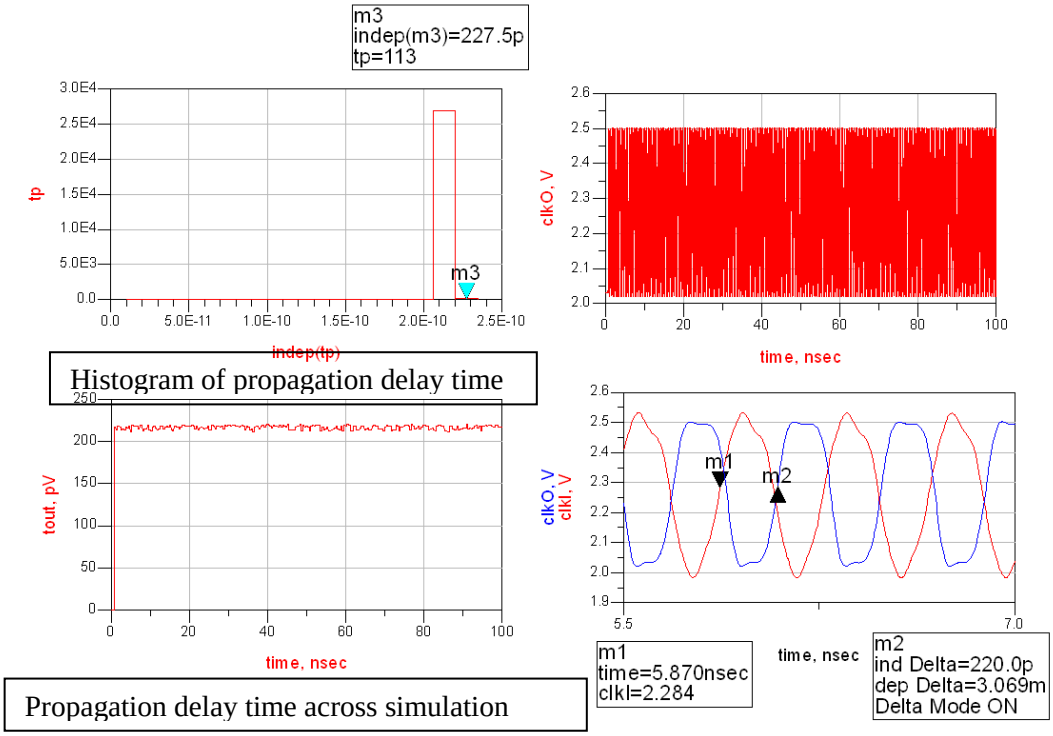


Figure 3-11 Simulation result from NB4L16M

Figure 3-12 shows the eye diagram information on NB4L16M. The threshold of the timing is 20% and 80%. The rising time and falling time are shown right hand lower corner picture, which read 49ps and 43ps respectively. They match the value from specification value of 60ps. All other chips prototyping follows exactly the same procedure.

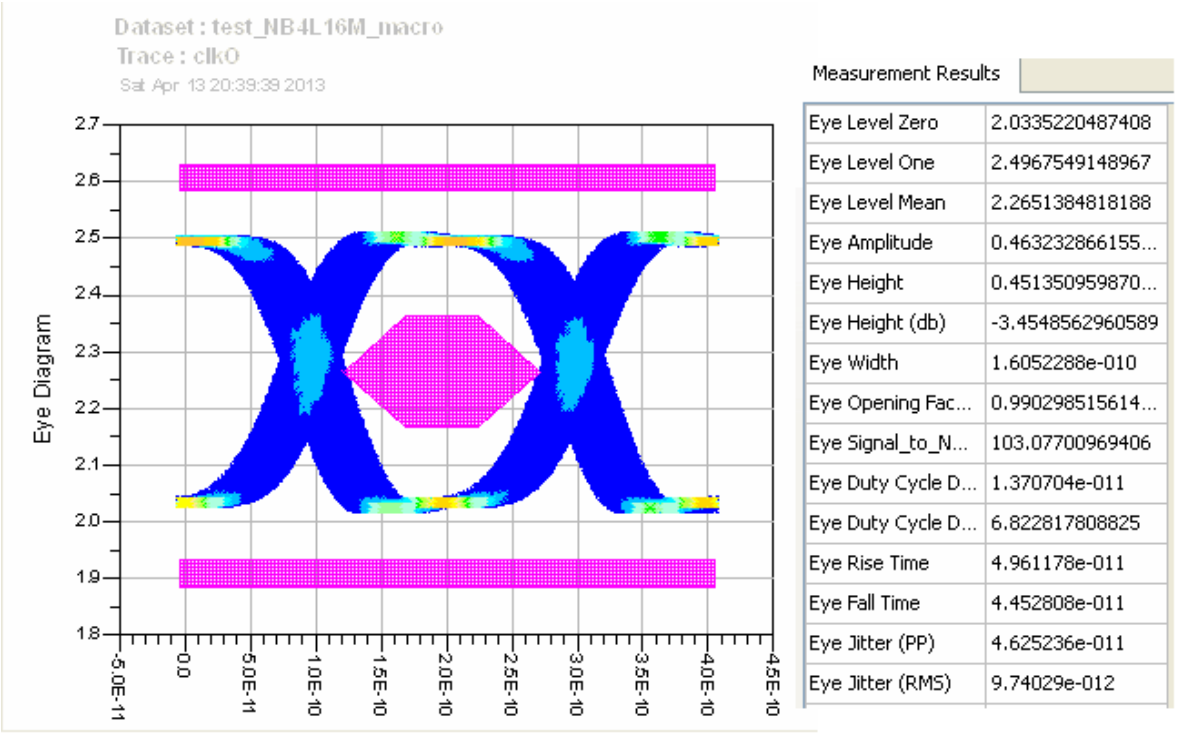
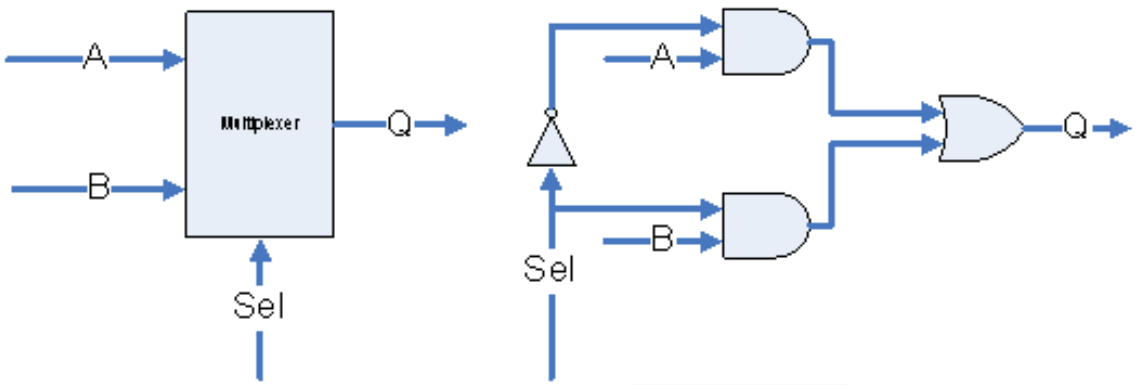


Figure 3-12 Eye diagram of NB4L16M test circuit.

3.4.2 NB7L86M

NB7L86M is a differential 2:1 multiplexer that can be configured into various basic logic gate such as AND/NAND gate, OR/NOR gate, XOR/XNOR gate. Figure 3-13 shows the simple block diagram, its truth table and simulated waveform output from the model.



Sel	A	B	Q
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

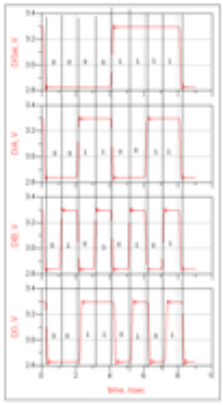


Figure 3-13 NB7L86M symbol, truth table and simulated waveform

The following shows the internal block diagram of NB7L86M. The propagation delay time is measured by connecting two other inputs to Vcc and ground, while toggling the test input with data frequency. Figure 3-14 shows the test circuit and simulation result. The chip typically causes 143ps t_p, which is close to component's datasheet typical specification of 135ps.

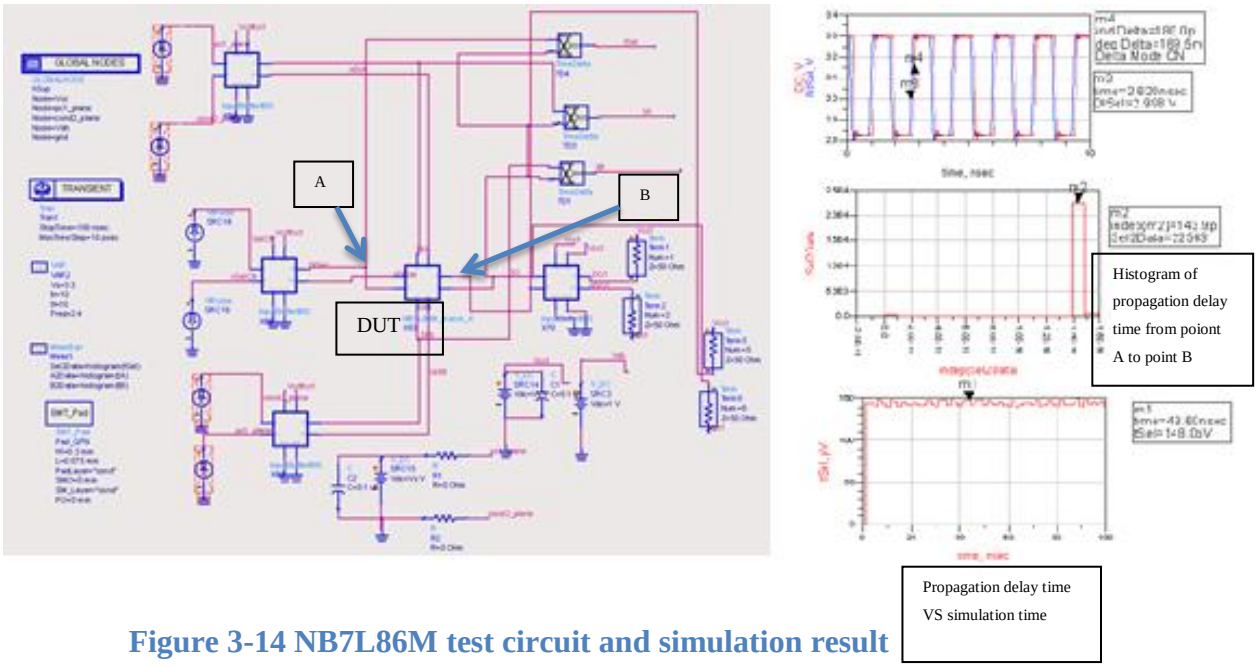
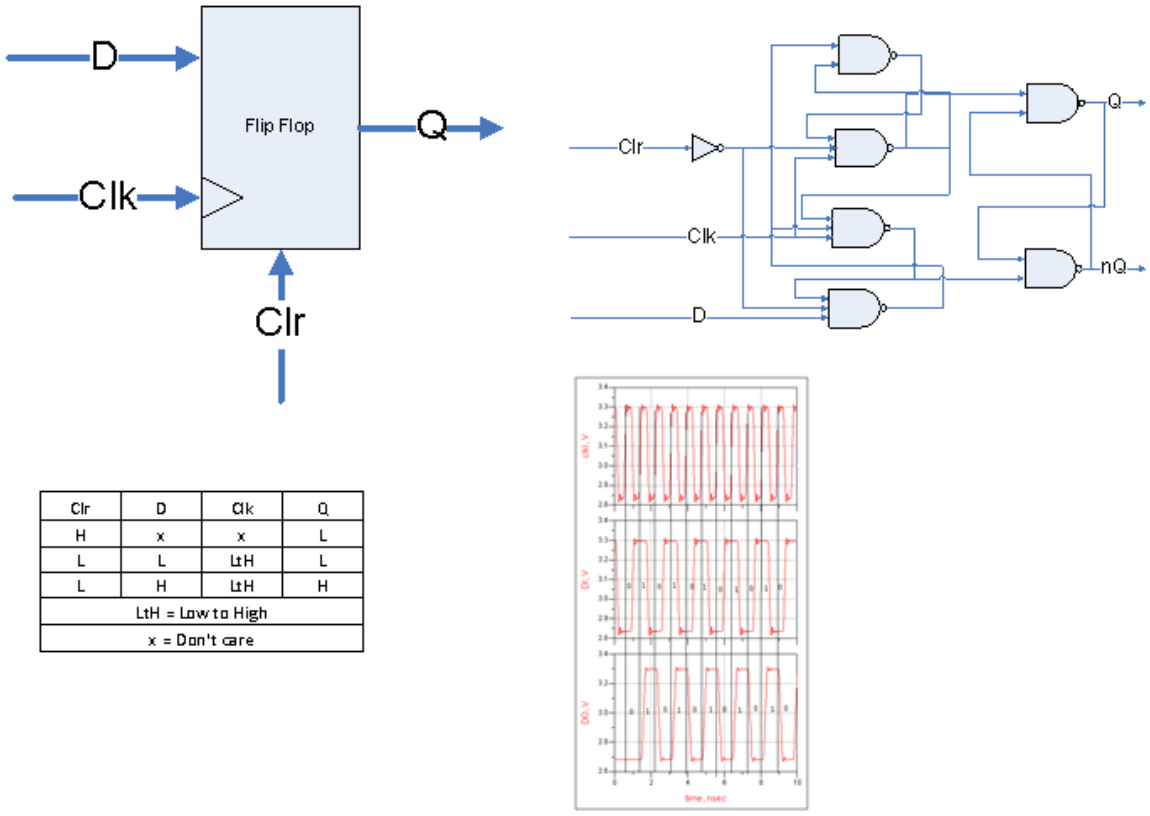


Figure 3-14 NB7L86M test circuit and simulation result

3.4.3 NB7V52M

NB7V52M is a differential D-type flip flop with reset pin. Internally, NAND gates are employed to produce functional level. NAND gates built flip flops is active high reset signal. So invertor is placed at the input of Reset to get active low reset matching actual chip level function. Figure 3-15 shows component symbol, gate level implementation and truth table.



Clr	D	Clk	Q
H	x	x	L
L	L	LtH	L
L	H	LtH	H
LtH = Low to High			
x = Don't care			

Figure 3-15 NB7V52M symbol, functional block, truth table and simulated waveform

Figure 3-16 shows chip test bench and simulation result. Simulated t_p, measured from rising edge of clock to changes in Q, is 207ps. The data sheet specifies 200ps typical value.

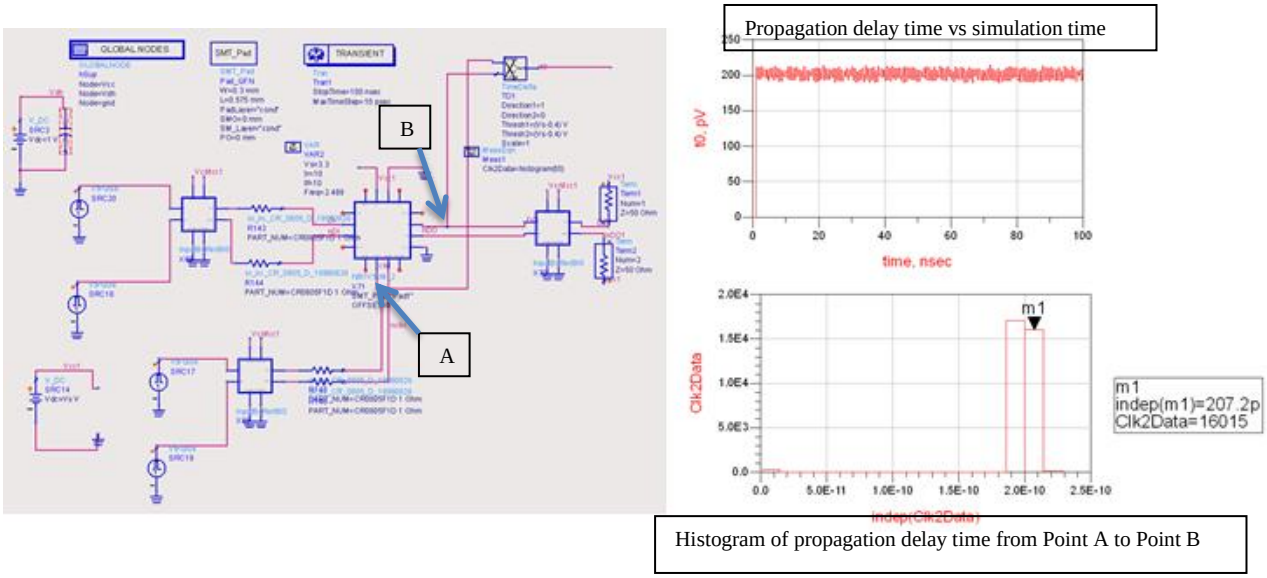


Figure 3-16 NB752M test bench and test result

3.4.4 NB6L14M

NB6L14M is a differential 1:4 CML fan-out buffer. The chip forms the core of clock distribution network and fan-out buffer for the feedback gate. Figure 3-17 shows the internal chip design of fan-out buffer.

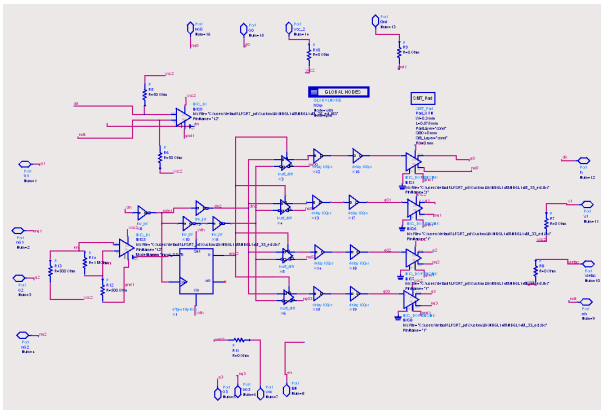


Figure 3-17 Internal chip design of NB6L14M

Figure 3-18 shows the test bench and simulation output. The t_p of signal from various outputs is 361 ps, which is not so much different from data sheet number of 350ps.

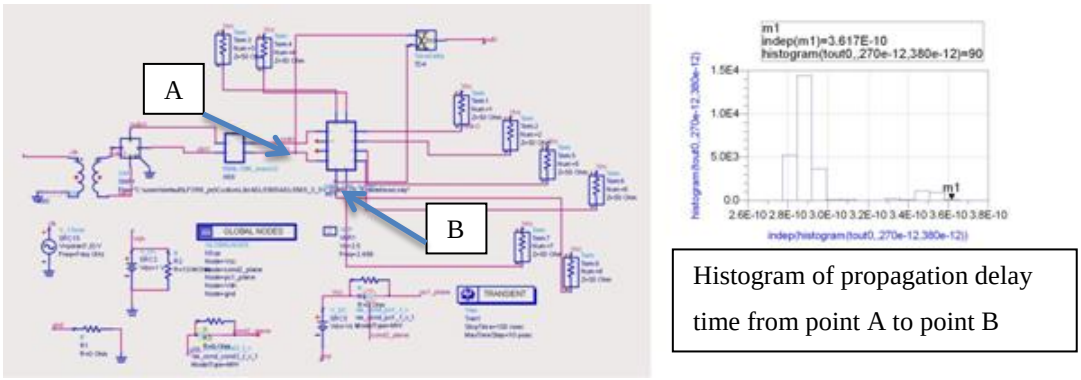


Figure 3-18 NB6L14M test bench and test result

3.5 Analog circuit

The circuit diagram using ADIsim is transferred to the ADS schematic diagram. IBIS model is not available for the PLL components. Chip level S-parameters are also not available. Behavior modeling of PLL circuit design is built. It will be partitioned into the components according to the function.

By using PLL design guide template from ADS environment, the behavior modeling is designed. All the circuit parameters are made reference to the circuit design obtained using ADIsim software. The envelop simulation is performed to make sure the performance of the schematic capture is agreed with the result from ADIsim software. It also takes significantly lesser time than transient simulator. Figure 3-19 shows the schematic design. Figure 3-20 shows the comparison of simulation results. The left hand side shows the simulation result from ADIsim and the right hand side shows the result from ADS synthesizer transient response. The shape of the results agrees with each other.

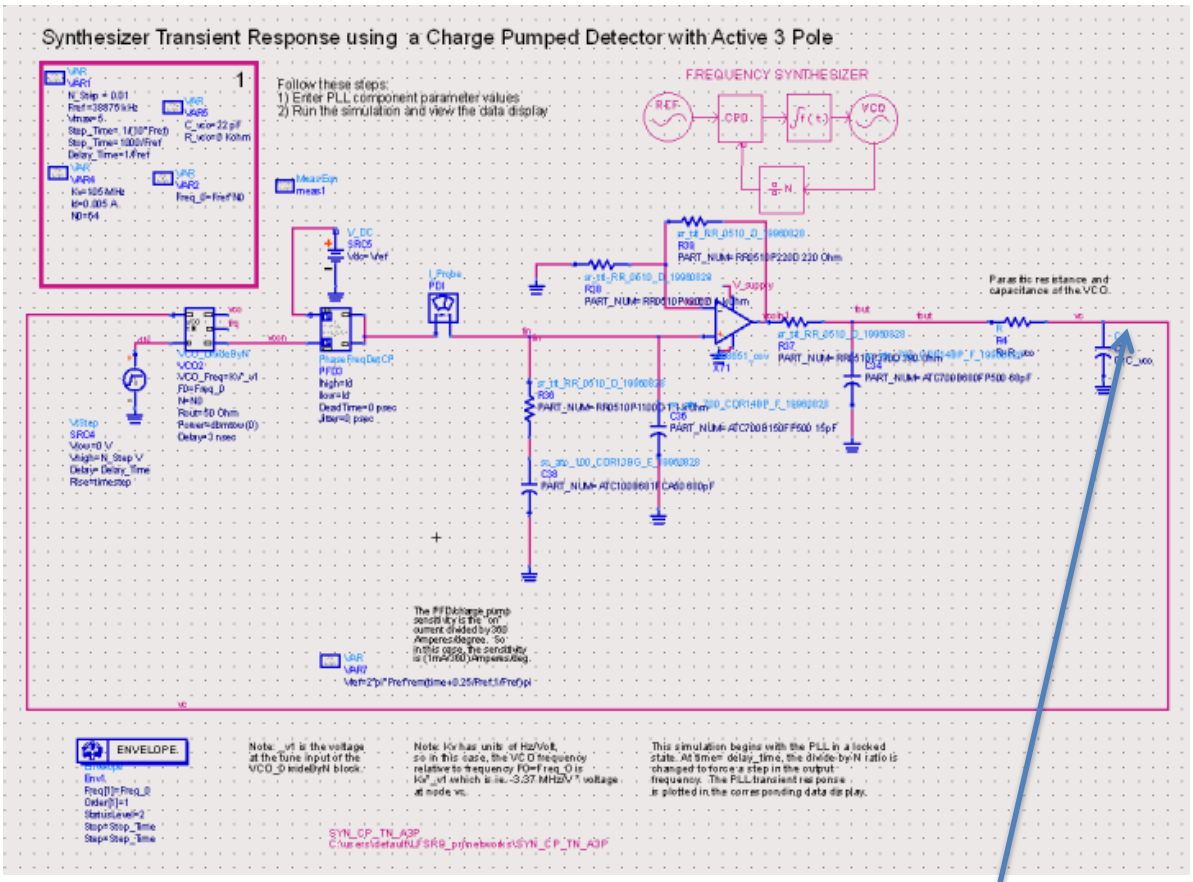


Figure 3-19 PLL transient response

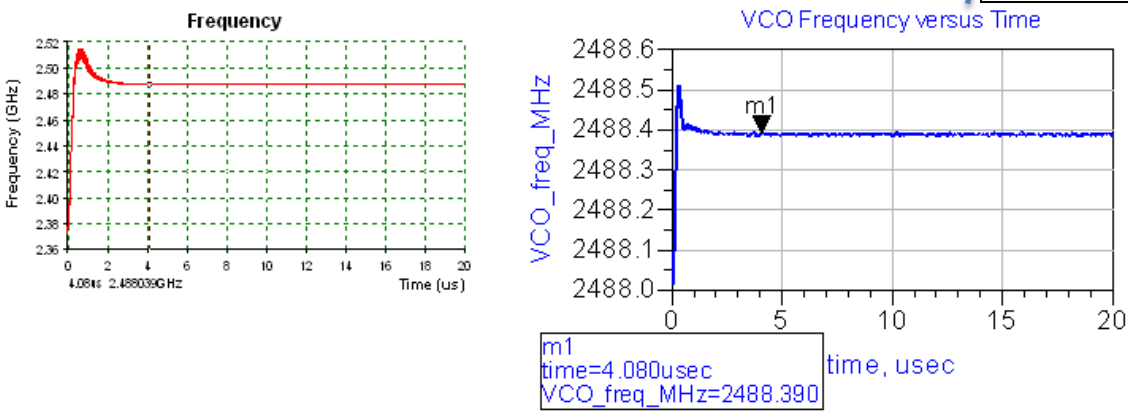


Figure 3-20 Simulation result comparison between ADIsim and ADS simulation

Figure 3-21 shows the noise performance simulation circuit. All the noise parameters are extracted from component data sheets. All the lump components are from ADS SMT capacitor library, ATC series. The sweep frequency is from 1Hz to 10GHz.

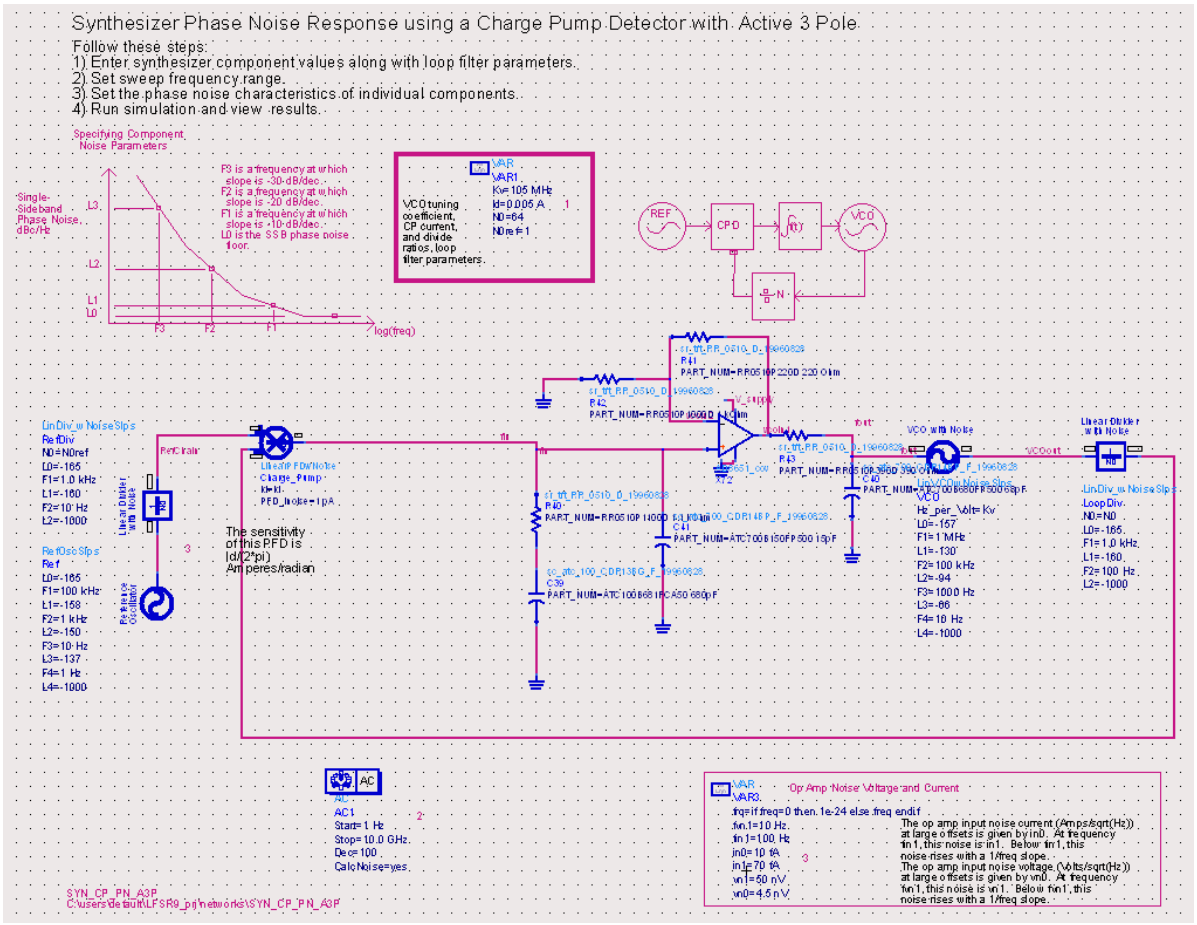
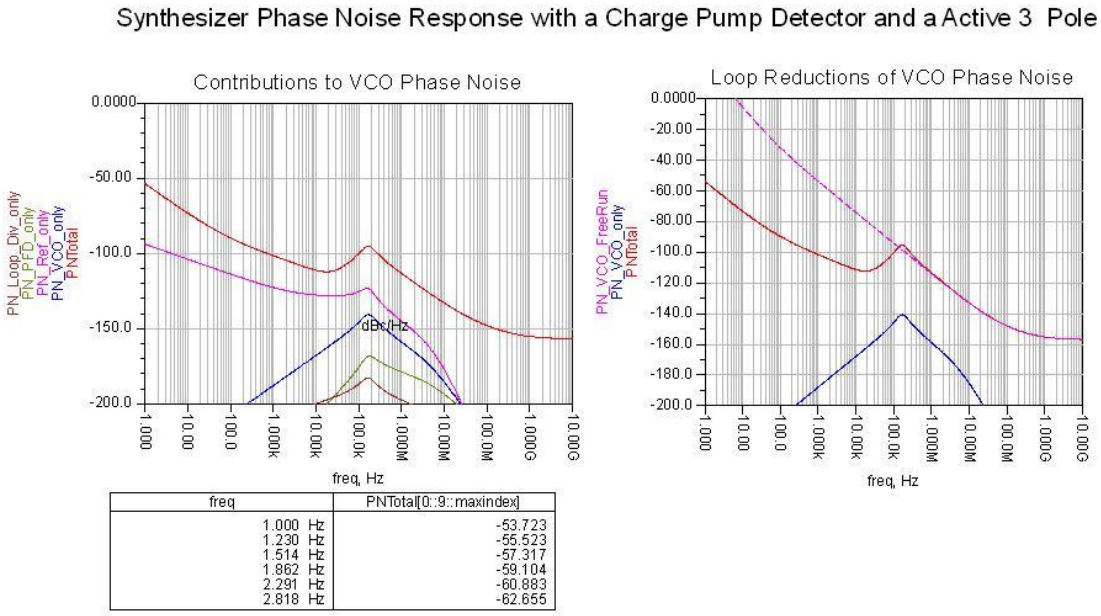


Figure 3-21 Synthesizer phase noise response

shows the simulation result. The red solid color line shows the overall circuit phase noise. The left hand side figure shows the noise contribution from various sources. The right hand side figures shows how loop filter performance from noise. At the low frequency, the loop attenuates the noise. Starting from bandwidth frequency (around 1MHz), the loop is no longer able to attenuate the noise but it is still tracking the input VCO noise.



PN_LOOP_DIV_ONLY = phase noise contributed by loop filter

PN_PFD_ONLY = phase noise contributed by PFD

PN_REF_ONLY = phase noise contributed by reference crystal

PN_VCO_ONLY = phase noise contributed by VCO

PN_TOTAL = total phase noise

Figure 3-22 Noise performance simulation result of PLL

3.6 Digital circuit

Figure 3-23 shows the basic test bench circuit for LFSR circuit design with reset circuit. The four NOR gate in the circle is a small circuit to generate a proper two sets of reset pulse to make sure that the circuit being reset properly.

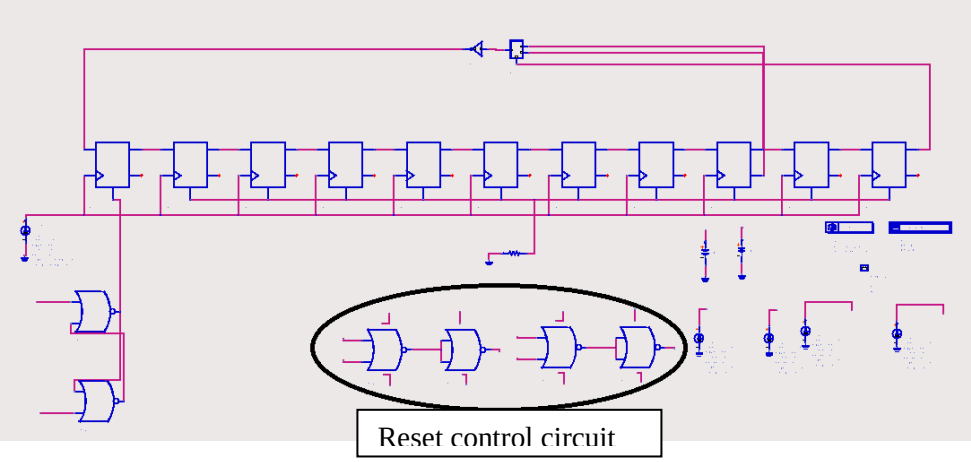


Figure 3-23 LFSR circuit test bench

The clock signals, reset signals and data signals are exported to MATLAB environment. By using getbitstreams_p.m (shown in Appendix 1.1), all the analog signals are converted to digital bit stream. flipflopsimu.m (shown in Appendix 1.2) is the MATLAB code to generate the PRBS digital bit stream.

Figure 3-24 shows how the simulated circuit output match with ideal PRBS bit stream. Cross-correlation between the two signals shows that the two signals are perfectly match.

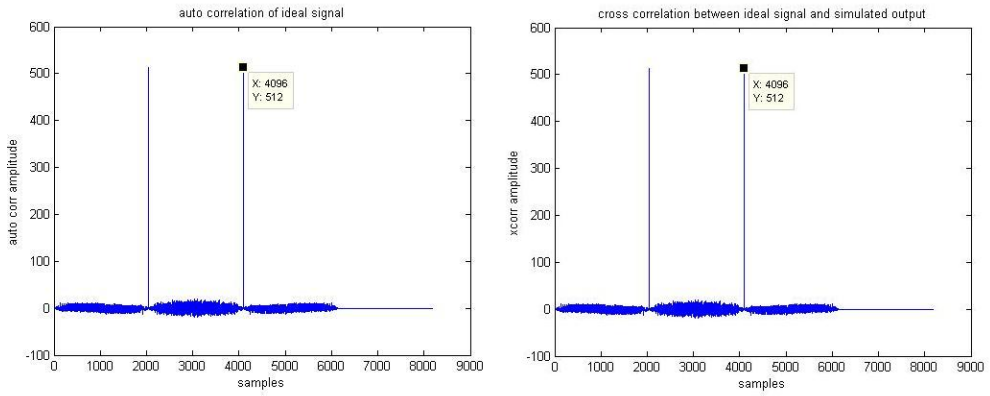


Figure 3-24 Matching of ideal signal and simulated signal

All the chips are using CML interface, which can only support one fan-out. Therefore fan-out buffers are necessary, especially clock distribution

network. An important assumption for shift register design is that all the clock signals reach to respective flip-flops at the same time. The operating frequency is 2.488GHz. So all the data has to settle down within 401.93ps before the next clock circle arrive. Figure 3-25 shows the timing diagram of the circuit. At the clock edge 1, the data D0 starts to change, but only after 200ps, the new data, D1 arrives at the stage A. The same thing happens at stage B, C and D. After the clock edge 9, stage A, stage B, stage C and stage C with have the data of D9, D8, D7, D6 respectively.

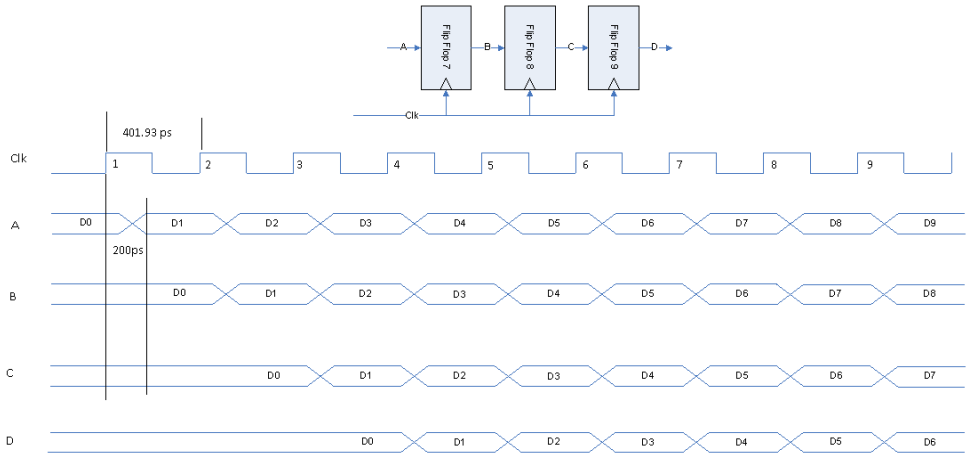


Figure 3-25 LFSR timing diagram

The fan-out buffer's t_p is 350ps. If the fan-out buffer is inserted between two flip-flops, together with flip-flops' t_p, the resultant t_p is 550ps, which is more than operating period of 401.93ps. The signal will not be able to reach to the input of subsequent flip-flop on time. Figure 3-26 illustrates the point. D0 at the stage B1 is not ready at the clock edge 3 and causes the data late by 1 clock cycle at the stage C. After the clock edge 9, stage A, B, C and D have the data of D9, D8, D6 and D5 respectively. At stage C and stage D, the data is corrupted.

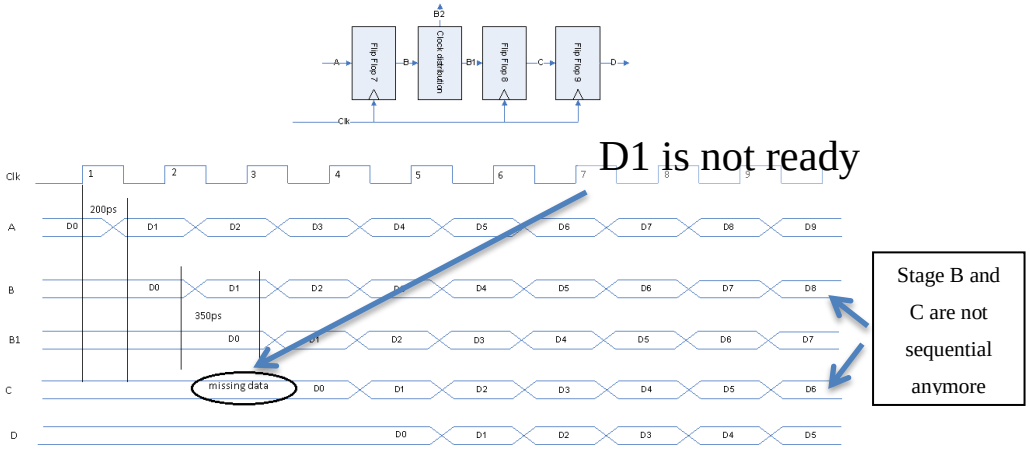


Figure 3-26 Missing data illustration

The solution is to remove the flip-flop 8, letting fan-out buffer acts at flip-flop8. Figure 3-27 shows that stage A, B, and D has restored the data sequence of D9, D8 and D6 respectively. It is similar to the data sequence of the first circuit with flip-flop8 and without fan-out buffer.

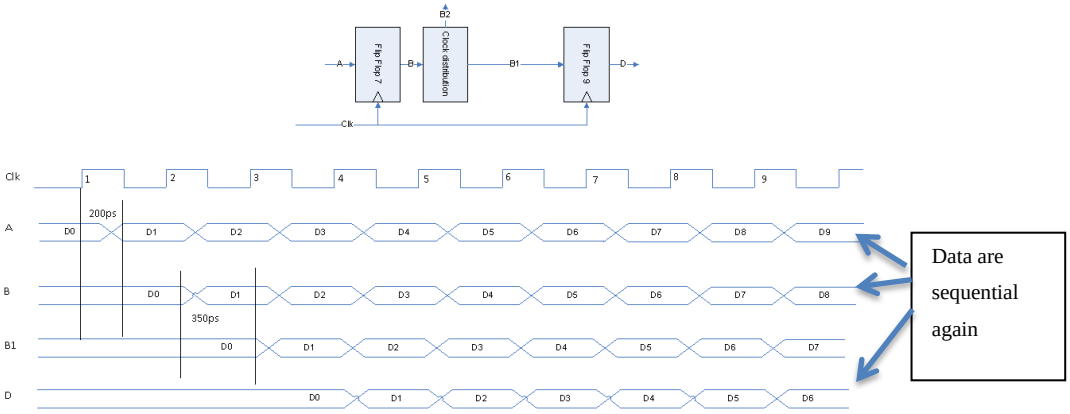


Figure 3-27 Circuit with flip-flop 8 removed

Fan-out buffers have to be inserted at tap 8 and tap 10. Tap 8 is to tap out the signal for feedback gate. Tap 10 is to tap out the LFSR signal to outside port. In this project, flip-flop 4 and flip-flop 11 is taken out to replace the fan-out buffers. Figure 3-28 shows auto correlation of simulated output. Tap8 and tap 10 are replaced with fan-out buffers. All the clock signals are driven from clock distribution network. The output is checked against ideal bit

stream using previous method. Cross-correlation between the ideal signal and it shows perfectly match.

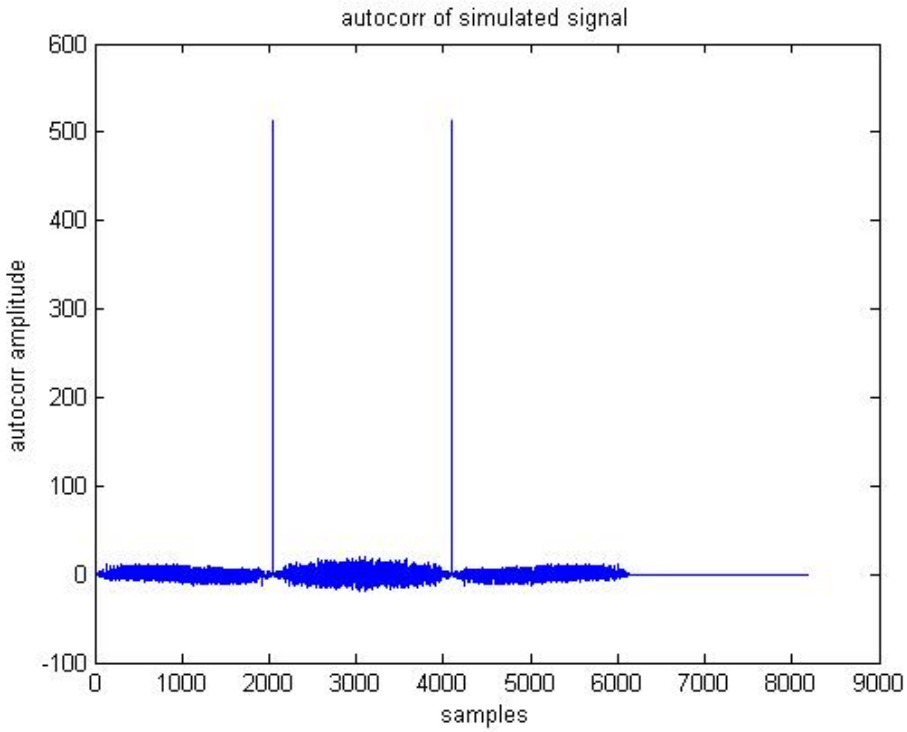


Figure 3-28 Overall LFSR design with simulation verification

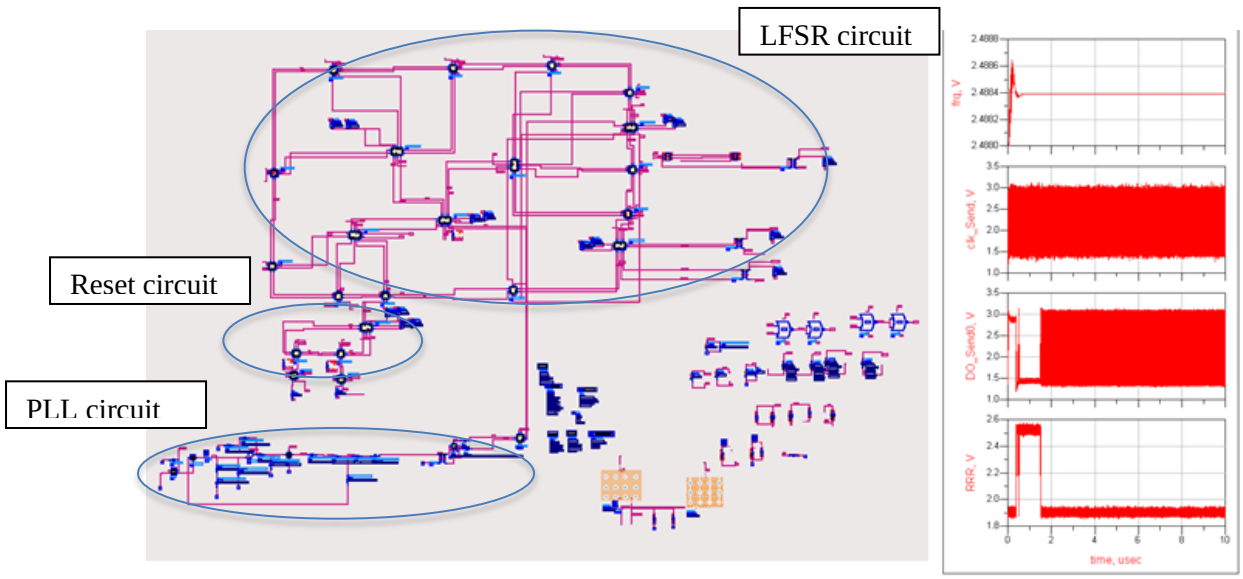


Figure 3-29 Overall simulation of LFSR circuit

Figure 3-29 shows the time domain result from simulating with both analog and digital circuit together. As shown in the schematic, there is a

partition between analog and digital circuit. The flip-flops are placed in circular shapes. The clock distribution network is placed at the center to ensure that all clock signals will reach the flip-flops at the same time. Below is the analog PLL circuit. The right hand side of the figure shows the PLL will generate the constant frequency within 1us. A reset signal is generated around 800us.

Figure 3-30 shows the eye diagram for data out. It is measured with rise time, fall time threshold of 20%-80% and eye boundary of 40%-46%.

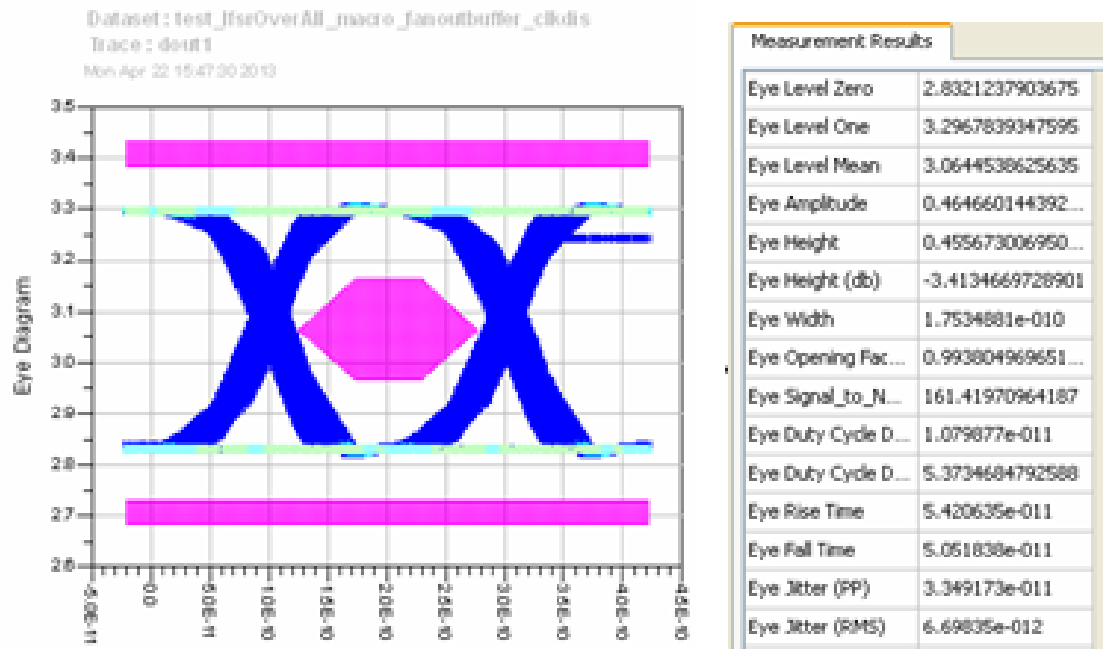


Figure 3-30 Eye diagram for Data out

4 Layout design

After the schematic design, the layout of the circuit is designed. The main consideration is noise performance. For the purpose of PCB level simulation, it involved modeling of substrate, defining of layout layers, the port naming and s-parameters extraction from trace model.

4.1 Substrate modeling

The first component to model in layout design is substrate. It defines the parameters of PCB that will be used to fabricate the chip design. In this project, FR4 substrate is used and its parameters are defined in Table 4-1. Four layers PCB is considered.

FR4 substrate	Parameter	unit
Thickness (overall)	1.6	mm
Relative Permittivity (ε_r)	4.5	
Relative Permeability(Mu_r)	1	
Loss Targent	0	
Impedance	48	mOhm/square

Table 4-1 FR4 parameters

The substrate model is extracted before layout is drawn. It will map various software layout layers to the physical PCB substrate. In ADS environment, it is called metallization. In this layout, four layers PCB is considered due to extreme low noise requirement, as followed, 2 layers for signals, one layer for ground plane and the last one for the power plane. The substrate between power plane and ground plane can be served as a coupling capacitor. The substrate model is shown Figure 4-1.

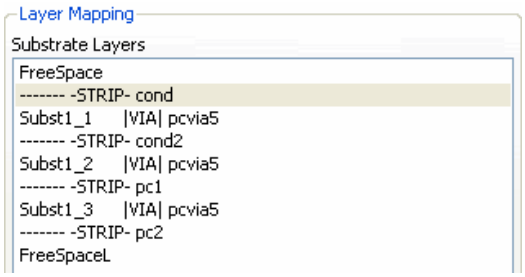


Figure 4-1 Substrate model mapping

This is a 4 layer boards, the upper most layer is signal layer. The second layer is ground plane, the third layer is power plane and the bottom layer is signal layer. The reason to separate the layers is to keep the noise as low as possible. By putting two power planes together at the center, it can also act as a coupling capacitor between ground and Vcc. The main concern is coupling noise from clock to the data signal. By physically separating them, the coupling noise is reduced to minimal.

Table 4-2 shows the detail of layer mapping. The cond and pc2 layers are mapped to signal layers. The cond2 and pc1 layers are mapped to ground plane layer and power plane layer respectively. pcvia5 is connected via layer which connects all the signals and reference layers. Hole layer is for drill layer. Those layers are physical layers meaning that they can be seen on the actual PCB board.

layer	Physical meaning	logical/physical
cond	signal layer	physical
cond2	ground layer	physical
pc1	power layer	physical
pc2	signal layer	physical
pcvia5	via layer	physical
hole	hole layer (for drill)	physical
pcvia1	cond clearance layer	logical

pcvia2	ground clearance layer	logical
pcvia3	power clearance layer	logical
pcvia4	pc2 clearance layer	logical

Table 4-2 layer mapping

There are other fours logical layers, which cannot be found on PCB board. They are logical layers which are used to create clearance of respective plane. Figure 4-2 shows a typical trace on cond layer on PCB board.

In the layout design simulation, all the ports are needed to make reference to ground plane in order to get better realistic result.

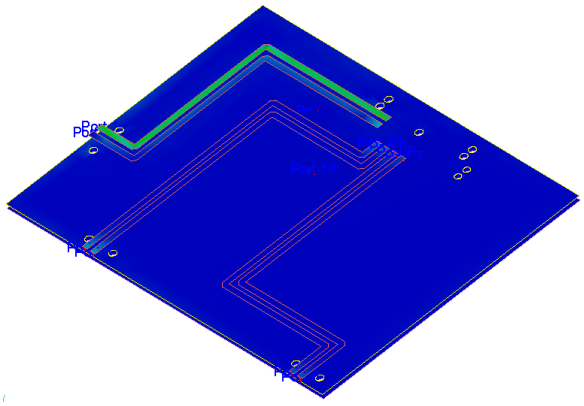


Figure 4-2 PCB board modeling

4.2 Trace modeling

The design step for trace design as followed. Firstly, the minimum length of the micro strip that needs termination is calculated. The relationship between bandwidth and rise time (T_r) is described in equation 4-1 [5].

$$Bandwidth = \frac{0.35}{T_r} \quad 4\text{-}1$$

The rise time can be taken from component vendor's IBIS model file, which is found to be worst case of 71ps. So the bandwidth is 4.93GHz. The equation to find the delay for a signal traveling through a micro-strip configuration is described in equation 4-2 [5].

$$delay = 85 * \sqrt{0.475\varepsilon_r + 0.675}\ ps\ per\ inch \tag{4-2}$$

On a FR4 board, with permittivity of 4.4, the delay is found to be 141.34ps per inch. Using the wavelength equation, the wavelength of the current circuit board is 1.43 inch.

$$wavelength = \frac{speed}{frequency} \tag{4-3}$$

The termination is required for the transmission longer than wavelength/10 [5]. For this project, any trace longer than 0.143 inch (3.6mm) will need a proper termination. Both parallel and series terminations, Figure 4-3, are employed in this project in order to improve signal integrity.

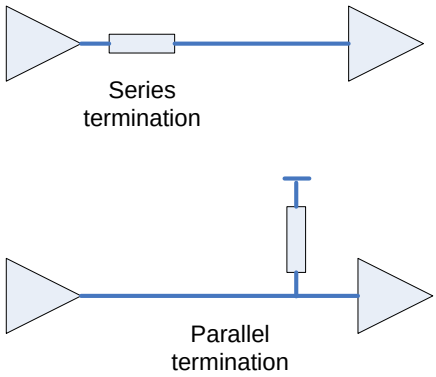


Figure 4-3 various termination scheme

4.3 Component's foot-print

There are two ways to generate foot-print. Manual drawing and generating foot print using scripts. This project make used of ADS's AEL scripts to generate various QFN and SMT standard foot prints. It allows easy generation of foot prints with minimum development time spent. Appendix 1.3 shows sample AEL script to generate QFN16 foot print. Pad size of the components has to be defined while building the model. That gives the designer freedom to use different Pad sizes for same component foot print. The example on how to generate a foot print has been demonstrated at page number 3-7, an example of producing foot print for NB4L16M.

For customized foot prints, it is manually drawn according to the dimension provided by the components' data sheet.

4.4 Via-hole modeling

One of the important layout designs is via design. In a multi-layers PCB design, a via-hole is used to connect two desired planes without connecting to other planes. Three types of via exist, through hole via, blind via and Buried via. Only through hole via is employed due to the ease the component prototyping. Step by step via design is shown as follow.

1) Define the pad of destination plane
2) Define the pad of source plane
3) Define the clearance layer for other planes. The clearance layer disallows the unrelated planes connected to the corresponded pad.
4) Define the hole layer for drilling information.

Figure 4-4 shows via 3D design that connects cond layer to pc1 layer using pc5via. At cond2 layer and pc2 layer, there is a clearance between pc5layer and the respective planes.

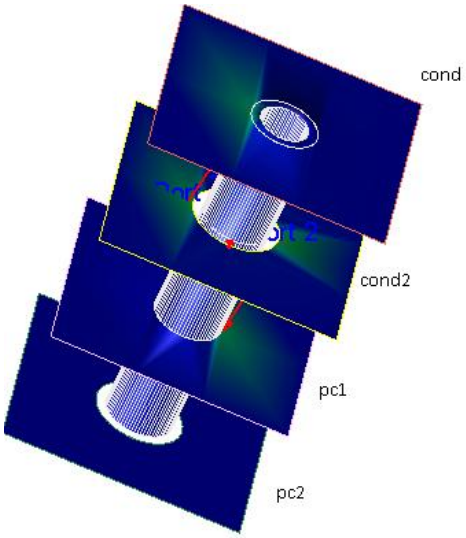


Figure 4-4 A via design

4.5 Layout rules

Various components' datasheets and industrial recommendation such as [5][6][7][8] are consulted for the PCB board performance. Component placement is one of the critical parts of the design process. Optimized component layout contributes better circuit noise performance and reduced layout size.

The following rules are enforced during the layout process.

1) Reduce as much via as possible
    a. To reduce impedance discontinuities as much as possible
2) Provide same amount via for differential traces pair
    a. To make sure the trace pair faces the same common mode interference.
    b. To avoid conversion of common mode interference to differential mode interference
3) Provide As much ground island as possible
    a. To give better return path for the trace.
4) Avoid 90degree band, instead use the curve band
    a. To minimize impedance discontinuities

5) Split the power and ground plane as much as possible
    a. To reduce the coupling noise
6) Place the termination resistors as close to the receiver end as possible.
    a. To give better termination

4.6 Analog design

Analog ground is separated from digital ground. It takes 40mmx25mm foot print. Figure 4-5 shows circuit layout and layout level simulation setup. All the capacitors are placed as near to the respective ICs as possible.

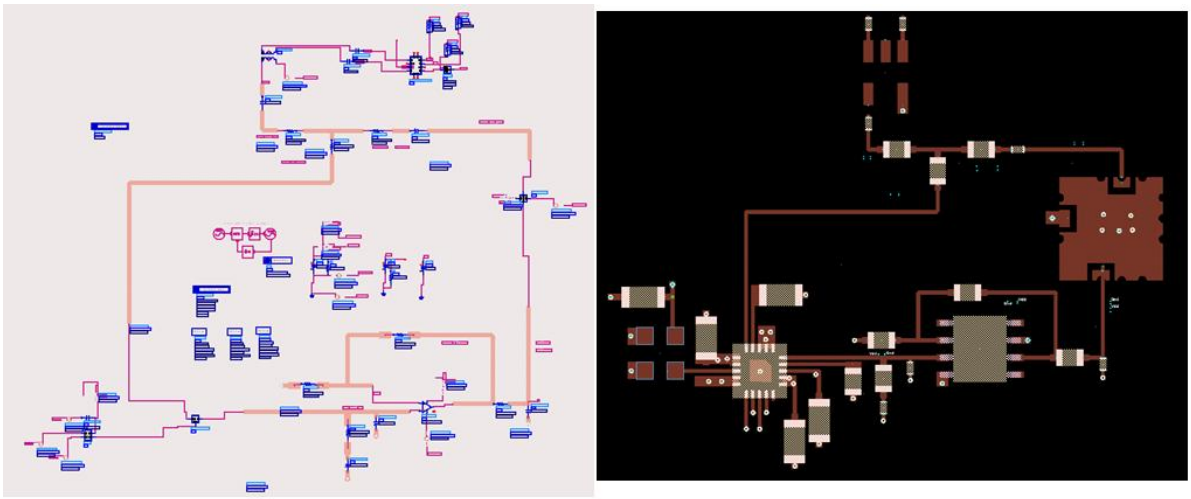


Figure 4-5 PLL layout level simulation and design

The output of analog design PLL circuit is 2.488GHz differential clock signal which will be connected to clock distribution network of LFSR design. Figure 4-6 shows simulation output with CML logic level.

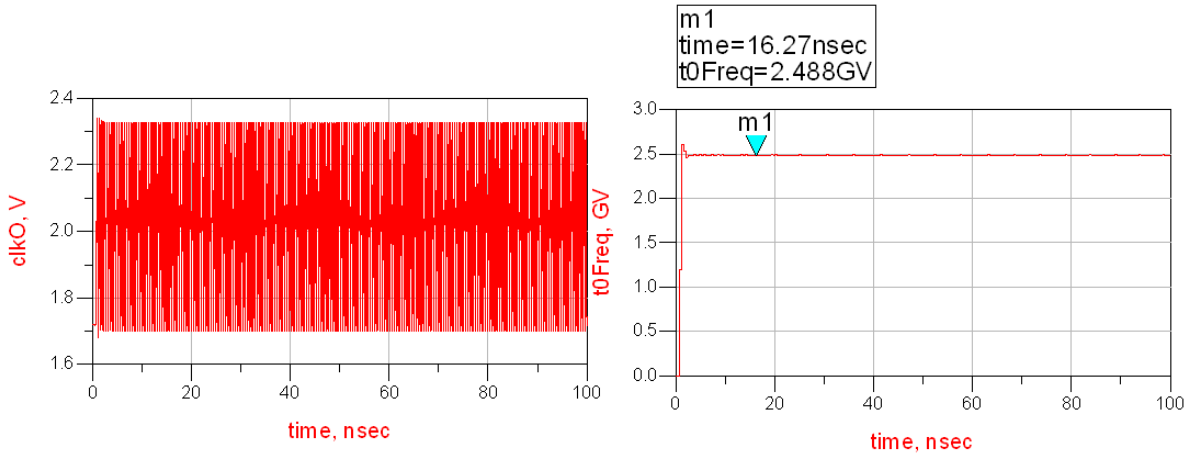


Figure 4-6 PLL layout level simulation output

4.7 Digital design

A circular layout pattern with clock distribution network at the center is chosen. It provides the following benefits,

1) Constant latency for all the clock signals connected to the flip flop.
2) Constant data line length of flip flops because of circular shape.

Figure 4-7 shows the various clock trace latency simulation circuit and result. The clock drivers drive three flip-flops and the timing is measured at three different locations. It shows that clocks from different traces reach to the respective destination at the same time, which is around 113ps.

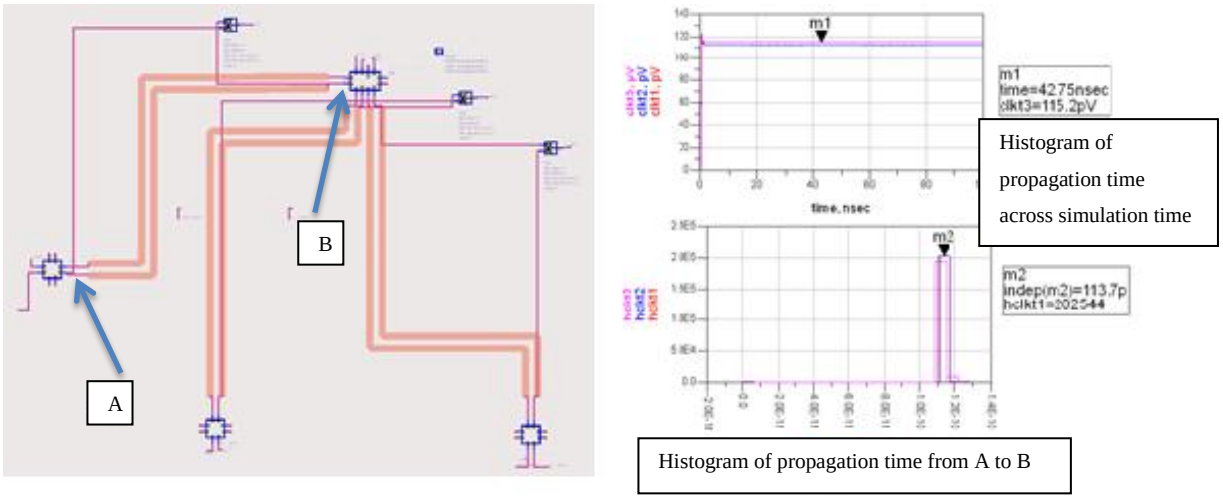


Figure 4-7 Signal propagation delays from various clock traces

Figure 4-8 shows the propagation delay time for the data signal travelling through the typical data trace of the circuit. The simulation shows most of the time, it needs 75ps delay at the worst case. Together with 200ps propagation delay time of D-type, it is still within the data settling time requirement of 401ps, for 2.488GHz operation frequency.

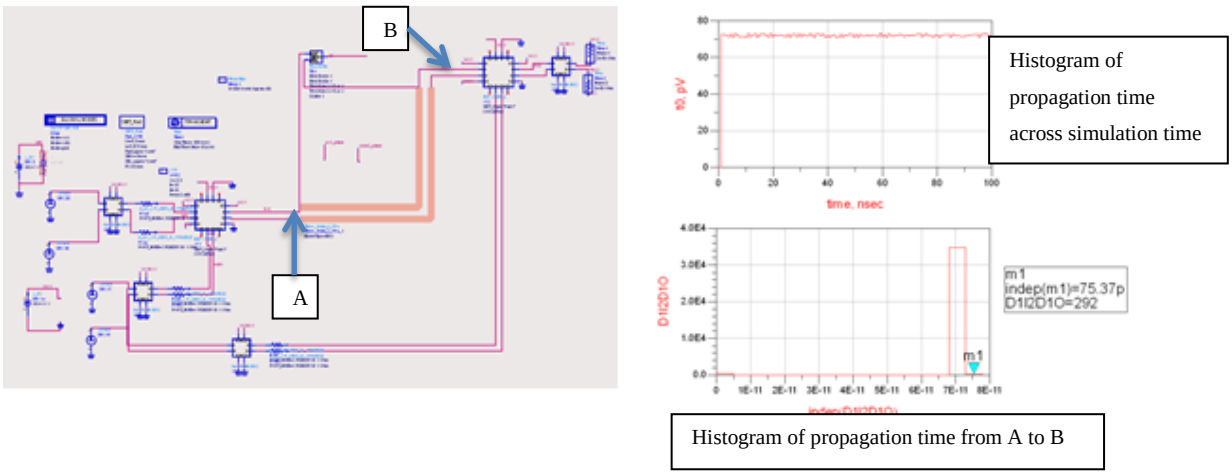


Figure 4-8 Signal propagation delay for data trace

The data trace with largest t_p is the connection from tap8 flip-flop to feedback gate (Figure 4-9). The feedback gate, which is a multiplexer, has three set of inputs, namely, SEL, A and B. SEL signal comes from tap10 flip-flop and it is considerably short. Signal A and B are from tap 8 flip flop. Based on the current layout design, the two data traces have longer trace length and have to go through via holes, which make them having the largest propagation

delay time. Based on the same method used in Figure 4-8, the propagation delay time of trace from tap8 to input A is 250ps worst case (Figure 4-10 blue trace, cursor m2) and for the trace from tap8 to input B is 218ps worst case (Figure 4-10 red trace, cursor m1). After adding t_p of fan-out buffer (350ps), the total tp is 600ps and 568ps.

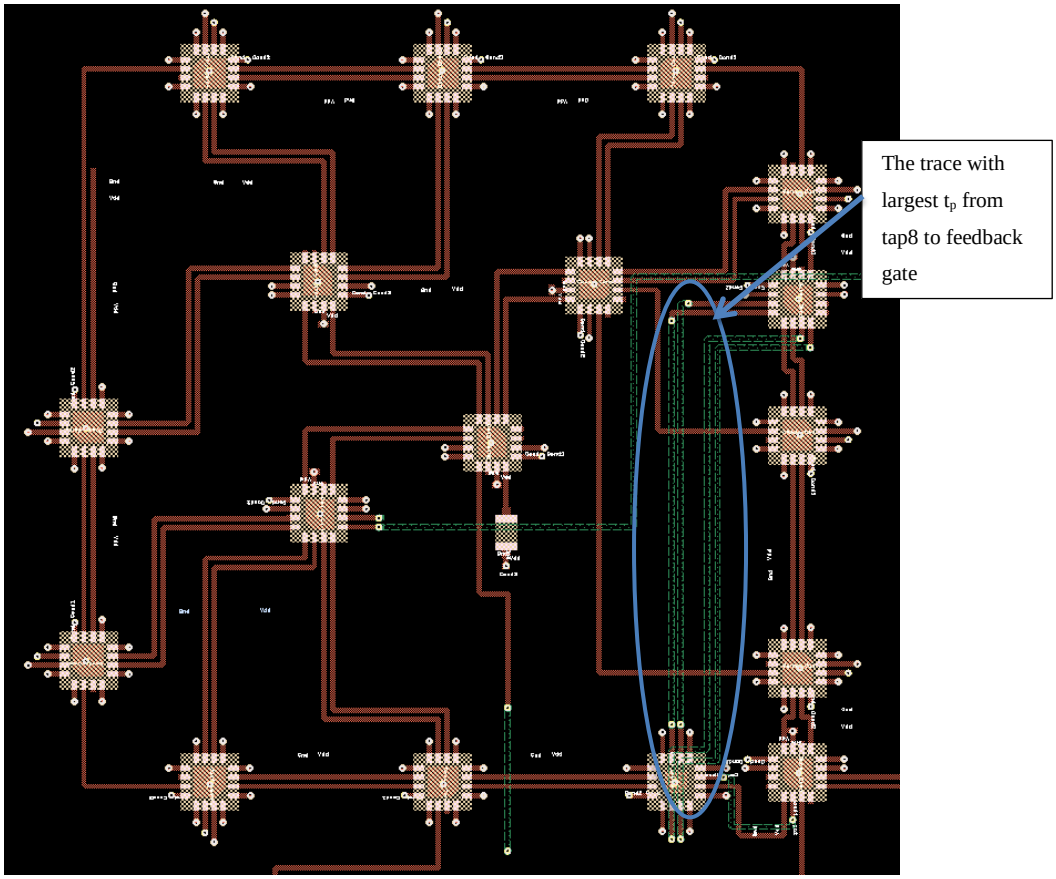


Figure 4-9 the trace with largest t_p

The feedback gate has around 150ps latency, and all the data need to settle down within 401ps. So the data need to reach feedback gate input by 250ps after the preceding clock edge, which is significantly less than 568ps.

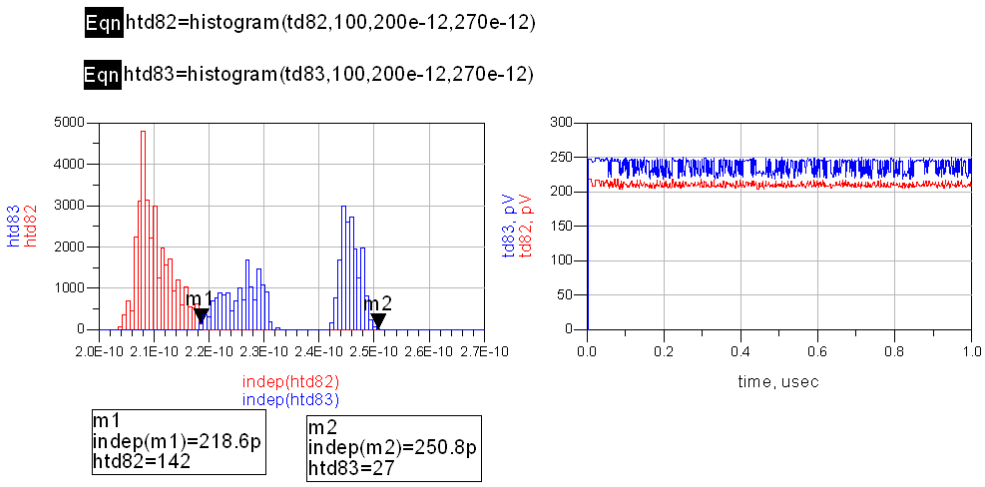


Figure 4-10 t_p of data from tap8 to multiplexer

To demonstrate the problem, Figure 3-27 can be modified with the delay elements replacing the connection between flip-flops (Figure 4-11). The time taken for the data from stage Bb to B1b is 400ps while it will take 568ps from stage Bb to B3. At the synchronizing clock edge, the data of B3 is still stuck at previous clock stage and it will affect the output of the feedback gate.

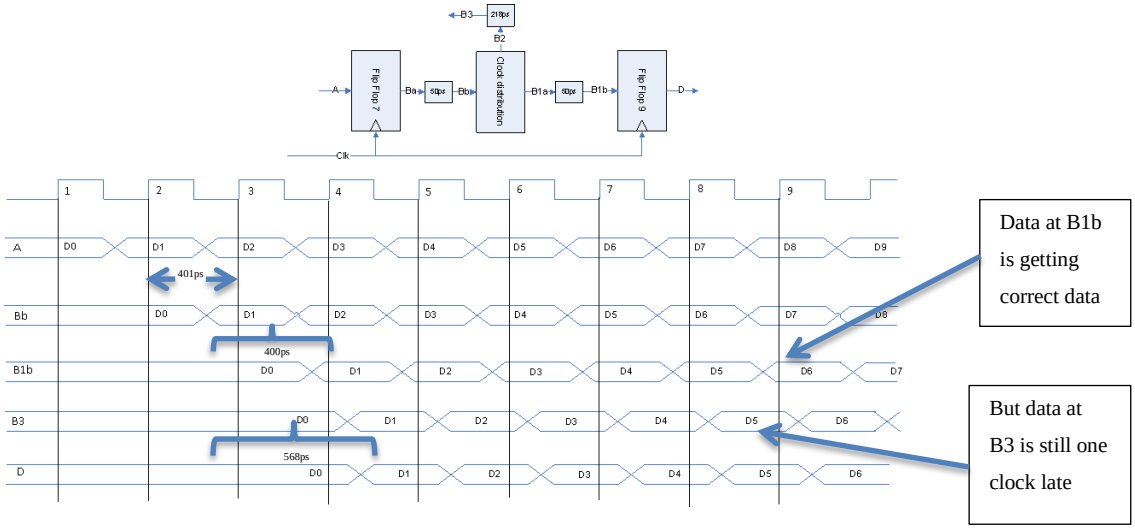


Figure 4-11 Fan-out buffer with the delay model

The solution is swapping the places of the fan-out buffer with flip-flop 7. As shown in Figure 4-12's timing diagram, the data at B3 and B1b are matched at the synchronized clock edge. The allowable time taken for the data

from A to B1b is 802ps due to two clock cycles distance. The data at A has to reach B3 within the timing of 400ps and 650ps to get meaningful feedback gate output. Based on this design, the t_p from A to B3 are 568ps and 600ps, which lies comfortably within that timing range.

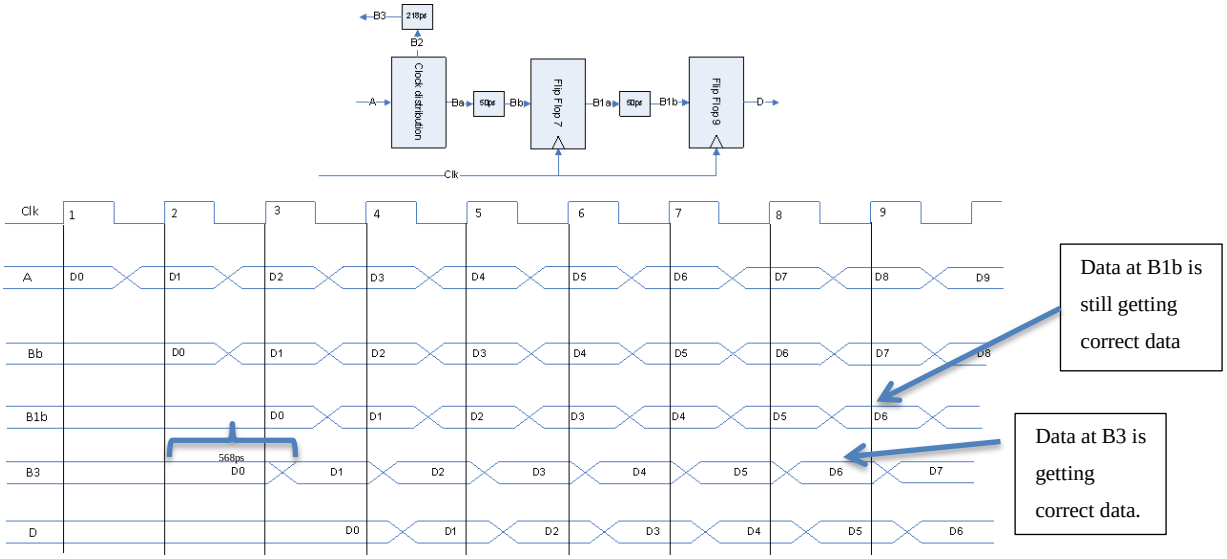


Figure 4-12 Swapping the places of fan-out buffer with flip flop 7

Figure 4-13 shows the final circuit design and the output of cross correlation between the circuit simulation output and ideal waveform.

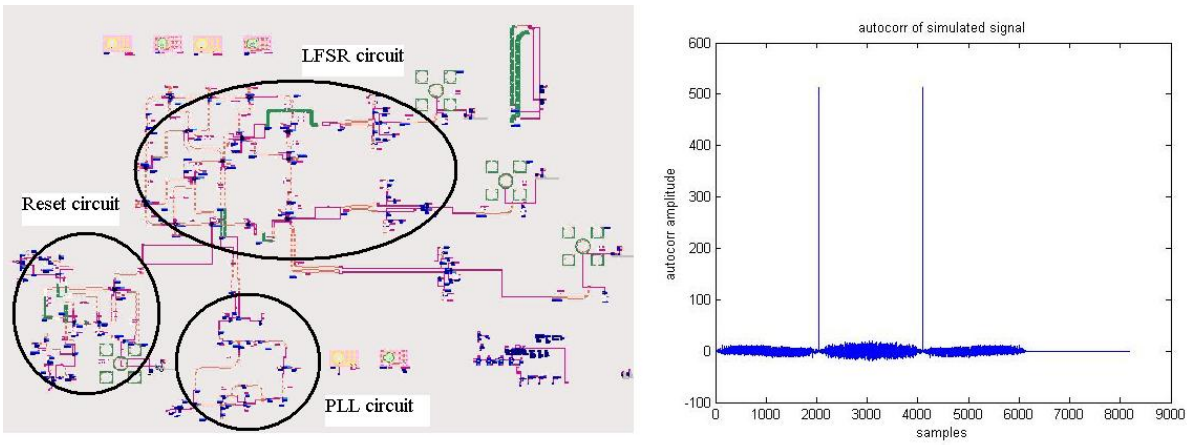


Figure 4-13 Layout level simulation for digital circuit

4.8 Mixed signal design

After designing analog layout and digital layout separately, it is integrated into a circuit board. The main objective in this section is tried to decouple analog noise to digital circuit. Analog layout and digital layout are partitioned. The power planes are separated since analog circuit needs 3.3V while digital circuit needs 2.5 V. The clock distribution network is treated as a analog circuit. Hence, the ground is de-coupled from flip-flops' ground.

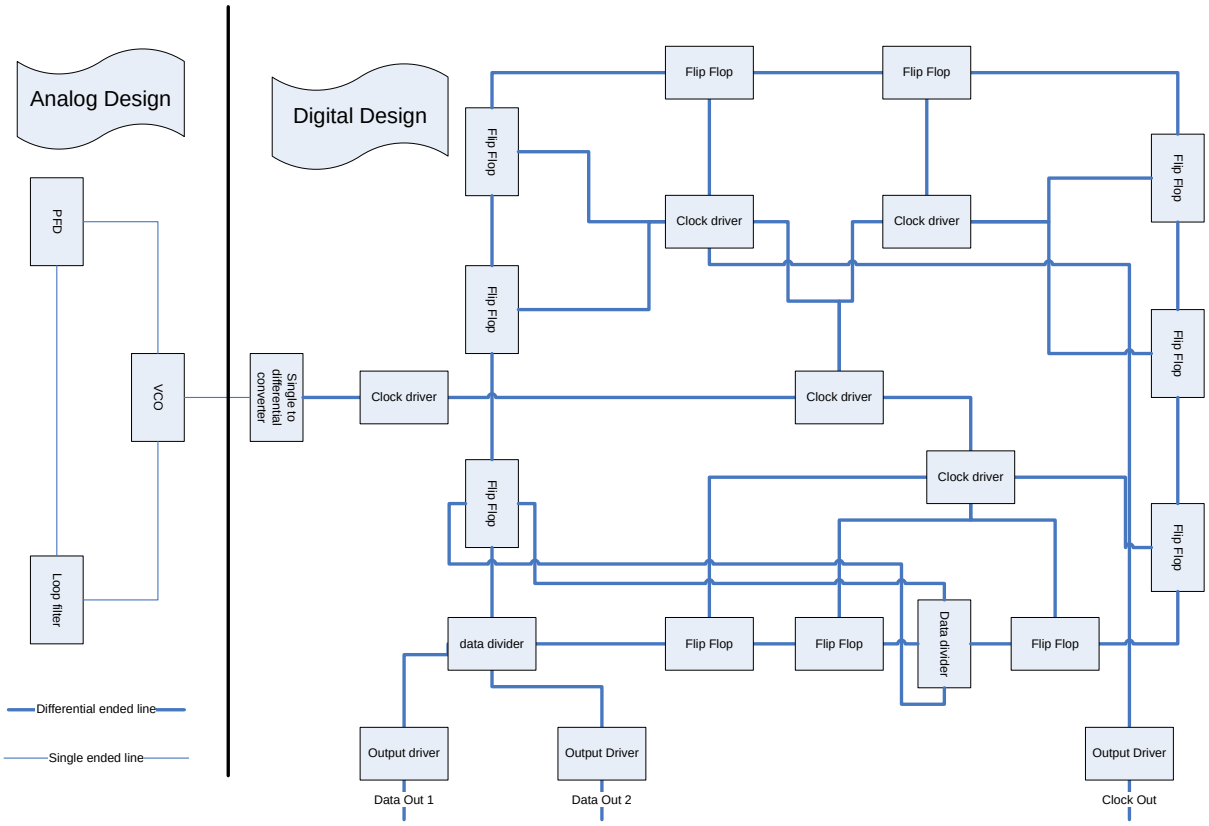


Figure 4-14 Layout Partitioning

Figure 4-15 final layout board shows the final layout. The overall size is 116mm X 116mm size board.

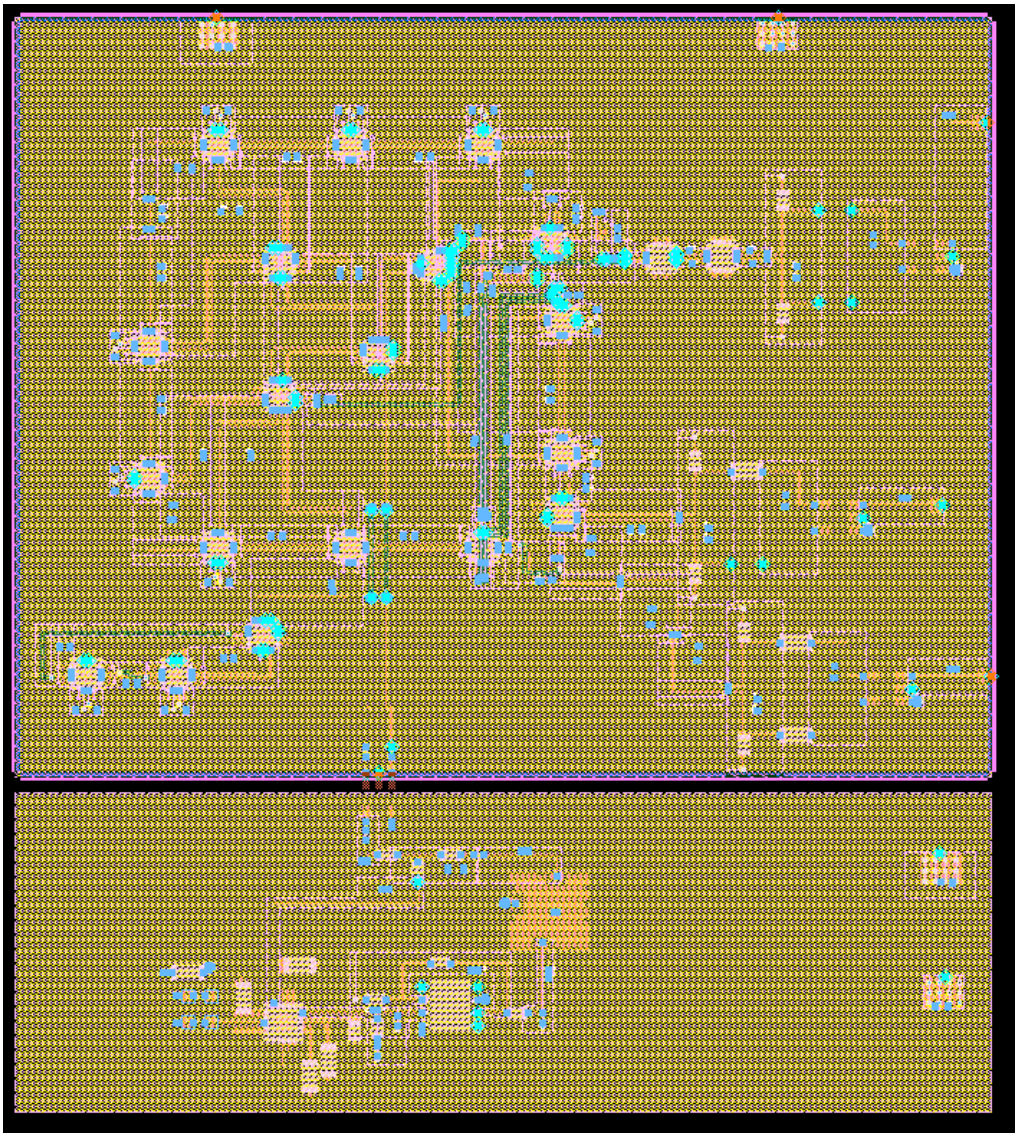


Figure 4-15 final layout board

5 Conclusion

High speed digital circuits are getting more prevalent nowadays. It is very important to perform simulation before the board is manufactured so that the cost will be kept down and the noise generated from PCB can be kept under control. The merit of this project is establishing a frame work and identifies most of the common pitfall to avoid. Since the frame work can cover both analog and digital circuit, any other circuit implementation can be done using this frame work. It will reduce development time on figuring out how to use software and will allow greater focus on the quality of the circuits.

6 Appendix

1.1

Getbitstreams_p.m

```
function [numPackets, relBitTime, serialInStream, clkY, packetLength] = getbitstreams_p( clkY, dataY, enaY, tim)
dataY = deglitch(dataY);
%make it active low
enaY=(-1*enaY)+1;
%% Avoid initial partial packets
% by replacing any leading hi with lo in ena
enaY = deglitch(enaY);
firstLo = find(0==enaY,1);
enaY(1:firstLo-1) = 0;
enaYThreshold = mean([min(enaY),max(enaY)]);

%% Count number of complete packets
numPackets = 1;

%% Find the high/low threshold for data signal
dataThreshold = mean([min(dataY),max(dataY)]);

%% Find the clock low-to-high transitions that happen during Ena==1.
clkY = deglitch(clkY);
clkLoToHi = 1==diff(clkY) & enaY(1:end-1);

%% Loop on enable to find length of each packet
packetIndex = 1;
packetSize = 0;
packetLength = zeros(1,numPackets)';
startIndex = find(enaY==1);
for ii = startIndex(1):length(enaY)-1
  if enaY(ii) == 1
    packetSize = packetSize + clkLoToHi(ii);
  elseif enaY(ii-1) == 1
    packetLength(packetIndex) = packetSize;
    packetSize = 0;
```

```
      packetIndex = packetIndex + 1;
    end
end

%% Generate the bitstreams.
serialInStream  = dataY(clkLoToHi)>dataThreshold;
relBitTime = tim(clkLoToHi==1);
return

function [out] = deglitch(in)
thresholdPercentage=5;
lo = min(in);
hi = max(in);
threshold(1) = lo + (50-thresholdPercentage)/100*(hi-lo);
threshold(2) = lo + (50+thresholdPercentage)/100*(hi-lo);

%% Guess initial state as best possible
out=zeros(size(in));
%  If input really high then 1, else 0.
out(1) = in(1)>threshold(2);

%% Loop (yuck)
%  Next state based on current state and input
for i=2:length(in)
   if out(i-1)
      % if at 1, stay at 1 unless very small
      out(i) = in(i) >= threshold(1);
   else
      % if at 0, transition to 1 if very large
      out(i) = in(i) > threshold(2);
   end
end
return
```

1.2

Flipflopsimu.m

```
function dOut=flipflopSimu
%dOut=x^10+x^8+1;
seed=0;
totalBit=11;
length=4096;
tap1=8; %starting counting from bit0
tap2=10;%starting counting from bit0
dOut=zeros(1,length);
carry=bitxor(bitget(seed,tap1+1),bitget(seed,tap2+1));
for ii=1:length
   dOut(ii)=bitget(seed,totalBit);
   %clock starting ticking here
   seed=bitshift(seed,1);
   seed=bitand(seed,(2^totalBit)-1); %mask out the rest of the bit
   %determine bit0
   if carry == 0
      %it is xnor gate
      seed=bitset(seed,1);
   end
   %prepare for next one
   carry=bitxor(bitget(seed,tap1+1),bitget(seed,tap2+1)); %"not" function is done in if carry
== 0 statement
end
return
```

1.3

AEL script to generate QFN16 footprint.

```
defun smtart_QFN16 (smtpad, offset)
{
  smtart_draw_SMT(smtpad, // smtpad
                offset,   // offset
                3.25,     // package Width
                3.25,     // package length
                0,        // not used
                0,        // not used
                list(0.5,0.5,0.5,0.5),
                list(0.725,0.725,0.725,0.725),
                list(4,4,4,4),
                list(0.3,0.575,0.3,0.575,0.3,0.575,0.3,0.575),
                list(-90.0,1,4, 180,16,13,90.0,9,12,0,5,8,1),
                0,
                "mm",
                "portOpt3",
                 0,
                 NULL);
}
```

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