FABRICATION AND PATTERNING OF METAL AND METAL OXIDE NANOSTRUCTURES FOR ELECTRONIC APPLICATIONS

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FABRICATION AND PATTERNING OF METAL AND METAL OXIDE NANOSTRUCTURES FOR ELECTRONIC APPLICATIONS

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DECLARATION

I hereby declare that this thesis is my original work and it has been written by me in its entirety.

I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Vignesh Suresh

24 July 2013

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Every man and his ideas are unique. To bring out the best within, it requires the right combination of skills, temperament, determination and untiring efforts to execute the ideas framed at the back of the mind. Just as the iron fillings get attracted towards the magnet, an exhibition of such qualities identifies the person as a good researcher who stands out from the mass receiving the attention of his peers towards him. It's the mind frame, thoughts, ideas and the distinct cliché that makes a researcher stand out.

During my career as a Ph.D research scholar, I happened to meet a number of personalities who were inspiring, supportive and played a key role towards the successful completion of my Ph.D. I would like to acknowledge all of them who contributed directly or indirectly to my research work.

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Summary

Materials reduced to the nanoscale exhibit properties different to what they exhibit on a macro scale, enabling unique applications. Increases in surface area to volume ratio, band gap changes are some characteristics that alter mechanical, thermal, optical, electronic and catalytic properties of materials. To obtain sub-100 nm and sub-50 nm material features by any of the top-down or bottom-up approach requires a meticulous study of the substrate properties (silicon or glass), material properties (metal and metal oxides), surface interactions, polymer chemistry and so on. The behavior of the materials at nanoscale and the mechanisms that drive these materials to exhibit such unique characteristics are being explored for a wide range of applications.

One of the approaches of fabricating materials on a nanoscale utilizes the concepts of self-assembly and/or block copolymer lithography (BCL) in which the molecules arrange themselves into some useful conformation through a bottom-up approach. These block copolymer (BCP) templates can then be used to direct the selective deposition of metal or metal oxides in a rich variety of geometry suitable for wide range of applications such as memory devices and sensing. Top-down patterning approaches can be equally powerful such as the nanoimprinting technique which makes use of the molds that are derived from BCL. Nanopatterning using nanoimprint lithography (NIL) is one of the most versatile nanostructure fabrication technologies to create nanoporous polymer templates with features in the sub-100 nm down to sub-50 nm regime on a silicon chip. Nanoimprinting has the ability to craft high throughput nanopatterns at great precision. Creating patterns this way has lot of

advantages over conventional fabrication methods in terms of process flexibility, process simplicity, material compatibility and cost effectiveness. Current challenges in creating patterned nanostructures are difficulty in producing large area patterns and issues with reproducibility and reliability. The power of NIL lies in the fact that it offers complete control and tunability in fabricating nanostructures of polymer templates. These nanoporous polymer templates carved using NIL are explored on a wide scale for guiding the growth of metal or metal oxide nanostructures in a variety of approaches. The immense potential of these imprinted templates could be realized when they help in engineering dimensions, feature size and periodicity of the nanostructures. This holds key to many engineering concerns that exist in electronic device fabrication such as improving the performance and longevity. It also addresses critical issues over wide area dot patterning of structures in sub-100 nm regime and provides solutions to the problem of difficulty in selective deposition at this scale.

The semiconductor industry is known for its trend setting nature. However, every time it sets a trend, it does not take much time to break it. It keeps setting and breaking a trend from time to time which is very evident when we look at the staggering transistor count on a single integrated circuit. Of late this stands at 2.3 billion following the famous Moore's law. The memory device can be a flash memory, dynamic random access memory (DRAM) or a static random access memory (SRAM). All memories have their own advantages and disadvantages in terms of power consumption, write-erase operations, longevity etc. The shortcomings are however, continuously being addressed and the device structure is expected to combine the advantages of both the write–erase speed of dynamic memories and the

retention characteristics of flash memories. There are reports on the memory devices fabricated using nanocrystals of Au, Pd, Pt and metal oxides such as TiO_2, ZnO, Fe_2O_3, Cu_2O. However, the performance of such devices built on patterned materials is less explored and is continuing to be the area of interest among researchers owing to its excellent electronic and optical properties.

The chapters in the thesis describe the utilization of the NIL derived polymer templates or block copolymer templates for selectively guiding and positioning the metal and/or metal oxide nanostructures. The resulting patterned nanostructures were utilized in nano-scale device fabrication such as flash memory devices. Structure property-feature geometry relationships are discussed in depth to elucidate the advantages of resorting to patterned surfaces.

ZnO is being widely investigated in memory applications owing to its advantageous direct band gap of 3.37 eV and a wide exciton binding energy of 60 meV. This gives ZnO, the potential to act as the right building block in memory device fabrication especially in charge trap flash memory devices. Similarly gold nanoparticles are widely explored in nanocrystal flash memory devices. Though the synthesis of ZnO and gold nanostructures on plain surfaces is well established, a number of inadequacies do exist in fabricating nanostructures in a geometrically defined pattern designs owing to the difficulties in producing high throughput patterns which is the need of the semiconductor industry. Our efforts in the work will try to address some of the key issues viz., How is the patterning achieved? How will the processing conditions differ from the non-patterning methods and their advantages? How flexible

and cost effectiveness will the operation be? What is the novelty behind nanopatterning of metal and metal oxides? How does the patterning affect the performance of the memory device? How can the protocols be extended to other applications?

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Nomenclature

ACG	Aqueous chemical growth
AFM	Atomic force microscopy
ALD	Atomic layer deposition
Au NP	Gold nanoparticle
BCP	Block copolymer
BE	Binding energy
BNSL	Binary nanoparticle super lattice
CSC	Charge storage centre
C-t	Capacitance-time
CTF	Charge trap flash
C-V	Capacitance-Voltage
d_B	Diameter of 'B' features
DI	De-ionized
DLS	Dynamic light scattering
EDS	Energy Dispersive Spectroscopy
eV	Electron volt
FESEM	Field emission scanning electron microscopy

FTIR	Fourier transform infrared spectroscopy
g_{curved}	Curved feature separation
ITRS	International technology roadmap for semiconductors
LBL	Layer-by-Layer
LED	Light emitting diode
MBE	Molecular beam epitaxy
MIS	Metal-insulator-semiconductor
MOCVD	Metal organic chemical vapour deposition
MOS	Metal-oxide-semiconductor
MSQ	Methyl silsesquioxane
NC	Nanocrystal
NIL	Nanoimprint lithography
NPT	Nanoporous templates
NVM	Non-volatile memory
PEI	Polyethylenimine
PL	Photoluminescence
PLD	Pulsed laser deposition
PMMA	Poly(methyl methacrylate)
PS-*b*-PVP	Polystyrene-block-poly(vinyl pyridine)

RF	Radio frequency
RH	Relative humidity
RIE	Reactive ion etch
RMS	Root mean square
S_A	Separation between *'A'* features
SAED	Selected area electron diffraction
SAM	Self assembled monolayer
SEM	Scanning electron microscopy
SILC	Stress induced leakage current
SONOS	Silicon-oxide-nitride-oxide-silicon
TEM	Transmission electron microscopy
TFT	Thin film transistor
Tg	Glass transition temperature
TNSL	Ternary nanoparticle super lattice
UBM	Unbalanced magnetron
UV-Vis	Ultraviolet-visible
VASE	Variable angle spectroscopic ellipsometry
V_{FB}	Flatband voltage
V_G	Gate voltage

VLS	Vapour-liquid-solid
x,*y* and *z*	Degrees of hierarchy
XPS	X-ray photoelectron spectroscopy
XRD	X-ray diffraction
ZnO NR	Zinc oxide nanorods
δ	S_A/d_B
λ	Wavelength
ω	Spin speeds in rpm

CHAPTER 1

INTRODUCTION

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Miniaturization of materials to nanoscale makes them exhibit properties different from what they exhibit on a macro scale, thereby enabling unique applications. Metal oxide nanostructures in general, and ZnO in particular, have gained a lot of significance and attention owing to their unique optoelectronic properties showing potential as basic building components in fabricating LEDs [1], memory devices [2], antireflection coatings [3] and solar cells [4], while their excellent piezo-responsive behaviour has been exploited in piezoelectric actuators [5, 6]. Moreover, nanostructures of various morphology, quality, geometry and dimensions in combination with the fabrication style have found specific applications in energy [6, 7], sensing [8], carrier charge transport in electronic cells and devices [9, 10].

Although many state-of-the-art techniques for synthesizing ZnO nanostructures with different morphologies such as metal organic chemical vapour deposition (MOCVD) [11], radio frequency (RF) sputtering [12], atomic layer deposition (ALD) [13], catalyst assisted vapour-liquid-solid deposition (VLS) [14, 15] are employed, they demand high capital investment or high temperature operations leading to high energy consumption, material wastage, contamination due to catalyst residues etc. When a level of control on high feature density over a macroscopic area, as well as the complexity of structures attainable is targeted, hydrothermal synthesis, a simple, cost effective approach is on par with what are achievable utilizing clean room tools [16, 17]. Such high density ZnO nanorods on silicon based substrates with tunable geometric characteristics are of prime interest in semiconductor compatible technologies.

However, as semiconductor electronics continues to be miniaturized, fabrication towards the sub-100 nm spatial resolution and below becomes vital necessitating the need to scale down device structures. Ability to fabricate metal oxides in the sub-100 nm regime over macroscopic areas has compelling advantages for application in silicon based technology [18]. Many of the nanofabrication and patterning techniques that are designed to further miniaturize the structures deliver excellent control over the dimensions, feature size, periodicity, uniformity, robustness and maximum area that can be patterned to set new bench marks. There are reports on the nanofabrication and patterning of ZnO based on several well established bottom-up and top-down approaches. The state-of-the-art nanopatterning techniques typically produce inorganic, metallic or polymeric patterns that can subsequently act as templates for pattern-transfer into ZnO. Template assisted ZnO nanoscale patterning has been demonstrated such as the VLS growth on patterned catalyst [19, 20, 21], seed directed hydrothermal synthesis [22, 23], e-beam lithography and AAO template assisted patterning [19, 24] and nanoimprinting [25]. As the features in the template approach the sub-100 nm mark, process design and engineering play a critical role determining the feasibility of pattern-transfer to realize nanoscale arrays of ZnO. However, in doing so, the templates created for metal oxide patterning fall short in the degree of control, process flexibility, quality, throughput and perfection attainable during pattern-transfer. In all these instances, the resulting ZnO patterns are either not robust, susceptible to pattern destruction while processing, or represent metal-metal oxide composite structures as in the case of VLS assisted patterns, with possible risks of contamination from the catalysts. These limitations restrict the integration of nanopatterned ZnO with silicon-based technology.

To combat the above nanoarray patterning and quality related issues, effective protocols to develop a well-defined, robust, mechanically stable ZnO nanoarray with sub-100 nm spatial resolution are discussed. The protocol combines the multiple advantages offered by nanoimprint lithography (NIL) such as high-throughput template patterning, low cost and compatibility with semiconductor manufacturing tools together with the high quality and robust thin film forming atomic layer deposition (ALD) technique. NIL, in turn makes use of the block copolymer lithography (BCL) assisted Si nanopillar molds, to carve nanoporous PMMA polymer templates that are used as masks [26] to cause selective deposition. In contrast to the established work on nanopatterning of metal oxides like HfO_2, TiO_2 and ZnO based on area selective ALD [13, 27, 28], our approach to produce polymer nanopatterns in the sub-100 nm scale and below offers excellent control over the dimensions, periodicity and wide area coverage. The protocol we present benefits from the combined advantages of BCL in yielding a high resolution mold that defines the template features and NIL, in terms of generating high throughput NPTs that helps in the guided growth of ZnO during deposition.

Nanopatterns of metal oxides on a macroscopic scale, with distinct features, high quality and well defined feature-to-feature interval can be achieved through area selective atomic layer deposition (ASALD) [29]. Although, ALD has been widely employed for obtaining good quality thin films over macroscopic areas, the growth can still be restricted to only designated regions on the surface by using masks or polymer templates that prevent the activated substrate surface to come in direct contact with the precursors thereby forming well isolated, discrete micro/nanopatterns making the patterning technique area selective. There are reports on the ASALD

using either a self assembled monolayer (SAM) [29, 30] or polymer templates [31] as growth-preventive masks to pattern metal oxides. But so far, use of ASALD to create robust ZnO nanopatterns with sub-100 nm spatial resolution combining the bottom-up (BCL) and top-down (NIL) approaches, compatible with the demanding silicon technology has not been established.

On the other hand, in another interesting front based on block copolymer lithography, we have developed hierarchical assemblies of metal nanoparticles for applications in metal nanocrystal flash memory devices that can be extended to micro-electro-mechanical systems (MEMS), plasmonics and sensing. Hierarchical assemblies have been repeatedly encountered in nature, and replicated in synthetic patterns and materials, as means of enhancing functionality, or imparting multi-functionality. Packing such hierarchy within a superstructure at a nanoscale, consisting of multiple material nanostructures as components, with control over their relative placements and stoichiometries have a promising impact in developing a versatile platform for different applications. Macroscopic arrays of such superstructures presenting up to third level hierarchy are achieved using self-assembly of soft, collapsible block copolymer nanospheres up to the 2nd level and directed self-assembly of metal nanospheres at the 3rd level. The fabrication combines advantages of soft-sphere self-assembly (to yield non-close packed, and stretch-at-will values for array pitch) with inherent functionality present within the soft-spheres allowing them to be transformed into a range of metal or semiconductor material nanostructures of interest, or to translate into an additional level of hierarchy. Structural investigation shows the superstructure formation to be governed by generic design rules. The hierarchically patterned gold nanoparticle arrays have proved to have significant enhancement in

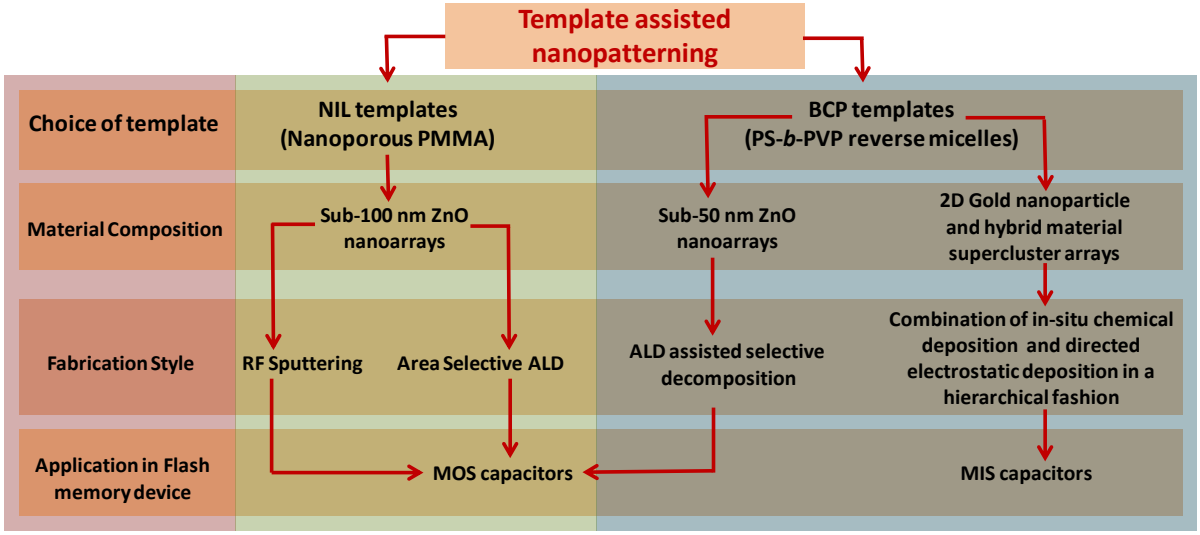
charge storage and retention in flash memory devices. The electrical characteristics of the corresponding metal-insulator-semiconductor (MIS) device structure are discussed in this thesis.

Technology development in non-volatile memories is cost driven. The ever increasing demand for lower cost per bit with higher density is the norm in the semiconductor industry [32]. Given the current market trend, majority of data flash devices are based on NAND (NOT AND) architecture and floating gate device designs. The aggressive scaling of flash memory cell is evident from the fact that the production of cell sizes of < 0.004 μm^2 per bit with 16 Gb data flash in the year 2006 was drastically scaled down to < 0.0015 μm^2 per bit with 128 Gb data flash memory in 2010 in a span of 4-5 years [32]. In this direction, the production of sub-10 nm NAND flash memory devices has been projected to hit the market in the year 2021 [33]. To meet these requirements and demands, continual efforts to shrink devices are in progress without compromising the flash memory characteristics such as high storage capacity, low operating voltages, high memory retention, and high endurance for next generation non-volatile memory devices.

The rapid scaling of flash memory device dimensions leads to several issues such as increased charge coupling between the floating gate and dielectric materials that affect the device performance [34]. Scaling down towards sub-30 nm range has further initiated the aggressive scaling of the tunneling oxide from the existing thickness of 6-7 nm to as thin as 3-4 nm [33]. However, thinning of the tunneling oxide is accompanied by issues related to charge leakage due to direct tunneling of

stored charge carriers, which would eventually result in the loss of all stored charge carriers in the continuous conventional polysilicon floating gate. While floating gate technology continues to counter its scaling limitations, some of the challenges associated with the charge storage is addressed when the floating gate is replaced by a dielectric layer containing a high density of deep traps to store charge carriers [35, 36] as in the case of silicon-oxide-nitride-oxide-silicon (SONOS) memory devices [37]. However, the classical SONOS device, with a low dielectric constant of 7.5 [38] for the Si_3N_4 also suffers from shallow trap levels affecting the retention capacity. This inarguably calls for the inevitable need for replacement of Si_3N_4 with new materials. ZnO, in this respect is a promising candidate because it possesses a rich density of discrete trap levels owing to defects in the form of oxygen vacancies and zinc interstitials making it a viable material for trapping and storing charge carriers [5]. Moreover, it combines the advantages of exhibiting a very large conduction band offset with SiO_2 or Al_2O_3 of 3.24 eV (which is comparable to 3.15 eV of polysilicon floating gate memory devices) together with the ability to demonstrate the charge storage behavior akin to conventional nitride based memory devices. Furthermore, apart from trapping and storing charges, the device structure that we have proposed is bestowed with well-isolated and discrete patterned ZnO nanoparticle arrays that help in enhancing the retention potential as well, due to reduced impact of stress-induced-leakage current (SILC) and lateral charge conduction. These ZnO arrays show high charge trap density of at a low operating voltage of 10 V, displaying its potential as a next generation memory device [39]. This charge trap density is on par with silicon nanocrystal memories, which demonstrate charge trap densities of the order of 10^{18} cm^{-3} [40].

This thesis begins with a detailed literature review followed by six parts of work discussing the results in depth. The entire focus of the thesis with respect to template assisted patterning can be captured in the flowchart below. The non-templated approach used a straight forward hydrothermal approach to produce ZnO nanorods.



Scheme 1.1 Flowchart capturing the scope of the thesis

Chapter 3 describes various state-of-the-art techniques and methodologies to obtain ZnO (metal oxide) nanopatterns in sub-100 nm and sub-50 nm regime. The ZnO nanopatterns are obtained using templated approaches where the templates are fabricated either through nanoimprint lithography or block copolymer lithography. Chapter 4 discusses in detail the fabrication of hierarchical gold nanoparticle and hybrid nanoparticle superclusters through block copolymer lithography. The morphology and the statistics about the geometry of the nanofeatures are analysed and the significance of the fabrication is particularly emphasized. Chapter 5 deals with the application of the sub-100 nm and sub-50 nm ZnO nanopatterns and the block copolymer derived hierarchically assembled gold nanoparticle clusters arrays in non-volatile flash memory devices. The capacitance-voltage and capacitance-time

characteristics to assess the performance of the MOS or MIS test capacitor devices are demonstrated. Chapter 6 discusses the fabrication of ZnO nanorods in a non-templated approach. The typical hydrothermal route of synthesizing rods demonstrates the feasibility to tune the geometry of the rods in-situ using polyelectrolytes and in obtaining quality nanorods. Various structural and optical characterizations are performed to study the in-situ size tailoring effects of the polyelectrolyte. Toward the end, Chapter 7 summarises the research work and the possible outcome of the established work and its impact in the relevant field of research and development.

The work reported by other authors that are cited in this thesis which forms an essential ingredient in any research work to come up with new and novel ideas is duly acknowledged. It has been a wonderful experience throughout my research all these years and during the preparation of the thesis that I had opportunities to learn from academics as well as in an extramural fashion. I believe, I am able to contribute significantly to the scientific community in the area of nanofabrication and patterning. It gives me immense pleasure to present my thesis here.

CHAPTER 2

LITERATURE SURVEY

2.1. Introduction

Designing and fabricating materials as per the needs of the semiconductor industry is crucial. This becomes very clear when the number of transistors packed in a single integrated circuit chip now stands at a staggering 2.3 billion following the famous Moore's law. Memory devices can be dynamic random-access memory (DRAM) or static random-access memory (SRAM) and capacitor or transistor based. All these memories [41] have their own advantages and disadvantages in terms of power consumption, write-erase operations and longevity. These shortcomings are continuously being addressed and the device structure is expected to exhibit both the write–erase speed of dynamic memories and the retention characteristics [42] of flash memories. Memory devices fabricated using nanocrystals and metal oxide semiconductors [43] fulfill some of these requirements and hence metal oxide nanostructure based memory devices attract the attention of researchers. Having said so, researchers have employed metal oxides like TiO_2 [44], ZnO [45], Fe_2O_3 [46], Cu_2O [47] for fabricating devices for photovoltaic and electronic applications. However, when it comes to fabricating a non-volatile memory based on metal oxide nanostructures, ZnO has always been unique and is continuing to be the material of interest among researchers owing to its excellent electronic and optical properties. The applications of ZnO nanostructures are numerous and a lot of minds continue to ponder over the exploitation of their unique properties to the fullest.

ZnO is being widely investigated in memory applications owing to its advantageous direct band gap of 3.37 eV and a wide exciton binding energy of 60 meV. This gives ZnO the potential to act as a right building block in memory device fabrication [48].

2.2. ZnO nanostructures – An overview

ZnO with its unique opto-electronic properties turns out to be an important semiconductor material in a variety of applications. ZnO has several advantages over other semiconductor nanostructures involved in device fabrication and the most important are its larger exciton binding energy, its ability to grow into a single crystal and exhibition of quantum confinement effects that helps in tailoring the band gap.

Over the last few decades tremendous improvements have taken place in ZnO related research, largely because of the possibilities to look out for improved types of electronic and photonic devices [10, 49, 50]. ZnO based memory devices share the same basic structural features of the conventional silicon or polysilicon based devices [51, 52]. In ZnO based devices, the oxygen defect levels and the zinc interstitials control the charge transportation which can in turn be controlled using dopants. They act as the charge traps giving rise to the memory effect in the fabricated devices. However, certain aspects of the growth of ZnO are still unclear owing to the lack of information about the complete mechanism and the effects of impurities and defects in ZnO nanostructures. It is this defect level in ZnO that determines most of the optical and electronic properties of the material. By exploiting the defect levels, multiple dimensionalities in terms of novel and improved properties could be imparted to the latest electronic devices. Analysis of the role played by the impurities, dopants and defects in ZnO which play a significant role is important in fabricating devices. Most of the ZnO structures synthesized with the available methods yield samples deficient in oxygen and rich in zinc. The oxygen defects [53] and the zinc interstitials [54] are the most important factors and though there are evidences in

literature based on photoluminescence data [55] and density functional theory [56, 57] suggesting that defects play an important role, satisfactory explanations for charge transport and storage are still lacking.

There are a number of techniques available to create ZnO structures such as thin films, nanorods, nanowires and nanodiscs. Selection of the right fabricating technique, deposition methods, processing of dielectric materials and source-drain materials are the key factors in establishing a competent ZnO based non-volatile memory device. ZnO based nanostructures have been fabricated using a variety of deposition methods that include radio frequency (RF) sputtering [58], pulsed-laser deposition (PLD) [59] and spin coating [60] of zinc oxide dispersion. Of these methods, RF sputtering from a ceramic ZnO target has been the leading choice largely because of convenience and ease in the process control.

2.3. Synthesis of ZnO nanostructures

2.3.1. Hydrothermal synthesis of ZnO nanorods/nanowires

The most energy efficient and cost efficient strategy to obtain nanorods and nanowires among a number of ZnO nanostructure synthesis techniques is the hydrothermal growth process. It does not demand high temperatures and vacuum environment. The hydrothermal synthesis of ZnO nanorods reported by L. Vayssieres *et al* [60, 61, 62] involves the epitaxial growth of ZnO rods on the seeded substrates from equimolar aqueous solution of zinc nitrate or zinc acetate and hexamine as precursors. The synthesis technique relies on the anisotropy exhibited by the crystal structure of ZnO

which resembles the hexagonal Wurtzite form. The different facets of the ZnO nanorods have different polarity, O^- being the negative basal plane and Zn^+ being the positive top surface. The lateral facets are non-polar in nature and are generally lower in energy. Since, the technique is substrate independent, a pre-coated seed placed on the substrate provides the nucleation sites [63] for further growth of the crystal. Nucleation sites are created by depositing a layer of ZnO particles by sputtering, spin coating a layer of colloidal ZnO nanoparticles, deposition from vapour phase etc. This causes the epitaxial growth of the nanorods or nanowires from the seeds and the rods obtained will be highly oriented whose aspect ratio could be tailored by varying the process conditions such as temperature, concentration of precursors, and growth time. This gives handle to exert control over the growth rate and the morphology of the resulting nanorods or nanowires. It has been shown that the aqueous chemical growth [64] carried out with a buffer ZnO layer beneath will result in the crystal formation along the (0 0 2) direction or c-axis.

A probable mechanism to explain the growth through this technique is as follows,

$$(CH_2)_6N_4 + 6H_2O \rightarrow 6HCHO + 4NH_3$$

$$NH_3 + H_2O \leftrightarrow NH_4^+ + OH^-$$

$$Zn^{2+} + 2OH^- \rightarrow Zn(OH)_2\downarrow$$

$$Zn(OH)_2 \rightarrow ZnO\downarrow + H_2O$$

Later when the technique became popular many researchers brought in their own modifications to the methodology followed in the conventional hydrothermal process. One such modification is the introduction of polyelectrolytes namely, polyethylenimine in the growth solution. The polyelectrolytes act as surfactants and

cause the growth of the ZnO nanorods in a controlled fashion. This helps in getting the ZnO nanorods of the required dimensions and aspect ratios. Ying Zhou *et al* reported the modifications [65] they performed to the hydrothermal methodology with the introduction of polyethylenimine. Possible mechanisms on how PEI or other surfactants [66] control the dimensions of the rods are established and provide methods to craft nanorods to cater to the needs in device fabrication.

2.3.2. Vapour Liquid Solid (VLS) growth

Metal-catalyst-assisted chemical vapor transportation to grow ZnO nanorods has always been a popular technique as they yield nanorods that are highly vertical and are of good quality. The VLS [67, 68] mechanism is known for several decades and it has been widely used to explain the nanostructures formation upon metal-catalyst-assisted thermal chemical vapor transport. However, certain experimental evidences are lacking to completely establish the mechanism of growth using the metal catalyst. Many have proposed that both vapour-solid (VS) mechanism [14] as well as vapour-liquid-solid (VLS) contribute to the growth assisted by the catalysts. But a satisfactory explanation is yet to be registered. Consequently, there are some issues in the existing mechanisms that describe ZnO nanowires growth through VLS regarding the i) composition of the alloy droplet, ii) position of the catalyst after growth etc. In a typical VLS as proved by Yao *et al* [69] and Kong *et al* [70], vapor species are first generated by thermal evaporation. The reactant species undergo chemical reduction and the products are then subsequently transported and getting condensed onto the surface of a solid substrate where the metal catalyst aids in the selective deposition.

By exercising proper control over the degree of super saturation and temperature one can obtain one-dimensional nanostructure over large area using this approach.

2.3.3. Thermal evaporation

The thermal evaporation [69] method is a relatively simple methodology wherein Zn metal is melted and its vapors are condensed on the substrate surface. The zinc metal films are then annealed in oxygen atmosphere to convert the metal into a metal oxide buffer layer which will now acts as the nucleation sites for further growth of ZnO nanorods. Its detailed mechanisms involve the vapour transportation followed by vapour condensation. Fouad *et al* [71] reported the evaporation of zinc to form zinc oxide thin films for applications in photocatalysis.

2.3.4. Sputtering of ZnO

Sputtering of ZnO is another popular method achieved by RF sputtering [58] to produce thin metal oxide films. The method is highly flexible when it comes to process conditions. The deposition is usually carried out in vacuum with argon as the sputtering enhancing gas with or without oxygen. When used, oxygen will be the reactive gas. ZnO can also be grown by DC sputtering from a Zn target in an argon-oxygen gas mixture. The RF power applied to the plasma, the sputtering time, oxygen content help in tuning the sputtering conditions to obtain good quality ZnO films. The target is pre-sputtered for at least 2-5 min before the actual deposition begins to remove any contamination on the target surface and to bring the system to a stable state. For devices [12] and piezoelectric studies, ZnO films have been deposited on Si

substrates. Cross *et al* reported the effects on photoluminescent properties [72] of nanorods grown on ZnO sputtered films. During ZnO thin films deposition on Si (100) by RF sputtering, upon increasing the argon-oxygen ratio, the visible emission in the room temperature PL spectra was drastically quenched without sacrificing the UV band-edge emission intensity. This tendency is attributed to the reduction of the oxygen vacancies and zinc interstitials in the film. The visible emission in ZnO originates possibly from oxygen vacancy or zinc interstitial related defects. So, by tailoring the ZnO thin films in a proper way by adjusting the deposition environment, ZnO nanostructures for application in CTF memory devices as charge storage centers could be realized.

2.3.5. Atomic layer deposition of ZnO

Atomic layer deposition is a highly controlled thin-film deposition technique to build layers with sub nm precision. It is unique owing to the fact the film grows through self-limiting surface reactions [73] unlike other physical or chemical vapour deposition techniques. It has been the state-of-the-art technique for obtaining high quality thin films of insulators, semiconductors, and metals for various optoelectronic applications [74, 75, 76]. Since the deposition is carried out on the basis of self-limiting surface reactions, the technique ensures precise control over film thickness, homogeneity, crystallinity and good uniformity over large areas. However, the fact that ALD is sensitive to surfaces has been exploited in using the technique to produce area selective patterns of the deposited material. Area selective atomic layer depositions of metal oxides such as ZnO, TiO_2 and metals such as Pt, Ni have been reported [13, 27, 75, 76, 77]. Area selective deposition requires the use of templates

that act as mask for the film growth while the deposition continues to takes place in the unmasked areas of the substrate. This way, patterns of materials are produced in a highly controlled fashion over large areas. The templates that are generally used are fabricated either through e-beam lithography, nanoimprint lithography, block copolymer lithography or SAM of silanes [29, 78, 79].

All such characteristics of ALD to produce highly controlled material patterns show promise towards adapting the technique in semiconductor industry. Moreover, in ASALD, each deposition cycle consisting of i) exposure to a precursors, ii) a purge period, iii) water pulse and iv) purge period determines the thickness of the film and so process variables such the number of cycles, precursor dosage, pulse duration etc can effectively be manipulated to achieve the desired patterning.

2.4. Gold nanoparticles in nanofabrication

2.4.1. Synthesis of gold nanoparticles

The synthesis of metal colloidal solution [80, 81, 82] has been studied for over a century and the most established methods involve the aqueous reduction of metal salts such as gold (III) citrate in the presence of citrate anions. The colloids are electrostatically stabilized by the adsorption of citrate ions to the gold nanocrystals' surfaces during growth. The nanoparticles can also be functionalized with other reactive end groups depending on the surface modification required. It can be citrate stabilized, amine stabilized or even thiol capped [83]. The colloidal solution is monodisperse with the particle sizes tunable between 8-15 nm. Schmid *et al*, provides an overview of the advances in metal colloid synthesis [84].

2.4.2. Gold nanoparticles based charge trap flash (CTF) memory devices

Nanoparticles owing to their small size and high surface to volume ratio have always attracted scientists to employ them in a number of applications. They are regularly used as charge storage centers in non-volatile devices [85, 86]. Gold nanoparticles owing to its suitable work function are used in fabricating devices such as flash memories [87] and bistable switching devices [43, 88]. Hybrid organic-inorganic systems [85] are being investigated, where metal nanoparticles are sandwiched between organic polymers for memory device applications. Recent trend aims in decorating the walls of the semiconductor materials to increase the density and hence the device performance.

2.5. Patterning of surfaces

The demand for producing sub-100 nm and sub-50 nm feature patterns is increasing in the field of optics, photonics, sensors and electronics. The ability to position the nanostructure (metal oxide or metal nano-sized particles) in the required geometry is of highest interest for the possible integration of these building blocks into devices. It's been demonstrated in the self assembly of gold nanoparticles [89] into thin films and how these films can be used as a platform for the layer-by-layer assembly of nanoparticles. Methods for patterning on nanoscale based on self-assembly approaches offer the advantage of macroscopic patterning with good uniformity without the need to rely on complex and expensive instruments. One such method to create high resolution patterns is self-assembly based block copolymer lithography [90, 91].

One can also think of using molds to create patterns based on nanoimprint lithography (NIL) [92, 93] – a top down patterning technique. Work from many research groups has shown that Si and SiO_2 have sufficient hardness and durability properties for nanoimprint applications and hence Si nanopillars could be used as potential molds. NIL molds having features in the sub-100 nm regime derived out of BCL has been reported earlier [94]. The high density protrusion Si molds can then be used in patterning the substrates using photoresists. The Si pillars on the molds produce its impressions on the photoresists during imprinting at high temperature and pressure. At the end of the process, when the flow of the polymer photoresist is arrested by cooling down to room temperature, the impressions are preserved.

It has been reported earlier on how Si nanopillars (molds) can be produced using nanospheres and nanoparticles as etch masks. Recently, Krishnamoorthy *et al* [94] reported on how the two-dimensional (2D) arrays of quasi-hexagonally ordered arrays of polystyrene-*block*-poly(2-vinylpyridine) (PS-*b*-P2VP) be used in creating Si nanopillars.

2.5.1. Nanoimprint Lithography

Nanoimprint lithography (NIL) is a powerful lithographic technique for high-throughput patterning of polymer nanostructures at great precision and at low costs. The technique of nanoimprinting was first proposed in the year 1995 by Chou *et al* [95, 96]. From then on, it has emerged as one of the most promising technologies for high-throughput nanoscale patterning.

NIL relies on direct mechanical deformation of the photoresist material as it reflects an exact replication of the surface features of molds. The polymer that is imprinted need to flow under an applied pressure and temperature and at the same time should have good mold-releasing properties to maintain their structural integrity during the de-molding process. This is described in detail in a review on NIL [97].

As a standard practice, the temperature chosen for NIL is generally more than the glass transition temperature of the material that is imprinted, so that the polymer can freely flow. Once the imprinting is done, the imprinted polymer needs to be cooled down to below its T_g so as to preserve the imprinted pattern after the mold is removed. Because of its numerous advantageous features and its potential for sub-50 nm lithography, NIL is widely regarded as one pioneering technology in nanopatterning.

2.5.2. Directed self assembly

Self-assembled monolayers (SAM) have long been serving as the means of chemically modifying surfaces for a variety of applications including surface patterning, sensing, layer-by-layer assembly [98]. Silane chemistry [99, 100] is a well established concept wherein the formation of monolayers on silicon surfaces takes place through covalent binding of silane molecules. The silanized surfaces are then used in binding functionalized nanoparticles and other molecules to the surfaces. Although quite interesting, this approach does not provide the advantage of achieving

patterns of nanoparticles over large areas of surface as does the deposition of homogenous colloidal monolayers of block copolymer micelles.

A block copolymer is composed of blocks repeating monomer units and can either be diblock copolymer or multiblock copolymers. The morphology of the features upon thin film formation can be spheres or cylinders, gyroid or lamellae, forming patterns of excellent uniformity over large areas. In PS-*b*-PVP diblock copolymer system, the two blocks are mutually incompatible with each other and hence when these block copolymers are cast on the substrate from a solvent that is selective to only one of the blocks, they phase separate, governed by the Flory-Huggins interaction parameter and produce well controlled micelle structures. Amphiphilic block copolymers such as PS-*b*-PVP, where one block (PVP) is hydrophilic and another (PS) is hydrophobic, when dissolved in selective solvents (*m*-xylene) instantaneously produce micellar structures due to micro phase separation where insoluble PVP forms the core and soluble PS forms the corona. In block copolymer lithography of PS-*b*-PVP micelles, the structure and orientation of the BCP micelles depend on the thickness of the block copolymer film spin coated from solvent and is influenced by spin speeds, solvent, and concentration.

The creation of high-density nanopatterns in the sub-50 nm regime and below is highly feasible based on block copolymer lithography. These BCP in turn act as templates for a controlled assembly of nanocrystal arrays. The resulting patterns of metal nanocrystals can then be exploited in flash memory devices as charge storage centers. The synthesis of metallic nanostructures and the control of their spatial

arrangement at the nanoscale by means of block copolymer (BCP) self-assembly have proved to be very attractive and powerful alternative [101, 102, 103, 104] to other techniques.

2.6. Flash memory devices

The possibility to form regular arrays of metallic nanostructures on semiconductor surfaces opens a large spectrum of applications in electronics. Majumdar *et al* [105] fabricated data-storage devices based on layer-by-layer self-assembled films of a phthalocyanine derivative. Recently, Leong *et al* [85, 106] fabricated memory devices using gold nanoparticles synthesized within a block copolymer (polystyrene-block-poly (4-vinylpyridine) over a pentacene layer. The devices demonstrated charge storage because of charge exchange between the nanoparticles and pentacene. The block copolymer acted as the dielectric material and the nanoparticles served as floating gate charge storage centers. However, metal oxide and metal based flash memory devices exhibit different mechanisms of storing charges and are discussed below.

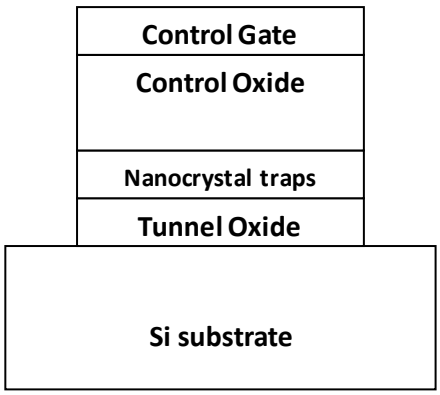
2.6.1. Metal oxide (ZnO) semiconductor based memory devices

ZnO-based nanostructures find a lot of applications in light emitting diodes (LEDs) [50, 107], gas, chemical and biological sensors [108], optoelectronic devices, and switching devices [47–50]. Recently more efforts are put in fabricating electronic devices and in particular ZnO nanowire Schottky diodes [109, 110], ZnO nanowire MOSFET [64], photo detectors and non-volatile memories [111, 112]. Epitaxial ZnO

also holds much promise as a semi-conducting transparent thin film, which again will be important for solar cells, gas sensors, displays and wavelength selective applications. The ability of ZnO dielectric for charge storage can be understood by studying the electrical characterizations of the metal–oxide–semiconductor (MOS) structure. By observing the hysteresis behavior during the capacitance-voltage (C-V) measurements, the charge storage capabilities of the device could be understood. From the outset, ZnO thin film transistors share many of the basic structural and process-related features of the well established Si and poly-Si transistors [52]. Using such structures, various aspects of device fabrication including deposition and processing, material selection, compatibility have been explored which gives the comprehensive set of results providing an aura around the fabrication of ZnO non-volatile memories. ZnO TFTs [113] have been fabricated using a variety of deposition methods that include RF sputtering [58], thermal evaporation [69], pulsed-laser deposition (PLD) [114], spin coating of ZnO nanoparticles and a variety of other solution based approaches. All such techniques are being explored for the convenience in the device fabrication and data retention abilities. Recently, in 2008, Cross *et al* [48] described the material properties and device characteristics of hybrid inorganic/organic memory devices produced using ZnO nanorods (ZnO NRs) in combination with the organic polymers polyvinyl acetate (PVAc) and polystyrene (PS).

2.6.2. Nanocrystal (Au NP) based flash memory devices – Performance

The ability of the nanocrystals to store charges is the basis behind the nanocrystal memories. Metal nanoparticle based flash memory devices [115] have the added advantage of controlling trap density, work function and the charge distribution in the memory devices. The nanocrystals can be Au, Pt, Pd or Ag. For commercialization, these devices can be integrated into large patterned arrays that would enhance the performance. The first step in the fabrication of such devices will be the deposition of thin film of nanocrystals on the silicon surface with thermally grown oxide. This thin film of nanocrystals is then covered by a thick control oxide. The schematic of a typical capacitor based flash memory device is shown in scheme.2.1.



Scheme 2.1 Schematic diagram of a typical nanocrystal memory device

In what is called the "write cycle", when a positive voltage (forward biased) is applied, electrons tunnel from the channel inversion layer to the nanocrystal via tunnel oxide layer. Under this condition, the surface of a p-type substrate becomes less accumulated with electrons creating an inversion region due to the effective injection of electrons in the nanocrystals. This reduces the conduction in the inversion

layer and hence the gate capacitance increases. The movement of the carriers through the oxide shall be because of Fowler-Nordheim (F-N) tunneling or channel hot electron injection. To bring the device back to normal state, a negative voltage is applied during erasure when the electrons tunnel back from the nanocrystals to the silicon substrate. As a result, the channel becomes more accumulated with electrons. This in turn increases the conduction in the accumulation layer and hence the gate capacitance decreases. In this way, the charge is stored and discharged in a program/erase cycle.

Recently, the production of ordered arrays of nanoparticles to be used as the charge storage centers was reported by Boontongkong *et al* [116] and Hinderling *et al* [117]. In 2007, Chai *et al* [118] reported on the assembly of aligned linear metallic patterns on silicon. In the same year, Shahrjerdi *et al* [119] reported on the fabrication of Ni nanocrystal flash memories using a polymeric self-assembly approach.

2.6.3. Nanocrystals based flash memory devices – Varieties

Nanocrystal memory devices offer the advantages of improved retention, low power consumption and fast program/erase operation [120]. The first Si nanocrystal memory device with silicon oxide barrier was demonstrated by Tiwari *et al* [121]. However, the silicon nanocrystal based memory devices suffered problems related to the leakages of charges through the weak tunnel oxide layers. This affected the charge retention capabilities of the devices fabricated [42]. SiO_2 possesses a low k-dielectric and had to be replaced with other dielectric materials that could solve the problem of charge leakages. As a next step, many research groups made significant efforts in

testing their devices with other dielectric materials such as HfO_2 and Al_2O_3 to enhance the device performance [122, 123]. Efforts were then taken to replace the Si nanocrystals with other semiconductor nanocrystals such as Ge and SiGe [124]. The charge storage capabilities of these nanocrystals were analyzed and they proved to be better candidates than the conventional Si nanocrystals. They even had better data retention capabilities due to their relatively small band gap compared to Si. In Ge nanocrystal based devices, the bandgap of Ge is small and hence the tunneling of the electrons while writing becomes easier and the electrons could be easily injected into these semiconductor nanocrystals.

The next generation of nanocrystal based memories is based on the metal nanocrystals such as Au, Pd or Pt owing to the advantages they offer in engineering their work functions for enhanced data storage capabilities. Any memory device has its own advantages and disadvantages. Metal nanocrystal memories definitely excel the conventional memory devices in a number of ways. However, metal nanocrystal memories do suffer from several other issues, including degraded retention characteristics due to contamination problem. Dielectric nanocrystals, on the other hand, are less favourable due to difficulties in controlling the defect-related traps of the dielectric material.

To benefit from the metal nanocrystal devices [86] the first and foremost step is to find the right fabrication technique that would give a handle to control the size, uniformity, density and distribution. New approaches are being tried out in increasing the density of the nanocrystals such as the layer-by-layer assembly. It has been recently demonstrated by Leong *et al* [106] that a polymeric memory device can be

fabricated based on the in situ synthesis of gold nanoparticles in a self-assembled block copolymer. Currently, many research groups work on the density control of the nanocrystals so as to enhance the device performance while it still continues to be a difficult task on a macroscopic scale. The other factors to be considered on the fabrication process include the capacitance-voltage characteristics to ensure high charge storage behavior [125]. Furthermore, much work is needed to understand the underlying mechanisms responsible for charge trapping and size-dependent properties of nanocrystal memory devices. The contribution of minority charge carriers, the majority charge carriers, nature of substrate, density of defect levels, dopant content, dielectric characteristics and charging behaviour need to be determined to effectively fabricate a memory device to be on par with the current trend associated with the nanocrystal memory devices.

2.7. Summary

The issues associated with the early nanocrystal based memory devices and the metal oxide based devices can be resolved by resorting to the patterned approaches of depositing the nanoparticles and nanostructures. The patterning provides an easy way to have complete control over size, morphology, density, spacing which is very advantageous than the randomly distributed nanoparticle layers. The mechanism behind forming such structures could be well analyzed and interpreted as there is a complete control in every step of fabrication. Various inadequacies of current data storage technologies on non-patterned substrates could be overcome by the templated metal nanocrystal and metal oxide nanostructured materials. There exists an area of research that needs further exploration wherein array of nanorods or nanodots could

be studied in depth for fabricating the memory devices using patterned approaches. Both the top down patterning approach (based on NIL) and the bottom up patterning approach (based on BCL) can be exploited in precisely positioning nanostructures or nanoparticles for fabricating multi functional 2D nanostructures. The drawbacks that exist in the current device fabricating approaches such as charge leakage, inefficiency in trapping charges could be well addressed.

CHAPTER 3

FABRICATION OF ZINC OXIDE NANOARRAYS USING LITHOGRAPHICALLY DEFINED TEMPLATES

Introduction

ZnO nanostructures are known to have proven technological value for applications such as UV photodetectors [126], piezoelectric devices [19, 127], LEDs [1], gas sensors [8], memory [128] and semiconductor devices [10]. Fabrication of ZnO nanopatterns presenting controlled feature sizes, spacing, dimensionality, feature alignment and unit cell orientations, with spatial resolutions below 100 nm using low-cost and high-throughput approaches are among goals that are widely sought after. Patterned growth of ZnO using templates obtained by techniques such as nanosphere lithography [129], AAO [19, 24], shadow mask [19, 130] or NIL [131, 132] provide an effective solution in this direction. Typically, these approaches have made use of patterned seed layers to guide hydrothermal [22, 23] or VLS growth [19, 20, 129], template-guided MOCVD [133] or electrodeposition of zinc [134], and direct patterning of sol-gel precursors [131]. Preparation of well-defined ZnO nanoarrays by lithography with sub-100 nm spatial resolutions and below that combine multiple advantages of low-cost, high-throughput fabrication and compatibility with semiconductor manufacturing tools have not been demonstrated before. In this direction, in Sections 3.2 and 3.3, we report a generic process design based on diblock copolymer assisted nanoimprint lithography (NIL) as means of generating uniform nano disc arrays of ZnO. The approach draws its benefits from the use of NIL, which is a high-throughput and repeatable tool, and from the use of block copolymer self-assembly, which provides for low-cost production of high-resolution NIL molds. The processing can be performed at low temperatures, thereby making it suitable for flexible substrates for low-cost printed electronics applications. We further investigate

the charge storage capability by the ZnO nano discs, and study their performance as charge storage centers for potential application in nanocrystal flash memory devices.

ZnO nanopatterns of even higher resolutions can be potentially achieved by increasing resolution of NIL molds using block copolymer templates with high spatial resolutions. The feasibility towards this ideal is supported by earlier literature evidence on realizing patterns with feature and spatial resolutions down to sub-10 nm in separate instances using NIL [135] and block copolymer self-assembly [136] respectively. However, the use of amphiphilic diblock copolymer reverse micelle arrays itself as templates is proposed as a conceptually simpler alternative that allows overcoming the limitations of NIL such as the ability to tune the density and other geometric attributes of the features. Moreover, the number of process steps to create a NIL mold derived from block copolymer lithography is not needed when the BCP polymeric template itself can be used directly to achieve the required patterns, thereby saving time and money. This will be discussed in Section 3.4. In either case, ability to create high-resolution patterns of ZnO, and their usefulness for application in flash memory devices has been demonstrated.

SECTION 3.1

FABRICATION OF NANOPOROUS TEMPLATES THROUGH NANOIMPRINT LITHOGRAPHY

3.1.1. Introduction

Nanoimprint lithography is one of the pioneering techniques to produce nanofeatures of polymers. Often, the polymers that are imprinted happen to be photoresists for application in electronics. This apart, NIL can also be helpful in patterning polymers that can be used as masks for pattern transfer to other materials of choice. This section deals with the imprinting of poly (methyl methacrylate) (PMMA) to be used as templates for guiding selective deposition of ZnO. The significance of using the NIL assisted templates for nanopatterning lies in their universal application; as long as the nanoporous PMMA can act as a suitable mask to selectively guide the deposition, any metal oxide can be patterned. The high-resolution NIL molds preparation starts with the deposition of spherical reverse micelles of PS-*b*-PVP from *m*-xylene by spin coating. These arrays can be obtained on a macroscopic wafer scale, with little variations (standard deviations < 10%) in the different geometric attributes such as feature width, periodicity and heights. The micellar arrangement is used as masks for pattern-transfer into the underlying Si substrate by dry plasma etch processes to produce Si nanopillars that are used as molds during imprinting. This hard mold containing the nanoscale surface features is pressed into a PMMA polymeric material cast on a substrate at a controlled temperature and pressure. This produces the replication of the mold features on the polymeric material which retains the features when cooled below the T_g of the photoresist material.

3.1.2. Experimental

3.1.2.1. Materials

Poly (methyl methacrylate) of molecular weight 75,000 g $gmol^{-1}$ was purchased from Microresist Technologies (Berlin, Germany) and used without further purification. Acetone and 2-propanol were obtained as anhydrous solvents with purity > 99 % from Sigma-Aldrich Pte Ltd. Prime grade p-type silicon wafers were obtained from Silicon Valley Microelectronics (Santa Clara, CA, USA). Point Probe Plus silicon tips for tapping mode imaging measurements with atomic force microscopy were purchased from Nanosensors (Neuchatel, Switzerland).

3.1.2.2. Methods

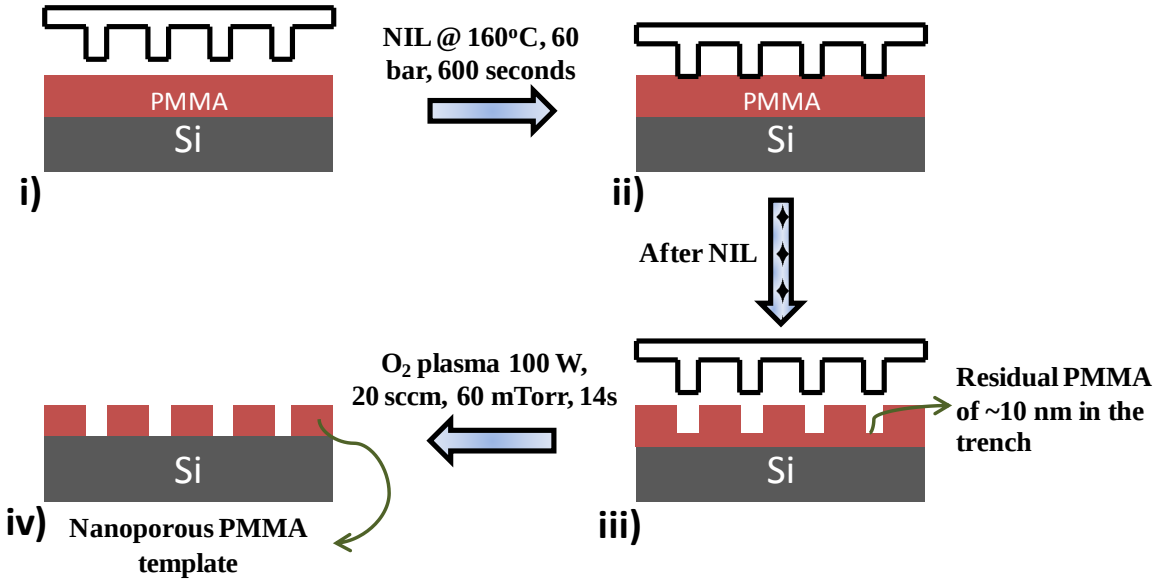
The silicon substrates were cleaned by ultrasonicating in acetone followed by 2-propanol and finally treated with UV/Ozone (SAMCO UV-1, SAMCO Inc., Kyoto, Japan) for 10 min. The thickness of the oxide layer was measured using ellipsometer (Wvase 32, J.A.Woollam.Co., Inc., Lincoln, USA). The molds used were prepared using procedure described elsewhere [137]. Briefly, 0.5 % (w/w) of the solution of the polystyrene-*block*-poly(2-vinylpyridine) 114 kDa, f_{PS}~0.5, with PDI of 1.1 were deposited from *m*-xylene solution by spin coating at 5000 rpm on to Si substrates with 25 nm of thermally grown oxide layer. Pattern transfer was performed by dry etching using C_4F_8/CH_4 using AMS 200 DSE, an inductively coupled plasma (ICP) etcher (Alcatel Micromachining Systems, Annecy, France). Subsequently, the SiO_2 patterns were transferred into Si by dry Cl_2 plasma etching using STS etcher (Surface Technology Systems, New Port, UK). The pattern characteristics, viz. the mean

heights, width, centre to centre spacing of reverse micelle arrays, nanoporous templates obtained upon NIL, and the ZnO nanoparticle arrays were characterized using tapping mode AFM (Nanoscope IV Multimode AFM, Veeco Instruments Inc., NY, USA) and SEM (FESEM 6700F, JEOL, Tokyo, Japan). PMMA-75k was spun at 3000 rpm for 45 seconds to obtain 100 nm thick film using CEE model 100CB spinner (Brewer Science Inc., MO, USA). Imprinting was carried out at 160^{o}C, at 60 bar pressure for 600 seconds using Obducat 4" imprinter (Obducat, Sweden). The residual polymer layer removal after imprinting was carried out using oxygen plasma in a reactive ion etcher (Oxford plasmlab100, Oxford Instruments, UK) at 60 mTorr, 100 W, 20 sccm O_2 for 14 minutes to yield nanoporous templates (NPTs).

3.1.3. Fabrication of nanoporous polymer template

The Si nanopillar molds for NIL were derived by exploiting self-assembled reverse micelle arrays of polystyrene-*block*-poly(2-vinylpyridine) on Si surface as shown earlier [138]. The ordered arrays served as etch masks for pattern transfer by reactive ion etching. The optimization of the self-assembly of amphiphilic copolymers to attain reverse micelle patterns with well-defined feature sizes and separations has been described in detail elsewhere [137]. A solution of polystyrene-block-poly (2-vinylpyridine) 114 kDa, f_{PS}~0.5 in *m*-xylene is coated on Si substrate with 25 nm thermally grown oxide layer. The reverse micelles self-assemble to produce two dimensional hexagonal networks of nanoscale polymeric features. These features can subsequently be transferred to the underlying substrate by dry etching processes (*cf* Experimental Information). The low etch contrast offered by the polymeric features is countered by a first transfer into the thermal oxide layer, followed by a second

transfer into Si to achieve Si nanopillar molds. This facilitates the formation of NIL molds with Si pillar height of ~100 nm and a diameter of 60-70 nm. The nanopillar arrays were treated with 1H,1H,2H,2H- perfluorododecyl trichlorosilane using a self assembled monolayer (SAM) coater in vapor phase to render the Si nanopillar arrays stiction-free and suitable for NIL. The complete flow of the NIL process is provided in the scheme 3.1.1 below to produce the nanoporous templates.



Scheme 3.1.1 Illustration of the imprinting process to fabricate the PMMA nanoporous template.

The imprinting on PMMA was carried out at a temperature of 160^0C, pressure of 60 bar for 10 min (step (ii) of scheme 3.1.1). The imprinted PMMA films revealed pore features of width and centre to centre spacing that mirrored the nanopillar arrays, as expected (Figure 3.1.1 (b)). A ~10 nm thick residual layer of PMMA was retained beneath the pores at the end of NIL process, which was removed by subjecting the nanoporous template to anisotropic reactive ion-etching (RIE) using O_2 plasma (60 mTorr, 100 W, 14 s). The RIE process was optimized such that the residual layer was

fully removed and the substrate underneath the template was exposed through the pores [138]. The resulting templates exhibited pore width of ~60 nm and depth of ~90-100 nm. There was some loss of aspect ratio of the pore features observed due to the O_2 plasma RIE, presumably due to a lower etch rate of polymer within the pores.

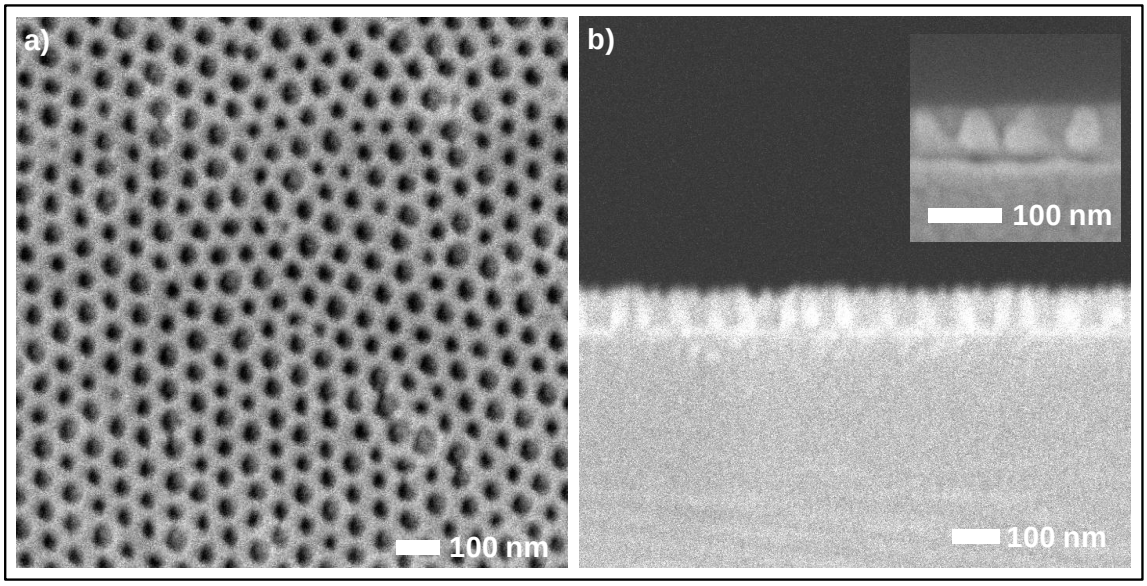


Figure 3.1.1 FESEM images showing the (a) top view and (b) cross section image of the nanoporous template. Inset: Higher magnification of (b).

The process of removing the residual layer required meticulous optimization since an underexposure retained the polymer in the trenches while an overexposure destroyed the hexagonal network pattern as shown in Figure 3.1.2 (c). The optimized plasma exposure was found to be 14 s that removed the residual layer and at the same time preserved the pattern integrity. This also resulted in generating patterns over large areas with very narrow variation in the geometry of the features of the NPTs as shown in Figure 3.1.2 (d).

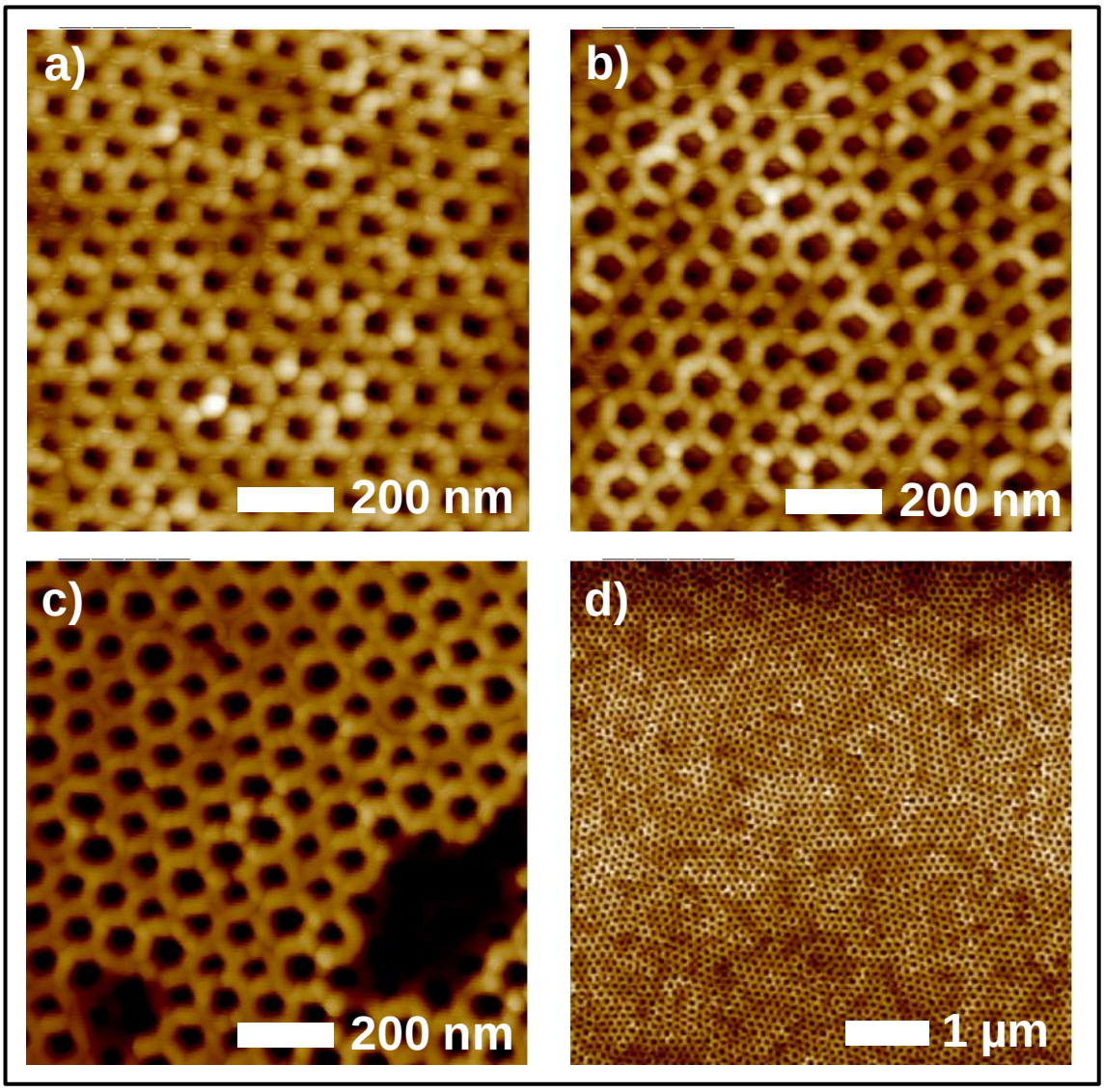


Figure 3.1.2 Tapping mode AFM images of the nanoporous templates when exposed to oxygen plasma for different time interval to determine the optimized condition for removal of residual polymer. (a) 10 s, (b) 14 s (optimal condition), (c) 18 s and (d) macroscopic image of (b).

3.1.4. Conclusions

The nanoporous polymer templates fabricated through nanoimprint lithography can thus be conveniently used as masks for material deposition. Moreover, the imprinted PMMA templates replicate the geometric attributes of the Si nanopillar molds craved out of block copolymer lithography and hence tunability can be achieved by

optimizing the self assembly process. Any further tunability of the imprinted features can be achieved during oxygen plasma exposure when a slightly long duration (avoiding overexposure) will end up in the widening of the pores preserving the hexagonal network. However, it compromises on the template height. As long as the resulting material patterns do not require high aspect ratios such as nanodiscs or nanodots, the morphology of the NPTs can be tuned accordingly. The utility of the templates to guide the fabrication of ZnO nanopatterns are discussed in Sections 3.2 and 3.3.

SECTION 3.2

PATTERNING OF NANODISC ARRAYS OF ZINC OXIDE THROUGH TOP-DOWN APPROACH

3.2.1. Introduction

Production of low aspect ratio features of metal oxides such as ZnO, TiO_2 is very much in need for applications in electronics and optics. Creating an array of ZnO nanodiscs on a macroscopic scale can be highly significant and can differ from the conventional style of producing ZnO nanofeatures, since the processing of patterning has its own advantages. Formation of nano disc arrays of ZnO with high densities (~22 Gbit/inch^2) with narrow distributions in size, shape and periodicities (< 15%) using a combination of block copolymer self-assembly and NIL is discussed in this section. ZnO nanodisc arrays with sub-100 nm spatial resolutions, using high-throughput and manufacturing compatible approaches are realized. The fabrication combines benefits from the use of NIL, which is a high-throughput and repeatable tool and from the use of block copolymer self-assembly which provides low-cost production of high-resolution NIL molds. The fabrication protocol, its novelty and significance are discussed in detail.

The electronic characteristics of the fabricated nanofeatures in capacitor configuration are discussed in detail in Section 5.1. In short, preliminary results from the investigation of memory performance show flat-band voltage shift of 2.53 V at a relatively low operating voltage of 10 V. A high charge trap density of 2.3×10^{18} cm^{-3} combined with excellent retention of ~80% after 1000 s of discharging is observed with low tunnelling oxide thickness of 3 nm, demonstrate significant promise of the ZnO nano discs to act as charge storage centres in non-volatile flash memory devices.

3.2.2. Experimental

3.2.2.1. Materials

Poly (methyl methacrylate) of molecular weight 75,000 g mol^{-1} was purchased from Microresist Technologies (Berlin, Germany) and used without further purification. Acetone and 2-propanol were obtained as anhydrous solvents with purity > 99 % from Sigma-Aldrich Pte Ltd. Prime grade p-type silicon wafers were obtained from Silicon Valley Microelectronics (Santa Clara, CA, USA). The p-type silicon wafers with thermally grown oxide (3 nm thickness) were obtained from GlobalFoundries Singapore Pte Ltd, Singapore. Point Probe Plus silicon tips for tapping mode imaging measurements with atomic force microscopy were purchased from Nanosensors (Neuchatel, Switzerland). 1H,1H,2H,2H-Perfluorododecyltrichlorosilane with a purity of 97 % was obtained from Sigma Aldrich.

3.2.2.2. Methods

The silicon substrates were cleaned by ultrasonicating in acetone followed by 2-propanol and finally treated with UV/Ozone (SAMCO UV-1, SAMCO Inc., Kyoto, Japan) for 10 min. The thickness of the oxide layer was measured using ellipsometer (Wvase 32, J.A.Woollam.Co., Inc., Lincoln, USA). The molds used were prepared as per the procedure described elsewhere [137]. The molds were used to imprint on PMMA using a Obducat 4 in. imprinter (Obducat, Sweden) at 160^0C, 60 bar pressure for 10 minutes to obtain the nanoporous templates as described in section 3.1. In short, PMMA-75k (Microresist Technologies, Germany) was used as imprinting resist. The resist was spun at 3000 rpm for 45 s to obtain 100 nm thick film using

CEE model 100CB spinner (Brewer Science Inc., MO, USA). Imprinting was then carried out and the residual polymer layer was removed using oxygen plasma in a reactive ion etcher (Oxford plasmlab100, Oxford Instruments, UK) at 60 mTorr, 100 W, 20 sccm O_2 for 14 seconds to yield nanoporous templates (NPTs). ZnO coatings on nanoporous templates were produced using Unbalanced Magnetron (UBM) sputtering system (Nanofilm Technologies International pte. Ltd., Singapore) using a ZnO target (99.995 % pure) with a copper backing plate. The variation in film uniformity was typically less than 5 %. All depositions were carried out at a chamber base pressure of less than 10^{-6} Torr. Ion beam milling (RF350, Veeco, Instruments Inc., NY, USA) was carried out to remove the excess ZnO deposited and to expose the polymer template beneath which was then removed using acetone wash and finally treated with UV/Ozone for 10 min. The pattern characteristics, viz. the mean heights, width, centre to centre spacing of reverse micelle arrays, nanoporous templates obtained upon NIL, and the ZnO nanodisc arrays were characterized using tapping mode AFM (Nanoscope IV Multimode AFM, Veeco Instruments Inc., NY, USA) and SEM (FESEM 6700F, JEOL, Tokyo, Japan). The cross-section of ZnO nanodiscs were obtained using transmission electron microscopy performed using Philips CM300 TEM operating at 300 kV and equipped with DX4 EDS system and Gatan Filter.

3.2.3. Results and discussion

The schematic of the process flow to create ZnO nanodisc arrays using block copolymer derived nanoimprint molds is illustrated in Figure 3.2.1. The nanoporous templates were subsequently coated with ZnO by RF sputtering for durations of 30

min, 45 min and 1 hr. The equivalent thickness of ZnO for these durations on bare Si substrates used as controls was found to be 75 nm, 100 nm and 125 nm, respectively. Given the depth of the PMMA pores of 90 nm, a 100 nm deposition of ZnO was used in order to achieve complete filling of the pores.

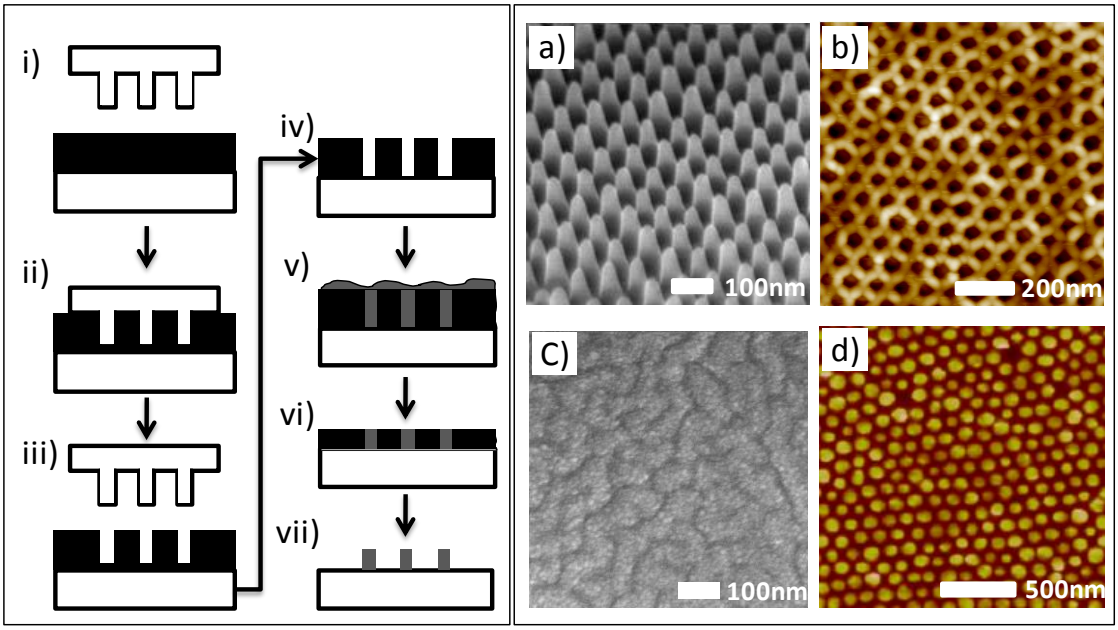


Figure 3.2.1 (i-vii) Illustration of steps towards creating ZnO nanodisc arrays by block copolymer derived NIL process. (a) FESEM image measured at 45^{o} tilt, showing Si nanopillar arrays derived out of block copolymer reverse micelles as etch masks (b) tapping mode AFM image of nanoporous PMMA templates (illustrated in step (iii) of schematic) (c) FESEM top-view measurement of sputtered ZnO films completely covering the nanoporous PMMA templates (illustrated by step (v) of schematic) (d) ZnO nanodisc arrays obtained upon ion-beam milling and removal of the PMMA templates.

FESEM investigation revealed that the ZnO films filled the pores and also formed a uniform overlayer on top of the templates. Definition of the ZnO nano arrays requires removal of the underlying nanoporous PMMA templates, as well as removing the ZnO overlayer. Towards this end, several treatments were tried separately such as ultrasonication or prolonged (~12 h) incubation in acetone, thermal annealing for 1 h at 150^{0}C, or UV light exposure. None of these treatments could get rid of PMMA

templates, which indicated a strong encapsulation and stabilization of the templates by the ZnO over coating. This eventually necessitated the use of ion beam milling, which enabled removal of ZnO overlayer, while at the same time exposed the PMMA templates underneath. Ion-beam milling was performed by exposing the ZnO coated nanoporous PMMA templates to Ar ions hitting the surface at an angle of 45^{o} for different durations of 200 s, 250 s, 300 s and 350 s. Ion beam milling for a duration of 250 s was found to be optimal towards removal of the ZnO overlayer and PMMA templates and resulted in the formation of a distinct ZnO nanopattern (Figure 3.2.2).

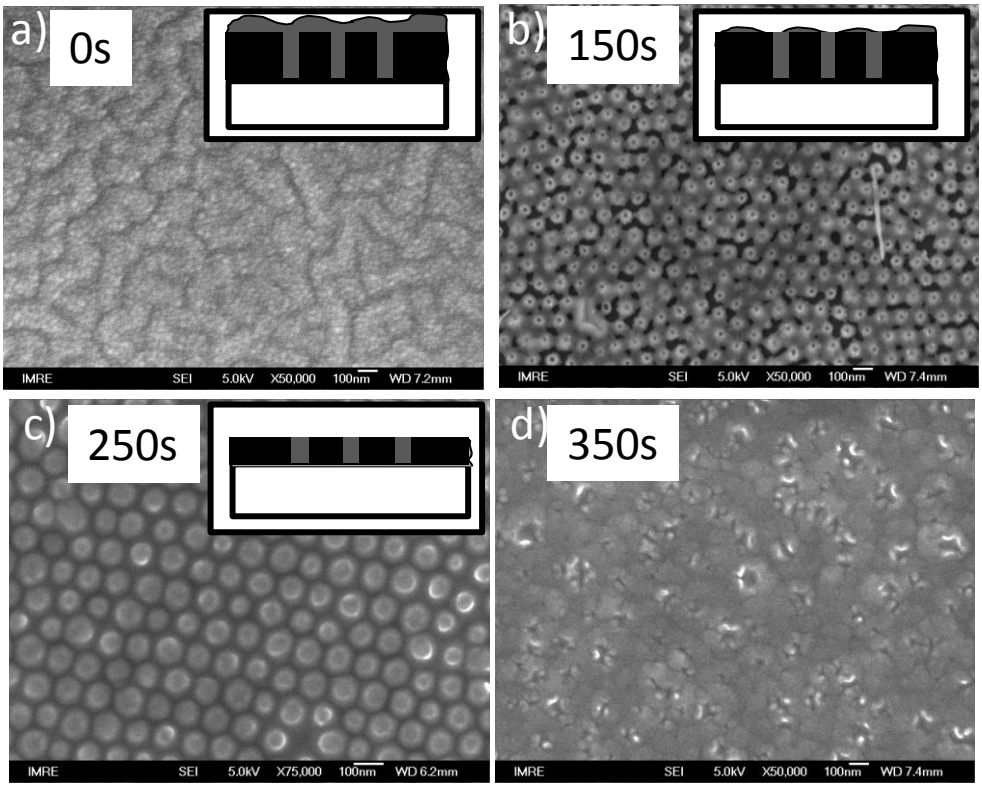


Figure 3.2.2 (a)-(d) Field emission scanning electron microscopy measurements on samples with ZnO coated nanoporous PMMA templates exposed to different durations of Ar ion-beam milling process show 250s to be most optimal in producing well-isolated ZnO nanostructures. Representative schematics of the evolution of the surface morphology are shown as inset. At 350s, the substrate appeared over etched, resulting in no recognizable features.

Subsequently, the ion milled sample was washed and rinsed in acetone followed by a brief exposure to UV-Ozone stripper to ensure complete removal of PMMA off the surface (Figure 3.2.3).

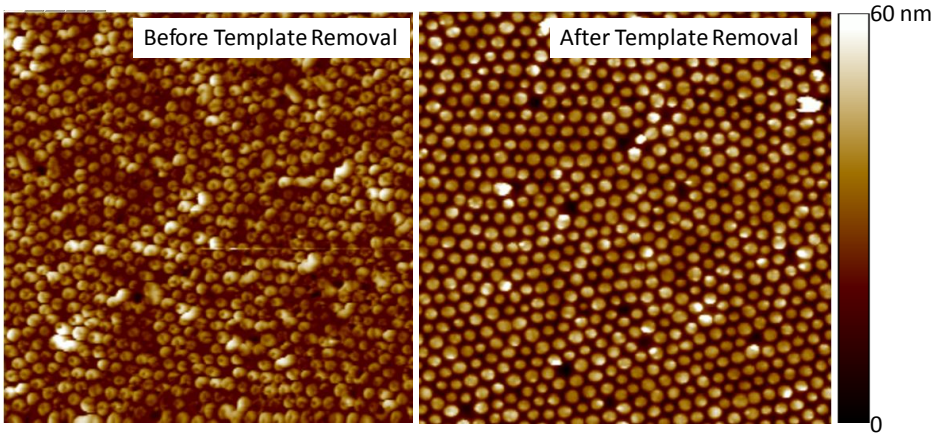


Figure 3.2.3 Tapping mode AFM measurements on ZnO coated nanoporous PMMA template subjected to 250 s of Ar ion milling, (left) before and (right) after removal of the PMMA templates.

The resulting ZnO nanoarrays were characterized by AFM, FESEM and TEM cross-sectional analysis (Figure 3.2.4 (a), (b) and (c) respectively). ZnO patterns were found to exhibit features with width of 65 nm, height of 25 nm, and periodicity of 80 nm. The histograms in height and diameter of the ZnO features as measured by AFM reveal a standard deviation of < 15% (Figure 3.2.4 (d)). The values for the feature width and heights obtained using AFM were consistent with those obtained from cross-sectional TEM analysis. Localized EDX analysis performed on and between ZnO features confirmed absence of any ZnO in-between the features and thereby demonstrated the integrity of the patterns (Figure 3.2.4 (e)).

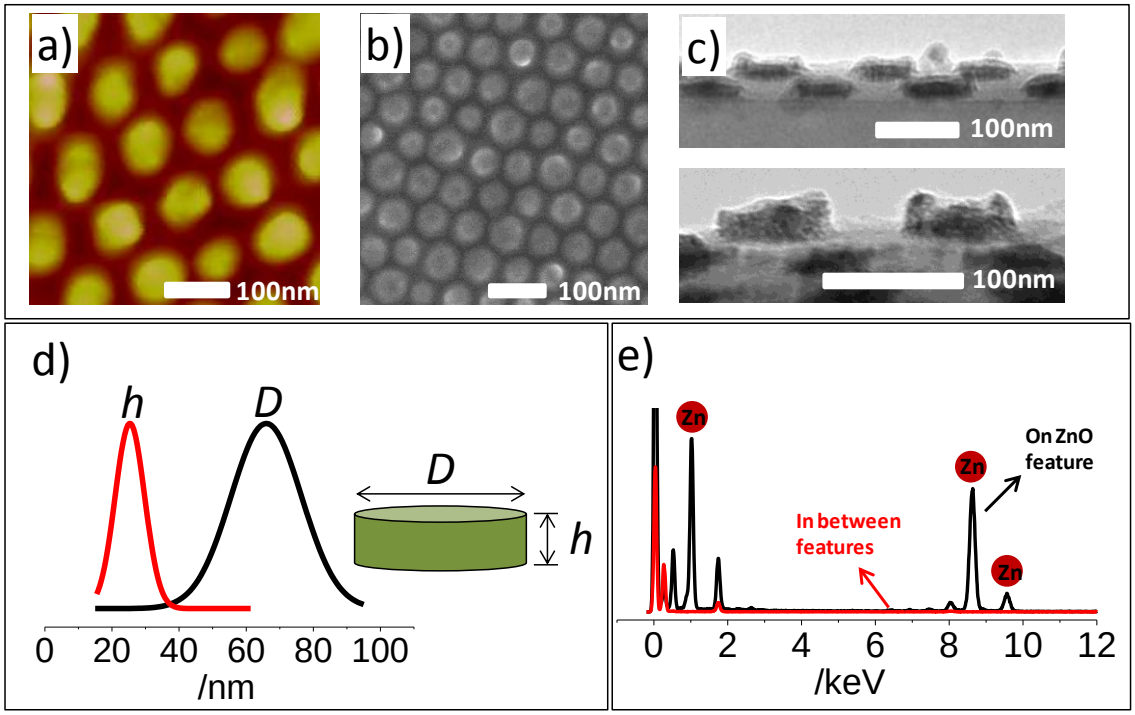


Figure 3.2.4 ZnO nanopatterns analyzed by (a) Tapping mode AFM (b) Field emission SEM and (c) cross-sectional TEM. (d) Distribution in height and width of the ZnO nanodiscs and (e) Localized EDS performed on and in between the features in ZnO nanopatterns shows absence of ZnO between features.

The feature width and periodicity of the ZnO were determined by nanoporous templates, which in turn were determined by the dimensions of the block copolymer reverse micelle nanopatterns that were used to produce the NIL molds. The feature heights were determined by the aspect ratio of the pillars, as well as the O_2 plasma RIE step employed to remove the residual layer. A controlled overexposure of the nanoporous templates to O_2 plasma RIE during residual layer removal can also help to widen the pore-diameters thereby enabling a larger ZnO feature widths with lower feature-to-feature separations. Tunability of the feature dimensions of ZnO arrays is therefore feasible by tailoring the block copolymer self-assembly process, or by varying the processing conditions. We have thus demonstrated here an optimal process that would result in uniform, high density nano disc arrays of ZnO over

macroscopic areas of surface. The fabrication process is simple to optimize and is less prone to reproducibility issues owing to lesser number of process variables in comparison to VLS, hydrothermal and sol-gel based ZnO patterning described in literature. The use of RF sputtering for material deposition and ion beam milling for material removal are non-specific to ZnO and can be readily extended to a range of other materials. Thus, the fabrication process is generic in nature and can be exploited to realize nanopatterns of other technologically relevant materials as well. In addition to RF sputtering we use here, other techniques for ZnO deposition such as pulsed layer deposition (PLD), or atomic layer deposition (ALD) can be employed to achieve features with desired material quality. If one desires to use other deposition tools such as molecular beam epitaxy (MBE) or metal organic chemical vapour deposition (MOCVD), the PMMA templates would not survive the high processing temperatures encountered in these processes. In such cases, the pattern transfer of nanoporous PMMA templates into an underlying inorganic thin film such as SiO_2 or Si_3N_4, can be applied as an alternative.

3.2.4. Conclusions

ZnO nanodisc arrays with narrow geometric distribution of features could be realized by a generic fabrication protocol utilizing NIL performed using block copolymer derived silicon nanopillar molds. In the present work, it has been established that the densely patterned, well isolated ZnO nanodisc array can be highly advantageous and can be used as potential charge storage centers for the next generation non-volatile memory devices at low operating voltages and scaled tunneling oxides. The fabrication protocol is generic and can be applicable for producing patterns of other

materials, and is therefore of high interest for diverse applications. The performance of the MOS capacitor memory device containing the ZnO nanodiscs is demonstrated in Section 5.1.

SECTION 3.3

PATTERNING OF ROBUST NANOARRAYS OF ZINC OXIDE THROUGH AREA SELECTIVE ALD

3.3.1. Introduction

The fabrication of ZnO nanodiscs as discussed in Section 3.2 involved a top-down approach of sputtering ZnO onto the NPTs. However, the approach described in this section demonstrates the use of NPTs for guiding the patterns by employing a surface sensitive atomic layer deposition (ALD) technique which is a well established bottom-up approach. Thus, we emphasize the versatility of using the NPTs to define the resulting material patterns using both top-down and bottom-up techniques. PMMA templates derived out of block copolymer self-assembly assisted NIL process are used to guide ALD to create high-quality robust ZnO nanopatterns. Nanopatterns with sub-100 nm feature and spatial resolutions, with standard deviations < 15 % in height, width and pitch are achieved this way.

Details of the performance of capacitor device incorporating the above mentioned ZnO nanopatterns are discussed in Section 5.1. In short, the capacitor showed a flat-band voltage shift of 2.82 V at relatively low operating voltage of 10 V. A high charge trap density of 7.39×10^{18} cm^{-3} combined with excellent retention of ~ 91 % after 10^4 s upon extrapolating is observed with low tunneling oxide thickness of 3 nm. This demonstrates the significant promise of the ZnO nanopatterned arrays to act as charge storage centres for potential application in non-volatile flash memory devices.

3.3.2. Experimental

3.3.2.1. Materials

Poly (methyl methacrylate) (PMMA) of molecular weight 75,000 g/gmol was purchased from Microresist Technologies (Berlin, Germany) and used without further purification. 2-propanol and Acetone were obtained as anhydrous solvents with purity > 99 % from Sigma-Aldrich Pte Ltd. Prime grade silicon wafers were obtained from Silicon Valley Microelectronics (Santa Clara, CA, USA). Silicon wafers with thermally grown oxide were obtained from GlobalFoundries, Singapore. Point Probe Plus silicon tips for tapping mode imaging measurements with atomic force microscopy were purchased from Nanosensors (Neuchatel, Switzerland). 1H,1H,2H,2H-Perfluorododecyltrichlorosilane with a purity of 97 % was obtained from Sigma Aldrich.

3.3.2.2. Methods

The silicon substrates were diced and cleaned by ultrasonicating in acetone followed by 2-propanol and finally exposed to UV/Ozone (UV-1, SAMCO Inc., Kyoto, Japan) for 10 minutes. Ellipsometry (Wvase 32, J.A.Woollam.Co., Inc., Lincoln, USA) was used to measure thickness of the oxide layers. The NIL molds were fabricated as reported earlier [137] using reverse micelle arrays coated from 0.5% (w/w) solution of polystyrene-*b*-poly(vinyl pyridine) in *m*-xylene. PMMA-75k (Microresist Technologies, Germany) was used as imprinting resist and was spun at 3000 rpm for 45 s to obtain 100 nm thick film using CEE model 100CB spinner (Brewer Science Inc., MO, USA). The molds were used to imprint on PMMA using a Obducat 4 in.

imprinter (Obducat, Sweden) at 160^0C, 60 bar pressure for 10 minutes to obtain the nanoporous templates as described in Section 3.1. Oxygen plasma exposure for residual layer removal following NIL was performed using reactive ion etcher (Oxford plasmlab100, Oxford Instruments, UK) at 60 mTorr, 100 W, 20 sccm O_2 for 14 seconds. AFM (Nanoscope IV Multimode AFM, Veeco Instruments Inc., NY, USA) and FESEM (JEOL 6700F, Tokyo, Japan), and TEM (Philips CM300, Amsterdam, Netherlands) were used to characterize the films during each step of fabrication. The TEM is equipped with DX4 EDS system and Gatan Filter that enables high-resolution elemental analysis. The ALD of ZnO was performed using an ALD system (TFS200, Beneq, Vantaa, Finland) at 70^oC. Diethyl zinc and de-ionized water were used as the precursors and were introduced into a viscous flow ALD chamber in pulses as $(C_2H_5)_2Zn$ (17 mTorr, 0.3 s) / N_2 purge (2 mTorr, 2 s) / H_2O (17 mTorr, 0.3 s) / N_2 purge (2 mTorr, 2 s)

3.3.3. Results and discussion

As mentioned in 3.3.2.2. Methods, a representative plot of chamber pressure versus time for a typical ALD cycle is shown in Figure 3.3.1 below. In our case, N_2 was used both as a carrier gas and purge gas.

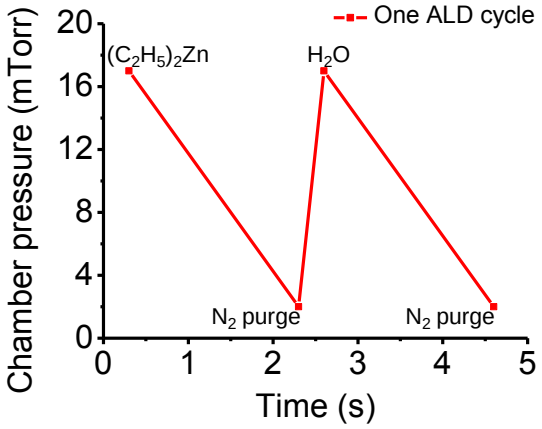


Figure 3.3.1 Plot of chamber pressure versus time for one ALD cycle.

ALD was first performed on bare OH-terminated Si substrates (without templates) to estimate growth rate, and to follow morphology of the films. Based on this control experiment, the ALD rate of 0.11 nm/cycle (or 1.43 nm/min) and RMS roughness of ~0.7 nm were obtained was obtained as shown in Figure 3.3.2. The values are comparable with those reported in literature [74, 139, 140].

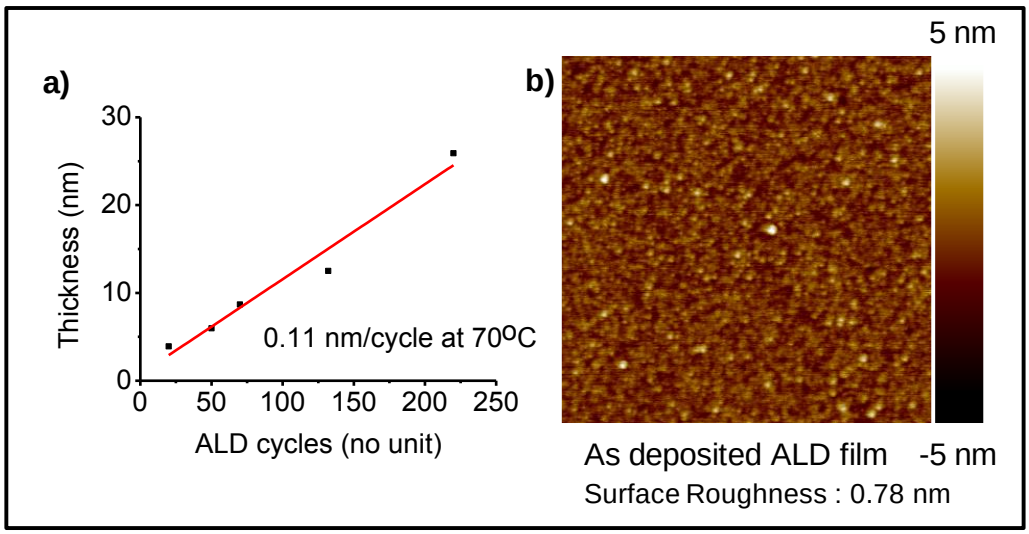


Figure 3.3.2 (a) Plot of ZnO film thickness versus ALD cycles performed at 70^0C and (b) Tapping mode AFM image of ZnO thin film (100 cycles) deposited on bare Si showing roughness of ~ 0.7 nm.

In this work, we employ reverse micelle arrays of polystyrene-*block*-poly (2-

vinylpyridine) 114 kDa, f_{PS}~0.5 in *m*-xylene to prepare Si nanopillar molds for NIL. The molds exhibit pillar height of ~120 nm, diameter of 65 nm and a pitch of 80 nm. These molds were used to create nanoporous PMMA films in a standard NIL process. The nanoporous PMMA templates were exposed to short oxygen plasma to remove the residual layer beneath the pores and expose the Si surface beneath. The use of O_2 plasma, besides removal of the residual layer, results in an OH-terminated Si surface within the pores, suitable for atomic layer deposition in the next step.

On completion of the pattern definition, an atomic layer deposition of ZnO was carried out on the nanoporous templates. Each ALD cycle consisted of i) Diethyl Zinc pulse (300 ms) ii) Nitrogen purging (2 s) iii) Water pulse (300 ms) iv) Nitrogen purging (2 s). The process flow to demonstrate the complete fabrication of ZnO nanoarrays is shown in Figure 3.3.3.

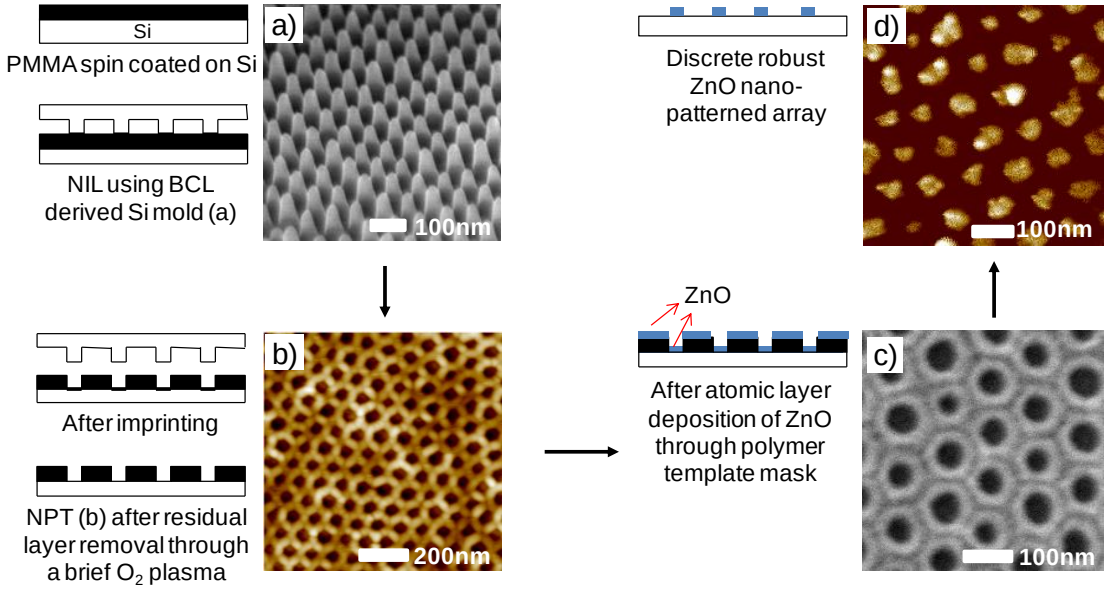


Figure 3.3.3 The process steps involved in fabricating the robust ZnO nanoarrays through area selective atomic layer deposition.

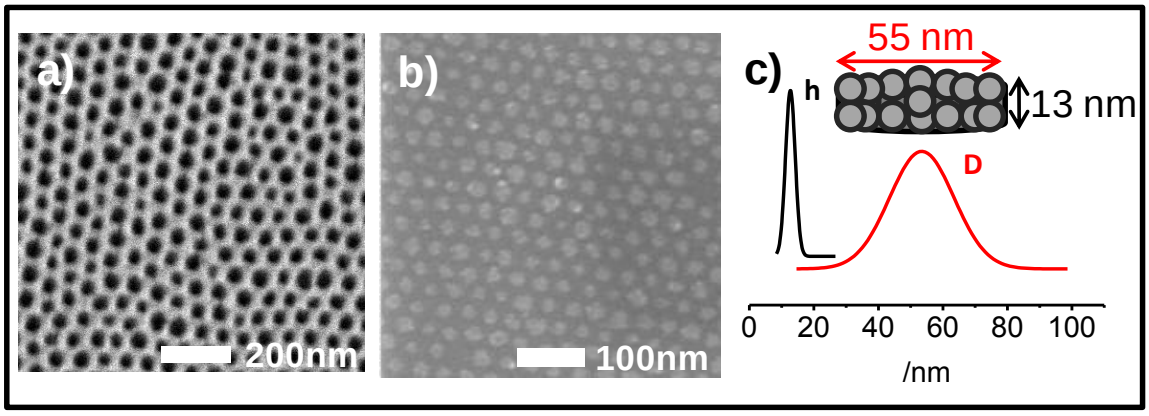


Figure 3.3.4 FESEM of the (a) NPT used as mask to create the (b) nanopatterned ZnO after polymer lift off showing the (c) distribution in diameter and height.

The nanoporous template with through-pores is subjected to ALD of ZnO for 50, 100 and 200 cycles. The ALD was performed at a low temperature of 70^0C in order to prevent pattern loss from occurring due to melting of PMMA above its Tg. ALD of ZnO performed at low temperature have been shown earlier to yield polycrystalline films suitable for memory devices [74, 139, 141]. Each ALD cycle comprised of alternating sequence of diethyl zinc and water vapour interspersed by a nitrogen purge.

After deposition of ZnO, the samples were ultrasonicated in boiling acetone for 1 h to lift-off the polymer template. Analysis of the resulting patterned substrates showed 100 cycles of ALD to be optimal in producing well-defined ZnO nanoarrays (Figure 3.3.4) of height 13 nm and diameter 55 nm. The results of different ALD exposures to fabricate ZnO nanoarrays are shown in Figure 3.3.5.

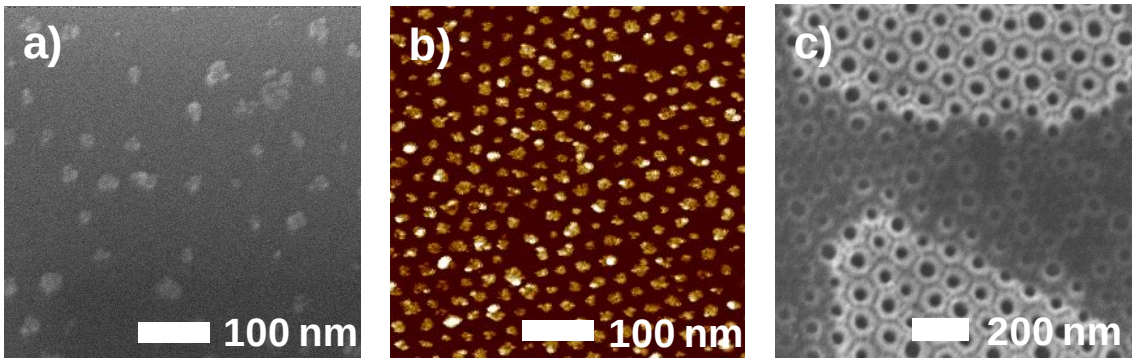


Figure 3.3.5 FESEM and AFM images of (a) 50 cycles (b) 100 cycles and (c) 200 cycles of ALD performed to fabricate ZnO nanoarrays. After ultrasonication in acetone, (b) 100 cycles of ALD proved to be optimal in delivering discrete ZnO arrays.

For 50 cycles of exposure, an incomplete ZnO growth was observed. For 200 cycles of exposure, the PMMA templates seem to cross-link due to in-growth of ZnO within the template resulting in a resistance to lift-off. Such cross-linking is expected to result due to the hydrophilic carbonyl functionality of PMMA that enables concentrating the zinc precursors within the template [142]. This could occur either through coordination of zinc with carbonyl ligands of PMMA, or through decomposition induced by moisture that is trapped within the polymer template. Such concentration of the ALD precursors within polymer matrices has been exploited toward templated in-situ synthesis of inorganic materials [137, 143, 144]. Earlier literature on selective area ALD has shown ideal masks to be those that exhibit minimal interaction with (or, be passive towards) the volatile precursors used, and exhibit sufficient height to prevent over-growth [26, 145]. PMMA would thus not constitute as an ideal ALD mask; however, it can be used with sufficient optimization to yield atomic layer deposited material patterns of interest [26, 142, 145]. This offers process advantages given the fact that PMMA is widely employed as a resist for NIL as well as e-beam or photolithography.

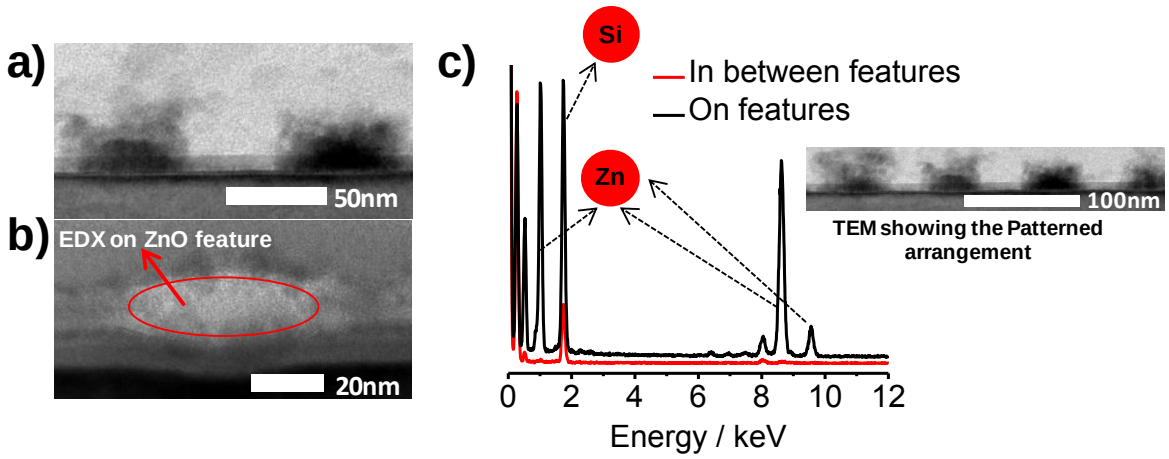


Figure 3.3.6 Transmission electron microscopy image of the (a) ZnO nanopatterns confirming the presence of ZnO through the (b) Localized EDX performed on the feature showing the (c) absence of ZnO in between features.

Characterizations of the ZnO arrays by AFM and FESEM show well-defined arrays exhibiting heights of ~13 nm and diameter of ~55 nm, and pitch of ~80 nm. These characteristics agree well with those expected from the NIL molds used. Despite clearly observed pattern formation, the ability of ZnO precursors to diffuse and grow within the PMMA templates raises the question whether the resulting features are indeed isolated. This was probed using EDX analysis performed with high spatial resolutions within the TEM equipment (Figure 3.3.6). The EDX spectra acquired on and between the features showed presence of Zn only on the features, thereby confirming their discrete nature. Figure 3.3.7 shows the macroscopic array of ZnO nanoparticle array.

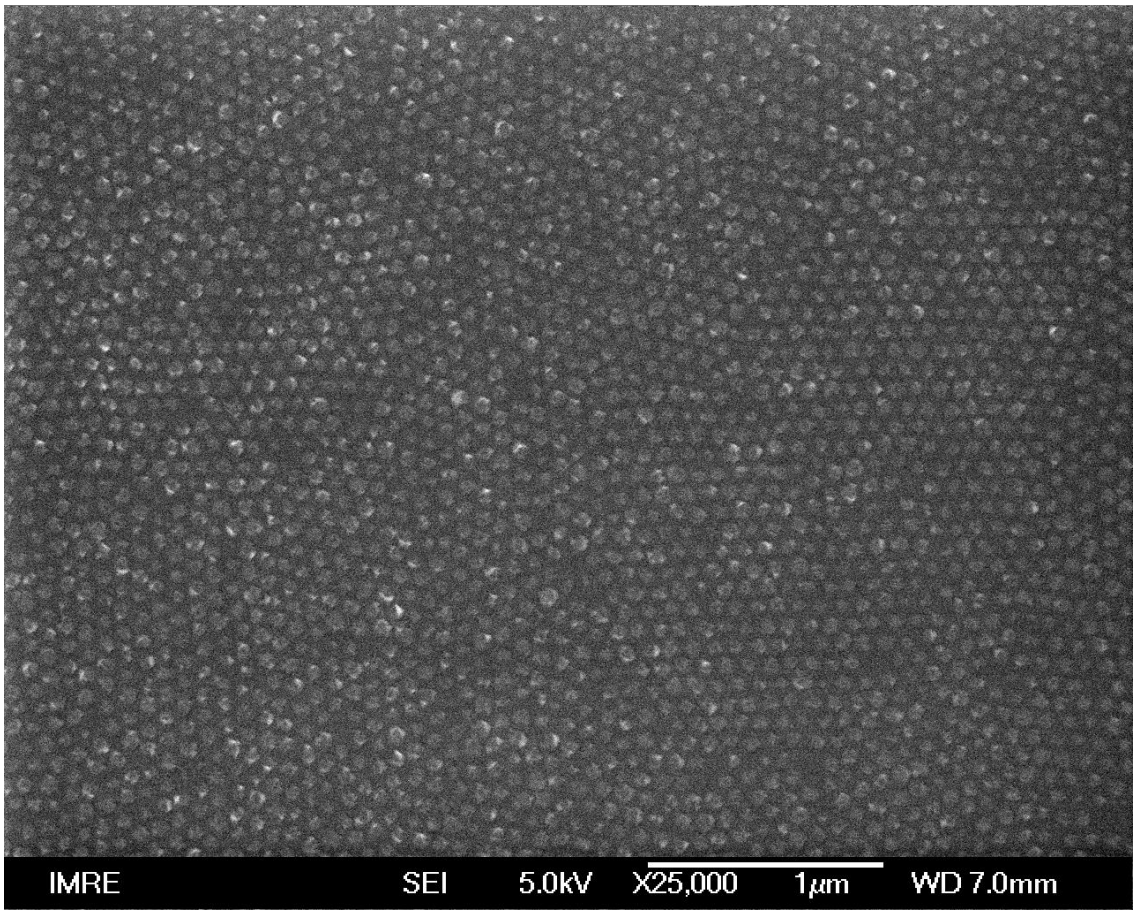


Figure 3.3.7 Representative FESEM measurement of ZnO nanopatterns spanning 1.5 cm x 1.5 cm chips.

As an additional confirmation, an unpatterned PMMA thin film (~110 nm) was exposed to 100 cycles of ALD with lift off performed under identical conditions as used for the nanoporous templates (Figure 3.3.8). XPS analysis confirmed that the lift off indeed left no traces of ZnO on surface, thereby suggesting that the substrate/PMMA interface in the template would have remained unaffected during ALD process.

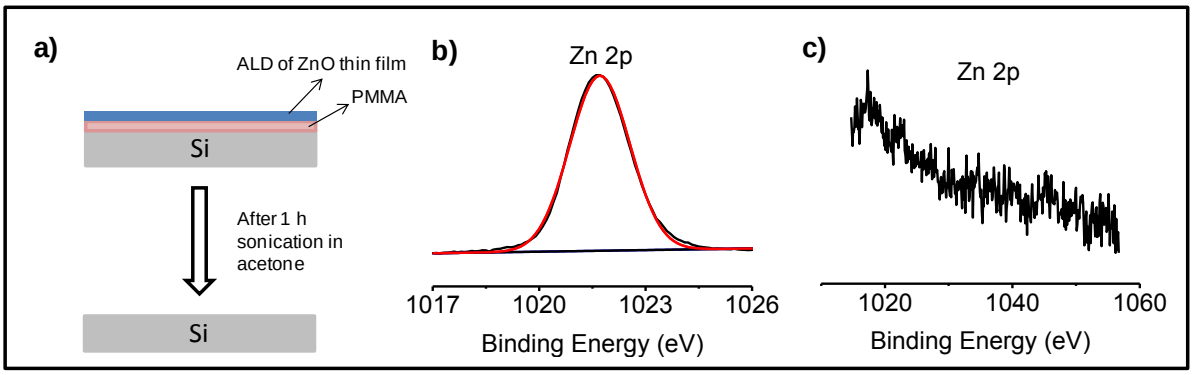


Figure 3.3.8 (a) Schematic explaining the ALD (under similar conditions to produce nanopatterns) of ZnO thin film on PMMA continuous layer as a control to demonstrate the absence of ZnO after sonication. XPS of Zn 2p spectra (b) before and (c) after ultrasonication.

Further, the fact that ZnO patterns survived tough ultrasonication conditions for duration of 1 h suggests a strong adhesion of the features to the substrate, as expected for an ALD process. The AFM measurements of ZnO patterns reveal features that seem rougher in comparison to the films obtained on unpatterned control Si substrates. To investigate a possible contribution to the increase in roughness due to ultrasonication, the ZnO thin films on the control (OH- terminated) Si substrates obtained upon 100 cycles of ALD were subjected to identical conditions of sonication as used for the lift-off of the templates. The RMS roughness was found to increase from 0.7 nm to 1.7 nm upon sonication. XPS analysis of the films showed no decrease in intensity of the Zn peaks, confirming that no loss of material occurred upon sonication, but only an increase in roughness (Figure 3.3.9). Such increase in roughness can be attributed to the structural changes occurring on surface in response to the mechanical forces of ultrasound [146].

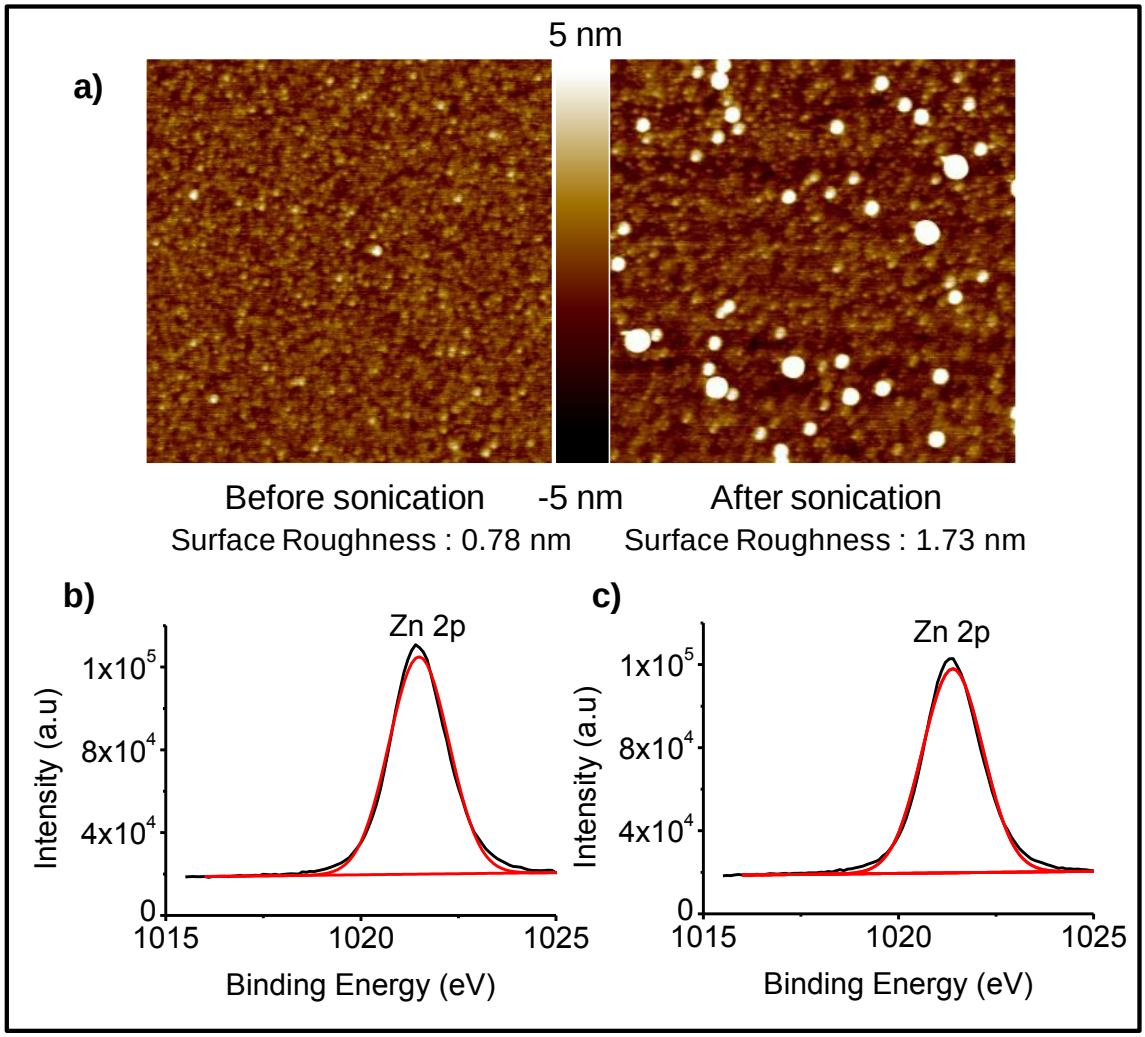


Figure 3.3.9 (a) Tapping mode AFM images of ZnO thin film deposited on bare Si before and after ultrasonication in acetone. XPS of ZnO thin film deposited on bare Si chip showing Zn 2p (b) before and (c) after ultrasonication with no appreciable change in the intensity.

Besides definition and robustness, an additionally useful capability follows from the low temperature processing that makes the approach a viable patterning solution for flexible substrates. In addition, since the feature size and periodicity of ZnO nanopatterns was guided by the polymer templates, tunability of these attributes in the ZnO arrays is feasible through tailoring the block copolymer self-assembly process or by varying the processing conditions. The molds used for the study were able to deliver identical copies of templates even after 50 imprinting sequences. The re-

usability requires re-deposition of the anti-stiction perfluorosilane coatings on the mold (cf. experimental information) once every 15 imprinting sequences.

3.3.4 Conclusions

The work presents a facile route to high-density periodic arrays of mechanically robust ZnO nanostructures with excellent pattern definition (low standard deviations in feature width, height and pitch) using selected area ALD within templates fabricated by a BCL-NIL process. The nanofabrication approach benefits from combined advantages due to BCL and NIL, and in particular the re-usability of the NIL molds. The molds were used over 50 times (with an un-determined upper limit) without compromising its quality or ability to generate identical pattern copy each time. The process can be readily extended to produce high-resolution patterns of a range of materials that can be grown by ALD. The low-temperature processing opens up opportunities to exploit the technique for patterning flexible substrates. The ability to create nanopatterns of ZnO, or possibly other semiconductors opens new avenues to create functional components for use within nanoscale devices for photovoltaic (e.g. solar cells, photocatalysis), and optoelectronic applications (e.g. LEDs).

SECTION 3.4

FABRICATION OF sub-50 nm ARRAYS OF ZINC OXIDE THROUGH PS-*b*-PVP MICELLAR TEMPLATES

3.4.1. Introduction

ZnO nanopatterns on different substrates offer an interesting opportunity to investigate and study various material properties in combination with the substrate properties. The nature of doping in silicon which can either be n-type or p-type has a distinct effect on the electrical and electronic properties of the material that is patterned on top of it. ZnO nanostructures generally have a lot of zinc interstitials and oxygen vacancies making it intrinsically n-type [9, 147]. The electrical behaviour of the ZnO nanofeatures on p-Si is different from that of n-Si and this characteristic is exploited in fabricating diodes or schottky barriers [148], transistors or capacitors [147].

There has been an increasing interest towards exploiting the ZnO nanostructures for fabricating electronic devices compatible with silicon technology. There are many reports on the utilization of ZnO nanostructures in electronics particularly in memory devices [10], thin film transistors [111, 149] and diodes [64]. Earlier reports on the ZnO nanofilm based memory devices [150, 151, 152] built on Si, though describe the electrical characteristics of the ZnO nanofilm, they do not exhibit good device performance such as meeting the minimum memory window required in non-volatile memory applications [33], use of thin scalable SiO_2 tunnel oxide layer, lower program/erase voltages, good charge retention and higher writing speeds [153]. This calls for a new device structure targeting such issues. Section 3.2 and Section 3.3 discussed the nanopatterning of sub-100 nm spatially isolated ZnO nanoarrays while this section describes another novel way of producing high density ZnO nanopatterns through in-situ synthesis using block copolymer templates with a sub-50 nm spatial

resolution and their application as charge storage centres in flash memory devices. The significance of this kind of patterning lies in the fact that the block copolymers are directly used as templates for pattern transfer to ZnO, instead of creating a Si mold out of it to produce nanoporous polymer templates for subsequently guiding ZnO. This saves both time and resources while at the same time prove its capability to produce scaled down device features for NVM applications. The results show a higher charge trap density of 3.47 x 10^{18} cm^{-3}. In contrast, the device fabricated on n-Si showed negligible or no hysteresis, thereby helping to understanding the electrical behavior of the ZnO floating gate patterns. The electrical characteristics are described in detail in Chapter 5, Section 5.1.

3.4.2. Experimental

3.4.2.1. Materials

Acetone and 2-propanol were obtained as anhydrous solvents with purity > 99 % from Sigma-Aldrich Pte Ltd. Prime grade silicon wafers were obtained from Silicon Valley Microelectronics (Santa Clara, CA, USA). Silicon wafers with thermally grown oxide were obtained from GlobalFoundries, Singapore. Point Probe Plus silicon tips for tapping mode imaging measurements with atomic force microscopy were purchased from Nanosensors (Neuchatel, Switzerland).

3.4.2.2. Methods

The silicon substrates were diced and cleaned by ultrasonicating in acetone followed

by 2-propanol and finally exposed to UV/Ozone (UV-1, SAMCO Inc., Kyoto, Japan) for 10 minutes. Ellipsometry (Wvase 32, J.A.Woollam.Co., Inc., Lincoln, USA) was used to measure thickness of the oxide layers. The block copolymer templates to guide the patterning of ZnO was obtained by spin coating (CEE model 100CB spinner, Brewer Science Inc., MO, USA) at 3000 rpm, a 0.5 % (w/w) solution of reverse micelles of polystyrene-block-poly(4-vinylpyridine) (PS-*b*-P2VP, MW 80.5 kDa, f_{PS} 0.78, PDI 1.09) from *m*-xylene. The coated micelles were then subjected to atomic layer deposition of ZnO performed using an ALD system (TFS200, Beneq, Vantaa, Finland) at 70^0C. Diethyl zinc (used as the Zn precursor) and de-ionized water were introduced into a viscous flow ALD chamber in pulses as $(C_2H_5)_2Zn$ (17 mTorr, 0.3 s) / N_2 purge (2 mTorr, 2 s) / H_2O (17 mTorr, 0.3 s) / N_2 purge (2 mTorr, 2 s). N_2 was used both as a carrier and purge gas. Oxygen plasma exposure for removing the polymer was performed using a reactive ion etcher (Oxford plasmlab100, Oxford Instruments, UK) at 65 mTorr, 30 W, 20 sccm O_2 for 15 minutes. AFM (Nanoscope IV Multimode AFM, Veeco Instruments Inc., NY, USA) and FESEM (JEOL 6700F, Tokyo, Japan), and TEM (Philips CM300, Amsterdam, Netherlands) were used to characterize the features during each step of fabrication. The TEM was equipped with DX4 EDS system and Gatan Filter that enabled high-resolution elemental analysis. The SiO_2 control oxide was deposited using a SiO_2 target (99.995 % pure) with a copper backing plate in unbalanced magnetron (UBM) sputtering system (Nanofilm Technologies International Pte. Ltd., Singapore). The variation in film uniformity was typically less than 5 %. All depositions were carried out at a chamber base pressure of less than 10^{-6} Torr. X-ray photoelectron spectroscopy (XPS) (AXIS UltraDLD, Kratos Analytical Ltd, Manchester, UK) measurements were performed using monochromatized Al Kα X-ray source (1486.71

eV photons) at a constant dwell time of 100 ms and pass energy of 40 eV.

3.4.3. Results and discussion

The fabrication protocols to produce the ZnO nanopatterns through RF sputtering and ALD using templates produced from a combination of BCL and NIL techniques were described in previous sections [154, 155]. Briefly, in the case of fabricating ZnO nanopatterns by RF sputtering, the nanoporous polymer templates (NPTs) carved out of NIL using high density Si molds derived from BCL is used for template assisted patterning. ZnO was sputter deposited onto the NPTs followed by ion bean milling to remove any excess ZnO overlayer. An acetone wash resulted in the removal of polymer templates completely to realize well isolated ZnO nanopatterns of feature diameter of ~65 nm and height of ~25 nm. In the second approach, an ALD of 100 cycles of ZnO over the nanoporous templates was carried out. This was followed by the template lift off by ultrasonicating in boiling acetone for an hour. This resulted in the ZnO nanopatterns with the feature diameter of ~55 nm and height of ~13 nm.

Although the techniques employed NIL assisted templates to produce ZnO patterns, the NIL molds were still obtained from BCL. So, any tunability in the feature geometry was possible only prior to the making of molds during self organization of the reverse micelles. On the other hand, the BCP template assisted pattering does not face such tunability issues and thus could readily be employed as a direct method to fabricate spatially isolated sub-50 nm ZnO nanopatterns. The ZnO feature in the patterns exhibited a diameter of ~38 nm and height of ~14 nm fabricated in a precisely controlled fashion in situ (Figure 3.4.1). Although, there are reports on in-

situ synthesis of inorganic materials [137, 143, 144] such as TiO_2, Al_2O_3 through ALD of precursors within templated polymer matrices, it becomes increasingly difficult to optimize the ZnO ALD process in terms of precursor-loading to ensure selective decomposition and to avoid any non-selective deposition that may otherwise compromise the resulting pattern quality and integrity. In this direction, we demonstrate the fabrication of ZnO nanopatterns of sub-50 nm spatial resolution obtained by incorporating a volatile zinc precursor through selective decomposition of the precursor within the core of the reverse micelles.

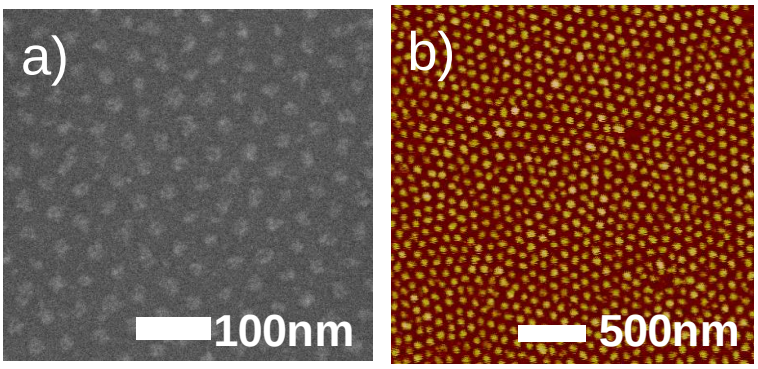
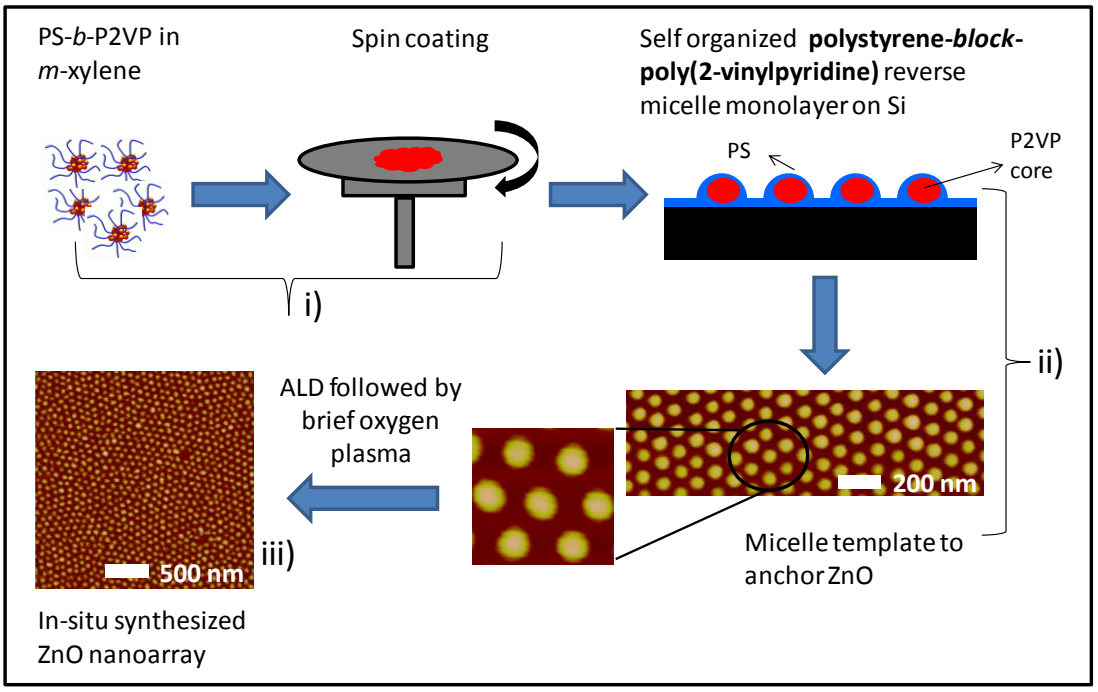


Figure 3.4.1 (a) FESEM and (b) AFM images of ZnO nanopatterns obtained through in-situ decomposition of Zn precursors into the micelle templates.

As described in Schematic 3.4.1, PS-*b*-P2VP (MW 80.5 kDa, f_{PS} 0.78, PDI 1.09) reverse micelles was spin coated from *m*-xylene at 3000 rpm, acceleration of 3000 rpm/s, and concentration of 0.5% (w/w) onto the silicon substrates. These amphiphlic diblock copolymers self-assembled on surfaces upon solvent evaporation. When optimized, the coatings exhibited continuous, quasi hexagonally ordered arrays of polymeric features that were used as templates for patterning purposes. The choice of solvent, the concentration of the micelles in the solution, humidity and the speed of coating can be used as handles to achieve high-resolution changes in the feature size and pitch in the patterns [102].



Scheme 3.4.1 Schematic diagram explaining the (i) spin coating of PS-*b*-P2VP reverse micelles. (ii) AFM image of the micelles that acted as templates for in-situ decomposition of Zn precursors into the PVP core to produce (iii) sub-50 nm ZnO nanoarrays upon exposure to oxygen plasma.

The Si chip containing a coating of reverse micelles is exposed to diethyl zinc vapors within an ALD chamber. The $(C_2H_5)_2Zn$ concentration was controlled by varying the number of cycles and time of exposure. Each cycle of exposure consisted of one $(C_2H_5)_2Zn$ pulse and one H_2O pulse with a nitrogen purge between each precursor pulse. High degree of control over the vapour concentrations employed in a typical ALD system allowed excellent control over the degree of incorporation of zinc precursor. As a process of optimization, four different experiments along with controls were carried out, when the PS-*b*-P2VP coatings were exposed to 10, 30, 50 and 100 cycles of exposure. The ALD was performed on bare silicon substrates without templates as controls to determine the growth rate and to highlight the fact that the deposition was indeed highly controlled (Figure 3.3.2 in Section 3.3). The $(C_2H_5)_2Zn$ selectively decomposed within the hydrophilic PVP core, thereby

anchoring its position defined by the polymer template. The PS thin film being non-selective to zinc precursor acted as mask preventing any deposition of zinc onto underlying silicon surface. After incorporation of the zinc precursor, the polymeric template could be removed by O_2 plasma etch to obtain ZnO nanoparticle arrays in an in situ fashion. The micelle templates subjected to 10 cycles did not reveal any patterns while 100 cycles compromised on the pattern morphology due to non-selective deposition of ZnO. 50 cycles of ALD on the micelle templates proved to be optimal in revealing well defined, high density and discrete nanopatterns of ZnO (Figure 3.4.2).

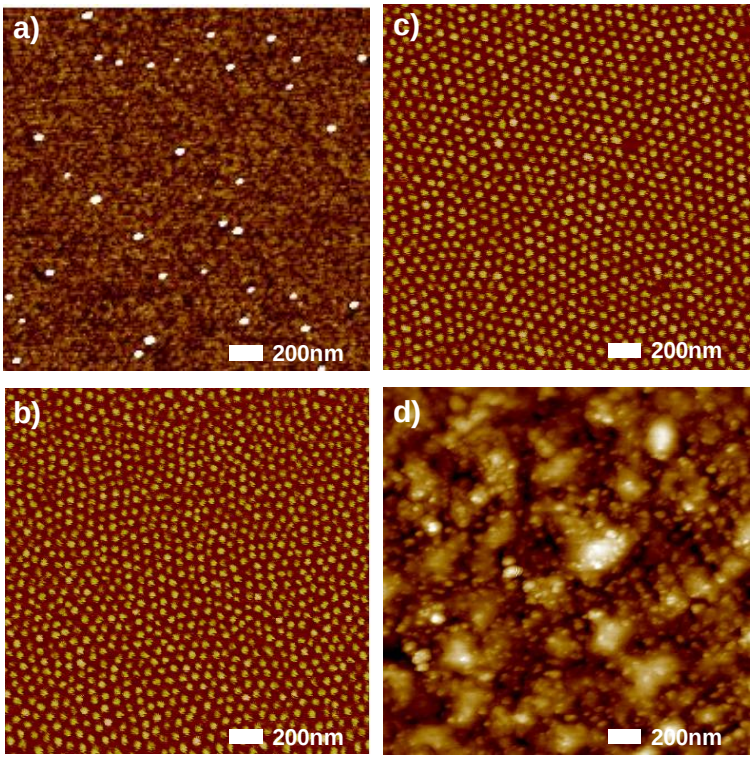


Figure 3.4.2 PS-*b*-PVP reverse micelles subjected to (a) 10, (b) 30, (c) 50 and (d) 100 ALD cycles for fabricating ZnO nanoarrays followed by oxygen plasma exposure. 50 cycles of exposure prove to be more optimal in delivering discrete ZnO arrays.

The resulting ZnO nanopatterned arrays exhibited a diameter of 38 nm and height of 14 nm for 50 cycle exposure as shown in Figure 3.4.3. Characterization of the ZnO

nanofeatures by FESEM and AFM (Figure 3.4.1 (a) and (b)) show well defined discrete nanoarrays. The ZnO nanoarrays exhibited a clear isolation after a 50 cycle ALD exposure and the discrete nature of the features was further confirmed by performing a cross section TEM of the ZnO features along with EDX probed with high spatial resolutions. The EDX spectra acquired on and between the ZnO features showed presence of only Zn on the features, thereby confirming the pattern integrity as shown in Figure 3.4.4.

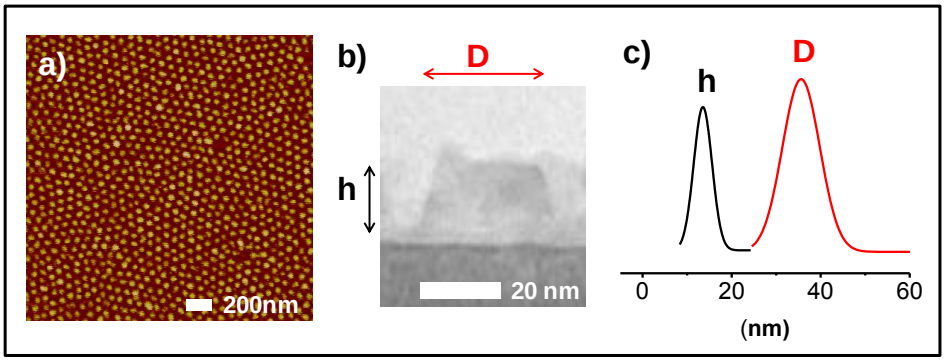


Figure 3.4.3 (a) Tapping mode AFM image of ZnO nanopatterns obtained after 50 cycles of ALD, (b) TEM cross section of a representative ZnO feature and (c) feature size distributions determined by AFM revealing mean values of 38 nm for diameter ('D') of 14 nm for height ('h').

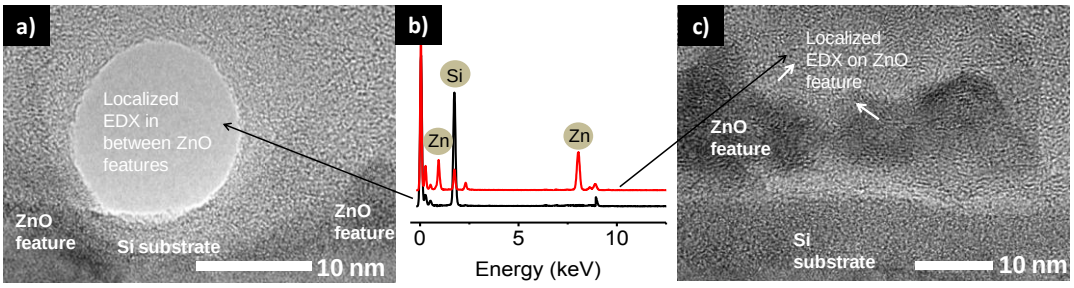


Figure 3.4.4 TEM images showing (a) the localized EDX performed in between the ZnO features and (c) on the features. (b) EDX showing the absence of Zn in between the features.

Since the patterning of ZnO is achieved through polymeric templates, it is essential to check the resulting ZnO nanopatterns for any residual polymeric contamination. XPS

analysis of the ZnO nanopatterns showed that no nitrogen was present and confirmed that the oxygen plasma has completely removed the polymer (Figure 3.4.5).

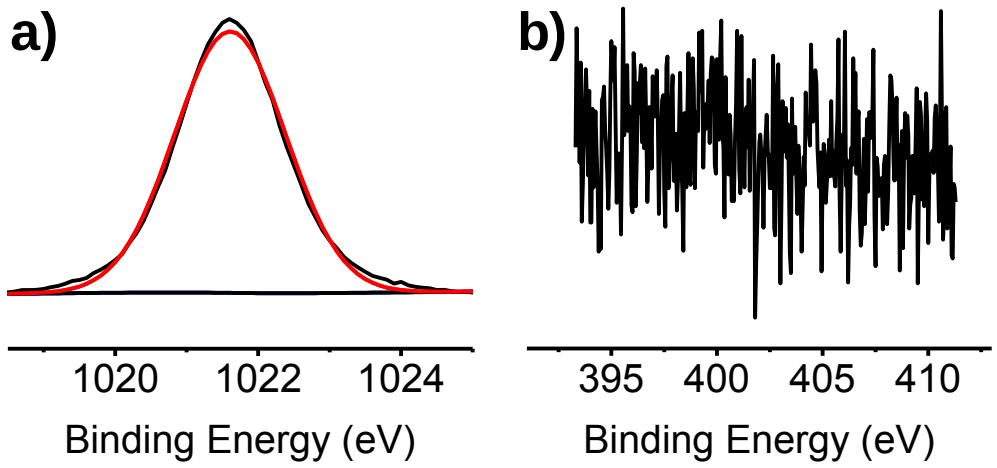


Figure 3.4.5 XPS of ZnO nanopatterns formed after in-situ decomposition of Zn precursors into micelles followed by an oxygen plasma exposure show the presence of (a) Zn 2p and absence of (b) N 1s.

The feature size, periodicity and spacing of ZnO nanopatterns were guided by the polymer templates and hence tunability of the geometric attributes in the ZnO arrays is feasible through tailoring the block copolymer self-assembly process. The advantages of this fabrication protocol are derived from the controlled incorporation of the precursor selectively into the micelle core without disturbing the morphology of the polymer template. Since ALD is employed to create patterns, ZnO nanofeatures are mechanically robust. In addition, the nanofeatures are produced on a macroscopic scale in a highly controlled and tunable manner offering a high feature resolution that is otherwise difficult to attain through other techniques. This apart, the ability to pattern at low operating temperatures positions this protocol ahead of other techniques for patterning on flexible plastic substrates.

3.4.4. Conclusions

The work presents a simple yet highly controlled route to produce high-density nanopatterns of ZnO with excellent pattern definition (low standard deviations in geometric attributes of the features) by incorporating the ALD precursor selectively into the micelle templates. The advantage is derived from the use of ALD that provides a high degree of control and from the use of block copolymer templates which offers tunability of the template that guides and controls the geometric attributes of the resulting ZnO nanopatterns. The precursor dosage, exposure cycles, reproducibility and the processing conditions can be manipulated to obtain reproducible patterns of high quality and resolution. The ability to create robust nanopatterns of ZnO in a tunable and controlled fashion widens the spectrum of applications of the patterns as basic building components in photovoltaics, solid state lighting and optoelectronics.

Preliminary results of the electrical characteristics of the arrays show their promise as charge storage centres with high storage density and excellent retention characteristics demonstrating significant potential for charge trap flash memories and are described in detail in Section 5.1.

CHAPTER 4

HIERARCHICALLY BUILT HETERO SUPERSTRUCTURE ARRAYS WITH STRUCTURALLY CONTROLLED MATERIAL COMPOSITIONS

Introduction

Hierarchical nanopatterns display attractive properties arising out of multiple length scale structuring and added functionalities. Lotus leaves [156], butterflies wings [157], moths eye [158] and numerous other biological surfaces display special properties traceable to their hierarchically nanostructured surfaces. Hierarchy allows one to add multiple functionality one on top of another thus making possible, a precise control over the extent of functionality there is of each type. Ordered multi-level hierarchies have been realized through fabrication employing colloids [159], supramolecules [159, 160] or lithography [161, 162] but those presenting beyond 2nd level of hierarchy in the sub-micron or nanoscale are rarely encountered. We demonstrate here, an entirely self-assembly driven approach to two-dimensional arrays of binary or ternary superstructures of ABx and $(ACy)(BCz)x$ type, where $C \in B, A$ and A, B, C are nanostructures having dimensions < 100 nm. Each level of hierarchy in the superstructure can be engineered to present a different material, and its degrees of hierarchy (x, y or z) tuned to control compositions. The assemblies present a branched hierarchy in binary super clusters, and mixture of branched and nested hierarchies in ternary superstructures. The degree of branching (x) in binary assemblies is controlled by tuning separation between features in the parent hierarchy (A) in relation to the size of branched component (B). The degree of nesting (y, z) in the ternary superclusters is determined by the size of the nested component (C) in relation to that of parent components, A and B respectively. Generic design principles that we extract from the investigation of these assemblies can be extended to design new multi-functional systems with desired geometric attributes. Such entirely self

assembly derived hybrid material hierarchies with rich flexibility in choice of material type and stoichiometries, is unprecedented, and has high implications for photonic, optoelectronic, and bio-device applications [163, 164, 165, 166, 167, 168, 169, 170].

SECTION 4.1

HIERARCHICALLY SELF-ASSEMBLED GOLD NANOPARTICLE SUPERCLUSTER ARRAYS

4.1.1. Introduction

By virtue of employing a combination of hard and soft spheres for assembly formation, the superstructures differ from 3D nanoparticle superlattices, e.g. binary (BNSL) [171, 172, 173, 174, 175] or ternary super lattices (TNSL) [176, 177] or 2D lattices, e.g. using sub-micron spheres [178] or confined adsorption of micro [179] or nanospheres [180], in terms of the driving force behind self-assembly of components, and in the realizable configurations. These assemblies predominantly rely on the space filling factors of close-packed spheres, or directed adsorption to pre-existing templates as driving forces for assembly formation. Both these approaches are generic, and are successful in yielding hierarchical assemblies, except when encountered with strenuous demands of scalability, and ease of controlling relative arrangements of nanoscale components. We employ combination of capillary force driven assembly of soft spheres at first two levels of hierarchy, and directed attachment of hard nanospheres at the third level. The use of non-close packed, and collapsible soft polymeric spheres at the first two levels is the key to attaining the superstructure arrays with high structural tunability, and ease of scaling up to arbitrarily large areas.

4.1.2. Experimental

4.1.2.1. Materials

Polystyrene-*block*-poly(vinylpyridine) copolymers used for the work were obtained from Polymer Source Inc. (Montreal, Canada) and used without further purification Gold citrate trihydrate from Sigma-Aldrich Pte Ltd. was used as obtained. 2-propanol,

m-xylene, acetone were obtained as anhydrous solvents with purity > 99% from Sigma-Aldrich Pte Ltd. Prime grade silicon wafers were obtained from Silicon Valley Microelectronics (Santa Clara, CA, USA). Point Probe Plus silicon tips for tapping mode imaging measurements with atomic force microscopy were bought from Nanosensors (Neuchatel, Switzerland).

4.1.2.2. Methods

Fabrication of *A*-arrays

i) The silicon substrates were diced and cleaned by ultrasonicating in acetone followed by 2-propanol and finally exposed to UV/Ozone (UV-1, SAMCO Inc., Kyoto, Japan) for 10 minutes.

ii) Reverse micelle from 0.5% (w/w) solution of the PS-*b*-PVP, 380 kDa, f_{PS}~0.5, PDI 1.1, from *m*-xylene was spin coated (CEE model 100CB spinner, Brewer Science Inc., MO, USA) at 1000, 2000, 4000 or 6000 rpm on Si substrates at high (RH~55%) or low humidity (RH~10%). For controlling humidity during the spin-coating step, the spin-coater was placed within a custom-built chamber from Electro-Tech systems, Inc. (ETS, PA, USA) that was designed to offer a closed-feedback humidity control in an operating range of RH- 1-100%.

iii) For the preparation of '*A*' arrays consisting of gold features, the spin coated substrates were immersed in aqueous solution of 5 mg/ml of $HAuCl_4$ for 15 min, rinsed with DI water and blown dry using nitrogen. After gold incorporation into the micelle core, the polymer template was then completely removed by subjecting to oxygen plasma reactive ion etching (20 sccm oxygen, 65 mTorr, 30 W for 15 min) to result in Au nanoparticle arrays.

iv) AFM (Nanoscope IV Multimode AFM, Veeco Instruments Inc., NY, USA) and FESEM (JEOL 6700F, Tokyo, Japan) were used to characterize the nanopatterns during each step of fabrication.

Fabrication of *ABx* arrays

The second level hierarchy was obtained by spin-coating reverse micelles of PS-*b*-P2VP (114KDa, *fps*~0.5) (B) on to pre-existing (A) arrays of gold at 3000 rpm for 45 s to result in $Au(PS\text{-}b\text{-}P2VP)_x$ assemblies (Figure. 4.1.1)

Fabrication of *(ACy)(BCz)x* arrays

i) The ternary superstructure arrays of type $(Au.Au_y)(\text{PS-}b\text{-P2VP}.Au_z)_x$ (Figure 4.1.5) with A=Gold, B=polymer, C=citrate-Au nanoparticles, are obtained by immersing $Au(PS\text{-}b\text{-}P2VP)_x$ into a citrate stabilized gold nanoparticle suspension for duration of 2h.

ii) The citrate stabilized colloidal Au nanoparticle are produced using the method described elsewhere [181].

4.1.3. Results and discussion

A schematic illustration of the fabrication of ***A, ABx*** and ***(ACy)(BCz)x*** hierarchical nanoarrays is shown in Figure 4.1.1. In this Section 4.1., hierarchically self assembled gold nanoparticle supercluster arrays where '*A*' and '*C*' are gold are discussed. The hybrid hierarchical supercluster arrays consisting of TiO_2 and/or ZnO in their hierarchies will be discussed in Section 4.2

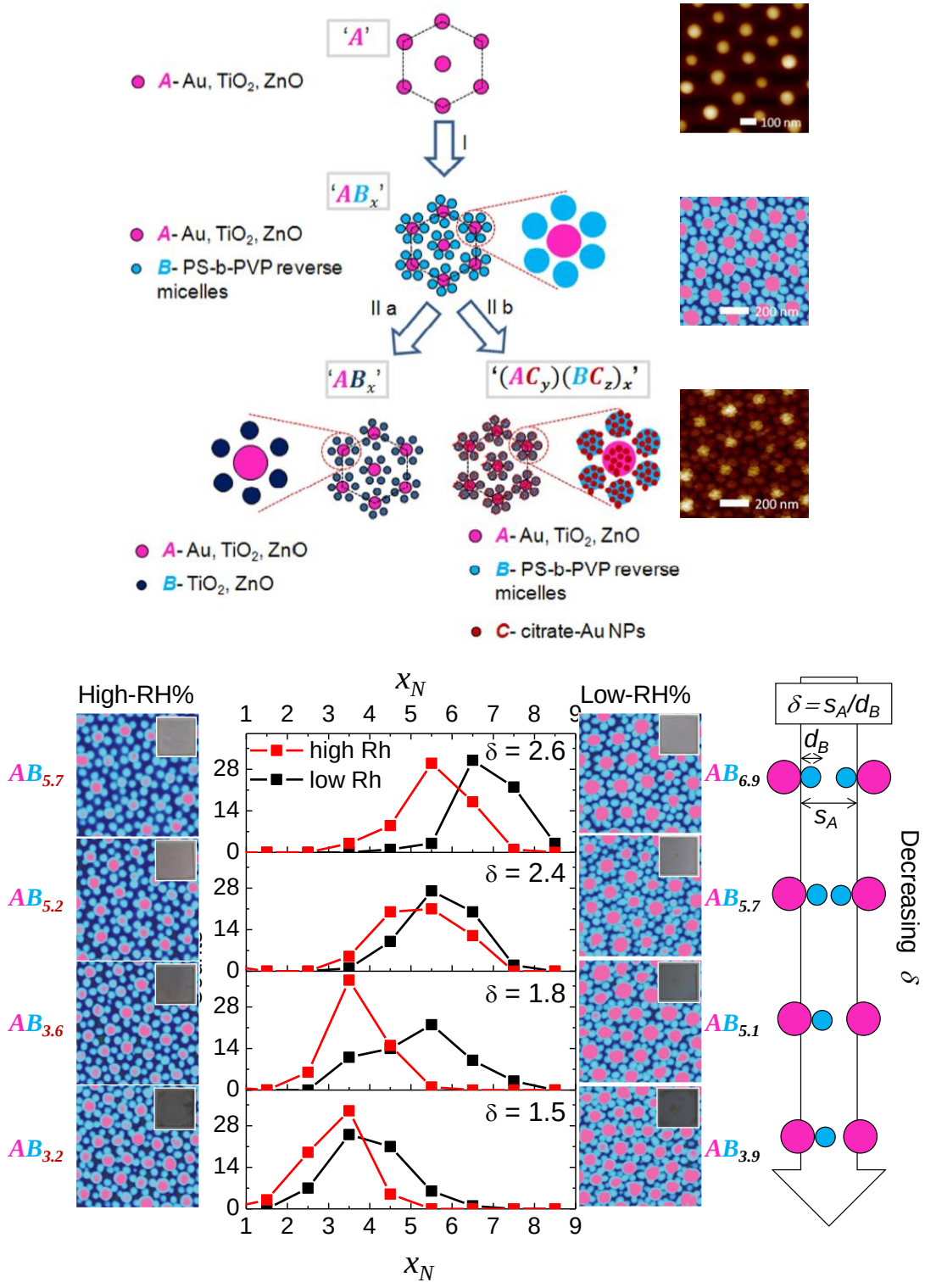


Figure 4.1.1 Schematic illustration of the formation of ***A, ABx, (ACy)(BCz)x*** arrays and the respective AFM images as explained in 4.1.2.2. Methods. Tapping mode AFM images of binary superstructures of ABx type, with x determined by the ratio (δ) of separation (s_A) between A to the diameter of B(d_B). The histogram of the number of 'B' (reverse micelles) present around each 'A' (Au nanoparticle) shows systematic control in x with variation in δ. Insets show Si chips with 1cm x 1cm dimensions, with uniformly coated ABx superstructure arrays.

The first level or the highest ranking hierarchy (A) consists of inorganic metal or semiconductor nanoparticle array achieved by in-situ synthesis within self-organized copolymer reverse micelles on surface [182, 183]. The reverse micelles are soft nanospheres that form non-close packed arrays on surface with opportunities for systematically expandable pitch, simply by varying spin-coating speeds [182, 183, 184]. The second level is attained by exploiting features in the first level as nodes to drive self-organization of diblock copolymer reverse micelles (B) of smaller dimensions, through capillary forces. The separation between 'A' features is of the order of the size of 'B' and thus provides confining influence and determines the number of the 'B' features organized around each A. The ratio (δ) of separation (s_A) between 'A' features to the diameter (d_B) of 'B' allows fine control over the degree of branching 'x' and also governs the transition from branching to overlapping hierarchies in the resulting ABx superclusters. The composite functionality of 'B' permits its further independent translation into other metal or semiconductor materials of interest, or towards adding a third level of hierarchy. The third level of hierarchy is attained through attachment of smaller nanoparticles to the surface of A and B through electrostatic interactions. This results in a nested hierarchy with a degree of nesting, y or z in $(AC_y)(BC_z)_x$ determined by the surface area of 'A' or 'B' in relation to the size of 'C'.

Binary superstructures of $Au(PS\text{-}b\text{-}P2VP)x$ with $3.2 < x < 6.9$, are represented in Figure 4.1.1 by their tapping mode AFM images, and the histograms in x derived thereof. The Au nanoarrays that constitute the first level hierarchy are realized through in-situ reduction of $HAuCl_4$ (immersed in 5 mg/ml of $HAuCl_4$ for 15 min,

rinsed with DI water and blown dry using nitrogen) within P2VP core of self-organized array of PS-*b*-P2VP (380 kDa, f_{PS}~0.5) reverse micelles [185]. The polymer is completely removed by subjecting to oxygen plasma exposure (20 sccm oxygen 65mTorr 30W for 15 min) to result in Au nanoparticle arrays presenting feature heights of 50 $\pm$5 nm. The periodicity of the array is systematically varied between 150-225 nm by varying the spin-coating speeds (1000, 2000, 4000 and 6000 rpm spin speeds offered pitch of 154 nm, 167 nm, 200 nm and 222 nm respectively) of the PS-*b*-P2VP reverse micelles. The fine-tunability in pitch of the arrays systematically also translates into an ability to fine-tune edge to edge separations (S_A) to 85, 103, 134 and 144 nm respectively [180, 184]. The second level hierarchy consist of reverse micelles of PS-*b*-P2VP (114 kDa, *fps*~0.5) coated on to pre-existing Au particle arrays.

4.1.3.1. Influence of 'δ' on 'x'

The reverse micelles used in the second step are of smaller size in relation to those used to generate the first level of hierarchy. These micelles organize themselves along the periphery of the Au nanoparticle features by capillary forces yielding well-defined binary superstructures with hierarchy determined by the ratio (δ) of the separation of '*A'* to diameter of '*B'*. The degree of hierarchy, 'x' was taken to be the mean value of the histogram (determined through a Gaussian fit to the histogram) in the number of reverse micelle features around each Au nanoparticle ('x_N') as estimated from AFM. As the separation between the Au features ('A') decreases, there is an increasing overlap between adjacent superstructures, thereby resulting in an overlapping hierarchy. The value of 'x' in the overlapping superstructures was obtained by

assigning each reverse micelle ('B') feature with an occupancy of ½ or ⅓ depending on whether it is shared by 2 or 3 'A' features. This avoids double counting of the features, and presents the real scenario of the density in 'B' features in relation to that of 'A'. Thus, the value of 'x' systematically decreases with an increase in overlap between the adjacent superstructures. In the dependence of x on δ, the branching hierarchy is observed for values of δ above 2, and overlapping hierarchy for values below. This is expected, as illustrated in Figure 4.1.2, as δ = 2 represent a value for separation between the 'A' features that is twice the diameter of 'B', and thus for $\delta < 2$ there is insufficient space to support independent superstructures. Even at the lowest feature separations, the maximum sharing is observed to be only 80%, due to presence of some 'B' features that are unshared. The unshared 'B' features are the consequence of greater distance between some 'A' features compared to others, as a result of standard deviation in separations.

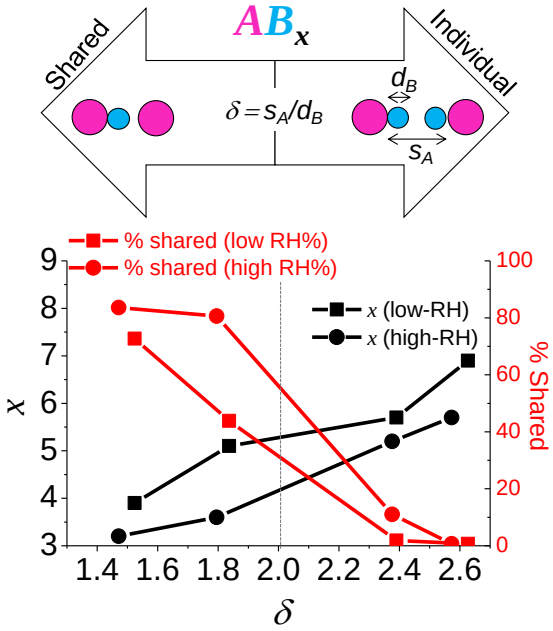


Figure 4.1.2 Dependence of x with δ and the existence of the branched and overlapping hierarchy above and below $\delta = 2$ respectively.

$$\%\ shared = \frac{Occupancy\ of\ shared\ features}{Total\ occupancy\ per\ supercluster} \times 100 = \left(\frac{\sum_{i=\frac{1}{2},\frac{1}{3}} (N_i \times i)}{\sum_{i=1,\frac{1}{2},\frac{1}{3}} (N_i \times i)} \right) \times 100 \quad \ldots\ldots (1)$$

where $i = \frac{1}{Number\ of\ times\ the\ feature\ is\ shared}$; The numbers are weighted by the factor 'i' that signifies the extent of sharing, or the contribution of a given feature to a specific super structure.

4.1.3.2. Influence of relative humidity on the micelle organization

In addition to the influence of δ on x, there is an additional influence noticed due to the relative humidity of the medium. The values of x were higher when the reverse micelles ('B') were coated on to the Au nanoarrays ('A') at a relative humidity (RH) of 10% as compared to ambient value of 55%. It is important to note that the influence due to relative humidity is felt only at the time of film formation, as a post-exposure of the coatings has no effect on the resulting assemblies. The influence is difficult to predict, given that the coatings are deposited from an apolar medium, and thus, presence of moisture in the environment is not expected to influence the evaporation rate, as it would for aqueous counterparts. There are, however, other ways in which the humidity can influence the quantity of material deposited on surface; for example, the quantity of adsorbed layers of water on a surface significantly increases with increase in relative humidity [186, 187, 188, 189]. Such ad layers can potentially influence the dynamics of the spin-coating process, especially the outflow rates that dominate the initial decrease in volume of the solution film [190]. Related instances of the influence of humidity are seen as an increase in volume of meniscus formed at the interface of a nanoscale probe and surface, by capillary condensation [191];

increase in transport of oil molecules through such meniscus and a drastic decrease in the nanoscopic sliding friction experienced by the tip on rough and hydrophilic surfaces, at a higher humidity [192]. Spin-coating on topographically patterned substrates exhibiting greater wettability have shown to result in a slightly higher thickness of spin-coated polymer film, as compared to partially wetting surfaces [193].

To gain better insight into the potential influence of relative humidity on the out-flow rates during spin coating, a control experiment was set up to determine sliding contact angles of a mineral oil on the substrates consisting of the Au nanoparticle arrays (the 1st level of hierarchy, or the A features. The sliding angles reflect the adhesive forces between the droplet and the surface, which in turn has indirect influence over the out-flow rates during spin coating. A mineral oil (Vaccubrand B-oil) with low vapor pressure was chosen for the experiment to ensure no evolution in droplet size occurs during measurements. The surface tension of the oil (31.2 +/- 0.03 mN/m), measured using Wilhelmy ring method) is close to that of *m*-xylene (28.9 mN/m) [194], thus allowing an extrapolation of its behavior to that of *m*-xylene solutions of reverse micelles. A tiny quantity of the mineral oil (~ 15 μL) was pipetted on a horizontally placed chip, and the chip slowly tilted (custom-designed set up) until the oil rolls off. A sliding angle of 22.9 (+/-2^{o}) and 30.2 (+/- 2^{o}) was observed for high (~55%) and low (< 10%) RH respectively, ascertaining a greater ease of flow at high RH. This was found to be true also for bare Si chips, yielding 24.1(+/-2^{o}) and 29.0 (+/- 2^{o}) at high and low RH respectively, albeit with a slightly lower contrast between the roll-off angles as compared with the case of Au nanoparticle arrays. The greater ease of

roll off of the oil droplet at a high RH shows a lower adhesion and supports arguments on water ad layers acting as a lubricating layer in facilitating greater outflow of the apolar solution during spin-coating. Additional control experiments were run to ascertain the densities of PS-*b*-P2VP reverse micelles (0.5 % w/w in *m*-xylene spin coated at 3000 rpm, the same as employed for ABx superstructure experiments) on bare Si substrates, at high and low RH (Figure 4.1.3). The arrays coated at RH < 10% show greater quantity of deposition, as manifested through a higher value for the density (154 +/- 9/μm^2) of the micelles as compared to high RH coatings (113 +/- 6/μm^2).

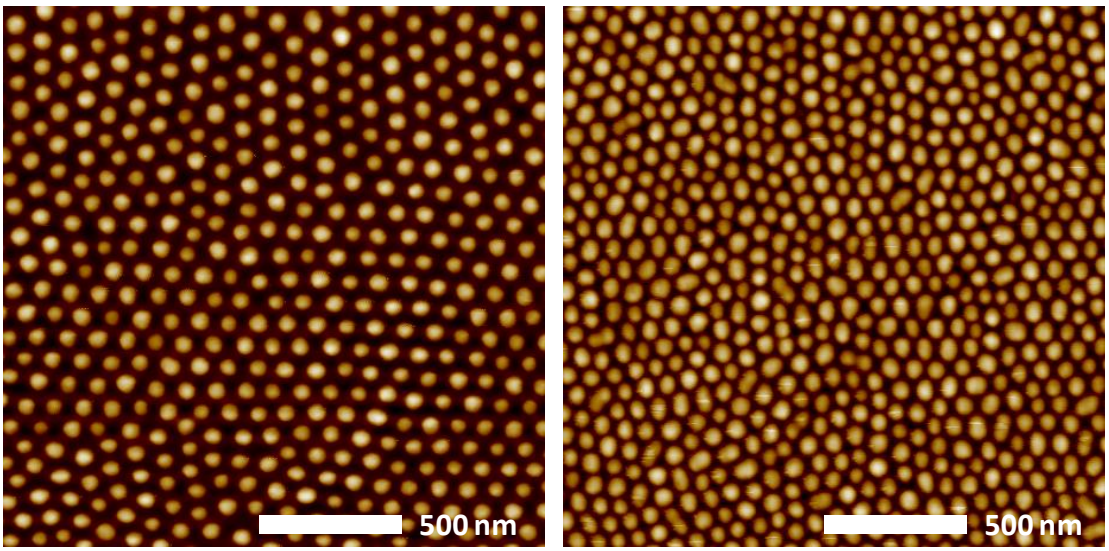


Figure 4.1.3 (left) high and (right) low humidity coatings of reverse micelle arrays of PS-*b*-P2VP, 114kDa, f_{PS}~0.5, used as '*B*' features, coated from 0.5% (w/w) *m*-xylene solutions, show a higher density at lower humidity.

We say 'quantity' rather than 'thickness' as in the case of reverse micelles, within the window of conditions we operate (for solution concentration of 0.5-1.0 % w/w and spin-coating speeds of 1000-6000 rpm), a change in polymer quantity on surface does not affect the vertical dimensions of the film, but manifest as a difference in feature densities on surface. Thus, our observation of the influence of humidity on the

thickness of the spin-coated film is generic, and not specific to reverse micelles used in the study. The control over humidity allows the process to be fine-tuned as well as facilitates maximization of the values for x, in the binary hierarchies.

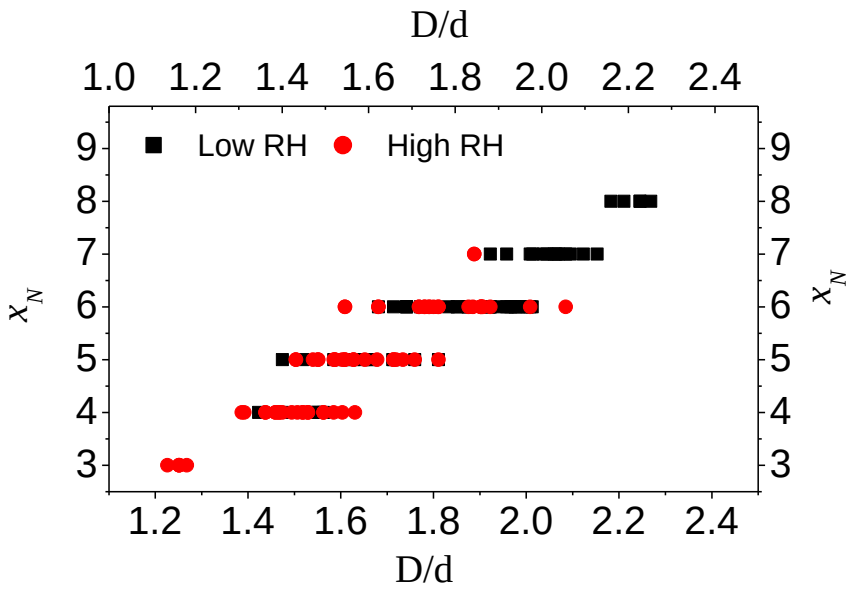
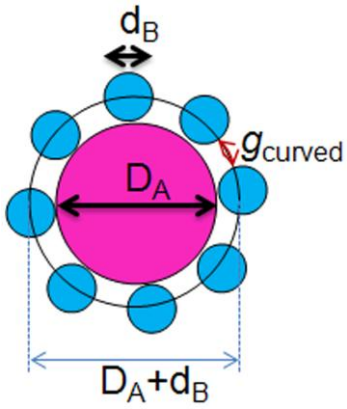


Figure 4.1.4 Plot of χ_N versus D_A/d_B for *Au(PS-b-P2VP)*$_{5.7}$ and *Au(PS-b-P2VP)*$_{6.9}$ binary superstructures.

Besides the dependence of x on δ, it is of interest to extend the understanding further to decipher its dependence on the feature size of 'A' in relation to that of 'B'. The AFM measurements show a standard deviation of 10% in the size of 'A' features which in turn contributes to a standard deviation in the degree of branching of 'B' features in resulting ABx super structures (Figure 4.1.1 histograms). Thus, by tabulating the degree of branching (x_N) against the ratio of diameters of 'B' to 'A' (d_B/D_A) for each of the individual super-structures appearing in the AFM image of a non-overlapping ABx hierarchy (e.g. $AB_{5.7}$ or $AB_{6.9}$), the dependence of $x_N$versus d_B/D_A can be deduced (Figure 4.1.4). The value of 'd_B' was taken to be the mean value of 65 nm for the diameter of micelles. x_N is taken to denote the degree of

branching for an individual superstructure, to differentiate it from x, which denotes mean value of the distribution in x_N. The comparison of x_N versus d_B/D_A obtained for $AB_{5.7}$ or $AB_{6.9}$ superstructures shows systematic increase of x_N with D, which is expected, based on the increasing peripheral space around 'A' features. However, a rather subtle and unexpected influence of D is noticed towards density of micelles (or how closely the micelles are packed) within the superstructure. This influence is best brought out through an estimation of feature separations (g_{curved}) of micelles within each superstructure using values for D, d and x_N obtained from AFM in the following equation derived from simple geometric considerations, as shown in schematic 4.1.1.



Scheme 4.1.1 Derivation of the value for g_{curved} from values of D and d, and using the equations 2, 3 with the model shown.

$$\pi(D_A + d_B) = x_N d_B + x_N g_{curved} \qquad \ldots\ldots (2)$$

$$g_{curved} = \frac{\pi(D_A + d_B) - x_N d_B}{x_N} \qquad \ldots\ldots (3)$$

$$g_{curved} = \frac{\pi(D + d) - x_N d}{x_N} \qquad \ldots\ldots (4)$$

A systematic increase in g_{curved} with d_B/D_A ratio for $AB_{6.9}$ superstructures of $3 < x_N < 8$ is shown in Figure 4.1.5. The plot of x_N versus D_A reveal that a specific value of x_N is exhibited by a range of D_A values.

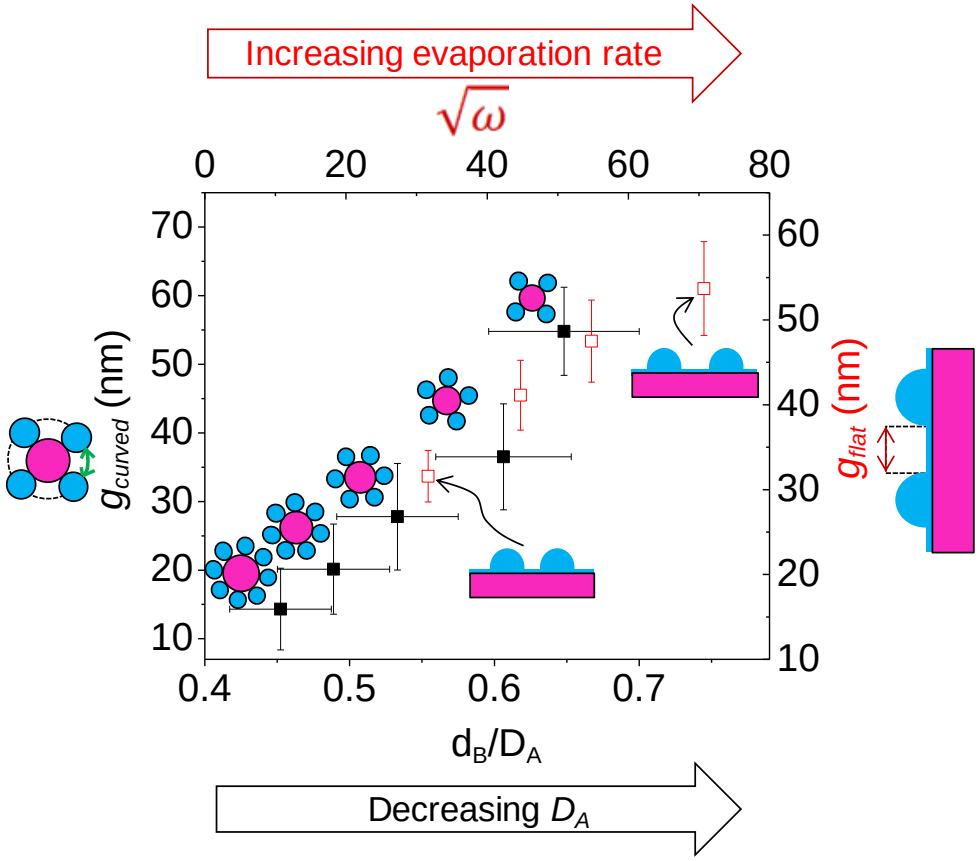


Figure 4.1.5 The systematic increase in g_{curved} with d_B/D_A ratio for $3 < x_N < 8$ in $AB_{6.9}$ superstructures is found to match the trend of increase in g_{flat} with an increase in evaporation rate (represented as $\sqrt{\omega}$, where, ω represents spin-coating speeds in rpm) on flat substrates. The x-axis errors shown for d_B/D_A include contribution due to co-existence in D_A values per x_N.

The x-error bars in Figure 4.1.5 take this range into account and in addition, they include errors due to tip convolution effects in determination of D_A and d_B. Although these error bars seem large (mainly due to coexistent D_A values per x_N), the trends noticed in the decrease in g_{curved} with decrease in d_B/D_A ratios are unmistakable. One way to account for this trend is by considering a greater meniscus volume of the

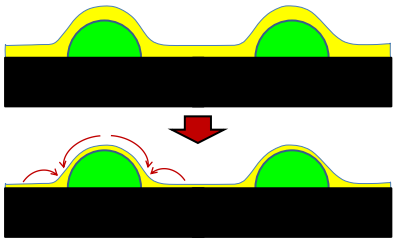
polymer solution associated with larger sized 'A' features, which as a consequence results in higher density of micelles at its periphery (Figure 4.1.5). However, our estimation of the equivalent volumes of the polymer solution that would carry as many micelles as x_N reveals ~164-437 attoliters for x_N values of 3-8.

Estimation of volume of the solution consisting of X_N micelles:

The hydrodynamic size ($2 \times Rh$) of PS-*b*-P2VP 114 kDa, f_{PS}~0.5 reverse micelles as measured using DLS was measured to be 104 nm. From the Rg/Rh ratio values commonly encountered for spherical micelles of ~0.75, Rg can be estimated to be ~39 nm [184, 195]. This can be taken as the dry state radius of the micelle. Assuming a density of 1.1 g/cc, the mass of a single micelle can be estimated to be 2.7×10^{-16} g. Given the concentration of the polymer in the solution employed is 0.005 g/mL, this would represent ~1.8×10^{13} micelles present per cm^3. This would equate to 1 micelle per 5.5×10^{-14} cm^3 (or, 5.5 attoliters (aL)) of solution, based on which the volume of the solution containing 3 - 8 micelles (corresponding to the values of x_N can be calculated to be ~164-437 aL). A minor deviation to this estimation is expected to arise based on the actual experimental value for Rg/Rh. Nevertheless, the estimation adequately serves to delineate the relative orders of magnitude for volume of the micelle solution consisting of x_N micelles in relation to that of the Au features. The mean volume of the '*A'* features can be estimated (approximated as hemisphere, as discerned by height and diameter values from AFM & SEM) as 0.09-0.48 aL.

The volumes (164-437 aL) are three orders of magnitude higher in comparison to that of the '*A'* features (0.09-0.48 aL for cases considered in Figure 4.1.5), and equates to

a solution films that are much thicker than the *A* features. Thus, we rule out meniscus volumes around the template as a contributor to the observed dependence of x_N on the d_B/D_A ratios. The onset of meniscus contribution is expected when the thickness of the drying film approaches the height of 'A' features [196]. By then the x_N values have already been decided by the system, thus requiring an alternative explanation to the above dependence. We expect this dependence to arise due to a higher rate of evaporation on smaller 'A' features due to their larger surface to volume ratio. The range of D values in Figure 4.1.5 represents an enhancement in surface to volume ratio of ~43% going from the largest to the smallest particles. During evaporation of solvent, the meniscus forces drive the micelles from both above and surrounding the 'A' features to its periphery.



Scheme 4.1.2 The dependence of the meniscus volume of *m*-xylene solution (in yellow) of PS-*b*-P2VP around the Au nanoparticle template on the template size is compared.

The periphery of larger features would experience relatively higher inflow of reverse micelles due to longer residence durations of the polymer solution resulting from a relatively lower evaporation rate. Such influence of the evaporation rate on the density of micelles on surface is known for flat substrates, where, micelle arrays formed at higher spin speeds (higher evaporation rates) result in lower feature densities. The data obtained from flat chips is overlaid in Figure 4.1.4, with the evaporation rate represented as square root of spin-coating speeds ($\sqrt{\omega}$) as known

from the theoretical treatment of spin-coating process [197, 198]. The similarity in trends for g_{curved} versus d_B/D_A with g_{flat} versus $\sqrt{\omega}$ strongly favors attributing the former dependence to the size dependent evaporation rate on A features. Establishing clarity on this influence allows evolution of rational design rules to tailor-make superstructures with desired g_{curved}, d_B, and D_A even if the 'A' features were to be fabricated through other means, e.g. nanoimprint lithography, or e-beam lithography.

4.1.4. Formation of ternary superclusters

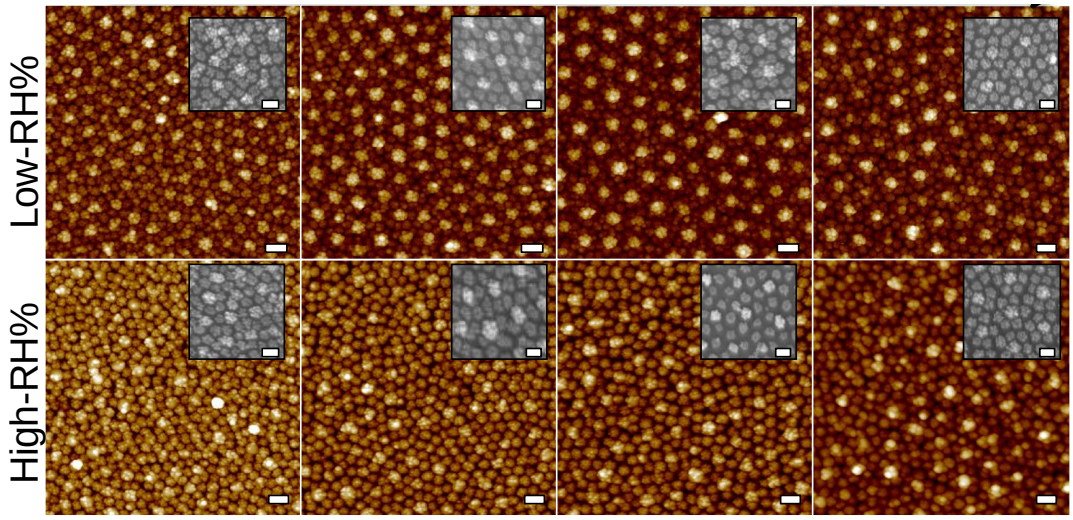


Figure 4.1.6 *(Au.Au$_y$)(PS-b-P2VP.Au$_z$)$_x$* at low and high RH, and increasing *x* from left to right, with Au nanoparticle arrays (*A*), PS-*b*-P2VP reverse micelles (*B*) and citrate-Au nanoparticles (*C*) adsorbed on '*A*' and '*B*' features. Scale bar indicates 100 nm.

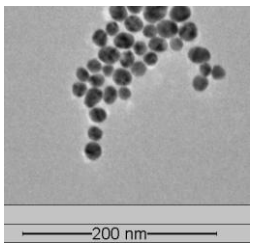


Figure 4.1.7 TEM of citrate stabilized colloidal Au NP

The ternary hierarchies of type $(ACy)(BCz)x$ (Figure 4.1.6) were realized upon immersion of the binary superstructures of ABx to an aqueous suspension of citrate-stabilized Au nanoparticles (C) of ~11.7 nm diameter (Figure 4.1.7). Since the 'B' features constitute PS-*b*-P2VP reverse micelles, the citrate-stabilized Au nanoparticles selectively attach to the surface of the 'B' features due to electrostatic attraction to result in Au nanoparticle clusters (BCz type) [180]. The size of these clusters (as defined by the number of nanoparticles adhering to each micelle) is determined by the surface area of the template feature, which we demonstrated in our earlier [180] study to be ~18 particles/cluster (thus, z ~ 18). In the present case, the citrate-Au nanoparticles were not only found to attach on the micelles, but also onto the central Au nanoparticle ('A' features). The latter is unexpected, and is likely a consequence of the presence of thin PS-*b*-P2VP brush layer [199] instantaneously on the surface of the A features, during the coating of the reverse micelle solution. When present, the PS-*b*-P2VP molecules would render the A features positively charge at the *p*H of 6.5 (corresponding to the citrate-Au nanoparticle suspension), and consequently direct attachment of negatively charged citrate-Au nanoparticles from solution, in a similar manner as the reverse micelles do. The number of citrate-Au nanoparticles adhering to the A features can be estimated [180] based on surface area of the A features to be 67 particles. However, the number of citrate-Au nanoparticles were observed to be far less in comparison, to be ~ 17 $\pm$ 4 particle per A feature (thus, y ~ 17) based on SEM measurement at high magnification. The significant fall in density of citrate-Au is likely due to the lower electrostatic attraction on the 'A' features, presumably due to a low density of PS-*b*-PVP molecules on its surface. An additional contribution is likely due to the repulsive forces from the citrate-Au particles on the neighboring micelle features, in excluding adsorption on the periphery of 'A' features. Under such

conditions, the number of citrate-Au attached to the 'A' features, although dictated by surface area, needs to be arrived at empirically. Based on the number of particles per 'A' feature, the surface coverage of citrate-Au nanoparticles equates to ~11%. If the 'A' features can be rendered strongly positive, e.g. by selective growth of PVP brushes, or deposition of thiol SAMs or use of polyelectrolyte multilayers, the density of citrate-Au features can be significantly increased to be close to the jamming limit of 54.7% [200].

4.1.5. Conclusions

The protocol to fabricate the hierarchically self assembled gold nanoparticle superclusters is relatively simple compared to other existing pattern producing techniques. Moreover, the entire process is driven by a directed layer-by-layer block copolymer self assembly process and so the complexity that can be achieved at every level of hierarchy is difficult to be achieved in any other known techniques. In addition, the introduction of block copolymer micelles at different levels of hierarchy allows tunability of the features and henceforth the overall orientation of the supercluster. Process variables such the relative humidity, block copolymer lengths and molecular weights remain key parameters to manipulate and arrive at the complex geometry that suits the researchers' requirements. Furthermore, the novelty of the protocol lies in the fact that, gold apart, different materials such as ZnO, TiO_2 at different levels of hierarchy can be patterned thereby giving rise to hybrid metal and/or metal oxide and/or polymer supercluster arrays. This is discussed in Section 4.2.

SECTION 4.2

HIERARCHICALLY SELF-ASSEMBLED HYBRID HETERO-SUPERCLUSTER ARRAYS

4.2.1. Introduction

Chapter 4, Section 4.1 dealt with the hierarchical nanopatterns consisting of entirely gold nanostructures. The statistical relationship between the different geometrical attributes of the features and the design rule to achieve a complex multilevel supercluster arrays were discussed. The generic design principles as discussed in Chapter 4.1 can readily be extended to design new multi-functional systems with desired geometric attributes. In this chapter, using the same directed self assembly in a hierarchical fashion, we demonstrate the possibility to realize hybrid material supercluster arrays by adding different functionalities at each level of hierarchy. Every level of hierarchy during the designing of superstructure assemblies can be engineered to present a different material with the ability to control their composition by tuning their degrees of hierarchy (x, y or z). As a prototype, we demonstrate here the fabrication of hybrid material supercluster arrays of type $Au(PS\text{-}b\text{-}P2VP)_x$, $TiO_2(PS\text{-}b\text{-}P2VP)_x$, $TiO_2(Au)_x$ and $Au(ZnO)_x$. However, owing to the advantage offered by the polymeric features for pattern transfer to different materials, the protocol can readily be extended to pattern any metal and/or metal oxide and/or polymer combinations irrespective of the material used in the prototypes. Such advantages in determining the choice of material, tunability and liberty to position different materials in different hierarchy are difficult to realize in other state-of-the-art technologies due to absence of a well designed directed self assembly technique as reported here.

4.2.2 Experimental

4.2.2.1. Materials

Polystyrene-*block*-poly(2-vinylpyridine) copolymers used for the work were obtained from Polymer Source Inc. (Montreal, Canada) and used without further purification Gold citrate trihydrate and zinc chloride from Sigma-Aldrich Pte Ltd. and were used as obtained. 2-propanol, *m*-xylene, acetone were obtained as anhydrous solvents with purity > 99% from Sigma-Aldrich Pte Ltd. Prime grade silicon wafers were obtained from Silicon Valley Microelectronics (Santa Clara, CA, USA). Point Probe Plus silicon tips for tapping mode imaging measurements with atomic force microscopy were bought from Nanosensors (Neuchatel, Switzerland).

4.2.2.2. Methods

Fabrication of *A*-arrays

i) The silicon substrate preparation and the fabrication of '*A'* arrays consisting of gold features were performed as mentioned in Section 4.1.

ii) Reverse micelle from 0.5% (w/w) solution of the PS-*b*-PVP, 380 kDa, f_{PS}~0.5, PDI 1.1, from *m*-xylene was spin coated (CEE model 100CB spinner, Brewer Science Inc., MO, USA) at 1000, 2000, 4000 or 6000 rpm on Si substrates at high (RH~55%) or low humidity (RH<10%). For controlling humidity during the spin-coating step, the spin-coater was placed within a custom-built chamber from Electro-Tech systems, Inc. (ETS, PA, USA) that was designed to offer a closed-feedback humidity control in an operating range of RH- 1-100%.

iii) For preparation of 'A' features consisting of TiO_2 nanoarrays, $TiCl_4$ and H_2O (de-ionized water) were used as volatile precursors and introduced into the atomic layer deposition (home-built ALD equipment) chamber in pulses (100 cycles). N_2 gas was used both as a carrier gas and purge gas. The number of cycles precisely determines the amount of precursor impregnated into the hydrophilic PVP core. In both the cases, after material incorporation into the micelle core, the polymer template was then completely removed by subjecting to oxygen plasma reactive ion etching (20 sccm oxygen 65mTorr 30W for 15 min) to result in either Au nanoparticle or TiO_2 arrays.

iv) AFM (Nanoscope IV Multimode AFM, Veeco Instruments Inc., NY, USA) and FESEM (JEOL 6700F, Tokyo, Japan) were used to characterize the nanopatterns during each step of fabrication.

Fabrication of *ABx* arrays (Figure 4.2.1)

i) The second level hierarchy was obtained by spin-coating reverse micelles of PS-*b*-P2VP (114 kDa, *fps*~0.5) (B) on to pre-existing 'A' arrays (with either Au or TiO_2 arrays) at 3000 rpm for 45 s to result in $Au(PS\text{-}b\text{-}P2VP)_x$, $TiO_2(PS\text{-}b\text{-}P2VP)_x$ hybrid assemblies.

ii) The hybrid superclusters arrays composing of TiO_2 and Au of type $TiO_2(Au)_x$ were obtained by incubating $TiO_2(PS\text{-}b\text{-}P2VP)_x$ into aqueous solution of 5 mg/ml of $HAuCl_4$ for 15 min, rinsed with DI water and blown dry using nitrogen followed by exposure to oxygen plasma RIE as before to remove the polymer and formation of the Au particles surrounding the TiO_2 features present in the 1st level hierarchy.

iii) The hybrid arrays of type $Au(ZnO)_x$ were prepared by incubating $Au(PS\text{-}b\text{-}P2VP)_x$ arrays into a solution of 1M zinc chloride in water for 15 min, rinsed and blown dry using nitrogen, followed by exposure to oxygen plasma.

Fabrication of *(ACy)(BCz)x* arrays

i) Earlier in Section 4.1., ternary superstructure arrays of type $(Au.Au_y)(\text{PS-}b\text{-P2VP}.Au_z)_x$ with A=Gold, B=polymer, C=citrate-Au nanoparticles obtained by immersing $Au(PS\text{-}b\text{-}P2VP)_x$ into a citrate stabilized gold nanoparticle suspension for duration of 2h were described. Similarly, $(TiO_2.Au_y)(\text{PS-}b\text{-P2VP}.Au_z)_x$ (Figure 4.2.3) with A=TiO_2, B=polymer, C= citrate-Au nanoparticles were obtained by incubating $TiO_2(PS\text{-}b\text{-}P2VP)_x$ into suspension of citrate-Au nanoparticles for duration of 2h.

ii) The citrate stabilized colloidal Au nanoparticle are produced using the method described elsewhere [181]. Briefly, in a 100 mL round-bottom flask fitted with a condenser, 60 mL of 1 mM $HAuCl_4$ in water was allowed to boil with constant stirring. 12 mL of 38.8 mM sodium citrate was added to the boiling solution. This resulted in change in the color of the solution to wine red. The solution was allowed to boil under constant stirring for 15 more minutes before they were cooled down to room temperature.

4.2.3. Results and discussion

The results establish separations between features in the first level as a convenient handle to tune the stoichiometries of the superstructures, and draw insights on influence on density of 'B' features on size of 'A', and influence due to relative

humidity. The ability to extend the understanding drawn from these results to realize ABx arrays of different material types is presented in Figure 4.2.1. The results convincingly support the versatility of the approach in yielding patterns of desired material combinations with stoichiometries that can be predicted before-hand. Since both the first and the second levels of hierarchy employ reverse micelles, the attainable combination for 'A' and 'B' are fairly large, as solution-phase as well as vapor-phase precursors can be used to synthesis materials within their functional core of the reverse micelles.

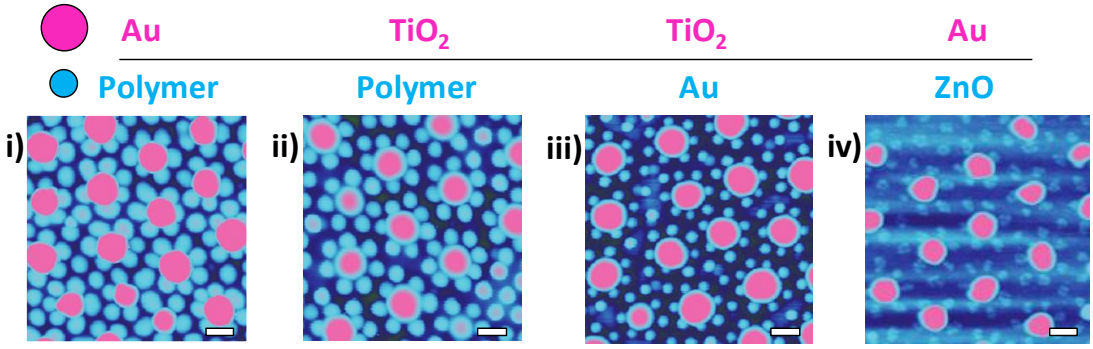


Figure 4.2.1 Hetero material hybrid superstructures of *ABx* type across a rich variety of *'A'* or *'B'* type materials can be readily achieved. Some prototypes are (i) $Au(PS\text{-}b\text{-}P2VP)_{6.9}$, (ii) $TiO_2(PS\text{-}b\text{-}P2VP)_{6.9}$, (iii) $TiO_2(Au)_{5.7}$, and (iv) $Au(ZnO)_{5.7}$ respectively.

The generality in attainment of ternary superstructures is seen from the similar arrangement obtained even when TiO_2 NPs were employed as the *'A'* features (Figure 4.2.3), thus precluding any chemical specificity of the process to Au as material. When desired, the polymeric template can be removed to yield superstructures consisting of entirely gold (Figure 4.2.2) or semiconductor-gold combinations.

As shown in Figure 4.2.2, the supercluster arrays consisting of entirely gold

nanoparticles show the significance in the arrangement of the patterns owing to the coatings done at different relative humidities. The influence of relative humidity over the self assembly of reverse micelles during the second hierarchy is dealt in depth in Section 4.1 under 4.1.3.2. Influence of relative humidity on the micelle organization. In addition, as we proceed from left to right, it could be observed that the increase in periodicity (spin speeds of 1000, 2000, 4000 and 6000 rpm) between the features in the first hierarchy determines the number of '*B'* features that can be accommodated in the second hierarchy. The influence of the separation between the features over the nature of hierarchy (branched or overlapping hierarchical assemblies) has been described in depth in Section 4.1.

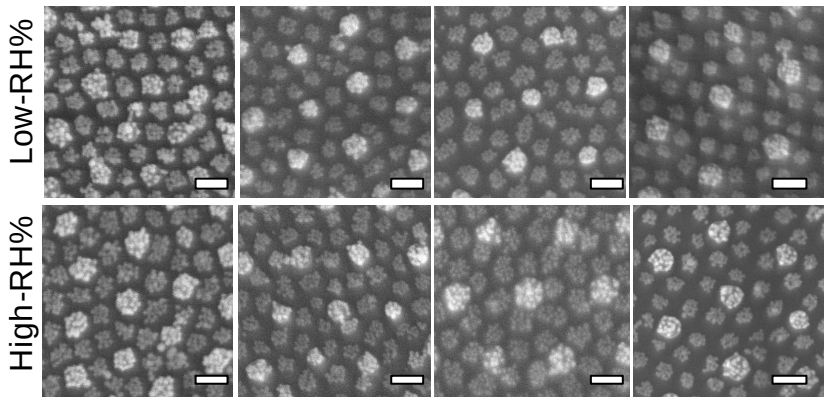


Figure 4.2.2 FESEM images of *(ACy)(Cz)x* (where *A* and *C* are gold features) formed upon removal of '*B*' (reverse micelle) features from *(ACy)(BCz)x* superstructures

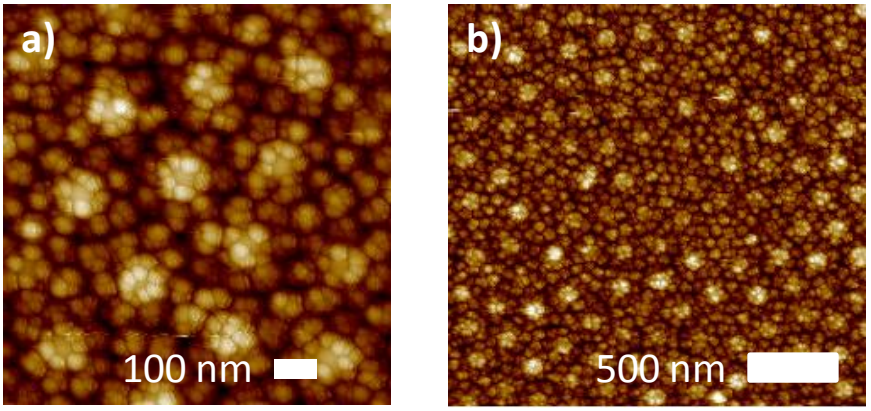


Figure 4.2.3 Left: *(ACy)(BCz)x* with TiO_2 nanoparticle arrays *'A',* PS-*b*-P2VP reverse micelles '*B'* and smaller Au NPs *'C'* adsorbed on to both *A* and *B* features from solution phase. Right: a) on a macroscopic scale.

4.2.4. Conclusions

The approach can be readily perceived as carrying fewer restrictions on the attainable material combinations by exploiting the choices available at each step of the hierarchy. The ability to pattern transfer the polymeric spheres into desired functional materials enable further independent ramifications in the nanostructures attainable, thus contributing to the hybrid 'hetero' material supercluster arrays. On a more significant note, PS-*b*-PVP reverse micelles can even be replaced with polystyrene-*b*-poly(acrylic acid) reverse micelles to produce patterns of Cu and Fe in a hierarchical arrangement, thereby offering increased benefits in terms of arriving at different magnetic material and polymer combinations. It is therefore clear that the approach draws its benefits from the usefulness of the assemblies in offering a high control over the lateral resolutions and composition attainable by tuning the geometrical attributes and interactions between the nanofeatures which can further be exploited in areas such as plasmon-plasmon, plasmon-exciton phenomena. The realization of the assemblies on macroscopic substrate areas will enable probing such interactions using less demanding techniques with macroscopic analysis footprints.

CHAPTER 5

APPLICATIONS OF sub-100 nm METAL OXIDE (ZINC OXIDE) AND METAL (GOLD) NANOPATTERNS

Introduction

Flash memory devices have been facing an ever increasing demand for high storage capacity, low operating voltages, high memory retention, and lowering costs for device fabrication. The scaling of flash memory devices dimensions down to the sub-30 nm range has led to aggressive scaling of the tunneling oxide from the existing thickness of 6-7 nm to as thin as 3-4 nm [33]. As devices continue to shrink, the conventional polysilicon floating gate is being replaced by an alternate charge storage medium, which uses discrete charge storage centers to store charge carriers [86]. Such discrete charge storage centers are realized in the form of well-isolated semiconductor [40] or metal [201] nanocrystals in nanocrystal flash memories, or discrete charge trap levels of a semiconductor thin film in charge trap flash (CTF) memories. The nanocrystal flash memories that store charge carriers within spatially isolated nanocrystals benefit from excellent charge retention due to reduced lateral charge conduction and the reduced impact of stress induced leakage current (SILC) [37]. On the other hand, the CTF memories benefit from an abundance of discrete trap levels that translates into high charge storage capacity. The discrete ZnO nano disc arrays embodies the strengths of both nanocrystal as well as CTF memories thus providing high charge storage capacity as well as good charge retention.

The state of the art CTF memory which is made up of a polysilicon-oxide-nitride-oxide-silicon (SONOS) stack relies on the discrete nitride levels of the silicon nitride (Si_3N_4) thin film [35] to store charge carriers. However, a low dielectric constant of 7.5 [202] together with the small conduction band offset (1.05 eV) of Si_3N_4 with SiO_2

[202] and the presence of shallow trap levels dictate the inevitable need for replacement of Si_3N_4 with new materials. A promising candidate that embodies characteristics to counter the above-mentioned issues with Si_3N_4 is ZnO. ZnO possesses a rich density of discrete trap levels due to defects such as oxygen vacancies and zinc interstitials [147] rendering it an excellent material for storing charge carriers [203].

On the contrary, nanocrystal-based memories offer multi-bit storage capability, deep trap states and with the process flexibility to progressively scale down device dimensions according to the needs of the silicon industry as per the International technology roadmap for semiconductors (ITRS) [32, 33, 204]. Fabrication of metal nanocrystal (NC) based non-volatile memories (NVM) has become increasingly important and is preferred over their semiconductor counterparts [86], conventional floating gate devices [205] or the SONOS devices [18, 206] as it offers numerous advantages in terms of higher density of states, better size tunability and scalability to optimize device characteristics [207, 208]. Moreover, metal NC based memory architectures are attractive due to enhanced retention due to deep trap levels and isolated features, ability to cope with the demanding scaling issues, multi-bit storage capability etc. The Au nanoparticle supercluster arrays (Section 4.1) based metal nanocrystal flash memory device throws light on enhancing the retention capabilities of the devices through charge multiplication by increasing the metal crystal arrangement in a hierarchical fashion on Si surface.

SECTION 5.1

APPLICATIONS OF sub-100 nm METAL OXIDE (ZINC OXIDE) NANOARRAYS

5.1.1. Introduction

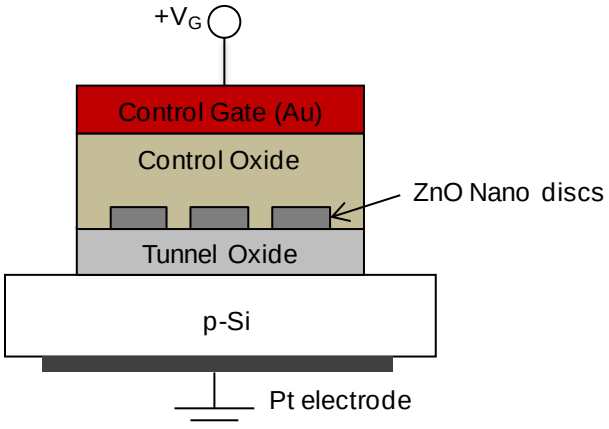
ZnO possesses a rich density of discrete trap levels due to defects such as oxygen vacancies and zinc interstitials [147] making it an excellent material for storing charge carriers [203]. In an earlier study investigating the electrical characteristics of ZnO nanocrystals embedded in a polyimide (PI) composite [151] (30nmC60/PI-ZnO/30nmC60) for non-volatile memory applications, a V_{FB} shift of 5.8 V at 20 V programming was reported [2]. A similar study using sputtered ZnO film (200nmMSQ/50nmZnO/120nmMSQ stack) reported memory window of 6 V at 10 V programming [209]. The charge trap densities for these studies were estimated to be 2.22 x 10^{18} cm^{-3} and 2.89 x 10^{16} cm^{-3}, respectively. ZnO has a high dielectric constant of 9.2-12.6 depending on the method of deposition [210]. The higher dielectric constant of ZnO compared to Si_3N_4 increases the equivalent oxide thickness of the charge trapping layer, allowing a thicker ZnO layer to be deposited without compromising on operation speeds. ZnO exhibits a large conduction band offset of 3.2 eV with SiO_2 or Al_2O_3 [211], which is comparable to that of polysilicon (3.15 eV) [212] used in conventional floating gate flash memory devices. This bestows superior charge retention properties on memory devices consisting of ZnO thin films as the charge storage layer.

The production of sub-10 nm NAND flash memory devices has been projected to launch in the year 2021 [33]. Since the use of optical lithography coupled with immersion lithography at sub-40 nm scale increases process time and production cost [18], NIL as well as directed self-assembly using block copolymers have been proposed as alternatives with lower cost and high throughput. In this Chapter, we

report the use of NIL in combination with block copolymer self-assembly to produce ZnO patterns with spatial resolutions below 100 nm to be used as charge storage centers in NVM devices. These ZnO arrays show high charge trap density of 2.3 x 10^{18} cm^{-3} at a low operating voltage of 10 V. This charge trap density is comparable to silicon nanocrystal memories, which demonstrate charge trap densities also of the order of 10^{18} cm^{-3} [40]. The introduction of well-isolated ZnO nano discs as charge storage centers is found to demonstrate good charge retention.

5.1.2. ZnO nanodisc array based MOS capacitor

As a demonstration of the application of NIL-derived ZnO nanodiscs, the charge storage characteristics of the ZnO nanodisc arrays were investigated by incorporating them within a metal-oxide-semiconductor (MOS) capacitor device (Scheme 5.1.1) on a p-type silicon substrate.



Scheme 5.1.1 MOS capacitor test structure incorporating ZnO nanodisc arrays as charge storage centers to investigate charge storage characteristics.

A 50 nm thick silicon dioxide was deposited by RF sputtering to act as the control oxide dielectric. Due to the isotropic nature of deposition by sputtering, the SiO_2 film completely covered the ZnO nano discs. The substrate was annealed before and after

deposition of the control oxide. Au contact electrodes of 0.03 cm diameter and spaced 1 mm apart were then deposited through a metal stencil mask. The electrode deposition was carried out by line of sight deposition of gold using an electron beam evaporator. A Pt back electrode was sputtered on the backside of the silicon substrate after removing the oxide using sandpaper. The Pt/p-Si/SiO_2/ZnO nanodiscs/SiO_2/Au (electrode) sandwich structure was used to investigate the charge storage characteristics.

5.1.2.1. Current density and Capacitance-Voltage measurements

Capacitance-Voltage (C-V) measurements (Figure 5.1.1.) were performed at 100 kHz frequency by applying a forward gate voltage sweep to the top electrode from +5 V to -10 V followed by a reverse gate voltage sweep from -10 V to +5 V while keeping the back electrode grounded. The capacitor was therefore subjected to inversion condition at positive voltages to inject minority electron carriers into the charge storage layer and accumulation condition at negative voltages to inject holes into the charge storage layer. The C-V curves of the sample were compared with that of control samples fabricated with an identical device structure, but without ZnO nano discs. A counter clockwise hysteresis loop with a window of 2.53 V was observed in the sample containing ZnO nano discs while a small hysteresis window of 0.4 V was observed in the control sample. The hysteresis window observed in the control sample can be attributed to residual trapped charges existing in the oxide or interface states. The counter clockwise hysteresis observed in the ZnO containing device indicates that there is a net storage of holes that were injected from the substrate through the tunneling oxide to the ZnO nano disc via the substrate injection mechanism [213]. To

further prove that the charges stored are indeed holes, the V_G was held at +10 V for 30 s for the injection of electrons via the substrate injection mechanism. The flatband voltage (V_{FB}) was then determined by applying a small voltage sweep from -2 V to -4 V to subject the capacitor to depletion condition. No shift in the V_{FB} voltage was observed, indicating negligible electron charge storage in the ZnO nano discs.

While the nano disc density was estimated from AFM images to be ~ 8.6 x 10^9 cm^{-2}, the number density of trapped charges was estimated from the area of the hysteresis window (after normalizing with the dimensions of the device) to be ~2.3 x 10^{18} cm^{-3}. This amounts to ~196 holes stored per ZnO nano disc and is suggestive of the presence of multiple defect sites in each ZnO nano disc that provide discrete trap levels for retaining holes. A large shift in the flat-band voltage by 2.53 V achieved at a relatively low operating voltage of 10 V would translate into an effective shift in the threshold voltage to distinguish between erased and programmed states [214]. The achievement of the large memory window at a low operating voltage of 10 V (which is lower than existing operating voltages of > 15 V), is a clear indication of the feasibility of using patterned arrays of ZnO nano discs as charge storage centers to serve as a memory device. This charge trapping capability of ZnO could also find its way in energy harvesting applications such as dye-sensitized solar cells [215] and in charge coupled devices (CCDs). The current-voltage characteristics of the MOS capacitor is shown in Figure 5.1.1.c

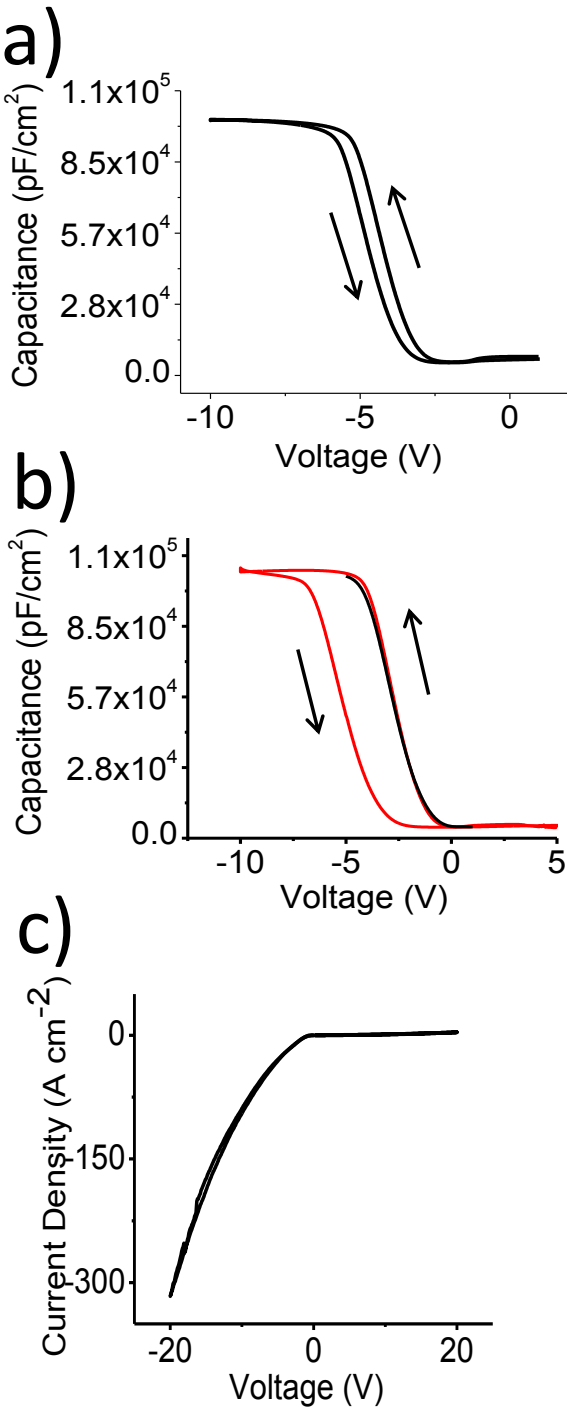


Figure 5.1.1 Capacitance-Voltage characteristics of devices fabricated on a 3nm thick thermally grown tunnel oxide (a) without ZnO nanodiscs (control device), (b) with ZnO nanodiscs sandwiched between the control oxide and thermally grown tunnel oxide and (c) Current-Voltage (I-V) characteristics of ZnO based MOS capacitor.

5.1.2.2. Capacitance-time measurements

The charge retention capability of the ZnO nano disc arrays were investigated by studying capacitance-time (C-t) plots after charging the device at V_G of -10 V for 30 s. A voltage equal to the uncharged flatband voltage V_{FB} (-3.14 V) was applied to the top electrode with the back electrode grounded for 1000 s. For a device containing ZnO nano disc fabricated on native oxide 68 % of the charge carriers were retained after 1000 s of discharging. This charge loss is dominated by the direct tunneling of the trapped charges to the interface states [216].

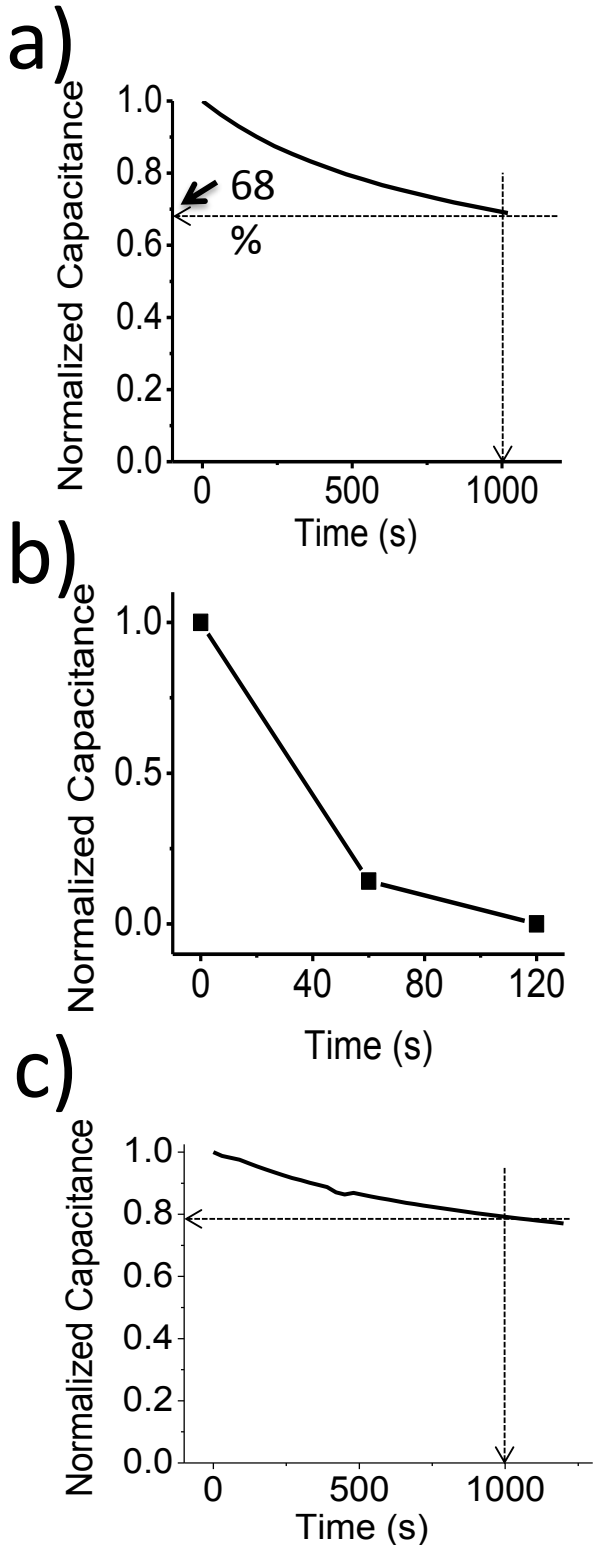
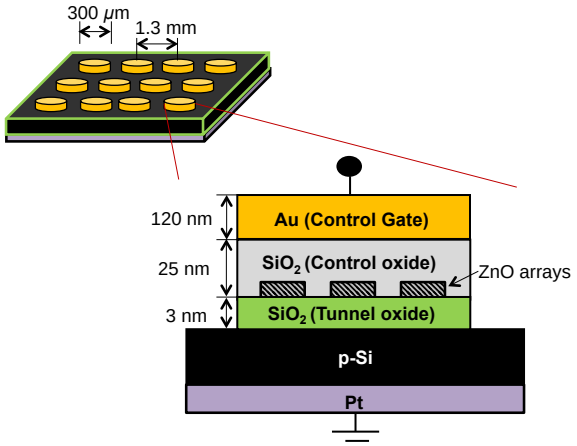


Figure 5.1.2 Capacitance-time characteristics measured for the MOS capacitor device incorporating ZnO nanodisc arrays with voltage held at (a) -10V with the native SiO_2 tunneling oxide layer, (b) at +10V with the 3 nm thermally grown SiO_2 as tunneling oxide layer, (c) -10 V on the 3 nm thick thermally grown tunnel oxide.

To reduce the density of the interface states, which dominates the rate of charge loss, the same device was prepared on a high quality 3 nm thick SiO_2 film grown by thermal oxidation. The C-t measurements under identical conditions as before showed that the percentage charge retention has increased from 68 % to 80 % (Figure 5.1.2 (a) and (c)). This result is comparable, if not superior, to CTF memory devices reported in literature that employ the conventional Si_3N_4 [217] or other high-k dielectric [218] as the charge trapping layer on tunneling oxides with the same EOT as this device. Charge retention between 70-80 % [218] were reported after 1000 s of discharging. This shows that the storage of charge carriers in the ZnO nano discs deters leakage by direct tunneling, which is a cause of poor charge retention when tunneling oxides of thicknesses less than 4 nm are employed. The improved charge retention can be explained by the presence of defect sites in the ZnO nano discs, which creates deep discrete trap levels that are capable of storing and retaining charge carriers over time [203]. Charge carriers thus trapped in spatially-isolated ZnO nano discs are expected to be well-isolated from each other resulting in minimal lateral charge conduction. This would result in a device that is more resilient to SILC [37] and to leakage paths created by pinhole defects than CTF memory devices that rely on a continuous dielectric film as the charge storage layer.

5.1.3. Area selective ALD derived ZnO nanoparticle array based MOS capacitor device



Scheme 5.1.2 Description of the physical dimensions of the capacitor test structure

Electrical characteristics of the ZnO nanopatterns on p-Si substrate were investigated by incorporating them within a metal-oxide-semiconductor (MOS) capacitor. A 25 nm thick silicon dioxide was deposited by RF sputtering to act as the control oxide dielectric. Due to the isotropic sputter deposition, the SiO_2 film completely encapsulated the ZnO nano discs. The substrate was annealed before and after deposition of the control oxide. Au contact electrodes of 0.03 cm diameter and spaced 1 mm apart were then deposited through a metal stencil mask. A 120 nm thick electrode deposition was carried out by line of sight evaporation of gold using an electron beam evaporator. A Pt back electrode was sputtered on the backside of the silicon substrate after removing the oxide using sandpaper. The Pt/p-Si/SiO_2/ZnO nanoarrays/SiO_2/Au (electrode) sandwich structure was used to investigate the charge storage characteristics.

5.1.3.1. Capacitance-Voltage and Capacitance-time measurements

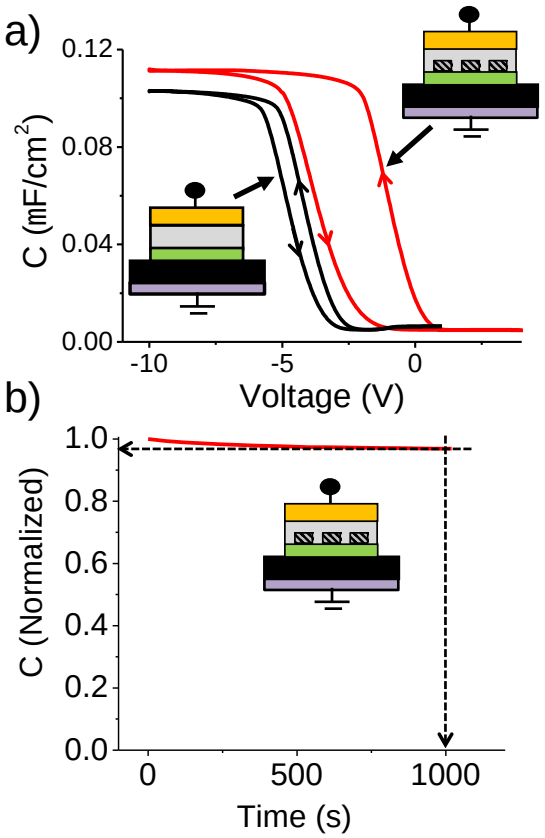


Figure 5.1.3 Capacitance-Voltage characteristics of the device (a) without and with ZnO nanoarrays sandwiched between the thermally grown tunnel and control oxides. (b) Capacitance-time measurement to check the retention ability of the ZnO nanoparticle arrays with a 3 nm thick thermally grown tunneling oxide.

The Capacitance-Voltage measurements were performed at 100 kHz for the test capacitors with and without ZnO arrays by sweeping the gate voltage from +5 V to -10 V and vice versa (Figure 5.1.3 (a)). The counter-clockwise hysteresis confirms hole-storage behavior. The capacitors incorporating ZnO arrays showed hysteresis of 2.82 V in comparison to a low hysteresis of ~0.4 V for the control substrates with no ZnO. The negligible hysteresis observed on the control substrates represent the residual trapped charges in the trap states present in the oxide or the interface. Normalization of the charge density with the feature density of ZnO as known from

the AFM (of ~8.6x10^{9} cm^{-2}) provides an estimate of ~228 holes stored per feature. Coupled with the information of the volume per ZnO feature obtained from the AFM, the charges trapped per unit volume of the material can be estimated to be 7.39 × 10^{18} cm^{-3}. This suggests a high density of trap states, and consequently high charge storage capacity. Capacitance-time measurement (C-t) was performed to study the depletion of charges as a function of time at an applied voltage corresponding to V_{FB} (-1.3 V). The C-t measurements show excellent retention of 97 % of the charge at the end of 1000 s (Figure 5.1.3 b). As an estimate of charge retention as a function of time for longer durations [218], extrapolation of the C-t curve shows retention of 84 % at end of 10^{8} s (Figure 5.1.4).

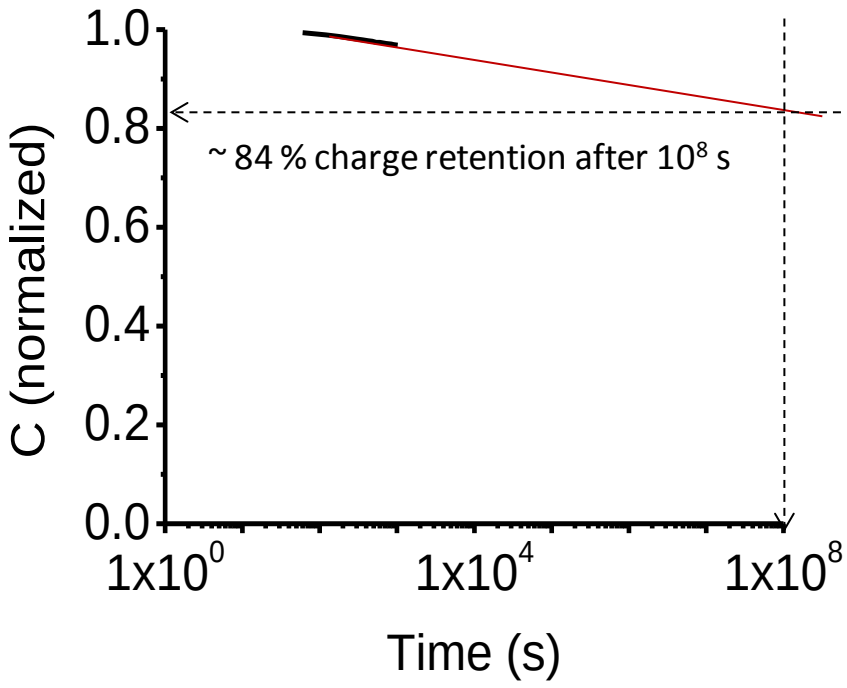
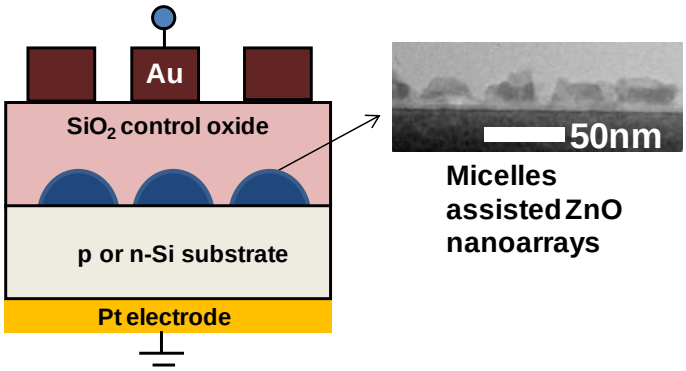


Figure 5.1.4 Extrapolated Capacitance-time characteristics of ZnO nanoparticle array fabricated on 3 nm thick thermally grown tunneling oxide showing 84 % charge retention after 10 years.

However, deviation from the extrapolated behavior is expected, with a decreasing slope of the C-t curve as a function of time [206]. This is due to the fact that the initial

phase of the C-t measurements represents depletion of charges mainly from shallow trap states. However, the charge carriers trapped in deeper levels tend to be more resistant to depletion. As a result, an extrapolation generally presents a worst-case scenario to the retention behavior of the device, which in our case is still confidence inducing. The retention characteristics is comparable to the CTF memory devices reported in literature that employ the conventional SONOS [217] or other high-k dielectric [218] as the charge trapping layer [37]. Besides presence of deep level traps in ZnO, the excellent charge retention ability can be attributed to the well patterned and spatially-isolated features that reduce leakage through lateral conduction as well as reduced stress induced leakage [207].

5.1.4. PS-*b*-PVP derived ZnO nanoparticle array based MOS capacitor device



Scheme 5.1.3 Capacitor test device structure showing the TEM side view of ZnO nanoarrays as charge storage centers.

The electrical characteristics of the ZnO nanopatterns on p-Si and n-Si substrate were investigated by sandwiching them within a metal-oxide-semiconductor (MOS) test capacitor as illustrated in Scheme 5.1.3. A 40 nm thick silicon dioxide was deposited by RF sputtering to act as the control oxide dielectric. The substrate was annealed before and after deposition of the control oxide. Au contact electrodes of 0.03 cm

diameter and spaced 1 mm apart were then deposited through a metal stencil mask. The electrode deposition was carried out by line of sight evaporation of gold using an electron beam evaporator. Platinum was used as the back electrode and was sputtered to the back of the silicon substrate after removing the oxide using sandpaper. The Pt/p-Si/SiO_2/ZnO nanoarrays/SiO_2/Au (electrode) sandwich structure was used to investigate the charge storage and retention characteristics.

5.1.4.1. Capacitance-Voltage measurements

The capacitance-voltage measurements were performed at 100 kHz for the test capacitors with ZnO arrays built on p-Si by sweeping the gate voltage from +5 V to -10 V and vice versa (Figure 5.1.5 (b)). The capacitors incorporating ZnO arrays showed hysteresis of 2.2 V. The counter-clockwise hysteresis observed confirms hole-storage behavior. The small hysteresis observed on the control substrates represent the residual charges in the trap states present in the oxide or the interface. Similarly, capacitance-voltage measurements were performed on n-Si by sweeping the applied gate voltage between -3 V and +3 V. As could be observed from Figure 5.1.5 (a), there is no appreciable hysteresis or flatband voltage (V_{FB}) shift. There is no net charge trapping taking place in the ZnO floating gate. This suggests that no charge injection into the ZnO nanopatterns takes place and hence charges are not trapped. The intrinsic n-type nature of the ZnO nanopatterns owing to the presence zinc interstitials and oxygen vacancies [219] may prevent the negatively charged electrons from being injected from n-Si and be stored in the ZnO traps during the voltage sweep. Moreover, any charges stored in the interface traps or in border traps are rapidly discharged while erasure so that a negligible or no flat band voltage shift is

observed [150]. The hysteresis behaviour is similar to earlier reports on the ZnO capacitor structures fabricated on n-Si [150, 220]. The charge storage density was estimated from area of the hysteresis curve of the capacitor device incorporating ZnO built on p-Si and after normalizing with the volume of the features was found to be 3.47×10^{18} cm^{-3}. With the feature density of ZnO as known from the AFM (of $\sim 2.4 \times 10^{10}$ cm^{-2}), the charge density translated into an estimated ~55 holes getting stored per nanofeature. This is indicative of high density of trap states that enables high charge storage capacity demonstrating the potential of the ZnO nanopatterned arrays to act as charge storage centres in flash memory devices.

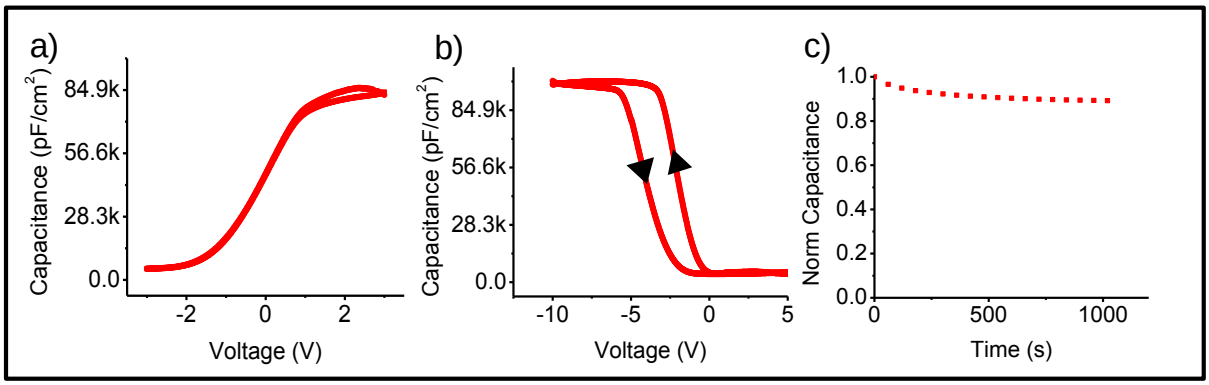


Figure 5.1.5 Capacitance-voltage characteristics of the device (a) built on n-Si and (b) p-Si. (c) Capacitance-time measurement to check the charge retention ability of the ZnO nanopatterns employing a 3 nm thick thermally grown tunneling oxide.

5.1.4.2. Capacitance-time measurements

Capacitance-time measurements for the test structure built on p-Si was performed to study the rate of discharge as a function of time at an applied voltage corresponding to V_{FB} (-2.35 V). The C-t measurements show good retention of ~90 % of the charge at the end of 1000 s (Figure 5.1.6 (c)). As an estimate of charge retention as a function of time for longer durations [206, 218], extrapolation of the C-t curve shows retention of 81 % at end of 10,000 s.

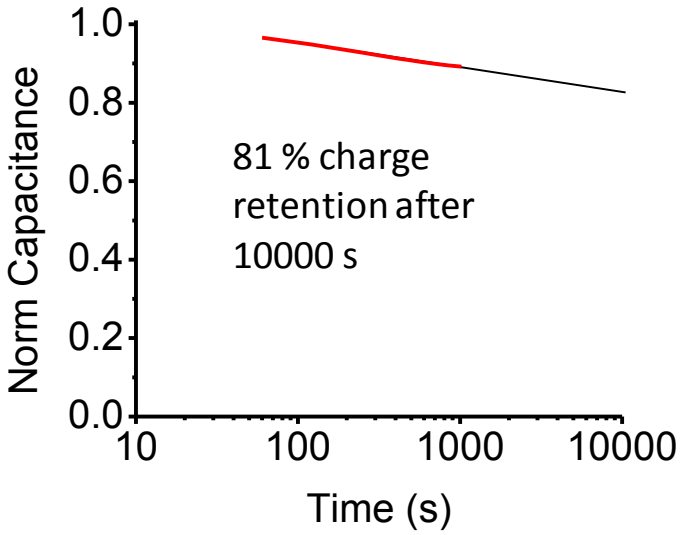


Figure 5.1.6 Extrapolated capacitance-time characteristics of ZnO nanopatterned array fabricated on 3 nm thick thermally grown tunneling oxide showing 81 % charge retention after 10^4 s.

The initial phase of the capacitance decay indicated the depletion of charges primarily from shallow trap states. However, the deeper levels trapping charge carriers tend to be more resistant to leakage and hence an extrapolated C-t decay represents a worst case scenario whereas the real C-t behavior is expected to show better retention [155]. Moreover, good charge retention characteristics can also be attributed to the well patterned and spatially-isolated nanoarrays when the chance of lateral conduction and charge leakage is almost negligible. At the same time, the device exhibits resilience to SILC [37, 207]. The retention characteristics is comparable to the charge trap flash CTF memory devices reported in literature that employ the conventional SONOS [217] or other high-k dielectric [218] as the charge trapping layer [37]. Since the fabrication of ZnO nanoarrays were carried out at low temperatures, the protocol can be extended to flexible plastic substrates. Moreover, incorporation of precursors into the reverse micelles is non-specific to Zn and hence variety of metal and metal oxide nanoarrays of different materials with specific interest toward charge trapping can be

patterned. Fabricating such patterns in sub-50 nm regime with lower aspect ratios, allow the possibility of widening the scope of application by employing them as building blocks within other optoelectronic nanoscale devices such as solar cells and solid state lighting etc.

5.1.5. Comparison of the ZnO nanoarray devices obtained using various techniques

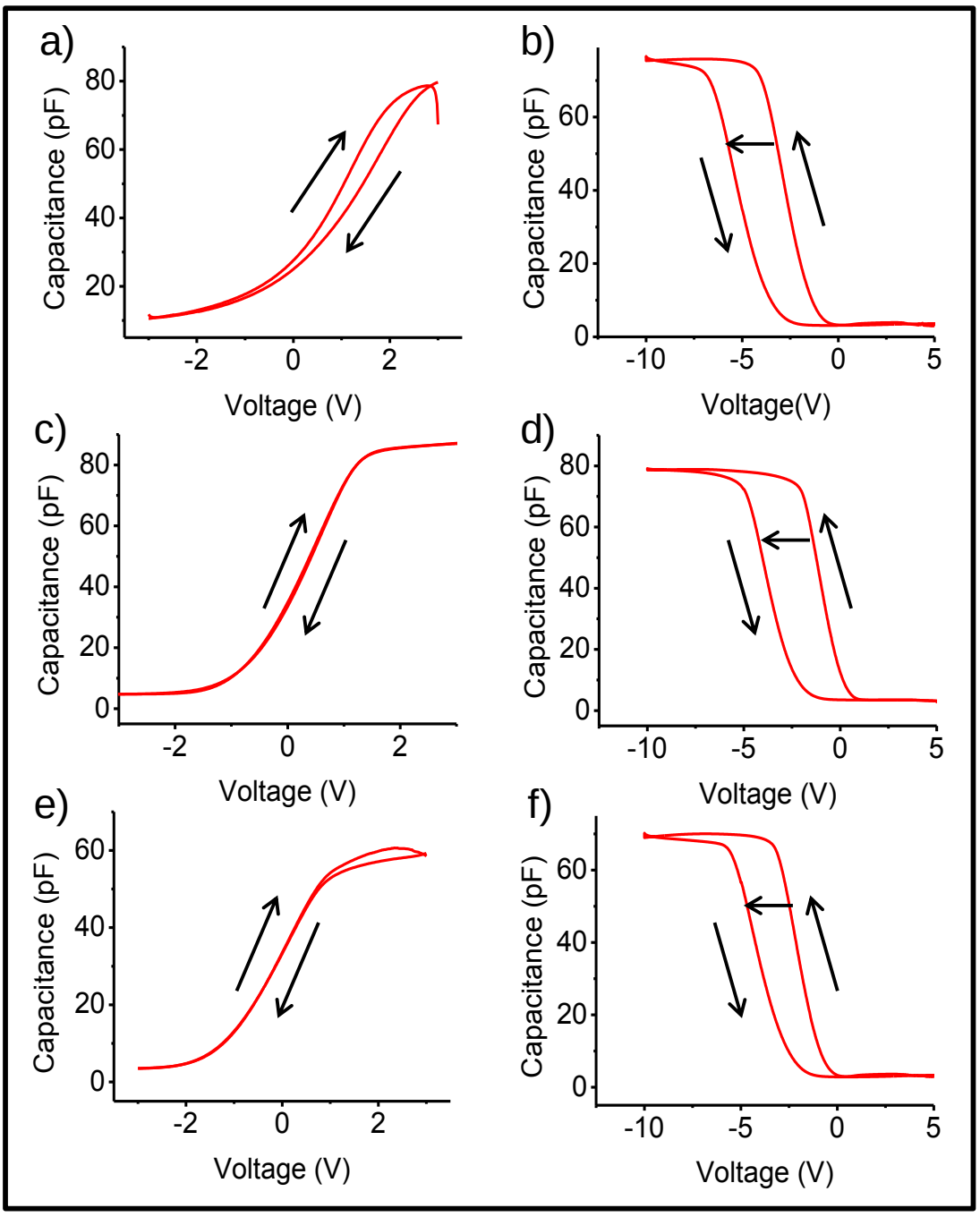


Figure 5.1.7 Capacitance-voltage characteristics of the capacitor devices incorporating ZnO nanoarrays fabricated through (a), (b) NIL assisted RF sputtering; (c), (d) NIL assisted ALD. (e), (f) PS-*b*-PVP micelle assisted ALD. (a), (c) and (e) correspond to device structures built on n-Si while (b), (d) and (f) employed p-Si.

In contrast to the devices constructed on p-type Si, the devices fabricated on n-Si showed no hysteresis in all three cases discussed above (Figure 5.1.7). The hysteresis behavior of the ZnO capacitor structures fabricated on n-Si is similar to those observed in earlier reports [150, 220] while the behavior p-Si varies significantly from case to case. Although operating voltage of the device remain the same in all the cases (10 V), variables such as ZnO crystallinity, feature dimension, density of features, thickness of different layers in the device stack are critical components that determine the device performance. The charge storage density was estimated based on the area of the hysteresis window normalized with the device dimensions. The device characteristics of all MOS capacitors described in this section are summarized in Table 5.1.1.

Fabrication style	**Flatband voltage shift**		**Operating voltage**		**Charge storage density (per cm^3)**	
	n-Si	**p-Si**	**n-Si**	**p-Si**	**n-Si**	**p-Si**
BCL-NIL assisted RF sputtering	Negligible shift (due to interface traps)	2.53 V	-3 V to 3 V	5 V to -10 V	----	2.36E+18
BCL-NIL assisted ALD	No shift	2.82 V	-3 V to 3 V	5 V to -10 V	----	7.39E+18
PS-*b*-PVP assisted ALD	No shift	2.20 V	-3 V to 3 V	5 V to -10 V	----	3.47E+18

Table 5.1.1 Summary of the electrical characteristics of the ZnO nanoarrays fabricated using various techniques.

5.1.6. Conclusions

The work presents a simple yet highly controlled route to produce high-density nanopatterns of ZnO with excellent pattern definition (low standard deviations in geometric attributes of the features) by incorporating the ALD precursor selectively into the micelle templates and by confining through physical and reactive deposition of ZnO using NIL templates. While the ZnO fabricated using NIL templates offer a sub-100 nm patterning, the in-situ ALD-formed ZnO produces sub-50 nm features. The results of the electrical characteristics of the ZnO nanoarrays showed their promise as charge storage centres with high storage density and excellent retention characteristics demonstrating significant potential for use in charge trap flash memories. In addition, the ability to create robust nanopatterns of ZnO in a tunable and controlled fashion donot restrict the application to just NVM devices but widens the spectrum of applications of the patterns as basic building components in other electronic devices as well.

SECTION 5.2

APPLICATIONS OF SELF ASSEMBLY DERIVED HIERARCHICAL GOLD NANOPARTICLE SUPERCLUSTERS

5.2.1. Introduction

Semiconductor devices for memory applications with high speed, high density, longevity and endurance are always in great demand. The conventional continuous floating gate device structures have issues with scaling down of critical feature dimensions that result in poor device performance and the need for an alternative [153, 221]. Furthermore, when the thickness of the floating gate layer is scaled down, multiplication of particle density becomes difficult which in turn compromises on the number density of stored charges thereby affecting the device performance significantly [205]. On the other hand, nitride based memory devices such as silicon-oxide-nitride-oxide-silicon (SONOS) suffers from the limitations due to the shallow trap levels that are vulnerable to easy leakage of stored charges [208]. Moreover, with the stringent norms associated with ultrathin tunnelling layer requirements, leakage of charges from the nitride traps raises a serious concern about the performance of the device in terms of charge retention [40, 222].

On the contrary, nanocrystal-based memories offer multi-bit storage capability, deep trap states and process flexibility to progressively scale down device dimensions according to the needs of the silicon industry as per ITRS [32, 33, 204]. Fabrication of metal nanocrystal (NC) based non-volatile memories (NVM) has become increasingly important and is preferred over their semiconductor counterparts [86], conventional floating gate devices [205] or the CTF devices [18, 223] as it offers numerous advantages in terms of higher density of states, better size tunability and scalability to optimize device characteristics [207, 208]. Moreover, metal NC based memory architectures are attractive due to enhanced retention due to deep trap levels and

isolated features, ability to cope with the demanding scaling issues, multi-bit storage capability etc.

The performance of nanocrystal memory devices critically depends on the size of nanoparticle, its density and distribution and spatial arrangement [224, 225, 226]. Various techniques employed to fabricate metal nanocrystals as the charge storing layer on Si surfaces include thin film deposition and annealing [214, 216, 227], in-situ synthesis within block copolymer templates [208, 228], binding of metal nanoparticles on surfaces using covalent assemblies [85, 229] and LBL assembly [230, 231]. Out of these, directing the metal nanoparticle deposition using block copolymer templates in a hierarchical fashion receives special attention due to the ability of templates to exert a definite control over the geometric attributes such as the nanoparticle density, feature-to-feature interval, periodicity and spacing of the resulting assemblies at every level [102]. This helps in overcoming the problem of inhomogenity in the size distribution of the nanoparticles, randomness, agglomeration and poor reproducibility associated with the conventional thin film producing techniques [86]. There are reports on the use of block copolymers as templates to produce patterns of metal and metal oxides such as TiO_2 [137], Ag [232], Pt [90] and gold nanoparticles [228, 233]. This allows to have mixed or hybrid structures in hierarchically assembled systems. There are reports on the hierarchical self assembly of metal nanostructures although a three level hierarchical system where complete control over each hierarchy, its functionalization, feature density and definition has not been reported [234, 235, 236]. Fabricating self assembly derived hierarchical nanostructures offer a precise control over the degree to which each level of

hierarchies could be functionalized with the required material and in exercising control over the feature density and organization. However, BCP templates for producing hierarchical gold nanoparticle assembly for enhancing the performance of metal NC flash memory devices have not been discussed before. BCP self-organization is a simple, economical, and scalable nanofabrication tool capable of producing sub-10 nm resolution in feature dimension and spacing for highly miniaturized silicon technology with an insight into the future [91, 136].

Any newly proposed device structures are expected to have characteristics that combine the benefits of 1) fabrication- tunability, offering nanoparticle density multiplication, uniformity and reproducibility; 2) device performance- low operating voltages, enhanced charge retention without compromising on the ultrathin tunnelling oxide layer, possibility for enhancing charge storage and multi-bit storage; 3) adaptability to incorporate multiple functionalities to the existing system. In this direction, we describe here unique device architecture with the potential to achieve the above-stated device performances by employing the self organized block copolymer templates in a hierarchical fashion to electrostatically direct the nanoparticle assembly.

The approach is targeted towards fabricating high density assemblies of electrostatically directed pre-formed gold nanoparticles on micelles in a hierarchical fashion. Density multiplication for enhancing the charge storage is achieved by the formation of gold nanoparticle superclusters (cluster of clusters of type *(ACy)(Cz)x* - where *A* and *C* are gold features) as demonstrated in Section 4.1 and 4.2. Moreover,

the protocol offers highly reproducible characteristics over the entire device area with the resulting supercluster arrays clearly exhibiting a 1.5 fold increase in charge storage density at low operating voltages over the device containing only *'A'* gold features. The proposed device exhibits 10 year charge retention behaviour and at the same time, a good charge storage behaviour with over 1.1 V hysteresis window at low operating voltages excelling our previous report on enhancing the charge storage capacity by ~0.25 V [224, 228].

5.2.2. Gold nanoparticle supercluster based MIS capacitor device

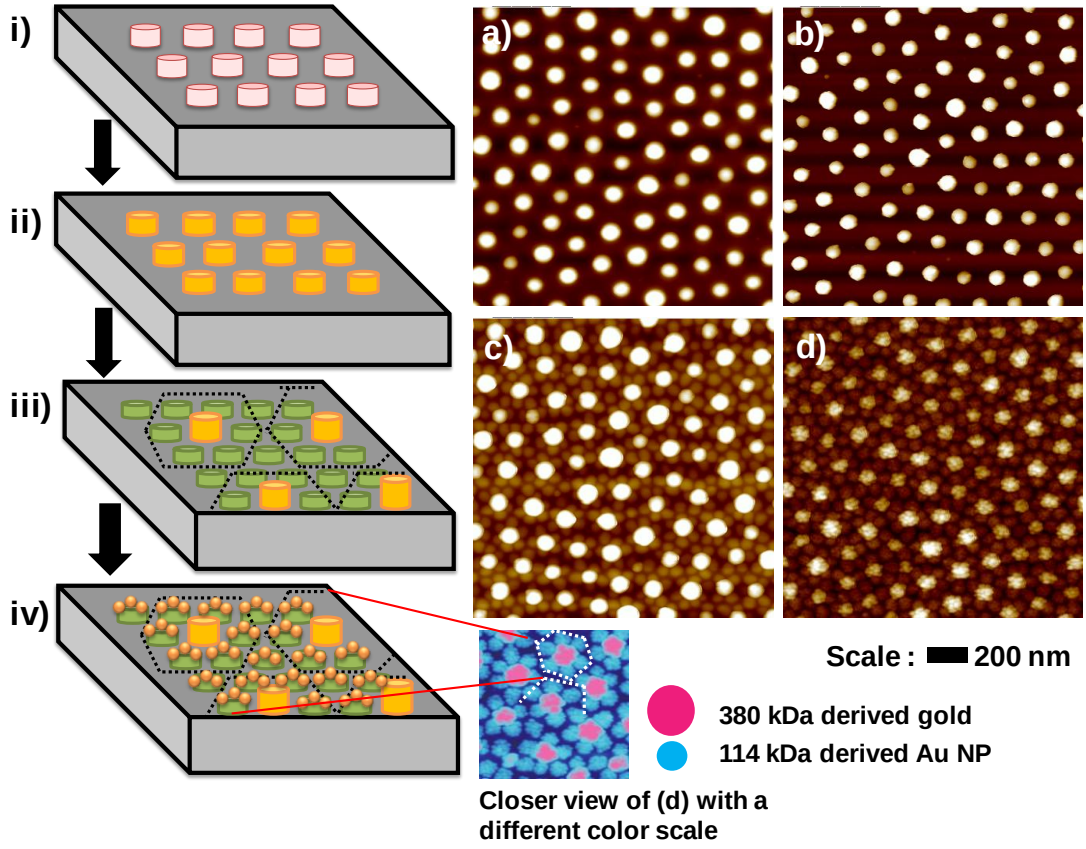


Figure 5.2.1 (i-iv) Illustration of steps towards creating Au NP hierarchical supercluster using block copolymer templates. Tapping mode AFM images showing (a) the spin coated PS-*b*-PVP (380 kDa) reverse micelles (illustrated in step (i) of schematic) that acted as anchor points for (b) in-situ synthesis of '*A*' gold features (illustrated in step (ii) of schematic). (c) Second level of hierarchy obtained after spin coating 114 kDa reverse micelles of PS-*b*-PVP *'B'* onto the '*A*' features (illustrated by step (iii) of schematic) which direct the (d) electrostatic self assembly of citrate stabilized preformed gold nanoparticles *'C'* giving rise to third hierarchy or superclusters illustrated by step (iv) of schematic.

The 380 kDa PS-*b*-PVP copolymer arrays exhibited quasi-hexagonal order and a number density of 2.1×10^{9} cm^{-2} (calculated from AFM measurements (Figure 5.2.1 (a))) with excellent uniformity over the entire coated area acted as the guiding BCP

template to drive the first hierarchy of '*A*'. The *'A'* gold features in the first level of hierarchy exhibited a diameter of ~90 nm and a periodicity of 220 nm. In the second level of hierarchy, the 114 kDa PS-*b*-PVP *'B'* was spin coated on top of the *'A'* features. The corresponding AFM images are shown in Figure 5.2.1 (c) (illustrated in schematic step (iii)). We find that each of the *'A'* features is surrounded by the *'B'* micelles in a flower like pattern. The array is then immersed in the pre-formed gold nanoparticles *'C'* that are citrate-stabilized in aqueous suspension exhibiting diameter of 10 (±2) nm. This results in electrostatically directed self assembly of *'C'* over *'A'* and *'B'* and thus the gold nanoparticle supercluster array as referred in Section 5.1. The illustration in Figure 5.2.1. shows the presence of 114 kDa micelles after the deposition of citrate-Au nanoparticles, while before device fabrication, the polymer *'B'* is removed using oxygen plasma followed by annealing (Figure 5.2.4). This results in the supercluster array of type $(Au.Au_y)(Au_z)_x$ which is used in MIS capacitor devices.

5.2.2.1. Control devices: 380 kDa derived gold template and 114 kDa gold Au NP cluster

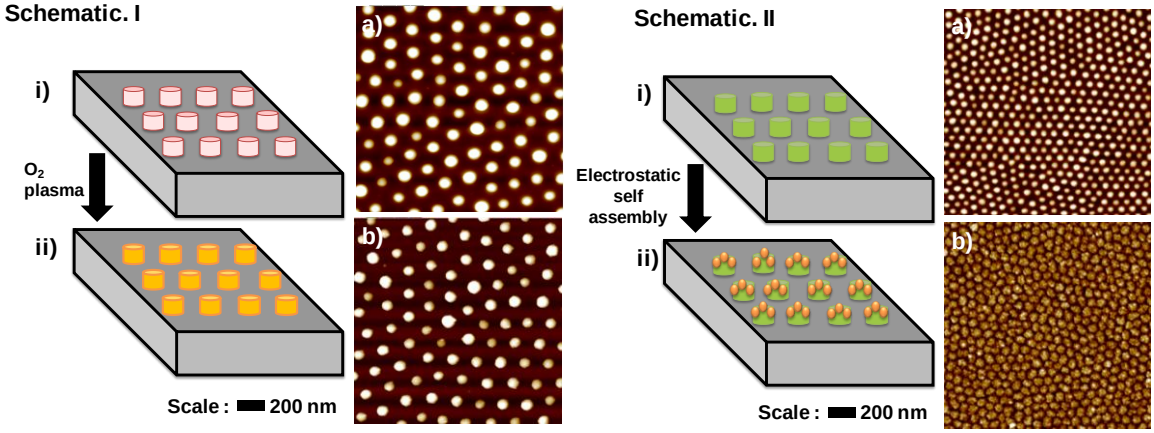


Figure 5.2.2 (I) (i-ii) Illustration of steps towards creating only *'A'* gold features as control. Tapping mode AFM images showing a) the spin coated PS-*b*-PVP (only 380 kDa) reverse micelles (illustrated in step (i) of schematic) that acted as anchor points for b) in-situ synthesis of *'A'* gold features (illustrated in step (ii) of schematic). II) (i-ii) Illustration of steps towards creating 114 kDa derived gold NP cluster as control. (a) Tapping mode AFM image of the spin coated PS-*b*-PVP (only 114 kDa) reverse micelles (illustrated in step (i) of schematic) which direct the (b) electrostatic self assembly of citrate stabilized preformed gold nanoparticles cluster arrays (illustrated by step (ii) of schematic).

In order to understand how the superclusters influence and enhance the charge storage and retention capabilities, the different hierarchical stages were split and the following control experiments on bare Si chips were independently carried out (Figure 5.2.2)- i) obtaining gold templates (*'A'* arrays of gold) using 380 kDa PS-*b*-PVP as described earlier and constructing MIS capacitors without building any further hierarchical structures, ii) obtaining Au NP clusters by directly spin coating the 114 kDa PS-*b*-PVP reverse micelles on bare Si chips followed by the electrostatic self assembly of pre-formed gold nanoparticles. The polymer is then removed using oxygen plasma before device making. The two samples are independently tested for their capacitance behavior when they do not form a part of the hierarchical assembly and when they are

under no influence from the superclusters. The number densities of *'A'* gold features and the 114 kDa PS-*b*-PVP were observed to be 2.1×10^{9} cm^{-2} and 1.1×10^{10} cm^{-2} respectively.

5.2.2.2. Au Supercluster MIS device characteristics

The (i) gold nanoparticle superclusters $(Au.Au_y)(Au_z)_x$., (ii) *'A'* gold features and (iii) 114 kDa derived gold nanoparticle cluster are tested separately for their charge storage characteristics by incorporating them within a metal-insulator-semiconductor (MIS) capacitor device on a p-type silicon substrate (schematic in Figure 5.2.3. (a), (b) and (c)). A control device with no charge storage centres was also fabricated. Side view TEM of the device structure (Figure 5.2.3) shows the Pt/p-Si/SiO_2/Au NP supercluster/SiO_2/Au (electrode) stack test capacitor structure. A 50 nm thick silicon dioxide was deposited by RF sputtering to act as the control oxide dielectric. Due to the isotropic nature of deposition by sputtering, the SiO_2 film completely covered the Au NP superclusters preventing any shorting between the top electrode and the CSC, as could be observed in the TEM image. The substrate was annealed after deposition of the control oxide. 120 nm thick Au contact electrodes were then deposited through a metal stencil mask of 0.03 cm diameter and spacing of 1 mm. The electrode deposition was carried out by line of sight deposition of gold using an electron beam evaporator. A Pt back electrode was sputtered on the backside of the silicon substrate after removing the native oxide using sandpaper.

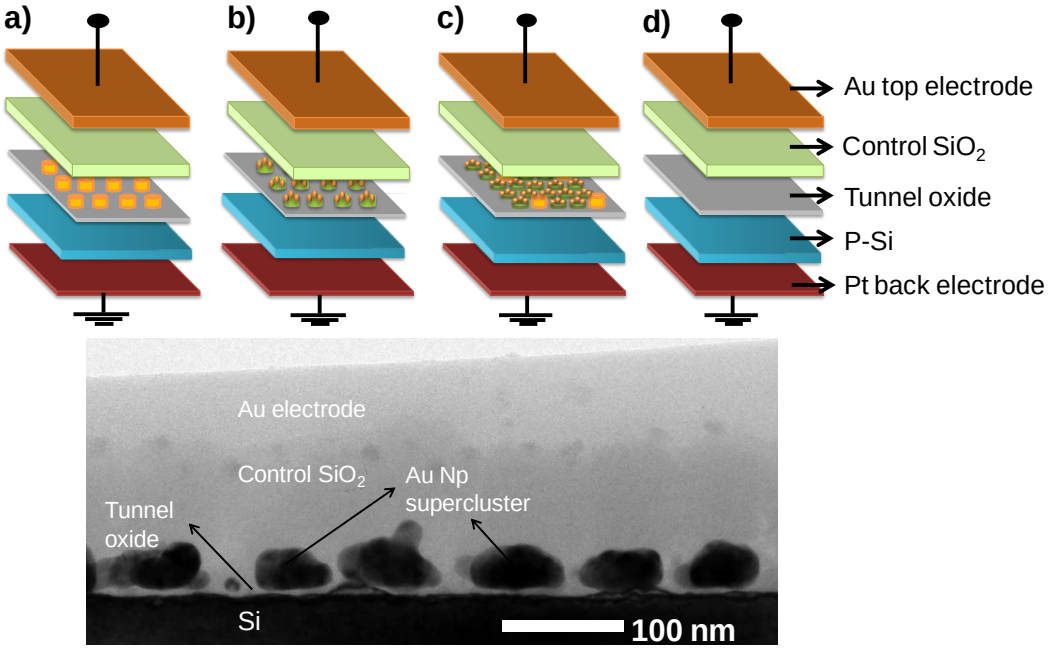


Figure 5.2.3 Schematic of the MIS capacitor test structure incorporating (a) *'A'* gold nanofeatures, (b) 114 kDa derived gold nanocluster and (c) supercluster arrays as CSCs to investigate charge storage characteristics. d) Control device with no charge storage centres. The cross section TEM shows various layers of the supercluster test device architecture.

Since the superclusters are built for enhancing the charge retention in the nanocrystal MIS device, it is essential to check for any presence of residual polymer after plasma treatment before the control oxide could be deposited. The XPS results as shown in Figure 5.2.4 shows that there is indeed no nitrogen present while at the same time, the gold signals from the arrays remain pronounced, thereby confirming that no residual polymer is present in the assembly.

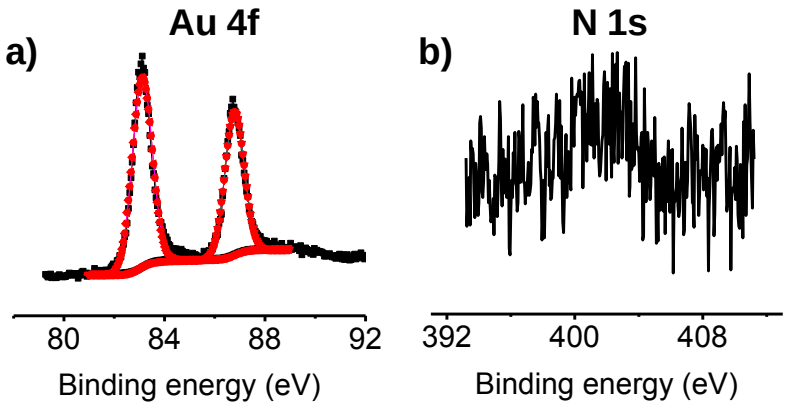


Figure 5.2.4 XPS results performed on the plasma treated superclusters to check for any polymer residues. (a) shows the Au 4f signals from the gold hierarchical structures while (b) no appreciable nitrogen from the PS-*b*-PVP is observed.

5.2.2.3. Capacitance-Voltage (C-V) characteristics

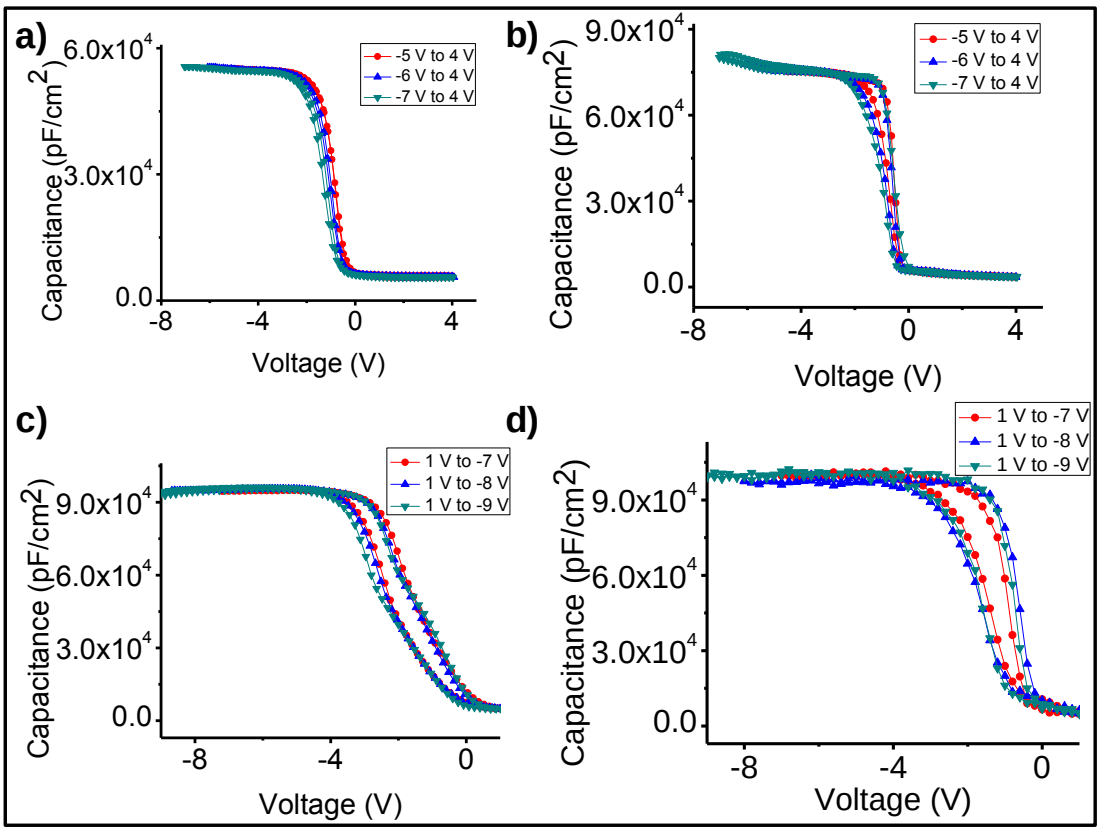


Figure 5.2.5 Capacitance-voltage characteristics of (a) control device with no CSC, (b) 114 kDa derived gold nanoparticle cluster, (c) 380 kDa derived gold template (only *'A'*) and (d) Gold nanoparticle supercluster with three levels of hierarchy.

The C-V characteristics were studied using a MIS structure (Figure 5.2.5). C-V hysteresis curves of the MIS memory device containing no gold nanostructures (control), 114 kDa derived Au NP cluster, *'A'* gold features and the hierarchical superclusters are shown in Figure 5.2.5 (a), (b), (c) and (d) respectively. The gate bias voltage was swept more towards negative potential. For any increase in the negative gate potential (until -7 V), the control sample showed little or negligible V_{FB} shift. In all the other three cases, the observed counter-clockwise hysteresis demonstrated net positive charging or hole injection into the charge storage centers due to net hole trapping from the substrate accumulation layer into the gold nanofeatures. The MIS test device with 114 kDa derived Au NPs showed a counter clockwise hysteresis with the memory window of 0.62 V when the applied negative operating potential was 7 V. The devices containing *'A'* gold nanofeatures and the hierarchical gold supercluster $(Au.Au_y)(Au_z)_x$ showed a memory window or V_{FB} shift of 0.82 V and 1.13 V respectively when operated at 9 V. It could be inferred that increasing amounts of charges tunnel through the oxide layer and get stored in the gold nanofeatures when the applied negative bias is increased and the C-V curve shifts more towards negative voltages. The memory window did not expand or shift when the applied voltage shifts more towards positive potential. This suggests that the charges trapped are indeed holes [213] (Figure 5.2.6).

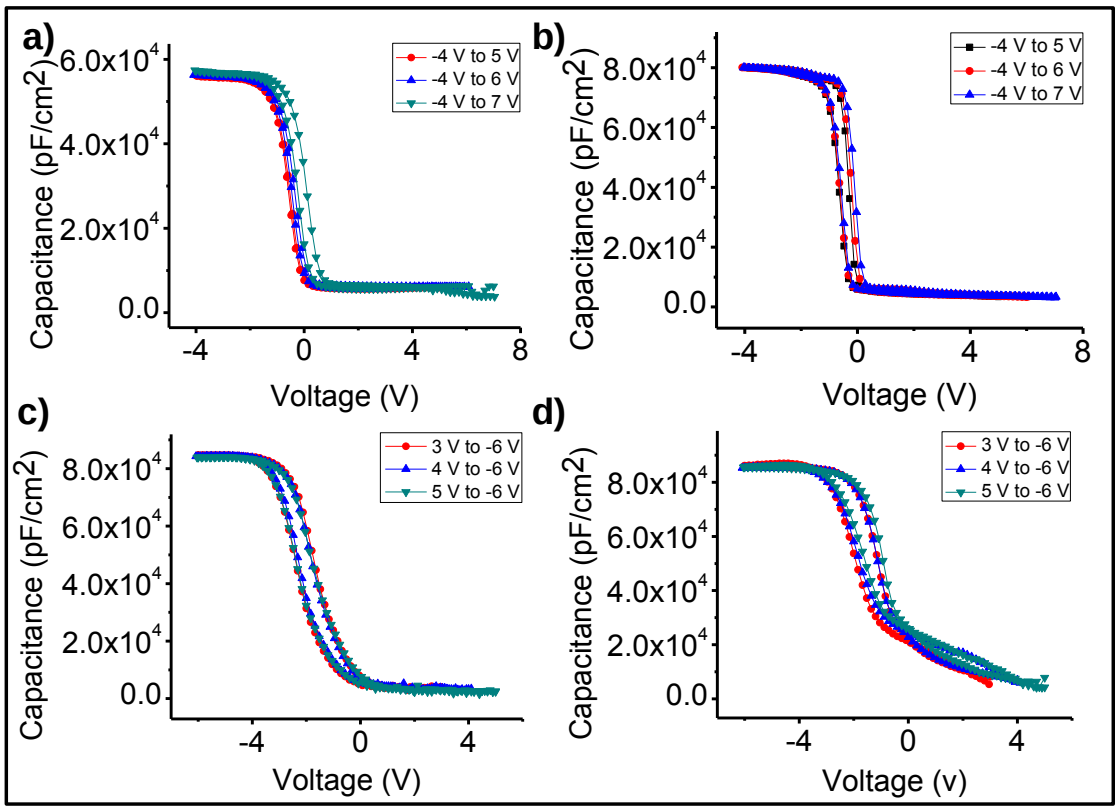


Figure 5.2.6 Application of positive bias voltages to check for any net electron trapping. Capacitance-voltage characteristics of devices (a) with no CSC, (b) 114 kDa derived gold nanoparticle cluster, (c) *'A'* gold features and (d) Gold nanoparticle supercluster with three levels of hierarchy. No appreciable flat band voltage shift is observed.

The gold nanoparticle supercluster of type $(ACy)(BCz)x$ (Figure 5.2.1 d)) as demonstrated in Section 4.1 were realized upon immersion of the binary superstructures of ABx into an aqueous suspension of citrate-stabilized Au nanoparticles (C) of ~11.7 nm diameter (refer Section 4.1 for experimental details and TEM of Au NP). The B features comprise of PS-*b*-P2VP reverse micelles that has a positively charged PVP core that selectively adsorbs the citrate-stabilized Au nanoparticles due to electrostatic attraction to result in Au nanoparticle clusters (BCz type) [237]. The size of the individual clusters (as defined by the number of nanoparticles adhering to each micelle) is determined by the surface area of the

template feature, which we demonstrated in our earlier study to be ~18 particles/cluster (thus, z ~ 18) [237]. In the case of, gold nanoparticle supercluster of type $(ACy)(BCz)x$, the citrate-Au nanoparticles were not only found to attach on the micelles, but also onto the central Au nanoparticle ('A' features). The latter is likely a consequence of the presence of thin PS-*b*-P2VP brush layer [199] on the surface of the 'A' features, during the coating of the reverse micelle solution during the formation of second hierarchy. Thus, from FESEM measurement of the superclusters at higher magnification, the observed number of citrate-Au NPs were found to be ~17 per parent gold feature which is 4 times less than the estimated Au nanoparticle density calculated based on the available surface area. In an ideal case, the number of citrate-Au NPs adhering to the parent gold template can be estimated [237] based on their surface area to be ~67 particles. The significant fall in density of citrate-Au NPs in the real scenario is likely due to the lower electrostatic attraction on the parent gold template, presumably due to low density of PS-*b*-PVP molecules on its surface. An additional contribution is likely due to the repulsive forces from the citrate-Au NPs on the neighbouring micelle features, in repelling the adsorption on the periphery of parent gold features.

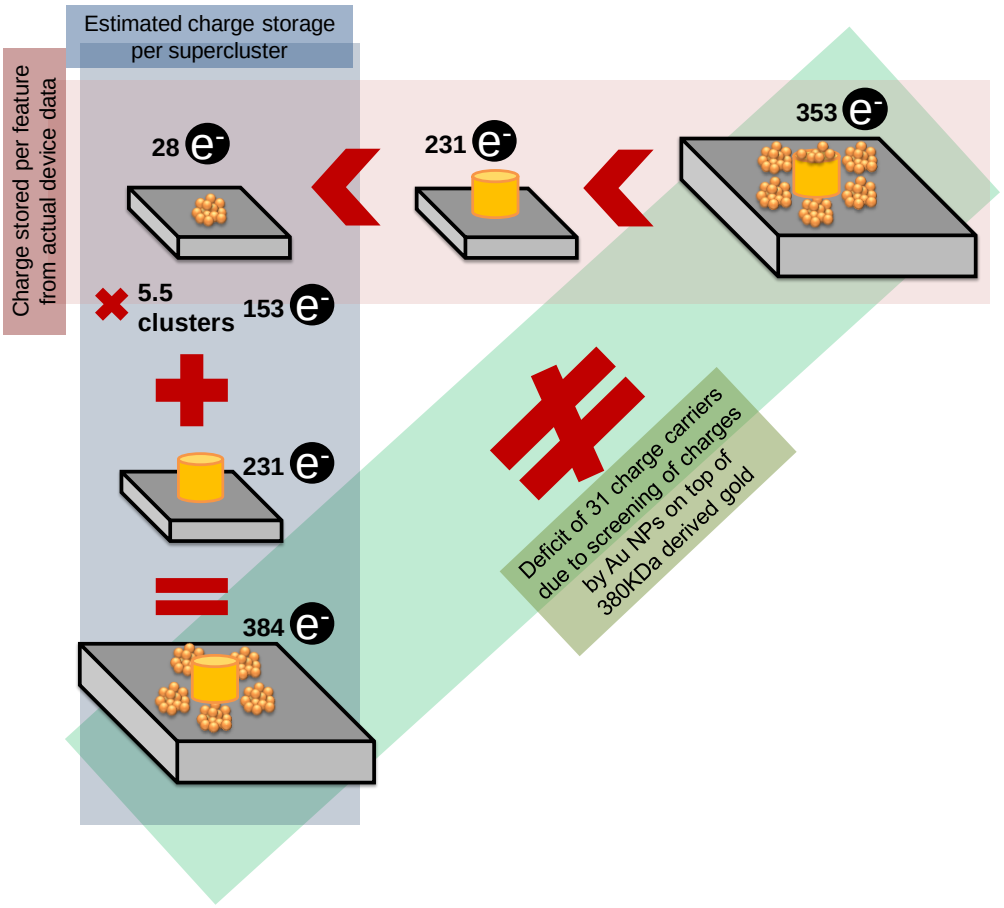
The hysteresis behavior of $(Au.Au_y)(Au_z)_x$) type device can be explained based on the charging/discharging of the nanoparticle charge storage centers. The density of the charge carriers can be estimated using the equation [238]: $Q = (C*V_{FB})/(qA)$, where C is the capacitance value of the dielectric stack layer, V_{FB} is the flat band voltage shift, q is the charge of an electron and A is the area of the electrode. In the MIS device constructed using 114 kDa derived gold nanoparticle cluster, a flat band voltage shift

of 0.62 V for a sweep voltage of 7 V is observed and the charge carrier density is estimated to be 3.14×10^{11} cm^{-2}. For the V_{FB} shift of 0.82 V at 9 V sweep for the device with just *'A'* features, the charge carrier density has been estimated to be 4.85×10^{11} cm^{-2}. With an assumption that the charges are distributed evenly, an estimated ~28 holes per cluster and ~231 holes per gold feature are stored, respectively, in the 114 kDa derived device and devices containing *'A'* gold arrays. From the supercluster device hysteresis, the number of charge carriers estimated increases to 5.06×10^8 when the shift in V_{FB} is 1.13 V at 9 V sweep (Figure 5.2.5 (d)). This charge carrier density is now being shared by three different distributions on the substrate (distribution in the *'A'* gold features, distribution in the Au NP on top of every *'A'* and distribution in the 114 kDa derived Au NP around the *'A'* gold features.). Since, the density of the features in the first hierarchy does not change (conditions similar to control device containing only *'A'* gold features), the number of charges carriers stored by the first hierarchy gold features *'A'* is assumed to be the same as the control device which is ~231 holes per gold feature. This implies that about 3.43×10^8 charges carriers of the total 5.06×10^8 charges carriers are stored in the first hierarchy. The remaining 1.63×10^8 charge carriers are expected to be shared between the 114 kDa derived Au NP cluster and the ~17 Au NPs on top of *'A'* features of the first hierarchy. The total number of citrate-Au NP in the entire supercluster accounts to be $\sim 1.72 \times 10^8$ which in turn accounts for the storage of 1 electron per Au NP. However, in the ideal case, this stands at ~0.7 charge carrier per Au NP when ~67 Au NP is considered to be present on top of 380 kDa gold (*'A'*). The relation between the Au NPs and the charge carriers getting stored into them can be explained by developing a simple supercluster model.

5.2.2.4. Comparison of supercluster model with the actual supercluster device data

The supercluster model (Scheme 5.2.1) can be considered to comprise of one 380 kDa derived gold feature *'A'* (excluding citrate-Au NPs on top of it) surrounded by the cluster of 114 kDa derived gold nanoparticles (refer Appendix 2 for calculations on charge storage density). The performance of the actual supercluster MIS capacitors as analysed from the device data is compared with the supercluster device model by fitting the data obtained from the control devices. From AFM images, the mean number of micelles that surround each *'A'* feature can be estimated to be 5.5 by dividing the total number of *'A'* features by the total number derived from the 114 kDa micelles per μm^2. In other words, one gold nanoparticle supercluster of type $(Au)(Au)_{5.5}$ is modeled. By fitting in the control device data values obtained from the control devices containing *'A'* gold and 114 kDa derived Au NP into the respective features of the model supercluster, it can be inferred that a total of 384 charge carriers are stored per model supercluster. (Calculations in Appendix 2)

On the other hand, from the actual supercluster device data, a supercluster (one *'A'* gold feature + 5.5 114 kDa derived Au NPs surrounding the one *'A'* + 17 citrate-Au NPs on top of *'A'*), stores 353 charge carriers. This is a clear indication of storage of lesser charges in the actual device as compared to a model device.



Scheme 5.2.1 Illustration of the actual supercluster device performance compared with the model.

Since the gold nanoparticle superclusters have three different size distributions (*'A'* gold and 114 kDa derived Au NPs and Au NPs on top of *'A'*) charges injected during programming prefer to reside in the larger sized crystallites because of their proximity to the silicon surface, higher density of states, and lower coulombic barrier [239] followed by the smaller crystallites. However, due to the repulsive forces from the citrate-Au particles on the neighboring 114 kDa derived micelle features and on top of *'A'*, any further injection of charges into the supercluster is screened which accounts for the deficit of 31 charge carriers and the deviation from the ideal case scenario. This is consistent with reports on the creation of electrostatic barrier for the charges to be injected from the substrate that limits the amount of charge carriers that can be

stored in the CSCs [226, 239]. However, despite the screening effect, in our case, the fabrication of the supercluster has facilitated multiplication of the particle density and thereby the charge storage density. This is evident from the fact that a large hysteresis is observed in the case of superclusters than the device fabricated separately from either 114 kDa derived clusters or *'A'* gold arrays.

The V_{FB} shift of various device structures with respect to the operating voltage sweeps is summarized below in Tables 5.2.1 and 5.2.2.

S. No	MIS device	Operating voltage (V)					
		-7	**-6**	**-5**	**+5**	**+6**	**+7**
a)	Control device	0.16	0.12	0.00	0.05	0.09	0.34
b)	114 kDa derived gold nanoparticle cluster	0.62	0.47	0.35	0.35	0.46	0.58

Table 5.2.1 lists the V_{FB} shift of the (a) control device with no CSCs and (b) 114 kDa derived gold NP cluster device.

S. No	MIS device	Operating voltage (V)					
		-9	**-8**	**-7**	**+3**	**+4**	**+5**
a)	380 kDa derived *'A'* gold nanofeatures	0.82	0.65	0.60	0.46	0.66	0.66
b)	Gold nanoparticle Superclusters	1.13	1.23	0.66	0.85	0.70	0.70

Table 5.2.2 lists the V_{FB} shift of the device with only *'A'* gold features and the superclusters with respect to the applied gate voltage.

5.2.2.5. Capacitance-time characteristics

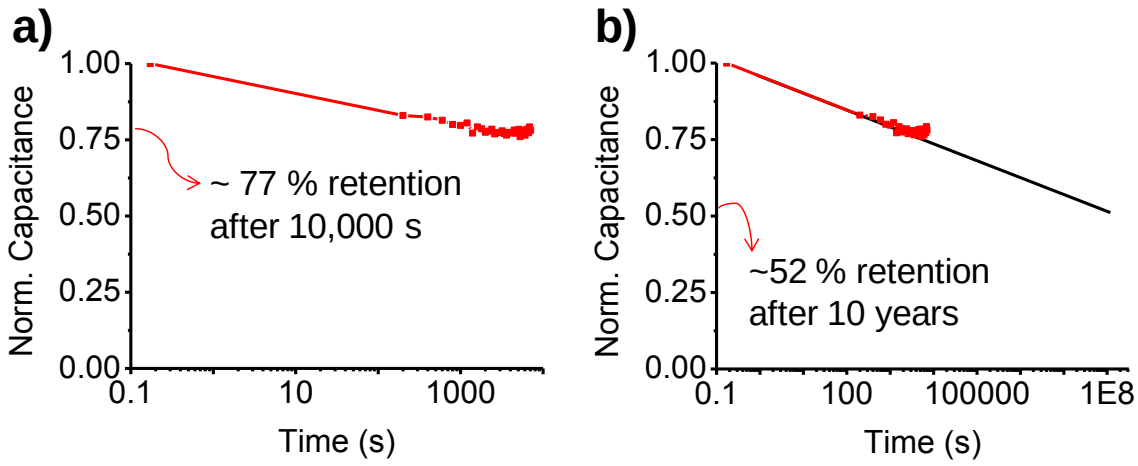


Figure 5.2.7 (a) Capacitance decay characteristics of the Au NP supercluster showing over 77 % retention after 10,000s and (b) extrapolated C-t plot showing a charge retention ability of 52 % after 10 years.

Capacitance decay (C-t) measurement was performed to assess the charge retention capacity of the supercluster MIS capacitor device after charging it at V_G of -9 V for 30 s. A voltage equal to the flatband voltage (V_{FB} = -0.91 V) was applied to the top electrode for 10,000 s with the back electrode grounded. As could be observed from the C-t plot in Figure 5.2.7 (a), the supercluster device shows good retention characteristics retaining over 77 % of the injected charges after 10,000 s. An increased retention can also be due to the well isolated patterns that inhibit any lateral charge conduction [225, 240]. The C-t plot is further extrapolated to evaluate the retention trend after 10 years and it could be observed that the supercluster device could still retain about half the injected charges. The retention characteristics of supercluster based MIS device capacitor is similar to or better than previously reported nanoparticle based memory devices [241] and it can be fabricated with a vastly simplified, economical and tunable method.

5.2.3. Conclusions

In summary, this work presents a novel route to large-scale hierarchical gold superclusters of with high particle and pattern densities. The electrostatic self assembly of Au NPs in a layer-by-layer fashion driven by block copolymer based nanopatterning for density multiplication for application in flash memory devices is described for the first time. The significance of the hierarchical superclusters can be realized when the test devices exhibited significant charge storage and charge retention characteristics due to the enhancement of charge storage density made possible through particle density multiplication, a unique feature offered by the superclusters. The protocol is simple involving cost cutting polymer based approach while at the same time effective in terms of memory performance. The process is amenable to realize a fourth level of hierarchy using metal nanocrystals or combination of materials to form a hybrid supercluster to increase nanoparticle densities even further by optimizing process variables such as the template periodicity of the features, spacing and levels of hierarchy. The protocol also offers handles to enable scaling down of the devices in accordance with the International technology roadmap for semiconductors (ITRS) as the approach is completely based on block copolymer self-assembly which is widely considered as a tool of the future for fabricating sub-10 nm electronic devices such as transistors and diodes.

CHAPTER 6

FABRICATION OF ZINC OXIDE NANORODS THROUGH NON-TEMPLATED APPROACHES

6.1. Introduction

Chapters 3, 4 and 5 described various synthesis protocols and instances where ZnO nanopatterns have been extremely useful as building blocks in NVM applications. Nanomaterials conforming to the desired needs of the researchers have always been exploited owing to the advantages offered in terms of material and structural properties, process flexibility and reproducibility, ultimately resulting in the commercialization of the products. The ability to fabricate metal oxide structures on a nanoscale has distinct advantages that are widely sought after. Synthesis of nanorods [60], nanowires [242], nanotubes [16], nanofilms [71, 243] using ZnO is of crucial importance since different morphologies of ZnO are desired for engineering different optoelectronic [10] devices. The functions and capabilities of these devices are very much associated with the quality, uniformity and crystallinity of the nanostructures for optimal performance.

When a level of control on high feature density over a macroscopic area, as well as the complexity of structures attainable is targeted, hydrothermal synthesis, a simple, cost effective approach is on par with what are achievable utilizing clean room tools [16, 17]. Such high density ZnO nanorods on silicon based substrates with tunable geometric characteristics are of prime interest in semiconductor compatible technologies. In nanomaterials processing, understanding and differentiating the bulk and surface properties becomes vital as they exhibit different optical and structural qualities. This influences and determines the utility of the synthesized nanostructures in many applications. This is best understood when the ZnO nanostructures fabricated using an external surface modifier such as polyelectrolytes is compared for the surface

properties with unmodified nanorods. There are reports on the utilization of cationic dispersants like polyethylenimine [244, 245] and surfactants like polyvinyl alcohol [66] in the growth of the ZnO nanostructures discussing the protocol to tailor the sizes of the nanostructures. However, sufficient focus has not been placed on the changes that take place on the material surface due to the introduction of the external agents. In ZnO nanorods, the surface properties differ significantly from those of the bulk counterpart due to surface related effects. These effects manifest themselves in the emission properties that are studied using photoluminescence spectra [246, 247]. In order to demonstrate the distinct variation in the bulk and surface properties of the ZnO features, we discuss a cost effective protocol in this chapter that i) offers good control over the growth of well aligned ZnO nanorods on a macroscopic scale using polyethylenimine (PEI) whose intentional introduction chemically tailors the size of nanorods in situ and ii) the photoluminescence emission map of the nanorods with and without PEI that helps in understanding the resulting nanorod defects, thereby differentiating the bulk and surface contributions.

ZnO nanorods were grown on bare Si (100) substrates using the conventional and cost effective aqueous chemical growth (ACG) technique [60]. The nanorods thus formed had diameters of several hundred nanometers and could be chemically tuned by the introduction of polyelectrolytes in the growth solution which resulted in the formation of rods with controlled diameters and enhanced growth predominantly in the (002) direction normal to the substrates over macroscopic areas. Optical and structural characterizations were performed to study the nature of the resulting PEI-modified and unmodified nanorods to highlight the role played by PEI in influencing the crystal surface quality.

6.2. Experimental

6.2.1. Materials

Acetone and 2-propanol were obtained as anhydrous solvents with purity > 99% from Sigma-Aldrich Pte Ltd and used without further purification. Prime grade silicon wafers were obtained from Silicon Valley Microelectronics (Santa Clara, CA, USA). Zinc acetate dihydrate and hexamethylenetetramine were obtained from Merck. Polyethyleneimine of molecular weight 750,000 g/gmol was purchased from Sigma Aldrich. Point Probe Plus silicon tips for tapping mode imaging measurements with atomic force microscopy were purchased from Nanosensors (Neuchatel, Switzerland).

6.2.2. Methods

The Si substrates were diced into 2cm x 2cm chips using the Disco automatic dicing and cleaning system. The silicon substrates were cleaned by ultrasonicating in acetone followed by 2-propanol and finally treated with UV/Ozone (SAMCO UV-1, SAMCO Inc., Kyoto, Japan) for 10 minute duration. Hydrothermal synthesis of ZnO nanorods was carried out in a growth solution constituting of equimolar quantities (0.001 M-0.05 M) of zinc acetate dihydrate and hexamethylenetetramine in water. To compensate for the lattice mismatch between the silicon substrate and the ZnO nanorods, a seed layer was deposited on the substrate by spin coating a solution of 0.01 M zinc acetate dihydrate in ethanol 4-5 times. After every coating, the seeded substrates were heated to 350^0C for 10 min. The substrates were then immersed in the growth solution for 5-8 h at 85^0C. For the PEI modified hydrothermal process, 100 µl of 1 wt% polyethylenimine (molecular weight of 750,000 g/gmol) was added to the

growth solution prior to the immersion of the seeded substrates. The concentrations of the precursors were as high as 200 mM to realize the size tailoring effects of PEI. The seed pattern characteristics were imaged using tapping mode AFM (Nanoscope IV Multimode AFM, Veeco Instruments Inc., NY, USA) and SEM (FESEM 6700F, JEOL, Tokyo, Japan). The EDS (energy dispersive spectroscopy) studies were carried out on a JSM (5600LV) SEM (scanning electron microscopy). Samples for the transmission electron microscopy (TEM) characterization were obtained by dispersing the nanorods in water and placing a few drops of the solution on a Cu grid. The TEM images were obtained using a Philips CM300 TEM operating at 300 kV. X-ray photoelectron spectroscopy (XPS) measurements were made on a Kratos Analytical AXIS HSi spectrometer with a monochromatized Al Kα X-ray source (1486.71 eV photons) at a constant dwell time of 100 ms and pass energy of 40 eV. In peak analysis, the line width (full width at half-maximum or FWHM) for the Gaussian peaks was maintained constant for all components in a particular spectrum. FTIR spectra for ZnO nanorods were obtained on a Bio-Rad FTIR (model-400 spectrophotometer, PA, USA) with a deuterated triglycine sulphate (DTGS) detector by accumulating 1024 scans at a resolution of 4 cm^{-1} with incidence angle of 75^0. A reflectance-mode configuration was employed and a bare silicon wafer was used as the background. The sample compartment was purged with nitrogen for 15 minutes prior to carrying out the scans. UV–visible absorption spectra were recorded on a Shimadzu UV-3101 PC scanning spectrophotometer. X-Ray Diffractometer system (XRD 6000, Shimadzu, Tokyo, Japan) used in the analysis employed copper as the target with an output voltage of 40 kV and current of 30 mA. The scans were continuous with a scan speed of 3 deg/min and 1^0 divergence and scatter slit. Photoluminescence spectra were obtained using a luminescence spectrometer

(QuantaMaster, Photon Technology International, Inc., Birmingham, NJ, USA) employing a xenon flash lamp as the excitation source covering the UV-visible wavelength range. The series of excitation wavelengths was set and the corresponding emission spectra were recorded.

6.3. Results and discussion

Polyelectrolytes undergo protonization in water to become charged species. The extent of interaction of the protonized molecules with their oppositely charged counterparts can be exploited to systematically control the local reaction environment during the growth of ZnO nanorods [65]. When a polyelectrolyte such as polyethylenimine protonizes in the nutrient aqueous solution for the growth of ZnO nanorods, a part of the positively charged species wrap themselves around the lateral facets of the nanorods [248]. This offers an opportunity to control the lateral dimensions of the ZnO nanorods in-situ. This is further explained in our experiments when we modified the growth solution consisting of equimolar concentrations of zinc acetate dihydrate and hexamethylenetetramine by adding a 100 µl of 1 wt% PEI. The concentrations of the precursors were as high as 200 mM. It is well established that, as the concentration of the precursor increases, the dimensions of the nanorods formed also increases [61]. Hence, the amount of PEI added is optimized to ensure that the nanorods produced are of the same dimension (~300-320 nm) as the nanorods produced with the growth solution of concentration 0.05 M without PEI to substantiate the tailoring effect of PEI. It is possible to further reduce the size of the rods by adjusting the molar ratio of the precursors and the polyelectrolyte such that there is always the likelihood to produce ZnO nanowires of high aspect ratios [249].

Higher the concentrations of PEI, smaller would be the sizes of the ZnO nanorods and vice versa.

We attribute the size tailoring effect to the dual role played by PEI [249]. When PEI protonizes at a pH of about ~8.5, it produces the positively charged PEI molecules that aid in the formation of a zinc-amino complex which in turn reduces the supersaturation of zinc ions. All zinc ions are not readily available for the crystal growth since there is a controlled release of the zinc ions from the complex. The addition of PEI to the growth solution shifts the pH to higher values (> 8.5) and the protonized PEI being positively charged attaches itself to the lateral facets of the rods. Thus, the growth in the lateral direction is inhibited and as a result the growth velocity along the (0 0 1) facet is eventually enhanced. As the reaction proceeds, more and more of the zinc and oxygen ions are consumed in producing the crystal lattice and the pH shifts to the lower values (< 8.5) and eventually falls below the isoelectric point of ZnO (7.2). The degree of protonization decreases which causes the PEI molecules to detach from the lateral facets. By continuously monitoring the pH throughout the process, the growth can be arrested at an appropriate pH in order to obtain ZnO nanorods of desired dimensions. With this observed mechanism, we speculate that the PEI modified ZnO nanorods should have better crystal arrangement than the unmodified counterparts due to the fact that the presence of excess of Zn ions is curbed which otherwise can act as interstitial traps. To validate this hypothesis, a series of optical and structural characterizations have been performed.

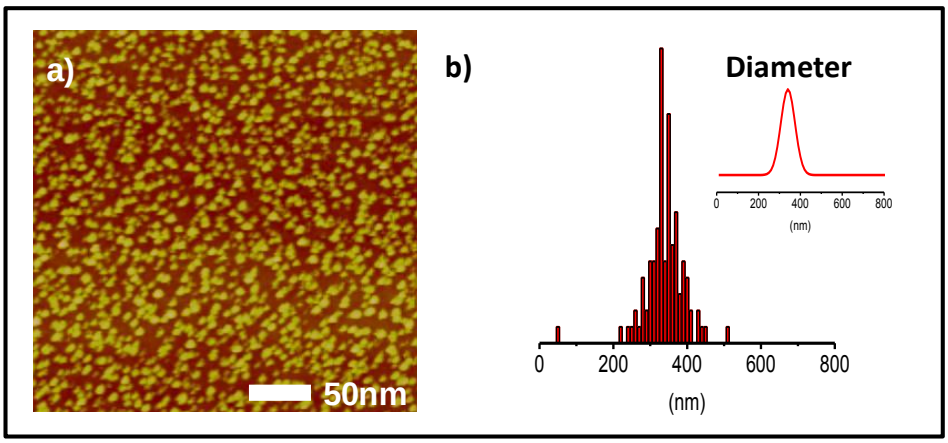


Figure 6.1 (a) AFM image showing morphology of the spincoated seed layer prior to hydrothermal synthesis of ZnO nanorods; (b) Histogram showing the distribution in the sizes of the resulting PEI modified nanorods concentrating around a single peak value of 330 nm with the corresponding gaussian fit (inset).

The AFM profile (Figure 6.1 (a)) shows the surface morphology of the spin coated seed layer that acted as the nucleation sites for the growth of the nanorods. The histogram (Figure 6.1 (b)) shows the distribution in the sizes of the nanorods (sampled on a 3 μm x 3 μm area) grown with PEI in the growth solution. The peak was concentrated at around ~330 nm and the number density of the nanorods was found to be 1.3×10^{9} cm^{-2}.

From the FESEM images of the ZnO nanorods synthesized without and with PEI (Figure 6.2), it can be observed that the nanorods formed in the latter case are quite dense, better aligned and orthogonal to the surface.

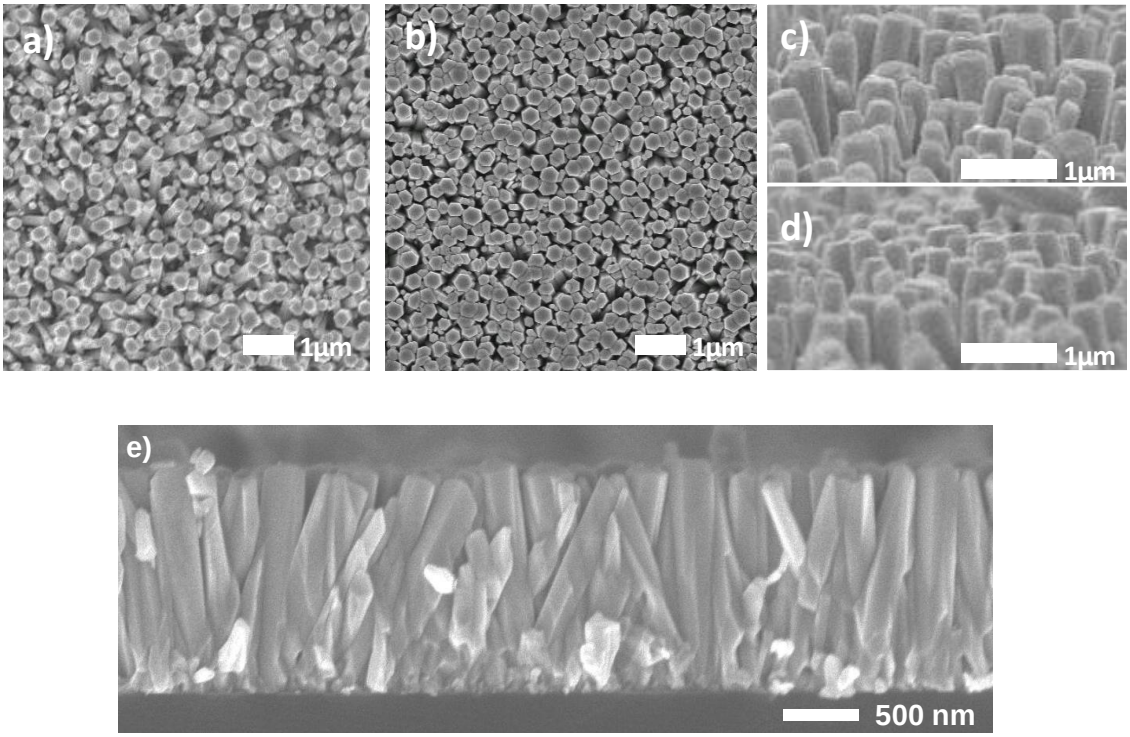


Figure 6.2 FESEM images of (a) ZnO nanorod arrays grown on Si substrate without PEI modification and (c) the corresponding tilt angle view; (b) ZnO nanorod arrays modified with PEI and (d) its corresponding tilt angle view and (e) cross section view of the PEI modified nanorods.

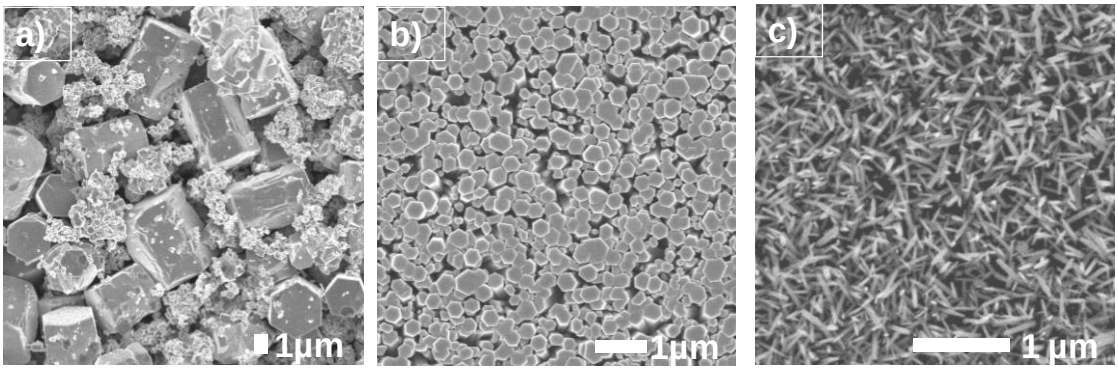


Figure 6.3 FESEM images showing the variation in the ZnO feature dimensions when (a) 25 µL (b) 100 µL (c) 200 µL of 1% PEI was added to 200 mM growth solution of hexamethylenetetramine and zinc acetate dihydrate.

The amount of PEI that is being added may also influence the dimensions of the nanorods. To validate this, we performed a control experiment by modifying the ZnO nanorods with varying quantities of PEI (25 µl, 100 µl, 200 µl of 1 % PEI) in the

nutrient growth solution. As the amount of the PEI increased for the same equimolar concentration of the zinc precursor solution, the diameter of the nanorods decreased. Thus, by varying the PEI content, the nucleation rate could be controlled and the dimensions of the rods can be tailored. When the nucleation rate is either too high (case (a) or too low case (c) in Figure 6.3, the nanorods formed are no longer orthogonal to the surface. At a certain optimized value (case (b))), the nanorods exhibit unimodal distribution in size and are orthogonal to the surface.

The lattice arrangement and d-spacing of the synthesized nanorods were obtained from HR-TEM illustrated in Figure 6.4 (a) and (b). The ZnO nanorods formed exhibited lattice spacing of 0.52 nm and the growth was predominantly in the [0001] direction. The corresponding selected area electron diffraction (SAED) patterns of the nanorods with and without PEI are shown in the inset.

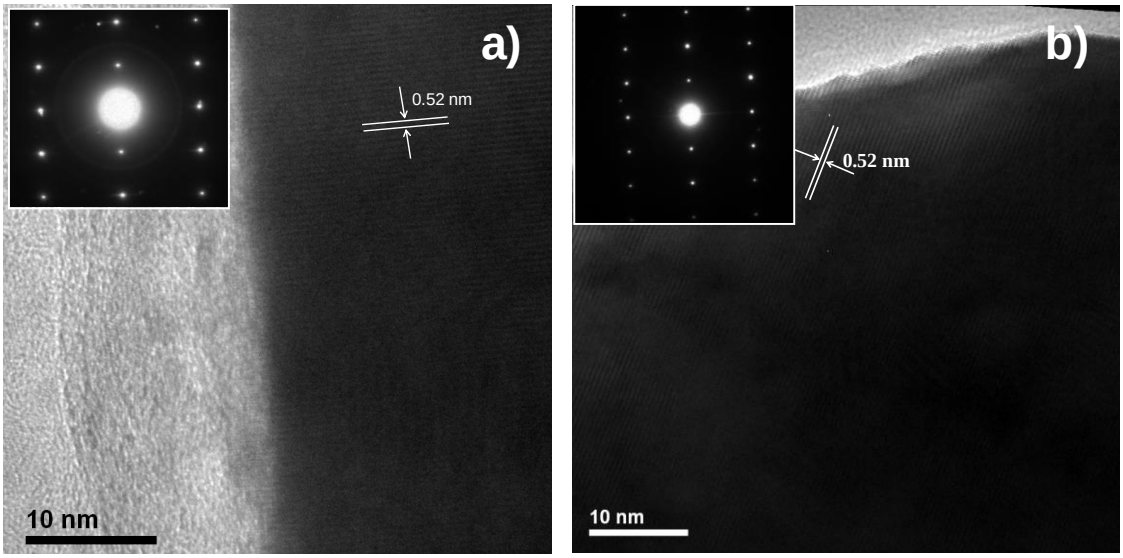


Figure 6.4 HR-TEM images of (a) hydrothermally grown ZnO NRs and (b) ZnO NRs grown by the PEI modified hydrothermal process. Their corresponding SAED patterns are shown in the inset.

To further ascertain the orientation and direction of growth of the nanorods, x-ray diffraction studies were carried out on samples without and with PEI modifications as shown in Figure 6.5 (a) and (b), respectively. In the former case, the nanorods showed growth along the c-axis; however, the (100) and (101) peaks had significant contributions. In contrast, nanorods modified with PEI also grew predominantly along the c-axis, but with negligible contributions from (100) and (101) peaks. The resulting ZnO nanorods possessed wurtzite structure and the diffraction peaks (JCPDS card No. 36-1451) was indexed to a hexagonal structure with the value for the cell constant as observed from HR-TEM analysis. From this observation, it is evident that PEI has indeed confined the growth of the nanorods to a large extent in the non-polar facets, thereby enhancing the growth primarily along the c-axis [249].

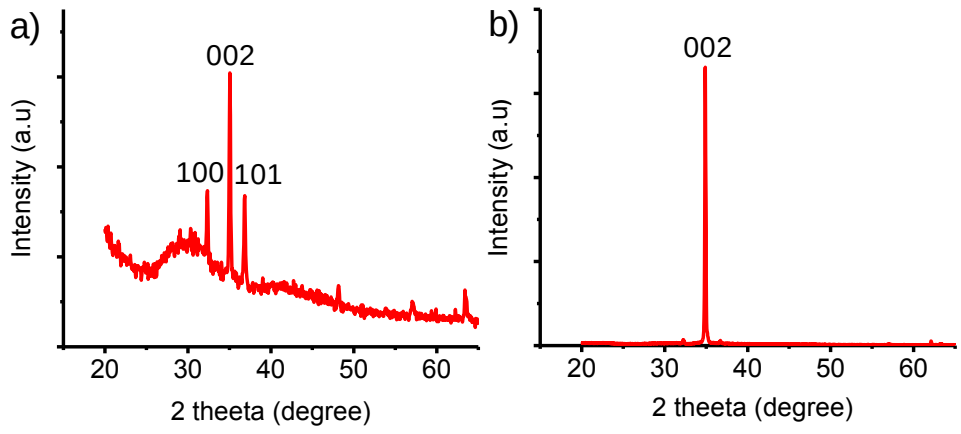


Figure 6.5 XRD patterns of (a) ZnO nanorod arrays without PEI modification and (b) ZnO nanorod arrays modified with PEI.

Since, the introduction of PEI was intentional, it was essential to check for any external contamination that might affect material properties. An EDS analysis (Figure 6.6) was performed to check the composition of the synthesized PEI modified ZnO nanorods. The results showed that there was negligible nitrogen content which

implied that the PEI had not introduced any contamination. Figure 6.6 (a) shows the localized area on which the analysis was carried out.

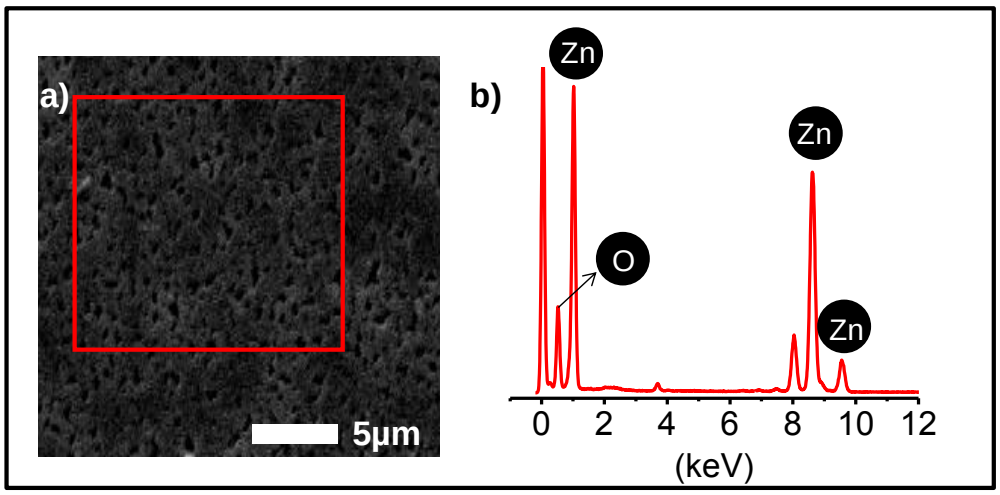


Figure 6.6 (a) and (b) Localized EDS performed on the ZnO nanorods grown using PEI.

The composition of the ZnO nanorods was examined by XPS. The XPS peaks were de-convoluted into Gaussian peaks. The peak at 1021.52 eV (Figure.6.7 (a)) corresponds to zinc in Zn-O while the peak at 530.26 eV (Figure 6.7 (b)) corresponds to oxygen in Zn-O.

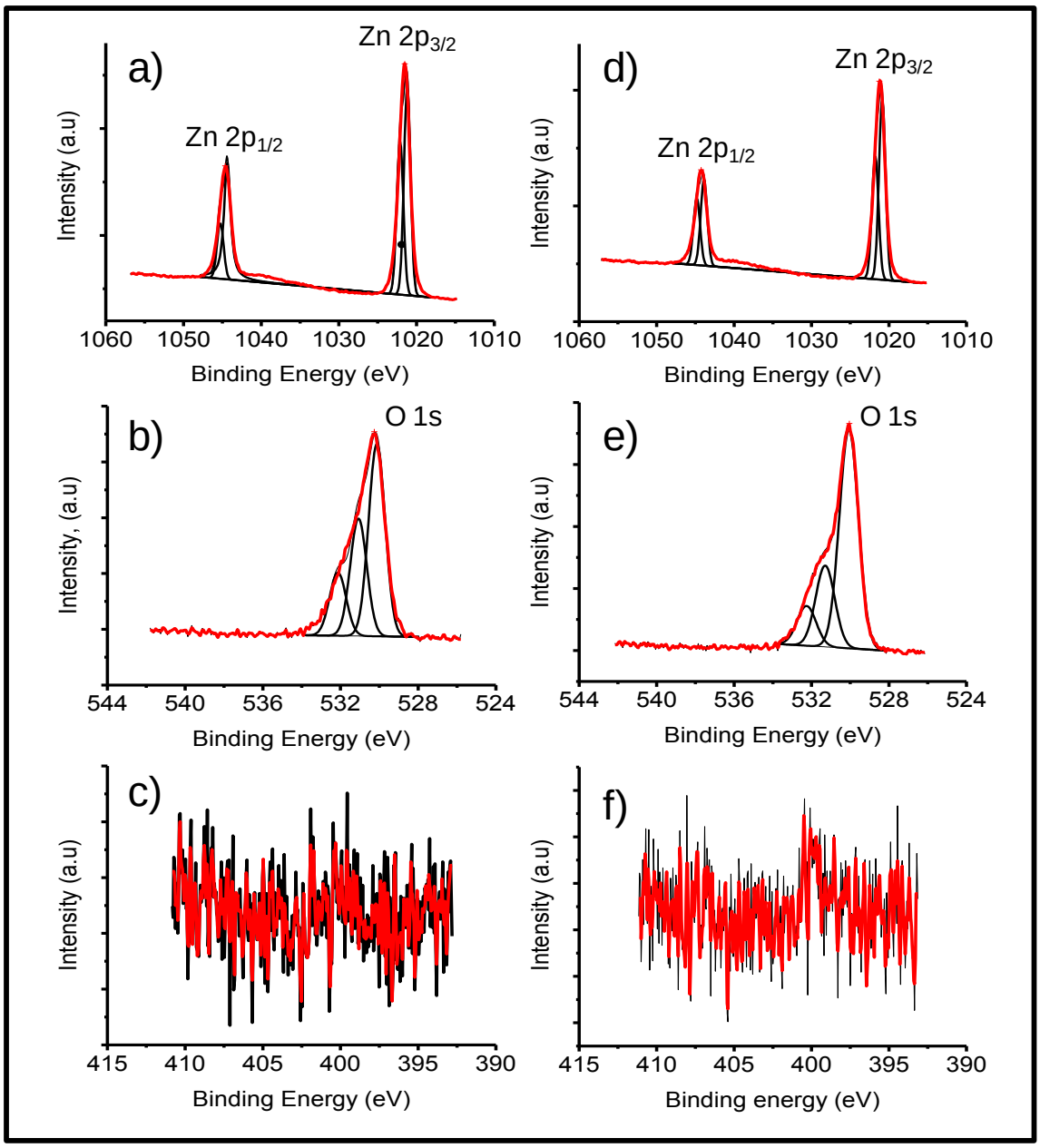


Figure 6.7 XPS spectra of (a) zinc; (b) oxygen; (c) nitrogen; in the nanorods without any PEI modification and (d) zinc; (e) oxygen; and (f) nitrogen in the nanorods with PEI modification.

For the nanorods without PEI modification, the ratio of zinc to oxygen in ZnO was calculated to be 5.65:1. For the nanorods modified with PEI the zinc to oxygen ratio was 3.85:1. The corresponding peaks for zinc and oxygen are shown in Figure 6.7 (d) and (e). Further, the absence of nitrogen peaks in all the XPS scans support the inference from the EDS results (Figure 6.6 (b)) that the PEI has not introduced any

physically adsorbed contaminants such as amine or imine in the samples. Comparing the ratios for unmodified and modified nanorods, it is further inferred that zinc ions are released in a controlled fashion [65] in the case of PEI-mediated growth, providing a better environment for crystal growth while helping in controlling the diameter of the rods formed and restricting the formation of zinc interstitial defects.

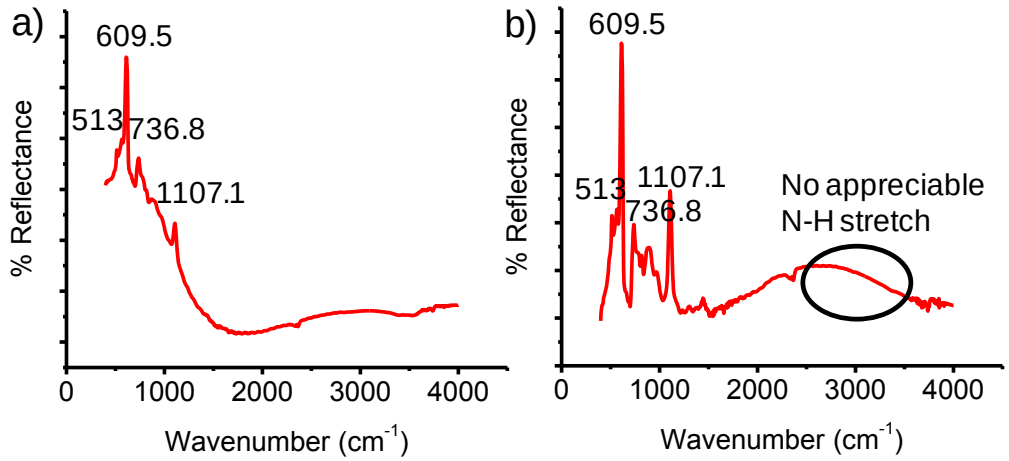


Figure 6.8 FTIR spectra of (a) ZnO nanorods grown without PEI and (b) ZnO nanorods grown with PEI in the growth solution.

The FTIR spectra for the ZnO nanorods prepared without and with PEI are shown in Figure 6.8 (a) and (b) respectively. The peak at ~513 cm^{-1} indicates the characteristic stretching frequency of Zn-O. The bending and stretching vibrations of Si-O-Si are observed at ~736.8 cm^{-1} and ~1107 cm^{-1}, respectively. In the case of nanorods modified with PEI, the typical stretching vibration of N-H bond at around ~3200 cm^{-1} [250] is not observed. This further establishes the fact that PEI is not adsorbed physically on the surface or on the facets of the nanorods and supports the inference that, during the growth process, the adsorbed PEI detached from the nanorod surface when the *p*H fell below the isoelectric point leaving no traces of it in the nanorods.

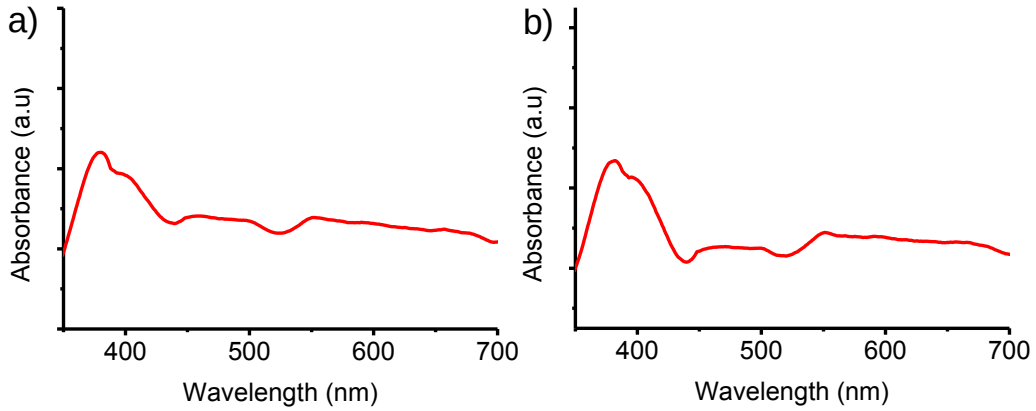


Figure 6.9 UV-Visible spectra of ZnO nanorods grown (a) without PEI and (b) with PEI in the growth solution.

The UV-Visible absorption spectra of the unmodified and PEI-modified rods are shown in Figure 6.9 (a) and (b) respectively. Both modified and unmodified nanorods showed absorption at ~380 nm which is characteristic of the hydrothermal growth technique. The room temperature photoluminescence spectra of the nanorods without and with the influence of PEI are shown in Figure 6.10 (a) and (b), respectively. The peak at ~377 nm occurs due to the exciton related recombination leading to the UV-band edge emission with energy equivalent to the band gap of ZnO. The green emission centered around ~450 nm accounts for oxygen vacancy and zinc interstitial related defects [53].

Figure 6.10 (c) and (d) show that, in contrast to the defect emission of unmodified nanorods, the green defect emission in the modified nanorods at ~450 nm is suppressed. We attribute this to the formation of good lattice arrangements during the ZnO nanorods growth due to controlled release of zinc facilitated by PEI. This

controlled release decreases the amount of freely available zinc ions and, as a consequence, the extent of interstitial defects in the crystal is highly reduced.

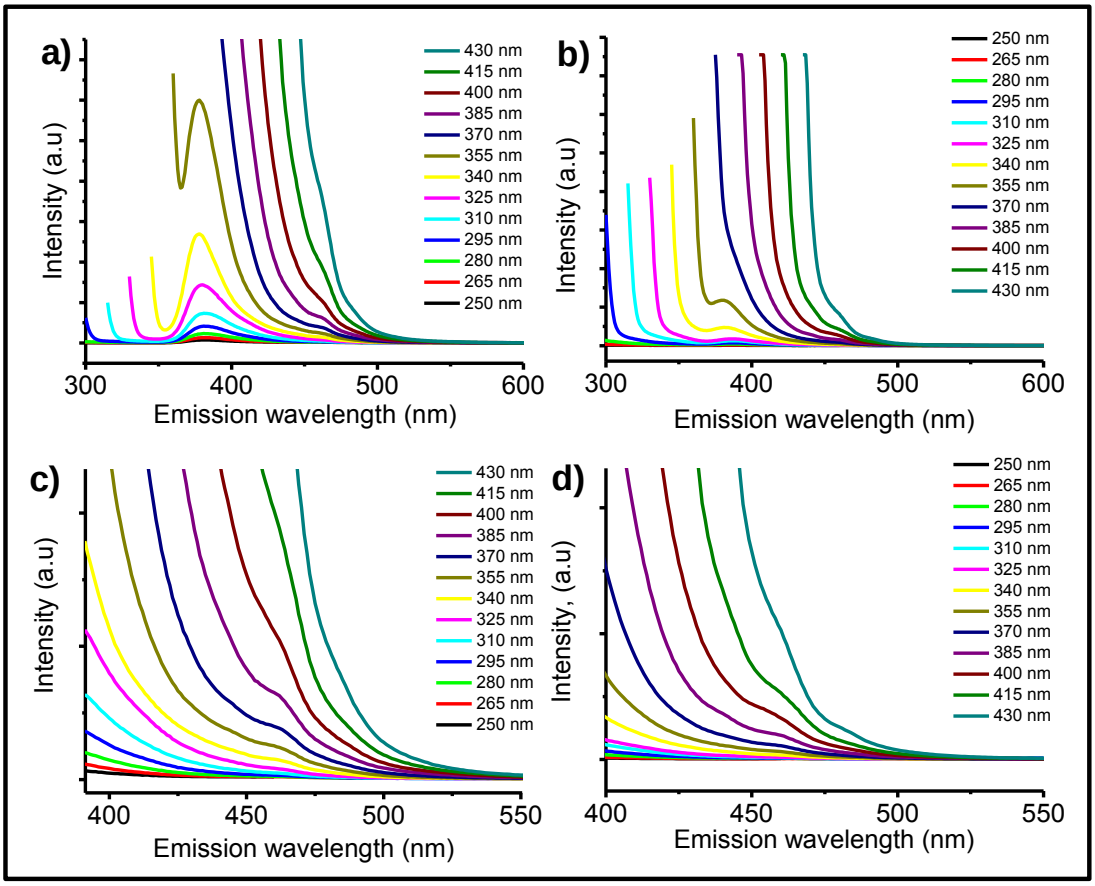


Figure 6.10 Photoluminescence spectra of ZnO nanorods grown (a) without and (b) with PEI and their respective (c) and (d) defect peaks.

In addition to tuning the sizes of the ZnO nanorods, the PEI modified ZnO nanorods exhibits good quality surface compared to its unmodified counterpart. Since the polyelectrolyte acts more like a surfactant to tailor the growth along the lateral facets of the ZnO nanorods [251], the surface and bulk properties of the modified and unmodified nanorods are expected to be different. The absorption of a material depends very much on the energy of the incident light. Therefore, the surface and the bulk can be analysed by varying the excitation wavelengths and observing the change in the absorption in the bulk and at the surface. In ZnO, which is a direct bandgap

semiconductor, excitation energy greater than the bandgap will produce more absorption at the surface as the penetration depth is smaller making it sensitive to surface effects [252]. On the other hand, when the excitation energy falls in the sub-bandgap range, the absorption is weaker and the light penetrates deeper into the sample. Here, the PL effects are dominated by bulk recombination [252]. A series of multiple excitation wavelengths and the corresponding PL spectra for the unmodified and modified nanorods are shown in Figure. 6.10 to distinguish the surface and bulk contributions.

The ratio of intensities of the UV emission (~377 nm) to visible emission (~450 nm) for different excitation wavelengths is tabulated below.

Excitation wavelength (nm)	**UV/Visible Intensity ratio**	
	Unmodified nanorods	**PEI modified nanorods**
355 (3.49 eV)	23.2	19.8
340 (3.65 eV)	16.9	12.3
325 (3.81 eV)	13.7	8.4
310 (4.00 eV)	10.7	7.4
295 (4.20 eV)	7.3	7.0
280 (4.43 eV)	6.7	13.9
265 (4.68 eV)	5.1	15.9
250 (4.96 eV)	4.8	18.5

Table 6.1 UV/Visible ratio of the emission spectra of PEI modified and unmodified nanorods for varying excitation wavelengths.

Since the PL emission spectra is obtained from the same area of the samples by varying the excitation wavelengths, rod density influencing any change in the intensity of the emission spectra can be ruled out. Thus, by varying the excitation wavelength the surface effects can be studied based on the change in the emission spectra. When the intensity of the band gap edge emission is relatively higher than the visible defect emission and is dominant, we infer that the crystals are of high quality. And when the visible emission begins to dominate, it is indicative of the presence of

defect levels. These defect levels are generally donor or acceptor levels existing near the surface of the metal oxides [53]. In the case of unmodified ZnO nanorods, with the increase in the excitation energy, the defect signals centered around 450 nm increases relative to the UV emission at ~377 nm. For the PEI modified ZnO nanorods, the variation in the UV/Visible ratio with increasing excitation energy show the visible emission peak to be greatly quenched. The peaks are dominated mainly by the UV band edge emission resulting in a gradual increase in the UV/Visible intensity ratio with increase in the excitation energy. The visible defect signal corresponds to the green emission arising out of the surface defects in the form of oxygen vacancy and zinc interstitials [53, 253]. This demonstrates the effect of PEI in providing a better quality material surface with less defects.

Intrinsic point defects in ZnO nanorod arrays act as donors and/or acceptors influencing the free charge carrier concentration, lifetime and luminescence efficiency in ZnO based opto-electronic devices. As established earlier in the XPS results (Figure 6.7), the ratio of zinc to oxygen was greater in the unmodified hydrothermal process and the resulting ZnO nanorods have a large number of defects [53, 147] in the form of oxygen vacancies and zinc interstitials in comparison to the number of defects in the PEI modified nanorods. This is further supported by the observed defect levels from the PL spectra. Since, photoluminescence emissions are sensitive to the defect states in ZnO, the signals from the visible range are likely due to existence of oxygen vacancies and zinc interstitials that act as donors giving ZnO a n-type conductivity [253]. Since the surface properties control many photo induced activities, the need to have an in-situ surface modifier such as a polyelectrolyte in a typical

hydrothermal ZnO growth is imperative to ensure a good quality surface along with tunability of features that can find applications in solid state lighting.

6.4. Conclusions

We have shown that ZnO nanorods of high density can be tailored to specified requirements with enhanced structural control by the addition of PEI. When it is required to exert a high degree of tunability and control over feature dimensions in-situ over macroscopic area, hydrothermal synthesis proves to be simple and cost effective compared to resource- and time- intensive techniques that demand clean room environments. Our detailed characterization has shown that the intentional introduction of PEI does not introduce any contamination in the samples while at the same time offering a better surface with less defects. The PL emission map of ZnO nanorods reveals their characteristic behavior of phosphors owing to the defect levels in the crystals and facilitates the differentiation between surface contributions from PEI modified and unmodified ZnO nanorods. Further, it validates the use of a polyelectrolyte to tailor the surface properties for applications that are surface sensitive in a more cost effective manner, as in light emitting diodes and sensing.

CHAPTER 7

CONCLUSIONS

Metal and metal oxide nanostructures are successfully patterned over macroscopic areas in sub-100 nm and sub-50 nm regime through top-down and bottom-up techniques. Metal oxide nanostructures, in particular, ZnO have been fabricated through both templated and non-templated approaches. While the non-templated approach of producing ZnO nanostructures helps in tuning the geometry of the features in-situ, the templated approaches confine the geometry of the resulting ZnO features as defined by the templates.

The NIL derived PMMA templates were used to direct and guide the deposition of ZnO either through RF sputtering or ALD. While PMMA template guided RF sputtering of ZnO - a top down approach to produce sub-100 nm ZnO nanoarrays, the ALD assisted pattering demonstrated the bottom-up approach. This proved the versatility of the nanoporous templates and its ability to adapt to different strategic methodologies of patterning materials. As long as the geometrical attributes of the resulting features fell within the tunable range of the protocol to meet the requirements, any metal oxides could be patterned since the NIL assisted patterning remained independent of the material that was patterned. Moreover, the nanofabrication approach benefited from combined advantages due to BCL and NIL, and in particular the re-usability of the NIL molds which in turn were derived out of BCL. The silicon nanopillar molds were used over 50 times as long as the antistiction coating remained intact without compromising the throughput or ability to generate identical pattern copy every time.

BCP-template assisted nanofabrication described various strategies to pattern ZnO through in-situ chemical decomposition of zinc precursors from ALD. This approach had the ability to produce sub-50 nm features and in future, could widely be adapted for applications in semiconductor industry where feature size scaling would be a significant demand. Moreover, the low-temperature processing involved in the fabrication sequences opens up opportunities to exploit the technique for flexible electronics. Since the micelles offer versatile functionality, the process could be readily extended to produce high-resolution sub-50 nm patterns of other material of choice grown through ALD.

In section 5.1 of chapter 5, we described the utility of the ZnO nanopatterns produced through various top-down and bottom-up approaches. We established that the densely patterned, well isolated ZnO nanoarrays are highly advantageous as potential charge storage centers for the next generation flash memory devices. The devices benefited from low power consumption operating at low voltages and scaled down tunneling oxides. Besides, we also observed that the MOS capacitor memory device exhibited improved charge retention capability by overcoming the problem of back tunneling and lateral charge leakages associated with the conventional continuous floating gate memory devices. NVM apart, the ability to create nanopatterns of ZnO and other semiconductor metal oxides widens the spectrum of application of the methodology to fabricate material patterns for use within nanoscale devices such as photovoltaics, solid state lighting.

The utility of BCP arrays does not stop with the patterning of ZnO (or metal oxide) nanoarrays. Chapter 4 explained in depth the fabrication of the hierarchically self assembled gold nanoparticle superclusters completely based and driven by self assembly approaches. Moreover, the entire process protocol was a directed layer-by-layer block copolymer self assembly process and was designed to produce complex features by tuning the material geometry and composition at every level of hierarchy. Such complexity in feature geometry was reproducible over and over again without loss of pattern quality. The statistical and geometrical measurements were well studied and analyzed. All process variables involved in the fabrication of supercluster arrays were taken into consideration and their influence over the hierarchical structure fabrication were explained. The electrostatic self assembly of Au NPs in a layer-by-layer fashion for multiplication of particle density found application in flash memory devices. The significance of the hierarchical superclusters could be realized when the test devices exhibited significant charge storage and charge retention characteristics due to the enhancement of charge storage density made possible through hierarchical arrangements, a unique feature offered by the superclusters. Furthermore, gold apart, the significance and the importance of the protocol in hierarchically pattern-designing with materials such as ZnO, TiO_2 at different levels of hierarchy widens the scope of this work beyond non-volatile memory applications. In summary, it is clear that the approach draws its benefits from the usefulness of the hierarchical assemblies in offering a high degree of control over the lateral resolutions, material composition, tunability of the geometrical attributes and interactions between the nanofeatures which can further be exploited in areas such as plasmon-plasmon, plasmon-exciton phenomena or MEMS devices.

The key benefit of employing block copolymer lithography is that it enables pattern-transfer in a highly tunable fashion using dry plasma etch to any material of choice (semiconductors, metals, metal oxides or combinations). In future, these advantages could be worked out in favour of fabricating MEMS sensors which will be discussed as an extension of the current research work in Chapter 8. The material of the sensing element being fabricated depends on what is being sensed, level of sensitivity required, concentration levels etc. In this direction, the nature of fabrication, geometry of the feature-assemblies, substrate choice and scaling (micro to nano dimensions) that are discussed in the chapters of this thesis could very well be tuned accordingly to target the desired sensing outcome.

CHAPTER 8

FUTURE RECOMMENDATIONS

Life-form on earth is an accident beyond belief. The macroscopic system in which we thrive to leave a note of our existence gets its shape by how we perceive it through eyes, i.e. sensory perception. Smallest of the smallest do co-exist amidst us but anything beyond the capability of our senses remain unnoticed and undisturbed. How so ever big the object is, it is still made up of the tiniest atoms that the human senses cannot perceive. Although they remain unseen they are the most powerful, sustaining life on earth. In fact, the eyes do fool us, not intentionally but when they fail to notice what exists beyond their perceiving capability, the technology at the nanoscale evolves. After all, the chapters in this thesis described the material fabrication at this scale.

If we now could realize the macroscopic entity in tens and hundreds of orders of magnitude lesser at the nano-dimensional scale, it's the ability to manipulate matter at the atomic level for a better tomorrow. Micro-electro-mechanical systems (MEMS) form one class of nanotechnology that manifests itself in producing varying real life art forms such as nanogears, nanointerconnects, nanoactuators and nanosensors made of semiconductors, metals or metal oxides at a miniaturized scale. Sensing or bio-sensing is one important aspects of day-today life that needs a closer attention for we live a more adulterated life style. Sensing using MEMS devices coupled with nanophotonics and plasmonics extend a great deal of promise toward sensing chemical species, metabolites, volatile organic compounds, air pollutants, radiations and adulteration in blood samples for proving grounds in biological sciences, pharmacy, quality control in consumable goods, air and water pollution monitoring and remote sensing applications.

How the MEMS sensor is fabricated and how well does it perform in delivering high sensitivity, low signal/noise ratio, high stability, high reliability and low-cost fabrication plays a crucial role in determining their success as MEMS nanosensor. From the chapters that discussed about various fabrication techniques, the two important aspects that can widely be adapted to implement and fabricate features for MEMS sensors at nano-scale are a) the top-down and b) the bottom-up approaches. In the former approach, the nanopatterns are fabricated in a template-guided approach involving selective deposition of materials through sputtering or physical vapour deposition by employing advanced nanoimprint lithography. The latter, typically involves the fabrication processes such as molecular self assembly, surface selective growth and epitaxy achievable through block copolymer lithography. Block copolymer self assembly allows scaling down to sub-20 nm and below, and also offers the advantage of macroscopic patterning without much compromise on the feature geometry and distribution.

As a potential sensing device, MEMS fabrication can be expected to employ block copolymer self assembly processes that would produce the basic quasi-hexagonal polymeric template for pattern-transfer into 1) metal nanocluster arrays, 2) metal or metal oxide or semiconductor arrays with tunable morphology or 3) Hybrid nanoarrays offering a combination of metal or metal oxide or semiconductor depending on the end-requirement. Given the scenario that the fabrication protocols and their geometry tunable aspects are well studied, preliminary investigations on their plasmonics properties crucial to sensing would extend a great deal of promise toward preparing them as MEMS nanosensors.

The critical feature dimensions and other geometric attributes of MEMS sensors can vary from several nanometers to micrometers, and so are the morphology of patterns which can either be simple dot patterns or complex features for extreme electromechanical systems. Block copolymer self-organization promises positional control for assembly of patterns on substrates offering the advantage to fabricate almost any structure, be it simple or complex or hybrid, and deliverable micro-nano-patterns at the molecular level for high degree of sensitivity. Perhaps, what is most attractive and novel will be the combined merits offered by the techniques that include increased performance and capabilities, scaling or miniaturization of building components pushed till the very end of the spectrum of magnitude and increased functionality offered by the hybrid material organization.

Health care ensures quality life and increases life expectancy. It has always been crucial and of late, is of prime importance given the current of style of living, environment, food quality, air quality etc. In this direction, any research that is performed in closely monitoring the aforementioned factors to ensure good and safe livings conditions will receive an overwhelming support. Thus, the proposed future work would throw light on quality control and regulates the supply chain exploiting wide range of sensing modalities. In the past few years, MEMS technology has widely been studied and researchers have demonstrated many different kinds of micro-nano-devices fabricated for different sensing functionalities. Remarkably, arriving at the right nanofabrication design and control over the geometric attributes for the right kind of sensing has been the major target to demonstrate performances bettering the existing microsensors. This leaves a huge impact when the level of

sensitivity achieved at the nanoscale causes significant effects in a macroscopic system as a result of execution of proper design rules in nanopatterning and fabrication of sensing elements.

Not only MEMS nanosensors can outperform the existing bulk counterparts, but their style of fabrication translate into reduced uni-device manufacturing costs resulting in reduced load in consumer procurement. Although, it is inevitable that there is often a trade-off between the key performance variables from the technical standpoint such as the degree of sensitivity and reproducibility and socio-economic aspects such as cost and consumer apprehension, it is imperative to develop such techniques for a better living.

A roadmap to successively carry out the compelling steps in realizing a potential MEMS sensor start when the up-stream processes involved in fabricating miniaturized micro-nano-sensors meet the down-stream end of product validation sensing target-species. Machining at nanoscale and framework of sensing components using dry plasma etch or pattern transfer methodologies with possible integration with plasmonics ensures high degree of understanding of the behavior of the micro-electro-mechanical systems in depth together with their ability to sense. While the sensing modalities are always available in the environment around us, a proper MEMS device-design implementation and interpretation of the results in a more deterministic approach throw light for continuous improvement in the fabrication designs and their influence in sensing the target species. Furthermore, each of the MEMS nanosensors is specific to target-species and hence fabrication geometry and functionality of the devices are target-species dependent. With the proposed protocols being tunable in

more than one way, commercialization would be more toward a batch production rather than bulk manufacturing throwing open the possibility for a full-fledged lab-on-a-chip to be realized.

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Appendix 1

List of publications

1. V. Suresh, M. P. Srinivasan, S. Krishnamoorthy, "Hierarchically built hetero superstructure arrays with structurally controlled material compositions", **ACS-Nano**, ***2013*** **(Accepted).**

2. V. Suresh, S. H. Meiyu, M. P. Srinivasan, S. Krishnamoorthy, "In-situ synthesis of high density sub-50 nm ZnO nanopatterned arrays using diblock copolymer templates", **ACS-Applied Materials and Interfaces**, *5* (12), pp 5727–5732***, 2013***.

3. V. Suresh, J. Sundaramoorthy, M. Iskhandar, M. P. Srinivasan, "In-situ application of polyelectrolytes in ZnO nanorod synthesis: understanding the effects on structural and optical characteristics", **Elsevier-Journal of Colloid and Interface Science**, *394* (0), 13-19, ***2013***.

4. V. Suresh, S. H. Meiyu, M. P. Srinivasan, S. Krishnamoorthy, "Robust, High Density Zinc oxide Nanoarrays by Nanoimprint Lithography-Assisted Area Selective Atomic Layer Deposition", **ACS-Journal of Physical Chemistry C**, *116* (44), pp 23729–23734, ***2012***.

5. V. Suresh, S. H. Meiyu, M. P. Srinivasan, S. Krishnamoorthy, "Macroscopic high density nano disc arrays of Zinc oxide fabricated by block copolymer self-assembly assisted nanoimprint lithography", **RSC-Journal of Materials Chemistry**, *22* (41), 21871-21877, ***2012 (highlighted as 'hot article' by the editor-http://blogs.rsc.org/jm/2012/10/19/hot-paper-nanodisc-arrays-of-zno-from-block-copolymer-self-assembly-and-nanoimprint-lithography/).***

6. V. Suresh, D.Y. Kusuma, P.S. Lee, M. P. Srinivasan, S. Krishnamoorthy, "Enhancing the memory performance of flash memory devices through hierarchically built gold nanoparticle supercluster arrays" **(Submitted).**

Patents filed

1. **Methods to Form Substrates for Optical Sensing by Surface Enhanced Raman Spectroscopy (SERS) and Substrates Formed by the Methods**. Inventors: F.L. Yap, P. Thoniyot, S. Krishnamoorthy, V. Suresh, S.Dinda. **Patent no. (US): 13/588,635.**

Conference proceedings

1. Vignesh Suresh, Huang Meiyu Stella, M.P.Srinivasan, Sivashankar Krishnamoorthy "**High density metal oxide (ZnO) nanopatterned platforms for electronic applications**", Proceedings of Symposium 'S', Volume 1498, 2013 - MRS Fall Meeting, Boston, Massachusetts, 25-30 Nov, **2012.**

Conference presentations

1. Vignesh Suresh, M.P.Srinivasan, Sivashankar Krishnamoorthy, "**Self-assembly derived hierarchical super-cluster arrays with structurally controlled hybrid material compositions**" – oral presentation at ICMAT, Singapore, 30 June-5 July, **2013.**

2. Vignesh Suresh, Huang Meiyu Stella, M.P.Srinivasan, Sivashankar Krishnamoorthy, "**High density metal and metal oxide nanopatterned platforms for optoelectronic applications**" – oral presentation in symposium 'S' of 2012 MRS Fall Meeting, Boston, Massachusetts, 25-30 Nov, **2012.**

3. Vignesh Suresh, Huang Meiyu Stella, M.P.Srinivasan, Sivashankar Krishnamoorthy, "**Fabrication of high density sub-100nm disc arrays of zinc oxide using nanoimprint lithography assisted templates**" – oral presentation at M3 International conference, Singapore, 9-11 January, **2012.**

4. Vignesh Suresh, M.P.Srinivasan, Sivashankar Krishnamoorthy, "**Fabrication of Semiconductor Nanostructures using Templated and Non-Templated Approaches for Application in Flash Memory Devices**" – oral presentation at ICMAT, Singapore, 26 June-1 July, **2011.**

5. Vignesh Suresh, M.P.Srinivasan, Sivashankar Krishnamoorthy, "**Controlled and uniform growth of ZnO nanorods over macroscopic areas using templated and non-templated approaches**" – poster presentation at M3 International conference, Singapore, 10-11 January, **2011.**

Appendix 2

	57k-57k (114k) control									
No of clusters per μm^2		=	113							
No of charge carriers per cluster		**=**	**28**							
No of AuNP per cluster		=	18							
No of charge carriers per Au NP		=	1.6							
	190k-190k (380k) control									
No of gold features per μm^2		=	21							
No of charge carriers per gold feature		**=**	**231**							
	Supercluster									
No of 380k gold features		=	21							
No of AuNP per 380k gold		=	17							
No of 114k clusters per μm^2		=	115							
No of AuNP per 114k cluster		=	18							
one supercluster		=	1	380k gold	+	5.48	114k	+	17	Au NP on top of 380k
one supercluster		=	1	380k gold	+	98.57	114k derived Au NP	+	17	Au NP on top of 380k
one supercluster		=	1	380k gold	+	115.57	of total Au NP			

From SC with Au NP-real scenario,

	A total of	**1.63E+08**	**charge carriers are present in**		**1.55E+08**	**Au NP of the entire supercluster**	
Therefore,		1.22E+02	charge carriers are present in		115.6	of Au NP corresponding to one supercluster	
Hence, no of charge carriers per supercluster			=	231	380k gold	+ 1.22E+02	from Au NP
			=	**352.62**	charge carriers per supercluster		
	One supercluster contains			352.62	charge carriers		
from control		1	380k	contains	231		
from control		5.48	114k will	contain	153.33		
				Total	**384.33**	no of charge carriers per supercluster from controls	

This already exceeds the original no of charge carriers per supercluster (without including no of charge carriers stored in Au NP on top of 380k)

Per feature	**No. of charge carriers**
114 k (control device data)	28
380k (control device data)	231

supercluster (device data)	353
supercluster (as estimated from 114k and 380 control not inclusive of charge carriers stored by Au NP on top of 380k)	384
Deficit	31