REAL-TIME MONITORING AND CONTROL OF CRITICAL DIMENSIONS IN LITHOGRAPHY

YANG GENG

A THESIS SUBMITTED

FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

DEPARTMENT OF ELECTRICAL AND COMPUTER

ENGINEERING

NATIONAL UNIVERSITY OF SINGAPORE

2012

DECLARATION

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Yang Geng

24 December 2012

Acknowledgments

I am grateful to many people for supporting me not only intellectually but also mentally and socially in my work and life besides work. These acknowledgements can only give a glimpse on how much I benefit and learn from all my mentors, colleagues, friends, and family. Thanks so much to all of you.

First of all, I wish to express my sincere gratitude to my supervisor Assoc. Prof. Arthur Tay, who supplies me with invaluable advice and guidance throughout my time at university concerning my research, writing, organization, and life. His insights in the semiconductor process control are always stimulating and many chapters of this thesis are shaped by the numerous discussions between us.

I also would like to thank my friends and colleagues who are working in the Advance Control Technology Lab. Their friendship, advice and encouragement make my experience at National University of Singapore unforgettable in my life. Special thanks are going to my parents and my wife for their companion and love. I would have never reached so far without their constant encouragement and support.

Contents

Summary

Lithography is a key enabler accounting for a third of IC manufacturing costs. Critical dimension (CD) is the most important variable in the lithography sequence affecting the speed of the circuit. Current approaches to CD control are primarily based on a run-to-run strategy due to a lack of in-situ sensors and control authority. In this thesis, we proposed an approach to conduct real-time CD monitoring and control. It is well-known that temperature has a direct effect on CD. First, a multi-zone programmable thermal processing system is developed, which is able to control the wafer temperature uniformity during the entire thermal cycle. Next, an in-situ ellipsometry system is established and integrated into the thermal process to measure the CD profile in real-time. Compared with the state of art in current semiconductor manufacturing based on a run-to-run strategy, the proposed real-time control system is capable to monitor and control the CD across wafer in real-time. Experimental results demonstrate that the real-time control system improves the across wafer CD uniformity more than 60% versus a run-to-run approach.

List of Tables

List of Figures

List of Acronyms

ADL	Acid Diffusion Length
AFM	Atomic Force Microscopy
CD	Critical Dimension
CDU	Critical Dimension Uniformity
DAQ	Data Acquisition
DI	Deionized
DICD	Develop Inspect Critical Dimension
DRAM	Dynamic Random-Access Memory
EUV	Extreme Ultraviolet Lithography
HMDS	Hexamethyl Disilazane
IC	Integrated Circuit
IO	Input/Output
ITRS	International Technology Roadmap for Semiconductors
KPI	Key Performance Indexes
LER	Line-Edge Roughness
MIMO	Multi-Input-Multi-Output

ML2 Mask Less Lithograph

MSE Mean-Square-Error

NI National Instrument

NIR Near Infrared

PAC Photoactive Compound

PEB Post-exposure Bake

PI Proportional-Integral

PWM Pulse Width Modulation

RGA Relative Gain Array

RTD Resistance Temperature Detector

R2R Run-to-Run

RCWA Rigorous Couple-Wave Analysis

SEM Scanning Electron Microscope

SPC Statistical Process Control

SSR Solid State Relay

TE Transverse Electric

TM Transverse Magnetic

UV Ultraviolet

VIS Visible Light

List of Symbols

α_0	thermal diffusivity of fluid
β_0	volume thermal expansion coefficient of fluid
Δ	phase shift
$\Delta\Omega$	change of spin speed
ΔT_{p1}	change of temperature of the bake-plate center
ΔT_{p2}	change of temperature of the bake-plate edge
ΔT_{w1}	change of temperature of the wafer center
ΔT_{w2}	change of temperature of the wafer edge
Δu_1	change of power input to the bake-plate center
Δu_2	change of power input to the bake-plate edge
δ	factor constant
λ	wavelength
μ	kinematic viscosity
μ_0	initial kinematic viscosity
Ω	spin speed
Φ_f	refracted angle

Φ_i	incident angle
Ψ	the angle of the first diagonal of the rectangle in which the ellipse is enclosed
ρ	density
ρ_c	state of polarization
σ	acid diffusion length
θ	variable angle
ζ	radiation dose
ζ_{eff}	effective dose
A	analyzer angle
A_0	Arrhenius constant
A_e	pre-exponential factor
A^{side}	contact area between the adjacent element
A_h^{bottom}	area of the bottom of the heater exposed to the ambient
A_w^{top}	area of the wafer top exposed to the ambient
A_x	analyzer matrix
C	thermal capacitance
C_0	solute concentration at the free surface of the thin film
C_A	concentration of species A
C_{ag}	thermal capacitance of air gap
C_c	thermal capacitance of cartridge
C_h	thermal capacitance of heater
C_p	thermal capacitance of bake-plate

C_w	thermal capacitance of wafer
$CDVar_{bake}$	CD variations caused by bake
$CDVar_{coat}$	CD variations caused by spin coating
$CDVar_{develop}$	CD variations caused by development
$CDVar_{expose}$	CD variations caused by exposure
$CDVar_{total}$	total CD variation
c_0	initial concentration of solid species in the photoresist
c_v	specific heat capacity
D	diffusion coefficient
D_0	initial diffusion coefficient
D_c	decoupling matrix
d	depth of fluid layer
E_0	power of the light source
E_a	activation energy
E_d	field amplitude on the detector
E_x	sample matrix
e_1	difference at the wafer center
e_2	difference at the wafer edge
$G_{bp-to-u}$	transformation matrix between bake-plate and power input
$G_{new,wfr-to-u}$	new transformation matrix between wafer and power input
$G_{wfr-to-u}$	transformation matrix between wafer and power input
g	acceleration of gravity

H final coating thickness

h convection coefficient

h^{top} wafer top convection coefficient

h_0 initial thickness of fluid

h_1 film thickness

h_c coating film thickness

h_l the l-th layer film thickness

I intensity seen by detector

K_i integral gain

K_p proportional gain

K_{p1} real-time control constant parameter for center zone

K_{p2} real-time control constant parameter for edge zone

k thermal conductivity

k_c rate constant of the chemical reaction

k_m mass transfer coefficient

k_r amount of absorption loss

L effect of the lamp source

L_0 characteristic length

l_p proximity pin height

M molecular weight of the solvent

m constant factor

N_r phase speed

$\overline{N}_u$	Nusselt number
n	complex refractive index
n_1	Cauchy coefficient
n_2	Cauchy coefficient
n_3	Cauchy coefficient
P	polarizer angle
P_v	vapor pressure of the pure solvent
P_x	polarizer matrix
Pr	Prandtl number
p	signature bottom position
p_r	reference bottom position
q^{input}	heater power
q_1	heater power to center
q_2	heater power to edge
q_{ag}^{bottom}	heat flow into the air gap element from bottom surface of air gap
q_{ag}^{in}	heat flow into the air gap element from inner zone of air gap
q_{ag}^{out}	heat flow into the air gap element from outer zone of air gap
q_{ag}^{top}	heat flow into the air gap element from top surface of air gap
q_c^{bottom}	heat flow into the cartridge element from bottom surface of cartridge
q_c^{in}	heat flow into the cartridge element from inner zone of cartridge
q_c^{out}	heat flow into the cartridge element from outer zone of cartridge
q_c^{top}	heat flow into the cartridge element from top surface of cartridge

q_h^{bottom}	heat flow into the heater element from bottom surface of heater
q_h^{in}	heat flow into the heater element from inner zone of heater
q_h^{out}	heat flow into the heater element from outer zone of heater
q_h^{top}	heat flow into the heater element from top surface of heater
q_p^{bottom}	heat flow into the bake-plate element from bottom surface of bake-plate
q_p^{in}	heat flow into the bake-plate element from inner zone of bake-plate
q_p^{out}	heat flow into the bake-plate element from outer zone of bake-plate
q_p^{top}	heat flow into the bake-plate element from top surface of bake-plate
q_w^{bottom}	heat flow into the wafer element from bottom surface of wafer
q_w^{in}	heat flow into the wafer element from inner zone of wafer
q_w^{out}	heat flow into the wafer element from outer zone of wafer
q_w^{top}	heat flow into the wafer element from top surface of wafer
Q_T	total exposure dose
R	universal gas constant
R_x	rotation matrix
Ra	Rayleigh number
r	fluid thin film radius
r_i	distance between the elements i and $i+1$
r_p	reflectivity of TM wave
r_s	reflectivity of TE wave
T	temperature
T_a	edge element temperature above ambient

T_{ag}	temperature of air gap above the ambient
T_{ag1}	temperature of air gap center above the ambient
T_{ag2}	temperature of air gap edge above the ambient
$T_{bp1setpoint}$	bake-plate center set point
T_c	temperature of cartridge above the ambient
T_{c1}	temperature of cartridge center above the ambient
T_{c2}	temperature of cartridge edge above the ambient
T_h	temperature of heater above the ambient
T_{h1}	temperature of heater center above the ambient
T_{h2}	temperature of heater edge above the ambient
T_p	temperature of bake-plate above the ambient
T_{p1}	temperature of bake-plate center above the ambient
T_{p2}	temperature of bake-plate edge above the ambient
T_s	sampling time
T_w	temperature of wafer above the ambient
T_{w1}	temperature of wafer center above the ambient
T_{w2}	temperature of wafer edge above the ambient
t	time
$\tan\Psi$	amplitude ratio upon reflection
u	control signal
u_1	control signal to center zone
u_2	control signal to edge zone

w_1	the CD latent image linewidth
w_l	the CD latent image linewidth at l-th layer
x_0	mole fraction of the solvent
z	thickness
$z_{ag,max}$	maximum air gap thickness
$z_{ag,min}$	minimum air gap thickness
z_{ag1}	air gap thickness at center zone
z_{ag2}	air gap thickness at edge zone

Chapter 1

Introduction

1.1 Motivation

The continuing down-scaling of the transistor printed on the silicon wafer has been driven principally by the demand for the faster and larger scale integrated circuit (IC). According to the Moore's Law, the number of transistors that can be placed inexpensively on an IC increases exponentially, and it approximately doubles for every two years [1]. This law has continued for almost half a century until now and is not expected to stop for another decade at least. The trend can be clearly observed from Figure 1.1 [2].

Lithography is the most critical step for IC fabrication. It aims to transfer the pattern from the inscribed mask to the respective layer on wafer with stringent requirements for photoresist parameters and overlay control. Lithography accounts for a third of the total manufacturing costs [3]. It also acts like a technical ceiling for chip size further reduction es-

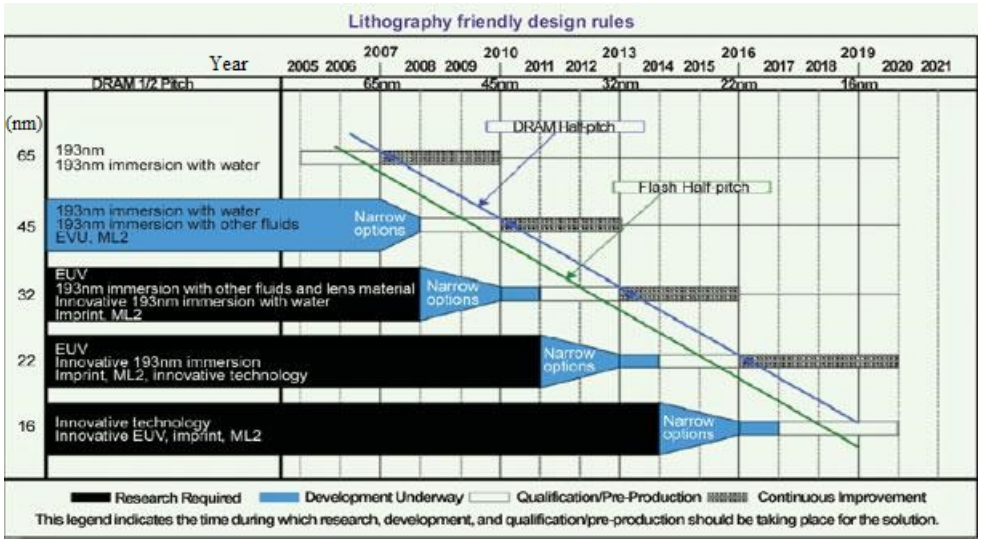

Figure 1.1: Transistor density and minimum feature [2]

pecially when the technology advances to nanometer scale. This motivates researchers to do a lot of works in lithography process control for cost reduction and technology advancement. A typical lithography process is stated in Figure 1.2. The lithography sequence starts with a priming step to promote adhesion of the polymer photoresist material to the substrate by hexamethyl disilazane (HMDS) baking. After that, the photoresist is spun coated on the wafer substrate by using centrifugation force. Soft-bake is then conducted to evaporate the residual solvent and relax the stress of film generated by coating. Thereafter, the wafer is sent for radiation exposure through a patterned mask to create the latent image in the resist film. Once the exposure is completed, post-exposure bake (PEB) is performed to reveal those patterns latently existed in the photosensitive layer through a series of catalytic reactions. For the positive photoresist, the bake enables the thermal activation of deprotection reaction which eliminates the disso-

lution inhibitor presented along the resist polymeric chain for the exposed area. After that, the lithography process comes to the last step, i.e. the development step. The exposed region becomes soluble in the developer solution and can be easily stripped away, revealing the three-dimensional resist pattern or develop inspect critical dimension (DICD).

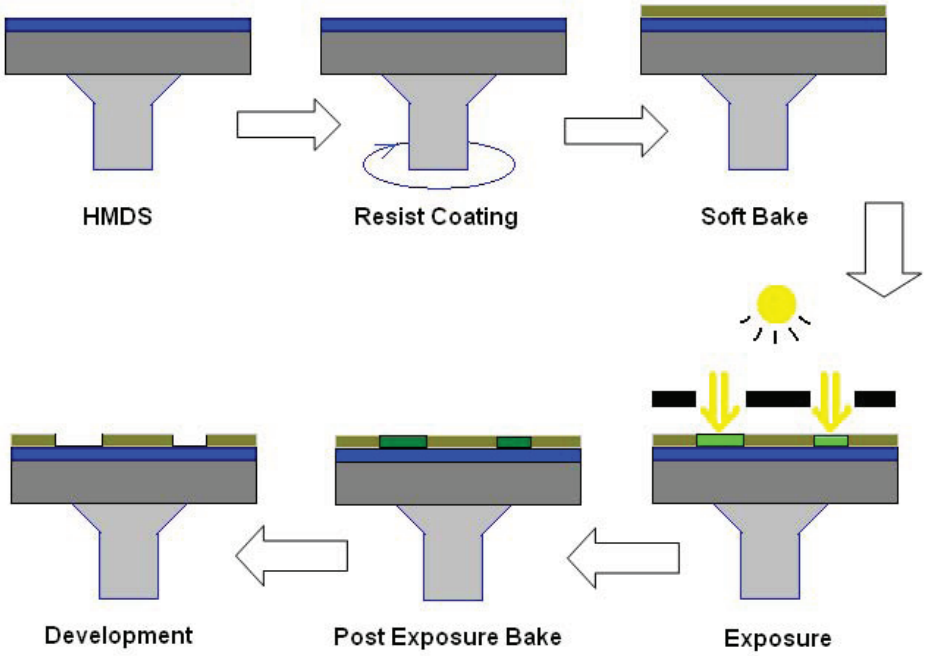

Figure 1.2: Microlithography sequence

Critical dimension (CD) is the most important variable in lithography, defining the speed of the microprocessor. It describes the minimum half pitch resolvable for a diffraction limited optical projection system and mainly depends on the photoresist properties, equipment design, mask pattern adjustment, and process control. CD is considered so central to integrated circuit fabrication that industry calls each generation of the process after a dimension. The fact shows that the performance of an IC is highly

assessed by the CD of the patterned feature on the photoresist layer. Some key performance indexes (KPI) such as gate delay and drive current are even inversely proportional to the gate length which is determined by CD. It is estimated that 1 nm CD variation in channel is equivalent to 1 MHz chip-speed variation and thus worth about $ 7.50 in the chip's unit selling price [4]. Therefore, it is of great importance for precise monitoring and control of CD during the lithography process.

Steele et al. [5] attributed CD variations to all the process steps through lithography, which is shown in Figure 1.3. Assuming the significant variables in CD variance are independent. The combined contribution can be stated as

$$CDVar_{total}^2 = {CDVar_{coat}}^2 + {CDVar_{develop}}^2 + {CDVar_{bake}}^2 + {CDVar_{expose}}^2 + \ldots \tag{1.1}$$

where $CDVar_{total}$ is the total CD variation caused by the whole process, $CDVar_{coat}$, $CDVar_{develop}$, $CDVar_{bake}$, and $CDVar_{expose}$ are the CD variations caused by spin coating, development, bake, and exposure steps, respectively.

The down-scaling of the transistor size for the next decade is summarized in Table 1.1 by International Technology Roadmap for Semiconductors (ITRS) [2]. It shows approximate 30% CD linewidth reduction for every two to three years. The performance of the IC chip is directly related to the result of CD. As the CD linewidth continues to shrink, its variation tolerance also reduces, resulting in the tighter uniformity specifications to maintain the satisfied chip performance. To meet such stringent

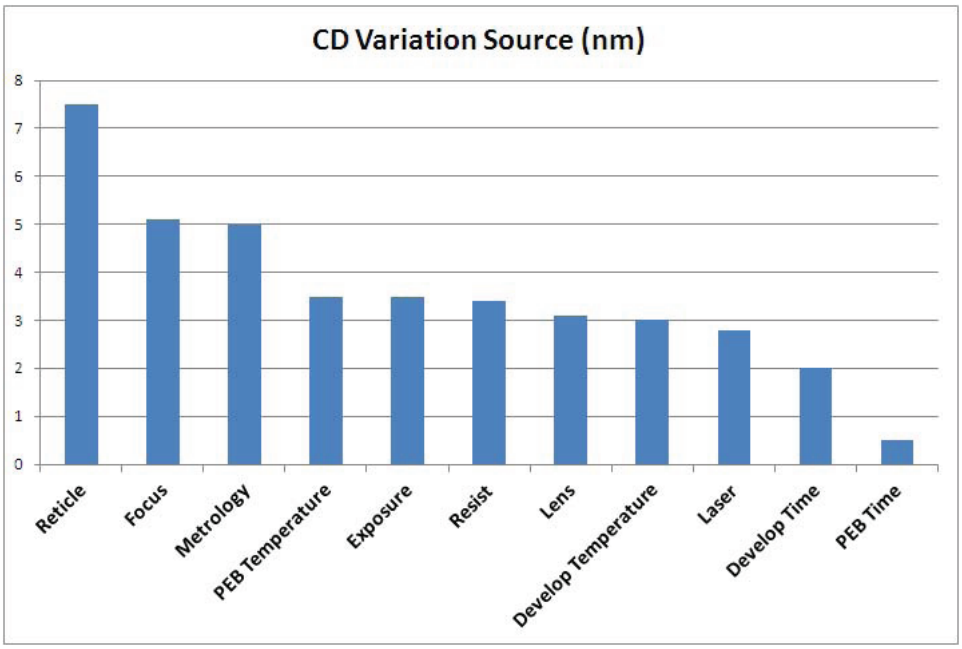

Figure 1.3: Source of CD variation [5]

specifications for CD, advanced control technologies are highly demanded for the lithography process. Especially when the channel length of a transistor shrinks to sub-100 nm, an adequate and econ-friendly lithography process technology becomes an increasingly challenging task.

Table 1.1: Lithography technology requirements for the next decade

Year of Production	2012	2013	2014	2015	2016	2017	2018
DRAM 1/2 pitch (nm)	32	28	25	23	20	18	16
CD control (3 sigma) (nm)	3.3	2.9	2.6	2.3	2.1	1.9	1.7

In the literature, thermal processing system is commonly used for photoresist processing in the lithography, and it is usually applied at the PEB step. Investigations in [6] showed that the variation in gate CD for the PEB process generally ranged from 3 to 7 nm/°C. Conventional baking is the mainstream for current semiconductor manufacturing, which a hotplate of large thermal mass is maintained at a constant temperature by a

feedback controller [7]. Because of the large thermal mass and sluggish dynamics, conventional baking system demonstrates great robustness to the temperature fluctuations and loading effects. However, these characteristics make conventional baking system misfit for the process control with tight tolerance. Moreover, conventional hotplate design also has hardware constraints for across wafer temperature control which is a source of across wafer process variation. Some novel programmable thermal processing systems have been developed in the last decade to address these issues. Tay et al. modelled and built a multi-zone thermal processing system in [8] and further extended in [9] which greatly enhanced the across wafer temperature uniformity at both transient and steady states by performing in-situ real-time power input control. In [10], the authors proposed a real-time photoresist extinction coefficient uniformity control algorithm with an array of spectrometers positioned above the bake-plate for in-situ parameters measurement. Subsequently, an in-situ real-time photoresist thickness and extinction coefficient control scheme was demonstrated in [11]. Similar research results were presented in [12] for the analysis of die-to-die CD uniformities. Differently, T. Tomita [13] also reported a CD uniformity (CDU) improvement technology with wafer warpage control oven for high volume manufacturing. The utilization of these novel designed thermal bake-plates allows more flexibility for thermal control in the lithography process.

Besides thermal bake-plate, researchers have also paid considerable attentions to the development of metrology tools. Scanning electron microscope (SEM) and atomic force microscopy (AFM) are the main CD metrol-

ogy tools in the current semiconductor manufacturing. However, both of them can only measure the CD after the lithography process is completed. If the CD measurements are out of the limits and the rework is not allowed, the wafers have to be scrapped. It may waste thousands of dollars. Moreover, the recipe of the lithography process has also been updated on the basis of the current CD measurement. It may not be suitable for the next batch of wafers which may have different incoming conditions. To tackle these approach obstacles, the concept of the real-time photoresist properties monitoring and control through the lithography process is introduced and developed by researchers. An exploration of the real-time control system is presented in this thesis.

1.2 Review of Process Control for Lithography

Automated process control in semiconductor manufacturing grows increasingly due to the economic impact of efficiency and reproducibility. In lithography, automated inspection techniques such as ellipsometry allow operator to easily monitor the process and identify the equipment malfunction when the fault occurs. However, process engineer also expects an intelligent system which can recover the fault efficiently more than just inspection. Over the last decade, the desire for better automated process control has engendered a series of technology breakthroughs in advanced process control. This section will review some of them.

1.2.1 Statistical process control

In manufacturing, the quality of a product is traditionally guaranteed by the post-manufacturing inspection. Each product may be accepted or rejected according to how well it meets the designed specifications. Variation is present in every process and can be categorized as either a common cause or an assignable cause. Process result exhibits that natural or common cause variation may form a bell-curve distribution. For these types of processes, a quality control method statistical process control (SPC) is proposed to ensure the production line running at full potential with minimum waste. The basic concept in SPC is the control chart which has an upper limit and a lower limit based on the acceptable process variation. The control chart is used to compare the measured data with a known distribution of data from an in-control process. For all the measured data within the limits, the products are characterized as qualified products. By using the most popular 3-sigma method in manufacturing industry, the confidence on quality is up to 95%. An assignable cause exists when a process is diagnosed as being out of the statistical control. The system can be brought back to the original benchmark once this assignable cause is eliminated. SPC can be applied to any process with the following characteristics: firstly, the output of process can be measured; secondly, the strength of each variation source can be determined numerically and further amenable to correction. SPC has been heavily applied in the semiconductor manufacturing. Unfortunately, SPC technique fails to provide the ideal process control. Although the out-of-control points may trigger the fault alarm, the equipment still

needs to be shut down for diagnosis and correction manually. Moreover, different products may be processed in a given tool, resulting in different process specifications or even baseline drift. For these circumstances, SPC technique is too coarse to perform corrective action, and advance control technologies are in need to address this shortcoming.

1.2.2 Run-to-run control

Run-to-run (R2R) control performs process parameter tuning based on the feedback or feedforward models between successive iterations of a given process. A reference is initially built, and the measurements are compared with the reference. Based on the difference, tunings on process parameters are conducted appropriately by using some algorithms. This control methodology keeps working through the lithography process so as to ensure the repeatability of the final CD result. Specifically, both feedback and feedforward models can be applied under the framework of R2R control. For feedback model, when CD linewidth is controlled by the PEB temperature, the drift of CD indicated by several consecutive runs can be feedback by the metrology sensor to the controller. Recipe tuning is then conducted on the PEB bake-plate before next wafer comes in. On the other hand, feedforward model can also be adopted for R2R control. In a feedforward situation, the properties of incoming wafer are used to tune the subsequent step parameter settings. For example, if the photoresist thickness suddenly drifts after soft bake, the PEB temperature may need to adjust properly to compensate this unexpected drift. R2R control may ensure a smooth man-

ufacturing operation and guarantee the product reproducibility. However, its drawback is also very obvious that all the measurements are conducted after the process is completed and no real-time correction is performed on the measured sample. The incoming wafers usually have different conditions. There is no guarantee that the tuning based on the measured sample is ideal for the next incoming wafers. To solve this problem, the in-situ real-time control technologies are necessary.

1.2.3 Real-time control

The essence of real-time control is to integrate the metrology sensor together with the process chamber. The sensor performs in-situ measurement and allows the actuator to react immediately based on the control algorithms. In lithography process, applying real-time temperature control at certain thermal baking steps such as soft bake or PEB can efficiently improve the CD uniformity. However, lithography actually consists of a series of process modules, and most of the real-time control methods are only employed within a single module. To make the system more robust and intelligent, it is necessary to have a framework to relate the successive modules throughout the lithography process. This framework also allows the operator to easily identify the fault and exclude the variation source from the previous steps.

1.3 Contribution

The most challenging parts for real-time control are the equipment design and implementation. This thesis proposes an approach to conduct real-time CD monitoring and control. It is well-known that temperature has a direct effect on CD. First, a multi-zone programmable thermal processing system is developed, which is able to control the wafer temperature uniformity during the entire thermal cycle. Next, an in-situ ellipsometry system is established and integrated into the thermal process to measure the CD profile in real-time. Experimental results demonstrate that the real-time control system is able to monitor and control the CD profile in real-time versus a run-to-run approach with more than 60% improvement. The summary of contributions is stated as below.

1.3.1 Modelling and real-time control of multi-zone thermal system

Current photoresist processes in advanced lithography systems are especially sensitive to temperature. This thesis presents an in-situ real-time method to control the wafer spatial temperature uniformity during thermal cycling of silicon wafer in the lithography sequence. These thermal steps are usually conducted by placing the substrate on the bake-plate for a given period of time. Tay et al. [8] have proposed an approach for controlling wafer temperature uniformity at steady-state. This thesis extends the approach by considering the dynamic properties of the system. A de-

tailed physical model of the thermal system is first developed to describe the temperature relationship between the bake-plate and wafer. Next, by monitoring the bake-plate temperature and fitting the data into the model, the wafer temperature can be real-time calculated and controlled. This is useful as production wafer usually does not have temperature sensors embedded on it. As the thermal baking processes are subject to drifts, disturbances, and wafer warpage, a real-time correction of the bake-plate temperature is further established to improve the across wafer temperature uniformity. Compared with the method presented in [8], our approach performs well not only at steady-state, but also at the transient state. In particular, the equipment design includes a programmable dual-zone thermal processing system together with a model-based feedback controller.

1.3.2 Ellipsometry equipment design and application

Metrology is important for the entire microelectronics fabrication industry. Optical metrology is widely used at the nanometer scale for its non-destructive and non-invasive characteristics. Optical probes are especially favored for in-situ real-time monitoring because of their small footprint, fast response, high accuracy and robustness. This thesis applies the spectroscopic ellipsometry technique which can in-situ monitor the process. Ellipsometry is an optical technique devoted to the application of surface analysis, which measures a change in polarization as light reflects or transmits from a material structure [14]. Since the 1960s, as ellipsometry is developed to provide the sensitivity necessary to measure the nanometer-scale layers

in microelectronics, interest in ellipsometry has grown steadily [15]. The advantage of using ellipsometry includes the non-destructive nature, high sensitivity, and simple implementation. Moreover, it is highly desirable to commission the ellipsometer as the contactless sensor for in-situ process monitoring to prevent wafer contamination in the semiconductor manufacturing. This thesis applies the spectroscopic ellipsometry at the PEB step to in-situ monitor the variation of CD latent image profile through thermal processing. Compared with the traditional SEM and AFM metrology techniques, ellipsometry demonstrates great capability for in-situ thin film properties measurement.

1.3.3 Dual-zone spatial CD in-situ real-time control through the PEB process

Conventional baking is commonly used at the PEB step where the bake-plate substrate is usually of large thermal mass and maintained at a constant temperature. Empirical experiments show that large across wafer CD nonuniformity exists at the end of the lithography process, which may lead to a significant yield loss. Semiconductor manufacturer can optimize the process flow to increase the device tolerance and compensate the CD nonuniformity [16]. However, as the device size keeps shrinking down and the wafer size keeps increasing up, the tolerance becomes much tighter than before. A multi-zone system is needed for better across wafer CD uniformity control. In this thesis, a dual-zone programmable thermal bake-plate is integrated together with a dual-probe spectroscopic ellipsometer. Based

on this equipment integration, an effective in-situ real-time across wafer CD monitoring and control system is further developed. Firstly, the reference signatures regarding to the target DICD profiles are built. Secondly, an electromagnetic wave model based on the rigorous coupled-wave analysis (RCWA) is developed to relate the CD latent image profile with the ellipsometry measurement. At the PEB step, the spectroscopic ellipsometer performs in-situ photoresist properties measurement. The measured data can be characterized into CD profile by RCWA model. Thirdly, a real-time thermal control algorithm is proposed for across wafer CD uniformity improvement. Through the entire PEB process, the computer keeps comparing ellipsometry in-situ measurement with the reference for both wafer center and edge. Moreover, two decentralized PI controllers real-time adjust power inputs to the bake-plate center and edge based on the difference between measurement and reference. With the proposed dual-zone real-time CD monitoring and control system, the temperature profile across the bake-plate is controlled dynamically. The across wafer CD uniformity has been improved by more than 60% comparing with the conventional baking.

1.3.4 Feedforward/Feedback control framework for lithography process

Literature shows that CD variation attributes to all the steps of lithography. Application of in-situ real-time thermal control at the PEB step may improve the CD result but can not correct the variation source prior to the PEB step. To obtain an intelligent system which is able to effectively rec-

tify the CD variation source and correct the recipe offset, this thesis strives for further improvements in the entire lithography process by building a feedforward/feedback control framework. The spin coating and PEB steps are selected as the controlled steps throughout the lithography process. For feedforward control, the perturbation caused by spin coating recipe offset is identified by the ellipsometer at the beginning of PEB process and then fixed by real-time thermal baking. When it comes to the feedback control, based on the in-situ measurement at the PEB step, the recipe of spin coating step is tuned appropriately before the next wafer comes in. With the application of such a feedforward/feedback control framework, apart from conducting real-time thermal control at the PEB step to achieve better CD results, the recipe offset at the spin coating step can also be corrected.

1.4 Organization of the Thesis

The rest of thesis is organized as follows. Chapter 2 describes the dual-zone programmable thermal system modelling and control. The spectroscopic ellipsometry working principle and its applications are presented in Chapter 3. Chapter 4 proposes an in-situ real-time across wafer CD monitoring and control system. Experiments are conducted with the real-time approach, demonstrating a significant CD uniformity improvement. Chapter 5 builds a feedforward/feedback control framework throughout the lithography process. It performs in-situ real-time CD control at the PEB step and further rectifies the perturbation at the spin coating step. Finally, conclusions and

potential future works are discussed in Chapter 6.

Chapter 2

Dual-Zone Programmable Thermal Baking System

2.1 Introduction

Temperature uniformity control is an important issue in photoresist processing with stringent specifications and has a significant impact on the CD. Variation in CD results in scrap products. The most temperature sensitive step in the lithography sequence is the PEB step. The variation in CD for this thermally activated process ranges from 3 to 7 nm/°C in bake temperature [6]. Requirements call for the temperature to be controlled within 0.1 °C across the wafer at temperatures between 70 °C and 150 °C [8], [17]. A number of recent investigations also showed the importance of proper bake-plate operation, both in steady and transient states, on CD control [18] - [25]. Two approaches exist in addressing this issue in industry. The first approach involves the development of less tempera-

ture sensitive photoresist. As outlined by the ITRS roadmap [2], there are currently no known manufacturing solutions and much work is required. The second approach is the development of algorithms [26], [27] and more advanced thermal processing systems [28], [29] for temperature and CD control, which is the approach undertaken in this chapter.

Thermal processing of semiconductor wafers is commonly performed by placing the substrate on a heated bake-plate for a given period of time. The heated bake-plate is held at a constant temperature by a feedback controller that adjusts the heater power in response to a temperature sensor embedded in the bake-plate near the surface. State-of-the-art heating systems consist of more heating zones. The wafers are usually placed on proximity pins to minimize contamination. When a wafer at room temperature is placed on the bake-plate, the temperature of bake-plate invariably drops first but recovers gradually because of closed-loop control. Different air gap sizes will result in different temperature drops in the bake-plate due to the difference in the air gap thermal resistance between the wafer and the bake-plate. A warped wafer will thus result in deviation of the wafer temperatures from its desired set points across the wafer surface.

Production wafers usually do not have temperature sensors embedded in them. Commercial bake-plates are usually calibrated based on test wafers with embedded sensors. However, as the processes are subject to drifts and disturbances, a fixed temperature set point is not able to address the issues. Any correction is therefore executed based on R2R control techniques, which depend on the sampling frequency of the wafers.

In [8], it demonstrated that information of the average air gap between the wafer and the bake-plate can be obtained with the use of system theory tools. The relationship between the wafer and plate temperatures at steady-state can then be derived from physical modelling of the baking process. By monitoring the maximum plate temperature drop, the average air gap in each heating zone can be estimated, and we are able to calculate the new bake-plate temperature set point to achieve the desirable steady-state temperature [8]. One of the major drawbacks of the mentioned approach is that it does not take into account the dynamic performances of the wafer temperature, although an improvement of steady-state temperature uniformity is obtained from about 1.1 °C to less than 0.1 °C when compared to conventional approaches where a simple feedback controller is used to regulate the plate temperature. The steady-state approach in [8] makes use of conduction thermal resistance terms which are strictly accurate only during steady-state. Consequently, that gives rise to significantly modelling error during the initial transient phase. It has also been reported that even though the resultant range of steady-state temperatures was minimized, the consequent gain in CD uniformity cannot be realized. This is attributed to the temperature distribution while rising to the PEB temperature [17].

In this chapter, a real-time wafer temperature control method to minimize temperature nonuniformity in the baking steps is proposed. The dynamic performance of the wafer temperature is improved. In contrast, the presented model adopts the full thermal diffusion formalism so that the thermal behavior during the initial transient period is properly cap-

tured. The average air gap thicknesses between the bake-plate and wafer in each of the heating zones, and consequently the wafer temperature can be extracted in real-time. The experimental result shows the feasibility of the proposed approach, and significant improvement is obtained when compared with conventional method and the steady-state approach [8].

The rest of Chapter 2 is organized as follows. In Section 2.2, the detailed thermal modelling is developed. The experimental results are then presented in Section 2.3. Finally, the conclusion is given in Section 2.4.

2.2 Thermal Modelling of the System

2.2.1 System modelling

The multi-zone programmable thermal processing system used in this chapter is shown in Figures 2.1 and 2.2. In the baking process, the bake-plate is heated up by the cartridge heater attached to it. Resistive heating elements and resistance temperature detector (RTD) sensors are embedded in each of the heater cartridge, which are connected to the main heater plate via epoxy. The bake-plate consists a total of 64 of these heating elements in four annular rings. The center ring has 4 elements, the second to fourth annular rings has 12, 20, and 28 elements, respectively. Depending on the application, the number of heating zones of the bake-plate can be easily configured by simple connection of these heating elements. In the actual experimental work, the system is configured as a dual-zone system. The inner zone consists of 16 heating elements, the out zone consists of 48

heating elements. Each heating zone is configured with its own temperature sensor and electronics embedded in the cartridge for feedback control. The fact that zones are spatially disjointed by 1.27 mm air gap ensures no direct thermal coupling between the zones. Detailed description of the programmable thermal processing system can be found in the work of Tay et al [8].

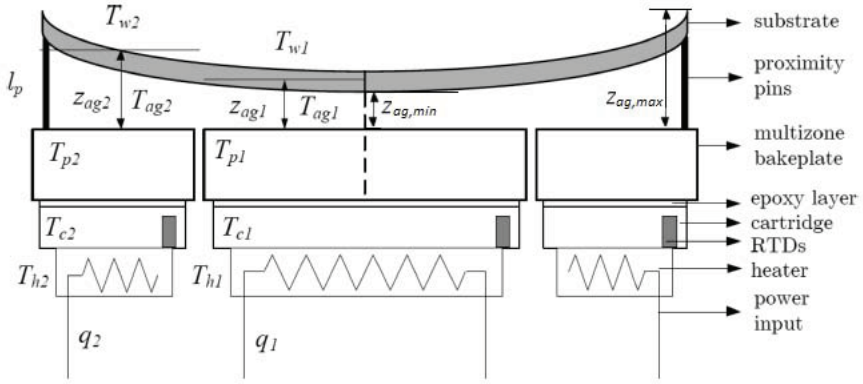

Figure 2.1: Schematic diagram of the thermal processing system

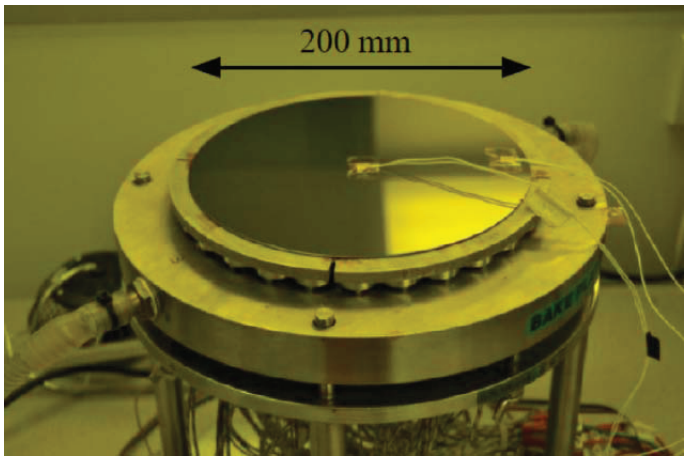

Figure 2.2: Photo of the thermal processing system

Thermal energy transport mechanisms are usually classified as conduc-

tion, convection, and radiation. The second law of thermodynamics states that heat flows whenever there is a temperature gradient. For our thermal system, radiation heat transfer has limited application and can be ignored. Conduction and convection are the main mechanisms for thermal energy exchange. Energy balances on the elements in the system can be carried out to obtain a thermal model as follows:

$$C_w\dot{T}_w = q_w^{in} + q_w^{out} + q_w^{top} + q_w^{bottom}, \tag{2.1}$$

$$C_{ag}\dot{T}_{ag} = q_{ag}^{in} + q_{ag}^{out} + q_{ag}^{top} + q_{ag}^{bottom}, \tag{2.2}$$

$$C_p\dot{T}_p = q_p^{in} + q_p^{out} + q_p^{top} + q_p^{bottom}, \tag{2.3}$$

$$C_c\dot{T}_c = q_c^{in} + q_c^{out} + q_c^{top} + q_c^{bottom}, \tag{2.4}$$

$$C_h\dot{T}_h = q_h^{in} + q_h^{out} + q_h^{top} + q_h^{bottom} + q^{input}, \tag{2.5}$$

where T is the temperature above the ambient, C is the thermal capacitance, q^{in},q^{out},q^{top} and q^{bottom} are the heat flows into the element from inner zone, outer zone, top surface, and bottom surface, respectively, q^{input} is the heater power and the subscripts w, ag, p, c, and h represent the wafer, the air gap, the bake-plate, the cartridge, and the heater, respectively. Detailed description of each of the terms are presented in the Appendix.

In the system, the wafer and the bake-plate can be discretized into several zones to simulate their temperature response. For each discrete element, heat is transferred between the adjacent inner and outer elements. There are

$$q_i^{in} = kA_i^{side}\frac{T_{i-1} - T_i}{r_{i-1}}, \tag{2.6}$$

$$q_i^{out} = kA_{i+1}^{side}\frac{T_{i+1} - T_i}{r_i}, \tag{2.7}$$

where k is the thermal conductivity, A^{side} is the contact area between the adjacent elements, and r_i is the distance between the elements i and $i+1$.

For the edge element, the side surface is exposed to the ambient, so there is

$$q_n^{out} = h_{lm} \cdot A_{lm}^{side}(-T_a), \tag{2.8}$$

where the subscript lm represents the different layers in the system, which are namely the wafer, the bake-plate, the cartridge and the heater. Variable T_a is the edge element temperature above the ambient. Variable h is the convection coefficient, which can be calculated as follows [30]:

$$h = \frac{k}{L_0}\overline{N}_u, \tag{2.9}$$

where L_0 is the characteristic length, $\overline{N}_u$ is the Nusselt number, and there is [30]

$$\overline{N}_u = \{0.6 + \frac{0.387(Ra)^{1/6}}{[1 + (0.559/Pr)^{9/16}]^{8/27}}\}^2, \tag{2.10}$$

where Ra is the Rayleigh number, Pr is the Prandtl number, and there are

$$Ra = \frac{g \cdot \beta_0 \cdot (T_1 - T_2) \cdot d^3}{\mu \cdot \alpha_0}, \tag{2.11}$$

$$Pr = \mu/\alpha_0, \tag{2.12}$$

where g is the acceleration of gravity, β_0 is the volume thermal expansion coefficient of fluid, T_1 and T_2 are the temperatures of two adjacent layers, d is the depth of fluid layer, μ is the kinematic viscosity, and α_0 is the thermal diffusivity of fluid.

The wafer top surface is exposed to the surroundings and so there is

$$q_n^{top} = h^{top} \cdot A_w^{top}(-T_w), \tag{2.13}$$

where A_w^{top} is the area of the wafer top exposed to the ambient. The convection coefficient h^{top} can be calculated from the following [30]:

$$h^{top} = 0.54(Ra)^{1/4}. \tag{2.14}$$

The air gap between the wafer and bake-plate is about 100 to 300 μm. The main mode of heat transfer between two materials separated by air depends on both the air gap and the temperature difference between the two materials [31]. When this air gap is below 5.8 mm, and their temperature difference is considerably smaller than 200 °C, the heat transfer mechanism is essentially conductive [31] and given by the following:

$$q_w^{bottom} = -k_{ag} A_{ag} \frac{\partial T_{ag}}{\partial z_{ag}}|_{boundary}, \tag{2.15}$$

where z is the thickness. The effect of radiative heat transfer is negligible at the temperature range that we are interested [7].

Since the governing thermal transport between the elements in the system is conductive, at the boundary layer of two adjacent elements, there is

$$-k_a A_a \frac{\partial T_a}{\partial z_a}|_{boundary} = -k_b A_b \frac{\partial T_b}{\partial z_b}|_{boundary}, \tag{2.16}$$

where the subscripts a and b represent the two vertical adjacent layers.

At the bottom layer of the system, the heater is exposed to the ambient, and there is

$$q_n^{bottom} = h_{bottom} \cdot A_h^{bottom} \cdot (-T_h), \tag{2.17}$$

Table 2.1: Physical parameters of the thermal processing system

	Property	Value
Wafer (Silicon)	Density, ρ	2330 kg m^{-3}
	Specific heat capacity, c_v	750 J K^{-1} kg^{-1}
	Thermal conductivity, k	99 W m^{-1} K^{-1}
	Convection coefficient, h	3.3824 W m^{-2} K^{-1}
	Thickness, z	0.700 mm
Air	Density, ρ	1.1 kg m^{-3}
	Specific heat capacity, c_v	1000 J K^{-1} kg^{-1}
	Thermal conductivity, k	0.03 W m^{-1} K^{-1}
Bake-plate (Aluminum)	Density, ρ	2700 kg m^{-3}
	Specific heat capacity, c_v	917 J K^{-1} kg^{-1}
	Thermal conductivity, k	250 W m^{-1} K^{-1}
	Convection coefficient, h	7.271 W m^{-2} K^{-1}
	Thickness, z	6.8 mm
Epoxy	Thermal conductivity, k	0.35 W m^{-1} K^{-1}
	Thickness, z	0.02 mm
Cartridge (Aluminum)	Density, ρ	2700 kg m^{-3}
	Specific heat capacity, c_v	917 J K^{-1} kg^{-1}
	Thermal conductivity, k	250 W m^{-1} K^{-1}
	Convection coefficient, h	4.86 W m^{-2} K^{-1}
	Thickness, z	4.4 mm
Heater (Aluminum)	Density, ρ	2700 kg m^{-3}
	Specific heat capacity, c_v	917 J K^{-1} kg^{-1}
	Thermal conductivity, k	250 W m^{-1} K^{-1}
	Convection coefficient, h	2.7828 W m^{-2} K^{-1}
	Thickness, z	5.4 mm

where A_h^{bottom} is the area of the bottom of the heater exposed to the ambient. The convection coefficient h_{bottom} can be calculated from the following [30]:

$$\overline{N}_u^{bottom} = 0.27(Ra)^{1/4}. \tag{2.18}$$

Most thermophysical properties are temperature dependent. However, for the temperature range of interest from 15 to 150 °C, it is reasonable to assume that they remain fairly constant and can be obtained from handbooks [32] as tabulated in Table 2.1.

2.2.2 Model verification

The modelling equations are expressed in state-space form in the Appendix. To assess the quality of the proposed system model, we perform conventional baking process experiment and compare the simulation with the experimental results. In this work, the system dynamics for a dual-zone system are simulated. The objective is to demonstrate that the proposed model succeeds in predicting the experimental wafer temperatures using the bake-plate temperature and the input signal without resorting to the use of any fitting parameter and is therefore useful for scaling up.

In the experiment, a flat wafer at room temperature is dropped on the baking system with a proximity pin height, l_p, of 140 μm. This causes the bake-plate temperature to drop at first but recovers gradually because of closed-loop control. Two proportional-integral (PI) controllers are used to control the temperature of the two zones of the bake-plate. The dynamic equation of the PI controller is

$$u(t) = K_p \cdot e(t) + K_i \cdot \int_0^t e(\tau) d\tau, \tag{2.19}$$

where $u(t)$ is the PI controller output at time t, $e(t)$ is the difference between the measured temperature and the reference temperature at time t, K_p is the proportional gain, and K_i is the integral gain. As the standard PI controller is implemented in LabVIEW, the dynamic equation for the PI controller is actually

$$u[k] = u[k-1] + (K_p + K_i \cdot T_s) \cdot e[k] - K_p \cdot e[k-1], \tag{2.20}$$

where $u[k]$ is the current power input, $u[k-1]$ is the previous power input,

T_s is the sampling time, $e[k]$ is the current difference between the bake-plate temperature measurement and set point, and $e[k-1]$ is the previous difference between the bake-plate temperature measurement and set point. The Ziegler-Nichols Reaction Curve Tuning Method is used for the PI controller tuning. This method is based on the open loop step response of the system. The selection of sampling time is discussed in Section 2.3. In the experiment, the sampling time is set to be 0.5 sec. The open loop step responses of the bake-plate center and edge are plotted in Figure 2.3. From the figures, we can obtain $K_p = 1.0098$, $K_i = 0.0634$ for the center zone, and $K_p = 0.5556$, $K_i = 0.0162$ for the edge zone. After several iterations of tuning, we finally use $K_p = 1.00$, $K_i = 0.10$ for the center zone, and $K_p = 0.50$, $K_i = 0.01$ for the edge zone in the experiment.

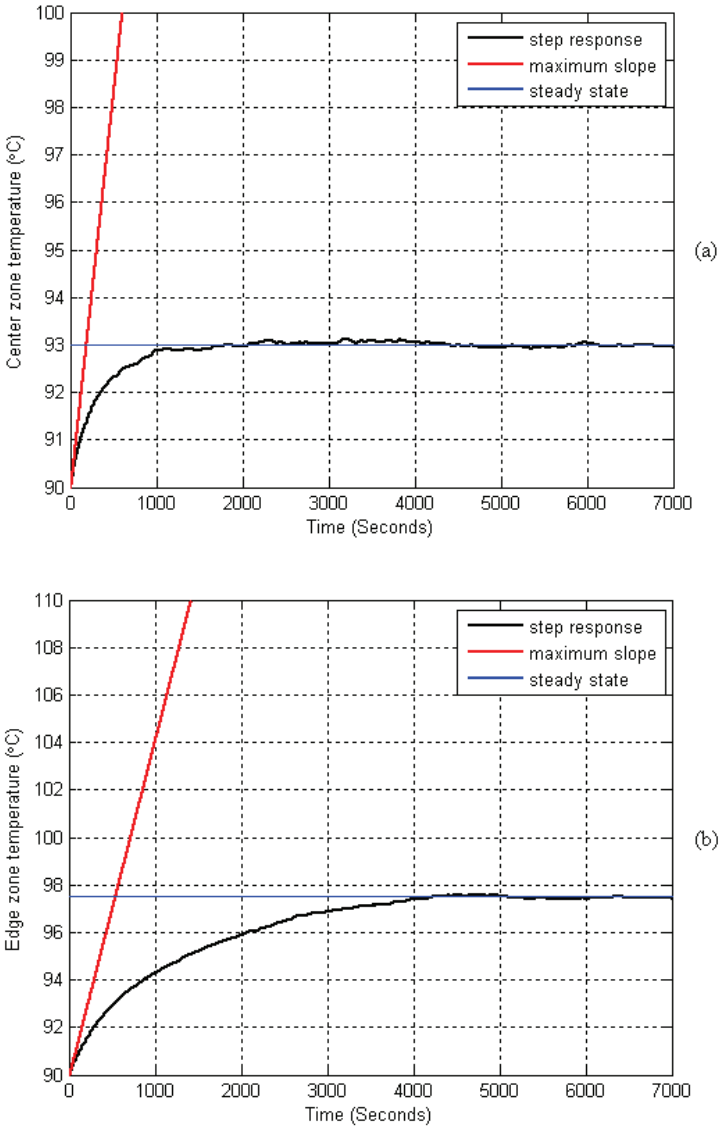

Figure 2.3: Open loop step responses for the 8-inch bake-plate. The bake-plate center and edge temperatures during the baking process are shown in subplots (a) and (b), respectively.

Figure 2.4 shows the comparison result of the simulation and experimental bake-plate temperatures and wafer temperatures when the air gap thickness is approximately 140 μm. It can be seen that the agreement between of the wafer temperatures from simulation and experimental results is excellent, thereby verifying the effectiveness of the proposed thermal model. The estimated air gap thicknesses are plotted in Figure 2.5. Being confident of our system modelling, we then conduct real-time control experiment with the system model.

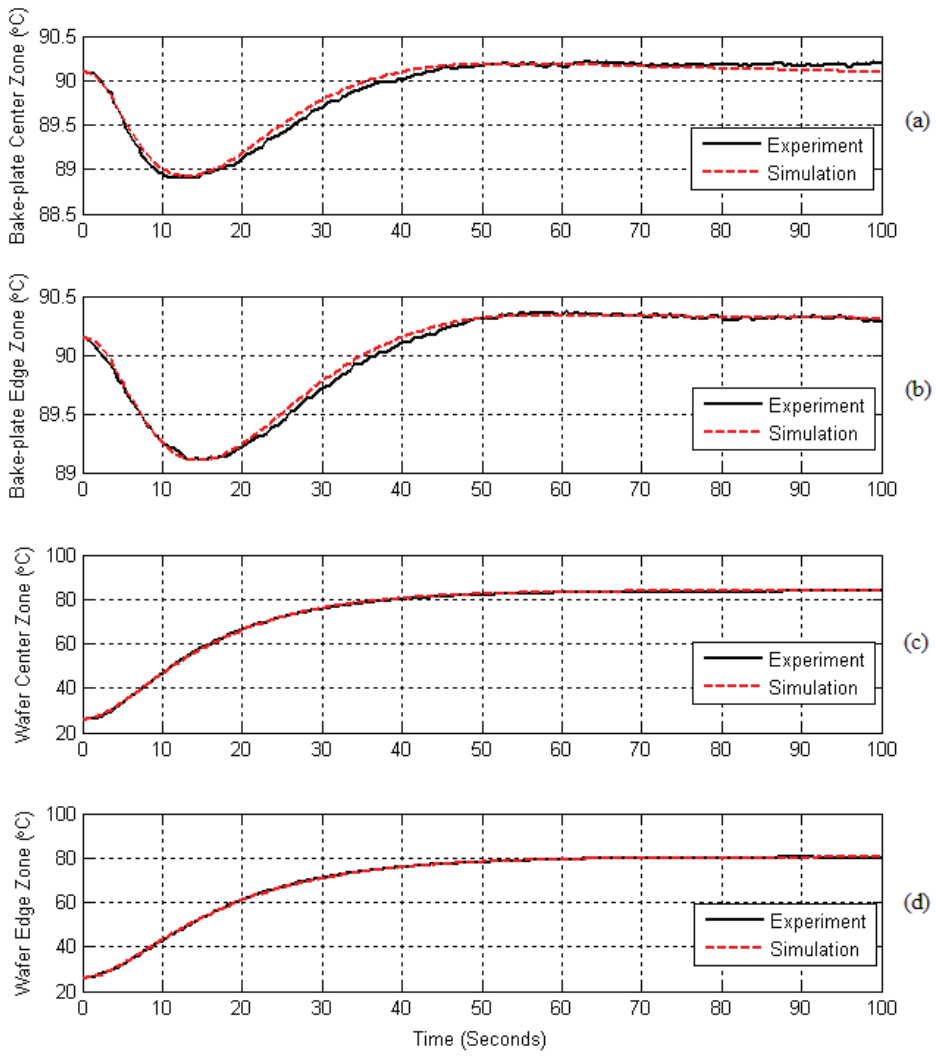

Figure 2.4: Plate and wafer temperature in simulation and experiment with air gap thickness be 140 μm using the calculated model. The bake-plate center temperatures, bake-plate edge temperatures, wafer center temperatures, and wafer edge temperatures during the baking process are shown in subplots (a), (b), (c) and (d), respectively.

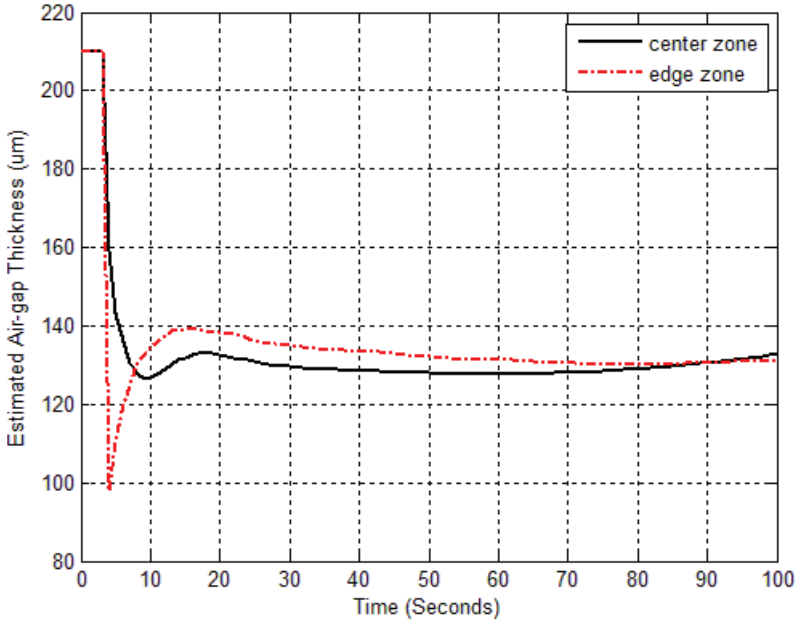

Figure 2.5: Air gap estimation for conventional baking with 140 μm proximity pins

2.3 Real-time Wafer Temperature Spatial Control

2.3.1 Experiment setup and control structure

Most of the experimental conditions are similar to [8]. The experimental setup for the baking of 200 mm wafer is shown in Figure 2.1. RTD sensors are attached to the wafer for temperature measurement [7], [33]. The wafer is dropped onto the bake-plate by aligning the major flat surface of the wafer with the proximity pins. A control-system software was developed using National Instrument (NI) LabVIEW programming environment to

create a multivariable PI control framework and a dynamic temperature control system.

Figure 2.4 shows the high quality modelling fit with experimental data for the case of a flat wafer. However, during actual wafer processing, wafers can warp due to other preprocessing steps. A wafer with non-flat surface is a warped wafer, where the maximum warpage is the difference between the maximum and the minimum air gap thicknesses [34]. Referring to Figure 2.1, the difference between the maximum air gap thickness, $z_{ag,max}$, and the minimum air gap thickness, $z_{ag,min}$, is the maximum warpage of the wafer. Once a wafer is warped, the air gap between the wafer and the bake-plate will change as shown in Figure 2.1. For the proximity baking, a warpage in the order of 10 - 20 μm will make a difference in the thermal processing rates across the wafer. This is because the distance between the wafer and the hot plate can be in the order of 100 μm, and a warped wafer will alter that gap considerably. Product wafers may come in with different shapes, given that they arrive at the wafer track with different layers on them. So, it is not uncommon to have product wafers with warpage of up to and sometimes exceeding 100 μm [5].

The thermal bake-plate usually has compact design and there is no space to insert external sensor for air gap thickness measurement. Estimating the air gap thickness from model can solve this issue. The proposed approach required detailed information of the system in order to identify the average air gap during subsequent processing. On the basis of the dual-zone system model, a state-space model [35] with the air gap thicknesses of the two

zones as unknown is developed. Detailed description of the thermal model in state-space form is given in the Appendix. In the experiment, the bake-plate temperature readings and input control signals are collected and fitted into the model to extract the air gap thicknesses and wafer temperatures using the gray-box modelling function from MATLAB system identification toolbox [35]. Because the linear thermal expansion coefficient of silicon wafer is as low as 3 - $4\times10^{-6}/^{\circ}$C when the temperature is less than 800 °C [36]. The variation of wafer warpage during the baking process can be neglected and we may assume that air gaps remain the same throughout the baking process. The estimated air gap thickness for the two zones under different experimental conditions are tabulated in Table 2.2. This approach is particularly useful since we understand the physics of the thermal system and can represent the thermal system using ordinary differential equations.

Table 2.2: Estimated air gap thickness and wafer warpage using the real-time control method with the proximity pin height of 210 μm

wafer	center zone	edge zone	extracted wafer warpage
flat wafer	208 μm	214 μm	12 μm
70 μm warpage	146 μm	182 μm	72 μm

Figure 2.6 shows the control systems framework. The bake-plate is connected to the power supply and computer through the solid state relay (SSR), which allows us to switch power to the load circuitry. The data acquisition (DAQ) module and input/output (IO) connector block from NI are used for data transmission. The bake-plate temperatures, T_{p1}, and, T_{p2}, and the control signal, u_1, and, u_2, in the dual-zone system are measured and sent to the estimator. The "Estimator" block estimates the new air

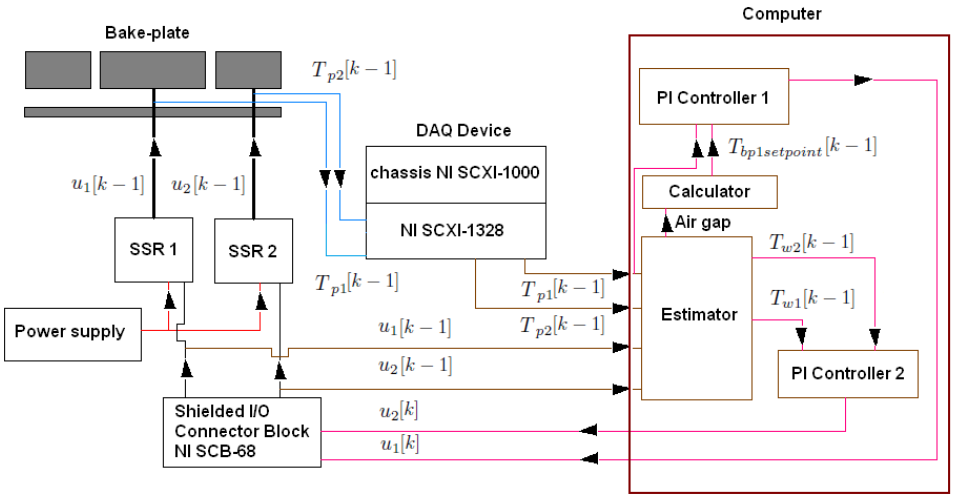

Figure 2.6: Block diagram of the control systems framework, where k indicates the state, $T_{bp1setpoint}$, T_{w1} and T_{w2} are the desired plate reference temperature in center zone based on the estimated air gaps, the estimated wafer temperatures in center and edge zones, respectively.

gap thickness. With the estimated air gap thickness and desired wafer temperature, the desired bake-plate temperature can be back calculated from Equation A.53 in Appendix. The set point of bake-plate center, $T_{bp1setpoint}$, can be determined. PI Controller 1 is used for the bake-plate center. It reads the bake-plate center temperatures and compares the readings with reference, $T_{bp1setpoint}$, and adjusts the power inputs to the bake-plate center appropriately. The estimated wafer temperatures, T_{w1}, and, T_{w2}, are used to control the wafer temperature uniformity in the process. PI Controller 2 is used for the bake-plate edge. It compares the estimated wafer edge temperature, T_{w2}, with the estimated wafer center temperature, T_{w1}, and adjusts the power inputs to the bake-plate edge appropriately. Using this method, we can real-time estimate the air gap thickness and wafer temper-

ature, and consequently regulate the control signal online to achieve the desired wafer temperature and minimize the temperature nonuniformity during the baking process.

Sampling rate is another concern in the real-time control. Selection of sampling rate is usually a compromise between performance and cost. It was stated that at least 10 samples were required within the rise time of system to effectively track the signal [37]. From Figure 2.4, it is observed that the rise time of wafer temperature is about 20 sec. Therefore, the sampling time should be at most 2 sec. In the experiment, the sampling time is set as small as 0.5 sec to achieve the best uniformity result.

2.3.2 Experimental result

To demonstrate our approach, an 8-inch flat wafer is dropped on the bake-plate with a proximity pin height of 210 μm. The initial air gap is fixed at 210 μm, i.e., the condition for a flat wafer. The final estimated air gaps are tabulated in Table 2.2. A good measure of the extent of warpage is to measure the deviation of the average air gap from the proximity pin height. For the flat wafer, the deviations are close to zero as expected.

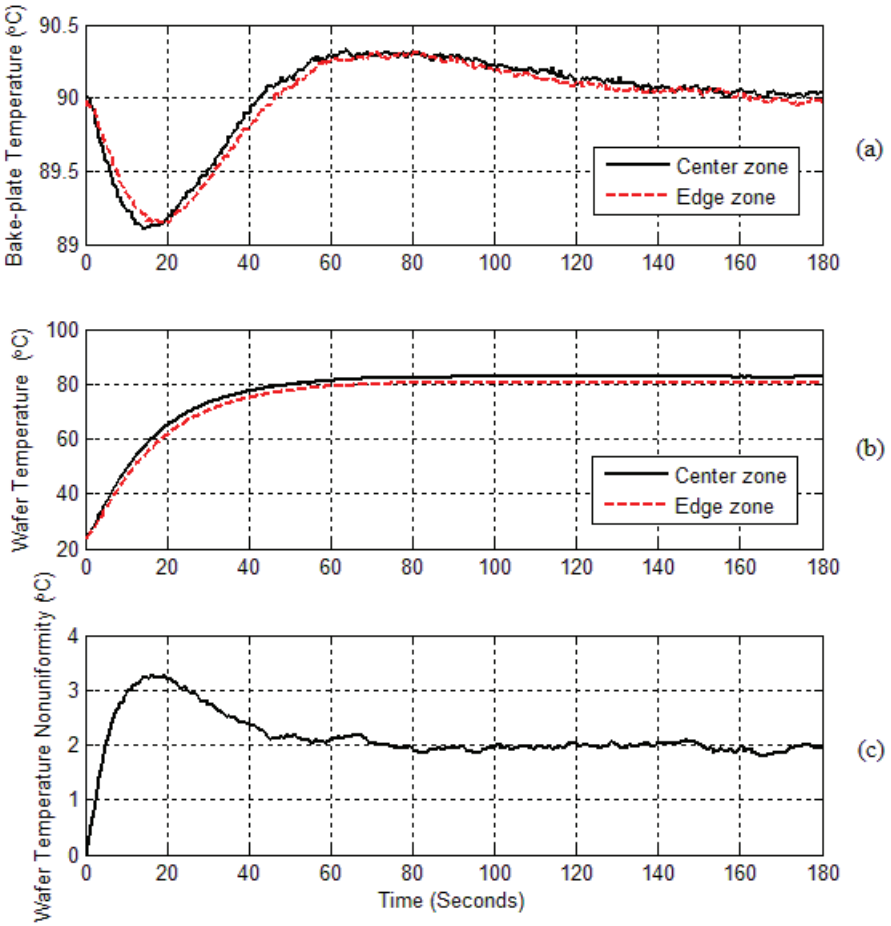

Figure 2.7: Temperature profile of bake-plate and wafer for conventional baking when a flat wafer is dropped on bake-plate with proximity pin height of 210 μm. The bake-plate temperatures, wafer temperatures, and wafer temperature nonuniformity during the baking process are shown in subplots (a), (b), and (c), respectively.

Conventional baking is first conducted at 90 °C. Figure 2.7 shows the bake-plate and wafer temperature profiles using the conventional baking. After that, the real-time control method is used with the same baking conditions. Figure 2.8 shows the bake-plate and wafer temperature profiles using the real-time control method. The power inputs of the real-time control method to the bake-plate center and edge zones are plotted in Figure 2.9, respectively. It is worth noting that the steady-state approach in [8] has already made a significant improvement in the wafer temperature uniformity comparing with the conventional baking. For the steady-state approach, when the wafer is dropped on the bake-plate, the air-gaps are first estimated based on the maximum bake-plate temperature drops. After that, the new bake-plate temperatures are set based on the estimated air gap thicknesses. In [8], the wafer temperature is controlled at 90 °C with a steady-state temperature nonuniformity about 0.1 °C. However, the steady-state approach only focuses on the wafer temperature uniformity at the steady-state. Since the new bake-plate temperature set points are implemented about 20 sec after the wafer is dropped to allow the maximum temperature drop point to occur as well as for computational delay of the corresponding air gap, the wafer can only reach steady-state after about 80 sec. Furthermore, the wafer has a temperature nonuniformity of about 4 °C in transient period.

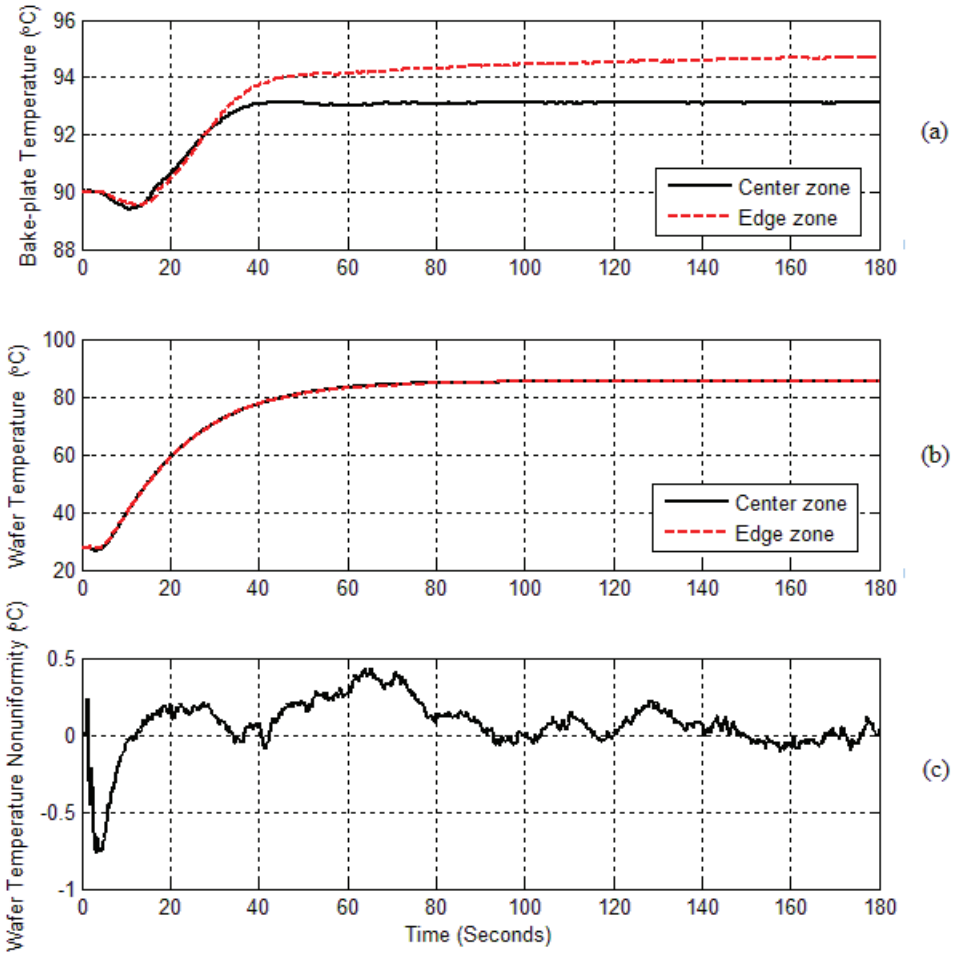

Figure 2.8: Temperature profile of bake-plate and wafer for real-time control method when a flat wafer is dropped on bake-plate with proximity pin height of 210 μm. The bake-plate temperatures, wafer temperatures, and wafer temperature nonuniformity during the baking process are shown in subplots (a), (b), and (c), respectively.

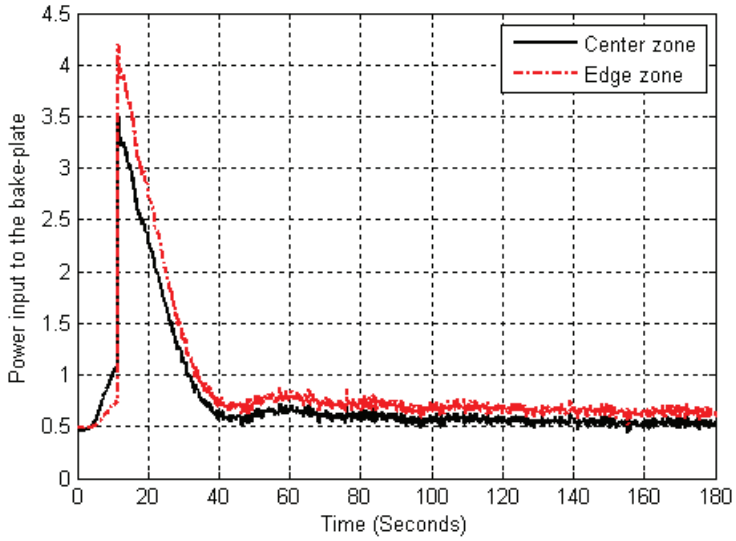

Figure 2.9: Power inputs to bake-plate center and edge zones for real-time control method when a flat wafer is dropped on bake-plate with proximity pin height of 210 μm.

The implementation of the real-time control method addresses the transient period wafer temperature nonuniformity issue. To validate the results, two RTD sensors are embedded into the wafer surface at locations corresponding to the center of each zone to monitor the wafer temperature. Figure 2.8 shows that the wafer temperature is controlled to 90 °C within 60 sec with a maximum temperature nonuniformity that is less than 1 °C during the transient period and steady-state temperature nonuniformity that is less than 0.1 °C. Compared with the steady-state approach, the real-time control method not only maintains almost zero nonuniformity at the steady-state but also significantly improves the temperature uniformity by more than 75% at the transient state. It is also believed that the maximum temperature variation of wafer middle zone should be less than the maximum temperature variation of wafer center and edge zones for

the dual-zone bake-plate. In [29], the wafer spatial temperature nonuniformity along the radius was monitored to verify the statement. Unexpected temperature variation may be obtained if the temperature sensor is just positioned above the air strip between the thermal zones. However, this issue can be solved by narrowing the air strip.

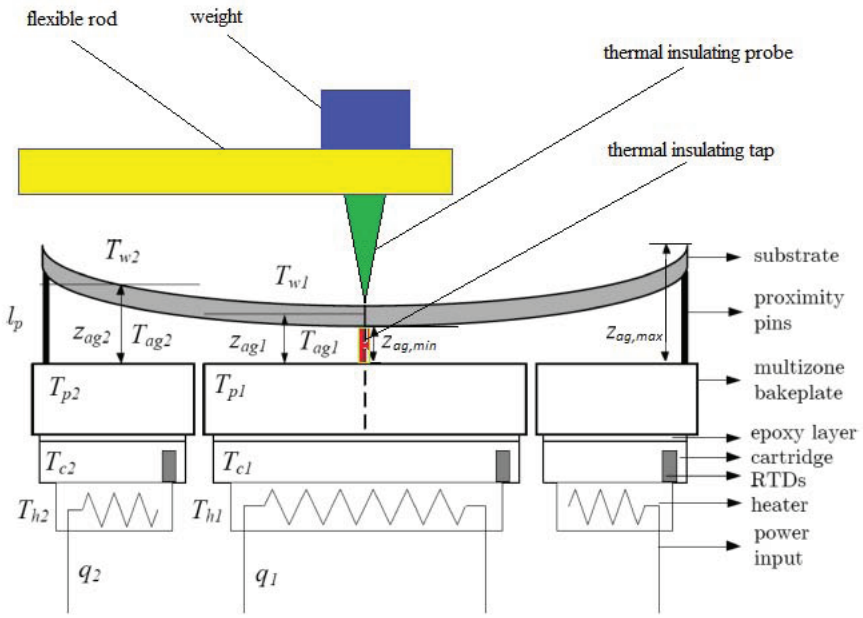

Figure 2.10: Schematic of warpage setup

The feasibility of the approach is further demonstrated by heating warped wafer. First, the wafer with center-to-edge warpage of 70 μm is dropped on the same bake-plate with the proximity pin height of 210 μm. Wafer warpage is created mechanically by putting a pointed weight at the center of wafer as described by Tay et al. [38] and shown in Figure 2.10. On the basis of the final estimated air gap thickness together with the proximity pin height, the profile of the wafer can be obtained by extrapolation. An

estimated warpage of 72 μm from center-to-edge for the warped wafer is obtained which is close to the known warpage of 70 μm. Figure 2.11 shows the bake-plate and wafer temperature profiles using the conventional baking for the warped wafer. Figure 2.12 shows the bake-plate and wafer temperature profiles using the real-time control method for the warped wafer. The power inputs of the real-time control method to the bake-plate center and edge zones are plotted in Figure 2.13, respectively. It can be seen that for the warped wafer, using the real-time control method, wafer temperature can reach the steady-state temperature within 50 sec, with a maximum temperature nonuniformity that is less than 1.3 °C during the transient period and steady-state temperature nonuniformity that is less than 0.1 °C. The comparison between the conventional baking, steady-state approach and real-time control method is summarized in Table 2.3.

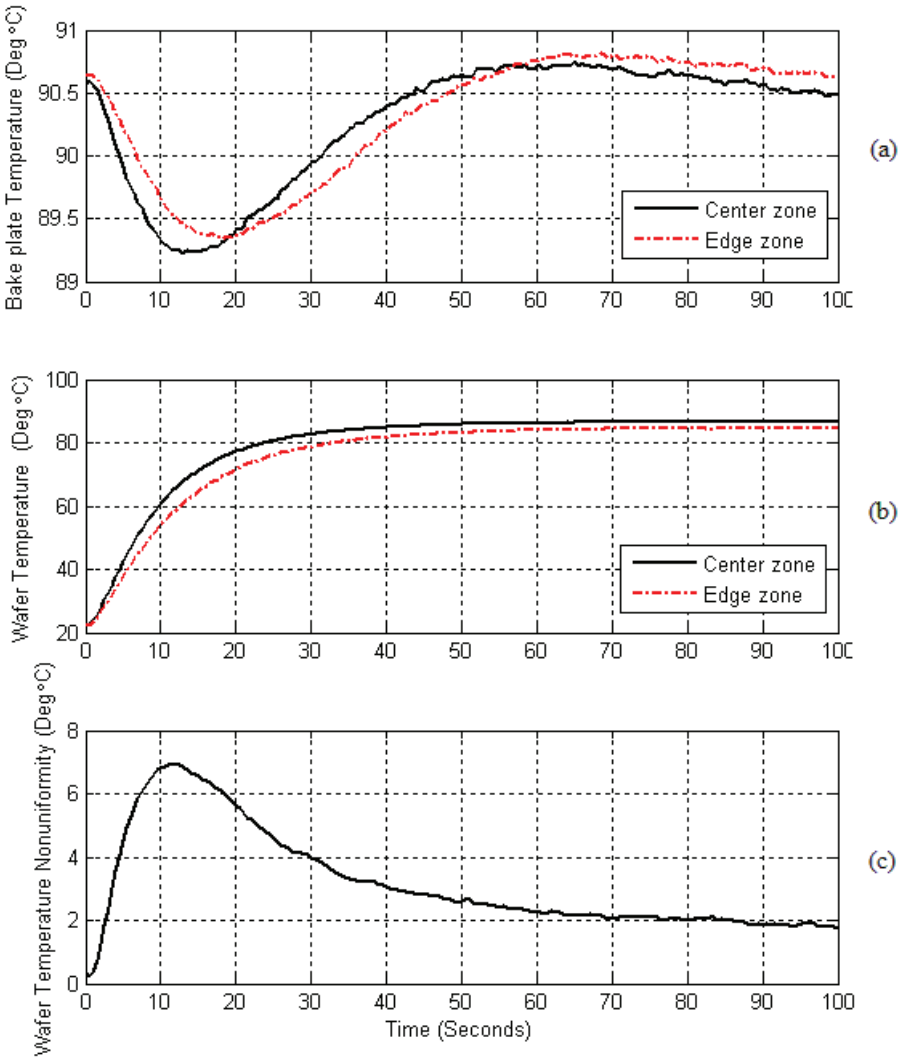

Figure 2.11: Temperature profile of bake-plate and wafer for conventional baking when a wafer with center-to-edge warpage of 70 μm is dropped on bake-plate with proximity pin height of 210 μm. The bake-plate temperatures, wafer temperatures, and wafer temperature nonuniformity during the baking process are shown in subplots (a), (b), and (c), respectively.

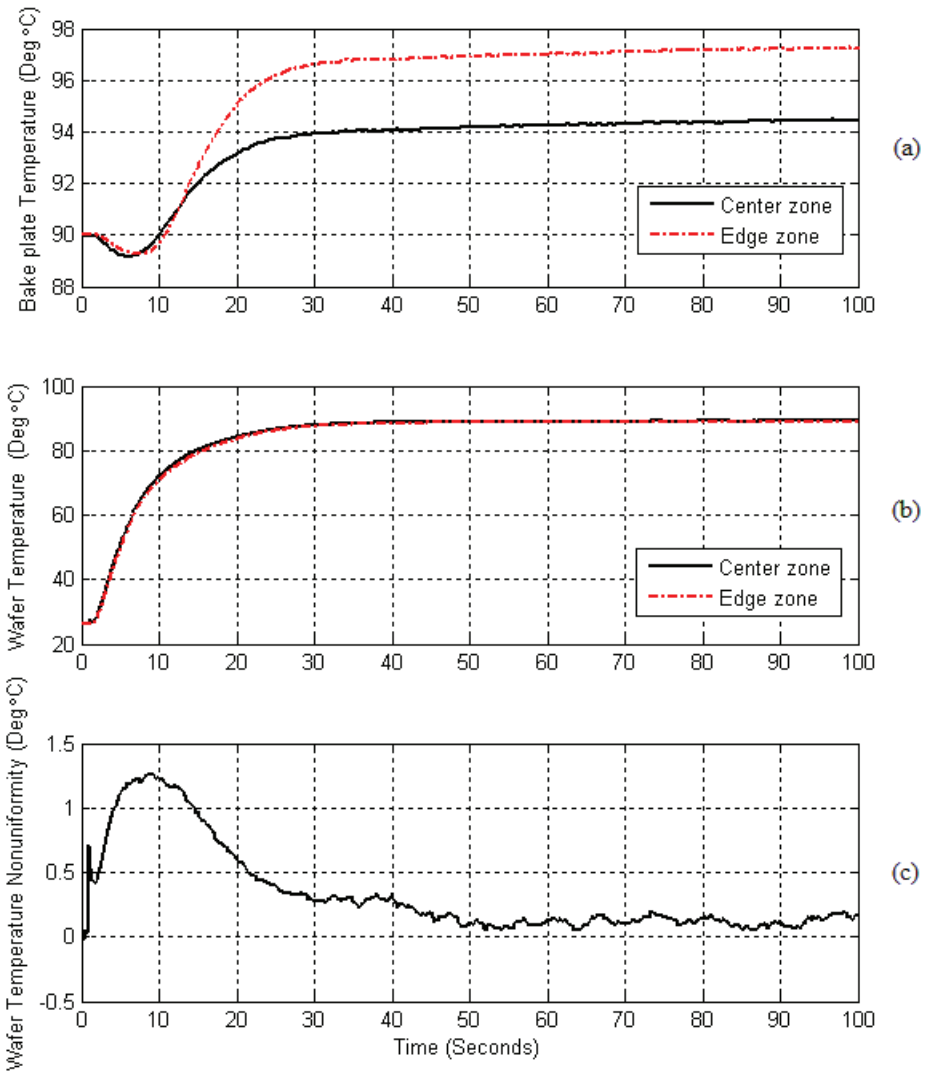

Figure 2.12: Temperature profile of bake-plate and wafer for real-time control method when a wafer with center-to-edge warpage of 70 μm is dropped on bake-plate with proximity pin height of 210 μm. The bake-plate temperatures, wafer temperatures, and wafer temperature nonuniformity during the baking process are shown in subplots (a), (b), and (c), respectively.

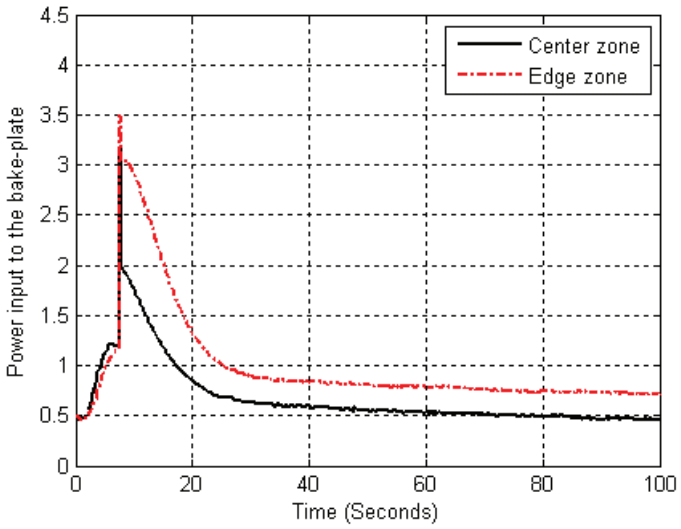

Figure 2.13: Power inputs to bake-plate center and edge zones for real-time control method when a wafer with center-to-edge warpage of 70 μm is dropped on bake-plate with proximity pin height of 210 μm.

Table 2.3: Comparison between conventional baking, steady-state approach and real-time approach

		Conventional baking	Steady-state approach [8]	Real-time approach	Improvement by real-time approach to conventional baking
flat wafer	transient steady	3.3°C 2.0°C	4.0°C 0.1°C	0.8°C 0.1°C	76% 97%
warped wafer	transient steady	6.9°C 1.8°C	4.4°C 0.1°C	1.3°C 0.1°C	81% 94%

2.4 Conclusion

In this chapter, an in-situ approach to real-time detection of wafer warpage and control of the wafer temperature uniformity in the heating process has been developed. Wafer temperature uniformity in transient period has been improved greatly compared with both the conventional baking and

steady-state approach. With the proposed approach, the wafer temperature is controlled to 90 °C within 60 sec with a maximum temperature nonuniformity that is less than 1.5 °C during the transient period and steady-state temperature nonuniformity that is less than 0.1 °C. The proposed approach can also be easily scaled up/down for larger/smaller wafers by increasing/decreasing the number of sensors, actuators, and controllers.

Chapter 3

Spectroscopic Ellipsometry Equipment Design and Application

3.1 Introduction

The applications of advanced computational and control methodologies in semiconductor manufacturing have received increasing research interests to improve yield, throughput, and, in some cases, to enable the actual process to print smaller devices. Optical metrology tools such as SEM and AFM are most commonly used for device structure measurement in the semiconductor manufacturing. However, they can only perform the ex-situ measurement, and the measurement is normally destructive and time consuming. A fast, accurate and non-destructive in-situ metrology is needed to address these issues. The objective of this chapter is to develop

an in-situ metrology for the photoresist properties monitoring through the PEB process.

The literature consists of a number of techniques for in-situ monitoring of the photoresist properties. Fadda et al. [39] used the contact angle measurements to monitor the photoresist thickness. Differently, an in-situ multi-wavelength reflection spectrometer was employed to measure the photoresist thickness [40]. Morton et al. [41] applied the in-situ ultrasonic sensors to monitor the change in photoresist properties to determine whether the photoresist had sufficiently been cured, thereby determining the endpoint of the soft bake process. Agrawal and Henderson [42] discussed the application of both single and multi-wavelength spectrometers in the estimation of photoresist thickness. However, these techniques can only deal with the unpatterned film and measure the one dimensional parameters such as film thickness. An in-situ metrology capable for the patterned film properties analysis is needed.

In this chapter, an in-situ metrology based on the ellipsometry is developed for the photoresist properties monitoring through the PEB process. It is worth noting that this in-situ metrology is applicable for the patterned film properties monitoring. Specifically, a PEB model is given on the basis of acid diffusion length (ADL) theory. The spectroscopic ellipsometry [43], [44] is then novelly implemented to measure the spectrum variation of the reflected light from the latent image of the photoresist. The experimental results demonstrate that ellipsometry exhibits the great capability to in-situ monitor the photoresist properties through the PEB process.

The rest of Chapter 3 is organized as follows. In Section 3.2, the working theory of the system is presented. Next, the hardware configurations of the machines are illustrated in Section 3.3. In Section 3.4, experiments are conducted to verify the capability of the proposed in-situ metrology. Conclusion is given in Section 3.5.

3.2 System Modelling

The aim of this chapter is to develop an in-situ metrology for the photoresist properties monitoring through the PEB process. In this section, the characterization of the PEB process is first discussed. After that, the working principle of the ellipsometry is presented.

3.2.1 Characterization of the PEB process

PEB is to thermally catalyze the chemical reaction amplifying the latent bulk image formed at exposure. It is one of the most important steps in the lithography for CD control. At the PEB step, the photoactive compound diffuses from the high density area to the low density area, in the direction of the largest concentration gradient [45].

Modelling of the photoresist properties variations through the PEB process is an active research area until today. Seligon et al. [46] described the PEB process in the form of effective dose based on the Arrhenius equation. Seligon's model states that the effective dose, ζ_{eff}, is given by:

$$\zeta_{eff} = \zeta \cdot e^{-E_a/RT} \cdot t^{\frac{1}{m}}, \tag{3.1}$$

where ζ is the radiation dose, E_a is the activation energy, R is the universal constant, T is the absolute temperature, t is the time, and m is a constant factor. The model is derived from the Arrhenius equation

$$k_c = A_e e^{-E_a/RT}, \tag{3.2}$$

where k_c is the chemical reaction rate, and A_e is the pre-exponential factor. Detailed derivation can be found in [46]. Differently, Satoru et al. employed the Dill's model and Gaussian diffusion to perform thermal modelling and simulation for the PEB effect in [47]. Chemically amplified resist has been widely used in the semiconductor industry since 1990s. The UV3 photoresist used for the experiment is a kind of chemically amplified resist, where the photo acid is generated by a photo acid generator through the light exposure. At the PEB step, the acid diffuses across the photoresist film and acts as a catalyst for chemical amplification. Park et al. [48] employed the concept of ADL to characterize the resist deprotection reactions through the PEB process for the chemically amplified resist. The ADL model is implemented to the in-situ measurement characterization in this chapter.

The details of ADL model is given as below. With Fick's second law of diffusion, molecular diffusion can be stated as

$$\frac{\partial C_A}{\partial t} = D \cdot \frac{\partial^2 C_A}{\partial z^2}, \tag{3.3}$$

where C_A is the concentration of species A, t is the PEB time, D is the diffusion coefficient of species A at the PEB temperature T, and z is the axis of diffusion direction. The diffusion coefficient D is expressed as

$$D = A_0 \cdot \exp(-E_a/RT), \tag{3.4}$$

where A_0 is the Arrhenius constant, E_a is the activation energy, and R is the universal gas constant.

The total exposure dose $Q_T = \int_0^\infty C_A(z,t)dz$ is a constant. The concentration in Equation 3.3 is solved as

$$C_A(z,t) = \frac{Q_T}{\sqrt{\pi Dt}} e^{-\frac{z^2}{4Dt}} = \frac{2Q_T}{\sqrt{2\pi\sigma^2}} e^{-\frac{z^2}{2\sigma^2}}, \tag{3.5}$$

where $\sigma = \sqrt{2Dt}$ is the ADL. According to Equation 3.4, the ADL, σ, is related to the PEB temperature, T, and time, t, as

$$\sigma = \sqrt{2tA_0}\sqrt{e^{-E_a/RT}}. \tag{3.6}$$

3.2.2 Working principle of the ellipsometry

Ellipsometry is one of the few metrology candidates that have true in-situ potential for the deep sub-micron photoresist properties analysis. As an in-situ metrology technique, ellipsometry came to the light of semiconductor manufacturing metrology in early 1990s [49]. Ellipsometry performs indirect geometrical structure measurement by analyzing the light reflectivity in a fast, accurate and non-destructive manner, which makes it an ideal candidate for the in-situ photoresist properties monitoring through the PEB process. Various kinds of ellipsometry techniques have been proposed in the literature. Optical fiber ellipsometry was presented in [50], [51], which reduced the size of ellipsometer by employing the highly birefringent fiber. It also modulated the polarization and thus eliminated the mechanical adjustment, at the cost of a more complex optical system arrangement. Another fast response ellipsometry technique was proposed in

[52], where the measurement of the light elliptical polarization was done directly via the electro-optic crystal. It allowed fast response up to 1 ms, but with the drawback of special requirements for materials. Differently, an interferometric ellipsometry was designed in [53], [54] to spatially reflect the beam and separate it to the parallel and perpendicular modes, followed by the interference measurement. It offered the high accuracy but required the double alignment that significantly reduced the measurement speed. The technique used in this chapter is the spectroscopic ellipsometry. Compared with the above mentioned other techniques, the spectroscopic ellipsometry is the promising method for the in-situ photoresist properties monitoring because it has a very simple optical device arrangement and allows a fast measurement.

The working principle of the proposed ellipsometer is very similar to the commercial product, such as SOPRA's product [55]. A typical structure of ellipsometer is shown in Figure 3.1. A linearly polarized beam is generally elliptically polarized after being reflected on a sample surface. The reflected light has phase changes that are different for the electric field components polarized parallel (p-polarized) and perpendicular (s-polarized) to the plane of incidence. The waves with the electrical field components polarized parallel and perpendicular to the incident plane are named as transverse magnetic (TM) and transverse electric (TE) waves, respectively.

Ellipsometry measures the state of polarization or more precisely the complex ratio, ρ_c, written as

$$\rho_c = \frac{r_p}{r_s} = e^{i\Delta} \tan \Psi, \tag{3.7}$$

where r_p and r_s are the reflectivity of TM and TE waves. They are stated as

$$r_p = \frac{n\cos\phi_i - \cos\phi_f}{n\cos\phi_i + \cos\phi_f}, \tag{3.8}$$

$$r_s = \frac{\cos\phi_i - n\cos\phi_f}{\cos\phi_i + n\cos\phi_f}. \tag{3.9}$$

The polar coordinates are used to present the value of ρ_c, where Δ is the phase shift, and $\tan\Psi$ is the amplitude ratio upon reflection. The parameter Ψ is the angle of the first diagonal of the rectangle in which the ellipse is enclosed. The incident and refracted angles are Φ_i and Φ_f. The complex refractive index is, $n = N_r - ik_r$, where N_r indicates the phase speed, and k_r indicates the amount of absorption loss when the electromagnetic wave propagates through the material. Ellipsometry does not require any reference as it measures a ratio rather than an absolute value.

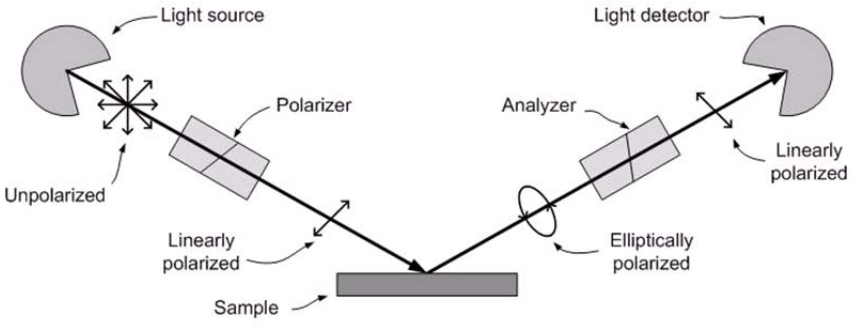

Figure 3.1: The structure of ellipsometer

The technique used in this chapter is the spectroscopic ellipsometry with the rotating polarizer method. A broadband unpolarized light is emitted from the light source. The light is then polarized by a polarizer before

falling onto the surface of the sample. The reflected light from the sample surface is subsequently polarized again by an analyzer, before being captured by a light detector. The spectrums of the reflected, polarized light with respect to the different polarizer angles are measured by a spectrometer.

In the measurement, the effect of each component in the spectroscopic ellipsometry is given by a matrix, which is described as below. These matrices are used to obtain the ellipsometric parameters $\log(\tan\Psi)$ and $\cos\Delta$.

Polarizer and analyzer are presented by the matrices P_x and A_x as below:

$$P_x = A_x = \begin{bmatrix} 1 & 0 \\ 0 & 0 \end{bmatrix}. \tag{3.10}$$

Sample is presented by the matrix E_x as below:

$$E_x = \begin{bmatrix} r_p & 0 \\ 0 & r_s \end{bmatrix}. \tag{3.11}$$

The analyzer is fixed at a certain angle to suppress the parasitic light when the polarizer is rotating. The rotation R_x of the polarizer or analyzer is presented by the following matrix:

$$R_x = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix}, \tag{3.12}$$

where θ is the variable angle of polarizer's rotation or the fixed angle of analyzer's position. Other than rotation, the effect of the lamp source is

expressed as

$$L = \begin{bmatrix} E_0 & E_0 \end{bmatrix}^T, \tag{3.13}$$

where E_0 denotes the power of the light source.

The derivation of the field amplitude on the detector can be found in [56]. The key steps are listed below. Assume P is the polarizer angle, A is the analyzer angle. On the detector, the field amplitude, E_d, is the following:

$$E_d = A_x \cdot R_x(A) \cdot E_x \cdot R_x(-P) \cdot P_x \cdot L. \tag{3.14}$$

Substitute Equations 3.10 - 3.13 into Equation 3.14, there is

$$E_d = \begin{bmatrix} \cos P \cdot E_1 + \sin P \cdot E_2 \\ \\ 0 \end{bmatrix}, \tag{3.15}$$

where $E_1 = r_p \cdot \cos A \cdot E_0$, and $E_2 = r_s \cdot \sin A \cdot E_0$. Therefore, the intensity I seen by the detector is stated as

$$I = E_d^{\dagger} \cdot E_d = \cos^2 P \cdot E_1 \cdot E_1^* + \sin^2 P \cdot E_2 \cdot E_2^* + \cos P \cdot \sin P \cdot (E_1 \cdot E_2^* + E_1^* \cdot E_2). \tag{3.16}$$

There are

$$\cos^2 P = \frac{1 + \cos 2P}{2}, \tag{3.17}$$

$$\sin^2 P = \frac{1 - \cos 2P}{2}, \tag{3.18}$$

$$\cos P \cdot \sin P = \frac{1}{2} \sin 2P. \tag{3.19}$$

Therefore, the intensity is given as

$$I = \frac{1}{2} \cdot [E_1 \cdot E_1^* + E_2 \cdot E_2^* + (E_1 \cdot E_1^* - E_2 \cdot E_2^*) \cdot \cos 2P + (E_1 \cdot E_2^* + E_1^* \cdot E_2) \cdot \sin 2P]. \tag{3.20}$$

Calculate the following equations:

$$E_1 \cdot E_1^* + E_2 \cdot E_2^* = |r_s|^2 \cdot |E_0|^2 \cdot \cos^2 A \cdot (\tan^2 \Psi + \tan^2 A), \tag{3.21}$$

$$E_1 \cdot E_1^* - E_2 \cdot E_2^* = |r_s|^2 \cdot |E_0|^2 \cdot \cos^2 A \cdot (\tan^2 \Psi - \tan^2 A), \tag{3.22}$$

$$E_1 \cdot E_2^* + E_1^* \cdot E_2 = |r_s|^2 \cdot \tan \Psi \cdot 2\cos \Delta \cdot \sin A \cdot \cos A \cdot |E_0|^2. \tag{3.23}$$

The light intensity seen by the detector is stated as

$$\begin{aligned} I &= \frac{1}{2} \cdot [E_1 \cdot E_1^* + E_2 \cdot E_2^* + (E_1 \cdot E_1^* - E_2 \cdot E_2^*) \cdot \cos 2P \\ &\quad + (E_1 \cdot E_2^* + E_1^* \cdot E_2) \cdot \sin 2P] \\ &= \frac{1}{2}\{|r_s|^2 \cdot |E_0|^2 \cdot \cos^2 A \cdot (\tan^2 \Psi + \tan^2 A) \\ &\quad + [|r_s|^2 \cdot |E_0|^2 \cdot \cos^2 A \cdot (\tan^2 \Psi - \tan^2 A)] \cdot \cos 2P \\ &\quad + (|r_s|^2 \cdot \tan \Psi \cdot 2\cos \Delta \cdot \sin A \cdot \cos A \cdot |E_0|^2) \cdot \sin 2P\}. \end{aligned} \tag{3.24}$$

Therefore, the intensity I seen by the detector is given as

$$I = I_0 \cdot (\alpha \cdot \cos 2P + \beta \cdot \sin 2P + 1), \tag{3.25}$$

where

$$I_0 = \frac{1}{2} \cdot |r_s|^2 \cdot |E_0|^2 \cdot \cos^2 A \cdot (\tan^2 \Psi + \tan^2 A), \tag{3.26}$$

$$\alpha = \frac{\tan^2 \Psi - \tan^2 A}{\tan^2 \Psi + \tan^2 A}, \tag{3.27}$$

$$\beta = 2\cos \Delta \cdot \frac{\tan \Psi \cdot \tan A}{\tan^2 \Psi + \tan^2 A}. \tag{3.28}$$

The ellipsometric parameters $\log(\tan \Psi)$ and $\cos \Delta$ are expressed versus α and A as

$$\log(\tan \Psi) = \log \left(\sqrt{\frac{1+\alpha}{1-\alpha}} \tan A \right), \tag{3.29}$$

$$\cos \Delta = \frac{\alpha}{\sqrt{1-\alpha^2}}. \tag{3.30}$$

The spectroscopic ellipsometry samples the time-variant signal for a few periods when the polarizer is rotating, and then converts the acquired variables into the ellipsometric parameters. The reflected, polarized light that has been digitized by the spectrometer is then integrated every quarter of the half-turn of the polarizer according to the following equations:

$$S_1 = \int_0^{\pi/4} I(P)dP = \frac{I_0}{2}\left(\frac{\pi}{2} + \alpha + \beta\right), \tag{3.31}$$

$$S_2 = \int_{\pi/4}^{\pi/2} I(P)dP = \frac{I_0}{2}\left(\frac{\pi}{2} - \alpha + \beta\right), \tag{3.32}$$

$$S_3 = \int_{\pi/2}^{3\pi/4} I(P)dP = \frac{I_0}{2}\left(\frac{\pi}{2} - \alpha - \beta\right), \tag{3.33}$$

$$S_4 = \int_{3\pi/4}^{\pi} I(P)dP = \frac{I_0}{2}\left(\frac{\pi}{2} + \alpha - \beta\right). \tag{3.34}$$

Therefore, α, β and I_0 are obtained as below.

$$\alpha = \frac{1}{2I_0}(S_1 - S_2 - S_3 + S_4), \tag{3.35}$$

$$\beta = \frac{1}{2I_0}(S_1 + S_2 - S_3 - S_4), \tag{3.36}$$

with

$$I_0 = \frac{1}{\pi}(S_1 + S_2 + S_3 + S_4). \tag{3.37}$$

After that, the ellipsometric parameters $\log(\tan\Psi)$ and $\cos\Delta$ can be obtained by Equation 3.29 and 3.30.

3.3 Equipment Setup

The working theory of the in-situ metrology has been discussed in the previous section. In this section, the equipment setup of the PEB thermal bake-plate and spectroscopic ellipsometer is discussed. It builds the system to examine the working theory.

3.3.1 Programmable thermal bake-plate

The proposed CD control experiments are designed for the 4-inch wafer. All the equipments, including the spin coater, exposure tool, and spectroscopic ellipsometer, are designed for the 4-inch wafer only. A programmable multi-zone bake-plate is developed for the thermal processing of 4-inch wafer as well. The bake-plate is similar to the one developed in Chapter 2. It comprises an array of heating zones that allow for spatial control of temperatures in nonsymmetric configurations. Resistive heating elements are embedded within each of the baking zones. Heat is supplied to each of the resistive heating elements by embedding a 3.2 mm cylindrical cartridge heater that is commercially available from Watlow, Inc. A RTD sensor available from Honeywell is also inserted into each zone of the bake-plate, and attached to the surface of the bake-plate with thermally conductive glue to measure temperatures. Each heating zone is configured with its own temperature sensor and electronics for feedback control. The heating electronics consist of a PWM and a SSR for voltage control. The heating zones are separated with a small air gap of approximately 1 mm. The fact that the zones are spatially disjoint ensures no significant thermal coupling between each other. Its small thermal mass allows for fast dynamic manipulation of the temperature profile. Moreover, the number of heating zones of the bake-plate can be easily modified.

In this chapter, the above mentioned bake-plate is implemented to the PEB step. The configurations of the thermal bake-plate are shown in Figure 3.2. The equipment setup and control algorithm of the proposed 4-inch

bake-plate are similar to the 8-inch bake-plate presented in Chapter 2. The bake-plate is divided into the center and edge zones. Each zone is connected to the power supply and computer through a SSR. The power inputs to the bake-plate center and edge are adjusted appropriately on the basis of spectroscopic ellipsometry measured results. There are also two temperature sensors inserted into the bake-plate center and edge zones and attached to the surface of the bake-plate with thermally conductive glue. They perform in-situ real-time measurements of the bake-plate temperatures throughout the PEB process. The National Instrument (NI) devices are used to read the measurements and send out the control signals.

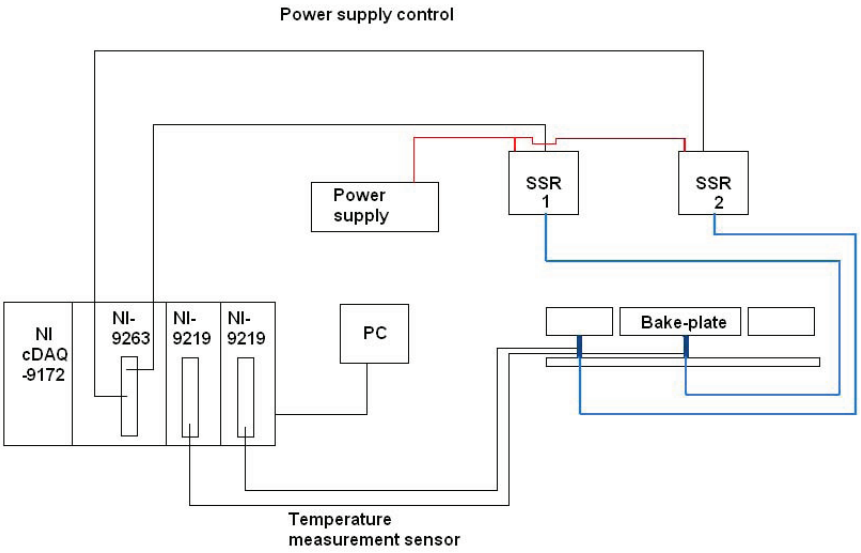

Figure 3.2: Thermal bake-plate configurations

3.3.2 Spectroscopic ellipsometer

3.3.2.1 Single probe spectroscopic ellipsometer

A single probe spectroscopic ellipsometer is fist developed. The setup of its main components is stated as below:

1. Stepper motor for polarizer, with accuracy of 80 arc-seconds, repeatability of 15 arc-seconds, and speed of 16 rpm.

2. Polarizer and analyzer extinction rate of 1000:1, rotation of 360°.

3. Spectrometry of visible light / near infrared range.

4. Broadband light source.

5. Analyzer angle set to -30°.

The design of the proposed spectroscopic ellipsometry is done with the mechatronics approach [57] as it requires a synergy between the electromechanical systems with the optical system. The core of the mechatronics design is the synchronization of the stepper motor and spectrometer. The single probe spectroscopic ellipsometer setup is shown in Figure 3.3. The polarizer is positioned on the left, while the analyzer is directly opposite the polarizer. Both of them are held by the independent arms, which are movable through the angular slots on the main stage. The wafer sample is placed on the bake-plate located at the light path such that the light reflection is inline with the analyzer arm's axis. The light source is a ultraviolet (UV) / visible light (VIS) / near infrared (NIR) source. It is connected to the polarizer via an optical fiber cable through a subminiature version A connector, which minimizes the light intensity loss. The reflected light is

captured by the light receptor, and then sent to the spectrometer.

The operation, including the rotation of the polarizer motor, is controlled via virtual instrumentation software of LabVIEW. It drives the stepper motor and reads the measurement of the spectrometer. The angular range of the polarizer can also be modified via the software, allowing the variation of the range of polarizer rotation to achieve an optimum trade-off between parasitic light suppressing and measurement speed. Homing of the polarizer is another important feature. The rotating polarizer method requires a known polarization state. Therefore, the polarization should always start from the same angular location, which is done by the homing function.

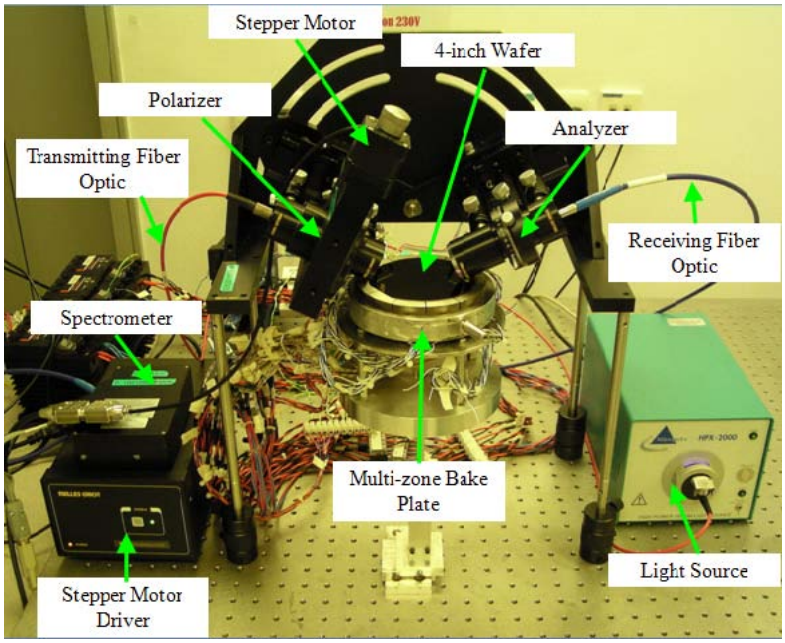

Figure 3.3: Single probe spectroscopic ellipsometer setup

3.3.2.2 Dual-probe spectroscopic ellipsometer

It is easy to upgrade a single probe spectroscopic ellipsometer to a dual-probe spectroscopic ellipsometer by adding extra sets of probes where they have exactly the same working principle. The design of a dual-probe spectroscopic ellipsometer is presented in Figure 3.4. One set of optical components, including a polarizer and an analyzer, are added to the original system, where two sets of probes are 4 cm apart. One set is to measure the CD latent image at the wafer center, and the other set is to measure the CD latent image at the wafer edge. All the other hardware configurations of the proposed dual-probe spectroscopic ellipsometer are exactly the same as the single probe spectroscopic ellipsometer except the analyzer angle is set to 30° due to the hardware limitations. The photo of the proposed dual-probe spectroscopic ellipsometry system is shown in Figure 3.5. In Chapter 4, this dual-probe spectroscopic ellipsometry system will be further discussed and used for across wafer CD uniformity control.

3.4 Experimental Results and Discussions

This section experimentally investigates the capability of spectroscopic ellipsometry for in-situ photoresist properties monitoring throughout the PEB process. The 4-inch wafers are processed with the same recipe prior to the PEB step. Therefore, all the wafers have the same incoming condition. At the PEB step, experiments are conducted for the different baking time and temperatures. The single probe spectroscopic ellipsometer is used to

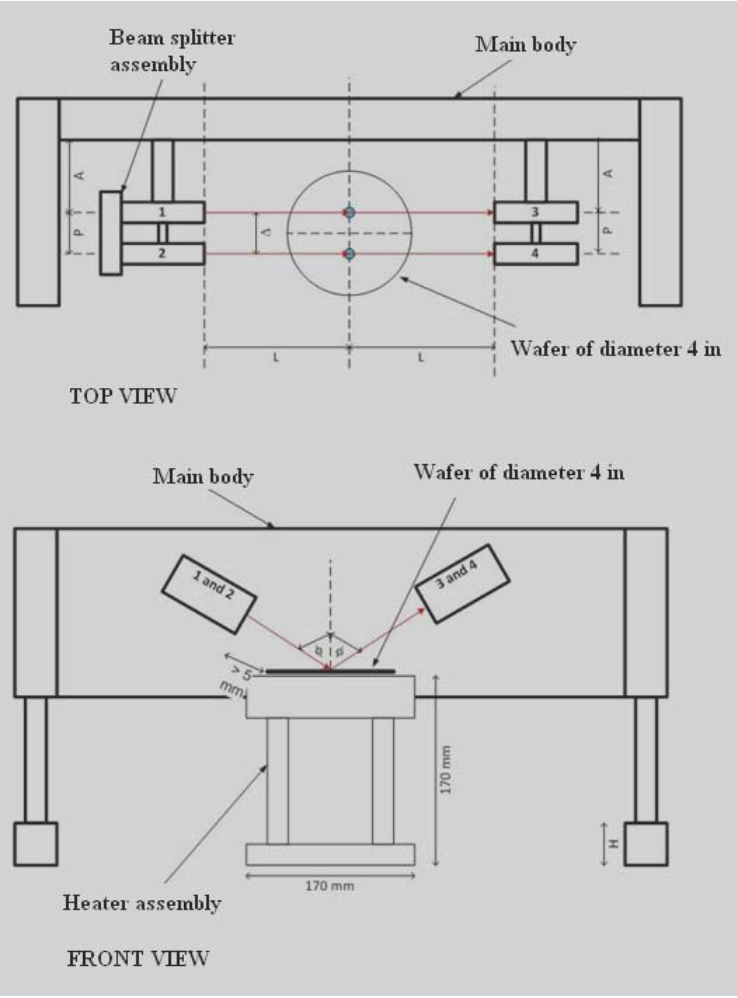

Figure 3.4: Design of the dual-probe ellipsometer

perform the in-situ photoresist properties measurements.

ADL model is used to describe the variation of photoresist properties throughout the PEB process. There is $ADL = \sqrt{2tA_0}\sqrt{e^{-E_a/RT}}$, where t is the baking time, A_0 is the Arrhenius constant, E_a is the activation energy around 0.28 ev or 26970 J/mol, R is the universal constant and equals to 8.314472 J/K·mol, and T is the baking temperature. State two wafers A and B which run the same recipe prior to the PEB step. However, Wafer A is baked at T_1 for t_1 while Wafer B is baked at T_2 for t_2. The following

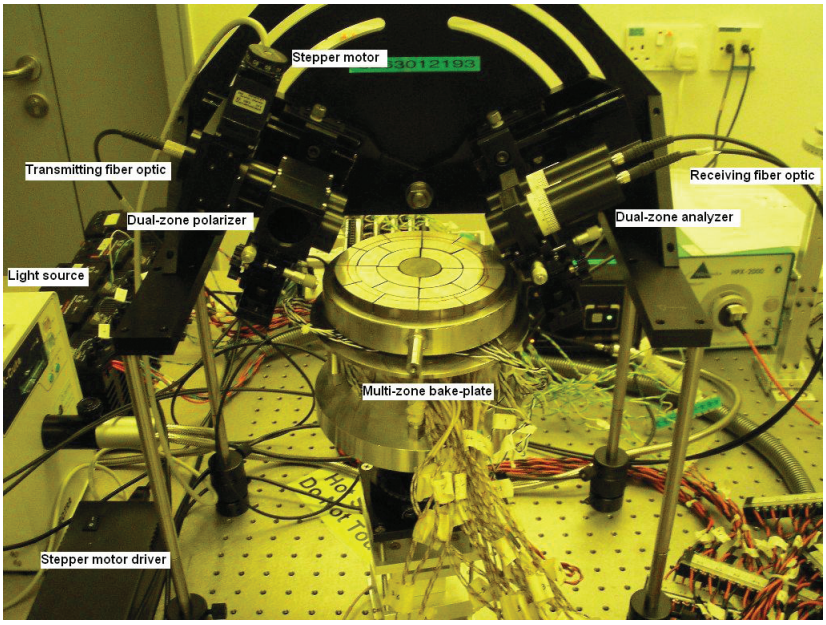

Figure 3.5: Dual-probe spectroscopic ellipsometer setup

equation must be satisfied if Wafers A and B have the same ADL result:

$$\sqrt{2t_1A_0}\sqrt{e^{-E_a/RT_1}} = \sqrt{2t_2A_0}\sqrt{e^{-E_a/RT_2}}. \tag{3.38}$$

Remove the common items on both sides, the equation becomes

$$t_1 e^{-\frac{E_a}{RT_1}} = t_2 e^{-\frac{E_a}{RT_2}}. \tag{3.39}$$

Rearrange the equation, the relationship between t_1 and t_2 is stated as

$$t_1 = \exp\left(\frac{E_a}{R} \cdot \left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right) \cdot t_2. \tag{3.40}$$

The experiments are designed appropriately on the basis of ADL model. Prior to the PEB step, all the wafers are processed step by step as below:

1. The 4-inch wafers are spin-coated with Shipley UV3 positive photoresist at 6000 rpm for 55 sec.

2. The wafers are sent for soft bake at 120 °C for 90 sec.

3. The wafers are exposed for 2.6 sec at 6.1 mJ/cm^2.

At the PEB step, four experiments are designed as shown in Table 3.1. The inspected area is on the wafer center and patterned with a periodic line grating with the width of 500 nm.

Table 3.1: Experiment design

	Post-Exposure Bake	
Experiment Series	Stage 1: First 45 sec	Stage 2: Next 80 sec
E1	140 °C	140 °C
E2	130 °C	130 °C
E3	145 °C	145 °C
E4	130 °C	145 °C

Experiments are used to examine how the spectroscopic ellipsometry measurement changes with the PEB baking time and temperature. Experiments E1, E2 and E3 only have one bake temperature throughout the PEB process. Experiment E4 has a temperature change during the PEB process. However, E1 and E4 are expected to have the same photoresist properties after the PEB process is completed according to Equation 3.40. The PEB process is divided into two stages: first 45 sec and rest 80 sec. For E4, the first stage is baking at 130 °C for 45 sec, which is equivalent to baking at 145 °C for 34 sec as per Equation 3.41:

$$t_{eq1} = \exp\left(\frac{26970}{8.314472} \cdot \left(\frac{1}{418} - \frac{1}{403}\right)\right) \cdot 45\ sec = 34\ sec. \tag{3.41}$$

E4 stage 2 is baking at 145 °C for 80 sec. Therefore, E4 is equivalent to baking at 145 °C for 114 sec. Recalling Equation 3.40, E4 is equivalent to baking at 140 °C for 125 sec or Experiment E1 as per Equation 3.42:

$$t_{eq2} = \exp\left(\frac{26970}{8.314472} \cdot \left(\frac{1}{413} - \frac{1}{418}\right)\right) \cdot 114\ sec = 125\ sec. \tag{3.42}$$

A total of 400 wafers are used for the experiment, which is equivalent to 20 lots of data with each lot consists of 20 wafers. The results are

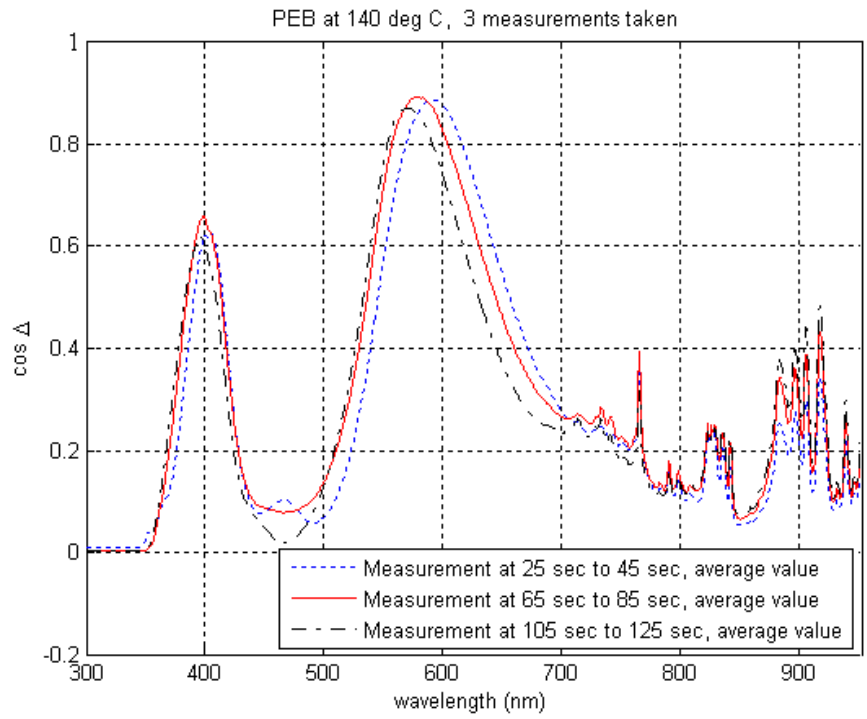

Figure 3.6: Thermal effect for PEB bake at 140°C

satisfactorily consistent, and the result of one lot is shown as below for the illustration purpose. There are twenty wafers in the sampled lot. Wafer 1 to Wafer 5 run Experiment E1, Wafer 6 to Wafer 10 run Experiment E2, Wafer 11 to Wafer 15 run Experiment E3, and Wafer 16 to Wafer 20 run Experiment E4. It is noted that the ellipsometric parameter, $\cos\Delta$, is more sensitive than $\log(\tan\Psi)$ because it only ranges from -1 to 1. Therefore, $\cos\Delta$ is used for the process analysis. The experimental results are plotted in Figures 3.6 to 3.8. The average values are used to obtain a better comparison.

Several conclusions can be derived from the experimental results. Firstly, the relationship between the baking time and the measured signature is discussed. In E1, five wafers are baked at 140 °C for 125 sec. The spec-

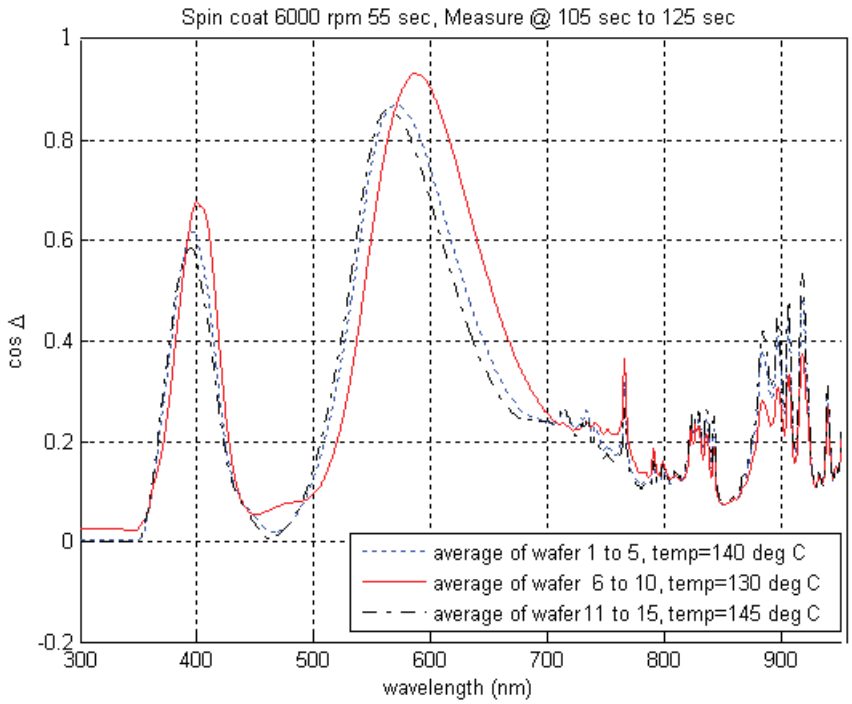

Figure 3.7: Thermal effect with baking temperature for PEB, measured at 125s

troscopic ellipsometry measurements are taken at 45 sec, 85 sec, and 125 sec, respectively. From the signatures plotted in Figure 3.6, it is observed that the measured signature moves from right to left as the baking time increases. Secondly, the relationship between the baking temperature and the measured signature is discussed. E2 and E3 are conducted and compared with E1. In E2 and E3, five wafers are used for each run and baked at 130 °C and 145 °C for 125 sec, respectively. The cosine signatures of them, together with E1, are plotted in Figure 3.7. It is also observed that the measured signature moves from right to left as the baking temperature increases.

In the previous two aspects, one baking temperature lasts for the entire

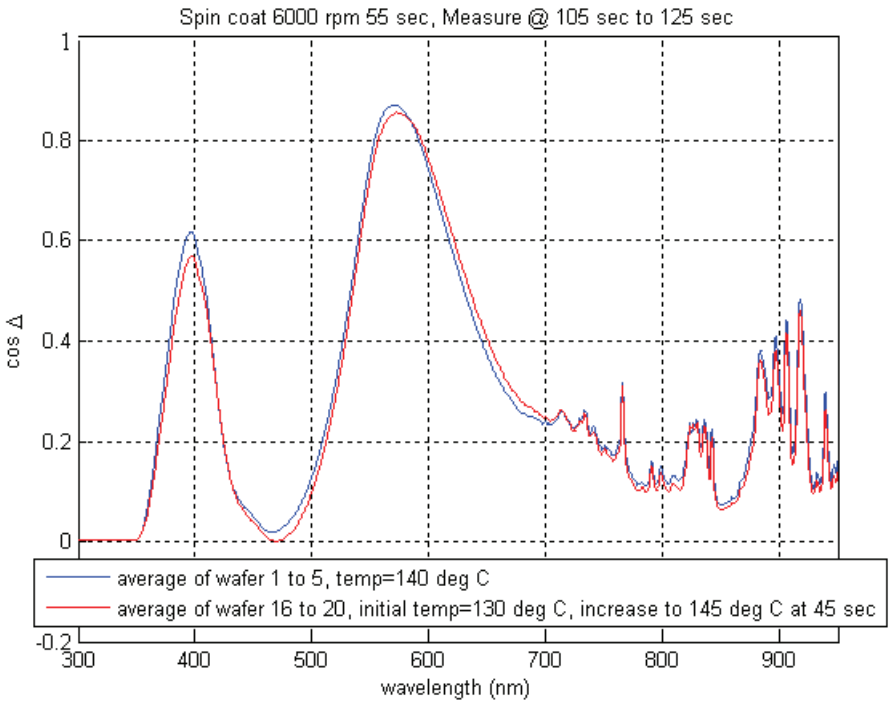

Figure 3.8: Thermal effect with the change of baking temperature in the middle

PEB process. However, Experiment E4 has a baking temperature change in the middle of the PEB process. The baking temperature starts from 130 °C and lasts for 45 sec, then increases to 145 °C and lasts for the rest 80 sec. The results of E4 and E1 are both plotted in Figure 3.8. It finds that their measured signatures are almost identical. The SEM analysis is conducted on the samples for further verification. The results are shown in Figure 3.9. It is clear that the CD results of E1 and E4 share the similar profile as compared with E2.

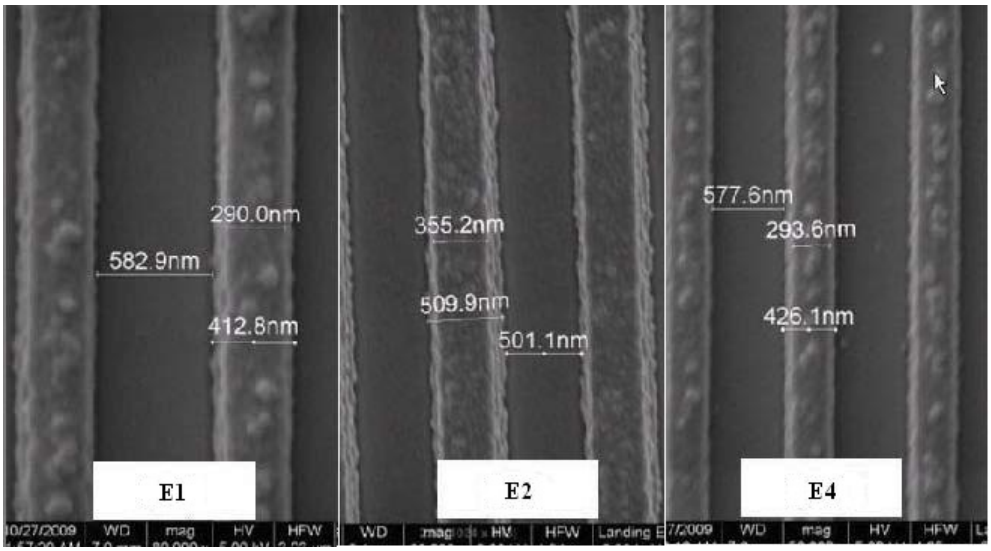

Figure 3.9: SEM result

3.5 Conclusion

In this chapter, an spectroscopic ellipsometry system has been developed for in-situ photoresist properties monitoring at the PEB step. The modelling of the PEB process and the working principle of the ellipsometry have been first reviewed. After that, the spectroscopic ellipsometry has been novelly implemented to the PEB process for in-situ photoresist properties measurements. From the experimental results, it has been observed that the ellipsometry measured signature changed with the PEB baking time and temperature. Empirically, the spectroscopic ellipsometry measured signature has moved from right to left as baking time or temperature increased. Moreover, it has been demonstrated that the spectroscopic ellipsometry measured signature could be controlled on target by manipulating the PEB baking time and temperature on the basis of ADL model. This implies that the CD value can be controlled on target by manipulating the

PEB baking time and temperature appropriately. In Chapter 4, an across wafer in-situ real-time CD monitoring and control system will be developed on the basis of current works.

Chapter 4

Dual-Zone Real-Time Monitoring and Control of Critical Dimensions

4.1 Introduction

CD is the most important parameter in the lithography process. The across wafer gate CD uniformity strongly affects the final chip-to-chip performance spread in terms of speed and power. Effective control of across wafer CD uniformity results in a tighter distribution of chip speed and power consumption. This, in turn, results in more consistent chip performance and higher yield [19]. However, significant across wafer CD nonuniformity may be observed at the end of lithography process for traditional conventional baking, which is due to but not limited to the following reasons: (1) the thermal transfer is not uniform across the wafer; (2) the initial condition

of the photoresist is not uniform across the wafer; (3) the perturbation during the PEB process affects the photoresist reaction and final CD result. These observations motivate us to develop a formal control method for across wafer CD uniformity improvement.

In the literature, extensive research has been conducted in CD uniformity control. The CD variation at R2R or wafer-to-wafer level was generally solved by the advanced process control [58] - [61]. In these works, CD data was used to correct the perturbations from process. The average CD of wafer was regulated, and the wafer-to-wafer CD variation was minimized. Across wafer CD uniformity is becoming dominant as technology advances. It requires that process control moves beyond the R2R or wafer-to-wafer level to the across wafer level. The in-situ real-time technique was widely used for across wafer photoresist properties uniformity control. In [8], [62] - [63], Tay et al. performed a series of approaches to in-situ real-time monitoring and control of the across wafer photoresist properties, such as wafer temperature, photoresist extinction coefficient and photoresist thickness, at the baking step. However, these approaches cannot measure the CD profile directly. A more straightforward approach for across wafer CD uniformity control is needed.

Throughout the lithography, the final CD value is strongly related to the thermal processing steps, such as PEB [5]. Paulsson et al. [64] examined the relationship between the PEB time, temperature and final CD linewidth by a series of experiments. It can be seen that the three-dimensional CD profile is significantly affected by the PEB temperature profile. In this

chapter, an in-situ real-time across wafer CD uniformity control method is developed and applied to the PEB step. A dual-probe spectroscopic ellipsometer is built and integrated with a dual-zone programmable thermal bake-plate. A physical model based on the rigorous coupled-wave analysis (RCWA) is used to characterize the CD latent image profile in terms of the spectroscopic ellipsometry in-situ measurement. Based on the spectroscopic ellipsometry in-situ measurements, a real-time control method is applied at the PEB step to real-time adjust the power inputs to the bake-plate center and edge, respectively. Compared with previous works, the proposed approach provides a straightforward way for in-situ real-time CD monitoring and control at the PEB step. A significant across wafer CD uniformity improvement is observed from the experiments.

The rest of Chapter 4 is organized as follows. In Section 4.2, the RCWA model is introduced, which characterizes the CD latent image profile in terms of the spectroscopic ellipsometry measurement. The real-time control algorithm and experimental results are then presented in Section 4.3. The conclusion is given in Section 4.4.

4.2 Measurement of CD Latent Image

The spectroscopic ellipsometer is employed to perform in-situ CD latent image profile measurement through the PEB process. The measurements are presented in terms of cosine signatures. This section builds a model to relate the cosine signature to the CD latent image profile.

Processing of photoresist is first studied. In the experiment, UV3 positive photoresist is used, which is a kind of chemically amplified resists. After exposure, the properties of exposed photoresist change significantly [65], [66]. Because the refractive index is different between the exposed and unexposed areas, the CD latent image profile structure can be treated as a diffraction grating. A cross-sectional geometric structure of the CD latent image is shown in Figure 4.1. It is actually a one-dimensional periodic grating structure, which can be characterized by the RCWA technique.

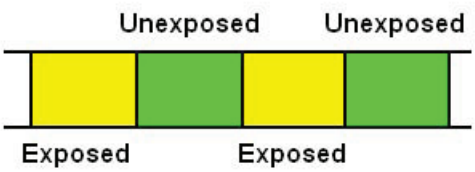

Figure 4.1: CD latent image grating structure

4.2.1 Approach with RCWA

RCWA was firstly proposed by Moharam and Gaylord in [67]. It is one of the most widely used techniques for the accurate analysis of the optical diffraction of periodic gratings. The RCWA computation consists of two steps. First, the Fourier expansion of the field inside the grating leads to a system of differential equations. A set of second-order differential equations can be used instead of first-order differential equations. The modifications

from first-order to second-order differential equations dramatically reduce the computation time and the memory requirements. Second, electromagnetic boundary conditions require that the tangential electric and tangential magnetic fields should be continuous across the boundaries between two non-conductive layers. Once the eigenvalues and the eigenvectors of this grating system are found, the boundary conditions at the grating interfaces are matched to compute the electric and magnetic fields. The details of RCWA can be found in [68]. Based on the RCWA theory, we use MATLAB to develop the model, which relates the spectroscopic ellipsometry measurement to the CD latent image. Two models are built: a one-layer model and a ten-layer model. For the one-layer model, only one layer of photoresist exists between the superstrate layer, i.e. air, and the substrate layer, i.e. silicon wafer. The CD latent image profile in the photoresist is presented in terms of the CD latent image linewidth w_1 and the film thickness h_1. For the ten-layer model, ten layers of photoresist exist between the superstrate layer and the substrate layer. The CD latent image profile at l-th layer is presented in terms of the CD latent image linewidth at l-th layer, w_l, and the l-th layer film thickness, h_l. In the next subsection, the one-layer model is compared with the ten-layer model. It states that the one-layer model performs as well as the ten-layer model, with less calculation cost. It also shows that the one-layer model fits the experimental result appropriately.

4.2.2 Model verification

The accuracy and consistency of the one-layer model is verified in this subsection. The one-layer model is first compared with the ten-layer model. After that, the experimental results are fitted into the one-layer model to check the consistency between model and experiment.

Photoresist properties are first studied before building the model. Shipley UV3 positive photoresist is used for the experiments because of its great post-exposure stability. The Cauchy coefficients of UV3 resist are n_1=1.5247, $n_2 = 4.17 \times 10^5$, and $n_3 = 4.61 \times 10^{12}$, the refractive index is

$$n(\lambda) = n_1 + n_2/\lambda^2 + n_3/\lambda^4, \tag{4.1}$$

where λ is the wavelength. After exposure, n_1 slightly decreases to 1.2607, and there are not too much variations on the other two parameters. A 1000 nm periodic grating mask with 1:1 duty cycle ratio is used at the exposure step, where the linewidth of exposed and unexposed areas are both 500 nm. Both the one-layer and ten-layer models are developed based on the given photoresist properties. Set the photoresist film thickness at 420 nm, each layer of the ten-layer model is with 42 nm thickness. The comparison between the one-layer and ten-layer models for an ideal unslanted sample is shown in Figure 4.2. The two signatures are exactly the same.

Next, a sloped CD latent image profile is used for the ten-layer model: bottom CD linewidth of ridge = 509 nm, top CD linewidth of ridge = 491 nm, each layer in between decreases by 2 nm from the bottom to top, and the average CD linewidth is still 500 nm. The comparison between the one-

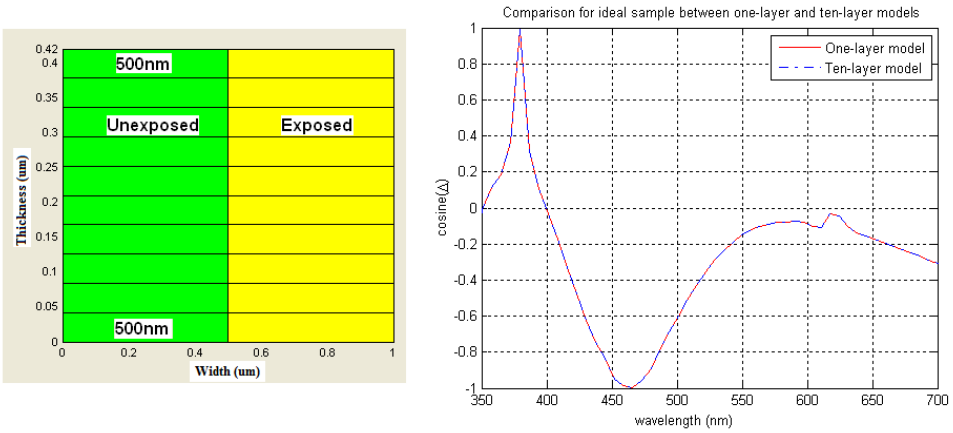

Figure 4.2: Comparison between one-layer and ten-layer models for an ideal unslanted sample

layer and ten-layer models for the sloped sample is shown in Figure 4.3. The mean square error between two signatures is only 0.005 which is negligible. It concludes that the one-layer model performs a good approximation to the ten-layer model.

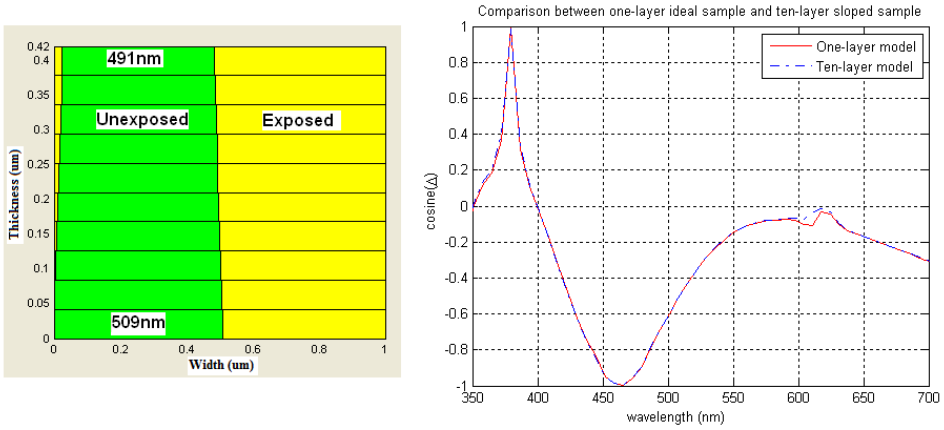

Figure 4.3: Comparison between the ideal unslanted sample in one-layer model and the sloped sample in ten-layer model

After that, experiments are conducted to verify the consistency of the one-layer model. Two samples are used for investigation. The post development CD profile of Sample 1 is of 500 nm linewidth in valley, 420 nm in height. The post development CD profile of Sample 2 is of 475 nm

linewidth in valley, 430 nm in height. SEM is used for sample verification, and the result is shown in Figure 4.4. UV3 photoresist has high selectivity at the development step. The same CD latent image profile can be assumed at the PEB step. The spectroscopic ellipsometry measurements on these two samples at the PEB step are plotted in Figures 4.5 and 4.6, together with the simulation results of the one-layer grating model.

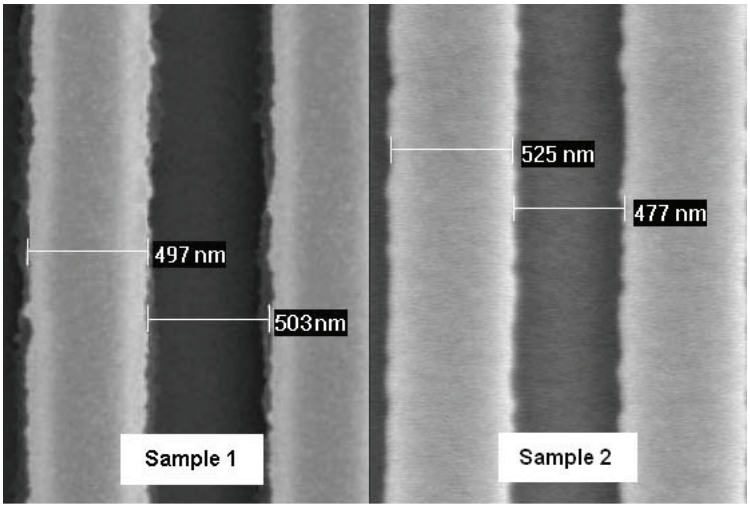

Figure 4.4: Post-development DICD SEM verification

Because of the limitations on physical properties, the spectroscopic ellipsometry measurements may not be able to catch some spikes in the simulation at certain wavelengths. However, it can be observed that the spectroscopic ellipsometry measurements and simulation results are almost matched within the wavelength range of 350 - 700 nm. Therefore, the capability of the one-layer diffraction grating model is verified.

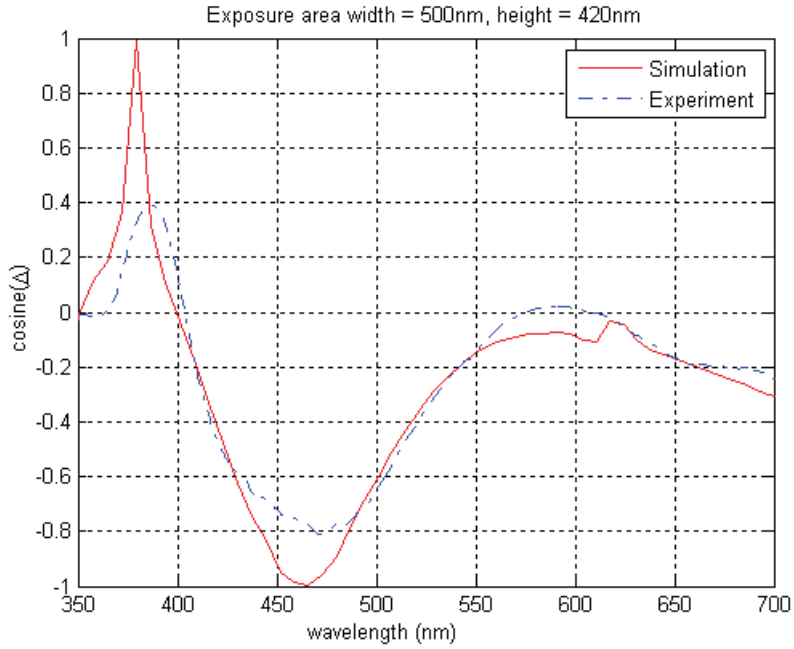

Figure 4.5: Simulation and experimental results for 500 nm CD latent image profile with 420 nm thickness

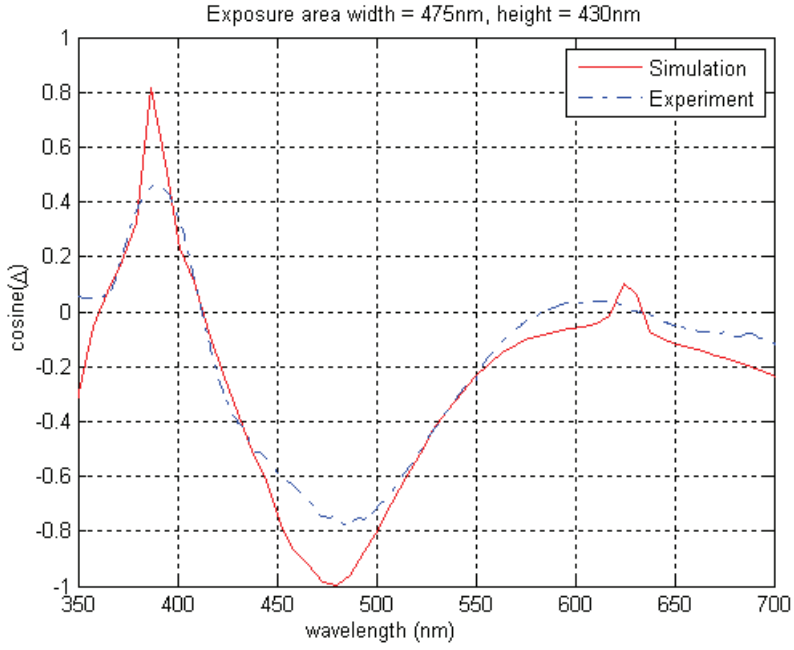

Figure 4.6: Simulation and experimental results for 475 nm CD latent image profile with 430 nm thickness

4.2.3 Extraction of CD latent image profile from spectroscopic ellipsometry measurement

Previous subsection indicates that the CD latent image profile is presented in terms of spectroscopic ellipsometry measurement $\cos\Delta$. In this subsection, the inverse CD latent image profile extraction from the spectroscopic ellipsometry measurement is investigated. A library is built. It contains a number of simulations, i.e. $\cos\Delta$, and the corresponding CD latent image profile, on the basis of the one-layer model mentioned in Subsection 4.2.2. Specifically, the CD latent image profiles in the library are described by two parameters: the linewidth w_1 and the height h_1 of the exposed area. The ideal CD latent image profile in the experiment is with 500 nm linewidth and thickness ranges from 420 nm to 440 nm. When the CD latent image profiles are established, w_1 starts from 460 nm and increases at a step size of 10 nm until 540 nm, h_1 starts from 420 nm and increases at a step size of 5 nm until 440 nm. There are total 45 references in the library. On the other hand, when the spectroscopic ellipsometer performs the in-situ measurement, the measured signature is compared with all the simulated $\cos\Delta$ in the library by calculating the mean-square-error (MSE) stated as

$$MSE = \frac{\sum_{\lambda=\lambda_1}^{\lambda=\lambda_n}(\cos(\lambda)_{Measurement} - \cos(\lambda)_{Reference})^2}{n}. \tag{4.2}$$

The most matched simulated $\cos\Delta$ is then chosen, and the corresponding CD latent image profile is stated as the extraction result.

The experiment is conducted to illustrate the feasibility of library and extraction process. A 500 nm CD shown in Figure 4.4 Sample 1 is generated

step by step as the following standard recipe:

1. The 4-inch wafer is coated with Shipley UV3 positive photoresist at 6000 rpm for 55 sec.

2. The wafer is sent for soft bake at 120 °C for 90 sec.

3. The wafer is exposed for 2.6 sec at 6.1 mJ/cm^2 through a 1000 nm square grating mask with 1:1 duty cycle ratio.

4. The wafer is sent for PEB. The PEB is conducted at 130 °C for 125 sec. The spectroscopic ellipsometer performs in-situ real-time measurement on the wafer center through the PEB process.

5. The wafer is immersed in the MF CD-26 developer solution for 10 sec, followed by rinsing with deionized (DI) water.

A CD profile with 503 nm valley linewidth and 420 nm height is revealed on the wafer center at the end of process. The measurements taken at the 25 sec, 65 sec and 125 sec of the process are presented in terms of $\cos\Delta$ signatures and shown in Figure 4.7.

The experimental results are matched to the simulated $\cos\Delta$ signatures in the library. The corresponding CD latent image profiles are then extracted and stated in Table 4.1, and shown in Figure 4.8. It can be seen that the extracted CD latent image profile at the end of process is of 510 nm linewidth and 420 nm thickness, which are very close to the dimensions of Sample 1 in Figure 4.4.

Table 4.1: CD latent image profile characterizations

	width(w_1)	height(h_1)
25 sec	470 nm	435 nm
65 sec	490 nm	425 nm
125 sec	510 nm	420 nm

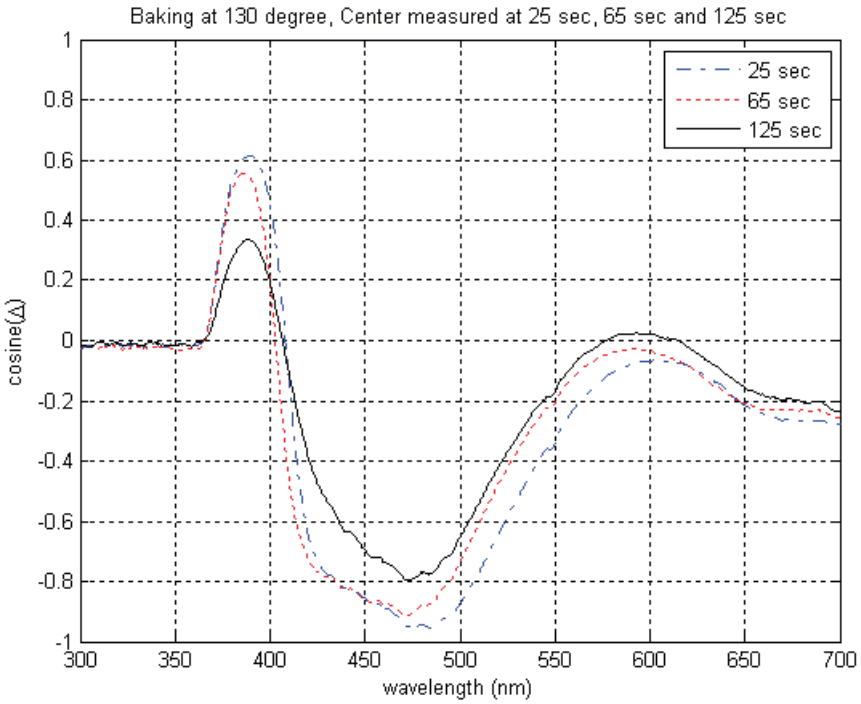

Figure 4.7: Inline measured cosine signatures through PEB

4.3 Control Framework and Experimental Results

The previous section verifies the capability of spectroscopic ellipsometry for in-situ real-time CD latent image profile measurement. Based on the spectroscopic ellipsometry technique, the dual-zone real-time CD monitoring and control system is implemented to the PEB step in this section. Moreover, experiments are conducted to examine the effectiveness of the dual-zone system for CD uniformity improvement.

4.3.1 Control framework

Real-time CD control is presented in this subsection. Figure 4.9 shows the framework of this real-time control method, where e_1 and e_2 are the differ-

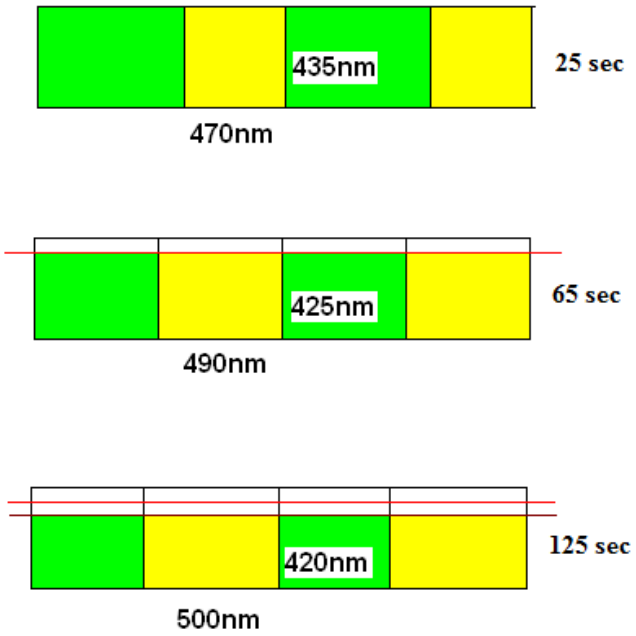

Figure 4.8: CD latent image profile variations throughout the PEB process

ences between the spectroscopic ellipsometry measurement and reference at the wafer center and edge, K_{p1} and K_{p2} are the proportional gains, Δu_1 and Δu_2 are the changes of power inputs to the bake-plate center and edge, ΔT_{p1} and ΔT_{p2} are the changes of temperatures of the bake-plate center and edge, D_c is the decoupling matrix, $G_{new,wfr-to-u}$ is the transfer function between the wafer temperatures and the power inputs after decoupling the thermal effects.

The working principle of the framework is presented as below. The CD latent image variations, on both wafer center and edge zones, are in-situ real-time measured by the dual-probe spectroscopic ellipsometer throughout the PEB process. The measurements are then compared with the reference. The differences between them are minimized by real-time adjusting the power inputs to the center and edge zones accordingly, which improves

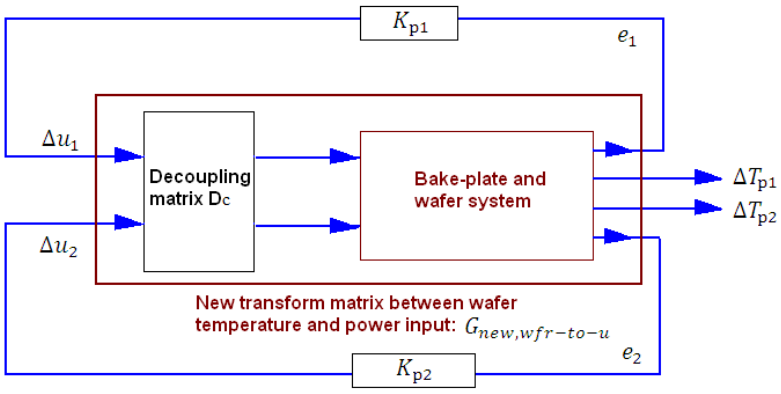

Figure 4.9: The scheme of the real-time control approach

the across wafer CD uniformity. Different from conventional baking, the real-time control method adjusts the power inputs to the bake-plate directly instead of using PI controllers to maintain the temperature, for ease of tuning. It is also worth noting that a decoupling matrix is employed in the framework, which allows us to control the wafer center and edge temperatures independently regardless of the good thermal conductivity of the silicon wafer.

Two issues need to be addressed before the framework is implemented. One is to identify e_1 and e_2. Define n_0 as the total data points, and 400 - 550 nm as the observation wavelength range for a 500 nm CD, the real-time MSEs between the measurements and reference at time t for the center and edge zones are

$$e_1(t) = \frac{\sum_{\lambda=400nm}^{\lambda=550nm}(\cos(\lambda,t)_{Measurement,Center} - \cos(\lambda,t)_{Reference})^2}{n_0} \cdot sign(\cos(550nm,t)_{Reference} - \cos(550nm,t)_{Measurement,Center}), \quad (4.3)$$

$$e_2(t) = \frac{\sum_{\lambda=400nm}^{\lambda=550nm}(\cos(\lambda,t)_{Measurement,Edge} - \cos(\lambda,t)_{Reference})^2}{n_0} \cdot sign($$
$$\cos(550nm,t)_{Reference} - \cos(550nm,t)_{Measurement,Edge}). \quad (4.4)$$

Based on $e_1(t)$ and $e_2(t)$, two controllers adjust the power inputs to the bake-plate center and edge zones accordingly. The proportional gains K_{p1} and K_{p2} are both set to 10 after several iterations of tuning.

The other issue is to design the decoupling matrix. The thermal coupling analysis is conducted for both the bake-plate and wafer, and their results are stated in Tables 4.2 and 4.3, where u_1 is the power input to bake-plate center, u_2 is the power input to bake-plate edge, T_{p1} is the bake-plate center temperature, T_{p2} is the bake-plate edge temperature, T_{w1} is the wafer center temperature, T_{w2} is the wafer edge temperature, and Δ indicates the variation. The tables state how the wafer and bake-plate temperatures change with the power inputs, at both center and edge zones.

Table 4.2: Thermal coupling analysis

u_1	u_2	T_{p1}°C	T_{p2}°C	T_{w1}°C	T_{w2}°C
0.77	1.78	130	130	114.2	112.0
0.95	1.74	135	130	116.5	113.2
0.59	1.83	125	130	112.0	110.7
0.65	1.92	130	135	115.2	114.0
0.90	1.67	130	125	113.0	109.8

Table 4.3: Temperature variation vs Power input variation

Δu_1	Δu_2	ΔT_{p1}°C	ΔT_{p2}°C	ΔT_{w1}°C	ΔT_{w2}°C
0.18	-0.04	5	0	2.3	1.2
-0.18	0.05	-5	0	-2.2	-1.3
-0.12	0.14	0	5	1.0	2.0
0.13	-0.11	0	-5	-1.2	-2.2

The transformation matrices between wafer temperature, bake-plate temperature and power inputs are then derived by using the linear fitting

of data from Table 4.3. They are stated as below:

$$G_{bp-to-u} = \begin{bmatrix} 35.87 & 34.82 \\ 11.95 & 50.70 \end{bmatrix}, \tag{4.5}$$

$$G_{wfr-to-u} = \begin{bmatrix} 18.64 & 26.59 \\ 13.82 & 29.68 \end{bmatrix}. \tag{4.6}$$

Relative gain array (RGA) analysis of the transformation matrices is conducted to study the thermal coupling effects for both the bake-plate and wafer. RGA is an analytical tool to determine the optimal input-output variable pairings for a multi-input-multi-output (MIMO) system. In other words, RGA is a normalized form of the gain matrix that describes the impact of each control variable on the output, relative to each control variable's impact on other variables. A perfect decoupled system results in an identity RGA matrix. For the proposed thermal system in this chapter, the RGA matrices of the bake-plate and wafer are stated as below:

$$RGA_{bp-to-u} = G_{bp-to-u} \cdot (G^T_{bp-to-u})^{-1} = \begin{bmatrix} 1.30 & -0.30 \\ -0.30 & 1.30 \end{bmatrix}, \tag{4.7}$$

$$RGA_{wfr-to-u} = G_{wfr-to-u} \cdot (G^T_{wfr-to-u})^{-1} = \begin{bmatrix} 2.98 & -1.98 \\ -1.98 & 2.98 \end{bmatrix}. \tag{4.8}$$

The values at the diagonal of $RGA_{bp-to-u}$ are close to 1, which indicates a weak thermal interaction between each zone of the bake-plate. However, the values in $RGA_{wfr-to-u}$ indicate a severe coupling effect for the silicon wafer. A decoupling matrix is needed to decouple the thermal interaction

between wafer center and edge zones. The new transfer function matrix, $G_{new,wfr-to-u}$, should be a diagonal matrix that keeps the diagonal elements of $G_{wfr-to-u}$. The decoupling matrix, D_c, should satisfy that

$$G_{new,wfr-to-u} = G_{wfr-to-u} \cdot D_c = \begin{bmatrix} 18.64 & 0 \\ 0 & 29.68 \end{bmatrix}. \tag{4.9}$$

By solving the equation, the decoupling matrix is obtained as

$$D_c = \begin{bmatrix} 2.98 & -4.25 \\ -1.39 & 2.98 \end{bmatrix}. \tag{4.10}$$

Performing the RGA analysis for the matrix $G_{new,wfr-to-u}$, there is

$$RGA_{new,wfr-to-u} = G_{new,wfr-to-u} \cdot (G^T_{new,wfr-to-u})^{-1} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}, \tag{4.11}$$

which indicates a good thermal decoupling effect with the use of decoupling matrix D_c.

4.3.2 Experimental results and discussion

The objective of this subsection is to experimentally verify the across wafer CD uniformity improvement which has been achieved by the real-time control method. Both conventional baking and real-time control method are performed. The resulting across wafer CD nonuniformities are compared with each other. For conventional baking, the setup of the bake-plate is presented in Chapter 3. The wafer is baked at 130 °C for 125 sec, where the bake-plate temperature set point 130 °C is recommended from the UV3 photoresist user manual. Two PI controllers are used to maintain the bake-plate temperature at 130 °C throughout the entire PEB process. As the

standard PI controller is implemented in LabVIEW, the dynamic equation for PI controller is

$$u[k] = u[k-1] + (K_p + K_i \cdot T_s) \cdot e[k] - K_p \cdot e[k-1], \tag{4.12}$$

where $u[k]$ is the current power input, $u[k-1]$ is the previous power input, K_p is the proportional gain, K_i is the integral gain, T_s is the sampling time, $e[k]$ is the current difference between the bake-plate temperature measurement and set point, and $e[k-1]$ is the previous difference between the bake-plate temperature measurement and set point. Ziegler-Nichols Reaction Curve Tuning Method is used for the PI controller parameters tuning. In the experiment, the sampling time is set to 0.1 sec based on the sampling theory [37]. The open loop step responses of the bake-plate are shown in Figure 4.10. From Ziegler-Nichols Reaction Curve Tuning Method, we obtain $K_p = 0.8189$, $K_i = 0.0586$ for the center zone PI controller, and $K_p = 0.5587$, $K_i = 0.0224$ for the edge zone PI controller. After several iterations of tuning, we finally use $K_p = 1.00$, $K_i = 0.05$ for the center zone PI controller, and $K_p = 0.50$, $K_i = 0.02$ for the edge zone PI controller in the experiment.

For the real-time control method, the reference is first built. Section 4.2 states that each CD profile corresponds to a specific cosine signature. In the experiment, a 500 nm CD latent image with 420 nm thickness is adopted as the reference. The cosine signatures of the reference are measured at 25 sec, 65 sec and 125 sec during the PEB process, which are plotted in Figure 4.7. Next, the CD latent image profiles, one at the center of wafer and the other one 4 cm apart from it, are in-situ measured by the spectroscopic

ellipsometer throughout the PEB process. Based on the difference between measurement and reference, the power inputs to the bake-plate center and edge are real-time adjusted, respectively.

Two sets of experiments are conducted to compared the real-time control method with the conventional baking, for wafers with different incoming conditions. In Experiment 1, twenty 4-inch silicon wafers are processed step by step as below:

1. The wafers are coated with Shipley UV3 positive photoresist at 6000 rpm for 55 sec.

2. The wafers are sent for soft bake at 120 °C for 90 sec.

3. The wafers are exposed for 2.6 sec at 6.1 mJ/cm^2.

After that, ten wafers go through the conventional baking while the other ten wafers go through the real-time control. The experimental results are shown in Figures 4.11 to 4.18. Figures 4.11, 4.12 and 4.13 show the experimental results of conventional baking. Large difference between the measured signature and reference is observed at the end of PEB process, especially for the measurement at the wafer edge. In Figure 4.13, the MSE between the center average and reference, and the MSE between the edge average and reference, sums up to 0.1521. The SEM verification is shown in Figure 4.14. It presents that the CD valley linewidth at the wafer center is 503 nm and the CD valley linewidth at the wafer edge is 550 nm. A total across wafer CD nonuniformity of 50.1 nm is obtained by measuring the total MSE to reference.

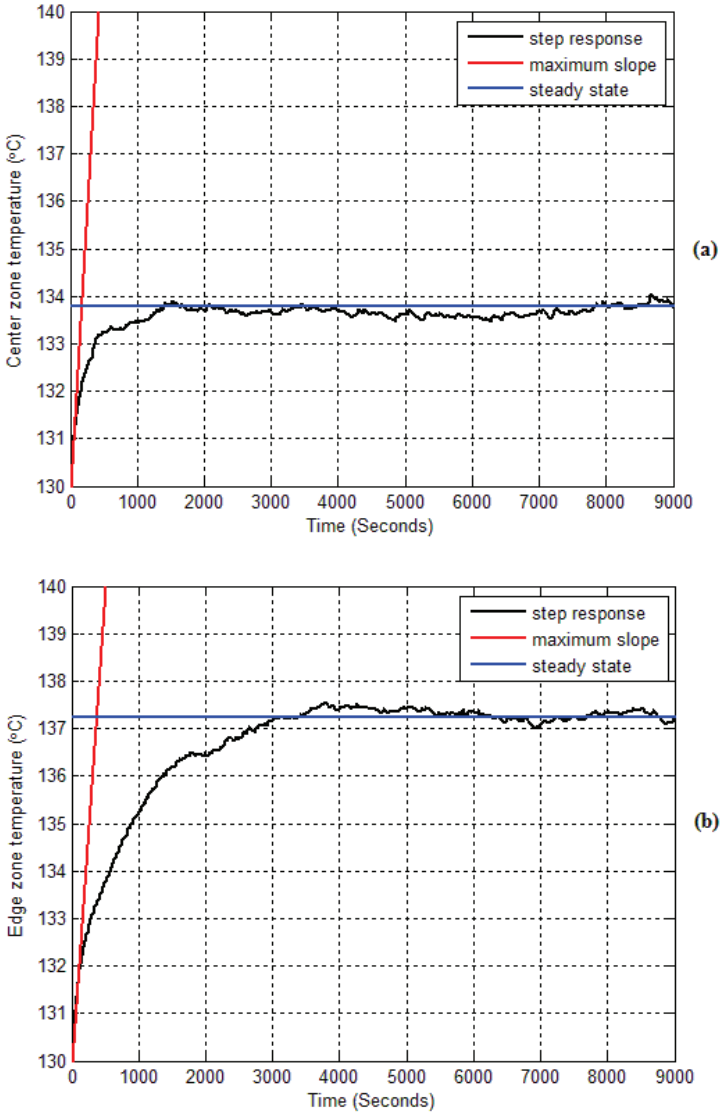

Figure 4.10: Open loop step responses for the 4-inch bake-plate. The bake-plate center and edge temperatures during the baking process are shown in subplots (a) and (b), respectively.

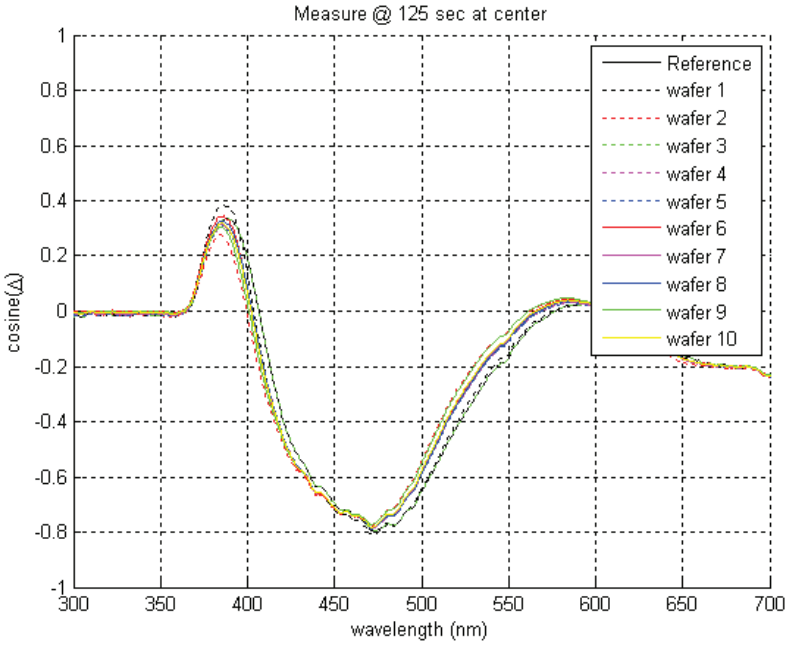

Figure 4.11: The cosine signatures of conventional baking for PEB at 130 °C for 125 sec at the wafer center

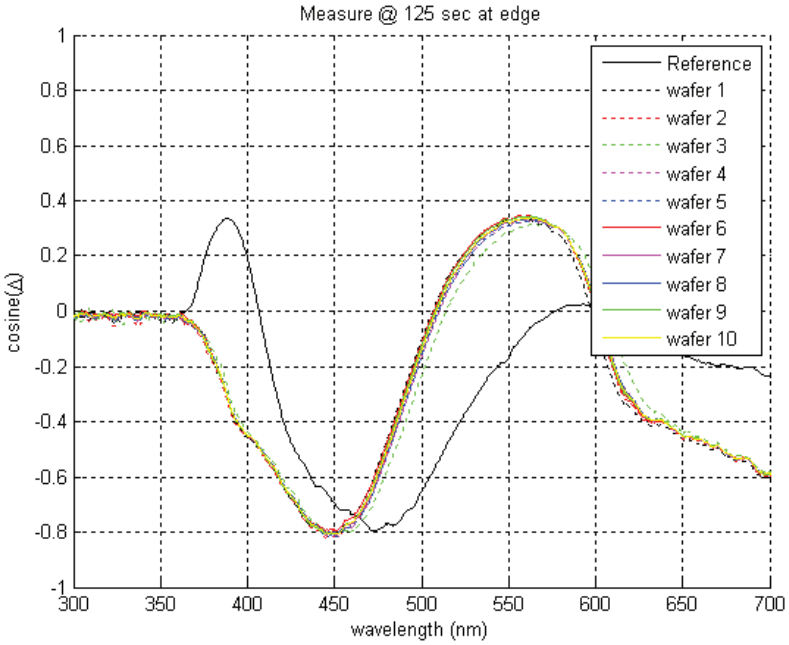

Figure 4.12: The cosine signatures of conventional baking for PEB at 130 °C for 125 sec at the wafer edge

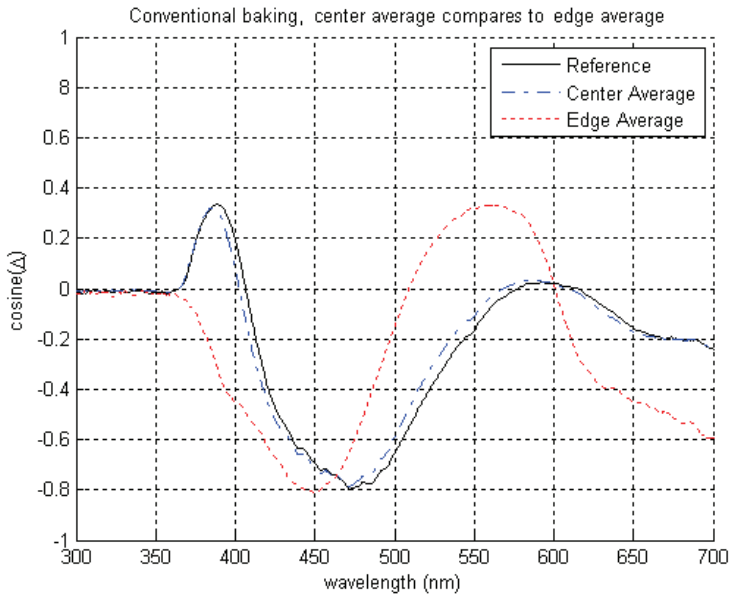

Figure 4.13: Averaged cosine signatures of conventional baking for PEB at 130 °C for 125 sec

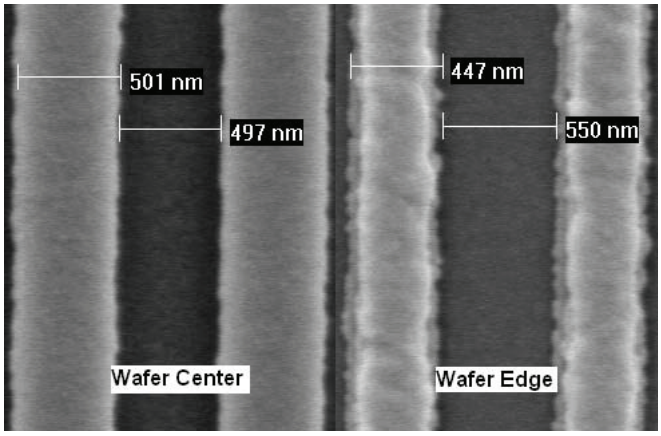

Figure 4.14: SEM results for the conventional baking at 130 °C for 125 sec

The real-time control results of the other ten wafers are shown in Figures 4.15 to 4.18. It is observed that the measured signatures at both the center and edge zones are quite close to the reference signature. In Figure 4.17, the total MSE between measurements and reference is reduced to 0.1040 compared with 0.1521 in the conventional baking, presenting a 31.6% decrease in the signature nonuniformity. Figure 4.18 shows the SEM result. It can be seen that the CD valley linewidth at the wafer center is 494 nm and the CD valley linewidth at the wafer edge is 515 nm. A total across wafer CD nonuniformity of 16.2 nm is obtained. Compared with the 50.1 nm across wafer CD nonuniformity resulted from the conventional baking, it is important to note that a 68% nonuniformity reduction is achieved by the proposed real-time control method.

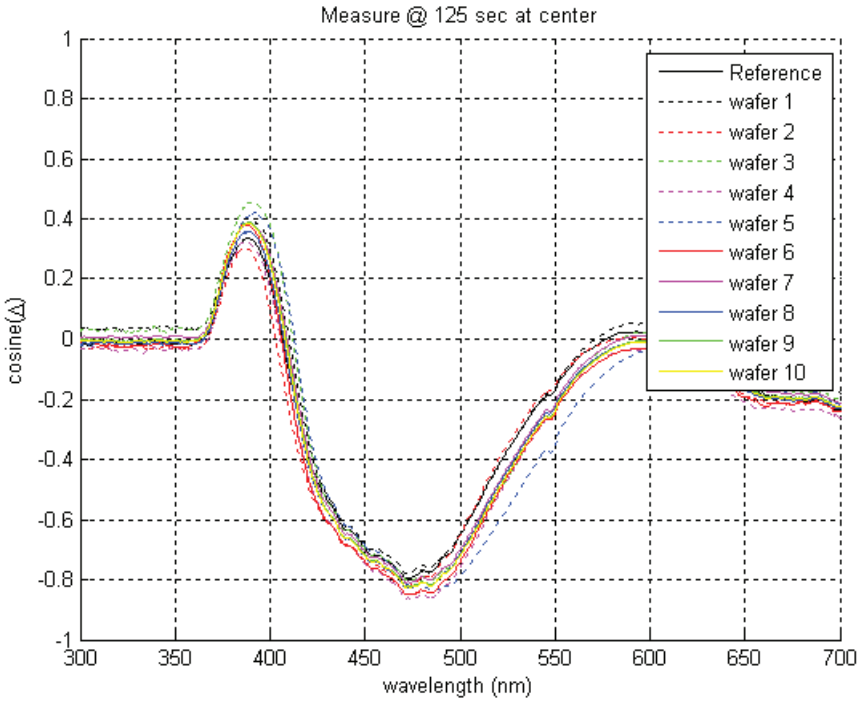

Figure 4.15: Cosine signatures for in-situ real-time control through the PEB process at the wafer center

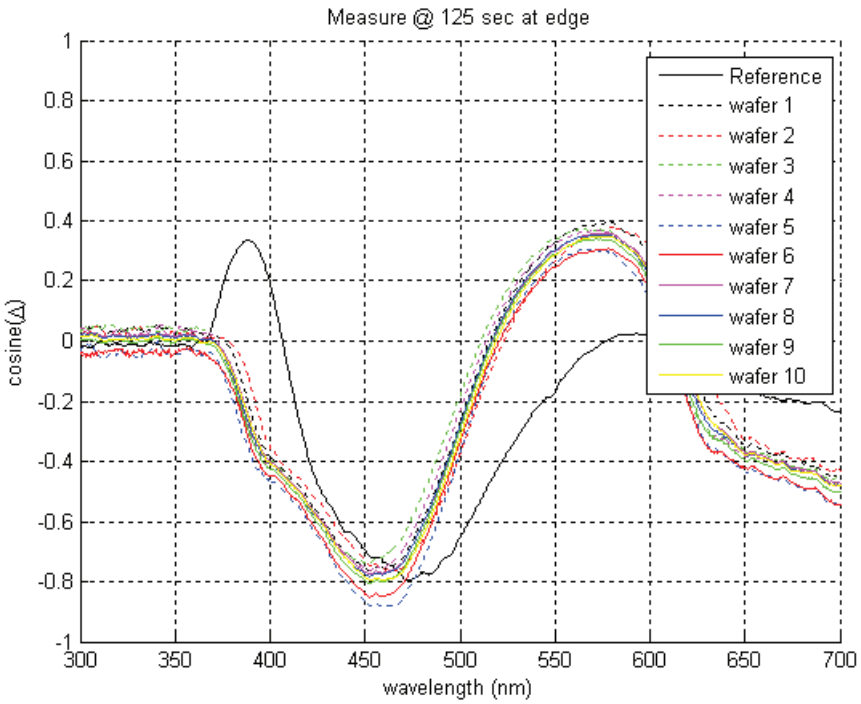

Figure 4.16: Cosine signatures for in-situ real-time control through the PEB process at the wafer edge

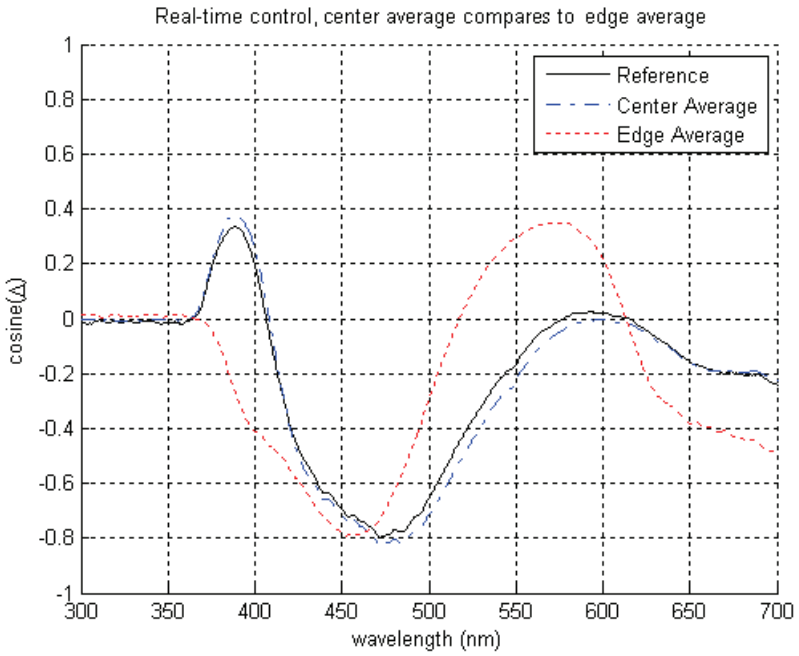

Figure 4.17: Averaged cosine signatures for in-situ real-time control through the PEB process

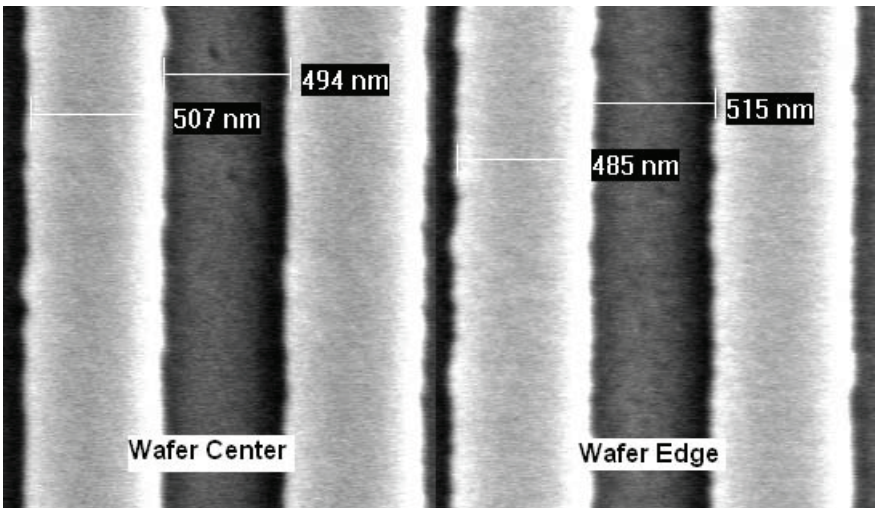

Figure 4.18: SEM results of the real-time temperature control through the PEB process

Next, Experiment 2 is conducted to further check the capability of the real-time control method for various kinds of pre-baking conditions. In Experiment 2, another ten wafers are processed with the same recipe as in Experiment 1 prior to the PEB step, but they are coated at 5500 rpm instead of 6000 rpm, resulting 4%-5% increase of photoresist thickness. After that, five wafers go through the conventional baking while the rest five wafers go through the real-time control. The experimental results are shown in Figures 4.19 to 4.26. Figures 4.19, 4.20, and 4.21 show the conventional baking results. The MSE between the center average and reference, and the MSE between the edge average and reference, sums up to 0.1208, which is subject to both the photoresist thickness and the CD linewidth. The SEM verification is shown in Figure 4.22, and a 43.6 nm across wafer CD nonuniformity is presented. Whereas, the real-time control results of the other five wafers are shown in Figures 4.23 to 4.26. It is observed that the total MSE is reduced to 0.0790, presenting a 34.6% decrease in the signature nonuniformity, while the across wafer CD nonuniformity is reduced to 15.6 nm, presenting a 64% reduction of across wafer CD nonuniformity compared with the conventional baking.

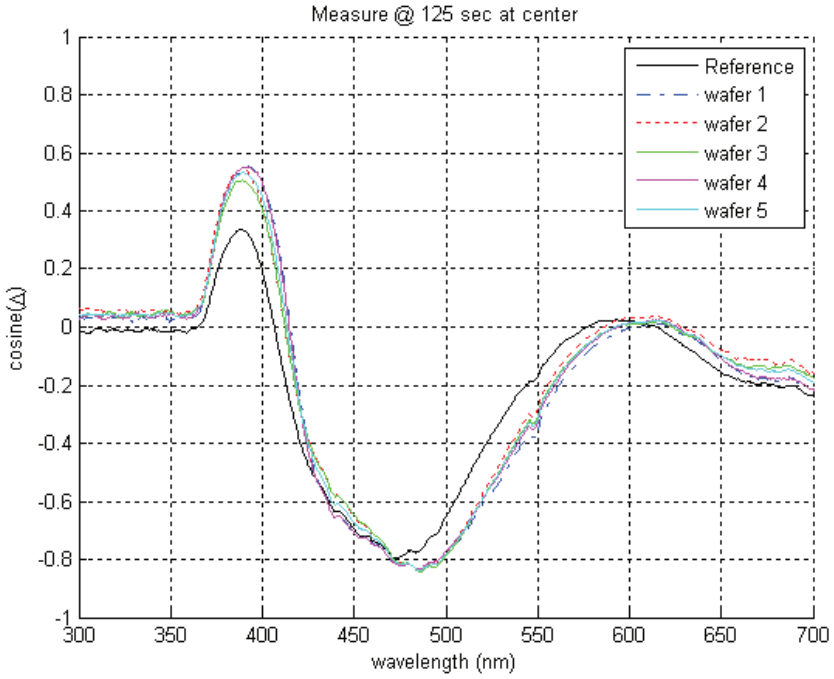

Figure 4.19: Cosine signatures of conventional baking for PEB at 130 °C for 125 sec with spin coating at 5500 rpm at the wafer center

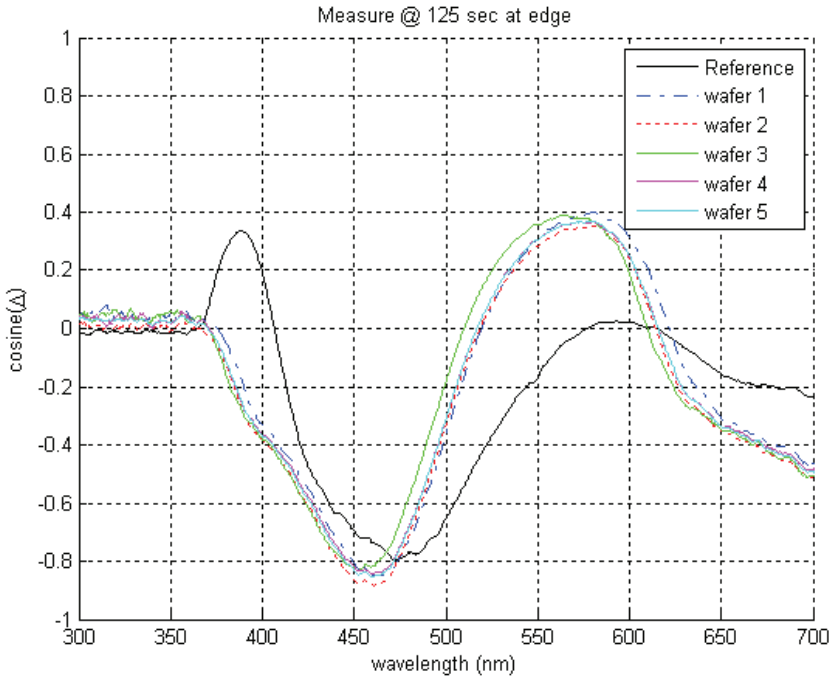

Figure 4.20: Cosine signatures of conventional baking for PEB at 130 °C for 125 sec with spin coating at 5500 rpm at the wafer edge

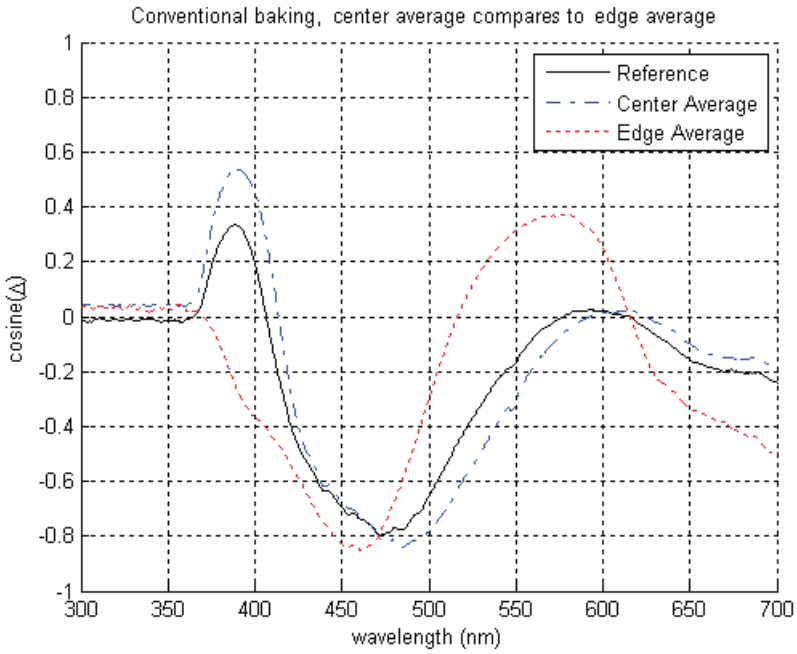

Figure 4.21: Averaged cosine signatures of conventional baking for PEB at 130 °C for 125 sec with spin coating at 5500 rpm

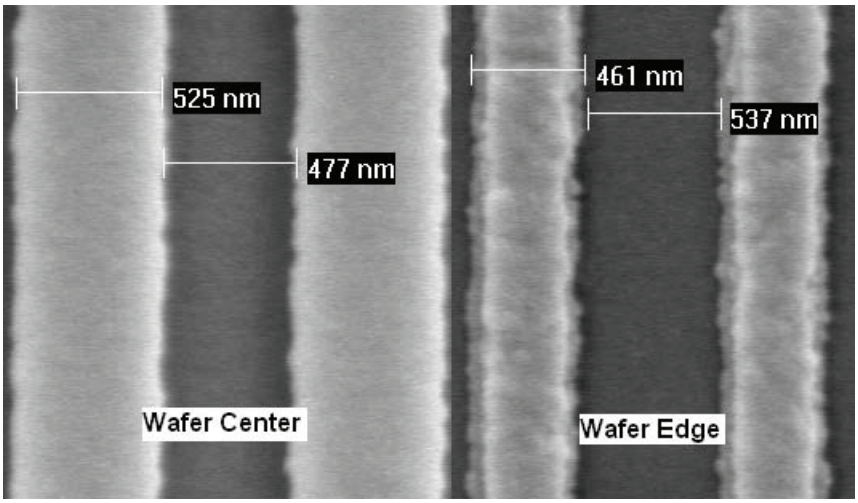

Figure 4.22: SEM results for conventional baking at 130 °C for 125 sec with spin coating at 5500 rpm

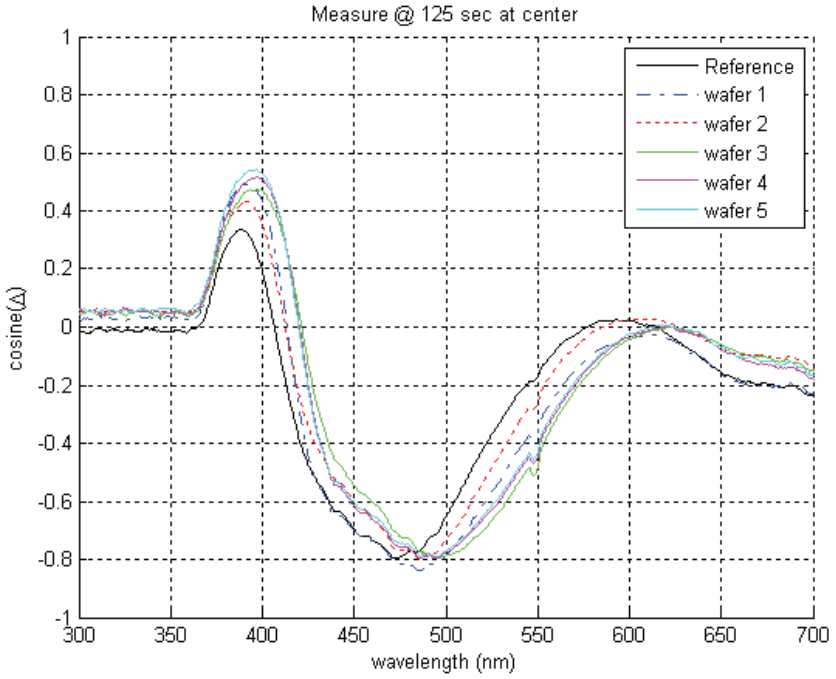

Figure 4.23: Cosine signatures for in-situ real-time control through the PEB process with spin coating at 5500 rpm at the wafer center

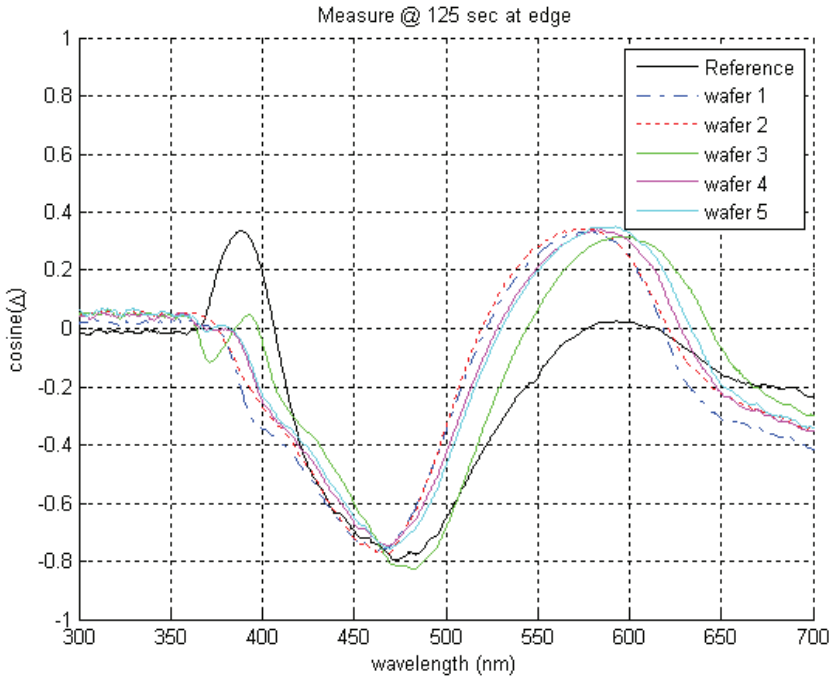

Figure 4.24: Cosine signatures for in-situ real-time control through the PEB process with spin coating at 5500 rpm at the wafer edge

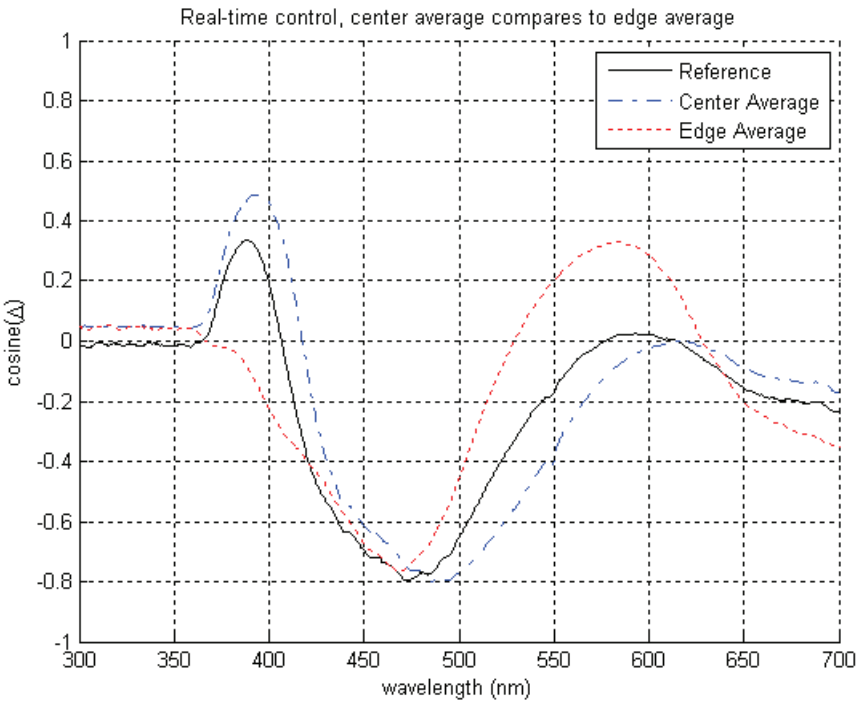

Figure 4.25: Averaged cosine signatures for in-situ real-time control through the PEB process with spin coating at 5500 rpm

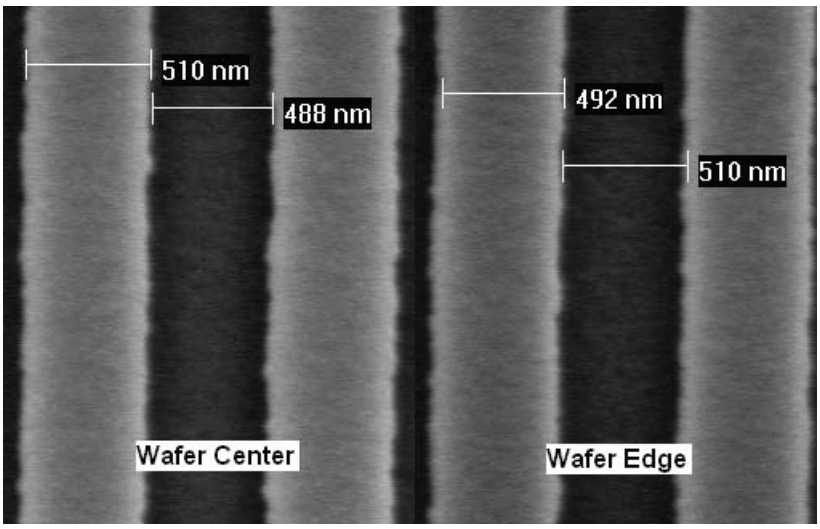

Figure 4.26: SEM results of the real-time temperature control for 125 sec with spin coating at 5500 rpm

4.4 Conclusion

This chapter demonstrated how the dual-zone in-situ real-time CD monitoring and control was performed throughout the PEB process, with the application of a dual-probe spectroscopic ellipsometer and a dual-zone programmable thermal baking system. The CD nonuniformity across the wafer has been reduced by more than 60% by performing a dynamic temperature profile control across the bake-plate and wafer.

Chapter 5

Feedforward/Feedback Control Framework for the Lithography Process

5.1 Introduction

In the current semiconductor manufacturing process, the operator usually performs daily recipe setup and tuning to enhance metrology tool utilization, instead of performing measurement on every outgoing production lot. However, such a R2R control method depends highly on the measurement of sample, and it may not provide the most appropriate parameter settings for each single incoming wafer. The previous chapter presented the in-situ real-time control method of photoresist properties at the PEB step, which can well rectify the variations of photoresist properties from previous steps. However, this method does not perform any tuning on those

steps. Therefore, this chapter aims at proposing a feedforward/feedback control framework throughout the entire lithography process, which performs tuning on both the spin coating and PEB steps based on the in-situ measurements. This framework rectifies the recipe variation at the spin coating step immediately. It also maintains an accurate CD result by employing the real-time control at the PEB step.

Over the last decade, a number of novel approaches for lithography process modelling, characterization and control were established in the existing literature. In [69], Mack built models for each single step through the lithography process, which provided a clear picture of the sequential reactions along the lithography process. The recipe settings of the previous step are extracted by monitoring the process indices in-situ at the subsequent step for which the incoming condition is the output of the previous step. Recently, researchers have done a lot of works to improve the capability of the whole process and reduce waste. Embedding sensors and controllers at every step of the lithography process is a way of immediately rectifying the inline disturbance or perturbation. However, this method increases the cost of equipment configuration and reduces the manufacturing efficiency. Virtual metrology [70], [71] was introduced to enhance the process capability and simplify the measurement. It assumes that the real-time tool state values reflect the actual process conditions and can be used to establish models for the prediction of wafer properties. For example, the thickness of the thin film formed by spin coating can be related to the spin speed and calculated precisely. Another technique to improve the process capability

is the measurement data selection. It relates the data whose measurements are costly to some easily measured data. For example, the thin film thickness can be related to the light reflection detected by ellipsometry [68]. If we are only interested in the thickness difference between several samples rather than the exact value of the thickness, ellipsometry measured signature may be used for comparison directly, instead of the actual thickness of the sample. However, these works focus on a single step only. In this chapter, the different steps along the lithography process are related, which enables the process automation and increases the manufacturing efficiency.

A relationship between the in-situ real-time photoresist properties monitoring result at the PEB step and the spin speed setting at the spin coating step is built in this chapter. Appropriate tuning is performed for the respective steps to reduce or eliminate the identified perturbations. To illustrate this approach in details, a feedforward/feedback framework is built throughout the lithography process which selects spin coating at the beginning and PEB at the end, as two control modules. The spin speed intentionally deviates from the standard recipe to generate some variations in the photoresist thickness, which may have a severe impact on the final CD value. For the feedforward control, the variations in the photoresist thickness are identified by the ellipsometer at the beginning of the PEB process and then compensated by real-time thermal baking. When it comes to the feedback control, the photoresist properties measured at the beginning of the PEB step by ellipsometer are compared with the reference, and the difference is used to estimate the tuning required for the spin speed at the

spin coating step. The new spin speed is adopted before the next wafer comes in.

The rest of Chapter 5 is organized as follows. In Section 5.2, the detailed framework is developed. The experimental results are then presented in Section 5.3. Finally, the conclusion is given in Section 5.4.

5.2 Design of Control Framework

5.2.1 Framework architecture

The lithography sequence has been stated in Chapter 1. In this chapter, spin coating and PEB steps are selected as the control modules in the lithography process. Spin coating is a process in which the solution is spread evenly over a surface using centrifugal force. Normally, it results in a uniform thin film of a specific thickness at the end of the process. PEB is to thermally catalyze the chemical reaction which amplifies the latent bulk image formed at the exposure step.

The architecture of the framework is presented in Figure 5.1. For the feedforward control, the drift of the spin speed at the spin coating step may cause the variation in photoresist thickness. This variation can be identified at the beginning of the PEB step by the ellipsometry in-situ measurement, and it is then compensated by the real-time thermal baking. For the feedback control, the ellipsometry in-situ measurement of the photoresist properties at the PEB step is compared with the reference. The difference is used to estimate the tuning required for the spin speed at the

spin coating step.

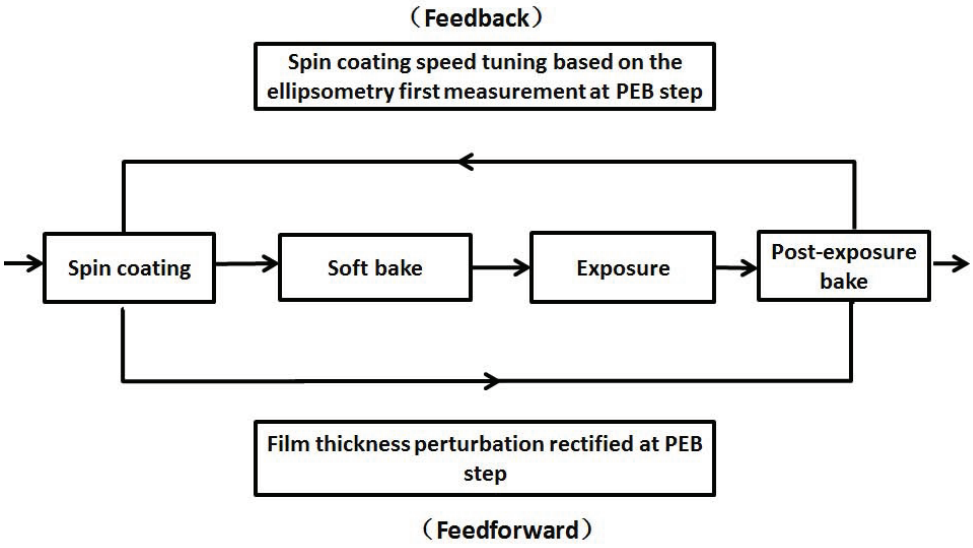

Figure 5.1: Architecture of the framework

5.2.2 Module characterization

It is necessary to characterize the control module before giving the exact control equations. As PEB has been discussed in the previous chapters, this subsection only focuses on the characterization of the spin coating process. Spin coating is widely used in the microelectronics industry. The first spin coating model was developed by Emslie et al. in 1958 [72]. This model was used as the basis for more specific or complicated models developed subsequently. A typical spin coating process consists of a dispense step in which the photoresist resin is deposited onto the wafer substrate surface, a high-speed spin step to thin the fluid, and a drying step to eliminate excess solvents from the resulted film. The basic spin coating model considers the viscosity of solution and centrifugal force only. The coating thickness, h_c,

can be expressed as

$$\frac{\partial h_c}{\partial t} = -\frac{\rho\Omega^2}{3\mu}\frac{1}{r}\frac{\partial}{\partial r}(r^2 h_c^3), \tag{5.1}$$

where t is the time, ρ is the fluid density, Ω is the spin speed of the wafer, μ is the fluid viscosity, and r is the fluid thin film radius, respectively. The thin film thickness can be solved as

$$h_c(t) = \frac{h_0}{(1 + t/\tau)^{1/2}}, \tag{5.2}$$

where h_0 is the initial thickness of fluid and $\tau = 3\mu/4\rho\Omega^2 h_0^2$. However, this simple model does not consider the factor of evaporation. In [73] - [76], evaporation was incorporated by assuming that the solvent evaporated uniformly over the entire surface area. The concentration of solid species in photoresist increased because of the evaporation. If there is a constant evaporation rate, the final coating thickness of the thin film can be stated as

$$H = c_0[\frac{3\mu}{2(1 - c_0)\rho^2\Omega^2} \cdot \frac{P_v M}{RT} \cdot k_m x_0]^{1/3}, \tag{5.3}$$

where H is the final coating thickness, c_0 is the initial concentration of solid species in the photoresist, P_v is the vapor pressure of the pure solvent, M is the molecular weight of the solvent, R is the ideal gas constant, T is the temperature, k_m is the mass transfer coefficient, and x_0 is the mole fraction of the solvent. However, the deep UV photoresist used in the experiment is actually a kind of slowly evaporating material whose evaporation rate varies with the square root of the spin speed. For such a kind of spin coating process, Lawrence [77] related the final thickness of thin film to the

spin speed as

$$H = C_0 \delta^{\frac{1}{2}} (\mu_0 D_0)^{\frac{1}{4}} \Omega^{-\frac{1}{2}}, \tag{5.4}$$

where C_0 is the concentration of solute at the free surface of thin film, δ is the factor constant normally taken as unity, μ_0 is the initial kinematic viscosity, D_0 is the initial diffusion coefficient, and Ω is the spin speed. In another way, we can state that the final thin film thickness H is inversely proportional to the square root of spin speed Ω for the deep UV photoresist coating,

$$H \propto \Omega^{-\frac{1}{2}}. \tag{5.5}$$

Experiments are conducted to identify the relationship between the thin film thickness and the spin speed. A Cee Model 100 spin coater from Brewer Science is used for the experiments. 2 ml of Shipley UV3 photoresist is dropped onto the wafer surface, and the wafers are spun for 55 sec with different spin speeds. Soft bake is then performed at 120 °C for 90 sec to evaporate the residual solution. The thin film thicknesses at different spin speeds are measured by reflectometer [11], and the results are shown in Table 5.1, which satisfy the Equation 5.5.

Table 5.1: Thin film thicknesses with different spin speeds

Spin speed	Thin film thickness
5000 rpm	475 nm
5500 rpm	455 nm
6000 rpm	435 nm

5.2.3 Control algorithm

The CD latent image profile is in-situ measured by the spectroscopic ellipsometer at the PEB step. From the first measurement of ellipsometer at the beginning of the PEB process, the initial CD latent image profile together with the film thickness can be extracted. The measurement is compared with the reference. Based on the difference, the feedforward/feedback control is performed accordingly. However, it is costly to extract the CD latent image profile with film thickness for every measurement. There remains a need to perform process tuning directly based on the ellipsometry in-situ measured signature. For the feedforward control, the first in-situ measured signature of ellipsometry at the PEB step is compared with the preset reference. The variation in film thickness results in the variation in measured signature. Based on the difference between the measured signature and reference, the power input to the bake-plate is adjusted accordingly in real-time. The variation in film thickness can be compensated appropriately. The details of the real-time control method have already been discussed in Chapter 4. The same bake-plate and thermal control method are adopted in Chapter 5. When it comes to the feedback control, the relationship between the ellipsometry in-situ measured signature and the spin speed at the spin coating step is further explored in this subsection. To identify this relationship, the RCWA model built in Chapter 4 is recalled. A CD latent image profile of 1000 nm periodic grating line with 1:1 duty cycle ratio is chosen. Varying its thickness from 425 nm to 445 nm at a step size of 5 nm, the respective signatures are plotted in Figure 5.2.

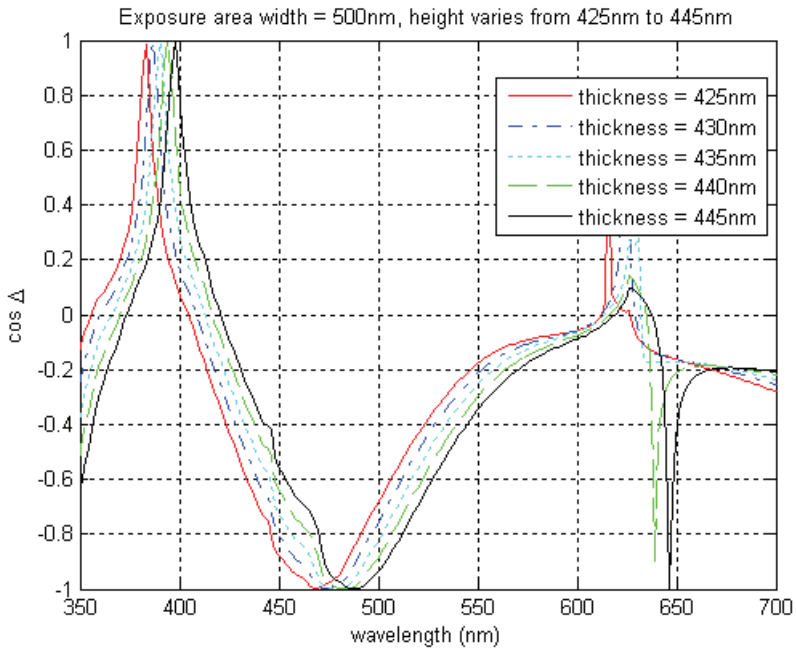

Figure 5.2: Signature variations with respect to the photoresist thicknesses

In Figure 5.2, it shows that the ellipsometry measured signature moves to the right as the photoresist thickness increases within the range of 425 nm to 445 nm. The positions of the signature bottom with respect to the different photoresist thicknesses are stated in Table 5.2. Empirically, it is observed that a position shift of approximately 5.3 nm takes place for every 5 nm variation in the film thickness. This statistic is used as a guideline for the spin coater speed tuning. For each measured signature, its bottom position is first identified and then compared with the reference. If the bottom position of measured signature is X nm on the right of the reference bottom, the spin speed should be increased to reduce the film thickness by $X/5.3 \times 5$ nm, while if the bottom position of measured signature is X nm on the left of the reference bottom, the spin speed should be decreased to increase the film thickness by $X/5.3 \times 5$ nm. For film thicknesses between 400 nm and 500 nm, a 500 rpm change in spin speed may result in a

thickness variation of approximately 20 nm, according to Table 5.1.

Table 5.2: Bottom positions of signatures with respect to the different film thicknesses

Film thickness	Horizontal position of signature bottom
425 nm	467.6 nm
430 nm	472.9 nm
435 nm	478.2 nm
440 nm	483.5 nm
445 nm	488.8 nm

5.3 Experimental Results and Discussions

A standard 500 nm CD linewidth with 420 nm thickness is generated by the following recipe:

1. The 4-inch silicon wafer is coated with Shipley UV3 positive photoresist at 6000 rpm for 55 sec.

2. The wafer is sent for soft bake at 120 °C for 90 sec.

3. The wafer is exposed for 2.6 sec at 6.1 mJ/cm^2 through a 1000 nm square grating mask with 1:1 duty cycle ratio.

4. The PEB is conducted for the wafer at 130 °C for 125 sec.

5. The wafer is immersed in the MF CD-26 developer solution for 10 sec, followed by rinsing with DI water.

A CD profile with 500 nm linewidth of valley and 420 nm height is revealed at the wafer center after the development process is completed. There is much uncertainty in the practical manufacturing process, which is another reason for applying the control framework. In the experiment, the perturbations are intentionally created by decreasing the spin speed from

6000 rpm to 5800 rpm. At the PEB step, the variation of film thickness caused by the spin speed offset can be successfully detected and corrected by employing the real-time control method stated in Chapter 4. Ten wafers are used in the experiments to verify the claim. They are processed with the recommended recipe until the PEB step, but they are coated at 5800 rpm instead of 6000 rpm, resulting in an approximately 2% increase in the photoresist thickness. Thereafter, five wafers go through the conventional baking while the other five wafers go through the real-time control. Their experimental results are shown in Figures 5.3 to 5.6. Figure 5.4 shows the average conventional baking result with the total MSE to reference up to 0.1665, which is subject to both the photoresist thickness and the CD linewidth variations. The results of real-time control method for the other five wafers are shown in Figures 5.5 and 5.6. It is observed that the total MSE is reduced to 0.0028, eliminating the signature difference.

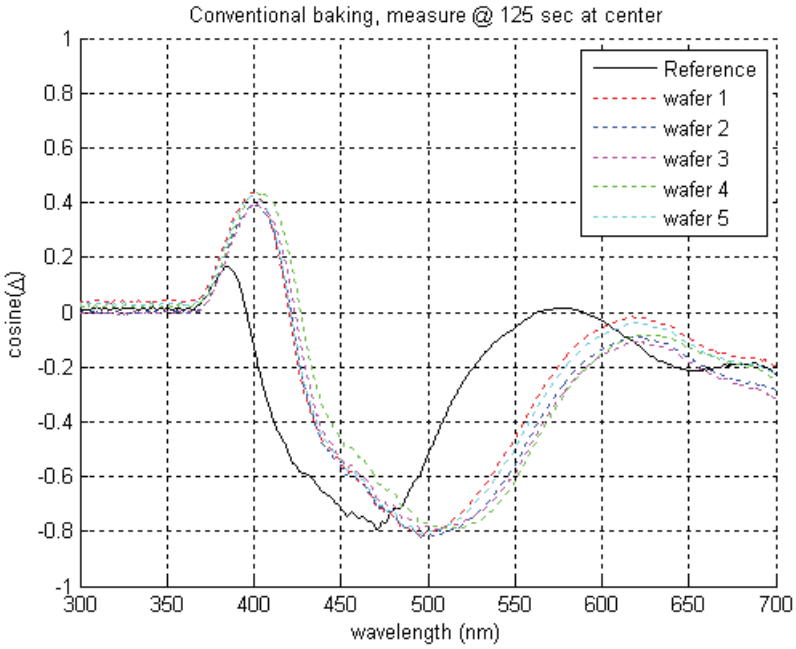

Figure 5.3: Cosine signature comparison for PEB at 130 °C for 125 sec with spin coating at 5800 rpm

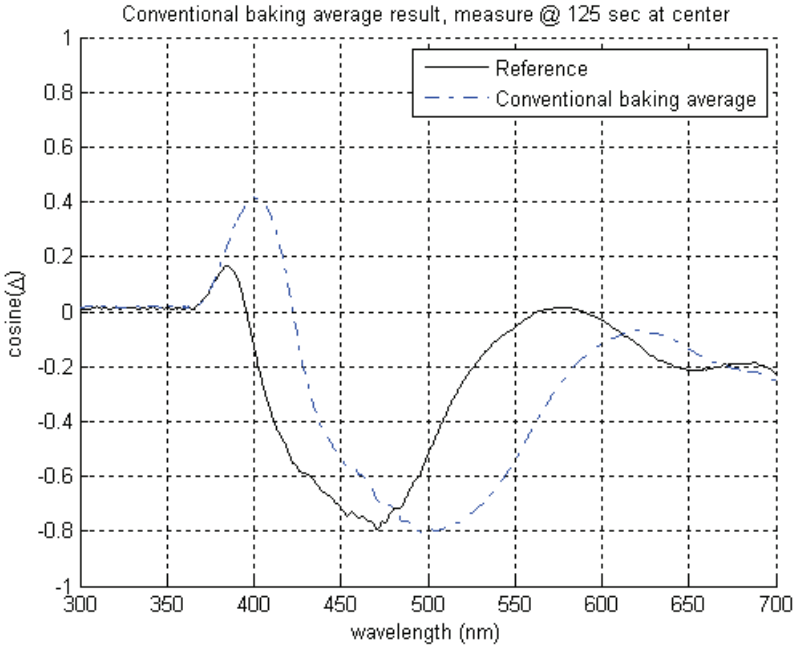

Figure 5.4: Average cosine signature comparison for PEB at 130 °C for 125 sec with spin coating at 5800 rpm

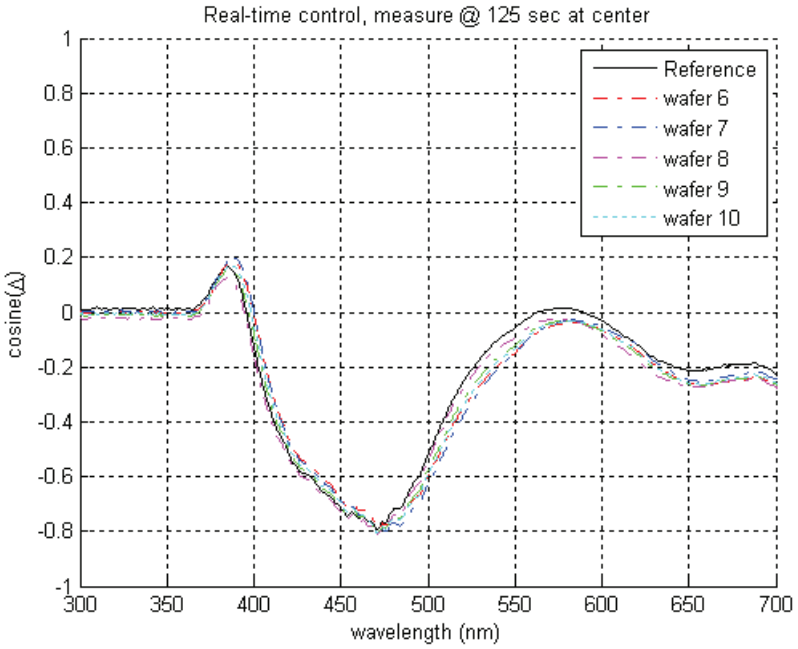

Figure 5.5: Cosine signature comparison for in-situ real-time control through the PEB process with spin coating at 5800 rpm

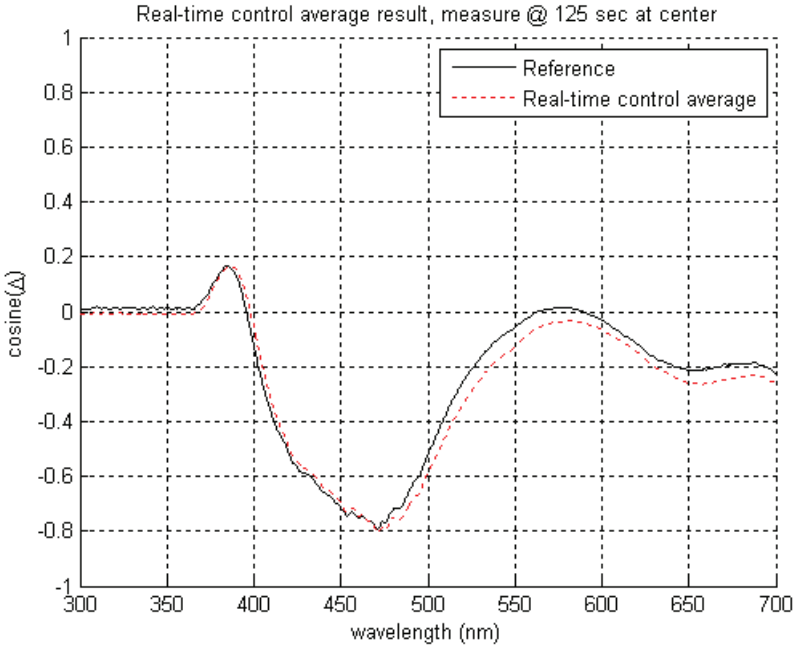

Figure 5.6: Average cosine signature comparison for in-situ real-time control through the PEB process with spin coating at 5800 rpm

Besides performing the ellipsometry assisted real-time control at the PEB step, the first in-situ measurement of ellipsometry at the beginning of the PEB process is used to calculate the necessary tuning for the spin coating step. For the five wafers that go through the real-time control at the PEB step, their first in-situ measured signatures are shown in Figure 5.7, together with the respective reference. The tuning action is derived, and is given in Table 5.3. Taking the average result, the spin speed needs to be increased by +191 rpm to reach 5991 rpm, which is close to that of the standard recipe. This adjustment should be made before the next batch of wafers come in.

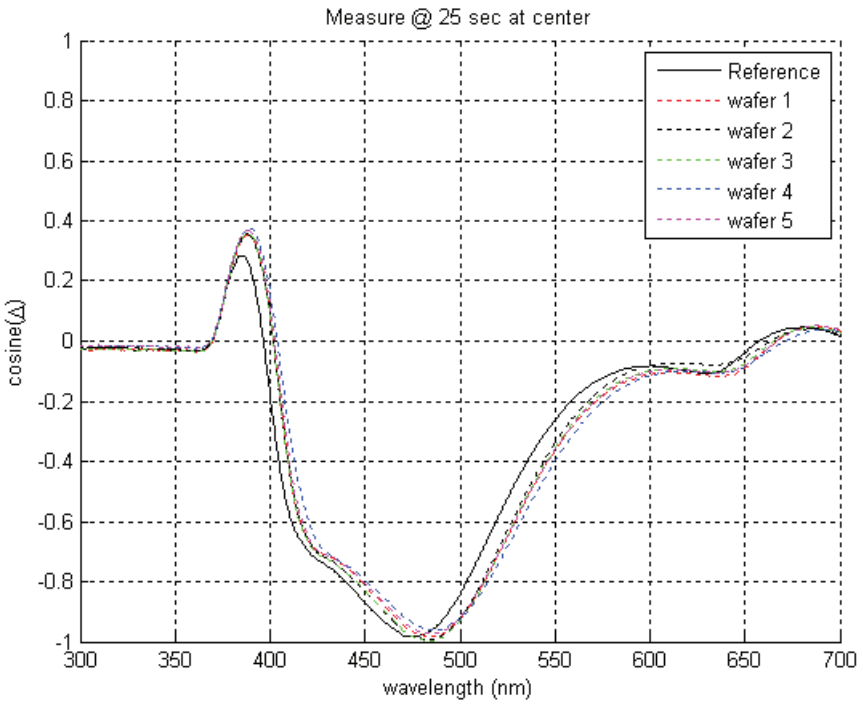

Figure 5.7: Comparison of signatures between the in-situ measurements and reference at 25 sec of PEB step

Table 5.3: Tuning performed at the spin coating step

	signature bottom position (p)	reference bottom position (p_r)	distance: $X = p - p_r$	spin speed tuning: $\Delta\Omega = \frac{X}{5.3} \cdot \frac{5}{20} \cdot 500$
wafer 1	482.8 nm	476.1 nm	6.7 nm	+158 rpm
wafer 2	484.2 nm	476.1 nm	8.1 nm	+191 rpm
wafer 3	482.8 nm	476.1 nm	6.7 nm	+158 rpm
wafer 4	487.0 nm	476.1 nm	10.9 nm	+257 rpm
wafer 5	484.2 nm	476.1 nm	8.1 nm	+191 rpm
Average	484.2 nm	476.1 nm	8.1 nm	+191 rpm

5.4 Conclusion

In this chapter, a feedforward/feedback control framework through the lithography process has been presented. Spin coating and PEB are selected as the beginning and end control modules for the framework. The perturbation caused by the offset at the spin coating step can be detected and corrected at the PEB step by employing the in-situ spectroscopic ellipsometer and thermal bake-plate for the real-time control. Moreover, based on the first in-situ measurement of ellipsometry at the beginning of the PEB step, the appropriate tuning for the spin coating step can be derived and should be performed before the next batch of wafers come in. By implementing such a feedforward/feedback control framework, the lithography system can conduct self-tuning to optimize its parameter settings at each step throughout the whole process, and enhance the performance of the system. This chapter only covers two steps: spin coating step and PEB step. For future research and development, this methodology can actually be applied to every single step throughout the lithography process if an accurate model is built to relate all the steps. If such conditions are achieved, the

whole lithography process will be operated by a highly intelligent system which can greatly reduce human errors and enhance production efficiency.

Chapter 6

Conclusion

6.1 Summary

The lithography process will continue to be a critical area in semiconductor manufacturing due to its impacts on the performance of microelectronics. Enabling advancements by computational, control, and signal processing methods are necessary for the purpose of effectively reducing the enormous costs and complexities associated with the lithography sequence. The contributions of the thesis mainly laid on the following two aspects. Firstly, a dual-zone programmable thermal baking system has been developed for across wafer temperature control. This work can be easily implemented in the industrial applications because the commercial multi-zone bake-plates have already been available in the market. Secondly, an in-situ real-time across wafer CD control method has been presented. The actuator, sensor and control scheme of the system have been discussed, respectively. It concludes that the CD uniformity can be greatly improved by employing

the proposed in-situ real-time control method throughout the lithography process. The proposed control method integrated the spectroscopic ellipsometer as the in-situ sensor with the bake-plate. However, some baking processes in semiconductor manufacturing are conducted in a sealed chamber, which poses challenges to the installation of the in-situ sensor. An interesting research topic is to design the chamber which can naturally integrate the spectroscopic ellipsometer.

In Chapter 2, an in-situ approach has been proposed for the real-time estimation and control of both the transient and steady states wafer temperatures during the baking steps in the lithography process. A detailed physical model has been built, which stated the relationship between the wafer temperatures, bake-plate temperatures and heat power inputs. The wafer temperatures were estimated from the real-time measured power inputs and bake-plate temperatures. With the proposed approach, the wafer temperature uniformity during the thermal process has been improved by more than 75%. The proposed approach can also be scaled up for larger wafers by increasing the numbers of sensors, actuators, and controllers.

Chapter 3 has discussed the feasibility of implementing the spectroscopic ellipsometer to the in-situ monitoring of photoresist properties at the PEB step. The PEB process has also been characterized by the ADL theory to explain the variations of ellipsometry measurements. Experiments have been conducted, which demonstrated the thermal heating impact on the measured signature of spectroscopic ellipsometry. Compared with the traditional SEM and AFM techniques in the semiconductor indus-

try, ellipsometer has been identified as an ideal metrology tool for in-situ measurement because of its fast, accurate, and non-destructive characteristics.

In Chapter 4, an in-situ real-time across wafer CD monitoring and control system has been developed. It consisted of a dual-zone programmable thermal bake-plate as the real-time actuator and a dual-probe spectroscopic ellipsometer as the in-situ metrology sensor. A periodic optical diffraction model based on the RCWA has been built to relate the ellipsometry measured signature to the CD latent image profile. Experiments have been conducted to compare the real-time control system with the conventional baking. It showed that the real-time control system achieved more than 60% improvement in the across wafer CD uniformity for various kinds of incoming conditions.

Chapter 5 has proposed a feedforward/feedback control framework for the lithography process. The spin coating and PEB steps were selected as the control modules in the lithography process. The perturbation caused at the spin coating step was identified at the beginning of the PEB step and corrected by the real-time thermal control through the PEB step. The framework also passed the perturbation measured at the PEB step to the spin coating step, and the spin speed was adjusted appropriately to compensate the perturbation. With the proposed framework, the process perturbation prior to the PEB step has been effectively eliminated while the across wafer CD uniformity has been greatly improved. The manufacturing production line can also be automated to increase the work efficiency and

reduce the human errors.

6.2 Future Works

This thesis provides a promising approach to the real-time monitoring and control of across wafer CD. It has significantly improved the across wafer CD uniformity and demonstrated great robustness to the process perturbation. Based on the current works, research efforts can be put into the following areas in the future.

In the thesis, the ellipsometry technique together with the RCWA has been used to perform the in-situ measurement of CD latent image profile on the periodic grating pattern. The one-layer model has been used to simulate the CD profile. It performs a good approximation to the ten-layer model. However, the actual CD profile may be very complex and requires much more layers to simulate, which is at the cost of calculation. It also takes a longer time to search the matched reference in the library. An optimized approach to model building and search engine design is needed so that the accuracy and calculation cost can be balanced appropriately. Moreover, classical RCWA modelling only works for the two-dimensional periodic grating pattern assuming infinite line length, which is suitable for some metal line structure measurements. However, it is insufficient to handle the more complicated circuit designs. For this issue, more complex mathematical models, e.g., three-dimensional profile analysis model, are expected to be developed in the future. Azimuth angle can be the key to en-

able the spectroscopic ellipsometry measurement for the three-dimensional periodic CD profile analysis. A set of ellipsometry measurements are obtained when the azimuth angle gradually varies and the light incident angle remains the same. Further analysis of the three-dimensional CD profile can be conducted on the obtained ellipsometry measurements.

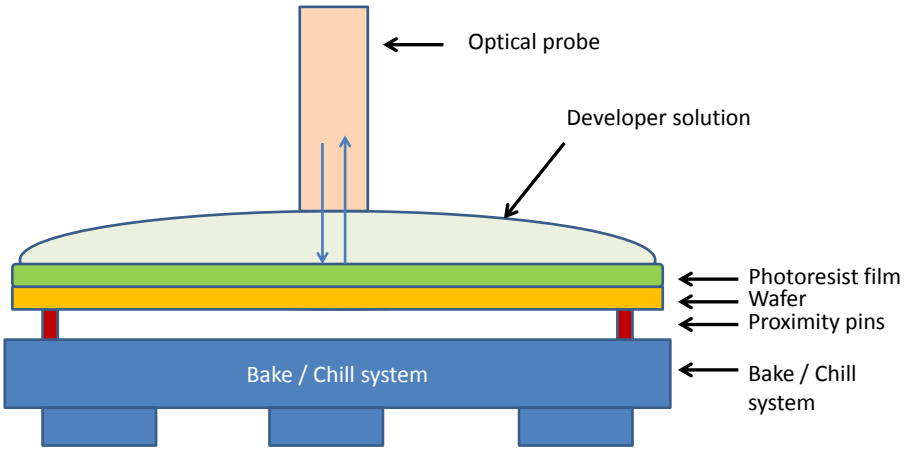

Figure 6.1: Schematic diagram of the bake / chill system and the spectrometry probe

The other interesting research direction is to apply the real-time control method to other steps throughout the lithography process. For example, development step makes more direct impacts on the final CD result rather than the PEB step as the CD profile is revealed only after the completion of development process. In lithography, there are two basic approaches to photoresist development process: the puddle spray method and the immersion method. For the puddle spray method, developer solution is sprayed

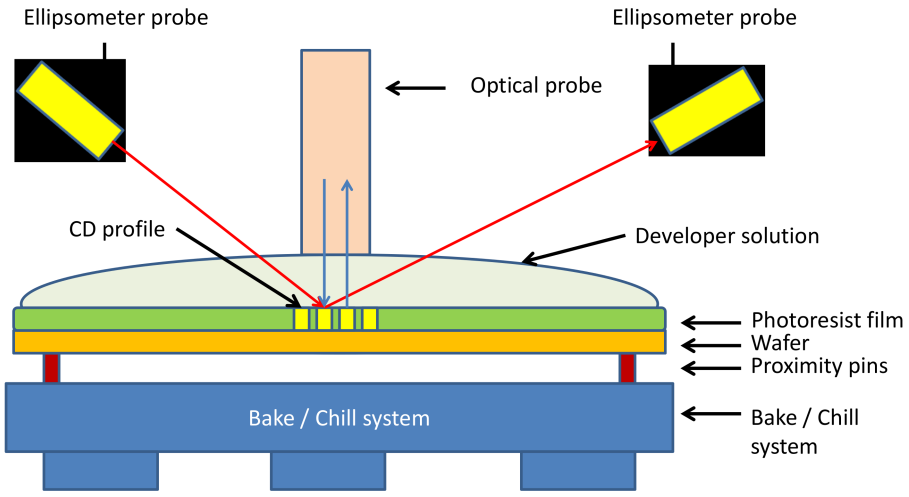

Figure 6.2: Schematic diagram of the bake / chill system, the spectrometry probe and the ellipsometer probes

onto the photoresist film surface so that a puddle of developer solution forms on top of the resist surface. For immersion method, the coated wafer is completely immersed into the developer solution in a container. The solution in the container is reused for subsequent wafers. It is a great challenge to monitor and control the development process in real-time because of the developer solution. The future work aims to build an in-situ real-time CD monitoring and control system for the development process with the puddle spray method. The initial work for real-time monitoring and control of the development process has been performed in [78]. A real-time feedback control system has been developed and applied at the development process for the puddle spray method in [78]. An optical reflectometer was used to in-situ monitor the film thickness, and a bake / chill system was

built to real-time control the temperature of bake-plate and develop rate. The schematic diagram of the system is shown in Figure 6.1. However, the system developed in [78] only works for the unpatterned photoresist film. When the CD pattern is considered, a new novel approach should be proposed. Firstly, a sensor capable of in-situ monitoring of the CD variation at the development step is required. One possible solution is to integrate the reflectometer with the spectroscopic ellipsometer. The schematic diagram is shown in Figure 6.2. Secondly, a comprehensive model is also needed to describe the development process and verify the experimental results. These are expected to be done in the future works.

Bibliography

[1] Moore G. E., "Cramming more components onto integrated circuits", *Electronics*, vol. 38, no. 8, pp. 114 - 117, 1965.

[2] "International Technology Roadmap for Semiconductors." [Online]. Available: http://www.itrs.net [2011]

[3] Plummer J. D., Deal M. D. and Griffin P. B., *Silicon VLSI Technology*, Englewood Cliff, NJ: Prentice-Hall, 2000.

[4] Sturtevant J., "CD control challenges for sub-0.25 μm patterning", *SEMAT- ECH DUV Lithography Workshop*, Austin, TX, Oct. 16 - 18, 1996.

[5] Steele D., Coniglio A., Tang C. and Singh B., "Characterizing Post Exposure Bake Processing for Transient and Steady State Condition, in the Context of Critical Dimension Control", In *Proceedings of the SPIE*, vol. 4689, pp. 517 - 530, 2002.

[6] Lee S., Kim W., Rahman D.M., Kudo T., Timko A., Anyadiegwu C., McKenzie D., Kanda T., Dammel R., Padmanaban M., "PEB Sensitiv-

ity Studies of ArF Resist", In *Proceedings of the SPIE*, vol. 5039, pp. 798 - 806, 2003.

[7] El-Awady K., Schaper C. D., and Kailath T., "Programmable thermal processing module for semiconductor substrates", *IEEE Transaction on Control Systems Technology*, vol. 12, no. 4, pp. 493 - 509, 2004.

[8] Tay A., Ho W. K. and Hu N., "An In Situ Approach to Real-Time Spatial Control of Steady-State Wafer Temperature During Thermal Processing in Microlithography", *IEEE Transaction on Semiconductor Manufacturing*, vol. 20, no. 1, pp. 5 - 12, 2007.

[9] Tay A., Chua H. T., Wang Y., and Yang G., "Control of semiconductor substrate temperature uniformity during photoresist processing in lithography", In *Proceedings of the 7th Asian Control Conference*, pp. 853 - 858, 2009.

[10] Tay A., Ho W. K. and Wu X., "Real-Time Control of Photoresist Extinction Coefficient Uniformity in the Microlithography Process", *IEEE Transaction on Control Systems Technology*, vol. 15, no. 1, pp. 99 - 105, 2007.

[11] Wu X., Yang G., Lim E. X. and Tay A., "In-situ monitoring and control of photoresist parameters during thermal processing in the lithography sequence", In *Proceedings of the SPIE*, vol. 7520, pp. 752035, 2009.

[12] Zhang Q., Poolla K. and Spanos C. J., "One step forward run-to-run critical dimension contro: Across-wafer level critical dimension control through lithography and etch process", *Journal of Process Control*, vol. 18, pp. 937 - 945, 2008.

[13] Tomita T. and Weichert H., "CDU Improvement with Wafer Warpage Control Oven for High Volume Manufacturing", In *Proceedings of the SPIE*, vol. 7273, pp. 72734C, 2009.

[14] Tompkins H. G. and Irene E. A., *Handbook of Ellipsometry*, William Andrew Publishing: Springer, 2005.

[15] [Online] Available: http://www.jawoollam.com/tutorial_1.html [2013]

[16] Balasinski A.P., Karklin L., and Axelrad V., "Impact of Subwavelength CD Tolerance on Device Performance", In *Proceedings of SPIE*, vol. 4692, pp. 361 - 368, 2002.

[17] Tiffany J. and Cohen B., "Reduction of across wafer CDU via constrain ed optimi zation of a multi-channel PEB plate controller based on in-situ measurements of thermal time constants", In *Proceedings of the SPIE*, vol. 5377, pp. 894 - 901, 2004.

[18] Hisai A., Kaneyama K. and Pieczulewski C., "Optimizing CD uniformity by total PEB cycle temperature control on track equipment", In *Proceedings of the SPIE*, vol. 4690, pp. 754 - 760, 2002.

[19] Zhang Q., Tang C., Cain J., Hui A., Hsieh T., Maccrae N., Singh B., Poolla K. and Spanos C. J., "Across-wafer CD uniformity control

through lithography and etch process: experimental verification", In *Proceedings of the SPIE*, vol. 6518, pp. 65182C, 2007.

[20] Ho W. K., Tay A., Fu J., Chen M. and Feng Y., "Critical dimension and real-time temperature control for warped wafers", *Journal of Process Control*, vol. 18, no. 10, pp. 916 - 921, 2008.

[21] Ning G. X., Ackmann P., Richter F., Kurth K., Maelzer S., Hsieh M., Schurack F. and Hong F., "Wafer CD variation for random units of track and polarization", In *Proceedings of SPIE*, vol. 8326, pp. 83261N, 2012.

[22] Narasimhan A. and Karra S., "An inverse heat transfer method to provide near-isothermal surface for disc heaters used in microlithography", *International Journal of Heat and Mass Transfer*, vol. 49, no. 23 - 24, pp. 4624 - 4632, 2006.

[23] Tay A., Chua H. T. and Wu X. D., "A lamp thermoelectricity based integrated bake / chill system for photoresist processing", *International Journal of Heat and Mass Transfer*, vol. 50, no. 3 - 4, pp. 580 - 594, 2007.

[24] Shimoaoki T., Enomoto M., Nafus K., Marumoto H. and Kosugi H., "Evaluation of next generation hardware for lithography processing", In *Proceedings of the SPIE*, vol. 7639, pp. 763922, 2010.

[25] Yan H., Ho W. K., Ling K. V. and Lim K. W., "Multi-Zone Thermal Processing in Semiconductor Manufacturing: Bias Estimation", *IEEE Transaction on Industrial Informatics*, vol. 6, no. 2, pp. 216 - 228, 2010.

[26] Tan K. K., Tay A., Zhao S., Huang S. and Lee T. H., "Predictive ratio control for interacting processes", *Industrial & Engineering Chemistry Research*, vol. 48, pp. 10515 - 10521, 2009.

[27] Ling K. V., Ho W. K., Wu B. F., Loh A. P. and Yan H., "Multiplex MPC for multizone thermal processing in semiconductor manufacturing", *IEEE Transaction on Control Systems Technology*, vol. 18, pp. 1371 - 1380, 2010.

[28] Schaper C. D., EI-Awady K., Kailath T., Tay A., Lee L. L., Ho W. K. and Fuller S., "Characterizing photolithographic linewidth sensitivity to process temperature variations for advanced resists using a thermal array", *Applied Physics A*, vol. 80, no. 4, pp. 899 - 902, 2005.

[29] Tay A., Chua H. T., Wang Y. and Ngo Y. S., "Equipment Design and Control of Advanced Thermal-Processing Module in Lithography", *IEEE Transaction on Industrial Electronics*, vol. 57, no. 3, pp. 1112 - 1119, 2010.

[30] Incropera F. P. and DeWitt D. P., *Fundamentals of Heat and Mass Transfer*, John Wiley and Sons, New York, 2011.

[31] Hollands K. G., Raithby G. and Konicek L., "Correlation equations for free convection heat transfer in horizontal layers of air and water",

International Journal of Heat and Mass Transfer, vol. 18, pp. 879 - 884, 1975.

[32] Raznjevic K., *Handbook of Thermodynamic Tables and Charts*, Washington, DC: Hemisphere, 1976.

[33] Tay A., Ho W. K., Loh A. P., Lim K. W., Tan W. W. and Schaper C. D., "Integrated bake/chill module with in-situ temperature measurement for photoresist process ing", *IEEE Transaction on Semiconductor Manufacturing*, vol. 17, no. 2, pp. 231 - 242, 2004.

[34] Ho W. K., Tay A., Zhou Y. and Yang K., "In Situ Fault Detection of Wafer Warpage in Microlithography", *IEEE Transaction on Semiconductor Manufacturing*, vol. 17, no. 3, pp. 402 - 407, 2004.

[35] Ljung L, *System Identification: Theory for the User*, Prentice Hall: New York, 1999.

[36] Swenson C. A., "Recommended Values for the Thermal Expansivity of Silicon from 0 to 1000 K", *Journal of Physical and Chemical Reference Data*, vol. 12, no. 2, pp. 179 - 182, 1983.

[37] Franklin G. F., Powell J. D. and Emami-Naeini A., *Feedback Control of Dynamic Systems*, Pearson, 2009.

[38] Tay A., Ho W. K., Hu N. and Chen X. Q., "Estimation of wafer warpage profile during thermal processing in microlithography", *Review of Scientific Instruments*, vol. 76, pp. 075111, 2005.

[39] Fadda E., Clarisse C., and Paniez P. J., "Bake mechanisms in novolak-based photoresist films: Investigation by contact angle measurements", In *Proceedings of the SPIE*, vol. 2724, pp. 460 468, 1996.

[40] Lee L. L., Schaper C. D., and Ho W. K., "Real-time predictive control of photoresist film thickness uniformity", *IEEE Transaction on Semiconductor Manufacturing*, vol. 15, no. 1, pp. 51 59, 2002.

[41] Morton S. L., Degertekin F. L., and Khuri-Yakub B. T., "Ultrasonic monitoring of photoresist processing", In *Proceedings of the SPIE*, vol. 3677, pp. 340 347, 1999.

[42] Agrawal A. and Henderson C. L., "Monitoring the dissolution rate of photoresist thin film via multiwavelength interferometry", In *Proceedings of the SPIE*, vol. 5038, pp. 1026 1037, 2003.

[43] Wang G., Arwin H. and Jansson R., "An Optical Gas Sensor based on Ellipsometric Readout", *IEEE Sensors Journal*, vol. 3, no. 6, pp. 739 - 743, 2003.

[44] Watkins L. R., "Spectroscopic ellipsometer based on direct measurement of polarization ellipticity", *Applied Optics*, vol. 50, no. 18, pp. 2973 - 2978, 2011.

[45] Landis S., *Lithography: main techniques*, Wiley-ISTE, Hoboken, NJ, 2011.

[46] Seligson D., Das S., Gaw H. and Pianetta P., "Process control with chemically amplification resists using deep ultraviolet and x-ray radia-

tion", *Journal Vacuum Science Technology B*, vol. 6, pp. 2303 - 2307, 1988.

[47] Asai S., Hanyu I., Nunokawa M. and Abe M., "Modeling Thermal Effect for Simulation of Post Exposure Baking (PEB) Process in Positive Photoresist", *Japanese Journal of Applied Physics*, vol. 30, pp. 612 - 614, 1991.

[48] Park J. B., Kim S. H., Kim S. J., Cho J. H. and Oh H. K., "Acid Diffusion Length Corresponding to Post Exposure Bake Time and Temperature", *Japanese Journal of Applied Physics*, vol. 46, pp. 28 - 30, 2007.

[49] Tompkins H. G. and Irene E. A., *Handbook of Ellipsometry*, William Andrew Publishing: Springer, 2005.

[50] Suchart S. and Chitaree R., "A Novel Optical Fiber Ellipsometer", In *Proceedings of the IEEE Asia-Pacific Conference on Circuits and Systems*, pp. 205 - 208, 1998.

[51] Eduard G. and Robert S., "Imaging ellipsometry based method and algorithm for the analysis of fiber-fiber bonds in a paper network", *Applied Optics*, vol. 51, no. 2, pp. 273 - 280, 2012.

[52] Pollard A. F. and House H., "Fast-response Automatic Ellipsometer", *Electronics Letters*, vol. 4, no. 9, pp. 166 - 167, 1968.

[53] Tsai C. C., Liao K. Y. and Chou C., "TN-LC Cells as an Elliptical Phase Retarder by Heterodyne Interferometric Ellipsometry", In

Proceedings of Quantum Electronics and Laser Science Conference, pp. 1582 - 1584, 2005.

[54] Watkins L. R., "Accurate heterodyne interferometric ellipsometer", *Optics and Lasers in Engineering*, vol. 48, no. 1, pp. 114 - 118, 2010.

[55] "SOPRA Theory Document." [Online]. Available: http://www.sopra-sa.com [2007].

[56] Röseler A., *Infrared Spectroscopic Ellipsometry*, Berlin: Akademie-Verlag, 1st Edition, 1990.

[57] Silva C. W., *Mechatronics: An Integrated Approach*, CRC Press, Boca Raton, FL, USA, 2011.

[58] Butler S. W. and Stefani J. A., "Supervisory run-to-run control of polysilicon gate etch using in situ ellipsometry", *IEEE Transaction on Semiconductor Manufacturing*, vol. 7, no. 2, pp. 193 201, 1994.

[59] Chemali C., Freudenberg J., Hankinson M., Collison W. and Ni T., "Critical dimension control of a plasma etch process by integrating feedforward and feedback run-to-run control", *Journal Vacuum Science Technology B*, vol. 21, no. 6, pp. 2304 2312, 2003.

[60] Kota G. P., Luque J., Vahedi V., Khathuria A., Dziura T. and Levy A., "Advanced process control for polysilicon gate etching using integrated CD metrology", In *Proceedings of SPIE*, vol. 5044, pp. 12 - 18, 2003.

[61] Ruegsegger S., Wagner A., Freudenberg J. S. and Grimard D. S., "Feedforward control for reduced run-to-run variation in microelectron-

ics manufacturing", *IEEE Transaction on Semiconductor Manufacturing*, vol. 12, no. 4, pp. 493 502, 1999.

[62] Tay A., Ho W. K., Wu X. and Chen X., "In Situ Monitoring of Photoresist Thickness Uniformity of a Rotating Wafer in Lithography", *IEEE Transactions on Instrumentation and Measurement*, vol. 58, no. 12, pp. 3978 - 3984, 2009.

[63] Tay A., Ho W. K. and Wu X., "Real-Time Control of Photoreisit Extinction Coefficient Uniformity in the Microlithogrpahy Process", *IEEE Transactions on Control Systems Technology*, vol. 15, no. 1, pp. 99 - 105, 2007.

[64] Paulsson A., Xing K., Fosshaug H., Lundvall A., Björnberg C. and Karlsson J., "Managing effects in CD control from PED and PEB in advanced DUV photomask manufacturing using FEP-171 resist", In *Proceedings of the SPIE*, vol. 5753, pp. 1119 - 1128, 2005.

[65] Sohn Y. S., Sung M. G., Lee Y. M., Oh J. K., Byun S. H., Jeong Y. U., Oh H. K., An I., Lee K. S., Park I. H., Cho J. Y. and Lee S. H., "Photoresist Exposure Parameter Extraction from Refractive Index Change during Exposure", *Japanese Journal of Applied Physics*, vol. 37, pp. 6877 - 6883, 1998.

[66] Sohn Y. S., Oh H. K. and An I., "Parameter extraction for 193 nm chemically amplified resist from refractive index change", *Journal of Vacuum Science and Technology B*, vol. 19, pp. 2077 - 2081, 2001.

[67] Moharam M. and Gaylord T., "Rigorous coupled-wave analysis of planar-grating diffraction", *Journal of the Optical Society of America*, vol. 71, no. 7, pp. 811 - 818, 1981.

[68] Niu X., An integrated system of optical metrology for deep sub-micron lithography, Ph.D. dissertation, University of California at Berkeley, 1999.

[69] Mack C., *Fundamental Principles of Optical Lithography*, Wiley, 2007.

[70] Chen P., "Virtual metrology: A solution for wafer to wafer advanced process control", In *Proceedings of the IEEE International Symposium on Semiconductor Manufacturing Conference*, pp. 155 - 157, 2005.

[71] Khan A. A., Moyne J. R. and Tilbury D. M., "An Approach for Factory-Wide Control Utilizing Virtual Metrology", *IEEE Transactions on Semiconductor Manufacturing*, vol. 20, no. 4, pp. 364 - 375, 2007.

[72] Emslie A.G., Bonner F.T. and Peck L.G., "Flow of a viscous liquid on a rotating disk", *Journal of Applied Physics*, vol. 29, no. 5, pp. 858 - 862, 1958.

[73] Meyerhofer D., "Characteristics of resist films produced by spinning", *Journal of Applied Physics*, vol. 49, no. 7, pp. 3993 - 3997, 1978.

[74] Bornside D. E., Macosko C. W. and Scriven L. E., "Spin coating: Onedimensional model", *Journal of Applied Physics*, vol. 66, no. 11, pp. 5185 - 5193, 1989.

[75] Bornside D. E., Brown R. A., Ackman P. W., Frank J. R., Tryba A. A. and Geyling F. T., "The effect of gas phase convection on mass transfer in spin coating", *Journal of Applied Physics*, vol. 73, no. 2, pp. 585 - 600, 1993.

[76] Han S., Derksen J. and Chun J. H., "Extrusion Spin Coating: An Efficient and Deterministic Photoresist Coating Method in Microlithography", *IEEE Transactions on Semiconductor Manufacturing*, vol. 17, no. 1, pp. 12 - 21, 2004.

[77] Lawrence C. J., "Spin coating with slow evaporation", *Physics Fluid A*, vol. 2, no. 3, pp. 453 - 456, 1990.

[78] Kiew C. M., Control of resist process in lithography, Ph.D. dissertation, National University of Singapore, 2007.

Appendix

Derivation of State-Space Model of the System

$$C_w\dot{T}_w = q_w^{in} + q_w^{out} + q_w^{top} + q_w^{bottom} \tag{A.1}$$

$$C_{ag}\dot{T}_{ag} = q_{ag}^{in} + q_{ag}^{out} + q_{ag}^{top} + q_{ag}^{bottom} \tag{A.2}$$

$$C_p\dot{T}_p = q_p^{in} + q_p^{out} + q_p^{top} + q_p^{bottom} \tag{A.3}$$

$$C_c\dot{T}_c = q_c^{side} + q_c^{top} + q_c^{bottom} \tag{A.4}$$

$$C_h\dot{T}_h = q_h^{side} + q_h^{top} + q_h^{bottom} + q^{input} \tag{A.5}$$

For the wafer modeling, define

$$r_w(i) = \begin{cases} \frac{\triangle r}{k_w A_{ws(i)}}, & 1 \le i \le N-1 \\ \frac{1}{h_w A_{ws(N)}}, & i = N \end{cases} \tag{A.6}$$

$$r_{aw}(i) = \frac{1}{h_w A_{wz(i)}}, 1 \le i \le N \tag{A.7}$$

$$r_{wag}(i) = \frac{z_{ag}/2k_a + z_w/2k_w}{A_{wag(i)}}, 1 \le i \le N \tag{A.8}$$

$$\frac{1}{R_{w(i)}} = \frac{1}{r_{w(i-1)}} + \frac{1}{r_{w(i)}} + \frac{1}{r_{aw(i)}} + \frac{1}{r_{wag(i)}} \tag{A.9}$$

As there are

$$q_{w(i)}^{in} = \frac{k_w A_{ws(i-1)}}{\Delta r}(T_{w(i-1)} - T_{w(i)}), 2 \le i \le N \tag{A.10}$$

$$q_{w(i)}^{out} = \begin{cases} \frac{k_w A_{ws(i)}}{\Delta r}(T_{w(i+1)} - T_{w(i)}), & 1 \le i \le N-1 \\ \\ h_w A_{ws(N)}(-T_{w(N)}), & i = N \end{cases} \tag{A.11}$$

$$q_{w(i)}^{top} = h_w A_{wz(i)}(-T_{w(i)}), 1 \le i \le N \tag{A.12}$$

$$q_{w(i)}^{bottom} = \frac{A_{wag(i)}(T_{ag(i)} - T_{w(i)})}{z_{ag}/2k_a + z_w/2k_w}, 1 \le i \le N \tag{A.13}$$

The Equation A.1 could be expressed as

$$\begin{aligned} C_{w(i)}\dot{T}_{w(i)}(t) = &\frac{1}{r_{w(i-1)}}T_{w(i-1)}(t) + \frac{1}{r_{w(i)}}T_{w(i+1)}(t) \\ &+\frac{1}{r_{wag(i)}}T_{ag(i)}(t) - \frac{1}{R_{w(i)}}T_{w(i)}(t) \end{aligned} \tag{A.14}$$

In the state-space model, we can get

$$F_{ww}(i,i) = -\frac{1}{C_{w(i)}R_{w(i)}}, 1 \le i \le N$$

$$F_{ww}(i,i+1) = \frac{1}{C_{w(i)}r_{w(i)}}, 1 \le i \le N-1$$

$$F_{ww}(i,i-1) = \frac{1}{C_{w(i)}r_{w(i-1)}}, 2 \le i \le N$$

$$F_{wag}(i,i) = \frac{1}{C_{w(i)}r_{wag(i)}}, 1 \le i \le N \tag{A.15}$$

For the air-gap layer modeling, define

$$r_{ag}(i) = \begin{cases} \frac{\triangle r}{k_{ag}A_{ags(i)}}, & 1 \le i \le N-1 \\ \\ \frac{1}{h_{ag}A_{ags(N)}}, & i = N \end{cases} \tag{A.16}$$

$$r_{agp}(i) = \frac{z_{ag}/2k_a + z_p/2k_p}{A_{agp(i)}}, 1 \le i \le N \tag{A.17}$$

$$\frac{1}{R_{ag(i)}} = \frac{1}{r_{ag(i-1)}} + \frac{1}{r_{ag(i)}} + \frac{1}{r_{wag(i)}} + \frac{1}{r_{agp(i)}} \tag{A.18}$$

As there are

$$q_{ag(i)}^{in} = \frac{k_a A_{ags(i-1)}}{\Delta r}(T_{ag(i-1)} - T_{ag(i)}), 2 \le i \le N \tag{A.19}$$

$$q_{ag(i)}^{out} = \begin{cases} \frac{k_a A_{ags(i)}}{\Delta r}(T_{ag(i+1)} - T_{ag(i)}), & 1 \le i \le N-1 \\ h_{ag} A_{ags(N)}(-T_{ag(N)}), & i = N \end{cases} \tag{A.20}$$

$$q_{ag(i)}^{top} = \frac{A_{wag(i)}(T_{w(i)} - T_{ag(i)})}{z_{ag}/2k_a + z_w/2k_w}, 1 \le i \le N \tag{A.21}$$

$$q_{ag(i)}^{bottom} = \frac{A_{agp(i)}(T_{p(i)} - T_{ag(i)})}{z_{ag}/2k_a + z_p/2k_p}, 1 \le i \le N \tag{A.22}$$

The Equation A.2 could be expressed as

$$\begin{aligned} C_{ag(i)}\dot{T}_{ag(i)}(t) = & \frac{1}{r_{ag(i-1)}}T_{ag(i-1)}(t) + \frac{1}{r_{ag(i)}}T_{w(i+1)}(t) \\ & + \frac{1}{r_{wag(i)}}T_{w(i)}(t) + \frac{1}{r_{agp(i)}}T_{p(i)}(t) \\ & - \frac{1}{R_{ag(i)}}T_{ag(i)}(t) \end{aligned} \tag{A.23}$$

The state-space model matrix can be calculated as

$$F_{agag}(i,i) = -\frac{1}{C_{ag(i)}R_{ag(i)}}, 1 \le i \le N$$

$$F_{agag}(i,i+1) = \frac{1}{C_{ag(i)}r_{ag(i)}}, 1 \le i \le N-1$$

$$F_{agag}(i,i-1) = \frac{1}{C_{ag(i)}r_{ag(i-1)}}, 2 \le i \le N$$

$$F_{agw}(i,i) = \frac{1}{C_{ag(i)}r_{wag(i)}}, 1 \le i \le N$$

$$F_{agp}(i,i) = \frac{1}{C_{ag(i)}r_{agp(i)}}, 1 \le i \le N \tag{A.24}$$

For the bake-plate modeling, define

$$r_{ip}(i) = \frac{t_{p(i)}}{k_p A_{ips(i)}}, 2 \le i \le N \tag{A.25}$$

$$r_{op}(i) = \begin{cases} \frac{t_{p(i)}}{k_p A_{ops(i)}}, & 1 \leq i \leq N-1 \\ \\ \frac{1}{h_p A_{ps(N)}}, & i = N \end{cases} \tag{A.26}$$

$$r_{pc}(i) = \frac{z_p/2k_p + z_c/2k_c}{A_{pc(i)}} + R_{ex(i)}, 1 \leq i \leq N \tag{A.27}$$

$$r_{pe}(i) = \frac{1}{h_p A_{pa(i)}}, 1 \leq i \leq N \tag{A.28}$$

$$\frac{1}{R_{p(i)}} = \frac{1}{r_{ip(i)}} + \frac{1}{r_{op(i)}} + \frac{1}{r_{agp(i)}} + \frac{1}{r_{pc(i)}} + \frac{1}{r_{pe(i)}} \tag{A.29}$$

As there are

$$q^{in}_{p(i)} = \frac{k_p A_{ips(i)}}{t_{p(i)}}(T_{p(i-1)} - T_{p(i)}), 2 \leq i \leq N \tag{A.30}$$

$$q^{out}_{p(i)} = \begin{cases} \frac{k_p A_{ops(i)}}{t_{p(i)}}(T_{p(i+1)} - T_{p(i)}), & 1 \leq i \leq N-1 \\ \\ h_p A_{ps(N)}(-T_{p(N)}), & i = N \end{cases} \tag{A.31}$$

$$q^{top}_{p(i)} = \frac{A_{agp(i)}(T_{ag(i)} - T_{p(i)})}{z_{ag}/2k_a + z_p/2k_p}, 1 \leq i \leq N \tag{A.32}$$

$$\begin{aligned} q^{bottom}_{p(i)} = & \frac{(T_{c(i)} - T_{p(i)})}{\frac{z_p/2k_p + z_c/2k_c}{A_{pc(i)}} + R_{ex(i)}} \\ & + h_p A_{pa(i)}(-T_{p(i)}), 1 \leq i \leq N \end{aligned} \tag{A.33}$$

where the $R_{ex(i)} = \frac{z_{ex}}{k_{ex} A_{pc(i)}}$ is the thermal resistance of epoxy layer of element i.

Thus the Equation A.3 could be expressed as

$$\begin{aligned} C_{p(i)}\dot{T}_{p(i)}(t) = & \frac{1}{r_{ip(i)}} T_{p(i-1)}(t) + \frac{1}{r_{op(i)}} T_{p(i+1)}(t) \\ & + \frac{1}{r_{agp(i)}} T_{ag(i)}(t) + \frac{1}{r_{pc(i)}} T_{c(i)}(t) \\ & - \frac{1}{R_{p(i)}} T_{p(i)}(t) \end{aligned} \tag{A.34}$$

The state-space model matrix can be calculated as

$$F_{pp}(i,i) = -\frac{1}{C_{p(i)} R_{p(i)}}, 1 \leq i \leq N$$

$$F_{pp}(i,i-1)=\frac{1}{C_{p(i)}r_{ip(i)}},2\le i\le N$$

$$F_{pp}(i,i+1)=\frac{1}{C_{p(i)}r_{op(i)}},1\le i\le N-1$$

$$F_{pag}(i,i)=\frac{1}{C_{p(i)}r_{agp(i)}},1\le i\le N$$

$$F_{pc}(i,i)=\frac{1}{C_{p(i)}r_{pc(i)}},1\le i\le N \tag{A.35}$$

For the cartridge modeling, define

$$r_c(i)=\frac{1}{h_cA_{cs(i)}},1\le i\le N \tag{A.36}$$

$$r_{ch}(i)=\frac{z_c/2k_c+z_h/2k_h}{A_{ch(i)}},1\le i\le N \tag{A.37}$$

$$r_{ce}(i)=\frac{1}{h_cA_{ca(i)}},1\le i\le N \tag{A.38}$$

$$\frac{1}{R_{c(i)}}=\frac{1}{r_{c(i)}}+\frac{1}{r_{pc(i)}}+\frac{1}{r_{ch(i)}}+\frac{1}{r_{ce(i)}} \tag{A.39}$$

As there are

$$q_{c(i)}^{side}=h_cA_{cs(i)}(-T_{c(i)}),1\le i\le N \tag{A.40}$$

$$q_{c(i)}^{top}=\frac{(T_{p(i)}-T_{c(i)})}{\frac{z_p/2k_p+z_c/2k_c}{A_{pc(i)}}+R_{ex(i)}},1\le i\le N \tag{A.41}$$

$$\begin{aligned}q_{c(i)}^{bottom}=&\frac{A_{ch(i)}\cdot(T_{h(i)}-T_{c(i)})}{z_c/2k_c+z_h/2k_h}\\&+h_cA_{ca(i)}(-T_{c(i)}),1\le i\le N\end{aligned} \tag{A.42}$$

Thus the Equation A.4 could be expressed as

$$\begin{aligned}C_{c(i)}\dot{T}_{c(i)}(t)=&\frac{1}{r_{pc(i)}}T_{p(i)}(t)+\frac{1}{r_{ch(i)}}T_{h(i)}(t)\\&-\frac{1}{R_{c(i)}}T_{c(i)}(t)\end{aligned} \tag{A.43}$$

The state-space model matrix can be calculated as

$$F_{cc}(i,i) = -\frac{1}{C_{c(i)}R_{c(i)}}, 1 \leq i \leq N$$

$$F_{cp}(i,i) = \frac{1}{C_{c(i)}r_{pc(i)}}, 1 \leq i \leq N$$

$$F_{ch}(i,i) = \frac{1}{C_{c(i)}r_{ch(i)}}, 1 \leq i \leq N \tag{A.44}$$

For the heater modeling, define

$$r_h(i) = \frac{1}{h_h A_{hs(i)}}, 1 \leq i \leq N \tag{A.45}$$

$$r_{he}(i) = \frac{1}{h_h A_{ha(i)}}, 1 \leq i \leq N \tag{A.46}$$

$$\frac{1}{R_{h(i)}} = \frac{1}{r_{h(i)}} + \frac{1}{r_{ch(i)}} + \frac{1}{r_{he(i)}} \tag{A.47}$$

As there are

$$q^{side}_{h(i)} = h_h A_{hs(i)}(-T_{h(i)}), 1 \leq i \leq N \tag{A.48}$$

$$q^{top}_{h(i)} = \frac{A_{ch(i)} \cdot (T_{p(i)} - T_{c(i)})}{z_c/2k_c + z_h/2k_h}, 1 \leq i \leq N \tag{A.49}$$

$$q^{bottom}_{h(i)} = h_h A_{ha(i)}(-T_{h(i)}), 1 \leq i \leq N \tag{A.50}$$

Thus the Equation A.5 could be expressed as

$$\begin{aligned} C_{h(i)}\dot{T}_{h(i)}(t) =& \frac{1}{r_{ch(i)}}T_{c(i-1)}(t) - \frac{1}{R_{h(i)}}T_{h(i)}(t) \\ &+ q^{input} \end{aligned} \tag{A.51}$$

The state-space model matrix can be calculated as

$$F_{hh}(i,i) = -\frac{1}{C_{h(i)}R_{h(i)}}, 1 \leq i \leq N$$

$$F_{hc}(i,i) = \frac{1}{C_{h(i)} r_{ch(i)}}, 1 \le i \le N \tag{A.52}$$

Therefore, the system could be modeling as

$$\dot{T} = \begin{bmatrix} \dot{T}_w \\ \dot{T}_{ag} \\ \dot{T}_p \\ \dot{T}_c \\ \dot{T}_h \end{bmatrix} = \begin{bmatrix} F_{ww} & F_{wag} & 0_{NN} & 0_{NN} & 0_{NN} \\ F_{agw} & F_{agag} & F_{agp} & 0_{NN} & 0_{NN} \\ 0_{NN} & F_{pag} & F_{pp} & F_{pc} & 0_{NN} \\ 0_{NN} & 0_{NN} & F_{cp} & F_{cc} & F_{ch} \\ 0_{NN} & 0_{NN} & 0_{NN} & F_{hc} & F_{hh} \end{bmatrix} \cdot \begin{bmatrix} T_w \\ T_{ag} \\ T_p \\ T_c \\ T_h \end{bmatrix} + \begin{bmatrix} 0_N \\ 0_N \\ 0_N \\ 0_N \\ G_{hh} \end{bmatrix} \cdot q^{input} \tag{A.53}$$

where the excitation matrix

$$G_{hh} = \begin{bmatrix} 1/C_{h(1)} & 0 & \cdots & 0 \\ 0 & 1/C_{h(2)} & & \vdots \\ \vdots & & \ddots & 0 \\ 0 & \cdots & 0 & 1/C_{h(N)} \end{bmatrix} \tag{A.54}$$

w: wafer

ag: air-gap

p: bake-plate

c: cartridge

h: heater

T: temperature above ambient

C: thermal capacitance

q: heat flow

k: thermal conductivity coefficient

h: the convection coefficient

Δr: the distance between the centroid of the adjacent element

$r_{w(i)}$: the thermal resistance between wafer element i and $i+1$

$r_{aw(i)}$: the thermal resistance between the air on top area and wafer of element i

$r_{wag(i)}$: the thermal resistance between the air gap layer and wafer of element i

$r_{ag(i)}$: the thermal resistance between air-gap element i and $i+1$

$r_{agp(i)}$: the thermal resistance between air-gap layer and bake-plate of element i

$r_{ip(i)}$: the thermal resistance between bake-plate element i and its inner adjacent air-gap

$r_{op(i)}$: the thermal resistance between bake-plate element i and its outer adjacent air-gap

$r_{pc(i)}$: the thermal resistance between the bake-plate and cartridge of element i

$r_{pe(i)}$: the thermal resistance between the bake-plate and air layer at bottom of element i

$r_{c(i)}$: the thermal resistance between cartridge element i and its surrounding air

$r_{ch(i)}$: the thermal resistance between the cartridge and heater of element i

$r_{ce(i)}$: the thermal resistance between cartridge element i and the air at its bottom

$r_{h(i)}$: the thermal resistance between heater element i and its surrounding air

$r_{he(i)}$: the thermal resistance between heater element i and the air at its bottom

$R_{ex(i)}$: the thermal resistance of epoxy layer of element i

$A_{ws(i)}$: the contact area between the adjacent elements i and $i+1$ of wafer

$A_{ws(N)}$: the wafer side surface area

$A_{wz(i)}$: the top area of wafer element i exposed to the ambient

$A_{wag(i)}$: the contact cross-sectional area between wafer and air-gap layer of element i

$A_{agp(i)}$: the contact cross-sectional area between air-gap layer and the bake-plate of element i

$A_{ags(i)}$: the contact area between the adjacent elements i and $i+1$ of air-gap layer

$A_{ags(N)}$: the air-gap layer side surface area

$A_{ips(i)}$: the contact area between the bake-plate of zone i and the inner adjacent air-gap

$A_{ops(i)}$: the contact area between the bake-plate of zone i and the outer adjacent air-gap

$A_{ps(N)}$: the bake-plate side surface area

$A_{pc(i)}$: the contact cross-sectional area between the bake-plate and the cartridge of element i

$A_{pa(i)}$: the contact cross-sectional area between the bake-plate and the the bottom ambient of element i

$A_{cs(i)}$: the area of the cartridge side surface of element i exposed to the surrounding air

$A_{ch(i)}$: the contact cross-sectional area between the the cartridge and the heater of element i

$A_{ca(i)}$: the area of the cartridge bottom surface of element i exposed to the ambient

$A_{hs(i)}$: the area of the heater side surface of element i exposed to the surrounding air

$A_{ha(i)}$: the area of the heater bottom surface of element i exposed to the ambient

z_w: wafer thickness

z_{ag}: air-gap thickness

z_p: bake-plate thickness

z_c: cartridge thickness

z_h: heater thickness

$t_{p(i)}$: the horizontal length of the bake-plate between the element i and $i+1$

Author's Publications

[1] Tay A., Chua H. T., Wang Y., Yang G. and Ho W. K., "Modeling and real-time control of multi-zone thermal processing system for photoresist processing", *Industrial & Engineering Chemistry Research*, vol. 52, no. 13, pp. 4805 - 4814, 2013.

[2] Yang G., Tay A. and Ho W. K., "Real-time spatial CD signature monitoring and control: Equipment development and Experimental results", *Microelectronic Engineering*, submitted, 2012.

[3] Yang G., Tay A. and Ho W. K., "Development of In-Situ Real-Time CD Monitoring and Control System through PEB Process", In *Proceedings of the 24th Chinese Control and Decision Conference*, pp. 3080 - 3085, 2012.

[4] Yang G., Ngo Y. S., Putra A. S., Ang K. T., Tay A. and Fang Z. P., "Monitoring and control of photoresist properties and CD during photoresist processing", In *Proceedings of SPIE*, vol. 7638, pp. 763828, 2010.

[5] Ngo Y. S., Yang G., Putra A. S., Ang K. T., Tay A. and Fang Z. P., "Equipment Design and Process Control of Critical Dimensions

in Lithography", In *Proceedings of the 8th IEEE International Conference on Control and Automation*, pp. 1572-1577, 2010.

[6] Wu X. D., Yang G., Lim E. X. and Tay A., "In-situ monitoring and control of photoresist parameters during thermal processing in the lithography sequence", In *Proceedings of SPIE*, vol. 7520, pp. 752035, 2009.

[7] Tay A., Chua H. T., Wang Y. and Yang G., "Control of semiconductor substrate temperature uniformity during photoresist processing in lithography", In *Proceedings of the 7th Asian Control Conference*, pp. 853-858, 2009.