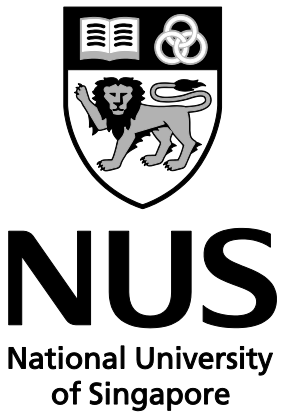
ANALYSIS AND DESIGN OF SILICON-BASED MILLIMETER-WAVE AMPLIFIERS



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ANALYSIS AND DESIGN OF SILICON-BASED MILLIMETER-WAVE AMPLIFIERS

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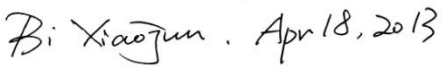
DECLARATION

I hereby declare that this thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.



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SUMMARY

With the continuous scaling of silicon processes, interest in silicon-based millimeter-wave frontends has been growing over the past few years. As the dominant roles in these silicon-based front-ends, the millimeter-wave amplifiers, including the power amplifier (PA) and the low noise amplifier (LNA), encounter numerous design challenges owing to the higher operating frequencies. This thesis aims to analyze the existing issues and propose new circuit topologies to overcome these challenges.

In order to enhance the output power and bandwidth of the 60 GHz power amplifiers, the performance enhancement by unilateralization technique is investigated. To evaluate these performance enhancements, a 60 GHz differential power amplifier in 90-nm CMOS is designed and fabricated. The amplifier demonstrates competitive performance compared with the state-of-art 60 GHz PAs using technologies with similar f_t/f_{max}.

Then, by investigating the channelization of the 60 GHz WPAN in IEEE Standard 802.15.3c, a band-tunable 60 GHz CMOS power amplifier is proposed and fabricated in 65 nm standard CMOS technology. This amplifier utilizes a differential band-switching circuit to tune the center frequency to the channel in use, while high-Q transformer matching and deep-neutralized differential pairs are employed to achieve high gain and PAE in a narrow bandwidth. Therefore, high gain and PAE covering the whole 7 GHz frequency band are obtained.

On the other hand, the design of the pre-amplifier in W-band imaging receiver requires additional circuit design methods which differ from those used in conventional LNAs. Important design factors that must be carefully considered for W-band amplifier are analyzed, including gain, noise figure, frequency selectivity, dynamic range and stability. Moreover, effective passive-structures are developed to overcome the stability degradation which is mainly caused by the very high forward gain and reduced reverse isolation. Overall, an ultra-high gain (>45 dB) amplifier with bandpass magnitude

response is proposed and evaluated. It could be helpful to simplify the W-band imaging receiver architecture.

Meanwhile, extracting more maximum available gain (MAG) out of a given device technology is fundamentally challenging in the millimeter-wave range. A cascode stage utilizing a passive compensation network is proposed to cancel the Miller-effect at millimeter-wave range without distinct penalty on noise figure and stability. This cascode stage demonstrates a record MAG at the applied band. In addition, the Miller-effect cancelling method can also be applied to the other building blocks.

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LIST OF ABBREVIATIONS

BEOL	Back-End-Of-Line
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
BPSK	Binary Phase Shift Keying
CMOS	Complementary Metal Oxide Semiconductor
CPCN	Capacitor Phase-inverter Capacitor Network
CSPF	Common Source Parallel Feedback
DAT	Distributed Active Transformer
EHF	Extremely High Frequency
EM	Electro-Magnetic
ENR	Excess Noise Ratio
EVM	Error Vector Magnitude
FET	Field Effect Transistor
f_{max}	Maximum Oscillation Frequency
FOM	Figure-Of-Merit
f_t	Transition Frequency
GaAs	Gallium Arsenide
GaN	Gallium Nitride
GSG	Ground-Signal-Ground
HFSS	High Frequency Structure Simulator
InP	Indium Phosphide
ISS	Impedance Standard Substrate

KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LNA	Low Noise Amplifier
LO	Local Oscillator
LRRM	Line Reflect Reflect Match
MIM	Metal Insulator Metal
MOM	Metal Oxide Metal
MOS	Metal Oxide Semiconductor
MAG	Maximum Available Gain
MSG	Maximum Stable Gain
NEΔT	Noise Equivalent Delta Temperature
NEP	Noise Equivalent Power
NF	Noise Figure
NMOS	N-type Metal Oxide Semiconductor
OIP3	Output 3rd Order Intercept Point
OOK	On-Off Keying
OP1dB	Output 1 dB Compression Point
P1dB	1 dB Compression Point
PA	Power Amplifier
PAE	Power Added Efficiency
PCB	Printed Circuit Board
PSD	Power Spectrum Density
Q-factor	Quality Factor

QPSK	Quadrature Phase Shift Keying
SC-GCPW	Semi-coaxial Grounded Coplanar Waveguide
SiGe	Silicon-Germanium
SNR	Signal to Noise Ratio
SOI	Silicon On Insulator
SW	Shielding Wall
TL	Transmission Line
TPR	Total Power Radiometer
UWB	Ultra-Wideband
VCO	Voltage Controlled Oscillator
VNA	Vector Network Analyzer
WPAN	Wireless Personal Area Network

CHAPTER 1

Introduction

1.1 Background

Millimeter-wave band runs the range of frequencies from 30 to 300 GHz, which is also known as extremely high frequency (EHF) band. Compared to lower bands, the features of EHF are high operating frequency, proportionately large amount of spectrum available and diversified propagation characteristics of different frequencies [1]. Due to these features, millimeter-wave circuits have been widely used in high-speed communications, inter-satellite links, radar communications, imaging, remote sensing etc. More specifically, the band 38.6-40.0 GHz is utilized for licensed high-speed microwave data links; the 60 GHz band can be used for unlicensed short range data links; the 71-76, 81-86 and 92-95 GHz bands are employed for point-to-point high-bandwidth communication links and imaging applications; and 94 GHz, 110 GHz to 170 GHz can be used in high speed communication and imaging systems [1], [2].

Traditionally, millimeter-wave integrated circuits are implemented in III-V technologies such as GaAs, GaN, InP etc. They are shown to be superior to silicon in noise figure, f_t, f_{max} and power handling capability [3], [4]. However,

driven by the demand for low cost consumer electronics and highly integrated systems, silicon process is more attractive. The study of silicon based millimeter-wave integrated circuits has been popular in recent years due to the development of Complementary Metal Oxide Semiconductor (CMOS) and Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) technologies. Benefitting from down scaling, CMOS/BiCMOS transistors became small enough, and consequently fast enough, to operate in the millimeter-wave range and beyond. As a consequence, radio frequency (RF) building blocks including power amplifier (PA), low noise amplifier (LNA), mixer, oscillator, frequency synthesizer etc. are gradually implemented in CMOS and BiCMOS technologies for millimeter-wave bands.

Nonetheless, the faster transistors do not necessarily mean that all obstacles on the path of realizing millimeter-wave integrated circuits in CMOS or BiCMOS technologies have been cleared. Some mechanisms in the CMOS and BiCMOS process may result in a poor performance of millimeter-wave integrated circuits. For instance, conductive losses in metals, the lossy silicon substrate, and radiation by metal patterns all may result in a low Q passive connection or component [5]. Many techniques such as new types of transmission line or shielding have to be used to alleviate these problems. In addition, the transistor performance may be degraded directly from the layout dependent f_t and f_{max}, due to the parasitic effects that generally exist at such a high frequency [5].

Two of the well-known RF building blocks, PA and LNA, play the dominant role in the transmitting and receiving path respectively. PA is the last amplifying stage in the transmitter, and it decides the transmitted signal quality in terms of power and linearity. On the other hand, LNA is the first gain stage in the receiver path. It determines the overall system noise figure. For PA and LNA implemented in advanced CMOS/BiCMOS processes, they will suffer from the above-mentioned limitations and degradation. Consequently, there is a need for innovative circuit and layout techniques to obtain better millimeter-wave PA and LNA performance.

1.2 Review of Millimeter-wave Amplifiers

As mentioned above, with the scaling of transistors, efforts have been put into implementing satisfying PAs and LNAs in CMOS/BiCMOS technology to meet the requirement of specific millimeter-wave systems. In this section, the recent advance of millimeter-wave CMOS/BiCMOS PAs and LNAs is reviewed.

For millimeter-wave CMOS/BiCMOS PA and LNA design, each of them has its own specific challenges besides the common challenges described in Section 1.1. For PA design, the main challenges are high gain, output power and efficiency in millimeter-wave bands as the working frequency of these amplifiers are approaching transistor cut-off frequencies. In 2007, the first successfully implemented silicon-based 60 GHz PA was reported using a 90 nm CMOS technology with transistor f_t/f_{max} of 120 GHz/200 GHz [6]. However, due to the use of these low f_t/f_{max} transistors and low Q passive

components, the PA only achieved a measured power gain of 5.2 dB, a power added efficiency (PAE) of 7 % and a saturated power of +9.3 dBm. In a study reported in 2008, due to the reduced passive loss using first metal ground shielding from lossy silicon substrates, a PA obtained a linear power gain of 19.7 dB at 52.4 GHz and 10.3 dB at 60 GHz [7]. In the same year, a transformer-coupled two-stage PA was implemented in 90 nm digital CMOS technology. This design greatly shrunk the area of transmission line based matching network and reduced the loss incurred by the substrate [8]. The PA obtained an output power of 12.3 dBm and PAE of 8.8 % with a peak power gain of 7.7 dB. Nonetheless, according to IEEE standard for wireless HD video streaming system (IEEE Std 802.15.3c), the above PAE and gain were still not enough. In 2009, innovations were made in both passive connections [9] and amplifying stages [10], which led to improved PA performance in terms of gain and PAE. In [9], the use of balanced transmission lines with artificial dielectric reduced PA size as well as passive loss. The PA fabricated in 90 nm CMOS technology achieved a remarkable PAE of 19.3 % and a saturated output power of 12.5 dBm. In [10], neutralization capacitances were used in differential FET pairs which partially cancelled C_{gd} and resulted in a gain of 15.8 dB and a PAE of 11%. Later on, 65 nm CMOS silicon-on-insulator (SOI) process with high resistivity substrate (3 kΩ·cm) was utilized in the PA design which provided almost perfect isolation between substrate and active regions. The PA implemented in this process achieved a remarkable peak PAE of 25% [11]. Nevertheless, referring to [9]-[11], it seems that the 60

GHz PA can only achieve a high PAE at a relatively high power supply (above 1.2 volts) or with special process which may increase manufacturing cost.

For LNA, since W-band LNA needs a large gain with a stringent noise requirement in the imaging system, it is chosen as a representative example in this section. In 2008, a W-band LNA implemented in 0.25 μm SiGe BiCMOS technology was reported [12]. The LNA demonstrated a gain of 16 dB and a noise figure of 10.6 dB with power consumption of 61 mW. Although this LNA could operate at 94 GHz successfully, it suffered from poor signal-to-noise ratio (SNR). In the same year, another LNA fabricated in 0.13 μm SiGe BiCMOS technology reported about 19 dB gain with 8.5 dB noise figure under 25 mW power consumption [13]. However, for direct detection imaging systems which generally require more than 30 dB gain, the achieved gain is not high enough [14]. In 2009, an LNA in 0.13 μm SiGe BiCMOS was reported with around 23 dB gain and 8 dB noise figure while drawing 29 mA from 1.2 V supply [15]. Compared to [13], this LNA used one more cascode stage to obtain a higher power gain. In another work, an LNA implemented in 65 nm CMOS technology was reported of an approximately 30 dB gain with 8 dB noise figure [16]. This lower noise figure was achieved due to the advanced 65 nm CMOS technology which demonstrated a lower noise figure than SiGe technologies. In 2010, the LNA reported in [17] achieved around 20 dB gain with approximately 9 dB noise figure in 0.18 μm SiGe BiCMOS. This LNA unit was actually used in a novel balanced switching LNA system which intended to reduce the switching loss in the Dicke receiver. Although low loss passive connections [13], [15], new processes [16] and novel system

architecture [17] were employed in the LNAs design to obtain higher performance, the LNA gain are below 30 dB. It will be analyzed in Chapter IV that the sensitivity of the receiver could be greatly boosted if higher LNA gain can be achieved. In summary, the review of various reported LNA reveals that the high gain and low noise LNAs required for the W-band imaging systems have not been achieved yet.

1.3 Research Gaps and Purpose for Millimeter-wave Amplifiers

Research gaps for the current silicon-based 60 GHz power amplifiers and W-band low noise amplifiers are summarized as follows:

- Although the reported CMOS and BiCMOS PAs have achieved reasonable PAE and output power, they mostly relied on a high voltage supply and a special process. Besides the transformer-coupled topology [8] and neutralized differential pairs [10], new circuit architecture with improved PA performance needs to be investigated.

- For W-band LNAs, current reported methods to improve W-band LNA performance are limited to using low loss passive connections and special processes. Hence, there is room for innovation to search for LNA with novel architecture.

- The imaging receiver needs a 45 dB ~ 50 dB gain and a noise figure as low as possible to guarantee a threshold temperature resolution which is below 0.5 K [18]. However, the current LNAs fail to meet this requirement. Although a novel receiver architecture [17] was used to alleviate the LNA

requirement to a certain extent. The final achievable performance is still inferior to the receiver with a high gain LNA.

The main objectives of this thesis are to find the path to boost millimeter-wave PA and LNA performance through in-depth analysis and to propose new circuit techniques to enhance the key performances. The objectives are:

- To analyze the effect of neutralized differential pairs on millimeter-wave PA design and gain important design insight to enhance PA performance.

- To propose new methods to optimize the CMOS PA performance based on the feature of 60 GHz WPAN.

- To develop high gain and high selectivity LNA by using novel passives while ensuing high performance with high stability.

- To explore new methods to boost gain of single cascode stage without penalizing the noise figure or power consumption.

1.4 Original Contributions Made by the Author

The aforementioned studies on millimeter-wave PA and W-band LNA could have significant impact on the implementation of high performance millimeter-wave amplifiers. The following summarises the main contributions in this research area.

- The unilateralization criterion is revealed through *Y*-parameter matrix analysis while the performance variation under neutralization is discussed.

- A novel method of achieving above 20 % PAE and 12.3 dBm output power for 60 GHz PA by tuning the band to the frequency range in use.

- A high performance 19 mW, above 45 dB gain and 7.2 dB noise figure 94 GHz high selectivity LNA is realized by using a new pass-band forming method and innovative passive shielding.

- A method to fundamentally boost the gain of cascode stage utilizing a novel passive compensation network.

This thesis incorporates the design, analysis and implementation of 60 GHz PA, and W-band LNA. All the methods and analysis are supported by the measurement of fabricated chips. Although the actual studies are conducted only in the above two millimeter-wave bands, the proposed techniques are applicable to other millimeter-wave bands. In the following four chapters, the 60 GHz PA and W-band LNA designs with chip verification are presented in detail.

1.5 Organization of the Thesis

The thesis is organized as follows:

Chapter 2: This chapter derives the unilateralization criterion for differential amplifiers, followed by analysis on the neutralization effect and a design example of 60 GHz PA in 90 nm CMOS technology.

Chapter 3: This chapter presents a new 60 GHz PA in 65 nm CMOS technology with tunable frequency configuration based on the requirement by

IEEE Standard 802.15.3c. The effects on tunability, power gain and PAE are discussed.

Chapter 4: This chapter presents the W-band imaging frontend requirement on LNA. Techniques to obtain high gain and low shape-factor are explained and their impacts on LNA design are discussed. The implemented high performance LNA in 0.13 μm BiCMOS technology is also demonstrated.

Chapter 5: This chapter presents a W-band gain boosted cascode stage utilizing a novel passive compensation network. The gain boosting effect is analyzed and compared with parallel-resonating method. Measurement results of the chip fabricated in 0.13 μm BiCMOS technology are presented.

Chapter 6: This chapter summarizes the study and draws conclusion. Future work of silicon-based millimeter-wave amplifier is also presented.

1.6 List of Publications

- X. J. Bi, Y. X. Guo, J. Brinkhoff, M. S. Leong, and F. Lin, "60GHz Unilateralized CMOS Differential Amplifier," in *IEEE Int. Conf on Microwave and Millimeter Wave Technology Dig. Papers*, 2010, pp.204-207.

- X. J. Bi, Y. X. Guo, J. Brinkhoff, L. Jia, L. Wang, Y. Z. Xiong, M. S. Leong, and F. Lin, "A 60 GHz 1V-Supply Band-tunable Power Amplifier in 65 nm CMOS," *IEEE Trans. Circuits Syst. II, Express Briefs.*, vol. 58, no. 11, pp.719-723, Nov 2011.

- X. J. Bi, Y. X. Guo, Y. Z. Xiong, M. A. Arasu, M. S. Zhang, and M. K. Je, "Passives Design for A High Performance W-band Amplifier, " *in IEEE MTT-S Int. Microwave Symp.* Dig., 2013, pp.1-3.

- X. J. Bi, Y. X. Guo, Y. Z. Xiong, M. A. Arasu, and M. K. Je, "A 19.2 mW, >45 dB Gain and High-Selectivity 94 GHz LNA in 0.13 μm SiGe BiCMOS," *IEEE Microw. Wireless Compon. Lett.*, vol.23, no.5, pp.261-263, May 2013

- X. J. Bi, Y. X. Guo, and M. K. Je, "Analysis and Design of Gain Enhanced Cascode Stage Utilizing a Novel Passive Compensation Network," *IEEE Trans. Microw. Theory Tech.*, vol.61, no.8, pp.2892-2900, Aug 2013

CHAPTER 2

Analysis of Unilateralized 60 GHz Power Amplifiers

2.1 Introduction

A PA dominates the transceiver's performance in terms of its output power, gain and efficiency. However, for millimeter-wave applications, the low supply voltage used by submicron CMOS processes limits the performance especially the gain which is closely related to the voltage swing at the drain [19]. Moreover, for stability consideration, designers have to reserve sufficient gain margins, which further reduce the achievable gain performance severely. The unilateralization technique proposed by Mason in 1954 gave an effective solution to improve both gain and stability of amplifiers [20]. Since then, the unilateralization technique was further explored in [21]-[23] and becomes increasingly popular. In [24], an amplifier achieved maximum unilateral gain and impedance matching using a novel transformer together with an inductive dual-loop feedback network. In [25], a linear parallel feedback network was utilized to optimize gain and output matching of the power amplifier.

Although these methods are verified at radio frequency range, they may

not be directly applicable to millimeter-wave bands. At millimeter-wave bands, usually the parasitic effects are critical and are highly related to the complexity of the circuits. Thus, to minimize the impact of parasitic, fewer components are preferred in the unilateralization network. Meanwhile, inductors and transformers should be kept minimal as they tend to occupy large chip area and may introduce unnecessary coupling at high frequencies. Furthermore, differential amplifying architecture is generally preferred for low supply amplifier designs. However, only single-ended amplifiers with unilateralization are reported in [24]–[25]. Hence, the reported unilateralization networks may not be directly utilized for differential amplifiers. For a differential amplifier, a pair of drain to source feedback capacitors has been used to improve the stability [26]. Recently, similar concept has been used in a millimeter-wave power amplifier which achieved good stability and gain performance [10]. However, these ideas are only limited to those using cross-coupled capacitors. As a matter of fact, the feedback network can be diversified and two-port *Y*-parameter matrix can be used to judge the status of unilateralization.

In this Chapter, based on the *Y*-parameter analysis, a criterion is derived to evaluate the unilateralization condition of a millimeter-wave differential amplifier. It also gives an intuitive guidance to simplify the design of feedback network in high frequency differential amplifiers. To demonstrate its effectiveness, a transformer based 60 GHz two-stage PA is designed. A pair of capacitors are used as the four-port feedback network. Each capacitor has similar value as the parasitic between drain and gate of the NMOS FET. This

allows the cancelling of the reverse feedback capacitance of C_{gd} and achieves unilateralization. High gain and stability can thus be achieved at the same time. Meanwhile, the drawback may be the slightly increased chip area and narrower bandwidth.

2.2 Unilateralization Criterion Based on *Y*-matrix Analysis

2.2.1 Unilateral *Y*-parameter Network

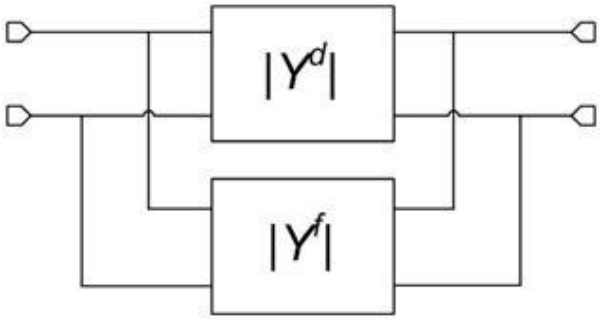


Figure 2.1: Two four-terminal networks connected in parallel.

Unilateralization can be defined as a method of converting a two port bilateral network to a unilateral network [20], [23]. As shown in Figure 2.1, although two two-port networks can be connected in various ways, only two networks in parallel connection will be discussed. This unilaterlization analysis is mainly based on the *Y*-parameter matrix. In the analysis of practical networks such as amplifiers, the forward transfer parameter is related to the forward gain, and the reverse transfer parameter is the undesired feedback effect which needs to be eliminated. For the two parallel Y^{d} and Y^{f} matrices, the resultant matrix Y^{t} is,

$$|Y^t| = \begin{vmatrix} Y_{11}^d + Y_{11}^f & Y_{12}^d + Y_{12}^f \\ Y_{21}^d + Y_{21}^f & Y_{22}^d + Y_{22}^f \end{vmatrix} \tag{2.1}$$

As the unilateralization of the original network requires that

$$Y_{12}^{t} = 0 \tag{2.2}$$

The required condition for unilateralization of the resultant network is

$$Y_{12}^{f} = -Y_{12}^{d} \tag{2.3}$$

Meanwhile, the power gain can be optimized to the unilateral gain (U) [23], where

$$U = \frac{\left|Y_{21}^{t}\right|^{2}}{4 \cdot \mathrm{Re}[Y_{11}^{t}] \cdot \mathrm{Re}[Y_{22}^{t}]} \tag{2.4}$$

Theoretically, the ideal S-parameters matrix of the complete unilateralized amplifier becomes

$$\begin{vmatrix} 0 & 0 \\ \sqrt{U}\angle\Phi & 0 \end{vmatrix} \tag{2.5}$$

With ideal input and output impedance matching and perfect reverse isolation, the input power is amplified to the output port without any reflection. Hence, the objective of the feedback networks is to improve the reverse isolation.

2.2.2 Stability at the Condition of Unilateralization

At the condition of unilateralization, input and output should be perfectly matched and $S_{12} = 0$.

And

$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |\Delta|^2}{2|S_{12}S_{21}|} \tag{2.6}$$

Knowing $S_{12} = 0$, we get $k = +\infty$. Intermediate quantity delta factor is defined as:

$$|\Delta| = |S_{11}S_{22} - S_{12}S_{21}| \tag{2.7}$$

If $|\Delta| < 1$, the amplifier is unconditionally stable.

2.2.3 Four- port Unilaterlization Network for a Differential Amplifier

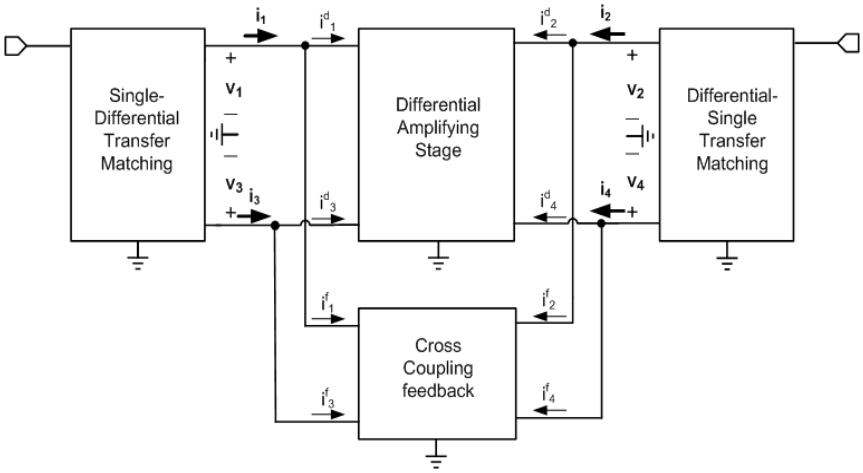


Figure 2.2: Schematic diagram of the differential feedback power amplifier

To minimize the complexity of the circuit design at high frequencies and make the performance more predictable, fewer components for feedback path is preferred. As shown in Figure 2.2, in a differential PA design with feedback networks, the main signal path includes an input single-differential transferring network, an amplifying stage, an output differential-single transferring network and a four-port feedback network. Before analyzing the *Y*-parameter networks, the following assumptions are made:

1) The device is operated in the linear region and the bias is fixed so that the amplifying stage can be represented by a certain *Y*-parameter matrix.

2) Both the amplifying device and feedback networks are ideally symmetrical for the differential paths.

3) The proof is provided only for the case of passive feedback network.

4) Parasitic coupling between differential paths is negligible.

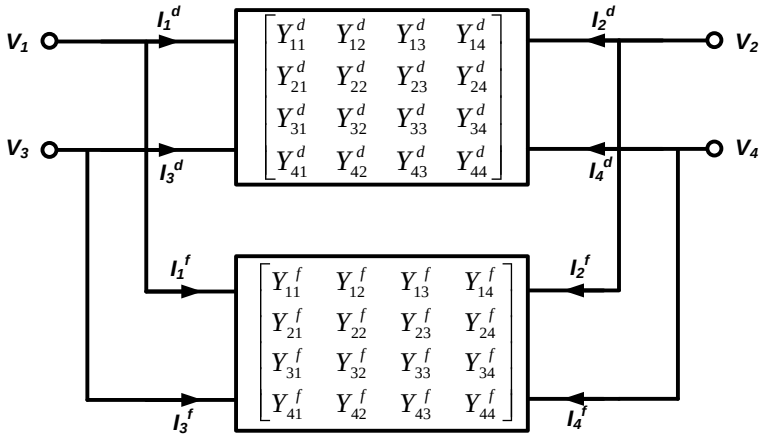


Figure 2.3: Two four-port networks connected in parallel

As illustrated in Figure 2.3, the equations for currents and voltages can be obtained from the linear-network admittance parameters of the devices [Y^d] and the feedback network [Y^f]. After considering the reciprocal and symmetrical passive network of the feedback matrix with ideal network and ensuring no mutual coupling between differential signal paths, we get the following equation:

$$\begin{bmatrix} i_1^d \\ i_2^d \\ i_3^d \\ i_4^d \end{bmatrix} = \begin{bmatrix} Y_{11}^d & Y_{12}^d & 0 & 0 \\ Y_{21}^d & Y_{22}^d & 0 & 0 \\ 0 & 0 & Y_{33}^d & Y_{34}^d \\ 0 & 0 & Y_{43}^d & Y_{44}^d \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} \tag{2.8}$$

For the capacitors feedback network [Y^f], which is reciprocal and symmetrical, the following equations can be assumed:

$$Y_{14}^f = Y_{32}^f = Y_{41}^f = Y_{23}^f \tag{2.9}$$

$$Y_{11}^f = Y_{22}^f = Y_{33}^f = Y_{44}^f \tag{2.10}$$

The feedback network employed is a cross-coupled network, the *Y*-matrix of this feedback network becomes

$$\begin{bmatrix} i_1^f \\ i_2^f \\ i_3^f \\ i_4^f \end{bmatrix} = \begin{bmatrix} Y_{11}^f & 0 & 0 & Y_{14}^f \\ 0 & Y_{22}^f & Y_{23}^f & 0 \\ 0 & Y_{32}^f & Y_{33}^f & 0 \\ Y_{41}^f & 0 & 0 & Y_{44}^f \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} \tag{2.11}$$

By combing equation (2.8) and (2.11), we have equation (2.12) below:

$$\begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ i_4 \end{bmatrix} = \begin{bmatrix} i_1^f + i_1^d \\ i_2^f + i_2^d \\ i_3^f + i_3^d \\ i_4^f + i_4^d \end{bmatrix} = \begin{bmatrix} Y_{11}^d + Y_{11}^f & Y_{12}^d & 0 & Y_{14}^f \\ Y_{21}^d & Y_{22}^d + Y_{22}^f & Y_{14}^f & 0 \\ 0 & Y_{14}^f & Y_{11}^d + Y_{11}^f & Y_{12}^d \\ Y_{14}^f & 0 & Y_{21}^d & Y_{22}^d + Y_{11}^f \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \\ v_3 \\ v_4 \end{bmatrix} \tag{2.12}$$

As shown in the Figure 2.3, if we assume the total two port power amplifier voltages are $V_1 = v_1 - v_3$, $V_2 = v_2 - v_4$ and the differential currents are $I_1 = i_1 - i_3$, $I_2 = i_2 - i_4$. Then, from equation (2.12), we derive:

$$i_1 - i_3 = (Y_{12}^d - Y_{14}^f)(v_2 - v_4) + (Y_{11}^d + Y_{11}^f)(v_1 - v_3) \tag{2.13}$$

Assume the *Y*-matrix of the whole power amplifier is

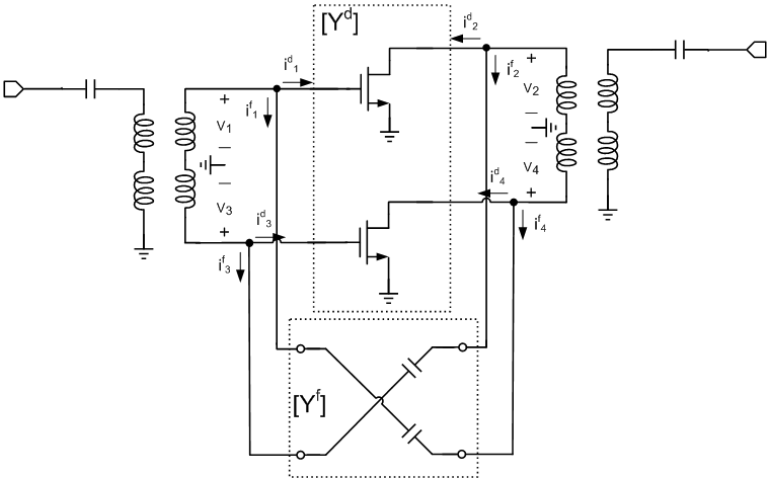
$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11}^U & Y_{12}^U \\ Y_{21}^U & Y_{22}^U \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \tag{2.14}$$

Hence,

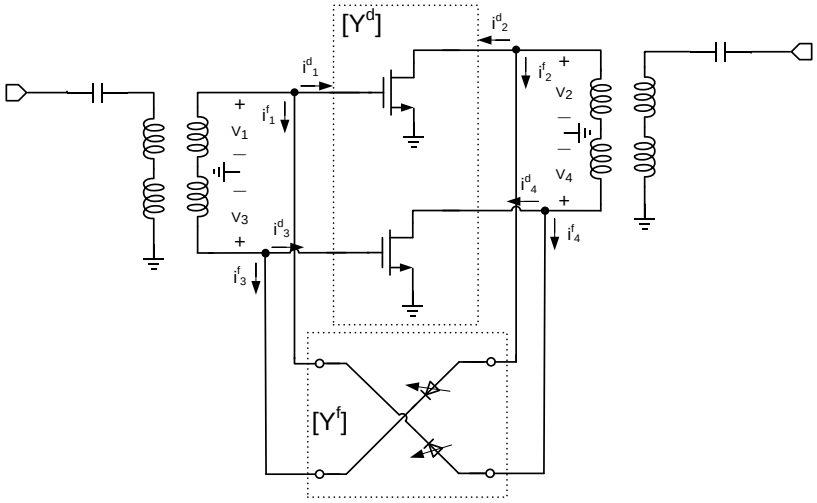
$$Y_{12}^{U} = Y_{12}^{d} - Y_{14}^{f} \tag{2.15}$$

Knowing $Y_{12}^{U} = 0$ in the case of unilaterilization, we can get

$$Y_{14}^{f} = Y_{12}^{d} \tag{2.16}$$



(a) Capacitor feedback network



(b) Varactor feedback network

Figure 2.4 MOSFET based differential amplifier with embedded network realized by a pair of cross-coupled capacitors

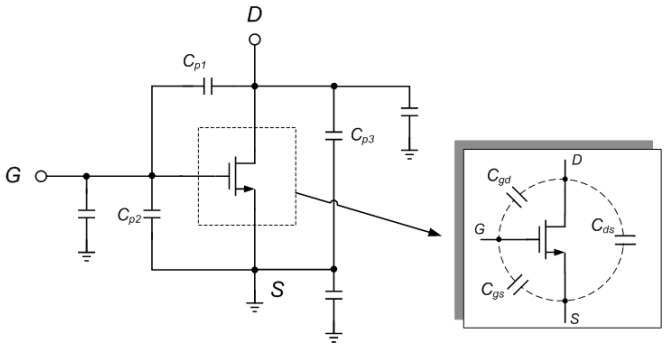
Equation (2.16) gives a simplified criterion to judge the requirement for the feedback network. Y_{14}^{f} represents the reverse cross-transferring coefficient from Port1 to Port 4 of the amplifying network; the intrinsic parasitics responsible for reverse transferring can be cancelled. With the input and output ports matched, the differential amplifier can approach the condition of maximum unilateral gain. Hence, as compared with the feedback network which consists of resistance and reactance in single-path amplifiers, this method provides a more flexible and simple guidance to design the feedback network in a differential amplifier. For the widely used common-source amplifying stages, a simple method to realize this kind of four-port feedback network uses a pair of cross-coupled capacitors. As shown in a simple amplifier design in Figure 2.4 (a), a pair of cross-coupled capacitors are placed between the drain and gate of the NMOS FET. As the source is connected to the ground for heat sink directly, to retain gain at millimeter-wave bands, no source feedback should be used. Since the main reverse transferring coefficient is due to the parasitic capacitance which exists between the drain and the gate, we only need to use a pure capacitive feedback network to cancel it. Different from the feedback network in single-path amplifier as shown in Figure 2.1, only a pair of cross-coupled capacitors are used to cancel the imaginary part of Y_{12}. In this differential power amplifier, Y_{12}^{d} denotes the positive feedback from the drain to the gate.

Hence, the unilateralized capacitor value can be chosen easily, i.e. $C_f = C_{\mathrm{gd}}$. However, due to the small value of this capacitor, it is difficult to achieve

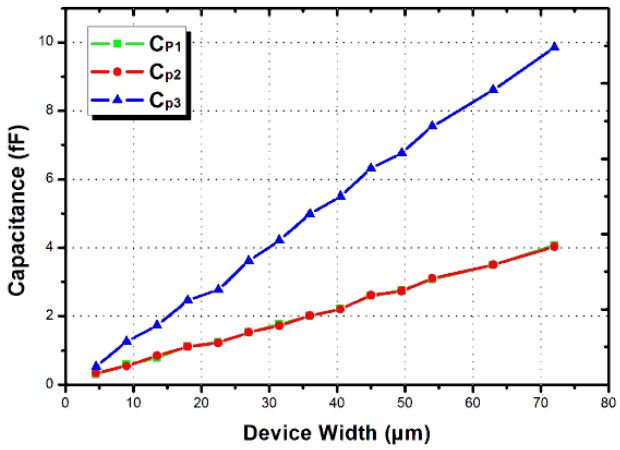
perfect unilateralization due to process variation. If $C_f < C_{gd}$, the feedback effect of C_{gd} is only partially neutralized (under-neutralization). On the other hand, if $C_f > C_{gd}$, the added networks cancel the negative feedback effect of C_{gd}, and provide extra positive feedbacks; the amplifier is then over-neutralized. In these two non-ideal cases, the gain and stability will deteriorate compared to the ideal case. However, the imperfect neutralizations may be useful in the realization of a variable gain amplifier. As shown in Figure 2.4 (b), by employing varactors or variable capacitors arrays, the amplifier can be tuned into weak, deep or over-neutralized conditions. As a result, tunable gain of the amplifier can be realized. However, the additional dc blocking capacitance and biasing inductance should be taken into consideration during the design.

Besides the above gain and stability variation, the bandwidth of the differential stage shrinks if C_f increases from zero to a value more than C_{gd}. This tendency is opposite to the gain variation.

2.2.4 Feedback Capacitance of a Millimeter-Wave Amplifier



(a) Intrinsic capacitor in BSIM4 model and parasitic coupling at millimeter-wave



(b) Simulated parasitic coupling related to device width

Figure 2.5: The main parasitic effects of transistors at millimeter frequency and its equivalent circuit.

In short-channel devices for millimeter-wave amplifier design, the transistor cross sections between the source and the drain metallization contribute significant capacitances [27]: the narrow distances between the source and drain contacts raise the fringing capacitance and create a large coupling between each pair of the three terminals. At millimeter-wave frequencies, the parasitic capacitance between metallization could significantly alter the reverse transferring coefficient of the common source amplifier. As shown in Figure 2.5 (a), the parasitic capacitances between drain-gate, gate-source and drain-source are denoted as C_{p1}, C_{p2} and C_{p3}, respectively. Then, Y_{12}^{d} can be represented by the combination of C_{gd} and C_{p1},

$$Y_{12}^{d} = j\omega(C_{gd} + C_{p1}) \tag{2.17}$$

Hence, the unilateralized capacitor value can be chosen as:

$$C_f = C_{gd} + C_{p1} \tag{2.18}$$

However, the above value might not be correct due to inaccurate assumptions. Unilateralization gain is obtained by assuming perfect conjugate matching of both input and output ports. However, this might not be the case in reality. Secondly, the above *Y*-parameter of the amplifying stage is based on the small signal consideration whereas a PA generally deals with large signal. Due to these reasons, fine-tuning of feedback capacitors is needed to result in slightly smaller value than $C_{\mathrm{gd}} + C_{\mathrm{p1}}$.

It should be pointed out that the feedback capacitor value will impact directly on the effect of parasitic cancelling and impedance matching.

2.3 Discussion on Effects Brought by the Neutralization

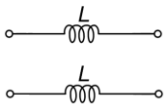
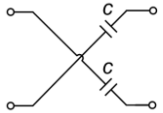
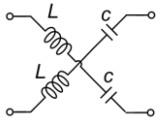
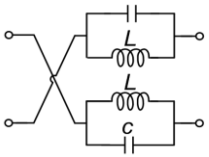
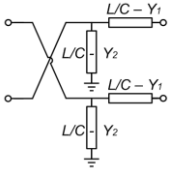
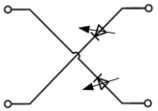
For the widely used common-source amplifying stages, the main reverse transferring coefficient is due to the parasitic capacitance between the drain and the gate. Y_{12}^{d} denotes the positive feedback from the drain to the gate, the main part of Y_{12}^{d} consists of C_{gd}.

Hence, $Y_{14}^{f} = j\omega C_{gd}$ (2.19)

From the derived general criterion, it is indicated that if the feedback network can satisfy equation (2.16), the differential amplifier is unilateralized. Based on the features in millimeter-wave integrated circuits, several typical and simple four-port feedback networks are summarized in TABLE 2.1. To simplify the derivation, lumped inductors are utilized to denote all possible

inductances in the theoretical derivation. The feedback networks A, B and C all lead to good neutralization and near-unilateralization. In these three networks, the absolute reverse isolation of network A only happens at the resonating frequency; meanwhile, network B can ideally work in the whole band. At millimeter-wave bands, connections may result in parasitic inductance. In the case of network C, $j\omega C/(1-\omega^2 CL)$ will modify Y_{14}. Therefore, ideal unilateralization cannot be achieved. However, as compared with network A and B, network C obtains 6 dB more isolation, wide bandwidth and a slightly lower gain than unilateral gain. Network D leads to the state of under-neutralization at which isolation and gain of the amplifier are all not high. Network E makes the amplifier over-neutralized and the high gain is achieved associated with low stability. Lastly, the aforementioned network F shows possibility for gain control of the amplifier.

TABLE 2.1: Comparison among Four-port Feedback Network Candidates
Simulated using 0.9 μm×64 μm CMOS for amplifier centered at 60 GHz

	A	B	C	D	E	F
Four-port feedback networks						
Feedback type	Parallel	Cross-coupled	Cross-coupled	Cross-coupled	Cross-coupled	Cross-coupled
Y_{14} of feedback network	0	$j\omega C$	$j\omega C/(1-\omega^2 CL)$	$j\omega C-j\cdot 1/(\omega L)$	$-Y_1$	$j\omega C_V$
3dB bandwidth*	Narrow	Whole band	Wide	Wide	None	Variable
Neutralization state	Unilateralized	Unilateralized	Under-neutralized	Under-neutralized	Over-neutralized	Variable
Peak gain [dB]*	13.1	13.2	12.6	6.4	NA	12.9
Reverse Isolation S_{12} [dB]*	-35	-35	-41	-30	NA	Variable
Features	Good unilateralization & narrow bandwidth	Ideal case	Unilateralization in a wide bandwidth, high isolation	Cancelling decided by capacitance and inductance	NA	Potential for variable gain amplifier

* Simulation of a two-stage millimeter-wave power amplifier with different four-port feedback networks, the architecture is shown is Figure 2.4.

Under unilateralization, the input and output impedances, and the gain can be fixed. This is because

$$\Gamma_{in} = S_{11} + \frac{S_{21}S_{12}\Gamma_L}{1 - S_{22}\Gamma_L} = S_{11} \tag{2.20}$$

$$\Gamma_{out} = S_{22} + \frac{S_{21}S_{12}\Gamma_S}{1 - S_{11}\Gamma_S} = S_{22} \tag{2.21}$$

Thus, matching impedance is more straightforward. As a consequence, isolated stages can be easily cascaded to achieve a high gain and stable amplifier.

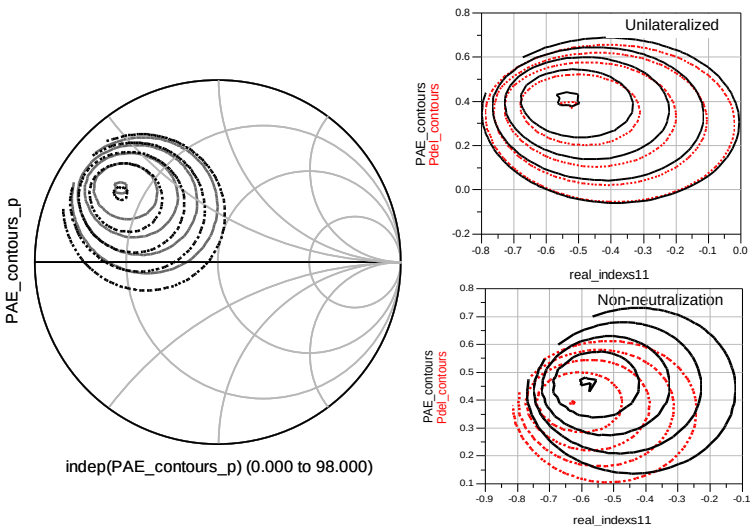


Figure 2.6: Power and PAE simulation of the differential amplifying pairs

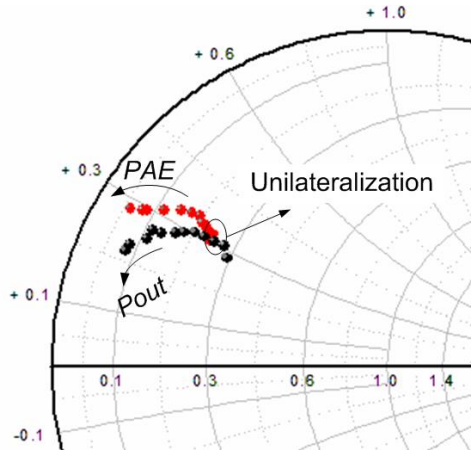


Figure 2.7: Simulated Pout and PAE matching impedance variation in Smith Chart when feedback capacitor varies from 0 *f*F, 8 *f*F, 16 *f*F, 24 *f*F, 32 *f*F, 40 *f*F, 48 *f*F, 51 *f*F, 65 *f*F, 80 *f*F, 95 *f*F to 110 *f*F.

Figure 2.6 shows the simulated power and PAE contours in the Smith chart. When the amplifier is unilateralized, the PAE and Pout matching contours almost overlap. More importantly, the maximum PAE and Pout coincide at the same point. On the other hand, the amplifying stage without unilateralization shows a different maximum matching point for power and PAE in the Smith chart. As an example for the latter case, by using an FET with a width of 64 μm and 1V power supply at the drain, the maximum PAE matching occurs at 12.1 + j16.5 Ω, whereas the maximum Pout matching is at 15.8 + j14.4 Ω. The achievable maximum PAE is 16.3% and the maximum Pout is 8.2 dBm. On the other hand, for the former case, the amplifying stage can achieve the maximum PAE of 18.5% and the maximum Pout of 8.9 dBm at the same matching point of 10.6 + j15 Ω. The power has been enhanced by 0.7 dB, while efficiency has been enhanced by 2.2%. Figure 2.7 shows the maximum PAE and Pout matching point change versus varying feedback capacitors. Similar to the analysis in [28], the matching impedance change can

be found through varying the feedback network. At the start point, the power and PAE matching point is separated. With increasing feedback capacitance, the maximum power matching point moves closer to PAE and finally coincides with it (with the exact unilateralization capacitance). After that, the amplifier enters into the over-neutralized region with the two curves breaking up. The only cross-point of the two curves is at the point of 24.9 *f*F which is approximately the unilateral capacitor needed in differential 64 μm FET pairs in this process. This indicates, with the intrinsic feedback in normal amplifiers, the maximum power matching point and the PAE matching point are different. By introducing unilateralization, simultaneous power and PAE matching is achieved along with power and PAE enhancement.

2.4 Implementation of Unilateralized 60 GHz PA in 90 nm CMOS

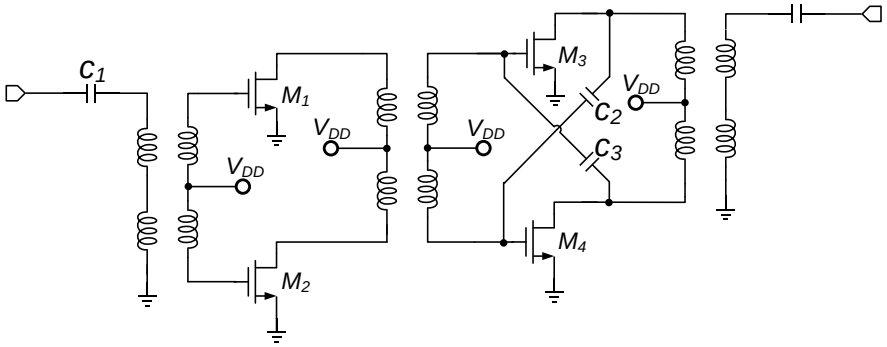


Figure 2.8: The proposed 60 GHz power amplifier in 90 nm CMOS technology

A transformer-based differential amplifier topology was chosen to verify the above analysis, due to the low supply voltage and advantages of differential architecture [29], [30]. As shown in Figure 2.8, based on the developed scalable transmission line models including inductor models and six-port transformer models [31], [32], a 60-GHz CMOS two-stage differential

PA was designed.

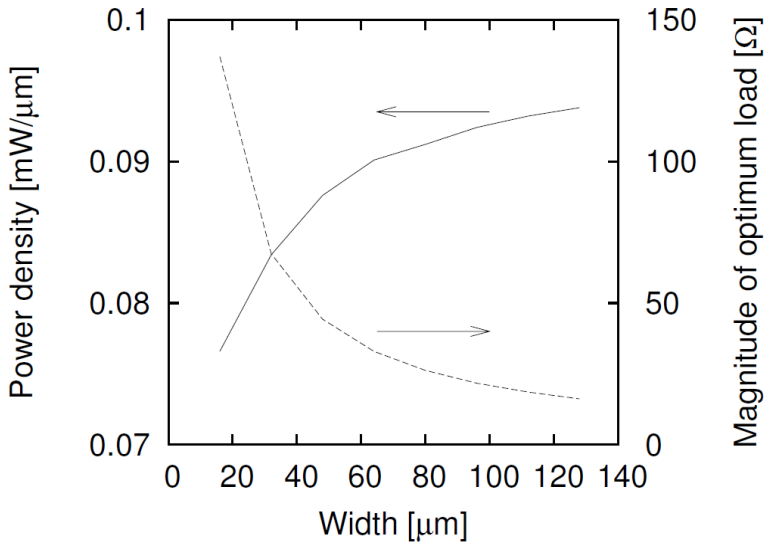


Figure 2.9: Simulated optimum 1-dB compressed output power density and corresponding optimum load impedance as a function of total device width

The amplifier was designed to operate below 1 V. This voltage is lower than the 1.2 V specified by the process in order to ensure reliability, as the signal swing at the FET terminals for class A can be as large as $2V_{DD}$. The power from the differential devices is combined and coupled to adjacent stages using 1:1 transformers. As the main task in this study is to investigate the unilateralization effect, only the pure cross-coupled capacitance feedback network is employed to verify its effectiveness. The modulation scheme is constant-envelope, so the amplifier can be driven into compression to maximize the power-added efficiency. The design starts from the critical final stage and progresses to the first stage.

The first step in the design was to determine the size of the output stage transistors to meet the output power requirement. Figure 2.9 shows that the

maximum OP1dB power density at 60 GHz for larger devices is around 0.09 mW/μm. This gives a simple rule-of-thumb for the required device size to meet certain OP1dB specification. For example, to achieve an output power of +10 dBm, the device will have to be significantly larger than this value to compensate for the wiring parasitics and the loss of the output matching network.

A 3 dB margin was considered based on a conservative estimate of the losses contributed by the output transformer and inter-connections. Therefore, each of the output transistors should be able to supply at least +7 dBm. This would require 56 μm FETs. To give some margins, 64 μm width devices were used. The next step in the design was to determine the first stage transistor sizes. In order to maximize efficiency, the output stage should compress before the input stage. Otherwise, the dominant current consumption of the output stage will be wasted if the input stage compresses first.

$$OP1dB_{stage2} < OP1dB_{stage1} + G_{stage2} \tag{2.22}$$

Assuming that the gain of the second stage is 6 dB, the first stage compression point should be more than the second stage compression point. To be conservative, the input stage is designed to have a 3 dB lower compression point than the output stage, which means the input transistors should be half the size of the output transistors since the OP1dB scales linearly with device size according to Figure 2.9. Thus, the first stage transistors are 32 μm wide.

The achievable output power of an amplifier is limited by the sizing of the final stage transistors. To determine the required device size to achieve the specified power level, a load pull simulation was done with swept device width and a 60 GHz input frequency. At each width, the load impedance was optimized to give the highest OP1dB. The simulation used 90nm NMOS devices with V_{GS} = V_{DS} = 1 V, which gave a current density close to 0.3 mA/μm. Figure 2.9 shows the optimized OP1dB power density and magnitude of the optimum load impedance. The magnitude of the drain voltage swing at OP1dB is relatively constant for different widths (between 0.6-0.7 V-peak) as it is limited by the supply voltage. The increase in power as a function of width comes from the increase in alternate current. This leads to a reduction of the optimum impedance as the inverse of the device width. For very large devices, the load impedance is very small, requiring a large transformation ratio to match to 50 Ω. This necessitates the use of power combining techniques for higher output powers.

Unilateralization capacitors between the adjacent gates and drains of the final stage transistors were added. These capacitors help to unilateralize the final stage, by partially cancelling of the gate-drain capacitors of the devices, thereby improving the stability of the stage as shown in Figure 2.10.

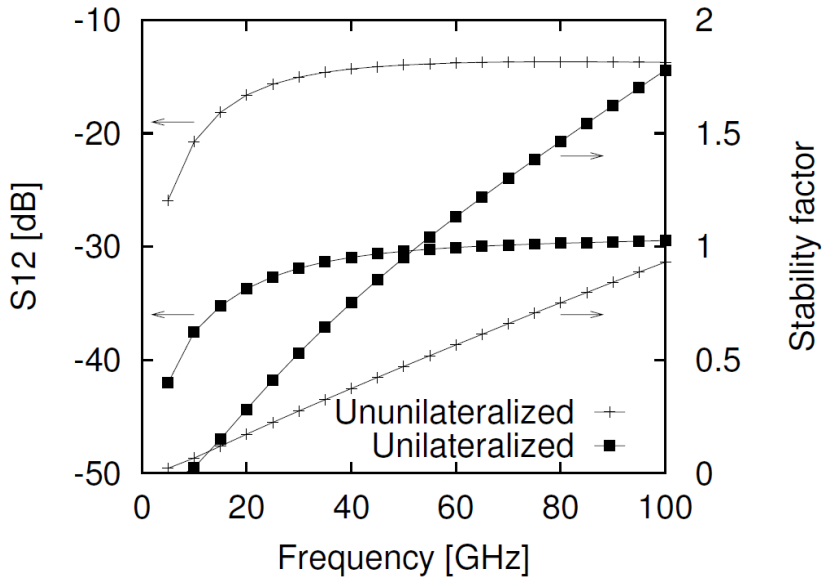


Figure 2.10: Simulated enhanced stability by the capacitive neutralization.

In the CMOS process, MOM capacitors with 2 *f*F/mm^2 can be used in the power amplifier design. Measurements have verified that the foundry models predict the performance of these capacitors very well up to at least 65 GHz. This is particularly important in this design, as capacitors are very small. For this process, C_{gd} of the FET we used is around 25 *f*F. Refer to Figure 2.5 (b), 64 μm width will result in 3.5 *f*F of C_{p1}. Therefore, C_f value which is slightly smaller than 28.5 *f*F is chosen.

The balun style transformer should be designed carefully. The ground parasitic impedance on the single-ended side of the balun has an effect on the voltage gain. To consider the severity of the effect, the voltage gain of the transformer is calculated with and without a ground parasitic when it is driving a 50 *f*F load. Without ground connection of the transformer to the nearest available ground in the layout, the voltage gain drops to −2.2 dB, corresponding to a loss of 1.7 dB. Such a loss can cause a significant drop in

power amplifier performance. Therefore, millimeter-wave component layouts using transformer baluns need to be very carefully designed to minimize these small, but critical parasitics. The balun should operate differentially and be insensitive to center-tap parasitics. Note that the analysis above assumed that there were no shunt admittances or coupling capacitances. Adding these capacitances complicates the analysis. However, for the 1:1 transformers that are typically used in millimeter-wave designs, with one turn on the metal layer directly above the other turn, the coupling capacitances can be very significant. Simulations show that adding these capacitances causes the outputs to be no longer differential. For example, simulations reveal that, a center-tap parasitic of only 15 pH can cause a 10-dB difference in the voltages at the output terminals of the transformer. In order to ensure differential operation and to maximize output power, it is thus also critical to minimize the parasitics to ensure the center-tap of the balun is grounded effectively.

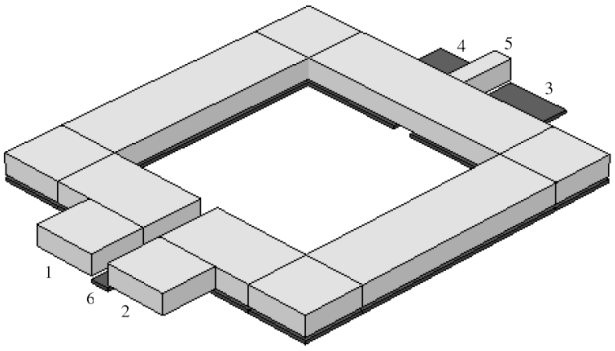
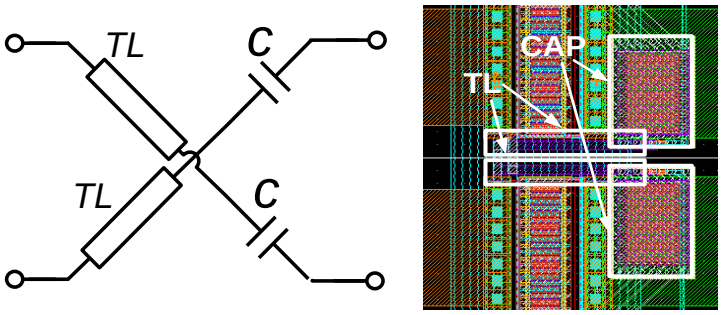


Figure 2.11: 3D model of the transformer

The output transformer is performing a single-ended to differential conversion, so the impedance looking into each of the differential inputs will

be lower than the load impedance of 50 Ω. A 1:1 transformer will allow the optimum load to be reached with minimal additional components. This optimum impedance could be realized using the series capacitor and a 55 μm diameter, 10 μm width, 1:1 transformer as shown in Figure 2.11. The inter-stage transformer diameter was designed to maximize the gain at 60 GHz by resonating with the device capacitances. The input transformer and capacitor C_1 were designed for a conjugate match to maximize the gain. The simulated peak gain is more than 14 dB at 61 GHz with a bandwidth of 6.6 GHz. The output 1 dB compression point is more than +7 dBm with a power consumption of 56 mW.

The interconnects between the transformers and ground, and particularly the parasitic interconnect to ground on the single-ended side of the input and output balun transformers, have very significant effect on gain, and also upsets the differential balance. Hence, a very careful layout design and post-layout verification should be conducted.



(a) (b)

Figure 2.12: Four-port feedback network and amplifying unit layout

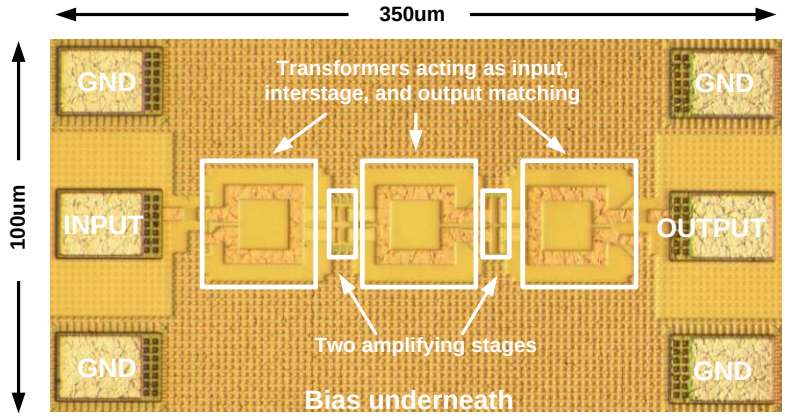


Figure 2.13: Die photograph of the 60 GHz Power amplifier on 90nm CMOS technology

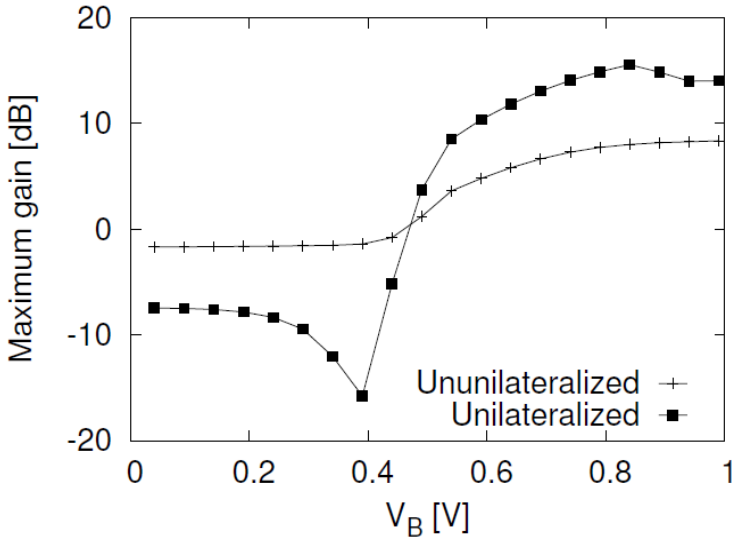


Figure 2.14: The amplifier changes from triode region to saturation region by changing V_B according to simulation.

The amplifier was fabricated in a 90-nm low leakage CMOS process. A photo of the chip is shown in Figure 2.13. The size of the circuit core is less than 350×100 μm^2. As shown in Figure 2.14, by changing the gate voltage V_b, the transistor operates from the triode region to the saturated region. This changes the differential amplifier operating from class B to class A. In order to get a high output power, this power amplifier still operates in class A

configuration. Thus, the value of C_f is related to the measured *Y*-parameter at the class A biasing condition. As can be seen from Figure 2.14, the amplifier is approaching maximum gain when V_B varies from 0 to 1 V.

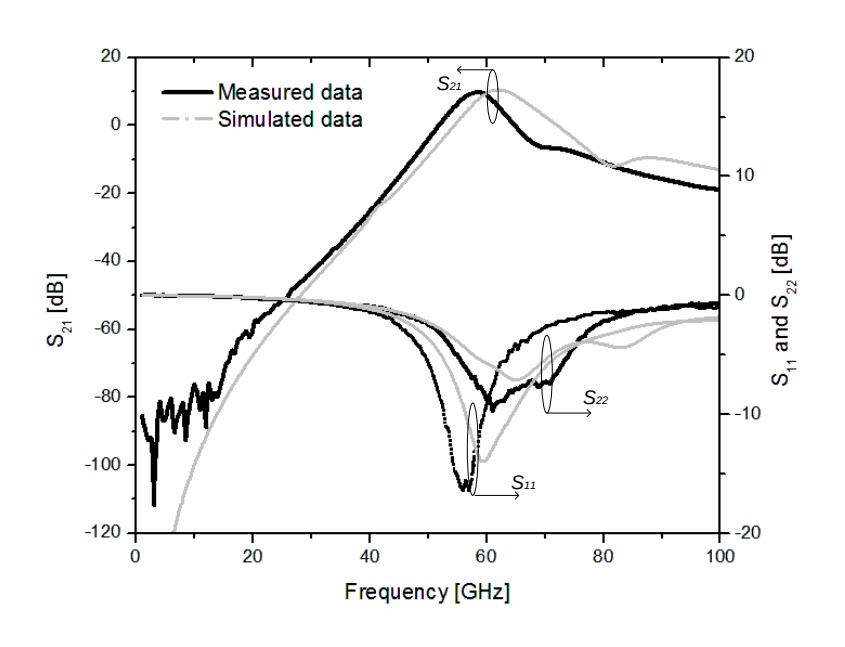


Figure 2.15: Measured S-parameters of the amplifier.

The S-parameters of the amplifier were also measured. This was performed using an Anritsu vector network analyzer, calibrated using the LRRM method from 1-100 GHz. Three randomly selected dies were measured, and the performance was consistent across three dies as shown in Figure 2.15. The frequency at which the gain peaks is around 58 GHz. The peak gain frequency varied less than 0.5 GHz (< 1%) across the three dies, and the peak gain varied less than 0.2 dB. This amplifier achieves high gain and efficiency with low power consumption using only two stages and operating below 1 V.

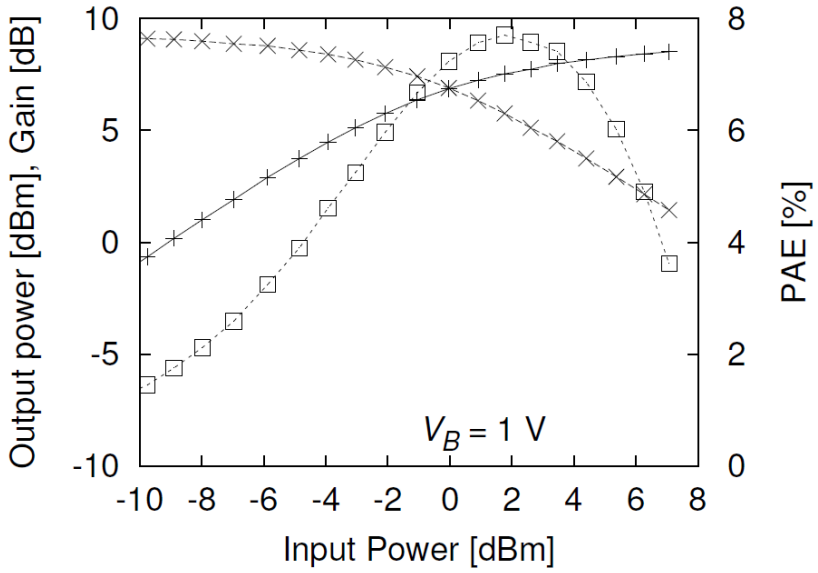


Figure 2.16: Measured gain, output power and efficiency of the amplifier

The power compression behaviour of the amplifier was tested across the different gain settings. The power loss of the input and output connections were removed, so the input power and output power were calibrated to the probe tips. Figure 2.16 shows the gain compression, output power and power added efficiency as a function of the input power. With VB = 1 V, the amplifier consumes 52 mW, and gives a saturated output power of +8.5 dBm, OP_{1dB} of +5.1 dBm and a peak PAE of 7.7 %. One remarkable aspect in the specification is the low power consumption which is only 52 mW. According to this feature, this differential amplifier architecture is suitable for the PA block implementation in low power 60 GHz transceiver systems [33].

According to the measured results, we may find that the advantage of unilateral networks is not only high gain stages, but also good isolated stages with high stability. Matching impedance is more independent of the influence introduced by source and drain impedance. These stages can be more easily

cascaded to achieve a high small signal gain and high stability amplifying block.

2.5 Conclusion

An analysis of the high-frequency differential amplifier design by using a four-port feedback has been proposed in this chapter. The criterion for archiving the unilateralization of a differential amplifier has been derived. Meanwhile, the benefits of an amplifier using unilateralized stages are discussed, such as higher gain, higher stability, great possibility for gain control and independence of matching networks. Based on this analysis, a 60-GHz power amplifier for short range communications has been designed and fabricated in the 90 nm CMOS technology. The two-stage amplifier has a gain of 10 dB, with a center frequency of 58.5 GHz and a bandwidth of 6.3 GHz. In the maximum gain state, the output 1dB compression point is +5.1 dBm, P_{sat} is +8.5 dBm and the peak PAE is 7.7 %, drawing 53 mA from a 1 V supply.

CHAPTER 3

Band Tunable 60 GHz Power Amplifier

For a millimeter-wave integrated amplifier design, the gain and efficiency, which have been limited by the low supply voltage of submicron CMOS processes [19], have gradually been increased using new design techniques [6], [7], [34]. To obtain high output power, the distributed-active-transformer (DAT) based CMOS power amplifier (PA) combines multiple power-units and new output power records have been achieved [35]-[37]. However, due to the losses associated with power splitting and combining in passive elements, the efficiency suffers. Besides the high power PAs, "small" and efficient PAs have been developed for millimeter-wave beam-forming radio systems [19] and indoor short range communications with a 10 dBm output power requirement [38]. A recent design [11] has achieved a 26% PAE under a 1.7 V supply using an SOI CMOS process. However, if this amplifier is biased under near 1.0 V supply, the efficiency might be lower. Differential transformer-coupled amplifiers have the potential to balance output power and efficiency requirements, as transformers are used for both impedance matching and power combining networks. Some reported transformer-coupled designs [8]-

[10] have achieved reasonable PAE and an output power of more than 10 dBm. However, it is difficult to achieve sufficient performance over the required 7 GHz bandwidth. According to the millimeter-wave physical layer (PHY) specification in IEEE 802.15.3c, four channels constitute the whole 60 GHz band, as shown in Figure 3.1.

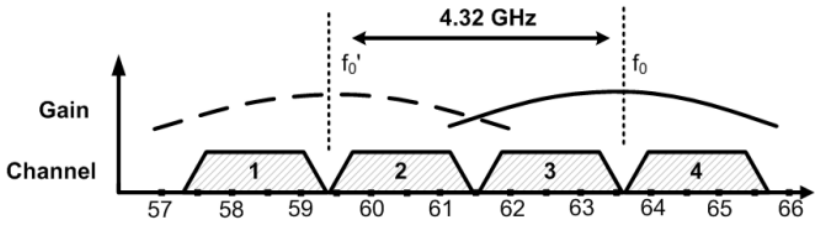


Figure 3.1: 60 GHz WPAN channels based on IEEE Standard 802.15.3c.

This standard specifies four frequency channels each with bandwidth of 2.160 GHz and a symbol rate of 1.728 Giga-symbols/second. Hence, band-tunable circuit can be employed for different channels while high gain and high efficiency in a narrow bandwidth through high-Q matching and deep-neutralization. The design approach can be simpler compared to the wide band design approach. A band-tunable power amplifier on 65 nm CMOS technology is thus proposed. This amplifier shows an ability to change the peak gain from 59.0 GHz to 53.5 GHz. The maximum output power is 12.3 dBm in the high frequency band. The peak PAE is 20.4 % with a 17.1 dB gain, and 17.2% with a 16.2 dB gain, for the high frequency band and low frequency band, respectively.

3.1 Switching Details and Band Tuning Mechanism

In order to cover the 7 GHz band around 60 GHz, a narrowband power amplifier is designed with a band-tunable circuit on the input. Therefore, by peaking gain at two different frequencies with an interval of approximately 4.3 GHz, high gain performance can be achieved in the whole band. By employing a high-Q band-switching circuit in the input matching network of the amplifier, as shown in Figure 3.2, the band can be tuned from a default frequency band to a lower frequency band. Similar switching circuit has been employed in voltage controlled oscillators (VCO) [39].

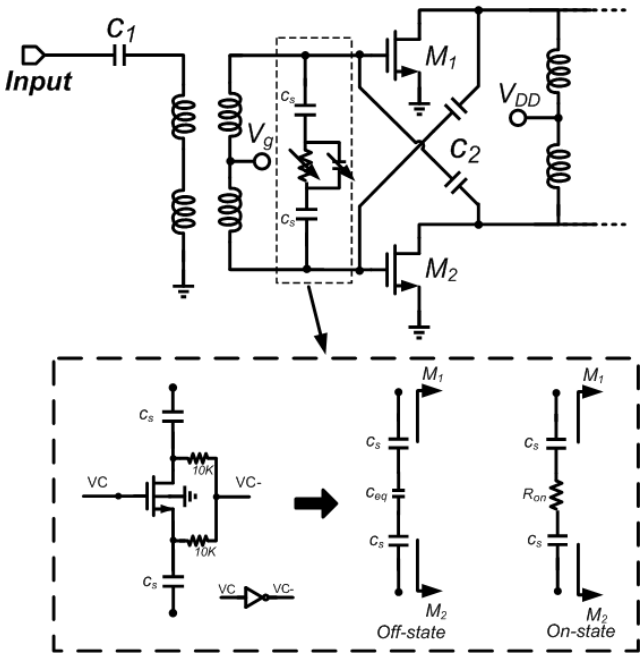
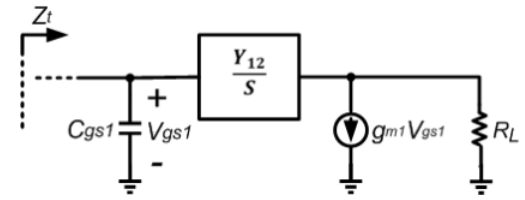


Figure 3.2: Input matching network of the 1st stage of the amplifier and the equivalent circuit of the differential switch operating in the off-state and on-state.

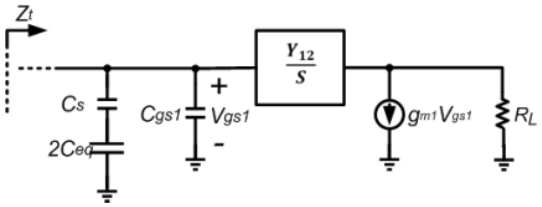
The prerequisite of using this switching circuit in power amplifier design is that high isolation between the drain and gate of the amplifying transistor is needed. Any input impedance change may cause instability and a shift in the

power matching impedance at the output. Hence, deeply-neutralized differential pairs are used for the amplifying stages to provide high isolation from output to input. As will be shown in Section 3.2, the level of neutralization has a significant effect on the amplifier's gain and bandwidth.

As shown in Figure 3.2, with a band-switching circuit connected between the gates of M1 and M2, the input impedance of the amplifier is varied as the switch turns on or off. Due to the shared turn-on resistance between the differential signal paths, only half the turn-on resistance is accounted in the matching network of each differential path. This minimizes the insertion loss and matching loss of the input matching network. For the two states of the switch in millimeter-wave frequency bands, the switching CMOS FET can be regarded as a capacitance in the off-state and a turn-on resistor in the on-state. As the two states contribute different capacitance values to the total capacitance between gate and source, the input matching frequency can be tuned by the switch.



(a)



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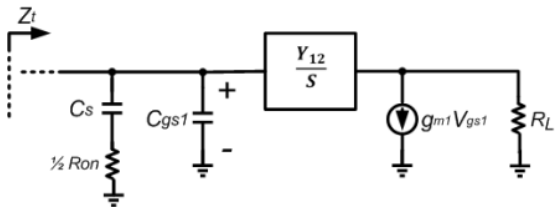


(c)

Figure 3.3: Equivalent circuit for single-ended path in the differential amplifier: (a) Amplifier without tuning switch, (b) Amplifier with tuning switch in the off-state, (c) Amplifier with tuning switch in the on-state.

TABLE 3.1: Design Values of the Input Matching Part

M_1	I_{dc}	M_{switch}	C_1	C_2	$L_{S\text{-}equivalent}$ *
60nm×96µm	3 mA	60nm×24µm	34 *f*F	27.4 *f*F	120 pH

* Equivalent inductance of half-length secondary transformer

TABLE 3.1 lists all the element values of the switching circuit used in this design. The voltage controlled switching circuit is implemented on-chip. Controlling voltage values are 0 and 1 for off and on states respectively. The amplifier needs approximately 0.5 ns for settling down after switching. With about 300 µA/µm current density in the second stage and 30 µA/µm in the first stage, the gate-source capacitance of the first stage FETs is 57.7 *f*F (the dimension of the first stage FETs is: length: 60 nm, width: 12 × 8 µm). The inductance of each side of the input matching transformer is approximately 120 pH ($0.5 \cdot L_S$ or $0.5 \cdot L_p$). As shown in the equivalent circuit in Figure 3.3(b) and Figure 3.3(c), the switch in the off-state and on-state can be approximated by an equivalent capacitor and a turn-on resistor, respectively. By choosing this switch with a dimension of length: 60 nm, width: 2 µm × 12, the equivalent capacitance of the switch at the off-state is 9.2 *f*F. At the on state, R_{on} equals 123.93 Ω. Thus, in the off-state, the equivalent shunt capacitance

connected to the gate is approximately equal to 12 *f*F. On the other hand, the equivalent circuit of the switch in the on-state can be regarded as a resistance with a value of $0.5 \cdot R_{on}$, which is 62 Ω in series with a 34 *f*F capacitor.

The band-tuning mechanism of the transformer matching is derived numerically as follows. The network between the drain and gate is represented by the *Y*-matrix shown in Figure 3.3. Based on the *Y*-matrix analysis in [40], at the condition of unilateralization, $Y_{12} = 0$. In order to derive the change in the matching frequencies (ignoring minor parasitic effects), the impedances looking into the gate of transistors (M1 or M2) are derived as follows. For the default amplifier without the switch connected between the FET's gates:

$$(Z_t)_d = (1 + R_L Y_{12}) / \{[1 + (sC_{gs} + g_m)R_L]Y_{12} + sC_{gs}\} \tag{3.1}$$

At the state of unilateralization, the input impedance Z_t is simplified to:

$$(Z_t)_d = 1/(sC_{gs}) \tag{3.2}$$

Then, for the tunable amplifier with the switch in the off-state:

$$(Z_t)_{off} = 1/\left[\frac{(1 + g_m R_L)Y_{12}}{Y_{12}R_L + 1} + sC_{gs} + \frac{2 \cdot sC_s \cdot C_{eq}}{2C_{eq} + C_s}\right] \tag{3.3}$$

When unilateralization is applied in the off-state, the impedance Z_t is simplified as follows:

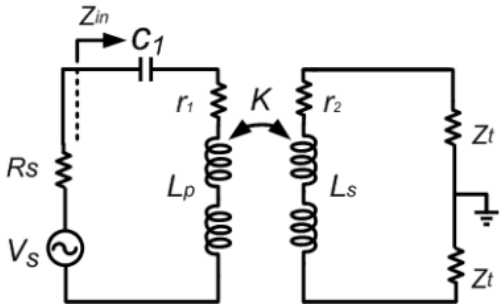
$$(Z_t)_{off-u} = 1/\left[sC_{gs} + \frac{2 \cdot sC_s \cdot C_{eq}}{2C_{eq} + C_s}\right] \tag{3.4}$$

Lastly, for the tunable amplifier with the switch in the on-state, the impedance Z_t can be presented as:

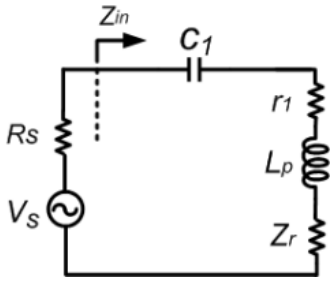
$$(Z_t)_{on} = 1/\left[\frac{(1+g_m R_L)Y_{12}}{Y_{12}R_L+1} + sC_{gs} + \frac{2\cdot sC_s}{2+sC_s R_{on}}\right] \tag{3.5}$$

When unilateralization is applied in the on-state, the impedance Z_t is simplified to:

$$(Z_t)_{on-u} = 1/\left[sC_{gs} + \frac{2\cdot sC_s}{2+sC_s R_{on}}\right] \tag{3.6}$$



(a)



(b)

Figure 3.4: Equivalent circuit of the transformer based input matching network: (a) Input matching network with transformer coupling, (b) Equivalent input matching circuit.

In Figure 3.4, r_1 and r_2 represent the conductor losses of the primary and

secondary inductors. The induced current flowing in the secondary inductor imposes a counter electromotive force on the primary inductor. This effect can be accounted for by adding a reflected impedance Z_r in series with the impedance of the primary circuit [41]. Z_r can be expressed in terms of the mutual inductance and the series impedance of the secondary circuit as:

$$Z_r = (\omega M)^2 / (2Z_t + sL_s + r_2) \tag{3.7}$$

Where $M = k\sqrt{L_1 \cdot L_2}$.

Therefore,

$$Z_{in} = 1/sC_1 + sL_p + Z_r + r_1 \tag{3.8}$$

$$|S_{11}| = \left| \frac{Z_{in} - Z_o}{Z_{in} + Z_o} \right| \tag{3.9}$$

$$20\log|S_{11}| = 20\log \left| \frac{\frac{1}{sC_1} + sL_p + r_1 + \frac{(\omega M)^2}{2Z_t + sL_s + r_2} - Z_o}{\frac{1}{sC_1} + sL_p + r_1 + \frac{(\omega M)^2}{2Z_t + sL_s + r_2} - Z_o} \right| \tag{3.10}$$

When $Z_{in} = Z_o$, the input port is ideally matched. Hence, the following equation needs to be satisfied:

$$r_1 + \frac{1}{sC_1} + sL_p + \frac{s^2 k_1^2 L_1^2}{2Z_t + sL_1 + r_2} = Z_o \tag{3.11}$$

Theoretically, the matching frequency can be derived from the above equations. However, a more intuitive way to find the resonant frequency is to

make $2Z_t$ resonate with sL_1 while C_1 resonates with L_p. Good matching can be achieved under this condition. This method is also described in [42].

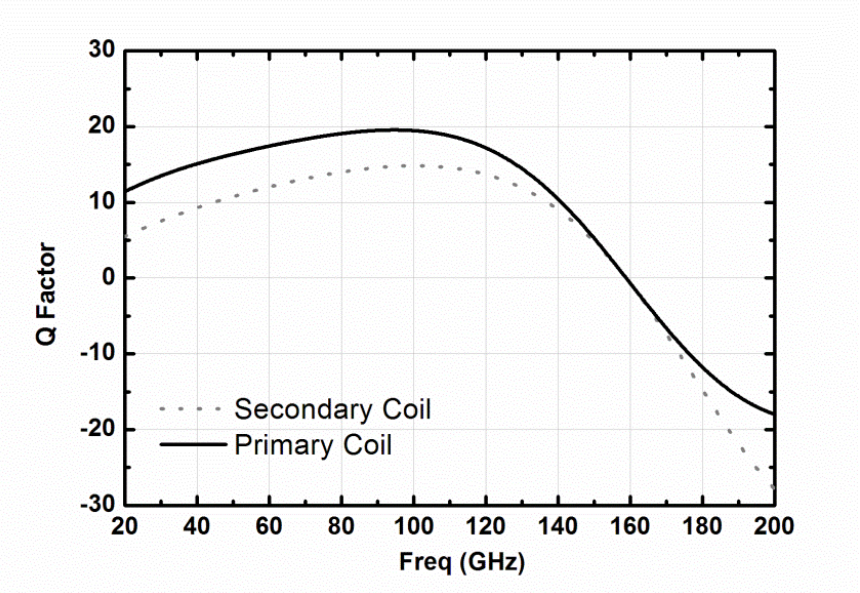
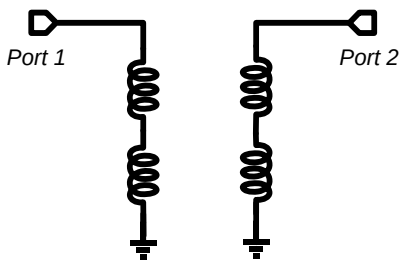
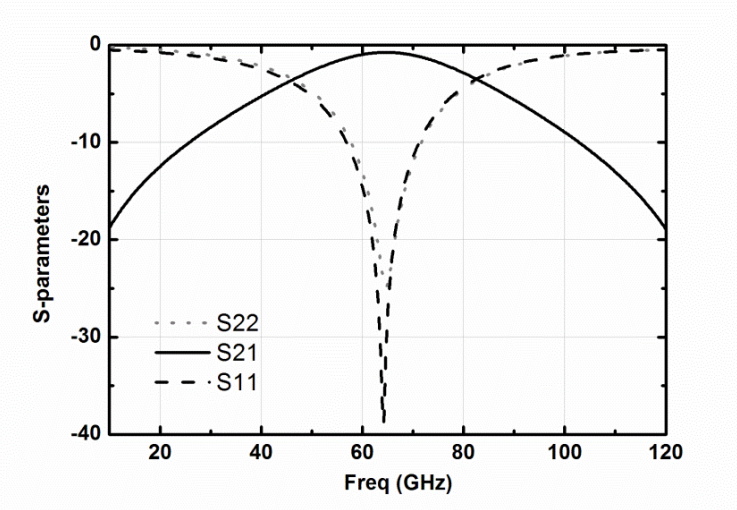


Figure 3.5: The Q-factor of primary and secondary coils in the transformer

Figure 3.5 shows the Q-factor of the transformer with a diameter of 43 μm in our design. At 60 GHz, the Q-factors of the primary coil and secondary coil are around 17 and 12, respectively. For the primary coil in our design, we use the top metal with a thickness of 3 μm. Meanwhile, for the secondary coil, the metal thickness is only 1.2 μm. Hence, the Q-factor is much smaller than the previous one due to its much thinner metal layer.



(a)



(b)

Figure 3.6: S-parameter of the transformer in inverting configuration: (a) port setup; (b) Simulated S-parameters.

Figure 3.6 shows the transformer performance (inversely connected). The insertion loss of the transformer is -0.76 dB and the coupling co-efficient is 0.85.

3.2 Effects of Tunability on the Bandwidth, Gain and PAE

In [43], the 7 GHz unlicensed band in IEEE 802.15.3c was fully covered by a 3-stage PA through systematically shifting the peaking frequency of each of the matching networks. However, the large bandwidth is obtained by sacrificing gain. Generally speaking, tapered resonant frequency peaking and reducing the Q-factor of the matching networks can both result in a wide bandwidth. In this work, with the band-tunable circuit described above, the bandwidth requirement is relaxed. In contrast to seeking a wide bandwidth design, the PA performance over a narrow bandwidth can be optimized.

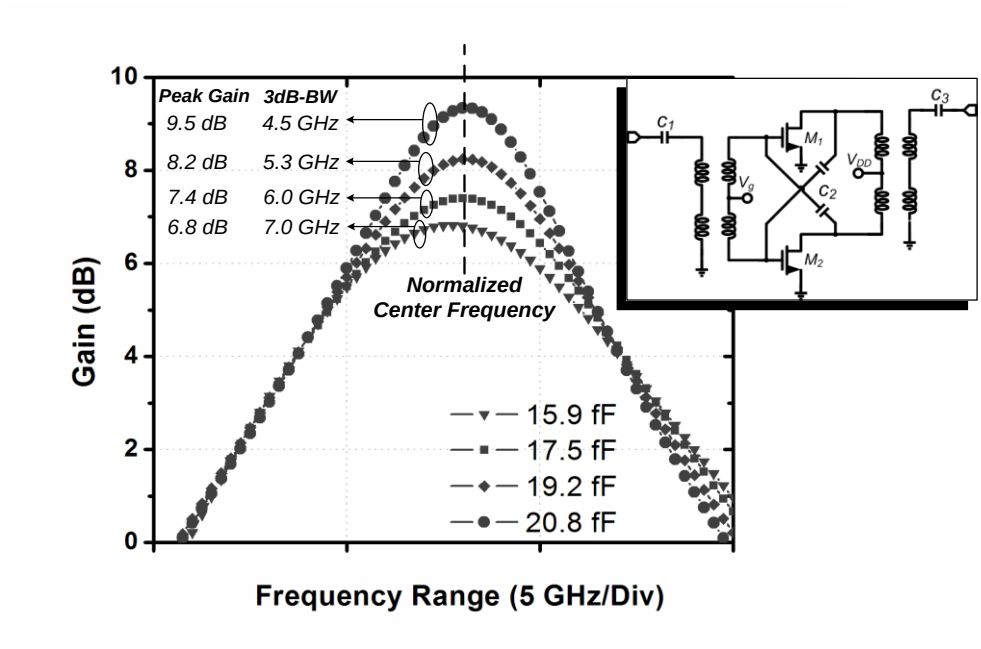


Figure 3.7: Gain and bandwidth varies with unilateralized capacitors of a single stage differential amplifier. The insert is the one-stage neutralized power amplifier schematic.

As unilateralization techniques [41], [44] cancel the reverse feedback through the FETs, they can provide maximum gain with the highest stability (highest reverse isolation) simultaneously. MOS capacitors feedback [45] can carry out accurate neutralization. However, layout parasitics due to large device size in this design may deteriorate gain and stability. Thus, cross-coupled capacitors are used for neutralization due to its simpler layout design. By increasing the value of the neutralization capacitor C_2 in Figure 3.2, the status can vary from weak-neutralization to intermediate-neutralization, then unilateralization and finally over-neutralization. Usually, the over-neutralization case should be avoided as it will cause instability. The former three cases are useful and have different gain and bandwidth performance. To clearly demonstrate the effectiveness of unilateralization, the gain and

bandwidth of one-stage transformer-coupled differential amplifier is simulated with various values of C_2. The amplifying transistors have a length of 60 nm, and a width of 48 m. The current density is around 300 µA/µm and the capacitances between drain and gate of M_1 and M_2 are approximately 23.4 *f*F. Thus, the values of C_2 and C_3 are related to the measured *Y*-parameter in the class A biasing condition. To prevent over-neutralization, we make sure the feedback capacitor values are smaller than the above value. The simulated gain variation with four different neutralization capacitors values are shown in Figure 3.7. As can be seen, the phenomenon brought by neutralization capacitors to the differential pair is somewhat like the "Q-factor" characteristics of passive circuits. Higher peak gain is accompanied with lower bandwidth and vice versa. Thus, by driving the differential pair into deep-neutralization, the amplifier can obtain the highest gain with the narrowest bandwidth.

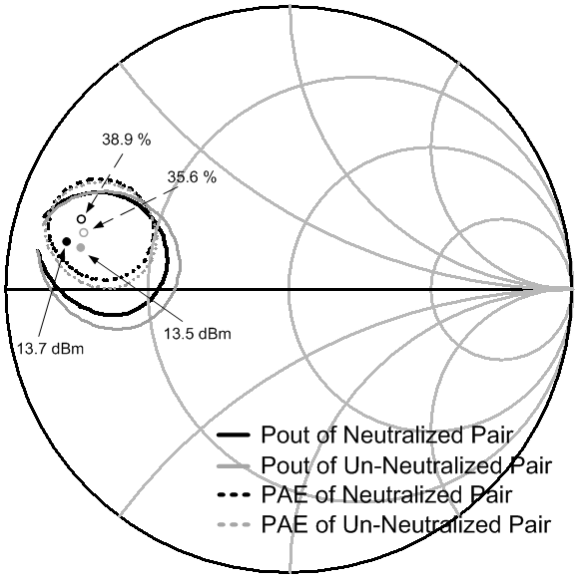


Figure 3.8: Comparison of simulated load-pull results for amplifiers with and without neutralization at 60 GHz.

Deep neutralization has additional benefits, due to its high isolation between drain and gate of the MOSFETs. An impedance change caused by switching in the input network will not affect the matching of the following stages. In particular, the output power matching impedance is almost the same before and after band switching. Instability in different impedance states can be prevented. Also, by load-pull simulation similar to [10], the neutralized pairs can have higher maximum output power (peaking difference is 0.2 dB) and PAE (peaking difference is 3.3%) compared to normal differential pairs as shown in Figure 3.8; Therefore, if the MOSFETs are set in deep-neutralization and high-Q matching networks are used, together with all the matching networks peaking at the same frequency, the resultant power gain and PAE at this frequency can be optimized.

For multistage PA design, gain and efficiency will behave interactively on the overall efficiency [46]. With matching peaking at the same frequency, to obtain the same gain as normal wideband amplifiers, the current consumption can be reduced. Also, for a given transistor size, lower current leads to a lower knee voltage which can also help improve the overall efficiency for low voltage supply design.

3.3 Analysis of Power Gain and Group Delay Uniformity

3.3.1 Analysis of Power Gain Uniformity

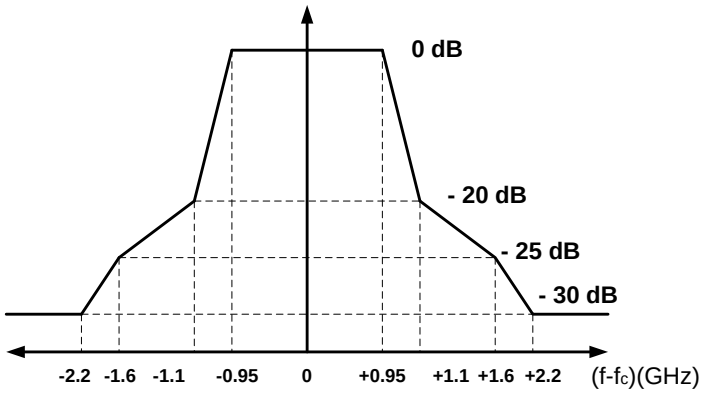


Figure 3.9: Transmit spectral mask in 802.15.3c-2009

According to IEEE Standard 802.15.3c-2009, the transmit spectral mask is shown in Figure 3.9. The transmitter emissions are required to meet the spectral mask shown in Figure 3.9. This suggests a sharp frequency peaking satisfy this PSD mask better. The maximum allowable output power, as measured in accordance with practices specified by the appropriate regulatory bodies, is shown in [38] (Page 59 in the standard doc). Meanwhile, TABLE 3.2 demonstrated the power limit and equivalent isotropic radiated power (EIRP) for three different geographical regions.

TABLE 3.2: Maximum Transmit Power Levels in Selected Geographical Regions

Geographical Region	Power Limit	EIRP Limit	Regulatory Document
USA	–	Maximum indoor EIRP: 27 dBm Maximum outdoor EIRP: 40 dBm	47 CFR 15.255
Japan	Maximum output power: 10 dBm	Maximum EIRP: 57 dBm	ARIB STD-T69 ARIB STD-T74
Australia	Maximum output power: 10 dBm	Maximum EIRP: 51.8 dBm	Radio communications Class License 2000

The maximum output power into the antenna is defined for selected geographical regions. Besides these, a recent work [47] concerning 60 GHz phased array system has also shown un-equalized gain for the different four channels where the EVM for the receiver is about -18 dB. The influence on system caused by un-equalized gain is analyzed as follows.

For the gain fluctuation issue, we have conducted a calculation to show the un-equalized gain's impact from a system perspective. The relation between received signal strength and gain fluctuation over the 60 GHz band is quantified.

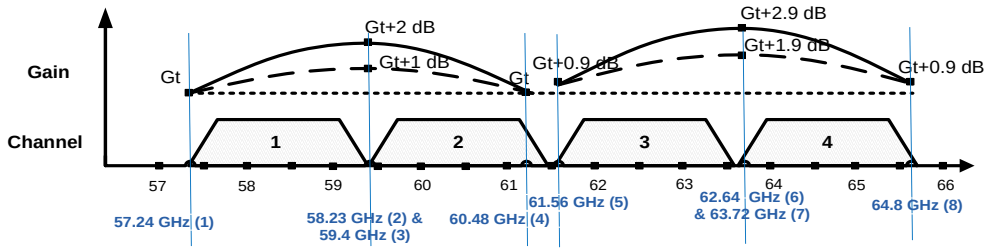


Figure 3.10: Gain of the 60 GHz band-tunable PA corresponding to different channels

As shown in Figure 3.10, if we define the channel borders' frequency (dotted lines) and gain as above, we may calculate the coverage range for the three gain cases: the amplifier has a constant gain of G_t; the amplifier has a distributed gain with 1 dB gain peaking in each tuned band; and the amplifier has a gain with 2 dB gain peaking for each tuned band. Assuming that the coverage range is 10 meters for the band edge, 57.24 GHz, at which the amplifier has a gain of G_t. Based on the Friis propagation rule, the coverage range for the above three gain cases are listed in TABLE 3.3 to TABLE 3.5.

TABLE 3.3: Coverage Range of Tx with Constant Gain (Gt)

Border Num	Freq (GHz)	Gain	Range (Meter)
1	57.24	Gt	10.0
2	58.23	Gt	9.6
3	59.40	Gt	9.3
4	60.64	Gt	9.0
5	61.56	Gt	8.7
6	62.64	Gt	8.4
7	63.72	Gt	8.1
8	64.80	Gt	7.8

TABLE 3.4: Coverage Range with Constant Gain with 1dB Peaking (G_t+1dB)

Border Num	Freq (GHz)	Gain	Range (Meter)
1	57.24	Gt	10.0
2	58.23	Gt+1dB	12.1
3	59.40	Gt+1dB	11.7
4	60.64	Gt	9.0
5	61.56	Gt+0.9dB	10.6
6	62.64	Gt+1.9dB	12.9
7	63.72	Gt+1.9dB	12.5
8	64.80	Gt+0.9dB	10.0

TABLE 3.5: Coverage Range with Constant Gain with 2dB Peaking (G_t+2dB)

Border Num	Freq (GHz)	Gain	Range (Meter)
1	57.24	Gt	10.0
2	58.23	Gt+2dB	15.3
3	59.40	Gt+2dB	14.7
4	60.64	Gt	9.0
5	61.56	Gt+0.9dB	10.6
6	62.64	Gt+2.9dB	16.3
7	63.72	Gt+2.9dB	15.7
8	64.80	Gt+0.9dB	10.0

As shown in TABLE 3.3, if the gain is constant in the whole 7 GHz unlicensed band, the coverage range differs from 10 meters to 7.8 meters as frequency increases. Meanwhile, as depicted in TABLE 3.5, if the gain fluctuation is 2 dB and with a 0.9 dB difference between upper and lower bands, the coverage range can go down to the lowest value of 9 meters and increases to the highest value of 16.3 meters. If this gain fluctuation is less than 1 dB (0.9 dB), the coverage range has comparable coverage range

flatness as the constant gain case. Thus, if a single tuned-band has wider bandwidth or achieves a gain fluctuation smaller than 1 dB, it may have comparable distortion in comparison with an ideal constant gain case as shown in TABLE 3.3.

Admittedly, if the gain variation of the amplifier can be reduced to 1 dB, the distortion can be further reduced. To alleviate this amplitude distortion issue in the 60 GHz system, a smaller neutralized capacitor can be used to trade for a flatter and smaller gain. Meanwhile, a slightly more DC power can be provided to compensate this reduced gain while sacrificing PAE at the same time.

3.3.2 Analysis of Group Delay

For group delay in amplifiers, it is indicated in [48] that it is impossible for a network of finite order to provide a constant time delay over an infinite bandwidth and all we can do is to provide an approximation to a constant delay over some finite bandwidth.

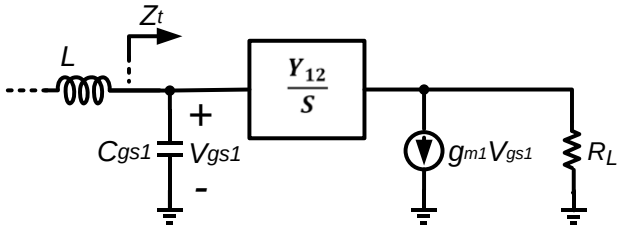


Figure 3.11: Small-signal model of the amplifier for analysis of group delay variation

For the differential amplifier, we may sketch the equivalent circuit of a single branch as shown in Figure 3.11.

According to (3.1),

$$A_V(s) = H_1(s) \times H_2(s) = \frac{Z_t}{sL + Z_t}\left(\frac{1 - g_m Z_F}{Z_F}\right) \; Z_L \parallel Z_F \tag{3.12}$$

It should be noted that the group delay is derived from the phase of the transfer function. Therefore, any resonance in the signal path will contribute to the distortion in group delay. The critical part for group delay variation comes from H_1(s), and H_1(s) can be approximated as:

$$H_1(s) = \frac{Z_t}{sL + Z_t} = 1 / \left(\frac{s^2}{1/(LC_{gs})} + \frac{s}{\frac{(1 + R_L Y_{12})}{LY_{12}(1 + g_m R_L)}} + 1 \right) \tag{3.13}$$

The equation is similar to that of a second-order low pass filter transfer function whose group delay variation depends on the resonating frequency, $\omega_{0,}$ and the quality factor, Q_0 [48]. They can be derived as:

$$\omega_0 = \sqrt{\frac{1}{LC_{gs}}}$$

$$Q_0 = \frac{1 + R_L Y_{12}}{LY_{12}(1 + g_m R_L)} \sqrt{LC_{gs}} = \frac{1/Y_{12} + R_L}{1 + g_m R_L} \sqrt{\frac{C_{gs}}{L}} \tag{3.14}$$

Therefore, the group delay expression of the circuit is:

$$\tau_{gr} = \frac{1}{\omega_0 Q_0}\left[\frac{1 + (\omega/\omega_0)^2}{1 - (\omega/\omega_0)^2 (2 - 1/Q_0)^2 + (\omega/\omega_0)^4}\right] \tag{3.15}$$

If Q_0 is bigger than 0.577, the denominator has two poles in the imaginary part, which results in a group delay peaking.

$$\tau_{gr} \approx \frac{1}{\omega_0 Q_0} = \frac{1}{L}\frac{1/Y_{12} + R_L}{1 + g_m R_L} \tag{3.16}$$

As shown in (3.16), a smaller feedback capacitor along with sharp peaking corresponds to a higher group delay. Meanwhile, group delay variation can be minimized by increasing ω_0 or decreasing Q_0. However, this effect may require increased equalization in the receiver. As shown in the τ_{gr} expression, the group delay peaking is also related to L, g_m and R_L. The peaking can be moved to higher frequency until it is outside the required bandwidth so that a lower fluctuation in group delay can be obtained at the applied frequency. Hence, if the inductance is chosen properly, it can help alleviate the distortion and obtain compromised performance between gain peaking and distortion. Figure 3.12 verifies the above analysis through simulation. It demonstrates that the group delay can vary with transformer's diameter. The 3D model of the transformer is similar as the model demonstrated in Figure 2.12. The slight difference is that metal thickness and height are changed.

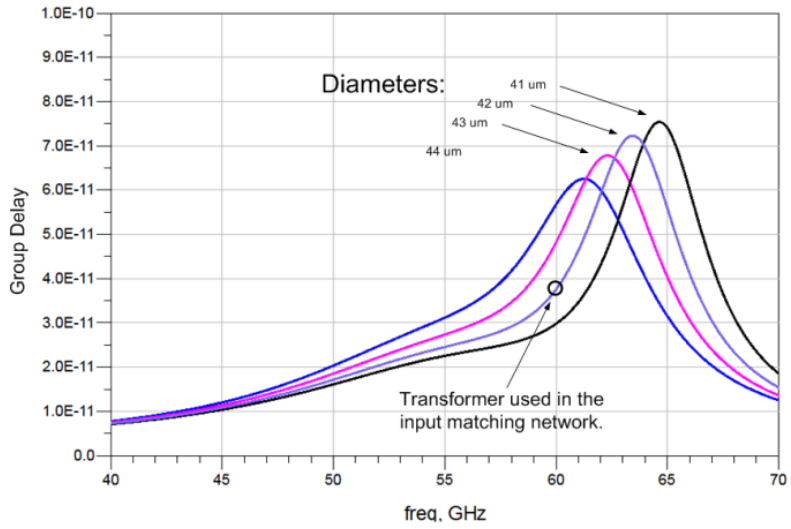


Figure 3.12: Simulated group delay varies with transformer's diameters

3.4 Power Amplifier Implementation

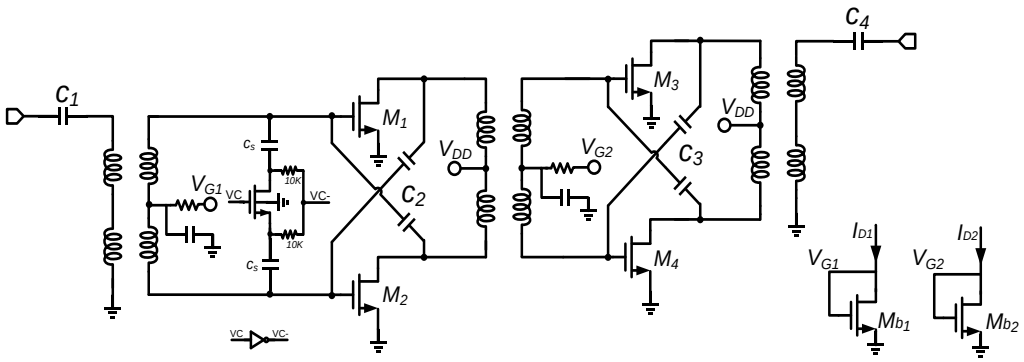


Figure 3.13: Two stage band-tunable 60 GHz differential amplifier schematic. The band-switching circuit is indicated in the input matching network of the first stage.

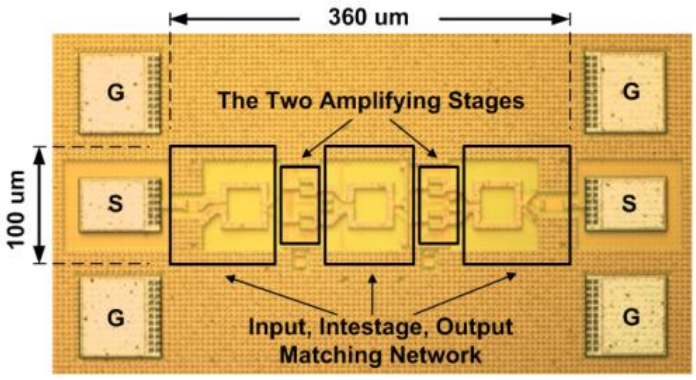


Figure 3.14: Die micrograph. The core area size is 360 μm × 100 μm.

Figure 3.13 shows the two-stage power amplifier with a differential switch in the input matching network. In the two-stage design, unit gate widths of 2 μm are chosen to ensure highest gain at 60 GHz. Total width of 96 μm and 300 μA/μm current density are designed to ensure power density and gain. The first stage's size is chosen after considering tuning effect and gain. Transformers are used for inter-stage matching, input and output baluns and power supply from the center-taps. The neutralization technique is used in both the first and second stage differential MOSFET pairs. The amplifier is fabricated in UMC 65 nm standard 1P10M CMOS process. A micrograph of the chip is shown in Figure 3.14. The size of the circuit core is less than 360 × 100 μm^2.

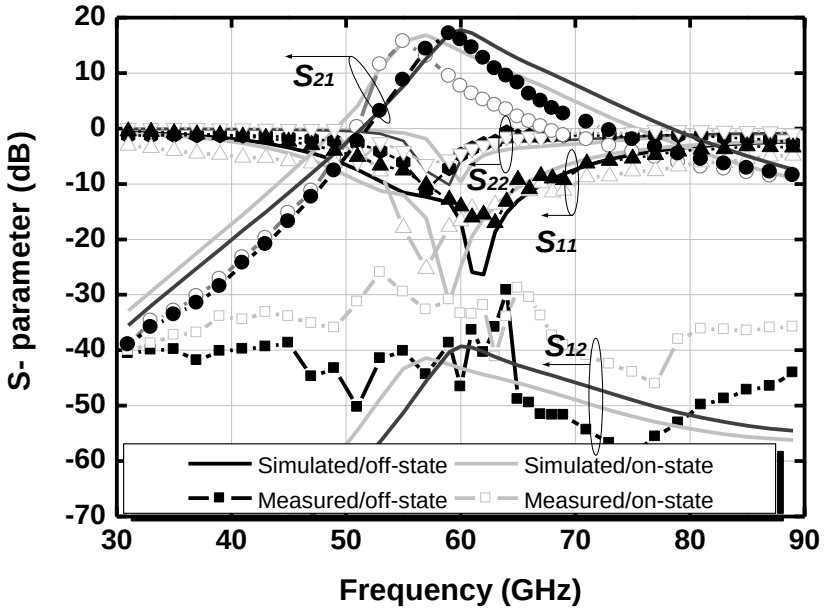


Figure 3.15: Measured S-parameter of the band-switching PA. The biasing condition is 1 Volt supply and 63 mA.

An Anritsu vector network analyzer is calibrated using the LRRM method from 30-90 GHz. The measured S-parameters are shown in Figure 3.15. The amplifier shows a capability to shift from a higher center frequency to a lower center frequency. The peak gain of 17.1 dB occurs at 59 GHz, with the switch in the off state. In the on state, the peak gain is 16.2 dB at 53.5 GHz. The combined 3-dB bandwidth is extended to more than 9 GHz. Some un-expected frequency shift happens in the whole frequency band, which may be due to un-accounted parasitic effects on the bends of connections and parasitics on the transistor feedlines. Also, there is about a 0.7 dB difference in the small signal gain S_{21} between the post-layout simulation and measurement. This may be due to metal and substrate losses not accounted entirely in the simulation. The lowest K factors are about 1.5 (on-state) and 2 (off-state) around the 60 GHz

band due to the sensitive ground tracing of transformer and layout dependent reverse isolation. As can be seen in Figure 3.15, reverse isolation is typically better than 30 dB in both the off-state and on-state.

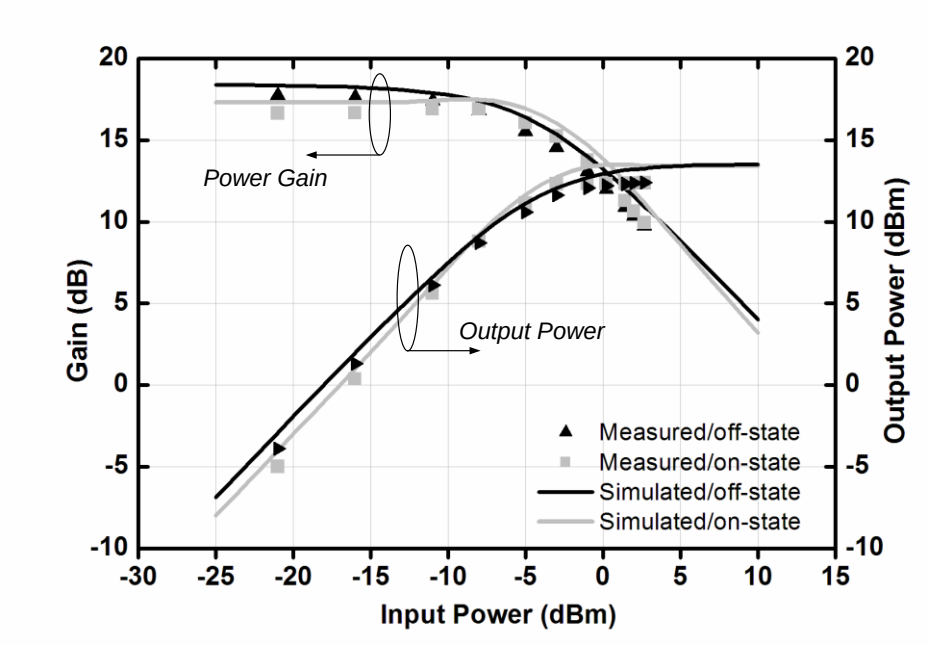


Figure 3.16: Gain compression & output power at 59 GHz in the off-state. The biasing condition is 1 V and 63 mA.

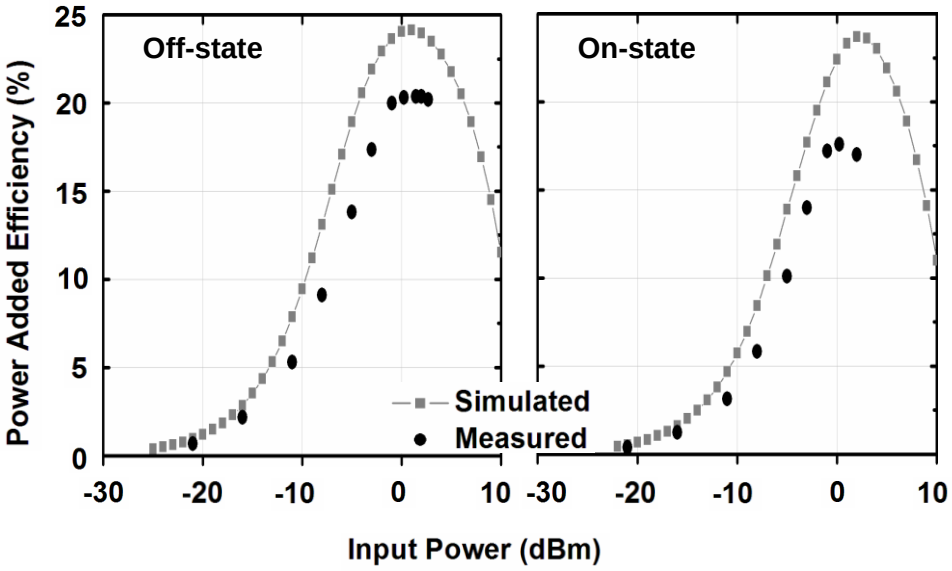


Figure 3.17: Measured power added efficiency at 59 GHz in the off-state. The biasing condition is 1 V and 63 mA.

Figure 3.16 shows how the output power varies with input power, under 63 mA current consumption. The measured output 1 dB compression points are approximately 8.5 dBm (off-state) and 9.1 dBm (on-state). Figure 3.17 demonstrates that the peak PAE at the off-state and on-state are around 20% and 17% respectively.

TABLE 3.6: Near 1 Volt Supply 60GHz CMOS PA Performance Comparison.

References	CMOS Technology	Supply (V)	Structure	Stages	Freq (GHz)	Psat (dBm)	Gain (dB)	OP1dB (dBm)	Max PAE (%)	FOM[&] ($W \times GHz^2$)
[34]	90nm *	1.0	Single-ended	3	60	11.0	14.3	10.0	8.2	97.6
[35]	65nm 10SF	1.0	DAT-based	3	60	17.7[@]	19.2[@]	15.1[@]	11.1[@]	1957.2
[11][§]	65nm SOI 1P7M	1.2	Single-ended	3	60	10.5	14.0	7.1	22.3	226.3
[8]	90nm 1P7M	1.0	Trans-coupled	3	62	12.3	14.3	9.0	8.8	154.6
[9]	90nm 1P9M	1.2	Trans-coupled	3	60	12.5	15.0	10.2	19.3	390.7
[10]	65nm *	1.0	Trans-coupled	3	58	11.5	15.4	8.0	15.2	307.7
This work[#]	**65nm 1P10M**	**1.0**	**Trans-coupled**	**2**	**59**	**12.3**	**17.1**	**8.5**	**20.4**	**618.5**

[#]at the off-state; [§] The case for lowest supply of 1.2 V is shown; * Metal option of the process is not specified; [@]the data are duplicated from bench marking table (Figure 23.6.7) in the original paper, [&] $FOM=P_{out} \times G \times PAE \times f^2$ [49].

3.5 Conclusion

This chapter presents a band-tunable power amplifier for millimeter-wave operation, designed for high gain and high efficiency in the required bandwidth. By applying a differential switch in the input matching network, the center frequency of the amplifier can be tuned from 53.5 GHz to 59.0 GHz. Due to the high reverse isolation (about 30 dB) from output to input port, stability in the different tuning states can be guaranteed. The benefits of narrow band matching and deep-neutralized MOSFETs are shown by the performance of this two stage design. With 63 mA current at 1 V, the peak output power is 12.3 dBm, the peak gain is 17.1 dB and the peak PAE is 20.4%.

CHAPTER 4

High Gain W-band Bandpass Amplifier

4.1 Introduction

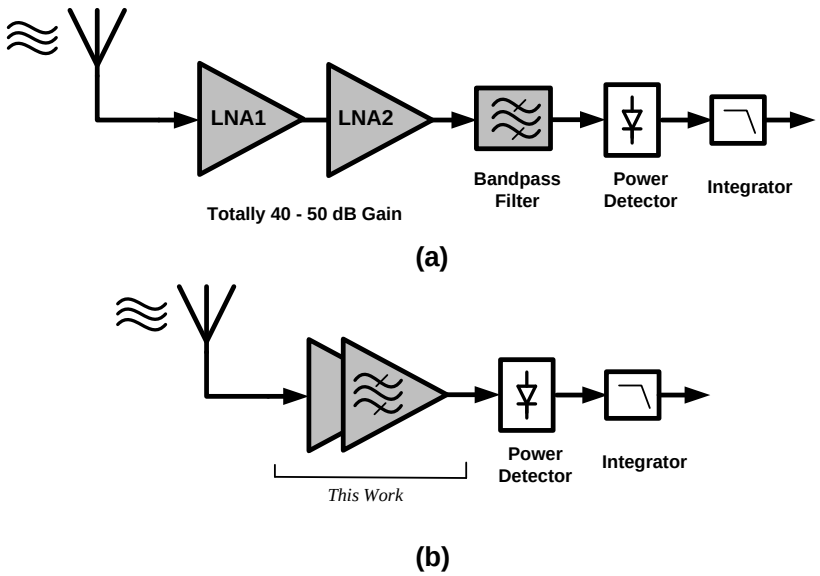


Figure 4.1: Block diagram of (a) standard W-band total power radiometer; (b) simplified W-band total power radiometer using high gain bandpass amplifier.

With CMOS and SiGe BiCMOS technologies achieving more than 240 GHz peak f_T and 300 GHz f_{max} [49], interest in silicon-based W-band imaging systems has been growing over the past few years. For silicon based passive imaging systems, a receiver with sufficient sensitivity at a low cost is critical to the success [50].

A typical passive imaging receiver consists of a total power radiometer (TPR). It includes an LNA, a bandpass filter and a square-law detector. In a typical TPR, the 1/*f* noise is overcome by using either a zero-biased high sensitivity detector or an ultra-high gain amplifier [14]. Responsivities of reported silicon-based detectors at present are around 12 to 90 kV/W [15], [51] which are significantly lower than the responsivity of Schottky diodes (300 kV/W) [52]. Thus, TPR based on silicon is still immature unless high performance diodes or transistors in silicon processes are developed. Alternatively, to achieve a typical threshold sensitivity value of 0.5-K $NE\Delta T$, very high gain (40 to 50 dB gain) can be obtained by cascading several amplifiers [52], [53]. Current single silicon-based W-band amplifier has achieved 12 to 27 dB gain [12], [13], [15]-[17], [54]-[58]. In addition, the bandpass filter is an essential part in the radiometer frontend [53], [59] which can prevent interferers from saturating the receiver. To date, silicon based millimeter-wave filters are still bulky and lossy to be used in system integration [60]-[66]. Hence, almost all reported silicon-based W-band passive imagers have excluded this block to guarantee the sensitivity performance by compromising frequency selectivity.

To solve the above two issues, a W-band bandpass amplifier is designed with both high gain and frequency selectivity, which avoids the use of multi-LNAs in cascade and passive millimeter-wave filters. As shown in Figure 4.1, the W-band receiver architecture can be simplified using the proposed bandpass amplifier. This bandpass amplifier uses gain-enhanced high-Q cascode stages, and makes the peaking frequencies obeying the Chebyshev

polynomials. The amplifier achieved more than 45 dB gain from 80-100 GHz and the obtained selectivity is comparable with reported passive millimeter-wave bandpass filters if not better. This amplifier is expected to help the silicon-based W-band TPR achieve a 0.5 K $NE\Delta T$. Moreover, stability is improved through specialized layout techniques.

4.2 Amplifier Performance required by the W-band Imaging System

4.2.1 Gain and Noise Figure

A microwave radiometer is a highly sensitive receiver capable of measuring low levels of microwave radiation. As shown in Figure 4.1 (a), the pre-amplifier, e.g. LNA before the detector is required to overcome the noise of the detector and to amplify the weak signal from the antenna. The gain and *NF* of LNA may greatly determine the TPR system sensitivity. Regarding signal detection, one important specification is the signal responsivity which can be expressed as:

$$\Re = \frac{V_{dc}}{P_{in-RF}} \tag{4.1}$$

Where $P_{in\text{-}RF}$ is the incident RF power and V_{dc} is the output voltage of the detector. Besides responsivity, the noise-equivalent power (*NEP*) and 1/*f* noise of the detector are also critical in determining the system performance. The definition of *NEP* is the input signal power to the sensor required to achieve an *SNR* of unity after detection, thus

$$NEP_{\det} = \frac{V_{out}}{\Re}\left(\frac{W}{\sqrt{Hz}}\right) \tag{4.2}$$

Where V_{out} is equivalent to the noise spectral density and its unit is $V/\sqrt{Hz}$, the noise bandwidth is 1 Hz.

For the detector in a normal TPR, it is desirable to minimize the *NEP*. But a low *NEP* requires high biasing current which may increase the 1/*f* noise. The system $NE\Delta T$ will deteriorate. To derive the temperature resolution, $NE\Delta T$, of the TPR, using the *NEP* definition (*SNR* = 1) and $\overline{P_{inc}} / dT \approx k \cdot B_{RF}$,

$$NE\Delta T \equiv \frac{P_{inc}}{\frac{d\overline{P_{inc}}}{dT}}$$

$$\equiv \left(\left[\frac{2\ T_B^2 + 1/\eta(F-1)T_2{}^2}{B_{RF}} + \left(\frac{NEP_{\det}}{\eta k G_{AMP} B_{RF}} \right)^2 \right] \frac{1}{2\tau} \right)^{1/2} \qquad (4.3)$$

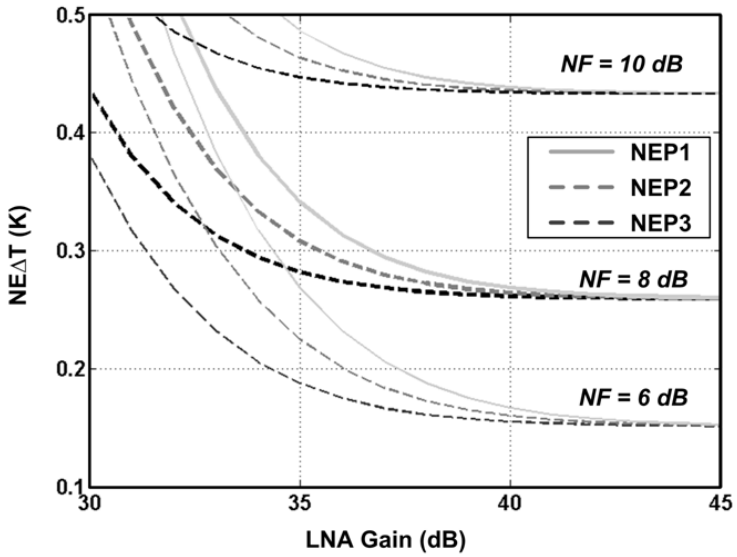


Figure 4.2: Calculated minimum temperature resolution (with *NEP*1, *NEP*2, *NEP*3 equals 3 $pW/\sqrt{Hz}$, 6 $pW/\sqrt{Hz}$ and 9 $pW/\sqrt{Hz}$ respectively for 6 dB, 8 dB and 10 dB LNA *NF*) for a preamplified total-power radiometer using the detector with *B* = 20 GHz and τ = 30 ms.

Referring to the specification of current silicon-based detectors, i.e. *NEPs* of 3 $pW/\sqrt{Hz}$, 6 $pW/\sqrt{Hz}$, 9 $pW/\sqrt{Hz}$, LNA *NF* of 6 dB, 8 dB and 10 dB, B_{RF} = 20 GHz, k = 1.38 × 10^{-23}, τ = 30 ms, T_0 = 298 K and η of 0.5, the corresponding $NE\Delta T$ is plotted in Figure 4.2. As shown, the minimum achievable $NE\Delta T$ is limited by the NF of the LNA. Meanwhile, if we increase the LNA gain from 30 dB to 40 dB, taking *NF* = 8 dB for example, the $NE\Delta T$ can be reduced from around 0.5 K to approximately 0.27 K. In addition, the smaller the *NF*, the more rapid reduction of $NE\Delta T$ with an increase in the amplifier gain. Note that this calculation did not consider the other two important factors, i.e. gain fluctuation $\Delta G/G$ and $1/f$ noise of the detector. Thus, the actual $NE\Delta T$ could be higher than this estimation. Another valuable observation is that the three resulting $NE\Delta T$ with different *NEP* are almost equal when LNA gain is around 40 dB or higher. This suggests the *NEP* requirement of the detector can be relaxed when the LNA gain is high enough. Overall, an LNA with a gain higher than 40 dB and NF below 8 dB are critical for the system to achieve < 0.5 dB $NE\Delta T$.

4.2.2 Bandwidth and Frequency Selectivity

Due to the atmospheric radio window centred at 94 GHz, the ideal bandwidth for a W-band receiver is 20 GHz. Even with such high operating frequency, bandpass filters are still needed in imagers to prevent the amplifier from being saturated [59] [53]. As a matter of fact, with the upcoming commercialization of millimeter-wave communication systems, frequency selectivity becomes more important for in-door W-band receivers. For

example, 60 GHz wireless personal area network (WPAN) with a maximum 10 dBm output power could be one of the interfering bands which may saturate the W-band LNA if the selectivity is not sufficient. As will be shown in 4.3.3, the high-Q characteristic of gain-enhanced stages and the synthesized bandpass filter matching method can help increase the selectivity of the amplifier which avoids the use of lossy millimeter-wave filters.

4.2.3 Dynamic Range

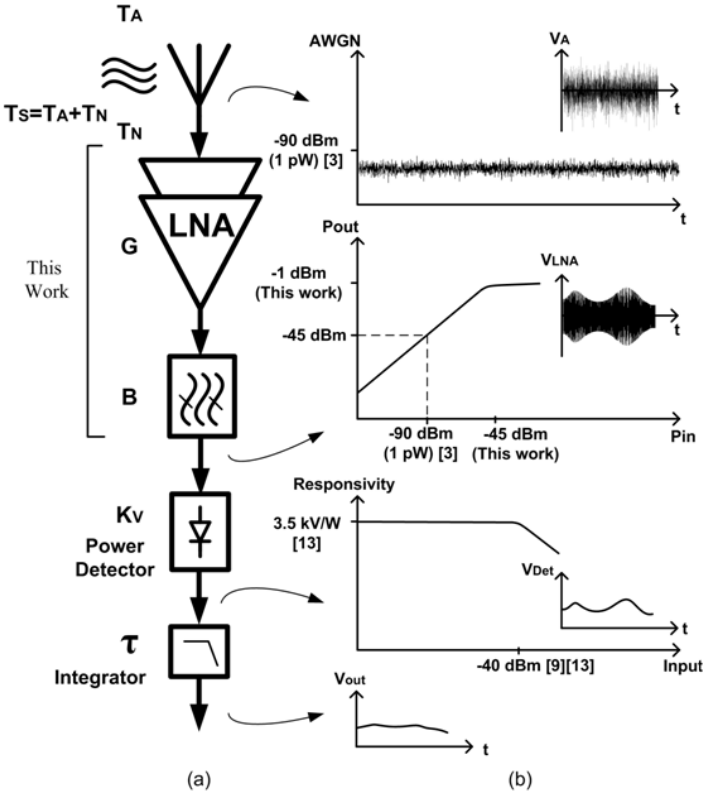


Figure 4.3：Block diagram of (a) a W-band total power radiometer; (b) Link budget of power at each node.

Since the energy of radiated thermal noise is extremely weak (10^{-15} to 10^{-20} W) [50] and input powers above approximately -40 dBm cannot guarantee a constant responsivity (in the square law region) in the current detectors [51],

[67], the LNA, which is located between the antenna and detector, should have above 40 dB gain. Additionally, the dynamic range of imaging systems needs to be shifted to lower power levels compared with communication systems. The input power of the LNA starts from -90 to -80 dBm, while the maximum output signal should be around -40 dBm.

4.3 High Gain and Frequency Selectivity Realization

It is challenging to achieve a high gain and bandpass function simultaneously with limited power consumption, especially at millimeter-wave frequencies and beyond. It is well known that using an inductance connected to the base of cascode HBT can improve the gain performance through positive feedback. However, the associated narrow bandwidth and poor stability are big issues for wideband high gain amplifier applications. In this section, the associated effects in terms of the degradation of stability, bandwidth and linearity in amplifiers are elaborated. Furthermore, compensation methods are proposed accordingly.

A straightforward method to implement a bandpass amplifier is to utilize DC block networks and matching networks with different types of magnitude response like high pass DC block network in combination with low pass input network or bandpass output network. Alternatively, low pass response in Chebyshev type or Butterworth type can be obtained by the choice of poles using inductance connected to the gate of common source stages [68]. However, the above methods may not achieve bandpass function and high gain simultaneously. Q compensation method and notch filter can be used to

achieve high gain and bandpass function [69]. The reported design demonstrated a remarkable gain of 22 dB and NF of 10 dB in CMOS technology. Nonetheless, this method may be more suitable for operating frequencies below 10 GHz. Similar to [69], the proposed W-band amplifier design used Q-enhanced bandpass filtering. The Q-factor enhancing is implemented by using gain-enhanced cascode as aforementioned. Moreover, by controlling the applied frequencies of source and load impedance of each stage and making peaking frequencies of each stage obey the Chebyshev polynomial, a bandpass amplifier with high gain is obtained. The topology of the inter-stage networks in this method can be diversified and not be restricted to a specific type as [68] since it only depends on input and output impedances.

4.3.1 Gain and Stability Tradeoff of Gain-Enhanced Stage

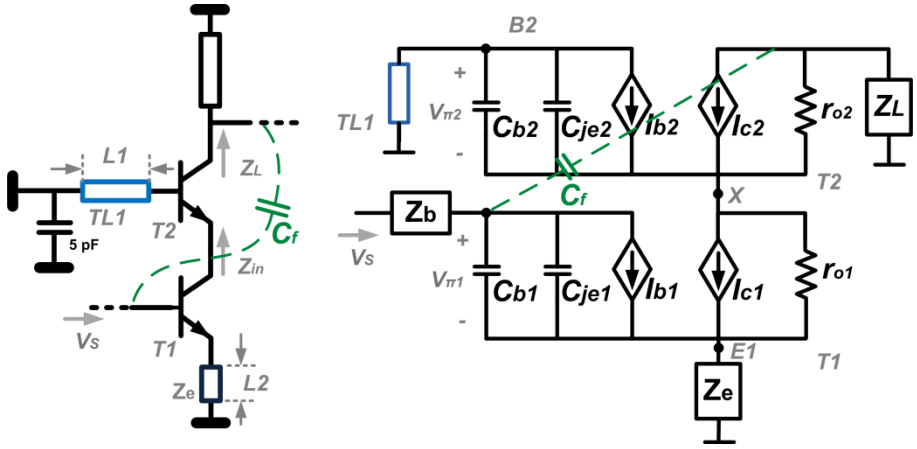


Figure 4.4： Gain enhanced cascade stage using a base-transmission line and its model.

As shown in Figure 4.4, the high-Q amplifying stages are realized by connecting a transmission line, TL1 to the base of Q2; the superior gain

performance of this approach was first presented in a 60 GHz receiver report [70]. Compared to a normal cascode, the base of T_2 in this architecture is no longer AC grounded. To quantify the achieved gain, a derivation is conducted based on a simplified model as shown in Figure 4.4.

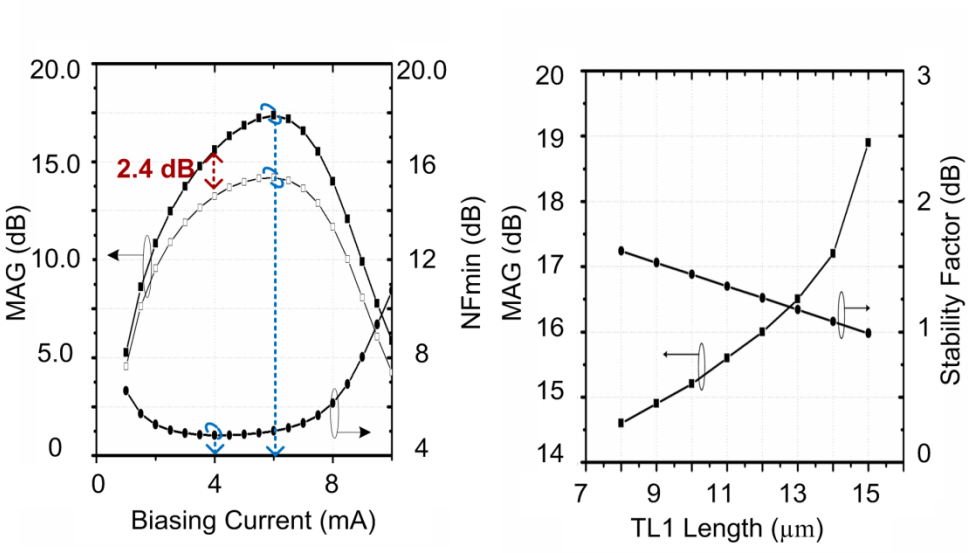
By applying KCL at nodes B_2 and X, gain can be derived as:

$$A = \frac{V_L}{V_S} = 10\log\left(1 + g_{m1} r_{be1} \frac{r_{o1}}{r_{be1}} \frac{Z_{TL1} + (1 + g_{m2} r_{o2}) Z_{be2}}{r_{o2} + Z_{TL1}} \frac{Z_L}{Z_{be2} + Z_{TL1}} \right) \tag{4.4}$$

where, $Z_{be1} = r_{be1} / (1 + s r_{be1} C_{b1})$, $Z_{be2} = r_{be2} / (1 + s r_{be2} C_{b2})$,

$Z_{TL1} = jZ_0 \tan(\beta l)$, $\beta = 2\pi / \lambda$; is the wavelength for on-chip transmission line and l is the physical length. In equation (4.4), the incremental gain of this gain-enhanced structure is shown to be approximately inversely-proportional to $Z_{be2} + Z_{TL1}$.

It is worth noting that this cascode stage can in fact achieve higher-Q than a normal cascode stage. By simulation, the peak gain can be boosted from 15.4 dB to 17.5 dB, and bandwidth can be reduced from 20.0 % to 11.3 % if the TL1 length increases from 0 μm to 10 μm. From the layout optimization work, an optimal TL1 length of 8 μm is chosen to maintain a K>1.5 for each stage.



(a) (b)

Figure 4.5: (a) MAG and NFmin versus biasing current. (b) MAG and stability factor versus TL1 length.

Figure 4.5 (a) plots the maximum achievable gain (MAG) and minimum noise figure (NF_{min}) versus biasing current with and without gain-enhancing transmission line, TL_2 (the supply voltage is 1.2 Volts and T_1 and T_2 emitters are 0.12 µm × 0.84 µm × 8). As shown in the above graph, the NF_{min} is exactly the same for cases with or without addition of TL_2 since TL_2 is noise free. On the other hand, the MAG can be boosted by 2.4 dB at the optimum NF_{min} biasing current (4 mA). This gain is even higher than the peak gain (with 6 mA biasing current) achieved without using the gain-enhancing technique.

4.3.2 Loaded Q Factor Enhancement and Passband Forming

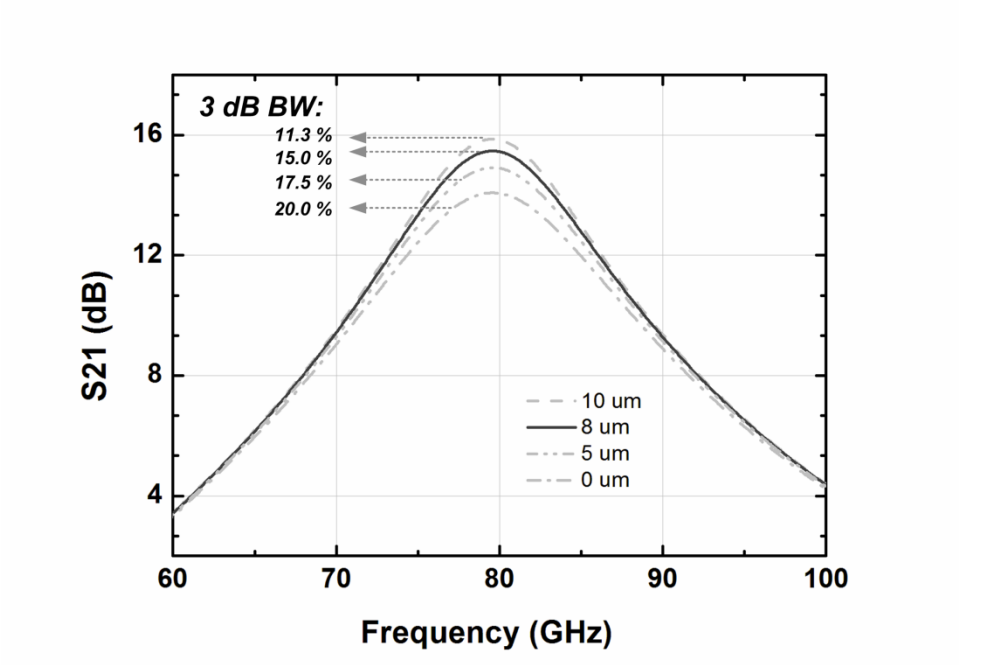


Figure 4.6: Loaded Q factor change with gain-enhancing effect.

The bandwidth of the gain-enhancing cascode decreases along with the increasing of TL_1 length (l_1) as shown in Figure 4.6. The 3 dB bandwidth decreases from 20.0 % to 11.3 % if the gain-enhancing effect becomes deeper. Therefore, the gain enhancement is obtained with the result of bandwidth reduction. On the other hand, the high loaded-Q characteristic of the gain-enhancing technique can bring benefits to the out-of-band rejection of the LNA, because the skirt of S_{21} as shown in Figure 4.6 is sharper for the higher Q stages.

For passband forming, the concept is to allow some ripple in the pass band of magnitude response and strategically choosing peaking frequencies of amplifying stages. To achieve the steepest transition, the four-stage peaking

frequencies, f_{s1} to f_{s4}, should be selected based on the Chebyshev polynomials (Chebyshev Ripple Frequencies):

$$T_n(\Omega) = \cos(4 \cdot \arccos(\Omega)), \qquad \text{for } |\Omega| \le 1$$

$$T_n(\Omega) = \cosh(4 \cdot \arccos h(\Omega)), \qquad \text{for } |\Omega| \ge 1 \tag{4.5}$$

Corresponding magnitude attenuations can be presented by the following equation:

$$A(\omega) = 10 \cdot \log_{10}(1 + \varepsilon^2 \cdot T_N^2(\Omega)) \tag{4.6}$$

where $\Omega = \frac{\sqrt{\omega_U \cdot \omega_L}}{\omega_U - \omega_L}\left(\frac{\omega}{\sqrt{\omega_U \cdot \omega_L}} - \frac{\sqrt{\omega_U \cdot \omega_L}}{\omega}\right)$, $\varepsilon = \sqrt{10^{0.1 \cdot A_p} - 1}$, A_p is the ripple in the passband.

By solving the equation:

$$\frac{\partial(A(\omega))}{\partial(\omega)} = 0 \ \| A(\omega) = 0 \tag{4.7}$$

The four-stage Chebyshev ripple frequencies from 80 - 99 GHz are calculated by Chebyshev polynomials accordingly and the magnitude response with 1dB ripple is plotted in Figure 4.7.

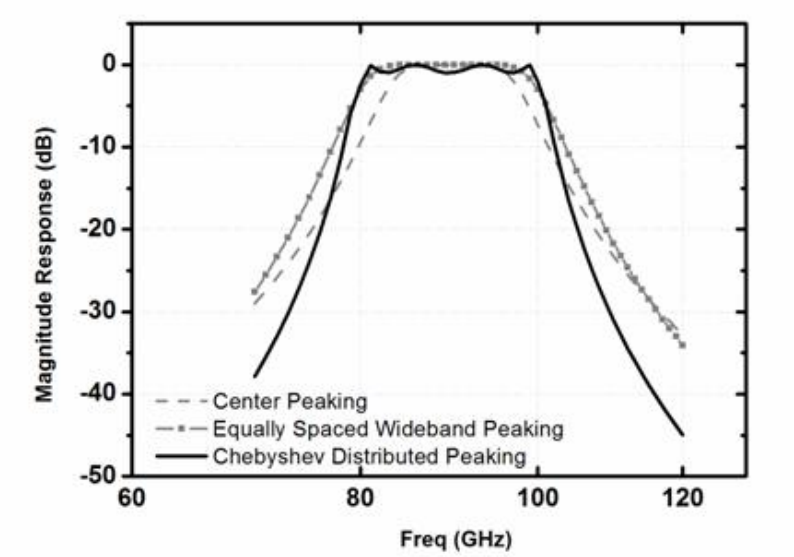


Figure 4.7: Simulated 4-stage magnitude response using center peaking, Butterworth bandpass and Chebyshev bandpass response at W-band.

These ripple frequencies are namely, 80.5 GHz, 85.5 GHz, 93.5 GHz and 98.5 GHz. The four stage-peaking frequencies, f_{s1} to f_{s4}, were set to be the same as these four frequencies by controlling the source and load impedances of the cascode stages. The matching network peaking-frequencies, f_{m1} to f_{m5} in between adjacent f_s were optimized to maintain a flat amplifier gain in band and compensate the degraded power gain at higher frequencies. The detailed peaking-frequencies of these stages and matching networks are presented in Figure 4.8. The phase delay violation caused by parasitic capacitance in the T-junctions is corrected by the final layout optimization in HFSS.

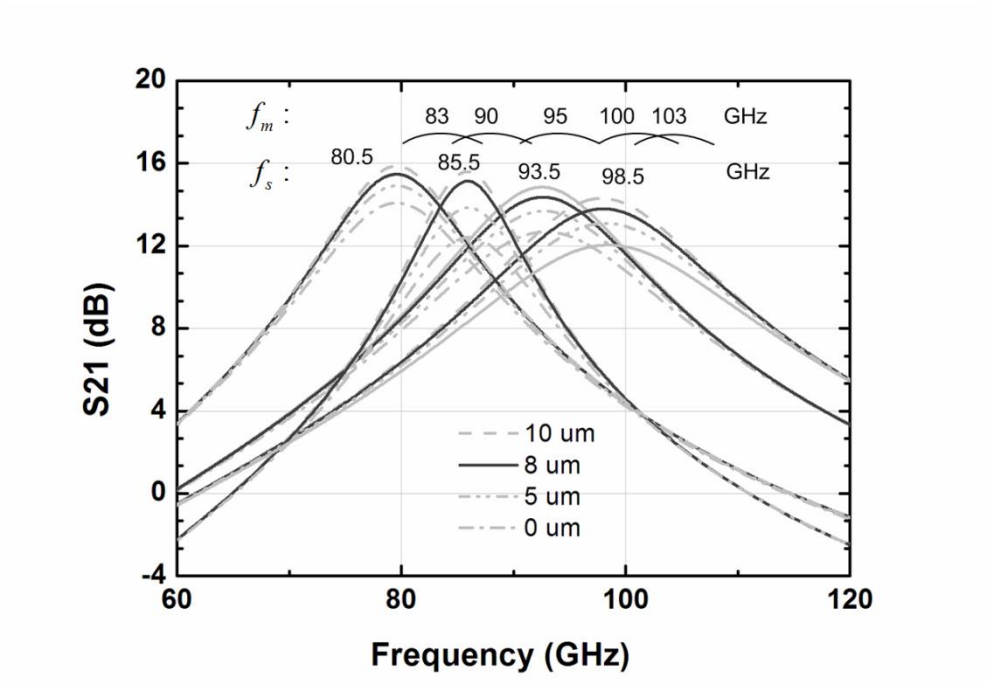


Figure 4.8: Simulated peaking frequencies based on basic Spectre models.

4.4 Passives to Ensure Stability

As aforementioned, the stability of the gain-enhanced stage is lower than normal cascode stages. At millimeter-wave frequencies, circuits encounter serious coupling problems in layout design. Parasitic effects which could cause instability in the LNA are analyzed. The shielding structure for the cascode stage and partition shielding walls are proposed to effectively reduce the coupling and enhance stability at the transistor level and circuit level respectively.

4.4.1 Shielding Structure for Cascode Stage

Transistor level passive feed-line modeling has been reported [72], which helps predict parasitic effects of passive connections on transistor performance precisely.

In the cascode stage, the detrimental parasitic effects between input and output VIAs also cannot be ignored. As shown in Figure 4.9 (a) and (b), parasitic coupling exists between the RF_IN and RF_OUT VIAs. Generally, the smaller the transistor length, the stronger the coupling effect will be. According to our process and the feedline width, this capacitance is around 13.9 *f*F. This feedback capacitance can cause both stability degradation and gain degradation.

From theoretical derivation, the voltage gain of the cascode stage including C_f is derived based on the model shown in Figure 4.4:

$$A = 10\log\left(\frac{1}{Z_{be1}}\frac{r_{o1}\ 1+g_{m1}Z_{be1}}{Z_L+r_{o2}+sC_fZ_Lr_{o2}}\left[1+\frac{g_mZ_{be2}r_o2}{Z_{be2}+Z_{TL1}}-\frac{sC_fr_{o2}Z_{be1}}{r_{o1}(1+g_{m1}Z_{be1})}\right]Z_L\right) \tag{4.8}$$

Compared with equation (4.4), there is one more term with a negative value in the brackets, $-sC_fr_{o2}Z_{be1}/r_{o1}(1+g_{m1}Z_{be1})$, which is proportional to C_f. Therefore, the cancellation of C_f results in a higher gain of the cascode stage.

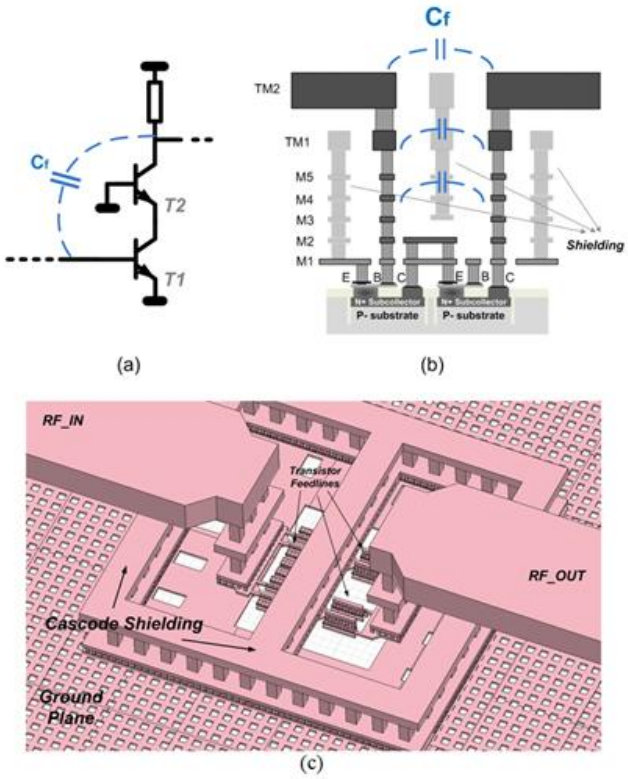


Figure 4.9: (a) Parasitic capacitor (C_f) between feedline-in and feedline-out. (b) 3D view of the feedlines and cascode shielding structure in Ansoft HFSS. (c) Cross-section and metal options of the shielding.

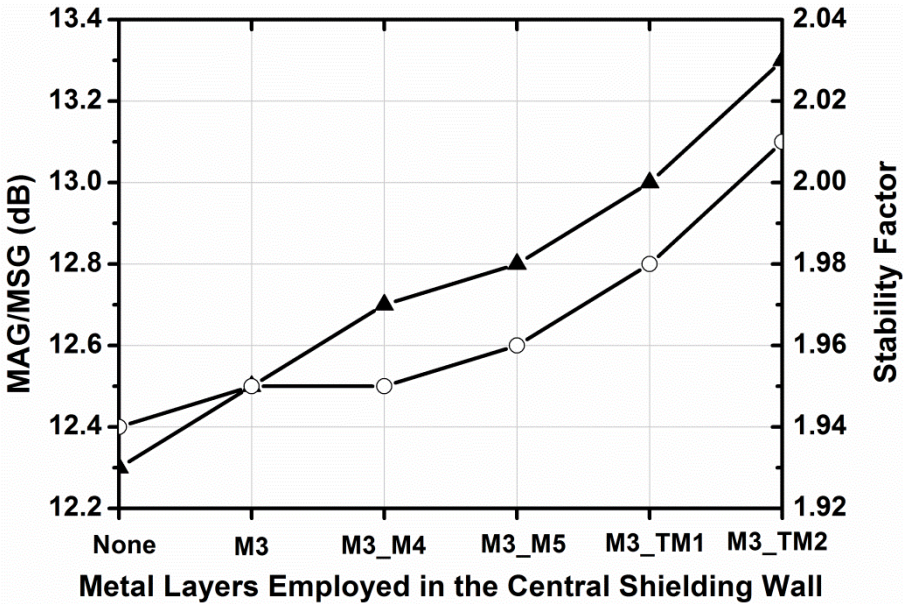
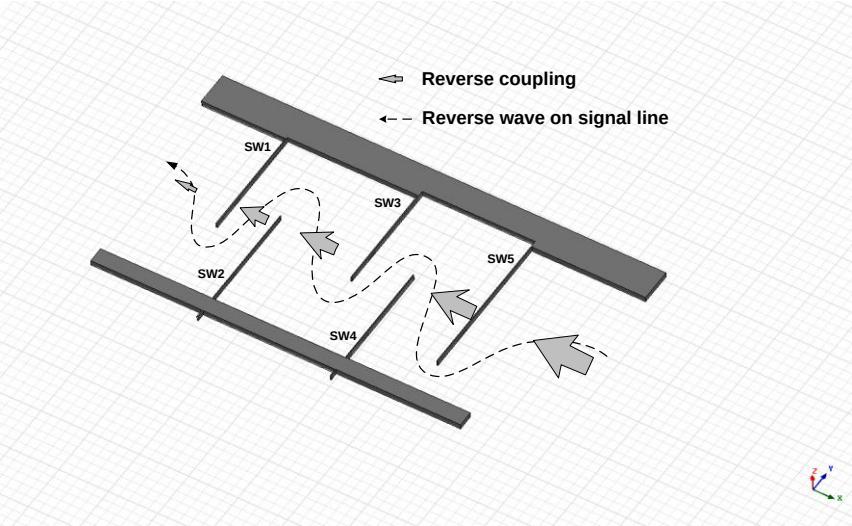


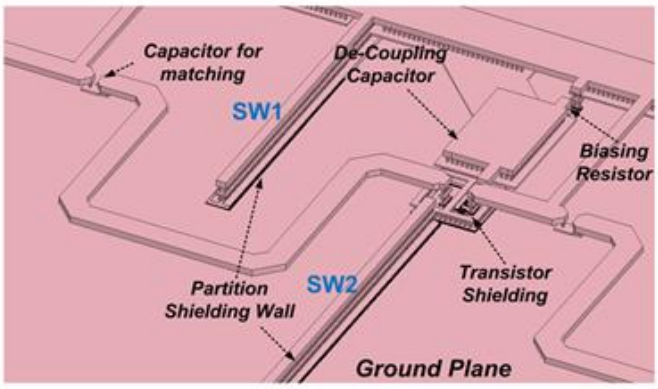
Figure 4.10: MAG/MSG and stability factor versus the height of the central shielding structure.

As shown in Figure 4.9 (b) and (c), a shielding structure for the cascode stage is developed to mitigate this parasitic coupling. The grounded-shielding structure and central isolation wall are formed by stacking metal layers from the bottom M1 layer to the top TM2 layer. The coupling capacitance between the interconnection vias is reduced greatly through the introduction of this shielding. This cascode shielding structure is similar to the one which was used in [73] to mitigate Miller-effect in common emitter HBT in frequency tripler design. The result shown in Figure 4.10 indicates that the gain for single stage can be increased for 1 dB and the stability factor can be enhanced for around 0.1 simultaneously. Using this cascode stage shielding, the single stage has a maximum gain of 13.3 dB and maximum stability factor of 2.03.

4.4.2 Partition Shielding



(a)

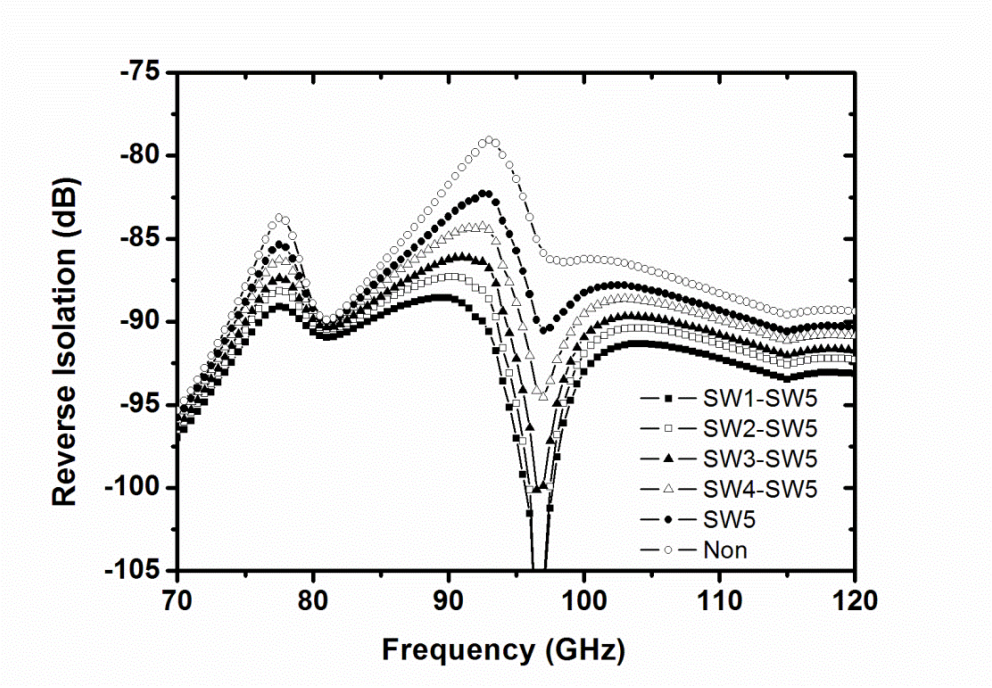


(b)

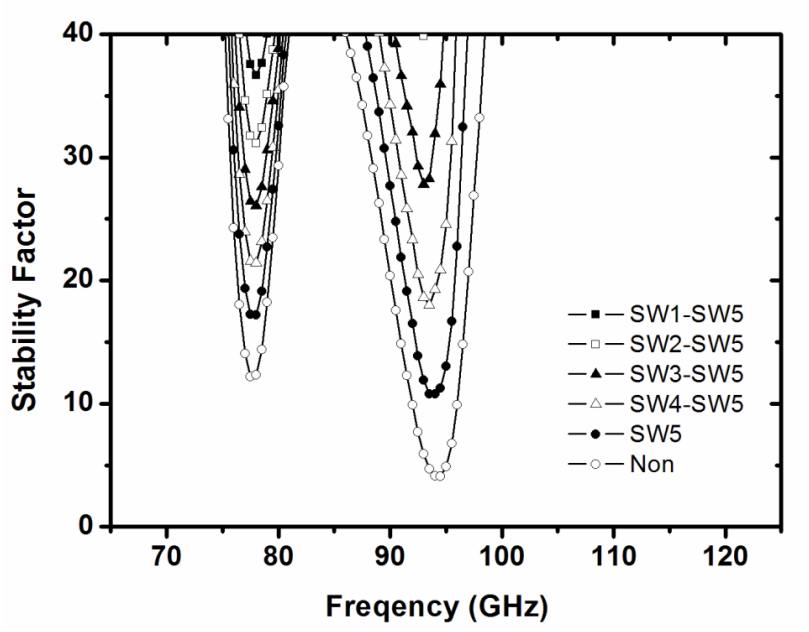
Figure 4.11: (a) Top view of the partition shielding walls. (b) 3D view of the shielding structures, capacitors, resistors and passive connection around SW1 and SW2 in Ansoft HFSS.

At the whole circuit level, high reverse isolation is achieved by the proposed partition shielding walls. As reverse isolation is layout-dependent in millimeter-wave circuits, sufficient reverse isolation and stability margin should be ensured particularly for high gain applications [74]. Figure 4.11 (a) shows that two mechanisms can affect the reverse isolation and further deteriorate the stability performance of the amplifier. One is the reverse wave existing on the signal line caused by the mismatching between stages. In this LNA, the reverse wave on the signal line can be mitigated due to the high isolation between cascode stages. The other one is the reverse EM coupling existing in the layout. This coupling effect is proportional to the power level of the signal at different stages and it propagates in a straight direction. As shown in Figure 4.11 (b), the inter-stage matching networks are designed to be twisted, which leaves space for the shielding walls to be inter-digital. All shielding walls are terminated with large MIM de-caps, which are also used for the de-coupling of collector and base bias lines. With the introduction of this shielding, the stability factor of the LNA is enhanced according to the

well-known Rollett stability factor definition. Using all the shielding walls as shown in Figure 4.11 (a), this issue is eliminated.



(a)



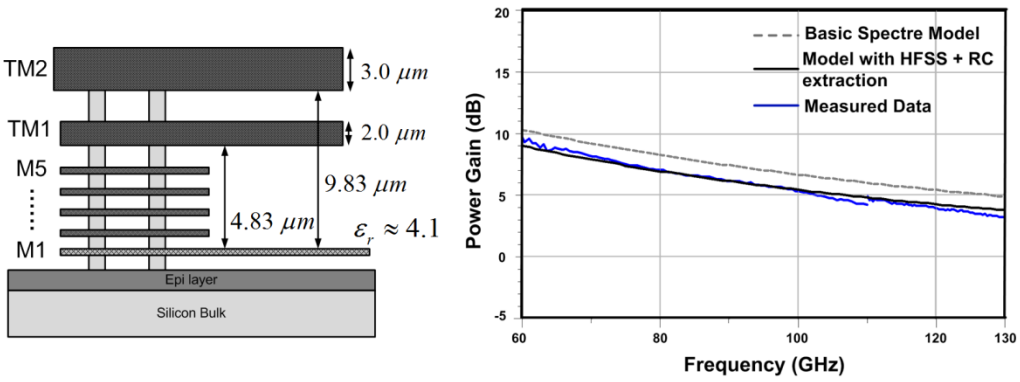
(b)

Figure 4.12: The simulated (a) reverse isolation and (b) stability factor with different partition shielding options in the LNA operation frequency range.

Figure 4.12 (a) shows that reverse coupling is greatly reduced by using the partition shielding walls from SW1 to SW5. The simulated reverse isolation at 94 GHz is improved from -79 dB to -90 dB. Meanwhile, as shown in Figure 4.12 (b), the stability factor increases from 4 (without using shielding wall) to above 35 (by using SW1 to SW5).

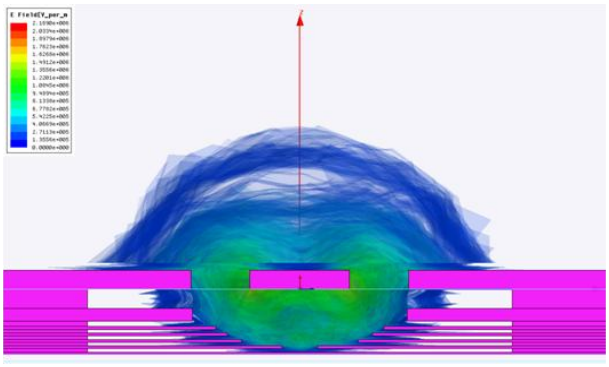
4.5 Amplifier Implementation

The process used is IHP 0.13 m SiGe BiCMOS [75]. The f_T and f_{max} are 240 GHz and 300 GHz respectively. With 4 mA collector biasing current of the common-emitter HBT (A_E = 2 × 0.12 μm × 0.84 μm), the f_T is 228 GHz. As shown in Figure 4.13 (a), the back-end-of-line (BEOL) in this process offers two thick metal layers (*TM*1, *TM*2) and five thin-metal layers (*M*1–*M*5). The top 3 μm thick metal layer (*TM*2) is employed for signal lines and the 0.4 μm thick bottom metal layer (*M*1) is used for the ground plane. The HBTs of *T*1 and *T*2 in the four cascode stages are all in size of 0.12 μm × 0.84 μm × 4 × 2. We have not optimized the performance of the cascode stage through sizing *M*1 and *M*2 since 0.12 μm × 0.84 μm × 4 model demonstrated the best fit with our device characterization results among all provided devices. Meanwhile, the used HBT model was verified using both the ANSYS HFSS and Assura RC extraction. As shown in Figure 4.13 (b), the variation caused by parasitic coupling is underestimated by the basic Spectre model. With the assistance of the above two tools, the simulation result fits well with measured power gain from 70 GHz to 120 GHz.

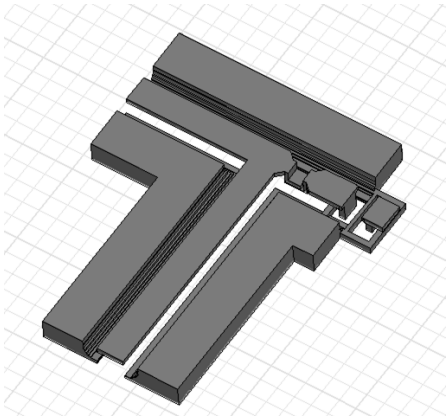


(a) (b)

Figure 4.13: The model verification: (a) Metal layers information for passive modeling; (b) Power gain verification of the used HBT with size of 0.12 µm × 0.84 µm × 4 under bias condition: I_b=25 µA, V_c=1.2 V.



(a)



(b)

Figure 4.14: (a) Cross-section view and simulated E-field of the used Semi-coaxial grounded coplanar waveguide (SC-GCPW) with 50 Ω characteristic impedance in Ansoft HFSS. (b) Full EM modeling of input matching network in Ansoft HFSS.

The input matching network design is important for LNA performance since the input matching loss will be added into *NF* directly. A semi-coaxial grounded coplanar waveguide (SC-GCPW) is used for the input matching to reduce the LNA noise factor. Its implementation in modern CMOS processes has been reported [76]. Due to the evenly distributed electric field in the semi-circular dielectric beneath the signal line, the area of dense E-field (green colour) is strengthened beneath the signal line as shown in Figure 4.14 (a). Therefore, the current path in the signal line cross section can be thicker, which results in lower conductor loss. Figure 4.14 (b) demonstrates the EM model of the input matching network in ANSYS HFSS. 0.3 dB smaller loss is obtained by this SC-GCPW input matching compared with a microstrip based input matching network. Thus, the *NF* of the LNA has also decreased by approximately 0.3 dB.

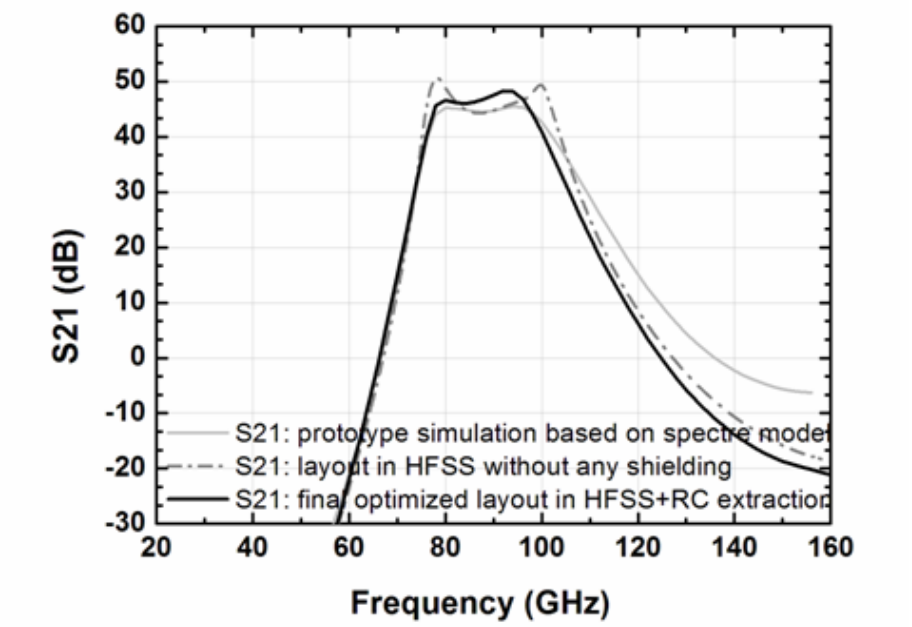


Figure 4.15: Simulation results of S21 using spectre model and S21 of final optimized layout.

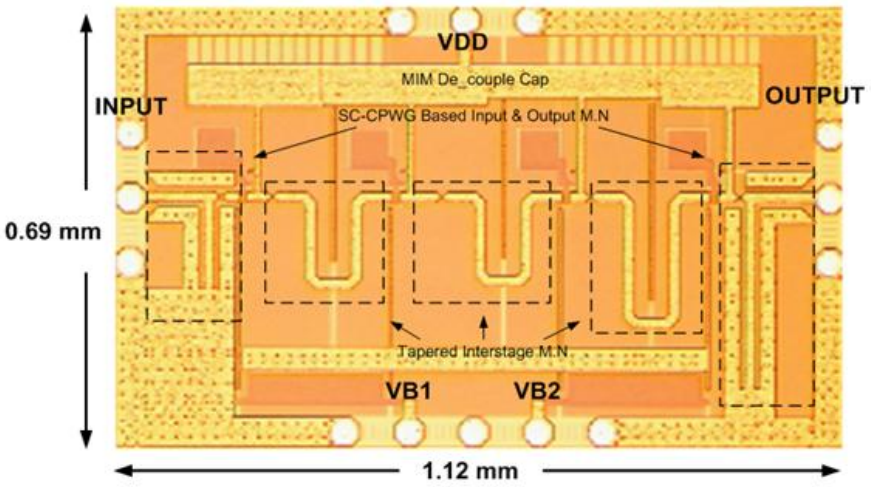


Figure 4.16: Micrograph of the 94 GHz LNA chip.

This amplifier is implemented with further layout optimization in ANSYS HFSS. The power gain responses of derived prototype, schematic with primary layout simulation and schematic with all shielding structures are shown in Figure 4.15. It is indicated in Figure 4.15 that, the amplifier layout without using any shielding may suffer instability. The frequencies at which this amplifier is potentially un-stable are 80 GHz and 100 GHz respectively. As shown by the curve in the solid line in Figure 4.15, the above stability issue is alleviated by using cascode shielding and partition shielding walls.

The total power consumption is 16 mA × 1.2 volts. This LNA demonstrates around 45 dB gain and 6.5 dB NF @ 95 GHz in simulation. The micrograph of the fabricated LNA is given in Figure 4.16 and the total chip area is 0.69 × 1.12 mm^2. Due to the process requirement of 2 μm minimum width for the TM2 layer, the actual central wall in cascode shielding used is the thick metal layer, TM1.

4.6 Measurement Method and Results

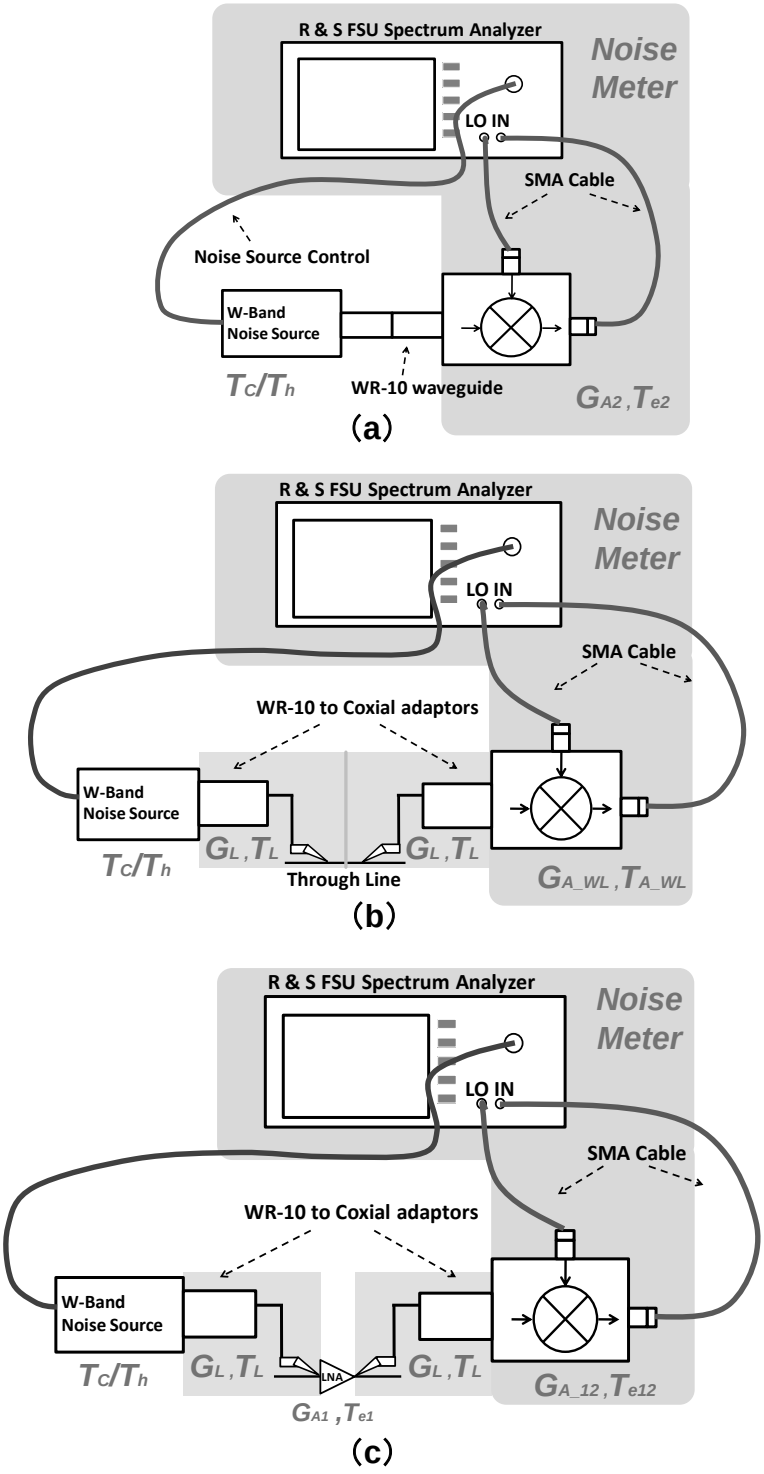
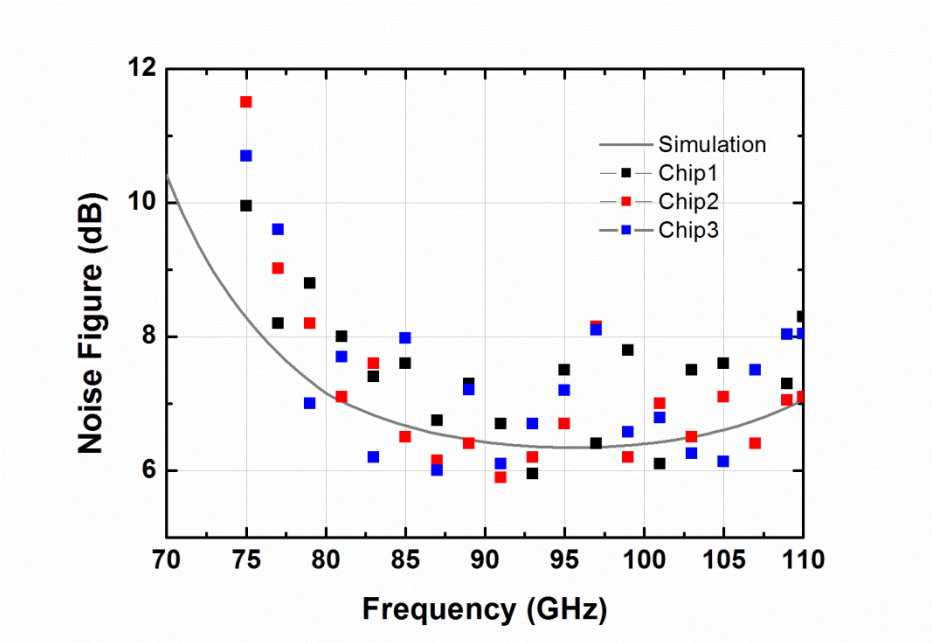


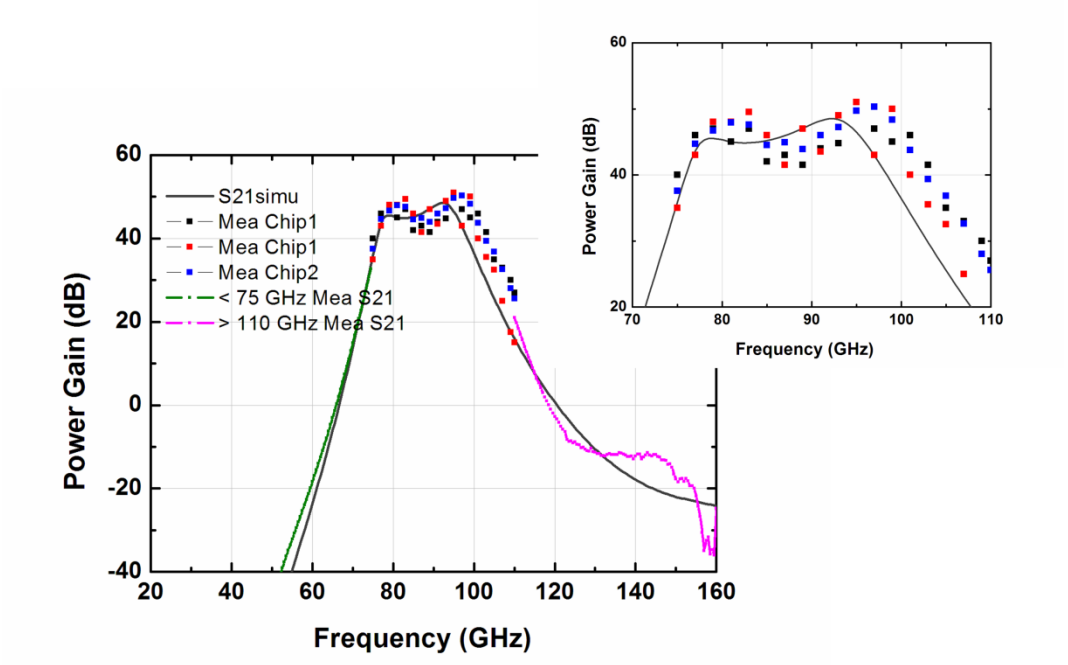
Figure 4.17: The W-Band gain and noise figure measurement setup. (a) Step1: Equipment Calibration; (b) Step2: Through line calibration for connection loss; (c) Step3: LNA measurement in the system.

To measure the gain and noise of this LNA in W-band, *Y*-factor technique [77] is used for noise characterization. The noise characterization system contains a W-band noise source, WR-10 waveguides, WR-10 to coaxial adaptors, 1.85 mm coaxial cables and on-wafer probing. Furthermore, the measuring frequency range is extended to 110 GHz by a 67-GHz spectrum analyzer (R&S FSU) through an external harmonic mixer similar to [78]. The LO signal required by the down converter (mixer) is provided by the spectrum analyzer LO/IF ports. Data were recorded for 19 frequency points, from 75 GHz - 109 GHz with 2 GHz intervals and a final point at 110 GHz. According to the excess noise ratio (ENR) table of the noise source provided, the typical ENR is around 12 dB with fluctuation from a minimum value of 11.4 dB at 77 GHz, 79 GHz and 110 GHz to a maximum value of 13.0 dB at 89 GHz and 109 GHz respectively. W-band isolators are connected after the noise source which can prevent reflections from reaching the noise source and combining with the incident signal. Since similar noise figures and gain measurement method of 60 GHz LNA have been reported [79], only the specific data and methods involved in this measurement are mentioned. In the first step, as depicted in Figure 4.17 (a), the spectrum analyzer noise and down-convertor noise are calibrated out with the W-band noise source. For the de-embedding step (second step) as illustrated in Figure 4.17 (b), the loss existing on the connections including waveguides, coaxial adaptors, cables, probes and GSG pads can be measured by inserting a 200 μm long through-line between the probes. After recording the total loss from 75 GHz - 110 GHz, the total measured connection loss is split equally and loaded into the spectrum

analyzer. The loaded loss-in or loss-out is around 10 dB with a minimum value of 9.5 dB at 91 GHz and a maximum value of 10.4 dB at 95 GHz. These corrections of connection loss are applied for measurements in the next step and processed automatically inside the spectrum analyzer. In the final step as shown in Figure 4.17 (c), the through-line in the above step is replaced by the properly biased LNA to measure the NF and gain. In order to achieve a low level of jitter, 10 readings, with a 0.2 second sweep time and a resolution bandwidth of 1 MHz were used in the measurement. The video bandwidth was set as low as 10 MHz to ensure measurement accuracy.



(a)

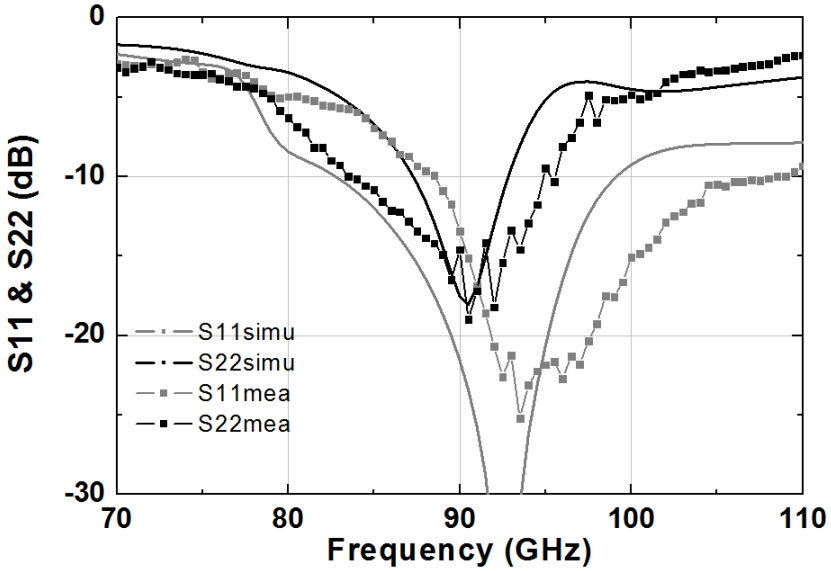


(b)

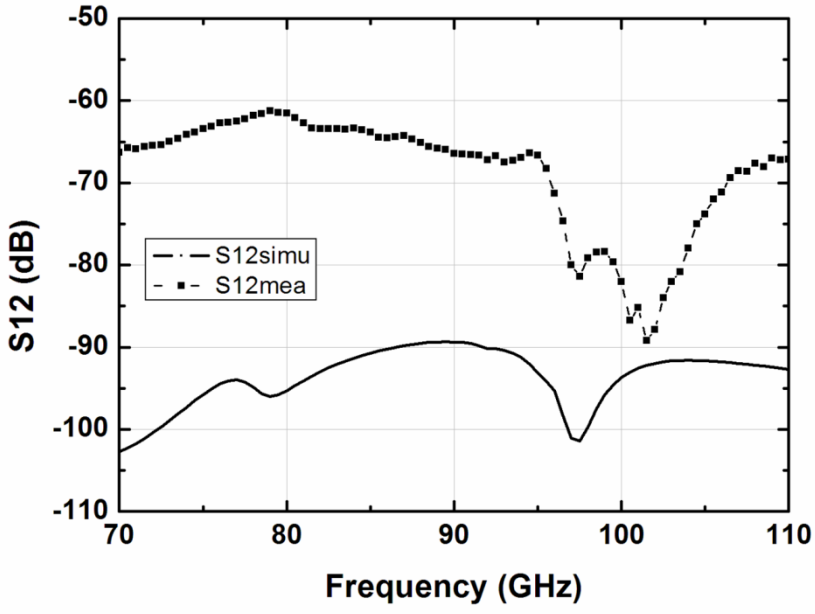
Figure 4.18: Simulated and measured (a) Noise figure; (b) Power gain.

Figure 4.18 (a) and (b) provide the simulated and measured LNA NF and gain. There is around 4 dB gain fluctuation in band and it achieves around 45 dB gain at around 95 GHz. The noise figure ranges from around 6 to 8 dB in band, and the NF at 95 GHz is 7.2 dB. Meanwhile, the average gain in the frequency band of interest is above 45 dB. The bands shift slightly to upper frequencies compared with simulated results. The un-symmetrical S21 response might be because both the input and output matching network are high pass networks. Besides the power gain measurement, two VNA systems for below 110 GHz (Anritsu 37397D extended system) [31], [74] and 110 GHz - 170 GHz (R&S ZVA24 extended system) are used to evaluate the lower-band S21 and upper-band S21 respectively. Using 67 GHz signal generator, an external quadrupler (VDI) and power meter (Erickson PM4), the dynamic range is also evaluated. The measured output P_{1dB} is -47 dBm.

Moreover, the P_{1dB} can be increased to -39 dBm by changing biasing current of the first two stages (VB1 as marked in Figure 4.16) to 2 mA.



(a)



(b)

Figure 4.19: (a) Simulated and measured return loss; (b) Measured reverse isolation.

Besides the above measurement, the other S-parameters including S11, S22 and S12 were measured on the < 110 GHz VNA on-wafer platform (Anritsu 37397D extended system) with a consistent frequency sweep from 70 to 110 GHz. The gain cannot be measured precisely by VNA due to the low input measurement power required by the 94 GHz LNA. The gain began to compress at an input power level of -50 dBm. Since current VNA is not able to calibrate with an input power of lower than -50 dBm, the VNA is not able to get the entire gain performance. The vector network analyzers were calibrated using the LRRM method from 70-110 GHz and 110-170 GHz respectively. Since the parasitic capacitance introduced by each GSG pad with 100 μm pitch is around 35 *f*F, thru-short de-embedding methods were used to de-embed the effects of the interconnections and GSG pads outside the reference planes [80]. The return loss at the input and output port after de-embedding are shown in Figure 4.19 (a). In addition, the reverse isolation of this amplifier is indicated in Figure 4.19 (b). The input matching and output matching peaks are around 91.0 GHz - 92 GHz. Due to the layout dependent reverse isolation, the measured reverse isolation in the whole band is above -60 dB which is different from the simulated value. However, six dies were measured using the above measuring method and they all worked stably. Good consistency from DC power consumption, gain, noise figure to S-parameters are obtained. TABLE 4.1 summarizes the measured performance and compares several recent reported LNA designs at W-band.

Several millimeter-wave bandpass filters are referred in TABLE 4.1 to compare their selectivity with this amplifier. A well-known specification, called the shape factor, is used to quantify the selectivity and is defined as:

$$SF = \frac{BW^{-ndB}}{BW^{-3dB}} \tag{4.7}$$

As exhibited in TABLE 4.2, this amplifier demonstrates smaller shape factor (higher selectivity) than most of the millimeter-wave filters. One reason is that the coupling between resonators in passive filters is somehow upset due to the serious parasitic coupling at millimeter-wave band. Thus, unexpected cross-coupling cannot be prevented. However, in this amplifier design, resonators (shielded cascode amplifying stages) are highly isolated from output to input. They are "coupled" through lumped matching networks which suffer from less parasitic effects and can be controlled more precisely. Another reason is that passive resonators in millimeter-wave bands are lossy and featured lower loaded Q factors than gain-enhanced stages.

TABLE 4.1: A Comparison of W-band Amplifiers on Silicon with Ft around 220 GHz

Ref	Technology	Peak Gain (dB)	Gain (dB)	Topology	Noise Figure (dB)	Power Consumption (mW)
[16]	65 nm CMOS	27 @ 88 GHz	> 24 (83-93 GHz)	5-stage cascode	6.8-10 (75-89 GHz)	36@1.2 V *
[54]	65 nm CMOS	15 @ 86 GHz	> 12 (81-92 GHz)	5-stage CS	7-9 (85-95 GHz)	42 @ 1.2 V
[55]	65 nm CMOS	25.3 @ 117.5 GHz	> 20 (75.5-120.5 GHz)	4-stage cascode	6-8.3 (87-100 GHz)	48 @ 2 V
[56]	65 nm CMOS	13.5 @ 81 GHz	> 10.5 (72-92 GHz)	3-stage cascode	6.4-8.4 (75-88.5 GHz)	36.3@1.5 V
[57]	65 nm CMOS	14.8 @ 90 GHz	> 11.8 (82-103 GHz)	4-stage CS	7.5 - 9 (82 - 100 GHz)	86.4 @ 1.2 V
[58]	65 nm CMOS	12 @ 79 GHz	> 9 (75-81 GHz)	6-stage CS	9 - 10.5 (75-81 GHz)	32.4 @ 1.2 V
[15]	0.13 µm BiCMOS	22.5 @ 98 GHz	> 19 (86-104 GHz)	5-stage CS	8 (80-110 GHz)	34.8 @ 1.2 V
[12]	0.13 µm BiCMOS	23 @ 89 GHz	> 20 (87-93 GHz)	3-stage diff cascode	N.A.	36.3 @ 3.3 V
This Work	**0.13 µm BiCMOS**	**48 @ 95 GHz**	**> 45 (77 - 100 GHz)**	**4-stage cascode**	**6.0 - 8.1 (80-107 GHz)**	**20 @ 1.2 V**

* Estimated from description or measured graph.

TABLE 4.2: A Comparison of Millimeter-wave Filters on Silicon

Ref	Technology	Center Frequency	S21 (dB)	Pass-Band	Shape Factor (SF)	Chip Size
[60]	0.18 µm CMOS	60 GHz	- 2.1	51 %	2.6 @ -15 dB	790 µm × 220 µm
[61]	0.18 µm CMOS	60 GHz	- 4.0	65 %	2.1 @ -20 dB	150 µm × 690 µm
[62]	0.18 µm CMOS	64 GHz	- 4.9	18.7 %	3.3 @ -30 dB	710 µm × 710 µm
[63]	0.18 µm CMOS	60 GHz	- 9.3	10 %	7.2 @ -40 dB	2010 µm × 200 µm
[64]	0.18 µm CMOS	70 GHz	- 3.6	25.7 %	2.3 @ -35 dB	650 µm × 670 µm
[65]	SiGe : C	77 GHz	- 6.4	15.6 %	3 @ -30 dB	110 µm × 60 µm
[66]	N.A	97 GHz	- 2.7	10 %	2.8 @ -20 dB	1644 µm × Width
This Work	**0.13 µm BiCMOS**	**90 GHz**	**> 45 (Amplifier)**	**25.5 %**	**1.5 @ -15 dB 1.6 @ -20 dB 2.0 @ -30 dB 2.7 @ -40 dB**	**1100 µm × 700 µm**

4.7 Conclusion

In this Chapter, the W-band imaging system requirement on the amplifier is analyzed. A high gain W-band amplifier with bandpass magnitude response is designed in 0.13 µm BiCMOS technology. The implemented amplifier has obtained a gain of > 45 dB in band, noise figure of 6.0 to 8.1 dB, high selectivity and power consumption of 19 mW in 0.13 µm BiCMOS which can help the TPR achieve a <0.5-K $NE\Delta T$. Moreover, the amplifier is expected to simplify the frontend design with its high gain and selectivity.

CHAPTER 5

High Gain Cascode Stage Utilizing a Passive Compensation Network

5.1 Introduction

As aforementioned in Chapter 4, high gain is needed for the low noise amplifier (LNA) in imaging receivers to enhance sensitivity. The Miller-effect is one of the main reasons which limit the f_T and the gain performance of the single stage. Although ultra-high gain can be obtained using the positive feedback at the base of the common base HBT, the stability of amplifier is degraded and additional passive shielding structures are needed. This chapter explores a neutralization method to enhance the fundamental performance of the device, MAG, without sacrificing any stability or noise figure. Meanwhile, by applying this method on the cascode stage, the highest MAG/MSG reported is achieved by the single stage.

The performance of the classic neutralization method using a tapped transformer in series with a capacitor is stated to be unattractive due to the poor quality of on-chip transformers [42]. In addition, it may also suffer from the relatively narrow bandwidth of the transformer. An easy way to cancel the

Miller-capacitance at high frequency is to use cross-coupled differential common emitter pairs [10], [42], [74]. This method features less parasitic effects and obviates the need for large additional inductors or transformers. However, the maximum stable gain has been demonstrated to be less than the normal cascode [10]. In addition, the noise figure of the differential pair is normally higher than its single-ended counterpart under the same power consumption. Cascode stage can lower the output impedance of the common emitter HBT (T_1) and reduce the influence caused by Miller-effect. It features high output impedance, high gain and high reverse isolation. Nevertheless, the Miller-effect still has not been totally eliminated, and its influence on gain performance still exists. Active cascode [81] introducing a negative gain at the base of the common base HBT (T_2) can boost the output impedance and gain of the cascode. The limitation is that the gain falls tremendously with increasing frequency, and the feedback loop may not be stable in all cases. It may also introduce more noise source if it is used for low noise amplifier design. Additional power consumption and more parasitic effects introduced may also make this topology unattractive for high frequency operation. Using an inductor for parallel resonance with C_{bc} has also been reported for amplifier design [82] and VCO design [83]. This inductor can resonate out the C_{bc} (or C_{gd} in CMOS) so as to improve the balanced amplifier's gain and VCO's phase noise. Nevertheless, the cancelling effect greatly relies on the Q-factor of the on-chip inductor and the cancellation is only effective around the resonating frequency. More importantly, a DC blocking capacitor in series with the inductor is needed for correct biasing, and this large capacitor might introduce

more parasitic coupling.

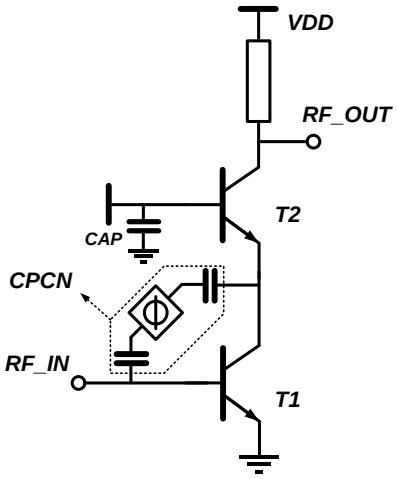


Figure 5.1: The proposed cascode stage.

This section proposes a gain enhanced cascode topology by connecting a passive compensation network in parallel with C_{bc}. of T_1. As shown in Figure 5.1, the compensation network consists of a passive phase inverter with two capacitors connected to its two different terminals. Their capacitances are the same and are slightly smaller than $2C_{bc1}$. It is demonstrated that by using this new Capacitor-Phase inverter-Capacitor Network (CPCN), the gain performance of single cascode stage can be enhanced in a wide bandwidth without penalty on noise figure and stability. To evaluate the usability, a cascode stage utilizing the new passive compensation network is implemented in a 0.13 µm BiCMOS process.

5.2 Analysis and Comparison of MAG/MSG

5.2.1 Maximum Available Gain With and Without Miller-Effect

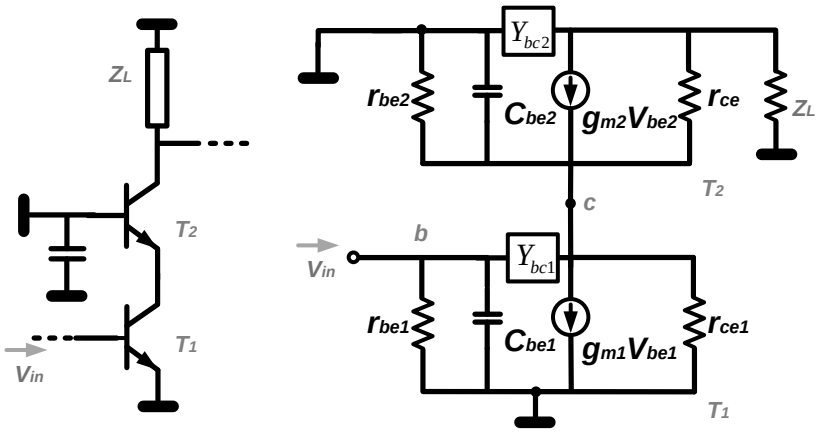


Figure 5.2: Hybrid-π model of cascode stage with considering base-collector capacitor.

The following discussions and investigations are based on cascode topologies since cascode topology demonstrates a potential to obtain higher gain than common emitter topology under the same biasing conditions. The common base HBT (T_2) can provide a low resistive load for the common-emitter HBT (T_1), so as to reduce the gain of T_1 and greatly desensitize the cascode performance from Miller-capacitance, C_{be1}. Nevertheless, the Miller-effect on the input tuning network still exists and the elimination of detuning is not perfect. More specifically, C_{bc1} cannot be totally offset by T_2 in the cascade; T_2 can only provide a high isolation between the output node and this Miller-capacitor. And C_{bc1} still exhibits negative behaviors such as loading the output node of T_1 and decreases gain, detunes the output tank and can even cause instability of T_1. As such, a theoretical analysis is conducted based on the HBT models in Figure 5.2. Using KVL and KCL, we find that the gain of

the single stage can be expressed as (5.1):

$$|A_V| = \left| \frac{g_{m1} - Y_{bc1} \cdot \left(g_{m2} + r_{ce2}^{-1} \right) Z_L}{g_{m2} + Y_{bc1} + r_{ce1}^{-1} + r_{ce2}^{-1} + Z_{be2}^{-1} \cdot Y_{bc2} Z_L + Z_L / r_{ce2} + 1 - Z_L / r_{ce2} \left(g_{m2} + r_{ce2}^{-1} \right)} \right| \quad (5.1)$$

where Z_{be1} and Z_{be2} denote the base-emitter impedance of T_1 and T_2 respectively. C_{be} is the base–emitter junction capacitance, C_{bc} is the base–collector junction capacitance, and Z_L is the load impedances. As shown in equation (5.1), the Y_{bc1} terms in both the numerator and the denominator are negative. Therefore, the cancellation of this C_{bc1} will result in an enhanced gain of the cascode stage. In the absence of C_{bc1}, the new gain expression can be expressed as equation (5.2):

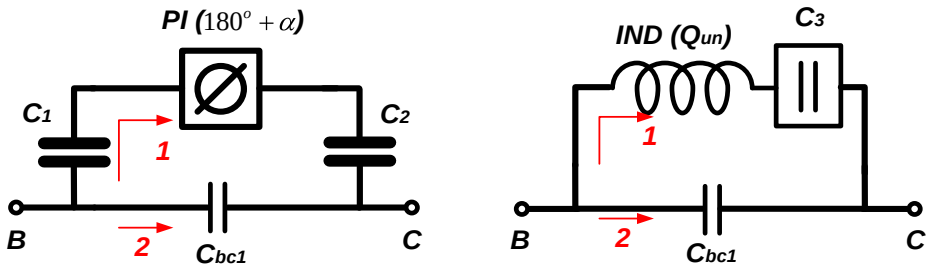
$$|A_V|_b = \left| \frac{g_{m1} \cdot \left(g_{m2} + r_{ce2}^{-1} \right) Z_L}{g_{m2} + r_{ce1}^{-1} + r_{ce2}^{-1} + Z_{be2}^{-1} \cdot Y_{bc2} Z_L + Z_L / r_{ce2} + 1 - Z_L / r_{ce2} \left(g_{m2} + r_{ce2}^{-1} \right)} \right| \quad (5.2)$$

5.2.2 Description of the Compensation Network

As shown in Figure 5.1, the CPCN consists of a passive phase inverter connected in series with two capacitors with capacitance value around $2C_{bc1}$. The phase inverter belongs to a pure passive network and can introduce 180 degree phase shift in a wide bandwidth. The two capacitors, C_1 and C_2, with value of $2C_{bc1}$ in series will result in a total capacitance of C_{bc1}. One of the reasons that we use two capacitors in series is due to the parallel strip topology of the phase inverter (as will be shown in Section 5.3) which needs DC blocking at both terminals. Another reason is that a larger capacitance results

in better immunity from process variation. Ideally, the whole CPCN is equivalent to a negative capacitor with an absolute value of C_{bc1}.

5.2.3 Miller-Capacitance Cancelling Effect Caused by Non-ideality



(a) (b)

Figure 5.3: Equivalent circuit between the base and collector of T1: (a) CPCN (b) Inductor parallel resonating network.

Given in Figure 5.3 are the equivalent passive circuits connected between the base and collector of T_1. To derive the two-port Y-matrix of the networks between node b and c, an ABCD matrix is adopted in the analysis. The ABCD matrix of the CPCN network can be presented as equation (5.3):

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{a1} = \begin{bmatrix} \cos(180^o+\alpha)+Z_{C_n}\cdot jY_0\sin(180^o+\alpha) & 2Z_{C_n}\cdot\cos(180^o+\alpha)+j\sin(180^o+\alpha)(Y_0\cdot Z_{C_n}^2+Z_0) \\ jY_0\sin(180^o+\alpha) & Z_{C_n}\cdot jY_0\sin(180^o+\alpha)+\cos(180^o+\alpha) \end{bmatrix} \quad (5.3)$$

Hence the admittance matrix between nodes b and c can be derived as:

$$Y_{bc\ a} = Y_{bc\ a1} + Y_{bc\ a2}$$

$$= \frac{-1}{2Z_{C_n}\cdot\cos(180^o+\alpha)+j\sin(180^o+\alpha)(Y_0\cdot Z_{C_n}^2+Z_0)} + Y_{C_{bc}} \quad (5.4)$$

where α denotes the phase error of the phase inverter, Q_{un} denotes the unloaded quality factor, and Z_{Cn} denotes the impedance of capacitors C_1 or C_2. If the phase inverter is ideal (α = 0º), from equation (5.4) we get $[Y_{bc}]_a = 0$.

For case (b), the compensation network consists of an inductor in series with a DC blocking capacitor, C_3. The capacitor C_3 is assumed to be ideal (large enough and loss less) and it can be ignored in AC signal response. Hence, the *ABCD* matrix can be expressed as:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix}_{b1} = \begin{bmatrix} 1 & R_L + jX_L \\ 0 & 1 \end{bmatrix} \tag{5.5}$$

where R_L and X_L are the impedance and reactance of the inductor respectively.

$$\begin{aligned} Y_{bc\ b} &= Y_{bc\ b1} + Y_{bc\ b2} \\ &= \frac{Q_{un}}{(1+Q_{um}^2)\cdot X_L} + j\left(\frac{X_L / Q_{un}}{(X_L / Q_{un})^2 + X_L^2} + B_{C_{bc}} \right) \end{aligned} \tag{5.6}$$

where Q_{un} denotes the unloaded quality factor.

If the inductance resonates with C_{bc1} at frequency ω, then

$$\omega = 1 \Big/ \sqrt{1 + 1/Q_{un}\ \ LC_{bc}} \tag{5.7}$$

It should be noted that the $[Y_{21}]_b$ still has the real part $Q_{un}/[(1+Q_{un}^2)\cdot X_L]$ in the first term in equation (5.6). This indicates that by using an inductor for C_{bc} cancellation, it also introduces parasitic resistances in the feedback loop.

By applying equations (5.4) and (5.6) into equation (5.1) respectively, the gain of the two different cascode stages can be estimated. If we define the equivalent collector-base capacitance after cancellation by networks (a) and (b)

in Figure 5.3 as $(C_{bc})_a$ and $(C_{bc})_b$ respectively, they can be used to evaluate the C_{bc} cancelling effect. Using a SiGe HBT, with emitter length of 0.13 μm, emitter width of 6.8 μm and biasing current of 4.0 mA connected with the above two different compensation networks, $(C_{bc})_a$ and $(C_{bc})_b$ are estimated by simulation and the results are shown in Figure 5.4.

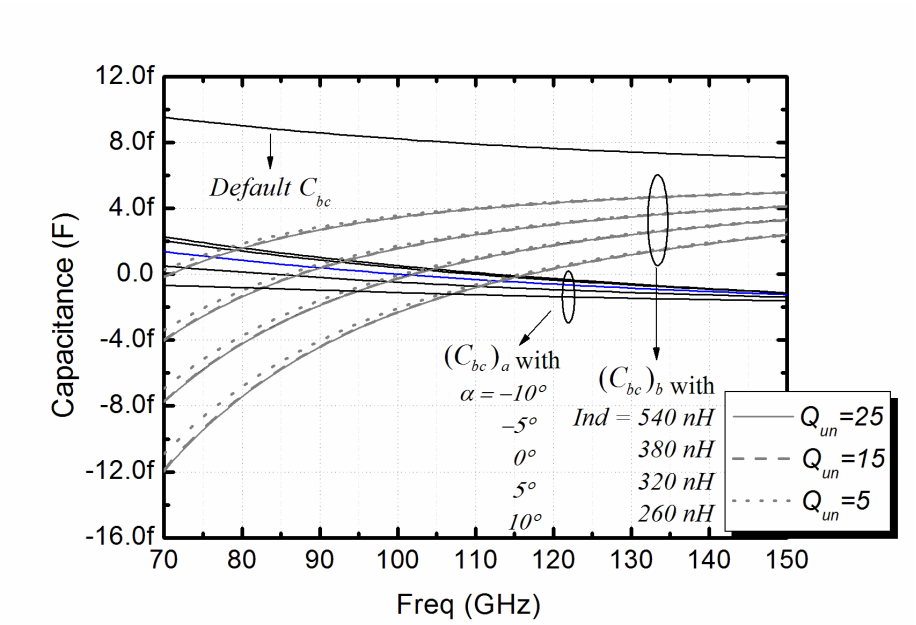


Figure 5.4. Comparison of the simulated C_{bc} among default Cascode, inductor parallel-resonating Cascode and Cascode with a CPCN.

As shown in Figure 5.4, the default C_{bc} is around 8.0 to 10 *f*F from 70 to 150 GHz. It is observed that C_{bc} decreases gradually with increasing frequency. With the use of a CPCN, $(C_{bc})_a$ can be reduced to a value of ± 0.8 *f*F if the phase error is zero. Furthermore, $(C_{bc})_a$ can track the frequency response of the default C_{bc} well. If α increases to −10º, $(C_{bc})_a$ could have a larger variation, from −0.7 *f*F@150 GHz to 2 *f*F@70 GHz. In addition, another method using parallel-resonating inductor is also evaluated. Four inductors, with inductance

of 260 pH, 320 pH, 380 pH and 540 pH with unloaded Q factors (Q_{un}) of 5, 15 and 25 are utilized to cancel the default C_{bc} respectively. The simulation results revealed that $(C_{bc})_b$ changes from inductive to capacitive rapidly with increasing frequency. Good cancellation only occurs at the specified resonating frequency points. More specifically, $(C_{bc})_b$ with a Q_{un} of 5 inductor demonstrated a slightly flatter response as compared to $(C_{bc})_b$ with using a Q_{un} of 15 inductors as well as a Q_{un} of 25 inductors. Herein, the capacitance cancelling bandwidth, defined by the frequency range at which C_{bc} has 10 % variation, is denoted as $\mathrm{BW}_{\pm 10\%}$. $\mathrm{BW}_{\pm 10\%}$ is approximately 51 GHz using CPCN ($\alpha=0$) while around 14 GHz using inductor cancelling (320 pH, Q_{un}=25). This indicates that the CPCN can achieve about 3.6 times $\mathrm{BW}_{\pm 10\%}$ of the parallel-resonating inductor. Furthermore, it should be noted that the C_3 in Figure 5.3 (b) cannot be ideal in the real implementation. The large area required for the capacitor and parasitic coupling exists between the large patterns in the layout could introduce more parasitic coupling and further deteriorate its effectiveness.

Meanwhile, as shown in Figure 5.4, the $(C_{bc})_a$ is below 2 fF for using a CPCN network even though α is as high as ±10º. Considering that α = 10º is equivalent to the phase shift of a transmission line with length = 52 μm and Z_o=50 Ω at 90 GHz in this process. This also reveals that the CPCN cancellation has a good tolerance for process violation.

5.2.4 Performance Change Brought by the CPCN

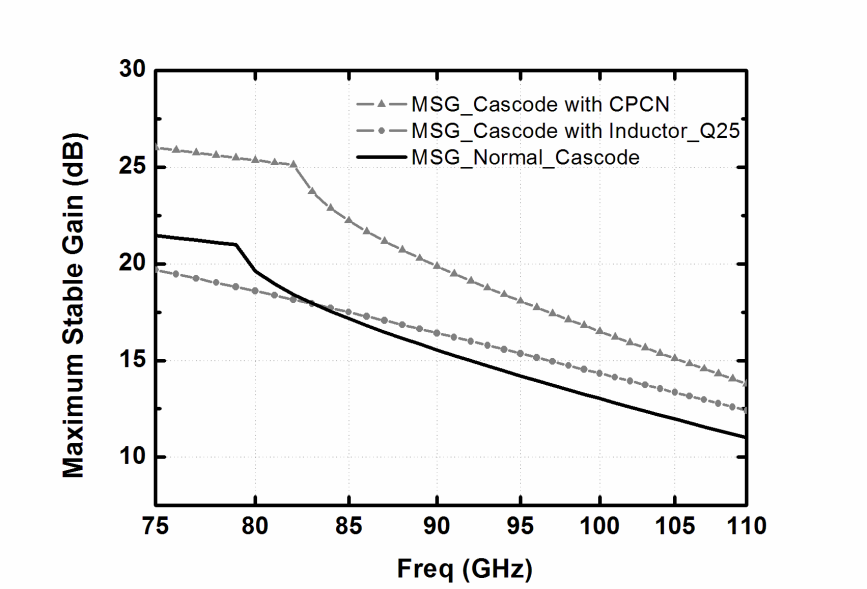


Figure 5.5: Comparison of the simulated MSG of three topologies - Normal Cascode, Cascode using a parallel-resonating inductor (*Ind* = 320 pH, Q_{un} = 15) and Cascode with a CPCN (Passive phase inverter + two 16.9 *f*F MIM capacitors).

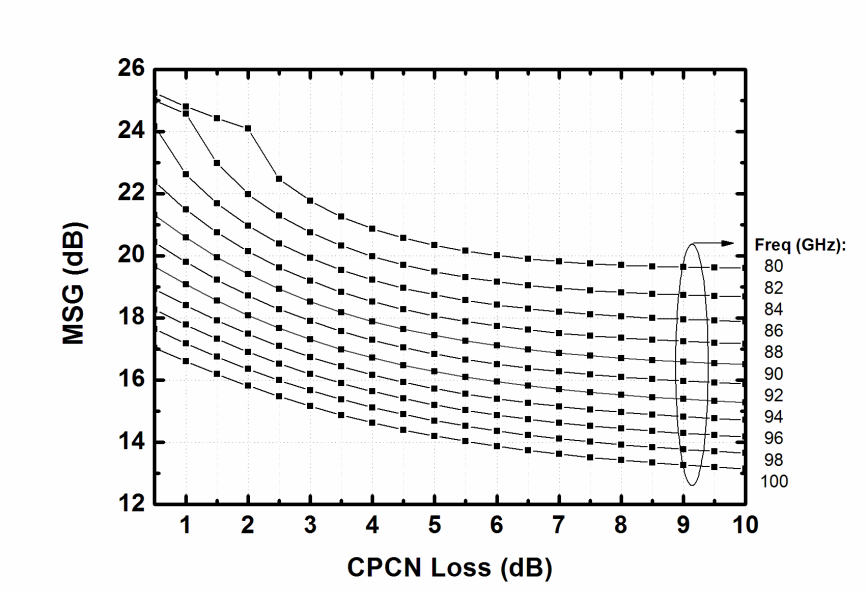


Figure 5.6: Simulated MSG of the Cascode with a CPCN changes with the CPCN loss for frequency from 80 - 100 GHz.

The MSG of three cascode topologies are simulated and compared in Figure 5.5. The cascode using a parallel-resonating inductor demonstrates slightly higher gain than normal cascode at frequencies above 83 GHz. In the mean time, the cascode with a CPCN can achieve a higher MSG in the whole frequency range as compared with the normal cascode. For instance, the MSG can be enhanced by around 3.5 dB at 75 GHz and 2.2 dB at 110 GHz. Also, this MSG is considerably larger than the cascode using a parallel-resonating inductor which introduces 5 dB more MSG at 75 GHz and 1.3 dB more MSG at 110 GHz. The passive loss is of concern for millimeter-wave circuits design and it may deteriorate the circuit performance greatly. The influence of CPCN loss on the gain enhancing performance is estimated by simulation. As shown in Figure 5.6, the MSG decreases with increasing CPCN loss increasing and saturates when CPCN loss further increases to 10 dB. Intuitively, this phenomenon can be interpreted as the feedback effect fades if CPCN loss increases. This reduces the effectiveness in cancelling C_{bc}. Moreover, by analyzing the simulation results at 90 GHz, if the CPCN loss can be maintained below ~ 6.5 dB, the cascode with a CPCN can demonstrate superior gain than a normal cascode. This suggests a wide boundary condition for CPCN use since the total loss introduced by the phase inverter and capacitors in the CPCN are typically below 3 dB according to the measurement results.

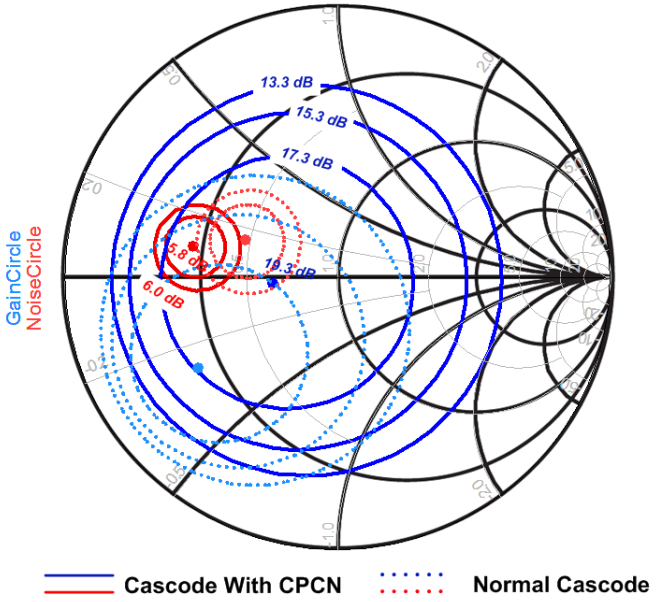


Figure 5.7: Gain circle and noise circle for input matching

Besides the gain improvement brought by the CPCN network, the noise figure of the cascade stage could also be influenced. The primary RF noise sources in bipolar transistors are base-current and collector current shot noise and base resistance induced thermal noise. It should be noted that the CPCN is a pure passive network that will not introduce additional noise source except for a minor conductor loss. This loss is a common phenomenon in other passive components and inter-connections. Thick top metal layers or parallel metal layers can be used for the CPCN network implementation to minimize the loss. Therefore, based on the noise figure expression in [42], the noise figure of the cascode can be presented as:

$$F = F_{\min} + \frac{R_n}{G_s}\left[(G_s - G_{opt})^2 + (B_s - B_{opt})^2\right] \tag{5.8}$$

where

$$NF_{\min} \cong 1 + \frac{g_m}{g_o^2}\left(\frac{1}{R_P} + \frac{g_m}{\beta}\right) + \frac{g_m^2}{g_o^2}\sqrt{2g_m r_b}\sqrt{\frac{1}{g_m^2}\left(\frac{g_o^2}{\beta} + \frac{1}{R_P{}^2}\right) + \left(\frac{f}{f_T}\right)^2}$$

$$g_o = g_m - 1/R_P$$

$$R_P = R_{cond} + \frac{1}{(2\pi f)^2 (C_{bc})_{default}{}^2 R_{cond}}.$$

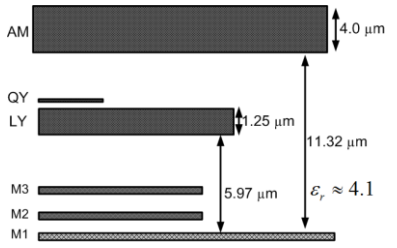
β is current gain, r_b is the base resistance, g_m is the transconductance and R_{cond} is the conductor loss.

The cancellation of C_{bc} can improve NF_{min} through f_T boosting. In this case, the noise figure change is similar to the amplifier with a parallel resistive feedback. From simulation, the NF_{min} using the CPCN is around 5.8 dB @ 90 GHz which is 0.25 dB higher than normal cascode. The simulation setup is the same as the previous equivalent capacitance estimation. Besides a slight increase of NF_{min} due to the conductor loss, the factors that may influence the amplifier noise figure significantly are the source Conductance (G_s) and Susceptance (B_s) change. It is well known that the noise figure and gain of the first stage have an equal contribution to the total amplifier noise figure, and the source reflection coefficient (Γ_s) is usually chosen so that the gain performance and noise figure are balanced. As shown in Figure 5.7, the optimum noise and gain reflection coefficient approach each other by the cascode using a CPCN, which is an extra benefit of the CPCN. Moreover, the gain circle expands considerably, which could bring about more tolerance for simultaneous matching. The above phenomenon is similar to the method of

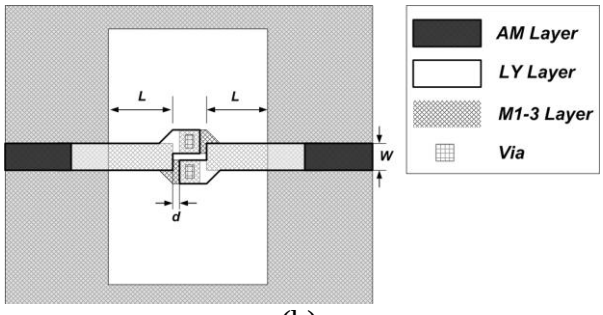
simultaneous noise and gain matching using common source parallel feedback (CSPF) in [84]. In summary, the final achievable *NF* is determined by both the optimization of the input matching network and the optimization of the three-dimensional structure of the CPCN.

Meanwhile, the cancellation of C_{bc} can also enhance stability. Reverse isolation of T_1 is increased due to the cancellation of C_{bc} which could enhance stability based on the well-known Rollet Stability Factor criterion. From simulation, the *K* factor of cascode with a CPCN is considerably higher than a normal cascode. This observation tallies with the cancelled C_{bc} and increased reverse isolation.

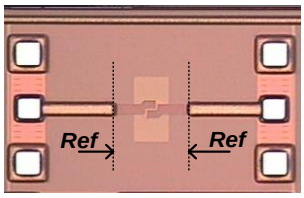
5.3 Implementation of the Phase Inverter and Cascode Stage



(a)



(b)



(c)

Figure 5.8: (a) Back-End-of-Line detail of the process; (b) Passive phase inverter structure; (c) Micro-photograph.

The detail of back-end-of-line in this process is depicted in Figure 5.8 (a). This process offers two thick metal layers (*AM, LY*) and three thin-metal layers (M_1–M_3). The top 4 µm thick metal layer (*AM*) is employed for signal lines and the 0.4 µm thick bottom metal layer (M_1) is used for the ground plane. The height from M_1 to *AM* is around 11.32 µm.

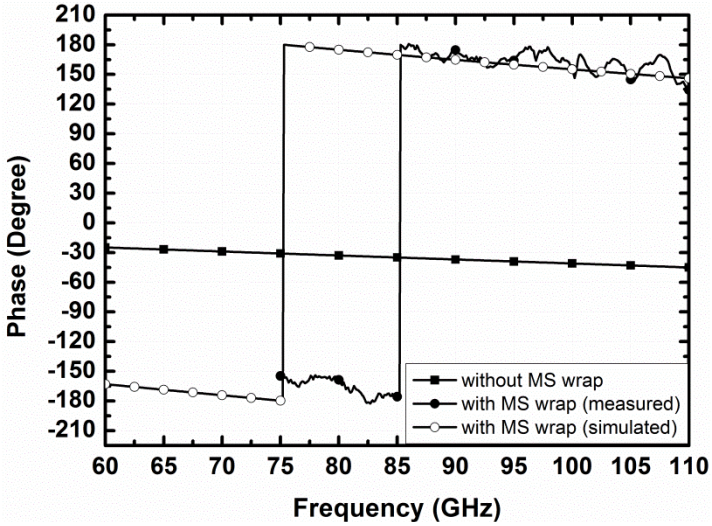


Figure 5.9. Phase responses of the phase inverter and through microstrip line without swap.

Until now, various passive phase inverters have been reported [85]-[87]. Among them, we have chosen a topology that consumes minimal chip area. The structure of the passive phase inverter is shown in Figure 5.8 (b). Basically, the 180^o phase shift is realized by inter-changing the signal line and ground line of the two encountered parallel strip lines through via holes. Then,

the parallel strip line is transformed to microstrip line. As shown in Figure 5.8 (b), *W* decides the reflection coefficient and can influence the matching impedances. *L* is optimized to compromise the consumed area and the bandwidth of the phase inverter. The minimum *d* is constrained by the fabrication precision. Previously, this Parallel-strip phase inverter has been used in microstrip filter design on PCB [86], [87]. This structure is proven to be able to implement phase inverting in a wide bandwidth on the silicon substrate. The micro-photograph of the phase inverter has been shown in Figure 5.8 (c). 1.25 µm thick *LY* layer is used for the signal line (top line) while M_1-M_3 are stacked by vias and used for ground line (bottom line). Thru-short de-embedding method was used to de-embed the effects of the interconnections and G-S-G pads outside the reference planes [80]. The measured phase shift of this phase inverter is shown in Figure 5.9. More than 18 GHz (from around 79 - 97 GHz) BW $\alpha_{=\pm 10^{o}}$ is obtained by the phase inverter. The measured insertion loss of this phase inverter is around 1.9 dB around W-band. The higher loss might be because the low loss top metal layer (AM) is not used for the phase inverter design due to the minimum spacing requirement of AM layer in this process.

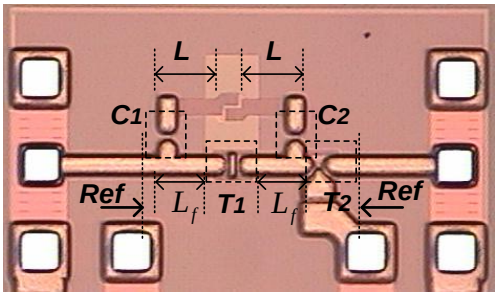


Figure 5.10. Micrograph of the proposed Cascode stage.

TABLE 5.1: Design Values of the New Cascode

T_1/ T_2	C_1/C_2	W	L_f	L
130 nm×6.8µm	16.9 fF	16.4 µm	42 µm	48 µm

Figure 5.10 depicts the architecture of the fabricated *CPCN* using the prescribed phase inverter. C_1 and C_2 have the same value as $2C_{bc1}$. Two additional feed lines, L_f, are added between the input and output of the T_1 to compensate the phase shift caused by L. The transmission line between T_1 and T_2 are formed using metal in AM layer. T_1 and T_2 sizes are both 2 × 3.4 μm × 0.13 μm. The cascode stage is biased with a supply voltage of 1.5 Volts and a biasing current of around 4 mA. Since a minor part of the base-collector capacitance is due to the parasitic coupling between base and collector feed lines, transistor shielding [73] is used for both T_1 and T_2 to reduce this somewhat un-predictable effect. The whole structure is optimized in the full-wave 3-D electromagnetic High Frequency Structure Simulator (ANSIS HFSS).

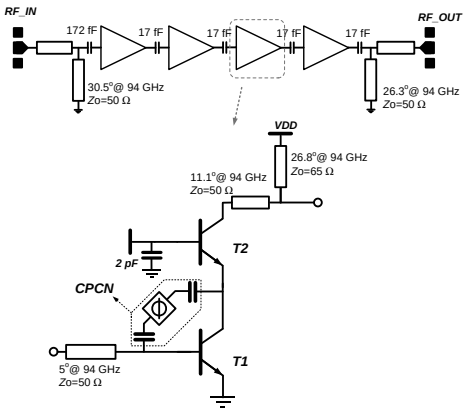


Figure 5. 11. Schematic of a cascaded amplifier using the new cascode stage.

A four-stage cascaded amplifier is designed utilizing the proposed cascode stages in W-band as shown in Figure 5. 11. The inter-stage matching networks consist of shunt transmission lines in series with capacitors. The source impedances of all the stages are matched for low noise while the output matching network is designed for maximum gain performance. The Γ_L of the former stage and Γs of the following stage are adjusted to be almost in the same resistive circle in the Smith chart so as to avoid the long series transmission line in the matching networks. The design was targeted for around 7 GHz BW to make sure the band is in the gain-enhanced frequency range. To obtain higher simulation accuracy, all the passive transmission lines, capacitors, phase inverters and shielding structures were evaluated together in ANSYS HFSS. Parasitics in the HBTs and surrounding passive connections are evaluated through Assura RC extraction and post layout simulation.

5.4 Measurement Results

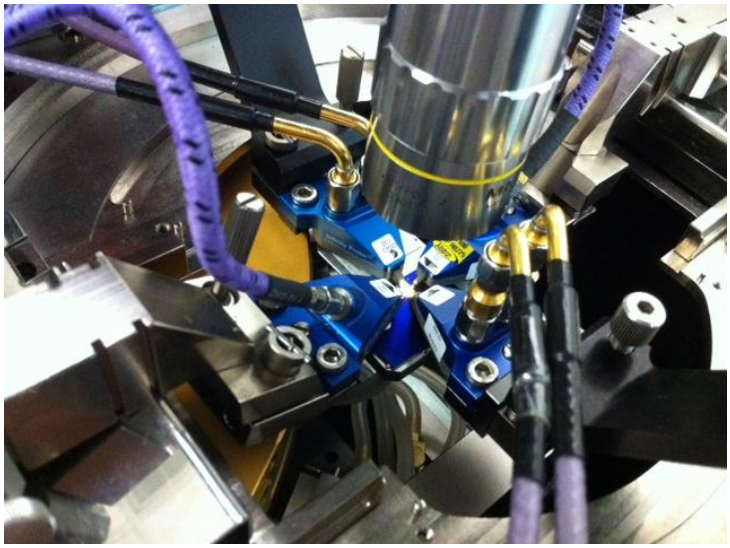


Figure 5.12: Measurement setup for the new cascode characterization.

Shown in Figure 5.12 is the measurement setup for the cascode stage characterization. On-wafer measurements of S-parameters were performed using Cascade Infinity 100-µm ground-signal-ground (G-S-G) probes on both R&S ZVA 50 extended 110-GHz VNA system and Anritsu ME7808B extended 110-GHz Vector Network Analyzer (VNA) system. Calibration was carried out using a line-reflect-reflect-match (LRRM) calibration technique with WinCal software and Impedance Standard Substrate (ISS) supplied by Cascade Microtech. W-Band bias tees are used to provide the biasing voltage for the cascode stage characterization. The same de-embedding method is used as aforementioned.

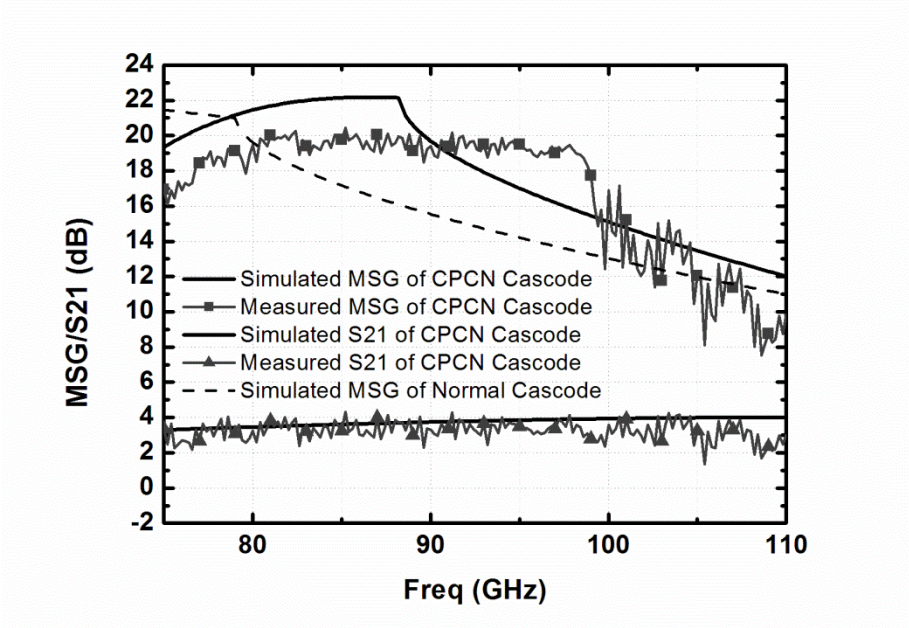


Figure 5.13: Simulated and measured maximum stable gain of the new Cascode stage.

The measured and simulated MSG and S21 are shown in Figure 5.13. It is observed that the cascode stage is able to achieve maximum stable gain above 19 dB from 80 to 97 GHz. For frequency below 80 GHz, the maximum gain

reduces gradually. This is because the feedline with length of L is designed to be small to save area, which limits the phase precision of the phase inverter at low frequencies. The MSG of the normal cascode is also simulated to compare with the proposed cascode. The proposed cascode demonstrated superior gain over the conventional topology from 81 GHz to above 100 GHz. For example, it can increase by more than 2 dB the MSG at 85 GHz and 5 dB the MSG at 97 GHz. However, besides the MSG of the single stage, the amplifier gain that can be achieved also depends on the choice of the matching network design strategy (matching for noise, gain or bandwidth of the amplifier), and loss of external passive elements.

The amplifier achieves a noise figure of 7.3 - 8 dB from 83 GHz to 91 GHz with around 1.5 V × 16 mA power consumption. The measured peak gain by this noise measurement system is around 36 dB which is higher than VNA measurement. The reason for the 2 dB gain difference in the two different types of the measurement might be because the VNA system is not able to be calibrated with enough low input power (normally around -20 dBm) to guarantee that the LNA is not saturated. To make a fair comparison of cascode stages, TABLE 5.2 outlines the performance of cascode amplifiers operating around W-band including this amplifier and other previously published state-of-the-art amplifiers working at similar bands and fabricated in processes with similar f_T. Overall, using a supply voltage as low as 1.5 V, this amplifier achieved a peak gain of 34.2 dB and a minimum noise figure of around 8.0 dB without introducing distinct penalty on noise figure and stability.

TABLE 5.2: Performance of Cascode Amplifiers Round W-Band

Ref	Technology	Peak Gain (dB)	Topology	3 dB Bandwidth (GHz)	Noise Figure (dB)	Power Consumption (mW)	VDD (V)
[16]	65 nm CMOS	27 @ 88 GHz	5 CAS	75 - 89	6.8-10	43.2	1.2
[55]	65 nm CMOS	25.3 @ 117.5 GHz	4 CAS	87 - 100	6-8.3	96	1.7
[56]	65 nm CMOS	13.5 @ 81 GHz	3 CAS	75 - 88.5	6.4-8.4	47	1.5
[88]	0.18 µm SiGe BiCMOS	19.5 @ 83 GHz	2 differential CAS	76.4 - 85.3*	N.A	1325	3.2
[12]	0.13 µm SiGe BiCMOS	14 @ 89 GHz*	3 differential CAS	86 - 93*	N.A.	119.8	3.3
[89]	90 nm CMOS	17.4 @ 91 GHz	3 CAS	86 - 108	N.A	54	2.5
[90]	0.18 µm SiGe BiCMOS	14.5 @ 77 GHz	Cascode + CE	65 - 85	< 8	37	3.3/1.5
[91]	45 nm CMOS SOI	12 @ 84 GHz	2 CAS	75 - 90*	N.A	122*	2
This Work	**0.13 µm SiGe BiCMOS**	**34.2 @ 86.2 GHz**	**4 CAS with CPCN**	**83 - 91**	**7.3 - 8.0**	**24**	**1.5**

* Estimated from description or measured graph.

5.5 Conclusion

This chapter proposes a cascode stage for millimeter-wave operation using a new Miller-capacitor cancelling method. The proposed compensation networks, CPCN, can eliminate the Miller-effect and enhance the gain performance in a wide bandwidth. The gain-enhanced bandwidth of the new cascode can be extended if more area can be consumed for the phase inverter implementation. A four stage amplifier design based on this cascode stage demonstrated good gain and noise performance for millimeter-wave operation. This CPCN also has a potential to be used in the other building blocks that need to minimize Miller-effect.

CHAPTER 6

Conclusions

Due to the high operating frequency and limited performance of current silicon processes, millimeter-wave amplifiers and related system designs have encountered a lot of challenges. In this thesis, the study was mainly aimed to develop high efficiency and high power millimeter-wave CMOS PAs and high gain W-band BiCMOS LNAs. State-of-the-art performances were obtained using new circuit techniques which are beneficial for the current millimeter-wave systems.

6.1 60-GHz CMOS Power Amplifier Design

This thesis proposes an intuitive guidance to simplify the design of feedback network in a millimeter-wave differential amplifier based on Y-parameter network analysis. The criterion of judging unilateralization has been analyzed and verified by a 60 GHz power amplifier in 90 nm CMOS process. Moreover, it has been found that the PA working status can vary from weak to intermediate neutralization, then unilateralization, and, finally, over-neutralization by increasing the value of neutralization capacitor.

Based on the deep-neutralized differential amplifying pairs, another PA fabricated in 65 nm CMOS process uses a band-tunable circuit to adapt to different channels (according to the millimeter-wave physical-layer specification in IEEE Standard 802.15.3c) in use, whereas high gain and high efficiency can be achieved in a narrow bandwidth by high-Q matching and deep neutralization. The amplifier can provide high gain and high efficiency for each individual channel rather than try to obtain such performance over the whole band. Based on this concept, the fabricated band-tunable PA in 65-nm CMOS technology shows an ability to change the peak gain from 59.0 to 53.5 GHz. The maximum output power is 12.3 dBm in the high-frequency band. The peak PAE is 20.4% with 17.1-dB gain and 17.2% with 16.2-dB gain for high- and low-frequency bands, respectively. Compared to the 60 GHz PAs using distributed-active-transformers (DAT), this PA can obtain higher PAE since less power is dissipated on the passive power-splitting and combing networks. On the other hand, compared with 60 GHz PAs using advanced process (for instance: silicon-on-insulator (SOI) CMOS processes), the cost of this power amplifier is lower as the proposed PA topology is process-independent. Since the four channels in IEEE Standard 802.15.3c are not used simultaneously, thus the 20 % PAE achieved by this PA is the highest among all 60 GHz PAs in the real usage based on normal CMOS process. Although this PA has already achieved the 10 dBm output power requirement of IEEE Standard 802.15.3c, the main limitation of this proposed PA topology is the relatively lower output power compared with DAT-based PA. If the millimeter-wave PA is used in the other applications with higher output power

requirement, the band-tunable architecture together with DAT-based power-combining output stage can be utilized to achieve a balance between PAE and output power.

6.2 W-band Low Noise Amplifier Design

The W-band LNA is a key part in the W-band total power radiometer which dominates the system noise figure (NF) and gain. Through the system analysis, the dynamic ranges in imaging systems need to be shifted to lower power levels compared to communication systems. Therefore, much excessive power can be saved for RF blocks through lower biasing current. A 94 GHz LNA design with gain of 45 dB and noise figure of 7.2 dB at 94 GHz and bandwidth of above 20 GHz is demonstrated. For the first time, gain boosted cascode and SC-GCPW are used in the W-Band LNA to achieve high gain and low noise performance for imaging applications. Meanwhile, elaborate layout design techniques including cascode shielding structure, lossy inter-stage matching, reverse isolation shielding walls and DC biasing tubes are used for the stability enhancement. This is the first W-band LNA obtaining above 45 dB gain on silicon which can greatly reduce the $NE\Delta T$ of total power radiometer. One possible drawback of this LNA design is the low output power since it is aimed for the low-power level imaging application. Thus, this output power may not be enough for communication system applications. However, through sizing of the later stages and increasing of biasing current, the output power can be increased and high gain can be maintained by the gain-boosting technique.

A new millimeter-wave gain boosting method utilizing passive compensation network is also developed. This technique can help increase the gain performance through Miller-effect cancellation and will not penalise the noise figure and stability performance. The cancelling effect at low frequency is limited and restricted by the provided chip area. Also, the model precision of the transistor and passive connection are important to the success of this technique. Diligence is needed for the optimization of these passive connections. It is promising to develop high performance amplifier, oscillator or the other building blocks based on the proposed Miller-effect cancellation method.

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