INGAAS N-MOSFETS WITH CMOS COMPATIBLE SOURCE/DRAIN TECHNOLOGY AND THE INTEGRATION ON SI PLATFORM

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2013

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(B.Eng.(Hons.), NTU

A THESIS SUBMITTED

FOR THE DEGREE OF DOCTOR OF PHILOSOPHY

NUS GRADUATE SCHOOL FOR INTEGRATIVE SCIENCES AND ENGINEERING

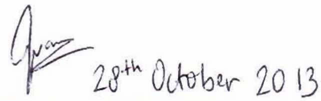
NATIONAL UNIVERSITY OF SINGAPORE

2013

Declaration

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.



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Acknowledgements

The works in this thesis would have been impossible without the support and contribution of many individuals in many ways.

First and foremost, I would like to thank my research advisor, Dr. Yeo Yee Chia, for his advice and guidance throughout my graduate study at NUS. I have benefited immensely from his invaluable technical insight, knowledge, and experience shared. I would also like to thank him for his time and effort in guiding this thesis.

I would like to thank my co-advisor, Dr. Pan Jisheng from Institute of Materials Research and Engineering (IMRE-A*STAR). He has always been there to give his instrumental advice and I have learned a lot through numerous discussions with him.

I am very grateful to have constructive support from many outstanding researchers and graduate students of Silicon Nano Device Laboratory (SNDL). Special thanks to Eugene Kong, Gong Xiao, Goh Kian Hui, Guo Huaxin, Dr. Samuel Owen, Sujith Subramanian, Zhang Xingui, Dr. Zhou Qian, and Zhu Zhu for their tremendous contribution in the works of this thesis. Dr. Zhou Qian's time and effort in providing TEM service on blanket samples are gratefully acknowledged. Special thanks also go to Dr. Pan Jisheng, Dr. Foo Yong Lim, and Dr. Zhang Zheng, I have benefited greatly from their vast experience in material characterization. I would also like to thank the team from NTU, Prof. Yoon Soon Fatt, Dr. Loke Wan Khai, Dr. Satrio Wicaksono, and Dr. Tan Kian Hua for their

technical contribution as well as effort in the growth of substrates used in some of the works in this thesis. Without them, the works of this thesis would be impossible.

I would like to acknowledge technical staffs of IMRE who have provided services such as SIMS, XRD, HRTEM, and TEM on patterned samples. In addition, I would like to acknowledge Dr. Rinus Lee from SEMATECH for the useful discussions and material characterization supports given in some of the collaboration works.

To friends of SNDL, Guo Pengfei, Low Kain Lu, Phyllis Lim, Yang Yue, Zhan Chunlei, and many others, I am very grateful for their earnest help, useful discussions, and friendship throughout the journey. In addition, I would also like to extend my appreciation to technical staffs of SNDL, Mr. O Yan Wai Linn, Mr. Patrick Tang, and Ms. Yu Yi for their help in one way or another.

Finally, I would also like to extend my deepest gratitude to my mum, dad, brother, and Welly who have been very supportive, caring, and encouraging throughout my academic endeavors.

Table of Contents

Acknowledgements ii

Table of Contents iv

Summary viii

List of Tables x

List of Figures xi

List of Symbols xxi

Chapter 1

Introduction

1.1 Background 1

1.2 Key Challenges of InGaAs MOSFETs 4

1.2.1 Poor Interface Quality of InGaAs Gate Stack..5

1.2.2 Issues Related to The Scaling of InGaAs Transistors..6

1.2.3 Lack of S/D Contact Technology Compatible with Si CMOS 7

1.2.4 Issues Related to Heterogeneous Integration of InGaAs Transistors on Si Platform 12

1.3 Research Objectives 14

1.4 Thesis Organization..14

Chapter 2

CoInGaAs as a Novel Self-Aligned Metallic Source/Drain Material for Implant-less $In_{0.53}Ga_{0.47}As$ n-MOSFETs

2.1 Introduction 16

2.2 CoInGaAs Contact Metallization Module: CoInGaAs Formation, Extraction of Contact Resistivity, and Selective Wet-Etch Process Development 17
2.2.1 CoInGaAs Formation 17
2.2.2 Extraction of Contact Resistivity 22
2.2.3 Selective Wet-Etch Process Development 26
2.3 Device Integration and Characterization 34
2.4 Summary 40

Chapter 3

Material Characterization of Ni-InGaAs as a Contact Material for InGaAs Field-Effect Transistors

3.1 Introduction 41
3.2 Photoelectron Spectroscopy Study of Band Alignment at Interface between Ni-InGaAs and InGaAs 43
3.2.1 Sample Preparation and Methodology 43
3.2.2 Work Function and Band Alignment Extraction 46
3.3 Crystal Structure and Epitaxial Relationship of Ni-InGaAs Films formed on InGaAs by Annealing 54
3.3.1 Sample Preparation 54
3.3.2 Ni-InGaAs Formation: Anneal Conditions, Elemental Composition, Material Structure and Thickness Ratio of Ni to Ni-InGaAs 55
3.3.3 Ni-InGaAs Sheet Resistance Uniformity and Bulk Resistivity 68
3.4 Summary 72

Chapter 4

N-Channel InGaAs Field-Effect Transistors on Germanium-on-Insulator Substrates with Self-Aligned Ni-InGaAs Source/Drain

4.1 Introduction 73

4.2 Extraction of Contact Resistivity 74
4.3 InGaAs n-MOSFETs with Ni-InGaAs as Self-Aligned S/D material 77
4.4 InGaAs n-MOSFETs Formed on Germanium-on-Insulator on Si Substrate 84
4.5 Pt Incorporation in Ni-InGaAs Metallization 90
4.6 Summary 96

Chapter 5

Process Development for InGaAs-based Transistor and Laser Integration on GeOI on Si Substrates

5.1 Introduction 97
5.2 Design Concept 100
5.2.1 Layer Structure of Substrate for Transistor-Laser Integration 100
5.2.2 Device Layout Structure for Transistor and Laser Co-Integration 103
5.2.3 Device Fabrication Process Flow of the InGaAs-based n-MOSFETs and QW Lasers 105
5.3 Electrical Performance of $In_{0.7}Ga_{0.3}As$ Transistors Fabricated on Grown Substrate for Transistor-Laser Integration 113
5.4 Impact of Growth Defects on The Electrical Performance of InGaAs transistor 122
5.5 Summary 131

Chapter 6

Conclusion and Future Works

6.1 Conclusion 133
6.2 Contributions of This Thesis 134
6.2.1 CoInGaAs as a Novel Self-Aligned Metallic Source/Drain Material for Implant-less $In_{0.53}Ga_{0.47}As$ n-MOSFETs 134

6.2.2 Material Characterization of Ni-InGaAs as a Contact Material for InGaAs Field-Effect Transistors 135
6.2.3 N-Channel InGaAs Field-Effect Transistors on Germanium-on-Insulator Substrates with Self-Aligned Ni-InGaAs Source/Drain ..135
6.2.4 Process Development for InGaAs-based Transistor and Laser Integration on GeOI on Si Substrates 136
6.3 Future Directions 136

References...139

Appendix

List of Publications 168

Summary

Over the past few decades, scaling of Si transistors have contributed to advances in semiconductor technology. Further improvements in the drive current of Si transistors will soon be hindered by the fundamental limits imposed by the material properties of Si. InGaAs is a potential n-channel material for future high-performance CMOS applications for sub-11 nm technology nodes. This is mainly due to its low electron effective mass (m^*) and high electron mobility. However, several technical challenges related to the lack of source/drain (S/D) contact technology compatible with Si CMOS and heterogeneous integration of InGaAs transistors on Si have to be overcome in order to take full advantage of its high mobility benefit. Even if these problems are addressed, physical limitations of the conventional metal interconnects are among other problems to be solved.

In this thesis, self-aligned metallization of InGaAs analogous to silicidation is explored. The reaction of Co and Ni with InGaAs to form M-InGaAs (M = Co or Ni) ohmic contact to n-type InGaAs was investigated. Selective wet etching process for the removal of Co or Ni over M-InGaAs was also developed. InGaAs n-MOSFETs with self-aligned M-InGaAs S/D were successfully demonstrated. The transistors exhibit good electrical characteristics. The results verify that silidice-like metallization concept can be adopted for InGaAs transistors.

This thesis also addresses challenges related to heterogeneous integration of InGaAs transistors on a Si platform. InGaAs n-MOSFETs were successfully

integrated on GeOI on Si substrate by employing molecular beam epitaxy (MBE) through a graded-buffer growth approach. The InGaAs n-MOSFETs on GeOI on Si substrate have intrinsic transconductance value that compares very well with other reported state-of-the-art InGaAs transistors. This thesis demonstrates the feasibility of integrating InGaAs n-MOSFETs on Si substrate. Finally, this thesis presents research efforts directed towards realizing electronic-photonic device co-integration on Si platform as one possible solution to the bandwidth limitation of metal interconnect. Some key challenges associated with the co-integration of InGaAs-based transistors and lasers on GeOI on Si substrate were addressed. The work enables realization of InGaAs-based transistor and laser device at the intra-chip level.

List of Tables

Table 2.1. Etch selectivity of Co over CoInGaAs in various etchants...............34
Table 3.1 Comparison between Ni-InGaAs and CoInGaAs. 72

List of Figures

Fig. 1.1 (a) Schematic illustrating the source-to-drain leakage ($I_{SD,leak}$) and gate leakage (I_G) of a transistor. (b) Band diagram across the channel from source to drain of a transistor with long (black lines) and short (dashed lines) L_G. The drain voltage (V_{DS}) affects the potential barrier ($q\Phi_B$) at the source end of transistor with small L_G, resulting in barrier lowering. E_c, E_{Fermi}, and E_v represent the conduction band, Fermi level, and valence band, respectively. 2

Fig. 1.2 Electron effective mass of $In_xGa_{1-x}As$ versus indium composition [3]. m_o is the free electron mass. 4

Fig. 1.3 Schematic illustrating key challenges faced by InGaAs MOSFETs. 4

Fig. 1.4 Plot of $R_{S/D}/R_{Total}$ versus gate length L_G for an advanced III-V transistor. The data point for L_G = 50 nm is from the reported experimental data in Ref. [31] taken at V_{DS} and V_{GS} of 0.5 V, while the rest of the data points were projected by the author by keeping $R_{S/D}$ constant and scaling the channel resistance in proportion to L_G. 8

Fig. 1.5 Schematic of a InGaAs transistor with non-self-aligned S/D contacts, showing the various resistance components in a device. R_c, $R_{n\text{-}doped}$, and $R_{channel}$ are the contact resistance, the resistance of the n-doped source or drain, and the channel resistance, respectively. x_j is the S/D junction depth and l is the distance between the contact pad and the channel. 9

Fig. 2.1. An illustration of self-aligned silicidation-like metallization for InGaAs transistor, which involves the reaction of a deposited metal (M) with InGaAs forming a metallic material (denoted as M-InGaAs) in the S/D region and the removal of the unreacted metal. 17

Fig. 2.2. TEM images of CoInGaAs formed by annealing 20 nm of Co on $In_{0.53}Ga_{0.47}As$ at (a) 300 ºC, (b) 350 ºC, and (c) 400 ºC. Most of the as-deposited Co remained unreacted at 300 ºC. In contrast, at 350 ºC, the entire Co layer reacted with InGaAs to form a CoInGaAs layer. Energy Dispersive X-ray Spectroscopy (EDX) was performed at various spots in the CoInGaAs film formed at 350 °C, indicated by the spots labeled 1 to 4. After annealing Co on $In_{0.53}Ga_{0.47}As$ at 400 ºC, a CoInGaAs layer with non-uniform thickness and a rough interface was formed. 19

Fig. 2.3. EDX reveals the elemental atomic percentage found in localized spots at various parts of the CoInGaAs film formed at 350 °C, as indicated in Fig. 2.2(b). The EDX spot size is ~10 nm. It is observed that the CoInGaAs film comprises a Co- and Ga-rich layer on top of a Co- and As-rich layer. 20

Fig. 2.4. Grazing angle XRD spectra of Co on $In_{0.53}Ga_{0.47}As$ samples as-deposited and annealed at 300, 350 and 400 °C. The presence of CoGa and CoAs phases were observed in 350 and 400 °C CoInGaAs film. The XRD characterization was carried out through an external service contract in IMRE. 20

Fig. 2.5. Sheet resistance R_{sh} measured after annealing 20 nm of Co on $In_{0.53}Ga_{0.47}As$ at various temperatures ranging from 200 to 350 °C for 60 s. The R_{sh} of the sample annealed at 350 °C is that of the CoInGaAs film. The dashed line indicates the R_{sh} of as-deposited Co. 22

Fig. 2.6. Schematics illustrating process flow for forming TLM structures, featuring mesa formation, formation of Co metal pads, and CoInGaAs formation. 23

Fig. 2.7. (a) Top-view optical microscope image of TLM structure with various contact spacings. This structure was used for the extraction of contact resistance and specific contact resistivity. (b) *I-V* curves obtained from a TLM structure with CoInGaAs metal contacts formed at 350 °C, showing ohmic behavior on n^+-$In_{0.53}Ga_{0.47}As$. (c) Contact resistance R_c and (d) specific contact resistivity of Co and CoInGaAs formed on n^+-$In_{0.53}Ga_{0.47}As$...25

Fig. 2.8. R_{sh}^{-1} versus etch time t of Co and CoInGaAs films in various chemical solutions. R_{sh} was recorded after each etch duration.........28

Fig. 2.9. Co and CoInGaAs thickness (t_f) versus etch time (t) in various chemical solutions...29

Fig. 2.10. Etch rate of Co and CoInGaAs films in various etchants. The gray and black symbols are the etch rate of Co and CoInGaAs, respectively. 29

Fig. 2.11. R_{sh} versus t (a-d) and the corresponding Co and CoInGaAs thickness (t_f) versus t (e-h) in various concentrations of HNO_3 solution. R_{sh} was recorded after an etch duration. 31

Fig. 2.12. Etch rate of Co and CoInGaAs films in various concentrations of HNO_3 solutions. The black open and solid symbols are the etch rate of Co and CoInGaAs, respectively. The HNO_3:H_2O ratio of 1:100, 1:50, 1:20, and 1:10 correspond to the molarity of 0.16, 0.31, 0.78, and 1.57 M, respectively. 33

Fig. 2.13. Process flow for forming $In_{0.53}Ga_{0.47}As$ n-MOSFET with self-aligned CoInGaAs metallic S/D. The schematics show the key process steps, including Co deposition, reaction with InGaAs, and selective Co removal. 35

Fig. 2.14. Cross-sectional TEM images of $In_{0.53}Ga_{0.47}As$ MOSFET with CoInGaAs metallic S/D formed using 350 °C 60 s anneal. Annealing ~10 nm of Co formed 28-35 nm of CoInGaAs. The inset shows a zoomed-in view of the $TaN/Al_2O_3/In_{0.53}Ga_{0.47}As$ gate stack. The physical thickness of the Al_2O_3 gate dielectric is ~6 nm. 36

Fig. 2.15. CoInGaAs/p-$In_{0.53}Ga_{0.47}As$ junction shows rectifying behavior. Voltage was applied to the CoInGaAs while the InP substrate was grounded. 37

Fig. 2.16. (a) I_{DS}-V_{GS} curves of a $In_{0.53}Ga_{0.47}As$ n-MOSFET with self-aligned CoInGaAs S/D. G_m is referred to the right axis. (b) I_{DS}-V_{DS} plot for the same $In_{0.53}Ga_{0.47}As$ n-MOSFET. Gate overdrive V_{GS}-V_{TH} is varied from 0 to 2.5 V in steps of 0.5 V. (c) Series resistance of transistors with conventional non-self-aligned S/D and CoInGaAs self-aligned S/D. 39

Fig. 3.1. Schematics showing the preparation process of Ni-InGaAs samples....44

Fig. 3.2. Transmission electron microscopy (TEM) images of (a) thin and (b) thick Ni-InGaAs formed on $In_{0.53}Ga_{0.47}As$ substrate. (c) The high resolution image shows periodic arrangement of atoms in Ni-InGaAs layer, demonstrating good crystalline quality. 45

Fig. 3.3. Schematic showing incoming photon causing photoemission of electron from a sample. Depending on the photon *hv* energy, free-electron near valence band (VB) down to core-level can be emitted....47

Fig. 3.4. He I (*hv* = 21.2 eV) UPS spectra of thick Ni-InGaAs formed on $In_{0.53}Ga_{0.47}As$. A -5 V bias was applied to the Ni-InGaAs layer. Fermi edge position was determined as the center of the slope as indicated by vertical line. Secondary electron cut-off position was determined from the intercept of the slope with the background level (horizontal gray line). 48

Fig. 3.5. He I (*hv* = 21.2 eV) UPS spectra of as-formed, after Ar sputter, and after complete oxide removal of thick Ni-InGaAs formed on $In_{0.53}Ga_{0.47}As$. A -5 V bias was applied to the Ni-InGaAs layer. The maximum difference in the spectra width is 0.37 eV. 49

Fig. 3.6. Normalized XPS core-level spectra of (a) As 3d for bulk Ni-InGaAs (bottom) and $In_{0.53}Ga_{0.47}As$ (top) samples. Comparison of (b) In $3d_{5/2}$, (c) Ga $2p_{3/2}$, and (d) As 3d from Ni-InGaAs/$In_{0.53}Ga_{0.47}As$ interface sample (bottom) and from bulk $In_{0.53}Ga_{0.47}As$ (top). The red and blue fitted curves correspond to signal coming from Ni-InGaAs and $In_{0.53}Ga_{0.47}As$, respectively. The In $3d_{5/2}$, Ga $2p_{3/2}$, and As 3d peaks at the interface resides 0.75 eV higher than that of $In_{0.53}Ga_{0.47}As$ substrate determined by the difference between the blue fitted curves. 50

Fig. 3.7. Schematics of energy band diagram showing interface dipole (dotted band) or Fermi level pinning could lead to a high electric field at the NiInGaAs-InGaAs interface. The band alignment of Ni-InGaAs in contact with $In_{0.53}Ga_{0.47}As$ substrate is consistent with XPS results. 53

Fig. 3.8. *I-V* characteristics measured between Ni-InGaAs pad and Au back-side contact to InP of a diode structure (inset). The dimension of Ni-InGaAs pad area is 100 μm×100 μm. The Ni-InGaAs/p-$In_{0.53}Ga_{0.47}As$ junction shows rectifying behavior. 54

Fig. 3.9. Sheet resistances R_{sh} of Ni-on-InGaAs samples annealed at various temperatures for a fixed time of 60 s. The inset shows an illustration of the formation of Ni-InGaAs (bottom) by annealing as-deposited Ni-on-InGaAs (top) at temperature *T* for time *t*. 56

Fig. 3.10. Negative ion Secondary Ion Mass Spectrometry (SIMS) depth profiles of Ni, In, Ga, and As for ~11 nm Ni on InGaAs (a) before and (b) after annealing at 200 °C for 60 s. The dotted lines represent the region where Ni and InGaAs could have intermixed even before annealing. (c) Ni, In, Ga, and As positive ion SIMS depth profiles of Ni-InGaAs formed at 250 °C for 60 s. The Ni-InGaAs/InGaAs interface is represented by dotted line. 58

Fig. 3.11. XRD General Area Detector Diffraction System (GADDS) integrated diffraction intensity as a function of 2θ (left). TEM images showing the thicknesses of films formed at 250, 300, and 350 ºC (right). 60

Fig. 3.12. (a) Time evolution of R_{sh} for ~28 nm of Ni deposited on InGaAs annealed at 250 °C. (b) Transmission electron microscopy (TEM) images of Ni-on-InGaAs annealed at 250 °C for (i) 10 s, (ii) 20 s, and (iii) 30 s. 60

Fig. 3.13. X-ray Photoelectron Spectroscopy (XPS) spectra of (a) Ni $2p_{3/2}$, (b) In $3d_{5/2}$, (c) Ga $2p_{3/2}$, and (d) As 3d. The elemental

composition of Ni-InGaAs was determined from the area under the fitted peaks (blue lines) excluding the Ga oxide peak. 62

Fig. 3.14. (a) TEM image of Ni-InGaAs/InGaAs sample where selective area diffraction (SAD) pattern shown in (b) was recorded. The SAD aperture, as indicated by a circle, has a diameter of 150 nm. (c) High resolution TEM image of Ni-InGaAs/InGaAs with insets showing the corresponding diffraction patterns extracted by Fast Fourier Transform. (d) Unit cell of Ni-InGaAs phase, illustrating the NiAs (B8) structure of Ni-InGaAs. 63

Fig. 3.15. X-ray pole figure (left) and the corresponding phi-scan (right) of Ni-InGaAs and InGaAs obtained from (110) and (220) diffraction planes. 65

Fig. 3.16. TEM images of (a) ~29 nm as-deposited Ni on InGaAs, and (b) ~49 nm, (c) ~39 nm and (d) ~21 nm of Ni-InGaAs formed by annealing ~29 nm, ~21 nm and ~12 nm of as-deposited Ni on InGaAs, respectively...67

Fig. 3.17. Plot of Ni-InGaAs thickness versus as-deposited Ni thickness, showing a linear relationship. The thickness ratio of ~1 : 1.7 for Ni to Ni-InGaAs is obtained by linear fitting. Thicknesses of Ni-InGaAs and Ni were determined from TEM images. 67

Fig. 3.18. Contour plot of sheet resistance of ~46-nm-thick Ni-InGaAs film in a 1 mm × 1 mm area as obtained by microscopic four-point probe. In the scale bar (top right), sheet resistance values range from 20.5 Ω/square to 22.5 Ω/square, with an interval of 0.5 Ω/square. A schematic diagram (bottom right) shows the microscopic four-point probe with probe spacing of ~10 μm used for R_{sh} measurement. 69

Fig. 3.19. (a) R_{sh} of Ni and Ni-InGaAs as a function of thickness. (b) The electrical resistivity of Ni and Ni-InGaAs extracted from their R_{sh} values and thicknesses. The thickness of Ni-InGaAs is obtained by multiplying the as-deposited Ni thickness and the thickness ratio (1.7) of Ni to Ni-InGaAs. 70

Fig. 4.1. (a) Schematics of TLM test structure fabrication featuring mesa formation, Ni-InGaAs formation, and thick Ni metal pads deposition. (b) Optical microscope image showing the top view of the fabricated TLM test structure. *L* and *Z* are the length and width of Ni-InGaAs metal pad, respectively, while *d* is the distance between two adjacent metal pads. 76

Fig. 4.2. (a) *I-V* curves obtained from a TLM test structure with Ni-InGaAs metal contacts formed at 250 °C, showing ohmic

behavior on n-$In_{0.53}Ga_{0.47}As$. (b) Total resistance versus Ni-InGaAs contact spacing determined from the *I-V* curves. 77

Fig. 4.3. Process flow and schematics of the key process steps in the fabrication of $In_{0.53}Ga_{0.47}As$ n-MOSFETs with self-aligned Ni-InGaAs metal S/D. 79

Fig. 4.4. (a) I_{DS}-V_{GS} and I_G-V_{GS} characteristics of a $In_{0.53}Ga_{0.47}As$ n-MOSFET with self-aligned Ni-InGaAs S/D. The gate length and gate width are 2 μm and 100 μm, respectively. The gate current is referred to the right axis. (b) I_{DS}-V_{DS} characteristics for the same $In_{0.53}Ga_{0.47}As$ n-MOSFET at gate overdrive V_{GS}-V_{TH} from 0 to 2.5 V in steps of 0.5 V. 80

Fig. 4.5. Total resistance (R_{Total} = V_{DS}/I_{DS}) as a function of gate voltage of the same device as in Fig. 4.4. I_{DS} is the drain current in the linear regime (V_{DS} = 0.1 V). Higher applied gate voltage causes the channel resistance to reduce which leads to a reduction in the total resistance of the device. The resistance at high V_{GS} gives the $R_{S/D}$ value. 81

Fig. 4.6. Extrinsic transconductance $G_{m,ext}$ of the same device as in Fig. 4.4 at V_{DS} of 0.1 and 1.1 V. 83

Fig. 4.7. Process flow used in this experiment, including the growth of InGaAs-on-GeOI and the fabrication of n-channel InGaAs metal oxide semiconductor field-effect transistor (MOSFET). Schematics on the right illustrate the self-aligned metallic S/D formation scheme employed in the fabrication of transistor on the MBE grown substrate. 85

Fig. 4.8. Cross-sectional TEM image of InGaAs-on-GeOI structure with $In_{0.7}Ga_{0.3}As$ channel n-MOSFET fabricated on it (left). High-resolution TEM image of the $In_{0.7}Ga_{0.3}As$ n-MOSFET with self-aligned Ni-InGaAs metallic S/D (right). 86

Fig. 4.9. (a) I_{DS} versus gate overdrive (V_{GS}-V_{TH}) of an n-MOSFET with $In_{0.7}Ga_{0.3}As$ channel and Ni-InGaAs metallic S/D at V_{DS} = 0.1 and 1.2 V. The gate length of the device is 2 μm and the gate width is 100 μm. Transconductance $G_{m,ext}$ characteristic is referred to the right axis. The peak $G_{m,ext}$ at V_{DS} = 1.2 V is 138.5 μS/μm. (b) Log (I_{DS}) and (I_G) versus V_{GS}-V_{TH} of the same device at V_{DS} = 0.1 and 1.2 V (c) I_{DS}-V_{DS} plot of the same device at various gate overdrives (V_{GS}-V_{TH}) from 0 to 2.5 V. (d) Series resistance of InGaAs n-MOSFET with Ni-InGaAs source/drain is compared with other reported series resistance of InGaAs n-MOSFETs 87

Fig. 4.10. Normalized peak transconductance $G_m.t_{ox}$ is plotted as a function of gate length (L_G). Device performance obtained in

this work (black solid symbols) is compared with those reported in other $In_xGa_{1-x}As$ channel n-MOSFETs in the literature (gray solid symbols for $x = 0.7$, open symbols for $x = 0.53$). Note that data from Ref. [17],[116]-[117] are extrinsic G_m, while those from the other references are intrinsic G_m. The G_m data are from various V_{DS}: $V_{DS} = 0.5$ V for Ref. [116], $V_{DS} = 1$ V for Refs. [17],[110],[117], $V_{DS} = 1.1$ V for Ref. [111], $V_{DS} = 1.2$ V for Ref. [43] and this work, and $V_{DS} = 2$ V for Refs. [10],[112]-[115]. $G_m.t_{ox}$ obtained in this work is significantly higher than those of $In_{0.53}Ga_{0.47}As$ MOSFETs fabricated on Si (open circles) [110]. The connecting dashed lines act only as a guide. 89

Fig. 4.11. XPS depth profiling across co-sputtered NiPt film. Pt concentration is ~15 at%, uniformly distributed in the film. The XPS characterization was done in IMRE through service contract...91

Fig. 4.12. **(a)** Sheet resistances R_{sh} of NiPt (blue symbols) and Ni (black symbols) on p-type InGaAs samples annealed at various temperatures for a fixed time of 60 s. (b) Surface roughness of the annealed NiPt and Ni on InGaAs. The as-deposited NiPt and Ni films have similar RMS surface roughness of ~0.4 nm as represented by dotted lines. 92

Fig. 4.13. Surface morphology of (a) as-deposited Ni and NiPt films, (b) 250 °C annealed Ni and NiPt films, (c) 500 °C formed NiPt-InGaAs and (d) Ni-InGaAs films in a 10 μm × 10 μm area obtained by AFM scan. The cross-section surface topology profile along section line A-A' is shown for 500 °C formed films. 94

Fig. 4.14. Cross-sectional TEM of NiPt on InGaAs annealed at 250, 400, and 500 ºC...95

Fig. 4.15. Contact resistivity ρ_c versus anneal temperature for NiPt-InGaAs and Ni-InGaAs on n-type InGaAs. Same doping concentration of ~2×10^{19} cm^{-3} was used for a fair comparison. 95

Fig. 5.1. An illustration of electronic and photonic device integrated system. The optical interconnect constitutes photonic devices such as laser diode, optical waveguide, and photodetector. Electrical output from transistor (e.g. of an inverter) is sent through a laser diode where the electrical signal is converted to optical signal. The optical signal is transmitted through a waveguide and received by a photodetector to convert the optical signal back to electrical signal that is received by transistor of another inverter at the other end. 99

Fig. 5.2. (a) Structure of epilayers grown on GeOI substrate for transistor-laser integration. (b) Transmission electron microscopy (TEM) image of the grown substrate. (c) Optical microscopy image showing the surface of the grown substrate where defects are observed. 101

Fig. 5.3. (Left) schematic showing the top view of a transistor-laser integrated circuit layout. The author involved in the discussion on the mask layout design although the drawing of the actual mask layout was not done by the author. Line A-A' and B-B' are cross-section along which the schematics in Fig. 5.4 and 5.6 were drawn. The corresponding symbols (right) illustrate the connection of the four transistors to a laser. 104

Fig. 5.4. Schematics showing transistor fabrication process flow. Schematics are drawn along line A-A' in Fig. 5.3.........................107

Fig. 5.5. Scanning electron microscopy (SEM) images showing a transistor after (a) gate formation, (b) Si implant and PdGe contact formation, (c) InGaAs mesa formation and SiO_2 removal on the gate pad. The completed transistor formation is shown in (d). 109

Fig. 5.6. Etch depth versus etch time of InAlAs buffer layer in HCl:H_2O = 3:1 solution. 110

Fig. 5.7. Schematics showing laser fabrication process flow, following the completed transistor formation (line A-A') in Fig. 5.4. The process steps of laser fabrication are drawn along line B-B' in Fig. 5.3. 112

Fig. 5.8. (a) I_{DS}-V_{GS} of $In_{0.7}Ga_{0.3}As$ channel n-MOSFET on transistor-laser integrated substrate obtained at V_{DS} = 0.1 and 1.2 V. The gate length of the device is 2 µm and the gate width is 100 µm. (b) Log (I_{DS}) versus V_{GS} of the same device at V_{DS} = 0.1 and 1.2 V. (c) I_{DS}-V_{DS} plot of the same device at various gate overdrives (V_{GS}-V_{TH}) from 0 to 2 V. 114

Fig. 5.9. Total resistance (R_{Total} = V_{DS}/I_{DS}) as a function of gate voltage of the same device as in Fig. 5.8. I_{DS} is the drain current in the linear regime (V_{DS} = 0.1 V). S/D series resistance $R_{S/D}$ of ~76.3 Ω is extracted at higher applied gate voltage when the channel is completely turned on and the total resistance is mainly contributed by S/D resistance. The normalized $R_{S/D}$ to the device gate width (W = 100 µm) is ~7.6 kΩ·µm. Inset shows the schematic of a non-self-aligned transistor where metal contact is l distance away from channel region. The l spacing of this device is 5 µm...115

Fig. 5.10. (a) I-V curves measured between two adjacent PdGe metal contacts with different contact spacing formed on n^+-InGaAs/InAlAs. (b) Plot of total resistance between two PdGe metal contacts as a function of the contact spacing. The intercept gives $2R_c$ of 35.1 Ω (also equals to 3.51 kΩ·μm). 117

Fig. 5.11. Extrinsic transconductance of the same device as in Fig. 5.8. 118

Fig. 5.12. Optical microscopy image of the fabricated transistors having large gate width (W = 720 μm). The transistors were fabricated by the author using the substrate illustrated in Fig. 5.2. 119

Fig. 5.13. I_{DS}-V_{GS} of a large-gate-width $In_{0.7}Ga_{0.3}As$ transistor measured at V_{DS} = 0.1, 1.2, and 2 V. The gate length of the device is 2 μm and the gate width is 720 μm. 120

Fig. 5.14. Statistical plot showing the distribution of drain current at gate overdrive (V_{GS}-V_{TH}) of 2.5 V and V_{DS} of 2 V. The drain current is in the range of 65 – 70 mA. The yield of the transistor fabrication is ~90%. ~50 transistors were measured for this plot. 120

Fig. 5.15. SEM image of a laser fabricated with non-optimized anisotropic dry etch recipe. Inset shows the rough mirror facet formed. 121

Fig. 5.16. Schematic of InGaAs device structure used in 2-D simulation. The thicknesses of Al_2O_3 and $In_{0.53}Ga_{0.47}As$ used in the 2-D simulation are 5 nm and 100 nm, respectively. The trap density used is 1×10^{22} cm^{-3}. 123

Fig. 5.17. I_{DS}-V_{GS} characteristics of 2-D simulated InGaAs transistors with the presence of (a) electron trap (acceptor characteristic), (b) hole trap (donor characteristic), and (c) electron and hole traps located at various energy positions. 124

Fig. 5.18. Potential diagram of InGaAs at 2 nm below channel surface from source to drain for transistor with (a) no trap, (b) electron trap (E_i+0.2 eV), (c) electron trap (E_i+0.3 eV), (d) hole trap (E_i), (e) hole trap (E_i-0.2 eV), and (f) electron (E_i+0.4 eV) and hole traps (E_i-0.05 eV, E_i+0.03 eV). 125

Fig. 5.19. Schematic of InGaAs device structure used in 3-D simulation. The thicknesses of Al_2O_3 and $In_{0.7}Ga_{0.3}As$ used in the 3-D simulation are 6 nm and 10 nm, respectively. The placement of traps to represent threading dislocation, dislocation segment, surface steps, and plane defect are illustrated. 127

Fig. 5.20. (a) Illustration of trap placement to model threading dislocations and dislocation segments. I_{DS}-V_{GS} characteristics of 3-D simulated InGaAs transistors with (b) threading

dislocations with varying spacing and (c) dislocation segments with varying length. 128

Fig. 5.21. (a) Illustration of trap placement of lines of surface steps and defect planes. I_{DS}-V_{GS} characteristics of 3-D simulated InGaAs transistors with various number of (b) lines of surface steps and (c) plane defects. 128

Fig. 5.22. I_{DS}-V_{GS} of $In_{0.7}Ga_{0.3}As$ transistors measured at V_{DS} = 0.1, 1.2, and 2 V. The gate length of the device is 2 µm and the gate width is 720 µm. Black and gray solid symbols are data obtained from transistor fabricated on InGaAs epilayer with defect density of $\sim 10^9$ cm^{-2} and $\sim 10^7$ cm^{-2}, respectively. 131

List of Symbols

Symbol	Description	Unit
C	Capacitance	F
C_{ox}	Oxide capacitance	F
d	Contact spacing	μm
d_{las}	Thickness of quantum well	nm
D_{it}	Interface trap density	$cm^{-2}eV^{-1}$
E_c	Conduction band	eV
$E_{cut-off}$	Binding energies of the secondary electron cut-off	eV
E_{CNL}	Charge neutrality level	eV
E_{Fermi}	Fermi level	eV
E_G	Bandgap	eV
E_v	Valence band	eV
G_D	Drain conductance	S
G_m	Transconductance (per unit width)	μS/μm
$G_{m,ext}$	Extrinsic transconductance (per unit width)	μS/μm
$G_{m,int}$	Intrinsic transconductance (per unit width)	μS/μm
h	Planck's constant	eV·s
I	current	A
I_{DS}	Drain current (per unit width)	μA/μm
I_G	Gate current (per unit width)	μA/μm
I_{off}	Off-state current (per unit width)	μA/μm
I_{on}	On-state current (per unit width)	μA/μm
$I_{SD,leak}$	Source-to-drain leakage current (per unit width)	μA/μm
I_{th}	Threshold current	A
J	Current density	A/cm^2
k	Boltzmann constant	eV/K
l	The distance between contact pad and channel	μm
l_{probe}	Distance between measurement probe and channel edge	μm
L	Length of metal pad	μm
L_G	Gate length	μm
L_{las}	Length of laser active layer	μm

L_T	Transfer length	μm
m^*	Carrier effective mass	kg
n	Carrier concentration	cm^{-3}
N_A	P-type doping concentration	cm^{-3}
N_D	N-type doping concentration	cm^{-3}
P_{off}	Standby power consumption	W
q	Electronic charge	C
$q\Phi_B$	Potential barrier	eV
r	Etch rate	nm/s
r_{Co}	Etch rate of Co	nm/s
$r_{CoInGaAs}$	Etch rate of CoInGaAs	nm/s
R	Resistance	Ω
R_c	Contact resistance	Ω
R_D	Drain resistance	Ω
R_{sh}	Sheet resistance	Ω/□
$R_{sh,InGaAs}$	Sheet resistance of n-InGaAs	Ω/□
$R_{n\text{-}doped}$	Resistance of n-doped source/drain	Ω
R_S	Source resistance	Ω
$R_{Si\text{-}doped}$	Resistance of Si-doped layer	Ω
$R_{S/D}$	Source/drain series resistance	Ω
R_{Total}	Total resistance	Ω
S	Etch selectivity	-
t	Time	s
t_f	Thickness of conductive film	nm
t_{Ni}	Ni thickness	nm
t_{NiPt}	NiPt thickness	nm
$t_{Ni\text{-}InGaAs}$	Ni-InGaAs thickness	nm
t_{ox}	Equivalent oxide thickness	nm
T	Temperature	K
V	Voltage	V
V_{dd}	Supply voltage	V
V_{DS}	Drain voltage	V
V_{GS}	Gate voltage	V

V_{TH}	Threshold voltage	V
W	Gate width	µm
W_{las}	Width of laser active layer	µm
x_j	Source/drain junction depth	nm
Z	Width of metal pad	µm
λ_m	Mean free path	m
μ	Carrier mobility	$cm^2\ V^{-1}s^{-1}$
μ_n	Electron mobility	$cm^2\ V^{-1}s^{-1}$
μ_p	Hole mobility	$cm^2\ V^{-1}s^{-1}$
ρ_c	Contact resistivity	$\Omega \cdot cm^2$
ρ_f	Resistivity of conductive film	Ω·nm
$\rho_{n\text{-}doped}$	Resistivity of n-doped source or drain region	Ω·nm
$\rho_{Ni\text{-}InGaAs}$	Resistivity of Ni-InGaAs	Ω·nm
τ_m	Mean free time	s
τ_{sp}	Carrier life time	s
v	Photon frequency	s^{-1}
Φ	Work function	eV
Φ_B^P	Hole barrier height	eV
Φ_B^N	Electron barrier height	eV

Chapter 1

Introduction

1.1 Background

For the past few decades, the continuous scaling down of Si-based complementary metal-oxide-semiconductor (CMOS) devices has enabled higher device packing density and on-state current performance. This exponential increase in the number of devices in an integrated circuit (IC) over time, enabled by the advancement of semiconductor technology, has kept the technology scaling trend in line with Moore's law [1]-[2]. However, with the aggressive scaling of Si transistors, further improvements in the on-state current I_{on} will soon be hindered by the fundamental limits imposed by the material properties of Si. Moreover, as the transistor gate length (L_G) is aggressively scaled to sub-hundred nanometer regime, high off-state leakage current (I_{off}) also becomes a major concern. The high off-state leakage current is contributed by source-to-drain leakage ($I_{SD,leak}$) and gate leakage (I_G) as illustrated in Fig. 1.1(a).

In a transistor with large L_G, carriers moving from source to drain see a potential barrier ($q\Phi_B$) at the source end [black line in Fig. 1.1(b)] that is influenced by the gate voltage (V_{GS}) but not the drain voltage (V_{DS}). However, as the gate length is shortened, the drain is close to the source and the V_{DS} influences

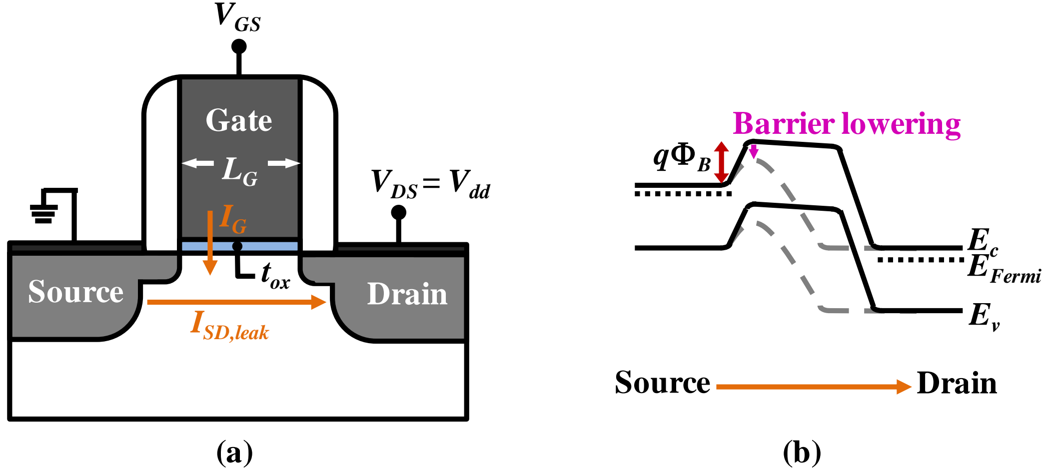


Fig. 1.1 (a) Schematic illustrating the source-to-drain leakage ($I_{SD,leak}$) and gate leakage (I_G) of a transistor. (b) Band diagram across the channel from source to drain of a transistor with long (black lines) and short (dashed lines) L_G. The drain voltage (V_{DS}) affects the potential barrier ($q\Phi_B$) at the source end of transistor with small L_G, resulting in barrier lowering. E_c, E_{Fermi}, and E_v represent the conduction band, Fermi level, and valence band, respectively.

the barrier at the source end. This results in a lower barrier seen by carriers moving from source to channel [dashed line in Fig. 1.1(b)], also known as drain induced barrier lowering (DIBL), which leads to higher $I_{SD,leak}$ for transistors with short L_G. Hence, as the gate length becomes shorter, the equivalent oxide thickness (t_{ox}) of the transistor needs to be reduced in order to achieve good gate control and suppress $I_{SD,leak}$. However, scaling of t_{ox} can lead to higher I_G.

The I_{off} contributes to high standby power consumption (P_{off}) as expressed by

$$P_{off} = I_{off} \times V_{dd}, \tag{1.1}$$

where V_{dd} is the supply voltage. As such, the benefit of scaling is offset by power loss due to high I_{off}. Fortunately, this tradeoff faced by the scaling of Si transistors can be resolved by using an alternative channel material with higher carrier

mobility, innovative device architectures, and high-k gate dielectric materials, so that I_{on} can be increased for a given I_{off}, or I_{off} can be reduced for a given I_{on}.

III-V materials such as $In_xGa_{1-x}As$ (also denoted as InGaAs) are very attractive as alternative channel materials as they have much higher electron mobilities than silicon, due to their very low electron effective mass. The high electron mobility of $In_xGa_{1-x}As$ makes it suitable for n-channel metal-oxide-semiconductor field-effect-transistors (MOSFETs) for future technology nodes. The dependence of carrier mobility (μ) in bulk materials on carrier effective mass (m^*) can be expressed using

$$\mu = \frac{q\tau_m}{m^*} = \frac{q\lambda_m}{\sqrt{3kTm^*}}, \tag{1.2}$$

where q is the electronic charge, τ_m is the mean free time, k is the Boltzmann constant, T is the temperature, and λ_m is the mean free path. Fig. 1.2 shows the electron effective mass of $In_xGa_{1-x}As$ as a function of indium concentration [3]. Electron mobility increases with higher indium composition due to reduction in the electron effective mass. However, to enable successful integration of $In_xGa_{1-x}As$ devices into Si-based CMOS technology, several key challenges have to be addressed.

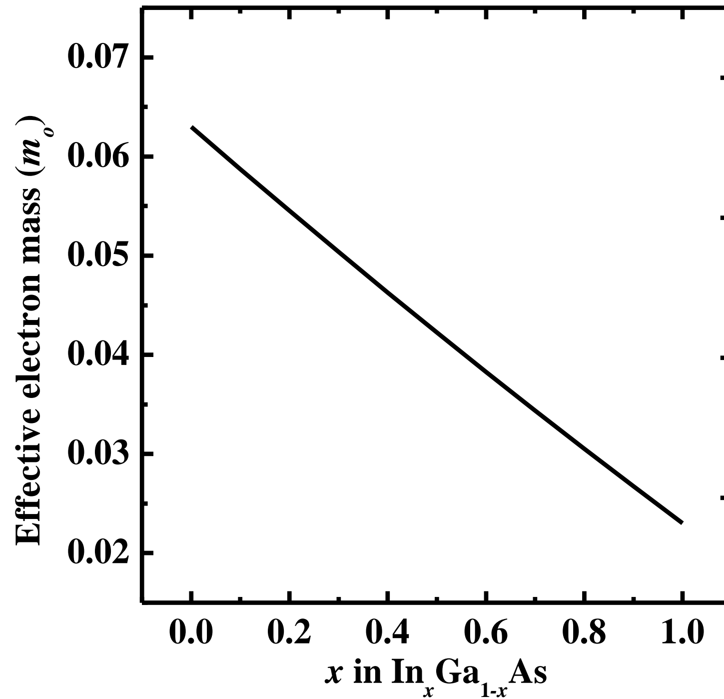


Fig. 1.2 Electron effective mass of $In_xGa_{1-x}As$ versus indium composition [3]. m_o is the free electron mass.

1.2 Key Challenges of InGaAs MOSFETs

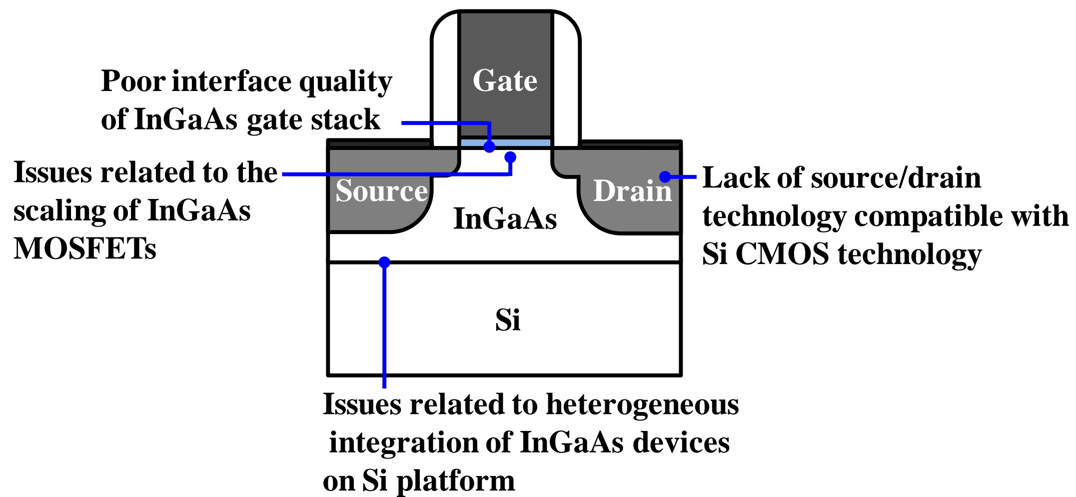


Fig. 1.3 Schematic illustrating key challenges faced by InGaAs MOSFETs.

Several key challenges [4] faced in the development of InGaAs MOSFET technology include (1) poor interface quality of InGaAs gate stack, (2) issues related to the scaling of InGaAs transistors, (3) lack of S/D contact technology compatible with Si CMOS, and (4) issues related to heterogeneous integration of InGaAs transistors on Si platform (Fig. 1.3). These are elaborated on in the following sub-sections.

1.2.1 Poor Interface Quality of InGaAs Gate Stack

A good gate stack is extremely important for InGaAs MOSFETs in order to benefit from the high carrier mobility of the channel material. The traps located near or at the interface between the gate dielectric and the channel act as trapping and scattering centers, degrading the mobility of carriers in the inversion layer of the channel. High interface trap density (D_{it}) also leads to undesired Fermi level pinning, resulting in poor gate control in the MOSFET.

Fortunately for Si, the quality of the gate stack is not a serious issue because of the high quality of the interface between Si native oxide (SiO_2) and Si. SiO_2 is thermodynamically stable, with a D_{it} as low as ~10^{10} cm^{-2}eV^{-1} at the SiO_2/Si interface [5]-[6]. Unfortunately for III-V materials such as InGaAs, their native oxides give rise to poor interface quality and are not suitable as gate dielectrics.

This has spurred intensive efforts to search for a gate dielectric/InGaAs stack that is as good as SiO_2/Si over the last few decades. The study of high-

k/InGaAs interfaces involving high-k dielectrics such as Gd_2O_3 [7], Ga_2O_3 [8]-[9], Al_2O_3 [10]-[11], HfO_2 [12], ZrO_2 [13], $ZrO_2/LaAlO_y$ [14], and Si_3N_4 [15] has been extensively reported. The use of passivation or interfacial layer techniques, such as sulfur passivation [16], phosphorus nitride passivation [17], InP interfacial layer [18], and Si interfacial layer [19]-[20] has also been well investigated. The purpose of the passivation or interfacial layer is to eliminate possible $In_xGa_{1-x}As$ native oxides formed before high-k dielectric deposition. Nevertheless, the best D_{it} of ~10^{12} $cm^{-2}eV^{-1}$ [16]-[22] reported so far is still considered too high. Further research on gate stack technology for InGaAs will be highly valuable, but will not be further discussed as the focus of this thesis is on the challenges outlined in sub-sections 1.2.3 and 1.2.4.

1.2.2 Issues Related to The Scaling of InGaAs Transistors

III-V transistors are projected to replace Si n-MOSFETs at the sub-11 nm technology nodes. As such, the scaling of III-V transistors needs to be as good as that of Si transistors. Issues such as short-channel effects (SCEs), which include DIBL, need to be effectively addressed for III-V transistors. Advanced device architectures such as ultra-thin body (UTB) and multi-gate device structures for InGaAs transistors have been proposed and used to counter these issues. The UTB structure can be used to suppress the source-to-drain leakage current by the insertion of a barrier layer below the ultra-thin channel layer [23]. The barrier layer can be a III-V material with a wide bandgap [23] or an insulator [24]. The multi-gate structure, on the other hand, can be used to obtain better gate control to

suppress SCEs, lower the source-to-drain leakage current, and increase the volume of the inversion layer in the channel. To date, many InGaAs transistors with advanced structures have been successfully demonstrated [25]-[30]. The successful realization of InGaAs transistors with advanced device structures will enable their adoption in future technology nodes.

1.2.3 Lack of S/D Contact Technology Compatible with Si CMOS

Whether InGaAs transistors will be adopted in future CMOS technology also depends on the achievement of high on-state drive current performance at V_{dd} lower than 0.5 V, and this requires low S/D series resistance. It is also desirable, from a manufacturing cost effectiveness viewpoint, for InGaAs S/D technology to be compatible with Si CMOS process.

Fig. 1.4 shows the contribution of S/D series resistance ($R_{S/D}$) to the total resistance (R_{Total}) of an advanced InGaAs transistor at various gate lengths (L_G). This figure shows that the contribution of $R_{S/D}$ to R_{Total} becomes significantly larger as the transistor is scaled. The large $R_{S/D}$ will become a serious concern if it is unoptimized, as it could limit the on-state performance of InGaAs transistors.

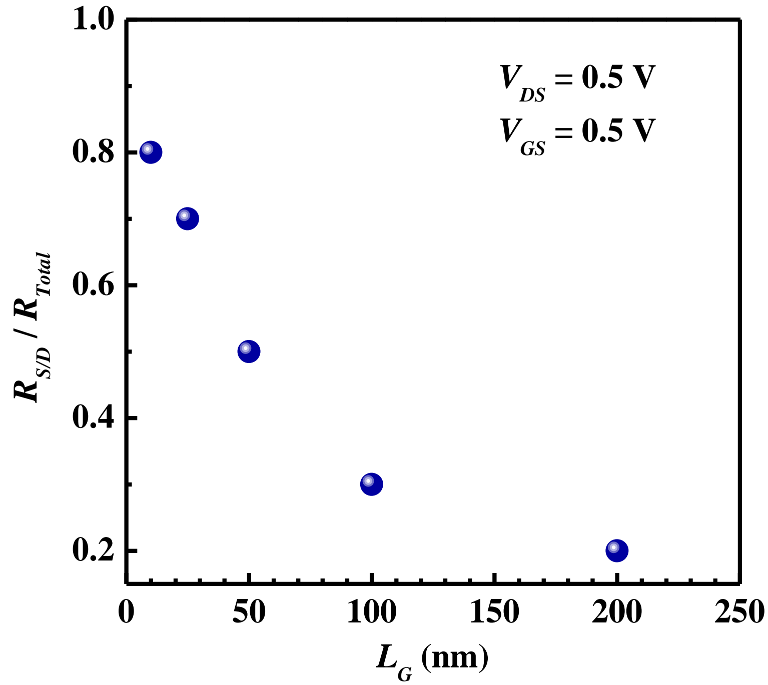


Fig. 1.4 Plot of $R_{S/D}/R_{Total}$ versus gate length L_G for an advanced III-V transistor. The data point for L_G = 50 nm is from the reported experimental data in Ref. [31] taken at V_{DS} and V_{GS} of 0.5 V, while the rest of the data points were projected by the author by keeping $R_{S/D}$ constant and scaling the channel resistance in proportion to L_G.

Most InGaAs MOSFETs reported to date [10],[25],[32]-[35] employ a non-self-aligned scheme (Fig. 1.5) where the metal contacts are located a distance l away from the channel. The total $R_{S/D}$ is contributed by the resistance of the n-doped S/D in between the metal contact and the channel region ($R_{n\text{-}doped}$) and the contact resistance (R_c) between the metal contact and the n-doped InGaAs.

For $In_xGa_{1-x}As$ materials, Si is a common impurity used for n-type doping. Using Si as the n-type dopant has several advantages such as low dopant activation temperature and low dopant diffusivity [36]-[38]. However, achieving a high S/D active doping concentration with conventional ion implantation and annealing is limited by the solid solubility of the implanted species in InGaAs

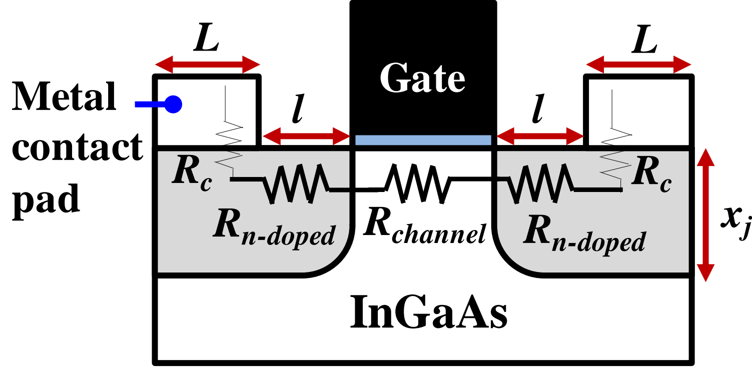


Fig. 1.5 Schematic of a InGaAs transistor with non-self-aligned S/D contacts, showing the various resistance components in a device. R_c, $R_{n\text{-}doped}$, and $R_{channel}$ are the contact resistance, the resistance of the n-doped source or drain, and the channel resistance, respectively. x_j is the S/D junction depth and l is the distance between the contact pad and the channel.

[36]-[38]. For example, introduction of Si in $In_xGa_{1-x}As$ n-MOSFETs by ion implantation gives a maximum concentration of 2×10^{18} cm^{-3} and 4.1×10^{18} cm^{-3} upon activation for In composition (x) of 0 and 0.53, respectively [37]-[38].

With a low dopant concentration in the low 10^{18} cm^{-3} range, the resistance of the n-doped $In_xGa_{1-x}As$ between the metal contact pads and the gate can be a concern as it contributes significantly to the total S/D series resistance of the device. The total S/D series resistance of the device can be expressed by

$$R_{S/D} = 2R_c + 2R_{n-doped} = 2\frac{\rho_c}{Z\times L_T} + 2\frac{\rho_{n-doped}\times l}{x_j\times W}, \qquad (1.3)$$

where ρ_c is the contact resistivity between metal contact pad and source (or drain), $\rho_{n\text{-}doped}$ is the source or drain resistivity, W is the gate width of the transistor, L, L_T, and Z are the length, transfer length, and width of the metal contact pad, respectively.

A highly doped S/D is needed to minimize the S/D series resistance. With highly doped n-type $In_xGa_{1-x}As$, low resistivity S/D regions ($\rho_{n\text{-}doped}$) can be obtained, as expressed by

$$\rho_{n-doped} = \frac{1}{q\mu_n N_D + q\mu_p N_A} \approx \frac{1}{q\mu_n N_D}, \tag{1.4}$$

where μ_n and μ_p are the electron and hole mobilities, respectively, and N_D and N_A are the active donor and acceptor concentration, respectively.

Selective growth of *in-situ* doped S/D material has been proposed to surmount the difficulty in achieving high active doping concentration by dopant implant and anneal. InGaAs MOSFETs with raised n^+-doped S/D formed by molecular beam epitaxy (MBE) regrowth [39]-[41] and metal organic chemical vapor deposition (MOCVD) selective epitaxial growth [42]-[43] have been demonstrated. InP/InGaAs composite channel MOSFETs with n^+-doped S/D regions selectively regrown by metal organic vapor phase epitaxy (MOVPE) have also been reported [44]-[45]. These reports show that significantly higher active n-type doping of ~5×10^{19} cm^{-3} can be obtained with *in-situ* doping.

Two well-studied non-self-aligned metal contacts for n-type $In_xGa_{1-x}As$ are AuGe-based metal and PdGe alloy [32]-[35],[46]. AuGe-based contact has been the most widely used contact scheme for GaAs-based devices. The main advantages of Au-based ohmic contacts are its low specific contact resistivity (1×10^{-6} $\Omega\cdot cm^2$ on n-type GaAs with doping concentration of 10^{18} cm^{-3}) and its low sheet resistance of ~1 Ω/□. The mechanism of the AuGe ohmic contact formation is as follows. During the annealing process, Ga reacts with Au to form

AuGa while Ge acts as donors when it fills the Ga vacancies. This process forms a thin, highly doped n-type layer just below the contact interface [46]. The heavily doped layer provides a tunneling path through the Schottky barrier at the interface between the metal and the S/D semiconductor.

However, there are also several drawbacks associated with the Au-based contact scheme. The main issue is its lack of thermal stability. The AuGa phases formed have a melting point of ~345 °C. Degradation of the contact, such as morphological and metallurgical changes at its interface with InGaAs, is typically observed at temperatures above 350 °C. Moreover, Au-based contact is not allowed in Si CMOS process as Au contributes deep-level traps in Si devices. Nonetheless, this contact scheme is still widely employed in $In_xGa_{1-x}As$ devices [32]-[34].

Pd-based contact was introduced to overcome problems faced by Au-based contact. PdGe contact, made by the deposition of Pd followed by Ge and annealing, forms a relatively good ohmic contact with contact resistivity as low as $9.8\times10^{-6}\ \Omega\cdot cm^2$ on GaAs highly doped with Si [35]. With the thickness ratio of Ge to Pd deposited being greater than two, the mechanism of the good ohmic contact formation is believed to be due to the formation of epitaxial Ge from the excess Ge under the PdGe alloy [47]-[49]. It is also believed that Ge substitution in Ga vacancies can occur during the annealing process, leading to the formation of an n^+-regrown GaAs layer below the epi-Ge layer. This contact has better thermal stability than AuGe, maintaining good contact morphology and smooth contact interface even at elevated temperatures as high as 400 ºC [50].

Self-aligned silicidation has long been implemented in Si CMOS technology. It allows the formation of metallic ohmic S/D contacts adjacent to the MOSFET's spacers, forming a highly conductive path close to the channel. It will be useful to develop a similar self-aligned S/D contact scheme for InGaAs transistors. By doing so, the contribution of $R_{n\text{-}doped}$ can be suppressed. Moreover, if InGaAs transistors can adopt S/D metallization similar to that used in Si technology (i.e. self-aligned silicidation-like process), the cost of having an additional lithography step can be saved. This will allow simple and more cost-effective integration with current Si CMOS processes. This sets the motivation of the research work presented in a few of the chapters in this thesis.

1.2.4 Issues Related to Heterogeneous Integration of InGaAs Transistors on Si Platform

InGaAs devices need to be eventually integrated on Si platform. Although the integration of InGaAs on Si substrate can be accomplished by means of chip bonding, a wafer-scale integration solution is more desirable from a manufacturing and cost effectiveness point of view. Various integration techniques have been explored to integrate GaAs on Si. These include direct heteroepitaxial growth of GaAs on Si [51]-[57], integration through a graded SiGe buffer [58]-[59], and selective aspect ratio trapping technique [60]. The success of these integration techniques is important for implementing InGaAs materials in current Si CMOS technology cost-effectively and without losing their high mobility benefit, which would otherwise occur due to the poor quality of the InGaAs channel layer grown.

The main issues with integrating InGaAs on Si are associated with the polar nature of InGaAs materials and the lattice mismatch between InGaAs and Si. The growth of a polar material such as InGaAs on a non-polar material like Si leads to the formation of domains with opposite sub-lattice allocation formed in InGaAs, also known as antiphase domains (APDs) [61]. One way in which this can be effectively overcome is by using a Si substrate with an off-cut surface [61].

The large 4.1% lattice mismatch between GaAs and Si imposes a more serious problem for direct integration. It leads to a high threading dislocation density in the grown GaAs layer (typically on the order of 10^8 cm^{-2}), resulting in defective channel layers unsuitable for MOSFET operation. The lattice mismatch is even larger for $In_xGa_{1-x}As$ with higher In content.

To ease this problem, GaAs (lattice constant = 5.653 Å) can be grown on Ge (lattice constant = 5.657 Å) which has almost equal lattice constant. Ge can be easily integrated on Si by using a graded SiGe buffer [58]-[59] or by using Ge-on-insulator (GeOI) on silicon substrate. An $In_xGa_{1-x}As$ layer can then be grown on GaAs-on-Ge by means of a compositionally graded buffer layer to relieve the in-built stress/strain due to the lattice mismatch. This would result in fewer stress-induced threading dislocations and thereby improving the quality of the $In_xGa_{1-x}As$ channel layer. As such, realizing InGaAs on graded SiGe or GeOI on Si substrate has the benefit of having a reduced graded buffer thickness as compared with direct InGaAs growth on Si. Another advantage is that Ge is a viable channel material for p-MOSFETs. This would also enable both high-mobility III-V n-

MOSFETs and Ge p-MOSFETs to be realized on a common substrate. This thesis also presents research work on InGaAs transistor integration on Si platform.

1.3 Research Objectives

The objective of this thesis is to address several key challenges associated with the integration of InGaAs transistors in Si IC chips. $In_xGa_{1-x}As$ MOSFETs with self-aligned silicide-like metallization compatible with Si CMOS is investigated. Common metals used in silicides, such as cobalt (Co) and nickel (Ni), are explored for self-aligned metallization of InGaAs. Potential heterogeneous integration of InGaAs transistors on silicon platform is also discussed. In addition, this thesis presents some key achievements towards realizing co-integration of InGaAs-based electronic and photonic devices at the intra-chip level. The results in this thesis will help in the assessment of InGaAs adoption for future logic applications.

1.4 Thesis Organization

This thesis is organized as follows. In Chapter 2, the concept of self-aligned metallization of InGaAs for InGaAs transistor using cobalt is demonstrated. The study includes the evaluation of the reaction between Co and InGaAs to form CoInGaAs, the development of selective wet etch process that etches Co over CoInGaAs, and the integration of Co self-aligned metallization in InGaAs MOSFETs. The successful demonstration of InGaAs n-MOSFET with

CoInGaAs metallic S/D highlights the prospect of self-aligned silicide-like metallization for InGaAs transistors.

In Chapter 3, Ni reaction with InGaAs to form Ni-InGaAs is investigated. A study of the band alignment between Ni-InGaAs and p-type InGaAs is presented. The material properties of Ni-InGaAs, such as crystal structure, lattice parameters, elemental composition, electrical uniformity, and electrical resistivity, are investigated. The results of this Chapter provide useful knowledge on the material characteristics of Ni-InGaAs.

Chapter 4 demonstrates Ni-InGaAs self-aligned metallization in InGaAs n-MOSFETs. The electrical performance of the transistors is characterized and evaluated. The integration of InGaAs n-MOSFETs on GeOI on Si platform is also presented. In addition, the impact of adding Pt in Ni-InGaAs is studied.

Chapter 5 presents key achievements towards realizing the co-integration of InGaAs-based electronic and photonic devices on a common GeOI on Si substrate. These include designing the layer structure of the substrate for transistor-laser integration, establishing the device layout structure, establishing device fabrication process flow suitable for the substrate, fabricating InGaAs n-MOSFETs, and characterizing the electrical output of the fabricated transistors. The results of this Chapter are important for enabling the co-integration of high-mobility InGaAs electronic and photonic devices on Si substrate at the intra-chip level.

Finally, the main contributions of this thesis and suggestions for future direction are summarized in Chapter 6.

Chapter 2

CoInGaAs as a Novel Self-Aligned Metallic Source/Drain Material for Implant-less $In_{0.53}Ga_{0.47}As$ n-MOSFETs

2.1 Introduction

Self-aligned silicidation process has been widely employed in Si complementary metal-oxide-semiconductor (CMOS) technology [62]-[73]. For InGaAs n-channel metal-oxide-semiconductor field-effect-transistors (n-MOSFETs), a self-aligned silicidation-like metallization process would need reaction of a deposited metal with InGaAs to form a metallic material in source/drain (S/D) region and a selective wet-etchant for the removal of the unreacted metal (Fig. 2.1). The metallic material formed should exhibit ohmic behavior on n-type InGaAs and preferably Schottky behavior on p-type InGaAs so that it can be used not only as a metal contact on n-type doped InGaAs S/D, but also possibly as the S/D material itself.

This Chapter investigates cobalt (Co) as a metal for self-aligned metallization of InGaAs. CoInGaAs formation was investigated by monitoring the sheet resistance of Co-on-InGaAs stack (Co/InGaAs) annealed at various

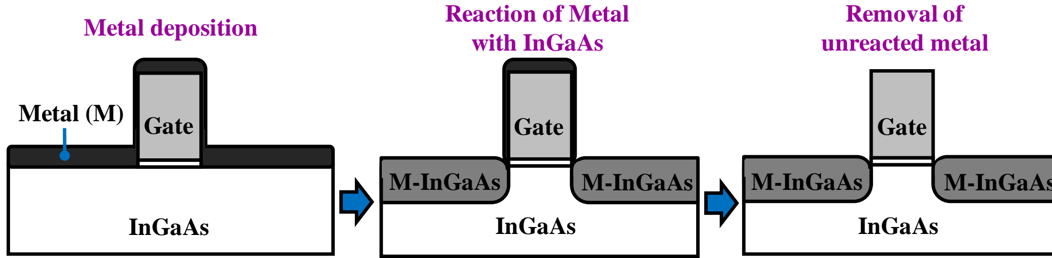


Fig. 2.1. An illustration of self-aligned silicidation-like metallization for InGaAs transistor, which involves the reaction of a deposited metal (M) with InGaAs forming a metallic material (denoted as M-InGaAs) in the S/D region and the removal of the unreacted metal.

temperatures. The contact resistivity between CoInGaAs and n^+-InGaAs was also extracted. Selective wet-etching of Co over CoInGaAs in various chemical etchants was also investigated to enable transistor integration. Finally, InGaAs n-MOSFETs with self-aligned CoInGaAs metallic S/D were successfully realized. The transistors exhibit relatively good electrical performance.

2.2 CoInGaAs Contact Metallization Module: CoInGaAs Formation, Extraction of Contact Resistivity, and Selective Wet-Etch Process Development

2.2.1 CoInGaAs Formation

The starting substrate was 2 inch p-type InP (100) substrates (doping concentration N_A of ~1×10^{19} cm^{-3}) with an epitaxially grown 500-nm-thick p-type $In_{0.53}Ga_{0.47}As$ (N_A ~2×10^{16} cm^{-3}) layer. This substrate is commercially available and was purchased for this work. Following native oxide removal in dilute hydrofluoric acid ($HF:H_2O$ = 1:100) solution, ~20 nm of Co was deposited by sputtering. The Co-on-$In_{0.53}Ga_{0.47}As$ (also denoted as Co/ $In_{0.53}Ga_{0.47}As$) sample

was then cut into smaller pieces. The pieces of samples were annealed for 60 s in a Rapid Thermal Processing (RTP) tool at various temperatures ranging from 200 to 400 °C in N_2 ambient.

The transmission electron microscope (TEM) images for samples of ~20 nm of Co deposited on $In_{0.53}Ga_{0.47}As$ annealed at various temperatures for 60 s are presented in Fig. 2.2. For the sample annealed at 300 °C [Fig. 2.2(a)], a change at the interface between Co and $In_{0.53}Ga_{0.47}As$ was observed. Energy Dispersive X-ray Spectroscopy (EDX) confirmed that the region near the surface consists of unreacted Co. Immediately below the unreacted Co, EDX measurements gave 35.2 atomic % (at%), 11.4 at%, 5.9 at%, and 47.5 at% for Co, In, Ga, and As, respectively. Co appears to have diffused into the $In_{0.53}Ga_{0.47}As$ layer where a reaction might have occurred.

When the anneal temperature is 350 °C [Fig. 2.2(b)], the reaction is complete and the thickness of CoInGaAs formed is ~60 nm. The CoInGaAs formed appears to have a more uniform thickness as compared to the one formed at 300 °C, though the CoInGaAs/$In_{0.53}Ga_{0.47}As$ interface is rough. EDX analysis was taken at localized spots [indicated in Fig. 2.2(b)] across the CoInGaAs film, and was summarized in Fig. 2.3. We observed a region rich in Co and Ga (~36 at% Co and ~46 at% Ga) at the top (Spot 1), followed by a region rich in Co and As (~39 at% Co and ~50 at% As) (Spot 2). In both spots, very little In (less than 6 at%) was detected. This could suggest that In out-diffused during the annealing and the remaining In may be in the form of In metallic element. The absence of a layer of pure Co indicates that the Co layer was fully consumed in the reaction.

For the sample annealed at 400 °C [Fig. 2.2(c)], the metallic film formed has an extremely rough interface with the underlying $In_{0.53}Ga_{0.47}As$ substrate.

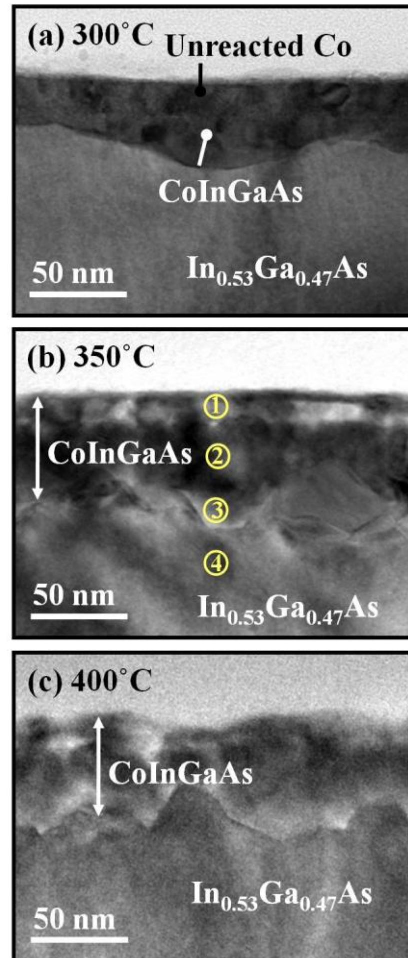


Fig. 2.2. TEM images of CoInGaAs formed by annealing 20 nm of Co on $In_{0.53}Ga_{0.47}As$ at (a) 300 ℃, (b) 350 ℃, and (c) 400 ℃. Most of the as-deposited Co remained unreacted at 300 ℃. In contrast, at 350 ℃, the entire Co layer reacted with InGaAs to form a CoInGaAs layer. Energy Dispersive X-ray Spectroscopy (EDX) was performed at various spots in the CoInGaAs film formed at 350 °C, indicated by the spots labeled 1 to 4. After annealing Co on $In_{0.53}Ga_{0.47}As$ at 400 ℃, a CoInGaAs layer with non-uniform thickness and a rough interface was formed.

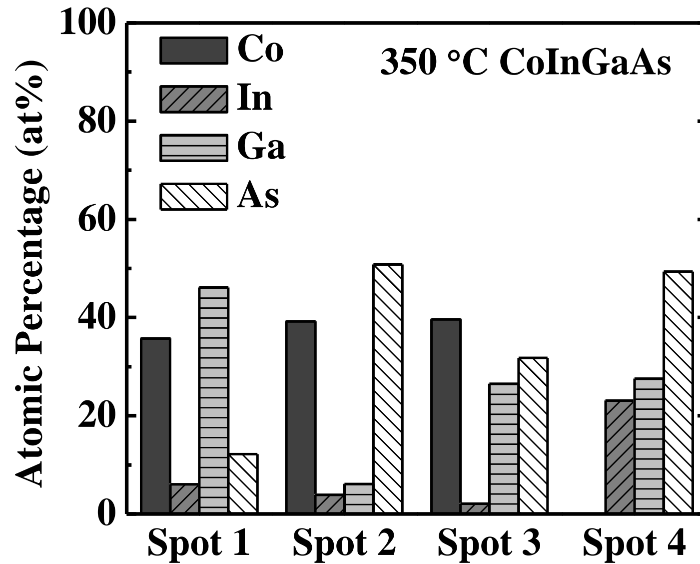


Fig. 2.3. EDX reveals the elemental atomic percentage found in localized spots at various parts of the CoInGaAs film formed at 350 °C, as indicated in Fig. 2.2(b). The EDX spot size is ~10 nm. It is observed that the CoInGaAs film comprises a Co- and Ga-rich layer on top of a Co- and As-rich layer.

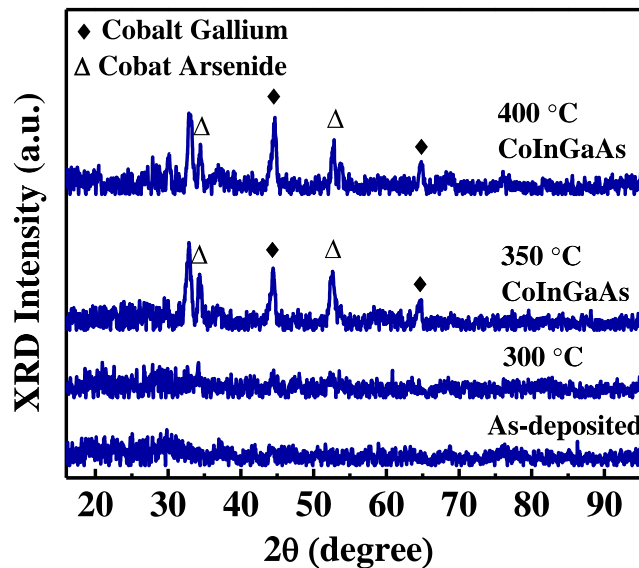


Fig. 2.4. Grazing angle XRD spectra of Co on $In_{0.53}Ga_{0.47}As$ samples as-deposited and annealed at 300, 350 and 400 °C. The presence of CoGa and CoAs phases were observed in 350 and 400 °C CoInGaAs film. The XRD characterization was carried out through an external service contract in IMRE.

X-ray Diffraction (XRD) detected the formation of Cobalt Gallium (CoGa) and Cobalt Arsenide (CoAs) binary phases in the CoInGaAs film, as shown in Fig. 2.4. It can be inferred that Cobalt Gallium phase made up the Co- and Ga-rich layer [Spot 1 in Fig. 2.2(b)] below which the Cobalt Arsenide phase constituted the Co- and As-rich region [Spot 2 in Fig. 2.2(b)]. This is similar to the reaction between Co and GaAs, where the formation of CoGa on CoAs occurs at 500 °C [74]-[75]. In this work, the CoGa and CoAs binary phases were formed at a temperature as low as 350 °C.

The sheet resistance (R_{sh}) values of the annealed samples are plotted in Fig. 2.5. As-deposited Co has a R_{sh} value of 10.4 Ω/square (Ω/□), as indicated by the dashed line. Upon annealing at 200 °C, R_{sh} remains unchanged. Considering the earlier TEM observation of partial or incomplete reaction at 300 °C, it is very likely that little or no reaction took place at 200 or 250 °C. The increase in sheet resistance at 300 °C marks the onset of reaction. The sheet resistance decreases upon complete reaction at 350 °C. The drop in sheet resistance upon the completion of reaction is related to the ~3 times increase in thickness of the layer formed.

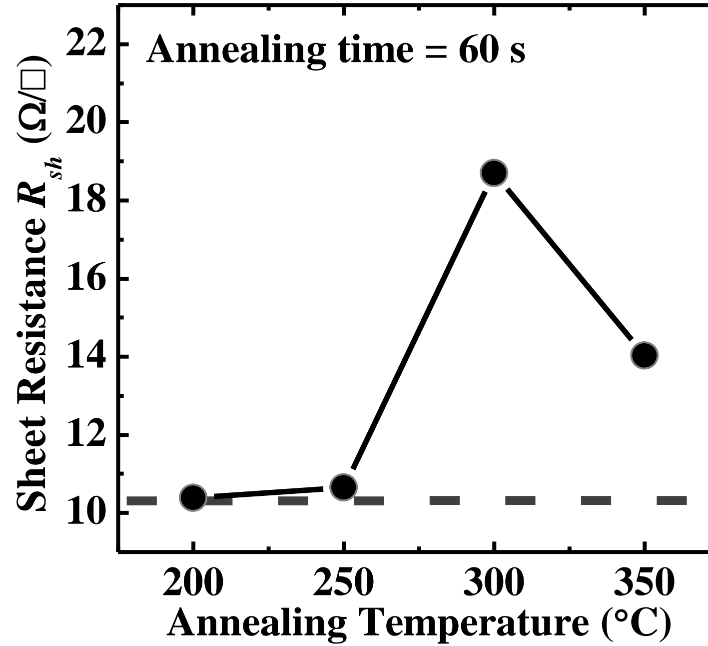


Fig. 2.5. Sheet resistance R_{sh} measured after annealing 20 nm of Co on $In_{0.53}Ga_{0.47}As$ at various temperatures ranging from 200 to 350 °C for 60 s. The R_{sh} of the sample annealed at 350 °C is that of the CoInGaAs film. The dashed line indicates the R_{sh} of as-deposited Co.

2.2.2 Extraction of Contact Resistivity

The ohmic behavior and the contact resistance of CoInGaAs on n-type $In_{0.53}Ga_{0.47}As$ were investigated from transfer length method (TLM) test structures. N-type $In_{0.53}Ga_{0.47}As$ (100 nm) with doping concentration N_D of ~5×10^{19} cm^{-3} on p-type $In_{0.53}Ga_{0.47}As$ with doping concentration N_A of ~1×10^{17} cm^{-3}, grown on top of 2 inch InP wafers (N_A of ~1×10^{19} cm^{-3}) was used as the starting substrate. ~15 nm of SiO_2 was deposited on the surface and n-type $In_{0.53}Ga_{0.47}As$ mesas were formed by wet etching. Contact holes were then patterned on the mesas to expose regions where metal pads would be formed. A short dip in buffered oxide etch was performed to remove SiO_2 right before Co deposition followed by a lift-off process. CoInGaAs metal pads were obtained by

annealing the sample. Finally, metal pads with various inter-pad spacings were obtained on the n-type $In_{0.53}Ga_{0.47}As$ mesas. Schematics in Fig. 2.6 illustrate the key process steps of the TLM test structure.

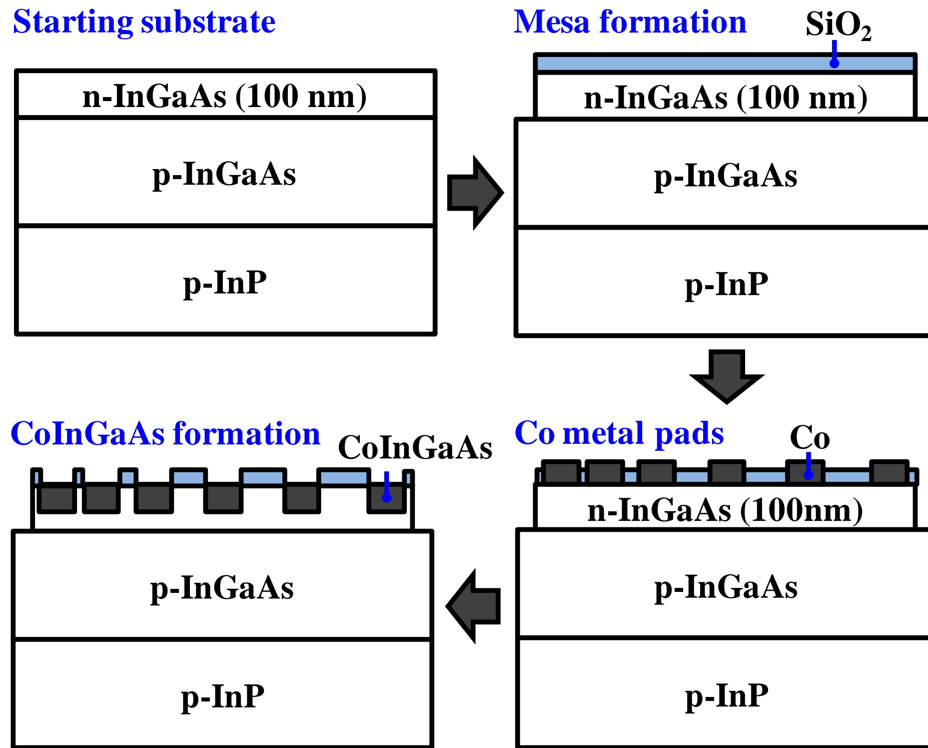


Fig. 2.6. Schematics illustrating process flow for forming TLM structures, featuring mesa formation, formation of Co metal pads, and CoInGaAs formation.

A top-view optical microscope image of the fabricated TLM test structure is depicted in Fig. 2.7(a). Fig. 2.7(b) shows the *I-V* characteristics of a TLM structure with CoInGaAs metal contacts formed at 350 °C 60 s. The current-voltage (*I-V*) characteristics were obtained from two adjacent metal pads with various contact spacings. The ohmic behavior of the CoInGaAs contact on n^+-$In_{0.53}Ga_{0.47}As$ is evident. From the plot of the total resistance as a function of contact spacing, the contact resistance and specific contact resistivity were extracted. The extraction of contact resistance and specific contact resistivity can be referred to Section 4.2 in Chapter 4. Fig. 2.7(c)-(d) plot the contact resistance and specific contact resistivity measured from TLM structures before and after CoInGaAs formation. The lowest contact resistance and specific contact resistivity of ~1.12 kΩ·μm and $\sim 6.25\times10^{-4}$ $\Omega\cdot cm^2$, respectively, were obtained with 350 °C annealing. The contact resistivity and other material characteristics (obtained in previous Section) of CoInGaAs will be compared with that of Ni-InGaAs in Chapter 3.

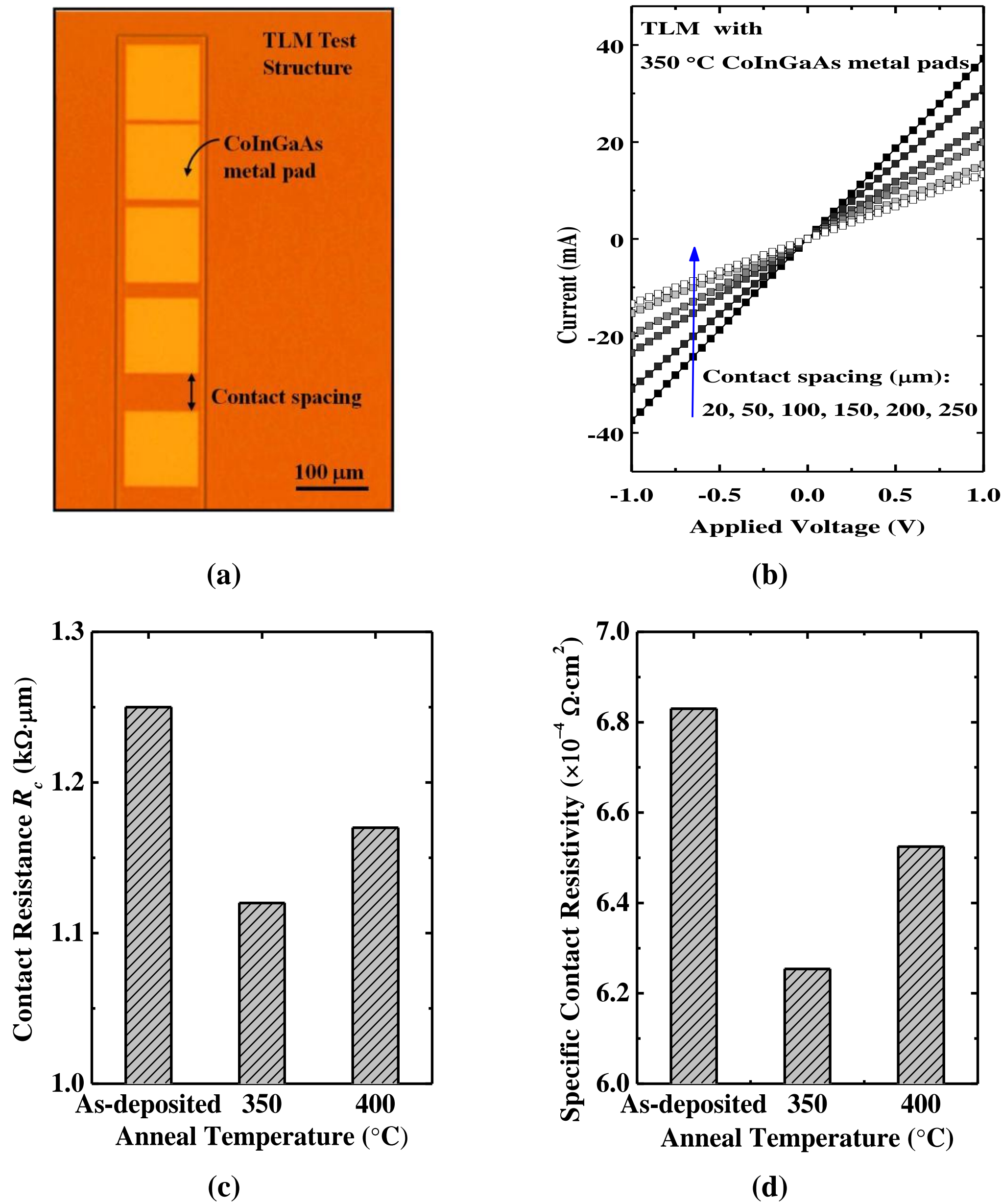


Fig. 2.7. (a) Top-view optical microscope image of TLM structure with various contact spacings. This structure was used for the extraction of contact resistance and specific contact resistivity. (b) *I-V* curves obtained from a TLM structure with CoInGaAs metal contacts formed at 350 °C, showing ohmic behavior on n^+-$In_{0.53}Ga_{0.47}As$. (c) Contact resistance R_c and (d) specific contact resistivity of Co and CoInGaAs formed on n^+-$In_{0.53}Ga_{0.47}As$.

2.2.3 Selective Wet-Etch Process Development

To successfully integrate CoInGaAs as self-aligned S/D material for InGaAs transistor, selective wet-etch process to etch Co without substantially etching CoInGaAs needs to be developed. The etch selectivity of Co over CoInGaAs in various chemical etchants is investigated in this Section.

~35 nm Co was deposited on p-type $In_{0.53}Ga_{0.37}As$/InP and annealed at 350 ºC for 5 min for ~100 nm CoInGaAs formation. ~100 nm Co was also evaporated on SiO_2/Si samples and annealed at 350 ºC for 5 minutes. These CoInGaAs/$In_{0.53}Ga_{0.37}As$/InP samples and Co/SiO_2/Si samples were prepared for the selective wet-etching study to obtain the etch rate of CoInGaAs and Co. Etching in various chemical etchants was performed right after Co deposition and CoInGaAs formation to prevent significant surface oxidation.

The R_{sh} value of the conductive films (Co or CoInGaAs) was recorded before the etching process. The sample was then dipped into an etchant for a short duration of time and was quenched in deionized wafer (DIW) before the R_{sh} value was recorded again. These processes were repeated subsequently using the same sample. A new sample was used for each different etchant.

The etching experiment was performed at room temperature using commonly used chemical acids such as hydrochloric acid (HCl), nitric acid (HNO_3), sulfuric acid (H_2SO_4), and phosphoric acid (H_3PO_4). An etchant that gives a high etch rate ratio of Co over CoInGaAs would be the one suitable for device integration. The etch rate of CoInGaAs in dilute hydrofluoric acid (DHF) was also determined as it is most commonly used etchant in device fabrication.

The etch rate of the conductive films (Co or CoInGaAs) was deduced from the sheet resistance obtained using four-point probe measurement. The R_{sh} is given by

$$R_{sh} = \rho_f / t_f , \tag{2.1}$$

where ρ_f is the resistivity of the conductive film and t_f is the thickness of the conductive film after going through each etch process for a duration of time in an etchant. The conductive film is expected to become thinner and has an increase in the R_{sh} value after each etch process. The etch rate r is determined from the R_{sh} change over a duration of etch time t which is given by

$$r = \left| \frac{dt_f}{dt} \right| = \left| \rho \frac{d(R_{sh}^{-1})}{dt} \right| . \tag{2.2}$$

The etch selectivity S of Co over CoInGaAs is determined from the ratio of the etch rate of Co (r_{Co}) and CoInGaAs ($r_{CoInGaAs}$) as expressed by

$$S = \frac{r_{Co}}{r_{CoInGaAs}} . \tag{2.3}$$

The R_{sh}^{-1} versus etch time (t) for CoInGaAs/$In_{0.53}Ga_{0.37}As$/InP samples and Co/SiO_2/Si samples etched in various etchants are plotted in Fig. 2.8. The volume ratio of the chemical acid and H_2O is 1 to 10 for HCl, HNO_3, H_3PO_4, H_2SO_4 solutions, and 1 to 100 for HF solution. The negative slopes of R_{sh}^{-1}-t plots indicate an increase in R_{sh} value of the conductive films. This suggests that the thicknesses of the conductive films reduce linearly over the etch time.

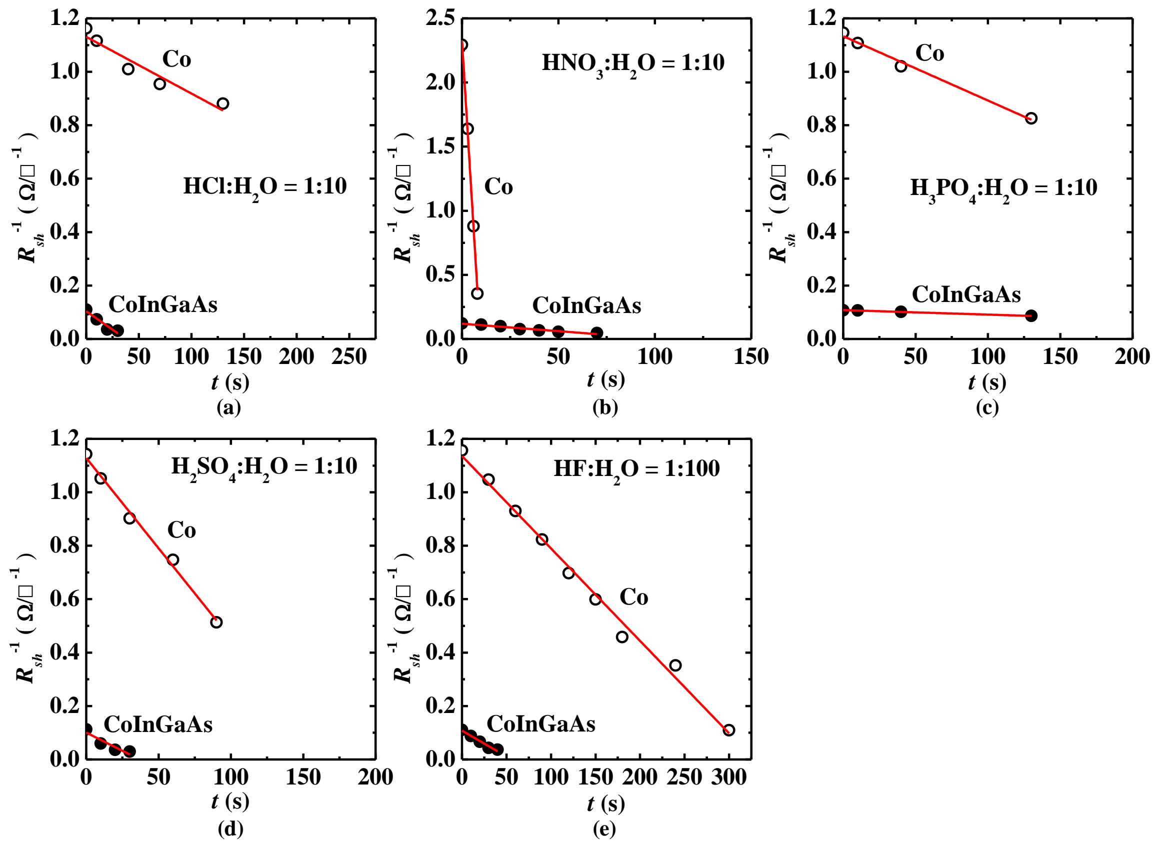


Fig. 2.8. R_{sh}^{-1} versus etch time t of Co and CoInGaAs films in various chemical solutions. R_{sh} was recorded after each etch duration.

The bulk resistivities of Co and CoInGaAs were determined from $R_{sh} \times t_f$ from the initial values of R_{sh} and t_f before etching. The bulk resistivities were calculated to be ~88 Ω·nm and ~945 Ω·nm for Co and CoInGaAs films, respectively. To simplify the etch development study, the bulk resistivities of Co and CoInGaAs films were assumed to be a constant value and were used to determine the remaining film thickness after each etch process. The thickness t_f versus t is shown in Fig. 2.9. From the slope of each linear curve, the etch rate of the conductive film in each etchant was determined.

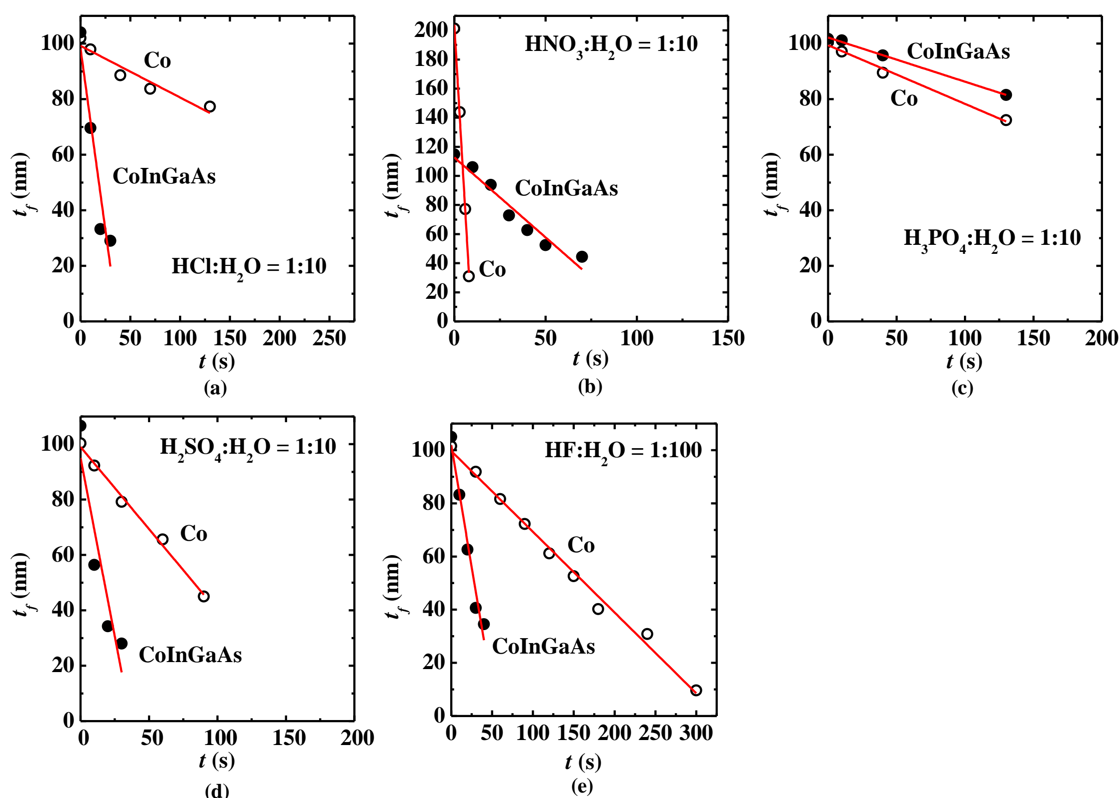


Fig. 2.9. Co and CoInGaAs thickness (t_f) versus etch time (t) in various chemical solutions.

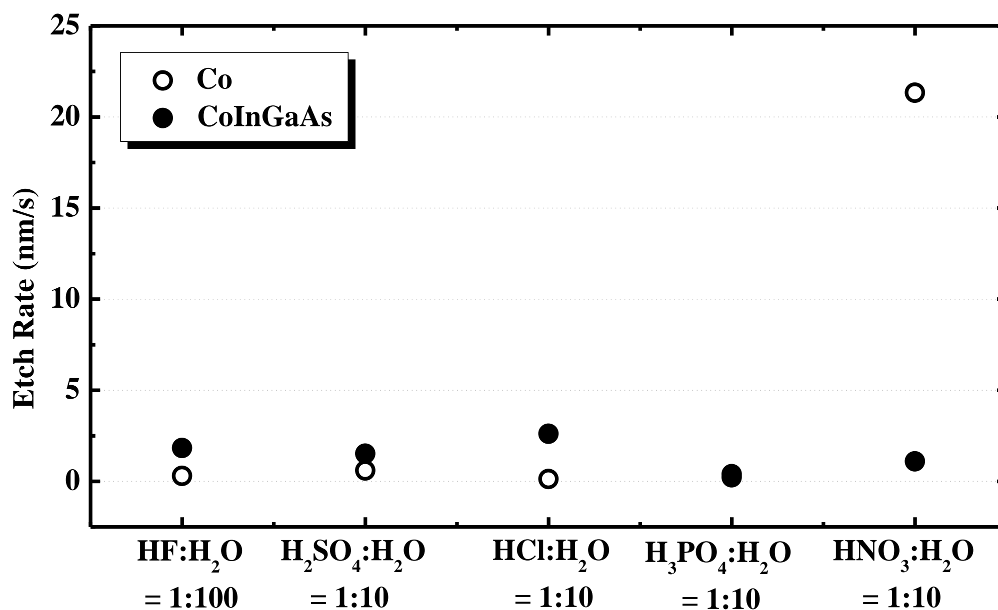


Fig. 2.10. Etch rate of Co and CoInGaAs films in various etchants. The gray and black symbols are the etch rate of Co and CoInGaAs, respectively.

The etch rate of Co and CoInGaAs in various etchants is plotted in Fig. 2.10. All the chemical etchants (HF, HCl, H_2SO_4, and H_3PO_4), except HNO_3, show comparable or higher etch rate for CoInGaAs than Co. This suggests poor etch selectivity of these etchants, hence not suitable for device integration. HNO_3 solution gives the highest selectivity as indicated by the etch rate of Co that is ~20 times higher than that of CoInGaAs.

Despite the high etch selectivity of $HNO_3:H_2O$ = 1:10 solution, a precise control of etching time in actual device fabrication will be very difficult to obtain. The ~1 nm/s etch rate of CoInGaAs in this solution can easily cause severe over-etch of the CoInGaAs layer at the source and drain regions of the device. HNO_3 solution was further diluted in attempt to explore a more suitable concentration which can give lower etch rate for CoInGaAs while maintaining high etch selectivity.

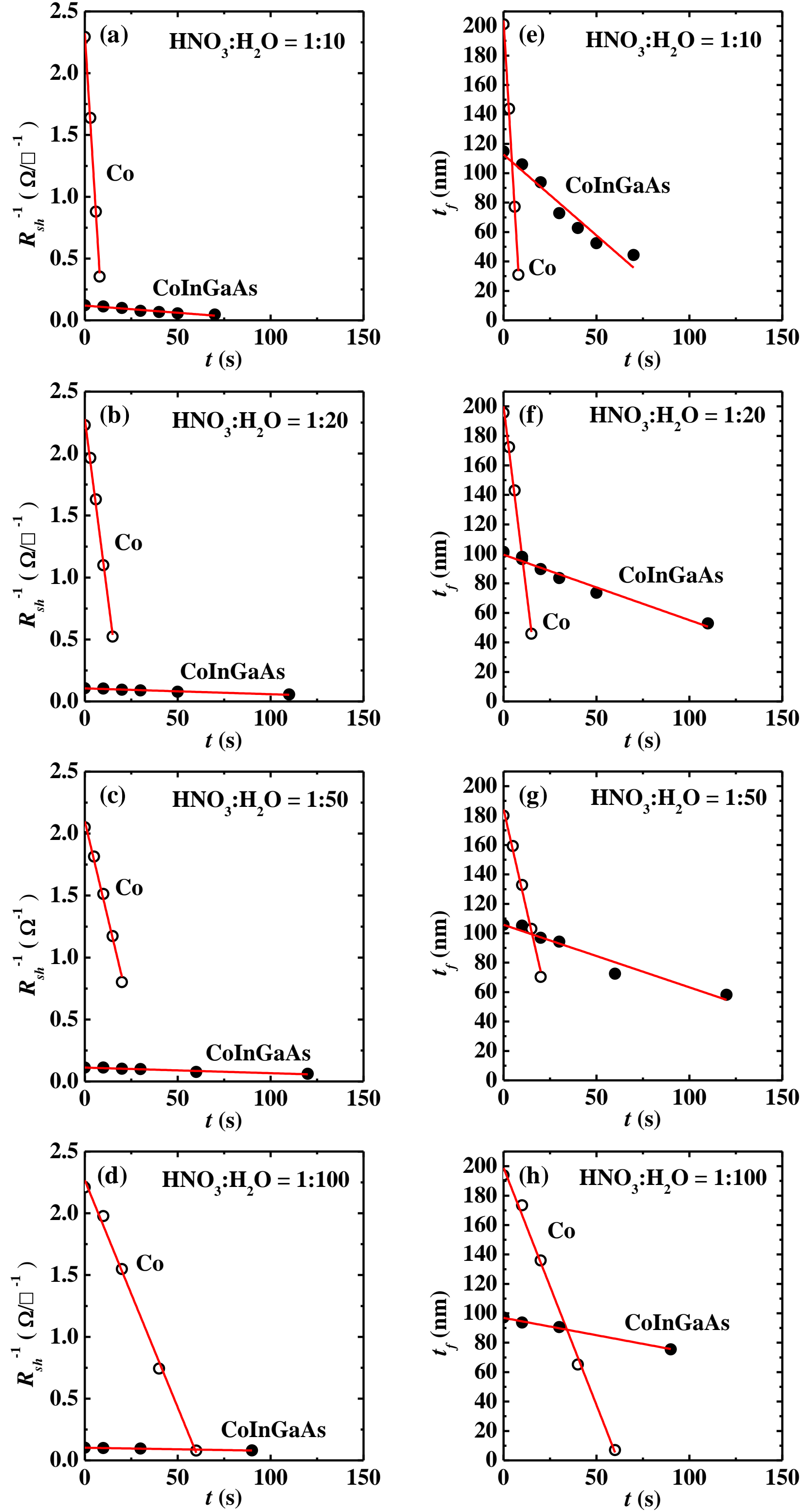


Fig. 2.11. R_{sh} versus t (a-d) and the corresponding Co and CoInGaAs thickness (t_f) versus t (e-h) in various concentrations of HNO_3 solution. R_{sh} was recorded after an etch duration.

HNO_3 solutions with various concentrations were prepared by mixing concentrated HNO_3 with H_2O in the HNO_3:H_2O ratio of 1:20, 1:50, and 1:100. Fig. 2.11 shows the R_{sh}^{-1}-t plot [Fig. 2.11(a)-(d)] and the corresponding thickness t_f versus time t plot [Fig. 2.11(e)-(h)] of Co and CoInGaAs in various concentrations of HNO_3 solutions.

The chemical reaction of Co with HNO_3 can be written as follows:

$$3\ Co_{(s)} + 8\ HNO_{3(aq)} \rightarrow 3\ Co(NO_3)_{2(aq)} + 2\ NO_{(g)} + 4\ H_2O_{(l)}\ .$$

The reaction between Co and HNO_3 is governed by two reaction mechanisms: (1) oxidizing reaction of Co and (2) dissolution reaction of the oxidized Co in the acid solution [76]-[77]. When the etching is limited by oxidizing reaction, the etch rate increases with increasing acid concentration.

On the contrary, the etch rate reduces with increasing acid concentration when the etching mechanism is limited by the dissolution reaction of the oxidized metal. This normally happens in a very acidic solution where the acidic environment helps to develop and sustain the oxide film formed on the surface of Co. This is due to the stability of the oxide film increases with the acid concentration which slows down the overall etching rate [76]-[77].

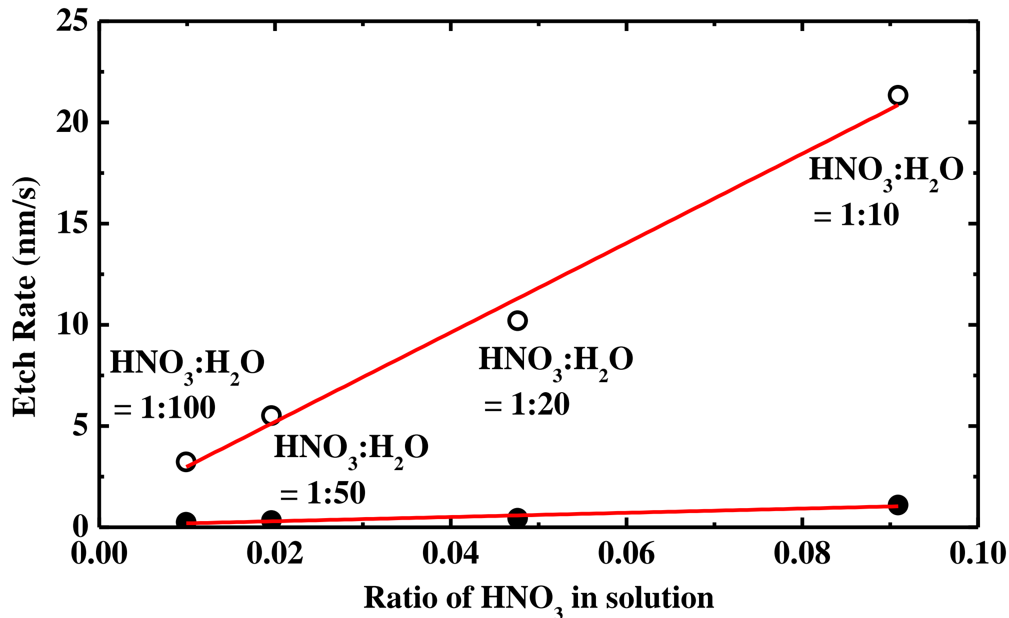


Fig. 2.12. Etch rate of Co and CoInGaAs films in various concentrations of HNO_3 solutions. The black open and solid symbols are the etch rate of Co and CoInGaAs, respectively. The HNO_3:H_2O ratio of 1:100, 1:50, 1:20, and 1:10 correspond to the molarity of 0.16, 0.31, 0.78, and 1.57 M, respectively.

The etch rate in HNO_3 solution with different concentration is plotted in Fig. 2.12. The etch rates for both Co and CoInGaAs reduce almost linearly with the amount of dilution. The decrease in etch rate with less concentrated HNO_3 acid suggests that the etching reaction is limited by oxidizing reaction of Co.

The etch rate of CoInGaAs that is lower than Co could be due to higher activation energy of the CoInGaAs etch reaction than that of Co. The different slope of the linear fitted line of Co and CoInGaAs indicates different selectivity value. Table 2.1 summarizes the selectivity value for all chemical etchants explored in this study. Both HNO_3:H_2O = 1:10 and HNO_3:H_2O = 1:20 solutions give very high etch selectivity. From device integration viewpoint, a much lower

Table 2.1. Etch selectivity of Co over CoInGaAs in various etchants.

Chemical etchants	**Selectivity *S***
HF:H_2O = 1:100	0.17
H_2SO_4:H_2O = 1:10	0.39
HCl:H_2O = 1:10	0.05
H_3PO_4:H_2O = 1:10	0.54
HNO_3:H_2O = 1:10	19.4
HNO_3:H_2O = 1:20	22.8
HNO_3:H_2O = 1:50	16.5
HNO_3:H_2O = 1:100	13.7

etch rate of ~0.4 nm/s for CoInGaAs in HNO_3:H_2O = 1:20 solution is preferred for a more controllable etching process.

2.3 Device Integration and Characterization

The process flow for integrating CoInGaAs as S/D material in an implant-less $In_{0.53}Ga_{0.47}As$ MOSFETs is shown in Fig. 2.13 (top left). Schematics of the device cross-sections illustrate the key process steps. The starting substrate comprises 500 nm of p-type $In_{0.53}Ga_{0.47}As$ grown on 2 inch p-type bulk InP wafer. This substrate was also purchased for this work. Pre-gate cleaning was performed to remove native oxide on the surface of $In_{0.53}Ga_{0.47}As$ using HCl and NH_4OH solutions. It was then dipped in $(NH_4)_2S$ solution for surface passivation and immediately transferred into an atomic layer deposition (ALD) chamber for the deposition of ~6 nm Al_2O_3. Post-deposition annealing (PDA) was then performed

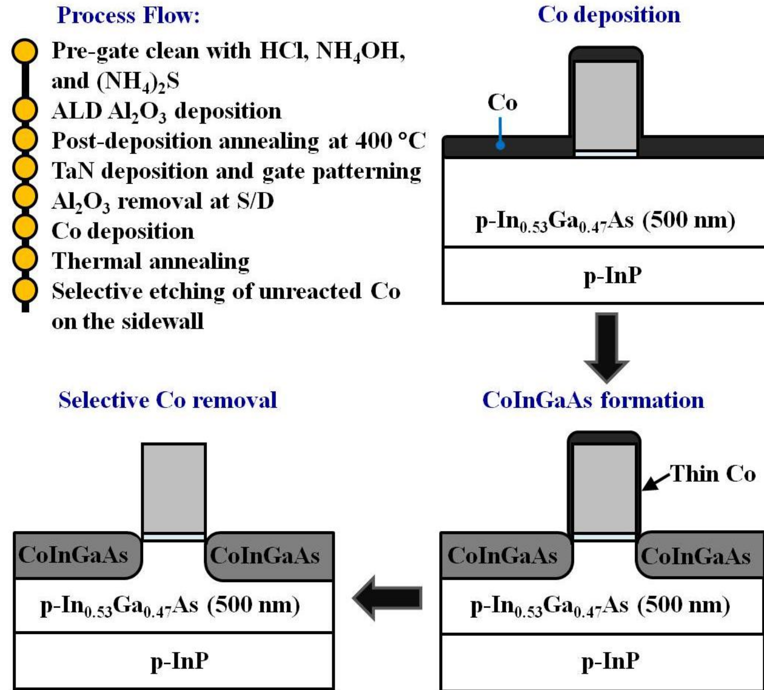


Fig. 2.13. Process flow for forming $In_{0.53}Ga_{0.47}As$ n-MOSFET with self-aligned CoInGaAs metallic S/D. The schematics show the key process steps, including Co deposition, reaction with InGaAs, and selective Co removal.

at 400 °C for 60 s. Next, 100 nm of tantalum nitride (TaN) gate electrode was deposited by sputtering. The gate stack was formed with patterning by optical lithography followed by chlorine-based plasma etching.

A 60 s dip in dilute hydrofluoric acid ($HF:H_2O$ = 1:100) solution was performed to remove the remaining Al_2O_3 right before a blanket deposition of ~10 nm Co on the patterned wafer. Rapid thermal anneal was performed at 350 °C for 60 s for CoInGaAs formation in the source and drain. A cross-sectional TEM image of the fabricated $In_{0.53}Ga_{0.47}As$ n-MOSFET with CoInGaAs metallic S/D is shown in Fig. 2.14. The CoInGaAs is self-aligned to the gate stack. The physical thickness of the Al_2O_3 gate dielectric is ~6 nm, as shown in the inset of Fig. 2.14.

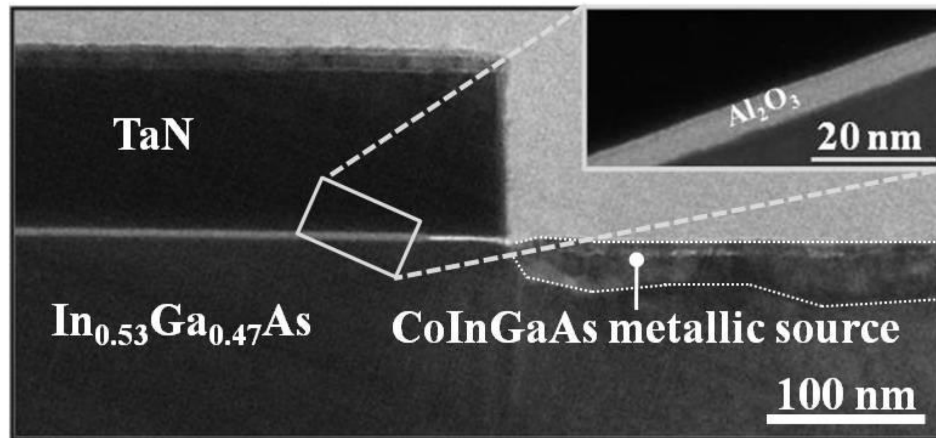


Fig. 2.14. Cross-sectional TEM images of $In_{0.53}Ga_{0.47}As$ MOSFET with CoInGaAs metallic S/D formed using 350 °C 60 s anneal. Annealing ~10 nm of Co formed 28-35 nm of CoInGaAs. The inset shows a zoomed-in view of the $TaN/Al_2O_3/In_{0.53}Ga_{0.47}As$ gate stack. The physical thickness of the Al_2O_3 gate dielectric is ~6 nm.

A continuous CoInGaAs film was formed in the S/D regions and the thickness is in the range of 28-35 nm. No unreacted Co remains on the surface of the S/D regions after annealing. The unreacted Co at the sidewalls of the gate was removed using diluted HNO_3 ($HNO_3:H_2O$ = 1:20) and device characterization was then performed.

To test the Schottky behavior of CoInGaAs on p-type $In_{0.53}Ga_{0.47}As$, voltage was applied to the CoInGaAs metallic source layer while the gold back contacted to InP was grounded. The CoInGaAs/p-$In_{0.53}Ga_{0.47}As$ structure demonstrates rectifying behavior, as shown in Fig. 2.15. This suggests that CoInGaAs can be a suitable S/D material. The reverse current at the positive voltage regime contributes to the off-state leakage current of the transistor. An increase in reverse current is observed with increasing applied voltage. This could be due to tunneling current across the junction and could be assisted by the

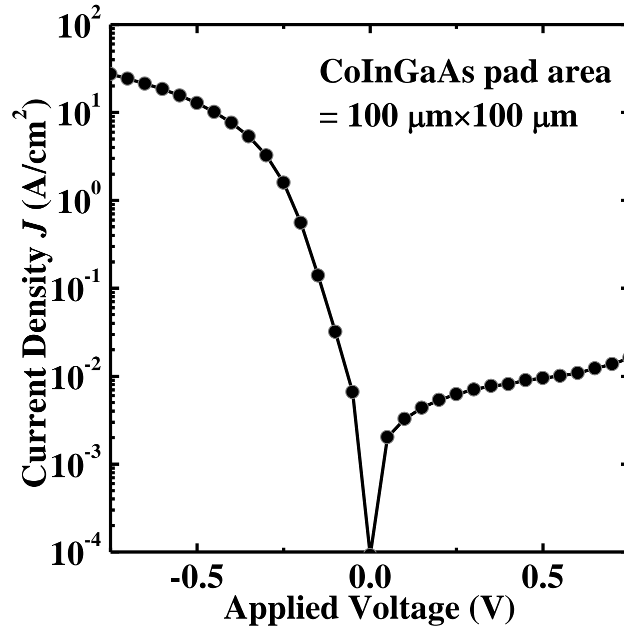


Fig. 2.15. CoInGaAs/p-$In_{0.53}Ga_{0.47}As$ junction shows rectifying behavior. Voltage was applied to the CoInGaAs while the InP substrate was grounded.

presence of traps at the CoInGaAs/$In_{0.53}Ga_{0.47}As$ junction. The reverse current could be suppressed by optimizing the formation process such that the interface between CoInGaAs and InGaAs is smoother, or by having an n-doped region [78] or wider band gap material beneath the CoInGaAs film [23].

Fig. 2.16(a) shows the I_{DS}-V_{GS} transfer characteristics of a transistor with gate length of 2 μm and gate width of 100 μm. Drain voltage V_{DS} of 0.1 and 1.2 V were applied. A threshold voltage (V_{TH}) of 0.57 V was obtained using linear extrapolation of the I_{DS}-V_{GS} curve (at V_{DS} = 0.1 V) at the maximum transconductance G_m. Hence, the I_{DS}-V_{GS} curve is extrapolated to I_{DS} = 0 and the V_{TH} is determined from the intercept gate voltage. A peak G_m value of 22.4 μS/μm at V_{DS} = 1.2 V was obtained. The high off-state current at V_{DS} = 1.2 V is due to the reverse leakage of the metal/semiconductor junction as described earlier. Fig.

2.16(b) plots the I_{DS}-V_{DS} characteristics of the transistor at various gate overdrives (V_{GS}-V_{TH}) ranging from 0 to 2.5 V in steps of 0.5 V. The low output characteristics are caused by a rather high S/D series resistance of ~23 kΩ·µm of this device [Fig. 2.16(c)]. The S/D series resistance is ~5× higher than that of transistor with conventional non-self-aligned S/D. The S/D series resistance comprises resistance from CoInGaAs S/D layer and the contact resistance between CoInGaAs and the InGaAs channel layer. The resistance of the CoInGaAs source and drain layer is estimated to be ~3 kΩ·µm, that is ~13% of the S/D series resistance. This indicates that the high S/D series resistance is dominated by the contact resistance between the CoInGaAs and the inversion InGaAs channel layer. Other metallic materials for the self-aligned metallization can be explored to obtain better S/D contacts that give lower S/D series resistance. In the next Chapter, nickel is explored as an alternative material for self-aligned metallization.

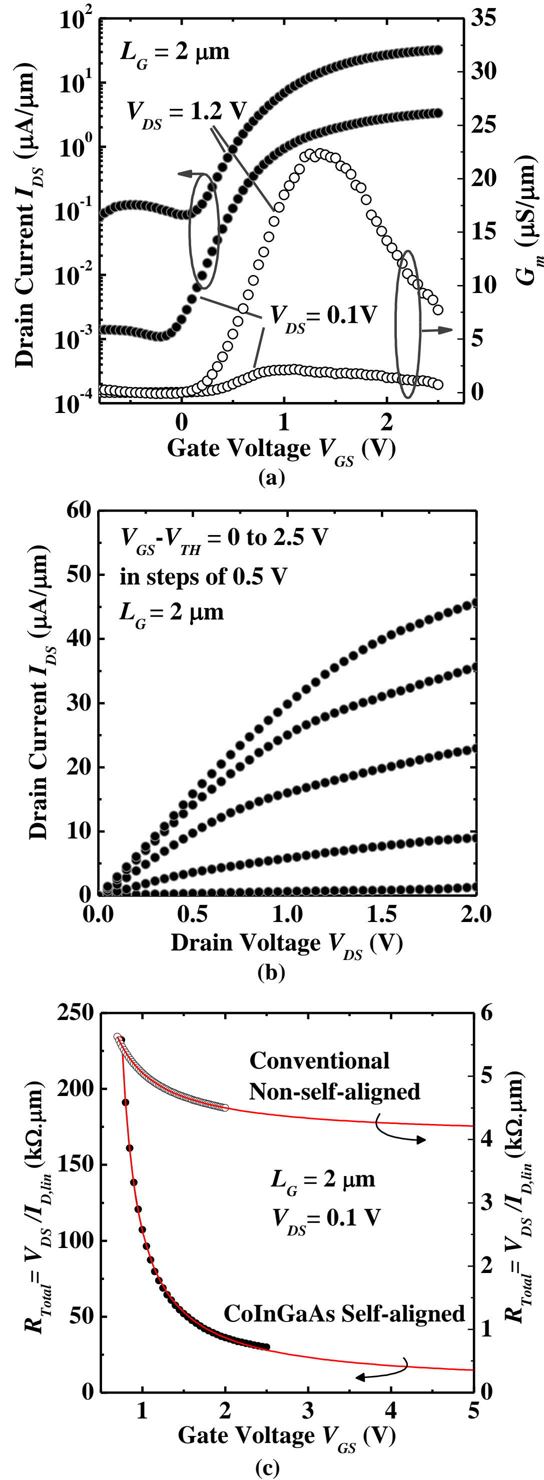


Fig. 2.16. (a) I_{DS}-V_{GS} curves of a $In_{0.53}Ga_{0.47}As$ n-MOSFET with self-aligned CoInGaAs S/D. G_m is referred to the right axis. (b) I_{DS}-V_{DS} plot for the same $In_{0.53}Ga_{0.47}As$ n-MOSFET. Gate overdrive V_{GS}-V_{TH} is varied from 0 to 2.5 V in steps of 0.5 V. (c) Series resistance of transistors with conventional non-self-aligned S/D and CoInGaAs self-aligned S/D.

2.4 Summary

In summary, self-aligned InGaAs metallization with Co for InGaAs n-MOSFETs was investigated. Co reacts with $In_{0.53}Ga_{0.47}As$ at temperatures as low as 350 °C to form a metallic CoInGaAs material. The formed film has relatively rough interface with InGaAs underneath. The CoInGaAs film formed at 350 °C has a sheet resistance of 14 Ω/□. It forms an ohmic contact on n-InGaAs and rectifying contact on p-InGaAs. The contact resistance and specific contact resistivity of CoInGaAs film on n-type InGaAs (doping concentration of ~5×10^{19} cm^{-3}) are ~1.12 kΩ·µm and 6.25×10^{-4} $\Omega\cdot cm^2$, respectively. Selective wet-etch of Co over CoInGaAs in various chemical etchants is explored. HNO_3 gives the highest etch selectivity of Co over CoInGaAs. An implant-less $In_{0.53}Ga_{0.47}As$ n-MOSFET with self-aligned CoInGaAs metallic S/D was demonstrated for the first time. $In_{0.53}Ga_{0.47}As$ n-MOSFET with CoInGaAs S/D shows reasonably well-behaved output characteristics.

Chapter 3

Material Characterization of Ni-InGaAs as a Contact Material for InGaAs Field-Effect Transistors

3.1 Introduction

In Si CMOS technology, nickel silicide (NiSi) has been widely used as the source/drain (S/D) contact material and is formed by reacting Ni with Si in a self-aligned silicidation process. Therefore, using Ni to form self-aligned contact metallization for future metal-oxide-semiconductor field-effect-transistors (MOSFETs) based on high-mobility channel materials, such as InGaAs, would be beneficial as it can take advantage of the well-established processes used for Si (e.g. wet etching of unreacted Ni). In this Chapter, the reaction of Ni with InGaAs is investigated as means for forming contacts that are the NiSi equivalent in InGaAs MOSFETs.

Ni has been used as a contact metal for $In_xGa_{1-x}As$ (InGaAs) MOSFETs in early work [79]-[81]. It has been employed in Au-Ge and Au-Sn metallization for forming non-self aligned ohmic contacts on n-InGaAs or in Au-Zn metallization for forming ohmic contacts on p-InGaAs. The presence of Ni at the contact

interface with InGaAs improves adhesion between the gold-based alloy and InGaAs, and also promotes interaction between them during metallization [82]-[84]. Reaction of Ni itself with GaAs has been extensively reported [85]-[87]. However, there is a lack of studies on the specifics of Ni reaction with InGaAs to form Ni-InGaAs.

For successful integration of Ni-InGaAs as metallic S/D material in aggressively scaled InGaAs n-MOSFETs, understanding the energy band alignment at the interface between Ni-InGaAs and InGaAs is essential as it relates to device junction leakage and standby power consumption. It is also an indicator whether Ni-InGaAs can establish a good ohmic contact material to InGaAs. A widely used technique to examine the band alignment of metal/semiconductor interfaces is photoelectron spectroscopy. In the first part of this Chapter, X-ray photoelectron spectroscopy (XPS) is employed to study the energy band alignment between Ni-InGaAs and $In_{0.53}Ga_{0.47}As$ [88]. The work function of Ni-InGaAs is also determined with ultraviolet photoelectron spectroscopy (UPS). Hole barrier height Φ_B^P at the Ni-InGaAs/$In_{0.53}Ga_{0.47}As$ interface was extracted. Electron barrier height Φ_B^N was determined by subtracting Φ_B^P from the band gap E_G of $In_{0.53}Ga_{0.47}As$.

Understanding the material properties of Ni-InGaAs, such as the crystal structure, lattice parameters, and epitaxial relationship with the underlying InGaAs layer, is also imperative. In addition, parameters such as the thickness ratio of Ni to Ni-InGaAs (i.e. the relationship between the initial thickness of Ni

deposited and the final thickness of the Ni-InGaAs formed), the electrical resistivity, and thickness uniformity of Ni-InGaAs are also important as they relate to the total series resistance of the device.

In the later part of this Chapter, the reaction between Ni and InGaAs to form $Ni_4InGaAs_2$ (denoted as Ni-InGaAs), the structural, compositional and electrical properties of this material are investigated [89]. Its crystal structure and lattice parameters were obtained from electron diffraction patterns and its epitaxial relationship with the underlying InGaAs layer was verified by X-ray Diffraction (XRD). Its composition was determined using XPS. The uniformity of the electrical properties of Ni-InGaAs film was examined using microscopic sheet resistance mapping. The electrical resistivity of Ni-InGaAs film was extracted from the sheet resistance.

The XPS, UPS, and high-resolution transmission electron microscopy (HRTEM) characterization were carried out in collaboration with a research team from IMRE. Other material characterization such as secondary ion mass spectrometry (SIMS) and X-ray diffraction (XRD) were performed through an external service contract. The design of experiments, fabrication, and analysis of the results were performed by the author.

3.2 Photoelectron Spectroscopy Study of Band Alignment at Interface between Ni-InGaAs and InGaAs

3.2.1 Sample Preparation and Methodology

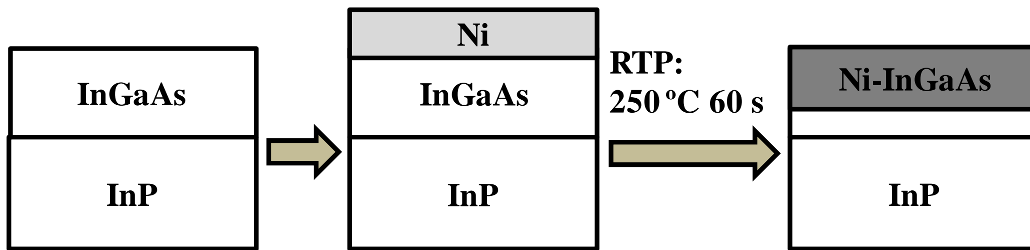


Fig. 3.1. Schematics showing the preparation process of Ni-InGaAs samples.

A small piece (1 cm × 1 cm) of wafer consisting of an epitaxial 1 μm thick $In_{0.53}Ga_{0.47}As$ with p-type (Be-doped) doping concentration N_A of ~2×10^{16} cm^{-3} grown on top of 2 inch p-type (N_A ~1×10^{19} cm^{-3}) InP wafer was used for this experiment. Such wafer is commercially available and was purchased for this work. The sample was dipped into diluted hydrofluoric acid (1:100) for 60 s to remove native oxide at sample's surface. Right after the native oxide removal, Ni with two different thicknesses was deposited by sputtering on $In_{0.53}Ga_{0.47}As$. Ni sputter was performed using DC power of 200 W at 25 °C and the chamber pressure kept at ~3 mTorr during the deposition. Samples were loaded into a rapid thermal processing (RTP) tool for 250 ºC 60 s annealing to form Ni-InGaAs. This thermal budget is sufficient for the reaction of Ni with InGaAs. Fig. 3.1 shows the schematics illustrating the sample preparation process. Further discussion on Ni-InGaAs formation would be presented in next Section.

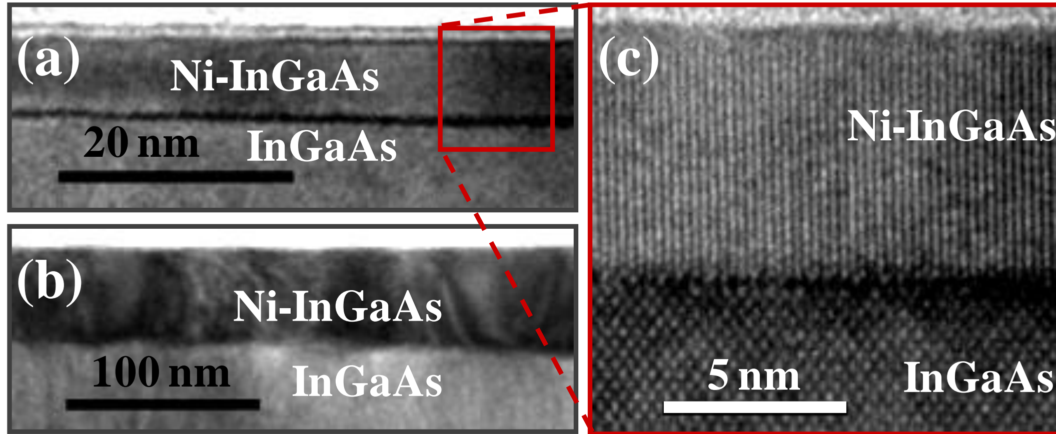


Fig. 3.2. Transmission electron microscopy (TEM) images of (a) thin and (b) thick Ni-InGaAs formed on $In_{0.53}Ga_{0.47}As$ substrate. (c) The high resolution image shows periodic arrangement of atoms in Ni-InGaAs layer, demonstrating good crystalline quality.

The transmission electron microscopy (TEM) images of thin (~6 nm) and thick (~46 nm) Ni-InGaAs on $In_{0.53}Ga_{0.47}As$ are shown in Fig. 3.2(a)-(b). A relatively smooth Ni-InGaAs layer with a distinct interface with $In_{0.53}Ga_{0.47}As$ was observed. The high resolution TEM image [Fig. 3.2(c)] shows good crystallinity of the Ni-InGaAs layer, where the periodic atomic arrangement can be observed.

Photoelectron spectroscopy was used to obtain the bulk property of two samples: $In_{0.53}Ga_{0.47}As$ substrate and a thick layer of Ni-InGaAs. XPS and UPS measurements were carried out using a spectrometer (Thermo VG Scientific ESCALAB 220i-XL system) equipped with a He discharge lamp (21.2 eV) for UPS and a monochromatic Al Kα (1486.6 eV) X-ray source for XPS. The calibration of the spectrometer was performed by determining the binding energies of Au $4f_{7/2}$, Ag $3d_{5/2}$, Cu $2p_{3/2}$, and Ni Fermi edge at 83.98 ± 0.02 eV,

368.26 ± 0.02 eV, 932.67 ± 0.02 eV, and 0.00 ± 0.02 eV. The XPS and UPS characterization was performed by our collaborators at IMRE.

All samples were subjected to *in-situ* 3 keV Ar^+ ion sputtering prior to XPS and UPS measurements to remove native oxide at the surface and also to reduce the thickness of the thin Ni-InGaAs film further for interface analysis. Ar^+ ion sputtering may induce changes in electronic and chemical states, thus may affect the interpretation of the measured data. However, in this study it was observed that no significant change in the XPS peak shapes, binding energy shifts, and atomic film composition of the sample before and after Ar^+ ion sputtering was performed. This indicates that Ar^+ ion sputtering performed for this study did not alter the material composition of all the samples.

3.2.2 Work Function and Band Alignment Extraction

UPS technique has been used widely to obtain work functions of materials [90]-[97]. It characterizes free-electron with certain range of kinetic energy liberated from sample by photon energy hv where h is the Planck's constant and v is the photon frequency (Fig. 3.3). A typical UPS spectrum consists of two superimposed spectra, i.e. primary photoelectron spectrum and inelastic secondary electron spectrum. Primary electrons are electrons that did not encounter inelastic scattering as they travel out to sample surface. They are electrons from near the Fermi level and have maximum kinetic energy. Primary electrons mark the onset of emission in the spectrum. Secondary electrons are electrons that lost the energy through scattering. Secondary electrons with zero

kinetic energy mark the cut-off of the emission. The work function (Φ) can be determined from the width of the spectrum using the following relation

$$\Phi = hv - E_{cut-off} + E_{Fermi}, \tag{3.1}$$

where $E_{cut-off}$ and E_{Fermi} are the binding energies of the secondary electron cut-off and the Fermi level, respectively [94].

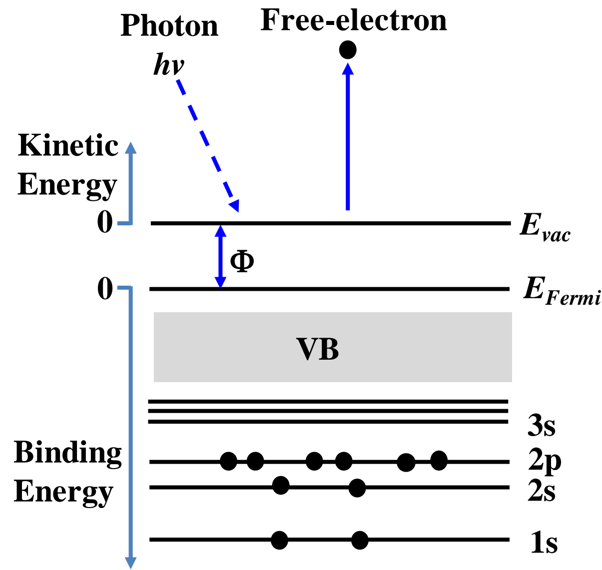


Fig. 3.3. Schematic showing incoming photon causing photoemission of electron from a sample. Depending on the photon *hv* energy, free-electron near valence band (VB) down to core-level can be emitted.

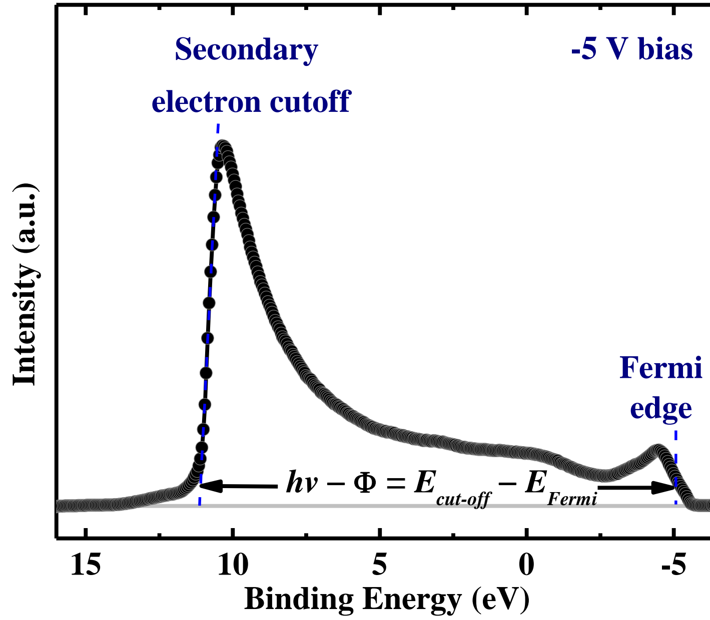


Fig. 3.4. He I (hv = 21.2 eV) UPS spectra of thick Ni-InGaAs formed on $In_{0.53}Ga_{0.47}As$. A -5 V bias was applied to the Ni-InGaAs layer. Fermi edge position was determined as the center of the slope as indicated by vertical line. Secondary electron cut-off position was determined from the intercept of the slope with the background level (horizontal gray line).

Fig. 3.4 shows Ni-InGaAs UPS spectrum. The sample was biased at -5 V during UPS measurement to separate the low energy cut-off from the spectrometer response. The work function of Ni-InGaAs of ~5.1 eV was obtained. It has to be noted that the Ar sputter used to remove Ni-InGaAs native oxide may cause damage in the Ni-InGaAs layer characterized by UPS and thus affect the accuracy of the extracted work function value. The inaccuracy of the extracted work function value was estimated from the change of work function value from the as-formed Ni-InGaAs to that of after complete oxide removal. Fig. 3.5 showed the UPS spectra obtained from as-formed, after a few minutes of Ar sputtering, and after complete oxide removal of thick Ni-InGaAs film. It can be observed that the work function difference of the as-formed Ni-InGaAs and after complete

oxide removal is 0.37 eV. Thus, the pure bulk Ni-InGaAs workfunction value is believed to be in between 4.73–5.1 eV.

Next, XPS measurement was carried out on a thin Ni-InGaAs layer on $In_{0.53}Ga_{0.47}As$ to study the Ni-InGaAs/$In_{0.53}Ga_{0.47}As$ interface. The band alignment and hole barrier height extraction were evaluated from the XPS spectra. As 3d core-level binding energy was employed as reference due to the significant difference (~1 eV) in the peak position of As 3d of thick Ni-InGaAs as compared to $In_{0.53}Ga_{0.47}As$ substrate as shown in Fig. 3.6(a) which was not observed from In $3d_{5/2}$ and Ga $2p_{3/2}$ core-level spectra.

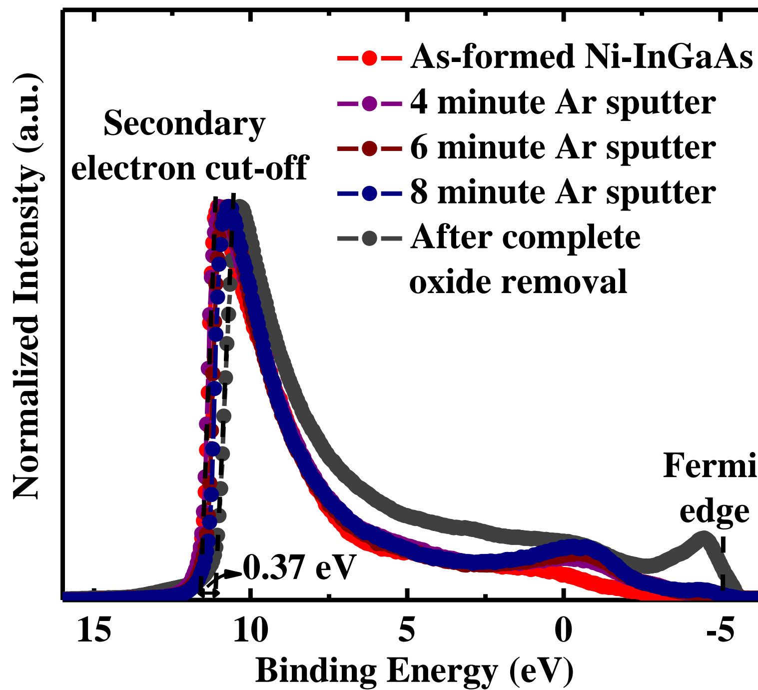


Fig. 3.5. He I (hv = 21.2 eV) UPS spectra of as-formed, after Ar sputter, and after complete oxide removal of thick Ni-InGaAs formed on $In_{0.53}Ga_{0.47}As$. A -5 V bias was applied to the Ni-InGaAs layer. The maximum difference in the spectra width is 0.37 eV.

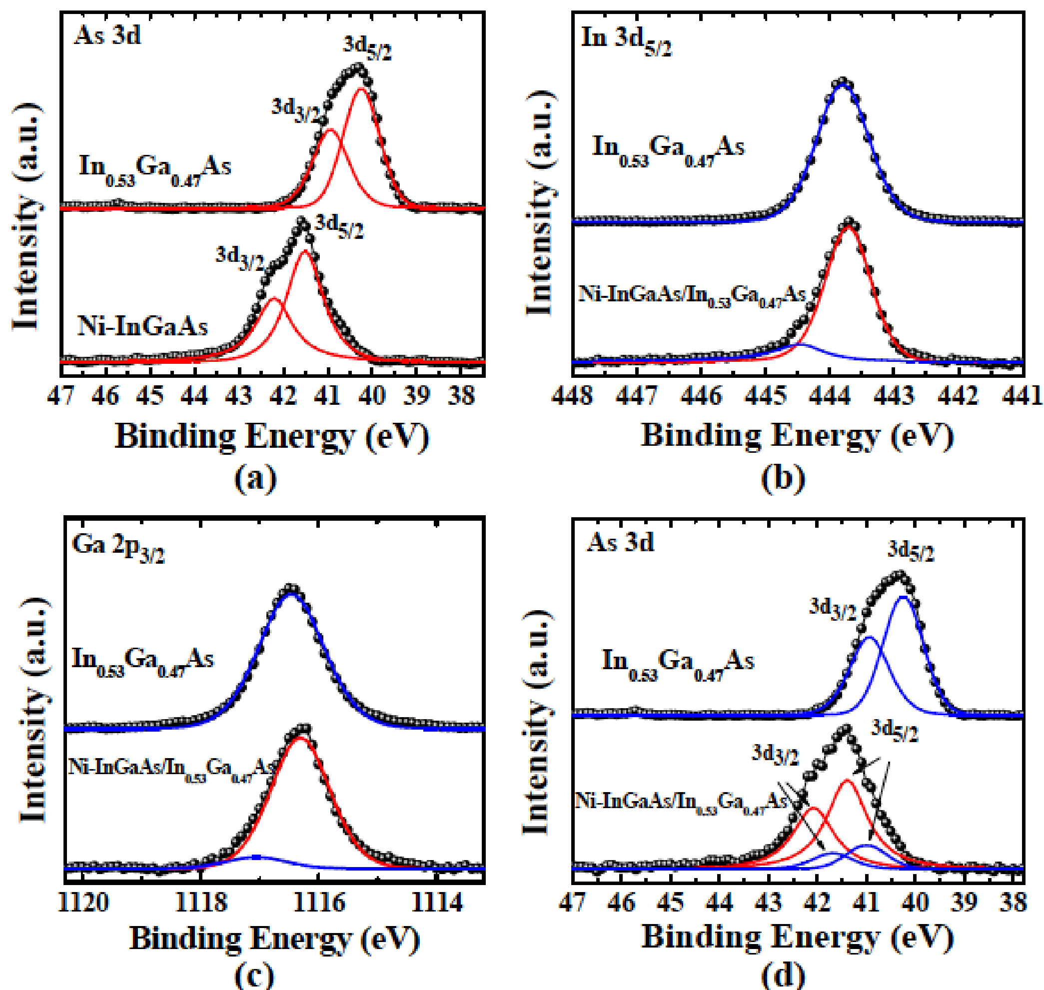


Fig. 3.6. Normalized XPS core-level spectra of (a) As 3d for bulk Ni-InGaAs (bottom) and $In_{0.53}Ga_{0.47}As$ (top) samples. Comparison of (b) In $3d_{5/2}$, (c) Ga $2p_{3/2}$, and (d) As 3d from Ni-InGaAs/$In_{0.53}Ga_{0.47}As$ interface sample (bottom) and from bulk $In_{0.53}Ga_{0.47}As$ (top). The red and blue fitted curves correspond to signal coming from Ni-InGaAs and $In_{0.53}Ga_{0.47}As$, respectively. The In $3d_{5/2}$, Ga $2p_{3/2}$, and As 3d peaks at the interface resides 0.75 eV higher than that of $In_{0.53}Ga_{0.47}As$ substrate determined by the difference between the blue fitted curves.

The large shift in As 3d seems to suggest Ni has formed chemical bonding with As. Nevertheless, binding energy shift of Ni $2p_{3/2}$ from bulk Ni-InGaAs relative to its metallic binding energy position was not observed. Information regarding the formation of chemical bonding in Ni-InGaAs layer is still inconclusive only based on XPS results obtained in this work. More experimental

work is required for further investigation. For instance, electron energy loss spectroscopy (EELS) characterization can be performed to obtain the electron energy loss information, the bonding, oscillation, or vibrational information of the solid [95]. Another reason to choose As 3d as reference spectrum is its large information depth due to lower binding energy (higher kinetic energy). Therefore, strong signals from the interface and less experimental error are expected.

To compute the barrier height between Ni-InGaAs and $In_{0.53}Ga_{0.47}As$, core-level alignment method reported by Kraut *et al*. was employed [96]. The hole barrier height at the interface is given by

$$\Phi_B^P = E_v - E_{CL}^{As3d_{5/2}} + E_{CL}^{As3d_{5/2}}{}_{(i)}, \tag{3.2}$$

where, E_v and $E_{CL}^{As3d_{5/2}}$ represent valence band maximum and peak core-level binding energy of bulk $In_{0.53}Ga_{0.47}As$, respectively. $E_{CL}^{As3d_{5/2}}{}_{(i)}$ represents core-level binding energy measured from the interface.

From the doping concentration of p-type $In_{0.53}Ga_{0.47}As$ used in this work, it is known that the valence band maximum is 0.1 eV below the Fermi level. The As 3d core-level binding energy at Ni-InGaAs/$In_{0.53}Ga_{0.47}As$ interface was obtained from the thin Ni-InGaAs sample. After careful curve fitting to both As 3d spectra obtained from Ni-InGaAs/$In_{0.53}Ga_{0.47}As$ interface and from the bulk $In_{0.53}Ga_{0.47}As$ samples, we observed that the As 3d peak core-level at the interface sample is located 0.75 eV away from that of the $In_{0.53}Ga_{0.47}As$ substrate [Fig. 3.6(d)]. Similar peak shift was also observed from In $3d_{5/2}$ and Ga $2p_{3/2}$ spectra of Ni-InGaAs/$In_{0.53}Ga_{0.47}As$ interface as shown in Fig. 3.6(b)-(c). The corresponding

Φ_B^P is evaluated to be 0.8 ± 0.1 eV. With $E_G = 0.7$ eV for $In_{0.53}Ga_{0.47}As$, this suggests that the Fermi level of Ni-InGaAs is at 0.1 ± 0.1 eV above the conduction band at the Ni-InGaAs/$In_{0.53}Ga_{0.47}As$ interface.

Note that the work function of bulk Ni-InGaAs is higher than the electron affinity of InGaAs. The alignment of the Fermi level of Ni-InGaAs to the conduction band of $In_{0.53}Ga_{0.47}As$ indicates that there could be significant Fermi level pinning or the presence of an interface dipole. A clearer view of how interface dipole or Fermi level pinning could lead to a high electric field at the Ni-InGaAs/InGaAs interface and band alignment consistent with XPS results is illustrated in Fig. 3.7. The charge neutrality E_{CNL} of $In_{0.53}Ga_{0.47}As$ is reported to be at ~0.2 eV below the conduction band [97]. Interface states located above or below the E_{CNL} are predominantly acceptor-like or donor-like, respectively. Filled acceptor-like (or donor-like) states are negatively charged (or neutral), while unfilled acceptor-like (donor-like) states are neutral (or positively charged). With the Fermi level of Ni-InGaAs located far below the E_{CNL} of InGaAs, donor-like interface states are unfilled and positive charge on the InGaAs side could possibly drive the Ni-InGaAs Fermi level to align towards the conduction band.

A Ni-InGaAs/p-InGaAs structure was fabricated, which shows rectifying *I-V* characteristics (Fig. 3.8). This is consistent with the results of photoelectron spectroscopy. More investigation would be needed to verify the origin of the high Schottky barrier height seen by holes at the Ni-InGaAs/$In_{0.53}Ga_{0.47}As$ interface. The results in this Section imply that a good ohmic contact can be obtained for Ni-InGaAs formed on n-type InGaAs.

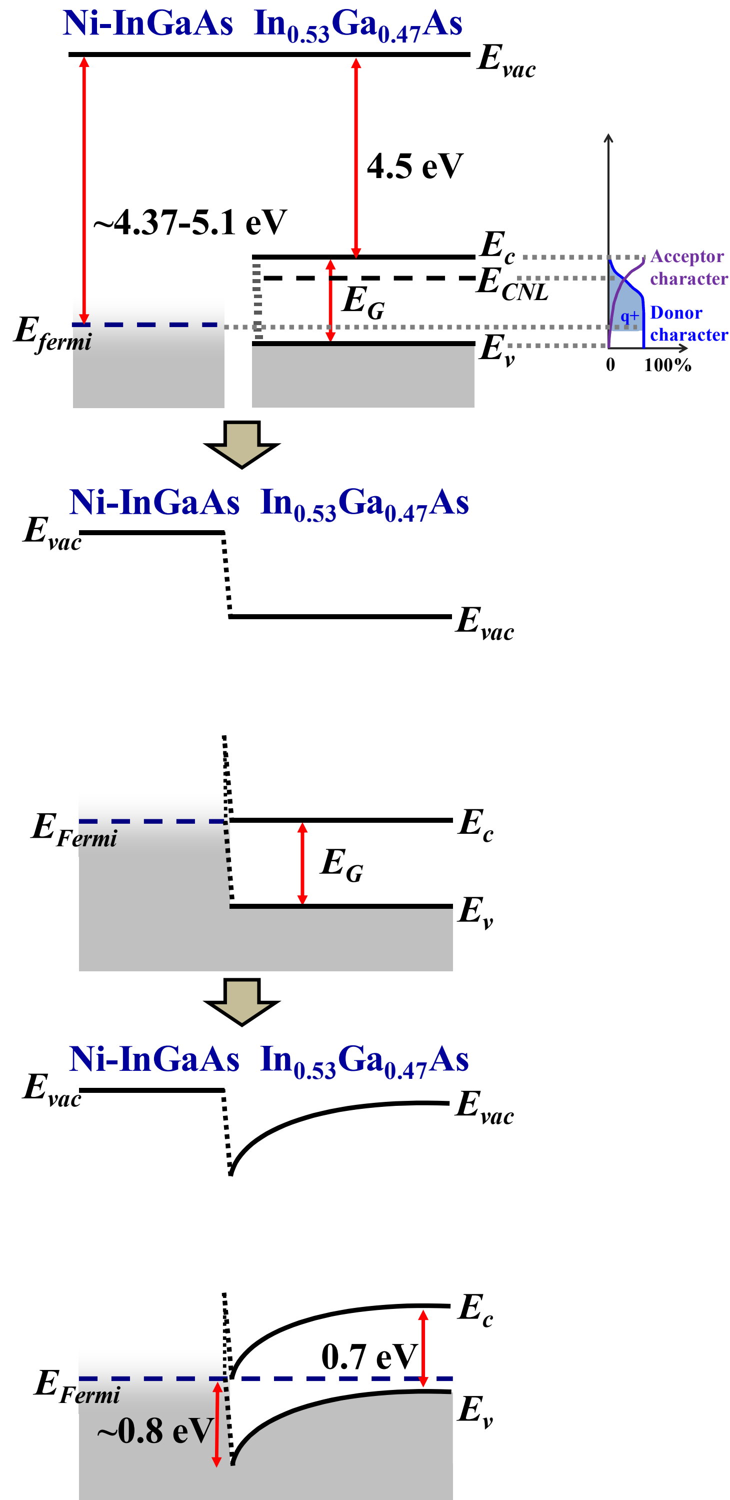


Fig. 3.7. Schematics of energy band diagram showing interface dipole (dotted band) or Fermi level pinning could lead to a high electric field at the NiInGaAs-InGaAs interface. The band alignment of Ni-InGaAs in contact with $In_{0.53}Ga_{0.47}As$ substrate is consistent with XPS results.

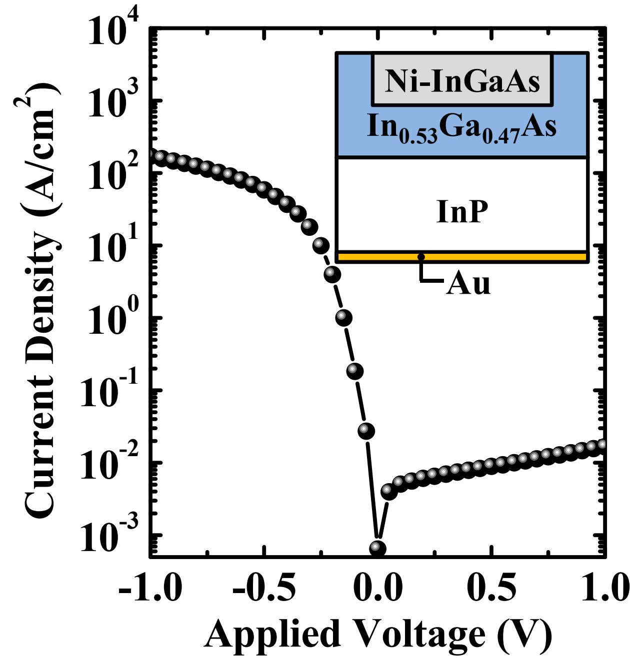


Fig. 3.8. *I-V* characteristics measured between Ni-InGaAs pad and Au back-side contact to InP of a diode structure (inset). The dimension of Ni-InGaAs pad area is 100 μm×100 μm. The Ni-InGaAs/p-$In_{0.53}Ga_{0.47}As$ junction shows rectifying behavior.

3.3 Crystal Structure and Epitaxial Relationship of Ni-InGaAs Films formed on InGaAs by Annealing

3.3.1 Sample Preparation

The starting 2 inch wafers comprise of a 20-nm-thick p-type $In_{0.7}Ga_{0.3}As$ layer (with a doping concentration of ~2×10^{16} cm^{-3}) on 500-nm-thick p-type $In_{0.53}Ga_{0.47}As$ (with a doping concentration of ~2×10^{17} cm^{-3}) grown on p-type (001) InP (with a doping concentration of ~1×10^{19} cm^{-3}) by molecular beam epitaxy. These wafers were purchased from an external vendor. Following native oxide removal in dilute hydrofluoric acid (1:100) solution, Ni was deposited on the wafers by sputtering using DC power of 200 W at 25 °C. The chamber pressure was ~3 mTorr during the deposition. Ni sputter condition employed here

is the same as in previous Section. Samples with Ni thicknesses t_{Ni} of ~11 nm and ~28 nm were prepared. Each of the two Ni-on-InGaAs samples was cut into smaller pieces. The pieces were annealed in a nitrogen ambient in a Rapid Thermal Processing (RTP) tool at different temperatures ranging from 200 to 350 °C.

3.3.2 Ni-InGaAs Formation: Anneal Conditions, Elemental Composition, Material Structure and Thickness Ratio of Ni to Ni-InGaAs

The annealing temperature T and time t are two critical parameters affecting the reaction between Ni and InGaAs. During the rapid thermal anneal, Ni with a thickness of t_{Ni} reacts with InGaAs to form a Ni-InGaAs layer with a thickness of $t_{Ni\text{-}InGaAs}$ [inset of Fig. 3.9]. The sheet resistances R_{sh} of the annealed samples were measured with a microscopic four-point probe [98]-[99]. Fig. 3.9 plots the R_{sh} of samples annealed at temperatures ranging from 200 to 350 °C for 60 s. The R_{sh} of unannealed samples (T = 25 °C) is also included.

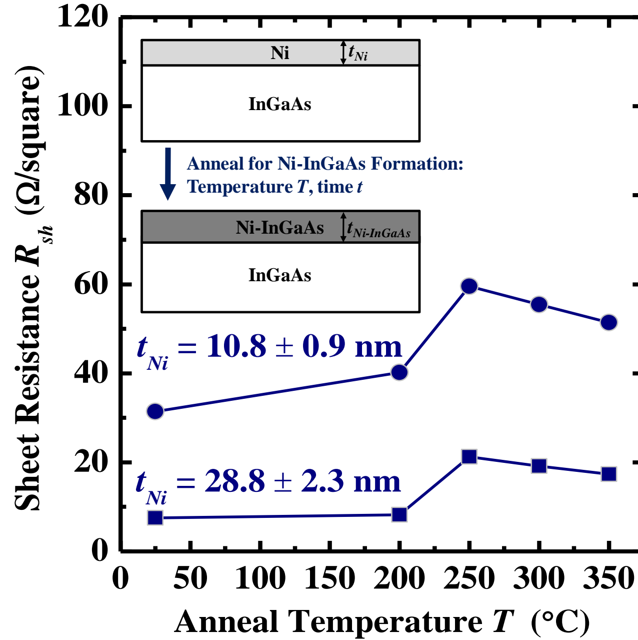


Fig. 3.9. Sheet resistances R_{sh} of Ni-on-InGaAs samples annealed at various temperatures for a fixed time of 60 s. The inset shows an illustration of the formation of Ni-InGaAs (bottom) by annealing as-deposited Ni-on-InGaAs (top) at temperature T for time t.

We observed that no significant reaction occurred at 200 ºC. The profiles of Ni, In, Ga, and As before and after 200 ºC 60 s anneal were obtained using Secondary Ion Mass Spectrometry (SIMS), as shown in Fig. 3.10(a) and (b). When Ni and InGaAs are brought into contact, a very thin intermixed layer may be formed at the Ni/InGaAs interface as implied from the two kinks observed in the SIMS profile [Fig. 3.10(a)]. At T = 200 °C, a broader intermixed layer and depletion in the as-deposited Ni are observed [Fig. 3.10(b)]. The slight reduction in Ni thickness could have caused a slight increase in R_{sh} at 200 °C. The percentage increase in R_{sh} after 200 ºC anneal is less significant when t_{Ni} is thicker.

At an annealing temperature of 250 °C and above for t = 60 s, Ni is fully consumed as it reacts with InGaAs to form a uniform Ni-InGaAs layer. Fig.

3.10(c) shows the SIMS profile of a Ni-InGaAs layer formed on InGaAs using a 250 °C 60 s anneal. A layer containing a relatively homogenous distribution of Ni, In, Ga, and As elements on InGaAs layer is observed. The reaction of Ni with InGaAs is complete, as no excess Ni is observed on the Ni-InGaAs. This is also confirmed with XRD, where the peak associated with the as-deposited Ni disappears for the sample annealed at 250 °C 60 s, as shown in the plot in Fig. 3.11.

As the formed layer is thicker than the as-deposited Ni thickness, it can be inferred that Ni-InGaAs has a higher resistivity value than Ni, which explains the increase in R_{sh}. The reaction between Ni and GaAs has been well reported to occur at temperatures as low as 220 °C, forming a metastable Ni_xGaAs [85]-[87]. As annealing at temperatures between 200 and 250 °C was not explored in this work, there could also be possibility that Ni can also react with InGaAs at temperatures below 250 °C.

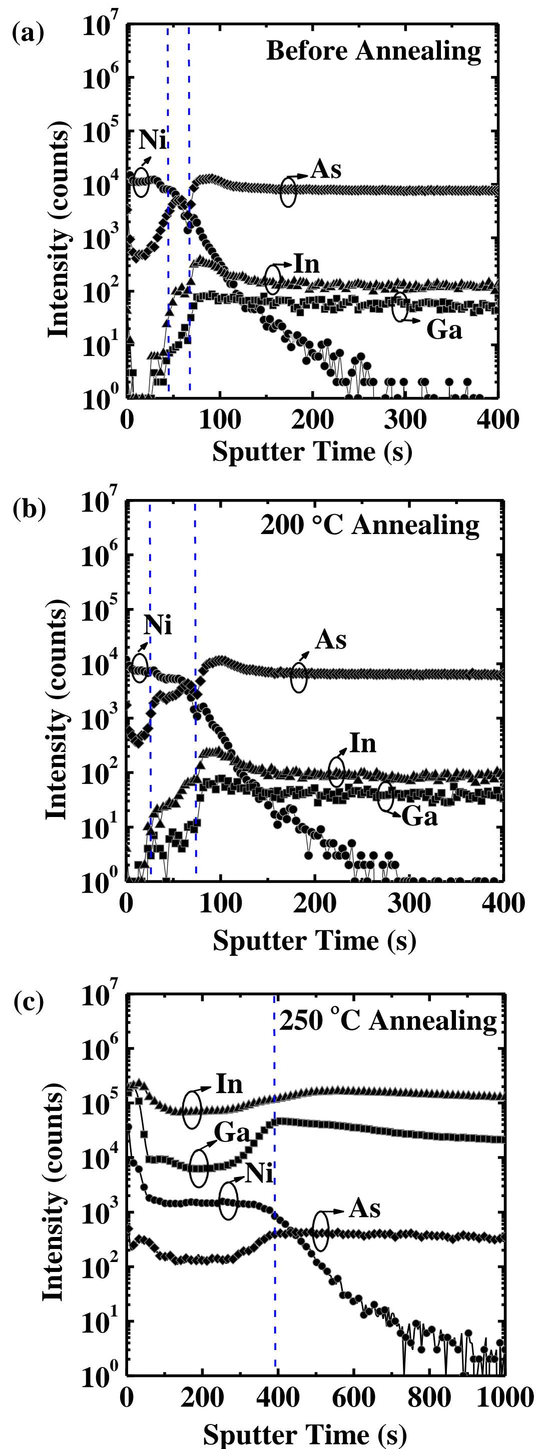


Fig. 3.10. Negative ion Secondary Ion Mass Spectrometry (SIMS) depth profiles of Ni, In, Ga, and As for ~11 nm Ni on InGaAs (a) before and (b) after annealing at 200 °C for 60 s. The dotted lines represent the region where Ni and InGaAs could have intermixed even before annealing. (c) Ni, In, Ga, and As positive ion SIMS depth profiles of Ni-InGaAs formed at 250 °C for 60 s. The Ni-InGaAs/InGaAs interface is represented by dotted line.

For the film formed by annealing Ni/InGaAs at 300 ºC for 60 s, two additional peaks associated with $Ni_4InGaAs_2$ (101) and (201) were observed in the XRD data. This suggests that there is a slight difference in orientation between the film formed at 300 ºC and that formed at 250 ºC. For the film formed at 350 ºC, an XRD peak is observed at 88º, and could be due to a slight difference in composition of Ni-InGaAs phase formed. A peak observed at 45.1º is believed to be from InNi or $Ni_{11}As_8$. This suggests the formation of a new phase at this temperature. A drop in R_{sh} value above 250 ºC in Fig. 3.9 may suggest that a thicker layer was formed or a reaction product with lower resistivity value was formed. The former is excluded as observed from the TEM analysis of the films [Fig. 3.11]. Therefore, the decrease of R_{sh} with increasing formation temperature is attributed to different bulk resistivities of the films formed. This study focused on a low reaction temperature of 250 °C for Ni-InGaAs formation which has been previously shown to form a good ohmic contact on n-type InGaAs. The results obtained in this study will be useful for achieving low thermal budget contact formation process, as a low thermal budget would be favorable for integration in InGaAs n-MOSFETs.

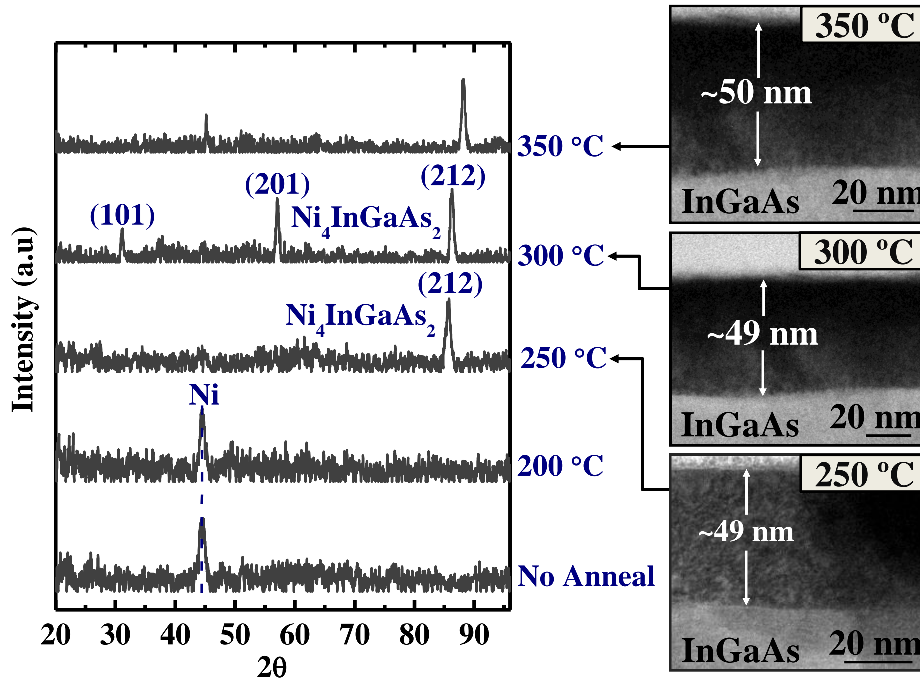


Fig. 3.11. XRD General Area Detector Diffraction System (GADDS) integrated diffraction intensity as a function of 2θ (left). TEM images showing the thicknesses of films formed at 250, 300, and 350 ºC (right).

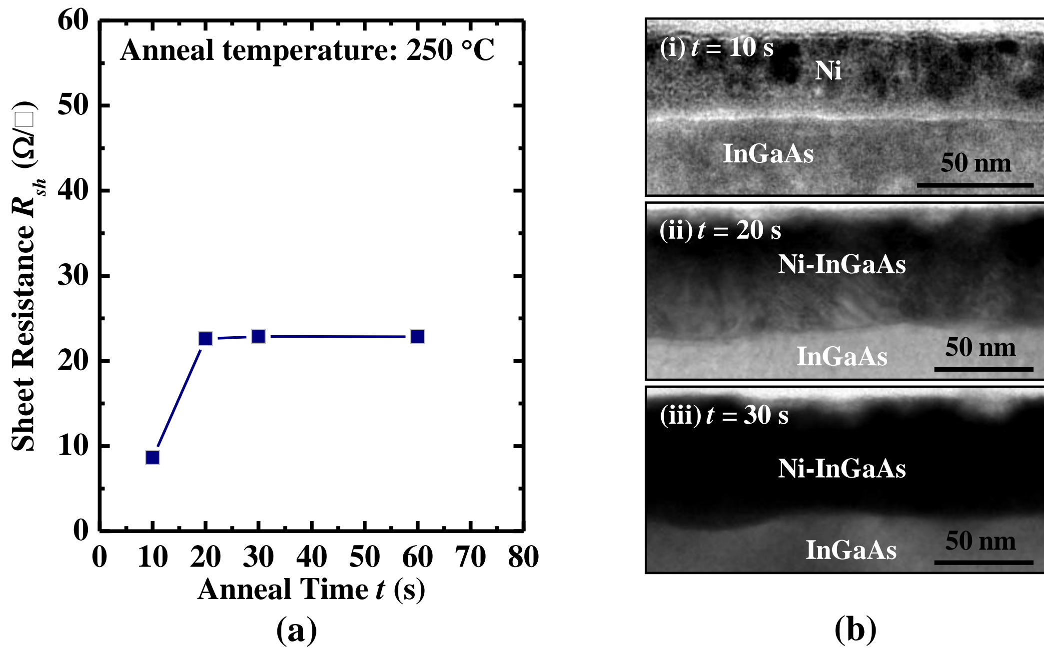


Fig. 3.12. (a) Time evolution of R_{sh} for ~28 nm of Ni deposited on InGaAs annealed at 250 °C. (b) Transmission electron microscopy (TEM) images of Ni-on-InGaAs annealed at 250 °C for (i) 10 s, (ii) 20 s, and (iii) 30 s.

The annealing time t was varied to study the time evolution of R_{sh} during Ni-InGaAs formation. A sample with ~28 nm Ni on InGaAs was cut into pieces, and each piece was separately annealed at 250 °C for 10, 20, 30, or 60 s. R_{sh} measurements were then performed using a microscopic four-point probe [98]-[99]. Fig. 3.12(a) plots R_{sh} as a function of annealing time. As the reaction between Ni and InGaAs proceeds over time, R_{sh} increases and then eventually saturates. An increase of R_{sh} from 8.6 to 22.6 Ω/square (or Ω /□) during the first 20 s signifies a reaction between Ni and InGaAs. R_{sh} saturates when the annealing time exceeds 20 s, with almost the same R_{sh} value obtained for t equals to 20, 30, and 60 s. This indicates that the reaction was completed within 20 s of annealing. We confirmed our observation with cross-sectional TEM characterization of Ni-on-InGaAs annealed for different durations as shown in Fig. 3.12(b). This also indicates that the 60 s annealing time used for R_{sh} comparison (Fig. 3.9) is sufficient to ensure all the as-deposited Ni reacted with InGaAs at various temperature.

To quantitatively determine the elemental composition of the Ni-InGaAs layer formed by 250 °C 60 s anneal, XPS characterization was performed. Fig. 3.13 shows the Ni $2p_{3/2}$, In $3d_{5/2}$, Ga $2p_{3/2}$, and As 3d XPS spectra of the Ni-InGaAs film where the atomic percentages of the elements in Ni-InGaAs were determined from the areas under the fitted curves. The Ni-InGaAs film shows average atomic concentrations of ~52%, ~10%, ~13%, and ~25% for Ni, In, Ga, and As, respectively. This corresponds to the atomic ratio of Ni : In : Ga : As = 4 : 1 : 1 : 2. This result is also consistent with the Energy Dispersive X-ray

Spectroscopy (EDX) analysis taken across the Ni-InGaAs film (Ni: In: Ga: As = ~52 : ~13 : ~10 : ~25), confirming that the phase of the formed layer is $Ni_4InGaAs_2$.

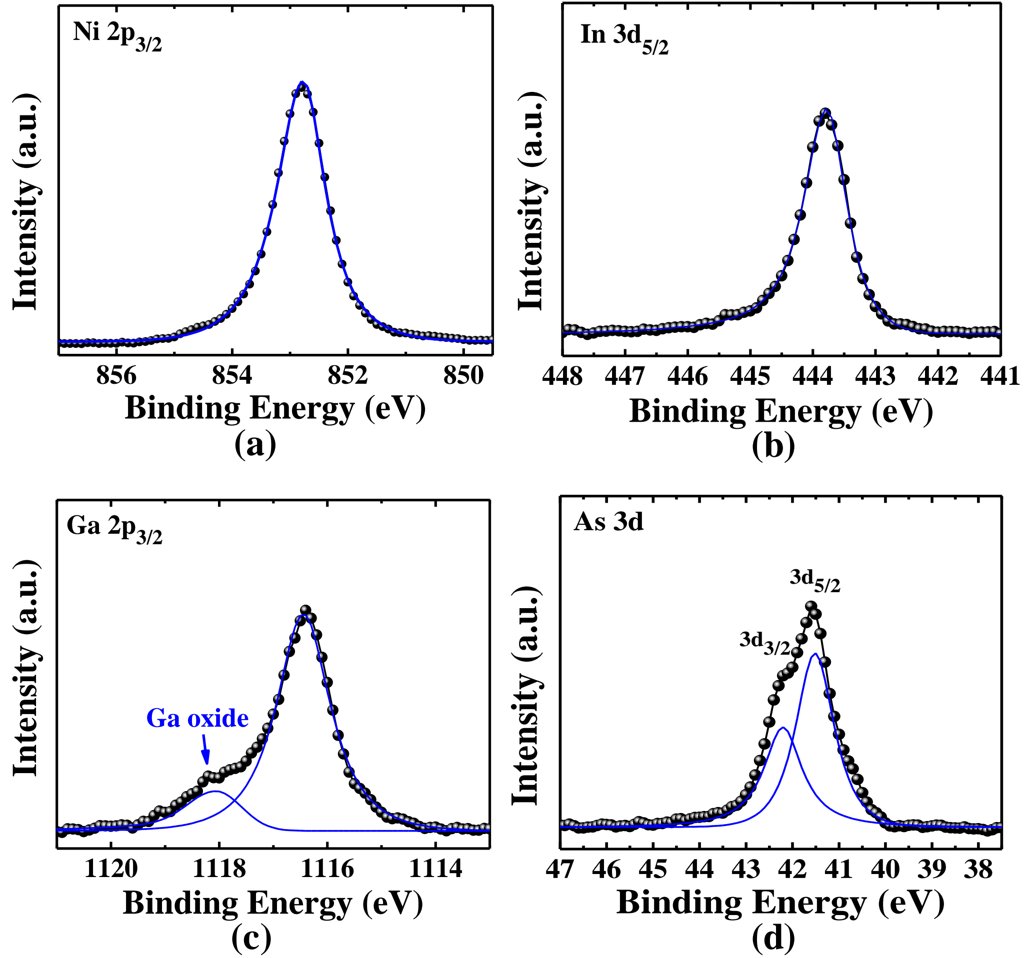


Fig. 3.13. X-ray Photoelectron Spectroscopy (XPS) spectra of (a) Ni $2p_{3/2}$, (b) In $3d_{5/2}$, (c) Ga $2p_{3/2}$, and (d) As 3d. The elemental composition of Ni-InGaAs was determined from the area under the fitted peaks (blue lines) excluding the Ga oxide peak.

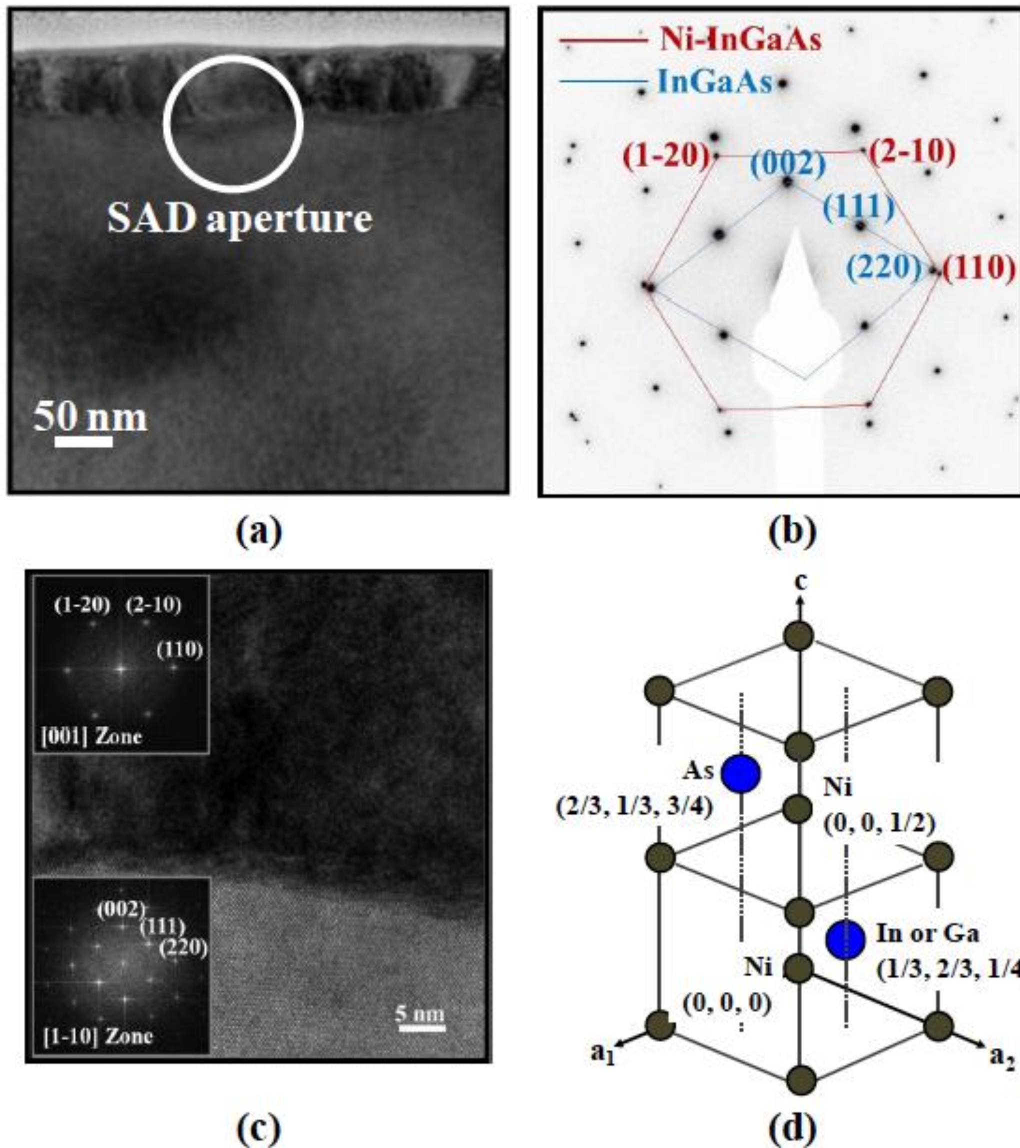
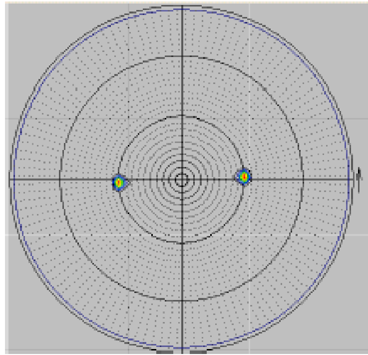


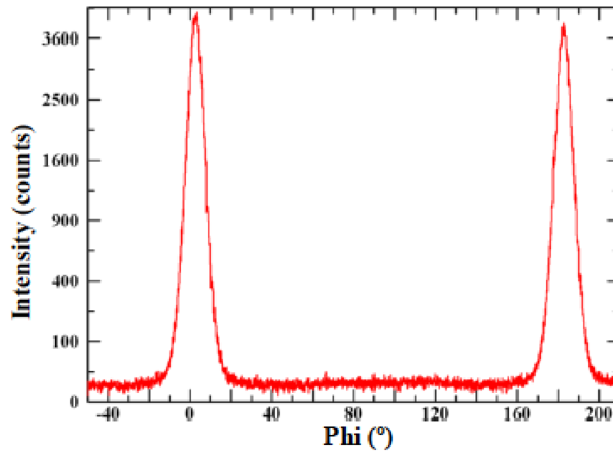
Fig. 3.14. (a) TEM image of Ni-InGaAs/InGaAs sample where selective area diffraction (SAD) pattern shown in (b) was recorded. The SAD aperture, as indicated by a circle, has a diameter of 150 nm. (c) High resolution TEM image of Ni-InGaAs/InGaAs with insets showing the corresponding diffraction patterns extracted by Fast Fourier Transform. (d) Unit cell of Ni-InGaAs phase, illustrating the NiAs (B8) structure of Ni-InGaAs.

The crystal structure of Ni-InGaAs was investigated with HRTEM and XRD. The selective area diffraction (SAD) pattern shown in Fig. 3.14(b) was taken from a cross-section TEM [Fig. 3.14(a)], in the region indicated by a white

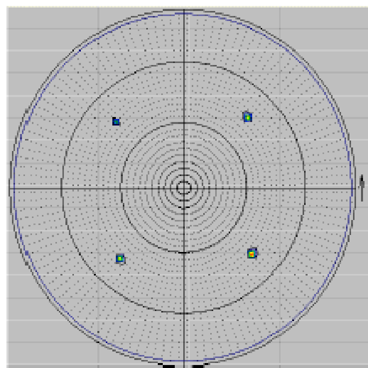
circle, covering both the Ni-InGaAs layer and the InGaAs layer below. The recorded SAD pattern shows highly epitaxial Ni-InGaAs overlayer formed on InGaAs. By analyzing the diffraction pattern obtained by Fast Fourier transform [Fig. 3.14(c)], a hexagonal crystal structure was identified for the Ni-InGaAs film. The lattice parameters of Ni-InGaAs was calculated to be $a = 0.396 \pm 0.002$ nm and $c = 0.516 \pm 0.002$ nm. The orientation relationship was further probed with XRD pole figure measurement through phi-scan (phi denotes a rotation angle around the surface normal to the sample surface) at fixed 2θ corresponding to Ni-InGaAs(110) and InGaAs(220) [Fig. 3.15]. For Ni-InGaAs(110), we observed two peaks located 180° apart, indicating diffraction from a single crystal. This suggests that Ni-InGaAs is an epitaxial film throughout. The epitaxial relationship has orientation of Ni-InGaAs $[\bar{1}10]$ //InGaAs $[001]$ and Ni-InGaAs$[110]$//InGaAs$[110]$.

Ni-InGaAs(110)





InGaAs(220)



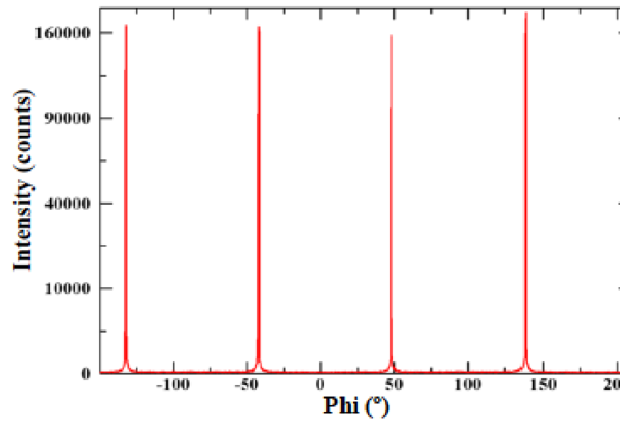


Fig. 3.15. X-ray pole figure (left) and the corresponding phi-scan (right) of Ni-InGaAs and InGaAs obtained from (110) and (220) diffraction planes.

Both the composition and structure of Ni-InGaAs suggest that it adopts a NiAs (B8) type of structure [92]-[94]. In the NiAs (B8) structure, transition metal atoms form simple hexagonal sub-lattices which interpenetrate with hexagonal close-packed sub-lattices of metalloid atoms [92]-[94]. The construction model of a Ni-InGaAs unit cell is illustrated in Fig. 3.14(d). For Ni-InGaAs to possess a NiAs structure, the (0, 0, 0) and (0, 0, 1/2) positions are occupied by Ni atoms, whereas the (1/3, 2/3, 1/4) and (2/3, 1/3, 3/4) positions are occupied by a gallium (or indium) atom and an arsenic atom, respectively. This is similar to Ni_xGaAs

and Ni_xInAs (where $2 \leq x \leq 3$) formed by Ni reaction with GaAs and InAs respectively, which are also based on the NiAs (B8) structure [85],[86],[103],[104].

The consumption ratio of metal and silicon has been widely examined for nickel silicidation in Si complementary metal-oxide-semiconductor (CMOS) technology [105]-[107]. In this study, we also investigated the thickness ratio of Ni to Ni-InGaAs formed. The final Ni-InGaAs thickness is a function of the as-deposited Ni film thickness, if the Ni is fully consumed in the reaction. Ni-on-InGaAs samples with three different Ni thicknesses (~29 nm, ~21 nm, and ~12 nm) were prepared and annealed at 250 °C for 60 s to ensure all the as-deposited Ni was fully consumed and reacted with the InGaAs layer. The mechanism of Ni reaction with InGaAs could be similar to that of Ni/GaAs reaction, in which Ni atoms would predominantly diffuse through interstitial sites in the Ni-InGaAs phase to reach the Ni-InGaAs/InGaAs interface [108], where solid-state reaction between Ni and InGaAs takes place. The reaction process probably involves breaking of In (or Ga)-As bonds and formation of In (or Ga)-Ni bonds and As-Ni bonds, leading to a transition from zinc blende to hexagonal close-packed (HCP) NiAs (B8) crystal structure.

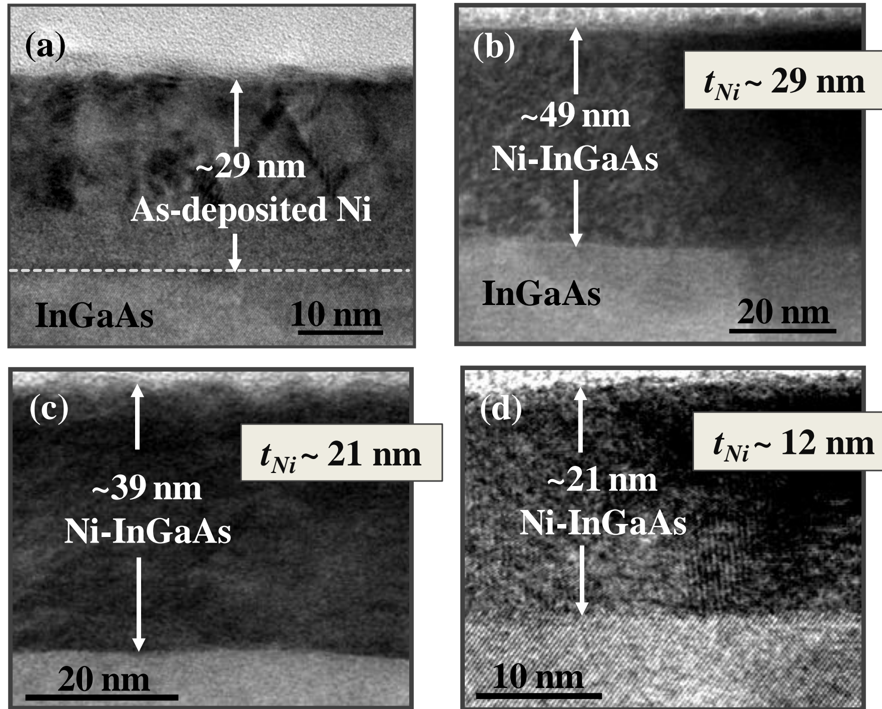


Fig. 3.16. TEM images of (a) ~29 nm as-deposited Ni on InGaAs, and (b) ~49 nm, (c) ~39 nm and (d) ~21 nm of Ni-InGaAs formed by annealing ~29 nm, ~21 nm and ~12 nm of as-deposited Ni on InGaAs, respectively.

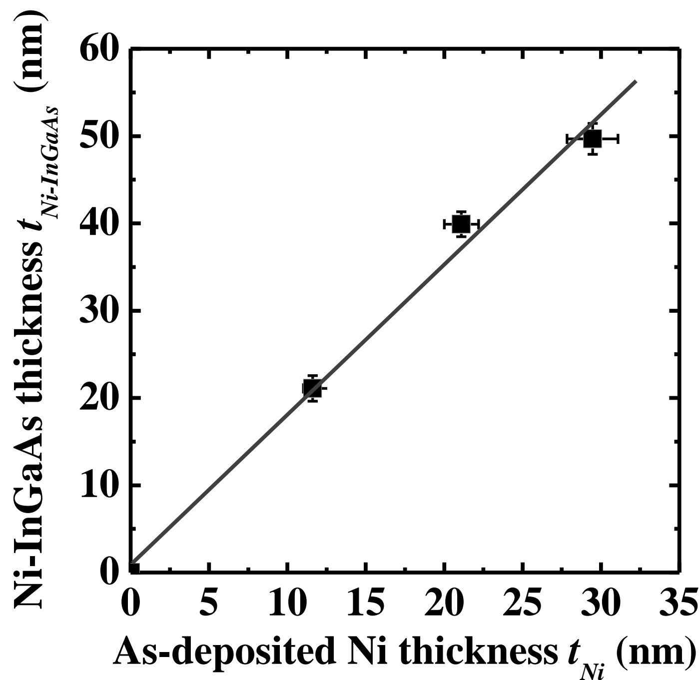


Fig. 3.17. Plot of Ni-InGaAs thickness versus as-deposited Ni thickness, showing a linear relationship. The thickness ratio of ~1 : 1.7 for Ni to Ni-InGaAs is obtained by linear fitting. Thicknesses of Ni-InGaAs and Ni were determined from TEM images.

Ni film with thicknesses of ~29 nm, ~21 nm, and ~12 nm formed Ni-InGaAs with thicknesses of ~49 nm, ~39 nm, and ~21 nm, respectively, as observed from TEM images shown in Fig. 3.16. Fig. 3.17 plots the resulting Ni-InGaAs thickness $t_{Ni\text{-}InGaAs}$ versus as-deposited Ni thickness t_{Ni}. The ratio of the Ni to Ni-InGaAs thicknesses is ~1 : 1.7, as obtained from the slope of the fitted line. This means that one thickness unit of Ni reacts with InGaAs to form 1.7 thickness units of Ni-InGaAs.

With the thickness ratio of Ni to Ni-InGaAs known, the final Ni-InGaAs thickness can be engineered by controlling the as-deposited Ni thickness. This was used to get R_{sh} as a function of $t_{Ni\text{-}InGaAs}$ as well as to extract the resistivity of the Ni-InGaAs film in the next Section. The information on thickness ratio, $t_{NiInGaAs}/t_{Ni}$ (Fig. 3.17) could also be very useful for the process design and fabrication of nanoscale InGaAs MOSFETs. For instance, InGaAs MOSFET having a gate length of less than 20 nm, ultra-shallow n^+/p S/D junctions of less than 10 nm would be required, and the thickness of the Ni-InGaAs contact should be less than 10 nm. With known thickness ratio, a desired Ni-InGaAs thickness can be precisely controlled.

3.3.3 Ni-InGaAs Sheet Resistance Uniformity and Bulk Resistivity

The Ni-InGaAs film uniformity was investigated by sheet resistance mapping of a ~46-nm-thick Ni-InGaAs film. Sheet resistance mapping was performed using a microscopic four-point probe [98]-[99], in which the adjacent probe tips are separated by ~10 μm. The small probe spacing ensures an accurate

R_{sh} measurement of the Ni-InGaAs film [99]. R_{sh} measurements were taken at 121 locations in a 11×11 matrix, in which a 100 μm step was taken in both y and z directions. The R_{sh} scan domain covered a 1 mm × 1 mm area. A contour map showing the Ni-InGaAs R_{sh} distribution in this area is plotted in Fig. 3.18. Different grayscale colors were used to represent the R_{sh} values ranging from 20.5 to 22.5 Ω/square, with a contour interval of 0.5 Ω/square as shown in the scale bar. The R_{sh} values show very good uniformity. The mean R_{sh} is 21.4 Ω/square and the standard deviation is 0.4 Ω/square.

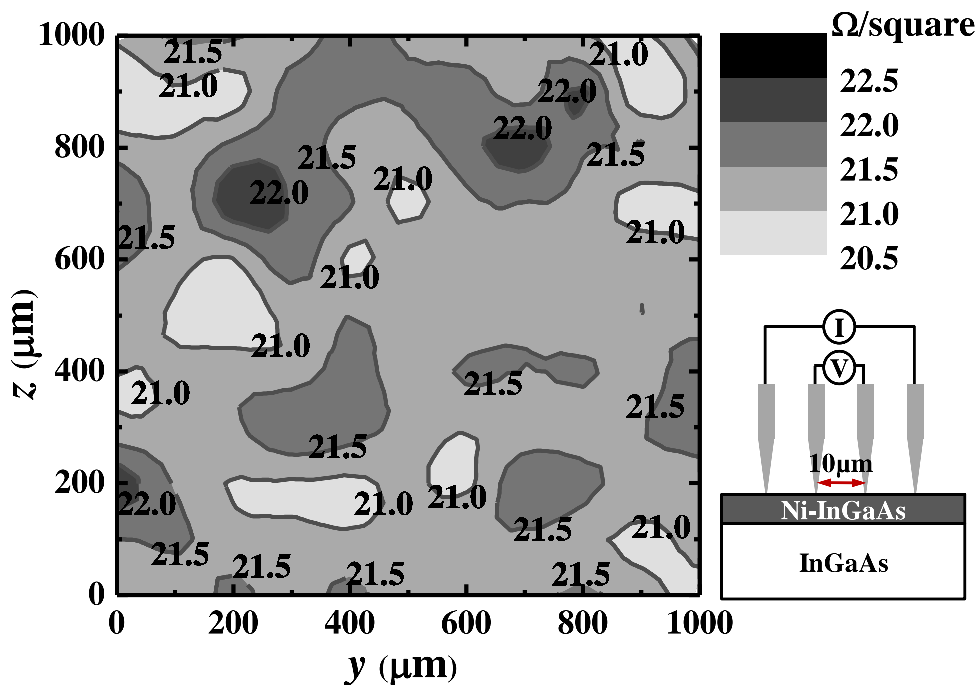


Fig. 3.18. Contour plot of sheet resistance of ~46-nm-thick Ni-InGaAs film in a 1 mm × 1 mm area as obtained by microscopic four-point probe. In the scale bar (top right), sheet resistance values range from 20.5 Ω/square to 22.5 Ω/square, with an interval of 0.5 Ω/square. A schematic diagram (bottom right) shows the microscopic four-point probe with probe spacing of ~10 μm used for R_{sh} measurement.

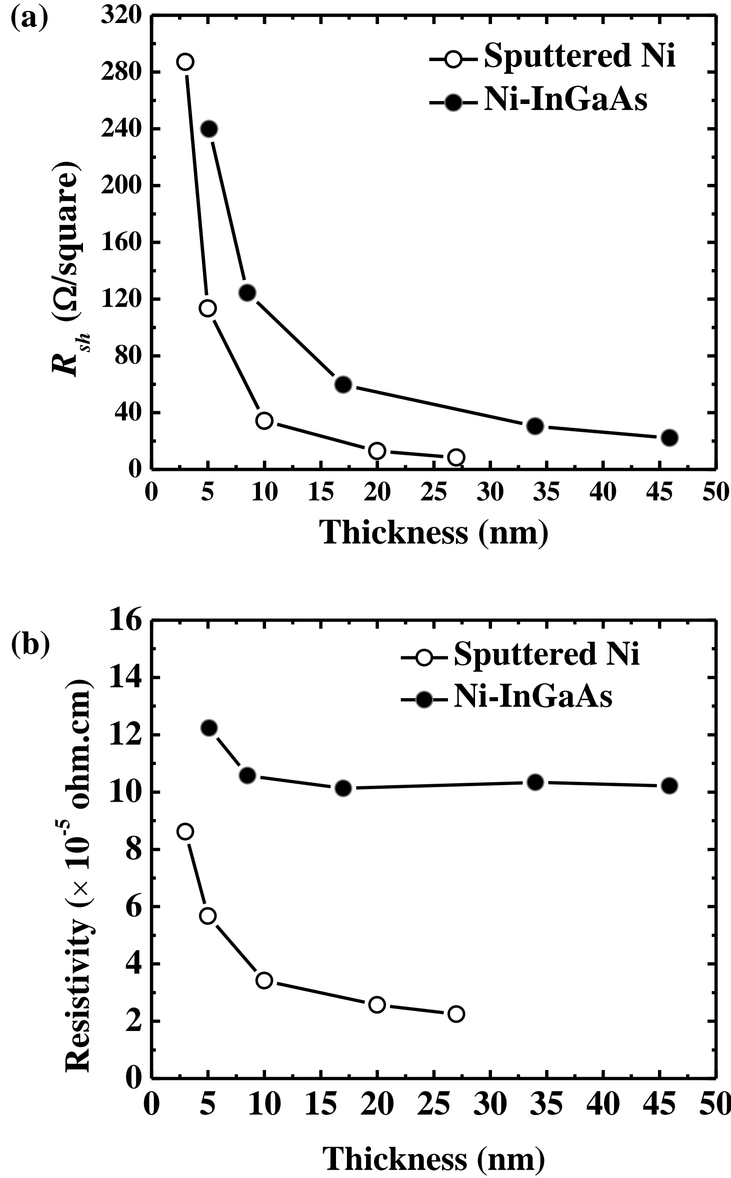


Fig. 3.19. (a) R_{sh} of Ni and Ni-InGaAs as a function of thickness. (b) The electrical resistivity of Ni and Ni-InGaAs extracted from their R_{sh} values and thicknesses. The thickness of Ni-InGaAs is obtained by multiplying the as-deposited Ni thickness and the thickness ratio (1.7) of Ni to Ni-InGaAs.

Furthermore, in order to study the effect of Ni-InGaAs film thickness on the electrical resistivity of Ni-InGaAs, Ni films with t_{Ni} of ~3, 5, 10, 20, and 27 nm were deposited on p-type $In_{0.53}Ga_{0.47}As$ on InP substrates. R_{sh} measurements were performed before and after annealing the samples at 250 °C for 60 s, as

plotted in Fig. 3.19(a). With $t_{Ni\text{-}InGaAs}$ much smaller than the micro-probe spacing, a strong dependence of the measured R_{sh} on $t_{Ni\text{-}InGaAs}$ is expected. The electrical resistivity of Ni-InGaAs film ($\rho_{Ni\text{-}InGaAs}$) was deduced from the values of R_{sh} and $t_{Ni\text{-}InGaAs}$ using

$$\rho_{Ni\text{-}InGaAs} = R_{sh} \times t_{Ni\text{-}InGaAs}\,, \tag{3.3}$$

where $t_{Ni\text{-}InGaAs}$ was determined from t_{Ni} and the thickness ratio of Ni to Ni-InGaAs obtained earlier.

Fig. 3.19(b) plots Ni-InGaAs film resistivity as a function of film thickness. The resistivity of Ni-InGaAs is almost a constant at ~102 μΩ·cm for $t_{Ni\text{-}InGaAs}$ ranging from ~10 nm to ~46 nm. This value is ~5 times higher than that of the sputtered Ni film of this work. The contribution of surface scattering to the total resistivity value starts to dominate when the film thickness is less than 10 nm, leading to an increase in the resistivity value for thinner films. The higher resistivity values for films thinner than 10 nm should be considered when a thin Ni-InGaAs contact layer is used in devices as it contributes to the total series resistance. Nonetheless, Ni-InGaAs film can also be considered for S/D extension as the R_{sh} of 5 – 10 nm Ni-InGaAs layer still meets the 10 nm international technology roadmap for semiconductors (ITRS) roadmap requirement for shallow junctions.

Table 3.1 summarizes the comparison between Ni-InGaAs and CoInGaAs. The comparison indicates that Ni-InGaAs has better material characteristics suitable for InGaAs self-aligned S/D technology than CoInGaAs.

Table 3.1 Comparison between Ni-InGaAs and CoInGaAs.

	Ni-InGaAs	**CoInGAs**
Formation temperature	250 ºC	350 ºC
Material crystallinity	Single crystalline	Polycrystalline
Film quality	Uniform with distinct interface with underlying InGaAs	Non-uniform with rough interface with underlying InGaAs
Electrical resistivity	~1,020 Ω·nm	~945 Ω·nm
Contact resistivity with n-type InGaAs (~10^{19} cm^{-3})	~3.4×10^{-5} $\Omega \cdot cm^2$	~6.25×10^{-4} $\Omega \cdot cm^2$
Availability of selective wet-etchant	HCl, HNO_3	HNO_3

3.4 Summary

In summary, Ni reacts with InGaAs to form $Ni_4InGaAs_2$ (known as Ni-InGaAs) at a temperature as low as 250 °C. The vacuum work function of Ni-InGaAs and band alignment at Ni-InGaAs/$In_{0.53}Ga_{0.47}As$ interface were investigated using photoelectron spectroscopy (UPS and XPS). The vacuum work function of Ni-InGaAs was measured by UPS to be ~5.1 eV. The Fermi level of Ni-InGaAs at the interface is aligned near the conduction band of $In_{0.53}Ga_{0.47}As$. Ni-InGaAs forms a good ohmic contact to n-type InGaAs. It is determined that Ni-InGaAs has a hexagonal NiAs (B8) crystal structure. It exhibits an epitaxial relationship with orientation of Ni-InGaAs $[\bar{1}10]$//InGaAs $[001]$ and Ni-InGaAs $[110]$//InGaAs $[110]$. The electrical resistivity of Ni-InGaAs was determined to be ~102 μΩ·cm down to $t_{Ni\text{-}InGaAs}$ of 10 nm, below which the resistivity value starts to dramatically increase.

Chapter 4

N-Channel InGaAs Field-Effect Transistors on Germanium-on-Insulator Substrates with Self-Aligned Ni-InGaAs Source/Drain

4.1 Introduction

The study of nickel reaction with InGaAs was presented in Chapter 3 and reported in Ref. [88]-[89] by the author. A selective wet-etch process to selectively remove unreacted Ni without substantially etching Ni-InGaAs was also developed and reported in Ref. [109], in which the author also contributed. The next important assessment is the adoption of Ni self-aligned metallization in InGaAs transistors. This will be presented in this Chapter.

Most of the high-performance InGaAs MOSFETs were realized on InGaAs grown on lattice-matched indium phosphide (InP) substrates [110]-[117]. However, InGaAs eventually needs to be integrated on Si substrates for logic applications, due to cost considerations. The challenges associated with heterogeneous integration of III-V on Si were elaborated in Chapter 1. In this Chapter, the integration of InGaAs n-MOSFETs on GeOI on Si platform is explored.

In addition, the incorporation of Pt in NiSi and NiGe films has been reported to improve the thermal stability of the films [119]-[123]. Hence, the study of adding Pt in Ni-InGaAs film is also presented in this Chapter.

In this Chapter, the electrical contact resistivity of Ni-InGaAs on n-InGaAs is determined. InGaAs transistor with Ni-InGaAs as self-aligned S/D material is demonstrated on InGaAs epitaxially grown on lattice-matched InP substrate. This self-aligned Ni metallization scheme is also employed in the integration of InGaAs n-MOSFETs on GeOI on silicon substrate. The on-state current performance and intrinsic transconductance of InGaAs MOSFETs integrated on GeOI on Si substrate are compared with those of InGaAs MOSFETs fabricated on InGaAs epitaxially grown on lattice-matched InP substrates, as well as on InGaAs directly grown on Si (InGaAs-on-Si) substrates. In addition, the effect of Pt incorporation in Ni-InGaAs film is studied by examining the electrical and physical characteristics of the film.

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4.2 Extraction of Contact Resistivity

In Chapter 3, it was shown that the Fermi level of Ni-InGaAs is aligned close to the conduction band of InGaAs and hence it would form a good ohmic contact on n-type InGaAs. In this Section, the electrical contact resistivity ρ_c of Ni-InGaAs on n-type InGaAs is extracted through transfer length method (TLM) test structure [124]-[125].

Schematics summarizing the TLM key fabrication steps are illustrated in Fig. 4.1(a). The TLM test structure fabrication went through the following process

steps. A wafer consisting of an epitaxial 100-nm-thick n-type $In_{0.53}Ga_{0.47}As$ (Si-doped) with doping concentration N_D of ~2×10^{19} cm^{-3} on p-type $In_{0.53}Ga_{0.47}As$ (Be-doped) with doping concentration N_A of ~1×10^{17} cm^{-3}, grown on 2 inch InP wafers (N_A of ~1×10^{19} cm^{-3}) was used as the starting substrate. Such wafer is commercially available and was purchased for this work. A thin SiO_2 (~15 nm) was deposited on the wafer surface and n-type InGaAs mesas were patterned and defined by wet etching with citric acid (citric acid:H_2O_2 = 20:1) reaching the p-type InGaAs layer. The thin SiO_2 was then removed and contact holes were patterned on the mesas to expose regions where metal pads with various inter-pad spacings would be formed. A 10-nm-thick Ni deposition was performed followed by lift-off process. Sample was then annealed at 250 ºC in rapid thermal processing (RTP) tool for Ni-InGaAs formation. Finally, thick Ni (~200 nm) metal pads were deposited on the Ni-InGaAs metal pads to reduce the total resistance of the metal. The optical microscope image showing the top view of the fabricated TLM structure is shown in Fig. 4.1(b).

Fig. 4.2(a) shows current-voltage (I-V) characteristics obtained from two adjacent metal pads with various contact spacings d. The contact spacings are 3, 4, 5, 6, 7, 8, 9, 10, 15, 20, 25, 30, 35, 40, 45, 50, and 55 μm. The total resistance R_{Total} between contacts for various contact spacings is plotted versus d as shown in Fig. 4.2(b). From the R_{Total}-d plot, the sheet resistance of the n-type InGaAs, contact resistance, and transfer length can be obtained. The sheet resistance of the n-type InGaAs was extracted from the slope of the plot. The intercept at d = 0 gives the value of the contact resistance R_c from the two metal contacts. The

transfer length L_T of the two metal contacts was determined when the total resistance is zero. From these parameters, the contact resistivity ρ_c was extracted using:

$$R_c = \frac{V}{I} = \frac{\rho_c}{L_T Z}\coth(L/L_T), \qquad (4.1)$$

for $L \leq 0.5L_T$, $\rho_c \approx R_c \times L \times Z$,

for $L \geq 1.5L_T$, $\rho_c \approx R_c \times L_T \times Z$,

where L and Z are the length and width of Ni-InGaAs metal pad [Fig. 4.1(b)], respectively.

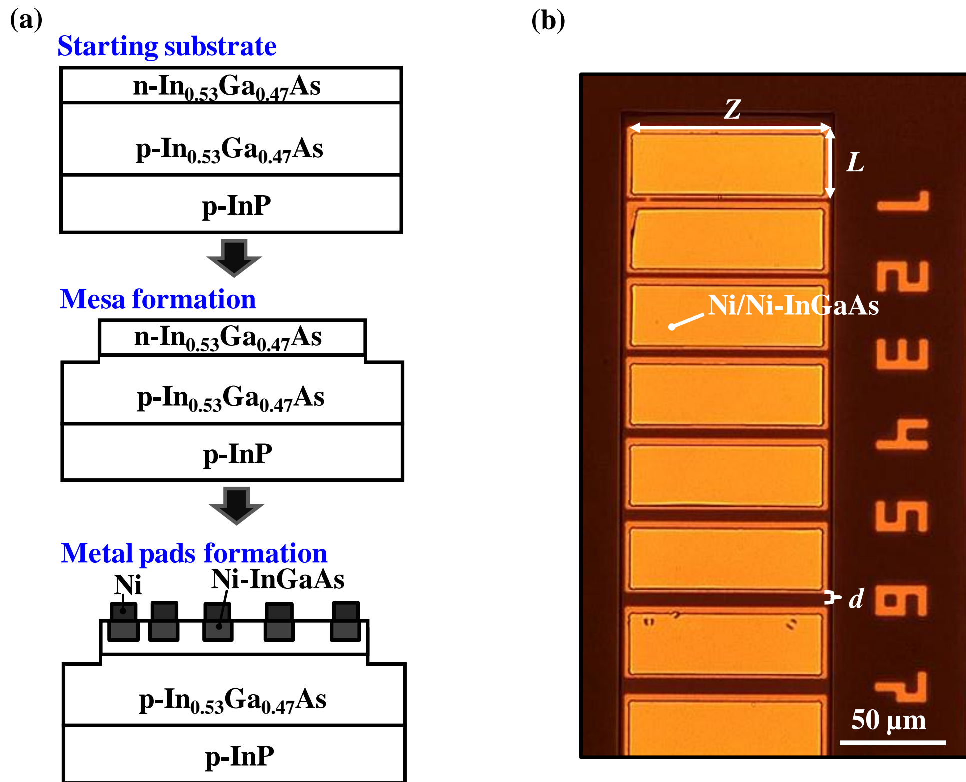

Fig. 4.1. (a) Schematics of TLM test structure fabrication featuring mesa formation, Ni-InGaAs formation, and thick Ni metal pads deposition. (b) Optical microscope image showing the top view of the fabricated TLM test structure. *L* and *Z* are the length and width of Ni-InGaAs metal pad, respectively, while *d* is the distance between two adjacent metal pads.

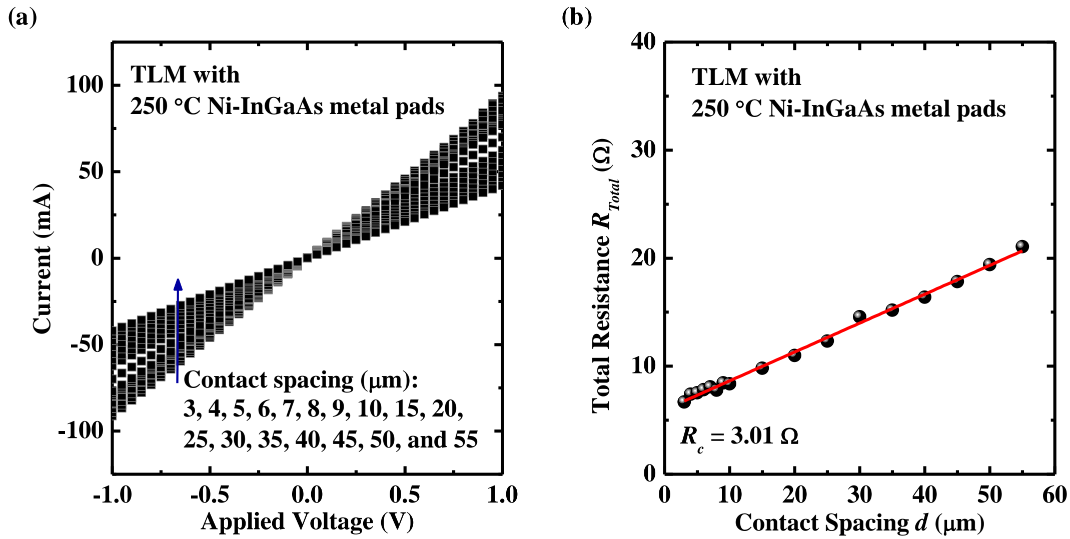

Fig. 4.2. (a) *I-V* curves obtained from a TLM test structure with Ni-InGaAs metal contacts formed at 250 °C, showing ohmic behavior on n-$In_{0.53}Ga_{0.47}As$. (b) Total resistance versus Ni-InGaAs contact spacing determined from the *I-V* curves.

From the intercept of the linear fitted line with the vertical axis [Fig. 4.2(b)], Ni-InGaAs/n-InGaAs contact resistance of ~301 Ω·μm is obtained. The sheet resistance $R_{sh,InGaAs}$ of the n-InGaAs and the transfer length are ~26 Ω/square and 11.4 μm, respectively. Thus, the calculated contact resistivity is ~3.4×10^{-5} $\Omega\cdot cm^2$. This extracted value suggests that Ni-InGaAs has lower contact resistivity than CoInGaAs. The realization of InGaAs n-MOSFETs with Ni-InGaAs as S/D material is presented in Section 4.3.

4.3 InGaAs n-MOSFETs with Ni-InGaAs as Self-Aligned S/D material

The fabrication process flow of InGaAs channel n-MOSFETs with self-aligned Ni-InGaAs S/D is summarized and illustrated in Fig. 4.3. The starting

substrate was a 500-nm-thick p-type $In_{0.53}Ga_{0.47}As$ epitaxially grown on p-type bulk InP wafer. This was also a commercially available wafer which was purchased for this work. After pre-gate cleaning with HCl and NH_4OH solutions for native oxide removal, the sample was dipped in $(NH_4)_2S$ solution for surface passivation to suppress surface oxidation when transferring the sample to atomic layer deposition (ALD) chamber for gate dielectric deposition. ~6 nm aluminium oxide (Al_2O_3) was deposited followed by a post-deposition annealing at 400 ºC 60 s. Tantalum nitride (TaN) gate electrode was then sputtered, followed by gate patterning using optical lithography and etching in Cl_2-based plasma. After the gate stack formation, sample was dipped in diluted hydrofluoric acid ($HF:H_2O$ = 1:100) to remove Al_2O_3 at the source and drain region prior to Ni sputter deposition. The sputter condition for Ni deposition is the same as the one employed in Chapter 3. The sample was then annealed at 250 ºC 60 s for ~40 nm Ni-InGaAs formation at source and drain regions. The fabrication process was completed with the removal of unreacted Ni using undiluted HCl solution at room temperature. HCl was chosen due to its high etching selectivity value of ~15 (etch rate for Ni and Ni-InGaAs is 60 nm/min and 4 nm/min, respectively) [109].

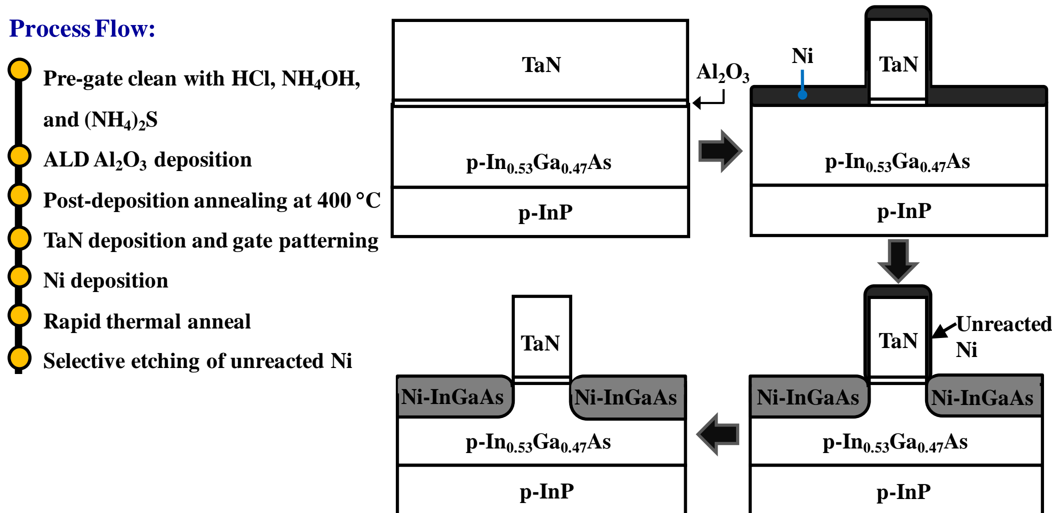

Fig. 4.3. Process flow and schematics of the key process steps in the fabrication of $In_{0.53}Ga_{0.47}As$ n-MOSFETs with self-aligned Ni-InGaAs metal S/D.

Fig. 4.4(a) shows the I_{DS}-V_{GS} and I_G-V_{GS} characteristics of a transistor with gate length of 2 µm at applied drain voltage V_{DS} of 0.1 and 1.1 V. From the linear extrapolation of I_{DS}-V_{GS} at V_{GS} where transconductance $G_{m,ext}$ is maximum, the threshold voltage V_{TH} of -0.172 V was obtained for this device. The device exhibits an on-state current of ~160 µA/µm at gate overdrive (V_{GS}-V_{TH}) of 2.5 V. The device exhibits on-state to off-state current ratio (I_{on}/I_{off}) of ~10^3. The I_{DS}-V_{DS} of the transistor at various gate overdrives (V_{GS}-V_{TH}) from 0 to 2.5 V in steps of 0.5 V are plotted in Fig. 4.4(b). The device demonstrates good saturation and pinch-off characteristics.

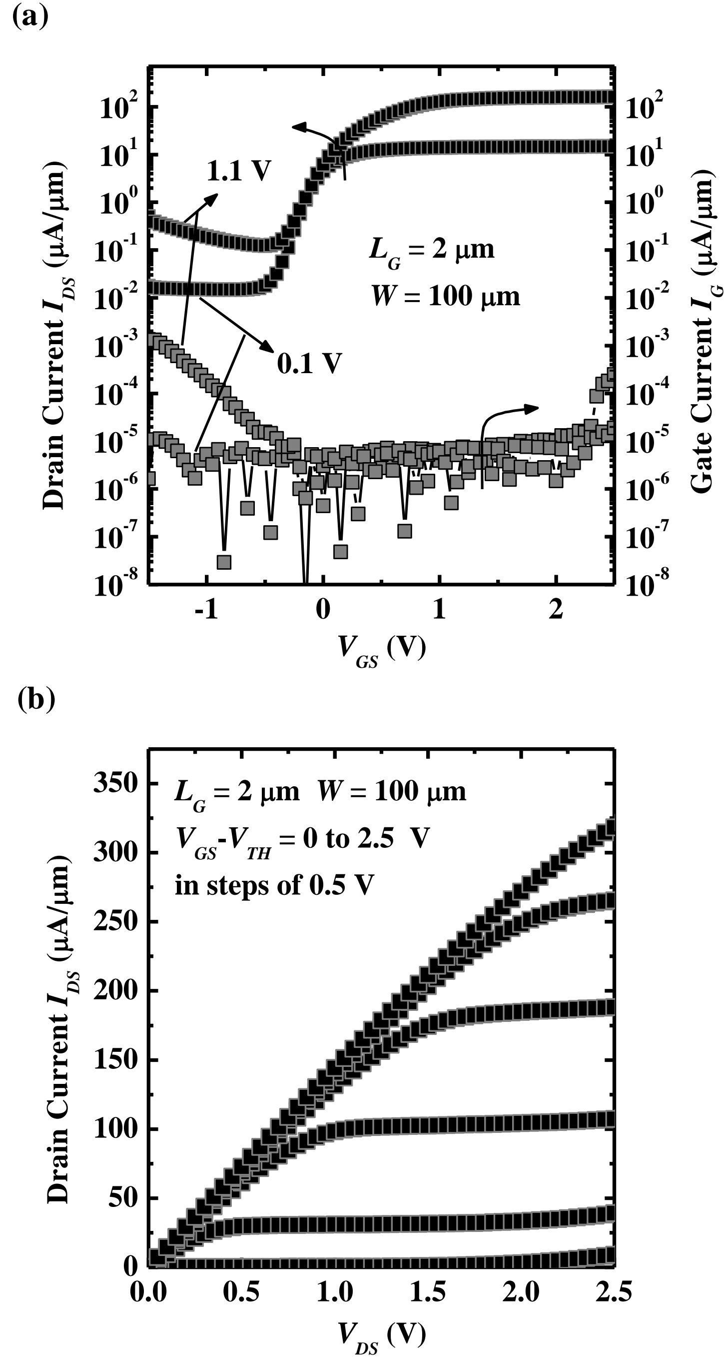

Fig. 4.4. (a) I_{DS}-V_{GS} and I_G-V_{GS} characteristics of a $In_{0.53}Ga_{0.47}As$ n-MOSFET with self-aligned Ni-InGaAs S/D. The gate length and gate width are 2 μm and 100 μm, respectively. The gate current is referred to the right axis. (b) I_{DS}-V_{DS} characteristics for the same $In_{0.53}Ga_{0.47}As$ n-MOSFET at gate overdrive V_{GS}-V_{TH} from 0 to 2.5 V in steps of 0.5 V.

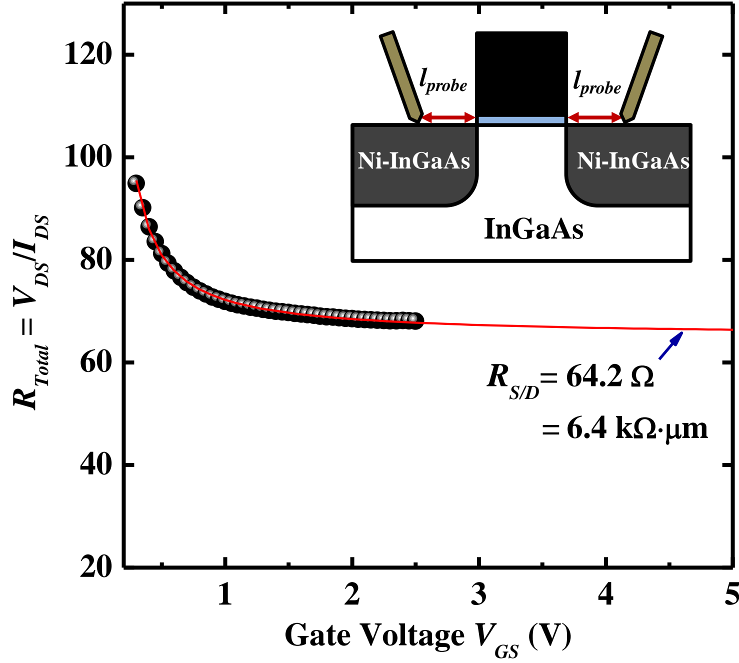

Fig. 4.5. Total resistance ($R_{Total} = V_{DS}/I_{DS}$) as a function of gate voltage of the same device as in Fig. 4.4. I_{DS} is the drain current in the linear regime (V_{DS} = 0.1 V). Higher applied gate voltage causes the channel resistance to reduce which leads to a reduction in the total resistance of the device. The resistance at high V_{GS} gives the $R_{S/D}$ value.

The extracted S/D series resistance ($R_{S/D} = V_{DS} / I_{DS}$ at V_{DS} = 0.1) of this device was normalized to the gate width which gave 6.4 kΩ·µm (Fig. 4.5). Ni-InGaAs S/D layer contributed ~3 kΩ·µm to the total $R_{S/D}$ as calculated from the Ni-InGaAs sheet resistance and the ~50 µm distance between the measurement probe and channel edge (l_{probe}) (inset of Fig. 4.5). This value is ~50% of the extracted $R_{S/D}$, which indicates that there is at least another parasitic resistance component other than Ni-InGaAs S/D layer. The resistance component other than that of Ni-InGaAs layer is from the contact resistance between Ni-InGaAs and the inversion layer of the InGaAs channel. The relatively high contact resistance contribution could be due to the following possible reasons: (1) the presence of

interfacial dipole at Ni-InGaAs/InGaAs interface (as interpreted from XPS results in Chapter 3) causes sharp band bending of InGaAs at the Ni-InGaAs/InGaAs interface which contributes to the high contact resistance, (2) the electron barrier height between Ni-InGaAs and inversion InGaAs layer is larger than that of Ni-InGaAs and p-type InGaAs (extracted in Chapter 3).

The total resistance of this device at V_{DS} and V_{GS}-V_{TH} of 0.5 V is ~16.9 kΩ·μm. The extracted series resistance ~6.4 kΩ·μm of this device contributes ~37.9% to the total resistance of the device. Further optimization can be performed to further reduce the resistance contribution from Ni-InGaAs S/D and the contact resistance of Ni-InGaAs/InGaAs inversion layer. For instance, the resistance contribution from Ni-InGaAs S/D layer can be further reduced by placing thick metal plugs very close to the channel to minimize the l_{probe} spacing. For example, 10× reduction of l_{probe} will lead to 10× reduction in the resistance contribution of Ni-InGaAs S/D. On the other hand, the contact resistance between Ni-InGaAs layer and InGaAs inversion layer can be further reduced by inserting a highly doped n^+-InGaAs layer [126] in between the two layers. This can lead to contact resistance reduction by one order of magnitude [126].

Fig. 4.6 shows the extrinsic transconductance $G_{m,ext}$ of the same device as in Fig. 4.4. The peak $G_{m,ext}$ at V_{DS} of 1.1 V is 150 μS/μm. The peak intrinsic transconductance $G_{m,int}$ was extracted by taking out the effect of $R_{S/D}$ using [127]:

$$G_{m,\text{int}} = \frac{G_m^o}{1-(R_S+R_D)\bullet G_D(1+R_S\bullet G_m^o)}, \qquad (4.2)$$

$$\text{where} \quad G_m^o = \frac{G_{m,ext}}{1 - R_S \bullet G_{m,ext}}.$$

The $G_D = \frac{\partial I_{DS}}{\partial V_{DS}}$ is the measured drain conductance. R_S and R_D are the resistance of source and drain, respectively. In long channel device, G_D is negligible and hence $G_{m,int}$ equals to G_m^o. The extracted peak $G_{m,int}$ of this device is ~288.5 μS/μm. This extracted $G_{m,int}$ value is free from series resistance effect and is directly related to the carrier mobility. The $G_{m,int}$ value extracted here together with other reported values in the literature, would be used for performance benchmarking when InGaAs n-MOSFETs were realized on InGaAs on silicon substrate in Section 4.4.

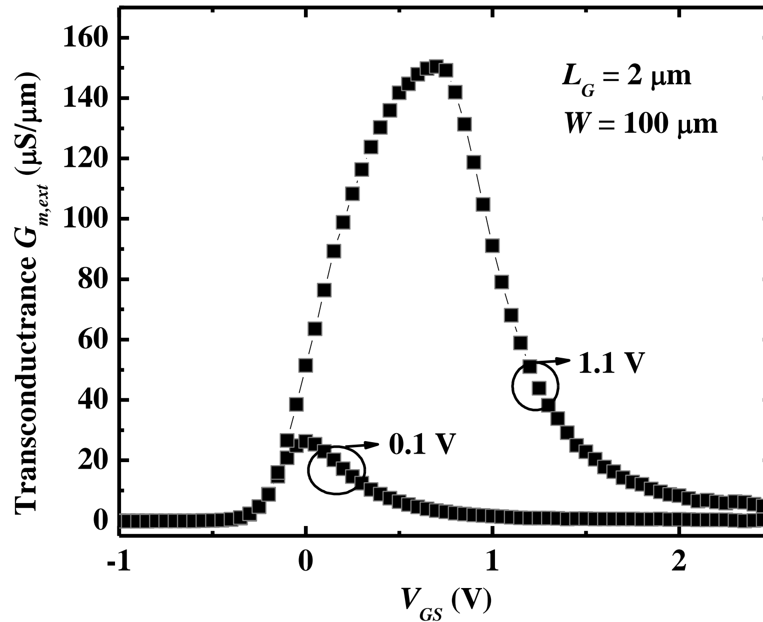

Fig. 4.6. Extrinsic transconductance $G_{m,ext}$ of the same device as in Fig. 4.4 at V_{DS} of 0.1 and 1.1 V.

4.4 InGaAs n-MOSFETs Formed on Germanium-on-Insulator on Si Substrate

The InGaAs on GeOI on Si substrate was grown using molecular beam epitaxy (MBE) system by our collaborator (Professor S.-F. Yoon's group) at Nanyang Technological University (NTU). GeOI on silicon substrate having a (001) Ge surface with a 10° offcut towards <111> was used for the MBE growth. Such GeOI substrates are commercially available and may be formed by layer transfer of Ge onto a SiO_2-covered Si substrate. The GeOI on Si substrate was annealed in ultrahigh vacuum at 650 °C for 30 minutes to form double atomic steps on the Ge surface prior to the MBE growth. A migration-enhanced epitaxy (MEE) of GaAs for ~10 monolayers was then performed at a temperature of 200 °C. The double atomic steps coupled with the MEE process significantly suppress the formation of anti-phase domains at the III-V/Ge interface and the propagation of anti-phase boundary defects in the subsequent III-V layers grown on the Ge surface. Furthermore, the low growth temperature prevents interdiffusion between Ge and the III-V layers. A 500 nm undoped GaAs buffer was then grown, followed by a 1 μm undoped graded $In_yAl_{1-y}As$ metamorphic buffer with y varying from 0 to 0.52 from the bottom to the top. The transistor channel layer, comprised of a 15-nm-thick Be-doped (10^{16} cm^{-3}) $In_{0.7}Ga_{0.3}As$ grown on 35-nm-thick Be-doped (10^{17} cm^{-3}) $In_{0.53}Ga_{0.47}As$, was grown on the relaxed $In_yAl_{1-y}As$ surface [128]. The growth temperatures for the GaAs, $In_yAl_{1-y}As$, and InGaAs layers were 580, 420, and 450 °C, respectively.

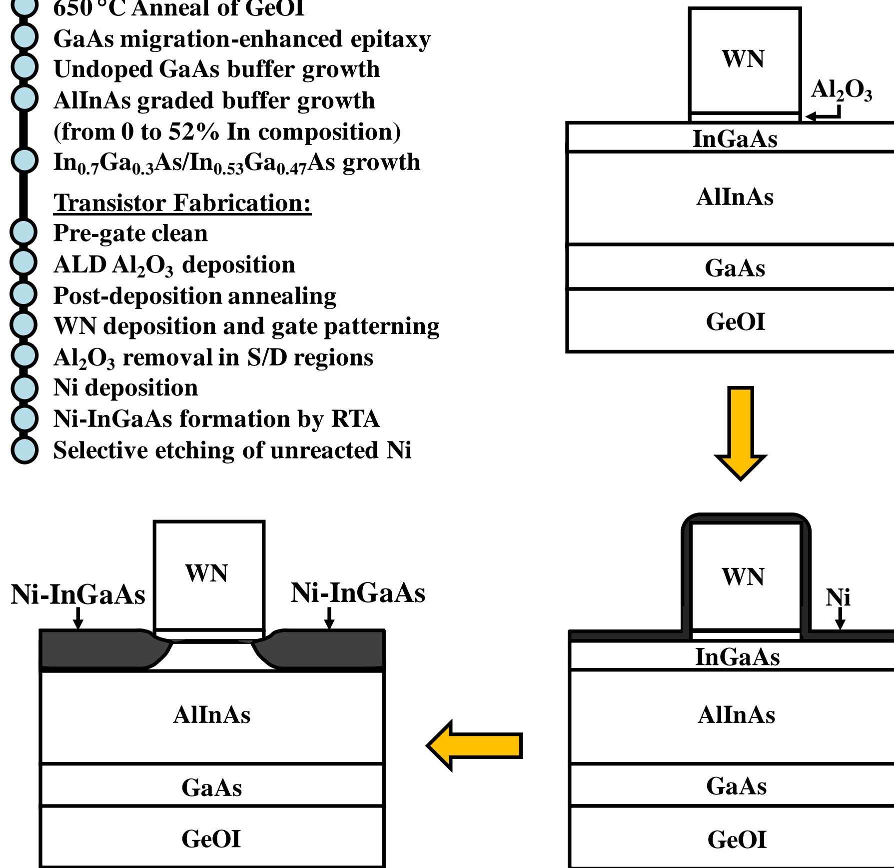

Fig. 4.7. Process flow used in this experiment, including the growth of InGaAs-on-GeOI and the fabrication of n-channel InGaAs metal oxide semiconductor field-effect transistor (MOSFET). Schematics on the right illustrate the self-aligned metallic S/D formation scheme employed in the fabrication of transistor on the MBE grown substrate.

The MOSFETs fabrication process flow is similar to the one employed in previous Section. Sample wafer was first dipped in HCl and NH_4OH solutions for surface native oxide removal. This was followed by surface passivation using $(NH_4)_2S$ solution. ~8 nm Al_2O_3 was then deposited using atomic layer deposition (ALD), and annealed at 400 °C for 60 s. The gate stack was eventually completed with sputter-deposited WN, followed by gate patterning with optical lithography and a fluorine-based metal etch. ~30 nm of Ni was then sputtered onto the sample

and rapid thermal annealed at 250 °C for 60 s to form the Ni-InGaAs S/D contacts. The device fabrication process was finally completed by selective removal of the unreacted Ni using nitric acid (HNO_3:H_2O = 1:10) at room temperature. The key steps of the process flow are illustrated in Fig. 4.7.

A cross-sectional TEM image of the MBE-grown layer structure with an InGaAs-channel transistor fabricated on it is shown in Fig. 4.8 (left). The root-mean-square (RMS) surface roughness of the $In_{0.7}Ga_{0.3}As$ layer is ~2.36 nm. Figure 4.8 (right) shows a high-magnification image of the fabricated $In_{0.7}Ga_{0.3}As$ channel n-MOSFET. The as-deposited Ni reacted with InGaAs layer forming a ~54-nm-thick Ni-InGaAs metallic S/D, well aligned to the WN/Al_2O_3 gate stack.

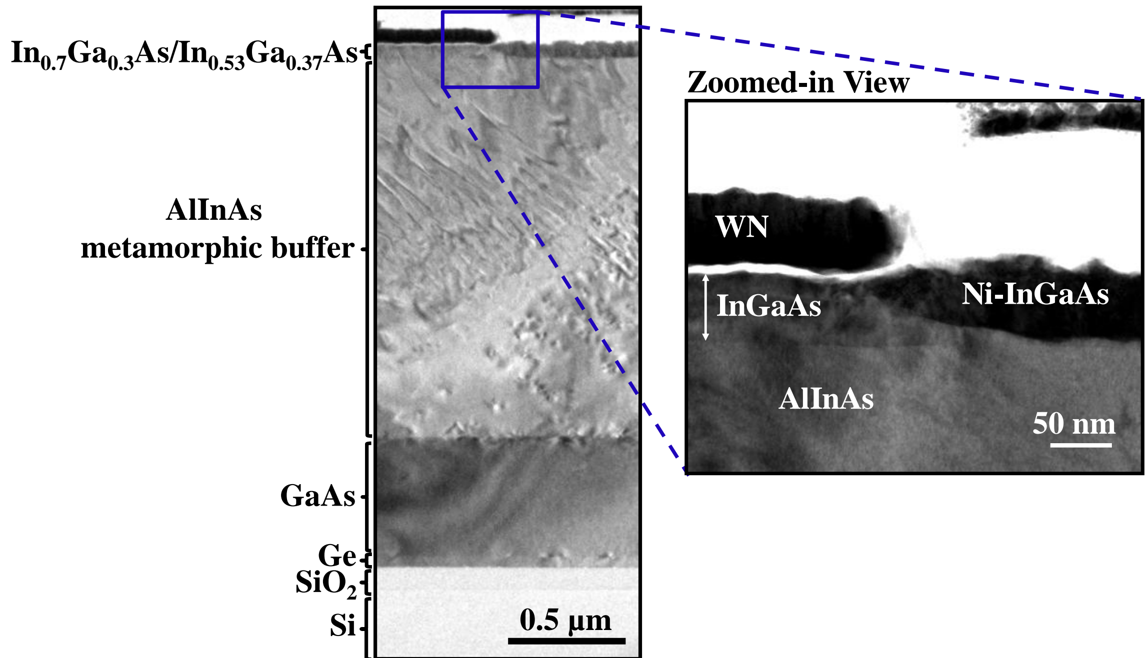

Fig. 4.8. Cross-sectional TEM image of InGaAs-on-GeOI structure with $In_{0.7}Ga_{0.3}As$ channel n-MOSFET fabricated on it (left). High-resolution TEM image of the $In_{0.7}Ga_{0.3}As$ n-MOSFET with self-aligned Ni-InGaAs metallic S/D (right).

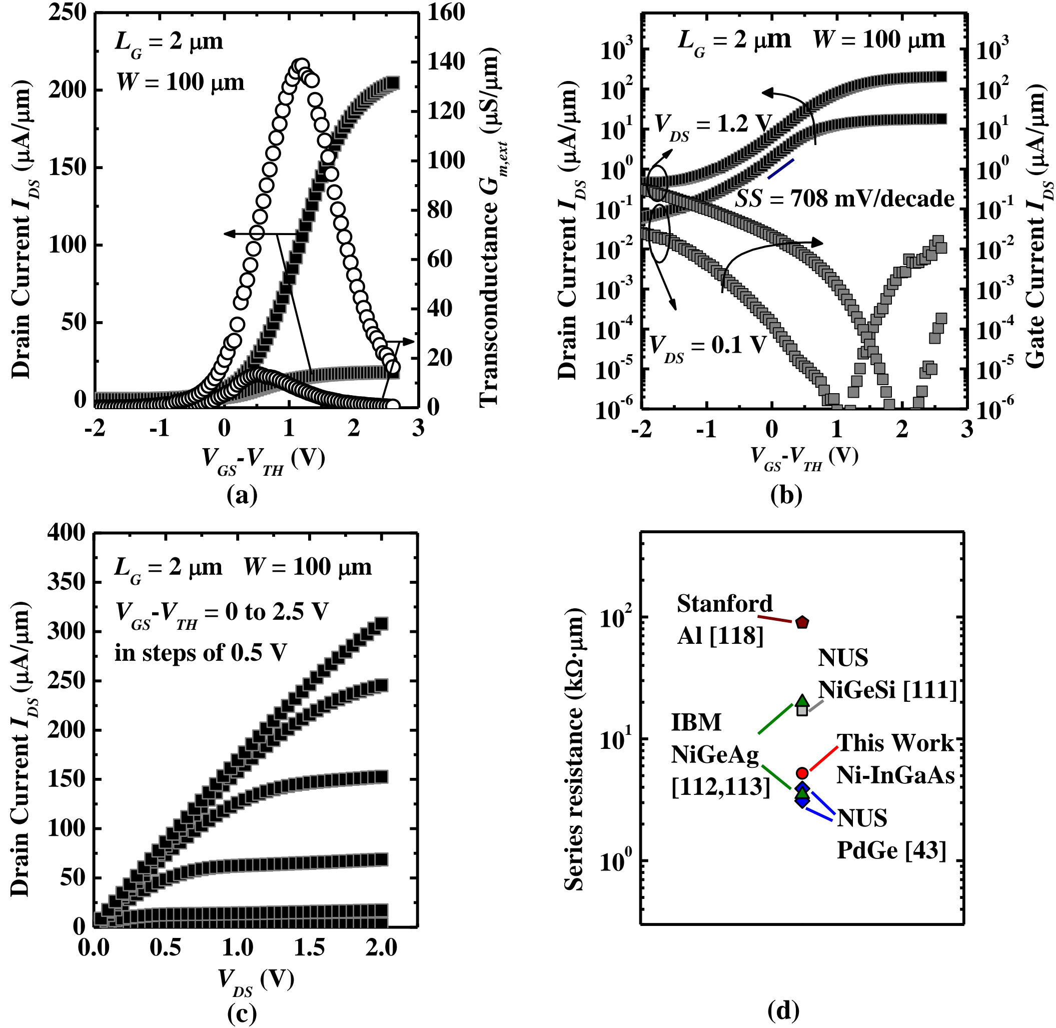

Fig. 4.9. (a) I_{DS} versus gate overdrive (V_{GS}-V_{TH}) of an n-MOSFET with $In_{0.7}Ga_{0.3}As$ channel and Ni-InGaAs metallic S/D at V_{DS} = 0.1 and 1.2 V. The gate length of the device is 2 μm and the gate width is 100 μm. Transconductance $G_{m,ext}$ characteristic is referred to the right axis. The peak $G_{m,ext}$ at V_{DS} = 1.2 V is 138.5 μS/μm. (b) Log (I_{DS}) and (I_G) versus V_{GS}-V_{TH} of the same device at V_{DS} = 0.1 and 1.2 V (c) I_{DS}-V_{DS} plot of the same device at various gate overdrives (V_{GS}-V_{TH}) from 0 to 2.5 V. (d) Series resistance of InGaAs n-MOSFET with Ni-InGaAs source/drain is compared with other reported series resistance of InGaAs n-MOSFETs

Fig. 4.9 shows the electrical characterization of the InGaAs surface channel n-MOSFET fabricated on GeOI on Si substrate. The I_{DS}-V_{GS} transfer characteristics of a transistor with a gate length of 2 μm and gate width of 100 μm were obtained at applied drain voltages V_{DS} of 0.1 and 1.2 V [Fig. 4.9(a)]. The device exhibits an

on-state current of 203 μA/μm at a gate overdrive V_{GS}-V_{TH} of 2.5 V. This value is comparable to those obtained from similar device structures made on InGaAs grown on InP substrate [78],[129]-[111].

The transconductance $G_{m,ext}$ is also plotted as a function of V_{GS}-V_{TH}. A peak $G_{m,ext}$ value of 139 μS/μm at V_{DS} = 1.2 V was obtained. The parasitic S/D resistance $R_{S/D}$ of this device is ~5.6 kΩ.μm as extracted at high V_{GS} using $R_{S/D} = V_{DS}/I_{DS}$ at V_{DS} = 0.1 V. The $R_{S/D}$ of this device is comparable with that of other reported InGaAs transistors [Fig. 4.9(d)]. The intrinsic transconductance $G_{m,int}$ of the device is ~227 μS/μm, after correcting for $R_{S/D}$. The I_{on}/I_{off} ratio of the device is around 2 orders of magnitude as shown in Fig. 4.9(b). This I_{on}/I_{off} is limited by leakage current flowing from the drain to the gate of the device, and could be due to incomplete removal of unreacted Ni. The source-to-drain leakage of this device could be lower than this value. Figure 4.9(c) shows the I_{DS}-V_{DS} characteristics of the device at gate overdrives from 0 to 2.5 V in steps of 0.5 V.

Figure 4.10 benchmarks the normalized peak transconductance G_m of devices in this work with the state-of-the-art $In_xGa_{1-x}As$ transistors reported in the literature [10],[17],[43],[110]-[117]. The peak G_m was normalized with the equivalent oxide thickness (t_{ox}) to account for the difference in high-k dielectric thickness in the various reports. The data fits (black solid symbols) very well with other reported values on the inverse proportional trend of G_m versus L_G. The transistors perform as well as other reported $In_xGa_{1-x}As$ channel n-MOSFETs. This implies that the MBE-grown InGaAs layer on top of the graded-buffer layer is of good quality. In comparison with InGaAs n-MOSFETs made on InGaAs-on-Si

substrate (open circles) [110], this $G_{m,int}$ values are significantly higher. This is the first demonstration of InGaAs surface channel n-MOSFET made on InGaAs-on-GeOI on silicon substrate. Further reduction of the graded buffer layer could enable integration of III-V n-MOSFETs and Ge p-MOSFETs on a common platform.

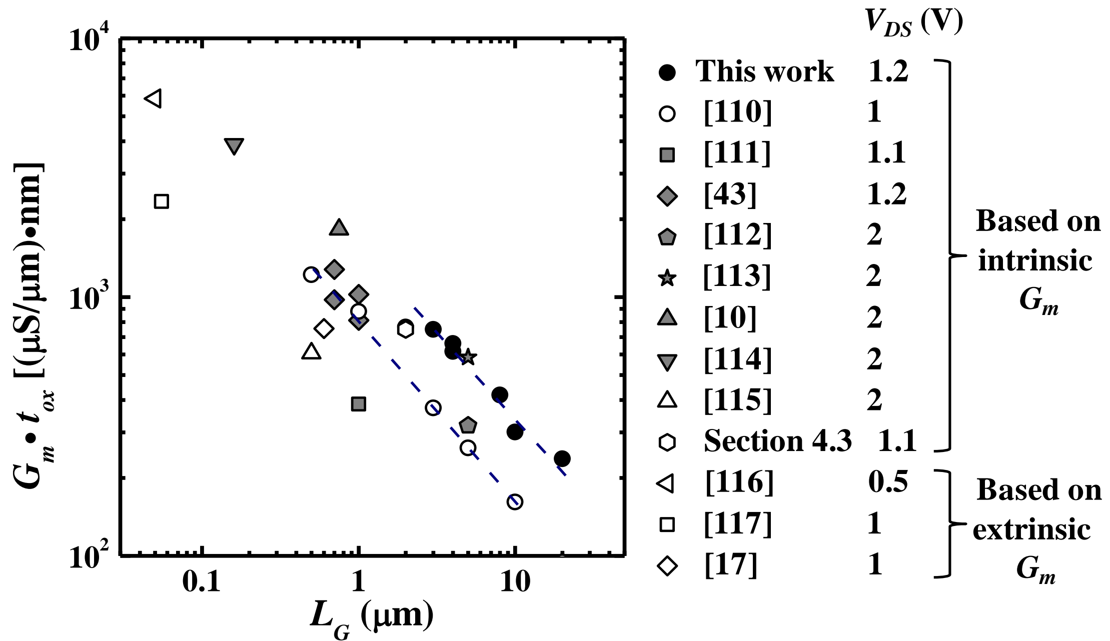

Fig. 4.10. Normalized peak transconductance $G_m.t_{ox}$ is plotted as a function of gate length (L_G). Device performance obtained in this work (black solid symbols) is compared with those reported in other $In_xGa_{1-x}As$ channel n-MOSFETs in the literature (gray solid symbols for $x = 0.7$, open symbols for $x = 0.53$). Note that data from Ref. [17],[116]-[117] are extrinsic G_m, while those from the other references are intrinsic G_m. The G_m data are from various V_{DS}: $V_{DS} = 0.5$ V for Ref. [116], $V_{DS} = 1$ V for Refs. [17],[110],[117], $V_{DS} = 1.1$ V for Ref. [111], $V_{DS} = 1.2$ V for Ref. [43] and this work, and $V_{DS} = 2$ V for Refs. [10],[112]-[115]. $G_m.t_{ox}$ obtained in this work is significantly higher than those of $In_{0.53}Ga_{0.47}As$ MOSFETs fabricated on Si (open circles) [110]. The connecting dashed lines act only as a guide.

4.5 Pt Incorporation in Ni-InGaAs Metallization

The impact of adding Pt in Ni silicide and germanide has been well reported [119]-[123]. However, little is known about Pt incorporation in Ni-InGaAs film. This study investigated the sheet resistance, film morphology, and contact resistivity of NiPt-InGaAs. Co-sputtering of Ni and Pt was employed for the NiPt-InGaAs formation.

The starting 2 inch substrates comprise a 500-nm-thick p-type $In_{0.53}Ga_{0.47}As$ (with a doping concentration of $\sim 2\times10^{16}$ cm^{-3}) grown on p-type (001) InP (with a doping concentration of $\sim 1\times10^{19}$ cm^{-3}) by MBE. Following the native oxide removal in dilute hydrofluoric acid ($HF:H_2O$ = 1:100) solution, Ni and Pt were co-sputtered onto the substrates. The sputtering DC power for Ni and Pt was adjusted so that a targeted Pt concentration in NiPt film was obtained. The DC power for Ni and Pt is 400 and 20 W, respectively. The Ar gas flow was set at 25 sccm and the chamber pressure was kept at ~4 mTorr during the deposition. Samples with NiPt thicknesses t_{NiPt} of ~27 nm were prepared. Fig. 4.11 shows XPS depth profiling of the co-sputtered NiPt film where ~15 at% Pt was detected.

The NiPt-on-InGaAs sample was cut into smaller pieces. The pieces were annealed in a nitrogen ambient in a Rapid Thermal Processing (RTP) tool at various temperatures ranging from 200 to 500 °C. For comparison, Ni-InGaAs films formed at same temperature range using the same substrate and Ni thickness were also prepared.

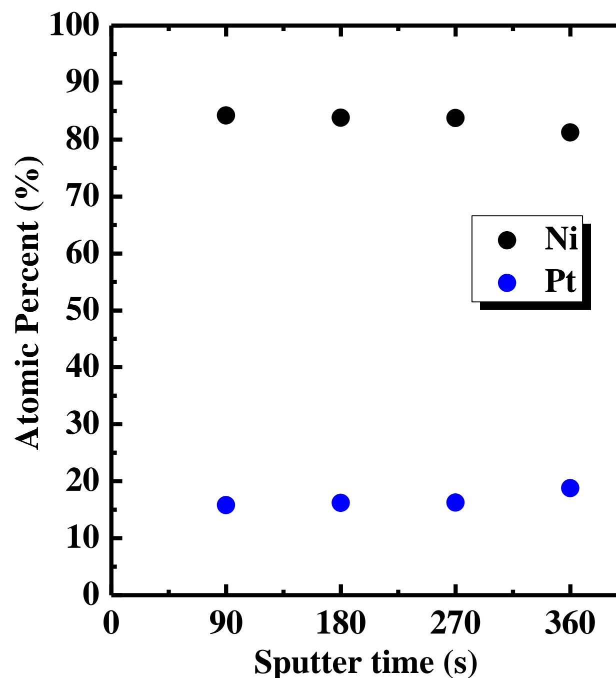

Fig. 4.11. XPS depth profiling across co-sputtered NiPt film. Pt concentration is ~15 at%, uniformly distributed in the film. The XPS characterization was done in IMRE through service contract.

Fig. 4.12(a) shows the sheet resistance R_{sh} of NiPt-InGaAs and Ni-InGaAs films formed at various temperatures. NiPt-InGaAs formed between 250 and 350 °C temperature range has ~15% higher R_{sh} value. A higher R_{sh} value for NiPt-InGaAs could be attributed to higher bulk resistivity of the film. At formation temperature above 400 °C, NiPt-InGaAs film formed has significantly lower R_{sh} value. While NiPt-InGaAs exhibited low R_{sh} value at 500 °C, the R_{sh} of Ni-InGaAs formed at this temperature cannot be measured by the micro four-point probe.

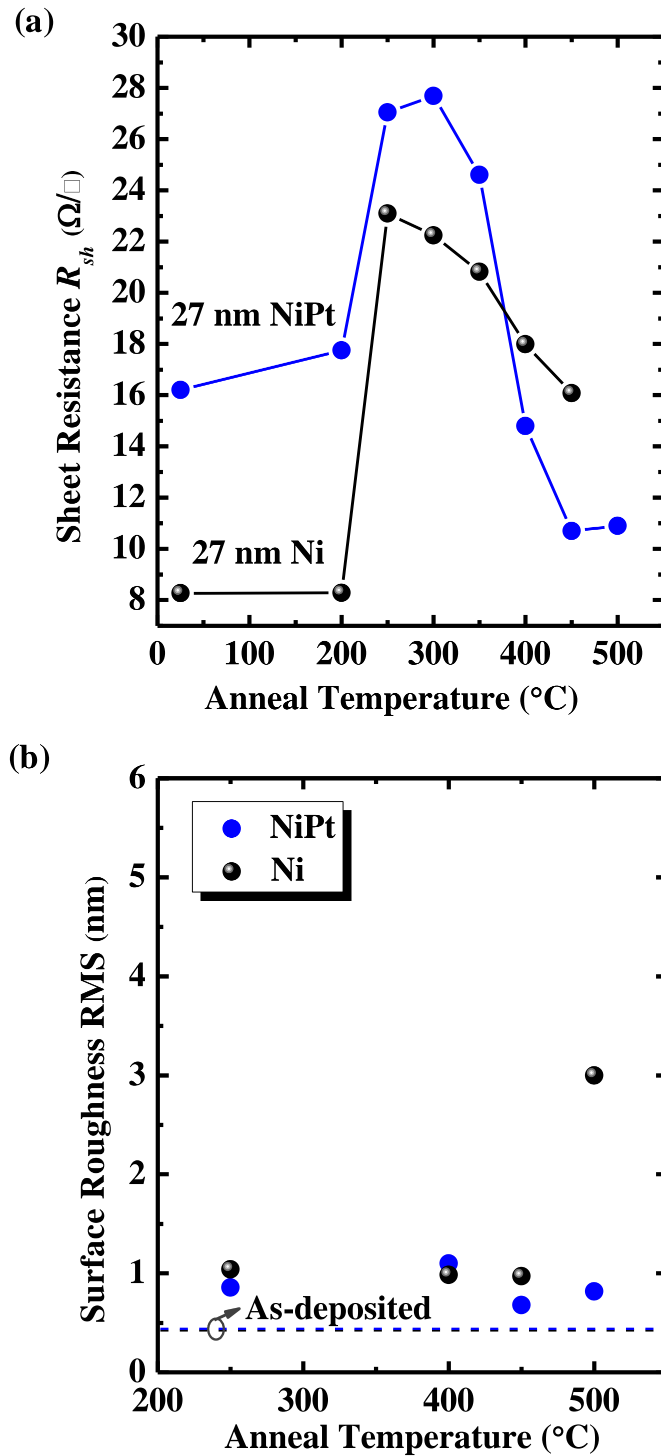

Fig. 4.12. **(a)** Sheet resistances R_{sh} of NiPt (blue symbols) and Ni (black symbols) on p-type InGaAs samples annealed at various temperatures for a fixed time of 60 s. (b) Surface roughness of the annealed NiPt and Ni on InGaAs. The as-deposited NiPt and Ni films have similar RMS surface roughness of ~0.4 nm as represented by dotted lines.

The surface morphology of the annealed NiPt and Ni on InGaAs was characterized with atomic force microscope (AFM) scan. No significant difference in the surface roughness between NiPt-InGaAs and Ni-InGaAs was observed up to 450 °C, as shown in Fig. 4.12(b). The formed films have reasonably low surface roughness value of ~0.8 – 1.1 nm. While the low surface roughness of NiPt-InGaAs is maintained at 500 °C, Ni-InGaAs has degraded surface roughness and surface morphology at this temperature. Fig. 4.13 compares the surface morphology of as-deposited, 250 °C, and 500 °C formed films. ~15 – 20 deep holes were observed on 500 °C formed Ni-InGaAs rough surface. This could be due to As or In desorption from the surface during the high temperature annealing. On the other hand, NiPt-InGaAs shows a very smooth and uniform surface morphology. This indicates the incorporation of Pt into Ni-InGaAs film improves the thermal stability of this film.

Fig 4.14 shows the cross-section TEM images of NiPt-InGaAs formed at 250, 400, and 500 °C. Although the surface roughness of 500 °C formed NiPt-InGaAs is very good, it has a relatively non-uniform NiPt-InGaAs/InGaAs interface as compared with lower temperature formed films. It also forms a much thicker film which contributes to the low R_{sh} value in Fig. 4.12(a).

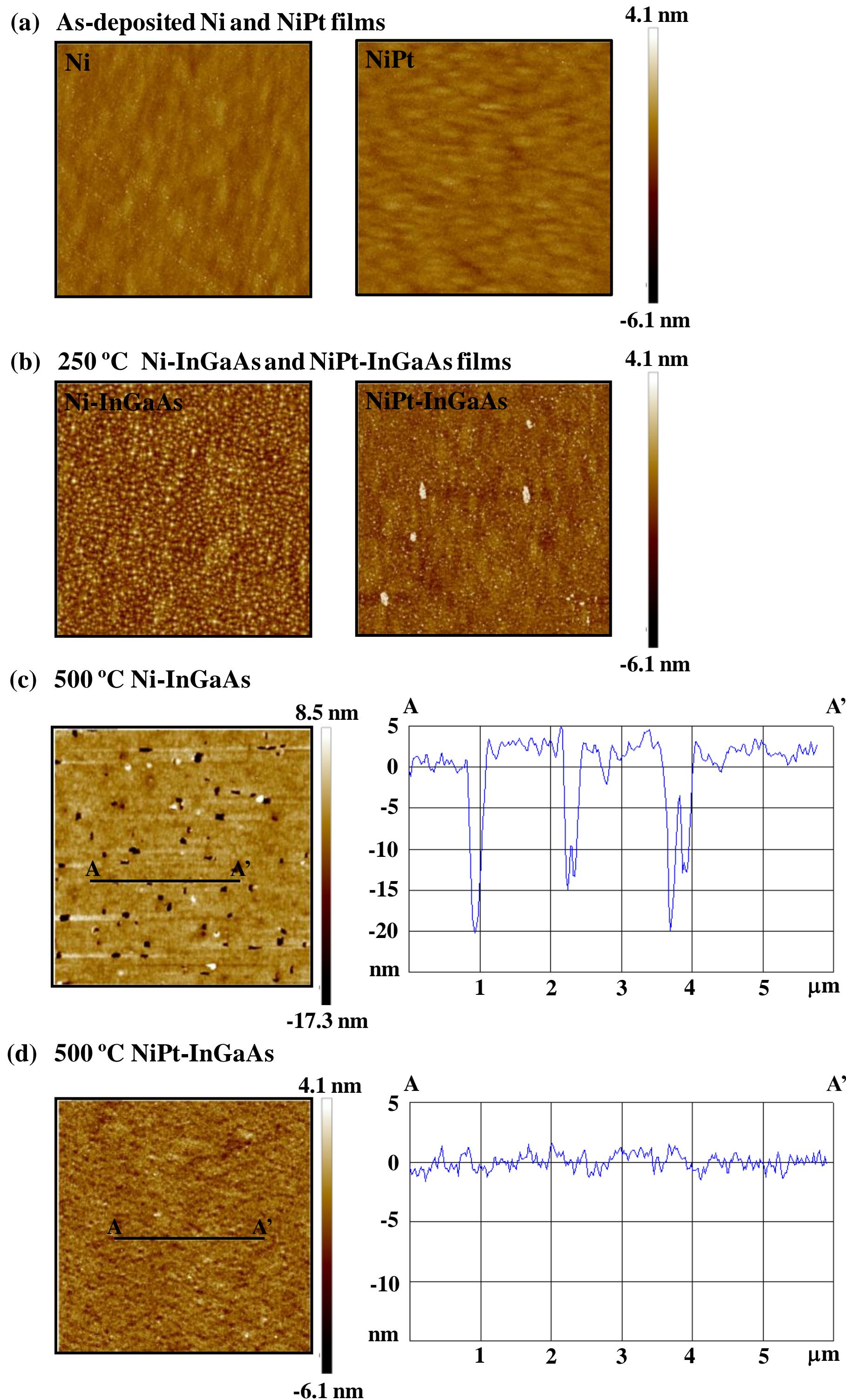

Fig. 4.13. Surface morphology of (a) as-deposited Ni and NiPt films, (b) 250 °C annealed Ni and NiPt films, (c) 500 °C formed NiPt-InGaAs and (d) Ni-InGaAs films in a 10 μm × 10 μm area obtained by AFM scan. The cross-section surface topology profile along section line A-A' is shown for 500 °C formed films.

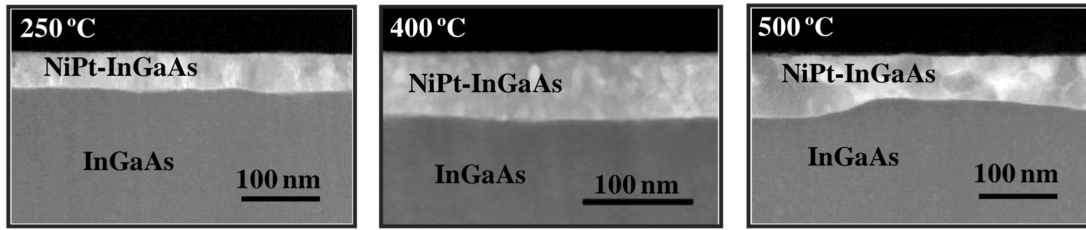

Fig. 4.14. Cross-sectional TEM of NiPt on InGaAs annealed at 250, 400, and 500 ºC.

The contact resistivity of NiPt-InGaAs on n-type InGaAs was also extracted from TLM test structure and compared with Ni-InGaAs as shown in Fig. 4.15. NiPt-InGaAs shows similar contact resistivity value at low formation temperature. The contact resistivity value is maintained over a wider formation temperature as indicated by the relatively stable value up to 500 ºC.

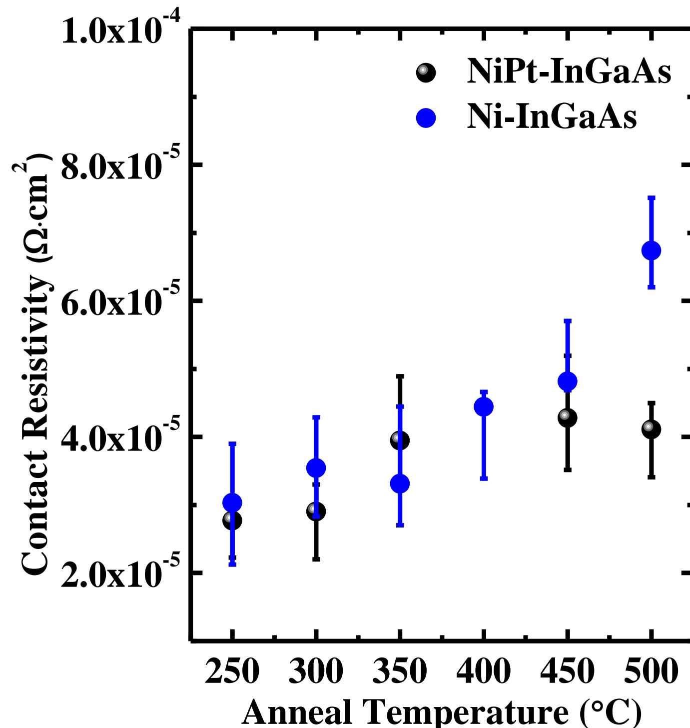

Fig. 4.15. Contact resistivity ρ_c versus anneal temperature for NiPt-InGaAs and Ni-InGaAs on n-type InGaAs. Same doping concentration of ~2×10^{19} cm^{-3} was used for a fair comparison.

4.6 Summary

InGaAs n-MOSFETs with self-aligned Ni-InGaAs metallization are well demonstrated. $In_{0.7}Ga_{0.3}As$ channel MOSFETs on GeOI on silicon substrate employing self-aligned Ni-InGaAs S/D scheme is also realized. The device exhibits excellent device performance with an on-state current as high as 203 μA/μm and an intrinsic transconductance at ~227 μS/μm at drain voltage of 1.2 V. These performance parameters are comparable to InGaAs devices made on the lattice-matched InP substrate. The normalized transconductance ($G_m.t_{ox}$) compares very well with those of other $In_xGa_{1-x}As$ channel n-MOSFETs reported in the literature. It is significantly higher than those of $In_{0.53}Ga_{0.47}As$ MOSFETs formed on InGaAs directly grown on Si substrate. The results of this study indicate that InGaAs-on-GeOI integration is promising, paving the way for co-integration of InGaAs n-MOSFET and Ge-based p-MOSFET on a common platform. In addition, the thermal stability and specific contact resistivity of Ni-InGaAs film is improved with Pt incorporation in the film. This suggests that Ni(Pt) can be a suitable metal for self-aligned S/D metallization not only for Ge and Si, but also for InGaAs.

Chapter 5

Process Development for InGaAs-based Transistor and Laser Integration on GeOI on Si Substrates

5.1 Introduction

High mobility channel materials for transistors are being pursued in order to keep up with increasing chip performance requirement based on Moore's law [1]-[2],[129]. While high mobility channel materials such as III-V and Ge are promising to keep up with the requirement for sub-11 nm technology [10],[114],[130]-[135], conventional copper line interconnect will eventually become insufficient to sustain the increasing bandwidth requirement for data transmission within an integrated circuit chip. This is due to several limitations attributed to the conventional metal interconnect such as resistive loss, frequency dependent loss, dielectric loss, power consumption, etc [136]-[138]. The limitations of on-chip metal interconnect make it unsuitable for signal transmission at data rate above 10 Gb/s especially for long distances such as above 10 mm [138]-[139].

Various approaches to overcome the metal interconnect limitations have been pursued [140]-[143]. One of the promising approaches is to use optical interconnect as replacement for metal interconnect [144]-[145]. The advantage of using photons to replace electrons as signal carrier is that the photon does not have resistance *R* and capacitance *C* and therefore it will not suffer from a *RC* delay. Thus, higher data rate for signal transmission can be obtained.

For optical interconnect to replace the conventional metal interconnect, photonic devices such as laser for converting electrical to optical signal, optical waveguide for transmitting the optical signal, and photodetector for converting optical signal back to electronic signal, are required. An illustration of electronic and photonic device integrated system is shown in Fig. 5.1.

With recent progress made in the integration of these optical devices on Si, inter-chip electronic and photonic device co-integration seems achievable [142]. However, it will be even more meaningful and important, from manufacturing cost effectiveness viewpoint, if an intra-chip level co-integration, i.e. co-integrating electronic and photonic devices on a common substrate, can be realized. In addition, the good progress made in the high mobility InGaAs channel transistors and the well-established III-V photonic devices can be an advantage for achieving high mobility electronic devices co-integrated with photonic devices on same substrate. To realize such co-integration, epilayers consisting of transistor and laser layers with good material quality grown on Si substrate are required. A well-designed device layout structure and fabrication process flow are important. Also, good assessment on device output performance is also required.

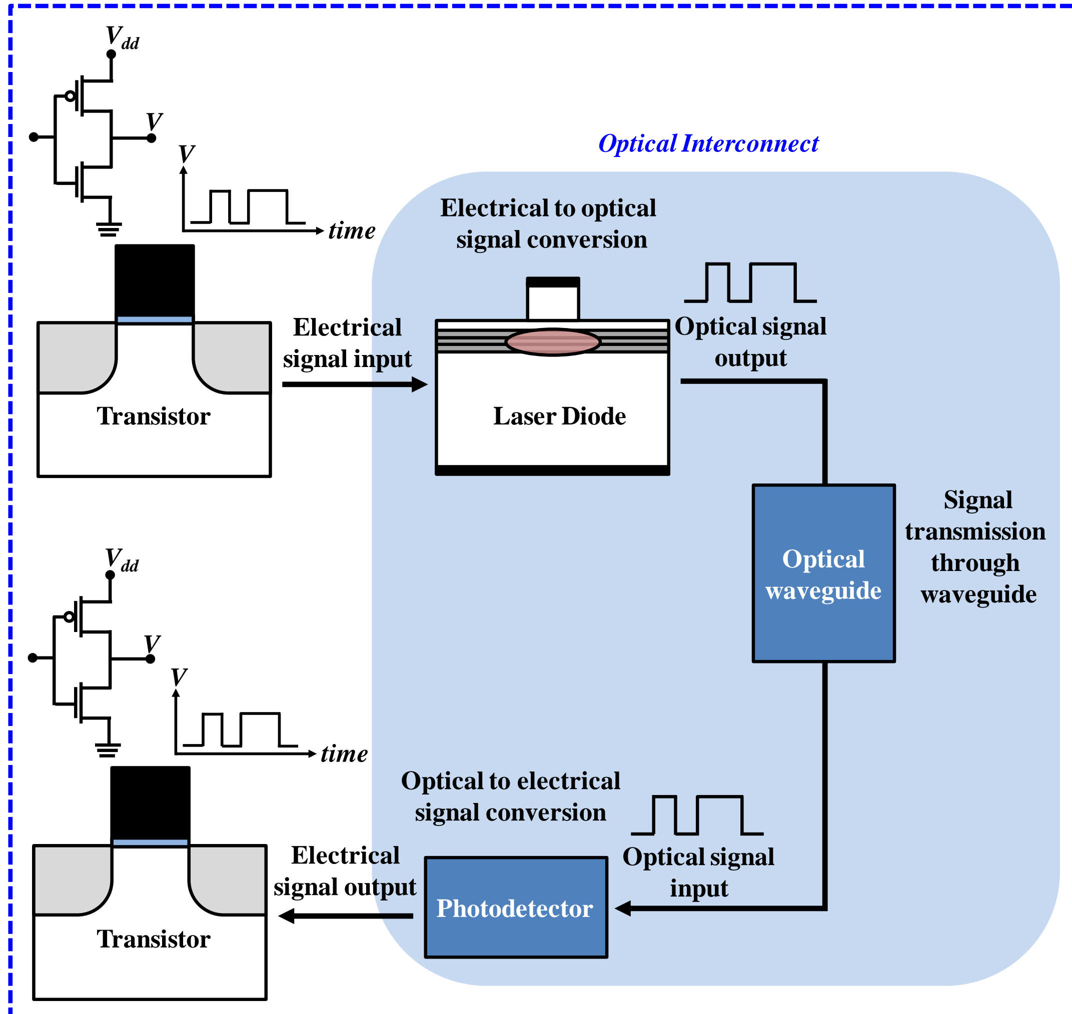

Fig. 5.1. An illustration of electronic and photonic device integrated system. The optical interconnect constitutes photonic devices such as laser diode, optical waveguide, and photodetector. Electrical output from transistor (e.g. of an inverter) is sent through a laser diode where the electrical signal is converted to optical signal. The optical signal is transmitted through a waveguide and received by a photodetector to convert the optical signal back to electrical signal that is received by transistor of another inverter at the other end.

This Chapter focuses on the co-integration of InGaAs-based transistors and lasers on common substrate. Some key achievements towards realizing InGaAs-based transistor and laser integration on a common platform are presented. The various challenges and efforts are also discussed. These include designing the layer

structure of the substrate for transistor-laser integration, establishing the device layout structure, fabricating InGaAs n-MOSFETs on the grown substrate, characterizing the electrical output of the fabricated transistors, and investigating the impact of material growth defect on transistors' electrical output characteristics. This is a collaboration work with Professor S.-F. Yoon's group at Nanyang Technological University (NTU). Our collaborator contributed to the growth of materials by molecular beam epitaxy (MBE) growth and is currently developing laser fabrication process which will be briefly presented in this Chapter. The results of this Chapter are a crucial milestone for enabling the realization of InGaAs-based transistor and laser device co-integration at the intra-chip level. The results of this Chapter also provide an important understanding on the effect of material growth defects in InGaAs layer on the transistor performance.

5.2 Design Concept

5.2.1 Layer Structure of Substrate for Transistor-Laser Integration

The layer structure of the substrate for transistor-laser integration was carefully designed for this experiment. Germanium-on-insulator (GeOI) on silicon substrate with a 10° offcut towards <111> was used as the starting substrate for the MBE growth. The layer sequence of the substrate for transistor-laser integration was prudently planned by considering lattice constant between two adjacent layers to minimize large lattice mismatch. Laser layers comprising $Al_{0.3}Ga_{0.7}As$ cladding layers and $In_{0.2}Ga_{0.8}As$/GaAs quantum-well (QW) layers

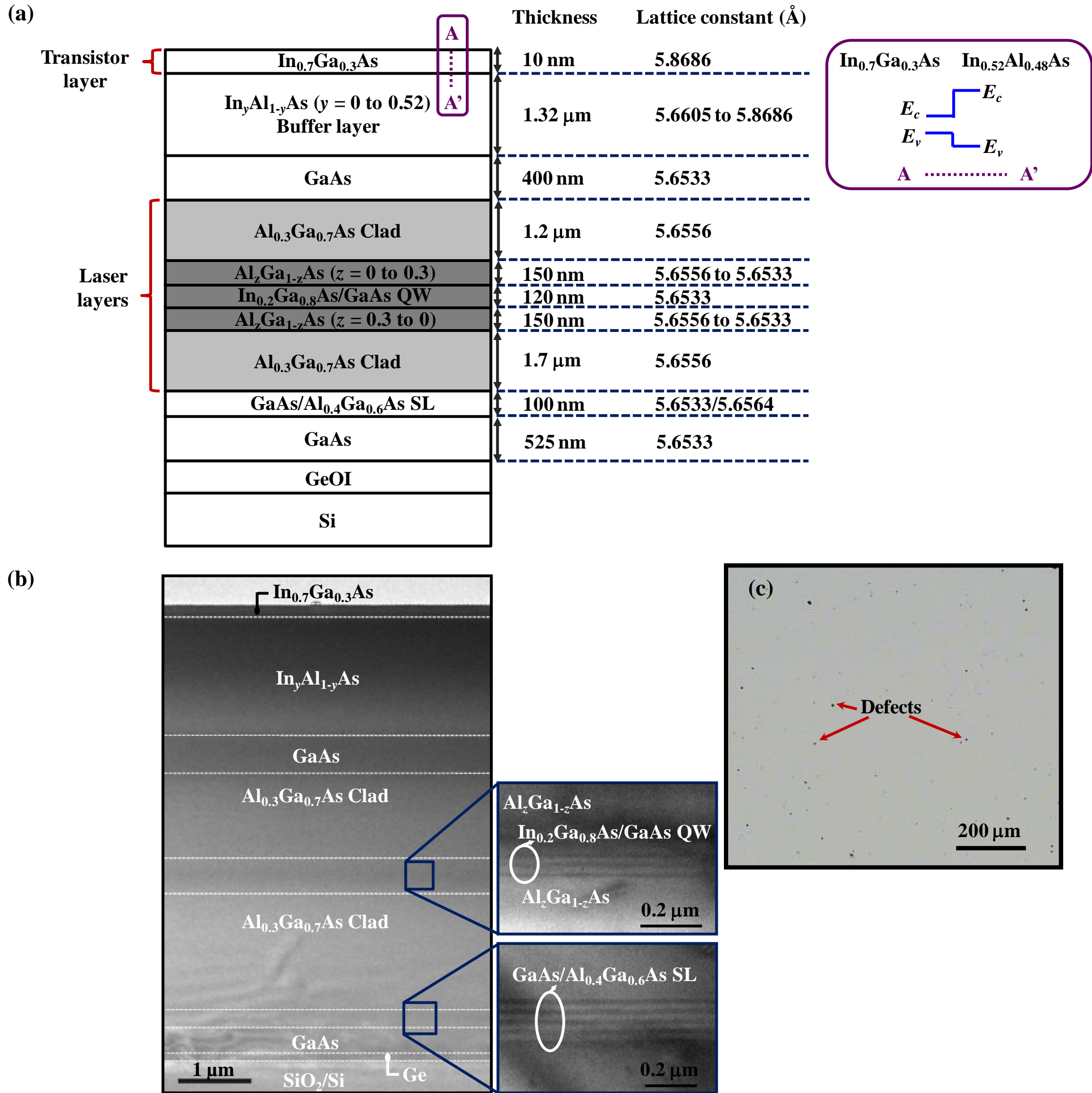

Fig. 5.2. (a) Structure of epilayers grown on GeOI substrate for transistor-laser integration. (b) Transmission electron microscopy (TEM) image of the grown substrate. (c) Optical microscopy image showing the surface of the grown substrate where defects are observed.

were the first material system to grow. This was followed by transistor channel layer, which comprises $In_{0.7}Ga_{0.3}As$ layer.

A schematic showing the designed layer structure is depicted in Fig. 5.2(a). Si-doped (5×10^{18} cm^{-3}) GaAs was the first grown layer due to its lattice constant

being almost equal to that of Ge. This was followed by five-period Si-doped (5×10^{18} cm^{-3}) GaAs/AlGaAs superlattice (SL) layers to filter threading dislocations induced by stress/strain due to lattice mismatch between GaAs and the subsequent laser layers [36],[146]. Next, laser layers which have relatively small lattice mismatch with GaAs were grown. This include the growth of a Si-doped (5×10^{17} cm^{-3}) $Al_{0.3}Ga_{0.7}As$ bottom cladding layer, an n-type bottom graded-index separate confinement heterostructure (GRINSCH) $Al_zGa_{1-z}As$ (z = 0.3 to 0) layer, three-period $In_{0.2}Ga_{0.8}As$/GaAs QW layers, a p-type upper GRINSCH $Al_zGa_{1-z}As$ (z = 0 to 0.3) layer, and a Be-doped (5×10^{17} cm^{-3}) $Al_{0.3}Ga_{0.7}As$ top cladding layer.

Above the laser layers, Ge-doped (1×10^{19} cm^{-3}) GaAs layer and $In_yAl_{1-y}As$ metamorphic buffer layer (y varying from 0 to 0.52) were grown to obtain the lattice constant close to that of transistor layer (InGaAs). This GaAs layer would also act as an etch stop layer in the device fabrication process (to be discussed in the next sub-section). Finally, a transistor channel layer comprising a 10-nm-thick Be-doped (10^{16} cm^{-3}) $In_{0.7}Ga_{0.3}As$ was grown on the relaxed $In_yAl_{1-y}As$ surface. Using InAlAs as buffer layer helps to reduce the source-to-drain leakage current of InGaAs transistors due to the wide bandgap of InAlAs [as illustrated in Fig. 5.2(a)].

The transmission electron microscopy (TEM) image of the grown substrate for transistor-laser integration is shown in Fig. 5.2(b). Visible defects were observed under optical microscope [Fig. 5.2(c)]. The estimated defect density is ~10^9 cm^{-2}. The presence of defects in the grown substrate would impose some restrictions on the fabrication process steps. This will be further discussed in

Section 5.2.3. In addition, the impact of growth defect on transistor electrical performance is also studied in section 5.4.

5.2.2 *Device Layout Structure for Transistor and Laser Co-Integration*

For a laser diode to produce optical output light from electrical input current, a typical minimum threshold current (I_{th}) is required. The I_{th} of a laser diode depends on parameters related to the material system and the dimension of the laser active layer as expressed by

$$I_{th} = \frac{nqd_{las}L_{las}W_{las}}{\tau_{sp}}, \tag{5.1}$$

where n is the injected carrier concentration, q is the electronic charge, τ_{sp} the carrier life time related to spontaneous recombination, d_{las} is the thickness of the QW active layer, L_{las} is the length of the laser active layer, and W_{las} is the width of the laser active layer [147].

A typical threshold current density of $In_{0.2}Ga_{0.8}As/GaAs$ QW laser diode with $Al_{0.3}Ga_{0.7}As$ cladding is ~900 A/cm^2 [148]. Based on the width and the length of the laser active layer designed in this work, this corresponds to ~50 mA for the same material system. To obtain such high output current from transistor, transistor structure with small gate length (L_G) or large gate width (W) can be employed, as expressed by the following relationship:

$$I = \frac{\mu C_{ox}W(V_{GS} - V_{TH})^2}{2L_G}, \tag{5.2}$$

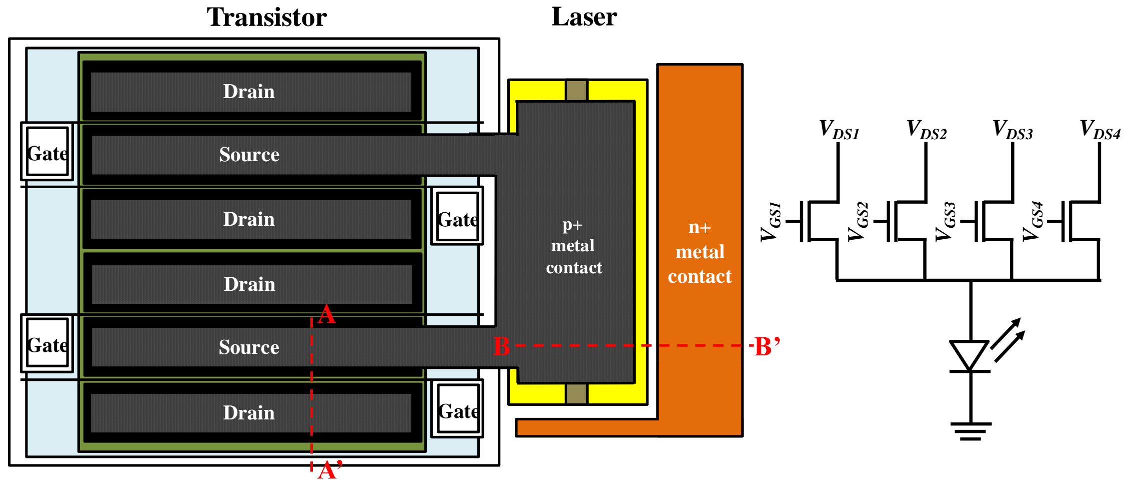

Fig. 5.3. (Left) schematic showing the top view of a transistor-laser integrated circuit layout. The author involved in the discussion on the mask layout design although the drawing of the actual mask layout was not done by the author. Line A-A' and B-B' are cross-section along which the schematics in Fig. 5.4 and 5.6 were drawn. The corresponding symbols (right) illustrate the connection of the four transistors to a laser.

where μ is the carrier mobility, C_{ox} is the oxide capacitance, V_{GS} and V_{TH} is the gate voltage and threshold voltage, respectively.

For this work, transistors with large gate width were implemented to achieve high absolute value for the output current. Fig. 5.3 (left) depicts device layout structure for the transistor-laser integration. Four transistors are connected to a laser device. The configuration of the designed circuit allows current flowing from one transistor up to four transistors to a laser diode as illustrated in Fig. 5.3 (right). The details of fabrication process flow to realize the transistor-laser integrated circuit will be presented next.

5.2.3 Device Fabrication Process Flow of the InGaAs-based n-MOSFETs and QW Lasers

The process flow was designed to begin with the fabrication of transistors followed by lasers. Presence of defects [Fig. 5.2(c)] in the substrate makes it unsuitable for a fabrication process that requires numerous wet etching steps. Wet etching process steps can cause severe etching through the defects of the epilayers [149]. Therefore, the transistor fabrication flow minimizes use of wet etching steps. For this reason, self-aligned source/drain (S/D) contact metallization that relies on chemical wet etch process for the removal of unreacted metal was not employed. Instead, non-self-aligned scheme with Si doped S/D and PdGe metal contacts were used.

Fig. 5.4 illustrates the transistor fabrication process flow designed and implemented in this work. The sample went through pre-gate clean in HCl and NH_4OH solutions for native oxide removal, and $(NH_4)_2S$ surface passivation for preventing surface oxidation. It was then quickly loaded into atomic layer deposition (ALD) chamber for ~6 nm of Al_2O_3 gate dielectric deposition. Post-deposition annealing at 400 °C for 60 s was performed followed by tantalum nitride (TaN) gate electrode sputter deposition [Fig. 5.4(a)-(b)]. The gate was patterned by optical lithography and etched in Cl_2-based plasma [Fig. 5.4(c)].

Si-doped S/D layer, InGaAs mesa, and PdGe non-self-aligned metal contacts were next formed [Fig. 5.4(d)-(f)]. The sample was patterned by optical lithography to expose the S/D regions for Si dopant implantation. The Si implant dose and energy were 1×10^{14} cm^{-2} and 10 keV, respectively. The implant was

carried out at 7° tilt to minimize dopant channeling. The sample was rotated during the implant process at 0°, 90°, 180°, 270° about axis normal to sample surface to obtain uniform doping. The expected Si implant range and straggle are ~12 and ~7 nm, respectively, as obtained by simulation of stopping and range of ions in matter (SRIM) [150]. Since InGaAs layer is only 10 nm thick, the implanted Si dopants would also reach the InAlAs layer underneath. ~30 nm of SiO_2 capping layer was

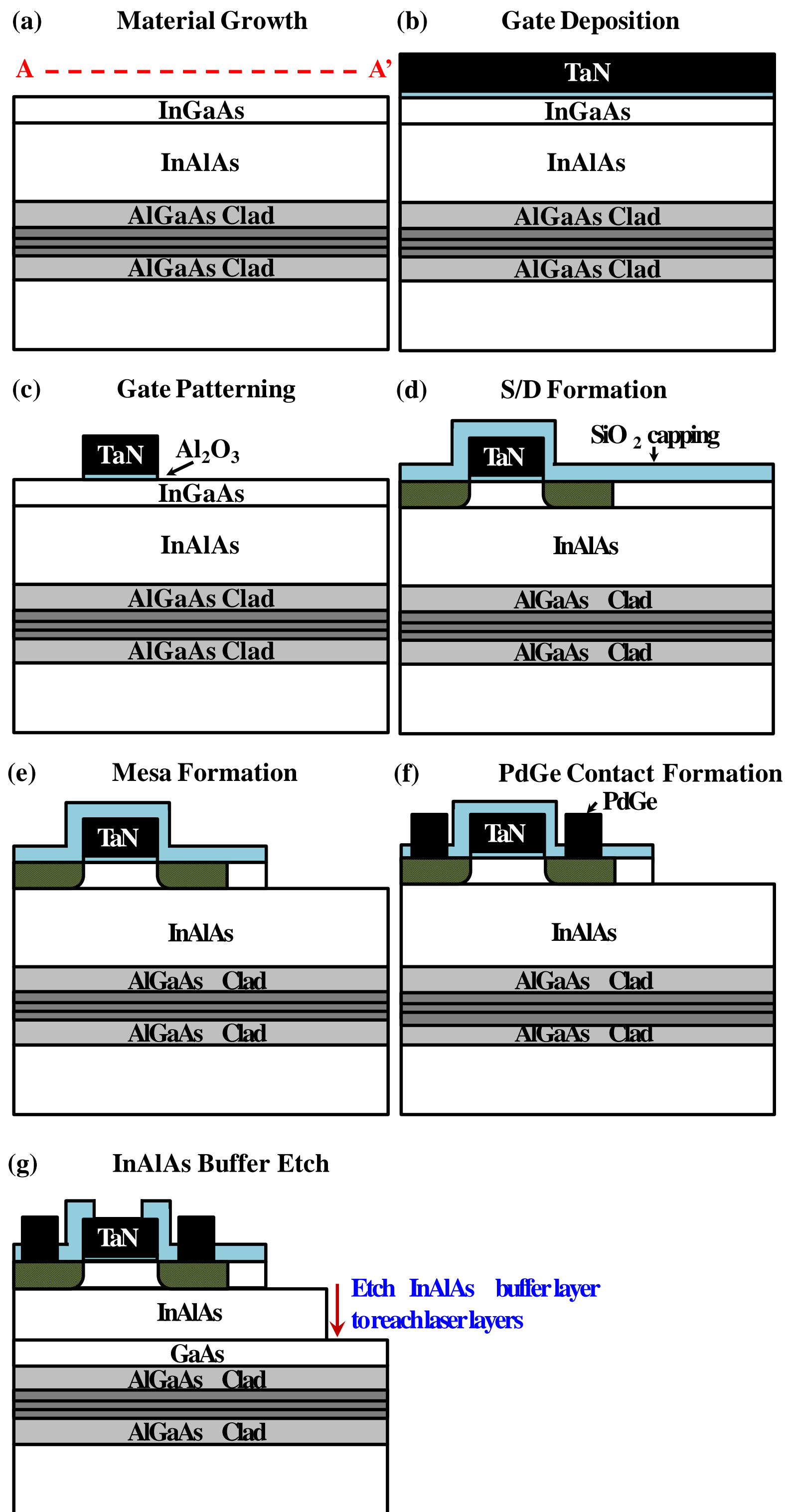

Fig. 5.4. Schematics showing transistor fabrication process flow. Schematics are drawn along line A-A' in Fig. 5.3.

deposited followed by an activation annealing at 600 °C for 60 s to complete the Si-doped S/D formation [Fig. 5.4(d)].

InGaAs mesa was formed by optical lithography patterning and Cl_2-based plasma etching [Fig. 5.4(e)]. This InGaAs mesa would provide isolation between transistors. The sample was next patterned for PdGe metal contact formation at the S/D regions. The SiO_2 was removed using dilute hydrofluoric (DHF) acid ($HF:H_2O$ = 1:100), which was then immediately followed by Pd (40 nm) and Ge (90 nm) e-beam evaporation and lift-off process to form Pd/Ge metal pads. Annealing at 400 °C for 10 s was next performed for the formation of PdGe metal contacts [Fig. 5.4(f)]. The annealing process allowed Ge to diffuse down to react with Pd and excess Ge would dope InGaAs at PdGe/InGaAs interface [47]-[49]. The transistor fabrication process was completed with a lithography step followed by DHF dip to remove the SiO_2 on the TaN gate pad for device characterization. Fig. 5.5 shows the scanning electron microscopy (SEM) images of a transistor after going through various key process steps. Fabricated transistors were characterized before continuing with laser fabrication steps. The results are discussed in Section 5.3.

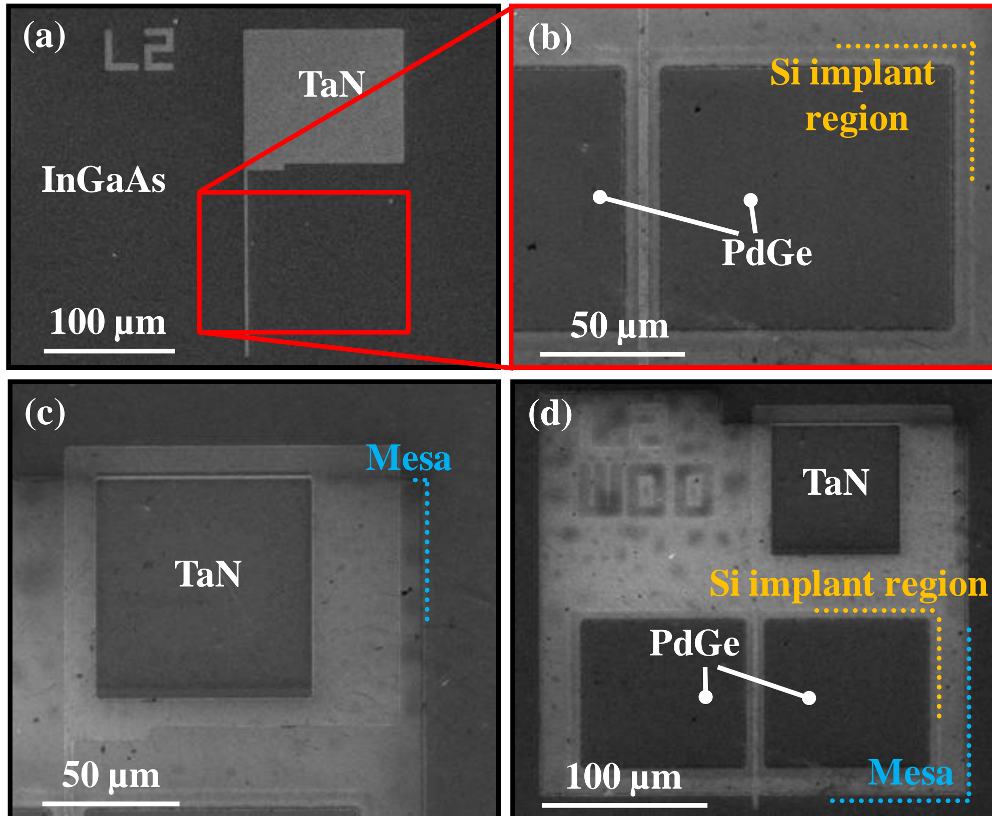

Fig. 5.5. Scanning electron microscopy (SEM) images showing a transistor after (a) gate formation, (b) Si implant and PdGe contact formation, (c) InGaAs mesa formation and SiO_2 removal on the gate pad. The completed transistor formation is shown in (d).

Another important step to be considered is the InAlAs buffer layer removal [Fig. 5.4(g)] to expose laser layers at region where lasers would be fabricated. HCl solution ($HCl:H_2O$ = 3 : 1) was used for the wet etching of InAlAs buffer layer due to its high etch selectivity of InAlAs over GaAs. Hence, GaAs would act as an etch stop layer.

The etching process was carefully monitored to ensure complete removal of the InAlAs buffer layer. Since HCl solution does not etch GaAs, the InAlAs etch depth would eventually saturate with longer etch time once InAlAs layer was completely removed. Fig. 5.6 shows InAlAs etch depth as a function of etch time

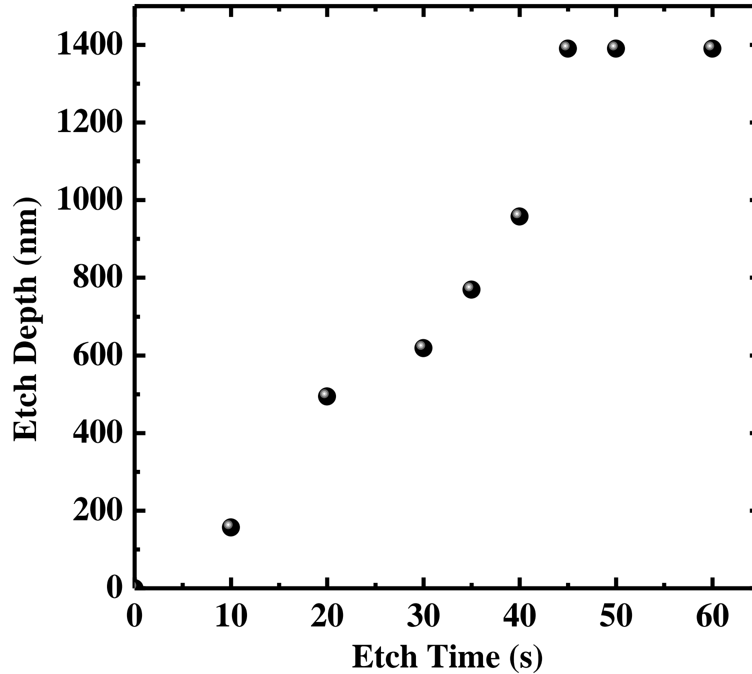

Fig. 5.6. Etch depth versus etch time of InAlAs buffer layer in $HCl:H_2O$ = 3:1 solution.

where the InAlAs etch depth was determined using step profiler after a duration of etch time. The etch depth increased with longer etch time and saturated after 45 s of etching, indicating complete removal of InAlAs buffer layer.

Before proceeding with laser fabrication steps, a thick 400 nm of SiO_2 was deposited on the sample using plasma enhanced chemical vapor deposition (PECVD) [Fig. 5.7(a)]. The thick SiO_2 would protect the fabricated transistors during the laser fabrication process. The SiO_2 in the laser region was then removed with buffered oxide etch (BOE) solution [Fig. 5.7(b)] which would be followed by laser waveguide (rib) formation by wet etching of GaAs and AlGaAs [Fig. 5.7(c)]. B-staged bisbenzocyclobutene (BCB) polymer would be used to fill in the gap next to the rib to get a flat surface with respect to the rib [Fig. 5.7(d)]. A flat surface

was needed to ensure continuous metal line connecting transistors to lasers, which would be formed last. The formation of mirror facet would then be performed by dry etching [Fig. 5.7(e)]. Lastly, Ni/Ge/Au/Ni/Au metal contact to n-type GaAs would be formed and Ti/Au metal line would be deposited to connect the source metal pad of InGaAs transistors to p-type GaAs of the lasers [Fig. 5.7(f)-(g)]. The complete transistors-laser integrated circuit obtained with the abovementioned process steps is illustrated in Fig. 5.3. Note that the laser fabrication process is still under development.

Laser Fabrication

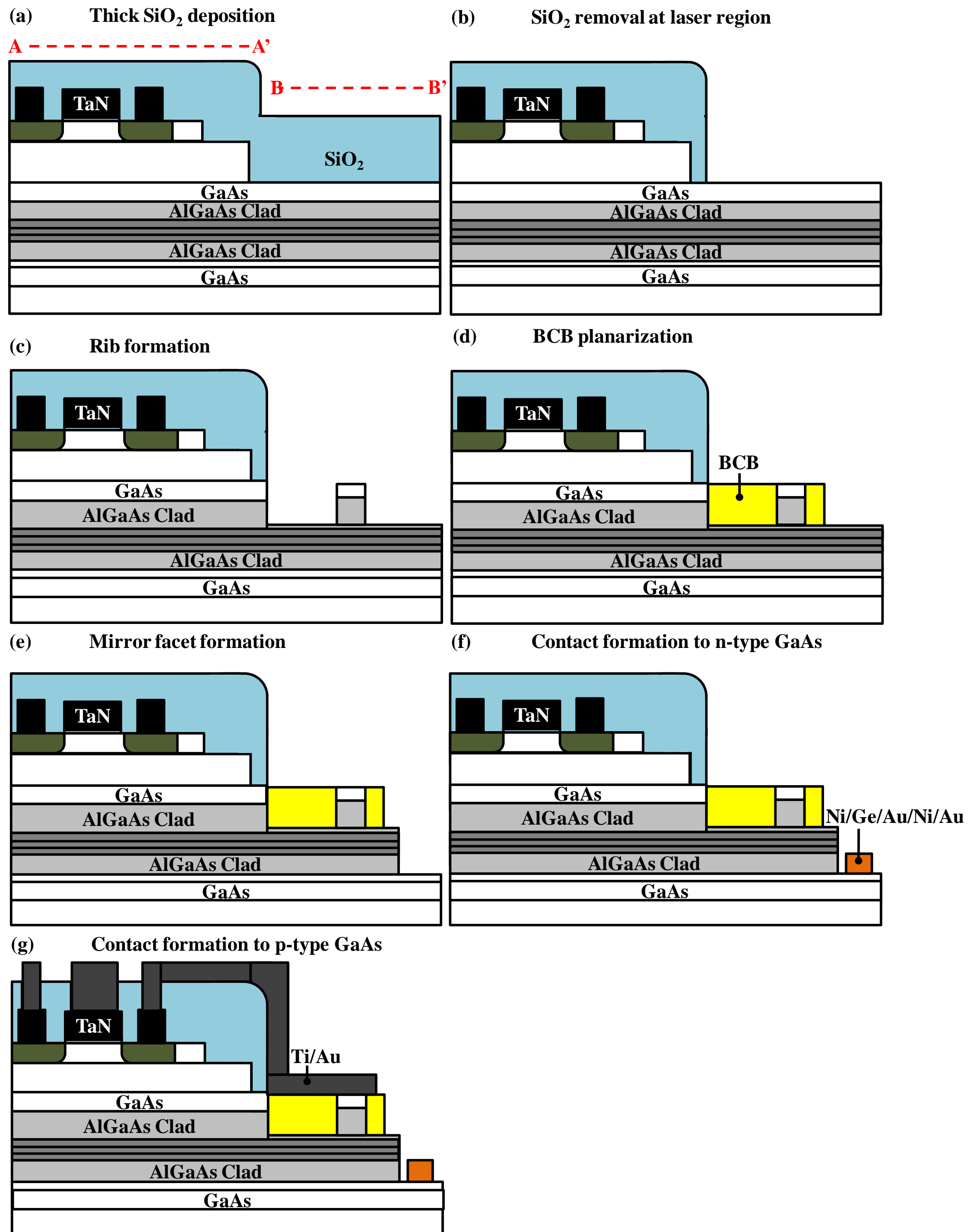

Fig. 5.7. Schematics showing laser fabrication process flow, following the completed transistor formation (line A-A') in Fig. 5.4. The process steps of laser fabrication are drawn along line B-B' in Fig. 5.3.

5.3 Electrical Performance of $In_{0.7}Ga_{0.3}As$ Transistors Fabricated on Grown Substrate for Transistor-Laser Integration

The drain current I_{DS} versus gate voltage V_{GS} of transistor with gate length of 2 μm at applied drain voltage V_{DS} of 0.1 and 1.2 V is shown in Fig. 5.8(a)-(b). The device exhibits an on-state current of ~152 μA/μm at gate overdrive (V_{GS}-V_{TH}) of 2.5 V.

The device of this work suffers from high off-state leakage, leading to I_{on}/I_{off} ratio of ~2 orders of magnitude at V_{DS} of 1.2 V. The high off-state leakage current is the result of poor subthreshold swing (gate voltage required to change the drain current by one decade) that is caused by poor gate dielectric/InGaAs interface due to high surface defect density of the grown InGaAs channel layer.

The I_{DS}-V_{DS} of the transistor at various gate overdrives (V_{GS}-V_{TH}) from 0 to 2 V in steps of 0.2 V are plotted in Fig. 5.8(c). It exhibits well-behaved output characteristics despite the high off-state leakage.

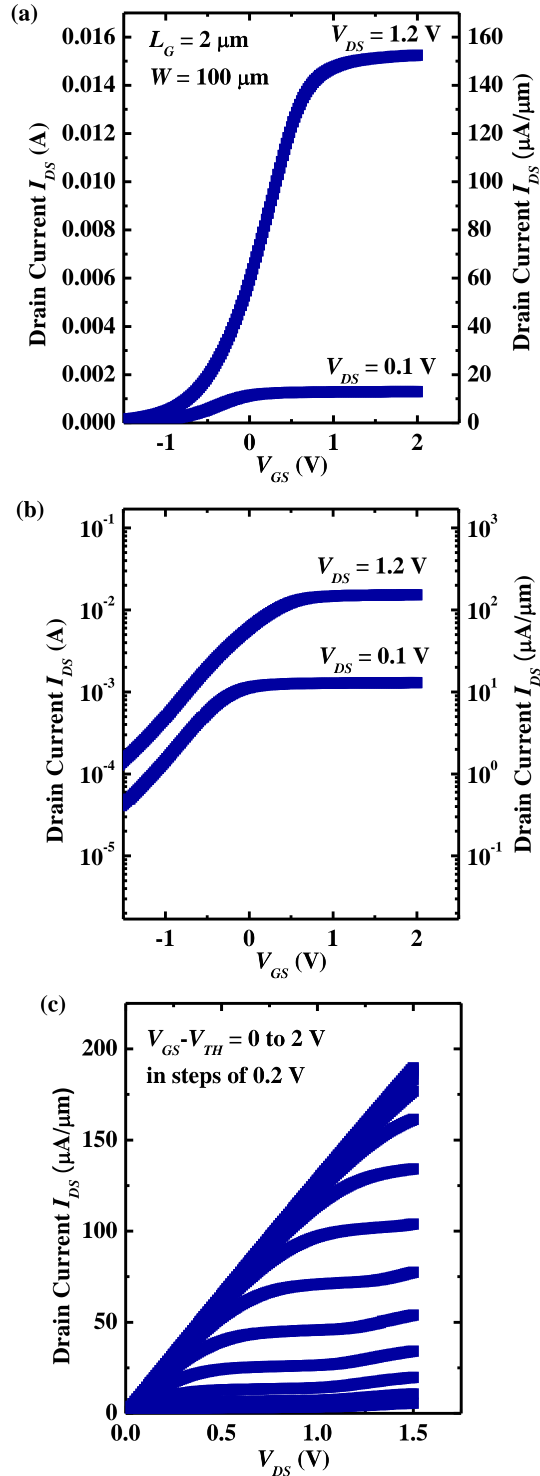

Fig. 5.8. (a) I_{DS}-V_{GS} of $In_{0.7}Ga_{0.3}As$ channel n-MOSFET on transistor-laser integrated substrate obtained at V_{DS} = 0.1 and 1.2 V. The gate length of the device is 2 µm and the gate width is 100 µm. (b) Log (I_{DS}) versus V_{GS} of the same device at V_{DS} = 0.1 and 1.2 V. (c) I_{DS}-V_{DS} plot of the same device at various gate overdrives (V_{GS}-V_{TH}) from 0 to 2 V.

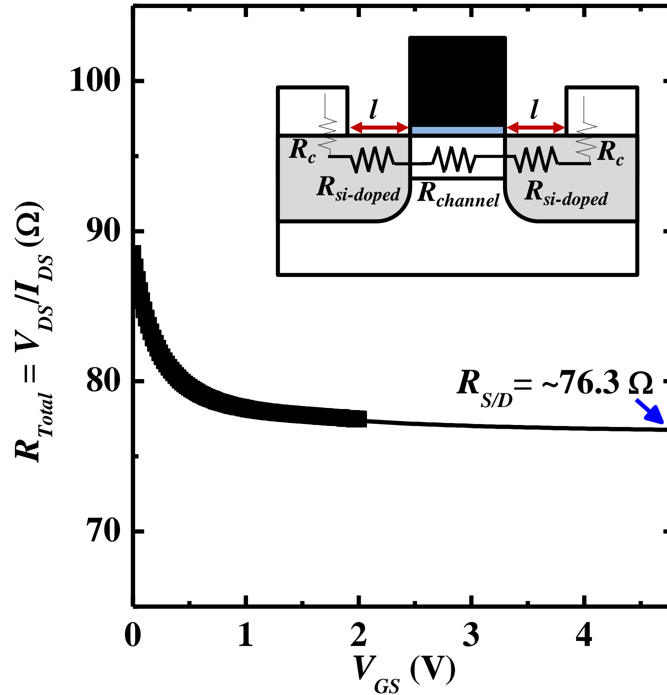

Fig. 5.9. Total resistance ($R_{Total} = V_{DS}/I_{DS}$) as a function of gate voltage of the same device as in Fig. 5.8. I_{DS} is the drain current in the linear regime (V_{DS} = 0.1 V). S/D series resistance $R_{S/D}$ of ~76.3 Ω is extracted at higher applied gate voltage when the channel is completely turned on and the total resistance is mainly contributed by S/D resistance. The normalized $R_{S/D}$ to the device gate width (W = 100 μm) is ~7.6 kΩ·μm. Inset shows the schematic of a non-self-aligned transistor where metal contact is l distance away from channel region. The l spacing of this device is 5 μm.

The S/D series resistance ($R_{S/D} = V_{DS} / I_{DS}$ at V_{DS} 0.1) of the device is ~7.6 kΩ·μm as extracted from R_{Total} versus gate voltage V_{GS} [Fig. 5.9]. The extracted $R_{S/D}$ is mainly contributed by PdGe/n$^+$-InGaAs contact resistance (R_c) and the resistance of Si-doped n$^+$-InGaAs/InAlAs ($R_{Si\text{-}doped}$) at source and drain regions due to the non-self-aligned process (inset of Fig. 5.9).

From transfer length method (TLM) test structure fabricated on the same substrate, the contact resistance between PdGe and n$^+$-InGaAs layer (R_c), and the sheet resistance of n$^+$-InGaAs/InAlAs (R_{sh}) were extracted. It should be noted that

the TLM test structure went through the same Si-implant and PdGe formation process as the fabricated transistors. Fig. 5.10(a) shows *I-V* characteristics obtained from two adjacent PdGe metal pads with various contact spacing. The extracted total resistance is plotted as a function of contact spacing d [Fig. 5.10(b)]. The $2R_c$ and R_{sh} values are extracted from the intercept and slope of the fitted line, respectively. The $2R_c$ and R_{sh} values are 35.1 Ω and 412.3 Ω/□, respectively. The $2R_c$ value normalized to the contact width gives ~3.51 kΩ.μm. The normalized $2R_c$ value represents the contact resistance between PdGe and n^+-InGaAs at both source and drain regions in the transistor. $R_{Si\text{-}doped}$ can be calculated from the extracted R_{sh} value using

$$R_{Si\text{-}doped} = [(l/W) \times R_{sh}] \times W, \tag{5.3}$$

where $R_{Si\text{-}doped}$ (Ω·μm) is the source or drain resistance between the edge of PdGe contact and the edge of InGaAs channel after normalizing by device gate width (W = 100 μm), l is the spacing distance between the edge of PdGe contact and the edge of InGaAs channel, and R_{sh} (Ω/□) is the sheet resistance of n^+-InGaAs/InAlAs.

The normalized $2R_{Si\text{-}doped}$ value is 4.12 kΩ.μm, representing n^+-InGaAs/InAlAs resistance between PdGe and channel from source and drain sides. The two values sum up to ~7.63 kΩ.μm, consistent with the extracted $R_{S/D}$ in Fig. 5.9. R_c and $R_{Si\text{-}doped}$ contribute 46% and 54% of the total $R_{S/D}$, respectively.

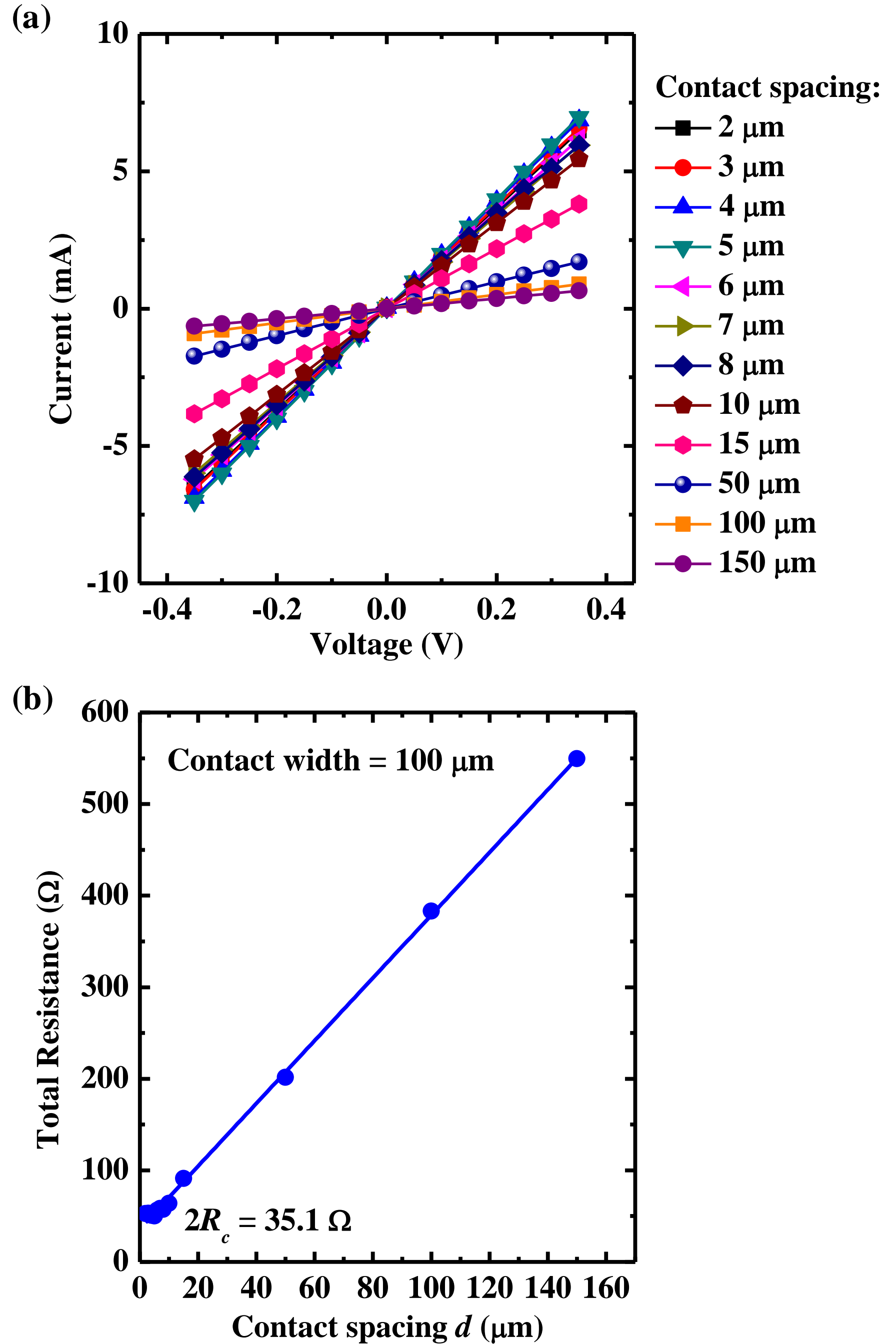

Fig. 5.10. (a) *I-V* curves measured between two adjacent PdGe metal contacts with different contact spacing formed on n^+-InGaAs/InAlAs. (b) Plot of total resistance between two PdGe metal contacts as a function of the contact spacing. The intercept gives $2R_c$ of 35.1 Ω (also equals to 3.51 kΩ·μm).

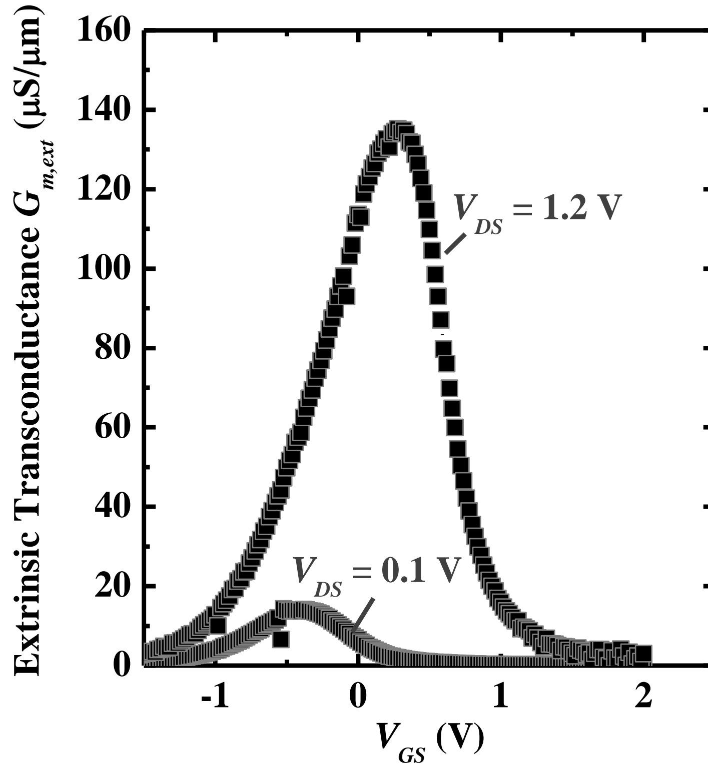

Fig. 5.11. Extrinsic transconductance of the same device as in Fig. 5.8.

Fig. 5.11 shows the extrinsic transconductance $G_{m,ext}$ of the device depicted in Fig. 5.8. The peak $G_{m,ext}$ value is 139 μS/μm at V_{DS} = 1.2 V. The peak intrinsic transconductance is obtained by taking out the effect of $R_{S/D}$ using Equation (4.2) in Chapter 4 [127]. The peak intrinsic transconductance ($G_{m,int}$) of the device is ~279 μS/μm at V_{DS} = 1.2 V. This value compares very well with InGaAs n-MOSFET made on InGaAs-on-GeOI on silicon substrate in Chapter 4.

In order to gain a much higher output current sufficient to meet the ~50 mA threshold current required by laser, transistors with large width were characterized. Fig. 5.12 shows the fabricated large-gate-width transistors. In a block of transistors that will be connected to a laser, there are four transistors with each two of them sharing one source layer.

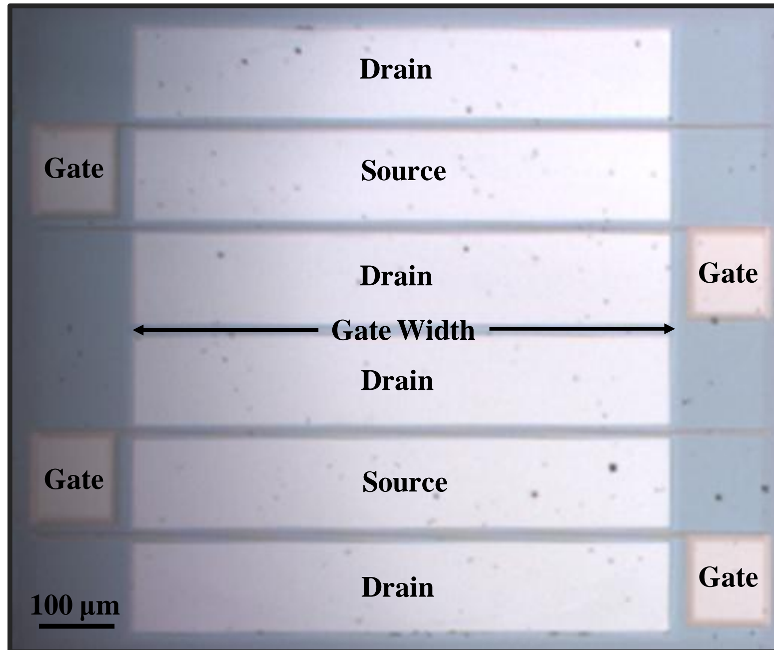

Fig. 5.12. Optical microscopy image of the fabricated transistors having large gate width (W = 720 μm). The transistors were fabricated by the author using the substrate illustrated in Fig. 5.2.

Fig. 5.13 shows the electrical performance of a large-gate-width transistor with gate length of 2 μm obtained at applied voltages V_{DS} of 0.1, 1.2, and 2 V. The device exhibits on-state current of 43 mA and 70 mA at V_{DS} of 1.2 and 2 V, respectively. This on-state current is higher than the threshold current required to turn on the laser.

Two options for supplying current to a laser are available, i.e. two transistors supplying current at V_{DS} = 1.2 V or a transistor supplying current at V_{DS} = 2 V. Fig. 5.14 shows the on-state drain current distribution of large-gate-width transistors at V_{DS} = 2 V. The output drain current of the transistors is in the range of 65 – 70 mA. The output drain current values are ~30% higher than the 50 mA threshold current required by the designed laser. This suggests that the width of the transistor of this work is appropriate and sufficient for pumping laser.

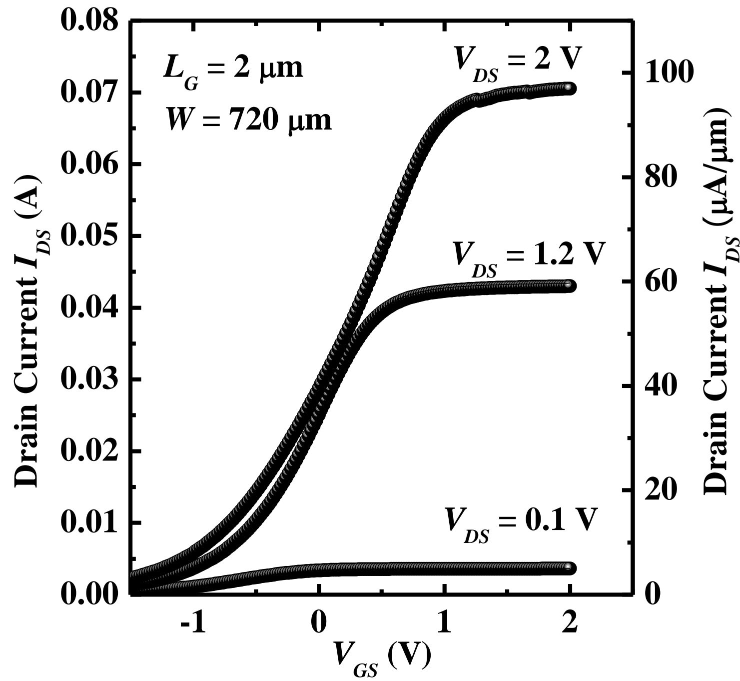

Fig. 5.13. I_{DS}-V_{GS} of a large-gate-width $In_{0.7}Ga_{0.3}As$ transistor measured at V_{DS} = 0.1, 1.2, and 2 V. The gate length of the device is 2 µm and the gate width is 720 µm.

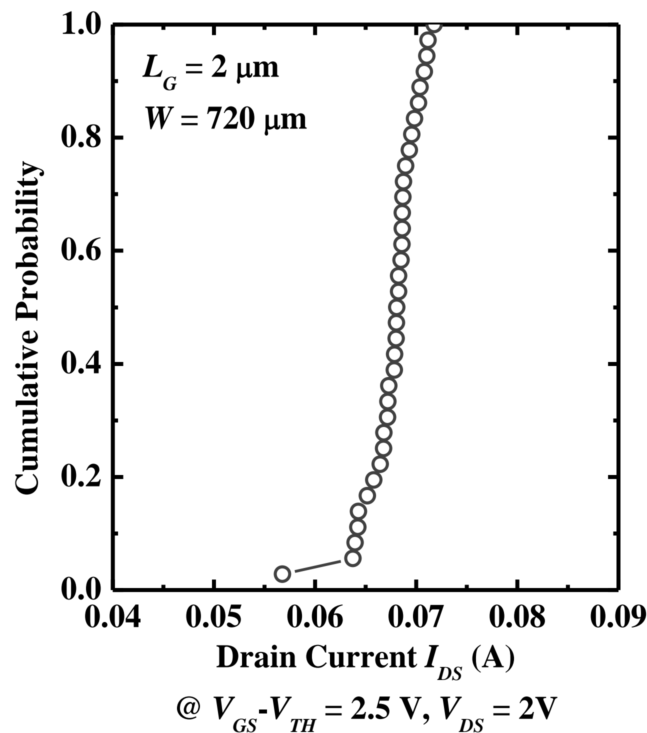

Fig. 5.14. Statistical plot showing the distribution of drain current at gate overdrive (V_{GS}-V_{TH}) of 2.5 V and V_{DS} of 2 V. The drain current is in the range of 65 – 70 mA. The yield of the transistor fabrication is ~90%. ~50 transistors were measured for this plot.

The laser diode fabrication which is undertaken by our collaborator is the final component to accomplish successful realization of transistor-laser co-integration. Currently, one of the challenges faced in the laser fabrication is the formation of a smooth mirror facet using anisotropic dry etching. Efforts in optimizing the anisotropic dry etching are currently on-going. Fig. 5.15 shows an SEM image of a laser fabricated with non-optimized dry etching recipe. The rough mirror facet resulted in inefficient laser with extremely poor lasing characteristics.

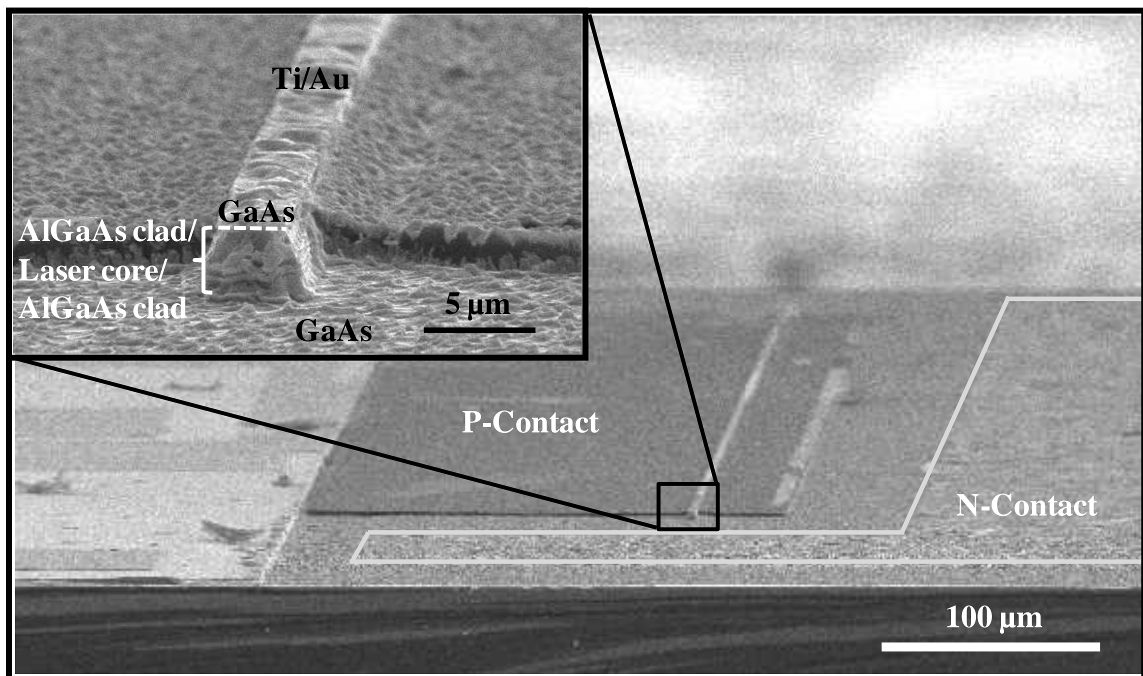

Fig. 5.15. SEM image of a laser fabricated with non-optimized anisotropic dry etch recipe. Inset shows the rough mirror facet formed.

5.4 Impact of Growth Defects on The Electrical Performance of InGaAs transistor

High quality InGaAs layer can be obtained by growing InGaAs layer on lattice-matched substrate, such as InP substrate. However, heteroepitaxial growth of InGaAs layer on Si substrate (lattice mismatch of 8%) with material quality comparable with that grown on lattice-matched substrate is still a challenge. While direct growth of InGaAs on Si can be avoided by using GeOI on Si substrate as starting substrate and by employing graded buffer technique for stress relaxation, the grown InGaAs layer is still far from defect free.

For InGaAs transistor formed on lattice-matched substrate, InGaAs surface dangling bonds are the main material defects that can cause detrimental effect on transistor electrical performance. Surface dangling bonds that are not well passivated right before gate-dielectric deposition will lead to interface traps formation, which can degrade the subthreshold slope and the on-state current of InGaAs transistor [151].

For InGaAs transistor formed on InGaAs heteroepitaxially grown on Si substrate, growth defects also need to be considered. However, the impact of growth defects on InGaAs transistor electrical performance has not been reported so far. In this section, the impact of common defects associated with heteroepitaxy growth, that are likely to be present in InGaAs layer (e.g. threading dislocations, surface steps, plane defects [152]-[157]) on InGaAs transistor electrical

performance is studied by means of two-dimensional (2-D) and three-dimensional (3-D) numerical simulations.

Threading dislocations, surface steps, and plane defects are primarily originated from misfit dislocation due to stress/strain relaxation during the heteroepitaxial growth process. These defects in InGaAs were modeled as electron traps (acceptor character, trap energy = 0.67 eV above valence band) and hole traps (donor character, trap energy = 0.32 eV and 0.4 eV above valence band) in the simulation [158]-[160].

The effect of electron and/or hole traps on the InGaAs transistor I_{DS}-V_{GS} characteristics was first studied using 2-D Taurus Medici simulator [161]. InGaAs transistors without and with a column of traps (electron traps or hole traps or electron and hole traps) placed in the center of the gate length were simulated. The transistor structure used in this simulation is depicted in Fig. 5.16. The effect of traps with different character on the I_{DS}-V_{GS} characteristics is shown in Fig. 5.17.

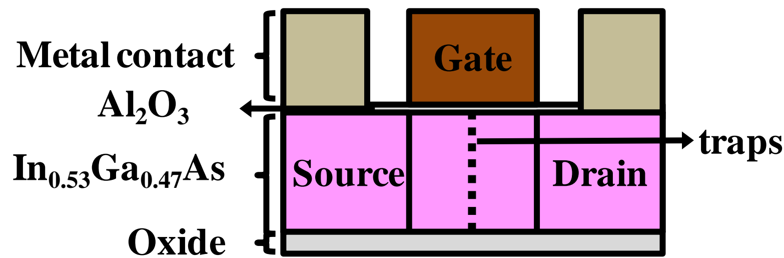

Fig. 5.16. Schematic of InGaAs device structure used in 2-D simulation. The thicknesses of Al_2O_3 and $In_{0.53}Ga_{0.47}As$ used in the 2-D simulation are 5 nm and 100 nm, respectively. The trap density used is 1×10^{22} cm^{-3}.

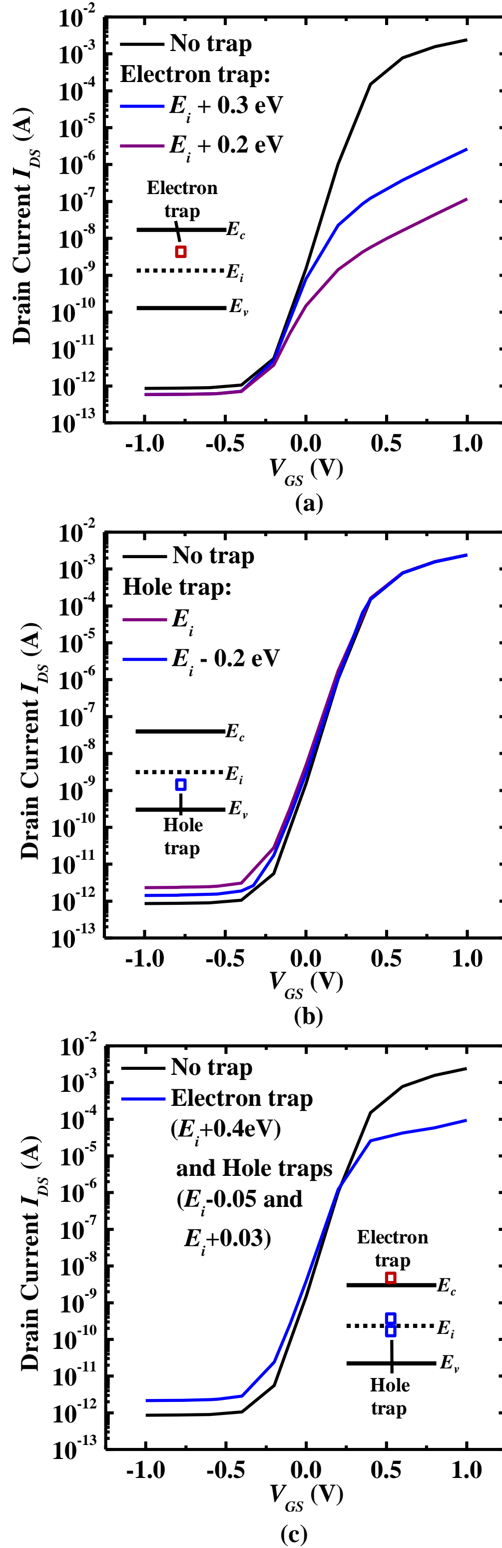

Fig. 5.17. I_{DS}-V_{GS} characteristics of 2-D simulated InGaAs transistors with the presence of (a) electron trap (acceptor characteristic), (b) hole trap (donor characteristic), and (c) electron and hole traps located at various energy positions.

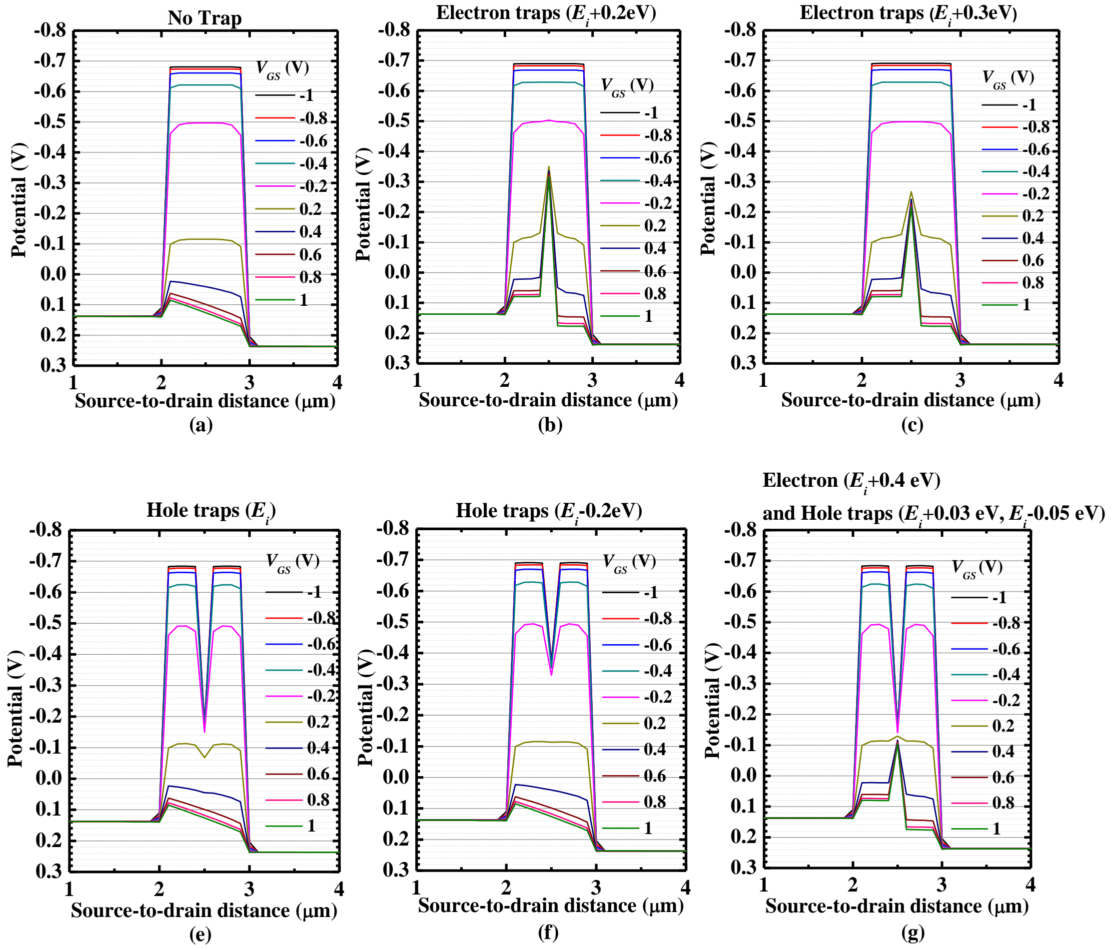

Fig. 5.18. Potential diagram of InGaAs at 2 nm below channel surface from source to drain for transistor with (a) no trap, (b) electron trap (E_i+0.2 eV), (c) electron trap (E_i+0.3 eV), (d) hole trap (E_i), (e) hole trap (E_i-0.2 eV), and (f) electron (E_i+0.4 eV) and hole traps (E_i-0.05 eV, E_i+0.03 eV).

Electron traps (acceptor character) are neutral when traps are empty, and negatively charged when traps are filled/occupied. The occupancy of traps is higher for trap energy position closer to valence band. Electron traps closer to valence band, therefore, create a relatively higher potential barrier [Fig. 5.18(a-c)] seen by carrier moving from source to drain when the transistor is inverted. This results in transistor with much lower on-state current as compared with that of no trap, under same positive gate voltage [Fig. 5.17(a)].

On the other hand, hole traps (donor character) are positive charged when traps are empty, and neutral when traps are filled. Unfilled hole traps create barrier lowering [Fig. 5.18(e-g)] which leads to higher subthreshold current and subthreshold slope [Fig. 5.17(b)]. When both electron and hole traps are present, degradation in both subtheshold slope and on-state current are observed [Fig. 5.17(c)].

Next, 3-D Technology Computer Aided Design (TCAD) Synopsys Sentaurus simulation [162] was carried out to model threading dislocation (TD), surface steps, plane defects in InGaAs transistor, and to study the effects of these defects on the I_{DS}-V_{GS} characteristics. Fig. 5.19 shows the simulated 3-D InGaAs transistor device structure. TD was modeled as electron and hole traps arranged in one column of atoms. Extension of TD forming a dislocation segment was also modeled as electron and hole traps arranged in a few columns of atoms. Surface steps are modeled as a row of electron and hole traps on InGaAs surface. Plane defects are modeled as a plane of electron and hole traps in InGaAs channel normal to the surface connecting source to drain.

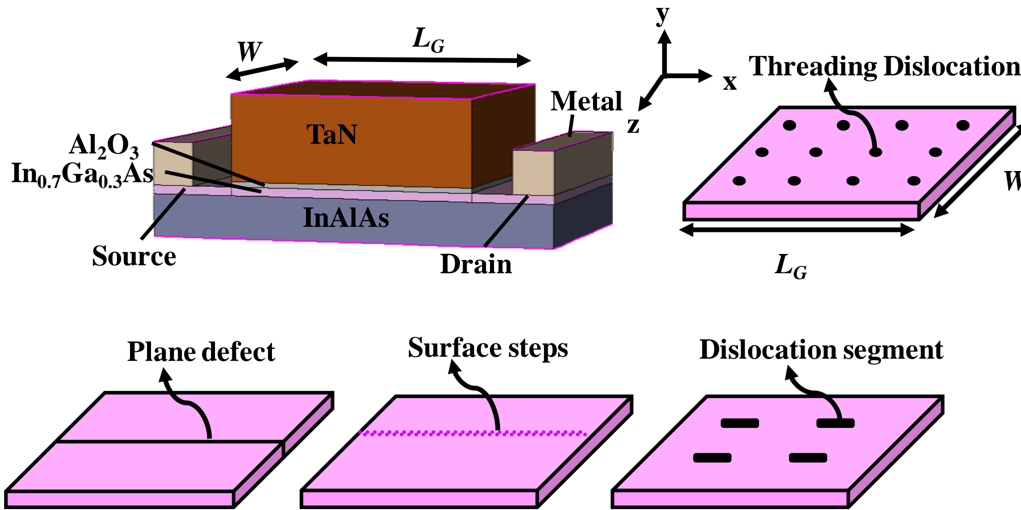

Fig. 5.19. Schematic of InGaAs device structure used in 3-D simulation. The thicknesses of Al_2O_3 and $In_{0.7}Ga_{0.3}As$ used in the 3-D simulation are 6 nm and 10 nm, respectively. The placement of traps to represent threading dislocation, dislocation segment, surface steps, and plane defect are illustrated.

The I_{DS}-V_{GS} characteristics of InGaAs transistor with various TD spacings are shown in Fig. 5.20(b). The effect of TD becomes significant for TD spacing below 50 nm. The subthreshold slope is degraded by 20% with TD spacing of 50 nm. However, comparable on-state currents for various TD spacings are observed. This can be explained by the tendency of carriers to avoid potential barrier created by a TD and to flow in between TDs where the potential is relatively low. Extending a TD to form a dislocation segment has negligible effect on the I_{DS}-V_{GS} characteristics as shown in Fig. 5.20(c).

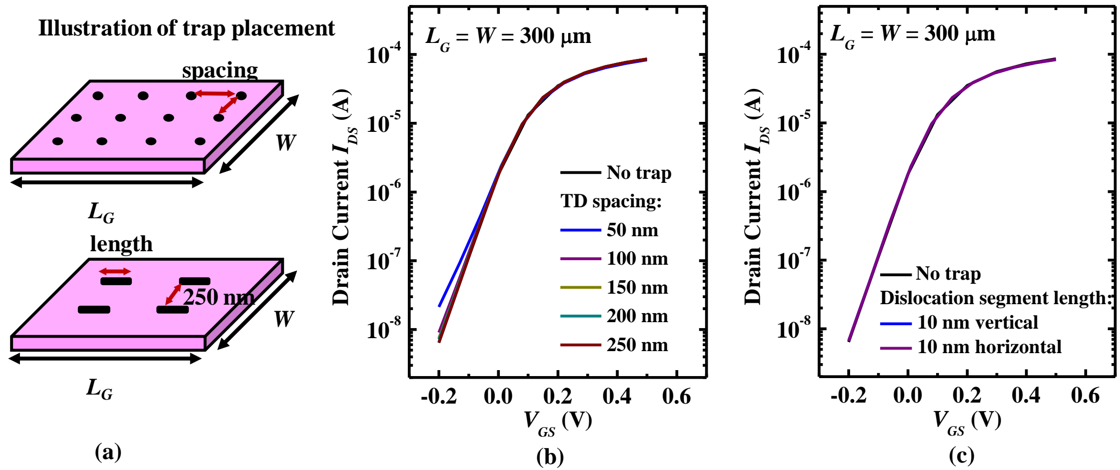

Fig. 5.20. (a) Illustration of trap placement to model threading dislocations and dislocation segments. I_{DS}-V_{GS} characteristics of 3-D simulated InGaAs transistors with (b) threading dislocations with varying spacing and (c) dislocation segments with varying length.

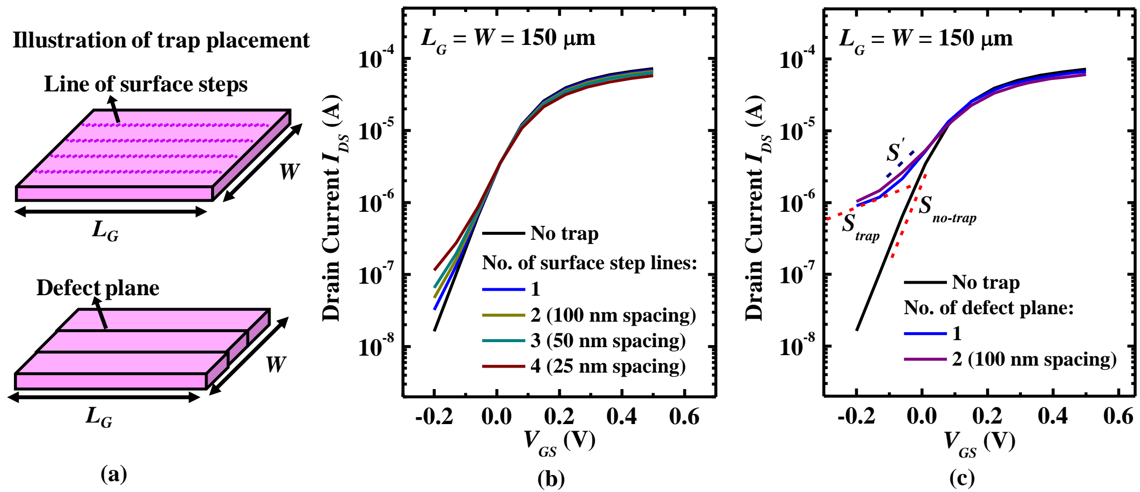

Fig. 5.21. (a) Illustration of trap placement of lines of surface steps and defect planes. I_{DS}-V_{GS} characteristics of 3-D simulated InGaAs transistors with various number of (b) lines of surface steps and (c) plane defects.

Surface steps lying from source to drain have an effect on the subthreshold region of the I_{DS}-V_{GS} characteristics when the number of lines increases [Fig. 5.21(b)]. When gate voltage is biased in depletion regime, the potential along the line of traps is lowered and thus allowing current to flow. Increasing the number of

lines allows higher current conduction that contributes to the higher subthreshold current observed. The on-state current reduction observed is likely to be caused by narrower line spacing. The potential at region in between neighboring lines has higher influence by the potential barrier created by the lines of traps when the line spacing is small. It is observed that transistor with four lines of surface steps with 50 nm spacing has 33% degradation in subthreshold slope and ~20% reduction in on-state current.

Plane defect extending from source to drain has the largest effect on the subthreshold characteristics as shown in Fig. 5.21(c). Two slopes (S_{trap} and $S_{no\text{-}trap}$) were observed in the subthreshold region of the I_{DS}-V_{GS} characteristics. The slope (S_{trap}) with the least steep gradient is contributed by current conduction through traps. When gate voltage (V_G) is biased in depletion regime, the potential along plane defect is lowered due to the present of traps and thus allowing current conduction from source to drain. This contributes to the high current observed in this regime as compared with that of no-trap. The slope S_{trap} suggests that the current conduction through traps is gate dependent. The small gradient of S_{trap} implies that the current conduction through defected region has weak gate control.

As gate voltage is increased, the slope (S') deviates from S_{trap}. This is due to current conduction at region away from defected region starts to dominate. It is observed that S' has gradient larger than $S_{no\text{-}trap}$ due to the influence of current flowing through defects. Slight reduction of on-state current of ~7% is also observed. With larger number of plane defects, larger deviation of S' from $S_{no\text{-}trap}$ which results in smaller gradient of S' is observed.

Fig. 5.22 shows experimental I_{DS}-V_{GS} data of two InGaAs transistors fabricated using same process conditions on InGaAs layer grown on GeOI on Si substrate with different growth conditions. The fabrication process flow and the epilayer structure grown are elaborated in section 5.2. From the cross-sectional TEM images of the two grown sample (not shown), the defect density of the two samples was estimated to be ~10^9 cm^{-2} and ~10^7 cm^{-2} by counting the number of defect reaching InGaAs surface. The type of defects (TD or dislocation segment or plane defect) cannot be distinguished from the cross-sectional images. Nevertheless, the ~100× difference in the density estimation suggests that one is of poorer quality than the other. The effect of growth defects on transistor I_{DS}-V_{GS} characteristics as shown in the 3-D simulation results can explain the similar characteristics observed in the experimental data in Fig. 5.22. Two slopes were observed in the subthreshold region of the experimental I_{DS}-V_{GS} plot. The slope S_{trap} suggests possible existence of high density of traps, such as plane defect, from source to drain in the InGaAs channel layer. The gate-dependent current conduction through defects causes the large subthreshold slope of the two transistors. Transistor on InGaAs layer with higher defect density would have larger subthreshold slope.

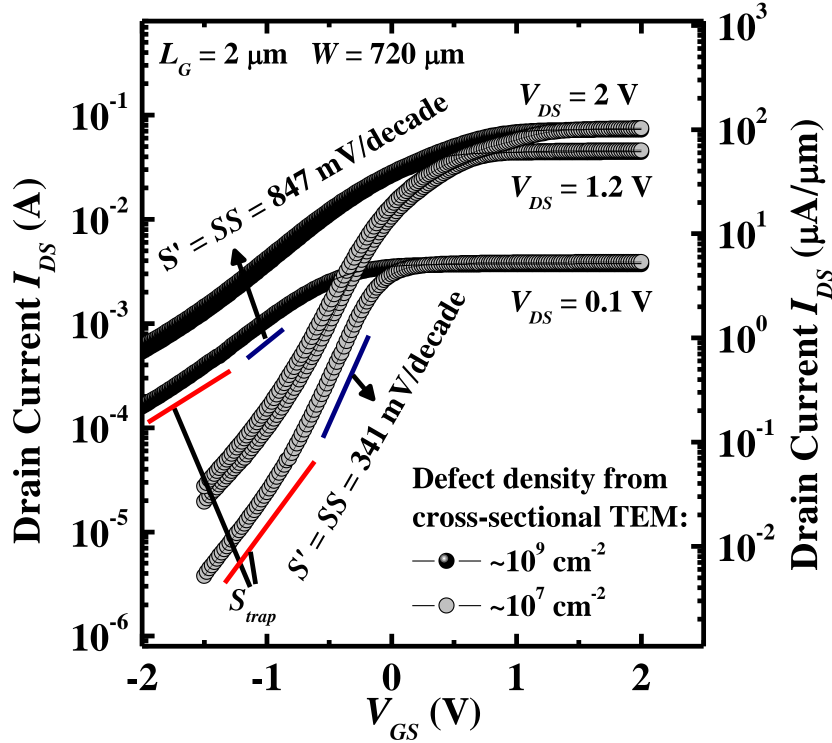

Fig. 5.22. I_{DS}-V_{GS} of $In_{0.7}Ga_{0.3}As$ transistors measured at V_{DS} = 0.1, 1.2, and 2 V. The gate length of the device is 2 µm and the gate width is 720 µm. Black and gray solid symbols are data obtained from transistor fabricated on InGaAs epilayer with defect density of ~10^9 cm^{-2} and ~10^7 cm^{-2}, respectively.

5.5 Summary

This Chapter presents several key works to address various challenges for the co-integration of InGaAs-based transistors and lasers on common GeOI on silicon platform. The design of layer structure of the substrate for transistor-laser integration, device layout structure, fabrication of InGaAs n-MOSFETs on the grown substrate, and electrical characterization of the fabricated transistors are discussed. The InGaAs n-MOSFETs formed on the grown substrate exhibit sufficiently high on-state current for pumping the lasers. The effect of growth defects on InGaAs transistor electrical performance is also studied. The results in

this Chapter are important and have contributed to progress towards InGaAs transistor integration in Si CMOS and the co-integration of high mobility electronic devices and photonic devices on a common platform.

Chapter 6

Conclusion and Future Works

6.1 Conclusion

The continuous down-scaling of Si-based complementary metal-oxide-semiconductor (CMOS) devices has enabled higher device packing density and performances. However, the performance enhancement will soon be limited by the fundamental limit imposed by the material properties of Si. Higher mobility material is needed to replace silicon channel material for future logic application. For n-channel metal-oxide-semiconductor field-effect-transistors (n-MOSFETs), III-V compound semiconductor, such as $In_xGa_{1-x}As$ (also denoted as InGaAs), is the most matured and suitable channel material.

Before InGaAs can be introduced in future CMOS technology node, several key challenges which include poor interface quality of InGaAs gate stack, issues related to the scaling of InGaAs transistors, lack of source/drain (S/D) contact technology compatible with Si CMOS, and issues related to heterogeneous integration of InGaAs transistors on Si platform, should be addressed.

Moreover, the high performance benefit of InGaAs n-MOSFETs should not be offset by limitations associated with scaled metal interconnect. One promising approach to overcome the metal interconnect limitations is by replacing it with

optical interconnect. However, the integration of high mobility transistors and optical devices, preferably at the intra-chip level, needs to be realized.

This thesis has explored new contact technology suitable for $In_xGa_{1-x}As$ n-MOSFETs, the integration of $In_xGa_{1-x}As$ n-MOSFETs on Si platform, and key works for the co-integration of InGaAs-based electronic and optical devices on a common Si platform. The main contributions of this thesis are summarized in next Section.

6.2 Contributions of This Thesis

6.2.1 CoInGaAs as a Novel Self-Aligned Metallic Source/Drain Material for Implant-less $In_{0.53}Ga_{0.47}As$ n-MOSFETs

In Chapter 2, self-aligned metallization analogous to silicidation process for InGaAs n-MOSFET using Co was successfully demonstrated [162]-[163]. The demonstration involved the study of Co reaction with InGaAs forming CoInGaAs metallic material, the investigation of chemical etchants for the removal of Co over CoInGaAs, and the adoption of self-aligned metallization of Co in InGaAs transistors. The realization of InGaAs n-MOSFETs with self-aligned metallic S/D allows the formation of metallic material close to the channel, thus eliminates the resistance contribution from n-doped InGaAs in between metal contact pad and channel that normally exists in InGaAs transistors with non-self-aligned scheme. $In_{0.53}Ga_{0.47}As$ n-MOSFETs with CoInGaAs S/D show reasonably well-behaved output characteristics. Several drawbacks of using CoInGaAs as S/D material

such as high off-state leakage and contact resistance were observed. These were later solved by exploring alternative metal for the self-aligned metallization.

6.2.2 Material Characterization of Ni-InGaAs as a Contact Material for InGaAs Field-Effect Transistors

In Chapter 3, an alternative material, such as Ni, was explored for self-aligned metallization of InGaAs [88]-[89]. This Chapter presents the study of Ni reaction with InGaAs forming Ni-InGaAs material, the investigation of band alignment at Ni-InGaAs/InGaAs interface, and the characterization of material as well as electrical properties of Ni-InGaAs. The results in this Chapter provide useful information for assessing the suitability of Ni-InGaAs to be used as S/D material for InGaAs transistors. In addition, the study in this Chapter indicates that Ni-InGaAs has better electrical property and uniformity than CoInGaAs.

6.2.3 N-Channel InGaAs Field-Effect Transistors on Germanium-on-Insulator Substrates with Self-Aligned Ni-InGaAs Source/Drain

In Chapter 4, InGaAs n-MOSFET with self-aligned Ni-InGaAs metallization is realized [164]. It was first demonstrated on InGaAs-on-InP substrate. Ni-InGaAs self-aligned contact technology was later employed in the integration of $In_{0.7}Ga_{0.3}As$ channel MOSFETs on GeOI on Si substrate. The performance of $In_{0.7}Ga_{0.3}As$ channel MOSFETs on GeOI on Si substrate compares very well with the state of the art InGaAs transistors. The results in this Chapter indicate that the integration of InGaAs-on-GeOI on Si substrate is

promising, paving the way for co-integrating InGaAs n-MOSFET and Ge-based p-MOSFET on a common platform. In addition, the thermal stability and specific contact resistivity of Ni-InGaAs film is improved with Pt incorporation in the film. This suggests that Ni(Pt) can be a suitable metal for self-aligned S/D metallization not only for Ge and Si, but also for InGaAs.

6.2.4 Process Development for InGaAs-based Transistor and Laser Integration on GeOI on Si Substrates

In Chapter 5, several key works to address various challenges for co-integrating InGaAs-based transistors and lasers on common GeOI on Si substrate are presented. These include designing the layer structure of the substrate for transistor-laser integration, establishing the device layout structure, fabricating InGaAs n-MOSFETs on the grown substrate, and characterizing the electrical output of the fabricated transistors. The fabricated InGaAs n-MOSFETs exhibit good transfer characteristics with on-state current higher than threshold current required by the laser diodes designed in this work. The works in this Chapter enable realization of InGaAs-based transistors and lasers at the intra-chip level.

6.3 Future Directions

This thesis has presented promising preliminary results for solving several key challenges of InGaAs n-MOSFETs for future logic applications. However, it also opens up issues for further improvement.

Although InGaAs n-MOSFETs with self-aligned silicide-like metallization have been successfully demonstrated in Chapter 2 to 4, contact resistance of the metallic S/D material contributes a significant portion to the total series resistance of the transistors. Future works should focus on the contact resistance reduction. One way to do so is to form highly n^+-doped layer in between Ni-InGaAs layer and InGaAs channel layer. Technique such as dopant segregation [166]-[169] which has been very well-studied in Si and Ge contact technology can be explored for forming the highly n^+-doped layer. This technique can be used to dope InGaAs at the Ni-InGaAs/InGaAs interface. Another way to form highly n^+-doped layer is by using *in-situ* doping technique [170],[39]. This will allow achieving doping concentration above maximum concentration (~4.1×10^{18} cm^{-3} [38]) that can be obtained using the conventional Si implant. Monolayer doping (MLD) technique can also be considered for the formation of highly n^+-doped S/D [171]-[172]. These proposed techniques are suitable for scaled planar and non-planar transistor. Another aspect for future work is thermal stability study of Ni-InGaAs contact material on InGaAs. This is also an important topic to explore as good contact material should be able to withstand any elevated temperature steps in the back-end process.

In Chapter 4 and 5, InGaAs n-MOSFETs were successfully integrated on GeOI on Si substrate by employing graded-buffer growth approach for the growth of the III-V layers. Several key works towards realizing InGaAs-based transistor and laser co-integration on a common substrate were presented. The success of this realization will potentially eliminate limitations associated with the scaling of

metal interconnect. Nevertheless, further work to reduce the epilayer thickness is required for the adoption of InGaAs MOSFETs in future technology node in a cost-effective way. At the same time, the defect density in the thin III-V layers should be kept low for realizing high performance InGaAs transistors.

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Appendix

List of Publications

Journal Publications

[1] **Ivana**, E. Y.-J. Kong, S. Subramanian, Q. Zhou, J. Pan, and Y.-C. Yeo, "CoInGaAs as a novel self-aligned metallic source/drain material for implant-less $In_{0.53}Ga_{0.47}As$ n-MOSFETs," *Solid-State Electronics*, vol. 78, pp. 62, 2012.

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[4] **Ivana**, S. Subramanian, M. H. S. Owen, K. H. Tan, W. K. Loke, S. Wicaksono, S. F. Yoon, and Y.-C. Yeo, "N-channel InGaAs field-effect transistors formed on germanium-on-insulator substrates," *Applied Physics Express*, vol. 5, 116502, 2012.

Conference Publication

[5] **Ivana**, S. Subramanian, E. Y.-J. Kong, Q. Zhou, and Y.-C. Yeo, "Co-InGaAs as a novel self-aligned metallic source/drain material for implant-

less $In_{0.53}Ga_{0.47}As$ n-MOSFETs," *International Semiconductor Device Research Symposium*, 2011, TA5-03.