ELECTROCHEMICAL DEPOSITION OF CIS FILMS FOR PHOTOVOLTAIC APPLICATIONS

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DECLARATION

I hereby declare that the thesis is my original work and it has been written by me in its entirety. I have duly acknowledged all the sources of information which have been used in the thesis.

This thesis has also not been submitted for any degree in any university previously.

Zhang Shiyun

26th Apr 2013

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SUMMARY

Copper indium diselenide polycrystalline films of p-, i- and n-type electrical conductivity were deposited on Molybdenum (metal strip and sputtered on Si-wafer) from a single bath using direct-current and pulse-plating deposition, at cathodic potential ranging -0.3V to -1.3V, with a thickness between 100-200nm. Electrochemical deposition mechanism results were correlated using Energy-Dispersive-X-ray Spectroscopy and X-Ray-Diffraction. Scanning-Electron-Microscopy was employed for surface morphology studies and Photoelectrochemical cell for p/i/n-type films conductivity. Photovoltage results indicate that p- and n-type CIS layers can be obtained by varying deposition potential under DC-plating at room temperature, pulse-plating at room temperature and 40°C on Mo-wafer. Generally, p-type can be obtained at relatively high potential of -0.3V and -0.7V, where n-type at more negative deposition potentials. To form a complete p-i-n junction from a single bath, pulse-plating at 40°C is recommended with negative plating limiting to pulse cycled from -0.3V (p-type) to -0.7V (intrinsic) and finally to -1.1V (n-type).

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1. INTRODUCTION

Present global energy production is largely accomplished by burning of fossil fuels, which inevitably relates inherent issues associated with the limited resources as well as environmental problems. Solar energy from photovoltaic has received increasing favor as an alternative source for future electricity by converting direct sunlight to electricity.

However, the costs of producing photovoltaics (cost per watt) are higher than the conventional methods. As a result, it may not be the preferred choice between the two. Nevertheless, cost effectiveness can be lowered through improving efficiency or reducing production cost.

Copper Indium Diselenide (CIS) is one of the fastest developing materials for thin-film photovoltaic solar cells due to its excellent optical and photovoltaic properties through direct energy band gap and high absorption coefficient. Having the advantage of direct bandgap of $\approx$ 1.05eV by [8], Copper Indium Diselenide is consider a high absorption coefficient materials as well as having large minority carrier diffusion length, thus forming a suitable film for photovoltaic applications. Contreras *et al* [9] have achieved a high conversion efficiency of almost 19% with these materials.

CIS films can be prepared by gaseous and liquid phases, such as physical vapour deposition, sputtering, molecular beam epitaxy, metal-organic chemical vapour deposition etc. Electrodeposition has its advantage for mass production in terms of large surface area and high volume productions. It is more economical since the steps are simple [6] and does not required sophisticated high vacuum machines and stringent environments it also uses relative lower temperature than other processes.

Generally, electrodeposition of CuInSe films can be simplified in the following written reaction:

$$Cu(II) + 2Se(IV) + In(III) + 13e^- \rightarrow CuInSe_2$$

Inevitably, the film would contain binary phases in addition to the chalcopyrite CIS phases [18] in acidic medium, namely Cu_xSe and In_2Se_3. The reactions can be summarized as follows:

I. $xCu(II) + Se(IV) + (2x+4)e^- \rightarrow Cu_xSe$

II. $3Se(-II) + 2In(III) \rightarrow In_2Se_3$

III. $Cu_2Se + In_2Se_3 \rightarrow CuInSe_2$

Where x is the ratio of fluxes at the electrode surface of Cu(II) ions and Se(IV) ions, which were proportional to the concentration of the ions in the electrolyte assuming reaction is limited by diffusion.

Formation of Copper Selenide Cu_2Se and Indium Selenide In_2Se_3 occurs first before the formation of CIS growth. Deposition of Cu_2Se occurs initially which depends on the diffusion coefficient of the Se(IV) and Cu(II). With sufficient In(III) in the solution, Selenium deposited can further reduced to Se(-II) while reacting with In(III) producing In_2Se_3, which were controlled by the deposition potential [15].

Further findings were made by Chassing E. et al (2008) [5] on the electrodeposition mechanism on a rotating disc electrode. At deposition potentials between -0.3V to -0.4V, Cu_3Se_2 were produced according to the following reactions:

$$3Cu(II) + 2\ H_2SeO_3 + 8H^+ + 14e^- \rightarrow Cu_3Se_2 + 6H_2O$$

As deposition potential decrease further, Cu_3Se_2 will be reduced to CuSe, and dissolution of Se(IV) would reduced to Se and deposit on CuSe, as follows:

$$Cu_3Se_2 + H_2SeO_3 + 4H^+ + 4e^- \rightarrow 3CuSe + 3H_2O$$

$$H_2SeO_3 + 4H^+ + 4e^- \rightarrow Se + H_2O$$

As the deposition potentials decreases to around -0.6V, Indium will be incorporated into the deposit. However, it was suggested that an amorphous passive layer would be form with stoichiometry close to $CuSe_2$, that acts like a blocking absorbate, suspected to be In-Se compound. This layer has low conductivity easily absorbed onto the surface. After the formation In-Se compound, $CuInSe_2$ will be formed according to the general reaction as stated above:

$$Cu(II) + 2H_2SeO_3 + In(III) + 8H^+ + 13e^- \rightarrow CuInSe_2 + 6H_2O$$

$$2Cu(II) + H_2SeO_3 + 4H^+ + 8e^- \rightarrow Cu_2Se + 3H_2O$$

In addition to the formation of $CuinSe_2$, Se was also produced together with CuSe binary phase concurrently. As the deposition potential further reduced, the “passivation” effect would be lifted off as the deposition current were limited by diffusion of Se(IV) and Cu(II) ions. In another words, composition is mainly governed by the ratio of the Cu and Se in solution and the kinetics of indium reaction.

Moreover, Chaure *et al* [8] have extensively studied the growing both p^+ and n^+ layers by electrodeposition, which is useful for forming good ohmic contacts to both p-, and n- type CIS layers. The conductivity type of the deposited layers was obtained in terms of structural and electrical properties through PEC measurements, verified with XRD and XRF. Furthermore, by varying the deposition potential, it is possible to deposit p-, i- and n-type materials directly from a single

deposition bath. The electrical parameters could be manipulated to control the film's properties, structure and composition.

Studies have been made in growth of copper indium diselenide compound by electrodeposition on Mo-coated glass (FTO), Roussel *et al* indicates that the growth of CuSe phase on the initial nucleation before corporation of Indium can proceed, moreover, the publication shown that In/Cu ratio relations increase with deposition time [18].

In addition, Phok *et al* [15] had successfully grown $CuInSe_2$ nanowires on porous alumina templates by pulse plating, which gave a $CuInSe_2$ composition close to stoichiometry. The purpose of this thesis is to further study the electrodeposition processes for the preparation of thin film $CuInSe_2$ on Mo substrates, produced by Mo sputtered on wafer and directly Mo metal strip, to obtain p-, i- and n-type conductivity from a single chemical bath by both direct current and pulse plating profile.

1.1 THIN FILMS SOLAR CELLS – COPPER INDIUM DISELENIDE

History of $CuInSe_2$ solar cells works were initiated at Bell laboratories in the early 1970s [22] where they grew a wide selection of these materials and characterized their structural, electronic and optical properties. However, optimized efficiency is only 12% back then. $CuInSe_2$ was considered promising for solar cell because of it favorable electronic and optical properties, including direct bandgap with absorption coefficient and inherent p-type conductivity which will be further discussed in the following section.

$CuInSe_2$ have chalcopyrite lattice structure, is a diamond-like structure, similar to sphalerite structure, with an order substitute of Group I (Cu) and Group III (In) elements on the Group II (Zn) sites of sphalerite. The diagram below shows a tetragonal unit cell of chalcopyrite lattice structure.

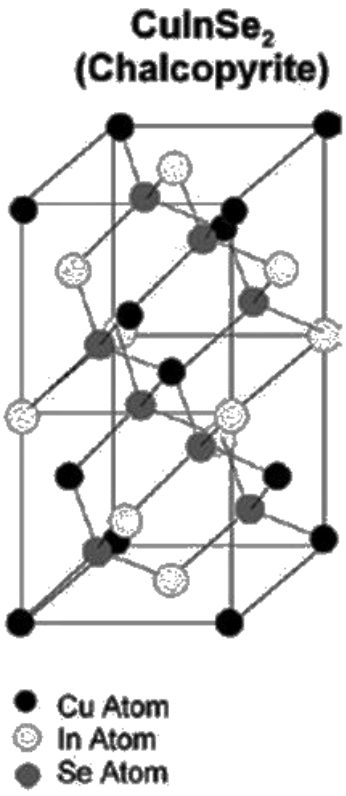


Figure 1: the unit cell of chalcopyrite lattice structure

The deviation from c/a =2 is called the tetragonal distortion and stem from different strengths of the Cu-Se and the In-Se bonds. Possible phases in Cu-In-Se system are indicated in the ternary diagram below:

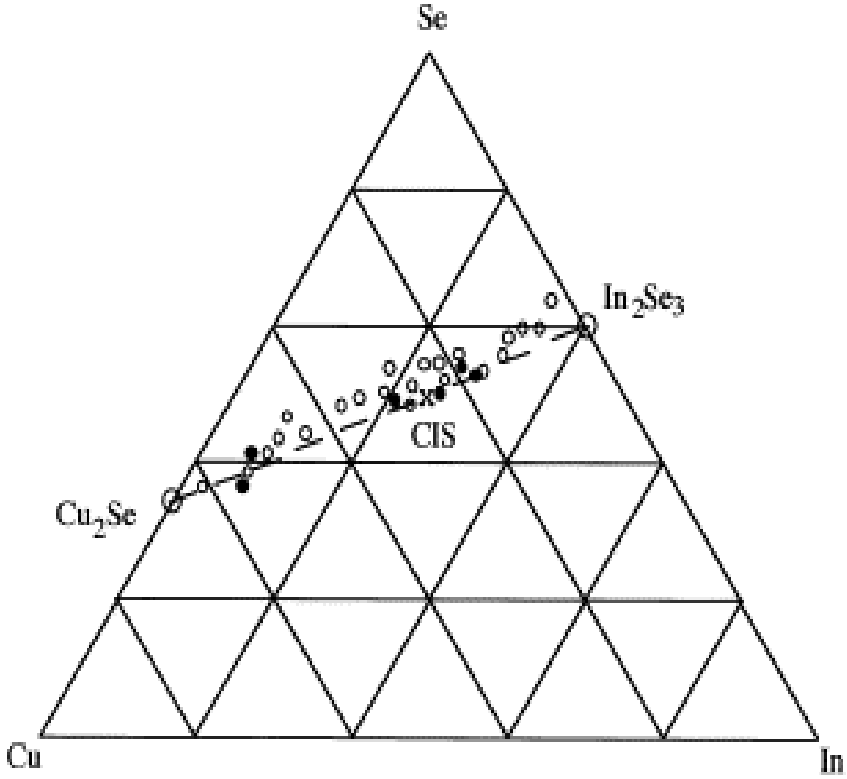


Figure 2: Ternary phase diagram of Cu-In-Se system. Thin film composition near pseudo-binary Cu2Se-In2Se3 tie line

Chalcopyrite CuInSe is located in this line. A detailed Cu_2Se-In_2Se_3 tie-line near $CuInSe_2$is described by the pseudo-binary phase diagram reproduced in the figure below:

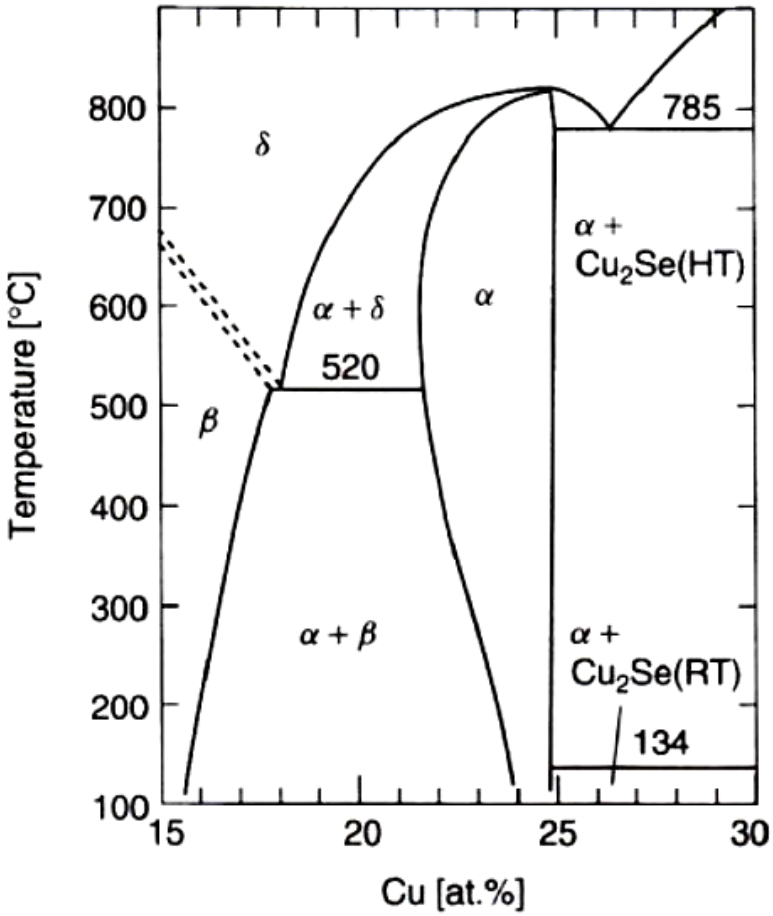


Figure 3: Pseudo-binary phase diagram of Cu-In-Se system

The chalcopyrite $CuInSe_2$ phase is denote as α, δ is a high temperature phase with sphalerite, and β is an ordered defect compounds (ODC) known to have chalcopyrite structure with structurally ordered insertion of intrinsic defects. At lower temperature, single phase field for $CuInSe_2$ is relative narrow and does not contain the composition of 25% Cu. However at higher temperature around 500°C, thin films are typically grown, and phase field widen towards the In-rich side. Typically average composition of device-quality film has 22-24% Cu, which falls within a single phase region at growth temperature.

Generally most of the solar cells are made of mono or polycrystalline silicon. However, silicon is not an ideal absorber material for solar cells due to the presence of indirect band gap which does not absorb light

as efficient as those with direct band gaps. In order to achieve sufficient light absorption, very thick and high quality silicon is used in solar cells and to allow for minority carrier lifetimes and diffusion length long enough such that recombination of the photo-generated charge carriers is minimized, to contribute to the photocurrent. Kasap [12] mentioned that Si-based solar cell efficiencies ranges from 18% for polycrystalline, up to 24% in high efficiency single crystal devices that have special structures to absorb as much photons as possible, known as homojunctions. The best Si-homojunction solar cell efficiencies are about 24% for single crystal passivated emitter rear locally diffused cells.

Nevertheless, due to the limitations of crystalline silicon, other absorber materials have been studied extensively, such as semiconductor with direct band gap with high absorption coefficients were studied for thin film application in solar cells.

Several advantages of thin film solar cells is preferred over crystalline silicon, in consideration of the follow, namely; usage of less material typically few micrometers, therefore impurities and crystalline imperfections can be greatly reduced relative a crystalline silicon. Secondly, there are a wide variety of processes to obtain thin films on inexpensive substrates (e.g. glass) as well as flexible substrate (e.g. flexible pcb), Lastly, composition of the thin film can be easily manipulate by processes.

Low cost thin film solar cell materials are usually CdTe (cadmium telluride), amorphous hydrogenated Silicon (a Si:H) and $CuInSe_2$ (Copper Indium Diselenide) and its alloy either Ga and/or S. Amorphous silicon has higher absorption coefficient and closer bandgap of 1.5eV from the ideal, than that of polycrystalline silicon. However, the major disadvantage of amorphous silicon made solar cell is the light-induced degradation leading to a drop of conversion efficiency from the initial value, knowning as "*Staebler-Wronski effect*".

This results from defects (such as dangling bonds) created by illumination that acts as recombination centers, causing stabilization efficiencies of amorphous silicon solar cell to be as low as 13% as mentioned by Kermell [13].

Unlike amorphous silicon, polycrystalline compound semiconductor materials such as CdTe (cadmium telluride) and $CuInSe_2$ (Copper Indium diselenide) and its alloy either Ga and/or S, do not face light-induced degradation. In addition, $CuInSe_2$-based solar cell shown improvement after illumination under normal operating conditions. Besides, polycrystalline compound semiconductors have high absorption coefficient due the direct bandgaps.

In this thesis studies, $CuInSe_2$ were chosen as the absorber material for studies. Although the bandgap is 1.04eV, the feasibility of vary the bandgap by altering the material composition with alloy such as Ga or S, may achieve high bandgap of 1.5eV of $CuGaS_2$. Studies shown that by altering the composition, $CuInSe_2$ can either be p-type or n-type, Kermell [14].

1.2 PHOTOVOLTAIC DEVICES

As solar cells, or photovoltaic devices, convert energy from the sunlight into electricity. Power generation part of a solid-state solar cells consist of a semiconductor that forms a rectifying junction either with another semiconductor or with another metal, producing an pn-diode or Schottky diode. However, there are some junctions such as semiconductors-insulators-semiconductors or a metal-insulator-semiconductors junction were form by a thin film placed in between two semiconductors or a semiconductor and a metal. A pn-junction are therefore classified into homojunction and heterojunction according to whether the semiconductor materials on one side of the junction is the

same as or different from that on the other side. Thin film solar cells are typically pn- or pin-diodes.

When the junction is illuminated with applied/external source, the semiconductor material absorbs the incoming photons when the energy (hv) is higher than that of the band gap of the semiconductor, forming an electron-hole pairs. These photogenerated electron hole pairs are separated by the internal electric field of the junction, whereby the electrons drifts to one side remaining the holes at the other side.

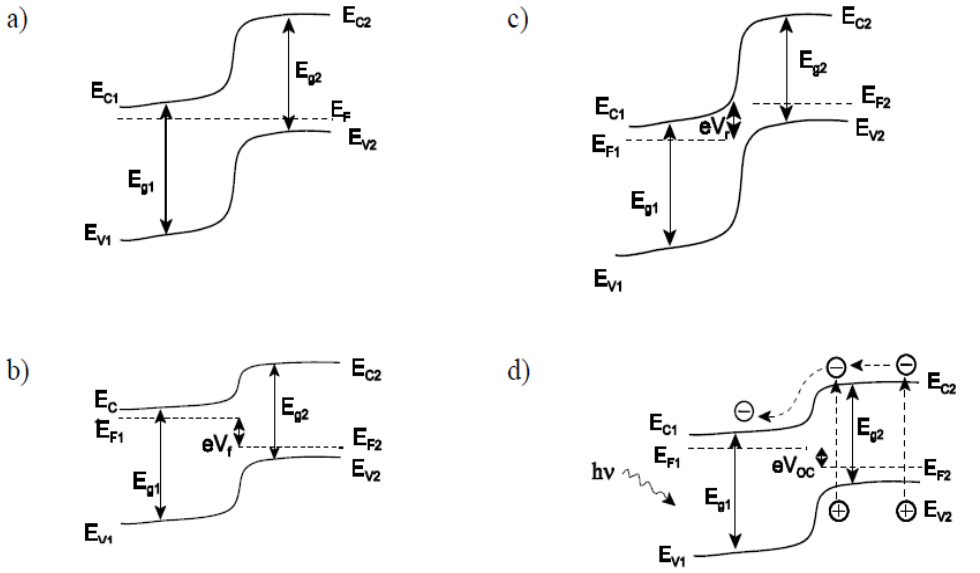


Figure 4: Schematic energy band diagram of a pn-heterojunction solar cell at various condition

The figure above illustrates a schematic energy band diagram of a pn-heterojunction solar cell (a) thermal equilibrium without any illumination, (b) under forward bias, (c) under reverse bias influences, (d) when illuminated open circuit conditions.

1.3 DOPING AND DEGENERACRY OF SEMICONDUCTOR

As mentioned in previous section, being a semiconductor materials, solar cells have weakly bonded electrons occupying a band of energy

called the valence band. In a nutshell, when the energy exceed a certain threshold of the material known, as the bandgap energy, is applied to a valence electron, the bonds are broken and the electron is "free" to move around in a new energy band called the conduction band where it can "conduct" electricity through the material. Therefore these free electrons in the conduction band are separated from the valence band by the bandgap, measured in electron volt (eV). This energy needed to free an electron can be supplied by photons.

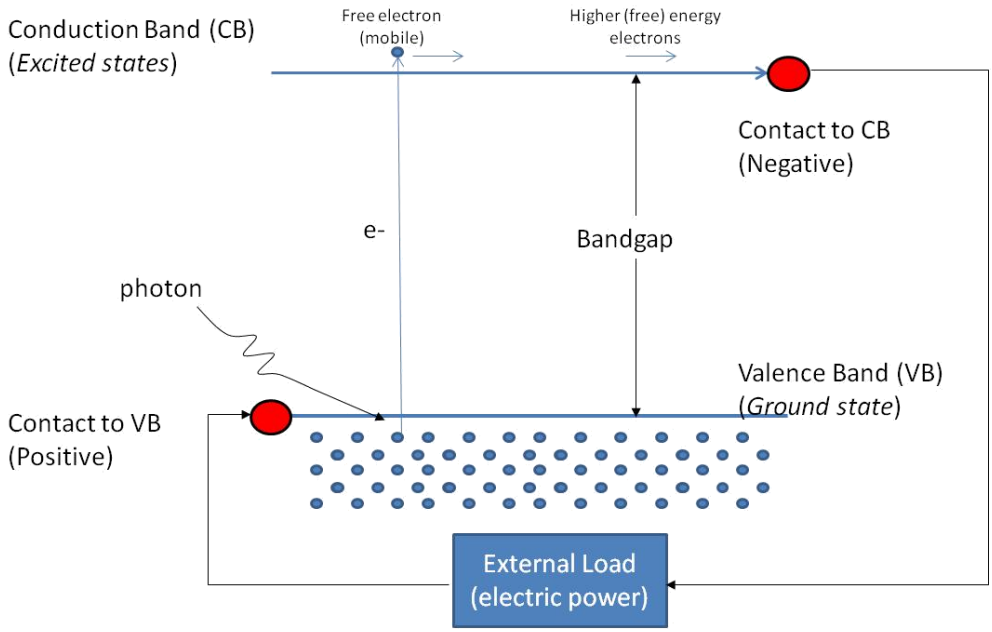


Figure 5: Schematic of solar cell where electrons are pumped by photons from the valence band (VB) to conduction band (CB), and extracted by a contact selective to the conduction band (an n-doped semiconductor) at a higher (free) energy and delivered to an external load, and returned to the valence band at a lower (free) energy by a contact selective to the valance band (a p-type semiconductor).

When a solar cell is exposed to external illumination or an applied field of sufficient energy, the incident solar photon is absorbed by the atoms, breaking the bonds of the valence electrons and pumping them up to higher energy in the conduction band (CB). Excitation of an electron form the valence band (VB) requires a minimum energy of a bandgap of the semiconductor, denotes as the E_g, to the CB. Correspondently, a "hole" is create at the VB. An electron-hole pair is thus created.

At the conduction band, selective contact collects conduction band electrons and drives these freed electrons to an external circuit. The electron loses energy by doing work in the external circuit. They are then restored to the solar cell by returning the loop via a second selective contact, which they return to the valence band with the same energy they had initially started with. The potential at which the electrons are delivered to the external load is less than the threshold energy that excited the electrons i.e. the bandgap (refer to Figure 5).

Sunlight has a spectrum of photons distributed over a range of energy. Photons with energy greater than the bandgap energy can excite electrons from VB to CB and to external load for power generation.

The following section will give a brief introduction on the conductivity of semiconductors as well degeneracy which is similar to the case of solar cell.

The general equation for the conductivity of a semiconductor depends on electron concentration (n) and hole concentration (p), and it can be expressed in the following equation [12]:

$$\sigma = en\mu_e + ep\mu_h$$

Where n and p are electron and hold concentration in CB and VB respectively.

The density of state, denotes as $g_{cb}(E)$, in the CB is the number of states per unit energy per unit volume. The probability of finding an electron in a state with energy E is given by the Fermi-Dirac function $f(E)$.

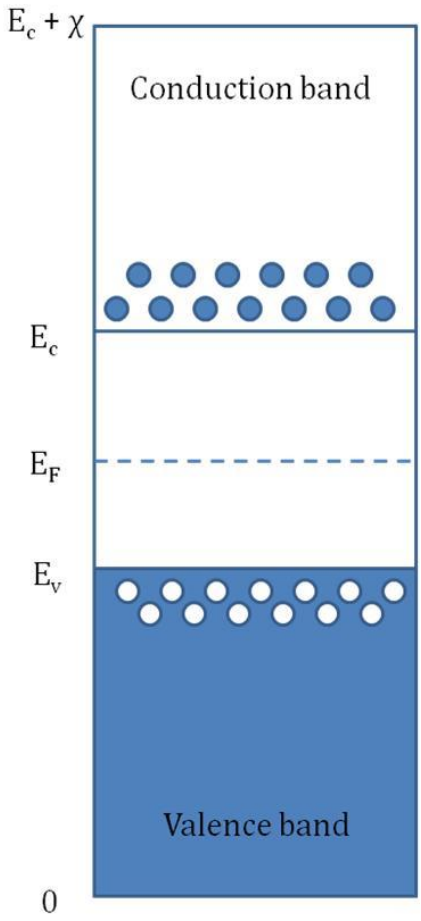


Figure 6: Energy band diagram of electrons and holes at CB and VB respectively.

Therefore, electron concentration in the CB can be expressed in the following equation;

$$n_E\, dE = g_{cb}(E)\, f(E)\, dE$$

$$n = \int_{E_c}^{E_c + \chi} g_{cb}(E)\, f(E)\, dE$$

Where $g_{cb}(E)\, f(E)\, dE$ is the actual number if electrons per unit energy per unit volume $n_E\,(E)$in the CB.

Moreover, replacing the Fermi-Dirac statistic by Boltzmann statistic, and assuming the number of electrons in the CB is less than number of

states in the band. In addition, considering a three dimensional PE well, the electron concentration leads to

$$n = N_c \exp\left[-\frac{(E_c - E_f)}{kT}\right]$$

Where kT is the product of the Boltzmann constant, k, and the temperature, T. N_c is the effective density state at CB edge.

Hence the hole concentration can also be expressed as follows:

$$p = N_v \exp\left[-\frac{(E_f - E_v)}{kT}\right]$$

Where N_v is the effective density of states at VB edge.

Taking the product of both the electron and hole concentration above,

$$np = N_c N_v \exp\left(-\frac{E_g}{kT}\right)$$

Where $E_g = E_c - E_v$.

An intrinsic semiconductor is a pure semiconductor crystal (i.e. no impurities in the crystal) in which the electron and hole concentration are equal. When an electron and hole meets in the crystal, the electrons falls in energy and occupies the empty electronic states that the hole represents, this process is known as "recombine". Recombination of an electron and hole results in their annihilation.

Being an intrinsic semiconductor, n = p, and the intrinsic concentration (denote as n_i) is therefore expressed as the following:

$$np = n_i^2 = N_c N_v \exp\left(-\frac{E_g}{kT}\right)$$

The condition $np = n_i^2$ (also known as the *mass action law*) suggest that electron concentration can be increase in the CB over the intrinsic values, such as addition of impurities into the semiconductor crystal that donates electrons in the CB. This results in a n-type semiconductor where n > p. Similarly, it is feasible to add impurities to remove electrons in the VB such that it yields an p-type semiconductors.

The general band diagrams with the respective Fermi level for intrinsic, n-type and p-type semiconductor are illustrated below:

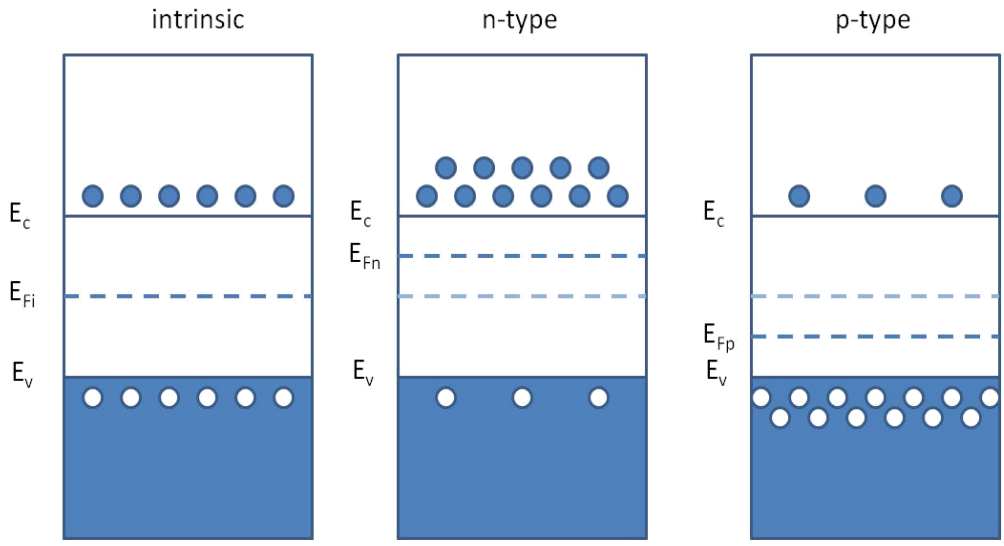


Figure 7: Energy band diagram of intrinsic, n-type and p-type.

Introducing small amount of impurities to an pure semiconductor (e.g. Si) crystal to obtain an semiconductor whereby the concentration of the carriers of one polarity is in excess of the other type as mention above. This type of semiconductor is known as extrinsic semiconductor. The process of introducing impurities is referred as doping. However, in the case of the CIS thin film, doping is not introduced from pure crystal, but the variation of elements within the composition by simultaneous

electrodeposition in a single bath, causes this phenomenon to occur of having different conductivity when varying composition.

From the above electron concentration in CB expression $n = N_c \exp\left[-\frac{(E_c - E_f)}{kT}\right]$ is base on replacing FermiDirac statistic with Boltzmann statistic, is valid when E_c is several kT above E_f. However, Kasap [22] highlighted that Pauli exclusion principle can be neglected and the electron statistic can be describe by Boltzmann statistic, where the n is only valid when $n \ll N_c$. Such semiconductor for which $n \ll N_c$ and $p \ll N_v$ are refer as nondegenerated semiconductor.

Nevertheless, for semiconductors where Pauli Exclusion Principle becomes significant in the electron statistic and Fermi-Dirac statistic is use. The n in $n = N_c \exp\left[-\frac{(E_c - E_f)}{kT}\right]$ is not valid in such a case. Such semiconductors will have $n > N_c$ or $p > N_v$ are refer as degenerated semiconductors. These semiconductors exhibit properties towards metal-like than semiconductor-like. Usually this type of semiconductors occurs at high doping levels which were not the case in CIS thin film. However, for explanatory purpose, a highly doped case is used. For instance, the donor concentration in an n-type semiconductor is increase at sufficiently high doping level, the donor atoms become so close to each other such that the orbital overlaps to form an narrow energy band that overlaps and becomes part of the CB in the n-type semiconductor. Thus the E_c is shifted down and the E_g become narrower. The valence electrons from the donors fill the band from E_c. In such situation is similar to valence electrons filling overlapping energy band in a metal.

In a degenerate n-type semiconductor, the Fermi-level conductor is within the CB or above E_c similar to E_f is within the band of a metal. The majority of the states between E_c and E_f are fill with electrons. This can be illustrated as following:

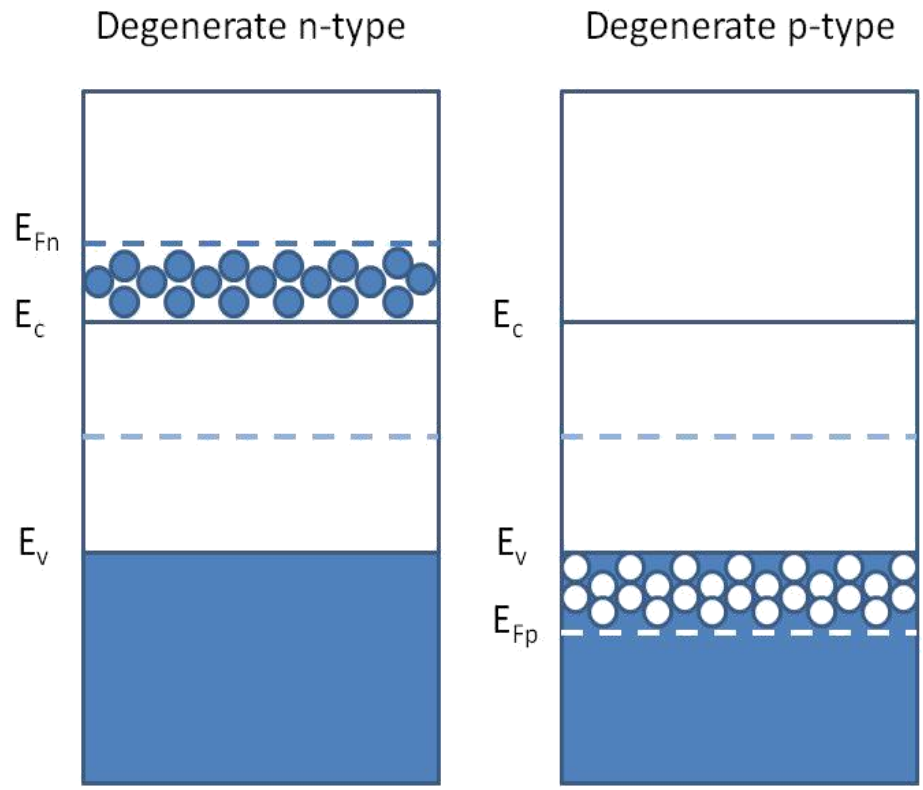


Figure 8: Degenerate n-type(left) and p-type(right) semiconductor.

In case of a p-type degenerate semiconductor, the Fermi level lies in the VB below E_v. In such case of the degeneracy of semiconductor, the mass action law $np = n_i^2$ can no longer be valid.

1.4 ELECTRODEPOSTION OF $CuInSe_2$

There are many methods to obtain thin film of $CuInSe_2$ solar cells. The type of processes use has direct impact on the properties of the thin films. For large scales manufacturing, cost of production may also have an direct impact on which process to chose from. Nevertheless, the underlying objective is to obtain a high efficiency solar cell.

One of the ways to obtain thin film of $CuInSe_2$ solar cells is by sequential processes either by co-evaporation from elemental sources or reactive annealing of precursor films under Se-rich environment. The annealing operation temperature typically above 400°C, which

enhanced the formation of $MoSe_2$ interlayers, but the resultant of high temperature may compensate for the loss of Se. Hence, annealing under Se-rich environment is preferred.

Co-evaporation from elemental sources is likely to yield high efficiency solar cell, and it consist of three stages [13, 22]. This process is commonly use in the market these days for preparation of CIGS film, instead of CIS films. However, this method is does yield high quality CIS or CIGS film in terms of orientation, it is usually applicable to small surface area, which is not feasible for mass production. This may due to the fact that co-evaporation requires very stringent process control to obtain the required composition, texture and electrical properties which is very difficult to achieve for large surface area.

Other methods of sequential processes may also involved process such as chemical vapor deposition, close-spaced vapor transport evaporation of compound sources, spray pyrolysis etc.

Beside the sequential process, electrodeposition involved one-step deposition of CIS-film. This usually involves liquid phase thin film deposition method base electrochemical reactions done by an external applied power. The setup is usually a three-electrode setup which will be introduced in the following section. One of the electrodes is used as a working electrode (cathode) on which the film will be deposited and grown, while the other one function as the counter electrode. The third electrode will be the reference electrode with reference to which the chemical potential of the working electrode is measured. Deposition is carried out at a constant potential (potentiostatically) or at constant current (galvanostatically) but the voltage and/or waveform or pulse can be use.

To achieve a desired film deposition, simultaneous reduction of all the constituent ions in suitable proportions occurring in this one step electrodeposition at the same potential is vital. This can be done by

balancing the diffusion flux of the constituents ions to the cathode, or it can be done by employing the induced co-deposition mechanism. However, this method does not favor large surface area because the flux balance approach is that the concentration and potential ranges for the formation of stoichiometric product are relatively narrow, therefore variation in concentration and potential may results in large changes in film deposition.

The other way of achieving a desirable film deposition, is by inducing co-deposition mechanism. Film composition achieved by co-deposition mainly controlled by thermodynamics. This type of deposition were widely used in CdTe base solar cell and other binary compound semiconductors, which is much less sensitive to the unavoidable variation in the electrolyte composition than processes relying on balancing diffusion fluxes. Moreover, the drop of potential is minimal across large substrate.

Deposition of CIS based thin films were prepared base on flux approach until recent years where induced co-deposition approach has been utilized. Studies of under potential assimilation of indium (In) into films have been observed. This is due to the fact that in one step electrodeposition of CIS is usually performed from solutions where Cu and Se precursor concentrations are of the same order of magnitude, and In is in excess. As such, film stoichiometry is determined by deposition potential and ratio of diffusion fluxes of Se and Cu to the substrate surface.

Flux balance approach is preferred because one the major attributes comes from the formation of Copper-Selenide (Cu-Se) which does not follows the induced co-deposition mechanism. This is so firstly, reduction of Se^{4+} to Se requires large overpotential or actual reduction potential is more negative than the standard reduction potential, and is dependent on the electrode surface. Secondly, the standard reduction potential of Cu^{+} to Cu^{2+} are close to the observed reduction potential of

Se^{4+} and depending on the required Se overpotential, can be either more positive or more negative than that of Se^{4+} ions. As such, independent co-deposition is observed instead of induced co-deposition in the Cu-Se system [14]. In addition, complication may arise from passivation nature of Se deposited at room temperature.

Solutions of the electrodeposition are usually made up from aqueous acidic solution containing Cu ions and In ions in either sulphate or chloride as. Aqueous selenium acid provides Se precursor, sometimes can be obtained from SeO_2 dissolved in slightly acidic solution. Nevertheless, in this thesis purpose, aqueous hydrochloride acid was added to reduce the pH of the solution to facilitate the reduction of $HSeO_3^-$ in acidic environment. In such case, chloride base compound (i.e. indium chloride and Copper chloride) is use to reduce the present of sulphate ions in the makeup solution. In addition, potassium chloride is use as a supporting electrolyte.

Pioneering in CIS deposition were done by Bhattachrya [2], where global simplified electrodeposition reaction were determined as follows:

$$Cu(II) + 2Se(IV) + In(III) + 13e^- \rightarrow CuInSe_2$$

Roussel [18] had investigate the first stage of CIS deposition from acidic solutions on molybdenum (Mo) glass plates and determined that Mo is the best candidate thus far to be tested on back contact in CIS devices. In his investigation, a quasi-instantaneous three dimensional nucleation occurs. First nucleation was made up of Cu-Se phase without indium. Co-deposition of indium then started when Se/Cu ratio reaches close to 1, which confirms what Cu-Se phase is a prerequisite for indium corporation.

The growth begins with very high copper content. The first nuclei are probably copper nanometric nuclei from the reduction of cupric species as follows:

$$Cu^{2+} + 2e^{-} \rightarrow Cu \qquad \text{— (1)}$$

The first copper rich phase allows the incorporation of Se. Although the redox potential of the Se(IV)/Se^0 couple is higher than the redox potential of Cu(II)/Cu^0, the Se(IV) species do not reduce separately on the bare Mo substrate. With the interaction with Cu, the incorporation reaction occurs as follows forming a binary Cu-Se phase.

$$Se(IV) + 2Cu^0 + 4e^{-} \rightarrow Cu_2Se \qquad \text{— (2)}$$

The formation of Cu_2Se shows that Cu is monovolent and at low deposition period, Se is essentially as Se(-II). As the deposition time increases, Se/Cu ratio increases and formation of the Cu-Se phase with x increasing deposition time, can be described as follows:

$$Cu(II) + (1+x)Se(IV) + (6+4x)e^{-} \rightarrow CuSe_{(1+x)} \qquad \text{— (3)}$$

For short deposition time, the Se/Cu is smaller than 2 indicates that the incorporation of Se is controlled by kinetic constrains rather than by diffusion.

Nevertheless, $CuSe_{(1+x)}$ phase may coexist with Cu_2Se and small trace of Se^0.With increasing deposition time, more oxidized form of selenium Se(-II) were formed. When x increases, Se/Cu ratio becomes greater than 1, incorporation of Indium may occur according to the following reaction:

$$CuSe_{(1+x)} + x\ In(III) + 3x\ e^{-} \rightarrow CuIn_xSe_{(1+x)}$$

This reaction agrees that Cu-Se binary phase is a prerequisite for indium assimilation. As the deposition time increases beyond 60 seconds, the layer will coalesced and Se/Cu ratio is close to 2 which correspond to the ratio of diffusion fluxes of Se(IV) and Cu(II).

In a recent study, Roussel [18] mentioned that composition of the evolution in the initial stages and during growth shown a clear difference of substrate reactivity with regards to the reactive ions. Copper is easily incorporated at all stages and Selenium is more passive even when copper is present in the substrate to activate the incorporation.

As selenium accumulates on the extreme surface beyond the diffusion flux ratio shows that elemental Se formation is preferred than Se-rich compound. Therefore, reaction occurs at the surface area exhibit different kinetic parameters similar corrosion phenomena such as selective dissolution of alloys where surface composition is different from bulk.

Chaure *et al* [7] has made structural and electrical properties studies of polycrystalline of $CuInSe_2$ thin film from a one-step electrodeposition form a single electrodeposition bath on fluorine-doped tin oxide (FTO) substrate. Deposition were carried out potentiostatically in an aqueous solution containing 0.002M $CuSO_4$, 0.004M $In_2(SO_4)_3$, and 0.004M H_2SeO_3 with Cu : In : Se ratio of 1:2:2 in the electrolyte. The pH of the bath was maintained between 1.9 and 2.2 using highly-purity H_2SO_4 solution. Bath temperature was maintained between 30°C to 40°C with stirring.

His studies showed that by varying cathodic potential yield different composition of CIS layers, as well as different conductivity determined by PEC. At cathodic potential below 0.6V yields copper-rich CIS layers, and above 0.9V yields indium-rich CIS layers. The conductivity

changes from p- to n- type as deposition cathodic voltage increase from low to high values. Between the two range (i.e. 0.7-0.85v), yields intrinsic CIS materials.

As a result of this study, the ability to obtain the type of conductivity by alter the deposition potential provides new possibilities to of forming ohmic contact of p- and n- type CIS layers.

Phok *et al* [15] has successfully fabricated vertically aligned arrays of $CuInSe_2$ (CIS) nanowires of controllable diameter and length. These were achieved by pulse cathodic electrodeposition from acidic electrolyte solution into anodized aluminum oxide templates. The growth of nanowires is consider to grow into nanoporous anodized alumina oxide template is because of the chemical inertness and periodicity. The template use consists of vertically open channels of amorphous aluminum oxide, which is self assembled into a host of hexagonal lattice using a two step anodization process.

Prior to the formation of the CIS nanowires, nanoporous anodized aluminum oxide template were fabricated. Electrolye solution contains 0.3M of oxalic acid dissolved in deionised water. Anodizations were carried out in a vertical two-electrode cell with platinum as the counter electrode at room temperature. The first step of anodization to produce a less than one micron in thickness aluminum oxide layer, was performed at constant voltage of 20V for 10mins. The oxide layer was then removed in a hot mixture of phosphoric acid and chromic acid for a few seconds.

The second step of anodization was performed at constant voltage ranging from 25V to 40V for less than 30mins. The barrier layer was then removed by ramping down the voltage at 1V/min followed by immersion in 50% phosphoric acid for less than 3mins. After which, a

thermal treatment at 230°C was carried out for several hours to removed the unwanted residuals such as hydroxide.

The CIS nanowires were then electrodeposited in anodized aluminum oxide by pulse plating. The electrolyte contains 1.5mM of copper sulphate hydrate, 2mM indium sulphate hydrate and 3.5mM seleneous acid and lithium chloride, dissolved in 100ml aqueous buffer solution (pH= 2.8) containing potassium hydrogen phthalate and hydrochloride acid. The electrodeposition was carried out in a two electrode cell with a platinum wire as counter electrode.

Before the pulse electrodeposition was administered, a first cathodic deposition was performed at 20V for few seconds to perforate any residual barrier layer. After which, several electrodeposition conditions employing voltage pulses of an amplitude of 1V, pulse width of 1s and a period of 3s were employed. Lastly, the electrodeposited $CuInSe_2$ nanowires were annealed at 220°C in vacuum to improve stoichiometry and crystallinity.

As a result, CIS nanowires array were synthesized, while pulsed potential was used to form CIS inside a nanoporous anodized alumina template of pore size ranging 5-40nm with pore length of 5um.

Valdes *et al* (2011) [21] had had made a recent investigation to addressed the benefits of cyclic pulsed electrodeposition of $CuInSe_2$ thin film on conductive glass. Prior to this study, highly efficient 3-D solar cells have been fabricated infiltrating nanostructure TiO_2 with copper indium sulphides prepared using reactive pulses such as atomic layering deposition (ALD) and chemical vapor deposition (CVD), where such processes are pretty costly and sophiscated. Hence, this study may create future viability of infiltrating nanostructures of TiO_2 with CIS electrodeposition by pulsing potential.

The CIS thin films were deposited on fluorine doped tin oxide (FTO) by cyclic pulse electrodeposition in a single bath configuration. A three electrode cell, with Pt mesh as counter electrode, saturated calomel electrode (SCE) as reference electrode was used. Precursor electrolyte contains 25mmol^{-1} $CuCl_2$, 10mmol^{-1} $InCl_3$, and 5mmol^{-1} SeO_2 with 0.2mol^{-1} KCl as supporting electrolyte. Concentrated HCl were use to adjust the pH between 2.0 – 2.5. Solution is purged with nitrogen to remove oxygen from the electrolyte prior to electrodeposition.

Studies were made with potentiostatic electrodeposition and cyclic pulse electrodeposition. Two potential were used in potentiostatic deposition namely; -0.7V and -0.9V, and time of deposition is 30min. As for cyclic pulse electrodeposition, one pulse consist of applying E_1 (= -0.7V and -0.9V) for 10s and E_2 (= -0.1V) for another 10s. This continues for 90cycles which took about 1800s. After electrodeposition, films were annealed in argon at 500°C for 30mins, and followed by chemical etching with 0.5molL^{-1} of KCN solution for 5mins.

Unlike the studies made by Chaure *et al* [7], Valdes *et al* (2011) [21] manage to obtain p-type conductivity CIS films from the above electrodeposition method.

1.5 DENDRITE GROWTH

Donald *et al*. [1] had defined nucleation as the formation of the first nano-size crystallite from molten material in the context of solidification. Generally, it refers to the initial stage of formation of one phase from another. In this section, discussion of nucleation is taken from solidification perspective but the phenomenon of nucleation is general and associated with phase transformation.

When a material solidifies, the energy associate with the crystalline structure of the solid is less than the energy of the liquid. This energy

difference between the liquid and the solid is the free per unit volume ΔG_v and this is the driving force for solidification.

Once the solid nuclei of a phase forms, growth begins to occur as more atoms becomes more attached to the solid surface. The nature of growth of the solid nuclei depends on how heat is removed during solidification, i.e. to reduce the overall energy. During solidification, two type of heat to be removed, firstly the specific heat of the liquid and secondly the latent heat of fusion. The method to remove the latent heat of fusion determines the material's growth mechanism and final structure of the material.

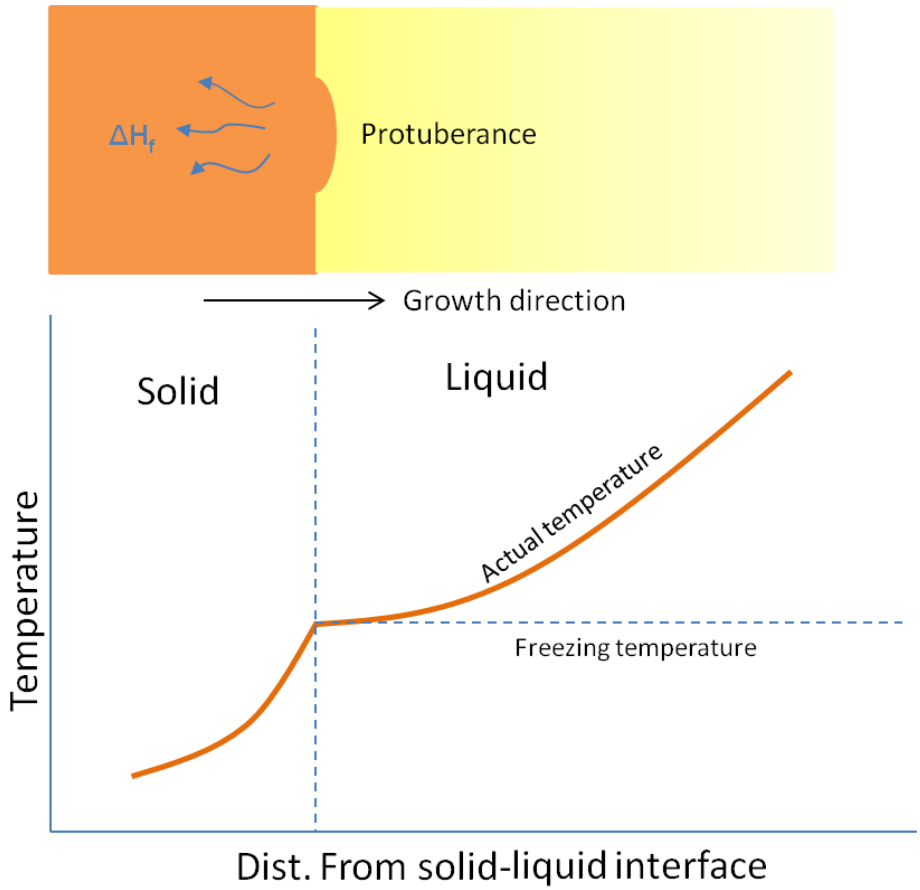


Figure 9 : Temperature of the liquid is above the freezing temperature, protuberance on the solid-liquid interface will not grow leading to a maintenance of a planar interface. Latent heat is removed from the interface through the solid.

A well-inoculate liquid containing nucleating agents cools under equilibrium conditions, heterogeneous nucleation occurs and therefore

under-cooling is not required. Hence the temperature of the liquid at the solid-liquid interface is greater than the freezing temperature. The temperature of the solid is at or below freezing temperature. During solidification, latent heat of fusion is removed by conduction from solid-liquid interface. Any small protuberance that begins to grow on the interface is surrounded by liquid above the freezing temperature as illustrated in the Figure 9. The growth of the protuberance will halt till the remainder of the interface catches up, this mechanism is known as the planar growth, occurs by the movements of a smooth solid-liquid interface into the liquid.

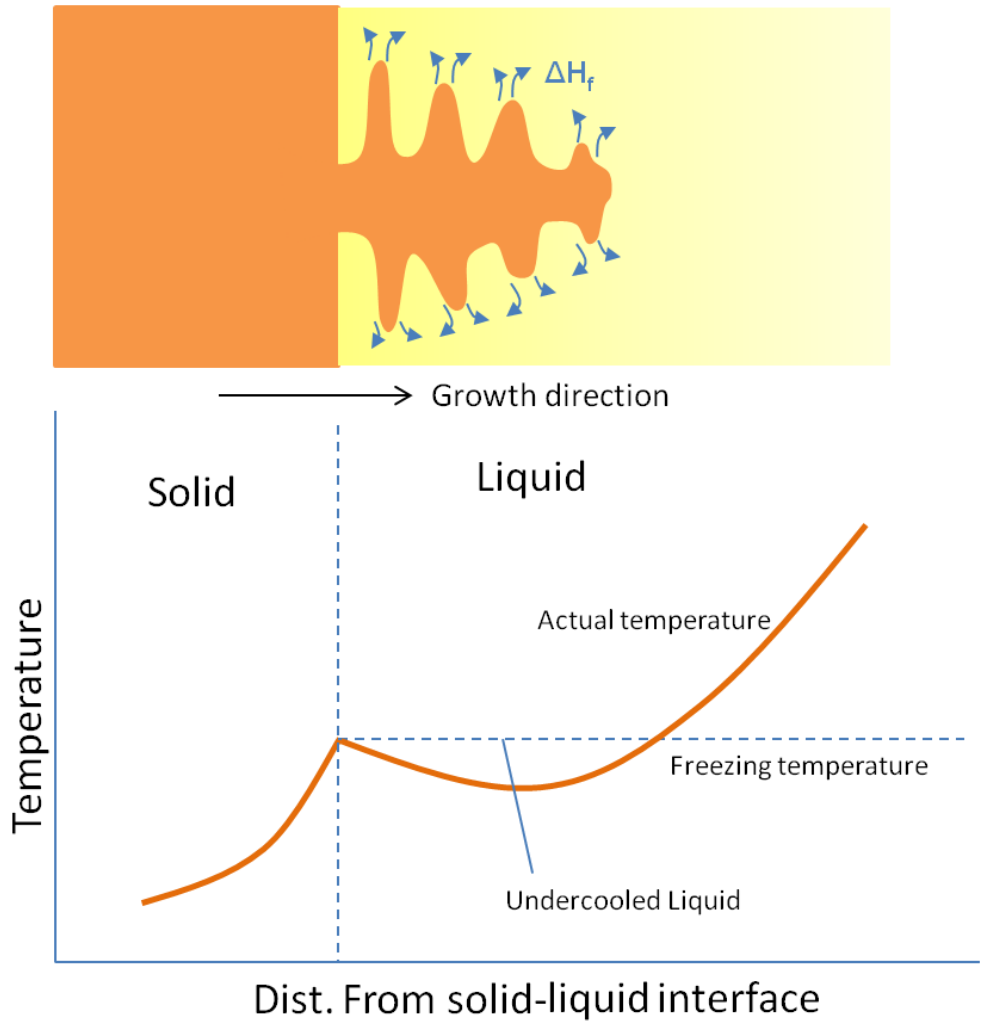


Figure 10 : Liquid is undercooled, a protuberance on the solild-liquid interface can grow rapidly as a dendrite. Latent heat of fusion is removed by raising the temperature of the liquid back to the freezing temperature.

On the other hand, when liquid is not inoculated and nucleation not desirable, under-cooling has to be carried out before the solid forms. In

such condition, the small solid protuberance that forms at the interface is known as the dendrites shown in Figure 10. These dendrites are favored in growth since the liquid before the solid-liquid interface is undercooled. As the dendrite grows, the latent heat of fusion is conducted into the undercooled liquid, raising the temperature of the liquid towards the freezing temperature. Secondary and tertiary dendrite arms can also form on the primary stalks to speed up the evolution of the latent heat. Dendritic growth continues until the undercooled liquid "warms" up to the freezing temperature. Remaining liquid shall then solidifies by planar growth. The difference between planar growth and dendritic growth arises because the different sinks for latent heat of fusion. In pure metals, dendritic growth can be represent only a small fraction of the total growth as follows:

$$Dendritic\ fraction\ = f = \frac{c\Delta T}{\Delta H_f}$$

Where c is the specific heat of the liquid. Numerator $c\Delta T$ represents the heat that the undercooled liquid can absorb, and the latent heat in the denominator ΔH_f represents the total heat that must be given up during solidification. As undercooling ΔT increases, more dendritic growth will occur. If the liquid is well inoculated, undercooling is almost zero, growth would generally be via planar front solidification mechanism.

1.6 ANNEALING OF COMPOUNDING PRECUROSOR

Electrodeposition of all elements simultaneously requires minutes of adjustment of concentration in the solution and the application of complexing agent. Hence, annealing at high temperature is inevitable in many processes due to the fact that the precursor film is not in its thermodynamic stable state in reaction step. This annealing of precursor compound is a re-crystallization process that completes with the deposition of the compound. Hence, optimization of the reaction

step is difficult. For instance, cells with good efficiencies were obtained by a hybrid process combining electrodeposition of a Cu-rich $CuInSe_2$ films and subsequently conditioning by a vacuum evaporation step of In(Se),with annealing of films at elevated temperature is a suitable atmosphere is vital.

During the post treatment annealing, polycrystalline precursor expects certain grain growth. The precursor materials, being polycrystalline, contain large numbers of grain boundaries, which represent a high-energy area according to Donald *et al*. [1] because of inefficient packing of atoms. To achieve a lower overall energy of the materials, the grain boundaries have to be reduced by grain growth. This grain growth involves the movements of grain boundaries, allowing larger grains to grow in the expense of smaller grains, which can be illustrated in the following simulated model of a single phase grain.

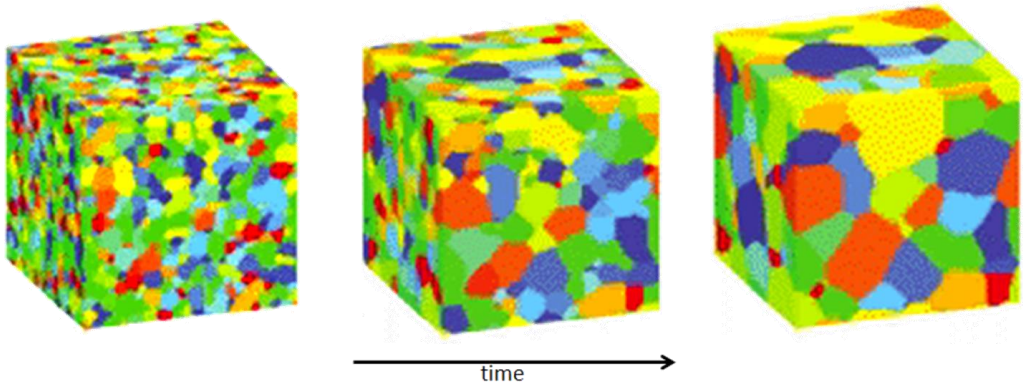


Figure 11: Model simulation of isotropic, single-phase grain growth in a polycrystalline material. Color corresponds to the site indices. Over time, average grain size increases as large grains grow at the expense of small grains.

Figure 11 above shows grain growth occurs as atoms diffuse across the grain boundary from one grain to another. For grain growth in the material, diffusion of atoms across the grain boundary is required, and as a result, the growth of the grains is related to the activation energy need for an atom to "jump" across the boundary. Therefore the driving force for grain growth is the reduction of grain boundaries, which are

defects. The presences of these grain boundaries cause the increase of free energy of the material. Hence the thermodynamic tendency is to drive the polycrystalline materials, in the case the precursor thin film, to increase the average grain size which can be achieved by applying external heat or lowering the activation energy.

Atoms or ions may possess thermal energy will move from a normal crystal structure location to occupy a nearby vacancy caused by an imperfection within the crystal structure, thus the atoms may "jump" across the grain boundary causing the grain boundary to move. The ability for an atom or ion to move or diffuse increase as temperature or thermal energy gain increases. This rate of diffusion is related by Arrhenius equations:

$$Rate = c_o \exp\left(\frac{-Q}{RT}\right)$$

Where c_o is a constant, R is the gas constant, T is the absolute temperature (K) and Q is the activation energy required to cause an Avogadro's number of atoms or ions to move.

Crystalline materials generally contains defects also known as vacancies , and the disorder of these vacancies creation increase in entropy, is able to minimize free energy therefore thermodynamically stabilize the crystalline material. In such materials, the atoms moves from one lattice position to another lattice position known as the self-diffusion. Nevertheless, self diffusion effect is generally not significant. Hence, by increasing the thermal energy, diffusion can be carried out by vacancy diffusion and interstitial diffusion.

In vacancy diffusion, the atom leaves a regular lattice position and fills a vacancy in the crystal, as such creates a new vacancy and process continues. However interstitial diffusion occurs when a small interstitial atom or ion is present in the crystal structure, the atom or ion moves

from one interstitial site to another interstitial site. Such diffusion does not require a prerequisite of available vacancy, and usually occurs much easier than vacancy diffusion.

The rate of diffusion at which atoms, ions, particles, and other species in a material can be measured by the flux (J), defines as the number of atoms passing through a plane of unit area per unit time. This can be summaries in Fick's first law as shown below:

$$J = -D\frac{dc}{dx}$$

Where J is the flux, D is the diffusivity and $\frac{dc}{dx}$ is the concentration gradient. The negative sign suggest that the flux diffused from a region of higher concentration to a lower concentration. At microscopic scale the thermodynamic driving force for diffusion is concentration gradient, hence the net flux is created depending on temperature and concentration gradient.

The flux at a particular temperature is constant if the concentration gradient is also constant. However, this case is it is assume a steady state diffusion. Generally, in practical situation, a non-steady state diffusion has to be considered with the Fick's second law.

$$\frac{\partial c}{\partial t} = \frac{\partial}{\partial x}\left(D\frac{\partial c}{\partial x}\right)$$

Assuming the diffusion coefficient D is not a function of location x and the concentration c of diffusion species, Fick's second law can be simplified as follows:

$$\frac{\partial c}{\partial t} = D\left(\frac{\partial^2 c}{\partial x^2}\right)$$

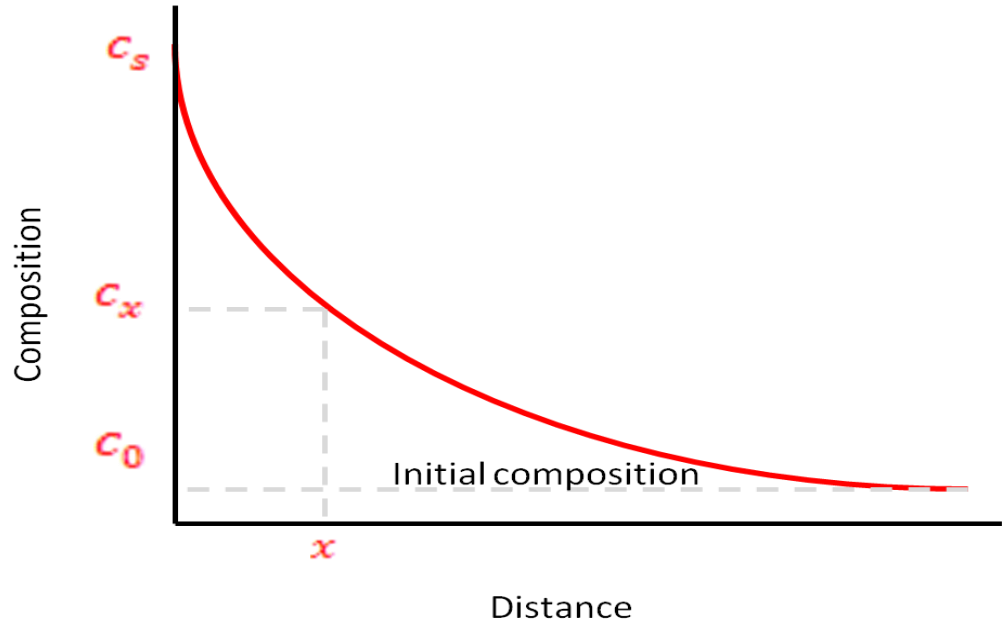


Figure 12 : Illustration of Fick's second law on the diffusion of atom into the surface of a material.

Considering the boundary conditions for a particular solution as illustrated in the above Figure 12, the solution can be written as follows:

$$\frac{c_s - c_x}{c_s - c_0} = \text{erf}\left(\frac{x}{2\sqrt{Dt}}\right)$$

Where c_s is a constant concentration of the diffusion atom t the surface of the material, c_0 is the initial uniform concentration of the diffusing atom in the material, and c_x is the of the diffusing atom at the location x below the surface after time t. This equation assumes the atoms or other diffusing species are moving in a single direction x. The function erf is the error function which mathematical definition is

$$erf(x) = \frac{2}{\sqrt{\pi}} \int_0^x exp(-y^2)\, dy$$

Where y is the argument of the error function, which also defines a complementary error function as follows :

$$erfc(x) = 1 - \mathrm{erf}(x)$$

The above provides a brief discussion on diffusion and grain growth, driven by the reduction of grain boundary.

1.7 BACK CONTACT – Mo

Mo is widely used contact materials for base electrode in A^{I}-B^{III}-C^{VI}_2 compound type thin film solar cells [19] because of its comparatively low cost, high melting A^{I}-B^{III}-C^{VI}_2 point of about 2700°C and expected low diffusitivity in the semiconductor films. Polycrystalline Mo films are usually sputtered at room temperature or electron beam evaporated onto glass substrate at about 300°C, however in this thesis will be on Silicon wafer substrate. The resistivity of Mo increase with oxygen incorporation from the residual gas atmosphere and with increasing tensile stress in the film. These tensile stress adhere to the substrate better [20].

One on the main advantage molybdenum is that the reactivity of Mo with selenium or sulphur is relatively small. However, at high substrate temperature of about 500°C, a $MoSe_2$ film or MoS_2 film forms before or during the growth of chalcopyrite film. Therefore, MoX_2 (X=Se or S) can form at the Mo/Chalcopyrite interface and/or on top of the Mo layer before formation of chalcopyrite by exposing to chalcopyrite vapour.

This MoX_2 (where X=Se or S) are layered semiconductors with an indirect bandgap of 1.06-1.16eV and 1.17-1.35eV respectively. Roland et al [19] reported that if MoX_2 films were oriented is such that the c-axis is perpendicular to the substrate, where it shows weak van der waals bonding, the layer may impede the adhesion of the chalcopyrite absorber. However, it has shown that parallel orientation appeared to be the preferred orientation for MoX_2 growth at the Mo/chalcopyrite interface which perpendicular orientation is preferred only at surface

controlled Mo chalcogenisation. Both processes may contribute to the MoX_2 film thickness which the growth rate of c axis parallel is higher. In the parallel c axis configuration, diffusion of metal ions into the van fer waals planes of $MoSe_2$ could lead to a chemical intermixing at $MoSe_2$/ A^{I}-B^{III}-C^{VI}_2 interface and induce the observed ohmic contact characteristic. In William N. (2011) [19] studies, it was reported that Ga diffusion into Mo layer is and diffusion of Cu, In and Se. The thickness of $MoSe_2$ layer increases with increasing substrate temperature. It also decreases with increasing O content in the Mo layer.

The optical reflection of Mo in the wavelength ranges of 500-600nm is only 60% tested alternative back contacts with the aim of improving the back contact reflectivity. Chromium (Cr), Vanadium (V), Titanium (Ti) and Manganese (Mn) has been rule out due to strong reactivity with Selenium. However, the use of Tantalum (Ta) and Niobidium (Nb) leads to good device quality. Unlike molybedeum (Mo) and Tungseten (W), it was found that Ta and Nb back contact needs a Galium (Ga) back surface gradient for high open circuit voltage V_{oc} [19] (i.e. the voltage the cell develops at zero load), probably due to the inferior properties of the selenium formed.

2. EXPERIMENTAL DETAILS

2.1 SUBSTRATE PREPARATION

Two types of substrates were used for this study. The initial study of CIS plating used Mo-strips. These Mo strips were obtained from a 2mm thick Mo metal sheet cut into small coupons of 1 x 2 cm. Being easily oxidized, the surface of the Mo strips were lightly polished with silicon carbide paper grid 600 before the start of the experiment to ensure that the CIS plated on the Mo surface.

The second type of substrate was obtained from Mo sputtered on an 8-inch Silicon wafer by physical vapour deposition (PVD). The Mo deposited by pulsed DC sputtering at a pressure of about 1.5mTorr. The molybdenum thickness is about 200nm. Thickness of the molybdenum on Si wafer was inspected by FESEM cross sectioning instead of using a surface profiler. The samples were then cleaved by a diamond scriber to obtained approximately 1cm by 2cm, adhered to the copper wire contacts by silver paint protected by a layer coat of fast cured two-part epoxy. Before the start of the electrochemical deposition, the Mo substrates were cleaned in 25% ammonia for 5mins and rinsed with high purity water as per Chassing *et al* [6].

2.2 DEPOSITION OF CIS THIN FILMS

The solutions were prepared from analyital grade purity high purity water of at least 18.2MΩ by Millipore Elix Progard 2 5UV. Copper Indium Diselenide solution was made-up of aqueous 0.002M Cu_2SO_4, 0.004M $InCl_3$ and 0.004M H_2SeO_3, having a ratio of 1:2:2 in the electrolyte. If an off-white precipitation occurred after mixing the four solutions this was resolved by adjusting to pH 2 with aqueous 37% hydrochloride acid [18].

Electrodeposition of CIS thin film was carried out using ACM instruments Field Machine DSP. The setup is a three-electrode electrochemical cell consisting of a Saturated Calomel Electrode (SCE) ($Hg/HgCl_2/KCl$) as the reference electrode, Mo substrate (either Mo-strip or Mo-wafer) as the working electrode (Cathode) and graphite rod as the counter electrode (anode) as illustrated in Figure 13. All the potentials in this thesis are quoted versus the SCE system.

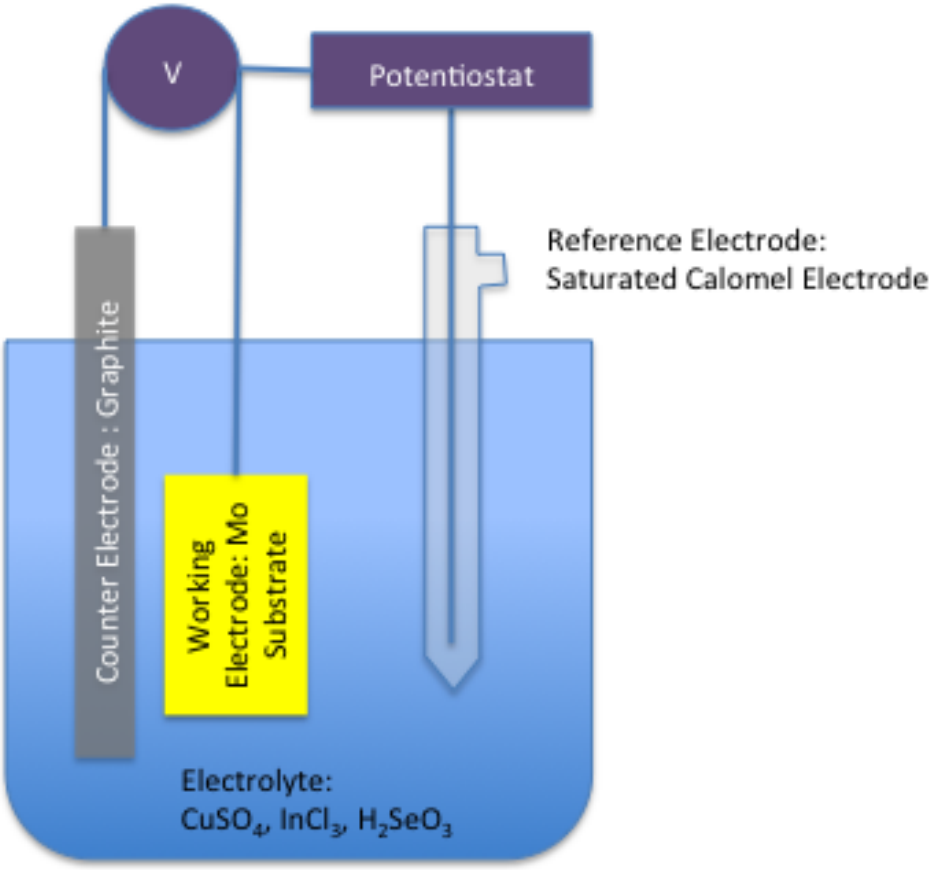


Figure 13: Electrodeposition setup

Three types of deposition were made. First DC deposition was performed at room temperature with both Mo-strip and Mo-wafer coupons. The second type of deposition was made with pulse deposition at room temperature employing a pulse width of 1 second (t_c) and period of 2 seconds rest (t_r) [15] with the voltage ranging from -0.3V to -1.3V.as illustrated in Figure 14. The third type of deposition

used the same pulse plating profile as type two deposition, but the solution was heated to 40°C.

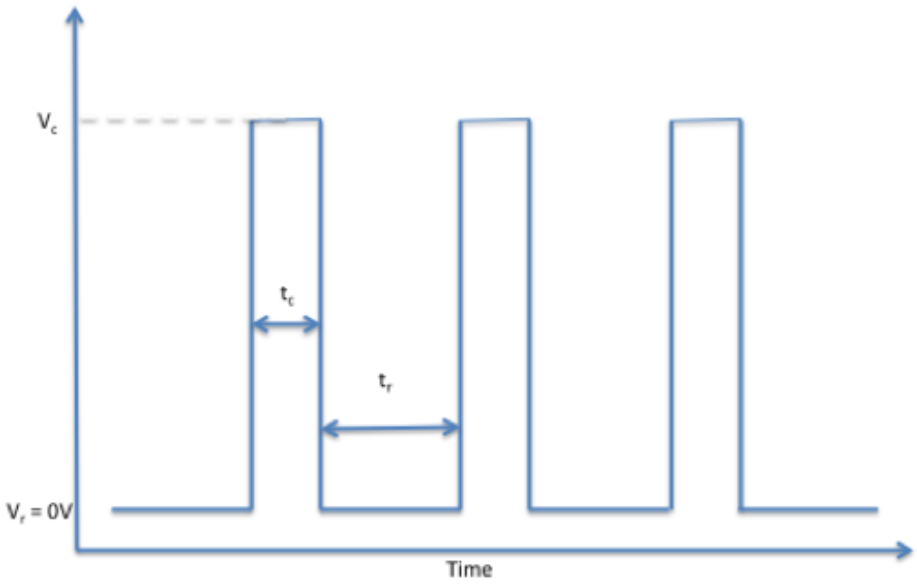


Figure 14: Voltage-time profile of pulse deposition of CIS thin film. V_c ranging for -0.3V to -1.3V, whereas t_r = 2 second and t_c = 1 second.

2.3 POST TREATMENT

The CIS thin films were subjected to post treatments to enhance the crystallinity of the CIS thin films at the Mo-CIS interface and to remove unwanted phases typically Cu_xSe_{1-x}. Phok *et al.* [15] have shown that annealing improves the adhesion between Mo-CIS interfaces by forming a more stable CIS thin film, as opposed to a Cu_xSe_{1-x} layer, at the Mo surface. This can be achieved by first annealing the samples at 450°C for 30mins in a vacuum environment to prevent oxidation from occurring by vacuum tube furnace and allow at least 4 hours to cool down to room temperature. These were followed by an etching of 5wt% KCN for a period of 5min in ultrasonic. The samples were then rinsed with high purify water and air dry. This etching step removes the excess Cu and Se compounds.

2.4 ELEMENTAL ANALYSIS BY ENERGY DISPERSIVE X-RAY (EDX) SPECTROCOPY

The CIS thin film composition were analyzed by energy dispersive x-ray (EDX) using Oxford instruments Inc. Solid Drift detector (SDD) X-Max 80 with 80mm^2 active window run on Aztec software, and 10mm^2 convention EDX detector on Inca software. A working distance of 10mm and an acceleration voltage of 15kV were used to sufficiently cover all three elements (Cu, In and Se) for studies up to the k-alpha lines.

Qualitatively, results were normalized to and fixed to only quantify the above 3 elements for studies. This is because with high acceleration voltage, the interaction volume penetrates deeper thus Molybdenum (Mo) and Silicon (Si) were also detected.

The advantage of Aztec software is that the processing time and dead count were controlled by software, thus sufficient counts were collected. With 80mm^2 active window, the processing time is greatly reduced. No overlapping of peaks is suspected during the analysis by Aztec software, thus wavelength dispersive x-ray spectroscopy (WDS) is not required. Copper quantimization were performed on copper tape before the start of the test to ensure the quantitative results were optimized on convention 10mm^2 active window. All samples CIS thin films were analyzed after electrodeposition.

2.5 SURFACE MORPHOLOGY EVALUATION BY SCANNING ELECTRON MICROSCOPY (SEM)

The CIS thin films surface morphologies were studied by means of Field Emission Gun Scanning Electron Microscopy (FESEM) using Zeiss Supra 25 and JEOL JSM 7800 FESEM. Secondary electron mode is use to give sufficient resolution, however, because the initial

characterization of EDX requires a high acceleration voltage of 15kV, the surface topography is compensated. Nevertheless, both Zeiss and JEOL has lower electron detector (LEI or InLens), these detector would improve the topography of the surface as the detector has the ability to collect lower energy secondary electrons at the surface. Since samples are generally conductive and EDX is required in the earlier studies, no sputtering metallization (Pt/Au) were needed even micrographs shows slight charging effect on the bigger grains and dendrites. Thin films surface were taken after electrodeposition. Both surface profile and cross-section views were studied.

2.6 PHASE ANALYSIS BY X-RAY DIFFRACTOMETER (XRD)

To identify the phases present as well as the crystal structure of the CIS films, X-ray Diffraction spectroscopy was performed. All three types of substrates were examined both after electrodeposition and after post treatments. Although only the Mo strip substrate had XRD performed after annealing treatment. The XRD was carried out by Bruker's D8 Advance and DIFFRAC.SUITE software, incidental angle starting from 20° to 80° with 0.1 diffraction silt.

2.7 ELECTRICAL CONDUCTIVITY BY PHOTOELECTRO-CHEMICAL (PEC)

Photoelectrochemical measurements allow a simple and fast characterization of the semiconducting properties of the film. The current-voltage characteristic of an illuminated semiconductor electrode in the contact with the redox electrolyte can be obtained easily by adding together the majority and minority current components [16].

Usually the working electrode is illuminated during measurement. Both polychromatic illumination (white light) and monochromatic illumination

can be use as long the energy of the light is higher than that of the energy bandgap of the semiconductor. If the film is photoactive, photocurrent or photovoltage will be detected i.e. when the current is higher under illumination than in the dark. The direction of the photocurrent or photovoltage gives the information of the conductivity type of the film whether it is p-, i- or n- type.

When a semiconductor is immersed in a solution, an electric field develops at the solid/liquid interface via charge transfer reactions between the two phases. The electric field enables the separation of charge carriers, analogously to a pn-junction or a Schottky junction. Illumination on the semiconductor cause an increase of the concentration of minority carriers such as electrons in a p-type semiconductor. The electric field drives the photogenerated minority carriers towards the semiconductor/liquid interface where they participate in electrochemical reactions in the solution with suitable redox species. Therefore a p-type semiconductor is capable of reducing more species under illumination than in the dark, resulting in an increase of cathodic current while the anodic current remains unaffected. An n-type semiconductor behaves likewise, where the anodic current increases under illumination than in the dark. PEC measurements provides information about the film properties after deposition.

Usually this type of experiment is carried out in an electrolyte solution containing redox species. The potential of which is in a suitable position with respect to the band edges of the semiconductor so that charge transfer reaction between the semiconductor and solution are possible. Nevertheless, band edge positions of CIS are dependent on the electrolyte and on the surface chemistry of the film [13]. In this project, the measurements were performed in aqueous 0.01M $CuSO_4$ electrolyte solution and the photovoltage shifts were recorded with respect to Saturated Calomel Electrode (SCE) ($Hg/HgCl2/KCl_{(sat)}$) as the reference electrode connected to a high impedance voltmeter.

In the dark the CIS films form a Schotty barrier with the 0.1 M $CuSO_4$ electrolyte, which is similar to the "Metal-semiconductor junction" shown in the Figure 15. For instant a n-type semiconductor of work function Φn and metal of work function Φm, such that Φm < Φp.

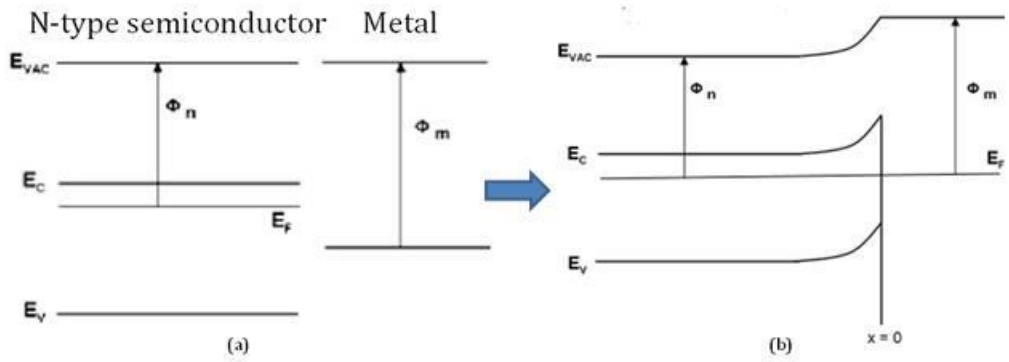


Figure 15: n-type semiconductor and metal (a) in isolation (b) semiconductor –metal junction in equilibrium.

When the metal and semiconductor are separated from each other, the Fermi levels will look like those in Figure 15(a). When both are in electronic contact, the Fermi levels will line up as shown in Figure 15(b). This is achieved by the exchange of charge carriers across the junction, with the consequence that the layers approached equilibrium. The energy at the conduction band edge at the interface between semiconductor and metal is higher than in the bulk of the semiconductor.

Upon illuminating with a 300 W Xenon lamp (Oriel Instruments) photons with energy greater than bandgap (E_g) are absorbed by the semiconductor resulting in electron-hole pair generation. This causes electrons to be accumulated at the semiconductor side and holes in the metal side of the depletion region. The separation of the electrons and holes causes an electric field that opposes the initial field creating a photovoltage V_{photo}, equal to the difference in the Fermi levels of semiconductor and metal far from the junction as shown in Figure 16.

In the case of a semiconductor electrolyte junction the metal's Fermi level is replaced by the redox potential of the solution.

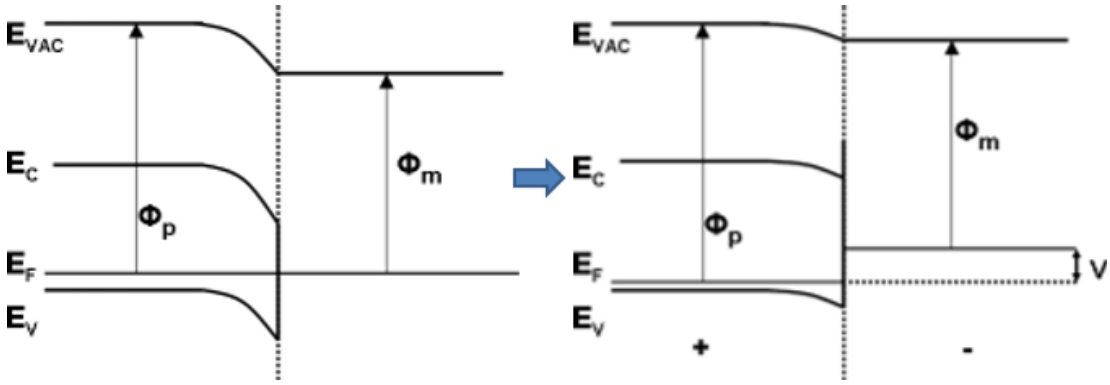


Figure 16: Band profiles for the p-type semiconductor-metal junction under illumination.

The polarity type of solid/liquid junction the CIS film deposited can thus be obtained when photovoltage is measure before and after illumination. That is an p-type semiconductor results in a positive photovoltage and a n-type a negative one. This study was done on DC plating and Pulse/heated Pulse plating on Mo-wafer substrates instead of Mo-strip substrates.

3. RESULTS & DISCUSSION

3.1 ELEMENTAL ANALYSIS BY ENERGY DISPERSIVE X-RAY (EDX) SPECTROCOPY

Table 1 to Table 4 tabulate the elemental compositions, as determined by EDX, of the CIS films as plated by the various plating processes on the two different substrates at different deposition potentials ranging from -0.3V to -1.3V with respect to SCE.

a) DC plating on Mo-strip
b) DC plating on Mo-wafer
c) Pulse plating on Mo-wafer
d) Pulse plating on Mo-wafer at 40°C

Table 1: Summary of EDX elemental results on the CIS films deposited on Mo-strip at room temperature by DC plating.

DC plating on Mo strip			
Cathodic Potential with respect to SCE	Composition (atomic %)		
	Cu	In	Se
Theoretical Values	25.0	25.0	50.0
-0.30	21.2	22.3	56.5
-0.70	19.0	37.6	43.5
-0.90	19.1	49.6	31.2
-1.10	19.9	44.7	35.4
-1.30	11.5	70.6	17.8

Table 2: Summary of EDX elemental results on the CIS films deposited on Mo wafer at room temperature by DC plating.

DC on Mo wafer			
Cathodic Potential with respect to SCE	Composition (atomic %)		
	Cu	In	Se
Theoretical Values	25.0	25.0	50.0
-0.30	28.4	11.9	59.7
-0.70	24.4	27.0	48.6
-0.90	24.6	28.4	47.0
-1.10	23.2	32.1	44.7
-1.30	24.9	27.9	47.2

Table 3: Summary of EDX elemental results on the CIS films deposited on Mo wafer at room temperature with pulse plating.

Pulse plating on Mo wafer at room temperature			
Cathodic Potential with respect to SCE	Composition (atomic %)		
	Cu	In	Se
Theoretical Values	25.0	25.0	50.0
-0.30	27.1	7.7	65.2
-0.70	27.7	19.6	52.6
-0.90	21.0	26.0	52.9
-1.10	22.1	29.1	48.8
-1.30	24.2	26.0	49.8

Table 4: Summary of EDX elemental results on the CIS films deposited on Mo wafer 40°Cwith pulse plating.

Pulse plating on Mo wafer at 40°C			
Cathodic Potential with respect to SCE	Composition (atomic %)		
	Cu	In	Se
Theoretical Values	25.0	25.0	50.0
-0.30	27.1	7.7	65.2
-0.70	27.7	19.6	52.6
-0.90	21.0	26.0	52.9
-1.10	22.1	29.1	48.8
-1.30	24.2	26.0	49.8

From Table 1 it can be seen that the DC plating on Mo-strip elemental composition differ considerably from the theoretical values of Cu:In:Se of 25:25:50, whereas the other tables show that CIS plated on Mo-wafer have a lower deviation especially for the potential range from -0.9V to -1.3V.

The copper composition in Mo-wafer by DC plating, pulse plating and heated pulse plating are relatively close to the 25% theoretical value, except for the -0.3V by pulse plating. In this later case the potential was too positive for sufficient indium to plate, thus the atomic percentage overall increased in both Cu and Se. Films deposited onto the Mo strips tended to be copper deficient.

The percentage of indium in the films generally had an increasing trend as the deposition voltage becomes more negative, while Se decrease, consistent with the more negative standard deposition potential of In compared to Se and Cu. This is most clearly seen in the DC plating on Mo-strip as the deposition potential was made more negative from -0.3 to -1.3, Se percentage fall from 56.5 to 17.8 in atomic concentration.

To provide a better correlation between the results, graphical presentations of the relationship between the composition (as atomic %) and deposition potentials of the deposited CIS thin films are shown in Figure 17 to Figure 20.

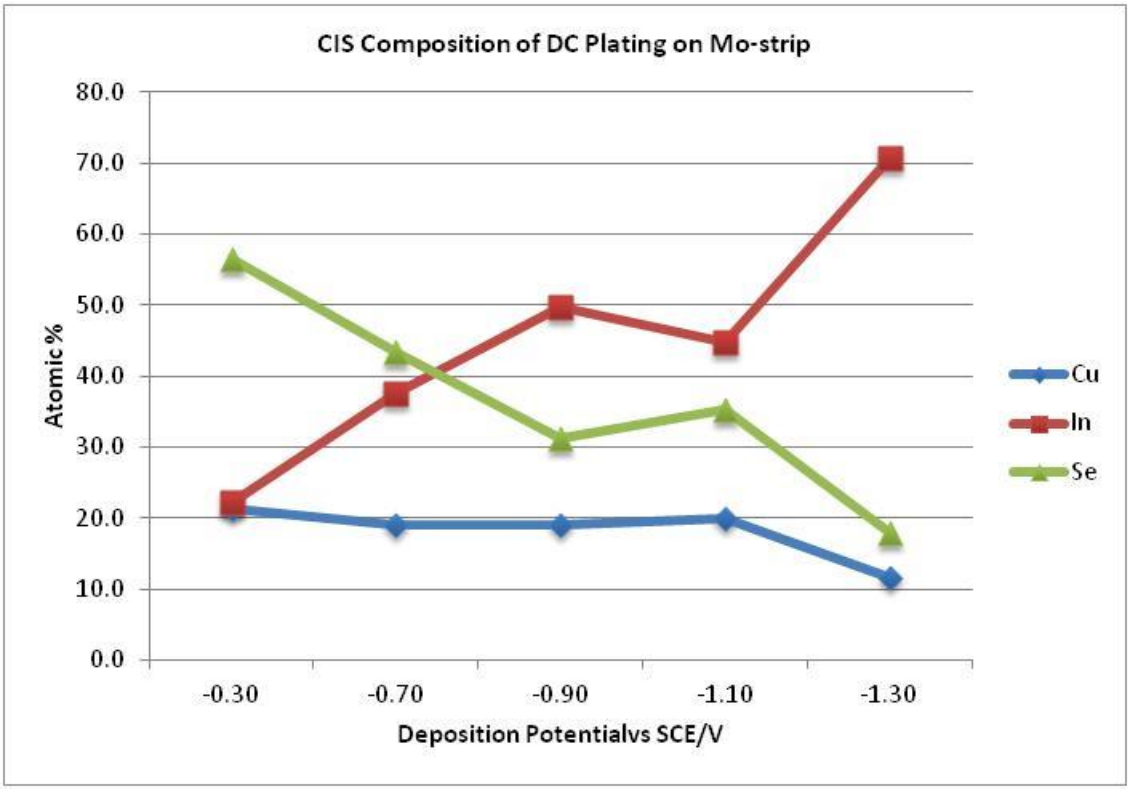


Figure 17: Composition of DC electrodeposition of CIS thin on Mo-strip at room temperature as a function of deposition potential as determined by EDX.

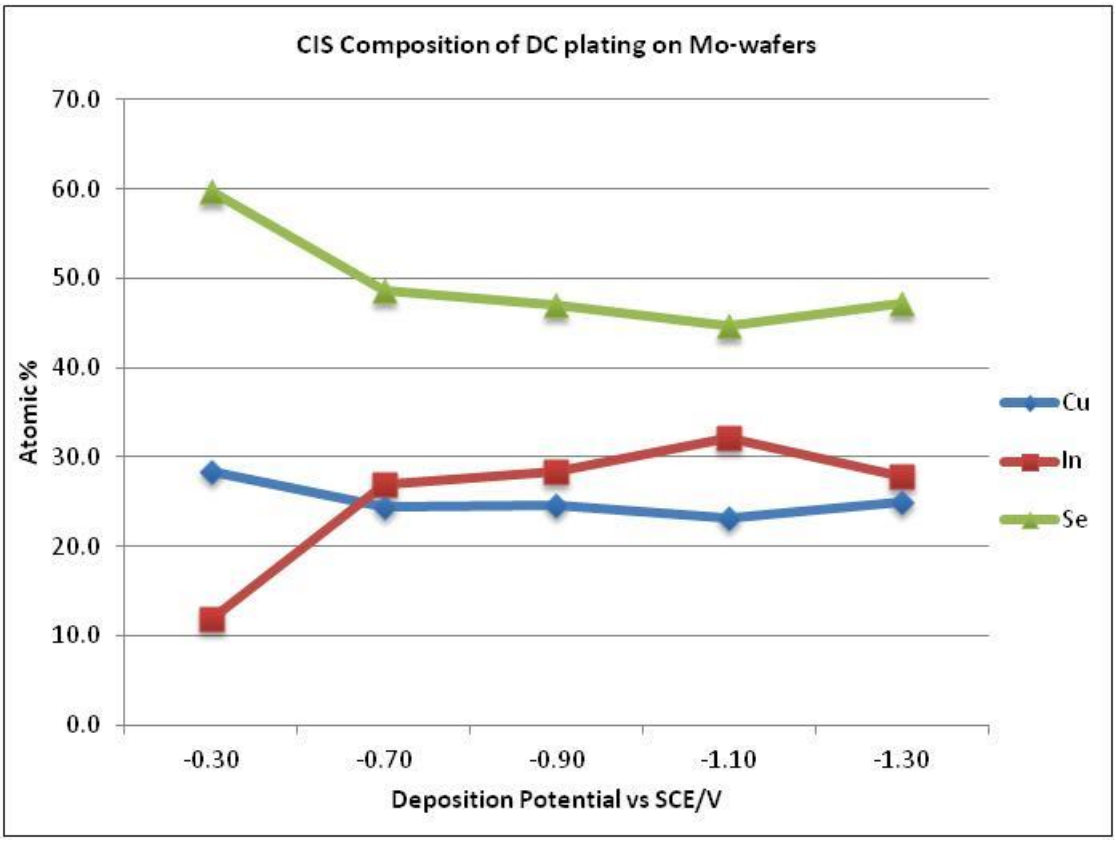


Figure 18: Composition of DC electrodeposition of CIS thin on Mo-wafer at room temperature as a function of deposition potential as determined by EDX.

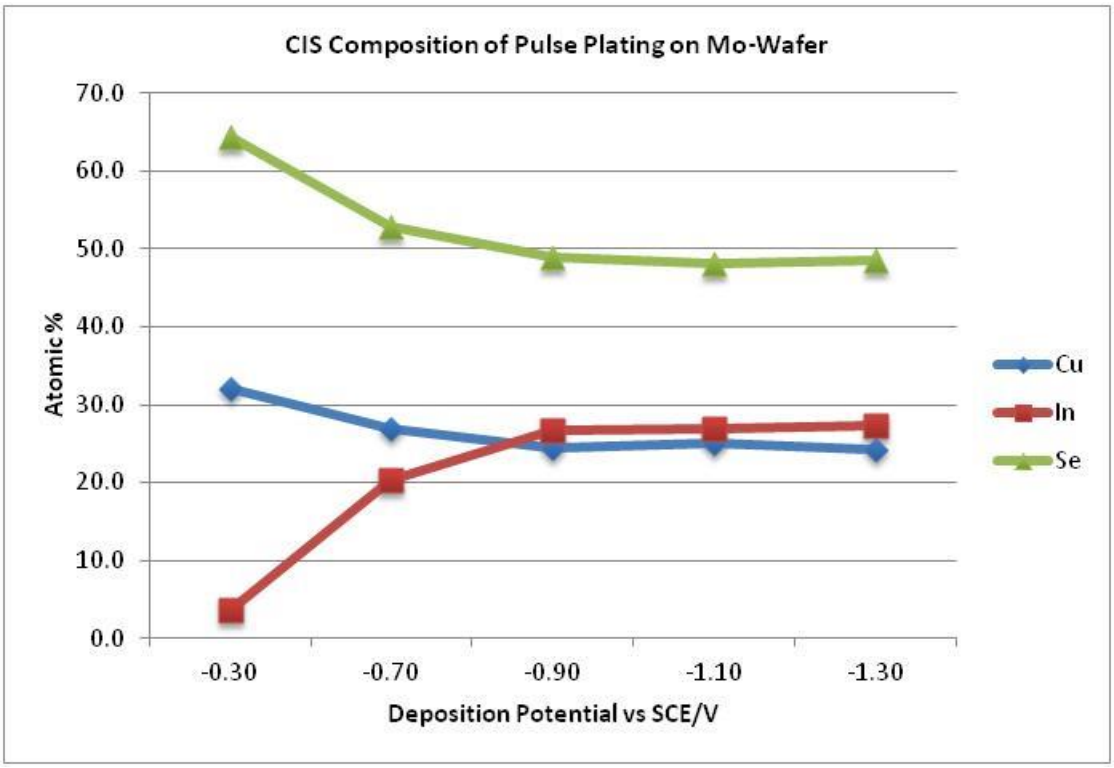


Figure 19: Composition of Pulse electrodeposition of CIS thin on Mo-wafer at room temperature as a function of deposition potential as determined by EDX.

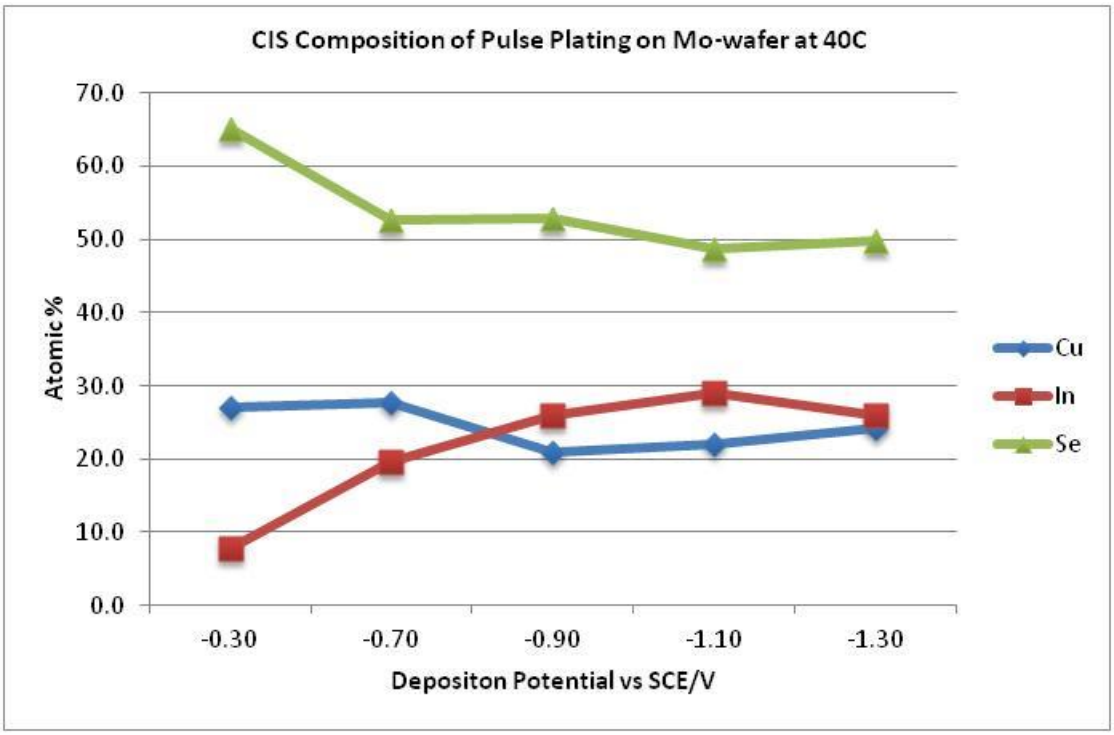


Figure 20: Composition of Pulse electrodeposition of CIS thin on Mo-wafer at 40°C as a function of deposition potential as determined by EDX.

There is a general trend of copper and selenium compositions decreasing, while indium composition increases as the deposition potential decreases from -0.3 to -1.3. This result correlates with the work of Chaure *et al* [8] who used XRF to determine the compositions of their films. It is not easily to incorporate indium in the film unless the deposition is carried out at more negative potential. The standard potential of indium with reference to standard hydrogen electrode is -0.338V, as compared to selenium at +0.740V and copper at +0.342V. Hence, at lower more negative potential range, the film is more copper and selenium rich. As the potential is made more negative, the indium content increases causing both copper and selenium decrease to makeup the 100% composition.

Moreover, excess selenium promotes the formation of Cu_xSe compounds as mentioned by Valdes [21]. Therefore for deposition at potentials between -0.3V and -0.7V the films are more Cu and Se rich. Note that some CIS can be deposited positive of the standard potential

for indium deposition as CIS is thermodynamically more stable than In metal. As the deposition potential is made further negative towards -1.3V the indium content increases, thus copper and selenium decreases at the total has to remain 100%.

The above results agree with the initial discussion in the introduction chapter as well as XRD results shown in the following Section 3.3. For the deposition potentials between -0.3V to -0.4V Cu_3Se_2 was produced according to the following reactions:

$$3Cu(II) + 2\ H_2SeO_3 + 8H^+ + 14e^- \rightarrow Cu_3Se_2 + 6H_2O$$

Cu_3Se_2 will be reduced to CuSe as the deposition potential is decreased further, and dissolution of Se(IV) would reduced to Se and deposit on CuSe. At deposition potentials near -0.7V, Indium will be incorporated into the deposit which is shown in Figure 18. Hence, it is believed that an amorphous passive layer (In-Se compound) would be form with stoichiometry close to $CuSe_2$, which acts like a blocking absorbate. $CuInSe_2$ will be formed as below:

$$Cu(II) + 2H_2SeO_3 + In(III) + 8H^+ + 13e^- \rightarrow CuInSe_2 + 6H_2O$$

$$2Cu(II) + H_2SeO_3 + 4H^+ + 8e^- \rightarrow Cu_2Se + 3H_2O$$

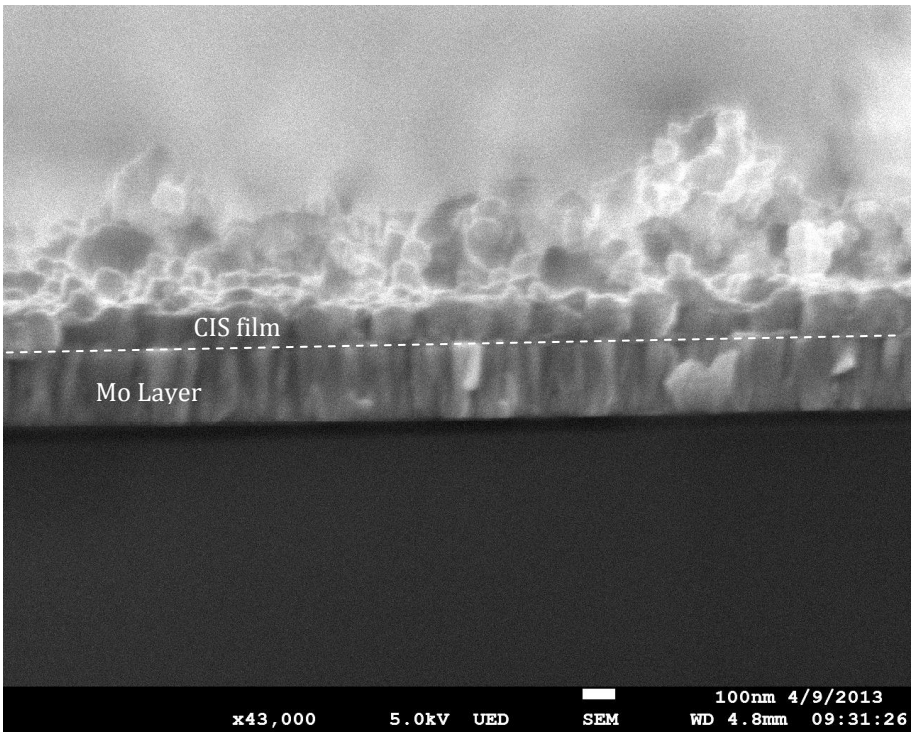
As stated above, for the Mo-wafer both DC deposition and Pulse deposition shows near stoichiometric CIS materials for deposition potential ranging from -0.9V to -1.3V.

Studies made by Endo *et al* [10] suggested that annealing would not make much change to the stoichiometry composition, which in this case has also proven in the EDX results shown above.

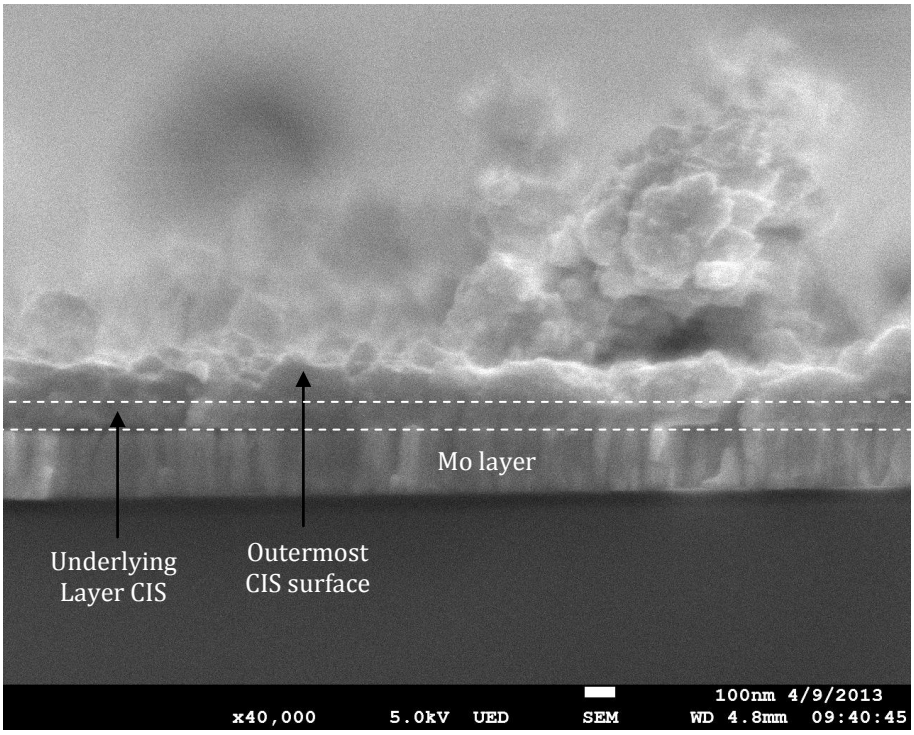
3.2 SURFACE MORPHOLOGY EVALUATION BY SCANNING ELECTRON MICROSCOPY (SEM)

3.2.1 Cross-section View

To view a “clean cut” of the cross sections, samples were cleaved directly with a diamond scriber. Because mechanical polishing may cause smearing and would change the whole profile due to the shearing effect, only Mo-wafers were imaged, as the Mo-strip cannot be cleaved.

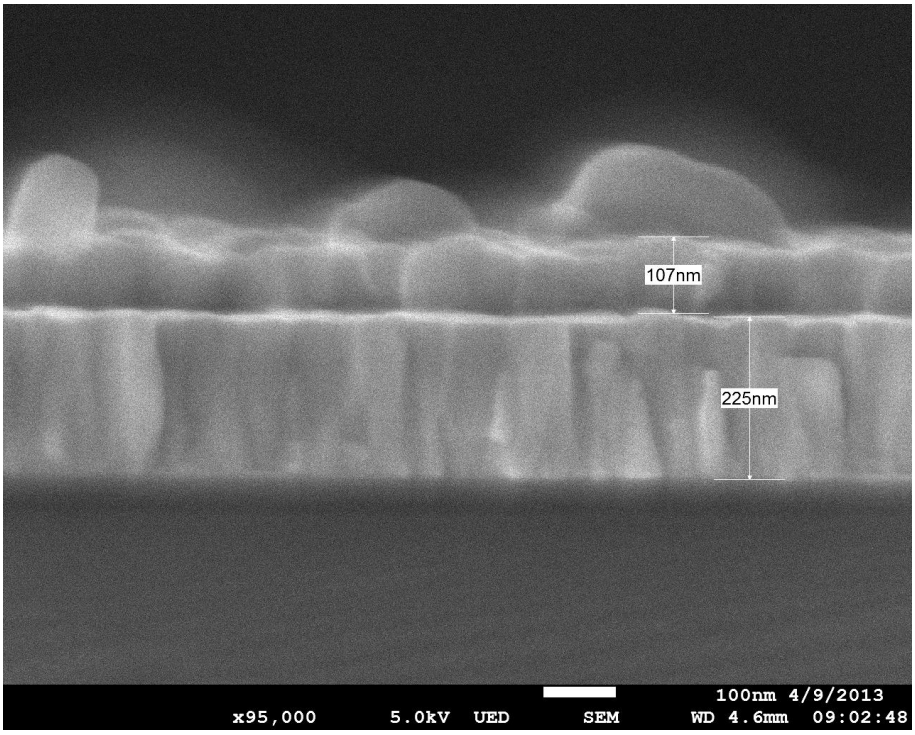


Pulse plating at -0.9V

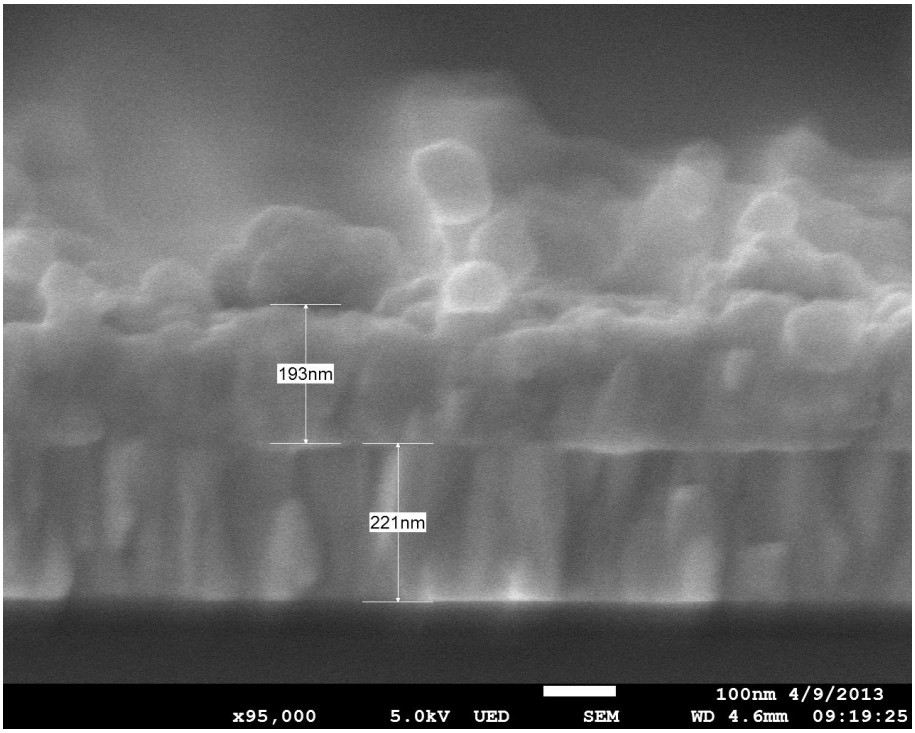


DC plating at -0.9V

Figure 21: Micrographs of Pulse plating at -0.9V and DC plating at -0.9V.



Direct Current Plating at -0.3V (with measurement)



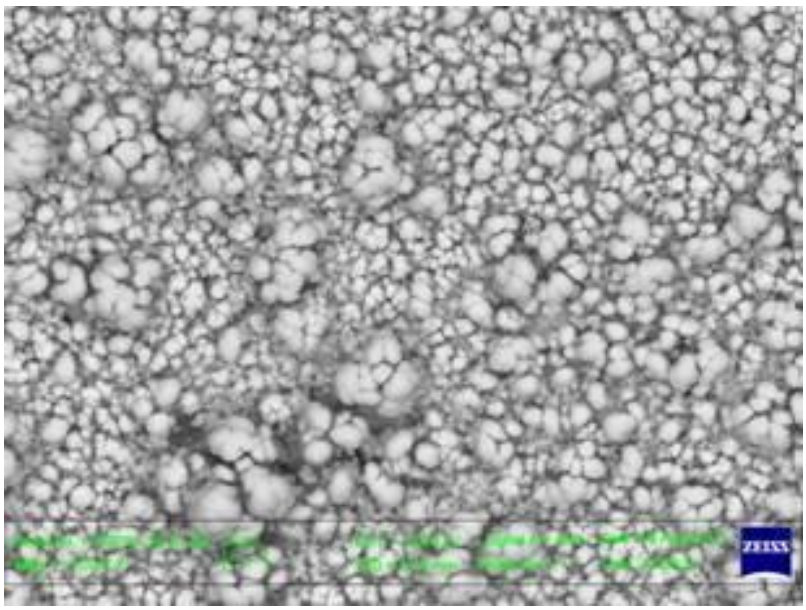
Direct Current Plating at -1.1V (with measurement)

Figure 22: Micrographs of DC plating and thickness of Mo and CIS films

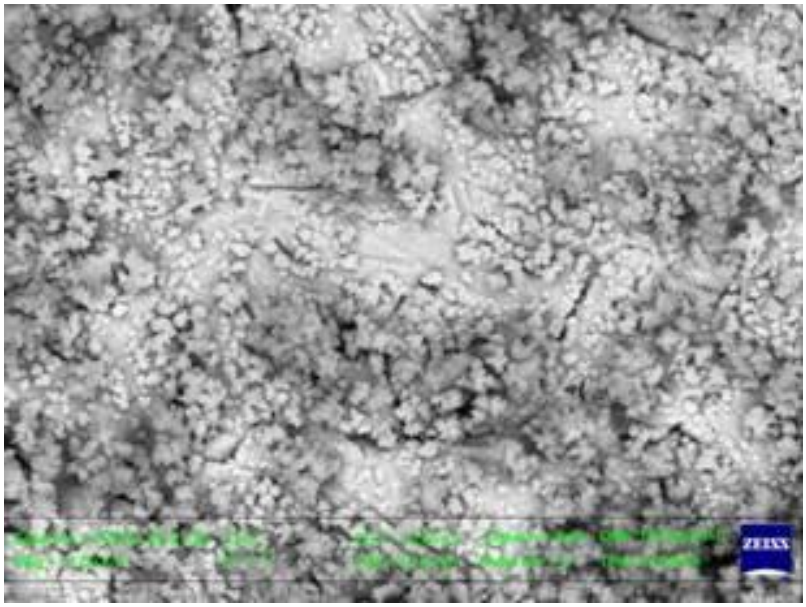
In Figure 21, the micrographs show that the grains are more distinct with pulse plating than with DC plating. The DC plating also shows a double layer structure of CIS on top of the Mo surface.

Figure 22 shows that the Mo layer is about 220nm, while the DC plated CIS layer thickness increases from about 100nm at -0.3V to almost 190nm at -1.1V. It is clearly shown that there is compact underlying layer and a more porous outer layer at -1.1V potential.

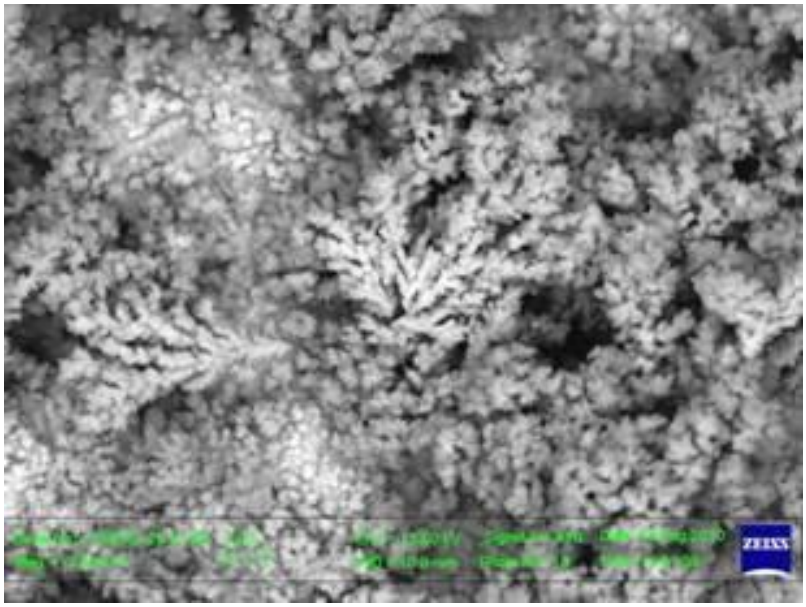
3.2.2 Surface Profile Morphology



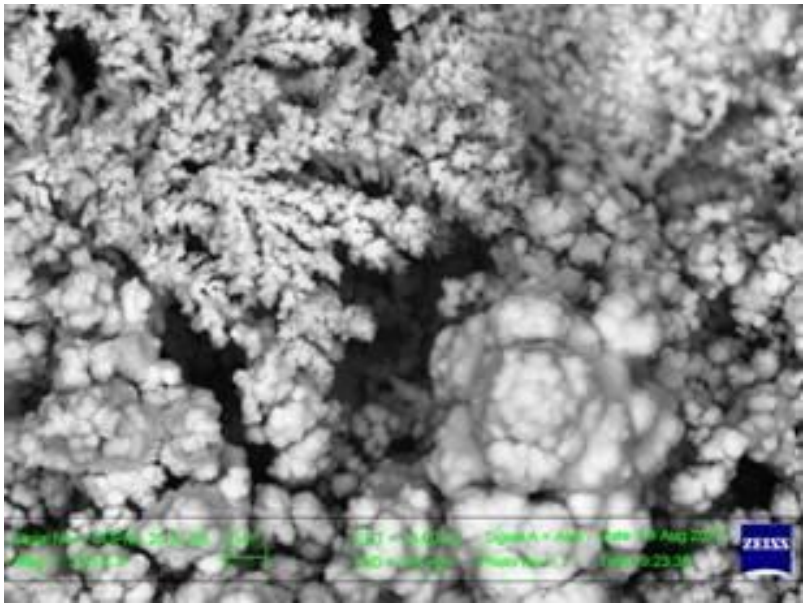
-0.3V(DC Mo-Strip)



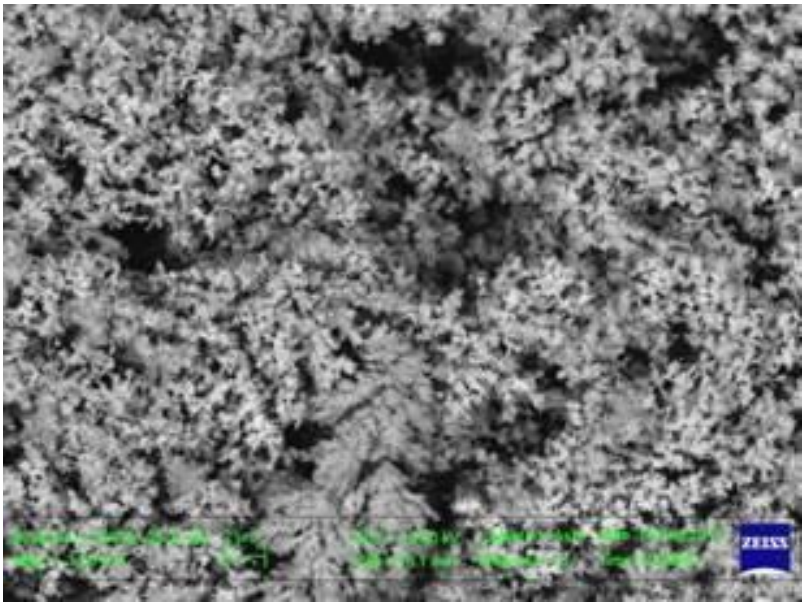
-0.7V(DC Mo-Strip)



-0.9V(DC Mo-Strip)



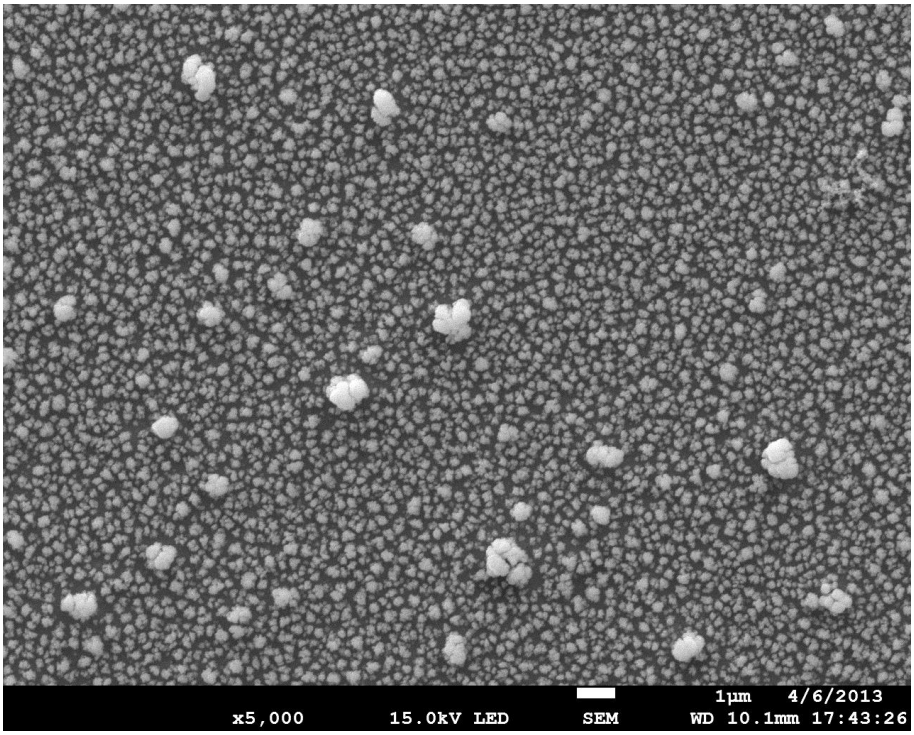
-1.1V (DC Mo-Strip)



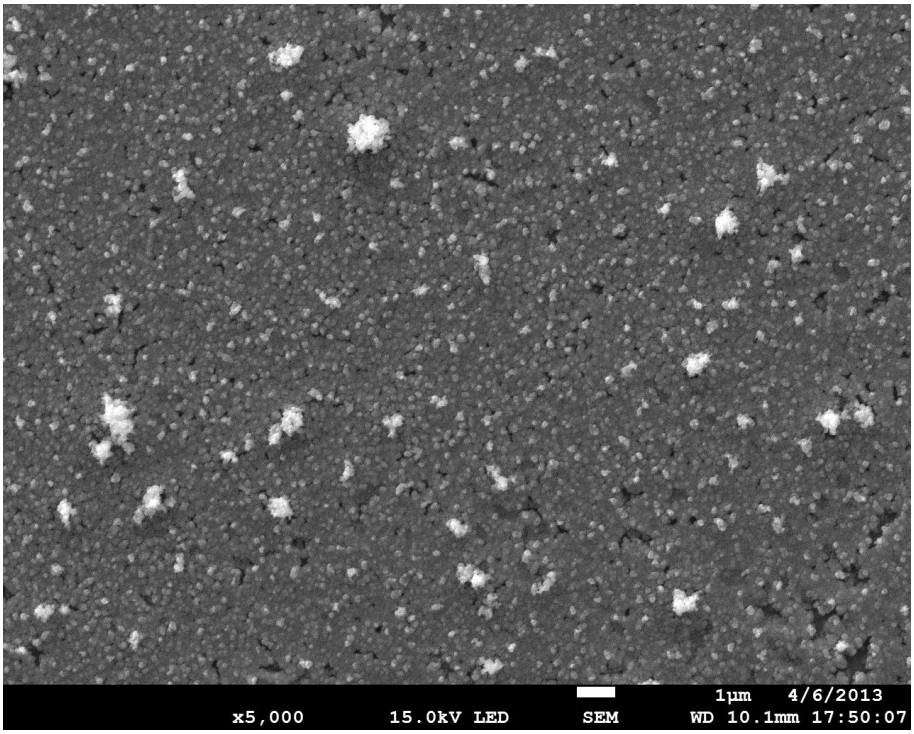
-1.3V(DC Mo-Strip)

Figure 23: DC plating on Mo wafer at room temperature micrographs

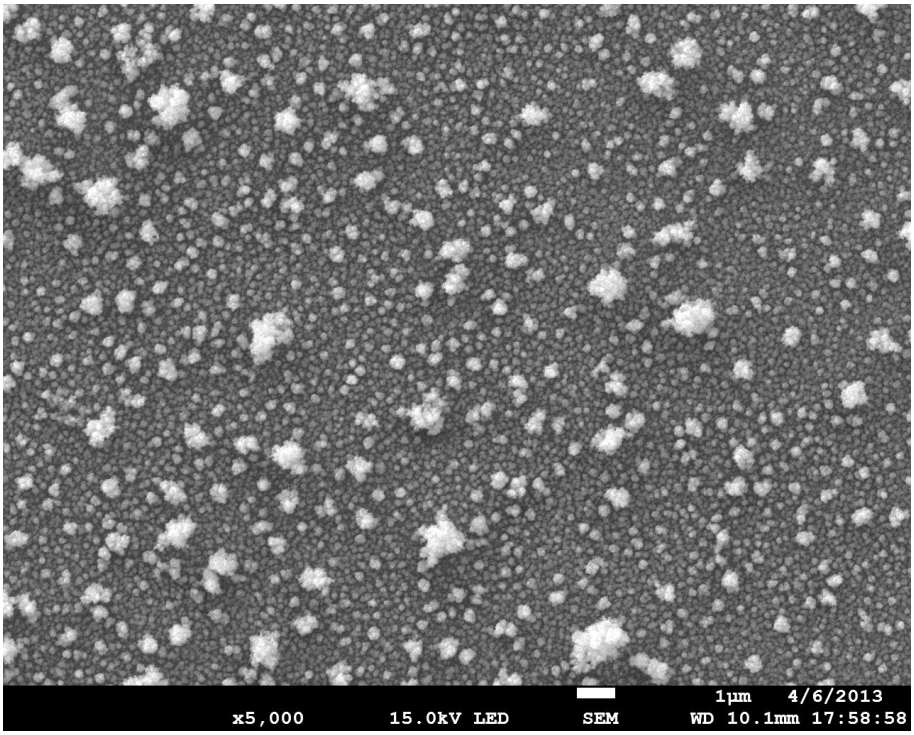
Figure 23 shows the various micrographs of CIS film at different potential surface morphology after DC plating at room temperature.



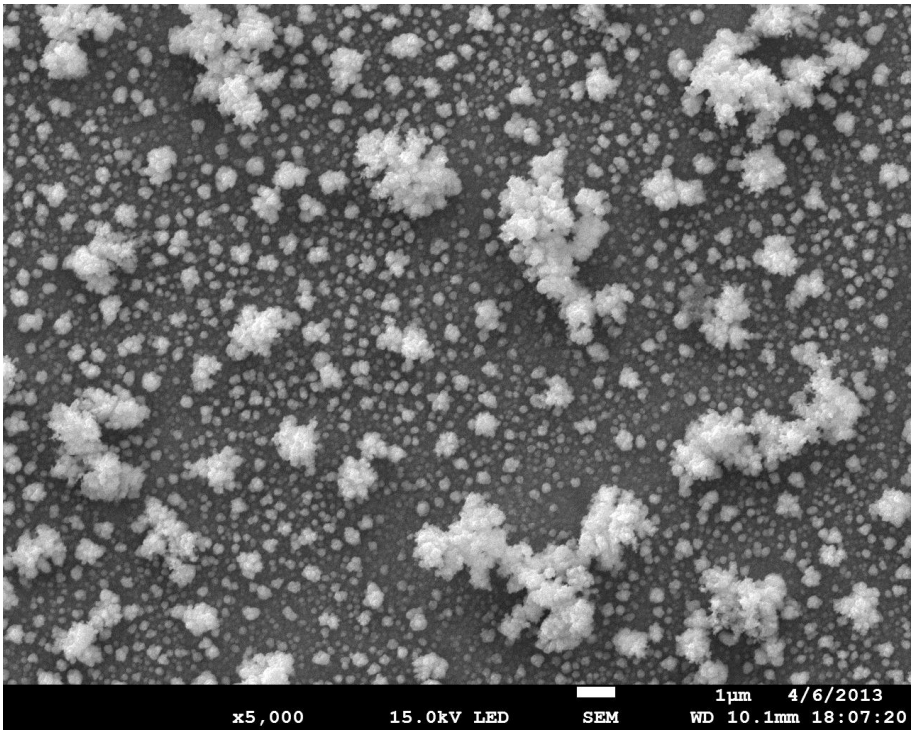
-0.3V (DC Mo-wafer)



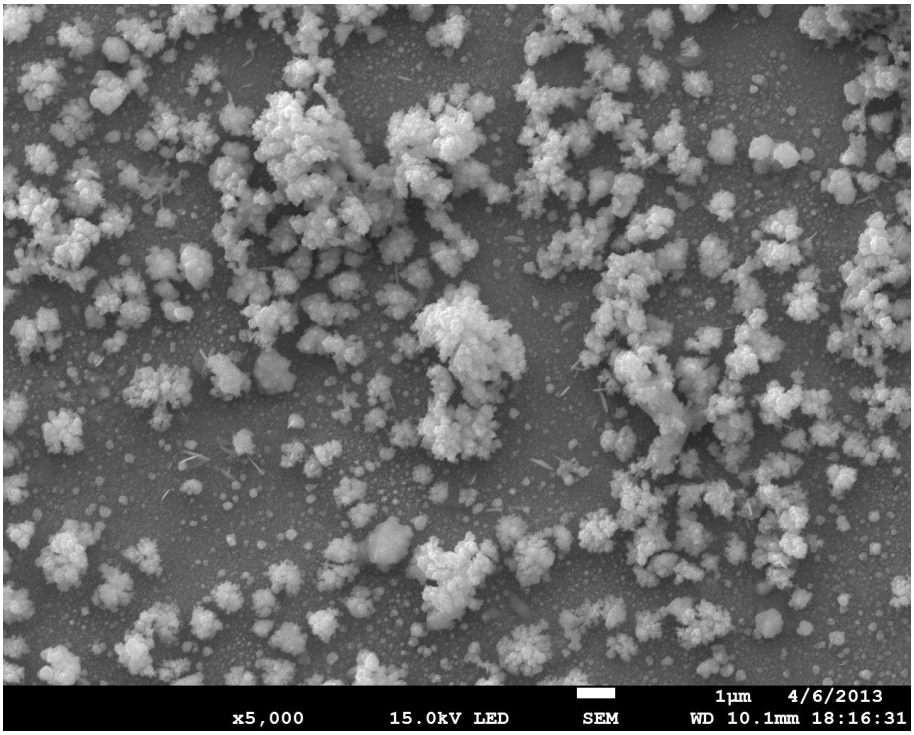
-0.7V (DC Mo-wafer)



-0.9V (DC Mo-wafer)



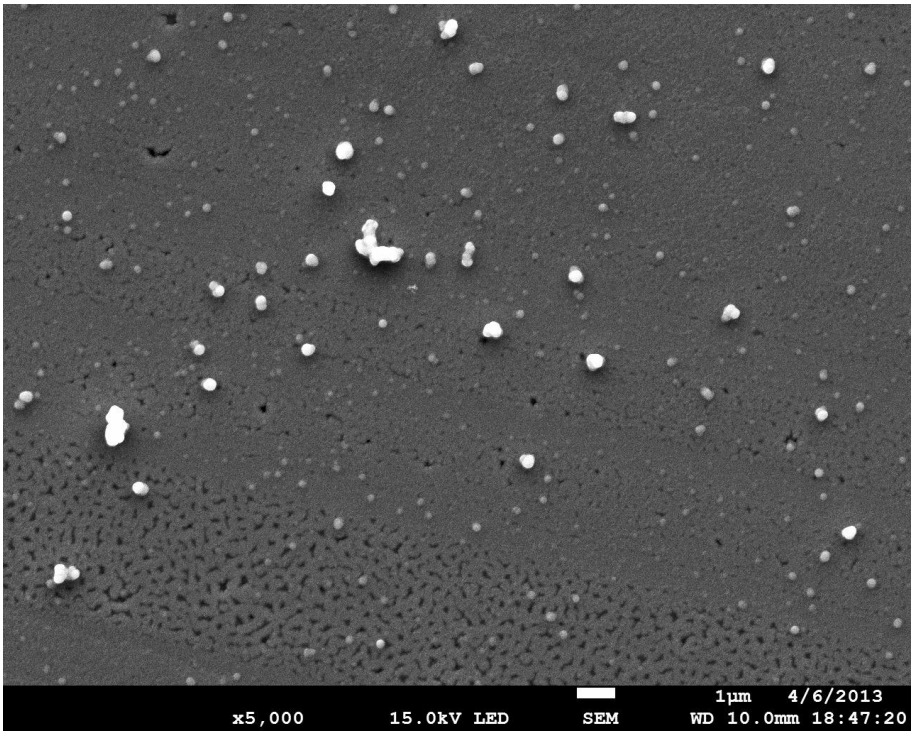
-1.1V (DC Mo-wafer)



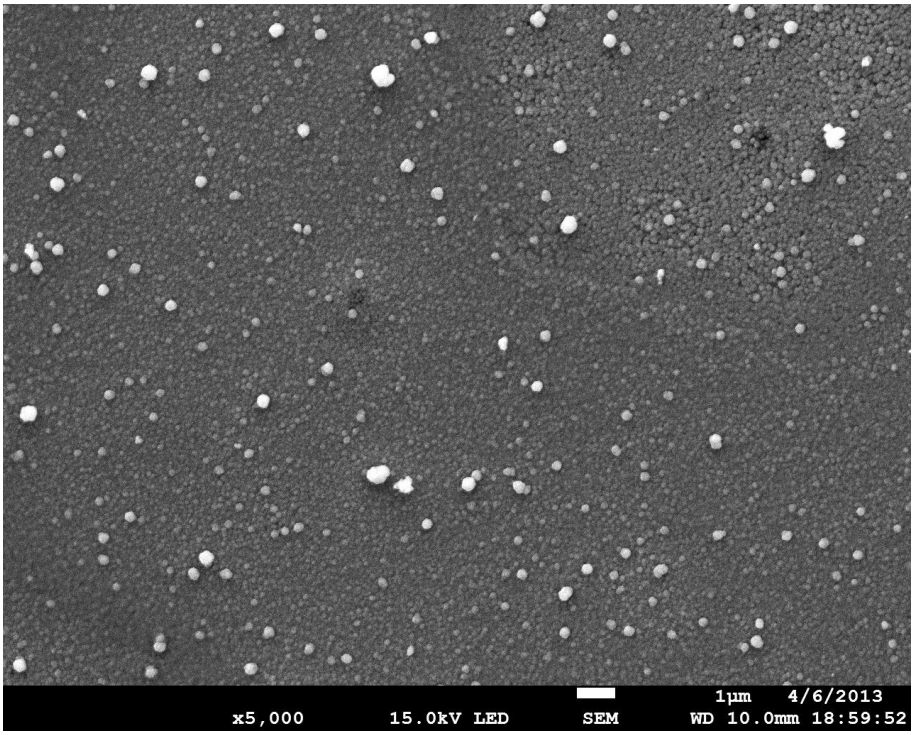
-1.3V (DC Mo-wafer)

Figure 24: DC plating on Mo wafer at room temperature micrographs

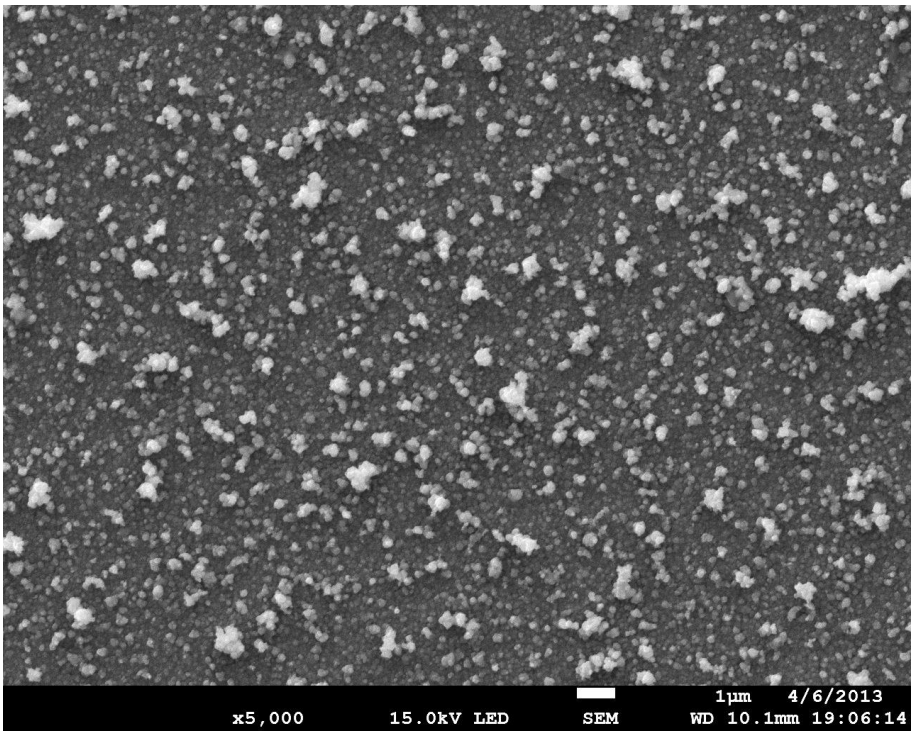
Figure 24 illustrate the micrographs of the CIS film surface morphology of various depositions potential after DC plating on Mo-wafer at room temperature.



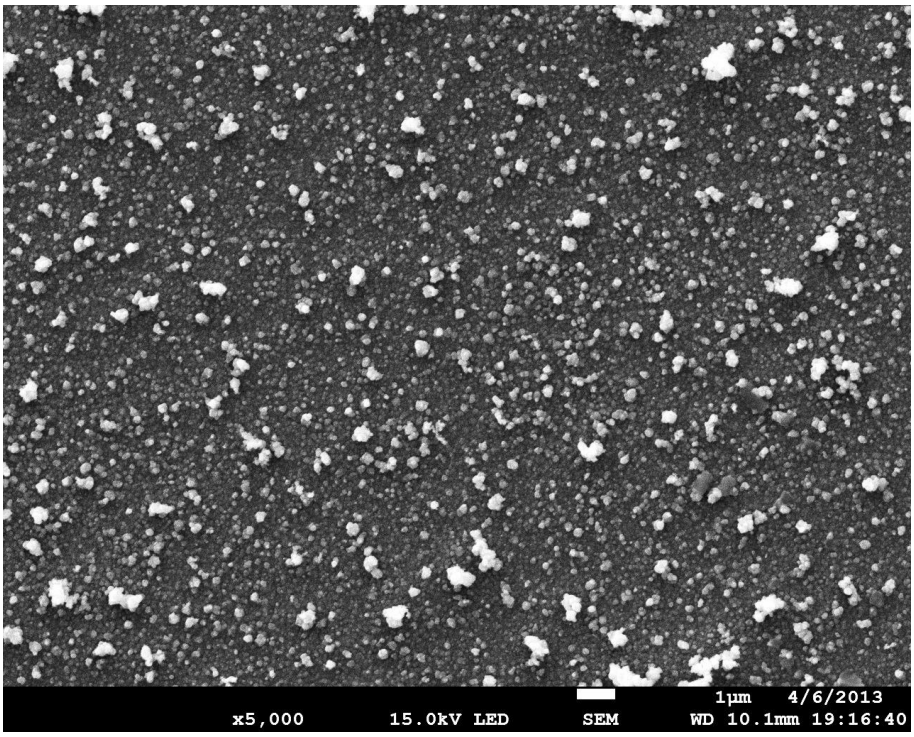
-0.3V (Pulse Mo-wafer)



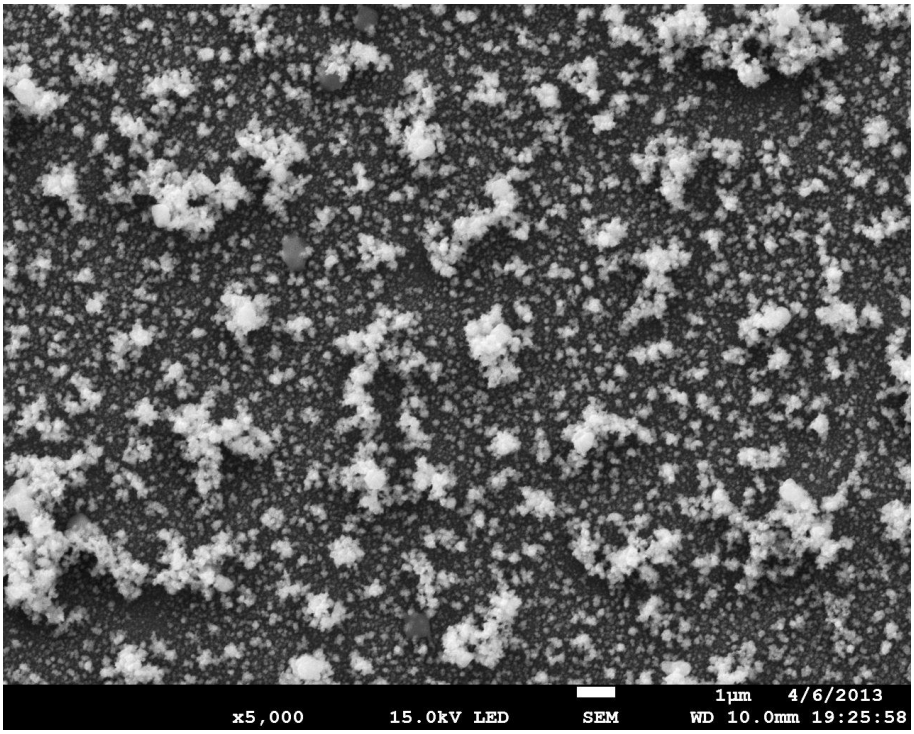
-0.7V (Pulse Mo-wafer)



-0.9V (Pulse Mo-wafer)



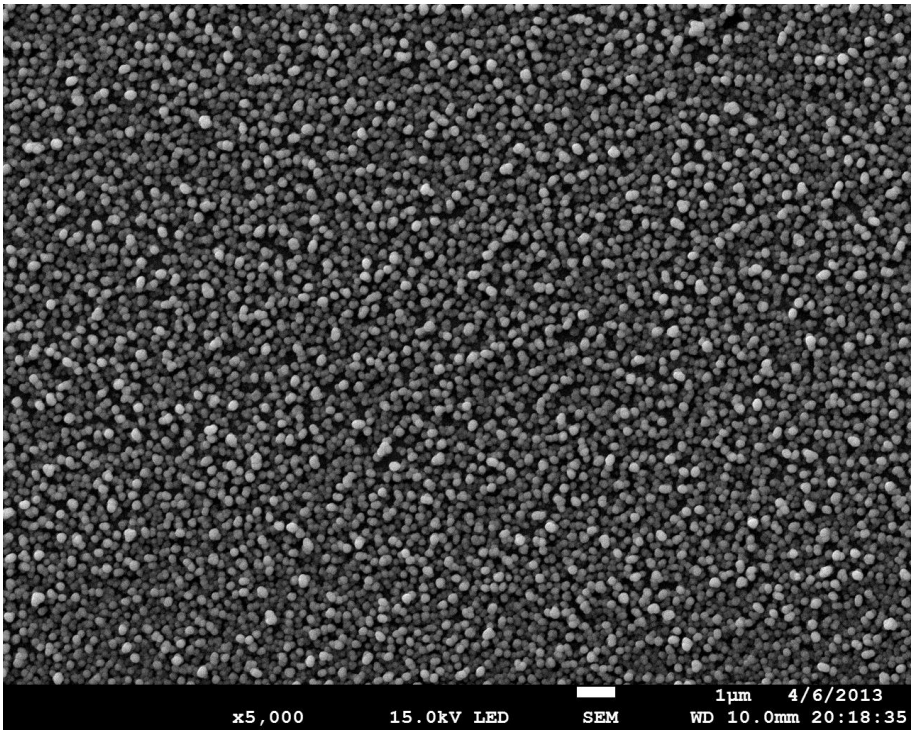
-1.1V (Pulse Mo-wafer)



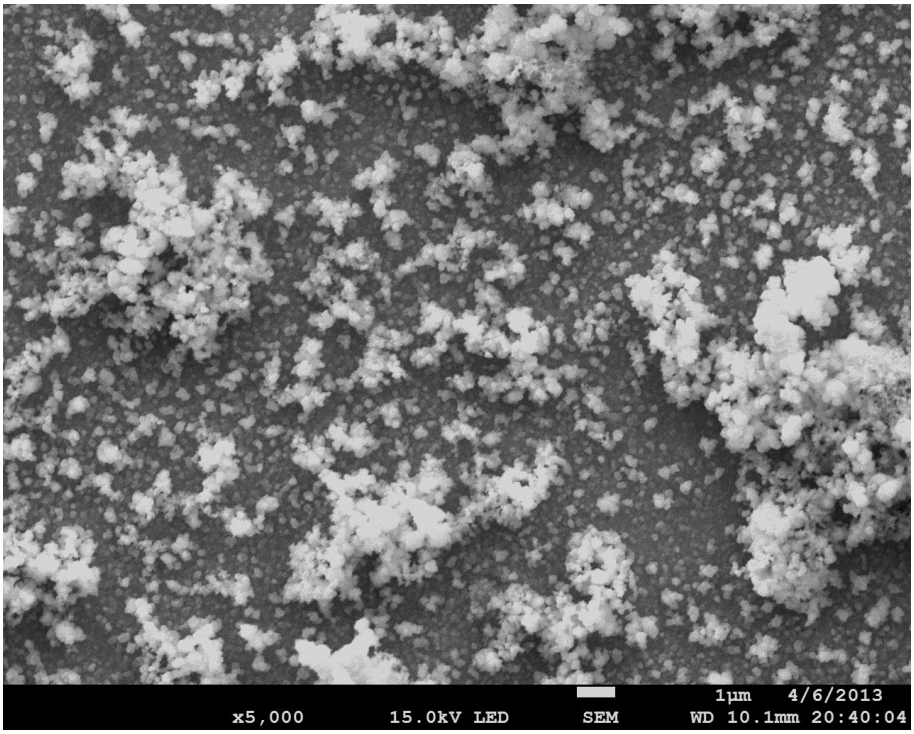
-1.3V (Pulse Mo-wafer)

Figure 25: Pulse plating on Mo-wafer substrate at room temperature

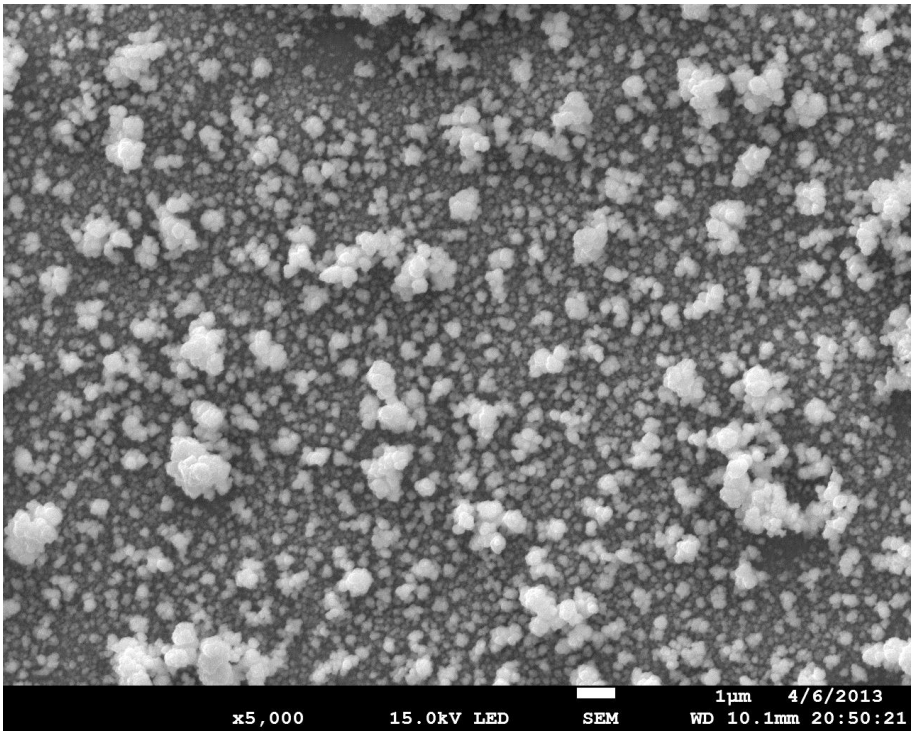
Figure 25 shows the micrographs of CIS film surface morphology of various deposition potentials by pulse plating at room temperature.



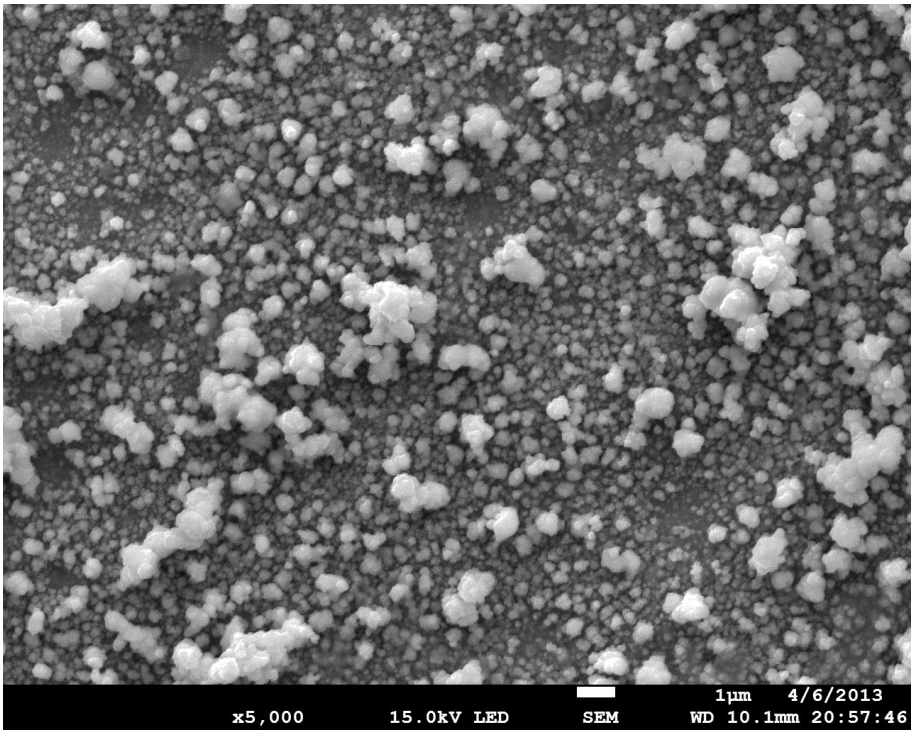
-0.3V (Pulse @40°C Mo-wafer)



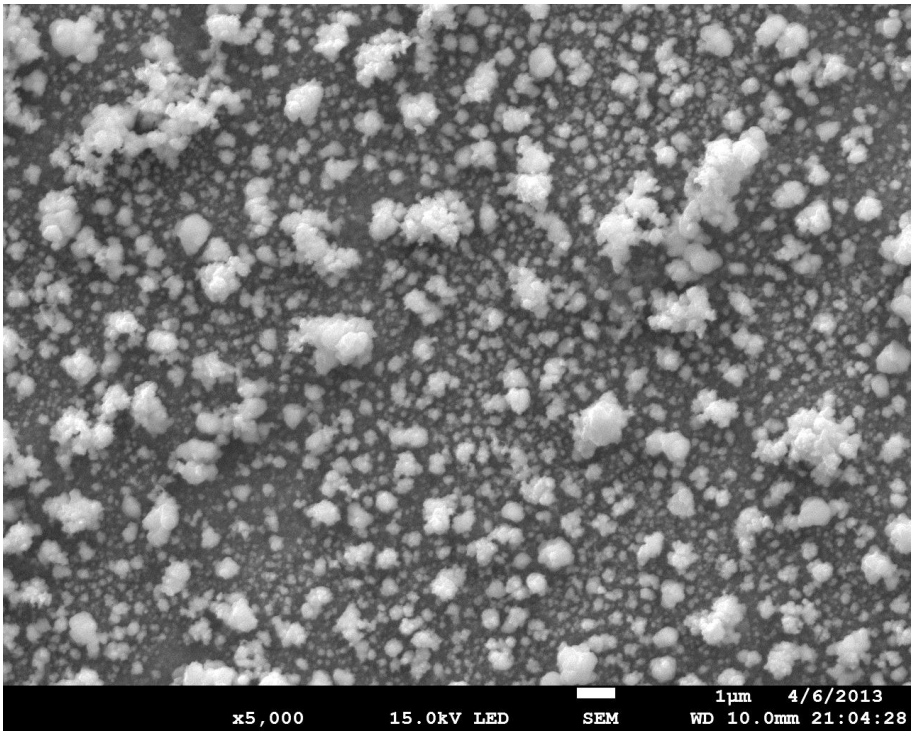
-0.7V (Pulse @40°C Mo-wafer)



-0.9V (Pulse @40°C Mo-wafer)



-1.1V (Pulse @40°C Mo-wafer)



-1.3V (Pulse @40°C Mo-wafer)

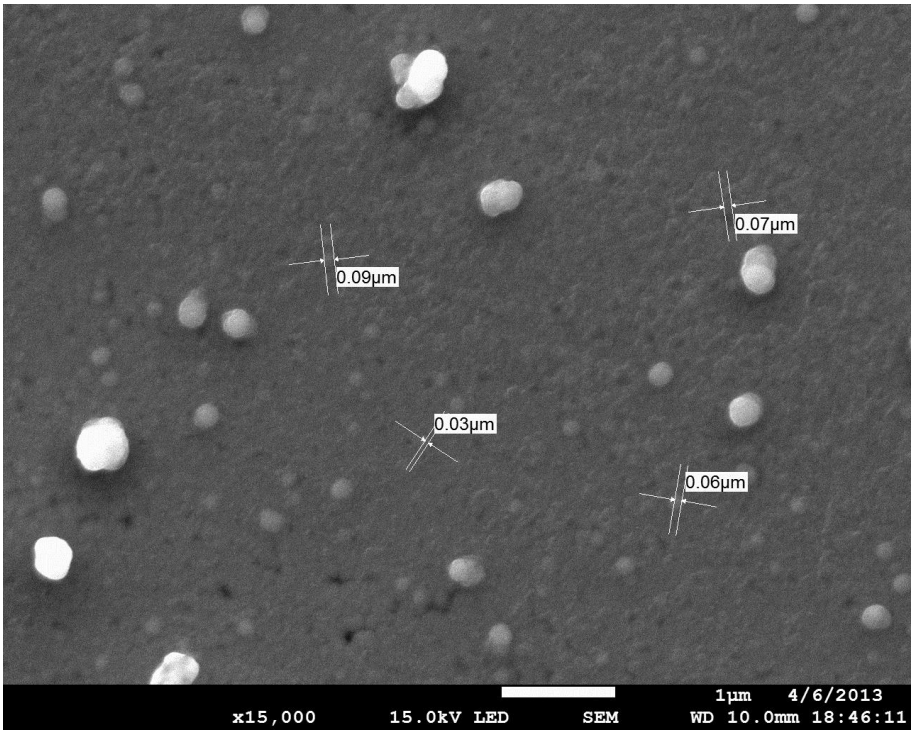
Figure 26: Pulse plating on Mo-wafer at 40°C micrographs.

Figure 23 shows that the morphology profile of CIS thin film deposited on Mo strips at -0.3V has a cauliflower-like structure on the surface, whereas at more negative potentials (-0.7 to -1.3V) more massive dendrite structures are formed.

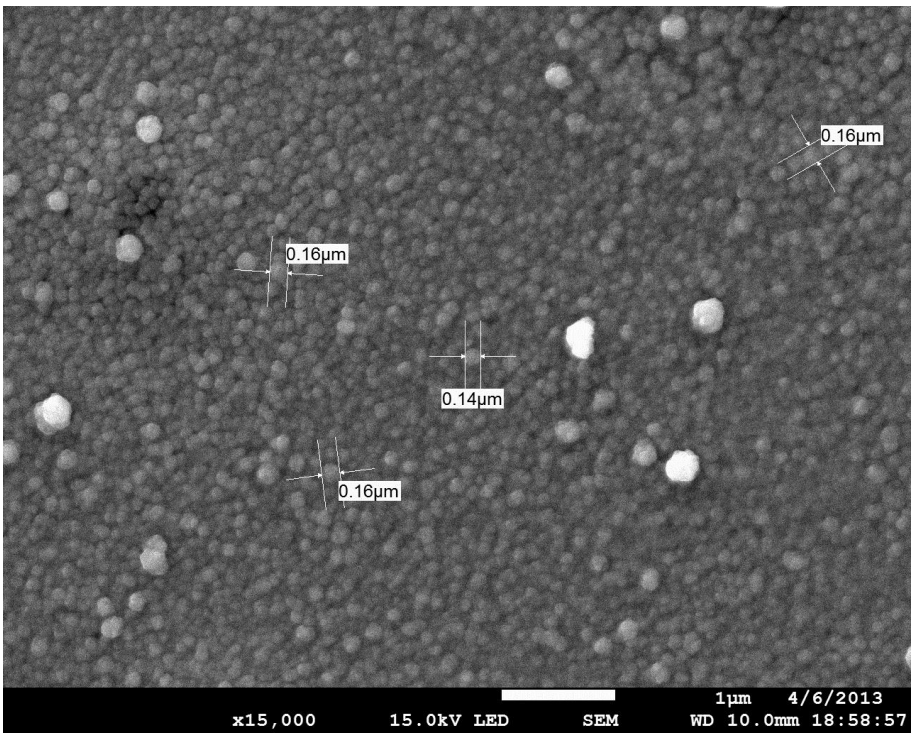
For DC electrodeposition on Mo-wafer it can be seen from Figure 23 that at -0.3V and -0.7V the morphology consists of small particle-like structures with small random cauliflower-like structure on the surface.

Unlike for the case of plating on Mo-strip, there were no massive dendrite structures observed for -0.9V, and -1.1V in Figure 24, instead the cauliflower like structure is still observed on the surface for the two depositions potential. Nevertheless, -1.3V deposition potential dendrite structures were partially seen. However, based on the cross-section images in Figure 21 and Figure 22 full coating was achieved so it is likely that the cauliflower structures are the porous outer layer observed in the cross sectional SEM images.

When pulse plating was used at room temperature, only small randomly distributed particles were observed at -0.3V and -0.7V vs SCE (Figure 24).



-0.3V (Pulse Mo-wafer)



-0.7V (Pulse Mo-wafer)

Figure 27: Pulse plating surface morphology at room temperature at -0.3V and -0.7V at higher magnification.

At higher magnification illustrated in Figure 27 it can be seen that the average size of the particles was 0.06um at -0.3V whereas there are larger ones of 0.16um at -0.7V. For deposition potentials at -0.9V and 1.1V, small cauliflowers like structures were seen and dendrite structures were observed at -1.3V. With pulse plating process at less negative potential (i.e. -0.3V and -0.7V), the ions in the electrolyte are given sufficient time to diffuse and forms a nuclei site Mo surface, thus favoring the nucleation of grains and increasing the number of nuclei per unit area. Reactions were controlled by charge transfer, thus discrete particle like morphology were observed. As the potential decreases further from -0.9 to -1.3, the mass transport may starts to occur, which results in the formation of dendrites structures.

Figure 26 shows that at the higher temperature of 40°C small uniform particle like structure were observed at -0.3V, while dendrite structures formed at all other potentials. Beyond which, all deposition potentials contain dendrite structures.

Fu *et al.* found that a dendrite structure obtained by plating usually exhibits poor adhesion and contains $Cu_{2-x}Se$ [23], As a result post annealing treatment is required to enhance the crystallinity and improved adhesion by allowing the grains at the CIS-Mo interface to grow.

Generally, a dendrite structure is the result of concentration gradients existing in the electrolyte leading to mass transport limiting the electrodeposition process. That is rate of the diffusion process of electrolyte ions to the surface is slower than that of the charge-transfer in the electrochemical deposition itself. Hence the rate determining step is controlled by the diffusion process of the reactive ions (i.e In^{3+}, Cu^{2+} and SeO_3^{2-})

During the electrodeposition process that is under mass transport control, the ions (Cu, In, Se etc) have insufficient time to diffuse to a

suitable site on the Mo substrate surface before reaching the lowest Gibbs free energy, hence they would nucleate and grow on the similar grain by stacking on the other existing grain. The resultant surface profile of thin film is therefore an irregular porous dendrite structure, and would not adhere well to the Mo substrate surface.

The higher the potential difference, the greater the current density and thus the faster ions are consumed at the surface, At some point the rate of arrival of ions at the electrode surface from the bulk electrolyte can no longer keep pace and the reaction becomes mass transport limited. This is clearly seen at deposition potentials -0.9V to -1.3V which usually has dendrite a structure especially for direct current plating (Figure 23 to Figure 26).

3.3 PHASE ANALYSIS BY X-RAY DIFFRACTOMETER (XRD)

Figure 28 to Figure 36 are the graphical plots of XRD data of “as plated” films and after annealing and KCN etching (after treatments). Peaks produced from substrates (metallic Mo or Si wafers) and from XRD Nickel filter are labeled with an asterisk (*).

3.3.1 Mo-strip by DC plating at room temperature

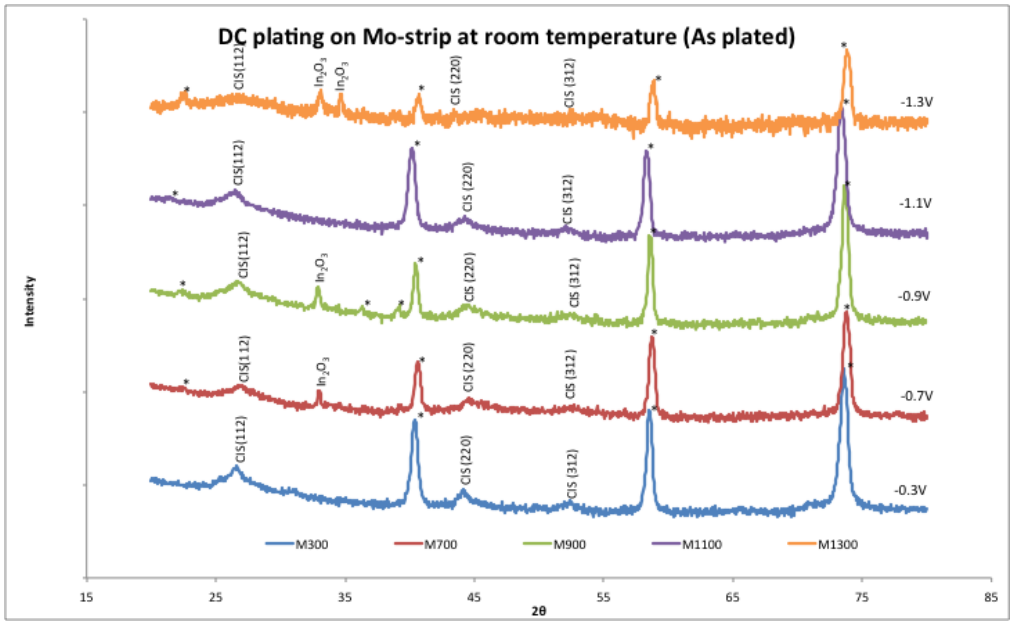


Figure 28: XRD plot of DC deposition of CIS thin film on Mo strip with potential at -0.3V, -0.7V, -0.9V, -1.1V and -1.3V performed at room temperature.

Figure 28 shows that CIS (112) and CIS (220) orientations were readily form upon direct deposition on Mo strips, with the CIS(112) and CIS(220) peaks being clearly visible even at the most positive deposition potential of -0.3V vs SCE. However, no In_2O_3 was were detected at a deposition potential of -1.1V., this might explain why there is a slight decrease in EDX atomic composition from -0.9V to -1.1V, where most of the Indium content is believed to be coming from CIS thin films.

Observing from the peaks of CIS(112), the Full Width Half Maximum (FWHM) of the peaks seemed to increase with decreasing deposition potentials. This shows that the crystal size decreases with decreasing potentials, which correlates with the mass transport dendritic growth shown in 3.2.2. Assuming the grains are spherical, the estimated crystallite size (D) can be calculated using Scherrer's formula [3]:

$$D\ (nm) = 0.9\lambda / FWHM\ (\cos\theta)$$

Where λ is the wavelength of the Bruker 8D advance x-ray used (1.5406 angstrom), θ is the Bragg's angle.

It was found that the size ranges from 42nm to 157nm at -0.3V to -1.3V respectively. Thus the more negative the deposition potential, the smaller the crystallite size, which is consistent with the domination of nucleation over the growth stage expected under mass transport limited conditions (i.e. there are many nucleation events but little growth of any single crystallite).

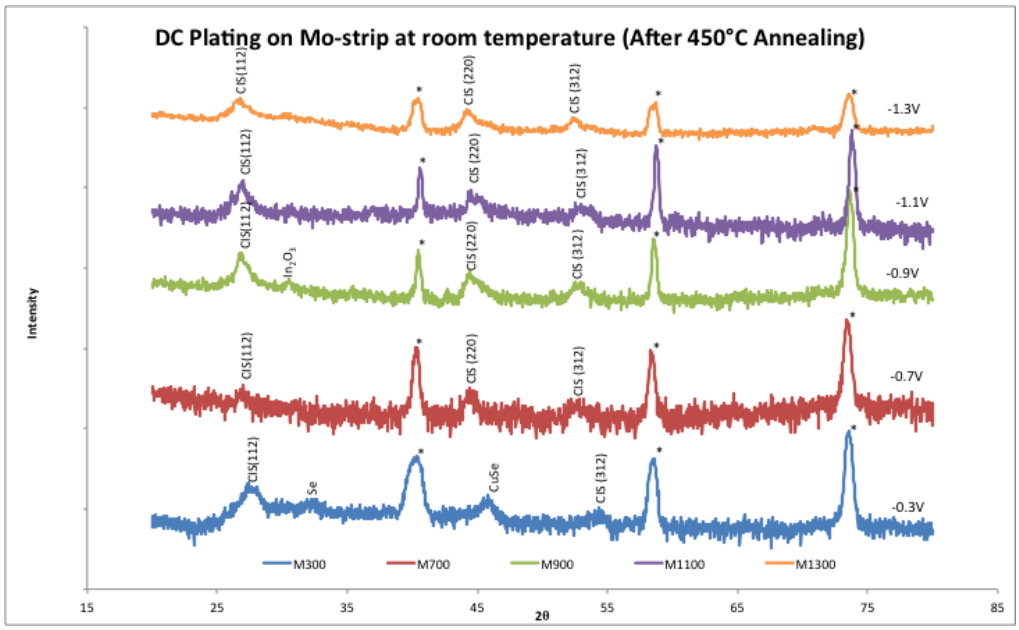


Figure 29: XRD plot of CIS thin film on Mo strip after annealing at 450°C for 30min with potential at -0.3V, -0.7V, -0.9V, -1.1V and -1.3V performed at room temperature.

It was observed from Figure 28 and Figure 29 that the peak width of CIS (112) increases on annealing meaning that, as expected, the crystal grains have increase in size during annealing. It has also shown that presence of Se peak were observed with deposition potential of -0.3V which correlates with the data shown in elemental dispersive analysis in the earlier section.

Table 5: Crystal size of CIS on Mo-strip before and after annealing at 450°C, base on CIS(211) peak widths.

Crystallite size of CIS(112)	As plated/nm	Annealed/nm
DC Mo-strip -1.3V	42	110
DC Mo-strip -1.1V	84	130
DC Mo-strip -0.9V	97	140
DC Mo-strip -0.7V	140	160
DC Mo-strip -0.3V	157	140

Table 5 shows the annealing effect on crystal size, using Scherrer's formula on the CIS(211) peaks. It indicates that the crystal size of CIS generally increased after annealing at 450°C, thus annealing does improved the crystallinity of the CIS films by enhancing crystal growth. Looking at the crystallite size of CIS after annealing, deposition potential of -0.3V is slightly smaller than -0.7V, which does not follow relationship of as-plated.

From the micrographs of the as-plated Mo-strip in Section 3.2.2 Figure 23, unlike the -0.7V to -1.3V dendrites structure, the -0.3V shows relative big cauliflower-like structure. This might be due to the likelihood that cauliflower-like structure, being more compacted than porous dendrite structures, experiencing dislocation strains during annealing and the ultrasonic frequency cleaning process causing a broadening of peak at -0.3V, thus the increase of crystal size is not as much as those with dendrite structures.

Furthermore, metallic Se and CuSe peaks at -0.3V are more distinct after annealing, this shows that Cu and Se rich phases are prevalent at the more positive deposition potentials. This correlates with the EDX results shown in earlier Section 3.1 ELEMENTAL ANALYSIS BY ENERGY DISPERSIVE X-RAY (EDX) SPECTROCOPY. Lastly, no In_2O_3 peaks were seen after annealing, except at -0.9V deposition potential, which might have reacted to form CIS films, suggesting that much of the indium tied up in the oxide became available for CIS formation at the elevated temperature.

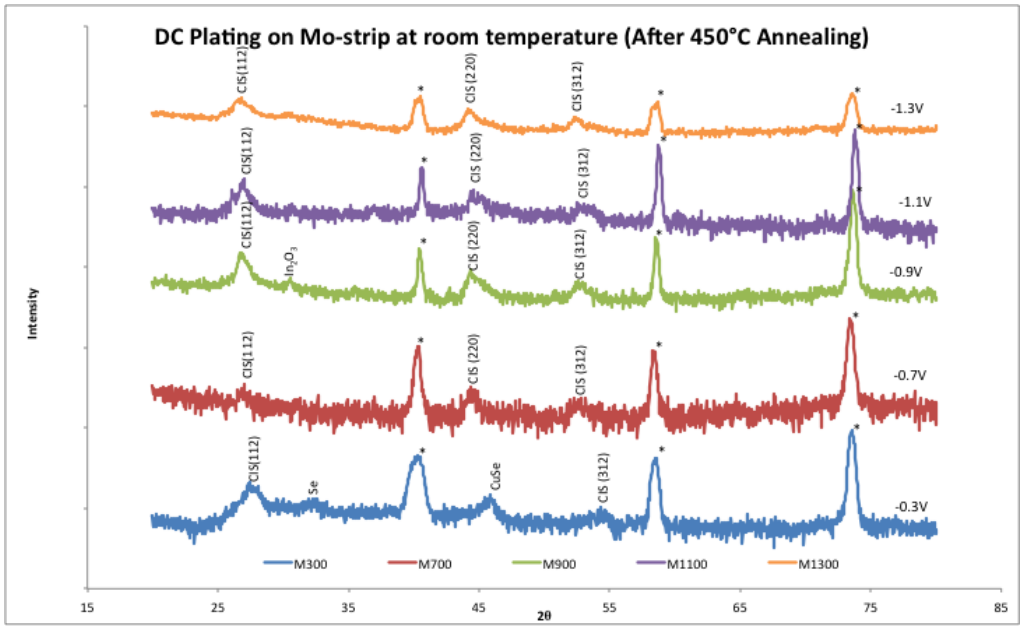


Figure 30: XRD plot of CIS thin film on Mo strip after KCN etching with potential at -0.3V, -0.7V, -0.9V, -1.1V and -1.3V

Figure 30 shows the XRD patterns after the KCN etch. It can be clearly seen that the etch was successful in removing both the Se and CuSe. As etching removed the unwanted phases the CIS (400) peak can also now be observed. Nevertheless, In_2O_3 compound peaks were also reveals which cannot be removed by KCN etching. In additions, CIS peaks were also removed in the process of KCN etching, this can be clearly shown in -0.3V and -1.1V XRD plot, this shows the poor adhesion of the films deposited at these potentials.

3.3.2 Mo-wafer by DC plating at room temperature

Figure 31 shows XRD plot of DC deposition of CIS thin film on Mo wafer of various deposition potentials after DC plating at room temperature.

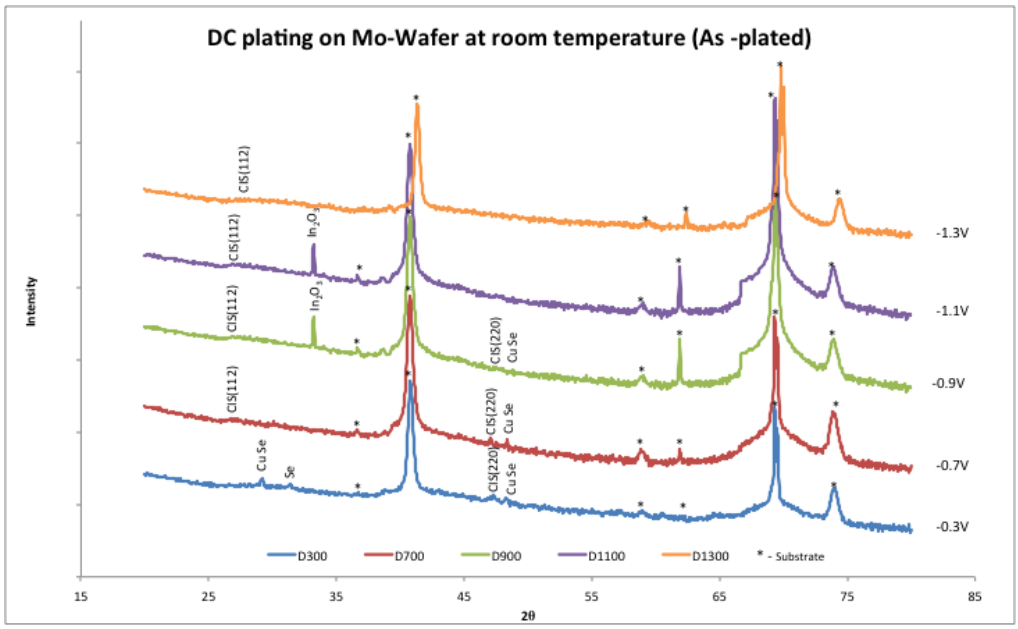


Figure 31: XRD plot of DC deposition of CIS thin film on Mo wafer with potential at -0.3V, -0.7V, -0.9V, -1.1V and -1.3V at room temperature.

It shows that the CIS (112) and CIS(220) can easily be distinguished in the XRD of the DC plated films on the Mo-wafer strip room temperature. However, In_2O_3 peaks are also present at -0.7V and -1.1V deposition potential. CuSe phase were also form at deposition potentials of -0.3V to -0.9V, with no CIS peaks being observable from the film deposited at a potential of -0.3V. Where CIS peaks were observed they were quite broad and the estimated crystallite sizes were calculated below.

Table 6: Calculated crystallite sizes for CIS dc plated on Mo-wafer at room temperature (as plated).

Crystallite size of CIS(112)	As plated/nm
DC Mo-wafer @ -1.3V	100
DC Mo-wafer @ -1.1V	110
DC Mo-wafer @ -0.9V	160
DC Mo-wafer @ -0.7V	180
DC Mo-wafer @ -0.3V	N.A.

**round off to the nearest 2 significant figure*

Table 6 shows the estimated crystallite sizes of CIS deposited with DC plating on Mo-wafer. The crystallite sizes ranges from 100 nm to 180nm, and it increases with increasing negative deposition potentials, for the reasons as given in Section 3.3.1. Relating back to the micrographs of Figure 24 shown in Section 3.2.2, the crystallite size shown in Table 6 tally with the transition from charge transfer to mass transport control that leads to formation of dendrite structures.

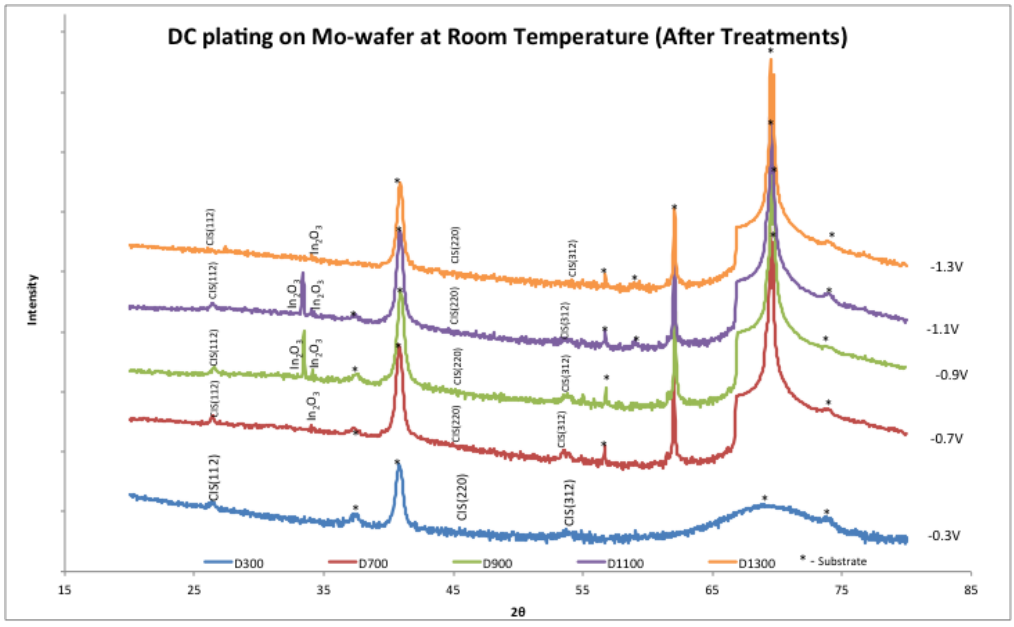


Figure 32: XRD plot CIS thin film after post treatment on Mo wafer with potential at -0.3V, -0.7V, -0.9V, -1.1V and -1.3V at room temperature.

Figure 32 shows that post treatments of annealing and KCN etching have successfully removed CuSe phase as well as enhance the crystallinity of the CIS films, thus revealing CIS (112), CIS (220) and CIS(212). However, the intensity of the CIS (220) XRD peak decreases from Figure 31 to Figure 32 suggesting that either the CIS film has thinned or partially detached from its substrate due to poor adhesion.

Figure 32 also shows that for the dc plating on the Mo-wafers annealing does not remove the In_2O_3 at deposition potentials at -0.9V and -1.1V and even reveals oxide peaks at -0.7V and -1.3V once the CuSe phase and Se were removed by etching.

Table 7: Crystallite sizes of CIS dc plated on Mo-wafer before and after post treatments (Annealing + KCN etch) at room temperature.

Crystallite size of CIS(112)	As plated/nm	After treatments/nm	Delta change/nm
DC Mo-wafer @ -1.3V	100	1200	1100
DC Mo-wafer @ -1.1V	110	400	290
DC Mo-wafer @ -0.9V	160	420	260
DC Mo-wafer @ -0.7V	180	630	450
DC Mo-wafer @ -0.3V	N.A.	310	310

**round off to the nearest 2 significant figure*

Table 7 shows crystallite sizes estimated from Figure 31 and Figure 32 i.e. before and after annealing and KCN treatments. Generally, there was an increase in crystallite size of the CIS films after treatments, as expected from annealing, which is also the similar to the studies made my Valdes [21].

The film deposited as a potential of -1.3V had the highest increment in crystallite size, which can be explained by the fact that as plated this film was the only one to have a dendrite structure (Figure 24) and the underlying CIS structure was likely to be porous. Thus, when subjected to annealing, the underlying crystallites were not experiencing much strain for growth compared to with cauliflower-like structures of the films deposited at the other potentials.

Comparing dc plating after treatments on Mo-wafer and dc plating on Mo-strip, the crystallite sizes were much bigger with the former. This can be seen from the micrographs of the DC plate Mo-wafer (Figure 24) and DC plate Mo-strip (Figure 23) in section 3.2.2, where the latter has more massive dendrite structure than the former, which favors the growth of larger crystallite size when less strain is experienced.

3.3.3 Mo-wafer by Pulse plating at room temperature

Figure 33 shows the XRD patterns for the CIS films deposited by pulse plating at room temperature on Mo wafers.

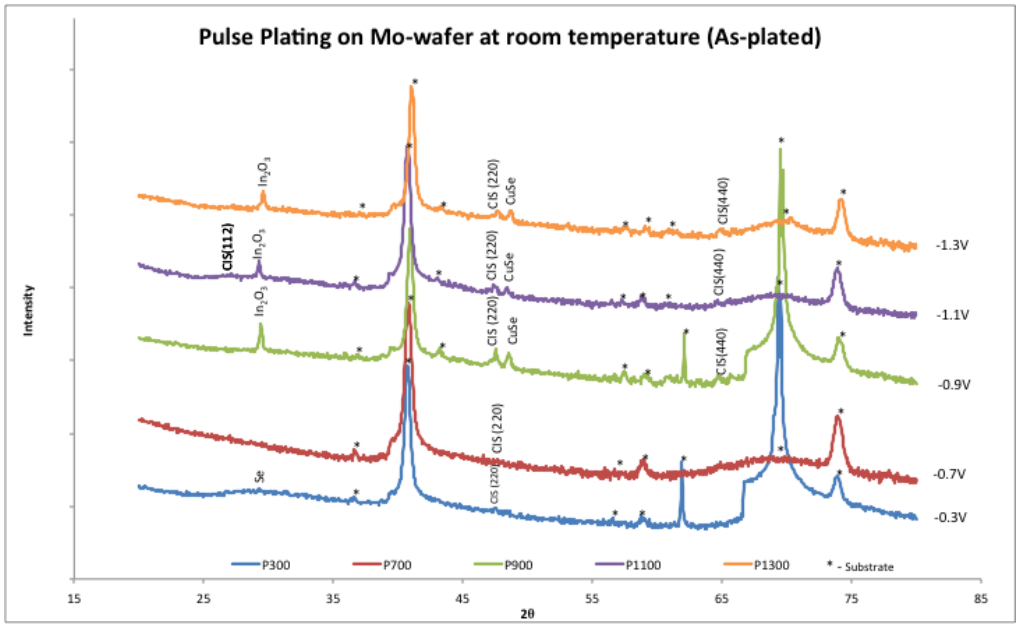


Figure 33: XRD of (as plated) CIS thin film deposited by Pulse plating on Mo wafer with potential at -0.3V, -0.7V, -0.9V, -1.1V and -1.3V at room temperature.

It can be seen that the CIS (220) peak is present in all deposition potentials, with (112) and (400) also being observed for the film deposited at -1.1V. The CuSe phase and In_2O_3 can be identified as being deposited at the two most negative potentials of -1.1V and -1.3V, whereas Se is detected at -0.3V.

From the CIS(112) peak detected at -1.1V potential, the crystallite sized shows the XRD patterns for the CIS films deposited by pulse plating at room temperature on Mo wafers. It can be seen that the CIS (220) peak is present in all deposition potentials, with (112) and (400) also being observed for the film deposited at -1.1V.

The CuSe phase and In_2O_3 can be identified as being deposited at the two most negative potentials of -1.1V and -1.3V, whereas Se is detected at -0.3V.was calculated to be about 160nm, this is larger than

the 110nm found for its DC plated counterpart. Again this result corresponds well with Section 3.2.2 on pulse plating surface morphology (as plated), where the surface of the films (Figure 25) shows little or no dendrite structure than those of DC plated Mo-wafer (Figure 24).

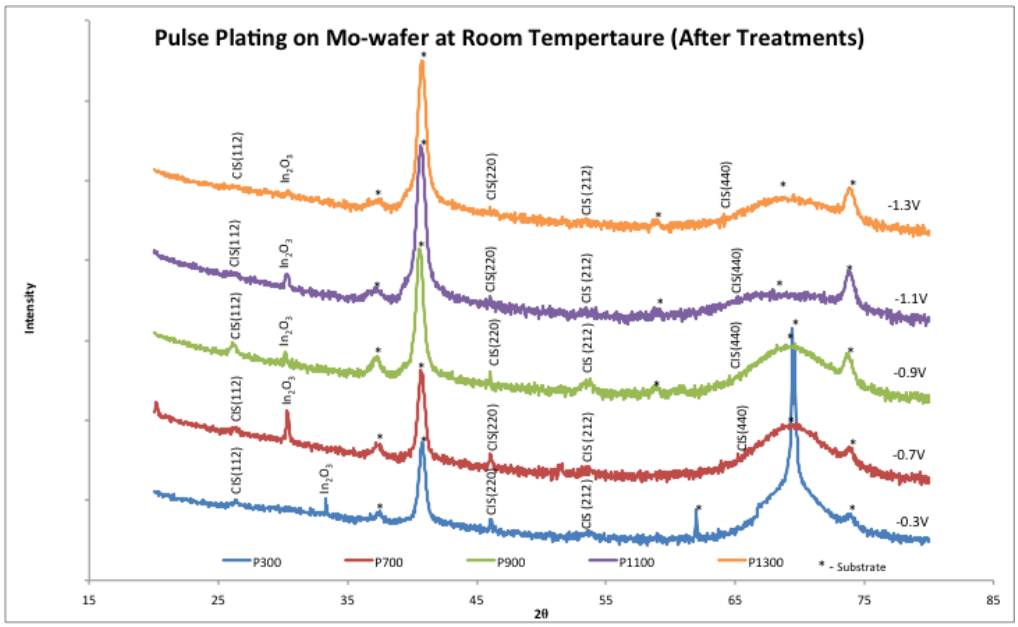


Figure 34: XRD plot of after post treatment CIS thin film deposited by Pulse plating on Mo wafer with potential at -0.3V, -0.7V, -0.9V, -1.1V and -1.3V at room temperature.

Figure 34 reveals that CuSe phase has been removed by post treatment. However, In_2O_3 compounds were still observed as these compounds might be found at the underlying layers, which would only be revealed upon etching.

Post treatment has shown to enhance the crystallinity of CIS(112) and CIS(220) phase. However, initial CIS(400) was no longer detectable after post treatment, this suggests that some of the CIS film itself was lost during etching, probably by either undermining of the excess Cu and Se phases or delamination during ultra-sonic bath in KCN etchants.

The crystallite sizes of CIS on Mo-wafer with and without post treatments were calculated and tabulated in Table 8.

Table 8: Tabulation of crystal size of CIS on Mo-wafer (as plated) before and after treatments (Annealing + KCN etch) at room temperature by pulse plating.

Crystallite size of CIS(112)	As plated/nm	After treatments/nm
Pulse Plating Mo-wafer @ -1.3V	N.A.	140
Pulse Plating Mo-wafer @ -1.1V	160	210
Pulse Plating Mo-wafer @ -0.9V	N.A.	420
Pulse Plating Mo-wafer @ -0.7V	N.A.	630
Pulse Plating Mo-wafer @ -0.3V	N.A.	450

**round off to the nearest 2 significant figure*

Generally, the crystallite sizes have increased with increasing deposition potential, except at -0.3V. This trend was also observed in Mo-strip after annealing. However, both -0.7V and -0.3V in Section 3.2.2 (Figure 27) have almost the same surface morphology where no dendrites structures were form.

Nevertheless, with lower measured grain size in Figure 27, -0.3V grains were more compact compare to -0.7V where the grains look more discrete. Thus, strain dislocation might also be experienced which results in lower increment in crystallite growth.

3.3.4 Mo-wafer by Pulse plating at 40°C

Figure 35 shows that with pulse plating on the Mo-wafer at 40°C.

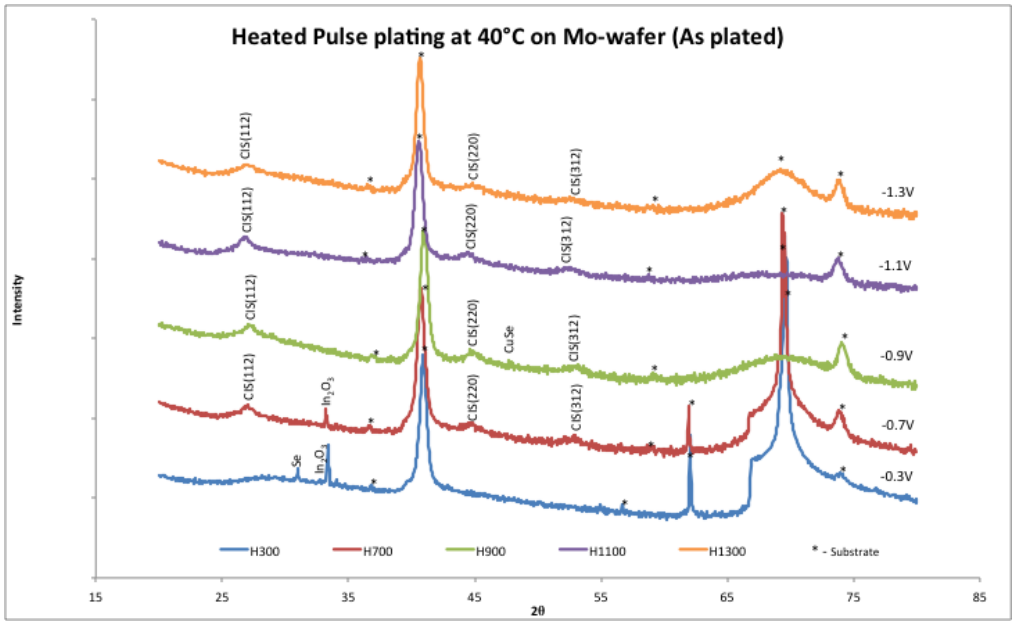


Figure 35: XRD plot of (as plated) CIS thin film deposited by Pulse plating on Mo wafer with potential at -0.3V, -0.7V, -0.9V, -1.1V and -1.3V heated bath at 40°C.

From Figure 35, CIS(112), CIS(220) and CIS(312) peaks were present across all deposition potentials except -0.3V. However, the increase in temperature also caused In_2O_3 phase to be formed at the more positive potentials of -0.3V and -0.7V as well as Se phase at -0.3V deposition potential.

Table 9: Tabulation of crystal size of CIS on Mo-wafer (as plated) by pulse plating at 40°C.

Crystallite size of CIS(112)	As plated/nm
40°C Pulse Plating Mo-wafer @ -1.3V	130
40°C Pulse Plating Mo-wafer @ -1.1V	140
40°C Pulse Plating Mo-wafer @ -0.9V	180
40°C Pulse Plating Mo-wafer @ -0.7V	210
40°C Pulse Plating Mo-wafer @ -0.3V	N.A.

**round off to the nearest 2 significant figure*

Table 9 shows that crystallite size decreases with decreasing deposition potential, and this might indicate that mass transport became the dominant process with the formation of dendrite structures (porous).

Comparing the films deposited at -1.1V by pulse plating at room temperature and 40°C, it can be seen that the crystallite size is smaller at the higher temperature (Table 8 & Table 9). This might due to the kinetics of the charge transfer process increasing with temperature (higher current density) so that the switch between charge transfer control and mass transport control occurs at a less negative potential, leading to forming dendrite structures that have smaller crystallite sizes.

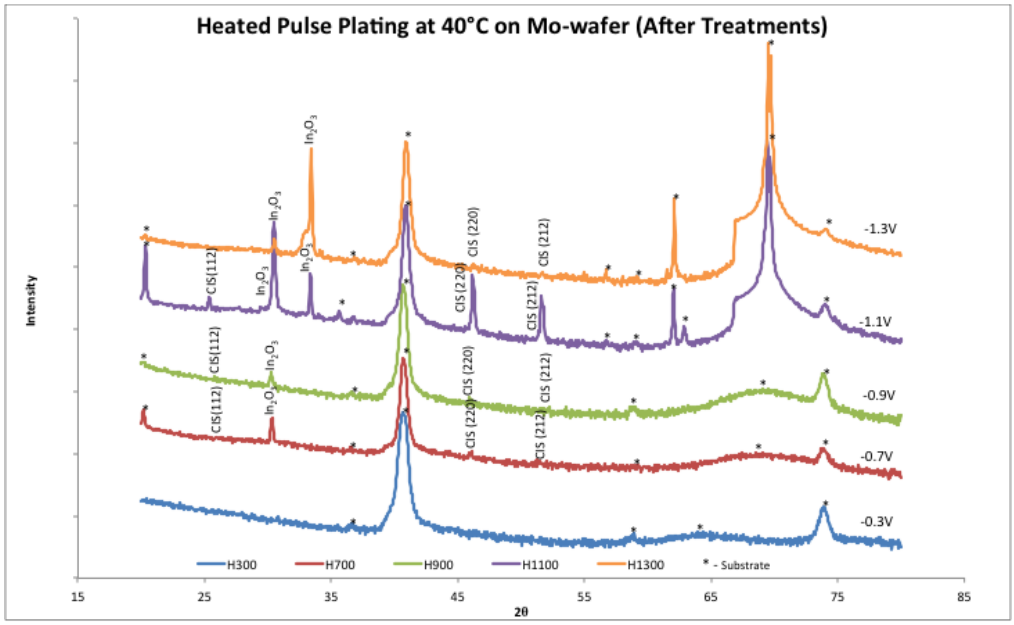


Figure 36: XRD plot of after post treatment CIS thin film deposited by Pulse plating on Mo wafer with potential at -0.3V, -0.7V, -0.9V, -1.1V and -1.3V at heated bath at 40°C.

Lastly as can be seen from Figure 36, post treatment successfully enhanced the crystallinity of the CIS film. CIS films (112), CIS (220) and CIS(312) were found at -0.7V to -1.1V. No CIS were found at -0.3V, possibly because it is absent or it thinned down during etching process (as discussed at the end of Section 3.3.4).

Post treatment has also revealed shaper and higher intensity In_2O_3 peaks from -0.7 to -1.3V. However, it is not clear if the In_2O_3 formed during the post treatments or was always present in an amorphous form.

Table 10: Tabulation of crystal size of CIS on Mo-wafer before and after treatments (Annealing + KCN etch) by pulse plating at 40°C.

Crystallite size of CIS(112)	As plated/nm	After treatments/nm
40°C Pulse Plating Mo-wafer @ -1.3V	130	N.A.
40°C Pulse Plating Mo-wafer @ -1.1V	140	630
40°C Pulse Plating Mo-wafer @ -0.9V	180	1200
40°C Pulse Plating Mo-wafer @ -0.7V	210	1600
40°C Pulse Plating Mo-wafer @ -0.3V	N.A.	N.A.

**round off to the nearest 2 significant figure*

Generally, the crystallite size of for the 40°C DC depositions at potentials -0.7V to -1.1V increased significantly after post treatments, and the crystallite sizes were the highest among all the other deposition conditions. From the micrographs shown in Figure 26, it can been that the films deposited at these three potential has dendrite structure. Hence, having dendritic structure, which is porous, growth of crystallite faces less strain, thus resulting bigger crystallite size after annealing.

In summary of XRD analysis, post treatment has successfully proven to enhance the crystallinity of the film as well as to remove the unwanted CuSe phases. Nevertheless, loss of part of the CIS film during post treatments, most likely due to undermining in the KCN etchant, revealed In_2O_3 that had not been removed by annealing or etching.

Size of the CIS crystallite increases as the deposition potential is made more positive.

3.4 ELECTRICAL CONDUCTIVITY BY PHOTOELECTRO-CHEMICAL (PEC)

Table 11 shows the values of the photovoltages of the deposited CIS films on Mo-substrates.

Table 11: PEC Photovoltage of films deposited on Mo-wafer with Pulse plating at room temperature, Pulse plating at 40°C and DC plating at room temperature.

	Deposition potential/V vs SCE	PhotoVoltage/mV	Type
Pulse plating at 40°C	-0.3	19.4	P
	-0.7	0.1	I
	-0.9	-5.7	N
	-1.1	-10.6	N
	-1.3	-7.1	N
Pulse plating at 25^{o}C	-0.3	4.5	P
	-0.7	2.7	P
	-0.9	-4.6	N
	-1.1	-9.1	N
	-1.3	-6.4	N
DC at Mo-wafer	-0.3	2.7	P
	-0.7	5	P
	-0.9	3.2	P
	-1.1	-3.3	N
	-1.3	-6.4	N

This shows that both n- and p-type layers can be obtained on CIS thin film deposited on both Mo-substrates. In heated pulse plating on MO-wafer, intrinsic (i-type) conductivity were observed at -0.7V deposition potential.

A graphical presentation is illustrated in Figure 37 for the three types of plating process for which there are PEC result as the deposition potential varies from -0.3V to -1.3V.

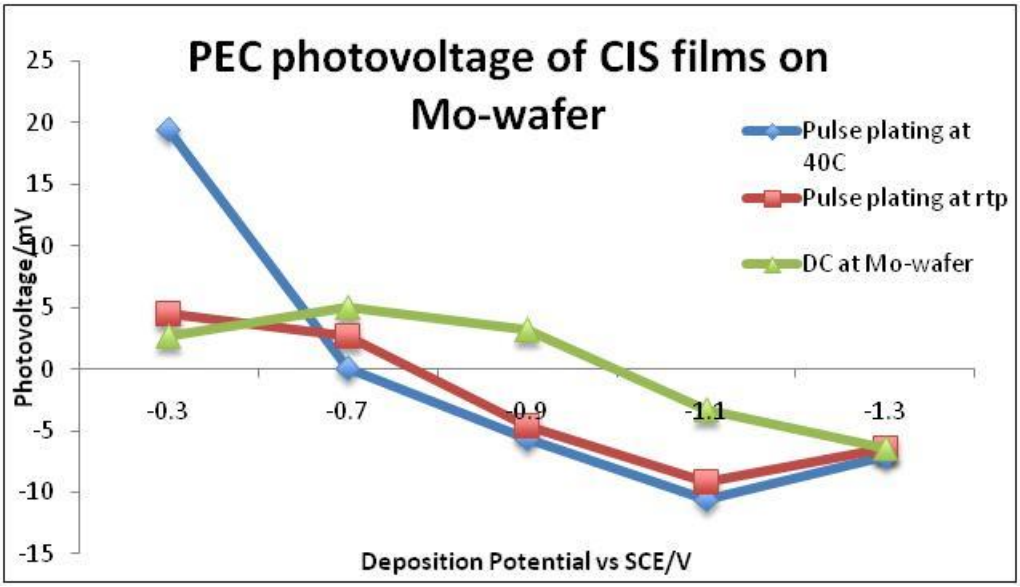


Figure 37: PEC photovoltage across DC plating at room temperature, Pulse plating at room temperature and Pulse plating at 40°C on Mo-wafer, ranging from -0.3V to -1.3 V.

It is clear from Figure 37 that at the two most positive deposition potentials (-0.3V & -0.7V) the CIS films always show p-type conductivity, which agrees with the finding of Chaure *et al.* [6]. This might due to the small amount of Indium, as revealed by the EDX (Table 2, 3 & 4) act as a p-dope material. By far the largest positive photovoltage was obtained for pulsed plating at -0.3V and a temperature of 40^{o}C.

At potentials negative of -0.9V n-type conductivity is observed for pulse plating, regardless of the temperature, this is also the case for DC plating negative of -1.1V. This might be due to the increase indium content whereby the "doping" had increase beyond the level where the layer is near a degenerate semiconductor when the Fermi level of the p-type semiconductor has been raised near to the valence band similar

to the case of a degenerate semiconductor as mention earlier in Section 1.3.

As mentioned in Valdes (2011) [21], the semiconductor characteristics of chalcopyrites depend on their non-stiochiometry and are governed by the presence of intrinsic detects such as vacancies and interstitials. For p-type films a slight excess in copper is required while n-type films involve excess indium. When exposed to illumination, the current driven is affect by the creation of electron-hole pairs which alters the concentration of the minority carriers and hence promotes processes governed by these carries. During photoexcitation, both photopotential and photocurrent can be observed even at open circuit. The photoexcited electrons and holes are separated in the space charge layer, and driven by the electric field in opposite directions. This migration induces an inverse potential in the electrode (photopotential), reducing the potential difference across the space charge layers and retarding the migration of the carriers.

In the case of p-type semiconductors, the Fermi level of the semiconductor decreases (the electrode potential increase) when the band edge level bends downward in the space charge layer. Moreover, a negative photovoltage is registered when photo-produced electron move across the space charge region towards the electrode/electrolyte interface and increase the cathodic current.

This can be further explain, as mentioned in Section 2.7, in that illumination generates an electron hole pair and the space-charge causes the holes to flow to the surface, i.e. the electrons will flow to the bulk. Under open circuit condition, the separation of the electron hold pair leads to the formation of a field which opposes that which was originally applied, whereby the bands remains "unbend". The separation of the electrons and holes causes an electric field that opposes the initial field creating a photovoltage V_{photo}, equal to the difference in the Fermi levels of semiconductor and metal far from the

junction as shown in Figure 16. The photopotential is at its maximum when flat band conditions are obtained whereby the Electron-hole pair no longer separated.

As the deposition potential is made more negative the magnitude of the photovoltage increases, although for the two pulse-plating cases the largest negative value is obtained at -1.1V. Chaure *et al* [8] noticed a similar trend, although these authors only used DC plating techniques, and suggested that the lost of photovoltage at extreme negative potentials is due to the presence of a metallic layer of indium. This explanation is consistent with the very high Indium percentages recorded by EDX at -1.3V (Table 1, 2, 3 and 4). As with the p-type samples, the largest n-type photovoltages were obtained by pulse plating, as opposed to DC methods, but in this case the solution temperature was less critical.

In summary, the photovoltage results indicate that p- and n-type layers of CIS materials can be obtained by varying the deposition potential under DC plating at room temperature, pulse plating at room temperature and pulse plating at 40°C on Mo-wafer. Typically, p-, i- and n-type layers of CIS materials can be obtained under pulse plating at 40°C on Mo-wafer, which also gives the highest photovoltages. This suggests that the best method to form a complete p-i-n junction from a single bath would be pulse plating at 40°C, with the negative plating limit cycled from -0.3V to -0.7 and finally to -1.1V.

4. CONCULSION

Copper Indium Diselenide thin film has been successfully deposited onto Mo-strip and Mo-wafer. The deposited composition of Cu, In and Se were very near theoretical values of 25:25:50 (Cu:In:Se) especially for plating done on Mo-wafers. Both p- and n-type films were achieved with the single bath deposition with minimum thickness of 100nm for pulse plating. Post treatment of annealing and KCN etch has proved to be effective to remove unwanted phases of CuSe, as well as enhancing the film crystallinity.

Photovoltage results above has indicate that p- and n-type layers of CIS materials can be obtained by varying the deposition potential under DC plating at room temperature, pulse plating at room temperature and pulse plating at 40°C on Mo-wafer. Generally, p- type can be obtain at relative high potential of -0.3V and -0.7V, where n-type can be achieve at more negative deposition potentials. However, XRD results have indicate that despite of post treatment, In_2O_3 compound will be formed and even further enhanced by annealing.

The main finding from this work is that the best method to electrochemically form CIS thin films is plating at 40°C on Mo-wafer, which gives both the best microstructure and the highest photovoltages for both n- and p-types. To form a complete p-i-n junction from a single bath at 40°C the negative plating limit of the pulse cycled from -0.3V (p-type) to -0.7V (intrinsic) and finally to -1.1V (n-type).

4.1 FUTURE WORK

This project had the ability to work on Mo sputter on Si wafer, which will be very similar to the industry process. However, it is suggested that the environmental be control further to improve on the quality of films. For example Phok, Suresh *et al* [13] used porous alumina templates to obtained CIS nanowire, the microstructure of which could be further

refine through pulse plating or possibly by using reverse pulse plating [23].

Measurements of PEC could also be performed *in situ* with sweep voltmmetry to determine flat band potentials and bandgaps [16]. Further studies can be made into investigating into absorption of energy as well as binding energy for characterization [20].

From the PEC results, p-i-n type CIS thin film can be obtained from -0.3V to -1.1, further studies can be made with more deposition potential within this range to fine tune the maximum photovolages. Further studies should also be made on formation of In_2O_3 phase in relation to the p-type conductivity of the film particularly how to avoid it; although its presence does not appear to hinder performance of the CIS films it is a waste of indium.

As mentioned in XRD diffraction results, certain grain growth were affected by the formation of dentrides structure, which may produce larger grains after post treatments due to less strains experienced. Electron Backscatter Diffraction (EBSD) is can be use to studies thin film CIS grains crystallography and strains experience on Mo back contacts on different processes.

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